SPECIAL LINEAR
REFERENCE MANUAL

SIGNAL COMPRESSION COMPONENTS • MULTIPLIERS / DIVIDERS •
RMS-TO-DC CONVERTERS • MASS STORAGE COMPONENTS •
ATE COMPONENTS • AUTOMOTIVE COMPONENTS •
MATCHED TRANSISTORS • TEMPERATURE SENSORS •
SIGNAL CONDITIONING COMPONENTS

ANALOG DEVICES

SPECIAL LINEAR
REFERENCE MANUAL

1992

Multipliers
RMS-to-DC
Sensors
Mass Storage
ATE
Automotive
ASICs

ANALOG DEVICES

How to Find Product Data in This Reference Manual

THIS VOLUME

Contains Data Sheets, Selection Guides and a wealth of background information on a wide variety of special linear components for analog signal processing.

It is one member of a five-volume set of reference manuals describing and specifying Special Linear, Amplifier, Converter and Audio/Video products from Analog Devices, Inc., in IC, hybrid and assembled form for measurement, control and real-world signal processing.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the Volume-Section-Page location of any data sheet in this volume or its companion manual, the *Amplifier Reference Manual*. You will find additional references for all other Analog Devices product categories currently available.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), you may find it by adding our "AD" prefix and looking it up in the index. Or call our nearest sales office.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your functional group in the list on the opposite page. Turn directly to the appropriate Section. You will find a functional Selection Tree and Selection Guide at the beginning of the Section. The Selection Tree and Selection Guide (and the accompanying "Orientation") will help you find the products that are the closest to satisfying your need. Use them to compare all products in the category by salient criteria. A comprehensive Table of Contents is provided for your convenience on pages 1–5 through 1–8.

IF YOU CAN'T FIND IT HERE . . . ASK!

If it's not a special linear product, it's probably in one of the four companion volumes, the *Amplifier Reference Manual*, the *Audio/Video Reference Manual* or the *Data Converter Reference Manual (Volume I* or *II)*. If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office, or phoning 1-800-262-5643.

See the Worldwide Sales Directory on pages 16–12 and 16–13 at the back of this volume for our sales office phone numbers.

Contents of Other Reference Manuals

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RE29,992, RE30,586, RE31,850, 3,729,660, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,054,829, 4,055,773, 4,056,740, 4,068,254, 4,088,905, 4,092,639, 4,092,698, 4,109,215, 4,118,699, 4,123,698, 4,131,884, 4,136,349, 4,138,671, 4,141,004, 4,142,117, 4,168,528, 4,210,830, 4,213,806, 4,228,367, 4,250,445, 4,260,911, 4,268,759, 4,270,118, 4,272,656, 4,285,051, 4,286,225, 4,309,693, 4,313,083, 4,323,795, 4,333,047, 4,338,591, 4,340,851, 4,349,811, 4,363,024, 4,374,314, 4,374,335, 4,383,222, 4,395,647, 4,399,345, 4,400,689, 4,400,690, 4,404,529, 4,427,973, 4,439,724, 4,444,309, 4,449,067, 4,454,413, 4,460,891, 4,471,321, 4,475,103, 4,475,169, 4,476,538, 4,481,708, 4,484,149, 4,485,372, 4,491,825, 4,503,381, 4,511,413, 4,521,764, 4,538,115, 4,542,349, 4,543,560, 4,543,561, 4,547,766, 4,547,961, 4,556,870, 4,558,242, 4,562,400, 4,565,000, 4,572,975, 4,583,051, 4,586,019, 4,586,155, 4,590,456, 4,596,976, 4,601,760, 4,604,532, 4,608,541, 4,622,512, 4,626,769, 4,633,165, 4,639,683, 4,644,253, 4,646,056, 4,646,238, 4,675,561, 4,677,369, 4,678,936, 4,683,423, 4,684,922, 4,685,200, 4,687,984, 4,694,276, 4,697,151, 4,703,283, 4,707,682, 4,709,167, 4,717,883, 4,722,910, 4,739,281, 4,742,331, 4,751,455, 4,752,900, 4,757,274, 4,761,636, 4,769,564, 4,771,011, 4,774,685, 4,791,318, 4,791,551, 4,800,524, 4,804,960, 4,808,908, 4,811,296, 4,814,767, 4,833,345, 4,839,653, 4,855,585, 4,855,618, 4,855,684, 4,857,862, 4,859,944, 4,862,073, 4,864,454, 4,866,505, 4,878,770, 4,879,505, 4,884,075, 4,885,585, 4,888,589, 4,891,533, 4,891,645, 4,899,152, 4,902,959, 4,904,921, 4,924,227, 4,926,178, 4,928,103, 4,928,934, 4,929,909, 4,933,572, 4,940,980, 4,957,583, 4,962,325, 4,969,823, 4,970,470, 4,973,978, 4,978,871, 4,980,634, 4,983,929, 4,985,739, 4,990,797, 4,990,803, 4,990,916, 5,008,671, 5,010,297, 5,010,337, 5,021,120, 5,026,667, 5,027,085, 5,030,849, 5,036,298, 5,036,322, 5,039,945, 5,041,795, 5,043,295, 5,043,657, 5,043,675, 5,043,732, 5,053,653, 5,055,723, 5,055,843, 5,065,144, 5,065,214, 5,070,331, 5,075,633, 5,075,677, 5,077,494, 5,077,541, 5,086,370, 5,087,889, 5,091,701, 5,095,274, 5,097,223

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General Information
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Introduction

Analog Devices, a *Fortune* 500 Industrials company, designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in real-world signal processing. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including several embodiments of CMOS, BiMOS, bipolar and hybrid integrated circuits, each optimized for specific attributes—and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies (including surface micromachining) have been utilized (and in many cases invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Our popular IC products are available in both conventional and surface-mount packages (SOIC, LCC, PLCC), and many of our assembled products employ surface-mount technology to reduce manufacturing costs and overall size. A quarter-century of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The ongoing application of today's state-of-the-art and the invention of tomorrow's state-of-the-art processes strengthen the leadership position of Analog Devices in standard data-acquisition and signal-processing products and make us a strong contender in high performance mixed-signal ASICs.

MAJOR PROGRESS

Since publication of the selection guides in the *1990/91 Linear Products Databook*, Analog Devices has introduced more than 120 significant new products; they run the gamut from brand new product and market categories and technologies to standard products (with improvements in price, performance, or design) to augmented second-source products. In addition to these new products, we now include the products of Precision Monolithics, Inc., which was acquired by Analog Devices in 1990. The combined company is the world's largest manufacturer of high-performance op amps and second in standard linear ICs. The newest special-linear products are all classified and summarized here, along with existing devices that are appropriate and desirable for use in new designs.

Examples of the variety, performance, and innovation content of outstanding new special-linear ICs to be found in this volume include:

- **ADXL50** first surface-micromachined monolithic accelerometer with on-chip signal conditioning—designed for airbag applications
- **TMP-01** programmable low power (2 mW) temperature sensor and controller, −55°C to +150°C
- **AD22150** Hall-effect gear-tooth sensor with on-chip signal conditioning outputs pulses for each tooth on a ferrous target in a magnetic field—useful in rotational speed measurements
- **AD600 and AD602** two-channel low distortion amplifiers for AGC with voltage-controlled exponential gain (0 dB to +40 dB and −10 dB to +30 dB) and 30 MHz bandwidth
- **AD800 and AD802** clock-recovery (45 MHz and 155 MHz) and data-retiming chips for phase-locked loops in data-network applications (SONET and SDH)
- **AD899** read channel-on-a-chip for hard disk drives
- **AD22001** "bulbwatcher" to detect failures in lamps and fuses, an important function in automotive applications
- **AD22050** single-supply instrumentation amplifier for hostile environments—like those found in automotive applications

Many more could have been added to this list.

SPECIAL-LINEAR REFERENCE MANUAL

This volume provides comprehensive technical data on Analog Devices analog-signal-processing products, such as multiplier/dividers, rms-to-dc converters, sensors and signal conditioners, and devices oriented to the computer, mass-storage, automotive, process control, and ATE markets. It is a companion to the *Amplifier Reference Manual*, which includes data on amplifier products, principally operational amplifiers (op amps), instrumentation amplifiers (in amps), isolation amplifiers, and comparators. Both are members of the series of Analog Devices *Reference Manuals*, which includes the *Audio/Video Reference Manual* and the two-volume *Data Converter Reference Manual*.

In the approximately 800 pages of this volume you will find:

- comprehensive data sheets and package information on 80 significant product families
- orientation material and selection guides/trees for finding products rapidly
- a representative list of available Analog Devices technical publications on real-world analog and digital signal processing
- our Worldwide Sales Directory
- the complete Product Index to all special linear and amplifier products listed in these two volumes, data conversion products listed in the *Data Converter Reference Manual* (Volumes I and II), products with audio and video signal processing applications listed in the *Audio/Video Reference Manual,* and DSP products for which data sheets are available.

The product data in this book are intended primarily for the majority of users who are concerned with new designs. For this reason, existing and available products that offer little if any unique advantage over newer products in future designs are listed in the Index, and data sheets may be available separately—but they are not published in this book.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for real-world signal processing. Besides tutorial material and comprehensive data sheets, including a large number in our Reference Manuals, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several free serial publications; for example, *Analog Productlog* provides brief information on new products being introduced, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, and test. *DSPatch*™ is a quarterly newsletter that brings its readers up-to-date applications information on our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition

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to these Reference Manual catalogs—and general short-form selection guides—we also publish several short-form catalogs on specific product families. You will find typical publications described on pages 16–8 to 16–11 at the back of the book.

SALES AND SERVICE

Backing up our design and manufacturing capabilities and our extensive array of publications, is a network of distributors, plus sales offices and representatives throughout the United States and most of the world, staffed by experienced sales and applications engineers. Our Worldwide Sales Directory, as of the publication date, appears on pages 16–12 and 16–13 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. The primary focus is a companywide Total Quality Management (TQM) Program. In addition, we maintain facilities that have been qualified under such standards as MIL-M-38510 (Class B and Class S) for ICs in the U.S., MIL-STD-1772 for hybrids, and ISO9000 (required by many European customers). Many of our products—both proprietary and second-source—have qualified for JAN part numbers; others are in the process. A larger number of products—including many of the newer ones just starting the JAN qualification process—are specifically characterized on Standard Military Drawings (SMDs). Most of our ICs are available in versions that comply with MIL-STD-883C Class B, and many also comply with Class S. We publish a *Military Products Databook* for designers who specify ICs and hybrids for military contracts. The 1990 issue consists of two volumes with data on 343 product families; the 120 entries in the second of those volumes describe qualified products manufactured by our PMI Division. A newsletter, *Analog Briefings*®, provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, these devices are suffixed "/+" and are available from stock.

PRODUCTS NOT FOUND IN THE SELECTION GUIDES

For maximum usefulness to designers of new equipment, we have limited the contents of selection guides to standard products most likely to be used for the design of new circuits and systems. If the model number of a product you are interested in is not in the Index, turn to page 16–4 at the back of this volume where you will find a list of older products for which data sheets are available upon request. On page 16–5 you will find a guide to substitutions (where possible) for products no longer available.

ICs embodying combinations of functions that you need but cannot find among our standard offerings may be available to meet your specific requirements as custom designs. Consult the section in this book on Application Specific ICs—and/or get in touch with Analog Devices.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices and distributors.

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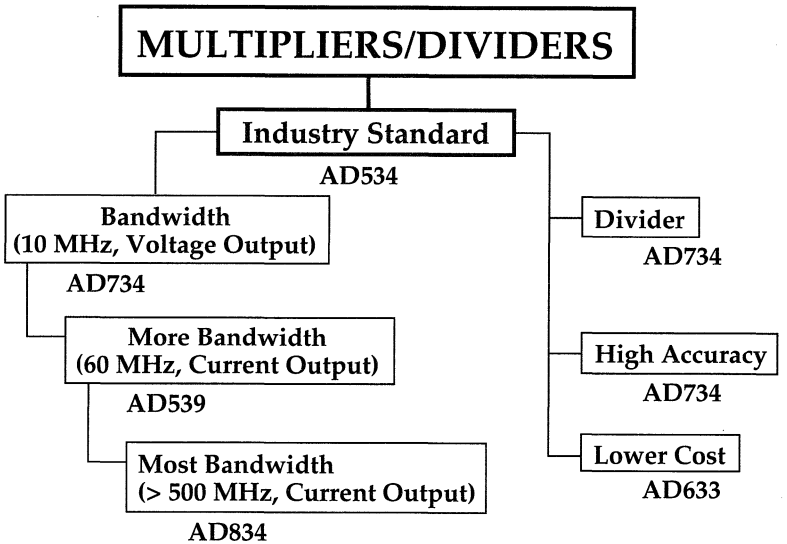
Analog Multipliers/Dividers



Selection Guides
Analog Multipliers/Dividers

Multipliers/Dividers

Model	BW MHz typ[1]	Accuracy % FS max	Supply Voltage	Output Voltage Swing	Package Options[2]	Temp Range[3]	Page	Comments
AD834	**>500**	**±2**	**+4 V to ±9 V**		**2, 3, 6**	**C, I, M**	**2–67**	**Very High Speed, 4-Quadrant Mult/Div**
AD539	**60**	**±1.5–2.5**	**±4.5 V to ±15 V**		**1, 2, 4**	**C, M**	**2–27**	**High Speed, 2-Channel, 2-Quadrant Mult/Div**
AD734	**10**	**±0.25–0.4**	**±8 V to ±16.5 V**	**±12 V min**	**2, 3**	**I, M**	**2–55**	**Very High Accuracy Replacement for AD534**
AD633	**1**	**±2**	**±8 V to ±18 V**	**±11 V min**	**2, 6**	**C**	**2–47**	**Low Cost, 4-Quadramt Multiplier**
AD532	1	±1–2	±10 V to ±22 V	±10 V min	1, 4, 7	C, M	2–9	Accurate 4-Quadrant Mult/Div
AD632	1	±0.5–1	±8 V to ±22 V	±11 V min	1, 7	I, M	2–43	High Accuracy Replacement for AD532
AD534	1	±0.25–1	±8 V to ±22 V	±11 V min	1, 4, 7	C, M	2–15	High Accuracy, 4 Quadrant Mult/Div
AD538	**0.4**	**±0.5–1**	**±4.5 V to ±18 V**	**±11 V**	**1**	**I, M**	**2–23**	**Simultaneous Mult/Div/Exponentiator**

Modulator/Demodulator

Model	Unity Gain BW MHz[1]	Gain	Slew Rate V/μs	Output Voltage Swing	Package Options[2]	Temp Range[3]	Page	Comments
AD630	**2**	**±1, ±2**	**45**	**±10 V min**	**1, 2, 4**	**C, I, M**	**2–35**	**Balanced Modulator/Demodulator with 10 V FS Output**

[1]Unity gain small signal bandwidth.
[2]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[3]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product.

Orientation
Analog Multipliers/Dividers

The devices catalogued in this section are high-performance ICs that accept analog voltages and multiply, divide, square and/or square-root them, depending on device properties and connections. Other multiplying devices available from Analog Devices include digital multipliers (*DSP data sheets available*) and multiplying D/A converters (*Data Converter Reference Manual*).

Multiplication: For two inputs, V_x and V_y, a multiplier will provide the output, $E_{out} = V_x V_y / E_{ref}$, where E_{ref} is a dimensional constant, usually of 10V nominal value. If $E_{ref} = 10V$, $E_{out} = 10V$ when V_x and V_y are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement and mathematical operations in analog computing, curve fitting and linearizing.

If the inputs may be of either positive or negative polarity and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the four quadrants of the X-Y plane.

Squaring: If $V_x = V_y = V_{in}$, a multiplier's output will be V_{in}^2/E_{ref}. A four-quadrant multiplier, used as a squarer, will have an output that is positive whether V_{in} is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads and mathematical operations.

Division: For a numerator input, V_z, and a denominator input, V_x, an analog divider will provide the output, $E_{out} = E_{ref}(V_z/V_x)$. If $E_{ref} = 10V$, E_{out} will be 10V or less for $V_z \leq V_x$. V_x is of a single polarity and will not provide meaningful results if it approaches zero too closely. If V_z may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of V_z. Analog dividers are used to compute ratios – such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements and for mathematical operations in analog computing.

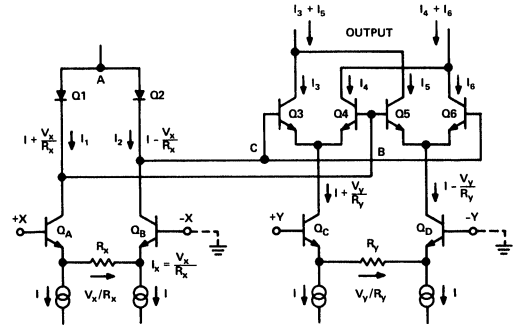
Square Rooting: For a numerator input, V_{in}, and a denominator input, E_o (the output fed back to the denominator input), the output of a divider is $E_o = E_{ref}(V_{in}/E_o)$; hence $E_o = \sqrt{E_{ref} V_{in}}$. A square rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

CHOOSING A MULTIPLIER, DIVIDER, ETC.

A number of devices are listed here, differing in internal architecture, external functional configuration and performance specifications. Most have essentially fixed references; the AD538 is a *multifunction device* that performs the one-quadrant operation, $E_o = V_z/(V_y/V_x)^m$, where m is an exponent adjustable from 1/5 to 5.

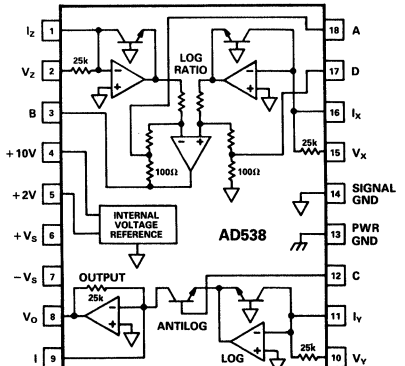
Considerable information on these functions, the nature of devices to perform them and extensive discussions of their applications can be found in the *Nonlinear Circuits Handbook*.[1] A wealth of information is also to be found in the data sheets for the individual devices published in this section. In addition to the products listed here, a number of popular earlier products are still available; data sheets are available upon request.

Internal Architecture: All of the devices in this section rely on the logarithmic properties of silicon P-N junctions. An example of the *translinear* principle that they embrace can be seen in the circuitry of a "Gilbert cell," employed in various forms for analog multiplication. Its four-quadrant multiplying circuitry and performance are described in (1), with further references to the original sources. The input voltages are converted to currents; the currents are multiplied together and divided by a reference, and the net output current, $I_x I_y / I_{ref}$, is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division.



Basic Four-Quadrant Variable-Transconductance Multiplier Circuit

$$I_O = (I_3 + I_5) - (I_4 + I_6) = \frac{2\,V_X\,V_Y}{I\,R_X\,R_Y}$$



AD538 Functional Block Diagram

In multifunction devices like the AD538, the feedback currents of the V_z and V_x input op amps are used to develop logarithmic voltages across transistor base-emitter junctions; these voltages are differenced to provide the logarithm of the ratio, V_z/V_x.

[1] ***Nonlinear Circuits Handbook*, D.H. Sheingold, ed., 1976, 536pp., $5.95, Analog Devices, Inc., P.O. Box 9106, Norwood, MA 02062-9106**

At the user's choice, this log ratio is either amplified (m>1), attenuated (m<1) or unchanged (m = 1), then applied to a product-antilog circuit which adds the logarithm of V_y, then takes the antilogarithm to produce the output equation,

$$V_{OUT} = V_y \left\{ \frac{V_z}{V_x} \right\}^m$$

Wideband Multipliers have bandwidths greatly exceeding 1MHz. The output is generally in the form of current, for maximum bandwidth (current-to-voltage conversion tends to reduce bandwidth and is unnecessary in many applications). The user can choose an appropriate external amplifier – or other circuitry – to meet the needs of the application. The AD734 is a four-quadrant multiplier/divider with a 10 MHz full power bandwidth and 0.15% satic accuracy specifications. The *AD539* is a dual multiplier/divider with two independent two-quadrant signal channels (inputs Y1 and Y2) and a common X-input, which provides linear control of gain for both channels. Signal bandwidth is 30MHz and control bandwidth is 5MHz. The *AD834* is a four-quadrant multiplier with 500MHz large-signal bandwidth and 0.5% static-accuracy specifications. It has differential X and Y inputs and differential open-collector current output. For 1-volt inputs, its differential output current is ±4mA.

External Functional Configuration: Most of the devices listed here can be used for multiplication, division, squaring and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. Performance of pretrimmed devices is optimized in specified modes of operation. The data sheets show how devices are connected for the various modes of operation; where appropriate, the suggested trim circuits and procedures for optimizing performance are provided.

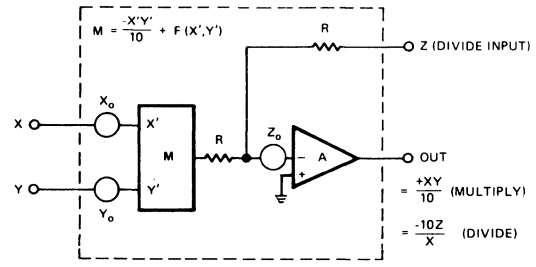
Technologies: The devices described in these two volumes are monolithic integrated circuits. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The pretrimmed ICs use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors as low as 0.15%, and high linearities.

Performance: Multiplier performance, specifications and test circuitry are described in great detail in the *Nonlinear Circuits Handbook*. Here is a brief digest of the factors relating to low-frequency performance.

An ideal multiplier has an output which is the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practical (see the simplified single-ended multiplier in the figure), a multiplier may be considered as having two parts, one (M) contains the input circuitry and the multiplying cell; the other is a gain-conditioning op amp, A.

Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The



Functional Block Diagram of Typical Multiplier/Divider

figure shows a model with 10-volt scale factor used for considering errors. X_o and Y_o are input offset voltages, Z_o is the offset-referred-to-the-input of the output amplifier, and f(X', Y') is the non-linearity, viewed as the departure from the ideal multiplication, $\frac{X'Y'}{10R}$. The output equation, including the errors is of the form

$$E_o = \frac{XY}{10B} \pm \left[\frac{X_oY}{10B} \pm \frac{XY_o}{10B} \pm Z_o + f(X,Y) \right]$$

Product; X_{offset} Linear "Y"; Y_{offset} Feedthrough "X"; Output offset; Nonlinearity and Feedthrough

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by adding external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) nonlinearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

$$f(X,Y) \cong |V_x|\epsilon_x + |V_y|\epsilon_y$$

where ϵ_x and ϵ_y are the specified fractional linearity errors (%/100) and V_x and V_Y are the input signals.

When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage ($10V/V_x$), and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (i.e., >10:1), will always benefit greatly by the trimming of offsets, especially Z_o (affects offsets) and X_o (affects gain), for small values of X.

DEFINITIONS OF SPECIFICATIONS*

Accuracy is defined in terms of *total error* of the multiplier at room temperature and constant nominal supply voltage. *Total error* includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. *Temperature dependence* and *supply-voltage effects* are specified separately.

Scale Factor: The *scale-factor error* (or *gain* error) is the difference between the average scale factor and the ideal scale factor (e.g., $(10V)^{-1}$). It is expressed in percent of the output signal. *Temperature dependence* is specified.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output *offset vs. temperature* is also specified.

Linearity Error or *Nonlinearity* is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in simple "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an *input offset* at the zero input, which can be trimmed out (but can drift and has a *temperature specification*), and a nonlinear one, which is irreducible. *Feedthrough* is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the mulitplier may improve small-signal resolution significantly.

Dynamic Parameters include: *small-signal bandwidth, full-power response, slew(ing) rate, small-signal amplitude error* and *settling time.*

Small-Signal Bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

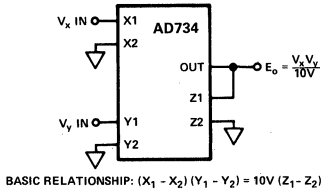
Full-Power Response is the maximum frequency at which the multiplier can produce the full-scale voltage into its rated load without noticeable distortion.

Slew(ing) Rate (V/μs) is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a full-scale step input.

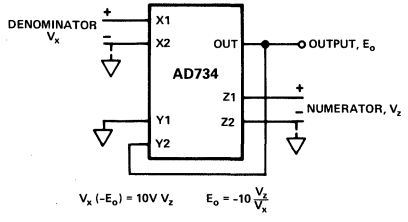
Small-Signal Amplitude Error is defined in relation to the frequency at which the amplitude response, or scale-factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Settling Time, for the product of a ±10V step and 10V dc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

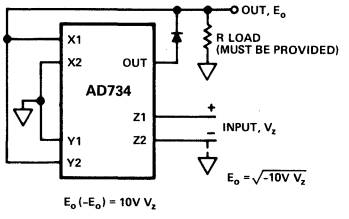
Vector Error is the most sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.



Multiplier



Divider



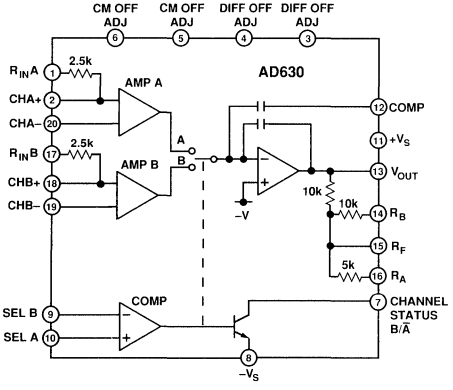
Square Rooter

***These are general definitions. Further definitions are provided as footnotes to the Specifications tables; they should be read carefully.**

MODULATORS/DEMODULATORS

AD630 Balanced Modulator/Demodulator

The AD630 is a fast, flexible, switched dual-input op amp with an on-chip comparator. Intended for wideband, low-level, and wide-dynamic-range instrumentation applications and coherent systems, it is capable of such analog signal-processing functions as balanced modulator, balanced demodulator, absolute-value amplifier, phase detector, square-wave multiplier and two-channel precision multiplexer. It can be used as a lock-in amplifier, synchronous detector, rectifier, dual-mode circuit, and much more. Essentially a complete device with on-chip scaling resistors, it can be used for these functions with little or no additional circuitry.



As a *lock-in amplifier*, it can recover a 0.1-Hz sine wave, transmitted as a modulation on a 400-Hz carrier, from a band-limited, clipped white-noise signal approximately 100,000 times larger – a dynamic range greater than 100dB.

It consists of a frequency-compensated op-amp-output stage, with two identical switched differential front ends (A and B), a differential comparator that controls the switching and a set of jumper-programmable matched precision resistors – trimmed to produce closed-loop gain accuracies to ±0.015% and gain match (between channels) to ±0.03%. When the net input to the comparator is positive, front-end A will be selected; when the comparator input is negative, front-end B is selected. A *status* output indicates the state of the comparator.

ANALOG DEVICES

Internally Trimmed Integrated Circuit Multiplier

AD532

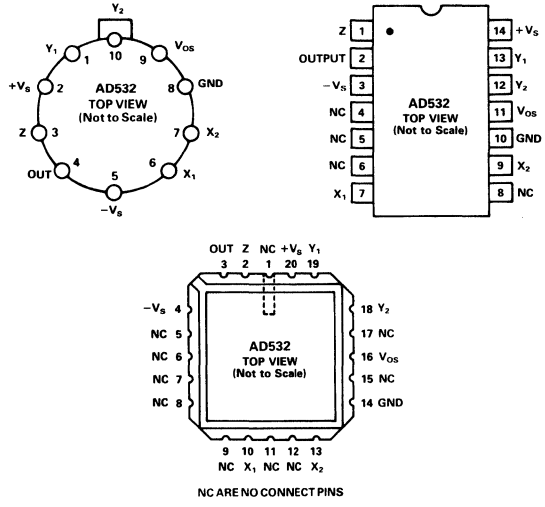
FEATURES

- Pretrimmed to ±1.0% (AD532K)
- No External Components Required
- Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
- Diff Inputs for (X_1-X_2) $(Y_1-Y_2)/10V$ Transfer Function
- Monolithic Construction, Low Cost

APPLICATIONS

- Multiplication, Division, Squaring, Square Rooting
- Algebraic Computation
- Power Measurements
- Instrumentation Applications
- Available in Chip Form

PIN CONFIGURATIONS



NC ARE NO CONNECT PINS

PRODUCT DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1-X_2)(Y_1-Y_2)/10V$, divides in two quadrants with a $10VZ/(X_1-X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10VZ}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as $XY/10V$, $(X^2-Y^2)/10V$, $\pm X^2/10V$, and $10VZ/(X_1-X_2)$ are easily attained, and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer-generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at +25°C, and are rated for operation from 0 to +70°C. The AD532S has a maximum multiplying error of ±1% of full scale at +25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of -55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can, TO-116 ceramic DIP or LCC packages. J, K and S grade chips are also available.

ADVANTAGES OF ON-THE-CHIP TRIMMING OF THE MONOLITHIC AD532

1. True ratiometric trim for improved power supply rejection.
2. Reduced power requirements since no networks across supplies are required.
3. More reliable since standard monolithic assembly techniques can be used rather than more complex hybrid approaches.
4. High impedance X and Y inputs with negligible circuit loading.
5. Differential X and Y inputs for noise rejection and additional computational flexibility.

AD532—SPECIFICATIONS (@ +25°C, V_S = ±15V, R≥2kΩ V_{OS} grounded).

Model	AD532J			AD532K			AD532S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$		
Total Error (−10V≤X, Y≤+10V)		±1.5	**±2.0**		±0.7	**±1.0**		±0.5	**±1.0**	%
T_A = min to max		±2.5			±1.5				**±4.0**	%
Total Error vs Temperature		±0.04			±0.03			±0.01	**±0.04**	%/°C
Supply Rejection (±15V ±10%)		±0.05			±0.05			±0.05		%/%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.8			±0.5			±0.5		%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.3			±0.2			±0.2		%
Feedthrough, X (Y Nulled, X = 20V pk-pk 50Hz)		50	**200**		30	**100**		30	**100**	mV
Feedthrough, Y (X Nulled, Y = 20V pk-pk 50Hz)		30	**150**		25	**80**		25	**80**	mV
Feedthrough vs. Temp.		2.0			1.0			1.0		mV p-p/°C
Feedthrough vs. Power Supply		±0.25			±0.25			±0.25		mV/%
DYNAMICS										
Small Signal BW (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error		75			75			75		kHz
Slew Rate (V_{OUT} 20 pk-pk)		45			45			45		V/μs
Settling Time (to 2%, ΔV_{OUT} = 20V)		1			1			1		μs
NOISE										
Wideband Noise f = 5Hz to 10kHz		0.6			0.6			0.6		mV (rms)
f = 5Hz to 5MHz		3.0			3.0			3.0		mV (rms)
OUTPUT										
Output Voltage Swing	±10	±13		±10	±13		±10	±13		V
Output Impedance (f≤1kHz)		1			1			1		Ω
Output Offset Voltage		±40				**±30**			**±30**	mV
Output Offset Voltage vs. Temp.		0.7			0.7				**2.0**	mV/°C
Output Offset Voltage vs. Supply		±2.5			±2.5			±2.5		mV/%
INPUT AMPLIFIERS (X, Y and Z)										
Signal Voltage Range (Diff. or CM Operating Diff)		±10			±10			±10		V
CMRR	**40**			**50**			**50**			dB
Input Bias Current										
X, Y Inputs		3			1.5	**4**		1.5	**4**	μA
X, Y Inputs T_{min} to T_{max}		10			8			8		μA
Z Input		±10			±5	**±15**		±5	**±15**	μA
Z Input T_{min} to T_{max}		±30			±25			±25		μA
Offset Current		±0.3			±0.1			±0.1		μA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\,Z/(X_1-X_2)$			$10V\,Z/(X_1-X_2)$			$10V\,Z/(X_1-X_2)$		
Total Error										
(V_X = −10V, −10V≤V_Z≤+10V)		±2			±1			±1		%
(V_X = −1V, −10V≤V_Z≤+10V)		±4			±3			±3		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$		
Total Error		±0.8			±0.4			±0.4		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function		$-\sqrt{10VZ}$			$-\sqrt{10VZ}$			$-\sqrt{10VZ}$		
Total Error (0V≤V_Z≤10V)		±1.5			±1.0			±1.0		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±10		**±18**	±10		**±18**	±10		±22	V
Supply Current										
Quiescent		4	**6**		4	**6**		4	**6**	mA

NOTE

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Thermal Characteristics:

H-10A: θ_{JC} = 25°C/W; θ_{JA} = 150°C/W

E-20A: θ_{JC} = 22°C/W; θ_{JA} = 85°C/W

D-14: θ_{JC} = 22°C/W; θ_{JA} = 85°C/W

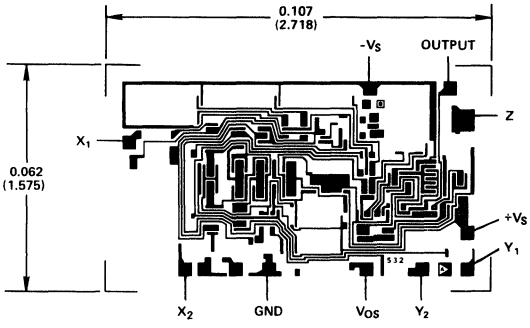
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD532JD	0°C to +70°C	Side Brazed DIP	D-14
AD532KD	0°C to +70°C	Side Brazed DIP	D-14
AD532JH	0°C to +70°C	Header	H-10A
AD532KH	0°C to +70°C	Header	H-10A
AD532J Chip	0°C to +70°C	Chip	
AD532K Chip	0°C to +70°C	Chip	
AD532SD	−55°C to +125°C	Side Brazed DIP	D-14
AD532SD/883B	−55°C to +125°C	Side Brazed DIP	D-14
JM38510/13903BCA	−55°C to +125°C	Side Brazed DIP	D-14
AD532SE	−55°C to +125°C	LCC	E-20A
AD532SE/883B	−55°C to +125°C	LCC	E-20A
AD532SH	−55°C to +125°C	Header	H-10A
AD532SH/883B	−55°C to +125°C	Header	H-10A
JM38510/13903BIA	−55°C to +125°C	Header	H-10A
AD532S Chip	−55°C to +125°C	Chip	

*For outline information see Package Information section.

CHIP DIMENSIONS AND BONDING DIAGRAM

Contact factory for latest dimensions.
Dimensions shown in inches and (mm).



FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown in Figure 1, and the complete schematic in Figure 2. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{out} = (X_1-X_2)(Y_1-Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{os} in critical applications . . . otherwise the V_{os} pin should be grounded.

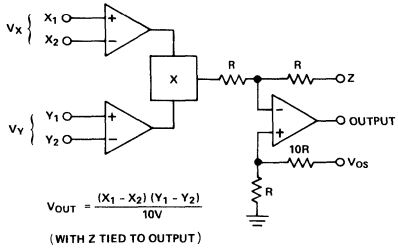


Figure 1. Functional Block Diagram

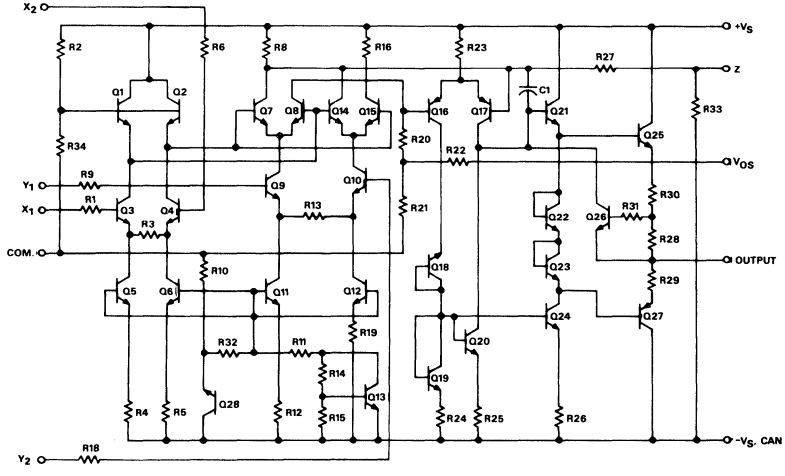


Figure 2. AD532 Schematic Diagram

AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components, since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output op amp as shown in Figure 13. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwidth and other multiplier cell errors are adversely affected. The divide error and drift are then $\epsilon_m \cdot 10V/X_1-X_2)$ where ϵ_m represents multiplier full scale error and drift, and (X_1-X_2) is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 3 and 4 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10V dc. In Figure 4 the sine wave amplitude is 20V(p-p).

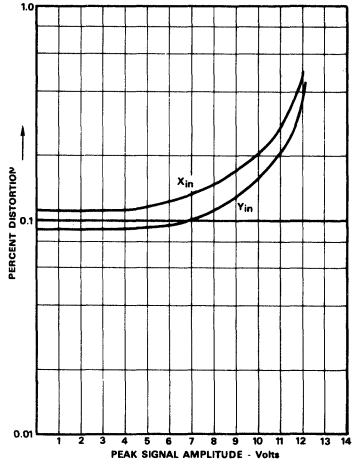


Figure 3. Percent Distortion vs. Input Signal

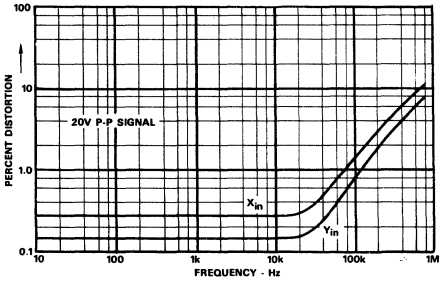


Figure 4. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC Feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 5. It is measured for the condition $V_X = 0$, $V_Y = 20V(p-p)$ and $V_Y = 0$, $V_X = 20V(p-p)$ over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

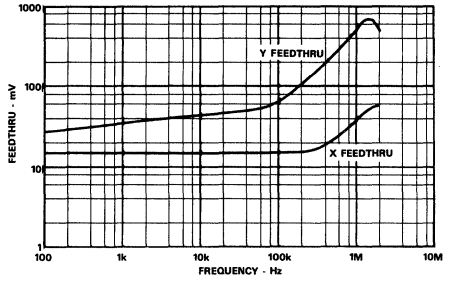


Figure 5. Feedthrough vs. Frequency

COMMON MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common mode rejection for both inputs as a function of frequency is shown in Figure 6. It is measured with $X_1 = X_2 = 20V(p-p)$, $(Y_1-Y_2) = \pm 10V$ dc and $Y_1 = Y_2 = 20V(p-p)$, $(X_1-X_2) = \pm 10V$ dc.

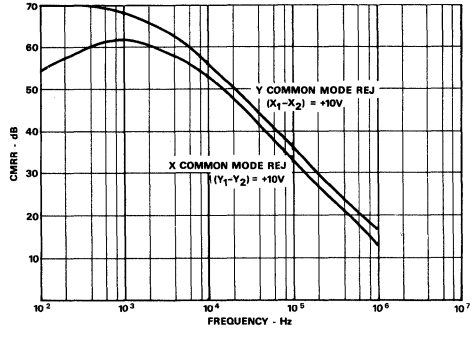


Figure 6. CMRR vs. Frequency

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls off at 6dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 7. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 8.

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

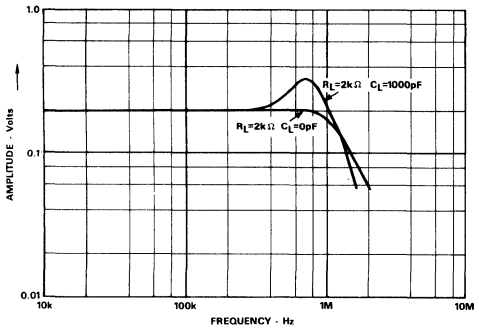


Figure 7. Frequency Response, Multiplying

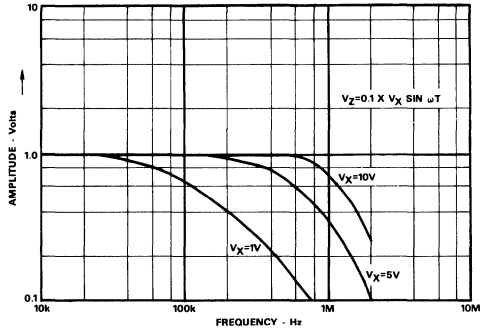


Figure 8. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15V dc supplies, it may be operated at any supply voltage from ±10V to ±18V for the J and K versions and ±10V to ±22V for the S version. The input and output signals must be reduced proportionately to prevent saturation, however, with supply voltages below ±15V, as shown in Figure 9. Since power supply sensitivity is not dependent on external null networks as in the AD530 and other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

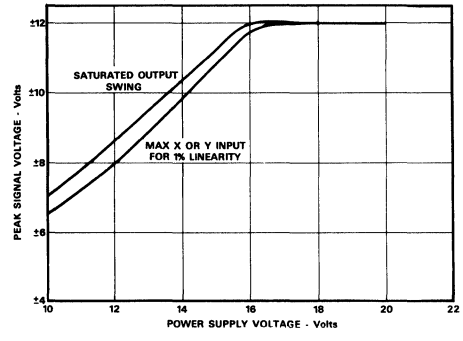


Figure 9. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532s are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 10.

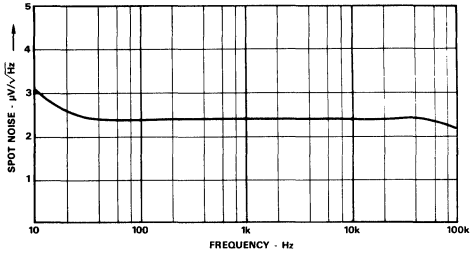


Figure 10. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks (e.g., AD530) have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks (such as the AD530) can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

For operation as a multiplier, the AD532 should be connected as shown in Figure 11. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see Figure 1). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

APPLICATIONS

MULTIPLICATION

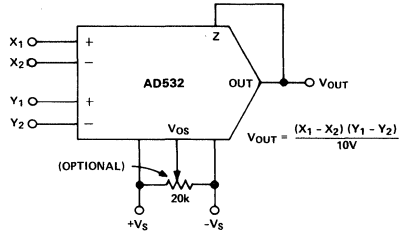


Figure 11. Multiplier Connection

The squaring circuit in Figure 12 is a simple variation of the multiplier. The differential input capability of the AD532 can be used, however, to obtain a positive or negative output response to the input....a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

SQUARE

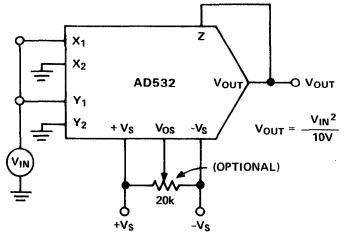


Figure 12. Squarer Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 13. It should be noted, however, that the output error is given approximately by $10V\epsilon_m/(X_1-X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \cdot (X_1-X_2)/10V$, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0V to -10V), connect the input to X and the offset null to X_2; for single-ended positive inputs (0V to +10V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

DIVISION

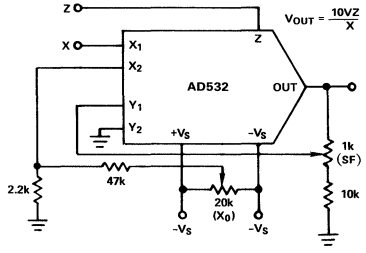


Figure 13. Divider Connection

For practical reasons, the useful range in denominator input is approximately $500mV \leq |(X_1-X_2)| \leq 10V$. The voltage offset adjust (V_{OS}), if used, is trimmed with Z at zero and (X_1-X_2) at full scale.

TABLE I

ADJUST PROCEDURE (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:	Adjust for:		With:	Adjust for:
Adjust	X	Z	V_{out}	Z	V_{out}
Scale Factor	−10V	+10V	-10V	+10V	−10V
X_o (Offset)	−1V	+0.1V	-1V	+0.1V	−1V

Repeat if required.

The connections for square root mode are shown in Figure 14. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{in} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{in} = +0.1V dc, adjusting V_{os} to obtain -1.0V dc in the output, $V_{out} = -\sqrt{10VZ}$. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

SQUARE ROOT

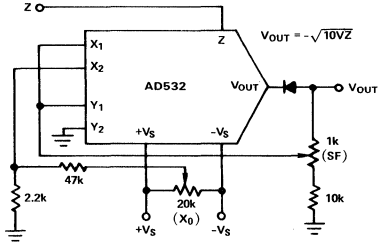


Figure 14. Square Rooter Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X^2-Y^2/10V$. As shown in Figure 15, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{in}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

DIFFERENCE OF SQUARES

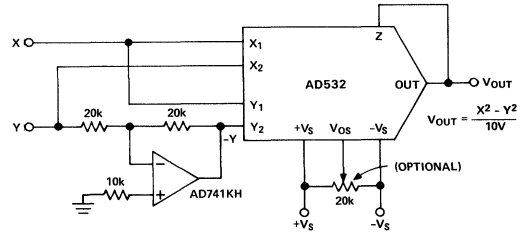


Figure 15. Differential of Squares Connection

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

AD534

FEATURES

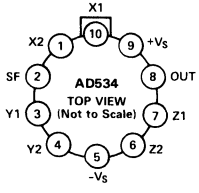
- Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
- All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10V]+Z_2$ Transfer Function
- Scale-Factor Adjustable to Provide up to X100 Gain
- Low Noise Design: 90μV rms, 10Hz–10kHz
- Low Cost, Monolithic Construction
- Excellent Long Term Stability

APPLICATIONS

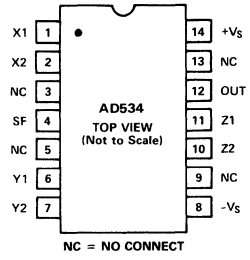
- High Quality Analog Signal Processing
- Differential Ratio and Percentage Computations
- Algebraic and Trigonometric Function Synthesis
- Wideband, High-Crest rms-to-dc Conversion
- Accurate Voltage Controlled Oscillators and Filters
- Available in Chip Form

PIN CONFIGURATIONS

TO-100 (H-10A) Package

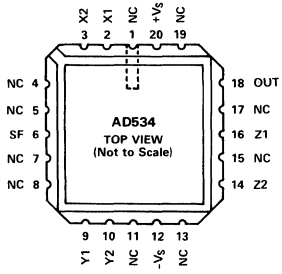


TO-116 (D-14) Package



NC = NO CONNECT

LCC (E-20A) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00V; by means of an external resistor, this can be reduced to values as low as 3V.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0 to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, -55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages. AD534J, K, S and T chips are also available.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90μV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

AD534—SPECIFICATIONS (T_A = +25°C, $\pm V_S$ = 15V, R≥2kΩ)

Model	AD534J Min	AD534J Typ	AD534J Max	AD534K Min	AD534K Typ	AD534K Max	AD534L Min	AD534L Typ	AD534L Max	Units
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] (−10V≤X, Y≤+10V)			**±1.0**			**±0.5**			**±0.25**	%
T_A = min to max		±1.5			±1.0			±0.5		%
Total Error vs Temperature		±0.022			±0.015			±0.008		%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02			±0.01			±0.005		%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	**±0.3**		±0.10	**±0.12**	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	**±0.1**		±0.005	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	**±0.3**		±0.05	**±0.12**	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	**±0.1**		±0.003	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±2	**±10**	mV
Output Offset Voltage Drift		200			100			100		μV/°C
DYNAMICS										
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20		V/μs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2		μs
NOISE										
Noise Spectral-Density SF = 10V		0.8			0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1			1			1		mV/rms
f = 10Hz to 10kHz		90			90			90		μV/rms
OUTPUT										
Output Voltage Swing	**±11**			**±11**			**±11**			V
Output Impedance (f≤1kHz)		0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]										
Signal Voltage Range (Diff. or CM		±10			±10			±10		V
Operating Diff.)		±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			50		μV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±2	**±10**	mV
Offset Voltage Drift Z		200			100			100		μV/°C
CMRR	**60**	80		**70**	90		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	μA
Offset Current		0.1			0.1			0.05	**0.2**	μA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function (X_1>X_2)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, −10V≤Z≤+10V)		±0.75			±0.35			±0.2		%
(X − 1V, −1V≤Z≤+1V)		±2.0			±1.0			±0.8		%
(0.1V≤X≤10V, −10V≤Z≤10V)		±2.5			±1.0			±0.8		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error (−10V≤X≤10V)		±0.6			±0.3			±0.2		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function (Z_1≤Z_2)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] (1V≤Z≤10V)		±1.0			±0.5			±0.25		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±8		**±18**	±8		**±18**	±8		**±18**	V
Supply Current										
Quiescent		4	**6**		4	6		4	**6**	mA

NOTES
[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

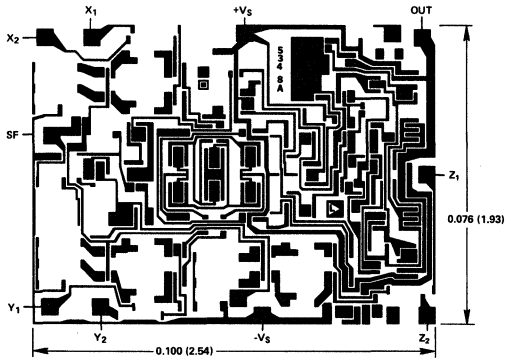
Model	AD534S Min	AD534S Typ	AD534S Max	AD534T Min	AD534T Typ	AD534T Max	Units
MULTIPLIER PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] ($-10V \le X, Y \le +10V$)			**±1.0**			**±0.5**	%
T_A = min to max			**±2.0**			**±1.0**	%
Total Error vs Temperature			**±0.02**			**±0.01**	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02				**±0.005**	%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	**±0.3**	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	**±0.3**	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift			**500**			**300**	µV/°C
DYNAMICS							
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2		µs
NOISE							
Noise Spectral-Density SF = 10V		0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1.0			1.0		mV/rms
f = 10Hz to 10kHz		90			90		µV/rms
OUTPUT							
Output Voltage Swing	**±11**			**±11**			V
Output Impedance (f ≤ 1kHz)		0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]							
Signal Voltage Range (Diff. or CM		±10			±10		V
Operating Diff.)		±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z			**500**			**300**	µV/°C
CMRR	**60**	80		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1		µA
Differential Resistance		10			10		MΩ
DIVIDER PERFORMANCE							
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, $-10V \le Z \le +10V$)		±0.75			±0.35		%
(X = 1V, $-1V \le Z \le +1V$)		±2.0			±1.0		%
($0.1V \le X \le 10V$, $-10V \le Z \le 10V$)		±2.5			±1.0		%
SQUARE PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error ($-10V \le X \le 10V$)		±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE							
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] ($1V \le Z \le 10V$)		±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS							
Supply Voltage							
Rated Performance		±15			±15		V
Operating	±8		**±22**	±8		**±22**	V
Supply Current							
Quiescent		4	**6**		4	6	mA

NOTES
[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.
Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



THE AD534 IS AVAILABLE IN LASER-TRIMMED CHIP FORM

Thermal Characteristics.

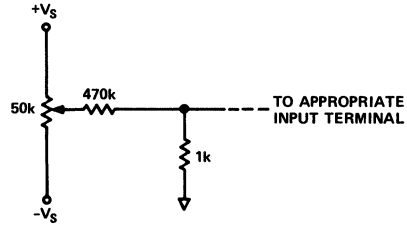
Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14 or E-20A
θ_{JA} = 95°C/W for D-14 or E-20A

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD534J specs.

OPTIONAL TRIMMING CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD534JD	0°C to +70°C	Side Brazed DIP	D-14
AD534KD	0°C to +70°C	Side Brazed DIP	D-14
AD534LD	0°C to +70°C	Side Brazed DIP	D-14
AD534JH	0°C to +70°C	Header	H-10A
AD534KH	0°C to +70°C	Header	H-10A
AD534LH	0°C to +70°C	Header	H-10A
AD534J Chip	0°C to +70°C	Chip	
AD534K Chip	0°C to +70°C	Chip	
AD534SD	−55°C to +125°C	Side Brazed DIP	D-14
AD534SD/883B	−55°C to +125°C	Side Brazed DIP	D-14
AD534TD	−55°C to +125°C	Side Brazed DIP	D-14
AD534TD/883B	−55°C to +125°C	Side Brazed DIP	D-14
JM38510/13902BCA	−55°C to +125°C	Side Brazed DIP	D-14
JM38510/13901BCA	−55°C to +125°C	Side Brazed DIP	D-14
AD534SE	−55°C to +125°C	LCC	E-20A
AD534SE/883B	−55°C to +125°C	LCC	E-20A
AD534TE	−55°C to +125°C	LCC	E-20A
AD534TE/883B	−55°C to +125°C	LCC	E-20A
AD534SH	−55°C to +125°C	Header	H-10A
AD534SH/883B	−55°C to +125°C	Header	H-10A
AD534TH	−55°C to +125°C	Header	H-10A
AD534TH/883B	−55°C to +125°C	Header	H-10A
JM38510/13902BIA	−55°C to +125°C	Header	H-10A
JM38510/13901BIA	−55°C to +125°C	Header	H-10A
AD534S Chip	−55°C to +125°C	Chip	
AD534T Chip	−55°C to +125°C	Chip	

*For outline information see Package Information section.

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4V, it is typically only ±0.05% of F.S. Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

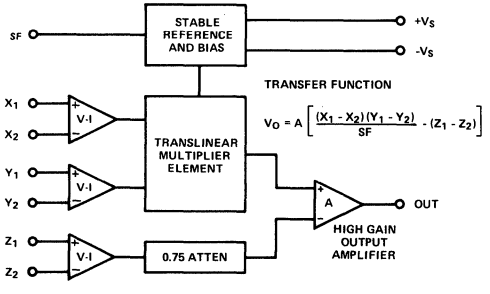


Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\left(\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right)$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak= ±1.25SF)

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite, and SF will be 10V. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10V\,(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00V and 3V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\,\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to 1.25SF (i.e., ±5V for SF = 4V) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15V are generally assumed. However, satisfactory operation is possible down to ±8V (see curve 1). Since all inputs maintain a constant peak input capability of ±1.25SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

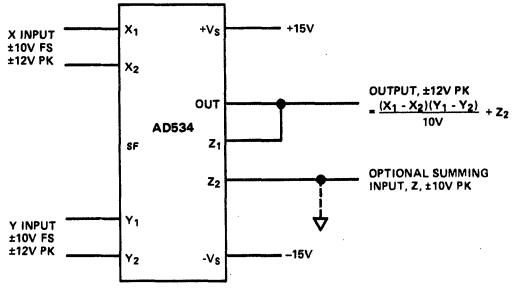


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input (see Optional Trimming Configuration, page 3). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F = 200pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300mV of trim range at the output.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10kΩ resistor, giving a gain of -9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

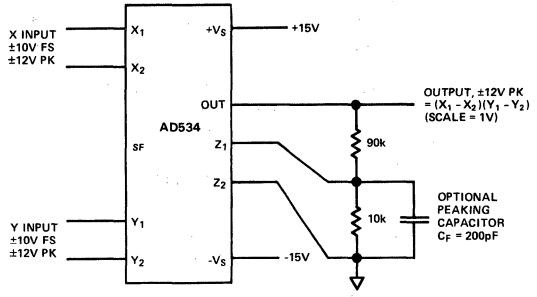


Figure 3. Connections for Scale-Factor of Unity

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

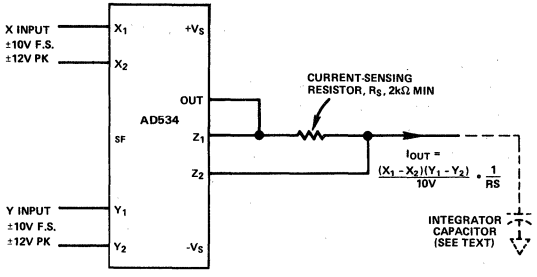


Figure 4. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1V.

If the application depends on accurate operation for inputs that are always less than ±3V, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 7).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin for pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10V to 1V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input (see Optional Trimming Configuration). To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

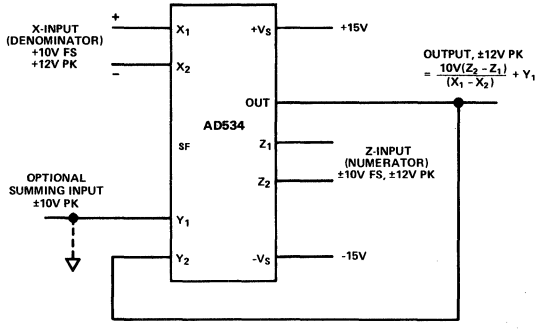


Figure 5. Basic Divider Connection

*See the AD535 Data Sheet for more details.

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

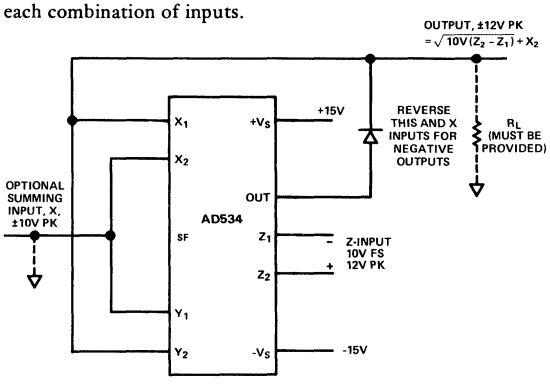


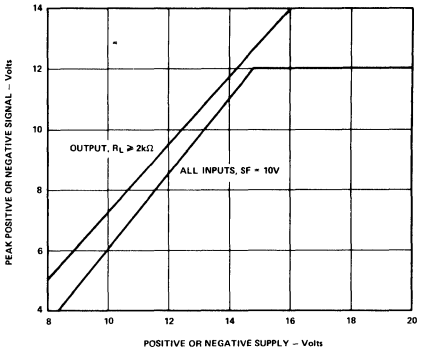
Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration) will improve accuracy for inputs below 1V.

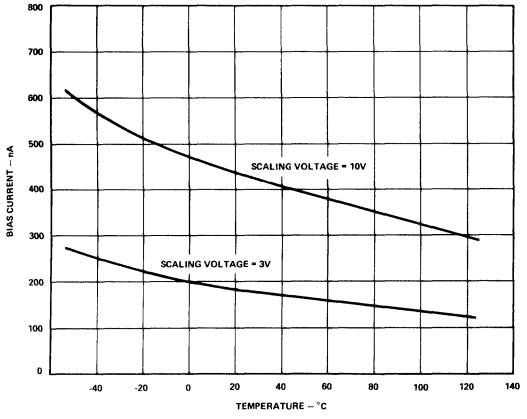
The versatility of the AD534 allows the creative designer to implement a variety of circuits such as wattmeters, frequency doublers and automatic gain controls to name but a few.

Typical Performance Curves

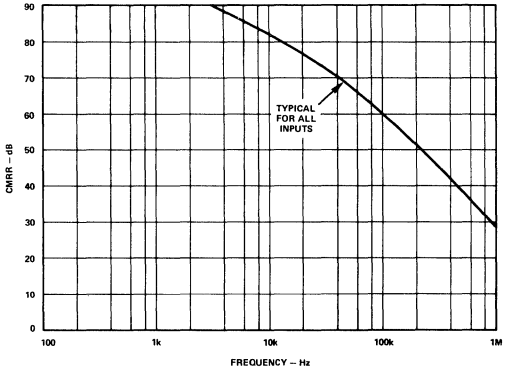
(typical at +25°C, with V_S = ±15V dc unless otherwise stated.)



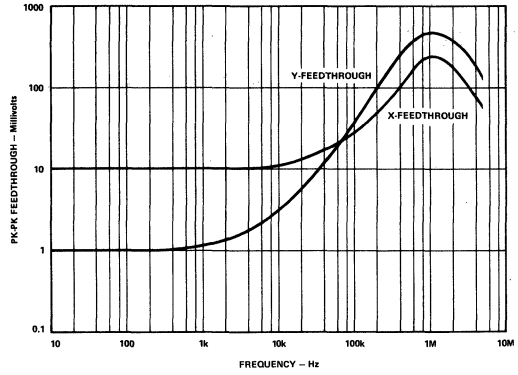
Curve 1. Input/Output Signal Range vs. Supply Voltages



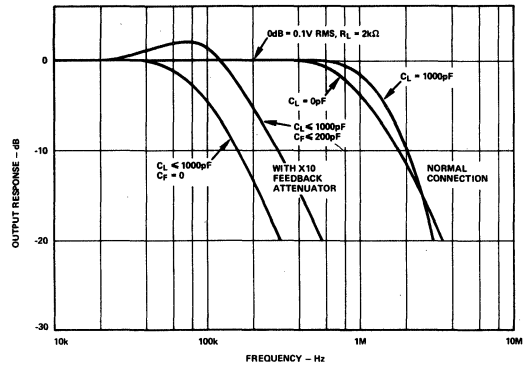
Curve 2. Bias Current vs. Temperature (X, Y or Z Inputs)



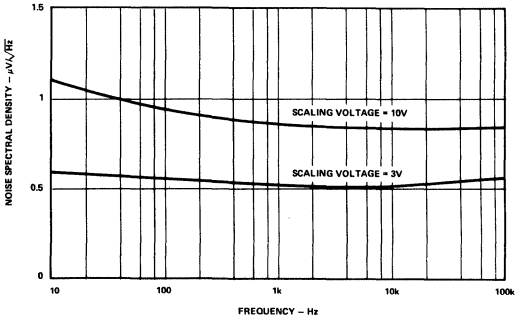
Curve 3. Common-Mode Rejection Ratio vs. Frequency



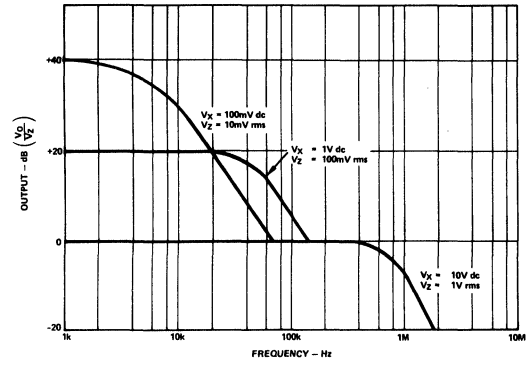
Curve 4. AC Feedthrough vs. Frequency



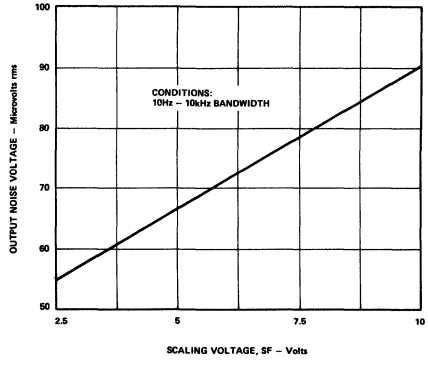
Curve 7. Frequency Response as a Multiplier



Curve 5. Noise Spectral Density vs. Frequency



Curve 8. Frequency Response vs. Divider Denominator Input Voltage



Curve 6. Wideband Noise vs. Scaling Voltages

ANALOG DEVICES

Real-Time Analog Computational Unit (ACU)

AD538

FEATURES

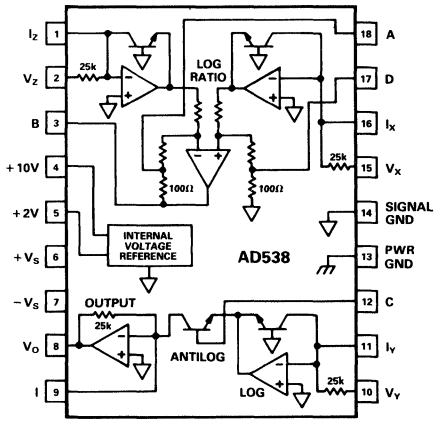
$V_{OUT} = V_Y \left(\frac{V_Z}{V_X}\right)^m$ Transfer Function

Wide Dynamic Range (Denominator) −1000:1
Simultaneous Multiplication and Division
Resistor-Programmable Powers & Roots
No External Trims Required
Low Input Offsets <100 μV
Low Error ±0.25% of Reading (100:1 Range)
+2 V and +10 V On-Chip References
Monolithic Construction

APPLICATIONS

One- or Two-Quadrant Mult/Div
Log Ratio Computation
Squaring/Square Rooting
Trigonometric Function Approximations
Linearization Via Curve Fitting
Precision AGC
Power Functions

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD538 is a monolithic real-time computational circuit which provides precision analog multiplication, division and exponentiation. The combination of low input and output offset voltages and excellent linearity results in accurate computation over an unusually wide input dynamic range. Laser wafer trimming makes multiplication and division with errors as low as 0.25% of reading possible, while typical output offsets of 100 μV or less add to the overall off-the-shelf performance level. Real-time analog signal processing is further enhanced by the device's 400 kHz bandwidth.

The AD538's overall transfer function is $V_O = V_Y (V_Z/V_X)^m$. Programming a particular function is via pin strapping. No external components are required for one-quadrant (positive input) multiplication and division. Two-quadrant (bipolar numerator) division is possible with the use of external level shifting and scaling resistors. The desired scale factor for both multiplication and division can be set using the on-chip +2 V or +10 V references, or controlled externally to provide simultaneous multiplication and division. Exponentiation with an m value from 0.2 to 5 can be implemented with the addition of one or two external resistors.

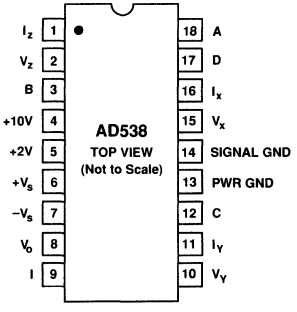
Direct log ratio computation is possible by utilizing only the log ratio and output sections of the chip. Access to the multiple summing junctions adds further to the AD538's flexibility. Finally, a wide power supply range of ±4.5 V to ±18 V allows operation from standard ±5 V, ±12 V and ±15 V supplies.

The AD538 is available in two accuracy grades (A and B) over the industrial (−25°C to +85°C) temperature range and one grade (S) over the military (−55°C to +125°C) temperature range. The device is packaged in an 18-pin TO-118 hermetic side-brazed ceramic DIP. A-grade chips are also available.

PRODUCT HIGHLIGHTS

1. Real-time analog multiplication, division and exponentiation.
2. High accuracy analog division with a wide input dynamic range.
3. On-chip +2 V or +10 V scaling reference voltages.
4. Both voltage and current (summing) input modes.
5. Monolithic construction with lower cost and higher reliability than hybrid and modular circuits.

PIN CONFIGURATION



This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

AD538—SPECIFICATIONS (V_S = ±15 V, T_A = +25°C unless otherwise specified)

Parameters	Conditions	AD538AD Min	AD538AD Typ	AD538AD Max	AD538BD Min	AD538BD Typ	AD538BD Max	AD538SD Min	AD538SD Typ	AD538SD Max	Units
MULTIPLIER/DIVIDER PERFORMANCE											
Nominal Transfer Function											
	10 V ≥ V_X, V_Y, V_Z ≥ 0		$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$		
	400 μA ≥ I_X, I_Y, I_Z ≥ 0		$V_O = 25\ k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25\ k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25\ k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$		
Total Error Terms	100 mV ≤ V_X ≤ 10 V		±0.5	**±1**		±0.25	**±0.5**		±0.5	**±1**	% of Reading +
100:1 Input Range[1]	100 mV ≤ V_Y ≤ 10 V		±200	**±500**		±100	**±250**		±200	**±500**	μV
	100 mV ≤ V_Z ≤ 10 V										
	V_Z ≤ 10 V_X, m = 1.0										
	T_A = T_{min} to T_{max}		±1	**±2**		±0.5	**±1**		±1.25	**+2.5**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	μV
Wide Dynamic Range[2]	10 mV ≤ V_X ≤ 10 V		±1	**±2**		±0.5	**±1**		±1	**±2**	% of Reading +
	1 mV ≤ V_Y ≤ 10 V		±200	**±500**		±100	**±250**		±200	**±500**	μV +
	0 mV ≤ V_Z ≤ 10 V		±100	**±250**		±750	**±150**		±200	**±250**	μV × (V_Y + V_Z)/V_X
	V_Z ≤ 10 V_X, m = 1.0										
	T_A = T_{min} to T_{max}		±1	**±3**		±1	**±2**		±2	**±4**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	μV +
			±450	±750		±350	**±500**		±750	**±1000**	μV × (V_Y + V_Z)/V_X
Exponent (m) Range	T_A = T_{min} to T_{max}	0.2		5	0.2		5	0.2		5	
OUTPUT CHARACTERISTICS											
Offset Voltage	V_Y = 0, V_C = −600 mV		±200	**±500**		±100	**±250**		±200	**±500**	μV
	T_A = T_{min} to T_{max}		±450	**±750**		±350	**±500**		±750	**±1000**	μV
Output Voltage Swing	R_L = 2 kΩ	−11		**±11**	−11		**+11**	−11		**+11**	V
Output Current		5	10		5	10		5	10		mA
FREQUENCY RESPONSE											
Slew Rate			1.4			1.4			1.4		V/μs
Small Signal Bandwidth	100 mV ≤ 10 V_Y, V_Z, V_X ≤ 10 V		400			400			400		kHz
VOLTAGE REFERENCE											
Accuracy	V_{REF} = 10 V or 2 V		±25	**±50**		±15	**±25**		±25	**±50**	mV
Additional Error	T_A = T_{min} or T_{max}		±20	**±30**		±20	**±30**		±30	**±50**	mV
Output Current	V_{REF} = 10 V to 2 V	**1**	2.5		**1**	2.5		**1**	2.5		mA
Power Supply Rejection											
+2 V = V_{REF}	±4.5 V ≤ V_S ≤ ±18 V		300	**600**		300	**600**		300	**600**	μV/V
+10 V = V_{REF}	±13 V ≤ V_S ≤ ±18 V		200	**500**		200	**500**		200	**500**	μV/V
POWER SUPPLY											
Rated	R_L = 2 kΩ		±15			±15			±15		V
Operating Range[3]		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
PSRR	±4.5 V < V_S < ±18 V		0.5	**0.1**		0.05	**0.1**		0.5	**0.1**	%/V
	V_X = V_Y = V_Z = 1 V										
	V_{OUT} = 1 V										
Quiescent Current			4.5	**7**		4.5	**7**		4.5	**7**	mA
TEMPERATURE RANGE											
Rated		−25		+85	−25		+85	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS[4]											
Ceramic (D-18)			AD538AD			AD538BD			AD538SD AD538SD/883B		
Chips			AD538A Chips								

NOTES

[1]Over the 100 mV to 10 V operating range total error is the sum of a percent of reading term and an output offset. With this input dynamic range the input offset contribution to total error is negligible compared to the percent of reading error. Thus, it is specified indirectly as a part of the percent of reading error.

[2]The most accurate representation of total error with low level inputs is the summation of a percent of reading term, an output offset and an input offset multiplied by the incremental gain (V_Y + V_Z)/V_X.

[3]When using supplies below ±13 V the 10 V reference pin *must* be connected to the 2 V pin in order for the AD538 to operate correctly.

[4]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

RE-EXAMINATION OF MULTIPLIER/DIVIDER ACCURACY

Traditionally, the "accuracy" of (actually the errors of) analog multipliers and dividers have been specified in terms of percent of full scale. Thus specified, a 1% multiplier error with a 10 V full-scale output would mean a worst case error of +100 mV at "any" level within its designated output range. While this type of error specification is easy to test, evaluate, and interpret, it can leave the user guessing as to how useful the multiplier actually is at low output levels, those approaching the specified error limit (in this case) 100 mV.

The AD538's error sources do not follow the percent of full-scale approach to specification, thus it more optimally fits the needs of the very wide dynamic range applications for which it is best suited. Rather than as a percent of full scale, the AD538's error as a multiplier or divider for a 100:1 (100 mV to 10 V) input range is specified as the sum of two error components: a percent of reading (ideal output) term plus a fixed output offset. Following this format the AD538AD, operating as a multiplier or divider with inputs down to 100 mV, has a maximum error of ±1% of reading ±500 μV. Some sample total error calculations for both grades over the 100:1 input range are illustrated in the chart below. This error specification format is a familiar one to designers and users of digital voltmeters where error is specified as a percent of reading ± a certain number of digits on the meter readout.

For operation as a multiplier or divider over a wider dynamic range (>100:1), the AD538 has a more detailed error specification which is the sum of three components: a percent of reading term, an output offset term and an input offset term for the V_Y/V_X log ratio section. A sample application of this specification, taken from the chart below, for the AD538AD with V_Y = 1 V, V_Z = 100 mV and V_X = 10 mV would yield a maximum error of ±2.0% of reading ±500 μV ±(1 V + 100 mV)/10 mV × 250 μV or ±2.0% of reading ±500 μV ± 27.5 mV. This example illustrates that with very low level inputs the AD538's incremental gain $(V_Y + V_Z)/V_X$ has increased to make the input offset contribution to error substantial.

AD538 SAMPLE ERROR CALCULATION CHART (Worst Case)

	V_Y Input (in V)	V_Z Input (in V)	V_X Input (in V)	Ideal Output (in V)	Total Offset Error Term (in mV)	% of Reading Error Term (in mV)	Total Error Summation (in mV)	Total Error Summation as a % of the Ideal Output
100:1 INPUT RANGE	10	10	10	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
Total Error = ±% rdg ±Output V_{OS}	10	0.1	0.1	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
	1	1	1	1	0.5 (AD) 0.25 (BD)	10 (AD) 5 (BD)	10.5 (AD) 5.25 (BD)	1.05 (AD) 0.5 (BD)
	0.1	0.1	0.1	0.1	0.5 (AD) 0.25 (BD)	1 (AD) 0.5 (BD)	1.5 (AD) 0.75 (BD)	1.5 (AD) 0.75 (BD)
WIDE DYNAMIC RANGE	1	0.10	0.01	10	28 (AD) 16.75 (BD)	200 (AD) 100 (BD)	228 (AD) 116.75 (BD)	2.28 (AD) 1.17 (BD)
Total Error = ±% rdg ±Output V_{OS}	10	0.05	2	0.25	1.76 (AD) 1 (BD)	5 (AD) 2.5 (BD)	6.76 (AD) 3.5 (BD)	2.7 (AD) 1.4 (BD)
±Input V_{OS} × $(V_Y+V_Z)/V_X$	5	0.01	0.01	5	125.75 (AD) 75.4 (BD)	100 (AD) 50 (BD)	225.75 (AD) 125.4 (BD)	4.52 (AD) 2.51 (BD)
	10	0.01	0.1	1	25.53 (AD) 15.27 (BD)	20 (AD) 10 (BD)	45.53 (AD) 25.27 (BD)	4.55 (AD) 2.53 (BD)

ABSOLUTE MAXIMUM RATINGS

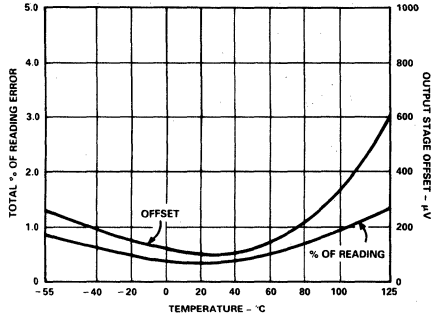
Supply Voltage . . . . . ±18 V
Internal Power Dissipation . . . . . 250 mW
Output Short Circuit-to-Ground . . . . . Indefinite
Input Voltages V_X, V_Y, V_Z . . . . . (+V_S −1 V), −1 V
Input Currents I_X, I_Y, I_Z, I_O . . . . . 1 mA
Operating Temperature Range . . . . . −25°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Storage . . . . . 60 sec, +300°C
Thermal Resistance
θ_{JC} . . . . . .35°C/W
θ_{JA} . . . . . 120°C/W

ORDERING GUIDE

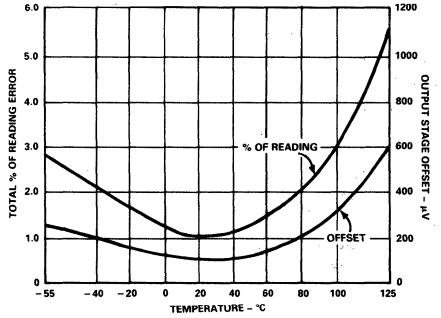
Model	Temperature Range	Package Description*
AD538AD	−25°C to +85°C	Side-Brazed Ceramic DIP
AD538BD	−25°C to +85°C	Side-Brazed Ceramic DIP
AD538A Chips	−25°C to +85°C	Chips
AD538SD	−55°C to +125°C	Side-Brazed Ceramic DIP
AD538SD/883B	−55°C to +125°C	Side-Brazed Ceramic DIP

*For outline information see Package Information section.

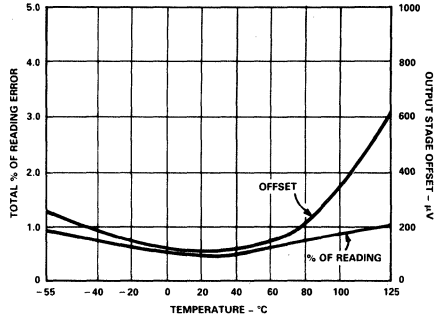
AD538—Typical Characteristics



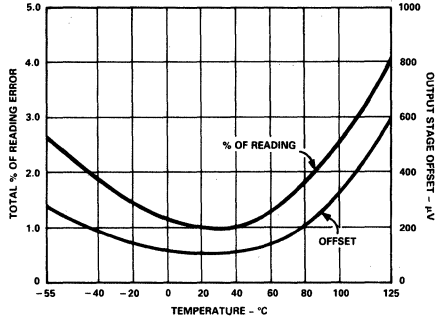
Multiplier Error vs. Temperature (100 mV < V_X, V_Y, V_Z ≤ 10 V)



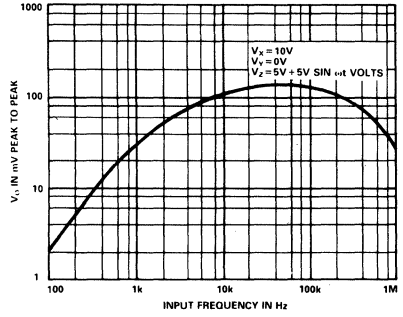
Multiplier Error vs. Temperature (10 mV < V_X, V_Y, V_Z ≤ 100 mV)



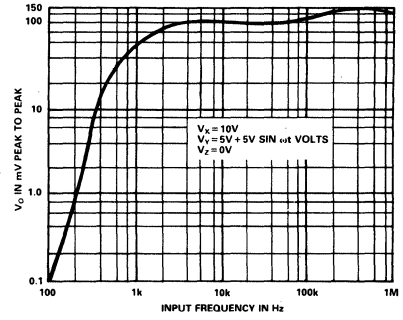
Divider Error vs. Temperature (100 mV < V_X, V_Y, V_Z ≤ 10 V)



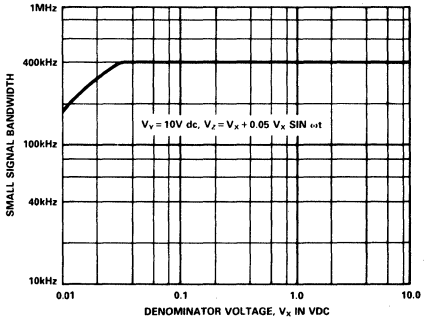
Divider Error vs. Temperature (10 mV < V_X, V_Y, V_Z ≤ 100 mV)



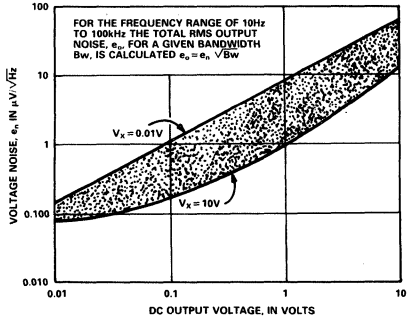
V_Z Feedthrough vs. Frequency



V_Y Feedthrough vs. Frequency



Small Signal Bandwidth vs. Denominator Voltage (One-Quadrant Mult/Div)



1 kHz Output Noise Spectral Density vs. DC Output Voltage

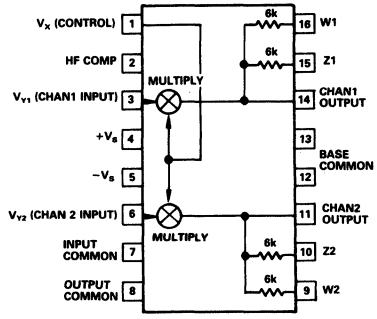
Wideband Dual-Channel Linear Multiplier/Divider

AD539

FEATURES
Two Quadrant Multiplication/Division
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Linear Control Channel Bandwidth of 5MHz
Low Distortion (to 0.01%)
Fully-Calibrated, Monolithic Circuit

APPLICATIONS
Precise High Bandwidth AGC and VCA Systems
Voltage-Controlled Filters
Video-Signal Processing
High-Speed Analog Division
Automatic Signal-Leveling
Square-Law Gain/Loss Control

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD539 is a low-distortion analog multiplier having two identical signal channels (Y1 and Y2), with a common X-input providing linear control of gain. Excellent ac characteristics up to video frequencies and a 3dB bandwidth of over 60MHz are provided. Although intended primarily for applications where speed is important the circuit exhibits good static accuracy in "computational" applications. Scaling is accurately determined by a band-gap voltage reference and all critical parameters are laser-trimmed during manufacture.

The full bandwidth can be realized over most of the gain range using the AD539 with simple resistive loads of up to 100Ω. Output voltage is restricted to a few hundred millivolts under these conditions. Using external op amps such as the AD5539 in conjunction with the on-chip scaling resistors, accurate multiplication can be achieved, with bandwidths typically as high as 50MHz.

The two channels provide flexibility. In single-channel applications they may be used in parallel, to double the output current, or in series, to achieve a square-law gain function with a control range of over 100dB, or differentially, to reduce distortion. Alternatively, they may be used independently, as in audio stereo applications, with low crosstalk between channels. Voltage-controlled filters and oscillators using the "state-variable" approach are easily designed, taking advantage of the dual channels and common control. The AD539 can also be configured as a divider with signal bandwidths up to 15MHz.

Power consumption is only 135mW using the recommended ±5V supplies. The AD539 is available in three versions: the "J" and "K" grades are specified for 0 to +70°C operation and "S" grade is guaranteed over the extended range of −55°C to +125°C. The J and K grades are available in either a hermetic ceramic DIP (D) or a low cost plastic DIP (N), while the S grade is available in ceramic DIP (D) or LCC (E). J-grade chips are also available. The S grade is now available in MIL-STD-883 and Standard Military Drawing (DESC) Number 5962–8980901EA versions.

DUAL SIGNAL CHANNELS

The signal voltage inputs, V_{Y1} and V_{Y2}, have nominal full-scale (FS) values of ±2V with a peak range to ±4.2V (using a negative supply of 7.5V or greater). For video applications where differential phase is critical a reduced input range of ±1 volt is recommended, resulting in a phase variation of typically ±0.2° at 3.579MHz for full gain. The input impedance is typically 400kΩ shunted by 3pF. Signal channel distortion is typically well under 0.1% at 10kHz and can be reduced to 0.01% by using the channels differentially.

COMMON CONTROL CHANNEL

The control channel accepts positive inputs, V_X, from 0 to +3V FS, ±3.3V peak. The input resistance is 500Ω. An external, grounded capacitor determines the small-signal bandwidth and recovery time of the control amplifier; the minimum value of 3nF allows a bandwidth at mid-gain of about 5MHz. Larger compensation capacitors slow the control channel but improve the high-frequency performance of the signal channels.

FLEXIBLE SCALING

Using either one or two external op amps in conjunction with the on-chip 6kΩ scaling resistors, the output currents (nominally ±1mA FS, ±2.25mA peak) can be converted to voltages with accurate transfer functions of $V_W = -V_X V_Y/2$, $V_W = -V_X V_Y$ or $V_W = -2V_X V_Y$ (where inputs V_X and V_Y and output V_W are expressed in volts), with corresponding full-scale outputs of ±3V, ±6V and ±12V. Alternatively, low-impedance grounded loads can be used to achieve the full signal bandwidth of 60MHz, in which mode the scaling is less accurate.

AD539—SPECIFICATIONS (@ T_A = 25°C, V_S = ±5V, unless otherwise noted)

Parameter	Conditions	AD539J Min	AD539J Typ	AD539J Max	AD539K Min	AD539K Typ	AD539K Max	AD539S Min	AD539S Typ	AD539S Max	Units
SIGNAL-CHANNEL DYNAMICS											
Minimal Configuration	Reference Figure 6a										
Bandwidth, −3dB	R_L = 50Ω, C_C = 0.01μF	30	60		30	60		30	60		MHz
Maximum Output	+0.1V<V_X< +3V, $V_Y$ac = 1V rms		−10			−10			−10		dBm
Feedthrough, f<1MHz	V_X = 0, $V_Y$ac = 1.5V rms		−75			−75			−75		dBm
f = 20MHz			−55			−55			−55		dBm
Differential Phase Linearity											
−1V<$V_Y$dc< +1V	f = 3.58MHz, V_X = +3V,		±0.2			±0.2			±0.2		Degrees
−2V<$V_Y$dc< +2V	$V_Y$ac = 100mV		±0.5			±0.5			±0.5		Degrees
Group Delay	V_X = +3V, $V_Y$ac = 1V rms, f = 1MHz		4			4			4		ns
Standard Dual-Channel Multiplier	Reference Figure 2										
Maximum Output	V_X = +3V, $V_Y$ac = 1.5V rms		4.5			4.5			4.5		V
Feedthrough, f<100kHz	V_X = 0, $V_Y$ac = 1.5V rms		1			1			1		mV rms
Crosstalk (CH1 to CH2)	V_{Y1} = 1V rms, V_{Y2} = 0										
	V_X = +3V, f<100kHz		−40			−40			−40		dB
RTO Noise, 10Hz to 1MHz	V_X = +1.5V, V_Y = 0, Figure 2		200			200			200		nV/√Hz
THD + Noise, V_X = +1V,	f = 10kHz, $V_Y$ac = 1V rms		0.02			0.02			0.02		%
V_Y = +3V	f = 10kHz, $V_Y$ac = 1V rms		0.04			0.04			0.04		%
Wide Band Two-Channel Multiplier	Figure 2										
Bandwidth, −3dB (LH0032)	+0.1V<V_X< +3V, $V_Y$ac = 1V rms		25			25			25		MHz
Maximum Output V_X = +3V	$V_Y$ac = 1.5V rms, f = 3MHz		4.5			4.5			4.5		V rms
Feedthrough V_X = 0V	$V_Y$ac = 1.0V rms, f = 3MHz		14			14			14		mV rms
Wide Band Single Channel VCA											
(AD5539)	Reference Figure 8										
Bandwidth, −3dB	+0.1V<V_X< +3V, $V_Y$ac = 1V rms		50			50			50		MHz
Maximum Output	75Ω Load		±1			±1			±1		V
Feedthrough	V_X = −0.01V, f = 5MHz		−54			−54			−54		dB
CONTROL CHANNEL DYNAMICS											
Bandwidth, −3dB	C_C = 3000pF, $V_X$dc = +1.5V,										
	$V_X$ac = 100mV rms		5			5			5		MHz
SIGNAL INPUTS, V_{Y1} & V_{Y2}											
Nominal Full-Scale Input			±2			±2			±2		V
Operational Range, Degraded Performance	$-V_S$≤7V	±4.2			±4.2			±4.2			V
Input Resistance			400			400			400		kΩ
Bias Current			10	30		10	20		10	30	μA
Offset Voltage	V_X = +3V, V_Y = 0		5	20		5	10		5	20	mV
(T_{min} to T_{max})			10			5			15	35	mV
Power Supply Sensitivity	V_X = +3V, V_Y = 0		2			2			2		mV/V
CONTROL INPUT, V_X											
Nominal Full-Scale Input			+3.0			+3.0			+3.0		V
Operational Range, Degraded Performance		+3.2			+3.2			+3.2			V
Input Resistance[1]			500			500			500		Ω
Offset Voltage			1	4		1	2		1	4	mV
(T_{min} to T_{max})			3			2			2	5	mV
Power Supply Sensitivity			30			30			30		μV/V
Gain	(Figure 2)										
Absolute Gain Error	V_X = +0.1V to +3.0V and		0.2	0.4		0.1	0.2		0.2	0.4	dB
(T_{min} to T_{max})	V_y = ±2V		0.3			0.15			0.25	0.5	dB
CURRENT OUTPUT[1]											
Full-Scale Output Current	V_X = +3V, V_Y = ±2V		±1			±1			±1		mA
Peak Output Current	V_X = +3.3V, V_Y = ±5V, V_S = ±7.5V	±2	±2.8		±2	±2.8		±2	±2.8		mA
Output Offset Current	V_X = 0, V_Y = 0		0.2	1.5		0.2	1.5		0.2	1.5	μA
Output Offset Voltage[2]	Figure 2, V_X = 0, V_Y = 0		3	10		3	10		3	10	mV
Output Resistance[1]			1.2			1.2			1.2		kΩ
Scaling Resistors											
CH1	Z1, W1 to CH1		6			6			6		kΩ
CH2	Z2, W2 to CH2		6			6			6		kΩ
VOLTAGE OUTPUTS, V_{W1} & V_{W2}[2]	(Figure 2)										
Multiplier Transfer Function,			$V_W = -V_X \cdot V_Y/V_U$			$V_W = -V_X \cdot V_Y/V_U$			$V_W = -V_X \cdot V_Y/V_U$		
Either Channel											
Multiplier Scaling Voltage, V_U		0.98	1.0	1.02	0.99	1.0	1.01	0.98	1.0	1.02	V
Accuracy			0.5	2		0.5	1		0.5	2	%
(T_{min} to T_{max})			1			0.5			1.0	3	%
Power Supply Sensitivity			0.04			0.04			0.04		%/V
Total Multiplication Error[3]	V_X< = +3V, −2V<V_Y<2V		1	2.5		0.6	1.5		1	2.5	% FSR
T_{min} to T_{max}			2			1			2	4	%
Control Feedthrough	V_X = 0 to +3V, V_Y = 0		25	60		15	30		15	60	mV
T_{min} to T_{max}			30			15			60	120	mV
TEMPERATURE RANGE											
Rated Performance		0		+70	0		+70	−55		+125	°C
POWER SUPPLIES											
Operational Range		±4.5		±15	±4.5		±15	±4.5		±15	V
Current Consumption											
+V_S			8.5	10.2		8.5	10.2		8.5	10.2	mA
−V_S			18.5	22.2		18.5	22.2		18.5	22.2	mA

NOTES

[1]Resistance value and absolute current outputs subject to 20% tolerance.

[2]Spec assumes the external op amp is trimmed for negligible input offset.

[3]Includes all errors.

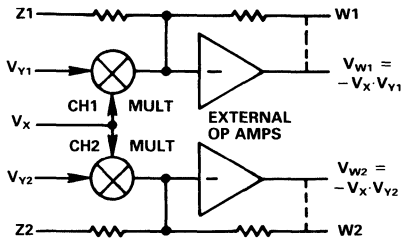
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option[1]
AD539JN	0°C to +70°C	Plastic DIP	N-16
AD539KN	0°C to +70°C	Plastic DIP	N-16
AD539JD	0°C to +70°C	Side Brazed DIP	D-16
AD539KD	0°C to +70°C	Side Brazed DIP	D-16
AD539J Chip	0°C to +70°C	Chip	
AD539SD	−55°C to +125°C	Side Brazed DIP	D-16
AD539SD/883B	−55°C to +125°C	Side Brazed DIP	D-16
5962–8980901EA[2]	−55°C to +125°C	Side Brazed DIP	D-16
AD539SE/883B	−55°C to +125°C	LCC	E-20A

NOTES
[1]For outline information see Package Information section.
[2]The standard military drawing version of the AD539 (5962–8980901EA) is now available.



AD539 Functional Block Diagram

CIRCUIT DESCRIPTION

Figure 1 is a simplified schematic of the AD539. Q1-Q6 are large-geometry transistors designed for low distortion and low noise. Emitter-area scaling further reduces distortion: Q1 is 3 times larger than Q2; Q4, Q5 are each 3 times larger than Q3, Q6, and these transistors are twice as large as Q1, Q2. A stable reference current I_{REF} = 1.375mA is produced by a band-gap reference circuit and applied to the common emitter node of a *controlled-cascode* formed by Q1 and Q2. When V_X = 0, all of I_{REF} flows in Q1, due to the action of the high-gain control amplifier which lowers the voltage on the base of Q2. As V_X is raised the fraction of I_{REF} flowing in Q2 is forced to balance the control current, V_X/2.5k. At the full-scale value of V_X (+3V) this fraction is 0.873. Since the bases of Q1, Q4 and Q5 are at ground potential and the bases of Q2, Q3 and Q6 are commoned, all three controlled-cascodes divide the current applied to their emitter nodes in the same proportion. The control loop is stabilized by the external capacitor, C_C.

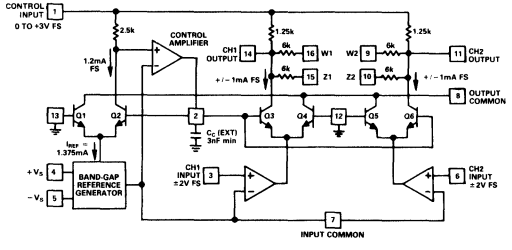


Figure 1. Simplified Schematic of AD539 Multiplier

The signal voltages V_{Y1} and V_{Y2} (generically referred to as V_Y) are first converted to currents by voltage-to-current converters with a g_m of 575μmhos; thus, the full-scale input of ±2V becomes a current of ±1.15mA, which is superimposed on a bias of 2.75mA, and applied to the common emitter node of controlled cascode Q3-Q4 or Q5-Q6. As just explained, the proportion of this current steered to the output node is linearly dependent on V_X. Thus for full-scale V_X and V_Y inputs, a signal of ±1mA (0.873 × ±1.15mA) and a bias component of 2.4mA (0.873 × 2.75mA) appear at the output. The bias component absorbed by the 1.25k resistors also connected to V_X, and the resulting signal current can be applied to an external load resistor (in which case scaling is not accurate) or can be forced into either or both of the 6kΩ feedback resistors (to the Z and W nodes) by an external op amp. In the latter case, scaling accuracy is guaranteed.

GENERAL RECOMMENDATIONS

The AD539 is a high speed circuit and requires considerable care to achieve its full performance potential. A high-quality ground plane should be used with the device either soldered directly into the board or mounted in a low-profile socket. In the figures used here an open triangle denotes a *direct, short* connection to this ground plane; pins 12 and 13 are especially prone to unwanted signal pick-up. Power supply decoupling capacitors of 0.1μF to 1μF should be connected from pins 4 and 5 to the ground plane. In applications using external high-speed op amps, separate supply decoupling should be used. It is good practice to insert small (10Ω) resistors between the primary supply and the decoupling capacitor.

The control amplifier compensation capacitor, C_C, should likewise have short leads to ground and a minimum value of 3nF. Unless maximum control bandwidth is esssential it is advisable to use a larger value of 0.01μF to 0.1μF to improve the signal channel phase response, high-frequency crosstalk and high-frequency distortion. The control bandwidth is inversely proportional to this capacitance, typically 2MHz for C_C = 0.01μF, V_X = 1.7V. The bandwidth and pulse response of the control channel can be improved by using a feedforward capacitor of 5% to 20% the value of C_C between pins 1 and 2. Optimum transient response will result when the rise/fall time of V_X are commensurate with the control-channel response time.

V_X should not exceed the specified range of 0 to +3V. The ac gain is zero for V_x<0 but there remains a feedforward path (see Figure 1) causing control feedthrough. Recovery time from negative values of V_X can be improved by adding a small-signal Schottky diode with its cathode connected to pin 2 and its anode grounded. This constrains the voltage swing on C_C. Above V_X = +3.2V, the ac gain limits at its maximum value, but any overdrive appears as control feedthrough at the output.

The power supplies to the AD539 can be as low as ±4.5V and as high as ±16.5V. The maximum allowable range of the signal inputs, V_Y, is approximately 0.5V above +V_S; the minimum value is 2.5V above −V_S. To accommodate the peak specified inputs of ±4.2V the supplies should be nominally +5V and −7.5V. While there is no performance advantage in raising supplies above these values, it may often be convenient to use the same supplies as for the op amps. The AD539 can tolerate the excess voltage with only a slight effect on dc accuracy but dissipation at ±16.5V can be as high as 535mW and some form of heat-sink is essential in the interests of reliability.

TRANSFER FUNCTION

In using any analog multiplier or divider careful attention must be paid to the matter of *scaling*, particularly in computational applications. To be *dimensionally consistent* a scaling voltage must appear in the transfer function, which, for each channel of the AD539 in the standard multiplier configuration (Figure 2) is

$$V_W = -V_X V_Y / V_U$$

where the inputs V_X and V_Y, the output V_W and the scaling voltage V_U are expressed in a consistent unit, usually volts. In this case, V_U is fixed by the design to be 1V and it is often acceptable in the interest of simplification to use the less rigorous expression

$$V_W = -V_X V_Y$$

where it is understood that *all signals must be expressed in volts*, that is, they are rendered dimensionless by division by (1V).

The accuracy specifications for V_U allow the use of either of the two feedback resistors supplied with each channel, since these are very closely matched, or they may be used in parallel to halve the gain (double the effective scaling voltage), when

$$V_W = -V_X V_Y / 2.$$

When an external load resistor, R_L, is used the scaling is no longer exact since the internal thin-film resistors, while trimmed to high *ratiometric* accuracy, have an absolute tolerance of 20%. However, the nominal transfer function is

$$V_W = -V_X V_Y / V_U'$$

where the effective scaling voltage, V_U' can be calculated for each channel using the formula $V_U' = V_U (5R_L + 6.25)/R_L$, where R_L is expressed in kilohms. For example, when $R_L = 100\Omega$, $V_U' = 67.5V$. Table II provides more detailed data for the case where both channels are used in parallel. The AD539 can also be used with no external load (output pin 11 or 14 open-circuit), when V_U' is quite accurately 5V.

BASIC MULTIPLIER CONNECTIONS

Figure 2 shows the connections for the standard two-channel multiplier, using op amps to provide useful output power and the AD539 feedback resistors to achieve accurate scaling. The transfer function for each channel is

$$V_W = -V_X V_Y$$

where inputs and outputs are expressed in volts (see TRANSFER FUNCTION). At the nominal full-scale inputs of $V_X = +3V$, $V_Y = \pm 2V$ the full-scale outputs are $\pm 6V$. Depending on the choice of op amp, their supply voltages usually need to be about 2V more than the peak output. Thus, supplies of at least $\pm 8V$ are required; the AD539 can share these supplies. Higher outputs are possible if V_X and V_Y are driven to their peak values of $+3.2V$ and $\pm 4.2V$ respectively, when the peak output is $\pm 13.4V$. This requires operating the op amps at supplies of $\pm 15V$. Under these conditions it is advisable to reduce the supplies to the AD539 to $\pm 7.5V$ to limit its power dissipation; however, with some form of heat sinking it is permissible to operate the AD539 directly from $\pm 15V$ supplies.

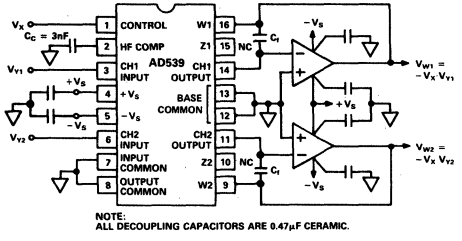


Figure 2. Standard Dual-Channel Multiplier

Viewed as a voltage-controlled amplifier, the decibel gain is simply

$$G = 20 \log V_X$$

where V_X is expressed in volts. This results in a gain of 10dB at $V_X = +3.162V$, 0dB at $V_X = +1V$, $-20dB$ at $V_X = +0.1V$, and so on. In many ac applications the output offset voltage (for $V_X = 0$ or $V_Y = 0$) will not be of major concern; however, it can be eliminated using the offset nulling method recommended for the particular op amp, with $V_X = V_Y = 0$.

At small values of V_X the offset voltage of the control channel will degrade the gain/loss accuracy. For example, a $\pm 1mV$ offset uncertainty will cause the nominal 40dB attenuation at $V_X = +0.01V$ to range from 39.2dB to 40.9dB. Figure 3a shows the maximum gain error boundaries based on the guaranteed control-channel offset voltages of $\pm 2mV$ for the AD539K and $\pm 4mV$ for the AD539J. These curves include all scaling errors and apply to all configurations using the internal feedback resistors (W1 and W2; alternatively, Z1 and Z2).

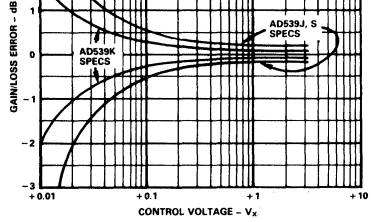


Figure 3a. Maximum AC Gain Error Boundaries

Distortion is a function of the signal input level (V_Y) and the control input (V_X). It is also a function of frequency, although in practice the op amp will generate most of the distortion at frequencies above 100kHz. Figure 3b shows typical results at f = 10kHz as a function of V_X with $V_Y = 0.5$ and 1.5V rms.

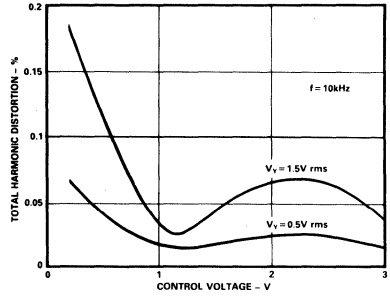


Figure 3b. Total Harmonic Distortion vs. Control Voltage

In some cases it may be desirable to alter the scaling. This can be achieved in several ways. One option is to use both the Z and W feedback resistors (see Figure 1) in parallel, in which case $V_W = -V_X V_Y/2$. This may be preferable where the output swing must be held at ±3V FS (±6.75V pk), for example, to allow the use of reduced supply voltages for the op amps. Alternatively, the gain can be doubled by connecting both channels in parallel and using only a single feedback resistor, in which case $V_W = -2V_X Y_Y$ and the full-scale output is ±12V. Another option is to insert a resistor in series with the control-channel input, permitting the use of a large (for example, 0 to +10V) control voltage. A disadvantage of this scheme is the need to adjust this resistor to accommodate the tolerance of the nominal 500Ω input resistance at pin 1. The signal channel inputs can also be resistively attenuated to permit operation at higher values of V_Y, in which case it may often be possible to partially compensate for the response roll-off of the op amp by adding a capacitor across the upper arm of this attenuator.

Signal-Channel ac and Transient Response

The HF response is dependent almost entirely on the op amp. Note that the "noise gain" for the op amp in Figure 2 is determined by the value of the feedback resistor (6kΩ) and the 1.25kΩ control-bias resistors (Figure 1). Op amps with provision for external frequency compensation (such as the AD301 and AD518) should be compensated for a closed-loop gain of 6.

The layout of the circuit components is very important if low feedthrough and flat response at low values of V_X is to be maintained (see GENERAL RECOMMENDATIONS).

For wide-bandwidth applications requiring an output voltage swing greater than ±1V, the LH0032 hybrid op-amp is recommended. Figure 4a shows the HF response of the circuit of Figure 2 using this amplifier with V_Y = 1V rms and other conditions as shown in Table I. C_F was adjusted for 1dB peaking at V_X = +1V; the −3dB bandwidth exceeds 25MHz. The effect of signal feedthrough on the response becomes apparent at V_X = +0.01V. The minimum feedthrough results when V_X is taken slightly negative to ensure that the residual control-channel offset is exceeded and the dc gain is reliably zero. Measurements show that the feedthrough can be held to −90dB relative to full output at low frequencies and to −60dB up to 20MHz with careful board layout. The corresponding pulse response is shown in Figure 4b for a signal input of V_Y of ±1V and two values of V_X (+3V and +0.1V).

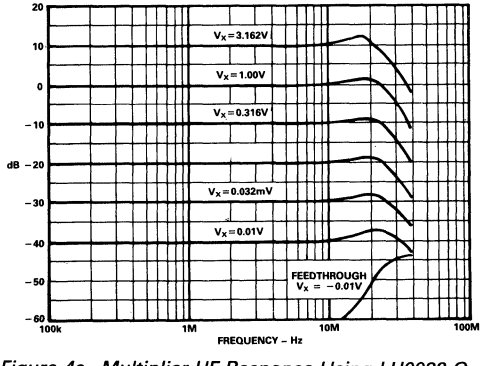
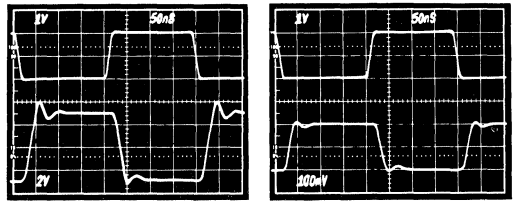


Figure 4a. Multiplier HF Response Using LH0032 Op Amps



V_X = +3V V_X = +0.1V

Figure 4b. Multiplier Pulse Response Using LH0032 Op Amps

	AD711[1]	AD5539[2]	LH0032[1]
Op Amp Supply Voltages	±15V	±9V	±10V
Op Amp Compensation Capacitor	None	None	1-5pF
Feedback Capacitor, C_F	None	0.25-1.5pF	1-4pF
−3dB Bandwidth, V_X = +1V	900kHz	50MHz	25MHz
Load Capacitance	<1nF	<10pF	<100pF
HF Feedthrough, V_X = −0.01V, f = 5MHz	N/A	−54dB	−70dB
rms Output Noise, V_X = +1V, BW 10Hz-10kHz	50μV	40μV	30μV
V_X = +1V, BW 10Hz-5MHz	120μV	620μV	500μV

In all cases, 0.47μF ceramic supply-decoupling capacitors were used at each IC pin, the AD539 supplies were ±5V and the control-compensation capacitor C_C was 3nF.

NOTES
[1]For the circuit of Figure 2.
[2]For the circuit of Figure 8.

Table I. Summary of Operating Conditions and Performance for the AD539 When Used with Various External Op-Amp Output Amplifiers

Minimal Wide-Band Configurations

The maximum bandwidth can be achieved using the AD539 with simple resistive loads to convert the output currents to voltages. These currents (nominally ±1mA FS, ±2.25mA pk,

Table II. Summary of Performance for Minimal Configuration

Load Resistance	50Ω	75Ω	100Ω	150Ω	600Ω	O/C
FS Output Voltage	±92.6mV	±134mV	±172mV	±242mV	±612mV	±1V
	65.5mV rms	94.7mV rms	122mV rms	171mV rms	433mV rms	*
FS Output-Power in Load	0.086mW	0.12mW	0.15mW	0.195mW	0.312mW	–
	−10.5dBm	−9.2dBm	−8.3dBm	−7.1dBm	−5.05dBm	–
Pk Output Voltage	±210mV	±300mV	±388mV	±544mV	±1V	±1V
	148mV rms	212mV rms	274mV rms	385mV rms	*	*
Pk Output-Power in Load	0.44mW	0.6mW	0.75mW	1mW	±1V	±1V
	−7dBm	−4.4dBm	−2.5dBm	0dBm	*	*
Effective Scaling Voltage, V_U'	67.5V	46.7V	36.3V	25.8V	10.2V	5V

*Peak negative voltage swing limited by output compliance.

into short-circuit loads) are shunted by their source resistance of 1.25kΩ (each channel). Calculations of load power and effective scaling-voltage must allow for this shunting effect when using resistive loads. The output power is quite low in this mode, and the device behaves more like a voltage-controlled attenuator than a classical multiplier. The matching of gain and phase between the two channels is excellent. From dc to 10MHz the gains are typically within ±0.025dB (measured using precision 50Ω load resistors) and the phase difference within ±0.1°.

For a given load resistance the output power can be quadrupled by using both channels in parallel, as shown in Figure 5a. The small-signal silicon diode D connected between ground and pins 12 and 13 provides extra voltage compliance at the output nodes in the negative direction (to −1V at 25°C); it is not required if the output swing does not exceed −300mV. Table II compares performance for various load resistances, using this configuration.

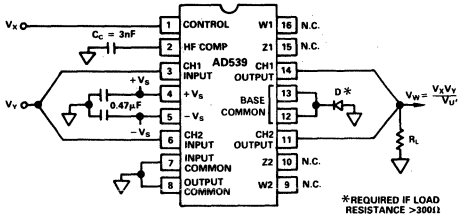


Figure 5a. Minimal Single-Channel Multiplier

Figure 5b shows the HF response for Figure 5a with the AD539 in a carefully-shielded 50Ω test-environment; the test system response was first characterized and this background removed by digital signal processing to show the inherent circuit response.

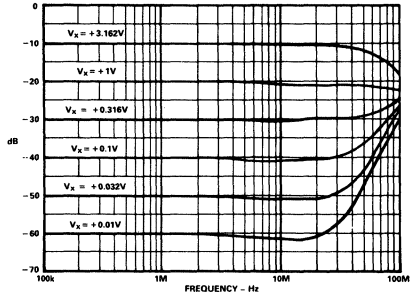


Figure 5b. HF Response in Minimal Configuration

In many applications *phase linearity* over frequency is important. Figure 5c shows the deviation from an ideal linear-phase response for a typical AD539 over the frequency range dc to 10MHz, for $V_X = +3V$; the peak deviation is slightly more than 1°. *Differential phase linearity* (the stability of phase over the signal window at a fixed frequency) is shown in Figure 5d for f = 3.579MHz and various values of V_X. The most rapid variation occurs for V_Y above +1V; in applications where this characteristic is critical, it is recommended that a ground-referenced, negative-going signal be used.

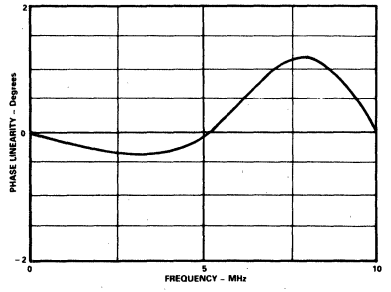


Figure 5c. Phase Linearity Error in Minimal Configuration

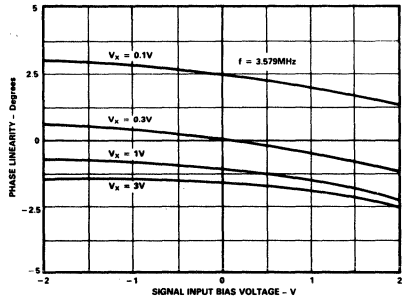


Figure 5d. Differential Phase Linearity in Minimal Configuration for a Typical Device

Differential Configurations

When only one signal channel must be handled it is often advantageous to use the channels differentially. By subtracting the CH1 and CH2 outputs any residual transient control feedthrough is virtually eliminated. Figure 6a shows a minimal configuration where it is assumed that the host system uses differential signals and a 50Ω environment throughout. This figure also shows a recommended control-feedforward network to improve large-signal

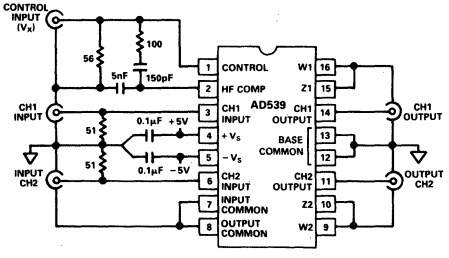


Figure 6a. High-Speed Differential Configuration

response time. The control feedthrough glitch is shown in Figure 6b, where the input was applied to CH1 and only the output of CH1 was displayed on the oscilloscope. The improvement obtained when CH1 and CH2 outputs are viewed differentially is clear in Figure 6c. The envelope rise-time is of the order of 40ns.

Lower distortion results when CH1 and CH2 are driven by *complementary* inputs and the outputs are utilized differentially, using a circuit such as Figure 7a. Resistors R1 and R2 should have a value in the range 100 to 1000Ω.

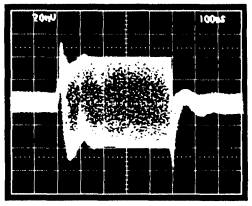


Figure 6b. Control Feedthrough One Channel of Figure 6a

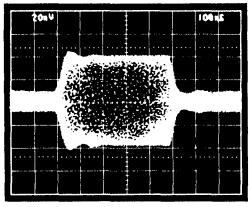


Figure 6c. Control Feedthrough Differential Mode, Figure 6a

They minimize a secondary distortion mechanism caused by a collector-modulation effect in the controlled cascodes (see CIRCUIT DESCRIPTION) by keeping the voltage-swing at the outputs to an acceptable level. Figure 7b shows the improvement in distortion over the standard configuration (compare Figure 3b). Note that the Z nodes (pins 10 and 15) are returned to the control input; this prevents the early onset of output-transistor saturation.

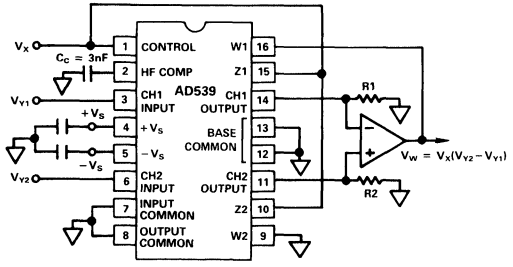


Figure 7a. Low-Distortion Differential Configuration

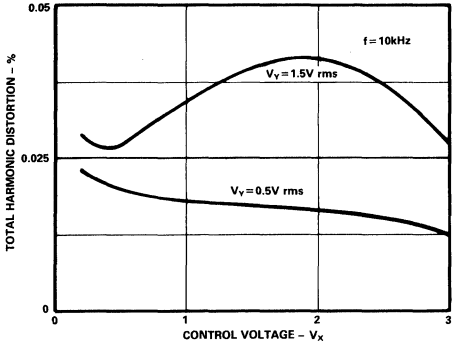


Figure 7b. Distortion in Differential Mode Using LH0032 Op Amp

Even lower distortion (0.01%, or −80dB) has been measured using two output op amps in a configuration similar to Figure 2 connected as virtual-ground current-summers (to prevent the modulation effect). Note that to generate the difference output it is merely necessary to connect the output of the CH1 op amp to the Z node of CH2. In this way, the net input to the CH2 op amp is the difference signal, and the low-distortion resultant appears as its output.

A 50MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 8 is a circuit for a 50MHz voltage-controlled amplifier (VCA) suitable for use in high-quality-video-speed applications. The outputs from the two-signal channels of the AD539 are applied to the op-amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven (V_X<0 or V_X>3.3V). Secondly, it provides a choice of either non-inverting or inverting responses, using either inputs V_{Y1} or V_{Y2} respectively. In this circuit, the output of the op-amp will equal:

$$V_{OUT} = \frac{V_X (V_{Y1} - V_{Y2})}{2V} \text{ for } V_X > 0$$

Hence, the gain is unity at V_X = +2V. Since V_X can over-range to +3.3V, the maximum gain in this configuration is about 4.3dB. (Note: If pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10dB.)

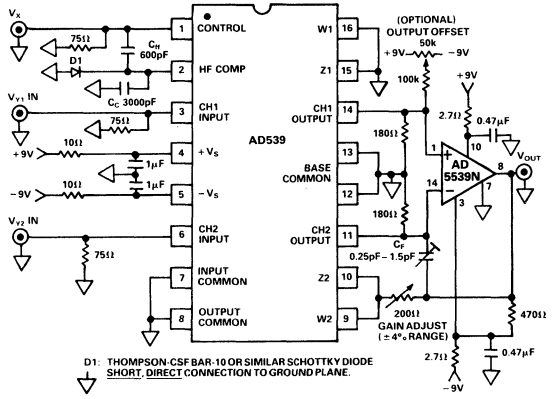


Figure 8. A Wide Bandwidth Voltage-Controlled Amplifier

The −3dB bandwidth of this circuit is over 50MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, *extreme* care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 9a shows the ac response from the noninverting

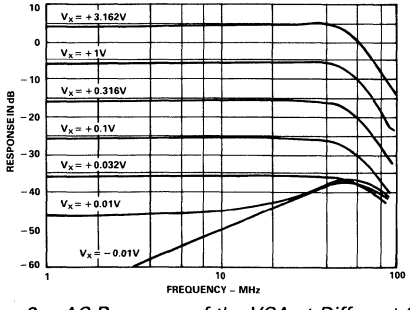


Figure 9a. AC Response of the VCA at Different Gains V_Y = 0.5V RMS

input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: $V_{Y1} = 0.5V$ rms for values of V_X from +10mV to +3.16V; this is with a 75Ω load on the output. The feedthrough at $V_X = -10mV$ is also shown.

The transient response of the signal channel at $V_X = +2V$, $V_Y = V_{OUT} = \pm 1V$ is shown in Figure 9b; with the VCA driving a 75Ω load. The rise and fall times are approximately 7ns.

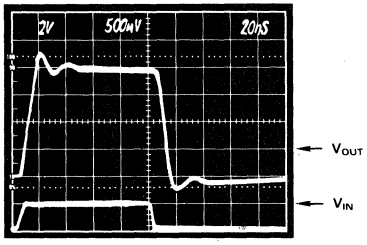


Figure 9b. Transient Response of the Voltage-Controlled Amplifier $V_X = +2$ Volts $V_Y = \pm 1$ Volt

A more detailed description of this circuit, including differential gain and phase characteristics, is given in the application note "Low Cost, Two Chip Voltage-Controlled Amplifier and Video Switch" available from Analog Devices.

BASIC DIVIDER CONNECTIONS

Standard Scaling

The AD539 provides excellent operation as a two-quadrant analog divider in wide-band wide gain-range applications, with the advantage of dual-channel operation. Figure 10a shows the simplest connections for division with a transfer function of

$$V_Y = -V_U V_W / V_X$$

Recalling that the nominal value of V_U is 1V, this can be simplified to

$$V_Y = -V_W / V_X$$

where all signals are expressed in volts. The circuit thus exhibits unity gain for $V_X = +1V$ and a gain of 40dB when $V_X = +0.01V$.

The output swing is limited to ±2V nominal full-scale and ±4.2V peak (using a $-V_S$ supply of at least 7.5V for the AD539). Since the maximum *loss* is 10dB (at $V_X = 3.162V$), it follows that the maximum input to V_W should be ±6.3V (4.4V rms)

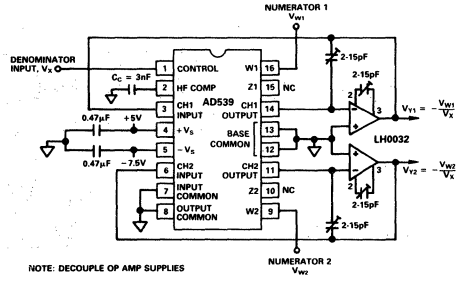


Figure 10a. Two-Channel Divider with 1V Scaling

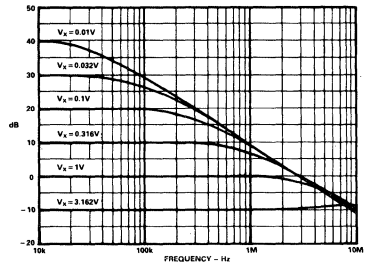


Figure 10b. HF Response of Figure 10a Divider

for low distortion applications, and no more than ±13.4V (9.5V rms) to avoid clipping. Note that offset adjustment will be needed for the op amps to maintain accurate dc levels at the output in high gain applications: the "noise gain" is $6V/V_X$, or 600 at $V_X = +0.01V$.

The gain-magnitude response for this configuration using the LH0032 op amps with nominally 12pF compensation (pins 2 to 3) and $C_F = 7pF$ is shown in Figure 10b; of course, other amplifiers may also be used. Since there is some manufacturing variation in the HF response of the op amps, and load conditions will also affect the response, these capacitors should be adjustable: 5-15pF is recommended for both positions. The bandwidth in this configuration is nominally 17MHz at $V_X = +3.162V$, 4.5MHz at $V_X = +1V$, 350kHz at $V_X = +0.1V$ and 35kHz at $V_X = +0.01V$. The general recommendations regarding the use of a good ground plane and power-supply decoupling should be carefully observed. Other suitable high speed op amps include: AD844, AD827 and AD811. Consult these data sheets for suitable applications circuits.

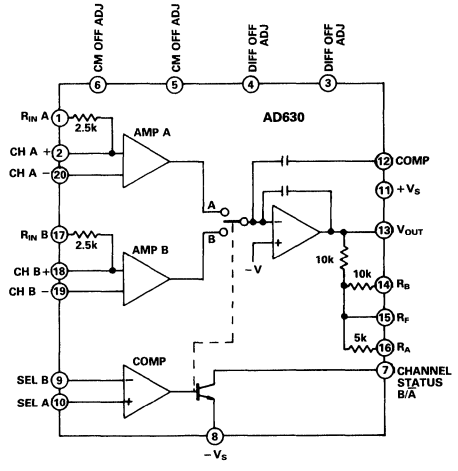
Balanced Modulator/Demodulator

AD630

FEATURES

Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth
Chips Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 may be thought of as a precision op amp with two independent differential input stages and a precision comparator which is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion. In addition, the AD630 has extremely low crosstalk between channels of −100dB @ 10kHz.

The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100dB of interfering noise (see lock-in amplifier application). Although optimized for operation up to 1kHz, the circuit is useful at frequencies up to several hundred kilohertz.

Other features of the AD630 include pin programmable frequency compensation, optional input bias current compensation resistors, common mode and differential offset voltage adjustment, and a channel status output which indicates which of the two differential inputs is active. This device is now available to Standard Military Drawing (DESC) numbers 5962–8980701RA and 5962–89807012A.

PRODUCT HIGHLIGHTS

1. The configuration of the AD630 makes it ideal for signal processing applications such as: balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication.
2. The application flexibility of the AD630 makes it the best choice for many applications requiring precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high-speed precision amplification.
3. The 100dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
4. The op-amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
5. The AD630 can be used as a two channel multiplexer with gains of +1, +2, +3 or +4. The channel separation of 100dB @ 10kHz approaches the limit which is achievable with an empty IC package.
6. The AD630 has pin-strappable frequency compensation (no external capacitor required) for stable operation at unity gain without sacrificing dynamic performance at higher gains.
7. Laser trimming of comparator and amplifying channel offsets eliminates the need for external nulling in most cases.

AD630 — SPECIFICATIONS (@ +25°C and $\pm V_S$ = ±15V unless otherwise specified)

Model	AD630J/A			AD630K/B			AD630S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN										
Open Loop Gain	90	110		100	120		90	110		dB
±1, ±2 Closed Loop Gain Error		0.1				0.05		0.1		%
Closed Loop Gain Match		0.1				0.05		0.1		%
Closed Loop Gain Drift		2			2			2		ppm°C
CHANNEL INPUTS										
V_{IN} Operational Limit[1]	$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			Volts
Input Offset Voltage			500			100			500	µV
Input Offset Voltage										
T_{min} to T_{max}[2]			800			160			1000	µV
Input Bias Current		100	300		100	300		100	300	nA
Input Offset Current		10	50		10	50		10	50	nA
Channel Separation @ 10kHz		100			100			100		dB
COMPARATOR										
V_{IN} Operational Limit[1]	$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.3V)$			Volts
Switching Window			±1.5			±1.5			±1.5	mV
Switching Window										
T_{min} to T_{max}[2]			±2.0			±2.0			±2.5	mV
Input Bias Current		100	300		100	300		100	300	nA
Response Time (−5mV to +5mV step)		200			200			200		ns
Channel Status										
I_{SINK} @ $V_{OL} = -V_S + 0.4V$[3]	1.6			1.6			1.6			mA
Pull-Up Voltage			$(-V_S+33V)$			$(-V_S+33V)$			$(-V_S+33V)$	Volts
DYNAMIC PERFORMANCE										
Unity Gain Bandwidth		2			2			2		MHz
Slew Rate[4]		45			45			45		V/µs
Settling Time to 0.1% (20V step)		3			3			3		µs
OPERATING CHARACTERISTICS										
Common-Mode Rejection	85	105		90	110		90	110		dB
Power Supply Rejection	90	110		90	110		90	110		dB
Supply Voltage Range	±5		±16.5	±5		±16.5	±5		±16.5	Volts
Supply Current		4	5		4	5		4	5	mA
OUTPUT VOLTAGE, @ R_L = 2kΩ										
T_{min} to T_{max}[2]	±10			±10			±10			Volts
Output Short Circuit Current		25			25			25		mA
TEMPERATURE RANGES										
Rated Performance – N Package	0		+70	0		+70		N/A		°C
D Package	−25		+85	−25		+85	−55		+125	°C

NOTES

[1]If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.

[2]These parameters are guaranteed but not tested for J and K grades. For A, B and S grades they are tested.

[3]I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4mA.

[4]Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/µs.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation 600mW
Output Short Circuit to Ground . . . . . Indefinite
Storage Temperature, Ceramic Package . . . −65°C to +150°C
Storage Temperature, Plastic Package . . . . −55°C to +125°C
Lead Temperature, 10 sec. Soldering . . . . . +300°C
Max Junction Temperature . . . . . +150°C

THERMAL CHARACTERISTICS

	θ_{JC}	θ_{JA}
20-Pin Plastic DIP (N)	24°C/W	61°C/W
20-Pin Ceramic DIP (D)	35°C/W	120°C/W
20-Pin Leadless Chip Carrier (E)	35°C/W	120°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD630JN	0°C to +70°C	Plastic DIP	N-20
AD630KN	0°C to +70°C	Plastic DIP	N-20
AD630AD	−25°C to +85°C	Side Brazed DIP	D-20
AD630BD	−25°C to +85°C	Side Brazed DIP	D-20
AD630SD	−55°C to +125°C	Side Brazed DIP	D-20
AD630SD/883B	−55°C to +125°C	Side Brazed DIP	D-20
5962-8980701RA	−55°C to +125°C	Side Brazed DIP	D-20
AD630SE	−55°C to +125°C	LCC	E-20A
AD630SE/883B	−55°C to +125°C	LCC	E-20A
5962-89807012A	−55°C to +125°C	LCC	E-20A
AD630J Chip	0°C to +70°C	Chip	
AD630S Chip	−55°C to +125°C	Chip	

*For outline information see Package Information section.

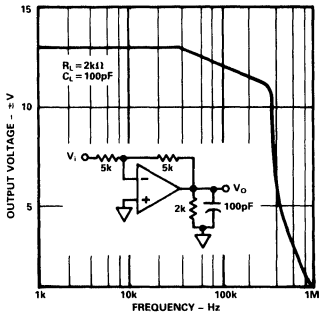


Figure 1. Output Voltage vs. Frequency

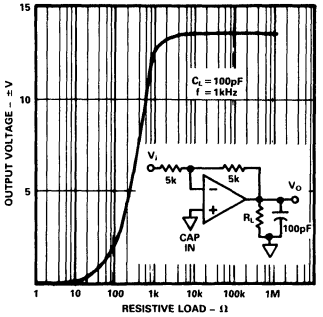


Figure 2. Output Voltage vs. Resistive Load

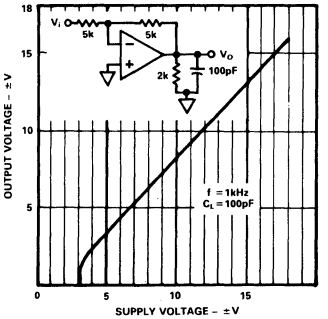


Figure 3. Output Voltage Swing vs. Supply Voltage

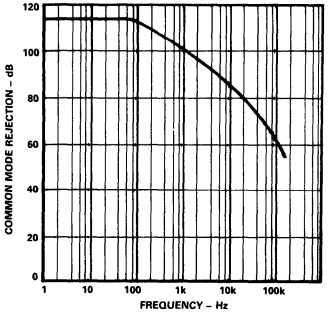


Figure 4. Common Mode Rejection vs. Frequency

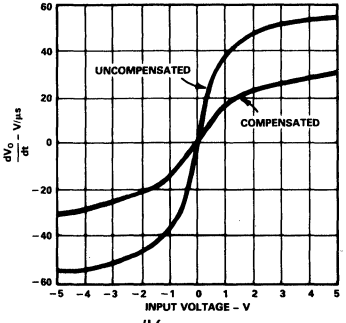


Figure 5. $\frac{dV_O}{dt}$ vs. Input Voltage

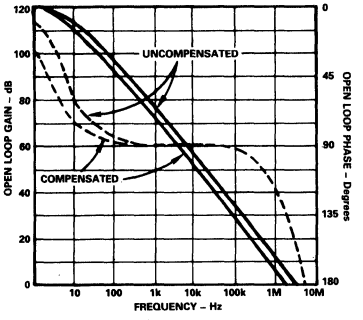


Figure 6. Gain and Phase vs. Frequency

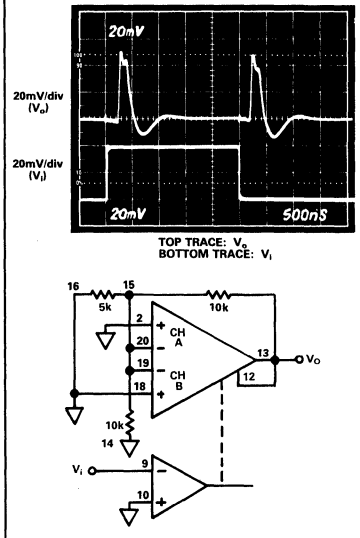


Figure 7. Channel-to-Channel Switch-Settling Characteristic

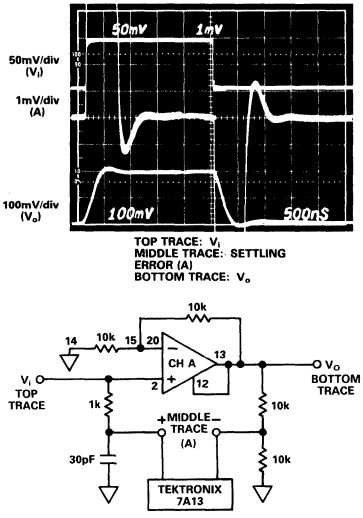


Figure 8. Small Signal Noninverting Step Response

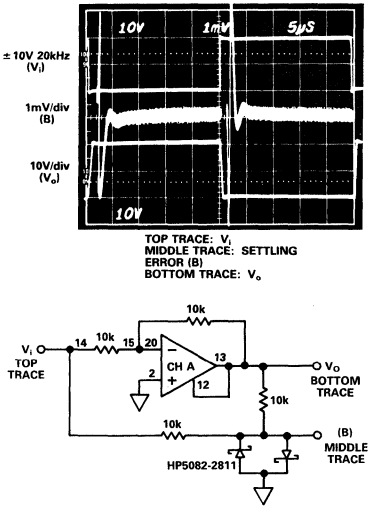
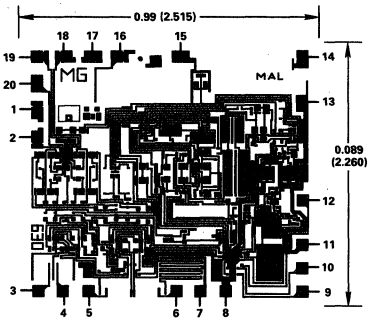


Figure 9. Large Signal Inverting Step Response

CHIP METALIZATION AND PINOUT

Dimensions shown in inches and (mm).
Contact factory for latest dimensions



CHIP AVAILABILITY

The AD630 is available in laser trimmed, passivated chip form. The figure shows the AD630 metalization pattern, bonding pads and dimensions. AD630 chips are available; consult factory for details.

TWO WAYS TO LOOK AT THE AD630

Figure 10 is a functional block diagram of the AD630 which also shows the pin connections of the internal functions. An alternative architectural diagram is shown in Figure 11. In this diagram, the individual A and B channel pre-amps, the switch, and the integrator-output amplifier are combined in a single op amp. This amplifier has two differential input channels, only one of which is active at a time.

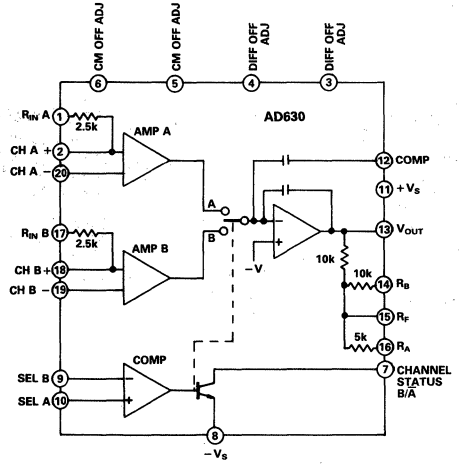


Figure 10. Functional Block Diagram

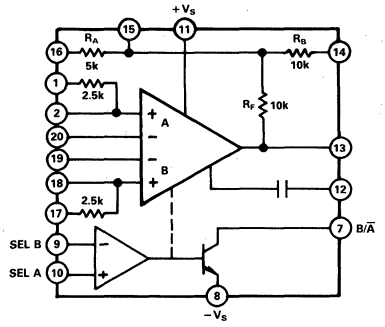


Figure 11. Architectural Block Diagram

HOW THE AD630 WORKS

The basic mode of operation of the AD630 may be more easy to recognize as two fixed gain stages which may be inserted into the signal path under the control of a sensitive voltage comparator. When the circuit is switched between inverting and noninverting gain, it provides the basic modulation/demodulation function. The AD630 is unique in that it includes laser wafer trimmed thin film feedback resistors on the monolithic chip. The configuration shown below yields a gain of ±2 and can be easily changed to ±1 by shifting R_B from its ground connection to the output.

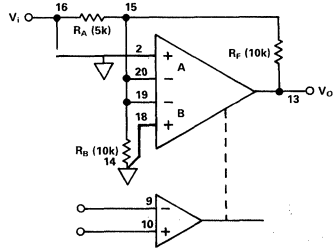


Figure 12. AD630 Symmetric Gain (±2)

The comparator selects one of the two input stages to complete an operational feedback connection around the AD630. The de-selected input is off and has negligible effect on the operation.

When channel B is selected, the resistors R_A and R_F are connected for inverting feedback as shown in the inverting gain configuration diagram in Figure 13. The amplifier has sufficient loop gain to minimize the loading effect of R_B at the virtual ground produced by the feedback connection. When the sign of the comparator input is reversed, input B will be de-selected and A will be

selected. The new equivalent circuit will be the noninverting gain configuration shown below. In this case R_A will appear across the op-amp input terminals, but since the amplifier drives this difference voltage to zero the closed loop gain is unaffected.

The two closed loop gain magnitudes will be equal when $R_F/R_A = 1 + R_F/R_B$, which will result from making R_A equal to $R_F R_B/(R_F + R_B)$ the parallel equivalent resistance of R_F and R_B.

The 5k and the two 10k resistors on the AD630 chip can be used to make a gain of two as shown here. By paralleling the 10k resistors to make R_F equal 5k and omitting R_B the circuit can be programmed for a gain of ± 1 (as shown in Figure 19a). These and other configurations using the on chip resistors present the inverting inputs with a 2.5k source impedance. The more complete AD630 diagrams show 2.5k resistors available at the noninverting inputs which can be conveniently used to minimize errors resulting from input bias currents.

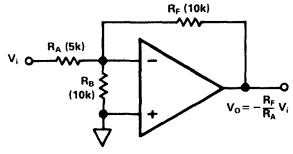


Figure 13. Inverting Gain Configuration

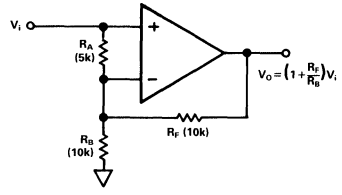


Figure 14. Noninverting Gain Configuration

CIRCUIT DESCRIPTION

The simplified schematic of the AD630 is shown in Figure 15. It has been subdivided into three major sections, the comparator, the two input stages and the output integrator. The comparator consists of a front end made up of Q52 and Q53, a flip-flop load formed by Q3 and Q4, and two current steering switching cells Q28, Q29 and Q30, Q31. This structure is designed so that a differential input voltage greater than 1.5mV in magnitude

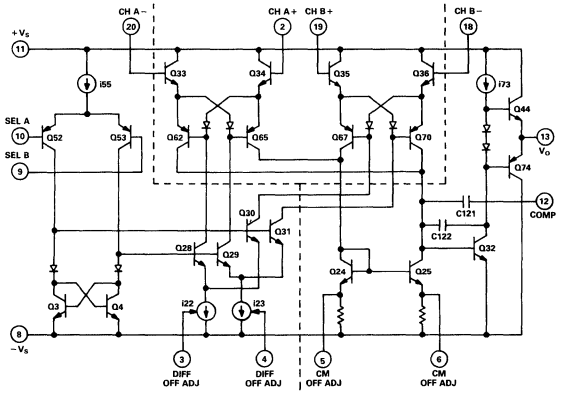


Figure 15. AD630 Simplified Schematic

applied to the comparator inputs will completely select one of the switching cells. The sign of this input voltage determines which of the two switching cells is selected.

The collectors of each switching cell connect to an input transconductance stage. The selected cell conveys bias currents i_{22} and i_{23} to the input stage it controls causing it to become active. The deselected cell blocks the bias to its input stage which, as a consequence, remains off.

The structure of the transconductance stages is such that they present a high impedance at their input terminals and draw no bias current when deselected. The deselected input does not interfere with the operation of the selected input insuring maximum channel separation.

Another feature of the input structure is that it enhances the slew rate of the circuit. The current output of the active stage follows a quasi-hyperbolic-sine relationship to the differential input voltage. This means that the greater the input voltage, the harder this stage will drive the output integrator, and hence, the faster the output signal will move. This feature helps insure rapid, symmetric settling when switching between inverting and noninverting closed loop configurations.

The output section of the AD630 includes a current mirror-load (Q24 and Q25), an integrator-voltage gain stage (Q32), and a complementary output buffer (Q44 and Q74). The outputs of both transconductance stages are connected in parallel to the current mirror. Since the deselected input stage produces no output current and presents a high impedance at its outputs, there is no conflict. The current mirror translates the differential output current from the active input transconductance amplifier into single ended form for the output integrator. The complementary output driver then buffers the integrator output to produce a low impedance output.

OTHER GAIN CONFIGURATIONS

Many applications require switched gains other than the ± 1 and ± 2 which the self-contained applications resistors provide. The AD630 can be readily programmed with 3 external resistors over a wide range of positive and negative gain by selecting R_B and R_F to give the noninverting gain $1 + R_F/R_B$ and subsequently R_A to give the desired inverting gain. Note that when the inverting magnitude equals the noninverting magnitude, the value of R_A is found to be $R_B R_F/(R_B + R_F)$. That is, R_A should equal the parallel combination of R_B and R_F to match positive and negative gain.

The feedback synthesis of the AD630 may also include reactive impedance. The gain magnitudes will match at all frequencies if the A impedance is made to equal the parallel combination of the B and F impedances. Essentially the same considerations apply to the AD630 as to conventional op-amp feedback circuits. Virtually any function which can be realized with simple non-inverting "L network" feedback can be used with the AD630. A common arrangement is shown in Figure 16. The low frequency gain of this circuit is 10. The response will have a pole (-3dB) at a frequency $f \simeq 1/(2\pi 100k\Omega C)$ and a zero (3dB from the high frequency asymptote) at about 10 times this frequency. The 2k resistor in series with each capacitor mitigates the loading effect on circuitry driving this circuit, eliminates stability problems, and has a minor effect on the pole-zero locations.

As a result of the reactive feedback, the high frequency components of the switched input signal will be transmitted at unity gain

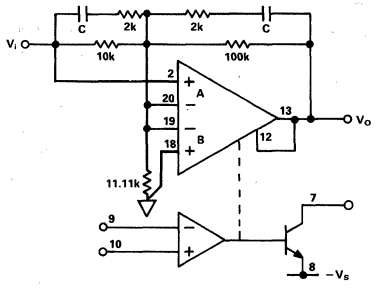


Figure 16. AD630 with External Feedback

while the low frequency components will be amplified. This arrangement is useful in demodulators and lock-in amplifiers. It increases the circuit dynamic range when the modulation or interference is substantially larger than the desired signal amplitude. The output signal will contain the desired signal multiplied by the low frequency gain (which may be several hundred for large feedback ratios) with the switching signal and interference superimposed at unity gain.

SWITCHED INPUT IMPEDANCE

The noninverting mode of operation is a high input impedance configuration while the inverting mode is a low input impedance configuration. This means that the input impedance of the circuit undergoes an abrupt change as the gain is switched under control of the comparator. If gain is switched when the input signal is not zero, as it is in many practical cases, a transient will be delivered to the circuitry driving the AD630. In most applications, this will require the AD630 circuit to be driven by a low impedance source which remains "stiff " at high frequencies. Generally this will be a wideband buffer amplifier.

FREQUENCY COMPENSATION

The AD630 combines the convenience of internal frequency compensation with the flexibility of external compensation by means of an optional self-contained compensation capacitor.

In gain of ± 2 applications the noise gain which must be addressed for stability purposes is actually 4. In this circumstance, the phase margin of the loop will be on the order of 60° without the optional compensation. This condition provides the maximum bandwidth and slew-rate for closed-loop gains of $|2|$ and above.

When the AD630 is used as a multiplexer, or in other configurations where one or both inputs are connected for unity gain feedback, the phase margin will be reduced to less than 20°. This may be acceptable in applications where fast slewing is a first priority, but the transient response will not be optimum. For these applications, the self-contained compensation capacitor may be added by connecting pin 12 to pin 13. This connection reduces the closed loop bandwidth somewhat, and improves the phase margin.

For intermediate conditions, such as gain of ± 1 where loop attenuation is 2, use of the compensation should be determined by whether bandwidth or settling response must be optimized. The optional compensation should also be used when the AD630 is driving capacitive loads or whenever conservative frequency compensation is desired.

OFFSET VOLTAGE NULLING

The offset voltages of both input stages and the comparator have been pre-trimmed so that external trimming will only be required in the most demanding applications. The offset adjustment of the two input channels is accomplished by means of a differential and common mode scheme. This facilitates fine adjustment of system errors in switched gain applications. With system input tied to 0V, and a switching or carrier waveform applied to the comparator, a low level square wave will appear at the output. The differential offset adjustment pot can be used to null the amplitude of this square wave (pins 3 and 4). The common mode offset adjustment can be used to zero the residual dc output voltage (pins 5 and 6). These functions should be implemented using 10k trim pots with wipers connected directly to pin 8 as shown in Figures 19a and 19b.

CHANNEL STATUS OUTPUT

The channel status output, pin 7, is an open collector output referenced to $-V_S$ which can be used to indicate which of the two input channels is active. The output will be active (pulled low) when channel A is selected. This output can also be used to supply positive feedback around the comparator. This produces hysteresis which serves to increase noise immunity. Figure 17 shows an example of how hysteresis may be implemented. Note that the feedback signal is applied to the inverting (−) terminal of the comparator to achieve positive feedback. This is because the open collector channel status output inverts the output sense of the internal comparator.

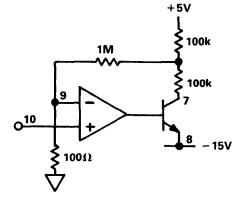


Figure 17. Comparator Hysteresis

The channel status output may be interfaced with TTL inputs as shown in Figure 18. This circuit provides appropriate level shifting from the open-collector AD630 channel status output to TTL inputs.

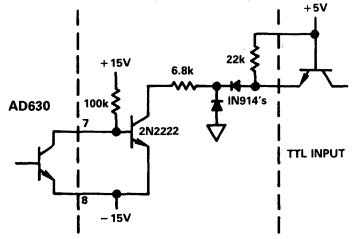


Figure 18. Channel Status – TTL Interface

APPLICATIONS:
BALANCED MODULATOR

Perhaps the most commonly used configuration of the AD630 is the balanced modulator. The application resistors provide precise symmetric gains of ± 1 and ± 2. The ± 1 arrangement is shown in Figure 19a and the ± 2 arrangement is shown in Figure 19b. These cases differ only in the connection of the 10k feedback resistor (pin 14) and the compensation capacitor (pin 12). Note

the use of the 2.5kΩ bias current compensation resistors in these examples. These resistors perform the identical function in the ±1 gain case. Figure 20 demonstrates the performance of the AD630 when used to modulate a 100kHz square wave carrier with a 10kHz sinusoid. The result is the double sideband suppressed carrier waveform.

These balanced modulator topologies accept two inputs, a signal (or modulation) input applied to the amplifying channels, and a reference (or carrier) input applied to the comparator.

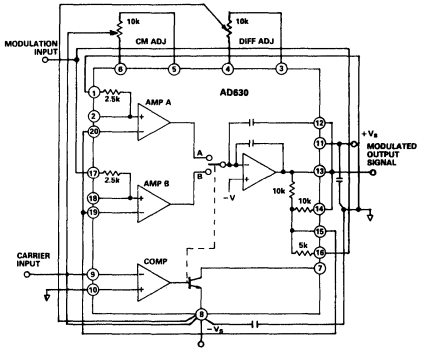


Figure 19a. AD630 Configured as a Gain-of-One Balanced Modulator

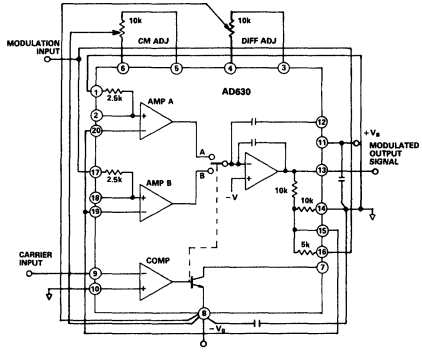


Figure 19b. AD630 Configured as a Gain-of-Two Balanced Modulator

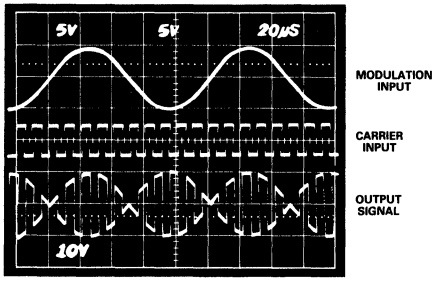


Figure 20. Gain-of-Two Balanced Modulator Sample Waveforms

BALANCED DEMODULATOR

The balanced modulator topology described above will also act as a balanced demodulator if a double sideband suppressed carrier waveform is applied to the signal input and the carrier signal is applied to the reference input. The output under these circumstances will be the baseband modulation signal. Higher order carrier components will also be present which can be removed with a low-pass filter. Other names for this function are synchronous demodulation and phase-sensitive detection.

PRECISION PHASE COMPARATOR

The balanced modulator topologies of Figures 19a and 19b can also be used as precision phase comparators. In this case, an ac waveform of a particular frequency is applied to the signal input and a waveform of the same frequency is applied to the reference input. The dc level of the output (obtained by low pass filtering) will be proportional to the signal amplitude and phase difference between the input signals. If the signal amplitude is held constant, then the output can be used as a direct indication of the phase. When these input signals are 90° out of phase, they are said to be in quadrature and the AD630 dc output will be zero.

PRECISION RECTIFIER-ABSOLUTE VALUE

If the input signal is used as its own reference in the balanced modulator topologies, the AD630 will act as a precision rectifier. The high frequency performance will be superior to that which can be achieved with diode feedback and op amps. There are no diode drops which the op amp must "leap over" with the commutating amplifier.

LVDT SIGNAL CONDITIONER

Many transducers function by modulating an ac carrier. A Linear Variable Differential Transformer (LVDT) is a transducer of this type. The amplitude of the output signal corresponds to core displacement. Figure 21 shows an accurate synchronous demodulation system which can be used to produce a dc voltage which corresponds to the LVDT core position. The inherent precision and temperature stability of the AD630 reduce demodulator drift to a second order effect.

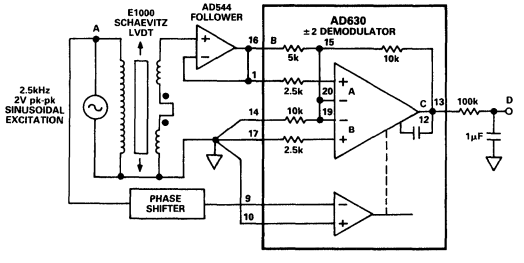


Figure 21. LVDT Signal Conditioner

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to

the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 22 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper-middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 3.2mV change in the low pass filtered dc output, well above the RTO drifts and noise.

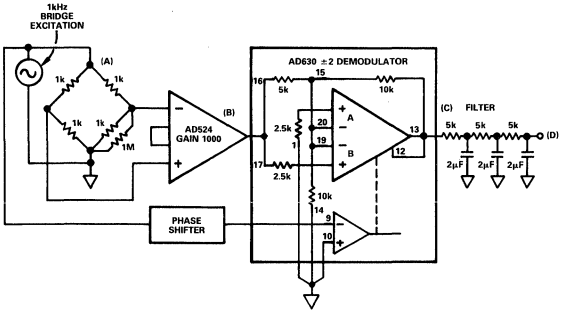


Figure 22. AC Bridge System

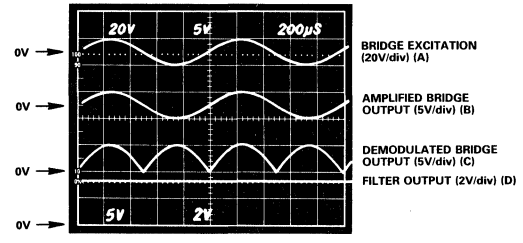


Figure 23. AC Bridge Waveforms

LOCK-IN AMPLIFIER APPLICATIONS

Lock-in amplification is a technique which is used to separate a small, narrow band signal from interfering noise. The lock-in amplifier acts as a detector and narrow band filter combined. Very small signals can be detected in the presence of large amounts of uncorrelated noise when the frequency and phase of the desired signal are known.

The lock-in amplifier is basically a synchronous demodulator followed by a low pass filter. An important measure of performance in a lock-in amplifier is the dynamic range of its demodulator. The schematic diagram of a demonstration circuit which exhibits the dynamic range of an AD630 as it might be used in a lock-in amplifier is shown in Figure 24. Figure 25 is an oscilloscope photo showing the recovery of a signal modulated at 400Hz from a noise signal approximately 100,000 times larger; a dynamic range of 100dB.

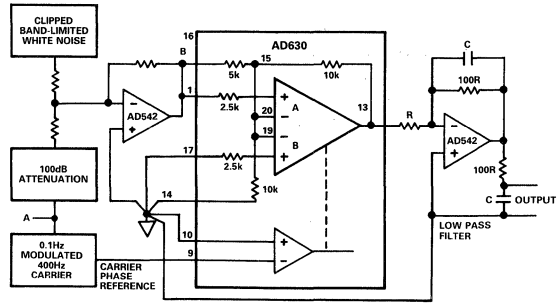


Figure 24. Lock-In Amplifier

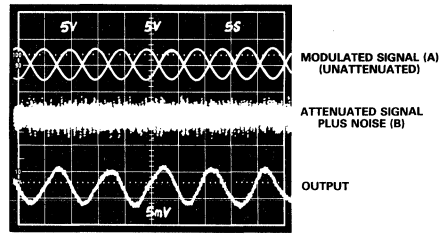


Figure 25. Lock-In Amplifier Waveforms

The test signal is produced by modulating a 400Hz carrier with a 0.1Hz sine wave. The signals produced, for example, by chopped radiation (IR, optical, etc.) detectors may have similar low frequency components. A sinusoidal modulation is used for clarity of illustration. This signal is produced by a circuit similar to Figure 19b and is shown in the upper trace of Figure 25. It is attenuated 100,000 times normalized to the output, B, of the summing amplifier. A noise signal which might represent, for example, background and detector noise in the chopped radiation case, is added to the modulated signal by the summing amplifier. This signal is simply band limited clipped white noise. Figure 25 shows the sum of attenuated signal plus noise in the center trace. This combined signal is demodulated synchronously using phase information derived from the modulator, and the result is low pass filtered using a 2-pole simple filter which also provides a gain of 100 to the output. This recovered signal is the lower trace of Figure 25.

The combined modulated signal and interfering noise used for this illustration is similar to the signals often requiring a lock-in amplifier for detection. The precision input performance of the AD630 provides more than 100dB of signal range and its dynamic response permits it to be used with carrier frequencies more than two orders of magnitude higher than in this example. A more sophisticated low pass output filter will aid in rejecting wider bandwidth interference.

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

AD632

FEATURES

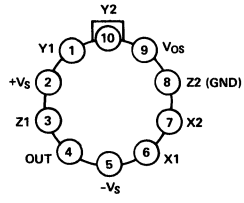
Pretrimmed to ±0.5% Max 4-Quadrant Error
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X10 Gain
Low Noise Design: 90μV rms, 10Hz-10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Accurate Voltage Controlled Oscillators and Filters

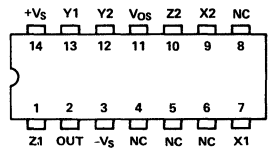
PIN CONFIGURATIONS

H-Package TO-100



TOP VIEW

D-Package TO-116



TOP VIEW

PRODUCT DESCRIPTION

The AD632 is an internally-trimmed monolithic four-quadrant multiplier/divider. The AD632B has a maximum multiplying error of ±0.5% without external trims.

Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions. The simplicity and flexibility of use provide an attractive alternative approach to the solution of complex control functions.

The AD632 is pin for pin compatible with the industry standard AD532 with improved specifications and a fully differential high impedance Z-input. The AD632 is capable of providing gains of up to X10, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD632 can be effectively employed as a variable gain differential input amplifier with high common mode rejection. The effectiveness of the variable gain capability is enhanced by the inherent low noise of the AD632: 90μV rms.

PRODUCT HIGHLIGHTS

Guaranteed Performance Over Temperature: The AD632A and AD632B are specified for maximum multiplying errors of ±1.0% and ±0.5% of full scale, respectively at +25°C and are rated for operation from -25°C to +85°C. Maximum multiplying errors of ±2.0% (AD632S) and ±1.0% (AD632T) are guaranteed over the extended temperature range of -55°C to +125°C.

High Reliability: The AD632S and AD632T series are also available with MIL-STD-883 Level B screening and all devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP package.

AD632—SPECIFICATIONS (@ +25°C, V_S = ±15V, R ≥ 2kΩ unless otherwise noted)

Model	AD632A Min	AD632A Typ	AD632A Max	AD632B Min	AD632B Typ	AD632B Max	AD632S Min	AD632S Typ	AD632S Max	AD632T Min	AD632T Typ	AD632T Max	Units
MULTIPLIER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] (−10V≤X, Y≤+10V)			**±1.0**			**±0.5**			**±1.0**			**±0.5**	%
T_A = min to max		**±1.5**			**±1.0**			**±2.0**			**±1.0**		%
Total Error vs Temperature		±0.022			±0.015			**±0.02**			**±0.01**		%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.25			±0.1		%
Temperature-Coefficient of Scaling-Voltage		**±0.02**			**±0.01**			±0.2			**±0.005**		%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	±0.3		±0.4			±0.2	±0.3	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	±0.1		±0.2			±0.1	±0.1	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	±0.3		±0.3			±0.15	±0.3	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	±0.1		±0.01			±0.01	±0.1	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift		200			100				**500**			**300**	µV/°C
DYNAMICS													
Small Signal BW, (V_{OUT} = 0.1rms)		1			1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2			2		µs
NOISE													
Noise Spectral-Density SF = 10V		0.8			0.8			0.8			0.8		µV/√Hz
SF = 3V[4]		0.4			0.4			0.4			0.4		µV/√Hz
Wideband Noise A = 10Hz to 5MHz		1.0			1.0			1.0			1.0		mV rms
P = 10Hz to 10kHz		90			90			90			90		µV/rms
OUTPUT													
Output Voltage Swing	**±11**			**±11**			**±11**			**±11**			V
Output Impedance (f≤1kHz)		0.1			0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]													
Signal Voltage Range (Diff. or CM		±10			±10			±10			±10		V
Operating Diff.)		±12			±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z		200			100				500			300	µV/°C
CMRR	**60**	80		**70**	90		**60**	80		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1			0.1			0.1		µA
Differential Resistance		10			10			10			10		MΩ
DIVIDER PERFORMANCE													
Transfer Function (X_1>X_2)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1]													
(X = 10V, −10V≤Z≤+10V)		±0.75			±0.35			±0.75			±0.35		%
(X = 1V, −1V≤Z≤+1V)		±2.0			±1.0			±2.0			±1.0		%
(0.1V≤X≤10V, −10V≤Z≤10V)		±2.5			±1.0			±2.5			±1.0		%
SQUARER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error (−10V≤X≤10V)		±0.6			±0.3			±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE													
Transfer Function, (Z_1≤Z_2)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] (1V≤Z≤10V)		±1.0			±0.5			±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS													
Supply Voltage													
Rated Performance		±15			±15			±15			±15		V
Operating	±8		**±18**	±8		**±18**	±8		**±22**	±8		±22	V
Supply Current													
Quiescent		4	6		4	6		4	6		4	6	mA
PACKAGE OPTIONS													
TO-100 (H-10A)		AD632AH			AD632BH			AD632SH			AD632TH		
TO-116 (D-14)		AD632AD			AD632BD			AD632SD			AD632TD		

NOTES
[1]Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.

Specifications subject to change without notice.

All min and max specifications are guaranteed.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Typical Performance Curves (typical at +25°C with $\pm V_S$ = 15V)

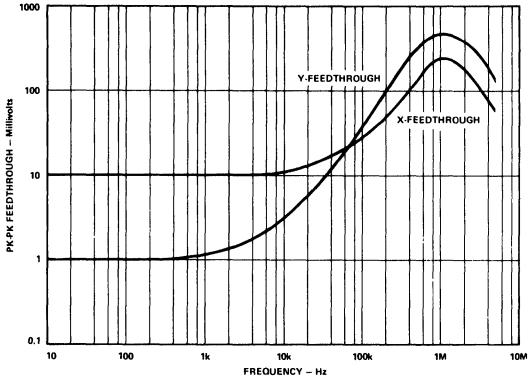


Figure 1. AC Feedthrough vs. Frequency

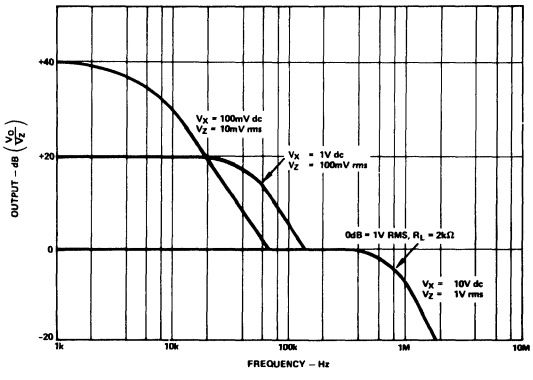


Figure 3. Frequency Response vs. Divider Denominator Input Voltage

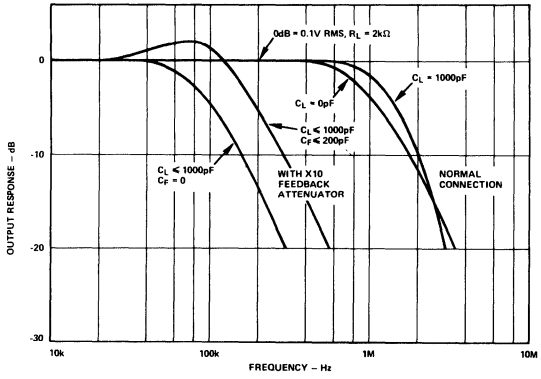
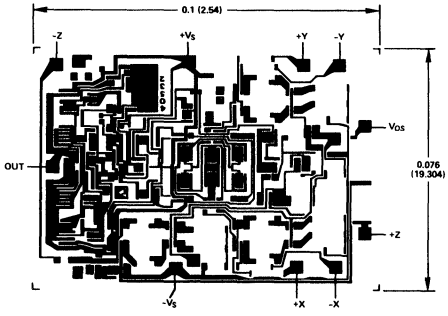


Figure 2. Frequency Response as a Multiplier

CHIP DIMENSIONS & PAD LAYOUT

Dimensions shown in inches and (mm).
(Contact factory for latest dimensions.)



For further information, consult factory

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD632AD	−25°C to +85°C	Side Brazed Ceramic DIP	D-14
AD632BD	−25°C to +85°C	Side Brazed Ceramic DIP	D-14
AD632AH	−25°C to +85°C	Header	H-10A
AD632BH	−25°C to +85°C	Header	H-10A
AD632SD	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD632SD/833B	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD632TD	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD632TD/883B	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD632SH	−55°C to +125°C	Header	H-10A
AD632SH/883B	−55°C to +125°C	Header	H-10A
AD632TH	−55°C to +125°C	Header	H-10A
AD632TH/883B	−55°C to +125°C	Header	H-10A

*For outline information see Package Information section.

Thermal Characteristics

Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14
θ_{JA} = 95°C/W for D-14

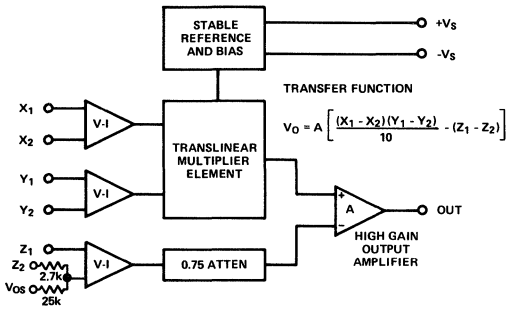


Figure 4. AD632 Functional Block Diagram

OPERATION AS A MULTIPLIER

Figure 5 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

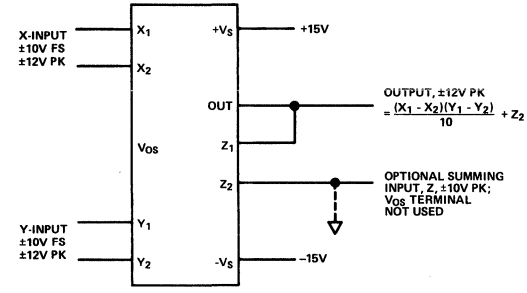


Figure 5. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input. Curve 1 shows the typical ac feedthrough with this adjustment mode. Note that the feedthrough of the Y input is a factor of 10 lower than that of the X input and should be used in applications where null suppression is critical.

The Z_2 terminal of the AD632 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective signal common potentials to realize the full accuracy of the AD632.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 6. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the Z_1 terminal where they are amplified by –10 or to the common ground connection where they are amplified by –1. Input signals may also be applied to the lower end of the 2.7kΩ resistor, giving a gain of +9.

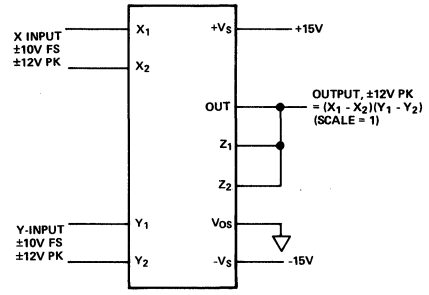


Figure 6. Connections for Scale-Factor of Unity

OPERATION AS A DIVIDER

Figure 7 shows the connection required for division. Unlike earlier products, the AD632 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in Figure 3.

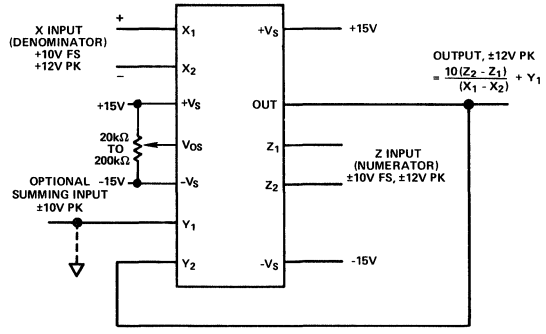


Figure 7. Basic Divider Connection

Without additional trimming, the accuracy of the AD632B is sufficient to maintain a 1% error over a 10V to 1V denominator range (The AD535 is functionally equivalent to the AD632 and has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications).

This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input. To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

*See the AD535 Data Sheet for more details.

ANALOG DEVICES

Low Cost Analog Multiplier

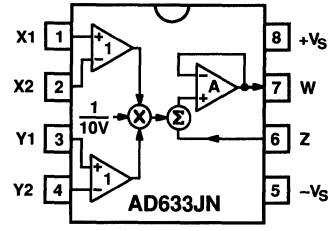
AD633

FEATURES
Four-Quadrant Multiplication
Low Cost 8-Pin Package
Complete—No External Components Required
Laser-Trimmed Accuracy and Stability
Total Error Within 2% of FS
Differential High Impedance X and Y Inputs
High Impedance Unity-Gain Summing Input
Laser-Trimmed 10 V Scaling Reference

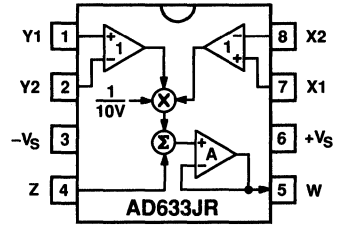
APPLICATIONS
Multiplication, Division, Squaring
Modulation/Demodulation, Phase Detection
Voltage-Controlled Amplifiers/Attenuators/Filters

CONNECTION DIAGRAMS

8-Pin Plastic DIP (N) Package



8-Pin Plastic SOIC (R) Package



$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10V} + Z$$

PRODUCT DESCRIPTION

The AD633 is a functionally complete, four-quadrant, analog multiplier. It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The AD633 is the first product to offer these features in modestly priced 8-pin plastic DIP and SOIC packages.

The AD633 is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y-input is typically less than 0.1% and noise referred to the output is typically less than 100 μV rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz bandwidth, 20 V/μs slew rate, and the ability to drive capacitive loads make the AD633 useful in a wide variety of applications where simplicity and cost are key concerns.

The AD633's versatility is not compromised by its simplicity. The Z-input provides access to the output buffer amplifier, enabling the user to sum the outputs of two or more multipliers, increase the multiplier gain, convert the output voltage to a current, and configure a variety of applications.

The AD633 is available in an 8-pin plastic mini-DIP package (N) and 8-pin SOIC (R) and is specified to operate over the 0°C to +70°C commercial temperature range.

PRODUCT HIGHLIGHTS

1. The AD633 is a complete four-quadrant multiplier offered in low cost 8-pin plastic packages. The result is a product that is cost effective and easy to apply.
2. No external components or expensive user calibration are required to apply the AD633.
3. Monolithic construction and laser calibration make the device stable and reliable.
4. High (10 MΩ) input resistances make signal source loading negligible.
5. Power supply voltages can range from ±8 V to ±18 V. The internal scaling voltage is generated by a stable Zener diode; multiplier accuracy is essentially supply insensitive.

AD633—SPECIFICATIONS (T_A = +25°C, V_S = ±15 V, $R_L \geq 2$ kΩ)

Model		AD633J			
TRANSFER FUNCTION		$W = \frac{(X_1-X_2)(Y_1-Y_2)}{10\,V} + Z$			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
MULTIPLIER PERFORMANCE					
Total Error	−10 V ≤ X, Y ≤ +10 V		±1	**±2**	% Full Scale
T_{min} to T_{max}			±3		% Full Scale
Scale Voltage Error	SF = 10.00 V Nominal		±0.25%		% Full Scale
Supply Rejection	V_S = ±14 V to ±16 V		±0.01		% Full Scale
Nonlinearity, X	X = ±10 V, Y = +10 V		±0.4	**±1**	% Full Scale
Nonlinearity, Y	Y = ±10 V, X = +10 V		±0.1	**±0.4**	% Full Scale
X Feedthrough	Y Nulled, X = ±10 V		±0.3	**±1**	% Full Scale
Y Feedthrough	X Nulled, Y = ±10 V		±0.1	**±0.4**	% Full Scale
Output Offset Voltage			±5	**±50**	mV
DYNAMICS					
Small Signal BW	V_O = 0.1 V rms,		1		MHz
Slew Rate	V_O = 20 V p–p		20		V/μs
Settling Time to 1%	Δ V_O = 20 V		2		μs
OUTPUT NOISE					
Spectral Density			0.8		$\mu V/\sqrt{Hz}$
Wideband Noise	f = 10 Hz to 5 MHz		1		mV rms
	f = 10 Hz to 10 kHz		90		μV rms
OUTPUT					
Output Voltage Swing		**±11**			V
Short Circuit Current	R_L = 0 Ω		30	**40**	mA
INPUT AMPLIFIERS					
Signal Voltage Range	Differential	**±10**			V
	Common Mode	**±10**			V
Offset Voltage X, Y			±5	**±30**	mV
CMRR X, Y	V_{CM} = ±10 V, f = 50 Hz	**60**	80		dB
Bias Current X, Y, Z			0.8	**2.0**	μA
Differential Resistance			10		MΩ
POWER SUPPLY					
Supply Voltage					
Rated Performance			±15		V
Operating Range		**±8**		**±18**	V
Supply Current	Quiescent		4	**6**	mA

NOTES

Specifications shown in **boldface** are tested on all production units at electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 500 mW
Input Voltages[3] . . . . . ±18 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . 0°C to +70°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

[2]8-Pin Plastic Package: θ_{JA} = 165°C/W; 8-Pin Small Outline Package: θ_{JA} = 155°C/W.

[3]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING GUIDE

Model	Description	Package Option*
AD633JN	8-Pin Plastic DIP	N-8
AD633JR	8-Pin Plastic SOIC	R-8
AD633JR-REEL	8-Pin Plastic SOIC	R-8

*For outline information see Package Information section.

FUNCTIONAL DESCRIPTION

The AD633 is a low cost multiplier comprising a translinear core, a buried Zener reference, and a unity gain connected output amplifier with an accessible summing node. Figure 1 shows the functional block diagram. The differential X and Y inputs are converted to differential currents by voltage-to-current converters. The product of these currents is generated by the multiplying core. A buried Zener reference provides an overall scale factor of 10 V. The sum of $(X \cdot Y)/10 + Z$ is then applied to the output amplifier. The amplifier summing node Z allows the user to add two or more multiplier outputs, convert the output voltage to a current, and configure various analog computational functions.

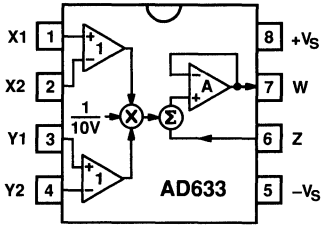


Figure 1. AD633 Functional Block Diagram (AD633JN Pinout Shown)

Inspection of the block diagram shows the overall transfer function to be:

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{10\ V} + Z \qquad \text{(Eq. 1)}$$

ERROR SOURCES

Multiplier errors consist primarily of input and output offsets, scale factor error, and nonlinearity in the multiplying core. The input and output offsets can be eliminated by using the optional trim of Figure 2. This scheme reduces the net error to scale factor errors (gain error) and an irreducible nonlinearity component in the multiplying core. The X and Y nonlinearities are typically 0.4% and 0.1% of full scale, respectively. Scale factor error is typically 0.25% of full scale. The high impedance Z input should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise, the differential X and Y inputs should be referenced to their respective grounds to realize the full accuracy of the AD633.

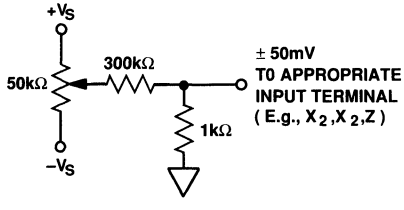


Figure 2. Optional Offset Trim Configuration

APPLICATIONS

The AD633 is well suited for such applications as modulation and demodulation, automatic gain control, power measurement, voltage controlled amplifiers, and frequency doublers. Note that these applications show the pin connections for the AD633JN pinout (8-pin DIP), which differs from the AD633JR pinout (8-pin SOIC).

Multiplier Connections

Figure 3 shows the basic connections for multiplication. The X and Y inputs will normally have their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both may be driven.

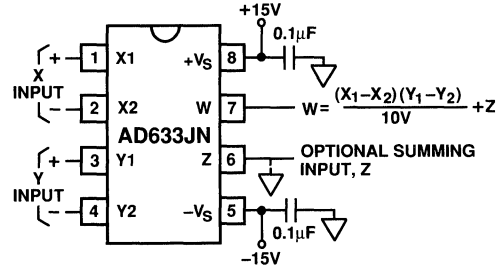


Figure 3. Basic Multiplier Connections

Squaring and Frequency Doubling

As Figure 4 shows, squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel to produce an output of $E^2/10$ V. The input may have either polarity, but the output will be positive. However, the output polarity may be reversed by interchanging the X or Y inputs. The Z input may be used to add a further signal to the output.

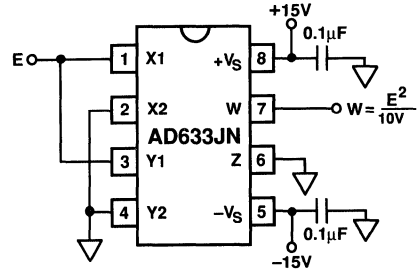


Figure 4. Connections for Squaring

When the input is a sine wave E sin ωt, this squarer behaves as a frequency doubler, since

$$\frac{(E\ sin\ \omega t)^2}{10\ V} = \frac{E^2}{20\ V}(1 - cos\ 2\ \omega t) \qquad \text{(Eq. 2)}$$

Equation 2 shows a dc term at the output which will vary strongly with the amplitude of the input, E. This can be

avoided using the connections shown in Figure 5, where an RC network is used to generate two signals whose product has no dc term. It uses the identity:

$$\cos\theta \sin\theta = \frac{1}{2}(\sin 2\theta) \qquad \text{(Eq. 3)}$$

At $\omega_o = 1/CR$, the X input leads the input signal by 45° (and is attenuated by $\sqrt{2}$), and the Y input lags the X input by 45° (and is also attenuated by $\sqrt{2}$). Since the X and Y inputs are 90° out of phase, the response of the circuit will be (satisfying Equation 3.):

$$W = \frac{1}{(10\ V)}\frac{E}{\sqrt{2}}(\sin(\omega_o t + 45°))\frac{E}{\sqrt{2}}(\sin(\omega_o t - 45°))$$
$$= \frac{E^2}{(40\ V)}(\sin 2\omega_o t) \qquad \text{(Eq. 4)}$$

which has no dc component. Resistors R1 and R2 are included to restore the output amplitude to 10 V for an input amplitude of 10 V.

The amplitude of the output is only a weak function of frequency: the output amplitude will be 0.5% too low at $\omega = 0.9\ \omega_o$ and $\omega = 1.1\ \omega_o$.

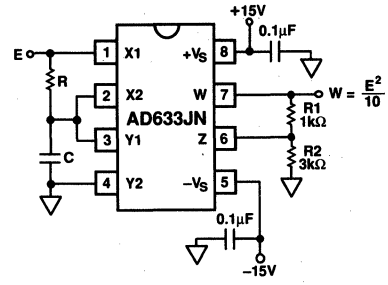


Figure 5. "Bounceless" Frequency Doubler

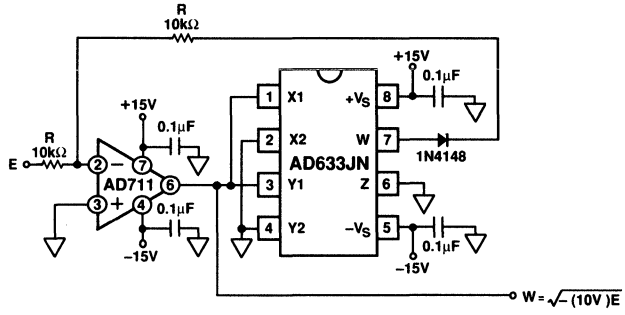


Figure 6. Connections for Square Rooting

Generating Inverse Functions

Inverse functions of multiplication, such as division and square rooting, can be implemented by placing a multiplier in the feedback loop of an op amp. Figure 6 shows how to implement a square rooter with the transfer function

$$W = \sqrt{-(10\ V)E} \qquad \text{(Eq. 5)}$$

for the condition E<0.

Likewise, Figure 7 shows how to implement a divider using a multiplier in a feedback loop. The transfer function for the divider is

$$W = -(10\ V)\frac{E}{E_X} \qquad \text{(Eq. 6)}$$

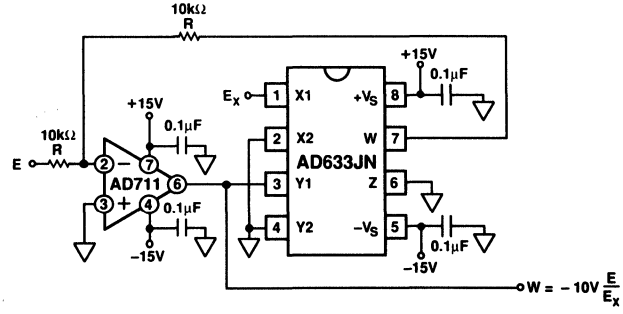


Figure 7. Connections for Division

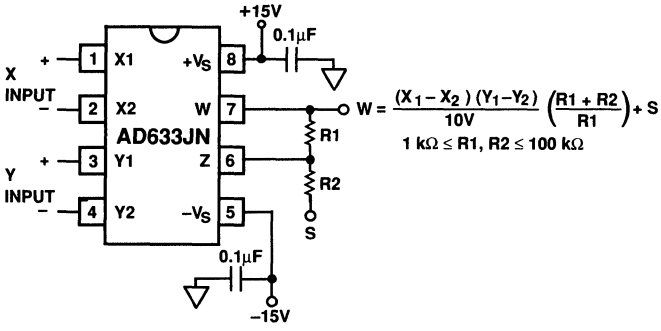


Figure 8. Connections for Variable Scale Factor

Variable Scale Factor

In some instances, it may be desirable to use a scaling voltage other than 10V. The connections shown in Figure 8 increase the gain of the system by the ratio (R1 + R2)/R1. This ratio is limited to 100 in practical applications. The summing input, S, may be used to add an additional signal to the output or it may be grounded.

Current Output

The AD633's voltage output can be converted to a current output by the addition of a resistor R between the AD633's W and Z pins as shown in Figure 9 below. This arrangement forms the basis of voltage controlled integrators and oscillators as will be shown later in this Applications section. The transfer function of this circuit has the form

$$I_O = \frac{1}{R}\frac{(X_1-X_2)(Y_1-Y_2)}{10\ V} \qquad \text{(Eq. 7)}$$

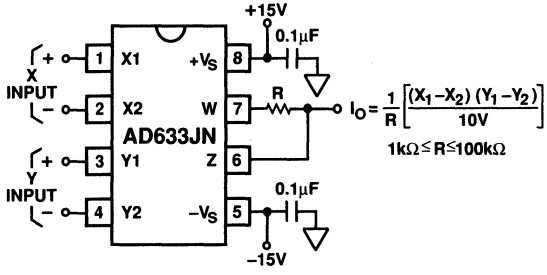


Figure 9. Current Output Connections

Linear Amplitude Modulator

The AD633 can be used as a linear amplitude modulator with no external components. Figure 10 shows the circuit. The carrier and modulation inputs to the AD633 are multiplied to produce a double-sideband signal. The carrier signal is fed forward to the AD633's Z input where it is summed with the double-sideband signal to produce a double-sideband with carrier output.

Voltage Controlled Low Pass and High Pass Filters

Figure 11 shows a single multiplier used to build a voltage controlled low pass filter. The voltage at output A is a result of filtering, E_S. The break frequency is modulated by E_C, the control input. The break frequency, f_2, equals

$$f_2 = \frac{E_C}{(20\ V)\ \pi\ RC} \qquad \text{(Eq. 8)}$$

and the rolloff is 6 dB per octave. This output, which is at a high impedance point, may need to be buffered.

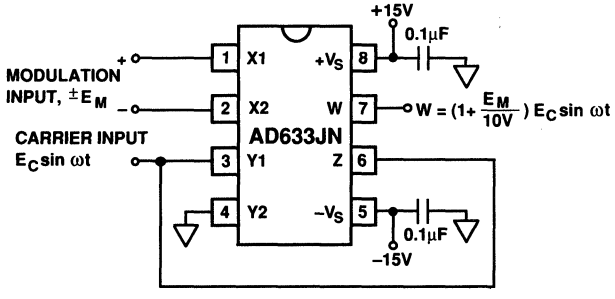


Figure 10. Linear Amplitude Modulator

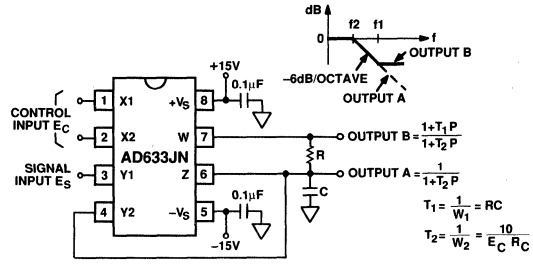


Figure 11. Voltage Controlled Low Pass Filter

The voltage at output B, the direct output of the AD633, has the same response up to frequency f_1, the natural breakpoint of the RC filter,

$$f_1 = \frac{1}{2\pi RC} \qquad \text{(Eq. 9)}$$

then levels off to a constant attenuation of $f_1/f_2 = E_C/10$.

For example, if R = 8 kΩ and C = 0.002 μF, then output A has a pole at frequencies from 100 Hz to 10 kHz for E_C ranging from 100 mV to 10 V. Output B has an additional zero at 10 kHz (and can be loaded because it is the multiplier's low impedance output). The circuit can be changed to a high pass filter by interchanging the resistor and capacitor as shown in Figure 12, below.

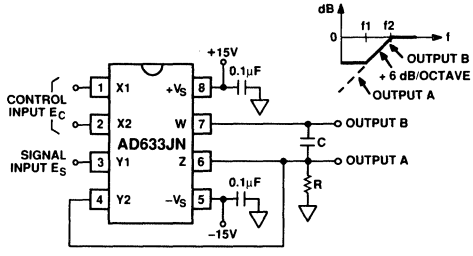


Figure 12. Voltage Controlled High Pass Filter

Voltage Controlled Quadrature Oscillator

Figure 13 shows two multipliers being used to form integrators with controllable time constants in a 2nd order differential equation feedback loop. R2 and R5 provide controlled current output operation. The currents are integrated in capacitors C1 and C2, and the resulting voltages at high impedance are applied to the X inputs of the "next" AD633. The frequency control input, E_C, connected to the Y inputs, varies the integrator gains with a calibration of 100 Hz/V. The accuracy is limited by the Y-input offsets. The practical tuning range of this circuit is 100:1. C2 (proportional to C1 and C3), R3, and R4 provide regenerative feedback to start and maintain oscillation. The diode bridge, D1 through D4 (1N914s), and Zener diode D5 provide economical temperature stabilization and amplitude stabilization at ±8.5 V by degenerative damping. The output from the second integrator (10 V sin ωt) has the lowest distortion.

AGC AMPLIFIERS

Figure 14 shows an AGC circuit that uses an rms-dc converter to measure the amplitude of the output waveform. The AD633 and A1, 1/2 of an AD712 dual op amp, form a voltage controlled amplifier. The rms dc converter, an AD736, measures the rms value of the output signal. Its output drives A2, an integrator/comparator, whose output controls the gain of the voltage controlled amplifier. The 1N4148 diode prevents the output of A2 from going negative. R8, a 50 kΩ variable resistor, sets the circuit's output level. Feedback around the loop forces the voltages at the inverting and noninverting inputs of A2 to be equal, thus the AGC.

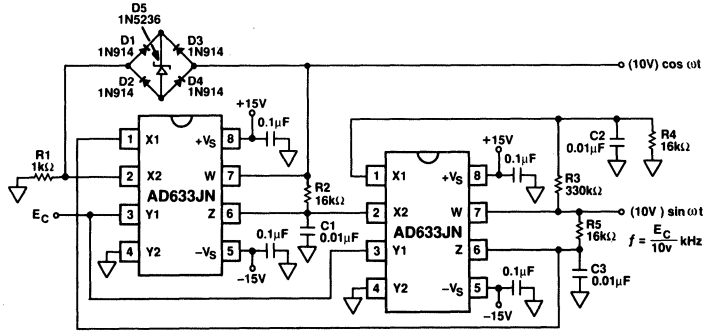


Figure 13. Voltage Controlled Quadrature Oscillator

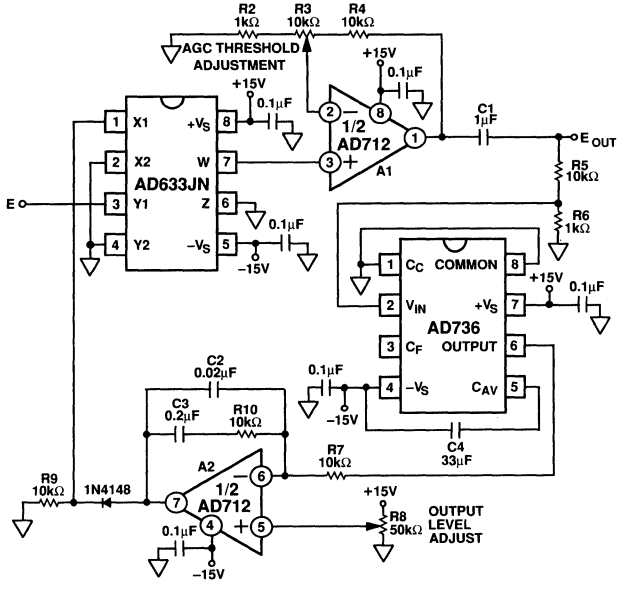


Figure 14. Connections for Use in Automatic Gain Control Circuit

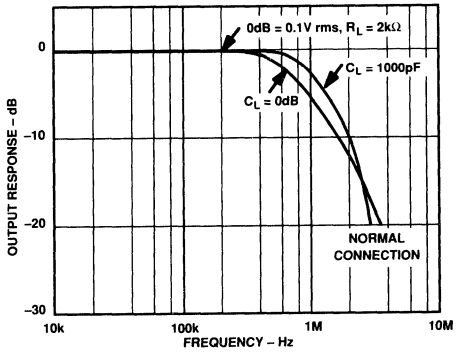


Figure 15. Frequency Response

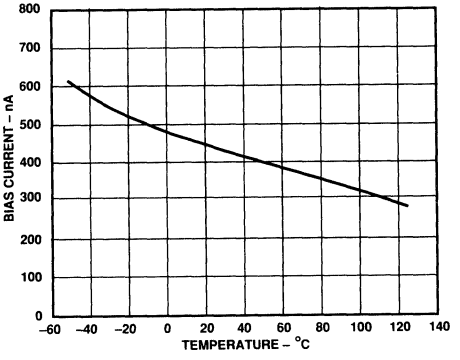


Figure 16. Input Bias Current vs. Temperature (X, Y, or Z Inputs)

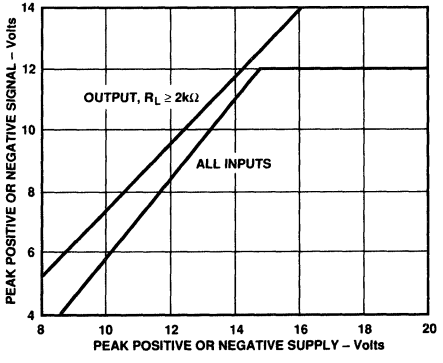


Figure 17. Input and Output Signal Ranges vs. Supply Voltages

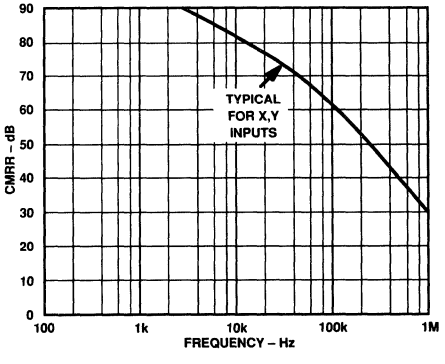


Figure 18. CMRR vs. Frequency

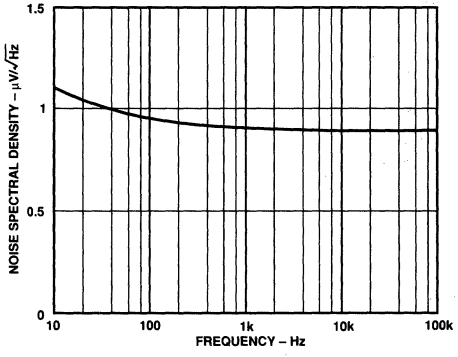


Figure 19. Noise Spectral Density vs. Frequency

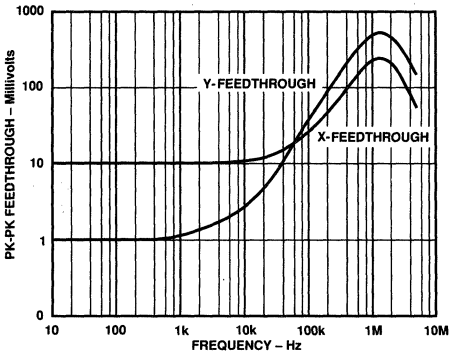


Figure 20. AC Feedthrough vs. Frequency

10 MHz, 4-Quadrant Multiplier/Divider

AD734

FEATURES

High Accuracy
- **0.1% Typical Error**

High Speed
- **10 MHz Full-Power Bandwidth**
- **450 V/μs Slew Rate**
- **200 ns Settling to 0.1% at Full Power**

Low Distortion
- **−80 dBc from Any Input**
- **Third-Order IMD Typically −75 dBc at 10 MHz**

Low Noise
- **94 dB SNR, 10 Hz to 20 kHz**
- **70 dB SNR, 10 Hz to 10 MHz**

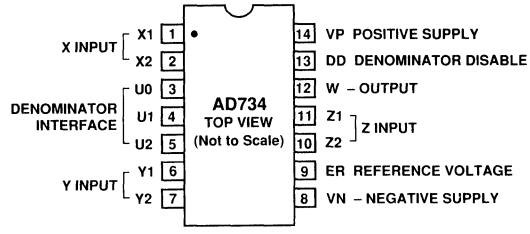
Direct Division Mode
- **2 MHz BW at Gain of 100**

APPLICATIONS

High Performance Replacement for AD534
Multiply, Divide, Square, Square Root
Modulator, Demodulator
Wideband Gain Control, RMS-DC Conversion
Voltage-Controlled Amplifiers, Oscillators, and Filters
Demodulator with 40 MHz Input Bandwidth

CONNECTION DIAGRAM

14-Pin DIP
(Q Package)



PRODUCT DESCRIPTION

The AD734 is an accurate high speed, four-quadrant analog multiplier that is pin-compatible with the industry-standard AD534 and provides the transfer function W = XY/U. The AD734 provides a low-impedance voltage output with a full-power (20 V pk–pk) bandwidth of 10 MHz. Total static error (scaling, offsets, and nonlinearities combined) is 0.1% of Full Scale. Distortion is typically less than −80 dBc and guaranteed. The low-capacitance X, Y and Z inputs are fully differential. In most applications, no external components are required to define the function.

The internal scaling (denominator) voltage U is 10 V, derived from a buried-Zener voltage reference. A new feature provides the option of substituting an external denominator voltage, allowing the use of the AD734 as a two-quadrant divider with a 1000:1 denominator range and a signal bandwidth that remains 10 MHz to a gain of 20 dB, 2 MHz at a gain of 40 dB and 200 kHz at a gain of 60 dB, for a gain-bandwidth product of 200 MHz.

The advanced performance of the AD734 is achieved by a combination of new circuit techniques, the use of a high speed complementary bipolar process and a novel approach to laser-trimming based on ac signals rather than the customary dc methods. The wide bandwidth (>40 MHz) of the AD734's input stages and the 200 MHz gain-bandwidth product of the multiplier core allow the AD734 to be used as a low distortion demodulator with input frequencies as high as 40 MHz as long as the desired output frequency is less than 10 MHz.

The AD734AQ and AD734BQ are specified for the industrial temperature range of −40°C to +85°C and come in a 14-pin ceramic DIP. The AD734SQ/883B, available processed to MIL-STD-883B for the military range of −55°C to +125°C, is available in a 14-pin ceramic DIP.

PRODUCT HIGHLIGHTS

The AD734 embodies more than two decades of experience in the design and manufacture of analog multipliers, to provide:

1. A new output amplifier design with more than twenty times the slew-rate of the AD534 (450 V/μs versus 20 V/μs) for a full power (20 V pk–pk) bandwidth of 10 MHz.
2. Very low distortion, even at full power, through the use of circuit and trimming techniques that virtually eliminate all of the spurious nonlinearities found in earlier designs.
3. Direct control of the denominator, resulting in higher multiplier accuracy and a gain-bandwidth product at small denominator values that is typically 200 times greater than that of the AD534 in divider modes.
4. Very clean transient response, achieved through the use of a novel input stage design and wide-band output amplifier, which also ensure that distortion remains low even at high frequencies.
5. Superior noise performance by careful choice of device geometries and operating conditions, which provide a guaranteed 88 dB of dynamic range in a 20 kHz bandwidth.

AD734—SPECIFICATIONS (T_A = +25°C, $+V_S$ = VP = +15 V, $-V_S$ = VN = −15 V, $R_L \geq 2$ kΩ)

TRANSFER FUNCTION

$$W = A_O\left\{\frac{(X_1-X_2)(Y_1-Y_2)}{(U_1-U_2)} - (Z_1 - Z_2)\right\}$$

Parameter	Conditions	A Min	A Typ	A Max	B Min	B Typ	B Max	S Min	S Typ	S Max	Units
MULTIPLIER PERFORMANCE											
Transfer Function			W = XY/10			W = XY/10			W = XY/10		
Total Static Error[1]	−10 V ≤ X,Y ≤ 10 V		0.1	**0.4**		0.1	**0.25**		0.1	**0.4**	%
Over T_{min} to T_{max}				**1**			**0.6**			**1.25**	%
vs. Temperature	T_{min} to T_{max}		0.004			0.003			0.004		%/°C
vs. Either Supply	$\pm V_S$ = 14 V to 16 V		0.01	**0.05**		0.01	**0.05**		0.01	**0.05**	%/V
Peak Nonlinearity	−10 V ≤ X ≤ +10 V, Y = +10 V		0.05			0.05			0.05		%
	−10 V ≤ Y ≤ +10 V, X = +10 V		0.025			0.025			0.025		%
THD[2]	X = 7 V rms, Y = +10 V, f ≤ 5 kHz			**−58**			**−66**			**−58**	dBc
	T_{min} to T_{max}			**−55**			**−63**			**−55**	dBc
	Y = 7 V rms, X = +10 V, f ≤ 5 kHz			**−60**			**−80**			**−60**	dBc
	T_{min} to T_{max}			**−57**			**−74**			**−57**	dBc
Feedthrough	X = 7 V rms, Y = nulled, f ≤ 5 kHz		−85	**−60**		−85	**−70**		−85	**−60**	dBc
	Y = 7 V rms, X = nulled, f ≤ 5 kHz		−85	**−66**		−85	**−76**		−85	**−66**	dBc
Noise (RTO)	X = Y = 0										
Spectral Density	100 Hz to 1 MHz		1.0			1.0			1.0		$\mu V/\sqrt{Hz}$
Total Output Noise	10 Hz to 20 kHz		−94	**−88**		−94	**−88**		−94	**−88**	dBc
	T_{min} to T_{max}			**−85**			**−85**			**−85**	dBc
DIVIDER PERFORMANCE (Y = 10 V)											
Transfer Function			W = XY/U			W = XY/U			W = XY/U		
Gain Error	Y = 10 V, U = 100 mV to 10 V		1			1			1		%
X Input Clipping Level	Y ≤ 10 V		1.25 × U			1.25 × U			1.25 × U		V
U Input Scaling Error[3]				**0.3**			**0.15**			**0.3**	%
	T_{min} to T_{max}			**0.8**			**0.65**			**1**	%
(Output to 1%)	U = 1 V to 10 V Step , X = 1 V		100			100			100		ns
INPUT INTERFACES (X, Y, & Z)											
3 dB Bandwidth			40			40			40		MHz
Operating Range	Differential or Common Mode		±12.5			±12.5			±12.5		V
X Input Offset Voltage				**15**			**5**			**15**	mV
	T_{min} to T_{max}			**25**			**15**			**25**	mV
Y Input Offset Voltage				**10**			5			**10**	mV
	T_{min} to T_{max}			**12**			**6**			**12**	mV
Z Input Offset Voltage				**20**			**10**			**20**	mV
	T_{min} to T_{max}			**50**			**50**			**90**	mV
Z Input PSRR (Either Supply)	f ≤ 1 kHz	**54**	70		**66**	70		**54**	70		dB
	T_{min} to T_{max}	**50**			**56**			**50**			dB
CMRR	f = 5 kHz	**70**	85		**70**	85		**70**	85		dB
Input Bias Current (X, Y, Z Inputs)			50	**300**		50	**150**		50	**300**	nA
	T_{min} to T_{max}			**400**			**300**			**500**	nA
Input Resistance	Differential		50			50			50		kΩ
Input Capacitance	Differential		2			2			2		pF
DENOMINATOR INTERFACES (U0, U1, & U2)											
Operating Range			VN to VP-3			VN to VP-3			VN to VP-3		V
Denominator Range			1000:1			1000:1			1000:1		
Interface Resistor	U1 to U2		28			28			28		kΩ
OUTPUT AMPLIFIER (W)											
Output Voltage Swing	T_{min} to T_{max}	±12			±12			±12			V
Open-Loop Voltage Gain	X = Y = 0, Input to Z		72			72			72		dB
Dynamic Response	From X or Y Input, CL ≤ 20 pF										
3 dB Bandwidth	W ≤ 7 V rms	8	10		8	10		8	10		MHz
Slew Rate			450			450			450		V/μs
Settling Time	+20 V or −20 V Output Step										
To 1%			125			125			125		ns
To 0.1%			200			200			200		ns
Short-Circuit Current	T_{min} to T_{min}	**20**	50	80	**20**	50	80	**20**	50	80	mA
POWER SUPPLIES, $\pm V_S$											
Operating Supply Range		±8		±16.5	±8		±16.5	±8		±16.5	V
Quiescent Current	T_{min} to T_{max}	6	9	**12**	6	9	**12**	6	9	**12**	mA

NOTES

[1]Figures given are percent of full scale (e.g., 0.01% = 1 mV).

[2]dBc refers to deciBels relative to the full scale input (carrier) level of 7 V rms.

[3]See Figure 10 for test circuit.

All min and max specifications are guaranteed. Specifications in **Boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2]
for T_J max = 175°C . . . . . 500 mW
X, Y and Z Input Voltages . . . . . VN to VP
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range
Q . . . . . −65°C to +150°C
Operating Temperature Range
AD734A, B (Industrial) . . . . . −40°C to +85°C
AD734S (Military) . . . . . −55°C to +125°C
Lead Temperature Range (soldering 60 sec) . . . . . +300°C
Transistor Count 81

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.
[2]14-Pin Ceramic DIP: θ_{JA} = 110°C/W

ORDERING GUIDE

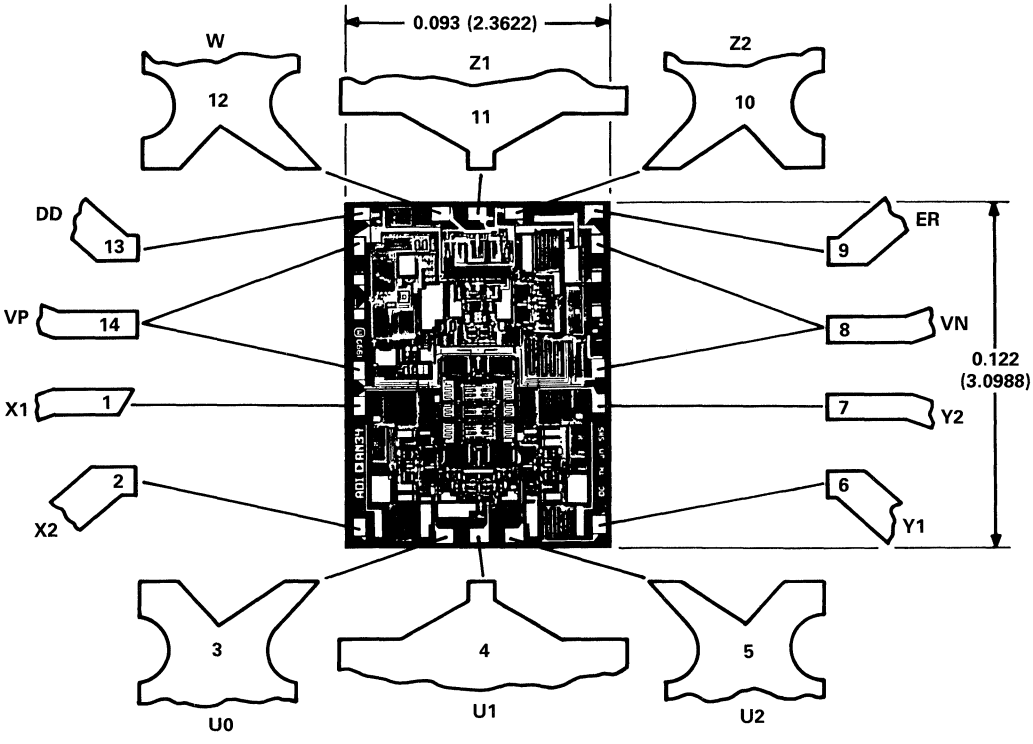
Model	Temperature Range	Package Description	Package Option*
AD734AN	−40°C to +85°C	Plastic DIP	N-14
AD734BN	−40°C to +85°C	Plastic DIP	N-14
AD734AQ	−40°C to +85°C	Cerdip	Q-14
AD734BQ	−40°C to +85°C	Cerdip	Q-14
AD734SQ	−55°C to +125°C	Cerdip	Q-14
AD734S Chip	−55°C to +125°C	Chip	

*For outline information see Package Information section.

2

CHIP DIMENSIONS & BONDING DIAGRAM

Dimensions shown in inches and (mm).
(Contact factory for latest dimensions.)



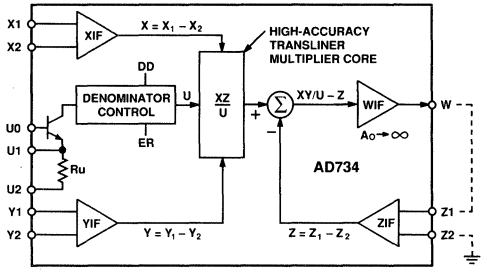


Figure 1. AD734 Block Diagram

FUNCTIONAL DESCRIPTION

Figure 1 is a simplified block diagram of the AD734. Operation is similar to that of the industry-standard AD534 and in many applications these parts are pin-compatible. The main functional difference is the provision for direct control of the denominator voltage, U, explained fully on the following page. Internal signals are actually in the form of currents, but the function of the AD734 can be understood using voltages throughout, as shown in this figure. Pins are named using upper-case characters (such as X1, Z2) while the *voltages* on these pins are denoted by subscripted variables (for example, X_1, Z_2).

The AD734's differential X, Y and Z inputs are handled by wideband interfaces that have low offset, low bias current and low distortion. The AD734 responds to the difference signals $X = X_1 - X_2$, $Y = Y_1 - Y_2$ and $Z = Z_1 - Z_2$, and rejects common-mode voltages on these inputs. The X, Y and Z interfaces provide a nominal full-scale (FS) voltage of ±10 V, but, due to the special design of the input stages, the linear range of the differential input can be as large as ±17 V. Also unlike previous designs, the response on these inputs is not clipped abruptly above ±15 V, but drops to a slope of one half.

The bipolar input signals X and Y are multiplied in a translinear core of novel design to generate the product XY/U. The denominator voltage, U, is internally set to an accurate, temperature-stable value of 10 V, derived from a buried-Zener reference. An uncalibrated fraction of the denominator voltage U appears between the voltage reference pin (ER) and the negative supply pin (VN), for use in certain applications where a temperature-compensated voltage reference is desirable. The internal denominator, U, can be disabled, by connecting the denominator disable Pin 13 (DD) to the positive supply pin (VP); the denominator can then be replaced by a fixed or variable external voltage ranging from 10 mV to more than 10 V.

The high-gain output op-amp nulls the difference between XY/U and an additional signal Z, to generate the final output W. The actual transfer function can take on several forms, depending on the connections used. The AD734 can perform all of the functions supported by the AD534, and new functions using the direct-division mode provided by the U-interface.

Each input pair (X1 and X2, Y1 and Y2, Z1 and Z2) has a differential input resistance of 50 kΩ; this is formed by "real" resistors (not a small-signal approximation) and is subject to a tolerance of ±20%. The common-mode input resistance is several megohms and the parasitic capacitance is about 2 pF.

The bias currents associated with these inputs are nulled by laser-trimming, such that when one input of a pair is optionally ac-coupled and the other is grounded, the residual offset voltage is typically less than 5 mV, which corresponds to a bias current of only 100 nA. This low bias current ensures that mismatches in the sources resistances at a pair of inputs does not cause an offset error. These currents remain low over the full temperature range and supply voltages.

The common-mode range of the X, Y and Z inputs does not fully extend to the supply rails. Nevertheless, it is often possible to operate the AD734 with one terminal of an input pair connected to either the positive or negative supply, unlike previous multipliers. The common-mode resistance is several megohms.

The full-scale output of ±10 V can be delivered to a load resistance of 1 kΩ (although the specifications apply to the standard multiplier load condition of 2 kΩ). The output amplifier is stable driving capacitive loads of at least 100 pF, when a slight increase in bandwidth results from the peaking caused by this capacitance. The 450 V/μs slew rate of the AD734's output amplifier ensures that the bandwidth of 10 MHz can be maintained up to the full output of 20 V pk-pk. Operation at reduced supply voltages is possible, down to ±8 V, with reduced signal levels.

Available Transfer Functions

The uncommitted (open-loop) transfer function of the AD734 is

$$W = A_O \left\{ \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} - (Z_1 - Z_2) \right\}, \quad (1)$$

where A_O is the open-loop gain of the output op-amp, typically 72 dB. When a negative feedback path is provided, the circuit will force the quantity inside the brackets essentially to zero, resulting in the equation

$$(X_1 - X_2)(Y_1 - Y_2) = U\,(Z_1 - Z_2). \quad (2)$$

This is the most useful generalized transfer function for the AD734; it expresses a balance between the product XY and the product UZ. The absence of the output, W, in this equation only reflects the fact that we have not yet specified which of the inputs is to be connected to the op-amp output.

Most of the functions of the AD734 (including division, unlike the AD534 in this respect) are realized with Z_1 connected to W. So, substituting W in place of Z_1 in the above equation results in an output.

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{U} + Z_2. \quad (3)$$

The free input Z2 can be used to sum another signal to the output; in the absence of a product signal, W simply follows the voltage at Z2 with the full 10 MHz bandwidth. When not needed for summation, Z2 should be connected to the ground associated with the load circuit. We can show the allowable polarities in the following shorthand form:

$$(\pm W) = \frac{(\pm X)(\pm Y)}{(+U)} + \pm Z. \quad (4)$$

In the recommended direct divider mode, the Y input is set to a fixed voltage (typically 10 V) and U is varied directly; it may have any value from 10 mV to 10 V. The magnitude of the ratio X/U cannot exceed 1.25; for example, the peak X-input for U = 1 V is ±1.25 V. Above this level, clipping occurs at the positive and negative extremities of the X-input. Alternatively, the AD734 can be operated using the standard (AD534) divider connections (Figure 8), when the negative feedback path is established via the Y_2 input. Substituting W for Y_2 in Equation (2),

we get

$$W = U\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1. \quad (5)$$

In this case, note that the variable X is now the denominator, and the above restriction (X/U ≤ 1.25) on the magnitude of the X input does not apply. However, X must be positive in order for the feedback polarity to be correct. Y_1 can be used for summing purposes or connected to the load ground if not needed. The shorthand form in this case is

$$(\pm W) = (+U)\frac{(\pm Z)}{(+X)} + (\pm Y). \quad (6)$$

In some cases, feedback may be connected to two of the available inputs. This is true for the square-rooting connections (Figure 9), where W is connected to both X_1 and Y_2. Setting X_1 = W and Y_2 = W in Equation (2), and anticipating the possibility of again providing a summing input, so setting X_2 = S and Y_1 = S, we find, in shorthand form

$$(\pm W) = \sqrt{(+U)(+Z)} + (\pm S). \quad (7)$$

This is seen more generally to be the geometric-mean function, since both U and Z can be variable; operation is restricted to one quadrant. Feedback may also be taken to the U-interface. Full details of the operation in these modes is provided in the appropriate section of this data sheet.

Direct Denominator Control

A valuable new feature of the AD734 is the provision to replace the internal denominator voltage, U, with any value from +10 mV to +10 V. This can be used (1) to simply alter the multiplier scaling, thus improve accuracy and achieve reduced noise levels when operating with small input signals; (2) to implement an accurate two-quadrant divider, with a 1000:1 gain range and an asymptotic gain-bandwidth product of 200 MHz; (3) to achieve certain other special functions, such as AGC or rms.

Figure 2 shows the internal circuitry associated with denominator control. Note first that the denominator is actually proportional to a current, Iu, having a nominal value of 356 μA for U = 10 V, whereas the primary reference is a voltage, generated by a buried-Zener circuit and laser-trimmed to have a very low temperature coefficient. This voltage is nominally 8 V with a tolerance of ±10%.

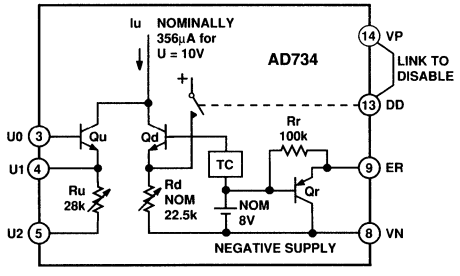


Figure 2. Denominator Control Circuitry

After temperature-correction (block TC), the reference voltage is applied to transistor Qd and trimmed resistor Rd, which generate the required reference current. Transistor Qu and resistor Ru are not involved in setting up the internal denominator, and their associated control pins U0, U1 and U2 will normally be grounded. The reference voltage is also made available, via the 100 kΩ resistor Rr, at Pin 9 (ER); the purpose of Qr is explained below.

When the control pin DD (denominator disable) is connected to VP, the internal source of Iu is shut off, and the collector current of Qu must provide the denominator current. The resistor Ru is laser-trimmed such that the multiplier denominator is exactly equal to the voltage across it (that is, across pins U1 and U2). Note that this trimming only sets up the correct internal ratio; the absolute value of Ru (nominally 28 kΩ) has a tolerance of ±20%. Also, the alpha of Qu, (typically 0.995) which might be seen as a source of scaling error, is canceled by the alpha of other transistors in the complete circuit.

In the simplest scheme (Figure 3), an externally-provided control voltage, V_G, is applied directly to U0 and U2 and the resulting voltage across Ru is therefore reduced by one V_{BE}. For example, when V_G = 2 V, the actual value of U will be about 1.3 V. This error will not be important in some closed-loop applications, such as automatic gain control (AGC), but clearly is not acceptable where the denominator value must be well-defined. When it is required to set up an accurate, fixed value of U, the on-chip reference may be used. The transistor Qr is provided to cancel the V_{BE} of Qu, and is biased by an external resistor, R2, as shown in Figure 4. R1 is chosen to set the desired value of U and consists of a fixed and adjustable resistor.

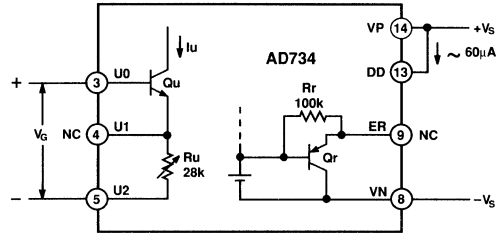


Figure 3. Low-Accuracy Denominator Control

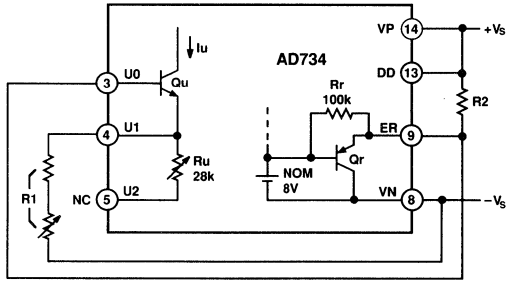


Figure 4. Connections for a Fixed Denominator

Table I shows useful values of the external components for setting up nonstandard denominator values.

Denominator	R1 (Fixed)	R1 (Variable)	R2
5 V	34.8 kΩ	20 kΩ	120 kΩ
3 V	64.9 kΩ	20 kΩ	220 kΩ
2 V	86.6 kΩ	50 kΩ	300 kΩ
1 V	174 kΩ	100 kΩ	620 kΩ

Table I. Component Values for Setting Up Nonstandard Denominator Values

The denominator can also be current controlled, by grounding Pin 3 (U0) and withdrawing a current of Iu from Pin 4 (U1). The nominal scaling relationship is U = 28 × Iu, where u is expressed in volts and Iu is expressed in milliamps. Note, however, that while the linearity of this relationship is very good, it is subject to a scale tolerance of ±20%. Note that the common mode range on Pins 3 through 5 actually extends from 4 V to 36 V below VP, so it is not necessary to restrict the connection of U0 to ground if it should be desirable to use some other voltage.

The output ER may also be buffered, re-scaled and used as a general-purpose reference voltage. It is generated with respect to the negative supply line Pin 8 (VN), but this is acceptable when driving one of the signal interfaces. An example is shown in Figure 12, where a fixed numerator of 10 V is generated for a divider application. There, Y_2 is tied to VN but Y_1 is 10 V above this; therefore the common-mode voltage at this interface is still 5 V above VN, which satisfies the internal biasing requirements (see Specifications Table).

OPERATION AS A MULTIPLIER

All of the connection schemes used in this section are essentially identical to those used for the AD534, with which the AD734 is pin-compatible. The only precaution to be noted in this regard is that in the AD534, Pins 3, 5, 9, and 13 are not internally connected and Pin 4 has a slightly different purpose. In many cases, an AD734 can be directly substituted for an AD534 with immediate benefits in static accuracy, distortion, feedthrough, and speed. Where Pin 4 was used in an AD534 application to achieve a reduced denominator voltage, this function can now be much more precisely implemented with the AD734 using alternative connections (see Direct Denominator Control, page 5).

Operation from supplies down to ±8 V is possible. The supply current is essentially independent of voltage. As is true of all high speed circuits, careful power-supply decoupling is important in maintaining stability under all conditions of use. The decoupling capacitors should always be connected to the load ground, since the load current circulates in these capacitors at high frequencies. Note the use of the special symbol (a triangle with the letter 'L' inside it) to denote the load ground.

Standard Multiplier Connections

Figure 5 shows the basic connections for multiplication. The X and Y inputs are shown as optionally having their negative nodes grounded, but they are fully differential, and in many applications the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity, while achieving some desired output polarity) or both may be driven.

The AD734 has an input resistance of 50 kΩ ± 20% at the X, Y, and Z interfaces, which allows ac-coupling to be achieved

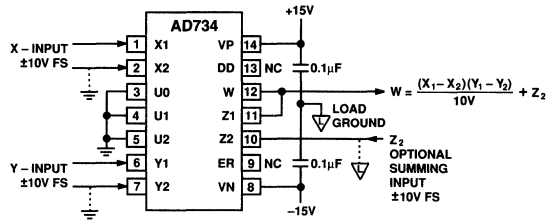


Figure 5. Basic Multiplier Circuit

with moderately good control of the high-pass (HP) corner frequency; a capacitor of 0.1 μF provides a HP corner frequency of 32 Hz. When a tighter control of this frequency is needed, or when the HP corner is above about 100 kHz, an external resistor should be added across the pair of input nodes.

At least one of the two inputs of any pair must be provided with a dc path (usually to ground). The careful selection of ground returns is important in realizing the full accuracy of the AD734. The Z2 pin will normally be connected to the load ground, which may be remote, in some cases. It may also be used as an optional summing input (see Equations (3) and (4), above) having a nominal FS input of ±10 V and the full 10 MHz bandwidth.

In applications where high absolute accuracy is essential, the scaling error caused by the finite resistance of the signal source(s) may be troublesome; for example, a 50 Ω source resistance at just one input will introduce a gain error of −0.1%; if both the X- and Y-inputs are driven from 50 Ω sources, the scaling error in the product will be −0.2%. Provided the source resistance(s) are known, this gain error can be completely compensated by including the appropriate resistance (50 Ω or 100 Ω, respectively, in the above cases) between the output W (Pin 12) and the Z1 feedback input (Pin 11). If Rx is the total source resistance associated with the X1 and X2 inputs, and Ry is the total source resistance associated with the Y1 and Y2 inputs, and neither Rx nor Ry exceeds 1 kΩ, a resistance of Rx+Ry in series with pin Z1 will provide the required gain restoration.

Pins 9 (ER) and 13 (DD) should be left unconnected in this application. The U-inputs (Pins 3, 4 and 5) are shown connected to ground; they may alternatively be connected to VN, if desired. In applications where Pin 2 (X2) happens to be driven with a high-amplitude, high-frequency signal, the capacitive coupling to the denominator control circuitry via an ungrounded Pin 3 can cause high-frequency distortion. However, the AD734 can be operated without modification in an AD534 socket, and these three pins left unconnected, with the above caution noted.

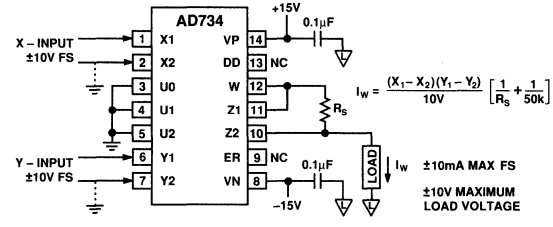


Figure 6. Conversion of Output to a Current

Current Output

It may occasionally be desirable to convert the output voltage to a current. In correlation applications, for example, multiplication is followed by integration; if the output is in the form of a current, a simple grounded capacitor can perform this function. Figure 6 shows how this can be achieved. The op-amp forces the voltage across Z1 and Z2, and thus across the resistor R_S, to be the product XY/U. Note that the input resistance of the Z interface is in shunt with R_S, which must be calculated accordingly.

The smallest FS current is simply ±10 V/50 kΩ, or ±200 μA, with a tolerance of about 20%. To guarantee a 1% conversion tolerance without adjustment, R_S must be less than 2.5 kΩ. The maximum full scale output current should be limited to about ±10 mA (thus, R_S = 1 kΩ). This concept can be applied to all connection modes, with the appropriate choice of terminals.

Squaring and Frequency-Doubling

Squaring of an input signal, E, is achieved simply by connecting the X and Y inputs in parallel; the phasing can be chosen to produce an output of E^2/U or $-E^2/U$ as desired. The input may have either polarity, but the basic output will either always be positive or negative; as for multiplication, the Z2 input may be used to add a further signal to the output.

When the input is a sinewave, a squarer behaves as a frequency-doubler, since

$$(Esin\omega t)^2 = E^2\,(1 - cos2\omega t)/2 \qquad (8)$$

Equation (8) shows a dc term at the output which will vary strongly with the amplitude of the input, E. This dc term can be avoided using the connection shown in Figure 7, where an RC-network is used to generate two signals whose product has no dc term. The output is

$$W = 4\left\{\frac{E}{\sqrt{2}}\,sin\left(\omega t + \frac{\pi}{4}\right)\right\}\left\{\frac{E}{\sqrt{2}}\,sin\left(\omega t - \frac{\pi}{4}\right)\right\}\left(\frac{1}{10\ V}\right) \qquad (9)$$

for ω = 1/CR1, which is just

$$W = E^2(cos2\omega t)/(10\ V) \qquad (10)$$

which has no dc component. To restore the output to ±10 V when E = 10 V, a feedback attenuator with an approximate ratio of 4 is used between W and Z1; this technique can be used wherever it is desired to achieve a higher overall gain in the transfer function.

In fact, the values of R3 and R4 include additional compensation for the effects of the 50 kΩ input resistance of all three interfaces; R2 is included for a similar reason. These resistor values should not be altered without careful calculation of the consequences; with the values shown, the center frequency f_0 is 100 kHz for C = 1 nF. The amplitude of the output is only a weak function of frequency: the output amplitude will be 0.5% too low at f = $0.9f_0$ and f = $1.1f_0$. The cross-connection is simply to produce the cosine output with the sign shown in Equation (10); however, the sign in this case will rarely be important.

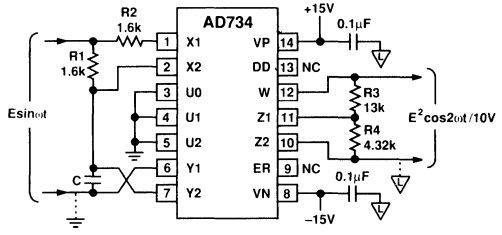


Figure 7. Frequency Doubler

OPERATION AS A DIVIDER

The AD734 supports two methods for performing analog division. The first is based on the use of a multiplier in a feedback loop. This is the standard mode recommended for multipliers having a fixed scaling voltage, such as the AD534, and will be described in this Section. The second uses the AD734's unique capability for externally varying the scaling (denominator) voltage directly, and will be described in the next section.

Feedback Divider Connections

Figure 8 shows the connections for the standard (AD534) divider mode. Feedback from the output, W, is now taken to the Y2 (inverting) input, which, provided that the X-input is positive, establishes a negative feedback path. Y1 should normally be connected to the ground associated with the load circuit, but may optionally be used to sum a further signal to the output. If desired, the polarity of the Y-input connections can be reversed, with W connected to Y1 and Y2 used as the optional summation input. In this case, either the polarity of the X-input connections must be reversed, or the X-input voltage must be negative.

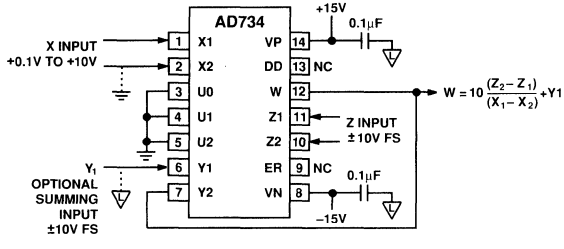


Figure 8. Standard (AD534) Divider Connection

The numerator input, which is differential and can have either polarity, is applied to pins Z1 and Z2. As with all dividers based on feedback, the bandwidth is directly proportional to the denominator, being 10 MHz for X = 10 V and reducing to 100 kHz for X = 100 mV. This reduction in bandwidth, and the increase in output noise (which is inversely proportional to the denominator voltage) preclude operation much below a denominator of 100 mV. Division using direct control of the denominator (Figure 10) does not have these shortcomings.

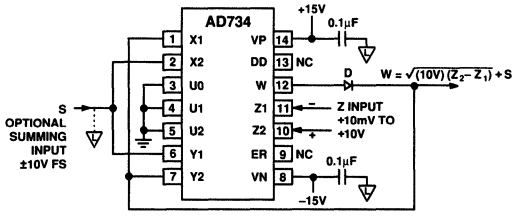


Figure 9. Connection for Square Rooting

Connections for Square-Rooting

The AD734 may be used to generate an output proportional to the square-root of an input using the connections shown in Figure 9. Feedback is now via both the X and Y inputs, and is always negative because of the reversed-polarity between these two inputs. The Z input must have the polarity shown, but because it is applied to a differential port, either polarity of input can be accepted with reversal of Z1 and Z2, if necessary. The diode D, which can be any small-signal type (1N4148 being suitable) is included to prevent a latching condition which could occur if the input momentarily was of the incorrect polarity of the input, the output will be always negative.

Note that the loading on the output side of the diode will be provided by the 25 kΩ of input resistance at X1 and Y2, and by the user's load. In high speed applications it may be beneficial to include further loading at the output (to 1 kΩ minimum) to speed up response time. As in previous applications, a further signal, shown here as S, may be summed to the output; if this option is not used, this node should be connected to the load ground.

DIVISION BY DIRECT DENOMINATOR CONTROL

The AD734 may be used as an analog divider by directly varying the denominator voltage. In addition to providing much higher accuracy and bandwidth, this mode also provides greater flexibility, because all inputs remain available. Figure 10 shows the connections for the general case of a three-input multiplier divider, providing the function

$$W = \frac{(X_1 - X_2)(Y_1 - Y_2)}{(U_1 - U_2)} + Z_2, \qquad (11)$$

where the X, Y, and Z signals may all be positive or negative, but the difference $U = U_1 - U_2$ must be positive and in the range +10 mV to +10 V. If a negative denominator voltage must be used, simply ground the noninverting input of the op amp. As previously noted, the X input must have a magnitude of less than 1.25U.

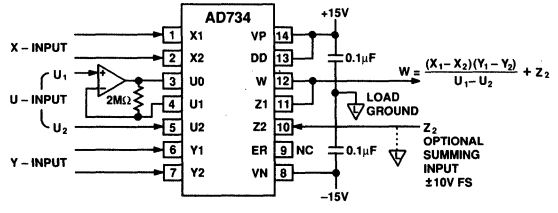


Figure 10. Three-Variable Multiplier/Divider Using Direct Denominator Control

This connection scheme may also be viewed as a variable-gain element, whose output, in response to a signal at the X input, is controllable by both the Y input (for attenuation, using Y less than U) and the U input (for amplification, using U less than Y). The ac performance is shown in Figure 11; for these results, Y was maintained at a constant 10 V. At U = 10 V, the gain is unity and the circuit bandwidth is a full 10 MHz. At U = 1 V, the gain is 20 dB and the bandwidth is essentially unaltered. At U = 100 mV, the gain is 40 dB and the bandwidth is 2 MHz. Finally, at U = 10 mV, the gain is 60 dB and the bandwidth is 250 kHz, corresponding to a 250 MHz gain-bandwidth product.

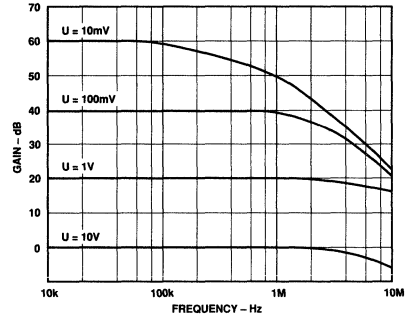


Figure 11. Three-Variable Multiplier/Divider Performance

The 2 MΩ resistor is included to improve the accuracy of the gain for small denominator voltages. At high gains, the X input offset voltage can cause a significant output offset voltage. To eliminate this problem, a low-pass feedback path can be used from W to X2; see Figure 13 for details.

Where a numerator of 10 V is needed, to implement a two-quadrant divider with fixed scaling, the connections shown in Figure 12 may be used. The reference voltage output appearing between Pin 9 (ER) and Pin 8 (VN) is amplified and buffered by the second op amp, to impose 10 V across the Y1/Y2 input. Note that Y2 is connected to the negative supply in this application. This is permissable because the common-mode voltage is still high enough to meet the internal requirements. The transfer function is

$$W = 10V\left(\frac{X_1 - X_2}{U_1 - U_2}\right) + Z_2. \qquad (12)$$

The ac performance of this circuit remains as shown in Figure 11.

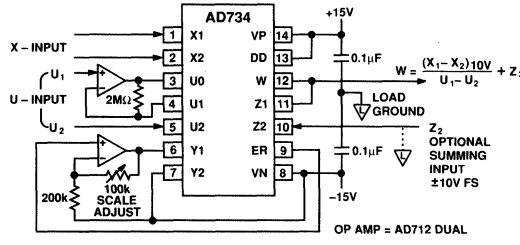


Figure 12. Two-Quadrant Divider with Fixed 10 V Scaling

A PRECISION AGC LOOP

The variable denominator of the AD734 and its high gain-bandwidth product make it an excellent choice for precise automatic gain control (AGC) applications. Figure 13 shows a suggested method. The input signal, E_{IN}, which may have a peak amplitude of from 10 mV to 10 V at any frequency from 100 Hz to 10 MHz, is applied to the X input, and a fixed positive voltage E_C to the Y input. Op amp A2 and capacitor C2 form an integrator having a current summing node at its inverting input. (The AD712 dual op amp is a suitable is a suitable choice for this application.) In the absence of an input, the current in D2 and R2 causes the integrator output to ramp negative, clamped by diode D3, which is included to reduce the time required for the loop to establish a stable, calibrated, output level once the circuit has received an input signal. With no input to the denominator (U0 and U2), the gain of the AD734 is very high (about 70 dB), and thus even a small input causes a substantial output.

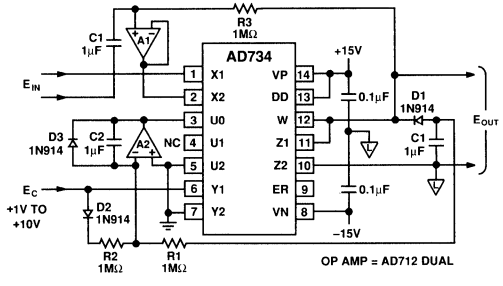


Figure 13. Precision AGC Loop

Diode D1 and C1 form a peak detector, which rectifies the output and causes the integrator to ramp positive. When the current in R1 balances the current in R2, the integrator output holds the denominator output at a constant value. This occurs when there is sufficient gain to raise the amplitude of E_{IN} to that required to establish an output amplitude of E_C over the range of +1 V to +10 V. The X input of the AD734, which has finite offset voltage, could be troublesome at the output at high gains. The output offset is reduced to that of the X input (one or two millivolts) by the offset loop comprising R3, C3, and buffer A1. The low pass corner frequency of 0.16 Hz is transformed to a high-pass corner that is multiplied by the gain (for example, 160 Hz at a gain of 1000).

In applications not requiring operation down to low frequencies, amplifier A1 can be eliminated, but the AD734's input resistance of 50 kΩ between X1 and X2 will reduce the time constant and increase the input offset. Using a non-polar 20 µF tantalum capacitor for C1 will result in the same unity-gain high-pass corner; in this case, the offset gain increases to 20, still very acceptable.

Figure 14 shows the error in the output for sinusoidal inputs at 100 Hz, 100 kHz, and 1 MHz, with E_C set to +10 V. The output error for any frequency between 300 Hz and 300 kHz is similar to that for 100 kHz. At low signal frequencies and low input amplitudes, the dynamics of the control loop determine the gain error and distortion; at high frequencies, the 200 MHz gain-bandwidth product of the AD734 limit the available gain.

The output amplitude tracks E_C over the range +1 V to slightly more than +10 V.

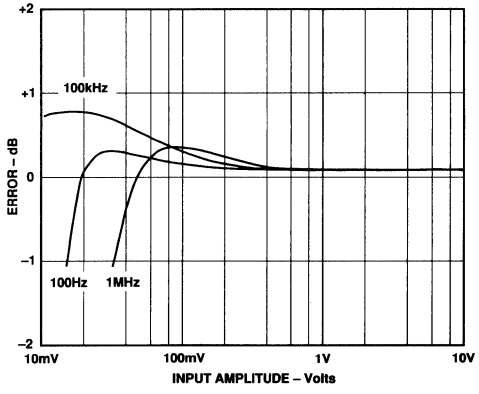


Figure 14. AGC Amplifier Output Error vs. Input Voltage

WIDEBAND RMS-DC CONVERTER USING U INTERFACE

The AD734 is well suited to such applications as implicit RMS-DC conversion, where the AD734 implements the function

$$V_{RMS} = \frac{avg\,[V_{IN}{}^2]}{V_{RMS}} \qquad (13)$$

using its direct divide mode. Figure 15 shows the circuit.

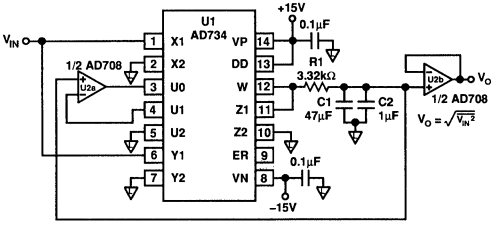


Figure 15. A 2-Chip, Wideband RMS-DC Converter

In this application, the AD734 and an AD708 dual op amp serve as a 2-chip RMS-DC converter with a 10 MHz bandwidth. Figure 16 shows the circuit's performance for square-, sine-, and triangle-wave inputs. The circuit accepts signals as high as 10 V p–p with a crest factor of 1 or 1 V p–p with a crest factor of 10. The circuit's response is flat to 10 MHz with an input of 10 V, flat to almost 5 MHz for an input of 1 V, and to almost 1 MHz for inputs of 100 mV. For accurate measurements of input levels below 100 mV, the AD734's output offset (Z interface) voltage, which contributes a dc error, must be trimmed out.

In Figure 15's circuit, the AD734 squares the input signal, and its output ($V_{IN}{}^2$) is averaged by a low-pass filter that consists of R1 and C1 and has a corner frequency of 1 Hz. Because of the implicit feedback loop, this value is both the output value, V_{RMS}, and the denominator in Equation (13). U2a and U2b, an AD708 dual dc precision op amp, serve as unity-gain buffers, supplying both the output voltage and driving the U interface.

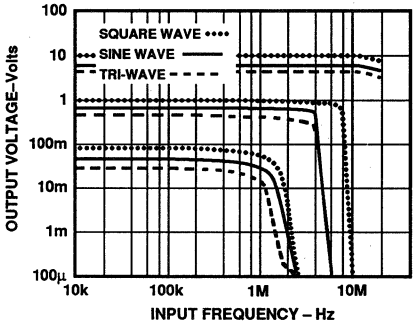


Figure 16. RMS-DC Converter Performance

LOW DISTORTION MIXER

The AD734's low noise and distortion make it especially suitable for use as a mixer, modulator, or demodulator. Although the AD734's −3 dB bandwidth is typically 10 MHz and is established by the output amplifier, the bandwidth of its X and Y interfaces and the multiplier core are typically in excess of 40 MHz. Thus, provided that the desired output signal is less than 10 MHz, as would typically be the case in demodulation, the AD734 can be used with both its X and Y input signals as high as 40 MHz. One test of mixer performance is to linearly combine two closely spaced, equal-amplitude sinusoidal signals and then mix them with a third signal to determine the mixer's 2-tone Third-Order Intermodulation Products.

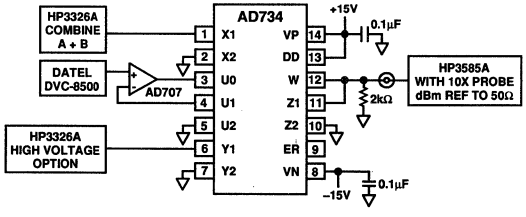


Figure 17. AD734 Mixer Test Circuit

Figure 17 shows a test circuit for measuring the AD734's performance in this regard. In this test, two signals, at 10.05 MHz and 9.95 MHz are summed and applied to the AD734's X interface. A second 9 MHz signal is applied to the AD734's Y interface. The voltage at the U interface is set to 2 V to use the full dynamic range of the AD734. That is, by connecting the W and Z1 pins together, grounding the Y2 and X2 pins, and setting U = 2 V, the overall transfer function is

$$W = \frac{X_1 Y_1}{2\,V} \qquad (14)$$

and W can be as high as 20 V p–p when X1 = 2 V p–p and Y1 = 10 V p–p. The 2 V p–p signal level corresponds to +10 dBm into a 50 Ω input termination resistor connected from X1 or Y1 to ground.

If the two X1 inputs are at frequencies f_1 and f_2 and the frequency at the Y1 input is f_0, then the two-tone third-order intermodulation products should appear at frequencies $2f_1 - f_2 \pm f_0$ and $2f_2 - f_1 \pm f_0$. Figures 18 and 19 show the output spectra of the AD734 with f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz for a signal level of f_1 & f_2 of 6 dBm and f_0 of +24 dBm in Figure 18 and f_1 & f_2 of 0 dBm and f_0 of +24 dBm in Figure 19. This performance is *without* external trimming of the AD734's X and Y input-offset voltages.

The possible Two Tone Intermodulation Products are at 2 × 9.95 MHz − 10.05 MHz ± 9.00 MHz and 2 × 10.05 − 9.95 MHz ±9.00 MHz; of these only the third-order products at 0.850 MHz and 1.150 MHz are within the 10 MHz bandwidth of the AD734; the desired output signals are at 0.950 MHz and 1.050 MHz. Note that the difference (Figure 18) between the desired outputs and third-order products is approximately 78 dB, which corresponds to a computed third-order intercept point of +46 dBm.

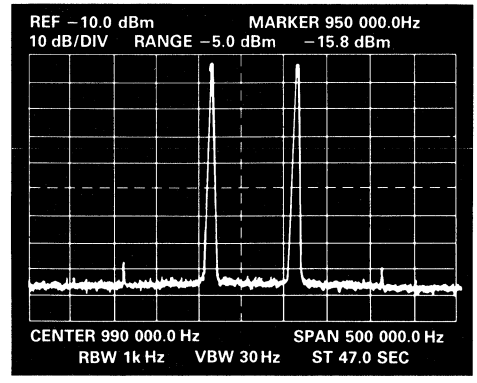


Figure 18. AD734 Third-Order Intermodulation Performance for f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz and for Signal Levels of f_1 & f_2 of 6 dBm and f_0 of +24 dBm. All Displayed Signal Levels Are Attenuated 20 dB by the 10X Probe Used to Measure the Mixer's Output

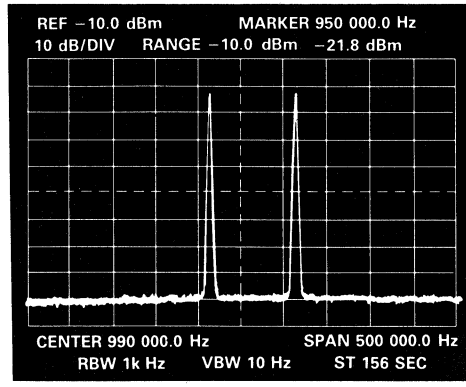


Figure 19. AD734 Third-Order Intermodulation Performance for f_1 = 9.95 MHz, f_2 = 10.05 MHz, and f_0 = 9.00 MHz and for Signal Levels of f_1 & f_2 of 0 dBm and f_0 of +24 dBm. All Displayed Signal Levels Are Attenuated 20 dB by the 10X Probe Used to Measure the Mixer's Output

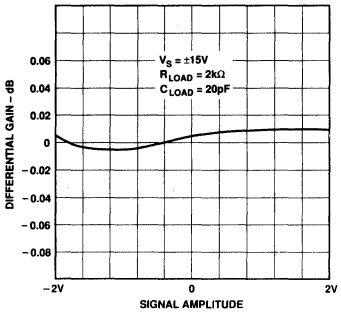


Figure 20. Differential Gain at 3.58 MHz and R_L = 2 kΩ

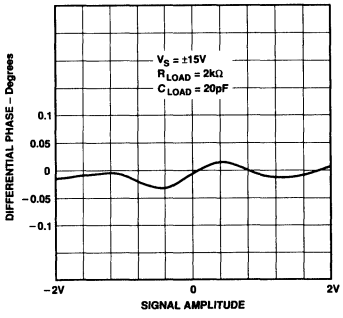


Figure 21. Differential Phase at 3.58 MHz and R_L = 2 kΩ

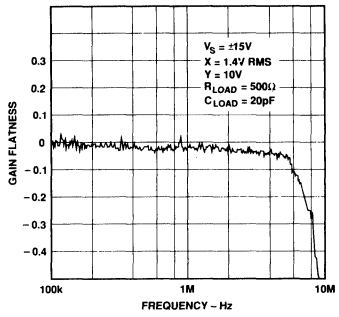


Figure 22. Gain Flatness, 300 kHz to 10 MHz, R_L = 500 Ω

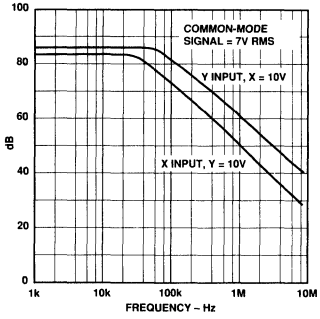


Figure 23. CMRR vs. Frequency

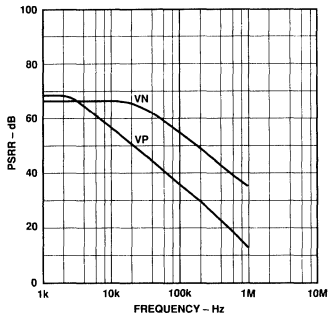


Figure 24. PSRR vs. Frequency

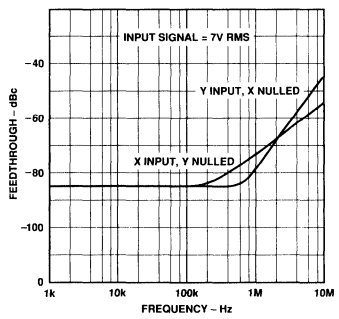


Figure 25. Feedthrough vs. Frequency

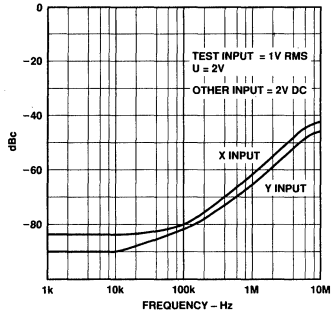


Figure 26. THD vs. Frequency, U = 2 V

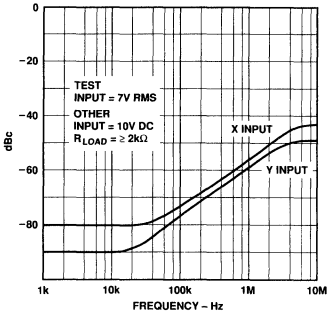


Figure 27. THD vs. Frequency, U = 10 V

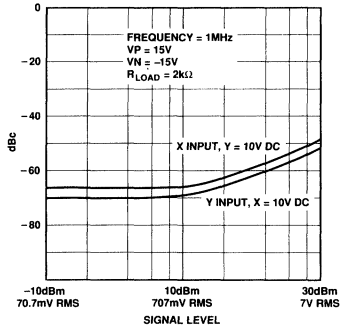


Figure 28. THD vs. Signal Level, f = 1 MHz

AD734—Typical Characteristics

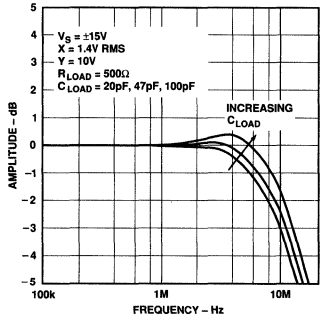


Figure 29. Gain vs. Frequency vs. C_{LOAD}

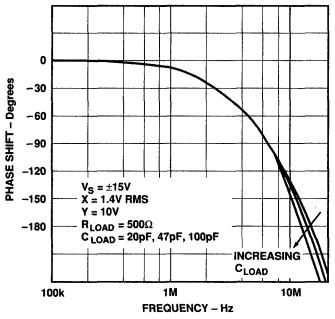


Figure 30. Phase vs. Frequency vs. C_{LOAD}

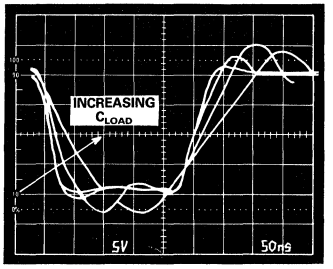


Figure 31. Pulse Response vs. C_{LOAD}, C_{LOAD} = 0 pF, 47 pF, 100 pF, 200 pF

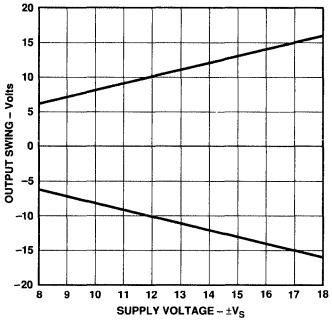


Figure 32. Output Swing vs. Supply Voltage

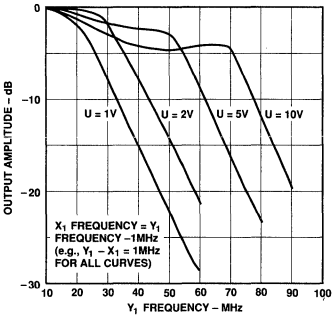


Figure 33. Output Amplitude vs. Input Frequency, When Used as Demodulator

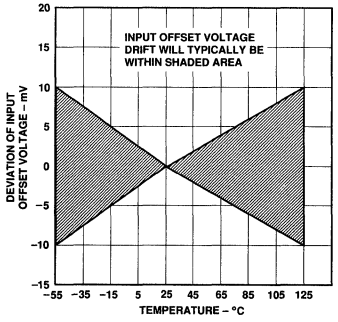


Figure 34. V_{OS} Drift, X Input

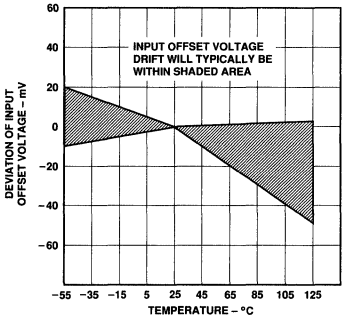


Figure 35. V_{OS} Drift, Z Input

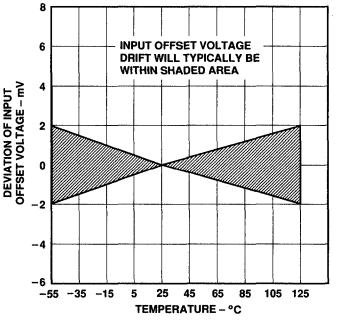


Figure 36. V_{OS} Drift, Y Input

ANALOG DEVICES

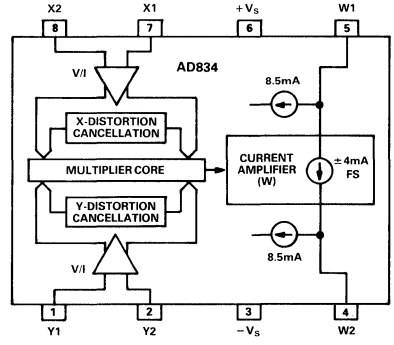
500MHz Four-Quadrant Multiplier

AD834

FEATURES
DC to >500MHz Operation
Differential ±1V Full Scale Inputs
Differential ±4mA Full Scale Output Current
Low Distortion (≤0.05% for 0dBm Input)
Supply Voltages from ±4V to ±9V
Low Power (280mW typical at V_S=±5V)

APPLICATIONS
High Speed Real Time Computation
Wideband Modulation and Gain Control
Signal Correlation and RF Power Measurement
Voltage Controlled Filters and Oscillators
Linear Keyers for High Resolution Television
Wideband True RMS

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD834 is a monolithic laser-trimmed four-quadrant analog multiplier intended for use in high frequency applications, having a transconductance bandwidth (R_L=50Ω) in excess of 500MHz from either of the differential voltage inputs. In multiplier modes, the typical total full scale error is 0.5%, dependent on the application mode and the external circuitry. Performance is relatively insensitive to temperature and supply variations, due to the use of stable biasing based on a bandgap reference generator and other design features.

To preserve the full bandwidth potential of the high speed bipolar process used to fabricate the AD834, the outputs appear as a differential pair of currents at open collectors. To provide a single ended ground referenced voltage output, some form of external current to voltage conversion is needed. This may take the form of a wideband transformer, balun, or active circuitry such as an op amp. In some applications (such as power measurement) the subsequent signal processing may not need to have high bandwidth.

The transfer function is accurately trimmed such that when X=Y=±1V, the differential output is ±4mA. This absolute calibration allows the outputs of two or more AD834s to be summed with precisely equal weighting, independent of the accuracy of the load circuit.

The AD834J is specified for use over the commercial temperature range of 0 to +70°C and is available in an 8-pin plastic DIP package and an 8-pin plastic SOIC package. AD834A is available in cerdip for operation over the industrial temperature range of −40°C to +85°C. The AD834S/883B is specified for operation over the military temperature range of −55°C to +125°C and is available in the 8-pin cerdip package. S-Grade chips are also available.

Two application notes featuring the AD834 (AN-212 and AN-216) can now be obtained by calling 1-800-ANALOG-D. For additional applications circuits, consult the AD811 data sheet.

PRODUCT HIGHLIGHTS

1. The AD834 combines high static accuracy (low input and output offsets and accurate scale factor) with very high bandwidth. As a four-quadrant multiplier or squarer, the response extends from dc to an upper frequency limited mainly by packaging and external board layout considerations. A large signal bandwidth of over 500MHz is attainable under optimum conditions.
2. The AD834 can be used in many high speed nonlinear operations, such as square rooting, analog division, vector addition and rms-to-dc conversion. In these modes, the bandwidth is limited by the external active components.
3. Special design techniques result in low distortion levels (better than −60dB on either input) at high frequencies and low signal feedthrough (typically −65dB up to 20MHz).
4. The AD834 exhibits low differential phase error over the input range—typically 0.08° at 5MHz and 0.8° at 50MHz. The large signal transient response is free from overshoot, and has an intrinsic rise time of 500ps, typically settling to within 1% in under 5ns.
5. The nonloading, high impedance, differential inputs simplify the application of the AD834.

AD834—SPECIFICATIONS (T_A = +25°C and $\pm V_S$ = ±5V, unless otherwise noted; dBm assumes 50Ω load.)

Model	Conditions	AD834J Min	AD834J Typ	AD834J Max	AD834A, S Min	AD834A, S Typ	AD834A, S Max	Units
MULTIPLIER PERFORMANCE								
Transfer Function			$W = \frac{XY}{(1V)^2} \times 4mA$			$W = \frac{XY}{(1V)^2} \times 4mA$		
Total Error[1] (Figure 6)	−1V≤X,Y<+1V		±0.5	**±2**		±0.5	**±2**	% FS
vs. Temperature	T_{min} to T_{max}					±1.5	**±3**	% FS
vs. Supplies[2]	±4V to ±6V		0.1	**0.3**		0.1	**0.3**	% FS/V
Linearity[3]			±0.5	**±1**		±0.5	**±1**	% FS
Bandwidth[4]	See Figure 5	500			500			MHz
Feedthrough, X	X=±1V, Y=Nulled		0.2	**0.3**		0.2	**0.3**	% FS
Feedthrough, Y	X=Nulled, Y=±1V		0.1	**0.2**		0.1	**0.2**	% FS
AC Feedthrough, X[5]	X=0dBm, Y=Nulled							
	f=10MHz		−65			−65		dB
	f=100MHz		−50			−50		dB
AC Feedthrough, Y[5]	X=Nulled, Y=0dBm							
	f=10MHz		−70			−70		dB
	f=100MHz		−50			−50		dB
INPUTS (X1, X2, Y1, Y2)								
Full Scale Range	Differential		±1			±1		V
Clipping Level	Differential	**±1.1**	±1.3		**±1.1**	±1.3		V
Input Resistance	Differential		25			25		kΩ
Offset Voltage			0.5	**3**		0.5	**3**	mV
vs. Temperature	T_{min} to T_{max}		10			10		µV/°C
				4			**4**	mV
vs. Supplies[2]	±4V to ±6V		100	**300**		100	**300**	µV/V
Bias Current			45			45		µA
Common Mode Rejection	f≤100kHz; 1V p-p		70			70		dB
Nonlinearity, X	Y=1V; X=±1V		0.2	**0.5**		0.2	**0.5**	% FS
Nonlinearity, Y	X=1V; Y=±1V		0.1	**0.3**		0.1	**0.3**	% FS
Distortion, X	X=0dBm, Y=1V							
	f=10MHz		−60			−60		dB
	f=100MHz		−44			−44		dB
Distortion, Y	X=1V, Y=0dBM							
	f=10MHz		−65			−65		dB
	f=100MHz		−50			−50		dB
OUTPUTS (W1, W2)								
Zero Signal Current	Each Output		8.5			8.5		mA
Differential Offset	X=0, Y=0		±20	**±60**		±20	**±60**	µA
vs. Temperature	T_{min} to T_{max}		40			40		nA/°C
							±60	µA
Scaling Current	Differential	3.96	4	4.04	3.96	4	4.04	mA
Output Compliance		4.75		9	4.75		9	V
Noise Spectral Density	f=10Hz to 1MHz Outputs into 50Ω Load		16			16		nV/$\sqrt{Hz}$
POWER SUPPLIES								
Operating Range		±4		±9	±4		±9	V
Quiescent Current[6]	T_{min} to T_{max}							
$+V_S$			11	**14**		11	**14**	mA
$-V_S$			28	**35**		28	**35**	mA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD834J, JR-REEL					
Military (−55°C to +125°C)						AD834S		
Industrial (−40°C to +85°C)						AD834A		
PACKAGE OPTIONS[7]								
8-Pin SOIC (R)			AD834JR					
8-Pin Cerdip (Q)						AD834AQ		
8-Pin Plastic DIP (N)			AD834JN			AD834SQ/883B		

NOTES

[1]Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full scale output.

[2]Both supplies taken simultaneously; sinusoidal input at f≤10kHz.

[3]Linearity is defined as residual error after compensating for input offset voltage, output offset current and scaling current errors.

[4]Bandwidth is guaranteed when configured in squarer mode. See Figure 5.

[5]Sine input; relative to full scale output; zero input port nulled; represents feedthrough of the fundamental.

[6]Negative supply current is equal to the sum of positive supply current, the signal currents into each output, W1 and W2, and the input bias currents.

[7]For outline information see Package Information section.

Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$ to $-V_S$) 18V
Internal Power Dissipation 500mW
Input Voltages (X1, X2, Y1, Y2) . . . . . $+V_S$
Operating Temperature Range
AD834J . . . . . 0 to +70°C
AD834A . . . . . −40°C to +85°C
AD834S/883B . . . . . −55°C to +125°C
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (R, N) . . . . . −65°C to +125°C
Lead Temperature, Soldering 60sec . . . . . +300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISCS

	θ_{JC}	θ_{JA}
8-Pin Cerdip Package (Q)	30°C/W	110°C/W
8-Pin Plastic SOIC (R)	45°C/W	165°C/W
8-Pin Plastic Mini-DIP (N)	50°C/W	99°C/W

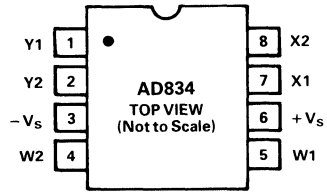
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD834JN	0 to +70°C	N-8
AD834JR	0 to +70°C	R-8
AD834JR-REEL	0 to +70°C	R-8
AD834AQ	−40°C to +85°C	Q-8
AD834SQ/883B	−55°C to +125°C	Q-8
AD834S Chips		Chips

*N = Plastic DIP; Q = Cerdip; R = Small Outline IC (SOIC) Package. For outline information see Package Information section.

CONNECTION DIAGRAM

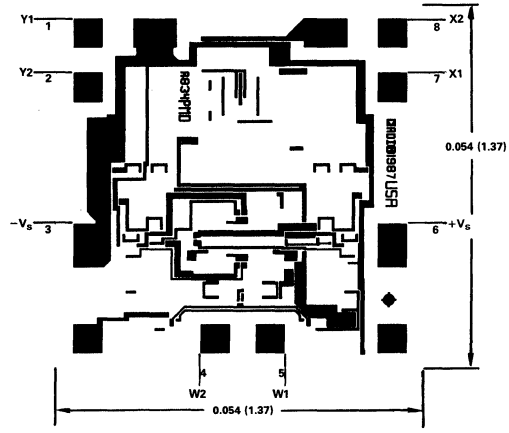
Small Outline (R) Package
Plastic DIP (N) Package
Cerdip (Q) Package



METALIZATION PHOTOGRAPH

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



AD834—Typical Characteristics

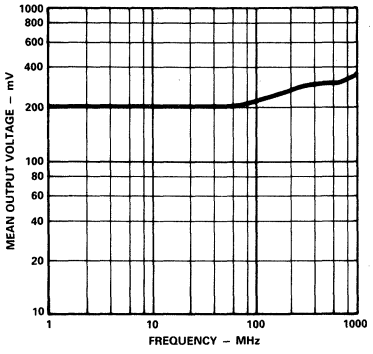


Figure 1. Mean-Square Output vs. Frequency

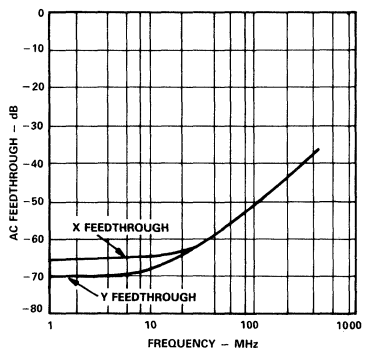


Figure 2. AC Feedthrough vs. Frequency

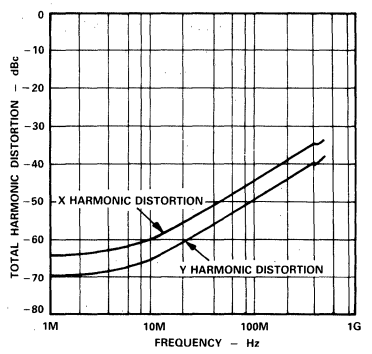


Figure 3. Total Harmonic Distortion vs. Frequency

Figure 1. Figure 1 is a plot of the mean-square output versus frequency for the test circuit of Figure 5. Note that the rising response is due to package resonances.

Figure 2. For frequencies below 1MHz, ac feedthrough is dominated by static nonlinearities in the transfer function and the finite offset voltages. The offset voltages cause a small fraction of the fundamental to appear at the output, and can be nulled out.

Figure 3. THD data represented in Figure 3 is dominated by the second harmonic, and is generated with 0dBm input on the ac input and +1V on the dc input. For a given amplitude on the ac input, THD is relatively insensitive to changes in the dc input amplitude. Varying the ac input amplitude while maintaining a constant dc input amplitude will affect THD performance.

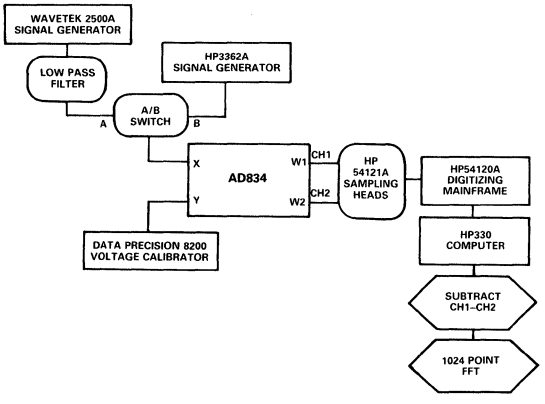


Figure 4. Test Configuration for Measuring ac Feedthrough and Total Harmonic Distortion

Figure 5. The squarer configuration shown in Figure 5 is used to determine wideband performance because it eliminates the need for (and the response uncertainties of) a wideband measurement device at the output. The wideband output of a squarer configuration is a fluctuating current at twice the input frequency with a mean value proportional to the square of the input amplitude.

By placing capacitors C3/C5 and C4/C6 across load resistors R1 and R2, a simple low-pass filter is formed, and the mean-square value is extracted. The mean-square response can be measured using a DVM connected across R1 and R2.

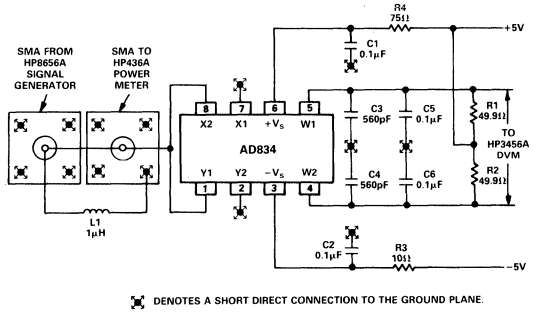


Figure 5. Bandwidth Test Circuit

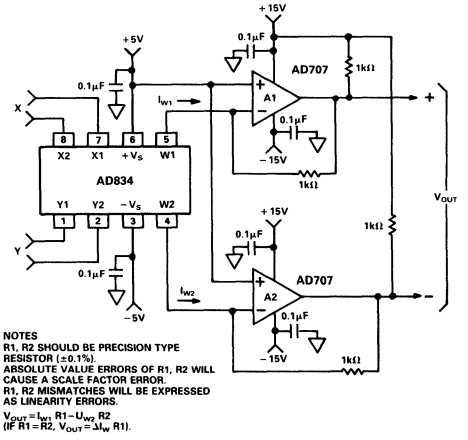


Figure 6. Low Frequency Test Circuit

BASIC OPERATION

Figure 7 is a functional equivalent of the AD834. There are three differential signal interfaces: the voltage inputs X= X1−X2 and Y=Y1−Y2, and the current output, W (see Fig. 7) which flows in the direction shown when X and Y are positive. The outputs W1 and W2 each have a standing current of typically 8.5mA.

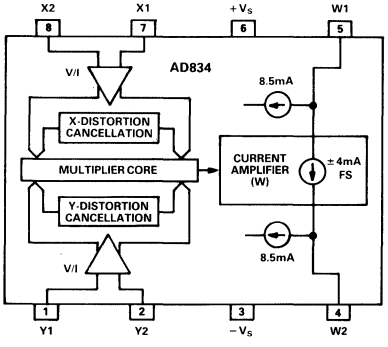


Figure 7. AD834 Functional Block Diagram

The input voltages are first converted to differential currents which drive the translinear core. The equivalent resistance of the voltage-to-current (V-I) converters is about 285Ω. This low value results in low input related noise and drift. However, the low full scale input voltage results in relatively high nonlinearity in the V-I converters. This is significantly reduced by the use of distortion cancellation circuits which operate by Kelvin sensing the voltages generated in the core — an important feature of the AD834.

The current mode output of the core is amplified by a special cascode stage which provides a current gain of nominally ×1.6, trimmed during manufacture to set up the full scale output current of ±4mA. **This output appears at a pair of open collectors which must be supplied with a voltage slightly above the voltage on Pin 6.** As shown in Figure 8, this can be arranged by inserting a resistor in series with the supply to this pin and taking the load resistors to the full supply. With R3=60Ω, the voltage drop across it is about 600mV. Using two 50Ω load resistors, the full scale differential output voltage is ±400mV.

The full bandwidth potential of the AD834 can only be realized when very careful attention is paid to grounding and decoupling. The device must be mounted close to a high quality ground plane and all lead lengths must be extremely short, in keeping with UHF circuit layout practice. In fact, the AD834 shows useful response to well beyond 1GHz, and the actual upper frequency in a typical application will usually be determined by the care with which the layout is effected. Note that R4 (in series with the $-V_S$ supply) carries about 30mA, and thus introduces a voltage drop of about 150mV. It is made large enough to reduce the Q of the resonant circuit formed by the supply lead and the decoupling capacitor. Slightly larger values can be used, particularly when using higher supply voltages. Alternatively, lossy RF chokes or ferrite beads on the supply leads may be used.

Figure 8 shows the use of optional termination resistors at the inputs. Note that although the resistive component of the input

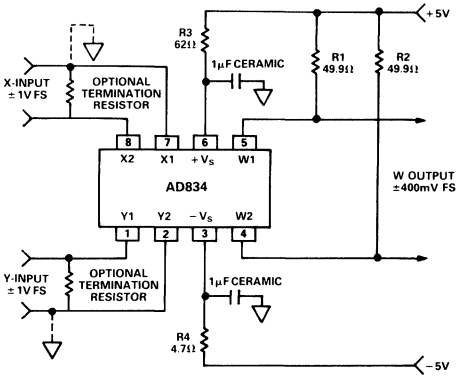


Figure 8. Basic Connections for Wideband Operation

impedance is quite high (about 25kΩ), the input bias current of typically 45μA can generate significant offset voltages if not compensated. For example, with a source and termination resistance of 50Ω (net source of 25Ω) the offset would be 25Ω×45μA=1.125mV. This can be almost fully cancelled by including (in this example) another 25Ω resistor in series with the "unused" input (in Figure 8, either X1 or Y2). In order to minimize crosstalk the input pins closest to the output (X1 and Y2) should be grounded; the effect is merely to reverse the phase of the X input and thus alter the polarity of the output.

TRANSFER FUNCTION

The output current W is the linear product of input voltages X and Y divided by $(1V)^2$ and multiplied by the "scaling current" of 4mA:

$$W = \frac{XY}{(1V)^2} \ 4mA$$

Provided that it is understood that the inputs are specified in *volts*, a simplified expression can be used:

$$W = (XY)\ 4mA$$

Alternatively, the full transfer function can be written:

$$W = \frac{XY}{1V} \cdot \frac{1}{250\Omega}$$

When both inputs are driven to their clipping level of about 1.3V, the peak output current is roughly doubled, to ±8mA, but distortion levels will then be very high.

TRANSFORMER COUPLING

In many high frequency applications where baseband operation is not required at either inputs or output, transformer coupling can be used. Figure 9 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design will depend entirely on the application. Transformers may also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals.

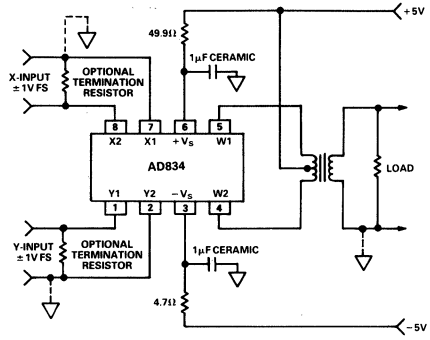


Figure 9. Transformer–Coupled Output

A particularly effective type of transformer is the balun[1] which is a short length of transmission line wound on to a toroidal ferrite core. Figure 10 shows this arrangement used to convert the bal(anced) output to an un(balanced) one (hence the use of the term). Although the symbol used is identical to that for a transformer, the mode of operation is quite different. In the first place, the load should now be equal to the characteristic impedance of the line (although this will usually not be critical for short line lengths). The collector load resistors R_C may also be chosen to reverse terminate the line, but again this will only be necessary when an electrically long line is used. In most cases, R_C will be made as large as the dc conditions allow, to minimize power loss to the load. The line may be a miniature coaxial cable or a twisted pair.

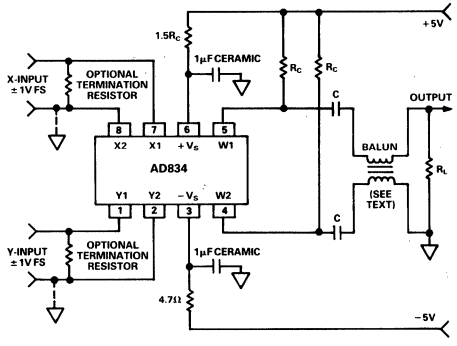


Figure 10. Using a Balun at the Output

It is important to note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; hence, it will usually exceed that of the multiplier. This is unlike a conventional transformer where the signal is conveyed as a flux in a magnetic core and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the *series* inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors C are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

[1]For a good treatment of baluns, see "Transmission Line Transformers" by Jerry Sevick; American Radio Relay League publication.

WIDEBAND MULTIPLIER CONNECTIONS

Where operation down to dc and a ground based output are necessary, the configuration shown in Figure 11 can be used. The element values were chosen in this example to result in a full-scale output of ±1V at the load, so the overall multiplier transfer function is

$$W = (X1-X2)(Y1-Y2)$$

where it is understood that the *inputs and output are in volts*. The polarity of the output can be reversed simply by reversing either the X or Y input.

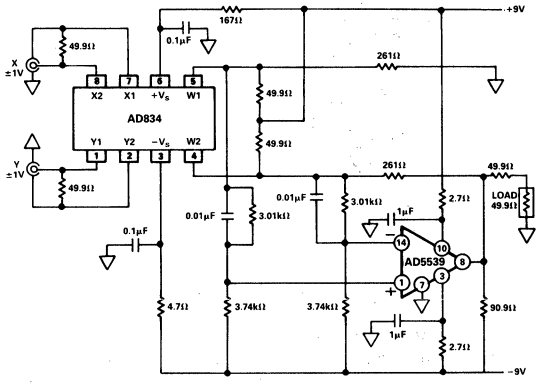


Figure 11. Wideband dc-Coupled Multiplier

The op amp should be chosen to support the desired output bandwidth. The AD5539 is shown here, providing an overall system bandwidth of 100MHz. Many other choices are possible where lower post multiplication bandwidths are acceptable. The level shifting network places the input nodes of the op amp to within a few hundred millivolts of ground using the recommended balanced supplies. The output offset may be nulled by including a 100Ω trim pot between each of the lower pair of resistors (3.74kΩ) and the negative supply.

The pulse response for this circuit shown in Figure 12; the X input was a pulse of 0 to +1V and the Y input was +1V dc. The transition times at the output are about 4ns.

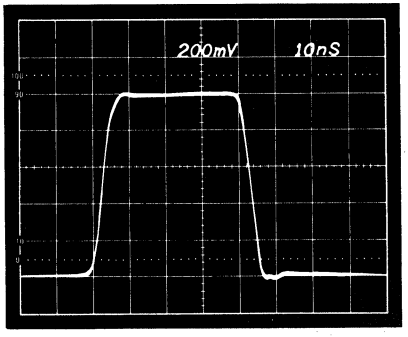


Figure 12. Pulse Response for the Circuit of Figure 11

POWER MEASUREMENT (MEAN SQUARE AND RMS)

The AD834 is well suited to measurement of average power in high frequency applications, connected either as a multiplier for the determination of the V×I product, or as a squarer for use with a single input. In these applications, the multiplier is followed by a low pass filter to extract the long term average value. Where the bandwidth extends to several hundred megahertz, the first pole of this filter should be formed by grounded capacitors placed directly at the output pins W1 and W2. This pole can be at a few kilohertz. The effective multiplication or squaring bandwidth is then limited solely by the AD834, since the following active circuitry is required to process only low frequency signals.

(Refer to Figure 5 test configuration.) Using the device as a squarer the wideband output in response to a sinusoidal stimulus is a raised cosine:

$$\sin^2\omega t = (1 + \cos 2\omega t)/2$$

Recall here that the full scale output current (when full scale input voltages of 1V are applied to both X and Y) is 4mA. In a 50Ω system, a sinusoid power of +10dBm has a peak value of 1V. Thus, at this drive level the peak output voltage across the differential 50Ω load in the absence of the filter capacitors would be 400mV (that is, 4mA ×50Ω×2), whereas the average value of the raised cosine is only 200mV. The averaging configuration is useful in evaluating the bandwidth of the AD834, since a dc voltage is easier to measure than a wideband, differential output. In fact, the squaring mode is an even more critical test than the direct measurement of the bandwidth of either channel taken independently (with a dc input on the nonsignal channel), because the phase relationship between the two channels also affects the average output. For example, a time delay difference of only 250ps between the X and Y channels would result in zero output when the input frequency is 1GHz, at which frequency the phase angle is 90 degrees and the intrinsic product is now between a sine and cosine function, which has zero average value.

The physical construction of the circuitry around the IC is critical to realizing the bandwidth potential of the device. The input is supplied from an HP8656A signal generator (100kHz to 990MHz) via an SMA connector and terminated by an HP436A power meter using an HP8482A sensor head connected via a second SMA connector. Since neither the generator nor the sensor provide a dc path to ground, a lossy 1μH inductor L1, formed by a 22-gauge wire passing through a ferrite bead (Fair-Rite type 2743001112) is included. This provides adequate impedance down to about 30MHz. The IC socket is mounted on a ground plane,with a clear area in the rectangle formed by the pins. This is important, since significant transformer action can arise if the pins pass through individual holes in the board; this has been seen to cause an oscillation at 1.3GHz in improperly constructed test jigs. The filter capacitors must be connected directly to the same point on the ground plane via the shortest possible leads. Parallel combinations of large and small capacitors are used to minimize the impedance over the full frequency range. (Refer to Figure 1 for mean-square response for the AD834 in cerdip package, using the configuration of Figure 5.)

To provide a square-root response and thus generate the rms value at the output, a second AD834, also connected as a squarer, can be used, as shown in Figure 13. Note that an attenuator is inserted both in the signal input and in the feedback path to the second AD834. This increases the maximum input capability to +15dBm and improves the response flatness by damping some of the resonances. The overall gain is unity; that is, the output voltage is exactly equal to the rms value of the input signal. The offset potentiometer at the AD834 outputs extends the dynamic range, and is adjusted for a dc output of 125.7mV when a 1MHz sinusoidal input at −5dBm is applied.

Additional filtering is provided; the time constants were chosen to allow operation down to frequencies as low as 1kHz and to provide a critically damped envelope response, which settles typically within 10ms for a full scale input (and proportionally slower for smaller inputs). The 5μF and 0.1μF capacitors may be scaled down to reduce response time if accurate rms operation at low frequencies is not required. The output op amp must be specified to accept a common-mode input near its supply. Note that the output polarity may be inverted by replacing the NPN transistor with a PNP type.

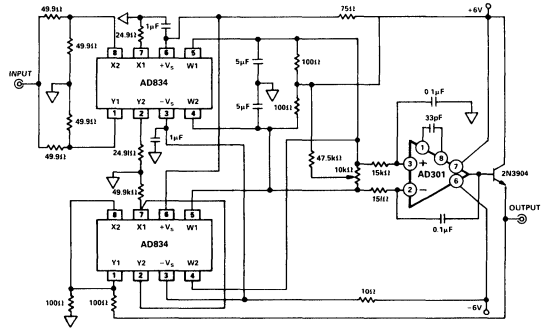


Figure 13. Connections for Wideband rms Measurement

FREQUENCY DOUBLER

Figure 14 shows another squaring application. In this case, the output filter has been removed and the wideband differential output is converted to a single sided signal using a "balun," which consists of a length of 50Ω coax cable fed through a ferrite core (Fair-Rite type 2677006301). No attempt is made to reverse terminate the output. Higher load power could be achieved by replacing the 50Ω load resistors by ferrite bead inductors. The same precautions should be observed with regard to PC board layout as recommended above. The output spectrum shown in Figure 15 is for an input power of +10dBm at a frequency of 200MHz. The second harmonic component at 400MHz has an output power of −15dBm. Some feedthrough of the fundamental occurs: it is 15dBs below the main output. It is believed that improvements in the design of the balun would reduce this feedthrough. A spurious output at 600MHz is also present, but it is 30dBs below the main output. At an input frequency of 100MHz, the measured power level at 200MHz is −16dBm, while the fundamental feedthrough is reduced to 25dBs below the main output; at an output of 600MHz the power is −11dBm and the third harmonic at 900MHz is 32dBs below the main output.

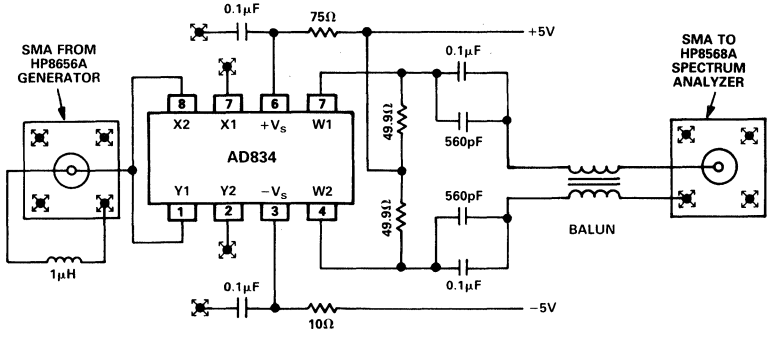


Figure 14. Frequency Doubler Connections

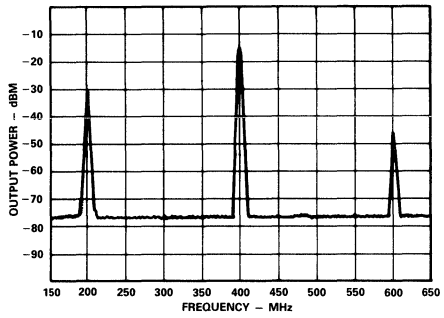


Figure 15. Output Spectrum for Configuration of Figure 14

WIDEBAND THREE SIGNAL MULTIPLIER/DIVIDER

Two AD834s and a wideband op amp can be connected to make a versatile multiplier/divider having the transfer function

$$W = \frac{(X1-X2)(Y1-Y2)}{(U1-U2)} + Z$$

with a denominator range of about 100:1. The denominator input U = U1−U2 must be positive and in the range 100mV to 10V; X, Y and Z inputs may have either polarity. Figure 16 shows a general configuration which may be simplified to suit a particular application. This circuit accepts full scale input voltages of 10V, and delivers a full scale output voltage of 10V. The optional offset trim at the output of the AD834 improves the accuracy for small denominator values. It is adjusted by nulling the output voltage when the X and Y inputs are zero and U = +100mV.

The AD840 is internally compensated to be stable without the use of any additional HF compensation. As the input U is reduced, the bandwidth falls because the feedback around the op amp is proportional to the input U.

This circuit may be modified in several ways. For example, if the differential input feature is not needed, the unused input

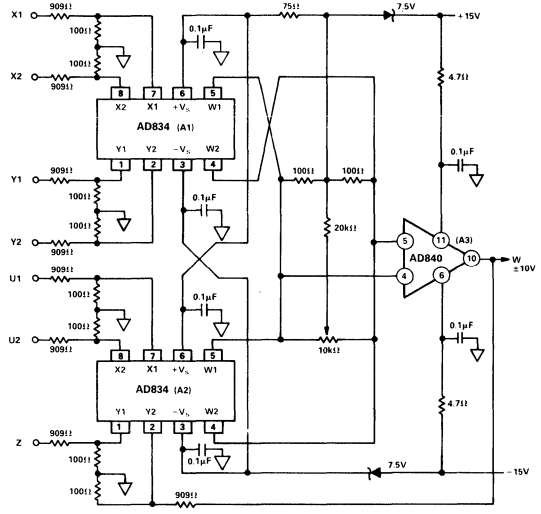


Figure 16. Wideband Three Signal Multiplier/Divider

can be connected to ground through a single resistor, equal to the parallel sum of the resistors in the attenuator section. The full scale input levels on X, Y and U can be adapted to any full scale voltage down to ±1V by altering the attenuator ratios. Note, however, that precautions must be taken if the attenuator ratio from the output of A3 back to the second AD834 (A2) is lowered. First, the HF compensation limit of the AD840 may be exceeded if the negative feedback factor is too high. Second, if the attenuated output at the AD834 exceeds its clipping level of ±1.3V, feedback control will be lost and the output will suddenly jump to the supply rails. However, with these limitations understood, it will be possible to adapt the circuit to smaller full scale inputs and/or outputs, and for use with lower supply voltages.

Signal Compression Components
Contents

3

Selection Guide
Signal Compression Components

Model	Input Range	Log Conformity RTI	BW kHz	Package Options[1]	Temp Range[2]	Page[3]	Comments
755	1 nA–1 mA	0.5%	10	Module	I	3–47	Complete, Current and Voltage, 6 Decade, High Accuracy
757	1 nA–1 mA	0.5%	25	Module	I	D	Complete, Log/Antilog Ratio, 6 Decade, High Accuracy
759	20 nA–0.2 mA	1.0%	200	Module	I	3–47	Complete, Current and Voltage, 4 Decade, Lowest Cost
AD640	**0.75 mV–200 mV**	**±0.6 dB**	**120 MHz**	**1, 2, 4, 5**	**C, I, M**	**3–31**	**120 MHz, 45 dB, DC Demodulating Logarithmic Amplifier**
***AD600**	**±2 V**	**±0.5 dB**	**30 MHz**	**2, 6**	**C**	**3–7**	**Dual 0 to +40 dB Variable Gain Amplifier**
***AD602**	**±2 V**	**±0.5 dB**	**30 MHz**	**2, 6**	**C**	**3–7**	**Dual −10 dB to +30 dB Variable Gain Amplifier**
***AD606**	**−80 to +10 dBm (50 Ω)**	**±1 dB**	**50 MHz**	**2, 6**	**I**	**3–25**	**50 MHz, 80 dB Demodulating Logarithmic Amplifier with Limiter Output**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[3]D = data sheet available.
Boldface Type: Product recommended for new design.
*New product.

Orientation
Signal Compression Components

The devices described in this section span frequencies from dc to RF. Low frequency devices are the 755N and 755P modular logarithmic amplifiers, which provide an output voltage proportional to the logarithm or antilogarithm of the input voltage for signals from dc to well under 1MHz.

For higher levels of integration, the AD640, a monolithic demodulating log amp, has five 10dB stages, each with a 350MHz small-signal bandwidth. The AD640 uses a successive detection scheme that produces a circuit proportional to the logarithm of the input voltage. The AD640 features an overall dc to 120MHz bandwidth along with a built-in attenuator and on-chip temperature compensation, as well as calibrated slope and intercept. Two AD640s can be cascaded for dynamic ranges as large as 95dB, depending on bandwidth.

For still higher levels of integration, there is the AD606, a complete, 80dB monolithic logarithmic amplifier using a 9-stage "successive-detection" technique. It provides both logarithmic (usable to >50MHz) and limited (usable to 100MHz) outputs. The logarithmic output is a voltage from a three-pole post-demodulation low-pass filter. The limited output is a differential current from a pair of open-collector outputs. The AD606 operates from a single +5V supply, consumes 65mW, and has a CMOS-compatible power-down input that reduces its power consumption to less than 500μW within 5μs.

The AD600 and AD602 are dual *exponential amplifiers* using Analog Devices' patented X-AMP™ technology. They are dual amplifiers offering 40dB of variable gain per amplifier (cascadable) with bandwidths of 30MHz and ultralow input noise spectral densities of $1.4nV/\sqrt{Hz}$. The AD600 amplifier's gains vary from 0 to +40dB while the AD602 amplifiers' gains vary from −10dB to +30dB.

LOGS AND LOG RATIOS

In the *logarithmic* mode, the ideal output equation is

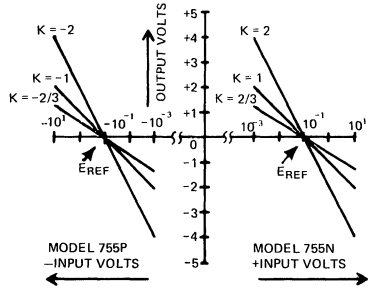
$$E_o = -K \log_{10} \left\{ \frac{I_{in}}{I_{ref}} \right\}$$

E_o can be positive or negative; it is zero when the ratio is unity, i.e., $I_{in} = I_{ref}$. K is the output scale constant; it is equal to the number of output volts corresponding to a decade* change of the ratio. In the 755 and 759 log amplifiers, K is pin programmable to be either 1V, 2V or 2/3V, or externally adjustable to any value ≥2/3V; in the model 757 log-ratio amplifier, K may be either a preset value of 1V or an arbitrary value adjustable by an external resistance ratio.

I_{in} is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$. In models 755 and 759, the magnitude of I_{ref} is internally fixed at 10μA (E_{ref} = 0.1V) or externally adjusted.

Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive*; "P" indicates that only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 759N, with K = +1V, would produce an output voltage, $E_o = -1V \log(100) = -2V$; on the other hand, −10V applied to model 759P with K = 1V, would produce an output voltage, $E_o = -(-1V) \log(100) = +2V$. The figure shows, in condensed form, the outputs of P and N log amps, with differing K values, for both voltage and current inputs, plotted on a semi-log scale.

Log amplifiers in the log mode are useful for applications requiring *compression* of wide-range analog input data, *linearization* of transducers having exponential outputs and *analog computing*, ranging from simple translation of natural relationships in log form (e.g., computing absorbence as the log ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multiterm products and ratios.



Log of Voltage

Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

***A *decade* is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1,000 (3 decades), the output would change by 6V.**

X-AMP is a trademark of Analog Devices, Inc.

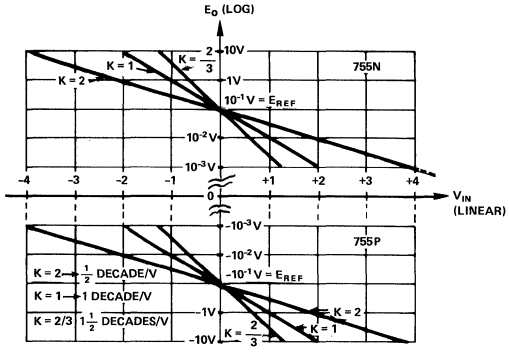
ANTILOGS

In the *antilogarithmic* (exponential) mode, the ideal output equation is

$$E_o = E_{ref}\,(10)^{-E_{in}/K}$$

E_{in} can be positive or negative; when it is zero, $E_o = E_{ref}$. However, E_o is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = −2V, if E_{in} = +4V, and E_{ref} = −0.1V, then $E_o = -0.1V{\cdot}10^{-4/-2}$, or −10V. If E_{in} = −4V, then $E_o = -0.1V{\cdot}10^{-(-4)/-2} = -1mV$. The figure on the next page shows in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

Antilog amplifiers are useful for applications requiring *expansion* of compressed data, *linearization* of transducers having logarithmic outputs, *analog function fitting* or function generation, to obtain relationships or generate curves having voltage-programmable rates of growth or decay, and in *analog computing*, for such functions as compound multiplication and division of terms having differing exponents.



Antilog Operator Response Curves, Semilog Scale
$E_O = E_{REF}\ 10^{V_{IN}/-K}$

LOG-ANTILOG AMPLIFIER PERFORMANCE

Considerable information regarding log- and antilog-amplifier circuit design, performance, selection and applications is to be found in the *Nonlinear Circuits Handbook*[1]. Several salient points will be covered here, and specifications will be defined.

A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the op-amp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.

In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

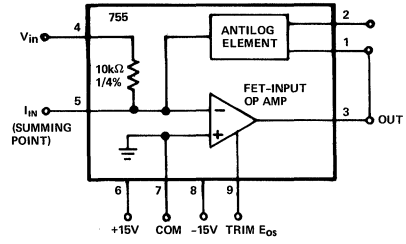
$$I = I_o(\epsilon^{qV/kT} - 1) \cong I_o\epsilon^{qV/kT}$$

and $V = (kT/q)\ \ln\ (I/I_o)$

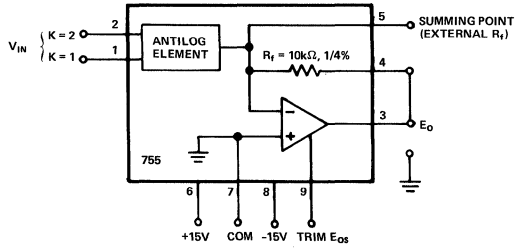
where I is the collector current, I_o is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11,605 K/V) is the ratio of charge of an electron to Boltzmann's constant and T is junction temperature in kelvins. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of I_o's variation with temperature.

$$\begin{aligned}\Delta V &= (kT/q)\ln(I_{in}/I_o) - (kT/q)\ln(I_{ref}/I_o)\\ &= (kT/q)(\ln I_{in} - \ln I_{ref}) + (kT/q)(\ln I_o - \ln I_o)\\ &= (kT/q)\ln(I_{in}/I_{ref})\end{aligned}$$

The temperature dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic 59mV/decade, (kT/q) ln10 at room temperature, to 1V/decade.



a) Log/Antilog Amplifier Connected in the Log Mode (K = 1)



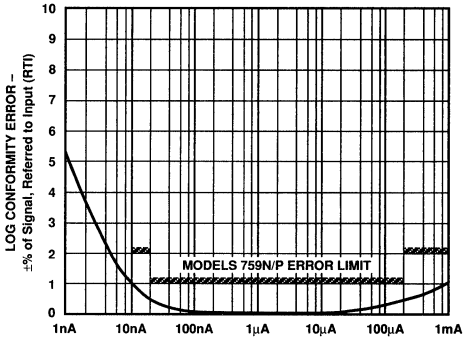
b) Log/Antilog Amplifier Connected in the Exponential Mode

[1]***Nonlinear Circuit Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete MasterCard data to P.O. Box 9106, Norwood, MA 02062-9106.**

Errors are introduced by the offset current of the amplifier (and the offset voltage) for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called *log-conformity error*, which is manifested as a "nonlinearity" of the input-output plot on semilog coordinates. Best log conformity is realized away from the extremities of the rated signal range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4-decade range from 10nA to 100μA. A plot of log conformity error for model 759 is shown below.

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at whatever input level, produce equal incremental errors at the output, for a given value of K. For example, if K = 1, and the RTI log-conformity error is +1%, the magnitude of the output error will be

$$\begin{aligned}\text{Error} &= \text{Actual output} - \text{ideal output}\\ &= 1\text{V}\cdot\log(1.01\ I/I_{ref}) - 1\text{V}\cdot\log(I/I_{ref})\\ &= 1\text{V}\cdot\log 1.01 = 0.0043\text{V} = 4.3\text{mV}\end{aligned}$$



Log Conformity Error for Models 759N and 759P

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

LOG OUTPUT ERROR (mV)

%ERROR RTI	K=1V	K=2V	K=(2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17	5.7
3.0	13	26	8.6
4.0	17	34	11
5.0	21	42	14
10.0	41	83	28

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1μA tend to be roughly comparable. However, below 1μA, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction – step changes in the direction of increasing current are responded to more quickly than step decreases of current.

DEFINITIONS OF SPECIFICATIONS

Log-Conformity Error: When the parameters have been adjusted to compensate for offset, scale-factor and reference errors, the *log-conformity error* is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Offset Current (I_{os}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Offset Voltage (E_{os}) depends on the operational amplifier used for the log operation. Its effect is that of a small voltage in series with the input resistor. For current-logging operations, with high-impedance sources, its error contribution is negligible. However, for voltage logging, it modifies the value of V_{in}. Though it can be adjusted to zero at room temperature, its drift over the temperature range should be considered. In antilog operation, E_{os} appears at the output as an essentially constant voltage; its percentage effect on error is greatest for small outputs.

Reference Current (I_{ref}) is the effective internally-generated current-source output to which all values of input current are compared. I_{ref} tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator or simply by adding a constant bias at the output's destination.

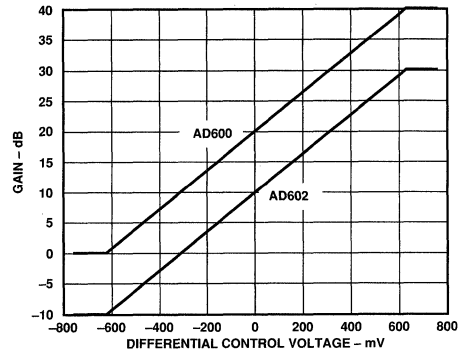
Reference Voltage (E_{ref}) is the effective internally generated voltage to which all input voltages are compared. It is related to I_{ref} by the equation: $E_{ref} = I_{ref}R_{in}$, where R_{in} is the value of input resistance. Typically, I_{ref} is less stable than R_{in}; therefore, practically all the tolerance is due to I_{ref}.

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.

EXPONENTIAL AMPLIFIERS

Another way to achieve signal compression is to vary the gain of an amplifier as the dynamic range of the signal changes. To achieve this, Analog Devices uses its patented X-AMP technology to build precision *exponential amplifiers*. These amplifiers have a linear-to-dB relationship between the applied control voltage and the resulting open loop gain. These amplifiers provide fast-slewing, wide-dynamic-range variable gain. Typically they are employed as fast-response automatic gain control (AGC) elements or to provide time gain control (TGC) in applications such as medical ultrasound or sonar.

The first products in this line are the AD600 and the AD602. These parts offer bandwidths of 30MHz and ultralow input noise spectral densities of 1.4nV/$\sqrt{\text{Hz}}$ in addition to 80dB of variable gain in a single package. Variable gain is actually achieved by providing a *variable attenuation* stage followed by a *fixed gain* stage. In this way, only linear elements are in the variable portion of the signal path, and the frequency response remains constant with gain.



Gain vs. Control Voltage for AD600, AD602

DEFINITIONS OF SPECIFICATIONS

Gain Scaling Factor (dB/V) is the ratio of the change in gain of the amplifier in response to a change in control voltage.

Gain Error (dB): When the parameters have been adjusted to compensate for offset errors, the *gain error* is the maximum deviation from the gain predicted by the gain scaling factor across the range of interest.

Input Noise Spectral Density (nV/$\sqrt{\text{Hz}}$) is the vector sum of *all* voltage and current noise sources referred to the input.

Response Rate (dB/μs) is a measure of how fast the amplifier gain can be changed across its *full* gain range in response to a step change in the control voltage.

Dual, Low Noise, Wideband Variable Gain Amplifiers

AD600/AD602*

FEATURES

Two Channels with Independent Gain Control
"Linear in dB" Gain Response
Two Gain Ranges:
AD600: 0 dB to +40 dB
AD602: −10 dB to +30 dB
Accurate Absolute Gain: ±0.3 dB
Low Input Noise: 1.4 nV/$\sqrt{Hz}$
Low Distortion: −60 dBc THD at ±1 V Output
High Bandwidth: DC to 35 MHz (−3 dB)
Stable Group Delay: ±2 ns
Low Power: 125 mW (max) per Amplifier
Signal Gating Function for Each Amplifier
Drives High Speed A/D Converters

APPLICATIONS

Ultrasound and Sonar Time-Gain Control
High Performance Audio and RF AGC Systems
Signal Measurement

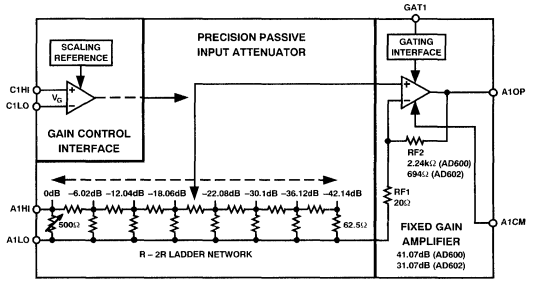
PRODUCT DESCRIPTION

The AD600 and AD602 dual channel, low noise variable gain amplifiers are optimized for use in ultrasound imaging systems, but are applicable to any application requiring very precise gain, low noise and distortion, and wide bandwidth. Each independent channel provides a gain of 0 to +40 dB in the AD600 and −10 dB to +30 dB in the AD602. The lower gain of the AD602 results in an improved signal-to-noise ratio at the output. However, both products have the same 1.4 nV/$\sqrt{Hz}$ input noise spectral density. The decibel gain is directly proportional to the control voltage, is accurately calibrated, and is supply- and temperature-stable.

To achieve the difficult performance objectives, a proprietary circuit form—the X-AMP™—has been developed. Each channel of the X-AMP comprises a variable attenuator of 0 dB to −42.14 dB followed by a high speed fixed gain amplifier. In this way, the amplifier never has to cope with large inputs, and can benefit from the use of negative feedback to precisely define the gain and dynamics. The attenuator is realized as a seven-stage R-2R ladder network having an input resistance of 100 Ω, laser-trimmed to ±2%. The attenuation between tap points is 6.02 dB; the gain-control circuit provides continuous interpolation between these taps. The resulting control function is linear in dB.

X-AMP is a trademark of Analog Devices, Inc.
*Patent pending.

FUNCTIONAL BLOCK DIAGRAM



The gain-control interfaces are fully differential, providing an input resistance of ~15 MΩ and a scale factor of 32 dB/V (that is, 31.25 mV/dB) defined by an internal voltage reference. The response time of this interface is less than 1 μs. Each channel also has an independent gating facility that optionally blocks signal transmission and sets the dc output level to within a few millivolts of the output ground. The gating control input is TTL and CMOS compatible.

The maximum gain of the AD600 is 41.07 dB, and that of the AD602 is 31.07 dB; the −3 dB bandwidth of both models is nominally 35 MHz, essentially independent of the gain. The signal-to-noise ratio (SNR) for a 1 V rms output and a 1 MHz noise bandwidth is typically 76 dB for the AD600 and 86 dB for the AD602. The amplitude response is flat within ±0.5 dB from 100 kHz to 10 MHz; over this frequency range the group delay varies by less than ±2 ns at all gain settings.

Each amplifier channel can drive 100 Ω load impedances with low distortion. For example, the peak specified output is ±2.5 V minimum into a 500 Ω load, or ±1 V into a 100 Ω load. For a 200 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically −60 dBc.

The AD600 and AD602 are available in either a 16-pin plastic DIP or 16-pin SOIC, and are guaranteed for operation over the commercial temperature range of 0°C to +70°C.

AD600/AD602—SPECIFICATIONS

(Each amplifier section, at T_A = +25°C, V_S = ±5 V, −625 mV ≤ V_G ≤ +625 mV, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted. Specifications for AD600 and AD602 are identical unless otherwise noted.)

Parameter	Conditions	AD600J/AD602J Min	Typ	Max	Units
INPUT CHARACTERISTICS					
Input Resistance	Pins 2 to 3; Pins 6 to 7	**98**	100	**102**	Ω
Input Capacitance			2		pF
Input Noise Spectral Density[1]			1.4		nV/√Hz
Noise Figure	R_S = 50 Ω, Maximum Gain		5.3		dB
	R_S = 200 Ω, Maximum Gain		2		dB
Common-Mode Rejection Ratio	f = 100 kHz		30		dB
OUTPUT CHARACTERISTICS					
−3 dB Bandwidth	V_{OUT} = 100 mV rms		35		MHz
Slew Rate			275		V/μs
Peak Output[2]	$R_L \geq$ 500 Ω	±2.5	±3		V
Output Impedance	f ≤ 10 MHz		2		Ω
Output Short-Circuit Current			50		mA
Group Delay Change vs. Gain	f = 3 MHz; Full Gain Range		±2		ns
Group Delay Change vs. Frequency	V_G = 0 V; f = 1 to 10 MHz		±2		ns
Total Harmonic Distortion	R_L = 200 Ω, V_{OUT} = ±1 V peak, Rpd = 1 kΩ		−60		dBc
ACCURACY					
AD600					
Gain Error	0 dB to 3 dB Gain	**0**	+0.5	**+1**	dB
	3 dB to 37 dB Gain	**−0.5**	±0.2	**+0.5**	dB
	37 dB to 40 dB Gain	**−1**	−0.5	**0**	dB
Maximum Output Offset Voltage[3]	V_G = −625 mV to +625 mV		10	**50**	mV
Output Offset Variation	V_G = −625 mV to +625 mV		10	**50**	mV
AD602					
Gain Error	−10 dB to −7 dB Gain	**0**	0.5	**+1**	dB
	−7 dB to 27 dB Gain	**−0.5**	±0.2	**+0.5**	dB
	27 dB to 30 dB Gain	**−1**	−0.5	**0**	dB
Maximum Output Offset Voltage[3]	V_G = −625 mV to +625 mV		5	**30**	mV
Output Offset Variation	V_G = −625 mV to +625 mV		5	**30**	mV
GAIN CONTROL INTERFACE					
Gain Scaling Factor	3 to 37 dB (AD600); −7 to 27 dB (AD602)	**31.7**	32	**32.3**	dB/V
Common-Mode Range		−0.75		2.5	V
Input Bias Current			0.35	1	μA
Input Offset Current			10	50	nA
Differential Input Resistance	Pins 1 to 16; Pins 8 to 9		15		MΩ
Response Rate	Full 40 dB Gain Change		40		dB/μs
SIGNAL GATING INTERFACE					
Logic Input "LO" (Output ON)				0.8	V
Logic Input "HI" (Output OFF)		2.4			V
Response Time	ON to OFF, OFF to ON		0.3		μs
Input Resistance	Pin 4 to 3; Pin 5 to 6		30		kΩ
Output Gated OFF					
Output Offset Voltage			±10	**±100**	mV
Output Noise Spectral Density			65		nV/√Hz
Signal Feedthrough @ 1 MHz					
AD600			−80		dB
AD602			−70		dB
POWER SUPPLY					
Specified Operating Range		±4.75		±5.25	V
Quiescent Current			22	**25**	mA

NOTES

[1]Typical open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited. This figure includes the effects of both voltage and current noise sources.

[2]Using resistive loads of 500 Ω or greater, or with the addition of a 1 kΩ pull-down resistor when driving lower loads.

[3]The dc gain of the main amplifier in the AD600 is X113; thus an input offset of only 100 μV becomes an 11.3 mV output offset. In the AD602, the amplifier's gain is X35.7; thus, an input offset of 100 μV becomes a 3.57 mV output offset.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $\pm V_S$ . . . . . ±7.5 V
Input Voltages
Pins 1, 8, 9, 16 . . . . . $\pm V_S$
Pins 2, 3, 6, 7 . . . . . ±2 V Continuous
. . . . . $\pm V_S$ for 10 ms
Pins 4, 5 . . . . . $\pm V_S$
Internal Power Dissipation . . . . . 600 mW
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Soldering 60 sec . . . . . +300°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics:
16-Pin Plastic Package: θ_{JA} = 85°C/Watt
16-Pin SOIC Package: θ_{JA} = 100°C/Watt

ORDERING GUIDE

Model	Gain Range	Temperature Range	Package Option*
AD600JN	0 dB to +40 dB	0°C to +70°C	N-16
AD600JR	0 dB to +40 dB	0°C to +70°C	R-16
AD602JN	−10 dB to +30 dB	0°C to +70°C	N-16
AD602JR	−10 dB to +30 dB	0°C to +70°C	R-16

*N = Plastic DIP; R = Small Outline IC (SOIC). For outline information see Package Information section.

3

CAUTION

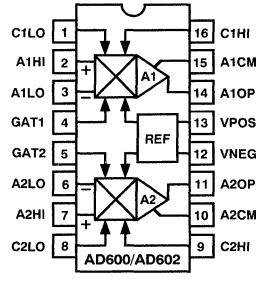
ESD (electrostatic discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN DESCRIPTIONS

Pin	Function	Description
Pin 1	C1LO	CH1 Gain-Control Input "LO" (Positive Voltage Reduces CH1 Gain).
Pin 2	A1HI	CH1 Signal Input "HI" (Positive Voltage Increases CH1 Output).
Pin 3	A1LO	CH1 Signal Input "LO" (Usually Taken to CH1 Input Ground).
Pin 4	GAT1	CH1 Gating Input (A Logic "HI" Shuts Off CH1 Signal Path).
Pin 5	GAT2	CH2 Gating Input (A Logic "HI" Shuts Off CH2 Signal Path).
Pin 6	A2LO	CH2 Signal Input "LO" (Usually Taken to CH2 Input Ground).
Pin 7	A2HI	CH2 Signal Input "HI" (Positive Voltage Increases CH2 Output).
Pin 8	C2LO	CH2 Gain-Control Input "LO" (Positive Voltage Reduces CH2 Gain).
Pin 9	C2HI	CH2 Gain-Control Input "HI" (Positive Voltage Increases CH2 Gain).
Pin 10	A2CM	CH2 Common (Usually Taken to CH2 Output Ground).
Pin 11	A2OP	CH2 Output.
Pin 12	VNEG	Negative Supply for Both Amplifiers.
Pin 13	VPOS	Positive Supply for Both Amplifiers.
Pin 14	A1OP	CH1 Output.
Pin 15	A1CM	CH1 Common (Usually Taken to CH1 Output Ground).
Pin 16	C1HI	CH1 Gain-Control Input "HI" (Positive Voltage Increases CH1 Gain).

CONNECTION DIAGRAM

16-Pin Plastic DIP (N) Package
16-Pin Plastic SOIC (R) Package



THEORY OF OPERATION

The AD600 and AD602 have the same general design and features. They comprise two fixed gain amplifiers, each preceded by a voltage-controlled attenuator of 0 dB to 42.14 dB with independent control interfaces, each having a scaling factor of 32 dB per volt. The gain of each amplifier in the AD600 is laser trimmed to 41.07 dB (X113), thus providing a control range of −1.07 dB to 41.07 dB (0 dB to 40 dB with overlap), while the AD602 amplifiers have a gain of 31.07 dB (X35.8) and provide an overall gain of −11.07 dB to 31.07 dB (−10 dB to 30 dB with overlap).

The advantage of this topology is that the amplifier can use negative feedback to increase the accuracy of its gain; also, since the amplifier never has to handle large signals at its input, the distortion can be very low. A further feature of this approach is that the small-signal gain and phase response, and thus the pulse response, are essentially independent of gain.

The following discussion describes the AD600. Figure 1 is a simplified schematic of one channel. The input attenuator is a seven-section R-2R ladder network, using untrimmed resistors of nominally R = 62.5 Ω, which results in a characteristic resistance of 125 Ω ±20%. A shunt resistor is included at the input and laser trimmed to establish a more exact input resistance of 100 Ω ±2%, which ensures accurate operation (gain and HP corner frequency) when used in conjunction with external resistors or capacitors.

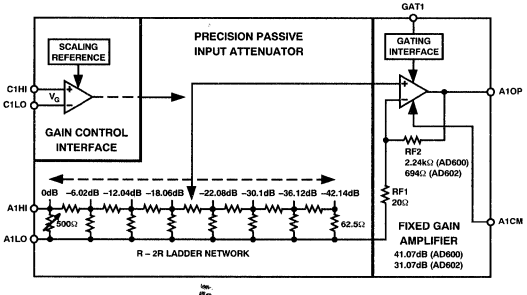


Figure 1. Simplified Block Diagram of Single Channel of the AD600 and AD602

The nominal maximum signal at input A1HI is 1 V rms (±1.4 V peak) when using the recommended ±5 V supplies, although operation to ±2 V peak is permissible with some increase in HF distortion and feedthrough. Each attenuator is provided with a separate signal "LO" connection, for use in rejecting common-mode, the voltage between input and output grounds. Circuitry is included to provide rejection of up to ±100 mV.

The signal applied at the input of the ladder network is attenuated by 6.02 dB by each section; thus, the attenuation to each of the taps is progressively 0, 6.02, 12.04, 18.06, 24.08, 30.1, 36.12 and 42.14 dB. A unique circuit technique is employed to interpolate between these tap points, indicated by the "slider" in Figure 1, providing continuous attenuation from 0 dB to 42.14 dB.

It will help, in understanding the AD600, to think in terms of a mechanical means for moving this slider from left to right; in fact, it is voltage controlled. The details of the control interface are discussed later. Note that the gain is at all times exactly determined, and a linear decibel relationship is automatically guaranteed between the gain and the control parameter which determines the position of the slider. In practice, the gain deviates from the ideal law, by about ±0.2 dB peak (see, for example, Figure 6).

Note that the signal inputs are not fully differential: A1LO and A1CM (for CH1) and A2LO and A2CM (for CH2) provide separate access to the input and output grounds. This recognizes the practical fact that even when using a ground plane, small differences will arise in the voltages at these nodes. It is important that A1LO and A2LO be connected directly to the input ground(s); significant impedance in these connections will reduce the gain accuracy. A1CM and A2CM should be connected to the load ground(s).

Noise Performance

An important reason for using this approach is the superior noise performance that can be achieved. The nominal resistance seen at the inner tap points of the attenuator is 41.7 Ω (one third of 125 Ω), which exhibits a Johnson noise spectral density (NSD) of 0.84 nV/$\sqrt{\text{Hz}}$ (that is, $\sqrt{4kTR}$) at 27°C, which is a large fraction of the total input noise. The first stage of the amplifier contributes a further 1.12 nV/$\sqrt{\text{Hz}}$, for a total input noise of 1.4 nV/$\sqrt{\text{Hz}}$.

The noise at the 0 dB tap depends on whether the input is short-circuited or open-circuited: when shorted, the minimum NSD of 1.12 nV/$\sqrt{\text{Hz}}$ is achieved; when open, the resistance of 100 Ω at the first tap generates 1.29 nV/$\sqrt{\text{Hz}}$, so the noise increases to a total of 1.71 nV/$\sqrt{\text{Hz}}$. (This last calculation would be important if the AD600 were preceded, for example, by a 900 Ω resistor to allow operation from inputs up to ±10 V rms. However, in most cases the low impedance of the source will limit the maximum noise resistance.)

It will be apparent from the foregoing that it is essential to use a low resistance in the design of the ladder network to achieve low noise. In some applications this may be inconvenient, requiring the use of an external buffer or preamplifier. However, very few amplifiers combine the needed low noise with low distortion at maximum input levels, and the power consumption needed to achieve this performance is fundamentally required to be quite high (due to the need to maintain very low resistance values while also coping with large inputs). On the other hand, there is little value in providing a buffer with high input impedance, since the usual reason for this—the minimization of loading of a high resistance source—is not compatible with low noise.

Apart from the small variations just discussed, the signal-to-noise (S/N) ratio at the output is essentially independent of the attenuator setting, since the maximum undistorted output is 1 V rms and the NSD at the output of the AD600 is fixed at 113 times 1.4 nV$\sqrt{\text{Hz}}$, or 158 nV/$\sqrt{\text{Hz}}$. Thus, in a 1 MHz bandwidth, the output S/N ratio would be 76 dB. The input NSD of the AD600 and AD602 are the same, but because of the 10 dB lower gain in the AD602's fixed amplifier, its output S/N ratio is 10 dB better, or 86 dB in a 1 MHz bandwidth.

The Gain-Control Interface

The attenuation is controlled through a differential, high impedance (15 MΩ) input, with a scaling factor which is laser trimmed to 32 dB per volt, that is, 31.25 mV/dB. Each of the two amplifiers has its own control interface. An internal bandgap reference ensures stability of the scaling with respect to supply and temperature variations, and is the only circuitry common to both channels.

When the differential input voltage V_G = 0 V, the attenuator "slider" is centered, providing an attenuation of 21.07 dB, thus resulting in an overall gain of 20 dB (= −21.07 dB + 41.07 dB). When the control input is −625 mV, the gain is lowered by 20 dB (= 0.625 × 32), to 0 dB; when set to +625 mV, the gain is increased by 20 dB, to 40 dB. When this interface is overdriven in either direction, the gain approaches either −1.07 dB (= −42.14 dB + 41.07 dB) or 41.07 dB (= 0 + 41.07 dB), respectively.

The gain of the AD600 can thus be calculated using the following simple expression:

$$Gain\ (dB) = 32\ V_G + 20 \quad (1)$$

where V_G is in volts. For the AD602, the expression is:

$$Gain\ (dB) = 32\ V_G + 10 \quad (2)$$

Operation is specified for V_G in the range from −625 mV dc to +625 mV dc. The high impedance gain-control input ensures minimal loading when driving many amplifiers in multiple-channel applications. The differential input configuration provides flexibility in choosing the appropriate signal levels and polarities for various control schemes.

For example, the gain-control input can be fed differentially to the inputs, or single-ended by simply grounding the unused input. In another example, if the gain is to be controlled by a DAC providing a positive only ground referenced output, the "Gain Control LO" pin (either C1LO or C2LO) should be biased to a fixed offset of +625 mV, to set the gain to 0 dB when "Gain Control HI" (C1HI or C2HI) is at zero, and to 40 dB when at +1.25 V.

It is a simple matter to include a voltage divider to achieve other scaling factors. When using an 8-bit DAC having a FS output of +2.55 V (10 mV/bit) a divider ratio of 1.6 (generating 6.25 mV/bit) would result in a gain setting resolution of 0.2 dB/bit. Later, we will discuss how the two sections of an AD600 or AD602 may be cascaded, when various options exist for gain control.

Signal-Gating Inputs

Each amplifier section of the AD600 and AD602 is equipped with a signal gating function, controlled by a TTL or CMOS logic input (GAT1 or GAT2). The ground references for these inputs are the signal input grounds A1LO and A2LO, respectively. Operation of the channel is unaffected when this input is LO or left open-circuited. Signal transmission is blocked when this input is HI. The dc output level of the channel is set to within a few millivolts of the output ground (A1CM or A2CM), and simultaneously the noise level drops significantly. The reduction in noise and spurious signal feedthrough is useful in ultrasound beam-forming applications, where many amplifier outputs are summed.

Common-Mode Rejection

A special circuit technique is used to provide rejection of voltages appearing between input grounds (A1LO and A2LO) and output grounds (A1CM and A2CM). This is necessary because of the "op amp" form of the amplifier, as shown in Figure 1. The feedback voltage is developed across the resistor RF1 (which, to achieve low noise, has a value of only 20 Ω). The voltage developed across this resistor is referenced to the input common, so the output voltage is also referred to that node.

To provide rejection of this common voltage, an auxiliary amplifier (not shown) is included, which senses the voltage difference between input and output commons and cancels this error component. Thus, for zero differential signal input between A1HI and A1LO, the output A1OP simply follows the voltage at A1CM. Note that the range of voltage differences which can exist between A1LO and A1CM (or A2LO and A2CM) is limited to about ±100 mV. Figure 50 (one of the typical performance curves at the end of this data sheet) shows typical common-mode rejection ratio versus frequency.

ACHIEVING 80 dB GAIN RANGE

The two amplifier sections of the X-AMP can be connected in series to achieve higher gain. In this mode, the output of A1 (A1OP and A1CM) drives the input of A2 via a high-pass network (usually just a capacitor) that rejects the dc offset. The nominal gain range is now −2 dB to +82 dB for the AD600 or −22 dB to +62 dB for the AD602.

There are several options in connecting the gain-control inputs. The choice depends on the desired signal-to-noise ratio (SNR) and gain error (output ripple). The following examples feature the AD600; the arguments generally apply to the AD602, with appropriate changes to the gain values.

Sequential Mode (Maximum S/N Ratio)

In the sequential mode of operation, the SNR is maintained at its highest level for as much of the gain control range possible, as shown in Figure 2. Note here that the gain range is 0 dB to 80 dB. Figure 3 shows the general connections to accomplish this. Both gain-control inputs, C1HI and C2HI, are driven in parallel by a positive only, ground referenced source with a range of 0 V to +2.5 V.

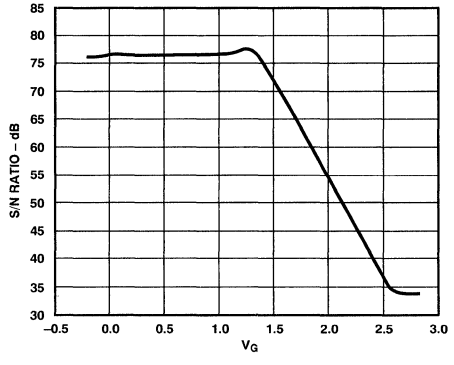


Figure 2. S/N Ratio vs. Control Voltage Sequential Control (1 MHz Bandwidth)

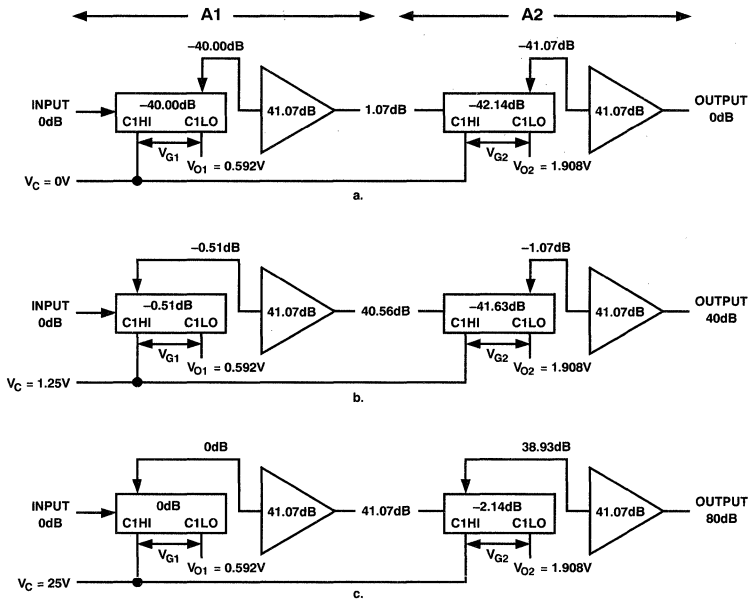


Figure 3. AD600 Gain Control Input Calculations for Sequential Control Operation

The gains are offset (Figure 4) such that A2's gain is increased only after A1's gain has reached its maximum value. Note that for a differential input of −700 mV or less, the gain of a single amplifier (A1 or A2) will be at its minimum value of −1.07 dB; for a differential input of +700 mV or more, the gain will be at its maximum value of 41.07 dB. Control inputs beyond these limits will not affect the gain and can be tolerated without damage or foldover in the response. See the Specifications Section of this data sheet for more details on the allowable voltage range. The gain is now

$$Gain\ (dB) = 32\ V_C \qquad (3)$$

where V_C is the applied control voltage.

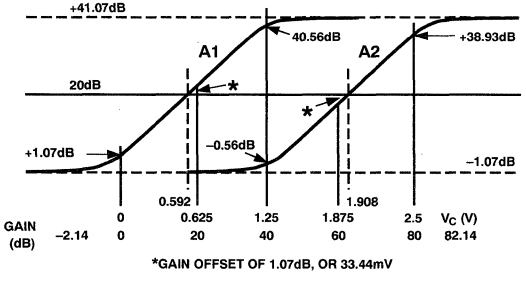


Figure 4. Explanation of Offset Calibration for Sequential Control

When V_C is set to zero, V_{G1} = −0.592 V and the gain of A1 is +1.07 dB (recall that the gain of each amplifier section is 0 dB for V_G = −625 mV); meanwhile, V_{G2} = −1.908 V so the gain of A2 is −1.07 dB. The overall gain is thus 0 dB (see Figure 3a). When V_C = +1.25 V, V_{G1} = 1.25 V − 0.592 V = +0.658 V, which sets the gain of A1 to 40.56 dB, while V_{G2} = 1.25 V − 1.908 V = −0.658 V, which sets A2's gain at −0.56 dB. The overall gain is now 40 dB (see Figure 3b). When V_C = +2.5 V, the gain of A1 is 41.07 dB and that of A2 is 38.93 dB, resulting in an overall gain of 80 dB (see Figure 3c). This mode of operation is further clarified by Figure 5, which is a plot of the separate gains of A1 and A2 and the overall gain versus the control voltage. Figure 6 is a plot of the gain error of the cascaded amplifiers versus the control voltage.

Parallel Mode (Simplest Gain-Control Interface)

In this mode, the gain-control voltage is applied to both inputs in parallel — C1HI and C2HI are connected to the control voltage, and C1LO and C2LO are optionally connected to an offset voltage of +0.625 V. The gain scaling is then doubled to 64 dB/V, requiring only 1.25 V for an 80 dB change of gain. The amplitude of the gain ripple in this case is also doubled, as shown in Figure 7, and the instantaneous signal-to-noise ratio at the output of A2 decreases linearly as the gain is increased (Figure 8).

Low Ripple Mode (Minimum Gain Error)

As can be seen in Figures 6 and 7, the output ripple is periodic. By offsetting the gains of A1 and A2 by half the period of the ripple, or 3 dB, the residual gain errors of the two amplifiers can be made to cancel. Figure 9 shows the much lower gain ripple when configured in this manner. Figure 10 plots the S/N ratio as a function of gain; it is very similar to that in the "Parallel Mode."

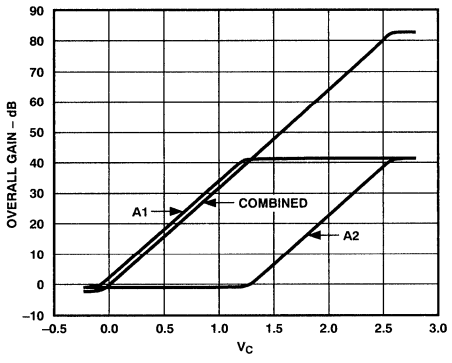


Figure 5. Plot of Separate and Overall Gains in Sequential Control

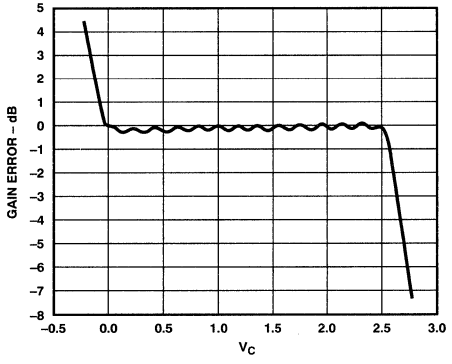


Figure 6. Gain Error for Cascaded Stages—Sequential Control

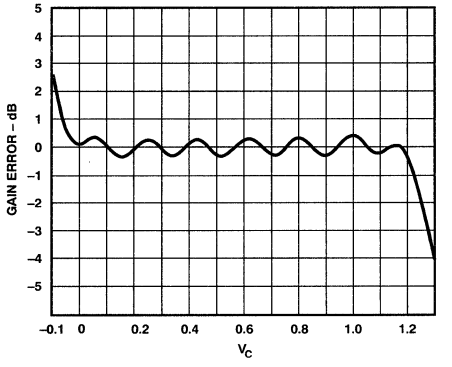


Figure 7. Gain Error for Cascaded Stages—Parallel Control

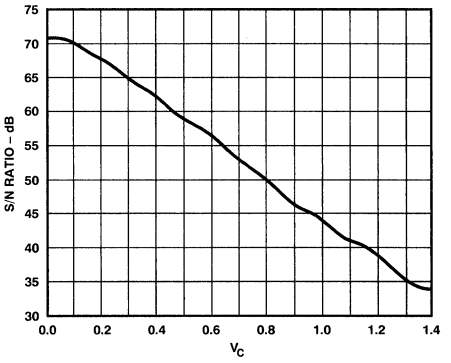


Figure 8. SNR for Cascaded Stages—Parallel Control

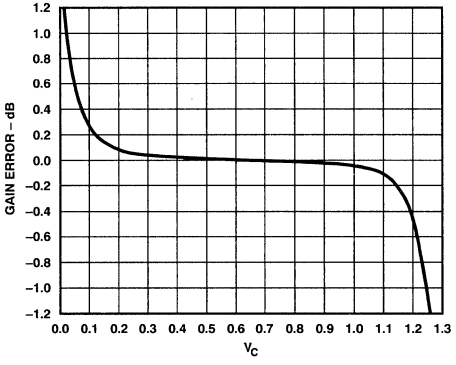


Figure 9. Gain Error for Cascaded Stages—Low Ripple Mode

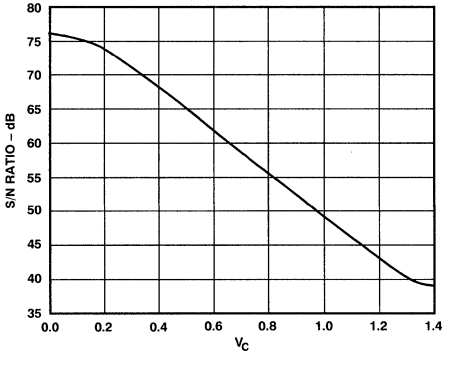


Figure 10. ISNR vs. Control Voltage—Low Ripple Mode

APPLICATIONS

The full potential of any high performance amplifier can only be realized by careful attention to details in its applications. The following pages describe fully tested circuits in which many such details have already been considered. However, as is always true of high accuracy, high speed analog circuits, the schematic is only part of the story; this is no less true for the AD600 and AD602. Appropriate choices in the overall board layout and the type and placement of power supply decoupling components are very important. As explained previously, the input grounds A1LO and A2LO must use the shortest possible connections.

The following circuits show examples of time-gain control for ultrasound and for sonar, methods for increasing the output drive, and AGC amplifiers for audio and RF/IF signal processing using both peak and rms detectors. These circuits also illustrate methods of cascading X-AMPs for either maintaining the optimal S/N ratio or maximizing the accuracy of the gain-control voltage for use in signal measurement. These AGC circuits may be modified for use as voltage-controlled amplifiers for use in sonar and ultrasound applications by removing the detector and substituting a DAC or other voltage source for supplying the control voltage.

Time-Gain Control (TGC) and Time-Variable Gain (TVG)

Ultrasound and sonar systems share a similar requirement: both need to provide an exponential increase in gain in response to a linear control voltage, that is, a gain control that is "linear in dB." Figure 11 shows the AD600/AD602 configured for a control voltage ramp starting at −625 mV and ending at +625 mV for a gain-control range of 40 dB. For simplicity, only the A1 connections are shown. The polarity of the gain-control voltage may be reversed and the control voltage inputs C1HI and C1LO reversed to achieve the same effect. The gain-control voltage can be supplied by a voltage-output DAC such as the AD7242, which contains two complete DACs, operates from ±5 V supplies, has an internal reference of 3 V, and provides ±3 V of output swing. As such it is well-suited for use with the AD600/AD602, needing only a few resistors to scale the output voltage of the DACs to the levels needed by the AD600/AD602.

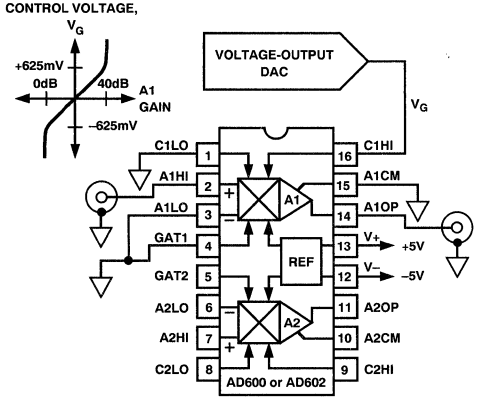


Figure 11. The Simplest Application of the X-AMP is as a TGC or TVG Amplifier in Ultrasound or Sonar. Only the A1 Connections Are Shown for Simplicity.

Increasing Output Drive

The AD600/AD602's output stage has limited capability for negative-load driving capability. For driving loads less than 500 Ω, the load drive may be increased by about 5 mA by connecting a 1 kΩ pull-down resistor from the output to the negative supply (Figure 12).

Driving Capacitive Loads

For driving capacitive loads of greater than 5 pF, insert a 10 Ω resistor between the output and the load. This lowers the possibility of oscillation.

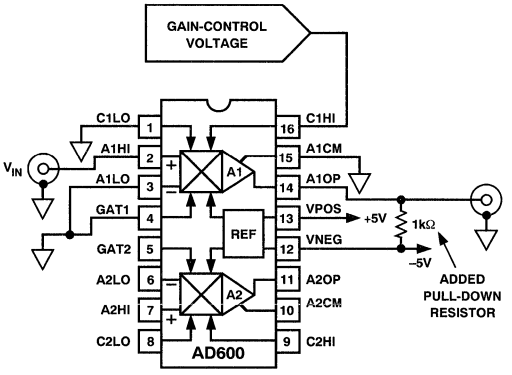


Figure 12. Adding a 1 kΩ Pull-Down Resistor Increases the X-AMP's Output Drive by About 5 mA. Only the A1 Connections Are Shown for Simplicity.

Realizing Other Gain Ranges

Larger gain ranges can be accommodated by cascading amplifiers. Combinations built by cascading two amplifiers include −20 dB to +60 dB (using one AD602), −10 dB to +70 dB (1/2 of an AD602 followed by 1/2 of an AD600), and 0 dB to 80 dB (one AD600). In multiple-channel applications, extra protection against oscillations can be provided by using amplifier sections from different packages.

An Ultralow Noise VCA

The two channels of the AD600 or AD602 may be operated in parallel to achieve a 3 dB improvement in noise level, providing 1 nV/$\sqrt{\text{Hz}}$ without any loss of gain accuracy or bandwidth.

In the simplest case, as shown in Figure 13, the signal inputs A1HI and A2HI are tied directly together, the outputs A1OP and A2OP are summed via R1 and R2 (100 Ω each), and the control inputs C1HI/C2HI and C1LO/C2LO operate in parallel. Using these connections, both the input and output resistances are 50 Ω. Thus, when driven from a 50 Ω source and terminated in a 50 Ω load, the gain is reduced by 12 dB, so the gain range becomes −12 dB to +28 dB for the AD600 and −22 dB to +18 dB for the AD602. The peak input capability remains unaffected (1 V rms at the IC pins, or 2 V rms from an unloaded 50 Ω source). The loading on each output, with a 50 Ω load, is effectively 200 Ω, because the load current is shared between the two channels, so the overall amplifier still meets its specified maximum output and distortion levels for a 200 Ω load. This amplifier can deliver a maximum sine wave power of +10 dBm to the load.

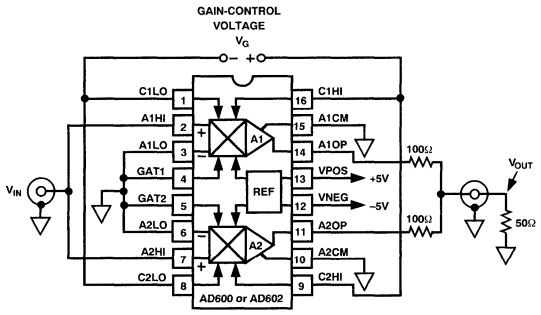


Figure 13. An Ultralow Noise VCA Using the AD600 or AD602

A Low Noise, 6 dB Preamplifier

In some ultrasound applications, the user may wish to use a high input impedance preamplifier to avoid the signal attenuation that would result from loading the transducer by the 100 Ω input resistance of the X-AMP. High gain cannot be tolerated, because the peak transducer signal is typically ±0.5 V, while the peak input capability of the AD600 or AD602 is only slightly more than ±1 V. A gain of two is a suitable choice. It can be shown that if the preamplifier's overall referred-to-input (RTI) noise is to be the same as that due to the X-AMP alone (1.4 nV/$\sqrt{\text{Hz}}$), then the input noise of a X2 preamplifier must be $\sqrt{(3/4)}$ times as large, that is, 1.2 nV/$\sqrt{\text{Hz}}$.

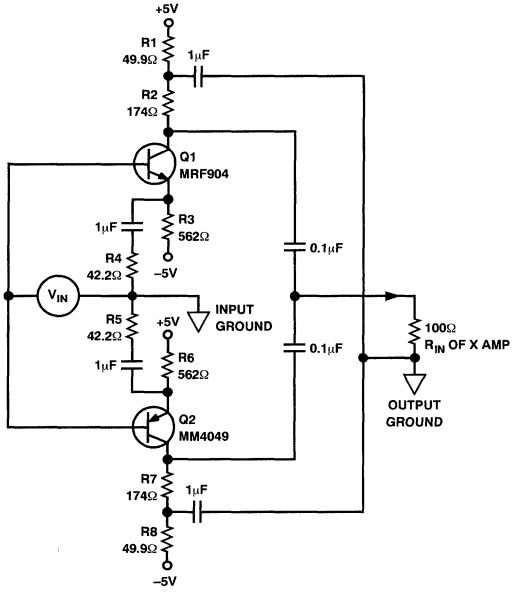


Figure 14. A Low Noise Preamplifier for the AD600 and AD602

An inexpensive circuit, using complementary transistor types chosen for their low $r_{bb'}$, is shown in Figure 14. The gain is determined by the ratio of the net collector load resistance to the net emitter resistance, that is, it is an open-loop amplifier. The gain will be X2 (6 dB) only into a 100 Ω load, assumed to be provided by the input resistance of the X-AMP; R2 and R7 are in shunt with this load, and their value is important in defining the gain. For small-signal inputs, both transistors contribute an equal transconductance, which is rendered less sensitive to signal level by the emitter resistors R4 and R5, which also play a dominant role in setting the gain.

This is a Class AB amplifier. As V_{IN} increases in a positive direction, Q1 conducts more heavily and its r_e becomes lower while that of Q2 increases. Conversely, more negative values of V_{IN} result in the r_e of Q2 decreasing, while that of Q1 increases. The design is chosen such that the net emitter resistance is essentially independent of the instantaneous value of V_{IN}, resulting in moderately low distortion. Low values of resistance and moderately high bias currents are important in achieving the low noise, wide bandwidth, and low distortion of this preamplifier. Heavy decoupling prevents noise on the power supply lines from being conveyed to the input of the X-AMP.

Table I. Measured Preamplifier Performance

Measurement		Value	Units
Gain (f = 30 MHz)		6	dB
Bandwidth (−3 dB)		250	MHz
Input Signal for 1 dB Compression		1	V p-p
Distortion			
V_{IN} = 200 mV p-p	HD2	0.27	%
	HD3	0.14	%
V_{IN} = 500 mV p-p	HD2	0.44	%
	HD3	0.58	%
System Input Noise Spectral Density (NSD) (Preamp plus X-AMP)		1.03	nV/$\sqrt{\text{Hz}}$
Input Resistance		1.4	kΩ
Input Capacitance		15	pF
Input Bias Current		±150	μA
Power Supply Voltage		±5	V
Quiescent Current		15	mA

A Low Noise AGC Amplifier with 80 dB Gain Range

Figure 15 provides an example of the ease with which the AD600 can be connected as an AGC amplifier. A1 and A2 are cascaded, with 6 dB of attenuation introduced by the 100 Ω resistor R1, while a time constant of 5 ns is formed by C1 and the 50 Ω of net resistance at the input of A2. This has the dual effect of (a) lowering the overall gain range from {0 dB to 80 dB} to {6 dB to 74 dB} and (b) introducing a single-pole low-pass filter with a −3 dB frequency of about 32 MHz. This ensures stability at the maximum gain for a slight reduction in the overall bandwidth. The capacitor C4 blocks the small dc offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high pass corner at about 8 kHz, useful in eliminating low frequency noise and spurious signals which may be present at the input.

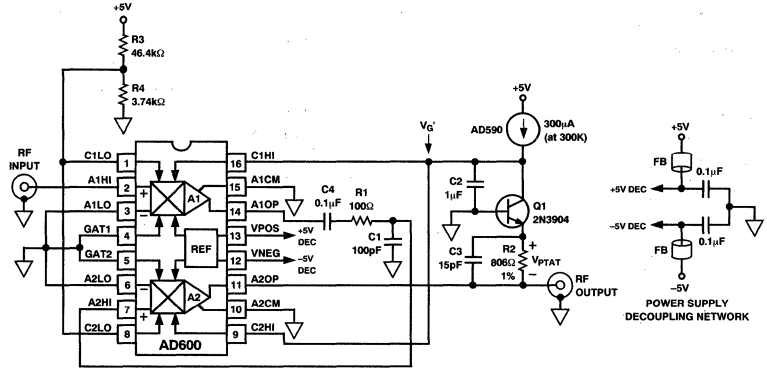


Figure 15. This Accurate HF AGC Amplifier Uses Just Three Active Components.

A simple half-wave detector is used, based on Q1 and R2. The average current into capacitor C2 is just the difference between the current provided by the AD590 (300 μA at 300 K, 27°C) and the collector current of Q1. In turn, the control voltage V_G is the time integral of this *error* current. When V_G (and thus the gain) is stable, the rectified current in Q1 must, on average, exactly balance the current in the AD590. If the output of A2 is too small to do this, V_G will ramp up, causing the gain to increase, until Q1 conducts sufficiently. The operation of this control system will now be described in detail.

First, consider the particular case where R2 *is zero* and the output voltage V_{OUT} is a square wave at, say, 100 kHz, that is, well above the corner frequency of the control loop. During the time V_{OUT} is negative, Q1 conducts; when V_{OUT} is positive, it is cut off. Since the *average* collector current is forced to be 300 μA, and the square wave has a 50% duty-cycle, the current when conducting must be 600 μA. With R2 omitted, the peak value of V_{OUT} would be just the V_{BE} of Q1 at 600 μA (typically about 700 mV) or 2 V_{BE} peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically −1.7 mV/°C. While this may not be troublesome in some applications, the correct value of R2 will render the output stable with temperature.

To understand this, first note that the current in the AD590 is closely proportional to absolute temperature (PTAT). (In fact, this IC is intended for use as a thermometer.) For the moment, continue to assume that the signal is a square wave. When Q1 is conducting, V_{OUT} is the now the *sum* of V_{BE} and a voltage which is PTAT and which can be chosen to have an equal but opposite TC to that of the base-to-emitter voltage. This is actually nothing more than the "bandgap voltage reference" principle in thinly veiled disguise! When we choose R2 such that the sum of the voltage across it and the V_{BE} of Q1 is close to the bandgap voltage of about 1.2 V, V_{OUT} will be stable over a wide range of temperatures, provided, of course, that Q1 and the AD590 share the same thermal environment.

Since the average emitter current is 600 μA during each half-cycle of the square wave, a resistor of 833 Ω would add a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value of R2 will depend on the transistor used, and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the devices shown and sine wave signals, the recommended value is 806 Ω. This resistor also serves to lower the peak current in Q1 and the 200 Hz LP filter it forms with C2 helps to minimize distortion due to ripple in V_G. Note that the output amplitude under sine wave conditions will be higher than for a square wave, since the average value of the current *for an ideal rectifier* would be 0.637 times as large, causing the output amplitude to be 1.88 (=1.2/0.637) V, or 1.33 V rms. In practice, the somewhat non-ideal rectifier results in the sine wave output being regulated to about 1.275 V rms.

An offset of +375 mV is applied to the inverting gain-control inputs C1LO and C2LO. Thus the nominal −625 mV to +625 mV range for V_G is translated upwards (at V_G') to −0.25 V for minimum gain to +1 V for maximum gain. This prevents Q1 from going into heavy saturation at low gains and leaves sufficient "headroom" of 4 V for the AD590 to operate correctly at high gains when using a +5 V supply.

In fact, the 6 dB interstage attenuator means that the overall gain of this AGC system actually runs from −6 dB to +74 dB. Thus, an input of 2 V rms would be required to produce a 1 V rms output at the minimum gain, which exceeds the 1 V rms maximum input specification of the AD600. The *available gain* range is therefore 0 dB to 74 dB (or, X1 to X5000). Since the gain scaling is 15.625 mV/dB (because of the cascaded stages) the minimum value of V_G' is actually increased by 6 × 15.625 mV, or about 94 mV, to −156 mV, so the risk of saturation in Q1 is reduced.

The emitter circuit of Q1 is somewhat inductive (due its finite f_t and base resistance). Consequently, the effective value of R2 increases with frequency. This would result in an increase in the stabilized output amplitude at high frequencies, but for the addition of C3, determined experimentally to be 15 pF for the 2N3904 for maximum response flatness. Alternatively, a faster transistor can be used here to reduce HF peaking. Figure 16 shows the ac response at the stabilized output level of about 1.3 V rms. Figure 17 demonstrates the output stabilization for sine wave inputs of 1 mV to 1 V rms at frequencies of 100 kHz, 1 MHz and 10 MHz.

While the "bandgap" principle used here sets the output amplitude to 1.2 V (for the square wave case), the stabilization point can be set to any higher amplitude, up to the maximum output of ± (V_S − 2) V which the AD600 can support. It is only necessary to split R2 into two components of appropriate ratio whose parallel sum remains close to the zero-TC value of 806 Ω. This is illustrated in Figure 18, which shows how the output can be raised, without altering the temperature stability.

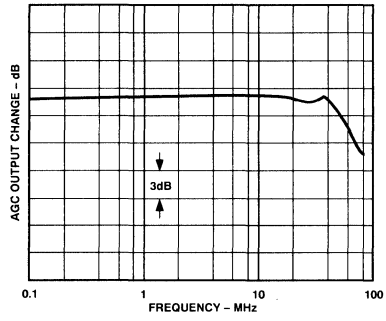


Figure 16. AC Response at the Stabilized Output Level of 1.3 V RMS

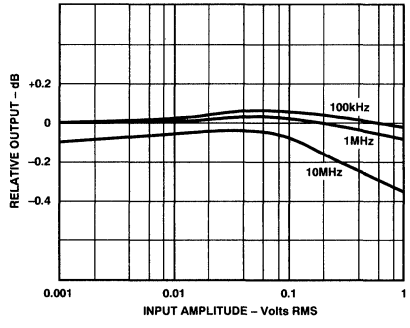


Figure 17. Output Stabilization vs. RMS Input for Sine Wave Inputs at 100 kHz, 1 MHz, and 10 MHz

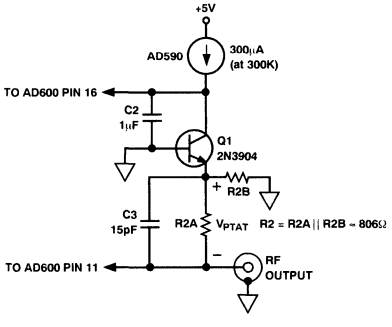


Figure 18. Modification in Detector to Raise Output to 2 V RMS

A Wide Range, RMS-Linear dB Measurement System (2 MHz AGC Amplifier with RMS Detector)

Monolithic rms-dc converters provide an inexpensive means to measure the rms value of a signal of arbitrary waveform, and they also may provide a low accuracy logarithmic ("decibel-scaled") output. However, they have certain shortcomings. The first of these is their restricted dynamic range, typically only 50 dB. More troublesome is that the bandwidth is roughly proportional to the signal level; for example, the AD636 provides a 3 dB bandwidth of 900 kHz for an input of 100 mV rms, but has a bandwidth of only 100 kHz for a 10 mV rms input. Its logarithmic output is unbuffered, uncalibrated and not stable over temperature; considerable support circuitry, including at least two adjustments and a special high TC resistor, is required to provide a useful output.

All of these problems can be eliminated using an AD636 as *merely the detector element* in an AGC loop, in which the difference between the rms output of the amplifier and a fixed dc reference are nulled in a loop integrator. The dynamic range and the accuracy with which the signal can be determined are now entirely dependent on the amplifier used in the AGC system. Since the input to the rms-dc converter is forced to a constant amplitude, close to its maximum input capability, the bandwidth is no longer signal dependent. If the amplifier has an exactly exponential ("linear-dB") gain-control law, its control voltage V_G is forced by the AGC loop to be have the general form:

$$V_{OUT} = V_{SCALE} \log 10 \frac{V_{IN(RMS)}}{V_{REF}} \quad (4)$$

Figure 19 shows a practical wide dynamic range rms-responding measurement system using the AD600. Note that the signal output of this system is available at A2OP, and the circuit can be used as a wideband AGC amplifier with an rms-responding detector. This circuit can handle inputs from 100 μV to 1 V rms with a constant measurement bandwidth of 20 Hz to 2 MHz, limited primarily by the AD636 rms converter. Its logarithmic output is a loadable voltage, accurately calibrated to 100 mV/dB, or 2 V per decade, which simplifies the interpretation of the reading when using a DVM, and is arranged to be −4 V for an input of 100 μV rms input, zero for 10 mV, and +4 V for a 1 V rms input. In terms of Equation 4, V_{REF} is 10 mV and V_{SCALE} is 2 V.

Note that the peak "log output" of ±4 V requires the use of ±6 V supplies for the dual op amp U3 (AD712) although lower supplies would suffice for the AD600 and AD636. If only ±5 V supplies are available, it will be either necessary to use a reduced value for V_{SCALE} (say 1 V, in which case the peak output would be only ±2 V) or restrict the dynamic range of the signal to about 60 dB.

As in the previous case, the two amplifiers of the AD600 are used in cascade. However, the 6 dB attenuator and low-pass filter found in Figure 1 are replaced by a unity gain buffer amplifier U3A, whose 4 MHz bandwidth eliminates the risk of instability at the highest gains. The buffer also allows the use of a high impedance coupling network (C1/R3) which introduces a high-pass corner at about 12 Hz. An input attenuator of 10 dB (X0.316) is now provided by R1 + R2 operating in conjunction with the AD600's input resistance of 100 Ω. The adjustment provides exact calibration of the logarithmic intercept V_{REF} in critical applications, but R1 and R2 may be replaced by a fixed resistor of 215 Ω if very close calibration is not needed, since the input resistance of the AD600 (and all other key parameters of it and the AD636) are already laser trimmed for accurate operation. This attenuator allows inputs as large as ±4 V to be accepted, that is, signals with an rms value of 1 V combined with a crest factor of up to 4.

The output of A2 is ac coupled via another 12 Hz high-pass filter formed by C2 and the 6.7 kΩ input resistance of the AD636. The averaging time constant for the rms-dc converter is determined by C4. The unbuffered output of the AD636 (at Pin 8) is compared with a fixed voltage of +316 mV set by the positive

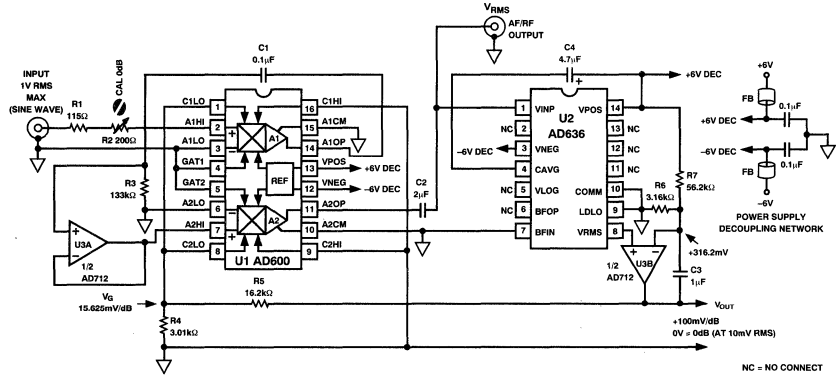


Figure 19. The Output of This Three-IC Circuit Is Proportional to the Decibel Value of the RMS Input.

supply voltage of +6 V and resistors R6 and R7. (V_{REF} is proportional to this voltage, and systems requiring greater calibration accuracy should replace the supply dependent reference with a more stable source.)

Any difference in these voltages is integrated by the op amp U3B, with a time constant of 3 ms formed by the parallel sum of R6/R7 and C3. Now, if the output of the AD600 is too high, V_{RMS} will be greater than the "setpoint" of 316 mV, causing the output of U3B—that is, V_{OUT}—to ramp up (note that the integrator is noninverting). A fraction of V_{OUT} is connected to the inverting gain-control inputs of the AD600, so causing the gain to be reduced, as required, until V_{RMS} is exactly equal to 316 mV, at which time the ac voltage at the output of A2 is forced to be exactly 316 mV rms. This fraction is set by R4 and R5 such that a 15.625 mV change in the control voltages of A1 and A2—which would change the gain of the cascaded amplifiers by 1 dB—requires a change of 100 mV at V_{OUT}. Notice here that since A2 is forced to operate at an output level well below its capacity, waveforms of high crest factor can be tolerated throughout the amplifier.

To check the operation, assume an input of 10 mV rms is applied to the input, which results in a voltage of 3.16 mV rms at the input to A1, due to the 10 dB loss in the attenuator. If the system operates as claimed, V_{OUT} (and hence V_G) should be zero. This being the case, the gain of both A1 and A2 will be 20 dB and the output of the AD600 will therefore be 100 times (40 dB) greater than its input, which evaluates to 316 mV rms, the input required at the AD636 to balance the loop. Finally, note that unlike most AGC circuits, needing strong temperature-compensation for the internal "kT/q" scaling, these voltages, and thus the output of this measurement system, are temperature stable, arising directly from the fundamental and exact exponential attenuation of the ladder networks in the AD600.

Typical results are presented for a sine wave input at 100 kHz. Figure 20 shows that the output is held very close to the setpoint of 316 mV rms over an input range in excess of 80 dB. (This system can, of course, be used as an AGC amplifier, in which the rms value of the input is leveled.) Figure 21 shows the "decibel" output voltage. More revealing is Figure 22, which shows that the *deviation* from the ideal output predicted by Equation 1 over the input range 80 µV to 500 mV rms is within ±0.5 dB, and within ±1 dB for the 80 dB range from 80 µV to 800 mV. By suitable choice of the input attenuator R1 + R2, this could be centered to cover any range from 25 mV to 250 mV

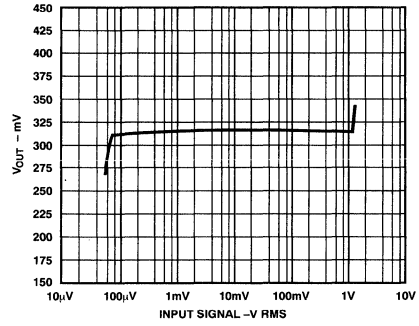


Figure 20. The RMS Output of A2 Is Held Close to the "Setpoint" 316 mV for an Input Range of Over 80 dB

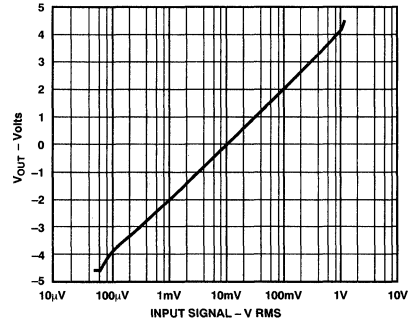


Figure 21. The dB Output of Figure 19's Circuit Is Linear Over an 80 dB Range

to, say, 1 mV to 10 V, with appropriate correction to the value of V_{REF}. (Note that V_{SCALE} is not affected by the changes in the range.) The gain ripple of ±0.2 dB seen in this curve is the result of the finite interpolation error of the X-AMP. Note that it occurs with a periodicity of 12 dB—twice the separation between the tap points (because of the two cascaded stages).

This ripple can be canceled whenever the X-AMP stages are cascaded by introducing a 3 dB offset between the two pairs of control voltages. A simple means to achieve this is shown in Figure 23: the voltages at C1HI and C2HI are "split" by

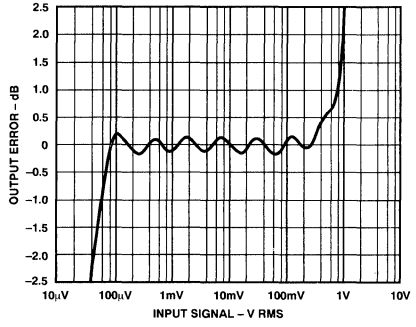


Figure 22. Data from Figure 20 Presented as the Deviation from the Ideal Output Given in Equation 4

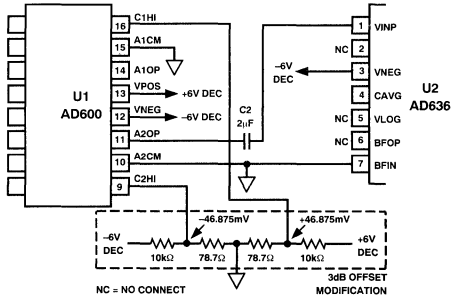


Figure 23. Reducing the Gain Error Ripple

±46.875 mV, or ±1.5 dB. Alternatively, either one of these pins can be individually offset by 3 dB and a 1.5 dB gain adjustment made at the input attenuator (R1 + R2).

The error curve shown in Figure 24 demonstrates that over the central portion of the range the output voltage can be maintained very close to the ideal value. The penalty for this modification is the higher errors at the extremities of the range. The next two applications show how three amplifier sections can be cascaded to extend the nominal conversion range to 120 dB, with the inclusion of simple LP filters of the type shown in Figure 15. Very low errors can then be maintained over a 100 dB range.

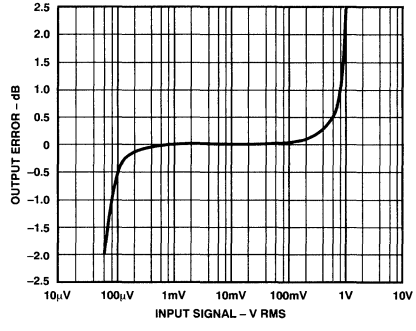


Figure 24. Using the 3 dB Offset Network, the Ripple Is Reduced

100 dB to 120 dB RMS Responding Constant Bandwidth AGC Systems with High Accuracy dB Outputs

The next two applications double as both AGC amplifiers and measurement systems. In both, precise gain offsets are used to achieve either (1) a very high gain linearity of ±0.1 dB over the full 100 dB range, or (2) the optimal signal-to-noise ratio at any gain.

A 100 dB RMS/AGC System with Minimal Gain Error (Parallel Gain with Offset)

Figure 25 shows an rms-responding AGC circuit, which can equally well be used as an accurate measurement system. It accepts inputs of 10 µV to 1 V rms (−100 dBV to 0 dBV) with generous overrange. Figure 26 shows the logarithmic output, V_{LOG}, which is accurately scaled 1 V per decade, that is, 50 mV/dB, with an intercept (V_{LOG} = 0) at 3.16 mV rms (−50 dBV). Gain offsets of ±2 dB have been introduced between the amplifiers, provided by the ±62.5 mV introduced by R6–R9. These offsets cancel a small gain ripple which arises in the X-AMP from its finite interpolation error, which has a period of 18 dB in the individual VCA sections. The gain ripple of all three amplifier sections without this offset (in which case the gain errors simply add) is shown in Figure 27; it is still a remarkably low ±0.25 dB over the 108 dB range from 6 µV to 1.5 V rms. However, with the gain offsets connected, the gain linearity remains under ±0.1 dB over the specified 100 dB range (Figure 28).

The maximum gain of this circuit is 120 dB. If no filtering were used, the noise spectral density of the AD600 (1.4 nV/$\sqrt{\text{Hz}}$) would amount to an input noise of 8.28 µV rms in the full bandwidth (35 MHz). At a gain of one million, the output noise would dominate. Consequently, some reduction of bandwidth is mandatory, and in the circuit of Figure 25 it is due mostly to a single-pole low-pass filter R5/C3, which provides a −3 dB frequency of 458 kHz, which reduces the worst-case output noise (at V_{AGC}) to about 100 mV rms at a gain of 100 dB. Of course, the bandwidth (and hence output noise) could be easily reduced further, for example, in audio applications, merely by increasing C3. The value chosen for this application is optimal in minimizing the error in the V_{LOG} output for small input signals.

The AD600 is dc-coupled, but even miniscule offset voltages at the input would overload the output at high gains, so high-pass filtering is also needed. To provide operation at low frequencies, two simple zeros at about 12 Hz are provided by R1/C1 and R4/C2; op amp sections U3A and U3B (AD713) are used to provide impedance buffering, since the input resistance of the AD600 is only 100 Ω. A further zero at 12 Hz is provided by C4 and the 6.7 kΩ input resistance of the AD636 rms converter.

The rms value of V_{LOG} is generated at Pin 8 of the AD636; the averaging time for this process is determined by C5, and the value shown results in less than 1% rms error at 20 Hz. The slowly varying V_{RMS} is compared with a fixed reference of 316 mV, derived from the positive supply by R10/R11. Any difference between these two voltages is integrated in C6, in conjunction with op amp U3C, the output of which is V_{LOG}. A fraction of this voltage, determined by R12 and R13, is returned to the gain control inputs of all AD600 sections. An increase in V_{LOG} lowers the gain, because this voltage is connected to the inverting polarity control inputs.

Now, in this case, the gains of all three VCA sections are being varied simultaneously, so the scaling is not 32 dB/V but 96 dB/V, or 10.42 mV/dB. The fraction of V_{LOG} required to set its

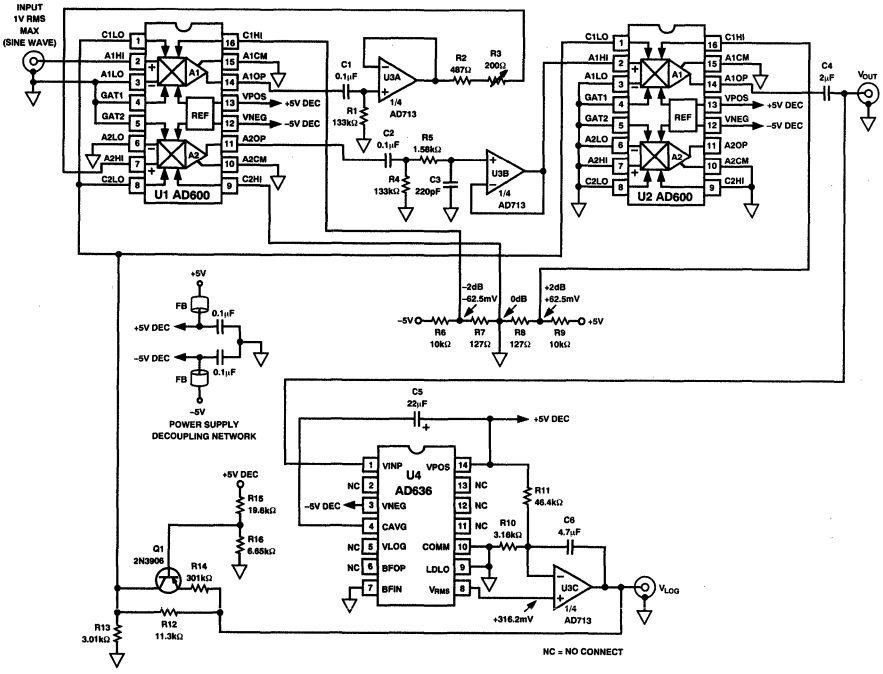


Figure 25. RMS Responding AGC Circuit with 100 dB Dynamic Range

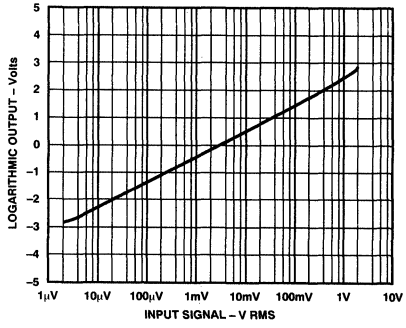


Figure 26. V_{LOG} Plotted vs. V_{IN} for Figure 25's Circuit Showing 120 dB AGC Range

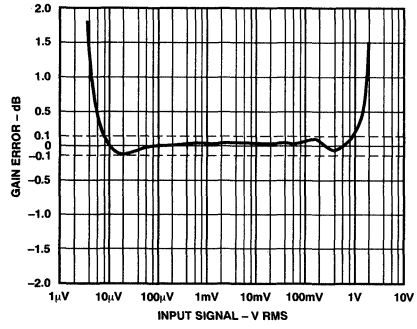


Figure 28. Adding the 2 dB Offsets Improves the Linearization

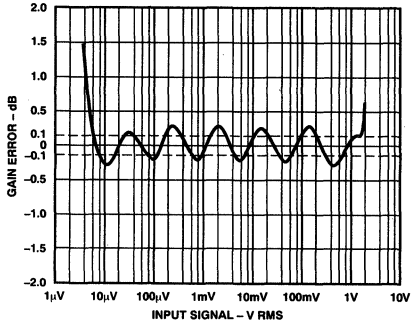


Figure 27. Gain Error for Figure 25 Without the 2 dB Offset Modification

scaling to 50 mV/dB is therefore 10.42/50, or 0.208. The resulting full-scale range of V_{LOG} is nominally ±2.5 V. This scaling was chosen to allow the circuit to operate from ±5 V supplies. Optionally, the scaling could be altered to 100 mV/dB, which would be more easily interpreted when V_{LOG} is displayed on a DVM, by increasing R12 to 25.5 kΩ. The full-scale output of ±5 V then requires the use of supply voltages of at least ±7.5 V.

A simple attenuator of 16.6 ± 1.25 dB is formed by R2/R3 and the 100 Ω input resistance of the AD600. This allows the reference level of the decibel output to be precisely set to zero for an input of 3.16 mV rms, and thus center the 100 dB range between 10 μV and 1 V. In many applications R2/R3 may be replaced by a fixed resistor of 590 Ω. For example, in AGC applications, neither the slope nor the intercept of the logarithmic output is important.

A few additional components (R14–R16 and Q1) improve the accuracy of V_{LOG} at the top end of the signal range (that is, for small gains). The gain starts rolling off when the input to the first amplifier, U1A, reaches 0 dB. To compensate for this nonlinearity, Q1 turns on at $V_{LOG} \sim +1.5$ V and increases the feedback to the control inputs of the AD600s, thereby needing a smaller voltage at V_{LOG} to maintain the input to the AD636 to the setpoint of 316 mV rms.

A 120 dB RMS/AGC System with Optimal S/N Ratio (Sequential Gain)

In the last case, all gains were adjusted simultaneously, resulting in an output signal-to-noise ratio (S/N ratio) which is always less than optimal. The use of sequential gain control results in a major improvement in S/N ratio, with only a slight penalty in the accuracy of V_{LOG}, and no penalty in the stabilization accuracy of V_{AGC}. The idea is simply to increase the gain of the earlier stages first (as the signal level decreases) and thus maintain the highest S/N ratio throughout the amplifier chain. This can be easily achieved with the AD600 because its gain is accurate even when the control input is overdriven; that is, each gain-control "window" of 1.25 V is used fully before moving to the next amplifier to the right.

Figure 29 shows the circuit for the sequential control scheme. R6 to R9 with R16 provide offsets of 42.14 dB between the individual amplifiers to ensure smooth transitions between the gain of each successive X-AMP, with the sequence of gain increase being U1A first, then U1B, and lastly U2A. The adjustable attenuator provided by R3 + R17 and the 100 Ω input resistance of U1A as well as the fixed 6 dB attenuation provided by R2 and the input resistance of U1B are included both to set V_{LOG} to read 0 dB when V_{IN} is 3.16 mV rms and to center the 100 dB range between 10 μV rms and 1 V rms input. R5 and C3 provide a 3 dB noise bandwidth of 30 kHz. R12 to R15 change the scaling from 625 mV/decade at the control inputs to 1 V/decade at the output and at the same time center the dynamic range at 60 dB, which occurs if the V_G of U1B is equal to zero. These arrangements ensure that the V_{LOG} will still fit within the ±6 V supplies.

Figure 30 shows V_{LOG} to be linear over a full 120 dB range. Figure 31 shows the error ripple due to the individual gain functions which is bounded by ±0.2 dB (dotted lines) from 6 μV to 2 V. The small perturbations at about 200 μV and 20 mV, caused by the impracticality of matching the gain functions perfectly, are the only sign that the gains are now sequential. Figure 32 is a plot of V_{AGC} which remains very close to its set value of 316 mV rms over the full 120 dB range.

To more directly compare the signal-to-noise ratios in the "simultaneous" and "sequential" modes of operation, all interstage attenuation was eliminated (R2 and R3 in Figure 25, R2 in Figure 29), the input of U1A was shorted, R5 was selected to provide a 20 kHz bandwidth (R5 = 7.87 kΩ), and only the gain control was varied, using an external source. The rms value of the noise was then measured at V_{OUT} and expressed as an S/N ratio relative to 0 dBV, this being almost the maximum output capability of the AD600. Results for the simultaneous mode can be seen in Figure 33. The S/N ratio degrades uniformly as the gain is increased. Note that since the inverting gain control was used, the gain in this curve and in Figure 34 decreases for more positive values of the gain-control voltage.

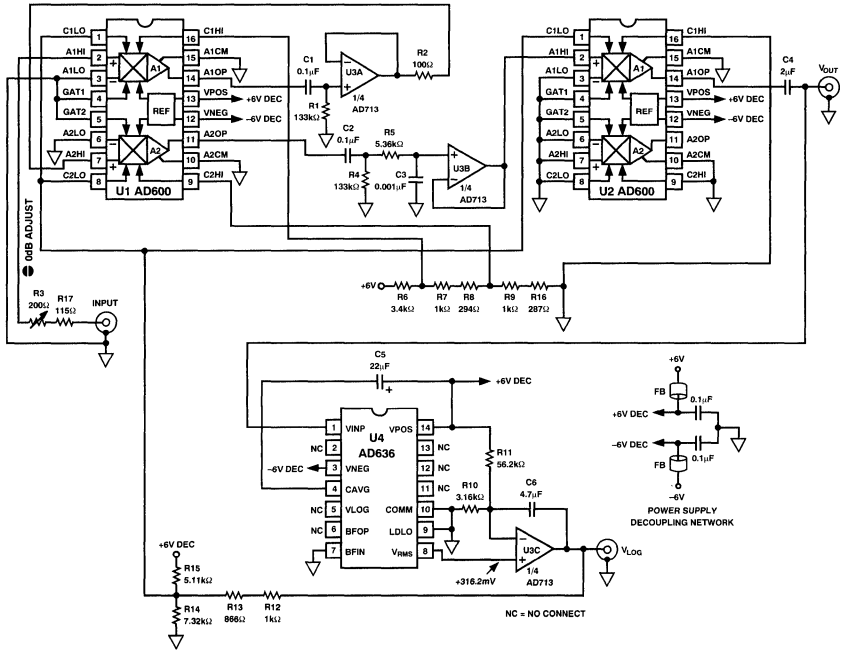


Figure 29. 120 dB Dynamic Range RMS Responding Circuit Optimized for S/N Ratio

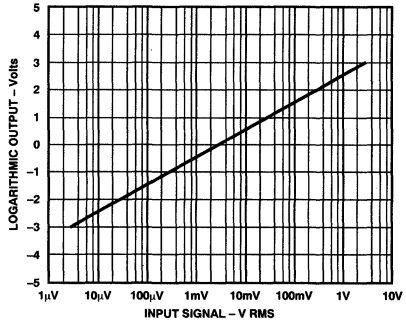


Figure 30. V_{LOG} Is Essentially Linear Over the Full 120 dB Range

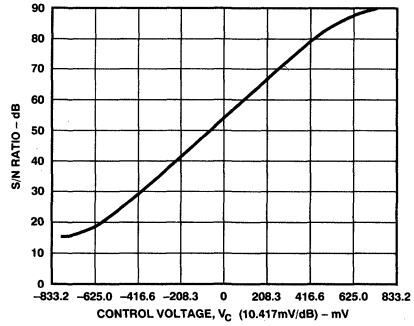


Figure 33. S/N Ratio vs. Control Voltage for Parallel Gain Control (Figure 25)

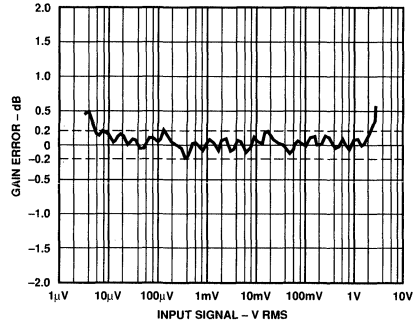


Figure 31. The Error Ripple Due to the Individual Gain Functions

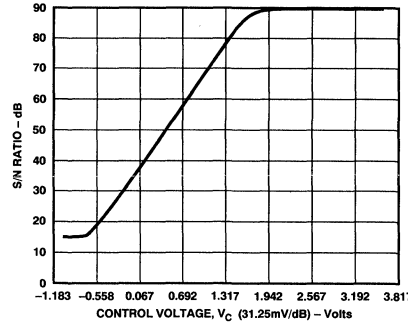


Figure 34. S/N Ratio vs. Control Voltage for Sequential Gain Control (Figure 29)

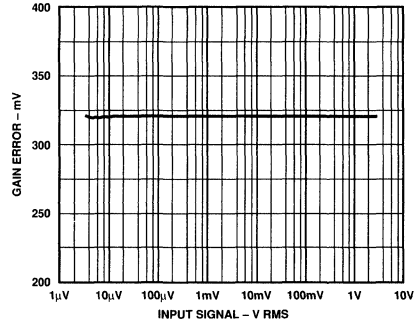


Figure 32. V_{AGC} Remains Close to Its Setpoint Value of 316 mV RMS Over the Full 120 dB Range

In contrast, the S/N ratio for the sequential mode is shown in Figure 34. U1A always acts as a fixed noise source; varying its gain has no influence on the output noise. (This is a feature of the X-AMP technique.) Thus, for the first 40 dB of control range (actually slightly more, as explained below), when only this VCA section has its gain varied, the S/N ratio remains constant. During this time, the gains of U1B and U2A are at their minimum value of −1.07 dB.

For the next 40 dB of control range, the gain of U1A remains fixed at its maximum value of 41.07 dB and only the gain of U1B is varied, while that of U2A remains at its minimum value of −1.07 dB. In this interval, the fixed output noise of U1A is amplified by the increasing gain of U1B and the S/N ratio progressively decreases.

Once U1B reaches its maximum gain of 41.07 dB, its output also becomes a gain independent noise source; this noise is presented to U2A. As the control voltage is further increased, the gains of both U1A and U1B remain fixed at their maximum value of 41.07 dB, and the S/N ratio continues to decrease. Figure 34 clearly shows this, because the maximum S/N ratio of 90 dB is extended for the first 40 dB of input signal before it starts to roll off.

This arrangement of staggered gains can be easily implemented because, when the control inputs of the AD600 are overdriven, the gain limits to its maximum or minimum values without side-effects. This eliminates the need for awkward nonlinear shaping circuits that have previously been used to break up the gain range of multistage AGC amplifiers. It is the precise values of the AD600's maximum and minimum gain (not 0 dB and 40 dB but −1.07 dB and 41.07 dB) that explain the rather odd values of the offset values that are used.

The optimization of the output S/N ratio is of obvious value in AGC systems. However, in applications where these circuit are considered for their wide range logarithmic measurements capabilities, the inevitable degradation of the S/N ratio at high gains need not seriously impair their utility. In fact, the bandwidth of the circuit shown in Figure 25 was specifically chosen so as to improve measurement accuracy by altering the shape of the log error curve (Figure 31) at low signal levels.

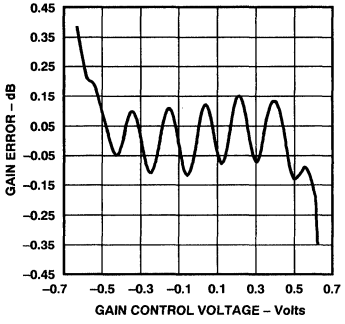


Figure 35. Gain Error vs. Gain Control Voltage

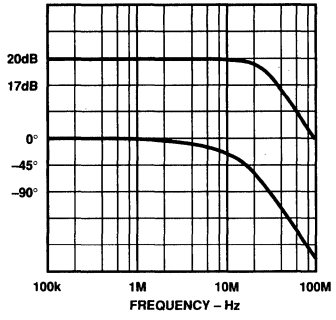


Figure 36. AD600 Frequency and Phase Response vs. Gain

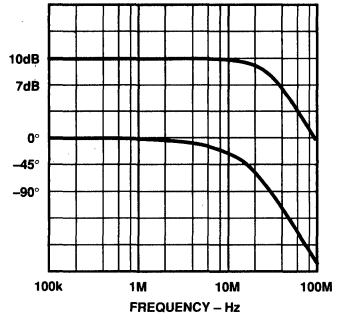


Figure 37. AD602 Frequency and Phase Response vs. Gain

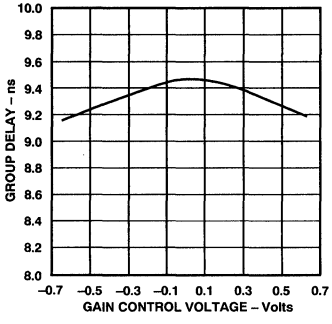


Figure 38. AD600 and AD602 Typical Group Delay vs. V_C

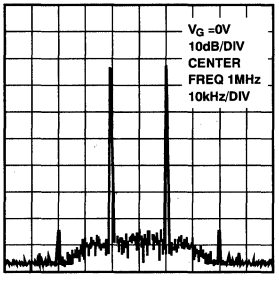


Figure 39. Third Order Intermodulation Distortion, V_{OUT} = 2 V p–p, R_L = 500 Ω

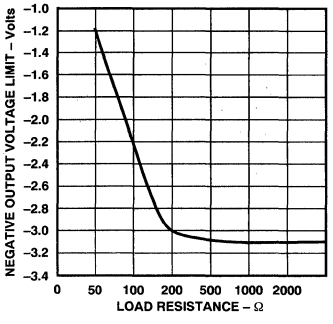


Figure 40. Typical Output Voltage vs. Load Resistance (Negative Output Swing Limits First)

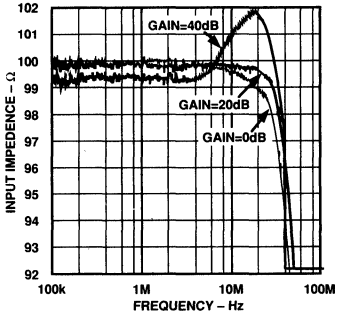


Figure 41. Input Impedance vs. Frequency

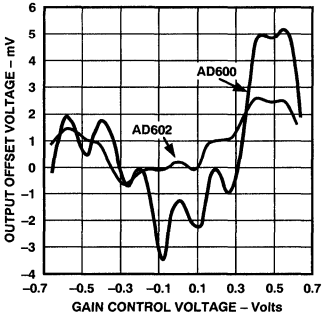


Figure 42. Output Offset vs. Gain Control Voltage (Control Channel Feedthrough)

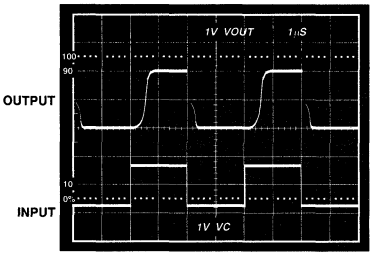


Figure 43. Gain Control Channel Response Time. Top: Output Voltage, 2 V max; Bottom: Gain Control Voltage V_C = ±625 mV

AD600/AD602—Typical Performance Characteristics

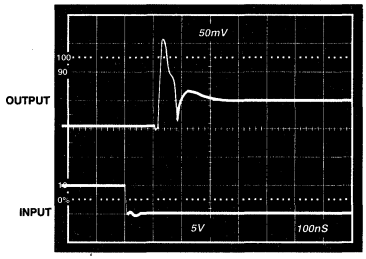


Figure 44. Gating Feedthrough to Output, Gating Off to On

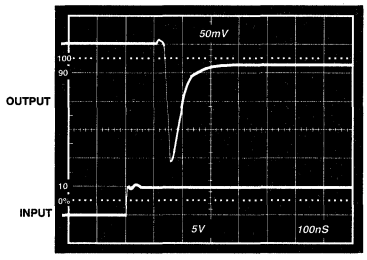


Figure 45. Gating Feedthrough to Output, Gating On to Off

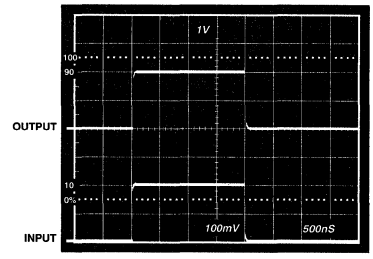


Figure 46. Transient Response, Medium and High Gain

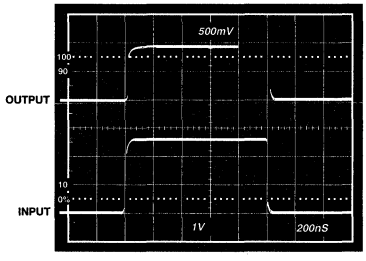


Figure 47. Input Stage Overload Recovery Time

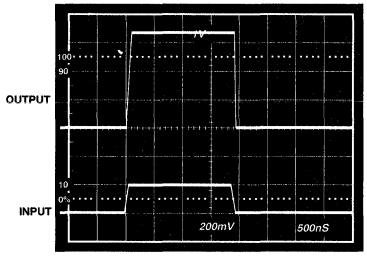


Figure 48. Output Stage Overload Recovery Time

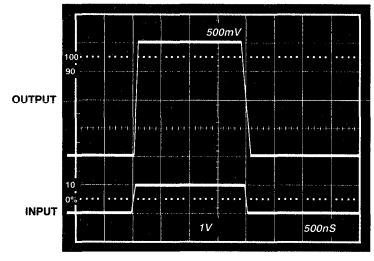


Figure 49. Transient Response Minimum Gain

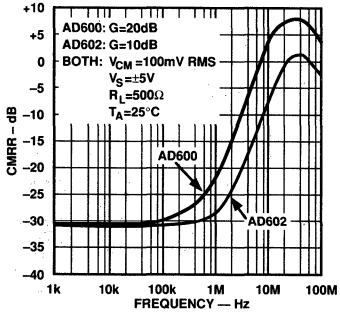


Figure 50. CMRR vs. Frequency

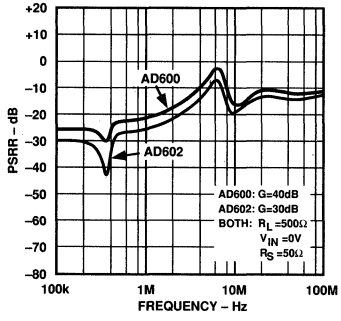


Figure 51. PSRR vs. Frequency

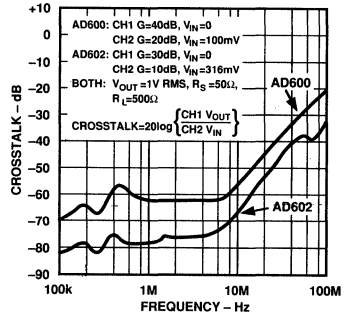


Figure 52. Crosstalk Between A1 and A2 vs. Frequency

50 MHz, 80 dB Demodulating Logarithmic Amplifier with Limiter Output

AD606

FEATURES

Logarithmic Amplifier Performance
- **−75 dBm to +5 dBm Dynamic Range**
- **≤1.5nV/√Hz Input Noise**
- **Usable to ≥50 MHz**
- **37.5 mV/dB Voltage Output**
- **On-Chip Low-Pass Output Filter**

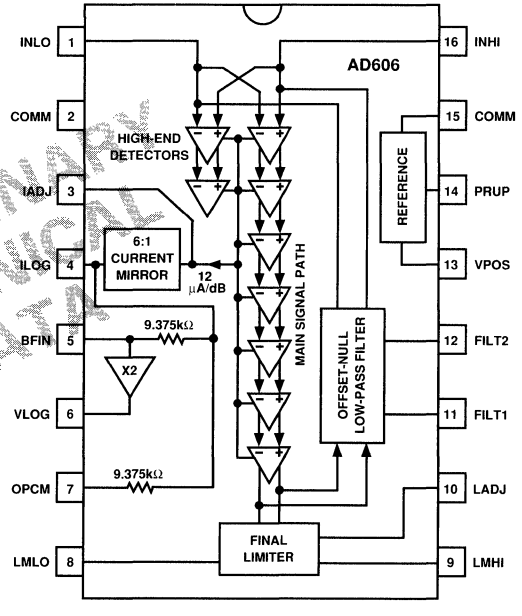
Limiter Performance
- **90 dB Typical Gain**
- **±4° Phase Stability at 45 MHz over 75 dB Range**
- **Adjustable Output Amplitude**

Low Power
- **+5 V Single Supply Operation**
- **65 mW Typical Power Consumption**
- **CMOS Compatible Power-Down to 250 μW typ**
- **<5 μs Enable/Disable Time**

APPLICATIONS

High-Performance Log-IF Strips in Radar
Ultrasound and Sonar Processing
Phase-Stable Limiting Amplifier to 100 MHz
Received Signal Strength Indicator (RSSI)
Wide Range Signal and Power Measurement

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD606 is a complete, monolithic logarithmic amplifier using a 9-stage "successive-detection" technique. It provides both logarithmic and limited outputs. The logarithmic output is from a three-pole post-demodulation low-pass filter and provides a loadable output voltage of +0.1 V to +4 V. The logarithmic scaling is such that the output is +0.5 V for a sinusoidal input of −75 dBm and +3.5 V at an input of +5 dBm; over this range the logarithmic linearity is typically within ±0.5 dB. All scaling parameters are proportional to the supply voltage.

The AD606 can operate above and below these limits, with reduced linearity, to provide as much as 90 dB of conversion range. A second low-pass filter automatically nulls the input offset of the first stage down to the submicrovolt level. Adding external capacitors to both filters allows operation at input frequencies as low as a few hertz.

The AD606's limiter output provides a hard-limited signal output as a differential current of ±1.2 mA from open-collector outputs. In a typical application, both of these outputs are loaded by 200 Ω resistors to provide a voltage gain of more than 90 dB from the input. Transition times are 1.5 ns, and the phase is stable to within ±4° at 45 MHz for signals from −70 dBm to +5 dBm.

The logarithmic amplifier operates from a single +5 V supply and typically consumes 65 mW. It is enabled by a CMOS logic-level voltage input, with a response time of <5 μs. When disabled, the standby power is reduced to <500 μW within 5 μs.

The AD606 is specified for the industrial temperature range of −40°C to +85°C and is available in 16-pin plastic DIPs or SOICs. Consult the factory for other packages and temperature ranges.

AD606—SPECIFICATIONS (T_A = +25°C and Supply = +5 V unless otherwise noted; dBm assumes 50 Ω.)

Model / Parameter	Conditions	AD606 Min	AD606 Typ	AD606 Max	Units
SIGNAL INPUT					
Bandwidth	Differential Sinusoidal Input		50		MHz
Signal Range		−75		+5	dBm
Input Resistance	Differential Input		2.5		kΩ
Input Capacitance	Differential Input		2		pF
SIGNAL OUTPUT					
Gain	With Pin 9 to VPOS via a 200 Ω Resistor and Pin 8 to VPOS via a 200 Ω Resistor	80	90		dB
Output Current	At Pins 8 or 9, Proportional to VPOS	0.96	1.2	1.44	mA
Phase Stability	At 45 MHz for -70 dBm ≤ P_{IN} ≤ +5 dBm		±4		Degrees
RSSI OUTPUT					
Nominal Slope	At 10.7 MHz; 7.5 mV/dB × VPOS		37.5		mV/dB
	At 45 MHz		35		mV/dB
Slope Accuracy	Untrimmed		±10		%
Slope Adjustment Range			±15		%
Intercept	Independent of VPOS		−88.33		dBm
Logarithmic Conformance	50 MHz Sinusoidal Input		±1		dB
Nominal Output	P_{IN} = −75 dBm		0.5		V
	P_{IN} = −35 dBm		2		V
	P_{IN} = +5 dBm		3.5		V
Stability over Temperature	0°C ≤ T_A ≤ +70°C After Calibration at −35 dBm at 45 MHz		±2		dB
Video Response Time				1	µs
POWER-DOWN INTERFACE					
Power-Up Response Time	Time Delay Until Device Meets Full Specifications After HI Transition			3.5	µs
Power-Down Response Time	Time Delay Until Device Powers-Down After LO Transition			5	µs
POWER SUPPLY CURRENT					
Powered Up	Zero Signal Input		13		mA
	T_{MIN} to T_{MAX}		13	25	mA
Powered Down	T_{MIN} to T_{MAX}			150	µA

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

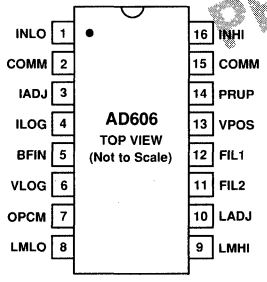
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage $+V_S$ . . . . . +7.5 V
Internal Power Dissipation . . . . . 600 mW
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Soldering 60 sec . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

Thermal Characteristics:
16-Pin Plastic Package: θ_{JA} = 85°C/W
16-Pin SOIC Package: TBD

PIN CONNECTIONS



PIN FUNCTIONS

Pin	Mnemonic	Function
1	INLO	DIFFERENTIAL RF INPUT −75 dBm to +5 dBm, Inverting, AC Coupled.
2	COMM	POWER SUPPLY COMMON Connect to Ground.
3	IADJ	INTERCEPT ADJUST Used to Adjust Intercept Level.
4	ILOG	LOG CURRENT OUTPUT Normally No Connection; 2 μA/dB Output Current.
5	BFIN	BUFFER INPUT Optionally Used to Realize Low Frequency Filters.
6	VLOG	BUFFERED LOG OUTPUT 37.5 mV/dB (100 mV to 4.5 V).
7	OPCM	OUTPUT COMMON Connect to Ground.
8	LMLO	DIFFERENTIAL LIMITER OUTPUT 1.2 mA Full-Scale Output Current Open Collector. Output Must Be "Pulled" Up to VPOS with R ≤ 200 Ω.
9	LMHI	DIFFERENTIAL LIMITER OUTPUT 1.2 mA Full-Scale Output Current. Open Collector Output Must Be "Pulled" Up to VPOS with R ≤ 200 Ω.
10	LADJ	LIMITER LEVEL ADJUSTMENT Used to Adjust Limiter Output Current.
11	FIL1	OFFSET LOOP LOW-PASS FILTER Normally No Connection; a Capacitor Between FIL1 and FIL2 May Be Added to Lower the Filter Cutoff Frequency.
12	FIL2	OFFSET LOOP LOW-PASS FILTER Normally No Connection; A Capacitor Between FIL1 and FIL2 May Be Added to Lower the Filter Cutoff Frequency.
13	VPOS	POSITIVE SUPPLY Connect to +5 V at 13 mA.
14	PRUP	POWER UP CMOS (5 V) Logical High = Device On (≈ 65 mW). CMOS (0 V) Logical Low = Device Off (≈ 250 μW).
15	COMM	POWER SUPPLY COMMON Connect to Ground.
16	INHI	DIFFERENTIAL RF INPUT −75 dBm to +5 dBm, Noninverting, AC Coupled.

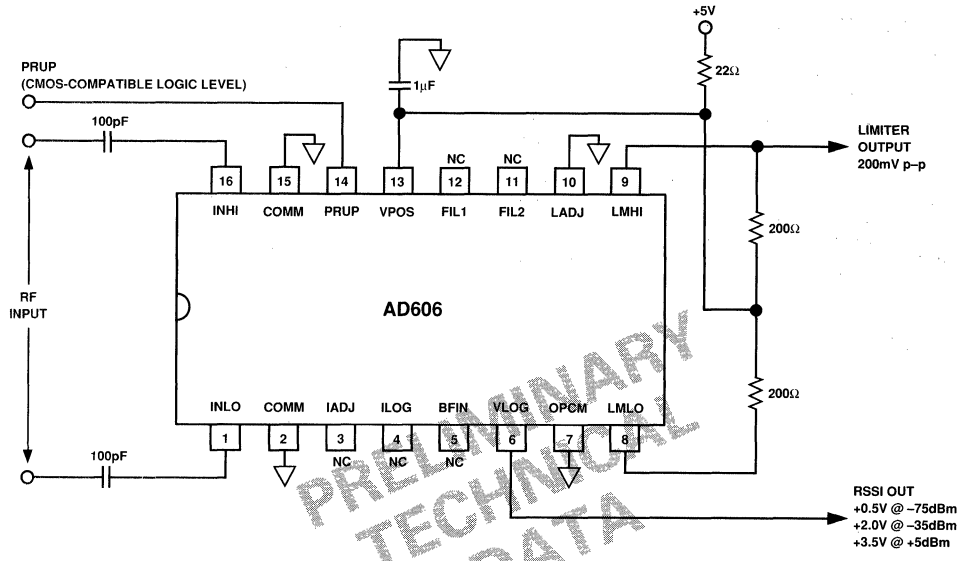


Figure 1. AD606 Typical Application

INPUT LEVEL CONVENTIONS

RF logarithmic amplifiers usually have their input specified in "dBm," meaning "decibels with respect to 1 mW." Unfortunately, this is not precise for several reasons.

1. Log amps respond not to power but to voltage. In this respect, it would be less ambiguous to use "dBV" (decibels with respect to 1 V) as the input metric. Also, power is dependent on the rms (root mean square) value of the signal, which differs with the waveform of the signal.
2. The response of a demodulating log amp depends on the waveform. Convention assumes that the input is sinusoidal. However, the AD606 is capable of accurately handling any input waveform, including dc voltages, pulses and square waves, Gaussian noise, and so on. We will later discuss the effect waveform has on the intercept voltage.
3. The impedance in which the specified power is measured is not always stated. In the log amp context it is invariably assumed to be 50 Ω. Thus, 0 dBm means "1 mW rms in 50 Ω", and thus corresponds to an rms voltage of $\sqrt{(1\text{ mW} \times 50\ \Omega)}$, or 224 mV.

Popular convention requires the use of dBm to simplify the comparison of log amp specifications. Thus, unless otherwise specified, sinusoidal inputs expressed as dBm in 50 Ω are used to specify the performance of the AD606 throughout this data sheet. We will also show the rms voltages where it helps to clarify the specification. Noise levels will likewise be given in dBm; the response to Gaussian noise is 0.5 dB higher than for a sinusoidal input of the same rms value.

Note that dynamic range, being a simple ratio, is always specified simply as "dB," and the slope of the logarithmic transfer function is specified as "mV/dB," NOT as "mV/dBm."

CIRCUIT DESCRIPTION

Figure 2 is a block diagram of the AD606, which is a complete logarithmic amplifier system in monolithic form. It uses a total of nine limiting amplifiers in a "successive detection" scheme to closely approximate a logarithmic response over a total dynamic range of 90 dB. The signal input is differential, at nodes INHI and INLO, and will usually be sinusoidal and ac-coupled. The source may be either differential or single sided; the input impedance is about 2.5 kΩ in parallel with 2 pF. Seven of the amplifier/detector stages handle inputs from −80 dBm (32 μV rms) up to about −14 dBm (45 mV rms). The noise floor is about −88 dBm (9 μV rms). Another two stages receive the input attenuated by 22.3 dB, and respond to inputs up to +10 dBm (707 mV rms). The gain of each of these stages is 11.15 dB and is accurately stabilized over temperature by a precise biasing system.

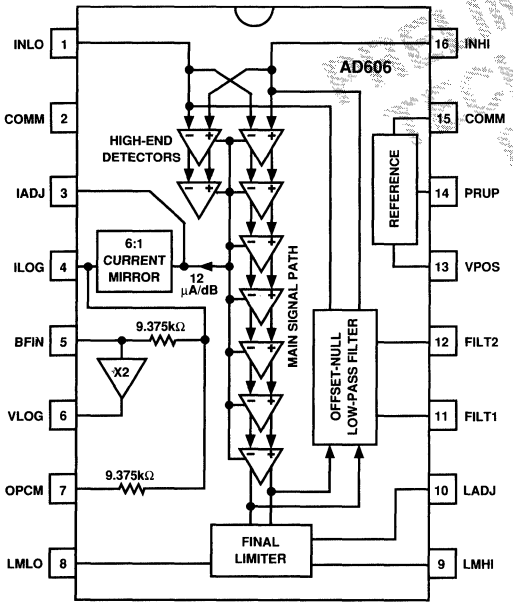


Figure 2. AD606 Functional Block Diagram

The detectors provide full wave rectification of the alternating signal present at each limiter output. Their outputs are in the form of currents, proportional to the supply voltage. Each cell incorporates a low-pass filter pole, as the first step in recovering the average value of the demodulated signal, which contains appreciable energy at even harmonics of the input frequency.

A further real pole can be introduced by adding a capacitor between the summing node IADJ and VPOS. The summed detector output currents are applied to a 6:1 reduction current mirror. Its output at ILOG is scaled 2 μA/dB, and is converted to voltage by an internal load resistor of 9.375 kΩ between ILOG and OPCM (output common, which is usually grounded). The nominal slope at this point is 18.75 mV/dB (375 mV/decade).

A buffer amplifier, having a gain of two, provides a final output scaling at VLOG of 37.5 mV/dB (750 mV/decade). This low-impedance output can run from close to ground to over +4 V (using the recommended +5 V supply) and is tolerant of resistive and capacitive loads. Further filtering is provided by a conjugate pole pair, formed by internal capacitors which are an integral part of the output buffer. The corner frequency of the overall filter is 2 MHz, and the 10%–90% rise time is 150 ns. Later, we will show how the low-pass corner of this three-pole filter can be set to arbitrarily low frequencies, allowing the AD606 to be used at, say, audio frequencies. We will also show how the slope and intercept can be altered using simple external adjustments. The direct buffer input BFIN is used in these cases.

The last limiter output is available as complementary currents from open collectors at pins LMHI and LMLO. These currents are each 1.2 mA ±20% (typical, 1 mA minimum) and may converted to voltages using external load resistors connected to VPOS; typically, a 200 Ω resistor is used on just one output. The voltage gain is then typically over 90 dB, resulting in a hard limited output for all input levels down to the noise floor. The phasing is such that LMHI goes high when the input (INHI to INLO) is positive. The delay time from the signal inputs to the limiter outputs is 8 ns. Of particular importance is the phase stability of these outputs versus input level. For example, at 50 MHz, the phase typically remains within ±4° from −70 dBm to +5 dBm. The rise time of this output (essentially a square wave) is about 1.2 ns, resulting in clean operation up to 100 MHz.

The AD606 can be used in an intermittent mode in order to reduce power consumption in portable applications. When powered down, the quiescent current is typically 50 μA, or about 250 μW. A CMOS logical HIGH applied to PRUP activates both internal references, and the system becomes fully functional (that is, meets its specifications) within about 3.5 μs. When this input is a CMOS logical LOW, the system shuts down to the quiescent level within about 5 μs. The input resistance from PRUP to COMM is typically 250 kΩ. In applications where VLOG is taken to an A/D converter which allows the use of an external reference, this reference input should also be connected to the same +5 V supply. The power supply voltage may be in the range +4 V to +6 V, providing a range of slopes from nominally 30 mV/dB (600 mV/decade) to 45 mV/dB (900 mV/decade).

Low Frequency Operation

Since all the amplifier stages are internally dc-coupled, the AD606 does not impose any limits on the lowest frequencies which may be handled. It is simply necessary to use larger input coupling capacitors and add external capacitors to the low-pass post demodulation filter. However, an unavoidable consequence of the use of dc coupling between the stages, and the very high overall gain, is that even very small offset voltages at the input will seriously degrade the accuracy for small ac inputs. The built-in offset is held to very low levels by the use of careful design, but a residual of typically 100 μV may remain. This is dealt with by the inclusion of an offset correction loop, which samples the offset at the output of the main amplifier chain and servos the input to null the offset. This requires a low-pass filter, the main components of which are also included in the AD606.

A real pole at 16 kHz is formed by internal resistors of 330 kΩ and capacitors of 30 pF. This time constant, whose effective value is reduced by the loop gain of about 70 dB, can be increased by the addition of an external capacitor between nodes FIL1 and FIL2. The overall response is transformed to a two-pole high pass, in conjunction with the input coupling capacitors.

For operation above 30 MHz, it is not necessary to add the external capacitor, although an improvement in low frequency noise can be achieved by so doing. Note that the offset control loop does not materially affect the low-frequency cutoff at high input levels when the offset voltage is swamped by the signal.

Note that the AD606 does not use trimming in production to achieve its accurate performance, but relies on the very close matching of similar elements which can be achieved in a monolithic circuit. However, the absolute values of the resistors and capacitors are subject to some process variability, which needs to be accounted for in some applications. This topic is addressed in the Applications section. In this connection, note that the scaling of internal currents referred to above is not absolute.

DC Coupled Demodulating 120MHz Logarithmic Amplifier

AD640

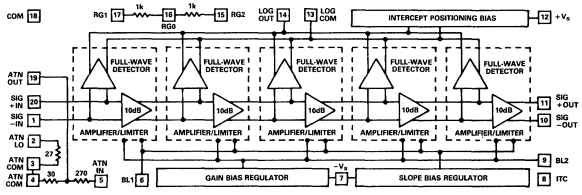
FEATURES

Complete, Fully Calibrated Monolithic System
Five Stages, Each Having 10dB Gain, 350MHz BW
Direct Coupled Fully Differential Signal Path
Logarithmic Slope, Intercept and AC Response are Stable Over Full Military Temperature Range
Dual Polarity Current Outputs Scaled 1mA/Decade
Voltage Slope Options (1V/Decade, 100mV/dB, etc.)
Low Power Operation (Typically 220mW at ±5V)
Low Cost Plastic Packages Also Available

APPLICATIONS

Radar, Sonar, Ultrasonic and Audio Systems
Precision Instrumentation from DC to 120MHz
Power Measurement with Absolute Calibration
Wide Range High Accuracy Signal Compression
Alternative to Discrete and Hybrid IF Strips
Replaces Several Discrete Log Amp ICs

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD640 is a complete monolithic logarithmic amplifier. A single AD640 provides up to 50dB of dynamic range for frequencies from dc to 120MHz. Two AD640s in cascade can provide up to 95dB of dynamic range at reduced bandwidth. The AD640 uses a successive detection scheme to provide an output current proportional to the logarithm of the input voltage. It is laser calibrated to close tolerances and maintains high accuracy over the full military temperature range using supply voltages from ±4.5V to ±7.5V.

The AD640 comprises five cascaded dc coupled amplifier/limiter stages, each having a small signal voltage gain of 10dB and a −3dB bandwidth of 350MHz. Each stage has an associated full-wave detector, whose output current depends on the absolute value of its input voltage. The five outputs are summed to provide the video output (when low pass filtered) scaled at 1mA per decade (50μA per dB). On chip resistors can be used to convert this output current to a voltage with several convenient slope options. A balanced signal output at +50dB (referred to input) is provided to operate AD640s in cascade.

The logarithmic response is absolutely calibrated to within ±1dB for dc or square wave inputs from ±0.75mV to ±200mV, with an intercept (logarithmic offset) at 1mV dc. An integral X10 attenuator provides an alternative input range of ±7.5mV to ±2V dc. Scaling is also guaranteed for sinusoidal inputs.

The AD640B is specified for the industrial temperature range of −40°C to +85°C and the AD640T, available processed to MIL-STD-883B, for the military range of −55°C to +125°C. Both are available in 20-pin side brazed ceramic DIPs or leadless chip carriers (LCC). The AD640J is specified for the commercial temperature range of 0 to +70°C, and is available in both 20-pin plastic DIP (N) and PLCC (P) packages.

This device is now available to Standard Military Drawing (DESC) number 5962-9095501MRA and 5962-9095501M2A.

PRODUCT HIGHLIGHTS

1. Absolute calibration of a wideband logarithmic amplifier is unique. The AD640 is a high accuracy measurement device, not simply a logarithmic building block.
2. Advanced design results in unprecedented stability over the full military temperature range.
3. The fully differential signal path greatly reduces the risk of instability due to inadequate power supply decoupling and shared ground connections, a serious problem with commonly used unbalanced designs.
4. Differential interfaces also ensure that the appropriate ground connection can be chosen for each signal port. They further increase versatility and simplify applications. The signal input impedance is ~500kΩ in shunt with ~2pF.
5. The dc coupled signal path eliminates the need for numerous interstage coupling capacitors and simplifies logarithmic conversion of subsonic signals.
6. The low input offset voltage of 50μV (200μV max) ensures good accuracy for low level dc inputs.
7. Thermal recovery "tails," which can obscure the response when a small signal immediately follows a high level input, have been minimized by special attention to design details.
8. The noise spectral density of $2nV/\sqrt{Hz}$ results in a noise floor of ~23μV rms (−80dBm) at a bandwidth of 100MHz. The dynamic range using cascaded AD640s can be extended to 95dB by the inclusion of a simple filter between the two devices.

AD640—SPECIFICATIONS

DC SPECIFICATIONS (V_S = ±5V, T_A = +25°C, unless otherwise noted)

Model		AD640J			AD640B			AD640T			
Transfer Function[1]		$I_{OUT}=I_Y$ LOG $\lvert V_{IN}/V_X\rvert$ for V_{IN}=±0.75mV to ±200mV dc									
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
SIGNAL INPUTS (Pins 1, 20)											
Input Resistance	Differential		500			500			500		kΩ
Input Offset Voltage	Differential		50	**500**		50	**200**		50	**200**	μV
vs. Temperature			0.8			0.8			0.8		μV/°C
Over Temperature	T_{min} to T_{max}									**300**	μV
vs. Supply			2			2			2		μV/V
Input Bias Current			7	25		7	25		7	25	μA
Input Bias Offset			1			1			1		μA
Common Mode Range		−2		+0.3	−2		+0.3	−2		+0.3	V
INPUT ATTENUATOR (Pins 2, 3, 4, 5 & 19)											
Attenuation[2]	Pin 5 to Pin 19		20			20			20		dB
Input Resistance	Pins 5 to 3/4		300			300			300		Ω
SIGNAL OUTPUT (Pins 10, 11)											
Small Signal Gain[4]			50			50			50		dB
Peak Differential Output[5]			±180			±180			±180		mV
Output Resistance	Either Pin to COM		75			75			75		Ω
Quiescent Output Voltage	Either Pin to COM		−90			−90			−90		mV
LOGARITHMIC OUTPUT[6] (Pin 14)											
Voltage Compliance Range		−0.3		$+V_S-1$	−0.3		$+V_S-1$	−0.3		$+V_S-1$	V
Slope Current, I_Y		**0.95**	1.00	**1.05**	**0.98**	1.00	**1.02**	**0.98**	1.00	**1.02**	mA
Accuracy vs. Temperature			0.002			0.002			0.002		%/°C
	T_{min} to T_{max}							**0.98**		**1.02**	mA
Accuracy vs. Supply	$\pm V_S$=4.5V to 7.5V		0.08	**1.0**		0.08	**0.4**		0.08	**0.4**	%/V
Intercept Voltage[7], V_X		**0.85**	1.00	**1.15**	**0.95**	1.00	**1.05**	**0.95**	1.00	**1.05**	mV
vs. Temperature			0.5			0.5			0.5		μV/°C
Over Temperature	T_{min} to T_{max}							**0.90**		**1.10**	mV
vs. Supply	$\pm V_S$=4.5V to 7.5V		2			2			2		μV/V
Logarithmic Offset (Alt. Definition of V_X)		−61.5	−60.0	−58.7	−60.5	−60.0	−59.5	−60.5	−60.0	−59.5	dBV
vs. Temperature			0.004			0.004			0.004		dB/°C
Over Temperature	T_{min} to T_{max}							−60.9		−59.1	dB
vs. Supply	$\pm V_S$=4.5V to 7.5V		0.017			0.017			0.017		dB/V
Intercept Voltage Using Attenuator		**8.25**	10.0	**11.75**	**9.0**	10.0	**11.0**	**9.0**	10.0	**11.0**	mV
Zero Signal Output Current[3]			−0.2			−0.2			−0.2		mA
ITC Disabled	Pin 8 to COM		−0.27			−0.27			−0.27		mA
Maximum Output Current			2.3			2.3			2.3		mA
APPLICATIONS RESISTORS (Pins 15, 16, 17)			1.000		**0.995**	1.000	**1.005**	**0.995**	1.000	**1.005**	kΩ
DC LINEARITY V_{IN}=±1mV to ±100mV			0.35	**1.2**		0.35	**0.6**		0.35	**0.6**	dB
TOTAL ABSOLUTE DC ACCURACY											
V_{IN}=±1mV to ±100mV[8]			0.55	**2**		0.55	**0.9**		0.55	**0.9**	dB
Over Temperature	T_{min} to T_{max}			3			**1.7**			**1.8**	dB
Over Supply Range	$\pm V_S$=4.5V to 7.5V			**2**			**1.0**			**1.0**	dB
V_{IN}=±0.75mV to ±200mV Using Attenuator			1.0	**3**		1.0	**2.0**		1.0	**2.0**	dB
V_{IN}=±10mV to ±1V			0.4	**2.5**		0.4	**1.5**		0.4	**1.5**	dB
Over Temperature	T_{min} to T_{max}		0.6	3		0.6	**2.0**		0.6	**2.0**	dB
V_{IN}=±7.5mV to 2V			1.2	**3.5**		1.2	**2.5**		1.2	**2.5**	dB
POWER REQUIREMENTS											
Voltage Supply Range		**±4.5**		**±7.5**	**±4.5**		**±7.5**	**±4.5**		**±7.5**	V
Quiescent Current[9]											
$+V_S$ (Pin 12)	T_{min} to T_{max}		9	15		9	**15**		9	**15**	mA
$-V_S$ (Pin 7)	T_{min} to T_{max}		35	60		35	**60**		35	**60**	mA

AC SPECIFICATIONS (V_S = ±5V, T_A = +25°C, unless otherwise noted)

Model / Parameter	Conditions	AD640J Min	AD640J Typ	AD640J Max	AD640B Min	AD640B Typ	AD640B Max	AD640T Min	AD640T Typ	AD640T Max	Units
SIGNAL INPUT (Pins 1, 20)											
Input Capacitance	Either Pin to COM		2			2			2		pF
Noise Spectral Density	1kHz to 10MHz		2			2			2		nV/√Hz
Tangential Sensitivity	BW=100MHz		−72			−72			−72		dBm
3dB BANDWIDTH											
Each Stage			350			350			350		MHz
All Five Stages	Pins 1 & 20 to 10 & 11		145			145			145		MHz
LOGARITHMIC OUTPUTS[6]											
Slope Current, I_Y											
f<=1MHz		0.96	1.0	1.04	0.98	1.0	1.02	0.98	1.0	1.02	mA
f=30MHz		0.88	0.94	1.00	0.91	0.94	0.97	0.91	0.94	0.97	mA
f=60MHz		0.82	0.90	0.98	0.86	0.90	0.94	0.86	0.90	0.94	mA
f=90MHz			0.88			0.88			0.88		mA
f=120MHz			0.85			0.85			0.85		mA
Intercept, Dual AD640s[10, 11]											
f<=1MHz		−90.6	−88.6	−86.6	−89.6	−88.6	−87.6	−89.6	−88.6	−87.6	dBm
f=30MHz			−87.6			−87.6			−87.6		dBm
f=60MHz			−86.3			−86.3			−86.3		dBm
f=90MHz			−83.9			−83.9			−83.9		dBm
f=120MHz			−80.3			−80.3			−80.3		dBm
AC LINEARITY											
−40dBm to −2dBm[12]	f=1MHz		0.5	2.0		0.5	1.0		0.5	1.0	dB
−35dBm to −10dBm[12]	f=1MHz		0.25	1.0		0.25	0.5		0.25	0.5	dB
−75dBm to 0dBm[10]	f=1MHz		0.75	3.0		0.75	1.5		0.75	1.5	dB
−70dBm to −10dBm[10]	f=1MHz		0.5	2.0		0.5	1.0		0.5	1.0	dB
−75dBm to +15dBm[13]	f=10kHz		0.5	3.0		0.5	1.5		0.5	1.5	dB
PACKAGE OPTION[14]											
20-Pin Ceramic DIP Package (D)						AD640BD			AD640TD		
20-Pin Leadless Ceramic Chip Carrier (E)						AD640BE			AD640TE		
20-Pin Plastic DIP Package (N)			AD640JN								
20-Pin Plastic Leadless Chip Carrier (P)			AD640JP			AD640BP					
NUMBER OF TRANSISTORS			155			155			155		

NOTES

[1]Logarithms to base 10 are used throughout. The response is independent of the sign of V_{IN}.

[2]Attenuation ratio trimmed to calibrate intercept to 10mV when in use. It has a temperature coefficient of +0.3%/°C.

[3]The zero-signal current is a function of temperature unless internal temperature compensation (ITC) pin is grounded.

[4]Overall gain is trimmed using a ±200μV square wave at 2kHz, corrected for the onset of compression.

[5]The fully limited signal output will appear to be a square wave; its amplitude is proportional to absolute temperature.

[6]Currents defined as flowing *into* Pin 14. See FUNDAMENTALS OF LOGARITHMIC CONVERSION for full explanation of scaling concepts. Slope is measured by linear regression over central region of transfer function.

[7]The logarithmic intercept in dBV (decibels relative to 1V) is defined as 20 LOG_{10} (V_X/1V).

[8]Operating in circuit of Figure 24 using ±0.1% accurate values for R_{LA} and R_{LB}. Includes slope and nonlinearity errors. Input offset errors also included for V_{IN} >3mV dc, and over the full input range in ac applications.

[9]Essentially independent of supply voltages.

[10]Using the circuit of Figure 27, using cascaded AD640s and offset nulling. Input is sinusoidal, 0dBm in 50Ω=223mV rms.

[11]For a sinusoidal signal (see EFFECT OF WAVEFORM ON INTERCEPT). Pin 8 on second AD640 must be grounded to ensure temperature stability of intercept for dual AD640 system.

[12]Using the circuit of Figure 24, using single AD640 and offset nulling. Input is sinusoidal, 0dBm in 50Ω=223mV rms.

[13]Using the circuit of Figure 32, using cascaded AD640s and attenuator. Square wave input.

[14]For outline information see Package Information section.

All min and max specifications are guaranteed, but only those in **boldface** are 100% tested on all production units. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

THERMAL CHARACTERISTICS

	θ_{JC} (°C/W)	θ_{JA} (°C/W)
20-Pin Ceramic DIP Package (D-20)	25	85
20-Pin Leadless Ceramic Chip Carrier (E-20A)	25	85
20-Pin Plastic DIP Package (N-20)	24	61
20-Pin Plastic Leadless Chip Carrier (P-20A)	28	75

ABSOLUTE MAXIMUM RATINGS*

Supply Voltages . . . . . ±7.5V
Input Voltage (Pin 1 or Pin 20 to COM) . . . . −3V to +300mV
Attenuator Input Voltage (Pin 5 to Pin 3/4) . . . . . ±4V
Storage Temperature Range D, E . . . . . −65°C to +150°C
Storage Temperature Range N, P . . . . . −65°C to +125°C
Ambient Temperature Range, Rated Performance
Industrial, AD640B . . . . . −40°C to +85°C
Military, AD640T . . . . . −55°C to +125°C
Commercial, AD640J . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

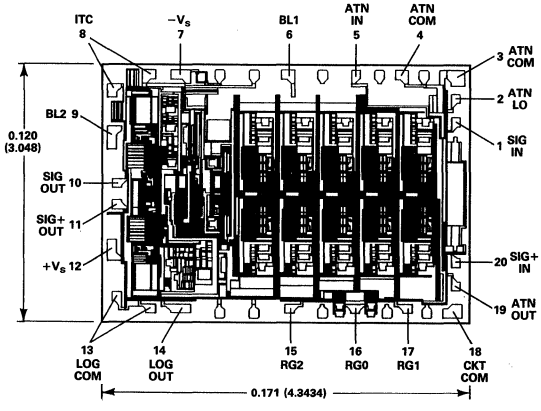
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description
AD640JN	0°C to +70°C	Plastic DIP
AD640JP	0°C to +70°C	Plastic Leaded Chip Carrier
AD640BD	−40°C to +85°C	Side Brazed Ceramic DIP
AD640BE	−40°C to +85°C	Ceramic Leadless Chip Carrier
AD640BP	−40°C to +85°C	Plastic Leaded Chip Carrier
AD640TD/883B 5962-9095501MRA	−55°C to +125°C	Side Brazed Ceramic DIP
AD640TE/883B 5962-9095501M2A	−55°C to +125°C	Ceramic Leadless Chip Carrier
AD640TCHIP	−55°C to +125°C	Chip

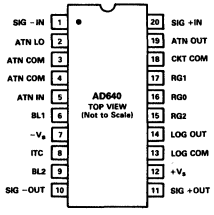
CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).

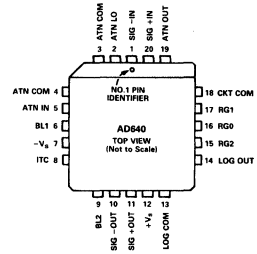


CONNECTION DIAGRAMS

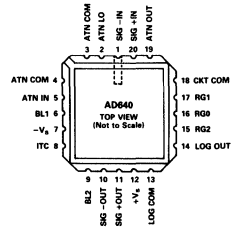
20-Pin Ceramic DIP (D) Package
20-Pin Plastic (DIP (N) Package



20-Pin PLCC (P) Package



20-Pin LCC (E) Package



Typical Performance (DC: Figures 1–9, AC: Figures 10–15)

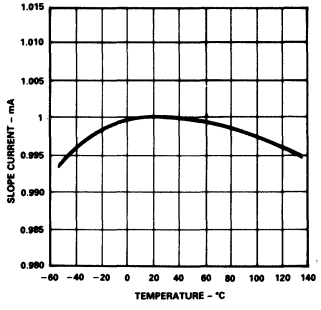


Figure 1. Slope Current, I_Y vs. Temperature

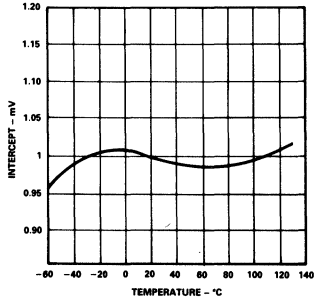


Figure 2. Intercept Voltage, V_X, vs. Temperature

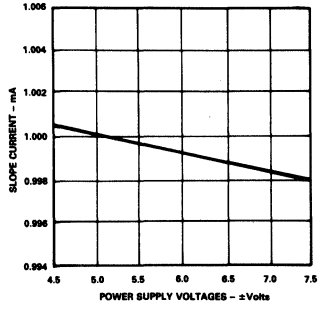


Figure 3. Slope Current, I_Y vs. Supply Voltages

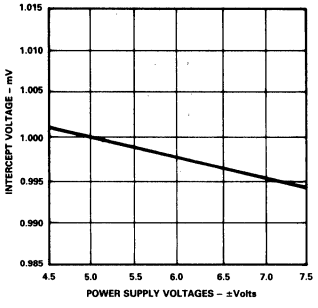


Figure 4. Intercept Voltage, V_X, vs. Supply Voltages

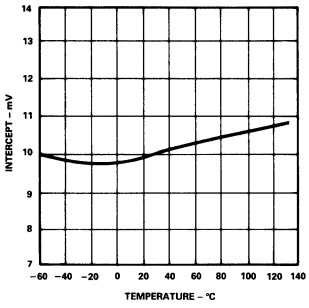


Figure 5. Intercept Voltage (Using Attenuator) vs. Temperature

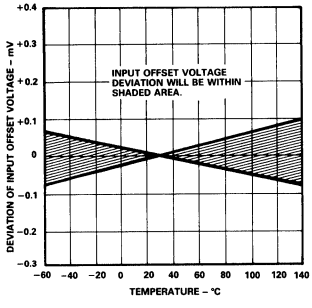


Figure 6. Input Offset Voltage Deviation vs. Temperature

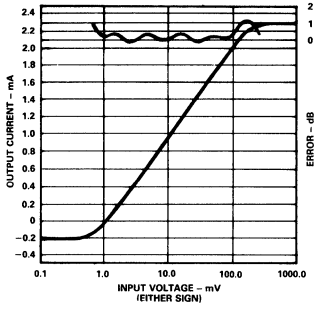


Figure 7. DC Logarithmic Transfer Function and Error Curve for Single AD640

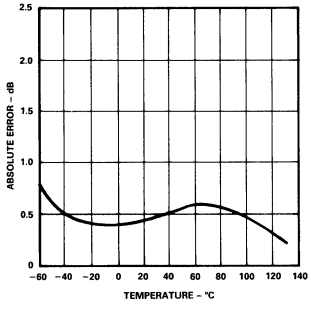


Figure 8. Absolute Error vs. Temperature, V_{IN} = ±1 mV to ±100 mV

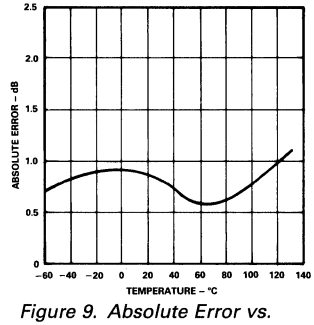


Figure 9. Absolute Error vs. Temperature, Using Attenuator. V_{In} = ±10mV to ±1 V, Pin 8 Grounded to Disable ITC Bias

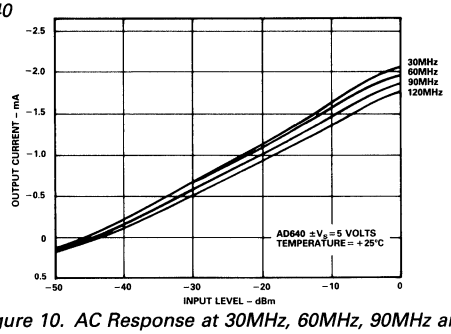


Figure 10. AC Response at 30MHz, 60MHz, 90MHz and 120MHz, vs. dBm Input (Sinusoidal Input)

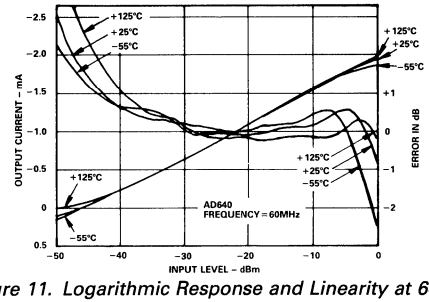


Figure 11. Logarithmic Response and Linearity at 60MHz, T_A for T_A = −55°C, +25°C, +125°C

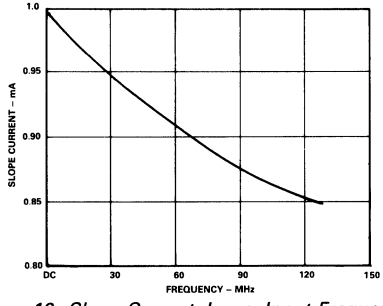


Figure 12. Slope Current, I_Y, vs. Input Frequency

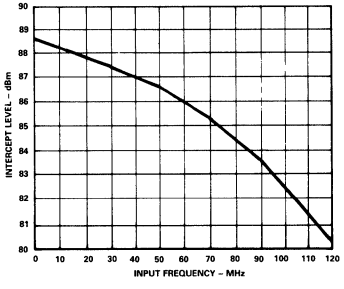


Figure 13. Intercept Level (dBm) vs. Frequency (Cascaded AD640s – Sinusoidal Input)

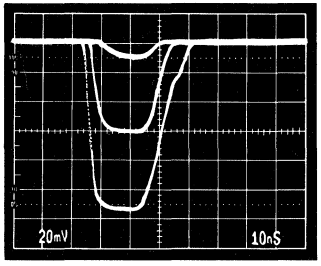


Figure 14. Baseband Pulse Response of Single AD640, Inputs of 1mV, 10mV and 100mV

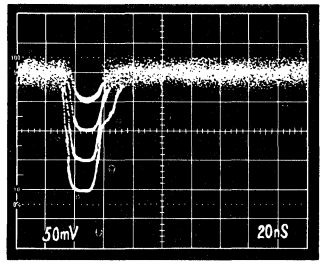


Figure 15. Baseband Pulse Response of Cascaded AD640s, at Inputs of 0.2mV, 2mV, 20mV and 200mV

CIRCUIT DESCRIPTION

The AD640 uses five cascaded limiting amplifiers to approximate a logarithmic response to an input signal of wide dynamic range and wide bandwidth. This type of logarithmic amplifier has traditionally been assembled from several small scale ICs and numerous external components. The performance of these semidiscrete circuits is often unsatisfactory. In particular, the logarithmic slope and intercept (see FUNDAMENTALS OF LOGARITHMIC CONVERSION) are usually not very stable in the presence of supply and temperature variations even after laborious and expensive individual calibration. The AD640 employs high precision analog circuit techniques to ensure stability of scaling over wide variations in supply voltage and temperature. Laser trimming, using ac stimuli and operating conditions similar to those encountered in practice, provides fully calibrated logarithmic conversion.

Each of the amplifier/limiter stages in the AD640 has a small signal voltage gain of 10dB (×3.162) and a −3dB bandwidth of 350MHz. Fully differential direct coupling is used throughout. This eliminates the many interstage coupling capacitors usually required in ac applications, and simplifies low frequency signal processing, for example, in audio and sonar systems. The AD640 is intended for use in demodulating applications. Each stage incorporates a detector (a full wave transconductance rectifier) whose output current depends on the absolute value of its input voltage.

Figure 16 is a simplified schematic of one stage of the AD640. All transistors in the basic cell operate at near zero collector to base voltage and low bias currents, resulting in low levels of thermally induced distortion. These arise when power shifts from one set of transistors to another during large input signals. Rapid recovery is essential when a small signal immediately follows a large one. This low power operation also contributes significantly to the excellent long term calibration stability of the AD640.

The complete AD640, shown in Figure 17, includes two bias regulators. One determines the small signal gain of the amplifier stages; the other determines the logarithmic slope. These bias regulators maintain a high degree of stability in the resulting function by compensating for potentially large uncertainties in transistor parameters, temperature and supply voltages. A third biasing block is used to accurately control the logarithmic intercept.

By summing the signals at the output of the detectors, a good approximation to a logarithmic transfer function can be achieved. The lower the stage gain, the more accurate the approximation, but more stages are then needed to cover a given dynamic range. The choice of 10dB results in a theoretical periodic deviation or ripple in the transfer function of ±0.15dB from the ideal response when the input is either a dc voltage or a square wave. The *slope* of the transfer function is unaffected by the input waveform; however, the intercept and rip-

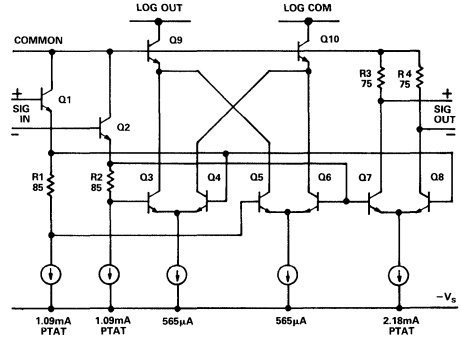


Figure 16. Simplified Schematic of a Single AD640 Stage

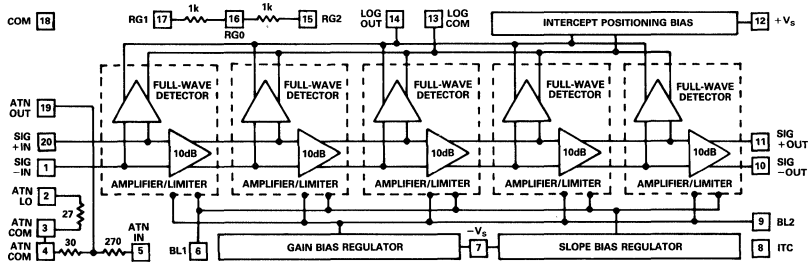


Figure 17. Block Diagram of the Complete AD640

ple are waveform dependent (see EFFECT OF WAVEFORM ON INTERCEPT). The input will usually be an amplitude modulated sinusoidal carrier. In these circumstances the output is a fluctuating current at *twice* the carrier frequency (because of the full wave detection) whose average value is extracted by an external low pass filter, which recovers a logarithmic measure of the baseband signal.

Circuit Operation

With reference to Figure 16, the transconductance pair Q7, Q8 and load resistors R3 and R4 form a limiting amplifier having a small signal gain of 10dB, set by the tail current of nominally 2.18mA at 27°C. This current is basically proportional to absolute temperature (PTAT) but includes additional current to compensate for finite beta and junction resistance. The limiting output voltage is ±180mV at 27°C and is PTAT. Emitter followers Q1 and Q2 raise the input resistance of the stage, provide level shifting to introduce collector bias for the gain stage and detectors, reduce offset drift by forming a thermally balanced quad with Q7 and Q8 and generate the detector biasing across resistors R1 and R2.

Transistors Q3 through Q6 form the full wave detector, whose output is buffered by the cascodes Q9 and Q10. For zero input Q3 and Q5 conduct only a small amount (a total of about 32μA) of the 565μA tail currents supplied to pairs Q3–Q4 and Q5–Q6. This "pedestal" current flows in output cascode Q9 to the LOG OUT node (Pin 14). When driven to the peak output of the preceding stage, Q3 or Q5 (depending on signal polarity) conducts most of the tail current, and the output rises to 532μA. The LOG OUT current has thus changed by 500μA as the input has changed from zero to its maximum value. Since the detectors are spaced at 10dB intervals, the output increases by 50μA/dB, or 1mA per decade. This scaling parameter is trimmed to absolute accuracy using a 2kHz square wave. At frequencies near the system bandwidth, the slope is reduced due to the reduced output of the limiter stages, but it is still relatively insensitive to temperature variations so that a simple external slope adjustment can restore scaling accuracy.

The intercept position bias generator (Figure 17) removes the pedestal current from the summed detector outputs. It is adjusted during manufacture such that the output (flowing into Pin 14) is 1mA when a 2kHz square-wave input of exactly ±10mV is applied to the AD640. This places the dc intercept at precisely 1mV. The LOG COM output (Pin 13) is the complement of LOG OUT. It also has a 1mV intercept, but with an inverted slope of −1mA/decade. Because its pedestal is very large (equivalent to about 100dB), its intercept voltage is not guaranteed. The intercept positioning currents include a special internal temperature compensation (ITC) term which can be disabled by connecting Pin 8 to ground.

The logarithmic function of the AD640 is absolutely calibrated to within ±0.3dB (or ±15μA) for 2kHz square-wave inputs of ±1mV to ±100mV, and to within ±1dB between ±750μV and ±200mV. Figure 18 is a typical plot of the dc transfer function, showing the outputs at temperatures of −55°C, +25°C and +125°C. While the slope and intercept are seen to be little affected by temperature, there is a lateral shift in the end points of the "linear" region of the transfer function, which reduces the effective dynamic range. The cause of this shift is explained in FUNDAMENTALS OF LOGARITHMIC CONVERSION.

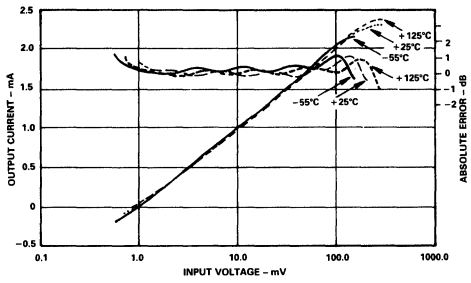


Figure 18. Logarithmic Output and Absolute Error vs. DC or Square Wave Input at T_A = −55°C, +25°C, Input Direct to Pins 1 and 20

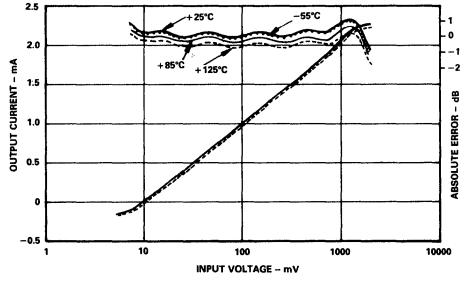


Figure 19. Logarithmic Output and Absolute Error vs. DC or Square Wave Input at T_A = −55°C, +25°C, +85°C and +125°C. Input via On-Chip Attenuator

The on chip attenuator can be used to handle input levels 20dB higher, that is, from ±7.5mV to ±2V for dc or square wave inputs. It is specially designed to have a positive temperature coefficient and is trimmed to position the intercept at 10mV dc (or −24dBm for a sinusoidal input) over the full temperature range. When using the attenuator the internal bias compensation should be disabled by grounding Pin 8. Figure 19 shows the output at −55°C, +25°C, +85°C and +125°C for a single AD640 with the attenuator in use; the curves overlap almost perfectly, and the lateral shift in the transfer function does not occur. Therefore, the full dynamic range is available at all temperatures.

The output of the final limiter is available in differential form at Pins 10 and 11. The output impedance is 75Ω to ground from either pin. For most input levels, this output will appear to have roughly a square waveform. The signal path may be extended using these outputs (see OPERATION OF CASCADED AD640s). The logarithmic outputs from two or more AD640s can be directly summed with full accuracy.

A pair of 1kΩ applications resistors, RG1 and RG2 (Figure 17) are accessed via Pins 15, 16 and 17. These can be used to convert an output current to a voltage, with a slope of 1V/decade (using one resistor), 2V/decade (both resistors in series) or 0.5V/decade (both in parallel). Using all the resistors from two AD640s (for example, in a cascaded configuration) ten slope options from 0.25V to 4V/decade are available.

FUNDAMENTALS OF LOGARITHMIC CONVERSION

The conversion of a signal to its equivalent logarithmic value involves a *nonlinear* operation, the consequences of which can be very confusing if not fully understood. It is important to realize from the outset that many of the familiar concepts of linear circuits are of little relevance in this context. For example, the incremental gain of an ideal logarithmic converter approaches *infinity* as the input approaches zero. Further, an offset at the output of a linear amplifier is simply equivalent to an offset at the input, while in a logarithmic converter it is equivalent to a change of *amplitude* at the input – a very different relationship.

We assume a dc signal in the following discussion to simplify the concepts; ac behavior and the effect of input waveform on calibration are discussed later. A logarithmic converter having a voltage input V_{IN} and output V_{OUT} must satisfy a transfer function of the form

$$V_{OUT} = V_Y \text{ LOG } (V_{IN}/V_X) \qquad \text{Equation (1)}$$

where V_Y and V_X are fixed voltages which determine the *scaling* of the converter. The input is *divided* by a voltage because the argument of a logarithm has to be a simple ratio. The logarithm must be *multiplied* by a voltage to develop a voltage output. These operations are not, of course, carried out by explicit computational elements, but are inherent in the behavior of the converter. For stable operation, V_X and V_Y must be based on sound design criteria and rendered stable over wide temperature and supply voltage extremes. This aspect of RF logarithmic amplifier design has traditionally received little attention.

When $V_{IN} = V_X$, the logarithm is zero. V_X is, therefore, called the *Intercept Voltage*, because a graph of V_{OUT} versus LOG (V_{IN}) – ideally a straight line – crosses the horizontal axis at this point (see Figure 20). For the AD640, V_X is calibrated to exactly 1mV. The slope of the line is directly proportional to V_Y. Base 10 logarithms are used in this context to simplify the relationship to decibel values. For $V_{IN} = 10V_X$, the logarithm has a value of 1, so the output voltage is V_Y. At $V_{IN} = 100V_X$, the output is $2V_Y$, and so on. V_Y can therefore be viewed either as the *Slope Voltage* or as the *Volts per Decade Factor*.

The AD640 conforms to Equation (1) except that its two outputs are in the form of currents, rather than voltages:

$$I_{OUT} = I_Y \text{ LOG } (V_{IN}/V_X) \qquad \text{Equation (2)}$$

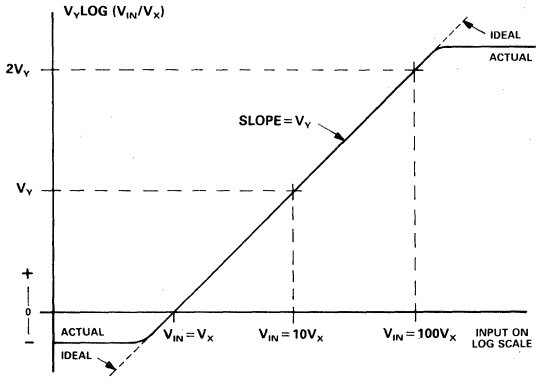


Figure 20. Basic DC Transfer Function of the AD640

I_Y, the *Slope Current*, is 1mA. The current output can readily be converted to a voltage with a slope of 1V/decade, for example, using one of the 1kΩ resistors provided for this purpose, in conjunction with an op amp, as shown in Figure 21.

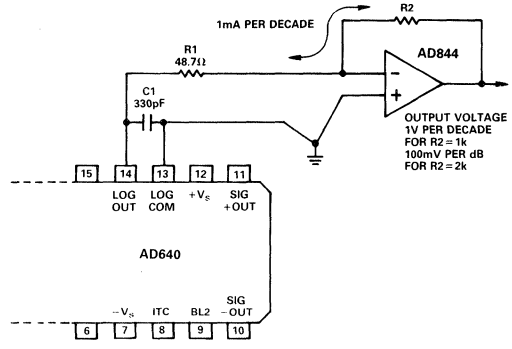


Figure 21. Using an External Op Amp to Convert the AD640 Output Current to a Buffered Voltage Output

Intercept Stabilization

Internally, the intercept voltage is a fraction of the thermal voltage kT/q, that is, $V_X = V_{XO}T/T_O$, where V_{XO} is the value of V_X at a reference temperature T_O. So the uncorrected transfer function has the form

$$I_{OUT} = I_Y \text{ LOG } (V_{IN} \, T_O/V_{XO}T) \qquad \text{Equation (3)}$$

Now, if the amplitude of the signal input V_{IN} could somehow be rendered PTAT, the intercept would be stable with temperature, since the temperature dependence in both the numerator and denominator of the logarithmic argument would cancel. This is what is *actually* achieved by interposing the on-chip attenuator, which has the necessary temperature dependence to cause the input to the first stage to vary in proportion to absolute temperature. *The end limits of the dynamic range are now totally independent of temperature.* Consequently, this is the preferred method of intercept stabilization for applications where the input signal is sufficiently large.

When the attenuator is *not* used, the PTAT variation in V_X will result in the intercept being temperature dependent. Near 300K (27°C) it will vary by 20LOG (301/300) dB/°C, about 0.03dB/°C. Unless corrected, the whole output function would drift up or down by this amount with changes in temperature. In the AD640 a temperature compensating current I_YLOG(T/T_O) is added to the output. This effectively maintains a constant intercept V_{XO}. This correction is active in the default state (Pin 8 open circuited). When using the attenuator, Pin 8 should be grounded, which disables the compensation current. The drift term needs to be compensated only once; when the outputs of two AD640s are summed, Pin 8 should be grounded on at least one of the two devices (both if the attenuator is used).

Conversion Range

Practical logarithmic converters have an upper and lower limit on the input, beyond which errors increase rapidly. The upper limit occurs when the *first* stage in the chain is driven into limiting. Above this, no further increase in the output can occur and the transfer function flattens off. The lower limit arises because a finite number of stages provide finite gain, and therefore at low signal levels the system becomes a simple linear amplifier.

Note that this lower limit is *not* determined by the intercept voltage, V_X; it can occur either above or below V_X, depending on the design. When using two AD640s in cascade, input offset voltage and wideband noise are the major limitations to low level accuracy. Offset can be eliminated in various ways. Noise can only be reduced by lowering the system bandwidth, using a filter between the two devices.

EFFECT OF WAVEFORM ON INTERCEPT

The absolute value response of the AD640 allows inputs of either polarity to be accepted. Thus, the logarithmic output in response to an amplitude-symmetric square wave is a steady value. For a sinusoidal input the fluctuating output current will usually be low pass filtered to extract the baseband signal. The unfiltered output is at *twice* the carrier frequency, simplifying the design of this filter when the video bandwidth must be maximized. The averaged output depends on waveform in a roughly analogous way to waveform dependence of rms value. The effect is to change the apparent intercept voltage. The intercept voltage appears to be doubled for a sinusoidal input, that is, the averaged output in response to a sine wave of *amplitude* (not rms value) of 20mV would be the same as for a dc or square wave input of 10mV. Other waveforms will result in different intercept factors. An amplitude-symmetric-rectangular waveform has the same intercept as a dc input, while the average of a baseband unipolar pulse can be determined by multiplying the response to a dc input of the same amplitude by the duty cycle. It is important to understand that in responding to pulsed RF signals it is the waveform of the *carrier* (usually sinusoidal) *not* the modulation envelope, that determines the effective intercept voltage. Table I shows the effective intercept and resulting decibel offset for commonly occurring waveforms. The input waveform does *not* affect the slope of the transfer function. Figure 22 shows the *absolute* deviation from the ideal response of cascaded AD640s for three common waveforms at input levels from −80dBV to −10dBV. The measured sine wave and triwave responses are 6dB and 8.7dB, respectively, below the square wave response – in agreement with theory.

Input Waveform	Peak or rms	Intercept Factor	Error (Relative to a dc Input)
Square Wave	Either	1	0.00dB
Sine Wave	Peak	2	−6.02dB
Sine Wave	rms	$1.414(\sqrt{2})$	−3.01dB
Triwave	Peak	2.718 (e)	−8.68dB
Triwave	rms	$1.569\ (e/\sqrt{3})$	−3.91dB
Gaussian Noise	rms	1.887	−5.52dB

Table I

Logarithmic Conformance and Waveform

The waveform also affects the ripple, or *periodic* deviation from an ideal logarithmic response. The ripple is greatest for dc or square wave inputs because every value of the input voltage maps to a single location on the transfer function and thus traces out the full nonlinearities in the logarithmic response.

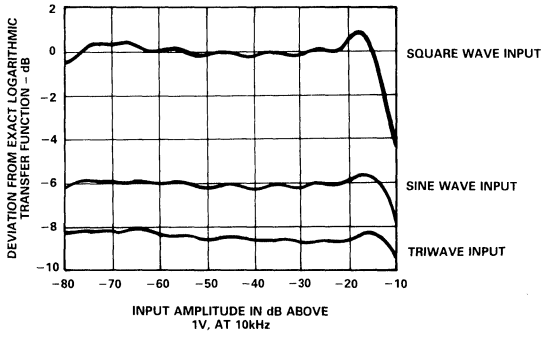


Figure 22. Deviation from Exact Logarithmic Transfer Function for Two Cascaded AD640s, Showing Effect of Waveform on Calibration and Linearity

By contrast, a general time varying signal has a continuum of values within each cycle of its waveform. The averaged output is thereby "smoothed" because the periodic deviations away from the ideal response, as the waveform "sweeps over" the transfer function, tend to cancel. This smoothing effect is greatest for a triwave input, as demonstrated in Figure 22.

The accuracy at *low signal inputs* is also waveform dependent. The detectors are not perfect absolute value circuits, having a sharp "corner" near zero; in fact they become parabolic at low levels and behave as if there were a dead zone. Consequently, the output tends to be higher than ideal. When there are enough stages in the system, as when two AD640s are connected in cascade, most detectors will be adequately loaded due to the high overall gain, but a single AD640 does not have sufficient gain to maintain high accuracy for low level sine wave or triwave inputs. Figure 23 shows the absolute deviation from calibration for the same three waveforms for a single AD640. For inputs between −10dBV and −40dBV the vertical displacement of the traces for the various waveforms remains in agreement with the predicted dependence, but significant calibration errors arise at low signal levels.

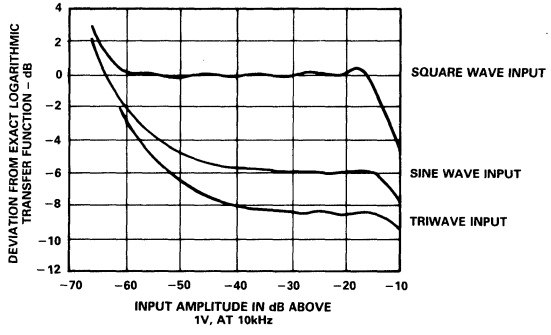


Figure 23. Deviation from Exact Logarithmic Transfer Function for a Single AD640; Compare Low Level Response with That of Figure 22

SIGNAL MAGNITUDE

The AD640 is a *calibrated* device. It is, therefore, important to be clear in specifying the signal magnitude under all waveform conditions. For dc or square wave inputs there is, of course, no ambiguity. Bounded periodic signals, such as sinusoids and triwaves, can be specified in terms of their simple *amplitude* (peak value) or alternatively by their *rms value* (which is a measure of *power when the impedance is specified*). It is generally better to define this type of signal in terms of its amplitude because the AD640 response is a consequence of the input *voltage*, not power. However, provided that the appropriate value of intercept for a specific waveform is observed, rms measures may be used. Random waveforms can only be specified in terms of rms value because their peak value may be unbounded, as is the case for Gaussian noise. These must be treated on a case-by-case basis. The effective intercept given in Table I should be used for Gaussian noise inputs.

On the other hand, for bounded signals the amplitude can be expressed either in volts or dBV (decibels relative to 1V). For example, a sine wave or triwave of 1mV amplitude can also be defined as an input of −60dBV, one of 100mV amplitude as −20dBV, and so on. RMS value is usually expressed in dBm (decibels above 1mW) for a specified impedance level. *Throughout this data sheet we assume a 50Ω environment, the customary impedance level for high speed systems, when referring to signal powers in dBm.* Bearing in mind the above discussion of the effect of waveform on the intercept calibration of the AD640, it will be apparent that a sine wave at a power of, say, −10dBm will *not* produce the same output as a triwave or square wave of the same *power*. Thus, a sine wave at a power level of −10dBm has an rms value of 70.7mV or an amplitude of 100mV (that is, $\sqrt{2}$ times as large, the ratio of amplitude to rms value for a sine wave), while a triwave of the same power has an amplitude which is $\sqrt{3}$ or 1.73 times its rms value, or 122.5mV.

"Intercept" and "Logarithmic Offset"

If the signals are expressed in dBV, we can write the output current in a simpler form, as

$$I_{OUT} = 50\mu A\ (Input_{dBV} - X_{dBV}) \qquad \text{Equation (4)}$$

where $Input_{dBV}$ is the input voltage *amplitude* (not rms) in dBV and X_{dBV} is the appropriate value of the intercept (for a given waveform) in dBV. This form shows more clearly why the intercept is often referred to as the *logarithmic offset*. For dc or square wave inputs, V_X is 1mV so the numerical value of X_{dBV} is −60, and Equation (4) becomes

$$I_{OUT} = 50\mu A\ (Input_{dBV} + 60) \qquad \text{Equation (5)}$$

Alternatively, for a sinusoidal input measured in dBm (power in dB above 1mW in a 50Ω system) the output can be written

$$I_{OUT} = 50\mu A\ (Input_{dBm} + 44) \qquad \text{Equation (6)}$$

because the intercept for a sine wave expressed in volts rms is at 1.414mV (from Table I) or −44dBm.

OPERATION OF A SINGLE AD640

Figure 24 shows the basic connections for a single device, using 100Ω load resistors. Output A is a negative going voltage with a slope of −100mV per decade; output B is positive going with a slope of +100mV per decade. For applications where absolute calibration of the intercept is essential, the main output (from LOG OUT, Pin 14) should be used; the LOG COM output can then be grounded. To evaluate the demodulation response, a simple low pass output filter having a time constant of roughly 500μs (3dB corner of 320Hz) is provided by a 4.7μF (−20% +80%) ceramic capacitor (Erie type RPE117-Z5U-475-K50V) placed across the load. A DVM may be used to measure the averaged output in verification tests. The voltage compliance at Pins 13 and 14 extends from 0.3V below ground up to 1V below $+V_S$. Since the current into Pin 14 is from −0.2mA at zero signal to +2.3mA when fully limited (dc input of >300mV) the output never drops below −230mV. On the other hand, the current *out* of Pin 13 ranges from −0.2mA to +2.3mA, and if desired, a load resistor of up to 2kΩ can be used on this output; the slope would then be 2V per decade. Use of the LOG COM output in this way provides a numerically correct decibel reading on a DVM (+100mV=+1.00dB).

Board layout is very important. The AD640 has both high gain and wide bandwidth; therefore every signal path must be very carefully considered. A high quality ground plane is essential, but it should not be assumed that it behaves as an equipotential plane. Even though the application may only call for modest bandwidth, each of the three differential signal interface pairs (SIG IN, Pins 1 and 20, SIG OUT, Pins 10 and 11, and LOG, Pins 13 and 14) must have their own "starred" ground points to avoid oscillation at low signal levels (where the gain is highest).

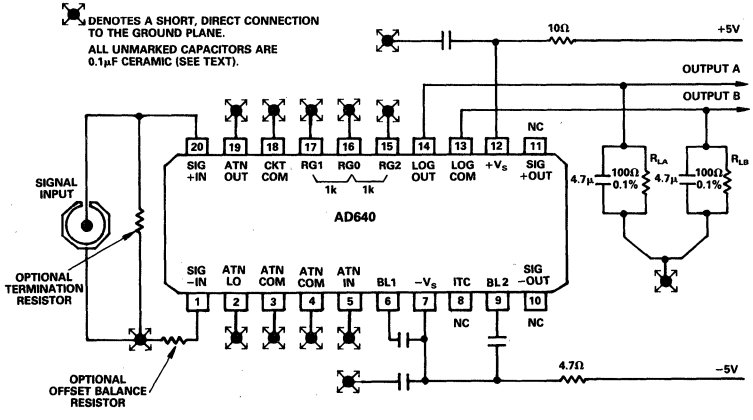


Figure 24. Connections for a Single AD640 to Verify Basic Performance

Unused pins (excluding Pins 8, 10 and 11) such as the attenuator and applications resistors should be grounded close to the package edge. BL1 (Pin 6) and BL2 (Pin 9) are internal bias lines a volt or two above the $-V_S$ node; access is provided solely for the addition of decoupling capacitors, which should be connected exactly as shown (not all of them connect to the ground). Use low impedance ceramic 0.1μF capacitors (for example, Erie RPE113-Z5U-105-K50V). Ferrite beads may be used instead of supply decoupling resistors in cases where the supply voltage is low.

Active Current-to-Voltage Conversion

The compliance at LOG OUT limits the available output voltage swing. The output of the AD640 may be converted to a larger, buffered output voltage by the addition of an operational amplifier connected as a current-to-voltage (transresistance) stage, as shown in Figure 21. Using a 2kΩ feedback resistor (R2) the 50μA/dB output at LOG OUT is converted to a voltage having a slope of +100mV/dB, that is, 2V per decade. This output ranges from roughly −0.4V for zero signal inputs to the AD640, crosses zero at a dc input of precisely +1mV (or −1mV) and is +4V for a dc input of 100mV. A passive prefilter, formed by R1 and C1, minimizes the high frequency energy conveyed to the op amp. The corner frequency is here shown as 10MHz. The AD844 is recommended for this application because of its excellent performance in transresistance modes. Its bandwidth of 35MHz (with the 2kΩ feedback resistor) will exceed the baseband response of the system in most applications. For lower bandwidth applications other op amps and multipole active filters may be substituted (see, for example, Figure 32 in the APPLICATIONS section).

Effect of Frequency on Calibration

The slope and intercept of the AD640 are calibrated during manufacture using a 2kHz square wave input. Calibration depends on the gain of each stage being 10dB. When the input frequency is an appreciable fraction of the 350MHz bandwidth of the amplifier stages, their gain becomes imprecise and the logarithmic slope and intercept are no longer fully calibrated. However, the AD640 can provide very stable operation at frequencies up to about one half the 3dB frequency of the amplifier stages. Figure 10 shows the averaged output current versus input level at 30MHz, 60MHz, 90MHz and 120MHz. Figure 11 shows the absolute error in the response at 60MHz and at temperatures of −55°C, +25°C and +125°C. Figure 12 shows the variation in the slope current, and Figure 13 shows the variation in the intercept level (sinusoidal input) versus frequency.

If absolute calibration is essential, or some other value of slope or intercept is required, there will usually be some point in the user's system at which an adjustment may be easily introduced. For example, the 5% slope deficit at 30MHz (see Figure 12) may be restored by a 5% increase in the value of the load resistor in the passive loading scheme shown in Figure 24, or by inserting a trim potentiometer of 100Ω in series with the feedback resistor in the scheme shown in Figure 21. The intercept can be adjusted by adding or subtracting a small current to the output. Since the slope current is 1mA/decade, a 50μA increment will move the intercept by 1dB. Note that any error in this current will invalidate the calibration of the AD640. For example, if one of the the 5V supplies were used with a resistor to generate the current to reposition the intercept by 20dB, a ±10% variation in this supply will cause a ±2dB error in the absolute calibration. Of course, slope calibration is unaffected.

Source Resistance and Input Offset

The bias currents at the signal inputs (Pins 1 and 20) are typically 7μA. These flow in the source resistances and generate input offset voltages which may limit the dynamic range because the AD640 is direct coupled and an offset is indistinguishable from a signal. It is good practice to keep the source resistances as low as possible and to equalize the resistance seen at each input. For example, if the source resistance to Pin 20 is 100Ω, a compensating resistor of 100Ω should be placed in series with Pin 1. The residual offset is then due to the *bias current offset*, which is typically under 1μA, causing an extra offset uncertainty of 100μV in this example. For a single AD640 this will rarely be troublesome, but in some applications it may need to be nulled out, along with the internal voltage offset component. This may be achieved by adding an adjustable voltage of up to ±250μV at the unused input. (Pins 1 and 20 may be interchanged with no change in function.)

In most applications there will be no need to use any offset adjustment. However, a general offset trimming circuit is shown in Figure 25. R_S is the source resistance of the signal. *Note: 50Ω rf sources may include a blocking capacitor and have no dc path to ground, or may be transformer coupled and have a near zero resistance to ground.* Determine whether the source resistance is zero, 25Ω or 50Ω (with the generator terminated in 50Ω) to find the correct value of bias compensating resistor, R_B, which should optimally be equal to R_S, unless $R_S = 0$, in which case use $R_B = 5\Omega$. The value of Ros should be set to $20{,}000R_B$ to provide a ±250μV trim range. To null the offset, set the source voltage to zero and use a DVM to observe the logarithmic output voltage. Recall that the LOG OUT current of the AD640 exhibits an *absolute value response* to the input voltage, so the offset potentiometer is adjusted to the point where the logarithmic output "turns around" (reaches a local maximum or minimum).

At high frequencies it may be desirable to insert a coupling capacitor and use a choke between Pin 20 and ground, when Pin 1 should be taken directly to ground. Alternatively, transformer coupling may be used. In these cases, there is no added offset due to bias currents. When using two dc coupled AD640s (overall gain 100,000), it is impractical to maintain a sufficiently low offset voltage using a manual nulling scheme. The section CASCADED OPERATION explains how the offset can be automatically nulled to submicrovolt levels by the use of a negative feedback network.

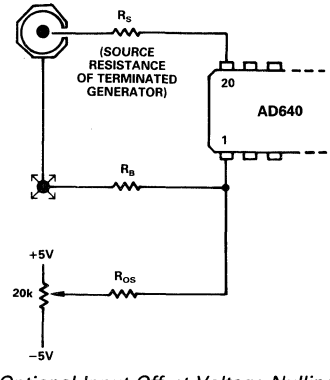


Figure 25. Optional Input Offset Voltage Nulling Circuit; See Text for Component Values

Using Higher Supply Voltages

The AD640 is calibrated using ±5V supplies. Scaling is very insensitive to the supply voltages (see dc SPECIFICATIONS) and higher supply voltages will not directly cause significant errors. However, the AD640 power dissipation must be kept below 500mW in the interest of reliability and long term stability. When using well regulated supply voltages above ±6V, the decoupling resistors shown in the application schematics can be increased to maintain ±5V at the IC. The resistor values are calculated using the specified maximum of 15mA current into the $+V_S$ terminal (Pin 12) and a maximum of 60mA into the $-V_S$ terminal (Pin 7). For example, when using ±9V supplies, a resistor of (9V-5V)/15mA, about 261Ω, should be included in the $+V_S$ lead to each AD640, and (9V–5V)/60mA, about 64.9Ω, in each $-V_S$ lead. Of course, asymmetric supplies may be dealt with in a similar way.

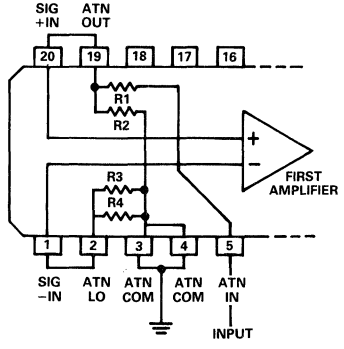


Figure 26. Details of the Input Attenuator

Using the Attenuator

In applications where the signal amplitude is sufficient, the on-chip attenuator should be used because it provides a temperature independent dynamic range (compare Figures 18 and 19). Figure 26 shows this attenuator in more detail. R1 is a thin film resistor of nominally 270Ω and low temperature coefficient (TC). It is trimmed to calibrate the intercept to 10mV dc (or −24dBm for sinusoidal inputs), that is, to an attenuation of nominally 20dBs at 27°C. R2 has a nominal value of 30Ω and has a high positive TC, such that the overall attenuation factor is 0.33%/°C at 27°C. This results in a transmission factor that is proportional to absolute temperature, or PTAT. (See Intercept Stabilization for further explanation.) To improve the accuracy of the attenuator, the ATN COM nodes are bonded to both Pin 3 and Pin 4. *These should be connected directly to the "SIGNAL LOW" of the source* (for example, to the grounded side of the signal connector, as shown in Figure 32) not to an arbitrary point on the ground plane.

R4 is identical to R2, and in shunt with R3 (270Ω thin film) forms a 27Ω resistor with the same TC as the output resistance of the attenuator. By connecting Pin 1 to ATN LOW (Pin 2) this resistance minimizes the offset caused by bias currents. The offset nulling scheme shown in Figure 25 may still be used, with the external resistor R_B omitted and $R_{OS} = 500k\Omega$. Offset stability is improved because the compensating voltage introduced at Pin 20 is now PTAT. Drifts of under 1μV/°C (referred to Pins 1 and 20) can be maintained using the attenuator.

It may occasionally be desirable to attenuate the signal even further. For example, the source may have a full scale value of ±10V, and since the basic range of the AD640 extends only to ±200mV dc, an attenuation factor of ×50 might be chosen. This may be achieved either by using an independent external attenuator or more simply by adding a resistor in series with ATN IN (Pin 5). In the latter case the resistor must be trimmed to calibrate the intercept, since the input resistance at Pin 5 is not guaranteed. A fixed resistor of 1kΩ in series with a 500Ω variable resistor calibrate to an intercept of 50mV (or −26dBV) for dc or square wave inputs and provide a ±10V input range. The intercept stability will be degraded to about 0.003dB/°C.

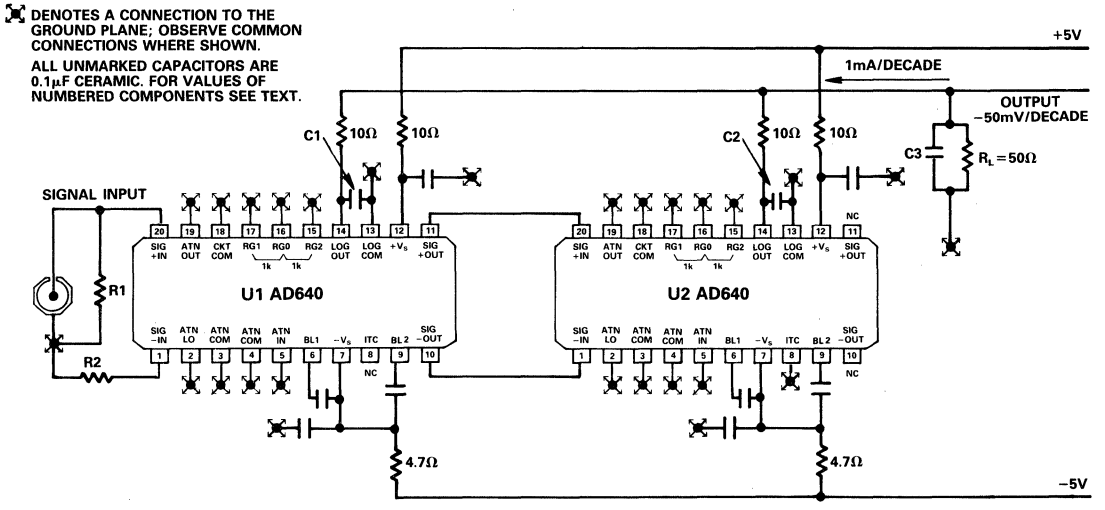


Figure 27. Basic Connections for Cascaded AD640s

OPERATION OF CASCADED AD640s

Frequently, the dynamic range of the input will be 50dB or more. AD640s can be cascaded, as shown in Figure 27. The balanced signal output from U1 becomes the input to U2. Resistors are included in series with each LOG OUT pin and capacitors C1 and C2 are placed *directly between Pins 13 and 14* to provide a local path for the RF current at these output pairs. C1 through C3 are chosen to provide the required low pass corner in conjunction with the load RL. Board layout and grounding disciplines are critically important at the high gain (X100,000) and bandwidth (~150MHz) of this system.

The intercept voltage is calculated as follows. First, note that if its LOG OUT is disconnected, U1 simply inserts 50dB of gain ahead of U2. This would lower the intercept by 50dB, to −110dBV for square wave calibration. With the LOG OUT of U1 added in, there is a finite zero signal current which slightly shifts the intercept. With the intercept temperature compensation on U1 disabled this zero signal output is −270μA (see DC SPECIFICATIONS) equivalent to a 5.4dB upward shift in the intercept, since the slope is 50μA/dB. Thus, the intercept is at −104.6dBV (−88.6dBm for 50Ω sine calibration). ITC may be disabled by grounding Pin 8 of either U1 or U2.

Cascaded AD640s can be used in dc applications, but input offset voltage will limit the dynamic range. The dc intercept is 6μV. *The offset should not be confused with the intercept*, which is found by *extrapolating* the transfer function from its central "log linear" region. This can be understood by referring to Equation (1) and noting that an input offset is simply additive to the value of V_{IN} in the numerator of the logarithmic argument; it does not affect the denominator (or intercept) V_X. In dc coupled applications of wide dynamic range, special precautions must be taken to null the input offset and minimize drift due to input bias offset. It is recommended that the input attenuator be used, providing a practical input range of −74dBV (±200μV dc) to +6dBV (±2V dc) when nulled using the adjustment circuit shown in Figure 25.

Eliminating the Effect of First Stage Offset

Usually, the input signal will be sinusoidal and U1 and U2 can be ac coupled. Figure 28a shows a low resistance choke at the input of U2 which shorts the dc output of U1 while preserving the hf response. Coupling capacitors may be inserted (Figure 28b) in which case two chokes are used to provide bias paths for U2. These chokes must exhibit high impedance over the operating frequency range.

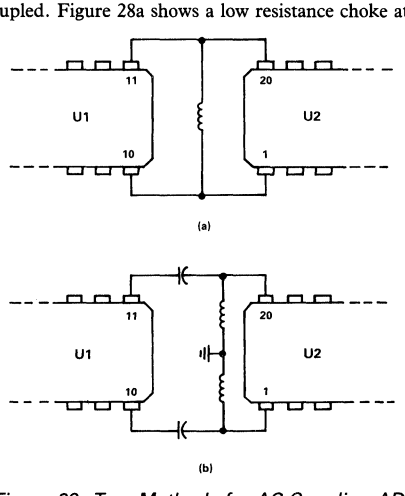


Figure 28. Two Methods for AC Coupling AD640s

Alternatively, the input offset can be nulled by a negative feedback network from the SIG OUT nodes of U2 to the SIG IN nodes of U1, as shown in Figure 29. The low pass response of the feedback path transforms to a closed-loop high pass response. The high gain (×100,000) of the signal path results in a commensurate reduction in the effective time constant of this network. For example, to achieve a high pass corner of 100kHz, the low pass corner must be at 1Hz.

In fact, it is somewhat more complicated than this. When the ac input sufficiently exceeds that of the offset, the feedback becomes ineffective and the response becomes essentially dc coupled. Even for quite modest inputs the last stage will be limiting and the output (Pins 10 and 11) of U2 will be a square wave of about ±180mV amplitude, dwelling approximately equal times at its two limit values, and thus having a net average value near zero. *Only when the input is very small does the high pass behavior of this nulling loop become apparent.* Consequently, the low pass time constant can usually be reduced considerably without serious performance degradation.

The resistor values are chosen such that the dc feedback is adequate to null the worst case input offset, say, 500μV. There must be some resistance at Pins 1 and 20 across which the offset compensation voltage is developed. The values shown in the figure assume that we wish to terminate a 50Ω source at Pin 20. The 50Ω resistor at Pin 1 is essential, both to minimize offsets due to bias current mismatch and because the outputs at Pins 10 and 11 can only swing negatively (from ground to −180mV) whereas we need to cater for input offsets of either polarity.

For a sine input of 1μV amplitude (−120dBV) and in the absence of offset, the differential voltage at Pins 10 and 11 of U2 would be almost sinusoidal but 100,000 times larger, or 100mV. The last limiter in U2 would be entering saturation. A 1μV input offset added to this signal would put the last limiter well into saturation, and its output would then have a *different average value*, which is extracted by the low pass network and delivered back to the input. For larger signals, the output approaches a square wave for zero input offset and becomes rectangular when offset is present. The duty cycle modulation of this output now produces the nonzero average value. Assume a maximum required differential output of 100mV (after averaging in C1 and C2) as shown in Figure 29. R3 through R6 can now be chosen to provide ±500μV of correction range, and with these values the input offset is reduced by a factor of 500. Using 4.7μF capacitors, the time constant of the network is about 1.2ms, and its corner frequency is at 13.5Hz. The closed loop high pass corner (for small signals) is, therefore, at 1.35MHz.

Bandwidth/Dynamic Range Tradeoffs

The first stage noise of the AD640 is 2nV/$\sqrt{\text{Hz}}$ (short circuited input) and the full bandwidth of the cascaded ten stages is about 150MHz. Thus, the noise referred to the input is 24.5μV rms, or −79dBm, which would limit the dynamic range to 77dBs (−79dBm to −2dBm). In practice, the source resistances will also generate noise, and the full bandwidth dynamic range will be less than this.

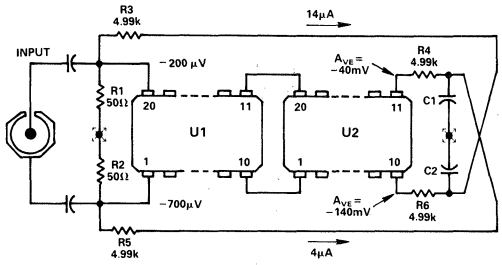


Figure 29. Feedback Offset Correction Network

A low pass filter between U1 and U2 can limit the noise bandwidth and extend the dynamic range. The simplest way to do this is by the addition of a pair of grounded capacitors at the signal outputs of U1 (shown as C1 and C2 in Figure 32). The −3dB frequency of the filter must be above the highest frequency to be handled by the converter; if not, nonlinearity in the transfer function will occur. This can be seen intuitively by noting that the system would then contract to a single AD640 at very high frequencies (when U2 has very little input). At intermediate frequencies, U2 will contribute less to the output than would be the case if there were no interstage attenuation, resulting in a kink in the transfer function.

More complex filtering may be considered. For example, if the signal has a fairly narrow bandwidth, the simple chokes shown in Figure 28 might be replaced by one or more parallel tuned circuits. Two separate tuned circuits or transformer coupling should be used to eliminate all undesirable hf common mode coupling between U1 and U2. The choice of Q for these circuits requires compromise. Frequency sensitive nonlinearities can arise at the edges of the band if the Q is set too high; if too low, the transmission of the signal from U1 to U2 will be affected even at the center frequency, again resulting in nonlinearity in the conversion response. In calculating the Q, note that the resistance from Pins 10 and 11 to ground is 75Ω. The input resistance at Pins 1 and 20 is very high, but the capacitances at these pins must also be factored into the total LCR circuit.

PRACTICAL APPLICATIONS

We show here two applications, using cascaded AD640s to achieve a wide dynamic range. As already mentioned, the use of a differential signal path and differential logarithmic outputs diminishes the risk of instability due to poor grounding. Nevertheless, it must be remembered that at high frequencies even very small lengths of wire, including the leads to capacitors, have significant impedance. The ground plane itself can also generate small but troublesome voltages due to circulating currents in a poor layout. A printed circuit evaluation board is available from Analog Devices (Part Number ADEB640) to facilitate the prototyping of an application using one or two AD640s, plus various external components.

At very low signal levels various effects can cause significant deviation from the ideal response, apart from the inherent nonlinearities of the transfer function already discussed. Note that *any spurious signal presented to the AD640s is demodulated and added to the output*. Thus, in the absence of thorough shielding, emissions from any radio transmitters or RFI from equipment operating in the locality will cause the output to appear too high. The only cure for this type of error is the use of very careful grounding and shielding techniques.

50MHz–150MHz Converter with 70dB Dynamic Range

Figure 30 shows a logarithmic converter using two AD640s which can provide at least 70dB of dynamic range, limited mostly by first stage noise. In this application, an rf choke (L1) prevents the transmission of dc offset from the first to the second AD640. One or two turns in a ferrite core will generally suffice for operation at frequencies above 30MHz. For example, one complete loop of 20 gauge wire through the two holes in a Fair-Rite type 2873002302 core provides an inductance of 5μH, which presents an impedance of 1.57kΩ at 50MHz. The shunting effect across the 150Ω differential impedance at the signal interface is thus fairly slight.

The signal source is optionally terminated by R1. To minimize the input offset voltage R2 should be chosen to match the dc resistance of the terminated source. (However, the offset voltage is not a critical consideration in this ac coupled application.)

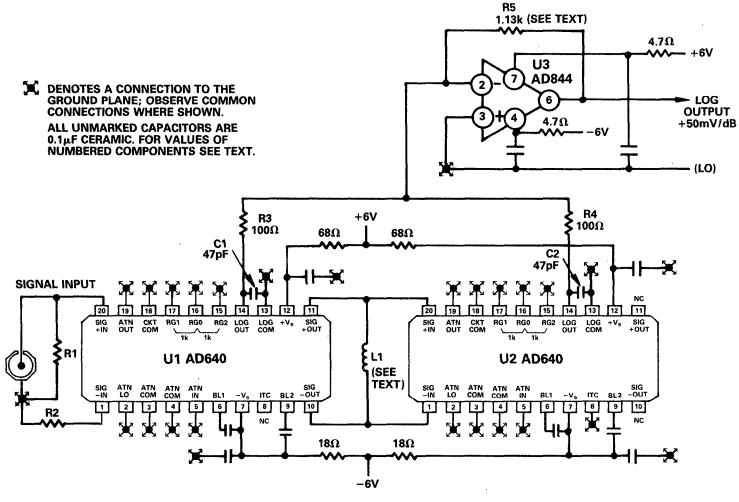


Figure 30. Complete 70dB Dynamic Range Converter for 50MHz–150MHz Operation

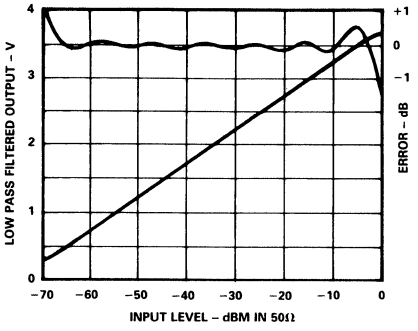


Figure 31. Logarithmic Output and Nonlinearity for Circuit of Figure 30, for a Sine Wave Input at f =80MHz

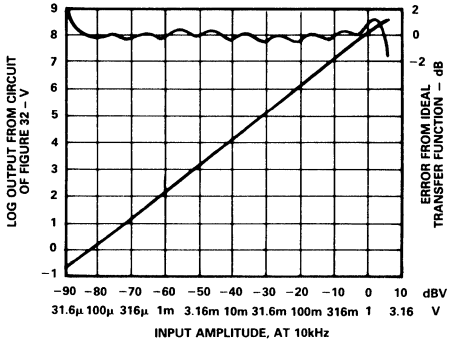


Figure 33. Logarithmic Output and Nonlinearity for Circuit of Figure 32, for a Square Wave Input at f= 10kHz

Note that all unused inputs are grounded; this improves the isolation from the outputs back to the inputs.

A transimpedance op amp (U3, AD844) converts the summed logarithmic output currents of U1 and U2 to a ground referenced voltage scaled 1V per decade. The resistor R5 is nominally 1kΩ but is increased slightly to compensate for the slope deficit at the operating frequency, which can be determined from Figure 12.

The inverting input of U3 forms a virtual ground, so that each logarithmic output of U1 and U2 is loaded by 100Ω (R3 or R4). These resistors in conjunction with capacitors C1 and C2 form independent low pass filters with a time constant of about 5ns. These capacitors should be connected directly across Pins 13 and 14, as shown, to prevent high frequency output currents from circulating in the ground plane. A second 5ns time constant is formed by feedback resistor R5 in conjunction with the transcapacitance of U3.

This filtering is adequate for input frequencies of 50MHz or above; more elaborate filtering can be devised for pulse applications requiring a faster rise time. In applications where only a long term measure of the input is needed, C1 and C2 can be increased and U3 can be replaced by a low speed op amp. Figure 31 shows typical performance of this converter.

10Hz–100kHz Converter with 95dB Dynamic Range

To increase the dynamic range it is necessary to reduce the bandwidth by the inclusion of a low pass filter at the signal interface between U1 and U2 (Figure 32). To provide operation down to low frequencies, dc coupling is used at the interface between AD640s and the input offset is nulled by a feedback circuit.

Using values of 0.02µF in the interstage filter formed by capacitors C1 and C2, the hf corner occurs at about 100kHz. U3 (AD712) forms a 4-pole 35Hz low pass filter. This provides operation to signal frequencies below 20Hz. The filter response is not critical, allowing the use of an electrolytic capacitor to form one of the poles.

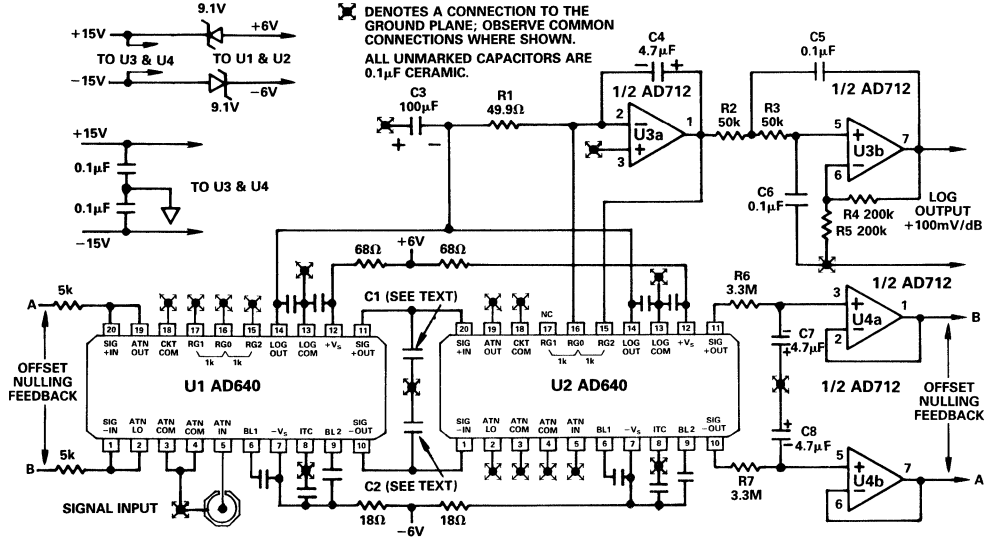


Figure 32. Complete 95dB Dynamic Range Converter

R1 is restricted to 50Ω by the compliance at Pin 14, so C3 needs to be large to form a 5ms time constant. A tantalum capacitor is used (note polarity). The output of U3a is scaled +1V per decade, and the X2 gain of U3b raises this to +2V per decade, or +100mV/dB. The differential offset at the output of U2 is low pass filtered by R6/C7 and R7/C8 and buffered by voltage followers U4a and U4b. The 16s open loop time constant translates to a closed loop high pass corner of 10Hz. (This high pass filter is only operative for very small inputs; see page 13.) Figure 33 shows the performance for square wave inputs. Since the attenuator is used, the upper end of the dynamic range now extends to +6dBV and the intercept is at −82dBV. The noise limited dynamic range is over 100dB, but in practice spurious signals at the input will determine the achievable range.

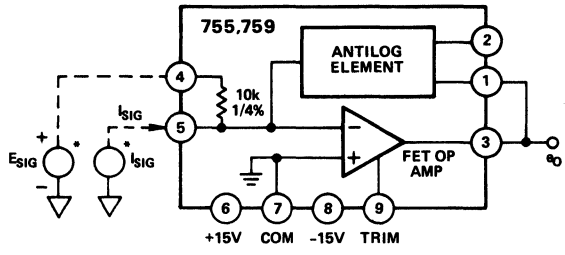
6-Decade, High Accuracy, Wideband Log, Antilog Amplifiers

755N/755P/759N/759P

FEATURES

High Accuracy: Models 755N, 755P
Wideband: Models 759N, 759P
Complete Log/Antilog Amplifiers: External Components Not Required
Temperature-Compensated Internal Reference
6 Decades Current Operation: 1nA to 1mA
1% max Error: 1nA to 1mA (755)
20nA to 200μA (759)
4 Decades Voltage Operation: 1mV to 10V
1% max Error: 1mV to 10V (755)
1mV to 2V (759)
Small Size: 1.1" X 1.1" X 0.4"

FUNCTIONAL BLOCK DIAGRAM



*POSITIVE INPUT SIGNALS, AS SHOWN; USE 759N, 755P.
NEGATIVE INPUT SIGNALS, USE 759N, 755P.

GENERAL DESCRIPTION

The models 755N, 755P and 759N, 759P are low cost dc logarithmic amplifiers offering conformance to ideal log operation over 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). For high accuracy requirements, models 755N, 755P offer maximum nonconformity of 0.5%, from 10nA to 1mA, and 1mV to 1V. For wideband applications, the models 759N, 759P provide fast response (300kHz @ I_{SIG} = 10μA to 1mA) and feature maximum nonconformity of 1% from 20nA to 200μA, and 1mV to 2V. The models 755N and 759N compute the log of positive (+) input signals, while the models 755P, 759P compute the log of negative (-) signals.

Designed for ease of use, the models 755N/P and 759N/P are complete, temperature compensated log/antilog amplifiers packaged in a compact epoxy-encapsulated module. External components are not required for logging currents over the complete 6 decade range of 1μA to 1mA. Both the scale factor (K=2, 1, or 2/3 volt/decade) and log/antilog operation are selected by simple pin connection. In addition, both the internal 10μA reference current as well as the offset voltage may be externally adjusted to improve overall accuracy.

The models 755 and 759 are ideally suited as an alternative to in-house designs of OEM applications. Advanced design techniques and superior performance place the 755 and 759 ahead of competitive designs in terms of price, performance and package design.

APPLICATIONS

When connected in the current or voltage logging configuration, as shown in Figure 1, the models 755 and 759 may be used in several key applications. A plot of input current versus output voltage is also presented to illustrate the log amplifier's transfer characteristics.

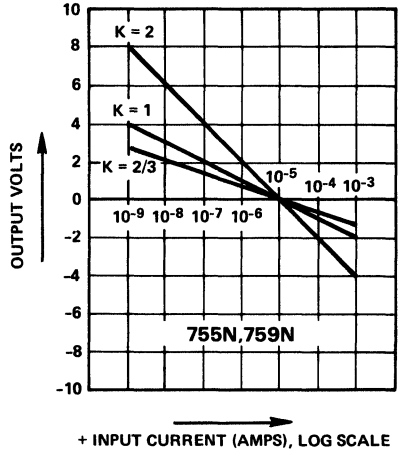


Figure 1. Transfer Function

755N/755P/759N/759P—SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	755N/P	759N/P
TRANSFER FUNCTIONS		
Current Mode	$e_O = -K\log_{10}\frac{I_{SIG}}{I_{REF}}$	•
Voltage Mode	$e_O = -K\log_{10}\frac{E_{SIG}}{E_{REF}}$	•
Antilog Mode	$e_O = E_{REF}\ 10^{-\left(\frac{E_{SIG}}{K}\right)}$	•
TRANSFER FUNCTION PARAMETERS		
Scale Factor (K) Selections[1, 2]	2, 1, 2/3 Volt/Decade	•
Error @ +25°C	±1% max	•
vs. Temperature (0 to +70°C)	±0.04%/°C max	•
Reference Voltage (E_{REF})[2]	0.1V	•
Error @ +25°C	±3% max	±4% max
vs. Temperature (0 to +70°C)	±0.1%/°C max	±0.05%/°C
Reference Current (I_{REF})[2]	10μA	•
Error @ +25°C	±3% max	•
vs. Temperature (0 to +70°C)	±0.1%/°C max	±0.05%/°C

MAXIMUM LOG CONFORMITY ERROR

I_{SIG} RANGE	E_{SIG} RANGE	RTI	RTO (K=1)	RTI	RTO (K=1)
1nA to 10nA	–	±1%	±4.3mV	±5%	±21mV
10nA to 20nA	–	±0.5%	±2.17mV	±2%	±8.64mV
20nA to 100μA	1mV to 1V	±0.5%	±2.17mV	±1%	±4.3mV
100μA to 200μA	1V to 2V	±1%	±4.3mV	±1%	±4.3mV
200μA to 1mA	2V to 10V	±1%	±4.3mV	±2%	±8.64mV

INPUT SPECIFICATIONS		
Current Signal Range		
Model 755N, 759N	+1nA to +1mA min	•
Model 755P, 759P	−1nA to −1mA min	•
Max Safe Input Current	±10mA max	•
Bias Current @ +25°C	(0, +) 10pA max	(0, +) 200pA max
vs. Temperature (0 to +70°C)	x2/+10°C	•
Voltage Signal Range (Log Mode)		
Model 755N, 759N	+1mV to +10V min	•
Model 755P, 759P	−1mV to −10V min	•
Voltage Signal Range, Antilog Mode Model 755N, 755P	$-2 \leqslant \frac{E_{SIG}}{K} \leqslant 2$	•
Offset Voltage @ +25°C (Adjustable to 0)	±400μV max	±2mV max
vs. Temperature (0 to +70°C)	±15μV/°C max	±10μV/°C
vs. Supply Voltage	±15μV/%	•
FREQUENCY RESPONSE, Sinewave		
Small Signal Bandwidth, −3dB		
I_{SIG} = 1nA	80Hz	250Hz
I_{SIG} = 1μA	10kHz	100kHz
I_{SIG} = 10μA	40kHz	200kHz
I_{SIG} = 1mA	100kHz	200kHz
RISE TIME		
Increasing Input Current		
10nA to 100nA	100μs	20μs
100nA to 1μA	7μs	3μs
1μA to 1mA	4μs	2.5μs
Decreasing Input Current		
1mA to 1μA	7μs	3μs
1μA to 100nA	30μs	10μs
100nA to 10nA	400μs	80μs
INPUT NOISE		
Voltage, 10Hz to 10kHz	2μV rms	10μV rms
Current, 10Hz to 10kHz	2pA rms	10pA rms
OUTPUT SPECIFICATIONS[3]		
Rated Output		
Voltage	±10V min	•
Current		
Log Mode	±5mA	•
Antilog Mode	±4mA	•
Resistance	0.5Ω	•
POWER SUPPLY[4]		
Rated Performance	±15Vdc	•
Operating	±(12 to 18)Vdc	•
Current, Quiescent	±7mA	±4mA
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	•
Operating	−25°C to +85°C	•
Storage	−55°C to +125°C	•
CASE SIZE[5] (W x L x H)	1.5" x 1.5" x 0.4" (38 x 38 x 10.4)	1.125" x 1.125" x 0.4" (29 x 29 x 10.4)

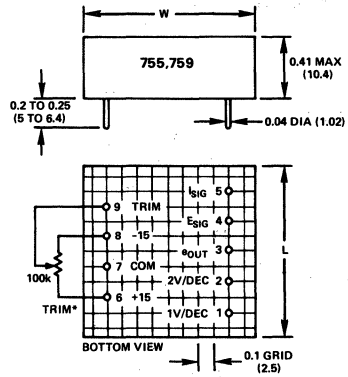
NOTES

[1] Use terminal 1 for K = 1V/decade; terminal 2 for K = 2V/decade; terminals 1 or 2 (shorted together) for K = 2/3V/decade.
[2] Specification is + for models 755N, 759N; − for 755P, 759P.
[3] No damage due to any pin being shorted to ground.
[4] Recommended power supply, model 904, ±15V @ ±50mA output.
[5] Case size in inches (mm).

Specifications subject to change without notice.

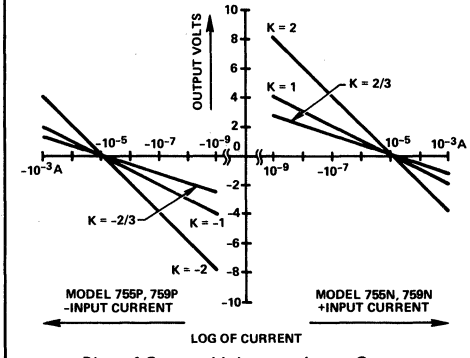
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

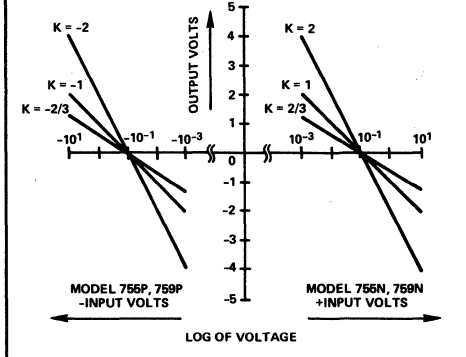


*Optional 100kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±0.4mV (755) or ±2mV (759) maximum.

MATING SOCKET AC1016



Plot of Output Voltage vs Input Current for Model 755 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Models 755, 759 Connected in the Log Mode

Figure 2. Transfer Curves

PRINCIPLE OF OPERATION

Log operation is obtained by placing the antilog element in the feedback loop of the op amp as shown in Figure 1. At the summing junction, terminal 5, the input signal current to be processed is summed with the output current of the antilog element. To attain a balance of these two currents, the op amp provides the required output voltage to the antilog feedback element. Under these conditions the ideal transfer equation (K = 1) is:

$$e_{OUT} = 1V \log_{10} I_{SIG}/I_{REF}$$

The log is a mathematical operator which is defined only for numbers, which are dimensionless quantities. Since an input current would have the dimensions of amperes it must be referenced to another current, I_{REF}, the ratio being dimensionless. For this purpose a temperature compensated reference of 10μA is generated internally.

The scale factor, K, is a multiplying constant. For a change in input current of one decade (decade = ratio of 10:1), the output changes by K volts. K may be selected as 1V or 2V by connecting the output to pin 1 or 2, respectively. If the output is connected to both pins 1 and 2, K will be 2/3V.

REFERRING ERRORS TO INPUT

A unique property of log amplifiers is that a dc error of any given amount at the output corresponds to a constant percent of the input, regardless of input level. To illustrate this, consider the output effects due to changing the input by 1%.

The output would be:

$$e_{OUT} = 1V \log_{10} (I_{SIG}/I_{REF})(1.01) \text{ which is equivalent to:}$$

$$e_{OUT} = \underbrace{1V \log_{10} (I_{SIG}/I_{REF})}_{\text{Initial Value}} \quad \underbrace{\pm 1V \log_{10} (1.01)}_{\text{Change}}$$

The change in output, due to a 1% input change is a constant value of ±4.3mV. Conversely, a dc error at the output of ±4.3mV is equivalent to a change at the input of 1%. An abbreviated table is presented below for converting between errors referred to output (R.T.O.), and errors referred to input (R.T.I.).

	ERROR R.T.O.		
ERROR R.T.I.	K = 1	K = 2	K = 2/3
0.1%	0.43mV	0.86mV	0.28mV
0.5	2.17	4.34	1.45
1.0	4.32	8.64	2.88
3.0	12.84	25.68	8.56
4.0	17.03	34.06	11.35
5.0	21.19	42.38	14.13
10.0	41.39	82.78	27.59

Table I. Converting Output Error in mV to Input Error in %

SOURCES OF ERROR

Log Conformity Error – Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the value of the transfer equation and the actual value which occurs at the output of the log module, after scale factor, reference and offset errors are eliminated to taken into account. The best linearity performance for the models 755, 759 are obtained in the 5 decades from 10nA to 1mA. To obtain optimum performance, the input data should be scaled to this range.

Offset Voltage – The offset voltage, E_{os}, of models 755, 759 is the offset voltage of the internal FET amplifier. This voltage appears as a small dc offset voltage in series with the input terminals. For current logging applications, its error contribution is negligible. However, for log voltage applications, best performance is obtained by an offset trim adjustment.

Bias Current – The bias current of models 755, 759 is the bias current of the internal FET amplifier. This parameter can be a significant source of error when processing signals in the nanoamp region. For this reason, the bias current for model 755 is 10pA, maximum, and 200pA maximum for model 759.

Reference Current – I_{REF} is the internally generated current source to which all input currents are compared. I_{REF} tolerance errors appear as a dc offset at the output. The specified value of I_{REF} is ±3% referred to the input, and, from Table I, corresponds to a dc offset of ±12.84mV for K = 1. This offset is independent of input signal and may be removed by injecting a current into terminal 1 or 2.

Reference Voltage – E_{REF} is the effective internally generated voltage to which all input voltages are compared. It is related to I_{REF} through the equation:
$E_{REF} = I_{REF} \times R_{IN}$, where R_{IN} is an internal 10kΩ, precision resistor. Virtually all tolerance in E_{REF} is due to I_{REF}. Consequently, variations in I_{REF} cause a shift in E_{REF}.

Scale Factor – Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in per cent of the nominal value. An external adjustment may be performed if fine trimming is desired for improved accuracy.

OPTIONAL EXTERNAL ADJUSTMENTS FOR LOG OPERATION

Trimming E_{OS} – The amplifier's offset voltage, E_{OS}, may be trimmed for improved accuracy with the models 755, 759 connected in its log circuit. To accomplish this, a 100kΩ, 10 turn pot is connected as shown in Figure 3. The input terminal, Pin 4, is connected to ground. Under these conditions the output voltage is:

$$e_{OUT} = -K \log_{10} E_{OS}/E_{REF}$$

To obtain an offset voltage of 100μV or less, for K = 1, the trim pot should be adjusted until the output voltage is between +3 and +4 volts for models 755N, 759N, and -3V to -4V for models 755P, 759P.

For other values of K, the trim pot should be adjusted for an output of e_{OUT} = 3 x K to 4 x K where K is the scale factor.

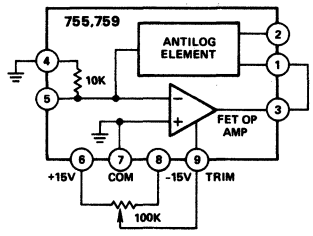


Figure 3. Trimming E_{OS} in Log Mode

Reference Current or Reference Voltage – The reference current or voltage of models 755, 759 may be shifted by injecting a constant current into the unused scale factor terminal (Pin 1 or Pin 2). The current injected will shift the reference one decade, in accordance with the expression: I_I = 66μA log 10μA/I_{REF} (755), I_I = 330μA log 10μA/I_{REF} (759), where I_I = current to be injected and I_{REF} = the desired reference current.

By changing I_{REF}, there is a corresponding change in E_{REF} since, E_{REF} = I_{REF} x R_{IN}. An alternate method for rescaling E_{REF} is to connect an external R_{IN}, at the I_{IN} terminal (Pin 5) to supplant the 10kΩ supplied internally (leaving it unconnected). The expression for E_{REF} is then, E_{REF} = R_{IN} I_{REF}. Care must be taken to choose R_{IN} such that (e_{SIG} max)/R_{IN} ⩽1mA.

Scale Factor (K) Adjustment – Scale factor may be increased from its nominal value by inserting a series resistor R_S between the output terminal, Pin 3, and either terminal 1 or 2. The table below should be consulted when making these scale factor changes.

RANGE OF K	CONNECT SERIES R TO PIN	VALUE OF R_S	NOTE
2/3V to 1.01V	1	R x (K - 2/3)	use pins 1, 2
1.01V to 2.02V	1	R x (K - 1)	use pin 1
>2.02V	2	R x (K - 2)	use pin 2

R = 15kΩ (755); 3kΩ (759)

Table 2. Resistor Selection Chart for Shifting Scale Factor

ANTILOG OPERATION

The models 755 and 759 may be used to develop the antilog of the input voltage when connected as shown in Figure 4. The antilog transfer function (an exponential), is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} \qquad [-2 \leqslant e_{IN}/K \leqslant 2]$$

Principle of Operation – The antilog element converts the voltage input, appearing at terminal 1, to a current which is proportional to the antilog of the applied voltage. The current-to-voltage conversion is then completed by the feedback resistor in a closed-loop op amp circuit.

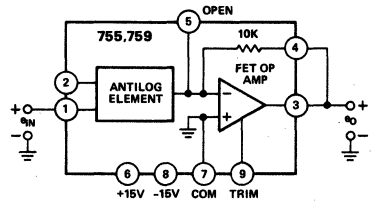


Figure 4. Functional Block Diagram

A more complete expression for the antilog function is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} + E_{OS}$$

The terms K, E_{OS}, and E_{REF} are those described previously in the LOG section.

Offset Voltage (E_{OS}) Adjustment – Although offset voltage of the antilog circuit may be balanced by connecting it in the log mode, and using the technique described previously, it may be more advantageous to use the circuit of Figure 5. In this configuration, offset voltage is equal to e_{OUT}/100. Adjust for the desired null, using the 100k trim pot. After adjusting, turn power off, remove the external 100Ω resistor, and the jumper from Pin 1 to +15V. For 755P, 759P use the same procedure but connect Pin 1 to -15V.

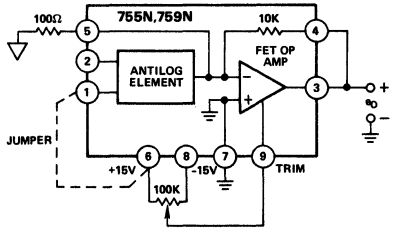


Figure 5. Trimming E_{OS} in Antilog Mode

Reference Voltage (E_{REF}) Adjustment – In antilog operation, the voltage reference appears as a multiplying constant. E_{REF} adjustment may be accomplished by connecting a resistor, R, from Pin 5 to Pin 3, in place of the internal 10kΩ. The value of R is determined by:

R = E_{REF} desired/10^{-5} A

Scale Factor (K) Adjustment – The scale factor may be adjusted for all values of K greater than 2/3V by the techniques described in the log section. If a value of K less than 2/3V is desired for a given application, an external op amp would be required as shown in Figure 6. The ratio of the two resistors is approximately:

$R1/R_G$ = (1/K – 1) where K = desired scale factor

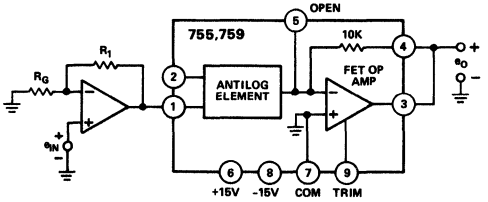


Figure 6. Method for Adjusting K<2/3V

RMS-to-DC Converters
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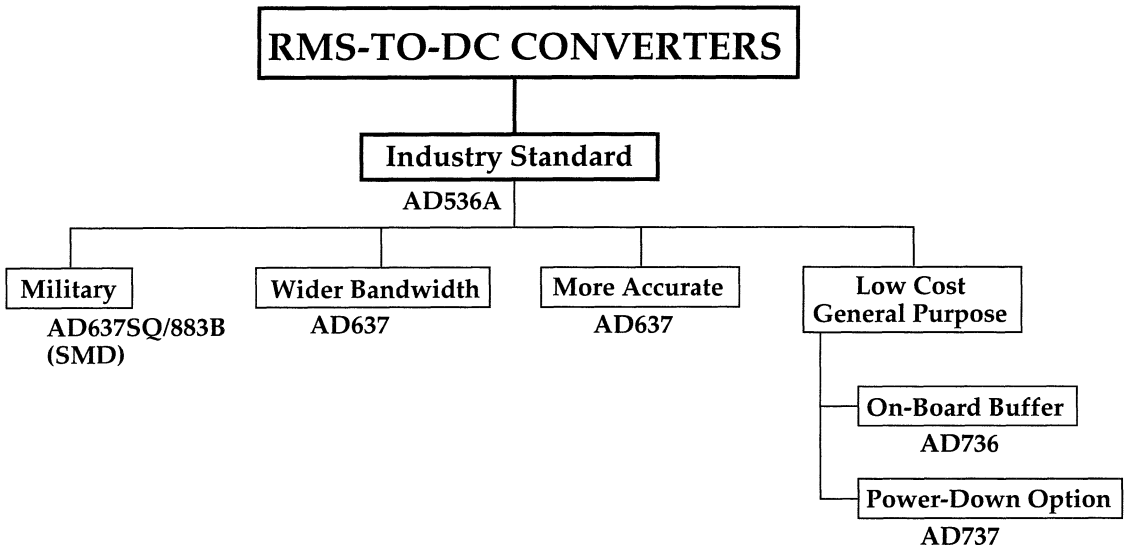
RMS-to-DC Converters



Selection Guide
RMS-to-DC Converters

Model	Conversion Accuracy mV ±%Read max	Full-Scale Range V RMS	dB Output Error dB max	Package Options[1]	Temp Range[2]	Page[3]	Comments
SSM-2110	0.2±0.012	7	0.5	2	C	AV	High Accuracy, Wide Dynamic Range
AD737	**(0.2±0.3)–(0.4±0.5)**	**0.2**		**2, 3, 6**	**C, I**	**4–39**	**Low Cost, Low Power, Power Down**
AD736	**(0.3±0.3)–(0.5±0.5)**	**0.2**		**2, 3, 6**	**C, I**	**4–31**	**General Purpose, Low Cost, Low Power**
AD636	(0.2±0.3)–(0.5±0.6)	0.2	0.2–0.5	1, 7	C	4–15	Low Power
AD637	**(0.5±0.2)–(1±0.5)**	**7**	**0.3 (typ)**	**1, 3, 6**	**C, M**	**4–23**	**High Accuracy, Wide Bandwidth**
AD536A	(2±0.2)–(5±0.5)	7	0.3–0.6	1, 3, 4, 6, 7	C, M	4–7	General Purpose

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[3]AV = *Audio/Video Reference Manual*.
Boldface Type: Product recommended for new design.
*New product.

Orientation
RMS-to-DC Converters

RMS-to-DC converters continuously compute the instantaneous square of the input signal, average it, and take the square root of the result, to provide a dc voltage proportional to the rms of the input (and, in the case of the AD536 and AD636, an auxiliary dc voltage that is proportional to the *log* of the rms, for dB measurements).

Excellent pretrimmed performance, improvable by simple optional trims, makes these devices ideal for all types of laboratory and OEM rms instrumentation where amplitude measurements must be made with high accuracy, independently of waveshape.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolute-deviation, or "ac average." It is performed by taking the absolute value of a signal (i.e., rectifying it) filtering it and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform; it will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

An important application is noise measurement – for example, thermal noise, transistor noise, and switch-contact noise. True rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties.

True rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise and acoustical noise.

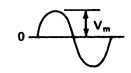
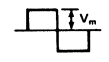
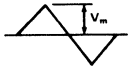
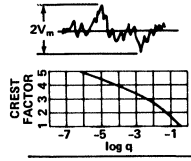
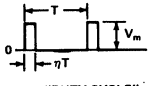
The electrical signals produced by these mechanical actions are often noisy, nonperiodic, nonsinusoidal, and superimposed on dc levels, and require true rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

The basic approach used in these converters for computing the rms is to take the absolute value, square it and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$V_{RMS} = Avg.\left[\frac{V_{in}^2}{V_{RMS}}\right] \cong \sqrt{Avg.\ (V_{in}^2)}$$

is valid if the averaging time constant is sufficiently long compared with the periods of the lowest frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter using an external filtering capacitor (C_{AV}). Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, an additional stage of 2-pole filtering is useful. The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of C_{AV}.

WAVEFORM		RMS	MAD	$\frac{\text{RMS}}{\text{MAD}}$	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ 0.707 V_m	$\frac{2}{\pi} V_m$ 0.637 V_m	$\frac{\pi}{2\sqrt{2}} = 1.111$	$\sqrt{2} = 1.414$
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}} = 1.155$	$\sqrt{3} = 1.732$
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS = 0.798 RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F. / q 1 / 32% 2 / 4.6% 3 / 0.37% 3.3 / 0.1% 3.9 / 0.01% 4 / 63ppm 4.4 / 10ppm 4.9 / 1ppm 6 / 2×10^{-9}
	PULSE TRAIN η / MARK/SPACE 1 / ∞ 0.25 / 0.3333 0.0625 / 0.0667 0.0156 / 0.0159 0.01 / 0.0101	$V_m\sqrt{\eta}$ V_m $0.5V_m$ $0.25V_m$ $0.125V_m$ $0.1V_m$	$V_m\eta$ V_m $0.25V_m$ $0.0625V_m$ $0.0156V_m$ $0.01V_m$	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10

PERFORMANCE SPECIFICATIONS

Considerable information regarding rms-to-dc converter circuit design, performance, selection and applications is to be found in the *RMS-to-DC Conversion Application Guide*[1] and in the application note *RMS-to-DC Converters Ease Measurement Task*.[2] In addition, useful applications information can be found in the *Nonlinear Circuits Handbook*.[3]

The most-salient feature of a true rms-to-dc converter is that *it ideally has no error due to an indirect approximation to the rms.* Static errors are due only to scale-factor, linearity and offset errors; dynamic errors are due to insufficient averaging time at the low end and finite bandwidth and slewing rate at the upper end. Linearity errors affect crest factor in midband. Dynamic errors are also a function of signal amplitude, due in part to the variation of bandwidth of the "log" transistors with signal level.

Total Error, Internal Trim, a specification for quick reference, is the maximum deviation of the dc component of the output voltage from the theoretical output value over a specified range of signal amplitude and frequency. It is shown as the sum of a fixed error and a component proportional to the theoretical output (% of reading). It is specified for a sinusoidal input in a given frequency and amplitude range. The fixed error component includes all offset errors and irreducible nonlinearities; the %-of-reading component includes the linear scale-factor error.

Total Error, External Adjustment is the amount by which the output may differ from the theoretical value when the output offset and scale factor have been trimmed. Note that the fixed error-component cannot be reduced to zero, even though the output offset can be nulled at zero input. This is because of residual input offsets and inherent nonlinearities in the converter.

Total Error vs. Temperature (T_{min} to T_{max}) is the average change of %-of-full-scale error component plus the average change of percent-of-reading error component per degree Celsius, over the rated temperature range.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for −3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal −30% of reading. It is a function of amplitude.

Crest Factor (to a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case – rectangular pulse – input signal.

Averaging Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance (C_{AV}).

Input: The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

Output: The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Power Supply: Power-supply range for specified performance, power-supply range for operation and quiescent current drain.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements (T_H − 25°C), (25°C − T_L), when measured.

[1]***RMS-to-DC Conversion Application Guide 2nd Edition*, by C. Kitchin and L. Counts (1986-61 pages). Available free from Analog Devices.**
[2]***RMS-to-DC Converters Ease Measurements Tasks*, Application Note E1519–18–4/91, Analog Devices, Inc. 1991, 12 pages available free from Analog Devices.**
[3]***Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536 pages, edited by D.H. Sheingold. ($5.95).**

ANALOG DEVICES

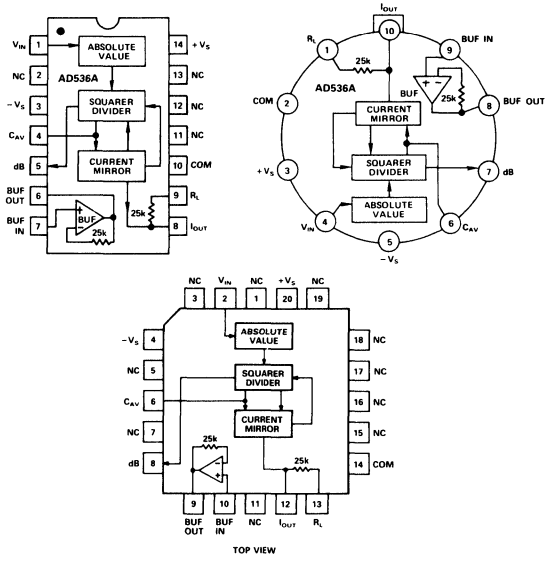
Integrated Circuit True RMS-to-DC Converter

AD536A

FEATURES

True RMS-to-DC Conversion
Laser-Trimmed to High Accuracy
0.2% max Error (AD536AK)
0.5% max Error (AD536AJ)
Wide Response Capability:
Computes RMS of AC and DC Signals
450kHz Bandwidth: V_{rms} > 100mV
2MHz Bandwidth: V_{rms} > 1V
Signal Crest Factor of 7 for 1% Error
dB Output with 60dB Range
Low Power: 1.2mA Quiescent Current
Single or Dual Supply Operation
Monolithic Integrated Circuit
−55°C to +125°C Operation (AD536AS)

PIN CONFIGURATIONS AND FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300kHz with 3dB error for signal levels above 100mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60 dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full-scale accuracy at 7V rms. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0 to +70°C) applications, and one grade (S) rated for the −55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2mV ±0.2% of reading, and the AD536AJ and AD536AS have maximum errors of ±5mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or 10-pin TO-100 metal can. The AD536AS is also available in a 20-pin hermetically sealed ceramic leadless chip carrier.

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536 and provides improved bandwidth and temperature drift specifications.

AD536A—SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted.)

Model	AD536AJ Min	AD536AJ Typ	AD536AJ Max	AD536AK Min	AD536AK Typ	AD536AK Max	AD536AS Min	AD536AS Typ	AD536AS Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Figure 1)			**±5 ±0.5**			**±2 ±0.2**			**±5 ±0.5**	mV ± % of Reading
vs. Temperature, T_{min} to +70°C			±0.1 ±0.01			±0.05 ±0.005			**±0.1 ±0.005**	mV ± % of Reading/°C
+70°C to +125°C									**±0.3 ±0.005**	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error		±0.2			±0.1			±0.2		± % of Reading
Total Error, External Trim[1] (Figure 2)		±3 ±0.3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
ERROR VS. CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.1			−0.1			−0.1		% of Reading
Crest Factor = 7		−1.0			−1.0			−1.0		% of Reading
FREQUENCY RESPONSE[3]										
Bandwidth for 1% additional error (0.09dB)										
V_{IN} = 10mV		5			5			5		kHz
V_{IN} = 100mV		45			45			45		kHz
V_{IN} = 1V		120			120			120		kHz
± 3dB Bandwidth										
V_{IN} = 10mV		90			90			90		kHz
V_{IN} = 100mV		450			450			450		kHz
V_{IN} = 1V		2.3			2.3			2.3		MHz
AVERAGING TIME CONSTANT (Figure 5)		25			25			25		ms/μF CAV
INPUT CHARACTERISTICS										
Signal Range, ± 15V Supplies										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±20			±20			±20	V peak
Continuous rms Level, ± 5V Supplies		0 to 2			0 to 2			0 to 2		V rms
Peak Transient Input, ± 5V Supplies			±7			±7			±7	V peak
Maximum Continuous Nondestructive Input Level (All Supply Voltages)			±25			±25			±25	V peak
Input Resistance	13.33	16.67	20	13.33	16.67	20	13.33	16.67	20	kΩ
Input Offset Voltage		0.8	±2		0.5	±1		0.8	±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage, V_{IN} = COM (Figure 1)		±1	**±2**		±0.5	**±1**			**±2**	mV
vs. Temperature		±0.1			±0.1				**±0.2**	mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
Voltage Swing, ± 15V Supplies	**0 to +11**	+12.5		**0 to +11**	+12.5		**0 to +11**	+12.5		V
± 5V Supply	0 to +2			0 to +2			0 to +2			V
dB OUTPUT (Figure 13)										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.4	**±0.6**		±0.2	**±0.3**		±0.5	**±0.6**	dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor TC (Uncompensated, see Figure 1 for Temperature Compensation)		−0.033			−0.033			−0.033		dB/°C
		+0.33			+0.33			+0.33		% of Reading/°C
I_{REF} for 0dB = 1V rms	**5**	20	**80**	**5**	20	**80**	**5**	20	**80**	μA
I_{REF} Range	1		100	1		100	1		100	μA
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		μA/V rms
I_{OUT} Scale Factor Tolerance		±10	±20		±10	±20		±10	±20	%
Output Resistance	20	25	30	20	25	30	20	25	30	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5)			$-V_S$ to ($+V_S$ −2.5V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range		$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)		V
Input Offset Voltage, R_S = 25k		±0.5	**±4**		±0.5	**±4**		±0.5	**±4**	mV
Input Bias Current		20	**60**		20	**60**		20	**60**	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			(+5mA, −130μA)			
Short Circuit Current		20			20			20		mA
Output Resistance			0.5			0.5			0.5	Ω
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/μs
POWER SUPPLY										
Voltage Rated Performance		±15			±15			±15		V
Dual Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S, 5V to 36V, T_{min} to T_{max}		1.2	**2**		1.2	**2**		1.2	**2**	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	−55		+125	°C
NUMBER OF TRANSISTORS		65			65			65		

NOTES
[1]Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced.
[2]Error vs. crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width = 200μs.
[3]Input voltages are expressed in volts rms, and error is percent of reading.
[4]With 2k external pulldown resistor.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
- Dual Supply . . . . . ±18V
- Single Supply . . . . . +36V

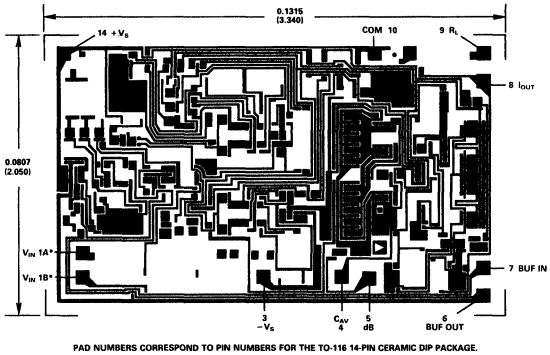
Internal Power Dissipation[2] 500mW
Maximum Input Voltage . . . . . ±25V Peak
Buffer Maximum Input Voltage . . . . . $\pm V_S$
Maximum Input Voltage . . . . . ±25V Peak
Storage Temperature Range . . . . . −55°C to +150°C
Operating Temperature Range
- AD536AJ/K . . . . . 0 to +70°C
- AD536AS . . . . . −55°C to +125°C

Lead Temperature Range
- (Soldering 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]10-Pin Header: θ_{JA} = 150°C/W
20-Pin LCC: θ_{JA} = 95°C/W
14-Pin Size Brazed Ceramic DIP: θ_{JA} = 95°C/W

CHIP DIMENSIONS AND PAD LAYOUT

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14-PIN CERAMIC DIP PACKAGE.

NOTE
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.
THE AD536A IS AVAILABLE IN LASER TRIMMED CHIP FORM.
SUBSTRATE CONNECTED TO $-V_S$.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
AD536AJD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AKD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD536AJH	0°C to +70°C	Header	H-10A
AD536AKH	0°C to +70°C	Header	H-10A
AD536AJQ	0°C to +70°C	Cerdip	Q-14
AD536AKQ	0°C to +70°C	Cerdip	Q-14
AD536ASD	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASD/883B	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD536ASE	−55°C to +125°C	LCC	E-20A
AD536ASE/883B	−55°C to +125°C	LCC	E-20A
AD536ASH	−55°C to +125°C	Header	H-10A
AD536ASH/883B	−55°C to +125°C	Header	H-10A

NOTES
[1]"S" grade chips are available tested at +25°C and +125°C. "J" grade chips are also available.
[2]For outline information see Package Information section.

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%; at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with the input, as shown in Figure 3, the capacitor must be nonpolar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

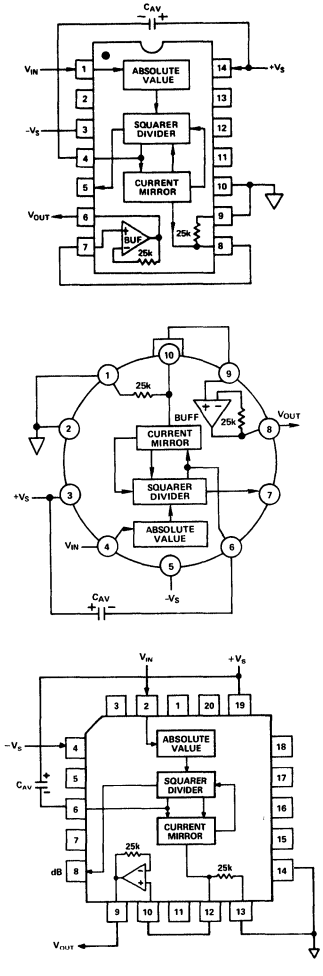


Figure 1. Standard RMS Connection

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 14. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25k resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25k resistor from ground. The output current is available at Pin 8 (Pin 10 on the "H" package) with a nominal scale of 40μA per volt rms input positive out.

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. Note that the offset trim circuit adds 365Ω in series with the internal 25kΩ resistor. This will cause a 1.5% increase in scale factor, which is trimmed out by using R_1 as shown. Range of scale factor adjustment is ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R4 to give zero volts output from Pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from Pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a ±1.000V peak-to-peak sine wave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full-scale range.

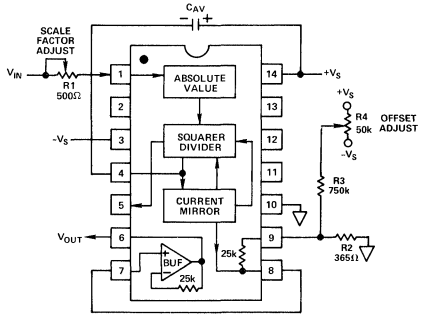


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at Pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 μA of current flows into Pin 10 (Pin 2 on the "H" package). AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 16.7kΩ; for a cut-off at 10Hz, C_2 should be 1μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 14. The load resistor, R_L, is necessary to provide output sink current.

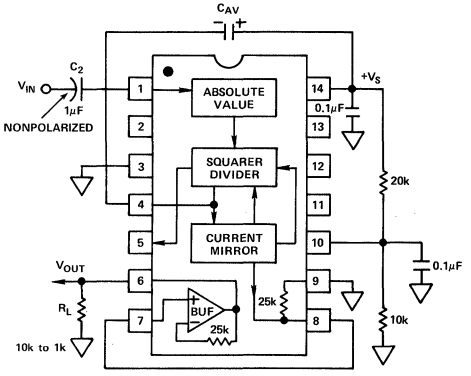


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly varying dc signal, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by a dc (or average) error and some amount of ripple, as demonstrated in Figure 4.

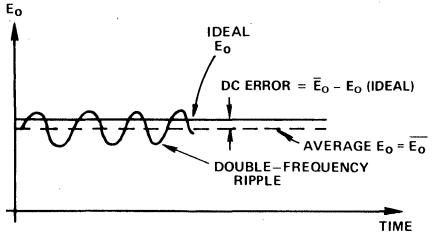


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield a given percent dc error above a given frequency using the standard rms connection.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and 1% settling time is 115 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

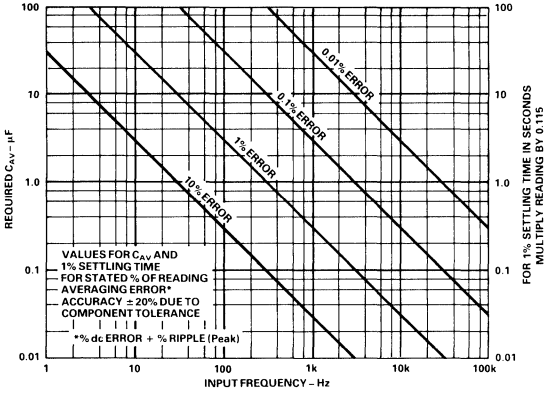


Figure 5. Error/Settling Time Graph for Use with the Standard RMS Connection in Figure 1

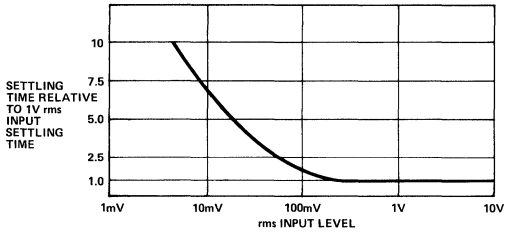


Figure 6. Settling Time vs. Input Level

A better method for reducing output ripple is the use of a "post-filter." Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8 and settling time is increased. For example, with C_{AV} = 1µF and C_2 = 2.2µF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explanation of these topics refer to the *RMS to DC Conversion Application Guide 2nd Edition*, available from Analog Devices.

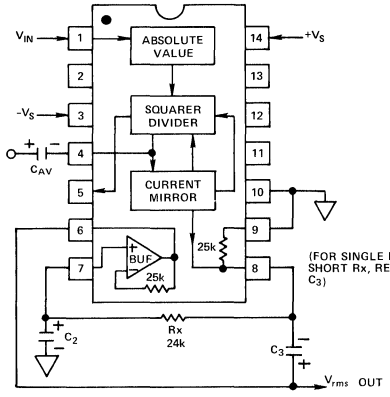


Figure 7. 2-Pole "Post" Filter

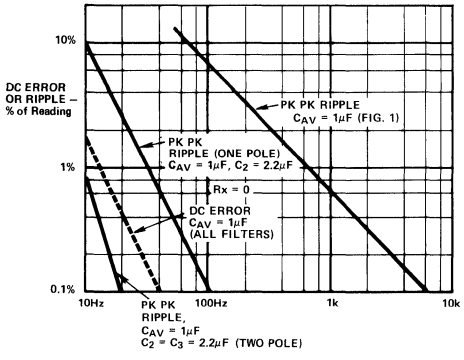


Figure 8. Performance Features of Various Filter Types

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V_{rms} = Avg.\left[\frac{V_{IN}^2}{V_{rms}}\right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2/I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = Avg.\ [I_1^2/I_4] = I_1\ rms$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2\ I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q3, since the voltage at this point is proportional to $-\log V_{IN}$. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

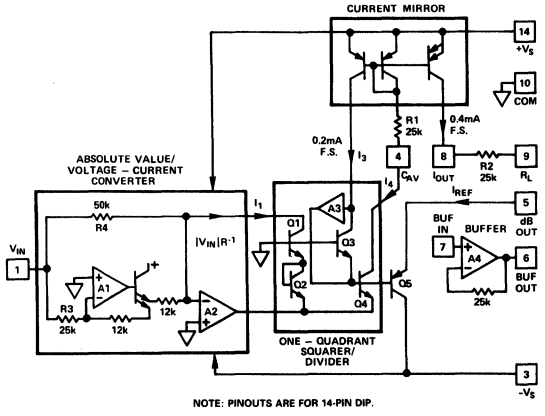


Figure 9. Simplified Schematic

CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A is the logarithmic or decibel output. The internal circuit computing dB works accurately over a 60dB range. The connections for dB measurements are shown in Figure 10. The user selects the 0dB level by adjusting R_1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the +0.33%/°C scale factor drift of the dB output pin. The special T.C. resistor, R_2, is available from Tel Labs in Londonderry, N.H. (Model Q-81) or from Precision Resistor Inc., Hillside, N.J. (model PT146). The averaged temperature coefficients of resistors R_2 and R_3 develop the +3300ppm needed to reverse compensate the dB output. The linear rms output is available at Pin 8 on DIP or Pin 10 on header device with an output impedance of 25kΩ; thus some applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00V dc or 1.00V rms
2. Adjust R_1 for dB out = 0.00V
3. Set V_{IN} = +0.1V dc or 0.10V rms
4. Adjust R_5 for dB out = −2.00V

Any other desired 0dB reference level can be used by setting V_{IN} and adjusting R_1 accordingly. Note that adjusting R_5 for the proper gain automatically gives the correct temperature compensation.

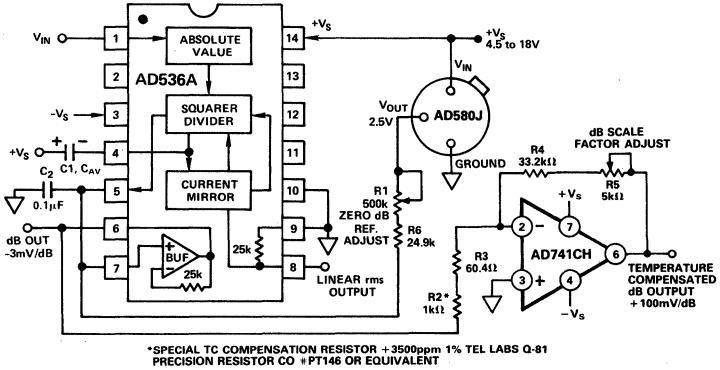


Figure 10. dB Connection

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 7 volts rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 120kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to only 5kHz.

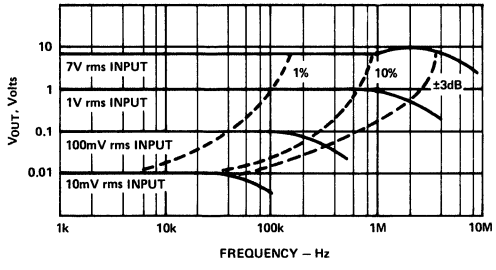


Figure 11. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (C.F. = V_p/Vrms). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 12 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 11 while maintaining a constant 1 volt rms input amplitude.

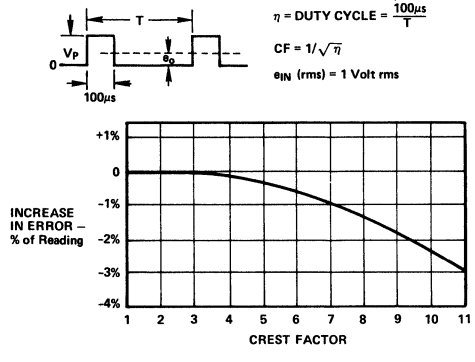


Figure 12. Error vs. Crest Factor

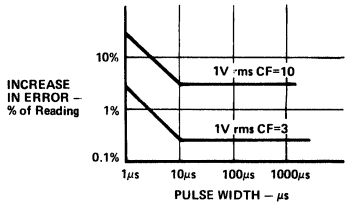
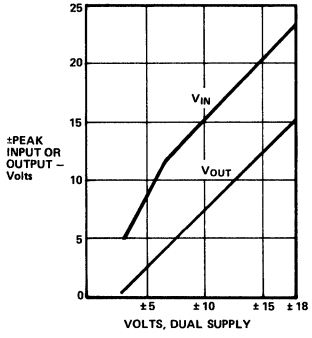


Figure 13. AD536A Error vs. Pulse Width Rectangular Pulse



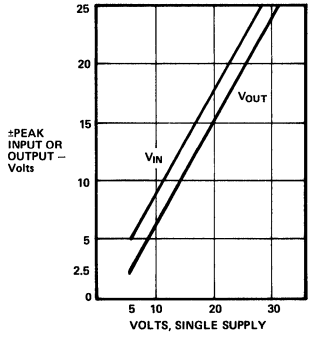


Figure 14. AD536A Input and Output Voltage Ranges vs. Supply

ANALOG DEVICES

Low Level, True RMS-to-DC Converter

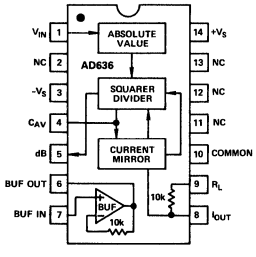
AD636

FEATURES

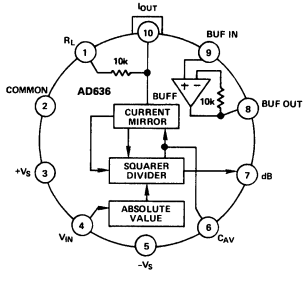
- True rms-to-dc Conversion
- 200mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.5% max Error (AD636K)
  - 1.0% max Error (AD636J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 1MHz -3dB Bandwidth: V_{rms}>100mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50dB Range
- Low Power: 800μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- Low Cost
- Available in Chip Form

PIN CONNECTIONS & FUNCTIONAL BLOCK DIAGRAM

"D" Package (TO-116)



"H" Package (TO-100)



PRODUCT DESCRIPTION

The AD636 is a low power monolithic IC which performs true rms-to-dc conversion on low level signals. It offers performance which is comparable or superior to that of hybrid and modular converters costing much more. The AD636 is specified for a signal range of 0 to 200 millivolts rms. Crest factors up to 6 can be accommodated with less than 0.5% additional error, allowing accurate measurement of complex input waveforms.

The low power supply current requirement of the AD636, typically 800μA, allows it to be used in battery-powered portable instruments. A wide range of power supplies can be used, from ±2.5V to ±16.5V or a single +5V to +24V supply. The input and output terminals are fully protected; the input signal can exceed the power supply with no damage to the device (allowing the presence of input signals in the absence of supply voltage) and the output buffer amplifier is short-circuit protected.

The AD636 includes an auxiliary dB output. This signal is derived from an internal circuit point which represents the logarithm of the rms output. The 0dB reference level is set by an externally supplied current and can be selected by the user to correspond to any input level from 0dBm (774.6mV) to -20dBm (77.46mV). Frequency response ranges from 1.2MHz at a 0dBm level to over 10kHz at -50dBm.

The AD636 is designed for ease of use. The device is factory-trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full scale accuracy at 200mV rms. Thus no external trims are required to achieve full rated accuracy.

AD636 is available in two accuracy grades; the AD636J total error of ±0.5mV ±0.06% of reading, and the AD636K is accurate within ±0.2mV to ±0.03% of reading. Both versions are specified for the 0 to +70°C temperature range, and are offered in either a hermetically sealed 14-pin DIP or a 10-pin TO-100 metal can. Chips are also available.

PRODUCT HIGHLIGHTS

1. The AD636 computes the true root-mean-square of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it is a measure of the power in the signal. The rms value of an ac-coupled signal is also its standard deviation.
2. The 200 millivolt full scale range of the AD636 is compatible with many popular display-oriented analog-to-digital converters. The low power supply current requirement permits use in battery-powered hand-held instruments.
3. The only external component required to perform measurements to the fully specified accuracy is the averaging capacitor. The value of this capacitor can be selected for the desired trade-off of low frequency accuracy, ripple, and settling time.
4. The on-chip buffer amplifier can be used to buffer either the input or the output. Used as an input buffer, it provides accurate performance from standard 10MΩ input attenuators. As an output buffer, it can supply up to 5 milliamps of output current.
5. The AD636 will operate over a wide range of power supply voltages, including single +5V to +24V or split ±2.5V to ±16.5V sources. A standard 9V battery will provide several hundred hours of continuous operation.

AD636—SPECIFICATIONS (@ +25°C, and $+V_S$ = +3V, $-V_S$ = −5V unless otherwise noted)

Model	AD636J Min	AD636J Typ	AD636J Max	AD636K Min	AD636K Typ	AD636K Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY							
Total Error, Internal Trim[1,2]			**±0.5 ±1.0**			**±0.2 ±0.5**	mV ± % of Reading
vs. Temperature, 0 to +70°C			±0.1 ±0.01			±0.1 ±0.005	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error at 200mV		±0.2			±0.1		% of Reading
Total Error, External Trim[1]		±0.3 ±0.3			±0.1 ±0.2		mV ± % of Reading
ERROR VS. CREST FACTOR[3]							
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.2			−0.2		% of Reading
Crest Factor = 6		−0.5			−0.5		% of Reading
AVERAGING TIME CONSTANT		25			25		ms/μF CAV
INPUT CHARACTERISTICS							
Signal Range, All Supplies							
Continuous rms Level		0 to 200			0 to 200		mV rms
Peak Transient Inputs							
+3V, −5V Supply			±2.8			±2.8	V pk
±2.5V Supply			±2.0			±2.0	V pk
±5V Supply			±5.0			±5.0	V pk
Maximum Continuous Non-Destructive							
Input Level (All Supply Voltages)			±12			±12	V pk
Input Resistance	5.33	6.67	8	5.33	6.67	8	kΩ
Input Offset Voltage			±0.5			±0.2	mV
FREQUENCY RESPONSE[2,4]							
Bandwidth for 1% additional error (0.09dB)							
V_{IN} = 10mV		14			14		kHz
V_{IN} = 100mV		90			90		kHz
V_{IN} = 200mV		130			130		kHz
±3dB Bandwidth							
V_{IN} = 10mV		100			100		kHz
V_{IN} = 100mV		900			900		kHz
V_{IN} = 200mV		1.5			1.5		MHz
OUTPUT CHARACTERISTICS[2]							
Offset Voltage, V_{IN} = COM			**±0.5**			**±0.2**	mV
vs. Temperature		±10			±10		μV/°C
vs. Supply		±0.1			±0.1		mV/V
Voltage Swing							
+3V, −5V Supply	0.3	0 to +1.0		0.3	0 to +1.0		V
±5V to ±16.5V Supply	0.3	0 to +1.0		0.3	0 to +1.0		V
Output Impedance	8	10	12	8	10	12	kΩ
dB OUTPUT							
Error, V_{IN} = 7mV to 300mV rms		±0.3	**±0.5**		±0.1	**±0.2**	dB
Scale Factor		−3.0			−3.0		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33		% of Reading/°C
		−0.033			−0.033		dB/°C
I_{REF} for 0dB = 0.1V rms	**2**	4	**8**	**2**	4	**8**	μA
I_{REF} Range	1		50	1		50	μA
I_{OUT} TERMINAL							
I_{OUT} Scale Factor		100			100		μA/V rms
I_{OUT} Scale Factor Tolerance	−20	±10	+20	−20	±10	+20	%
Output Resistance	8	10	12	8	10	12	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2V)			$-V_S$ to ($+V_S$ −2V)		V
BUFFER AMPLIFIER							
Input and Output Voltage Range	$-V_S$ to ($+V_S$ −2V)			$-V_S$ to ($+V_S$ −2V)			V
Input Offset Voltage, R_S = 10k		±0.8	**±2**		±0.5	**±1**	mV
Input Bias Current		100	**300**		100	**300**	nA
Input Resistance		10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			
Short Circuit Current		20			20		mA
Small Signal Bandwidth		1			1		MHz
Slew Rate[5]		5			5		V/μs
POWER SUPPLY							
Voltage, Rated Performance		+3, −5			+3, −5		V
Dual Supply	+2, −2.5		±16.5	+2, −2.5		±16.5	V
Single Supply	+5		+24	+5		+24	V
Quiescent Current[6]		0.80	**1.00**		0.80	**1.00**	mA

TEMPERATURE RANGE					
Rated Performance	0	+70	0	+70	°C
Storage	−55	+150	−55	+150	°C
TRANSISTOR COUNT	62		62		

NOTES
[1]Accuracy specified for 0 to 200mV rms, dc or 1kHz sinewave input. Accuracy is degraded at higher rms signal levels.
[2]Measured at pin 8 of DIP (I_{OUT}), with pin 9 tied to common.
[3]Error vs. crest factor is specified as additional error for a 200mV rms rectangular pulse train, pulse width = 200μs.
[4]Input voltages are expressed in volts rms.
[5]With 10kΩ pull down resistor from pin 6 (BUF OUT) to $-V_S$.
[6]With BUF input tied to Common.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications shown in **boldface** are tested on all production units at final electrical test are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage
- Dual Supply . . . . . ±16.5 V
- Single Supply . . . . . +24 V

Internal Power Dissipation[2] . . . . . 500 mW
Maximum Input Voltage . . . . . ±12 V Peak
Storage Temperature Range . . . . . −55°C to +150°C
Operating Temperature Range
- AD636J/K . . . . . 0 to +70°C

Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation ofthe device at these or anyother conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]10-Pin Header: θ_{JA} = 150°C/W.
14-Pin Sidebrazed Ceramic DIP: θ_{JA} = 95°C/W.

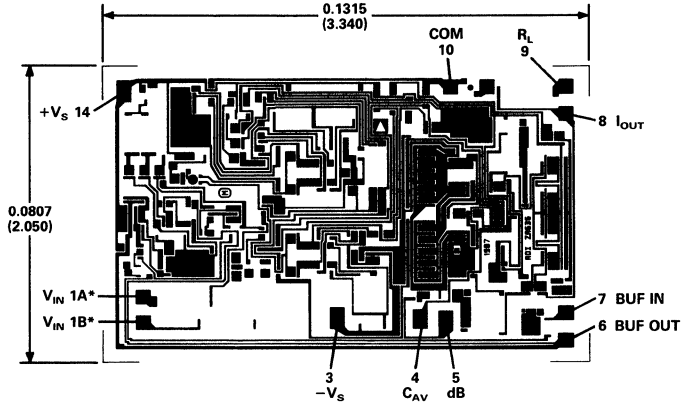
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD636JD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD636KD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD636JH	0°C to +70°C	Header	H-10A
AD636KH	0°C to +70°C	Header	H-10A
AD636J Chip	0°C to +70°C	Chip	
AD636K Chip	0°C to +70°C	Chip	

*For outline information see Package Information section.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14-PIN CERAMIC DIP PACKAGE.

NOTE
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.

STANDARD CONNECTION

The AD636 is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD636 will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD636 is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible. C_F is an optional output ripple filter, as discussed elsewhere in this data sheet.

The input and output signal ranges are a function of the supply voltages as detailed in the specifications. The AD636 can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 10k resistor. The buffer amplifier can then be used for other purposes. Further, the AD636 can be used in a current output mode by disconnecting the 10k resistor from the ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 100μA per volt rms input, positive out.

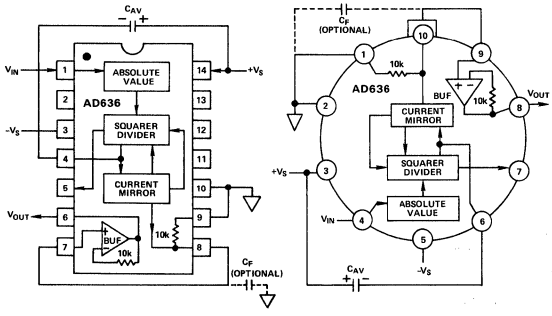


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD636, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. The scale factor is trimmed by using R_1 as shown. The insertion of R_2 allows R_1 to either increase or decrease the scale factor by ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 200mV dc input should give 200mV dc output. Of course, a ±200mV peak-to-peak sinewave should give a 141.4mV dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 assume the use of dual power supplies. The AD636 can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. Figure 3 is optimized for use with a 9 volt battery. The major limitation of this connection is that only ac signals can be measured since the input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 1 microamp of current flows into pin 10 (pin 2 on the "H" package). Alternately, the COM pin of some CMOS ADCs provides a suitable artificial ground for the AD636. AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 6.7kΩ; for a cut-off at 10Hz, C_2 should be 3.3μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The load resistor, R_L, is necessary to provide current sinking capability.

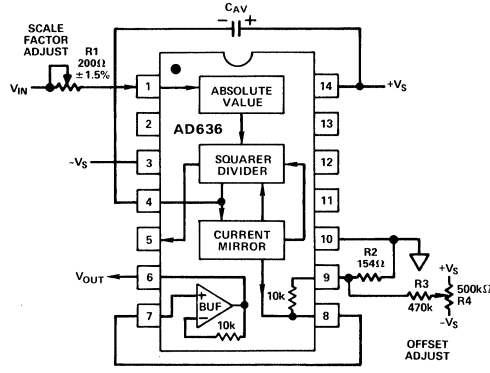


Figure 2. Optional External Gain and Output Offset Trims

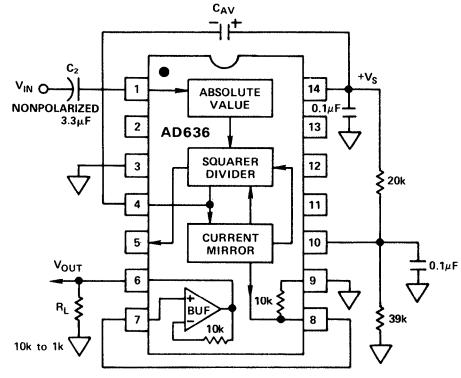


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD636 will compute the rms of both ac and dc signals. If the input is a slowly-varying dc voltage, the output of the AD636 will track the input exactly. At higher frequencies, the average output of the AD636 will approach the rms value of the input signal. The actual output of the AD636 will differ from the ideal output by a dc (or average) error and some amount of ripple, as demonstrated in Figure 4.

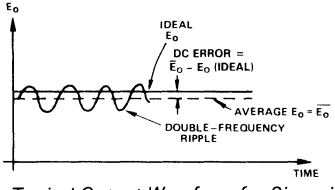


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield a given % dc error above a given frequency using the standard rms connection.

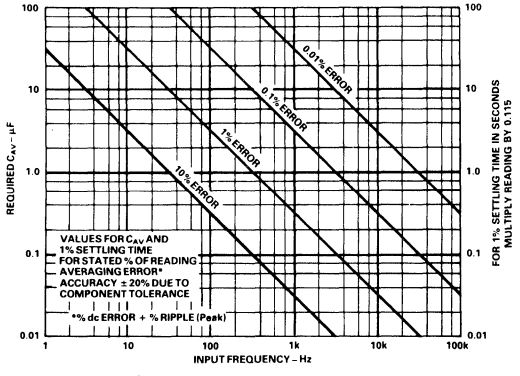


Figure 5. Error/Settling Time Graph for Use with the Standard rms Connection

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4µF capacitor (time constant = 25ms per µF).

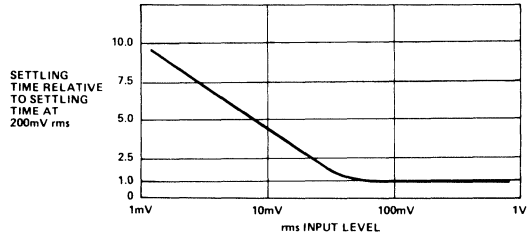


Figure 6. Settling Time vs. Input Level

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows the the relationship between C_{AV} and 1% settling time is 115 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately 5 times the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1µF and C_2 = 4.7µF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

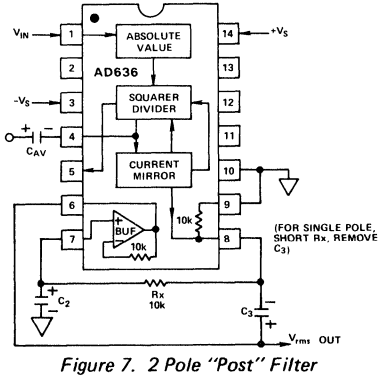


Figure 7. 2 Pole "Post" Filter

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explaination of these topics refer to the ***RMS-to-DC Conversion Application Guide, 2nd Edition,*** available from Analog Devices.

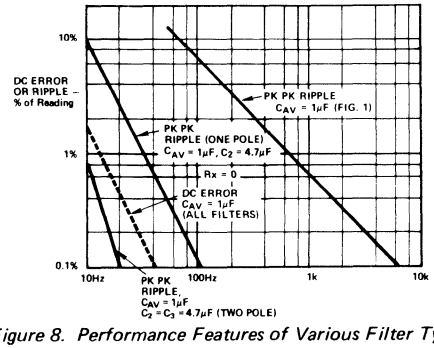


Figure 8. Performance Features of Various Filter Types

AD636—RMS Measurement

AD636 PRINCIPLE OF OPERATION

The AD636 embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD636 follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD636; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.} [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD636 thus results:

$$V_{OUT} = 2R_2 I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to -log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

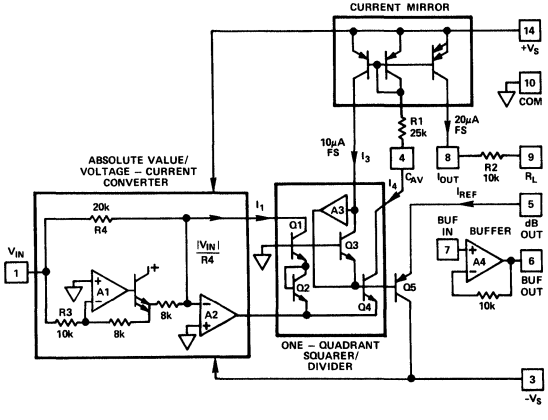


Figure 9. Simplified Schematic

THE AD636 BUFFER AMPLIFIER

The buffer amplifier included in the AD636 offers the user additional application flexibility. It is important to understand some of the characteristics of this amplifier to obtain optimum performance. Figure 10 shows a simplified schematic of the buffer.

Since the output of an rms-to-dc converter is always positive, it is not necessary to use a traditional complementary Class AB output stage. In the AD636 buffer, a Class A emitter follower is used instead. In addition to excellent positive output voltage swing, this configuration allows the output to swing fully down to ground in single-supply applications without the problems associated with most IC operational amplifiers.

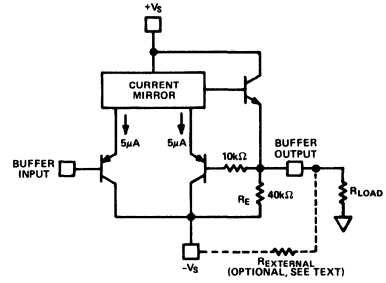


Figure 10. AD636 Buffer Amplifier Simplified Schematic

When this amplifier is used in dual-supply applications as an input buffer amplifier driving a load resistance referred to ground, steps must be taken to insure an adequate negative voltage swing. For negative outputs, current will flow from the load resistor through the 40kΩ emitter resistor, setting up a voltage divider between $-V_S$ and ground. This reduced effective $-V_S$ will limit the available negative output swing of the buffer. Addition of an external resistor in parallel with R_E alters this voltage divider such that increased negative swing is possible.

Figure 11 shows the value of $R_{EXTERNAL}$ for a particular ratio of V_{PEAK} to $-V_S$ for several values of R_{LOAD}. Addition of $R_{EXTERNAL}$ increases the quiescent current of the buffer amplifier by an amount equal to $R_{EXT}/-V_S$. Nominal buffer quiescent current with no $R_{EXTERNAL}$ is 30μA at $-V_S$ = -5V.

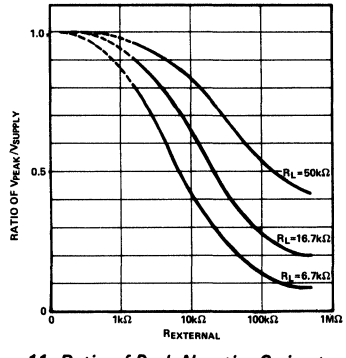


Figure 11. Ratio of Peak Negative Swing to $-V_S$ vs. $R_{EXTERNAL}$ for Several Load Resistances

FREQUENCY RESPONSE

The AD636 utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD636 at input levels from 1 millivolt to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and ±3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 220kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to 14kHz.

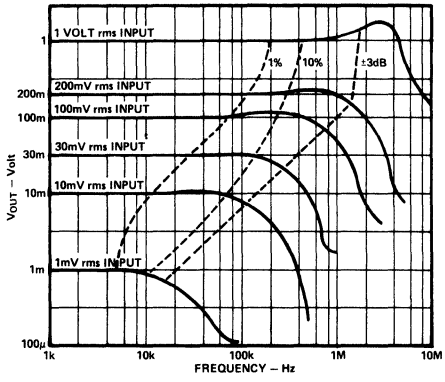


Figure 12. AD636 Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 13 is a curve of reading error for the AD636 for a 200mV rms input signal with crest factors from 1 to 7. A rectangular pulse train (pulse width 200μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 7 while maintaining a constant 200mV rms input amplitude.

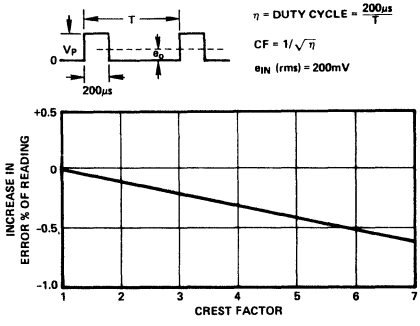


Figure 13. Error vs. Crest Factor

A COMPLETE AC DIGITAL VOLTMETER

Figure 14 shows a design for a complete low power ac digital voltmeter circuit based on the AD636. The 10MΩ input attenuator allows full scale ranges of 200mV, 2V, 20V and 200V rms. Signals are capacitively coupled to the AD636 buffer amplifier, which is connected in an ac bootstrapped configuration to minimize loading. The buffer then drives the 6.7kΩ input impedance of the AD636. The COM terminal of the ADC chip provides the false ground required by the AD636 for single supply operation. An AD589 1.2 volt reference diode is used to provide a stable 100 millivolt reference for the ADC in the linear rms mode; in the dB mode, a 1N4148 diode is inserted in series to provide correction for the temperature coefficient of the dB scale factor. Calibration of the meter is done by first adjusting offset pot R17 for a proper zero reading, then adjusting the R13 for an accurate readout at full scale.

Calibration of the dB range is accomplished by adjusting R9 for the desired 0dB reference point, then adjusting R14 for the desired dB scale factor (a scale of 10 counts per dB is convenient).

Total power supply current for this circuit is typically 2.8mA using a 7106-type ADC.

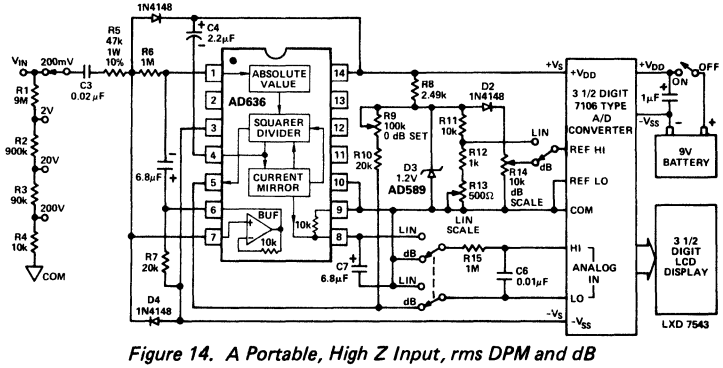


Figure 14. A Portable, High Z Input, rms DPM and dB Meter Circuit

A LOW POWER, HIGH INPUT IMPEDANCE dB METER

Introduction

The portable dB meter circuit featured here combines the functions of the AD636 rms converter, the AD589 voltage reference, and a μA776 low power operational amplifier. This meter offers excellent bandwidth and superior high and low level accuracy while consuming minimal power from a standard 9 volt transistor radio battery.

In this circuit, the built-in buffer amplifier of the AD636 is used as a "bootstrapped" input stage increasing the normal 6.7kΩ input Z to an input impedance of approximately $10^{10}\Omega$.

Circuit Description

The input voltage, V_{IN}, is ac coupled by C_4 while resistor R_8, together with diodes D_1 and D_2, provide high input voltage protection.

The buffer's output, pin 6, is ac coupled to the rms converter's input (pin 1) by capacitor C_2. Resistor R_9 is connected between the buffer's output, a Class A output stage, and the negative output swing. Resistor R_1 is the amplifier's "bootstrapping" resistor.

With this circuit, single supply operation is made possible by setting "ground" at a point between the positive and negative sides of the battery. This is accomplished by sending 250μA from the positive battery terminal through resistor R_2, then through the 1.2 volt AD589 bandgap reference, and finally back to the negative side of the battery via resistor R_{10}. This sets ground at 1.2 volts +3.18 volts (250μA × 12.7kΩ) = 4.4 volts below the positive battery terminal and 5.0 volts (250μA × 20kΩ) above the negative battery terminal. Bypass capacitors C_3 and C_5 keep both sides of the battery at a low ac impedance to ground. The AD589 bandgap reference establishes the 1.2 volt regulated reference voltage which together with resistor R_3 and trimming potentiometer R_4 set the zero dB reference current I_{REF}.

Performance Data

0dB Reference Range = 0dBm (770mV) to −20dBm (77mV) rms

0dBm = 1 milliwatt in 600Ω
Input Range (at I_{REF} = 770mV) = 50dBm
Input Impedance = approximately $10^{10}\Omega$
V_{SUPPLY} Operating Range +5V dc to +20V dc
$I_{QUIESCENT}$ = 1.8mA typical

Accuracy with 1kHz sinewave and 9 volt dc supply:
0dB to −40dBm ±0.1dBm
0dBm to −50dBm ±0.15dBm
+10dBm to −50dBm ±0.5dBm

Frequency Response ±3dBm:
Input
0dBm = 5Hz to 380kHz
−10dBm = 5Hz to 370kHz
−20dBm = 5Hz to 240kHz
−30dBm = 5Hz to 100kHz
−40dBm = 5Hz to 45kHz
−50dBm = 5Hz to 17kHz

Calibration

1. First calibrate the zero dB reference level by applying a 1kHz sinewave from an audio oscillator at the desired zero dB amplitude. This may be anywhere from zero dBm (770mV rms – 2.2 volts p–p) to −20dBm (77mV rms 220mV – p–p). Adjust the I_{REF} cal trimmer for a zero indication on the analog meter.
2. The final step is to calibrate the meter scale factor or gain. Apply an input signal −40dB below the set zero dB reference and adjust the scale factor calibration trimmer for a 40μA reading on the analog meter.

The temperature compensation resistors for this circuit may be purchased from: *Tel Labs Inc.*, 154 Harvey Road, P.O. Box 375, Londonderry, NH 03053, Part #Q332A 2kΩ 1% +3500ppm/°C or from *Precision Resistor Company*, 109 U.S. Highway 22, Hillside, NJ 07205, Part #PT146 2kΩ 1% +3500ppm/°C.

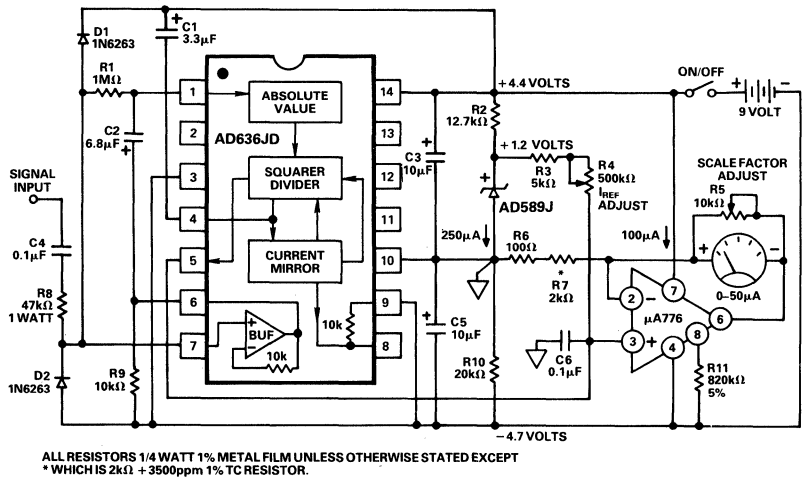


Figure 15. A Low Power, High Input Impedance dB Meter

High Precision, Wideband RMS-to-DC Converter

AD637

FEATURES

High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V RMS Input**
- **0.10% Additional Error to Crest Factor of 3**

Wide Bandwidth
- **8MHz at 1V RMS Input**
- **600kHz at 100mV RMS**

Computes:
- **True RMS**
- **Square**
- **Mean Square**
- **Absolute Value**

dB Output (60dB Range)

Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiescent Current Reduction from 2.2mA to 350μA**

Side Brazed DIP, Low-Cost Cerdip and SOIC

PRODUCT DESCRIPTION

The AD637 is a complete high accuracy monolithic rms to dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms to dc converters and comparable to discrete and modular techniques in accuracy, bandwidth and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signals up to 600kHz with inputs of 200mV rms and up to 8MHz when the input levels are above 1V rms.

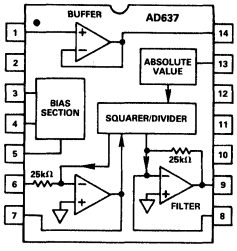
As with previous monolithic rms converters from Analog Devices, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin allowing direct dB measurement with a useful range of 60dB. An externally programmed reference current allows the user to select the 0dB reference voltage to correspond to any level between 0.1V and 2.0V rms.

A chip select connection on the AD637 permits the user to decrease the supply current from 2.2mA to 350μA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition when the AD637 is powered down the output goes to a high impedance state. This allows several AD637s to be tied together to form a wide-band true rms multiplexer.

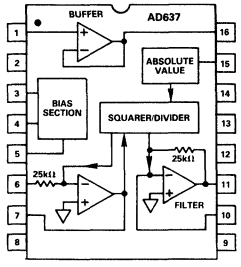
The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs will not be damaged by input signals if the supply voltages are lost.

FUNCTIONAL BLOCK DIAGRAMS

Ceramic DIP (D) and Cerdip (Q) Package



SOIC (R) Package



The AD637 is available in two accuracy grades (J, K) for commercial (0 to +70°C) temperature range applications and one (S) rated over the −55°C to +125°C temperature range. All versions are available in hermetically-sealed, 14-pin side-brazed ceramic DIPs as well as low-cost cerdip packages. A 16-pin SOIC package is also available.

PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square, mean square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.
2. The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor which sets the averaging time period. The value of this capacitor also determines low frequency accuracy, ripple level and settling time.
3. The chip select feature of the AD637 permits the user to power down the device down during periods of nonuse, thereby, decreasing battery drain in remote or hand-held applications.
4. The on-chip buffer amplifier can be used as either an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby, increasing the accuracy of the measurement.

AD637—SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted.)

Model	AD637J			AD637K			AD637S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Fig. 2)			±1 ±0.5			±0.5±0.2			±1 ±0.5	mV ± % of Reading
T_{min} to T_{max}			±3.0 ±0.6			±2.0 ±0.3			±6 ±0.7	mV ± % of Reading
vs. Supply, + V_{IN} = + 300mV		30	150		30	150		30	150	µV/V
vs. Supply, − V_{IN} = − 300mV		100	300		100	300		100	300	µV/V
dc Reversal Error at 2V			0.25			0.1			0.25	% of Reading
Nonlinearity 2V Full Scale[2]			0.04			0.02			0.04	% of FSR
Nonlinearity 7V Full Scale			0.05			0.05			0.05	% of FSR
Total Error, External Trim		±0.5 ±0.1			±0.25 ±0.05			±0.5 ±0.1		mV ± % of Reading
ERROR VS. CREST FACTOR[3]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		±0.1			±0.1			±0.1		% of Reading
Crest Factor = 10		±1.0			±1.0			±1.0		% of Reading
AVERAGING TIME CONSTANT		25			25			25		ms/µF C_{AV}
INPUT CHARACTERISTICS										
Signal Range, ± 15V Supply										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±15			±15			±15	V p-p
Signal Range, ± 5V Supply										
Continuous rms Level		0 to 4			0 to 4			0 to 4		V rms
Peak Transient Input			±6			±6			±6	V p-p
Maximum Continuous Non-Destructive Input Level (All Supply Voltages)			±15			±15			±15	V p-p
Input Resistance	6.4	8	9.6	6.4	8	9.6	6.4	8	9.6	kΩ
Input Offset Voltage			±0.5			±0.2			±0.5	mV
FREQUENCY RESPONSE[4]										
Bandwidth for 1% additional error (0.09dB)										
V_{IN} = 20mV		11			11			11		kHz
V_{IN} = 200mV		66			66			66		kHz
V_{IN} = 2V		200			200			200		kHz
± 3dB Bandwidth										
V_{IN} = 20mV		150			150			150		kHz
V_{IN} = 200mV		1			1			1		MHz
V_{IN} = 2V		8			8			8		MHz
OUTPUT CHARACTERISTICS										
Offset Voltage			±1			±0.5			±1	mV
vs. Temperature		±0.05	±0.089		±0.04	±0.056		±0.04	±0.07	mV/°C
Voltage Swing, ± 15V Supply, 2kΩ Load	0 to +12.0	+13.5		0 to +12.0	+13.5		0 to +12.0	+13.5		V
Voltage Swing, ± 3V Supply, 2kΩ Load	0 to +2	+2.2		0 to +2	+2.2		0 to +2	+2.2		V
Output Current	6			6			6			mA
Short Circuit Current		20			20			20		mA
Resistance, Chip Select "High"		0.5			0.5			0.5		Ω
Resistance, Chip Select "Low"		100			100			100		kΩ
dB OUTPUT										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.5			±0.3			±0.5		dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33			+0.33		% of Reading/°C
		−0.033			−0.033			−0.033		dB/°C
I_{REF} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	µA
I_{REF} Range	1		100	1		100	1		100	µA
BUFFER AMPLIFIER										
Input and Output Voltage Range	−V_S to (+V_S −2.5V)			−V_S to (+V_S −2.5V)			−V_S to (+V_S −2.5V)			V
Input Offset Voltage		±0.8	±2		±0.5	±1		±0.8	±2	mV
Input Current		±2	±10		±2	±5		±2	±10	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130µA)			(+5mA, −130µA)			(+5mA, −130µA)			
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[5]		5			5			5		V/µs
DENOMINATOR INPUT										
Input Range		0 to +10			0 to +10			0 to +10		V
Input Resistance	20	25	30	20	25	30	20	25	30	kΩ
Offset Voltage		±0.2	±0.5		±0.2	±0.5		±0.2	±0.5	mV
CHIP SELECT PROVISION (CS)										
rms "ON" Level		Open or +2.4V<V_C<+V_S			Open or +2.4V<V_C<+V_S			Open or +2.4V<V_C<+V_S		
rms "OFF" Level		V_C<+0.2V			V_C<+0.2V			V_C<+0.2V		
I_{OUT} of Chip Select										
CS "LOW"		10			10			10		µA
CS "HIGH"		Zero			Zero			Zero		
On Time Constant		10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})		
Off Time Constant		10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})		
POWER SUPPLY										
Operating Voltage Range	±3.0		±18	±3.0		±18	±3.0		±18	V
Quiescent Current		2.2	3		2.2	3		2.2	3	mA
Standby Current		350	450		350	450		350	450	µA

Model	AD637J Min	AD637J Typ	AD637J Max	AD637K Min	AD637K Typ	AD637K Max	AD637S Min	AD637S Typ	AD637S Max	Units
TRANSISTOR COUNT		107			107			107		

NOTES
[1]Accuracy specified 0-7V rms dc with AD637 connected as shown in Figure 2.
[2]Nonlinearity is defined as the maximum deviation from the straight line connecting the readings at 10mV and 2V.
[3]Error vs. crest factor is specified as additional error for 1V rms.
[4]Input voltages are expressed in volts rms. % are in % of reading.
[5]With external 2kΩ pull down resistor tied to $-V_S$.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

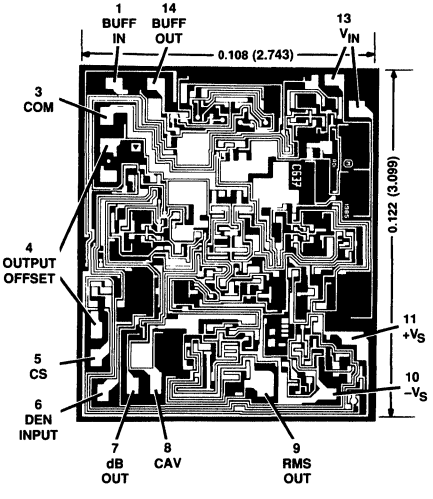
ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option[3]
AD637JD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD637KD	0°C to +70°C	Side Brazed Ceramic DIP	D-14
AD637JQ	0°C to +70°C	Cerdip	Q-14
AD637KQ	0°C to +70°C	Cerdip	Q-14
AD637JR	0°C to +70°C	SOIC	R-16
AD637SD	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD637SD/883B	−55°C to +125°C	Side Brazed Ceramic DIP	D-14
AD637SQ	−55°C to +125°C	Cerdip	Q-14
AD637SQ/883B	−55°C to +125°C	Cerdip	Q-14

NOTES
[1]"J" and "S" grade chips are also available.
[2]Standard Military Drawing, 5962-89637, is also available.
[3]For outline information see Package Information section.

Chip Dimensions and Bonding Diagram

Dimensions shown in inches and (mm).



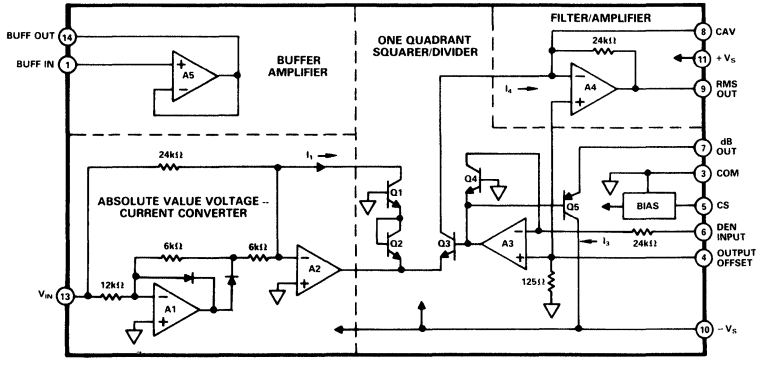


Figure 1. Simplified Schematic

FUNCTIONAL DESCRIPTION

The AD637 embodies an implicit solution of the rms equation that overcomes the inherent limitations of straightforward rms computation. The actual computation performed by the AD637 follows the equation

$$V\ rms = Avg\left[\frac{V_{IN}^2}{V\ rms}\right]$$

Figure 1 is a simplified schematic of the AD637, it is subdivided into four major sections; absolute value circuit (active rectifier), square/divider, filter circuit and buffer amplifier. The input voltage V_{IN} which can be ac or dc is converted to a unipolar current I1 by the active rectifier A1, A2. I1 drives one input of the squarer divider which has the transfer function

$$I_4 = \frac{I_1^2}{I_3}$$

The output current of the squarer/divider, I4 drives A4 which forms a low pass filter with the external averaging capacitor. If the RC time constant of the filter is much greater than the longest period of the input signal than A4s output will be proportional to the average of I4. The output of this filter amplifier is used by A3 to provide the denominator current I3 which equals Avg. I4 and is returned to the squarer/divider to complete the implicit rms computation.

$$I_4 = Avg\left[\frac{I_1^2}{I_4}\right] = I_1\ rms$$

and

$$V_{OUT} = V_{IN}\ rms$$

If the averaging capacitor is omitted the AD637 will compute the absolute value of the input signal. A nominal 5pF capacitor should be used to insure stability. The circuit operates identically to that of the rms configuration except that I3 is now equal to I4 giving

$$I_4 = \frac{I_1^2}{I_4}$$

$$I_4 = |I_1|$$

The denominator current can also be supplied externally by providing a reference voltage, V_{REF}, to pin 6. The circuit operates identically to the rms case except that I3 is now proportional to V_{REF}. Thus:

$$I_4 = Avg\ \frac{I_1^2}{I_3}$$

and

$$V_O = \frac{V_{IN}^2}{V_{DEN}}$$

This is the mean square of the input signal.

STANDARD CONNECTION

The AD637 is simple to connect for a majority of rms measurements. In the standard rms connection shown in Figure 2, only a single external capacitor is required to set the averaging time constant. In this configuration, the AD637 will compute the true rms of any input signal. An averaging error, the magnitude of which will be dependent on the value of the averaging capacitor, will be present at low frequencies. For example, if the filter capacitor C_{AV}, is 4μF this error will be 0.1% at 10Hz and increases to 1% at 3Hz. If it is desired to measure only ac signals the AD637 can be ac coupled through the addition of a nonpolar capacitor in series with the input as shown in Figure 2.

The performance of the AD637 is tolerant of minor variations in the power supply voltages, however, if the supplies being used exhibit a considerable amount of high frequency ripple it is advisable to bypass both supplies to ground through a 0.1μF ceramic disc capacitor placed as close to the device as possible.

The output signal range of the AD637 is a function of the supply voltages, as shown in Figure 3. The output signal can be used buffered or nonbuffered depending on the characteristics of the load. If no buffer is needed, tie buffer input (pin 1) to common. The output of the AD637 is capable of driving 5mA into a 2kΩ load without degrading the accuracy of the device.

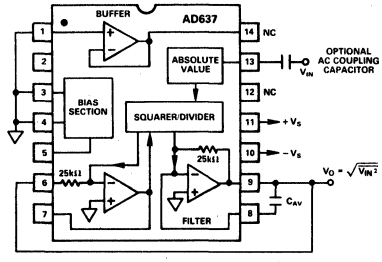


Figure 2. Standard RMS Connection

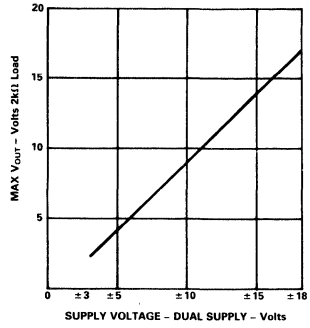


Figure 3. AD637 max V_{OUT} vs. Supply Voltage

CHIP SELECT

The AD637 includes a chip select feature which allows the user to decrease the quiescent current of the device from 2.2mA to 350μA. This is done by driving the CS, pin 5, to below 0.2V dc. Under these conditions, the output will go into a high impedance state. In addition to lowering power consumption, this feature permits bussing the outputs of a number of AD637s to form a wide bandwidth rms multiplexer. If the chip select is not being used, pin 5 should be tied high.

OPTIONAL TRIMS FOR HIGH ACCURACY

The AD637 includes provisions to allow the user to trim out both output offset and scale factor errors. These trims will result in significant reduction in the maximum total error as shown in Figure 4. This remaining error is due to a nontrimmable input offset in the absolute value circuit and the irreducible nonlinearity of the device.

The trimming procedure on the AD637 is as follows:

1. Ground the input signal, V_{IN} and adjust R1 to give 0V output from pin 9. Alternatively R1 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input to V_{IN}, using either a dc or a calibrated ac signal, trim R3 to give the correct output at pin 9, i.e., 1V dc should give 1.000V dc output. Of course, a 2V peak-to-peak sine wave should give 0.707V dc output. Remaining errors are due to the nonlinearity.

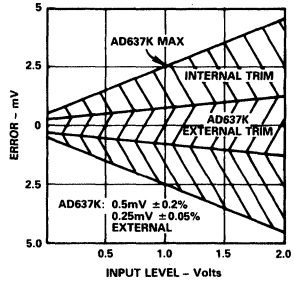


Figure 4. Max Total Error vs. Input Level AD637K Internal and External Trims

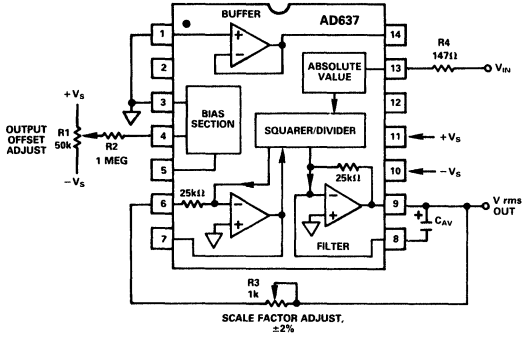


Figure 5. Optional External Gain and Offset Trims

CHOOSING THE AVERAGING TIME CONSTANT

The AD637 will compute the true rms value of both dc and ac input signals. At dc the output will track the absolute value of the input exactly; with ac signals the AD637's output will approach the true rms value of the input. The deviation from the ideal rms value is due to an averaging error. The averaging error is comprised of an ac and dc component. Both components are functions of input signal frequency f, and the averaging time constant τ (τ: 25ms/μF of averaging capacitance). As shown in Figure 6, the averaging error is defined as the peak value of the ac component, ripple, plus the value of the dc error.

The peak value of the ac ripple component of the averaging error is defined approximately by the relationship:

$$\frac{50}{6.3\tau f} \text{ in \% of reading where } (\tau > 1/f)$$

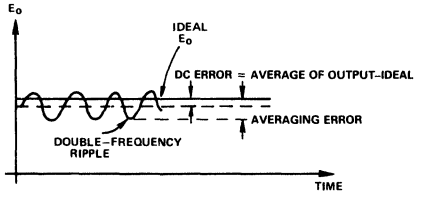


Figure 6. Typical Output Waveform for a Sinusoidal Input

This ripple can add a significant amount of uncertainty to the accuracy of the measurement being made. The uncertainty can be significantly reduced through the use of a post filtering network or by increasing the value of the averaging capacitor.

The dc error appears as a frequency dependent offset at the output of the AD637 and follows the equation:

$$\frac{1}{0.16 + 6.4\tau^2 f^2} \text{ in \% of reading}$$

Since the averaging time constant, set by C_{AV}, directly sets the time that the rms converter "holds" the input signal during computation, the magnitude of the dc error is determined only by C_{AV} and will not be affected by post filtering.

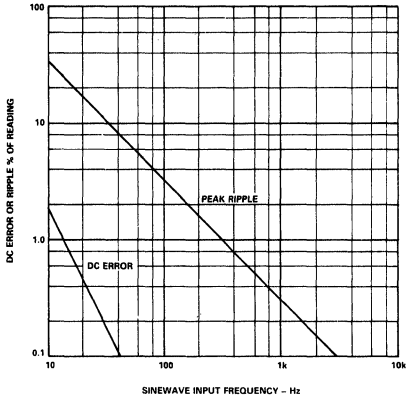


Figure 7. Comparison of Percent dc Error to the Percent Peak Ripple over Frequency Using the AD637 in the Standard RMS Connection with a 1×μF C_{AV}

The ac ripple component of averaging error can be greatly reduced by increasing the value of the averaging capacitor. There are two major disadvantages to this: first, the value of the averaging capacitor will become extremely large and second, the settling time of the AD637 increases in direct proportion to the value of the averaging capacitor (Ts = 115ms/μF of averaging capacitance). A preferrable method of reducing the ripple is through the use of the post filter network, shown in Figure 8. This network can be used in either a one or two pole configuration. For most applications the single pole filter will give the best overall compromise between ripple and settling time.

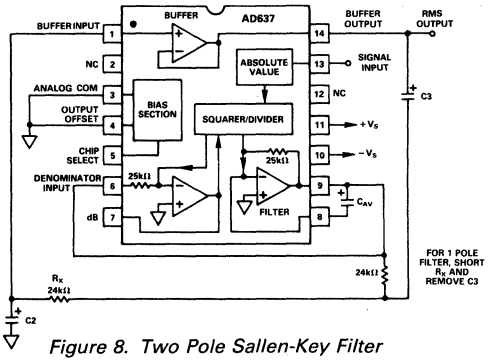


Figure 8. Two Pole Sallen-Key Filter

Figure 9a shows values of C_{AV} and the corresponding averaging error as a function of sine-wave frequency for the standard rms connection. The 1% settling time is shown on the right side of the graph.

Figure 9b shows the relationship between averaging error, signal frequency settling time and averaging capacitor value. This graph is drawn for filter capacitor values of 3.3 times the averaging capacitor value. This ratio sets the magnitude of the ac and dc errors equal at 50Hz. As an example, by using a 1μF averaging capacitor and a 3.3μF filter capacitor the ripple for a 60Hz input signal will be reduced from 5.3% of reading using the averaging capacitor alone to 0.15% using the single pole filter. This gives a factor of thirty reduction in ripple and yet the settling time would only increase by a factor of three. The values of C_{AV} and C_2, the filter capacitor, can be calculated for the desired value of averaging error and settling time by using Figure 9b.

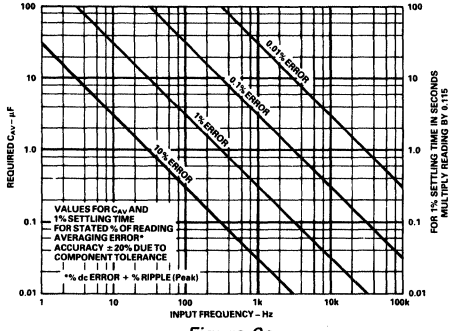


Figure 9a.

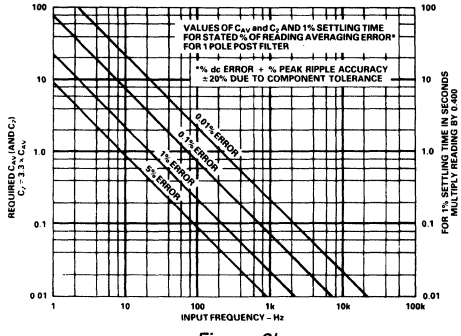


Figure 9b.

The symmetry of the input signal also has an effect on the magnitude of the averaging error. Table I gives practical component values for various types of 60Hz input signals. These capacitor values can be directly scaled for frequencies other than 60Hz, i.e., for 30Hz double these values, for 120Hz they are halved.

	Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum R×CAV Time Constant	Recommended CAV and C2 Values for 1% Averaging Error@ 60Hz with T = 16.6ms		1% Settling Time
				Recommended Standard Value CAV	Recommended Standard Value C2	
A	Symmetrical Sine Wave		1/2T	0.47μF	1.5μF	181ms
B	Sine Wave with dc Offset		T	0.82μF	2.7μF	325ms
C	Pulse Train Waveform		10(T − T2)	6.8μF	22μF	2.67sec
D			10(T − 2T2)	5.6μF	18μF	2.17sec

Table I. Practical Values of C_{AV} and C2 for Various Input Waveforms

For applications that are extremely sensitive to ripple, the two pole configuration is suggested. This configuration will minimize capacitor values and settling time while maximizing performance.

Figure 9c can be used to determine the required value of C_{AV}, C_2 and C_3 for the desired level of ripple and settling time.

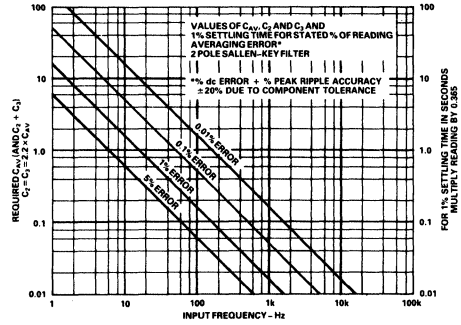


Figure 9c.

FREQUENCY RESPONSE

The frequency response of the AD637 at various signal levels is shown in Figure 10. The dashed lines show the upper frequency limits for 1%, 10% and ± 3dB of additional error. For example, note that for 1% additional error with a 2V rms input the highest frequency allowable is 200kHz. A 200mV signal can be measured with 1% error at signal frequencies up to 100kHz.

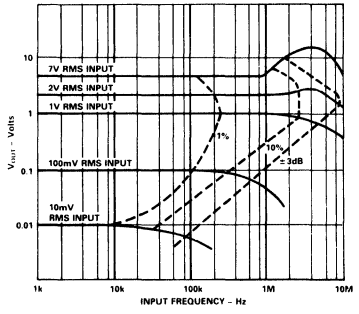


Figure 10. Frequency Response

To take full advantage of the wide bandwidth of the AD637 care must be taken in the selection of the input buffer amplifier. To insure that the input signal is accurately presented to the converter, the input buffer must have a −3dB bandwidth that is wider than that of the AD637. A point that should not be overlooked is the importance of slew rate in this application. For example, the minimum slew rate required for a 1V rms 5MHz sine-wave input signal is 44V/μs. The user is cautioned that this is the minimum rising or falling slew rate and that care must be exercised in the selection of the buffer amplifier as some amplifiers exhibit a two-to-one difference between rising and falling slew rates. The AD845 is recommended as a precision input buffer.

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (≤2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

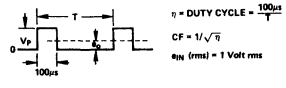


Figure 12 is a curve of additional reading error for the AD637 for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

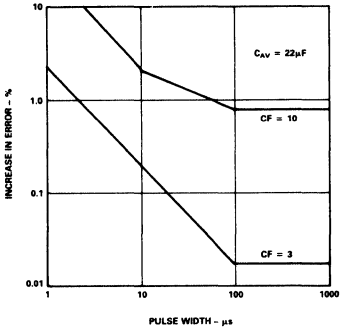


Figure 11. AD637 Error vs. Pulse Width Rectangular Pulse

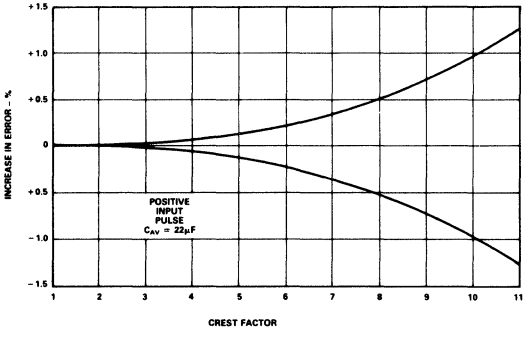


Figure 12. Additional Error vs. Crest Factor

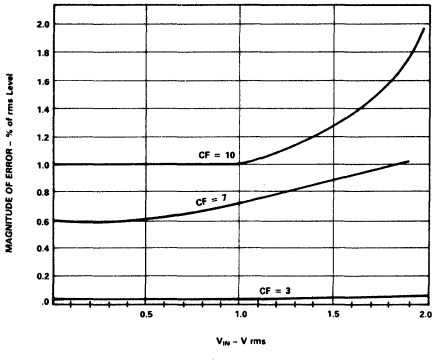


Figure 13. Error vs. RMS Input Level for Three Common Crest Factors

CONNECTION FOR dB OUTPUT

Another feature of the AD637 is the logarithmic or decibel output. The internal circuit which computes dB works well over a 60dB range. The connection for dB measurement is shown in Figure 14. The user selects the 0dB level by setting R1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer/divider circuit at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the +0.33%/°C temperature drift of the dB circuit. The special T.C. resistor R3 is available from Tel Labs in Londenderry, New Hampshire (model Q-81) and from Precision Resistor Inc., Hillside, N.J. (model PT146).

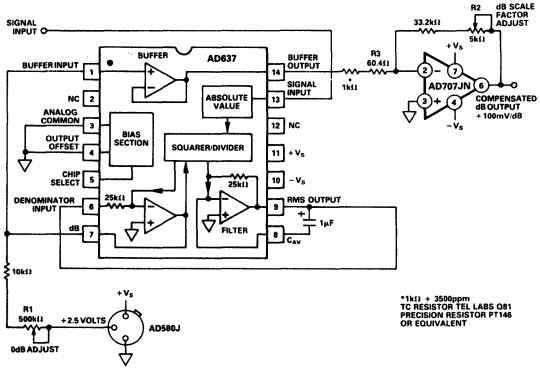


Figure 14. dB Connection

dB CALIBRATION

1. Set V_{IN} = 1.00V dc or 1.00V rms
2. Adjust R1 for 0dB out = 0.00V
3. Set V_{IN} = 0.1V dc or 0.10V rms
4. Adjust R2 for dB out = −2.00V

Any other dB reference can be used by setting V_{IN} and R1 accordingly.

LOW FREQUENCY MEASUREMENTS

If the frequencies of the signals to be measured are below 10Hz, the value of the averaging capacitor required to deliver even 1% averaging error in the standard rms connection becomes extremely large. The circuit shown in Figure 15 shows an alternative method of obtaining low frequency rms measurements. The averaging time constant is determined by the product of R and C_{AV1}, in this circuit 0.5s/μF of C_{AV}. This circuit permits a 20:1 reduction in the value of the averaging capacitor, permitting the use of high quality tantalum capacitors. It is suggested that the two pole Sallen-Key filter shown in the diagram be used to obtain a low ripple level and minimize the value of the averaging capacitor.

If the frequency of interest is below 1Hz, or if the value of the averaging capacitor is still too large, the 20:1 ratio can be increased. This is accomplished by increasing the value of R. If this is done it is suggested that a low input current, low offset voltage amplifier like the AD548 be used instead of the internal buffer amplifier. This is necessary to minimize the offset error introduced by the combination of amplifier input currents and the larger resistance.

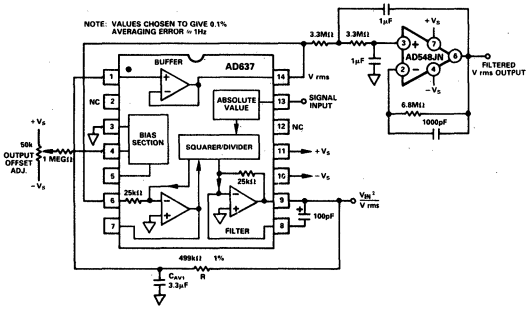


Figure 15. AD637 as a Low Frequency rms Converter

VECTOR SUMMATION

Vector summation can be accomplished through the use of two AD637s as shown in Figure 16. Here the averaging capacitors are omitted (nominal 100pF capacitors are used to insure stability of the filter amplifier), and the outputs are summed as shown. The output of the circuit is

$$V_O = \sqrt{V_X^2 + V_Y^2}$$

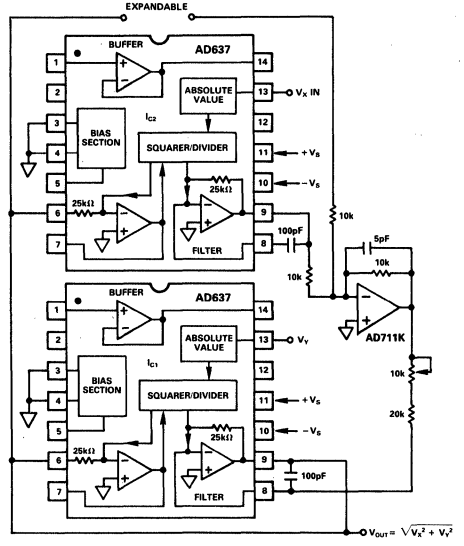


Figure 16. AD637 Vector Sum Configuration

This concept can be expanded to include additional terms by feeding the signal from pin 9 of each additional AD637 through a 10kΩ resistor to the summing junction of the AD711, and tying all of the denominator inputs (pin 6) together.

If C_{AV} is added to IC1 in this configuration the output is $\sqrt{V_X^2 + V_Y^2}$ If the averaging capacitor is included on both IC1 and IC2 the output will be $\sqrt{V_X^2 + V_Y^2}$

This circuit has a dynamic range of 10V to 10mV and is limited only by the 0.5mV offset voltage of the AD637. The useful bandwidth is 100kHz.

Low Cost, Low Power True RMS-to-DC Converter

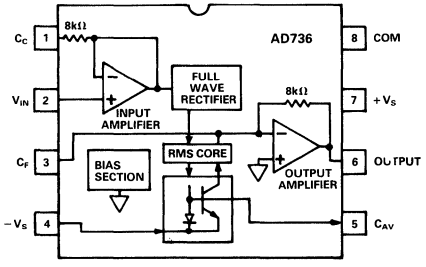
AD736

FEATURES

COMPUTES
- True RMS Value
- Average Rectified Value
- Absolute Value

PROVIDES
- 200mV Full-Scale Input Range (Larger Inputs with Input Attenuator)
- High Input Impedance of $10^{12}\Omega$
- Low Input Bias Current: 25pA max
- High Accuracy: ±0.3mV ±0.3% of Reading
- RMS Conversion with Signal Crest Factors Up to 5
- Wide Power Supply Range: +2.8V, −3.2V to ±16.5V
- Low Power: 200μA max Supply Current
- Buffered Voltage Output
- No External Trims Needed for Specified Accuracy
- AD737 – An Unbuffered Voltage Output Version with Chip Power Down Is Also Available

FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT DESCRIPTION

The AD736 is a low power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of ±0.3mV ±0.3% of reading with sine-wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD736 offers higher accuracy at equal or lower cost.

The AD736 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD736 can resolve input signal levels of 100μV rms or less, despite variations in temperature or supply voltage. High acccuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200mV full-scale input level.

The AD736 has its own output buffer amplifier, thereby providing a great deal of design flexibility. Requiring only 200μA of power supply current, the AD736 is optimized for use in portable multimeters and other battery powered applications.

The AD736 allows the choice of two signal input terminals: a high impedance ($10^{12}\Omega$) FET input which will directly interface with high Z input attenuators and a low impedance (8kΩ) input which allows the measurement of 300mV input levels, while operating from the minimum power supply voltage of +2.8V, −3.2V. The two inputs may be used either singly or differentially.

The AD736 achieves a 1% of reading error bandwidth exceeding 10kHz for input amplitudes from 20mV rms to 200mV rms while consuming only 1mW.

The AD736 is available in four performance grades. The AD736J and AD736K grades are rated over the commercial temperature range of 0 to +70°C. The AD736A and AD736B grades are rated over the industrial temperature range of −40°C to +85°C.

The AD736 is available in three low-cost 8-pin packages: plastic mini-DIP, plastic SO and hermetic cerdip.

PRODUCT HIGHLIGHTS

1. The AD736 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD736 to perform true rms measurement.
3. The low power consumption of 1mW makes the AD736 suitable for many battery powered applications.
4. A high input impedance of $10^{12}\Omega$ eliminates the need for an external buffer when interfacing with input attenuators.
5. A low impedance input is available for those applications requiring up to 300mV rms input signal operating from low power supply voltages.

AD736—SPECIFICATIONS (@ +25°C ±5V supplies, ac coupled with 1kHz sine-wave input applied unless otherwise noted.)

Model	Conditions	AD736J/A Min	AD736J/A Typ	AD736J/A Max	AD736K/B Min	AD736K/B Typ	AD736K/B Max	Units
TRANSFER FUNCTION			V_{OUT} $\sqrt{Avg.(V_{IN}^2)}$			V_{OUT} $\sqrt{Avg.(V_{IN}^2)}$		
CONVERSION ACCURACY	1kHz Sine Wave							
Total Error, Internal Trim[1]	ac Coupled Using C_C:							
All Grades	0-200mV rms		0.3/0.3	**0.5/0.5**		0.2/0.2	**0.3/0.3**	± mV/± % of Reading
	200mV-1V rms		1.2	**±2.0**		1.2	**±2.0**	% of Reading
T_{min}-T_{max}								
A&B Grades	@ 200mV rms			**0.7/0.7**			**0.5/0.5**	± mV/± % of Reading
J&K Grades	@ 200mV rms		0.007			0.007		± % of Reading/°C
vs. Supply Voltage								
@ 200mV rms Input	V_S ±5V to ±16.5V	**0**	+0.06	**+0.1**	**0**	+0.06	**+0.1**	%/V
@ 200mV rms Input	V_S ±5V to ±3V	**0**	0.18	**−0.3**	**0**	−0.18	**−0.3**	%/V
dc Reversal Error, dc Coupled	@ 600mV dc		1.3	2.5		1.3	2.5	% of Reading
Nonlinearity[2], 0-200mV	@ 100mV rms	**0**	+0.25	**+0.35**	**0**	+0.25	**+0.35**	% of Reading
Total Error, External Trim	0-200mV rms		0.1/0.5			0.1/0.3		± mV/± % of Reading
ERROR vs. CREST FACTOR[3]								
Crest Factor 1 to 3	C_{AV}, C_F = 100µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S +2.8V, 3.2V			**200**			**200**	mV rms
Continuous rms Level	V_S ±5V to ±16.5V			**1**			**1**	V rms
Peak Transient Input	V_S +2.8V, 3.2V	**±0.9**			**±0.9**			V
Peak Transient Input	V_S ±5V		±2.7			±2.7		V
Peak Transient Input	V_S ±16.5V	**±4.0**			**±4.0**			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	±5V		1	25		1	25	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8V, −3.2V			300			300	mV rms
Continuous rms Level	V_S = ±5V to ±16.5V			1			1	V rms
Peak Transient Input	V_S = +2.8V, −3.2V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous Non-Destructive Input	All Supply Voltages			±12			±12	V p-p
Input Offset Voltage[4]	ac Coupled							
J&K Grades				**±3**			**±3**	mV
A&B Grades				**±3**			**±3**	mV
vs. Temperature			8	30		8	30	µV/°C
vs. Supply	V_S = ±5V to ±16.5V		50	**150**		50	**150**	µV/V
vs. Supply	V_S = ±5V to ±3V		80			80		µV/V
OUTPUT CHARACTERISTICS								
Output Offset Voltage								
J&K Grades			±0.1	**±0.5**		±0.1	**±0.3**	mV
A&B Grades				**±0.5**			**±0.3**	mV
vs. Temperature			1	20		1	20	µV/°C
vs. Supply	V_S = ±5V to ±16.5V		50	**130**		50	**130**	µV/V
	V_S = ±5V to ±3V		50			50		µV/V
Output Voltage Swing								
2kΩ Load	V_S = +2.8V, −3.2V	0 to +1.6	+1.7		0 to +1.6	+1.7		V
2kΩ Load	V_S = ±5V	0 to +3.6	+3.8		0 to +3.6	+3.8		V
2kΩ Load	V_S = ±16.5V	**0 to +4**	+5		**0 to +4**	+5		V
No Load	V_S = ±16.5V	**0 to +4**	+12		**0 to +4**	+12		V
Output Current		2			2			mA
Short-Circuit Current			3			3		mA
Output Resistance	@ dc		0.2			0.2		Ω
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1mV rms			1			1		kHz
V_{IN} = 10mV rms			6			6		kHz
V_{IN} = 100mV rms			37			37		kHz
V_{IN} = 200mV rms			33			33		kHz
±3dB Bandwidth	Sine-Wave Input							
V_{IN} = 1mV rms			5			5		kHz
V_{IN} = 10mV rms			55			55		kHz
V_{IN} = 100mV rms			170			170		kHz
V_{IN} = 200mV rms			190			190		kHz

Model	Conditions	AD736J/A Min	AD736J/A Typ	AD736J/A Max	AD736K/B Min	AD736K/B Typ	AD736K/B Max	Units
FREQUENCY RESPONSE								
Low Impedance Input (Pin 1)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1mV rms			1			1		kHz
V_{IN} = 10mV rms			6			6		kHz
V_{IN} = 100mV rms			90			90		kHz
V_{IN} = 200mV rms			90			90		kHz
±3dB Bandwidth	Sine-Wave Input							
V_{IN} = 1mV rms			5			5		kHz
V_{IN} = 10mV rms			55			55		kHz
V_{IN} = 100mV rms			350			350		kHz
V_{IN} = 200mV rms			460			460		kHz
POWER SUPPLY								
Operating Voltage Range		+2.8, −3.2	±5	±16.5	+2.8, −3.2	±5	±16.5	Volts
Quiescent Current	Zero Signal		160	**200**		160	**200**	μA
200mV rms, No Load	Sine-Wave Input		230	270		230	270	μA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD736J			AD736K		
Industrial (−40°C to +85°C)			AD736A			AD736B		

NOTES
[1]Accuracy is specified with the AD736 connected as shown in Figure 16 with capacitor C_C.
[2]Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 and 200mV rms. Output offset voltage is adjusted to zero.
[3]Error vs. Crest Factor is specified as additional error for a 200mV rms signal. C.F. = V_{PEAK}/V rms.
[4]DC offset does not limit ac resolution.

Specifications are subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final electrical test.
Results from those tests are used to calculate outgoing quality levels.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD736JN	0°C to +70°C	Plastic Mini-DIP	N-8
AD736KN	0°C to +70°C	Plastic Mini-DIP	N-8
AD736JR	0°C to +70°C	Plastic SOIC	R-8
AD736KR	0°C to +70°C	Plastic SOIC	R-8
AD736AQ	−40°C to +85°C	Cerdip	Q-8
AD736BQ	−40°C to +85°C	Cerdip	Q-8

*For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±16.5V
Internal Power Dissipation[2] 200mW
Input Voltage . . . . . ±V_S
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . +V_S and −V_S
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD736J/K . . . . . 0 to +70°C
AD736A/B . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/W
8-Pin Cerdip Package: θ_{JA} = 110°C/W
8-Pin Small Outline Package: θ_{JA} = 155°C/W

AD736—Typical Characteristics

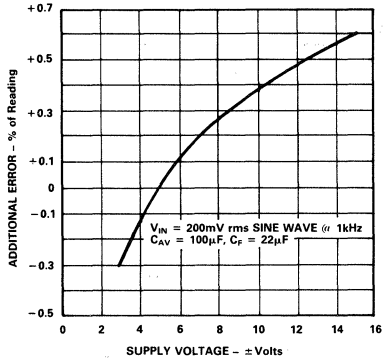


Figure 1. Additional Error vs. Supply Voltage

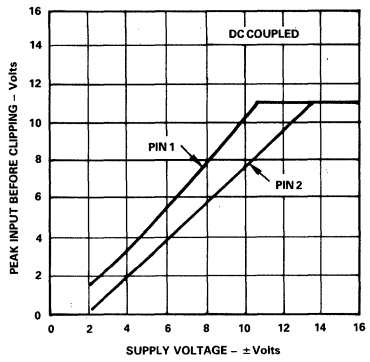


Figure 2. Maximum Input Level vs. Supply Voltage

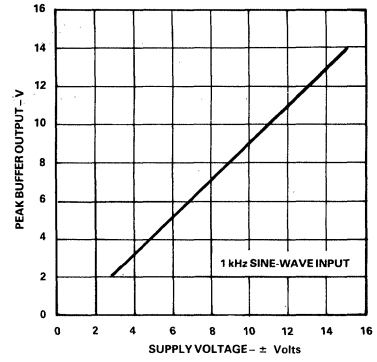


Figure 3. Peak Buffer Output vs. Supply Voltage

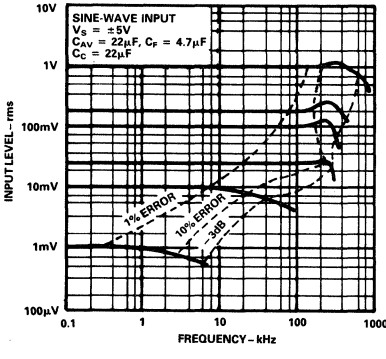


Figure 4. Frequency Response Driving Pin 1

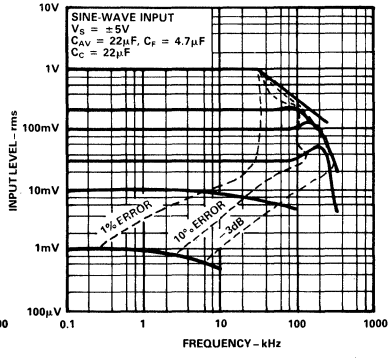


Figure 5. Frequency Response Driving Pin 2

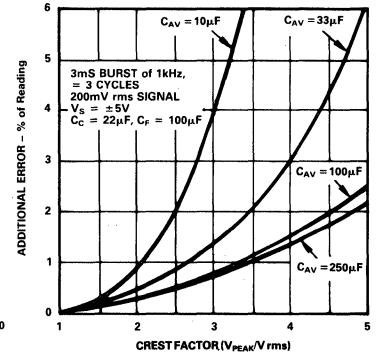


Figure 6. Additional Error vs. Crest Factor vs. C_{AV}

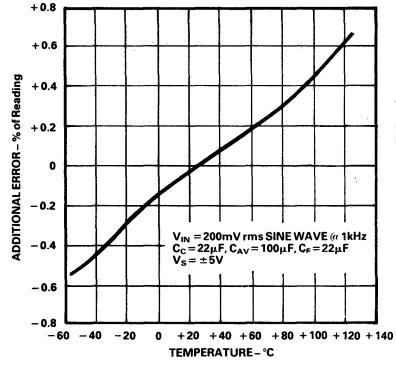


Figure 7. Additional Error vs. Temperature

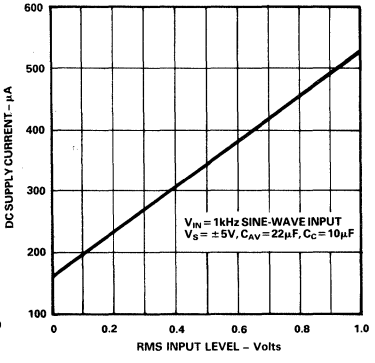


Figure 8. DC Supply current vs. RMS Input Level

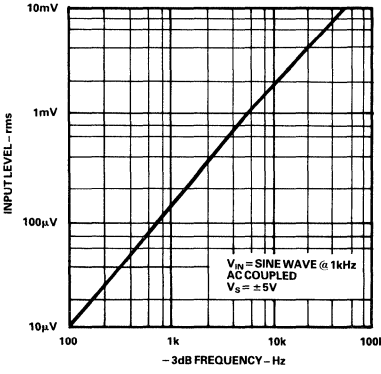


Figure 9. –3dB Frequency vs. RMS Input Level (Pin 2)

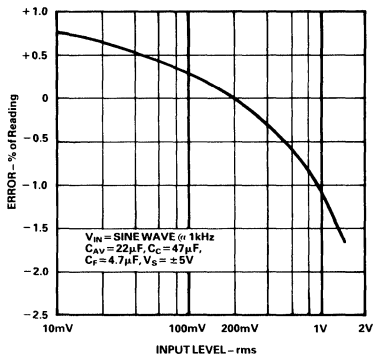


Figure 10. Error vs. RMS Input Voltage (Pin 2), Output Buffer Offset Is Adjusted To Zero

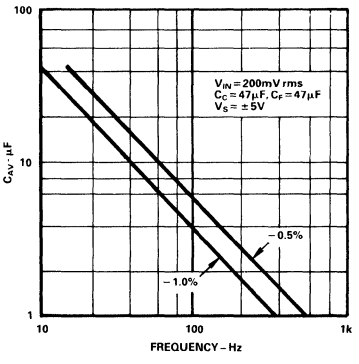


Figure 11. C_{AV} vs. Frequency for Specified Averaging Error

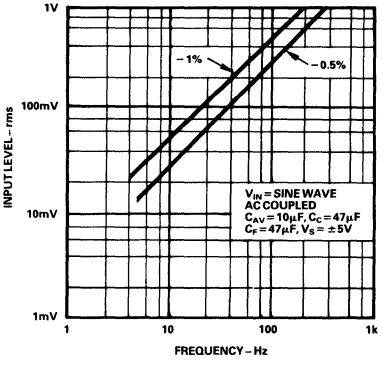


Figure 12. RMS Input Level vs. Frequency for Specified Averaging Error

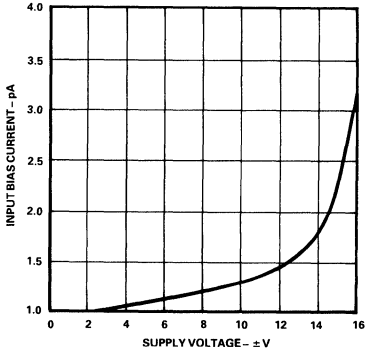


Figure 13. Pin 2 Input Bias Current vs. Supply Voltage

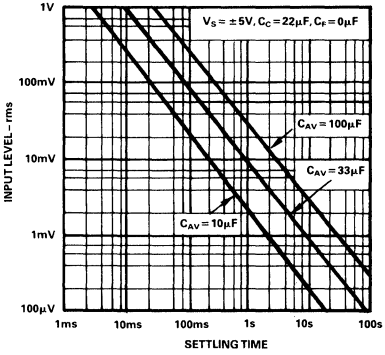


Figure 14. Settling Time vs. RMS Input Level for Various Values of C_{AV}

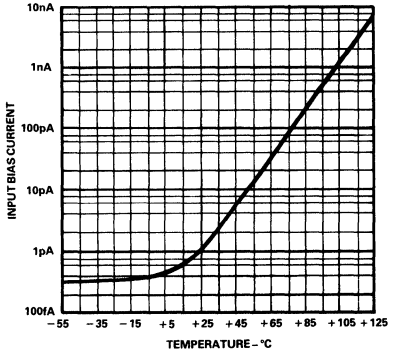


Figure 15. Pin 2 Input Bias Current vs. Temperature

CALCULATING SETTLING TIME USING FIGURE 14

The graph of Figure 14 may be used to closely approximate the time required for the AD736 to settle when its input level is reduced in amplitude. The *net time* required for the rms converter to settle will be the *difference* between two times extracted from the graph – the initial time minus the final settling time. As an example, consider the following conditions: a 33µF averaging capacitor, an initial rms input level of 100mV and a final (reduced) input level of 1mV. From Figure 14, the initial settling time (where the 100mV line intersects the 33µF line) is around 80ms.

The settling time corresponding to the new or final input level of 1mV is approximately 8 seconds. Therefore, the net time for the circuit to settle to its new value will be 8 seconds minus 80ms which is 7.92 seconds. Note that, because of the smooth decay characteristic inherent with a capacitor/diode combination, this is the total settling time to the final value (i.e., *not* the settling time to 1%, 0.1%, etc., of final value). Also, this graph provides the worst case settling time, since the AD736 will settle very quickly with increasing input levels.

TYPES OF AC MEASUREMENT

The AD736 is capable of measuring ac signals by operating as either an average responding or a true rms-to-dc converter. As its name implies, an average responding converter computes the average absolute value of an ac (or ac and dc) voltage or current by full wave rectifing and low-pass filtering the input signal; this will approximate the average. The resulting output, a dc "average" level, is then scaled by adding (or reducing) gain; this scale factor converts the dc average reading to an rms equivalent value for the waveform being measured. For example, the average absolute value of a sine-wave voltage is 0.636 that of V_{PEAK}; the corresponding rms value is 0.707 times V_{PEAK}. Therefore, for sine-wave voltages, the required scale factor is 1.11 (0.707 divided by 0.636).

In contrast to measuring the "average" value, true rms measurement is a "universal language" among waveforms, allowing the magnitudes of all types of voltage (or current) waveforms to be compared to one another and to dc. RMS is a direct measure of the power or heating value of an ac voltage compared to that of dc: an ac signal of 1 volt rms will produce the same amount of heat in a resistor as a 1 volt dc signal.

Mathematically, the rms value of a voltage is defined (using a simplified equation) as:

$$V \text{ rms} = \sqrt{\text{Avg. } (V^2)}$$

This involves squaring the signal, taking the average, and then obtaining the square root. True rms converters are "smart rectifiers": they provide an accurate rms reading regardless of the type of waveform being measured. However, average responding converters can exhibit very high errors when their input signals deviate from their precalibrated waveform; the magnitude of the error will depend upon the type of waveform being measured. As an example, if an average responding converter is calibrated to measure the rms value of sine-wave voltages, and then is used to measure either symmetrical square waves or dc voltages, the converter will have a computational error 11% (of reading) higher than the true rms value (see Table I).

AD736 THEORY OF OPERATION

As shown by Figure 16, the AD736 has five functional subsections: input amplifier, full-wave rectifier, rms core, output amplifier and bias sections. The FET input amplifier allows both a high impedance, buffered input (Pin 2) or a low impedance, wide-dynamic-range input (Pin 1). The high impedance input, with its low input bias current, is well suited for use with high impedance input attenuators.

The output of the input amplifier drives a full wave precision rectifier, which in turn, drives the rms core. It is in the core that the essential rms operations of squaring, averaging and square rooting are performed, using an external averaging capacitor, C_{AV}. Without C_{AV}, the rectified input signal travels through the core unprocessed, as is done with the average responding connection (Figure 17).

A final subsection, an output amplifier, buffers the output from the core and also allows optional low-pass filtering to be performed via external capacitor, C_F, connected across the feedback path of the amplifier. In the average responding connection, this is where all of the averaging is carried out. In the rms circuit, this additional filtering stage helps reduce any output ripple which was not removed by the averaging capacitor, C_{AV}.

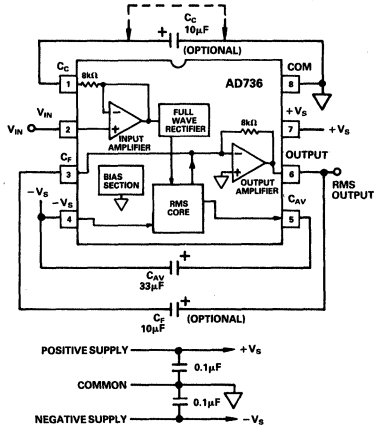


Figure 16. AD736 True RMS Circuit

Waveform Type 1 Volt Peak Amplitude	Crest Factor (V_{PEAK}/V rms)	True rms Value	Average Responding Circuit Calibrated to Read rms Value of Sine Waves Will Read	% of Reading Error* Using Average Responding Circuit
Undistorted Sine Wave	1.414	0.707V	0.707V	0%
Symmetrical Square Wave	1.00	1.00V	1.11V	+11.0%
Undistorted Triangle Wave	1.73	0.577V	0.555V	−3.8%
Gaussian Noise (98% of Peaks <1 V)	3	0.333V	0.295V	−11.4%
Rectangular Pulse Train	2 10	0.5V 0.1V	0.278V 0.011V	−44% −89%
SCR Waveforms 50% Duty Cycle 25% Duty Cycle	2 4.7	0.495V 0.212V	0.354V 0.150V	−28% −30%

$$*\%\text{ of Reading Error} = \frac{\text{Average Responding Value} - \text{True rms Value}}{\text{True rms Value}} \times 100\%$$

Table I. Error Introduced by an Average Responding Circuit When Measuring Common Waveforms

RMS MEASUREMENT – CHOOSING THE OPTIMUM VALUE FOR C_{AV}

Since the external averaging capacitor, C_{AV}, "holds" the rectified input signal during rms computation, its value directly affects the accuracy of the rms measurement, especially at low frequencies. Furthermore, because the averaging capacitor appears across a diode in the rms core, the averaging time constant will increase exponentially as the input signal is reduced. This means that as the input level decreases, errors due to nonideal averaging will *reduce* while the time it takes for the circuit to settle to the new rms level will *increase*. Therefore, lower input levels allow the circuit to perform better (due to increased averaging) but increase the waiting time between measurements. Obviously, when selecting C_{AV}, a trade-off between computational accuracy and settling time is required.

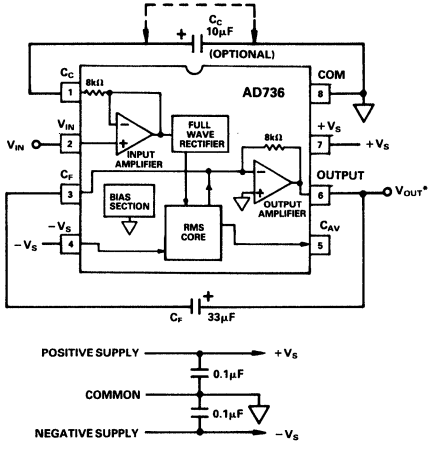


Figure 17. AD736 Average Responding Circuit

RAPID SETTLING TIMES VIA THE AVERAGE RESPONDING CONNECTION (FIGURE 17)

Because the average responding connection does not use the C_{AV} averaging capacitor, its settling time does not vary with input signal level; it is determined solely by the RC time constant of C_F and the internal 8kΩ resistor in the output amplifier's feedback path.

DC ERROR, OUTPUT RIPPLE, AND AVERAGING ERROR

Figure 18 shows the typical output waveform of the AD736 with a sine-wave input applied. As with all real-world devices, the ideal output of $V_{OUT} = V_{IN}$ is never exactly achieved; instead, the output contains both a dc and an ac error component.

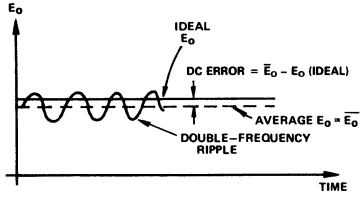


Figure 18. Output Waveform for Sine-Wave Input Voltage

As shown, the dc error is the difference between the average of the output signal (when all the ripple in the output has been removed by external filtering) and the ideal dc output. The dc error component is therefore set solely by the value of averaging capacitor used – *no* amount of post filtering (i.e., using a very large C_F) will allow the output voltage to equal its ideal value. The ac error component, an output ripple, may be easily removed by using a large enough post filtering capacitor, C_F.

In most cases, the combined magnitudes of both the dc and ac error components need to be considered when selecting appropriate values for capacitors C_{AV} and C_F. This combined error, representing the maximum uncertainty of the measurement is termed the "averaging error" and is equal to the peak value of the output ripple plus the dc error.

As the input frequency increases, both error components decrease rapidly: if the input frequency doubles, the dc error and ripple reduce to 1/4 and 1/2 their original values, respectively, and rapidly become insignificant.

AC MEASUREMENT ACCURACY AND CREST FACTOR

The crest factor of the input waveform is often overlooked when determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms amplitude (C.F. = V_{PEAK}/V rms). Many common waveforms, such as sine and triangle waves, have relatively low crest factors (≤2). Other waveforms, such as low duty cycle pulse trains and SCR waveforms, have high crest factors. These types of waveforms require a long averaging time constant (to average out the long time periods between pulses). Figure 6 shows the additional error vs. crest factor of the AD736 for various values of C_{AV}.

SELECTING PRACTICAL VALUES FOR INPUT COUPLING (C_C), AVERAGING (C_{AV}) AND FILTERING (C_F) CAPACITORS

Table II provides practical values of C_{AV} and C_F for several common applications.

Application	rms Input Level	Low Frequency Cutoff (–3dB)	Max Crest Factor	C_{AV}	C_F	Settling Time* to 1%
General Purpose rms Computation	0-1V	20Hz	5	150µF	10µF	360ms
		200Hz	5	15µF	1µF	36ms
	0-200mV	20Hz	5	33µF	10µF	360ms
		200Hz	5	3.3µF	1µF	36ms
General Purpose Average Responding	0-1V	20Hz		None	33µF	1.2sec
		200Hz		None	3.3µF	120ms
	0-200mV	20Hz		None	33µF	1.2sec
		200Hz		None	3.3µF	120ms
SCR Waveform Measurement	0-200mV	50Hz	5	100µF	33µF	1.2sec
		60Hz	5	82µF	27µF	1.0sec
	0-100mV	50Hz	5	50µF	33µF	1.2sec
		60Hz	5	47µF	27µF	1.0sec
Audio Applications						
Speech	0-200mV	300Hz	3	1.5µF	0.5µF	18ms
Music	0-100mV	20Hz	10	100µF	68µF	2.4sec

* Settling time is specified over the stated rms input level with the input signal increasing from zero. Settling times will be greater for decreasing amplitude input signals.

Table II. AD737 Capacitor Selection Chart

The input coupling capacitor, C_C, in conjunction with the 8kΩ internal input scaling resistor, determine the −3dB low frequency rolloff. This frequency, F_L is equal to:

$$F_L = \frac{1}{2\pi\ (8{,}000)\ (\text{The Value of } C_C \text{ in Farads})}$$

Note that at F_L, the amplitude error will be approximately −30% (−3dB) of reading. To reduce this error to 0.5% of reading, choose a value of C_C that sets F_L at one tenth the lowest frequency to be measured.

In addition, if the input voltage has more than 100mV of dc offset, than the ac coupling network shown in Figure 21 should be used in addition to capacitor C_C.

Applications Circuits

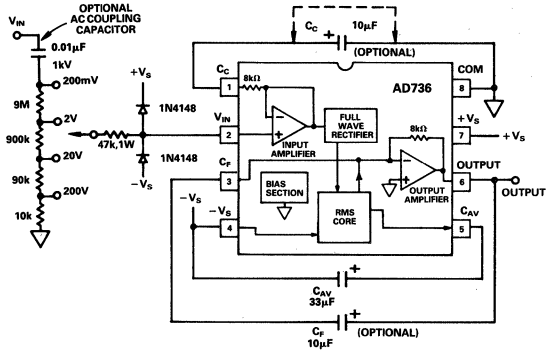


Figure 19. AD736 with a High Impedance Input Attenuator

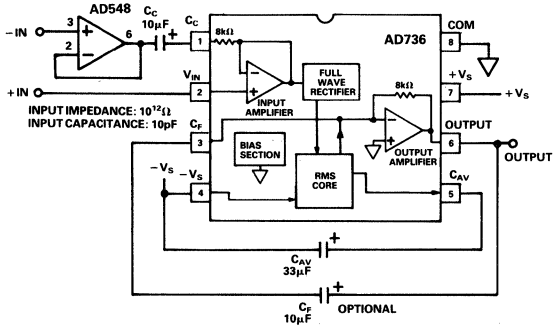


Figure 20. Differential Input Connection

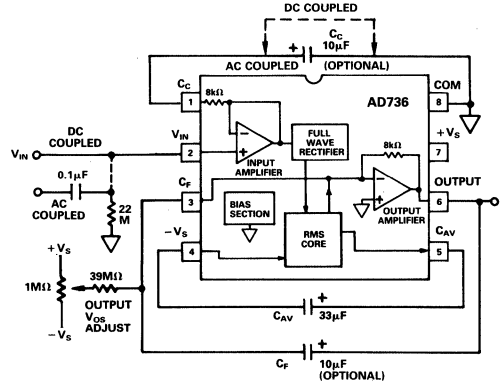


Figure 21. External Output V_{OS} Adjustment

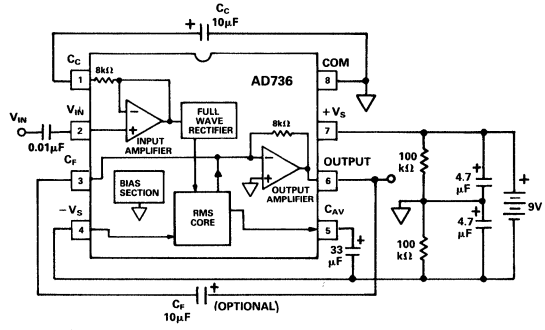


Figure 22. Battery Powered Option

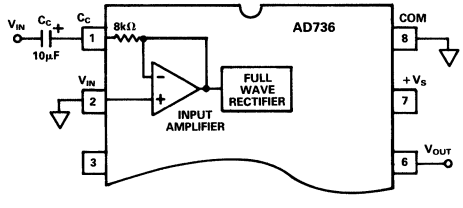


Figure 23. Low Z, AC Coupled Input Connection

Low Cost, Low Power, True RMS-to-DC Converter

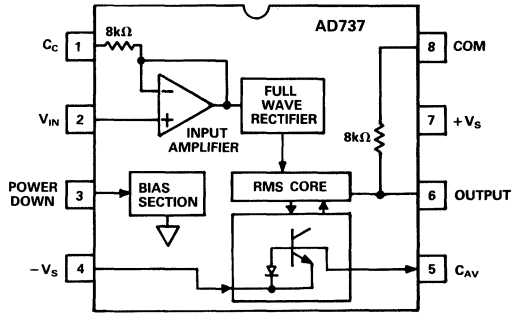
AD737

FEATURES

COMPUTES
- True RMS Value
- Average Rectified Value
- Absolute Value

PROVIDES
- 200mV Full-Scale Input Range (Larger Inputs with Input Attenuator)
- Direct Interfacing with 3 1/2 Digit CMOS A/D Converters
- Power Down Feature Which Reduces Supply Current
- High Input Impedance: 10^{12} Ω
- Low Input Bias Current: 25 pA max
- High Accuracy: ±0.2 mV ±0.3% of Reading
- RMS Conversion with Signal Crest Factors Up to 5
- Wide Power Supply Range: +2.8 V, −3.2 V to ±16.5 V
- Low Power: 160 μA max Supply Current
- No External Trims Needed for Specified Accuracy
- AD736 – A General Purpose, Buffered Voltage Output Version Also Available

FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT DESCRIPTION

The AD737 is a low power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of ±0.2 mV ±0.3% of reading with sine wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD737 offers higher accuracy at equal or lower cost.

The AD737 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD737 can resolve input signal levels of 100 μV rms or less, despite variations in temperature or supply voltage. High accuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200 mV full-scale input level.

The AD737 has no output buffer amplifier, thereby significantly reducing dc offset errors occurring at the output. This allows the device to be highly compatible with high input impedance A/D converters.

Requiring only 160 μA of power supply current, the AD737 is optimized for use in portable multimeters and other battery powered applications. This converter also provides a "power down" feature which reduces the power supply standby current to less than 30 μA.

The AD737 allows the choice of two signal input terminals: a high impedance (10^{12} Ω) FET input which will directly interface with high Z input attenuators and a low impedance (8 kΩ) input which allows the measurement of 300 mV input levels while operating from the minimum power supply voltage of +2.8 V, −3.2 V. The two inputs may be used either singly or differentially.

The AD737 achieves a 1% of reading error bandwidth exceeding 10 kHz for input amplitudes from 20 mV rms to 200 mV rms while consuming only 0.72 mW.

The AD737 is available in four performance grades. The AD737J and AD737K grades are rated over the commercial temperature range of 0 to +70°C. The AD737A and AD737B grades are rated over the industrial temperature range of −40°C to +85°C.

The AD737 is available in three low cost, 8-pin packages: plastic mini-DIP, plastic SO and hermetic cerdip.

PRODUCT HIGHLIGHTS

1. The AD737 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD737 to perform true rms measurement.
3. The low power consumption of 0.72 mW makes the AD737 suitable for many battery powered applications.

AD737—SPECIFICATIONS (@ +25°C, ±5 V supplies, ac coupled with 1 kHz sine wave input applied unless otherwise noted.)

Model	Conditions	AD737J/A Min	AD737J/A Typ	AD737J/A Max	AD737K/B Min	AD737K/B Typ	AD737K/B Max	Units
TRANSFER FUNCTION		$V_{OUT} = -\sqrt{Avg.(V_{IN}^2)}$			$V_{OUT} = -\sqrt{Avg.(V_{IN}^2)}$			
CONVERSION ACCURACY	1 kHz Sine Wave							
Total Error, Internal Trim[1]	AC Coupled Using C_C							
All Grades	0–200 mV rms		0.2/0.3	**0.4/0.5**		0.2/0.2	**0.2/0.3**	±mV/±% of Reading
	200 mV–1 V rms		−1.2	**±2.0**		−1.2	**±2.0**	% of Reading
T_{min}–T_{max}								
A&B Grades	@ 200 mV rms			**0.5/0.7**			**0.3/0.5**	±mV/±% of Reading
J&K Grades	@ 200 mV rms		0.007			0.007		±% of Reading/°C
vs. Supply Voltage								
@ 200 mV rms Input	V_S = ±5 V to ±16.5 V	**0**	+0.06	**+0.1**	**0**	+0.06	**+0.1**	%/V
@ 200 mV rms Input	V_S = ±5 V to ±3 V	**0**	−0.18	**−0.3**	**0**	−0.18	**−0.3**	%/V
dc Reversal Error, dc Coupled	@ 600 mV dc		1.3	**2.5**		1.3	**2.5**	% of Reading
Nonlinearity[2], 0–200 mV	@ 100 mV rms	**0**	+0.25	**+0.35**	**0**	+0.25	**+0.35**	% of Reading
Total Error, External Trim	0–200 mV rms		0.1/0.2			0.1/0.2		±mV/±% of Reading
ERROR VS. CREST FACTOR[3]								
Crest Factor 1 to 3	C_{AV}, C_F = 100 µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100 µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, −3.2 V			**200**			**200**	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			**1**			**1**	V rms
Peak Transient Input	V_S = +2.8 V, −3.2 V	**±0.9**			**±0.9**			V
Peak Transient Input	V_S = ±5 V		±2.7			±2.7		V
Peak Transient Input	V_S = ±16.5 V	**±4.0**			**±4.0**			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	V_S = ±5 V		1	**25**		1	**25**	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8 V, −3.2 V			300			300	mV rms
Continuous rms Level	V_S = ±5 V to ±16.5 V			1			1	V rms
Peak Transient Input	V_S = +2.8 V, −3.2 V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5 V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5 V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous Nondestructive Input	All Supply Voltages			±12			±12	V p–p
Input Offset Voltage[4]	ac Coupled							
J&K Grades				**±3**			**±3**	mV
A&B Grades				**±3**			**±3**	mV
vs. Temperature			8	30		8	30	µV/°C
vs. Supply	V_S = ±5 V to ±16.5 V		50	**150**		50	**150**	µV/V
vs. Supply	V_S = ±5 V to ±3 V		80			80		µV/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
No Load	V_S = +2.8 V, −3.2 V	0 to −1.6	−1.7		0 to −1.6	−1.7		V
No Load	V_S = ±5 V	0 to −3.3	−3.4		0 to −3.3	−3.4		V
No Load	V_S = ±16.5 V	**0 to −4**	−5		**0 to −4**	−5		V
Output Resistance	@ dc	6.4	8	9.6	6.4	8	9.6	kΩ
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			37			37		kHz
V_{IN} = 200 mV rms			33			33		kHz
±3 dB Bandwidth	Sine Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			170			170		kHz
V_{IN} = 200 mV rms			190			190		kHz
FREQUENCY RESPONSE								
Low Impedance Input (Pin 1)								
For 1% Additional Error	Sine Wave Input							
V_{IN} = 1 mV rms			1			1		kHz
V_{IN} = 10 mV rms			6			6		kHz
V_{IN} = 100 mV rms			90			90		kHz
V_{IN} = 200 mV rms			90			90		kHz
±3 dB Bandwidth	Sine Wave Input							
V_{IN} = 1 mV rms			5			5		kHz
V_{IN} = 10 mV rms			55			55		kHz
V_{IN} = 100 mV rms			350			350		kHz
V_{IN} = 200 mV rms			460			460		kHz

Model	Conditions	AD737J/A Min	AD737J/A Typ	AD737J/A Max	AD737K/B Min	AD737K/B Typ	AD737K/B Max	Units
POWER SUPPLY								
Operating Voltage Range		+2.8,−3.2	±5	±16.5	+2.8,−3.2	±5	±16.5	V
Quiescent Current	Zero Signal		120	**160**		120	**160**	μA
V_{IN} = 200 mV rms, No Load	Sine Wave Input		170	210		170	210	μA
Power Down Mode Current	Pin 3 tied to $+V_S$		25	**40**		25	**40**	μA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD737J			AD737K		
Industrial (−40°C to +85°C)			AD737A			AD737B		

NOTES
[1]Accuracy is specified with the AD737 connected as shown in Figure 16 with capacitor C_C.
[2]Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 and 200 mV rms.
[3]Error vs. Crest Factor is specified as additional error for a 200 mV rms signal. C.F. = V_{PEAK}/V rms.
[4]DC offset does not limit ac resolution.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Specifications subject to change without notice.

4

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±16.5 V
Internal Power Dissipation[2] . . . . . 200 mW
Input Voltage . . . . . $\pm V_S$
Output Short-Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . $+V_S$ and $-V_S$
Storage Temperature Range (Q) . . . . . −65°C to +150°C
Storage Temperature Range (N, R) . . . . . −65°C to +125°C
Operating Temperature Range
AD737J/K . . . . . 0 to +70°C
AD737A/B . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]8-Pin Plastic Package: θ_{JA} = 165°C/W
8-Pin Ceramic Package: θ_{JA} = 110°C/W
8-Pin SOIC: θ_{JA} = 155°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD737JN	0°C to +70°C	Plastic Mini-DIP	N-8
AD737KN	0°C to +70°C	Plastic Mini-DIP	N-8
AD737JR	0°C to +70°C	SOIC	R-8
AD737KR	0°C to +70°C	SOIC	R-8
AD737AQ	−40°C to +85°C	Cerdip	Q-8
AD737BQ	−40°C to +85°C	Cerdip	Q-8

*For outline information see Package Information section.

AD737—Typical Characteristics

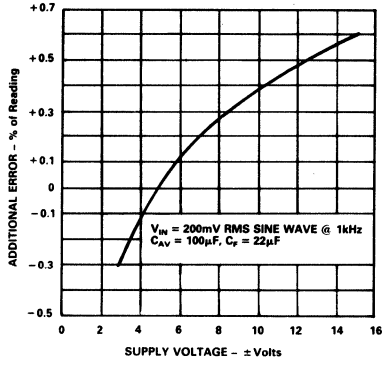


Figure 1. Additional Error vs. Supply Voltage

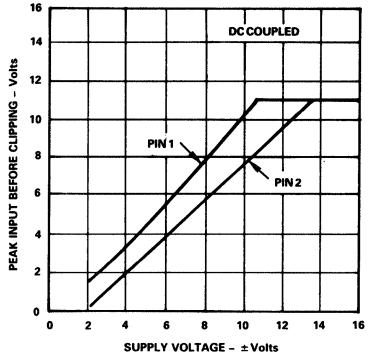


Figure 2. Maximum Input Level vs. Supply Voltage

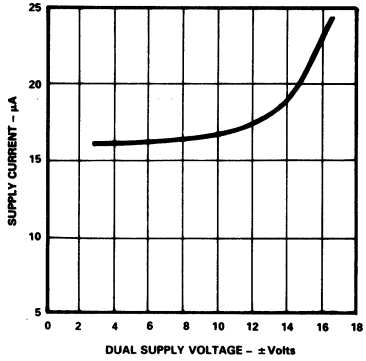


Figure 3. Power Down Current vs. Supply Voltage

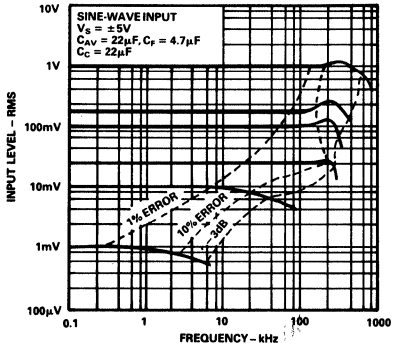


Figure 4. Frequency Response Driving Pin 1

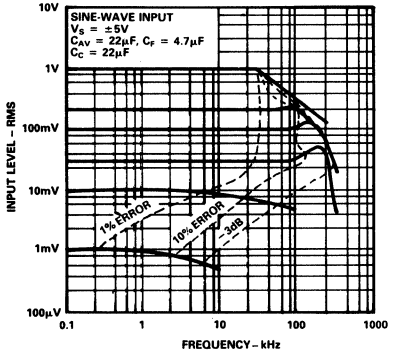


Figure 5. Frequency Response Driving Pin 2

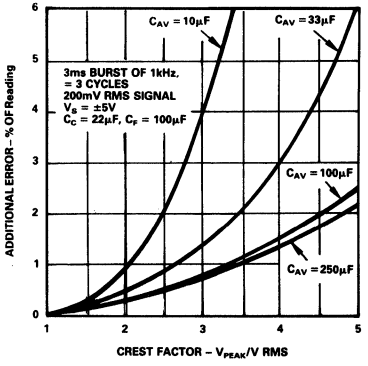


Figure 6. Additional Error vs. Crest Factor vs. C_{AV}

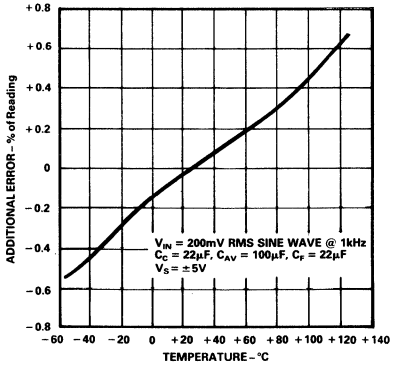


Figure 7. Additional Error vs. Temperature

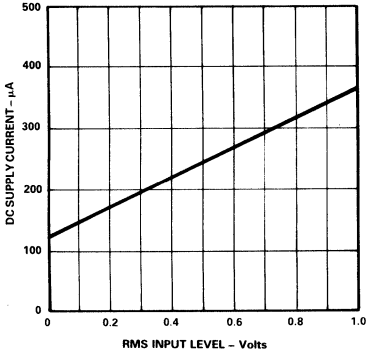


Figure 8. DC Supply Current vs. RMS Input Level

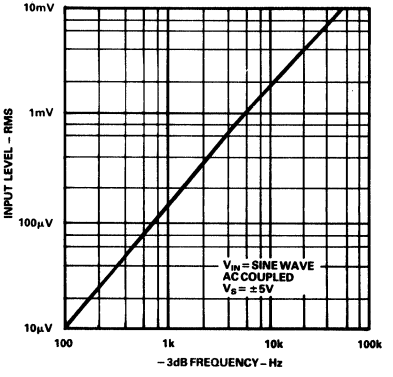


Figure 9. 23dB Frequency vs. RMS Input Level (Pin 2)

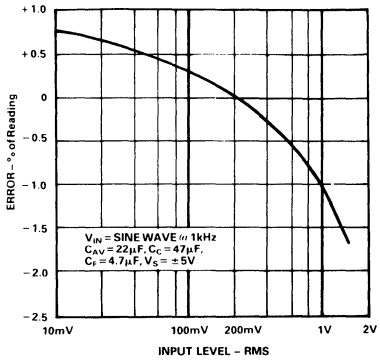


Figure 10. Error vs. RMS Input Voltage (Pin 2) Using Circuit of Figure 21

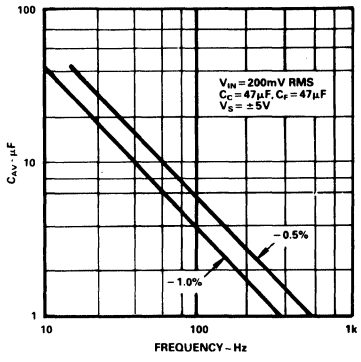


Figure 11. C_{AV} vs. Frequency for Specified Averaging Error

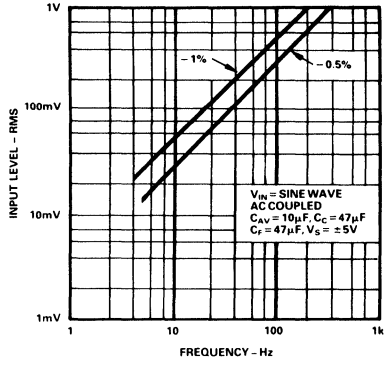


Figure 12. RMS Input Level vs. Frequency for Specified Averaging Error

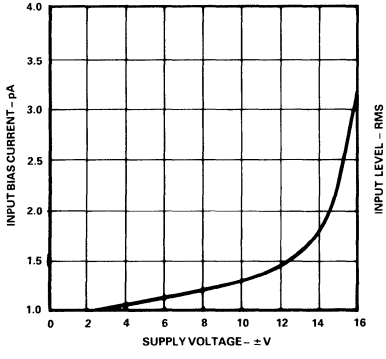


Figure 13. Pin 2 Input Bias Current vs. Supply Voltage

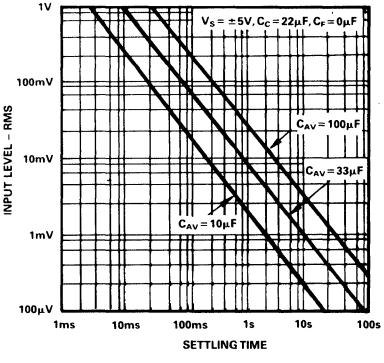


Figure 14. Settling Time vs. RMS Input Level for Various Values of C_{AV}

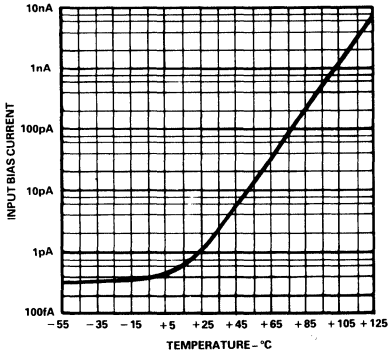


Figure 15. Pin 2 Input Bias Current vs. Temperature

CALCULATING SETTLING TIME USING FIGURE 14

The graph of Figure 14 may be used to closely approximate the time required for the AD737 to settle when its input level is reduced in amplitude. The *net time* required for the rms converter to settle will be the *difference* between two times extracted from the graph — the initial time minus the final settling time. As an example, consider the following conditions: a 33 µF averaging capacitor, an initial rms input level of 100 mV and a final (reduced) input level of 1 mV. From Figure 14, the initial settling time (where the 100 mV line intersects the 33 µF line) is around 80 ms. The settling time corresponding to the new or final input level of 1 mV is approximately 8 seconds. Therefore, the net time for the circuit to settle to its new value will be 8 seconds minus 80 ms which is 7.92 seconds. Note that, because of the smooth decay characteristic inherent with a capacitor/diode combination, this is the total settling time to the final value (i.e., *not* the settling time to 1%, 0.1%, etc., of final value). Also, this graph provides the worst case settling time, since the AD737 will settle very quickly with increasing input levels.

TYPES OF AC MEASUREMENT

The AD737 is capable of measuring ac signals by operating as either an average responding or true rms to dc converter. As its name implies, an average responding converter computes the average absolute value of an ac (or ac & dc) voltage or current by full wave rectifying and low pass filtering the input signal; this will approximate the average. The resulting output, a dc "average" level, is then scaled by adding (or reducing) gain; this scale factor converts the dc average reading to an rms equivalent value for the waveform being measured. For example, the average absolute value of a sine wave voltage is 0.636 that of V_{PEAK}; the corresponding rms value is 0.707 times V_{PEAK}. Therefore, for sine wave voltages, the required scale factor is 1.11 (0.707 divided by 0.636).

In contrast to measuring the "average" value, true rms measurement is a "universal language" among waveforms, allowing the magnitudes of all types of voltage (or current) waveforms to be compared to one another and to dc. RMS is a direct measure of the power or heating value of an ac voltage compared to that of dc: an ac signal of 1 volt rms will produce the same amount of heat in a resistor as a 1 volt dc signal.

Mathematically, the rms value of a voltage is defined (using a simplified equation) as:

$$V\,rms = \sqrt{Avg.\,(V^2)}$$

This involves squaring the signal, taking the average, and then obtaining the square root. True rms converters are "smart rectifiers": they provide an accurate rms reading regardless of the type of waveform being measured. However, average responding converters can exhibit very high errors when their input signals deviate from their precalibrated waveform; the magnitude of the error will depend upon the type of waveform being measured. As an example, if an average responding converter is calibrated to measure the rms value of sine wave voltages, and then is used to measure either symmetrical square waves or dc voltages, the converter will have a computational error 11% (of reading) higher than the true rms value (see Table I).

AD737 THEORY OF OPERATION

As shown by Figure 16, the AD737 has four functional subsections: input amplifier, full wave rectifier, rms core and bias section. The FET input amplifier allows both a high impedance, buffered input (Pin 2) or a low impedance, wide-dynamic-range input (Pin 1). The high impedance input, with its low input bias current, is well suited for use with high impedance input attenuators. The input signal may be either dc or ac coupled to the input amplifier. Unlike other rms converters, the AD737 permits both direct and indirect ac coupling of the inputs. AC coupling is provided by placing a series capacitor between the input signal and Pin 2 (or Pin 1) for direct coupling and between Pin 1 and ground (while driving Pin 2) for indirect coupling.

The output of the input amplifier drives a full-wave precision rectifier, which in turn, drives the rms core. It is in the core that the essential rms operations of squaring, averaging and square rooting are performed, using an external averaging capacitor, C_{AV}. Without C_{AV}, the rectified input signal travels through the core unprocessed, as is done with the average responding connection (Figure 17).

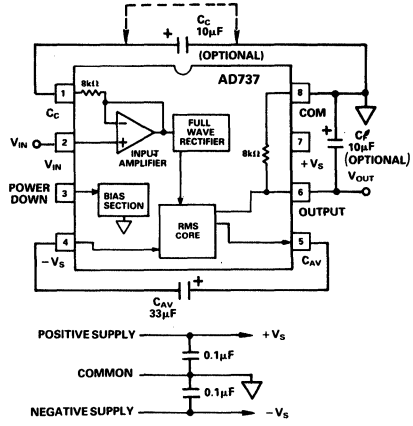


Figure 16. AD737 True RMS Circuit

Waveform Type 1 Volt Peak Amplitude	Crest Factor (V_{PEAK}/V RMS)	True RMS Value	Average Responding Circuit Calibrated to Read RMS Value of Sine Waves Will Read	% of Reading Error* Average Responding Circuit
Undistorted Sine Wave	1.414	0.707 V	0.707 V	0%
Symmetrical Square Wave	1.00	1.00 V	1.11 V	+11.0%
Undistorted Triangle Wave	1.73	0.577 V	0.555 V	−3.8%
Gaussian Noise (98% of Peaks <1 V)	3	0.333 V	0.295 V	−11.4%
Rectangular Pulse Train	2 10	0.5 V 0.1 V	0.278 V 0.011 V	−44% −89%
SCR Waveforms 50% Duty Cycle 25% Duty Cycle	2 4.7	0.495 V 0.212 V	0.354 V 0.150 V	−28% −30%

$$*\%\ \text{of Reading Error} = \frac{\text{Average Responding Value} - \text{True RMS Value}}{\text{True RMS Value}} \times 100\%$$

Table I. Error Introduced by an Average Responding Circuit when Measuring Common Waveforms

A final subsection, the bias section, permits a "power down" function. This reduces the idle current of the AD737 from 160 μA down to a mere 30 μA. This feature is selected by tying Pin 3 to the $+V_S$ terminal. In the average responding connection, all of the averaging is carried out by an RC post filter consisting of an 8 kΩ internal scale-factor resistor connected between Pins 6 and 8 and an external averaging capacitor, C_F. In the rms circuit, this additional filtering stage helps reduce any output ripple which was not removed by the averaging capacitor, C_{AV}.

RMS MEASUREMENT – CHOOSING THE OPTIMUM VALUE FOR C_{AV}

Since the external averaging capacitor, C_{AV}, "holds" the rectified input signal during rms computation, its value directly affects the accuracy of the rms measurement, especially at low frequencies. Furthermore, because the averaging capacitor appears across a diode in the rms core, the averaging time constant will increase exponentially as the input signal is reduced. This means that as the input level decreases, errors due to nonideal averaging will *reduce* while the time it takes for the circuit to settle to the new rms level will *increase*. Therefore, lower input levels allow the circuit to perform better (due to increased averaging) but increase the waiting time between measurements. Obviously, when selecting C_{AV}, a trade-off between computational accuracy and settling time is required.

RAPID SETTLING TIMES VIA THE AVERAGE RESPONDING CONNECTION (FIGURE 17)

Because the average responding connection does not use an averaging capacitor, its settling time does not vary with input signal level; it is determined solely by the RC time constant of C_F and the internal 8 kΩ output scaling resistor.

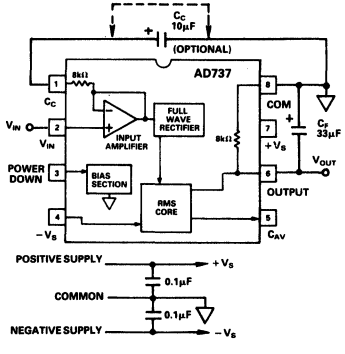


Figure 17. AD737 Average Responding Circuit

DC ERROR, OUTPUT RIPPLE, AND AVERAGING ERROR

Figure 18 shows the typical output waveform of the AD737 with a sine-wave input voltage applied. As with all real-world devices, the ideal output of $V_{OUT} = V_{IN}$ is never exactly achieved; instead, the output contains both a dc and an ac error component.

As shown, the dc error is the difference between the average of the output signal (when all the ripple in the output has been removed by external filtering) and the ideal dc output. The dc error component is therefore set solely by the value of averaging capacitor used—*no* amount of post filtering (i.e., using a very large C_F) will allow the output voltage to equal its ideal value.

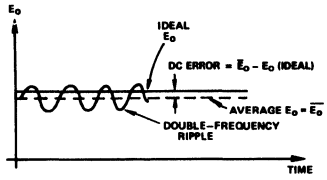


Figure 18. Output Waveform for Sine Wave Input Voltage

The ac error component, an output ripple, may be easily removed by using a large enough post filtering capacitor, C_F.

In most cases, the combined magnitudes of both the dc and ac error components need to be considered when selecting appropriate values for capacitors C_{AV} and C_F. This combined error, representing the maximum uncertainty of the measurement is termed the "averaging error" and is equal to the peak value of the output ripple plus the dc error. As the input frequency increases, both error components decrease rapidly: if the input frequency doubles, the dc error and ripple reduce to 1/4 and 1/2 their original values respectively and rapidly become insignificant.

AC MEASUREMENT ACCURACY AND CREST FACTOR

The crest factor of the input waveform is often overlooked when determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms amplitude (CF = V_{PEAK}/V rms). Many common waveforms, such as sine and triangle waves, have relatively low crest factors (≥2). Other waveforms, such as low duty cycle pulse trains and SCR waveforms, have high crest factors. These types of waveforms require a long averaging time constant (to average out the long time periods between pulses). Figure 6 shows the additional error vs. crest factor of the AD737 for various values of C_{AV}.

SELECTING PRACTICAL VALUES FOR INPUT COUPLING (C_C), AVERAGING (C_{AV}) AND FILTERING (C_F) CAPACITORS

Table II provides practical values of C_{AV} and C_F for several common applications.

Application	RMS Input Level	Low Frequency Cutoff (−3 dB)	Max Crest Factor	C_{AV}	C_F	Settling Time* to 1%
General Purpose RMS Computation	0–1 V	20 Hz	5	150 μF	10 μF	360 ms
		200 Hz	5	15 μF	1 μF	36 ms
	0–200 mV	20 Hz	5	33 μF	10 μF	360 ms
		200 Hz	5	3.3 μF	1 μF	36 ms
General Purpose Average Responding	0–1 V	20 Hz		None	33 μF	1.2 sec
		200 Hz		None	3.3 μF	120 ms
	0–200 mV	20 Hz		None	33 μF	1.2 sec
		200 Hz		None	3.3 μF	120 ms
SCR Waveform Measurement	0–200 mV	50 Hz	5	100 μF	33 μF	1.2 sec
		60 Hz	5	82 μF	27 μF	1.0 sec
	0–100 mV	50 Hz	5	50 μF	33 μF	1.2 sec
		60 Hz	5	47 μF	27 μF	1.0 sec
Audio Applications						
Speech	0–200 mV	300 Hz	3	1.5 μF	0.5 μF	18 ms
Music	0–100 mV	20 Hz	10	100 μF	68 μF	2.4 sec

*Settling time is specified over the stated rms input level with the input signal increasing from zero. Settling times will be greater for decreasing amplitude input signals.

Table II. AD737 Capacitor Selection Chart

The input coupling capacitor, C_C, in conjunction with the 8 kΩ internal input scaling resistor, determine the −3 dB low frequency rolloff. This frequency, F_L, is equal to:

$$F_L = \frac{1}{2\pi\ (8{,}000)\ (\textit{The Value of } C_C \textit{ in Farads})}$$

Note that at F_L, the amplitude error will be approximately −30% (−3 dB) of reading. To reduce this error to 0.5% of reading, choose a value of C_C that sets F_L at one tenth the lowest frequency to be measured.

In addition, if the input voltage has more than 100 mV of dc offset, then an ac coupling network at Pin 2 should be used in addition to capacitor C_C.

Applications Circuits

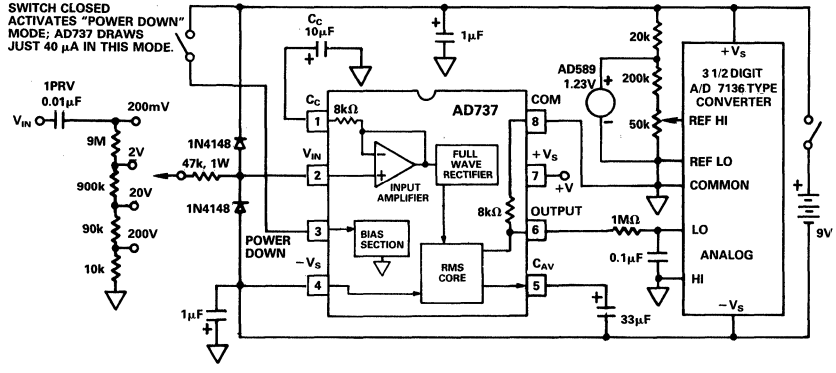


Figure 19. 3 1/2 Digit DVM Circuit

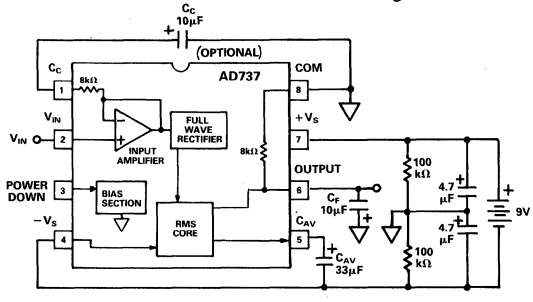


Figure 20. Battery Powered Operation for 200 mV max RMS Full-Scale Input

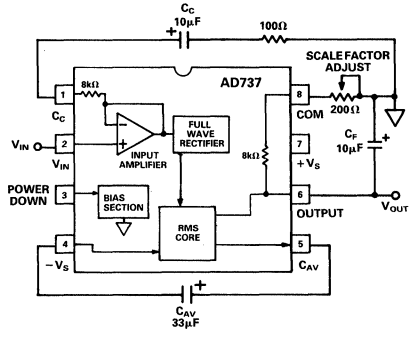


Figure 21. External Scale Factor Trim

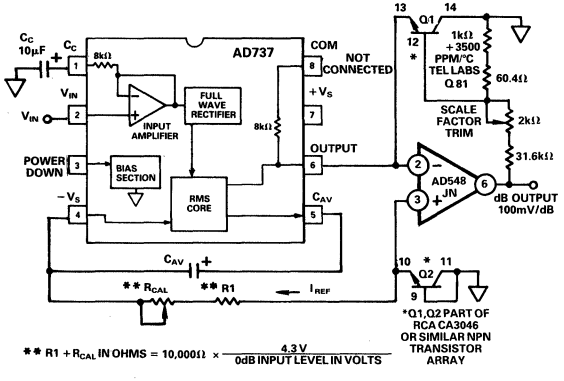


Figure 22. dB Output Connection

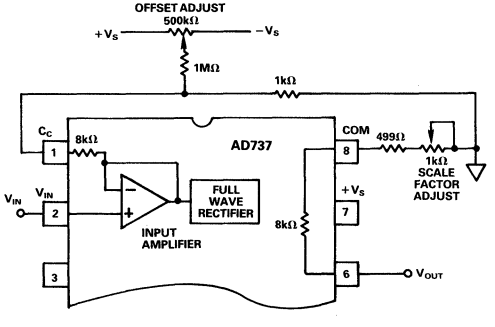


Figure 23. DC Coupled V_{OS} and Scale Factor Trims

Mass Storage Components
Contents

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Selection Guides
Mass Storage Components

Optical Storage Component

Model	Description	Package Options[1]	Temp[2]	Page
AD880	**Optical Disk Drive Data/Servo Channel Processor**	**6**	**C**	**5-5**

Magnetic Storage Components

Model	Description	Package Options[1]	Temp[2]	Page
AD890	**Precision, Wideband Channel Processing Element**	**3, 5**	**C**	**5-7**
AD891	**Rigid Disk Data Channel Qualifier**	**3, 5**	**C**	**5-9**
AD891A	**50 Mb/s Rigid Disk Data Qualifier**	**5**	**C**	**5-11**
AD892T/E	**30 Mb/s Peak Detector**	**5**	**C**	**5-13**
***AD896**	**Programmable Filter**	**2, 6**	**C**	**5-15**
AD897	**40 Mb/s Peak Detector and Data Synchronizer**	**10**	**C**	**5-27**
***AD899**	**32 Mb/s Read-Channel Electronics**	**6**	**C**	**5-29**

Other Mass Storage-Related Components

Servo Components

Model	Description	Package Options[1]	Temp[2]	Page[3]
AD7569	Complete, 8-Bit Analog I/O Port with DAC, ADC, SHA, Amps, and Reference	2, 3, 4, 5	C, I, M	C II
AD7669	Complete, 8-Bit Analog I/O Port with 2 DACs, ADC, SHA, Amps, and Reference	2, 5	C, I, M	C II
AD7769	8-Bit Analog I/O Port with Two-Channel ADC/DAC	2, 5	C	C II

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[3]C II = *Data Converter Reference Manual, Volume II.*
Boldface Type: Product recommended for new design.
*New product.

Our mass storage components offer the industry's highest performance products specifically designed for optical or magnetic disk drives.

AD880: The AD880 is a servo/data channel processing element for an optical disk drive. It is configured around four matched transimpedance amplifiers and normalization circuitry enabling it to perform all of the signal processing needed to generate the data, normalized track and normalized focus signal.

Figure 1 depicts a functional block diagram of the read electronics in a magnetic disk drive and the corresponding functional integration being offered by each of our hard disk products.

AD890/AD891 or AD890/AD891A: Both pairs of products comprise a chip set to perform the peak detection function in high performance disk drives (up to 50 Mb/s). The AD890 offers read channel designers flexibility by offering dual ×4 buffers which enable the channel designer to separate the low pass filtering function from the pulse slimming filters. The AD890 also offers a very fast 1 μs AGC loop. Two choices of data qualifiers—AD891 and AD891A—are offered as a companion chip to the AD890. Each data qualifier offers a different but highly accurate data qualification algorithm with extremely low pulse pairing.

AD892: The AD892 integrates the same function as the AD890/AD891 pair at a data transfer rate of 30 Mb/s. By maintaining the same architectural features of the AD890/AD891, the AD892 offers a smaller form factor, while not compromising design flexibility.

AD896: The AD896 is a 7th order Bessel filter with a programmable cutoff frequency and equalization/boost. Two versions are offered, 5–13 MHz cutoff frequency range and 9–23 MHz cutoff frequency range. Both versions have a 0 dB–9 dB boost range.

AD897: The AD897 incorporates an AGC, data qualifier and phase lock loop while offering a 40 Mb/s data transfer rate. The AGC and data qualifier architecture is very similar to the AD890/AD891A pair while employing a novel approach to the PLL architecture.

AD899: Our next generation Read/Write product, the AD899, offers a single chip 32 Mb/s read channel, including an AGC, filter/equalizer, data qualifier, data synchronizer, Endec, frequency synthesizer and a servo demodulator. The AD899 is offered in a 52-pin PQFP package.

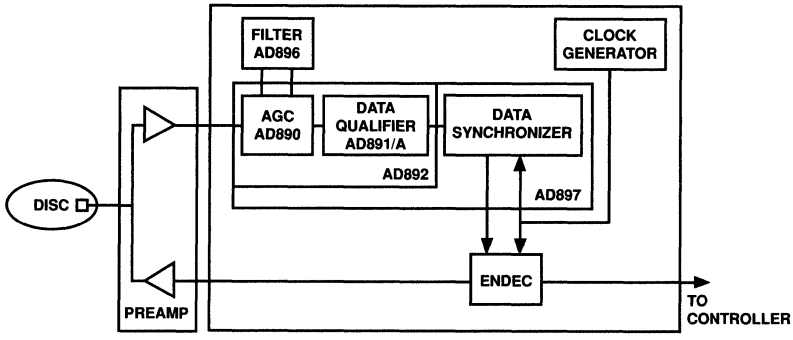


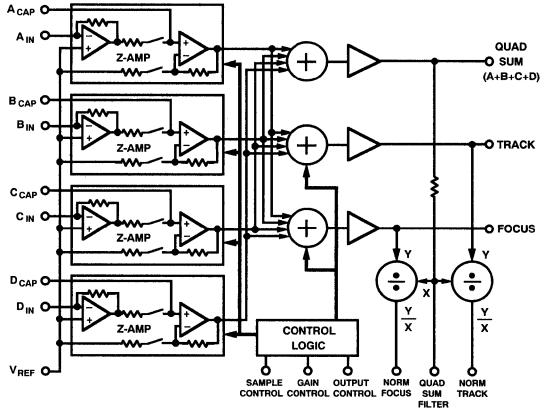
Figure 1.

Optical Disk Servo/Data Channel Processing Element

AD880

FEATURES
4 Matched Transimpedance Amplifiers
30 MHz Bandwidth
Selectable 36 kΩ/120 kΩ Transimpedance
Continuous or Sampled Servo Capability
Outputs:
Quad Sum
Track
Normalized Track
Focus
Normalized Focus
10 MHz Normalization Dividers
Fast Write Recovery with Sampling
Low Output Noise

FUNCTIONAL BLOCK DIAGRAM



5

PRODUCT DESCRIPTION

The AD880 is a monolithic integrated circuit intended for applications in the servo/read systems of an optical disk drive product.

The AD880 consists of four matched transimpedance amplifiers (A, B, C, D) with selectable 36 kΩ or 120 kΩ transimpedance. The basic transimpedance stage consists of a 10 kΩ transimpedance amplifier that drives a programmable X1 or X3.3 buffer. Each stage has been configured to minimize noise and noise peaking. To further enhance overall signal-to-noise performance an external capacitor may be added between the transimpedance amplifier and the programmable buffer to implement a first order low-pass filter.

The AD880 is stable over the full range of input source capacitances. To ensure stability and maximize available bandwidth in both transimpedance modes, the internal compensation capacitor in the programmable buffer is appropriately modified for each mode.

Fast read after write recovery is implemented through the transimpedance sample function. The "sample" function prevents the channel from saturating during writes. The "sample capacitor" also serves the dual purpose of providing the low-pass filter.

In addition, the part contains three offset trimmed summing amplifiers with 30 MHz bandwidth. One amplifier provides the Quad-Sum output that can be low-pass filtered prior to driving the normalization dividers. Two other summing amplifiers generate the Track and Focus outputs.

- Quad Sum : (A+B+C+D)
- Track : (A+D) − (B+C) or (A−B)
- Focus : (A+C) − (B+D) or (C−D)

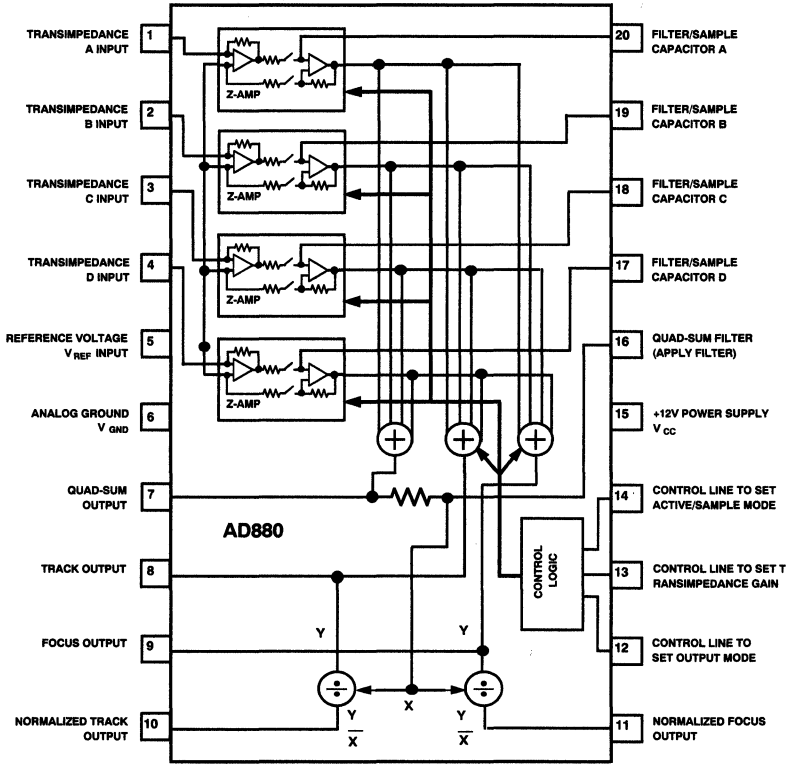
The selectable outputs are programmed through a CMOS compatible control line.

Finally, a pair of two quadrant dividers are provided. These generate the normalized focus and track signals with an accuracy of 5%, and have bandwidths in excess of 10 MHz.

The AD880 is available in a 20-pin wide body SOIC package and is specified to operate over the 0°C to +70°C commercial temperature range. However, evaluation samples are available in a 20-pin side braze package.

This is an abridged version of the datasheet. To obtain a complete data sheet, contact your nearest sales office.

AD880 PIN ASSIGNMENTS



ORDERING GUIDE

Model No.	Package Description	Package Option*
AD880JR	20-Pin Small Outline	R-20

*R = Small Outline IC. For outline information see Package Information section.

ANALOG DEVICES

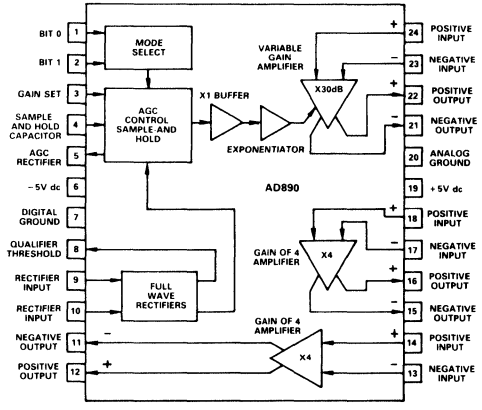
Precision, Wideband Channel Processing Element

AD890

FEATURES

- **An 80 MHz Bandwidth Permitting a 50 Mb/s Data Transfer Rate**
- **A Variable Gain Amplifier with 30 dB max Gain and 40 dB Control Range**
- **Two Gain of 4 RF Buffers**
- **200 Ω Differential Load Drive Capability**
- **A Pair of Precision Rectifiers**
- **AGC Level and Threshold Outputs**
- **An Averaging, High Gain Sample-and-Hold for Accurate AGC Operation**
- **Typical Gain Drift in Hold Mode: 0.2 dB/ms**
- **Gains Trimmed and Temperature Compensated**
- **AGC Operation Independent of AGC Level**
- **Symmetrical AGC Attack/Decay Times**
- **1 μs AGC Attack/Decay Times Using a 1000 pF External Capacitor**
- **Suitable for Use as an Accurate Video Programmable Gain Amplifier**
- **Dynamic Clamp Ensures Fast Recovery After Write to Read Transients**
- **AGC RF Output Level Is Internally Preset**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD890 is primarily intended for high performance disk subsystem use, and as such it is configured around the classic read channel processing block diagram. It is intended to be connected between the head preamplifier and the qualification circuitry required for digital data recovery. When used with the AD891 rigid disk data qualifier, data transfer rates in excess of 50 Mb/s can be processed.

A temperature-compensated AGC loop, with an exponential transfer characteristic, permits optimal settling and allows for predictable performance in the classic single integrator control loop configuration. Fast acquisition and low droop while in the hold mode allow for AGC operation to be performed within the sector header without compromising channel behavior when reading data.

The AD890 processing element has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Two user-defined filter/equalizer stages may be employed, thus allowing maximum design flexibility. This greatly simplifies the design of the overall channel characteristics. Using the AD890, the designer no longer needs to resort to passive techniques to isolate network functions; this avoids problems of signal loss and interaction. Two low offset, 100 MHz, full wave rectifiers provide the capability to track a 1 V peak signal. The rectifier generating the "Qualifier Threshold" output may be used for creating a data qualification level. A second rectifier is used to drive the sample-and-hold circuitry.

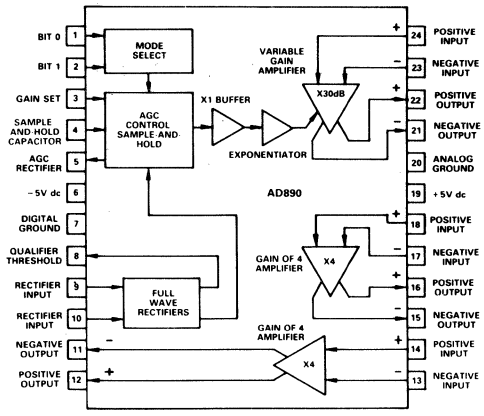
The 80 MHz bandwidth of the AD890 ensures good phase linearity up to 50 MHz. Thus, data transfer rates in excess of 50 Mb/s can be supported with good error rates and predictable channel behavior.

The AD890 is available in both a 24-pin, slim-line cerdip package and in a 28-pin PLCC package and is specified to operate over the 0 to +70°C commercial temperature range.

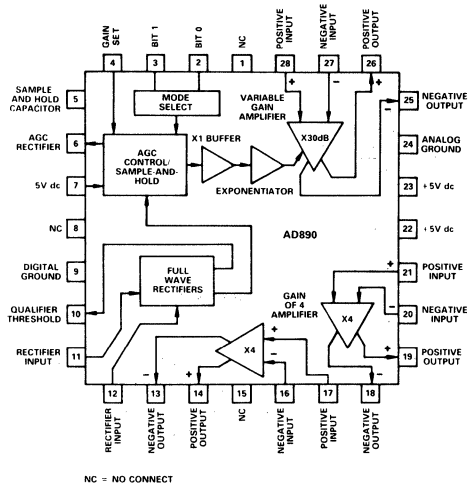
This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

PIN CONFIGURATIONS

24-Pin Cerdip Package



28-Pin PLCC Package



NC = NO CONNECT

ORDERING GUIDE

Model	Package Description	Package Option*
AD890JQ	24-Pin Cerdip	Q-24
AD890JP	28-Pin PLCC	P-28A

*For outline information see Package Information section.

ANALOG DEVICES

Rigid Disk Data Channel Qualifier

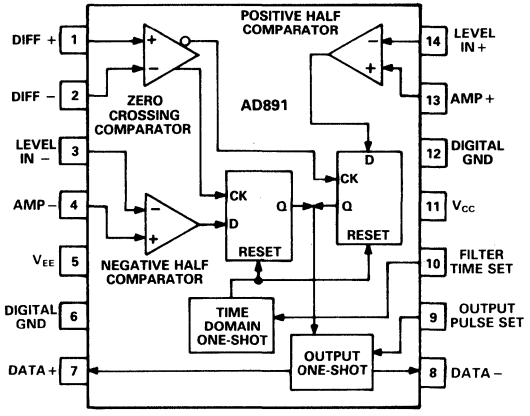
AD891

FEATURES

Three Matched, Offset-Trimmed Comparators
3.1 ns (typ) Comparator Propagation Delay
ECL Logic Permits 50 Mb/s Transfer Rates
6.8 ns Delay (typ) from Inputs to Data Output
500 ps (typ) Additional Pulse Pairing
Temperature-Compensated Operation
Compatible with 10 KH ECL Logic
Two Temperature-Compensated One-Shots
One-Shot Periods Set Using External Resistors

FUNCTIONAL BLOCK DIAGRAM

Cerdip (Q) Package



PRODUCT DESCRIPTION

The AD891 disk channel qualifier is intended as a companion chip to the AD890 wideband channel processor. Together, they comprise a sophisticated package, capable of recovering binary information from differentiating channels with transfer rates in excess of 50 megabits per second.

The AD891 provides both level and time-domain qualification. Level qualification is performed on alternating half cycles of the data waveform using a user-defined threshold level which is applied to each of two 3.1 ns propagation delay comparators. This technique prevents single bit errors from being propagated into two bit errors. A third comparator is used to provide zero-crossing detection. Factory trimmed offsets and a careful internal layout ensure symmetric operation and low pulse pairing with a differential input waveform.

An external RLC passive delay-line differentiator should be used with the AD891; the design for a typical network is specified in detail in the applications section of this data sheet. The use of an external network permits equal delay times through both the differentiated and undifferentiated signal paths, thus ensuring correct centering of the qualification windows. Using the recommended external network also helps ensure optimal signal passband flatness and dispersion.

The outputs from the amplitude-qualification comparators are applied to the "D" inputs of two master-slave D-type flip-flops which are then clocked by the outputs from the zero-crossing comparator. Each valid zero-crossing event causes a one-shot with a user-definable period to be triggered. This disables the operation of the flip-flops, thus preventing the detection of additional zero-crossing events during the one-shot period.

Simultaneously, an output one-shot is activated, the leading edge of which is synchronous with the change in the flip-flop outputs. The period of this one-shot is also user-definable and is intended to ensure adequate output pulse duration for transmission within the external environment. Each one-shot requires a single metal-film resistor to set its period. All one-shots have trimmed pulse periods; temperature stability is maintained by the use of an internal bandgap reference.

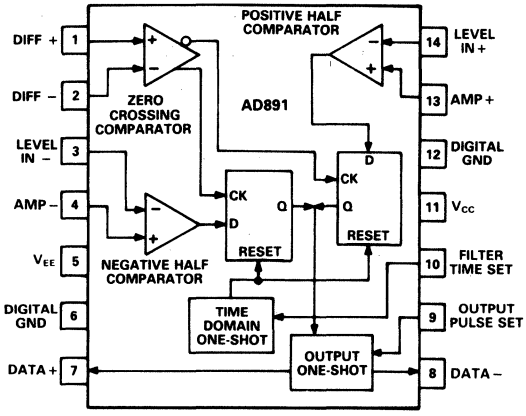
The AD891's internal logic consists of temperature-compensated reduced-swing ECL which exhibits typical propagation delays of 600 ps per gate. The output data conforms to standard 10 KH ECL logic levels. The AD891 can drive a properly terminated 75 Ω transmission line.

The AD891 is specified to operate over the commercial (0 to +70°C) temperature range. It is available either in a 14-pin cerdip package or in a 20-pin PLCC package.

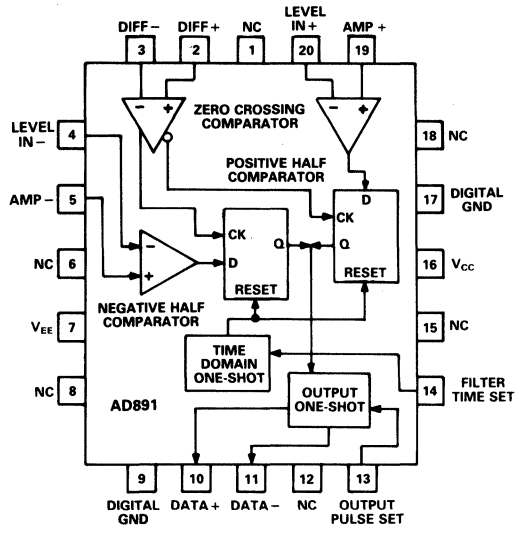
This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

PIN CONFIGURATIONS

14-Pin Cerdip (Q) Package



20-Pin PLCC (P) Package



ORDERING GUIDE

Model No.	Package Description	Package Option*
AD891JQ	14-Pin Cerdip	Q-14
AD891JP	20-Pin PLCC	P-20A

*For outline information see Package Information section.

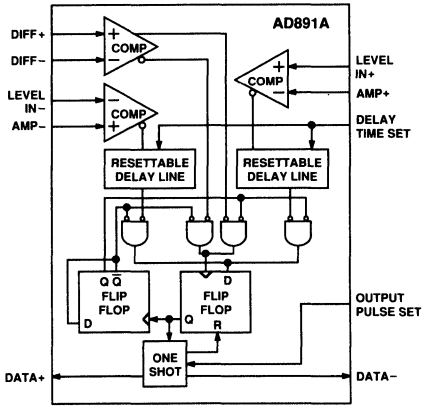
50 Mb/s Rigid Disk Data Qualifier

AD891A

FEATURES

- **Three Matched, Offset-Trimmed Comparators**
- **ECL Logic Permits 50 Mb/s Transfer Rates**
- **Three Levels of Data Qualification**
  - **Amplitude**
  - **Time Above Threshold**
  - **Polarity of Data**
- **100 ps Typical Additional Pulse Pairing**
- **Temperature Compensated Operation**
- **Compatible with 10KH ECL Logic**
- **One-Shot Period Set Using External Resistor**
- **Time Above Threshold Qualification Set Using an External Resistor**

FUNCTIONAL BLOCK DIAGRAM



5

PRODUCT DESCRIPTION

The AD891A disk channel qualifier is intended as a companion chip to the AD890 wideband channel processor. Together, they comprise a sophisticated package, capable of recovering binary information from differentiating channels with transfer rates in excess of 50 megabits per second.

The AD891A provides three levels of data qualification. Level qualification is performed on alternating half-cycles of the data waveform using a user-defined threshold level which is applied to each of two comparators. The outputs of each comparator drive a user-programmable "resettable" delay-line. The "resettable" delay-line function allows the user to define the minimum time a data pulse must exceed the amplitude qualification level before a zero-crossing can be detected. The resettable delay-lines drive NAND gated flip-flops. A third zero-crossing comparator is employed to clock the NAND gated flip-flop. The NAND-gated flip-flop in turn drives the second flip-flop. The second flip-flop feeds back to the input of the NAND-gated flip-flop. The toggle action of the second flip-flop, therefore, provides alternate polarity data qualification. To ensure symmetric operation and low pulse pairing, all three comparators have trimmed offsets.

An external RLC passive delay-line/differentiator should be used with the AD891A; the design for a typical network is specified in detail in the applications section of this data sheet. The use of an external network permits equal delay times through both the differentiated and undifferentiated signal paths, thus ensuring correct centering of the qualification windows. Using the recommended external network also helps ensure optimal signal passband flatness and dispersion.

Each valid data pulse causes a one-shot to generate a pulse with a user-defined width. During the one-shot period the NAND-gated flip-flop is disabled, preventing detection of additional zero-crossing events. The one-shot also drives the ECL "Data Output" driver. The one-shot requires a single metal-film resistor to set its pulse width. Temperature stability is maintained by the use of an internal bandgap reference.

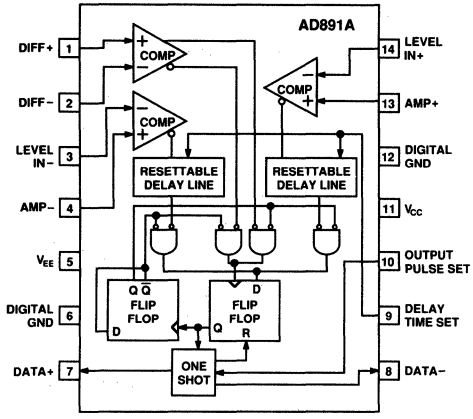
The AD891A's internal logic consists of temperature-compensated reduced-swing ECL which exhibits typical propagation delays of 600 ps per gate. The output data conforms to standard 10KH ECL logic levels. The AD891A can drive a properly terminated 75 Ω transmission line.

The AD891A is specified to operate over the commercial (0 to +70°C) temperature range. It is available in a 20-pin PLCC package (samples are available in a 14-pin side braze package).

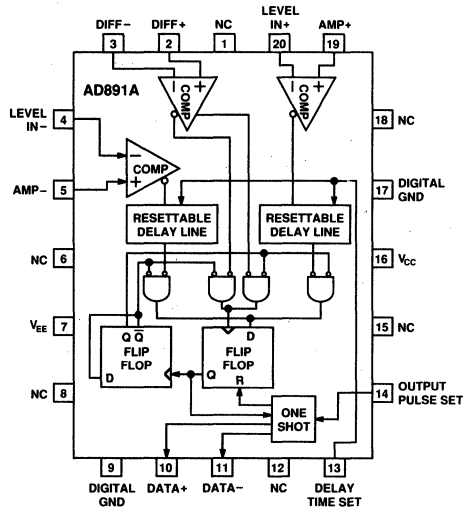
This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

PIN CONFIGURATIONS

14-Pin Side Brazed Package (D)



20-Pin PLCC Package (P)



ORDERING GUIDE

Model	Package Description	Package Option*
AD891AJP	20-Pin PLCC	P-20A
AD891AJD	14-Pin Side Brazed Ceramic DIP (Samples Only)	D-14

*For outline information see Package Outline section.

ANALOG DEVICES

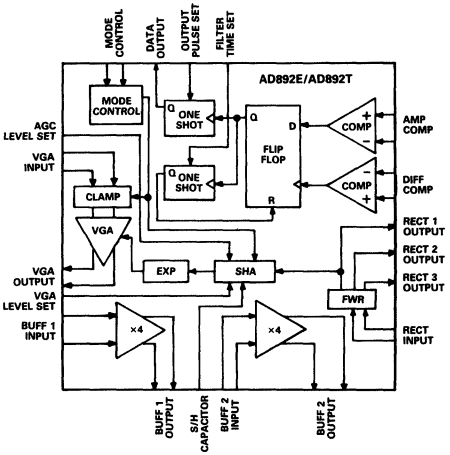
30 Mb/s Peak Detectors

AD892E/AD892T

FEATURES

30 Mb/s Data Transfer Rate Capability (AD892E)
25 Mb/s Data Transfer Rate Capability (AD892T)
1 ns (max) Additional Pulse Pairing
Two Versions
Differential ECL Data Output (AD892E)
TTL Data Output (AD892T)
Variable Gain Amplifier with 30 dB max Gain and 40 dB Control Range
Two Gain of 4 RF Buffers with 200 Ω Differential-Load Drive Capability
0.2 dB/ms Typical Gain Drift in Hold Mode
1 μs AGC Attack/Decay Times Using a 1000 pF External Capacitor
Dynamic Input Clamp Ensures Fast Recovery after Write to Read Transients
Two Matched Offset Trimmed Comparators
One-Shot Pulse Width Set Using External Resistor
Operates from +5 V and +12 V Supplies

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD892E/AD892T is a complete subsystem for recovering binary information from differentiating channels with transfer rates up to 30 megabits per second. It is connected to the output of the head amplifier and performs the signal conditioning and the data qualification task with a minimum of external components.

The AD892E/AD892T has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Fast acquisition and low droop while in the hold mode allows for the AGC operation to be performed within the sector header without compromising channel behavior when reading data. Two user-defined filter/equalizer stages may be employed, thus allowing maximum design flexibility. This greatly simplifies the design of the overall channel characteristics.

Three low offset, 50 MHz full-wave rectifiers are provided. One rectifier drives the internal sample-and-hold circuitry; this signal is available to the user to set the attack and decay characteristics of the sample and hold. The other two rectifier outputs are provided to generate the qualification level and to feed the single-ended passive differentiator. The threshold setting and differentiation is performed by an external RLC network.

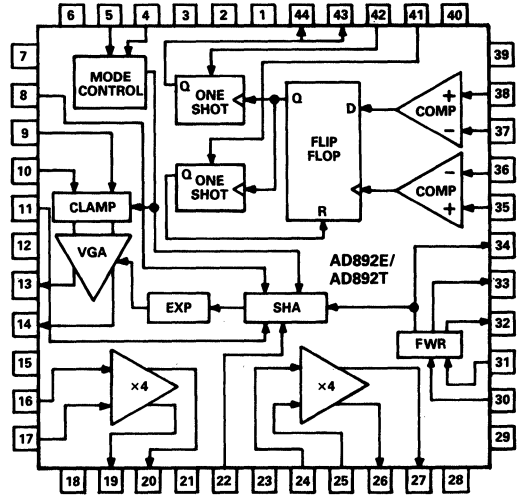
The AD892E/AD892T provides both level and time-domain qualification. Level qualification is performed on half cycles of the rectified data waveform using a user-defined threshold level which is applied to the level qualification comparator. The output of this comparator drives the data input of a master-slave flip-flop. A second, matched comparator detects zero-crossings and clocks the flip-flop. Each valid zero-crossing causes a time-domain filter one-shot to generate a pulse with a user-defined period. During the one-shot period the flip-flop is disabled, preventing the detection of additional zero-crossing events. This technique prevents single-bit errors from being propagated into two-bit errors. The zero-crossing event also triggers an output one-shot, again with a user defined pulse width. For maximum flexibility, the data output is a Schottky open-collector transistor with a separate digital ground to minimize digital feedthrough (AD892T) or differential ECL (AD892E).

The AD892E/AD892T is available in a 44-pin plastic leaded chip carrier (PLCC) and is specified to operate over the commercial (0 to +70°C) temperature range.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

PIN ASSIGNENTS

Pin	Description
1	+5 V Supply
2	No Connection (Can Be Left Floating)
3	No Connection (Can Be Left Floating)
4	Mode Control Bit B (TTL Compatible)
5	Mode Control Bit A (TTL Compatible)
6	Digital Ground
7	No Connection (Can Be Left Floating)
8	"AGC Level Set" Input Voltage
9	Variable Gain Amplifier Input (+)
10	Variable Gain Amplifier Input (−)
11	"VGA Level Set" Input Voltage
12	No Connection (Can Be Left Floating)
13	Variable Gain Amplifier Output (−)
14	Variable Gain Amplifier Output (+)
15	No Connection (Can Be Left Floating)
16	#1 12.75 dB Buffer Input (−)
17	#1 12.75 dB Buffer Input (+)
18	+12 V Supply (Analog)
19	#1 12.75 dB Buffer Output (+)
20	#1 12.75 dB Buffer Output (−)
21	No Connection (Can Be Left Floating)
22	Sample-and-Hold Capacitor
23	No Connection (Can Be Left Floating)
24	#2 12.75 dB Buffer Input (−)
25	#2 12.75 dB Buffer Input (+)
26	#2 12.75 dB Buffer Output (+)
27	#2 12.75 dB Buffer Output (−)
28	Analog Ground
29	No Connection (Can Be Left Floating)
30	Full Wave Rectifier Input (+)
31	Full Wave Rectifier Input (−)
32	Rectified Signal to Derive Threshold
33	Rectified Signal for Differentiator
34	Rectified Signal to S/H; AGC Attack and Decay Is Programmed at This Point
35	Zero Crossing Comparator Input (+)
36	Zero Crossing Comparator Input (−)
37	Minimum Threshold Level Input
38	Signal Amplitude Comparator Input
39	Internal Voltage Reference
40	+12 V Supply (Digital)
41	Apply Resistor to Program Time Domain Filter Pulse Width
42	Apply Resistor to Program Output Pulse Width
43	Data Output (Open Collector AD892T) Data Output (+ ECL AD892E)
44	Data Output Ground (Emitter of Output Device AD892T) Data Output (− ECL AD892E)



ORDERING GUIDE

Model No.	Package Description	Package Option*
AD892EJP	44-Pin PLCC	P-44A
AD892TJP	44-Pin PLCC	P-44A

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

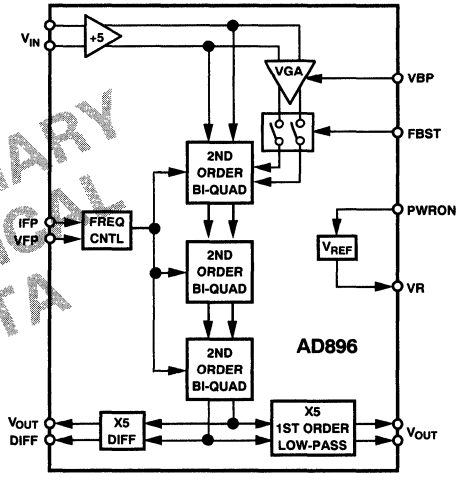
ANALOG DEVICES

Fully Programmable Filter

AD896

FEATURES
7th Order Bessel Filter
Programmable Characteristics
Cutoff Frequency
Boost Amplitude
Two Versions
13 MHz Max Cutoff Frequency AD896-13
23 MHz Max Cutoff Frequency AD896-23
Fully Differential Data Path
±10% Cutoff Frequency Accuracy
750 ps Group Delay Variation
Power-Down Function
16-Pin SOIC, Plastic DIP
+5 V Supply

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD896 is a seventh order Bessel filter with a programmable cutoff frequency and equalization/boost. The seventh order Bessel function provides excellent group delay characteristics making it ideal for applications requiring time domain signal integrity, such as in disk drive read channels. Group delay flatness for the AD896 is specified at ±750 ps over its complete operating range. The programmable equalization/boost function is implemented by a "$1-kS^2$" providing up to 9 dB boost. Since the "$1-kS^2$" function provides for two real and complementary zeros, it does not impact the group delay characteristics.

The AD896 signal path is completely differential for both the low-pass normal and differentiated signals. The normal and differentiated outputs have matched delays to ensure time coherency. By providing time coherent low-passed and differentiated signals, the AD896 easily replaces discrete low-pass filters and differentiators for most data qualification schemes in disk drive read channels.

With the advent of constant density recording, programmability of cutoff frequency and equalization/boost becomes a must. Programmability of the AD896 is easily achieved through analog control lines: IFP, VFP and VBP. The analog control lines may be readily interfaced with DACs for ultimate system flexibility.

Also, the equalization/boost function is enabled through a separate control line, FBST.

The AD896 also provides a power management capability. A separate control line provides the "power-up" function which enables the chip (logic level high) during read mode and disables (logic level low) it for power savings during write or idle mode. Power dissipation during idle mode is a low 50 mW.

The AD896 is available in a 16-pin narrow body SOIC, and plastic DIP; it is also specified to operate over the commercial (0°C to +70°C) temperature range.

AD896—SPECIFICATIONS

AD896-13 (@ 0°C ≤ T_A ≤ +70°C, 4.50 V ≤ V_{CC} ≤ 5.50 V)

Parameter		Conditions	Min	Typ	Max	Units
Filter						
FC	Filter Cutoff Frequency	FC = 16.25 MHz/mA × (IFP)	5		13	MHz
FCA	Filter Cutoff Frequency Accuracy	FC = 13 MHz	−10		+10	%
AO	V_{OUT} Norm Differential Gain	F = 0.67 FC, FB = 0 dB	0.8		1.2	V/V
AD	V_{OUT} Diff Differential Gain	F = 0.67 FC, FB = 0 dB	0.8AO		1.0AO	V/V
FB	Frequency Boost at FC	$FB(dB) = 20\ Log\left[1.884 \times \frac{(VBP)}{(VR)} + 1\right]$		9.2		dB
FBA	Frequency Boost Accuracy	FB = 9 dB	−1		+1	dB
TGDO	Group Delay Variation	0 dB ≤ FB ≤ 9.2 dB	−0.75		+0.75	ns
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 FC	1.5			V p–p
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 FC	1.5			V p–p
RIN	Filter Diff Input Resistance		3.0			kΩ
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage Differential Output	BW = 100 MHz, R_S = 50 Ω		5.5		mV rms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, R_S = 50 Ω		2.5		mV rms
IO−	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance				60	Ω
VR	Reference Voltage		2.0		2.4	V
IFP	Frequency Program Current	VR = 2.2 V	0.31		0.8	mA
VFP	Frequency Program Current	I_{VFP} = 0.33 × VR/RX, VR = 2.2 V[1]	0.31		0.8	mA
Logic Levels		TTL Inputs (PWRON, FBST)				
V_{IL}			−0.3		0.8	V
V_{IH}			2.0		V_{CC}+0.3	V
I_{IL}		V_{INPUT} = 0.8 V			−1.5	mA
I_{IH}		V_{INPUT} = 2.7 V			20	μA
Power Supply Requirements						
Supply Voltage V_{CC}			4.5	5.0	5.5	V
Supply Current I_{CC}		PWRON = 0.8 V		10	13	mA
		PWRON = 2.0 V		60	78	mA
Absolute Maximum Ratings[2]						
Supply Voltage V_{CC}					7.5	V
Storage Temperature Range			−65		+150	°C
Operating Temperature Range[3]			0		+70	°C
Lead Temperature Range		Soldering 60 Sec			300	°C

NOTES

[1]RX is a series resistance placed between VR and VFP. The voltage difference between VR and VFP is .33 × VR.

[2]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.

[3]16-Pin Narrow Body SOIC Package θ_{JA} = 105°C/Watt
16-Pin Plastic DIP Package: θ_{JA} = 170°C/Watt.

Specifications subject to change without notice.

AD896-23 (@ 0°C ≤ T_A ≤ +70°C, 4.50 V ≤ V_{CC} ≤ 5.50 V)

Parameter		Conditions	Min	Typ	Max	Units
Filter						
FC	Filter Cutoff Frequency	FC = 28 MHz/mA × (IFP)	8.7		22.5	MHz
FCA	Filter Cutoff Frequency Accuracy	FC = 13 MHz	−10		+10	%
AO	V_{OUT} Norm Differential Gain	F = 0.67 FC, FB = 0 dB	0.8		1.2	V/V
AD	V_{OUT} Diff Differential Gain	F = 0.67 FC, FB = 0 dB	0.8AO		1.0AO	V/V
FB	Frequency Boost at FC	$FB(dB) = 20 \text{ Log} \left[1.884 \times \frac{(VBP)}{(VR)} + 1\right]$		9.2		dB
FBA	Frequency Boost Accuracy	FB = 9 dB	−1		+1	dB
TGDO	Group Delay Variation	0 dB ≤ FB ≤ 9.2 dB	−0.75		+0.75	ns
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 FC	1.5			V p–p
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 FC	1.5			V p–p
RIN	Filter Diff Input Resistance		3.0			kΩ
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage Differential Output	BW = 100 MHz, R_S = 50 Ω		5.5		mV rms
EOUT	Output Noise Voltage Normal Output	BW = 100 MHz, R_S = 50 Ω		2.5		mV rms
IO−	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance				60	Ω
VR	Reference Voltage		2.0		2.4	V
IFP	Frequency Program Current	VR = 2.2 V	0.31		0.8	mA
VFP	Frequency Program Current	I_{VFP} = 0.33 × VR/RX, VR = 2.2V[1]	0.31		0.8	mA
Logic Levels		TTL Inputs (PWRON, FBST)				
V_{IL}			−0.3		0.8	V
V_{IH}			2.0		V_{CC}+0.3	V
I_{IL}		V_{INPUT} = 0.8 V			−1.5	mA
I_{IH}		V_{INPUT} = 2.7 V			20	μA
Power Supply Requirements						
Supply Voltage V_{CC}			4.5	5.0	5.5	V
Supply Current I_{CC}		PWRON = 0.8 V		10	13	mA
		PWRON = 2.0 V		75	95	mA
Absolute Maximum Ratings[2]						
Supply Voltage V_{CC}					7.5	V
Storage Temperature Range			−65		+150	°C
Operating Temperature Range[3]			0		+70	°C
Lead Temperature Range		Soldering 60 Sec			300	°C

NOTES

[1]RX is a series resistance placed between VR and VFP. The voltage difference between VR and VFP is .33 × VR.

[2]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.

[3]16-Pin Narrow Body SOIC Package θ_{JA} = 105°C/Watt
16-Pin Plastic DIP Package: θ_{JA} = 170°C/Watt.

Specifications subject to change without notice.

AD896-13—Typical Characteristics

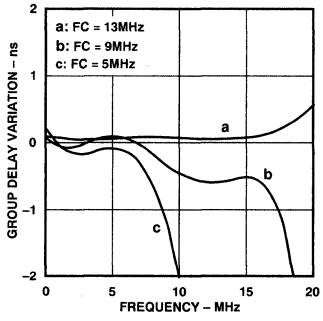


Figure 1. Normal Output Group Delay Variation vs. Frequency

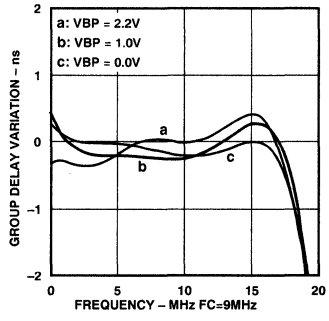


Figure 2. Normal Output Group Delay Variation vs. Frequency with Boost

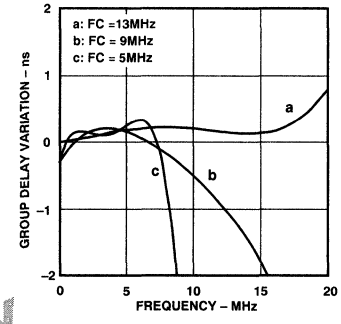


Figure 3. Differentiated Output Group Delay Variation vs. Frequency

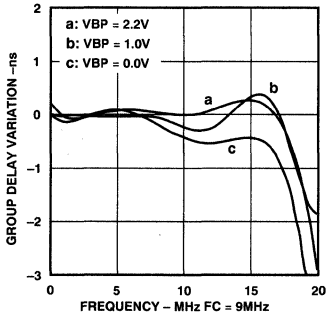


Figure 4. Differentiated Output Group Delay Variation vs. Frequency with Boost

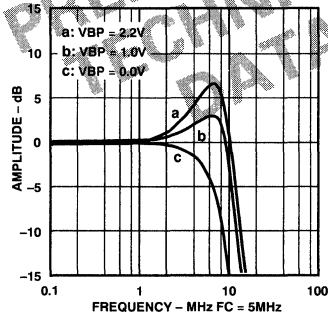


Figure 5. Normal Output Frequency Response with Boost

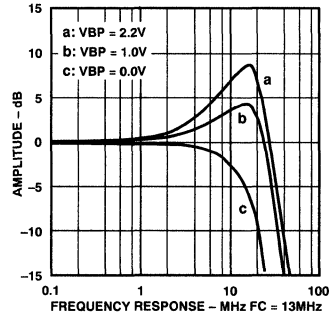


Figure 6. Normal Output Frequency Response with Boost

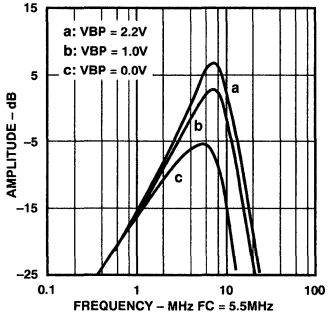


Figure 7. Differentiated Output Frequency Response with Boost

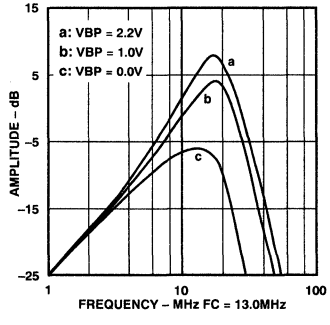


Figure 8. Differentiated Output Frequency Response with Boost

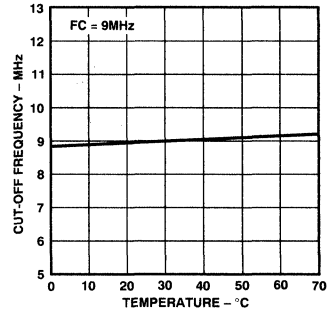


Figure 9. Cutoff Frequency vs. Temperature

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

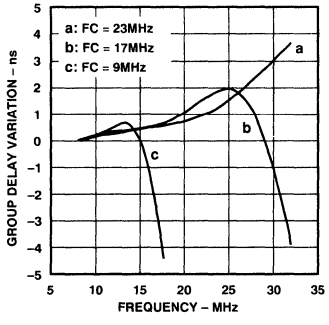


Figure 10. Normal Output Group Delay Variation vs. Frequency

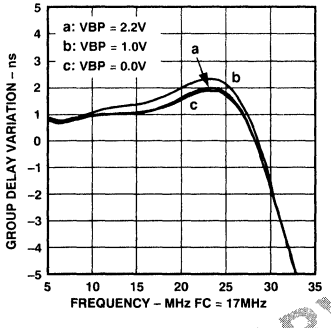


Figure 11. Normal Output Group Delay Variation vs. Frequency with Boost

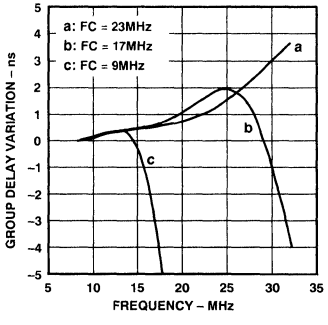


Figure 12. Differentiated Output Group Delay Variation vs. Frequency

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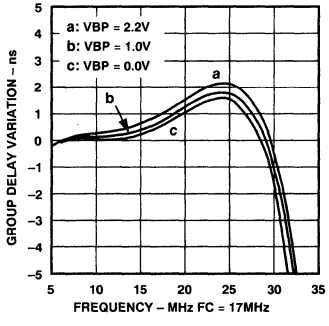


Figure 13. Differentiated Output Group Delay Variation vs. Frequency with Boost

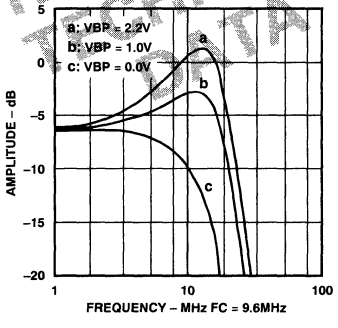


Figure 14. Normal Output Frequency Response with Boost

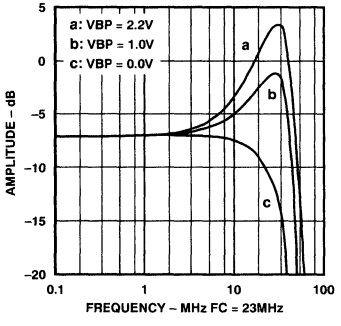


Figure 15. Normal Output Frequency Response with Boost

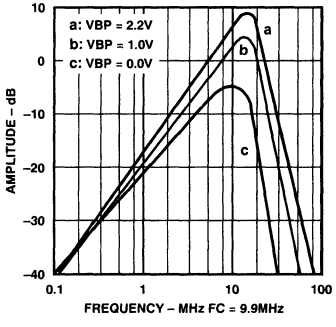


Figure 16. Differentiated Output Frequency Response with Boost

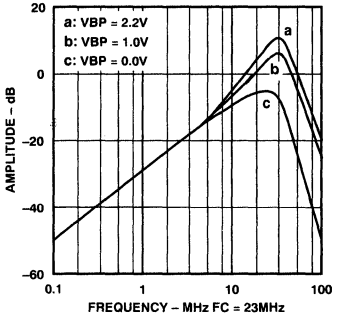


Figure 17. Differentiated Output Frequency Response with Boost

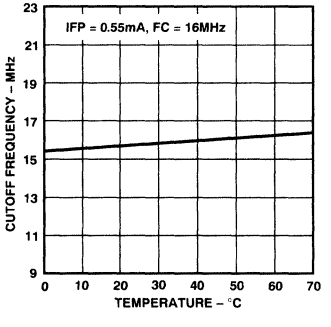
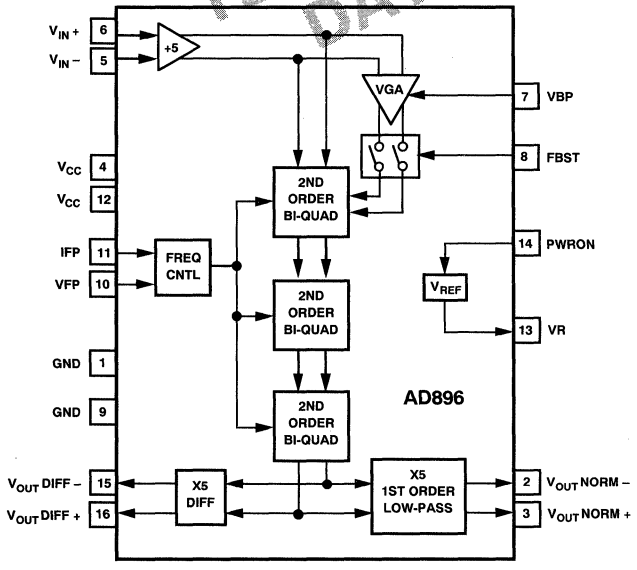


Figure 18. Cutoff Frequency vs. Temperature

Pin	Description	I/O Type	Application Notes
1	Ground	Power Input	
2	V_{OUT} NORMAL (Neg)	Analog Voltage Output	Low-Pass Filter Output, AC Couple
3	V_{OUT} NORMAL (Pos)	Analog Voltage Output	Low-Pass Filter Output, AC Couple
4	V_{CC} (+5 V dc)	Power Input	Decoupling with 0.1 μF‖0.01 μF Capacitors Required
5	V_{IN} (Neg)	Analog Voltage Input	Filter Input, Biased at V_{REF}, AC Couple Signal into Pin
6	V_{IN} (Pos)	Analog Voltage Input	Filter Input, Biased at V_{REF}, AC Couple Signal into Pin
7	VBP	Analog Voltage Input	Voltage to Set Amount of Boost
8	FBST	TTL Compatible Input	Boost/Equalizer Switch: Enabled (High Level), Disabled (Low Level)
9	Ground	Power Input	
10	VFP	Analog Current Input	Set Filter Cutoff Frequency. If VFP Is Used Leave IFP Floating
11	IFP	Analog Current Input	Set Filter Cutoff Frequency. If IFP Is Used Leave VFP Floating.
12	V_{CC} (+5 V dc)	Power Input	Decoupling with 0.1 μF‖0.01 μF Capacitors Required
13	VR	Voltage Output	Internally Generated Reference Voltage (2.2 V)
14	PWRON	TTL Compatible Input	Power-Up (High Level) or Power-Down (Low Level) the Chip
15	V_{OUT} DIFFERENTIATED (Neg)	Analog Voltage Output	Differentiated Output, AC Couple
16	V_{OUT} DIFFERENTIATED (Pos)	Analog Voltage Output	Differentiated Output, AC Couple

PIN CONFIGURATIONS



ORDERING GUIDE

Model	Description	Package Option*
AD896JR-13N	Narrow Body 16-Pin SOIC	R-16A
AD896JN-13	Plastic 16-Pin DIP	N-16
AD896JR-23N	Narrow Body 16-Pin SOIC	R-16A
AD896JN-23	Plastic 16-Pin DIP	R-16

*N = Plastic DIP; R = Small Outline IC (SOIC). For outline information see Package Information section.

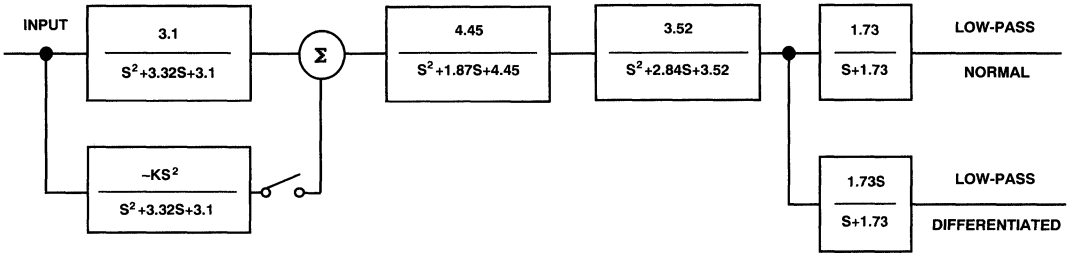


Figure 19. Block Diagram

FILTER OPERATION

The AD896 performs a seventh order Bessel function approximation by cascading three bi-quad sections and a single pole section to produce the normal low-pass output. The differentiated output is produced by placing a single zero, single pole section in parallel with the normal output single pole section. The architecture implemented in the AD896 ensures no time delay differential between the normal low-pass and the differentiated output. This is an important characteristic for data qualification schemes which depend on time coherency between the low-pass normal and differentiated read back signals. The normalized block diagram for the AD896 is shown in Figure 19.

The programmability of the AD896 is made possible by using variable transconductance amplifiers in the bi-quad sections to produce tunable amplifiers. The transconductivity (Gm) of each amplifier is changed by varying the current ratios in different stages of the amplifier. By varying the transconductance (Gm) the amplifier can be "tuned" to different frequencies. With the use of the tunable amplifiers in the bi-quad sections the cutoff frequency of the AD896 can be changed without changing external components or altering the approximation of the Bessel function. This makes the AD896 ideal for use in applications where programmable cutoff frequencies are desired.

The cutoff frequency of the AD896 is programmed by a control current which is used to tune the bi-quad sections. This control current can be applied directly to IFP or by connecting a voltage source in series with a resistor to VFP. By using a DAC the cutoff frequency can be microprocessor controlled (see application Figures 26 and 27).

Figure 20 and 21 are plots of IFP current versus cutoff frequency for the AD896-13 and AD896-23 respectively. Because the AD896 uses current to control the cutoff frequency of the filter the supply current varies with the setting of the cutoff frequency. Figure 22 and 23 illustrate the relationship between cutoff frequency and supply current for the AD896-13 and AD896-23, respectively.

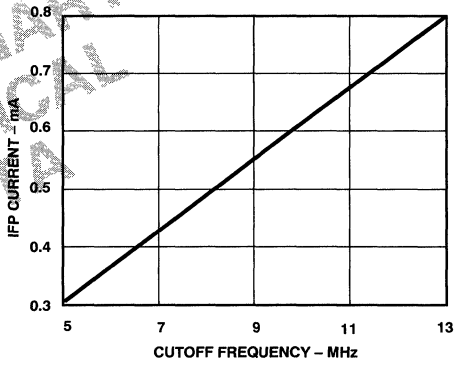


Figure 20. AD896-13 IFP Current vs. Cutoff Frequency

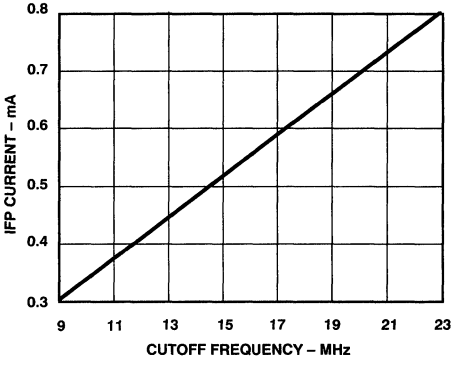


Figure 21. AD896-23 IFP Current vs. Cutoff Frequency

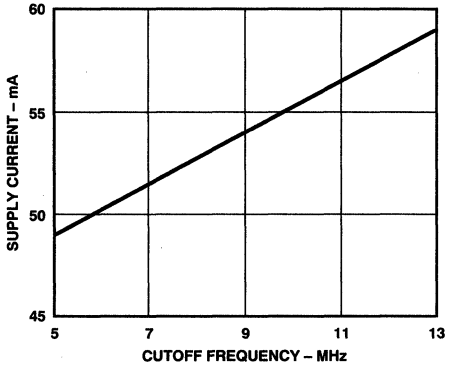


Figure 22. AD896-13 Supply Current vs. Cutoff Frequency

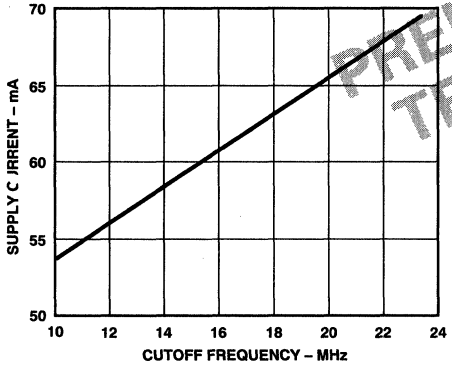


Figure 23. AD896-23 Supply Current vs. Cutoff Frequency

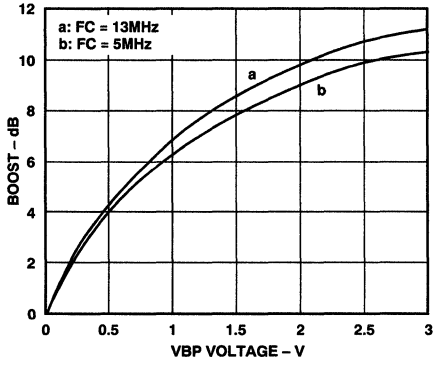


Figure 24. AD896-13 Boost vs. VBP Voltage

EQUALIZATION/BOOST

The Equalization/Boost can be enabled (high level) or disabled (low level) by a TTL input to the FBST pin. Gain equalization is performed, when enabled, by feeding forward the input signal and combining the signal with the low-pass filtered output of the first bi-quad section. The feed forward signal is amplified by a variable gain amplifier, which the user controls by applying a voltage to the VBP pin. The amplified signal is then summed together with the low-pass output of the first bi-quad and continues through the remaining bi-quad sections. The amount of boost is controlled by the voltage level applied to the VBF pin. The VBP voltage vs. Boost for the AD896-13 and AD896-23 are presented in Figures 24 and 25.

POWER-DOWN

Power management for the AD896 is achieved through the "PWRON" pin. A "high level" applied at this pin will enable the chip for normal operation. A "low level" applied to the PWRON pin will put the AD896 into the sleep mode. In the sleep mode, the AD896 will dissipate only 50 mW of power.

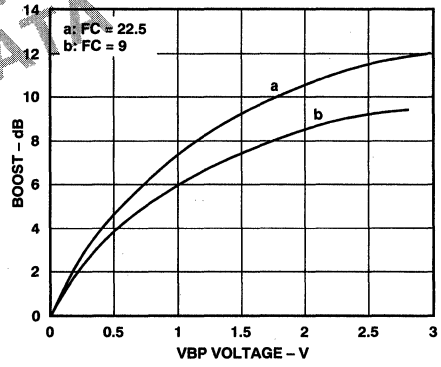


Figure 25. AD896-23 Boost vs. VBP Voltage

APPLICATIONS FOR THE AD896

The AD896 is a seventh order Bessel function filter with both programmable cutoff frequency and boost equalization. The AD896 is fully differential providing both low-pass normal and differentiated outputs with no time delay introduced between the two signals. The AD896 is ideally suited for applications where low group delay and time coherency between the normal low-pass and differentiated signals is a necessity. In order to enable the equalization/boost function the FBST must be held high (Logic Level 1), a low level will disable equalization.

Programming the cutoff frequency can be achieved through the IFP or VFP input. Both inputs are connected to the emitter of a PNP transistor which behaves as a current sink. The IFP input has a series combination of a 500 Ω resistor and two diodes. The input bias voltage at VFP is VR − 700 mV. The bias voltage at IFP with 300 μA program current is approximately VR + 200 mV; with 800 μA it is approximately VR + 500 mV. Programming of the AD896 through the IFP pin is achieved by varying the current from 0.3 mA to 0.8 mA. Programming the AD896 through the VFP is achieved by applying a voltage through a series resistor (R_X) to the VFP pin. The following formula can be used to calculate the current into the VFP: = (VFP voltage − 0.66 VR)/R_X.

Programming the amount of Boost is achieved by applying a voltage to the VBP input which is a high impedance input. The voltage range for operation is 0 to VR volts, where VR is the AD896 reference voltage (normally 2.2 V).

Figure 26 shows the AD896 being used along with an AD897 "40 mb/s Peak Detector and Data Synchronizer" and an AD7528 "CMOS Dual 8-Bit Buffered Multiplying DAC" in a constant density recording disk drive application. The cutoff frequency and equalization/boost are microprocessor controlled through the AD7528 dual DAC. The AD7528 is operated in the voltage mode with the reference being applied to OUTA (Pin 2) and OUTB (Pin 20) pins, the voltage output taken from V_{REF} A (Pin 4) and V_{REF} B (Pin 18). DAC A controls the voltage applied to the VBP pin for equalization/boost. The voltage from DAC B is used to develop a current which sets the cutoff frequency. Both outputs of the DAC are buffered through an OP-221 operational amplifiers before being applied to the AD896. The microprocessor controls the enabling/disabling of the equalization through the FBST input (Pin 8 high level = ON, low level = OFF), and the power up/ down of the filter is accomplished by the PWRON input (Pin 14 high level = ON, low level = OFF).

This application will allow the cutoff frequency to be changed by the processor to match the data rate of a particular zone (as in a disk drive) The amount of boost can also be changed as needed for different areas of the disk and for different data rates through DAC A. The low-pass normal and differentiated outputs of the AD896 are both needed for data qualification in the AD897. The AD896 is internally biased by VR (typically 2.2 V), therefore the input and output signals need to be ac coupled. The LSB of DAC B in this application corresponds to approximately 100 kHz after the bias voltage is reached of (0.66 VR). This will vary slightly with the reference voltage of different parts.

Figure 27 shows the AD896 being used as an antialiasing filter in a high speed data acquisition application. Using the AD773 "10-Bit 18 MSPS Monolithic A/D Converter," AD7528 "CMOS Dual 8-Bit Buffered Multiplying DAC," AD680 "2.5 V Reference," and a matched transistor pair. In this application the Boost is controlled by the DAC A voltage, the same as the previous application. The cutoff frequency is controlled by the current set up by the voltage out of DAC B and the matched transistors. This is a very accurate method of programming the cutoff frequency. The cutoff frequency must be set below Nyquist frequency (sample frequency/2) to prevent aliasing errors.

GENERAL LAYOUT REQUIREMENT

Care must be taken to ensure good RF practice in the PC layout to avoid oscillations. A parallel combination of 0.1 μF and 0.01 μF ceramic capacitors should be used as close to the V_{CC} (Pin 4 and Pin 12) as possible.

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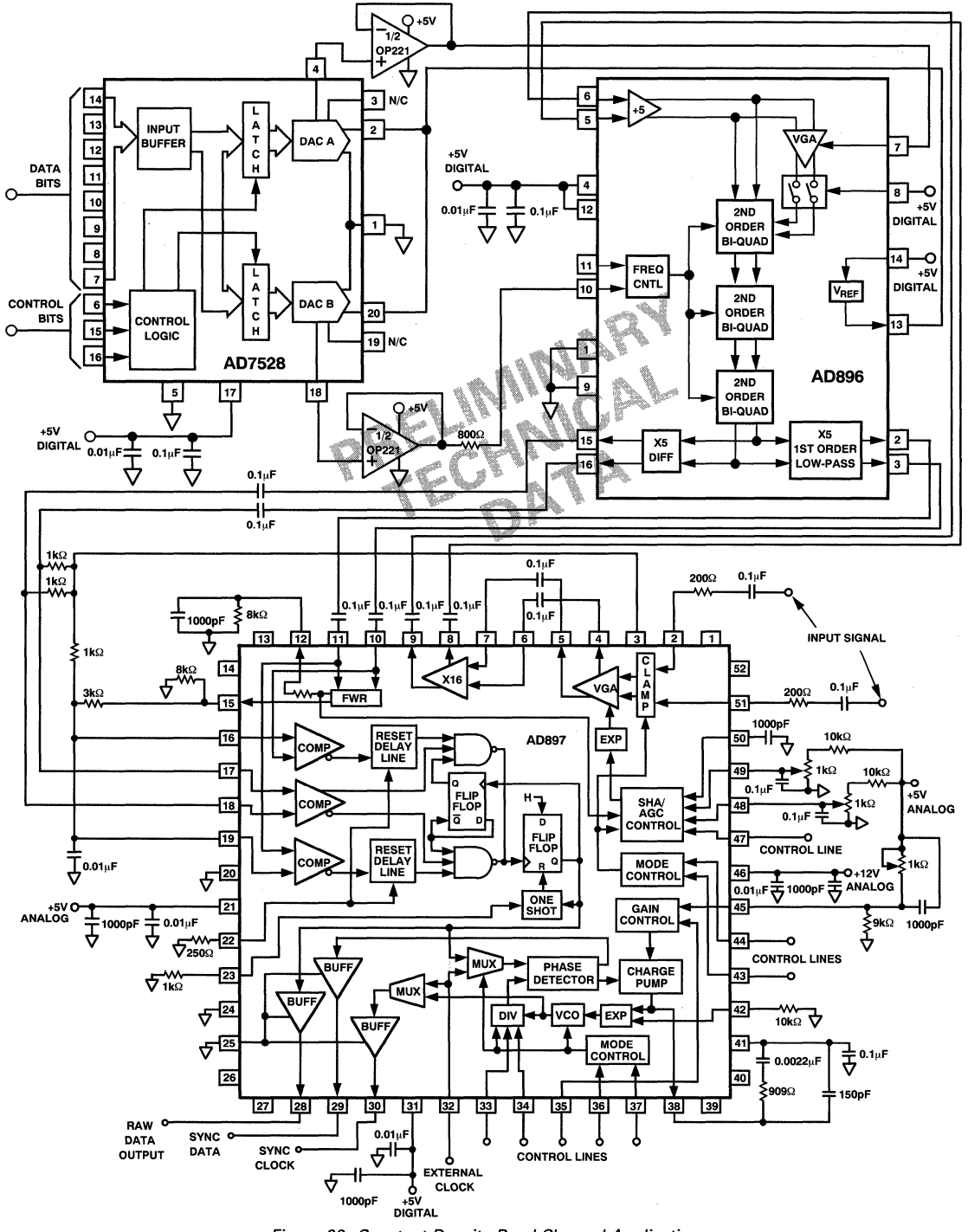


Figure 26. Constant Density Read Channel Application

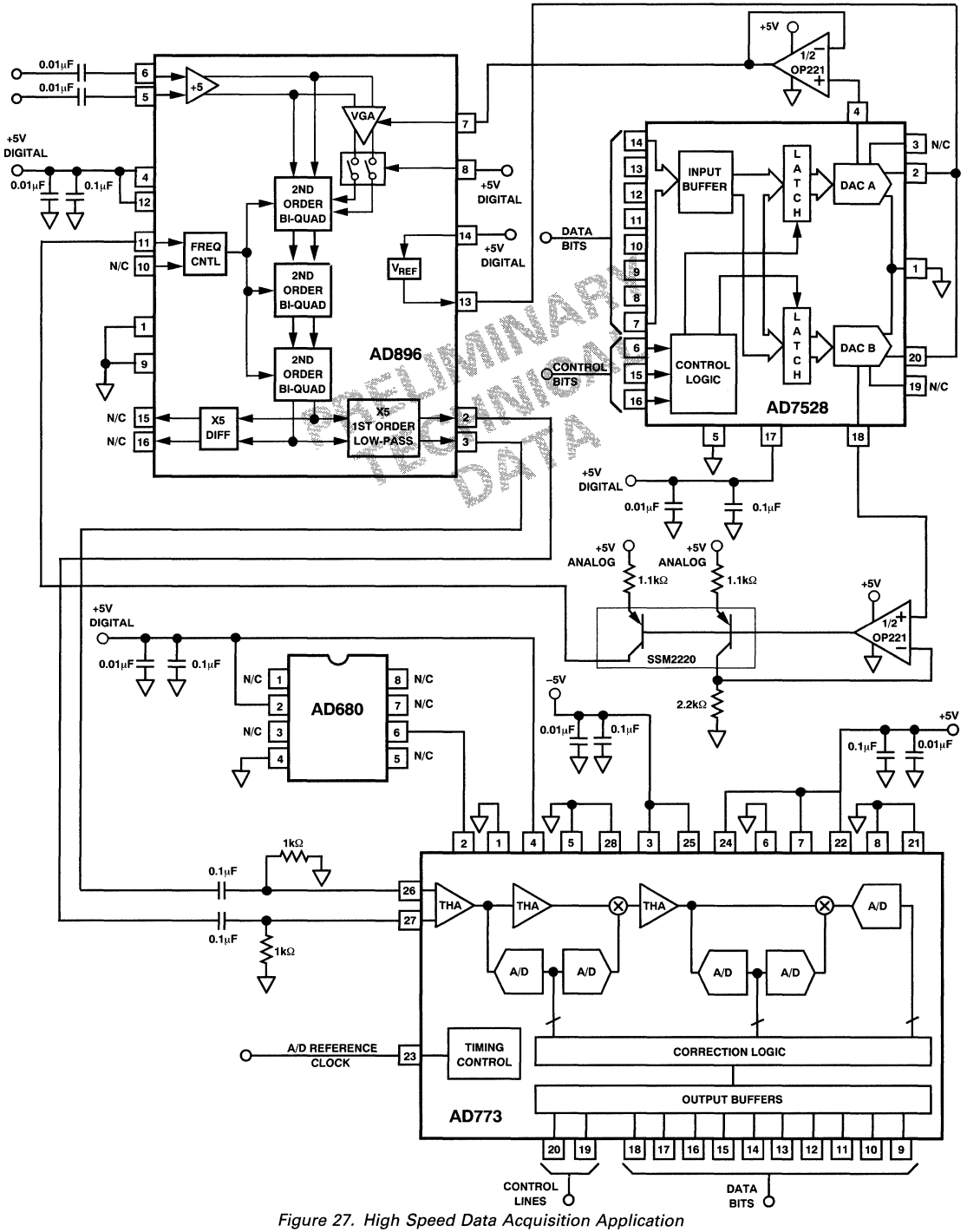


Figure 27. High Speed Data Acquisition Application

ANALOG DEVICES

40 Mb/s Peak Detector and Data Synchronizer

AD897

FEATURES

40 Mb/s Data Transfer Rate Capability
1000 ps (max) Additional Pulse Pairing
30 dB Gain VGA with 40 dB Control Range
24 dB Buffer with 200 Ω Differential Load Drive Capabilities
0.1 dB/ms Typical Gain Drift in Hold Mode
Symmetrical and User Programmable AGC Attack/Decay Times
Three Levels of Data Qualification
Amplitude Threshold
Time Above Threshold
Data Polarity
Offset Trimmed Zero Crossing Comparator
Zero Phase Error VCO Start-Up
No Phase Detector Dead Band at Center of Decode Window
Exponential VCO Control
52-Pin PQFP Package, +5 V and +12 V Supplies

PRODUCT DESCRIPTION

The AD897 is a complete solution for recovering binary information in a hard disk drive with data transfer rates up to 40 megabits per second. It is connected to the output of the head amplifier and performs the signal conditioning, data qualification and data synchronization tasks with a minimum of external components.

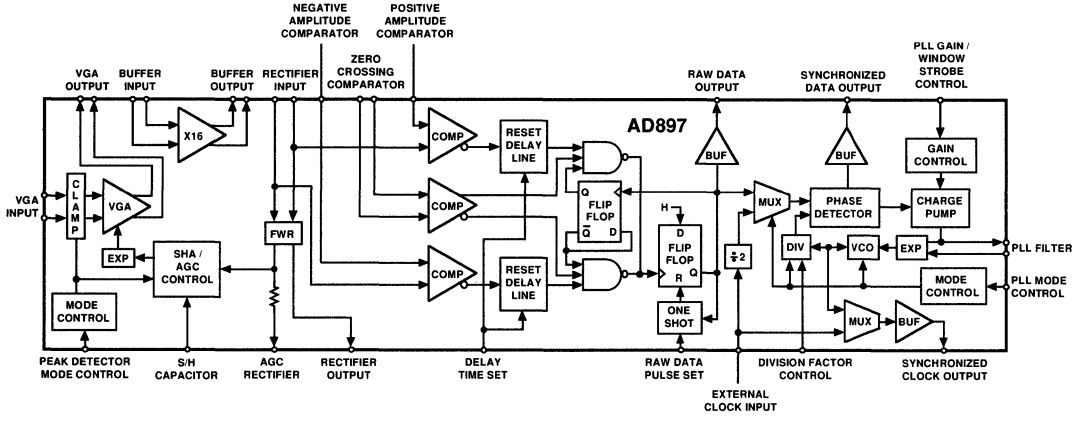
The AD897 has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Fast acquisition and low droop while in the hold mode allow for the AGC operation to be performed within the sector header without compromising channel behavior when reading data.

Three levels of data qualification are provided: amplitude threshold, time above amplitude threshold, and data polarity. Level qualification is performed on positive and negative cycles of the data waveform using a user-defined threshold level which is applied to the level qualification comparators. Each comparator then drives a resettable delay line, which implements the time above threshold qualification. Once the first two qualification criteria have been satisfied, a third comparator is able to detect a zero crossings and clock a flip-flop if the data also exhibits the correct polarity. Each clocking of the flip-flop causes a second flip-flop to toggle and thereby implement the polarity check. The valid data event also triggers an output one-shot, with a user-defined pulse width.

The data synchronizer section provides four modes of operation: lock to external clock, lock to preamble, lock to data, and tristate. The phase detector/charge pump utilizes a tri-phase pump-up, pump-down, pump-up approach in the lock to data mode, thereby ensuring no dead band zone in the center of the window. In addition, when switching to the lock to data mode, zero-phase error start-up is initiated. In the lock to external clock mode, feedback dividers provide the capability to achieve VCO to external clock ratios of 1:2, 1:1, 3:2, 2:1. When switching PLL operating modes, the charge pump is temporarily tristated to prevent the VCO control voltage from being disturbed.

The AD897 is available in a 52-pin plastic flat pack package (PQFP) and is specified to operate over the commercial (0°C to +70°C) temperature range.

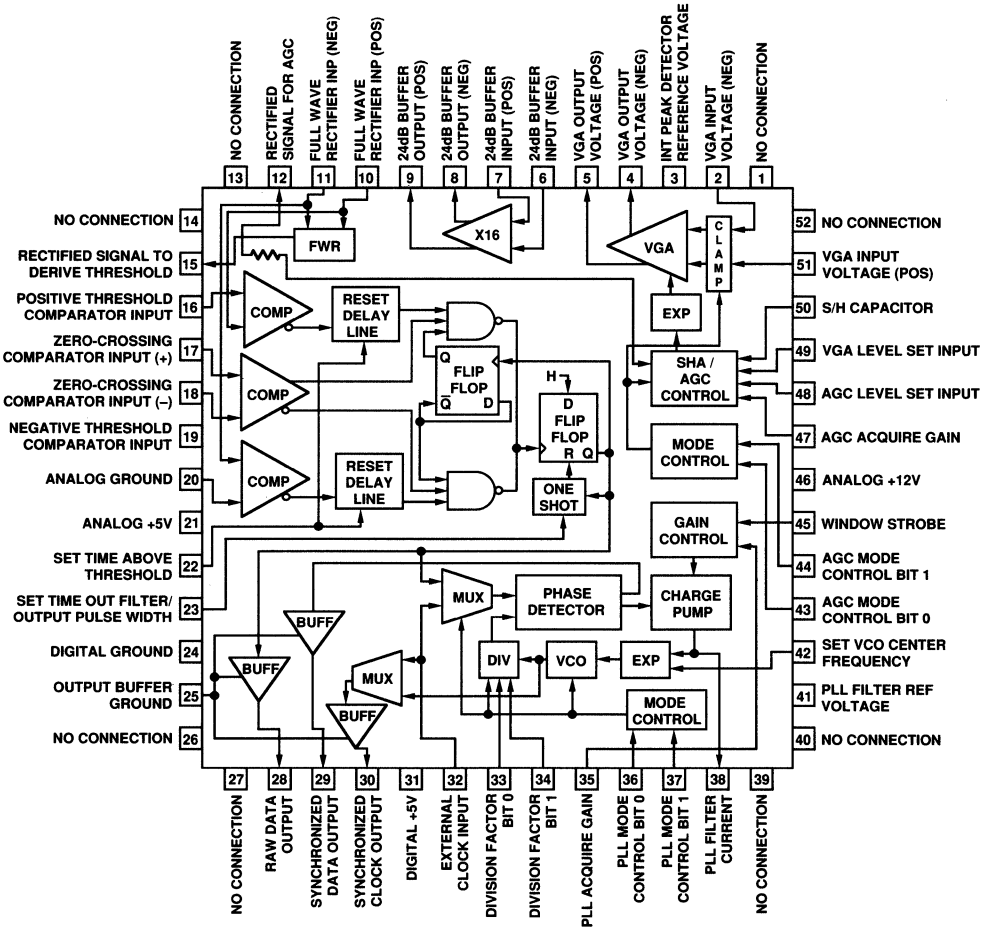
FUNCTIONAL BLOCK DIAGRAM



This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

CONNECTION DIAGRAM

52-Pin PQFP



ORDERING GUIDE

Model	Package Description	Package Option*
AD897JS	52-Pin PQFP	S-52

*For outline information see Package Information section.

ANALOG DEVICES

32 Mb/s Read Channel Electronics

AD899

FEATURES

32 Mb/s Data Transfer Rate Capability
Functionally Complete Read Channel Wideband AGC
- **Peak Hold Mode or Averaging**
- **7th Order Bessel Filter**
  - **Programmable Cutoff Frequency**
  - **Programmable Equalization**
- **Data Qualifier**
  - **Amplitude Qualification**
  - **Data Polarity Check**
- **Data Synchronizer**
  - **Zero Phase Start-Up**
  - **DAC Controlled Center Frequency**
  - **DAC Controlled Window Center**
- **1–7 ENDEC**
  - **Independent Early/Late Precompensation**
- **Write Clock Synthesizer**
  - **6-Bit M and N Dividers**
- **Servo Demodulator**
  - **A, B, C, D Sampling**
  - **Slew Rate Limiting or Peak Hold**

Power Down Options
52-Pin PQFP Package
+5 Volt Supply

PRODUCT DESCRIPTION

The AD899 offers a functionally complete read channel operating at up to 32 Mb/s and is completely compatible with constant density recording. When it is connected to the output of the head amplifier, it performs the signal conditioning, data qualification, data synchronization and Encoding/Decoding task with a minimum of external components. To support constant density recording, a high performance frequency synthesizer and a programmable filter are also included, as is a servo demodulator to support embedded servo applications.

The AD899 is ideally suited for a wide variety of applications given its built in flexibility. All major read channel characteristics are programmable on the AD899 through a standard serial port. The serial port controls the following critical characteristics: AGC setting, filter cutoff frequency and boost, data qualification amplitude threshold, data synchronizer center frequency and window center, write precompensation amount (Independent Early and Late), M and N divider ratios for the frequency synthesizer, as well as the power down options.

The AD899 will be available in a 52-pin quad flat pack package (PQFP) and is specified to operate over the commercial (0°C to +70°C) temperature range.

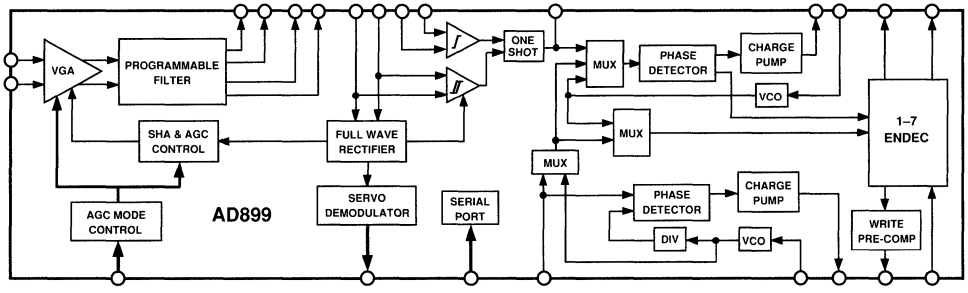
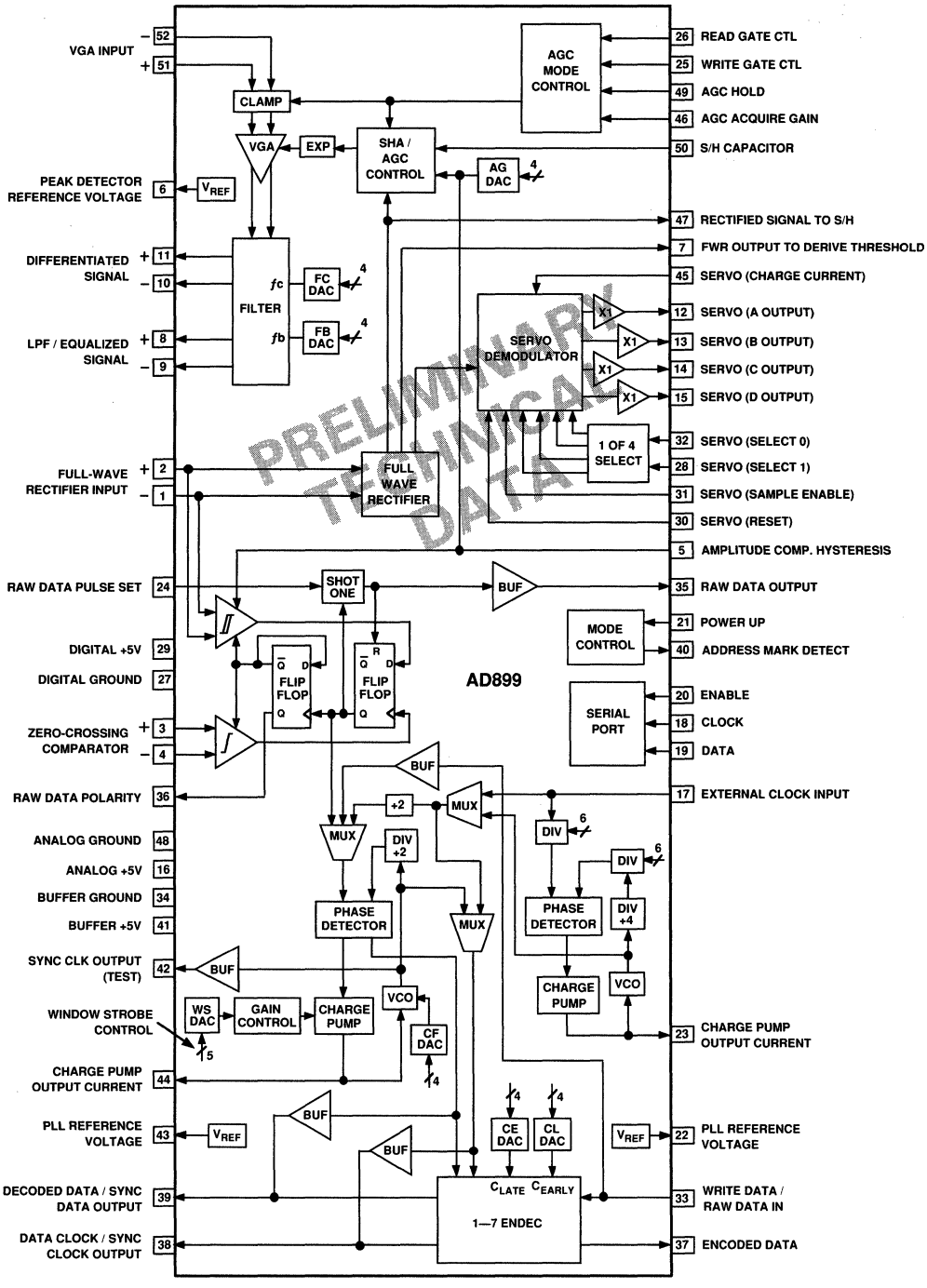


Figure 1. Simplified AD899 Block Diagram

AD899

FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ATE Components
Contents

Selection Guides
ATE Components

Pin Drivers

Model	Speed MHz	V_{RANGE}	Slew Rate at 5 V (V/ns)	Output Capacitance pF	Linearity % of V_{REF}	Package Options[1]	Temp Range[2]	Page
*AD1324	200	−2 V to 7 V	1.8	3.5	0.15	12	C	6-45
AD1321	100	−2 V to 7 V	1.25	8	0.5	12	C	6-33
*AD1320	40	−12 V to +12 V	0.5	20	0.5	3	C	6-27

Comparators

Model	Prop Delay ns	Common-Mode Range	Dispersion ps	Input Capacitance pF typ	Input Offset mv max	Package Options[1]	Temp Range[2]	Page
AD1317	2.5	−2 V to 7 V	250	2 (max)	±10	12	C	6-15
AD96685	3.5	−2.5 V to 5 V	50	2	2	3, 4, 5, 7	I, M	3-21
AD96687†	3.5	−2.5 V to 5 V	50	2	2	3, 4, 5	I, M	3-21
AD9696	7.0	−2.2 V to 3.7 V	100	3	2	2, 3, 6, 7	C, M	3-13
AD9698†	7.0	−2.2 V to 3.7 V	100	3	2	2, 3, 6	C, M	3-13

Active Load

Model	Prop Delay ns	Program Current mA	Input Leakage nA	V_{OUT} Capacitance pF	Package Options[1]	Temp Range[2]	Page
AD1315	1.5	±50	±200	2	12	C	6-7

Delay Generators

Model	Description	Package Options[1]	Temp[2]	Page
AD9500	ECL Digitally Programmable Delay Generator	3, 4, 5	C, M	6-57
AD9501	TTL/CMOS Digitally Programmable Delay Generator	2, 3, 5	C, M	6-67
*AD9505	60 MHz "On the Fly" Programmable Delay Generator	5	C	6-79

Other ATE-Related Components

Parametric Measurement Components

Model	Description	Package Options[1]	Temp Range[2]	Page[3]
AD676	**16-Bit, 10 µs Sampling ADC**	**1, 2**	**C, I, M**	**C II**
AD1377	16-Bit, 10 µs ADC	1	C	C II
AD1380	**16-Bit, 20 µs Sampling ADC**	**1**	**C**	**C II**
AD1382/AD1385	**16-Bit, 2 µs Sampling ADC**	**1**	**C, M**	**C II**

Custom Voltage/Current Force/Sense Functions

Level-Setting Components

Model	Description	Package Options[1]	Temp Range[2]	Page[3]
AD664	**Quad 12-Bit DAC, V_{OUT} Reset, Readback**	**1, 2, 4, 5**	**C, I, M**	**C I**
AD7228	Octal 8-Bit DAC, V_{OUT}	2, 3, 4, 5, 6	C, I, M	C I
AD7244	**Dual 14-Bit DAC, V_{OUT}, Ref, Serial I/O**	**2, 3, 6**	**C, I, M**	**C I**
AD7568	**Octal 12-Bit DAC, I_{OUT}, Serial I/O**	**10**	**I**	**C I**
AD75004	**Quad 12-Bit DAC, V_{OUT}, Reference**	**2, 5**	**C**	**C I**
AD75069	**Octal 12-Bit DAC, V_{OUT}, Readback, Ref**	**5, 14**	**C, I**	**C I**
DAC-8412	**Quad 12-Bit DAC, V_{OUT}, Reset to Midscale**	**1, 2, 4, 5**	**I, M**	**C I**
DAC-8413	**Quad 12-Bit, DAC, V_{OUT}, Reset to Zero**	**1, 2, 4, 5**	**I, M**	**C I**
SMP-08	**Octal Mux/SHA, 4 µs Acquisition Time**	**2, 3, 6**	**I, M**	**C II**
SMP-18	**Octal Mux/SHA, 2 µs Acquisition Time**	**2, 3, 6**	**I**	**C II**

Custom Multiple-DAC and/or Multiple-SHA Functions
Industry's Broadest Selection of DACs, from 8 to 20 Bits

Multiplexer

Model	Description	Package Option[1]	Temp Range[2]	Page[3]
AD75019	**16 × 16 Analog Crosspoint Switch**	**5**	**C, I**	**C II**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[3]C I = Data Converter Reference Manual, Volume I; C II = *Data Converter Reference Manual, Volume II.*
Boldface Type: Product recommended for new design.
*New product.
†Dual Comparators

Orientation
ATE Components

A complete ATE test-head design requires an appropriate mix of high speed, high performance components that are small enough to provide the needed functional density. Analog Devices provides a wide selection of components, based on various IC process technologies and logic families, to provide appropriate choices for ATE.

Designers of automatic test equipment (ATE) systems for advanced components have always had a dilemma; in order to test the newest, fastest, most precise products, they themselves need components that are even better than those they are testing. The unique design constraints of ATE add to the difficulties of assembling a system for testing high speed, high pin-count devices. The electrical interface between the device under test (DUT) and the rest of the ATE system is the *pin electronics*, a complex subsystem containing the functions needed to source precise signals to the DUT pins as well as measure DUT-generated signals. There is an identical—or nearly so—pin electronics circuit for each active pin of the DUT, arranged in a circle around the DUT at the test head to maximize achievable density and partially equalize propagation delays between pin electronics and the DUT.

The heart of the pin electronics is the pin driver. This device must produce highly repeatable, low jitter pulses with precisely set amplitude and slew rate for the DUT. The pin-driver timing is set digitally; its amplitude is determined by analog control voltages. Because of the high speeds of pin drivers—a 100 MHz repetition rate corresponds to a 5 ns pulse width—the driver and DUT are typically interconnected by a 50 Ω transmission line. The pin driver can be digitally disconnected via a high impedance three-state output mode, needed when the DUT has an input/output pin (two modes) that must be tested without physically disconnecting the driver.

Figure 1, a typical pin-electronics block diagram, shows the variety of devices needed for the complete function. Under control of the test computer and dedicated hardware, desired data patterns must be generated for simultaneous application to DUT inputs; at the same time, appropriate DUT outputs must be captured and measured. For complete parametric testing, signal levels must be precisely varied by the test program to determine maximum and minimum performance boundaries.

The complete pin-electronics function requires many digital-to-analog converters (DACs) to program the source current, sink current, and the threshold (commutation) voltage between current sourcing and sinking modes.

Although Figure 1 shows DACs setting key levels, many testers now use rapidly refreshed *sample/hold* circuits—driven by a shared, precise DAC. The S/H amplifier is used in *data distribution* instead of data acquisition, i.e., the S/H *holds* a digitally determined value during the test to establish a quasi-steady-state value instead of capturing an unknown signal value prior to digitizing it.

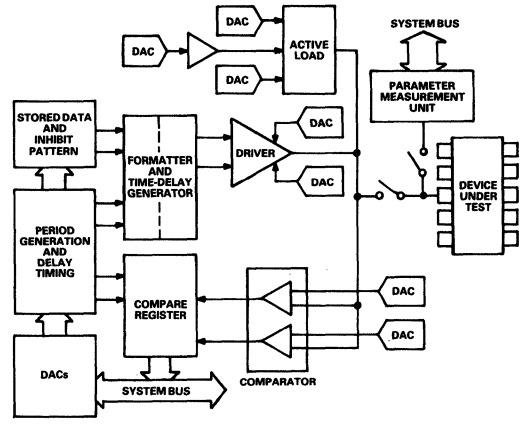


Figure 1. Typical Pin-Electronics Block Diagram; All Items Shown May Recur for Each Driven Pin in High Performance Systems

Unavoidable time skew occurs between signals from the many drivers as they reach the DUT. This is due to different path lengths (and therefore delays), as well as propagation delays within active components. To compensate for this, a time-delay deskewing circuit or delay line is included with each pin's electronics. The precise delay time must be set with high resolution; it is determined during the system calibration cycles or by actual test.

The pulse output of a DUT pin is measured to provide rise and fall times (time from 10 to 90 per cent of upswing or downswing), amplitudes, slew rate, and related information. For the short time periods associated with these parameters, the measurements are made using pairs of comparators; the comparator output changes state when the waveform under observation crosses a specific threshold value. The threshold values for all these comparators are established by DACs or S/H circuits, under control of the test computer. The comparator outputs, in turn are connected to circuits that measure the period between changes in output states of the comparators.

DESIGN CHALLENGES

The designer's task is made more difficult by many simultaneous and often conflicting demands, as ATE speeds reach 200 MHz (and beyond), and DUT package content increases:

- high speed signal transitions are affected by parasitic inductance and capacitance, which slow the transitions and affect waveshape fidelity.
- noise glitches induced by high speed signals corrupt signals in nearby wiring; although decoupling, short leads, and ground planes are a minimum line of defense against these, more advanced techniques, such as differential signal paths, may also be required.
- accuracy in measurement requires components whose dynamic performance is predictable and stable with time and temperature. For a 200 MHz pin driver, the leading-edge-to-trailing-edge matching specification should be better than 200 ps. Low *dispersion* (variation in propagation delay as a function of the input signal swing) reduces skewing and makes compensation more precise; for example, low dispersion is critical in memory testers, to minimize the need for compensating delay lines on their many data pins. Dispersion matching should be close, both within a device and from device to device, for ease of replacement and calibration.
- slew rates must also be controlled (2 V/ns for the 200 MHz driver) for performance consistency.
- undershoot and overshoot of the pin-driver output must be limited in amplitude.
- the DUT must be tested at its normal operating voltages–and stressed beyond these values, so the ATE components must typically be capable of functioning with signals from −2 to +7 volts.
- *mixed-signal* testing imposes *additional* requirements for signal linearity, ramping, precision, and distortion for typically 20 out of 64 DUT pins.

The constraints are not solely electronic; electromechanical factors are also significant:

- test-head pin counts are increasing from 64 (typically) to 512 pins, requiring that more electronic circuitry be packed into the limited available space; using a larger test head means more propagation-delay uncertainty, timing mismatches, and corresponding inaccuracies.
- power consumption of the high speed circuitry is relatively high, exceeding 3 watts per pin; cooling the large number of densely populated pin-electronic circuits is difficult.
- power consumption and heating, along with other factors, affect reliability, which must be very high in a multimillion dollar test machine; users expect satisfactory up time and test throughput.
- the layout of the test head must maintain signal fidelity; transmission-line impedances must be held constant to minimize signal reflections between DUT and pin electronics.
- and, of course, cost becomes a significant factor when the per-pin cost is multiplied by the large number of pins.

FUTURE ATE PRODUCTS

For further information on the above products and future ATE products not listed here, please contact the factory directly.

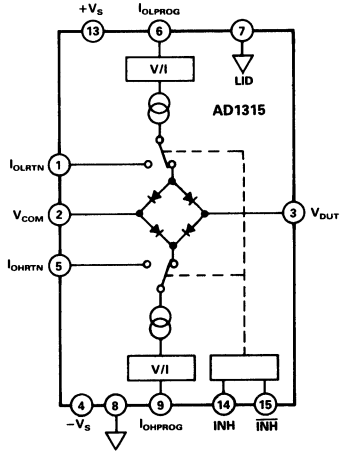
High Speed Active Load with Inhibit Mode

AD1315

FEATURES
±50 mA Voltage Programmable Current Range
1.5 ns Propagation Delay
Inhibit Mode Function
High Speed Differential Inputs for Maximum Flexibility
Hermetically Sealed Small Gull Wing Package
Compatible with AD1321, AD1324 Pin Drivers

APPLICATIONS
Automatic Test Equipment
Semiconductor Test System
Board Level Test System

FUNCTIONAL BLOCK DIAGRAM



6

PRODUCT DESCRIPTION

The AD1315 is a complete, high speed, current switching load designed for use in linear, digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities in an ultrasmall 16-lead, hermetically sealed gull wing package.

Featuring current programmability of up to ±50 mA, the AD1315 is designed to force the device under test to source or sink the programmed I_{OHPROG} and I_{OLPROG} currents. The I_{OH} and I_{OL} currents are determined by applying a corresponding voltage (5 V = 50 mA) to the I_{OH} and I_{OL} pins. The voltage-to-current conversion is performed within the AD1315 thus allowing the current levels to be set by a standard voltage out digital-to-analog converter.

The AD1315's transition from I_{OH} to I_{OL} occurs when the output voltage of the device under test slews above or below the programmed threshold, or commutation voltage. The commutation voltage is programmable from −2 V to +7 V, covering the large spectrum of logic devices while able to support the large current specifications (48 mA) typically associated with line drivers. To test I/O devices, the active load can be switched into a high impedance state (Inhibit mode) electrically removing the active load from the path through the Inhibit mode feature. The active load leakage current in Inhibit is typically 20 nA.

The Inhibit input circuitry is implemented utilizing high speed differential inputs with a common-mode voltage range of 7 volts and a maximum differential voltage of 4 volts. This allows for the direct interface to the precision of differential ECL timing or the simplicity of switching the Active Load from a single ended TTL or CMOS logic source. With switching speeds from I_{OH} or I_{OL} into Inhibit of less than 1.5 ns, the AD1315 can be electrically removed from the signal path "on-the-fly."

The AD1315 is available in a 16-lead, hermetically sealed gull wing package and is specified to operate over the ambient commercial temperature range from 0 to +70°C.

AD1315—SPECIFICATIONS (All measurements made in free air at +25°C. $+V_S$ = +10 V, $-V_S$ = −5.2 V, unless otherwise specified.)

Parameter	AD1315KZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
INH to $\overline{INH}$					
Input Voltage, Any One Input	−3.0		4.0	Volts	
Differential Input Range	0.4	ECL	4.0	Volts	
Bias Current	−2.0	1.0	2.0	mA	
Current Program Voltage Range					
I_{OH}, 0 mA to +50 mA (Sink)	0		+5.0	Volts	Note 1
I_{OL}, 0 mA to −50 mA (Source)	0		+5.0	Volts	Note 1
Input Resistance		50		kΩ	
I_{OHRTN}, I_{OLRTN} Range	−2.0		+7.0	Volts	Note 2
V_{COM}, V_{DUT} Range	−2.0		+7.0	Volts	
I_{OH}, 0 mA to 50 mA	0.5		+7.0	Volts	V_{DUT}–V_{COM}>1 V
I_{OL}, 0 mA to −50 mA	−2.0		+4.0	Volts	V_{COM}–V_{DUT}>1 V
OUTPUT CHARACTERISTICS					See Note 3
Active (Sink/Source) Mode					
Transfer Function		10		mA/V	See Figure 1
Accuracy					See Figure 1
Linearity Error	−0.12		+0.12	% FSR	
Gain Error	−2.0		+2.0	% FSR	
Offset Error	−1.0		+1.0	mA	
Output Current TC		10		μA/°C	
Inhibit Mode					
Output Capacitance			3.0	pF	
Inhibit Leakage	−200	20	200	nA	
DYNAMIC PERFORMANCE					See Note 3
Propagation Delay					See Figure 2
$\pm I_{MAX}$ to INHIBIT (t_{PD1})		0.5	1.5	ns	See Note 4
INHIBIT to $\pm I_{MAX}$ (t_{PD2})		1.5	3.0	ns	See Note 4
POWER SUPPLIES					
$-V_S$ to $+V_S$ Difference		15.2	15.4	Volts	
Supply Range					
Positive Supply	+9.5	+10	+10.5	Volts	
Negative Supply	−5.45	−5.2	−4.95	Volts	
Current					
Positive Supply	+70	+85	+100	mA	See Note 5
Negative Supply	−100	−85	−70	mA	See Note 5
Power Dissipation		1.3	1.54	Watts	See Note 6
PSRR			0.05	%/%	See Note 7

NOTES

[1] I_{OHPROG}/I_{OLPROG} voltage range may be extended to −100 mV due to a possible 1 mA offset current.

[2] I_{OHRTN}/I_{OLRTN} should be connected to V_{COM} to minimize power dissipation.

[3] V_{DUT} = −2 V to +7 V, C_{TOTAL} = 10 pF, R_{DUT} = 10 Ω. For inhibit leakage tests, V_{DUT} = 0 V to +5.9 V, I_{OH} = −4 mA, I_{OL} = +4 mA, T_{CASE} = +36°C.

[4] Measured from the ECL crossing to the 10% change in the output current.

[5] $I_{PROGRAM}$ = ±50 mA.

[6] Maximum power dissipation with $+V_S$ = +10 V, $-V_S$ = −5.2 V, $I_{PROGRAM}$ = ±50 mA, V_{COM} = V_{DUT} = 0V.

[7] For a 1% change in $+V_S$ or $-V_S$, the output current may change a maximum of 0.05% of Full Scale Range (FSR).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- $+V_S$ to GND . . . . . +12 V
- $-V_S$ to GND . . . . . −11 V
- Difference from $+V_S$ to $-V_S$ . . . . . 16 V

Inputs
- Difference from INH to $\overline{INH}$ . . . . . 5 V
- INH, $\overline{INH}$ . . . . . $+V_S$ −13.4 V, $-V_S$ +11 V
- V_{COM}, V_{DUT} . . . . . $+V_S$ −13.1 V, $-V_S$ +13.2 V
- I_{OL}, I_{OH} Program Voltage . . . . . $+V_S$ −15 V, $-V_S$ +15 V

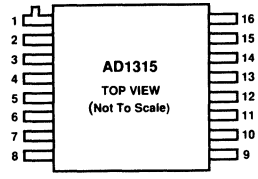
Operating Temperature Range . . . . . 0 to +70°C
Storage Temperature Range . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 20 sec)** . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**To ensure lead coplanarity (±0.002 inches) and solderability handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

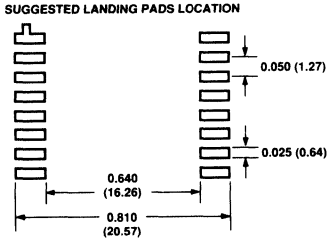
PIN NO.	SYMBOL	FUNCTION
1	I_{OLRTN}	LOGIC LOW CURRENT RETURN
2	V_{COM}	COMMUTATION VOLTAGE
3	V_{DUT}	LOAD/DUT CONNECTION
4	$-V_S$	NEGATIVE SUPPLY
5	I_{OHRTN}	LOGIC HIGH CURRENT RETURN
6	I_{OLPROG}	LOGIC LOW CURRENT PROGRAM VOLTAGE
7	LID	LID CONNECTION (INTERNAL)
8	GND	GROUND
9	I_{OHPROG}	LOGIC HIGH CURRENT PROGRAM VOLTAGE
10	N/C	NO CONNECTION
11	N/C	NO CONNECTION
12	N/C	NO CONNECTION
13	$+V_S$	POSITIVE SUPPLY
14	INH	INHIBIT
15	$\overline{INH}$	$\overline{INHIBIT}$
16	N/C	NO CONNECTION

CONNECTION DIAGRAM



SUGGESTED PAD LOCATION

Dimensions shown in inches and (mm).



ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD1315KZ	0 to +70°C	16-Lead Gull Wing	Z-16B

*For outline information see Package Information section.

DEFINITION OF TERMS

Gain

The measured transconductance.

$$Gain = \frac{I_{OUT}\ (@\ 5\ V\ Input) - I_{OUT}\ (@\ 0.2\ V\ Input)}{V_{PROG}\ (@\ 5\ V) - V_{PROG}\ (@\ 0.2\ V)}$$

where V_{PROG} values are measured at I_{OL}/I_{OH} PROG

Gain Error

The difference between the measured transconductance and the ideal expressed as a % of full-scale range.

$$Ideal\ Gain = 10\ mA/V$$

$$Gain\ Error = \frac{Ideal\ Gain - Actual\ Gain}{Ideal\ Gain} \times 100$$

Offset Error

Offset Error is measured by setting the I_{OHPROG} or I_{OLPROG} inputs to 0.2 V and measuring I_{OUT}. Since both I_{OH} and I_{OL} outputs are unipolar, this small initial offset of 2 mA must be set to allow for measurement of possible negative offset. With a gain of 10 mA/V, a 0.2 V input should yield an output of ±2 mA. The difference between the observed output and the ideal ± 2 mA output is the offset error.

$$Offset\ Error = I_{OUT}\ (@\ 0.2\ V) - Gain \times V_{PROG}\ (@\ 0.2\ V)$$

Linearity Error

The deviation of the transfer function from a straight line defined by Offset and Gain expressed as a % of FSR.

$$I_{OUT}\ (calc) = Gain \times V_{PROG}\ (@\ set\ point) + Offset$$

$$where\ set\ point = V_{PROG}\ (from\ 0.2\ V\ to\ 5\ V)$$

$$I_{OUT}\ (FSR) = Gain \times V_{PROG}\ (@\ 5\ V) + Offset$$

$$Linearity\ Error = \frac{I_{OUT}\ (measured) - I_{OUT}\ (calc)}{I_{OUT}\ (FSR)} \times 100$$

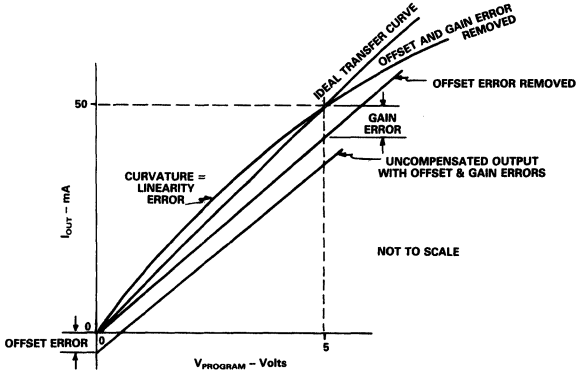


Figure 1. Definition of Terms

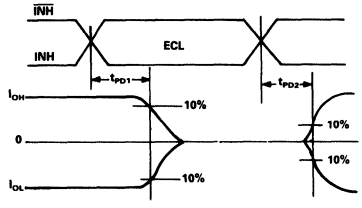


Figure 2. Timing Diagram for Inhibit Transition

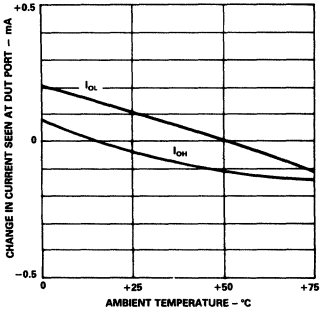


Figure 3. I_{OL}, I_{OH} Offset Current vs. Temperature

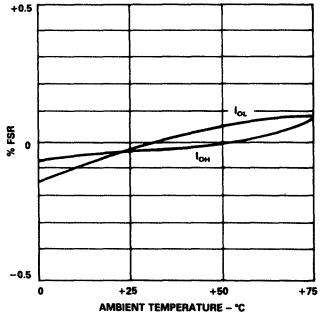


Figure 4. I_{OL}, I_{OH} Gain Error vs. Temperature

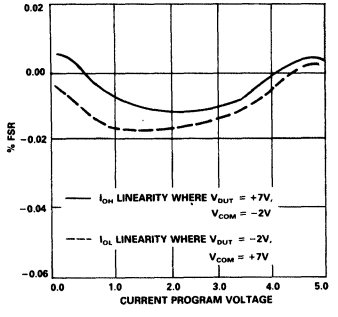


Figure 5. I_{OH}, I_{OL} Linearity Error vs. Current Program Voltage

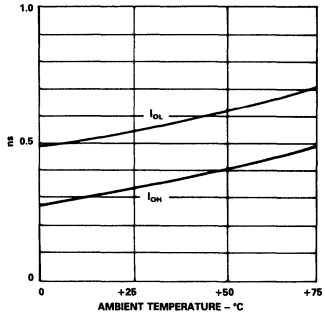


Figure 6. $+I_{MAX}$, $-I_{MAX}$ to Inhibit Propagation Delay vs. Temperature

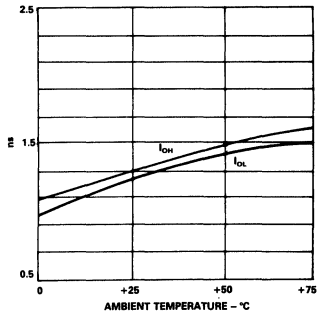


Figure 7. Inhibit to $+I_{MAX}$, $-I_{MAX}$ Propagation Delay vs. Temperature

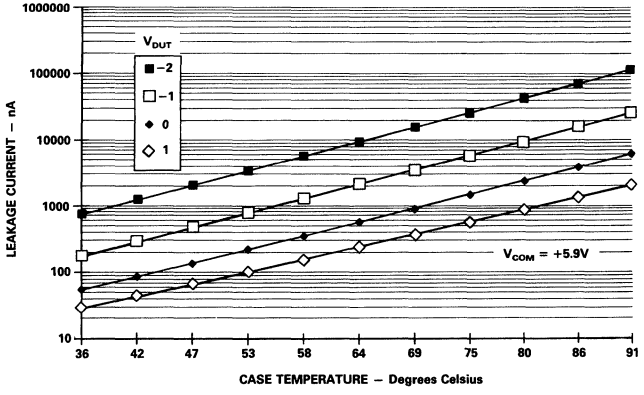


Figure 8. Inhibit Mode Leakage Current vs. Case Temperature

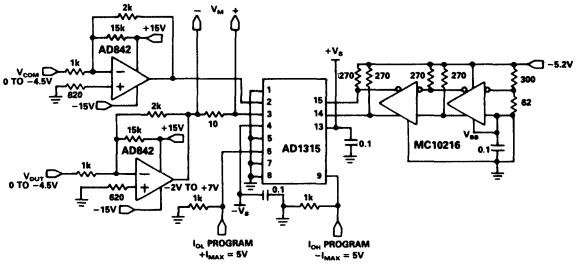


Figure 9. AD1315 DC Test Circuit

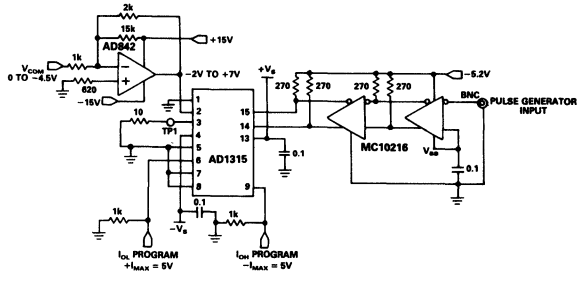


Figure 10. AD1315 Propagation Delay Test Circuit

FUNCTIONAL DESCRIPTION

The AD1315 is a complete high speed active load designed for use in general purpose instrumentation and digital functional test equipment. The function of the active load is to provide independently variable source and sink currents for the device to be tested.

The equivalent circuit for the AD1315 is shown in Figure 11. An active load performs the function of loading the output of the device under test with a programmed I_{OH} or I_{OL}. These currents are independently programmable. V_{COM} is the commutation voltage point at which the load switches from source to sink mode. The active load may also be inhibited, steering current to the I_{OLRTN} and I_{OHRTN} pins, effectively disconnecting it from the test pin.

The AD1315 accepts differential digital signals at its inhibit inputs ensuring precise timing control and high noise immunity. The wide inhibit input voltage range allows for ECL power supplies of −5.2 V and 0 V, −3.2 V and +2 V, and 0 V and +5 V. Where speed and timing accuracy are less important, TTL or CMOS logic levels may be used to toggle the Inhibit inputs of the AD1315. Single ended operation is possible by biasing one of the inputs to approximately +1.3 V for TTL or $V_{CC}/2$ for CMOS. Care should be taken to observe the 4 V maximum allowable input voltage.

The I_{OH} and I_{OL} programming inputs accept 0 V to +5 V analog inputs, corresponding to 0 to 50 mA output currents. The V_{COM} input, which sets the I_{OH}/I_{OL} switch point, may be set anywhere within the input range of −2 V to +7 V.

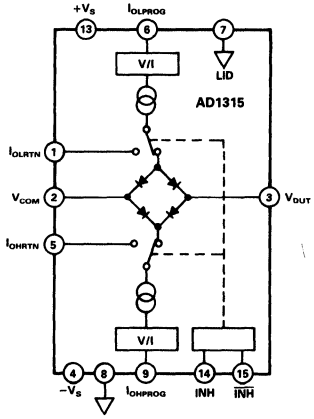


Figure 11. Block Diagram

V_{DUT} VOLTAGE RANGE

In Figure 12, V_{DUT} range, I_{OH} and I_{OL} typical current maximums are plotted versus DUT voltage. In the I_{OH} mode (V_{DUT} higher than V_{COM}), the load will sink 50 mA, until its output starts to saturate at approximately −1.5 V. In the I_{OL} mode (V_{DUT} lower than V_{COM}), the load will source 50 mA until its output starts to saturate at approximately +5.5 V. At +7 V, the source current will be close to zero.

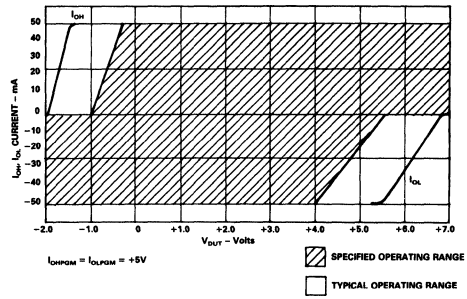


Figure 12. Allowable Current Range for I_{OH}, I_{OL} vs. V_{DUT}

Ideally, the commutation point set at V_{COM} would provide instantaneous current sink/source switching. Because of I/V characteristics of the internal bridge diodes, this is not the case. To guarantee full current switching at the DUT, at least a 1 volt difference between V_{COM} and V_{DUT} must be maintained in steady state conditions. Because of the relatively fast edge rates exhibited by typical logic device outputs, this should not be a problem in normal ATE applications.

INHIBIT MODE LEAKAGE

The AD1315's inhibit-mode leakage current changes with both temperature and bias levels. There are two major contributing effects: transistor reverse-bias collector-base leakage and reverse leakage in the Schottky-diode bridge. Leakage variations with V_{DUT} arise primarily from transistor collector-base leakage, while both effects contribute to leakage current temperature variations. Inhibit-mode leakage is weakly dependent on V_{COM} and decreases slightly as the difference between V_{DUT} and V_{COM} is reduced. Figure 8 shows typical AD1315 inhibit leakage current as a function of V_{DUT} and temperature.

THERMAL CONSIDERATIONS

The AD1315 is provided in a 0.550″ × 0.550″, 16-lead (bottom brazed) gull wing, surface mount package with a θ_{JC} of 10°C/W (typ). Thermal resistance (case-to-ambient) vs. air flow for the AD1315 in this package is shown in Figure 13. The data presented is for a ZIF socketed device. For PCB mounted devices (w/30 mils clearance) the thermal resistance should be ≈3 to 7% lower with air flows below 320 lfm[1]. Notice that the improvement in thermal resistance vs. air flow starts to flatten out just above 400 lfm[2].

NOTES
[1]lfm is air flow in linear feet/minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

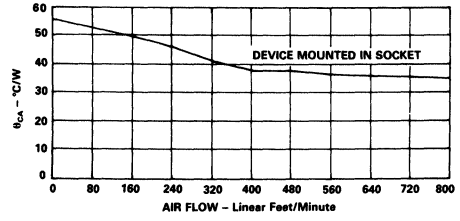


Figure 13. Case-to-Ambient Thermal Resistance vs. Air Flow

APPLICATIONS

The AD1315 has been optimized to function as an active load in an ATE test system. Figure 14 shows a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. The AD1315 active load, AD1321 or AD1324 pin driver, AD1317 high speed dual comparator and the AD664 quad 12-bit voltage DAC would comprise the pin electronic portion of the test system. Such a system could operate at 100 MHz with the AD1321 (200 MHz with the AD1324) in a data mode or 50 MHz (100 MHz) in the I/O mode.

The V_{COM} input sets the commutation voltage of the active load. With DUT output voltage above V_{COM}, the load will sink current (I_{OH}). With DUT output voltage below V_{COM}, the load will source current (I_{OL}). Like the I_{OH} and I_{OL} return lines, the V_{COM} must be able to sink or source 50 mA, therefore a standard op amp will not suffice. An op amp with an external complementary output stage or a high power op amp such as the AD842 will work well here. A typical application is shown in Figure 15.

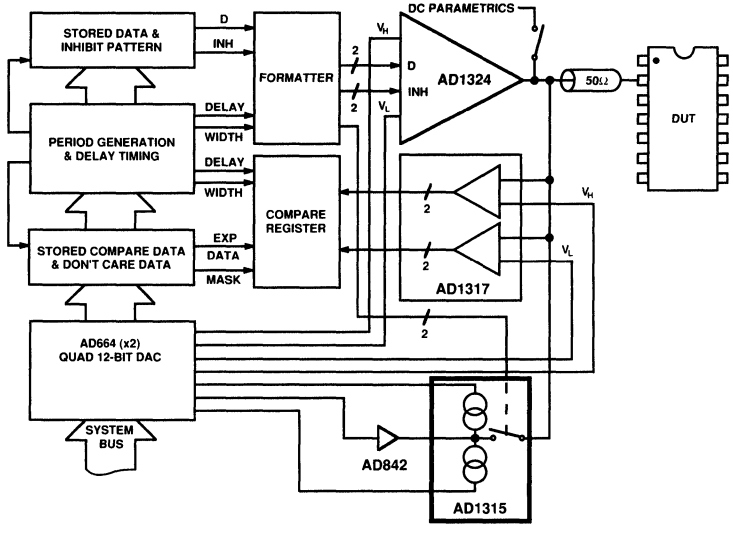


Figure 14. High Speed Digital Test System Block Diagram

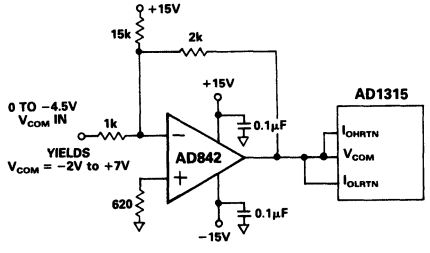


Figure 15. Suggested I_{OHRTN}, I_{OLRTN}, V_{COM} Hookup

LAYOUT CONSIDERATIONS

I_{OHRTN} and I_{OLRTN} may be connected to any potential between −2 V and +7 V. These return points must be able to source or sink 50 mA, since the I_{OH} and I_{OL} programmed currents are diverted here in the inhibit mode. The RTNs may be connected to a suitable GND. However, to keep transient ground currents to a minimum, they are typically tied to the V_{COM} programming voltage point.

EVALUATION BOARD

The AD1315 Evaluation Board allows the designer to easily evaluate the performance of the AD1315 and its suitability for the specific application. The AD1315EB includes a mounted AD1315KZ active load, an ECL input buffer for Inhibit and the oscilloscope probe jacks necessary to properly analyze the true performance of the AD1315KZ. An equipment list is provided in order to minimize variations due to test setups.

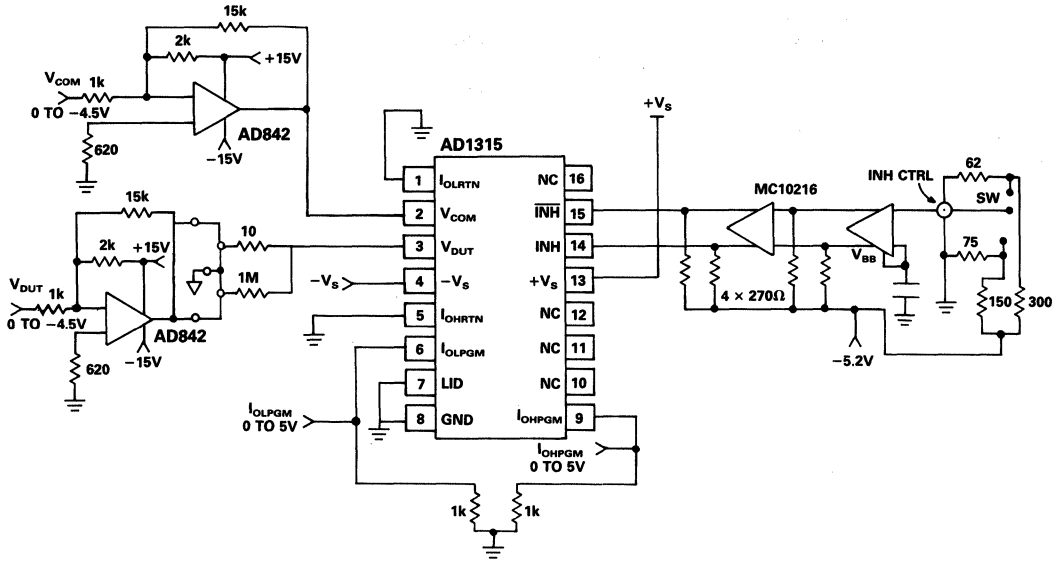


Figure 16. AD1315EB Evaluation Board Circuit

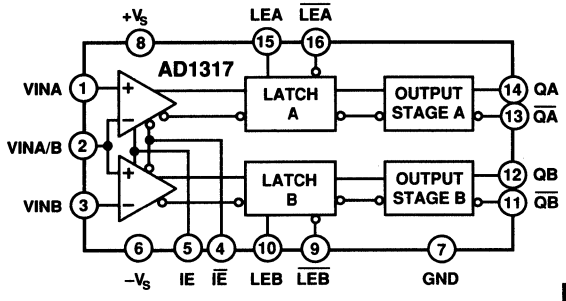
Ultrahigh Speed Window Comparator with Latch

AD1317

FEATURES
Full Window Comparator
2.0 pF max Input Capacitance
9 V max Differential Input Voltage
2.5 ns Propagation Delays
Low Dispersion
Low Input Bias Current
Independent Latch Function
Input Inhibit Mode
80 dB CMRR

APPLICATIONS
High Speed Pin Electronic Receiver
High Speed Triggers
Threshold Detectors
Peak Detectors

FUNCTIONAL BLOCK DIAGRAM



6

PRODUCT DESCRIPTION

The AD1317 is an ultrahigh speed window comparator with a latch. It uses a high speed monolithic process to provide high dc accuracy without sacrificing input voltage range. The AD1317 guarantees a 2.8 ns maximum propagation delay.

On-chip connection of the common input eliminates the contributions of a second bonding pad and package pin to the input capacitance, resulting in a maximum input capacitance of 2 pF.

The dispersion, or variation in propagation delay with input overdrive levels and slew rates, is typically 350 ps for 5 V signals and 200 ps for 1 V inputs.

The AD1317 employs a high precision differential input stage with a common-mode range of 9 V. Its complementary digital outputs are ECL compatible. The output stage is capable of driving a 50 Ω line terminated to −2 V. The AD1317 also provides a latch function, allowing operation in a sample-hold mode. The latch inputs can also be used to generate hysteresis.

The comparator input can be switched into a high impedance state through the inhibit mode feature, electrically removing the comparator from the circuit. The bias current in inhibit mode is typically 50 pA.

The AD1317 is available in a small 16-lead, hermetically sealed "gull-wing" surface mount package and operates over the commercial temperature range, 0 to +70°C.

AD1317—SPECIFICATIONS

(All specifications at +25°C, free air. Outputs terminated into 50 Ω to −2 V, with $+V_S$ = +10 V, $-V_S$ = −5.2 V unless otherwise specified.)

Parameter	Symbol	AD1317KZ Min	Typ	Max	Units	Comments
DC INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	−10		10	mV	CMV = 0 V
Offset Drift	dV_{OS}/dT		20		µV/°C	
VINA/B Bias Currents						−2 V to +7 V
Active	Ibca		10	33	µA	
Inhibit	Ibci		50		pA	
VINA, VINB Bias Currents						−2 V to +7 V
Active	Ibsa		5	16.5	µA	
Inhibit	Ibsi		50		pA	
VINA/B Resistance	Rinc		4		MΩ	
VINA, VINB Resistance	Rins		8		MΩ	
Capacitance VINA/B, VINA, VINB	C_{IN}		1.5	2.0	pF	
Voltage Range	V_{CM}	−2		7	Volts	See Note 5
Differential Voltage	V_{DIFF}			9	Volts	
Common-Mode Rejection Ratio	CMRR	70	80		dB	−2 V to +7 V
LATCH ENABLE INPUTS						
Input Voltage, Any Input		−2.0		5.0	Volts	
Differential Voltage		0.4		4	Volts	
Logic "1" Current	I_{IH}			10	µA	
Logic "0" Current	I_{IL}	−200			µA	
Capacitance				4	pF	
INPUT ENABLE CURRENTS						
Input Voltage, Any Input		−2.0		5.0	Volts	
Differential Voltage		0.4		4	Volts	
Logic "1" Current	I_{IH}			20	µA	
Logic "0" Current	I_{IL}	−200			µA	
Capacitance				4	pF	
DIGITAL OUTPUTS						
Logic "1" Voltage	V_{OH}	−0.98			Volts	
Logic "0" Voltage	V_{OL}			−1.50	Volts	
SWITCHING PERFORMANCE						See Figure 3
Propagation Delays						
Input to Output	t_{PDR}, t_{PDF}		1.8	2.8	ns	See Note 1
Latch Enable to Output	t_{LO}		2.0	2.5	ns	See Note 1
Active to Inhibit	t_{ID}		2.5		ns	See Note 2
Inhibit to Active	t_{IE}		15		ns	See Note 3
Propagation Delay T.C.			5		ps/°C	
Dispersion						See Note 4
5 V Signal						See Figure 1
All Edges			450	600	ps	
Rising Edge			350		ps	
Falling Edge			350		ps	
1 V Signal						See Figure 2
All Edges			250	400	ps	
Rising Edge			200		ps	
Falling Edge			200		ps	
LATCH TIMING						See Figure 3
Input Pulse Width	t_{PW}	2.5	1.0		ns	
Setup Time	t_S	1.5	0.4		ns	
Hold Time	t_H	0			ns	
POWER SUPPLIES						
$-V_S$ to $+V_S$ Range			15.2	15.6		See Note 5
Positive Supply	$+V_S$	8.0	10.0	11.0	Volts	
Negative Supply	$-V_S$	−7.2	−5.2	−4.2	Volts	
Positive Supply Current	I+		50	70	mA	
Negative Supply Current	I−	−100	−70		mA	
PSRR		65	75		dB	Measured at ±2.5% of $+V_S$ and $-V_S$

NOTES

[1]Propagation Delay is measured from the input threshold crossing at the 50% point of a 0 V to 5 V input to the output Q and $\overline{Q}$ crossing.

[2]Propagation Delay is measured from the input crossing of IE and $\overline{IE}$ to when the input bias currents drop to 10% of their nominal value.

[3]Propagation Delay is measured from the input crossing of IE and $\overline{IE}$ to when the input bias currents rise to 90% of their nominal value.

[4]Dispersion is measured with input slew rates of 0.5 V/ns and 2.5 V/ns for 5 V swings, 0.5 V/ns and 1 V/ns for 1 V swings..

[5]The comparator input voltage range is specified for −2 V to +7 V for typical power supply values of −5.2 V and +10.0 V but can be offset for different input ranges such as −1 V to +8 V with power supplies of −4.2 V and +11 V, as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $-V_S$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage
- $+V_S$ to GND . . . . . +12 V
- $-V_S$ to GND . . . . . −9 V
- Difference from $+V_S$ to $-V_S$ . . . . . +16 V

Inputs
- VINA/B, VINA, VINB . . . . . $+V_S$ −13.5 V, $-V_S$ +13.7 V
- LEA, $\overline{\text{LEA}}$, LEB, $\overline{\text{LEB}}$ . . . . . $+V_S$ −14 V, $-V_S$ +12 V
- IE, $\overline{\text{IE}}$ . . . . . $+V_S$ −14 V, $-V_S$ +10.3 V

Outputs[2]
- QA, $\overline{\text{QA}}$, QB, $\overline{\text{QB}}$ . . . . . GND −0.5 V, GND +3.5 V

Operating Temperature Range . . . . . 0°C to +70°C

Storage Temperature Range
- After Soldering . . . . . −65°C to +125°C

Lead Temperature Range (Soldering 20 sec)[3] . . . . . +300°C

NOTES

[1]Stresses above those limits under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Limits apply for shorted output.

[3]To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in an environment at 24°C ±5°C (75°F ±10°F) with relative humidity not to exceed 65%.

WINDOW COMPARATOR PIN ASSIGNMENT

Pin No.	Description	
1	VINA	Noninverting Comparator A Input
2	VINA/B	Window Comparator Common Input
3	VINB	Inverting Comparator B Input
4	$\overline{\text{IE}}$	$\overline{\text{Input Enable}}$
5	IE	Input Enable
6	$-V_S$	Negative Supply, −5.2V
7	GND	Ground
8	$+V_S$	Positive Supply, +10V
9	$\overline{\text{LEB}}$	$\overline{\text{Latch Enable B}}$
10	LEB	Latch Enable B
11	$\overline{\text{QB}}$	$\overline{\text{Comparator B Output}}$
12	QB	Comparator B Output
13	$\overline{\text{QA}}$	$\overline{\text{Comparator A Output}}$
14	QA	Comparator A Output
15	LEA	Latch Enable A
16	$\overline{\text{LEA}}$	$\overline{\text{Latch Enable A}}$

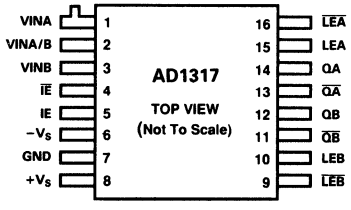
ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD1317KZ	0 to +70°C	16-Lead Gull Wing	Z-16A

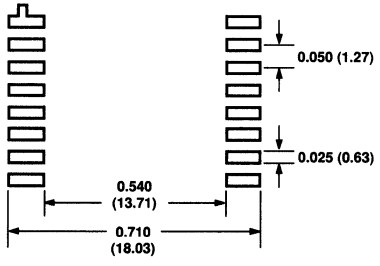
*For outline information see Package Information section.

CONNECTION DIAGRAMS

Dimensions shown in inches and (mm).



SUGGESTED LANDING PADS LOCATION



AD1317—Definition of Terms

V_{OS} INPUT OFFSET VOLTAGE – The voltage which must be applied between either VINA and VINA/B or VINB and VINA/B to obtain zero voltage between outputs QA and $\overline{QA}$, or QB and $\overline{QB}$, respectively.

dV_{OS}/dT OFFSET DRIFT – The ratio of the change in input offset voltages, over the operating temperature range, to the change in temperature.

Ibca INPUT BIAS CURRENT (VINA/B, ACTIVE) – The bias current of the window comparator's common input with inputs enabled.

Ibci INPUT BIAS CURRENT (VINA/B, INHIBIT) – The bias current of the window comparator's common input with inputs inhibited.

Ibsa INPUT BIAS CURRENT (VINA or VINB, ACTIVE) – The bias current of either single input with inputs active.

Ibsi INPUT BIAS CURRENT (VINA or VINB, INHIBIT) – The bias current of either single input with inputs inhibited.

Rinc INPUT RESISTANCE (VINA/B) – The input resistance looking into the window comparator's common input.

Rins INPUT RESISTANCE (VINA or VINB) – The input resistance looking into either single input.

C_{IN} INPUT CAPACITANCE (VINA/B) – The capacitance looking into the window comparator's common input.

V_{CM} INPUT COMMON-MODE VOLTAGE RANGE – The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

V_{DIFF} INPUT DIFFERENTIAL VOLTAGE RANGE – The maximum difference between any input terminal voltages.

CMRR COMMON-MODE REJECTION RATIO – The ratio of common-mode input voltage range to the peak-to-peak change in input offset voltage over this range.

I_{IH} LOGIC "1" INPUT CURRENT – The logic high current flowing into (+) or out of (−) a logic input.

I_{IL} LOGIC "0" INPUT CURRENT – The logic low current flowing into (+) or out of (−) a logic input.

V_{OH} LOGIC "1" OUTPUT VOLTAGE – The logic high output voltage with a specified load.

V_{OL} LOGIC "0" OUTPUT VOLTAGE – The logic low output voltage with a specified load.

I_{OH} LOGIC "1" OUTPUT CURRENT – The logic high output source current.

I_{OL} LOGIC "0" OUTPUT CURRENT – The logic low output source current.

I+ POSITIVE SUPPLY CURRENT – The current required from the $+V_S$ supply.

I− NEGATIVE SUPPLY CURRENT – The current required from the $-V_S$ supply.

PSRR POWER SUPPLY REJECTION RATIO – The ratio of power supply voltage change to the peak-to-peak change in input offset voltage.

AD1317 SWITCHING TERMS (See Figure 3)

t_{PDR} INPUT TO OUTPUT RISING EDGE DELAY – The propagation delay measured from the time VINA/B crosses either VINA or VINB, in a low to high transition, to the time QA and $\overline{QA}$ or QB and $\overline{QB}$ cross, respectively.

t_{PDF} INPUT TO OUTPUT FALLING EDGE DELAY – The propagation delay measured from the time VINA/B crosses either VINA or VINB, in a high to low transition, to the time QA and $\overline{QA}$ or QB and $\overline{QB}$ cross, respectively.

t_S MINIMUM LATCH SET-UP TIME – The minimum time before LE goes high with respect to $\overline{LE}$ that an input signal change must be present in order to be acquired and held at the outputs.

t_H MINIMUM LATCH HOLD TIME – The minimum time after LE goes high with respect to $\overline{LE}$ that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{PW} MINIMUM LATCH ENABLE PULSE WIDTH – The minimum time that LE must be held high with respect to $\overline{LE}$ in order to acquire and hold an input change.

t_{LO} LATCH ENABLE TO OUTPUT DELAY – The time between when LE goes high with respect to $\overline{LE}$ that QA and $\overline{QA}$ or QB and $\overline{QB}$ cross.

t_{ID} INPUT STAGE DISABLE TIME – The time between when $\overline{IE}$ goes high with respect to IE that the input bias currents drop to 10% of their nominal value.

t_{IE} INPUT STAGE ENABLE TIME – The time between when IE goes high with respect to $\overline{IE}$ that the input bias currents rise to 90% of their nominal values.

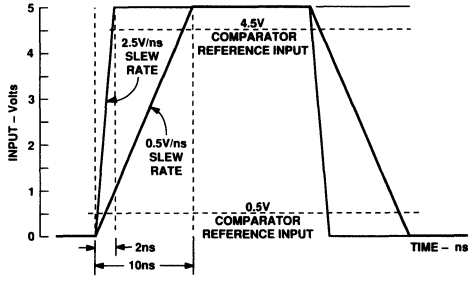


Figure 1. Dispersion Test Input Conditions – 5 V Signal

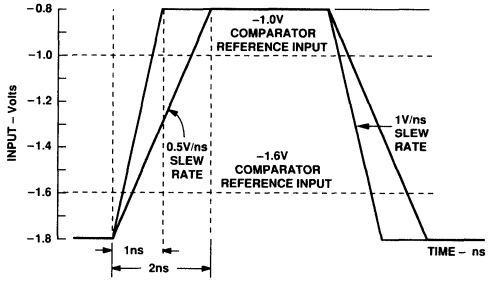


Figure 2. Dispersion Test Input Conditions – 1 V Signal

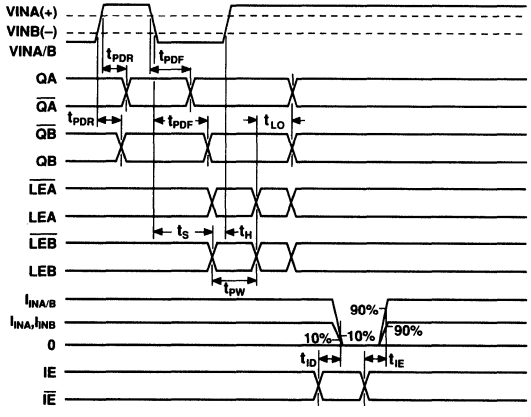


Figure 3. Timing Diagram

AD1317—Typical Performance Characteristics

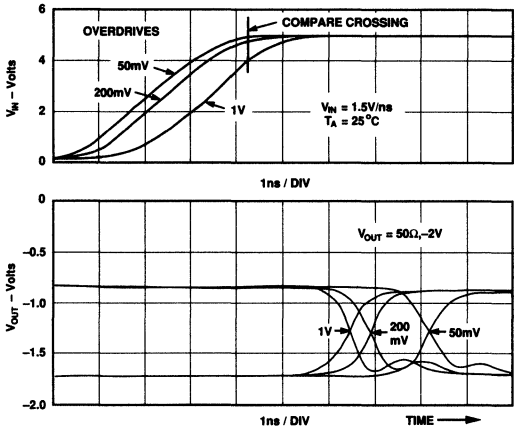


Figure 4. Response to Overdrive Variation – Rising Edge

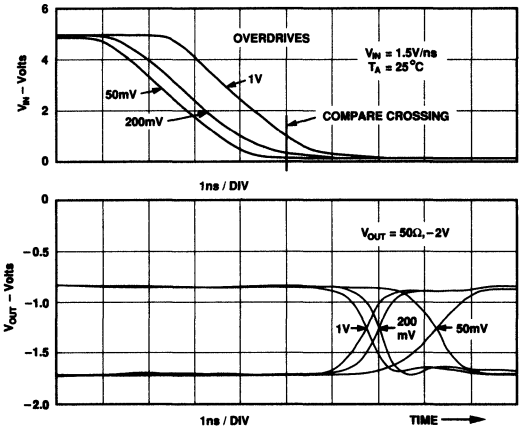


Figure 5. Response to Overdrive Variation – Falling Edge

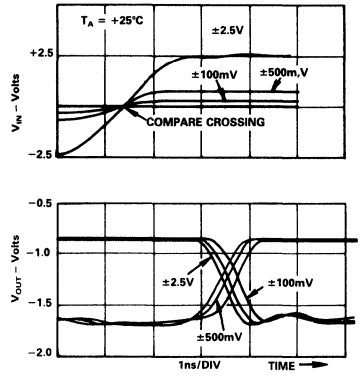


Figure 6. Response to Various Signal Levels – Rising Edge

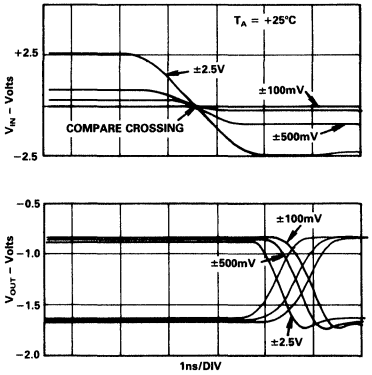


Figure 7. Response to Various Signal Levels – Falling Edge

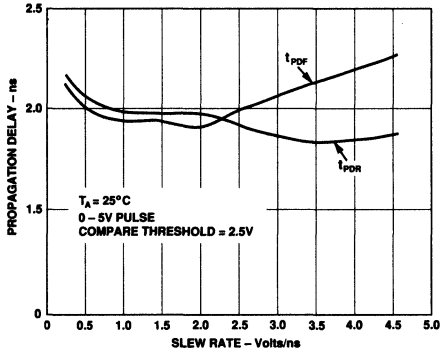


Figure 8. Propagation Delay vs. Slew Rate

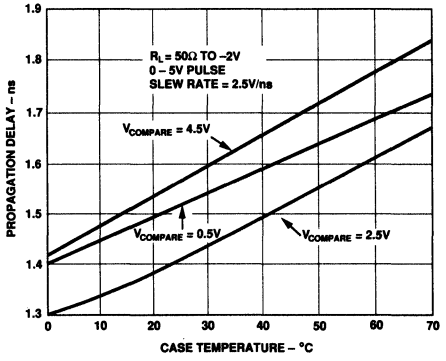


Figure 9. Propagation Delay vs. Temperature – Rising Edge

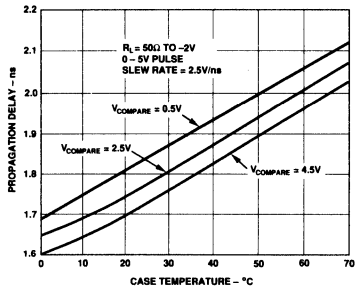


Figure 10. Propagation Delay vs. Temperature – Falling Edge

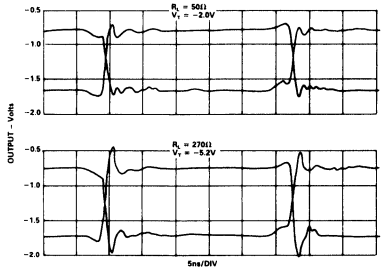


Figure 11. Output Waveform vs. Load

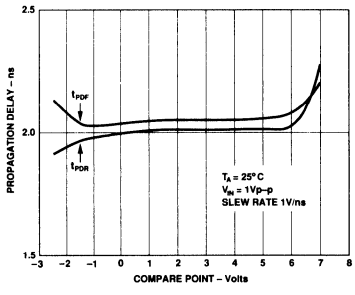


Figure 12. Propagation Delay vs. Common-Mode Voltage

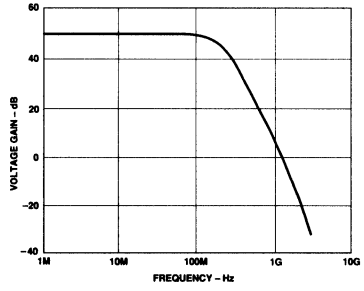


Figure 13. Voltage Gain vs. Frequency

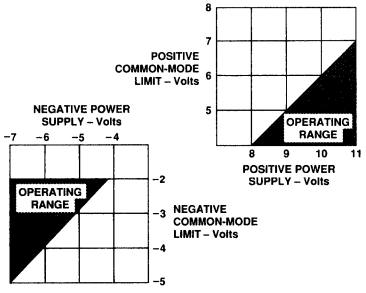


Figure 14. Common-Mode Range vs. Power Supply

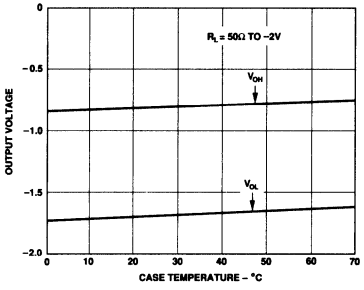


Figure 15. Output Levels vs. Temperature

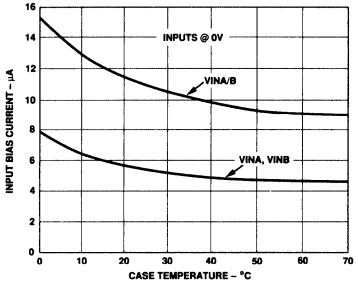


Figure 16. Input Bias Current vs. Temperature

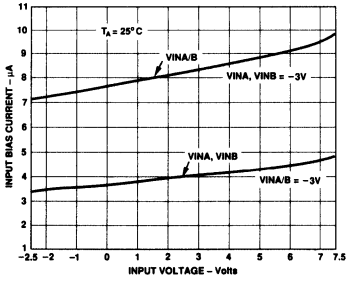


Figure 17. Input Bias Current vs. Input Voltage

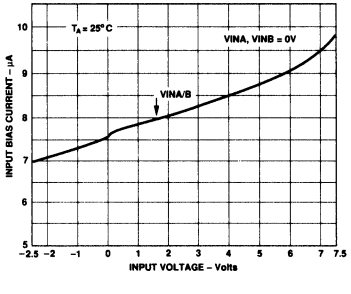


Figure 18. Input Bias Current vs. Input Voltage

AD1317—Typical Performance Characteristics

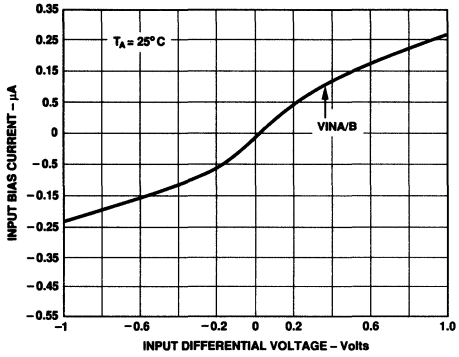


Figure 19. Change in Bias Current vs. Input Differential Voltage (VINA/B – VINA, VINB)

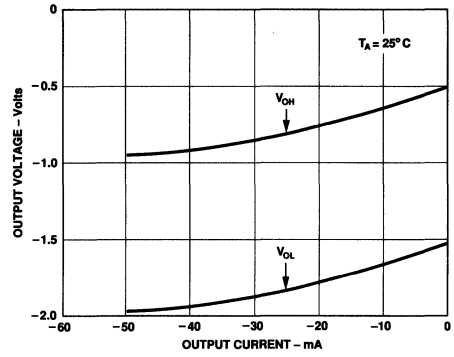


Figure 20. Output Voltage vs. Source Current

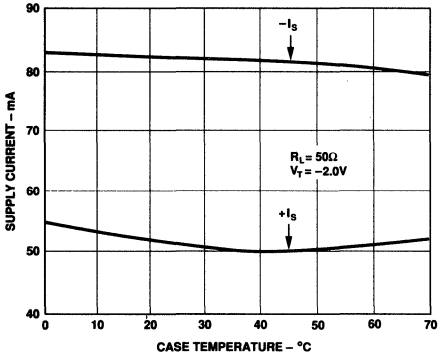


Figure 21. Power Supply Currents vs. Temperature

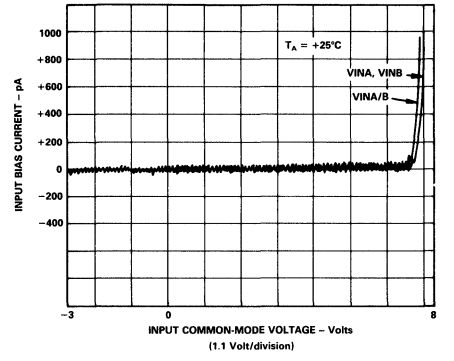


Figure 22. Inhibit Input Bias Current vs. Common-Mode Voltage

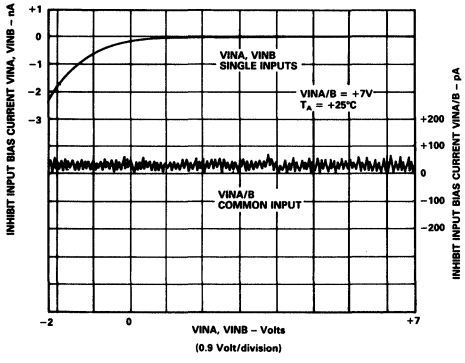


Figure 23. Inhibit Input Bias Current vs. Input Voltage (VINA/B = 7 V)

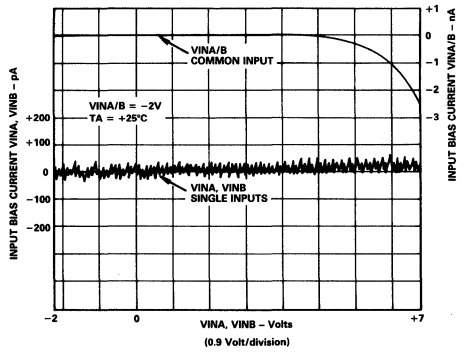


Figure 24. Inhibit Input Bias Current vs. Input Voltage (VINA/B = −2 V)

FUNCTIONAL DESCRIPTION

The AD1317 is an ultrahigh speed window comparator designed for use in general purpose instrumentation and automatic test equipment. The internal connections for windowing operation keep the capacitance at the critical common input (VINA/B) well below what could normally be obtained using separate input pins.

Another key feature is that the front end circuitry may be disabled, decreasing input bias currents to 50 pA (typical). This enables sensitive dc current testing without having to physically disconnect the AD1317's input from the circuit. The comparator's outputs would normally be latched to maintain absolute logic levels prior to inhibiting the input.

High speed comparators using bipolar process technology usually have input bias currents in the 1 μA to 20 μA range, and the AD1317 is no exception in this regard. This occurs because the input devices usually have low current gain but must be operated at high currents to obtain the widest possible bandwidth. Careful design minimizes variations in the AD1317's bias current with respect to both differential and common-mode input variations. This translates directly to a high equivalent input resistance, the minimum of which occurs with zero differential input. The typical input resistance of the AD1317's common input under this condition is on the order of 4 megohms.

Many ATE applications have required input dividers/buffers to reduce standard logic voltages to levels which can be processed by "687" type comparators. These dividers have also reduced the slew rates at which the comparators must properly function. The AD1317's 9 volt differential and common-mode input ranges and 2.5 V/ns slew rate capability make these buffer circuits unnecessary in most applications.

Separate, complementary latch inputs are provided for each comparator. These may be driven by differential or single-ended sources ranging from ECL to HCMOS logic. When using the comparator's transparent mode, the latch inputs may be tied anywhere within their common-mode range with a maximum differential of 4 V. Symmetrical hysteresis may also be generated by applying a small differential voltage to the latch inputs (see HYSTERESIS).

The AD1317's outputs are standard emitter followers with ECL-compatible voltage swings. The recommended output termination is 50 ohms to −2 V. Larger value termination resistors connected to $-V_S$ may be used, but will reduce edge fidelity. Typical output rise and fall times (20%–80%) are 1 ns with a 50 ohm, 10 pF load. The maximum output source current is 40 mA.

THERMAL CONSIDERATIONS

The AD1317 is provided in a 0.450″ × 0.450″, 16-lead (bottom brazed) gull wing, surface mount package with a typical θ_{JC} (junction-to-case thermal resistance) of 17.5°C/W. Thermal resistance θ_{CA} (case to ambient) vs. air flow for the AD1317 in this package is shown in Figure 25. The improvement in thermal resistance vs. air flow begins to flatten out just above 400 lfm[1, 2]

NOTES
[1]lfm is airflow in linear feet/minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

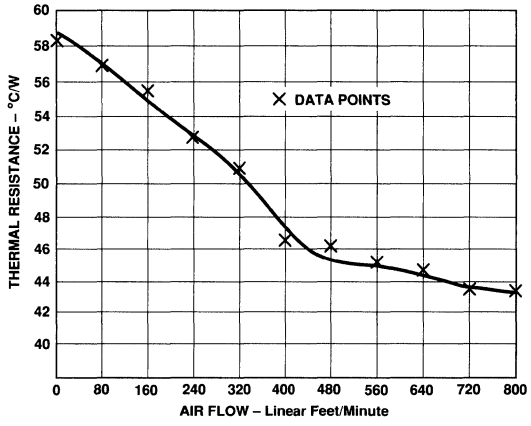


Figure 25. Case-to-Ambient Thermal Resistance vs. Air Flow

6

DISPERSION

Propagation delay dispersion is the change in device propagation delay which results from changes in the input signal conditions. Dispersion is an indicator of how well the comparator's front-end design balances the conflicting requirements of high gain and wide bandwidth. High gain is needed to ensure that small overdrives will produce valid logic outputs without an increase in propagation delay, while wide bandwidth enables the comparator to handle fast input slew rates. The input signal criteria used to determine the AD1317's dispersion performance are amplitude, overdrive and slew rate for both standard CMOS and ECL signal levels.

HYSTERESIS

The customary technique for introducing hysteresis into a comparator uses positive feedback as shown in Figure 27. The major problems with this approach are that the amount of hysteresis varies with the output logic levels and that the hysteresis is not symmetrical around zero.

The AD1317 does not use this technique. Instead, hysteresis is generated by introducing a differential voltage between LE and $\overline{LE}$ as shown in Figure 28. Hysteresis generated in this manner is independent of output swing and is symmetrical around zero. The variation of hysteresis with input voltage is shown in Figure 29; the useful hysteresis range is about 20 mV.

LAYOUT CONSIDERATIONS

Like any high speed device, the AD1317 requires careful layout and bypassing to obtain optimum performance. Oscillations are generally caused by coupling from an output to the high impedance inputs. All drive impedances should be as low as possible, and lead lengths should be minimized. A ground plane should be used to provide low impedance return paths. Care should be taken in selecting sockets for incoming or other testing to minimize lead inductance, and sockets are not recommended for production use.

Output wire lengths should be kept below one inch. Longer connections require the use of transmission line techniques to prevent ringing and reflections. Lines should be terminated with their characteristic impedance to −2 V. Thevenin-equivalent termination to $-V_S$ is also possible.

High quality RF capacitors should be used for power supply bypassing. These should be located as closely as possible to the AD1317's power pins and connections to the ground plane should have the minimum possible length. Both $+V_S$ and $-V_S$ must be bypassed with 470 pF capacitors located within 0.25 inches of the device's supply pins. In addition, each supply should be bypassed with 0.1 μF ceramic and 10 μF tantalum capacitors. Low impedance power distribution techniques will make the locations of these components less critical. Adding 470 pF capacitors at the VINA and VINB inputs, as close as possible to the package, will improve circuit performance and noise immunity in dc-compare applications.

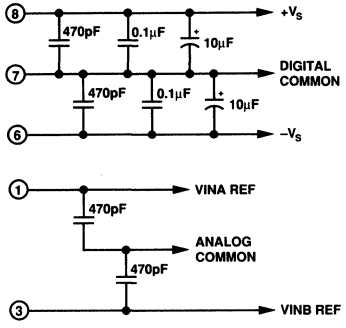


Figure 26. AD1317 Basic Circuit Decoupling

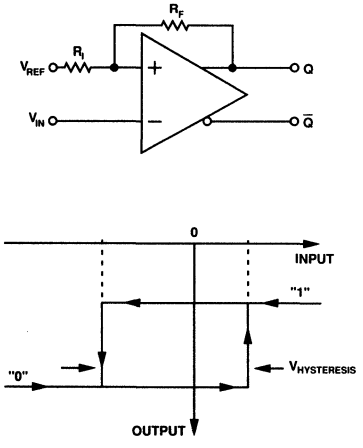


Figure 27. Typical Comparator Hysteresis

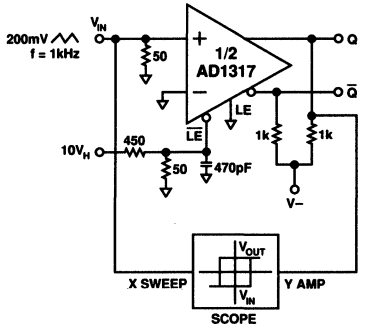


Figure 28. AD1317 Comparator Hysteresis Test Setup

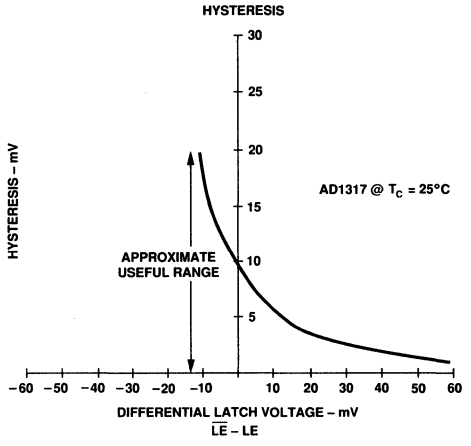


Figure 29. AD1317 Typical Hysteresis Curve

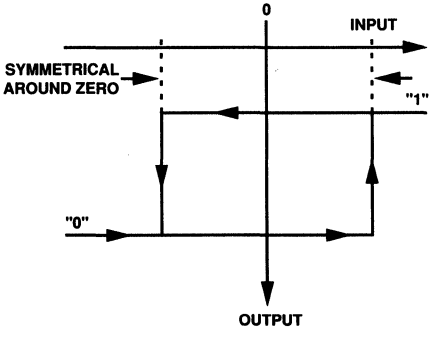


Figure 30. AD1317 Hysteresis

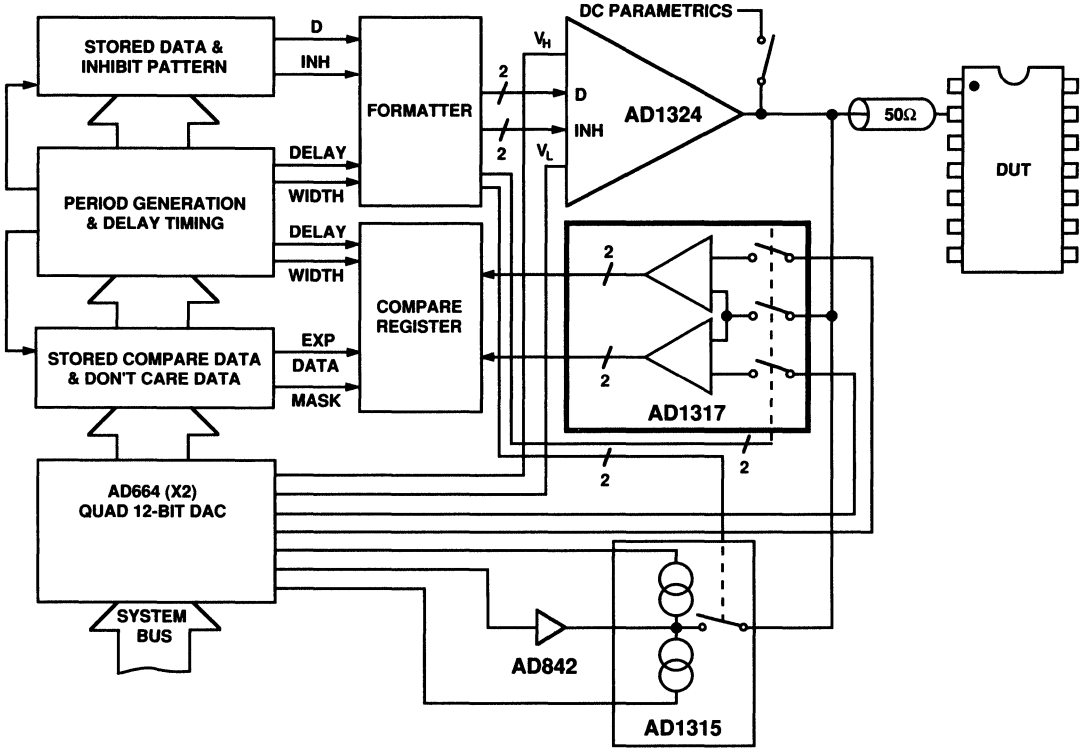


Figure 31. High Speed Digital Test System Block Diagram

High Voltage Pin Driver with Inhibit Mode

AD1320

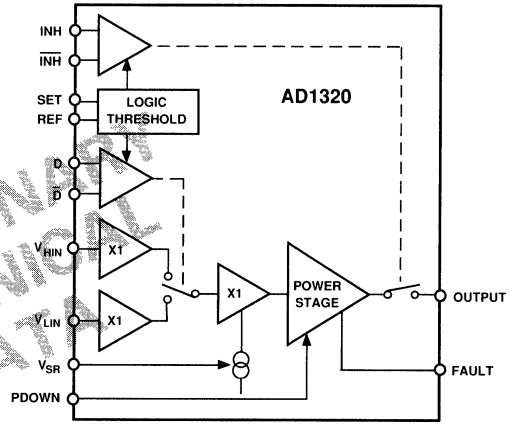
FEATURES

Output Swing Adjustable to 22 V (24 V with ±16 V Supplies)
100 mA Output Current Drive
Slew Rate to 500 V/μs
Power Down "Stand-By" Mode
Driver Inhibit Function
Over Current Fault Indicator
High Speed Differential Inputs

APPLICATIONS

Automatic Test Equipment
System Testers
Functional Testers
Instrumentation & Characterization Equipment
General Purpose Driver

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1320 is a complete high voltage pin driver designed for use in PC board, mixed-signal and large system testers including portable and ground military and commercial testers. Using a high speed, high breakdown, monolithic process, this product offers outstanding electrical performance, optimum packing density, and long term reliability in its 18-pin hermetically sealed DIP package.

Featuring unity gain, output levels programmable from −11 V to +11 V, and an output swing capability of 400 mV to 22 V, the AD1320 is designed to drive ECL, TTL, and CMOS logic families, RS-232 lines, and mixed-signal inputs. Its high output current capability allows real-time stimulation in the most difficult tester environments with a minimum of external components. The pin driver can be switched into a high impedance state using its inhibit mode for testing I/O devices. The AD1320's typical inhibit leakage current is 500 nA, and the output charge transfer when going into inhibit mode is typically less than 50 pC.

Transitions between output High and Low and to and from inhibit are controlled via the AD1320's high speed differential data and inhibit inputs. This allows for direct interfaces with the precision timing of differential ECL or the simplicity of single-ended TTL or CMOS logic. The analog High and Low reference inputs are equally easy to interface. Requiring typically 1 μA of bias current, these inputs can be directly coupled to the output of a DAC, either singly or in parallel with the inputs of a number of other drivers.

AD1320—SPECIFICATIONS

(All specifications at T_A = +25°C in still air, V_{CC} = +15 V, V_{EE} = −15 V, V_{HOUT} = +10 V, V_{LOUT} = −10 V, V_{SR} = +5.0 V, unless otherwise noted. See Figure 1 for output load and stability circuitry.)

Parameter	Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Voltage Range, Any Single Input	−2.0		+7.0	V	
Differential Input Amplitude	0.4	ECL	5.0	V	
Bias Current	−35		35	μA	
REFERENCE INPUTS					
V_{HIN}, V_{LIN} Bias Currents		1		μA	Note 1
CONTROL INPUTS					
V_{SR} (Slew Rate) Input Current	4		15	μA	0.5 V < V_{SR} <5 V
Power-Down Input					
Logic High (Powered Down)	2.0		5.5	V	
Logic Low (Active)	0.0		0.8	V	
Input Resistance		16		kΩ	Note 2
LOGIC REFERENCE PINS					
Logic Reference Voltage Out					
Logic Reference Set Open		2.5		V	
Logic Reference Set Grounded		1.4		V	
Output Impedance		2.5		kΩ	
Logic Reference Set Current, Grounded		430		μA	
OUTPUT CHARACTERISTICS					
Output Voltage Range	V_{EE} + 4		V_{CC} − 4	V	
Output Voltage Amplitude	0.4		24	V	Note 3
Offset	−30	±10	+30	mV	Note 4
Gain	0.999	1.000	1.001	V/V	Note 5
Linearity Error	−50		+50	mV	Note 6
Output Voltage Temperature Drift		±0.5		mV/°C	
Current Drive					
Static	−100		100	mA	
Positive Current Limit	100		175	mA	To GND
Negative Current Limit	−175		−100	mA	To GND
Leakage Current, Inhibit Mode	−1		1	μA	Note 7
Output Resistance, I_{LOAD} = ±5 mA	2.7	TBD	5.5	Ω	Note 8
Output Resistance, I_{LOAD} = ±100 mA	1.5	TBD	8.5	Ω	Note 8
FAULT INDICATOR					
Current Fault (Active Low)					Note 9
Positive Output Current Setpoint	90	100	110	mA	
Negative Output Current Setpoint	−110	−100	−90	mA	
DYNAMIC PERFORMANCE					Note 10
Driver Mode					
Delay Time	4.0	5.0	6.0	ns	Note 11
Delay Time Matching, Edge-to-Edge		1.5	2.0	ns	
Rise & Fall Time					Note 12
5 V Swing		6	8	ns	
20 V Swing		35	40	ns	
Slew Rate, V_{SR} = +5.0 V	TBD	500	TBD	V/μs	Note 13
Slew Rate, V_{SR} = +0.5 V	TBD	50	TBD	V/μs	Note 13
Overshoot	−500		500	mV	
Preshoot	−200		+200	mV	
Settling Time		TBD		ns	Note 14

Parameter	Min	Typ	Max	Units	Comments
DYNAMIC PERFORMANCE					
Inhibit Mode					
Delay Time					Note 15
Output High or Low to Inhibit	3.0	4.0	5.0	ns	
Inhibit to Output High or Low	6.5	7.4	8.5	ns	
Overshoot & Preshoot	−500		500	mV	
Output Capacitance			20	pF	
Output Charge Entering Inhibit Mode			50	pC	C_L = 100 pF
POWER SUPPLIES					
Current					
Positive Supply, Active		40	45	mA	
Positive Supply, Powered Down			5	mA	
Negative Supply, Active	−45	−40		mA	
Negative Supply, Powered Down	−5			mA	
+PSRR		2	5	mV/V	V_{CC} ±2.5%
−PSRR		2	5	mV/V	V_{EE} ±2.5%

NOTES

[1]Specification applies for $V_{EE} + 4 < V_{HIN}, V_{LIN} < V_{CC} - 4$.

[2]Resistance to ground.

[3]24 V output swing requires ±16 V supplies; maximum output amplitude using ±15 V supplies is 22 V.

[4]Measured for output "high" and output "low" with $V_{HIN}, V_{LIN} = 0$ V.

[5]Gain is defined as 20 V/($V_{IN1} - V_{IN2}$) where V_{IN1} and V_{IN2} are the input voltages required to force V_{OUT} to ±10.000 V. Gain is measured for both output "high" and output "low" by applying the inputs to V_{HIN} and V_{LIN}, respectively. V_{LIN} is held at −11 V when measuring output "high" gain; V_{HIN} is held at +11 V when measuring output "low" gain.

[6]Linearity is measured for both the output "high" and output "low" states using the endpoint method with endpoints determined during the gain measurement (see Note 5).

[7]Specification applies for $V_{EE} + 4 < V_{OUT} < V_{CC} - 4$.

[8]Tested with V_{HOUT} = +5 V and V_{LOUT} = −5 V.

[9]The Current Fault Indicator pin (Pin 4, CFI) should be pulled up to +5 V with a 2kΩ resistor. Active Low is defined as $V_{CFI} < 2.5$ V.

[10]V_{HOUT} = +5.0 V, V_{LOUT} = 0.0 V, V_{SR} = +5.0 V for all dynamic specifications, except V_{HOUT} = +10 V, V_{LOUT} = −10 V for 20 V output swing tests.

[11]Drive mode delay times are measured from the crossing of differential ECL data inputs to a 200 mV transition (excluding preshoot) at the driver output. See Figure 2.

[12]Measured between the 10% and 90% points of the output waveform.

[13]Slew rates are calculated based on the measured 20% to 80% rise time and fall time for a 20 V output swing.

[14]Settling time is measured between the time at which 90% of a 5 V output transition has been completed and the time at which the output is within ±200 mV of its final value. See Figure 3.

[15]Inhibit Mode delay times are measured from the crossing of differential ECL inputs to a 200 mV transition at the output. The output load is 50 Ω in parallel with less than 10 pF to ground, V_{HOUT} = +500 mV, V_{LOUT} = −500 mV. See Figure 2.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Power Supply Voltage
- V_{CC} to Ground . . . . . +30 V
- V_{EE} to Ground . . . . . −30 V
- V_{CC} to V_{EE} . . . . . +36 V

Data and Inhibit Inputs
- Any Input . . . . . −TBD V to +TBD V
- Maximum Differential Input . . . . . 5.5 V

Maximum Current Into Any Input . . . . . 20 mA
Power Dissipation . . . . . 2.8 W at 25°C with 400 lfm Airflow
. . . . . and No Heat Sink

Output Short Circuit Duration
- To Ground . . . . . Indefinite
- To V_{CC} − 3 V . . . . . Indefinite*
- To V_{EE} + 3 V . . . . . Indefinite*

NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

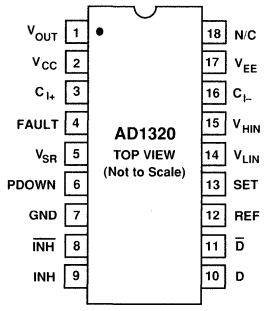
*The AD1320's output is not protected against short circuits outside this range. Shorting the output to potentials greater than V_{CC} − 3 V or less than V_{EE} + 3 V may destroy the device.

ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD1320KQ	0°C to +70°C	18-Lead Cerdip	Q-18

*For outline information see Package Information section.

PIN CONFIGURATION



PIN DESIGNATIONS

Pin No.	Symbol	Function
1	V_{OUT}	Driver Output
2	V_{CC}	Positive Supply
3	C_{I+}	Positive Overcurrent Bypass
4	Fault	Output Overcurrent Flag
5	V_{SR}	Slew Rate Control Voltage
6	PDOWN	Powerdown Control Input
7	GND	Device Ground
8	$\overline{INH}$	Inhibit Input Complement
9	INH	Inhibit Input
10	D	Driver Input
11	$\overline{D}$	Driver Input Complement
12	REF	Logic Reference Out
13	SET	Logic Reference Level Set
14	V_{LIN}	Output Voltage Low Level Set
15	V_{HIN}	Output Voltage High Level Set
16	C_{I-}	Negative Overcurrent Bypass
17	V_{EE}	Negative Supply
18	N/C	No Connect

DEFINITION OF TERMS

OFFSET

The offset error for logic high is determined by forcing the driver's output to logic high with zero volts applied to V_{HIN}. The driver output voltage then represents the offset "high" error. The same approach is used to determine the offset "low" error.

GAIN

Logic high gain error is measured by driving the AD1320's output to logic high, holding V_{LIN} at −11 V, and measuring the change in V_{HIN} required to change the output voltage by 20.000 V (from −10.000 V to +10.000 V). Logic low gain error is measured holding V_{HIN} at +11 V and varying V_{LIN} to change the output from −10.000 V to +10.000 V. Gain is specified with no output load and will vary as a function of loading because of the AD1320's nonzero output impedance.

LINEARITY

The maximum deviation of the driver's transfer function from a reference line with endpoints of −10.000 V and +10.000 V. Logic high linearity is measured by holding V_{LIN} at −11 V and varying V_{HIN} between the voltages needed to drive the AD1320's output to ±10.000 V. Logic low linearity is measured in similar fashion, holding V_{HIN} at +11 V and changing V_{LIN}. Linearity is specified and tested with no dc load.

DELAY TIME

The time required for the input signal(s) to propagate through the driver and be converted to the desired output levels. The precise measurement techniques are defined in the notes and are shown in Figure 2.

EDGE-TO-EDGE MATCHING

Edge-to-edge matching is the difference, in time, between the delay times of the rising and falling edges.

SLEW RATE

The average rate of change of the output waveform between two specified voltages. Maximum slew rate is achieved during large-signal output transitions.

OVERSHOOT AND PRESHOOT

The amount by which transients on the driver's output exceed the desired beginning and ending set voltages for a given transition. Refer to Figure 3.

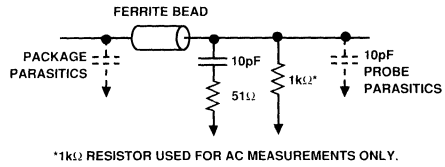


Figure 1. Output Stability Network and Load

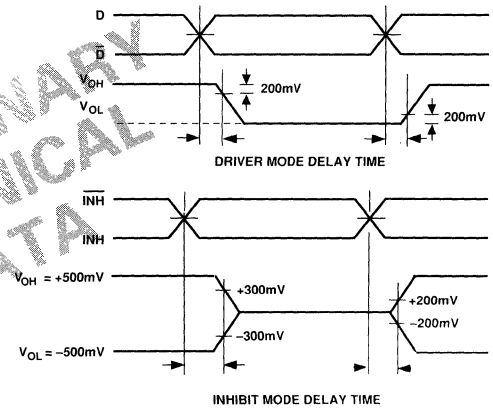


Figure 2. Timing Diagram for Drive and Inhibit Propagation Delays

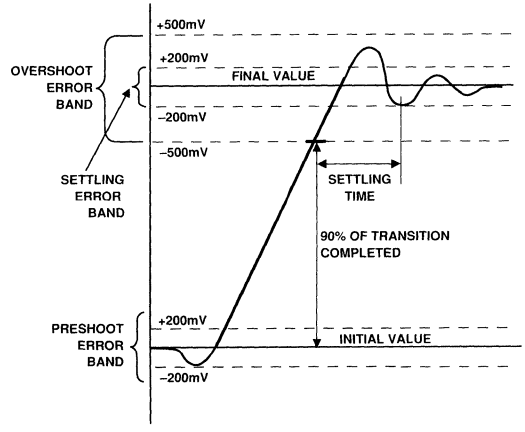


Figure 3. Definition of Waveform Aberrations and Settling Time

6

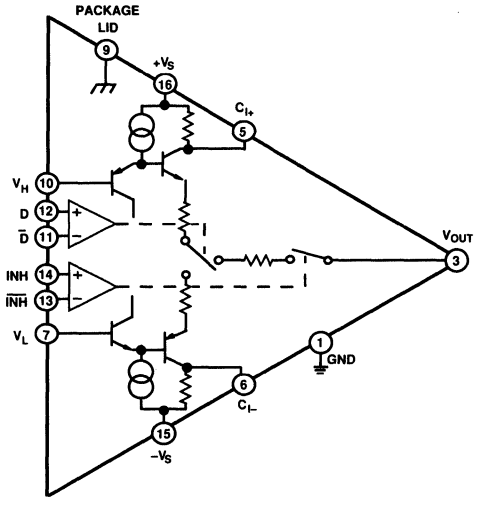
High Speed Pin Driver with Inhibit Mode

AD1321

FEATURES
100 MHz Driver Operation
Driver Inhibit Function
250 ps Edge Matching
Guaranteed Industry Specifications
50 Ω Output Impedance
1 V/ns Slew Rate
Variable Output Voltages for ECL, TTL and CMOS
High Speed Differential Inputs for Maximum Flexibility
Hermetically Sealed Small Gull Wing Package

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems
Instrumentation & Characterization Equipment

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1321 is a complete high speed pin driver designed for use in digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities and long term reliability in an ultrasmall 16-lead, hermetically sealed gull wing package.

Featuring unity gain programmable output levels of −2 V to +7 V with output swing capability of less than 100 mV to 9 V, the AD1321 is designed to stimulate ECL, TTL and CMOS logic families. The 100 MHz (5.0 ns pulsewidth) data rate capacity, 1 V/ns slew rate, and matched output impedance allows for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (inhibit mode) electrically removing the driver from the path through the inhibit mode feature. The pin driver leakage current in inhibit is typically 50 nA, and output charge transfer entering inhibit is typically less than 15 pC.

The AD1321 transition from HI/LO or to inhibit is controlled through the data and inhibit inputs. The input circuitry is implemented utilizing high speed differential inputs with a common mode range of 3 volts. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog logic HI/LO inputs are equally easy to interface. Typically requiring 350 μA of bias current, the AD1321 can be directly coupled to the output of a digital-to-analog converter.

The 150 MHz analog bandwidth of the logic HI/LO inputs allows for four quadrant multiplying providing maximum flexibility as a standard pin driver and a waveform generator all in one package.

The AD1321 is available in a 16-lead, hermetically sealed gull wing package and is specified to operate over the ambient commercial temperature range from 0 to +70°C.

AD1321—SPECIFICATIONS (All measurements made in free air at +25°C. Output load 10 kΩ/6 pF with $+V_S$ = +10 V, $-V_S$ = −5.2 V unless otherwise noted)

Parameter	AD1321KZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Input Voltage, Any One Input	−2.0		+7.0	Volts	
Differential Input Range	0.4	ECL	3.0	Volts	
Bias Current		175	300	μA	
REFERENCE INPUTS					See Note 1
V_{HIGH} Range (V_H)	−2.5		+7.5	Volts	
V_{LOW} Range (V_L)	−2.5		+7.5	Volts	
V_{HIGH} Bias Currents (V_H)		0.5	1.2	mA	
V_{LOW} Bias Currents (V_L)		0.3	0.5	mA	
Input Bandwidth		150		MHz	See Figure 9
OUTPUT CHARACTERISTICS					See Notes 1, 2
Logic High Range	−2.0		+7.0	Volts	
Logic Low Range	−2.0		+7.0	Volts	
Amplitude [V_H−V_L]	0.1		+9.0	Volts	
Accuracy					See Figure 1
Initial Offset	−50		+50	mV	
Gain Error	−4.5	−2.5	−0.5	% of Set Level	See Note 3
Linearity Error					
0 V to +5.5 V	−0.5		+0.5	% of Set Level	
−2 V to +7 V	−1.0		+1.0	% of Set Level	
Output Voltage TC		0.5		mV/°C	See Figures 7 & 8
Current Drive					
Static	30			mA	
Dynamic	100			mA	See Note 4
Current Limit			85	mA	
Output Impedance	48.5	50.0	51.5	ohms	See Note 5
DYNAMIC PERFORMANCE					
Driver Mode					See Note 6
Delay Time	0.8	1.2	1.6	ns	See Figure 2
Prop Delay TC		2.0		ps/°C	See Figure 4
Delay Time Matching					
Edge-to-Edge	−250	±80	+250	ps	See Figure 5
Rise & Fall Times					See Figure 10
1 V Swing		0.9	1.2	ns	Measurement 20%–80%
3 V Swing		2.7	3.0	ns	Measurement 10%–90%
5 V Swing		4.0	4.4	ns	Measurement 10%–90%
Large Signal Slew	0.8	1.1		V/ns	Measurement 20%–80% of 9 V Swing
Toggle Rate	100			MHz	ECL Output
Minimum PW, V_{OUT} = 2 V		5.0		ns	See Figure 12
Overshoot & Preshoot	−(3% V_O)−50		+(3% V_O)+50	mV	See Figure 3, Note 7
Settling Time					See Figure 3, Note 7
to ±1% V_O			15	ns	
Delay Time vs. PW		150		ps	See Note 8; See Figure 6

Parameter	AD1321KZ Min	Typ	Max	Units	Comments
DYNAMIC PERFORMANCE					
Inhibit Mode					See Figure 2
Delay Time					See Note 9
Drive-to-Inhibit	1.1		1.7	ns	
Inhibit-to-Drive	1.6		2.2	ns	
Edge-to-Edge Matching	−250	±100	+250	ps	
Overshoot & Preshoot		40	80	mV	See Figure 3
Output Capacitance		8	10	pF	
Output Charge Going into Inhibit Mode		15		pC	See Figure 13
Leakage Current in Inhibit Mode					
−2 V to +5 V		50	200	nA	
+5 V to +7 V			1.0	μA	
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range		15.2	15.4	Volts	
Supply Range					See Note 10
Positive Supply	+8.0	+10.0	+12.0	Volts	
Negative Supply	−7.2	−5.2	−3.2	Volts	
Current					
Positive Supply	42	60	78	mA	
Negative Supply	−78	−60	−42	mA	
$+PSRR\ V_{OH} = +7$ V	0.5		0.5	$\%/\%V_{OUT}$	+V = ±2.5%
$-PSRR\ V_{OL} = -2$ V	0.5		0.5	$\%/\%V_{OUT}$	−V = ±2.5%

NOTES

[1]The output voltage range is specified for −2 V to +7 V for typical power supply values of −5.2 V and +10.0 V but can be offset for different values of V_{OUT} such as 0 V to +9 V as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $-V_S$.

[2]V_H can be set to be as much as 4 volts below V_L without any harm to the driver with the restriction that neither level can go below −2 V with the typical power supply setting. In this condition the rise and fall times will approximately double.

[3]The gain error of the driver is always in the negative direction with respect to the voltage set level.

[4]Transient output current can easily exceed the AD1321's steady-state current limit when driving capacitive loads. The transient output current capability can be increased by connecting 0.039 μF capacitors between Pin 5 and ground and Pin 6 and ground. This will prevent the driver from current limiting by providing the "edge" current necessary when driving capacitive loads. These capacitors will not affect the driver's dc current limit.

[5]Driver output resistance is trimmed and guaranteed for a 3 V swing into a 50 ohm cable.

[6]Delay times are measured from the crossing of differential ECL outputs at the inputs to the driver to the 50% point of an ±400 mV driver output.

[7]Due to uncontrolled inductances in the test socket, overshoot, preshoot and settling time cannot be 100% tested. These characteristics are guaranteed based on characterization data.

[8]Delay matching vs. PW is defined as the amount of change in propagation, with respect to the leading edge, due to change in pulsewidth of the input signal. The AD1321 is characterized over the pulsewidth range of 5 ns to 100 ns.

[9]Inhibit mode delay times are measured from the crossing of differential (ECL) INH inputs to a 200 mV transition at the pin driver output. V_{OUT} is connected to a 100 ohm/15 pF load terminated to ground. $V_{O'I}$ is set at +1 V and V_{OL} is set at −1 V for this test.

[10]A supply range of 15.2 V must be maintained to guarantee a 9 V output swing.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- $+V_S$ to GND . . . . . +13 V
- $-V_S$ to GND . . . . . −8.2 V
- Difference from $+V_S$ to $-V_S$ . . . . . 16 V

Inputs
- Difference from D to $\overline{D}$ . . . . . 5 V
- Difference from INH to $\overline{INH}$ . . . . . 5 V
- D, $\overline{D}$, INH, $\overline{INH}$ . . . . . $+V_S$ −12 V, $-V_S$ +11.5 V
- V_H to V_L . . . . . −4 V, +9 V
- V_H, V_L . . . . . $+V_S$ −13.0 V, $-V_S$ +13.2 V

Driver Output
- Voltage . . . . . $+V_S$ −13.0 V, $-V_S$ +13.2 V
- Short Circuit to GND . . . . . Indefinite

Operating Temperature Range . . . . . 0 to +70°C
Storage Temperature Range . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 20 sec)† . . . . . +300°C

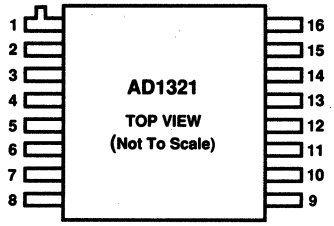
NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

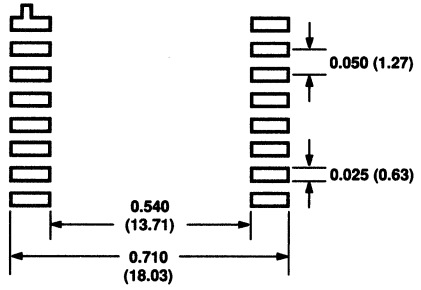
†To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

CONNECTION DIAGRAMS

Dimensions shown in inches and (mm).



SUGGESTED LANDING PADS LOCATION



PIN CONFIGURATION

PIN NO.	SYMBOL	FUNCTION
1	GND	CIRCUIT GROUND
2	N/C	NO CONNECTION
3	V_{OUT}	DRIVER OUTPUT
4	N/C	NO CONNECTION
5	C_{I+}	POSITIVE DECOUPLE
6	C_{I-}	NEGATIVE DECOUPLE
7	V_L	VOLTAGE LOGIC LOW
8	N/C	NO CONNECTION
9	LID	LID CONNECTION*
10	V_H	VOLTAGE LOGIC HIGH
11	$\overline{D}$	$\overline{\text{DRIVER INPUT}}$
12	D	DRIVER INPUT
13	$\overline{INH}$	$\overline{\text{INHIBIT INPUT}}$
14	INH	INHIBIT INPUT
15	$-V_S$	NEGATIVE SUPPLY
16	$+V_S$	POSITIVE SUPPLY

*IT IS RECOMMENDED TO CONNECT PIN 9 TO CIRCUIT GROUND.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD1321KZ	0 to +70°C	16-Lead Gull Wing (Z-16A)

*For outline information see Package Information section.

OFFSET ERROR

The offset error for logic high is determined by holding the output of the driver at logic high, and applying zero volts to the logic high reference input. The driver output value represents the offset "high" error. The same approach is used to identify offset "low" error

$$V_{HIGH\ OFFSET} = V_{OUT}$$

where:

V_H = 0 V
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH.

GAIN ERROR

Defined as the ratio of the driver's output voltage to its logic set level voltage and is expressed in terms of percent of set level. The gain error is typically seen as 2.5% and is always in the negative direction with respect to the logic set level

$$V_{HIGH\ GAIN}\ (\%) = \frac{V_{OUT} - V_H - V_{HIGH\ OFFSET}}{V_H} \times 100$$

where:

V_H = 5.0 V+$V_{HIGH\ OFFSET}$
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH.

LINEARITY ERROR

The deviation of the transfer function from a reference line. For the AD1321, the linearity error is calculated by subtracting the worst case gain error from the best case gain error (for the specified range) and divide the result by two. This method guarantees that the maximum linearity error for any set level within the specified range will be within the specified limits

where:

$$V_{HIGH\ LINEARITY}\ (\%) = \frac{V_{HIGH\ GAIN}\ (max) - V_{HIGH\ GAIN}\ (min)}{2} \times 100.$$

DELAY TIME

The amount of time it takes the input signal to propagate through the driver and be converted to the desired logic levels. The measurement technique is defined in the notes and is shown in Figure 2.

EDGE-TO-EDGE MATCHING

Edge-to-edge matching is the difference, in time, between the delay time of the rising edge and the falling edge.

MINIMUM PULSEWIDTH

Defined as the smallest pulse applied to the input of the driver which can maintain an output signal amplitude of 2 V. The minimum pulsewidth is measured at the 50% points of the waveform.

OVERSHOOT AND PRESHOOT

The amount by which the driver's output voltage exceeds the desired set voltage. Preshoot is similar to overshoot but is the amount by which the driver's output goes below the initial voltage when driving to the new set level (or inhibit mode). See Figure 3.

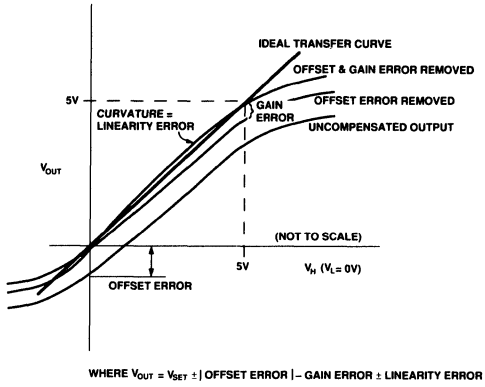


Figure 1. Definition of Terms

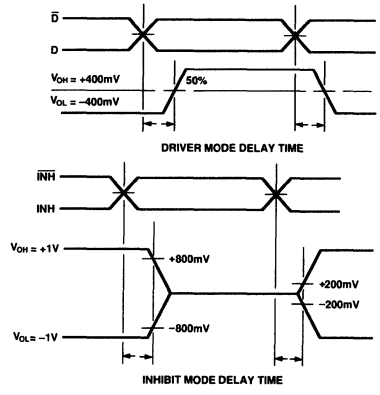


Figure 2. Timing Diagram for Driver and Inhibit Propagation Delay

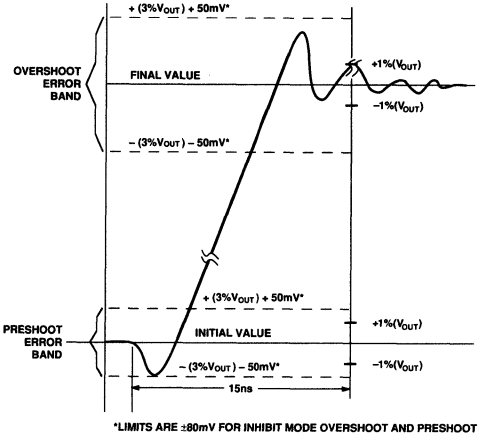


Figure 3. Definition of Waveform Aberrations

AD1321—Typical Performance Characteristics

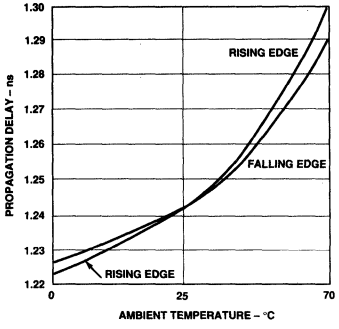


Figure 4. Driver Propagation Delay vs. Temperature

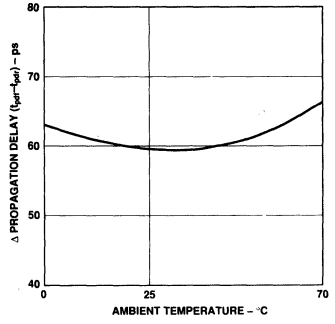


Figure 5. Propagation Delay Edge Matching vs. Temperature

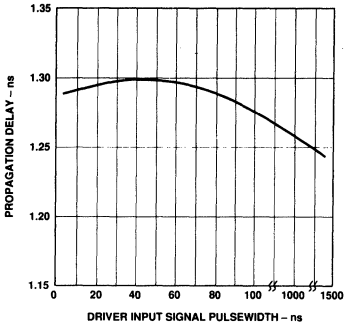


Figure 6. Propagation Delay vs. Input Signal Pulsewidth

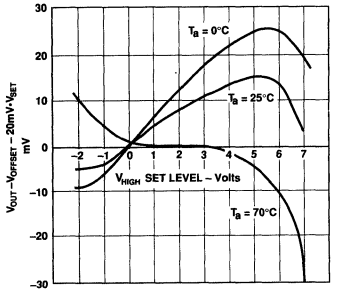


Figure 7. Change in V_{HIGH} over Temperature

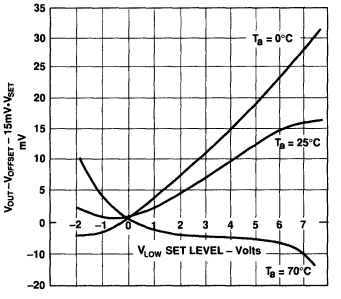


Figure 8. Change in V_{LOW} over Temperature

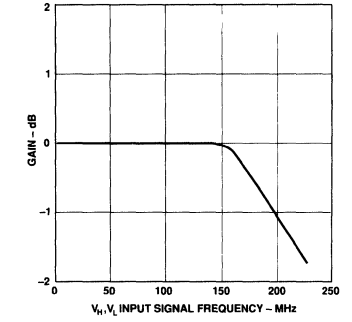


Figure 9. V_{HIGH} , V_{LOW} Input Bandwidth

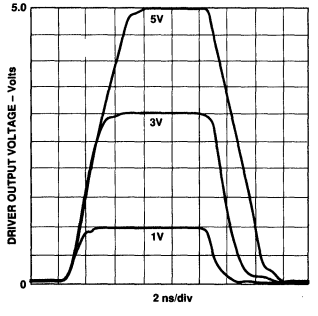


Figure 10. 10 ns Output Pulse at 1 V, 3 V and 5 V

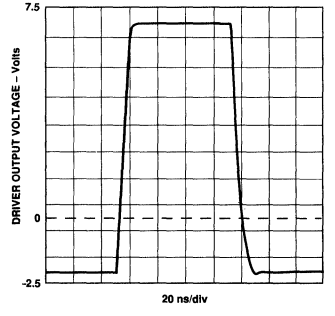


Figure 11. V_{OUT} = 9 V as Seen at the End of a 50 ns, 50 Ω Cable

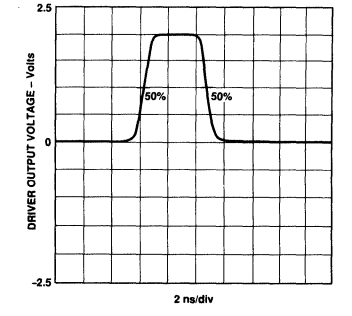


Figure 12. Minimum (Data) Pulsewidth as Defined by V_{OUT} = 2 V, 50% Crossing ≤ 5 ns

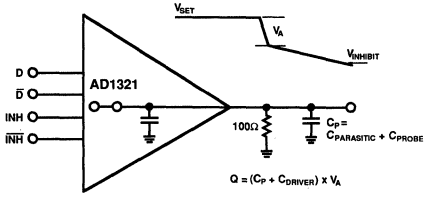


Figure 13. Charge into Inhibit Test Setup

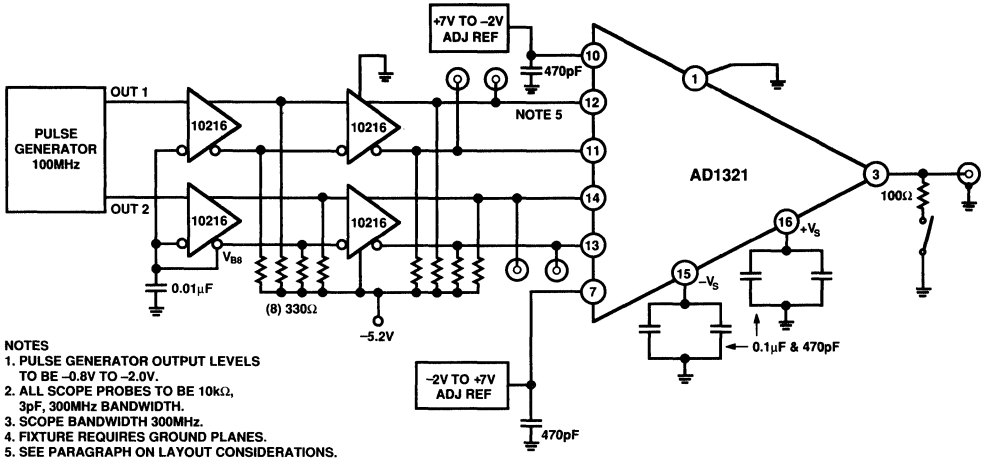


Figure 14. AD1321 Test Setup

6

FUNCTIONAL DESCRIPTION

The AD1321 is a complete high speed pin driver designed for use in general purpose instrumentation and digital functional test equipment. The purpose of a pin driver is to accept digital, analog and timing information from a system source and combine these to drive the device to be tested.

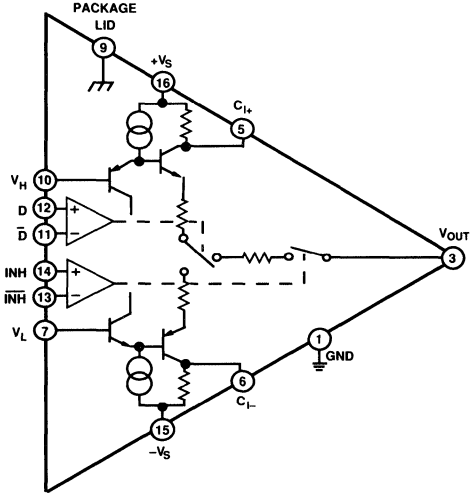


Figure 15. AD1321 Block Diagram

The circuit configuration for the AD1321 is outlined in Figure 15. Simply stated, a pin driver performs the function of a precise, high speed level translator with an output which can be disabled. The AD1321 accepts differential digital information utilizing a high speed differential design on the D and INH inputs providing precise timing at logic crossover and high noise immunity. The wide input voltage range allows for ECL operation with power supplies at 0 to −5.2 V, +2 V to −3.2 V or +5 V to 0 V. Where timing is less critical, TTL or CMOS logic levels may be used to toggle the AD1321. By biasing the D and INH inputs to approximately +1.3 V for TTL and 1/2 V_{CC} for CMOS, the D and INH inputs can be directly driven from these single-ended output sources. The output of the pin driver will follow the logic state of the D input providing the INH input is low. When inhibit is asserted, the output is disconnected and any activity on the input does not affect the output.

Analog information is provided to the pin driver through the V_H and V_L terminals as reference voltages. These analog voltages are buffered internally using unity gain followers. The resulting gain and linearity errors are provided in the specification table. System timing requirements are achieved through a specified 1.2 ns, ±400 ps driver propagation delay, 1.0 V/ns slew rate, defined preshoot and overshoot, and a dynamically trimmed 50 Ω output impedance.

LAYOUT CONSIDERATIONS

While it is generally considered good engineering practice to capacitively decouple the power supplies of an active device, it is absolutely essential for a high power, high speed device such as the AD1321. The engineer merely has to consider the current pulse demand from the power supply when a dynamic current change of −100 mA to +100 mA is required in only a few nanoseconds. Therefore, a 470 pF high frequency decoupling capacitor must be located within 0.25 inches of the $+V_S$ and $-V_S$ terminals to a low impedance ground. A 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor should also be situated between the power supplies and ground however, the proximity to the device is less critical assuming low impedance power supply distribution techniques are employed. Circuit performance will be similarly enhanced and noise minimized by locating a 470 pF capacitor as close as possible to V_H, V_L and connected to ground. Bypass considerations have been summarized in Figure 16.

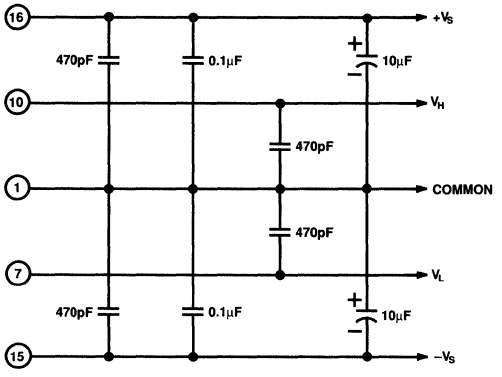


Figure 16. Basic Circuit Decoupling

An equally important consideration is the use of microwave stripline techniques on the output of the AD1321. Failure to preserve the 50 Ω output impedance of the pin driver will result in unwanted reflections, ringing and general corruption of the wave shape. Care should be exercised when selecting etch widths and routing, wire and cable to the device to be tested, and in choosing relays if they are required.

THERMAL CONSIDERATIONS

The AD1321 is provided in a 0.450″ × 0.450″, 16-lead (bottom brazed) gull wing, surface mount package with a typical junction-to-case thermal resistance of 5.6°C/W. Thermal resistance θ_{CA} (case to ambient) vs. air flow for the AD1321 in this package is shown in Figure 17. The improvement in thermal resistance vs. air flow begins to flatten out just above 400 lfm[1,2].

NOTES
[1]lfm is air flow in Linear Feet/Minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

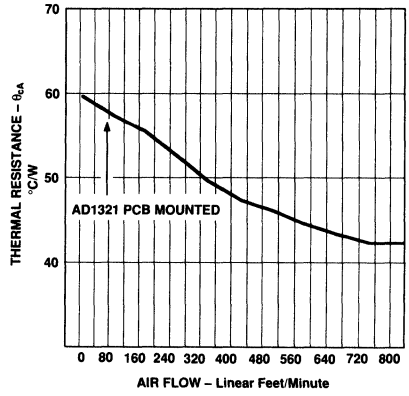


Figure 17. Case-to-Ambient Thermal Resistance vs. Air Flow

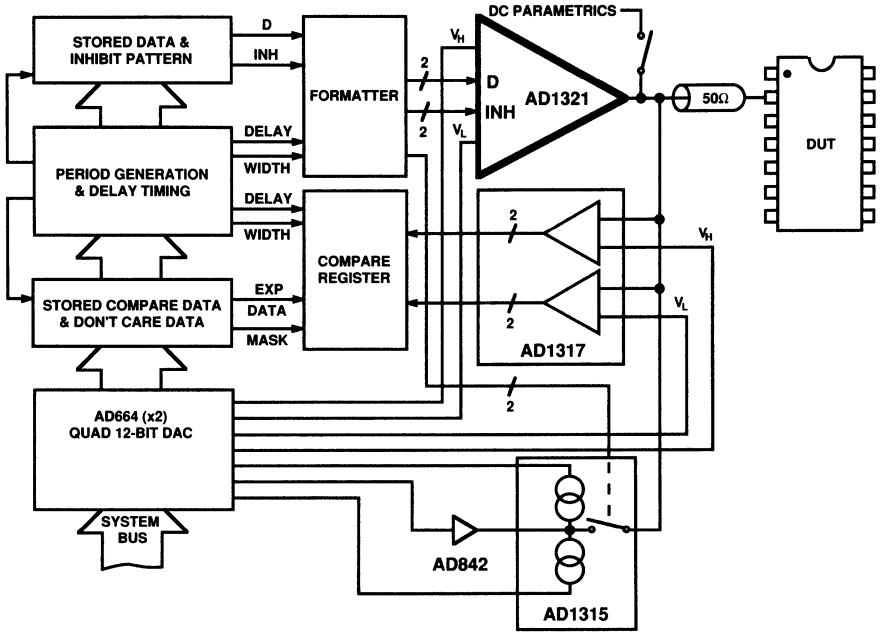
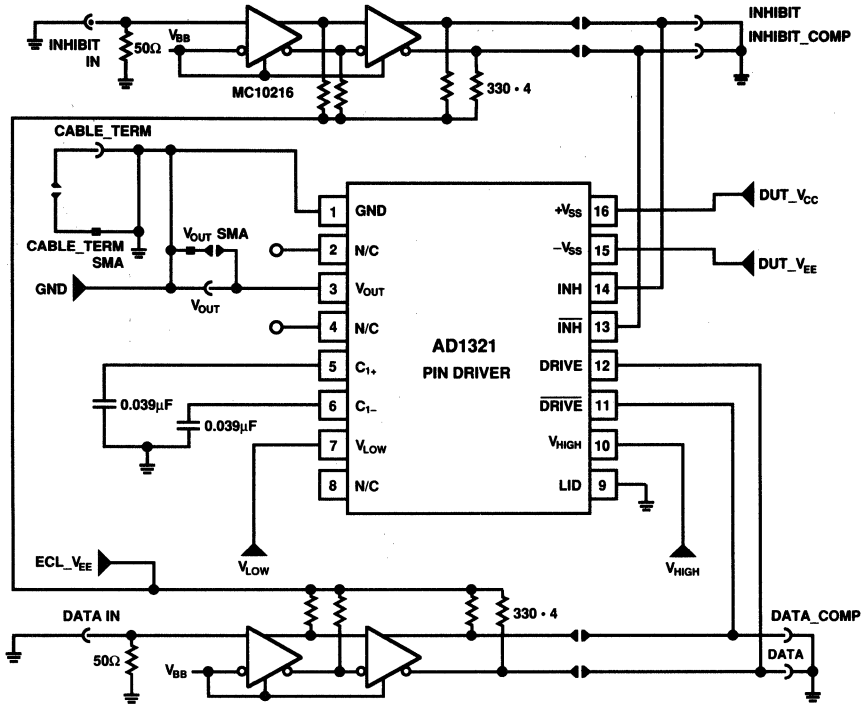


Figure 18. High Speed Digital Test System Block Diagram

APPLICATIONS

The AD1321 has been optimized to function as a pin driver in an ATE test system. Shown in Figure 18 is a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. The AD1321 pin driver, AD1317 high speed dual comparator, AD1315 active load, and the AD664 quad 12-bit voltage DAC would comprise the pin electronic portion of the test system. Such a system could operate at 100 MHz in a data mode or 50 MHz in the I/O mode, yet fit into a neat trim package.



NOTES:
"HALF-MOON" CONNECTORS CAN BE CONNECTED OR DISCONNECTED AS REQUIRED . . .
DECOUPLING CAPS ARE NOT SHOWN ON THIS SCHEMATIC, BUT THE BOARD USES 0.1µF AND 470pF CAPS TO DECOUPLE THE V_{CC}, V_{EE}, V_{LOW} AND V_{HIGH} SUPPLIES.
SMA CONNECTORS ■
PROBE JACKS)
BNC CONNECTORS (

Figure 19. AD1321EB Evaluation Board Schematic

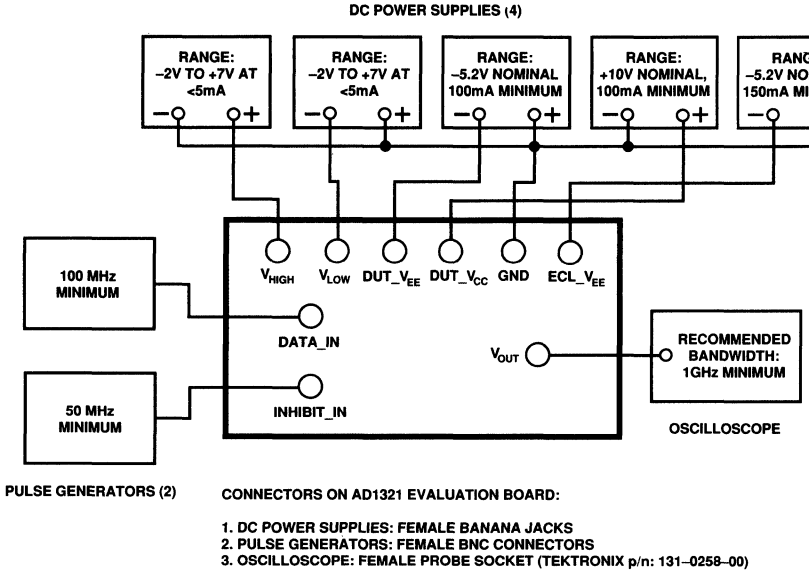


Figure 20. AD1321 Evaluation Board Connections

AD1321 EVALUATION BOARD

Introduction

The AD1321EB evaluation board was developed to aid the customer in quickly evaluating the performance of the AD1321. Included is complete documentation of the evaluation board along with suggestions on equipment to use and measurement limitations.

Overview

The AD1321 is a high speed pin driver used in automatic test equipment.

The device has true differential inputs for both the drive and inhibit which can be driven from either TTL or ECL logic levels (ECL is recommended). Standard ECL design and layout techniques should be used.

The device runs from dual power supplies +10 V and −5.2 V. It is very important that these power supplies are decoupled properly at the device pin. (High frequency oscillations will couple through to the device output.)

The reference input pins are dc inputs; therefore they also should be decoupled properly. The reference input range is −2 V to +7 V.

The output slew rate is 1 V/ns for large signals and has a rep rate for an ECL level of 100 MHz minimum.

Equipment

The Drive and Inhibit inputs should be driven with standard ECL levels. If the full performance of the AD1321 needs to be evaluated, the generator must be able to supply an ECL level at frequencies greater than 200 MHz. Motorola's MC10216 is used on the evaluation board to simulate the actual application. V_{BB} is used on the MC10216 as the logic reference and the outputs have 330 ohm pulldowns to V_{EE}.

Five power supplies are required: DUT_V_{CC}, DUT_V_{EE}, V_{HIGH}, V_{LOW} and ECL_V_{EE}. DUT_V_{CC} requires +10 V at 100 mA minimum; DUT_V_{EE} requires −5.2 V at 100 mA minimum; ECL_V_{EE} requires −5.2 V at 150 mA minimum. V_{HIGH} and V_{LOW} require −2 V to +7 V at 5 mA (each).

The output performance of the pin driver can only be measured properly with a scope which has the proper bandwidth for the required application. The input impedance and the bandwidth of the scope probe should be taken into consideration when evaluating the performance of the device. The resultant bandwidth of the system is the RMS value of the components in the system.

The characterizations performed by Analog Devices were performed using the following equipment: Tektronix 11402 mainframe (1 GHz BW), P6203 FET probe (1 GHz, 1.2 pF, 1 M ohm) and 11A71 plug-in (1 GHz BW, 50 ohm).

The Hewlett-Packard 54120 and 54110 were also evaluated with 500 ohm, 1.2 pF passive probes and the Data Precision 6100 with their model 640 FET probe (50 kΩ, 4 pF). When measuring the performance of waveforms close to or exceeding the bandwidth of a scope, it is not uncommon for the results between scopes to be different because of aberrations and slew rates.

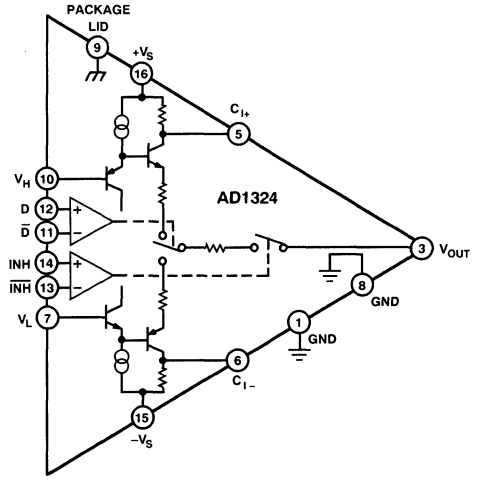
Ultrahigh Speed Pin Driver with Inhibit Mode

AD1324

FEATURES
200 MHz Driver Operation
Driver Inhibit Function
200 ps Edge Matching
Guaranteed Industry Specifications
50 Ω Output Impedance
2 V/ns Slew Rate
Variable Output Voltages for ECL, TTL and CMOS
High Speed Differential Inputs for Maximum Flexibility
Hermetically Sealed Small Gull Wing Package

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems
Instrumentation & Characterization Equipment

FUNCTIONAL BLOCK DIAGRAM



6

PRODUCT DESCRIPTION

The AD1324 is a complete high speed pin driver designed for use in digital or mixed signal test systems. By combining a high speed monolithic process with a unique surface mount package, this product attains superb electrical performance while preserving optimum packaging densities and long term reliability in an ultrasmall 16-lead, hermetically sealed gull wing package.

Featuring unity gain programmable output levels of −2 V to +7 V with output swing capability of less than 100 mV to 9 V, the AD1324 is designed to stimulate ECL, TTL and CMOS logic families. The 200 MHz (2.5 ns pulsewidth) data rate capacity, and matched output impedance allows for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (inhibit mode) electrically removing the driver from the path, through the inhibit mode feature. The pin driver leakage current in inhibit is typically 50 nA, and output charge transfer entering inhibit is typically less than 15 pC.

The AD1324 transition from HI/LO or to inhibit is controlled through the data and inhibit inputs. The input circuitry is implemented utilizing high speed differential inputs with a common-mode range of 3 volts. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog logic HI/LO inputs are equally easy to interface. Typically requiring 15 μA of bias current, the AD1324 can be directly coupled to the output of a digital-to-analog converter.

The AD1324 is available in a 16-lead, hermetically sealed gull wing package and is specified to operate over the ambient commercial temperature range from 0°C to +70°C.

AD1324—SPECIFICATIONS (All measurements made in free air at +25°C. Output load 10 kΩ/6 pF with $+V_S = +10$ V, $-V_S = -5.2$ V unless otherwise specified)

Parameter	AD1324KZ Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Input Voltage, Any Input	−3.0		+5.5	Volts	
Differential Input Range	0.4	ECL	3.0	Volts	
Bias Current	−1350	+200	+500	μA	
REFERENCE INPUTS					See Note 1
V_{HIGH} Range (V_H)	−2.5		+7.5	Volts	
V_{LOW} Range (V_L)	−2.5		+7.5	Volts	
Bias Currents	−40	±15	40	μA	
Bias Current Change		2	10	μA	See Note 2
OUTPUT CHARACTERISTICS					See Notes 1, 3
Logic High Range	−1.6		+7.0	Volts	
Logic Low Range	−2.0		+6.6	Volts	
Amplitude [$V_H - V_L$]	0.4		+9.0	Volts	
Accuracy					
Initial Offset	−200		+200	mV	
Gain Error	−3.0	−1.0	0.0	% of V_{SET}	
Linearity Error					See Note 4
−1.0 V to +5.6 V	−(0.2% + 10)		(0.2% + 10)	% of V_{SET} + mV	V_L
−1.0 V to +6.0 V	−(0.2% + 10)		(0.2% + 10)	% of V_{SET} + mV	V_H
−2.0 V to −1.0 V	−(0.2% + 40)		(0.2% + 40)	% of V_{SET} + mV	V_L, V_H
+6.0 V to +7.0 V	−(0.2% + 40)		(0.2% + 40)	% of V_{SET} + mV	V_H
+5.6 V to +7.0 V	−(0.2% + 40)		(0.2% + 40)	% of V_{SET} + mV	V_L
Output Voltage Drift		0.5		mV/°C	
Current Drive					
Static	30			mA	
Dynamic	100			mA	See Note 5
Current Limit	35		85	mA	Output to GND
Output Resistance	48.5	50.0	51.5	Ω	See Note 6
Leakage Current in Inhibit Mode					
−1 V to +6 V	−1	±0.25	+1	μA	T_J = 95°C ± 5°C; See Note 7
−2 V to +7 V	−10		+10	μA	T_J = 95°C ± 5°C; See Note 7
DYNAMIC PERFORMANCE					See Note 8
Driver Mode					
Delay Time	0.9	1.2	1.5	ns	See Note 9
Prop Delay TC		1.0		ps/°C	
Delay Time Matching Edge-to-Edge	0	50	250	ps	
Rise & Fall Times					See Note 10
1 V Swing	0.4	0.6	0.8	ns	Measurement 20%–80%
2 V Swing	1.0	1.2	1.4	ns	Measurement 10%–90%
3 V Swing	1.4	1.7	2.0	ns	Measurement 10%–90%
5 V Swing	2.3	2.6	2.9	ns	Measurement 10%–90%
9 V Swing		5.5	6.5	ns	Measurement 10%–90%
Toggle Rate	200			MHz	ECL Output
Large Signal Slew Rate		1.5		V/ns	
Minimum Pulsewidth, V_{OUT} = 2 V		2.0		ns	See Figure 11
Overshoot & Preshoot					
1 V to 7 V	−(3% V_O) −50		+(3%V_O) +50	mV	% of V_{OUT} Swing; See Note 11
Settling Time					
1 V to 7 V, ±(1% × V_O)			15	ns	See Note 11
Delay Time vs. PW		100		ps	See Note 12
DYNAMIC PERFORMANCE					
Inhibit Mode Delay Time					See Note 13
Drive-to-Inhibit	1.0	1.3	1.6	ns	
Inhibit-to-Drive	1.4	1.9	2.4	ns	
Delay Time Matching					
Edge-to-Edge	0	100	400	ps	1 V Swing
Overshoot & Preshoot			300	mV	
Output Capacitance		3.5	5	pF	
Output Charge Going into Inhibit Mode		5		pC	

Parameter	AD1324KZ Min	Typ	Max	Units	Comments
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range		15.2	15.6	Volts	
Supply Range					See Note 14
Positive Supply	+8.0	+10.0	+11.0	Volts	
Negative Supply	−7.2	−5.2	−4.2	Volts	
Current					
Positive Supply	42	82	100	mA	
Negative Supply	−100	−82	−42	mA	
PSRR		5	20	mV/V	$+V_S$, $-V_S$ = ±2.5%

NOTES

[1]The output voltage range is specified for −2 V to +7 V for typical power supply values of −5.2 V and +10.0 V but can be offset for different values of V_{OUT} such as −1 V to +8 V or −4 V to +5 V as long as the required headroom of 3 V is maintained between both V_H and $+V_S$ and V_L and $-V_S$.

[2]V_H and V_L inputs have internal buffers which reduce the input bias current requirements. These buffers also reduce the amount of bias current change when the output switches logic levels.

[3]V_H must remain at least 400 mV more positive than V_L for specified performance. V_H may be as much as 5 V more negative than V_L, with degraded performance.

[4]Linearity testing is performed in 1 V increments over the following ranges:
V_L Linearity: V_H fixed at +7.0 V, V_L = −2.0 V to +6.6 V;
V_H Linearity: V_L fixed at −2.0 V, V_H = −1.6 V to +7.0 V.
Linearity error includes the error due to interaction for a minimum amplitude of 400 mV. Interaction error testing is performed with V_H = −0.6 V, V_L = −1.0 V and with V_H = +6.0 V, V_L = +5.6 V.

[5]Transient output current can easily exceed the AD1324's steady-state current limit when driving capacitive loads. The transient output current capability can be increased by connecting 0.039 µF capacitors between Pin 5 and $+V_S$ and between Pin 6 and $-V_S$. This will prevent the driver from current limiting by providing the "edge" current necessary when driving capacitive loads. These capacitors will not affect the driver's dc current limit.

[6]Driver output impedance is 50 Ω for a 3 V p–p signal into a 50 Ω load.

[7]While in inhibit mode, the output voltage must not go more than 6 V above V_{HIGH} or 6 V below V_{LOW}.

[8]The driver output has 2 ns length of 50 Ω coaxial cable attached with a 10 kΩ/6 pF probe, 1 GHz bandwidth or equivalent at the far end.

[9]Delay times are measured from the crossing of differential ECL levels at the input to the 50% point of an 800 mV driver output with V_H and V_L set at ±400 mV, respectively.

[10]Rise and fall time performance guaranteed over the output range of $+V_S$ −4 V to $-V_S$ +4.2 V except for 9 V swing, which is measured over the output range of $+V_S$ −3 V to $-V_S$ + 3.2 V.

[11]Due to uncontrolled inductances in the test socket, overshoot, preshoot and settling time cannot be 100% tested. These characteristics are guaranteed by characterization data .

[12]Delay matching vs. PW is defined as the amount of change in propagation delay, with respect to the leading edge, due to change in pulsewidth of the input signal. The specification applies over the pulsewidth range of 2.5 ns to 100 ns.

[13]Inhibit mode delay times are measured from the crossing of differential (ECL) INH inputs to a 200 mV crossing at the pin driver's output connected to 2 ns length of 50 Ω coaxial cable. The cable is terminated to ground through a 50 Ω resistor. The measurement is made at the 50 Ω resistor to GND with a 10 kΩ/6 pF scope probe.

[14]A supply range of 15.2 V must be maintained to guarantee a 9 V output swing.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage
- $+V_S$ to GND . . . . . +13 V
- $-V_S$ to GND . . . . . −8.2 V
- Difference from $+V_S$ to $-V_S$ . . . . . 16 V

Inputs
- Difference from D to $\overline{D}$ . . . . . 4.75 V
- Difference from INH to $\overline{INH}$ . . . . . 4.75 V
- D, $\overline{D}$, INH, $\overline{INH}$ . . . . . $+V_S$ − 13 V, $-V_S$ + 11.5 V
- V_H to V_L . . . . . −1 V, +9 V
- V_H, V_L . . . . . $+V_S$ − 13.2 V, $-V_S$ + 13.2 V

Driver Output
- Voltage . . . . . $+V_S$ − 13.2 V, $-V_S$ + 13.2 V
- Short Circuit to GND . . . . . Indefinite

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +125°C
Lead Temperature Range (Soldering 20 sec)† . . . . . +300°C

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†To ensure lead coplanarity (±0.002 inches) and solderability handling with bare hands should be avoided and the device should be stored in an environment at 24°C, ±5°C (75°F, ±10°F) with relative humidity not to exceed 65%.

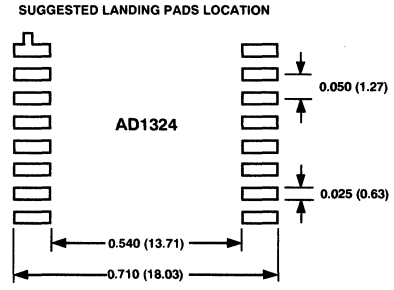
ORDERING GUIDE

Model	Temperature Range	Description	Package Option*
AD1324KZ	0 to +70°C	16-Lead Gull Wing	Z-16A

*For outline information see Package Information section.

CONNECTION DIAGRAMS

Dimensions shown in inches and (mm).



PIN DESCRIPTION

Pin No.	Symbol	Function
1	GND	Circuit Ground
2	N/C	No Connection
3	V_{OUT}	Driver Output
4	N/C	No Connection
5	C_{I+}	Positive Decouple
6	C_{I-}	Negative Decouple
7	V_L	Voltage Logic Low
8	GND	Internal Ground*
9	LID	Lid Connection*
10	V_H	Voltage Logic High
11	$\overline{D}$	Driver Input
12	D	Driver Input
13	$\overline{INH}$	Inhibit Input
14	INH	Inhibit Input
15	$-V_S$	Negative Supply
16	$+V_S$	Positive Supply

*It is recommended to connect Pins 8 and 9 to Circuit Ground.

OFFSET ERROR

The offset error for logic high is determined by holding the output of the driver at logic high, and applying zero volts to the logic high reference input. The driver output value represents the offset "high" error. The same approach is used to identify offset "low" error.

$$V_{HIGH\ OFFSET} = V_{OUT}$$

where:

V_H = 0 V
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH

GAIN ERROR

Defined as the ratio of the driver's output voltage to its logic set level voltage and is expressed in terms of percent of set level. The gain error is typically seen as 1.0% and is always in the negative direction with respect to the logic set level.

$$V_{HIGH\ GAIN}\ (\%) = \frac{V_{OUT} - V_H - V_{HIGH\ OFFSET}}{V_H} \times 100$$

where:

V_H = 5.0 V+$V_{HIGH\ OFFSET}$
D = HIGH
$\overline{D}$ = LOW
INH = LOW
$\overline{INH}$ = HIGH

LINEARITY ERROR

The deviation of the transfer function from a reference line. For the AD1324, the linearity error is calculated by subtracting the worst case gain error from the best case gain error (for the specified range) and dividing the result by two. This method guarantees that the maximum linearity error for any set level within the specified range will be within the specified limits.

$$V_{HIGH\ LINEARITY}\ (\%) = \frac{V_{HIGH\ GAIN}\ (max) - V_{HIGH\ GAIN}\ (min)}{2} \times 100$$

DELAY TIME

The amount of time it takes the input signal to propagate through the driver and be converted to the desired logic levels. The measurement technique is defined in the notes and is shown in Figure 2.

EDGE-TO-EDGE MATCHING

Edge-to-edge matching is the difference, in time, between the delay time of the rising edge and the falling edge.

MINIMUM PULSEWIDTH

Defined as the smallest pulse applied to the input of the driver which can maintain an output signal amplitude of 2 V. The minimum pulsewidth is measured at the 50% point of the waveform.

OVERSHOOT AND PRESHOOT

The amount by which the driver's output voltage exceeds the desired set voltage. Preshoot is similar to overshoot but is the amount by which the driver's output goes above or below the initial voltage when driving to the new set level (or inhibit mode). See Figure 3.

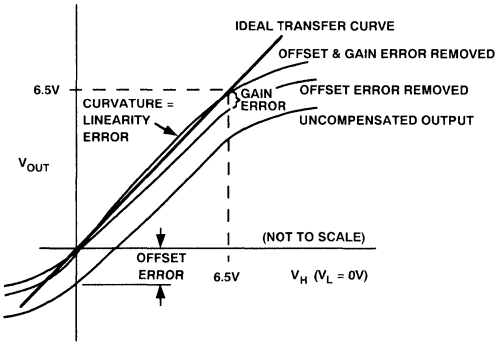


Figure 1. Definition of Terms

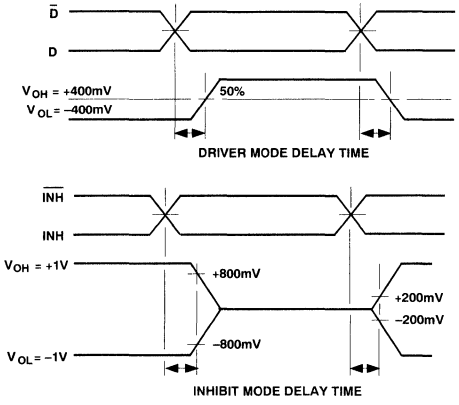


Figure 2. Timing Diagram for Driver and Inhibit Propagation Delay

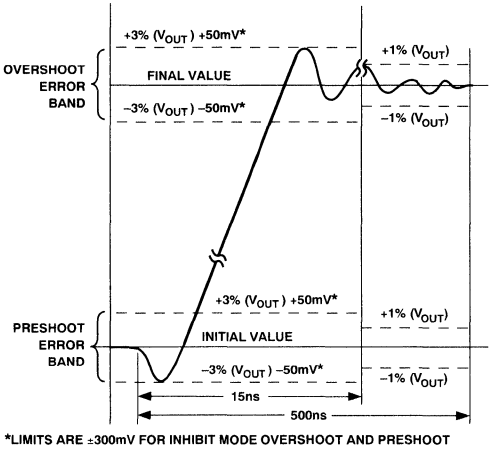


Figure 3. Definition of Waveform Aberrations

AD1324—Typical Performance

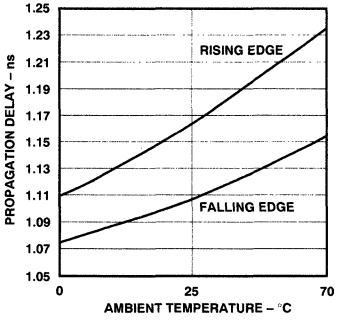


Figure 4. Driver Propagation Delay vs. Temperature

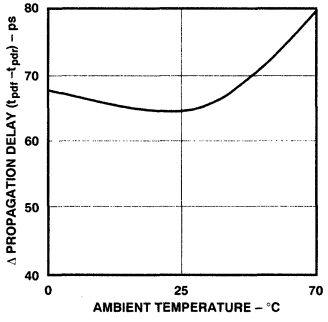


Figure 5. Propagation Delay Edge Matching vs. Temperature

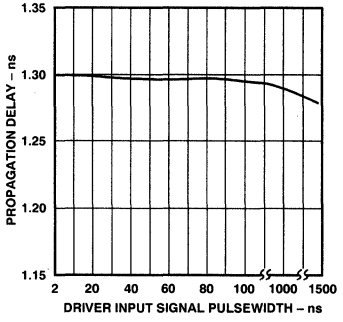


Figure 6. Propagation Delay vs. Input Signal Pulsewidth

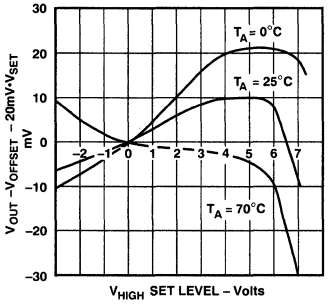


Figure 7. Change in V_{HIGH} over Temperature

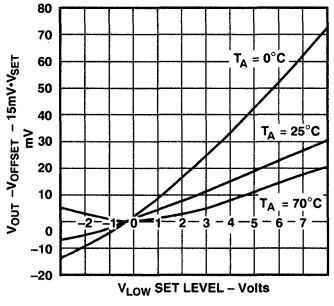


Figure 8. Change in V_{LOW} over Temperature

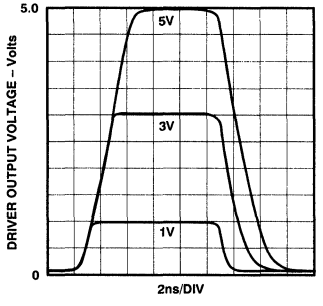


Figure 9. 10 ns Output Pulse at 1 V, 3 V and 5 V

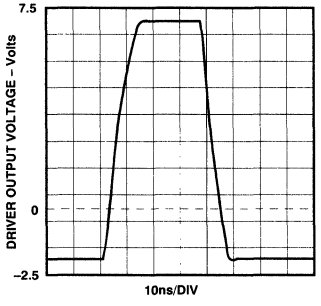


Figure 10. V_{OUT} = 9 V as Seen at the End of a 50 ns, 50 Ω Cable

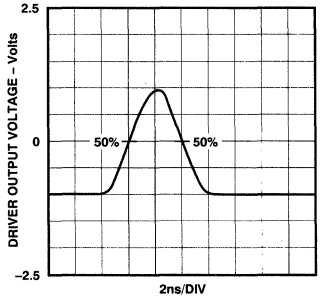


Figure 11. Minimum (Data) Pulse-width as Defined by V_{OUT} = 2 V, 50% Crossing ≤ 2 ns

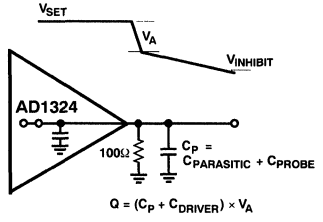


Figure 12. Charge into Inhibit Test Setup

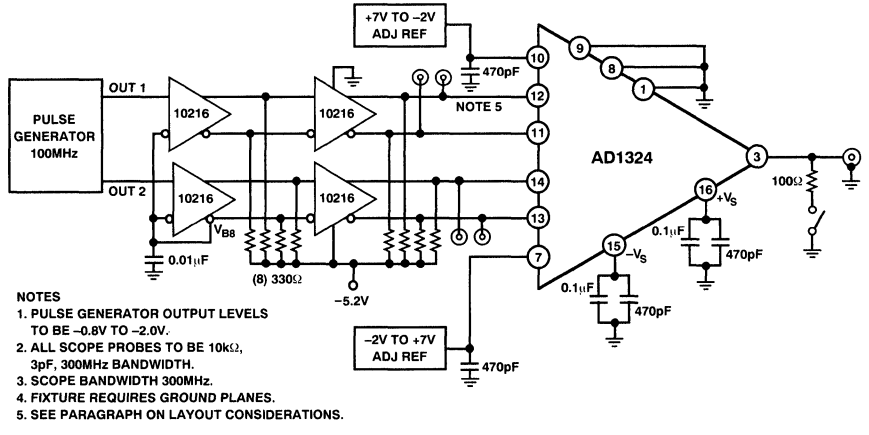


Figure 13. AD1324 Test Setup

6

FUNCTIONAL DESCRIPTION

The AD1324 is a complete high speed pin driver designed for use in general purpose instrumentation and digital functional test equipment. The purpose of a pin driver is to accept digital, analog and timing information from a system source and combine these to drive the device to be tested.

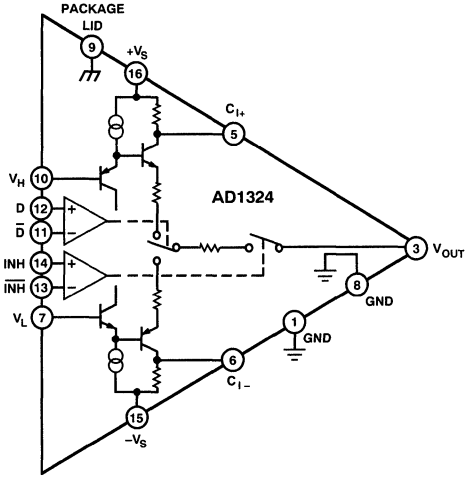


Figure 14. AD1324 Block Diagram

The circuit configuration for the AD1324 is outlined in Figure 14. Simply stated, a pin driver performs the function of a precise, high speed level translator with an output which can be disabled. The AD1324 accepts differential digital information utilizing a high speed differential design on the D and INH inputs providing precise timing at logic crossover and high noise immunity. The wide input voltage range allows for ECL operation with power supplies at 0 to −5.2 V, +2 V to −3.2 V or +5 V to 0 V. Where timing is less critical TTL or CMOS logic levels may be used to toggle the AD1324. By biasing the D and INH inputs to approximately +1.3 V for TTL and 1/2 V_{CC} for CMOS, the D and INH inputs can be directly driven from these single-ended output sources. The output of the pin driver will follow the logic state of the D input providing the INH input is low. When inhibit is asserted the output is disconnected and any activity on the input does not affect the output.

Analog information is provided to the pin driver through the V_H and V_L terminals as reference voltages. These analog voltages are buffered internally using unity gain followers. The resulting gain and linearity errors are provided in the specification table. System timing requirements are achieved through a specified 1.2 ns, ±300 ps driver propagation delay, defined preshoot and overshoot, and a dynamically trimmed 50 Ω output impedance.

LAYOUT CONSIDERATIONS

While it is generally considered good engineering practice to capacitively decouple the power supplies of an active device, it is absolutely essential for a high power, high speed device such as the AD1324. The engineer merely has to consider the current pulse demand from the power supply when a dynamic current change of −100 mA to +100 mA is required in only a few nanoseconds. Therefore, a 470 pF high frequency decoupling capacitor must be located within 0.25 inches of the $+V_S$ and $-V_S$ terminals to a low impedance ground. A 0.1 μF capacitor in parallel with a 10 μF tantalum capacitor should also be situated between the power supplies and ground. However, the proximity to the device is less critical assuming low impedance power supply distribution techniques are employed. Circuit performance will be similarly enhanced and noise minimized by locating a 470 pF capacitor as close as possible to V_H, V_L and connected to ground. Bypass considerations have been summarized in Figure 15.

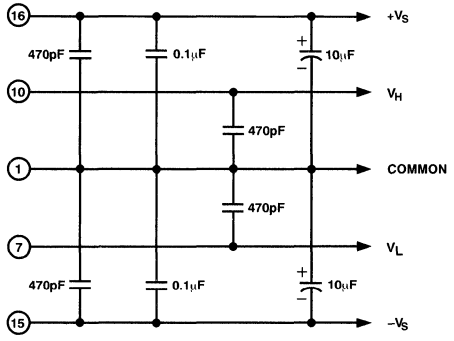


Figure 15. Basic Circuit Decoupling

An equally important consideration is the use of microwave stripline techniques on the output of the AD1324. Failure to preserve the 50 Ω output impedance of the pin driver will result in unwanted reflections, ringing and general corruption of the wave shape. Care should be exercised when selecting etch widths and routing, wire and cable to the device to be tested, and in choosing relays if they are required.

THERMAL CONSIDERATIONS

The AD1324 is provided in a 0.450″ × 0.450″, 16 lead (bottom brazed) gull wing, surface mount package with a typical junction-to-case thermal resistance of 17.5°C/W. Thermal resistance θ_{CA} (case to ambient) vs. air flow for the AD1324 in this package is shown in Figure 16. The improvement in thermal resistance vs. air flow begins to flatten out just above 400 lfm[1, 2].

NOTES
[1]lfm is air flow in Linear Feet/Minute.
[2]For convection cooled systems, the minimum recommended airflow is 400 lfm.

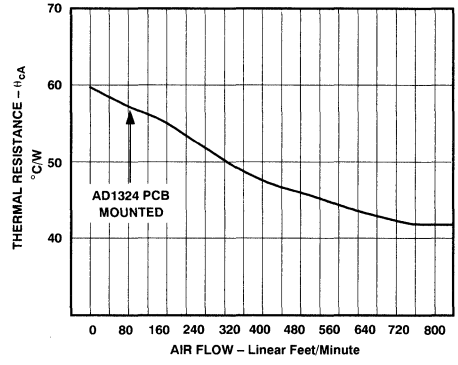


Figure 16. Case-to-Ambient Thermal Resistance vs. Air Flow

APPLICATIONS

The AD1324 has been optimized to function as a pin driver in an ATE test system. Shown in Figure 18 is a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. The AD1324 pin driver, AD1317 high speed dual comparator, AD1315 active load, and the AD75069 octal 12-bit voltage DAC would comprise the pin electronic portion of the test system. Such a system could operate at 200 MHz in a data mode or 100 MHz in the I/O mode, yet fit into a neat trim package.

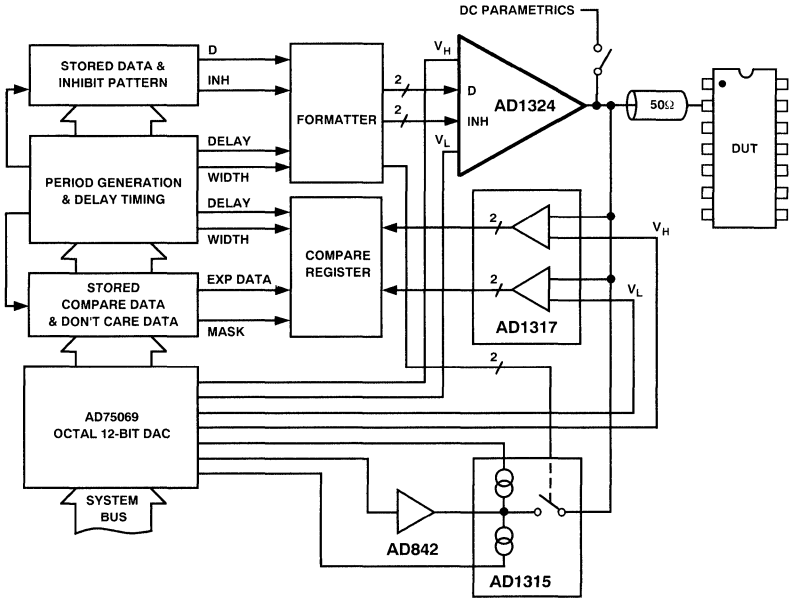


Figure 17. High Speed Digital Test System Block Diagram

6

AD1324 EVALUATION BOARD

Introduction

The AD1324EB evaluation board was developed to aid in quickly evaluating the performance of the AD1324. Included is complete documentation of the evaluation board along with suggestions on equipment to use and measurement limitations.

Overview

The AD1324 is a high speed pin driver used in automatic test equipment

The device has true differential inputs for both the drive and inhibit which can be driven from either TTL or ECL logic levels (ECL is recommended). Standard ECL design and layout techniques should be used.

The device runs from dual power supplies +10 V and −5.2 V. It is very important that these power supplies are decoupled properly at the device pin. (High frequency oscillations will couple through to the device output.)

The reference input pins are dc inputs; therefore they also should be decoupled properly. The reference input range is −2 V to +7 V.

The output slew rate is 2 V/ns for large signals and has a repetition rate for an ECL level of 200 MHz minimum.

Equipment

The Drive and Inhibit inputs should be driven with standard ECL levels. If the full performance of the AD1324 needs to be evaluated, the generator must be able to supply an ECL level at frequencies greater than 200 MHz. Motorola's MC10216 is used on the evaluation board to simulate the actual application. V_{BB} is used on the MC10216 as the logic reference and the outputs have 330 ohm pulldowns to V_{EE}.

Five power supplies are required: DUT_V_{CC}, DUT_V_{EE}, V_{HIGH}, V_{LOW} and ECL_V_{EE}. DUT_V_{CC} requires +10 V at 100 mA minimum; DUT_V_{EE} requires −5.2 V at 100 mA minimum; ECL_V_{EE} requires −5.2 V at 150 mA minimum. V_{HIGH} and V_{LOW} require −2 V to +7 V at 5 mA (each).

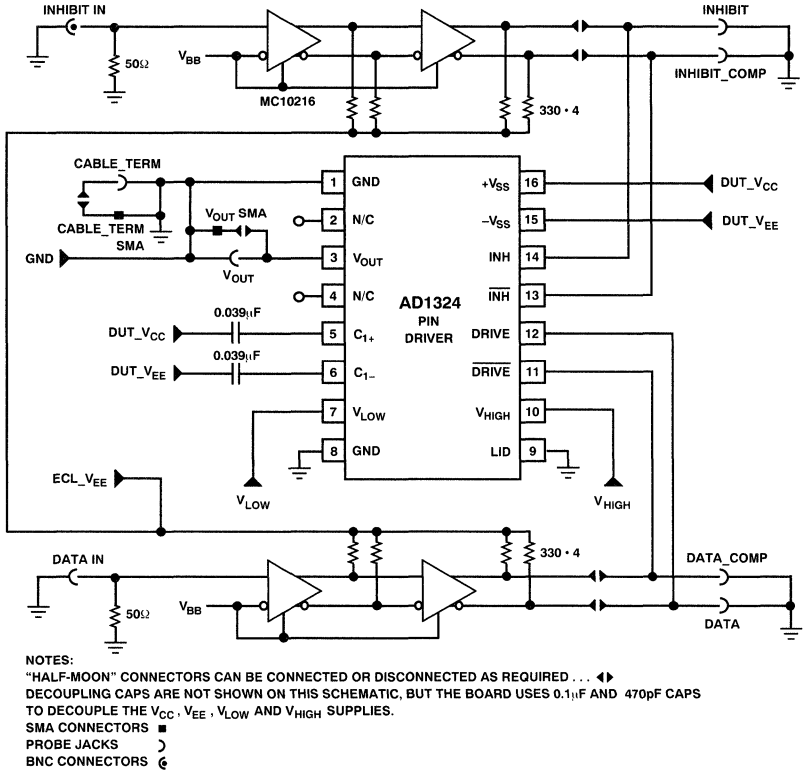


Figure 18. AD1324EB Evaluation Board Schematic

The output performance of the pin driver can only be measured properly with a scope which has the proper bandwidth for the required application. The input impedance and the bandwidth of the scope probe should be taken into consideration when evaluating the performance of the device. The resultant bandwidth of the system is the rms value of the components in the system.

The characterizations performed by Analog Devices were performed using the following equipment: Tektronix 11402 mainframe (1 GHz BW), P6203 probe (1 GHz, 2 pF, 10 kΩ), and 11A71 plug-in (1 GHz BW, 50 Ω).

The Hewlett-Packard 54120 and 54110 were also evaluated with 500 Ω, 1.2 pF passive probes and the Data Precision 6100 with their model 640 FET probe (50 kΩ, 4 pF). When measuring the performance of waveforms close to or exceeding the bandwidth of a scope, it is not uncommon for the results between scopes to be different because of aberrations and slew rates.

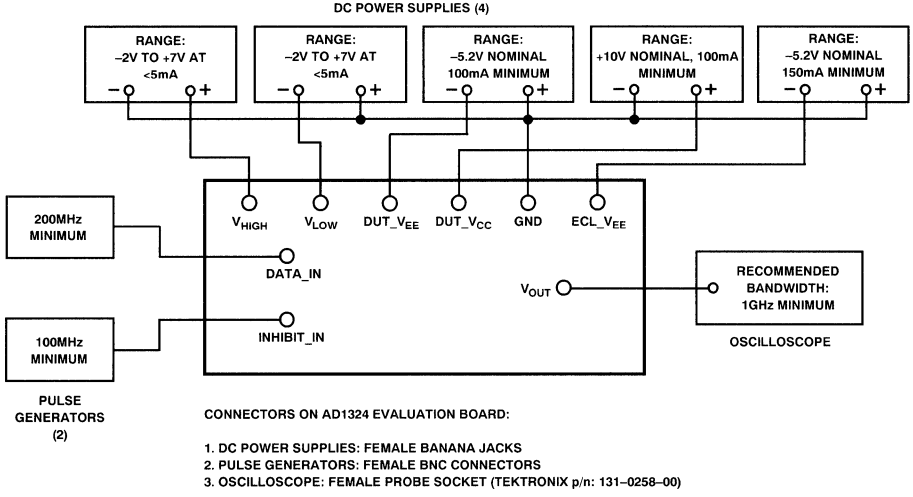


Figure 19. AD1324EB Evaluation Board Connections

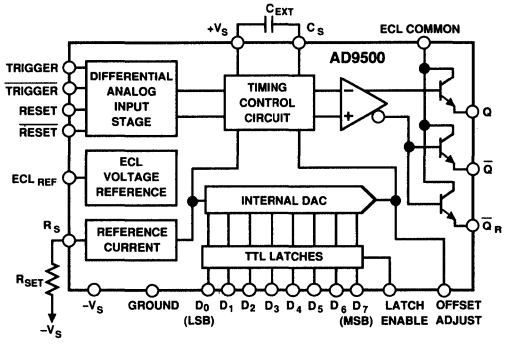
Digitally Programmable Delay Generator

AD9500

FEATURES
10ps Delay Resolution
2.5ns to 10μs Full-Scale Range
Fully Differential Inputs
Separate Trigger and Reset Inputs
Low Power Dissipation – 310mW
MIL-STD-883 Compliant Versions Available

APPLICATIONS
ATE
Pulse Deskewing
Arbitrary Waveform Generators
High-Stability Timing Source
Multiple Phase Clock Generators

FUNCTIONAL BLOCK DIAGRAM



6

GENERAL DESCRIPTION

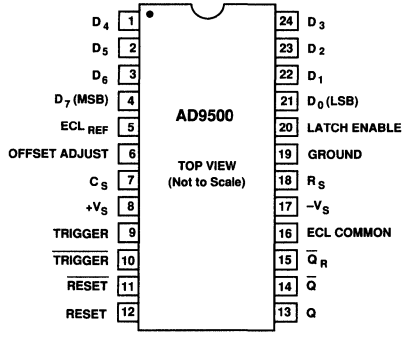
The AD9500 is a digitally programmable delay generator, which provides programmed delays, selected through an 8-bit digital code, in resolutions as small as 10ps. The AD9500 is constructed in a high-performance bipolar process, designed to provide high-speed operation for both digital and analog circuits.

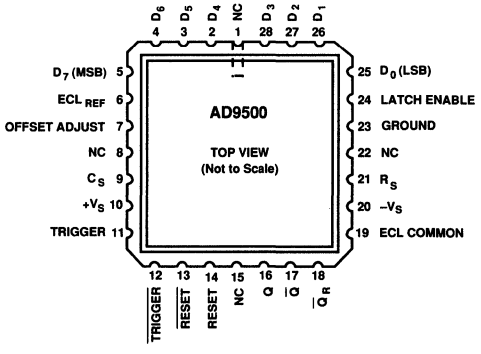
The AD9500 employs differential TRIGGER and RESET inputs which are designed primarily for ECL signal levels but function with analog and TTL input levels. An on-board ECL reference midpoint allows both of the inputs to be driven by either single ended or differential ECL circuits. The AD9500 output is a complementary ECL stage, which also provides a parallel $\overline{Q_R}$ output circuit to facilitate reset timing implementations.

The digital control data is passed to the AD9500 through a transparent latch controlled by the LATCH ENABLE signal. In the transparent mode, the internal DAC of the AD9500 will attempt to follow changes at the inputs. The LATCH ENABLE is otherwise used to strobe the digital data into the AD9500 latches.

The AD9500 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades are packaged in a 24-pin ceramic "Skinny" DIP (0.3" package width), as well as 28-pin surface mount packages. The AD9500 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9500/883B data sheet for detailed specifications.

PIN CONFIGURATIONS





AD9500—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +7V
Negative Supply Voltage ($-V_S$) . . . . . −7V
ECL COMMON to Ground Differential . . −2.0V to +5.0V
Digital Input Voltage Range . . . . . −3.5V to +5.0V
Trigger/Reset Input Voltage Range . . . . . ±5.0V
Trigger/Reset Differential Voltage 5.0V
Minimum R_{SET} 220Ω
Digital Output Current (Q and $\overline{Q}$) 30mA
Digital Output Current ($\overline{Q_R}$) 2mA
Offset Adjust Current (Sinking) 4mA
Operating Temperature Range
AD9500BP/BQ . . . . . −25°C to +85°C
AD9500TE/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages $+V_S$ = +5.0V, $-V_S$ = −5.2V; C_{EXT} = 0pF; R_{SET} = 500Ω, unless otherwise noted)

Parameter	Test Level	Temp	−25°C to +85°C AD9500BP/BQ Min	Typ	Max	−55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
RESOLUTION			8			8			Bits
ACCURACY[3]									
Differential Linearity	I	+25°C			0.5			0.5	LSB
Integral Linearity	I	+25°C			1.0			1.0	LSB
Monotonicity	I	+25°C		Guaranteed			Guaranteed		
DIGITAL INPUT									
Logic "1" Voltage	VI	Full	2.0			2.0			V
Logic "0" Voltage	VI	Full			0.8			0.8	V
Logic "1" Current	VI	Full			5			5	μA
Logic "0" Current	VI	Full			5			5	μA
Digital Input Capacitance	VI	+25°C			5.5			5.5	pF
Data Setup Time[4]	V	+25°C		0.4	0.75		0.4	0.75	ns
Data Hold Time[5]	V	+25°C		0.4	0.75		0.4	0.75	ns
Latch Pulse Width (t_{LPW})	V	+25°C	3.0			3.0			ns
RESET/TRIGGER INPUTS[6]									
TRIGGER Input Voltage Range	IV	Full		−2.5; 4.5			−2.5; 4.5		V
RESET Input Voltage Range	IV	Full		−2.5; 2.0			−2.5; 2.0		V
Differential Switching Voltage	IV	Full		40	300		40	300	mV
Input Bias Current	I	+25°C		40	50		40	50	μA
	VI	Full			75			75	μA
Input Resistance	IV	+25°C		4			4		kΩ
Input Capacitance	IV	+25°C		6.5	7.25		6.5	7.25	pF
Minimum Input Pulse Width t_{TPW}, t_{RPW}	V	+25°C		2.0			2.0		ns
DYNAMIC PERFORMANCE[7]									
Maximum Trigger Rate	IV	+25°C		60			60		MHz
Minimum Propagation Delay (t_{PD})[8]	I	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Minimum Propagation Delay TC	V	Full		7.5			7.5		ps/°C
Full-Scale Range TC[9]	V	Full		0.5			0.5		ps/°C
Delay Uncertainty (Jitter)	V	+25°C		10			10		ps
Reset Propagation Delay (t_{RD})[10]	I	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Reset-to-Trigger Holdoff (t_{THO})[11]	IV	+25°C	0.2	0		0.2	0		ns
Trigger-to-Reset Holdoff (t_{RHO})[12]	IV	+25°C	2.0	1.5		2.0	1.5		ns
Minimum Output Pulse Width	V	+25°C		3.3			3.3		ns
Output Rise Time[7]	I	+25°C			2.0			2.0	ns
Output Fall Time[7]	I	+25°C			2.0			2.0	ns
Delay Coefficient Settling Time (t_{DAC})[13]	V	+25°C		29			29		ns
Linear Ramp Settling Time (t_{LRS})	V	+25°C		22			22		ns

Parameter	Test Level	Temp	−25°C to +85°C AD9500BP/BQ Min	Typ	Max	−55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
SUPPORT FUNCTIONS									
ECL_{REF}	IV	+25°C	−1.4	−1.3	−1.2	−1.4	−1.3	−1.2	V
ECL_{REF} Voltage Drift[14]	V	Full		1.1			1.1		mV/°C
Offset Adjust Range	V	Full		−2			−2		mA
DIGITAL OUTPUTS[7]									
Logic "1" Voltage	VI	Full	−1.1			−1.1			V
Logic "0" Voltage	VI	Full			−1.5			−1.5	V
POWER SUPPLY[15]									
Positive Supply Current (+5.0V)	I	+25°C		24	28		24	28	mA
	VI	Full			30			30	mA
Negative Supply Current (−5.2V)	I	+25°C		37	42		37	42	mA
	VI	Full			44			44	mA
Nominal Power Dissipation	V	+25°C		312			312		mW
Power Supply Rejection Ratio[16]									
Full-Scale Range Sensitivity	I	+25°C		70	300		70	300	ps/V
Minimum Propagation Delay Sensitivity	I	+25°C		150	500		150	500	ps/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance

24-Pin Ceramic $\theta_{JA} = 56°C/W; \theta_{JC} = 16°C/W$

28-Pin PLCC (Plastic) $\theta_{JA} = 60°C/W; \theta_{JC} = 22°C/W$

28-Pin Ceramic LCC $\theta_{JA} = 69°C/W; \theta_{JC} = 25°C/W$

[3]R_{SET} = 10kΩ (Full-scale delay = 100ns).

[4]The digital data inputs must remain stable for the specified time prior to the LATCH ENABLE signal.

[5]The digital data inputs must remain stable for the specified time after the LATCH ENABLE signal.

[6]The TRIGGER and RESET inputs are differential and must be driven relative to one another. Both of these inputs are ECL compatible, but can also be used with TTL logic families in a limited fashion.

[7]Outputs terminated through 50Ω resistors to −2.0V.

[8]Program Delay = 0.0ps (Digital Data = 00_H). In Operation, any programmed delays are in addition to the Minimum Propagation Delay.

[9]Change in total delay through AD9500, exclusive of changes in minimum-propagation delay t_{PD}.

[10]Measured from the 50% transition point of the reset signal input, to the 50% transition point of the resetting output.

[11]Minimum time from falling edge of RESET to triggering input, to insure a valid output event.

[12]Minimum time from triggering event to rising edge of RESET, to insure a valid output event.

[13]Measured from the LATCH ENABLE input to the point when the AD9500 becomes 8-bit accurate again, after a full-scale change in the programmed delay.

[14]Standard 10K and 10KH ECL families operate with a 1.1mV/°C drift by design.

[15]Supply voltages should remain stable within ± 5% for normal operation.

[16]Measured at ± 5% of $-V_S$ and $+V_S$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Periodically sample tested.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

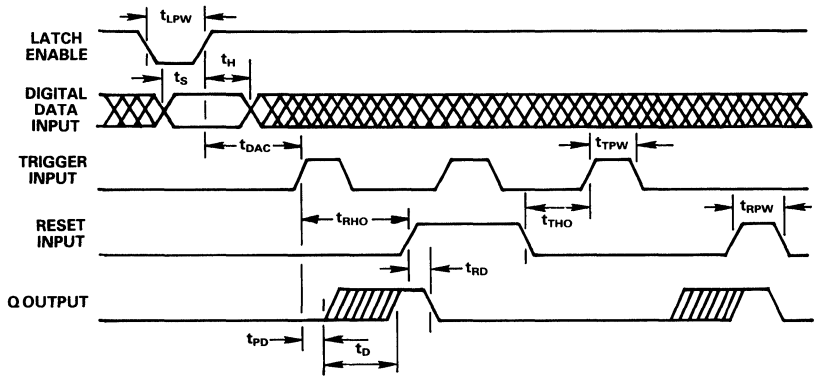
ORDERING INFORMATION

Model	Temperature Range	Description	Package Options*
AD9500BP	−25°C to +85°C	28-Pin PLCC (Plastic), Industrial Temperature	P-28A
AD9500BQ	−25°C to +85°C	24-Pin "Skinny" DIP, Industrial Temperature	Q-28
AD9500TE	−55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9500TQ	−55°C to +125°C	24-Pin "Skinny" DIP, Extended Temperature	Q-28

*E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
D_4–D_6	– One of eight digital inputs used to set the programmed delay.
D_7 (MSB)	– One of eight digital inputs used to set the programmed delay. D_7 (MSB) is the most significant bit of the digital input word.
ECL_{REF}	– ECL midpoint reference, nominally −1.3V. Use of the ECL_{REF}, allows either of the TRIGGER or the RESET inputs to be configured for single-ended ECL inputs.
OFFSET ADJUST	– The OFFSET ADJUST is used to adjust the minimum propagation delay (t_{PD}), by pulling or pushing a small current out of or into the pin.
C_S	– C_S allows the full-scale range to be extended by using an external timing capacitor. The value of C_{EXT}, connected between C_S and $+V_S$, may range from no external capacitance to 0.1μF+. See R_S ($C_{INTERNAL}$ = 10pF).
$+V_S$	– Positive supply terminal, nominally +5.0V.
TRIGGER	– Noninverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The TRIGGER input must be driven in conjunction with the $\overline{\text{TRIGGER}}$ input.
$\overline{\text{TRIGGER}}$	– Inverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The $\overline{\text{TRIGGER}}$ input must be driven in conjunction with the TRIGGER input.
$\overline{\text{RESET}}$	– Inverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The RESET input must be driven in conjunction with the $\overline{\text{RESET}}$ input.
RESET	– Noninverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The $\overline{\text{RESET}}$ input must be driven in conjunction with the RESET input.
Q	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic HIGH on the Q output. A "resetting" event at the inputs will produce a logic LOW on the Q output
$\overline{Q}$	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q}$ output.
$\overline{Q_R}$	– $\overline{Q_R}$ output is parallel to the $\overline{Q}$ output. The $\overline{Q_R}$ output is typically used to drive delaying circuits for extending output pulse widths. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q_R}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q_R}$ output.
ECL COMMON	– The collector common for the ECL output stage. The collector common may be tied to +5.0V, but normally it is tied to the circuit ground for standard ECL outputs.
$-V_S$	– Negative supply terminal, nominally −5.2V.
R_S	– R_S is the reference current setting terminal. An external setting resistor, R_{SET}, connected between R_S and $-V_S$ determines the internal reference current. See C_S ($250\Omega \leq R_{SET} \leq 50k\Omega$).
GROUND	– The ground return for the TTL and analog inputs.
LATCH ENABLE	– Transparent TTL latch control line. A logic HIGH on the LATCH ENABLE freezes the digital code at the logic inputs. A logic LOW on the LATCH ENABLE allows the internal current levels to be continuously updated through the logic inputs D_0 thru D_7.
D_0 (LSB)	– One of eight digital inputs used to set the programmed delay. D_0 (LSB) is the least significant bit of the digital input word.
D_3–D_1	– One of eight digital inputs used to set the programmed delay.



t_S – DIGITAL DATA SETUP TIME
t_H – DIGITAL DATA HOLD TIME
t_{LPW} – LATCH ENABLE PULSE WIDTH
t_{DAC} – INTERNAL DAC SETTLING TIME
t_{PD} – MINIMUM PROPAGATION DELAY
t_{RD} – RESET PROPAGATION DELAY
t_D – PROGRAMMED DELAY
t_{TPW} – TRIGGER PULSE WIDTH
t_{RPW} – RESET PULSE WIDTH
t_{THO} – RESET-TO-TRIGGER HOLDOFF
t_{RHO} – TRIGGER-TO-RESET HOLDOFF

NOTE
A TRIGGERING EVENT MAY OCCUR AT ANY TIME WHILE THE INTERNAL DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

System Timing Diagram

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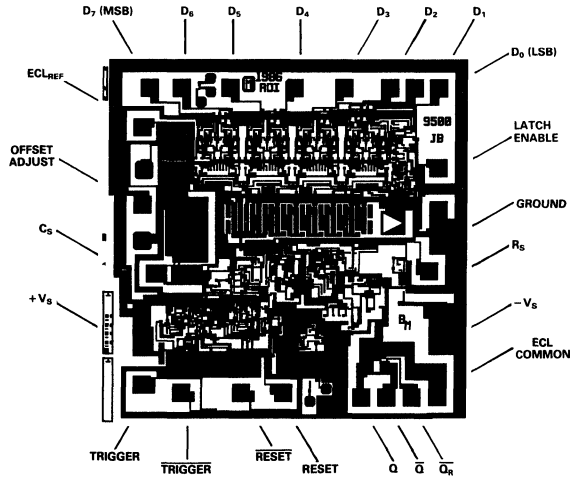
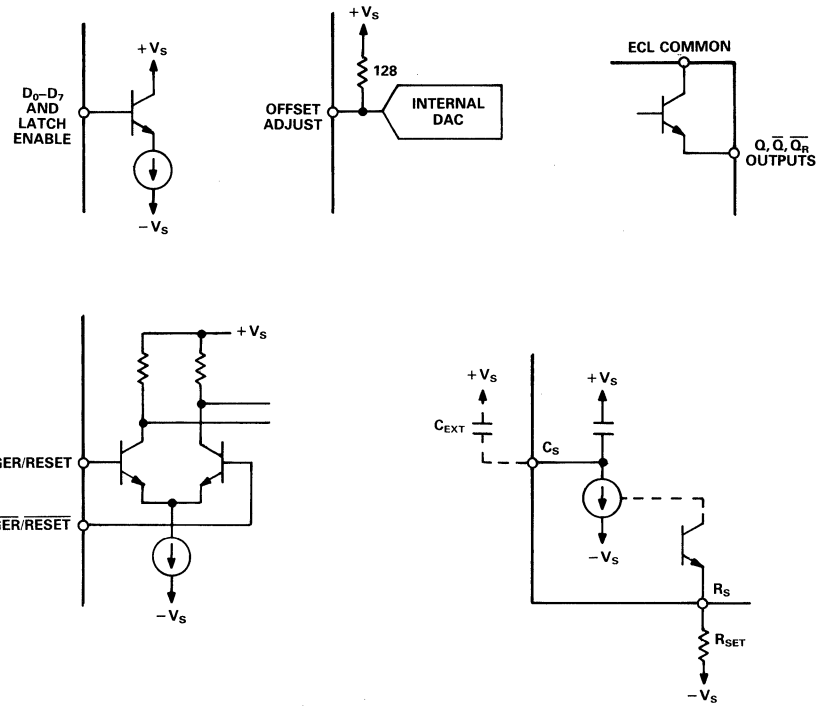
DIE LAYOUT



MECHANICAL INFORMATION

Die Dimensions	104 × 103 × 18 (max) mils
Pad Dimensions	4 × 4 (min)mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold; Gold Ball Bonding

Input/Output Circuits



INSIDE THE AD9500

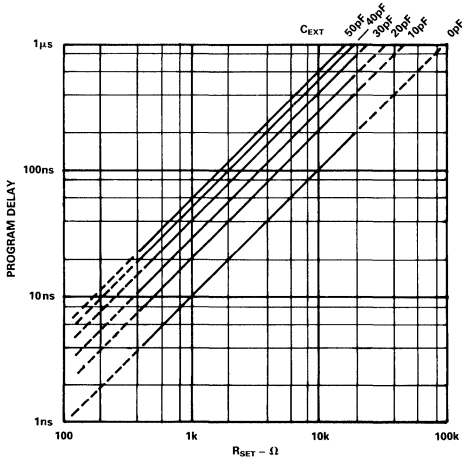
The heart of the AD9500 is the linear ramp generator. A triggering event at the input of the AD9500 initiates the ramp cycle. As the ramp voltage falls, it will eventualy go below the threshold set up by the internal DAC (digital-to-analog converter). A comparator monitors both the linear ramp voltage and the DAC threshold level. The output of the comparator serves as the output for the AD9500, and the interval from the trigger until the output switches is the total delay time of the AD9500.

The total delay through the AD9500 is made up of two components. The first is the full-scale programmed delay, $t_{D\ (max)}$, determined by R_{SET} and C_{EXT}. The second component of the total delay is the minimum propagation delay through the AD9500 (t_{PD}). The full-scale delay is variable from 2.5ns to greater than 1ms. The internal DAC is capable of generating 256 separate programmed delays within the full-scale range (this gives 10ps increments for a 2.5ns full-scale setting).

The actual programmed delay is directly related to both the digital control data (digital data to the internal DAC) and the RC time constant established by R_{SET} and C_{EXT}. The specific relationship is as follows:

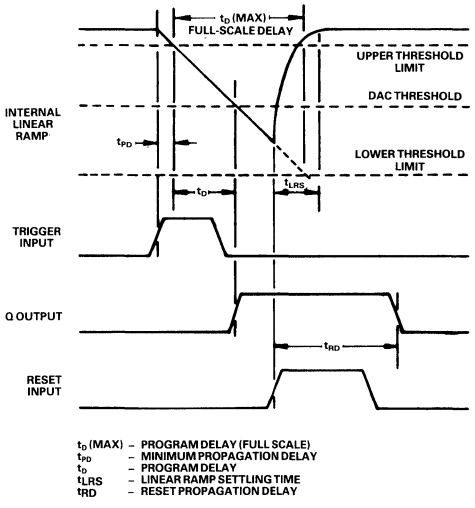
Total Delay = Minimum Propagation Delay + Programmed Delay

$= t_{PD} + (\text{digital value}/256)\ R_{SET}\ (C_{EXT} + 10pF)$



Typical Programmed Delay Ranges

The internal DAC determines the programmed delay by way of the threshold level at its output. The LATCH ENABLE control for the on-board latch is active (latches) logic "HIGH". In the logic "LOW" state, the latch is transparent, and the internal DAC will attempt to follow changes at the digital data inputs. Both the LATCH ENABLE control and the data inputs are TTL compatible. The internal DAC may be updated at any time, but full timing accuracy may not be attained unless triggering events are held off until after the DAC settling time (t_{DAC}).



Internal Timing Diagram

On resetting, the ramp voltage held in the timing capacitor (C_{EXT} + 10pF) is discharged. The AD9500 discharges the bulk of the ramp voltage very quickly, but to maintain *absolute* accuracy, subsequent triggering events should be held off until after the linear ramp settling time (t_{LRS}). Applications which employ high frequency triggering at a constant rate will not be affected by the slight settling errors since they will be constant for fixed reset-to-trigger cycles.

The RESET and TRIGGER inputs of the AD9500 are differential and must be driven relative to one another. Accordingly, the TRIGGER and RESET inputs are ideally suited for analog or complementary input signals. Single-ended ECL input signals can be accommodated by using the ECL midpoint reference (ECL_{REF}) to drive one side of the differential inputs.

The output of the AD9500 consists of both Q and $\overline{Q}$ driver stages, as well as the $\overline{Q_R}$ output which is used primarily for extending the output pulse width. In the most direct reset configuration, either the Q or the $\overline{Q}$ output is tied to the respective RESET input. This generates a delayed output pulse with a duration equal to the reset delay time (t_{RD}) of approximately 6ns. Note that the reset delay time (t_{RD}) becomes extended for very small programmed delay settings. The duration of the output pulse can be extended by driving the reset inputs with the $\overline{Q_R}$ output through an RC network (see "Extended Output Pulse Width" application). Using the $\overline{Q_R}$ output to drive the reset circuit avoids loading the Q or $\overline{Q}$ outputs.

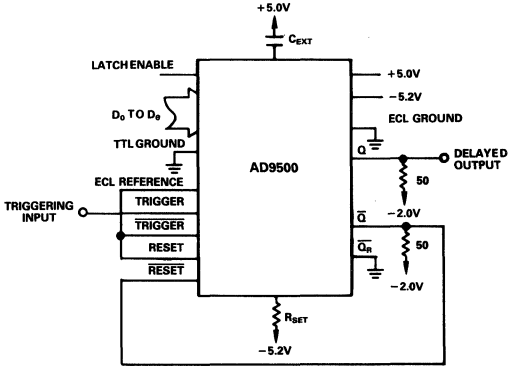
Values in the specification table are based on 5ns FSR test conditions. Nearly all dynamic specifications degrade for longer full-scales. For details of performance change, request the application note "Using Digitally Programmable Delay Generators."

APPLICATIONS

The AD9500 is a very versatile device, but at the same time, it is not difficult to use. Essentially there are only a few basic configurations which can be extended into a number of applications. The TRIGGER and RESET inputs of the AD9500 can be treated as single ended, or as differential, which allows the AD9500 to operate with a wide range of signal sources. The output pulse from the AD9500 can be reset in one of two ways, either immediately by driving the RESET inputs with the output itself, or in a delayed mode.

MINIMUM CONFIGURATION

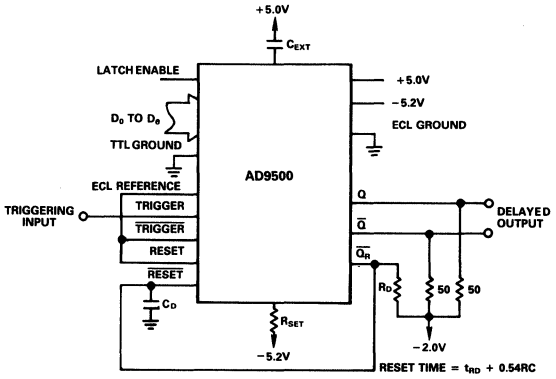
The minimum configuration uses only one of the TRIGGER inputs. The other is connected to the ECL reference midpoint, ECL_{REF}. This allows the AD9500 to be triggered with standard 10K or 10KH ECL signals. Once a triggering event occurs, the Q output will go into the logic HIGH state, and the $\overline{Q}$ output will go into the logic LOW state after the programmed delay. The Q output is then used to drive the RESET input, causing the AD9500 to reset itself. The result is a delayed output pulse which is only as wide as the reset propagation delay (t_{RD}).



Single Input – Minimum Timing Configuration

EXTENDED OUTPUT PULSE WIDTHS

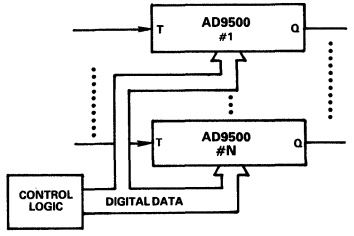
The extended pulse configuration is similar to the minimum configuration. The difference here is that the output pulse width has been extended. Operation is identical in terms of triggering the AD9500; the functional difference is in the resetting circuit. In this case the $\overline{Q_R}$ output is used to drive the $\overline{RESET}$ input through a resistor/capacitor charging network. The charging network will cause the signal at the $\overline{RESET}$ input to fall more slowly, which will extend the output pulse width. An added benefit of the extended pulse width configurations is that both the Q and the $\overline{Q}$ outputs are completely free for other uses. $\overline{Q}$ has limited current drive; the minimum resistance for R_D should be 4kΩ.



Extended Output Pulse Width Configuration

MULTICHANNEL DESKEWING

Perhaps the most appropriate use of the AD9500 is in multiple delay matching applications. Slight differences in impedance and cable length can create large timing skews within a high-speed system. Much of this skew can be eliminated by running each signal through an AD9500. With one line used as a standard, the programmed delays of the other AD9500s are adjusted to eliminate the timing skews. With the very fine timing adjustments possible from the AD9500 (as small as 10ps), nearly any high-speed system should be able to automatically adjust itself to extremely tight tolerances.

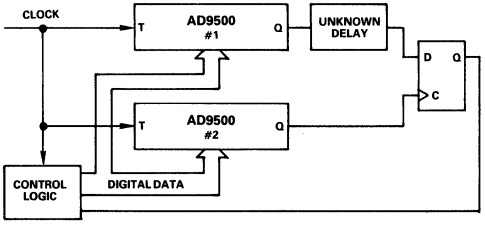


Multiple Delay Matching

MEASURING UNKNOWN DELAYS

Two AD9500s can be combined to measure delays with a high degree of precision. One AD9500 is set with little or no programmed delay, and its output is used to drive the unknown delay circuit, which in turn drives the input of a "D" type flipflop. The second AD9500 is triggered along with the first, and its output provides a clocking signal for the flipflop. The programmed delay of the second AD9500 is then varied to detect the output edge from the unknown delay circuit.

Detecting the output edge is relatively straightforward. If the programmed delay through the second AD9500 is too long, the flipflop output will be at logic HIGH. If, on the other hand, the programmed delay through the second AD9500 is too short, the flipflop output will be at logic LOW. When the programmed delay is properly adjusted, the flipflop will likely bounce between logic HIGH and logic LOW. The digital code value used to create the second programmed delay is a direct indication of the delay through the unknown circuit. The most accurate results can only be attained by calibrating the system without the unknown delay circuit in place.

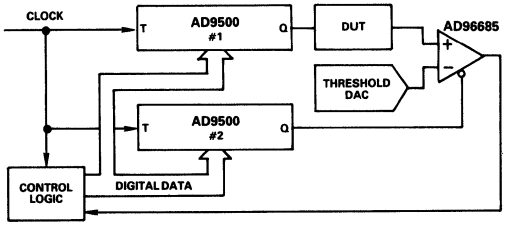


Measuring Unknown Delays

MEASURING HIGH-SPEED AC WAVEFORMS

The same circuitry used to measure unknown delays can be extended to measure the time response of high-speed ac waveforms. With the addition of a digital-to-analog converter and an analog comparator, the circuit functions very much like the previous application. The DAC sets a threshold level which drives one of the differential comparator inputs. The other comparator input is driven by the device under test (DUT). The output of the first AD9500 causes the DUT to produce an output. The second AD9500, which is also triggered along with the first AD9500, strobes the comparator latch enable.

If the DUT output is greater than the DAC threshold when the comparator is latched, the comparator output will be at logic HIGH. If the output is below the DAC threshold, the comparator will be at logic LOW. The programmed delay setting of the second AD9500 is adjusted to the point where the DUT output equals the DAC threshold. By varying the DAC threshold level and adjusting the second AD9500 programmed delay, a point by point reconstruction of the ac waveform can be created.

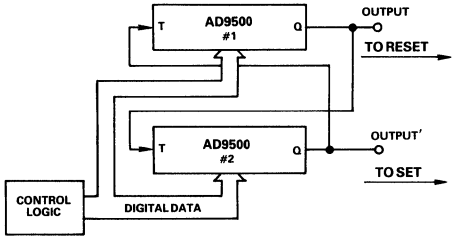


Measuring AC Waveforms

PROGRAMMABLE OSCILLATOR

Another interesting use of the AD9500 is in a digitally programmable oscillator. The highly accurate delays generated by the AD9500 can be exploited to create a ring oscillator with variable duty cycle. The delayed output of the first AD9500 is used to drive the TRIGGER input of the second AD9500. The output of the second AD9500, in turn, is used to drive the TRIGGER input of the first AD9500. Together the two devices will alternately trigger each other creating two pulse chains on the outputs.

The total delay through both AD9500s combined, determines the period of the oscillation frequency. The duty cycle can be controlled by using the outputs to drive the SET and RESET inputs of a flipflop. The total delay through the first AD9500 will control the flipflop logic LOW output pulse width, and the second AD9500 will control the flipflop logic HIGH output pulse width.



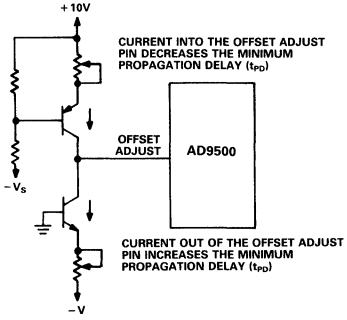
Ring Oscillator

LAYOUT CONSIDERATIONS

The AD9500 is a precision timing device, and as such high-frequency design techniques must be employed to achieve the best performance. The use of a low impedance ground plane is particularly important. Ideally the ground plane should be on the component side of the layout and extend under the AD9500, to shield it from system timing signals. Sockets pose a special problem for a circuit like the AD9500 because of the additional inter-lead capacitance they create. If sockets must be used, pin sockets are generally preferred. Power supply decoupling is also critical to a high-speed design; a 0.1μF ceramic capacitor and a 0.01μF mica capacitor for both power supplies should be very effective. DAC threshold stability can be improved by decoupling the OFFSET ADJUST pin to +5.0V (note that this will lengthen the DAC settling time, t_{DAC}).

DELAY OFFSET ADJUSTMENTS

As the full-scale delay is increased, a component of the minimum propagation delay also increases. This is caused by the additional time required by the ramp (now with a much "flatter" slope) to fall below the DAC threshold corresponding to the minimum propagation delay (t_{PD}). One means of decreasing the minimum propagation delay (when the full-scale delay, set by R_{SET} and C_{EXT} is large) is to offset the internal DAC threshold toward the initial ramp levels, thus reducing the time for the internal ramp to cross the threshold once the AD9500 is triggered.



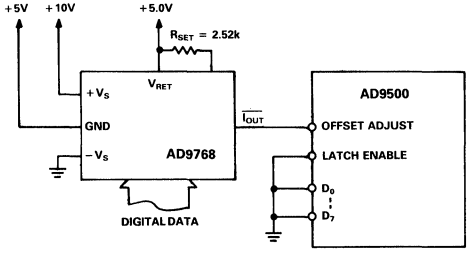
The Offset Adjust Pin Can Be Used to Match Several AD9500s

The DAC levels are offset toward the initial ramp level by injecting a small current into the offset adjust pin. Note, however, that the ramp start-up region is less linear than the later portions of the ramp, which is the primary reason for the built-in offset. If the minimum propagation delay is kept above 5ns (the linear portion of the ramp), no significant degradation in linearity should result. This concept can be extended to match the actual propagation delays of several AD9500s, by injecting or sinking a small current (<2mA) into or out of each of the OFFSET ADJUST pins.

GENERAL PERFORMANCE ENCHANCEMENTS

High-speed operation is generally more consistent if C_{EXT} is kept small (i.e., no external capacitor) to maintain small discharge time constants. Integral linearity, however, benefits from larger values of C_{EXT} by buffering small system spikes and surges. Another means of improving integral linearity is to draw a small current (≈200μA) out of the OFFSET ADJUST pin with a 47kΩ pull-down resistor. This has the effect of moving the internal DAC reference levels into a relatively more linear region of the ramp. This technique is generally only useful for small full-scale delay configurations. Its use with larger full-scale delays will extend the minimum propagation delay (t_{PD}). A pull-up resistor to +5.0V creates the opposite effect by reducing the minimum propagation delay (t_{PD}) at the expense of increased reset propagation delay (t_{RD}) and degraded linearity (see OFFSET matching circuit).

An external DAC can be used with the AD9500 for increased resolution and higher update rates. For the most part, a standard ECL DAC, operating between +5.0V and ground, should work with the AD9500. The output of the external DAC must be connected to the OFFSET ADJUST pin of the AD9500 with the internal DAC turned off (D_0 thru D_7 at logic LOW). For normal operation, the external DAC output should range from 0mA to −2mA (sinking).



Operation with External DAC

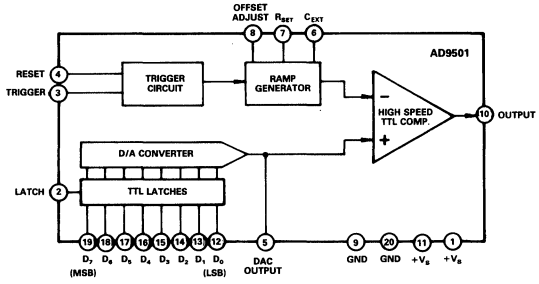
Digitally Programmable Delay Generator

AD9501

FEATURES
Single +5 V Supply
TTL and CMOS Compatible
10 ps Delay Resolution
2.5 ns to 10 μs Full-Scale Range
Maximum Trigger Rate 50 MHz
MIL-STD-883-Compliant Versions Available

APPLICATIONS
Disk Drive Deskewing
Data Communications
Test Equipment
Radar I & Q Matching

FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD9501 is a digitally programmable delay generator which provides programmed time delays of an input pulse. Operating from a single +5 V supply, the AD9501 is TTL- or CMOS-compatible, and is capable of providing accurate timing adjustments with resolutions as low as 10 ps. Its accuracy and programmability make it ideal for use in data deskewing and pulse delay applications, as well as clock timing adjustments.

Full-scale delay range is set by the combination of an external resistor and capacitor, and can range from 2.5 ns to 10 μs for a single AD9501. An eight-bit digital word selects a time delay within the full-scale range. When triggered by the rising edge of an input pulse, the output of the AD9501 will be delayed by an amount equal to the selected time delay (t_D) plus an inherent propagation delay (t_{PD}).

The AD9501 is available for a commercial temperature range of 0°C to +70°C in a 20-pin plastic DIP, 20-pin ceramic DIP, and a 20-lead plastic leaded chip carrier (PLCC). Devices fully compliant to MIL-STD-883 are available in ceramic DIPs. Refer to the *Analog Devices Military Products Databook* or current AD9501/883B data sheet for detailed specifications.

AD9501—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage . . . . . +7 V
Digital Input Voltage Range . . . . . −0.5 V to $+V_S$
Trigger/Reset Input Volt. Range . . . . . −0.5 V to $+V_S$
Minimum R_{SET} . . . . . 30 Ω
Digital Output Current (Sourcing) . . . . . 10 mA
Digital Output Current (Sinking) . . . . . 50 mA

Operating Temperature Range
AD9501JN/JP/JQ . . . . . 0°C to +70°C
AD9501SQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[2] . . . . . +175°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS

[$+V_S = +5$ V; C_{EXT} = Open; $R_{SET} = 3090$ Ω (Full-scale range = 100 ns); Pin 8 grounded; and device output connected to Pin 4 RESET input unless otherwise noted]

Parameter	Temp	Test Level	0°C to +70°C AD9501JN/JP/JQ Min	Typ	Max	−55°C to +125°C AD9501SQ Min	Typ	Max	Units
RESOLUTION			8			8			Bits
ACCURACY									
Differential Nonlinearity	+25°C	I			0.5			0.5	LSB
Integral Nonlinearity	+25°C	I			1			1	LSB
Monotonicity	+25°C	I		Guaranteed			Guaranteed		
DIGITAL INPUTS									
Latch Input "1" Voltage	Full	VI	2.0			2.3			V
Latch Input "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Voltage	Full	VI	2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			60			60	μA
Logic "0" Current	Full	VI			3			3	μA
Digital Input Capacitance	+25°C	IV			5.5			5.5	pF
Data Setup Time (t_S)[3]	+25°C	V		2.5			2.5		ns
Data Hold Time (t_H)[4]	+25°C	V		2.5			2.5		ns
Latch Pulse Width (t_L)	+25°C	V		3.5			3.5		ns
Reset/Trigger Pulse Width (t_R, t_T)	+25°C	V		2			2		ns
DYNAMIC PERFORMANCE									
Maximum Trigger Rate[5]	+25°C	IV	18	22		18	22		MHz
Minimum Propagation Delay (t_{PD})[6]	+25°C	I		25	30		25	30	ns
Propagation Delay Tempco[7]	Full	V		25			25		ps/°C
Full-Scale Range Tempco	Full	V		36			36		ps/°C
Delay Uncertainty	+25°C	V		53			53		ps
Reset Propagation Delay (t_{RD})[8]	+25°C	I		14.5	17.5		14.5	17.5	ns
Reset-to-Trigger Holdoff (t_{THO})[9]	+25°C	V		4.5			4.5		ns
Trigger-to-Reset Holdoff (t_{RHO})[10]	+25°C	V		19			19		ns
Minimum Output Pulse Width[11]	+25°C	V		7.5			7.5		ns
Output Rise Time[12]	+25°C	I		2.3	3.5		2.3	3.5	ns
Output Fall Time[12]	+25°C	I		1.0	2.0		1.0	2.0	ns
DAC Settling Time (t_{LD})[13]	+25°C	V		30			30		ns
Linear Ramp Settling Time (t_{LRS})[14]	+25°C	V		20			20		ns
DIGITAL OUTPUT									
Logic "1" Voltage (Source 1 mA)	Full	VI	2.4			2.4			V
Logic "0" Voltage (Sink 4 mA)	Full	VI		0.24	0.4		0.24	0.5	V
POWER SUPPLY[15]									
Positive Supply Current (+5.0 V)	Full	VI		69.5	83		69.5	83	mA
Power Dissipation	Full	VI			415			415	mW
Power Supply Rejection Ratio[16]									
Full-Scale Range Sensitivity	+25°C	I		0.7	2.0		0.7	2.0	ns/V
Minimum Prop Delay Sensitivity	+25°C	I		0.45	1.7		0.45	1.7	ns/V

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: 20-lead plastic leaded chip carrier θ_{JA}=73°C/W; θ_{JC}=29°C/W. 20-pin ceramic DIP θ_{JA}=65°C/W; θ_{JC}=20°C/W. 20-pin plastic DIP θ_{JA}=65°C/W; θ_{JC}=26°C/W.
[3]Digital data inputs must remain stable for the specified time prior to the positive transition of the LATCH signal.
[4]Digital data inputs must remain stable for the specified time after the positive transition of the LATCH signal.
[5]Programmed delay (t_D)=0 ns. Maximum self-resetting trigger rate is limited to 6.9 MHz with 100 ns programmed delay. If t_D=0 ns and external RESET signal is used, maximum trigger rate is 23 MHz.
[6]Programmed delay (t_D)=0 ns. In operation, any programmed delays are in addition to the minimum propagation delay (t_{PD}).
[7]Programmed delay (t_D)=0 ns. [Minimum propagation delay (t_{PD})]
[8]Measured from 50% transition point of the RESET signal input to the 50% transition point of the falling edge of the output.
[9]Minimum time from the falling edge of RESET to the triggering input to insure valid output pulse, using external RESET pulse.
[10]Minimum time from triggering event to rising edge of RESET to insure valid output event, using external RESET pulse. Extends to 125 ns when programmed delay is 100 ns.
[11]When self-resetting with a full-scale programmed delay.
[12]Measured from +0.4 V to +2.4 V; source = 1 mA; sink = 4 mA.
[13]Measured from the data input to the time when the AD9501 becomes 8-bit accurate, after a full-scale change in the program delay data word.
[14]Measured from the RESET input to the time when the AD9501 becomes 8-bit accurate, after a full-scale programmed delay.
[15]Supply voltage should remain stable within ±5% for normal operation.
[16]Measured at $+V_S$ = +5.0 V ±5%; specification shown is for worst case.
Specifications subject to change without notice.

6

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

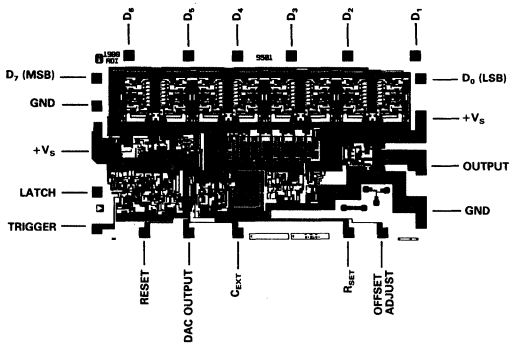
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

ORDERING GUIDE

Device	Temperature	Description	Package Option*
AD9501JN	0°C to +70°C	20-Pin Plastic DIP	N-20
AD9501JP	0°C to +70°C	20-Lead PLCC	P-20A
AD9501JQ	0°C to +70°C	20-Pin Ceramic DIP	Q-20
AD9501SQ	−55°C to +125°C	20-Pin Ceramic DIP	Q-20

*N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

DIE LAYOUT AND MECHANICAL INFORMATION

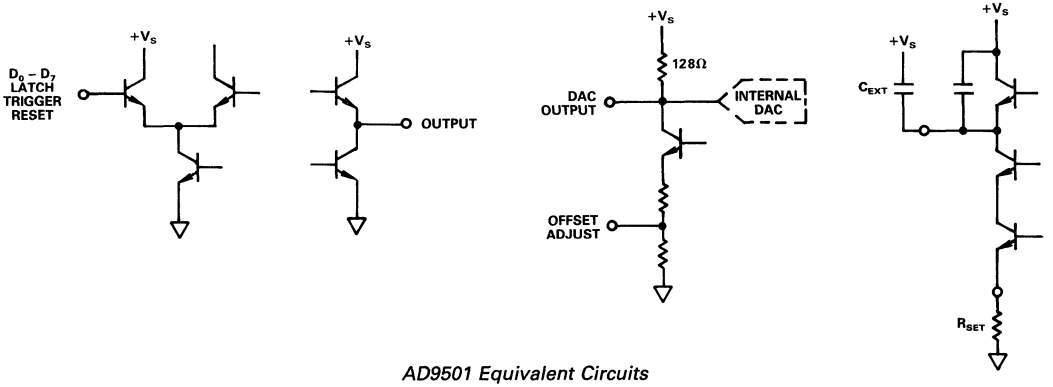


MECHANICAL INFORMATION

Die Dimensions . . . . . .89 × 153 × 15 (±2) mils
Pad Dimensions. . . . . .4 × 4 mils
Metalization. . . . . Aluminum
Backing . . . . . .None
Substrate Potential . . . . . .Ground
Passivation . . . . . .Oxynitride
Die Attach . . . . . .Gold Eutectic
Bond Wire. . . . . 1.25 mil, Aluminum; Ultrasonic Bonding
or 1 mil, Gold; Gold Ball Bonding

AD9501 PIN DESCRIPTIONS

Pin No.	Name	Function
1	$+V_S$	Positive voltage supply; nominally +5 V.
2	LATCH	TTL/CMOS register control line. Logic HIGH latches input data D_0–D_7. Register is transparent for logic LOW.
3	TRIGGER	TTL/CMOS-compatible input. Rising edge triggers the internal ramp generator, and begins the delay cycle.
4	RESET	TTL/CMOS-compatible input. Logic HIGH resets the ramp voltage and OUTPUT.
5	DAC OUTPUT	Output voltage of the internal digital-to-analog converter.
6	C_{EXT}	Optional external capacitor connected to $+V_S$; used with R_{SET} and 8.5 pF internal capacitor to determine full-scale delay range (t_{DFS}).
7	R_{SET}	External resistor to ground, used to determine full-scale delay range (t_{DFS}).
8	OFFSET ADJUST	Normally connected to GROUND. Can be used to adjust minimum propagation delay (t_{PD}); see Theory of Operation text.
9	GROUND	Circuit ground return.
10	OUTPUT	TTL-compatible delayed output pulse.
11	$+V_S$	Positive voltage supply; nominally +5 V.
12–19	D_0–D_7	TTL/CMOS-compatible inputs, used to set the programmed delay of the AD9501 delayed output. D_0 is LSB and D_7 is MSB.
20	GROUND	Circuit ground return.



AD9501 Equivalent Circuits

THEORY OF OPERATION

The AD9501 is a digitally programmable delay device. Its function is to provide a precise incremental delay between input and output, proportional to an 8-bit digital word applied to its delay control port. Incremental delay resolution is 10 ps at the minimum full-scale range of 2.5 ns. Digital delay data inputs, latch, trigger and reset are all TTL/CMOS-compatible. Output is TTL-compatible.

Refer to the block diagram of the AD9501.

Inside the unit, there are three main subcircuits: a linear ramp generator, an 8-bit digital-to-analog converter (DAC) and a voltage comparator. The rising edge of the input (TRIGGER) pulse initiates the delay cycle by triggering the ramp generator. The voltage comparator monitors the ramp voltage and switches the delayed output (Pin 10) HIGH when the ramp voltage crosses the threshold set by the DAC output voltage. The DAC threshold voltage is programmed by the user with digital inputs.

Figure 1, the AD9501 Internal Timing diagram, illustrates in detail how the delay is determined. Minimum Delay (t_{PD}) is the sum of Trigger Circuit delay, Ramp Generator delay, and Comparator delay.

The Trigger Circuit delay and Comparator delay are fixed; Ramp Generator delay is a variable affected by the rate of change of the linear ramp and (to a lesser degree) the value of the offset voltage described below.

Maximum Delay is the sum of Minimum Delay (t_{PD}) and Full-Scale Program Delay (t_{DFS}).

Ramp Generator delay is the time required for the ramp to slew from its reset voltage to the most positive DAC reference voltage (00_H). The difference in these two voltages is nominally 18 mV (with OFFSET ADJUST open) or 34 mV (OFFSET ADJUST grounded).

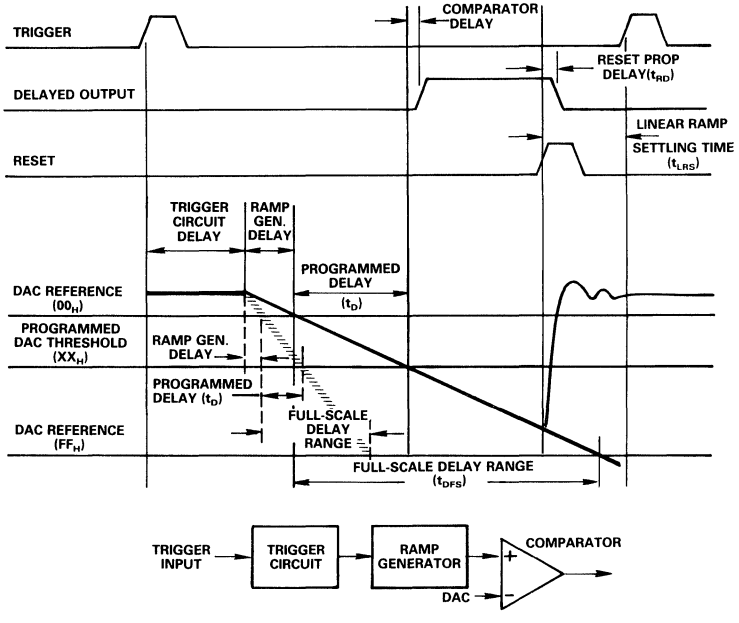


Figure 1. AD9501 Internal Timing

Offset between the two levels is necessary for three reasons. First, offset allows the ramp to reset and settle without re-entering the voltage range of the DAC. Second, the DAC may overshoot as it switches to its most positive value (00_H); this could lead to false output pulses if there were no offset between the ramp reset voltage and the upper reference. Overshoot on the ramp could also lead to false outputs without the offset. Finally, the ramp is slightly nonlinear for a short interval when it is first started; the offset shifts the most positive DAC level below this nonlinear region and maintains ramp linearity for short programmed delay settings.

Pin 8 of the AD9501 is called OFFSET ADJUST (see block diagram) and allows the user to control the amount of offset separating the initial ramp voltage and the most positive DAC reference. This, in turn, causes the Ramp Generator delay to vary.

Figure 2 shows differences in timing which occur if OFFSET ADJUST Pin 8 is grounded or open. The variable Ramp Generator delay is the major component of the three components which comprise Minimum Delay (t_{PD}) and, therefore, is affected by the connection to Pin 8.

It is preferable to ground Pin 8 because the smaller offset that results from leaving it open increases the possibility of false output pulses. When grounding the pin, it should be grounded directly or connected to ground through a resistor or potentiometer with a value of 10 kΩ or less.

Caution is urged when using resistance in series with Pin 8. The possibility of false output pulses, as discussed above, is increased under these circumstances. Using resistance in series with Pin 8 is recommended only when matching minimum delays between two or more AD9501 devices; it is not recommended if using a single AD9501. Changing the resistance between Pin 8 and ground from zero to 10 kΩ varies the Ramp Generator Delay by approximately 35%.

The Full-Scale Delay Range (t_{DFS}) can be calculated from the equation:

$$(t_{DFS}) = R_{SET} \times (C_{EXT} + 8.5\ pF) \times 3.84$$

Whenever Full-Scale Delay Range is 326 ns or less, C_{EXT} should be left open. Additional capacitance and/or larger values of R_{SET} increase the Linear Ramp Settling Time, which reduces the maximum trigger rate. When delays longer than 326 ns are required, up to 500 pF can be connected from C_{EXT} to $+V_S$. R_{SET} should be selected in the range from 50 Ω to 10 kΩ. Graph 1 shows typical Full-Scale Delay Ranges for various values of R_{SET} and C_{EXT}.

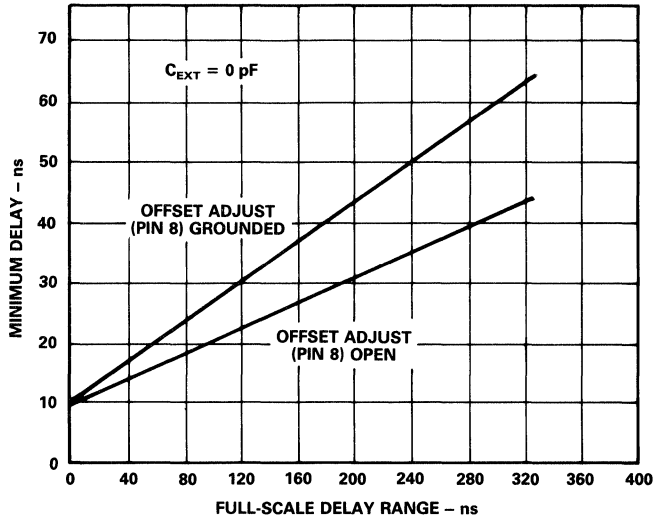
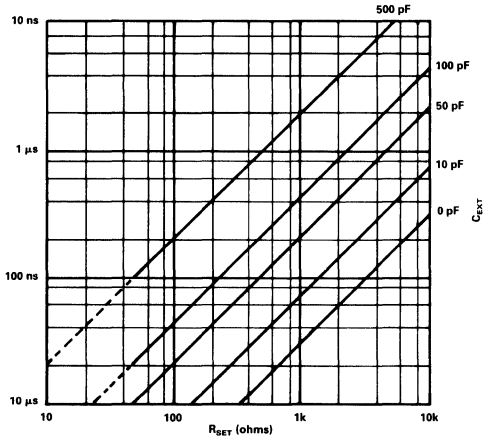


Figure 2. AD9501 Minimum Delay (t_{PD}) vs. Full-Scale Delay Range (t_{DFS})

Ramp charging current and DAC full-scale current are slaved together in the AD9501 to minimize delay drift over temperature. To preserve the unit's low drift performance, both R_{SET} and C_{EXT} should have low temperature coefficients. Resistors which are used should be 1% metal film types.

The programmed delay (t_D) is set by the DAC inputs, D_0–D_7.



Graph 1. RC Values vs. Full-Scale Delay Range (t_{DFS})

The minimum delay through the AD9501 corresponds to an input code of 00_H, and FF_H gives the full-scale delay. Any programmed delay can be approximated by:

$$t_D = (DAC\ code/256) \times t_{DFS}$$

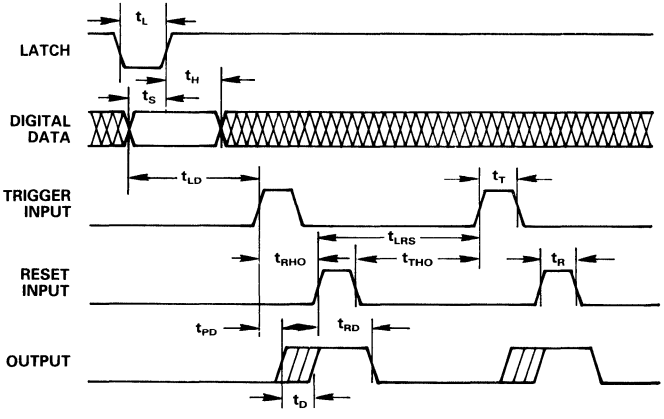
Total delay through the AD9501 for any given DAC code is equal to:

$$t_{TOTAL} = t_D + t_{PD}$$

As shown on the block diagram, TTL/CMOS latches are included to store the digital delay data. Data is latched when LATCH is HIGH. When LATCH is LOW, the latches are transparent, and the DAC will attempt to follow any changes on inputs D_0–D_7.

The System Timing Diagram, Figure 3, shows the timing relationship between the input data and the latch. The DAC settling time (t_{LD}) is approximately 30 ns. After the digital (Programmed Delay) data is updated, a minimum 30 ns must elapse between the time LATCH goes high and the arrival of a TRIGGER pulse to assure rated pulse delay accuracy.

When RESET goes HIGH, the ramp timing capacitor (C_{EXT} + 8.5 pF) is discharged. The RESET input is level-sensitive, and overrides the TRIGGER input. Therefore, any trigger pulse which occurs when RESET is HIGH will not produce an output pulse. As shown on the system timing diagram, Figure 3, the next trigger pulse should not occur before the Linear Ramp Settling Time (t_{LRS}) interval is completed to assure rated pulse delay accuracy.



NOTE: A TRIGGERING EVENT MAY OCCUR AT ANY TIME THE INTERNAL DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

t_L	– LATCH PULSE WIDTH	t_{RHO}	– TRIGGER-TO-RESET HOLD-OFF
t_H	– DIGITAL HOLD TIME	t_{THO}	– RESET-TO-TRIGGER HOLD-OFF
t_S	– DIGITAL DATA SETUP TIME	t_R	– RESET PULSE WIDTH
t_{LD}	– DAC SETTLING TIME	t_{PD}	– MINIMUM PROPAGATION DELAY
t_T	– TRIGGER PULSE WIDTH	t_{RD}	– RESET PROPAGATION DELAY
t_{LRS}	– LINEAR RAMP SETTLING TIME	t_D	– PROGRAMMED DELAY

Figure 3. AD9501 System Timing

For most applications, OUTPUT can be tied to RESET. This causes the output pulse to be narrow (equal to the Reset Propagation Delay t_{RD}). Alternatively, an external pulse can be applied to RESET. To assure a valid output pulse, however, the delay between TRIGGER and RESET should be equal to or greater than the total delay of t_{PD} + t_D illustrated in the internal timing diagram Figure 1.

As shown in that figure, the capacitor voltage discharges very rapidly and includes a small amount of overshoot and ringing. Rated timing delay will not be realized unless subsequent trigger events are delayed until after the linear ramp settles to its reset voltage value.

The values for the various delay increments in the specification table are based on a Full-Scale Delay Range of 100 ns with OUTPUT tied to RESET (self-resetting operation).

When Full-Scale Delay Range is set for intervals shorter than 100 ns, the rate of change of the linear ramp is increased. This faster rate means the Maximum Trigger Rate shown in the specification table is increased because the Ramp Generator Delay and, consequently, Minimum Propagation Delay t_{PD} become smaller.

Linear Ramp Settling Time t_{LRS} also becomes shorter as Full-Scale Delay Range is decreased. Minimum Delays for various Full-Scale Delay Range values are shown in Figure 2.

APPLICATIONS

The AD9501 is useful in a wide variety of precision timing applications because of its ability to delay TTL/CMOS pulse edges by increments as small as 10 ps.

In Figure 4, the AD9501 typical circuit configuration, the delayed output is tied back to the RESET input. This will produce a narrow output pulse whose leading edge is delayed by an amount proportional to the 8-bit digital word stored in the on-board latches. For the configuration shown, the output pulse width will be equal to the Reset Propagation Delay (t_{RD}). If wider pulses are required, a delay can be inserted between OUTPUT and RESET. If preferred, an external pulse can be used as a reset input to control the timing of the falling edge (and consequently, the width) of the delayed output.

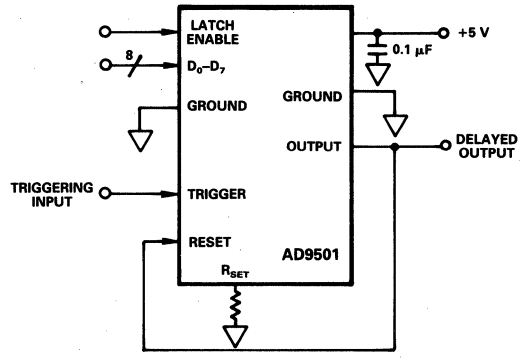


Figure 4. AD9501 Typical Circuit Configuration

Multiple Signal Path Deskewing

High speed electronic systems with parallel signal paths require that close delay matching be maintained. If delay mismatch (time skew) occurs, errors can occur during data transfer. For these situations, the matching of delays is generally accomplished by carefully matching lead lengths.

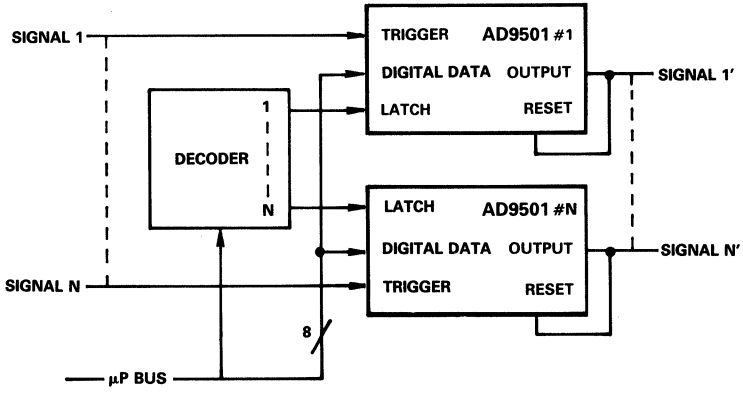


Figure 5. Multiple Signal Path Deskewing

This delay matching is often difficult when using high speed, high-pin-count testers because lead length and circuit impedance can change when the tester setup is changed for different types of devices. The skew which might result from these changes can be compensated by using AD9501 units as shown in Figure 5.

When deskewing multiple signal paths, a single stimulus pulse is applied to all inputs of the AD9501s which are used. The delay for each signal path is then measured by the tester's delay measurement circuit. Using a closed loop technique, all delays are equalized by changing the digital value held in the register of each AD9501. Once all delays have been matched to the desired tolerance, the calibration loop is opened; and the tester is ready to test the new type of device.

Digitally Programmable Oscillator

Two AD9501s can be configured as an astable oscillator, as shown in Figure 6.

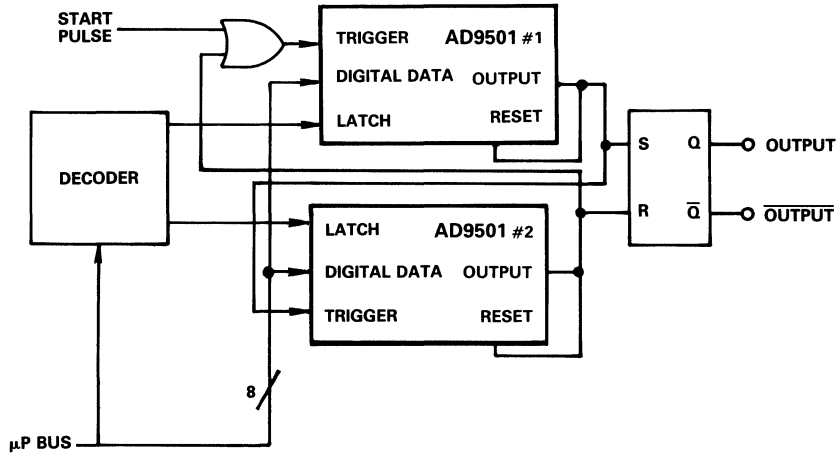


Figure 6. Digitally Programmable Oscillator

Delay through each side of the oscillator is determined by the programmed delay (t_D) of each AD9501 plus the minimum propagation delay (t_{PD}) of each. Increasing the digital value applied to either AD9501 decreases frequency, just as increasing RC decreases frequency in an analog ring oscillator.

Using a pair of AD9501 Delay Generators as shown allows the user great flexibility because both the frequency and the duty cycle of the oscillator are easily controlled.

Frequency of the oscillator output can be established with the equation:

$$f = 1/(2t_{PD} + t_{D1} + t_{D2})$$

when t_{D1} and t_{D2} are the programmed delays of AD9501 #1 and AD9502 #2, respectively.

Programmable Pulse Generator

In this application, shown in Figure 7, two AD9501 units are triggered from a common clock signal. Their outputs go to the inputs of an RS flip-flop. A digital delay value is applied as an input to each with AD9501 #2 typically having a larger value than AD9501 #1.

As shown by the timing portion of the diagram, changing the delay value from one clock cycle to the next generates a pseudo-random pulse whose leading and trailing edge delays are controlled relative to Clock In. The dashed lines illustrate how the programmed delays of the AD9501 components control both the timing and width of the generator output.

The frequency (f) and pulse width (t_{pw}) of the pulse generator can be determined as follows:

$$f = f_{CLOCK\ IN}$$

and:

$$t_{pw} = t_{TOT2} - t_{TOT1}$$

with T_{TOT} being equal to each AD9501's minimum propagation delay (t_{PD}) plus programmed delay (t_D). If both AD9501s are set for the same full-scale delay range, their minimum propagation delays will be approximately the same, and the pulse width will be approximately equal to the difference in programmed delays.

Digital Delay Detector

An unknown digital delay can be measured by applying a repetitive clock to the circuit shown in Figure 8.

The pictured delay detector works in a manner similar to a successive approximation ADC; in this circuit, however, a D-type flip-flop replaces the ADC's voltage comparator.

To calibrate the circuit, short out the unknown delay and apply the clock input to both AD9501 units.

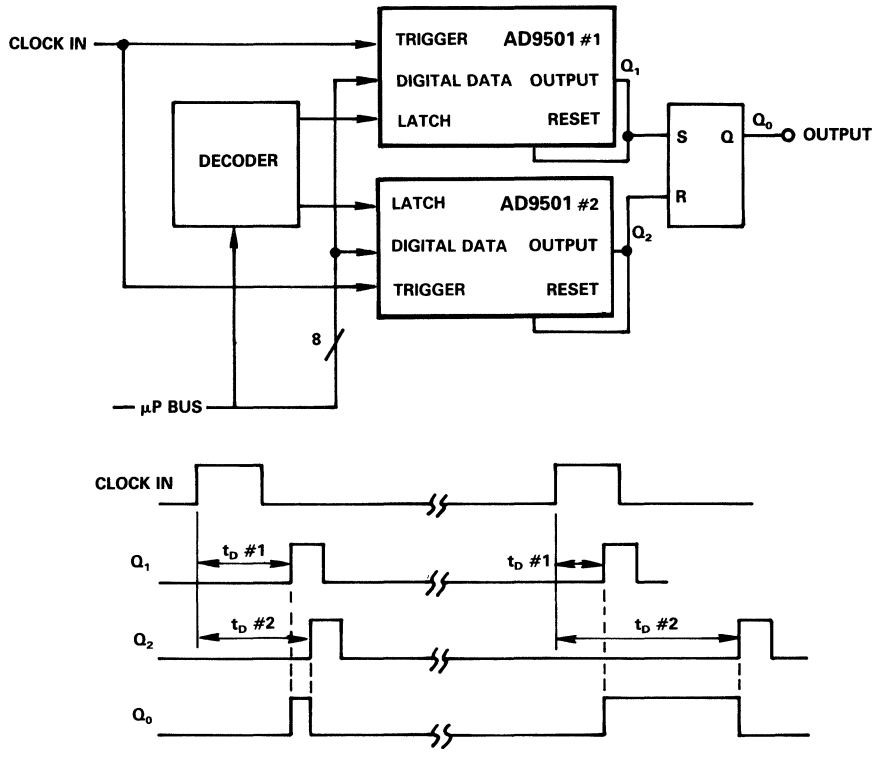


Figure 7. Programmable Pulse Delay Generator

AD9501 #1 should be programmed so its delay is greater than the zero-set programmed delay of AD9501 #2. To accomplish this, continue to apply clock pulses and increment the digital data into AD9501 #1 until the output of the successive approximation register (SAR) is 02H (00000010) or greater. At this point, the delay through AD9501 #1 is slightly longer than the delay through AD9501 #2, making it possible to use the SAR output as the zero reference point for measuring the unknown delay when it is reinserted into the circuit.

This calibration procedure compensates for the setup time of the flip-flop, stray circuit delays and other nonideal characteristics which are an inherent part of any circuit.

Eight cycles of the clock input are required to determine the value of the unknown delay.

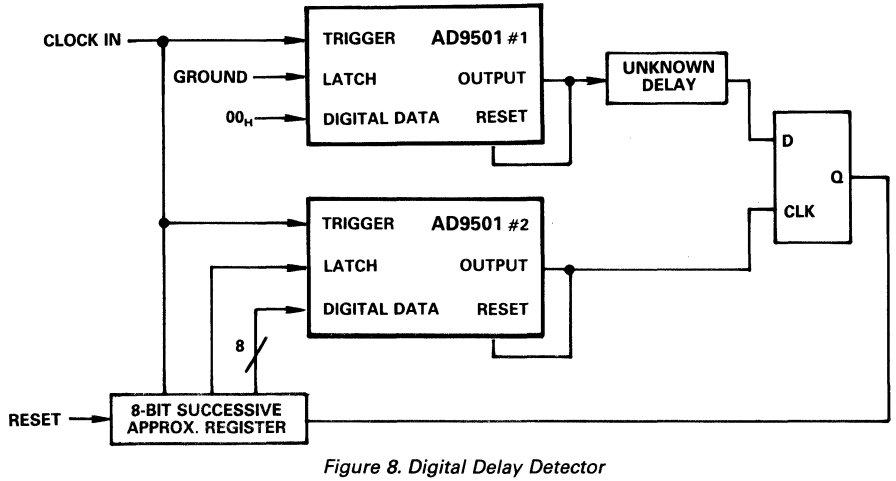


Figure 8. Digital Delay Detector

Analog Settling Time Measurement

This circuit, shown in Figure 9, functions in a manner similar to the digital delay detector; for this application, too, the clock must be repetitive. As in the delay detector, AD9501 #1 is used to cancel the propagation delay of AD9501 #2, propagation delay of the comparators, stray delays, etc. To accomplish this, use the calibration procedure described earlier for the digital delay generator.

The difference betwen the two circuits is in the detection method. The register of the digital delay is replaced by a window comparator for the analog settling measurement.

Threshold voltages V1 and V2 are set for the desired tolerance around the final value of the DUT output signal. As shown in the lower portion of the diagram, the output of the detector is high when the analog output signal of the converter is within the limits set by V_1 and V_2.

Therefore, the settling time can be measured by starting the delay of AD9501 #2 at its maximum setting and decrementing it until the window comparator goes low. The difference between the DAC codes applied to AD9501 #2 and AD9501 #1 is a measure of the settling time of the D/A converter being tested.

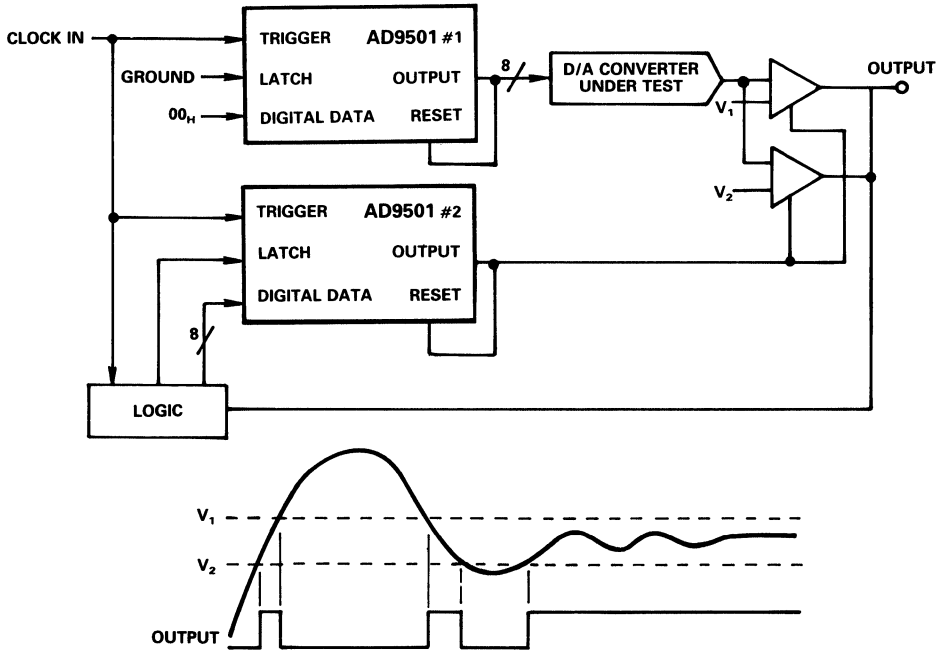


Figure 9. Analog Settling Time Measurement

Layout Considerations

Although the inputs and output of the AD9501 are digital, the delay is determined by analog circuits. This makes it critical to use high speed analog circuit layout techniques to achieve rated performance.

The ground plane should be on the component side of the board and extend under the AD9501 to shield it from digital switching signals. Most socket assemblies add significant inter-lead capacitance, and should be avoided whenever possible. If sockets must be used, individual pin sockets such as AMP part number 6-330808-0 (closed knock-out end) or 6-330808-3 (open end) should be used.

Power supply decoupling is also critical for high speed design; a 0.1 μF capacitor should be connected as close as possible to each supply pin.

ANALOG DEVICES

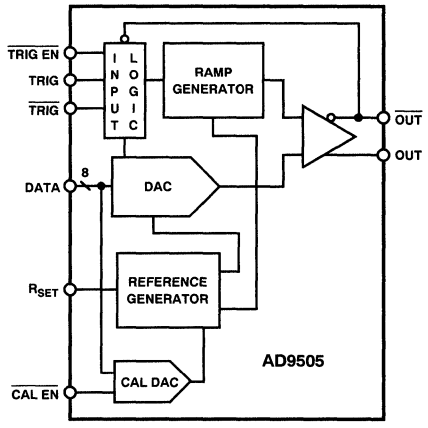
Digitally Programmable Pulse Edge Delay Vernier

AD9505

FEATURES
60 MHz Update Rate
±1.5 LSB Dynamic Nonlinearity
100 MHz Update Rate
±5 LSB Dynamic Nonlinearity
On-the-Fly Delay Update
8-Bit Resolution
2.5 ns to 25 ns Full-Scale Range
10 ps Incremental Delay
On-Board Calibration DAC

APPLICATIONS
ATE Pattern Generator
Programmable Pulse Generator
Frequency-Agile Clock Generator
Precise Pulse Phase Delay
Variable Duty Cycle Clock
Laser Printers
High Speed PWM
Line-to-Line Deskew

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9505 is a high performance, digitally programmable timing vernier with "on-the-fly" update capability. The delay from the triggering edge to the output is proportional to the 8-bit delay data.

With the timing capacitor and CalDAC included on the die, external components are reduced and manual trim of full-scale range is not required. A single external resistor sets the nominal full scale, and fine tuning can be accomplished under processor control. Pulse edge placement can be controlled to 10 ps resolution when full scale is set to its minimum value of 2.5 ns.

The AD9505 is designed specifically for applications requiring dynamic delay update such as ATE pulse pattern generation and very high speed, pulse width modulation. A new delay value is latched into the DAC on the positive edge of each TRIGGER pulse. This permits generation of high speed, pseudo-random pulse patterns with edges controlled to very precise increments.

Logic input and output levels are compatible with ECL-10K. TRIGGER and OUTPUT signals are differential to assure maximum noise immunity and minimum jitter when interfacing to any ECL logic family. An ECL midpoint reference is included for single-ended input interface.

Only 650 mW is required from a single −5.2 V power supply. This makes it possible to package the AD9505 in plastic PLCC. As a result, dense PC board layout is made possible. The AD9505KP is rated for operation from 0°C to +70°C.

PRODUCT HIGHLIGHTS

1. On-the-Fly Delay Update
2. Low Power—650 mW
3. Single Power Supply
4. 10K ECL Compatible

6

AD9505–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{EE} = −5.2 V; R_{SET} = 62 Ω; FSR = 4.1 ns; R_L = 100 Ω to −2 V)

Parameter	Temp	Test Level	Min	Typ	Max	Units
RESOLUTION			8			Bits
ACCURACY[1]						
Differential Nonlinearity[2]	+25°C	I		±0.5	±1	LSB
Integral Nonlinearity[2]	+25°C	I		±0.75	±1.75	LSB
Dynamic Integral Nonlinearity[3]	+25°C	V		±1		LSB
	Full	V		±2		LSB
Monotonicity	+25°C	I		Guaranteed		
DIGITAL INPUTS						
Logic "1" Voltage	Full	VI	−1.1			V
Logic "0" Voltage	Full	VI			−1.5	V
Logic "1" Input Current	Full	VI			25	μA
Logic "0" Input Current	Full	VI			25	μA
ECL Midpoint Reference	Full	VI	−1.38		−1.17	V
Input Capacitance	+25°C	V		3		pF
TRIG EN Setup Time (t_{SU})[4]	+25°C	V		1.5		ns
TRIG EN Hold Time (t_H)[5]	+25°C	V		2.5		ns
Data Setup Time (t_{DSU})[6]	+25°C	V		1		ns
Data Hold Time (t_{DH})[6]	+25°C	V		3		ns
Minimum Trigger Pulse Width High	Full	V		2		ns
DIGITAL OUTPUT						
Logic "1" Voltage	Full	IV	−1.0			V
Logic "0" Voltage	Full	IV			−1.63	V
DYNAMIC PERFORMANCE[1]						
Maximum Trigger Rate	+25°C	I	60			MHz
Minimum Propagation Delay (t_{PD})	+25°C					
FSR = 4 ns		I	4		6	ns
FSR = 20 ns		V		7		ns
Minimum Propagation Delay TC	Full	V		6		ps/°C
Full-Scale Range TC	Full	V		1		ps/°C
Delay Uncertainty	+25°C	V		6		ps
Output Rise Time	+25°C	V		900		ps
Output Fall Time	+25°C	V		900		ps
Output Pulse Width	+25°C	I	3.2	3.9	4.6	ns
POWER SUPPLY[7]						
Negative Supply Current (−5.2 V)	Full	VI		125	150	mA
Power Dissipation	Full	VI		650	780	mW
Power Supply Rejection Ratio[8]						
Full-Scale Range Sensitivity	+25°C	I		100	275	ps/V
Minimum Propagation Delay Sensitivity	+25°C	I		50	200	ps/V

NOTES
[1]With full scale set at 4.1 ns and 60 MHz TRIGGER rate.
[2]Measured with delay data changing at a slow rate and trigger at 60 MHz (Best Fit).
[3]Measured with delay changing on each trigger at 60 MHz.
[4]TRIGGER ENABLE must remain stable for the specified time prior to the leading edge of TRIGGER.
[5]TRIGGER ENABLE must remain stable for the specified time after the leading edge of TRIGGER.
[6]The DATA inputs must be stable for the specified times prior to and after the leading edge of TRIGGER.
[7]Supply voltage should remain stable within ±5% for normal operation.
[8]Measured at ±5% of V_{EE}.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Negative Supply Voltage (V_{EE}) . . . . . −7 V
Digital Input Voltage Range . . . . . GND to V_{EE}
Trigger Input Voltage Range . . . . . GND to V_{EE}
Minimum R_{SET} . . . . . 20 Ω
Digital Output Current (Sourcing) . . . . . 30 mA
Operating Temperature Range
AD9505KP . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature[2] . . . . . +175°C
Vapor Phase Soldering (1 minute)[3] . . . . . +220°C

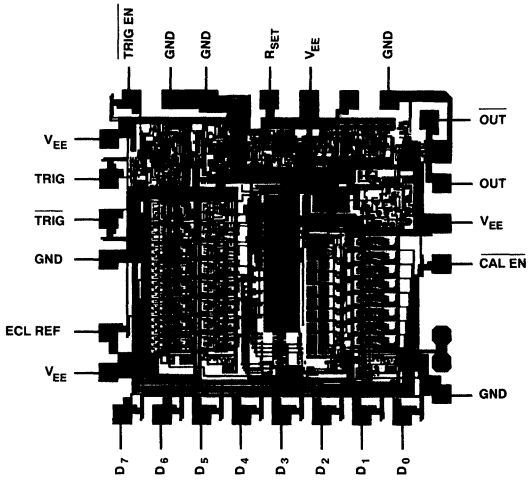
NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability may be impaired. Functional operability under any of these conditions is not necessarily implied.
[2]Typical thermal impedance:
28-Lead PLCC, θ_{JA} = 55°C/W; θ_{JC} = 15°C/W.
[3]Prior to vapor phase soldering, plastic packages should receive a minimum of 8 hours bake-out at 110°C to assure that moisture trapped during shipping and storage is driven out.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9505KP	0°C to +70°C	Plastic PLCC	P-28A

*For outline information see Package Information section.

MECHANICAL INFORMATION

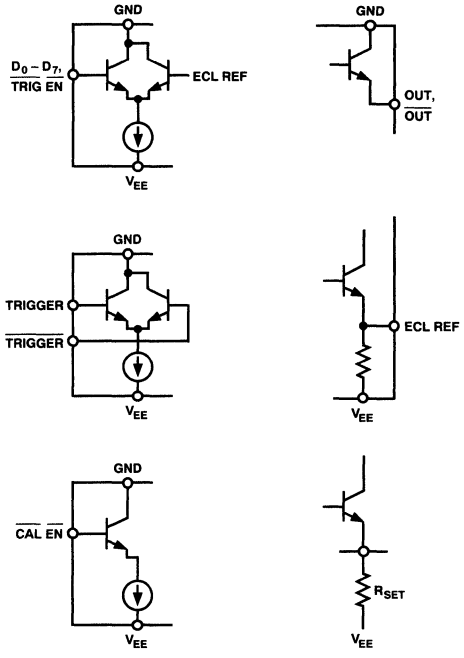


Die Dimensions . . . . . 101 × 97 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Aluminum
Backing . . . . . None
Substrate Potential . . . . . V_{EE}
Passivation . . . . . Oxynitride
Die Attach . . . . . Epoxy or Gold Eutectic
Bond Diameter . . . . 1.25 mil, Aluminum; Ultrasonic Bonding
. . . . . or 1 mil, Gold; Gold Ball Bonding

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Periodically sample tested.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



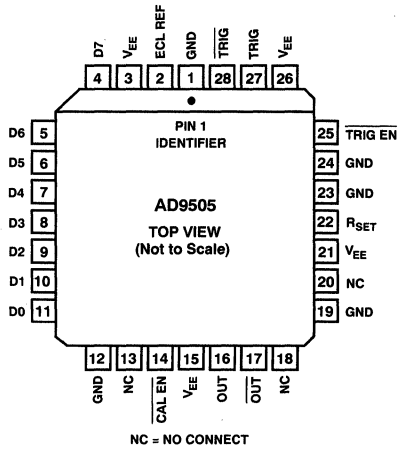
Equivalent Circuits

PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	GND	Ground Return; Digital Current.
2	ECL REF	Logic Midpoint Reference.
3	V_{EE}	Negative Supply; −5.2 V, Digital.
4	D7	Delay Data Bit 7 (MSB).
5	D6	Delay Data Bit 6.
6	D5	Delay Data Bit 5.
7	D4	Delay Data Bit 4.
8	D3	Delay Data Bit 3.
9	D2	Delay Data Bit 2.
10	D1	Delay Data Bit 1.
11	D0	Delay Data Bit 0 (LSB).
12	GND	Ground Return; Digital Current.
13	N/C	No Connection: Do Not Use as a Tie Point.
14	$\overline{\text{CAL EN}}$	Calibrate Enable; Cal Is Initiated When Logic "Zero" Applied.
15	V_{EE}	Negative Supply; −5.2 V, Digital.
16	OUT	True Output Signal.
17	$\overline{\text{OUT}}$	Complementary Output.
18	NC	No Connection; Do Not Use as a Tie Point.
19	GND	Ground Return; Digital Current.
20	NC	No Connection; Do Not Use as a Tie Point.
21	V_{EE}	Negative Supply; −5.2 V, Analog.
22	R_{SET}	Resistor to Set Nominal Full Scale.
23	GND	Ground Return; Analog Current.
24	GND	Ground Return; Analog Current.
25	$\overline{\text{TRIG EN}}$	Trigger Enable; Enabled When Logic "Zero" Applied.
26	V_{EE}	Negative Supply, −5.2 V, Digital.
27	TRIG	Trigger Input; Initiates Delay.
28	$\overline{\text{TRIG}}$	Complementary Trigger Input.

PIN CONFIGURATION

28-Lead PLCC



FUNCTIONAL DESCRIPTION

The AD9505 comprises a ramp generator, DAC, and comparator. A TRIGGER signal initiates a linear ramp and latches data into the DAC. The comparator monitors the ramp signal versus the DAC reference level. When the ramp crosses the level set by the DAC, an OUTPUT signal of constant pulse width is generated.

The comparator also generates an internal signal which resets the ramp and returns the DAC latch to its transparent state. The DAC then switches and settles to the voltage corresponding to its next data word. It is then ready for the next triggering event.

TIMING CONSIDERATIONS

As shown in the timing diagram below, the leading edge of TRIGGER initiates a delay cycle whenever $\overline{\text{TRIGGER ENABLE}}$ is a logic zero. Minimum setup and hold times must be observed to assure that DATA is properly latched into the DAC and the TRIGGER is enabled.

For "on-the-fly" operation, the DATA setup time should be a minimum of 5 ns. This is necessary to assure minimum settling time for the DAC. The DAC latches become transparent immediately following the previous delayed event. Figure 1 demonstrates typical nonlinearity versus update rate with new DATA for each TRIGGER (FSR = 4 ns).

Some applications for delay verniers do not require the delay value to change on a TRIGGER-by-TRIGGER basis. In cases where delay DATA changes relatively slowly, dynamic linearity will improve markedly. An octal holding register may be required since the AD9505 data inputs are latches rather than registers. Figure 2 shows nonlinearity versus TRIGGER rate with DATA update at 100 Hz (FSR = 4 ns).

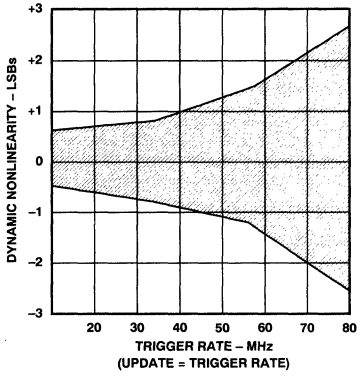


Figure 1. Dynamic Nonlinearity vs. Update Rate

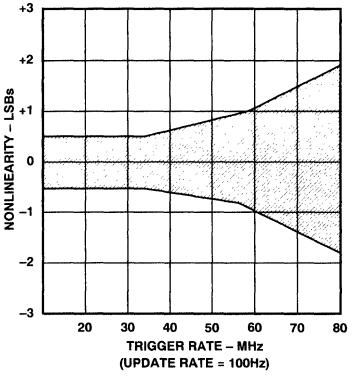


Figure 2. Nonlinearity vs. Trigger Rate

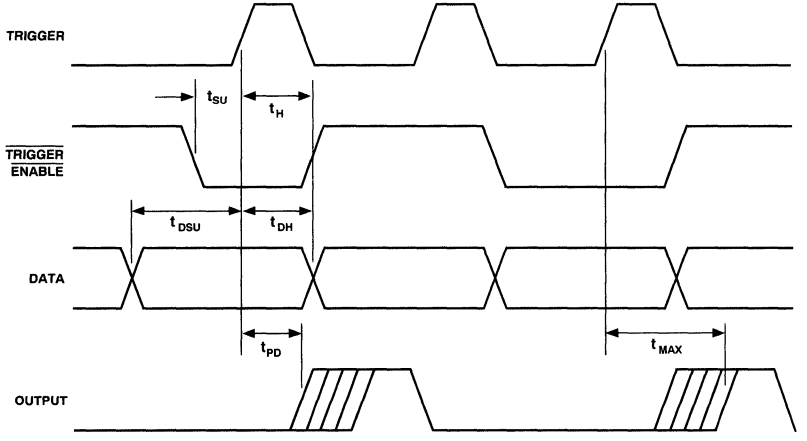


Figure 3. Timing Diagram

Because of timing overhead such as setup times, minimum propagation delay, and ramp/DAC settling time, it is not possible for the programmed delay to be as long as the full TRIGGER interval. The table below lists maximum full-scale ranges for various trigger rates to maintain rated linearity.

Trigger Rate	Trigger Interval	Maximum FSR
60 MHz	16.7 ns	5 ns
50 MHz	20 ns	11 ns
25 MHz	40 ns	15 ns

Figure 4 illustrates dynamic nonlinearity versus full-scale range for 20 MHz, 60 MHz, and 100 MHz TRIGGER rates.

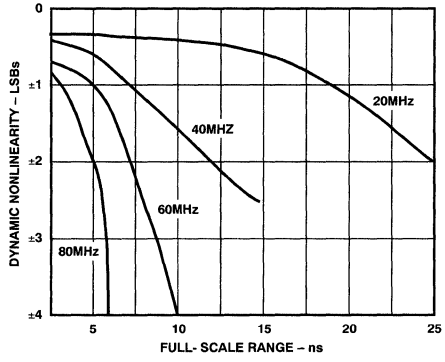


Figure 4. Dynamic Nonlinearity vs. FSR

The AD9505 outputs a constant width pulse whose leading edge is delayed with respect to the leading edge of TRIGGER. Total delay is the sum of a minimum delay and the programmed delay or:

$$t_{TOTAL} = t_{PD} + t_{PROG}$$

Minimum delay (t_{PD}) consists of the fixed propagation delay of the input logic and the comparator plus a variable ramp delay. The ramp delay is due to an offset between the reset ramp level and the most positive DAC value. This offset is necessary to avoid false output signals when the ramp resets. The offset is constant, but the delay varies as a function of the slope of the ramp. Thus, this portion of t_{PD} will be proportional to the full-scale range.

Minimum delay can be calculated by the equation:

$$t_{PD} = 4.7\ ns + (0.1 \times FSR)$$

Minimum delays for various full-scale delays are shown in Figure 5.

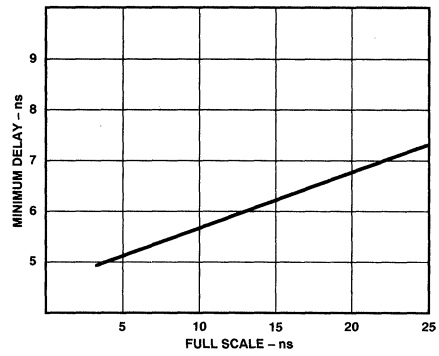


Figure 5. Minimum Delay

Full-scale programmable range is set by an external R_{SET} in combination with an internal capacitor with a nominal value of 14 pF. Full-scale range is found by the equation:

$$FSR = 4.7 \cdot R_{SET} \cdot C_{INT}$$

or R_{SET} is found by:

$$R_{SET} = FSR/(65.8 \cdot 10^{-12})$$

For best overall performance, the full-scale range for the AD9505 should be limited to the range from 2.5 ns to 25 ns. It should be noted that data sheet specifications are based on a full-scale range of 4.1 ns. Figure 6 shows the required value for R_{SET} for various nominal full-scale ranges.

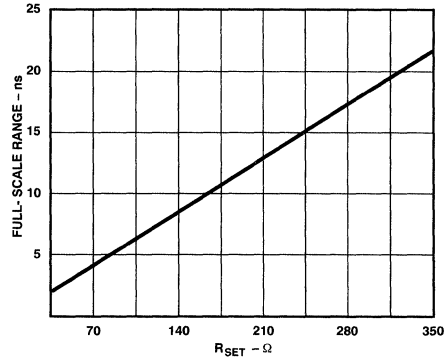


Figure 6. Full Scale vs. R_{SET}

Although operation at longer delay ranges is possible, certain characteristics may degrade to undesirable levels. The first characteristic to degrade will be FSR tempco. The reference circuit which regulates this tempco is effective over the R_{SET} range from 35 Ω to 350 Ω. Further imbalance in this circuit causes rapid degradation of tempco.

Additionally, the jitter (which is actually a measure of timing repeatability) increases rapidly. Since the purpose of the AD9505 is to provide repeatable delay with fine incremental resolution, jitter is undesirable. Typical jitter versus full-scale delay is illustrated below. Data for Figure 7 was taken with the AD9505 operating at low data update..

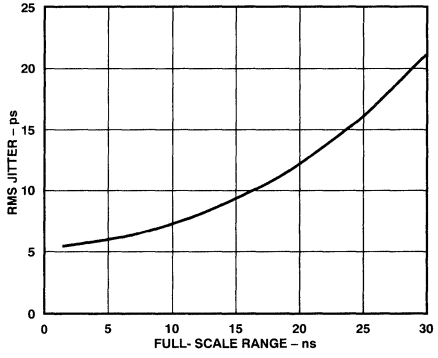


Figure 7. Jitter vs. FSR

The tolerance on the internal capacitor is approximately ±20%. Thus, the full-scale range calculated by the above equations will have a like tolerance. Because many applications for timing verniers require better absolute range tolerance as well as tight matching between multiple devices, the AD9505 also includes an on-board CalDAC. This facilitates fine tuning the FSR under processor control.

APPLICATIONS INFORMATION

Fine-Tuning FSR with the CalDAC

Data for the CalDAC is applied to the same 8-bit bus as delay DATA. When CAL Enable is low, data is loaded into the CalDAC; when it goes high, the data is latched. (It should be noted that this data is also loaded into the delay DATA latches. Therefore, a new delay value should be loaded prior to testing the new calibration value or returning to normal operation.)

Since the capacitor may vary by ±20%, the CalDAC's range is proportional to FSR so it is always slightly more than ±20%. Additionally, it is guaranteed monotonic by design so it will operate properly in a closed correction loop. The effective resolution of the calibration is ±1/4 LSB referred to the full-scale range.

R_{SET} is selected per the equations under Timing Considerations. Starting with a midscale code in the CalDAC, its input should be increased to lengthen FSR and vice versa.

As long as CAL ENABLE is held high, the CalDAC will retain its calibration code until another calibration cycle is initiated. The user should note that the calibration code is lost when power is removed. The CalDAC latch may come up in any state. Therefore, a power-up cal should always be performed.

Layout Considerations

Although the AD9505 performs an essentially digital function, its incremental resolution and accuracy depend upon linear analog subcircuits. The internal comparator measures millivolt levels in order to resolve very small time increments. Therefore, high frequency analog layout techniques should be employed in order to obtain rated performance.

Driving the device with a differential signal will enhance the repeatability of the timing accuracy. The complementary outputs should also be loaded equally to balance output digital switching currents.

Grounding and power supply decoupling should receive special attention. The ground plane should cover as much as possible of the component side or first interior layer of the board. Avoid signal runs on the component side of the board between the device and ground plane.

All ground pins should be connected directly to the ground plane. In systems with split grounds, all ground pins of the AD9505 should be connected to the Analog Ground. A single point connection from the ground plane of the AD9505 to digital ground is required for return currents for the digital interface.

All V_{EE} pins should be decoupled with 0.01 μF to 0.1 μF chip capacitors. Circuit connections from the capacitors to package pins and ground should be as short as possible to minimize inductance.

The analog V_{EE}, Pin 21, should require no special treatment except on boards with considerable digital switching current. In those cases, a ferrite bead in series with the supply connection should provide satisfactory isolation. Otherwise, normal decoupling should be adequate.

In most cases, sockets should be avoided, even for prototyping. The contacts in sockets add capacitance and inductance which usually degrade dynamic performance of high performance ICs such as the AD9505. If socketing is necessary, and the user can tolerate small losses in performance, the best-known socket through our experience is the Methode 213-028-602 for the PLCC.

An evaluation board is available. Its part number is AD9505PCB.

Special Function Components
Contents

Selection Guide
Special Function Components

Model	Description	Package Options[1]	Temp Range[2]	Page
AD639	Universal Trigonometric Function Converter	1	I, M	7-5
PKD-01	**Monolithic Peak Detector with Reset-and-Hold Mode**	**2, 3**	**C, M**	**7-33**
***ADXL-50**	**Monolithic Accelerometer with Signal Conditioning**	**1, 7**	**M**	**7-27, 11-10**
***AD730**	**Programmable Clock Generator**	**6**	**C**	**7-13**
***AD720**	**RGB to NTSC/PAL Encoder**	**5**	**C**	**7-9**
***AD800/802**	**Clock Recovery and Data Retiming Phase Locked Loop**	**1, 2, 6**	**C, I**	**7-19**
***AD805**	**Clock Recovery and Data Retiming Phase Locked Loop**	**1, 6**	**C, I**	**7-23**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product.

This section contains technical data on integrated circuit chips that could not be classified in any of the major sections of this databook without losing their identities. For example, the AD639 trigonometric function generator is a close relative of analog multiplier/dividers, in both function and circuitry; but if it were listed in that section, its unique trigonometric capabilities would be "buried."

We describe briefly here the function and salient uses of these devices. For further information, consult the individual data sheets.

ANALOG FUNCTIONS

AD639 Universal Trigonometric Function Generator

The AD639 is an analog "trigonometric microsystem" on a single silicon chip, packaged in a 16-pin DIP. From a differential input voltage, representing an angle (20 mV/°), it can be programmed to generate a voltage output, accurately determined by any of the standards functions—sine, cosine, tangent, secant, cosecant, and contangent—as well as some lesser known variants, such as the versine and exsecant, plus a corresponding set of inverse functions. All inputs are differential, and either polarity of input or output can be generated.

Trigonometric functions play an important role in electronics. Inherent to many communications, measurement and display systems, they also find increasing application in control and robotics. Most familiar are the *sine* and *cosine*, which find wide use as fundamental signal source—both separately and in orthogonal pairs. In display systems, these functions are basic to graphical manipulations (axis rotation and polar-to-Cartesian conversion), and they also appear in Cartesian-to-polar conversion and in determining phase angle from the real and imaginary components of a complex signal.

With its large repertoire of functions, the AD639 makes it possible to include trigonometric transformations in the analog portion of a system with:

- little added cost or board space
- with high accuracy
- without the overhead in software, memory or time (which would accompany such computations in an associated digital system). The use of the AD639 also makes it easy to generate low distortion sine-wave signals, with voltage control of amplitude and frequency, up to 10 V and 1 MHz, respectively.

AD720 RGB to NTSC/PAL Encoder

The AD720 RGB to NTSC/PAL Encoder converts red, green, and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance (subcarrier amplitude and phase) signals in accordance with either NTSC or PAL standards. These two outputs are also combined to provide a composite video output. All three outputs are available separately at voltages of twice the standard signal levels as required for driving 75 Ω reverse-terminated cables.

AD730—Programmable Clock Generator

The AD730 is a monolithic solution for providing up to 16 output frequencies from a single frequency source. Output frequencies of up to 216 MHz are realizable, combined with excellent jitter performance. The available output frequencies are determined through a "Personalization Mask Option." An output frequency is selected through a standard MPU interface. Low jitter and excellent power supply rejection are achieved by careful attention to layout and the use of an active integrator in the loop filter. The only external components required are a reference crystal and three passive components for the PLL loop filter.

AD800 and AD802 Clock Recovery and Data Retiming Circuits

These phase-locked loop based circuits have been designed for use in high data rate (≥20 Mbps, NRZ) receiver circuits, in particular those adhering to telecommunications standards for fiber optic receivers.

These circuits contain two control loops: a frequency acquisition loop and a phase acquisition loop. The frequency acquisition loop acquires the clock frequency of the input data signal. The phase acquisition loop tracks the phase of the input data signal. The AD800/AD802 has wide capture and tracking ranges. This, coupled with the factory's ability to laser trim VCO center frequency, eliminates the need to rely on external components (crystal, VCXO, or precision network) for center frequency setting for operation over temperature.

An external capacitor controls the loop damping factor of an AD800/AD802. The user can design the circuit with a loop damping factor between 1 and 10. The loop damping factor controls the tradeoff between frequency acquisition and jitter peaking. A lower damping factor decreases frequency acquisition time at the expense of greater jitter peaking.

A mask set determines the loop bandwidth of an AD800/AD802 (between 0.01% and 1% of nominal center frequency). A very low loop bandwidth circuit (0.01% of the nominal center frequency) could effectively filter a jittery timing reference.

The factory can develop an AD800 for NRZ bit rates from 20 Mbps to 70 Mbps, and an AD802 for NRZ bit rates from 90 Mbps to 160 Mbps. The factory offers products for standard bit rates (e.g., CCITT Recommendation G.958: Synchronous Digital Hiearchy STM1 155.52 Mbps).

AD805 Clock Recovery and Data Retiming Circuit

This phase-locked loop based circuit has been designed for use in high data rate (155.52 Mbps, NRZ) receiver and transmitter circuits, in particular those adhering to telecommunications standards for fiber optic transmission (e.g., CCITT Recommendation G.958: Synchronous Digital Hiearchy STM1 155.52 Mbps).

An AD805 works with a 155.52 MHz VCXO to provide fast acquisition (40 bit periods) clock recovery and data retiming. This circuit has wideband jitter tolerance, and no jitter peaking, in addition to fast acquisition. The VCXO provides a clock output when no input data transitions are present. This circuit can be used to multiply a 19.44 MHz or 25.92 MHz system clock to a 155.52 MHz clock for serial, NRZ, data transmission at 155.52 Mbps.

The AD805—VCXO circuit uses a frequency and a phase acquisition control loop for clock recovery and data retiming. The VCXO present in the frequency acquisition control loop aids frequency locking due to its output's accuracy. The phase acquisition loop uses a voltage controlled phase shifter to acquire phase lock.

The AD805 can be used by itself to automatically phase align (deskew) 155.52 Mbps input data to a reference 155.52 MHz clock. The phase acquisition loop works to match RETIMING MODULE input data phase with reference clock phase in this application. The voltage controlled phase shifter has a ±1/2 Unit Interval range.

PKD-01 Monolithic Peak Detector with Reset-and-Hold Mode

The PKD-01 is a monolithic peak detector which tracks an analog input signal until a maximum value has been reached and retains this peak value on its hold capacitor. The option to detect or ignore new peaks with its $\overline{\text{DET}}$ control pin is also offered. Detected peaks are presented as positive output levels, however negative peaks may also be detected without additional circuitry. This flexibility is due to its input amplifier which may operate as either an inverting or noninverting gain stage.

Its monolithic design offers significant advantages over hybrid and discrete designs. The matching characteristics attained in a monolithic circuit provide inherent advantages when charge injection and droop rate error reduction are primary goals. The PKD-01 maximizes the advantages of this technology by using *transconductance* amplifiers which: simplify internal frequency compensation, minimize acquisition time, and maximize circuit accuracy.

Accuracy is enhanced by the use of an output buffer which employes an FET amplifier input stage. This reduces droop rate error during lengthy peak hold periods. Temperature related droop rate error is reduced by employing bias current cancellation circuitry to minimize the gate currents tendency to double for every 10°C temperature change.

ADXL50 Monolithic Accelerometer with Signal Conditioning

The ADXL50 employs surface-micromachining technology to produce a device which senses uni-axis acceleration and outputs a linearly proportional voltage. The ADXL50 is a low cost IC accelerometer which is able to measure acceleration from 0 to ±50 g, and withstand shocks greater than 2000 g. The device operates on an output voltage range from 1.8 V at 0 g, and has a full scale variation of ±1 V. An uncommitted operational amplifier is also provided which allows the user to vary the full scale output voltage to as much as 0.25 V to 4.75 V.

The ADXL50 employs a variable, differential airgap capacitor to sense the direction and magnitude of acceleration. A simplified depiction of this device would contain a moveable center mass suspended above a polysilicon slab. This center mass is spring tethered at each end, to restore the mass position to absolute zero with no acceleration, and to allow it to move on only one axis (that axis being on a plane with the chip surface). This mass would have an extruding "arm" at a right angle to the axis of movement. On each side of the "arm" would be a capacitor plate, each driven by an equal amplitude but opposite phase signal. As the device is accelerated, a force described by F = ma. overcomes the force due to the spring constant. This movement relates to a change in capacitance which is linearly proportional to the phase and amplitude of the differential output signal. The amplitude is proportional to the acceleration magnitude while the resulting phase indicates the direction of acceleration. A force balancing technique is employed to reduce the mass arm movement thereby increasing its linearity as well as its dynamic range. (*For a more in depth description please refer to SAE Technical Paper Series #910496.*)

Analog Devices intends the ADXL50 to be the first in a family of accelerometers rated to detect acceleration from fractions of a g to several 100 g. Intended uses include: automotive airbags, automotive suspension, shock and vibration detection, and many military applications. The small size of the surface micromachined capacitors will allow the advent of multiaxis sensors.

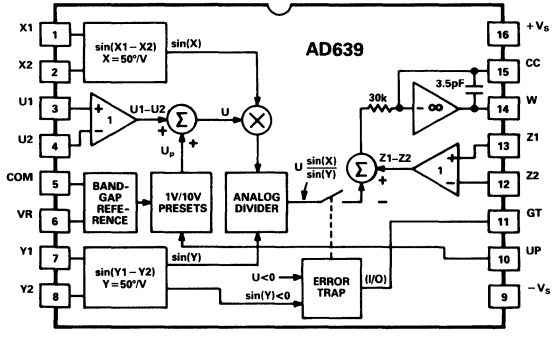
Universal Trigonometric Function Converter

AD639*

FEATURES
Complete, Fully-Calibrated Synthesis System
All Standard Functions: Sin, Cos, Tan, Cosec, Sec, Cot, Arcsin, Arccos, Arctan, etc.
Accurate Law Conformance (Sine to 0.02%)
Angular Range of ±500° (Sine Mode)
Function Programmable by Pin Strapping
1.5MHz Bandwidth (Sine Mode)
Multiplication via External Amplitude Input

APPLICATIONS
Continuous Wave Sine Generators
Synchro Sine/Cosine Multiplication
Coordinate Conversion and Vector Resolution
Imaging and Scanning Linearization Circuits
Quadrature and Variable Phase Oscillators

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD639 is a high accuracy monolithic function converter which provides all the standard trigonometric functions and their inverses via pin-strapping. Law conformance and total harmonic distortion surpass that previously attained using analog shaping techniques. Speed also exceeds that possible using ROM look-up tables and a DAC; in the sine mode, bandwidth is typically 1.5MHz. Unlike other function synthesis circuits, the AD639 provides a smooth and continuous sine conformance over a range of −500° to +500°. A unique sine generation technique results in 0.02% law conformance errors and distortion levels of −74dB in triwave to sinewave conversion.

The AD639 is available in three performance grades. The A and B are specified from −25°C to +85°C and the S is guaranteed over the extended temperature range of −55°C to +125°C. All versions are packaged in a hermetic TO-116, 16-pin ceramic DIP. A-grade chips are also available.

PRODUCT HIGHLIGHTS

The AD639 generates a basic function which is the ratio of a pair of independent sines:

$$W = U \frac{\sin (x_1 - x_2)}{\sin (y_1 - y_2)}$$

The differential angle arguments are proportional to the input voltages X and Y scaled by 50°/V. Using the 1.8V on-board reference any of the angular inputs can be preset to 90°. This provides the means to set up a fixed numerator or denominator (sin 90° = 1) or to convert either sine function to a cosine (cosθ = sin (90° − θ)). Using the ratio of sines, all trigonometric functions can be generated (see Table I).

The amplitude of the function is proportional to a voltage U, which is the sum of an external differential voltage ($U_1 - U_2$) and an optional internal preset voltage (U_p). The control pin UP selects a 0V, 1V or 10V laser-trimmed preset amplitude which may be used alone ($U_1 - U_2 = 0$) or internally added to the $U_1 - U_2$ analog input. At the output, a further differential voltage Z can be added to the ratio of sines to obtain the offset trigonometric functions versine (1 − cos θ), coversine (1 − sin θ) and exsecant (1 − sec θ). A gating input is available which may be used to enable or disable the analog output. This pin also acts as an error flag output in situations where a combination of inputs will cause the output to saturate or to be undefined.

In the inverse modes, the argument can be the ratio of two input signals. This allows the user to compute the phase angle between the real and imaginary components of a signal using the arctangent mode.

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*Protected by U.S. Patent Numbers 3,887,863; 4,475,169; 4,476,538.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

AD639—SPECIFICATIONS (typical @ T_A = 25°C, V_S = ±15 V, U or U_P = 10V unless otherwise specified)

Parameter	Conditions	AD639A Min	AD639A Typ	AD639A Max	AD639B Min	AD639B Typ	AD639B Max	AD639S Min	AD639S Typ	AD639S Max	Units
SYSTEM PERFORMANCE											
SINE AND COSINE MODE ACCURACY											
Law Conformance[1]	−90° to +90°, U = 10V		0.02			0.02			0.02		%
Total Harmonic Distortion[2]	@ 10kHz, U = 10V		−74			−74			−74		dB
Mismatch of Six Peaks	−540° to +540°		0.05			0.05			0.05		%
Output Noise	@ 10kHz, U = 10V		2.8			2.8			2.8		$\mu V/\sqrt{Hz}$
	@ 10kHz, U = 1V		0.5			0.5			0.5		$\mu V/\sqrt{Hz}$
PEAK ABSOLUTE ERROR											
Sine Mode	−90° to +90°, U_p = 10V		0.4	**0.8**		0.2	**0.4**		0.2	**0.8**	%FS
	T_{min} to T_{max}		1.0			0.8	**1.8**		1.2	**2.5**	%FS
Cosine Mode	−90° to +90°, U_p = 10V		0.6	**1.2**		0.4	**0.7**		0.5	**1.2**	%FS
	T_{min} to T_{max}		1.5			1.2	**2.0**		1.7	**2.7**	%FS
Sine or Cosine	−180° to +180°, U_p = 10V		0.8	**1.5**		0.5	**0.8**		0.6	**1.5**	%FS
	T_{min} to T_{max}		1.7			1.3	**2.5**		2.1	**3.0**	%FS
	−360° to +360°, U_p = 10V		1.2			1.0			0.9		%FS
	−90° to +90°, U_p = 1V		1.3	**2.5**		1.0	**1.7**		0.9	**2.5**	%FS
	T_{min} to T_{max}		1.5			1.0	**2.3**		2.0	**3.5**	%FS
	−180° to +180°, U_p = 1V		1.5	**3.0**		1.2	**2.0**		1.1	**3.0**	%FS
	T_{min} to T_{max}		1.7			1.3	**2.5**		2.3	**4.0**	%FS
	−360° to +360°, U_p = 1V		2.0			1.8			1.5		%FS
vs Supply	−360° to +360°, U_p = 10V V_s = ±15V ±1V		0.02			0.02			0.02		%FS/V
	−360° to +360°, U_p = 1V V_s = ±15V ±1V		0.07			0.07			0.07		%FS/V
TANGENT MODE ACCURACY											
Peak Error[3]	−45° to +45°, U_p = 10V		0.5	**3.5**		0.5	**2.0**		0.5	**3.5**	%FS
	T_{min} to T_{max}		2.5			1.5	**2.8**		3.0		%FS
	−45° to +45°, U_p = 1V		0.9	**5.0**		0.9	**3.0**		0.9	**2.5**	%FS
	T_{min} to T_{max}		4.0			2.0	**5.0**		**1.5**	**3.0**	%FS
ARCTANGENT MODE ACCURACY											
Peak Angular Error											
Fixed Scale	U_p = 1V		0.5			0.5			0.5		Degrees
Variable Scale	U = 0.1V, −11V≤Z≤+11V		1.5			1.5			1.5		Degrees
	U = 10V, −11V≤Z≤+11V		0.2			0.2			0.2		Degrees
SECTIONAL SPECIFICATIONS											
ANGLE INPUTS (X1 & X2, Y1 & Y2)[4]											
Input Resistance to COM			3.6			3.6			3.6		kΩ
Nominal Scaling Factor			50			50			50		°/V
X1 & X2 Inputs											
Angular Range For Specified Error(X1 − X2)		−360		+360	−360		+360	−360		+360	Degrees
Scaling Error X1 or X2			0.2	**0.65**		0.2	**0.65**		0.2	**0.65**	%
Angular Offset X1 = X2 = 0			0.1	**0.3**		0.1	**0.3**		0.1	**0.3**	Degrees
Y1 & Y2 Inputs											
Angular Range For Specified Error (Y1 − Y2)		0		+180	0		+180	0		+180	Degrees
Scaling Error Y1 or Y2			0.2	**2.0**		0.2	**2.0**		0.2	**1.0**	%
Angular Offset Y1 = Y2 = 0			0.1	**1.0**		0.1	**1.0**		0.1	**0.5**	Degrees
AMPLITUDE INPUTS (U1 & U2)											
Input Resistance to COM			50			50			50		kΩ
Nominal Gain	X = Y = VR, W to Z1		1			1			1		V/V
Gain Error	U = 0.1 to 10V		0.01	**0.5**		0.01	**0.5**		0.01	**0.5**	%
	T_{min} to T_{max}		0.08			0.08			0.25		%
Voltage Offset	$U_1 = U_2$ = 0V		3.0	**10**		3.0	**10**		3.0	**10**	mV
	T_{min} to T_{max}		3.0			3.0			4.0		mV
Linearity Error	0≤$U_1 - U_2$≤10V		0.1			0.1			0.1		%
AMPLITUDE PRESET (UP)											
1V Preset Enabled	UP tied to $-V_S$										
Amplitude Accuracy			0.4	**2.0**		0.4	**2.0**		0.4	**2.0**	%
	T_{min} to T_{max}		1.5			1.5			2.0		%
10V Preset Enabled	UP tied to $+V_S$										
Amplitude Accuracy			0.1	**0.55**		0.1	**0.55**		0.1	**0.55**	%
	T_{min} to T_{max}		1.0			1.0			1.5		%
INVERSE INPUTS (Z1 & Z2)											
Input Resistance to COM			50			50			50		kΩ

Parameter	Conditions	AD639A Min	AD639A Typ	AD639A Max	AD639B Min	AD639B Typ	AD639B Max	AD639S Min	AD639S Typ	AD639S Max	Units
SIGNAL OUTPUT (W)[5]	$R_L \geq 2k\Omega, C_L \leq 100pF$										
Small Signal Bandwidth W to Z1											
	Cc = 0		1.5			1.5			1.5		MHz
	Cc = 200pF		30			30			30		kHz
Slew Rate	Cc = 0		30			30			30		V/μs
Output Voltage Swing		**±11**	±13		**±11**	±13		**±11**	±13		V
Short Circuit Current		**20**	30	**45**	**20**	30	**45**	**20**	30	**45**	mA
Output Offset	$Z_1 = Z_2 = 0, U_p = 10$		5	**30**		5	**30**		5	**30**	mV
	T_{min} to T_{max}		10			10					mV
	$Z_1 = Z_2 = 0, U_p = 1V$			**20**			**20**			**20**	mV
	T_{min} to T_{max}		7			7					mV
VOLTAGE REFERENCE (VR)											
$R_L \geq = 1.8k\Omega$											
Nominal Output			+1.8			+1.8			+1.8		V
Output Voltage Tolerance			0.05	**0.45**		0.05	**0.45**		0.05	**0.45**	%
	T_{min} to T_{max}		0.08			0.08	**0.5**		0.2	**0.6**	%
Supply Regulation	$+V_S = 5V$ to 18V		150			150			150		μV/V
Maximum Output Current			4			4			4		mA
GATE I/O (GT)											
Switching Threshold as an Input	Output Valid		+1.5			+1.5			+1.5		V
	Output Invalid		0.1			0.1			0.1		V
Voltage Output	Error, $R_L = 5k\Omega$		+2.25			+2.25			+2.25		V
	No Error, $R_L = 5k\Omega$		−0.25			−0.25			−0.25		V
POWER SUPPLIES											
Operating Range		**±5.5**		**±18**	**±5.5**		**±18**	**±5.5**		**±18**	V
$+V_S$ Quiescent Current	U = X = 0V, Y = Vr		8.0	**11**		8.0	**11**		8.0	**11**	mA
$-V_S$, Quiescent Current	U = X = 0V, Y = Vr		5.5	**7.5**		5.5	**7.5**		5.5	**7.5**	mA
TEMPERATURE RANGE											
Operating, Rated Performance		−25		+85	−25		+85	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[6]											
16-Pin Ceramic Side Braze DIP (D)		AD639AD			AD639BD			AD639SD			
								AD639SD/883B			
Chips		AD639 A-Chips									

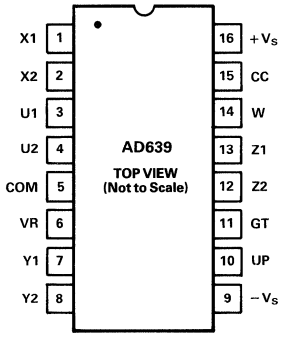
NOTES
[1]Intrinsic accuracy measured at an amplitude of 10V using external adjustments to absorb residual errors in angular scaling, angular offset, amplitude scaling and output offset.
[2]Using a time and amplitude symmetric triangular wave of +3.6V peak-to-peak and external adjustments to absorb residual errors in angular scaling and offset.
[3]Full scale is defined as the ideal output when the angle input is at either end of the limit specified.
[4]Specifications for the X inputs apply for range U = 1V to 10V, while the Y input errors are specifically given for U = 1V.
[5]When driving loads of less than 4kΩ, a 25pF capacitor from pin 15 to pin 9 avoids possible instability, although this is unnecessary when C_L is greater than 150pF.
[6]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units. Contact the factory for details.

PIN CONFIGURATION

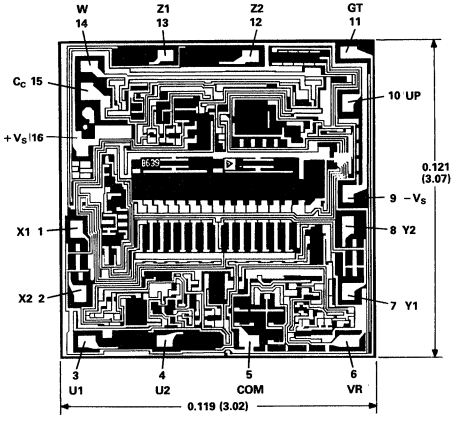
16-Pin Side Brazed DIP (Ceramic) (D-16) Package



METALIZATION PHOTO

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).
Consult factory for latest dimensions.



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD639AD	−25°C to +85°C	Side Brazed Ceramic DIP	D-16
AD639BD	−25°C to +85°C	Side Brazed Ceramic DIP	D-16
AD639A-Chips	−25°C to +85°C	Chips	
AD639SD	−55°C to +125°C	Side Brazed Ceramic DIP	D-16
AD639SD/883B	−55°C to +125°C	Side Brazed Ceramic DIP	D-16

*For outline information see Package Information section.

ANALOG DEVICES

RGB to NTSC/PAL Encoder

AD720

FEATURES

Separate Chrominance, Luminance, and Composite Video Outputs
Drives 75 Ω Reverse-Terminated Loads
No External Filters or Delay Lines Required
Compact 28-Pin PLCC
Logic Selectable NTSC or PAL Encoding Modes
Logic Selectable Power-Down Mode

APPLICATIONS

RGB to NTSC or PAL Encoding

PRODUCT DESCRIPTION

The AD720 RGB to NTSC/PAL Encoder is a BiCMOS LSI circuit that converts red, green and blue color component signals into their corresponding luminance (baseband amplitude) and chrominance (subcarrier amplitude and phase) signals in accordance with either NTSC or PAL standards. These two outputs are also combined to provide a composite video output. All three outputs are available separately at voltages of twice the standard signal levels as required for driving 75 Ω reverse-terminated cables.

The AD720 provides a complete, fully calibrated function, requiring only termination resistors, decoupling networks, a clock input at four times the subcarrier frequency, and a composite sync pulse. The AD720 also has two control inputs: one input selects the TV standard (NTSC/PAL) and the other (ENCD) powers down most sections of the chip when the encoding function is not in use. All logical inputs are TTL and CMOS compatible. The chip operates from ±5 V supplies.

All required low-pass filters are on chip. After the input signals pass through a precision RGB to YUV encoding matrix, two on-chip low-pass filters limit the bandwidth of the U and V color-difference signals to 1.2 MHz prior to quadrature modulation of the color subcarrier; a third low-pass filter at 3.6 MHz (NTSC) or 4.4 MHz (PAL) follows the modulators to limit the harmonic content of the output. Delays in the U and V chroma filters are matched by an on-chip sampled-data delay line in the Y signal path; to prevent aliasing, a prefilter at 5 MHz is included ahead of the delay line and a postfilter at 5 MHz is added after the delay line to suppress harmonics in the output. These low-pass filters are optimized for minimum pulse overshoot.

The AD720 is available in a 28-pin plastic leaded chip carrier for the 0°C to +70°C commercial temperature range.

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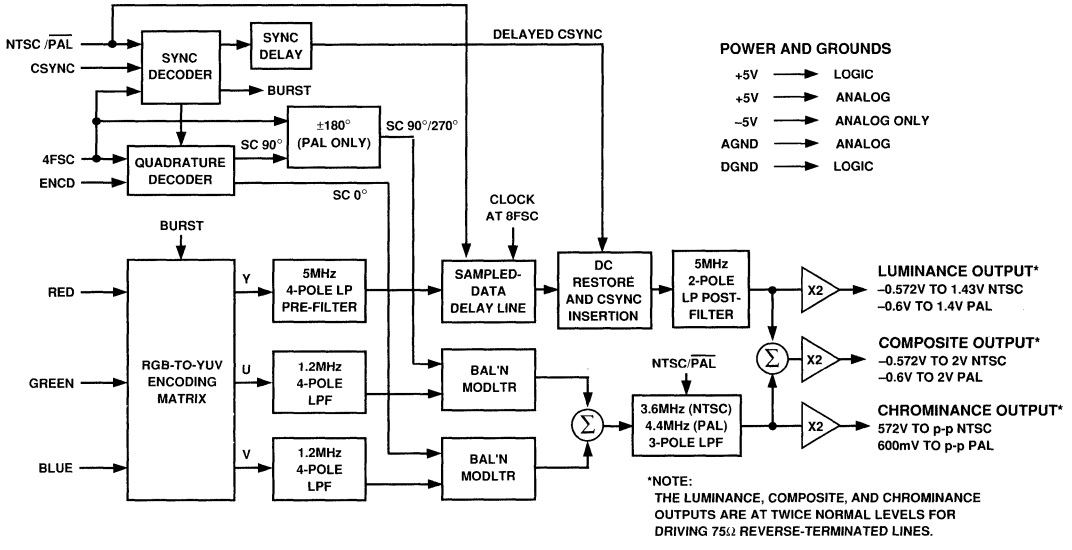
FUNCTIONAL BLOCK DIAGRAM

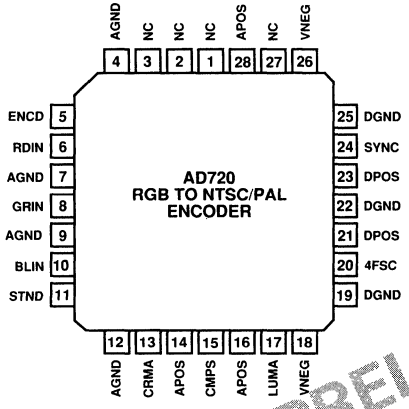


AD720—SPECIFICATIONS (T_A = +25°C and Supplies ±5 V unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
SIGNAL INPUTS (RDIN, GRIN, BLIN)					
Input Amplitude	NTSC		714		mV
	PAL		700		mV
Input Resistances[1]					
RDIN with Respect to AGND			6		kΩ
GRIN with Respect to AGND			15		kΩ
BLIN with Respect to AGND			3		kΩ
Input Capacitance			5		pF
LOGIC INPUTS (C-SYNC, 4FSC, ENCD, NTSC)					
Logic LO Input Voltage				1	V
Logic HI Input Voltage		4			V
Logic LO Input Current			20		μA
Logic HI Input Current			100		μA
VIDEO OUTPUTS[2] (LUMA, CRMA, CMPS)					
Luminance (LUMA) Output					
Bandwidth			5		MHz
Gain Error			±1		%
Linearity			±0.1		%
Chrominance (CRMA) Output					
Bandwidth	NTSC		4		MHz
	PAL		5.5		MHz
Color Burst Amplitude	NTSC		286		mV
	PAL		300		mV
Absolute Gain Error			±5		%
Absolute Phase Error			±3		Degree
Chroma/Luma Time Alignment[3]	NTSC		−170		ns
Composite Output					
Differential Gain			±5		%
Differential Phase			±5		Degree
Output Offset Voltage	Chroma, Luma, or Composite Outputs		±50		mV
Chroma Feedthrough	Monochrome Input		20		mV
POWER SUPPLIES (APOS, DPOS, VNEG)					
Recommended Supply Range	Dual Supply	±4.5		±5.5	V
Zero-Signal Quiescent Current	−5 V Supply		17		mA
	+5 V Supply		17		mA
Full-Output Quiescent Current[4]	−5 V Supply		35		mA
	+5 V Supply		67		mA

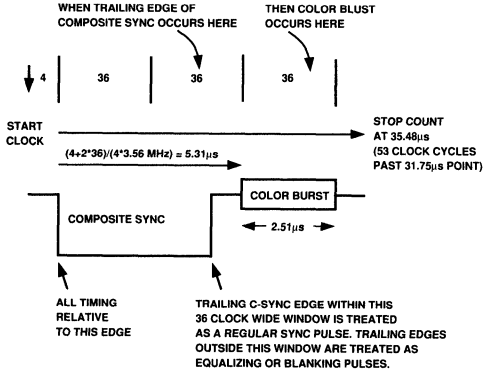
NOTES
[1]Input scaling resistors provide best scaling accuracy when source resistance is 37.5 Ω (75 Ω reverse-terminated input).
[2]All outputs are measured at a reverse-terminated load; voltages at IC pins are twice those specified here.
[3]This is a predistortion (per FCC specifications) that compensates for the chroma/luma delay in the low-pass filter that separates the luminance and chrominance signals in a television receiver.
[4]CRMA, LUMA, and CMPS outputs are all connected to 75 Ω reverse-terminated loads; full-white signal for entire field.
Specifications subject to change without notice.

PIN CONFIGURATION

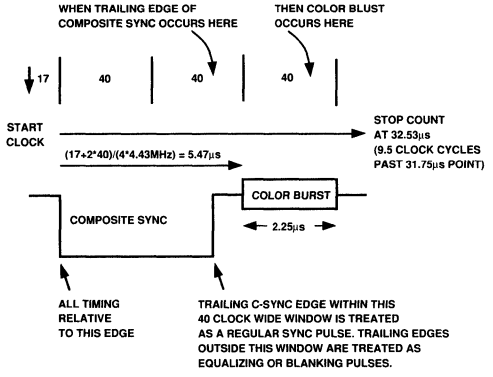


PIN DESCRIPTIONS

ENCD	A logical low level powers down chip when not in use
STND	A logical high level input selects NTSC encoding; A logical low level selects PAL encoding
4FSC	Clock input at at four times the subcarrier frequency
SYNC	Input pin for composite television synchronization pulses
RDIN	Red Component Input
GRIN	Green Component Input
BLIN	Blue Component Input
CRMA	Chrominance Output (Subcarrier Only)
CMPS	Composite Video Output
LUMA	Luminance Plus SYNC Output
AGND	Analog Ground Connections (4)
DGND	Digital Ground Connections (3)
APOS	Analog Positive Supply (+5 V ± 5%) (3)
DPOS	Digital Positive Supply (+5 V ± 5%) (2)
VNEG	System Negative Supply (−5 V ± 5%) (2)

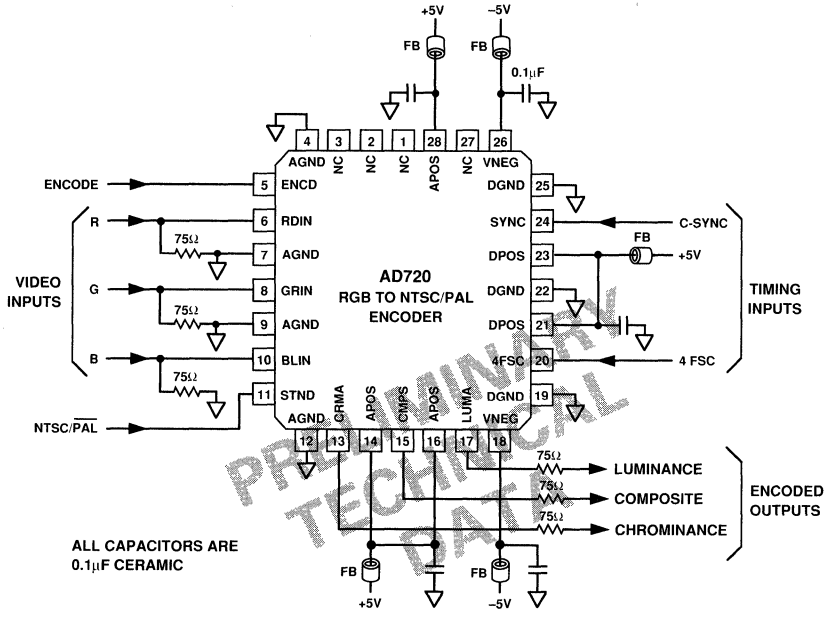


NTSC Timing



PAL Timing

AD720 — Typical Application



Encoded Outputs

ANALOG DEVICES

Programmable Clock Generator

AD730

FEATURES
16 Selectable Frequencies
216 MHz max ECL Output
54 MHz max TTL Output
Low Output Jitter
Low Cost
Mask Programmable Frequencies
Single Reference Crystal or TTL Clock
Standard MPU Interface
Bt458 Compatible Reset
+5 Volt Supply
20-Pin SOIC Packaging

PRODUCT DESCRIPTION

The AD730 Programmable Clock Generator is a monolithic solution for providing up to 16 output frequencies. Output frequencies of greater than 216 MHz are realizable, combined with excellent jitter performance. The available output frequencies are determined through a "Personalization Mask Option." The AD730-1 has been personalized to provide the following frequencies with a 6.75 MHz reference crystal:

47.25 MHz	54.00 MHz
64.125 MHz	74.250 MHz
94.50 MHz	108.00 MHz
118.125 MHz	135.00 MHz
189.00 MHz	216.00 MHz

Other frequencies may be personalized on an AD730 using the following algorithm:

$$f_{OUT} = f_{REF}\frac{M}{N}$$

where: N = 1 or 2
M = 1 to 64

The output frequency is selected through a standard MPU interface. When selecting a new frequency, the ECL output is glitch free during the transition. To ensure compatibility with video DACs, the AD730 provides pipeline setup sequencing during frequency select switching. In addition to supplying the ECL output clock frequency, the AD730 provides a divide by 4 and divide by 64 TTL outputs.

Low jitter and excellent power supply rejection are achieved by careful attention to layout and the use of an active integrator in the loop filter. The only external components required are a reference crystal and three passive components for the PLL loop filter.

The AD730 will be available in a 20-pin SOIC package and is specified to operate over the 0°C to +70°C commercial temperature range. However, evaluation samples are available in a 20-pin side brazed package.

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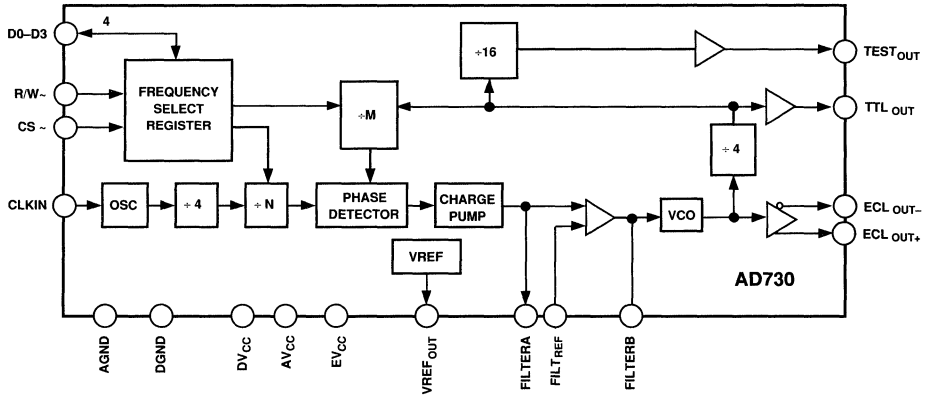
FUNCTIONAL BLOCK DIAGRAM



AD730—SPECIFICATIONS

PROGRAMMABLE CLOCK GENERATOR ($0°C \le T_A \le 70°C$, $4.65 \le V_{CC} \le 5.25$)

Parameter	Conditions	Min	Typ	Max	Units
CLOCK FREQUENCY (ECL)	See Note 1				
Jitter	f_{OUT} = 47.25 MHz (divide ratios = 28/4)		250	500	ps rms
Jitter	f_{OUT} = 54.00 MHz (divide ratios = 32/4)		250	500	ps rms
Jitter	f_{OUT} = 94.50 MHz (divide ratios = 56/4)		175	350	ps rms
Jitter	f_{OUT} = 108.00 MHz (divide ratios = 64/4)		175	350	ps rms
Jitter	f_{OUT} = 118.125 MHz (divide ratios = 140/8)		175	350	ps rms
Jitter	f_{OUT} = 135.00 MHz (divide ratios = 80/4)		175	350	ps rms
Jitter	f_{OUT} = 189.00 MHz (divide ratios = 112/4)		125	250	ps rms
Jitter	f_{OUT} = 216.00 MHz (divide ratios = 128/4)		125	250	ps rms
Jitter	f_{OUT} = 64.125 MHz (1024 × 768 @ 60 Hz)		250	500	ps rms
Jitter	f_{OUT} = 74.250 MHz (1024 × 768 @ 70 Hz)		250	500	ps rms
CLOCK FREQUENCY (TTL)[1]					
Jitter	1/4 Frequency of ECL Clock		250		ps rms
REFERENCE CLOCK INPUT					
Input Frequency			6.75		MHz
V_{IH}		2.0			V
V_{IL}				0.8	V
REFERENCE VOLTAGE[2]					
Output Voltage		1.215		1.255	V
Max Source Current		1.0			mA
Max Sink Current		300			μA
CLOCK OUTPUT (ECL)					
V_{OH}	See Note 3	4.04		4.19	V
V_{OL}	See Note 3	3.15		3.35	V
I_{OH}		10.5			mA
Rise Time	See Note 3	1.3		2.0	ns
Fall Time	See Note 3	1.3		2.0	ns
Duty Cycle Asymmetry	See Note 3	−10		+10	%
Output Frequency Range		47.25		216	MHz
CLOCK OUTPUT (TTL)					
V_{OH}		2.4			V
V_{OL}				0.4	V
I_{OL}				−2.0	mA
Rise Time	See Note 4			4	ns
Fall Time	See Note 4			4	ns
Duty Cycle Asymmetry	See Note 4	−20		+20	%
Output Frequency Range		11.8		54	MHz
CONTROL BUS LOGIC	CS~, D0, D1, D2, D3, R/W~				
V_{IH}		2.0			V
V_{IL}				0.8	V

NOTES

[1]a. Jitter is measured by triggering on the output clock, delayed 16 μs and then measuring the time period from the trigger edge to the next edge of the output clock after the delay. This measurement is repeated multiple times and then the RMS value is determined.

[1]b. The V_{CO} gain is 100 MHz/V (±40% tolerance). The charge pump current is 200 μA peak.

[2]The reference voltage will be trimmed within limits specified at Trim & Probe. However, we are not certain if these limits can be maintained when the part has been packaged. Initial silicon samples will determine what limits are achievable.

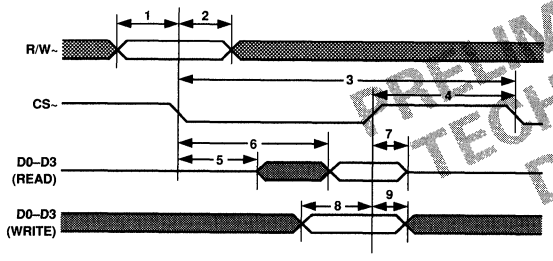
[3]ECL Output specifications are determined with the following load conditions: each output has a 330 Ω pull-down resistor to ground and a 220 Ω pull-up resistor to V_{CC}.

[4]TTL output rise time/fall time is determined with a 10 pF load. Rise time/fall time is defined as the 10% to 90% point.

Specifications subject to change without notice.

TIMING ($0°C \leq T_A \leq 70°C$, $4.65 \leq V_{CC} \leq 5.25$)

Parameter	Conditions	Min	Typ	Max	Units
TIMING					
R/W~ Setup Time	Timing Diagram – 1	0			ns
R/W~ Hold Time	Timing Diagram – 2	15			ns
CS~ Low + High Time	Timing Diagram – 3	70			ns
CS~ High Time	Timing Diagram – 4	25			ns
CS~ Asserted to Data Driven	Timing Diagram – 5	10			ns
CS~ Asserted to Data Valid	Timing Diagram – 6			75	ns
CS~ Negated to Data Tristated	Timing Diagram – 7			25	ns
Write Data Setup Time	Timing Diagram – 8	35			ns
Write Data Hold Time	Timing Diagram – 9	0			ns



Timing Diagram

ORDERING GUIDE

Model	Description	Package Option*
AD730JR-1	Wide Body 20-Pin SOIC	R-20

*For outline information see Package Information section.

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POWER SUPPLIES ($0°C \leq T_A < 70°C$, $4.5\ V \leq V_{CC} \leq 5.5\ V$)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{CC}		4.5	5	5.5	V
Quiescent Current I_{CC}			62		mA
Power Dissipation			310		mW

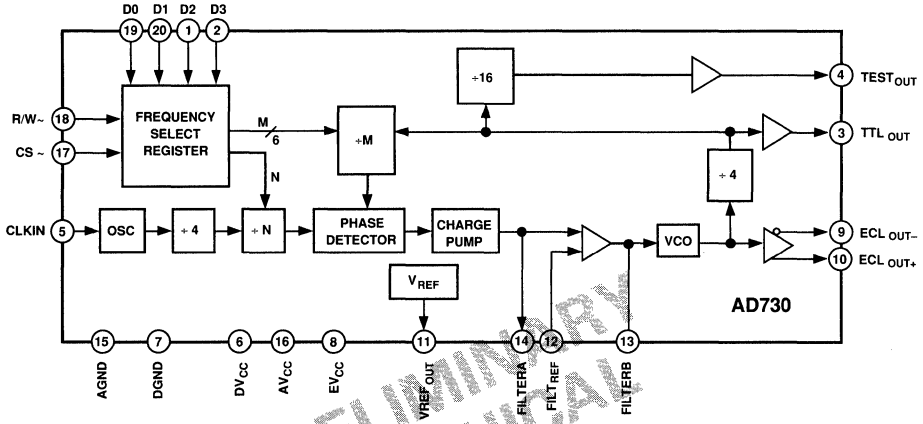
ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{CC}				7.5	V
Storage Temperature Range		–65		150	°C
Operating Temperature Range[2]		0		70	°C
Lead Temperature Range	Soldering 60 Sec			300	°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other condition above those indicated in the operational section of this specification is not implied. Exposure to absolute rating conditions for extended period may affect device reliability.
[2]20-pin SOIC package $\theta_{JA} = 100°C/W$.

FREQUENCY SELECT REGISTER ASSIGNMENTS

				f_{OUT}		
D3	**D2**	**D1**	**D0**	**ECL**	**TTL**	
0	0	0	0	47.25	11.8125	MHz
0	0	0	1	54.00	13.50	MHz
0	0	1	0	94.50	23.625	MHz
0	0	1	1	108.00	27.00	MHz
0	1	0	0	118.125	29.53	MHz
0	1	0	1	135.00	33.75	MHz
0	1	1	0	189.00	47.25	MHz
0	1	1	1	216.00	54.00	MHz
1	0	0	0	64.125	16.031	MHz
1	0	0	1	74.250	18.5625	MHz
1	0	1	0	undefined	undefined	
1	0	1	1	undefined	undefined	
1	1	0	0	undefined	undefined	
1	1	0	1	undefined	undefined	
1	1	1	0	undefined	undefined	
1	1	1	1	OSCILLATOR STOPPED		



PIN ASSIGNMENTS

Pin	Description		I/O Type	Application Notes
01	D2	Frequency Select Bit 2	TTL I/O	2nd MSB of four frequency select pins.
02	D3	Frequency Select Bit 3	TTL I/O	MSB of four frequency select pins.
03	TTL_{OUT}	TTL Clock Output	TTL Output	TTL output frequency is one quarter of ECL output frequency. Output is actively driven high and low. It does not require a pull-up resistor.
04	$TEST_{OUT}$	Test Output	TTL Output	This is the ECL output divided by 64. Allows for in-circuit functional testing.
05	CLKIN	Crystal Oscillator Input	TTL Input	6.75 MHz Reference Crystal or Crystal Oscillator.
06	DV_{CC}	Digital V_{CC}	Power	V_{CC} for CMOS logic and TTL output.
07	DGND	Digital Ground	Power	Ground for CMOS logic and TTL output.
08	EV_{CC}	ECL V_{CC}	Power	V_{CC} for ECL Clock Output. Decoupling with 0.1 μF‖0.01 μF required.
09	ECL_{OUT-}	ECL clock output (negative)	ECL Output	ECL output referenced to V_{CC}.
10	ECL_{OUT+}	ECL clock output (positive)	ECL Output	ECL output referenced to V_{CC}.
11	V_{REFOUT}	1.235 V Bandgap Reference	Analog	Voltage reference for video DAC.
12	$FILT_{REF}$	Loop Filter Reference	Analog	An external capacitor allows adjustment for optimal loop noise performance.
13	FILTERB	PLL Filter	Analog	External loop filter. Apply PLL filter to FILTERB.
14	FILTERA	PLL Filter	Analog	External loop filter. Apply PLL filter to FILTERA.
15	AGND	Analog Ground	Power	Ground for PLL.
16	AV_{CC}	Analog V_{CC}	Power	V_{CC} for PLL. Decoupling with 0.1 μF‖0.01 μF required.
17	CS~	Chip Select	TTL Input	Negative edge latches state R/W~. Positive edge latches state of D0, D1, D2, D3.
18	R/W~	Read or Write to Data Bus	TTL Input	State is latched on negative CS~. Low for writing to and high for reading from the frequency select register.
19	D0	Frequency Select Bit 0	TTL I/O	LSB of four frequency select pins.
20	D1	Frequency Select Bit 1	TTL I/O	2nd LSB of four frequency select pins.

THEORY OF OPERATION

START-UP OPERATION

An internal power on reset function is provided in the AD730. Upon power-up, the device will reset to a fixed output frequency. This frequency is the lowest frequency output available −47.25 MHz. This frequency can also be obtained during normal operation by loading an all "0"s pattern (D0–D3) into the frequency select register.

CONTROL INTERFACE

The timing and operation of the digital interface is defined as the standard MPU interface. The state of the R/W~ signal is latched on the falling edge of CS~. This determines whether one is reading the current selected output frequency from the device or writing a new output frequency to the device. During a read operation, on the falling edge of CS~, the content of the frequency select register is driven onto the four data lines (D0–D3). On the rising edge of CS~, while writing, the four data inputs (D0–D3) are latched into the frequency select register. The content of the frequency select register determines which one of sixteen possible output frequencies will be generated. The AD730–1 has only ten frequencies that are defined in the device (see Frequency Select Register Assignments Table).

RESET FUNCTION

Two programmed reset modes are supported. The first reset is invoked by loading an all "1"s pattern (D0–D3) into the frequency select register. This reset function causes the main PLL oscillator to synchronously halt with the ECL output in the high state. When the frequency select register reprogrammed to a valid output frequency (see Frequency Select Register Assignments Table), the oscillator is released. Short duration clock half- cycles are avoided, both when entering and leaving this reset mode.

The second reset occurs each time the frequency select register is reprogrammed to a new frequency. This reset is intended to set the pipeline delay of the Bt458 video DAC. When a new frequency is programmed, the $ECL_{OUT(+)}$ and $ECL_{OUT(-)}$ are stopped with the $ECL_{OUT(+)}$ high and $ECL_{OUT}(-)$ low for four rising edges of the TTL_{OUT} clock. On the fourth rising edge of the TTL_{OUT} clock, the ECL_{OUT} clock is synchronously released (see Figure 1).

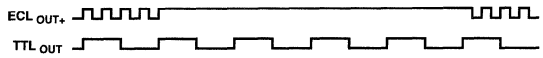


Figure 1.

REFERENCE CLOCK INPUT

The reference clock input, CLKIN, will accept either a standard TTL input or serve as a single pin oscillator by applying a <10 MHz crystal.

CLOCK OUTPUTS

The clock output is an ECL output, referenced to V_{CC}, that is capable of operating up to 216 MHz. This output contains circuitry that provides a smooth transition during changes in the output frequency. Specifically, in order to prevent a short cycle from occurring, the circuit checks the state of the output when a new frequency is written to the device in order to prevent a short cycle from occurring during frequency transitions. When the output reaches the correct state, a glitch free transition in frequency occurs.

TTL compatible, divide by 4 and 64, outputs are also provided, TTL_{OUT} and $TEST_{OUT}$ respectively.

GROUNDING

Proper grounding and decoupling should be a primary design objective when working with PLL circuits. Separate analog and digital supplies are present on chip, but it is recommended that there be one common analog and digital ground plane. This approach is less difficult to design, and it will produce good results. Decoupling of the analog power pins (Pins 8 and 16) should contain a 0.1 μF capacitor in parallel with a 0.01 μF capacitor.

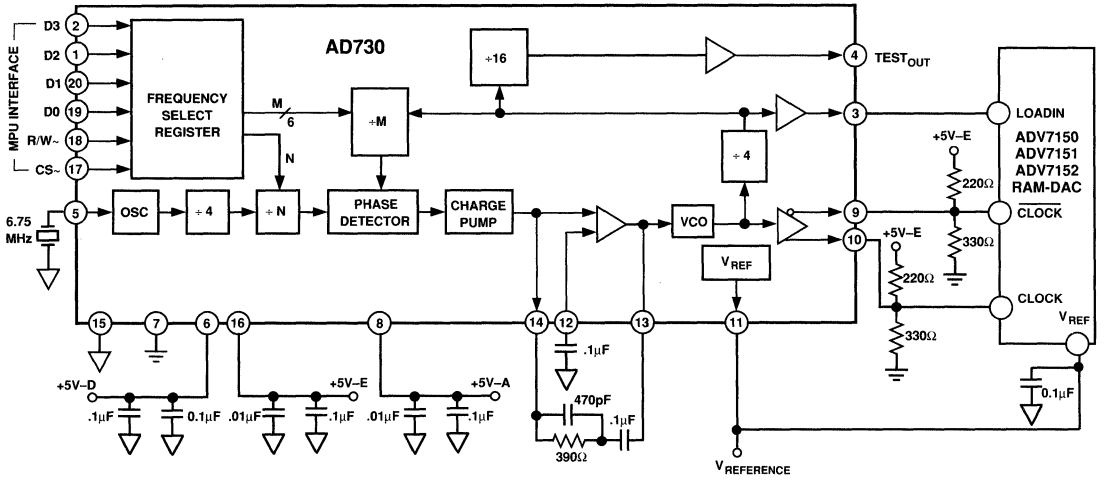


Figure 2. Typical Application

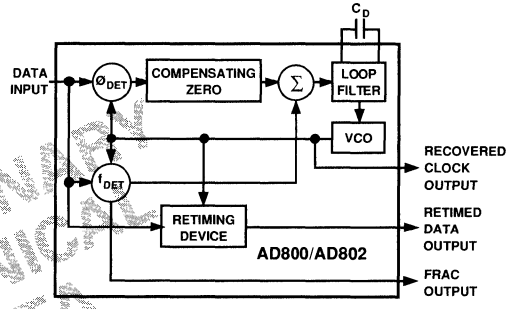
Clock Recovery and Data Retiming Phase-Locked Loop

AD800/AD802

FEATURES

Clock Recovery Center Frequency:
20 MHz to 155 MHz, Factory Programmable
Fractional Loop Bandwidth: 0.01% to 1% Bit Rate, Factory Programmable
Accepts NRZ Data, No Preamble Required
Recovered Clock and Retimed Data Outputs
Phase-Locked Loop Type Clock Recovery—No Crystal Required
Random Jitter: 20° Peak-to-Peak
Pattern Jitter: Virtually Eliminated
10KH ECL Compatible

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD800/AD802 provides clock recovery and data retiming from an NRZ encoded data stream. The factory trims the center frequency of the VCO to guarantee loop capture range and tracking range over the operating temperature range. This eliminates a reliance on external components for center frequency setting.

The AD800/AD802 acquires frequency and phase lock on input data using two control loops. The frequency acquisition control loop initially acquires the clock frequency of the input data, without the need for a VCXO. At frequency lock, the frequency error is zero, and the frequency detector has no effect. The phase acquisition control loop then works to ensure that the output phase tracks the input phase. The AD800/AD802 requires no control input for the different types of acquisitions.

The device will acquire to random or scrambled data; no preamble is required. The VCO provides a clock output within ±20% of the nominal system frequency in the absence of input data transitions. The AD800/AD802 typically dissipates 750 mW and is specified to operate from a single −5.2 V supply.

The frequency detector provides a frequency acquisition (FRAC) output, which indicates when the device is acquiring frequency lock. During the frequency acquisition process this output is a series of pulses that occur at the points of cycle slip between the data frequency and the recovered clock. Once the device has acquired frequency lock, no pulses appear at the FRAC output.

The user sets the acquisition time of the AD800/AD802 by choosing a capacitor whose value determines loop damping. A loop damping factor of 5 corresponds to an acquisition time of 1×10^6 bit periods, and a loop damping factor of 1 corresponds to an acquisition time of 1×10^4 bit periods.

The AD800/AD802 exhibits virtually no pattern jitter due to its phase detector (patented). AD802-155 total loop jitter measures 20° peak-to-peak.

Refer to the Ordering Guide for devices.

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AD800/AD802—SPECIFICATIONS (V_{EE} = −5.2 V, V_{CC} = GND, T_A = 25°C, Loop Damping Factor = 5, unless otherwise noted)

Parameter	Condition	AD802-155KR Min	Typ	Max	Units
NOMINAL CENTER FREQUENCY			155.52		MHz
TRACKING RANGE		140		170	Mbps
	T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}	155		156	Mbps
CAPTURE RANGE		140		170	Mbps
	T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}	155		156	Mbps
STATIC PHASE ERROR	ρ = 1		10	30	Degrees
	ρ = 1, T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}		10	30	Degrees
TRANSITIONLESS DATA RUN				240	Bit Periods
	T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}			240	Bit Periods
OUTPUT JITTER	ρ = 1		2.3		Degrees rms
	2^7-1 PRN Sequence		3.3	5	Degrees rms
	$2^{23}-1$ PRN Sequence		3.3	5	Degrees rms
	ρ = 1, T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}		5		Degrees rms
	2^7-1 PRN Sequence, T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}		5	7	Degrees rms
	$2^{23}-1$ PRN Sequence, T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}		5	7	Degrees rms
JITTER TOLERANCE	f = 10 Hz		20,000		Unit Intervals
	f = 6.5 kHz	1.5	80		Unit Intervals
	f = 65 kHz	0.15	2		Unit Intervals
	f = 10 Hz, T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}	1.5	20,000		Unit Intervals
	f = 6.5 kHz, T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}	1.5	80		Unit Intervals
	f = 65 kHz, T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}	0.15	2		Unit Intervals
JITTER TRANSFER					
Damping Factor (Nominal)	C_D = 2.2 nF		1		ζ (no units)
	C_D = 0.047 µF		5		ζ (no units)
	C_D = 0.22 µF		10		ζ (no units)
Peaking	ζ = 1		2		dB
	ζ = 5		0.08		dB
	ζ = 10		0.02		dB
Bandwidth	T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}			130	kHz
ACQUISITION TIME	ζ = 1, 2^7-1 PRN Sequence		1×10^4		Bit Periods
	ζ = 5, 2^7-1 PRN Sequence		1×10^6	1.5×10^6	Bit Periods
	ζ = 10, 2^7-1 PRN Sequence		1×10^6		Bit Periods
POWER SUPPLY					
Voltage (V_{MIN} to V_{MAX})		−4.5	−5.2	−5.5	Volts
Current			140	170	mA
	T_{MIN} to T_{MAX}, V_{MIN} to V_{MAX}			180	mA
INPUT VOLTAGE LEVELS	V_{MIN} to V_{MAX}				
Input Logic High, V_{IH}		−1.084		−0.720	Volts
Input Logic Low, V_{IL}		−1.95		−1.594	Volts
OUTPUT VOLTAGE LEVELS	V_{MIN} to V_{MAX}				
Output Logic High, V_{OL}		−1.084		−0.72	Volts
Output Logic Low, V_{OH}		−1.95		−1.60	Volts
INPUT CURRENT LEVELS	V_{MIN} to V_{MAX}				
Input Logic High, I_{IH}		25		62	µA
Input Logic Low, I_{IL}		15		39	µA
OUTPUT SLEW TIMES	V_{MIN} to V_{MAX}				
Rise Time (t_R)	20%–80%		0.75	1.5	ns
Fall Time (t_F)	80%–20%		0.75	1.5	ns
SYMMETRY	ρ = 1/2				
Recovered Clock Output		45		55	%

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −6 V
Input Voltage (Pin 16 or Pin 17 to V_{CC}) . . . . V_{EE} to +300 mV
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to an absolute maximum rating condition for an extended period may adversely affect device reliability.

ORDERING GUIDE

Device	Center Frequency	Fractional Loop Bandwidth	Description	Operating Temperature	Package Option*
AD802-155KR	155.52 MHz	0.08%	20-Pin Plastic SOIC	0°C to +70°C	R-20

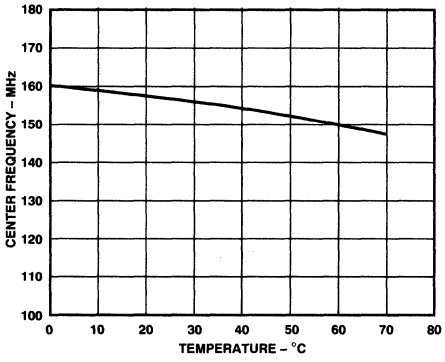
*For outline information see Package Information section.

PIN DESCRIPTIONS

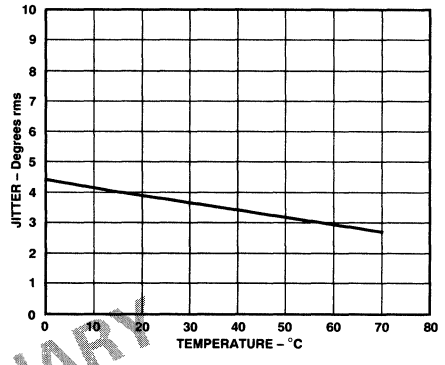
Number	Mnemonic	Description
1	$\overline{\text{DATAOUT}}$	Differential Retimed Data Output
2	DATAOUT	Differential Retimed Data Output
3	V_{CC2}	Digital Ground
4	$\overline{\text{CLKOUT}}$	Differential Recovered Clock Output
5	CLKOUT	Differential Recovered Clock Output
6	V_{EE}	Digital V_{EE}
7	V_{EE}	Digital V_{EE}
8	V_{CC1}	Analog Ground
9	AV_{EE}	Analog V_{EE}
10	ASUBST	Analog Substrate
11	CF_2	Loop Damping Capacitor Input
12	CF_1	Loop Damping Capacitor Input
13	AV_{CC}	Analog Ground
14	V_{CC1}	Analog Ground
15	V_{EE}	Digital V_{EE}
16	DATAIN	Differential Data Input
17	$\overline{\text{DATAIN}}$	Differential Data Input
18	SUBST	Digital Substrate
19	$\overline{\text{FRAC}}$	Differential Frequency Acquisition Indicator Output
20	FRAC	Differential Frequency Acquisition Indicator Output

7

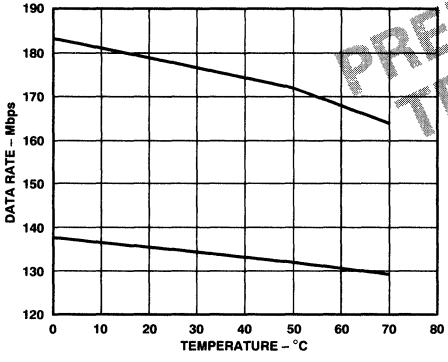
AD800/AD802—Typical Characteristics



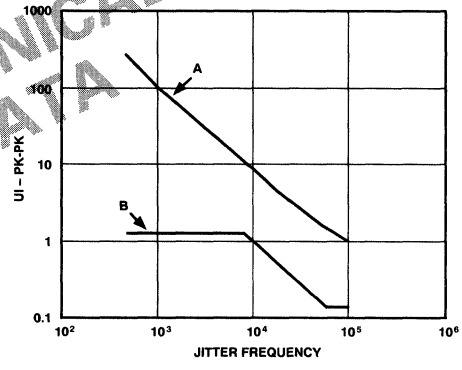
AD802-155 Center Frequency vs. Temperature



AD800/AD802 Output Jitter vs. Temperature



AD802-155 Capture Range, Tracking Range vs. Temperature



A: AD802-155 JITTER TOLERANCE, 2^7-1 PRN SEQUENCE INPUT
B: CCITT G958 STM1 TYPE A JITTER TOLERANCE MASK

Jitter Tolerance

ANALOG DEVICES

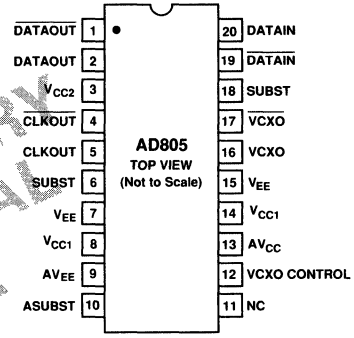
Clock Recovery and Data Retiming Phase-Locked Loop with Flat Jitter Response

AD805

FEATURES
155 Mbps Clock Recovery and Data Retiming
Flat Jitter Response
Acquisition: 40 Bit Periods
Accepts NRZ Data without Preamble
Single Supply Operation
ECL 10 KH Input and Output Levels
Random Jitter: 2° rms
Pattern Jitter: Virtually Eliminated

APPLICATIONS
Clock Recovery and Data Retiming for Sonet STS3 (155.52 MHz)
155 Mbps Data Deskewing
Large Factor Frequency Multiplication

PIN CONFIGURATION
20-Pin Ceramic DIP (D) Package



NOTES:
*PINS 6 AND 18 ARE DIGITAL SUBSTRATE AND SHOULD BE CONNECTED TO PINS 7 AND 15, WHICH ARE DIGITAL V_{EE}.
* PIN 10 IS ANALOG SUBSTRATE AND SHOULD BE CONNECTED TO PIN 9, WHICH IS ANALOG V_{EE}.

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PRODUCT DESCRIPTION

The AD805 provides truly flat jitter response clock recovery and data retiming from an NRZ-encoded data stream in conjunction with a VCXO operating at 155.52 MHz. The device uses 10 KH ECL levels and consumes 350 mW from a −5.2 V power supply. The VCXO is the only external component required.

The AD805 employs an architecture (patented) that guarantees a flat jitter transfer function, that is, no jitter peaking. The jitter peaking associated with traditional PLL-based clock recovery and data retiming circuits places an upper limit on the number of PLL-based regenerators in a path.

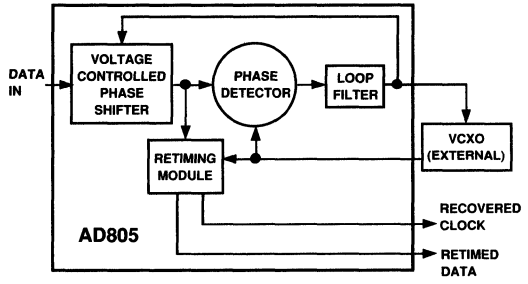
The AD805 also exhibits virtually no pattern jitter (<0.5° p–p) due to a newly developed phase detector (patented).

The clock recovery and data retiming application for the AD805 requires a VCXO with a gain of 1 Mrad/v-s, a positive slope, and a modulation bandwidth greater than 100 kHz. The AD805 tolerates wideband input jitter while simultaneously attenuating high frequency jitter in this application. The circuit acquires lock quickly (in 40 bit periods), unlike traditional PLL-based circuits, and provides a clock output even in the absence of input data, unlike Surface Acoustic Wave (or other resonant) filter based circuits.

The AD805 can be used for deskewing data, that is, retiming the data to a reference clock. The AD805 will deskew data that differs ±1/2 unit interval. The device's high operating frequency, low jitter, and unique phase detector make it suitable as a building block for such demanding phase-lock loop applications as frequency multiplication by a large factor (e.g., 19.44 MHz multiplication by eight to 155.52 MHz).

The AD805 is specified for operation over the industrial temperature range of −40°C to +85°C, and is available in 20-pin SOIC or side-brazed ceramic DIP.

Consult the factory for availability of the AD805 for other bit rates.



Clock Recovery and Data Retiming Application

AD805—SPECIFICATIONS (V_{EE} = −5.2 V, T_A = +25°C unless otherwise noted)

Parameter	Condition	Min	Typ	Max	Units
TRACKING RANGE[1]					
STATIC PHASE ERROR	ρ = 1[2]		23	TBD	Degree
CLOCK PHASE DRIFT[3]	20 Bit Periods			0.72	Degree
	60 Bit Periods			2.2	Degree
JITTER	ρ = 1		2	TBD	Degree rms
	ρ = 1/2		2		Degree rms
	2^7–1 PRN Sequence		2		Degree rms
	2^{23}–1 PRN Sequence			TBD	Degree rms
JITTER TOLERANCE	500 Hz	2.1	15		Unit Intervals
	6.5 kHz	1.5	3		Unit Intervals
	65 kHz	0.21	2		Unit Intervals
	1.3 MHz	0.15	0.7		Unit Intervals
JITTER TRANSFER					
Peaking				0	dB
Bandwidth			15.5		kHz
ACQUISITION TIME[4]	ρ = 1/2			40	Bit Periods
POWER SUPPLY					
Voltage		−4.5		−5.5	Volts
Current			70	TBD	mA
INPUT VOLTAGE LEVELS	V_{EE} = −5.2, V_{CC} = GND				
Input Logic High, V_{IH}		−1.13		−0.81	Volts
Input Logic Low, V_{IL}		−1.95		−1.63	Volts
OUTPUT VOLTAGE LEVELS	V_{EE} = −5.2, V_{CC} = GND				
Output Logic High, V_{OH}		−0.98		−0.81	Volts
Output Logic Low, V_{OL}		−1.95		−1.63	Volts
INPUT CURRENT LEVELS	V_{EE} = −5.2, V_{CC} = GND				
Input Logic High, I_{IH}		25		62	μA
Input Logic Low, I_{IL}		15		39	μA
OUTPUT SLEW TIMES					
Rise Time (t_R)	20%–80%		1.5		ns
Fall Time (t_F)	80%–20%		1.5		ns
SYMMETRY (DUTY CYCLE)[5]	ρ = 1/2				
Recovered Clock Output				51	%

NOTES
[1]Tracking Range: VCXO characteristics determine tracking range.
[2]ρ: input data transition density, (0<ρ<1).
[3]Clock Phase Drift: This parameter is measured with input data without transitions for the given number of bit periods.
[4]Acquisition Time: This parameter is measured with a control voltage within its extremes.
[5]Symmetry is calculated as (100 × on time)/period, where on time equals the time that the clock signal is greater than the midpoint between its "0" level and its "1" level.

Specifications subject to change without notice.

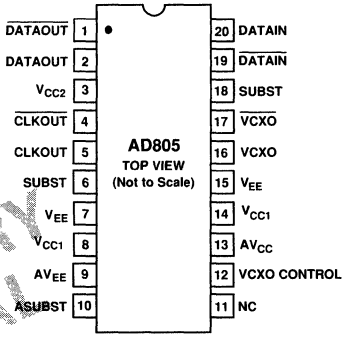
ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (Relative to V_{CC}) . . . . . −7.5 V
Input Voltage (Pins 19 or 20 to V_{EE}) . . . . −3 V to +300 mV
Storage Temperature Range . . . . . −65°C to +150°C
Ambient Temperature Range
Rated Performance . . . . . −40°C to +85°C
Lead Temperature (Soldering 60 sec) . . . . . +300°C

*A stress beyond any absolute maximum rating may cause permanent damage to the device. An absolute maximum rating is a stress rating only; functional operation of the device at or beyond an absolute maximum rating is not implied. Exposure to any absolute maximum rating condition for an extended period may adversely affect device reliability.

PIN CONFIGURATION

20-Pin Ceramic DIP (D) Package



NOTES:
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* PIN 10 IS ANALOG SUBSTRATE AND SHOULD BE CONNECTED TO PIN 9, WHICH IS ANALOG V_{EE}.

7

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

THEORY OF OPERATION

The AD805 (patented) is a phase-locked loop circuit for recovery of clock from an NRZ-encoded data stream. Figure 1 is a block diagram of the device shown with an external VCXO. Note that the AD805 employs a voltage controlled phase shifter (VCPS). This element implements the zero that is required to stabilize any second-order loop, but places it in the feedback path so that the zero does not appear in the closed-loop transfer function. Jitter peaking in conventional PLLs is caused by the presence of this zero in the closed-loop transfer function, and the AD805, therefore, is free of this problem.

Placing the zero in the feedback path results in a number of other advantages: the closed-loop bandwidth (which controls jitter filtering) and the loop transmission crossover frequency (which controls acquisition) can be very different. That is, the AD805's architecture simultaneously accommodates exceptionally low closed-loop bandwidths for good jitter filtering and large crossover frequencies needed for rapid acquisition. The AD805 thus typically acquires in 40 bit periods while possessing a closed-loop bandwidth that is only 100 ppm of the bit rate.

Jitter caused by variations in data transition density (pattern jitter) is virtually eliminated by the use of a new phase detector (patented). Briefly, the measurement of zero phase error does not cause the VCXO phase to increase above the average run rate set by the data frequency. The peak-to-peak pattern jitter created by a 27-1 pseudorandom code is less than one-half degree, and is not detectable against the random background jitter of approximately 2° rms.

The bandwidth of the AD805 is mask-programmable. The nominal closed-loop bandwidth and crossover frequency are chosen to be compatible with the requirements of a wide variety of systems, such as those conforming to SONET OC-3 specifications. Contact the factory for other requirements.

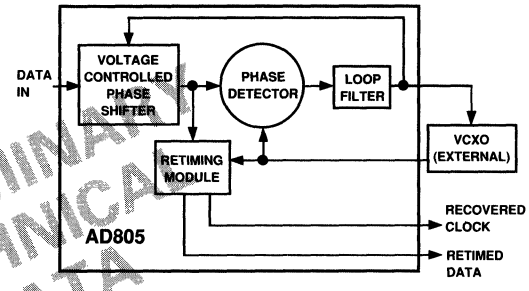


Figure 1. FJR PLL Block Diagram

ANALOG DEVICES

Monolithic Accelerometer with Signal Conditioning

ADXL50*

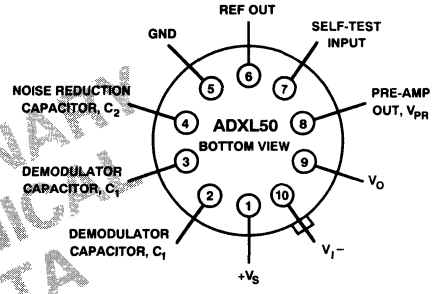
FEATURES

Full-Scale Measurement Range: ±50 g
Self-Test on Digital Command
Single Supply Operation: +5 V to +24 V
Output Range: 0.25 V to 4.75 V
Accuracy of Span: 8% over −55°C to +125°C
Uncommitted Output Amplifier for Custom Scaling and Zero-g Level Adjustment
Programmable Bandwidth: DC up to 1 kHz
Additional Filtering: 2-Pole with External Passive Components
High Shock Survival: >2000 g Unpowered

APPLICATIONS

Crash Detection for Airbag Deployment and Seatbelt Retraction
Vibration Analysis and Cancellation
Measurement, Characterization and Instrumentation, e.g., Crash Dummies

PIN CONFIGURATIONS
(TO-100 Metal Can)



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GENERAL DESCRIPTION

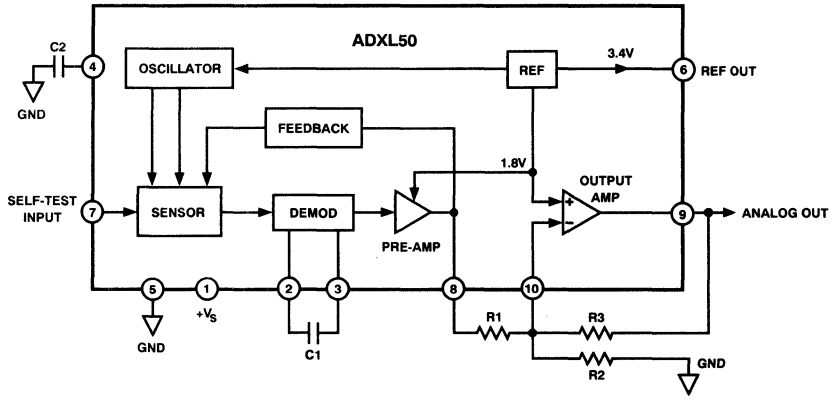
The ADXL50 is a monolithic accelerometer which combines a polysilicon micromachined sensor with signal conditioning and signal processing circuitry. It is capable of measuring both positive and negative acceleration in the ±50 g range, offering a bandwidth of dc up to 1 kHz.

The ADXL50 uses a capacitive measurement scheme. The analog output is directly proportional to acceleration, and is fully scaled, referenced and temperature compensated resulting in high accuracy and linearity over the automotive temperature range.

A digitally commandable self-test allows the sensor beam to be electrostatically deflected at any time, producing an output voltage which corresponds to the −50 g output of a healthy sensor beam.

*Patents pending.

FUNCTIONAL BLOCK DIAGRAM



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

ADXL50—SPECIFICATIONS (T_A = +25°C and V_S = +5 V, unless otherwise noted.)

Parameter	Test Conditions	Min	Typ	Max	Units
INPUT					
Measurement Range[1]	T_{MIN} to T_{MAX}	−50		+50	g
Transverse Sensitivity	T_{MIN} to T_{MAX}			2	%
PREAMPLIFIER					
Zero-g Output	Applied Acceleration = 0 g	1.75	1.80	1.85	V
Sensitivity			20		mV/g
Full-Scale Output Span	Applied Acceleration = −50 g to +50 g	0.8		2.80	V
Output at Self-Test[2]	Pin 7 = "High"		0.80		V
Voltage Noise[6]	At Bandwidth = 0.3 kHz		±0.33		% FS
	At Bandwidth = 1.0 kHz		±0.6		% FS
UNCOMMITTED AMPLIFIER					
Input Offset Voltage	T_{MIN} to T_{MAX}			±10	mV
Input Bias Current	T_{MIN} to T_{MAX}			10	nA
Open-Loop Gain		100			dB
Output Swing	No Output Load	0.10		V_S−0.1	V
Output Swing	Output Current = 100 μA	0.25		4.75	V
Capacitive Load				1000	pF
ACCURACY					
Initial Accuracy			5		% FS
Overall Accuracy of Span	T_{MIN} to T_{MAX}		8		% FS
LINEARITY					
Overall Linearity	T_{MIN} to T_{MAX}		0.5		% FS
FREQUENCY RESPONSE					
Bandwidth[3]	C_1 = 25 nF (See Figure 1)		1		kHz
Resonant Frequency[4]			22		kHz
REFERENCE					
Output Voltage		3.395	3.400	3.405	V
Output Voltage Drift	T_{MIN} to T_{MAX}			50	ppm/°C
Power Supply Rejection (DC)		60			dB
Output Current				500	μA
POWER SUPPLY					
Operating Voltage[5]		+4.75	+5	+5.25	V
Quiescent Supply Current			10	13	mA
TEMPERATURE					
Operating Range	T_{MIN} to T_{MAX}	−55		+125	°C
PACKAGE	Metal Can Side Brazed Ceramic		ADXL50H ADXL50D		

NOTES

[1]Positive acceleration, causing the output of the preamplifier to rise, is defined as follows: Header Package: acceleration in the plane of Pins 5 and 10, towards Pin 10. Pin 10 is identified by the metal tab (see "PIN CONFIGURATIONS" diagram). Ceramic Package: acceleration in the plane of the package, towards the end of the package containing the notch.

[2]Applying +5 V to the self-test input has an effect on the acceleration sensing element equivalent to applying an acceleration of −50 g to the ADXL50.

[3]The bandwidth is user-programmable, and set by an external capacitor (C_1 in Figure 1). C_1 = 25 nF sets the −3 dB point at 1 kHz, the maximum recommended measurement frequency. The bandwidth is inversely proportional to C_1.

[4]With the bandwidth set at the recommended maximum (i.e., 1 kHz), the beam resonant frequency produces a peak at 3× below the passband signal level.

[5]The ADXL50 is guaranteed to meet the above specifications operating from a supply of +5 V ± 5%. It will continue to operate, and will suffer no permanent damage, from a supply as high as +24 V (see "Absolute Maximum Ratings").

[6]A noise reduction capacitor, C_N = 16 nF, must be connected from Pin 4 to ground.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Acceleration (Any Axis) . . . . . 2000 g
$+V_S$ . . . . . +24 V
Output Short Circuit Duration . . . . . Indefinite
Operating Temperature . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

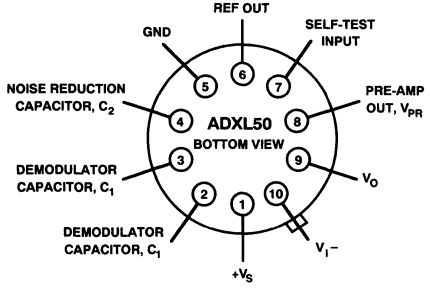
PIN DESIGNATIONS

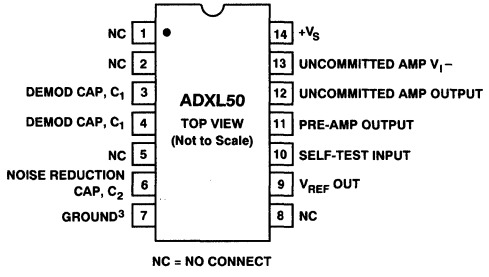
10-Pin Metal Can

Pin	Function
1	$+V_S$
2	Demod Cap, C_1
3	Demod Cap, C_1
4	Noise Reduction Cap, C_2
5	Ground[1]
6	V_{REF} Out
7	Self-Test Input
8	Pre-Amp Output
9	Uncommitted Amp Output
10	Uncommitted Amp V_I-

14-Pin Ceramic

Pin	Function
1	NC[2]
2	NC
3	Demod Cap, C_1
4	Demod Cap, C_1
5	NC
6	Noise Reduction Cap, C_2
7	Ground[3]
8	NC
9	V_{REF} Out
10	Self-Test Input
11	Pre-Amp Output
12	Uncommitted Amp Output
13	Uncommitted Amp Vi−
14	$+V_S$





NOTES
[1]The case of the metal can package is connected to Pin 5, Ground.
[2]"NC" designates that the pin is unconnected internally.
[3]The lid of the side brazed ceramic package is connected to Pin 7, Ground.

ADXL50 PRODUCT DESCRIPTION

The ADXL50's novel architecture merges surface micromachined polysilicon with BiMOS circuitry and laser wafer-trimmed thin-film resistors. The sensor is a differential capacitor so it is inherently stable over temperature. Analog's expertise in signal conditioning, along with the large portfolio of proven BiMOS circuits, allow the ADXL50 to be fully scaled, referenced and temperature compensated. No external active components are required to interface directly to an ADC.

For additional flexibility, the ADXL50 has an uncommitted output amplifier for user programming of the output zero-g level, scaling, and filtering. The output span of the ADXL50's preamp is 1.8 V ±1.0 V at ±50 g. The uncommitted output amplifier allows the user to adjust the zero-g level and output span (up to 0.25 V to 4.75 V) by adding external resistors. External capacitors may be added to the resistor network for 1 or 2 poles of filtering.

The ADXL50 can be powered from a standard +5 V supply and is robust enough to survive harsh automotive conditions and shocks of more than 2000 g unpowered. The structure of the ADXL50 is intrinsically more stable over temperature than piezoelectric or piezoresistive techniques.

SELF TEST FEATURE

The ADXL50 employs on-chip test circuits for a self-test at any time. The tight mechanical spacings on the sensor allow electrostatic manipulation of the beam structure with a +5 V supply. With a digital input to begin the ADXL50's self-test, the beam is deflected in a controlled manner resulting in an output which is within 5% of the specified negative full-scale output.

APPLICATIONS

AMPLIFYING AND OFFSET SHIFTING THE PREAMP SIGNAL

The unconditioned output of the ADXL50's preamplifier is 1.8 V at 0 g acceleration with a span of ±1.0 V for ±50 g input, i.e., 20 mV/g. An uncommitted output amplifier has been included on the chip to enhance the user's ability to offset the 0 g level and to amplify and filter the signal. In Figure 1, it can be seen that access is provided to the inverting input and the output of this amplifier via Pins 10 and 9, respectively, while the noninverting input is connected internally to +1.8 V, which is derived from the on-chip 3.4 V reference.

The scaling factor in the configuration shown is given by $-R_3/R_1$ (since the amplifier is in inverter mode) and the offset is provided by R_2. Therefore, if the span desired is ±2.25 V for the ±50 g input, then R_3/R_1 should be chosen such that

$$\frac{R_3}{R_1} = \frac{V_O\ span}{V_{PR}\ span} = \frac{2.25}{1.0} \quad (1)$$

where V_{PR} span is the output from the preamplifier and V_O span is the uncommitted amplifier's output, giving

$$R_3 = 2.25 \times R_1 \quad (2)$$

R_2 can then be found from the following equation, derived from standard amplifier theory:

$$R_2 = \frac{1.8 \times R_3}{V_{oo} - 1.8} \quad (3)$$

where V_{oo} is the desired 0 g output level.

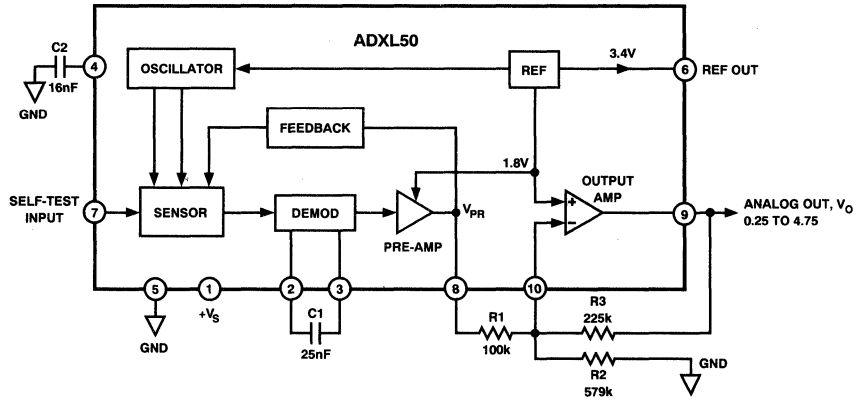


Figure 1. Connections to Be Made to the ADXL50 to Provide an Analog Signal of 0.25 V to 4.75 V, with a Bandwidth of 1 kHz

To provide an output span of ±2.25 V, with a 0 g output of +2.5 V, then R_1 could be set at 100 kΩ. From Equation 2, R_3 = 225 kΩ, and using Equation 3, R_2 = 579 kΩ.

A general transfer function for the circuit, given by the resistor configuration shown, is:

$$V_O = (1.8 - V_{PR})\frac{R_3}{R_1} + 1.8\left(1 + \frac{R_3}{R_2}\right)$$

which for the resistor values given reduces to:

$$V_O = (1.8 - V_{PR})\,2.25 + 2.50$$

FILTERING THE PREAMP SIGNAL

The uncommitted output amplifier can also be used to filter the signal, if more filtering is required than the 1 pole inherently provided at 1 kHz by the 25 nF demodulation capacitor. The circuit shown in Figure 2, which gives a gain of 3.94, provides an extra 3 poles of filtering at 200 Hz, without using any external active components.

ADXL FAMILY

Analog Devices' ADXL family of accelerometers provides a fully conditioned analog output voltage proportional to acceleration. The family is expected to include accelerometers with measurement ranges from ±2 g up to ±500 g. There are products planned with dual axis and redundant sensing.

The product features of the ADXL series make them ideal for automotive applications such as crash detection/airbag deployment, antilock brake systems, active suspension, and vibration analysis and suppression.

REDUNDANCY

Multiple sensors on the same IC are possible with the ADXL50's architecture due to the small size of the sensor itself and the high density of the BiMOS circuitry. Monolithic dual axis accelerometers can be made by placing the sensors orthogonally on the die. Some sharing of the support circuitry will provide even greater economic value.

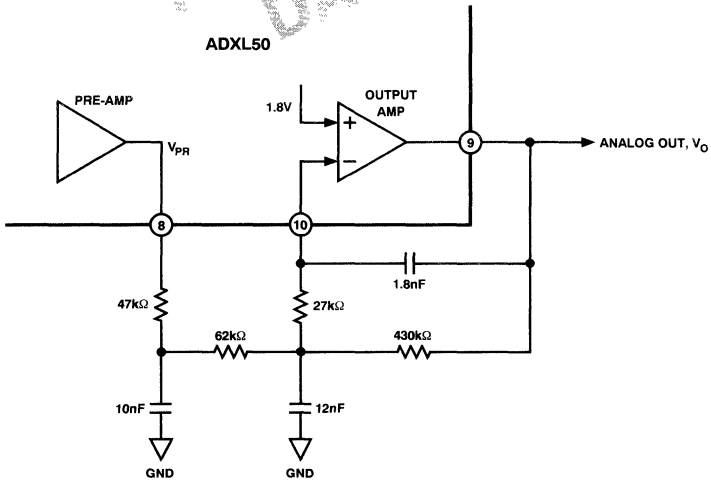


Figure 2. Using the Uncommitted Output Amplifier to Provide an Extra 2 Poles of Filtering, with a Gain of 3.94

ANALOG DEVICES

Monolithic Peak Detector with Reset-and-Hold Mode

PKD-01

FEATURES

- **Monolithic Design for Reliability and Low Cost**
- **High Slew Rate** **0.5V/μs**
- **Low Droop Rate**
  - $T_A = 25°C$ **0.1mV/ms**
  - $T_A = 125°C$ **10mV/ms**
- **Low Zero-Scale Error** **4mV**
- **Digitally Selected Hold and Reset Modes**
- **Reset to Positive or Negative Voltage Levels**
- **Logic Signals TTL and CMOS Compatible**
- **Uncommitted Comparator on Chip**
- **Available in Die Form**

ORDERING INFORMATION†

25°C V_{ZS} (mV)	PACKAGE 14-PIN DUAL-IN-LINE PACKAGE HERMETIC*	PLASTIC	OPERATING TEMPERATURE RANGE
4	PKD01AY*	—	MIL
4	PKD01EY	—	IND
7	PKD01FY	—	IND
4	—	PKD01EP	COM
7	—	PKD01FP	COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The PKD-01 tracks an analog input signal until a maximum amplitude is reached. The maximum value is then retained as a peak voltage on a hold capacitor. Being a monolithic circuit, the PKD-01 offers significant performance and package density advantages over hybrid modules and discrete designs without sacrificing system versatility. The matching characteristics attained in a monolithic circuit provide inherent advantages when charge injection and droop rate error reduction are primary goals.

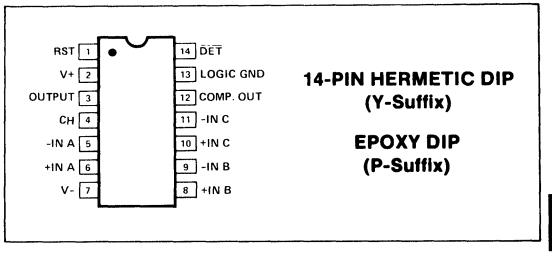
Innovative design techniques maximize the advantages of monolithic technology. Transconductance (g_m) amplifiers were chosen over conventional voltage amplifier circuit building blocks. The "g_m" amplifiers simplify internal frequency compensation, minimize acquisition time and maximize circuit accuracy. Their outputs are easily switched by low glitch current steering circuits. The steered outputs are clamped to reduce charge injection errors upon entering the hold mode or exiting the reset mode. The inherently low zero-scale error is reduced further by active "Zener-Zap" trimming to optimize overall accuracy.

The output buffer amplifier features an FET input stage to reduce droop rate error during lengthy peak hold periods. A bias current cancellation circuit minimizes droop error at high ambient temperatures.

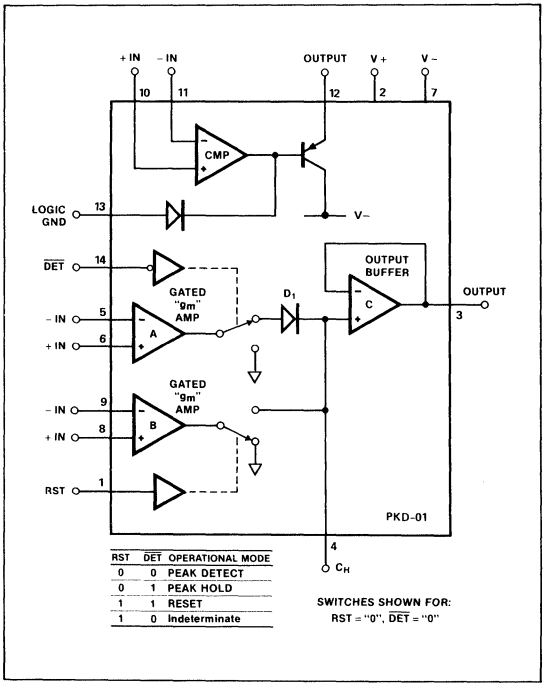
Through the $\overline{DET}$ control pin, new peaks may either be detected or ignored. Detected peaks are presented as positive output levels. Positive or negative peaks may be detected without additional active circuits since amplifier A can operate as an inverting or noninverting gain stage.

An uncommitted comparator provides many application options. Status indication and logic shaping/shifting are typical examples.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



RST	DET	OPERATIONAL MODE
0	0	PEAK DETECT
0	1	PEAK HOLD
1	1	RESET
1	0	Indeterminate

7

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Ground
Voltage ..... Equal to Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Amplifier A or B Differential Input Voltage ..... ±24V
Comparator Differential Input Voltage ..... ±24V
Comparator Output Voltage
..... Equal to Positive Supply Voltage
Hold Capacitor Short-Circuit Duration ..... Indefinite
Lead Temperature (Soldering, 60 sec) ..... 300°C
Storage Temperature Range
PKD-01AY, PKD-01EY, PKD-01FY ..... –65°C to +150°C
PKD-01EP, PKD-01FP ..... –65°C to +125°C
Operating Temperature Range
PKD-01AY ..... –55°C to +125°C
PKD-01EY, PKD-01FY ..... –25°C to +85°C
PKD-01EP, PKD-01FP ..... 0°C to +70°C
Junction Temperature ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E MIN	PKD-01A/E TYP	PKD-01A/E MAX	PKD-01F MIN	PKD-01F TYP	PKD-01F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	2	4	—	3	7	mV
Input Offset Voltage	V_{OS}		—	2	3	—	3	6	mV
Input Bias Current	I_B		—	80	150	—	80	250	nA
Input Offset Current	I_{OS}		—	20	40	—	20	75	nA
Voltage Gain	A_V	$R_L = 10k\Omega$, $V_O = \pm10V$	18	25	—	10	25	—	V/mV
Open-Loop Bandwidth	BW	$A_V = 1$	—	0.4	—	—	0.4	—	MHz
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	$\pm9V \le V_S \le \pm18V$	86	96	—	76	96	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±10	±11	—	±10	±11	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/μs
Feedthrough Error		$\Delta V_{IN} = 20V$, DET = 1, RST = 0, (Note 1)	66	80	—	66	80	—	dB
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$, (Note 1)	—	41	70	—	41	70	μs
Acquisition Time to 0.01% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$, (Note 1)	—	45	—	—	45	—	μs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	0.5	1.5	—	1	3	mV
Input Bias Current	I_B		—	700	1000	—	700	1000	nA
Input Offset Current	I_{OS}		—	75	300	—	75	300	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V	5	7.5	—	3.5	7.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	$\pm9V \le V_S \le \pm18V$	76	90	—	76	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11.5	±12.5	—	±11.5	±12.5	—	V

NOTES:
1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, RST = 0.

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 1000pF$, $T_A = 25°C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E MIN	PKD-01A/E TYP	PKD-01A/E MAX	PKD-01F MIN	PKD-01F TYP	PKD-01F MAX	UNITS
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	µA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	7	12	45	7	12	45	mA
Response Time	t_S	5mV Overdrive, (Note 3) 2kΩ Pull-up Resistor to 5V	—	150	—	—	150	—	ns
DIGITAL INPUTS-RST, $\overline{DET}$ (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	µA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	1.6	10	µA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_j = 25°C$, (See Note 2) $T_A = 25°C$ (See Note 2)	— —	0.01 0.02	0.07 0.15	— —	0.01 0.03	0.1 0.20	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$\overline{DET} = 1$ $R_L = 2.5k$	±11.5	±12.5	—	±11	±12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Switch Switching Time	ts		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/µs
Power Supply Current	I_{SY}	No Load	—	5	7	—	6	9	mA

ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $C_H = 1000pF$, $-55°C \leq T_A \leq +125°C$ for PKD-01AY, $-25°C \leq T_A \leq +85°C$ for PKD-01EY, PKD-01FY and $0°C \leq T_A \leq +70°C$ for PKD-01EP, PKD-01FP.

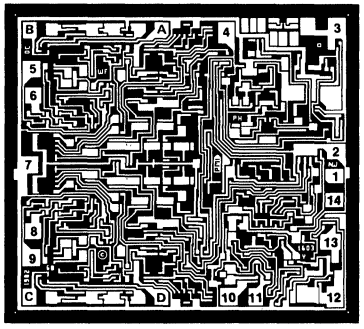
PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E MIN	PKD-01A/E TYP	PKD-01A/E MAX	PKD-01F MIN	PKD-01F TYP	PKD-01F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	4	7	—	6	12	mV
Input Offset Voltage	V_{OS}		—	3	6	—	5	10	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-9	-24	—	-9	-24	µV/°C
Input Bias Current	I_B		—	160	250	—	160	500	nA
Input Offset Current	I_{OS}		—	30	100	—	30	150	nA
Voltage Gain	A_V	$R_L = 10k\Omega$, $V_O = \pm10V$	7.5	9	—	5	9	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	$\pm9V \leq V_S \leq \pm18V$	80	90	—	70	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±10	±11	—	±10	±11	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/µs
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$, (Note 1)	—	60	—	—	60	—	µs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	2	2.5	—	2	5	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	-4	-6	—	-4	-6	µV/°C
Input Bias Current	I_B		—	1000	2000	—	1100	2000	nA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55°C \le T_A \le +125°C$ for PKD-01AY, $-25°C \le T_A \le +85°C$ for PKD-01EY, PKD-01FY and $0°C \le T_A \le +70°C$ for PKD-01EP, PKD-01FP. *Continued*

			PKD-01A/E			PKD-01F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V	4	6.5	—	2.5	6.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11	—	—	±11	—	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	100	180	μA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	6	10	45	6	10	45	mA
Response Time	t_S	5mV Overdrive, 2kΩ Pull-up Resistor to 5V	—	200	—	—	200	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	T_j = Max. Operating Temp T_A = Max. Operating Temp. DET = 1, (Note 2)	— —	1.2 2.4	10 20	— —	3 6	15 20	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11	±12	—	±10.5	±12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2	—	—	2	—	V/μs
Power Supply Current	I_{SY}	No Load	—	5.5	8	—	6.5	10	mA

NOTES:
1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, RST = 0.

DICE CHARACTERISTICS



1. RST (RESET CONTROL)
2. V+
3. OUTPUT
4. C_H (HOLD CAPACITOR)
5. INVERTING INPUT (A)
6. NONINVERTING INPUT (A)
7. V−
8. NONINVERTING INPUT (B)
9. INVERTING INPUT (B)
10. COMPARATOR NONINVERTING INPUT
11. COMPARATOR INVERTING INPUT
12. COMPARATOR OUTPUT
13. LOGIC GROUND
14. $\overline{\text{DET}}$ (PEAK DETECT CONTROL)

A,B (A) NULL
C,D (B) NULL

DIE SIZE 0.101 × 0.091 inch, 9191 sq. mils
(2.565 × 2.311mm, 5.93 sq mm)

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V_{ZS}		7	mV MAX
Input Offset Voltage	V_{OS}		6	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		75	nA MAX
Voltage Gain	A_V	$R_L = 10k\Omega$, $V_O = \pm 10V$	10	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, $\overline{\text{DET}} = 1$, RST = 0, (Note 1)	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V, (Note 1)	3.5	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	±11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 5V	0.4 −0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	μA MAX
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7	mA MAX mA MIN

NOTES:
1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{\text{DET}} = 1$, RST = 0.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
DIGITAL INPUTS-RST, DET (See Note 3)				
Logic "1" Input Voltage	V_H		2	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1	μA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	μA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$T_j = 25°C$, (See Note 2) $T_A = 25°C$	0.1 0.20	mV/ms MAX mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11	V MIN
Short-Circuit Current: Amplifier C	I_{SC}		40 7	mA MAX mA MIN
Power Supply Current	I_{SY}	No Load	9	mA MAX

NOTES:

1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures. Ambient (T_A) temperature specifications are not subject to production testing.
3. $\overline{DET} = 1$, $RST = 0$.

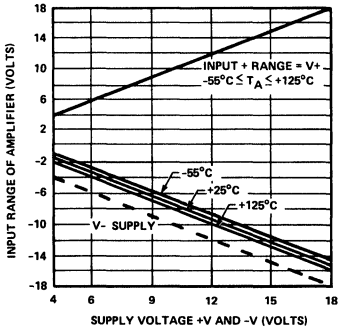
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, and $T_A = 25°C$, unless otherwise noted.

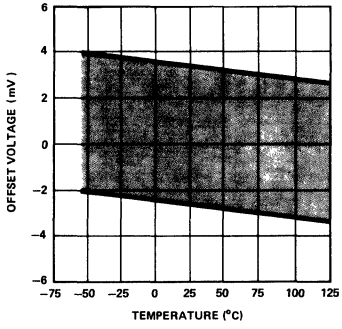
PARAMETER	SYMBOL	CONDITIONS	PKD-01N TYPICAL	UNITS
"g_m" AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/μs
Acquisition Time	t_a	0.1% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	41	μs
Acquisition Time	t_a	0.01% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	45	μs
COMPARATOR				
Response Time		5mV Overdrive, 2kΩ Pull-up Resistor to +5V	150	ns
MISCELLANEOUS				
Switch Aperature Time	t_{ap}		75	ns
Switching Time	t_S		50	ns
Buffer Slew Rate	SR	$R_L = 2.5k\Omega$	2.5	V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

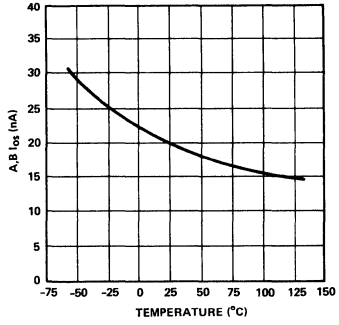
A AND B INPUT RANGE vs SUPPLY VOLTAGE



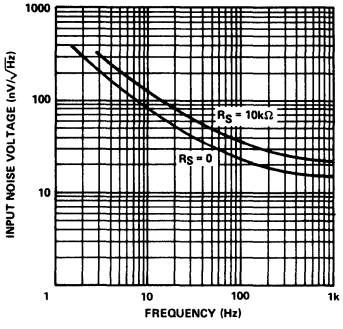
A AND B AMPLIFIERS OFFSET VOLTAGE vs TEMPERATURE



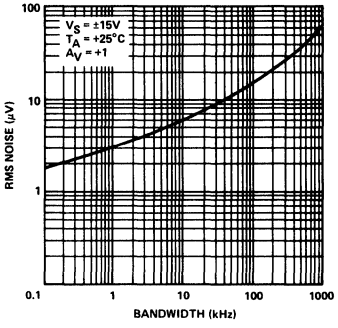
A, B I_{OS} vs TEMPERATURE



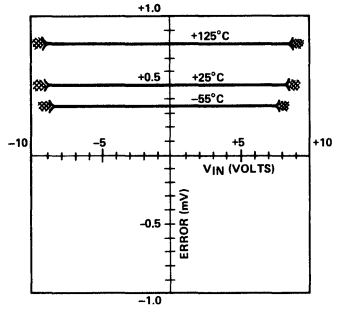
INPUT SPOT NOISE vs FREQUENCY



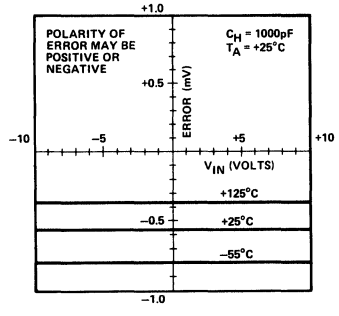
WIDEBAND NOISE vs BANDWIDTH



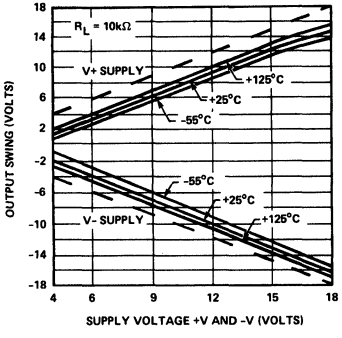
AMPLIFIER B CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE



AMPLIFIER A CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE

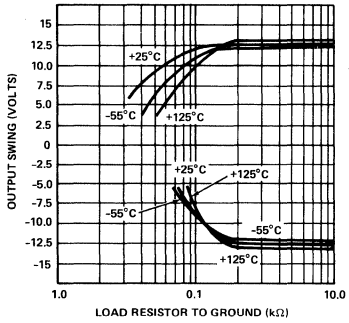


OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (DUAL SUPPLY OPERATION)

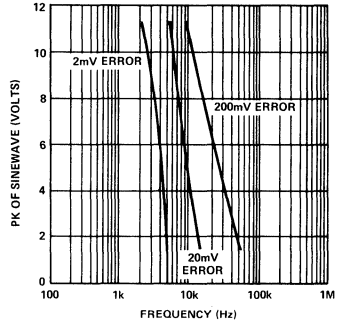


TYPICAL PERFORMANCE CHARACTERISTICS

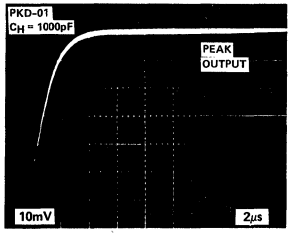
OUTPUT VOLTAGE vs LOAD RESISTANCE



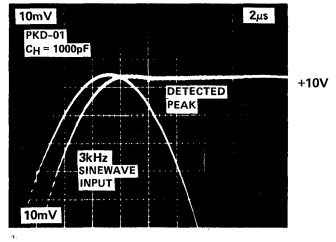
OUTPUT ERROR vs FREQUENCY AND INPUT VOLTAGE



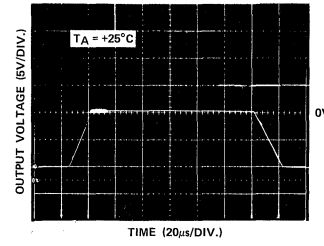
PKD-01 SETTLING RESPONSE



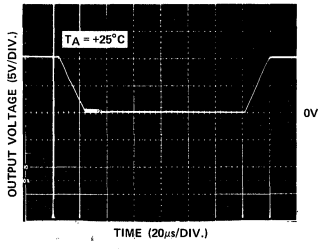
PKD-01 SETTLING RESPONSE



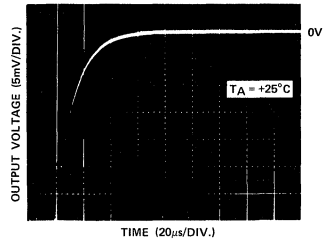
LARGE-SIGNAL INVERTING RESPONSE



LARGE-SIGNAL NONINVERTING RESPONSE



SETTLING TIME FOR −10V TO 0V STEP INPUT



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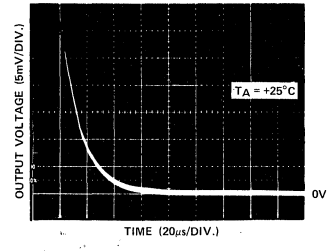
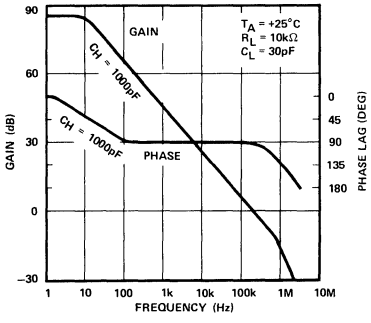
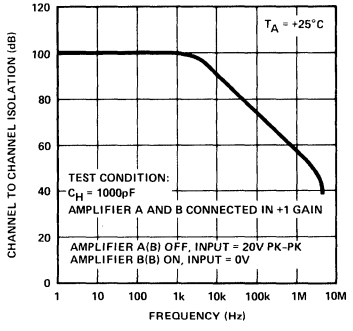


TYPICAL PERFORMANCE CHARACTERISTICS

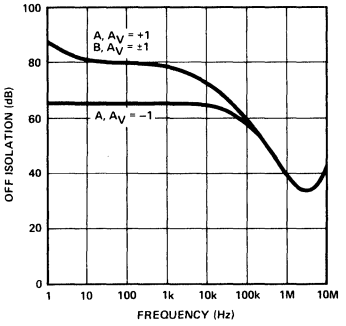
SMALL-SIGNAL OPEN LOOP GAIN/PHASE vs FREQUENCY



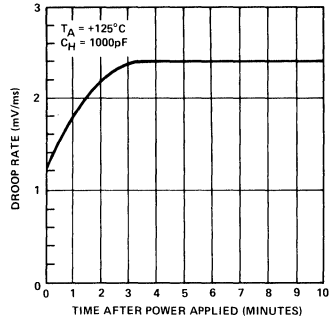
CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



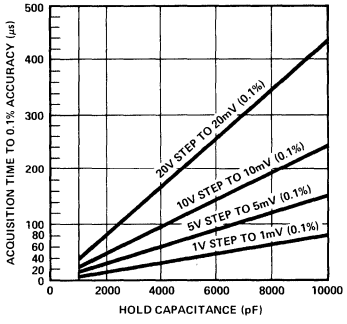
OFF ISOLATION vs FREQUENCY



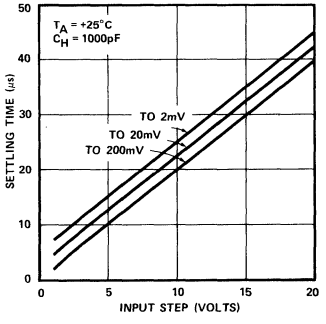
DROOP RATE vs TIME AFTER POWER ON



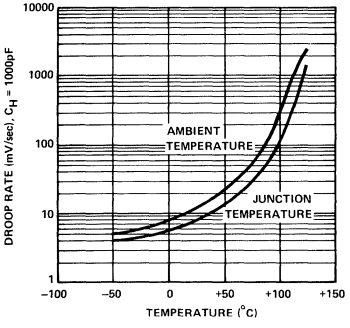
ACQUISITION TIME vs EXTERNAL HOLD CAPACITOR AND ACQUISITION STEP



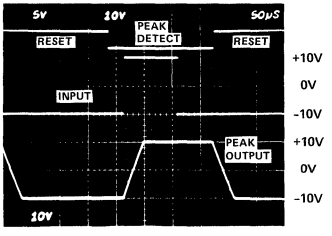
ACQUISITION TIME vs INPUT VOLTAGE STEP SIZE



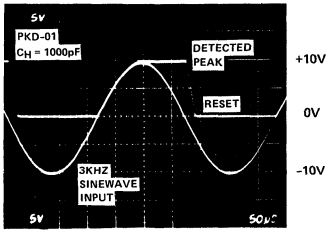
DROOP RATE vs TEMPERATURE



ACQUISITION OF STEP INPUT

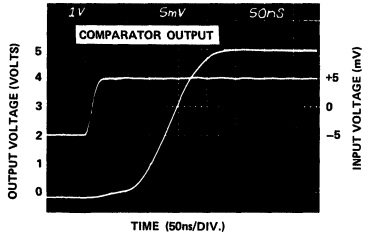


ACQUISITION OF SINEWAVE PEAK

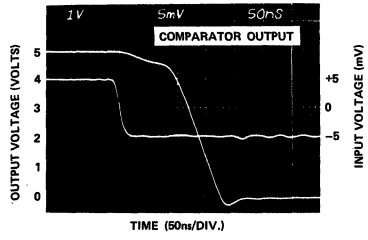


TYPICAL PERFORMANCE CHARACTERISTICS

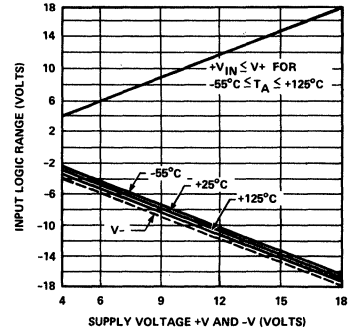
COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, T_A = +25°C)



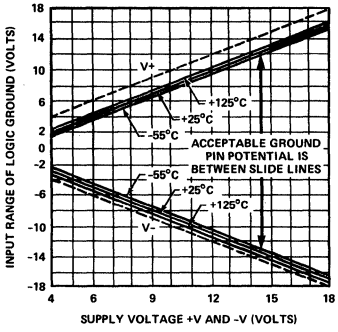
COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, T_A = +25°C)



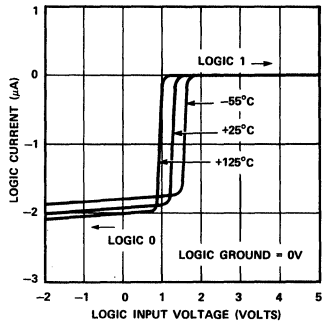
INPUT LOGIC RANGE vs SUPPLY VOLTAGE



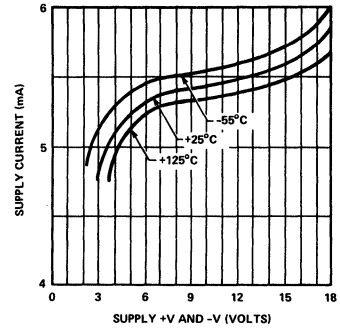
INPUT RANGE OF LOGIC GROUND vs SUPPLY VOLTAGE



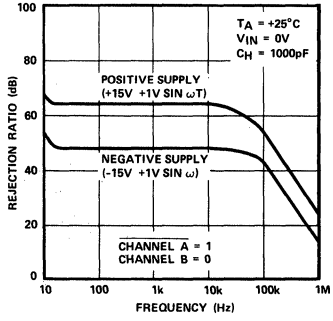
LOGIC INPUT CURRENT vs LOGIC INPUT VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE

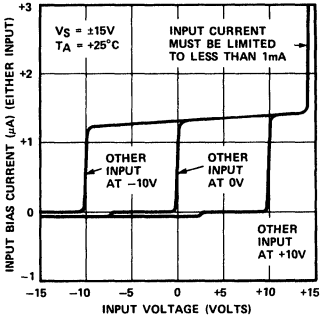


HOLD MODE POWER SUPPLY REJECTION vs FREQUENCY

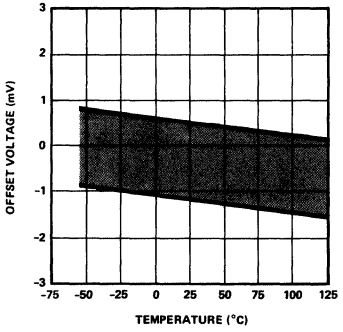


TYPICAL PERFORMANCE CHARACTERISTICS

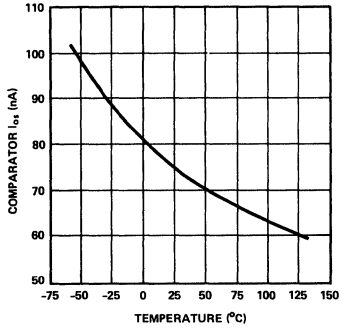
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



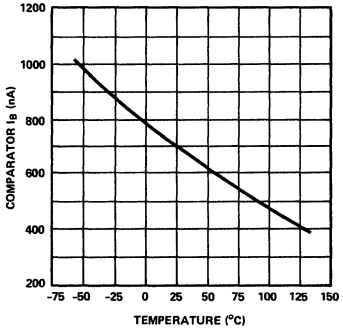
COMPARATOR OFFSET VOLTAGE vs TEMPERATURE



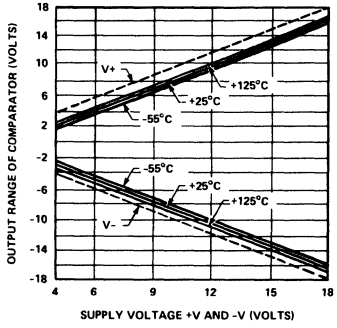
COMPARATOR I_{OS} vs TEMPERATURE



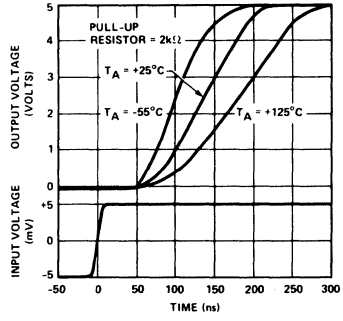
COMPARATOR I_B vs TEMPERATURE



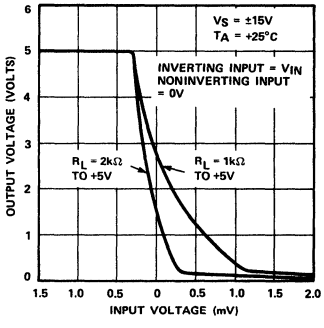
OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE



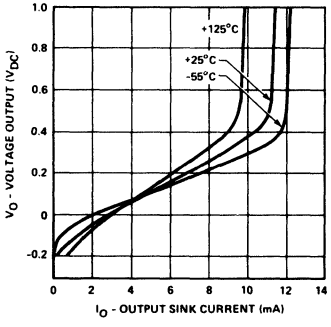
COMPARATOR RESPONSE TIME vs TEMPERATURE



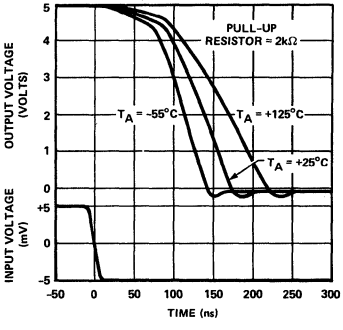
COMPARATOR TRANSFER CHARACTERISTIC



COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



COMPARATOR RESPONSE TIME vs TEMPERATURE



7

THEORY OF OPERATION

The typical peak detector uses voltage amplifiers and a diode or an emitter follower to charge the hold capacitor, C_H, unidirectionally (Figure 1). The output impedance of A plus D_1's dynamic impedance, r_d, make up the resistance which determines the feedback loop pole. The dynamic impedance is $r_d = \frac{kT}{qI_d}$. I_d is the capacitor charging current.

The pole moves toward the origin of the S plane as I_d goes to zero. The pole movement in itself will not significantly lengthen the acquisition time since the pole is enclosed in the system feedback loop.

When the moving pole is considered with the typical frequency compensation of voltage amplifiers there is however, a loop stability problem. The necessary compensation can increase the required acquisition time. PMI's approach replaces the input voltage amplifier with a transconductance amplifier; Figure 2.

The PKD-01 transfer function can be reduced to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + \frac{sC_H}{g_m} + \frac{1}{g_m R_{OUT}}} \approx \frac{1}{1 + \frac{sC_H}{g_m}}$$

Where: $g_m \approx 1\mu A/mV$, $R_{OUT} \approx 20M\Omega$.

The diode in series with A's output (Figure 2) has no effect because it is a resistance in series with a current source. In addition to simplifying the system compensation, the input transconductance amplifier output current is switched by current steering. The steered output is clamped to reduce and match any charge injection.

Fig. 3 shows a simplified schematic of the reset "g_m" amplifier, B. In the track mode, Q_1 & Q_4 are ON and Q_2 & Q_3 are OFF. A current of 2I passes through D_1, I is summed at "B" and passes through Q_1, and is summed with $g_m V_{IN}$. The current sink can absorb only 3I, thus, the current passing through D_2 can only be: $2K - g_m V_{IN}$. The net current into the hold capacitor node then, is $g_m V_{IN}$ ($C_H = 2I - (2I - g_m V_{IN})$. The hold mode, Q_2 & Q_3 are ON while Q_1 & Q_4 are OFF. The net current into the top of D_1 is $-I$ until D_3 turns ON. With Q_1 OFF, the bottom of D_2 is pulled up with a current I until D_4 turns ON, thus D_1 & D_2 are reverse biased by $\approx 0.6V$ and charge injection is independent of input level.

The monolithic layout results in points A and B having equal nodal capacitance. In addition, matched diodes D_1 and D_2 have equal diffusion capacitance. When the transconductance amplifier outputs are switched open, points A and B are ramped equally but in opposite phase. Diode clamps D_3 and D_4 cause the swings to have equal amplitudes. The net charge injection (voltage change) at node C is therefore zero.

The peak transconductance amplifier, A, is shown in Figure 4. Unidirectional hold capacitor charging requires diode D_1 to be connected in series with the output. Upon entering the peak hold mode D_1 is reverse biased. The voltage clamp limits charge injection to approximately 1pC and the hold step to 0.6mV.

Minimizing acquisition time dictated a small C_H capacitance. A 1000pF value was selected. Droop rate was also minimized by providing the output buffer with an FET input stage. A current cancellation circuit further reduces droop current and minimizes the gate current's tendency to double for every 10°C temperature change.

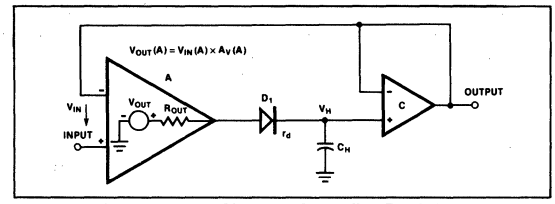


Figure 1. Conventional Voltage Amplifier Peak Detector

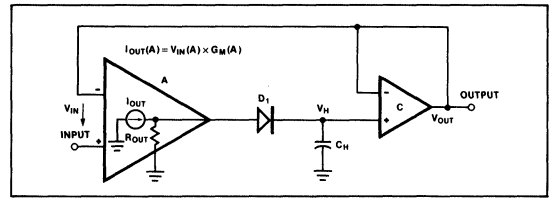


Figure 2. Transconductance Amplifier Peak Detector

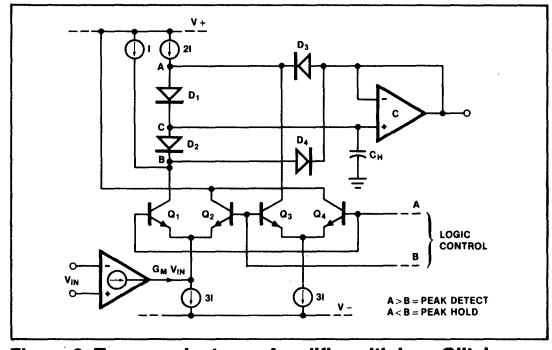


Figure 3. Transconductance Amplifier with Low Glitch Current Switch

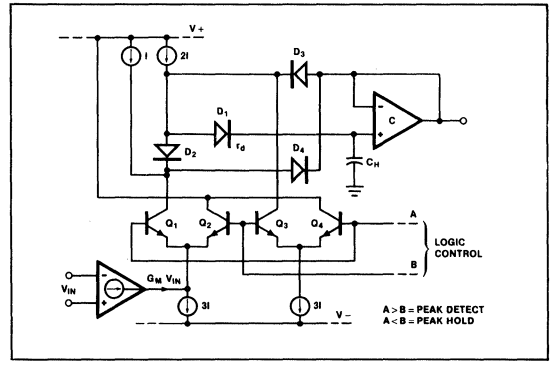


Figure 4. Peak Detecting Transconductance Amplifier with Switched Output

APPLICATIONS INFORMATION

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

Offset voltage is the primary zero scale error component since a variable voltage clamp limits voltage excursions at D_1's anode and reduces charge injection. The PKD-01 circuit gain and operational mode (positive or negative peak detection) determine the applicable null circuit. Figures A through D are suggested circuits. Each circuit corrects amplifier C offset voltage error also.

A. NULLING GATED OUTPUT g_m AMPLIFIER A. Diode D_1 must be conducting to close the feedback circuit during amplifier A V_{OS} adjustment. Resistor network $R_A - R_C$ cause D_1 to conduct slightly. With DET = 0 and V_{IN} = 0V monitor the PKD-01 output. Adjust the null potentiometer until V_{OUT} = 0V. After adjustment, disconnect R_C from C_H.

B. NULLING GATED g_m AMPLIFIER B. Set amplifier B signal input to V_{IN} = 0V and monitor the PKD-01 output. Set DET = 1, RST = 1 and adjust the null potentiometer for V_{OUT} = 0V. The circuit gain — inverting or noninverting — will determine which null circuit illustrated in Figures A through D is applicable.

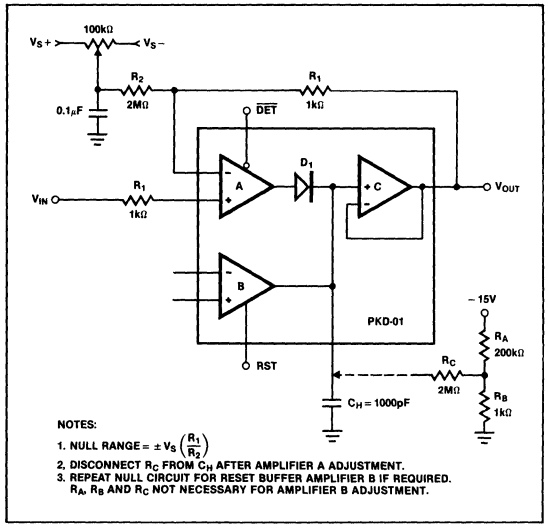


Figure A. V_{OS} Null Circuit for Unity Gain Positive Peak Detector

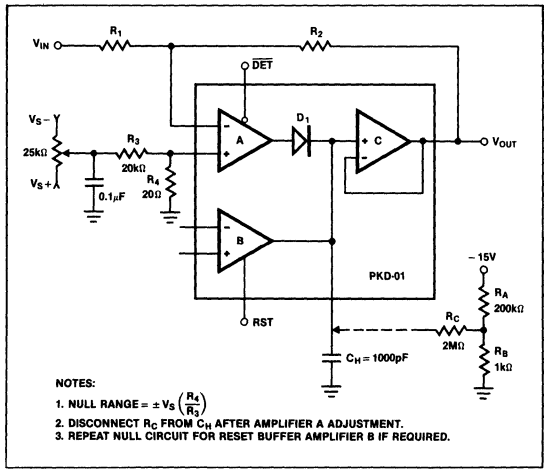


Figure C. V_{OS} Null Circuit for Negative Peak Detector

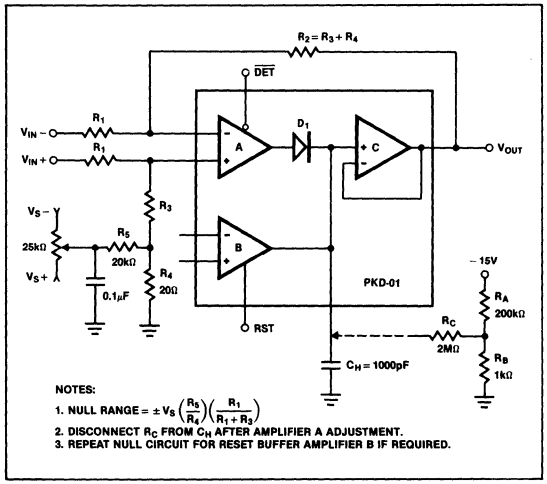


Figure B. V_{OS} Null Circuit for Differential Peak Detector

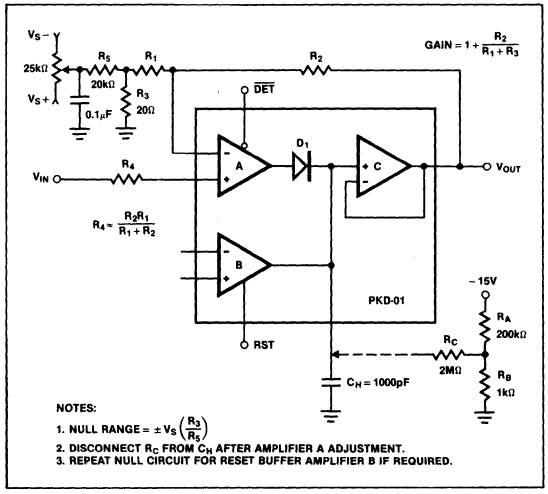


Figure D. V_{OS} Null Circuit for Positive Peak Detector With Gain

PEAK HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) serves as the peak memory element and compensating capacitor. Stable operation requires a minimum value of 1000pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase.

Zero scale error is internally trimmed for C_H = 1000pF. Other C_H values will cause a zero scale shift which can be approximated with the following equation.

$$\Delta V_{ZS}(mV) = \frac{1 \times 10^3(pC)}{C_H(nF)} - 0.6mV$$

The peak hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85° C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. This avoids digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point. To minimize gain errors and maintain the PKD-01's inherently low droop rate, guarding Pin 4 as shown in Figure 2 is recommended.

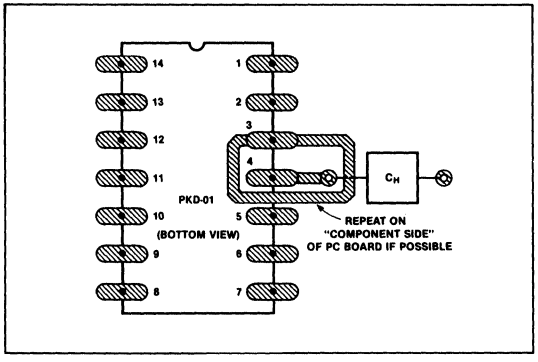


Figure 2. C_H terminal (Pin 4) guarding. See text.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

The maximum comparator high output voltage (V_{OH}) should be limited to:

$V_{OH}(maximum) < V^+ - 2.0V$

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1.

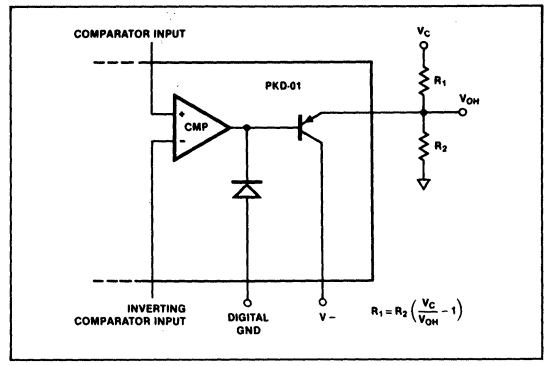


Figure 1

Table I.

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{SINK}}$$

$$R_2 \approx \left(\frac{1}{\frac{V_C}{V_{OH}} - 1}\right)$$

PEAK DETECTOR LOGIC CONTROL (RST, $\overline{DET}$)

The transconductance amplifier outputs are controlled by the digital logic signals RST and $\overline{DET}$. The PKD-01 operational mode is selected by steering the current (I_1) through Q_1 and Q_2, thus providing high-speed switching and a predictable logic threshold. The logic threshold voltage is 1.4 volts when digital ground is at zero volts.

Other threshold voltages (V_{TH}) may be selected by applying the formula:

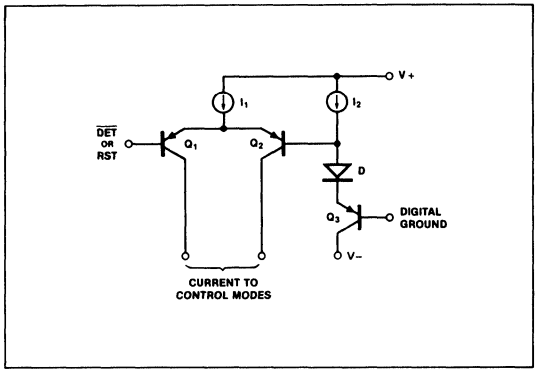
$V_{TH} \approx 1.4V$ + Digital Ground Potential.

For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The RST or $\overline{DET}$ signal must always be at least 2.8V above the negative supply.

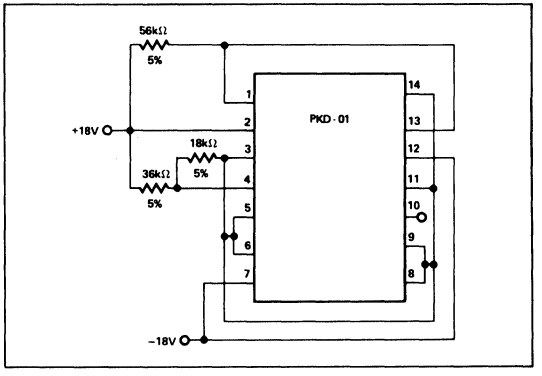
Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

$V_{OL} \approx 0.2V$ + Digital Ground Potential.

PKD-01 LOGIC CONTROL

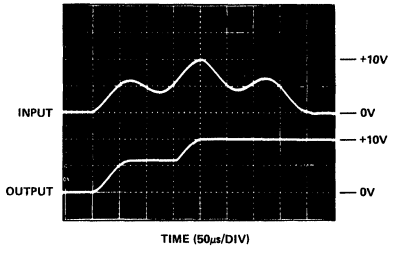


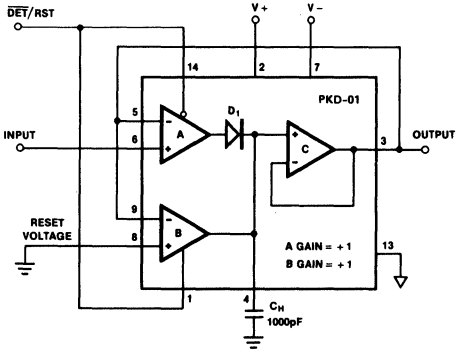
BURN-IN CIRCUIT



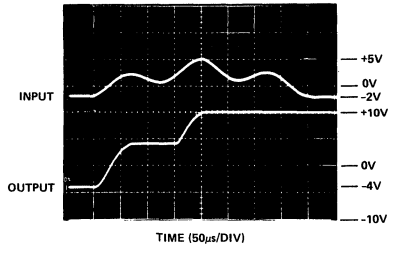
TYPICAL CIRCUIT CONFIGURATIONS

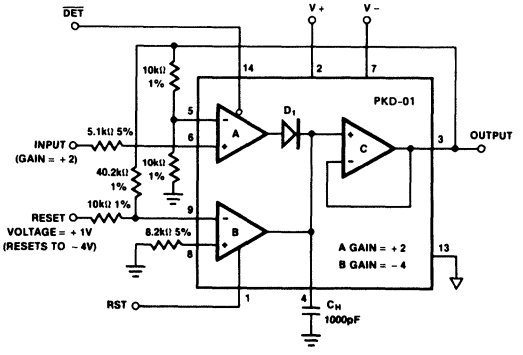
UNITY GAIN POSITIVE PEAK DETECTOR



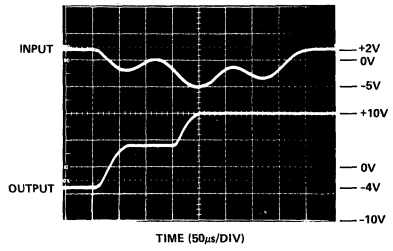


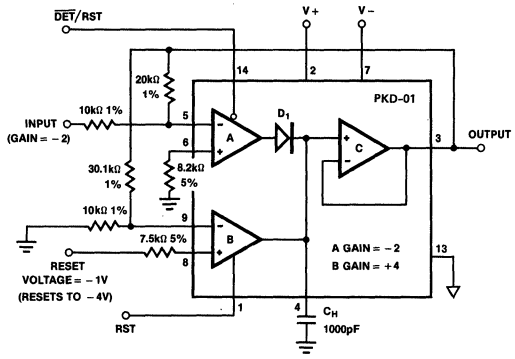
POSITIVE PEAK DETECTOR WITH GAIN



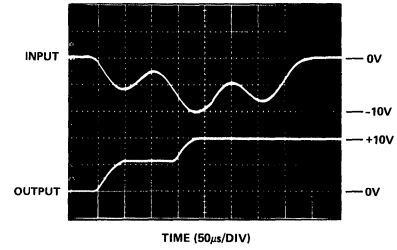


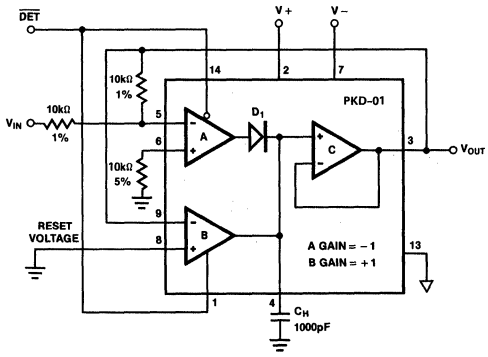
NEGATIVE PEAK DETECTOR WITH GAIN



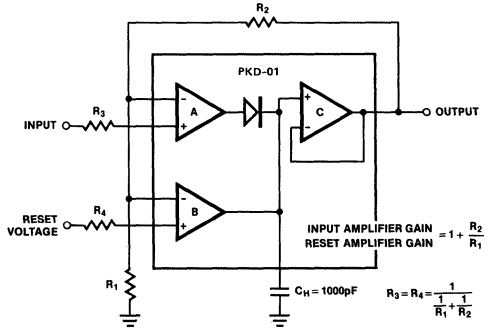


UNITY GAIN NEGATIVE PEAK DETECTOR





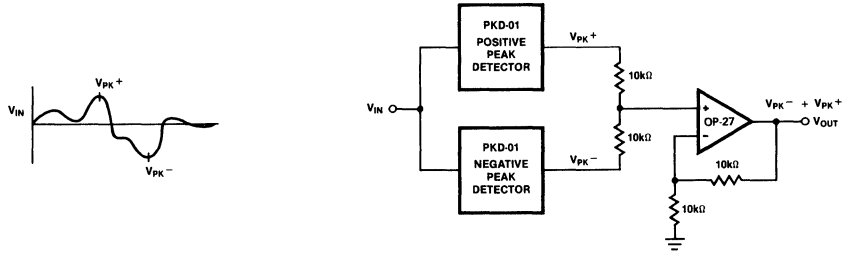
ALTERNATE GAIN CONFIGURATION



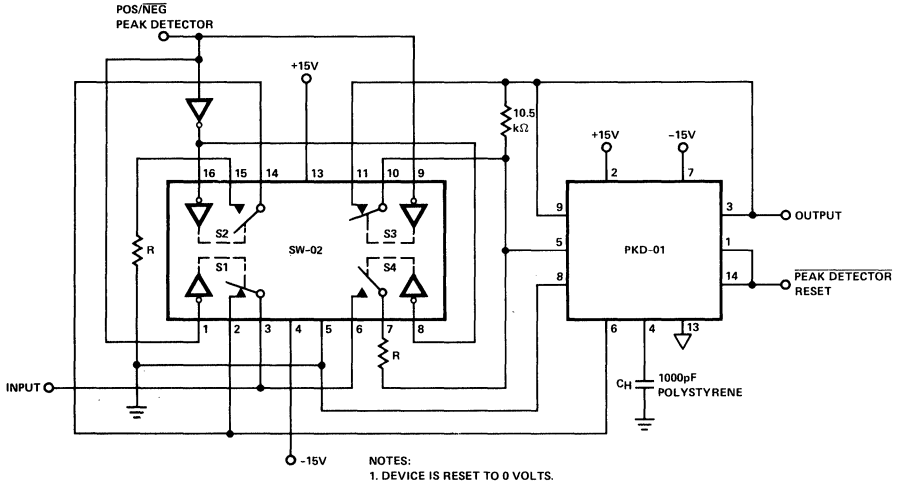
IF BOTH INPUT SIGNAL (AMPLIFIER A INPUT) AND THE RESET VOLTAGE (AMPLIFIER B INPUT HAVE THE SAME POSITIVE VOLTAGE GAIN THE GAIN CAN BE SET BY A SINGLE VOLTAGE DIVIDER FOR BOTH INPUT AMPLIFIERS.

NOTE:
R1, R2, R3 AND R4 > 5kΩ

PEAK-TO-PEAK DETECTOR

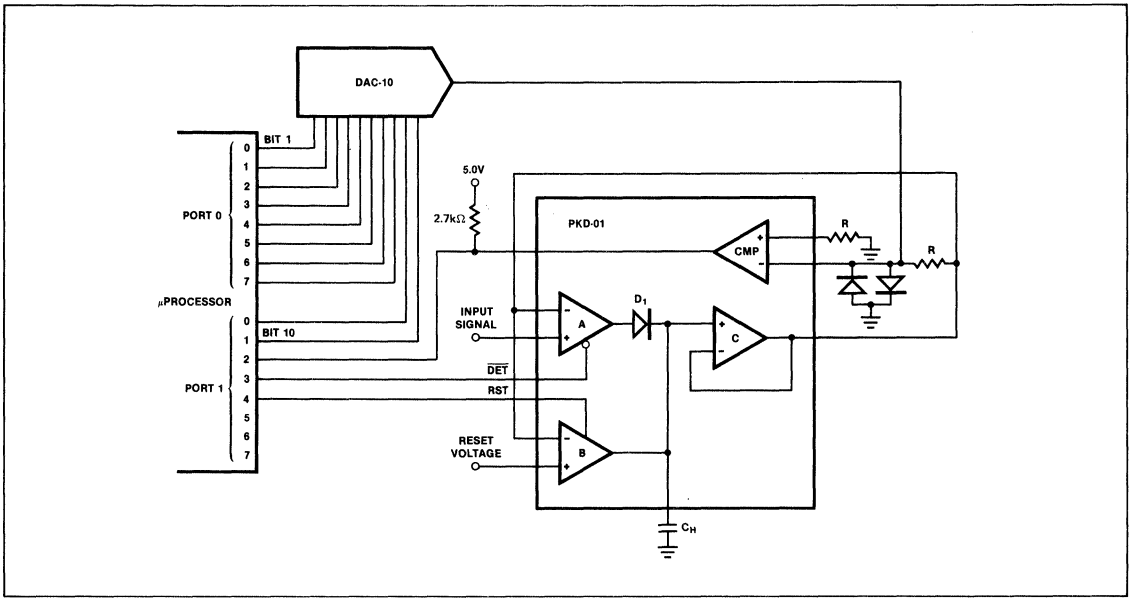


LOGIC SELECTABLE POSITIVE OR NEGATIVE PEAK DETECTOR

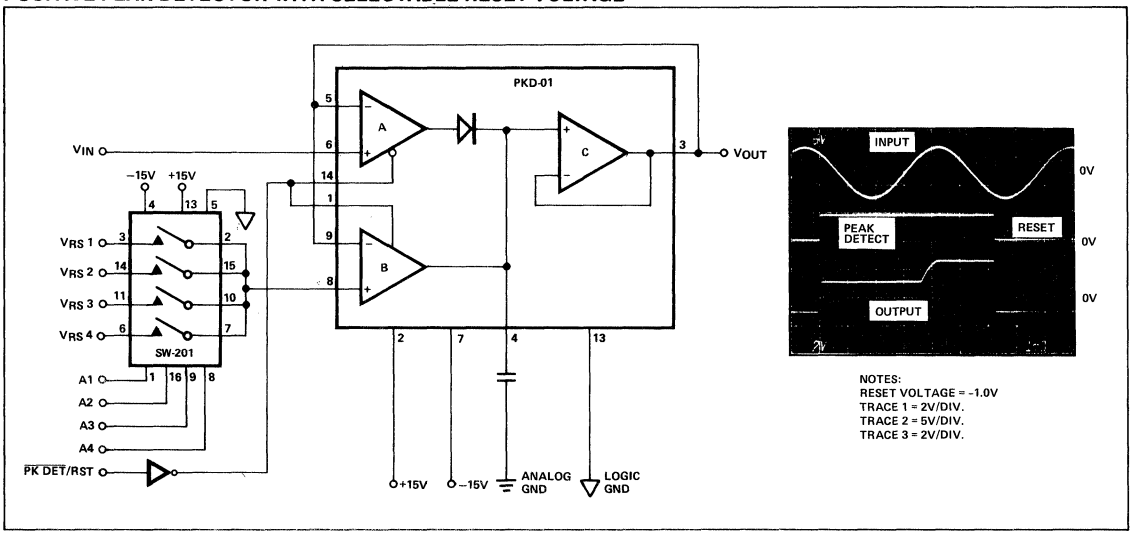


NOTES:
1. DEVICE IS RESET TO 0 VOLTS.
2. DETECTED PEAKS ARE PRESENTED AS POSITIVE OUTPUT LEVELS.
3. R = 10kΩ.

PEAK READING A/D CONVERTER

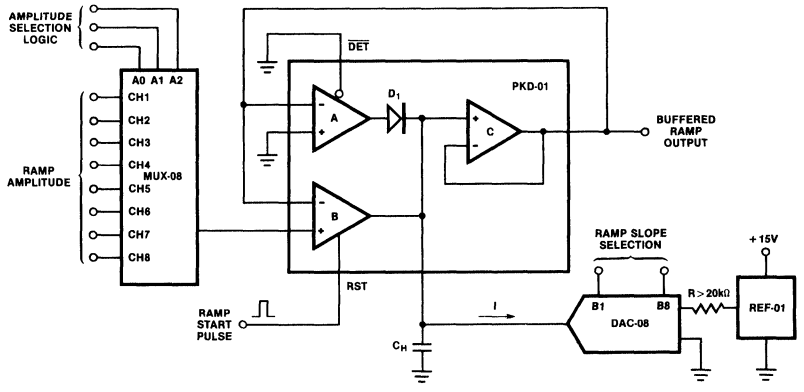


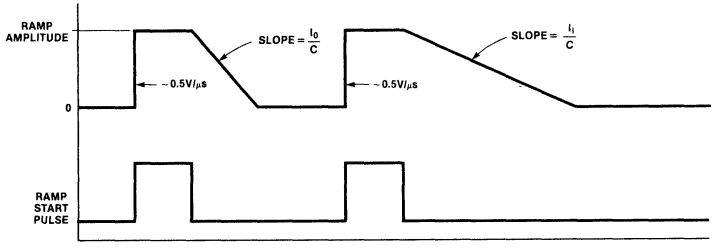
POSITIVE PEAK DETECTOR WITH SELECTABLE RESET VOLTAGE



NOTES:
RESET VOLTAGE = -1.0V
TRACE 1 = 2V/DIV.
TRACE 2 = 5V/DIV.
TRACE 3 = 2V/DIV.

PROGRAMMABLE LOW FREQUENCY RAMP GENERATOR





NOTES:
1. NEGATIVE SLOPE OF RAMP IS SET BY DAC-08 OUTPUT CURRENT.
2. DAC-08 IS DIGITALLY CONTROLLED CURRENT GENERATOR. THE MAXIMUM FULL SCALE CURRENT MUST BE LESS THAN 0.5mA.

7

Matched Transistors
Contents

Selection Guide
Matched Transistors

Model	Type	V_{OS} Max μV	TCV_{OS} Max μV/°C	hFE Min[1]	ΔhFE max %	en max nV/√Hz[2]	Package Options[3]	Temp Range[4]	Page[5]	Comments
MAT-01	Dual NPN	100	0.5	500	3	7.5	7	M	8-5	Low Cost
MAT-02	Dual NPN	50	0.1	500	2	1	4, 7	I, M	8-11	Low Noise, Low r_{BE}
MAT-03	Dual PNP	100	0.5	100	2	1	4, 7	I, M	8-23	Low Noise
MAT-04	Quad NPN	200	1	300	2	2.5	2, 3, 6	I, M	8-33	Low Cost
SSM-2210	Dual NPN	200	1	300	5	1	2, 6	I	AV	Low Cost, Audio
SSM-2220	Dual PNP	200	1	80	6	1	2, 6	I	AV	Low Cost, Audio

[1] I_C = 1 mA
[2] $f_C \geq 100$ Hz
[3] Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[4] Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
[5] AV = *Audio/Video Reference Manual.*
Boldface Type: Product recommended for new design.
*New product.

INTRODUCTION

ADI's matched transistor arrays are specifically designed for low offset voltage, low offset voltage drift, ultralow voltage noise, and high gain, specified over a wide range of collector currents. Monolithic duals provide the best possible differential input stage performance. The dual and quad transistors are excellent for use in high performance audio systems, high gain instrumentation amplifiers, precision current mirrors and active loads. ADI offers both NPN and PNP type matched transistors.

Both the dual and quad transistors are also designed for minimal base-to-emitter resistance which makes log conformity excellent. For an ideal transistor, the base-to-emitter voltage is equal to (kT/q) In (I_C/I_S). An added term, I_C r_{BE}, causes departure from this idealized logarithmic relationship. The NPN MAT-02 and MAT-04 and PNP MAT-03 have very low r_{BE} over a wide range of collector current. Circuits for squaring, rms-to-dc conversion, and logarithmic amplification can be accurately implemented through use of these low r_{BE} products.

The well defined relationship between V_{BE} and collector current can also be used for temperature sensing or for generating bandgap reference voltages.

DEFINITIONS

Average Offset Current Drift (TCI_{OS})
The ratio of the change in I_{OS} to the change in temperature producing it.

Average Offset Voltage Drift (TCV_{OS})
The ratio of the change in V_{OS} to the change in temperature producing it.

Bias Current (I_B)
The average of the base currents at a specified collector voltage and current.

Broadband Noise Voltage (e_{NRMS})
The root-mean-square noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Current Gain Match (Δh_{FE})
The difference in h_{FE} between the transistors at a specified voltage and current, expressed as a percentage of the higher of the two h_{FE}s.

$$\Delta h_{FE} = \left(1 - \frac{h_{FE1}}{h_{FE2}}\right) \times 100$$

Excess Emitter Resistance (r_{BE})
The effective resistance between the base and emitter terminals of each transistor.

Noise Voltage (e_N p–p)
The peak-to-peak noise voltage referred to the input over a specified bandwidth at a specified collector voltage and current.

Noise Voltage Density (e_N)
The spectral input referred voltage noise measured at a specified collector voltage and current.

Offset Current (I_{OS})
The difference between the base currents at a specified collector voltage and current.

Offset Current Change ($\Delta I_{OS}/\Delta V_{CB}$)
The ratio of the change in offset current to the change in collector base voltage producing it.

Offset Voltage (V_{OS})
The difference between the base emitter voltages (V_{BE1}–V_{BE2}) at a specified collector voltage and current.

8

ANALOG DEVICES

Matched Monolithic Dual Transistor

MAT-01

FEATURES

- **Low V_{OS} (V_{BE} Match) ..... 40μV Typ**
  100μV Max
- **Low TCV_{OS} ..... 0.5μV/° C Max**
- **High h_{FE} ..... 500 Min**
- **Excellent h_{FE} Linearity from 10nA to 10mA**
- **Low Noise Voltage ..... 0.23μV_{p-p} — 0.1Hz to 10Hz**
- **High Breakdown ..... 45V Min**
- **Available in Die Form**

ORDERING INFORMATION†

T_A = 25° C V_{OS} MAX (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
0.1	MAT01AH*	MIL
0.5	MAT01GH	MIL

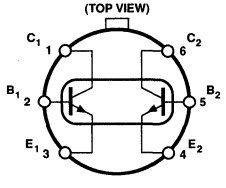
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The MAT-01 is a monolithic dual NPN transistor. An exclusive Silicon Nitride "Triple-Passivation" process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of 40μV, temperature drift of 0.15μV/° C, and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at a collector current of only 10nA. The high gain at low collector current makes the MAT-01 ideal for use in low-power, low-level input stages.

PIN CONNECTIONS



TO-78
(H-Suffix)

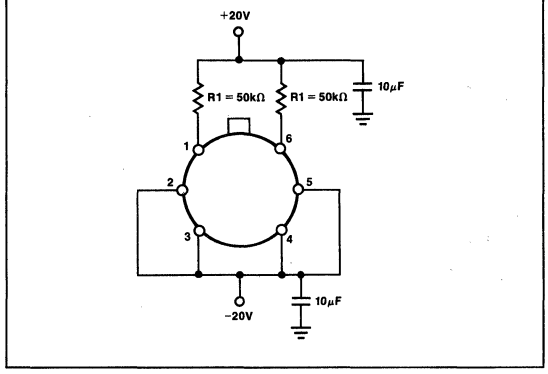
NOTE:
Substrate is connected to case.

ABSOLUTE MAXIMUM RATINGS (Note 4)

Collector-Base Voltage (BV_{CBO})
MAT-01AH, GH, N 45V
Collector-Emitter Voltage (BV_{CEO})
MAT-01AH, GH, N 45V
Collector-Collector Voltage (BV_{CC})
MAT-01AH, GH, N 45V
Emitter-Emitter Voltage (BV_{EE})
MAT-01AH, GH, N 45V
Emitter-Base Voltage (BV_{EBO}) (Note 1) 5V
Collector Current (I_C) 25mA
Emitter Current (I_E) 25mA
Total Power Dissipation
Case Temperature ≤ 40° C (Note 2) 1.8W
Ambient Temperature ≤ 70° C (Note 3) 500mW
Operating Ambient Temperature ..... −55° C to +125° C
Operating Junction Temperature ..... −55° C to +150° C
Storage Temperature ..... −65° C to +150° C
Lead Temperature (Soldering, 60 sec) ..... 300° C
DICE Junction Temperature ..... −65° C to +150° C

NOTES:
1. Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5V rating shown.
2. Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/° C for case temperatures above 40° C.
3. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/° C for ambient temperatures above 70° C.
4. Absolute maximum ratings apply to both DICE and packaged devices.

BURN-IN CIRCUIT



8

MAT-01

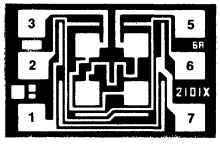
ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01AH MIN	MAT-01AH TYP	MAT-01AH MAX	MAT-01GH MIN	MAT-01GH TYP	MAT-01GH MAX	UNITS
Breakdown Voltage	BV_{CEO}	I_C = 100μA	45	—	—	45	—	—	V
Offset Voltage	V_{OS}		—	0.04	0.1	—	0.10	0.5	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)	—	2.0	—	—	2.0	—	μV/Mo
Long-Term		(Note 2)	—	0.2	—	—	0.2	—	
Offset Current	I_{OS}		—	0.1	0.6	—	0.2	3.2	nA
Bias Current	I_B		—	13	20	—	18	40	nA
Current Gain	h_{FE}	I_C = 10nA	—	590	—	—	430	—	
		I_C = 10μA	500	770	—	250	560	—	
		I_C = 10mA	—	840	—	—	610	—	
Current Gain Match	Δh_{FE}	I_C = 10μA	—	0.7	3.0	—	1.0	8.0	%
		100nA ≤ I_C ≤ 10mA	—	0.8	—	—	1.2	—	
Low Frequency Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	—	0.23	0.4	—	0.23	0.4	μV_{p-p}
Broadband Noise Voltage	e_{nRMS}	1Hz to 10kHz	—	0.60	—	—	0.60	—	μV_{RMS}
Noise Voltage Density	e_n	f_O = 10Hz (Note 3)	—	7.0	9.0	—	7.0	9.0	
		f_O = 100Hz (Note 3)	—	6.1	7.6	—	6.1	7.6	$nV/\sqrt{Hz}$
		f_O = 1000Hz (Note 3)	—	6.0	7.5	—	6.0	7.5	
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30V	—	0.5	3.0	—	0.8	8.0	μV/V
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 30V	—	2	15	—	3	70	pA/V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 30V, I_E = 0 (Note 4)	—	15	50	—	25	200	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = 30V, V_{BE} = 0 (Notes 4, 6)	—	50	200	—	90	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = 30V, (Note 6)	—	20	200	—	30	400	pA
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 0.1mA, I_C = 1mA	—	0.12	0.20	—	0.12	0.25	V
		I_B = 1mA, I_C = 10mA	—	0.8	—	—	0.8	—	
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	—	450	—	—	450	—	MHz
Output Capacitance	C_{ob}	V_{CB} = 15V, I_E = 0	—	2.8	—	—	2.8	—	pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	—	8.5	—	—	8.5	—	pF

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01AH MIN	MAT-01AH TYP	MAT-01AH MAX	MAT-01GH MIN	MAT-01GH TYP	MAT-01GH MAX	UNITS
Offset Voltage	V_{OS}		—	0.06	0.15	—	0.14	0.70	mV
Average Offset Voltage Drift	TCV_{OS}	(Note 7)	—	0.15	0.50	—	0.35	1.8	μV/°C
Offset Current	I_{OS}		—	0.9	8.0	—	1.5	15.0	nA
Average Offset Current Drift	TCI_{OS}	(Note 5)	—	10	90	—	15	150	pA/°C
Bias Current	I_B		—	28	60	—	36	130	nA
Current Gain	h_{FE}		167	400	—	77	300	—	
Collector-Base Leakage Current	I_{CBO}	T_A = 125°C, V_{CB} = 30V, I_E = 0 (Note 4)	—	15	80	—	25	200	nA
Collector-Emitter Leakage Current	I_{CES}	T_A = 125°C, V_{CE} = 30V, V_{BE} = 0 (Notes 4, 6)	—	50	300	—	90	400	nA
Collector-Collector Leakage Current	I_{CC}	T_A = 125°C, V_{CC} = 30V (Note 6)	—	30	200	—	50	400	nA

DICE CHARACTERISTICS



1. COLLECTOR (1)
2. BASE (1)
3. EMITTER (1)
5. EMITTER (2)
6. BASE (2)
7. COLLECTOR (2)

DIE SIZE 0.035 × 0.025 inch, 875 sq. mils
(0.89 × 0.64 mm, 0.58 sq. mm)

WAFER TEST LIMITS at V_{CB} = 15V and I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}	I_C = 100μA	45	V MIN
Offset Voltage	V_{OS}		0.5	mV MAX
Offset Current	I_{OS}		3.2	nA MAX
Bias Current	I_B		40	nA MAX
Current Gain	h_{FE}		250	MIN
Current Gain Match	Δh_{FE}		8.0	% MAX
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \le V_{CB} \le 30V$	8.0	μV/V MAX
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \le V_{CB} \le 30V$	70	pA/V MAX
Collector Saturation Voltage	$V_{CE\ (SAT)}$	I_B = 0.1mA, I_C = 1mA	0.25	V MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in asembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V_{CB} = 15V and I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-01N TYPICAL	UNITS
Average Offset Voltage Drift	TCV_{OS}		0.35	μV/°C
Average Offset Current Drift	TCI_{OS}		15	pA/°C
Collector-Emitter-Leakage Current	I_{CES}	V_{CE} = 30V, V_{BE} = 0	90	pA
Collector-Base-Leakage Current	I_{CBO}	V_{CB} = 30V, I_E = 0	25	pA
Gain Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	450	MHz
Offset Voltage Stability	$\Delta V_{OS}/T$	First Month (Note 1) Long-Term (Note 2)	2.0 0.2	μV/Mo

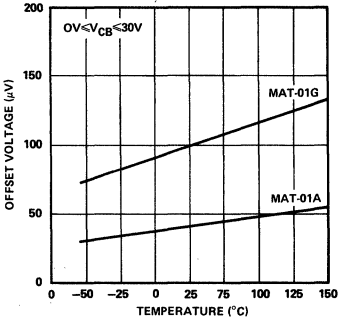
NOTES:
1. Exclude first hour of operation to allow for stabilization.
2. Parameter describes long-term average drift after first month of operation.
3. Sample tested.
4. The collector-base (I_{CBO}) and collector-emitter (I_{CES}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.
5. Guaranteed by I_{OS} test limits over temperature.
6. I_{CC} and I_{CES} are guaranteed by measurement of I_{CBO}.
7. Guaranteed by V_{OS} test ($TCV_{OS} \simeq \frac{V_{OS}}{T}$ for $V_{OS} \ll V_{BE}$) T = 298°K for T_A = 25°C.

8

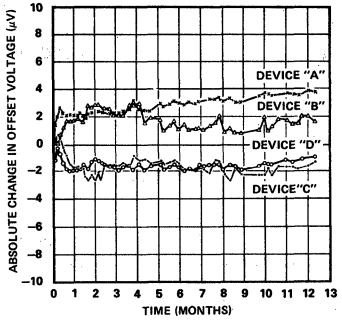
MAT-01

TYPICAL PERFORMANCE CHARACTERISTICS

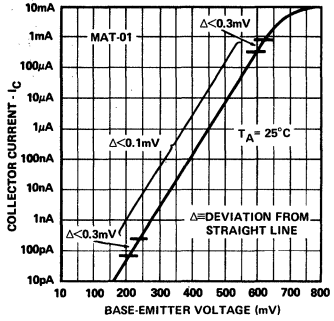
OFFSET VOLTAGE vs TEMPERATURE



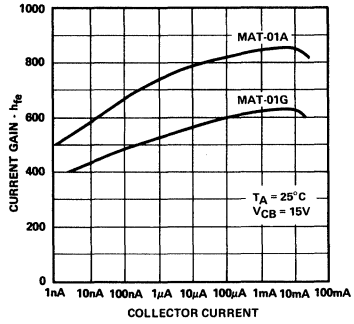
OFFSET VOLTAGE vs TIME



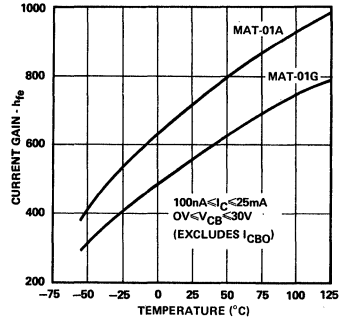
BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT



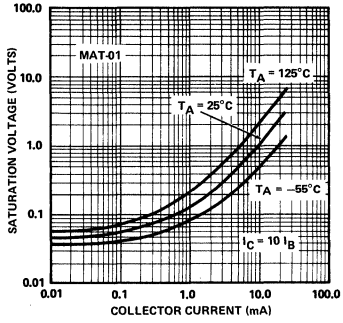
CURRENT GAIN vs COLLECTOR CURRENT



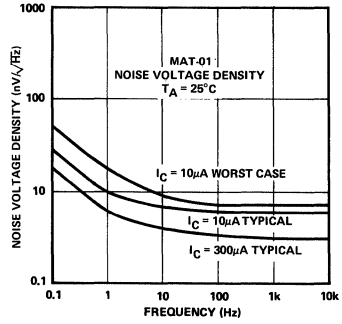
CURRENT GAIN vs TEMPERATURE



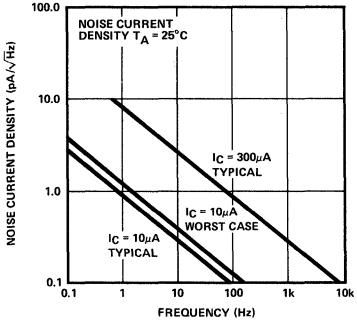
SATURATION VOLTAGE vs COLLECTOR CURRENT



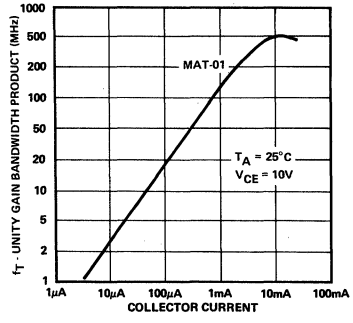
NOISE VOLTAGE



NOISE CURRENT DENSITY

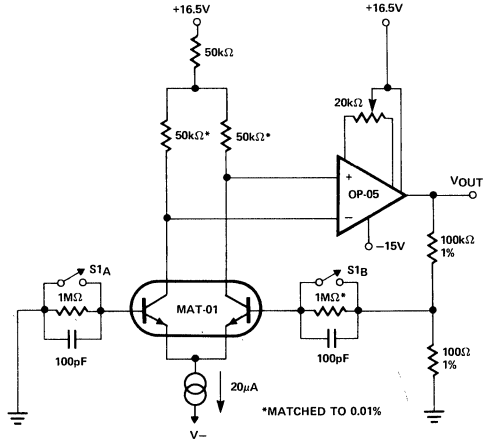


GAIN-BANDWIDTH vs COLLECTOR CURRENT



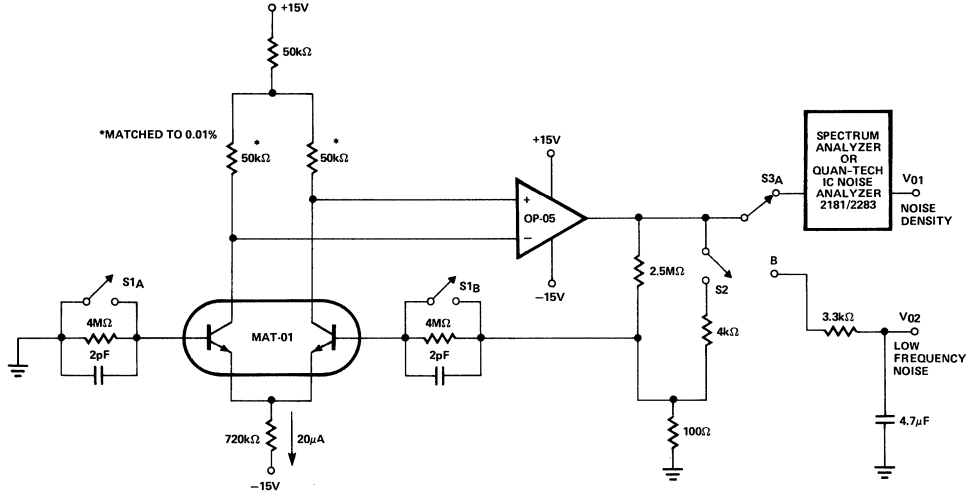
MAT-01 TEST CIRCUITS

MAT-01 MATCHING MEASUREMENT CIRCUIT



TEST	SI_A	SI_B	UNITS	
V_{OS}	X	X	V_{OUT_1}	1 volt per mV
I_{OS}	O	O	$V_{OUT_2} - V_{OUT_1}$	1 volt per nA

MAT-01 NOISE MEASUREMENT CIRCUIT



TEST	SI_A	SI_B	S_2	S_3	READING
Noise Voltage Density (Per Transistor)	X	X	X	A	$V_{01}/\sqrt{2}$
Noise Current Density (Per Transistor)	O	O	X	A	$V_{01}/(\sqrt{2} \times 4M\Omega)$
Low Frequency Noise (Referred to Input)	X	X	O	B	$\frac{V_{02}\ \text{PEAK-TO-PEAK}}{25{,}000}$

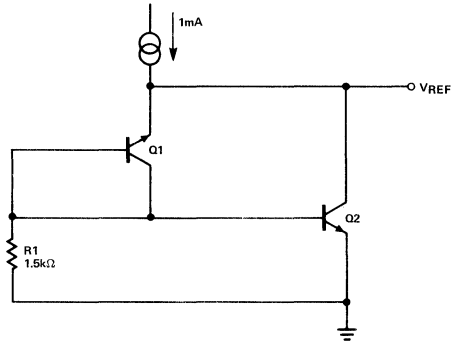
APPLICATION NOTES

Application of reverse bias voltages to the emitter-base junctions in excess of ratings (5V) may result in degradation of h_{FE} and h_{FE} matching characteristics. Circuit designs should be checked to ensure that reverse bias voltages above 5V cannot be applied during such transient conditions as at circuit turn-on and turn-off.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the predicted drift performance. Both input terminals should be maintained at the same temperature, preferably close to the temperature of the device's package.

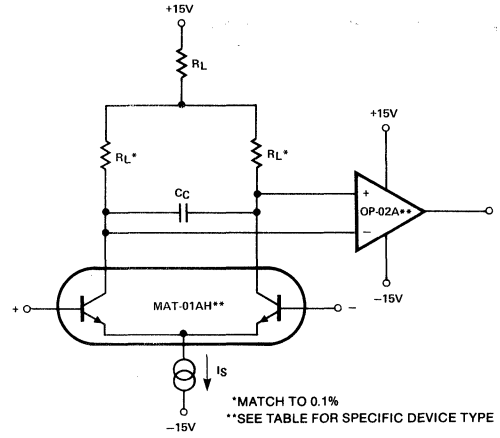
TYPICAL APPLICATIONS

PRECISION REFERENCE



$V_{REF} \approx 7.0V$
$TCV_{REF} \approx 10ppm/°C$
$R_O \approx 40\Omega$
R_1 MAY BE ADJUSTED TO MINIMIZE TCV_{REF}. INCREASING R_1 WILL CAUSE A POSITIVE CHANGE IN TCV_{REF}.
NOTE: h_{FE} OF Q1 WILL BE REDUCED BY OPERATION OF BREAKDOWN MODE.

PRECISION OPERATIONAL AMPLIFIERS

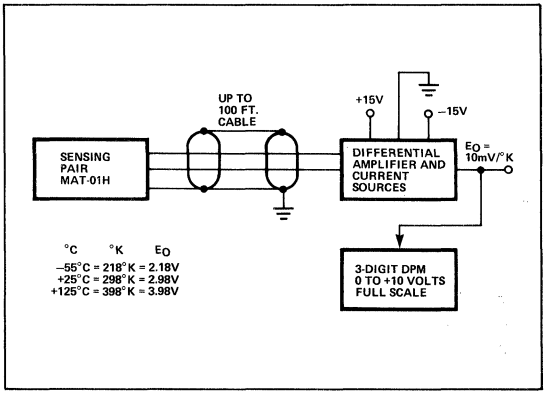


*MATCH TO 0.1%
**SEE TABLE FOR SPECIFIC DEVICE TYPE

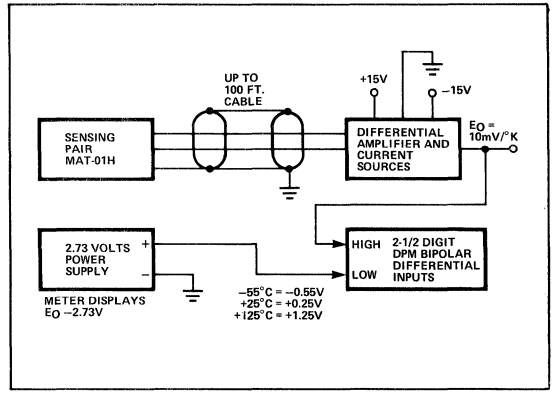
THIS CONFIGURATION CAN ALSO BE USED WITH THE LOW POWER OP-21 OR MICROPOWER OP-22 TO ACHIEVE A LOW NOISE AND LOW POWER PRECISION OP-AMP.

	MAT-01AH OP-02A	MAT-01AH OP-02A	MAT-01GH OP-02	MAT-01GH OP-02
V_{OS} Maximum	0.15mV	0.27mV	0.65mV	1.2mV
TCV_{OS} Maximum	0.6μV/°C	1μV/°C	2μV/°C	4μV/°C
I_{OS} Maximum	0.8nA	0.1nA	3.2nA	0.32nA
I_B Maximum	20nA	2nA	40nA	4nA
Gain Minimum	2,000,000	2,000,000	800,000	800,000
I_S	20μA	2μA	20μA	2μA
R_L	100kΩ	1MΩ	100kΩ	1MΩ

BASIC DIGITAL THERMOMETER READOUT IN DEGREES KELVIN (°K)



DIGITAL THERMOMETER WITH READOUT IN °C



ANALOG DEVICES

Low-Noise Matched Dual Monolithic Transistor

MAT-02

FEATURES

- **Low Offset Voltage** ..... **50μV Max**
- **Low Noise Voltage at 100Hz, 1mA** ... **1.0nV/√Hz Max**
- **High Gain (h_{FE})** ..... **500 Min at I_C = 1mA**
  ..... **300 Min at I_C = 1μA**
- **Excellent Log Conformance** ..... **$r_{BE} \simeq 0.3\Omega$**
- **Low Offset Voltage Drift** ..... **0.1μV/° C Max**
- **Improved Direct Replacement for LM194/394**
- **Available in Die Form**

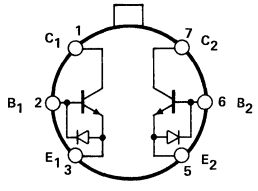
ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE TO-78	PACKAGE LCC 20-CONTACT	OPERATING TEMPERATURE RANGE
50	MAT02AH*	–	MIL
50	MAT02EH	–	IND
150	–	MAT02BRC/883	MIL
150	MAT02FH	–	IND

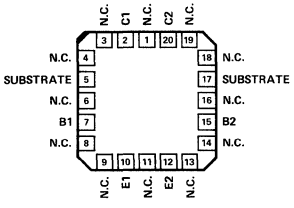
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

PIN CONNECTIONS



TO-78 (H-Suffix)



MAT-02BRC/883 20-LEAD LCC (RC-Suffix)

NOTE: Substrate is connected to case on TO-78 package. Substrate is normally connected to the most negative circuit potential, but can be floated.

8

GENERAL DESCRIPTION

The design of the MAT-02 series of NPN dual monolithic transistors is optimized for very low noise, low drift, and low r_{BE}. Precision Monolithics' exclusive Silicon Nitride "Triple-Passivation" process stabilizes the critical device parameters over wide ranges of temperature and elapsed time. Also, the high current gain (h_{FE}) of the MAT-02 is maintained over a wide range of collector current. Exceptional characteristics of the MAT-02 include offset voltage of 50μV max (A/E grades) and 150μV max (B/F grades). Device performance is specified over the full military temperature range as well as at 25° C.

Input protection diodes are provided across the emitter-base junctions to prevent degradation of the device characteristics due to reverse-biased emitter current. The substrate is clamped to the most negative emitter by the parasitic isolation junction created by the protection diodes. This results in complete isolation between the transistors.

The MAT-02 should be used in any application where low noise is a priority. The MAT-02 can be used as an input stage to make an amplifier with noise voltage of less than 1.0nV/√Hz at 100Hz. Other applications, such as log/anti-log circuits, may use the excellent logging conformity of the MAT-02. Typical bulk resistance is only 0.3Ω to 0.4Ω. The MAT-02 electrical characteristics approach those of an ideal transistor when operated over a collector current range of 1μA to 10mA. For applications requiring multiple devices see MAT-04 Quad Matched Transistor data sheet.

ABSOLUTE MAXIMUM RATINGS (Note 3)

Collector-Base Voltage (BV_{CBO})	40V
Collector-Emitter Voltage (BV_{CEO})	40V
Collector-Collector Voltage (BV_{CC})	40V
Emitter-Emitter Voltage (BV_{EE})	40V
Collector Current (I_C)	20mA
Emitter Current (I_E)	20mA
Total Power Dissipation	
Case Temperature ≤40°C (Note 1)	1.8W
Ambient Temperature ≤70°C (Note 2)	500mW
Operating Temperature Range	
MAT-02A, B	–55°C to +125°C
MAT-02E, F	–25°C to +85°C
Operating Junction Temperature	–55°C to +150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C
Junction Temperature	–65°C to +150°C

NOTES:

1. Rating applies to applications using heat sinking to control case temperature. Derate linearly at 16.4mW/° C for case temperature above 40° C.
2. Rating applies to applications not using heat sinking; device in free air only. Derate linearly at 6.3mW/° C for ambient temperature above 70° C.
3. Absolute maximum ratings apply to both DICE and packaged devices.

MAT-02

ELECTRICAL CHARACTERISTICS at V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02A/E MIN	MAT-02A/E TYP	MAT-02A/E MAX	MAT-02B/F MIN	MAT-02B/F TYP	MAT-02B/F MAX	UNITS
Current Gain	h_{FE}	I_C = 1mA (Note 1)	500	605	—	400	605	—	
		I_C = 100μA	500	590	—	400	590	—	
		I_C = 10μA	400	550	—	300	550	—	
		I_C = 1μA	300	485	—	200	485	—	
Current Gain Match	Δh_{FE}	10μA ≤ I_C ≤ 1mA, (Note 2)	—	0.5	2	—	0.5	4	%
Offset Voltage	V_{OS}	V_{CB} = 0 1μA ≤ I_C ≤ 1mA (Note 7)	—	10	50	—	80	150	μV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX}, (Note 6) 1μA ≤ I_C ≤ 1mA (Note 7)	—	10	25	—	10	50	μV
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V 1μA ≤ I_C ≤ 1mA (Note 7)	—	5	25	—	5	50	μV
Offset Current Change vs V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX}	—	30	70	—	30	70	pA/V
Bulk Resistance	r_{BE}	10μA ≤ I_C ≤ 10mA (Note 3)	—	0.3	0.5	—	0.3	0.5	Ω
Collector-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX}	—	25	200	—	25	400	pA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX}, (Notes 3, 5)	—	35	200	—	35	400	pA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX}, (Notes 3, 5) V_{BE} = 0	—	35	200	—	35	400	pA
Noise Voltage Density	e_n	I_C = 1mA, V_{CB} = 0, (Note 4) f_O = 10Hz	—	1.6	2	—	1.6	3	nV/√Hz
		f_O = 100Hz	—	0.9	1	—	0.9	2	
		f_O = 1kHz	—	0.85	1	—	0.85	2	
		f_O = 10kHz	—	0.85	1	—	0.85	2	
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA I_B = 100μA	—	0.05	0.1	—	0.05	0.2	V
Input Bias Current	I_B	I_C = 10μA	—	—	25	—	—	34	nA
Input Offset Current	I_{OS}	I_C = 10μA	—	—	0.6	—	—	1.3	nA
Breakdown Voltage	BV_{CEO}		40	—	—	40	—	—	V
Gain-Bandwidth Product	f_T	I_C = 10mA, V_{CE} = 10V	—	200	—	—	200	—	MHz
Output Capacitance	C_{OB}	V_{CB} = 15V, I_E = 0	—	23	—	—	23	—	pF
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	—	35	—	—	35	—	pF

NOTES:

1. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
2. Current Gain Match (Δh_{FE}) is defined as:

$$\Delta h_{FE} = \frac{100\ (\Delta I_B)\ (h_{FE}\ \text{min})}{I_C}$$

3. Guaranteed by design.
4. Sample tested.
5. I_{CC} and I_{CES} are verified by measurement of I_{CBO}.
6. This is the maximum change in V_{OS} as V_{CB} is swept from 0V to 40V.
7. Measured at I_C = 10μA and guaranteed by design over the specified range of I_C.

ELECTRICAL CHARACTERISTICS V_{CB} = 15V, −25°C ≤ T_A ≤ +85°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02E MIN	MAT-02E TYP	MAT-02E MAX	MAT-02F MIN	MAT-02F TYP	MAT-02F MAX	UNITS
Offset Voltage	V_{OS}	V_{CB} = 0 1μA ≤ I_C ≤ 1mA (Note 5)	—	—	70	—	—	220	μV
Average Offset Voltage Drift	TCV_{OS}	10μA ≤ I_C ≤ 1mA, 0 ≤ V_{CB} ≤ V_{MAX}, (Note 1) V_{OS} Trimmed to Zero, (Note 3)	— —	0.08 0.03	0.3 0.1	— —	0.08 0.03	1 0.3	μV/°C
Input Offset Current	I_{OS}	I_C = 10μA	—	—	8	—	—	13	nA
Input Offset Current Drift	TCI_{OS}	I_C = 10μA, (Note 4)	—	40	90	—	40	150	pA/°C
Input Bias Current	I_B	I_C = 10μA	—	—	45	—	—	50	nA
Current Gain	h_{FE}	I_C = 1mA, (Note 2) I_C = 100μA I_C = 10μA I_C = 1μA	325 275 225 200	— — — —	— — — —	300 250 200 150	— — — —	— — — —	
Collector-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX}	—	2	—	—	3	—	nA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX}, V_{BE} = 0	—	3	—	—	4	—	nA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX}	—	3	—	—	4	—	nA

ELECTRICAL CHARACTERISTICS V_{CB} = 15V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

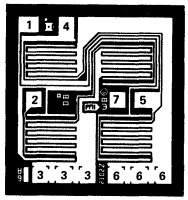
PARAMETER	SYMBOL	CONDITIONS	MAT-02A MIN	MAT-02A TYP	MAT-02A MAX	MAT-02B MIN	MAT-02B TYP	MAT-02B MAX	UNITS
Offset Voltage	V_{OS}	V_{CB} = 0 1μA ≤ I_C ≤ 1mA (Note 5)	—	—	80	—	—	250	μV
Average Offset Voltage Drift	TCV_{OS}	10μA ≤ I_C ≤ 1mA, 0 ≤ V_{CB} ≤ V_{MAX}, (Note 1) V_{OS} Trimmed to Zero, (Note 3)	— —	0.08 0.03	0.3 0.1	— —	0.08 0.03	1 0.3	μV/°C
Input Offset Current	I_{OS}	I_C = 10μA	—	—	9	—	—	15	nA
Input Offset Current Drift	TCI_{OS}	I_C = 10μA, (Note 4)	—	40	90	—	40	150	pA/°C
Input Bias Current	I_B	I_C = 10μA	—	—	60	—	—	70	nA
Current Gain	h_{FE}	I_C = 1mA, (Note 2) I_C = 100 μA I_C = 10μA I_C = 1μA	275 225 175 150	— — — —	— — — —	250 200 150 100	— — — —	— — — —	
Collector-Base Leakage Current	I_{CBO}	V_{CB} = V_{MAX} T_A = 125°C	—	15	—	—	25	—	nA
Collector-Emitter Leakage Current	I_{CES}	V_{CE} = V_{MAX}, V_{BE} = 0 T_A = 125°C	—	50	—	—	50	—	nA
Collector-Collector Leakage Current	I_{CC}	V_{CC} = V_{MAX} T_A = 125°C	—	30	—	—	40	—	nA

NOTES:

1. Guaranteed by V_{OS} test ($TCV_{OS} \simeq \frac{V_{OS}}{T}$ for $V_{OS} \ll V_{BE}$) T = 298k for T_A = 25°C.
2. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector current.
3. The initial zero offset voltage is established by adjusting the ratio of I_{C1} to I_{C2} at T_A = 25°C. This ratio must be held to 0.003% over the entire temperature range. Measurements are taken at the temperature extremes and 25°C.
4. Guaranteed by design.
5. Measured at I_C = 10μA and guaranteed by design over the specified range of I_C.

MAT-02

DICE CHARACTERISTICS



DIE SIZE 0.061 × 0.057 inch, 3,477 sq. mils
(1.549 × 1.448 mm, 224 sq. mm)

1. COLLECTOR 1
2. BASE 1
3. EMITTER 1
4. COLLECTOR 2
5. BASE 2
6. EMITTER 2
7. SUBSTRATE

WAFER TEST LIMITS at 25°C for V_{CB} = 15V and I_C = 10μA, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-02N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}		40	V MIN
Offset Voltage	V_{OS}	10μA ≤ I_C ≤ 1mA (Note 1)	150	μV MAX
Input Offset Current	I_{OS}		1.2	nA MAX
Input Bias Current	I_B	V_{CB} = 0V	34	nA MAX
Current Gain	h_{FE}	I_C = 1mA, V_{CB} = 0V I_C = 10μA, V_{CB} = 0V	400 300	MIN
Current Gain Match	Δh_{FE}	10μA ≤ I_C ≤ 1mA, V_{CB} = 0V	4	% MAX
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	0V ≤ V_{CB} ≤ 40V 10μA ≤ I_C ≤ 1mA (Note 1)	50	μV MAX
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0 10μA ≤ I_C ≤ 1mA (Note 1)	50	μV MAX
Bulk Resistance	r_{BE}	100μA ≤ I_C ≤ 10mA	0.5	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA I_B = 100μA	0.2	V MAX

NOTES:
1. Measured at I_C = 10μA and guaranteed by design over the specified range of I_C.

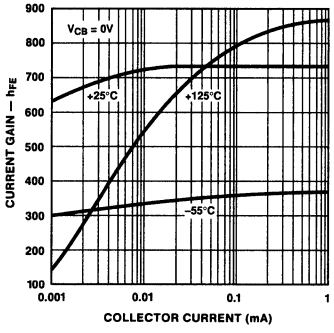
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS V_{CB} = 15V, I_C = 10μA, T_A = 25°C, unless otherwise noted.

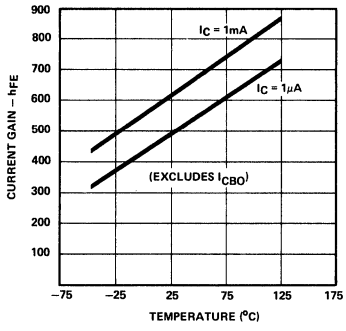
PARAMETER	SYMBOL	CONDITIONS	MAT-02N TYPICAL	UNITS
Average Offset Voltage Drift	TCV_{OS}	10μA ≤ I_C ≤ 1mA 0 ≤ V_{CB} ≤ V_{MAX}	0.08	μV/°C
Average Offset Current Drift	TCI_{OS}	I_C = 10μA	40	pA/°C
Gain-Bandwidth Product	f_T	V_{CE} = 10V, I_C = 10mA	200	MHz
Offset Current Change vs V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ 40V	70	pA/V

TYPICAL PERFORMANCE CHARACTERISTICS

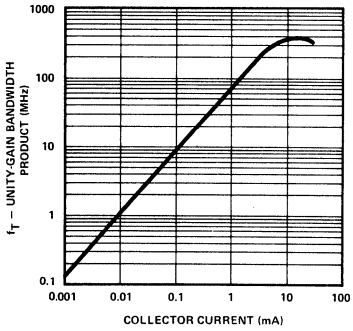
CURRENT GAIN vs COLLECTOR CURRENT



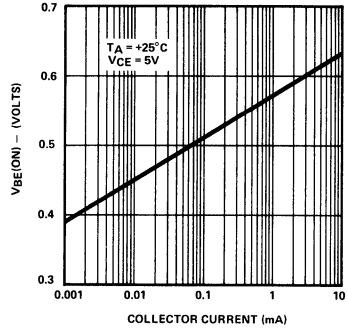
CURRENT GAIN vs TEMPERATURE



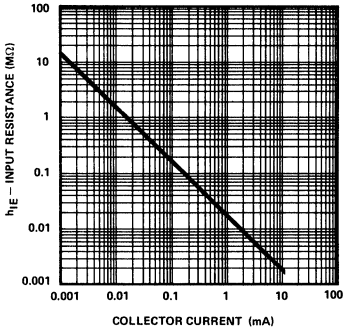
GAIN BANDWIDTH vs COLLECTOR CURRENT



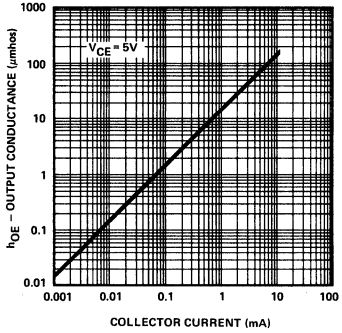
BASE-EMITTER-ON-VOLTAGE vs COLLECTOR CURRENT



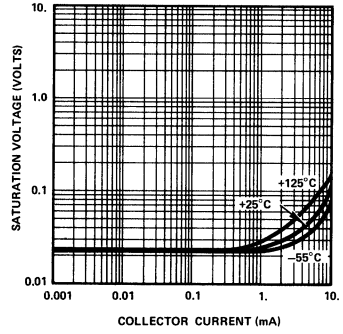
SMALL-SIGNAL INPUT RESISTANCE vs COLLECTOR CURRENT



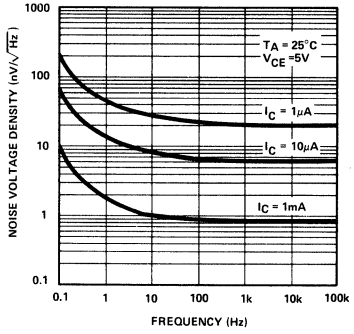
SMALL-SIGNAL OUTPUT CONDUCTANCE vs COLLECTOR CURRENT



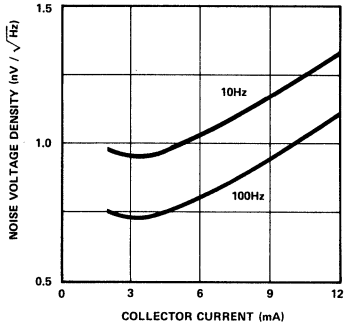
SATURATION VOLTAGE vs COLLECTOR CURRENT



NOISE VOLTAGE DENSITY vs FREQUENCY



NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



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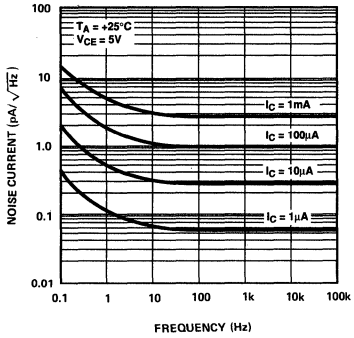
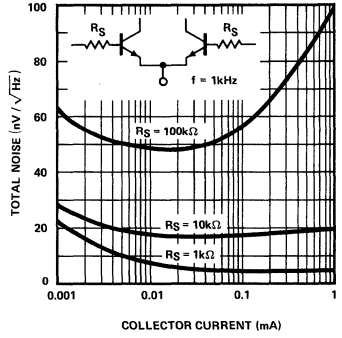
MAT-02

TYPICAL PERFORMANCE CHARACTERISTICS

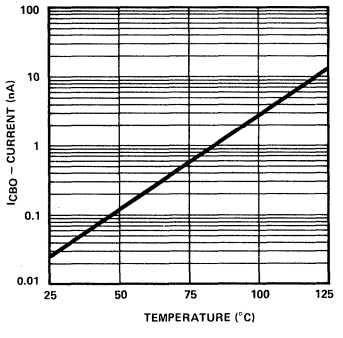
NOISE CURRENT DENSITY vs FREQUENCY



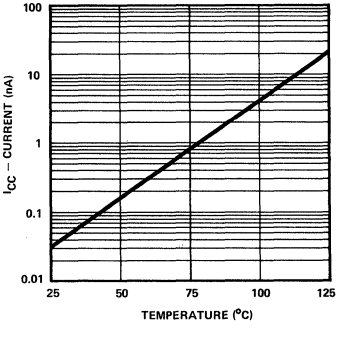
TOTAL NOISE vs COLLECTOR CURRENT



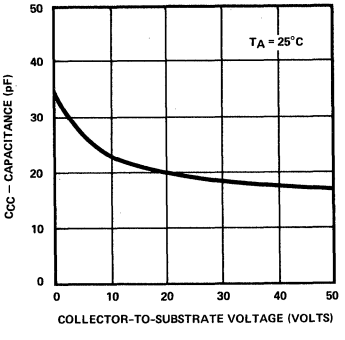
COLLECTOR-TO-BASE LEAKAGE vs TEMPERATURE



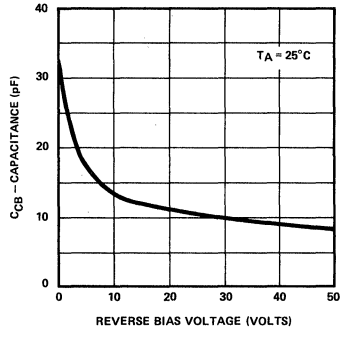
COLLECTOR-TO-COLLECTOR LEAKAGE vs TEMPERATURE



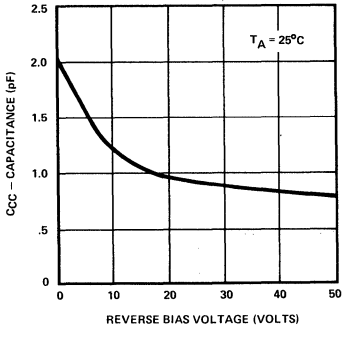
COLLECTOR-TO-COLLECTOR CAPACITANCE vs COLLECTOR-TO-SUBSTRATE VOLTAGE



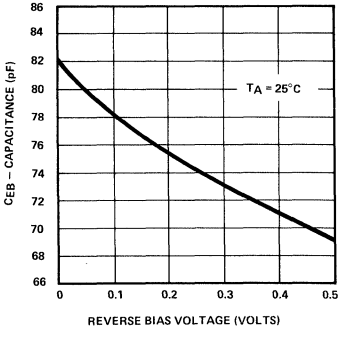
COLLECTOR-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE



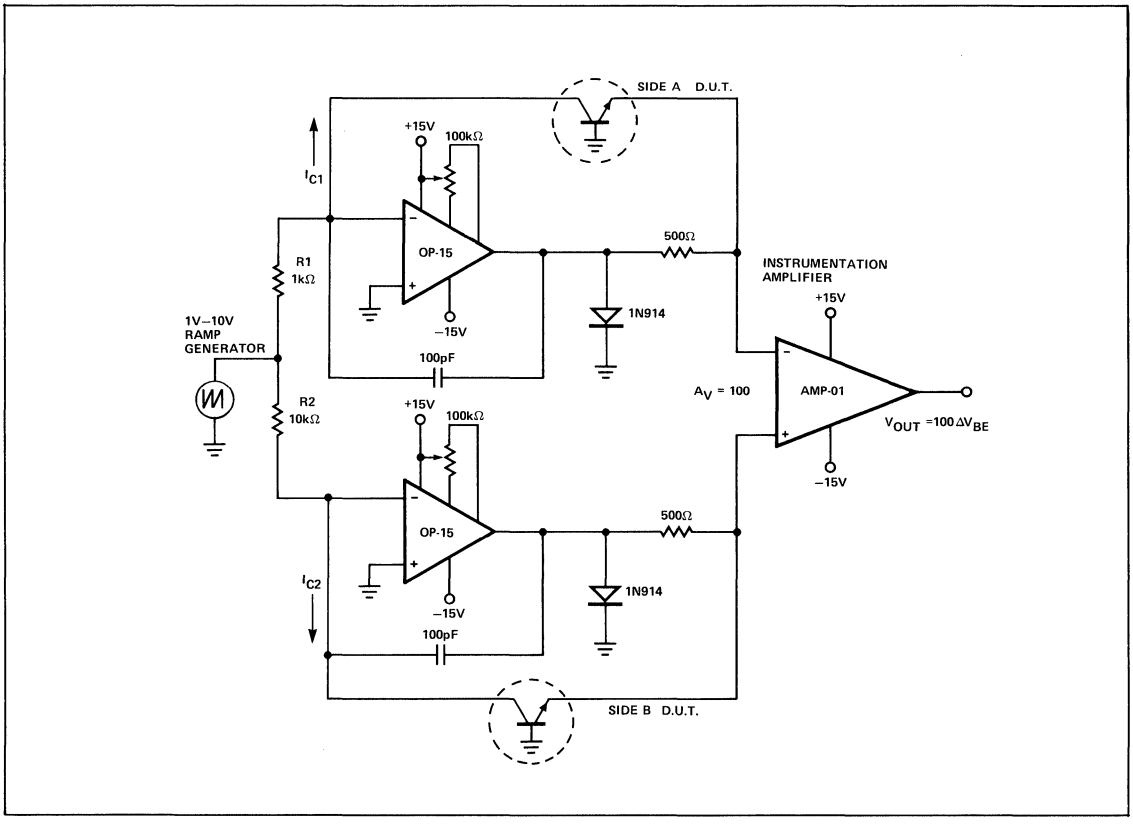
COLLECTOR-TO-COLLECTOR CAPACITANCE vs REVERSE BIAS VOLTAGE



EMITTER-BASE CAPACITANCE vs REVERSE BIAS VOLTAGE



LOG CONFORMANCE TEST CIRCUIT



LOG CONFORMANCE TESTING

The log conformance of the MAT-02 is tested using the circuit shown above. The circuit employs a dual transdiode logarithmic converter operating at a fixed ratio of collector currents that are swept over a 10:1 range. The output of each transdiode converter is the V_{BE} of the transistor plus an error term which is the product of the collector current and r_{BE}, the bulk emitter resistance. The difference of the V_{BE} is amplified at a gain of ×100 by the AMP-01 instrumentation amplifier. The differential emitter-base voltage (ΔV_{BE}) consists of a temperature-dependent DC level plus an AC error voltage which is the deviation from true log conformity as the collector currents vary.

The output of the transdiode logarithmic converter comes from the idealized intrinsic transistor equation (for silicon):

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} \text{ where} \qquad (1)$$

k = Boltzmann's Constant (1.38062×10^{-23} J/° K)
q = Unit Electron Charge (1.60219×10^{-19} C)
T = Absolute Temperature, ° K (= ° C + 273.2)
I_S = Extrapolated Current for $V_{BE} \rightarrow 0$
I_C = Collector Current

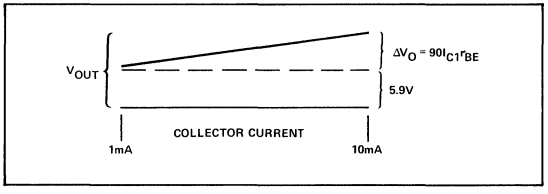
An error term must be added to this equation to allow for the bulk resistance (r_{BE}) of the transistor. Error due to the op amp input current is limited by use of the OP-15 BIFET-input op amp. The resulting AMP-01 input is:

$$\Delta V_{BE} = \frac{kT}{q} \ln \frac{I_{C1}}{I_{C2}} + I_{C1}\, r_{BE1} - I_{C2}\, r_{BE2} \qquad (2)$$

A ramp function which sweeps from 1V to 10V is converted by the op amps to a collector current ramp through each transistor. Because I_{C1} is made equal to 10 I_{C2}, and assuming T_A = 25° C, the previous equation becomes:

$$\Delta V_{BE} = 59\text{mV} + 0.9\, I_{C1}\, r_{BE} \quad (\Delta r_{BE} \sim 0)$$

As viewed on an oscilloscope, the change in ΔV_{BE} for a 10:1 change in I_C is then displayed as shown below:



With the oscilloscope AC coupled, the temperature dependent term becomes a DC offset and the trace represents the deviation from true log conformity. The bulk resistance can be calculated from the voltage deviation ΔV_O and the change in collector current (9mA):

$$r_{BE} = \frac{\Delta V_O}{9mA} \times \frac{1}{100} \quad (3)$$

This procedure finds r_{BE} for Side A. Switching R_1 and R_2 will provide the r_{BE} for Side B. Differential r_{BE} is found by making $R_1 = R_2$.

APPLICATIONS: NONLINEAR FUNCTIONS

MULTIPLIER/DIVIDER CIRCUIT

The excellent log conformity of the MAT-02 over a very wide range of collector current makes it ideal for use in log-antilog circuits. Such nonlinear functions as multiplying, dividing, squaring, and square-rooting are accurately and easily implemented with a log-antilog circuit using two MAT-02 pairs (see Figure 1). The transistor circuit accepts three input currents (I_1, I_2, and I_3) and provides an output current I_O according to $I_O = I_1 I_2 / I_3$. All four currents must be positive in the log-antilog circuit, but negative input voltages can be easily accomodated by various offsetting techniques. Protective diodes across each base-to-emitter junction would normally be needed, but these diodes are built into the MAT-02. External protection diodes are therefore not needed.

For the circuit shown in Figure 1, the operational amplifiers make $I_1 = V_X/R_1$, $I_2 = V_Y/R_2$, $I_3 = V_Z/R_3$, and $I_O = V_O/R_O$. The output voltage for this one-quadrant, log-antilog multiplier/divider is ideally:

$$V_O = \frac{R_3 R_O}{R_1 R_2} \frac{V_X V_Y}{V_Z} \quad (V_X, V_Y, V_Z > 0) \quad (4)$$

If all the resistors (R_O, R_1, R_2, R_3) are made equal, then $V_O = V_X V_Y / V_Z$. Resistor values of 50kΩ to 100kΩ are recommended assuming an input range of 0.1V to +10V.

ERROR ANALYSIS

The base-to-emitter voltage of the MAT-02 in its forward-active operation is:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S} + r_{BE} I_C, V_{CB} \sim 0 \quad (5)$$

The first term comes from the idealized intrinsic transistor equation previously discussed (see equation (1)).

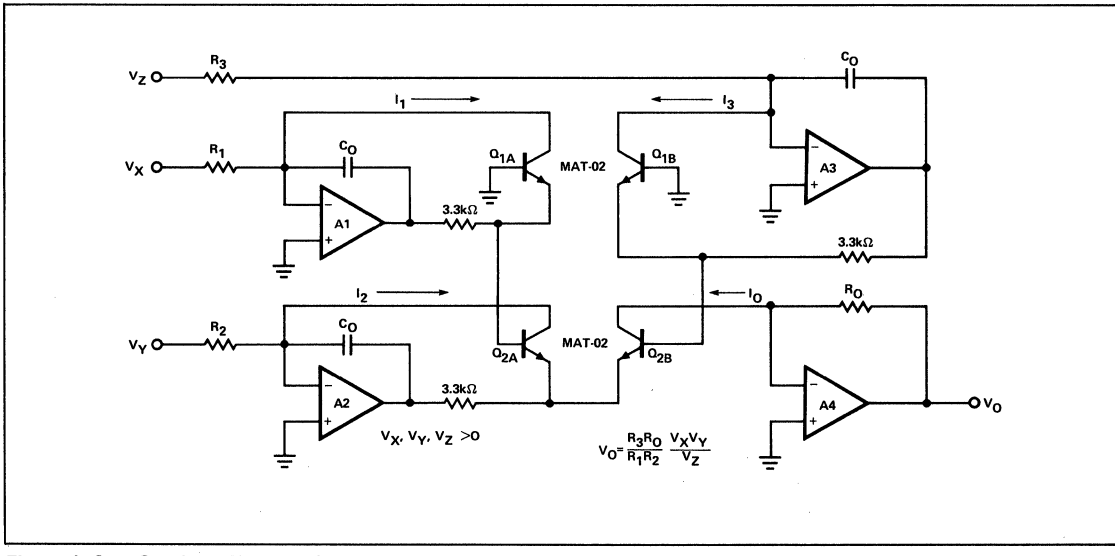


Figure 1. One-Quadrant Multiplier/Divider

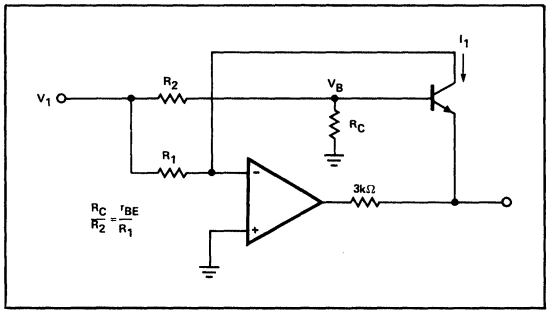


Figure 2. Compensation of Bulk Resistance Error

Extrinsic resistive terms and the Early effect cause departure from the ideal logarithmic relationship. For small V_{CB}, all of these effects can be lumped together as a total effective bulk resistance r_{BE}. The $r_{BE}I_C$ term causes departure from the desired logarithmic relationship. The r_{BE} term for the MAT-02 is less than 0.5Ω and Δr_{BE} between the two sides is negligible.

Returning to the multiplier/divider circuit of Figure 1 and using Equation (4):

$$V_{BE1A} + V_{BE2A} - V_{BE2B} - V_{BE1B} + (I_1 + I_2 - I_O - I_3)\, r_{BE} = 0$$

If the transistor pairs are held to the same temperature, then:

$$\frac{kT}{q} \ln \frac{I_1 I_2}{I_3 I_O} = \frac{kT}{q} \ln \frac{I_{S1A} I_{S2A}}{I_{S1B} I_{S2B}} + (I_1 + I_2 - I_O - I_3)\, r_{BE} \qquad (6)$$

If all the terms on the right-hand side were zero, then we would have $\ln (I_1 I_2/I_3 I_O)$ equal to zero which would lead directly to the desired result:

$$I_O = \frac{I_1 I_2}{I_3}, \text{ where } I_1, I_2, I_3, I_O > 0 \qquad (7)$$

Note that this relationship is temperature independent. The right-hand side of Equation (6) is near zero and the output current I_O will be approximately $I_1 I_2/I_3$. To estimate error, define ϕ as the right-hand side terms of Equation (6):

$$\phi = \ln \frac{I_{S1A} I_{S2A}}{I_{S1B} I_{S2B}} + \frac{q}{kT} (I_1 + I_2 - I_O - I_3)\, r_{BE} \qquad (8)$$

For the MAT-02, $\ln (I_{SA}/I_{SB})$ and $I_C r_{BE}$ are very small. For small ϕ, $\epsilon^{\phi} \sim 1 + \phi$ and therefore:

$$\frac{I_1 I_2}{I_3 I_O} = 1 + \phi$$

$$I_O \sim \frac{I_1 I_2}{I_3} (1 - \phi) \qquad (9)$$

The $\ln (I_{SA}/I_{SB})$ terms in ϕ cause a fixed gain error of less than ±0.6% from each pair when using the MAT-02, and this gain error is easily trimmed out by varying R_O. The $I_C r_{BE}$ terms are more troublesome because they vary with signal levels and are multiplied by absolute temperature. At 25°C, kT/q is approximately 26mV and the error due to an $r_{BE}I_C$ term will be $r_{BE}I_C/26mV$. Using an r_{BE} of 0.4Ω for the MAT-02 and assuming a collector-current range of up to 200μA, then a peak error of 0.3% could be expected for an $r_{BE}I_C$ error term when using the MAT-02. Total error is dependent on the specific application configuration (multiply, divide, square, etc.) and the required dynamic range. An obvious way to reduce $I_C r_{BE}$ error is to reduce the maximum collector current, but then op amp offsets and leakage currents become a limiting factor at low input levels. A design range of no greater than 10μA to 1mA is generally recommended for most nonlinear function circuits.

A powerful technique for reducing error due to $I_C r_{BE}$ is shown in Figure 2. A small voltage equal to $I_C r_{BE}$ is applied to the transistor base. For this circuit:

$$V_B = \frac{R_C}{R_2} V_1 \quad \text{and} \quad I_C r_{BE} = \frac{r_{BE}}{R_1} V_1 \qquad (10)$$

The error from $r_{BE}I_C$ is cancelled if R_C/R_2 is made equal to r_{BE}/R_1. Since the MAT-02 bulk resistance is approximately 0.39Ω, an R_C of 3.9Ω and R_2 of $10R_1$ will give good error cancellation.

In more complex circuits, such as the circuit in Figure 1, it may be inconvenient to apply a compensation voltage to each individual base. A better approach is to sum all compensation to the bases of Q1. The "A" side needs a base voltage of $(V_O/R_O + V_Z/R_3)\, r_{BE}$ and the "B" side needs a base voltage of $(V_X/R_1 + V_Y/R_2)\, r_{BE}$. Linearity of better than ±0.1% is readily achievable with this compensation technique.

Operational amplifier offsets are another source of error. In Figure 2, the input offset voltage and input bias current will cause an error in collector current of $(V_{OS}/R_1) + I_B$. A low offset op amp, such as the OP-07 with less than 75μV of V_{OS} and I_B of less than ±3nA, is recommended. The OP-22/32, a programmable micropower op amp, should be considered if low power consumption or single-supply operation is needed. The value of frequency-compensating capacitor (C_O) is dependent on the op amp frequency response and peak collector current. Typical values for C_O range from 30pF to 300pF.

FOUR-QUADRANT MULTIPLIER

A simplified schematic for a four-quadrant log/antilog multiplier is shown in Figure 3. As with the previously discussed one-quadrant multiplier, the circuit makes $I_O = I_1 I_2/I_3$. The two input currents, I_1 and I_2, are each offset in the positive direction. This positive offset is then subtracted out at the output stage. Assuming ideal op amps, the currents are:

$$I_1 = \frac{V_X}{R_1} + \frac{V_R}{R_2}, \; I_2 = \frac{V_Y}{R_1} + \frac{V_R}{R_2}$$

$$I_O = \frac{V_X}{R_1} + \frac{V_Y}{R_1} + \frac{V_R}{R_2} + \frac{V_O}{R_O}, \; I_3 = \frac{V_R}{R_2} \qquad (11)$$

From $I_O = I_1 I_2/I_3$, the output voltage will be:

$$V_O = \frac{R_O R_2}{R_1^2} \frac{V_X V_Y}{V_R} \qquad (12)$$

Collector-current range is the key design decision. The inherently low r_{BE} of the MAT-02 allows the use of a relatively high collector current. For input scaling of ±10V full-scale and using a 10V reference, we have a collector-current range for I_1 and I_2 of:

$$\left(\frac{-10}{R_1}+\frac{10}{R_2}\right) \leq I_C \leq \left(\frac{10}{R_1}+\frac{10}{R_2}\right) \quad (13)$$

Practical values for R_1 and R_2 would range from 50kΩ to 100kΩ. Choosing an R_1 of 82kΩ and R_2 of 62kΩ provides a collector-current range of approximately 39μA to 283μA. An R_O of 108kΩ will then make the output scale factor 1/10 and $V_O = V_X V_Y/10$. The output, as well as both inputs, are scaled for ±10V full-scale.

Linear error for this circuit is substantially improved by the small correction voltage applied to the base of Q1 as shown in Figure 3. Assuming an equal bulk emitter resistance for each MAT-02 transistor, then the error is nulled if:

$$(I_1 + I_2 - I_3 - I_O)\, r_{BE} + \rho V_O = 0$$

The currents are known from the previous discussion, and the relationship needed is simply:

$$V_O = \frac{r_{BE}}{R_O} V_O \quad (14)$$

The output voltage is attenuated by a factor of r_{BE}/R_O and applied to the base of Q1 to cancel the summation of voltage drops due to $r_{BE}I_C$ terms. This will make ln $(I_1\, I_2/I_3\, I_O)$ more nearly zero which will thereby make $I_O = I_1\, I_2/I_3$ a more accurate relationship. Linearity of better than 0.1% is readily achievable with this circuit if the MAT-02 pairs are carefully kept at the same temperature.

MULTIFUNCTION CONVERTER

The multifunction converter circuit provides an accurate means of squaring, square rooting, and of raising ratios to arbitrary powers. The excellent log conformity of the MAT-02 allows a wide range of exponents. The general transfer function is:

$$V_O = V_Y \left(\frac{V_Z}{V_X}\right)^m \quad (15)$$

V_X, V_Y, and V_Z are input voltages and the exponent "m" has a practical range of approximately 0.2 to 5. Inputs V_X and V_Y are often taken from a fixed reference voltage. With a REF-01 providing a precision +10V to both V_X and V_Y, the transfer function would simplify to:

$$V_O = 10 \left(\frac{V_Z}{10}\right)^m \quad (16)$$

As with the multiplier/divider circuits, assume that the transistor pairs have excellent matching and are at the same temperature. The ln I_{SA}/I_{SB} will then be zero. In the circuit of Figure 4, the voltage drops across the base-emitter junctions of Q1 provide:

$$\frac{R_B}{R_B + KR_A} V_A = \frac{kT}{q} \ln \frac{I_Z}{I_X} \quad (17)$$

I_Z is V_Z/R_1 and I_X is V_X/R_1. Similarly, the relationship for Q2 is:

$$\frac{R_B}{R_B + (1\text{-}K)R_A} V_A = \frac{kT}{q} \ln \frac{I_O}{I_Y} \quad (18)$$

I_O is V_O/R_O and I_Y is V_Y/R_1. These equations for Q1 and Q2 can then be combined.

$$\frac{R_B + KR_A}{R_B + (1\text{-}K)R_A} \ln \frac{I_Z}{I_X} = \ln \frac{I_O}{I_Y} \quad (19)$$

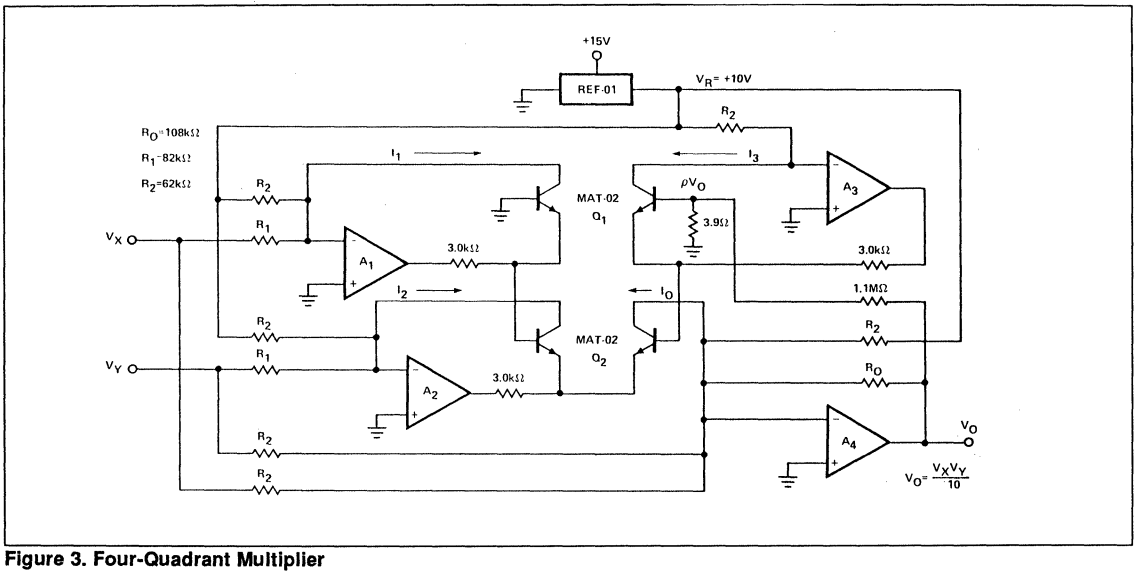


Figure 3. Four-Quadrant Multiplier

Substituting in the voltage relationships and simplifying leads to:

$$V_O = \frac{R_O}{R_1} V_Y \left(\frac{V_Z}{V_X}\right)^m \text{, where} \quad (20)$$

$$m = \frac{R_B + KR_A}{R_B + (1\text{-}K)\,R_A}$$

The factor "K" is a potentiometer position and varies from zero to 1.0, so "m" ranges from $R_B/(R_A+R_B)$ to $(R_B+R_A)/R_B$. Practical values are 125Ω for R_B and 500Ω for R_A; these values will provide an adjustment range of 0.2 to 5.0. A value of 100kΩ is recommended for the R_1 resistors assuming a full-scale input range of 10V. As with the one-quadrant multiplier/divider circuit previously discussed, the V_X, V_Y, and V_Z inputs must all be positive.

The op amps should have the lowest possible input offsets. The OP-07 is recommended for most applications, although such programmable micropower op amps as the OP-22 or OP-32 offer advantages in low-power or single-supply circuits. The micropower op amps also have very low input-bias-current drift, an important advantage in log/antilog circuits. External offset nulling may be needed, particularly for applications requiring a wide dynamic range. Frequency-compensating capacitors, on the order of 50pF, may be required for A2 and A3. Amplifier A1 is likely to need a larger capacitor, typically 0.0047μF, to assure stability.

Accuracy is limited at the higher input levels by bulk emitter resistance, but this is much lower for the MAT-02 than for other transistor pairs. Accuracy at the lower signal levels primarily depends on the op amp offsets. Accuracies of better than 1% are readily achievable with this circuit configuration and can be better than ±0.1% over a limited operating range.

FAST LOGARITHMIC AMPLIFIER

The circuit of Figure 5 is a modification of a standard logarithmic amplifier configuration. Running the MAT-02 at 2.5mA per side (full-scale) allows a fast response with wide dynamic range. The circuit has a 7 decade current range, a 5 decade voltage range, and is capable of 2.5μsec settling time to 1% with a 1 to 10V step.

The output follows the equation:

$$V_O = \frac{R_3 + R_2}{R_2} \frac{kT}{q} \ln \frac{V_{REF}}{V_{in}} \quad (21)$$

The output is inverted with respect to the input, and is nominally −1V/decade using the component values indicated.

LOW-NOISE ×1000 AMPLIFIER

The MAT-02 noise voltage is exceptionally low, only $1nV/\sqrt{Hz}$ at 10Hz when operated over a collector-current range of 1 to 4mA. A single-ended ×1000 amplifier that takes advantage of this low MAT-02 noise level is shown in Figure 6. In addition to low noise, the amplifier has very low drift and high CMRR. An OP-32 programmable low-power op amp is used for the second stage to obtain good speed with minimal power consumption. Small-signal bandwidth is 1MHz, slew-rate is 2.4V/μs, and total supply current is approximately 2.8mA.

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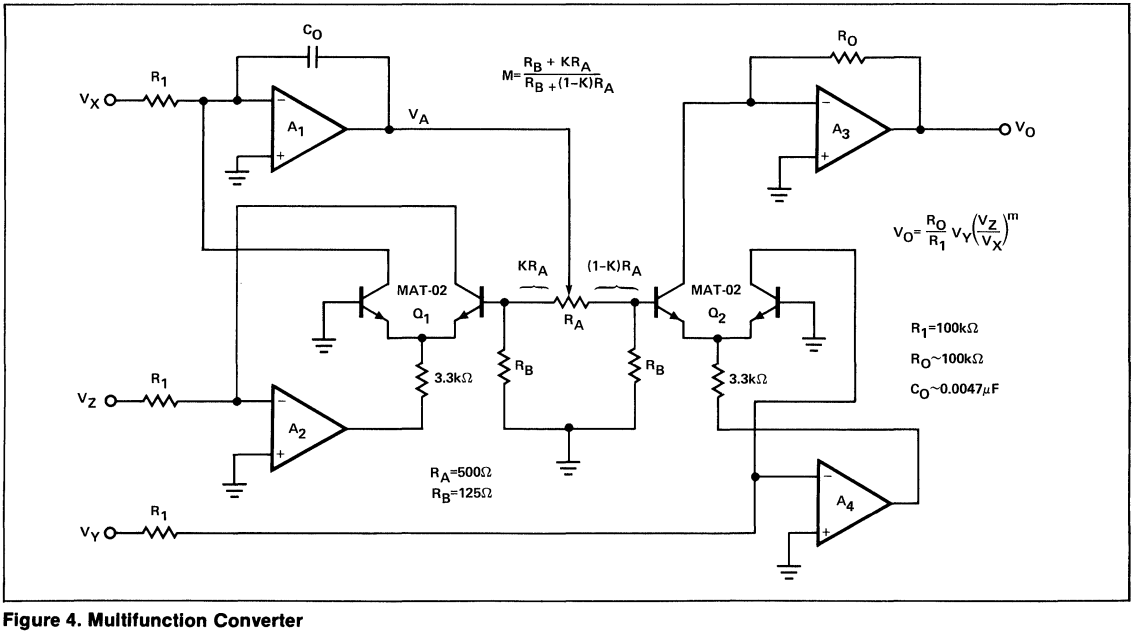


Figure 4. Multifunction Converter

Transistors Q2 and Q3 form a 2mA current source (0.65V/330Ω ~ 2mA). Each collector of Q1 operates at 1mA. The OP-32 inputs are 3V below the positive supply voltage ($R_L I_C$ ~ 3V). The OP-32's low input offset current, typically less than 1nA, and low offset voltage of 1mV cause negligible error when referred to the amplifier input. Input stage gain is $g_m R_L$, which is approximately 100 when operating at I_C of 1ma with R_L of 3kΩ. Since the OP-32 has a minimum open-loop gain of 500,000, total open-loop gain for the composite amplifier is over 50 million. Even at closed-loop gain of 1000, the gain error due to finite open-loop gain will be negligible. The OP-32 features excellent symmetry of slew-rate and very linear gain. Signal distortion is minimal.

Frequency compensation is very easy with this circuit; just vary the set-resistor R_S for the desired frequency response. Gain-bandwidth of the OP-32 varies directly with the supply current. A set resistor of 549kΩ was found to provide the best step response for this circuit. The resultant supply current is found from:

$$R_{SET} = \frac{(V+) - (V-) - (2V_{BE})}{I_{SET}}, \quad I_{SY} = 15\ I_{SET} \qquad (22)$$

The I_{SET}, using ±15V supplies and an R_{SET} of 549kΩ, is approximately 52μA which will result in supply current of 784μA.

Dynamic range of this amplifier is excellent; the OP-32 has an output voltage swing of ±14V with a ±15V supply.

Input characteristics are outstanding. The MAT-02B/F has offset voltage of less than 150μV at 25° C and a maximum offset drift of 1μV/° C. Nulling the offset will further reduce offset drift. This can be accomplished by slightly unbalancing the collector load resistors. This adjustment will reduce the drift to less than 0.1μV/° C.

Input bias current is relatively low due to the high current gain of the MAT-02. The minimum β of 400 at 1mA for the MAT-02B/F implies an input bias current of approximately 2.5μA. This circuit should be used with signals having relatively low source impedance. A high source impedance will degrade offset and noise performance.

This circuit configuration provides exceptionally low input noise voltage and low drift. Noise can be reduced even further by raising the collector currents from 1mA to 3mA, but power consumption is then increased.

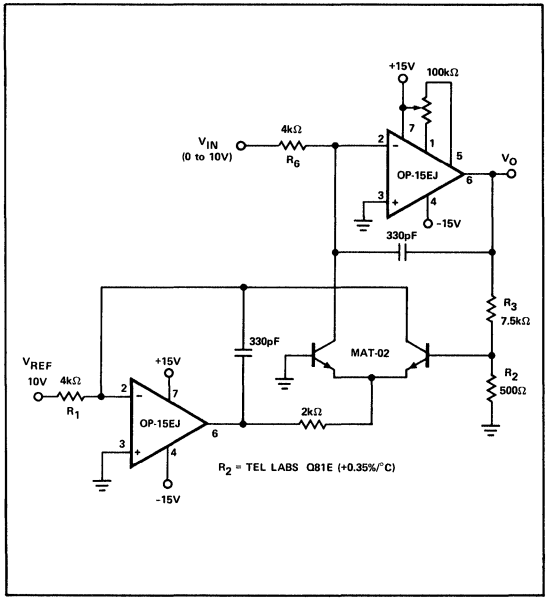


Figure 5. Fast Logarithmic Amplifier

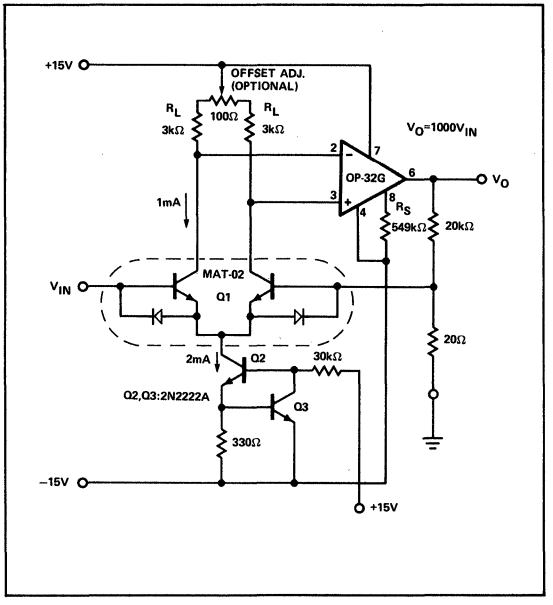


Figure 6. Low-Noise, Single-Ended X1000 Amplifier

ANALOG DEVICES

Low Noise, Matched Dual PNP Transistor

MAT-03

FEATURES

- **Dual Matched PNP Transistor**
- **Low Offset Voltage** ..... **100μV Max**
- **Low Noise** ..... **1nV/√Hz @ 1kHz Max**
- **High Gain** ..... **100 Min**
- **High Gain Bandwidth** ..... **190MHz Typ**
- **Tight Gain Matching** ..... **3% Max**
- **Excellent Logarithmic Conformance** ..... **$r_{BE} \simeq 0.3\Omega$ Typ**
- **Available in Die Form**

ORDERING INFORMATION†

$T_A = +25°C$ V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-78	LCC	
100	MAT03AH*	MAT03ARC/883	MIL
100	MAT03EH	—	XIND
200	MAT03FH	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

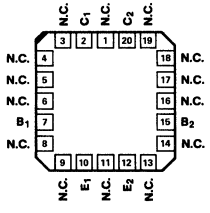
† Burn-in is available on industrial temperature range parts.

GENERAL DESCRIPTION

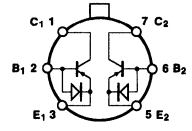
The MAT-03 dual monolithic PNP transistor offers excellent parametric matching and high frequency performance. Low noise characteristics (1nV/√Hz Max @ 1kHz), high bandwidth (190MHz typical), and low offset voltage (100μV Max), makes the MAT-03 an excellent choice for demanding preamplifier applications. Tight current gain matching (3% Max mismatch) and high current gain (100 Min), over a wide range of collector current, makes the MAT-03 an excellent choice for current mirrors. A low value of bulk resistance (typically 0.3Ω) also makes the MAT-03 an ideal component for applications requiring accurate logarithmic conformance.

Each transistor is individually tested to data sheet specifications. Device performance is guaranteed at 25°C and over the extended industrial and military temperature ranges. To insure the long-term stability of the matching parameters, internal protection diodes across the base-emitter junction clamp any reverse base-emitter junction potential. This prevents a base-emitter breakdown condition which can result in degradation of gain and matching performance due to excessive breakdown current.

PIN CONNECTIONS



MAT-03ARC/883
20-CONTACT LCC
(RC-Suffix)



TO-78
(H-Suffix)

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MAT-03

ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector-Base Voltage (BV_{CBO}) 36V
Collector-Emitter Voltage (BV_{CEO}) 36V
Collector-Collector Voltage (BV_{CC}) 36V
Emitter-Emitter Voltage (BV_{EE}) 36V
Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Total Power Dissipation
  Ambient Temperature ≤ 70°C (Note 2) 500mW
Operating Temperature Range
  MAT-03A ..... −55°C to +125°C
  MAT-03E/F ..... −40°C to +85°C
Operating Junction Temperature ..... −55°C to +150°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... −65°C to +150°C

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged devices.
2. Rating applies to TO-78 not using a heat sink, and LCC; devices in free air only. For TO-78, derate linearly at 6.3mW/°C above 70°C ambient temperature; for LCC, derate at 7.8mW/°C.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, unless otherwise noted.

			MAT-03A			MAT-03E			MAT-03F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Current Gain (Note 1)	h_{FE}	V_{CB} = 0V, −36V I_C = 1mA	100	165	—	100	165	—	80	165	—	
		I_C = 100μA	90	150	—	90	150	—	70	150	—	
		I_C = 10μA	80	120	—	80	120	—	60	120	—	
Current Gain Matching (Note 2)	Δh_{FE}	I_C = 100μA, V_{CB} = 0V	—	0.5	3	—	0.5	3	—	0.5	6	%
Offset Voltage (Note 3)	V_{OS}	V_{CB} = 0V, I_C = 100μA	—	40	100	—	40	100	—	40	200	μV
Offset Voltage Change vs Collector Voltage	$\Delta V_{OS}/\Delta V_{CB}$	I_C = 100μA V_{CB_1} = 0V V_{CB_2} = −36V	—	11	150	—	11	150	—	11	200	μV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V I_{C_1} = 10μA, I_{C_2} = 1mA	—	12	50	—	12	50	—	12	75	μV
Bulk Resistance	r_{BE}	V_{CB} = 0V, 10μA ≤ I_C ≤ 1mA	—	0.3	0.75	—	0.3	0.75	—	0.3	0.75	Ω
Offset Current	I_{OS}	I_C = 100μA, V_{CB} = 0V	—	6	35	—	6	35	—	6	45	nA
Collector-Base Leakage Current	I_{CB_0}	V_{CB} = −36V = V_{MAX}	—	50	200	—	50	200	—	50	400	pA
Noise Voltage Density (Note 4)	e_N	I_C = 1mA, V_{CB} = 0 fo = 10Hz	—	0.8	2	—	0.8	—	—	0.8	—	nV/√Hz
		fo = 100Hz	—	0.7	1	—	0.7	—	—	0.7	—	
		fo = 1kHz	—	0.7	1	—	0.7	—	—	0.7	—	
		fo = 10kHz	—	0.7	1	—	0.7	—	—	0.7	—	
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA, I_B = 100μA	—	0.025	0.1	—	0.025	0.1	—	0.025	0.1	V

NOTES:
1. Current gain is measured at collector-base voltages (V_{CB}) swept from 0 to V_{MAX} at indicated collector current. Typicals are measured at V_{CB} = 0V.
2. Current gain matching (Δh_{FE}) is defined as:
$$\Delta h_{FE} = \frac{100\,(\Delta I_B)\;h_{FE}\,(MIN)}{I_C}.$$
3. Offset voltage is defined as:
$V_{OS} = V_{BE_1} - V_{BE_2}$,
where V_{OS} is the differential voltage for
$$I_{C_1} = I_{C_2}: V_{OS} = V_{BE_1} - V_{BE_2} = \frac{KT}{q} \ln\left(\frac{I_{C_1}}{I_{C_2}}\right).$$
4. Sample tested. Noise tested and specified as equivalent input voltage for each transistor.

ELECTRICAL CHARACTERISTICS at $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-03A MIN	MAT-03A TYP	MAT-03A MAX	UNITS
		V_{CB} = 0V, −36V				
		I_C = 1mA	70	110	—	
Current Gain	h_{FE}	I_C = 100μA	60	100	—	
		I_C = 10μA	50	85	—	
Offset Voltage	V_{OS}	I_C = 100μA, V_{CB} = 0V	—	40	150	μV
Offset Voltage Drift (Note 1)	TCV_{OS}	I_C = 100μA, V_{CB} = 0V	—	0.3	0.5	μV/°C
Offset Current	I_{OS}	I_C = 100μA, V_{CB} = 0V	—	15	85	nA
Breakdown Voltage	BV_{CEO}		36	54	—	V

NOTE:
1. Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} \ll V_{BE}$) where T = 298°K for T_A = 25°C.

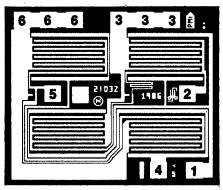
ELECTRICAL CHARACTERISTICS at $-40°C \leq T_A \leq +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-03E MIN	MAT-03E TYP	MAT-03E MAX	MAT-03F MIN	MAT-03F TYP	MAT-03F MAX	UNITS
		V_{CB} = 0V, −36V							
		I_C = 1mA	70	120	—	60	120	—	
Current Gain	h_{FE}	I_C = 100μA	60	105	—	50	105	—	
		I_C = 10μA	50	90	—	40	90	—	
Offset Voltage	V_{OS}	I_C = 100μA, V_{CB} = 0V	—	30	135	—	30	265	μV
Offset Voltage Drift (Note 1)	TCV_{OS}	I_C = 100μA, V_{CB} = 0V	—	0.3	0.5	—	0.3	1.0	μV/°C
Offset Current	I_{OS}	I_C = 100μA, V_{CB} = 0V	—	10	85	—	10	200	nA
Breakdown Voltage	BV_{CEO}		36	—	—	36	—	—	V

NOTE:
1. Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} \ll V_{BE}$) where T = 298°K for T_A = 25°C.

MAT-03

DICE CHARACTERISTICS



DIE SIZE 0.070 × 0.060 inch, 4,200 sq. mils
(1.78 × 1.52 mm, 2.70 sq. mm)

1. COLLECTOR 1
2. BASE 1
3. EMITTER 1
4. COLLECTOR 2
5. BASE 2
6. EMITTER 2

Substrate can be connected to V– or floated.

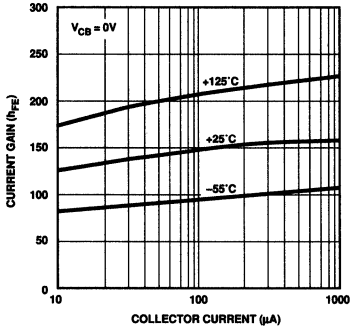
WAFER TEST LIMITS at 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-03N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}		36	V MIN
Offset Voltage	V_{OS}	$I_C = 100\mu A$, $V_{CB} = 0V$ $10\mu A \le I_C \le 1mA$	200	μV MAX
Current Gain	h_{FE}	$I_C = 1mA$, $V_{CB} = 0V$, -36 V $I_C = 10\mu A$, $V_{CB} = 0V$, $-36V$	80 60	MIN
Current Gain Match	Δh_{FE}	$I_C = 100\mu A$, $V_{CB} = 0V$	6	% MAX
Offset Voltage Change vs. V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$V_{CB_1} = 0V$, $I_C = 100\mu A$ $V_{CB_2} = -36V$	200	μV MAX
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	$V_{CB} = 0$ $I_{C_1} = 10\mu A$, $I_{C_2} = 1mA$	75	μV MAX
Bulk Resistance	r_{BE}	$10\mu A \le I_C \le 1mA$	0.75	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1mA$ $I_B = 100\mu A$	0.1	V MAX

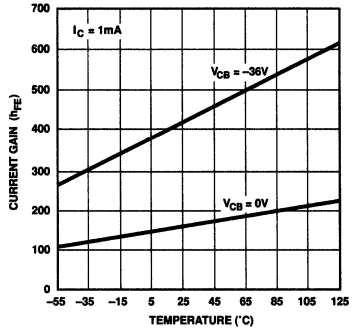
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

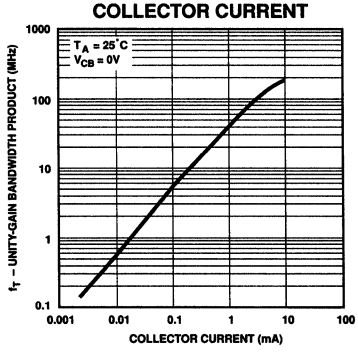
CURRENT GAIN vs COLLECTOR CURRENT



CURRENT GAIN vs TEMPERATURE

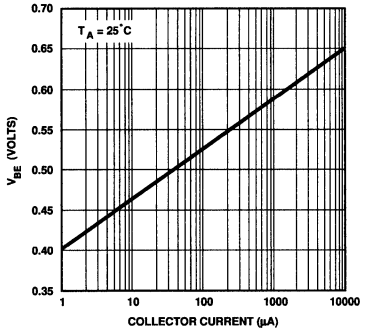


GAIN BANDWIDTH vs COLLECTOR CURRENT

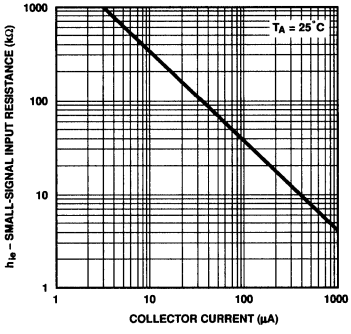


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

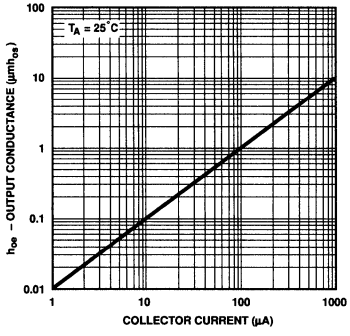
BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT



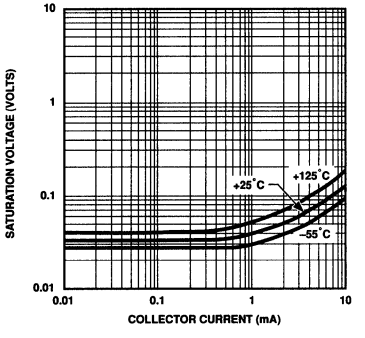
SMALL-SIGNAL INPUT RESISTANCE (h_{ie}) vs COLLECTOR CURRENT



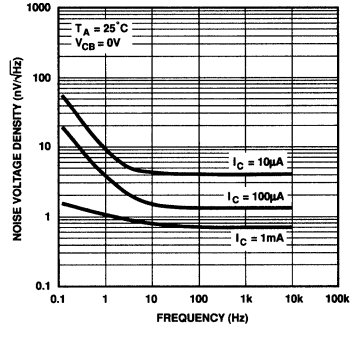
SMALL-SIGNAL OUTPUT CONDUCTANCE (h_{oe}) vs COLLECTOR CURRENT



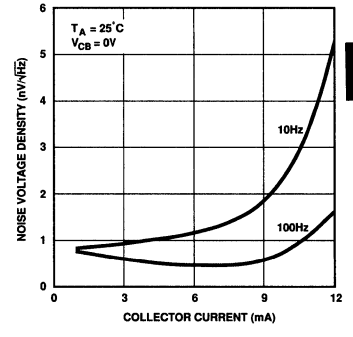
SATURATION VOLTAGE vs COLLECTOR CURRENT



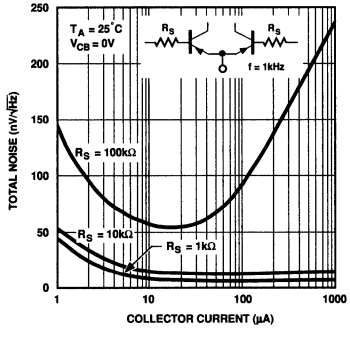
NOISE VOLTAGE DENSITY vs FREQUENCY



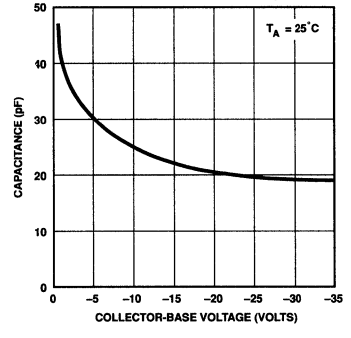
NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



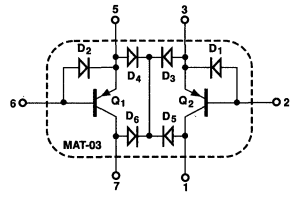
TOTAL NOISE vs COLLECTOR CURRENT



COLLECTOR-BASE CAPACITANCE vs V_{CB}



8



SPICE MODEL PARAMETERS

```
•SUBCKT MAT03 1 2 3 5 6 7
Q1 1 2 3 PMAT
Q2 7 6 5 PMAT
D1 2 3 DMAT1
D2 6 5 DMAT1
D3 3 4 DMAT1
D4 5 4 DMAT1
D5 1 4 DMAT2
D6 7 4 DMAT2
•MODEL DMAT1 D IS = 7.2E-16 RS = 20
•MODEL DMAT2 D IS = 1E-14 VJ = 0.6 CJ = 68P
•MODEL PMAT PNP BF = 160 IS = 1.4E-13 VAF = 60 BR = 5 VAR = 7 RB = 16
+ PC = 12 RE = 0.35 CJE = 57P VJE = 0.7 MJE = 0.4 IF = 1.08E-9
+ TR = 3E-8 CJC = 40P VJC = 0.55 MJC = 0.5 CJS = 0 IKF =1 60M)
```

SABER* MODEL PARAMETERS

```
template mat03 n1 n2 n3 n5 n6 n7
electrical n1,n2,n3,n5,n6,n7
{
d..model dmat1 = (is = 7.2e-16,rs = 20)
d..model dmat2 = (is = 1e-14,vj = 0.6,cjo = 68p)
q..model pmat = (type = __ p,bf = 160, is = 1.4e-13,vaf = 60,br = 5,var = 7,
rb = 16,rc = 12,re = 0.45,cje = 57p,vje = 0.7,mje = 0.4,tf = 1.08e-9,tr = 3e-8,
cjc = 40p,vjc = 0.55, mjc = 0.5,cjs = 0,ikf = 160m)
q.q1 n1 n2 n3 n4 = model = pmat
q.q2 n7 n6 n5 n4 = model = pmat
d.d1 n2 n3 = model = dmat1
d.d2 n6 n5 = model = dmat1
d.d3 n3 n4 = model = dmat1
d.d4 n5 n4 = model = dmat1
d.d5 n1 n4 = model = dmat2
d.d6 n7 n4 = model = dmat2
}
```

*SABER is a registered trademark of Analogy Inc.

FIGURE 1: *SPICE or SABER Model*

APPLICATIONS INFORMATION

MAT-03 MODELS

The MAT-03 model (Figure 1) includes parasitic diodes D_3 through D_6. D_1 and D_2 are internal protection diodes which prevent zenering of the base-emitter junctions.

The analysis programs, SPICE and SABER, are primarily used in evaluating the functional performance of systems. The models are provided only as an aid in utilizing these simulation programs.

MAT-03 NOISE MEASUREMENT

All resistive components (Johnson noise, $e_n^2 = 4kTBR$, or $e_n = 0.13\sqrt{R}$ nV/$\sqrt{Hz}$, where R is in kΩ) and semiconductor junctions (Shot noise, caused by current flowing through a junction, produces voltage noise in series impedances such as transistor-collector load resistors, $I_n = 0.566\sqrt{I}$ pA/$\sqrt{Hz}$ where I is in μA) contribute to the system input noise.

Figure 2 illustrates a technique for measuring the equivalent input noise voltage of the MAT-03. 1mA of stage current is used

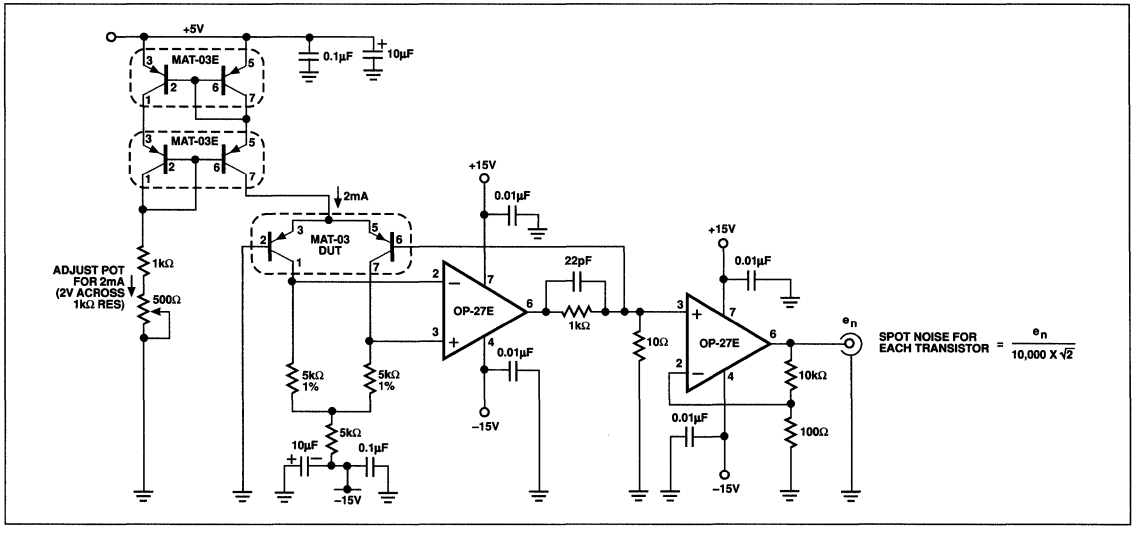


FIGURE 2: *MAT-03 Voltage Noise Measurement Circuit*

to bias each side of the differential pair. The 5kΩ collector resistors noise contribution is insignificant compared to the voltage noise of the MAT-03. Since noise in the signal path is referred back to the input, this voltage noise is attenuated by the gain of the circuit. Consequently, the noise contribution of the collector load resistors is only $0.048nV/\sqrt{Hz}$. This is considerably less than the typical $0.8nV/\sqrt{Hz}$ input noise voltage of the MAT-03 transistor.

The noise contribution of the OP-27 gain stages is also negligible due to the gain in the signal path. The op amp stages amplify the input referred noise of the transistors to increase the signal strength to allow the noise spectral density ($e_n \times 10000$) to be measured with a spectrum analyzer. And, since we assume equal noise contributions from each transistor in the MAT-03, the output is divided by $\sqrt{2}$ to determine a single transistor's input noise.

Air currents cause small temperature changes that can appear as low frequency noise. To eliminate this noise source, the measurement circuit must be thermally isolated. Effects of extraneous noise sources must also be eliminated by totally shielding the circuit.

SUPER LOW NOISE AMPLIFIER

The circuit in Figure 3a is a super low noise amplifier with equivalent input voltage noise of $0.32nV/\sqrt{Hz}$. By paralleling three MAT-03 matched pairs, a further reduction of amplifier noise is attained by a reduction of the base spreading resistance by a factor of 3, and consequently the noise by $\sqrt{3}$. Additionally, the shot noise contribution is reduced by maintaining a high collector current (2mA/device) which reduces the dynamic emitter resistance and decreases voltage noise. The voltage noise is inversely proportional to the square root of the stage current, and current noise increases proportionally to the square root of the stage current. Accordingly, this amplifier capitalizes on voltage noise reduction techniques at the expense of increasing the current noise. However, high current noise is not usually important when dealing with low impedance sources.

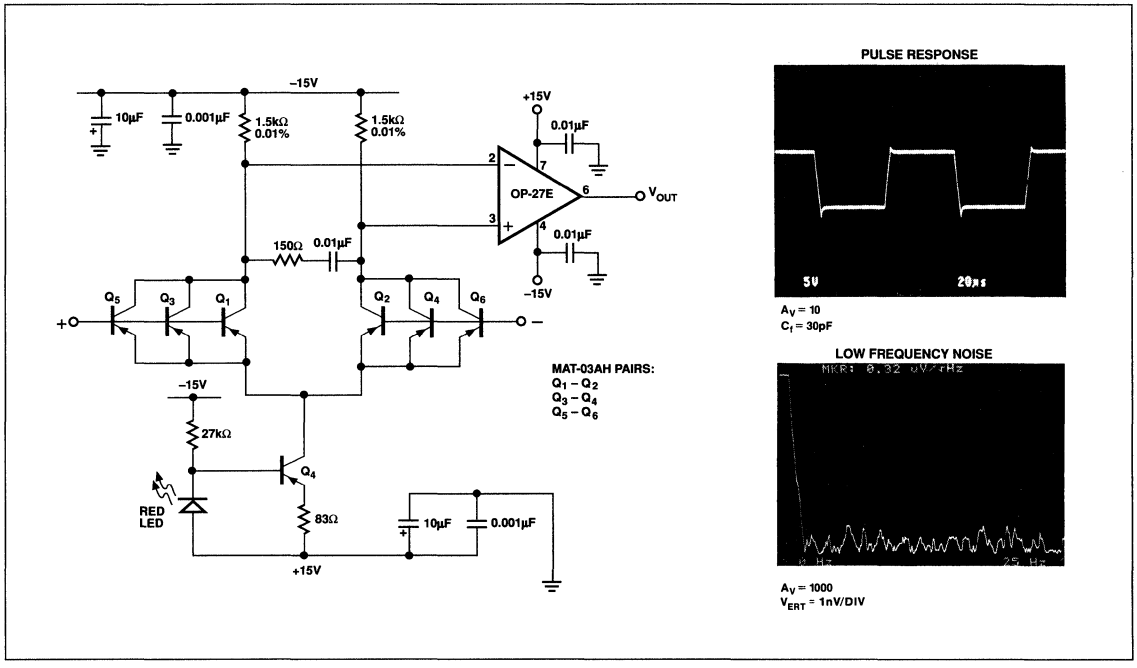


FIGURE 3a: *Super Low Noise Amplifier*

This amplifier exhibits excellent full power AC performance, 0.08% THD into a 600Ω load, making it suitable for exacting audio applications (see Figure 3b).

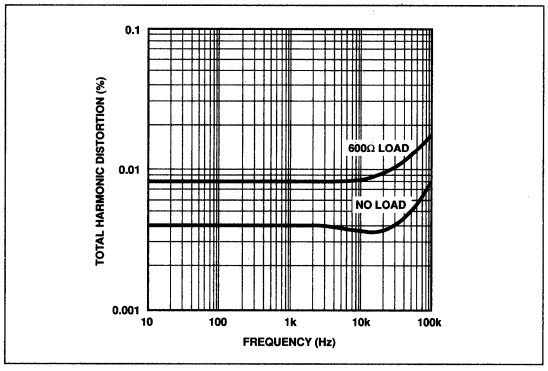


FIGURE 3b: *Super Low Noise Amplifier – Total Harmonic Distortion*

LOW NOISE MICROPHONE PREAMPLIFIER

Figure 4 shows a microphone preamplifier that consists of a MAT-03 and a low noise op amp. The input stage operates at a relatively high quiescent current of 2mA per side, which reduces the MAT-03 transistor's voltage noise. The $1/f$ corner is less than 1Hz. Total harmonic distortion is under 0.005% for a $10V_{p-p}$ signal from 20Hz to 20kHz. The preamp gain is 100, but can be modified by varying R_5 or R_6 ($V_{OUT}/V_{IN} = R_5/R_6 + 1$).

A total input stage emitter current of 4mA is provided by Q_2. The constant current in Q_2 is set by using the forward voltage of a GaAsP LED as a reference. The difference between this voltage and the V_{BE} of a silicon transistor is predictable and constant (to a few percent) over a wide temperature range. The voltage difference, approximately 1V, is dropped across the 250Ω resistor which produces a temperature stabilized emitter current.

CURRENT SOURCES

A fundamental requirement for accurate current mirrors and active load stages is matched transistor components. Due to the excellent V_{BE} matching (the voltage difference between V_{BE}'s required to equalize collector current) and gain matching, the MAT-03 can be used to implement a variety of standard current mirrors that can source current into a load such as an amplifier stage. The advantages of current loads in amplifiers versus resistors is an increase of voltage gain due to higher impedances, larger signal range, and in many applications a wider signal bandwidth.

Figure 5 illustrates a cascode current mirror consisting of two MAT-03 transistor pairs.

The cascode current source has a common base transistor in series with the output which causes an increase in output impedance of the current source since V_{CE} stays relatively constant. High frequency characteristics are improved due to a reduction of Miller capacitance. The small-signal output impedance can be determined by consulting "h_{OF} vs Collector Current" typical graph. Typical output impedance levels approach the performance of a perfect current source.

Considering a typical collector current of 100μA, we have:

$$ro_{Q3} = \frac{1}{1.0\mu MHOS} = 1M\Omega.$$

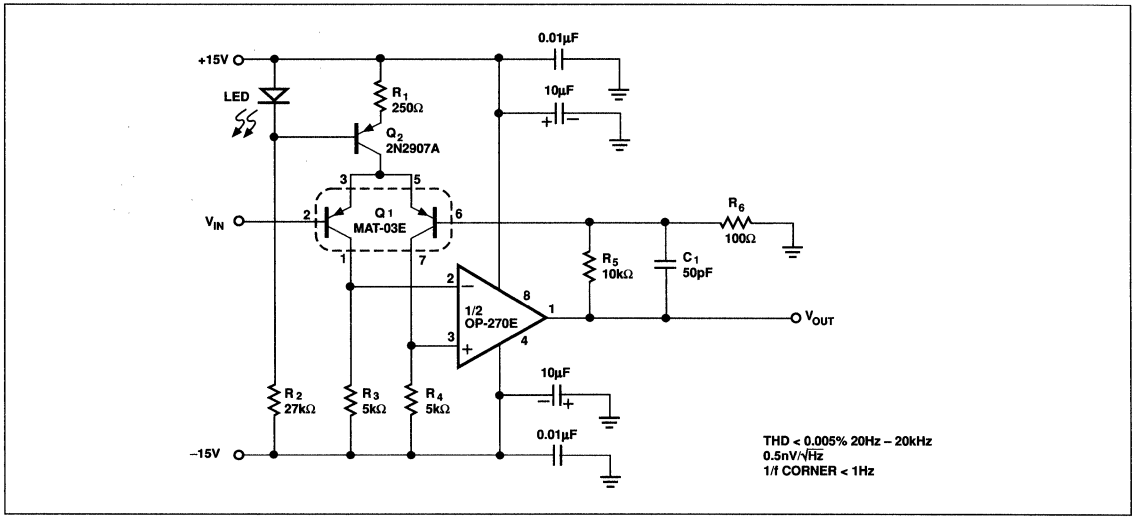


FIGURE 4: *Low Noise Microphone Preamplifier*

Q_2 and Q_3 are in series and operate at the same current level, so the total output impedance is:

$R_O = h_{FE}\, ro_{Q_3} \simeq (160)(1M\Omega) = 160M\Omega$.

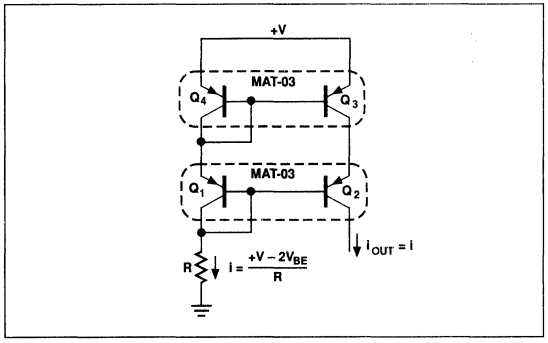


FIGURE 5: *Cascode Current Source*

CURRENT MATCHING

The objective of current source or mirror design is generation of currents that are either matched or must maintain a constant ratio. However, mismatch of base-emitter voltages cause output current errors. Consider the example of Figure 6a. If the resistors and transistors are equal and the collector voltages are the same, the collector currents will match precisely. Investigating the current-matching errors resulting from a non-zero V_{OS}, we define ΔI_C as the current error between the two transistors.

Graph 6b describes the relationship of current matching errors versus offset voltage for a specified average current I_C. Note that since the relative error between the currents is exponentially proportional to the offset voltage, tight matching is required to design high accuracy current sources. For example, if the offset voltage is 5mV at 100μA collector current, the current matching error would be 20%. Additionally, temperature effects such as offset drift (3μV/°C per mV of V_{OS}) will degrade performance if Q_1 and Q_2 are not well matched.

DIGITALLY PROGRAMMABLE BIPOLAR CURRENT PUMP

The circuit of Figure 7 is a digitally programmable current pump. The current pump incorporates a DAC-08, and a fast Wilson current source using the MAT-03. Examining Figure 7, the DAC-08 is set for 2mA full-scale range so that bipolar current operation of ±2mA is achieved. The Wilson current mirror maintains linearity within the LSB range of the 8-bit DAC-08 (±2mA/256 = 15.6μA resolution) as seen in Figure 8. A negative feedback path established by Q_2 regulates the collector current so that it matches the reference current programmed by the DAC-08.

Collector-emitter voltages across both Q_1 and Q_3 are matched by D_1, with Q_3's collector-emitter voltage remaining constant, independent of the voltage across the current source output.

Since Q_2 buffers Q_3, both transistors in the MAT-03, Q_1 and Q_3, maintain the same collector current. D_2 and D_3 form a Baker clamp which prevents Q_2 from turning off, thereby improving the switching speed of the current mirror. The feedback serves to increase the output impedance and improves accuracy by reducing the base-width modulation which occurs with varying collector-emitter voltages. Accuracy and linearity performance of the current pump is summarized in Figure 8.

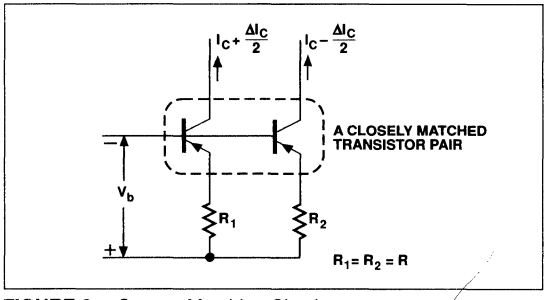


FIGURE 6a: *Current Matching Circuit*

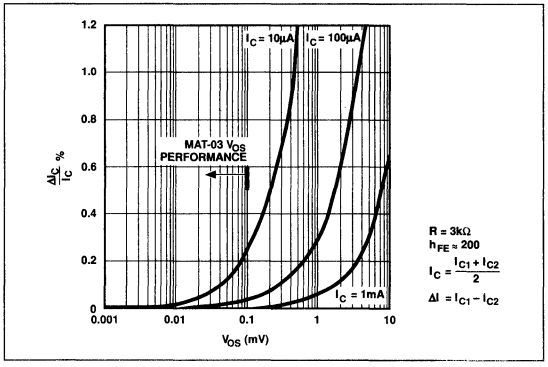


FIGURE 6b: *Current Matching Accuracy % vs Offset Voltage*

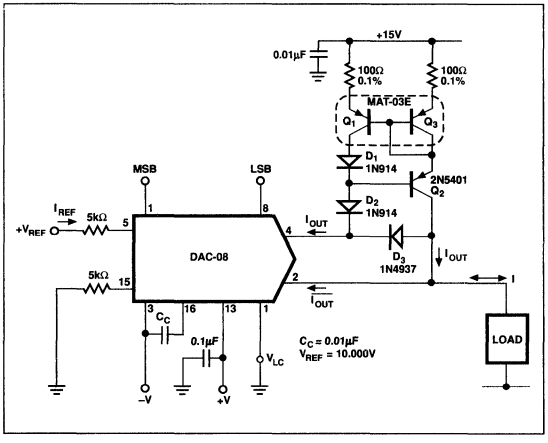


FIGURE 7: *Digitally Programmable Bipolar Current Pump*

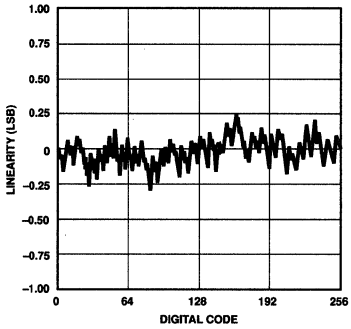


FIGURE 8: *Digitally Programmable Current Pump – INL Error vs Digital Code*

The full scale output of the DAC-08, I_{OUT}, is a linear function of I_{REF}:

$$I_{FR} = \frac{255}{256} \times I_{REF}, \text{ and } I_{OUT} + \overline{I_{OUT}} = I_{REF}\left(\frac{255}{256}\right).$$

The current mirror output is $I_{OUT} - \overline{I_{OUT}} = I$, so that if $I_{REF} = 2mA$:

$$I = 2\, I_{OUT} - 1.992mA$$

$$= 2\left(\frac{\text{Input Code}}{256}\right)(2mA) - 1.992mA.$$

DIGITAL CURRENT PUMP CODING

	DIGITAL INPUT B1 . . . B8	OUTPUT CURRENT
FULL RANGE	1111 1111	I = 1.992mA
HALF-RANGE	1000 0000	I = 0.008mA
ZERO-SCALE	0000 0000	I = -1.992mA

ANALOG DEVICES

Matched Monolithic Quad Transistor

MAT-04

FEATURES

- **Low Offset Voltage ..... 200μV Max**
- **High Current Gain ..... 400 Min**
- **Excellent Current Gain Match ..... 2% Max**
- **Low Noise Voltage at 100Hz, 1mA ..... 2.5nV/ Hz Max**
- **Excellent Log Conformance ..... rBE = 0.6Ω Max**
- **Matching Guaranteed for All Transistors**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (μV)	PACKAGE CERDIP 14-PIN	PACKAGE PLASTIC 14-PIN	OPERATING TEMPERATURE RANGE
200	MAT04AY*	—	MIL
200	MAT04EY	—	IND
400	MAT04BY*	—	MIL
400	MAT04FY	MAT04FP	XIND
400	—	MAT04FS††	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

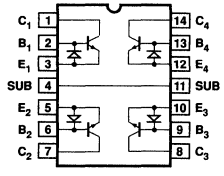
GENERAL DESCRIPTION

The MAT-04 is a quad monolithic NPN transistor that offers excellent parametric matching for precision amplifier and non-linear circuit applications. Performance characteristics of the MAT-04 include high gain (400 minimum) over a wide range of collector current, low noise (2.5nV/$\sqrt{Hz}$ maximum at 100Hz, I_C = 1 mA) and excellent logarithmic conformance. The MAT-04 also features a low offset voltage of 200μV and tight current gain matching, to within 2%. Each transistor of the MAT-04 is individually tested to data sheet specifications. For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are verified to meet stated limits. Device performance is guaranteed at 25°C and over the industrial and military temperature ranges.

The long-term stability of matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias base-emitter current.

The superior logarithmic conformance and accurate matching characteristics of the MAT-04 makes it an excellent choice for use in log and antilog circuits. The MAT-04 is an ideal choice in applications where low noise and high gain are required.

PIN CONNECTIONS



14-PIN CERDIP (Y-Suffix)
14-PIN PLASTIC DIP (P-Suffix)
14-PIN SO (S-Suffix)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector-Base Voltage (BV_{CBO}) 40V
Collector-Emitter Voltage (BV_{CEO}) 40V
Collector-Collector Voltage (BV_{CC}) 40V
Emitter-Emitter Voltage (BV_{EE}) 40V
Collector Current 30mA
Emitter Current 30mA
Substrate (Pin-4 to Pin-11) Current 30mA
Operating Temperature Range
MAT-04AY, BY ..... –55°C TO +125°C
MAT-04EY ..... –25°C TO +85°C
MAT-04FY,FP,FS ..... –40°C to +85°C
Storage Temperature
Y Package ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
14-Pin CERDIP (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SO (S)	120	36	°C/W

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

8

ELECTRICAL CHARACTERISTICS at T_A = 25°C unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}, Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

			MAT-04A/E			MAT-04B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Current Gain	h_{FE}	10μA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 1)	400	800	—	300	600	—	
Current Gain Match	Δh_{FE}	I_C = 100μA 0V ≤ V_{CB} ≤ 30V (Note 2)	—	0.5	2	—	1	4	%
Offset Voltage	V_{OS}	10μA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 4)	—	50	200	—	100	400	μV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	10μA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 4)	—	5	25	—	10	50	μV
Offset Voltage Change vs V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	10μA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 4)	—	50	100	—	100	200	μV
Bulk Emitter Resistance	r_{BE}	10μA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 5)	—	0.4	0.6	—	0.4	0.6	Ω
Input Bias Current	I_B	I_C = 100μA 0V ≤ V_{CB} ≤ 30V	—	125	250	—	165	330	nA
Input Offset Current	I_{OS}	I_C = 100μA V_{CB} = 0V	—	0.6	5	—	2	13	nA
Breakdown Voltage	BV_{CEO}	I_C = 10μA	40	—	—	40	—	—	V
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 100μA I_C = 1mA	—	0.03	0.06	—	0.03	0.06	V
Collector-Base Leakage Current	I_{CBO}	V_{CB} = 40V	—	5	—	—	5	—	pA
Noise Voltage Density	e_n	V_{CB} = 0V f_O = 10Hz I_C = 1mA f_O = 100Hz (Note 3) f_O = 1kHz	— — —	2 1.8 1.8	3 2.5 2.5	— — —	2 1.8 1.8	4 3 3	nV/√Hz
Gain Bandwidth Product	f_T	I_C = 1mA V_{CE} = 10V	—	300	—	—	300	—	MHz
Output Capacitance	C_{OBO}	V_{CB} = 15V I_E = 0 f = 1MHz	—	10	—	—	10	—	pF
Input Capacitance	C_{EBO}	V_{BE} = 0V I_C = 0 f = 1MHz	—	40	—	—	40	—	pF

NOTES:

1. Current gain measured at I_C = 10μA, 100μA and 1mA.
2. Current gain match is defined as: $\Delta h_{FE} = \frac{100\,(\Delta I_B)\,(h_{FE}\,\text{min})}{I_C}$
3. Sample tested.
4. Measured at I_C = 10μA and guaranteed by design over the specified range of I_C.
5. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at $-25°C \le T_A \le +85°C$ for MAT-04E, $-40°C \le T_A \le +85°C$ for MAT-04F, unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

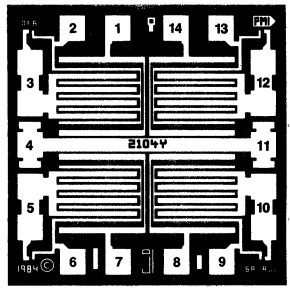
PARAMETER	SYMBOL	CONDITIONS	MAT-04E MIN	MAT-04E TYP	MAT-04E MAX	MAT-04F MIN	MAT-04F TYP	MAT-04F MAX	UNITS
Current Gain	h_{FE}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 1)	225	625	—	200	500	—	
Offset Voltage	V_{OS}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 3)	—	60	260	—	120	520	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$ (Note 2)	—	0.2	1	—	0.4	2	μV/°C
Input Bias Current	I_B	$I_C = 100\mu A$ $0V \le V_{CB} \le 30V$	—	160	445	—	200	500	nA
Input Offset Current	I_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	4	20	—	8	40	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	50	—	—	100	—	pA/°C
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu A$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40V$	—	0.5	—	—	0.5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40V$	—	5	—	—	5	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40V$	—	0.7	—	—	0.7	—	nA

ELECTRICAL CHARACTERISTICS at $-55°C \le T_A \le 125°C$ unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04A MIN	MAT-04A TYP	MAT-04A MAX	MAT-04B MIN	MAT-04B TYP	MAT-04B MAX	UNITS
Current Gain	h_{FE}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 1)	175	475	—	125	425	—	
Offset Voltage	V_{OS}	$10\mu A \le I_C \le 1mA$ $0V \le V_{CB} \le 30V$ (Note 3)	—	70	300	—	140	600	μV
Average Offset Voltage Drift	TCV_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$ (Note 2)	—	0.2	1	—	0.4	2	μV/°C
Input Bias Current	I_B	$I_C = 100\mu A$ $0V \le V_{CB} \le 30V$	—	210	570	—	235	800	nA
Input Offset Current	I_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	6	30	—	12	60	nA
Average Offset Current Drift	TCI_{OS}	$I_C = 100\mu A$ $V_{CB} = 0V$	—	50	—	—	100	—	pA/°C
Breakdown Voltage	BV_{CEO}	$I_C = 10\mu A$	40	—	—	40	—	—	V
Collector-Base Leakage Current	I_{CBO}	$V_{CB} = 40V$	—	5	—	—	5	—	nA
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = 40V$	—	100	—	—	100	—	nA
Collector-Substrate Leakage Current	I_{CS}	$V_{CS} = 40V$	—	7	—	—	7	—	nA

NOTES:
1. Current gain measured at $I_C = 10\mu A$, $100\mu A$ and 1mA.
2. Guaranteed by V_{OS} test ($TCV_{OS} \le V_{OS}/T$ for $V_{OS} << V_{BE}$) $T = 298°K$ for $T_A = 25°C$.
3. Measured at $I_C = 10\mu A$ and guaranteed by design over the specified range of I_C.

DICE CHARACTERISTICS



DIE SIZE 0.060 x 0.060 inch, 3600 sq. mils
(1.52 x 1.52 mm, 2.31 sq. mm)

1. Q_1 COLLECTOR
2. Q_1 BASE
3. Q_1 EMITTER
4. SUBSTRATE
5. Q_2 EMITTER
6. Q_2 BASE
7. Q_2 COLLECTOR
8. Q_3 COLLECTOR
9. Q_3 BASE
10. Q_3 EMITTER
11. SUBSTRATE
12. Q_4 EMITTER
13. Q_4 BASE
14. Q_4 COLLECTOR

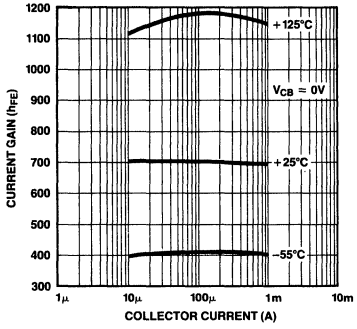
WAFER TEST LIMITS at T_A = +25°C unless otherwise noted. Each transistor is individually tested. For matching parameters (V_{OS}, I_{OS}, Δh_{FE}) each dual transistor combination is verified to meet stated limits. All tests made at endpoints unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-04N LIMITS	UNITS
Current Gain	h_{FE}	I_C = 100µA 0V ≤ V_{CB} ≤ 30V	300	MIN
Current Gain Match	Δh_{FE}	I_C = 100µA, V_{CB} = 0V	4	% MAX
Offset Voltage	V_{OS}	10µA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 1)	400	µV MAX
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	10µA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 1)	50	µV MAX
Offset Voltage Change us VCB	$\Delta V_{OS}/\Delta V_{CB}$	10µA ≤ I_C ≤ 1mA 0V ≤ V_{CB} ≤ 30V (Note 1)	200	µV MAX
Bulk Emitter Resistance	r_{BE}	10µA ≤ I_C ≤ 1mA V_{CB} = 0V (Note 2)	0.6	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	I_B = 100µA I_C = 1mA	0.06	V MAX
Input Bias Current	I_B	I_C = 100µA 0V ≤ V_{CB} ≤ 30V	330	nA MAX
Input Offset Current	I_{OS}	I_C = 100µA V_{CB} = 0V	13	nA MAX
Breakdown Voltage	BV_{CEO}	I_C = 10µA	40	V MIN

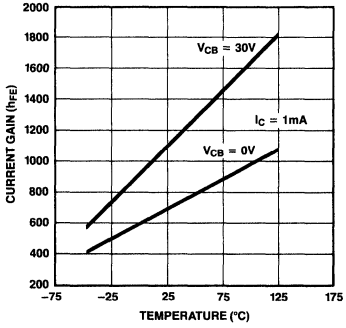
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

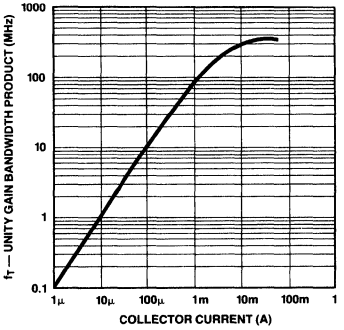
CURRENT GAIN vs COLLECTOR CURRENT



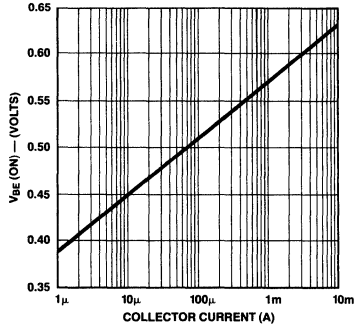
CURRENT GAIN vs TEMPERATURE



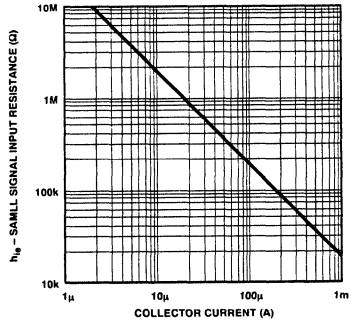
GAIN BANDWIDTH vs COLLECTOR CURRENT



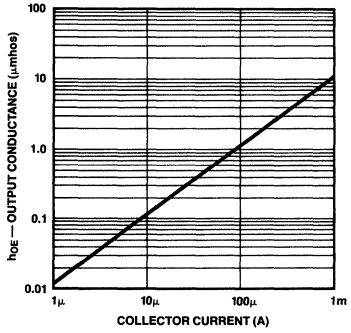
BASE-EMITTER-ON-VOLTAGE vs COLLECTOR CURRENT



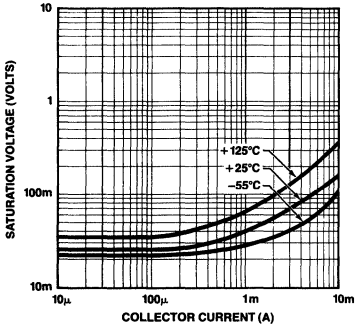
SMALL SIGNAL INPUT RESISTANCE (h_{ie}) vs COLLECTOR CURRENT



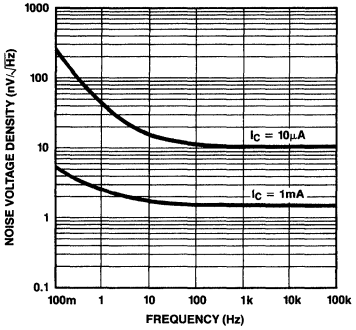
SMALL SIGNAL OUTPUT CONDUCTANCE vs COLLECTOR CURRENT



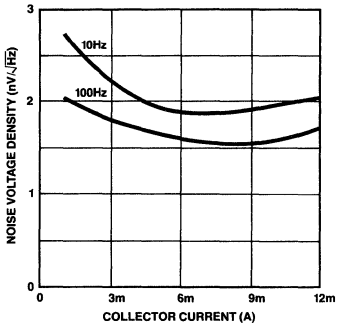
SATURATION VOLTAGE vs COLLECTOR CURRENT



NOISE VOLTAGE DENSITY vs FREQUENCY



NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



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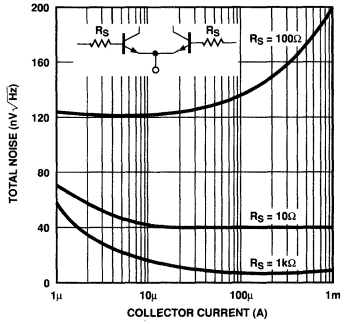
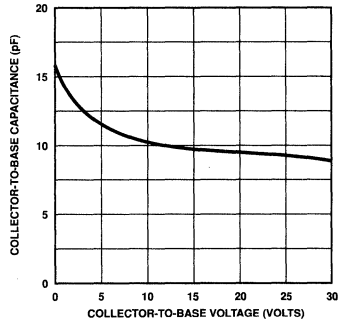
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

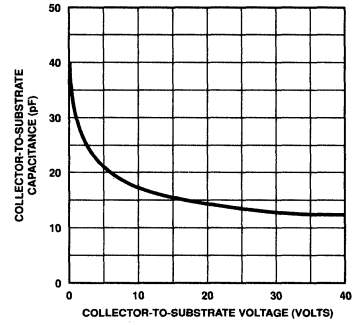
TOTAL NOISE vs COLLECTOR CURRENT



COLLECTOR-TO-BASE CAPACITANCE vs COLLECTOR-TO-BASE VOLTAGE



COLLECTOR-TO-SUBSTRATE CAPACITANCE vs COLLECTOR-TO- SUBSTRATE VOLTAGE



APPLICATION NOTES

It is recommended that one of the substrate pins (Pins 4 and 11) be tied to the most negative circuit potential to minimize coupling between devices. Pins 4 and 11 are internally connected.

APPLICATIONS

CURRENT SOURCES

The MAT-04 can be used to implement a variety of high impedance current mirrors as shown in Figures 1, 2, and 3. These current mirrors can be used as biasing elements and load devices for amplifier stages.

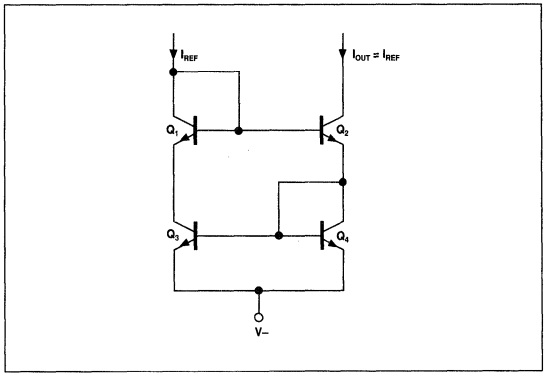


FIGURE 1: *Unity Gain Current Mirror, $I_{OUT} = I_{REF}$*

The unity-gain current mirror of Figure 1, using a MAT-04AY, has an accuracy of better than 1% and an output impedance of over 100MΩ at 100µA. Figures 2 and 3 show modified current mirrors designed for a current gain of two, and one-half respectively. The accuracy of these mirrors is reduced from that of the unity-gain source due to base current errors but is still better than 2%.

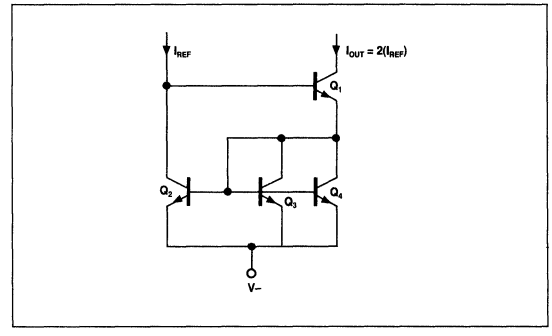


FIGURE 2: *Current Mirror, $I_{OUT} = 2(I_{REF})$*

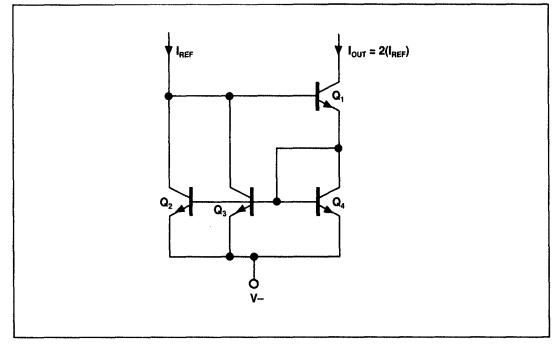
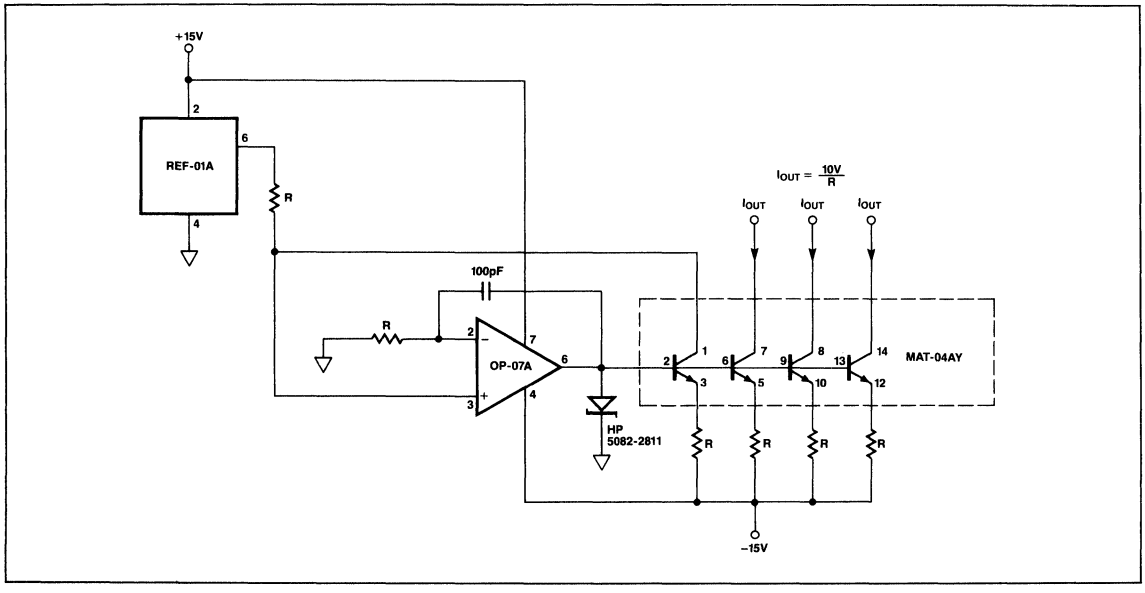


FIGURE 2: *Current Mirror, $I_{OUT} = 2(I_{REF})$*

Figure 4 is a temperature independent current sink that has an accuracy of better than 1% over the military temperature range at an output current of 100µA to 1 mA. The Schottky diode acts as a clamp to insure correct circuit start-up at power on. The resistors used in this circuit should be 1% metal-film type.

FIGURE 4: Temperature Independent Current Sink, $I_{OUT} = 10V/R\Omega$



NONLINEAR FUNCTIONS

An application where precision matched-transistors are a powerful tool is in the generation of nonlinear functions. These circuits are based on the transistor's logarithmic property which takes the following idealized form:

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C}{I_S}$$

The MAT-04, with its excellent logarithmic conformance, maintains this idealized function over many decades of collector current. This, in addition to the stringent parametric matching of the MAT-04, enables the implementation of extremely accurate log/antilog circuits.

The circuit of Figure 5 is a vector summer that adds and subtracts logged inputs to generate the following transfer function:

$$V_{OUT} = \frac{1}{\sqrt{2}} \sqrt{V_A^2 + V_B^2}$$

This circuit uses two MAT-04AYs and maintains an accuracy of better than 0.5% over an input range of 10mV to 10V. The layout of the MAT-04s reduces errors due to matching and temperature differences between the two precision quad matched-transistors.

Op amps A1 and A2 translate the input voltages into logarithmic valued currents (I_A and I_B in Figure 5) that flow through transistor Q_3 and Q_5. These currents are summed by transistor Q_4 ($I_O = I_A + I_B = \sqrt{I_1^2 + I_2^2}$) which feeds the current-to-voltage converter consisting of op amp A3. To maintain accuracy, 1% metal-film resistors should be used.

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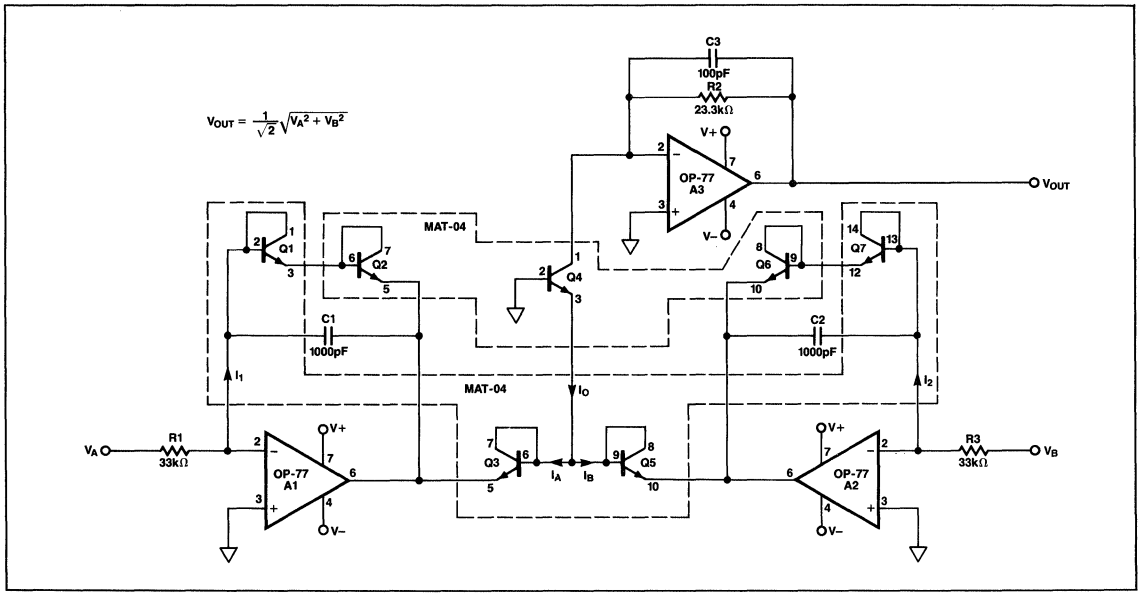
FIGURE 5: Vector Summer



LOW NOISE, HIGH SPEED INSTRUMENTATION AMPLIFIER

The circuit of Figure 6 is a very low noise, high speed amplifier, ideal for use in precision transducer and professional audio applications. The performance of the amplifier is summarized in Table I. Figure 7 shows the input referred spot noise over the 0-25kHz bandwidth to be flat at 1.2nV/ $\sqrt{Hz}$. Figure 8 highlights the low 1/f noise corner at 2Hz.

The circuit uses a high speed op amp, the OP-17, preceded by an input amplifier. This consists of a precision dual matched-transistor, the MAT-02, and a feedback V-to-I converter, the MAT-04. The arrangement of the MAT-04 is known as a "linearized cross quad" which performs the voltage-to-current conversion. The OP-17 acts as an overall nulling amplifier to complete the feedback loop. Resistors R1, R2, and R3, R4 form voltage dividers that attenuate the output voltage swing since the "cross quad" arrangement has a limited input range. Biasing for the input stage is set by zener diode Z1. At low currents the effective zener voltage is about 3.3V due to the soft knee characteristic of the zener diode. This results in a bias current of 530μA per side for the input stage. The gain of this amplifier with the values shown in Figure 6 is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{33000}{R_G}$$

TABLE I: Instrumentation Amplifier Characteristics

Input Noise Voltage Density	G = 1000	1.2nV/$\sqrt{Hz}$
	G = 100	3.6nV/$\sqrt{Hz}$
	G = 10	30nV/$\sqrt{Hz}$
Bandwidth	G = 500	400kHz
	G = 100	1MHz
	G = 10	1.2MHz
Slew Rate		40V/μs
Common-Mode Rejection	G = 1000	130dB
Distortion	G = 100 f = 20Hz to 20kHz	0.03%
Settling Time	G = 1000	10μs
Power Consumption		350mW

FIGURE 6: Low Noise, High Speed Instrumentation Amplifier

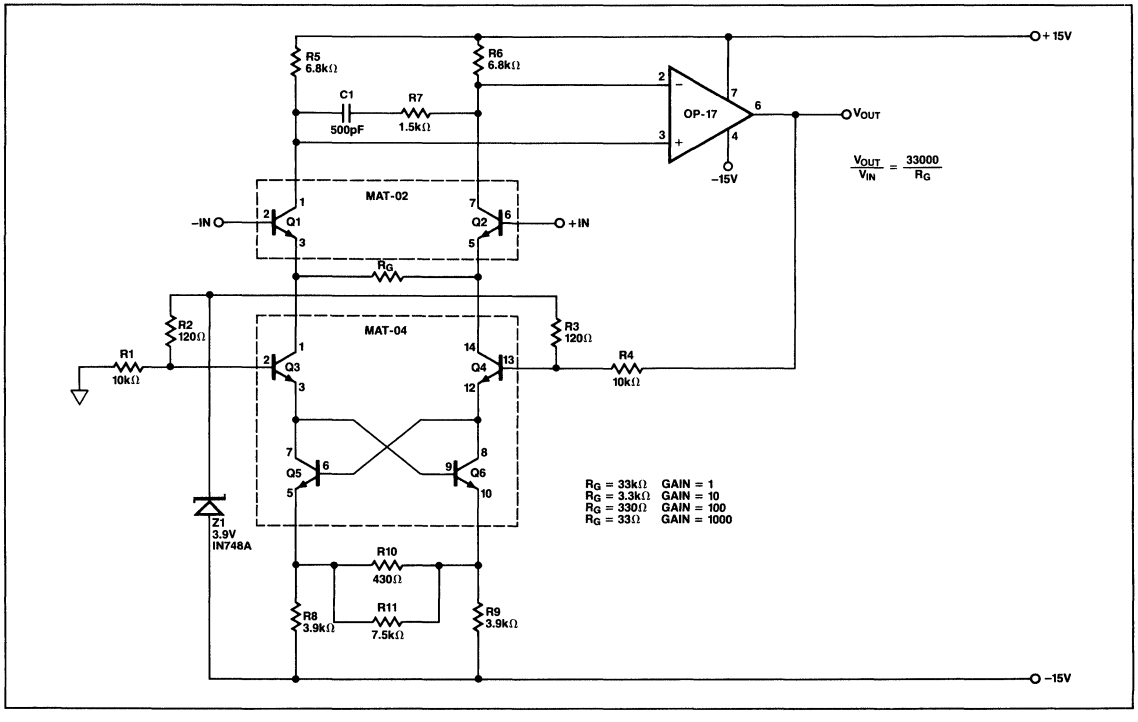


FIGURE 7: Spot Noise of the Instrumentation Amplifier from 0-25kHz at a Gain of 1000

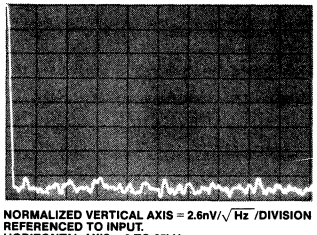


FIGURE 8: Low Frequency Noise Spectrum Showing Low 2Hz Noise Corner. Gain = 1000.

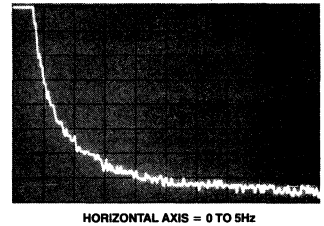


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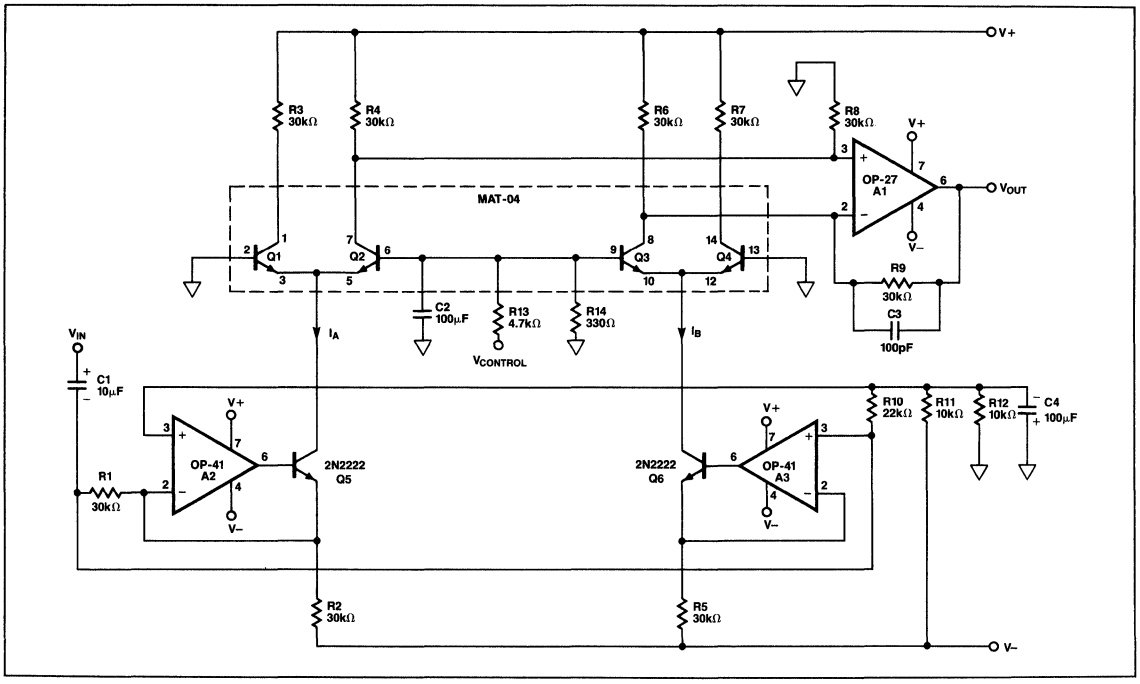
FIGURE 9: Voltage-Controlled Attenuator



VOLTAGE-CONTROLLED ATTENUATOR

The voltage-controlled attenuator (VCA) of Figure 9, widely used in professional audio circles, can easily be implemented using a MAT-04. The excellent matching characteristics of the MAT-04 enables the VCA to have a distortion level of under 0.03% over a wide range of control voltages. The VCA accepts a 3V RMS input and easily handles the full 20Hz-20kHz audio bandwidth as shown in Figure 10. Noise level for the VCA is more than 110dB below maximum output.

In the voltage-controlled attenuator, the input signal modulates the stage current of each differential pair. Op amps A2 and A3 in conjunction with transistors Q5 and Q6 form voltage-to-current converters that transform a single input voltage into differential currents which form the stage currents of each differential pair. The control voltage shifts the current between each side of the two differential pairs, regulating the signal level reaching the output stage which consists of op amp A1. Figure 11 shows the increase in signal attenuation as the control voltage becomes more negative.

The ideal transfer function for the voltage-controlled attenuator is:

$$V_{OUT}/V_{IN} = \frac{2}{1 + \exp\left((-V_{CONTROL})\left(\frac{R14}{R13 + R14}\right)\Big/\left(\frac{kT}{q}\right)\right)}$$

Where k = Boltzmann constant 1.38×10^{-23} J/°K
T = temperature in °K
q = electronic charge = 1.602×10^{-19}C

From the transfer function it can be seen that the maximum gain of the circuit is 2 (6dB).

To insure best performance, resistors R2 through R7 should be 1% metal film resistors. Since capacitor C2 can see small amounts of reverse bias when the control voltage is positive, it may be prudent to use a nonpolarized tantalum capacitor.

FIGURE 10: Voltage-Controlled Attenuator, Attenuation vs Frequency

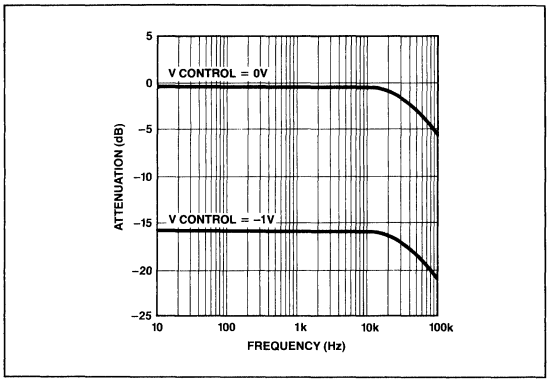
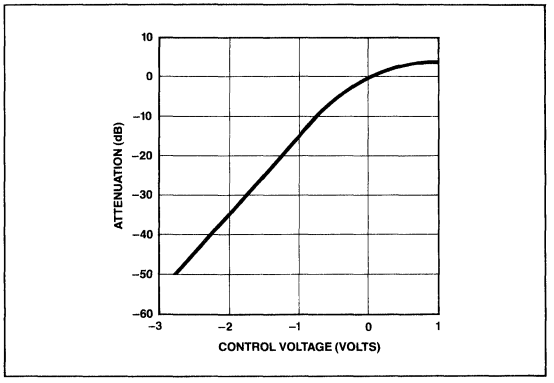


FIGURE 11: Voltage-Controlled Attenuator, Attenuation vs Control Voltage



8

Temperature Sensors
Contents

Selection Guide
Temperature Sensors

Model	I_{OUT} µA/K	V_{OUT} mV/K	Cal Error °C max	Nonlin °C max	Package Options[1]	Temp Range[2]	Page	Comments
AC2626	**1**	**—**	**0.5–5**	**0.3–1.5 Steel Sheath**	**3/16″ Stainless**	**C, M**	**9-5**	**General Purpose Temperature Probe 4″ and 6″ Length**
AD590	**1**	**—**	**0.5–5**	**0.3–1.5**	**7, 9**	**M+**	**9-7**	**Wide Temperature Range, Accurate**
AD592	**1**	**—**	**0.5–2.5**	**0.15–0.35**	**2**	**I+**	**9-17**	**Low Cost, Accurate**
***TMP-01**	**—**	**5**	**1.2–6**	**0.4–1.0**	**2, 3, 6, 7, 11**	**I, M+**	**9-25**	**Complete Programmable Temperature Controller**

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product.

Orientation
Temperature Sensors

Integrated circuit temperature transducers offer a number of advantages over other temperature measurement technologies such as RTDs and thermistors. They offer linear output temperature coefficients, eliminating the need for linearization circuitry. The output signal levels are generally larger than other types of sensor outputs and are more immune to noise and interference. Integrated circuit sensors are available in a variety of temperature ranges, output formats, and temperature coefficients.

Integrated circuit temperature transducers will find applications in cold junction compensation of thermocouples, appliance temperature sensing, automotive temperature measurement and control, HVAC (heating, ventilating and air conditioning) system monitoring, industrial temperature control, board-level electronic temperature diagnostics, temperature readout options in instrumentation, and temperature-correction circuitry for precision electronics.

Current Output Temperature Transducers
The devices in this section are two-terminal monolithic integrated circuits designed to measure temperatures within the range −55°C to +150°C. When +4 V to +30 V of excitation voltage is applied, they act as current sources that provide an output proportional to absolute temperature, 1 μA/K. Expressed in degrees Celsius (T_C),

$$I = 1\ \mu A/^{\circ}C \cdot T_C = 273.2\ \mu A$$

Current Temperature transducers have a number of advantages:

- They are based on a linear relationship and are highly repeatable.
- The current is independent of voltage drops, voltage noise common-mode voltage, and practically independent of excitation voltage.
- The current can be translated to a voltage at a remote destination via an appropriate value of resistance (V = IR); simple offsetting circuitry may be used when necessary.
- They are easy to use; they don't require linearization circuitry, high precision voltage amplifiers, resistance-measuring circuitry or cold-junction compensation.

Indeed, they are themselves widely used for cold-junction compensation of thermocouple circuitry.

Voltage Output Temperature Transducers
When voltage drops and noise are not an important consideration in design, it may be more convenient to work with a voltage output temperature transducer. These provide a direct output to an analog-to-digital converter or a comparator setpoint. The following products provide a voltage output while performing other functions as well.

AD22100 Ratiometric Voltage Output Temperature Sensor
The AD22100 is a monolithic temperature sensor with on-chip signal conditioning that operates over the range of −50°C to +150°C. The output voltage is proportional to the temperature times the supply current. This unique feature allows the AD22100 supply voltage to act as a voltage reference for an analog-to-digital converter, eliminating the need for a separate voltage reference. The part has a 22.5 mV/°C temperature coefficient when operated with a 5 V supply. It will be available in a TO-5 can, TO-92 or 4-pin SIP. See the section on Automotive Components for a preliminary data sheet.

AD680 Voltage Reference and REF-02 +5 V Voltage Reference
These voltage references have an extra pin that outputs a voltage proportional to absolute temperature. They are convenient to use when both a temperature sensor and a voltage reference are required. See the section on Voltage Reference in Volume II of the *Data Converter Reference Manual*.

Setpoint Controllers
TMP-01 Low Power Programmable Temperature Controller
The TMP-01 is a complete, easy-to-use programmable thermostat in a single 8-pin package. In addition to a highly linear sensor with a buffered output calibrated to 5 mV/K, it features over- and under-temperature comparators. The user can program these temperature comparators by dividing a stable 2.5 V reference voltage output with external potentiometers, or by simply applying the appropriate voltage source. The open-collector outputs of the comparators are capable of driving TTL/CMOS logic, cables, and small relays directly. Setpoint hysteresis is also programmable. Operating over wide temperature (−55°C to +150°C) and supply (4.5 V to 25 V) ranges, it is offered in two grades which are calibrated to 2°C or 4°C accuracy over the specified temperature ranges (with no external adjustments required). In addition to the low cost 8-pin mini-DIP and surface mount SOL packages, the TMP-01 is available in the ceramic DIP, TO-99 metal can, and in die form.

RELATED PRODUCTS
The AD594, AD595, AD596 and AD597 are monolithic thermocouple amplifiers with built in cold junction compensation. These can be used with thermocouples to get a precalibrated output of 10 mV/°C, or can be configured as a setpoint controller. They can also be connected as a voltage or current output temperature sensor. See the section on Signal Conditioning Components in this reference manual.

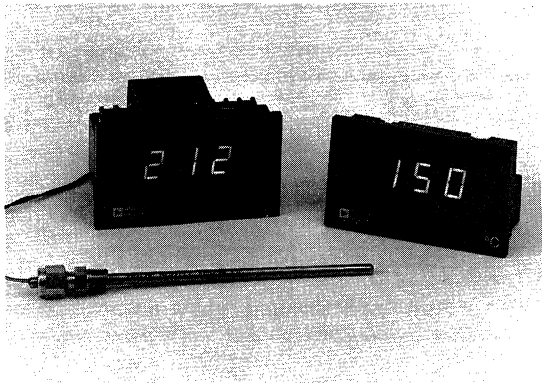
Analog Devices's wide offering of complete Signal Conditioners (found in this volume) provide many creative options for interfacing a wide variety of transducers to their respective measurement systems. Also, Analog Devices offers a diverse range of operational amplifiers, instrumentation amplifiers, and isolation amplifiers to meet all of your signal conditioning needs. For the optimal choice, consult Volume I of this set, the *Amplifier Reference Manual*. For background information, the *Transducer Interfacing Handbook*, published by Analog Devices (1980), provides valuable insight in understanding, designing, and applying transducers in physical systems. It is available for $14.50 (hardcover) from P.O. Box 9106, Norwood, MA 02062-9106.

General Purpose Temperature Probe

AC2626

FEATURES

Linear Current Output: 1μA/K
Wide Range: -55°C to +150°C
Laser Trimmed Sensor (AD590) to ±1.0°C Calibration Accuracy (AC2626L)
Excellent Linearity: ±0.4°C Over Full Range (AC2626L)
6 Inch or 4 Inch Standard, Stainless Steel Sheath
3/16 Inch in Outside Diameter
3 Feet Teflon Coated Lead Wire
Wide Power Supply Range +4V to +30V
Low Cost
Fast Response: 2 Seconds (In Stirred Water)
Sensor Isolated From Sheath



PRODUCT DESCRIPTION

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4-inch (101.6mm) lengths. The probe is available in linearity grades of 0.3°C, 0.4°C, 0.8°C or 1.5°C.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AC2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.

PRODUCT HIGHLIGHTS

The AC2626 is based on the AD590 temperature transducer, a two terminal integrated circuit which produces an output current linearly proportional to absolute temperature.

Costly linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AC2626.

Due to the high impedance current output of the AD590, the AC2626 is particularly useful in remote sensing applications, because of its insensitivity to voltage drops over lines. The output characteristics also make the AC2626 easy to multiplex.

In addition to temperature measurement, applications include temperature compensation, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry.

DIRECT INTERFACE PRODUCTS

For display and/or control applications, two companion products are available. The AD2038, 6 channel digital thermometer, and the AD2040, low cost temperature indicator, were designed to be used in conjunction with the AC2626.

1. The AD2038 is a low cost, ac line powered 6 channel digital scanning thermometer designed to interface to printers, computers, serial data transmitters, etc., for display, control, logging or transmission of multi-point temperature data. Channel selection is made via three methods: manual, using the switch provided on the front; auto/scan, where the AD2038 cycling on an internal clock can continually scan the six input channels or external selection, where control inputs provided on the rear connector enable channel selection via external BCD coding.
2. The AD2040 is a low cost, 3 digit temperature indicator. An internal precision voltage reference, resistor network and span and zero adjusts allow the AD2040 to read out directly in °C, °F, K or R. User selectable readout as well as all other connections, i.e., +5V dc power and AC2626 interface are all made via the terminal block on the rear.

APPLICATION HINTS

1. Under all operating conditions, a minimum 4V dc must be present across the AC2626.
2. Use of twisted pair wiring is recommended, particularly for remote applications or in high noise environments. Shielded wire is desirable in severe noise environments.
3. For the lowest cost, the J and K grades are recommended. Where probe interchangeability is desired, grade L is recommended.

AC2626—SPECIFICATIONS (typical @ +25°C and +5V unless otherwise specified)

MODEL	AC2626J	AC2626K	AC2626L	AC2626M
ABSOLUTE MAXIMUM RATINGS[1]				
Forward Voltage (V_S)	+44V	*	*	*
Reverse Voltage (V_S)	-20V	*	*	*
Breakdown Voltage (Case to Leads)	±200V	*	*	*
Rated Performance Temp. Range	-55°C to +150°C	*	*	*
Storage Temperature Range	-60°C to +160°C	*	*	*
POWER SUPPLY				
Operating Voltage Range	+4V to +30V	*	*	*
OUTPUT				
Nominal Current Output @ +25°C (298.2°K)	298.2μA	*	*	*
Nominal Temperature Coefficient	1μA/°C	*	*	*
Calibration Error @ +25°C	±5.0°C max	±2.5°C max	±1.0°C max	±0.5°C max
Absolute Error (over rated performance temperature range)				
Without External Calibration Adjustment	±10.0°C max	±5.5°C max	±3.0°C max	±1.7°C max
With +25°C Calibration Error Set to Zero	±3.0°C max	±2.0°C max	±1.6°C max	±1.0°C max
Nonlinearity	±1.5°C max	±0.8°C max	±0.4°C max	±0.3°C max
Repeatability[2]	0.1°C	*	*	*
Long Term Drift[3]	0.1°C max/month	*	*	*
Time Constant[4] (in stirred water)	2 sec.	*	*	*
Current Noise	40pA$\sqrt{Hz}$	*	*	*
Power Supply Rejection				
+4V≤V_S≤+5V	0.5μA/V	*	*	*
+5V≤V_S≤+15V	0.2μA/V	*	*	*
+15V≤V_S≤+30V	0.1μA/V	*	*	*
Electrical Turn-On Time	20μs	*	*	*
+ Lead Color	yellow	orange	blue	green

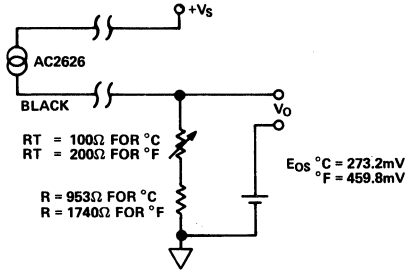
ORDERING GUIDE

AC2626
- GRADE: J, K, L — ENTER
- LENGTH: 4, 6 — ENTER

AC2629
- BRASS: B
- TYPE 316 STAINLESS: SS — ENTER

NOTES
[1] Maximum safe recommended pressure: 7500psi (5.17 X 10^4 Kpa).
[2] Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C; guaranteed, not tested.
[3] Conditions: constant +5V, constant +125°C; guaranteed, not tested.
[4] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.
*Specifications same as AC2626J.
Specifications subject to change without notice.

CALIBRATION



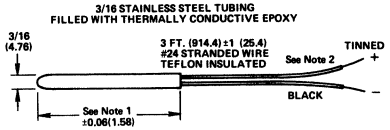
For most applications, a single point calibration is sufficient. With the probe at a known temperature, adjust R_T so that V_O corresponds to the known temperature.

If more detailed information is desired, see the AD590 data sheet and application note.

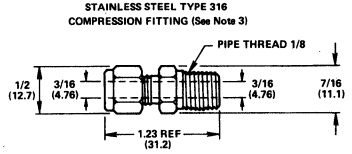
MECHANICAL OUTLINE

Dimensions shown in inches and (mm).

AC2626



AC2629



NOTE 1 Probes are available in 4-inch or 6-inch lengths.
NOTE 2 + lead wire is color coded: J, yellow; K, orange; L, blue.
NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight.

ANALOG DEVICES

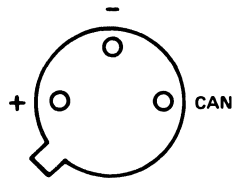
Two-Terminal IC Temperature Transducer

AD590*

FEATURES

Linear Current Output: 1μA/K
Wide Range: -55°C to +150°C
Probe Compatible Ceramic Sensor Package
Two-Terminal Device: Voltage In/Current Out
Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
Excellent Linearity: ±0.3°C Over Full Range (AD590M)
Wide Power Supply Range: +4V to +30V
Sensor Isolation from Case
Low Cost

PIN DESIGNATIONS



BOTTOM VIEW

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

***Covered by Patent No. 4,123,698.**

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.

AD590—SPECIFICATIONS (@ +25°C and V_S = +5V unless otherwise noted)

Model	AD590J			AD590K			
	Min	Typ	Max	Min	Typ	Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			**±5.0**			**±2.5**	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			**±10**			**±5.5**	°C
With +25°C Calibration Error Set to Zero			**±3.0**			**±2.0**	°C
Nonlinearity			**±1.5**			**±0.8**	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA/$\sqrt{Hz}$
Power Supply Rejection							
$+4V \leq V_S \leq +5V$		0.5			0.5		μA/V
$+5V \leq V_S \leq +15V$		0.2			0.2		μA/V
$+15V \leq V_S \leq +30V$		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4]							
(Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTIONS[5]							
TO-52 (H-03A)		AD590JH			AD590KH		
Flat Pack (F-2A)		AD590JF			AD590KF		

NOTES

[1]The AD590 has been used at −100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2]Maximum deviation between +25°C readings after temperature cycling between −55°C and +150°C; guaranteed not tested.

[3]Conditions: constant +5V, constant +125°C; guaranteed, not tested.

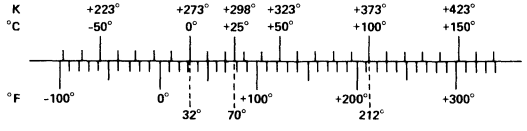
[4]Leakage current doubles every 10°C.

[5]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Model	AD590L Min	AD590L Typ	AD590L Max	AD590M Min	AD590M Typ	AD590M Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			**±1.0**			**±0.5**	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			**±3.0**			**±1.7**	°C
With +25°C Calibration Error Set to Zero			**±1.6**			**±1.0**	°C
Nonlinearity			**±0.4**			**±0.3**	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA$\sqrt{\text{Hz}}$
Power Supply Rejection							
+4V≤V_S≤+5V		0.5			0.5		μA/V
+5V≤V_S≤+15V		0.2			0.2		μA/V
+15V≤V_S≤+30V		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTION[5]							
TO-52 (H-03A)		AD590LH			AD590MH		
Flat Pack (F-2A)		AD590LF			AD590MF		



TEMPERATURE SCALE CONVERSION EQUATIONS

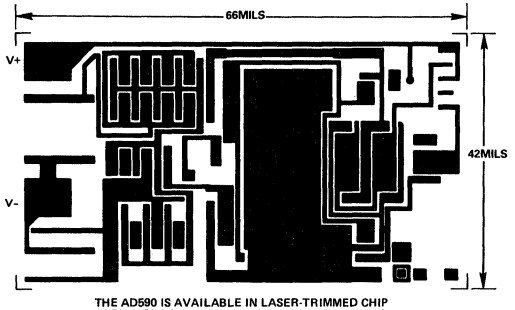
$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

The 590H has 60μ inches of gold plating on its Kovar leads and Kovar header. A resistance welder is used to seal the nickel cap to the header. The AD590 chip is eutectically mounted to the header and ultrasonically bonded to with 1 MIL aluminum wire. Kovar composition: 53% iron nominal; 29% ±1% nickel; 17% ±1% cobalt; 0.65% manganese max; 0.20% silicon max; 0.10% aluminum max; 0.10% magnesium max; 0.10% zirconium max; 0.10% titanium max; 0.06% carbon max.

The 590F is a ceramic package with gold plating on its Kovar leads, Kovar lid, and chip cavity. Solder of 80/20 Au/Sn composition is used for the 1.5 mil thick solder ring under the lid. The chip cavity has a nickel underlay between the metalization and the gold plating. The AD590 chip is eutectically mounted in the chip cavity at 410°C and ultrasonically bonded to with 1 mil aluminum wire. Note that the chip is in direct contact with the ceramic base, not the metal lid. When using the AD590 in die form, the chip substrate must be kept electrically isolated, (floating), for correct circuit operation.

METALIZATION DIAGRAM



THE AD590 IS AVAILABLE IN LASER-TRIMMED CHIP FORM; CONSULT THE CHIP CATALOG FOR DETAILS.

CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(In r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly porportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

Figure 2 shows the typical V–I characteristic of the circuit at +25°C and the temperature extremes.

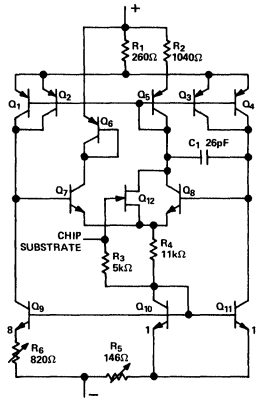


Figure 1. Schematic Diagram

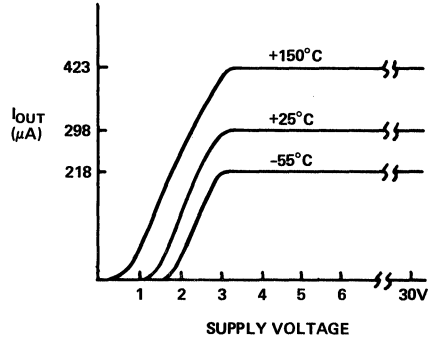


Figure 2. V–I Plot

[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)[1] current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to 1μA/K at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of 25°C (298.2K). The device is then packaged and tested for accuracy over temperature.

CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the 1°C specified maximum error of the AD590L varies from 0.73°C at -55°C to 1.42°C at 150°C. Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

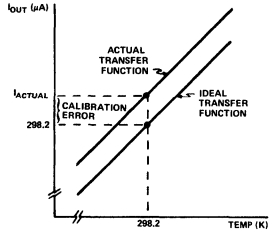


Figure 3. Calibration Error vs. Temperature

The calibration error is a primary contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that V_T = 1mV/K at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

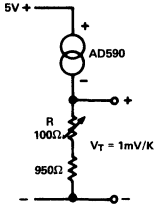


Figure 4. One Temperature Trim

[1] T(°C) = T(K) -273.2; Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at 25°C. This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

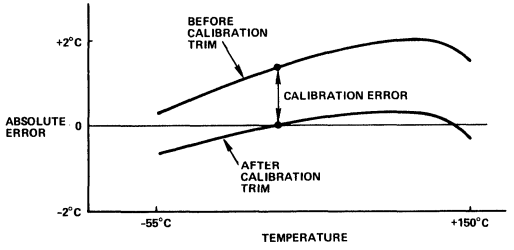


Figure 5. Effect of Scale Factor Trim on Accuracy

ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from 2.33°C at -55°C to 3.02°C at 150°C. For simplicity, only the larger figure is shown on the specification page.

NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the -55°C to +150°C range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

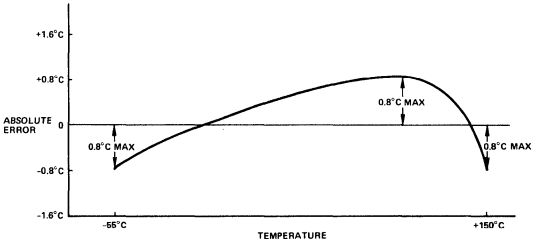


Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with the AD590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ of the op amp must be greater than 17V. Also note that V- should be at least -4V: if V- is ground there is no voltage applied across the device.

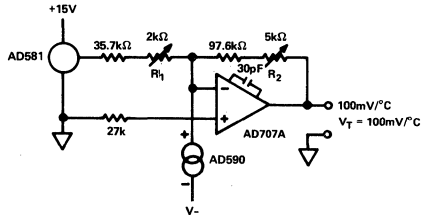


Figure 7A. Two Temperature Trim

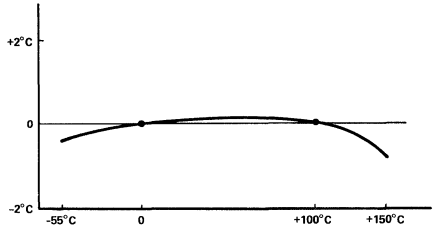


Figure 7B. Typical Two-Trim Accuracy

VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection specifications show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. In other words, this change is equivalent to a calibration error and can be removed by the scale factor trim (see previous page).

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Large changes in the thermal resistance of the sensor's environment will change the amount of self-heating and result in changes in the output which are predictable but not necessarily desirable.

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

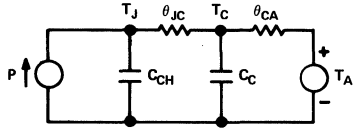


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. As an example, for the TO-52 package, θ_{JC} is the thermal resistance between the chip and the case, about 26°C/watt. θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source P represents the power dissipated on the chip. The rise of the junction temperature, T_J, above the ambient temperature T_A is:

$$T_J - T_A = P(\theta_{JC} + \theta_{CA}). \qquad \text{Eq. 1}$$

Table I gives the sum of θ_{JC} and θ_{CA} for several common thermal media for both the "H" and "F" packages. The heatsink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 "H" package in a stirred bath at +25°C, when driven with a 5V supply, will be 0.06°C. However, for the same conditions in still air the temperature rise is 0.72°C. For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

MEDIUM	$\theta_{JC} + \theta_{CA}$ (°C/watt)		τ (sec) (Note 3)	
	H	F	H	F
Aluminum Block	30	10	0.6	0.1
Stirred Oil[1]	42	60	1.4	0.6
Moving Air[2]				
With Heat Sink	45	—	5.0	—
Without Heat Sink	115	190	13.5	10.0
Still Air				
With Heat Sink	191	—	108	—
Without Heat Sink	480	650	60	30

[1] Note: τ is dependent upon velocity of oil; average of several velocities listed above.

[2] Air velocity ≅ 9ft/sec.

[3] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Table I. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip, C_{CH}, and the case, C_C. C_{CH} is about 0.04 watt-sec/°C for the AD590. C_C varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response, T(t). Table I shows the effective time constant, τ, for several media.

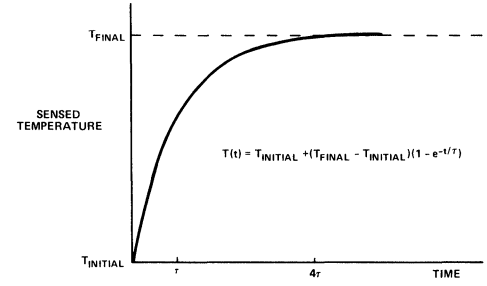


Figure 9. Time Response Curve

GENERAL APPLICATIONS

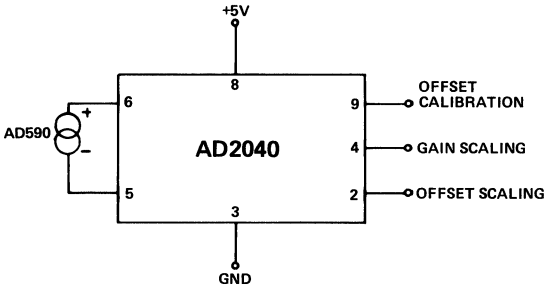


Figure 10. Variable Scale Display

Figure 10 demonstrates the use of a low-cost Digital Panel Meter for the display of temperature on either the Kelvin, Celsius or Fahrenheit scales. For Kelvin temperature Pins 9, 4 and 2 are grounded; and for Fahrenheit temperature Pins 4 and 2 are left open.

The above configuration yields a 3 digit display with 1°C or 1°F resolution, in addition to an absolute accuracy of ±2.0°C over the -55°C to +125°C temperature range if a one-temperature calibration is performed on an AD590K, L, or M.

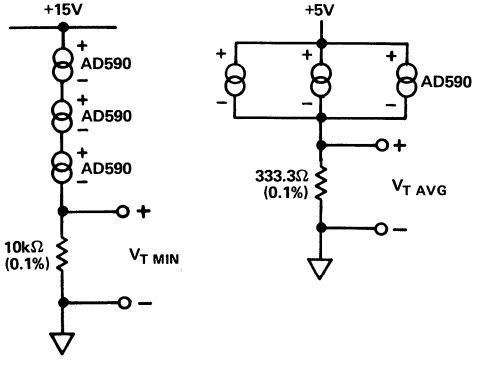


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made. R_1 and R_2 can be used to trim the output of the op amp to indicate

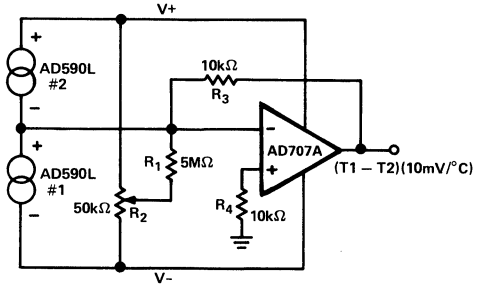


Figure 12. Differential Measurements

a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If V+ and V- are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

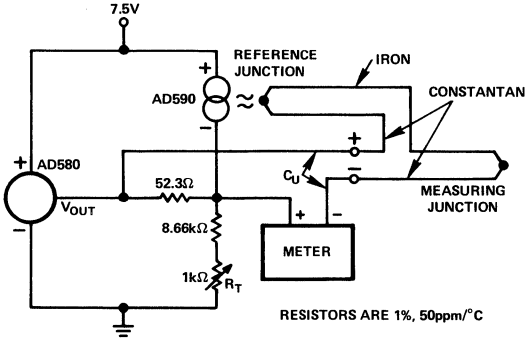


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between +15°C and +35°C. The circuit is calibrated by adjusting R_T for a proper meter reading with the measuring junction at a known reference temperature and the circuit near +25°C. Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within ±0.5°C for circuit temperatures between +15°C and +35°C. Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

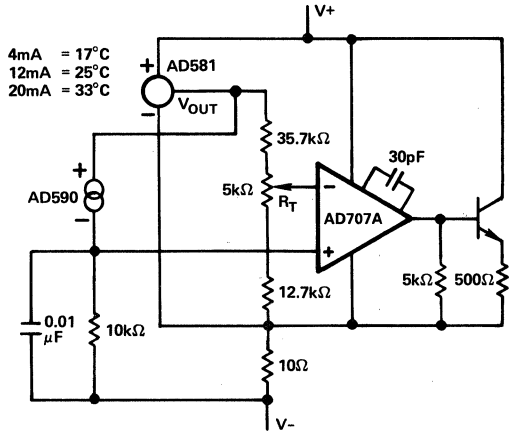


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1μA/K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. R_T is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

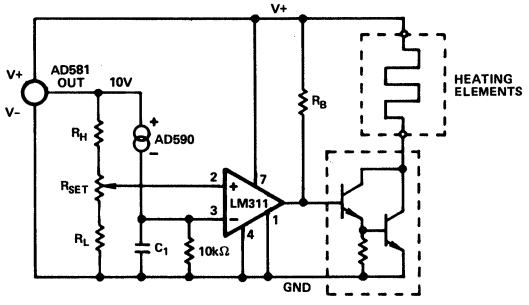


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590. R_H and R_L are selected to set the high and low limits for R_{SET}. R_{SET} could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor C_1 is often needed to filter extraneous noise from remote sensors. R_B is determined by the β of the power transistor and the current requirements of the load.

Figure 16 shows how the AD590 can be configured with an 8-bit DAC to produce a digitally controlled set point. This

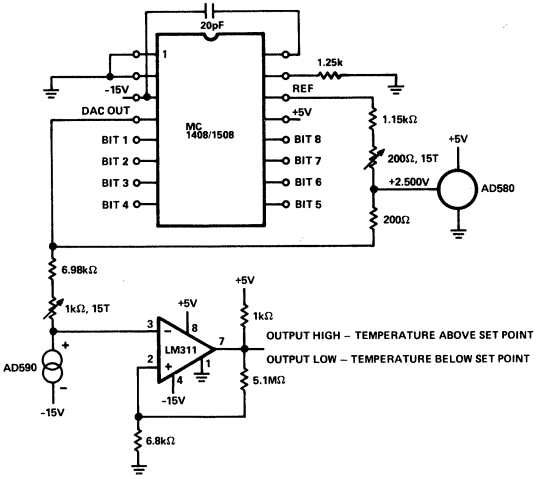


Figure 16. DAC Set Point

particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

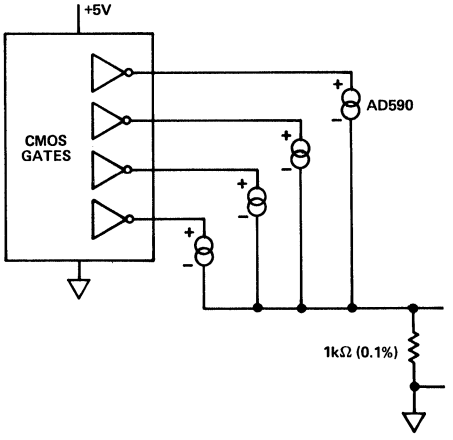


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.

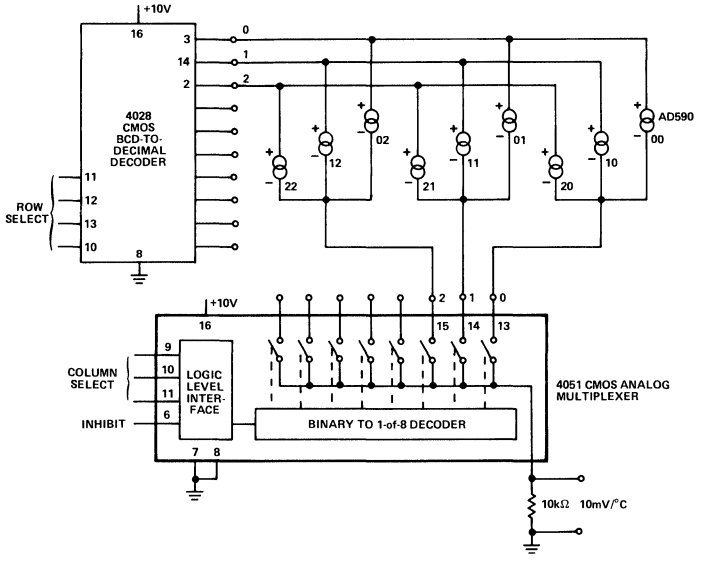


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

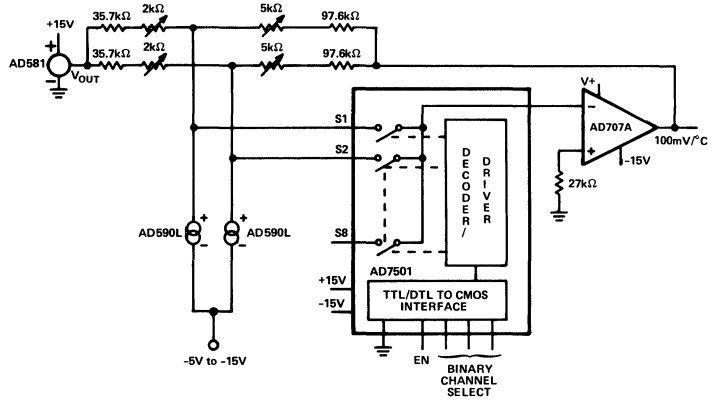


Figure 19. 8-Channel Multiplexer

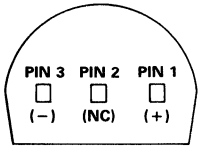
Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of ±0.5°C absolute accuracy over the temperature range of -55°C to +125°C. The high temperature restriction of +125°C is due to the output range of the op amps; output to +150°C can be achieved by using a +20V supply for the op amp.

Low Cost, Precision IC Temperature Transducer

AD592*

FEATURES
High Precalibrated Accuracy: 0.5°C max @ 25°C
Excellent Linearity: 0.15°C max (0 to +70°C)
Wide Operating Temperature Range: −25°C to +105°C
Single Supply Operation: +4V to +30V
Excellent Repeatability and Stability
High Level Output: 1μA/K
Two Terminal Monolithic IC: Temperature In/ Current Out
Minimal Self-Heating Errors

CONNECTION DIAGRAM



*PIN 2 CAN BE EITHER ATTACHED OR UNCONNECTED

BOTTOM VIEW

PRODUCT DESCRIPTION

The AD592 is a two terminal monolithic integrated circuit temperature transducer that provides an output current proportional to absolute temperature. For a wide range of supply voltages the transducer acts as a high impedance temperature dependent current source of 1μA/K. Improved design and laser wafer trimming of the IC's thin film resistors allows the AD592 to achieve absolute accuracy levels and nonlinearity errors previously unattainable at a comparable price.

The AD592 can be employed in applications between −25°C and +105°C where conventional temperature sensors (i.e., thermistor, RTD, thermocouple, diode) are currently being used. The inherent low cost of a monolithic integrated circuit in a plastic package, combined with a low total parts count in any given application, make the AD592 the most cost effective temperature transducer currently available. Expensive linearization circuitry, precision voltage references, bridge components, resistance measuring circuitry and cold junction compensation are not required with the AD592.

Typical application areas include; appliance temperature sensing, automotive temperature measurement and control, HVAC (heating/ventilating/air conditioning) system monitoring, industrial temperature control, thermocouple cold junction compensation, board-level electronics temperature diagnostics, temperature readout options in instrumentation, and temperature correction circuitry for precision electronics. Particularly useful in remote sensing applications, the AD592 is immune to voltage drops and voltage noise over long lines due to its high impedance current output. AD592s can easily be multiplexed; the signal current can be switched by a CMOS multiplexer or the supply voltage can be enabled with a tri-state logic gate.

The AD592 is available in three performance grades; the AD592AN, AD592BN and AD592CN. All devices are packaged in a plastic TO-92 case rated from −45°C to +125°C. Performance is specified from −25°C to +105°C. AD592 chips are also available, contact the factory for details.

PRODUCT HIGHLIGHTS

1. With a single supply (4V to 30V) the AD592 offers 0.5°C temperature measurement accuracy.
2. A wide operating temperature range (−25°C to +105°C) and highly linear output make the AD592 an ideal substitute for older, more limited sensor technologies (i.e., thermistors, RTDs, diodes, thermocouples).
3. The AD592 is electrically rugged; supply irregularities and variations or reverse voltages up to 20V will not damage the device.
4. Because the AD592 is a temperature dependent current source, it is immune to voltage noise pickup and IR drops in the signal leads when used remotely.
5. The high output impedance of the AD592 provides greater than 0.5°C/V rejection of supply voltage drift and ripple.
6. Laser wafer trimming and temperature testing insures that AD592 units are easily interchangeable.
7. Initial system accuracy will not degrade significantly over time. The AD592 has proven long term performance and repeatability advantages inherent in integrated circuit design and construction.

9

***Protected by Patent No. 4,123,698.**

AD592—SPECIFICATIONS (typical @ +25°C, V_S = +5V unless otherwise noted)

Model	AD592AN Min	AD592AN Typ	AD592AN Max	AD592BN Min	AD592BN Typ	AD592BN Max	AD592CN Min	AD592CN Typ	AD592CN Max	Units
ACCURACY										
Calibration Error @25°C[1]		1.5	**2.5**		0.7	**1.0**		0.3	**0.5**	°C
T_A = 0 to +70°C										
Error over Temperature		1.8	3.0		0.8	1.5		0.4	0.8	°C
Nonlinearity[2]		0.15	0.35		0.1	0.25		0.05	0.15	°C
T_A = −25 to +105°C										
Error over Temperature[3]		2.0	**3.5**		0.9	**2.0**		0.5	**1.0**	°C
Nonlinearity[2]		0.25	0.5		0.2	0.4		0.1	0.35	°C
OUTPUT CHARACTERISTICS										
Nominal Current Output @25°C (298.2K)		298.2			298.2			298.2		µA
Temperature Coefficient		1			1			1		µA/°C
Repeatability[4]			0.1			0.1			0.1	°C
Long Term Stability[5]			0.1			0.1			0.1	°C/month
ABSOLUTE MAXIMUM RATINGS										
Operating Temperature	−25		+105	−25		+105	−25		+105	°C
Package Temperature[6]	−45		+125	−45		+125	−45		+125	°C
Forward Voltage (+ to −)			**44**			**44**			**44**	V
Reverse Voltage (− to +)			**20**			**20**			**20**	V
Lead Temperature (Soldering 10 sec)			300			300			300	°C
POWER SUPPLY										
Operating Voltage Range	4		30	4		30	4		30	V
Power Supply Rejection										
+4V<V_S<+5V			**0.5**			**0.5**			**0.5**	°C/V
+5V<V_S<+15V			**0.2**			**0.2**			**0.2**	°C/V
+15V<V_S<+30V			**0.1**			**0.1**			**0.1**	°C/V

NOTES

[1]An external calibration trim can be used to zero the error @25°C.

[2]Defined as the maximum deviation from a mathematically best fit line.

[3]Parameter tested on all production units at +105°C only. C grade at −25°C also.

[4]Maximum deviation between +25°C readings after a temperature cycle between −45°C and +125°C. Errors of this type are noncummulative.

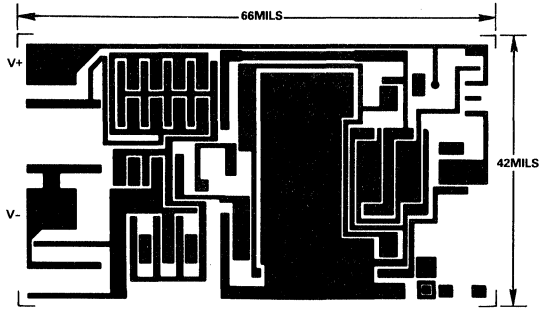
[5]Operation @125°C, error over time is noncummulative.

[6]Although performance is not specified beyond the operating temperature range, temperature excursions within the package temperature range will not damage the device.

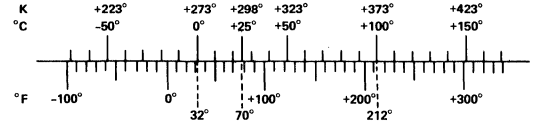
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

METALIZATION DIAGRAM



THE AD592 IS AVAILABLE IN LASER-TRIMMED CHIP FORM.



TEMPERATURE SCALE CONVERSION EQUATIONS

$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

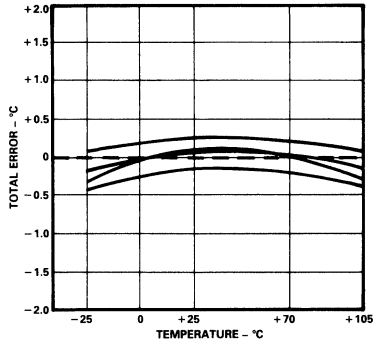
$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

ORDERING GUIDE

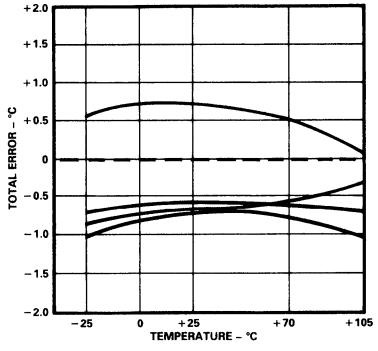
Model	Max Cal Error @ 25°C	Max Error −25°C to +105°C	Max Nonlinearity −25°C to +105°C	Package Option*
AD592CN	0.5°C	1.0°C	0.35°C	TO-92
AD592BN	1.0°C	2.0°C	0.4°C	TO-92
AD592AN	2.5°C	3.5°C	0.5°C	TO-92

For outline information see Package Information section.

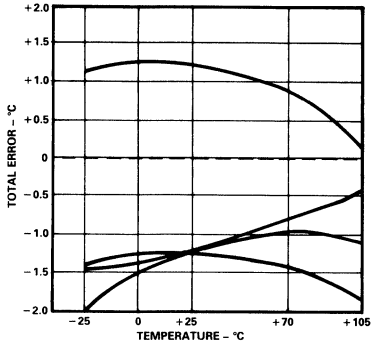
Typical @ V_S = +5V



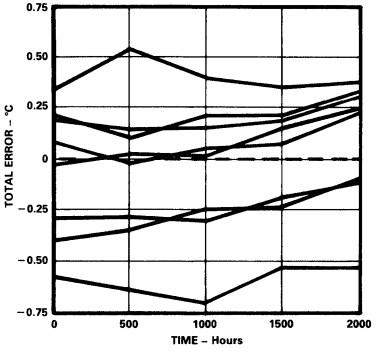
AD592CN Accuracy Over Temperature



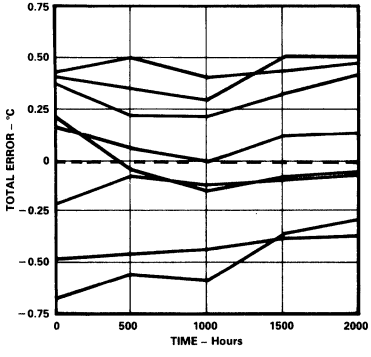
AD592BN Accuracy Over Temperature



AD592AN Accuracy Over Temperature



Long-Term Stability @ 85°C and 85% Relative Humidity



Long-Term Stability @ 125°C

THEORY OF OPERATION

The AD592 uses a fundamental property of silicon transistors to realize its temperature proportional output. If two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in base-emitter voltages will be (kT/q)(ln r). Since both k, Boltzman's constant and q, the charge of an electron are constant, the resulting voltage is directly Proportional To Absolute Temperature (PTAT). In the AD592 this difference voltage is converted to a PTAT current by low temperature coefficient thin film resistors. This PTAT current is then used to force the total output current to be proportional to degrees Kelvin. The result is a current source with an output equal to a scale factor times the temperature (K) of the sensor. A typical V-I plot of the circuit at +25°C and the temperature extremes is shown in Figure 1.

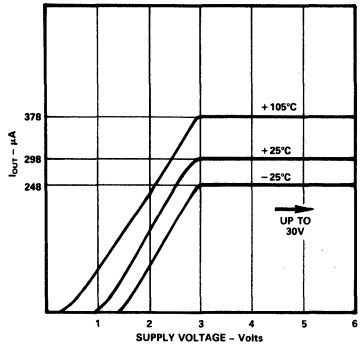


Figure 1. V–I Characteristics

Factory trimming of the scale factor to 1μA/K is accomplished at the wafer level by adjusting the AD592's temperature reading so it corresponds to the actual temperature. During laser trimming the IC is at a temperature within a few degrees of 25°C and is powered by a 5V supply. The device is then packaged and automatically temperature tested to specification.

FACTORS AFFECTING AD592 SYSTEM PRECISION

The accuracy limits given on the Specifications page for the AD592 makes it easy to apply in a variety of diverse applications. To calculate a total error budget in a given system it is important to correctly interpret the accuracy specifications, nonlinearity errors, the response of the circuit to supply voltage variations and the effect of the surrounding thermal environment. As with other electronic designs external component selection will have a major effect on accuracy.

CALIBRATION ERROR, ABSOLUTE ACCURACY AND NONLINEARITY SPECIFICATIONS

Three primary limits of error are given for the AD592 such that the correct grade for any given application can easily be chosen for the overall level of accuracy required. They are the calibration accuracy at 25°C, and the error over temperature from 0 to 70°C and −25°C to +105°C. These specifications correspond to the actual error the user would see if the current output of a AD592 were converted to a voltage with a precision resistor. Note that the maximum error at room temperature, over the commercial IC temperature range, or an extended range including the boiling point of water, can be directly read from the Specifications Table. All three error limits are a combination of initial error, scale factor variation and nonlinearity deviation from the ideal 1μA/K output. Figure 2 graphically depicts the guaranteed limits of accuracy for an AD592CN.

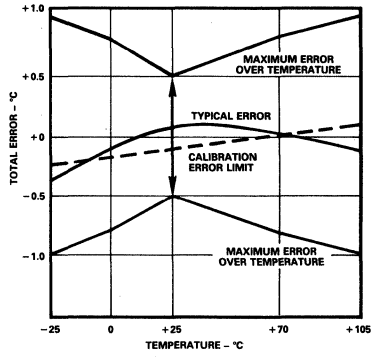


Figure 2. Error Specifications (AD592CN)

The AD592 has a highly linear output in comparison to older technology sensors (i.e., thermistors, RTDs and thermocouples), thus a nonlinearity error specification is separated from the absolute accuracy given over temperature. As a maximum deviation from a best-fit straight line this specification represents the only error which cannot be trimmed out. Figure 3 is a plot of typical AD592CN nonlinearity over the full rated temperature range.

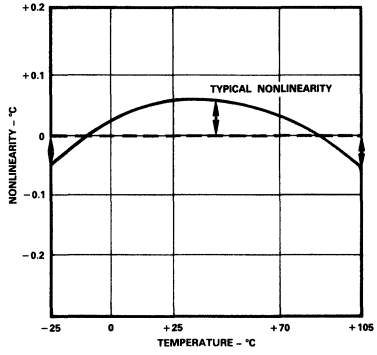


Figure 3. Nonlinearity Error (AD592CN)

TRIMMING FOR HIGHER ACCURACY

Calibration error at 25°C can be removed with a single temperature trim. Figure 4 shows how to adjust the AD592's scale factor in the basic voltage output circuit.

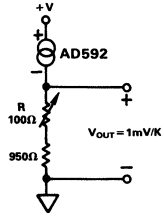


Figure 4. Basic Voltage Output (Single Temperature Trim)

To trim the circuit the temperature must be measured by a reference sensor and the value of R should be adjusted so the output (V_{OUT}) corresponds to 1mV/K. Note that the trim procedure should be implemented as close as possible to the temperature highest accuracy is desired for. In most applications if a single temperature trim is desired it can be implemented where the AD592 current-to-output voltage conversion takes place (e.g., output resistor, offset to an op amp). Figure 5 illustrates the effect on total error when using this technique.

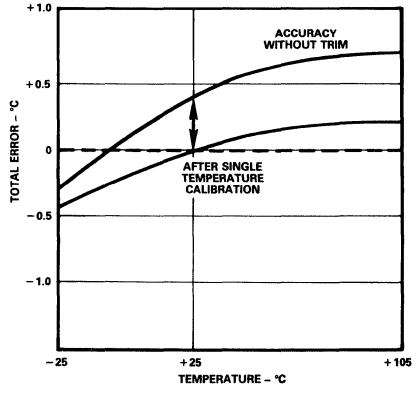


Figure 5. Effect of Scale Factor Trim on Accuracy

If greater accuracy is desired, initial calibration and scale factor errors can be removed by using the AD592 in the circuit of Figure 6.

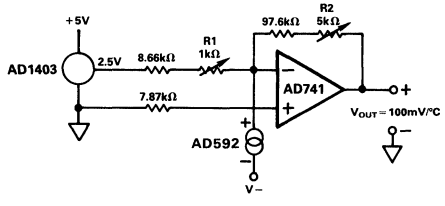


Figure 6. Two Temperature Trim Circuit

With the transducer at 0°C adjustment of R1 for a 0V output nulls the initial calibration error and shifts the output from K to °C. Tweaking the gain of the circuit at an elevated temperature by adjusting R2 trims out scale factor error. The only error remaining over the temperature range being trimmed for is nonlinearity. A typical plot of two trim accuracy is given in Figure 7.

SUPPLY VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection characteristics of the AD592 minimizes errors due to voltage irregularity, ripple and noise. If a supply is used other than 5V (used in factory trimming), the power supply error can be removed with a single temperature trim. The PTAT nature of the AD592 will remain unchanged. The general insensitivity of the output allows the use of lower cost unregulated supplies and means that a series resistance of several hundred ohms (e.g., CMOS multiplexer, meter coil resistance) will not degrade the overall performance.

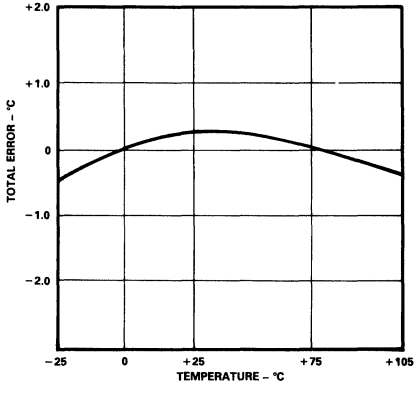


Figure 7. Typical Two Trim Accuracy

The thermal environment in which the AD592 is used determines two performance traits: the effect of self-heating on accuracy and the response time of the sensor to rapid changes in temperature. In the first case, a rise in the IC junction temperature above the ambient temperature is a function of two variables; the power consumption level of the circuit and the thermal resistance between the chip and the ambient environment (θ_{JA}). Self-heating error in °C can be derived by multiplying the power dissipation by θ_{JA}. Because errors of this type can vary widely for surroundings with different heat sinking capacities it is necessary to specify θ_{JA} under several conditions. Table I shows how the magnitude of self-heating error varies relative to the environment. In typical free air applications at 25°C with a 5V supply the magnitude of the error is 0.2°C or less. A common clip-on heat sink will reduce the error by 25% or more in critical high temperature, large supply voltage situations.

Medium	θ_{JA} (°C/watt)	τ (sec)*
Still Air		
Without Heat Sink	175	60
With Heat Sink	130	55
Moving Air		
Without Heat Sink	60	12
With Heat Sink	40	10
Fluorinert Liquid	35	5
Aluminum Block**	30	2.4

*τ is an average of five time constants (99.3% of final value). In cases where the thermal response is not a simple exponential function, the actual thermal response may be better than indicated.
**With thermal grease.

Table I. Thermal Characteristics

Response of the AD592 output to abrupt changes in ambient temperature can be modeled by a single time constant τ exponential function. Figure 8 shows typical response time plots for several media of interest.

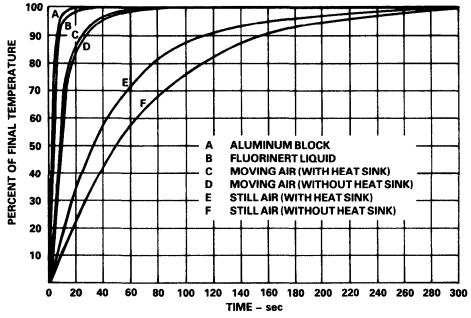


Figure 8. Thermal Response Curves

The time constant, τ, is dependent on θ_{JA} and the thermal capacities of the chip and the package.Table I lists the effective τ (time to reach 63.2% of the final value) for several different media. Copper printed circuit board connections where neglected in the analysis, however, they will sink or conduct heat directly through the AD592's solder dipped Kovar leads. When faster response is required a thermally conductive grease or glue between the AD592 and the surface temperature being measured should be used. In free air applications a clip-on heat sink will decrease output stabilization time by 10–20%.

MOUNTING CONSIDERATIONS

If the AD592 is thermally attached and properly protected, it can be used in any temperature measuring situation where the maximum range of temperatures encountered is between −25°C and +105°C. Because plastic IC packaging technology is employed, excessive mechanical stress must be safeguarded against when fastening the device with a clamp or screw-on heat tab. Thermally conductive epoxy or glue is recommended under typical mounting conditions. In wet or corrosive environments any electrically isolated metal or ceramic well can be used to shield the AD592. Condensation at cold temperatures can cause leakage current related errors and should be avoided by sealing the device in nonconductive epoxy paint or dips.

APPLICATIONS

Connecting several AD592 devices in parallel adds the currents through them and produces a reading proportional to the average temperature. Series AD592s will indicate the lowest temperature because the coldest device limits the series current flowing through the sensors. Both of these circuits are depicted in Figure 9.

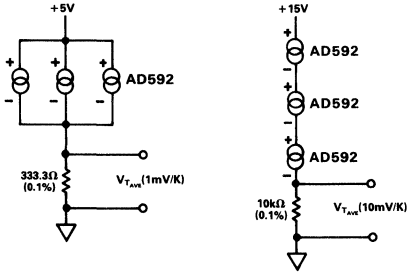


Figure 9. Average and Minimum Temperature Connections

The circuit of Figure 10 demonstrates a method in which a voltage output can be derived in a differential temperature measurement.

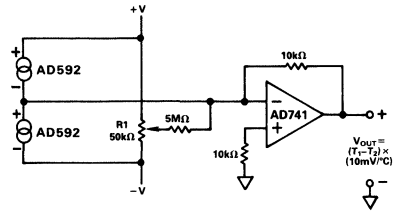


Figure 10. Differential Measurements

R1 can be used to trim out the inherent offset between the two devices. By increasing the gain resistor (10kΩ) temperature measurements can be made with higher resolution. If the magnitude of V+ and V− is not the same, the difference in power consumption between the two devices can cause a differential self-heating error.

Cold junction compensation (CJC) used in thermocouple signal conditioning can be implemented using an AD592 in the circuit configuration of Figure 11. Expensive simulated ice baths or hard to trim, inaccurate bridge circuits are no longer required.

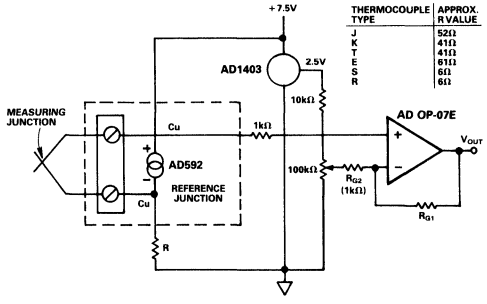


Figure 11. Thermocouple Cold Junction Compensation

The circuit shown can be optimized for any ambient temperature range or thermocouple type by simply selecting the correct value for the scaling resistor – R. The AD592 output (1μA/K) times R should approximate the line best fit to the thermocouple curve (slope in V/°C) over the most likely ambient temperature range. Additionally, the output sensitivity can be chosen by selecting the resistors R_{G1} and R_{G2} for the desired noninverting gain. The offset adjustment shown simply references the AD592 to °C. Note that the TC's of the reference and the resistors are the primary contributors to error. Temperature rejection of 40 to 1 can be easily achieved using the above technique.

Although the AD592 offers a noise immune current output, it is not compatible with process control/industrial automation current loop standards. Figure 12 is an example of a temperature to 4-20mA transmitter for use with 40V, 1kΩ systems.

In this circuit the 1μA/K output of the AD592 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. Rt is trimmed for proper reading at an

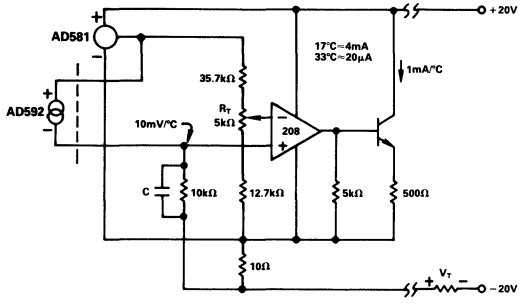


Figure 12. Temperature to 4–20mA Current Transmitter

intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD592 may be chosen.

Reading temperature with an AD592 in a microprocessor based system can be implemented with the circuit shown in Figure 13.

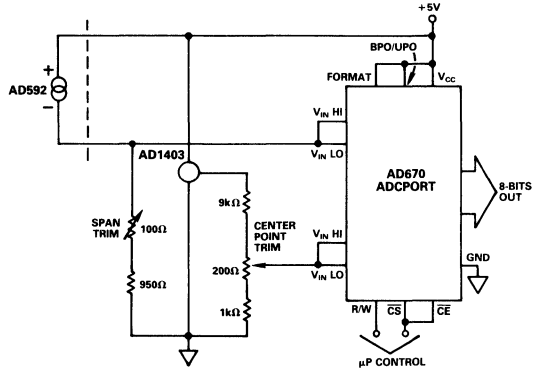


Figure 13. Temperature to Digital Output

By using a differential input A/D converter and choosing the current to voltage conversion resistor correctly any range of temperatures (up to the 130°C span the AD592 is rated for) centered at any point can be measured using a minimal number of components. In this configuration the system will resolve up to 1°C.

A variable temperature controlling thermostat can easily be built using the AD592 in the circuit of Figure 14.

R_{HIGH} and R_{LOW} determine the limits of temperature controlled by the potentiometer R_{SET}. The circuit shown operates over the full temperature range (−25°C to +105°C) the AD592 is rated for. The reference maintains a constant set point voltage and insures that approximately 7V appears across the sensor. If it is necessary to guardband for extraneous noise hysteresis can be added by tying a resistor from the output to the ungrounded end of R_{LOW}.

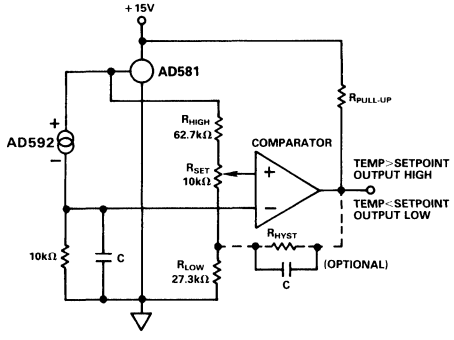


Figure 14. Variable Temperature Thermostat

Multiple remote temperatures can be measured using several AD592s with a CMOS multiplexer or a series of 5V logic gates because of the device's current-mode output and supply-voltage compliance range. The on-resistance of a FET switch or output impedance of a gate will not effect the accuracy, as long as 4V is maintained across the transducer. MUXs and logic driving circuits should be chosen to minimize leakage current related errors. Figure 15 illustrates a locally controlled MUX switching the signal current from several remote AD592s. CMOS or TTL gates can also be used to switch the AD592 supply voltages, with the multiplexed signal being transmitted over a single twisted pair to the load.

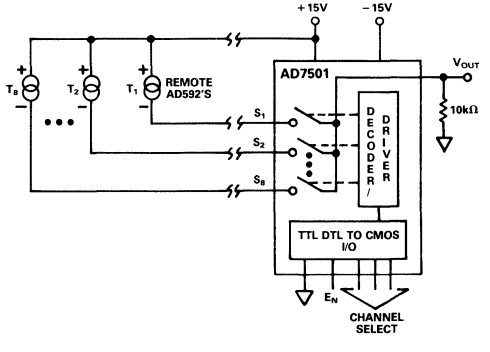


Figure 15. Remote Temperature Multiplexing

To minimize the number of MUXs required when a large number of AD592s are being used, the circuit can be configured in a matrix. That is, a decoder can be used to switch the supply voltage to a column of AD592s while a MUX is used to control which row of sensors are being measured. The maximum number of AD592s which can be used is the product of the number of channels of the decoder and MUX.

An example circuit controlling 80 AD592s is shown in Figure 16. A 7-bit digital word is all that is required to select one of the sensors. The enable input of the multiplexer turns all the sensors off for minimum dissipation while idling.

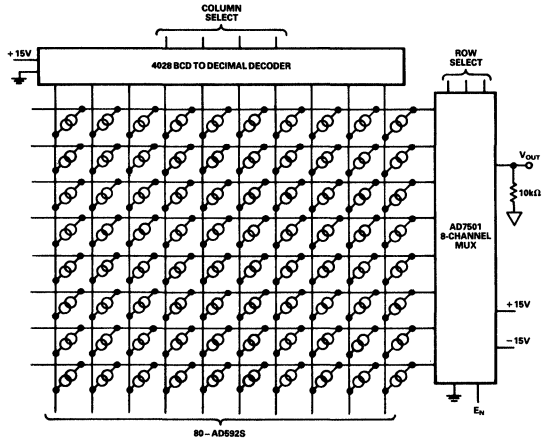
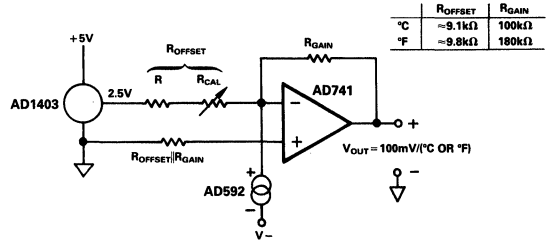


Figure 16. Matrix Multiplexer

To convert the AD592 output to °C or °F a single inexpensive reference and op amp can be used as shown in Figure 17. Although this circuit is similar to the two temperature trim circuit shown in Figure 6, two important differences exist. First, the gain resistor is fixed alleviating the need for an elevated temperature trim. Acceptable accuracy can be achieved by choosing an inexpensive resistor with the correct tolerance. Second, the AD592 calibration error can be trimmed out at a known convenient temperature (i.e., room temperature) with a single pot adjustment. This step is independent of the gain selection.



	R_{OFFSET}	R_{GAIN}
°C	≈9.1kΩ	100kΩ
°F	≈9.8kΩ	180kΩ

Figure 17. Celsius or Fahrenheit Thermometer

Low Power, Programmable Temperature Controller

TMP-01

FEATURES
−55°C to +150°C (−60°F to +300°F) Operation
2°C Accuracy Over Temperature
Temperature-Proportional Voltage Output
User-Programmable Temperature Trip Points
User-Programmable Hysteresis
20 mA Open-Collector Trip Point Outputs
TTL/CMOS Compatible
Single-Supply Operation (4.5 V to 25 V)
Low Cost 8-Pin DIP, SO, and TO-99 Packages

APPLICATIONS
Over/Under Temperature Sensor and Alarm
Board Level Temperature Sensing
Temperature Controllers
Electronic Thermostats
Thermal Protection
HVAC Systems
Industrial Process Control
Remote Sensors

GENERAL DESCRIPTION

The TMP-01 is a temperature sensor which generates a voltage output proportional to ambient temperature and a control signal from one of two outputs when the device is either above or below a specific temperature range. Both the high/low temperature trip points and hysteresis (overshoot) band are determined by user-selected external resistors. For high volume production, these resistors are available onboard.

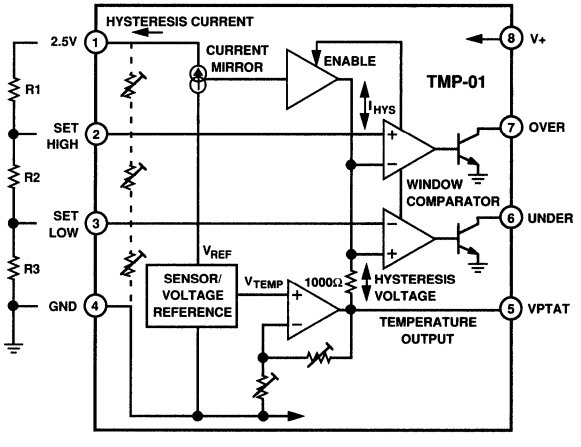
The TMP-01 consists of a bandgap voltage reference combined with a pair of matched comparators. The reference provides both a constant 2.5 V output and a voltage proportional to absolute temperature (VPTAT) which has a precise temperature coefficient of 5 mV/K and is 1.49 V (nominal) at +25°C. The comparators compare VPTAT with the externally set temperature trip points and generate an open-collector output signal when one of their respective thresholds has been exceeded. Hysteresis is also programmed by the external resistor chain and is determined by the total current drawn out of the 2.5 V reference. This current is mirrored and used to generate a hysteresis offset voltage of the appropriate polarity after a comparator has been tripped. The comparators are connected in parallel, which guarantees that there is no hysteresis overlap and eliminates erratic transitions between adjacent trip zones.

The TMP-01 utilizes proprietary thin film resistors in conjunction with production laser trimming to maintain a temperature accuracy of 2°C, with excellent linearity. The open-collector outputs are capable of sinking 20 mA, enabling the TMP-01 to drive control relays directly. Operating from a +5 V supply, quiescent current is only 400 μA (max).

The TMP-01 is available in the low cost 8-pin epoxy mini-DIP, cerdip, SO (small outline) packages, the TO-99 metal can, and in die form. Other industrial-grade packages will also be available. For applications requiring product which complies with MIL-STD/883 see the TMP-01/883 data sheet, available from your local sales office.

9

FUNCTIONAL BLOCK DIAGRAM



$$R1 + R2 + R3 = \frac{2.5}{(\text{HYSTERESIS} \times 0.005) + 0.010} = \text{RTOTAL}$$

$$R1 = \frac{(227 - \text{SETHIGH}) \times 0.005 \times \text{RTOTAL}}{2.5}$$

$$R3 = \frac{(\text{SETLOW} + 273) \times 0.005 \times \text{RTOTAL}}{2.5}$$

$$R2 = \text{RTOTAL} - R1 - R3$$

$$250k\Omega \geq R1 + R2 + R3 \geq 2.5k\Omega$$

TMP-01 —SPECIFICATIONS (V+ = +5 V, GND = 0 V, −40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUTS SET HIGH, SET LOW						
Setpoint Scale Factor				5		mV/K
Offset Voltage	V_{OS}				–	mV
Input Bias Current	I_B				–	nA
Nominal Input Voltage Range	V_{SET}		1.116		2.116	V
Input Voltage Range	V_{SET}	T_A = 25°C[1]	GND		V+ − TBD	V
OUTPUT VPTAT						
Scale Factor				5		mV/K
Nominal Output			1.116		2.116	V
Nominal Output		T_A = 25°C, I_{OUT} = TBD mA		1.49		V
Total Unadjusted Error, "E"	TUE	(Note 2)		±0.6	±1.2	K
Total Unadjusted Error, "F"	TUE	(Note 2)		±2	±4	K
Nonlinearity, "E"				0.4		%
Nonlinearity, "F"				0.8		%
Power Supply Rejection Ratio	PSRR	T_A = 25°C		0.1		%
OUTPUT 2.5 V						
Nominal Value	V_{REF}	T_A = 25°C		2.50	–	V
Drift				15	40	ppm/°C
Line Regulation		Over Supply Range		–		%/V
Load Regulation		Over I_{HYS} Range		–		%/mA
Output Current	I_{HYS}	To maintain rated accuracy			–	mA
Hysteresis Current Scale Factor				5		μA/Degree
Turn-On Settling Time		To rated accuracy[1]		–		ms
OPEN-COLLECTOR OUTPUTS OVER, UNDER						
Comparator Offset, "E"				0.3	0.6	mV
Comparator Offset, "F"				0.6	1.2	mV
Output Low Voltage	V_{OL}	I_{SINK} = 1 mA			–	mV
Output Low Voltage	V_{OL}	I_{SINK} = 20 mA		0.6		V
Output Leakage Current	I_{OH}			1	–	μA
Fall Time	t_{HL}	See Test Load[1]			–	ns
POWER SUPPLY						
Supply Range	V+		4.5		–	V
Supply Current	I_{SY}	Unloaded			–	μA

NOTES
[1]Guaranteed but not tested.
[2]Includes only the effects of self-heating due to quiescent currents and does not consider errors caused by heating due to dissipation of output load currents.
Specifications subject to change without notice.

Test Load
1 kΩ to V+, 20 pF to GND

ABSOLUTE MAXIMUM RATINGS*
Maximum Supply Voltage . . . . . +18 V
Maximum Output Current (Open Collector Outputs) . . 50 mA
Maximum Output Voltage (Open Collector Outputs) . . . . 18 V
Operating Temperature Range . . . . . −55°C to +150°C
Dice Junction Temperature . . . . . TBD
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

SPECIFICATIONS (V+ = +5 V, GND = 0 V, −55°C ≤ T_A ≤ +150°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUTS SET HIGH, SET LOW						
Setpoint Scale Factor				5		mV/K
Offset Voltage	V_{OS}				–	mV
Input Bias Current	I_B				–	nA
Nominal Input Voltage Range	V_{SET}		1.116		2.116	V
Input Voltage Range	V_{SET}	T_A = +25°C[1]	GND		V+ − TBD	V
OUTPUT VPTAT						
Scale Factor				5		mV/K
Nominal Output			1.116		2.116	V
Nominal Output		T_A = +25°C, I_{OUT} = TBD mA		1.49		V
Total Unadjusted Error, "A"	TUE	(Note 2)		±1	±2	K
Total Unadjusted Error, "B"	TUE	(Note 2)		±3	±6	K
Nonlinearity, "A"				0.5		%
Nonlinearity, "B"				1.0		%
Power Supply Rejection Ratio	PSRR	T_A = +25°C		0.1		%
OUTPUT 2.5V						
Nominal Value	V_{REF}	T_A = +25°C	–	2.50	–	V
Drift				15	40	ppm/°C
Line Regulation		Over Supply Range		–		%/V
Load Regulation		Over I_{HYS} Range		–		%/mA
Output Current	I_{HYS}	To maintain rated accuracy			–	mA
Hysteresis Current Scale Factor				5		μA/degree
Turn-On Settling Time		To rated accuracy[1]		–		ms
OPEN-COLLECTOR OUTPUTS OVER, UNDER						
Comparator Offset, "A"				0.5	1	mV
Comparator Offset, "B"				1	2	mV
Output Low Voltage	V_{OL}	I_{SINK} = 1 mA			–	mV
Output Low Voltage	V_{OL}	I_{SINK} = 20 mA		0.6		V
Output Leakage Current	I_{OH}			1	–	μA
Fall Time	t_{HL}	See Test Load[1]			–	ns
POWER SUPPLY						
Supply Range	V+		4.5		–	V
Supply Current	I_{SY}	Unloaded			–	μA

NOTES
[1]Guaranteed but not tested.
[2]Does not consider errors caused by heating due to dissipation of output load currents.
Specifications subject to change without notice.

Test Load
1 kΩ to V+, 20 pF to GND

GENERAL DESCRIPTION

The TMP-01 is a very linear voltage-output temperature sensor with a window comparator which can be programmed by the user to activate one of two open-collector outputs when a predetermined temperature setpoint has been exceeded. The temperature sensor is basically a very accurately temperature-compensated voltage reference, with a buffered output voltage proportional to absolute temperature (PTAT), accurately trimmed to a scale factor of 5 mV/K.

The low drift 2.5 V reference output serves two functions. The output voltage is easily divided externally with fixed resistors or potentiometers to establish the programmed heat/cool setpoints. In addition, the total output current of the reference determines the magnitude of the hysteresis band. As shown in the block diagram, this current is mirrored internally and fed to a bipolar three-state buffer. After a temperature setpoint has been exceeded and a comparator tripped, the buffer is enabled and outputs a current of the appropriate polarity which generates a hysteresis offset voltage across the 1000 Ω resistor at the comparator input. The comparator output remains HIGH until the voltage at the comparator input, equal to the temperature sensor voltage VPTAT summed with the hysteresis offset, has returned to the programmed setpoint. The comparator then returns LOW, deactivating the open-collector output and disabling the hysteresis current buffer.

With excellent drift and noise characteristics, the 2.5 V output offers a superior voltage reference for data acquisition and transducer excitation applications as well. Selection of a low drift buffer such as the OP-97 will ensure optimal reference accuracy without affecting the programmed hysteresis current.

Programming the TMP-01

The High/Low setpoints are easily programmed by the user with voltages divided down from the 2.5 V reference voltage output using fixed resistors or potentiometers. Alternatively, the setpoint voltages can be supplied by other ground-referenced voltage sources such as user-programmed DACs or controllers.

Noting that the hysteresis voltage is developed across 1000 Ω, with 5 mV/degree sensitivity at the inputs to the comparators the scale factor for the programmed hysteresis current flowing out of the 2.5 V reference output is 5 μA/degree. A 10 μA baseline must be included in calculating the desired hysteresis value to correct for the offset bias current of the reference.

Within the overall accuracy of the device, the minimum value of hysteresis that the user will obtain in practice is one degree or less with the maximum recommended 250 kΩ load.

Using the Nomograph

Figure 1 can help the user to obtain a rough-cut estimate of the external resistor values needed in the basic divider chain configuration to program the TMP-01 heat/cool setpoints and temperature hysteresis. The degrees Centigrade, degrees Farenheit, and VPTAT conversion scales are also useful in determining programming values. Examining the graph, it can be seen that each line dictates a range of resistor values across the operating temperature range of the TMP-01. For example, if 2 degrees of hysteresis is desired, the total reference current must be set to 20 μA, which dictates a divider chain of 125 kΩ total. Reading across and down from the 2°C line, we can see the approximate values of the resistor taps in the divider chain needed to set the desired heat/cool setpoints. Calculation of the actual values to be used, using the resistor formulas above, is recommended to obtain the exact temperature programming values desired.

Self-Heating Effects

Observing the thermal conductivity of the various TMP-01 packages, in some applications the user should consider the effects of self-heating due to the power dissipated by the open-collector outputs, which are capable of sinking up to 20 mA continuous. Under full load, the TMP-01 open-collector output device is dissipating

$$P_{DISS} = (0.6\ V)(0.020A) = 12\ mW$$

which in a free-standing surface-mount SO package accounts for a temperature increase due to self-heating of

$$\Delta T = P_{DISS} \times \theta_{JA} = 0.012\ W \times 158°C/W = 1.9°C.$$

This will of course directly affect the accuracy of the TMP-01 and will for example cause the device to switch the heating output "OFF" 2 degrees early. Alternatively, bonding the same package to a moderate heatsink limits the self-heating affect to approximately

$$\Delta T = P_{DISS} \times \theta_{JC} = 0.012W \times 45°C/W = 0.54°C.$$

which is a much more tolerable error in most systems.

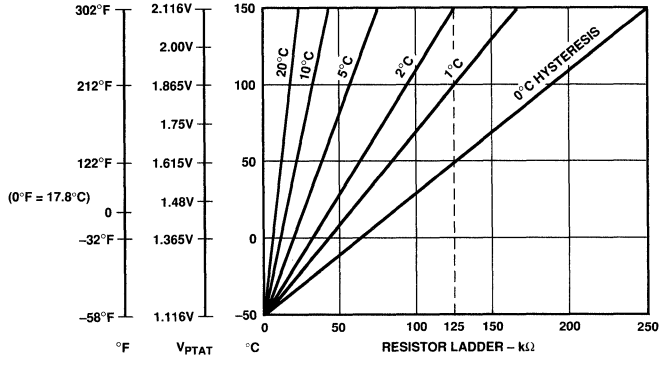
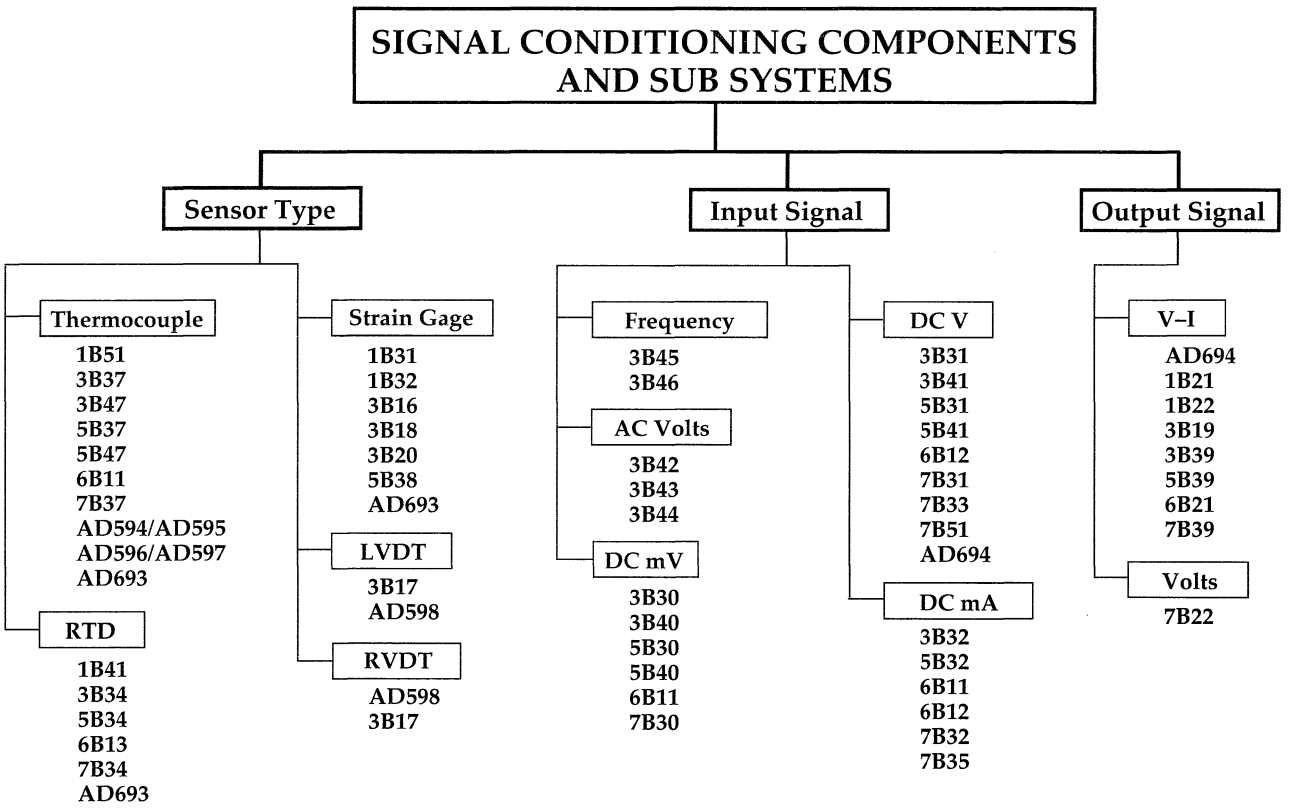


Figure 1. TMP-01 Nomograph

Signal Conditioning Components
Contents

Selection Tree
Signal Conditioning Components



Selection Guide
Signal Conditioning Components & Subsystems

Model	V/I Transmitters: Loop Power	V/I Transmitters: Local Power	Isolated	Sensor Excitation	Sensor Type(s)	IC	Hybrid Package	Module	Page[1]
AD594/AD595					**Thermocouple**	**X**			**10-9**
AD596/AD597					**Thermocouple**	**X**			**10-17**
AD598				**X**	**LVDT**	**X**			**10-23**
AD693	**X**	**X**		**X**	**mV: All**	**X**			**10-39**
AD694		**X**		**X**	**0–2 or 10 V Input Range**	**X**			**10-51**
1B21	**X**		**X**		**V–I**			**X**	**10-63**
1B22		**X**	**X**		**V–I**			**X**	**10-67**
1B31				**X**	**Strain Gage**		X		**10-71**
1B32				**X**	**Strain Gage**		**X**		**10-79**
1B41			**X**	**X**	**RTD**			**X**	**10-87**
1B51			**X**		**Thermocouple, mV**			**X**	**10-91**
AC1226			**Thermocouple Cold Junction Compensator**			**X**			**10-5**
2B20		X			V–I			X	10-95
2B22		X	X		V–I			X	10-99
2B23		X	X		V–I, Pin Programmable			X	10-103
2B24	X		X		I–I			X	D
2B30					Strain Gage, RTD			X	10-107
2B31					Strain Gage, RTD			X	10-107
2B50			X		Thermocouple, mV			X	10-113
2B52	X		X		Thermocouple, mV			X	D
2B53	X				Thermocouple, mV			X	D
2B54/2B55			X		Thermocouple, mV, 4-Channel			X	10-117
2B57	X			X	Solid State (AD590)			X	D
2B58				X	3-Wire RTD			X	D
2B59	X			X	3-Wire RTD			X	D
3B Series[2]	**Modular Signal Conditioning Subsystem, Flexible, User Configurable**								**D**
5B Series[2]	**Modular Signal Conditioning Subsystem; System Applications**								**D**
6B Series[2]	**Software Configurable, Digitizing Signal Conditioning Subsystem**								**D**
***7B Series[2]**	**Low Cost, Modular Process Control Signal Conditioners**								**10-123**

[1]D – data sheet available.
[2]For detailed information on 3B–7B Series, call 1-800-4-Analog and (for domestic versions only) request the *Data Acquisition and Control Catalog*. (For international versions, contact the local sales office.)
*New product.
Boldface Type: Product recommended for new design.

Orientation
Signal Conditioning Components

Signal conditioners provide an analog interface between sensors and the systems they serve. They amplify signals, provide zero suppression where necessary, introduce electrical isolation, furnish excitation for passive transducers and provide analog outputs in the form required by the system – either voltage or current – at appropriate levels.

The most popular sensors are thermocouples, RTDs (resistance temperature detectors) and strain gages; they are low-level devices requiring precision amplification with low drift and noise. A useful discussion of their properties and signal-conditioning requirements can be found in the Analog Devices *Transducer Interfacing Handbook* (1980, $14.50 postpaid), available from P.O.Box 9106, Norwood MA 02062-9106.

Signal-conditioning circuits can be assembled using many of the precision products to be found in this databook, such as operational amplifiers, instrumentation amplifiers, and isolation amplifiers, along with other electronic circuit elements and appropriate hardware. However, many system designers have found that, with less expenditure of valuable engineering talent, excellent and reliable results can be achieved at lower cost by purchasing complete dedicated signal conditioners with fully specified performance in standard packages.

Many sensors require auxiliary circuitry; for example, thermocouples require a constant-temperature reference junction or an equivalent "ice-point" reference circuit, and strain gages and RTDs are passive devices that need excitation. Although the results of a measurement may be produced – and are ultimately needed – in the form of voltage, they may have to be transmitted as a varying current with a standard span, such as 4 to 20mA; often the power for such current loops is furnished to the sensor and its conditioner from the remote destination.

Another requirement arises from the fact that systems often involve many diverse channels of measurement. Such systems need a *family* of signal conditioners to meet the multiplicity of functional needs, yet it is desirable that they be compactly and ruggedly housed, modular, provided with a power supply and capable of being interchanged as system needs change. It is for such applications that the 7B family and its housing was designed.

The *selection guide* lists the available devices that are recommended for new system designs, along with their salient features; detailed information will be found in the data sheets. Examples of such devices include conditioners for thermocouples, RTDs, strain gages, and low (mV)-level signal sources and current transmitters that convert the signal information to 4-20mA or 0-20mA currents for loops requiring analog information in that form.

The individually listed devices are manufactured in various forms, ranging from monolithic integrated circuits (AD594/595/596/597 and AD693/AD694) to devices in dual in-line packages – using hybrid and surface-mount technologies – to modules with either pins for chassis wiring or screw terminals for field wiring.

The *7B Series* of Process Control Signal Conditioners is a family of isolation-based, plug-in, signal-channel signal conditioners that accept inputs from a wide range of process control sensors and low level signals while providing high level output signals. Characterized by high performance, compact size and low cost, these modules have been optimized for use in process control applications.

The 7B modules are isolated (1.5kV rms), operate from a single +24V dc supply and have a ±0.1%, max calibrated accuracy; they are identical in size (1.7″ × 2.11″ × 0.60″) and are footprint compatible with standard solid-state relays. Signal conditioning functions include input protection, filtering, isolation, linearization for RTD and thermocouple inputs, excitation for remote transmitters and an output current module. User-specified custom ranges, that are technically feasible, can be supplied.

The 7B modules have 240 volt protection (−25°C to +85°C) for all field wiring terminations. All modules feature high common-mode rejection and operate over the extended industrial temperature range of −40°C to +85°C. The modules are packaged in a rugged, compact plastic case, and they utilize sturdy 0.04″ pin connections. No external adjustment potentiometers are provided, thus minimizing the possibility of mechanical or human errors in the field that may adversely affect the system integrity. The 7B modules are secured with a single self-contained mounting screw.

ANALOG DEVICES

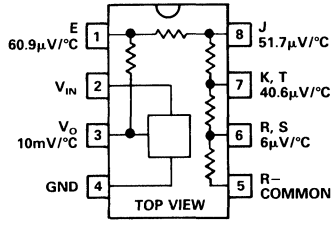
Micropower Thermocouple Cold Junction Compensator

AC1226

FEATURES
- 80μA Supply Current
- 4V to 36V Operation
- 0.5°C Typical Initial Accuracy
- Compatible with Standard Thermocouples (E, J, K, R, S, T)
- Auxiliary 10mV/°C Output
- Bow Corrected

APPLICATIONS
- Thermocouple Cold Junction Compensator
- Centigrade Thermometer
- Temperature Compensation Network

PIN CONFIGURATION

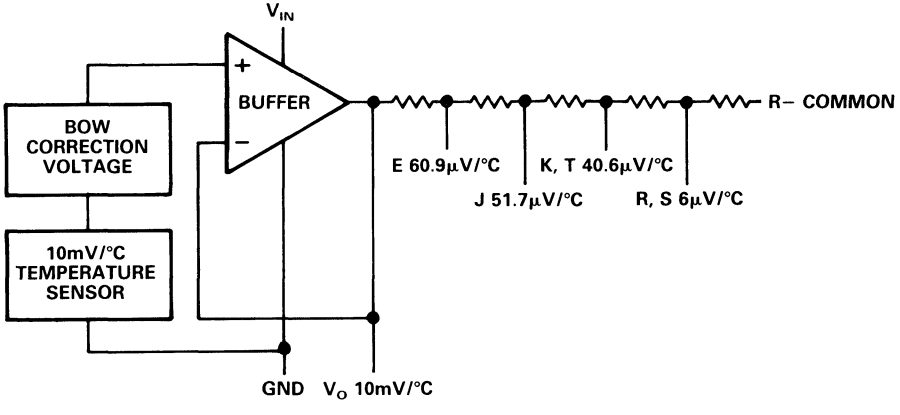


PRODUCT DESCRIPTION

The AC1226 is a micropower thermocouple cold junction compensator for use with type E, J, K, R, S and T thermocouples. It utilizes wafer level and post-package trimming to achieve typical 0.5°C initial accuracy. Special curvature correction circuitry is used to match the "bow" found in all thermocouples so that accurate cold junction compensation is maintained over a wider temperature range.

The AC1226 will operate with a supply voltage from 4V to 36V. Typical supply current is 80μA, resulting in less than 0.1°C internal temperature rise for supply voltages under 10V. A 10mV/°C output is available at low impedance in addition to the direct thermocouple voltages of 60.9μV/°C (E), 51.7μV/°C (J), 40.3μV/°C (K, T) and 5.95μV/°C (R, S). All outputs are essentially independent of power supply voltage.

The AC1226 is available in an 8-pin plastic mini-DIP for temperatures between 0 and +70°C.



AC1226 Block Diagram

10

AC1226—SPECIFICATIONS

Electrical Characteristics (V_S = 5V, T_A = +25°C, Pin 5 tied to Pin 4, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Units
TEMPERATURE ERROR AT 10mV/°C OUTPUT[1,2]	T_J = +25°C Full Temperature Span*		0.5 See Curve	2.0	°C
RESISTOR DIVIDER ACCURACY[1,3]	V_{OUT} = 10mV/°C E J K, T R, S	 60.4 51.2 40.2 5.75	 60.9 51.7 40.6 5.95	 61.6 52.3 41.2 6.3	µV/°C
SUPPLY CURRENT	4V≤V_{IN}≤36V *	50 50	80	100 150	µA
LINE REGULATION[4]	4V≤V_{IN}≤36V*		0.003	0.02	°C/V
LOAD REGULATION[4]	0≤I_O≤1mA*		0.04	0.2	°C
DIVIDER IMPEDANCE	E J K, T R, S		2.5 2.1 4.4 3.8		kΩ
CHANGE IN SUPPLY CURRENT	4V≤V_{IN}≤36V		0.01	0.05	µA/V
PACKAGE OPTION[5] Plastic DIP (N-8)					

NOTES

[1]To calculate total temperature error at individual thermocouple outputs, add 10mV/°C output error to the resistor divider error. Total error for type K output at +25°C with an AC1226 is 2.0°C plus (0.6µV/°C) (25°C)/(40.6µV/°C=2.0°C+0.37°C=2.37°C.

[2]Temperature error is defined as the deviation from the following formula: V_{OUT}=10mV(T) + (10mV)(5.5×10^{-4})(T−25°C)^2. The second term is a built-in nonlinearity designed to help compensate the nonlinearity of the cold junction. This "bow" is ≈0.34°C for a 25°C temperature change.

[3]Divider accuracy is measured by applying a 10.000V signal to the output divider and measuring the individual outputs.

[4]Regulation does not include the effects of self-heating. See "Internal Temperature Rise" in Application Guide. Load regulation is 30µA≤I_O≤1mA for T_A≤0°C.

[5]For outline information see Package Information section.

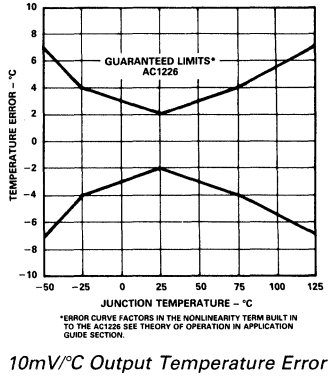
*Denotes the specifications which apply over the full operating temperature range.

Specifications subject to change without notice.

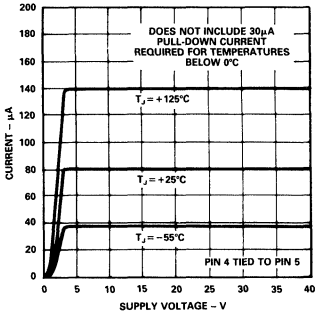
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage 36V
Output Voltage (Forced) 5V
Output Short Circuit Duration . . . . . .Indefinite
Operating Temperature Range . . . . . .0 to +70°C
Storage Temperature Range . . . . . .−55°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . .+300°C

Typical Performance Characteristics



10mV/°C Output Temperature Error



Supply Current

APPLICATION GUIDE

The AC1226 was designed to be extremely easy to use, but the following ideas and suggestions should be helpful in obtaining the best possible performance and versatility from this new cold junction compensator.

THEORY OF OPERATION

A thermocouple consists of two dissimilar metals joined together. A voltage (Seebeck EMF) will be generated if the two ends of the thermocouple are at different temperatures. In Figure 1, iron and constantan are joined at the temperature measuring point T1. Two additional thermocouple junctions are formed where the iron and constantan connect to ordinary copper wire. For the purposes of this discussion it is assumed that these two junctions are at the same temperature, T2. The Seebeck voltage, V_S, is the product of the Seebeck coefficient α, and the temperature difference, T1–T2; $V_S = \alpha$ (T1–T2). The junctions at T2 are commonly called the cold junction because a common practice is to immerse the T2 junction in 0°C ice/water slurry to make T2 independent of room temperature variations. Thermocouple tables are based on a cold junction temperature of 0°C.

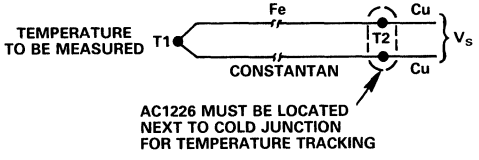


Figure 1.

For most applications an electronically simulated cold junction is required. The idea is basically to add a temperature dependent voltage to V_S such that the voltage sum is the same as if the T2 junction were at a constant 0°C instead of at room temperature. This voltage source is called a cold junction compensator. Its output is designed to be 0V at 0°C and have a slope equal to the Seebeck coefficient over the expected range of T2 temperatures.

To operate properly, a cold junction compensator must be at exactly the same temperature as the cold junction of the thermocouple (T2). *Therefore, it is important to locate the AC1226 physically close to the cold junction with local temperature gradients minimized.* If this is not possible, an extender made of matching thermocouple wire can be used. This shifts the cold junction from the user termination to the end of the extender so that the AC1226 can be located remotely from the user termination as shown in Figure 2.

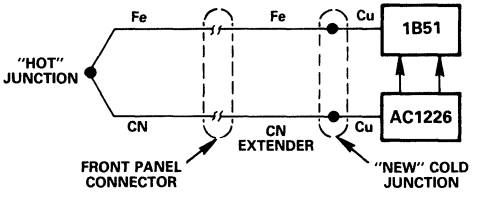


Figure 2.

The four thermocouple outputs on the AC1226 are 60.9μV/°C (E), 51.7μV/°C (J), 40.6μV/°C (K and T) and 6μV/°C (R and S). These particular coefficients are chosen to match the room temperature (+25°C) slope of the thermocouples. Over wide temperature ranges, however, the slope of thermocouples changes, yielding a quasi-parabolic error compared to a constant slope. The AC1226 outputs have a deliberate parabolic "bow" to help compensate for this effect. The outputs can be mathematically described as the sum of a linear term equal to room temperature slope plus a quadratic term proportional to temperature deviation from +25°C *squared*. The coefficient (β) of the quadratic term is a compromise value chosen to offer improvement in all the outputs.

$$V_{OUT} = \alpha T + \beta(T - 25°C)^2$$
$$\beta \approx 5.5 \times 10^{-4}$$

The actual β term which would be required to best compensate each thermocouple type in the temperature range of 0 to +50°C is: E, 6.6×10^{-4}; J, 4.8×10^{-4}; K, 4.3×10^{-4}; R, 1.9×10^{-3}; S, 1.9×10^{-3}; T, 1×10^{-3}.

The temperature error specification for the AC1226 (shown as a graph) assumes a β of 5.5×10^{-4}. For example, an AC1226 is considered "perfect" if its 10mV/°C output fits the equation $V_O = 10mV(T) + 5.5 \times 10^{-4}(T-25)^2$.

OPERATING AT NEGATIVE TEMPERATURES

The AC1226 is designed to operate with a single positive supply. It therefore cannot deliver proper outputs for temperatures below zero unless an external pull-down resistor is added to the V_O output. This resistor can be connected to any convenient negative supply. It should be selected to sink at least 30μA of current. Suggested value for a −5V supply is 150kΩ, and for a −15V supply, 470kΩ. Smaller resistors must be used if an external load is connected to the 10mV/°C output. The AC1226 can source up to 1mA of current, but there is a trade-off with internal temperature rise.

INTERNAL TEMPERATURE RISE

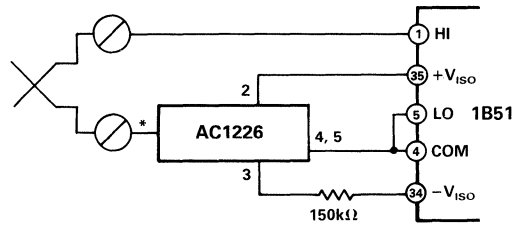
The AC1226 is specified for temperature accuracy assuming no internal temperature rise. At low supply voltages this rise is usually negligible (≈0.05°C @ 5V), but at higher supply voltages or with external loads or pull-down current, internal rise could become significant. This effect can be calculated from a simple thermal formula, $\Delta T = (\theta J_A)(V^+)(I_Q + I_L)$, where θJ_A is thermal resistance from junction to ambient (≈130°C/W), V^+ is the AC1226 supply voltage, I_Q, is the AC1226 supply current (≈80μA), and I_L is the total load current including actual load to ground and any pull-down current needed to generate negative outputs. A sample calculation with a 15V supply and 50μA pull-down current would yield, (130°C/W) (15V) (80+50μA) = 0.32°C. This is a significant rise in some applications. It can be reduced by lowering supply voltage (a simple fix is to insert a 10V Zener in the V_{IN} lead) or the system can be calibrated and specified after an initial warm-up period of several minutes.

THERMOCOUPLE EFFECTS IN LEADS

Thermocouple voltages are generated whenever dissimilar materials are joined. *This includes the leads of IC packages,* which may be kovar in TO-5 cans, alloy 42 or copper in dual-in-line packages, and a variety of other materials in plating finishes and solders. The net effect of these thermocouples is "zero" if all are at exactly the same temperature, but temperature gradients exist within IC packages and across PC boards whenever power is dissipated. For this reason, extreme care must be used to ensure that no temperature gradients exist in the vicinity of thermocouple terminations, the AC1226, or the thermocouple amplifier. If a gradient cannot be eliminated, leads should be positioned isothermally, especially the AC1226 R^- and appropriate output pins, the amplifier input pins and the gain setting resistor leads. An effect to watch for is amplifier offset voltage warm-up drift caused by mismatched thermocouple materials in the wire bond/lead system of the package. This effect can be as high as tens of microvolts in TO-5 cans with kovar leads. It has nothing to do with the actual offset drift specification of the amplifier and can occur in amplifiers with measured "zero" drift. Warm-up drift is directly proportional to amplifier power dissipation. It can be minimized by avoiding TO-5 cans, using low supply current amplifiers and by using the lowest possible supply voltages. Finally, it can be accommodated by calibrating and specifying the system after a five minute warm-up period.

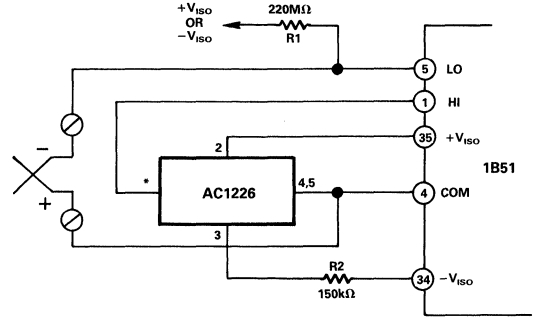
Figure 3 shows how to connect the AC1226 to the IB51 to compensate for the cold junction. This circuit is a conditioned and isolated channel for E, J, K, R, S or T thermocouples.

Figure 4 shows optional AC1226/1B51 connections with open input detection. This circuit minimizes input offset error generated by the pull up (or pull down) resistor, by eliminating the AC1226's divider impedance as seen by theresistor R1.



*PIN NUMBER DEPENDS ON THERMOCOUPLE TYPE.

Figure 3. Using the AC21226 with the 1B51, Isolated mV/Thermocouple Signal Conditioner



*PIN NUMBER DEPENDS ON THERMOCOUPLE TYPE.

Figure 4. Optional AC1226/1B51 Connections for Thermocouple Input with Open Detection Circuit

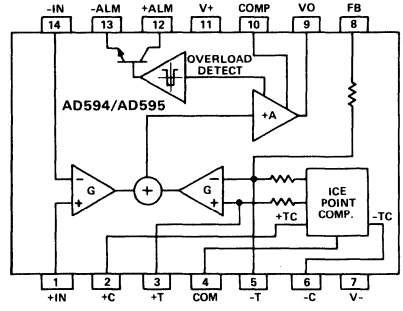
Monolithic Thermocouple Amplifiers with Cold Junction Compensation

AD594*/AD595*

FEATURES

- **Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples**
- **Can Be Used with Type T Thermocouple Inputs**
- **Low Impedance Voltage Output: 10mV/°C**
- **Built-in Ice Point Compensation**
- **Wide Power Supply Range: +5V to ±15V**
- **Low Power: <1mW typical**
- **Thermocouple Failure Alarm**
- **Laser Wafer Trimmed to 1°C Calibration Accuracy**
- **Set-Point Mode Operation**
- **Self-Contained Celsius Thermometer Operation**
- **High Impedance Differential Input**
- **Side-Brazed DIP or Low Cost Cerdip**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low-impedance voltage output.

The AD594/AD595 includes a thermocouple failure alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD594/AD595 can be powered from a single ended supply (including +5V) and by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will typically operate with a total supply current of 160μA, but is also capable of delivering in excess of ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristic of type J (iron-constantan) thermocouples and the AD595 is laser trimmed for type K (chromel-alumel) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of two or three resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications.

*Protected by U.S. Patent No. 4,029,974.

The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used from 0 to +50°C, and are available in 14-pin, hermetically sealed, side-brazed ceramic DIPs as well as low cost cerdip packages.

PRODUCT HIGHLIGHTS

1. The AD594/AD595 provides cold junction compensation, amplification, and an output buffer in a single IC package.
2. Compensation, zero, and scale factor are all precalibrated by laser wafer trimming (LWT) of each IC chip.
3. Flexible pin-out provides for operation as a set-point controller or a stand-alone temperature transducer calibrated in degrees Celsius.
4. Operation at remote application sites is facilitated by low quiescent current and a wide supply voltage range of +5V to dual supplies spanning 30V.
5. Differential input rejects common-mode noise voltage on the thermocouple leads.

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AD594/AD595—SPECIFICATIONS (@ +25°C and V_S = 5 V, Type J (AD594), Type K (AD595) Thermocouple, unless otherwise noted)

Model	AD594A			AD594C			AD595A			AD595C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS													
$+V_S$ to $-V_S$			36			36			36			36	Volts
Common-Mode Input Voltage	$-V_S$ −0.15		$+V_S$	$-V_S$ −0.15		$+V_S$	$-V_S$ −0.15		$+V_S$	$-V_S$ −0.15		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages													
+ALM	$-V_S$		$-V_S$ +36	$-V_S$		$-V_S$ +36	$-V_S$		$-V_S$ +36	$-V_S$		$-V_S$ +36	Volts
−ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	−55		+125	−55		+125	−55		+125	−55		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			Indefinite			Indefinite			
TEMPERATURE MEASUREMENT													
(Specified Temperature Range 0 to +50°C)													
Calibration Error at +25°C[1]			**±3**			**±1**			**±3**			**±1**	°C
Stability vs. Temperature[2]			**±0.05**			**±0.025**			**±0.05**			**±0.025**	°C/°C
Gain Error			**±1.5**			**±0.75**			**±1.5**			**±0.75**	%
Nominal Transfer Function			10			10			10			10	mV/°C
AMPLIFIER CHARACTERISTICS													
Closed Loop Gain[3]		**193.4**			**193.4**			**247.3**			**247.3**		
Input Offset Voltage	(Temperature in °C)×51.70 μV/°C			(Temperature in °C)×51.70 μV/°C			(Temperature in °C)×40.44 μV/°C			(Temperature in °C)×40.44 μV/°C			μV
Input Bias Current		0.1			0.1			0.1			0.1		μA
Differential Input Range	−10		+50				−10		+50	−10		+50	mV
Common-Mode Range	**$-V_S$ −0.15**		**$+V_S$ −4**	**$-V_S$ −0.15**		**$+V_S$ −4**	**$-V_S$ −0.15**		**$+V_S$ −4**	**$-V_S$ −0.15**		**$+V_S$ −4**	Volts
Common-Mode Sensitivity – RTO		**10**			**10**			**10**			**10**		mV/V
Power Supply Sensitivity – RTO		**10**			**10**			**10**			**10**		mV/V
Output Voltage Range													
Dual Supplies	**$-V_S$ +2.5**		**$+V_S$ −2**	**$-V_S$ +2.5**		**$+V_S$ −2**	**$-V_S$ +2.5**		**$+V_S$ −2**	**$-V_S$ +2.5**		**$+V_S$ −2**	Volts
Single Supply	0		$+V_S$ −2	0		$+V_S$ −2	0		$+V_S$ +2	0		$+V_S$ −2	Volts
Usable Output Current[4]		±5			±5			±5			±5		mA
3 dB Bandwidth		15			15			15			15		kHz
ALARM CHARACTERISTICS													
$V_{CE(SAT)}$ at 2 mA		0.3			0.3			0.3			0.3		Volts
Leakage Current			**±1**			**±1**			**±1**			**±1**	μA max
Operating Voltage at – ALM			**$+V_S$ −4**			**$+V_S$ −4**			**$+V_S$ −4**			**$+V_S$ −4**	Volts
Short Circuit Current		20			20			20			20		mA
POWER REQUIREMENTS													
Specified Performance	$+V_S$ = 5, $-V_S$ = 0			$+V_S$ = 5, $-V_S$ = 0			$+V_S$ = 5, $-V_S$ = 0			$+V_S$ = 5, $-V_S$ = 0			Volts
Operating[5]	$+V_S$ to $-V_S$ ≤30			$+V_S$ to $-V_S$ ≤30			$+V_S$ to $-V_S$ ≤30			$+V_S$ to $-V_S$ ≤30			Volts
Quiescent Current (No Load)													
$+V_S$		160	300		160	300		160	300		160	300	μA
$-V_S$		100			100			100			100		μA
PACKAGE OPTION[6]													
TO-116 (D-14)	AD594AD			AD594CD			AD595AD			AD595CD			
Cerdip (Q-14A)	AD594AQ			AD594CQ			AD595AQ			AD595CQ			

NOTES

[1]Calibrated for minimum error at +25°C using a thermocouple sensitivity of 51.7 μV/°C. Since a J type thermocouple deviates from this straight line approximation, the AD594 will normally read 3.1 mV when the measuring junction is at 0°C. The AD595 will similarly read 2.7 mV at 0°C.

[2]Defined as the slope of the line connecting the AD594/AD595 errors measured at 0°C and 50°C ambient temperature.

[3]Pin 8 shorted to Pin 9.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50 kΩ resistor at output voltages below 2.5 V.

[5]$-V_S$ must not exceed −16.5 V.

[6]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Thermocouple Temperature °C	Type J Voltage mV	AD594 Output mV	Type K Voltage mV	AD595 Output mV
− 200	− 7.890	− 1523	− 5.891	− 1454
− 180	− 7.402	− 1428	− 5.550	− 1370
− 160	− 6.821	− 1316	− 5.141	− 1269
− 140	− 6.159	− 1188	− 4.669	− 1152
− 120	− 5.426	− 1046	− 4.138	− 1021
− 100	− 4.632	− 893	− 3.553	− 876
− 80	− 3.785	− 729	− 2.920	− 719
− 60	− 2.892	− 556	− 2.243	− 552
− 40	− 1.960	− 376	− 1.527	− 375
− 20	− .995	− 189	− .777	− 189
− 10	− .501	− 94	− .392	− 94
0	0	3.1	0	2.7
10	.507	101	.397	101
20	1.019	200	.798	200
25	1.277	250	1.000	250
30	1.536	300	1.203	300
40	2.058	401	1.611	401
50	2.585	503	2.022	503
60	3.115	606	2.436	605
80	4.186	813	3.266	810
100	5.268	1022	4.095	1015
120	6.359	1233	4.919	1219
140	7.457	1445	5.733	1420
160	8.560	1659	6.539	1620
180	9.667	1873	7.338	1817
200	10.777	2087	8.137	2015
220	11.887	2302	8.938	2213
240	12.998	2517	9.745	2413
260	14.108	2732	10.560	2614
280	15.217	2946	11.381	2817
300	16.325	3160	12.207	3022
320	17.432	3374	13.039	3327
340	18.537	3588	13.874	3434
360	19.640	3801	14.712	3641
380	20.743	4015	15.552	3849
400	21.846	4228	16.395	4057
420	22.949	4441	17.241	4266
440	24.054	4655	18.088	4476
460	25.161	4869	18.938	4686
480	26.272	5084	19.788	4896
500	27.388	5300	20.640	5107
520	28.511	5517	21.493	5318
540	29.642	5736	22.346	5529
560	30.782	5956	23.198	5740
580	31.933	6179	24.050	5950
600	33.096	6404	24.902	6161
620	34.273	6632	25.751	6371
640	35.464	6862	26.599	6581
660	36.671	7095	27.445	6790
680	37.893	7332	28.288	6998
700	39.130	7571	28.128	7206
720	40.382	7813	29.965	7413
740	41.647	8058	30.799	7619
750	42.283	8181	31.214	7722
760	–	–	31.629	7825
780	–	–	32.455	8029
800	–	–	33.277	8232
820	–	–	34.095	8434
840	–	–	34.909	8636
860	–	–	35.718	8836
880	–	–	36.524	9035
900	–	–	37.325	9233
920	–	–	38.122	9430
940	–	–	38.915	9626
960	–	–	39.703	9821
980	–	–	40.488	10015
1000	–	–	41.269	10209
1020	–	–	42.045	10400
1040	–	–	42.817	10591
1060	–	–	43.585	10781
1080	–	–	44.349	10970
1100	–	–	45.108	11158
1120	–	–	45.863	11345
1140	–	–	46.612	11530
1160	–	–	47.356	11714
1180	–	–	48.095	11897
1200	–	–	48.828	12078
1220	–	–	49.555	12258
1240	–	–	50.276	12436
1250	–	–	50.633	12524

Table I. Output Voltage vs. Thermocouple Temperature (Ambient +25°C, V_S = −5V, +15V)

INTERPRETING AD594/AD595 OUTPUT VOLTAGES

To achieve a temperature proportional output of 10mV/°C and accurately compensate for the reference junction over the rated operating range of the circuit, the AD594/AD595 is gain trimmed to match the transfer characteristic of J and K type thermocouples at 25°C. For a type J output in this temperature range the TC is 51.70μV/°C, while for a type K it is 40.44μV/°C. The resulting gain for the AD594 is 193.4 (10mV/°C divided by 51.7μV/°C) and for the AD595 is 247.3 (10mV/°C divided by 40.44μV/°C). In addition, an absolute accuracy trim induces an input offset to the output amplifier characteristic of 16μV for the AD594 and 11μV for the AD595. This offset arises because the AD594/AD595 is trimmed for a 250mV output while applying a 25°C thermocouple input.

Because a thermocouple output voltage is nonlinear with respect to temperature, and the AD594/AD595 linearly amplifies the compensated signal, the following transfer functions should be used to determine the actual output voltages:

AD594 output = (Type J Voltage + 16μV) × 193.4

AD595 output = (Type K Voltage + 11μV) × 247.3
or conversely:

Type J voltage = (AD594 output / 193.4) − 16μV

Type K voltage = (AD595 output / 247.3) − 11μV

Table I above lists the ideal AD594/AD595 output voltages as a function of Celsius temperature for type J and K ANSI standard thermocouples, with the package and reference junction at 25°C. As is normally the case, these outputs are subject to calibration, gain and temperature sensitivity errors. Output values for intermediate temperatures can be interpolated, or calculated using the output equations and ANSI thermocouple voltage tables referred to zero degrees Celsius. Due to a slight variation in alloy content between ANSI type J and DIN FE–CUNI thermocouples Table I should not be used in conjunction with European standard thermocouples. Instead the transfer function given previously and a DIN thermocouple table should be used. ANSI type K and DIN NICR–NI thermocouples are composed of identical alloys and exhibit similar behavior. The upper temperature limits in Table I are those recommended for type J and type K thermocouples by the majority of vendors.

SINGLE AND DUAL SUPPLY CONNECTIONS

The AD594/AD595 is a completely self-contained thermocouple conditioner. Using a single +5V supply the interconnections shown in Figure 1 will provide a direct output from a type J thermocouple (AD594) or type K thermocouple (AD595) measuring from 0 to +300°C.

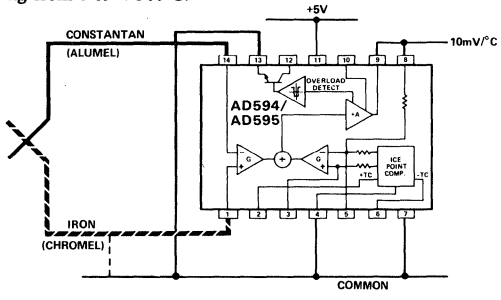

Figure 1. Basic Connection, Single Supply Operation

Any convenient supply voltage from +5V to +30V may be used, with self-heating errors being minimized at lower supply levels. In the single supply configuration the +5V supply connects to pin 11 with the V− connection at pin 7 strapped to power and signal common at pin 4. The thermocouple wire inputs connect to pins 1 and 14 either directly from the measuring point or through intervening connections of similar thermocouple wire type. When the alarm output at pin 13 is not used it should be connected to common or −V. The precalibrated feedback network at pin 8 is tied to the output at pin 9 to provide a 10mV/°C nominal temperature transfer characteristic.

By using a wider ranging dual supply, as shown in Figure 2, the AD594/AD595 can be interfaced to thermocouples measuring both negative and extended positive temperatures.

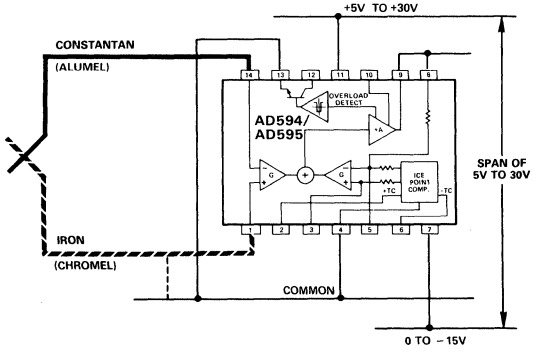

Figure 2. Dual Supply Operation

With a negative supply the output can indicate negative temperatures and drive grounded loads or loads returned to positive voltages. Increasing the positive supply from 5V to 15V extends the output voltage range well beyond the 750°C temperature limit recommended for type J thermocouples (AD594) and the 1250°C for type K thermocouples (AD595).

Common-mode voltages on the thermocouple inputs must remain within the common-mode range of the AD594/AD595, with a return path provided for the bias currents. If the thermocouple is not remotely grounded, then the dotted line connections in Figures 1 and 2 are recommended. A resistor may be needed in this connection to assure that common mode voltages induced in the thermocouple loop are not converted to normal mode.

THERMOCOUPLE CONNECTIONS

The isothermal terminating connections of a pair of themocouple wires forms an effective reference junction. This junction must be kept at the same temperature as the AD594/AD595 for the internal cold junction compensation to be effective.

A method that provides for thermal equilibrium is the printed circuit board connection layout illustrated in Figure 3.

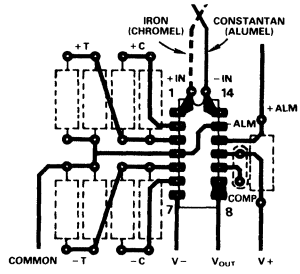

Figure 3. PCB Connections

Here the AD594/AD595 package temperature and circuit board are thermally contacted in the copper printed circuit board tracks under pins 1 and 14. The reference junction is now composed of a copper-constantan (or copper-alumel) connection and copper-iron (or copper-chromel) connection, both of which are at the same temperature as the AD594/AD595.

The printed circuit board layout shown also provides for placement of optional alarm load resistors, recalibration resistors and a compensation capacitor to limit bandwidth.

To ensure secure bonding the thermocouple wire should be cleaned to remove oxidation prior to soldering. Noncorrosive rosin flux is effective with iron, constantan, chromel and alumel and the following solders: 95% tin-5% antimony, 95% tin-5% silver or 90% tin-10% lead.

FUNCTIONAL DESCRIPTION

The AD594 behaves like two differential amplifiers. The outputs are summed and used to control a high-gain amplifier, as shown in Figure 4.

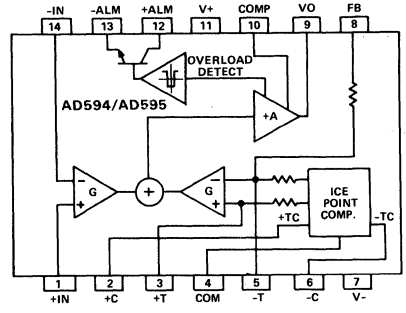

Figure 4. AD594/AD595 Block Diagram

In normal operation the main amplifier output, at pin 9, is connected to the feedback network, at pin 8. Thermocouple signals applied to the floating input stage, at pins 1 and 14, are

amplified by gain G of the differential amplifier and are then further amplified by gain A in the main amplifier. The output of the main amplifier is fed back to a second differential stage in an inverting connection. The feedback signal is amplified by this stage and is also applied to the main amplifier input through a summing circuit. Because of the inversion, the amplifier causes the feedback to be driven to reduce this difference signal to a small value. The two differential amplifiers are made to match and have identical gains, G. As a result, the feedback signal that must be applied to the right-hand differential amplifier will precisely match the thermocouple input signal when the difference signal has been reduced to zero. The feedback network is trimmed so that the effective gain to the output, at pins 8 and 9, results in a voltage of 10mV/°C of thermocouple excitation.

In addition to the feedback signal, a cold junction compensation voltage is applied to the right-hand differential amplifier. The compensation is a differential voltage proportional to the Celsius temperature of the AD594/AD595. This signal disturbs the differential input so that the amplifier output must adjust to restore the input to equal the applied thermocouple voltage.

The compensation is applied through the gain scaling resistors so that its effect on the main output is also 10mV/°C. As a result, the compensation voltage adds to the effect of the thermocouple voltage a signal directly proportional to the difference between 0°C and the AD594/AD595 temperature. If the thermocouple reference junction is maintained at the AD594/AD595 temperature, the output of the AD594/AD595 will correspond to the reading that would have been obtained from amplification of a signal from a thermocouple referenced to an ice bath.

The AD594/AD595 also includes an input open circuit detector that switches on an alarm transistor. This transistor is actually a current-limited output buffer, but can be used up to the limit as a switch transistor for either pull-up or pull-down operation of external alarms.

The ice point compensation network has voltages available with positive and negative temperature coefficients. These voltages may be used with external resistors to modify the ice point compensation and recalibrate the AD594/AD595 as described in the next column.

The feedback resistor is separately pinned out so that its value can be padded with a series resistor, or replaced with an external resistor between pins 5 and 9. External availability of the feedback resistor allows gain to be adjusted, and also permits the AD594/AD595 to operate in a switching mode for set-point operation.

CAUTIONS:

The temperature compensation terminals (+C and −C) at pins 2 and 6 are provided to supply small calibration currents only. The AD594/AD595 may be permanently damaged if they are grounded or connected to a low impedance.

The AD594/AD595 is internally frequency compensated for feedback ratios (corresponding to normal signal gain) of 75 or more. If a lower gain is desired, additional frequency compensation should be added in the form of a 300pF capacitor from pin 10 to the output at pin 9. As shown in Figure 5 an additional 0.01μF capacitor between pins 10 and 11 is recommended.

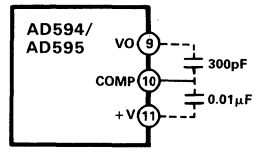

Figure 5. Low Gain Frequency Compensation

RECALIBRATION PRINCIPLES AND LIMITATIONS

The ice point compensation network of the AD594/AD595 produces a differential signal which is zero at 0°C and corresponds to the output of an ice referenced thermocouple at the temperature of the chip. The positive TC output of the circuit is proportional to Kelvin temperature and appears as a voltage at +T. It is possible to decrease this signal by loading it with a resistor from +T to COM, or increase it with a pull-up resistor from +T to the larger positive TC voltage at +C. Note that adjustments to +T should be made by measuring the voltage which tracks it at −T. To avoid destabilizing the feedback amplifier the measuring instrument should be isolated by a few thousand ohms in series with the lead connected to −T.

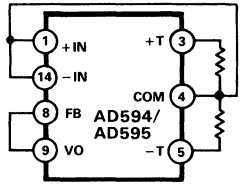

Figure 6. Decreased Sensitivity Adjustment

Changing the positive TC half of the differential output of the compensation scheme shifts the zero point away from 0°C. The zero can be restored by adjusting the current flow into the negative input of the feedback amplifier, the −T pin. A current into this terminal can be produced with a resistor between −C and −T to balance an increase in +T, or a resistor from −T to COM to offset a decrease in +T.

If the compensation is adjusted substantially to accommodate a different thermocouple type, its effect on the final output voltage will increase or decrease in proportion. To restore the nominal output to 10mV/°C the gain may be adjusted to match the new compensation and thermocouple input characteristics. When reducing the compensation the resistance between −T and COM automatically increases the gain to within 0.5% of the correct value. If a smaller gain is required, however, the nominal 47kΩ internal feedback resistor can be paralleled or replaced with an external resistor.

Fine calibration adjustments will require temperature response measurements of individual devices to assure accuracy. Major reconfigurations for other thermocouple types can be achieved without seriously compromising initial calibration accuracy, so long as the procedure is done at a fixed temperature using the factory calibration as a reference. It should be noted that intermediate recalibration conditions may require the use of a negative supply. An example using a type E thermocouple and an AD594 is given on the next page.

EXAMPLE: TYPE E RECALIBRATION – AD594/AD595

Both the AD594 and AD595 can be configured to condition the output of a type E (chromel-constantan) thermocouple. Temperature characteristics of type E thermocouples differ less from type J, than from type K, therefore the AD594 is preferred for recalibration.

While maintaining the device at a constant temperature follow the recalibration steps given here. First, measure the device temperature by tying both inputs to common (or a selected common mode potential) and connecting FB to V_O. The AD594 is now in the stand alone Celsius thermometer mode. For this example assume the ambient is 24°C and the initial output V_O is 240mV. Check the output at V_O to verify that it corresponds to the temperature of the device.

Next, measure the voltage −T at pin 5 with a high impedance DVM (capacitance should be isolated by a few thousand ohms of resistance at the measured terminals). At 24°C the −T voltage will be about 8.3mV. To adjust the compensation of an AD594 to a type E thermocouple a resistor, R1, should be connected between +T and +C, pins 2 and 3, to raise the voltage at −T by the ratio of thermocouple sensitivities. The ratio for converting a type J device to a type E characteristic is:

$$r\,(AD594) = (60.9\mu V/°C)/(51.7\mu V/°C) = 1.18$$

Thus, multiply the initial voltage measured at −T by r and experimentally determine the R1 value required to raise −T to that level. For the example the new −T voltage should be about 9.8mV. The resistance value should be approximately 1.8kΩ.

The zero differential point must now be shifted back to 0°C. This is accomplished by multiplying the original output voltage V_O by r and adjusting the measured output voltage to this value by experimentally adding a resistor, R2, between −C and −T, pins 5 and 6. The target output value in this case should be about 283mV. The resistance value of R2 should be approximately 240kΩ.

Finally, the gain must be recalibrated such that the output V_O indicates the device's temperature once again. Do this by adding a third resistor, R3, between FB and −T, pins 8 and 5. V_O should now be back to the initial 240mV reading. The resistance value of R3 should be approximately 280kΩ. The final connection diagram is shown in Figure 7. An approximate verification of the effectiveness of recalibration is to measure the differential gain to the output. For type E it should be 164.2.

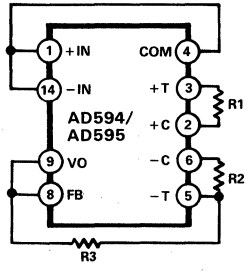

Figure 7. Type E Recalibration

When implementing a similar recalibration procedure for the AD595 the values for R1, R2, R3 and r will be approximately 650Ω, 84kΩ, 93kΩ and 1.51, respectively. Power consumption will increase by about 50% when using the AD595 with type E inputs.

Note that during this procedure it is crucial to maintain the AD594/AD595 at a stable temperature because it is used as the temperature reference. Contact with fingers or any tools not at ambient temperature will quickly produce errors. Radiational heating from a change in lighting or approach of a soldering iron must also be guarded against.

USING TYPE T THERMOCOUPLES WITH THE AD595

Because of the similarity of thermal EMFs in the 0 to 50°C range between type K and type T thermocouples, the AD595 can be directly used with both types of inputs. Within this ambient temperature range the AD595 should exhibit no more than an additional 0.2°C output calibration error when used with type T inputs. The error arises because the ice point compensator is trimmed to type K characteristics at 25°C. To calculate the AD595 output values over the recommended −200 to 350°C range for type T thermocouples, simply use the ANSI thermocouple voltages referred to 0°C and the output equation given on page 3 for the AD595. Because of the relatively large nonlinearities associated with type T thermocouples the output will deviate widely from the nominal 10mV/°C. However, cold junction compensation over the rated 0 to 50°C ambient will remain accurate.

STABILITY OVER TEMPERATURE

Each AD594/AD595 is tested for error over temperature with the measuring thermocouple at 0°C. The combined effects of cold junction compensation error, amplifier offset drift and gain error determine the stability of the AD594/AD595 output over the rated ambient temperature range. Figure 8 shows an AD594/AD595 drift error envelope. The slope of this figure has units of °C/°C.

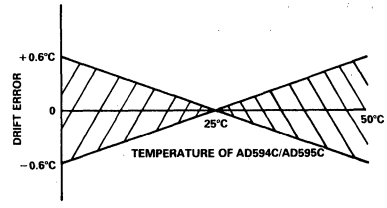

Figure 8. Drift Error vs. Temperature

THERMAL ENVIRONMENT EFFECTS

The inherent low power dissipation of the AD594/AD595 and the low thermal resistance of the package make self-heating errors almost negligible. For example, in still air the chip to ambient thermal resistance is about 80°C/watt (for the D package). At the nominal dissipation of 800μW the self-heating in free air is less than 0.065°C. Submerged in fluorinert liquid (unstirred) the thermal resistance is about 40°C/watt, resulting in a self-heating error of about 0.032°C.

SET-POINT CONTROLLER

The AD594/AD595 can readily be connected as a set-point controller as shown in Figure 9.

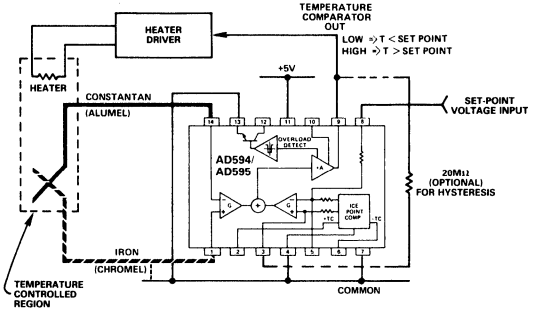

Figure 9. Set-Point Controller

The thermocouple is used to sense the unknown temperature and provide a thermal EMF to the input of the AD594/AD595. The signal is cold junction compensated, amplified to 10mV/°C and compared to an external set-point voltage applied by the user to the feedback at pin 8. Table I lists the correspondence between set-point voltage and temperature, accounting for the nonlinearity of the measurement thermocouple. If the set-point temperature range is within the operating range (−55°C to +125°C) of the AD594/AD595, the chip can be used as the transducer for the circuit by shorting the inputs together and utilizing the nominal calibration of 10mV/°C. This is the centigrade thermometer configuration as shown in Figure 13.

In operation if the set-point voltage is above the voltage corresponding to the temperature being measured the output swings low to approximately zero volts. Conversely, when the temperature rises above the set-point voltage the output switches to the positive limit of about 4 volts with a +5V supply. Figure 9 shows the set-point comparator configuration complete with a heater element driver circuit being controlled by the AD594/AD595 toggled output. Hysteresis can be introduced by injecting a current into the positive input of the feedback amplifier when the output is toggled high. With an AD594 about 200nA into the +T terminal provides 1°C of hysteresis. When using a single 5V supply with an AD594, a 20MΩ resistor from V_O to +T will supply the 200nA of current when the output is forced high (about 4V). To widen the hysteresis band decrease the resistance connected from V_O to +T.

ALARM CIRCUIT

In all applications of the AD594/AD595 the −ALM connection, pin 13, should be constrained so that it is not more positive than (V+) − 4V. This can be most easily achieved by connecting pin 13 to either common at pin 4 or V− at pin 7. For most applications that use the alarm signal, pin 13 will be grounded and the signal will be taken from +ALM on pin 12. A typical application is shown in Figure 10.

In this configuration the alarm transistor will be off in normal operation and the 20k pull up will cause the +ALM output on pin 12 to go high. If one or both of the thermocouple leads are interrupted, the +ALM pin will be driven low. As shown in Figure 10 this signal is compatible with the input of a TTL gate which can be used as a buffer and/or inverter.

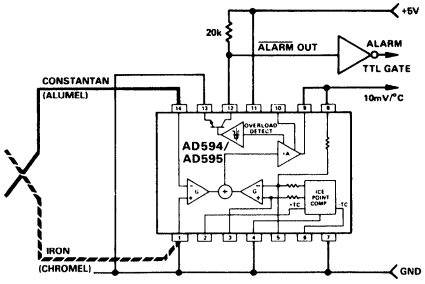

Figure 10. Using the Alarm to Drive a TTL Gate ("Grounded" Emitter Configuration)

Since the alarm is a high level output it may be used to directly drive an LED or other indicator as shown in Figure 11.

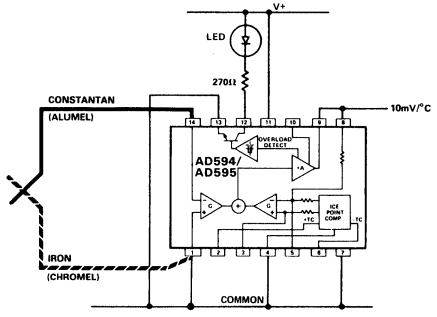

Figure 11. Alarm Directly Drives LED

A 270Ω series resistor will limit current in the LED to 10mA, but may be omitted since the alarm output transistor is current limited at about 20mA. The transistor, however, will operate in a high dissipation mode and the temperature of the circuit will rise well above ambient. Note that the cold junction compensation will be affected whenever the alarm circuit is activated. The time required for the chip to return to ambient temperature will depend on the power dissipation of the alarm circuit, the nature of the thermal path to the environment and the alarm duration.

The alarm can be used with both single and dual supplies. It can be operated above or below ground. The collector and emitter of the output transistor can be used in any normal switch configuration. As an example a negative referenced load can be driven from −ALM as shown in Figure 12.

The collector (+ALM) should not be allowed to become more positive than (V−) +36V, however, it may be permitted to be more positive than V+. The emitter voltage (−ALM) should be constrained so that it does not become more positive than 4 volts below the V+ applied to the circuit.

Additionally, the AD594/AD595 can be configured to produce an extreme upscale or downscale output in applications where an extra signal line for an alarm is inappropriate. By tying either of the thermocouple inputs to common most runaway control conditions can be automatically avoided. A +IN to common connection creates a downscale output if the thermocouple opens, while connecting −IN to common provides an upscale output.

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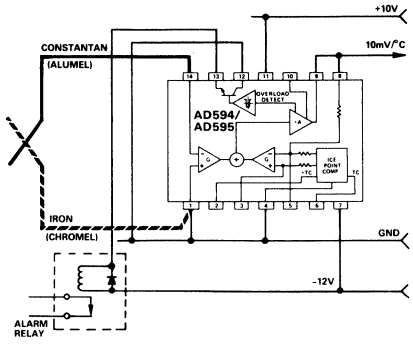


Figure 12. –ALM Driving A Negative Referenced Load

CELSIUS THERMOMETER

The AD594/AD595 may be configured as a stand-alone celsius thermometer as shown in Figure 13.

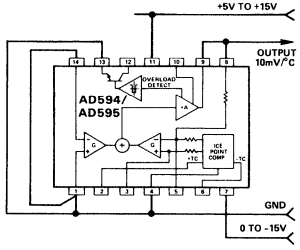


Figure 13. AD594/AD595 as a Stand-Alone Celsius Thermometer

Simply omit the thermocouple and connect the inputs (pins 1 and 14) to common. The output now will reflect the compensation voltage and hence will indicate the AD594/AD595 temperature with a scale factor of 10mV/°C. In this three terminal, voltage output, temperature sensing mode, the AD594/AD595 will operate over the full military −55°C to +125°C temperature range.

THERMOCOUPLE BASICS

Thermocouples are economical and rugged; they have reasonably good long-term stability. Because of their small size, they respond quickly and are good choices where fast response is important. They function over temperature ranges from cryogenics to jet-engine exhaust and have reasonable linearity and accuracy.

Because the number of free electrons in a piece of metal depends on both temperature and composition of the metal, two pieces of dissimilar metal in isothermal contact will exhibit a potential difference that is a repeatable function of temperature, as shown in Figure 14. The resulting voltage depends on the temperatures, T1 and T2, in a repeatable way.

Since the thermocouple is basically a differential rather than absolute measuring device, a known reference temperature is required for one of the junctions if the temperature of the other is to be inferred from the output voltage. Thermocouples made of specially selected materials have been exhaustively characterized in terms of voltage versus temperature compared to primary temperature standards. Most notably the water-ice point of 0°C is used for tables of standard thermocouple performance.

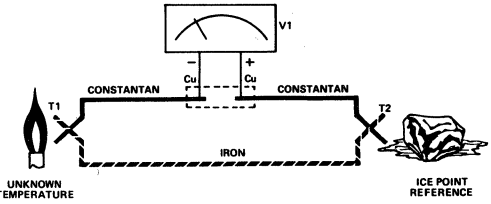


Figure 14. Thermocouple Voltage with 0°C Reference

An alternative measurement technique, illustrated in Figure 15, is used in most practical applications where accuracy requirements do not warrant maintenance of primary standards. The reference junction temperature is allowed to change with the environment

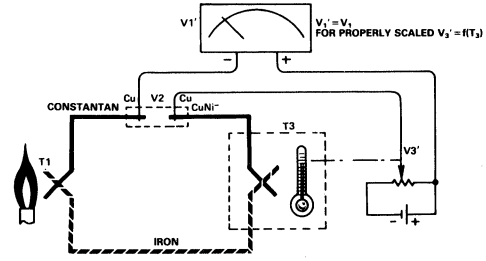


Figure 15. Substitution of Measured Reference Temperature for Ice Point Reference

of the measurement system, but it is carefully measured by some type of absolute thermometer. A measurement of the thermocouple voltage combined with a knowledge of the reference temperature can be used to calculate the measurement junction temperature. Usual practice, however, is to use a convenient thermoelectric method to measure the reference temperature and to arrange its output voltage so that it corresponds to a thermocouple referred to 0°C. This voltage is simply added to the thermocouple voltage and the sum then corresponds to the standard voltage tabulated for an ice-point referenced thermocouple.

The temperature sensitivity of silicon integrated circuit transistors is quite predictable and repeatable. This sensitivity is exploited in the AD594/AD595 to produce a temperature related voltage to compensate the reference or "cold" junction of a thermocouple as shown in Figure 16.

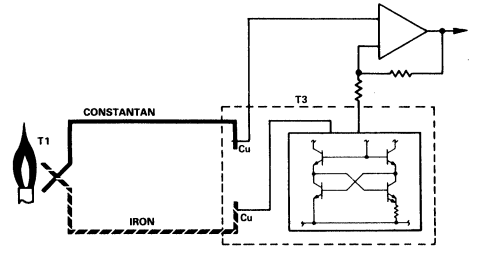


Figure 16. Connecting Isothermal Junctions

Since the compensation is at the reference junction temperature, it is often convenient to form the reference "junction" by connecting directly to the circuit wiring. So long as these connections and the compensation are at the same temperature no error will result.

Thermocouple Conditioner and Set-Point Controller

AD596*/AD597*

FEATURES
Low Cost
Operates with Type J (AD596) or Type K (AD597) Thermocouples
Built-in Ice Point Compensation
Temperature Proportional Operation – 10mV/°C
Temperature Set-Point Operation – ON/OFF
Programmable Switching Hysteresis
High Impedance Differential Input

PRODUCT DESCRIPTION

The AD596/AD597 is a monolithic temperature set-point controller which has been optimized for use at elevated temperatures such as those found in oven control applications. The device cold junction compensates and amplifies a type J or K thermocouple input to derive an internal signal proportional to temperature. The internal signal is then compared with an externally applied set-point voltage to yield a low impedance switched output voltage. Dead-Band or switching hysteresis can be programmed using a single external resistor. Alternately, the AD596/AD597 can be configured to provide a voltage output (10mV/°C) directly from a type J or K thermocouple signal. It can also be used as a stand-alone voltage output temperature sensor.

The AD596/AD597 can be powered with a single supply from +5V to +30V, or dual supplies up to a total span of 36V. Typical quiescent supply current is 160μA which minimizes self-heating errors.

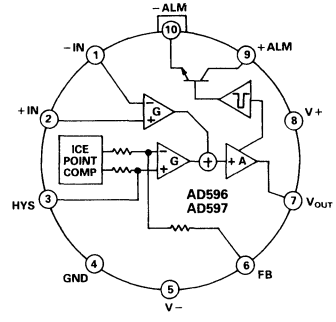
The AD596/AD597 H package option includes a thermocouple failure alarm that indicates an open thermocouple lead when operated in the temperature proportional measurement mode. The alarm output has a flexible format which can be used to drive relays, LEDs or TTL logic.

The device is packaged in a reliability qualified, cost effective 10-pin metal can, 8-pin plastic minidip or SOIC and is trimmed to operate over an ambient temperature range from +25°C to +100°C. Operation over an extended ambient temperature range is possible with slightly reduced accuracy. The AD596 will amplify thermocouple signals covering the entire −200°C to +760°C temperature range recommended for type J thermocouples while the AD597 can accommodate −200°C to +1250°C type K inputs.

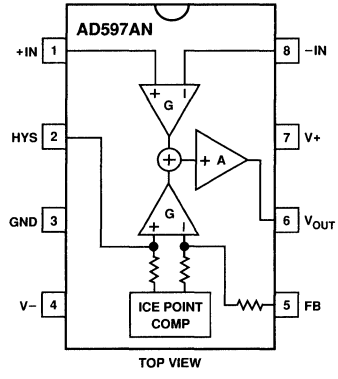
The AD596/AD597 has a calibration accuracy of ±4°C at an ambient temperature of 60°C and an ambient temperature stability specification of 0.05°C/°C from +25°C to +100°C. If higher accuracy, or a lower ambient operating temperature is required, either the AD594 (J thermocouple) or AD595 (K thermocouple) should be considered.

FUNCTIONAL BLOCK DIAGRAMS

TO-100
(H) Package



8-Pin Plastic Mini-DIP (N) Package
or SOIC (R) Package



PRODUCT HIGHLIGHTS

1. The AD596/AD597 provides cold junction compensation and a high gain amplifier which can be used as a set-point comparator.
2. The input stage of the AD596/AD597 is a high quality instrumentation amplifier that allows the thermocouple to float over most of the supply voltage range.
3. Linearization not required for thermocouple temperatures close to 175°C (+100°C to +540°C for AD596).
4. Cold junction compensation is optimized for ambient temperatures ranging from +25°C to +100°C.
5. In the stand-alone mode, the AD596/AD597 produces an output voltage that indicates its own temperature.

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*Protected by U.S. Patent No. 4,029,974.

AD596/AD597—SPECIFICATIONS (@ +60°C and V_S = 10V, Type J (AD596), Type K (AD597) Thermocouple, unless otherwise noted)

Model	AD596AH			AD597AH			AD597AN/AR			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS										
$+V_S$ to $-V_S$			36			36			36	Volts
Common-Mode Input Voltage	$(-V_S -0.15)$		$+V_S$	$(-V_S -0.15)$		$+V_S$	$(-V_S -0.15)$		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages										
+ALM	$-V_S$		$(-V_S +36)$	$-V_S$		$(-V_S +36)$	$-V_S$		$(-V_S +36)$	Volts
−ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	−55		+125	−55		+125	−40		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			Indefinite			
TEMPERATURE MEASUREMENT										
(Specified Temperature Range +25°C to +100°C)										
Calibration Error[1]	**−4**		**+4**	**−4**		**+4**	**−4**		**+4**	°C
Stability vs. Temperature[2]		±0.02	±0.05		±0.02	±0.05		±0.02	±0.05	°C/°C
Gain Error	**−1.5**		**+1.5**	**−1.5**		**+1.5**	**−1.5**		**+1.5**	%
Nominal Transfer Function		10			10			10		mV/°C
AMPLIFIER CHARACTERISTICS										
Closed Loop Gain[3]		180.6			245.5			245.5		V/V
Input Offset Voltage		°C×53.21+235			°C×41.27−37			°C×41.27−37		µV
Input Bias Current		0.1			0.1			0.1		µA
Differential Input Range	−10		+50	−10		+50	−10		+50	mV
Common Mode Range	$(-V_S-0.15)$		$(+V_S-4)$	$(+V_S-0.15)$		$(+V_S-4)$	$(-V_S-0.15)$		$(+V_S-4)$	Volts
Common Mode Sensitivity–RTO			**10**			**10**			**10**	mV/V
Power Supply Sensitivity–RTO		1	**10**		1	**10**		1	**10**	mV/V
Output Voltage Range										
Dual Supplies	**$(-V_S+2.5)$**		**$(+V_S-2)$**	**$(-V_S+2.5)$**		**$(+V_S-2)$**	**$(-V_S+2.5)$**		**$(+V_S-2)$**	Volts
Single Supply	**0**		**$(+V_S-2)$**	**0**		**$(+V_S-2)$**	**0**		**$(+V_S-2)$**	Volts
Usable Output Current[4]	±5			±5			±5			mA
3dB Bandwidth		15			15			15		kHz
ALARM CHARACTERISTICS[5]							Alarm Function Not Pinned Out			
$V_{CE(SAT)}$ at 2mA		0.3			0.3					Volts
Leakage Current			**±1**			**±1**				µA
Operating Voltage at −ALM			**$(+V_S-4)$**			**$(+V_S-4)$**				Volts
Short Circuit Current		20			20					mA
POWER REQUIREMENTS										
Operating		$(+V_S$ to $-V_S)\leq 30$			$(+V_S$ to $-V_S)\leq 30$			$(+V_S$ to $-V_S)\leq 30$		Volts
Quiescent Current										
$+V_S$		160	**300**		160	**300**		160	**300**	µA
$-V_S$		100	**200**		100	**200**		100	**200**	µA

NOTES

[1]This is a measure of the deviation from ideal with a measuring thermocouple junction of 175°C and a chip temperature of 60°C. The ideal transfer function is given by:

AD596: V_{OUT} = 180.57×(V_m-V_a+ (ambient in °C)×53.21µV/°C +235µV)

AD597: V_{OUT} = 245.46×(V_m-V_a+ (ambient in °C)×41.27µV/°C −37µV)

where V_m and V_a represent the measuring and ambient temperatures and are taken from the appropriate J or K thermocouple table. The ideal transfer function minimizes the error over the ambient temperature range of 25°C to 100°C with a thermocouple temperature of approximately 175°C.

[2]Defined as the slope of the line connecting the AD596/AD597 CJC errors measured at 25°C and 100°C ambient temperature.

[3]Pin 6 shorted to pin 7.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50kΩ resistor at output voltages below 2.5V.

[5]Alarm function available on H package option only.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model	Package Description	Package Option[1]
AD596AH	TO-100	H-10A
AD597AH	TO-100	H-10A
AD597AN[2]	Plastic DIP	N-8
AD597AR[2]	SOIC	R-8

NOTES

[1]For outline information see Package Information section.

[2]Consult factory for availability.

Thermocouple Temperature °C	Type J Voltage mV	AD596 Output mV	Type K Voltage mV	AD597 Output mV	Thermocouple Temperature °C	Type J Voltage mV	AD596 Output mV	Type K Voltage mV	AD597 Output mV
− 200	− 7.890	−1370	− 5.891	−1446	500	27.388	5000	20.640	5066
− 180	− 7.402	−1282	− 5.550	−1362	520	28.511	5203	21.493	5276
− 160	− 6.821	−1177	− 5.141	−1262	540	29.642	5407	22.346	5485
− 140	− 6.159	−1058	− 4.669	−1146	560	30.782	5613	23.198	5694
− 120	− 5.426	− 925	− 4.138	−1016	580	31.933	5821	24.050	5903
− 100	− 4.632	− 782	− 3.553	− 872	600	33.096	6031	24.902	6112
− 80	− 3.785	− 629	− 2.920	− 717	620	34.273	6243	25.751	6321
− 60	− 2.892	− 468	− 2.243	− 551	640	35.464	6458	26.599	6529
− 40	− 1.960	− 299	− 1.527	− 375	660	36.671	6676	27.445	6737
− 20	− .995	− 125	− .777	− 191	680	37.893	6897	28.288	6944
− 10	− .501	− 36	− .392	− 96	700	39.130	7120	29.128	7150
0	0	54	0	0	720	40.382	7346	29.965	7355
10	.507	146	.397	97	740	41.647	7575	30.799	7560
20	1.019	238	.798	196	750	42.283	7689	31.214	7662
25	1.277	285	1.000	245	760	–	–	31.629	7764
30	1.536	332	1.203	295	780	–	–	32.455	7966
40	2.058	426	1.611	395	800	–	–	33.277	8168
50	2.585	521	2.022	496	820	–	–	34.095	8369
60	3.115	617	2.436	598	840	–	–	34.909	8569
80	4.186	810	3.266	802	860	–	–	35.718	8767
100	5.268	1006	4.095	1005	880	–	–	36.524	8965
120	6.359	1203	4.919	1207	900	–	–	37.325	9162
140	7.457	1401	5.733	1407	920	–	–	38.122	9357
160	8.560	1600	6.539	1605	940	–	–	38.915	9552
180	9.667	1800	7.338	1801	960	–	–	39.703	9745
200	10.777	2000	8.137	1997	980	–	–	40.488	9938
220	11.887	2201	8.938	2194	1000	–	–	41.269	10130
240	12.998	2401	9.745	2392	1020	–	–	42.045	10320
260	14.108	2602	10.560	2592	1040	–	–	42.817	10510
280	15.217	2802	11.381	2794	1060	–	–	43.585	10698
300	16.325	3002	12.207	2996	1080	–	–	44.439	10908
320	17.432	3202	13.039	3201	1100	–	–	45.108	11072
340	18.537	3402	13.874	3406	1120	–	–	45.863	11258
360	19.640	3601	14.712	3611	1140	–	–	46.612	11441
380	20.743	3800	15.552	3817	1160	–	–	47.356	11624
400	21.846	3999	16.395	4024	1180	–	–	48.095	11805
420	22.949	4198	17.241	4232	1200	–	–	48.828	11985
440	24.054	4398	18.088	4440	1220	–	–	49.555	12164
460	25.161	4598	18.938	4649	1240	–	–	50.276	12341
480	26.272	4798	19.788	4857	1250	–	–	50.633	12428

Table I. Output Voltage vs. Thermocouple Temperature (Ambient +60°C, V_S = −5V, +15V)

10

TEMPERATURE PROPORTIONAL OUTPUT MODE

The AD596/AD597 can be used to generate a temperature proportional output of 10mV/°C when operated with J and K type thermocouples as shown in Figure 1. Thermocouples produce low level output voltages which are a function of both the temperature being measured and the reference or cold junction temperature. The AD596/AD597 compensates for the cold junction temperature and amplifies the thermocouple signal to produce a high level 10mV/°C voltage output which is a function only of the temperature being measured. The temperature stability of the part indicates the sensitivity of the output voltage to changes in ambient or device temperatures. This is typically 0.02°C/°C over the +25°C to +100°C recommended ambient temperature range. The parts will operate over the extended ambient temperature ranges from −55°C to +125°C, but thermocouple nonlinearity at the reference junction will degrade the temperature stability over this extended range. Table I is a list of ideal AD596/AD597 output voltages as a function of Celsius temperature for type J and K ANSI standard thermocouples with package and reference junction at 60°C. As is normally the case, these outputs

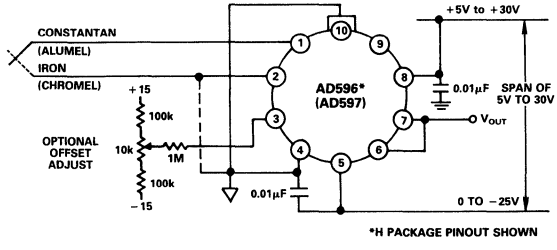

Figure 1. Temperature Proportional Output Connection

are subject to calibration and temperature sensitivity errors. These tables are derived using the ideal transfer functions:

AD596 output = (Type J voltage +301.5µV) × 180.57
AD597 output = (Type K voltage) × 245.46

The offsets and gains of these devices have been laser trimmed to closely approximate thermocouple characteristics over measurement temperature ranges centered around 175°C with the

AD596/AD597 at an ambient temperature between 25°C and 100°C. This eliminates the need for additional gain or offset adjustments to make the output voltage read:

V_{OUT} = 10mV/°C × (thermocouple temperature in °C) (within specified tolerances).

Excluding calibration errors, the above transfer function is accurate to within 1°C from +80°C to +550°C for the AD596 and −20°C to +350°C for the AD597. The different temperature ranges are due to the differences in J and K type thermocouple curves.

European DIN FE-CuNi thermocouple vary slightly from ANSI type J thermocouples. Table I does not apply when these types of thermocouples are used. The transfer functions given previously and a thermocouple table should be used instead.

Figure 1 also shows an optional trimming network which can be used to change the device's offset voltage. Injecting or sinking 200nA from Pin 3 will offset the output aproximately 10mV (1°C).

The AD596/AD597 can operate from a single supply from 5V to 36V or from split supplies totalling 36V or less as shown. Since the output can only swing to within 2V of the positive supply, the usable measurement temperature range will be restricted when positive supplies less than 15V for the AD597 and 10V for the AD596 are used. If the AD596/AD597 is to be used to indicate negative Celsius temperatures, then a negative supply is required.

Common-mode voltages on the thermocouple inputs must remain within the common-mode voltage range of the AD596/AD597, with a return path provided for the bias currents. If the thermocouple is not remotely grounded, then the dotted line connection shown in Figure 1 must be made to one of the thermocouple inputs. If there is no return path for the bias currents, the input stage will saturate, causing erroneous output voltages.

In this configuration, the AD596/AD597 H package option has circuitry which detects the presence of an open thermocouple. If the thermocouple loop becomes open, one or both of the inputs to the device will be deprived of bias current causing the output to saturate. It is this saturation which is detected internally and used to activate the alarm circuitry. The output of this feature has a flexible format which can be used to source or sink up to 20mA of current. The collector (+ALM) should not be allowed to become more positive than ($-V_S$ +36V), however, it may be permitted to be more positive than $+V_S$. The emitter voltage (−ALM) should be constrained such that it does not become more positive than 4V below $+V_S$. If the alarm feature is not used, this pin should be connected to Pins 4 or 5 as shown in Figure 1. The alarm function is unavailable on the AN/AR package option.

SET-POINT CONTROL MODE

The AD596/AD597 can be connected as a set-point controller as shown in Figure 2. The thermocouple voltage is cold junction compensated, amplified, and compared to an external set-point voltage. The relationship between set-point voltage and temperature is given in Table I. If the temperature to be controlled is within the operating range (−55°C to +125°C) of the device, it can monitor its own temperature by shorting the inputs to ground. The set-point voltage with the thermocouple inputs grounded is given by the expressions:

AD596 Set-Point Voltage = °C × 9.6mV/°C +42mV
AD597 Set-Point Voltage = °C × 10.1mV/°C −9.1mV

The input impedance of the set-point pin of the AD596/AD597 is approximately 50kΩ. The temperature coefficient of this resistance is ±15ppm/°C. Therefore, the 100ppm/°C 5kΩ pot shown in Figure 2 will only introduce an additional ±1°C degradation of temperature stability over the +25°C to +100°C ambient temperature range.

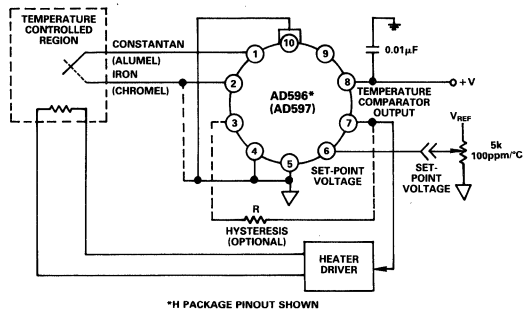

Figure 2. Set-Point Control Mode

Switching hysteresis is often used in set-point systems of this type to provide noise immunity and increase system reliability. By reducing the frequency of on-off cycling, mechanical component wear is reduced leading to enhanced system reliability. This can easily be implemented with a single external resistor between Pins 7 and 3 of the AD596/AD597. Each 200nA of current injected into Pin 3 when the output switches will cause about 1°C of hysteresis; that is: $R_{HYST}\ (\Omega) = \frac{V_{OUT}}{200nA} \times \frac{1}{°C_{HYST}}$.

In the set-point configuration, the AD596/AD597 output is saturated at all times, so the alarm transistor will be ON regardless of whether there is an open circuit or not. However, −ALM must be tied to a voltage below ($+V_S$ −4V) for proper operation of the rest of the circuit.

STAND-ALONE TEMPERATURE TRANSDUCER

The AD596/AD597 may be configured as a stand-alone Celsius thermometer as shown in Figure 3.

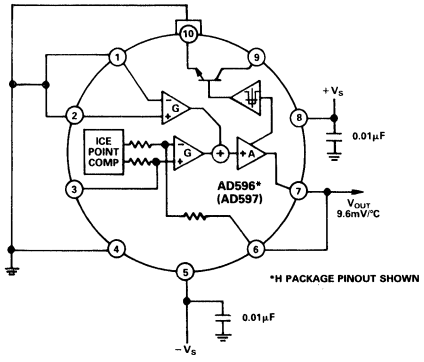

Figure 3. Stand-Alone Temperature Transducer Temperature Proportional Output Connection

Simply omit the thermocouple and connect the inputs (Pins 1 and 2) to common. The output will now reflect the compensation voltage and hence will indicate the AD596/AD597 temperature. In this three terminal, voltage output, temperature sensing mode, the AD596/AD597 will operate over the full extended −55°C to +125°C temperature range. The output scaling will be

9.6mV per °C with the AD596 and 10.1mV per °C with the AD597. Additionally there will be a 42mV offset with the AD596 causing it to read slightly high when used in this mode.

THERMOCOUPLE CONNECTIONS

The connection of the thermocouple wire and the normal wire or printed circuit board traces going to the AD596/AD597 forms an effective reference junction as shown in Figure 4. This junction must be kept at the same temperature as the AD596/AD597 for the internal cold junction compensation to work properly. Unless the AD596/AD597 is in a thermally stable enclosure, the thermocouple leads should be brought in directly to Pins 1 and 2.

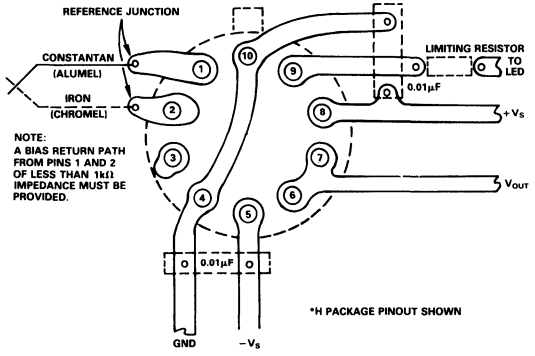

Figure 4. PCB Connections

To ensure secure bonding, the thermocouple wire should be cleaned to remove oxidization prior to soldering. Noncorrosive resin flux is effective with iron, constantan, chromel, and alumel, and the following solders: 95% tin–5% silver, or 90% tin–10% lead.

SINGLE AND DUAL SUPPLY CONNECTIONS

In the single supply configuration as used in the set-point controller of Figure 2, any convenient voltage from +5V to +36V may be used, with self-heating errors being minimized at lower supply levels. In this configuration, the $-V_S$ connection at Pin 5 is tied to ground. Temperatures below zero can be accommodated in the single supply set-point mode, but not in the single supply temperature measuring mode (Figure 1 reconnected for single supply). Temperatures below zero can only be indicated by a negative output voltage, which is impossible in the single supply mode.

Common-mode voltages on the thermocouple inputs must remain below the positive supply, and not more than 0.15V more negative than the minus supply. In addition, a return path for the input bias currents must be provided. If the thermocouple is not remotely grounded, then the dotted line connections in Figures 1 and 2 are mandatory.

STABILITY OVER TEMPERATURE

The AD596/AD597 is specified for a maximum error of ±4°C at an ambient temperature of 60°C and a measuring junction temperature at 175°C. The ambient temperature stability is specified to be a maximum of 0.05°C/°C. In other words, for every degree change in the ambient temperature, the output will change no more than 0.05 degrees. So, at 25°C the maximum deviation from the temperature-voltage characteristic of Table I is ±5.75°C, and at 100°C it is ±6°C maximum (see Figure 5). If the offset error of ±4°C is removed with a single offset adjustment, these errors will be be reduced to ±1.75°C and ±2°C max. The optional trim circuit shown in Figure 1 demonstrates how the ambient offset error can be adjusted to zero.

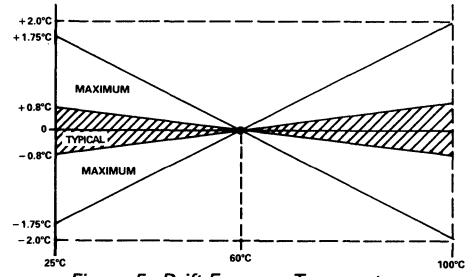

Figure 5. Drift Error vs. Temperature

THERMAL ENVIRONMENTAL EFFECTS

The inherent low power dissipation of the AD596/AD597 keeps self-heating errors to a minimum. However, device output is capable of delivering ±5mA to an external load and the alarm circuitry can supply up to 20mA. Since the typical junction to ambient thermal resistance in free air is 150°C/W, significant temperature difference between the package pins (where the reference junction is located) and the chip (where the cold junction temperature is measured and then compensated) can exist when the device is operated in a high dissipation mode. These temperature differences will result in a direct error at the output. In the temperature proportional mode, the alarm feature will only activate in the event of an open thermocouple or system transient which causes the device output to saturate. Self-Heating errors will not effect the operation of the alarm but two cases do need to be considered. First, after a fault is corrected and the alarm is reset, the AD596/AD597 must be allowed to cool before readings can again be accurate. This can take 5 minutes or more depending upon the thermal environment seen by the device. Second, the junction temperature of the part should not be allowed to exceed 150°C. If the alarm circuit of the AD596/AD597 is made to source or sink 20mA with 30V across it, the junction temperature will be 90°C above ambient causing the die temperature to exceed 150°C when ambient is above 60°C. In this case, either the load must be reduced, or a heat sink used to lower the thermal resistance.

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TEMPERATURE READOUT AND CONTROL

Figure 6 shows a complete temperature indication and control system based on the AD596/AD597. Here the AD596/AD597 is being used as a closed-loop thermocouple signal conditioner and an external op-amp is used to implement set point. This has two important advantages. It provides a high level (10mV/°C) output for the A/D panel meter and also preserves the alarm function for open thermocouples.

The A/D panel meter can easily be offset and scaled as shown to read directly in degrees Fahrenheit. If a two temperature calibration scheme is used, the dominant residual errors will arise from two sources; the ambient temperature rejection (typically ±2°C over a 25°C to 100°C range) and thermocouple nonlinearity typical +1°C from 80°C to 550°C for type J and +1°C from −20°C to 350°C for type K.

An external voltage reference is used both to increase the stability of the A/D converter and supply a stable reference for the set-point voltage.

A traditional requirement for the design of set-point control thermocouple systems has been to configure the system such that the appropriate action is taken in the event of an open thermocouple. The open thermocouple alarm pin with its flexible current-limited output format supports this function when the part operates in the temperature proportional mode. In addition, if the thermocouple is not remotely grounded, it is possible to program the device for either a positive or negative full scale output in the event of an open thermocouple. This is done by connecting the bias return resistor directly to Pin 1 if a high output voltage is desired to indicate a fault condition. Alternately, if the bias return is provided on the thermocouple lead connected to Pin 2, an open circuit will result in an output low reading. Figure 6 shows the ground return connected to Pin 1 so that if the thermocouple fails, the heater will remain off. At the same time, the alarm circuit lights the LED signalling the need to service the thermocouple. Grounding Pin 2 would lead to low output voltage saturation, and in this circuit would result in a potentially dangerous thermal runaway under fault conditions.

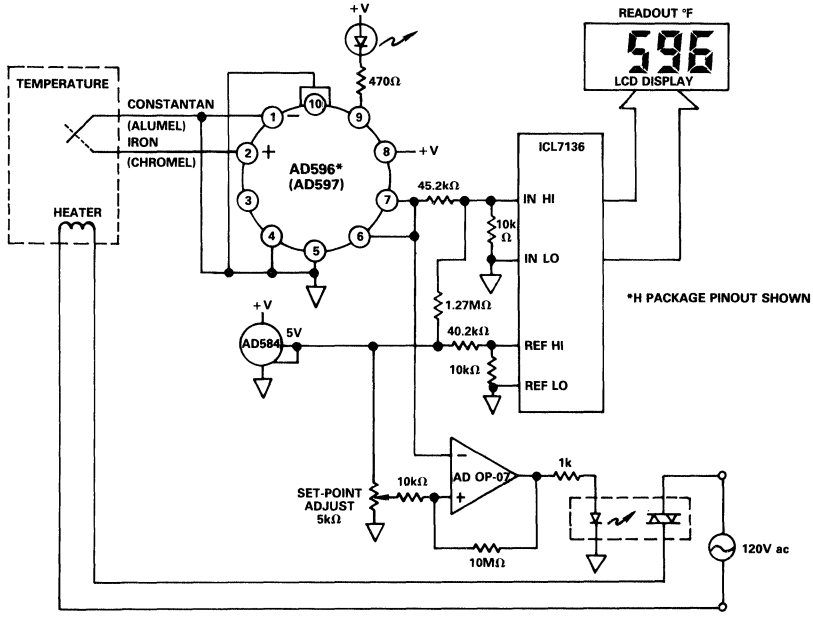


Figure 6. Temperature Measurement and Control

LVDT Signal Conditioner

AD598

FEATURES

Single Chip Solution, Contains Internal Oscillator and Voltage Reference
No Adjustments Required
Insensitive to Transducer Null Voltage
Insensitive to Primary to Secondary Phase Shifts
DC Output Proportional to Position
20 Hz to 20 kHz Frequency Range
Single or Dual Supply Operation
Unipolar or Bipolar Output
Will Operate a Remote LVDT at Up to 300 Feet
Position Output Can Drive Up to 1000 Feet of Cable
Will Also Interface to an RVDT
Outstanding Performance
Linearity: 0.05% of FS max
Output Voltage: ±11 V min
Gain Drift: 50 ppm/°C of FS max
Offset Drift: 50 ppm/°C of FS max

PRODUCT DESCRIPTION

The AD598 is a complete, monolithic Linear Variable Differential Transformer (LVDT) signal conditioning subsystem. It is used in conjunction with LVDTs to convert transducer mechanical position to a unipolar or bipolar dc voltage with a high degree of accuracy and repeatability. All circuit functions are included on the chip. With the addition of a few external passive components to set frequency and gain, the AD598 converts the raw LVDT secondary output to a scaled dc signal. The device can also be used with RVDT transducers.

The AD598 contains a low distortion sine wave oscillator to drive the LVDT primary. The LVDT secondary output consists of two sine waves that drive the AD598 directly. The AD598 operates upon the two signals, dividing their difference by their sum, producing a scaled unipolar or bipolar dc output.

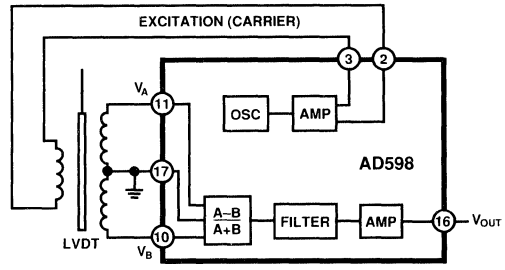
The AD598 uses a unique ratiometric architecture (patent pending) to eliminate several of the disadvantages associated with traditional approaches to LVDT interfacing. The benefits of this new circuit are: no adjustments are necessary, transformer null voltage and primary to secondary phase shift does not affect system accuracy, temperature stability is improved, and transducer interchangeinterchangeabilityability is improved.

The AD598 is available in two performance grades:

Grade	Temperature Range	Package
AD598JR	0 to +70°C	20-Pin Small Outline (SOIC)
AD598AD	−40°C to +85°C	20-Pin Ceramic DIP

It is also available processed to MIL-STD-883B, for the military range of −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD598 offers a monolithic solution to LVDT and RVDT signal conditioning problems; few extra passive components are required to complete the conversion from mechanical position to dc voltage and no adjustments are required.
2. The AD598 can be used with many different types of LVDTs because the circuit accommodates a wide range of input and output voltages and frequencies; the AD598 can drive an LVDT primary with up to 24 V rms and accept secondary input levels as low as 100 mV rms.
3. The 20 Hz to 20 kHz LVDT excitation frequency is determined by a single external capacitor. The AD598 input signal need not be synchronous with the LVDT primary drive. This means that an external primary excitation, such as the 400 Hz power mains in aircraft, can be used.
4. The AD598 uses a ratiometric decoding scheme such that primary to secondary phase shifts and transducer null voltage have absolutely no effect on overall circuit performance.
5. Multiple LVDTs can be driven by a single AD598, either in series or parallel as long as power dissipation limits are not exceeded. The excitation output is thermally protected.
6. The AD598 may be used in telemetry applications or in hostile environments where the interface electronics may be remote from the LVDT. The AD598 can drive an LVDT at the end of 300 feet of cable, since the circuit is not affected by phase shifts or absolute signal magnitudes. The position output can drive as much as 1000 feet of cable.
7. The AD598 may be used as a loop integrator in the design of simple electromechanical servo loops.

AD598—SPECIFICATIONS (typical @ +25°C and ±15 V dc, C1 = 0.015 μF, R2 = 80 kΩ, R_L = 2 kΩ, unless otherwise noted. See Figure 7.)

Model	AD598J Min	AD598J Typ	AD598J Max	AD598A Min	AD598A Typ	AD598A Max	Unit
TRANSFER FUNCTION[1]	$V_{OUT} = \frac{V_A - V_B}{V_A + V_B} \times 500\ \mu A \times R2$						V
OVERALL ERROR[2]							
T_{min} to T_{max}		0.6	2.35		0.6	1.65	% of FS
SIGNAL OUTPUT CHARACTERISTICS							
Output Voltage Range (T_{min} to T_{max})	**±11**			**±11**			V
Output Current (T_{min} to T_{max})	**8**			**6**			mA
Short Circuit Current		20			20		mA
Nonlinearity[3] (T_{min} to T_{max})		75	**±500**		75	**±500**	ppm of FS
Gain Error[4]		0.4	**±1**		0.4	**±1**	% of FS
Gain Drift		20	**±100**		20	**±50**	ppm/°C of FS
Offset[5]		0.3	**±1**		0.3	**±1**	% of FS
Offset Drift		7	**±200**		7	**±50**	ppm/°C of FS
Excitation Voltage Rejection[6]		100			100		ppm/dB
Power Supply Rejection (±12 V to ±18 V)							
PSRR Gain (T_{min} to T_{max})	**300**	100		**400**	100		ppm/V
PSRR Offset (T_{min} to T_{max})	**100**	15		**200**	15		ppm/V
Common Mode Rejection (±3 V)							
CMRR Gain (T_{min} to T_{max})	**100**	25		**200**	25		ppm/V
CMRR Offset (T_{min} to T_{max})	**100**	6		**200**	6		ppm/V
Output Ripple[7]		4			4		mV rms
EXCITATION OUTPUT CHARACTERISTICS (@ 2.5 kHz)							
Excitation Voltage Range	2.1		24	2.1		24	V rms
Excitation Voltage							
(R1 = Open)[8]	**1.2**		**2.1**	**1.2**		**2.1**	V rms
(R1 = 12.7 kΩ)[8]	**2.6**		**4.1**	**2.6**		**4.1**	V rms
(R1 = 487 Ω)[8]	**14**		**20**	**14**		**20**	V rms
Excitation Voltage TC[9]		600			600		ppm/°C
Output Current	**30**			**30**			mA rms
T_{min} to T_{max}	12			12			mA rms
Short Circuit Current		60			60		mA
DC Offset Voltage (Differential, R1 = 12.7 kΩ)							
T_{min} to T_{max}		30	**±100**		30	**±100**	mV
Frequency	20		20k	20		20k	Hz
Frequency TC, (R1 = 12.7 kΩ)		200			200		ppm/°C
Total Harmonic Distortion		−50			−50		dB
SIGNAL INPUT CHARACTERISTICS							
Signal Voltage	0.1		3.5	0.1		3.5	V rms
Input Impedance		200			200		kΩ
Input Bias Current (AIN and BIN)		1	5		1	5	μA
Signal Reference Bias Current		2	**10**		2	**10**	μA
Excitation Frequency	0		20	0		20	kHz
POWER SUPPLY REQUIREMENTS							
Operating Range	13		36	13		36	V
Dual Supply Operation (±10 V Output)	±13			±13			V
Single Supply Operation							
0 to +10 V Output	17.5			17.5			V
0 to −10 V Output	17.5			17.5			V
Current (No Load at Signal and Excitation Outputs)		12	**15**		12	**15**	mA
T_{min} to T_{max}			**16**			**18**	mA
TEMPERATURE RANGE							
JR (SOIC)	0		70				°C
AD (DIP)				−40		+85	°C
PACKAGE OPTION[10]							
SOIC (R-20)		AD598JR					
Side Brazed DIP (D-20)					AD598AD		

NOTES

[1]V_A and V_B represent the Mean Average Deviation (MAD) of the detected sine waves. Note that for this Transfer Function to linearly represent positive displacement, the sum of V_A and V_B of the LVDT must remain constant with stroke length. See "Theory of Operation." Also see Figures 7 and 12 for R2.

[2]From T_{min} to T_{max} the overall error due to the AD598 alone is determined by combining gain error, gain drift and offset drift. For example, the worst case overall error for the AD598AD from T_{min} to T_{max} is calculated as follows: overall error = gain error at +25°C (±1% full scale) + gain drift from −40°C to +25°C (50 ppm/°C of FS × +65°C) + offset drift from −40°C to +25°C (50 ppm/°C of FS× 65°C) = ±1.65% of full scale. Note that 1000 ppm of full scale equals 0.1% of full scale. Full scale is defined as the voltage difference between the maximum positive and maximum negative output.

[3]Nonlinearity of the AD598 only, in units of ppm of full scale. Nonlinearity is defined as the maximum measured deviation of the AD598 output voltage from a straight line. The straight line is determined by connecting the maximum produced full-scale negative voltage with the maximum produced full-scale positive voltage.

[4]See Transfer Function.

[5]This offset refers to the $(V_A-V_B)/(V_A+V_B)$ input spanning a full-scale range of ±1. [For $(V_A-V_B)/(V_A+V_B)$ to equal +1, V_B must equal zero volts; and correspondingly for $(V_A-V_B)/(V_A+V_B)$ to equal −1, V_A must equal zero volts. Note that offset errors do not allow accurate use of zero magnitude inputs; practical inputs are limited to 100 mV rms.] The ±1 span is a convenient reference point to define offset referred to input. For example, with this input span a value of R2 = 20 kΩ would give V_{OUT} span a value of ±10 volts. Caution, most LVDTs will typically exercise less of the $(V_A-V_B)/(V_A+V_B)$ input span and thus require a larger value of R2 to produce the ±10 V output span. In this case the offset is correspondingly magnified when referred to the output voltage. For example, a Schaevitz E100 LVDT requires 80.2 kΩ for R2 to produce a ±10.69 V output and $(V_A-V_B)/(V_A+V_B)$ equals 0.27. This ratio may be determined from the graph shown in Figure 18, $(V_A-V_B)/(V_A+V_B)$ = (1.71 V rms−0.99 V rms)/(1.71 V rms+0.99 V rms). The maximum offset value referred to the ±10.69 V output may be determined by multiplying the maximum value shown in the data sheet (±1% of FS by 1/0.27 which equals ±3.7% maximum. Similarly, to determine the maximum values of offset drift, offset CMRR and offset PSRR when referred to the ±10.69 V output, these data sheet values should also be multiplied by (1/0.27). For this example, for the AD598AD the maximum values of offset drift, PSRR offset and CMRR offset would be: 185 ppm/°C of FS; 741 ppm/V and 741 ppm/V respectively when referred to the ±10.69 V output.

[6]For example, if the excitation to the primary changes by 1 dB, the gain of the system will change by typically 100 ppm.

[7]Output ripple is a function of the AD598 bandwidth determined by C2, C3 and C4. See Figures 16 and 17.

[8]R1 is shown in Figures 7 and 12.

[9]Excitation voltage drift is not an important specification because of the ratiometric operation of the AD598.

[10]For outline information see Package Information section.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tested are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

THERMAL CHARACTERISTICS

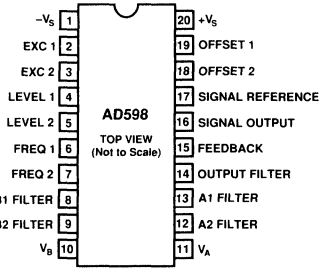
	θ_{JC}	θ_{JA}
SOIC Package	22°C/W	80°C/W
Side Brazed Package	25°C/W	85°C/W

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ . . . . . 36 V
Storage Temperature Range
R Package . . . . . −65°C to +150°C
D Package . . . . . −65°C to +150°C
Operating Temperature Range
AD598JR . . . . . 0 to +70°C
AD598AD . . . . . −40°C to +85°C
Lead Temperature Range (Soldering 60 Seconds) . . . . +300°C
Power Dissipation Up to +65°C . . . . . 1.2 W
Derates Above +65°C . . . . . 12 mW/°C

CONNECTION DIAGRAM

Plastic SOIC (R) Package
and
Side Brazed Ceramic DIP (D) Package



AD598—Typical Characteristics (at +25°C and V_S = ±15V, unless otherwise noted)

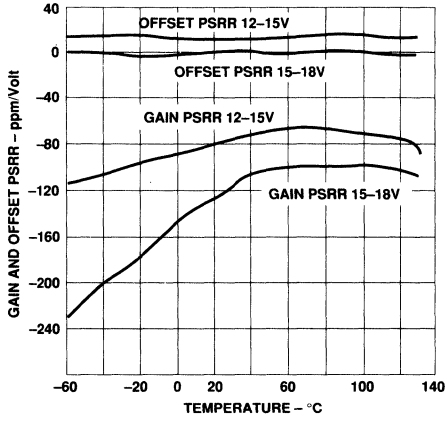


Figure 1. Gain and Offset PSRR vs. Temperature

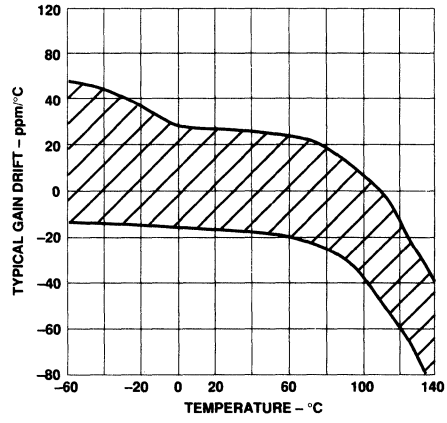


Figure 2. Typical Gain Drift vs. Temperature

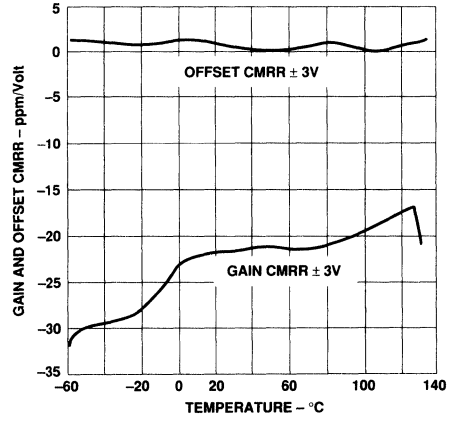


Figure 3. Gain and Offset CMRR vs. Temperature

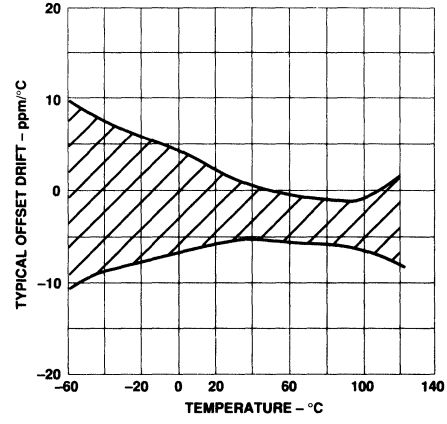


Figure 4. Typical Offset Drift vs. Temperature

THEORY OF OPERATION

A block diagram of the AD598 along with an LVDT (Linear Variable Differential Transformer) connected to its input is shown in Figure 5. The LVDT is an electromechanical transducer whose input is the mechanical displacement of a core and whose output is a pair of ac voltages proportional to core position. The transducer consists of a primary winding energized by an external sine wave reference source, two secondary windings connected in series, and the moveable core to couple flux between the primary and secondary windings.

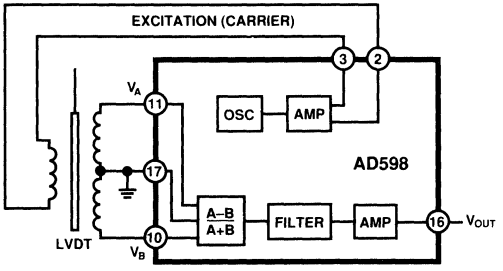


Figure 5. AD598 Functional Block Diagram

The AD598 energizes the LVDT primary, senses the LVDT secondary output voltages and produces a dc output voltage proportional to core position. The AD598 consists of a sine wave oscillator and power amplifier to drive the primary, a decoder which determines the ratio of the difference between the LVDT secondary voltages divided by their sum, a filter and an output amplifier.

The oscillator comprises a multivibrator which produces a triwave output. The triwave drives a sine shaper, which produces a low distortion sine wave whose frequency is determined by a single capacitor. Output frequency can range from 20 Hz to 20 kHz and amplitude from 2 V rms to 24 V rms. Total harmonic distortion is typically −50 dB.

The output from the LVDT secondaries consists of a pair of sine waves whose amplitude difference, (V_A-V_B), is proportional to core position. Previous LVDT conditioners synchronously detect this amplitude difference and convert its absolute value to a voltage proportional to position. This technique uses the primary excitation voltage as a phase reference to determine the polarity of the output voltage. There are a number of problems associated with this technique such as (1) producing a constant amplitude, constant frequency excitation signal, (2) compensating for LVDT primary to secondary phase shifts, and (3) compensating for these shifts as a function of temperature and frequency.

The AD598 eliminates all of these problems. The AD598 does not require a constant amplitude because it works on the ratio of the difference and sum of the LVDT output signals. A constant frequency signal is not necessary because the inputs are rectified and only the sine wave carrier magnitude is processed. There is no sensitivity to phase shift between the primary excitation and the LVDT outputs because synchronous detection is not employed. The ratiometric principle upon which the AD598 operates requires that the sum of the LVDT secondary voltages remains constant with LVDT stroke length. Although LVDT manufacturers generally do not specify the relationship between V_A+V_B and stroke length, it is recognized that some LVDTs do not meet this requirement. In these cases a nonlinearity will result. However, the majority of available LVDTs do in fact meet these requirements.

The AD598 utilizes a special decoder circuit. Referring to the block diagram and Figure 6 below, an implicit analog computing loop is employed. After rectification, the A and B signals are multiplied by complementary duty cycle signals, d and (1–d) respectively. The difference of these processed signals is integrated and sampled by a comparator. It is the output of this comparator that defines the original duty cycle, d, which is fed back to the multipliers.

As shown in Figure 6, the input to the integrator is [(A+B)d]-B. Since the integrator input is forced to 0, the duty cycle $d = B/(A+B)$.

The output comparator which produces $d = B/(A+B)$ also controls an output amplifier driven by a reference current. Duty cycle signals d and (1−d) perform separate modulations on the reference current as shown in Figure 6, which are summed. The summed current, which is the output current, is $I_{REF} \times (1-2d)$.

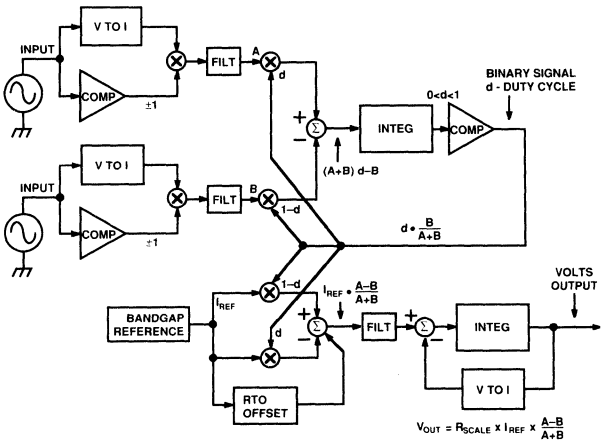


Figure 6. Block Diagram of Decoder

Since d = B/(A+B), by substitution the output current equals $I_{REF} \times (A-B)/(A+B)$. This output current is then filtered and converted to a voltage since it is forced to flow through the scaling resistor R2 such that:

$$V_{OUT} = I_{REF} \times (A-B)/(A+B) \times R2$$

CONNECTING THE AD598

The AD598 can easily be connected for dual or single supply operation as shown in Figures 7 and 12. The following general design procedures demonstrate how external component values are selected and can be used for any LVDT which meets AD598 input/output criteria.

Parameters which are set with external passive components include: excitation frequency and amplitude, AD598 system bandwidth, and the scale factor (V/inch). Additionally, there are optional features, offset null adjustment, filtering, and signal integration which can be used by adding external components.

DESIGN PROCEDURE
DUAL SUPPLY OPERATION

Figure 7 shows the connection method with dual ±15 volt power supplies and a Schaevitz E100 LVDT. This design procedure can be used to select component values for other LVDTs as well. The procedure is outlined in Steps 1 through 10 as follows:

1. Determine the mechanical bandwidth required for LVDT position measurement subsystem, $f_{SUBSYSTEM}$. For this example, assume $f_{SUBSYSTEM}$ = 250 Hz.
2. Select minimum LVDT excitation frequency, approximately 10 × $f_{SUBSYSTEM}$. Therefore, let excitation frequency = 2.5 kHz.
3. Select a suitable LVDT that will operate with an excitation frequency of 2.5 kHz. The Schaevitz E100, for instance, will operate over a range of 50 Hz to 10 kHz and is an eligible candidate for this example.
4. Determine the sum of LVDT secondary voltages V_A and V_B. Energize the LVDT at its typical drive level V_{PRI} as shown in the manufacturer's data sheet (3 V rms for the E100). Set the core displacement to its center position where $V_A = V_B$. Measure these values and compute their sum V_A+V_B. For the E100, V_A+V_B = 2.70 V rms. This calculation will be used later in determining AD598 output voltage.
5. Determine optimum LVDT excitation voltage, V_{EXC}. With the LVDT energized at its typical drive level V_{PRI}, set the core displacement to its mechanical full-scale position and measure the output V_{SEC} of whichever secondary produces the largest signal. Compute LVDT voltage transformation ratio, VTR.

   $$VTR = V_{PRI}/V_{SEC}$$

   For the E100, V_{SEC} = 1.71 V rms for V_{PRI} = 3 V rms. VTR = 1.75

   The AD598 signal input, V_{SEC}, should be in the range of 1 V rms to 3.5 V rms for maximum AD598 linearity and minimum noise susceptibility. Select V_{SEC} = 3 V rms. Therefore, LVDT excitation voltage V_{EXC} should be:

   $$V_{EXC} = V_{SEC} \times VTR = 3 \times 1.75 = 5.25\ Vrms$$

   Check the power supply voltages by verifying that the peak values of V_A and V_B are at least 2.5 volts less than the voltages at $+V_S$ and $-V_S$.
6. Referring to Figure 7, for V_S = ±15 V, select the value of the amplitude determining component R1 as shown by the curve in Figure 8.
7. Select excitation frequency determining component C1.

   $$C1 = 35\ \mu F\ Hz/f_{EXCITATION}$$

8. C2, C3 and C4 are a function of the desired bandwidth of the AD598 position measurement subsystem. They should be nominally equal values.

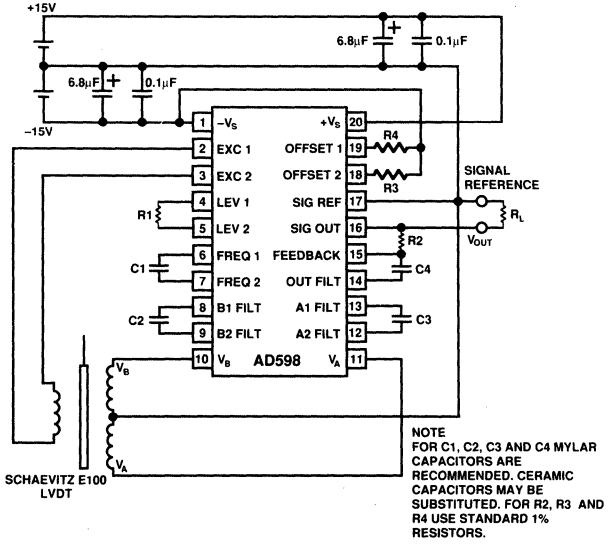


Figure 7. Interconnection Diagram for Dual Supply Operation

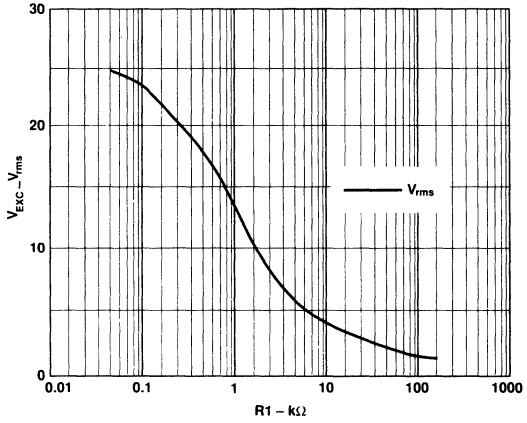


Figure 8. Excitation Voltage V_{EXC} vs. R1

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/f_{SUBSYSTEM}\ (Hz)$$

If the desired system bandwidth is 250 Hz, then

$$C2 = C3 = C4 = 10^{-4}\ Farad\ Hz/250\ Hz = 0.4\ \mu F$$

See Figures 13, 14 and 15 for more information about AD598 bandwidth and phase characterization.

9. In order to Compute R2, which sets the AD598 gain or full-scale output range, several pieces of information are needed:
   a. LVDT sensitivity, S
   b. Full-scale core displacement, d
   c. Ratio of manufacturer recommended primary drive level, V_{PRI}, to $(V_A + V_B)$ computed in Step 4.

   LVDT sensitivity is listed in the LVDT manufacturer's catalog and has units of millivolts output per volts input per inch displacement. The E100 has a sensitivity of 2.4 mV/V/mil. In the event that LVDT sensitivity is not given by the manufacturer, it can be computed. See section on Determining LVDT Sensitivity.

   For a full-scale displacement of d inches, voltage out of the AD598 is computed as

$$V_{OUT} = S \times \left[\frac{V_{PRI}}{(V_A + V_B)}\right] \times 500\mu A \times R2 \times d.$$

   V_{OUT} is measured with respect to the signal reference, Pin 17 shown in Figure 7.

   Solving for R2,

$$R2 = \frac{V_{OUT} \times (V_A + V_B)}{S \times V_{PRI} \times 500\ \mu A \times d} \qquad (1)$$

   Note that V_{PRI} is the same signal level used in Step 4 to determine $(V_A + V_B)$

   For V_{OUT} = 20 V full-scale range (±10 V) and d = 0.2 inch full-scale displacement (±0.1 inch),

$$R2 = \frac{20\ V \times 2.70\ V}{2.4 \times 3 \times 500\ \mu A \times 0.2} = 75.3\ k\Omega$$

   V_{OUT} as a function of displacement for the above example is shown in Figure 9.

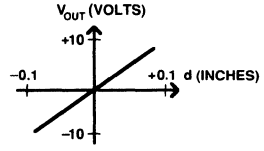


Figure 9. V_{OUT} (±10 V Full Scale) vs. Core Displacement (±0.1 Inch)

10. Selections of R3 and R4 permit a positive or negative output voltage offset adjustment.

$$V_{OS} = 1.2\ V \times R2 \times \left(\frac{1}{R3 + 5\ k\Omega^*} - \frac{1}{R4 + 5\ k\Omega^*}\right) \qquad (2)$$

*These values have a ±20% tolerance.

For no offset adjustment R3 and R4 should be open circuit.

To design a circuit producing a 0 to +10 V output for a displacement of ±0.1 inch, set V_{OUT} to +10 V, d = 0.2 inch and solve Equation (1) for R2.

$$R2 = 37.6\ k\Omega$$

This will produce a response shown in Figure 10.

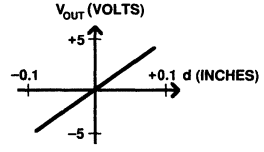


Figure 10. V_{OUT} (±5 V Full Scale) vs. Core Displacement (±0.1 Inch)

In Equation (2) set V_{OS} = 5 V and solve for R3 and R4. Since a positive offset is desired, let R4 be open circuit.

Rearranging Equation (2) and solving for R3

$$R3 = \frac{1.2 \times R2}{V_{OS}} - 5\ k\Omega = 4.02\ k\Omega$$

Figure 11 shows the desired response.

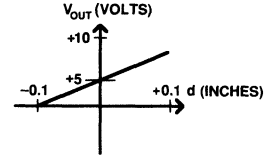


Figure 11. V_{OUT} (0–10 V Full Scale) vs. Displacement (±0.1 Inch)

10

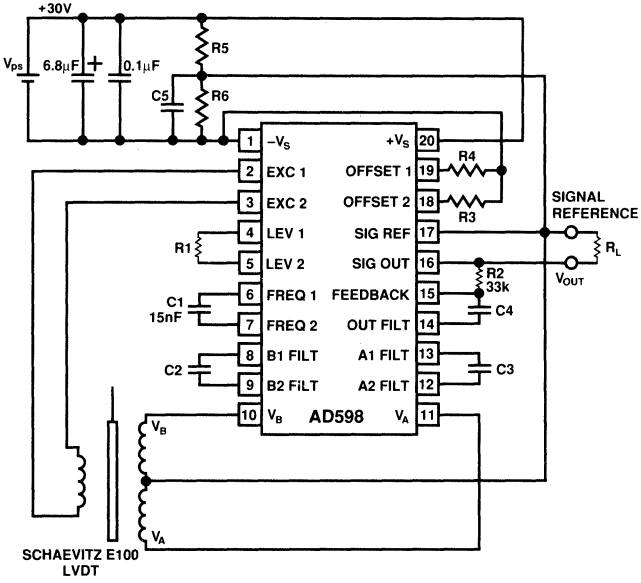


Figure 12. Interconnection Diagram for Single Supply Operation

DESIGN PROCEDURE
SINGLE SUPPLY OPERATION

Figure 12 shows the single supply connection method.

For single supply operation, repeat Steps 1 through 10 of the design procedure for dual supply operation, then complete the additional Steps 11 through 14 below. R5, R6 and C5 are additional component values to be determined. V_{OUT} is measured with respect to SIGNAL REFERENCE.

11. Compute a maximum value of R5 and R6 based upon the relationship

$$R5 + R6 \leq V_{PS}/100\ \mu A$$

12. The voltage drop across R5 must be greater than

$$2 + 10\ k\Omega^{\star}\left(\frac{1.2\ V}{R4 + 5\ k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2}\right)\ Volts$$

Therefore

$$R5 \geq \frac{2 + 10\ k\Omega^{\star}\left(\frac{1.2\ V}{R4 + 5\ k\Omega} + 250\ \mu A + \frac{V_{OUT}}{4 \times R2}\right)}{100\ \mu A}\ Ohms$$

*These values have ±20% tolerance.

Based upon the constraints of R5 + R6 (Step 11) and R5 (Step 12), select an interim value of R6.

13. Load current through R_L returns to the junction of R5 and R6, and flows back to V_{PS}. Under maximum load conditions, make sure the voltage drop across R5 is met as defined in Step 12.

    As a final check on the power supply voltages, verify that the peak values of V_A and V_B are at least 2.5 volts less than the voltages at $+V_S$ and $-V_S$.

14. C5 is a bypass capacitor in the range of 0.1 μF to 1 μF.

Gain Phase Characteristics

To use an LVDT in a closed loop mechanical servo application, it is necessary to know the dynamic characteristics of the transducer and interface elements. The transducer itself is very quick to respond once the core is moved. The dynamics arise primarily from the interface electronics. Figures 13, 14 and 15 show the frequency response of the AD598 LVDT Signal Conditioner. Note that Figures 14 and 15 are basically the same; the difference is frequency range covered. Figure 14 shows a wider range of mechanical input frequencies at the expense of accuracy. Figure 15 shows a more limited frequency range with

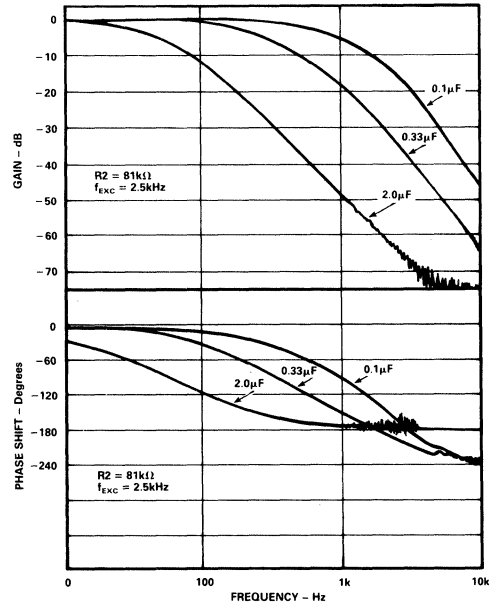


Figure 13. Gain and Phase Characteristics vs. Frequency (0–10 kHz)

enhanced accuracy. The figures are transfer functions with the input to be considered as a sinusoidally varying mechanical position and the output as the voltage from the AD598; the units of the transfer function are volts per inch. The value of C2, C3 and C4, from Figure 7, are all equal and designated as a parameter in the figures. The response is approximately that of two real poles. However, there is appreciable excess phase at higher frequencies. An additional pole of filtering can be introduced with a shunt capacitor across R2, (see Figure 7); this will also increase phase lag.

When selecting values of C2, C3 and C4 to set the bandwidth of the system, a trade-off is involved. There is ripple on the "dc" position output voltage, and the magnitude is determined by the filter capacitors. Generally, smaller capacitors will give higher system bandwidth and larger ripple. Figures 16 and 17 show the magnitude of ripple as a function of C2, C3 and C4, again all equal in value. Note also a shunt capacitor across R2 shown as a parameter (see Figure 7). The value of R2 used was 81 kΩ with a Schaevitz E100 LVDT.

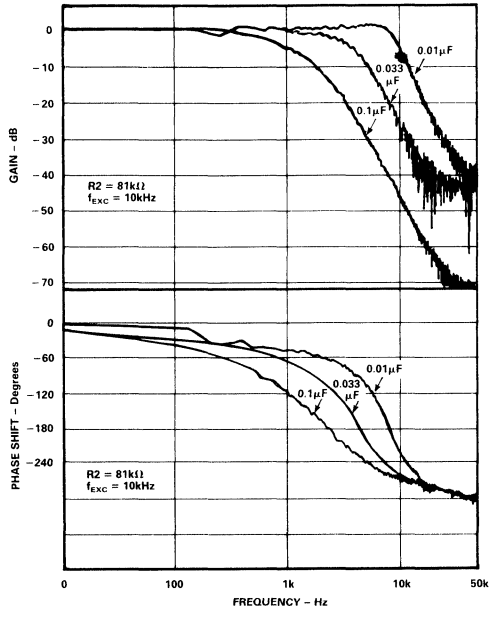


Figure 14. Gain and Phase Characteristics vs. Frequency (0–50 kHz)

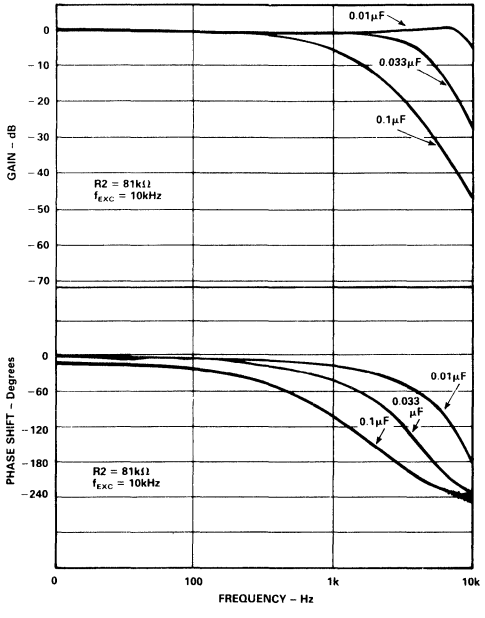


Figure 15. Gain and Phase Characteristics vs. Frequency (0–10 kHz)

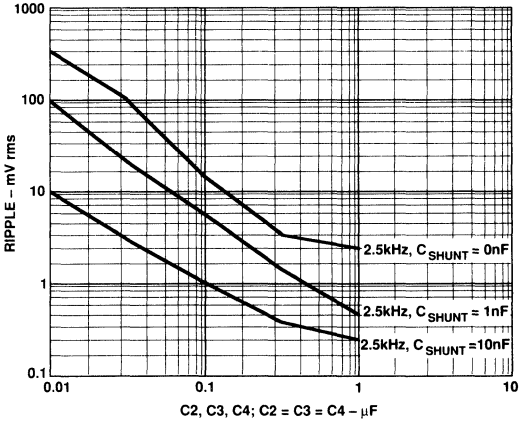


Figure 16. Output Voltage Ripple vs. Filter Capacitance

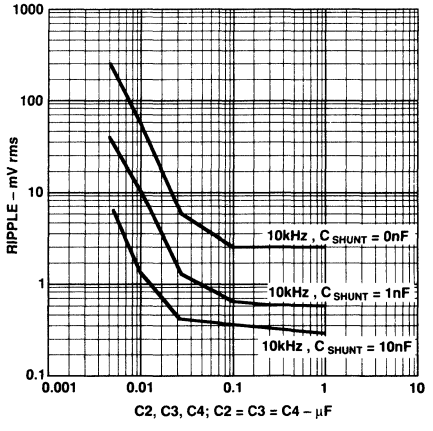


Figure 17. Output Voltage Ripple vs. Filter Capacitance

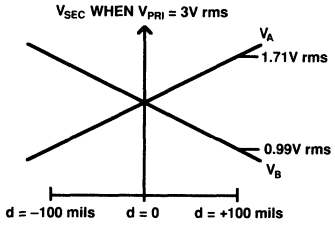


Figure 18. LVDT Secondary Voltage vs. Core Displacement

Determining LVDT Sensitivity
LVDT sensitivity can be determined by measuring the LVDT secondary voltages as a function of primary drive and core position, and performing a simple computation.

Energize the LVDT at its recommended primary drive level, V_{PRI} (3 V rms for the E100). Set the core to midpoint where $V_A = V_B$. Set the core displacement to its mechanical full-scale position and measure secondary voltages V_A and V_B.

$$Sensitivity = \frac{V_A\ (at\ Full\ Scale) - V_B\ (at\ Full\ Scale)}{V_{PRI} \times d}$$

From Figure 18,

$$Sensitivity = \frac{1.71 - 0.99}{3 \times 100\ mils} = 2.4\ mV/V/mil$$

Thermal Shutdown and Loading Considerations.
The AD598 is protected by a thermal overload circuit.If the die temperature reaches 165°C, the sine wave excitation amplitude gradually reduces, thereby lowering the internal power dissipation and temperature.

Due to the ratiometric operation of the decoder circuit, only small errors result from the reduction of the excitation amplitude. Under these conditions the signal-processing section of the AD598 continues to meet its output specifications.

The thermal load depends upon the voltage and current delivered to the load as well as the power supply potentials. An LVDT Primary will present an inductive load to the sine wave excitation. The phase angle between the excitation voltage and current must also be considered, further complicating thermal calculations.

APPLICATIONS

PROVING RING-WEIGH SCALE
Figure 20 shows an elastic member (steel proving ring) combined with an LVDT to provide a means of measuring very small loads. Figure 19 shows the electrical circuit details.

The advantage of using a Proving Ring in combination with an LVDT is that no friction is involved between the core and the coils of the LVDT. This means that weights can be measured without confusion from frictional forces. This is especially important for very low full-scale weight applications.

Although it is recognized that this type of measurement system may best be applied to weigh very small weights, this circuit was designed to give a full-scale output of 10 V for a 500 lb weight, using a Morehouse Instruments model 5BT Proving Ring. The LVDT is a Schaevitz type HR050 (±50 mil full scale). Although this LVDT provides ± 50 mil full scale, the value of R2 was calculated for d = ±30 mil and V_{OUT} equal to 10 V as in Step 9 of the design procedures.

The 1 μF capacitor provides extra filtering, which reduces noise induced by mechanical vibrations. The other circuit values were calculated in the usual manner using the design procedures.

This weigh-scale can be designed to measure tare weight simply by putting in an offset voltage by selecting either R3 or R4 (as shown in Figures 7 and 12). Tare weight is the weight of a container that is deducted from the gross weight to obtain the net weight.

The value of R3 or R4 can be calculated using one of two separate methods. First, a potentiometer may be connected between Pins 18 and 19 of the AD598, with the wiper connected to $-V_{SUPPLY}$. This gives a small offset of either polarity; and the value can be calculated using Step 10 of the design procedures. For a large offset in one direction, replace either R3 or R4 with a potentiometer with its wiper connected to $-V_{SUPPLY}$.

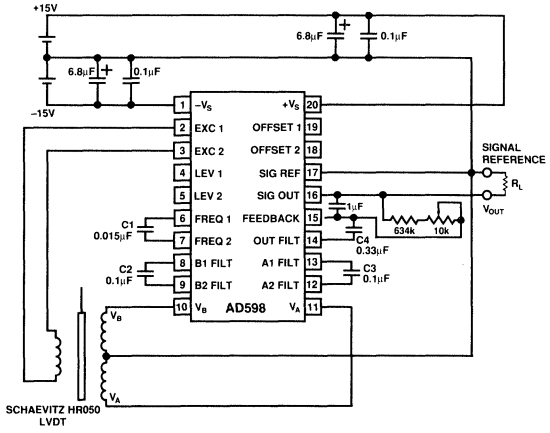


Figure 19. Proving Ring-Weigh Scale Circuit

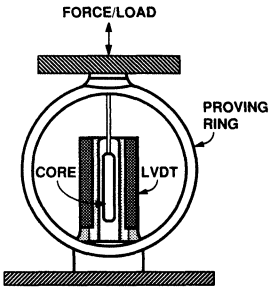


Figure 20. Proving Ring-Weigh Scale Cross Section

The resolution of this weigh-scale was checked by placing a 100 gram weight on the scale and observing the AD598 output signal deflection on an oscilloscope. The deflection was 4.8 mV.

The smallest signal deflection which could be measured on the oscilloscope was 450 μV which corresponds to a 10 gram weight. This 450 μV signal corresponds to an LVDT displacement of 1.32 microinches which is equivalent to one tenth of the wave length of blue light.

The Proving Ring used in this circuit has a temperature coefficient of 250 ppm/°C due to Young's Modulus of steel. By putting a resistor with a temperature coefficient in place of R2 it is possible to temperature compensate the weigh-scale. Since the steel of the Proving Ring gets softer at higher temperatures, the deflection for a given force is larger, so a resistor with a negative temperature coefficient is required.

SYNCHRONOUS OPERATION OF MULTIPLE LVDTS

In many applications, such as multiple gaging measurement, a large number of LVDTs are used in close physical proximity. If these LVDTs are operated at similar carrier frequencies, stray magnetic coupling could cause beat notes to be generated. The resulting beat notes would interfere with the accuracy of measurements made under these conditions. To avoid this situation all the LVDTs are operated synchronously.

The circuit shown in Figure 21 has one master oscillator and any number of slaves. The master AD598 oscillator has its frequency and amplitude programmed in the usual manner via R1 and C2 using Steps 6 and 7 in the design procedures. The slave AD598s all have Pins 6 and 7 connected together to disable their internal oscillators. Pins 4 and 5 of each slave are connected to Pins 2 and 3 of the master via 15 kΩ resistors, thus setting the amplitudes of the slaves equal to the amplitude of the master. If a different amplitude is required the 15 kΩ resistor values should be changed. Note that the amplitude scales linearly with the resistor value.The 15 kΩ value was selected because it matches the nominal value of resistors internal to the circuit. Tolerances of 20% between the slave amplitudes arise due to differing internal resistors values, but this does not affect the operation of the circuit.

Note that each LVDT primary is driven from its own power amplifier and thus the thermal load is shared between the AD598s. There is virtually no limit on the number of slaves in this circuit, since each slave presents a 30 kΩ load to the master AD598 power amplifier. For a very large number of slaves (say 100 or more) one may need to consider the maximum output current drawn from the master AD598 power amplifier.

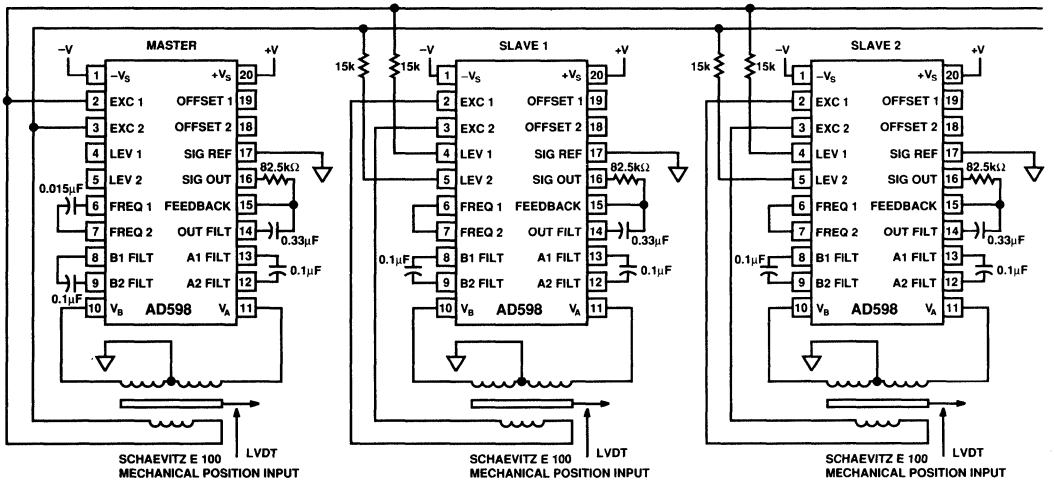


Figure 21. Multiple LVDTs – Synchronous Operation

HIGH RESOLUTION POSITION-TO-FREQUENCY CIRCUIT

In the circuit shown in Figure 22, the AD598 is combined with an AD652 voltage-to-frequency (V/F) converter to produce an effective, simple data converter which can make high resolution measurements.

This circuit transfers the signal from the LVDT to the V/F converter in the form of a current, thus eliminating the errors normally caused by the offset voltage of the V/F converter. The V/F converter offset voltage is normally the largest source of error in such circuits. The analog input signal to the AD652 is converted to digital frequency output pulses which can be counted by simple digital means.

This circuit is particularly useful if there is a large degree of mechanical vibration (hum) on the position to be measured. The hum may be completely rejected by counting the digital frequency pulses over a gate time (fixed period) equal to a multiple of the hum period. For the effects of the hum to be completely rejected, the hum must be a periodic signal.

The V/F converter is currently set up for unipolar operation. The AD652 data sheet explains how to set up for bipolar operation. Note that when the LVDT core is centered, the output frequency is zero. When the LVDT core is positioned off center, and to one side, the frequency increases to a full-scale value. To introduce bipolar operation to this circuit, an offset must be introduced at the LVDT as shown in Step 10 of the design procedures.

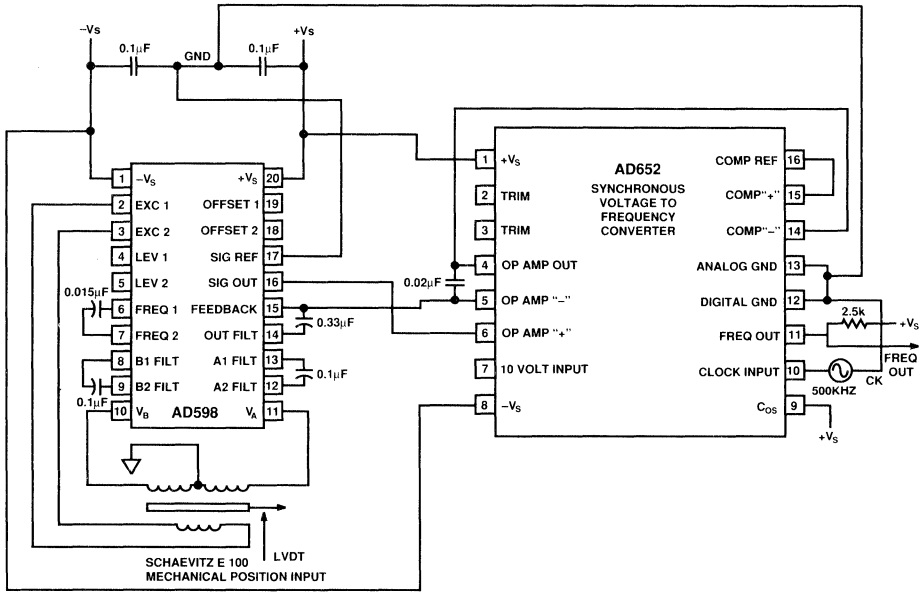


Figure 22. High Resolution Position-to-Frequency Converter

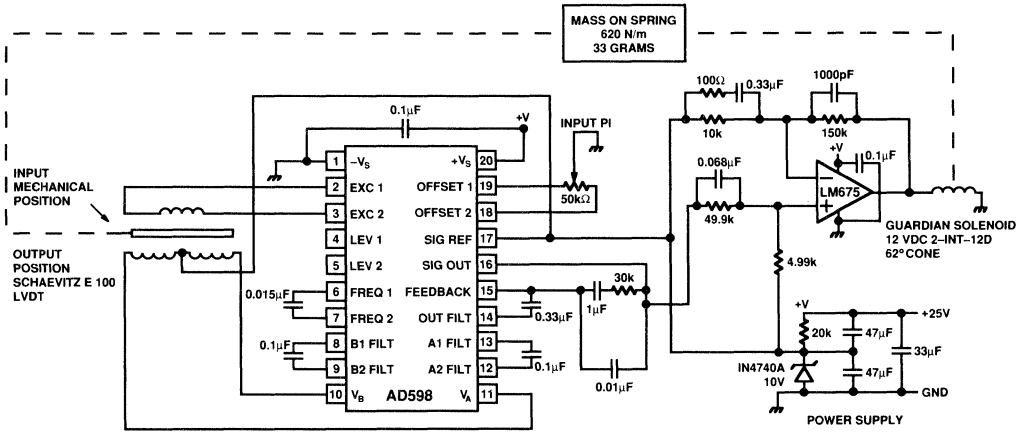


Figure 23. Low Cost Set-Point Controller

LOW COST SET-POINT CONTROLLER

A low cost set-point controller can be implemented with the circuit shown in Figure 23. Such a circuit could possibly be used in automobile fuel control systems. The potentiometer, P1, is attached to the gas pedal, and the LVDT is attached to the butterfly valve of the fuel injection system or carburetor. The position of the butterfly valve is electronically controlled by the position of the gas pedal, without mechanical linkage.

This circuit is a simple two IC closed loop servo-controller. It is simple because the LVDT circuit is functioning as the loop integrator. By putting a capacitor in the feedback path (normally occupied by R2), the output signal from the AD598 corresponds to the time integral of the position being measured by the LVDT. The LVDT position signal is summed with the offset signal introduced by the potentiometer, P1. Since this sum is integrated, it must be forced to zero. Thus the LVDT position is forced to follow the value of the input potentiometer, P1. The output signal from the AD598 drives the LM675 power amplifier, which in turn drives the solenoid.

This circuit has dual advantages of being both low cost and high accuracy. The high accuracy results from avoiding the offset errors normally associated with converting the LVDT signal to a voltage and then subsequently integrating that voltage.

MECHANICAL FOLLOWER SERVO-LOOP

Figure 24 shows how two Schaevitz E100 LVDTs may be combined with two AD598s in a mechanical follower servo-loop configuration. One of the LVDTs provides the mechanical input position signal, while the other LVDT mimics the motion.

The signal from the input position circuit is fed to the output as a current so that voltage offset errors are avoided. This current signal is summed with the signal from the output position LVDT; this summed signal is integrated such that the output position is now equal to the input position. This circuit is an efficient means of implementing a mechanical servo-loop since only three ICs are required.

This circuit is similar to the previous circuit (Figure 23) with one exception: the previous circuit uses a potentiometer instead of an LVDT to provide the input position signal. Replacing the potentiometer with an LVDT offers two advantages. First, the increased reliability and robustness of the LVDT can be exploited in applications where the position input sensor is located in a hostile environment. Second, the mechanical motions of the input and output LVDTs are guaranteed to be identical to within the matching of their individual scale factors. These particular advantages make this circuit ideal for application as a hydraulic actuator controller.

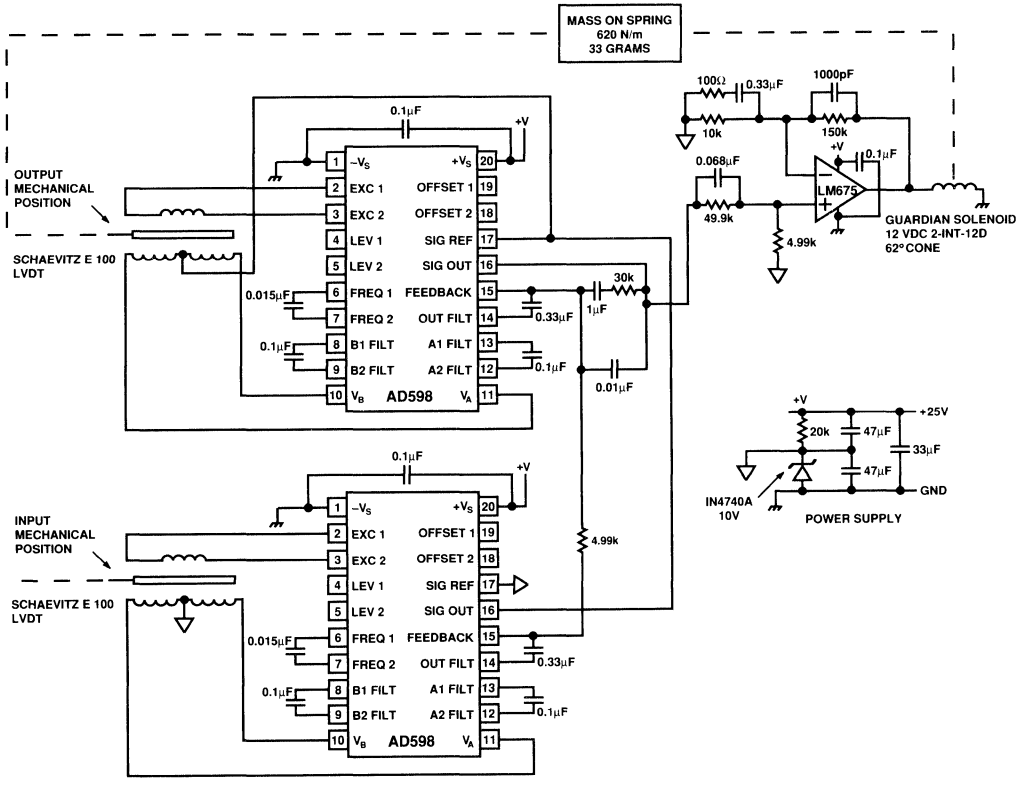


Figure 24. Mechanical Follower Servo-Loop

DIFFERENTIAL GAGING

LVDTs are commonly used in gaging systems. Two LVDTs can be used to measure the thickness or taper of an object. To measure thickness, the LVDTs are placed on either side of the object to be measured. The LVDTs are positioned such that there is a known maximum distance between them in the fully retracted position.

This circuit is both simple and inexpensive. It has the advantage that two LVDTs may be driven from one AD598, but the disadvantage is that the scale factor of each LVDT may not match exactly. This causes the workpiece thickness measurement to vary depending upon its absolute position in the differential gage head.

This circuit was designed to produce a ±10 V signal output swing, composed of the sum of the two independent ±5 V swings from each LVDT. The output voltage swing is set with an 80.9 kΩ resistor. The output voltage Vout for this circuit is given by:

$$V_{OUT} = \left[\frac{(V_A - V_B)}{(V_A + V_B)} + \frac{(V_C - V_D)}{(V_C + V_D)}\right] \times 500\ \mu A \times R2.$$

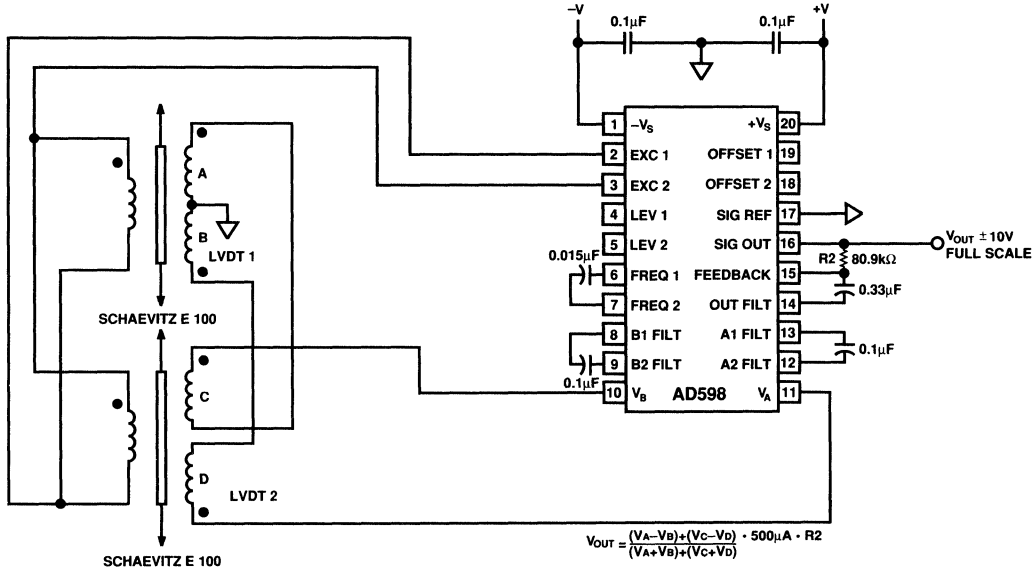


Figure 25. Differential Gaging

PRECISION DIFFERENTIAL GAGING

The circuit shown in Figure 26 is functionally similar to the differential gaging circuit shown in Figure 25. In contrast to Figure 25, it provides a means of independently adjusting the scale factor of each LVDT so that both scale factors may be matched.

The two LVDTs are driven in a master-slave arrangement where the output signal from the slave LVDT is summed with the output signal from the master LVDT. The scale factor of the slave LVDT only is adjusted with R1 and R2. The summed scale factor of the master LVDT and the slave LVDT is adjusted with R3.

R1 and R2 are chosen to be 80.9 kΩ resistors to give a ±10 V full-scale output signal for a single Schaevitz E100 LVDT. R3 is chosen to be 40.2 kΩ to give a ±10 V output signal when the two E100 LVDT output signals are summed. The output voltage for this circuit is given by:

$$V_{OUT} = \left[\frac{(V_A - V_B)}{(V_A + V_B)} + \frac{(V_C - V_D)}{(V_C + V_D)} \times \frac{R2}{R1}\right] \times 500\ \mu A \times R3.$$

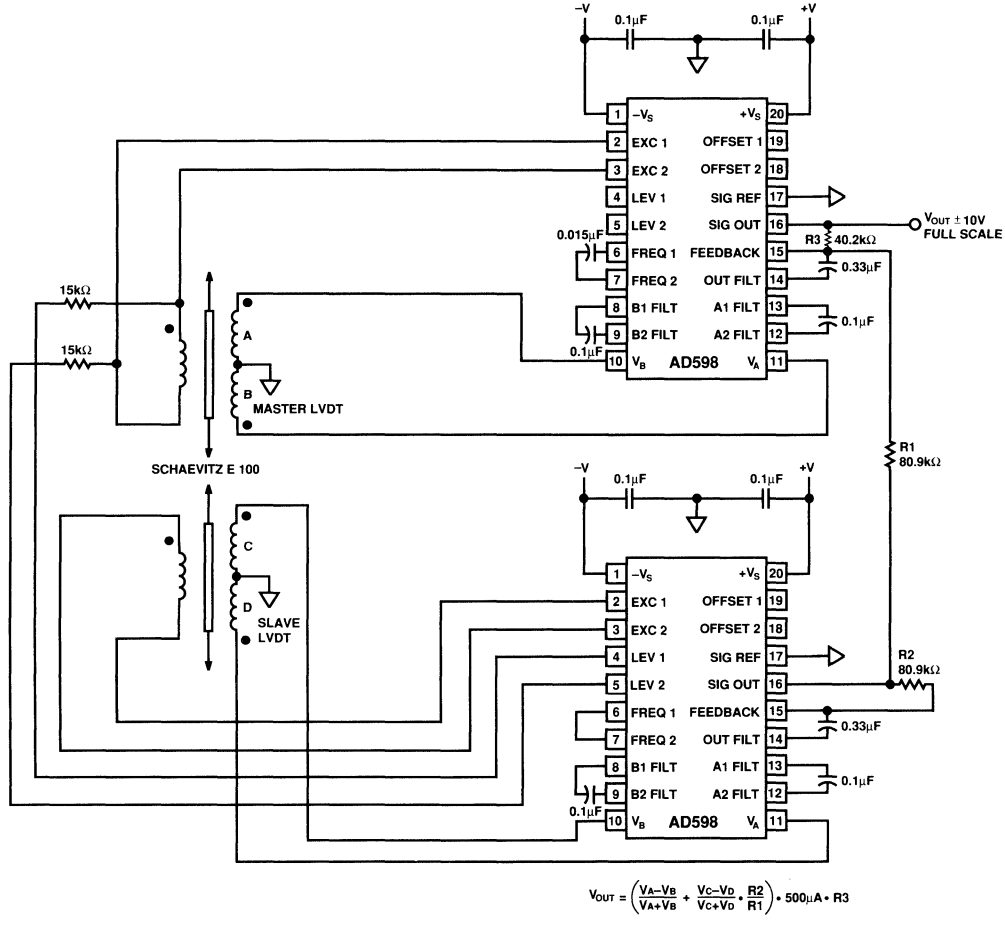


Figure 26. Precision Differential Gaging

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OPERATION WITH A HALF-BRIDGE TRANSDUCER

Although the AD598 is not intended for use with a half-bridge type transducer, it may be made to function with degraded performance.

A half-bridge type transducer is a popular transducer. It works in a similar manner to the LVDT in that two coils are wound around a moveable core and the inductance of each coil is a function of core position.

In the circuit shown in Figure 27 the V_A and V_B input voltages are developed as two resistive-inductor dividers. If the inductors are equal (i.e., the core is centered), the V_A and V_B input voltages to the AD598 are equal and the output voltage V_{OUT} is zero. When the core is positioned off center, the inductors are unequal and an output voltage V_{OUT} is developed.

The linearity of this circuit is dependent upon the value of the resistors in the resistive-inductor dividers. The optimum value may be transducer dependent and therefore must be selected by trial and error. The 300 Ω resistors in this circuit optimize the nonlinearity of the transfer function to within several tenths of 1%. This circuit uses a Sangamo AGH1 half-bridge transducer. The 1 μF capacitor blocks the dc offset of the excitation output signal. The 4 nF capacitor sets the transducer excitation frequency to 10 kHz as recommended by the manufacturer.

ALTERNATE HALF-BRIDGE TRANSDUCER CIRCUIT

This circuit suffers from similar accuracy problems to those mentioned in the previous circuit description. In this circuit the V_A input signal to the AD598 really and truly is a linear function of core position, and the input signal V_B, is one half of the excitation voltage level. However, a nonlinearity is introduced by the A−B/A+B transfer function.

The 500 Ω resistors in this circuit are chosen to minimize errors caused by dc bias currents from the V_A and V_B inputs. Note that in the previous circuit these bias currents see very low resistance paths to ground through the coils.

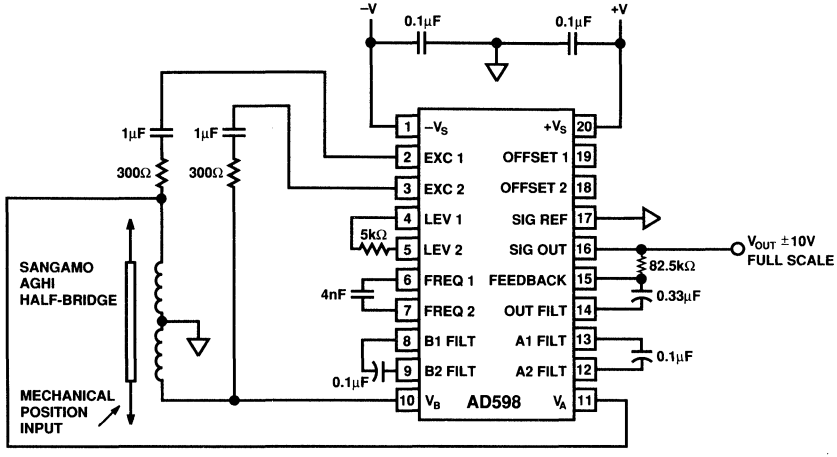


Figure 27. Half-Bridge Operation

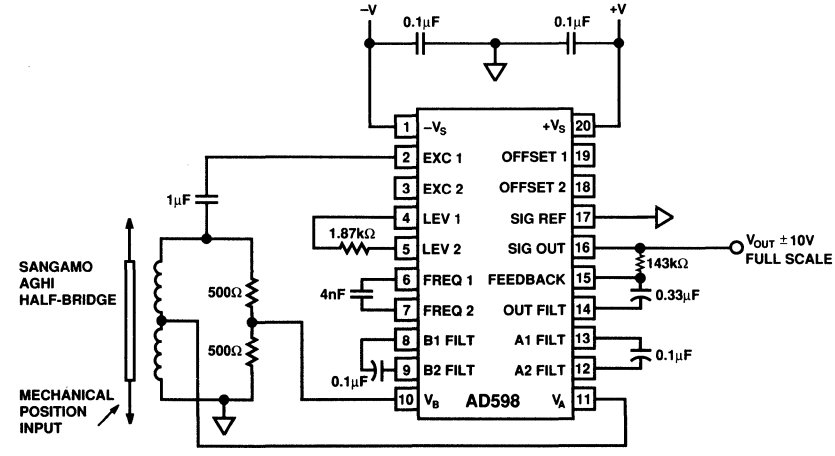


Figure 28. Alternate Half-Bridge Circuit

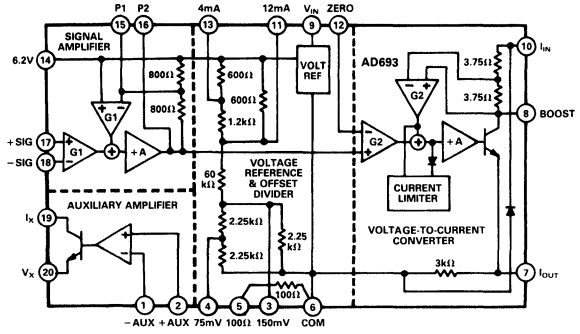
Loop-Powered 4–20mA Sensor Transmitter

AD693

FEATURES

- **Instrumentation Amplifier Front End**
- **Loop-Powered Operation**
- **Precalibrated 30mV or 60mV Input Spans**
- **Independently Adjustable Output Span and Zero**
- **Precalibrated Output Spans: 4–20mA Unipolar**
  0–20mA Unipolar
  12 ± 8mA Bipolar
- **Precalibrated 100Ω RTD Interface**
- **6.2V Reference with Up to 3.5mA of Current Available**
- **Uncommitted Auxiliary Amp for Extra Flexibility**
- **Optional External Pass Transistor to Reduce Self-Heating Errors**

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD693 is a monolithic signal conditioning circuit which accepts low-level inputs from a variety of transducers to control a standard 4–20mA, two-wire current loop. An on-chip voltage reference and auxiliary amplifier are provided for transducer excitation; up to 3.5mA of excitation current is available when the device is operated in the loop-powered mode. Alternatively, the device may be locally powered for three-wire applications when 0–20mA operation is desired.

Precalibrated 30mV and 60mV input spans may be set by simple pin strapping. Other spans from 1mV to 100mV may be realized with the addition of external resistors. The auxiliary amplifier may be used in combination with on-chip voltages to provide six precalibrated ranges for 100Ω RTDs. Output span and zero are also determined by pin strapping to obtain the standard ranges: 4–20mA, 12 ± 8mA and 0–20mA.

Active laser trimming of the AD693's thin-film resistors result in high levels of accuracy without the need for additional adjustments and calibration. Total unadjusted error is tested on every device to be less than 0.5% of full scale at +25°C, and less than 0.75% over the industrial temperature range. Residual nonlinearity is under 0.05%. The AD693 also allows for the use of an external pass transistor to further reduce errors caused by self-heating.

For transmission of low-level signals from RTDs, bridges and pressure transducers, the AD693 offers a cost-effective signal conditioning solution. It is recommended as a replacement for discrete designs in a variety of applications in process control, factory automation and system monitoring.

The AD693 is packaged in a 20-pin ceramic side-brazed DIP, 20-pin Cerdip, and 20-pin LCCC and is specified over the −40°C to +85°C industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD693 is a complete monolithic low-level voltage-to-current loop signal conditioner.
2. Precalibrated output zero and span options include 4–20mA, 0–20mA, and 12 ± 8mA in two- and three-wire configurations.
3. Simple resistor programming adds a continuum of ranges to the basic 30mV and 60mV input spans.
4. The common-mode range of the signal amplifier input extends from ground to near the device's operating voltage.
5. Provision for transducer excitation includes a 6.2V reference output and an auxiliary amplifier which may be configured for voltage or current output and signal amplification.
6. The circuit configuration permits simple linearization of bridge, RTD, and other transducer signals.
7. A monitored output is provided to drive an external pass transistor. This feature off-loads power dissipation to extend the temperature range of operation, enhance reliability, and minimize self-heating errors.
8. Laser-wafer trimming results in low unadjusted errors and affords precalibrated input and output spans.
9. Zero and span are independently adjustable and noninteractive to accommodate transducers or user defined ranges.
10. Six precalibrated temperature ranges are available with a 100Ω RTD via pin strapping.

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AD693—SPECIFICATIONS (@ +25°C and V_S = +24V. Input Span = 30mV or 60mV, Output Span = 4–20mA, R_L = 250Ω, V_{CM} = 3.1V, with external pass transistor unless otherwise noted)

Model	Conditions	AD693AD/AQ/AE Min	Typ	Max	Units
LOOP-POWERED OPERATION					
TOTAL UNADJUSTED ERROR[1, 2]			±0.25	**±0.5**	% Full Scale
T_{min} to T_{max}			±0.4	**±0.75**	% Full Scale
100Ω RTD CALIBRATION ERROR[3]	(See Fig. 17)		±0.5	±2.0	°C
LOOP POWERED OPERATION[2]					
Zero Current Error[4]	Zero = 4mA		±25	**±80**	μA
	Zero = 12mA		±40	**±120**	μA
	Zero = 0mA[5]	+7	+35	**+100**	μA
vs. Temp.	Zero = 4mA		±0.5	±1.5	μA/°C
Power Supply Rejection (RTI)	12V ≤ V_{OP} ≤ 36V[6]		±3.0	**±5.6**	μV/V
	0V ≤ V_{CM} ≤ 6.2V				
Common-Mode Input Range	(See Fig. 3)	0		$+V_{OP}-4V$[6]	V
Common-Mode Rejection (RTI)	0V ≤ V_{CM} ≤ 6.2V		±10	**±30**	μV/V
Input Bias Current[7]			+5	**+20**	nA
T_{min} to T_{max}			+7	**+25**	nA
Input Offset Current[7]	V_{SIG} = 0		±0.5	**±3.0**	nA
Transconductance					
Nominal	30mV Input Span		0.5333		A/V
	60mV Input Span		0.2666		A/V
Unadjusted Error			±0.05	**±0.2**	%
vs. Common-Mode	0V ≤ V_{CM} ≤ 6.2V				
	30mV Input Span		±0.03	±0.04	%/V
	60mV Input Span		±0.05	±0.06	%/V
Error vs. Temp.			±20	±50	ppm/°C
Nonlinearity[8]	30mV Input Span		±0.01	**±0.05**	% of Span
	60mV Input Span		±0.02	**±0.07**	% of Span
OPERATIONAL VOLTAGE RANGE					
Operational Voltage, V_{OP}[6]		**+12**		**+36**	V
Quiescent Current	Into Pin 9		+500	**+700**	μA
OUTPUT CURRENT LIMIT		**+21**	+25	**+32**	mA
COMPONENTS OF ERROR					
SIGNAL AMPLIFIER[9]					
Input Voltage Offset			±40	**±200**	μV
vs. Temp			±1.0	±2.5	μV/°C
Power Supply Rejection	12V ≤ V_{OP} ≤ 36V[6]		±3.0	**±5.6**	μV/V
	0V ≤ V_{CM} ≤ 6.2V				
V/I CONVERTER[9, 10]					
Zero Current Error	Output Span = 4–20mA		±30	±80	μA
Power Supply Rejection	12V ≤ V_{OP} ≤ 36V[6]		±1.0	±3.0	μA/V
Transconductance					
Nominal			0.2666		A/V
Unadjusted Error			±0.05	±0.2	%
6.200V REFERENCE[9, 12]					
Output Voltage Tolerance			±3	**±12**	mV
vs. Temp.			±20	±50	ppm/°C
Line Regulation	12V ≤ V_{OP} ≤ 36V[6]		±200	**±300**	μV/V
Load Regulation[11]	0mA ≤ I_{REF} ≤ 3mA		±0.3	**±0.75**	mV/mA
Output Current[13]	Loop Powered, (Fig. 10)	**+3.0**	+3.5		mA
	3-Wire Mode, (Fig. 15)		+5.0		mA

Model	Conditions	AD693AD Min	Typ	Max	Units
AUXILIARY AMPLIFIER					
Common-Mode Range		0		$+V_{OP}-4V$[6]	V
Input Offset Voltage			±50	±200	μV
Input Bias Current			+5	+20	nA
Input Offset Current			+0.5	±3.0	nA
Common-Mode Rejection			90		dB
Power Supply Rejection			105		dB
Output Current Range	Pin I_X OUT	+0.01		+5	mA
Output Current Error	Pin V_X – Pin I_X		±0.005		%
TEMPERATURE RANGE					
Case Operating[14]	T_{min} to T_{max}	−40		+85	°C
Storage		−65		+150	°C

NOTES

[1]Total error can be significantly reduced (typically less than 0.1%) by trimming the zero current. The remaining unadjusted error sources are transconductance and nonlinearity.

[2]The AD693 is tested as a loop powered device with the signal amp, V/I converter, voltage reference, and application voltages operating together. Specifications are valid for preset spans and spans between 30mV and 60mV.

[3]Error from ideal output assuming a perfect 100Ω RTD at 0 and +100°C.

[4]Refer to the Error Analysis to calculate zero current error for input spans less than 30mV.

[5]By forcing the differential signal amplifier input sufficiently negative the 7μA zero current can always be achieved.

[6]The operational voltage (V_{OP}) is the voltage directly across the AD693 (Pin 10 to 6 in two-wire mode, Pin 9 to 6 in local power mode). For example, $V_{OP} = V_S - (I_{LOOP} \times R_L)$ in two-wire mode (refer to Figure 10).

[7]Bias currents are not symmetrical with input signal level and flow out of the input pins. The input bias current of the inverting input increases with input signal voltage, see Figure 2.

[8]Nonlinearity is defined as the deviation of the output from a straight line connecting the endpoints as the input is swept over a 30mV and 60mV input span.

[9]Specifications for the individual functional blocks are components of error that contribute to, and that are included in, the Loop Powered Operation specifications.

[10]Includes error contributions of V/I converter and Application Voltages.

[11]Changes in the reference output voltage due to load will affect the Zero Current. A 1% change in the voltage reference output will result in an error of 1% in the value of the Zero Current.

[12]If not used for external excitation, the reference should be loaded by approximately 1mA (6.2kΩ to common).

[13]In the loop powered mode up to 5mA can be drawn from the reference, however, the lower limit of the output span will be increased accordingly. 3.5mA is the maximum current the reference can source while still maintaining a 4mA zero.

[14]The AD693 is tested with a pass transistor so $T_A \cong T_C$.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

10

ABSOLUTE MAXIMUM RATINGS

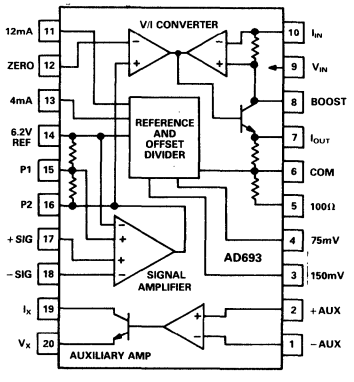
Supply Voltage . . . . . +36V
Reverse Loop Current 200mA
Signal Amp Input Range . . . . . −0.3V to V_{OP}
Reference Short Circuit to Common . . . . . Indefinite
Auxiliary Amp Input Voltage Range . . . . . −0.3V to V_{OP}
Auxiliary Amp Current Output 10mA
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature, 10sec Soldering . . . . . +300°C
Max Junction Temperature . . . . . +150°C

ORDERING GUIDE

Model	Package Description	Package Option*
AD693AD	Ceramic Side-Brazed DIP	D-20
AD693AQ	Cerdip	Q-20
AD693AE	Leadless Ceramic Chip Carrier (LCCC)	E-20A

*For outline information see Package Information section.

AD693 PIN CONFIGURATION (AD, AW, AE Packages)



Functional Diagram

AD693—Typical Characteristics

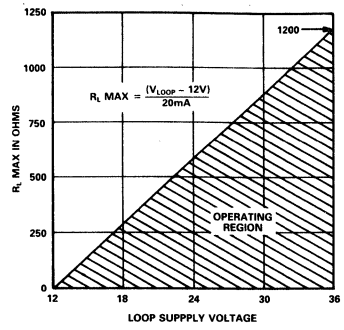


Figure 1. Maximum Load Resistance vs. Power Supply

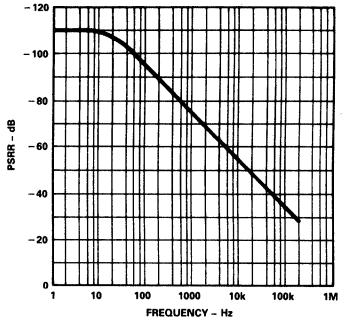


Figure 5. Signal Amplifier PSRR vs. Frequency

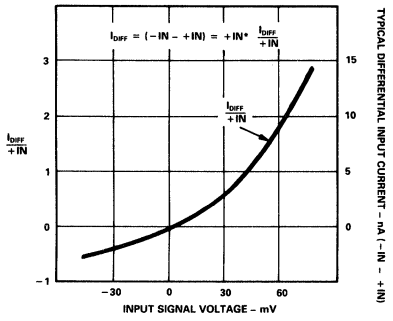


Figure 2. Differential Input Current vs. Input Signal Voltage Normalized to +IN

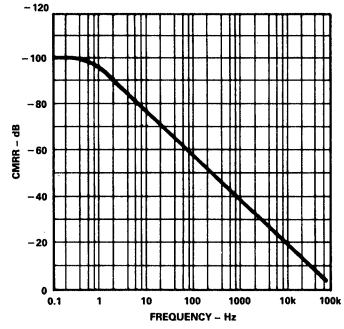


Figure 6. CMRR (RTI) vs. Frequency

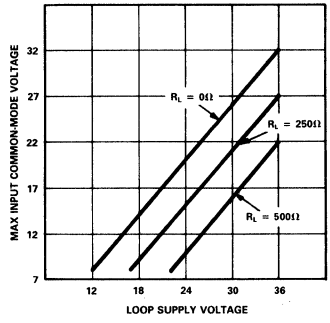


Figure 3. Maximum Common-Mode Voltage vs. Supply

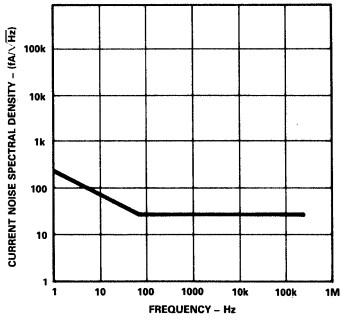


Figure 7. Input Current Noise vs. Frequency

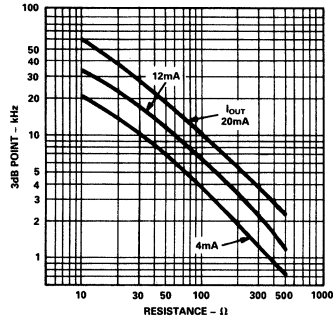


Figure 4. Bandwidth vs. Series Load Resistance

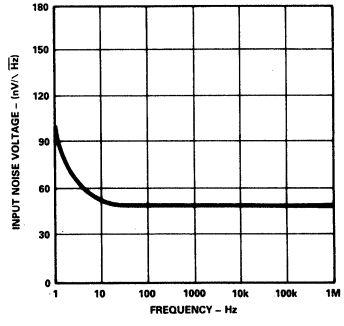


Figure 8. Input Voltage Noise vs. Frequency

FUNCTIONAL DESCRIPTION

The operation of the AD693 can be understood by dividing the circuit into three functional parts (see Figure 9). First, an instrumentation amplifier front-end buffers and scales the low-level input signal. This amplifier drives the second section, a V/I converter, which provides the 4–to–20mA loop current. The third section, a voltage reference and resistance divider, provides application voltages for setting the various "live zero" currents. In addition to these three main sections, there is an on-chip auxiliary amplifier which can be used for transducer excitation.

VOLTAGE-TO-CURRENT (V/I) CONVERTER

The output NPN transistor for the V/I section sinks loop current when driven on by a high gain amplifier at its base. The input for this amplifier is derived from the difference in the outputs of the matched preamplifiers having gains, G2. This difference is caused to be small by the large gain, +A, and the negative feedback through the NPN transistor and the loop current sampling resistor between I_{IN} and Boost. The signal across this resistor is compared to the input of the left preamp and servos the loop current until both signals are equal. Accurate voltage-to-current transformation is thereby assured. The preamplifiers employ a special design which allows the active feedback amplifier to operate from the most positive point in the circuit, I_{IN}.

The V/I stage is designed to have a nominal transconductance of 0.2666 A/V. Thus, a 75mV signal applied to the inputs of the V/I (Pin 16, noninverting; Pin 12, inverting) results in a full-scale output current of 20mA.

The current limiter operates as follows: the output of the feedback preamp is an accurate indication of the loop current. This output is compared to an internal setpoint which backs off the drive to the NPN transistor when the loop current approaches 25mA. As a result, the loop and the AD693 are protected from the consequences of voltage overdrive at the V/I input.

VOLTAGE REFERENCE AND DIVIDER

A stabilized bandgap voltage reference and laser-trimmed resistor divider provide for both transducer excitation as well as precalibrated offsets for the V/I converter. When not used for external excitation, the reference should be loaded by approximately 1mA (6.2kΩ to common).

The 4mA and 12mA taps on the resistor divider correspond to −15mV and −45mV, respectively, and result in a live zero of 4mA or 12mA of loop current when connected to the V/I converter's inverting input (Pin 12). Arranging the zero offset in this way makes the zero signal output current independent of input span. When the input to the signal amp is zero, the noninverting input of the V/I is at 6.2V.

Since the standard offsets are laser trimmed at the factory, adjustment is seldom necessary except to accommodate the zero offset of the actual source. (See "Adjusting Zero".)

SIGNAL AMPLIFIER

The Signal Amplifier is an instrumentation amplifier used to buffer and scale the input to match the desired span. Inputs applied to the Signal Amplifier (at Pins 17 and 18) are amplified and referred to the 6.2V reference output in much the same way as the level translation occurs in the V/I converter. Signals from the two preamplifiers are subtracted, the difference is amplified, and the result is fed back to the upper preamp to minimize the difference. Since the two preamps are identical, this minimum will occur when the voltage at the upper preamp just matches the differential input applied to the Signal Amplifier at the left.

Since the signal which is applied to the V/I is attenuated across the two 800Ω resistors before driving the upper preamp, it will necessarily be an amplified version of the signal applied between Pins 17 and 18. By changing this attenuation, you can control the span referred to the Signal Amplifier. To illustrate: a 75mV signal applied to the V/I results in a 20mA loop current. Nominally, 15mV is applied to offset the zero to 4mA leaving a 60mV range to correspond to the span. And, since the nominal attenuation of the resistors connected to Pins 16, 15 and 14 is 2.00, a 30mV input signal will be doubled to result in 20mA of loop current. Shorting Pins 15 and 16 results in unity gain and permits a 60mV input span. Other choices of span may be implemented with user supplied resistors to modify the attenuation. (See section "Adjusting Input Span".)

The Signal Amplifier is specially designed to accommodate a large common-mode range. Common-mode signals anywhere up to and beyond the 6.2V reference are easily handled as long as V_{IN} is sufficiently positive. The Signal Amplifier is biased with respect to V_{IN} and requires about 3.5 volts of headroom. The extended range will be useful when measuring sensors driven, for example, by the auxiliary amplifier which may go above the 6.2V potential. In addition, the PNP input stage will continue to operate normally with common-mode voltages of several hundred mV, negative, with respect to common. This feature accommodates self-generating sensors, such as thermocouples,

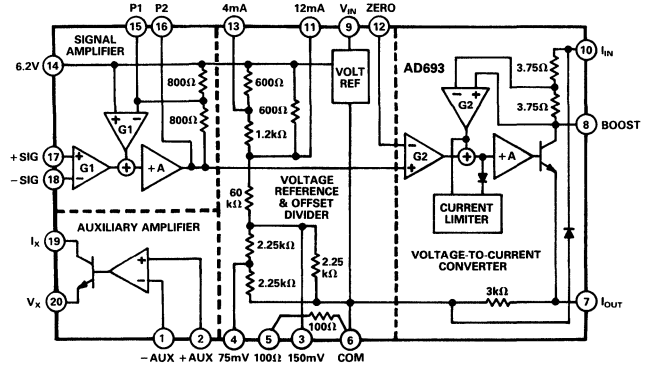


Figure 9. Functional Block Diagram

which may produce small negative normal-mode signals as well as common-mode noise on "grounded" signal sources.

AUXILIARY AMPLIFIER

The Auxiliary Amplifier is included in the AD693 as a signal conditioning aid. It can be used as an op amp in noninverting applications and has special provisions to provide a controlled current output. Designed with a differential input stage and an unbiased Class A output stage, the amplifier can be resistively loaded to common with the self-contained 100Ω resistor or with a user supplied resistor.

As a functional element, the Auxiliary Amplifier can be used in dynamic bridges and arrangements such as the RTD signal conditioner shown in Figure 17. It can be used to buffer, amplify and combine other signals with the main Signal Amplifier. The Auxiliary Amplifier can also provide other voltages for excitation if the 6.2V of the reference is unsuitable. Configured as a simple follower, it can be driven from a user supplied voltage divider or the precalibrated outputs of the AD693 divider (Pins 3 and 4) to provide a stiff voltage output at less than the 6.2 level, or by incorporating a voltage divider as feedback around the amplifier, one can gain-up the reference to levels higher than 6.2V. If large positive outputs are desired, I_X, the Auxiliary Amplifier output current supply, should be strapped to either V_{IN} or Boost. Like the Signal Amplifier, the Auxiliary requires about 3.5V of headroom with respect to V_{IN} at its input and about 2V of difference between I_X and the voltage to which V_X is required to swing.

The output stage of the Auxiliary Amplifier is actually a high gain Darlington transistor where I_X is the collector and V_X is the emitter. Thus, the Auxiliary Amplifier can be used as a V/I converter when configured as a follower and resistively loaded. I_X functions as a high-impedance current source whose current is equal to the voltage at V_X divided by the load resistance. For example, using the onboard 100Ω resistor and the 75mV or 150mV application voltages, either a 750μA or 1.5mA current source can be set up for transducer excitation.

The I_X terminal has voltage compliance within 2V of V_X. If the Auxiliary Amplifier is not to be used, then Pin 2, the noninverting input, should be grounded.

REVERSE VOLTAGE PROTECTION FEATURE

In the event of a reverse voltage being applied to the AD693 through a current-limited loop (limited to 200mA), an internal shunt diode protects the device from damage. This protection mode avoids the compliance voltage penalty which results from a series diode that must be added if reversal protection is required in high-current loops.

Applying the AD693

CONNECTIONS FOR BASIC OPERATION

Figure 10 shows the minimal connections for basic operation: 0–30mV input span, 4–20mA output span in the two-wire, loop-powered mode. If not used for external excitation, the 6.2V reference should be loaded by approximately 1mA (6.2kΩ to common).

USING AN EXTERNAL PASS TRANSISTOR

The emitter of the NPN output section, I_{OUT}, of the AD693 is usually connected to common and the negative loop connection (Pins 7 to 6). Provision has been made to reconnect I_{OUT} to the base of a user supplied NPN transistor as shown in Figure 11. This permits the majority of the power dissipation to be moved off chip to enhance performance, improve reliability, and extend the operating temperature range. An internal hold-down resistor of about 3k is connected across the base emitter of the external transistor.

The external pass transistor selected should have a BV_{CEO} greater than the intended supply voltage with a sufficient power rating for continuous operation with 25mA current at the supply voltage. Ft should be in the 10MHz to 100MHz range and β should be greater than 10 at a 20mA emitter current. Some transistors that meet this criteria are the 2N1711 and 2N2219A. Heat sinking the external pass transistor is suggested.

The pass transistor option may also be employed for other applications as well. For example, I_{OUT} can be used to drive an LED connected to Common, thus providing a local monitor of loop fault conditions without reducing the minimum compliance voltage.

ADJUSTING ZERO

In general, the desired zero offset value is obtained by connecting an appropriate tap of the precision reference/voltage divider network to the inverting terminal of the V/I converter. As shown in Figure 9, precalibrated taps at Pins 14, 13 and 11 result in zero offsets of 0mA, 4mA and 12mA, respectively, when connected to Pin 12. The voltages which set the 4mA and 12mA zero operating points are 15mV and 45mV negative with respect to

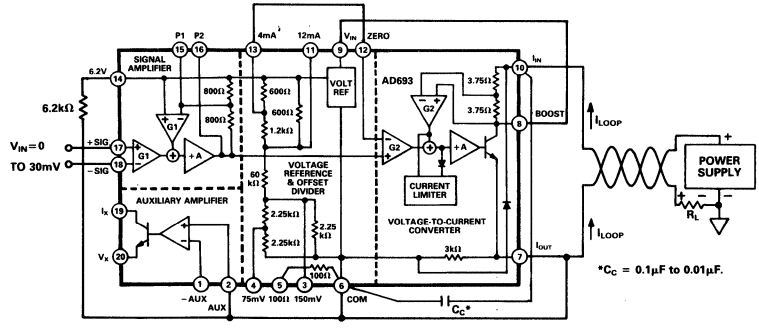


Figure 10. Minimal Connection for 0–30mV Unipolar Input, 4–20mA Output

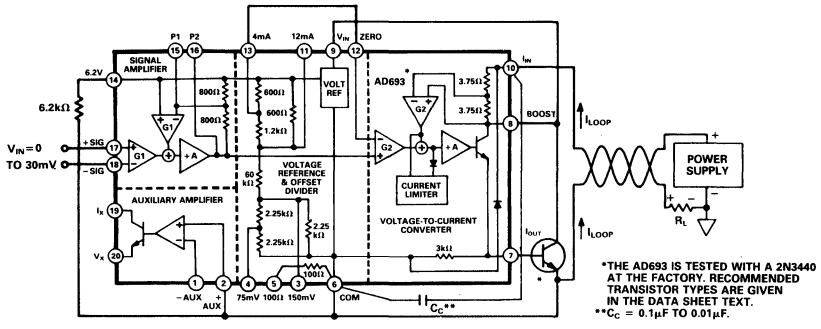


Figure 11. Using an External Pass Transistor to Minimize Self-Heating Errors

6.2V, and they each have a nominal source resistance of 450Ω. While these voltages are laser trimmed to high accuracy, they may require some adjustment to accommodate variability between sensors or to provide additional ranges. You can adjust zero by pulling up or down on the selected zero tap, or by making a separate voltage divider to drive the zero pin.

The arrangement of Figure 12 will give an approximately linear adjustment of the precalibrated options with fixed limits. To find the proper resistor values, first select I_A, the desired range of adjustment of the output current from nominal. Substitute this value in the appropriate formula below for adjustment at the 4mA tap.

$R_{Z1} = (1.6V/I_A) - 400\Omega$and

$R_{Z2} = R_{Z1} \times 3.1V/(15mV + I_A \times 3.75\Omega)$

Use a similar connection with the following resistances for adjustments at the 12mA tap.

$R_{Z1} = (4.8V/I_A) - 400\Omega$ and

$R_{Z2} = R_{Z1} \times 3.1V/(45mV + I_A \times 3.75\Omega)$

These formulae take into account the ±10% tolerance of tap resistance and insure a minimum adjustment range of I_A. For example, choosing I_A = 200μA will give a zero adjustment range of ±1% of the 20mA full-scale output. At the 4mA tap the maximum value of:

$R_{Z1} = 1.6V/200\mu A - 400\Omega = 7.6k\Omega$ and

$R_{Z2} = 7.6k\Omega \times 3.1V/(15mV + 200\mu A \times 3.75\Omega) = 1.49M\Omega$

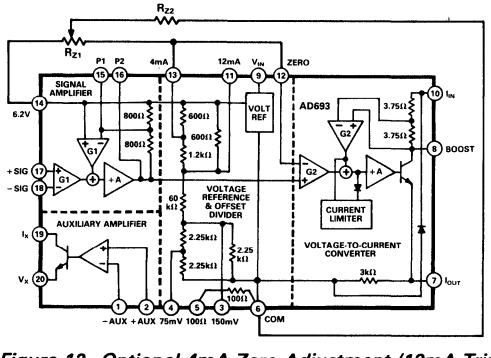


Figure 12. Optional 4mA Zero Adjustment (12mA Trim Available Also)

These can be rounded down to more convenient values of 7.5kΩ and 1.3MΩ, which will result in an adjustment range comfortably greater than ±200μA.

ADJUSTING INPUT SPAN

Input Span is adjusted by changing the gain of the Signal Amplifier. This amplifier provides a 0–to–60mV signal to the V/I section to produce the 4–to–20mA output span (or a 0–to–75mV signal in the 0–to–20mA mode). The gain of this amplifier is trimmed to 2.00 so that an input signal ranging from 0–to–30mV will drive the V/I section to produce 4–to–20mA. Joining P1 and P2 (Pins 15 and 16) will reduce the Signal Amplifier gain to one, thereby requiring a 60mV signal to drive the V/I to a full 20mA span.

To produce spans less than 30mV, an external resistor, R_{S1}, can be connected between P1 and 6.2V. The nominal value is given by:

$$R_{S1} = \frac{400\Omega}{\frac{30mV}{S} - 1}$$

where S is the desired span. For example, to change the span to 6mV a value of:

$$R_{S1} = \frac{400\Omega}{\frac{30mV}{6mV} - 1} = 100\Omega$$

is required. Since the internal, 800Ω gain setting resistors exhibit an absolute tolerance of 10%, R_{S1} should be provided with up to ±10% range of adjustment if the span must be well controlled.

For spans between 30mV and 60mV a resistor R_{S2} should be connected between P1 and P2. The nominal value is given by:

$$R_{S2} = \frac{400\Omega\ (1 - \frac{60mV}{S})}{\frac{30mV}{S} - 1}$$

For example, to change the span to 40mV, a value of:

$$R_{S2} = \frac{400\Omega\ (1 - \frac{60mV}{40mV})}{\frac{30mV}{40mV} - 1} = 800\Omega$$

is required. Remember that this is a nominal value and may require adjustment up to ±10%. In many applications the span must be adjusted to accommodate *individual* variations in the sensor as well as the AD693. The span changing resistor should, therefore, include enough adjustment range to handle both the

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sensor uncertainty and the absolute resistance tolerance of P1 and P2. Note that the temperature coefficient of the internal resistors is nominally −17ppm/°C, and that the external resistors should be comparably stable to insure good temperature performance.

An alternative arrangement, allowing wide range span adjustment between two set ranges, is shown in Figure 13. R_{S1} and R_{S2} are calculated to be 90% of the values determined from the previous formulae. The smallest value is then placed in series with the wiper of the 1.5kΩ potentiometer shown in the figure. For example, to adjust the span between 25mV and 40mV, R_{S1} and R_{S2} are calculated to be 2000Ω and 800Ω, respectively. The smaller value, 800Ω, is then reduced by 10% to cover the possible ranges of resistance in the AD693 and that value is put in place.

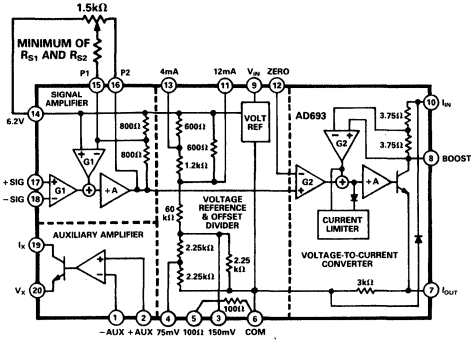


Figure 13. Wide Range Span Adjustment

A number of other arrangements can be used to set the span as long as they are compatible with the pretrimmed noninverting gain of two. The span adjustment can even include thermistors or other sensitive elements to compensate the span of a sensor.

In devising your own adjustment scheme, remember that you should adjust the gain such that the desired span voltage at the Signal Amplifier input translates to 60mV at the output. Note also that the full differential voltage applied to the V/I converter is 75mV; in the 4–20mA mode, −15mV is applied to the inverting input (zero pin) by the Divider Network and +60mV is applied to the noninverting input by the Signal Amplifier. In the 0–20mA mode, the total 75mV must be applied by the Signal Amplifier. As a result, the total span voltage will be 25% larger than that calculated for a 4–20mA output.

Finally, the external resistance from P2 to 6.2V should not be made less than 1kΩ unless the voltage reference is loaded to at least 1.0mA. (A simple load resistor can be used to meet this requirement if a low value potentiometer is desired.) In no case should the resistance from P2 to 6.2V be less than 200Ω.

Input Spans Between 60 and 100mV

Input spans of up to 100mV can be obtained by adding an offset proportional to the output signal into the zero pin of the V/I converter. This can be accomplished with two resistors and adjusted via the optional trim scheme shown in Figure 14. The resistor divider formed by R_{E1} and R_{E2} from the output of the Signal Amplifier modifies the differential input voltage range applied to the V/I converter.

In order to determine the fixed resistor values, R_{E1} and R_{E2}, first measure the source resistance (R_D) of the internal divider network. This can be accomplished (power supply disconnected) by measuring the resistance between the 4mA of offset (Pin 13) and common (Pin 6) with the 6.2V reference (Pin 14) connected to common. The measured value, R_D, is then used to calculate R_{E1} and R_{E2} via the following formula:

$$R_{E2} = R_D\left(\frac{S}{S - 60mV} - 1.0024\right)$$

and $R_{E1} = 412R_{E2}$

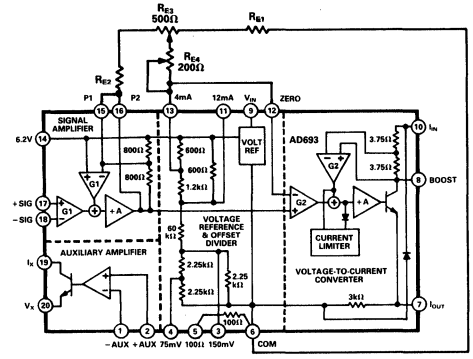


Figure 14. Adjusting for Spans between 60mV and 100mV (R_{E1} and R_{E2}) with Fine-Scale Adjust (R_{E3} and R_{E4})

Figure 14 shows a scheme for adjusting the modified span and 4mA offset via R_{E3} and R_{E4}. The trim procedure is to first connect both signal inputs to the 6.2V Reference, set R_{E4} to zero and then adjust R_{E3} so that 4mA flows in the current loop. This in effect, creates a divider with the same ratio as the internal divider that sets the 4mA zero level (−15mV with respect to 6.2V). As long as the input signal remains zero the voltage at Pin 12, the zero adjust, will remain at −15mV with respect to 6.2V.

After adjusting R_{E3} place the desired full scale (S) across the signal inputs and adjust R_{E4} so that 20mA flows in the current loop. An attenuated portion of the input signal is now added into the V/I zero to maintain the 75mV maximum differential. If there is some small offset at the input to the Signal Amplifier, it may be necessary to repeat the two adjustments.

LOCAL-POWERED OPERATION FOR 0–20mA OUTPUT

The AD693 is designed for local-powered, three-wire systems as well as two-wire loops. All its usual ranges are available in three-wire operation, and in addition, the 0–20mA range can be used. The 0–20mA convention offers slightly more resolution and may simplify the loop receiver, two reasons why it is sometimes preferred.

The arrangement, illustrated in Figure 15, results in a 0–20mA transmitter where the precalibrated span is 37.5mV. Connecting P1 to P2 will double the span to 75mV. Sensor input and excitation is unchanged from the two-wire mode except for the 25% increase in span. Many sensors are ratiometric so that an increase in excitation can be used instead of a span adjustment.

In the local-powered mode, increases in excitation are made easier. Voltage compliance at the I_{IN} terminal is also improved; the loop voltage may be permitted to fall to 6 volts at the AD693, easing the trade-off between loop voltage and loop resistance. Note that the load resistor, R_L, should meter the current into Pin 10, I_{IN}, so as not to confuse the loop current with the local power supply current.

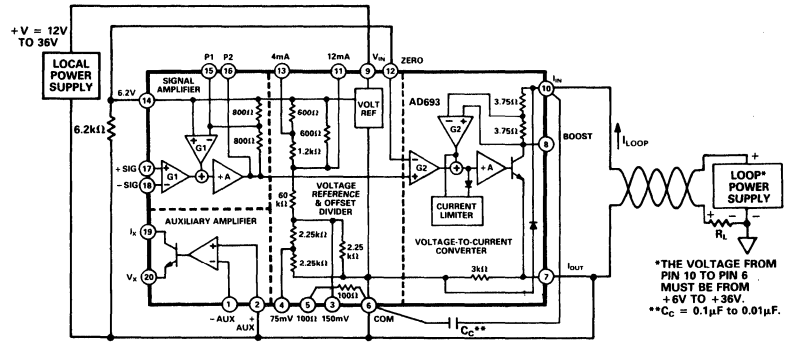


Figure 15. Local Powered Operation with 0–20mA Output

OPTIONAL INPUT FILTERING

Input filtering is recommended for all applications of the AD693 due to its low input signal range. An RC filter network at each input of the signal amplifier is sufficient, as shown in Figure 16. In the case of a resistive signal source it may be necessary only to add the capacitors, as shown in Figure 18. The capacitors should be placed as close to the AD693 as possible. The value of the filter resistors should be kept low to minimize errors due to input bias current. Choose the 3dB point of the filter high enough so as not to compromise the bandwidth of the desired signal. The RC time constant of the filter should be matched to preserve the ac common-mode rejection.

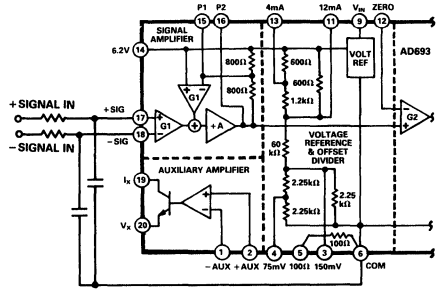


Figure 16. Optional Input Filtering

INTERFACING PLATINUM RTDs

The AD693 has been specially configured to accept inputs from 100Ω Platinum RTDs (Resistance Temperature Detectors). Referring to Figure 17, the RTD and the temperature stable 100Ω resistor form a feedback network around the Auxiliary Amplifier resulting in a noninverting gain of $(1+R_T/100\Omega)$, where R_T is the temperature dependent resistance of the RTD. The noninverting input of the Auxiliary Amplifier (Pin 2) is then driven by the 75mV signal from the Voltage Divider (Pin 4). When the RTD is at 0, its 100Ω resistance results in an amplifier gain of +2 causing V_X to be 150mV. The Signal Amplifier compares this voltage to the 150mV output (Pin 3) so that zero differential signal results. As the temperature (and therefore, the resistance) of the RTD increases, V_X will likewise increase according to the gain relationship. The difference between this voltage and the zero degree value of 150mV drives the Signal Amp to modulate the loop current. The AD693 is pre-calibrated such that the full 4–20mA output span corresponds to a 0 to 104°C range in the RTD. (This assumes the European Standard of $\alpha = 0.00385$.) A total of 6 precalibrated ranges for three-wire (or two-wire) RTDs are available using only the pin strapping options as shown in Table I.

A variety of other temperature ranges can be realized by using different application voltages. For example, loading the Voltage Divider with a 1.5kΩ resistor from Pin 3 to Pin 6 (common) will approximately halve the original application voltages and

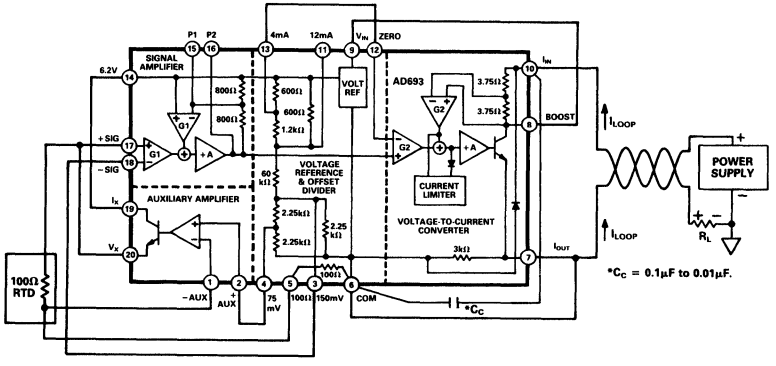


Figure 17. 0-to-104°C Direct Three-Wire 100Ω RTD Interface, 4–20mA Output

Temperature Range	Pin Connections
0 to +104°C	12 to 13
0 to +211°C	12 to 13, and 15 to 16
+25°C to +130°C	12 to 14
+51°C to +266°C	12 to 14, and 15 to 16
–50°C to +51°C	12 to 11
–100°C to +104°C	12 to 11 and 15 to 16

Table I. Precalibrated Temperature Range Options Using a European Standard 100Ω RTD and the AD693

allow for a doubling of the range of resistance (and therefore, temperature) required to fill the two standard spans. Likewise, increasing the application voltages by adding resistance between Pins 14 and 3 will decrease the temperature span.

An external voltage divider may also be used in conjunction with the circuit shown to produce any range of temperature spans as well as providing zero output (4mA) for a non 0 temperature input. For example, measuring V_X with respect to a voltage 2.385 times the excitation (rather than 2 times) will result in zero input to the Signal Amplifier when the RTD is at 100°C (or 138.5Ω).

As suggested in Table I, the temperature span may also be adjusted by changing the voltage span of the Signal Amplifier. Changing the gain from 2 to 4, for example, will halve the temperature span to about 52°C on the 4–20mA output configuration. (See section "Adjusting Input Span".)

The configuration for a three-wire RTD shown in Figure 17 can accommodate two-wire sensors by simply joining Pins 1 and 5 of the AD693.

INTERFACING LOAD CELLS AND METAL FOIL STRAIN GAGES

The availability of the on-chip Voltage Reference, Auxiliary Amplifier and 3mA of excitation current make it easy to adapt the AD693 to a variety of load cells and strain gages.

The circuit shown in Figure 18 illustrates a generalized approach in which the full flexibility of the AD693 is required to interface to a low resistance bridge. For a high impedance transducer the bridge can be directly powered from the 6.2V Reference.

Component values in this example have been selected to match the popular standard of 2mV/V sensitivity and 350Ω bridge resistance. Load cells are generally made for either tension and compression, or compression only; use of the 12mA zero tap allows for operation in the tension and compression mode. An optional zero adjustment is provided with values selected for ±2% FS adjustment range.

Because of the low resistance of most foil bridges, the excitation voltage must be low so as not to exceed the available 4mA zero current. About 1V is derived from the 6.2V Reference and an external voltage divider; the Aux-Amp is then used as a follower to make a stiff drive for the bridge. Similar applications with higher resistance sensors can use proportionally higher voltage.

Finally, to accommodate the 2mV/V sensitivity of the bridge, the full-scale span of the Signal Amplifier must be reduced. Using the load cell in both tension and compression with 1V of excitation, therefore, dictates that the span be adjusted to 4mV. By substituting in the expression, $R_{S1} = 400\Omega/[(30mV/S) - 1]$, the nominal resistance required to achieve this span is found to be 61.54Ω. Calculate the minimum resistance required by subtracting 10% from 61.54Ω to allow for the internal resistor tolerance of the AD693, leaving 55.38Ω (See "Adjusting Input Span".) The standard value of 54.9Ω is used with a 20Ω potentiometer for full-scale adjustment.

If a load cell with a precalibrated sensitivity constant is to be used, the resultant full-scale span applied to the Signal Amplifier is found by multiplying that sensitivity by the excitation voltage. (In Figure 18, the excitation voltage is actually (10kΩ/62.3kΩ) (6.2V) = 0.995V).

THERMOCOUPLE MEASUREMENTS

The AD693 can be used with several types of thermocouple inputs to provide a 4–20mA current loop output corresponding to a variety of measurement temperature ranges. Cold junction compensation (CJC) can be implemented using an AD592 or AD590 and a few external resistors as shown in Figure 19.

From Table II simply choose the type of thermocouple and the appropriate average reference junction temperature to select values for R_{COMP} and R_Z. The CJC voltage is developed across R_{COMP} as a result of the AD592 1μA/K output and is added to the thermocouple loop voltage. The 50Ω potentiometer is biased by R_Z to provide the correct zero adjustment range appropriate for the divider and also translates the Kelvin scale of the AD592 to °Celsius. To calibrate the circuit, put the thermocouple in an ice bath (or use a thermocouple simulator set to 0) and adjust the potentiometer for a 4mA loop current.

The span of the circuit in °C is determined by matching the signal amplifier input voltage range to it's temperature equivalent

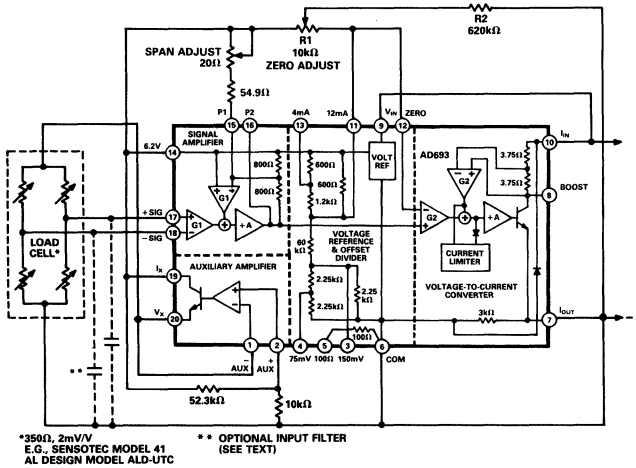


Figure 18. Utilizing the Auxiliary Amplifier to Drive a Load Cell, 12mA ±8mA Output

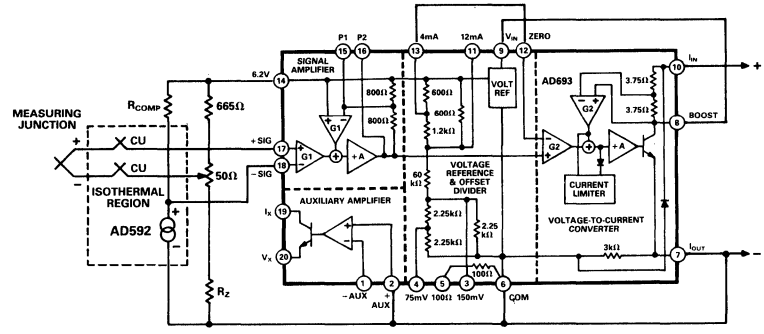


Figure 19. Thermocouple Inputs with Cold Junction Compensation

POLARITY	MATERIAL	TYPE	AMBIENT TEMP	RCOMP	RZ	30mV TEMP RANGE	60mV TEMP RANGE
+	IRON	J	25°	51.7Ω	301K	546°C	1035°C
−	CONSTANTAN		75°	53.6Ω	294K		
+	NICKEL-CHROME	K	25°	40.2Ω	392K	721°C	—
−	NICKEL-ALUMINUM		75°	42.2Ω	374K		
+	NICKEL-CHROME	E	25°	60.4Ω	261K	413°C	787°C
−	COPPER-NICKEL		75°	64.9Ω	243K		
+	COPPER	T	25°	40.2Ω	392K	USE WITH GAIN>2	
−	COPPER-NICKEL		75°	45.3Ω	340K		

Table II. Thermocouple Application – Cold Junction Compensation Table

via a set of thermocouple tables referenced to °C. For example, the output of a properly referenced type J thermocouple is 60mV when the hot junction is at 1035°C. Table II lists the maximum measurement temperature for several thermocouple types using the preadjusted 30mV and 60mV input ranges.

More convenient temperature ranges can be selected by determining the full-scale input voltages via standard thermocouple tables and adjusting the AD693 span. For example, suppose only a 300°C span is to be measured with a type K thermocouple. From a standard table, the thermocouple output is 12.207mV; since 60mV at the signal amplifier corresponds to a 16mA span at the output a gain of 5, or more precisely 60mV/12.207mV = 4.915 will be needed. Using a 12.207mV span in the gain resistor formula given in "Adjusting Input Span" yields a value of about 270Ω as the minimum from P1 to 6.2V. Adding a 50Ω potentiometer will allow ample adjustment range.

With the connection illustrated, the AD693 will give a full-scale indication with an open thermocouple.

ERROR BUDGET ANALYSIS

Loop-Powered Operation specifications refer to parameters tested with the AD693 operating as a loop-powered transmitter. The specifications are valid for the preset spans of 30mV, 60mV and those spans in between. The section, "Components of Error", refers to parameters tested on the individual functional blocks, (Signal Amplifier, V/I Converter, Voltage Reference, and Auxiliary Amplifier). These can be used to get an indication of device performance when the AD693 is used in local power mode or when it is adjusted to spans of less than 30mV.

Table III lists the expressions required to calculate the total error. The AD693 is tested with a 250Ω load, a 24V loop supply

RTI Contributions to Offset Error

	Error Source	Expression for RTI Error at Zero
I_{ZE}	Zero Current Error	I_{ZE}/X_S
PSRR	Power Supply Rejection Ratio	$(\|V_{LOOP} - 24V\| + [\|R_L - 250\Omega\| \times I_Z]) \times PSRR$
CMRR	Common-Mode Rejection Ratio	$\|V_{CM} - 3.1V\| \times CMRR$
IOS	Input Offset Current	$R_S \times IOS$

RTI Contributions to Span Error

	Error Source	Expression for RTI Error at Full Scale
X_{SE}	Transconductance Error	$V_{SPAN} \times X_{SE}$
X_{PSRR}	Transconductance PSRR[1]	$\|R_L - 250\Omega\| \times I_S \times PSRR$
X_{CMRR}	Transconductance CMRR	$\|V_{CM} - 3.1V\| \times V_{SPAN} \times X_{CMRR}$
X_{NL}	Nonlinearity	$V_{SPAN} \times X_{NL}$
I_{DIFF}	Differential Input Current[2]	$R_S \times I_{DIFF}$

Abbreviations

I_Z	Zero Current (usually 4mA)
I_S	Output span (usually 16mA)
R_S	Input source impedance
R_L	Load resistance
V_{LOOP}	Loop supply voltage
V_{CM}	Input common-mode voltage
V_{SPAN}	Input span
X_S	Nominal transconductance in A/V

[1]The 4-20mA signal, flowing through the metering resistor, modulates the power supply voltage seen by the AD693. The change in voltage causes a power supply rejection error that varies with the output current, thus it appears as a span error.

[2]The input bias current of the inverting input increases with input signal voltage. The differential input current, I_{DIFF}, equals the inverting input current minus the noninverting input current; see Figure 2. I_{DIFF}, flowing into an input source inpedance, will cause an input voltage error that varies with signal. If the change in differential input current with input signal is approximated as a linear function, then any error due to source impedance may be approximated as a span error. To calculate I_{DIFF}, refer to Figure 2 and find the value for I_{DIFF}/+In corresponding to the full-scale input voltage for your application. Multiply by +In max to get I_{DIFF}. Multiply I_{DIFF} by the source impedance to get the input voltage error at full scale.

Table III. RTI Contributions to Span and Offset Error

and an input common-mode voltage of 3.1V. The expressions below calculate errors due to deviations from these nominal conditions.

The total error at zero consists only of offset errors. The total error at full scale consists of the offset errors plus the span errors. Adding the above errors in this manner may result in an error as large as 0.8% of full scale, however, as a rule, the AD693 performs better as the span and offset errors do not tend to add worst case. The specification "Total Unadjusted Error", (TUE), reflects this and gives the maximum error as a % of full scale for any point in the transfer function when the device is operated in one of its preset spans, with no external trims. The TUE is less than the error you would get by adding the span and offset errors worst case.

Thus, an alternative way of calculating the total error is to start with the TUE and add to it those errors that result from operation of the AD693 with a load resistance, loop supply voltage, or common-mode input voltage different than specified. (See Example 1 below.)

ERROR BUDGET FOR SPANS LESS THAN 30mV

An accommodation must be made to include the input voltage offset of the signal amplifier when the span is adjusted to less than 30mV. The TUE and the Zero Current Error include the input offset voltage contribution of the signal amplifier in a gain of 2. As the input offset voltage is multiplied by the gain of the signal amplifier, one must include the additional error when the signal amplifier is set to gains greater than 2.

For example, the 300K span thermocouple application discussed previously requires a 12.207mV input span; the signal amplifier must be adjusted to a gain of approximately 5. The loop transconductance is now 1.333 A/V, (5 × 0.2666 A/V). Calculate the total error by substituting the new values for the transconductance and span into the equations in Table III as was done in Example I. The error contribution due to V_{OS} is $5 \times V_{OS}$, however, since $2 \times V_{OS}$ is already included in the TUE and the Zero Current Error it is necessary to add an error of only $(5-2) \times V_{OS}$ to the error budget. Note that span error may by reduced to zero with the span trim, leaving only the offset and nonlinearity of the AD693.

EXAMPLE I

The AD693 is configured as a 4-20mA loop powered transmitter with a 60mV FS input. The inputs are driven by a differential voltage at 2V common mode with a 300Ω balanced source resistance. A 24V loop supply is used with a 500Ω metering resistance. (See Table IV below.)

Trimming the offset and span for your application will remove all span and offset errors except the nonlinearity of the AD693.

OFFSET ERRORS		
I_Z	Already included in the TUE spec.	0.0μV
PSRR	PSRR = 5.6μV/V; (|24V − 24V| + [|500Ω − 250Ω| × 4mA]) × 5.6μV/V = V_{LOOP} = 24V R_L = 500Ω I_Z = 4mA	5.6μV
CMRR	CMRR = 30μV/V; |2V − 3.1V| × 30μV/V = V_{CM} = 2V	33.0μV
IOS	IOS = ±3nA, R_S = 300Ω; 300Ω × 3nA =	0.9μV
Total Additional Error at 4mA		**39.5μV**
As % of full scale; (39.5μV × 0.2666 A/V)/20mA × 100% =		0.053% of FS
SPAN ERRORS		
X_{SE}	Already included in the TUE spec.	0.0μV
X_{PSRR}	PSRR = 5.6μV/V; (|500Ω − 250Ω| × 16mA) × 5.6μV/V = R_L = 500Ω, I_S = 16mA	22.4μV
X_{CMRR}	X_{CMRR} = 0.06%/V; |2V − 3.1V| × 60mV × 0.06%/V = V_{CM} = 2V, V_{SPAN} = 60mV	39.6μV
I_{DIFF}	V_{SPAN} = +60mV; 300Ω × 2 × 20nA I_{DIFF}/+In = 2 from Figure 2)	12.0μV
X_{NL}	Already included in the TUE	0.0μV
Total Additional Span Error at Full Scale		**74.0μV**
Total Additional Error at Full Scale; $\epsilon_{OFFSET} + \epsilon_{SPAN}$ = 39.5μV + 74.0μV =		113.5μV
As % of Full Scale; (113.5μV × 0.2666 A/V)/20mA × 100% =		0.151% of FS
New Total Unadjusted Error @ FS; $\epsilon_{TUE} + \epsilon_{ADDITIONAL}$ = 0.5% + 0.151% =		**0.651% of FS**

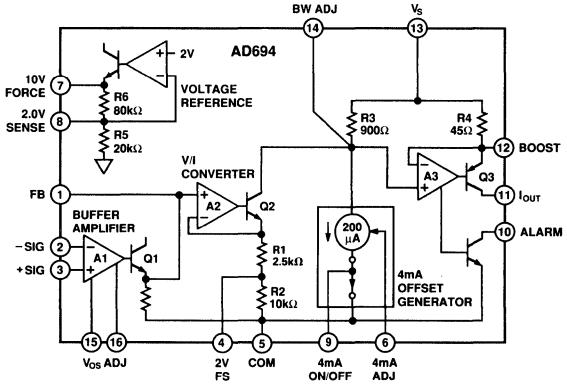
Table IV. Example 1

4–20 mA Transmitter

AD694*

FEATURES
4–20 mA, 0–20 mA Output Ranges
Precalibrated Input Ranges:
0 V to 2 V, 0 V to 10 V
Precision Voltage Reference
Programmable to 2.000 V or 10.000 V
Single or Dual Supply Operation
Wide Power Supply Range: +4.5 V to +36 V
Wide Output Compliance
Input Buffer Amplifier
Open-Loop Alarm
Optional External Pass Transistor to Reduce Self-Heating Errors
0.002% typ Nonlinearity

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD694 is a monolithic current transmitter that accepts high level signal inputs to drive a standard 4–20 mA current loop for the control of valves, actuators, and other devices commonly used in process control. The input signal is buffered by an input amplifier that can be used to scale the input signal or buffer the output from a current mode DAC. Precalibrated input spans of 0 V to 2 V and 0 V to 10 V are selected by simple pin strapping; other spans may be programmed with external resistor.

The output stage compliance extends to within 2 V of V_S and its special design allows the output voltage to extend below common in dual supply operation. An alarm warns of an open 4 to 20 mA loop or noncompliance of the output stage.

Active laser trimming of the AD694's thin film resistors results in high levels of accuracy without the need for additional adjustments and calibration. An external pass transistor may be used with the AD694 to off-load power dissipation, extending the temperature range of operation.

The AD694 is the ideal building block for systems requiring noise immune 4–20 mA signal transmission to operate valves, actuators, and other control devices, as well as for the transmission of process parameters such as pressure, temperature, or flow. It is recommended as a replacement for discrete designs in a variety of applications in industrial process control, factory automation, and system monitoring.

The AD694 is available in hermetically sealed, 16-pin cerdip and plastic SOIC, specified over the −40°C to +85°C industrial temperature range, and in a 16-pin plastic DIP, specified over the 0 to +70°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD694 is a complete voltage in to 4–20 mA out current transmitter.
2. Pin programmable input ranges are pre-calibrated at 0 V to 2 V and 0 V to 10 V.
3. The input amplifier may be configured to buffer and scale the input voltage, or to serve as an output amplifier for current output DACs.
4. The output voltage compliance extends to within 2 V of the positive supply and below common. When operated with a 5 V supply, the output voltage compliance extends 30 V below common.
5. The AD694 interfaces directly to 8-, 10-, and 12-bit single supply CMOS and bipolar DACs.
6. The 4 mA zero current may be switched on and off with a TTL control pin, allowing 0–20 mA operation.
7. An open collector alarm warns of loop failure due to open wires or noncompliance of the output stage.
8. A monitored output is provided to drive an external pass transistor. The feature off-loads power dissipation to extend the temperature range of operation and minimize self-heating error.

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*Protected by U.S. Patents: 30,586; 4,250,445; 4,857,862.

AD694—SPECIFICATIONS (@ +25°C, R_L = 250 Ω and V_S = +24 V, unless otherwise noted)

Model	AD694JN/AQ/AR			AD694BQ/BR			Units
	Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS							
Input Voltage Range	−0.2	V_S−2.0V	**V_S−2.5 V**	−0.2	V_S−2.0 V	**V_S−2.5 V**	V
Input Bias Current							
Either Input, T_{min} to T_{max}		1.5	**5**		1.5	**5**	nA
Offset Current, T_{min} to T_{max}		±0.1	**±1**		±0.1	**±1**	nA
Offset Current Drift		±1.0	±5.0		±1.0	±5.0	pA/°C
Input Impedance	5			5			MΩ
OUTPUT CHARACTERISTICS							
Operating Current Range	0		23	0		23	mA
Specified Performance	4		20	4		20	mA
Output Voltage Compliance	**V_S−36 V**		**V_S−2 V**	**V_S−36 V**		**V_S−2 V**	V
Output Impedance, 4–20 mA	40.0	50.0		40.0	50.0		MΩ
Current Limit @ 2× FS Overdrive	**24**		**44**	**24**		**44**	mA
Slew Rate		1.3			1.3		mA/μs
SPAN AND ZERO ACCURACY[1]							
4 mA Offset Error @ 0 V Input[2]							
Error from 4.000 mA, 4 mA On		±10	**±20**		±5	**±10**	μA
Error from 0.000 mA, 4 mA Off	0	+10	**+20**	0	+5	**+10**	μA
T_{min} to T_{max}		±10	**±40**		±5	**±20**	μA
vs. Supply (2 V Span/10 V Span)		0.3/0.05	**0.8/0.4**		0.3/0.05	**0.8/0.4**	μA/V
Trim Range, 4 mA Zero	2.0		4.8	2.0		4.8	mA
Span							
Nominal Transfer Function							
Input FS = 2 V		8.0			8.0		mA/V
Input FS = 10 V		1.6			1.6		mA/V
Transfer Function Error from Nom,							
Input FS = 2 V, 10 V		±0.1	**±0.3**		±0.05	**±0.15**	% of Span
T_{min} to T_{max}		±0.002	±0.005		±0.001	**±0.0025**	% of Span/°C
vs. Supply		±0.001	**±0.005**		±0.001	**±0.005**	% of Span/V
Nonlinearity[3]		±0.005	**±0.015**		±0.001	**±0.005**	% of Span
4 mA On: Max Pin 9 Voltage			0.8			0.8	V
4 mA Off: Min Pin 9 Voltage	3.0	2.5		3.0	2.5		V
VOLTAGE REFERENCE							
Output Voltage: 10 V Reference	**9.960**	10.000	**10.040**	**9.980**	10.000	**10.020**	V
Output Voltage: 2 V Reference	**1.992**	2.000	**2.008**	**1.996**	2.000	**2.004**	V
T_{min} to T_{max}[4]		30	**50**		20	**30**	ppm/°C
vs. Load, V_{REF} = 2 V, 10 V		0.15	**0.50**		0.15	**0.50**	mV/mA
vs. Supply, V_{REF} = 2 V, 10 V		±0.001	**±0.005**		±0.001	**±0.005**	%/V
Output Current							
Source	5			5			mA
Sink		0.2			0.2		mA
ALARM CHARACTERISTICS							
$V_{CE(SAT)}$ @ 2.5 mA		0.35			0.35		V
Leakage Current			**±1**			**±1**	μA
Alarm Pin Current (Pin 10)		20			20		mA
POWER REQUIREMENTS							
Specified Performance		24			24		V
Operating Range							
2 V FS, V_{REF} = 2 V	**4.5**		**36**	**4.5**		**36**	V
2 V, 10 V FS, V_{REF} = 2 V, 10 V	**12.5**		**36**	**12.5**		**36**	V
Quiescent Current, 4 mA Off		1.5	**2.0**		1.5	**2.0**	mA
TEMPERATURE RANGE							
Specified Performance[5] AD694AQ/BQ/AR/BR	−40		+85	−40		+85	°C
AD694JN	0		+70	0		+70	°C
Operating AD694AQ/BQ/AR/BR	−55		+125	−55		+125	°C
AD694JN	−40		+85	−40		+85	°C

Model	AD694JN/AQ/AR Min	Typ	Max	AD694BQ/BR Min	Typ	Max	Units
BUFFER AMPLIFIER[6]							
Input Offset Voltage							
Initial Offset		±150	**±500**		±50	**±500**	μV
T_{min} to T_{max}		±2	±3		±2	±3	μV/°C
vs. Supply	80	90		80	90		dB
vs. Common Mode	80	90		80	90		dB
Trim Range	**±2.5**	±4.0		**±2.5**	±4.0		mV
Frequency Response							
Unity Gain, Small Signal		300			300		kHz
Input Voltage Noise (0.1 to 10 Hz)		2			2		μV p–p
Open-Loop Gain							
V_O = +10 V, $R_L \geq 10$ kΩ		50			50		V/mV
Output Voltage @ Pin 1, FB[1]							
Minimum Output Voltage		1.0	10		1.0	10	mV
Maximum Output Voltage	V_S–2.5 V	V_S–2 V		V_S–2.5 V	V_S–2 V		V

NOTES
[1]The single supply op amps of the AD694, lacking pull down current, may not reach 0.000 V at their outputs. For this reason, span, offset, and nonlinearity are specified with the input amplifiers operating in their linear range. The input voltage used for the tests is 5 mV to 2 V and 5 mV to 10 V for the two pre-calibrated input ranges. Span and zero accuracy are tested with the buffer amplifier configured as a follower.
[2]Offset at 4 mA out and 0 mA out are extrapolated to 0.000 V input from measurements made at 5 mV and at full scale. See Note 1.
[3]Nonlinearity is specified as the maximum deviation of the output, as a % of span, from a straight line drawn through the endpoints of the transfer function.
[4]Voltage reference drift guaranteed by the Box Method. The voltage reference output over temperature will fall inside of a box whose length is determined by the temperature range and whose height is determined by the maximum temperature coefficient multiplied by the temperature span in degrees C.
[5]Devices tested at these temperatures with a pass transistor. Allowable temperature range of operation is dependent upon internal power dissipation. Absolute maximum junction and case temperature should not be exceeded. See section: "Power Dissipation Considerations."
[6]Buffer amplifier specs for reference. Buffer amplifier offset and drift already included in Span and Zero accuracy specs above.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +36 V
V_S to I_{OUT} . . . . . +36 V
Input Voltage, (Either Input Pin 2 or 3) . . . . −0.3 V to +36 V
Reference Short Circuit to Common . . . . . Indefinite
Alarm Voltage, Pin 10 . . . . . +36 V
4 mA Adj, Pin 6 . . . . . +1 V
4 mA On/Off, Pin 9 . . . . . 0 V to 36 V
Storage Temperature Range
AD694Q . . . . . −65°C to +150°C
AD694N, R . . . . . −65°C to +125°C
Lead Temperature, 10 sec Soldering . . . . . +300°C
Maximum Junction Temperature . . . . . +150°C
Maximum Case Temperature
Plastic Package (N, R) . . . . . +125°C
Cerdip Package (Q) . . . . . +125°C

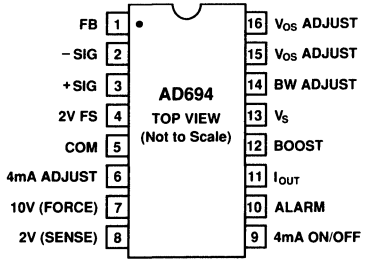
Transistor Count: . . . . . 75 Active Devices
Substrate Connection: . . . . . to Com, Pin 5

Thermal Characteristics:
Plastic (N) Package: θ_{JC} = 50°C/Watt
θ_{CA} (Still Air) = 85°C/Watt
Cerdip (Q) Package: θ_{JC} = 30°C/Watt
θ_{CA} (Still Air) = 70°C/Watt
Plastic (R) Package: θ_{JC} = 27°C/Watt
θ_{CA} (Still Air) = 73°C/Watt

ESD Susceptibility
All pins are rated for a minimum of 4000 V protection, except for Pins 2, 3 and 9 which are rated to survive a minimum of 1500 V. ESD testing conforms to Human Body Model. Always practice ESD prevention.

No pin, other than I_{OUT} (11) and ±Sig (2), (3) as noted, may be permitted to become more negative than Com (5). No pin may be permitted to become more positive than V_S (13).

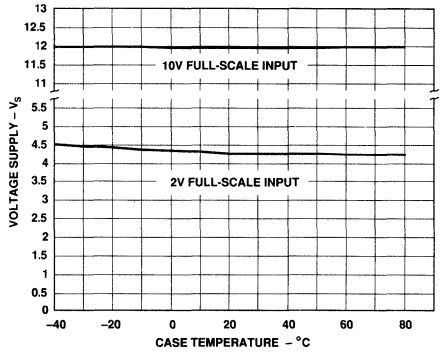
PIN CONFIGURATION (N, R, Q Package)



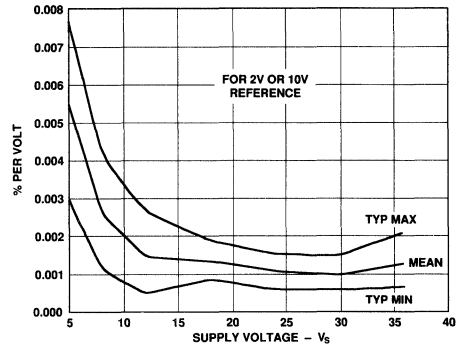
ORDERING GUIDE

Model	Temperature Range	Package Options*
AD694JN	0°C to +70°C	N-16
AD694AQ	−40°C to +85°C	Q-16
AD694AR	−40°C to +85°C	R-16
AD694BQ	−40°C to +85°C	Q-16
AD694BR	−40°C to +85°C	R-16

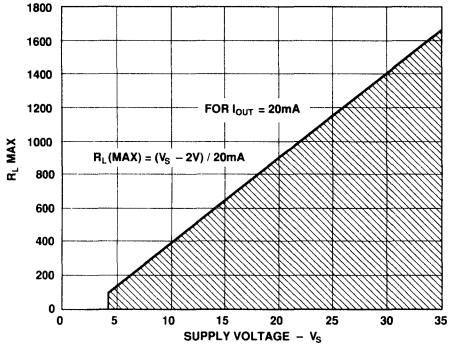
*N = Plastic DIP; Q = Cerdip; R = SOIC. For outline information see Package Information section.



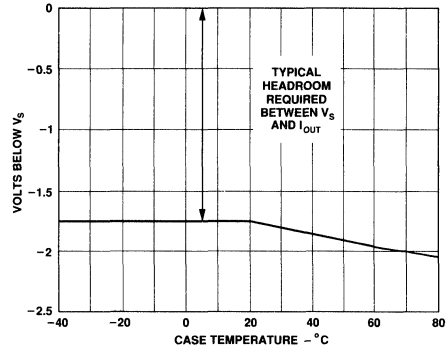
Typical Minimum Supply Voltage vs. Temperature for 2 V & 10 V Full Scale



Voltage Reference Power Supply Rejection



Maximum R_L vs. Supply Voltage



I_{OUT}: Voltage Compliance vs. Temperature

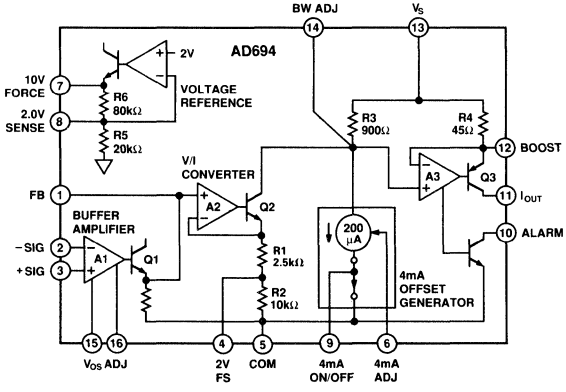


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

The operation of the AD694 can best be understood by dividing the circuit into three functional parts (see Figure 1). First, a single supply input amplifier buffers the high level, single-ended input signal. The buffer amplifier drives the second section, a voltage to current (V/I) converter, that makes a 0 to 16 mA signal dependent current.

The third section, a voltage reference and offset generator, is responsible for providing the 4 mA offset current signal.

BUFFER AMPLIFIER

The buffer amplifier is a single supply amplifier that may be used as a unity gain buffer, an output amplifier for a current output D/A converter, or as a gain block to amplify low level signals. The amplifier's PNP input stage has a common-mode range that extends from a few hundred mV below ground to within 2.5 V of V_S. The Class A output of the amplifier appears at Pin 1 (FB). The output range extends from about 1 mV above common to within 2.5 V of V_S when the amplifier is operated as a follower. The amplifier can source a maximum load of 5 kΩ, but can sink only as much as its internal 10 kΩ pull-down resistor allows.

V/I CONVERTER

The ground referenced, input signal from the buffer amplifier is converted to a 0 to 0.8 mA current by A2 and level shifted to the positive supply. A current mirror then multiplies this signal by a factor of 20 to make the signal current of 0 to 16 mA. This technique allows the output stage to drive a load to within 2 V of the positive supply (V_S). Amplifier A2 forces the voltage at Pin 1 across resistors R1 and R2 by driving the Darlington transistor, Q2. The high gain Darlington transmits the resistor current to its collector and to R3 (900 Ω). A3 forces the level shifted signal across the 45 Ω resistor to get a current gain of 20. The transfer function of the V/I stage is therefore:

$$I_{OUT} = (20 \times V_{(PIN1)}) / (R1 + R2)$$

resulting in a 0–16 mA output swing for a 0–10 V input. Tying Pin 4 (2 V FS) to ground shorts out R2 and results in a 2 V full-scale input for a 16 mA output span.

The output stage of the V/I converter is of a unique design that allows the I_{OUT} pin to drive a load below the common (substrate) potential of the device. The output transistor can always drive a load to a point 36 V below the positive supply (V_S). An optional NPN pass transistor can be added to transfer most of the power dissipation off-chip, to extend the temperature range of operation.

The output stage is current-limited at approximately 38 mA to protect the output from an overdrive at its inputs. The V/I will allow linear operation to approximately 24 mA. The V/I converter also has an open collector alarm (Pin 10) which warns of open-circuit condition at the I_{OUT} pin or of attempts to drive the output to a voltage greater than V_S −2 V.

4 mA OFFSET GENERATOR

This circuit converts a constant voltage from the voltage reference to a constant current of approximately 200 μA. This current is summed with the signal current at Pin 14 (BW Adjust), to result in a constant 4 mA offset current at I_{OUT}. The 4 mA Adj (Pin 6) allows the offset current to be adjusted to any current in the range of 2 mA to 4.8 mA. Pin 9 (4 mA On/Off) can shut off the offset current completely if it is lifted to 3.0 V or more, allowing 0 to 20 mA operation of the AD694. In normal 4–20 mA operation, Pin 9 is connected to ground.

VOLTAGE REFERENCE

A 2 V or 10 V voltage reference is available for user applications, selectable by pin-strapping. The 10 V option is available for supply voltages greater than 12.5 V, the 2 V output is available over the whole 4.5 V – 36 V power supply range. The reference can source up to 5 mA for user applications. A boost transistor can be added to increase the current drive capability of the 2 V mode.

APPLYING THE AD694

The AD694 can easily be connected for either dual or single supply operation, to operate from supplies as low as 4.5 V and as high as 36 V. The following sections describe the different connection configurations, as well as adjustment methods. Table I shows possible connection options.

Table I. Precalibrated Ranges for the AD694

Input Range	Output Range	Voltage Reference	Min V_S	Pin 9	Pin 4	Pin 8
0–2 V	4–20 mA	2 V	4.5 V	Pin 5	Pin 5	Pin 7
0–10 V	4–20 mA	2 V	12.5 V	Pin 5	Open	Pin 7
0–2.5 V	0–20 mA	2 V	5.0 V	≥3 V	Pin 5	Pin 7
0–12.5 V	0–20 mA	2 V	15.0 V	≥3 V	Open	Pin 7
0–2 V	4–20 mA	10 V	12.5 V	Pin 5	Pin 5	Open
0–10 V	4–20 mA	10 V	12.5 V	Pin 5	Open	Open
0–2.5 V	0–20 mA	10 V	12.5 V	≥3 V	Pin 5	Open
0–12.5 V	0–20 mA	10 V	15.0 V	≥3 V	Open	Open

BASIC CONNECTIONS: 12.5 V SINGLE SUPPLY OPERATION WITH 10 V FS

Figure 2 shows the minimal connections required for basic operation with a +12.5 V power supply, 10 V input span, 4–20 mA output span, and a 10 V voltage reference. The buffer amplifier is connected as a voltage follower to drive the V/I converter by connecting FB (Pin 1) to −Sig (Pin 2). 4 mA On/Off (Pin 9) is tied to ground (Pin 5) to enable the 4 mA offset current. The AD694 can drive a maximum load $R_L = [V_S - 2\text{ V}] / 20\text{ mA}$, thus the maximum load with a 12.5 V supply is 525 Ω.

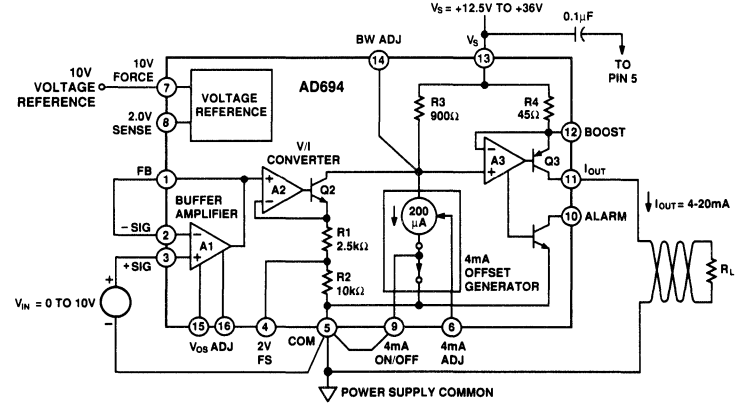


Figure 2. Minimal Connections for 0–10 V Single-Ended Input, 4–20 mA Output, 10 V Reference Output

SELECTING A 2 V FULL-SCALE INPUT

The 2 V full-scale option is selected by shorting Pin 4 (2 V FS) to Pin 5 (Common). The connection should be as short as possible; any parasitic resistance will affect the precalibrated span accuracy.

SELECTING THE 2 V VOLTAGE REFERENCE

The voltage reference is set to a 2 V output by shorting Pin 7 to Pin 8 (10 V Force to 2 V Sense). If desired, the 2 V reference can be set up for remote force and sense connection. Keep in mind that the 2 V Sense line carries a constant current of 100 μA that could cause an offset error over long wire runs. The 2 V reference option can be used with all supply voltages greater than 4.5 V.

An NPN boost transistor can be added in the 2 V mode to increase the current drive capability of the 2 V reference. The 10 V force pin is connected to the base of the NPN, and the NPN emitter is connected to the 2 V sense pin. The minimum V_S of the part increases by approximately 0.7 V.

4.5 V SINGLE SUPPLY OPERATION

For operation with a +4.5 V power supply, the input span and the voltage reference output must be reduced to give the amplifiers their required 2.5 V of head room for operation. This is done by adjusting the AD694 for 2 V full-scale input, and a voltage reference output of 2 V as described above.

GENERAL DESIGN GUIDELINES

A 0.1 μF decoupling capacitor is recommended in all applications from V_S (Pin 13) to Com (Pin 5). Additional components may be required if the output load is nonresistive, see section on driving nonresistive loads. The buffer amplifier PNP inputs should not be brought more than −0.3 V of common, or they will begin to source large amounts of current. Input protection resistors must be added to the inputs if there is a danger of this occurring. The output of the buffer amplifier, Pin 1 (FB), is not short circuit protected. Shorting this pin to ground or V_S with a signal present on the amplifier may damage it. Input signals should not drive Pin 1 (FB) directly; always use the buffer amplifier to buffer input signals.

DRIVING NONRESISTIVE LOADS

The AD694 is designed to be stable when driving resistive loads. Adding a 0.01 μF capacitor from I_{OUT} (Pin 11) to Com (Pin 5), as shown in Figure 3, insures the stability of the AD694 when driving inductive or poorly defined loads. This capacitor is recommended when there is any uncertainty as to the characteristics of the load.

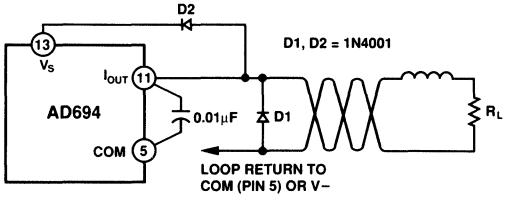


Figure 3. Capacitor Utilized When Driving Nonresistive Loads; Protection Diodes Used When Driving Inductive Loads

Additional protection is recommended when driving inductive loads. Figure 3 shows two protective diodes, D1 and D2, added to protect against voltage spikes that may extend above V_S or below common that could damage the AD694. These diodes should be used in addition to the 0.01 μF capacitor. When the optional NPN transistor is used, the capacitor and diodes should connect to the NPN emitter instead of Pin 11.

0–20 mA OPERATION

A 0–20 mA output range is available with the AD694 by removing the 4 mA offset current with the 4 mA On/Off pin. In normal 4–20 mA operation 4 mA On/Off (Pin 9) is tied to ground, enabling the 4 mA offset current. Tying Pin 9 to a potential of 3 V or greater turns off the 4 mA offset current; connecting Pin 9 to the 10 V reference, the positive supply, or a TTL control pin, is a convenient way to do this. In 0–20 mA mode the input span is increased by 20%, thus the precalibrated input spans of 2 V and 10 V become 2.5 V and 12.5 V. Minimum supply voltages for the two spans increase to 5 V and 15 V.

The 4 mA On/Off pin may also be used as a "jiggle pin" to unstick valves or actuators, or as a way to shut off a 4–20 mA loop entirely. Note that the pin only removes the 4 mA offset and not the signal current.

DUAL SUPPLY OPERATION

Figure 4 shows the AD694 operated in dual supply mode. (Note that the pass transistor is shown for illustration and is not required for dual supply operation.) The device is powered completely by the positive supply which may be as low as 4.5 V. The unique design of the output stage allows the I_{OUT} pin to extend below common to a negative supply. The output stage can source a current to a point 36 V below the positive supply. For example, when operated with a +12.5 V supply, the AD694 can source a current to a point as low as 23.5 V below common. This feature can simplify the interface to dual supply D/A converters by eliminating grounding and level-shifting problems while increasing the load that the transmitter is able to drive. Note that the I_{OUT} pin is the only pin that should be allowed to extend lower than −0.3 V of common.

OPERATION WITH A PASS TRANSISTOR

The AD694 can operate as a stand-alone 4–20 mA converter with no additional active components. However, provisions have been made to connect I_{OUT} to the base of an external NPN pass transistor as shown in Figure 4. This permits a majority of the power dissipation to be moved off-chip to enhance performance and extend the temperature range of operation. Note that the positive output voltage compliance is reduced by approximately 0.7 V, the V_{BE} of the pass device. A 50 Ω resistor should be added in series with the pass transistor collector, when the AD694 is operated with dual supplies, as shown in Figure 4. This will not reduce the voltage compliance of the output stage.

The external pass transistor selected should have a BV_{CEO} greater than the intended supply voltage with a sufficient power rating for continuous operation with 25 mA current at the supply voltage. Ft should be in the 10 MHz to 100 MHz range and β should be greater than 10 at a 20 mA emitter current. Heat sinking the external pass transistor is suggested.

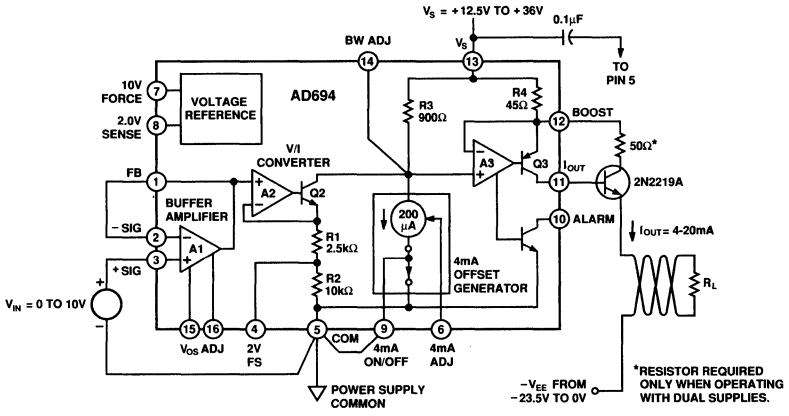


Figure 4. Using Optional Pass Transistor to Minimize Self-Heating Errors; Dual Supply Operation Shown

POWER DISSIPATION CONSIDERATIONS

The AD694 is rated for operation over its specified temperature without the use of an external pass transistor. However, it is possible to exceed the absolute maximum power dissipation, with some combinations of power supply voltage and voltage reference load. The internal dissipation of the part can be calculated to determine if there is a chance that the absolute maximum dissipation may be exceeded. The die temperature must never exceed 150°C.

Total power dissipation (P_{TOT}), is the sum of power dissipated by the internal amplifiers, P (Standing), the voltage reference, P (V_{REF}) and the current output stage, P(I_{OUT}) as follows:

$$P_{TOT} = P\ (Standing) + P\ (V_{REF}) + P\ (I_{OUT})$$

where:

$P\ (Standing)$ = 2 mA (max) × V_S
$P\ (V_{REF})$ = (V_S – V_{REF})× I_{VREF}
$P\ (I_{OUT})$ = (V_S – V_{OUT}) × I_{OUT} (max):

$I_{OUT}\ (max)$ may be the max expected operating current, or the overdriven current of the device.

$P\ (I_{OUT})$ drops to (2 Volts × I_{OUT}) if a pass transistor is used.

Definitions:

V_{REF} = output voltage of reference
I_{VREF} = output current of reference
V_S = supply voltage
V_{OUT} = voltage at I_{OUT} pin.

An appropriate safety factor should be added to P_{TOT}.

The junction temperature may be calculated with the following formula:

$$T_J = P_{TOT}\ (\theta_{JC} + \theta_{CA}) + T_{AMBIENT}$$

θ_{JC} is the thermal resistance between the chip and the package (case), θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection of the case to ambient.

For example, assume that the part is operating with a V_S of 24 V in the cerdip package at 50°C, with a 1 mA load on the 10 V reference. Assume that I_{OUT} is grounded and that the max I_{OUT} would be 20 mA. The internal dissipation would be:

$$P_{(TOT)} = 2\ mA \times 24\ V + (24\ V - 10\ V) \times 1\ mA + (24\ V - 0\ V) \times 20\ mA$$
$$= 48\ mW + 14\ mW + 480\ mW = 542\ mW$$

Using θ_{JC} of 30°C/Watt and θ_{CA} of 70°C/Watt, (from spec page) the junction temperature is:

$$T_J = 542\ mW\ (30°C/W + 70°C/W) + 50°C = 104.2°C$$

The junction temperature is in the safe region.

Internal power dissipation can be reduced either by reducing the value of θ_{CA} through the use of air flow or heat sinks, or by reducing $P_{(TOT)}$ of the AD694 through the use of an external pass transistor. Figure 5 shows the maximum case and still air temperatures for a given level of power dissipation.

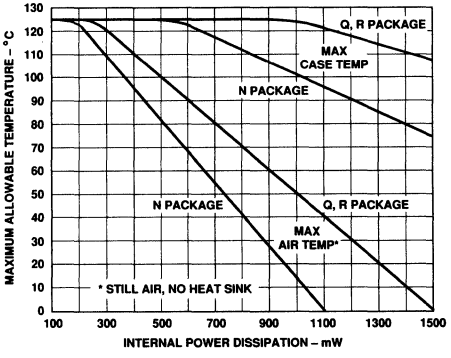


Figure 5. Internal Power Dissipation in mW

10

ADJUSTMENT PROCEDURES

The following sections describe methods for trimming the output current offset, the span and the voltage reference.

ADJUSTING 4 mA ZERO

The 4 mA zero current may be adjusted over the range of 2 mA to 4.8 mA to accommodate large input signal offsets, or to allow small adjustment in the zero current. The zero may be adjusted by pulling up or down on Pin 6 (4 mA Adj) to increase or decrease the nominal offset current. The 4 mA Adj. (Pin 6) should not be driven to a voltage greater than 1 V. The arrangement of Figure 6 will give an approximately linear adjustment of the 4 mA offset within fixed limits. To find the proper resistor values, first select X, the desired range of adjustment as a fraction of 4 mA. Substitute this value in the appropriate formula below along with the chosen reference output voltage (V_{REF} = 2 V or 10 V usually), to determine the resistor values required.

$$R_P = 180\ \Omega\ (1/X - 4.5)$$

$$R_F = 500\ \Omega\ [(V_{REF} / 1.22\ V) - 0.18 - 0.82X][1/X - 4.5]$$

These formulae take into account the ±10% internal resistor tolerance and ensure a minimum adjustment range for the 4 mA offset. For example, assume the 2 V reference option has been selected. Choosing X = 0.05; gives an adjustment range of ±5% of the 4 mA offset.

$$R_P = 180\ \Omega\ (1/0.05 - 4.5) = 2.79\ k\Omega$$

$$R_F = 500\ \Omega\ [(2\ V / 1.22) - 0.18 - 0.82 \times 0.05][1/0.05 - 4.5] = 10.99\ k\Omega$$

These can be rounded down to more convenient values of 2.5 kΩ and 9.76 kΩ. In general, if the value of R_P is rounded down slightly, the value of R_F should be rounded down proportionately and vice versa. This helps to keep the adjustment range symmetrical.

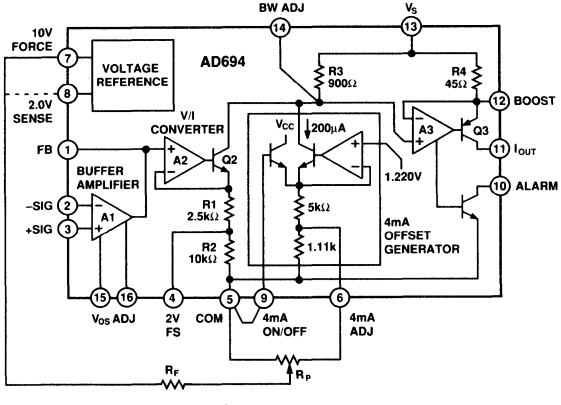


Figure 6. Optional 4 mA Zero Adjustment

ADJUSTING SPAN FOR 10 V FS

When the AD694 is configured with a 10 V input full-scale the span maybe adjusted using the network shown in Figure 7. This scheme allows an approximately linear adjustment of the span above or below the nominal value. The span adjustment does not interact with the 4 mA offset. To select R_S and R_T, choose

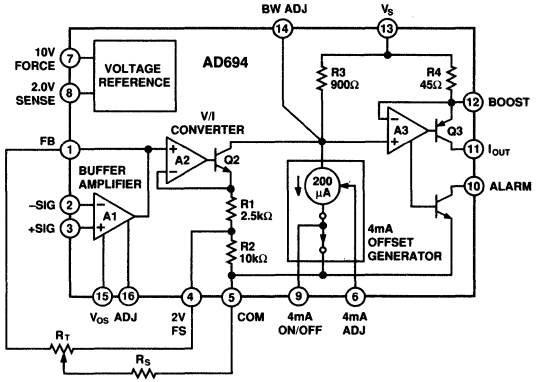


Figure 7. Span Adjustment, 10 V Full Scale

X, the desired adjustment range as a fraction of the span. Substitute this value in the appropriate formula below.

$$R_T = 1.8\ k\Omega\ ((1 - X) / X)$$

$$R_S = 9\ k\Omega[\ 1 - 0.2\ (1 + X)(\ 1 - X\ )]\ /\ 2X$$

These formulae take into account the ±10% absolute resistor tolerance of the internal span resistors and ensures a minimum adjustment range of the span. For example, choosing the adjustment range to be ±2%, or 0.02 gives:

$$R_T = 1.8\ k\Omega((1 - 0.02) / 0.02) = 88.2\ k\Omega$$

$$R_S = 9\ k\Omega\ [\ 1 - 0.2\ (1 + 0.02)(\ 1 - 0.02\ )]\ /\ (2 \times 0.02) = 175.5\ k\Omega$$

These values can be rounded up to the more convenient values of 100 kΩ and 198 kΩ. In general, if R_T is rounded up, then the value of R_S should be rounded up proportionally and vice versa.

ADJUSTING SPAN FOR 2 V FS

The precalibrated 2 V full-scale range requires a different adjustment scheme due to the single supply nature of the AD694. Figure 8 shows an adjustment scheme that allows an approximately linear adjustment of the 2 V span plus or minus the nominal value. The span adjustment does not affect the value of the 4 mA offset current.

To find the proper resistor values first select X, the desired range of adjustment as a fraction of the output span. Substitute this value into the following formulae:

$$R_A = 2 \times X \times R_B \text{ where } R_B \text{ is greater than 5 K}$$

$$R_C = (2.75\ k\Omega \times X) / (1 - 0.275X)$$

These formulae take into account the ±10% absolute tolerance of the internal span resistors and ensure a minimum adjustment range.

For example, choosing the adjustment range to be ±320 μA of FS or, ±2%, let X = 0.02. Thus:

Setting R_B = 10 K, then $R_A = 2(.02) \times 10\ k\Omega = 400\ \Omega$

$R_C = (2.75\ k\Omega \times 0.02)/\ (1 - 0.275 \times (0.02)) = 55.3\ \Omega$

The value of R_C can be rounded to the more convenient values of 49.9 Ω. In general, if R_A is rounded up, then R_C should be rounded up proportionally and vice versa; rounding up will increase the range of adjustment.

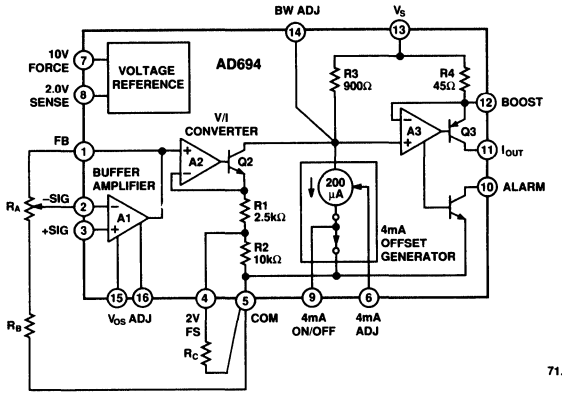


Figure 8. Span Adjustment, 2 V Full Scale

PROGRAMMING OTHER SPANS

There are two methods for programming input spans less than 10 V. The first decreases the input span by programming a noninverting gain into the buffer amplifier. For example, to achieve an input span of 0–5 V, the AD694 is set in its 10 V full-scale mode and the buffer amplifier is configured with a noninverting gain of 2 by adding 2 resistors. Now a 5 V signal at +Sig results in a 10 V full-scale signal at FB (Pin 1), the input to the V/I. This method requires that the V/I be programmed to a 10 V full scale for input spans between 2 V to 10 V. It should be programmed to a 2 V full scale if input spans of less than 2 V are required. This adjustment scheme makes the accuracy of the span adjustment dependent upon the ratio accuracy of the required gain resistors. Thus, it is possible to accurately configure spans other than 2 V or 10 V without using trimming potentiometers, given that the resistor ratios are sufficiently accurate. A supply voltage of 12.5 V is required for spans between 2 V and 10 V. Spans below 2 V require a V_S of 4.5 V or greater.

A second method, allows other spans of less than 10 V to be programmed when supply voltage is less than 12.5 V. Since the AD694 amplifiers require 2.5 V of headroom for operation, a 5 V full-scale input is possible with a 7.5 V supply. This is achieved by placing a resistor, in parallel with R2, (2 V FS (Pin 4) to Com (Pin 5)), to adjust the transconductance of the V/I converter without a headroom penalty. A disadvantage of this method is that the external resistor must match the internal resistor in a precise manner, thus a span trim will be required. The value should be chosen to allow for the ±10% uncertainty in the absolute value of the internal resistor R2.

ADJUSTING REFERENCE OUTPUT

Figure 9 shows one method of making small adjustments to the 10 V reference output. This circuit allows a linear adjustment range of ±200 mV. The 2 V reference may also be adjusted but only in the positive direction.

Other reference voltages can be programmed by adding external resistors. For example, a resistor placed in parallel with R5 can be added to boost the reference output as high as 20 V. Conversely, a resistor in parallel with R6 can be used to set the reference voltage to a value between 2 V and 10 V. The output voltage V_{REF} = 2 V (R6 + R5) / R5. In choosing external adjustment resistors remember that the internal resistors, while ratio matched to a high degree of accuracy, have an absolute resistor tolerance of only ±10%. Be prepared to compensate for this if a precise voltage other than the precalibrated values of 2 V or 10 V is required.

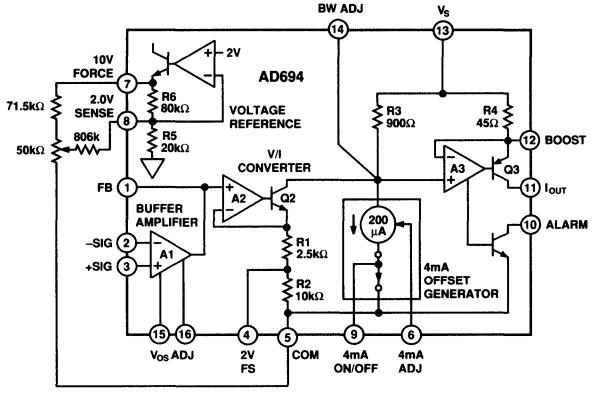


Figure 9. 10 V Reference Output Adjustment

BANDWIDTH CONTROL

The bandwidth of the AD694 can be limited to provide noise filtering. This is achieved by connecting an external capacitor from BW ADJ (Pin 14) to V_S (Pin 13) as shown in Figure 10. To program the bandwidth, substitute the desired bandwidth in Hz, into the formula below to determine the required capacitor.

$$C = 1\ farad\ Hz\ \Omega\ /\ (2\ \pi\ 900\ \Omega\ BW)$$

The bandwidth chosen will vary ±10% due to internal resistor tolerance, plus an additional amount due to capacitor tolerance.

This method of bandwidth control is not recommended as a way to filter large high frequency transients in the input signal. It is recommended that frequencies greater than the BW of the buffer amplifier be eliminated with an input filter to avoid rectification of noise by the input amplifiers.

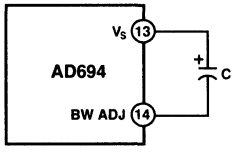


Figure 10. Noise Filtering with an External Capacitor

10

BUFFER AMPLIFIER OFFSET ADJUST

The buffer amplifier input voltage offset has been laser trimmed to a high degree of accuracy; however, there may be occasions when an offset trim is desired. Figure 11 shows the adjustment method; a trim range of greater than ±2.5 mV is available with this scheme. It is not recommended that this adjustment method be used to affect the 4 mA offset current as the trim will induce offset drift into the buffer amplifier. The buffer amplifier will drift approximately 1μV/°C for each 300 μV of induced offset. To adjust the 4 mA offset current refer to the section "ADJUSTING ZERO."

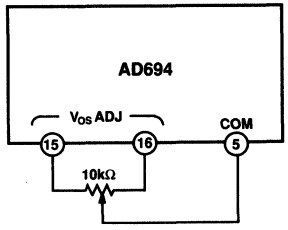


Figure 11. Buffer Amplifier V_{OS} Adjustment

ALARM CIRCUIT

The AD694 has an alarm circuit which warns of open circuit conditions at I_{OUT} (Pin 11), or of attempts to drive the voltage at I_{OUT} higher than V_S-2 V. The alarm transistor will pull down if an out of control condition is sensed. The alarm current is limited to about 20 mA.

Figure 12 shows a typical application. In a digital/analog system the alarm can provide a TTL signal to a controller. The collector of the alarm transistor is tied to the system logic supply through a 20 kΩ pull-up resistor. The alarm is off in normal operation and the voltage at the alarm pin is high. In the event that the wire from I_{OUT} (Pin 11) is opened, or if a large input overdrive forces I_{OUT} too close to V_S, then the alarm pin is driven low. This configuration is compatible with CMOS or TTL logic levels. The alarm transistor can also be used to directly drive an LED or other indicators.

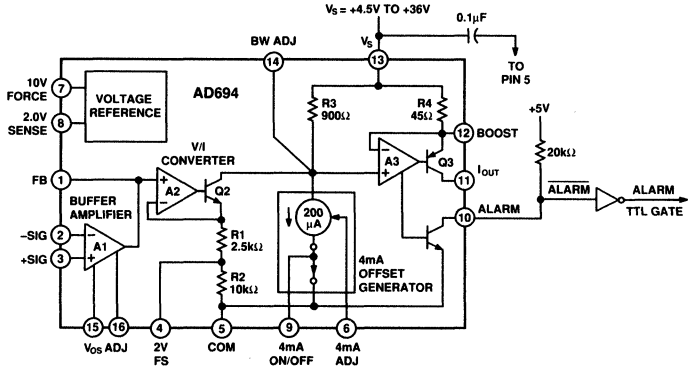


Figure 12. Using the Alarm to Drive a TTL Gate

APPLICATIONS

CURRENT OUTPUT DAC INTERFACE

The AD694 can be easily interfaced to current output DACs such as the AD566A to construct a digital to 4–20 mA interface as shown in Figure 13. The AD694 provides the voltage reference and the buffer amplifier necessary to operate the DAC. Only simple connections are necessary to construct the circuit. The 10 V reference of the AD694 supplies reference input of the AD566. The buffer amplifier converts the full-scale current to +10 V utilizing the internal resistors in the DAC; therefore the AD694 is configured for a 10 V full-scale input. A 10 pF capacitor compensates for the 25 pF output capacitance of the DAC. An optional 100 Ω trim resistor, (R_T), allows the full-scale to be trimmed, a 50 Ω resistor may be substituted if a trim is not required; accuracy will be typically ±1 LSB and the trim does not affect the 4 mA offset. Care should be taken in managing the circuit grounds. Connections from AD694 Pins 9, 3 and AD566 Pins 3 and 7 should be as short as possible and to a single point close to Pin 5 of the AD694. Best practice would have separate connections to the star ground from each pin; this is essential for the AD566 power ground from Pin 12. The 4–20 mA output (Pin 11) must have a return path to the power ground. The return line from the load may be connected to the power ground, or to the −15 V supply based upon the size of the load to be driven, and on power dissipation considerations.

SINGLE SUPPLY DIGITAL TO 4–20 mA INTERFACE

A 12 bit input to 4–20 mA output interface can be constructed that operates on a single 15 V supply. The DAC is operated in its voltage switching mode; this allows the DAC, when supplied with a voltage reference of less than 2.5 V, to provide an output voltage that is proportional to the digital input code and ranges from 0 V to V_{REF}. The AD694 voltage reference is connected to supply 2 V and the input stage is set to a 2 V full scale; the input buffer amplifier serves to buffer the voltage output from the DAC. Connected in this manner a full-scale DAC input code will result in a 20 mA output and an all 0 code will result in a 4 mA output. The loading on the AD694 voltage reference is

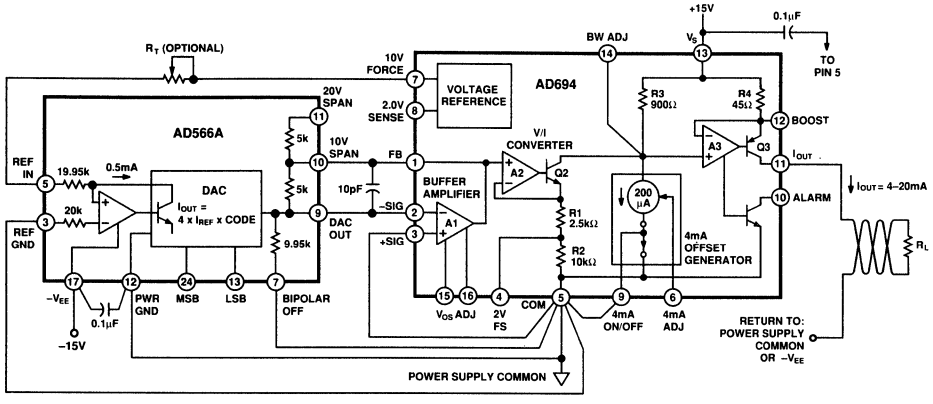


Figure 13. Digital to 4–20 mA Interface Using a Current Steering DAC

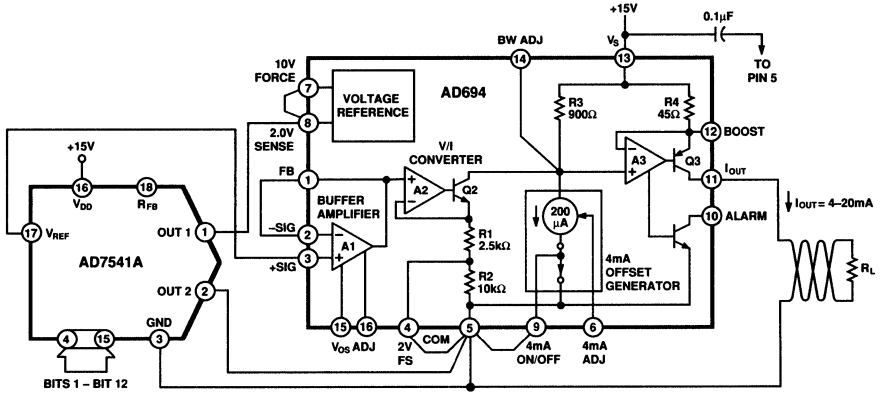


Figure 14. Single Supply Digital Input to 4–20 mA Output

code dependent, and the response time of the circuit will be determined by the reaction of the voltage reference. The supply voltage to the AD7541A should be kept close to 15 V. If V_S is reduced significantly from 15 V the differential nonlinearity of the DAC will increase and the linearity will be degraded.

In some applications it is desirable to have some under-range and over-range in the 4–20 mA output. For example, assume an over and under range capability of ±5% of span is needed, then the output current range corresponding to the full scale of the DAC is 3.2 mA to 20.8 mA. To accomplish this, the span of the AD694 would be increased 10% to 17.6 mA by adding a noninverting gain of 1.1 to the buffer amplifier. The 4 mA offset would then be reduced by 0.8 mA, by utilizing the adjustment scheme explained in "Adjusting 4 mA Zero." Then a digital input from all zero code to full scale would result in an output current of 3.2 mA to 20.8 mA.

LOW COST SENSOR TRANSMITTER

Sensor bridges typically output differential signals in the 10 mV to 100 mV full-scale range. With an AD694, a dual op amp, and some resistors, an instrumentation amplifier front end can be added which easily handles these types of low level signals.

The traditional 3 op amp instrumentation amplifier is built using an AD708, dual op amp for the front end, and the AD694's buffer amplifier is used for the subtractor circuit, as shown in Figure 15. The AD694's 2 V reference is used to provide a "ground" of 2 V that insures proper operation of the in amp over a wide common mode range. The reference pin of the subtractor circuit is tied to the 2 V reference (point C). A 2 kΩ pull-down resistor insures that the voltage reference will be able to sink any subtractor current. The 2 V FS (Pin 4) is attached to the 2 V reference; this offsets the input range of the V/I converter 2 volts positive, to match the "ground" of the in amp.

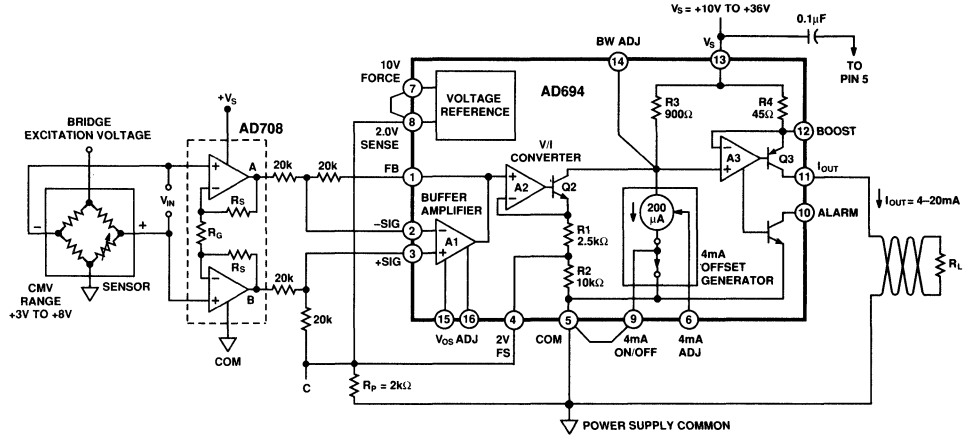


Figure 15. Low Cost Sensor Transmitter

The AD694 will now output a 4–20 mA output current for a 0 to 2 V differential swing across V_A. The gain of the in amp front end is adjusted so that the desired full-scale input signal at V_{IN} results in a V_A of 2 V. For example a sensor that has a 100 mV full scale will require a gain of 20 in the front end. The gain is determined according to the equation:

$$G = [2R_S / Rg] + 1$$

The circuit shown, will convert a positive differential signal at V_{IN} to a 4–20 mA current. The circuit has common-mode range of 3 V to 8 V. The low end of the common-mode range is limited by the AD708's ability to pull down on R_S. A single supply amplifier could be used instead to extend the common-mode range down to about 1.5 V.

As shown, the circuit handles positive differential signals, (V_{IN} positive). To handle bipolar differential signals (V_{IN} is positive or negative), the reference pin of the in amp (point C) must be offset positively from the 2 V reference. For example, disconnected point C from the 2 V reference and connecting it to a 3 V source would result in a V_A of 1 V, (or half scale) for a zero volt differential input from the sensor.

ANALOG DEVICES

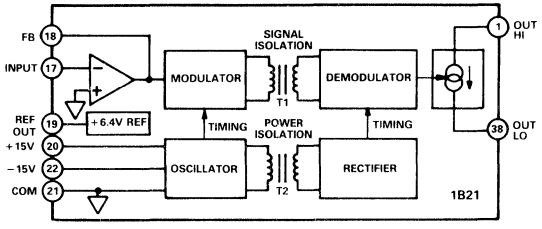
Isolated, Loop-Powered Voltage-to-Current Converter

1B21

FEATURES
Wide Input Range: 0-1V to 0-10V
High CMV Isolation: 1500V rms
Programmable Output Ranges: 4mA to 20mA
0 to 20mA
Load Resistance Range: 0 to 1.35kΩ max
High Accuracy
Low Offset Tempco: ±300nA/°C
Low Gain Tempco: ±50ppm/°C
Low Nonlinearity: ±0.02%
High CMR: 90dB min
Small Package: 0.7″ × 2.1″ × 0.35″
Meets IEEE STD 472: Transient Protection (SWC)

APPLICATIONS
Multichannel Process Control
D/A Converter – Current Loop Interface
Analog Transmitters and Controllers
Remote Data Acquisition Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 1B21 is an isolated voltage-to-current converter that incorporates a unique circuit design utilizing transformer based isolation and automated surface mount manufacturing technology. It provides an unbeatable combination of versatility and performance in a compact plastic package. Designed for industrial applications, it is especially suited for harsh environments with extremely high common-mode interference.

Functionally, the V/I converter consists of four basic sections: input conditioning, modulator, demodulator and current source (1B21 Functional Block Diagram). The input is a resistor programmable gain stage that accepts a 0-1V to 0-10V voltage input. This maps into a 0 to 20mA output or can be offset by 20% using the internal reference for 4mA to 20mA operation. The high level signal is modulated and passed across the barrier which provides complete input to output galvanic isolation of 1500V rms continuous by the use of transformer coupling techniques. Nonlinearity is an excellent ±0.05% max.

Designed for multichannel applications, the 1B21 requires an external loop supply and can accept up to 30V max. This would provide a loop compliance of 27V, which is sufficient to drive a 1.35kΩ load resistance.

The 1B21 is fully specified over −25°C to +85°C and operates over the industrial (−40°C to +85°C) temperature range.

DESIGN FEATURES AND USER BENEFITS

High CMV Isolation: The 1B21 features high input to output galvanic isolation to eliminate ground loops and offer protection against damage from transients and fault voltages. The isolation barrier will withstand continuous CMV of 1500V rms and meets the IEEE Standard for Transient Voltage Protection (STD 472-SWC).

Small Size: The 1B21 package size (0.7″ × 2.1″ DIP) makes it an excellent choice in multichannel systems for maximum channel density. The 0.35″ height also facilitates applications with limited board clearance.

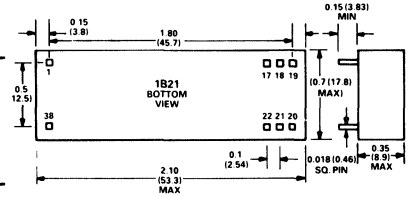
Ease of Use: Complete isolated voltage-to-current conversion with minimum external parts required to get a conditioned current signal. No external buffers or drivers are required.

1B21—SPECIFICATIONS (typical at +25°C and V_S = ±15V unless otherwise noted)

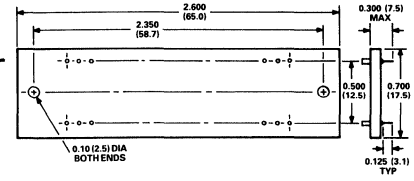
Model	1B21AN
INPUT SPECIFICATIONS	
Input Range	0 to + 10V
Full-Scale Input	+ 1V min to + 10V max
Input Bias Current	± 30pA (± 400pA max)
OUTPUT SPECIFICATIONS	
Current Output Range	4mA to 20mA, 0 to 20mA
Load Compliance at V_{LOOP} = 30V	27V min
Max Output Current @ Input Overload	25mA
Output Noise, 100Hz Bandwidth	1μA p-p
NONLINEARITY (% of Span)	± 0.02% (± 0.05% max)
ISOLATION	
CMV, Input to Output Continuous	1500V rms
CMR, @ 60Hz	90dB min
Transient Protection	IEEE-STD 472 (SWC)
ACCURACY	
Warm-Up Time to Rated Performance	5 min
Total Output Error @ + 25°C (Untrimmed)	
Offset (V_{IN} = 0V)[1]	± 100μA
Span (V_{IN} = + 10V)	± 0.6% FSR
vs. Temperature (− 25°C to + 85°C)	
Offset[2]	± 300nA/°C
Span	± 50ppm/°C
REFERENCE OUTPUT	
Voltage	+ 6.4V dc
Output Error	± 1.5% max
Temperature Coefficient	± 20ppm/°C max
DYNAMIC RESPONSE	
Settling Time to 0.1% of F.S. for 10V Step	9ms
Small Signal Bandwidth	100Hz
POWER SUPPLY	
Input Side	
Operating Voltage	± 15V ± 5%
Quiescent Current	
+ 15V Supply	10mA
− 15V Supply	5mA
Power Supply Rejection	± 0.01%/V
Loop Side	
Operating Voltage	+ 15V to + 30V
Maximum Current	25mA
ENVIRONMENTAL	
Temperature Range	
Rated Performance	− 25°C to + 85°C
Operating	− 40°C to + 85°C
Storage	− 40°C to + 85°C
Relative Humidity, Noncondensing	0 to 95% @ + 60°C
CASE SIZE	0.7" × 2.1" × 0.35" (17.8 × 53.3 × 8.9)mm

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1060 MATING SOCKET



PIN DESIGNATIONS

PIN	FUNCTION
1	OUT HI
17	IN
18	FB
19	REF
20	+ 15V
21	COM
22	− 15V
38	OUT LOW

NOTES

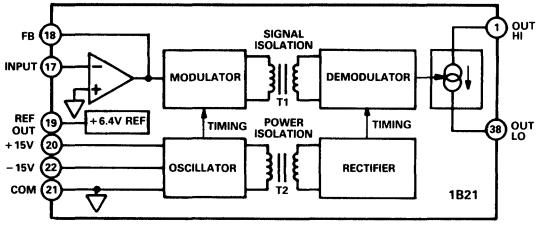
[1]For 0-20mA mode. For 4-20mA mode an additional 60μA is contributed by the ± 1.5% reference error on the 4mA output.

[2]For a complete discussion of the temperature effects of the offset resistor and reference refer to "Using the 1B21" section.

Specifications subject to change without notice.

INSIDE THE 1B21

Referring to the functional block diagram, the ±15V power inputs provide power to both the input side circuitry and the power oscillator. The 25kHz power oscillator provides both the timing information for the signal modulator and drives transformer T2 for the output side power supplies. The secondary winding of T2 is full wave rectified and filtered to create the output side power.



1B21 Functional Block Diagram

The input stage is configured as an inverting amplifier with three user supplied resistors for gain, offset and feedback. The conditioned signal is modulated to generate a square wave with a peak-to-peak amplitude proportional to V_{IN}. This signal drives the signal transformer T1. An internal reference with a nominal output voltage of +6.4V and tempco of ±20ppm/°C is provided to develop a 4mA offset for 4mA to 20mA current loop applications.

After passing through signal transformer T1, the amplitude modulated signal is demodulated and filtered by a single pole filter. Timing information for the output side is derived from the power transformer T2. The filtered output provides the control signal for the voltage-to-current converter stage. An external power supply is required in series with the load to complete the current loop.

USING THE 1B21

Input Configurations: The 1B21 has been designed with a flexible input stage for a variety of input and output ranges. The basic interconnection for setting gain and offset is shown in Figure 1. The output of the internal amplifier is constrained to 0 to −5V, which maps into 0 to 20mA across the isolation barrier. Thus to create a 4mA offset at the output, the input amplifier has to be offset by 1V.

For example, for 0 to 20mA operation the transfer function for the input stage is:

$$5/V_{IN} = R_F/R_I$$

and no offset resistor is needed. For 4mA to 20mA operation we get:

$$4/V_{IN} = R_F/R_I$$

which maps the input voltage into a 4V span. To create a 1V offset at the output of the internal amplifier (4mA at the output of the 1B21) a current derived from the reference can be fed into the summing node. The offset resistor (for a 1V output offset) will be given by the equation: $R_O = 6.4R_F$. For most applications it is recommended that R_F be in the 25kΩ ±20% range. Resistor values for typical input and output ranges are shown in Table I.

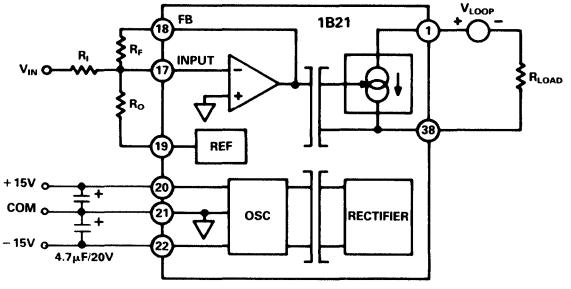


Figure 1. Basic Interconnections

Input Volts	Output mA	R_I kΩ	R_F kΩ	R_O kΩ
0-5	0-20	25	25	Open
0-10	0-20	50	25	Open
0-5	4-20	25	20	128
0-10	4-20	50	20	128
1-5	4-20	25	25	Open

Table I. Resistor Values for Typical Ranges

Adjustments: Figure 2 is an example of using potentiometers for trimming gain and offset for a 0-5V input and 0 to 20mA output. The network for offset adjustment keeps the resistors relatively small to minimize noise effects while giving a sensitivity of ±1% of span. For more adjustment range, resistors smaller than 274k can be used. Resistor values from Table I can be substituted for other input and output ranges.

In general, any bipolar voltage can be input to the 1B21 as long as it is offset to meet the 0 to −5V constraint of the modulator and the input signal range is 1V minimum.

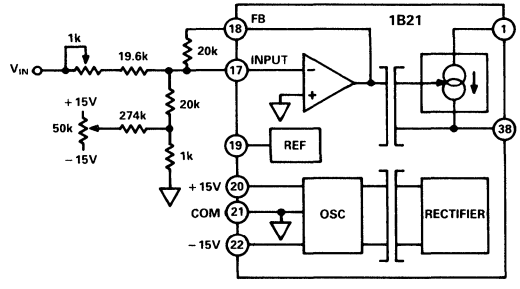


Figure 2. Offset and Span Adjustment

TC Considerations of External Resistors: The specifications for gain and offset temperature coefficient (TC) for the 1B21 exclude the effects of external components. The total gain TC for the circuit in Figure 1 is:

Gain TC = 1B21 Gain TC + (Tracking TC of R_F and R_I)

The offset TC is also affected by the thermal stability of the internal voltage reference and its contribution is:

Ref TC = $(V_{REF})(R_F/R_O)(4mA/V)$(TC of V_{REF} + Tracking TC of R_F and R_O)$/1 \times 10^6$

Total Offset TC = 1B21 Offset TC + Ref TC

Specifically using R_F, R_I and R_O from Case 3 in Table I, with absolute TCs of ±25ppm/°C we get:

Gain TC = 50 + (25+25) = 100ppm/°C

Offset TC = $300+(6.4V)(20k/128k)(4mA/V)(20+25+25)/1\times10^6$

= ±580nA/°C

Similarly, when using a resistor network with a tracking spec of ±5ppm/°C, the total gain TC would be ±55ppm/°C and the total offset TC would be ±400nA/°C.

APPLICATIONS

Output Protection: In many industrial applications it may be necessary to protect the current output from accidental shorts to ac line voltages in addition to high common-mode voltages and short circuits to ground. The circuit shown in Figure 3 can be used for this purpose. The maximum permissible load resistance will be lowered by the fuse resistance (typically 8Ω) when protection circuitry is utilized.

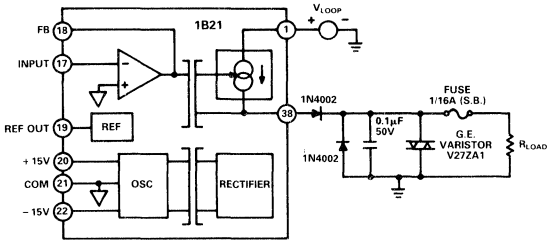


Figure 3. Output Protection Circuitry

Low Drift Input Network: Figure 4 shows a configuration suitable for applications where errors have to be minimized over a wide temperature range. A temperature tracking network such as a 50k Beckman (PN 698-3R50KD) can be used to implement both offset and gain for either 0 to 20mA or 4mA to 20mA current loops. For 0-10V signals either IN1 or IN2 can be used for input. For 0-5V signals, jumper IN1 to IN2. Similarly, for 4mA to 20mA operation the 4mA node should be jumpered to OFFSET, while for 0 to 20mA it should be tied to COM.

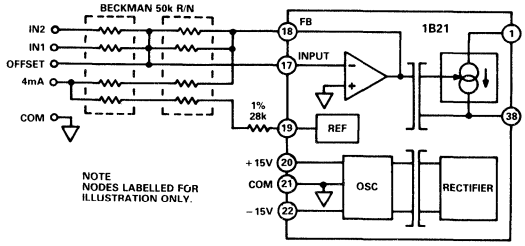


Figure 4. Low Tempco Resistor Network Configuration

Multiloop Isolation: Multiple 1B21s can be connected to a single loop supply in parallel as shown in Figure 5. The amperage of the loop supply should be sufficient to drive all the loops at full-scale output.

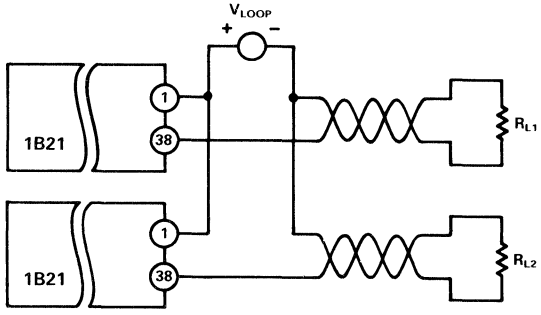


Figure 5. Multiple 1B21s with Single Loop Supply

Programmable, Isolated Voltage-to-Current Converter

1B22

FEATURES

Internal Isolated Loop Supply Drives 1000 Ω Load
Pin Programmable Inputs: 0 to +5 V or 0 to +10 V
Pin Programmable Outputs: 4 to 20 mA or 0 to 20 mA
High CMV Isolation: 1500 V RMS
Normal Mode Output Protection: 240 V RMS
High Accuracy
- **Low Offset Tempco: ±300 nA/°C**
- **Low Gain Tempco: ±50 ppm/°C**
- **Low Nonlinearity: ±0.02%**
- **High CMR: 90 dB min**

Small Package: 1.0″×2.10″×0.35″
Meets IEEE STD 472: CMV Transient Protection (SWC)

APPLICATIONS

Multichannel Process Control
D/A Converter – Current Loop Interface
Analog Transmitters and Controllers
Remote Data Acquisition Systems

GENERAL DESCRIPTION

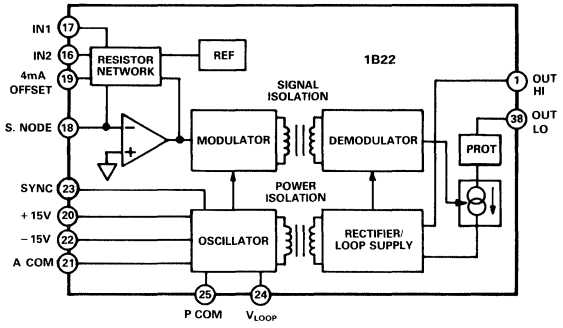
The 1B22 is an isolated voltage-to-current converter that incorporates transformer isolation to achieve high performance and automated surface mount manufacturing for low cost and increased reliability. Designed for industrial applications, it is especially suited for harsh environments with extremely high common mode interference. With programmable inputs and outputs, the 1B22 provides an unbeatable combination of versatility and performance in a compact plastic package.

Functionally, the V/I converter consists of four basic sections: input conditioning, modulator/demodulator, isolated loop supply and current source (Figure 1). The 1B22 is pin programmable for 0 to +5 V or 0 to +10 V inputs and 0 to 20 mA or 4 to 20 mA outputs using an internal resistor network. It can also be set by an external resistor to accept 0 to +1 V to 0 to +10 V inputs. Transformer coupling provides 1500 V rms galvanic isolation between the inputs and the current loop. Nonlinearity is an excellent ±0.05% max.

Loop power is generated internally through a dc/dc converter and is also isolated from the input side (1500 V rms). Loop compliance voltage is dependent on the voltage supplied to the 1B22, and with V_{LOOP} = 28 V, it is sufficient to drive a 1000 Ω load.

The 1B22 is fully specified over −25°C to +85°C and operates over the industrial (−40°C to +85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



DESIGN FEATURES AND USER BENEFITS

Isolated Loop Power: Internal loop supply completely isolates the loop from the input terminals (1500 V rms) and provides the capability to drive 0 to 1000 Ω loads. This eliminates the need for an external dc/dc converter.

Ease of Use: The 1B22 offers complete isolated voltage-to-current conversion with minimum external parts required to get a conditioned current signal. No external buffers or drivers are required.

High CMV Isolation: The 1B22 features high input to output galvanic isolation to eliminate ground loops and offer protection against damage from transients and fault voltages. The isolation barrier will withstand continuous CMV of 1500 V rms and meets the IEEE Standard for Common Mode Voltage Transient Protection (STD 472-SWC).

Small Size: The 1B22 package size (1.0″×2.1″ DIP) makes it an excellent choice in multichannel systems for maximum channel density. The 0.35″ height also facilitates applications with limited board clearance.

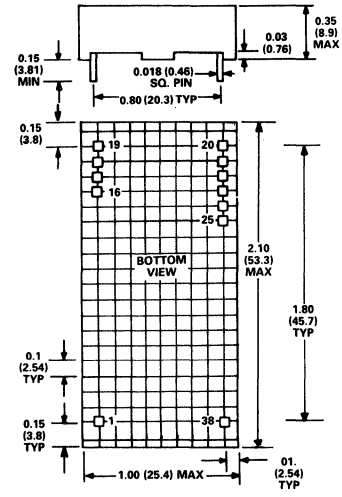
1B22—SPECIFICATIONS (typical @ +25°C and V_S = ±15 V, V_{LOOP} = +24 V, unless otherwise noted)

Model	1B22AN
INPUT SPECIFICATIONS	
Factory Calibrated, User Selectable	0 to +5 V, 0 to +10 V
Input Impedance	
0 to +10 V Input Range	50 kΩ
0 to +5 V Input Range	25 kΩ
OUTPUT SPECIFICATIONS	
Current Output Range, User Selectable	4 to 20 mA, 0 to 20 mA
Load Compliance Range, V_{LOOP}=+15 V	8 V min
V_{LOOP}=+28 V	20 V min
Maximum Output Current @ Input Overload	30 mA
Output Noise, 100 Hz Bandwidth	300 nA p-p
NONLINEARITY (% OF SPAN)	±0.02% (±0.05% max)
ISOLATION	
CMV, Input to Output Continuous	1500 V rms max
CMR, @ 60 Hz	90 dB min
Normal-Mode Output Protection	240 V rms continuous
CMV Transient Protection	IEEE - STD 472 (SWC)
ACCURACY	
Warm-Up Time to Rated Performance	5 min
Total Output Error @ +25°C	
Offset (V_{IN} = 0 V)	±60 μA
Span (V_{IN} = +10 V)	±0.7% Full Scale
vs. Temperature (−25°C to +85°C)	
Offset	±300 nA/°C
Span	±50 ppm/°C
DYNAMIC RESPONSE	
Settling Time to 0.1% of FS for 10 V Step	9 ms
Small Signal Bandwidth	400 Hz
POWER SUPPLY	
Bipolar Input Supplies	
Operating Voltage	±15 V ±5%
Quiescent Current	±7.5 mA
Power Supply Rejection	±0.01%/V
Loop Supply	
Operating Voltage	+14 V to +30 V
Operating Current, at Full-Scale Output	25 mA
Loop Supply Rejection	±0.005%/V
ENVIRONMENTAL	
Temperature Range	
Rated Performance	−25°C to +85°C
Operating	−40°C to +85°C
Storage	−40°C to +85°C
Relative Humidity, Noncondensing	0 to 95% @ 60°C
CASE SIZE	1.0″×2.1″×0.35″

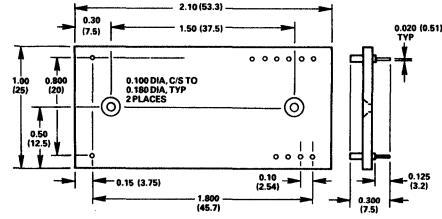
NOTE
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1225 MATING SOCKET



PIN DESIGNATIONS

PIN	FUNCTION
1	OUT HI
16	IN2
17	IN1
18	S. NODE
19	4mA OFFSET
20	+15V
21	ANA COM
22	−15V
23	SYNC
24	V_{LOOP}
25	POWER COM
38	OUT LOW

INSIDE THE 1B22

The 1B22 produces an isolated 4 to 20 mA or 0 to 20 mA output current which is proportional to the input voltage and independent of the output load resistance (Figure 1). The input stage is configured as an inverting amplifier with a resistor network to provide pin-strappable input ranges of 0 to +5 V and 0 to +10 V and output ranges of 0 to 20 mA and 4 to 20 mA. The conditioned signal is modulated to generate a square wave that drives transformer T1. The peak-to-peak amplitude of the signal is proportional to V_{IN}. An internal, high stability reference with a nominal output voltage of +6.4 V is used to develop a 4 mA offset for the 4 to 20 mA current loop output.

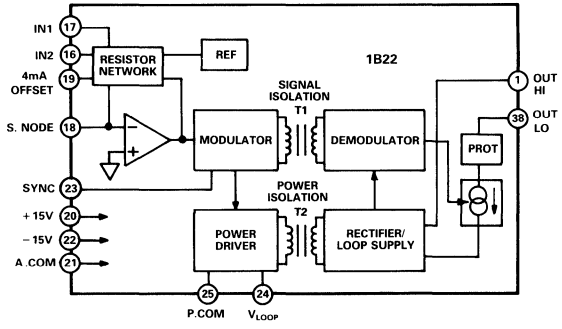


Figure 1. 1B22 Functional Block Diagram

After passing through signal transformer T1, the amplitude modulated signal is demodulated and filtered by a single pole filter. This filtered output is the control signal for the voltage-to-current converter stage. Timing information for the demodulator is derived from the power transformer T2. The 1B22 outputs are protected from accidental shorts to ac line voltages up to 240 V rms. Combined with 1500 V input to output isolation, the 1B22 provides unbeatable protection against transients, wiring errors and current loop short circuits to power lines.

The dc-dc converter consists of a power driver, power transformer T2, a full wave rectifier and a filter. The dc-dc converter provides the power for the output circuitry as well as the isolated compliance voltage for the loop. This voltage is proportional to V_{LOOP} on the input side. The 1B22 requires ±15 V supplies to power the input side circuitry and a +14 V to +30 V supply for the dc-dc converter.

USING THE 1B22

Basic Interconnections: The 1B22 may be applied to achieve rated performance as shown in Figure 2. For 0 to 10 V signals either IN1 or IN2 can be used for input; for 0 to +5 V signals jumper IN1 to IN2. Similarly, for 4 to 20 mA operation the 4 mA OFFSET node should be jumpered to the S. NODE, while for 0 to 20 mA it should be tied to COM. Figure 3 shows the functional diagram of the resistor network used in the 1B22.

For applications where a separate loop supply is not available, the ±15 V supplies can be used by connecting +15 V to V_{LOOP} (Pin 24) and COM to P.COM (Pin 25). For additional compliance voltage, P.COM can be connected to −15 V to drive higher loads.

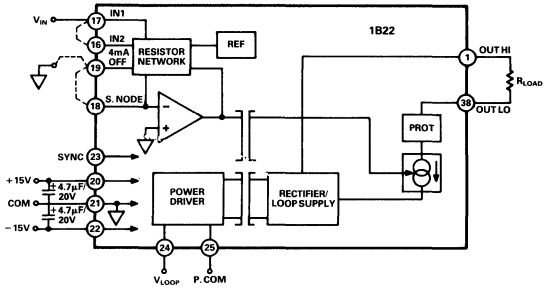


Figure 2. Basic Interconnections

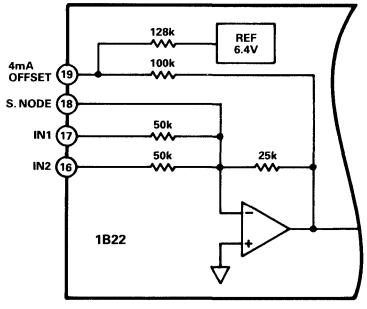


Figure 3. Internal Resistor Network

Optional Trim Adjustments: Figure 4 is an example of using potentiometers for trimming gain and offset for a 0 to +10 V input and 4 to 20 mA output. The network for offset adjustment keeps the resistors relatively small to minimize noise effects while giving a sensitivity of ±1% of span. For more adjustment range, resistors smaller than 274 kΩ can be used.

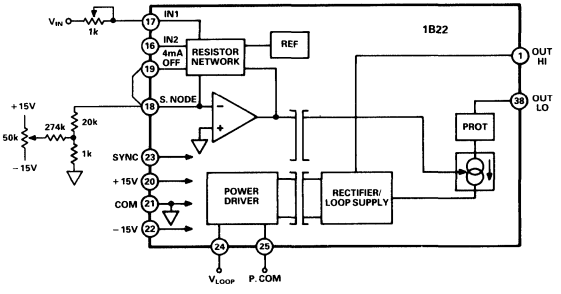


Figure 4. Optional Offset and Span Adjustment

Synchronizing Multiple 1B22s: In applications where multiple 1B22s are used in close proximity, radiated individual oscillator frequencies may cause "beat frequency" related output errors. These errors can be eliminated by driving the SYNC pins of all the units with a 40 kHz clock circuit at 50% duty cycle (Figure 5). The SYNC input typically has an input impedance of 150 kΩ‖180 pF.

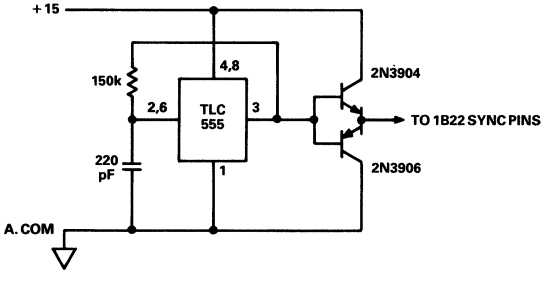


Figure 5. Multiple 1B22s' Synchronization

Loop Supply Requirements: The 1B22 design allows flexible loop supply options. The loop supply voltage required for any value of load resistance can be calculated from the following equation:

$$V_{LOOP} = \frac{2R_L + 780}{106}$$

This value allows for approximately 10% overrange capability. The graph in Figure 6 shows the relationship between supply voltage and load resistance.

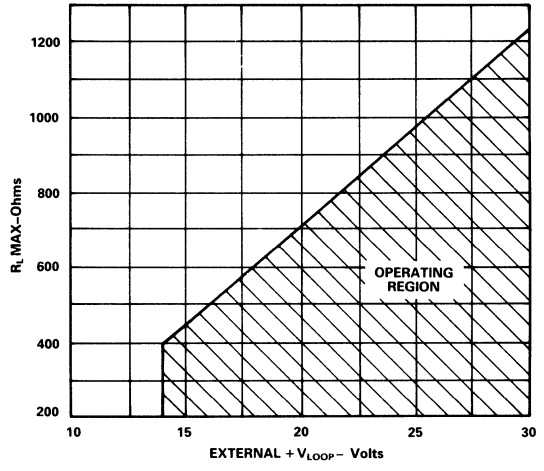


Figure 6. Loop Supply vs. Load

APPLICATIONS

Isolated D/A Converter: The 1B22 offers total ground isolation and protection from high voltage transients in interfacing D/A converters to standard 4 to 20 mA current loops. The D/A converter, such as the Analog Devices' 12-bit AD7245 DACPORT™, should be connected for operation on the unipolar 0 to +10 V output range. This is shown in Figure 7.

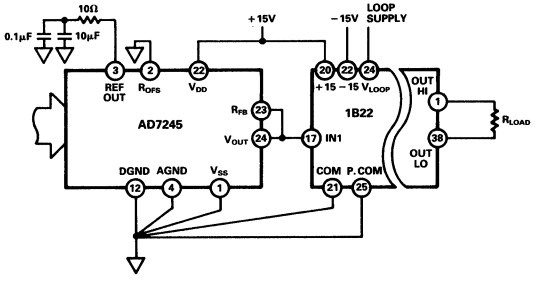


Figure 7. D/A Converter – Isolated 4–20 mA Interface

Pressure Transmitter: In Figure 8, the 1B22 is used in a pressure transmitter application to provide complete input-output isolation and avoid signal errors due to ground loop currents. The process pressure is monitored with a strain gage type pressure transducer interfaced by the Analog Devices' 1B32 transducer signal conditioner. The high level voltage output of the 1B32 is converted to the isolated 4 to 20 mA current for transmission to a remote recorder or indicator.

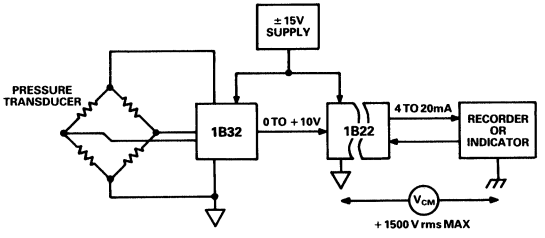


Figure 8. Isolated Pressure Transmitter

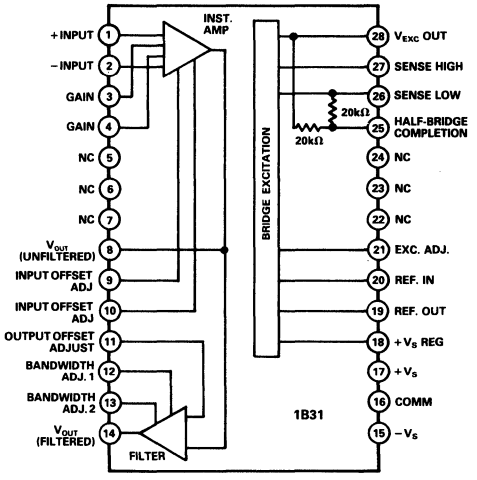
Wide Bandwidth Strain Gage Signal Conditioner

1B31

FEATURES
- **Low Cost**
- **Complete Signal-Conditioning Solution**
- **Small Package: 28-Pin Double DIP**
- **Internal Half-Bridge Completion Resistors**
- **Remote Sensing**
- **High Accuracy**
  - **Low Drift: ±0.25μV/°C**
  - **Low Noise: 0.3μV p-p**
  - **Low Nonlinearity: ±0.005% max**
  - **High CMR: 140dB min (60Hz, G = 1000V/V)**
- **Programmable Bridge Excitation: +4V to +15V**
- **Adjustable Low Pass Filter: f_C = 10Hz to 20kHz**

APPLICATIONS
- **Measurement of: Strain, Torque, Force, Pressure**
- **Instrumentation: Indicators, Recorders, Controllers**
- **Data Acquisition Systems**
- **Microcomputer Analog I/O**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Model 1B31 is a high performance strain gage signal-conditioning component that offers the industry's best price/performance solution for applications involving high-accuracy interface to strain gage transducers and load cells. Packaged in a 28-pin double DIP using hybrid technology, the 1B31 is a compact and highly reliable product. Functionally, the signal conditioner consists of three sections: a precision instrumentation amplifier, a two-pole low pass filter, and an adjustable transducer excitation.

The instrumentation amplifier (IA) section features low input offset drift of ±0.25μV/°C (RTI, G = 1000V/V) and excellent nonlinearity of ±0.005% max. In addition, the IA exhibits low noise of 0.3μV p-p typ (0.1Hz-10Hz), and outstanding 140dB min common-mode rejection (G = 1000V/V, 60Hz). The gain is programmable from 2V/V up to 5000V/V by one external resistor.

The two-pole low pass filter offers a 40dB/decade roll-off from 1kHz to reduce high frequency noise and improve system signal-to-noise ratio. The corner frequency is adjustable downwards by external capacitors and upwards to 20kHz by three resistors. The output voltage can also be offset by ±10V with an external potentiometer to null out dead weight.

The 1B31's regulated transducer excitation stage features low output drift (±0.004%/°C typ) and can drive 120Ω or higher resistance load cells. The excitation is preset at +10V and is adjustable from +4V and +15V. This section also has remote sensing capability to allow for lead-wire compensation in 6-wire bridge configurations. For half-bridge strain gages, a matched pair of thin-film 20kΩ resistors is connected across the excitation outputs. This assures temperature tracking of ±5ppm/°C max and reduces part count.

The 1B31 is available in a plastic package specified over the industrial (−40°C to +85°C) temperature range and will be available soon in a bottom-brazed ceramic package specified over the military (−55°C to +125°C) temperature range.

DESIGN FEATURES AND USER BENEFITS

Ease of Use: Direct transducer interface with minimum external parts required, convenient offset and span adjustment capability.

Half-Bridge Completion: Matched resistor pair tracking to ±5ppm/°C max for half-bridge strain gage applications.

Remote Sensing: Voltage drops across the excitation lead-wires are compensated by the regulated supply, making 6-wire load-cell interfacing straightforward.

Programmable Transducer Excitation: Excitation source preset for +10V dc operation without external components. User-programmable from a +4V to +15V dc to optimize transducer performance.

Adjustable Low Pass Filter: The two-pole active filter (f_C = 1kHz) reduces noise bandwidth and aliasing errors with provisions for external adjustment of cutoff frequency (10Hz to 20kHz).

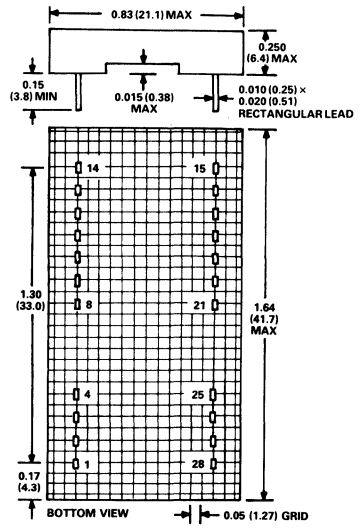
1B31—SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

Model	1B31AN	1B31SD†
GAIN[1]		
Gain Range	2 to 5000V/V	*
Gain Equation	$R_G = \frac{80k\Omega}{G-2}$	*
Gain Equation Accuracy, G≤1000V/V	±3%	*
Gain Temperature Coefficient[2]	±15ppm/°C (±25ppm/°C max)	*
Nonlinearity	±0.005% max	*
OFFSET VOLTAGES[1]		
Total Offset Voltage, Referred to Input		
Initial, @ +25°C (Adjustable to Zero)		
G = 2V/V	±2mV (±10mV max)	*
G = 1000V/V	±50µV (±200µV max)	*
Warm-Up Drift, 5 min., G = 1000V/V	Within ±1µV of final value	*
vs. Temperature		
G = 2V/V	±25µV/°C (±50µV/°C max)	*
G = 1000V/V	±0.25µV/°C (±2µV/°C max)	*
At Other Gains	$\left(\pm 2 \pm \frac{100}{G}\right)\mu V/°C$	*
vs. Supply		
G = 2V/V	±50µV/V	*
G = 1000V/V	±0.5µV/V	*
Output Offset Adjust Range	±10V min	*
INPUT BIAS CURRENT		
Initial @25°C	±10nA (±50nA max)	*
vs. Temperature	±25pA/°C	*
INPUT DIFFERENCE CURRENT		
Initial @ +25°C	±5nA (±20nA max)	*
vs. Temperature	±10pA/°C	*
INPUT IMPEDANCE		
Differential	1GΩ‖4pF	*
Common Mode	1GΩ‖4pF	*
INPUT VOLTAGE RANGE		
Linear Differential Input (V_D)	±5V	*
Maximum CMV Input	$\pm\left(12 - \frac{G \times V_D}{4}\right)$ V max	*
CMR, 1kΩ Source Imbalance		
G = 2V/V, dc to 60Hz	86dB	*
G = 100V/V to 5000V/V		
1kHz Bandwidth[3]		
@ dc to 60Hz	110dB min	*
10Hz Bandwidth[4]		
@ dc	110dB min	*
@ 60Hz	140dB min	*
INPUT NOISE		
Voltage, G = 1000V/V		
0.1Hz to 10Hz	0.3µV p-p	*
10Hz to 100Hz	1µV p-p	*
Current, G = 1000V/V		
0.1Hz to 10Hz	60pA p-p	*
10Hz to 100Hz	100pA p-p	*
RATED OUTPUT[1]		
Voltage, 2kΩ Load, min	±10V	*
Current	±5mA	*
Impedance, dc to 2Hz, G = 2V/V to 1000V/V	0.5Ω	*
Load Capacitance	1000pF	*
Output Short-Circuit Duration	Indefinite	*
DYNAMIC RESPONSE[1]		
Small Signal Bandwidth −3dB, G = 2V/V to 1000V/V	1kHz	*
Slew Rate	0.05V/µs	*
Full Power	350Hz	*
Settling Time, G = 2V/V to 1000V/V, ±10V Output, Step to ±0.1%	2ms	*
LOW PASS FILTER		
Number of Poles	2	*
Gain (Pass Band)	−2V/V	*
Cutoff Frequency (−3dB Point)	1kHz	*
Roll-Off	40dB/decade	*

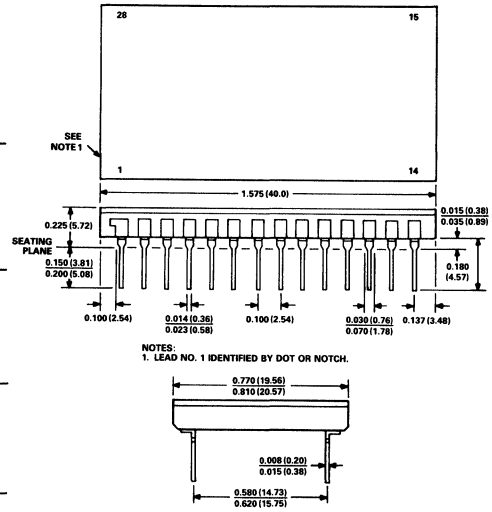
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic Package (N)



Ceramic Package (D)



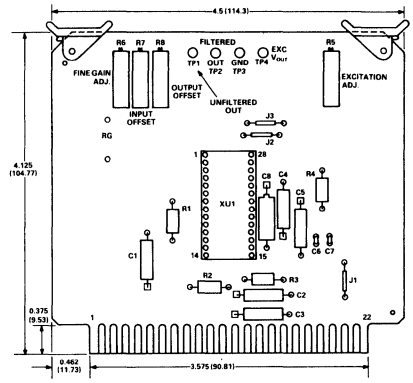
PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+INPUT	15	$-V_S$
2	−INPUT	16	COMMON
3	GAIN	17	$+V_S$
4	GAIN	18	$+V_S$ REGULATOR
8	V_{OUT} (UNFILTERED)	19	REF OUT
9	INPUT OFFSET ADJ.	20	REF IN
10	INPUT OFFSET ADJ.	21	EXCITATION ADJ.
11	OUTPUT OFFSET ADJ.	25	HALF-BRIDGE COMP.
12	BANDWIDTH ADJ. 1	26	SENSE LOW
13	BANDWIDTH ADJ. 2	27	SENSE HIGH
14	V_{OUT} (FILTERED)	28	V_{EXC} OUT

Model	1B31AN	1B31SD†
BRIDGE EXCITATION		
Regulator Input Voltage Range	+9.5V to +28V	*
Output Voltage Range	+4V to +15V	*
Regulator Input/Output Voltage Differential	+3V to +24V	*
Output Current[5]	100mA max	*
Regulation, Output Voltage vs. Supply	±0.05%/V	*
Load Regulation, I_L = 1mA to 50mA	±0.1%	*
Output Voltage vs. Temperature	±0.004%/°C	*
Output Noise, 10Hz to 1kHz[6]	200μV p-p	*
Reference Voltage (Internal)	+6.8V ±5%	*
Internal Half-Bridge Completion		
Nominal Resistor Value	20kΩ ±1%	*
Temperature Tracking	±5ppm/°C max	*
POWER SUPPLY		
Voltage, Rated Performance	±15V dc	*
Voltage, Operating	±12V to ±18V dc	*
Current, Quiescent[7]	+10mA	*
ENVIRONMENTAL		
Temperature Range		
Rated Performance	−40°C to +85°C	−55°C to +125°C
Operating	−40°C to +85°C	−55°C to +125°C
Storage	−40°C to +100°C	−65°C to +150°C
Relative Humidity	0 to 95% @ +60°C	*
CASE SIZE	0.83" × 1.64" × 0.25" (21.1 × 41.7 × 6.350mm) max	0.81" × 1.57" × 0.23" (20.6 × 40.0 × 5.72mm)

NOTES
*Specifications same as 1B31AN.
†SD grade available in Spring 1988.
[1]Specifications referred to the filtered output at Pin 14.
[2]Exclusive of external gain settling resistor.
[3]Unadjusted filter setting.
[4]Filter cutoff frequency set with external capacitors.
[5]Derate from +50°C as shown in Figure 14.
[6]4.7μF capacitor from $V_{REF\ IN}$ (Pin 20) to COMM.
[7]Excluding bridge excitation's current, and with no loading on the output.
Specifications subject to change without notice.

AC1222 MOUNTING CARD



AC1222 CONNECTOR DESIGNATION

PIN	FUNCTION	PIN	FUNCTION
1	+INPUT	S	V_{EXC} OUT
2	−INPUT	T	SENSE HIGH
3	N/C	U	SENSE LOW
4	GAIN (3)	V	HALF-BRIDGE COMP.
5	GAIN (4)	X	REF OUT
6	V_{OUT} (UNFILTERED)	Y	REF IN
7	INPUT OFFSET ADJ. (9)	Z	EXC. ADJ.
8	INPUT OFFSET ADJ. (10)		
9	OUTPUT OFFSET ADJ.		
10	BANDWIDTH ADJ. 1		
11	BANDWIDTH ADJ. 2		
12	V_{OUT} (FILTERED)		
19	$-V_S$		
20	COMMON		
21	$+V_S$		
22	$+V_S$ REG		

The AC1222 mounting card is available for the 1B31. The AC1222 is an edge connector card with a 28-pin socket for plugging in the 1B31. In addition, it has provisions for installing the gain resistor and adjusting the bridge excitation voltage and cutoff frequency. Adjustment potentiometers for offset, fine gain and excitation are also provided. The AC1222 comes with a Cinch 251-22-30-160 (or equivalent) edge connector.

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APPLICATIONS

The 1B31 can be interfaced easily and directly to a wide variety of transducers for precise measurement of strain, torque, force and pressure. For applications in harsh industrial environments, such characteristics as high CMR, low noise and excellent temperature stability make the 1B31 unsurpassed for use in indicators, recorders and controllers.

The combination of low cost, small size and high performance of the 1B31 allows the system designer to use one conditioner per channel. The advantages include significantly lower system noise and high resolution, and elimination of crosstalk and aliasing errors.

FUNCTIONAL DESCRIPTION

Model 1B31 is based on a two-stage amplifier design and an adjustable voltage regulator section, as shown in Figure 1. The front end is a low noise, low drift, instrumentation amplifier (IA) that is optimized to amplify low level transducer signals (from 2mV full scale) riding on high common-mode voltage (±9.5V). The gain of the IA is programmed by a single resistor (1V/V to 2500V/V) and the input offset nulled out by an external potentiometer across the offset adjust Pins 9 and 10. The inverted signal ($V_{-INPUT} - V_{+INPUT}$) is brought out to Pin 8 for applications such as vibration and torque testing where the unfiltered output is required.

The signal is also fed to an inverting Butterworth filter with a fixed gain of −2V/V. This two-pole filter is preset with a 1kHz

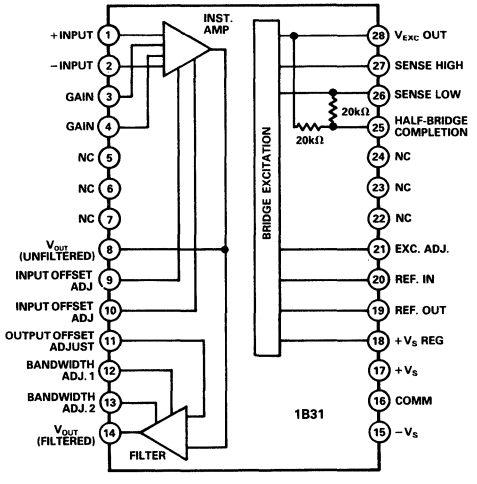


Figure 1. Block Diagram and Pinout

corner frequency which can be adjusted downwards to 10Hz by using two external capacitors or upwards to 20kHz by three resistors. This stage also provides a convenient means of adjusting output offset voltage (±10V) by connecting a 50kΩ potentiometer to Pin 11.

The bridge excitation section is an adjustable output, regulated supply with an internally provided reference voltage (+6.8V). It is configured as a gain stage with the output preset at +10V. The excitation voltage is increased by connecting a resistor between Pins 21 and 26, and decreased by connecting a resistor between Pins 19 and 20. Sense lines are provided to compensate for lead-wire resistance by effectively bringing the leads into the feedback loop.

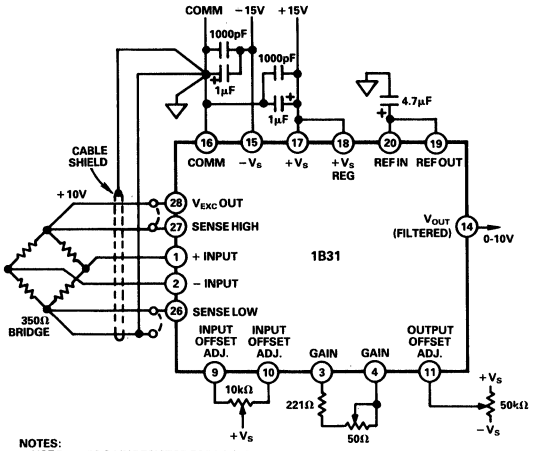
For half-bridge applications, two tracking thin-film resistors (20kΩ), ±5ppm/°C max) are connected from V_{EXC} OUT (Pin 28) to SENSE LOW (Pin 26).

OPERATING INSTRUCTIONS

Gain Setting: The differential gain, G, is determined by the equation:

$$G = 2 + \frac{80k\Omega}{R_G}$$

where R_G is connected between the GAIN terminals (Pins 3 and 4) of the IB31, as shown in Figure 2. For best performance, a low temperature coefficient (5ppm/°C) R_G is recommended. For fine span adjustment, a 50Ω potentiometer may be connected in series with R_G.



NOTES:
- USE 5ppm/°C GAIN RESISTOR FOR LOW GAIN TEMPCO.
- ALL TRIM POTS SHOULD BE 100 ppm/°C OR BETTER (TYPE 79PR 15 TURN CERMET RECOMMENDED).

Figure 2. Typical Application

Input Offset Adjustment: To null input offset voltage, an optional 10kΩ potentiometer may be connected across the INPUT OFFSET ADJ. terminals (Pins 9 and 10 in Figure 2). With gain set at the desired value, connect both inputs (Pins 1 and 2) to COMMON (Pin 16), and adjust the 10kΩ potentiometer for zero volts at Pin 14. For applications using software nulling, Pins 9 and 10 should be left unconnected.

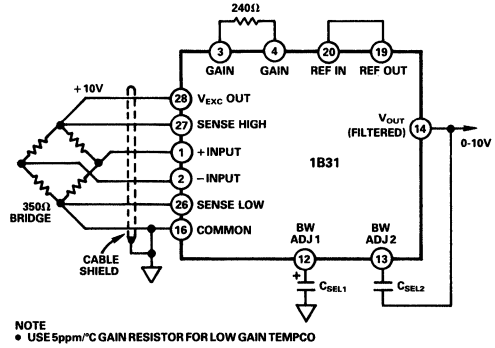
Output Offset Adjustment: The output can be offset over the ±10V range to compensate for dead load or bridge imbalance by using a 50kΩ potentiometer connected to Pin 11 as shown in Figure 2. Pin 11 is normally grounded if output offsetting is not desired.

Filter Cutoff Frequency Programming: The low pass filter cutoff frequency is internally set at 1kHz. It may be decreased from 1kHz by the addition of two external capacitors connected as shown in Figure 3 (from Pin 12 to common and between Pins 13 and 14). The values of capacitors required for a desired cutoff frequency, f_C, below 1kHz are obtained by the equations below:

$$C_{SEL1} = 0.015\mu F \left[\frac{1kHz}{f_C} - 1\right]$$

$$C_{SEL2} = 0.0022\mu F \left[\frac{1kHz}{f_C} - 1\right]$$

C_{SEL1} can be polarized for large values.



NOTE
- USE 5ppm/°C GAIN RESISTOR FOR LOW GAIN TEMPCO

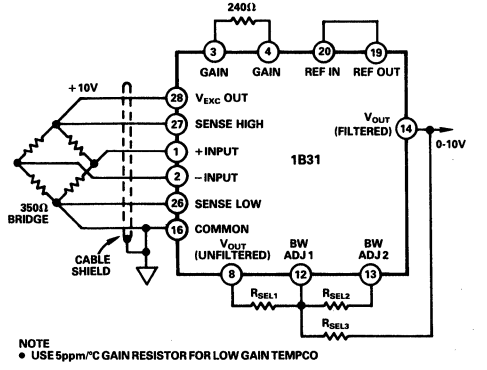
Figure 3. Narrow Bandwidth Application

The cutoff frequency may also be increased from 1kHz to 20kHz by the addition of three external resistors, connected as shown in Figure 4. The equations for determining the resistor values are:

$$R_{SEL1} = 20k\Omega / \left[\frac{f_C}{1kHz} - 1\right]$$

$$R_{SEL2} = 16k\Omega / \left[\frac{f_C}{1kHz} - 1\right]$$

$$R_{SEL3} = 40k\Omega / \left[\frac{f_C}{1kHz} - 1\right]$$



NOTE
- USE 5ppm/°C GAIN RESISTOR FOR LOW GAIN TEMPCO

Figure 4. Wide Bandwidth Application

Table I gives the nearest resistor and capacitor values for several common filter cutoff frequencies.

f_C(Hz)	C_{SEL1} (μF)	C_{SEL2} (μF)
10	1.5	0.2
50	0.27	0.039
100	0.15	0.02
200	0.056	0.0082
500	0.015	0.0022

	R_{SEL1} (kΩ)	R_{SEL2} (kΩ)	R_{SEL3} (kΩ)
2000	20	16.2	40.2
5000	4.99	4.12	10.0
10000	2.21	1.78	4.42
20000	1.05	0.866	2.21

Table I. Filter Cutoff Frequency vs. R_{SEL} and C_{SEL}

Note: The 25MHz gain bandwidth product of the IA should be considered in high-gain, wide bandwidth configurations.

Voltage Excitation Programming: The excitation voltage is preset to +10V when Pin 19 is connected to Pin 20. To increase V_{EXC} up to +15V a resistor must be connected between EXC. ADJ. and SENSE LOW (Pins 21 and 26) as shown in Figure 5. For a desired V_{EXC} the resistor value, R_{EXT}, is determined by the following equations:

$$R_T = \frac{10k\Omega \times V_{REF\ OUT}}{V_{EXC} - V_{REF\ OUT}} \quad ; \quad V_{REF\ OUT} = +6.8V$$

$$R_{EXT} = \frac{20k\Omega \times R_T}{20k\Omega - R_T}$$

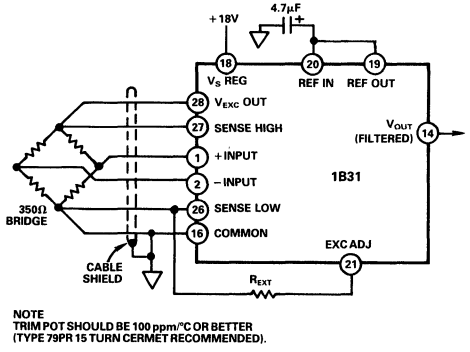


Figure 5. Increasing the Excitation Voltage: +10V to +15V Range.

To decrease V_{EXC} from +10V to +4V, a resistor has to be connected between REF IN and REF OUT (Pins 19 and 20) as shown in Figure 6. The equations to determine the value of R_{EXT} are:

$$V_{REF\ IN} = 0.68V_{EXC}$$

$$R_{EXT} = 10k\Omega \left[\frac{V_{REF\ OUT}}{V_{REF\ IN}} - 1\right] ; \quad V_{REF\ OUT} = +6.8V$$

A 20kΩ potentiometer between the REF IN and REF OUT pins will span the +4V to +10V excitation range. A 4.7μF tantalum capacitor from REF IN (Pin 20) to COMMON (Pin 16) is recommended in all cases to lower the voltage noise at the reference input.

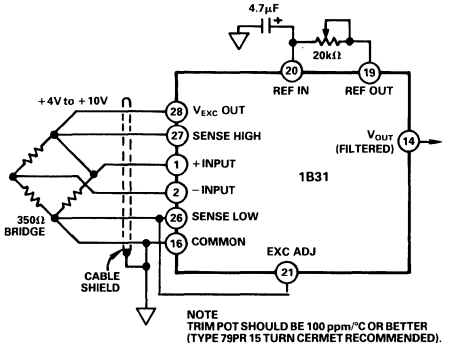


Figure 6. Decreasing the Excitation Voltage: +4V to +10V Range

The remote sensing inputs should be connected to the transducer separately from the excitation leads or jumpered as shown in Figure 2.

Power Supply Decoupling: The power supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the 1B31 as possible (Figure 2).

Input Protection: The differential inputs of the 1B31 can be protected from accidental shorts to power line voltages (115V rms) by the circuit shown in Figure 7. The back-to-back diodes clamp the inputs to a maximum of ±12.5V and were selected for low leakage current. The 15kΩ resistors in series with the inputs will degrade the noise performance of the 1B31 to 4.2μV p-p in a bandwidth of 0.1Hz to 1kHz. For six-wire load cells in harsh environments the additional protection for the sense inputs shown in Figure 7 is recommended.

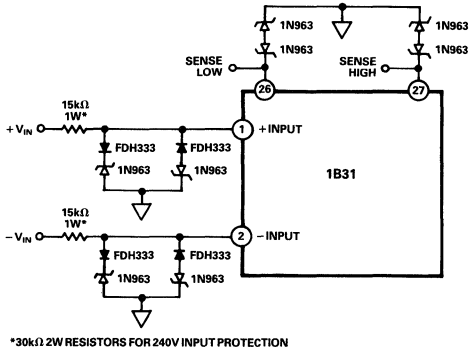


Figure 7. 115V Input Protection for 1B31

10

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Total offset voltage drift is composed of input and output drifts and is a function of gain. The 1B31 typically exhibits ±0.25μV/°C RTI drift at a gain of 1000V/V over the full temperature range. The RTI voltage offset drift vs. gain is graphed in Figure 8.

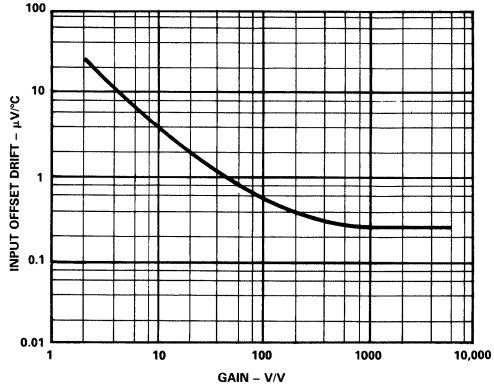


Figure 8. Total Input Offset Drift vs. Gain

Low Pass Filter: The two pole Butterworth filter is a multiple feedback design with a gain of −2V/V. It is preset at a cutoff frequency of 1kHz (−3dB) with a 40dB/decade roll-off. The step response at 1kHz is 1.5ms settling time to 0.1% of final value with less than 5% overshoot. The frequency response of the filter is shown graphically in Figure 9.

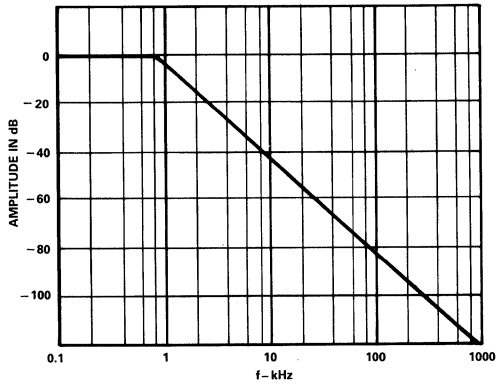
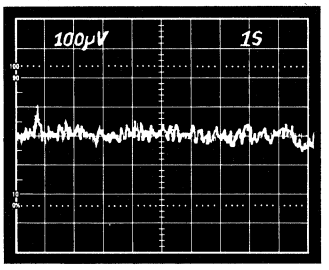
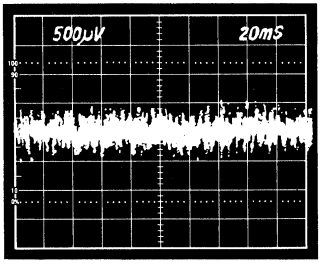


Figure 9. Filter Amplitude Response vs. Frequency

Gain Nonlinearity and Noise: Gain Nonlinearity is specified as a percent of full-scale output, and for the 1B31 it is ±0.005% maximum over the full-gain range. The IA design also offers exceptionally quiet performance with typical input noise of 0.3μV p-p for a 10Hz bandwidth (Figure 10a) and 1μV p-p for a 1kHz bandwidth (Figure 10b).



a. Bandwidth = 0.1Hz to 10Hz



b. Bandwidth = 0.1Hz to 1kHz

Figure 10. Voltage Noise, RTO @ G = 1000V/V

Common-Mode Rejection: CMR as a function of gain and frequency is shown in Figure 11. The best results (140dB @ 60Hz) are obtained by programming the low pass filter with a 10Hz cutoff frequency, which contributes an additional 30dB to the 1kHz specification where 60Hz noise is not attenuated by the filter.

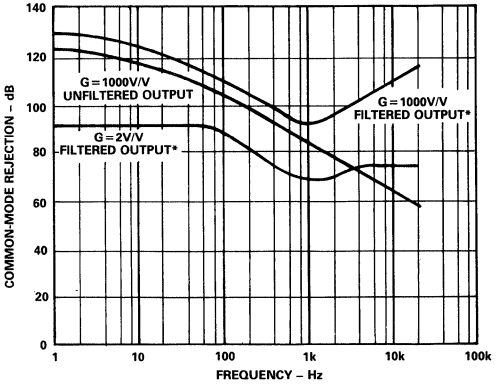


Figure 11. Common-Mode Rejection vs. Frequency and Gain

Turn On Drift: The input offset of the 1B31 stabilizes to within 1μV of final value in 5 minutes (Figure 12). The test conditions are: 350Ω bridge with +10V excitation and ambient temperature of +25°C.

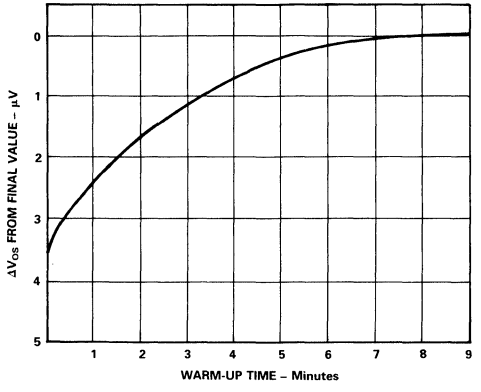


Figure 12. Offset Voltage, RTI, Turn-On Drift

Bridge Excitation: The adjustable bridge excitation is specified over a wide regulator input voltage range (+9.5V to +28V). Maximum load current I_L as a function of regulator input-output differential voltage is shown in Figure 13. The maximum output current also depends on ambient temperature and above 50°C a derating factor should be derived from Figure 14.

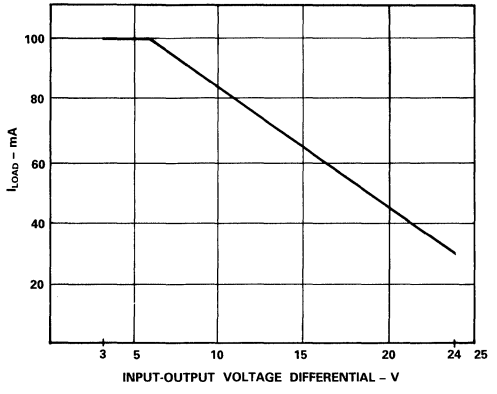


Figure 13. Excitation Source Input – Output Voltage Differential vs. Load Current; Ambient Temperature ≤25°C.

APPLYING THE 1B31

Strain Measurement: The 1B31 is shown in a strain measurement system in Figure 15. A single active gage (120Ω, Gage Factor = 2) is used in a bridge configuration to detect fractional changes in gage resistance caused by strain. An equivalent resistance

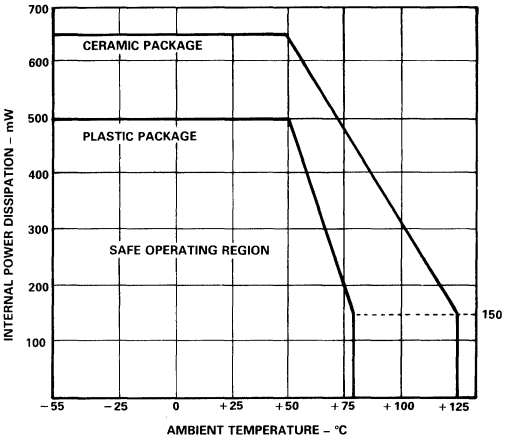


Figure 14. Excitation Source Internal Power Dissipation vs. Temperature

dummy gage mounted adjacent to the active gage provides temperature compensation. The rest of the bridge is completed by the 1B31 internal half-bridge network which consists of two 20kΩ, 1% thin-film resistors tracking to within ±5ppm/°C max. Bridge excitation is set at +4V to avoid self-heating errors from the strain gage. System calibration produces a +1V output for an input of 1000 microstrains. The filter cutoff frequency is set at approximately 100Hz.

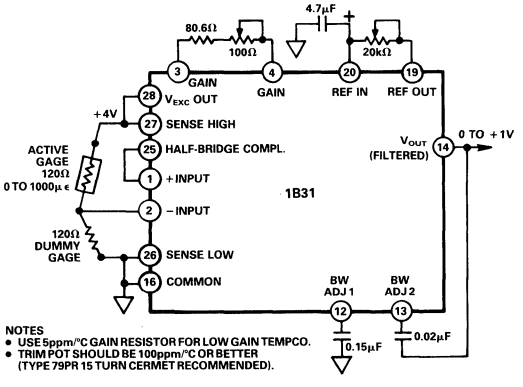


Figure 15. Strain Gage Application Using Internal Half-Bridge

Pressure Transducer Inferface: A strain gage type pressure transducer (Dynisco 800 series) is interfaced to a 1B31 in Figure 16. Regulated excitation of +10V dc is provided for a 30mV full-scale output. The gain is sett at 333.3 to achieve a 0-10V output for a 0-10,000 psi range of the transducer. A shunt calibration resistor is built into the transducer for easy verification of the 80% point of its full-scale output. A typical shielding scheme to preserve the excellent performance characteristics of the 1B31 is also shown. To avoid ground loops, signal return or cable shield should be grounded only at one point.

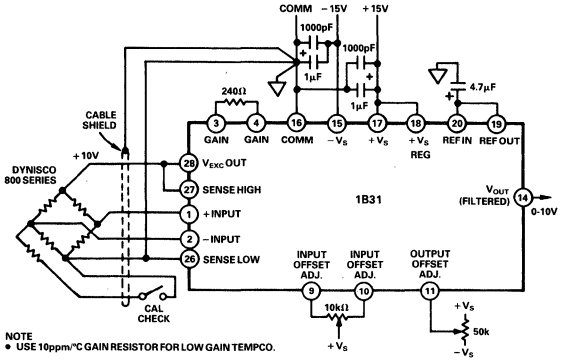


Figure 16. Pressure Transducer Application

Multiple Load-Cells: For transducer configurations where the maximum load current of 100mA of the 1B31 is not sufficient, a buffer and a power transistor such as a TIP31 can be used as shown in Figure 17. This design can supply 300mA at +10V excitation over the full industrial temperature range (−25°C to +85°C). In a multiple 1B31 system an added advantage is that ratiometric operation can be preserved by using one excitation source which also serves as the reference voltage for the system A/D converter.

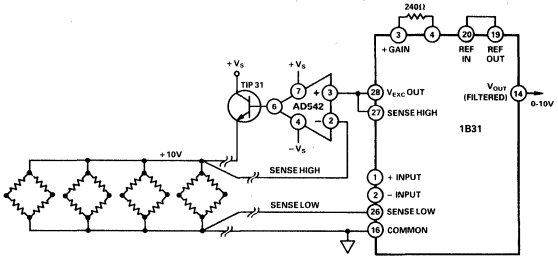


Figure 17. Multiple Load-Cell Application

Mobile Transducer Application: The small size and reliability of the 1B31 make it an ideal choice for mobile applications. Since the 1B31 requires a negative supply, one possible solution for its generation is shown in Figure 18. The positive voltage of a +12V battery is used to drive a CMOS TLC555 oscillator with a typical supply current of 360µA. The output is a square wave that is rectified by the diodes and filtered to provide a −9V supply. Excitation voltage should be equal to or less than +9V for adequate headroom for the 1B31 voltage regulator.

Pressure Transducer Data Acquisition System: Figure 19 shows a two module solution for microcomputer based data acquisition using a 1B31 and an AD1170 18-bit A/D converter. A 3mV/V pressure transducer (e.g. Dynisco 800 series) is interfaced to a 1B31 set up with a gain of 333.3 to give a 0 – 5V output. The regulated excitation is +5V, and for ratiometric operation it is also used as the voltage reference input for the AD1170. An initial ECAL command establishes the voltage excitation as the full-initial-scale input of the AD1170 and periodic calibration cycles keep the converter tracking the reference input. This configuration yields very high CMR (168dB @ 60Hz) enhanced by the 1B31 low pass filter and the integrating conversion scheme of the

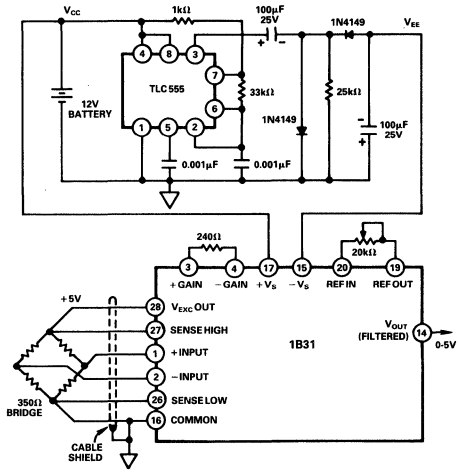


Figure 18. Negative Supply Generation for 1B31

AD1170. In addition, fixed offsets caused by bridge imbalance can be nulled out by the AD1170 with a power-up initialization command from the microcomputer. This eliminates a potentiometer or software overhead which might otherwise be needed.

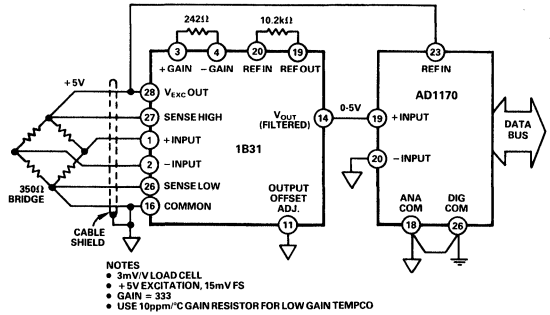


Figure 19. Pressure Transducer Data Acquisition Using 1B31 and AD1170

Isolated Current Loop Interface: The output of the 1B31 can be interfaced to a process loop as shown in Figure 20. The 2B23 module produces an isolated 4-to-20mA output current which is proportional to the input voltage and independent of the output load resistance. Common-mode input/output isolation is ±1500V pk continuous.

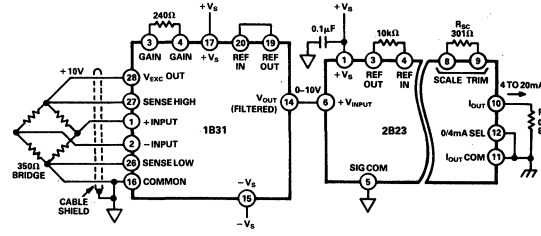


Figure 20. Isolated 4-20mA Transmitter

ANALOG DEVICES

Bridge Transducer Signal Conditioner

1B32

FEATURES
- **Low Cost**
- **Complete Signal-Conditioning Solution**
- **Small Package: 28-Pin Double DIP**
- **Internal Thin-Film Gain Network**
- **High Accuracy**
  - **Low Input Offset Tempco: ±0.07μV/°C**
  - **Low Gain Tempco: ±2ppm/°C**
  - **Low Nonlinearity: ±0.005% max**
  - **High CMR: 140dB min (60Hz, G=1000V/V)**
- **Programmable Bridge Excitation: +4V to +15V**
- **Remote Sensing**
- **Low Pass Filter (f_C=4Hz)**

APPLICATIONS
- **Weigh Scales**
- **Instrumentation: Indicators, Recorders, Controllers**
- **Data Acquisition Systems**
- **Microcomputer Analog I/O**

GENERAL DESCRIPTION

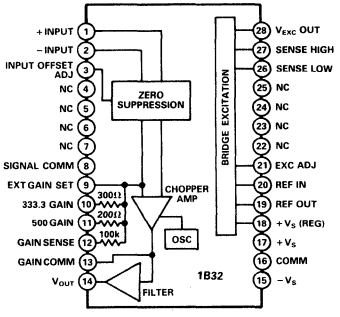
Model 1B32 is a precision, chopper-based, signal-conditioning component ideally suited for high-accuracy applications of load cells and bridge transducers. Packaged in a compact 28-pin plastic double DIP, the 1B32 takes advantage of hybrid technology for high reliability as well as higher channel density. Functionally, the signal conditioner consists of three basic parts: a high performance chopper-based amplifier, a low-pass filter and an adjustable transducer excitation source.

The chopper-based amplifier features extremely low input offset tempco of ±0.07μV/°C (RTI, G=500V/V) and excellent nonlinearity of ±0.005% max over its full gain range of 100 to 5000V/V. The 1B32 has a thin-film resistor network for pin-strapping the gain to 500V/V or 333.3V/V (for 2mV/V and 3mV/V load cells). The gain tempco for these fixed gains is a highly stable ±2ppm/°C. Additionally, the gain can be set to any value in the gain range with two external resistors. The amplifier also has a wide-range input referred zero suppression capability (±10V), which can easily be interfaced to a D/A converter. The bandwidth of the chopper is 4Hz at G=100V/V.

The integral three-pole, low-pass filter offers a 60dB/decade roll-off from 4Hz to reduce common-mode noise and improve system signal-to-noise ratio.

The 1B32's regulated transducer excitation stage features low output drift (±40ppm/°C typ) and can drive 120Ω or higher resistance load cells. The excitation is preset at +10V with other voltages between +4V and +15V programmable with external resistors. This section also has remote sensing capability to allow for lead-wire compensation in 6-wire load cells and other bridge configurations.

FUNCTIONAL BLOCK DIAGRAM



The 1B32 is fully specified over the industrial (−25°C to +85°C) temperature range.

DESIGN FEATURES AND USER BENEFITS

Pin-Strappable Gain: The internal resistor network can be pin-strapped for gains of 500V/V and 333.3V/V for 2mV/V and 3mV/V load cells. The tracking network guarantees a gain tempco of ±6ppm/°C max.

Custom Trimmable Network: For volume applications, the 1B32 can be supplied with a custom laser trimmed gain network. Contact factory for further information.

Wide Range Zero Suppression: The output can be offset by ±10V for nulling out a dead load or to do a tare adjustment.

Remote Sensing: Voltage drops across the excitation lead-wires are compensated by the regulated supply, making 6-wire load-cell interfacing straightforward.

Programmable Transducer Excitation: The excitation source is preset for +10V dc operation without external components. It is user-programmable for a +4V to +15V dc range (@ 100mA) to optimize transducer performance.

Low-Pass Filter: The three-pole active filter (f_C=4Hz) reduces 60Hz line noise and improves system signal-to-noise ratio.

10

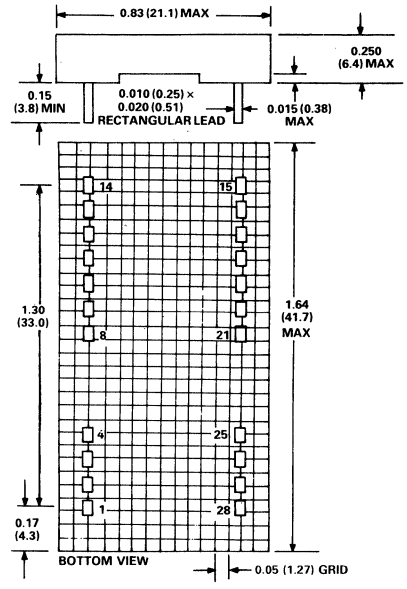
1B32—SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

Model	1B32AN
GAIN	
Gain Range	100V/V to 5000V/V
Internal Gain Setting	333.3V/V and 500V/V
External Gain Equation	$G = 1 + \frac{R_F}{R_I}; G \geq 100$
Gain Accuracy[1]	±0.1%
Gain Temperature Coefficient[2]	±2ppm/°C (±6ppm/°C max)
Gain Nonlinearity	±0.005% max
OFFSET VOLTAGES	
Total Offset Voltage, RTI	
Initial, @ +25°C, G = 1000V/V	±40μV
Warm-Up Drift, G = 1000V/V, 10 min	Within ±1μV of final value
vs. Temperature (−25°C to +85°C)	
G = 1000V/V	±0.07μV/°C (±0.2μV/°C max)
At Other Gains	$\pm\left(0.06 + \frac{15}{G}\right)\mu V/°C$
Output Offset Adjust Range	±10V
INPUT BIAS CURRENT	
Initial @25°C	±3nA
vs. Temperature (−25°C to +85°C)	±50pA/°C
INPUT DIFFERENCE CURRENT	
Initial @ +25°C	±3nA
vs. Temperature (−25°C to +85°C)	±10pA/°C
INPUT RESISTANCE	
Differential	100MΩ
Common Mode	100MΩ
INPUT VOLTAGE RANGE	
Linear Differential Input	±0.1V
Maximum Differential Input	+5V
CMV Input Range	0 to +7.5V
CMR, 1kΩ Source Imbalance[3]	
G = 100V/V to 5000V/V @ dc	86dB
G = 100V/V, @ 60Hz	120dB
G = 1000V/V, @ 60Hz	140dB min
INPUT NOISE	
Voltage, G = 1000V/V	
0.1Hz to 10Hz	1μV p-p
Current, G = 1000V/V	
0.1Hz to 10Hz	3pA p-p
RATED OUTPUT	
Voltage, 2kΩLoad, min	±10V
Current	±5mA
Impedance, dc to 2Hz, G = 100V/V	0.6Ω
Load Capacitance	500pF
Output Short Circuit Duration (to Ground)	Indefinite
DYNAMIC RESPONSE	
Small Signal Bandwidth	
−3dB Gain Accuracy, G = 100V/V	4Hz
G = 1000V/V	3.5Hz
Slew Rate	20V/sec
Full Power	0.5Hz
Settling Time, G = 100V/V, ±10V Output Step to ±0.1%	2sec
LOW PASS FILTER	
Number of Poles	3
Cutoff Frequency (−3dB Point)	4Hz
Roll-Off	60dB/decade

(Continued on next page)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



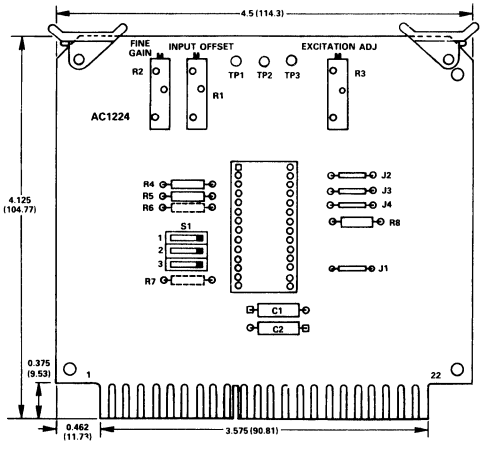
PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+INPUT	15	$-V_S$
2	−INPUT	16	COMM
3	INPUT OFFSET ADJ	17	$+V_S$
4	NC	18	$+V_S$ REG
5	NC	19	REF OUT
6	NC	20	REF IN
7	NC	21	EXC ADJ
8	SIGNAL COMM	22	NC
9	EXT GAIN SET	23	NC
10	333.3 GAIN	24	NC
11	500 GAIN	25	NC
12	GAIN SENSE	26	SENSE LOW
13	GAIN COMM	27	SENSE HIGH
14	V_{OUT}	28	V_{EXC} OUT

Model	1B32AN
BRIDGE EXCITATION	
Regulator Input Voltage Range	+9.5V to +28V
Output Voltage Range	+4V to +15V
Regulator Input/Output Voltage Differential	+3V to +24V
Output Current[4]	100mA max
Regulation, Output Voltage vs. Supply	±0.05%/V
Load Regulation, I_L = 1mA to 50mA	±0.1%
Output Voltage vs. Temperature (−25°C to +85°C)	±40ppm/°C
Output Noise, 0.1Hz to 10Hz[5]	300μV p-p
Reference Voltage (Internal)	+6.8V ±5%
Sense & Excitation Lead Resistance	10Ω max
POWER SUPPLY	
Voltage, Rated Performance	±15V dc
Voltage, Operating	±12V to ±18V dc
Current, Quiescent[6]	+4mA, −1mA
ENVIRONMENTAL	
Temperature Range	
Rated Performance	−25°C to +85°C
Operating	−40°C to +85°C
Storage	−40°C to +100°C
Relative Humidity	0 to 95%, Noncondensing, @ +60°C
CASE SIZE	0.83" × 1.64" × 0.25" (21.1 × 41.7 × 6.35mm) max

NOTES
[1]Using internal network for gain.
[2]For pin-strapped gain. The tempco of the individual thin-film resistors is ±50ppm/°C max.
[3]3V p-p 60Hz common-mode signal used in test setup.
[4]Derate 2mA/°C from +50°C.
[5]4.7μF capacitor from REF IN (Pin 20) to COMM.
[6]Excluding bridge excitation current and with no loading on the output.
Specifications subject to change without notice.

AC1224 Mounting Card



AC1224 GAIN SETTINGS VIA SWITCH S1

GAIN	S1–1	S1–2	S1–3
333	CLOSED	OPEN	CLOSED
500	OPEN	CLOSED	CLOSED
EXTERNAL	OPEN	OPEN	OPEN

AC1224 CONNECTOR DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
T	V_{EXC} OUT	1	+INPUT
U	SENSE HIGH	2	−INPUT
V	SENSE LOW	12	V_{OUT}
X	REF OUT	19	$-V_S$
Y	REF IN	20	COMM
Z	EXC ADJ	21	$+V_S$
		22	$+V_S$ REG

The AC1224 mounting card is available for the 1B32. The AC1224 is an edge connector card with a socket for plugging in the 1B32. In addition it has provisions for switch selecting internal gains as well as installing gain resistors. Adjustment pots for offset, fine gain and excitation are also provided. The AC1224 comes with a Cinch 251-22-30-160 (or equivalent) edge connector.

FUNCTIONAL DESCRIPTION

Model 1B32 is based on a switched capacitor, chopper based amplifier followed by an active filter and an adjustable voltage regulator section for excitation. The ultralow drift chopper samples the difference between the +INPUT and −INPUT at 190Hz. The signal is modulated, amplified and then demodulated. This stage introduces a pole with a 20dB/decade rolloff from 4Hz. The high-level signal is then filtered by a two-pole active filter with a 4Hz cutoff frequency to give a ±10V output. The clock signal for the chopper is generated by an on-board oscillator.

As shown in Figure 1, the gain can be pin-strapped by an internal resistor network. Standard gains of 333.3 and 500 can be achieved by this method with gain tempco of ±6ppm/°C max. Finally, the offset adjust of the amplifier is input referred, and requires a voltage input similar to the differential input voltage to implement wide range suppression.

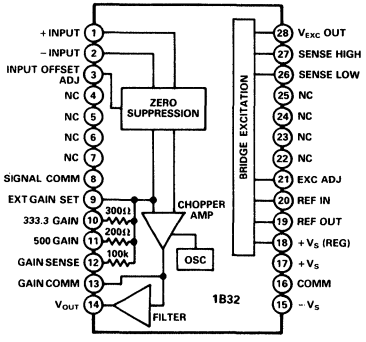


Figure 1. 1B32 Block Diagram and Pinout

The bridge excitation section is an adjustable output, regulated supply with an internally provided reference voltage (+6.8V). It is configured as a gain stage with the output preset at +10V. The excitation voltage is increased by connecting a resistor between Pins 21 and 26. Sense lines are provided to compensate for lead-wire resistance by bringing the leads into the feedback loop.

OPERATING INSTRUCTIONS

Ground Connections: Signal common (Pin 8) and power common (Pin 16) are not internally connected within the 1B32. These pins must be connected together externally or excessive current will be drawn.

Gain Setting: The differential gain of the 1B32 can be either pin-strapped or programmed externally with two resistors. The internal thin-film gain network (Figure 1) provides gains of 500 and 333.3 for standard load-cell sensitivities of 2mV/V and 3mV/V. This is achieved by connecting GAIN SENSE (Pin 12) to GAIN COMM (Pin 13) and grounding Pin 10 or Pin 11 (Figure 2). The gain tempco using the internal network is an excellent ±2ppm/°C typ (±6ppm/°C max).

To program the gain externally, two resistors are connected as shown in Figure 3. The gain equation is:

$$G = 1 + \frac{R_F}{R_I}$$

The gain-strapping Pins (10 and 11) and GAIN SENSE (Pin 12) are left unconnected, effectively floating the internal network.

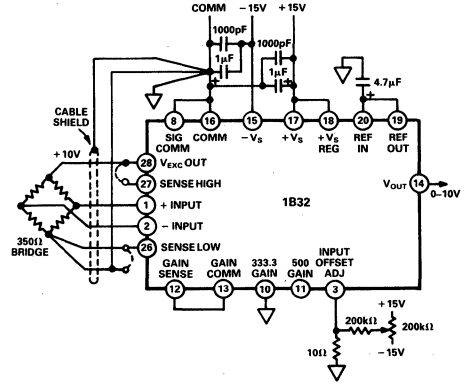


Figure 2. Internal Gain Strapping

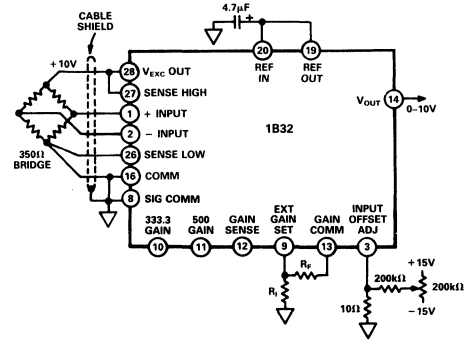


Figure 3. External Gain Setting

Offset Adjustment: The input-referred offset adjust has the same sensitivity as the inputs of the 1B32. The voltage level at INPUT OFFSET ADJ (Pin 3) is gained by the same factor as the input signal to provide a ±10V output adjust. Figure 2 shows an external network and potentiometer set up for a ±7.5mV span at the input, which gives a ±2.5V (7.5mV × 333.3) output adjust capability. Wider ranges can be chosen with the appropriate resistor and potentiometer values.

Note: If offset adjustment is not required, Pin 3 must be grounded.

Voltage Excitation Programming: The excitation voltage is preset to +10V. To increase V_{EXC} up to +15V a resistor must be connected between EXC ADJ and SENSE LOW (Pins 21 and 26) as shown in Figure 4.

The V_S (REG) input (Pin 18) must be raised to +18V to satisfy the +3V min input-output voltage differential of the regulator. Consult the Performance Characteristics section for safe operating conditions of the regulator. For a desired V_{EXC} the resistor value, R_{EXT}, is determined by the following equations:

$$R_T = \frac{10k\Omega \times V_{REF\ OUT}}{V_{EXC} - V_{REF\ OUT}} \quad ; \quad V_{REF\ OUT} = +6.8V$$

$$R_{EXT} = \frac{20k\Omega \times R_T}{20k\Omega - R_T}$$

The +10V to +15V range can be covered by a 20kΩ potentiometer between REF IN (Pin 20) and REF OUT (Pin 19). R_{EXT} of

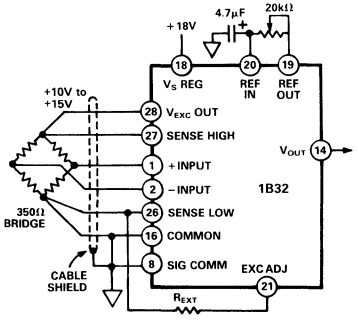


Figure 4. Constant Voltage Excitation: +10V to +15V Range.

200kΩ is recommended for fine adjustment at +10V excitation voltage.

Similarly to decrease V_{EXC} down to +4V, connect a 20kΩ potentiometer between Pins 19 and 20, as shown in Figure 5.

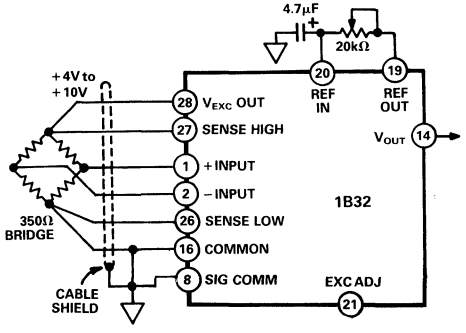


Figure 5. Constant Voltage Excitation: +4V to +10V Range.

A 4.7µF tantalum capacitor from REF IN (Pin 20) to COMMON (16) is recommended in all cases to lower the voltage noise at the reference input.

The remote sensing inputs should be connected to the transducer separately from the excitation leads or jumpered as shown in Figure 2. The resistance of the excitation and sense lines should not exceed 10Ω.

Power Supply: The V_S REG input (Pin 18) should be connected to $+V_S$ (Pin 17) even if the bridge excitation section is not used. Also the power supplies should be decoupled with 1µF tantalum and 1000pF ceramic capacitors as close to the 1B32 as possible (Figure 2).

Input Protection: The 1B32 differential inputs can be protected from accidental shorts to power line voltages (115V rms) by the circuit shown in Figure 6. The back-to-back diodes clamp the inputs to a maximum of ±12.5V and were selected for low leakage current. The 15kΩ resistors in series with the inputs will degrade the noise performance of the 1B32 to 4µV p-p (0.1Hz to 10Hz). When interfacing with six-wire load cells in harsh environments, input protection for the sense inputs is also recommended (Figure 6).

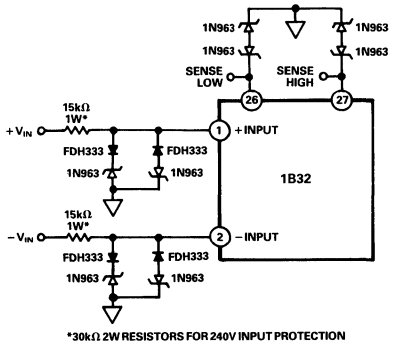


Figure 6. 115V Input Protection

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: The chopper front end of the 1B32 gives it excellent input offset stability. As shown in Figure 7, it typically exhibits drift of ±0.07µV/°C RTI at a gain of 1000V/V (±75µV/°C RTO). The measurement is two-point, and is taken at −25°C and +85°C, which covers the specified temperature range of the 1B32.

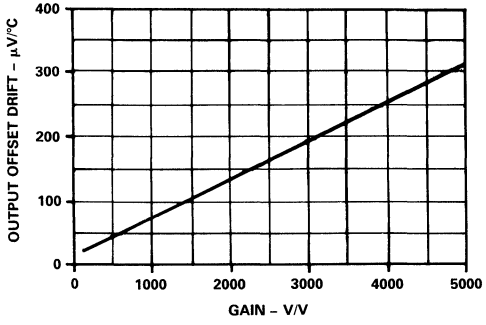


Figure 7. Total Output Offset Drift vs. Gain

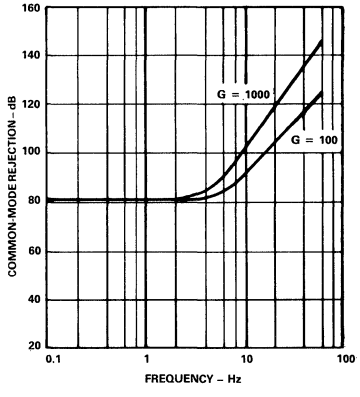


Figure 8. Common-Mode Rejection vs. Frequency

Common-Mode Rejection: CMR as a function of frequency is shown in Figure 8. Test conditions are a 3V p-p common-mode signal and 1kΩ source imbalance. The CMR improves with increasing gain. Note that the 4Hz filter enhances the CMR performance above the corner frequency by attenuating the normal-mode signal at 60dB/decade.

Gain Nonlinearity and Noise: Gain Nonlinearity is specified as a percent of full-scale output, and for the 1B32 it is ±0.005% max over the full span. The chopper design also offers exceptional low-noise performance, with typical input noise of 1μV p-p in the 0.1Hz to 10Hz bandwidth (Figure 9).

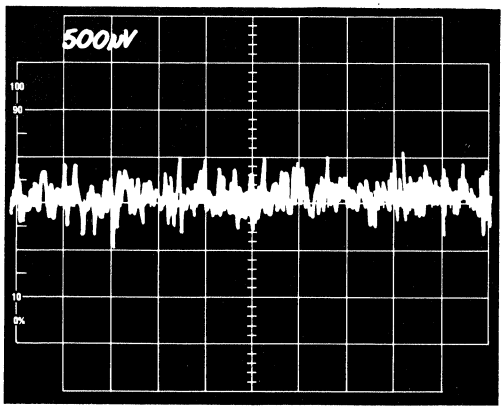


Figure 9. Voltage Noise, 0.1Hz to 10Hz, G = 1000

Low-Pass Filter: The 1B32 has three poles at 4Hz in its design. One is introduced in the amplifier, while the other two are provided by an active Butterworth filter following the amplifier. Total roll-off is 60dB/decade from 4Hz. The frequency response of the filter is shown in Figure 10.

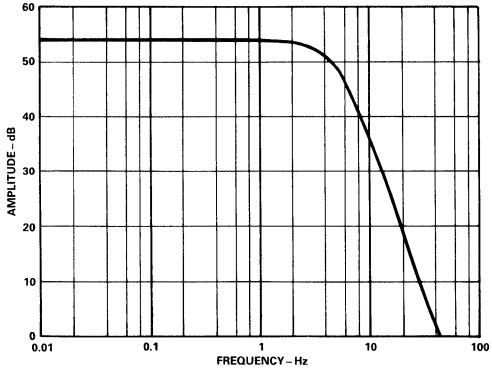


Figure 10. Filter Amplitude Response vs. Frequency, G = 500

Turn-On Drift: The 1B32 offset voltage typically stabilizes to within 1μV of its final value in 10 minutes (Figure 11). The test conditions are: 350Ω bridge with a +10V excitation and ambient temperature of +25°C.

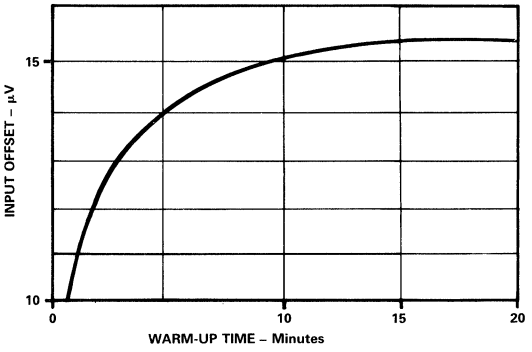


Figure 11. Offset Voltage RTI, Turn-On Drift

Bridge Excitation: The adjustable bridge excitation is specified over a wide regulator input voltage range (+9.5V to +28V). Maximum load current I_L as a function of regulator input-output differential voltage is shown in Figure 12. The maximum output current also depends on ambient temperature, and above +50°C a derating factor of 2mA/°C must be applied. The safe operating region for internal power dissipation vs. temperature is graphed in Figure 13.

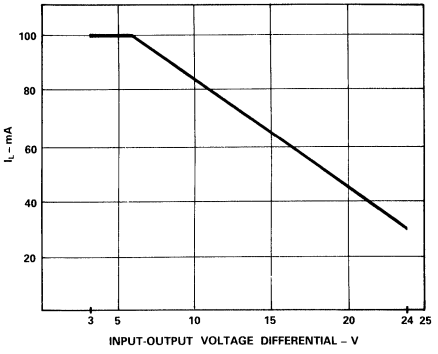


Figure 12. Excitation Source Load Current vs. Input-Output Voltage Differential, ≤25°C

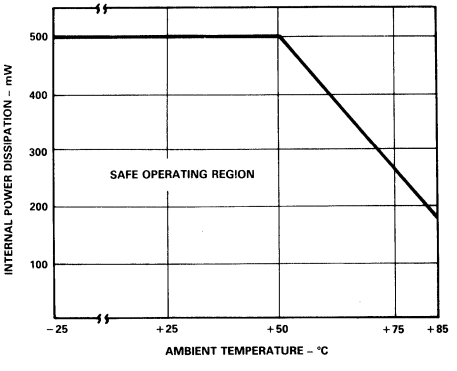


Figure 13. Excitation Source Internal Power Dissipation vs. Temperature

APPLYING THE 1B32

Pressure Transducer Interface: A strain gage type pressure transducer (Dynisco 800 series) is interfaced to a 1B32 in Figure 14. Regulated excitation of +10V dc is provided for a 30mV full-scale output for a 0-10,000 psi range of the transducer. A shunt calibration resistor is built into the transducer for easy verification of the 80% point of its full-scale output. A typical shielding scheme to preserve the excellent performance characteristics of the 1B32 is also shown. To avoid ground loops, signal return and cable shield should be grounded only at one point.

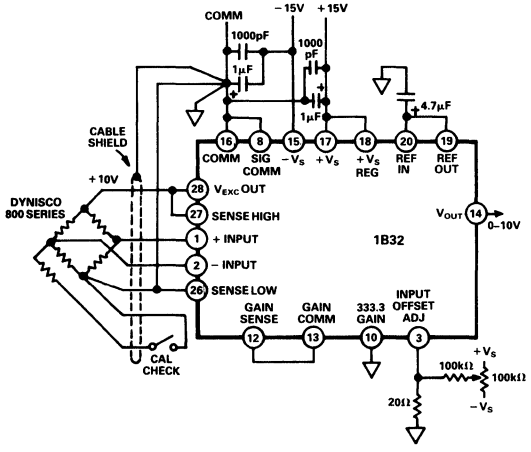


Figure 14. Pressure Transducer Interface

Pressure Transducer Data Acquisition System: A two module solution for microcomputer based data acquisition using a 1B32 and an AD1170 18-bit A/D converter is shown in Figure 15. A 3mV/V pressure transducer (e.g. Dynisco 800 series) is interfaced to a 1B32 configured with a gain of 333.3, to provide a 0 to 5V output. The regulated excitation is +5V, and is used as the reference input for the AD1170 to produce ratiometric operation. This configuration yields very high CMR enhanced by the 1B32 low pass filter and the integrating conversion scheme of the AD1170.

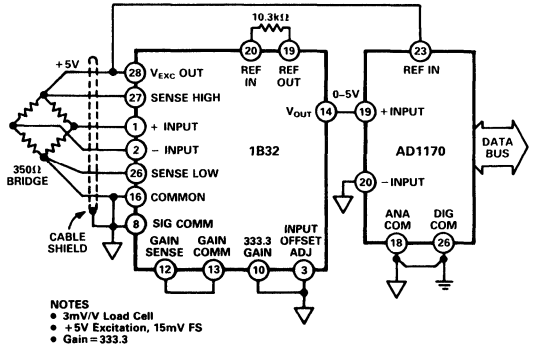


Figure 15. Auto-Calibrating Data Acquisition Using 1B32 and AD1170

In addition, fixed offsets caused by bridge imbalance can be nulled out by the AD1170 with a power-up initialization command from the microcomputer. The full-scale output of the 1B32 and transducer can be normalized to the AD1170 full scale through the electronic calibration command ECAL. Both the offset and full-scale correction data will then be stored in nonvolatile memory to eliminate the need for the trim process after each power-up. The AD1170 eliminates a potentiometer or software overhead which might otherwise be needed for these functions.

Multiple Load-Cells: For transducer configurations where the maximum load current of the 1B32 is not sufficient, a buffer and a power transistor such as a TIP31 can be used as shown in Figure 16. This approach will supply 300mA at +10V excitation over −25°C to +85°C temperature range. In a multiple 1B32 system an added advantage is that ratiometric operation can be preserved by using the excitation voltage as the reference for the system A/D converter.

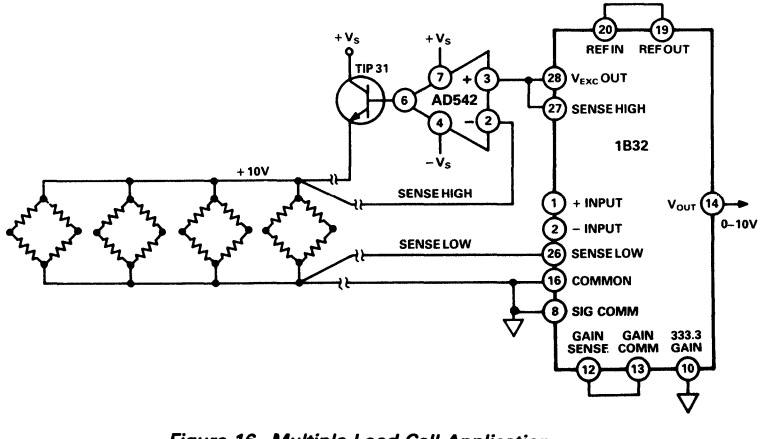


Figure 16. Multiple Load-Cell Application

Mobile Transducer Applications: The small size and reliability of the 1B32 make it an excellent choice for mobile applications. Since the 1B32 requires bipolar supplies, a possible circuit to provide the negative voltage is shown in Figure 17. The CMOS TLC555 is powered by a +12V battery, and typically draws 360μA. The output is a square wave that is rectified by the diodes and filtered to provide a −9V supply. Excitation voltage should be equal to or less than +9V for adequate headroom for the 1B32 voltage regulator. Note that the 1B32 will operate with ±9V supplies as long as the excitation voltage and the output range are less than 5V.

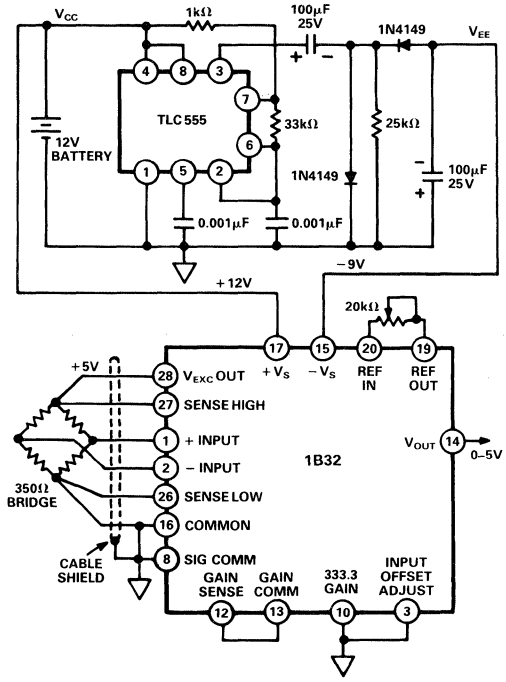


Figure 17. Negative Supply Generation for 1B32

Digital Output Offset Adjust: A 10-bit multiplying DAC such as the AD7533 can be used to control the output offset of the 1B32 as shown in Figure 18. The DAC is configured for unipolar operation with an AD OP-07 generating a voltage output. This 0-10V output is attenuated by R_1 and R_{SEL} and superposed on another fixed voltage derived from V_{EXC}. Thus the voltage at Pin 3 (INPUT OFFSET ADJUST) is insensitive to the tempco of the excitation voltage since it is also used as the reference of the DAC. For best performance R_1 and R_2 should track to ±5ppm/°C. As an example, a ±5V output adjustment can be obtained by using R_{SEL} = 200Ω for G = 500 and V_{EXC} = 10V.

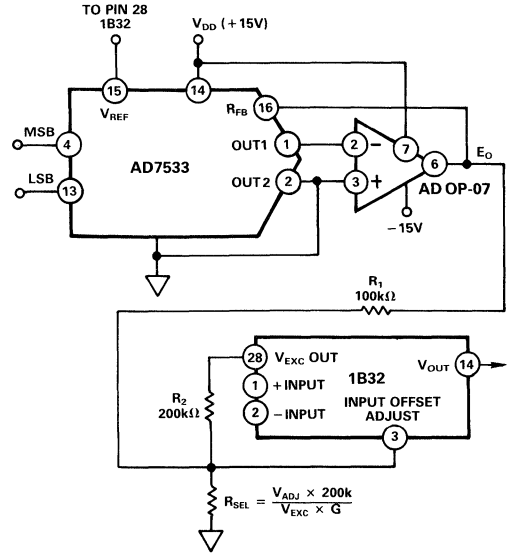


Figure 18. Output Offset Adjust Using a 10-Bit DAC

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (E_O as shown in Figure 18)
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{1024}\right)=\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{1024}\right)=0$

Table I. Unipolar Binary Code Table

ANALOG DEVICES

Isolated RTD Signal Conditioner

1B41

FEATURES

Complete RTD Signal Conditioning Solution
Resistor Programmable Linearization
Lead Resistance Compensation
High CMV Isolation: 1500 V rms Continuous
High Accuracy
Low Input Offset Tempco: 0.002 Ω/°C
Linearization Conformance: ±0.1% FSR
High CMR: 160 dB (60 Hz, G = 1000 V/V)
Small Package: 1.0″×2.1″×0.35″ DIP
Low Pass Filter (f_C = 3 Hz)
Pin Compatible with 1B51 Isolated mV/Thermocouple Conditioner

APPLICATIONS

Multichannel RTD Temperature Measurement
Industrial Measurement and Control Systems
Data Acquisition Systems

GENERAL DESCRIPTION

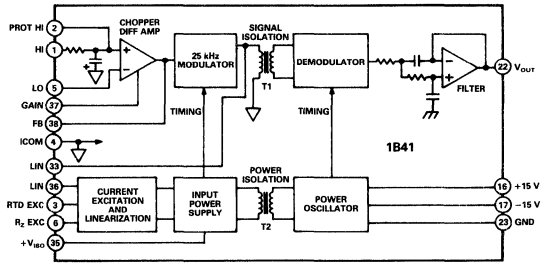
The 1B41 is a precision, isolated, RTD signal conditioner that incorporates a circuit design utilizing transformer based isolation and automated surface mount manufacturing technology. It provides an unbeatable combination of versatility and performance in a compact plastic package. Designed for measurement and control applications, it is especially suited for harsh environments with extremely high common mode interference. Unlike expensive solutions that require separate dc/dc converters, each 1B41 generates its own floating current excitation, providing true low cost channel-to-channel isolation.

Functionally, the signal conditioner consists of four basic sections: chopper stabilized amplifier, isolation, current excitation and output filter. The amplifier section allows an RTD resistance range of 20 Ω to 5 kΩ. Wide range zero suppression can be implemented at this stage.

The isolation section has complete input to output galvanic isolation of 1500 V rms continuous by the use of transformer coupling techniques. A stable sensor excitation provides 0.25 mA for most RTD applications. For platinum RTDs the excitation is internally compensated to provide an output that is linear with temperature. Filtering at 3 Hz is implemented by a passive antialiasing filter at the input and a two-pole active filter at the output. Overall NMR is 60 dB and CMR is 160 dB min @ 60 Hz.

The 1B41 is fully specified over −25°C to +85°C and operates over the industrial (−40°C to +85°C) temperature range.

FUNCTIONAL BLOCK DIAGRAM



DESIGN FEATURES AND USER BENEFITS

Ease of Use: The 1B41 has direct RTD interface with minimum external parts required to get a high-level, conditioned signal.

Lead Resistance Compensation: Voltage drops in RTD lead wires are compensated by the use of matching current sources in the 1B41.

High Noise Rejection: The combination of a chopper stabilized front end with a low pass filter provides high system accuracy in harsh industrial environments as well as good rejection of 50/60 Hz noise.

Small Size: The 1B41 package size (1.00″×2.1″×0.35″) and functional completeness makes it an excellent choice in systems with limited board space and clearance.

Wide Range Zero Suppression: This input referred function is a convenient way to null large input offsets. A single resistor value sets the RTD resistance for which the output is zero volts.

Low Pass Filter: The three-pole active filter (f_C = 3 Hz) reduces 50/60 Hz noise and aliasing errors.

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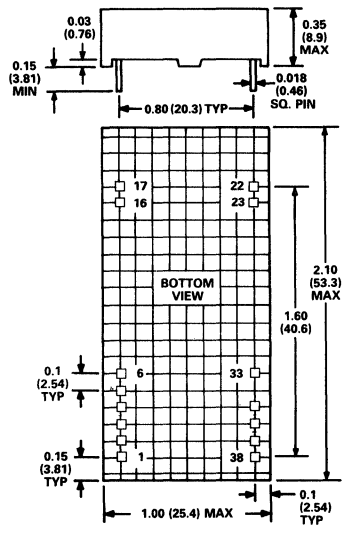
1B41—SPECIFICATIONS (typical @ +25°C and V_S = +15 V unless otherwise noted)

Model	1B41AN	1B41BN
INPUT SPECIFICATIONS		
Sensor Type	Pt 100 Ω @ 0°C, α = 0.00385, 0.00392	*
Linear Input Resistance Range	20 Ω to 5 kΩ Full Scale	*
Max InputVoltage Range	+1 V to −5 V	*
Input Offset	0.5 Ω (2 Ω max)	*
Input Offset Tempco	0.002 Ω/°C (0.01 Ω/°C max)	*
Max CMV, Input to Output		
ac, 60 Hz, Continuous	1500 V rms	*
Continuous, dc	±2000 V peak	*
CMR, @ 60 Hz, 1 kΩ Source Imbalance	160 dB min	*
NMR, @ 60 Hz	60 dB min	*
Common Mode Transient Protection	IEEE-STD 472 (SWC)	*
Sensor Current Excitation	0.25 mA	*
Current Source Matching	1.5 μA	*
OUTPUT SPECIFICATIONS		
Voltage, 2 kΩ Load, min	±10 V	*
Current	±5 mA	*
Output Offset Voltage		
Initial	50 mV typ	25 mV typ
vs. Temperature	175 μV/°C	50 μV/°C
Output Noise, dc to 100 kHz	1 mV pk-pk	*
Impedance, dc	0.1 Ω	*
ACCURACY		
Gain Accuracy[2]	2% FSR (5% FSR max)	*
Gain Tempco (0 to +70°C)	±50 ppm/°C	*
(−25°C to +85°C)	±75 ppm/°C	*
Gain Nonlinearity	±0.035%	±0.025%
Linearization Conformance		
Pt 100 Ω	0.1% FSR	
0 to +600°C	0.09% FSR	*
0 to +200°C	0.06% FSR	*
0 to +100°C	0.06% FSR	*
−100°C to +100°C	0.06% FSR	*
Lead Wire Compensation	0.01 Ω/Ω	*
DYNAMIC RESPONSE		
Bandwidth, −3 dB	dc to 3 Hz	*
POWER SUPPLY		
Voltage, Rated Performance	±15 V dc	*
Voltage, Operating	±13.5 V to ±18 V	*
Current, Quiescent	+12 mA, −4 mA	*
ENVIRONMENTAL		
Temperature Range		
Rated Performance	−25°C to +85°C	*
Operating	−40°C to +85°C	*
Storage	−40°C to +85°C	*
Relative Humidity	0 to 95% @ 60°C	*
CASE SIZE	1.0″×2.1″×0.35″	*
	(25.4×53.3×8.9) mm	*

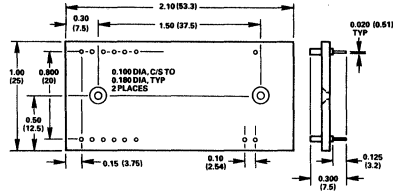
NOTES
*Specifications same as 1B41AN.
[1]All specifications use the test circuit of Figure 1.
[2]Excluding external ranging resistor errors.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC 1227 MATING SOCKET

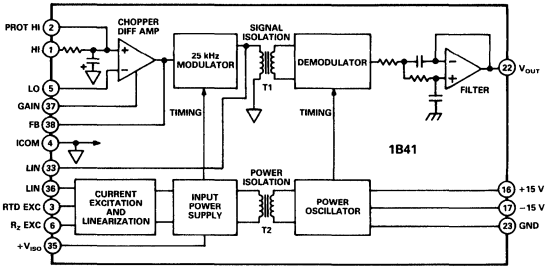


PIN DESIGNATIONS

PIN	DESIGNATION
1	HI
2	PROT HI
3	RTD EXC
4	ICOM
5	LO
6	R_Z EXC
16	+15 V
17	−15 V
22	V_O
23	GND
33	LIN
35	$+V_{ISO}$
36	LIN
37	GAIN
38	FB

INSIDE THE 1B41

Referring to the functional block diagram, the ±15 V power inputs provide power to both the output side circuitry and the power oscillator. The 25 kHz power oscillator provides both the timing information for the signal demodulator and drives transformer T2 for the input side power supplies. The secondary winding of T2 is half wave rectified and filtered to create the input side power.



1B41 Functional Block Diagram

Dual current sources of 0.25 mA are derived from the floating power supply and accomplish 3-wire compensation as well. This creates a voltage difference between the RTD and R_Z. This voltage is applied to the chopper stabilized differential amplifier. Linearization can be implemented at this stage by a simple jumper option. This creates a bow in the current source that nulls out the nonlinearity of Pt 100 RTDs.

The signal input (HI) is single pole filtered for noise rejection and antialiasing. PROT HI is the output node of the filter, and is used only for special input applications as described in the applications section of this data sheet.

The chopper stabilized gain stage amplifies the differential input voltage with a gain set by external resistors.

The signal is amplitude modulated onto a 25 kHz carrier and passed through the signal transformer T1. The synchronous demodulator restores the signal to the baseband. A two-pole active low pass stage filters out clock noise and completes a three-pole Butterworth filter formed with the input pole.

USING THE 1B41

Range Setting: The gain of the 1B41 is controlled on the input side by a pair of user provided resistors (see Figure 1). A feedback resistor of 20 kΩ ±1% is required between the feedback pin (Pin 38) and the gain pin (Pin 37). The gain setting resistor is connected between the gain pin (Pin 37) and input side common (Pin 4).

In the equations below R_Z is the value of the RTD resistance at the temperature at which zero volts ouptut is desired, R_{HS} is the resistance of the RTD when the temperature is the average of the zero ouput temperature and the full-scale temperature, and R_{FS} is the resistance of the RTD at the full-scale temperature.

$$R_G = 20\ k\Omega/(G-1)$$

$$R_{LIN} = 6.1\ k\Omega(2Q-3)/(2-Q)$$

where $Q \equiv \Delta R_{FS}/\Delta R_{HS}$

$G \equiv (20\ k\Omega/\Delta R_{FS})(Q-1)$

$\Delta R_{FS} = R_{FS} - R_Z$

$\Delta R_{HS} = R_{HS} - R_Z$

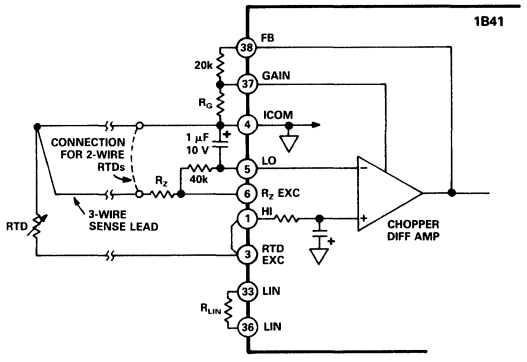


Figure 1. 1B41 Basic Hookup

Since gain and linearization are interactive, it is recommended that any offset and span errors be removed in software or at a later stage in the data acquisition circuitry.

The accuracy of the resistor values must be taken into account when calculating the initial gain accuracy of an application. The initial accuracy of the 1B41 must then be added to the resistor errors to predict the total accuracy. Likewise, the ratiometric temperature coefficient of the gain and feedback resistors must be added to the temperature coefficient of the 1B41 to predict the total resulting thermal drift.

3-Wire Compensation: The 1B41 accomplishes 3-wire compensation by using matched current sources on both RTD EXC (Pin 3) and R_Z EXC (Pin 6). Figure 2 shows lead wires with resistances of R_{L1}, R_{L2} and R_{L3}. The following equation describes the error voltage caused by lead resistance and the current source mismatch.

$$V_{ERROR} = I_1R_{L3} - I_2R_{L2}$$

This equation depends upon the matching of the wire resistance and the matching of the 1B41 current sources. When all leads have the same resistance and the current sources are matched, no error is introduced.

For 2-wire RTDs, ICOM (Pin 4) can be connected as shown in Figure 1. This does not compensate for lead wire resistance.

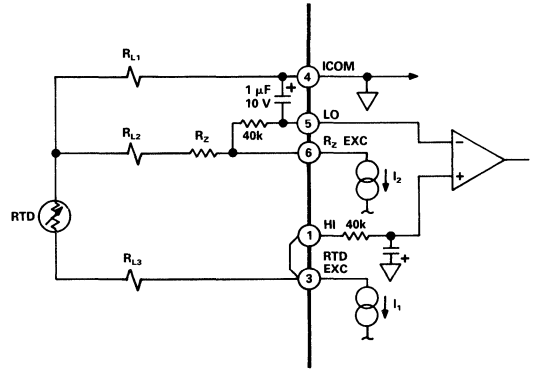


Figure 2. 3-Wire Compensation

Note that since the current sources are in fact *current sinks*, as the RTD resistance increases, the voltage at HI (Pin 1) gets more negative. This causes the output of the 1B41 to get more positive.

Example: A 100 Ω platinum RTD, α = 0.00385, is 100 Ω at 0°C, 138.50 Ω at 100°C, and 175.84 Ω at 200°C.

$$R_Z = 100\ \Omega,\ R_{HS} = 138.50\ \Omega,\ R_{FS} = 175.84\ \Omega$$

$$Q = \frac{175.84-100}{138.50-100} = 1.9699$$

$$R_{LIN} = \frac{6.1\ k\Omega(2\times 1.9699-3)}{(2-1.9699)} = 190.46\ k\Omega$$

$$R_G = \frac{20\ k\Omega}{255.78-1} = 78.5\ \Omega$$

PERFORMANCE

CMR and NMR: Common mode rejection is a result of both isolation and filtering, and is dependent on signal frequency, conditioner gain and source impedance imbalance.

The CMR performance is also enhanced by low pass filtering, giving an effective CMR of 160 dB at 60 Hz (f_C = 3 Hz) at the output of the filter.

Gain Nonlinearity: 1B41 gain nonlinearity is defined as the deviation of the output voltage from the best straight line and is specified as % peak-to-peak of a ±10 V output span.

APPLICATION EXAMPLES

Input Protection: Although the 1B41 provides ±1500 V of common mode protection, it is sometimes desirable to have some level of normal mode protection as well. The signal input of the 1B41 is normally less than 500 mV but could be very large under a fault condition.

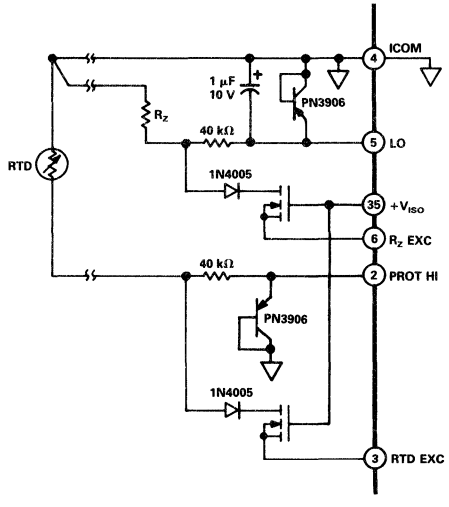


Figure 3. 120 V/240 V AC Normal Mode Input Protection

Referring to Figure 3, the inputs and current sources show 240 V rms protection. The PN3906 pnp transistors are used for the diode properties of the base emitter junction. When the emitter is more positive than the base, the transistor functions as a forward biased diode. When the emitter is negative with respect to the base, the junction is a very low leakage Zener diode with a breakdown voltage of about −8 V. This serves as a voltage clamp for LO and PROT HI. A fault voltage applied between ICOM and either of the two inputs will appear mostly across the 40 kΩ resistor. The power dissipated in the resistor is approximately 1.44W for a 240 V fault.

Each current source is protected by a MOSFET and a diode. The MOSFET is an n-channel enhancement mode device. The RTD EXC and R_Z EXC pins are normally about −3.5 V with respect to ICOM. The voltage at $+V_{ISO}$ is about +6.5 V, yielding a V_{GS} of about 10 V. For normal operation, the FET must be saturated on. A device with a threshold voltage of less than 5 V at 1 mA I_{DS} guarantees saturation.

The V_{DS} breakdown voltage must be greater than the expected fault voltage. At 240 V rms, the peak voltage is 339V, so the FET must have a breakdown voltage of at least 350 V. The power dissipation requirements are minimal, however. The power dissipated in the FET under fault mode is 240 V×0.25 mA×0.5 = 30 mW. The factor of 0.5 is due to the 50% duty cycle. This allows a compact TO-92 packaged device, such as the VN0650.

During the other half of the cycle, the fault voltage is applied across the series diode. The diode must have a reverse breakdown voltage of at least 350 V.

Other RTD Measurements. The 1B41 can be configured for making differential measurements using 2-wire RTDs. As shown in Figure 4, the two RTDs are connected between ICOM and HI and LO. The current sources at R_Z EXC and RTD EXC create a differential signal across HI and LO that is proportional to the difference in resistance of the two RTDs. The following equation shows how to calculate R_G for applications where hardware linearization is not desired.

$$R_G = \frac{40\ k\Omega}{G-2}$$

The LIN pins (Pins 33 and 36) must be left unconnected to maintain a constant current source.

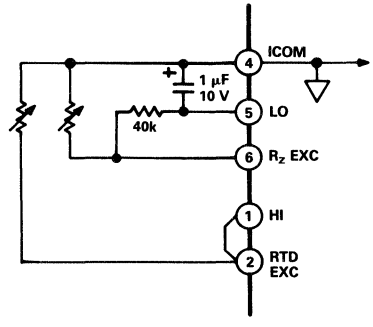


Figure 4. Differential RTD Measurement

Isolated mV/Thermocouple Signal Conditioner

1B51

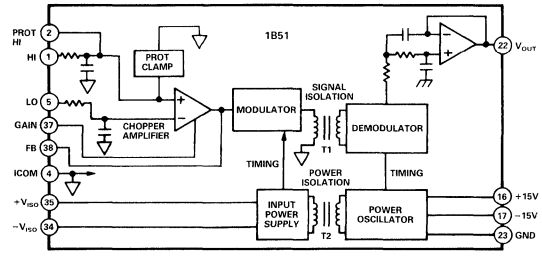
FEATURES

Functionally Complete Precision Conditioner
High Accuracy
Low Input Offset Tempco: ±0.1μV/°C
Low Nonlinearity: ±0.025%
High CMR: 160dB (60Hz, G=1000V/V)
High CMV Isolation: 1500V rms Continuous
240V rms Input Protection
Small Package: 1.0″×2.1″×0.35″ DIP
Isolated Power
Low Pass Filter (f_C=3Hz)
Pin Compatible with 1B41 Isolated RTD Conditioner

APPLICATIONS

Multichannel Thermocouple Temperature Measurement
Low Level Data Acquisition Systems
Industrial Measurement & Control Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 1B51 is a precision, mV/thermocouple signal conditioner that incorporates a circuit design utilizing transformer based isolation and automated surface mount manufacturing technology. It provides an unbeatable combination of versatility and performance in a compact plastic package. Designed for measurement and control applications, it is specially suited for harsh environments with extremely high common-mode interference. Unlike costlier solutions that require separate dc/dc converters, each 1B51 generates its own input side power, providing true, low cost channel-to-channel isolation.

Functionally, the signal conditioner consists of three basic sections: chopper stabilized amplifier, isolation and output filter. The chopper amplifier features a highly stable offset tempco of ±0.1μV/°C and resistor programmable gains from 2 to 1000. Wide range zero suppression can be implemented at this stage.

The isolation section has complete input to output galvanic isolation of 1500V rms continuous using transformer coupling techniques. Isolated power of 2mA at ±6.2V is provided for ancillary circuits such as zero suppression and open-input detection. Filtering at 3Hz is implemented by a passive antialiasing filter at the front end and a two-pole active filter at the output. Overall NMR is 60dB and CMR is 160dB min @ 60Hz, G = 1000.

The 1B51 is specified over −25°C to +85°C and operates over the industrial (−40°C to +85°C) temperature range.

DESIGN FEATURES AND USER BENEFITS

High Noise Rejection: The combination of a chopper stabilized front end with a low pass filter provides high system accuracy in harsh industrial environments as well as excellent rejection of 50/60Hz noise.

Input Protection: The input is internally protected against continuous application of 240V rms.

Low Cost: The 1B51 offers a very low cost per channel for high performance, isolated, low level signal conditioners.

Wide Range Zero Suppression: This input referred function is a convenient way to null large input offsets.

Low Pass Filter: The three pole active filter (f_C=3Hz) reduces 60Hz noise and aliasing errors.

Small Size: The 1B51 package size (1.0″×2.1″×0.35″) and functional completeness make it an excellent choice in systems with limited board space and clearance.

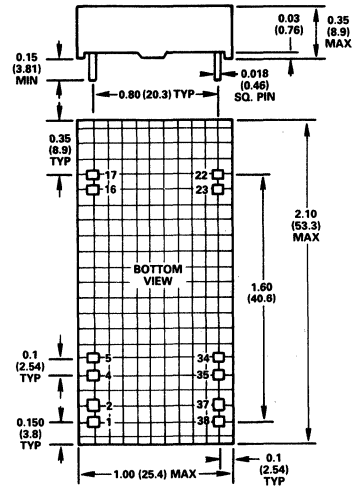
1B51—SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

Model	1B51AN	1B51BN
GAIN		
Gain Equation	$G=\left[1+\frac{R_{FB}}{R_G}\right] \times 2$	*
Gain Error	1% max	*
Gain Temperature Coefficient[1]	50ppm/°C	*
Gain Nonlinearity	±0.035% (±0.05% max)	±0.025% (±0.04% max)
OFFSET VOLTAGES		
Input Offset Voltage		
Initial, @ +25°C (Adjustable to Zero)	25μV (100μV max)	*
vs. Temperature	±0.1μV/°C (±0.5μV/°C max)	*
vs. Time, Noncumulative	±1μV/month max	*
Output Offset Voltage		
Initial	−50mV	−25mV
vs. Temperature	−175μV/°C	−50μV/°C
INPUT OFFSET CURRENT		
Initial	0.6nA (2.5nA max)	*
vs. Temperature	±2.5pA/°C (12.5pA/°C max)	*
INPUT BIAS CURRENT		
Initial @ +25°C	10nA	*
vs. Temperature	10pA/°C	*
INPUT IMPEDANCE		
Power On	50MΩ	*
Power Off	40kΩ min	*
INPUT VOLTAGE RANGE		
Linear Differential Input	±10mV to ±5V	*
Max CMV, Input to Output		
ac, 60Hz, Continuous	1500V rms	*
Continuous, dc	±2000V	*
CMR @ 60Hz, 1kΩ Source Imbalance, G = 1000	160dB min	*
NMR @ 60Hz	60dB min	*
Transient Protection	IEEE-STD 472 (SWC)	*
INPUT NOISE		
Voltage, 0.1Hz to 10Hz, 1kΩ Source Imbalance	1μV p-p	*
RATED OUTPUT		
Voltage, 2kΩ Load, min	±10V	*
Current	±5mA	*
Output Noise, dc to 100kHz	1mV p-p	*
Impedance, dc	0.1Ω	*
FREQUENCY RESPONSE		
Bandwidth, −3dB	dc to 3Hz	*
ISOLATED POWER		
Voltage, No Load	±6.2V±5%	*
Current	2mA	*
Regulation, No Load to Full Load	7.5%	*
Ripple	250mV p-p	*
POWER SUPPLY		
Voltage, Rated Performance	±15V dc	*
Voltage, Operating	±13.5V to ±18V	*
Current, Quiescent	+12mA @ +15V, −4mA @ −15V	*
PSRR	0.1%/V	*
ENVIRONMENTAL		
Temperature Range		
Rated Performance	−25°C to +85°C	*
Operating	−40°C to +85°C	*
Storage	−40°C to +85°C	*
Relative Humidity	0 to 95% @ +60°C	*
CASE SIZE	1.00″×2.10″×0.35″ (25.4×53.3×8.9)mm	*

NOTES
*Specifications same as 1B51AN.
[1]See graph in text.
Specifications subject to change without notice.

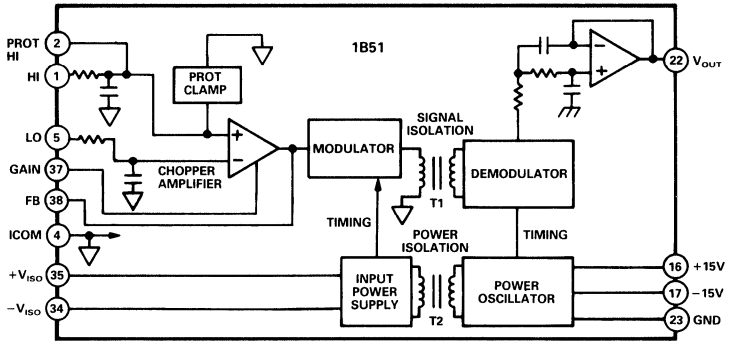
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	DESIGNATION
1	HI
2	PROT HI
4	ICOM
5	LO
16	+15V
17	−15V
22	V_O
23	GND
34	$-V_{ISO}$
35	$+V_{ISO}$
37	GAIN
38	FB



Functional Block Diagram

INSIDE THE 1B51

Referring to the functional block diagram, the ±15V power inputs provide power to both the output side circuitry and the power oscillator. The 25kHz power oscillator provides the timing information for the signal demodulator and drives power transformer T2 for the input side power supplies. The secondary winding of T2 is half wave rectified and filtered to create the input side bipolar unregulated supplies.

The signal input (HI) is single-pole filtered for noise rejection and antialiasing. The protection clamps limit the voltage at PROT HI to ±8V. Thus, a large voltage applied between HI and input common (I COM) appears mostly across the input resistor.

The chopper stabilized gain stage amplifies the differential input voltage with a gain set by external resistors. The voltage at the inverting input of the chopper stabilized amplifier (LO) should be equal to the input voltage at which the desired output voltage is zero. This is a true input referred zero suppression function.

The signal is amplitude modulated onto a 25kHz carrier and passed through the signal transformer T1. The synchronous demodulator restores the signal to the baseband. A two-pole active low pass stage filters out clock noise and completes a three-pole Butterworth filter formed with the input pole.

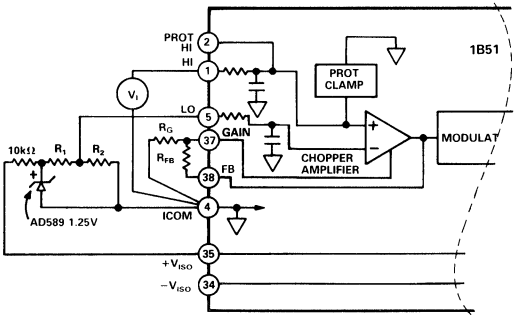


Figure 1. Input Gain Setting and Zero Supression

USING THE 1B51

Gain Setting:

The gain of the 1B51 is controlled on the input side by a pair of user provided resistors (see Figure 1). A feedback resistor of between 10kΩ and 20kΩ is required between the feedback pin (FB) and the gain pin. The gain setting resistor is connected between the gain pin and input side common (ICOM). The gain equation is

$$G = \left[1 + \frac{R_{FB}}{R_G}\right] \times 2$$

Gains of 2–1000 can be achieved by adjusting this ratio.

The accuracy of the resistor values must be taken into account when calculating the initial gain accuracy of an application. The initial accuracy of the 1B51 must then be added to the resistor errors to predict the total accuracy. Likewise, the ratiometric temperature coefficient of the gain and feedback resistors must be added to the temperature coefficient of the 1B51 to predict the total resulting thermal drift.

It is possible to use a trimming potentiometer to correct for initial gain and system gain errors. The feedback resistor can be comprised of a resistor in series with a trimming potentiometer, as long as the total resistance remains between 10kΩ and 20kΩ. Alternatively, the gain resistor can also be an adjustable resistor. In general, the greater the trim range, the coarser the resolution.

Zero Suppression:

Since the 1B51 is a differential input device, true input referred zero suppression can be accomplished (see Figure 1). A voltage reference powered by the input side power supplies is applied to the LO terminal. Since the transfer function is

$$V_O = (V(HI) - V(LO)) \times GAIN$$

the input voltage for which the desired output is zero should be applied to the LO pin. The equation is

$$V_Z = 1.25(R_2/(R_1 + R_2))$$

Any drift of this input zero suppression voltage appears as offset drift, so a temperature stable reference should be used. The source impedance at the LO terminal should be kept below 1kΩ.

Open Input Detection:
The 1B51 can sense an open thermocouple or broken input line with the addition of an external resistor. By connecting a 220MΩ resistor between the HI pin and the positive or negative isolated supply, an open input will cause a positive or negative full scale output, respectively.

To preserve the normal mode input protection capability of the 1B51, the resistor must be able to withstand 220Vac. A high voltage rating can be obtained by connecting lower value resistors in series.

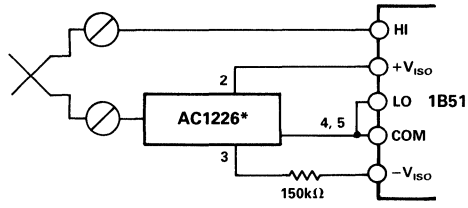
Cold Junction Compensation:
When using a thermocouple as an input to the 1B51, a second thermocouple junction is formed at the terminations of the thermocouple wires, commonly referred to as the cold junction. The measured output voltage of the sensor is the voltage generated by the thermocouple minus the voltage generated by the cold junction.

Since thermocouples are specified with 0V representing 0°C, it would be ideal to maintain the cold junction at 0°C. A more practical approach involves adding a temperature dependent voltage to the thermocouple signal so as to oppose the cold junction effects. This type of correction is known as cold junction compensation.

Many different methods are commonly used to implement cold junction compensation. Usually a thermistor or a semiconductor sensor is used to generate the cold junction voltage. The slope of the cold junction voltage must be the same as that of the thermocouple. Therefore, the cold junction compensation depends on the thermocouple type.

Sometimes, one cold junction compensation sensor is used by a number of thermocouple channels. This is accomplished by measuring the temperature of the connection block directly, and adding the appropriate voltage to each uncompensated thermocouple channel after the gain has been taken. *In all cases, the cold junction sensor must be in the thermal proximity with the connection block.*

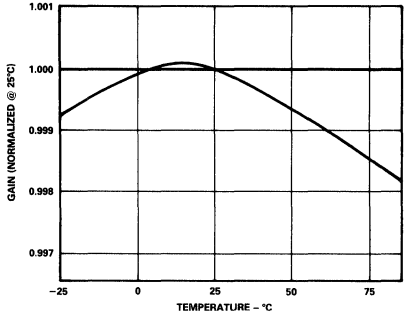
Figure 2 shows a monolithic cold junction compensation device used with the 1B51. The Analog Devices AC1226 measures the ambient temperature and generates the appropriate cold junction voltage for several different thermocouple types.



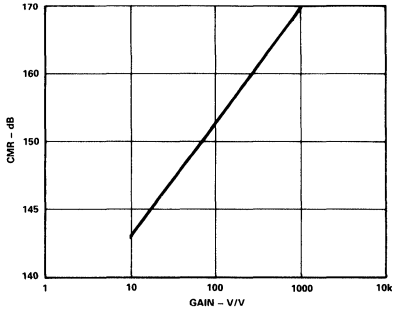
*PIN NUMBER DEPENDS ON THERMOCOUPLE TYPE.
SEE AC1226 DATA SHEET FOR DETAILS.

Figure 2. 1B51 Cold Junction Compensation

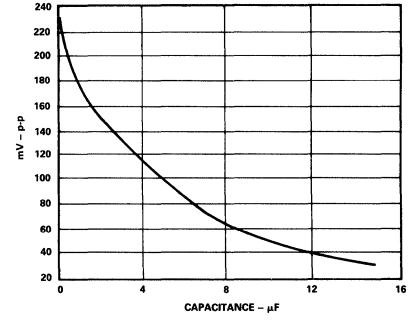
TYPICAL PERFORMANCE CURVES (@T_A = +25°C, V_S = ±15V)



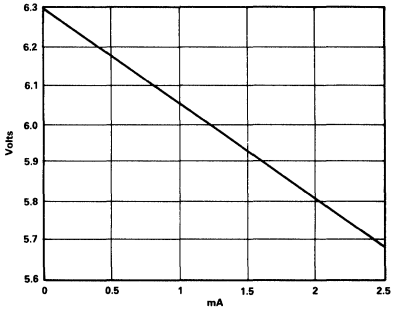
Gain vs. Temperature



CMR vs. Gain



$+V_{ISO}$ Ripple vs. Capacitance



$+V_{ISO}$ vs. Load

High Performance, 4–20mA Output Voltage-to-Current Converter

2B20

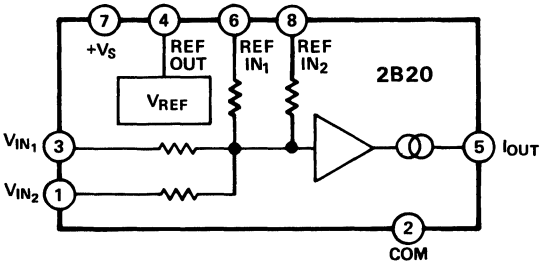
FEATURES

- Complete, No External Components Needed
- Small Size: 1.1″ x 1.1″ x 0.4″ Module
- Input: 0 to +10V; Output: 4 to 20mA
- Low Drift: 0.005%/°C max; Nonlinearity: 0.005% max (2B20B)
- Wide Temperature Range: -25°C to +85°C
- Single Supply: +10V to +32V
- Meets ISA Std 50.1 for Type 3, Class L and U, Nonisolated Current Loop Transmitters
- Economical

APPLICATIONS

- Industrial Instrumentation and Control Systems
- D/A Converter – Current Loop Interface
- Analog Transmitters and Controllers
- Remote Data Acquisition Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Model 2B20 is a complete, modular voltage-to-current converter providing the user with a convenient way to produce a current output signal which is proportional to the voltage input. The nominal input voltage range is 0 to +10V. The output current range is 4 to 20mA into a grounded load.

Featuring low drift (0.005%/°C max, 2B20B) over the -25°C to +85°C temperature range and single supply operation (+10V to +32V), model 2B20 is available in two accuracy grades. The 2B20B offers precision performance with nonlinearity error of 0.005% (max) and guaranteed low offset error of ±0.1% max and span error of ±0.2% max, without external trims. The 2B20A is an economical solution for applications with lesser accuracy requirements, featuring nonlinearity error of 0.025% (max), offset error of ±0.4% (max), span error of ±0.6% (max), and span stability of 0.01%/°C max.

The 2B20 is contained in a small (1.1″ x 1.1″ x 0.4″), rugged, epoxy encapsulated package. For maximum versatility, two signal input (V_{IN1} and V_{IN2}) and two reference input (REF_{IN1} and REF_{IN2}) terminals are provided. Utilizing terminals V_{IN1} and REF_{IN1} eliminates the need for any external components, since offset and span are internally calibrated. If higher accuracy (up to ±0.01%) is required, inputs V_{IN2} and REF_{IN2} with series trim potentiometers may be utilized.

APPLICATIONS

Model 2B20 has been designed for applications in process control and monitoring systems to transmit information between subsystems or separated system elements. The 2B20 can serve as a transmission link between such elements of process control system as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners.

In a typical application, model 2B20 may act as an interface between the D/A converter output of a microcomputer based system and a process control device such as a variable position valve. Another typical application of the 2B20 may be as a current output stage of a proportional controller to interface devices such as current-to-position converters and current-to-pneumatic transducers.

DESIGN FEATURES AND USER BENEFITS

Process Signal Compatibility: To provide output signal compatibility, the 2B20 meets the requirements of the Instrument Society of America Standard S50.1, "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 3, Class L and U, nonisolated current loop transmitters.

External Reference Use: For increased flexibility, when ratiometric operation is desired, the 2B20 offers a capability of connecting an external reference (i.e., from multiplying D/A converter) to the REF_{IN2} terminal.

Wide Power Supply Range: A wide power supply range (+10V to +32V dc) allows for operation with either a +12V battery, a +15V powered data acquisition system, or a +24V powered process control instrumentation.

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2B20—SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

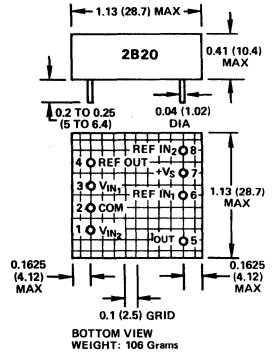
Model	2B20A	2B20B
INPUT SPECIFICATIONS		
Voltage Signal Range	0 to +10V	*
Input Impedance	10kΩ	*
OUTPUT SPECIFICATIONS		
Current Output Range[1]	4 to 20mA	*
Load Resistance Range[2]		
V_S = +12V	0 to 350Ω max	*
V_S = +15V	0 to 500Ω max	*
V_S = +24V	0 to 950Ω max	*
NONLINEARITY (% of Span)	±0.025% max	±0.005% max
ACCURACY[3]		
Warm-Up Time to Rated Specs	1 minute	*
Total Output Error @ +25°C[3,4]		
Offset (V_{IN} = 0 volts)	±0.4% max	±0.1% max
Span (V_{IN} = +10 volts)	±0.6% max	±0.2% max
vs. Temperature (-25°C to +85°C)		
Offset (V_{IN} = 0 volts)	±0.01%/°C max	±0.005%/°C max
Span (V_{IN} = +10 volts)	±0.01%/°C max	±0.005%/°C max
DYNAMIC RESPONSE		
Settling Time – to 0.1% of F.S. for 10V Step	25μs	*
Slew Rate	2.5mA/μs	*
REFERENCE INPUT[5]		
Voltage	+2.5V dc	*
Input Impedance	10kΩ	*
POWER SUPPLY		
Voltage, Rated Performance	+15V dc	*
Voltage, Operating	+10V to +32V dc max	*
Supply Change Effect (% of Span)[6]		
on Offset	±0.005%/V	*
on Span	±0.005%/V	*
Supply Current	6mA + I_{LOAD}	*
TEMPERATURE RANGE		
Rated Performance	-25°C to +85°C	*
Storage	-55°C to +125°C	*
CASE SIZE	1.125" X 1.125" X 0.4"	*

NOTES
*Specifications same as 2B20A.
[1] Current output sourced into a grounded load over a supply voltage range of +10V to +32V.
[2] See Figure 1 for the maximum load resistance value over the power supply range.
[3] Accuracy is guaranteed with no external trim adjustments when REF_{IN} is connected to REF_{OUT}.
[4] All accuracy is specified as % of output span where output span is 16mA (±0.1% = ±0.016mA output error).
[5] Reference input is normally connected to the reference output (+2.5V dc).
[6] Optional trim pots may be used for calibration at each supply voltage.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET: AC1016

LOAD RESISTANCE RANGE

The load resistance is the sum of the resistances of all connected receivers and the connection lines. The 2B20 operating load resistance is power supply dependent and will decrease by 50 ohms for each 1 volt reduction in the power supply. Similarly, it will increase by 50 ohms per volt increase in the power supply, but must not exceed the safe voltage capability of the unit.

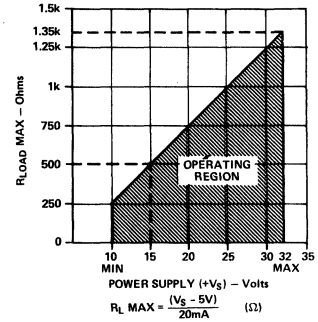


Figure 1. Maximum Load Resistance vs. Power Supply

PRINCIPLE OF OPERATION

The design of the 2B20 is comprised of high performance op amps, precision resistors and a high stability voltage reference to develop biasing and output drive capability. The 2B20 is designed to operate from a single positive power supply over a wide range of +10V to +32V dc and accepts a single ended, 0 to +10V voltage input. The internal reference has nominal output voltage of +2.5V (REF_{OUT}) and is used to develop 4mA output current for a zero volts input when REF_{IN} is connected to REF_{OUT}.

The output stage of the 2B20 utilizes a sensing resistor in the feedback loop, so the output current is linearly related to the voltage input and independent of the load resistance. There is no minimum resistance for the loads driven by the 2B20; it can drive even a short circuit with no damage to the unit. The maximum resistance of the load as seen by the unit (resistance of the load plus the resistance of the connecting wire) is limited. The maximum external loop resistance, R_L, is given by:

$$R_L\ (\Omega)\ max = \left(\frac{+V_S - 5V}{20mA}\right)$$

Figure 1 shows the operating region of the 2B20. The load must be returned to power supply common. The voltage appearing between I_{OUT} (pin 5) and COM (pin 2) should not exceed $V_{max} = +V_S - 5V$. Exceeding this value (up to +32V dc) will not damage the unit, but it will result in a loss of linearity.

The basic connections of the 2B20 are shown in Figure 2.

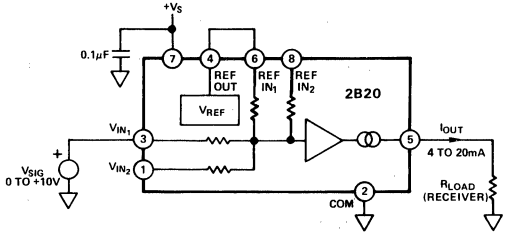


Figure 2. Basic Connections Diagram

OPTIONAL CALIBRATION AND TRIM PROCEDURE

Model 2B20's factory trimmed offset error is ±0.1% max and span error is ±0.2% max (2B20B). In most applications, further trimming will not be required. If it is necessary to obtain calibrated accuracy of up to ±0.01%, or, if a high signal source resistance (with respect to 10kΩ) introduces calibration error, inputs V_{IN2} and REF_{IN2} and optional trim pots should be used with V_{IN1} and REF_{IN1} open. To perform external trims, connect 500Ω potentiometers in series with V_{IN2} (span trim) and REF_{IN2} (offset trim) as shown in Figure 3. Adjust span pot, monitoring voltage drop across R_{LOAD}, to obtain an output voltage of 5.000V (I_{OUT}=20mA) for a +10V input. Next, with 0 volts input, adjust offset pot to obtain 1.000V output (I_{OUT}=4mA). Check both offset and span and retrim if necessary after each adjustment.

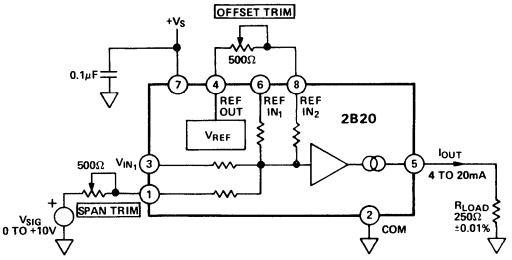


Figure 3. Model 2B20 Connections Using Optional Offset and Span Trims

CONNECTING THE 2B20 FOR 0 TO 10mA OUTPUT

The 2B20 may be utilized in applications requiring 0 to 10mA current output for a 0 to +10V input voltage range as shown in Figure 4a. To obtain 0mA output for 0V input, adjust the offset potentiometer until there is no current flowing in the output. The 2B20 span calibration may be adjusted by a 2kΩ gain potentiometer in series with the V_{SIG} input.

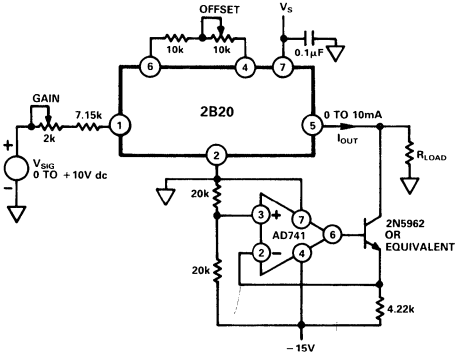


Figure 4a. 2B20 Configuration for 0 to 10mA Operation

CONNECTING THE 2B20 FOR 0 TO 20mA OUTPUT

The 2B20 may also be configured for use in applications requiring 0 to 20mA output for a 0 to +10V input range as shown in Figure 4b. To obtain 0mA output for 0V input, adjust the offset potentiometer. The 2B20 span calibration may be adjusted by a 2kΩ gain potentiometer in series with the V_{SIG} input.

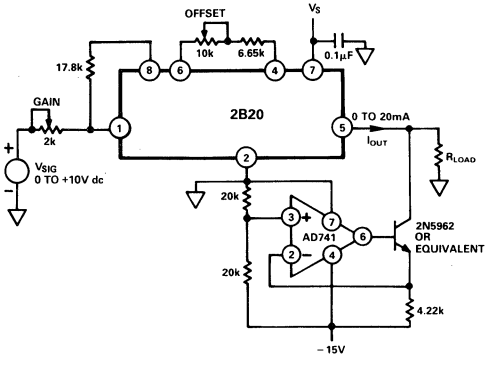


Figure 4b. 2B20 Configuration for 0 to 20mA Operation

OUTPUT PROTECTION

In many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages. The circuit shown in Figure 5 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

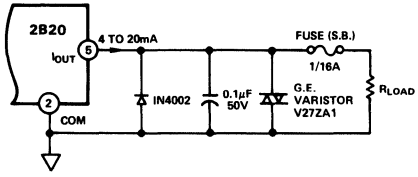


Figure 5. Output Protection Circuitry Connections

APPLICATIONS

Interfacing Voltage Output D/A Converters: The 2B20 is well suited in applications requiring 4 to 20mA output from D/A converters. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 6. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B20 (or the AD DAC80). First, a digital input code of all ones is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all 0s is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA –1LSB = 19.9961mA.

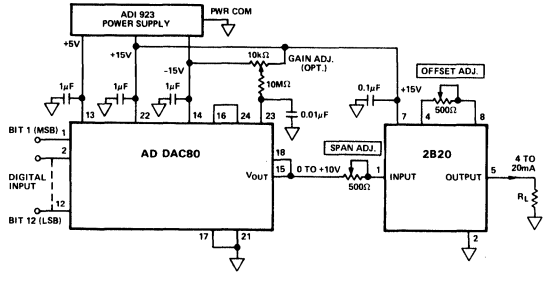


Figure 6. AD DAC80 – 4 to 20mA Current Loop Interface

Interfacing Current Output D/A Converters: To interface current output D/A converters, such as the AD562, a circuit configuration illustrated in Figure 7 should be used. Since the AD562 is designed to operate with an external +10V reference, the same external reference may be utilized by the 2B20 for ratiometric operation. The output of the AD562 is used to drive the summing junction of an operational amplifier to produce an output voltage. Using the internal feedback resistor of the AD562 provides a 0 to +10V output voltage range suitable to drive the 2B20.

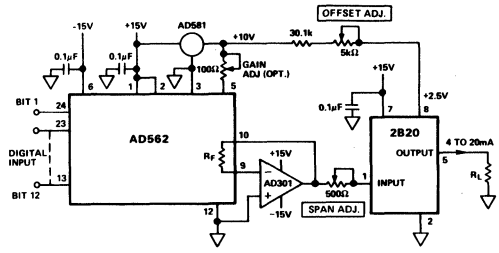


Figure 7. 12-Bit – 4 to 20mA Current Loop Interface

Microcomputer – Current Loop Interface: Figure 8 shows a typical application of the 2B20 in a multichannel microcomputer analog output system. When a microcomputer is to control a final control element, such as a valve positioner, servomechanism or motor, an analog output board with 4 to 20mA outputs is often necessary. The output boards typically have from one to eight channels, each with its own D/A converter. The 2B20, in a compact package, allows for an easy installation without any additional components and offers a 12-bit system compatible performance.

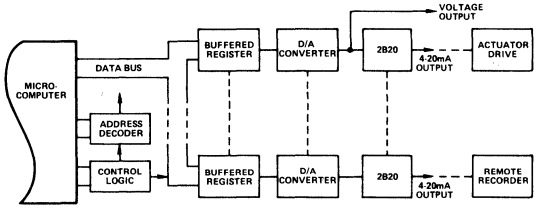


Figure 8. Microcomputer Analog Output Subsystem

Pressure Control System: In Figure 9, model 2B20 is used in a proportional pressure control system. The 3-15psi working pressure of a system is monitored with a pressure transducer interfaced by the model 2B31 signal conditioner. The high level voltage output of the 2B31 is converted to a 4 to 20mA to provide signal to the limit alarm and proportional control circuitry. A current-to-position converter controlling a motorized valve completes the pressure-control loop.

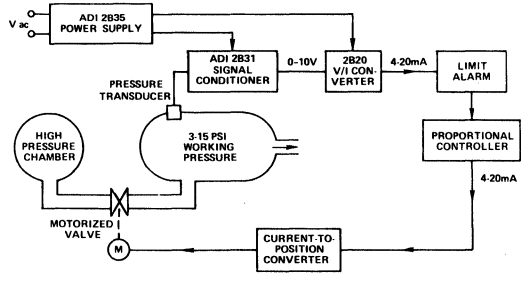


Figure 9. Proportional Pressure Control System

Isolated 4 to 20mA Output: For applications requiring up to ±1500V dc input to output isolation, consider using Analog Devices' model 2B22 isolated voltage-to-current converter.

ANALOG DEVICES

High Performance, Isolated Voltage-to-Current Converter

2B22

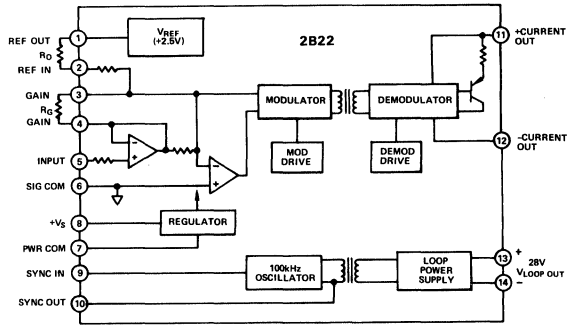
FEATURES

Wide Input Range: 0 to +1V to 0 to +10V
Standard Output Range: 4 to 20mA
High CMV Input/Output Isolation: 1500V dc Continuous
Low Nonlinearity: 0.05% max, 2B22L
Low Span Drift: 0.005%/°C max, 2B22L
Single Supply: +14V to +32V
Meets IEEE Std 472: Transient Protection (SWC)
Meets ISA Std 50.1: Isolated Current Loop Transmitters

APPLICATIONS

Industrial Instrumentation and Process Control
Ground Loop Elimination
High Voltage Transient Protection
D/A Converter – Current Loop Interface
Analog Transmitters and Controllers
Remote Data Acquisition Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Model 2B22 is a high performance, compact voltage-to-current converter offering 1500V dc input to output isolation in interfacing standard process signals. The input stage of the model 2B22 is single resistor programmable to accept voltage ranges from 0 to +1V to 0 to +10V. The isolated output current range is 4 to 20mA, and the 2B22 can be operated with 0 to 1000Ω grounded or floating loads.

Using modulation techniques with transformer isolation for reliable performance, the 2B22 is available in three accuracy selections offering guaranteed nonlinearity error (2B22L: ±0.05% max, 2B22K: ±0.1% max, and 2B22J: ±0.2% max) and guaranteed low span drift: ±0.005%/°C max, ±0.01%/°C max, and ±0.015%/°C max, respectively. The internally trimmed span and offset errors are ±0.1% max for the 2B22L and ±0.25% max for the 2B22J/2B22K. Both span and offset are adjustable by the optional external potentiometers.

Featuring a wide range, single supply operation (+14V to +32V), the 2B22 provides isolated +28V loop power and is capable of delivering rated current into an external 0 to 1000Ω load resistance. The unique output stage configuration also allows the user to utilize an optional external loop power supply to interface systems designed for a two-wire operation.

APPLICATIONS

Model 2B22 has been specifically designed for high accuracy applications in process control and monitoring systems to offer complete galvanic isolation and protection against damage from transients and fault voltages in transmitting information between subsystems or separated system elements. The 2B22 meets the requirements of the Instrument Society of America Std. 50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments" for Type 4, Class U isolated current loop transmitters.

In the industrial environment, model 2B22 can serve as a transmission link between such system elements as transmitters, indicators, controllers, recorders, computers, actuators and signal conditioners. In data acquisition and control systems, the 2B22 may act as an isolated interface between the D/A converter output of a microcomputer and standard 4 to 20mA analog loops.

10

DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 2B22 is a conservatively designed, compact module capable of reliable operation in harsh environments. To assure high reliability, the 2B22 has a calculated MTBF of over 270,000 hours and has been designed to meet the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

Process Signal Compatibility: The versatile input stage design with a single resistor gain adjustment enables the 2B22 to accept any one of the standard inputs—0-1V, 0-10V, 1-5V; or 1-5mA, 4-20mA, 10-50mA; and provide standard, isolated 4-20mA output.

Isolated Loop Power: Internal 28V dc loop supply, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to drive 0 to 1000Ω loads and eliminates the need for an external dc/dc converter.

2B22—SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

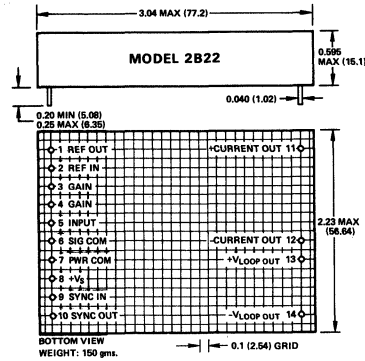
Model	2B22J	2B22K	2B22L
INPUT SPECIFICATIONS			
Voltage Signal Range, G = 1.6mA/V	0 to +10V	*	*
G = 16mA/V	0 to +1V	*	*
Gain Range	1.6 to 16mA/V	*	*
Maximum Safe Input	+15V	*	*
Input Impedance	10MΩ	*	*
OUTPUT SPECIFICATIONS			
Current Output Range	4 to 20mA	*	*
Load Resistance Range, V_S = +14V to +32V,			
Internal Loop Power	0 to 1000Ω max	*	*
Maximum Output Current,			
@ Input Overload	25mA	*	*
Output Ripple, 100Hz Bandwidth			
G = 1.6mA/V	60μA pk-pk	*	*
NONLINEARITY (% of Span)	±0.2% max	±0.1% max	±0.05% max
CMV, INPUT TO OUTPUT			
ac, 60Hz, 1 Minute Duration	1500V rms	*	*
Continuous, ac or dc	±1500V pk max	*	*
CMR, INPUT TO OUTPUT			
60Hz, 1kΩ Source Imbalance	90dB	*	*
ACCURACY[1]			
Warm Up Time to Rated Performance 5 Minutes			
Total Output Error @ +25°C[1,2]			
Offset (V_{IN} = 0V)	±0.25% max	±0.25% max	±0.1% max
Span (V_{IN} = +10V)	±0.25% max	±0.25% max	±0.1% max
vs. Temperature (0 to +70°C, G = 1.6mA/V)			
Offset (V_{IN} = 0V)	±0.01%/°C max	±0.005%/°C max	±0.0025%/°C max
Span (V_{IN} = +10V)	±0.015%/°C max	±0.01%/°C max	±0.005%/°C max
vs. Temperature (0 to +70°C)			
Offset (V_{IN} = 0V, G = 1.6mA/V to 16mA/V)	±0.01%/°C	±0.005%/°C	±0.0025%/°C
Span (G = 1.6mA/V to 16mA/V)[3]	±0.015%/°C	±0.01%/°C	±0.005%/°C
DYNAMIC RESPONSE			
Settling Time — to 0.1% of F.S. for 10V Step	300μs	*	*
Slew Rate	0.06mA/μs	*	*
REFERENCE INPUT			
Voltage	+2.5V dc	*	*
Input Impedance	6kΩ	*	*
OSCILLATOR			
Frequency, Internal Oscillator	100kHz ± 10%	*	*
External Sync Input			
Frequency	100kHz ± 10% max	*	*
Waveform	Square wave, 50% duty cycle	*	*
Voltage	20V p-p	*	*
POWER SUPPLY			
Voltage, Rated Performance	+15V dc	*	*
Voltage, Operating	+14V to +32V dc	*	*
Supply Current (at Full Scale Output)			
Using Internal Loop Power	100mA	*	*
Using External Loop Power	50mA	*	*
Supply Change Effect (% of Span)			
on Offset (V_{IN} = 0V)	±0.0005%/V	*	*
on Span (V_{IN} = +10V)	±0.0005%/V	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	−25°C to +75°C	*	*
Storage	−55°C to +85°C	*	*
CASE SIZE	2.2" X 3" X 0.6"	*	*

NOTES
[1] Accuracy is guaranteed at G = 1.6mA/V with no external trim adjustments when connected as shown in Figure 1.
[2] All accuracy is % of span where span is 16mA (±0.1% = ±0.016mA error).
[3] Span T.C. for gains higher than 1.6mA/V is R_G dependent — a low T.C. (±10ppm/°C) R_G is recommended for best performance.
*Specifications same as 2B22J.

Specifications subject to change without notice.

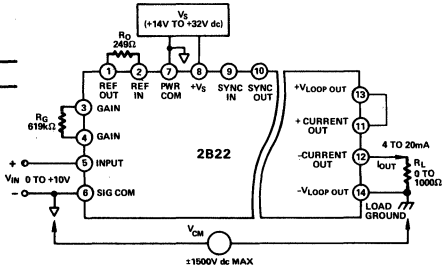
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



INTERCONNECTION DIAGRAM

Model 2B22 can be applied directly to achieve rated performance as shown in Figure 1 below. The input stage gain of 1.6mA/V, to convert a 0 to +10V signal into a 4 to 20mA output current, is obtained with the values shown. A single polarity power supply (+14V to +32V dc) should be connected to pin 8. To eliminate ground loops, the user should ensure that the signal return (common) lead does not carry the power supply current. Power common (pin 7) and signal common (pin 6) should be tied at the power supply common terminal. The voltage difference between pins 6 and 7 should not exceed 0.2V. An internal dc-dc converter provides isolated output loop power (pins 13 and 14), which is connected externally to the current output terminals (pins 11 and 12) and a load resistance. The standard 4 to 20mA current output signal is delivered into any external load between zero and 1000Ω.



NOTE: Resistors R_O and R_G are 1%, 50ppm/°C Metal Film Type. Values shown are for G = 1.6mA/V. For G = 16mA/V, use 10ppm/°C R_G and 50ppm/°C R_O.

Figure 1. Basic Connections

FUNCTIONAL DESCRIPTION

The high performance of model 2B22 is derived from the carrier isolation technique which is used to transfer both signal and power between the V/I converter's input circuitry and the output stage. High CMV isolation is achieved by the transformer coupling between the input amplifier, modulator section and the current output circuitry. The block diagram for model 2B22 is shown in Figure 2 below.

The 2B22 produces an isolated 4 to 20mA output current which is proportional to the voltage input and independent of the load resistance. The input amplifier operates single-ended and accepts a positive voltage within 0 to +10V range. Gain can be set from 1.6mA/V to 16mA/V by changing the gain resistor R_G to accommodate input ranges from 0 to +1V (G = 16mA/V) to 0 to +10V (G = 1.6mA/V). The transfer function is $I_{OUT} = (4mA + G \times V_{IN})$.

An internal, high stability reference has nominal output voltage of +2.5V (REF OUT) and is used to develop a 4mA output current for a 0 volts input. The terminals REF OUT (pin 1) and REF IN (pin 2) should be connected via the offset setting resistor R_O. For ratiometric operation, an external reference voltage can be connected to the REF IN terminal.

The 2B22 is designed to operate from a single positive power supply over a wide range of +14V to +32V dc. An internal dc-dc converter provides isolated +28V loop power which is independent of $+V_S$. The maximum resistance of the load R_L (resistance of the receivers plus the resistance of the connecting wire) is 1000Ω. Since the loop power is derived from the input side, the current capability of the power supply ($+V_S$) must be 100mA min to supply full output signal current.

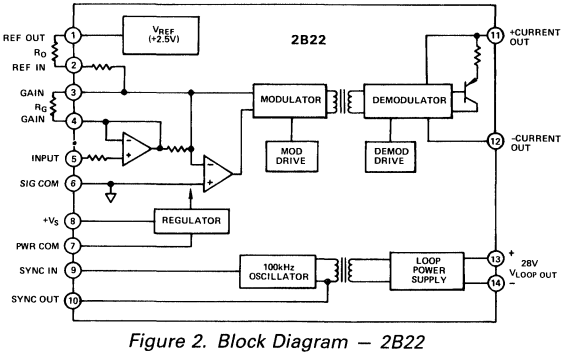


Figure 2. Block Diagram — 2B22

OPTIONAL TRIM ADJUSTMENTS

Model 2B22 is factory calibrated for a 0 to +10V input range (G = 1.6mA/V). As shipped, the 2B22 meets its listed specifications without use of any external trim potentiometers. Additional trim adjustment capability, to reduce span and offset errors to ±0.05% max, is easily provided as shown in Figure 3. The span and offset trim pots are adjusted while monitoring the voltage drop across a precision (or known) load resistor. The following trim procedure is recommended:

1. Connect model 2B22 as shown in Figure 3.
2. Apply V_{IN} = 0 volts and adjust R_O (Offset Adjust) for V_{OUT} = +2V ±4mV.
3. Apply V_{IN} = +10.00V and adjust R_G (Span Adjust) for V_{OUT} = +10V ±4mV.

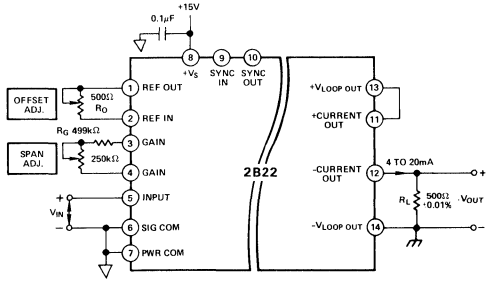


Figure 3. Optional Span and Offset Adjustment

GAIN AND OFFSET SETTING

The gain of the 2B22 is a scale factor setting that establishes the nominal conversion relationship to accommodate +1V to +10V full scale inputs (V_{IN}). The value of the gain setting resistor R_G is determined by: $R_G(k\Omega) = 6.314SF/(10.1 - SF)$ where SF is a scale factor equal to the value of V_{IN} F.S. Example: to convert a 0 to +1V input to the 4 to 20mA output, SF = 1 and R_G = 693Ω. Due to device tolerances, allowance should be made to vary R_G by ±5% using the potentiometer.

The value of the offset resistor R_O is independent from the gain setting and given by the relationship: $R_O(k\Omega) = 2.5(V_{REF} - 2.4)$ where V_{REF} is the reference voltage applied. For example, the reference provided by the 2B22 is +2.5V and therefore R_O = 250Ω. The accuracy of the R_O calculation from from the above formula is ±5%. When an external reference operation is desired (i.e. for ratiometric operation), connect the reference voltage via R_O to pin 2 and leave pin 1 open.

EXTERNAL LOOP POWER OPERATION

For maximum versatility, the 2B22's output stage is designed to operate from the optional, isolated external loop power supply. This feature allows the user to interface systems wired for a two-wire operation. As shown in Figure 4, the same wiring is used for loop power and output. The load resistance is connected in series with an external dc power supply (+6V to +32V), and the current drawn from the supply is the 4 to 20mA output signal. The input stage of the 2B22 still requires $+V_S$ power, but the current drain from $+V_S$ is limited to 50mA. Use of an external loop power may require gain and offset trimming to obtain specified accuracy. The maximum series load resistance depends on the loop supply voltage as shown in Figure 4.

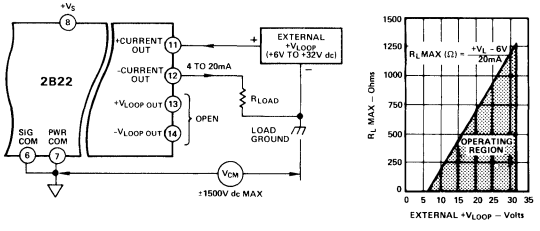


Figure 4. Optional External Loop Power Operation

SYNCHRONIZING MULTIPLE 2B22'S

In applications where multiple 2B22's are used in close proximity, radiated individual oscillator frequencies may cause "beat frequency" related output errors. These errors can be eliminated by synchronizing multiple units by connecting the SYNC OUT (pin 10) terminal to the SYNC IN (pin 9) terminal of the adjacent 2B22. The SYNC OUT terminal of this "slaved" unit can be used to drive another adjacent 2B22 (Figure 5). For best accuracy, each 2B22 should be retrimmed when synchronizing connections are used.

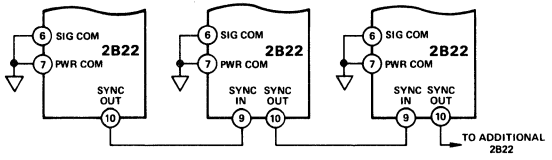


Figure 5. Multiple 2B22's Synchronization

OUTPUT PROTECTION

The current output terminals (pins 11 and 12) are protected from shorts up to +32V dc but in many industrial applications, it may be necessary to protect the 4 to 20mA output from accidental shorts to ac line voltages in addition to back EMF induced from long output connections. The circuit shown in Figure 6 can be used for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

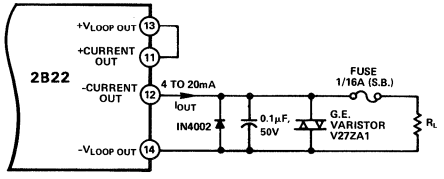


Figure 6. Output Protection Circuitry Connections

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Process Signal Isolator: In process control applications, model 2B22 can be applied to interface standard process signals (e.g. 1 to 5mA, 4 to 20mA, 10 to 50mA, 1 to 5V) and convert them to isolated 4 to 20mA output. A typical hook-up of model 2B22 is illustrated in Figure 7, showing input resistor R_C converting the current from a remote loop to a voltage input, and a span adjustment resistor R_G. A value of R_C should be selected to develop a minimum of +1V signal with full scale input current applied. For example, a 50Ω resistor converts the 4 to 20mA current input to a 200mV to 1V voltage input, which the 2B22 isolates and converts to a 4 to 20mA output. The reference input (pin 2) is not connected since the process signal provides a desired offset.

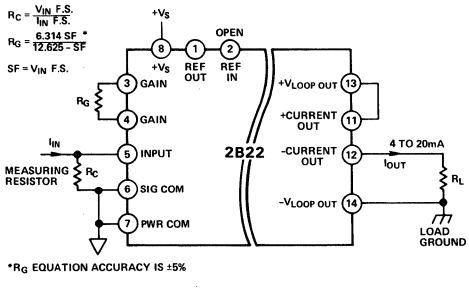


Figure 7. Process Signal Current Isolator

Isolated D/A Converter: Model 2B22 offers total ground isolation and protection from high voltage transients in interfacing D/A converters to standard 4 to 20mA current loops. This requirement is common in a microcomputer-based control system. The voltage necessary to power the current loop can be derived from the same +15V supply that is used to power the D/A converter. The D/A converter, such as the 12-bit AD DAC80, should be connected for operation on the unipolar 0 to +10V output range. This is shown in Figure 8. After the load resistor connection has been made, the current loop can be calibrated using the offset and span adjustment potentiometers associated with the 2B22. First, a digital input code of all one's is loaded into the D/A, and the offset adjustment potentiometer is adjusted for a current output of exactly 4mA. Then, a digital code of all zero's is loaded into the D/A, and the span adjustment potentiometer is adjusted for a voltage across the load that corresponds to a current of 20mA less 1LSB (19.9961mA).

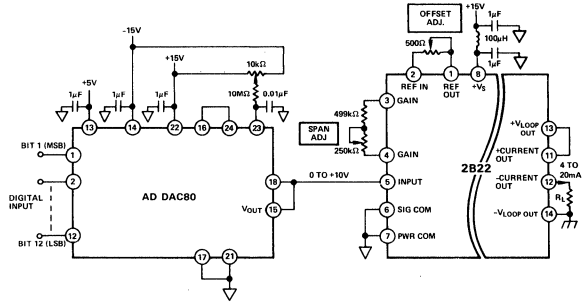


Figure 8. D/A Converter – Isolated 4 to 20mA Interface

Pressure Transmitter: In Figure 9, model 2B22 is used in a pressure transmitter application to provide complete input-output isolation and avoid signal errors due to ground loop currents. The process pressure is monitored with a strain gage type pressure transducer interfaced by the Analog Devices' model 2B30 transducer conditioner. The bridge excitation and system power is provided by the model 2B35 triple output power supply. The high level voltage output of the 2B30 is converted to the isolated 4 to 20mA current for transmission to a remote recorder or indicator.

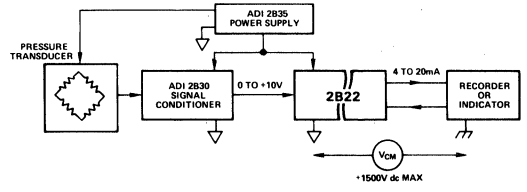


Figure 9. Isolated Pressure Transmitter

Programmable Output, Isolated Voltage-to-Current Converter

2B23

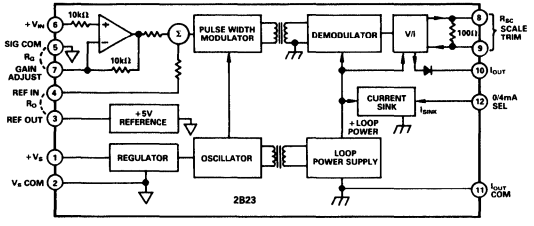
FEATURES

- **Wide Input Range, Resistor Programmable**
- **Pin Programmable Output: 4 to 20mA or 0 to 20mA**
- **High CMV Input/Output Isolation: ±1500V pk Continuous**
- **Low Nonlinearity: ±0.05% max (2B23K)**
- **Low Span Drift: ±0.005%/°C max (2B23K)**
- **Single Supply Operation: +14V to +28V**
- **Small Size: 1.8″ × 2.4″ × 0.6″**
- **Meets IEEE Std. 472: Transient Protection (SWC)**
- **Meets ISA Std. 50.1: Isolated Current Loop Transmitters**

APPLICATIONS

- **Industrial Instrumentation and Process Control**
  - **Ground Loop Elimination**
  - **Transient Voltage Protection**
- **Analog Transmitters and Controllers**
- **Remote Data Acquisition Systems**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The model 2B23 is a high performance, low cost voltage to current converter featuring ±1500V pk input to output isolation for interfacing with standard process signals. The input stage of the 2B23 may be single resistor programmed to accept voltages within a 0 to +10V range (+0.1V to +10V full scale). The isolated output is pin programmable to provide current in the range of 4 to 20mA or 0 to 20mA and can be operated with 0 to 800Ω grounded or floating loads.

The 2B23 uses reliable transformer isolation techniques and is available in two accuracy selections offering guaranteed nonlinearity error (2B23K: ±0.05% max, 2B23J: ±0.1% max) and guaranteed low span drift (2B23K: ±0.005%/°C max, 2B23J: ±0.01%/°C max). The internally trimmed span and offset errors are ±0.1% for the 2B23K and ±0.25% for the 2B23J. Both span and offset may be adjusted using optional external potentiometers.

Featuring wide range, single supply operation (+14V to +28V dc), the 2B23 provides isolated loop power, thus eliminating the need for an external dc/dc converter.

APPLICATIONS

Model 2B23 has been designed to provide high accuracy, versatility and low cost in industrial and laboratory system applications requiring isolated current transmission. The 2B23 meets the requirements of the Instrument Society of America Std. 50.1 "Compatibility of Analog Signals for Electronic Industrial Process Instruments" and may serve as a transmission link between such system elements as computers, controllers, actuators, recorders and indicators.

In data acquisition and control systems, the 2B23 may act as an isolated interface between the D/A converter output of a microcomputer analog I/O and standard 4 to 20mA or 0 to 20mA analog loops. In process control systems, the 2B23 may be used as a current output stage of a proportional controller to interface devices such as current-to-position converters and current-to-pneumatic transducers.

DESIGN FEATURES AND USER BENEFITS

High CMV Isolation: The 2B23 features high input to output galvanic isolation to eliminate ground loops and offer protection against damage from transients and fault voltages. Its isolation barrier will withstand continuous CMV of ±1500V pk and 1500V rms @ 60Hz for 60 seconds.

High Reliability: To assure high reliability in harsh industrial environments, reliable magnetic isolation is used. The 2B23 meets the IEEE Standard for Transient Voltage Protection (472–1974: Surge Withstand Capability) and offers reliable operation over −25°C to +85°C temperature range.

Versatility: The 2B23 can be easily tailored to the user's application, accommodating a wide range of input voltages, providing pin programmable, standard current outputs and offering wide range, single supply operation.

Small Size: To conserve board space, the 2B23 is packaged in a compact, 1.8″ × 2.4″ × 0.6″ module.

2B23—SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

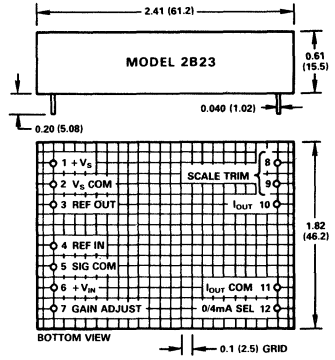
Model	2B23J	2B23K
INPUT SPECIFICATIONS		
Input Voltage Range		
Factory Calibrated	0 to +10V	*
Full Scale Input	+0.1V min to +10V max	*
Transfer Function (TF)		
Factory Calibrated	1.6mA/V	*
User Programmable	1.6mA/V to 200mA/V	*
Maximum Safe Input	±15V	*
Input Impedance	10MΩ	*
OUTPUT SPECIFICATIONS		
Current Output Range		
User Selectable	4 to 20mA, 0 to 20mA	*
Load Resistance Range		
Internal Loop Power	0 to 800Ω max	*
Maximum Output Current		
@ Input Overload	22mA typ	*
Output Noise		
100Hz Bandwidth	1.5μA pk-pk	*
NONLINEARITY	±0.1% max	±0.05% max (±0.02% typ)
ISOLATION		
CMV, Input to Output		
ac, 60Hz, 1 min	1500V rms	*
Continuous, ac or dc	±1500V pk	*
Transient Protection	IEEE Std. 472 (SWC)	*
CMR		
@ 60Hz, 1kΩ Source Imbalance	86dB	*
ACCURACY[1]		
Warm Up Time to Rated Performance	5 Minutes	*
Total Output Error @ +25°C[2,3]		
Offset (V_{IN} = 0V)	±0.25% max	±0.1% max
Span (V_{IN} = +10V)	±0.25% max	±0.1% max
vs. Temperature (0 to +70°C)		
Offset, 4-20mA Mode	±0.01%/°C max	±0.005%/°C max
0-20mA Mode	±0.01%/°C typ	±0.005%/°C typ
Span, Both Modes	±0.01%/°C max	±0.005%/°C max
DYNAMIC RESPONSE		
Settling Time to 0.1% of FS for 10V Step	5ms	*
Small Signal Bandwidth	400Hz	*
POWER SUPPLY		
Voltage, Rated Performance (+V_S)	+15V dc	*
Voltage, Operating	+14V min to +28V max	*
Supply Current (@ 20mA Output)	75mA	*
Supply Change Effect		
on Offset and Span	±0.0015%/V	*
ENVIRONMENTAL		
Temperature Range		
Rated Performance	0 to +70°C	*
Operating	−25°C to +85°C	*
Relative Humidity		
per MIL-STD 202, Method 103B	±0.2% Error	*
RFI Immunity		
27MHz @ 5W @ 3ft	±0.1% Error	*
CASE SIZE	1.8" × 2.4" × 0.6"	*

NOTES
[1]Accuracy is guaranteed @ TF = 1.6mA/V with no external trim adjustments when connected in the basic configuration.
[2]All accuracy is % of span where span is 16mA (i.e., ±0.1% = 0.016mA error).
[3]Span T.C. for transfer functions higher than 1.6mA/V is R_G dependent – low T.C. (±10ppm/°C)
R_G recommended for best performance.

*Specifications same as 2B23J.
Specifications subject to change without notice.

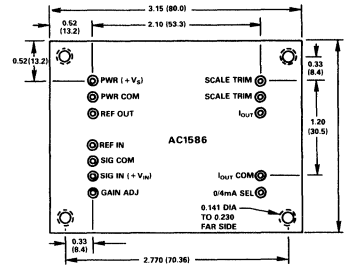
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



MATING SOCKET: AC1586

Dimensions shown in inches and (mm).



FUNCTIONAL DESCRIPTION

The high performance of model 2B23 is derived from the carrier isolation technique which is used to transfer both signal and power between the V/I converter's input circuitry and the output stage. High CMV isolation is achieved by the transformer coupling between the input amplifier stage, modulator, and current output circuitry. A block diagram of the 2B23 is shown in Figure 1.

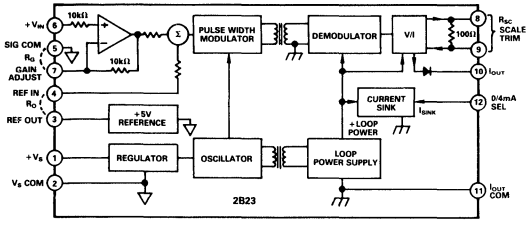


Figure 1. 2B23 Functional Block Diagram

The model 2B23 produces an isolated 4 to 20mA or 0 to 20mA output current which is proportional to the input voltage and independent of the output load resistance. The input amplifier accepts a positive voltage within the range of 0 to +10V. The transfer function of the input stage may be set from 1.6mA/V to 200mA/V (dependent upon the output current range desired) by changing the gain resistor R_G connected between pins 5 and 7.

An internal, high stability reference having a nominal output voltage of +5V (REF OUT) is used to develop a 4mA output current for a 0 volts input. REF OUT (Pin 3) and REF IN (Pin 4) should be connected via the offset scaling resistor R_O. An output current bypass section allows scaling of the nominal 4 to 20mA output current to a range of 0 to 20mA. This is accomplished by connecting the output range select pin (Pin 12) to the I_{OUT} pin (Pin 10) thereby providing a bypass for the 4mA. For 4-20mA operation, the bypass pin is connected to I_{OUT} COMMON (Pin 11).

The 2B23 is designed to operate from a single positive power supply ($+V_S$) over a range of +14V to +28V dc. The power supply section consists of an input voltage regulator, a dc/dc converter, plus associated rectifying and filtering circuitry. The dc/dc converter generates isolated loop power which is independent of V_S and capable of driving the maximum load resistance (resistance of receivers plus the resistance of connecting wire) of 800Ω. The current capability of the power supply ($+V_S$) must be 75mA minimum to supply full output signal current.

BASIC INTERCONNECTIONS

The 2B23 may be applied to achieve rated performance as shown in Figure 2. The transfer function of 1.6mA/V, for conversion of the 0 to +10V input signal into a 4 to 20mA output current, is obtained using the values shown (R_O = 10kΩ, R_{SC} = 301Ω, R_G open). For best performance, R_{SC} should be a metal film, ±0.1% tolerance, 25ppm/°C resistor and R_O should be ±1%, 100ppm/°C.

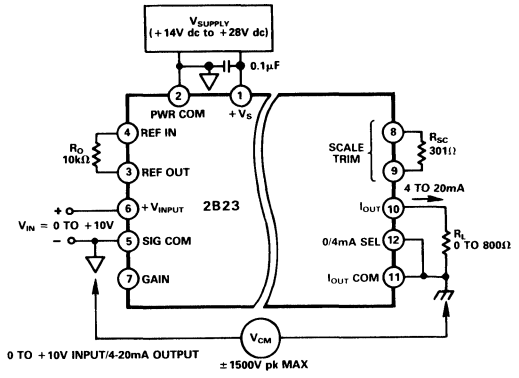


Figure 2. Basic Interconnections

A power supply ($+V_S$) is connected to Pin 1. To avoid ground loops, the user should ensure that the input signal return (SIG COM) does not carry the power supply return current. Power common (Pin 2) and signal common (Pin 5) should be tied at the power supply common terminal.

OPTIONAL TRIM ADJUSTMENTS

Model 2B23 is factory calibrated for a 0 to +10V input range and an output of 4 to 20mA, meeting its listed specifications without use of any external trim potentiometers. If desired, optional span and zero trim adjustments may be easily accomplished as described in the following sections.

Input Gain Adjustment: The input gain of the 2B23 is a scale factor setting that establishes the nominal conversion relationship to accommodate +1V to +10V full scale inputs (V_{IN}). In addition, full scale inputs as low as 100mV may be accommodated.

The value of the gain setting resistor R_G is determined by: R_G (kΩ) = 10kΩ/(G−1) where G represents a ratio of 10V/V_{IN}(V) F.S. For example, to convert a 0 to +1V input to 4 to 20mA output, V_{IN} F.S. = +1V and G = 10V/1V = 10, therefore R_G = 10kΩ/9 = 1.1kΩ. Due to resistor tolerances, allowance should be made to vary R_G by using a series cermet type potentiometer (Figure 3). For best performance, R_G should be a metal film, 1% tolerance, 25ppm/°C resistor.

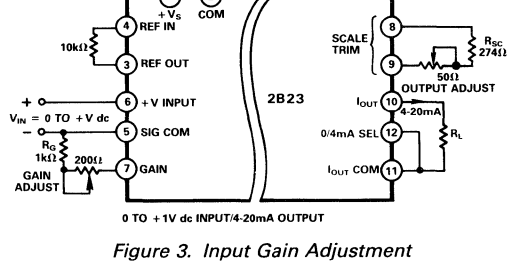
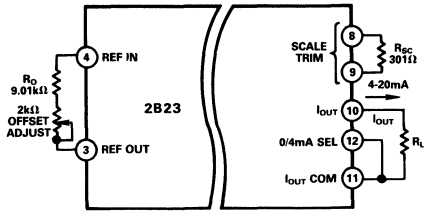


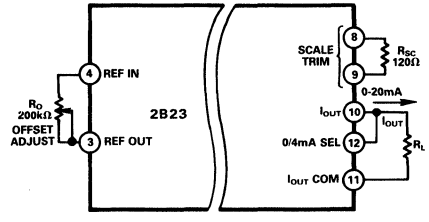
Figure 3. Input Gain Adjustment

Offset and Output Scaling Adjustments: After selecting the required input stage gain, the 2B23 must then be configured for either 4 to 20mA or 0 to 20mA output current range. Figures 4a and 4b illustrate the respective methods for each. The value of the offset resistor R_O is independent from the gain setting and may be adjusted by a series cermet pot.

For fine adjustment of the output current, R_{SC} value should be trimmed as shown in Figure 3.



4a. 4–20mA Output Connections



4b. 0–20mA Output Connections

Figure 4. 4–20mA/0–20mA Scaling Connections

USING MULTIPLE 2B23s

Unlike other transformer-based isolators, the 2B23 does not require any synchronizing circuits to eliminate beat frequency related output errors in multichannel applications. This is due to the use of pulse-width modulation technique in the 2B23. Radiated individual oscillator frequencies will have no effect upon performance, even in situations requiring multiple 2B23s to be located in close proximity to one another. For this reason, no provisions for external synchronization are necessary.

OUTPUT PROTECTION

The current output terminals (Pins 10 and 11) are protected for reverse voltage and shorts up to +32V dc but in many industrial applications it may be necessary to protect the 4 to 20mA from accidental shorts to ac line voltages. The circuit shown in Figure 5 may be employed for this purpose. The maximum permissible load resistance will be lowered by a fuse resistance value when protection circuitry is utilized.

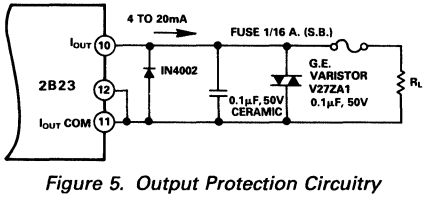


Figure 5. Output Protection Circuitry

APPLICATIONS

In Figure 6, model 2B23 is used in multiloop application of the data acquisition and control system to provide isolated current interface to a recorder, indicator and a valve positioner.

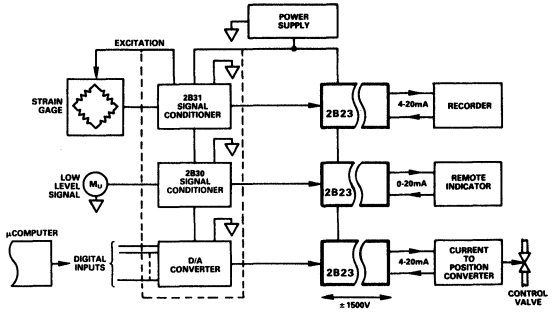


Figure 6. Multiloop Isolation

In applications requiring current to voltage conversion, the 2B23 may be used as shown in Figure 7. An external −10V reference is used to provide necessary input offset. This circuit will provide ±1500V isolation in converting 4-20mA into a 0 to +10V output. The output measurement device must have a high input impedance to avoid loading errors.

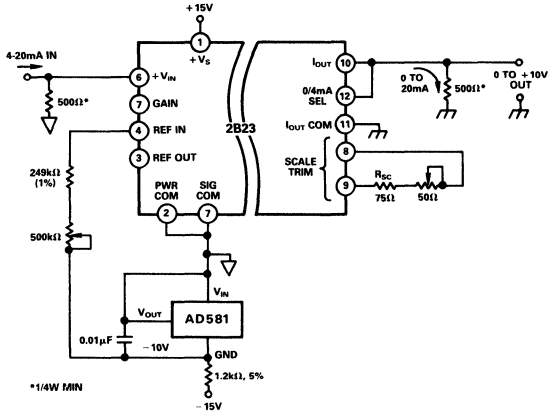


Figure 7. 4–20mA to 0 to +10V Isolated Converter

ANALOG DEVICES

High Performance, Economy Strain Gage/RTD Conditioners

2B30/2B31

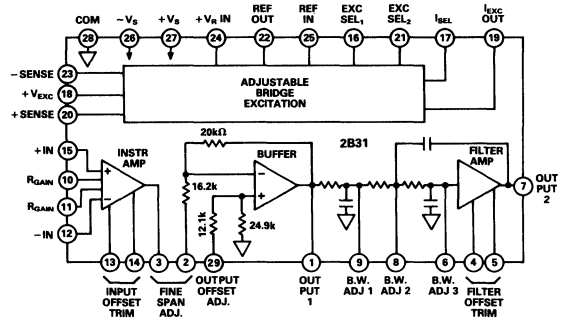
FEATURES

- **Low Cost**
- **Complete Signal Conditioning Function**
- **Low Drift: 0.5μV/°C max ("L"); Low Noise: 1μV p-p max**
- **Wide Gain Range: 1 to 2000V/V**
- **Low Nonlinearity: 0.0025% max ("L")**
- **High CMR: 140dB min (60Hz, G = 1000V/V)**
- **Input Protected to 130V rms**
- **Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)**
- **Programmable Transducer Excitation: Voltage (4V to 15V @ 100mA) or Current (100μA to 10mA)**

APPLICATIONS

- **Measurement and Control of:**
  - **Pressure, Temperature, Strain/Stress, Force, Torque**
- **Instrumentation: Indicators, Recorders, Controllers**
- **Data Acquisition Systems**
- **Microcomputer Analog I/O**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Models 2B30 and 2B31 are high performance, low cost, compact signal conditioning modules designed specifically for high accuracy interface to strain gage-type transducers and RTD's (resistance temperature detectors). The 2B31 consists of three basic sections: a high quality instrumentation amplifier; a three-pole low pass filter, and an adjustable transducer excitation. The 2B30 has the same amplifier and filter as the 2B31, but no excitation capability.

Available with low offset drift of 0.5μV/°C max (RTI, G = 1000V/V) and excellent linearity of 0.0025% max, both models feature guaranteed low noise performance (1μV p-p max) and outstanding 140dB common mode rejection (60Hz, CMV = ±10V, G = 1000V/V) enabling the 2B30/2B31 to maintain total amplifier errors below 0.1% over a 20°C temperature range. The low pass filter offers 60dB/decade roll-off from 2Hz to reduce normal-mode noise bandwidth and improve system signal-to-noise ratio. The 2B31's regulated transducer excitation stage features a low output drift (0.015%/°C max) and a capability of either constant voltage or constant current operation.

Gain, filter cutoff frequency, output offset level and bridge excitation (2B31) are all adjustable, making the 2B30/2B31 the industry's most versatile high-accuracy transducer-interface modules. Both models are offered in three accuracy selections, J/K/L, differing only in maximum nonlinearity and offset drift specifications.

APPLICATIONS

The 2B30/2B31 may be easily and directly interfaced to a wide variety of transducers for precise measurement and control of pressure, temperature, stress, force and torque. For applications in harsh industrial environments, such characteristics as high CMR, input protection, low noise, and excellent temperature stability make 2B30/2B31 ideally suited for use in indicators, recorders, and controllers.

The combination of low cost, small size and high performance of the 2B30/2B31 offers also exceptional quality and value to the data acquisition system designer, allowing him to assign a conditioner to each transducer channel. The advantages of this approach over low level multiplexers include significant improvements in system noise and resolution, and elimination of crosstalk and aliasing errors.

DESIGN FEATURES AND USER BENEFITS

High Noise Rejection: The true differential input circuitry with high CMR (140dB) eliminating common-mode noise pickup errors, input filtering minimizing RFI/EMI effects, output low pass filtering (f_c=2Hz) rejecting 50/60Hz line frequency pickup and series-mode noise.

Input and Output Protection: Input protected for shorts to power lines (130V rms), output protected for shorts to ground and either supply.

Ease of Use: Direct transducer interface with minimum external parts required, convenient offset and span adjustment capability.

Programmable Transducer Excitation: User-programmable adjustable excitation source-constant voltage (4V to 15V @ 100mA) or constant current (100μA to 10mA) to optimize transducer performance.

Adjustable Low Pass Filter: The three-pole active filter (f_c=2Hz) reducing noise bandwidth and aliasing errors with provisions for external adjustment of cutoff frequency.

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2B30/2B31 — SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwise noted)

MODEL	2B30J 2B31J	2B30K 2B31K	2B30L 2B31L
GAIN[1]			
Gain Range	1 to 2000V/V	*	*
Gain Equation	$G = (1 + 94k\Omega/R_G)$ [$20k\Omega/(R_F + 16.2k\Omega)$]	*	*
Gain Equation Accuracy	±2%	*	*
Fine Gain (Span) Adjust. Range	±20%	*	*
Gain Temperature Coefficient	±25ppm/°C max (±10ppm/°C typ)	*	*
Gain Nonlinearity,	±0.01% max	±0.005% max	±0.0025% max
OFFSET VOLTAGES[1]			
Total Offset Voltage, Referred to Input			
Initial, @ +25°C	Adjustable to Zero (±0.5mV typ)	*	*
Warm-Up Drift, 10 Min., G = 1000	Within ±5µV (RTI) of Final Value	*	*
vs. Temperature			
G = 1V/V	±150µV/°C max	±75µV/°C max	±50µV/°C max
G = 1000V/V	±3µV/°C max	±1µV/°C max	±0.5µV/°C max
At Other Gains	±(3 ± 150/G)µV/°C max	±(1 ± 75/G)µV/°C max	±(0.5 ± 50/G)µV/°C max
vs. Supply, G = 1000V/V[5]	±25µV/V	*	*
vs. Time, G = 1000V/V	±5µV/month	*	*
Output Offset Adjust. Range	±10V	*	*
INPUT BIAS CURRENT			
Initial @ +25°C	+200nA max (100nA typ)	*	*
vs. Temperature (0 to +70°C)	−0.6nA/°C	*	*
INPUT DIFFERENCE CURRENT			
Initial @ +25°C	±5nA	*	*
vs. Temperature (0 to +70°C)	±40pA/°C	*	*
INPUT IMPEDANCE			
Differential	100MΩ‖47pF	*	*
Common Mode	100MΩ‖47pF	*	*
INPUT VOLTAGE RANGE			
Linear Differential Input	±10V	*	*
Maximum Differential or CMV Input			
Without Damage	130V rms	*	*
Common Mode Voltage	±10V	*	*
CMR, 1kΩ Source Imbalance			
G = 1V/V, dc to 60Hz[1]	90dB	*	*
G = 100V/V to 2000V/V, 60Hz[1]	140dB min	*	*
dc[2]	90dB min (112 typ.)	*	*
INPUT NOISE			
Voltage, G = 1000V/V			
0.01Hz to 2Hz	1µV p-p max	*	*
10Hz to 100Hz[2]	1µV p-p	*	*
Current, G = 1000			
0.01Hz to 2Hz	70pA p-p	*	*
10Hz to 100Hz[2]	30pA rms	*	*
RATED OUTPUT[1]			
Voltage, 2kΩ Load[3]	±10V min	*	*
Current	±5mA min	*	*
Impedance, dc to 2Hz, G = 100V/V	0.1Ω	*	*
Load Capacitance	0.01µF max	*	*
DYNAMIC RESPONSE (Unfiltered)[2]			
Small Signal Bandwidth			
−3dB Gain Accuracy, G = 100V/V	30kHz	*	*
G = 1000V/V	5kHz	*	*
Slew Rate	1V/µs	*	*
Full Power	15kHz	*	*
Settling Time, G = 100, ±10V Output			
Step to ±0.1%	30µs	*	*
LOW PASS FILTER (Bessel)			
Number of Poles	3	*	*
Gain (Pass Band)	+1	*	*
Cutoff Frequency (−3dB Point)	2Hz	*	*
Roll-Off	60dB/decade	*	*
Offset (at 25°C)	±5mV	*	*
Settling Time, G = 100V/V, ±10V			
Output Step to ±0.1%	600ms	*	*
BRIDGE EXCITATION (See Table 1)			
POWER SUPPLY[4]			
Voltage, Rated Performance	±15V dc	*	*
Voltage, Operating	±(12 to 18)V dc	*	*
Current, Quiescent[6]	±15mA	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	*
Operating	−25°C to +85°C	*	*
Storage	−55°C to +125°C	*	*
CASE SIZE	2" x 2" x 0.4" (51 x 51 x 10.2mm)	*	*

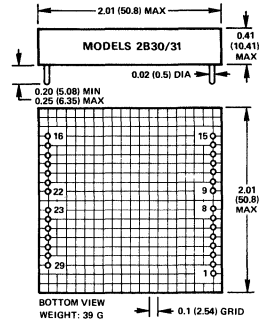
NOTES

*Specifications same as 2B30J/2B31J.
[1] Specifications referred to output at pin 7 with 3.75k, 1%, 25ppm/°C fine span resistor installed and internally set 2Hz filter cutoff frequency.
[2] Specifications referred to the unfiltered output at pin 1.
[3] Protected for shorts to ground and/or either supply voltage.
[4] Recommended power supply ADI model 902-2 or model 2B35
[5] Tracking power supplies.
[6] Does not include bridge excitation and load currents.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

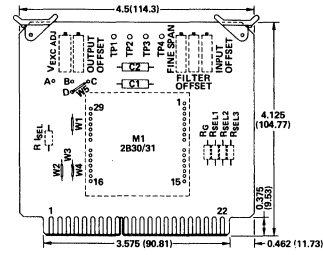


PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT 1 (UNFILTERED)	16	EXC SEL 1
2	FINE GAIN (SPAN) ADJ.	17	I SEL
3	FINE GAIN (SPAN) ADJ.	18	$V_{EXC\ OUT}$
4	FILTER OFFSET TRIM	19	$I_{EXC\ OUT}$
5	FILTER OFFSET TRIM	20	SENSE HIGH (+)
6	BANDWIDTH ADJ. 3	21	EXC SEL 2
7	OUTPUT 2 (FILTERED)	22	REF OUT
8	BANDWIDTH ADJ. 2	23	SENSE LOW (−)
9	BANDWIDTH ADJ. 1	24	REGULATOR $+V_{R\ IN}$
10	R_{GAIN}	25	REF IN
11	R_{GAIN}	26	$-V_S$
12	-INPUT	27	$+V_S$
13	INPUT OFFSET TRIM	28	COMMON
14	INPUT OFFSET TRIM	29	OUTPUT OFFSET TRIM
15	+ INPUT		

Note: Pins 16 thru 25 are not connected in Model 2B30

AC1211/AC1213 MOUNTING CARDS



AC1211/AC1213 CONNECTOR DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
A	REGULATOR $+V_{R\ IN}$	1	EXC SEL 1
B	SENSE LOW (−)	2	I SEL
C	REF OUT	3	$V_{EXC\ OUT}$
D	REF IN	4	$I_{EXC\ OUT}$
E		5	SENSE HIGH (+)
F		6	EXC SEL 2
H		7	OUTPUT OFFSET TRIM
J		8	
K	$-V_S$	9	$-V_S$
L	$+V_S$	10	$+V_S$
M		11	
N	COMMON	12	COMMON
P		13	
R	FINE GAIN ADJ.	14	
S	FINE GAIN ADJ.	15	
T	FILTER OFFSET TRIM	16	
U	FILTER OFFSET TRIM	17	R_{GAIN}
V	OUTPUT 2 (FILTERED)	18	R_{GAIN}
W	- INPUT	19	OUTPUT 1 (UNFILTERED)
X	INPUT OFFSET TRIM	20	BANDWIDTH ADJ. 1
Y	INPUT OFFSET TRIM	21	BANDWIDTH ADJ. 3
Z	+ INPUT	22	BANDWIDTH ADJ. 2

The AC1211/AC1213 mounting card is available for the 2B30/2B31. The AC1211/AC1213 is an edge connector card with pin receptacles for plugging in the 2B30/2B31. In addition, it has provisions for installing the gain resistors and the bridge excitation, offset adjustment and filter cutoff programming components. The AC1211/AC1213 is provided with a Cinch 251-22-30-160 (or equivalent) edge connector. The AC1213 includes the adjustment pots; no pots are provided with the AC1211.

FUNCTIONAL DESCRIPTION

Models 2B30 and 2B31 accept inputs from a variety of full bridge strain gage-type transducers or RTD sensors and convert the inputs to conditioned high level analog outputs. The primary transducers providing direct inputs may be 60Ω to 1000Ω strain gage bridges, four-wire RTD's or two- or three-wire RTD's in the bridge configuration.

The 2B30 and 2B31 employ a multi-stage design, shown in Figure 1, to provide excellent performance and maximum versatility. The input stage is a high input impedance ($10^8\Omega$), low offset and drift, low noise differential instrumentation amplifier. The design is optimized to accurately amplify low level (mV) transducer signals riding on high common mode voltages (±10V), with wide (1-2000V/V), single resistor (R_G), programmable gain to accommodate 0.5mV/V to 36mV/V transducer spans and 5Ω to 2000Ω RTD spans. The input stage contains protection circuitry for accidental shorts to power line voltage (130V rms) and RFI filtering circuitry.

The inverting buffer amplifier stage provides a convenient means of fine gain trim (0.8 to 1.2) by using a 10kΩ potentiometer (R_F); the buffer also allows the output to be offset by up to ±10V by applying a voltage to the noninverting input (pin 29). For dynamic, high bandwidth measurements—the buffer output (pin 1) should be used.

The three-pole active filter uses a unity-gain configuration and provides low-pass Bessel-type characteristics-minimum overshoot response to step inputs and a fast rise time. The cutoff frequency (-3dB) is factory set at 2Hz, but may be increased up to 5kHz by addition of three external resistors (R_{SEL_1} - R_{SEL_3}).

INTERCONNECTION DIAGRAM AND SHIELDING TECHNIQUES

Figure 1 illustrates the 2B31 wiring configuration when used in a typical bridge transducer signal conditioning application. A recommended shielding and grounding technique for preserving the excellent performance characteristics of the 2B30/2B31 is shown.

Because models 2B30/2B31 are direct coupled, a ground return path for amplifier bias currents must be provided either by direct connection (as shown) or by an implicit ground path having up to 1MΩ resistance between signal ground and conditioner common (pin 28). The sensitive input and gain setting terminals should be shielded from noise sources for best performance, especially at high gains. To avoid ground loops, signal return or cable shield should never be grounded at more than one point.

The power supplies should be decoupled with 1μF tantalum and 1000pF ceramic capacitors as close to the amplifier as possible.

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS

Models 2B30/2B31 have been conservatively specified using min-max values as well as typicals to allow the designer to develop accurate error budgets for predictable performance. The error calculations for a typical transducer application, shown in Figure 1 (350Ω bridge, 1mV/V F.S., 10V excitation), are illustrated below.

Assumptions: 2B31L is used, G = 1000, ΔT = ±10°C, source imbalance is 100Ω, common mode noise is 0.25V (60Hz) on the ground return.

Absolute gain and offset errors can be trimmed to zero. The remaining error sources and their effect on system accuracy (worst case) as a % of Full Scale (10V) are listed:

Error Source	Effect on Absolute Accuracy % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.0025	±0.0025
Gain Drift	±0.025	
Voltage Offset Drift	±0.05	
Offset Current Drift	±0.004	
CMR	±0.00025	±0.00025
Noise (0.01 to 2Hz)	±0.01	±0.01
Total Amplifier Error	±0.09175 max	±0.01275 max
Excitation Drift	±0.15 (±0.03 typ)	
Total Output Error (Worst Case)	±0.24175 max (±0.1 typ)	±0.0127 max

The total worst case effect on absolute accuracy over ±10°C is less than ±0.25% and the 2B31 is capable of 1/2 LSB resolution in a 12 bit, low input level system. Since the 2B31 is conservatively specified, a typical overall accuracy error would be lower than ±0.1% of F.S.

In a computer or microprocessor based system, automatic recalibration can nullify gain and offset drifts leaving noise, nonlinearity and CMR as the only error sources. A transducer excitation drift error is frequently eliminated by a ratiometric operation with the system's A/D converter.

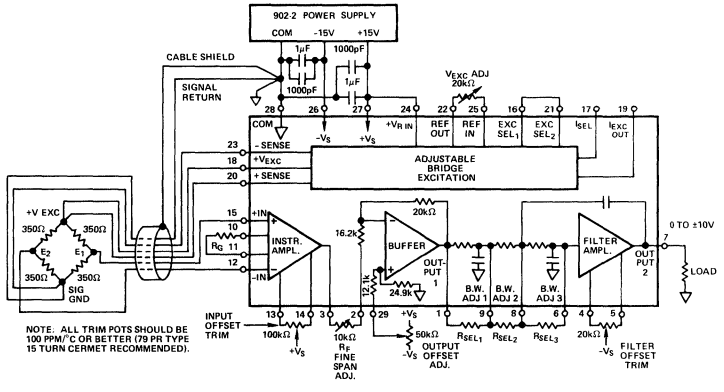


Figure 1. Typical Bridge Transducer Application Using 2B31

BRIDGE EXCITATION (2B31)

The bridge excitation stage of the model 2B31 is an adjustable output, short circuit protected, regulated supply with internally provided reference voltage (+7.15V). The remote sensing inputs are used in the voltage output mode to compensate for the voltage drop variations in long leads to the transducer. The regulator circuitry input (pin 24) may be connected to $+V_S$ or some other positive dc voltage (pin 28 referenced) within specified voltage level and load current range. User-programmable constant voltage or constant current excitation mode may be used. Specifications are listed below in Table I.

MODEL	2B31J	2B31K	2B31L
Constant Voltage Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	*	*
Output Voltage Range	+4V to +15V	*	*
Regulator Input/Output Voltage Differential	3V to 24V	*	*
Output Current[1]	0 to 100mA max	*	*
Regulation, Output Voltage vs. Supply	0.05%/V	*	*
Load Regulation, I_L = 1mA to I_L = 50mA	0.1%	*	
Output Voltage vs. Temperature (0 to +70°C)	0.015%/°C max 0.003%/°C typ	* *	* *
Output Noise	1mV rms	*	*
Reference Voltage (Internal)	7.15V ±3%	*	*
Constant Current Output Mode			
Regulator Input Voltage Range	+9.5V to +28V	*	*
Output Current Range	100µA to 10mA	*	*
Compliance Voltage	0 to 10V	*	*
Load Regulation	0.1%	*	*
Temperature Coefficient (0 to +70°C)	0.003%/°C	*	*
Output Noise	1µA rms	*	*

[1] Output Current derated to 33mA max for 24V regulator input/output voltage differential.

Table I. Bridge Excitation Specifications

OPERATING INSTRUCTIONS

Gain Setting: The differential gain, G, is determined according to the equation:

$$G = (1 + 94k\Omega/R_G)\ [20k\Omega/(R_F + 16.2k\Omega)]$$

where R_G is the input stage resistor shown in Figure 1 and R_F is the variable 10kΩ resistor in the output stage. For best performance, the input stage gain should be made as large as possible, using a low temperature coefficient (10ppm/°C) R_G, and the output stage gain can then be used to make a ±20% linear gain adjustment by varying R_F.

Input Offset Adjustment: To null input offset voltage, an optional 100kΩ potentiometer connected between pins 13 and 14 (Figure 1) can be used. With gain set at the desired value, connect both inputs (pins 12 and 15) to the system common (pin 28), and adjust the 100kΩ potentiometer for zero volts at pin 3. The purpose of this adjustment is to null the internal amplifier offset and it is not intended to compensate for the transducer bridge unbalance.

Output Offset Adjustment: The output of the 2B30/2B31 can be intentionally offset from zero over the ±10V range by applying a voltage to pin 29, e.g., by using an external potentiometer or a fixed resistor. Pin 29 is normally grounded if output offsetting is not desired. The optional filter amplifier offset null capability is also provided as illustrated in Figure 1.

Filter Cutoff Frequency Programming: The low pass filter cutoff frequency may be increased from the internally set 2Hz by the addition of three external resistors connected as shown in Figure 1. The values of resistors required for a desired cutoff frequency, f_c, above 5Hz are obtained by the equation below:

$$R_{SEL_1} = 11.6 \times 10^6/(2.67f_c - 4.34);$$

$$R_{SEL_2} = 27.6 \times 10^6/(4.12f_c - 7)$$

$$R_{SEL_3} = 1.05 \times 10^6/(0.806f_c - 1.3)$$

where R_{SEL} is in ohms and f_c in Hz. Table II gives the nearest 1% R_{SEL} for several common filter cutoff (-3dB) frequencies.

f_c (Hz)	R_{SEL1} (kΩ) (Pin 1 to 9)	R_{SEL2} (kΩ) (Pin 9 to 8)	R_{SEL3} (kΩ) (Pin 8 to 6)
2	Open	Open	Open
5	1270.000	2050.00	383.000
10	523.000	806.00	154.000
50	90.000	137.00	26.700
100	44.200	68.10	13.300
500	8.660	13.30	2.610
1000	4.320	6.65	1.300
5000	0.866	1.33	0.261

Table II. Filter Cutoff Frequency vs. R_{SEL}

Voltage Excitation Programming: Pin connections for a constant voltage output operation are shown in Figure 2. The bridge excitation voltage, V_{EXC}, is adjusted between +4V to +15V by the 20kΩ (50ppm/°C) R_{VSEL} potentiometer. For ratiometric operation, the bridge excitation can be adjusted by applying an external positive reference to pin 25 of the 2B31. The output voltage is given by: $V_{EXC\ OUT} = 3.265V_{REF\ IN}$. The remote sensing leads should be externally connected to the excitation leads at the transducer or jumpered as shown in Figure 2 if sensing is not required.

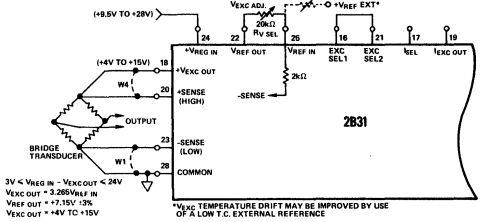


Figure 2. Constant Voltage Excitation Connections

Current Excitation Programming: The constant current excitation output can be adjusted between 100µA to 10mA by two methods with the 2B31. Figure 3 shows circuit configuration for a current output with the maximum voltage developed across the sensor (compliance voltage) constrained to +5V. The value of programming resistor R_{ISEL} may be calculated from the relationship: $R_{ISEL} = (V_{REG\ IN} - V_{REF\ IN})/I_{EXC\ OUT}$. This application requires a stable power supply because any variation of the input supply voltage will result in a change in the excitation current output.

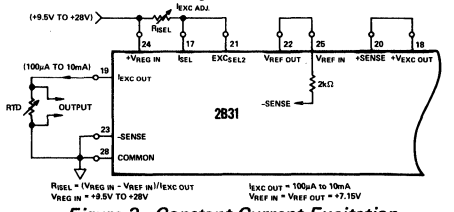


Figure 3. Constant Current Excitation Connections (V_{COMPL} = 0 to +5V)

A compliance voltage range of 0 to +10V can be obtained by connecting the 2B31 as shown in Figure 4. The 2kΩ potentiometer R_{ISEL} is adjusted for desired constant current excitation output.

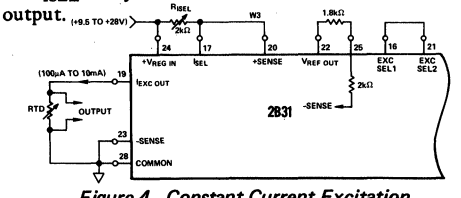


Figure 4. Constant Current Excitation Connections (V_{COMPL} = 0 to +10V)

APPLICATIONS

Strain Measurement: The 2B30 is shown in Figure 5 in a strain measurement system. A single active gage (120Ω, GF = 2) is used in a bridge configuration to detect small changes in gage resistance caused by strain. The temperature compensation is provided by an equivalent dummy gage and two high precision 120Ω resistors complete the bridge. The 2B35 adjustable power supply is set to a low +3V excitation voltage to avoid the self-heating error effects of the gage and bridge elements. System calibration produces a 1V output for an input of 1000 microstrains. The filter cutoff frequency is set at 100Hz.

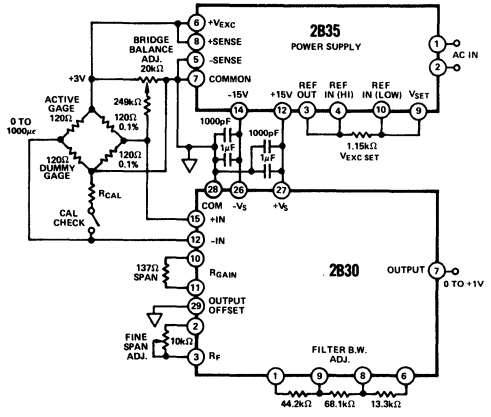


Figure 5. Interfacing Half-Bridge Strain Gage Circuit

Pressure Transducer Interface: A strain gage type pressure transducer (BLH Electronics, DHF Series) is interfaced by the 2B31 in Figure 6. The 2B31 supplies regulated excitation (+10V) to the transducer and operates at a gain of 333.3 to achieve 0-10V output for 0-10,000 p.s.i. at the pressure transducer. Bridge Balance potentiometer is used to cancel out any offset which may be present and the Fine Span potentiometer adjustment accurately sets the full scale output. Depressing the calibration check pushbutton switch shunts a system calibration resistor (R_{CAL}) across the transducer bridge to give an instant check on system calibration.

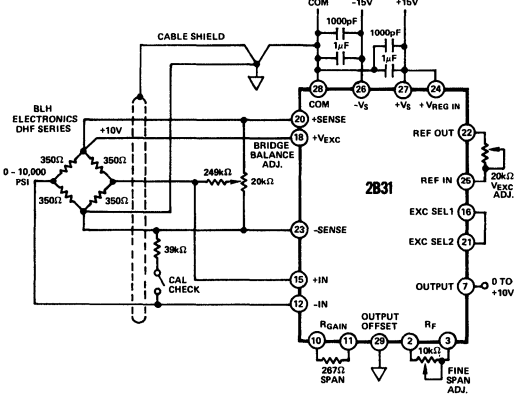


Figure 6. Pressure Transducer Interface Application

Platinum RTD Temperature Measurement: In Figure 7 model 2B31 provides complete convenient signal conditioning in a wide range (-100°C to +600°C) RTD temperature measurement system. YSI - Sostman four-wire, 100Ω platinum RTD (PT139AX) is used. The four wire sensor configuration, combined with a constant current excitation and a high input impedance offered by the 2B31, eliminates measurement errors resulting from voltage drops in the lead wires. Offsetting may be provided via the 2B31's offset terminal. The gain is set by the gain resistor for a +10V output at +600°C. This application requires a stable power supply.

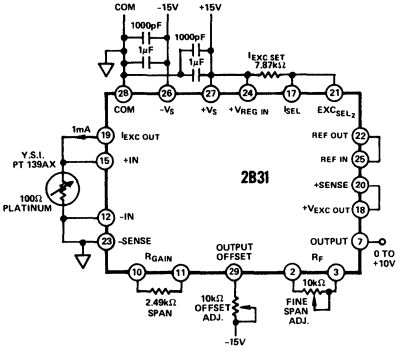


Figure 7. Platinum RTD Temperature Measurement

Interfacing Three-Wire Sensors: A bridge configuration is particularly useful to provide offset in interfacing to a platinum RTD and to detect small, fractional sensor resistance changes. Lead compensation is employed, as shown in Figure 8, to maintain high measurement accuracy when the lead lengths are so long that thermal gradients along the RTD leg may cause changes in line resistance. The two completion resistors (R1, R2) in the bridge should have a good ratio tracking (±5ppm/°C) to eliminate bridge error due to drift. The single resistor (R3) in series with the platinum sensor must, however, be of very high absolute stability. The adjustable excitation in the 2B31 controls the power dissipated by the RTD itself to avoid self-heating errors.

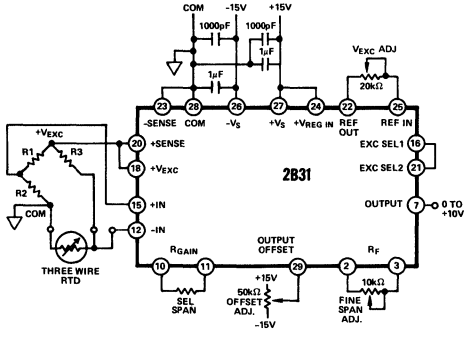


Figure 8. Three-Wire RTD Interface

Linearizing Transducer Output: To maximize overall system linearity and accuracy, some strain gage-type and RTD transducer analog outputs may require linearization. A simple circuit may be used with the 2B31 to correct for the curvature in the input signal as shown in Figure 9. The addition of feedback in the excitation stage will allow for the correction of

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nonlinearity by the addition of two components. The sense of the feedback is determined by whether the nonlinearity is concave upward or concave downward (jumper A to pin 21, or to pin 25). The magnitude of the correction is determined by the resistor, R_{SEL}, and the *linearity adjust* pot provides a fine trim.

If an RTD is to be used, the adjustment can be made efficiently, without actually changing the temperature, by simulating the RTD with a precision resistance decade. The offset is adjusted at the low end of the resistance range, the fine span is adjusted at about one third of the range, and the linearity is adjusted at a resistance corresponding to full-scale temperature. One or two iterations of the adjustments will probably be found necessary because of the interaction of linearity error and scale-factor error. This circuit's applications are not restricted to RTD's; it will work in most cases where bridges are used – e.g., load cells and pressure transducers.

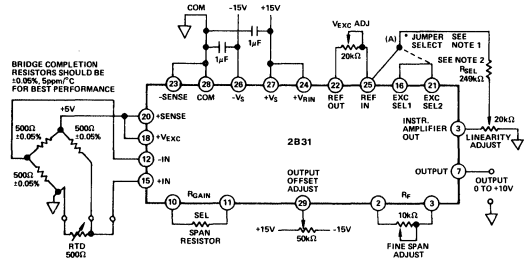


Figure 9. Transducer Nonlinearity Correction

PERFORMANCE CHARACTERISTICS

Input Offset Voltage Drift: Models 2B30/2B31 are available in three drift selections: ±0.5, ±1 and ±3μV/°C (max, RTI, G = 1000V/V). Total input drift is composed of two sources (input and output stage drifts) and is gain dependent. Figure 10 is a graph of the worst case total voltage offset drift vs. gain for all versions.

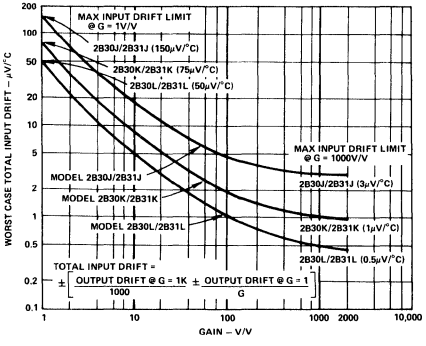


Figure 10. Total Input Offset Drift (Worst Case) vs. Gain

Gain Nonlinearity and Noise: Nonlinearity is specified as a percent of full scale (10V), e.g. 0.25mV RTO for 0.0025%. Three maximum nonlinearity selections offered are: ±0.0025%, ±0.005% and ±0.01% (G = 1 to 2000V/V). Models 2B30/2B31 offer also an excellent voltage noise performance by guaranteeing maximum RTI noise of 1μV p-p (G = 1000V/V, $R_S \leq 5k\Omega$) with noise bandwidth reduced to 2Hz by the LPF.

Common Mode Rejection: CMR is rated at ±10V CMV and 1kΩ source imbalance. The CMR improves with increasing gain. As a function of frequency, the CMR performance is enhanced by the incorporation of low pass filtering, adding to the 90dB minimum rejection ratio of the instrumentation amplifier. The effective CMR at 60Hz at the output of the filter (f_C = 2Hz) is 140dB min. Figure 11 illustrates a typical CMR vs. Frequency and Gain.

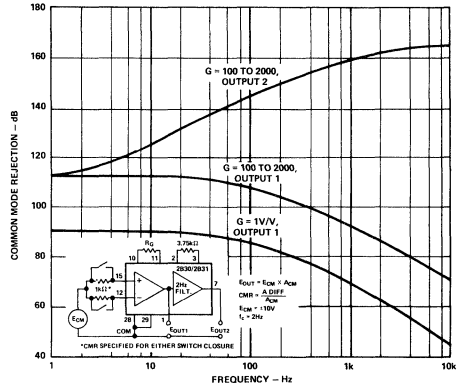


Figure 11. Common-Mode Rejection vs. Frequency and Gain

Low Pass Filter: The three pole Bessel-type active filter attenuates unwanted high-frequency components of the input signal above its cutoff frequency (–3dB) with 60dB/decade rolloff. With a 2Hz filter, attenuation of 70dB at 60Hz is obtained, settling time is 600ms to 0.1% of final value with less than 1% overshoot response to step inputs. Figure 12 shows the filter response.

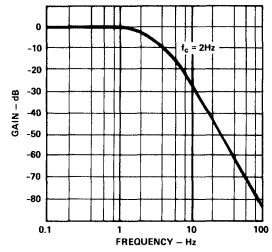


Figure 12. Filter Amplitude Response vs. Frequency

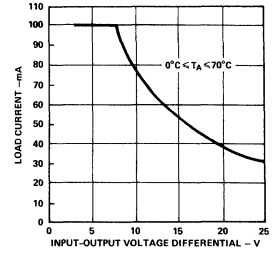


Figure 13. Maximum Load Current vs. Regulator Input-Output Voltage Differential

Bridge Excitation (2B31): The adjustable bridge excitation is specified to operate over a wide regulator input voltage range (+9.5V to +28V). However, the maximum load current is a function of the regulator circuit input-output differential voltage, as shown in Figure 13. Voltage output is short circuit protected and its temperature coefficient is ±0.015% V_{OUT}/°C max (±0.003%/°C typ). Output temperature stability is directly dependent on a temperature coefficient of a reference and for higher stability requirements, a precision external reference may be used.

ANALOG DEVICES

Isolated, Thermocouple Signal Conditioner

2B50

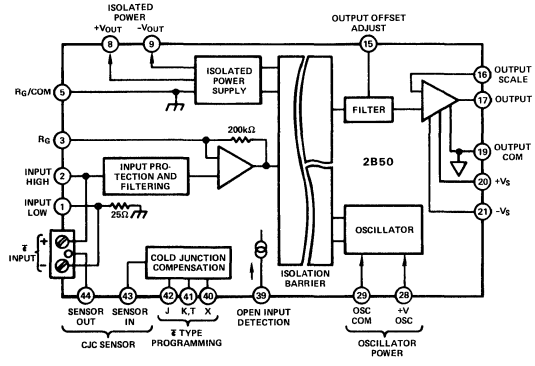
FEATURES

Accepts J, K, T, E, R, S or B Thermocouple Types
Internally Provided Cold Junction Compensation
High CMV Isolation: ±1500V pk
High CMR: 160dB min @ 60Hz
Low Drift: ±1μV/°C max (2B50B)
High Linearity: ±0.01% max (2B50B)
Input Protection and Filtering
Screw Terminal Input Connections

APPLICATIONS

Precision Thermocouple Signal Conditioning For:
- **Process Control and Monitoring**
- **Industrial Automation**
- **Energy Management**
- **Data Acquisition Systems**

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The model 2B50 is a high performance thermocouple signal conditioner providing input protection, isolation and common mode rejection, amplification, filtering and integral cold junction compensation in a single, compact package.

The 2B50 has been designed to condition low level analog signals, such as those produced by thermocouples, in the presence of high common mode voltages. Featuring direct thermocouple connection via screw terminals and internally provided reference junction temperature sensor, the 2B50 may be jumper programmed to provide cold junction compensation for thermocouple types J, K, T, and B, or resistor programmed for types E, R, and S.

The high performance of the 2B50 is accomplished by the use of reliable transformer isolation techniques. This assures complete input to output galvanic isolation (±1500V pk) and excellent common mode rejection (160dB @ 60Hz).

Other key features include: input protection (220V rms), filtering (NMR of 70dB @ 60Hz), low drift amplification (±1μV/°C max - 2B50B), and high linearity (±0.01% max - 2B50B).

APPLICATIONS

The 2B50 has been designed to provide thermocouple signal conditioning in data acquisition systems, computer interface systems, and temperature measurement and control instrumentation.

In thermocouple temperature measurement applications, outstanding features such as low drift, high noise rejection, and 1500V isolation make the 2B50 an ideal choice for systems used in harsh industrial environments.

DESIGN FEATURES AND USER BENEFITS

High Reliability: To assure high reliability and provide isolation protection to electronic instrumentation, the 2B50 has been conservatively designed to meet the IEEE Standard for transient voltage protection (472-1974: SWC) and provide 220V rms differential input protection.

High Noise Rejection: The 2B50 features internal filtering circuitry for elimination of errors caused by RFI/EMI, series mode noise, and 50Hz/60Hz pickup.

Ease of Use: Internal compensation enables the 2B50 to be used with seven different thermocouple types. Unique circuitry offers a choice of internal or remote reference junction temperature sensing. Thermocouple connections may be made either by screw terminals or, in applications requiring PC Board connections, by terminal pins.

Small Package: 1.5" X 2.5" X 0.6" size conserves board space.

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2B50—SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

MODEL	2B50A	2B50B
INPUT SPECIFICATIONS		
Thermocouple Types		
Jumper Configurable Compensation	J, K, T, or B	*
Resistor Configurable Compensation	R, S, or E	*
Input Span Range	±5mV to ±100mV	*
Gain Range	50V/V to 1000V/V	*
Gain Equation	$1 + (200k\Omega/R_G)$	*
Gain Error	±0.25%	*
Gain Temperature Coefficient	±35ppm/°C max	±25ppm/°C max
Gain Nonlinearity[1]	±0.025% max	±0.01% max
Offset Voltage		
Input Offset (Adjustable to Zero)	±50μV	*
vs. Temperature	±2.5μV/°C max	±1μV/°C max
vs. Time	±1.5μV/month	*
Output Offset (Adjustable to Zero)	±10mV	*
vs. Temperature	±30μV/°C	*
Total Offset Drift	$\pm\left(2.5 + \frac{30}{G}\right)$ μV/°C	$\pm\left(1 + \frac{30}{G}\right)$ μV/°C
Input Noise Voltage		
0.01Hz to 100Hz, R_S = 1kΩ	1μV p-p	*
Maximum Safe Differential Input Voltage	220V rms, Continuous	*
CMV, Input to Output		
Continuous, ac or dc	±1500V pk max	*
Common Mode Rejection		
@ 60Hz, 1kΩ Source Unbalance	160dB min	*
Normal Mode Rejection @ 60Hz	70dB min	*
Bandwidth	dc to 2.5Hz (-3dB)	*
Input Impedance	100MΩ	*
Input Bias Current[2]	±5nA	*
Open Input Detection	Downscale	*
Response Time[3], G = 250	1.4sec	*
Cold Junction Compensation		
Initial Accuracy[4]	±0.5°C	*
vs. Temperature[5] (+5°C to +45°C)	±0.01°C/°C	*
OUTPUT SPECIFICATIONS		
Output Voltage Range[6]	±5V @ ±2mA	*
Output Resistance	0.1Ω	*
Output Protection	Continuous Short to Ground	*
POWER SUPPLY		
Voltage		
Output ±V_S (Rated Performance)	±15V dc ±10% @ ±0.5mA	*
(Operating)	±12V to ±18V dc max	*
Oscillator +V_{OSC} (Rated Performance)	+13V to +18V @ 15mA	*
ENVIRONMENTAL		
Temperature Range, Rated Performance	0 to +70°C	*
Operating	-25°C to +85°C	*
Storage Temperature Range	-55°C to +85°C	*
RFI Effect (5W @ 470MHz @ 3ft)		
Error	±0.5% of Span	*
PHYSICAL		
Case Size	1.5" X 2.5" X 0.6"	*

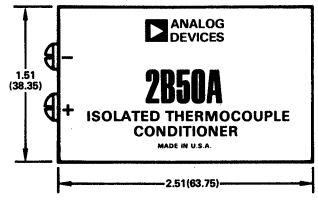
NOTES

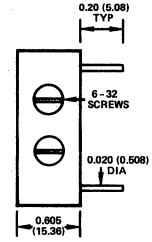
*Specifications same as 2B50A.
[1] Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line; e.g., nonlinearity at an output span of 10V pk-pk (±5V) is ±0.01% or ±1mV.
[2] Does not include open circuit detection current of 20nA (optional by jumper connection).
[3] Open input response time is dependent upon gain.
[4] When used with internally provided CJC sensor.
[5] Compensation error contributed by ambient temperature changes at the module.
[6] Output swing of ±10V may be obtained through output scaling (Figure 5).

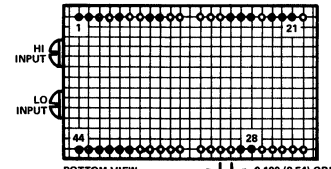
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).







PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	INPUT LO	23	
2	INPUT HI	24	
3	R_G	25	
4		26	
5	R_G/COM	27	
6		28	+V OSC
7		29	OSC COM
8	+V ISO OUT	30	
9	-V ISO OUT	31	
10		32	
11		33	
12		34	
13		35	
14		36	
15	OUTPUT OFFSET ADJUST	37	
		38	
16	OUTPUT SCALE	39	OPEN INPUT DET.
17	OUTPUT	40	X
18		41	K, T ‡ TYPE PROGRAMMING
19	OUTPUT COM	42	J
20	+V_S	43	CJC SENSOR IN
21	-V_S	44	CJC SENSOR OUT
22			

MATING SOCKET: AC1218

FUNCTIONAL DESCRIPTION

The internal structure of the 2B50 is shown in Figure 1. An input filtering and protection network precedes a low drift, high performance amplifier whose gain is set by a user supplied resistor (R_G) for gains of 50 to 1000V/V. Isolated power is brought out to permit convenient adjustment of the input offset voltage, if desired.

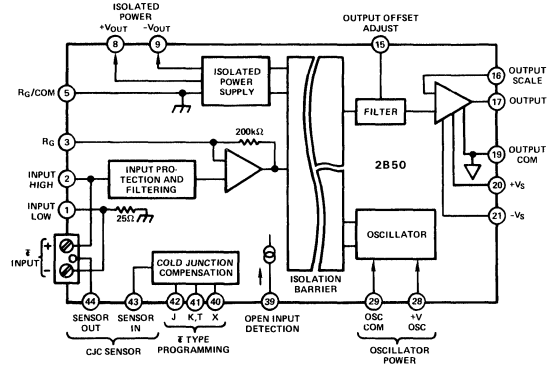


Figure 1. 2B50 Functional Block Diagram

Internal circuitry provides reference junction compensation. An integral reference junction sensor is provided for direct thermocouple connections, or an external reference sensor (2N2222 transistor) may be used in applications having remote thermocouple termination. Compensating networks for thermocouple types J, K, and T are built into the 2B50. A fourth compensation (X) may be programmed with a single resistor for any other thermocouple type. The 2B50 can be programmed for uncompensated output when used with inputs other than thermocouples.

Transformer coupling is used to achieve stable, reliable input to output galvanic isolation, as well as elimination of ground loop error effects.

Normally, the full scale output of the 2B50 is ±5V. However, with the addition of an external resistive divider, the output buffer amplifier may be scaled for a gain of up to 2, providing a full scale output swing of ±10V.

OPERATING INSTRUCTIONS

The connections shown in Figure 2 are common to most applications using the 2B50, and, in many cases, will be all that is required.

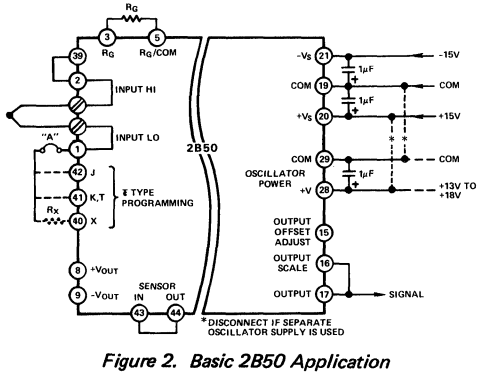


Figure 2. Basic 2B50 Application

Two sets of parallel thermocouple input connections are provided. The thermocouple input may be connected by screw terminals (Input+, Input –) or to terminal Pins 1(–) and 2(+) in cases where thermocouples are to be remotely terminated. The following sections describe a basic thermocouple application, as well as detail some optional connections to enhance performance in more demanding applications. Jumper A (Figure 2) is used to disconnect cold junction compensation circuitry during offset adjustments.

INTERCONNECTION GUIDELINES

All power supply inputs should be decoupled with 1μF capacitors as close to the unit as possible. Any jumpers installed for programming purposes should also be installed as close as possible to minimize noise pickup effects.

Since the oscillator section of the 2B50 accounts for most of the power consumption but can accept a wide range of voltage (+13V to +18V), it may be desirable to power this section from a convenient source of unregulated power.

If the same supply is to be used for both amplifier and oscillator circuitry, the power supply returns should be brought out separately so that oscillator power supply currents do not flow in the low lead of the signal output. In either case, a 1μF capacitor must be connected from $+V_{OSC}$ (Pin 28 to Oscillator COM (Pin 29).

The oscillator and amplifier sections are completely isolated; therefore, a dc power return path is not required between the two power supply commons.

GAIN SETTING

The gain of the 2B50 is set by a user-supplied resistor (R_G) connected as shown in Figure 2. Gain will normally be selected so that the maximum output of the signal source will result in a plus full scale output swing. The resistor value required is determined by the equation: $R_G = 200k\Omega/G-1)$.

A series trim on the gain setting resistor can be used to trim out the resistor tolerance and module gain error (Figure 3). Since addition of a series resistance will always decrease gain, the value of the gain-setting resistor should be selected to provide a gain somewhat higher than the desired trimmed gain. A good quality (e.g., 10ppm/°C), metal-film resistor should be used for R_G, since drift of R_G will add to the overall gain drift of the 2B50. A cermet pot is suitable for the trim. Note that a minimum gain of 50 is required for guaranteed operation.

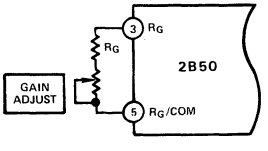


Figure 3. Gain Adjustment

INPUT AND OUTPUT OFFSET ADJUSTMENTS

The 2B50 has provisions for adjusting input and output offset errors of the module. None of the offset adjustments will affect drift performance, and adjustments need not be used unless the particular application calls for lower offsets than those specified.

Connections for offset adjustments are shown in Figure 4. Isolated supply voltages are brought out for input trimming convenience only and are not for use as a power supply for external components.

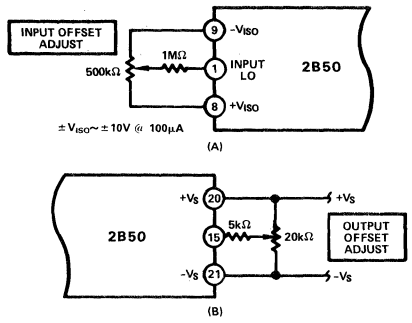


Figure 4. (A) Input and (B) Output Offset Adjustment

OFFSET CALIBRATION

1. Short Input + and Input – together.
2. Disconnect cold junction compensation circuitry by removing Jumper "A" (Figure 2).
3. Adjust input offset trim pot (±250μV range, RTI) to zero output while operating at the desired gain. In most applications, adjustment of the input offset alone will be sufficient. Output offset adjustment (±30mV range) may be performed if it is desired to adjust output offset on the nonisolated side.

OPEN INPUT DETECTION

Connecting the open input detection pin (Pin 39) to Input High (Pin 2) creates a 20nA bias current which will provide a negative overscale response if the input is opened, or in case of thermocouple "burn out". The speed at which this occurs is dependent on gain, with a typical response time of 1.4sec @ G = 250. For positive upscale response, connect a 500MΩ resistor between $+V_{ISO}$ (Pin 8) and Input Hi (Pin 2).

OUTPUT SCALING

With the output scale (Pin 16) connected to the output (Pin 17), the full scale output range is ±5V and the total gain is equal to the gain set by R_G. For applications requiring a full scale output of ±10V, a resistive divider may be connected to provide a gain of 2 at the output amplifier (see Figure 5). In this configuration, total gain will be twice the gain set by R_G. Output gains greater than 2 cannot be used.

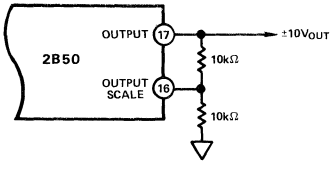


Figure 5. Output Scaling Connections

COLD JUNCTION COMPENSATION

The 2B50 may be programmed to provide cold junction compensation for types J, K and T thermocouples by connecting a jumper from Input Low (Pin 1) to the appropriate programming points (Pin 42 for J, Pin 41 for K or T). To compensate other themocouple types, a resistor (R_X) is connected from the "X" programming point (Pin 40) to Input Low (Pin 1). Table I shows the appropriate R_X values for types E, R, and S. R_X should be a 50ppm/°C, 1% tolerance resistor.

Type B thermocouples are unique, in that they have almost no output in the +5°C to +45°C range, and therefore, do not require cold junction compensation at all. To accommodate a type B thermocouple, resistor R_X must be left open. Error due to cold junction temperature will be less than ±1°C for any measurement above 260°C. In the measurement range above 1000°C (where type B thermocouples are normally used) the error will be less than ±0.3°C.

T Type	R_X (kΩ)
E	1.85
R, S	19.6
B	Open

Table I. Compensation Values for Thermocouple Types E, R, S and B

REMOTE REFERENCE SENSING

In applications requiring termination of themocouple leads at a point located remotely from the 2B50, with connections brought to the 2B50 (Pins 1, 2) by copper wires, reference temperature sensing at the remote location will be necessary. The 2B50 has provisions for connection of a 2N2222 transistor (metal can version) for use as a reference junction sensor. The connections are shown in Figure 6. The remote sensing transistor is calibrated by adjusting R_{CAL} to obtain the value of V_{CAL} as specified in Table II.

(Example: V_{CAL} = 570.0mV @ 25°C)

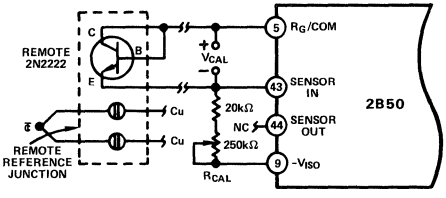


Figure 6. Remote Reference Junction Sensing

Sensor Temp (°C)	V_{CAL} (mV)
5	616.5
10	604.9
15	593.3
20	581.6
25	570.0
30	558.4
35	546.8
40	535.1
45	523.5

(Values may be interpolated)

Table II. Calibration Voltages vs. Sensor Temperature

Proper sensor placement is important. Close thermal contact of the sensor and thermocouple termination point (reference junction) is essential for accurate operation of the 2B50. The sensor may be placed any distance from the 2B50. When the sensor leads are more than ten feet long, or in the presence of strong noise signal sources, shielded cable should be used.

ANALOG DEVICES

Four-Channel, Isolated Thermocouple/mV Conditioners

2B54/2B55

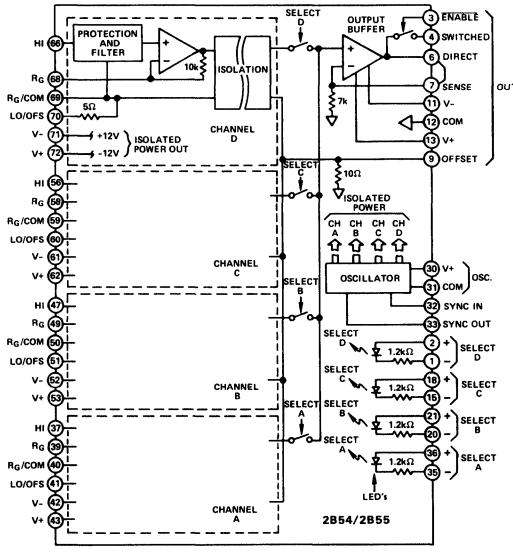
FEATURES

Low Cost Per Channel
Wide Input Span Range: ±5mV to ±100mV (2B54)
±50mV to ±5V (2B55)
Pin Compatible with 2B34 RTD Conditioner
High CMV Isolation: ±1000V *dc*; CMR = 156dB min @ 60Hz
Low Input Offset Voltage Drift: ±1μV/°C max (2B54B)
Low Gain Drift: ±25ppm/°C max (2B54B)
Low Nonlinearity: ±0.02% max (±0.012% typ)
Normal Mode Input Protection (130V rms) and Filtering
Channel Multiplexing: 400 chan/sec Scanning Speed
Solid State Reliability

APPLICATIONS

Multichannel Thermocouple Temperature Measurements
Low and High Level Data Acquisition Systems
Industrial Measurement and Control Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Models 2B54 and 2B55 are low cost, high performance, four-channel signal conditioners. Both models are functionally complete, providing input protection, isolation and common mode rejection, multiplexing, filtering and amplification.

The 2B54 has been designed to condition low level signals (±5mV to ±100mV), like those generated by thermocouples or strain gages, in the presence of high common mode voltages. The 2B55 is optimized to condition ±50mV to ±5V or 4 to 20mA transmitter signals as inputs. The four-channel structure of both models results in significant cost and size reduction.

The high performance of the 2B54 and 2B55 is accomplished by the use of reliable transformer isolation techniques and an amplifier-per-channel architecture. Each of the input channels is galvanically isolated (±1000V dc) from the other input channels and from output ground. The amplifier-per-channel structure is used to obtain low input drift (±1μV/°C max, 2B54B), high common mode rejection (156dB @ 60Hz), and very stable gain (±25ppm/°C max). Other key features include low input noise (1μV p-p), low nonlinearity (±0.02% max) and open-thermocouple detection (2B54).

APPLICATIONS

Models 2B54 and 2B55 were designed to serve as a superior alternative to the relay multiplexing circuits used in multi-channel data acquisition systems, computer interface systems, process signal isolators, and temperature measurement and control instrumentation. Advantages over relay circuits include functional versatility, superior performance, and solid state reliability. Both models are also pin compatible with the 2B34, four-channel RTD/strain gage conditioner.

In thermocouple temperature measurement applications, outstanding low drift, high noise rejection, high throughput and 1000V isolation make the 2B54 a natural choice over flying capacitor multiplexers in conditioning any thermocouple type. When cold junction compensation is required in measurement of temperature with thermocouples, the 2B54 may be used directly with the model 2B56 Universal Cold Junction Compensator.

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DESIGN FEATURES AND USER BENEFITS

High Reliability: To assure high reliability and provide isolation protection to electronic instrumentation, reliable transformer isolation and solid state switching are used. Both models have been conservatively designed to meet the IEEE standard for Transient Voltage Protection (472-1974:SWC) and offer 130V rms normal mode input protection.

High Noise Rejection: To preserve high system accuracy in electrically noisy industrial environments, the 2B54 and 2B55 provide excellent common mode noise rejection, RFI/EMI immunity, and low pass filtering for rejection of series mode noise and 50Hz/60Hz pickup.

Ease of Use: The multichannel, functionally complete design in a compact (2" X 4" X 0.4") module, assures ease of use, conserves board space and eliminates the need for a number of discrete components necessary in relay multiplexing circuits.

Low Cost: The 2B54 and 2B55 offer the lowest cost per channel for isolated, solid state, low level signal conditioners.

2B54/2B55—SPECIFICATIONS (typical @ +25°C and V_S = ±15V and V_{OSC} = +15V, unless otherwise noted)

Model	2B54A	2B54B	2B55A
ANALOG INPUTS			
Number of Channels	4	*	*
Input Span Range	±5mV to ±100mV	*	±50mV to ±5V
Gain Equation	$G = 1 + 10k\Omega/R_G$	*	*
Gain Error	±0.2% max (G = 50 to 300)	*	±0.2% max (G = 1 to 100)
	±1% max (G = 1000)	*	NA
Gain Temperature Coefficient	±35ppm/°C max	±25ppm/°C max	±25ppm/°C max
Gain Nonlinearity[1]	±0.03% max (G = 50 to 300)	±0.02% max(±0.012% typ)	±0.02% max (G = 1 to 100)
	±0.03% (G = 1000)	*	NA
Offset Voltage			
Input Offset, Initial (Adj. to Zero)	±20µV max	*	±50µV max
vs. Temperature	±2.5µV/°C max	±1µV/°C max(±0.5µV/°C typ)	±5µV/°C max
vs. Time	±1.5µV/month	*	*
Output Offset (Adjustable to Zero)	±12mV max	*	*
vs. Temperature	±50µV/°C max	*	*
Total Offset Drift (RTI), max	$\pm\left(2.5+\frac{50}{G}\right)\mu V/°C$	$\pm\left(1+\frac{50}{G}\right)\mu V/°C$	$\pm\left(5\mu V+\frac{50}{G}\right)\mu V/°C$
Input Noise Voltage			
0.01Hz –100Hz, R_S = 1kΩ	1µV p-p	*	*
CMV, Channel-to-Channel or Channel-to-Ground			
Continuous, ac, 60Hz	750V rms	*	*
Continuous, ac or dc	±1000V pk max	*	*
Common Mode Rejection			
$R_S \leq 100\Omega, f \geq 50Hz$	156dB min (G = 1000)	*	145dB min (G = 100)
$R_S \leq 100\Omega, f \geq 50Hz$	128dB min (G = 50)	*	110dB min (G = 1)
Normal Mode Input, Without Damage	130V rms, 60Hz	*	*
Normal Mode Rejection, @ 60Hz	55dB min (G = 1000)	*	55dB min (G = 100)
Input Resistance, Power On	100MΩ	*	*
Power Off	35kΩ min	*	74kΩ min
Input Bias Current	+8nA max	*	*
ANALOG OUPUT			
Output Voltage Swing[2]	±5V @ ±5mA	*	*
Output Noise, dc – 100kHz	0.8mV p-p	*	*
Output Resistance			
Direct Output	0.1Ω	*	*
Switched Output	35Ω	*	*
CHANNEL SELECTION			
Channel Selection Time to ±0.01% FS	2.5ms max	*	*
Channel Scanning Speed	400 chan/sec min	*	*
Channel Select Input Reverse Voltage			
Rating	3V max	*	*
POWER SUPPLY			
Voltage			
Output $\pm V_S$ (Rated Performance)	±15V dc ±10%	*	*
(Operating)	±12V to ±18V dc max	*	*
Oscillator $+V_{OSC}$			
(Rated Performance)	+13.5V to +24V	*	*
Absolute max $+V_{OSC}$	+26V	*	*
Current			
Output $\pm V_S$ = ±15V	±4mA max	*	*
Oscillator $+V_{OSC}$ = +15V	40mA max	*	*
Supply Effect on Offset			
Output $\pm V_S$	100µV/V RTO	*	*
Oscillator $+V_{OSC}$	1µV/V RTI	*	*
ENVIRONMENTAL			
Temperature			
Rated Performance	0 to +70°C	*	*
Operating	–25°C to +85°C	*	*
Storage	–55°C to +85°C	*	*
Relative Humidity			
Non-Condensing to +40°C	0 to 85%	*	*
CASE SIZE	2" X 4" X 0.4"	*	*

NOTES

*Specifications same as 2B54A.

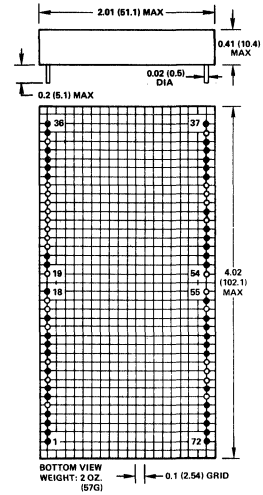
[1] Gain nonlinearity is specified as a percentage of output signal span representing peak deviation from the best straight line; e.g. nonlinearity at an output span of 10V pk-pk (±5V) is ±0.02% or ±2mV.

[2] Protected for shorts to ground and/or either supply voltage.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTES:
TERMINAL PINS INSTALLED ONLY IN SHADED HOLE LOCATIONS.

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	–	37	HI
2	+ SELECT CH. D	38	
3	SW'D OUTPUT ENABLE	39	R_G
4	SWITCHED	40	R_G/COM CHANNEL A
5		41	LO/OFS
6	DIRECT	42	V- OUT
7	SENSE	43	V+ OUT
8	OUTPUT	44	
9	OFS. ADJ.	45	
10		46	
11	-V_S	47	HI
12	COM	48	
13	+V_S	49	R_G
14		50	R_G/COM CHANNEL B
15	–	51	LO/OFS
16	SELECT CH. C	52	V- OUT
17		53	V+ OUT
18	+	54	
19		55	
20	–	56	HI
21	+ SELECT CH. B	57	
22		58	R_G
23		59	R_G/COM CHANNEL C
24		60	LO/OFS
25		61	V- OUT
26		62	V+ OUT
27		63	
28		64	
29		65	
30	+V_{OSC}	66	HI
31	COM OSC. POWER	67	
32	IN	68	R_G
33	OUT SYNC	69	R_G/COM CHANNEL D
34		70	LO/OFS
35	–	71	V- OUT
36	+ SELECT CH. A	72	V+ OUT

FUNCTIONAL DESCRIPTION

The internal structure of the 2B54/2B55 is shown in Figure 1. Four individually isolated input channels are multiplexed into a single output buffer, with the desired channel selected by control inputs SELECT A through SELECT D. Isolated power and timing signals for the input channels are provided by an internal oscillator.

Each channel contains an input protection and filtering network and a low-drift amplifier whose gain is set by a user-supplied resistor (R_G). Additional filtering is provided in the amplifier circuit. This structure preserves signal integrity by taking all signal gain ahead of the isolation and multiplexing circuits. The isolated power supply for each channel is brought out to permit convenient fine adjustment of the input offset voltage if desired.

Transformer coupling is used to achieve stable, reliable galvanic isolation of each channel from all other channels and from output ground. Although the bandwidth of the input channels is small (<2Hz at high gains) to provide immunity to normal-mode noise, the multiplexing technique allows the channels to be scanned at a high rate (400 channels/sec). Thus a high revisitation rate is maintained even in systems with a large number of input channels.

The output buffer amplifier operates at unity gain with feedback provided by an external connection from the DIRECT output to the SENSE input. The DIRECT output provides a ±5V swing with low source resistance to permit error-free operation with heavy loads. In addition, a separate series-switched output with an active-low enable control is provided so that multiple modules may be combined without the use of external analog multiplexers. An offset trim point which does not affect drift is also provided on the output channel.

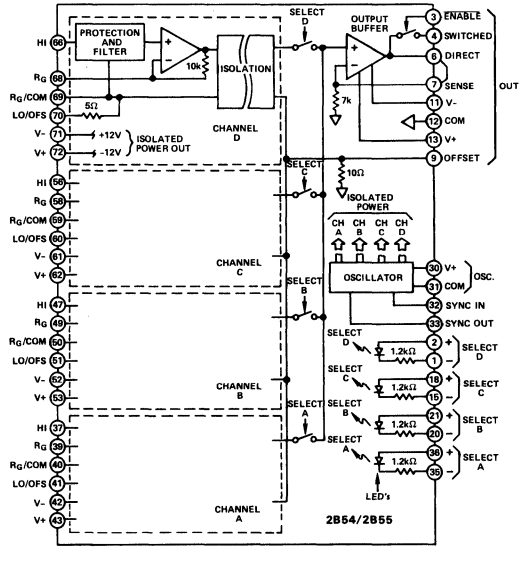


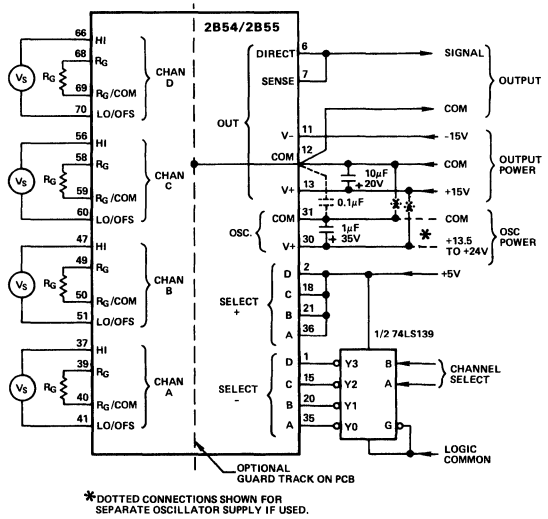
Figure 1. 2B54/2B55 Functional Block Diagram

The internal oscillator has its own power supply pins for enhanced application flexibility, and a sync mechanism is provided to eliminate beat-frequency errors when multiple 2B54/2B55's are used or when a system clock is present.

The 2B54 and 2B55 share the same design, differing only in input specifications and filter characteristics.

OPERATING INSTRUCTIONS

The connections shown in Figure 2 are common to most applications of the 2B54/2B55, and in many cases will be all that is required. The following sections describe this basic application and also detail some optional connections which enhance the module's utility in more complex applications.



*DOTTED CONNECTIONS SHOWN FOR SEPARATE OSCILLATOR SUPPLY IF USED.

Figure 2. Basic 2B54/2B55 Application

Interconnection Guidelines

In any high accuracy isolator application it is important to minimize coupling between input and output, and the 2B54/2B55 pinout has been designed to make this easy to do. For best results, keep all leads associated with signals on the input edge as far as possible from signals on the output edge. This will minimize the effects of board leakage and capacitance. The use of a guard track on both sides of the board (Figure 2) can also be helpful.

The power supplies should be decoupled with tantalum capacitors as close to the unit as possible. For lowest noise, the output grounding scheme should be as shown in Figure 2. The output signal common is connected directly to pin 12, with power supply returns brought separately to that pin so that power supply currents do not flow in the low lead of the signal output.

Since most of the power taken by the 2B54/2B55 is supplied to the internal oscillator which requires only a positive supply and can accommodate a wide range of supply voltages, it is sometimes desirable to power the oscillator from a convenient source of unregulated power (such as +24V — Figure 2). A 0.1µF capacitor should be then connected directly from pin 12 to pin 31. Since the output and oscillator circuits are not fully isolated, a dc path must exist between the two power supply commons. A small (one or two volts) potential difference between OUT COM and OSC COM will not affect operation.

Gain Setting

The gain of each channel is independently set by a user-supplied resistor (R_G) connected as shown in Figure 2. Channel gain will normally be selected so that the maximum output of the signal source will result in a plus or minus full scale (±5V) output swing. The resistor value required is R_G = 10kΩ/ (G - 1). Thus if R_G = 101Ω, the gain will be 100, and an input signal swing of ±50mV will yield an output span of ±5V.

A parallel trim on the gain-setting resistor can be used to trim out the resistor's tolerance and the module's gain error (Figure 3). Since a parallel trim will always increase the gain, the value of the gain-setting resistor should be chosen to give an untrimmed gain somewhat lower than the desired trimmed gain. Good quality metal-film resistors should be used for R_G since gain accuracy and drift are a direct function of R_G's characteristics. Cermet pots are suitable for the trim.

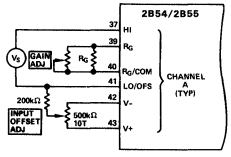


Figure 3. Input Offset and Gain Adjustments

Optional Offset Adjustment

The 2B54/2B55 has provision for fine adjustment of the input offset of each channel and the output offset of the entire module. None of the offset adjustments affect offset drift, and there is no need to make any adjustment unless the application calls for tighter offsets than those specified for the module type.

Connections for input offset adjustment are shown in Figure 3. This is a fine trim with a limited range (±250μV – 2B54 and ±1mV – 2B55, RTI), used to adjust each channel for zero offset while operating at the desired gain. Since the range of the input offset trim is small, it will usually be necessary to adjust output offset first. This can be conveniently done by operating one channel with zero input at unity gain (by disconnecting the gain resistor) and adjusting the output offset control for zero output. Connections for output offset adjustment are shown in Figure 4.

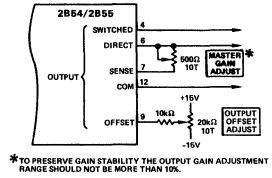


Figure 4. Output Offset and Master Gain Adjustments

An alternative offset adjustment procedure is appropriate in applications where the channel gains are field-selected by switching the gain-setting resistor. Here it is desirable to set the input offset so that there is no zero shift at the output when the gain is changed. To make the adjustment, switch back and forth from low to high gain with zero input and adjust the input offset control until no shift occurs at the output when changing gains. Then adjust the output offset control for zero output at the lower gain.

Stable components (a metal film resistor and a cermet pot) should be used for the input offset adjustment to avoid compromising drift. Output offset adjustment components are not critical and may be omitted altogether when a single 2B54/2B55 is followed by an A to D Converter that has a zero adjustment.

Channel Selection

Each channel in the 2B54/2B55 is turned on and off by a SELECT input. As indicated in Figure 1, each SELECT input consists of an LED in series with a resistor, and is not connected to any other circuits in the module. Turning the LED on (I≥2.5mA) turns the channel on, and turning the LED off (I≤50μA) turns the channel off. This allows considerable flexibility of connection, but the easiest way to use the SELECT inputs is to tie all four SELECT + pins to +5V and drive the SELECT–inputs from TTL logic (either open-collector or totem-pole outputs can be used), as shown in Figure 2.

It is also possible to use CMOS logic to drive the SELECT inputs (Figure 5). With a +15V logic supply a standard CMOS decoder or gate can supply enough current to drive the SELECT inputs directly, but at lower supply voltages it is advisable to use a buffer such as that shown in Figure 5b. The power taken by the SELECT inputs is small, since only one is on at a time, but at the higher CMOS supply voltages more current than the required 2.5mA will flow. This does not affect operation, but if desired the current can be brought back to the minimum value with series resistors as shown in Figure 5. Use 2kΩ for 10V operation, and 3.9kΩ at 15V.

The maximum reverse voltage applied to any SELECT input must be limited to 3V to avoid damage to the LED. Maximum forward current should be kept below 25mA. Each SELECT input is isolated from all other circuits in the module and may be operated up to ±50V away from output and power ground.

Channels may be selected in any order, and there are no restrictions on rate or duty cycle except the 2.5ms settling time for access to a channel. It should be noted, however, that selecting two or more channels simultaneously for more than a few microseconds will result in a very long settling time when the conflict is resolved. Timing overlaps should therefore be avoided.

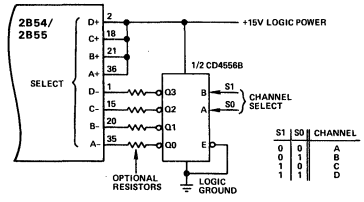


Figure 5a.

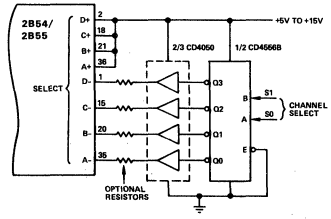


Figure 5b.

Figure 5. CMOS Channel Selection

Channel Expansion

The 2B54/2B55 has provision for directly interconnecting several modules when more than four channels are needed. The series-switched outputs of a group of modules are connected together, the SELECT inputs are driven in parallel, and the output of the desired module is selected using the Output Enable pin. This is shown in Figure 6. A single 74LS139 decoder is used to drive the SELECT inputs of up to four modules, and also provides address expansion so that the binary coded channel address word selects the appropriate module output via the Output Enable pins. The overall operation of the series-switched outputs is analogous to three-state logic, and the output rail is thus an analog bus.

It is possible to operate up to sixteen modules in parallel, for a total of 64 input channels. Note that it will be necessary to break up the SELECT inputs into several groups to avoid overloading the decoder when many modules are used. The settling time of the output switches is <50μs to ±0.01% and is thus negligible in comparison to the channel selection times.

The Output Enable signal is active low, and is compatible with both TTL and CMOS logic. The switching threshold is +1.8V; input current at 0V is typically -0.4mA.

The output resistance of the Switched Output (typically 35Ω +0.5%/°C) is low enough to provide fast switching times but will cause gain errors when driving a heavy load. A single buffer isolating the Switched Outputs from the load will solve this problem in an "analog bus" application (Figure 6). In single-module applications the DIRECT (low impedance) output should be used. Note that in all cases the SENSE pin *must* be connected to the DIRECT output to provide feedback for the output amplifier.

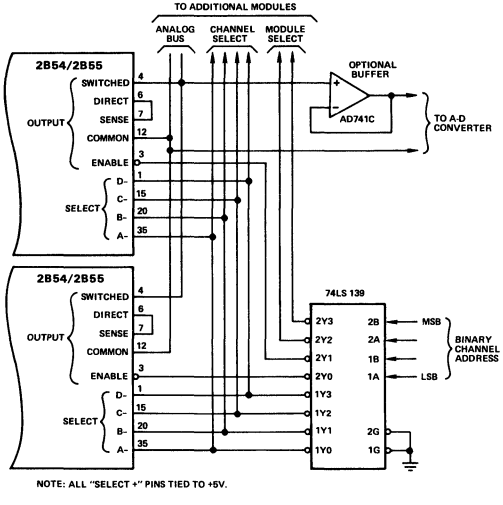


Figure 6. Expansion to More than Four Channels

Synchronization

In applications where multiple 2B54/2B55's are used in close proximity or when system clock signals are present near the isolator, differences in individual oscillator frequencies may cause "beat frequency" related output errors. To eliminate these errors, multiple units may be synchronized by connecting the SYNC OUT (pin 33) terminal to the SYNC IN (pin 32) terminal of the adjacent 2B54/2B55 (Figure 7). The first of a group of modules may be synchronized to an external source via the SYNC IN pin. To minimize noise pickup, sync wiring should be separated from analog signal runs.

The frequency of the external sync source, when used, will have a small effect on the gain and output offset of the 2B54/2B55. Thus any adjustments should be made with the module synchronized.

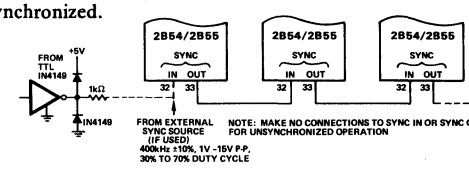


Figure 7. Synchronization

Open Input Detection

The 2B54 can be programmed to respond to an open-circuit condition on a channel input with either an upscale or downscale response when the affected channel is selected. The response time to detect an open input can be in the tens of seconds, since only a few nA of input bias current are available to charge the input filter. The circuits in Figure 8 indicate the selection of either downscale or upscale response and can be used to provide shorter open-circuit response times. Either circuit will produce a bias current of approximately 20nA which can be used to aid or oppose the 3nA typically supplied by the module, as shown. The circuit of Figure 8A has the advantage of simplicity, but the high-value resistor may not be readily available. Figure 8B shows how to solve the problem at the expense of complexity. The values shown may be modified to give an optimum trade of bias current for response time in a given application. A 2 to 5 second response is typical for the values shown.

If a downscale response is desired, a resistor divider circuit like Figure 8B may be desired to prevent a negative overscale. If a negative overscale condition occurs (typically -7V), the output will saturate on all channels.

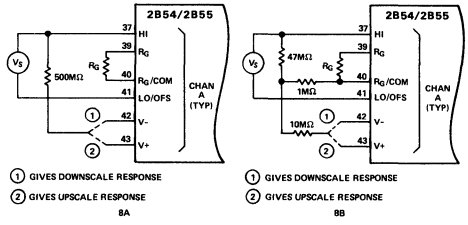


Figure 8. High Speed or Reversed Open Input Detection

Output Filtering

In most applications, no output filtering will be required since the effect of the small carrier-related noise spikes on the output (<1mV p-p, 100kHz B.W.) drops off rapidly as bandwidth decreases and in many cases will be negligible. In some applications (e.g., when driving a successive-approximation A to D) the effective system bandwidth may be large enough to pass the noise. To eliminate the carrier noise (without any effect on switching times), a simple R-C filter may be used at the output (Figure 9A). Only one filter is needed even when multiple modules are used, as shown in Figure 9B. If the load to be driven has an input resistance of less than 10MΩ, a buffer will be needed.

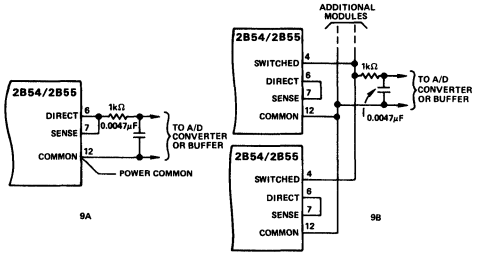


Figure 9. Output Filtering

CMR AND NMR PERFORMANCE

Common mode rejection is a result of both isolation and filtering and indicates ability to reject common mode inputs while amplifying differential signal inputs. CMR is dependent on source impedance imbalance, signal frequency and conditioner gain.

Normal mode rejection is also a function of the 2B54/2B55 gain. Figures 10 and 11 illustrate typical CMR and NMR performance. Note that any additional low pass filtering (e.g., an integrating A to D converter) at the output of the 2B54/2B55 will further improve both CMR and NMR performance.

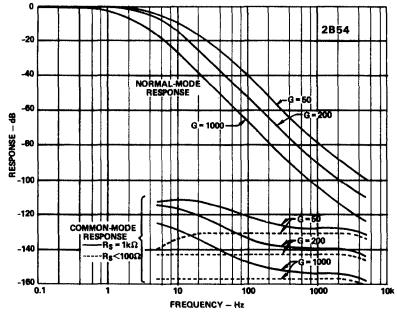


Figure 10. Common Mode and Normal Mode Response – 2B54

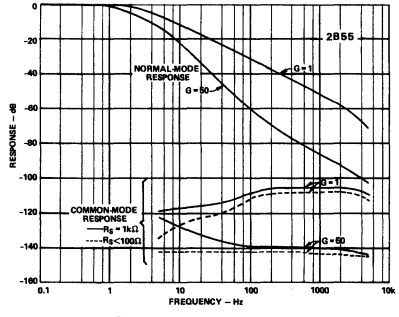


Figure 11. Common Mode and Normal Mode Response – 2B55

APPLICATIONS

Thermocouple Temperature Measurement: Figure 12 shows a four-channel thermocouple input system with isolation, amplification, and multiplexing provided by the 2B54. Several different thermocouple types are used, and the gain-setting resistors on each channel have been chosen to take the standard ANSI range for each type to a 5V output span. Since thermocouples must be compensated for the temperature of the reference junction which is formed where the thermocouple leads are terminated, the 2B56 Universal Cold Junction Compensator is used. The 2B56 monitors the temperature of the reference junction (terminal block) via an external sensor and corrects the signal at the output of the 2B54 for reference temperature. Compensation for several thermocouple types is selectable via digital control inputs. Thermocouple linearization, if needed, would be typically performed in system's software.

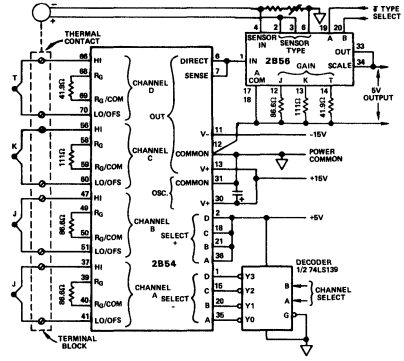


Figure 12. Four-Channel Thermocouple Temperature Measurement with Cold Junction Compensation

Process Signals Interface: In Figure 13, the 2B55 is used to provide floating inputs for four 4-20mA process signal loops. The use of floating inputs in this type of application gives protection from common-mode voltages and greatly simplifies system configuration, since additional loads in series with the loop can be connected on either side of the isolator input.

Each current input is converted into a 1 to 5 volt signal by a 250Ω resistor. The 2B55 is operated at unity gain (no gain-setting resistors) so that a 1 to 5 volt signal appears at the output. Since no gain-setting resistors are used, gain adjustment, if required, is done by connecting trims directly across the input resistors. Other current ranges can be accommodated by changing the value of the input resistors.

When there are several loads on the loop, compliance voltage at the transmitter may be at a premium. In this case it will be advantageous to reduce the voltage swing at the isolator inputs by using smaller resistors (perhaps 25Ω) and scaling the output back to a 5V span by taking an appropriate gain in the isolator.

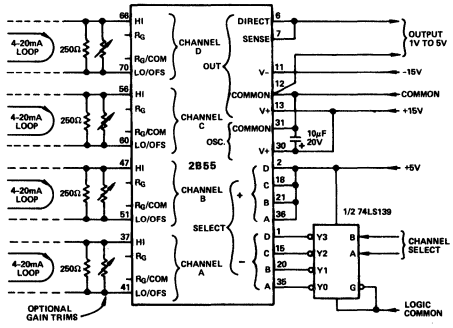


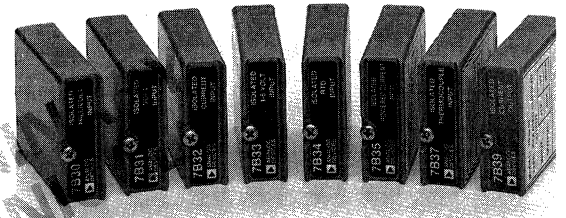
Figure 13. Isolated 4–20mA Loop Signals Interface

Low Cost, Modular Process Control Signal Conditioners

7B Series

FEATURES

- **Accepts Process Control Input Signals: Thermocouples, RTDs, Current, Millivolt and Voltage Inputs**
- **Powered Current Input Provides Isolated +24 V for a Transmitter**
- **Analog Current Output Module**
- **Complete Signal Conditioning Function: 120 V RMS Field Wiring Protection, Filtering, Amplification, 1500 V RMS Transformer Based Isolation**
- **Operates From +14 V DC to +35 V DC Power**
- **Factory Calibrated Accuracy**
- **Mix and Match Modularity**



GENERAL DESCRIPTION

The 7B Series of signal conditioners represents a new level of price versus performance for the process control industry. These modular, plug-in conditioners accept inputs from the most common process control transducers and signals and provide a high level isolated output voltage. Galvanic isolation of 1500 volts rms is achieved by transformer based circuitry. Both the signal path and the power supply are isolated enabling true channel-to-channel isolation.

The modules accept a nominal power supply input of +24 volts dc with a range of +14 volts to +35 volts. The small size of 1.7″ × 2.1″ × 0.60″ allows large point count applications without taking up a lot of space. All specifications are valid over −40°C to +85°C.

Isolated input modules are available for J, K, T, E, R, S and B thermocouples; platinum RTDs; and current, voltage and millivolt signals. The isolated powered loop input module provides +24 volts for a transmitter and accepts a 4–20 mA current input. All input modules provide a high level 1–5 volt output signal, with additional output ranges available. An isolated current output module provides a 0–20 mA or 4–20 mA signal to the field for control applications. A compact sensor for cold junction compensation reduces the space required on the backplane.

A variety of backplanes are available to provide a complete solution for the end user or systems integrator. Each backplane contains screw terminals for the field wiring connections. A cold junction compensation thermistor is installed under the terminal blocks on each channel. Only the thermocouple input module receives this input signal. This flexibility allows any module type, input or output, to be used in any channel on the backplane. A 25-pin D style connector is used for system hookup. Provisions are made for redundant power connections as well as an LED to indicate power on. Nineteen-inch rack mount kits are available.

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APPLICATIONS

The 7B Series of signal conditioners is designed to provide an easy and cost effective solution to interfacing to transducers in process monitoring and control systems. These modules can be designed into a system as a component or used with Analog Devices' backplanes to provide a higher level solution. The +24 volt power supply requirement and a simple pinout eases the integration of the 7B Series into a user designed backplane. Applications requiring monitoring and control of large numbers of analog signals are a perfect fit for the 7B Series.

7B Series—SPECIFICATIONS

Input Modules (All specifications are at +25°C, +24 V power.)

Model	7B30/7B31	7B32	7B33	7B34	7B35	7B37
Input Ranges	DC mV/DC V	Current	dc V	RTD	Current	Thermocouples
Output Ranges	1–5 V, 0–10 V	1–5 V, 2–10 V	1–5 V, 2–10 V	*	1–5 V, 2–10 V	*
Accuracy[1]	±0.1% Span max	*	*	±0.13%–±0.25% Span max[2]	*	±0.10% Span max[2]
Nonlinearity	±0.02% max	*	*	±0.05% Span Conformance	*	*
Stability vs. Ambient Temperature						
Span	±35 ppm/°C ±55 ppm/°C	±35 ppm/°C	±15 ppm/°C	±60 ppm/°C	±40 ppm/°C	±35 ppm/°C
Output Offset	±0.002% Span/°C	*	*	*	*	*
Input Offset	1 μV/°C	*	NA	*	NA	*
CMV, Input to Output	1500 V RMS Continuous	*	*	*	*	*
CMR @ 50 or 60 Hz,						
1 kΩ, Source Unbalance	160 dB/120 dB	105 dB min	105 dB min	160 dB min	105 dB	160 dB
NMR @ 60 Hz	60 dB	NA	NA	*	NA	*
NMR @ 50 Hz	56 dB	NA	NA	*	NA	*
Input Protection, Continuous	120 V AC Continuous	*	*	*	*	*
Voltage Output Protection	Continuous Short to Gnd	*	*	*	*	*
Input Transient Protection	Meets IEEE-STD472	*	*	*	*	*
Input Resistance	10 MΩ/100 kΩ	200 Ω	2 MΩ	NA	NA	10 MΩ
Bandwidth	3 Hz	100 Hz	100 Hz	3 Hz	100 Hz	3 Hz
Response Time, 0 to 90%	200 ms	10 ms	10 ms	500 ms	10 ms	200 ms
Minimum Output Voltage	−1.2 V[3]/−30 V[4]	*	*	*	*	*
Maximum Output Voltage	+7.4 V[3]/+13.5 V[4]	*	*	*	*	*
Open Input Response	NA	Downscale	Downscale	Upscale	Downscale	Upscale
Open Input Detection Time	NA	2 s max	2 s max	10 s max	2 s max	10 s max
Power Supply	+14 V to +35 V	*	*	*	+18 V to +30 V	*
Power Supply Sensitivity	±0.01% Span/V	*	*	*	±0.025% Span/°C	*
Power Consumption	25 mA	*	*	*	60 mA max	*
Size (H)(W)(D)	2.13″×1.705″×0.605″, max	*	*	*	*	
Environmental						
Rated Temperature Range	−40°C to +85°C	*	*	*	*	*
Operating Temperature Range	−40°C to +85°C	*	*	*	*	*
Storage Temperature Range	−40°C to +85°C	*	*	*	*	*
Relative Humidity	0 to 90%, Noncondensing	*	*	*	*	*

NOTES
[1]Accuracy specification includes the combined effects of repeatability, hysteresis and linearity and does not include sensor or signal source error.
[2]Accuracy specification is dependent on input range, consult factory.
[3]1–5 V output.
[4]0–10 V output.

*Specifications same as 7B30.

Specifications subject to change without notice.

Table I. Input Selection

Input Type / Span	Output	Model
VOLTAGE		
mV DC: 0–10 mV, ±10 mV, ±100 mV, 0–100 mV	1–5 V, 0–10 V	7B30
V DC: 0–1 V, 0–5 V, 1–5 V	1–5 V, 0–10 V	7B30
V DC: 0–10 V, ±10 V, ±5 V	1–5 V, 0–10 V	7B31
V: 1–5 V	1–5 V	7B33
PROCESS CURRENT		
4–20 mA	1–5 V	7B32
4–20 mA, External 250 Ω Resistor	1–5 V	7B33
0–20 mA dc/4–20 mA dc, External 250 Ω Resistor	1–5 V, 0–10 V	7B31
4–20 mA Powered Loop Current	1–5 V	7B35
RTDs		
100 Ω Pt	1–5 V, 0–10 V	7B34
THERMOCOUPLES		
J, K, T, E, R, S, B	1–5 V, 0–10 V	7B37

PIN DESIGNATIONS

I/O & POWER COM	5
V_{OUT}	4
+24 VOLTS	3
INPUT LOW	2
INPUT HIGH	1
SENSOR	0

NOTE
Pin 0 is only used on the 7B34 the 7B34 RTD Input and the 7B37 Thermocouple Input Modules.

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

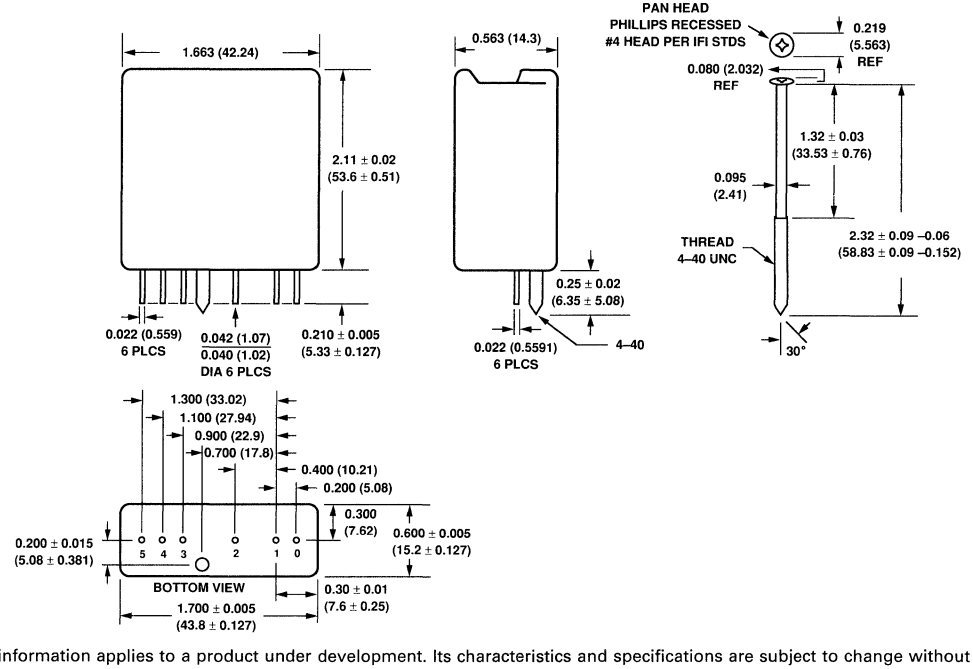
Output Module (All specifications are at +25°C, +24 V power.)

Model	7B39
Input Range	1–5 V, 0–10 V
Output Range	4–20 mA, 0–20 mA
Load Resistance Range	0 to 850 Ω
Accuracy[1]	±0.1% max
Nonlinearity	±0.02% max
Stability vs. Ambient Temperature	±0.01%/°C
CMV, Input To Output	1500 V RMS Continuous
Output Protection	120 V RMS Continuous
Output Transient Protection	Meets IEEE-STD472 (SWC)
Input Resistance	10 MΩ
Response Time 0 to 90%	10 ms
Output Range	
Minimum Output Current	0 mA
Maximum Output Current	32 mA
Bandwidth	100 Hz
Power Supply	+14 V dc to +35 V dc
Power Supply Sensitivity	±0.012%/V
Power Consumption	65 mA
Size	2.13″×1.705″×0.605″ max
Environmental	
Rated Temperature Range	−40°C to +85°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +85°C
Relative Humidity	0 to 90% Noncondensing

NOTES
[1]Accuracy specification includes the combined effects of repeatability, hysteresis and linearity. Does not include signal source error.
Specifications subject to change without notice.

7B SERIES MODULE OUTLINE

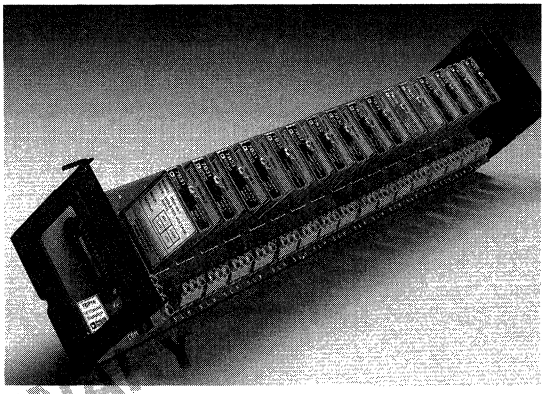
Dimensions shown in inches and (mm).



This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

SYSTEM DESIGN FEATURES

- **Power Supply Range of +14 Volts to +35 Volts**
- **Single Threaded Insert for Module Hold Down**
- **Accepts Thermistor for Cold Junction Compensation**



SYSTEM DESIGN INFORMATION

The 7B Series was designed to be easily integrated into a process control system. The pins and the hold down screw fit into the same sockets as those used with solid-state relays. The thermistor recommended for cold junction compensation is commercially available. The pins are 0.022″ in diameter and 0.210″ extending from the bottom of the case. The millivolt, volt and current input modules and the current output module have five pins and the thermocouple and RTD modules have six pins each. The RTD module requires three field wiring connections, all others need two.

BASIC DESIGN GUIDELINES

Modules may be mounted in any position and will normally be placed next to the screw terminals connecting to the associated field wiring. The temperature sensor is used only by the thermocouple modules; but if it is installed in each channel, then modules can be inserted in any channel depending upon the application. The operation of the non-thermocouple modules is not affected by the temperature sensor. This sensor must be physically close to the terminals where the thermocouple wire connects to copper. Because the low power dissipation of the 7B Series modules minimizes temperature gradients on the backplane, no special precautions are needed to get accurate temperature sensing.

Provisions must be made for a current sense resistor if there are current inputs and the 7B32 with the internal sense resistor is not being used. The screw terminals for the field wiring connections are large enough for a resistor to be connected directly on the terminals. Provisions can also be made to use the pluggable current sense resistor offered as an accessory.

The width of the modules permits installation on 0.625″ centers where required, but consideration must be given in each application to the required distance between backplane conductors where large interchannel voltages exist or code requirements apply. The isolation specification may be downrated due to the module spacings.

MODULE DESCRIPTIONS

7B30 and 7B31: Isolated Millivolt and Voltage Input

The 7B30 and 7B31 accept millivolt and volt signals, respectively. They each provide an isolated +1 to +5 volt or 0 to +10 volt output signal. Both modules have standard ranges from ±10 mV up to ±10 V. The 7B31 can be used with a current sense resistor to provide a 0 to +10 volt output. These modules have a 3 Hz bandwidth.

Figure 1 shows a block diagram of the 7B30/7B31. The high and low input terminals are protected for up to 120 V rms. The high level signals of the 7B31 are attenuated and both modules have a one pole low pass filter on the input. A low drift amplifier provides the gain of the module. The signal is modulated and passed across a transformer supplying 1500 volts of isolation. The signal is then demodulated so the original signal is recovered. The two pole output filter and buffer ensure a clean low noise signal on the output. The power supply section of the module is also isolated allowing channel-to-channel isolation.

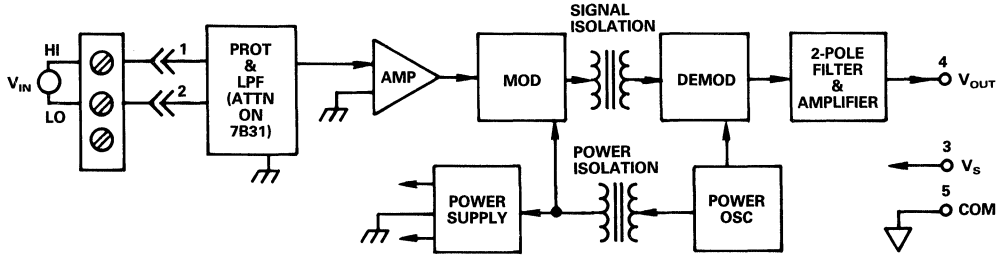


Figure 1. 7B30/7B31 Block Diagram

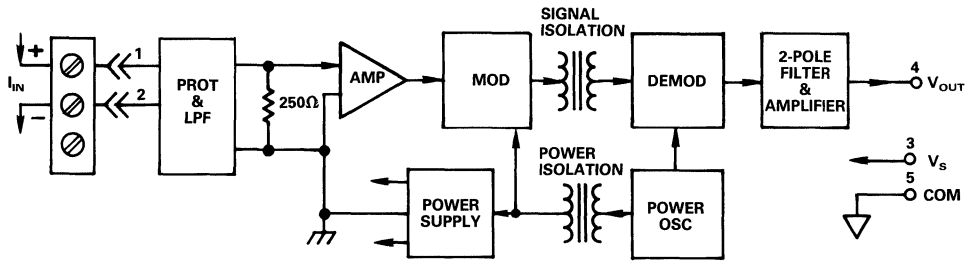


Figure 2. 7B32 Block Diagram

7B32: Isolated Current Input

The 7B32 accepts a 4–20 mA current input and provides a +1 to +5 volt output. The 7B32 incorporates an internal protected current conversion resistor allowing the process current to be directly connected to the module without compromising system integrity. The internal resistor allows the module calibration to include the current sense resistor. Downscale open input detection and a bandwidth of 100 Hz is featured.

Figure 2 is a functional block diagram of the 7B32. The module features input protection of 120 V rms in addition to a low pass filter on the input. The input current is converted to a voltage signal and then modulated to pass across the transformer barrier. The isolated signal is then demodulated and buffered and filtered to provide a clean output voltage proportional to the input current.

The 7B32 is available with a +1 to +5 volt output. If a current input module with a 0 to +10 volt output is desired, a standard 7B31 with a +1 to + 5 volt input and a 250 Ω current conversion resistor can be used. In applications where an external current sense resistor is preferred, the 7B33 voltage input module and the current sense resistor can be used to allow a +1 to +5 volt output.

7B33: Isolated High Level Voltage Input

The 7B33 accepts a +1 to +5 volt input signal and provides a +1 to +5 volt output with a signal bandwidth of 100 Hz.

Figure 3 is a functional block diagram of the 7B33. The two input terminals are protected for the hookup of 120 V rms. A 2.2 MΩ resistor on the input provides downscale open input detection within 2 seconds of a break on the input. A low pass filter combined with a low drift amplifier insure a clean signal into the modulator stage. The signal is modulated and passed across the transformer to provide 1500 V rms common mode isolation. The signal is recovered by the demodulator and fed through a 2-pole filter and buffered to provide a clean, low impedance output signal.

The +24 volt power input to the 7B33 provides power for the output stage and is passed across a second transformer in order to provide isolated power for the input circuitry. This ensures channel-to-channel isolation of the modules.

The 7B33 is available with a +1 to +5 volt input and a +1 to +5 volt output, this module has no provisions for gain or attenuation. The 7B30 and 7B31 mV and V input modules should be used for different input or output ranges.

The 7B33 can be used with a 250 Ω resistor as a current input module. This external current sense resistor allows the current loop to be maintained if the module has to be removed.

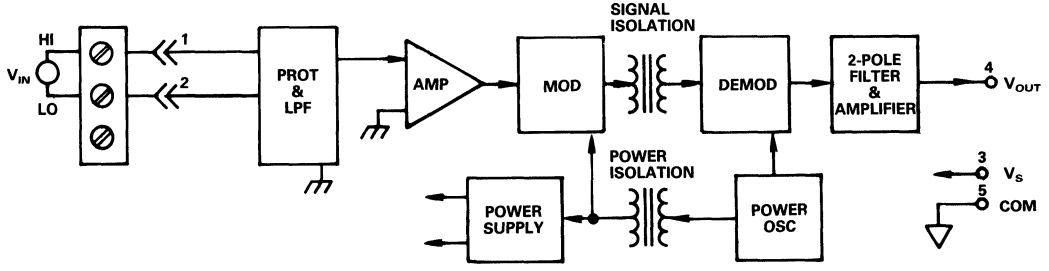


Figure 3. 7B33 Block Diagram

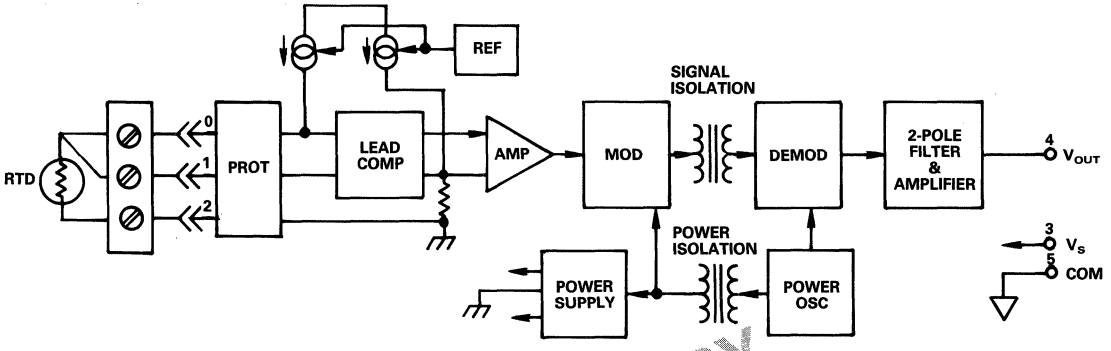


Figure 4. 7B34 Functional Block Diagram

7B34: Isolated Linearized RTD Input

The 7B34 accepts inputs from 100 Ω platinum RTDs and provides a linear voltage output. The 7B34 is available with a +1 to +5 volt or a 0 to +10 volt output range, all ranges feature a 3 Hz bandwidth. Three wire lead compensation is provided, and 2, 3 or 4 wire RTDs may be used. Upscale open input protection is provided on the signal leads.

Figure 4 is a functional block diagram of the 7B34. The 7B34 uses three pins for the RTD input, two for the sensor and a third for the excitation. All three input terminals are protected for up to 120 V rms. Low drift sensor excitation current of 0.25 mA is provided for platinum RTDs. A current source identical to the excitation current source is connected to the third lead of the RTD to cancel the effects of lead resistance. This current also flows through Rz, chosen to represent the RTD value of the zero output to voltage of the module. This signal is then amplified and modulated to be passed across the isolation barrier. The original signal is recovered in the demodulator stage. A two pole filter and a buffer ensure a clean low noise output voltage is provided.

The +24 volt power is also isolated by transformer coupling to provide channel-to-channel isolation and signal to power isolation. The 7B34 will accept power supply inputs from +14 volts to +35 volts.

7B35: Isolated Powered Current Loop Input

The 7B35 accepts a 4–20 mA current input and provides the loop power for a transmitter. This module features downscale open input detection and a bandwidth of 100 Hz. The module incorporates a protected 200 Ω current sense resistor eliminating the need for external resistors. A +1 to +5 volt output range is standard.

The functional block diagram is shown in Figure 5. The two input terminals are protected for 120 V rms. A one-pole input filter eliminates high frequency noise. A 200 Ω current conversion resistor converts the signal to a voltage to be amplified. The signal is then modulated and passed across the galvanic isolation of the transformer to provide 1500 volts of common mode isolation. The demodulator reclaims the original signal, which is filtered and buffered to give a clean, low noise output voltage.

The power supply for the module is also isolated and the module will accept power inputs from +18 volts to +30 volts.

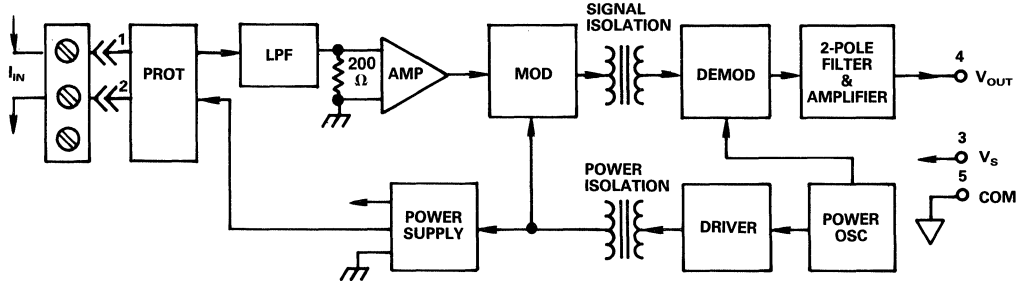


Figure 5. 7B35 Functional Block Diagram

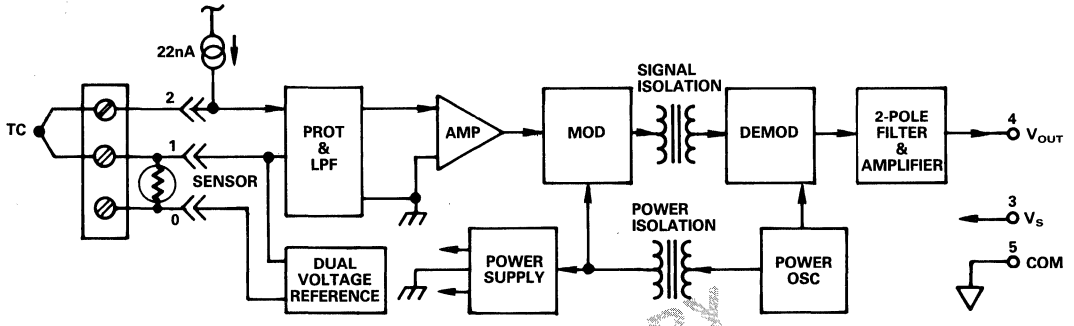


Figure 6. 7B37 Block Diagram

7B37: Isolated Thermocouple Input

The 7B37 accepts inputs from J, K, T, E, R, S and B type thermocouples and provides a nonlinearized +1 to +5 volt or 0 to +10 volt output. Upscale open thermocouple detection is featured within 10 seconds of a break in in the thermocouple wiring. This module is designed to accept cold junction compensation from a thermistor mounted on the backplane adjacent to the field wiring terminals. There are standard ranges available for each thermocouple type.

Figure 6 is a functional block diagram of the 7B37. In order to accommodate the CJC input, the 7B37 uses three input pins. Cold junction compensation circuitry corrects for the effects of connecting the thermocouple wires to the screw terminals on the backplane. Upscale open input detection is provided through the 22 nA current source. The input terminals are protected for the inadvertent connection of 120 V rms. A one-pole low pass filter on the input rejects high frequency noise. The input signal is offset to set the zero scale input value. A low drift amplifier provides a stable signal into the modulator; 1500 volt signal isolation is provided by transformer coupling. A demodulator on the output side recovers the original, which is buffered and filtered to provide a clean output signal.

7B39: Isolated Current Output

This module accepts a +1 to +5 volt or 0 to +10 volt input from the user's system and provides a galvanically isolated 4–20 mA or 0–20 mA current output to the field wiring capable of driving a 750 Ω load at +24 volt power. The bandwidth is 100 Hz.

The functional block diagram is shown in Figure 7. The module accepts its input signal from the user's system, typically a D/A. The signal is buffered and then modulated to be passed across the transformer isolation barrier. After the signal is demodulated, it is converted to an output current. The output current loop is floating. The output terminals are protected even if a 120 V rms signal is connected.

A single +24 volt power supply drives the module's power transformer and the clock oscillator. The power is isolated from the input signal.

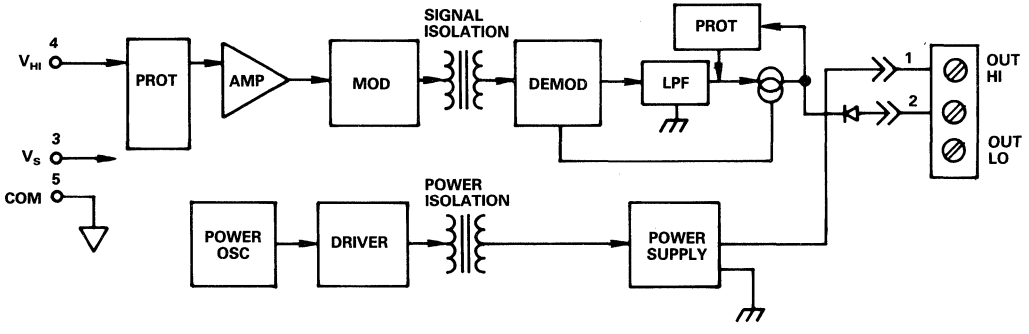


Figure 7. 7B39 Functional Block Diagram

BACKPLANE FUNCTIONAL DESCRIPTION

The 7B Series includes a variety of backplanes to address end user and evaluation needs. Backplanes are available in 16-, 8- and 4-channel sizes. The 16- and 8-channel backplanes can be mounted in a 19″ by 3.5″ panel space. The 4-channel backplane is ideal for evaluation purposes or small point count applications.

Each backplane channel has three screw terminals for field connections. The field connections accept transducer or signal inputs and provide excitation and current outputs when needed. A cold junction compensation sensor is mounted underneath the screw terminal block on each channel to accommodate thermocouple modules. Each I/O channel has six pin sockets to ensure interchangeability of the modules. A standard D type 25-pin connector is used for system interface on the 16-channel backplane. The connector provides 16 single ended input and/or output signals.

All 7B Series backplanes have three power supply connections. The modules can accept power supply levels from +14 to +35 volts. Two connections are used for a primary +24 volt power input and a backup power supply. A series diode is used to sense the power supply. If one supply fails, the other supply can take over. The diode also provides reverse power connection protection. The third power connection can be used for a +15 volt power supply since there is no diode drop in the line to affect the power supply level. A LED on each backplane indicates the power status.

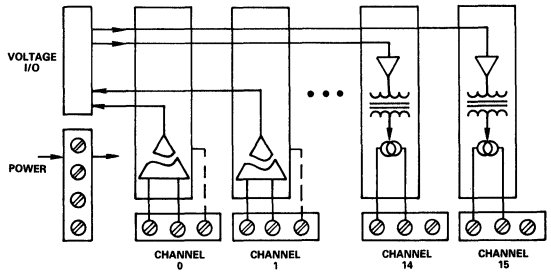


Figure 8. 7BP16 Block Diagram

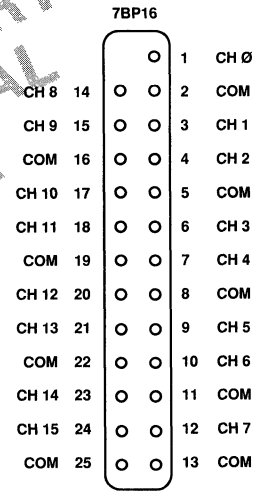


Figure 9. System Connection Pinout (Bottom View)

BACKPLANE SPECIFICATIONS

	7BP16	7BP08	7BP04
Channels	16	8	4
External Power Requirement	+14 V to +35 V	*	*
Cold Junction Sensor	On Each Channel	*	*
Size	3.5″ × 17.4″ (88.9×441.96 mm)	3.5″ × 10″ (88.9×254 mm)	3.5″ × 6″ (88.9×152.4 mm)

*Specifications same as 7BP16

ACCESSORIES

To facilitate system design with the 7B Series the following accessories are available:

Current Conversion Resistor. This encapsulated, precision 250 Ω resistor can be used with the 7B33 Isolated Voltage Input Module to convert a 4–20 mA current input to the 1–5 volt input for the module.

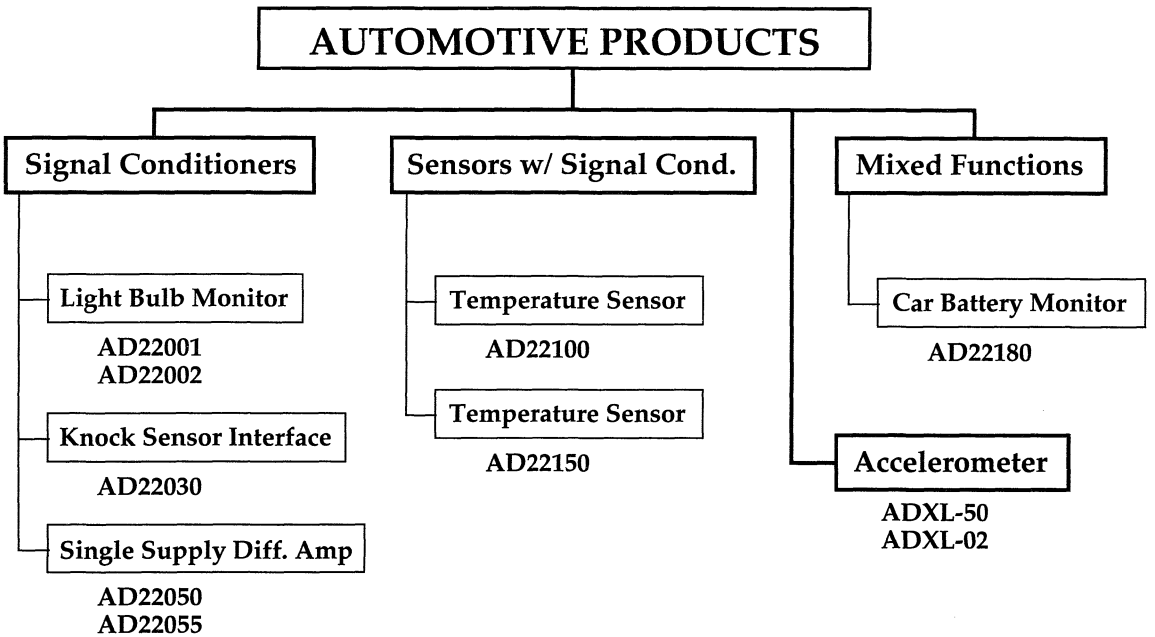
Rack Mount. A single piece metal chassis for mounting a 7B Series backplane in a 19″ rack. Model number AC1363.

Cables. A 2 foot cable with a 25-pin D type connector and a 26-pin connector is available to connect the 7B Series backplane to systems compatible with the 3B and 5B Series families.

User's Manual. A complete manual is available to instruct the user on how to design and install systems using the 7B Series.

Automotive Components
Contents

Selection Tree
Automotive Components



Selection Guide
Automotive Components

Model	Description	Package Options[1]	Temp Range[2]	Page
*AD22001	5-Channel Monolithic Comparator for Lamp Monitoring	2	−40°C to +125°C	11-5
*AD22050	Single-Supply Sensor Interface Circuit	2	−40°C to +125°C	11-6
*AD22100	Monolithic Temperature Sensor with Signal Conditioning	2, 7, 11	−50°C to +150°C	11-7
*AD22150	Monolithic Hall Effect Sensor with Signal Conditioning	11	−40°C to +150°C	11-8
*AD22180	Battery Monitor Circuit	2, 11	−55°C to +125°C	11-8
*AD22181	Alternator Control Circuit	7	−55°C to +125°C	11-9
*ADXL50	Monolithic Accelerometer with Signal Conditioning (50 g Version)	1, 7	−55°C to +125°C	7-27; 11-10
*AD22002	9-Channel Lamp Monitor	2	−40°C to +125°C	11-5
*AD22030	Monolithic, Dual Input Knock Sensor Interface Circuit	5	−40°C to +85°C	11-6
*AD22055	Resistor Bridge Amplifier, Gain = 400	6	−40°C to +150°C	11-6
*ADXL02	Monolithic Accelerometer with Signal Conditioning (2 g Version)	1, 7	−55°C to +125°C	11-9

[1]Package Options: 1 = Hermetic DIP, Ceramic or Metal; 2 = Plastic or Epoxy Sealed DIP; 3 = Cerdip; 4 = Ceramic Leadless Chip Carrier; 5 = Plastic Leaded Chip Carrier; 6 = Small Outline "SOIC" Package; 7 = Hermetic Metal Can; 8 = Hermetic Metal Can DIP; 9 = Ceramic Flatpack; 10 = Plastic Quad Flatpack, 11 = Single-in-Line "SIP" Package; 12 = Ceramic Leaded Chip Carrier; 13 = Nonhermetic Ceramic/Glass DIP; 14 = J-Leaded Ceramic Package; 15 = Ceramic Pin Grid Array; 16 = TO-92; 17 = Plastic Pin Grid Array.
[2]Temperature Ranges: C = Commercial, 0°C to +70°C; I = Industrial, −40°C to +85°C (Some older products −25°C to +85°C); M = Military, −55°C to +125°C.
Boldface Type: Product recommended for new design.
*New product.

Orientation
Automotive Components

Analog Devices provides advanced semiconductor-based solutions for automotive measurement applications to make high performance systems affordable to the end user.

This section contains solid-state sensors and sensor signal conditioners designed specifically for automotive applications. The solid-state sensors integrate one or more sensors with signal conditioning circuitry and a complete output interface onto a single monolithic IC. The ability of many products to work from typical automotive voltage supplies over wide temperature ranges, together with the benefits of advanced signal conditioning, make the products inherently user friendly.

The devices in this section represent several years of product development in a cooperative effort with major customers in the automotive industry. While ideally suited for automotive applications, many of the products are attractive for nonautomotive applications as well. All products are available as described and in modified versions for custom volume applications.

SOLID-STATE SENSOR PRODUCT CONCEPT

In order to achieve significant improvement in automotive sensors, Analog Devices utilizes its knowledge and expertise in process technology, signal conditioning circuitry, and laser trimmable on-chip thin-film resistors. This allows the sensor and signal conditioning circuitry to be brought onto one and the same IC resulting in the following benefits:

1. *Higher signal resolution* is achieved by combining the sensor and signal conditioner to get a high level output (for example linear 0 V to 5 V) which can be transferred with high noise immunity to the microcontroller.

   This is an improvement over traditional (often inactive operating) sensors which transfer low level outputs (for example 100 mV) across long transfer lines between the sensor and microcontroller with significant loss of resolution.

2. *Increased accuracy and linearity* are attained by using on-chip smart compensation circuitry, linear signal processing and laser trimmable on-chip thin-film resistors to compensate for all major sensor errors and unwanted drifts over temperature and time.

3. *Standard signal interfaces* include voltage (for example 0 V to 5 V), current, or digital signal outputs. This increases the possibility of sharing the solid-state sensor with more than one controller unit.

AUTOMOTIVE POWER SUPPLY CONSIDERATIONS

Many of Analog Devices' solid-state sensors are designed to operate directly from the car battery, and thus withstand the inherent harsh conditions present from an unregulated and unprotected power supply. Other members of the sensor family are designed to use the existing +5 V regulated power supply from the microcontroller PC board.

The car battery voltage, nominally +12 V, is a dc voltage which varies between +8.5 V and +14.6 V during normal operating conditions. However, in some cases, the battery voltage can drop far below +8.5 V (for example, during engine start in winter) or can go above +14.6 V (for example, when the alternator charge controller fails). Many systems must remain operative even under these harsh conditions, and all systems should remain undamaged.

Other circuit protections which Analog Devices considers when designing automotive components are:
- reversed power supply (incorrectly installed battery)
- double battery voltage (jump start)
- voltage transients in the range of ±60 V to beyond ±100 V
- load dump
- EMI (electromagnetic interference)

OPERATING TEMPERATURE RANGE

Automotive sensors must operate over a wide temperature range. Typical requirement include:

Passenger Compartment The minimum temperature rises above 0°C almost immediately after the car has been started.	−40°C to +85°C
Engine Compartment Temperatures may exceed 150°C or even 180°C depending on ventilation.	−40°C to +125°C
Trunk and Chassis	−40°C to +110°C
Brake Systems This may extend to +250°C depending on location and ventilation.	−40°C to +180°C

All of the devices in this section meet the temperature range of −40°C to +125°C. Many of the products extend to +150°C, and Analog Devices is continuing developments to increase the temperature range to +180°C and beyond.

FUTURE DEVELOPMENTS

Analog Devices is continuing to develop new solid-state sensors and signal conditioning circuits, both general purpose and application specific (ASIC) to be used in applications such as: Local Area network, single point torque sensing, contactless angle positioning sensing and multiaxis motion detection. We will continue to seek direction from key automotive system designers to develop and produce products that will enhance the next generation of automobiles.

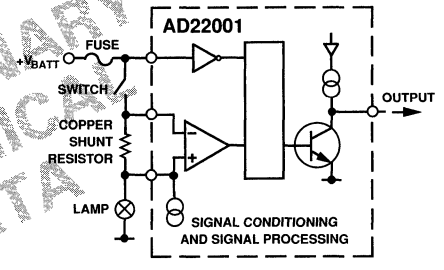
AD22001* – 5-Channel Monolithic Comparator for Lamp Monitoring

FEATURES
Continuous Status Checks of Five Bulbs
Lamp Status Check In "On" and "Off" State
Status Checks of Two In-Line Fuses
Very Low Voltage Drop at Sensor Shunt Resistor (Comparator Threshold 1.75 mV at 22°C)
Temperature and Supply Voltage Compensated
Powered Directly from Car Battery: Protection Included for Transient, Reverse Supply, Load Dump
Operating Temperature Range: −40°C to +125°C
15 V CMOS Compatible Digital Output Signals
Voltage Limited Power Supply Output for 15 V CMOS Logic ICs

The AD22001 is a monolithic, five channel comparator circuit for monitoring the functionality of lamps in automotive applications.

The IC tests the series circuit leading to the lamp to determine if the circuit is intact and a functional lamp is in the socket. The AD22001 continuously checks the functionality of up to five bulbs in either their "on" or "off" state, and also tests for the presence of an in-line fuse in two of the series circuits.

Digital outputs indicate the status of each channel. Additionally, the AD22001 provides a voltage limited power supply output to supply 15 V CMOS circuits that may interface to the AD22001.



Typical Application Circuit for a Single Channel Lamp Monitor

Patents pending.

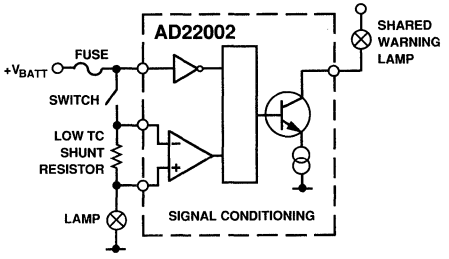
AD22002* – 9-Channel Monolithic Comparator for Lamp Monitoring

FEATURES
Continuous Status Checks of Nine Bulbs
Status Checks of Five In-Line Fuses
Very Low Voltage Drop at Sensor Shunt Resistor (Comparator Threshold 5 mV at 22°C)
Includes "Memory" Function for Brake Light Applications
Current-Limited Warning-Lamp Driver
Under- and Overvoltage Shut-Down Protection
User Configuable Error-Allowable and Interruption Times
Threshold Voltage Power Supply Compensated
Powered Directly from Car Battery: Protection Included for Transients, Reverse Supply, Load Dump
Operating Temperature Range: −40°C to +125°C

The AD22002 is a monolithic, nine channel comparator circuit for monitoring the functionality of lamps in automotive applications.

Each comparator tests whether the circuit to the lamp is complete and intact, and determines the functionality of the bulb in the socket. The status of five in-line fuses is also checked.

Faults can be tolerated for a user-definable time before the output is brought low to drive a warning light.



Typical Application Circuit for One Channel of Lamp Monitoring

Patents pending.

AD22030 – Monolithic, Dual Input Knock-Sensor Interface Circuit

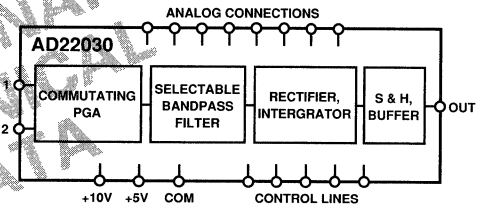
FEATURES
Combines Channel Selection, Gain Control, Filtering, Rectifying, Integrating and Buffering Functions on One Chip
Gain Is Programmable to 1, 2, 4, 8 and 16
User Definable Filter Bandwidth and Center Frequency
Filter Tunable to Different Frequencies for Channels 1 and 2
Rectifier and Output Reset Between Cylinder Firings
Accepts Knock-Sensor Signals Directly
Output Is Compatible with A-to-D Converter Inputs
Operating Temperature Range Is −40°C to +85°C
Operates from +10 V, +5 V and Common

The AD22030 is a monolithic, dual channel interface circuit for automotive engine knock sensors.

It has inputs for the signals from two sensors, and commutates between them. These are amplified in turn by a PGA, and then bandpass filtered, rectified and averaged to extract the information of interest. This signal is then buffered by a sample-and-hold function, the result being a direct indication of the knock intensity.

No external active devices are required to derive this signal, while the center frequency and bandwidth of the filter are both user-definable by passive components.

The AD22030 can easily be used to process the signal from a single knock sensor.



Functional Block Diagram

AD22050* – Single-Supply Sensor Interface Circuit

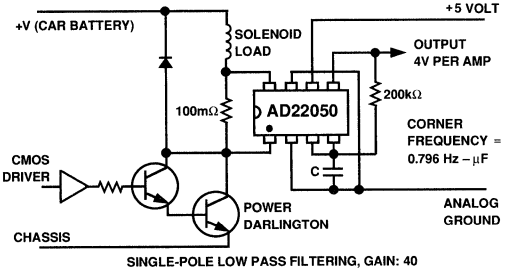
FEATURES
Gain of ×20 Alterable from ×1 to ×160
Input CMR from Ground to 6× (V_S −1 V)
Output Span 10 mV to (V_S −0.2) V
1-, 2-, 3-Pole Low-Pass Filtering Capabilities
Accurate Midscale Offset Capability
Differential Input Resistance 400 kΩ
Drives 1 kΩ Load to +4 V Using V_S = +5 V
Transient Spike Protection & RFI Filters Included
Operating Temperate Range −40°C to +125°C

APPLICATIONS
Current Sensing
Motor Control
Interface for Pressure Transducers, Position Indicators, Strain Gages, and Other Low Level Signal Sources

The AD22050 is a single supply difference amplifier for amplifying and low-pass filtering small differential voltages (typically 200 mV FS at a gain of 20) from sources having a large common-mode voltage.

While the circuit is optimized for +5 V, supply voltages between +3.0 V and +36 V can be used. The input common-mode range extends from ground to over +24 V using a +5 V supply with excellent rejection of this common-mode voltage. This is achieved by the use of a special resistive attenuator at the input, laser trimmed to a very high differential balance at both dc and high frequencies.

Provisions are included for optional low-pass filtering and gain adjustments. An accurate mid-scale offset feature allows bipolar signals to be amplified.



Typical Application Circuit for a Current Sensor Interface

*Patents pending.

AD22055* – Single-Supply Bridge Transducer Amplifier

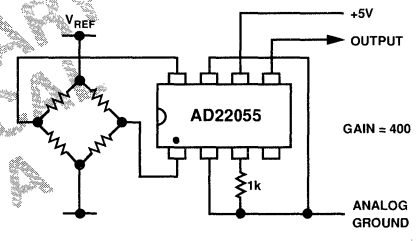
FEATURES
Gain of 400. Alterable from 40 to 1000
Output Span: 20 mV to (V_S–0.25) V
One Pole Low-Pass Filtering Available
Offset Capability
Differential Input Resistance: 230 kΩ
Drives 1 kΩ Load to +4 V Using V_S = +5 V
Supply Voltage: +3 V to +36 V
Transient Spike Protection & RFI Filters Included
Peak Input Voltage (40 ms): 60 V
Reversed Supply Protection: −34 V
Operating Temperate Range: −40°C to +150°C

The AD22055 accepts a differential signal from a bridge transducer whose common-mode signal can be anywhere between the power supplies.

There is an offset pin available which allows the user to shift the zero output point from less than 20 mV to $V_S/2$. This is helpful when compensating bridge offsets.

The extended temperature range allows for local signal conditioning for oil and hydraulic pressure sensors as well as other automotive sensors.

The use of an external gain resistor allows the user to compensate transducer gain error and temperature drift.



Typical Application Circuit for a Pressure Sensor Interface

*Patents pending.

AD22100* – Monolithic Temperature Sensor with Signal Conditioning

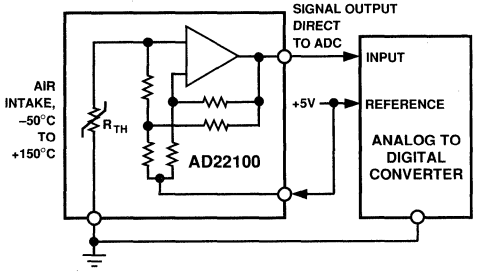
FEATURES
200°C Temperature Span
Accuracy Better Than 2% of Full Scale
Linearity Better Than ±2°C
Ratiometric Output Voltage – Output Proportional to Temperature × Supply Voltage
Reverse Voltage Protection
Low Quiescent Current – Minimal Self-Heating
High Level, Low Impedance Output
22.5 mV/°C from +5.000 V Supply
Wide Power Supply Range

The AD22100 is a monolithic temperature sensor with on-chip signal conditioning. It covers the range −50°C to +150°C making it ideal for use in a wide range of automotive applications, including both liquid and air temperature measurement.

The signal conditioning obviates the need for any trimming, buffering or linearization circuitry, greatly simplifying the overall system design and reducing the overall system cost.

The output voltage, which is proportional to the temperature times the supply voltage, ranges from 0.25 V at −50°C to 4.75 V at +150°C from a +5 V supply.

The output voltage can be input directly to an analog-to-digital converter, which can use the AD22100 supply voltage as its reference.



Typical Application Circuit for a Temperature Sensor

*Patents pending.

AD22150* – Monolithic Hall Effect Sensor with Signal Conditioning

FEATURES

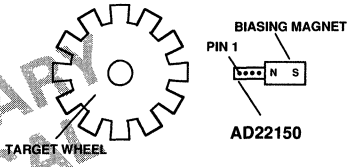
Sensitive to Small Changes in Field: Operate and Release Points at −12 G and +12 G Respectively
Switch Points Moved in Presence of Large Dynamic Fields (±200 G)
Open Collector Output
Open and Release Points
Stable Over −40°C to +150°C Temperature Range
Hysteresis Built Into the Output
Maximum Frequency 50 kHz
Minimum Frequency User Selectable with One External Capacitor

The AD22150 is a monolithic Hall effect sensor complete with signal conditioning circuitry, which is sensitive to changes in magnetic field provided, for example, by teeth on a moving ferrous wheel.

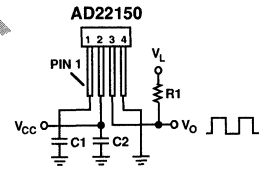
When used in a biasing magnetic field, the ac coupling rejects the steady state field to provide precisely controlled switch points, while hysteresis of the output ensures bounce free transitions between states.

*Patents pending.

The AD22150 is stable over a wide temperature range and has a broad frequency response. Its tolerance of assembly inaccuracies and its immunity to surface roughness combine to give a part ideal for use in diverse applications.



Typical Application Circuit



AD22150 Basic Connection Diagram

AD22180* – Automotive Battery Monitor Circuit

FEATURES

Measures Automotive Battery Temperature & Voltage
Built-In Battery Charging Characteristic
Provides a Signal to Maximize the Battery Charging Without Exceeding the Battery Gassing Voltage at Any Given Temperature
Signals "Charge Battery" for Battery Voltage Below the Battery Voltage Characteristics of the Figure: 13.35 V @ 40°C +35 mV/°C for Temperatures Below 40°C and −11 mV/°C Above 40°C
TTL Compatible Open Collector Output
Output Short Circuit Protected
No External Components Required
Powered Directly by Automobile Battery with Transient and Reverse Voltage Protection
Operating Temperature Range −55°C to +125°C

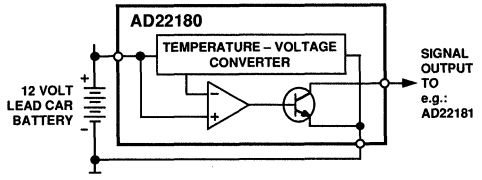
The AD22180 is a three-terminal, monolithic monitor circuit for 12 V, lead based, automotive batteries.

The basic function of this IC is to measure the battery voltage and temperature. The measured voltage and temperature will then be compared with the internal battery charging curve. This IC should be mounted in thermal contact with the battery case.

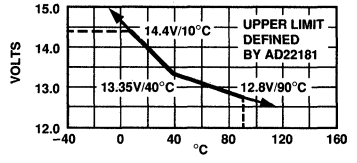
*Protected by U.S. Patent Re30,586; others pending.

The digital open collector output indicates when the battery can be further charged without damaging or reducing its lifetime (digital state: high), and when to stop charging (digital state: low).

The digital output of the AD22180 can be directly connected to the Alternator Controller Circuit AD22181.



Typical Application Circuit



Temperature-Voltage Characteristics

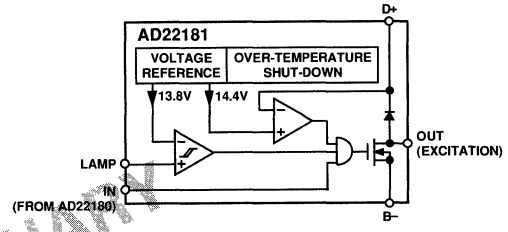
AD22181* – Alternator Control Circuit

FEATURES
Directly Controls Alternator Excitation
Temperature Invariant Charging Voltage Limiter
Over-Temperature Protective Shutdown
Remote Sensed Headlamp Voltage Charging Limit
Interface for Battery Temperature – Voltage Charge Control Using AD22180
Fail-Safe Operation
Acceleration Cut-Off Mode

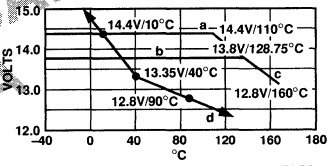
The AD22181 is a 4-pin hybrid device to control an automobile alternator. The AD22181 and AD22180 work together to provide a complete charging control system designed to maximize battery charge without damaging the battery, alternator, headlamps, or electrical system, due to overvoltage or extreme temperature.

The AD22181 contains sensors, control circuitry, and a power transistor to control the excitation to the alternator based on the following input parameters: AD22180 output (car battery voltage and temperature control), alternator temperature (to avoid extreme temperatures), headlamp voltage (to avoid overvoltage to headlamps when they are in "on" condition), and alternator voltage (fail-safe mechanism to avoid overvoltage to the electrical system in case the signal from the AD22180 is lost).

*Protected by U.S. Patent Re30,586; others pending.



Typical Application Circuit



a) FIXED UPPER LIMIT FOR BATTERY VOLTAGE
b) FIXED CHARGING LIMIT HEADLAMP VOLTAGE
c) OVER-TEMPERATURE SHUT-DOWN
d) BATTERY VOLTAGE vs. TEMPERATURE CHARGING LIMIT FROM AD22180

Temperature-Voltage Characteristics

ADXL02* – Monolithic ±2 g Accelerometer with Signal Conditioning

FEATURES
Full-Scale Measurement Range: ±2 g
Self-Test on Digital Command
Single Supply Operation: ±5 V to +24 V
Output Range: 0.25 V to 4.75 V
Accuracy of Span: 8% over −55°C to +125°C
Programmable Bandwidth: DC up to 1 kHz
Linearity: 1% of Full Scale

APPLICATIONS
Anti-Lock Braking Systems
Traction Control Systems
Smart Suspension Systems
Vibration Analysis and Cancellation
Disk Drive
Inertial Guidance
Tilt Sensing
Motion Detection

The ADXL02 is a monolithic accelerometer which combines a polysilicon micromachined sensor with signal conditioning and signal processing circuitry. It is capable of measuring both positive and negative acceleration in the ±2 g range, offering a bandwidth of dc up to 1 kHz.

The ADXL02 uses a capacitive measurement scheme. The analog output is directly proportional to acceleration, and is fully scaled, referenced and temperature compensated resulting in high accuracy and linearity over the automotive temperature range.

A digital commandable self-test allows the sensor beam to be electrostatically deflected at any time, producing an output voltage which corresponds to the −2 g output of a healthy sensor beam.

*Patents pending.

ADXL50* – Monolithic Accelerometer with Signal Conditioning

FEATURES

Full-Scale Measurement Range: ±50 g
Self-Test on Digital Command
Single Supply Operation: +5 V to +24 V
Output Range: 0.25 V to 4.75 V
Accuracy of Span: 8% over −55°C to +125°C
Uncommitted Output Amplifier for Custom Scaling and Zero-g Level Adjustment
Programmable Bandwidth: DC up to 1 kHz
Additional Filtering: 2-Pole with External Passive Components
High Shock Survival: <2000 g Unpowered

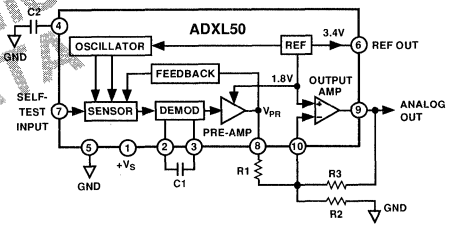
APPLICATIONS

Crash Detection for Airbag Deployment and Seatbelt Retraction
Vibration Analysis and Cancellation
Measurement, Characterization and Instrumentation, e.g., Crash Dummies

The ADXL50 is a monolithic accelerometer which combines a polysilicon micromachined sensor with signal conditioning and signal processing circuitry. It is capable of measuring both positive and negative acceleration in the ±50 g range, offering a bandwidth of dc up to 1 kHz.

The ADXL50 uses a capacitive measurement scheme. The analog output is directly proportional to acceleration, and is fully scaled, referenced and temperature compensated resulting in high accuracy and linearity over the automotive temperature range.

A digitally commandable self-test allows the sensor beam to be electrostatically deflected at any time, producing an output voltage which corresponds to the −50 g output of a healthy sensor beam.



Functional Block Diagram

*Patents pending.

Digital Signal Processing Components

For more than twenty-five years, Analog Devices has provided high-performance solutions to signal processing problems. This extensive interaction with designers of leading-edge signal processing systems forms the basis for continued development of new signal processing products. Today, Analog Devices offers a wide range of programmable DSP processors based on an architecture that is optimized for signal processing. Processors range from a very low cost fixed-point microcomputer, to the highest performance IEEE-compatible floating-point microprocessor.

Together with our signal processing customers, Analog Devices has created the industry's first family of Mixed-Signal Processors (MSProcessors™) and Mixed-Signal Peripherals (MSPeripherals™). Mixed-Signal Processors combine a programmable DSP architecture for signal processing with Analog Devices' precision signal acquisition circuitry to provide compact, low cost, high performance, single-chip solutions. Analog Devices is committed to the continuing integration of high-performance signal acquisition systems with optimized DSP processors.

Future MSProcessors will extend the performance of both the signal acquisition system and the DSP engine to address emerging applications requirements. What applications can you imagine with MSProcessors?

OPTIMIZED DSP ARCHITECTURE

Architectures optimized for DSP must meet the five following requirements:

Fast, Flexible Arithmetic
- Arithmetic units arranged in parallel for Fixed- and Floating-Point families
- Single-cycle register context switch for Fixed- and Floating-Point families
- Separate input and output registers for Fixed-Point family
- General purpose register file for Floating-Point family

Extended Dynamic Range of Multiply/Accumulate
- 40-Bit accumulator for Fixed-Point family
- 80-Bit accumulator for Floating-Point family

Single-Cycle Access of Dual Operands
- Provides single-cycle, 3-bus performance:
  — next instruction fetch
  —2 data operands

Hardware Circular Buffer
- Maintains 8 simultaneous circular buffers for Fixed-Point family
- Maintains 16 simultaneous circular buffers for Floating-Point family

Zero-Overhead Looping and Single-Cycle Conditional Branching
- Single-cycle conditional arithmetic instruction for Fixed- and Floating-Point families
- Stack supports 4 levels of nested loops for Fixed-Point family
- Stack supports 16 levels of nested loops for Floating-Point family

Analog Devices extends the optimized DSP architecture to include features such as:
- Auto data buffering
- Auto boot from external byte-wide EPROM
- Auto companding of data through serial port

DSP DEVELOPMENT SUPPORT

All processors are supported with a comprehensive set of development tools including:

- ANSI C-Compiler
- Linker
- System Builder
- Low Cost EZ-TOOLS
- Assembler
- Simulator
- Demonstration Board
- In-Circuit Emulators

Applications assistance is provided by:

- Expert DSP Staff
- Applications Handbooks
- Applications Assistance Line
- Computer Bulletin Board
- *DSPatch* Applications Newsletter
- Applications Library
- 3-Day Programming Workshop

For more information on our DSP products, contact your local Analog Devices sales office or authorized distributor. For marketing information, contact DSP marketing (617) 461-3881. For applications assistance, contact DSP applications (617) 461-3672.

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Selection Guide
DSP Processor Key Feature Summary

Model	Inst Cycle Time ns	Off-Chip Harvard Arch	Internal Program Memory RAM	Internal Data Memory RAM	Internal Program Cache Word	Program Memory Boot	Serial Ports	8/16-Bit Host Interface Port	Program Timer	On-Chip A/D and D/A	Ext Interrupts	Low Power Modes	Pin Count	Package Options[1]
16-Bit Fixed-Point														
ADSP-2100A	80	\	—	—	16 × 24	—	—	—	—	—	4	—	100	PGA, PQFP, CQFP
ADSP-2101	60	—	2K × 24	1K × 16	—	\	2	—	\	—	3	1	68	PGA, PLCC
ADSP-2102	60	—	2K × 24[2]	1K × 16	—	\	2	—	\	—	3	1	68	PGA, PLCC
ADSP-2105	100	—	1K × 24	0.5K × 16	—	\	1	—	\	—	3	1	68	PLCC
ADSP-2106	100	—	1K × 24[2]	0.5K × 16	—	\	1	—	\	—	3	1	68	PLCC
ADSP-2111	60	—	2K × 24	1K × 16	—	\	2	\	\	—	3	1	100	PGA, PQFP
ADSP-2112	60	—	2K × 24[2]	1K × 16	—	\	2	\	\	—	3	1	100	PGA, PQFP
ADSP-21msp50	77	—	2K × 24	1K × 16	—	\	2	\	\	\	3	2	132/144	PQFP/PGA
ADSP-21msp51	77	—	2K × 24[2] & 2K × 24 ROM	1K × 16	—	\	2	\	\	\	3	2	132/144	PQFP/PGA
32/40-Bit Floating-Point														
ADSP-21010	80	\	—	—	32 × 48	—	—	—	\	—	4	1	304	PQFP
ADSP-21020	40	\	—	—	32 × 48	—	—	—	\	—	4	1	223	PGA

NOTES
[1]Package Options: CQFP = Ceramic Quad Flat Pack; PGA = Ceramic Pin Grid Array; PLCC = Plastic Leaded Chip Carrier; PQFP = Plastic Quad Flat Pack; PPGA = Plastic Pin Grid Array.
[2]RAM/ROM.

Mixed-Signal Application Specific Integrated Circuits

Analog Devices offers a full spectrum of signal conditioning and conversion capabilities in mixed-signal application specific integrated circuits (ASICs). These chip-level systems can implement combined analog/digital designs with 10- to 14-bit accuracy and 12- to 20-bit resolution that formerly required board-level solutions. Combined with our general purpose DSPs from the ADSP-2100 and ADSP-21000 families, our ASICs can provide custom two-chip solutions to meet complex system requirements.

Analog Devices can incorporate most of the functions of its standard monolithic linear and converter parts in full-custom and semicustom ICs. Full-custom parts optimize performance and space requirements, while cell-based semicustom parts reduce development time and engineering expense. Development costs can be cut further by tailoring a predefined system-on-a-chip known as a Linear System Macro to your application.

Analog's experienced design engineers work with powerful computer-aided design tools to design and lay out your circuit. Design centers are currently in Massachusetts, Japan and Ireland.

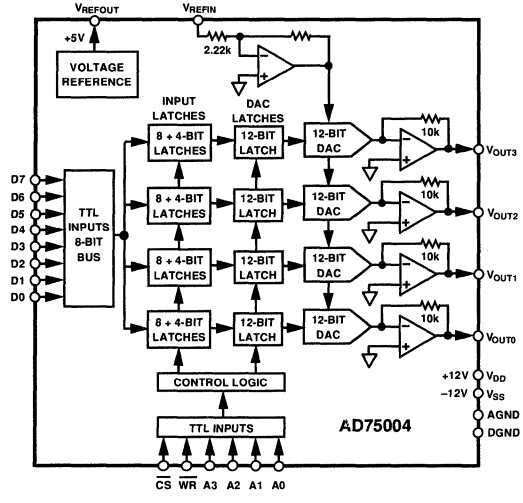
Multiple locations for fabrication, assembly and testing ensure a ready supply of production parts. Products are processed in our MIL-38510 certified facilities.

DESIGN EXAMPLES

Analog Devices has created a variety of customer-specific and function-specific ASICs for data acquisition and signal processing. Two examples of cell-based designs are the following application specific standard products (ASSPs).

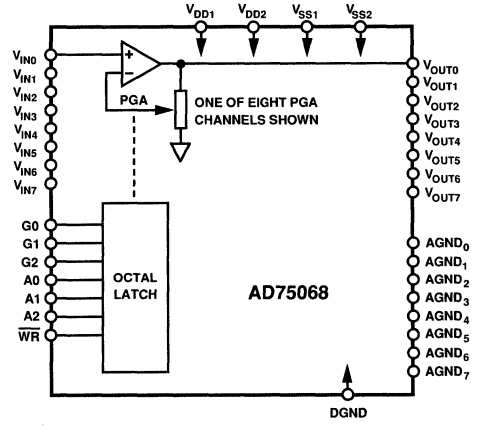
AD75004 Quad DAC

This circuit contains four separate 12-bit D/A converters with amplifiers for voltage output and an on-board reference. Double-buffering latches interface with an 8-bit parallel bus and permit updating of all four channels individually or simultaneously. Outputs swing ±5 V, drive ±5 mA, and settle within 4 μs.



AD75068 Octal Programmable Gain Amplifier

The AD75068 contains eight programmable gain amplifiers (PGAs). Each is complete, including switch/resistor network and gain programming latch, and requires no external components. Each channel may be independently programmed for gains from 1 to 128. A unique circuit design maintains constant 2 MHz bandwidth at all gains and offers very low phase shift; the PGAs also feature low input bias current (<4 pA).



Derivative Circuits

The circuits outlined above can be modified to suit a specific customer's application. For example, the AD75004 quad DAC could be expanded to 6 channels, each of which may have separate reference inputs. The AD75068 could be configured to include filtering. These modifications, when based on standard library cells, can provide the fastest, most cost effective semicustom solution.

Analog/Digital BiCMOS Processes

Analog Devices fabricates ASICs and USICs in four bipolar-CMOS processes, which are also used for volume production of standard ICs. All of these processes are optimized for analog and mixed-signal circuits and handle wide dynamic ranges. They combine bipolar and CMOS transistors with accurate resistors on one chip.

The bipolar transistors provide precision, low noise, low offset input stages and moderate-power output stages. The CMOS devices make low power logic; switches for analog multiplexers, data converters, and switched-capacitor filters; and high impedance input stages and current sources for linear circuitry. The thin-film resistors are very stable over time and temperature, and may be laser-trimmed for tight tolerance on relative matching and absolute values.

The BiMOS II Process

BiMOS II has the most comprehensive cell library of Analog's BiCMOS processes; highlights of the library are listed below. With supply voltages up to 24 V and its very low noise, it can handle signals with a dynamic range of over 20 bits.

BiMOS II features high quality NPN transistors that have very low noise, tight matching, and high Early voltage. These characteristics make possible high performance amplifiers and comparators with low offset input stages and excellent linearity, as well as stable bandgap references.

The 3-μ CMOS builds logic as well as analog switches and high impedance input stages and current sources. The exceptionally stable thin-film resistors are used in precision data converters, programmable-gain amplifiers, and other linear circuits.

BiMOS II uses two levels of metal interconnect as well as self-aligned polysilicon to reduce chip area and layout time. It is fabricated on epitaxial wafers that minimize crosstalk, leakage, and ESD susceptibility.

The BiMOS II process can operate with supplies up to 24 V; the cell library is designed to run on ±12 V supplies. Most BiMOS II cells are designed to accommodate ±5 V signals, although some cells can handle ±8 V or ±10 V swings.

BiMOS II Cell Library

The following table lists key examples of analog and converter cells in the BiMOS II library. Logic cells include gates, counters, registers, microsequencer, PLA, RAM and ROM. Interface cells include 8-bit and 16-bit parallel I/O ports as well as synchronous serial ports and UARTs.

Analog-to-Digital Converter

ADC1210	12-bit resolution, 15 μs conversion time, ±5 V input range, SAR type

Amplifiers

AMPBH10	Bipolar input op amp; gain > 120 dB, BW > 1.6 MHz, offset < 0.5 mV
AMPBH20	Bipolar input op amp; uncompensated, bandwidth > 2.75 MHz at gain ≥ 4
AMPBH30	Bipolar input instrument amplifier; CMRR ≥ 75 dB, nonlinearity < 20 ppm
AMPBH40	Bipolar input op amp; I_B < 1 nA, gain > 120 dB, offset < 0.5 mV
AMPMH10	MOS input op amp; I_B < 50 pA, gain > 120 dB, bandwidth > 1.6 MHz

Comparator

CMPBH10	Bipolar input comparator; clocked; prop delay < 130 ns at 1 mV overdrive

Digital-to-Analog Converters

DAC0810	8-bit res., settling time < 70 ns, 0–248 μA output, INL & DNL < 0.25 LSB
DAC1210	12-bit res., settling time < 100 ns, 0–1 mA output, INL & DNL < 1 LSB
DAC1220	12-bit res., settling time < 25 ns, 4-quad multiplying, INL & DNL < 1 LSB
DAC1410	14-bit resolution, settling time < 120 ns, 0–2 mA output, DNL < 1 LSB

Analog Multiplexers

MUX1B10D	2-channel mux; R_{ON} < 3 kΩ, turn-on time < 30 ns, charge injection ≈ 0.1 pC
MUX1B30	Analog switch; R_{ON} < 100 Ω, turn-on time < 30 ns, charge injection ≈ 1 pC

Voltage References

REF5V30	5 V reference; TC < 25 ppm/°C, I_{load} <4 mA, w/force and sense lines
REF10V10	10 V reference; TC < 25 ppm/°C, I_{load} <4 mA, w/force and sense lines

Sample-and-Hold Amplifier

SHATF10	For 12-bit use; acquisition time < 3 μs, slew rate ≈ 6 V/μs, droop ≈ 2.5 mV/ms

Temperature Sensor

TMP10	Outputs 10 mV/K (3.00 V at 27°C)

ANALOG DEVICES HIGH PERFORMANCE BiCMOS PROCESSES FOR ASICs

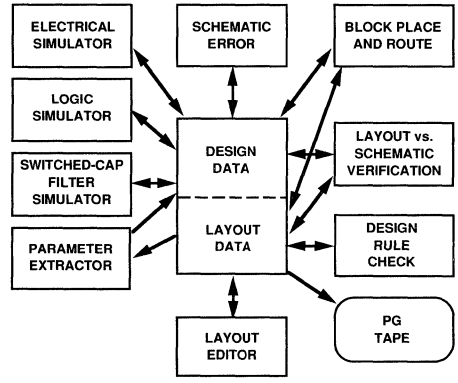
Process	Supply Voltage	Gate Length	f_T	Gate Capacity	Features
BiMOS II	24 V	3 μ	300 MHz	2,000	Large Cell Library
ABCMOS	12 V	2 μ	2 GHz	10,000	Highest Speed, Density
LC²MOS-2	12 V	2 μ	1 GHz	5,000	JFET, Buried Zener
LC²MOS-5	30 V	5 μ	1 GHz	1,000	JFET, Buried Zener

Other Processes

While BiMOS II is used for most cell-based USICs, Analog Devices fabricates USICs in three other processes which may be used in applications that require higher speed, lower noise, or higher supply voltage. ABCMOS (Advanced Analog BiCMOS) is our newest, fastest, and densest BiCMOS process. It features 2 GHz NPN devices and fine-geometry CMOS and runs on ±5 V supplies, with ±3 V signal swings. LC²MOS (Linear-Compatible CMOS) has two variants: one runs on ±5 V supplies, with ±3 V signal swings; the other runs on ±15 V, with ±10 V swings. LC²MOS also includes JFETs for very low input noise at high input impedance, and buried Zener diodes with better noise and drift than many bandgap references.

The table above compares our BiCMOS USIC processes and highlights the key features of each. Analog Devices will review your application and recommend the appropriate bipolar process for your needs.

COMPUTER-AIDED DESIGN FLOW



COMPUTER-AIDED DESIGN TOOLS

Designing a high performance mixed-signal IC is inherently more difficult than designing a gate array. The variety of analog and digital functions requires a cell-based approach. However, the use of powerful tools gives high confidence of functionality at first silicon through thorough simulation and layout verification. Complete computer-generated documentation of all schematics and analog and logic simulation waveforms permits thorough evaluation of Analog's design by your design staff before signoff for final layout and fabrication.

The overall work flow through the CAD environment follows. Key to meeting the special challenges of mixed analog/digital circuitry are the simulation and auto-layout tools, and the unification of design and layout information in a single database. Analog Devices has developed a suite of proprietary computer-aided design tools, called JANUS™, to address these issues and to implement turn-key designs.

The JANUS schematic editor offers numerous time-saving techniques and provides for specification of such data as wire widths, routing layers and routing priorities. It automatically generates a net list used by subsequent tools.

Analog uses several simulators, including electrical, logic and behavioral types. ADICE, a proprietary enhanced version of the SPICE electrical simulator, gives precision simulation of critical analog sections. It uses Newton-Raphson methods to iteratively solve nonlinear time-dependent simultaneous differential equations. It is efficient for circuits up to about 250 active devices and is used for the frequency domain or transient analysis of analog cells such as op amps, or sensitive digital cells such as dynamic RAM.

Event-driven simulators handle larger circuits, with thousands of devices, and are typically used to simulate logic. The JANUS mixed-signal simulator combines an event-driven simulator with Newton-Raphson methods. It dynamically partitions the circuit to apply the faster event-driven techniques where possible, and the matrix methods where necessary. It also dynamically sizes the matrix and time steps to speed simulation further. The simulator can operate at the transistor level or use behavioral models, or both at the same time, allowing trade-offs between accuracy and speed.

For layout, the challenge is to increase automation while accommodating the layout sensitivity of analog circuitry. Device generators exist for the full range of active and passive devices available in the technology to automatically create a physical representation of the circuit schematic. This layout may be optimized through conventional interactive polygon-pushing.

The JANUS routing editor is driven by the connectivity of the schematics, but allows great freedom to manually control the routing of critical analog signal paths or power/ground lines while autorouting noncritical nets and spacing the layout to achieve automatic enforcement of layout rules. The JANUS routing editor uses up to three interconnect levels, and will automatically expand and compact placement as necessary to achieve 100% routing.

Finally, industry-standard layout verification tools assure conformance of the layout to both the schematic and design rules to give high confidence of functionality in first silicon. The CAD tool suite communicates via industry-standard stream formats to external databases and pattern generators.

JANUS is a trademark of Analog Devices, Inc.

TEST AND TRIM

Analog Devices has over 20 years of experience in testing complex circuits and manufactures commercial test systems for precision linear ICs. In each fabrication facility, a computer network integrates Analog Devices, H-P, Teradyne and LTX test equipment. The design, wafer probe and test areas share data on the network for statistical analysis and device modeling.

All Analog Devices ASICs are tested at the wafer level, and most are laser-wafer trimmed to achieve high accuracy. Untrimmed thin-film resistors match within 1% to 0.1%, depending on area. Trimmed resistors can match to better than 0.01%. Wafers may be laser drift trimmed with a hot-chuck probe to minimize the effects of temperature on accuracy.

After packaging, all parts are tested to assure that they meet guaranteed specifications. Environmental handlers can verify parts at multiple temperatures. Burn-in is performed as specified by the customer.

PACKAGING

Analog Devices ICs are available in most modern package types, including high pin-count and surface mount varieties. ASICs may be assembled in any of Analog Devices' standard packages, listed below. This list is constantly expanded and other packages may be used if they are suitable for high performance applications.

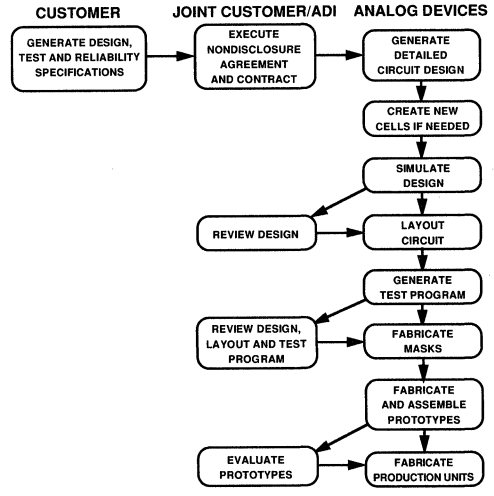
Available Packages

Pin Grid Array (PGA): 68 to 144 pins
Ceramic J Leaded Chip Carrier (CJLCC): 44 to 68 pins
Plastic Quad Flat Pack (PQFP): 44 to 132 pins
Plastic Leaded Chip Carrier (PLCC): 20 to 68 pins
Plastic Dual Inline Package (DIP): 14 to 64 pins
Side-Brazed DIP: 14 to 64 pins
Frit-Seal DIP (Cerdip): 14 to 40 pins
Small Outline (SO): 14 to 28 pins
Ceramic Quad Flat Pack (CQFP): 80 to 104 leads

PROGRAM RESPONSIBILITIES AND INTERFACES

The following figure shows the major phases in developing an ASIC and responsibilities during each phase. The overall development time depends on the complexity of the circuit and on how custom the design is.

Your Analog Devices sales engineer is your first interface for ASIC development. Your local sales office can provide further information on Analog Devices' custom/semicustom capabilities.



Power Supplies
Modular AC/DC Power Supplies

GENERAL DESCRIPTION

Analog Devices offers a broad line of modular ac/dc power supplies that provide both OEMs and designers a reliable, easy to use, low-cost solution to their power requirements. Models are available in PC mountable and chassis mountable designs with 5 volt to 15 volt (single, dual, triple) outputs and current ratings from 25 mA to 5 amps. Since these modular supplies are fully encapsulated, no trimming or external component selection is necessary; simply mount the unit, connect power and output leads, and you're on the air! Most Analog Devices' power supplies are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

AC/DC POWER SUPPLY FEATURES

- Current Limit Short Circuit Protection
- PC Mounted and Chassis Mounted Versions
- Single (+5 V), Dual (±12 V, ±15 V), and Triple (±15 V/+5 V, ±15 V/+1 V to +15 V) Output Supplies
- Current Outputs:
  25 mA to 1000 mA for Dual and Triple Output Supplies
  250 mA to 5000 mA for Single Output Supplies
- Wide Input Voltage Range
- Low Output Ripple and Noise
- Excellent Line & Load Regulation Characteristics
- High Temperature Stability
- Free-Air Convection Cooling; No External Heat Sink Required

GENERAL SPECIFICATIONS

Power Requirements

Input Voltage Range:	105 V ac to 125 V ac
Frequency:	50 Hz to 250 Hz

Electrical Specifications

Temperature Coefficient:	0.02%/°C
Output Voltage Accuracy:	±2%, max See Specifications Table
Breakdown Voltage:	500 V rms, min
Isolation Resistance:	50 MΩ
Short Circuit Protection:	All ac/dc power supplies employ current limiting. They can withstand substantial overload including direct short. Prolonged operation should be avoided since excessive temperature rises will occur.

Environmental Requirements

Operating Temperature Range:	−25°C to +71°C
Storage Temperature Range:	−25°C to +85°C

SPECIFICATIONS – Typical @ +25°C and 115 V ac 60 Hz unless otherwise noted*

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. max %	Load Reg. max %	Output Voltage Error max	Ripple & Noise mV rms max	Dimensions Inches
PC Board Mounted	Dual Output	904	±15	±50	0.02	0.02	±200 mV −0 mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300 mV −0 mV	0.5	3.5×2.5×1.25
	Single Output	905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
		928	5	3000	0.05	0.10	±2%	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1%	0.5	
		927	±15	±150	0.02	0.02	±2%	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2%	1.0 (typ)	
Chassis Mounted	Dual Output	970	±15	±200	0.05	0.05	±2%	1	4.4×2.7×1.45
		975	±15	±500	0.05	0.05	±2%	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.45
		976	5	3000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
		977	5	5000	0.05	0.10	±2%	5 (typ)	4.75×2.7×1.45
	Triple Output	974	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2%	1.0 (typ)	

*Consult Analog Devices Power Supplies Catalog for additional information.
Specifications subject to change without notice.

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Power Supplies
Modular DC/DC Converters

GENERAL DESCRIPTION

Analog Devices' line of compact dc/dc converters offers system designers a means of supplying a reliable, easy to use, low cost solution to a variety of floating (analog and digital) power applications. These devices provide high accuracy, short circuit protected, regulated outputs with very low output noise and ripple characteristics.

Fourteen models are offered in five power levels of 1 watt, 1.8 watts, 4.5 watts, 6 watts and 12 watts. Input voltage versions include 5 volt, 12 volt, 24 volt and 28 volt with output ranges as follows: +5 volt, ±12 volts and ±15 volts at ±60 mA to 1000 mA output current capability.

Most models are high efficiency (typically over 60% at full load) and feature complete 6-sided continuous shielding for EMI/RFI protection. A π-type input filter is contained, in some models, which virtually eliminates the effects of reflected input ripple current. Most Analog Devices' dc/dc converters are available from stock in both large and small quantities with substantial discounts being applied to large quantity orders.

DC/DC POWER SUPPLY FEATURES

- Inaudible (>20 kHz) Converter Switching Frequency
- Continuous, Six-Sided EMI/RFI Shielding Except on 1 Watt and 1.8 Watt Models
- Output Short Circuit Protection (Either Output to Common)
- Automatic Restart After Short Condition Removed
- Automatic Starting with Reverse Current Injected into Outputs
- Low Output Ripple and Noise
- High Temperature Stability
- Free Air Convection Cooling
  No external heat sink or specification derating is required over the operating temperature range.

GENERAL SPECIFICATIONS FOR 1 W AND 1.8 W MODELS

Line Regulation – Full Range: ±0.3% (±1% max, 949)
Load Regulation – No Load to Full Load: ±0.4% (±0.5% max, 949)
Output Noise and Ripple: 20 mV p-p, with 15 μF tantalum capacitor across each output (2 mV rms max, 949)
Breakdown Voltage: 300 V dc min (500 V dc min, 949)
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C (+100°C, 949)
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

GENERAL SPECIFICATIONS FOR 4.5 W, 6 W AND 12 W MODELS

Line Regulation – Full Range: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Load Regulation – No Load to Full Load: ±0.07% max (±0.02% max, 951, 960 Series) (±0.1% max, 943)
Output Noise and Ripple: 1 mV rms max
Breakdown Voltage: 500 V dc min
Input Filter Type: π
Operating Temperature Range: −25°C to +71°C
Storage Temperature Range: −40°C to +125°C
Fusing: If input fusing is desired, we recommend the use of a slow blow type fuse that is rated at 150%–200% of the dc/dc converter's full load input current.

SPECIFICATIONS – Typical @ +25°C at nominal input voltage unless otherwise noted*

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[1] Voltage Range Volts	Input Current Full Load	Output Voltage Error max	Temperature Coefficient /°C max	Efficiency Full Load min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52A	±1%	±0.02%	62%	2.0×2.0×0.38
958	5	100	5	4.5/5.5	200 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.75/5.25	1.17A	±1%	±0.01%	58%	2.0×2.0×0.38
960	±12	±40	5	4.5/5.5	384 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
962	±15	±33	5	4.5/5.5	396 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
964	±15	±33	12	10.8/13.2	165 mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
965	±15	±190	5	4.65/5.5	1.7 A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
966	±15	±190	12	11.2/13.2	710 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
967	±15	±190	24	22.3/26.4	350 mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6 A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35 A	±1%	±0.01%	62%	2.0×2.0×0.38
953	±15	±150	12	11/13	0.6 A	±0.5%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250 mA	±0.5%	±0.01%	61%	2.0×2.0×0.38

NOTES
[1]Models 940 and 941 will deliver up to 120 mA output current (and Model 943 will deliver up to 600 mA) over an input voltage range of 4.65 V dc and 5.5 V dc.
*Consult Analog Devices Power Supplies Catalog for additional information.
**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120 mA.
Specifications subject to change without notice.

Package Information
Contents

*Special Order Only

ADI Letter Designator	PMI Letter Designator	Package Description	MIL-STD-1835 Applicable Configuration	Page
Plastic Quad Flatpack				
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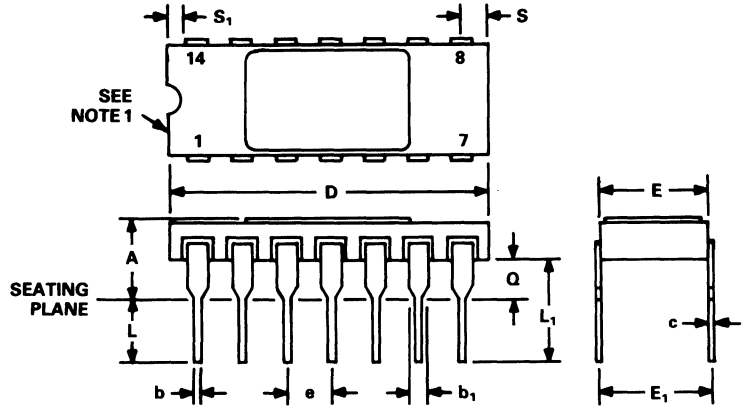
Plastic				
TO-92		3-Lead		15-36
Single In-Line Package (SIP)				
Y-4		4-Lead		15-37
Leaded Chip Carrier				
Z-16A		16-Lead		15-38
Z-16B		16-Lead (Wide)		15-39

Package Outline Dimensions

D-14

14-Lead Side Brazed Ceramic DIP
(YB Suffix)



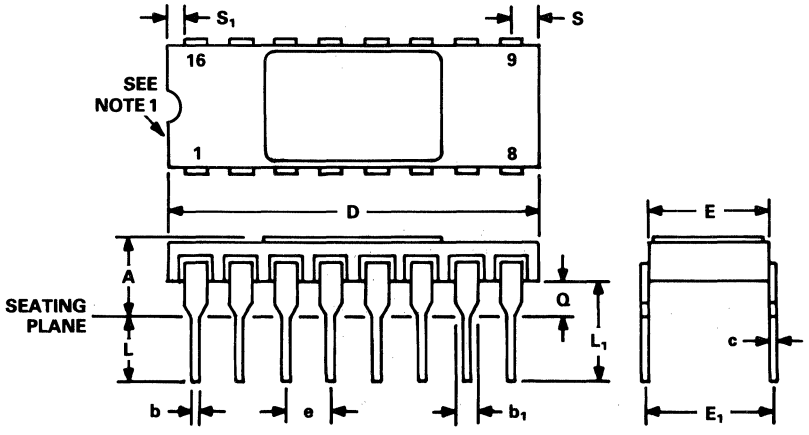
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder DIP lead finish is applied.
7. Twelve spaces.

15

D-16

16-Lead Side Brazed Ceramic DIP
(QB Suffix)



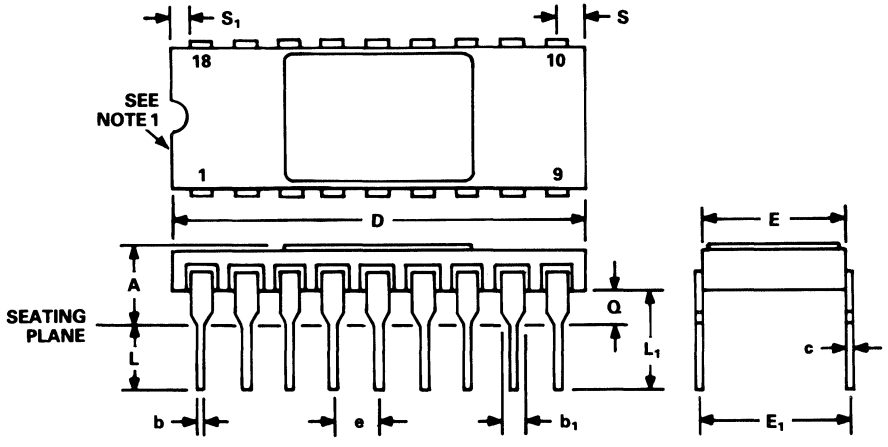
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003″ (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Fourteen spaces.

D-18

18-Lead Side Brazed Ceramic DIP
(XB Suffix)



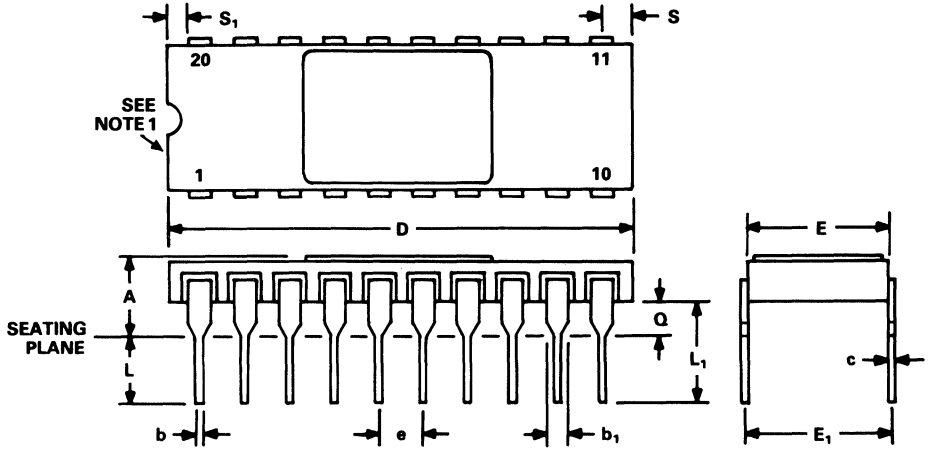
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Sixteen spaces.

D-20

20-Lead Side Brazed Ceramic DIP
(RB Suffix)

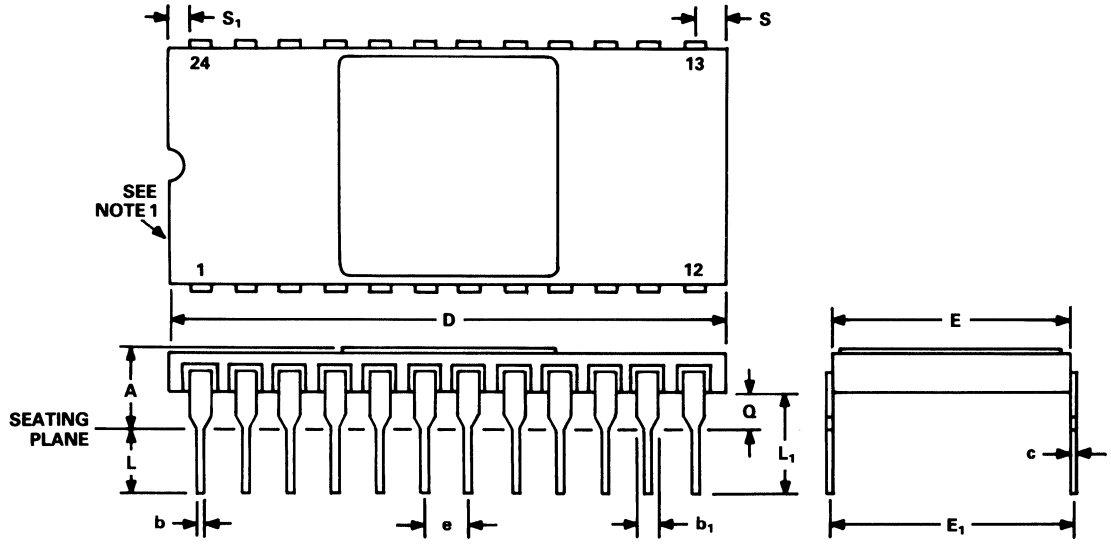


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2, 6
c	0.008	0.015	0.20	0.38	6
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	
e	0.100 BSC		2.54 BSC		7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003″ (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Eighteen spaces.

D-24
24-Lead Side Brazed Ceramic DIP

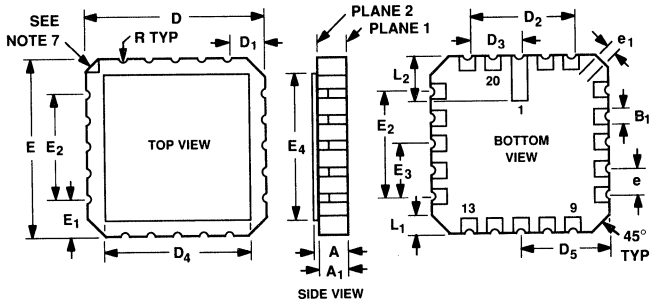


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.225		5.72	
b	0.014	0.023	0.36	0.58	6
b_1	0.030	0.070	0.76	1.78	2,6
c	0.008	0.015	0.20	0.38	6
D		1.290		32.77	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	
e	0.090	0.110	2.29	2.79	7
L	0.120	0.200	3.05	5.08	
L_1	0.150		3.81		
Q	0.015	0.075	0.38	1.91	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. All leads – increase maximum limit by 0.003" (0.08mm) measured at the center of the flat, when hot solder dip lead finish is applied.
7. Twenty-two spaces.

E-20A

20-Terminal Leadless Chip Carrier
(RC Suffix)



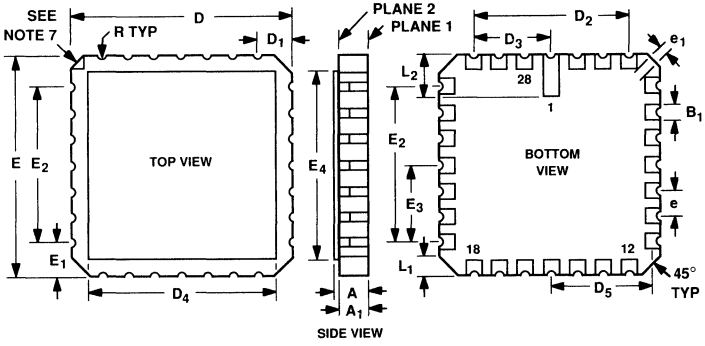
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.100	1.63	2.54	5
A_1	0.054	0.088	1.37	2.24	
B_1	0.022	0.028	0.56	0.71	2
D	0.342	0.358	8.69	9.09	
D_1	0.075 REF		1.91 REF		
D_2	0.200 REF		5.08 REF		
D_3	0.100 REF		2.54 REF		
D_4		0.358		9.09	3
D_5	0.150 BSC		3.81 BSC		
E	0.342	0.358	8.69	9.09	
E_1	0.075 REF		1.91 REF		
E_2	0.200 REF		5.08 REF		
E_3	0.100 REF		2.54 REF		
E_4		0.358		9.09	3
e	0.050 BSC		1.27 BSC		
e_1	0.015		0.38		1
L_1	0.045	0.055	1.14	1.40	
L_2	0.075	0.095	1.90	2.41	4
R	0.007	0.011	0.18	0.28	

NOTES

1. A minimum clearance of 0.015″ (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on Plane 1. Metalization is optional on Plane 2. However, if Plane 2 is metalized, it must be electrically connected.
3. A minimum clearance of 0.020″ (0.508 mm) is maintained between overall dimensions $D_4 \times E_4$ and all other features including metalization, chamfers and edges.
4. Nonelectrical feature for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on Plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metalization may increase only toward package periphery.
7. When space is available, the index corner may be metalized on either or both Planes 1 and 2. The package edge at the index corner shall not be metalized.

E-28A

28-Terminal Leadless Chip Carrier
(TC Suffix)



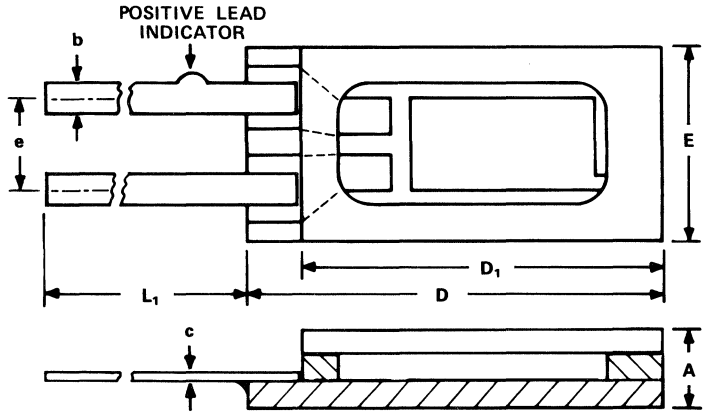
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.064	0.100	1.63	2.54	5
A_1	0.054	0.088	1.37	2.24	
B_1	0.022	0.028	0.56	0.71	2
D	0.442	0.458	11.23	11.63	
D_1	0.075 REF		1.91 REF		
D_2	0.300 REF		7.62 REF		
D_3	0.150 REF		3.81 REF		
D_4		0.458		11.63	3
D_5	0.200 BSC		5.08 BSC		
E	0.442	0.458	11.23	11.63	
E_1	0.075 REF		1.91 REF		
E_2	0.300 REF		7.62 REF		
E_3	0.150 REF		3.81 REF		
E_4		0.458		11.63	3
e	0.050		1.27		
e_1	0.015		0.38		1
L_1	0.045	0.055	1.14	1.40	
L_2	0.075	0.095	1.90	2.41	4
R	0.007	0.011	0.18	0.28	

NOTES

1. A minimum clearance of 0.015" (0.381 mm) is maintained between corner terminals.
2. Electrical connection is required on Plane 1. Metalization is optional on Plane 2. However, if Plane 2 is metalized, it must be electrically connected.
3. A minimum clearance of 0.020" (0.508 mm) is maintained between overall dimensions $D_4 \times E_4$ and all other features including metalization, chamfers and edges.
4. Nonelectrical feature for No. 1 terminal identification, optical orientation or handling purposes shall be within the shaded area shown on Plane 2.
5. Dimension A controls the overall package thickness.
6. Length of pad metalization may increase only toward package periphery.
7. When space is available, the index corner may be metalized on either or both Planes 1 and 2. The package edge at the index corner shall not be metalized.

F-2A

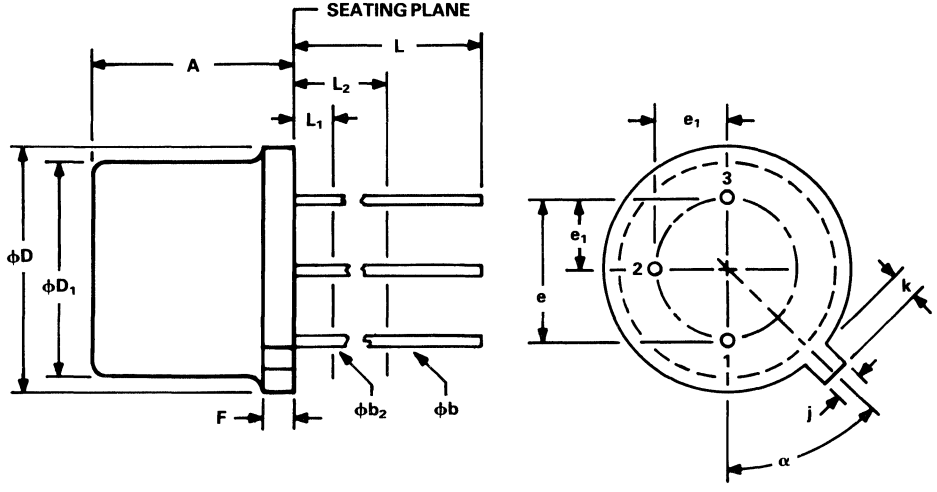
2-Lead Flatpack



	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.044	0.066	1.12	1.67	
b	0.015	0.019	0.38	0.48	2
c	0.0045	0.0065	0.12	0.17	2
D		0.250		6.35	1
D_1		0.220		5.59	
E	0.081	0.093	2.06	2.36	1
e	0.045	0.055	1.14	1.40	
L_1	0.750		19.05		

NOTES
1. This dimension allows for off-center lid, meniscus and solder overrun.
2. All leads – increase maximum limit by 0.003" (0.08 mm) when hot solder dip finish is applied.

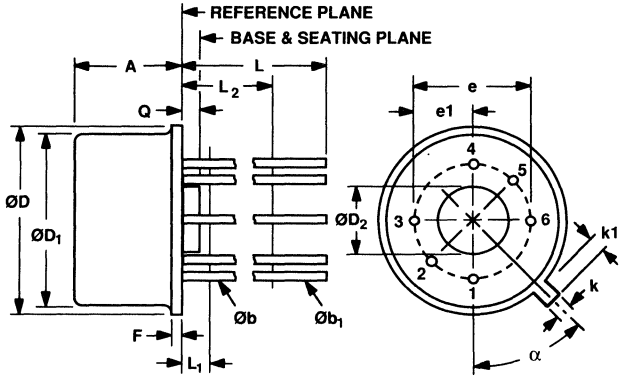
H-03A
3-Lead Metal Can (TO-52)



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.115	0.150	2.92	3.81	
ϕb		0.021		0.53	1,4
ϕb_2	0.016	0.019	0.41	0.48	1,4
ϕD	0.209	0.230	5.31	5.84	
ϕD_1	0.178	0.195	4.52	4.95	
e	0.100 T.P.		2.54 T.P.		2
e_1	0.050 T.P.		1.27 T.P.		2
F		0.030		0.76	
j	0.036	0.046	0.91	1.17	
k	0.028	0.048	0.71	1.22	3
L	0.500		12.70		1
L_1		0.050		1.27	1
L_2	0.250		6.35		
α	45° T.P.				

NOTES
1. (Three Leads) ϕb_2 applies between L_1 and L_2. ϕb applies between L_2 and 0.5" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5" (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.054" (1.4mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

6-Lead TO-78 Metal Can
(H Suffix)



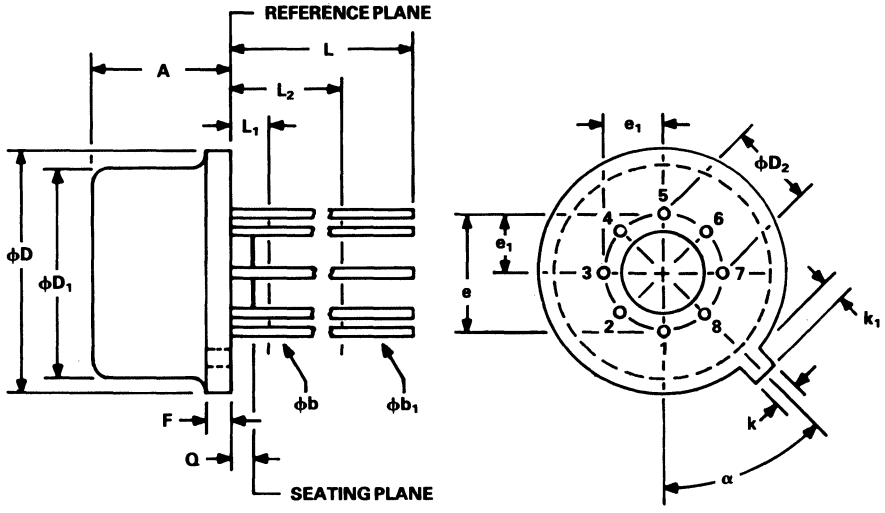
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES

1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500″ (12.70 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500″ (12.70 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019″ (0.48 mm) measured in gaging plane 0.054″ (1.37 mm) + 0.001″ (0.03 mm) – 0.000″ (0.00 mm) below the base plane of the product is within 0.007″ (0.18 mm) of their true position relative to a maximum width tab.

H-08A

8-Lead Metal Can (TO-99)
(J Suffix)



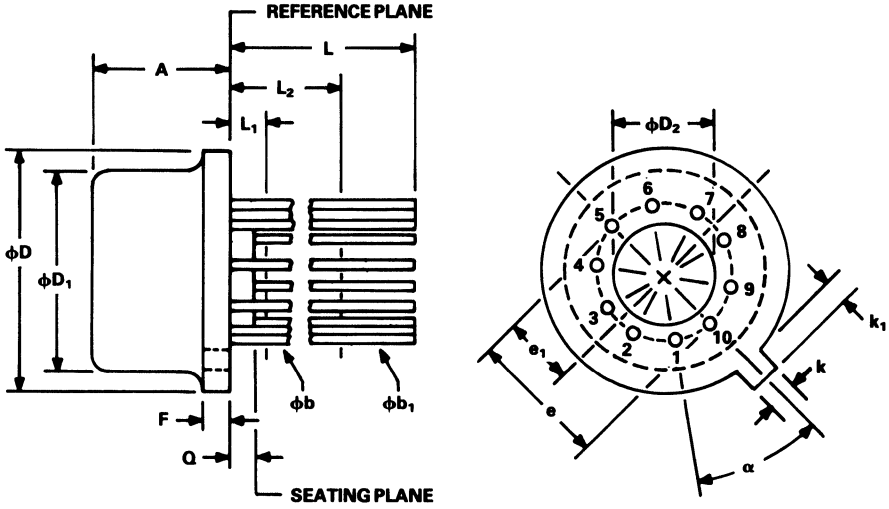
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
ϕb_1	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
ϕD_1	0.305	0.335	7.75	8.51	
ϕD_2	0.110	0.160	2.79	4.06	
e	0.200 BSC		5.08 BSC		3
e_1	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	
L	0.500	0.750	12.70	19.05	
L_1		0.050		1.27	
L_2	0.250		6.35		
Q	0.010	0.045	0.25	1.14	
α	45° BSC		45° BSC		3

NOTES
1. (All leads) ϕb applies between L_1 and L_2. ϕb_1 applies between L_2 and 0.500" (12.70mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.500" (12.70mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019" (0.48mm) measued in gauging plane 0.054" (1.37mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the base plane of the product are within 0.007" (0.18mm) of their true position relative to the maximum width tab.
4. All leads – increase maximum limit 0.003" (0.08mm) when hot solder dip finish is applied.

15

H-10A

10-Lead Metal Can (TO-100)
(K Suffix)

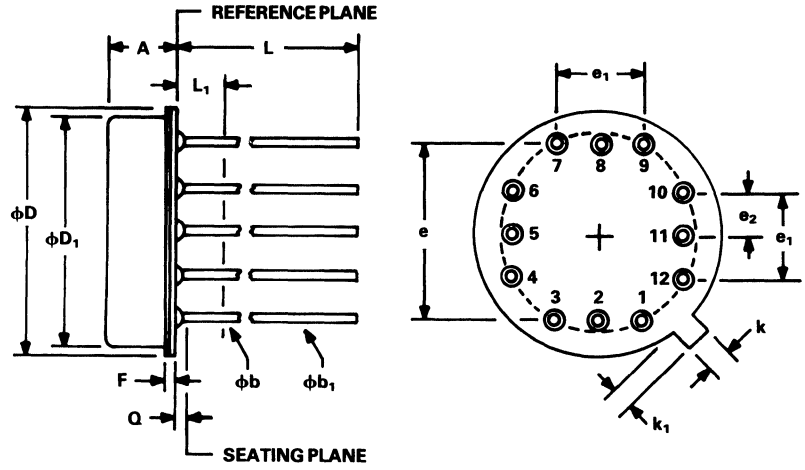


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	
ϕb	0.016	0.019	0.41	0.48	1,4
$ϕb_1$	0.016	0.021	0.41	0.53	1,4
ϕD	0.335	0.370	8.51	9.40	
$ϕD_1$	0.305	0.335	7.75	8.51	
$ϕD_2$	0.110	0.160	2.79	4.06	
e	0.230 BSC		5.84 BSC		3
e_1	0.115 BSC		2.92 BSC		3
F		0.040		1.02	
k	0.027	0.034	0.69	0.86	
k_1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L_1		0.050		1.27	1
L_2	0.250		6.35		1
Q	0.010	0.045	0.25	1.14	
α	36° BSC		36° BSC		3

NOTES
1. (Three Leads) $ϕb_2$ applies between L_1 and L_2. ϕb applies between L_2 and 0.5" (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.5" (12.70mm) from seating plane.
2. Leads having maximum diameter 0.019" (0.48mm) measured in gauging plane 0.054" (1.4mm) + 0.001" (0.03mm) – 0.000" (0.00mm) below the seating plane of the device are within 0.007" (0.18mm) of their true positions relative to a maximum-width tab.
3. Measured from maximum diameter of the actual device.
4. All leads – increase maximum limit by 0.003" (0.08mm) when hot solder dip finish is applied.

H-12A

12-Lead Metal Can (TO-8 Style)



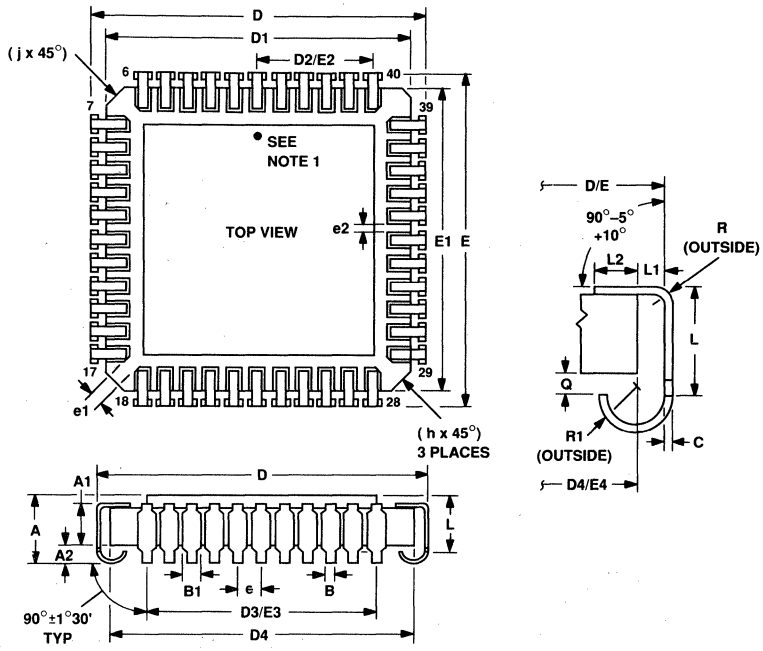
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.148	0.181	3.76	4.60	
ϕb	0.016	0.019	0.41	0.48	1
ϕb_1	0.016	0.021	0.41	0.53	1
ϕD	0.592	0.615	15.04	15.62	
ϕD_1	0.545	0.555	13.84	14.10	
e	0.400 BSC		10.16 BSC		3
e_1	0.200 BSC		5.08 BSC		3
e_2	0.100 BSC		2.54 BSC		3
F		0.040		1.02	
k	0.026	0.036	0.66	0.91	
k_1	0.026	0.037	0.66	0.94	2
L	0.375		9.53		1
L_1		0.050		1.27	1
Q	0.000	0.045	0.000	1.14	

NOTES

1. (All leads) ϕb applies between L and L_1. ϕb_1 applies between L_1 and 0.375″ (9.50 mm) from the reference plane. Diameter is uncontrolled in L_1 and beyond 0.375″ (9.50 mm) from the reference plane.
2. Measured from the maximum diameter of the product.
3. Leads having a maximum diameter 0.019″ (0.48 mm) measured in gaging plane 0.054″ (1.37 mm) + 0.001″ (0.03 mm) – 0.000″ (0.00 mm) below the base plane of the product is within 0.007″ (0.18 mm) of their true position relative to a maximum width tab.

J-44

44-Lead J-Leaded Chip Carrier



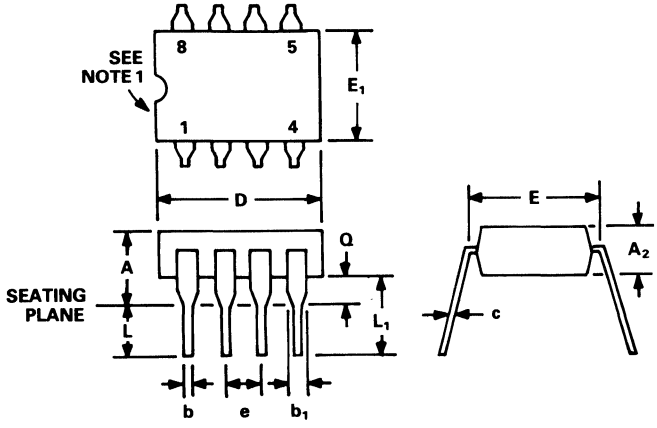
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.100	0.135	2.54	3.43	2
A1	0.054	0.078	1.37	1.98	
A2	0.025		0.64		
B	0.013	0.023	0.33	0.58	3
B1	0.020	0.032	0.51	0.81	3
C	0.006	0.013	0.15	0.33	3
D/E	0.680	0.700	17.27	17.78	
D1/E1	0.628	0.662	15.95	16.82	
D2/E2	0.250 BSC		6.35 BSC		
D3/E3	0.500 BSC		12.70 BSC		
D4/E4	0.610	0.650	15.49	16.51	
e	0.050 BSC		1.27 BSC		
e1/e2	0.012		0.30		
L	0.030		0.76		
L1	0.005		0.12		
L2	0.025		0.76		
Q	0.003		0.08		
R	0.015		0.38		
R1	0.025	0.040	0.76	1.02	
h	0.040 REF		1.02 REF		
j	0.020 REF		0.52 REF		

NOTES

1. **Pin 1 indicator is on the bottom of the package.**
2. **Dimension A controls the overall package thickness.**
3. **All leads–increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.**

N-8

8-Lead Plastic DIP
(P Suffix)

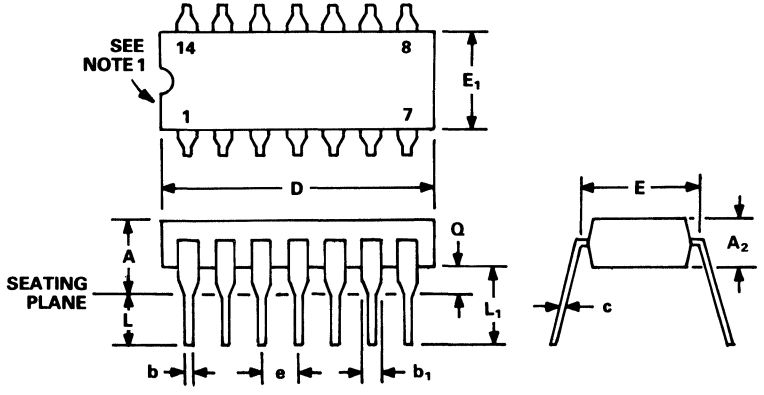


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.115	0.160	2.93	4.06	
L_1	0.130		3.30		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-14

14-Lead Plastic DIP
(P Suffix)

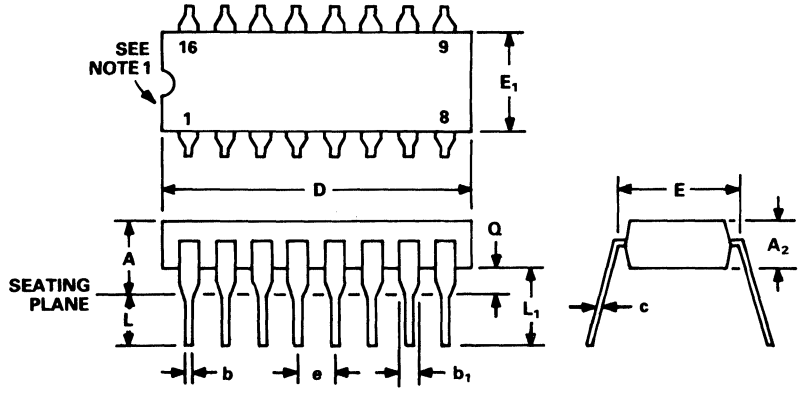


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.115	0.160	2.93	4.06	
L_1	0.130		3.30		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-16

16-Lead Plastic DIP
(P Suffix)

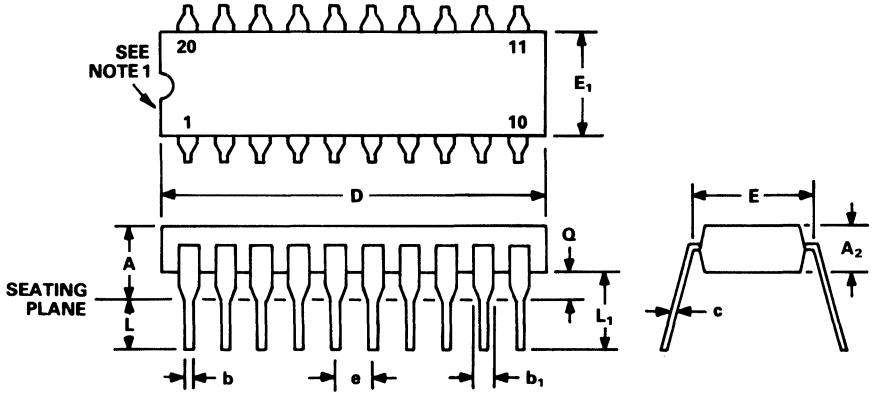


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.115	0.160	2.93	4.06	
L_1	0.130		3.30		
Q	0.015	0.060	0.38	1.52	

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. This dimension does not include mold flash or protrusions.

N-20

20-Lead Plastic DIP
(P Suffix)



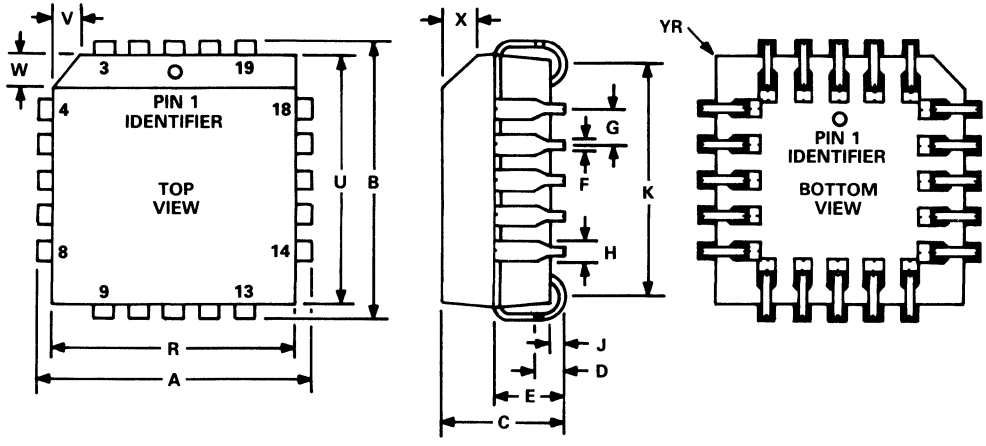
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.210		5.33	
A_2	0.115	0.195	2.93	4.95	
b	0.014	0.022	0.356	0.558	
b_1	0.045	0.070	1.15	1.77	
c	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.50	26.90	2
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.280	6.10	7.11	2
e	0.100 BSC		2.54 BSC		
L	0.115	0.160	2.93	4.06	
L_1	0.130		3.30		
Q	0.015	0.060	0.38	1.52	

NOTES

1. **Index area; a notch or a lead one identification mark is located adjacent to lead one.**
2. **This dimension does not include mold flash or protrusions.**

P-20A

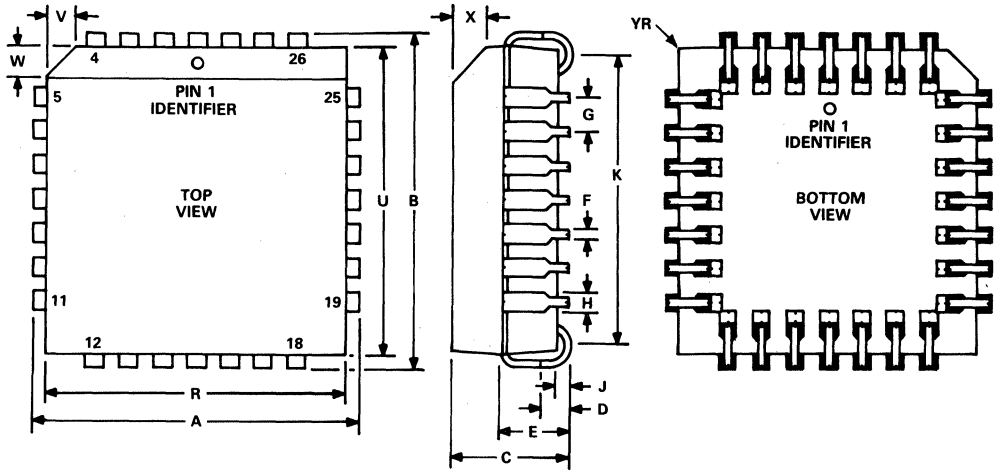
20-Lead Plastic Leaded Chip Carrier (PLCC)
(PC Suffix)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.02
B	0.385	0.395	9.78	10.02
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.290	0.330	7.37	8.38
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

P-28A

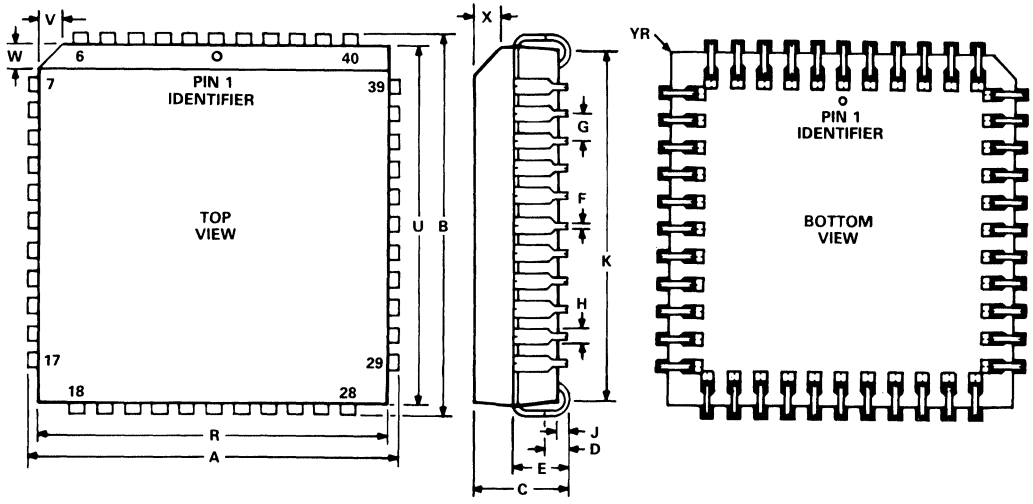
28-Lead Plastic Leaded Chip Carrier (PLCC)
(PC Suffix)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.390	0.430	9.91	10.92
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

P-44A

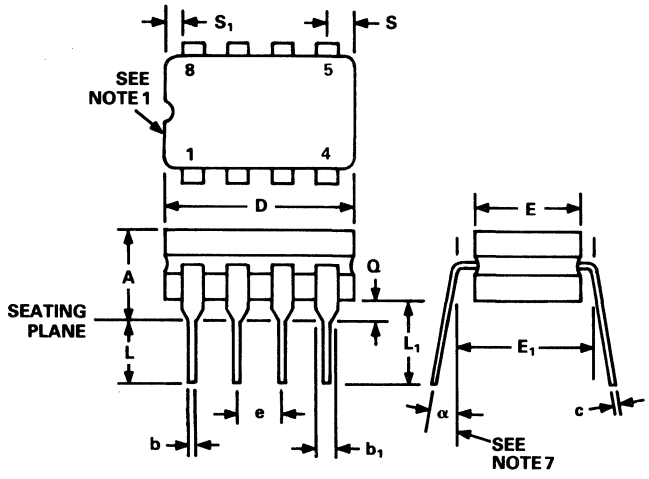
44-Lead Plastic Leaded Chip Carrier (PLCC)
(PC Suffix)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.19	4.57
D	0.025	0.040	0.64	1.01
E	0.085	0.110	2.16	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.015	0.025	0.38	0.63
K	0.59	0.63	14.99	16.00
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y		0.020		0.50

Q-8

8-Lead Cerdip
(Z Suffix)



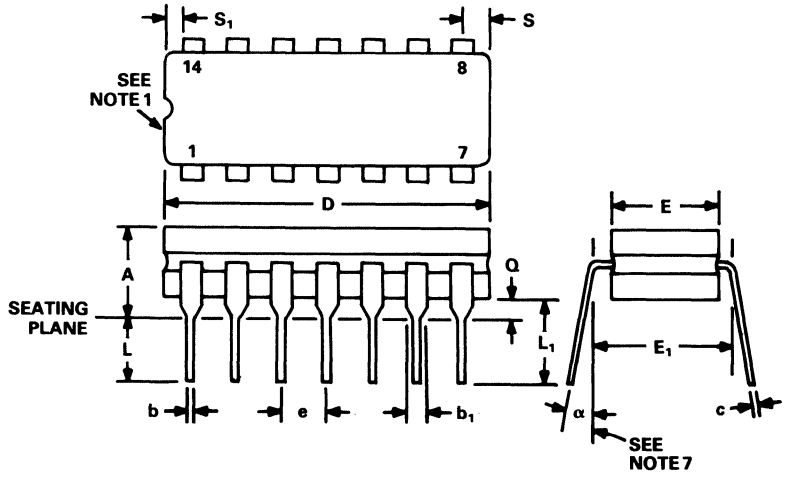
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.405		10.29	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.055		1.4	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Leads center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003″ (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Six spaces.

Q-14

14-Lead Cerdip
(Y Suffix)



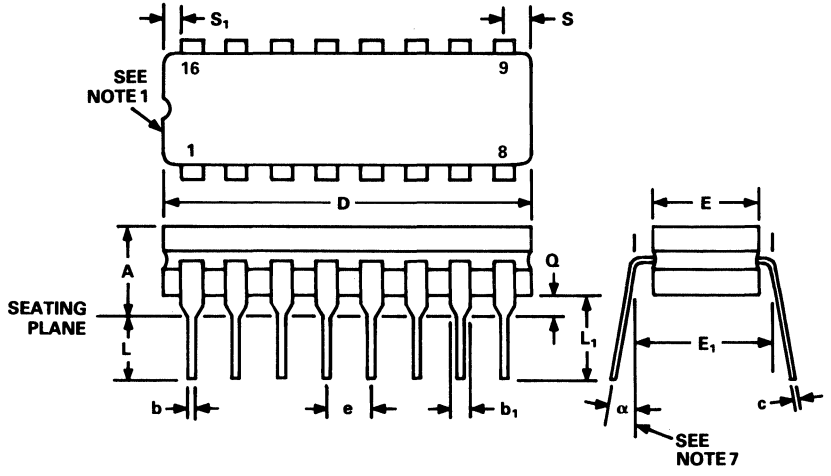
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.785		19.94	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat when hot solder dip lead finish is applied.
8. Twelve spaces.

Q-16

16-Lead Cerdip
(Q Suffix)



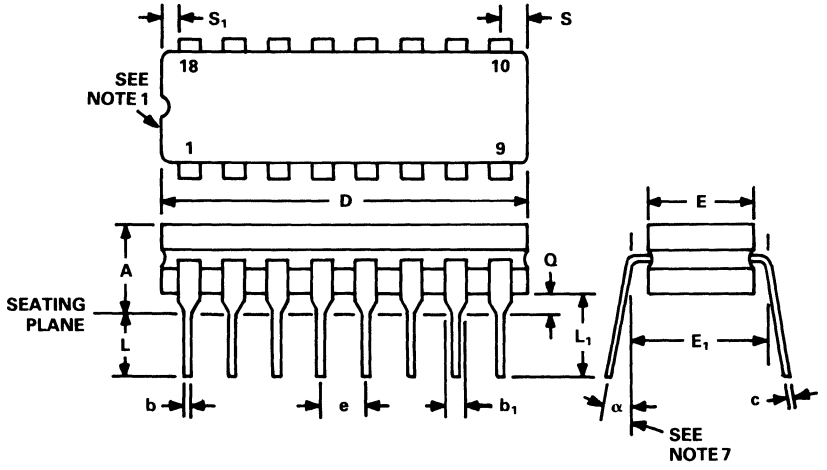
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.840		21.34	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.080		2.03	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003″ (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Fourteen spaces.

Q-18

18-Lead Cerdip
(X Suffix)



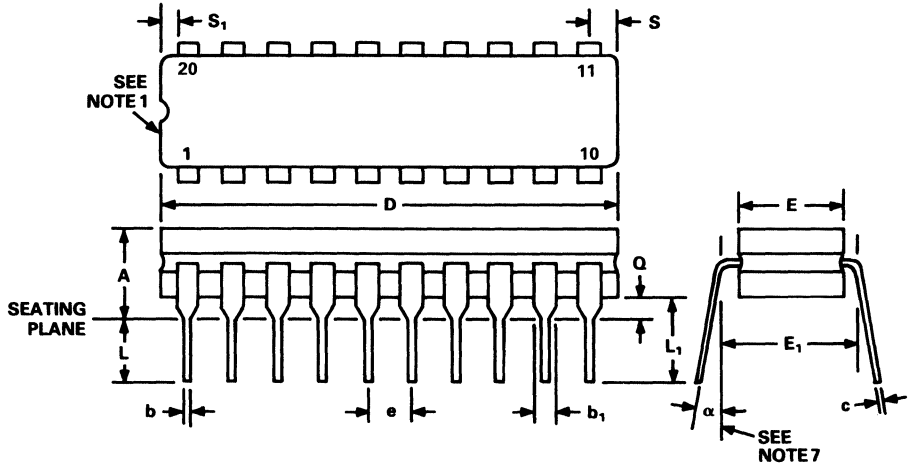
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		0.960		24.38	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Sixteen spaces.

Q-20

20-Lead Cerdip
(R Suffix)



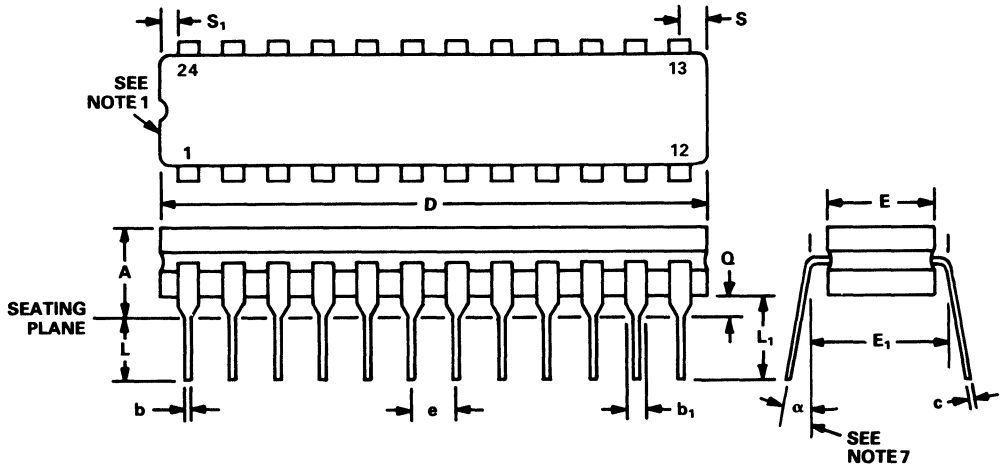
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		1.060		26.92	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003" (0.08 mm) measured at the center of the flat, when hot solder dip lead finish is applied.
8. Eighteen spaces.

Q-24

24-Lead Cerdip
(W Suffix)



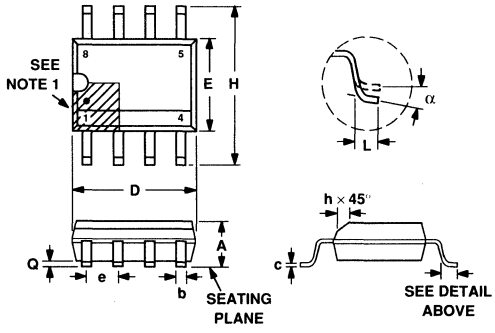
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.200		5.08	
b	0.014	0.023	0.36	0.58	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.015	0.20	0.38	7
D		1.280		32.51	4
E	0.220	0.310	5.59	7.87	4
E_1	0.290	0.320	7.37	8.13	6
e	0.100 BSC		2.54 BSC		8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	0.38	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTES

1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023″ (0.58 mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. All leads – increase maximum limit by 0.003″ (0.08 mm) measured at the center of the flat when hot solder dip lead finish is applied.
8. Twenty-two spaces.

R-8

8-Lead Narrow-Body (SO)



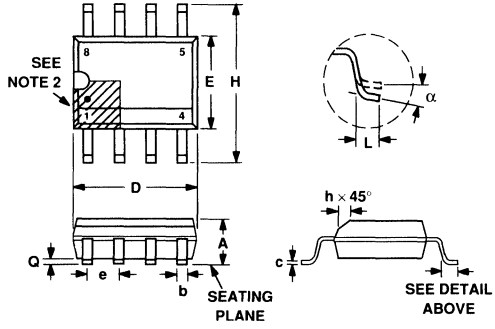
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.094	0.102	2.39	2.59	2
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**
2. **The R-8 and SO-8 packages differ only in this dimension.**

SO-8

8-Lead Narrow-Body SO
(S-Suffix)



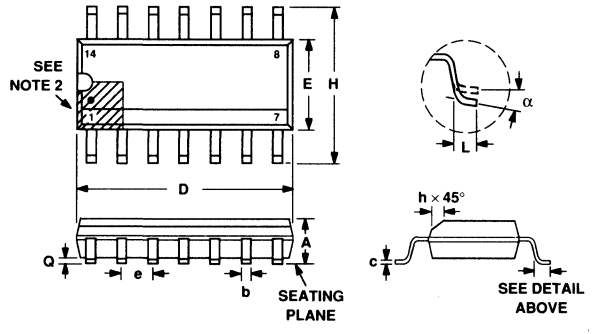
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	3
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-012-AA (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.
3. The SO-8 and R-8 packages differ only in this dimension.

SO-14

14-Lead Narrow-Body SO
(S-Suffix)



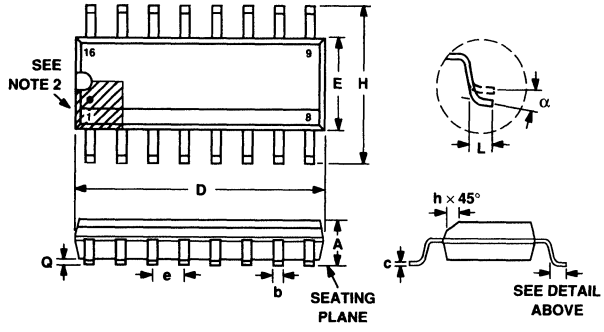
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-012-AB (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

R-16A
SO-16

16-Lead Narrow Body SO
(S Suffix)



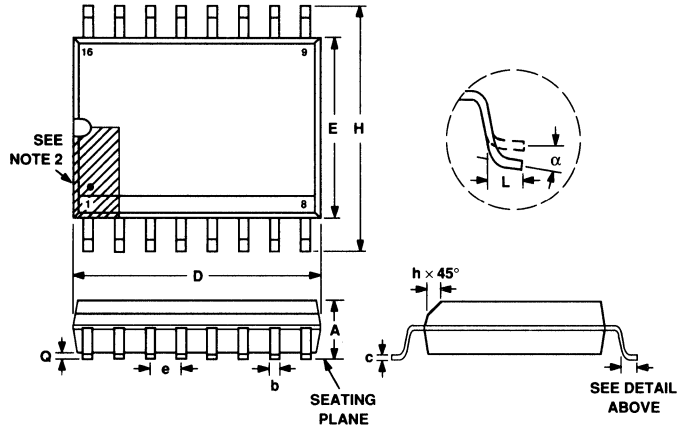
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	
b	0.0138	0.0192	0.35	0.49	
c	0.0075	0.0099	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	
E	0.1497	0.1574	3.80	4.00	
H	0.2284	0.2440	5.80	6.20	
e	0.0500 BSC		1.27 BSC		
h	0.0099	0.0196	0.25	0.50	
L	0.0160	0.0500	0.41	1.27	
Q	0.0040	0.0098	0.10	0.25	
α	0°	8°	0°	8°	

NOTES

1. **Package dimensions conform to JEDEC specification MS-012-AC (Issue A, June 1985).**
2. **Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.**

R-16
SOL-16

16-Lead Wide Body SO
(S Suffix)



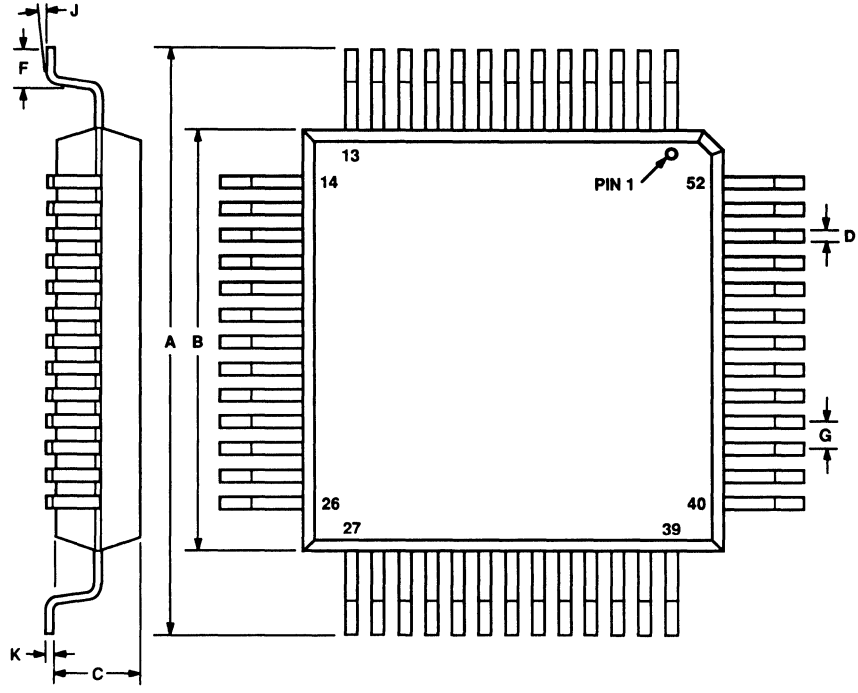
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	
b	0.0138	0.0192	0.35	0.49	
c	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	
E	0.2914	0.2992	7.40	7.60	
H	0.3937	0.4193	10.00	10.65	
e	0.0500 BSC		1.27 BSC		
h	0.0098	0.0291	0.25	0.74	
L	0.0157	0.0500	0.40	1.27	
Q	0.0040	0.0118	0.10	0.30	
α	0°	8°	0°	8°	

NOTES

1. Package dimensions conform to JEDEC specification MS-013-AA (Issue A, June 1985).
2. Index area; a dimple or lead one identification mark is located adjacent to lead one and is within the shaded area shown.

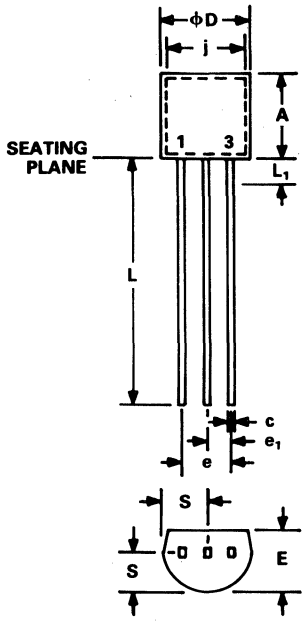
S-52

52-Lead Plastic Quad Flatpack



	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.537	0.557	13.65	14.15
B	0.390	0.398	9.9	10.10
C	0.078	0.082	1.97	2.09
D	0.010	0.014	0.25	0.35
F	0.026	0.037	0.65	0.95
G	0.0256 BSC		0.65 BSC	
J	0.006	0.008	0.15	0.20
K	0.006	0.012	0.15	0.30

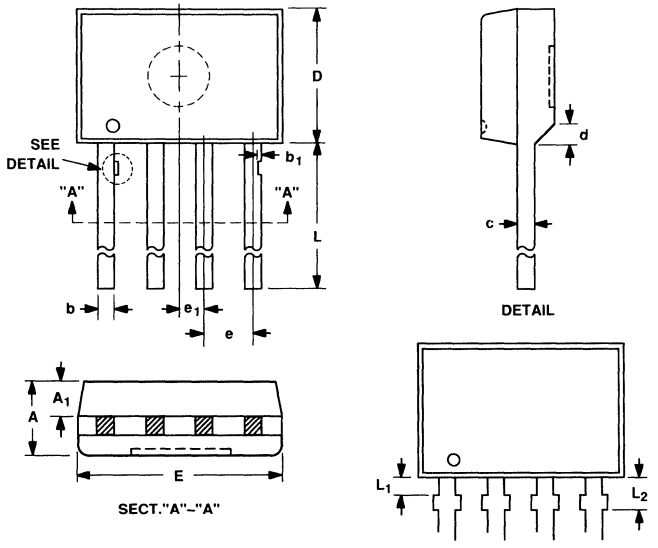
TO-92
3-Lead Plastic



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.170	0.210	4.58	5.33
c	0.016	0.019	0.407	0.482
ϕD	0.175	0.205	4.96	5.20
e	0.095	0.105	2.42	2.66
e_1	0.045	0.055	1.15	1.39
E	0.125	0.165	3.94	4.19
J	0.175	0.205	4.96	5.20
L	0.500		12.70	
L_1		0.050		1.27
S	0.080	0.105	2.42	2.66

Y-4

4-Lead Single In-Line Package (SIP)

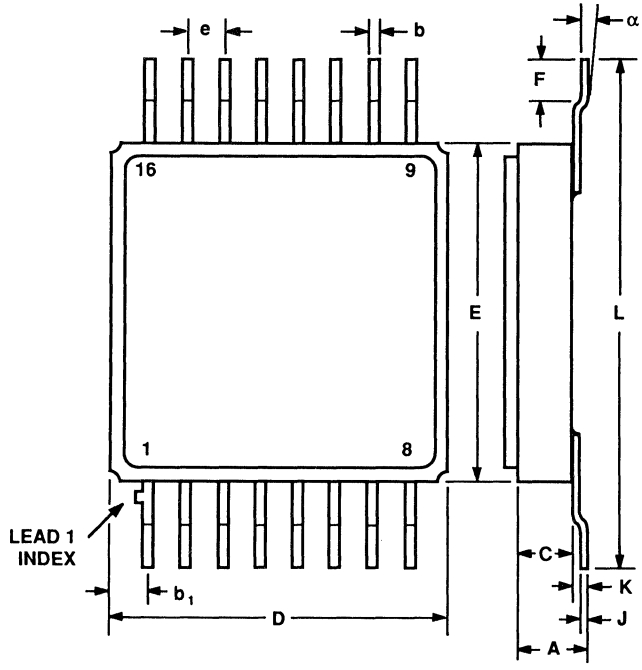


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.066	0.070	1.68	1.78	
A_1	0.035 BSC		0.89 BSC		
b	0.013	0.019	0.33	0.48	
b_1		0.003		0.076	
c	0.013	0.017	0.33	0.43	
D	0.125	0.135	3.17	3.43	
d	0.015	0.021	0.38	0.533	
E	0.196	0.204	4.98	5.18	1
e	0.05 BSC		1.27 BSC		
e_1	0.025 BSC		0.64 BSC		
L	0.500	0.530	12.70	13.46	
L_1	0.020 REF		0.51 REF		
L_2		0.040		1.02	

NOTES
1. Includes package mismatch.

Z-16A

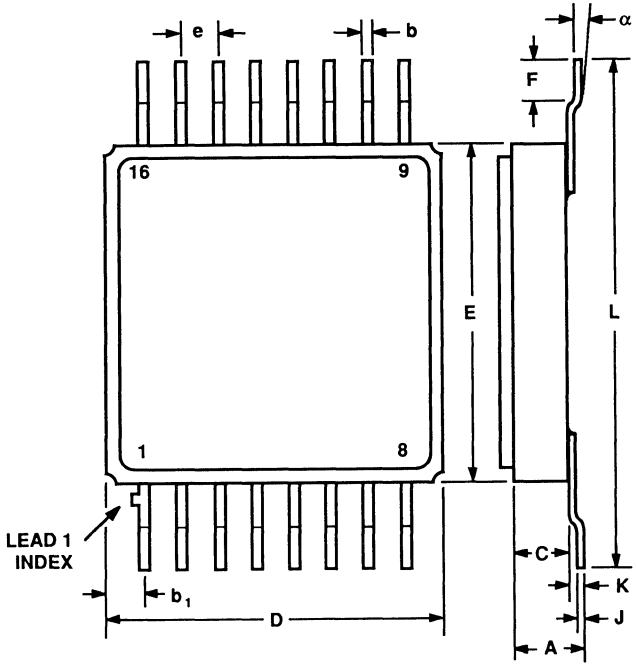
16-Lead Leaded Chip Carrier (Gull Wing)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.103	0.133	2.62	3.38
b	0.013	0.017	0.33	0.43
b_1	0.040	0.060	1.02	1.52
C	0.080	0.100	2.03	2.54
D	0.442	0.458	11.23	11.63
E	0.442	0.458	11.23	11.63
e	0.045	0.055	1.14	1.40
J	0.007	0.010	0.18	0.25
K	0.023	0.033	0.58	0.84
L	0.675	0.685	17.15	17.40
α	−5°	+5°	−5°	+5°

Z-16B

16-Lead Leaded Chip Carrier (Gull Wing–Wide)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.113	0.143	2.87	3.63
b	0.013	0.017	0.33	0.43
b_1	0.090	0.110	2.29	2.79
C	0.090	0.110	2.29	2.79
D	0.542	0.558	13.77	14.17
E	0.542	0.558	13.77	14.17
e	0.045	0.055	1.14	1.40
J	0.007	0.010	0.18	0.25
K	0.023	0.033	0.58	0.84
L	0.775	0.785	19.69	19.94
α	−5°	+5°	−5°	+5°

Appendix Contents

16

Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

In this reference manual many of the data sheets for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. Two model numbering schemes are used by Analog Devices. The first model numbering scheme is used for designating standard Analog Devices monolithic and hybrid products. The second scheme is used by our Precision Monolithics Division (formerly PMI) as designators for its product line.

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3-to-5-digit number,* an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows a different numbering scheme used by our Precision Monolithics Division. This numbering scheme starts with a prefix which designates the device type and model number. It is then followed by a suffix consisting of alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

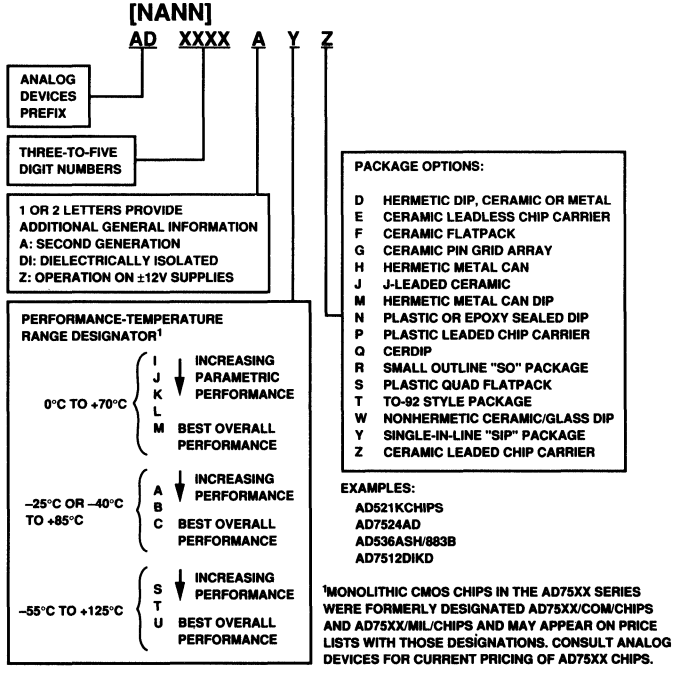


Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products. S, T and U Grades Have the Added Suffix, /883B for Devices that Qualify to the Latest Revision of MIL-STD-883, Level B.

***For some models, the combination [digit][letter] [two or three digits] is used instead of ADXXXX, e.g., 2S80.**

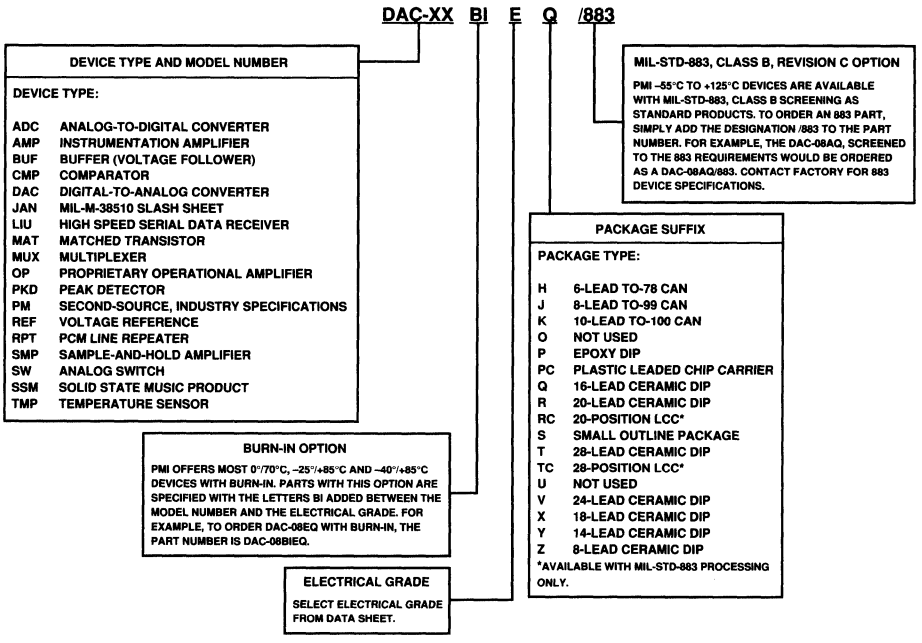


Figure 2. Precision Monolithics Division's Product Designations

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via fax or telex, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. Analog Devices' minimum order value is two hundred fifty dollars ($250.00).

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

You may also order Analog Devices parts through distributors. For information on distributors, please see pages 16–12 and 16–13 at the back of this volume.

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and μMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Product Families Not Included in the Reference Manual (But Still Available)

The information published in this Reference Manual is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs. Data sheets on these products are available upon request.

Model	Model	Model	Model
AD101	ADC-912	DAC1138	SW-01/02
AD201	ADC1130	DAC1146	SW-7510/7511
AD301	ADC1131	DAC-1408A	2B24
AD301AL	ADC1143	DAC1508A	2B34
AD363R	AD DAC-08	DAC-8212	2B52
AD364R	AD DAC71	DAS1153	2B53
AD503	AD DAC72	DAS1157	2B56
AD504	ADEB770	HDS-1240E	2B57
AD506	ADSP-1008A	HDS-1250	2B58
AD507SH/883B	ADSP-1009A	HOS-050/050A/050C	2B59
AD510	ADSP-1010A	HOS-060	4B Series
AD515	ADSP-1010B	HTC-0300A	40
AD518	ADSP-1012A	HTS-0010	171
AD533	ADSP-1016A	HTS-0025	233
AD535	ADSP-1024A	JM38510/11301/11302	277
AD545	ADSP-1080A	MUX-88	285
AD567	ADSP-1081A	OP-08	290
AD611	ADSP-1101	OP-43	292
AD651	ADSP-1110A	OP-44	310
AD689	ADSP-1401	OP-65	426
AD757	ADSP-1402	OP-111	429
AD1175	ADSP-1410	OP-147	434
AD1322	ADSP-3128A	OP-150	436
AD1403	ADSP-3201	OP-166	442
AD2004	ADSP-3202	PM-119	451
AD2006	ADSP-3210	PM-219	453
AD2020	ADSP-3211	PM-148/248	460
AD5200 Series	ADSP-3212	PM-155	741A
AD5210 Series	ADSP-3220	PM-156	751
AD7110	ADSP-3221	PM-157	756
AD7240	ADSP-3222	PM-355	947
AD7520	CAV-1210	PM-356	950
AD7521	CMP-08	PM-562	968
AD7522	CMP-404	PM-725	
AD7523	DAC-01	PM-741	
AD7525	DAC-02/03	PM-0820	
AD7530	DAC-05/06	PM-7541	
AD7531	DAC-12QS	PM-7574	
AD7541	DAC-20	SHA-1144	
AD7546	DAC71/72	SMP-81	
AD7576	DAC-86	SSM-2044	
AD7772	DAC-88	SSM-2045	
AD9502	DAC-89	SSM-2047	
AD9611	DAC-210	SSM-2100	
AD9686	DAC-888	SSM-2132	
ADC-908	DAC1136	SSM-2300	

Substitution Guide for Product Families No Longer Available

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but—as a rule—they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
AD108/208/308	AD705	AD2008	None	ADC-14I/17I	AD1170
AD108A/208A/308A	AD705	AD2009	None	ADC1100	AD1170
AD111/211/311	AD790	AD2016	None	ADC1102	AD7870
AD246	AD204/AD208	AD2022	None	ADC1103	AD7572A
AD295	AD210	AD2023	None	ADC1105	AD7550/AD7552
AD293	AD210	AD2024	None	ADC1109	AD7572A
AD294	AD210	AD2025	None	ADC1111	AD574A
AD345	AD1321/1324	AD2027	None	ADC1121	AD7880
AD351	AD790	AD2028	None	ADC1123	AD7880
AD362	AD1362	AD2033	None	ADC1133	AD574A
AD367	None	AD2036	None	ADC-QU	AD574A/AD674A
AD368	None	AD2037	None	AD DAC100	AD561
AD369	None	AD2038	None	ADG200	None
AD370/371	AD767	AD2040	None	ADG201	ADG201A
AD376	AD1376	AD2050	None	ADLH0032G/CG	AD843
AD381	AD744	AD2051	None	ADLH0033G/CG	AD9620/AD9630
AD382	AD744/AD845	AD2060	None	ADM501	None
AD386	AD1154	AD2061	None	ADP501	None
AD392	AD664	AD2070	None	ADREF01	REF-01
AD501	AD711	AD2071	None	ADREF02	REF-02
AD502	AD711	AD3554	None	ADSHC-85	AD585
AD505	AD509	AD3860	AD567	ADSHM-5	HTC-0300A
AD506SH/883B	AD42626	AD5010/6020	AD9000	AMP-01BX	AMP-01AX
AD508	AD517	AD5240	AD ADC85	AMP-01BX/883C	AMP-01AX/883C
AD511	AD711	AD6012	AD565A	AMP-05BX	AMP-05AX
AD512	AD711	AD7115	AD7111	AMP-05BX/883C	AMP-05Z/883C
AD513	AD711	AD7513	ADG201A	API1620/1718	Consult ADI
AD514	AD711	AD7516	AD7510DI	BDM 1615/16/17	None
AD516	AD711	AD7519	None	BUF-03BJ/883C	BUF-03AJ/883C
AD520	AD524	AD7527	AD7548	CAV-0920/1020	AD9020/9060
AD523	AD549	AD7544	AD7548	CAV-1202	AD9007
AD528	AD711/744	AD7550	None	CAV-1205	AD9007
AD530	AD533	AD7552	None	CMP-01Z	CMP-01J
AD531	AD532	AD7555	AD1175K	CMP-05BJ	CMP-05CJ
AD540	AD544	AD7560	None	CMP-05BZ	CMP-05CZ
AD559	AD557/AD558	AD7570	AD7579/AD7580	CMP-05GJ	CMP-05CJ
AD565	AD565A	AD7571	AD7579/AD7580	CMP-404BY	CMP-404AY
AD566	AD566A	AD7583	AD7880+MUX	CMP-404BY/883C	CMP-404AY/883C
AD612	AD524	AD9011	AD9002	DAC-02ACX1	DAC-02CCX1
AD614	AD524	AD9521	AD640	DAC-05AX1	DAC-02CCX1
AD801	AD711	AD9615	AD9611/AD9617	DAC-05EX1	DAC-02CCX1
AD1145	AD7846	AD9685	AD96685	DAC-10BX	DAC-10FX
AD1147/48	AD669	AD9687	AD96686	DAC-10CX	DAC-10GX
AD1332	None	AD9688	AD9002/AD9028	DAC-10DF	AD568
AD1408	AD558	AD ADC-816	AD7820/AD7821	DAC-10H	None
AD1508	AD558	ADC-8S	AD673	DAC-10Z	None
AD1678	AD678	ADC-10Z	AD574A	DAC-12QZ	AD667
AD1679	AD679	ADC-12QL	AD7578	DAC-12M	AD7845
AD1779	AD779	ADC-12QM	AD574A/AD674A	DAC-14QM	DAC1136
AD2003	AD2021	ADC-12QZ	AD574A/AD674A	DAC-16QM	DAC1136

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
DAC-100AAQ7	DAC-100ACQ7	HOS-100AH/SH	None	OP-12CZ	OP-12AZ
DAC-100AAQ8	DAC-100ACQ8	HOS-200	AD9620/30	OP-12GZ	OP-12FZ
DAC-100ABQ7	DAC-100ACQ7	HTC-0300	HTC-0300A	OP-14DZ	OP-14CZ
DAC-100ABQ8	DAC-100ACQ8	HTC-0500	HTC-0300A	OP-14GRBC	OP-14GBC
DAC-100BBQ5/ 883C	DAC-100ACQ5/ 883C	IPA-1751	IPA-1764	OP-14J/883C	OP-14AJ/883C
		IRDC1730-33	AD2S80A/82A	OP-15BJ	OP-15AJ
DAC-100BCQ7	DAC-100BBQ7	MAH-0801	AD9005	OP-15BZ	OP-15AZ
DAC-100DDQ7	DAC-100CCQ7	MAH-1001	AD9005	OP-16BJ	OP-16AJ
DAC-312BR	DAC-312ER	MAS-0801	AD9005	OP-17BZ/883C	OP-17AZ/883C
DAC-888AX	DAC-888EX	MAS-1001	AD9005	OP-17CJ	OP-17AJ
DAC-888BX	DAC-888EX	MAS-1202	AD9005	OP-17FJ	OP-17EJ
DAC1009	AD767	MAT-01/883C	MAT-01AH/883C	OP-17FZ	OP-17EZ
DAC1106	AD568	MAT-02BH	MAT-02AH	OP-20CJ	OP-20BJ
DAC1108	AD568	MAT-02BH/883C	MAT-02AH/883C	OP-21GRBC	OP-21GBC
DAC1112	DAC12QS	MATV-0811	AD9012/48	OP-215BJ	OP-215AJ
DAC1118	AD767	MATV-0816	AD9012/48	OP-215BJ/883C	OP-215AJ/883C
DAC1122	AD7541A	MATV-0820	AD9012/48	OP-215BZ	OP-215AZ
DAC1125	AD7533	MCI-1794	AD2S80A/82A	OP-215CZ/883C	OP-215BZ/883
DAC1132	AD667	MDA Family	AD9712B/13B	OP-21BJ	OP-21AJ
DAC-1408-6P	DAC-1408-8P	MDH Family	AD9712B/13B	OP-21BZ	OP-21AZ
DAC-1408-7P	DAC-1408-8P	MDMS Family	AD9712B/13B	OP-21EJ	OP-21AJ
DAC-1408-7Q	DAC-1408-8Q	MDS Family	AD9712B/13B	OP-220BJ	OP-220AJ
DAC-1408-GQ	DAC-1408-8Q	MDSL Family	AD9712B/13B	OP-22AJ	OP-22AJ/883C
DAC1420	None	MOD-1005/20	AD9020/60	OP-22EJ	OP-22AJ/883C
DAC1422	None	MUX-08AQ	MUX-08BQ	OP-32BZ	OP-32AZ
DAC1423	None	MUX-24AQ	MUX-24EQ	OP-32BZ/883C	OP-32AZ/883C
DAC1508A-8Q	DAC-1408-8Q	MUX-24BQ	MUX-24FQ	OP-32FZ	OP-32EZ
DAS1128	AD1341	MUX-16AT	MUX-16ET	OP-50BY	OP-50AY
DAS1150	None	MUX-16BT	MUX-16FT	OP-50BY/883C	OP-50AY/883C
DAS1151	None	OP-01HJ	OP-01J	OSC-1754	OSC-1758
DAS1155	None	OP-01HZ	OP-01HP	PKD-01BY	PKD-01AY
DAS1156	None	OP-02BJ	OP-02AJ	PKD-01BY/883C	PKD-01AY/883C
DRC1605/06	Consult ADI	OP-02BJ/883C	OP-02AJ/883C	PM-111Y	PM-111J
DRC1705/1706	Consult ADI	OP-02EJ	OP-07DJ	PM-11Y/883C	PM-111J/883C
DRC1765/66	AD2S65/66.	OP-02EP	OP-177GP	PM-139AY	PM-139AY/883C
DSC1605/06	Consult ADI	OP-02EZ	OP-177GZ	PM-156AZ	PM-156AZ/883C
DSC1705/1706	Consult ADI	OP-02J	OP-02AJ	PM-157J	PM-175J/883C
DSC1765/66	AD2S65/66	OP-02/883C	OP-02AZ/883C	PM-157J/883C	PM-157AJ/883C
DTM1716/17	AD2S65/66	OP-04DY	OP-04CY	PM-208AJ	PM-108AJ/883C
HAS-0802	HAS1202A	OP-04GBC	OP-04NBC	PM-208AZ	PM-108AZ
HAS-1002	HAS1202A	OP-04Y/883C	OP-04AY/883C	PM-308AZ	PM-1008GZ
HAS-1202	HAS1202A	OP-05Z	OP-05AZ	PM-308J	PM-1008G
HDD-1015	AD9712A	OP-05/883C	OP-05AZ/883C	PM-4136RC	OP-11ARC/883C
HDD-1409	None	OP-06BJ/883C	OP-06AJ/883C	PM-562AV	PM-562HV
HDG-0805	AD9701	OP-06EZ	OP-06GZ	PM-562BV	PM-562HV
HDH-0802	AD9713B	OP-06FZ	OP-06GZ	PM-562FV	PM-562HV
HDH-1003	AD9713B	OP-08AJ	PM-1008AJ	PM-562GV	PM-562HV
HDH-1205	AD9713B	OP-08AJ/883C	PM-1008AJ/883C	PM-741J	OP-02AJ
HDL-3805	ADV453/ADV478	OP-08AZ/883C	PM-1008AZ/883C	RAC1763	None
HDL-3806	ADV453/ADV478	OP-08CZ/883C	PM-1008AZ/883C	RDC1602/03	RDC1702/03
HDM-1210	AD668/AD9713B	OP-08EJ	PM-1008EJ	RDC1700	Consult ADI
HDS-0810E	AD9712B	OP-08EZ	PM-1008EZ	RDC1702	Consult ADI
HDS-0820	AD9713B	OP-09ARC/883C	OP-11ARC/883C	RDC1704	Consult ADI
HDS-1015E	AD9712B	OP-09FY	OP-09EY	RDC1711	None
HDS-1025	AD9713B	OP-12BZ	OP-12AZ	RDC1721	AD2S46

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
RDC1725	Consult ADI	2B35	None	280	281
RDC1726	Consult ADI	2S20	AD2S80A/82A	282J	292A
RDC1728	Consult ADI	5S70/5S72	AD2S75	283J	292A
RDC1767	Consult ADI	9S70/71/72	None	287	None
RDC1768	Consult ADI	9S75/76/79	None	288	AD210
RSCT1621	AD2S80A/82A	41	AD515A	301	310 (Module)
RTI-1200	RTI-711 Series	42	AD549	302	310 (Module)
RTI-1201	RTI-711 Series	43	AD549	311	AD549
RTI-1202	RTI-711 Series	44	AD845	350	None
RTM Series	Consult ADI	45	AD744	424	AD534
SAC1763	None	46	AD844	427	None
SBCD1752/53/56/57	None	47	AD845	428	AD538
SCDX1623	None	48	AD845	432	None
SCM1677	None	50	AD844	433	434
SDC1602/3/4	Consult ADI	51	AD844	435	AD734
SDC1700	Consult ADI	52	AD707	440	442
SDC1702	Consult ADI	102	AD845	450	AD652
SDC1703	Consult ADI	106	AD711	452	None
SDC1704	Consult ADI	107	AD711	454	AD537
SDC1711	None	108	AD845	456	AD537
SDC1721	AD2S46	110	AD845	458	460
SDC1725	Consult ADI	118	AD711	602J10	AD524
SDC1726	Consult ADI	120	AD844	602J100	AD524
SDC1728	Consult ADI	141	40	602K100	AD524
SDC1767	Consult ADI	142	AD845	603	AD524
SDC1768	Consult ADI	143	AD845	605	AD524
SERDEX	μMAC-5000	146	AD382	606	AD625
SHA-1A	AD585	148	AD549	610	AD625
SHA-2A	AD781	149	AD844	752	759
SHA-3	AD585	153	AD517	901	904
SHA-4	AD585	161	None	903	905
SHA-5	None	163	None	906	905
SHA-6	AD1154	165	None	907	921
SHA1114	AD585	170	None	908	921
SHA-1134	None	180	AD OP-07	909	921
SMP-10BY	SMP-10AY	183	AD707	915	904
SMP-10BY/883C	SMP-10AY/883C	184	AD707	926	927
SPA-1695	None	220	233	931	None
SSCT1621	AD2S80A/82A	230	233	932	None
SSCT1622/23	None	231	233	933	None
STM Series	Consult ADI	232	233	935	None
SW-01BQ	SW-01FQ	234	233	942	None
SW-7510AQ	SW-7510EQ	235	233	944	None
SW-7510BQ	SW-7510FQ	260	AD707	946	None
SW-7511AQ	SW-1577BQ	261	OP-177	948	947
THC-Family	HTC-0300A	272	None	951	None
THS-Family	HTC-0300A	273	None	952	970
TSL1612	Consult ADI	274J	284J	956	None
1S10/20	AD2S80A/82A	275	AD210	959	960
1S14/24/44/64/74	AD2S83	276	None	971	921
1S60/61	AD2S80A/82A	279	286J	972	974
				973	975

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Brief descriptions of typical publications appear below. For copies of any items, to subscribe to any of our free serials or to request any other publications, please get in touch with the nearest sales office or the Analog Devices literature center; phone (617) 461-3392, fax (617) 821-4273.

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DATA CONVERTER REFERENCE MANUAL—1992: Volumes 1 and 2. Data sheets and selection guides on A/D and D/A Converters, V/F and F/V Converters, Synchro/Resolver-to-Digital Converters, Sample/Track-Hold Amplifiers, Switches and Multiplexers, Voltage References, Data-Acquisition Subsystems, Analog I/O Ports, Communications Products, Bus Interface and I/O Products, Application-Specific ICs, Digital Panel Meters, Power Supplies. (Available FREE)

AUDIO/VIDEO REFERENCE MANUAL—1992. Data sheets and selection guides on Operational Amplifiers, Audio A/D and D/A Converters, Video A/D and D/A Converters, Special Function Audio Products, Special Function Video Products, and Digital Signal Processing Products, plus 42 Application Notes.

MILITARY PRODUCTS DATABOOK—1990 (in two volumes). Information and data on products available with processing in accordance with MIL-STD-883.

Volume 2: PMI Division products—including Class S
Volume 1: All other Analog Devices products

DATA-ACQUISITION AND CONTROL CATALOG—1990. Tutorial and Configuration Guide, with Product Reference and Index. Bus-Compatible I/O Boards for: IBM PS/2,* IBM PC/XT/ AT,* STD Bus, VMEbus, MULTIBUS.† Distributed I/O Subsystems—fixed-function front ends, programmable units, and distributed control systems. Modular Signal Conditioners—analog and digitizing. Analog Signal-Conditioning Panels—isolated and nonisolated. Digital Subsystems—16- and 24/32-channel. Software—DOS drivers and applications packages.

POWER SUPPLIES‡–Linear Supplies•DC-DC Converters. 12-page Short-Form Catalog listing AC/DC Power Supplies, Modular DC/DC Converters, Power-Supply Test Procedures, Transients, Thermal Derating, Mechanical Outlines of Packages and Sockets.

APPLICATION NOTES Available individually upon request:

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"Bipolar Operations with the AD7572" [E1010]
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"An Ultralow-Noise Preamplifier" [AN-136]
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"Applications of High-Performance BiFET Op Amps" [E727]
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"Using the AD9610 Transimpedance Amplifier" [E1097]
"Video VCAs and Keyers Using the AD843 and AD811" [AN-216]

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"A Function Generator and Linearization Circuit Using the AD7569" [E1369]
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"A Balanced Mute Circuit for Audio Mixing Consoles" [AN-122]
"A Constant-Power 'Pan' Control Circuit for Microphone Audio Mixing" [AN-123]
"A High-Performance Compandor for Wireless Audio Systems" [AN-133]
"An Automatic Microphone Mixer" [AN-134]
"A Two-Channel Dynamic Filter Noise Reduction System" [AN-125]
"High Performance Stereo Routing Switcher" [AN-121]
"Interfacing Two 16-Bit AD1856 (AD1851) Audio DACs with the Philips SAA7220 Digital Filter" [AN-207]

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"AD7528 Dual 8-Bit CMOS DAC" [E757]
"Analog Panning Circuits Provide Almost Constant Output Power" [AN-206]
"Circuit Applications of the AD7226 Quad CMOS DAC" [E873]
"Dynamic Performance of CMOS DACs in Modem Applications" [E1172]
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"Exploring the AD667 12-Bit Analog Output Port" [E875]
"Gain Error and Tempco of CMOS Multiplying DACs" [E630C]
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"Considerations for Selecting a DSP Processor" (ADSP-2100A vs. TMS320C25) [E1306]
"Considerations for Selecting a DSP Processor" (ADSP-2101 vs. TMS320C50) [AN-233]
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"Applying IC Sample-Hold Amplifiers" [E931]
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"ADG201A/202A and ADG221/222 Performance with Reduced Power Supplies" [E1052]
"Bandwidth, OFF Isolation, and Crosstalk Performance of the ADG5XXAA Multiplexer Series" [E1340]
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"Changing Your VGA Design from a 171/176 to an ADV471" [E1260]

"Design and Layout of a Video Graphics System for Reduced EMI" [E1309]

"Improved PCB Layouts for Video RAM-DACs Can Use Either PLCC or DIP Package Types" [E1225]

"Low Cost Two-Chip Voltage-Controlled Amplifier and Video Switch." (AD539) [AN-213]

"Video Formats & Required Load Terminations." [AN-205]

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1992 Short Form Designers' Guide. A 142-page summary of Analog Devices products, including data converters, amplifiers, transducers, audio/video components, voltage references, switches and multiplexers, data-acquisition subsystems—and components for analog and digital signal processing, audio/video, disk drives, automotive electronics, ATE, and communications. It features new-product descriptions, specifications, and block diagrams—and provides selection guides, selection trees, and characteristics tables, plus a comprehensive index to all products.

Analog CMOS Switches and Multiplexers. A 16-page short form guide to high-speed CMOS switches, CMOS switches with dielectric isolation and CMOS multiplexers. Also included are reliability data and information on single-supply operation.

Applications Guide for Isolation Amplifiers and Signal Conditioners. A 20-page guide to specifications and applications of galvanically isolated amplifiers and signal conditioners for industrial, instrumentation and medical applications.

CMOS DAC Application Guide 3rd Edition by Phil Burton (1989—64 pages). Introduction to CMOS DACs, Inside CMOS DACs, Basic Application Circuits in Current-Steering Mode, Single-Supply Operation Using Voltage-Switching Mode, The Logic Interface, Applications.

Digital Signal Processing—a 20-page brochure outlining the Analog Devices approach to DSP, mixed-signal processing and signal computing. Includes philosophies, fixed- and floating-point architectures, products, benchmarks, applications, tools (hardware, software, and third-party), support—and migration paths to the future.

ESD Prevention Manual—Protecting ICs from electrostatic discharges. Thirty pages of information that will assist the reader in implementing an appropriate and effective program to ensure protection against electrostatic discharge (ESD) failures.

High-Speed Data Conversion. A 24-page short-form guide to video and other high-speed A/D and D/A converters and accessories, in forms ranging from monolithic ICs to card-level products.

High-Speed Op Amp Selection Guide. A 4-page quick-reference chart outlining specs and characteristics of high-speed op amps, further subdivided into precision, low-noise, FET-input, transimpedance, general-purpose and buffer classifications. Includes a worldwide sales directory.

Instrumentation Amplifier Application Guide, by Charles Kitchin and Lew Counts. Its 44 pages include basic instrumentation-amplifier ("in-amp") theory, design considerations, applications, specifications, and products—plus a brief bibliography and two indexes (by topic and by device model number).

Multiple Digital-to-Analog Converter Integrated Circuits Selection Guide. A 32-page guide for the designer who wants to save space and cost in applications calling for from two to eight or more DACs and resolutions from 6 to 18 bits. Devices include triple 6-, 8-, and 10-bit video DACs, dual 18-bit audio DACs, 8-bit octuples, and 12- and 14-bit quads.

Resolver-to-Digital Converter Selection Chart. A 40-page collection of accuracy and speed data for use in the design of systems combining Analog Devices monolithic integrated-circuit RDCs with a variety of resolvers. Topics include single- and multi-speed resolvers, speed-accuracy charts, resolver charts for nine different manufacturers, and definitions of terms.

RMS-to-DC Conversion Application Guide 2nd Edition by C. Kitchin and L. Counts (1986—61 pages). RMS-DC Conversion: Theory, Basic Design Considerations; RMS Application Circuits; Testing Critical Parameters; Input Buffer Amplifier Requirements; Programs for Computing Errors, Ripple and Settling Time.

Sampling Analog-to-Digital Converter Integrated Circuits—1992 Short-Form Selection Guide. Its 28 pages cover 35 different models with resolutions from 8 to 16 bits, and 12-bit resolution up to 20 MSPS. Besides block diagrams and key specs of each product, the booklet includes a detailed discussion of selection issues and a selection table sorted by resolution and speed.

Signal Computing. A 16-page brochure describing the present and future of product designs that require synchronous, real-time execution of complex mathematical signal-processing algorithms. In it, chipsets (e.g., a DSP teamed with appropriate analog ports) provide the hardware platform; and prepackaged third-party software, written by experts in a variety of fields (but modified to meet the needs of individual designs) provides the problem-solving configuration. So (for example) the same processor can be used as a PC-based sound coprocessor, or an embedded audio processor in digital TVs, or a host processor in digital cellular telephones. Some illustrations are provided, using Analog Devices products.

*Surface Mount IC.** A 28-page guide to ICs in SO and PLCC packages. Products include op amps, rms-to-dc converters, DACs, ADCs, VFCs, sample-holds and CMOS switches.

DIGITAL SIGNAL PROCESSING MANUALS

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ADSP-2101/ADSP-2102 USER'S MANUAL—Architecture. [Fixed-point processor] Introduction; Computational Units; Data Moves, Program Control; Timer; Serial Ports; System Interface; Memory Interface; Instruction Set Overview; Appendixes; Index. 190 pages.

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ADSP-21020 USER'S MANUAL. [Floating-point processor] Introduction; Computational Units; Program Sequencing; Data Addressing; Timer; Memory Interface; Instruction Summary; Assembly Programmer's Tutorial; Hardware System Configuration; Appendixes; Index. 394 pages.

TECHNICAL REFERENCE BOOKS

Can be purchased from Analog Devices, Inc., at the prices shown. If more than one book is ordered, deduct a discount of $1.00 from the price of each book. Price of the entire set of 10 books is $177.00—a bargain for your department's library (in effect, the Amplifier Applications and High-Speed books come free). VISA and MasterCard are welcome; phone (617) 461-3392 or fax (617) 821-4273. Or send your check for the indicated amount to Analog Devices, Inc., P.O. Box 9106, Norwood, MA 02062-9106.

NEW—*AMPLIFIER APPLICATIONS GUIDE*, by the Applications Engineering Staff of Analog Devices and edited by Walt Kester, published by Analog Devices (1992). 648 pages of timely and practical information on amplifiers—including operational, audio, instrumentation, video, and log amps. Topics include: Introduction; Precision transducer interfaces; High-impedance, low current; Single-supply, low-power; Audio; Filtering, Driving ADCs; Video and other high-speed applications; Nonlinear circuit applications; Unusual applications; Subtleties; Hardware techniques; Simulation; and a complete Index. $20.00

ANALOG-DIGITAL CONVERSION HANDBOOK: Third Edition, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice Hall (1986). A comprehensive guide to A/D and D/A converters and their applications. This third edition of our classic is in hardcover and has more than 700 pages, an Index, a Bibliography, and much new material, including: video-speed, synchro-resolver, V/F, high-resolution, and logarithmic converters, ICs for DSP, and a "Guide for the Troubled." Seven of its 22 chapters are totally new. $32.95

DIGITAL SIGNAL-PROCESSING APPLICATIONS USING THE ADSP-2100 FAMILY, by the Applications Staff of Analog Devices, DSP Division; edited by Amy Mar (628 pages). Englewood Cliffs NJ: Prentice Hall (1990). Bridge the gap between DSP algorithms and their real-world implementation on state-of-the-art signal processors. Each chapter tackles a specific application topic, briefly describing the algorithm and discussing its implementation on the ADSP-2100 family of DSP chips. Comprehensive source-code listings are complete with comments and accompanied by explanatory text. Programs are listed on a pair of supplementary diskettes—furnished with the book. Application areas include fixed- and floating-point arithmetic, function approximation, digital filters, one- and two-dimensional FFTs, image processing, graphics, LP speech coding, PCM, ADPCM, high-speed modem algorithms, DTMF coding, sonar beamforming. Additional topics include memory interface, multiprocessing, and host interface. The book can serve as a companion to *Digital Signal Processing in VLSI*. **Now in paperback**; its price includes a diskette.

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DIGITAL SIGNAL PROCESSING IN VLSI, by Richard J. Higgins. Englewood Cliffs NJ: Prentice Hall (1990). An introductory 614-page guide for the engineer and scientist who needs to understand and use DSP algorithms and special-purpose DSP hardware ICs—and the software tools developed to carry them out efficiently. Real-World Signal Processing; Sampled Signals and Systems; The DFT and the FFT Algorithm; Digital Filters; The Bridge to VLSI; Real DSP Hardware; Software Development for the DSP System; DSP Applications; plus Bibliography and Index. $38.00

DIGITAL SIGNAL PROCESSING LABORATORY Using the ADSP-2101 Microcomputer, by Vinay K. Ingle and John G. Proakis (Northeastern University). Englewood Cliffs NJ: Prentice Hall (1991). Contents: Introduction to the ADSP-2100/2101 family; ADSP-2101 instruction set overview; Overview of development tools; Getting started with the ADSP-2101; Laboratory experiments using the ADSP-2101; FIR filter implementation; IIR filter implementation; Fast Fourier transform implementation; Applications in communications; Adaptive filters and their applications; References; Index. $24.00

HIGH-SPEED DESIGN SEMINAR, published by Analog Devices (1990). A 496-page guide to the practical application of high-speed semiconductor devices in processing of analog signals. Topics include: data conversion, digital video applications, high-speed sample-holds and operational amplifiers, nonlinear signal processors (including log amps), comparators and pin electronics, time-delay generators, phase-locked loops, direct digital synthesis, computer graphics and RAMDACs, and high-speed techniques. $20.00

MIXED-SIGNAL DESIGN SEMINAR, published by Analog Devices (1991). Contents: Introduction to mixed-signal processing of real-world signals and signal conditioning; Linear and nonlinear analog signal processing; Fundamentals of sampled-data systems; ADCs for DSP applications; DACs for DSP applications; Sigma-delta ADCs and DACs; Digital signal-processing techniques; DSP hardware; Interfacing ADCs and DACs to digital signal processors; Mixed-signal processing applications; Mixed-signal circuit techniques; Index. $22.00

NONLINEAR CIRCUITS HANDBOOK: Designing with Analog Function Modules and ICs, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1974). A 540-page guide to multiplying and dividing, squaring and rooting, rms-to-dc conversion, and multifunction devices. Principles, circuitry, performance, specifications, testing, and application of these devices–contains 325 illustrations. $5.95

SYNCHRO & RESOLVER CONVERSION, edited by Geoff Boyes. Norwood, MA; Analog Devices, Inc. (1980). Principles and practice of interfacing synchros, resolvers, and Inductosyns* to digital and analog circuitry. $11.50

TRANSDUCER INTERFACING HANDBOOK: A Guide to Analog Signal Conditioning, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1980). A book for the electronic engineer who must interface transducers for temperature, pressure, force, level, or flow to electronics, these 260 pages tell how transducers work—as circuit elements—and how to connect them to electronic circuits for effective processing of their signals. $14.50

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Product Index

Alphanumeric by Model Number

*New product.

†A = *Amplifier Reference Manual*; AV = *Audio/Video Reference Manual*; C I = *Data Converter Reference Manual, Volume I*; C II = *Data Converter Reference Manual, Volume II*; D = *Data Sheet*; ; SL = *Special Linear Reference Manual*.

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