Data Book

AT&T

Communication Devices

1988

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January 1988

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A Word About Trademarks . . .

The following product mentioned in this data book is identified with an AT&T trademark:

ESS™ Switching Equipment

The following products mentioned in this data book are identified with AT&T registered trademarks:

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WE® DSP16 Digital Signal Processor
WE® DSP16-DS Digital Signal Processor Development System
WE® DSP16-SL Support Software Library
WE® DSP20 Digital Signal Processor
WE® DSP32 Digital Signal Processor
WE® DSP32-DS Digital Signal Processor Development System, or DSP Development System
WE® DSP32-SL Support Software Library
SLC® Carrier System, or Carrier
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ODL® 50 Lightwave Data Link
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Data sheets without a status marking are final and are issued when tool made samples are approved or when the product is delivered for usage, whichever occurs first. The other data sheet status markings used throughout this catalog are defined as:

Advance – Issued at the exploratory stage of development when the principal characteristics are available. Some functional characteristics are subject to change.

Preliminary – Issued after development for manufacture has been started. Some electrical and timing parameters are subject to change.

1988 Communication Devices Data Book

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5. ISDN Primary Rate/T1

6. Signal Processing

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1. General

Introduction

For more than a century, AT&T has set the standard for information exchange. AT&T innovation and excellence have created the most extensive, efficient, and reliable communication system in the world. This sophisticated voice and data communication system demands components of superior technology, quality, and reliability.

AT&T manufactures integrated circuits specifically designed to meet the needs of the communications market. The strong research and design capabilities of AT&T Bell Laboratories, combined with the high-volume, high-quality manufacturing capabilities of AT&T Technology Systems, allow AT&T to maintain the leading edge in advanced technology devices.

In this new Information Age, the telephone and the computer are becoming one, and AT&T is building upon this merger with new products and services. New devices have been developed to interface these two complex fields into a highly flexible and reliable network. This catalog contains the technical information on devices used for switching, analog and digital transmission, data transmission and protocol control, T1 interfacing, integrated services digital network (ISDN) interfacing, and signal processing.

Quality and Reliability

AT&T standards and stringent processing controls, along with the design and construction techniques developed at AT&T Bell Laboratories, ensure the excellent quality and reliability of AT&T devices. Laboratory tests and field failure data confirm that high-quality, reliable AT&T products are produced at the component, circuit pack/board, and system levels. Devices are tested by comparing the actual electrical, mechanical, and visual properties of the device to user specifications and manufacturing requirements. Quality is determined at a single point in time; reliability is ascertained over a longer period of time.

The engineering quality control (QC) and final inspection (FI) organizations located at each integrated circuit (IC) manufacturing plant perform the actual inspection and testing of devices. After the products have been inspected, the resident quality assurance (QA) organizations audit the results of the tests to determine acceptability. Quality is usually stated in terms of the number of defects contained in an IC population.

Various mechanical tests are performed to ensure the integrity of internal lead bonds and the strength of exterior leads. Packages are visually inspected during assembly to check for such reliability risk defects as poor alignment of bonds or damaged wires. Assembly shop tests are repeated by QA and FI on a sample of devices prior to shipment. Tests performed include worst-case conditions, speed, leakage, power supply current, etc. The tests are usually performed at room temperature and/or elevated temperature.

Operational life testing (OTL), based on simulated worst-case field conditions, is used to test reliability. Mechanical and electrical stress conditions beyond normal specifications are applied to accelerate latent manufacturing defects. Since some mechanical defects are only minimally affected by accelerated stress conditions, mechanical problems are effectively screened by thermal cycling and hot testing.

Handling and Mounting

AT&T products have a long life expectancy and a correspondingly low failure rate when handling and operating specifications are followed by the user. Operating specifications include product mounting, use, operating limits, power requirements, environmental conditions, and other items specific to the product. Device temperature specifications are usually given as T_A (ambient temperature); however, in a few cases, they are given as T_C (case temperature).

Precaution against static discharge must always be observed since devices may be damaged or destroyed by electrostatic discharge. This includes grounding all personnel and equipment before contact with static-sensitive devices. Circuit packs/boards must be shipped in and stored in conductive plastic bags. Nonconductive plastic foam or boxes must never be used for device storage.

Integrated circuit devices can be inserted directly into printed circuit boards and mounted in any position. The leads on the opposite side of the board can be bent to facilitate assembly. Devices can be soldered to printed circuit boards or inserted into sockets but are not intended for spring-type socket insertion.

In solder bath assembly, the solder bath fountain temperature should not exceed 300 °C for a maximum bath time of 10 seconds, unless otherwise stated. For assembly with a soldering iron, the soldering iron tip temperature should not exceed 500 °C, and solder time per lead should be limited to 5 seconds, unless otherwise stated.

Following completion of assembly and soldering operations, all printed wiring assemblies should be cleaned to remove fingerprints, dust, dirt, grease, excessive flux residue, and other foreign matter. Hybrid ICs require a special cleaning process (see below). A brush cleaning process using solvents is an acceptable cleaning method, provided only occasional isolated droplets of solvent come in contact with the devices and the component side of the board. The recommended solvents are such chlorinated hydrocarbons as trichloroethylene, 1,1,1-trichloroethane, and perchloroethylene.

Where aggressive fluxes are employed in assembly of printed wiring, total immersion cleaning with high-velocity spraying of an aqueous solution or such solvents as fluorinated azeotrope is required. Stringent requirements must be placed on the cleanliness of the assemblies to assure removal of ionic residues.

Handling Hybrid ICs

Additional handling procedures are required for Hybrid ICs. Hybrid ICs are encapsulated with a single layer of RTV silicone rubber. This material is solvent-sensitive and special precautions are required in removing solder flux residues from printed circuit boards containing these devices. Unless otherwise designated by specific agreement with the responsible AT&T organizations, cleaning procedures must fall within the conditions that follow.

Cleaning Procedure

Cleaning processes that avoid contact between solvents and the room temperature vulcanizing (RTV) silicone rubber are preferred. The following cleaning constraints should be observed:

CAUTION: It is recommended that these devices be subjected to either of the following procedures only once. Repeated exposure may yield cumulative effects that result in device damage.

1. Brush cleaning processes are acceptable, provided that only occasional isolated droplets fall on areas of the devices and the component side of the board.
2. RTV areas in which solvent can be trapped should be cleaned by using one of two types of solvents:
   a. Immersion of one minute maximum in Freon TE or Freon TE-35 or equivalents followed by:
      - Forced air drying or shaking to remove excess liquid solvent
      - Transferring to an air oven in one minute or less
      - Baking for 15 minutes at 55 °C
   b. Specially denatured alcohol (SDA), which contains between 5% and 30% methyl alcohol. May be used for a cumulative exposure time of 10 minutes.

2. Network

41LF Quad Differential Line Receiver

Features

- Pin-equivalent to the general-trade AM26LS32 device, with improved speed and reduced power consumption
- Four line receivers per package
- Meets ESDI Standards
- Complementary inputs for each line receiver
- Maximum power dissipation, 250 mW
- Maximum propagation delay, 7 ns
- 0.20 V input sensitivity
- Common mode rejection range of ±4 V
- Single 5 V supply
- 0 to 85 °C operating temperature

Description

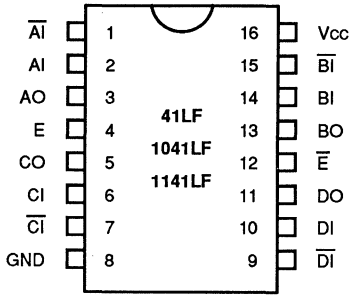
The 41LF Quad Differential Line Receiver integrated circuit is a quad differential input to a TTL output line receiver. This OXIL-technology device contains enable circuitry and four receiver clusters. The average propagation delay is 4 ns and the common mode operating range is ±4 V. The 41LF Line Receiver is pin-equivalent to the general-trade AM26LS32 device, but has improved speed and reduced power consumption.

The quad differential line receiver is available in a 16-pin plastic DIP (41LF), SOJ package (1041LG), and SOIC package (1141LG).

The *41LG Line Driver and 41LF Line Receiver* application note (AP86-35DBIP) describes two modes of propagation with balanced twisted-pair transmission lines.

User Information

Pin Descriptions



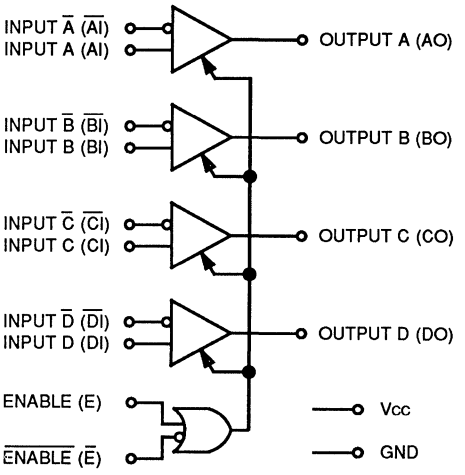


Figure 1. Pin Function and Logic Diagrams

Characteristics

Electrical Characteristics

T_A = 0 to 85 °C, V_{CC} = 5 V ± 0.5 V

Parameter	Sym	Min	Typ	Max	Unit
Output voltage, V_{CC} = 4.5 V:					
low, I_{OL} = 8 mA	V_{OL}	—	—	0.5	V
high, I_{OH} = –400 μA	V_{OH}	2.5	—	—	V
Enable input voltages:					
low, V_{CC} = 5.5 V	V_{IL}*	—	—	0.7	V
high, V_{CC} = 4.5 V	V_{IH}*	2.0	—	—	V
clamp, V_{CC} = 4.5 V; I_{IN} = –18 mA	V_{IK}	—	—	–1.5	V
Differential input voltages,** V_O = V_{OL} or V_{OH}, –0.80 V < V_{IH} < 7.2 V, –1.2 V < V_{IL} < 6.8 V	V_{TH}*	0.2	0.1	—	V

* These input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.

** Unused differential input pairs should be biased alternately to Vcc and GND. No protection resistor is required.

Parameter	Sym	Min	Typ	Max	Unit
Output currents, V_{CC} = 5.5 V:					
off-state (high-Z), V_O = 0.4 V	I_{OZL}	—	—	20	μA
off-state (high-Z), V_O = 2.4 V	I_{OZH}	—	—	20	μA
short-circuit	I_{SC}	–25.0	—	–100	mA
Enable input currents, V_{CC} = 5.5 V:					
low, V_{IN} = 0.4 V	I_{IL}	—	—	–360	μA
high, V_{IN} = 2.7 V	I_{IH}	—	—	20	μA
reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	μA
Differential input currents:					
low, V_{IN} = –1.2 V	I_{IL}	—	—	–1.0	mA
high, V_{IN} = 7.2 V	I_{IH}	—	—	1.0	mA
Power supply current, V_{CC} = 5.5 V					
all outputs disabled	I_{CC}	—	35	45	mA

Maximum Ratings

DC power supply voltage (V_{CC}) ..... 7.0 V
Ambient operating temperature (T_A) range ..... 0 to 125 °C
Storage temperature (Tstg) range ..... –40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

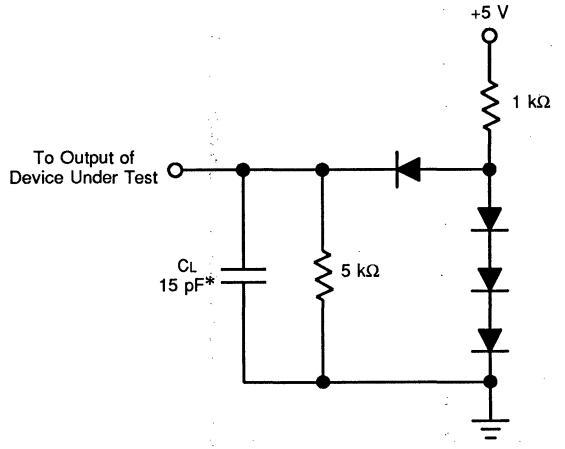
External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics (See Figures 4 and 5)

T_A = 25 °C, V_{CC} = 5 V

Symbol	Description	Typ	Max	Unit
	Propagation delay (see Figure 2):			
t_{PLH}	input high (low) to output high	3.5	7.0	ns
t_{PHL}	input low (high) to output low	4.5	7.0	ns
	Disable time:*			
t_{PHZ}	high to high impedance	30	—	ns
t_{PLZ}	low to high impedance	30	—	ns
	Enable time:*			
t_{PZH}	high impedance to high	35	—	ns
t_{PZL}	high impedance to low	35	—	ns

* The device is disabled when E = 0 and $\bar{E}$ = 1; all other combinations of E and $\bar{E}$ enable the device.



Note: All 458E or 1N4148 diodes.
* Includes probe and jig capacitances.

Figure 2. Output Voltage and Propagation Delay Test Circuit

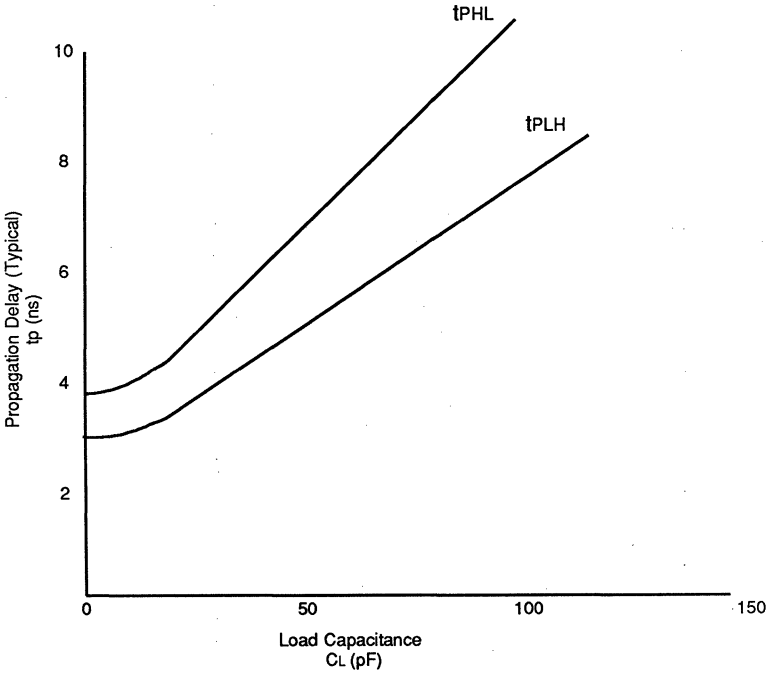


Figure 3. Propagation Delay Versus Load Capacitance

Timing Diagrams

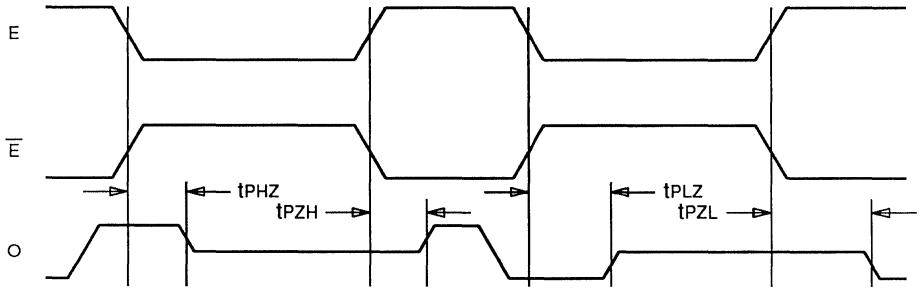


Figure 4. Enable and Disable Timing

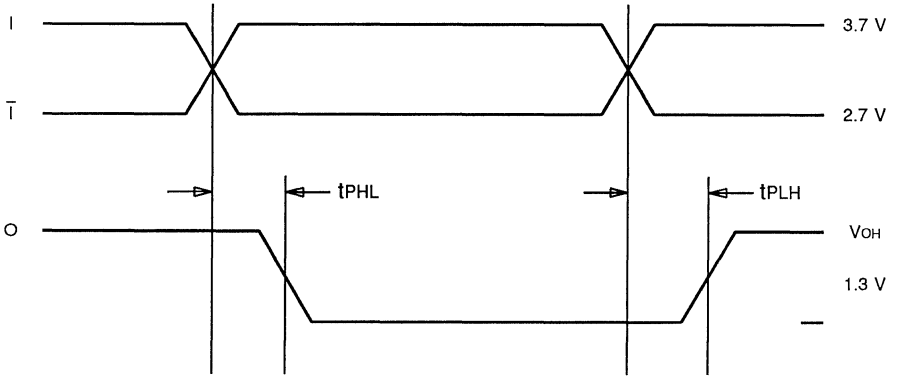


Figure 5. Propagation Delay

41LG Quad Differential Line Driver

Features

- Pin-equivalent to the general-trade AM26LS31 device, with improved speed, reduced power consumption, and reduced EMI
- Four line drivers per package
- Meets ESDI standards
- Complementary outputs from each line driver
- No line loading when V_{CC} = 0 V
- Maximum power dissipation, 300 mW
- Maximum propagation delay, 6 ns
- Drive capability, 40 mA
- High output drive for 50-Ω lines
- Minimum output short-circuit current, 100 mA
- Output skew 0.2 ns, typical
- Single 5 V supply
- 0 to 85 °C operating temperature

Description

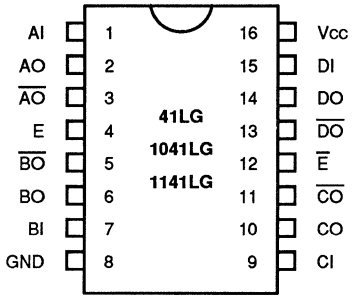
The 41LG Quad Differential Line Driver integrated circuit transmits digital data over balanced transmission lines. It translates TTL input logic levels to ECL output levels that directly drive the line. This OXIL-technology device contains enable circuitry and four drivers. It is pin-equivalent to the general-trade AM26LS31 device; however, it has reduced power consumption and generates lower levels of electromagnetic interference (EMI). The 41LG line driver is compatible with many line receivers, including the AT&T 41LF and 858B HIC (built-in terminations) devices, and the general-trade AM26LS32 device.

The quad differential line driver is available in a 16-pin plastic DIP (41LG), SOJ package (1041LG), and SOIC package (1141LG).

The *41LG Line Driver and 41LF Line Receiver* application note (AP86-35DBIP) describes two modes of propagation with balanced twisted-pair transmission lines.

User Information

Pin Descriptions



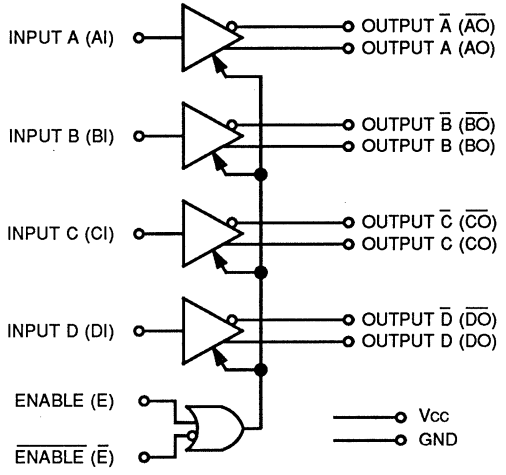


Figure 1. Pin Function and Logic Diagrams

Characteristics

Electrical Characteristics

T_A = 0 to 85 °C, V_{CC} = 5 V ± 0.5 V

Parameter	Sym	Min	Typ	Max	Unit
Output voltages, V_{CC} = 4.5 V (see Figures 2 and 3):					
low, I_{OL} = –8.0 mA*	V_{OL}	—	—	V_{OH} – 0.80**	V
high, I_{OH} = –40.0 mA*	V_{OH}	3.0	—	—	V
high-Z	V_{OZ}	—	2.0	V_{OL} – 0.05	V
high-Z, V_{CC} = 4.75 V	V_{OZ}	—	2.0	V_{OL} – 0.20	V
Input voltages:					
low, V_{CC} = 5.5 V	V_{IL}†	—	—	0.8	V
high, V_{CC} = 4.5 V	V_{IH}†	2.0	—	—	V
clamp, V_{CC} = 4.5 V, I_{IN} = –18.0 mA	V_{IK}	—	—	–1.5	V
Output current					
short-circuit	I_{SC}	–100	–200	–300	mA
Input currents, V_{CC} = 5.5 V:					
low, V_{IN} = 0.4 V	I_{IL}	—	—	–400	μA
high, V_{IN} = 2.7 V	I_{IH}	—	—	20	μA
reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	μA
Power supply current, V_{CC} = 5.5 V:					
all outputs disabled	I_{CC}	—	60	85	mA
all outputs enabled	I_{CC}	—	40	65	mA

* Typical value of output current when the load shown in Figure 4 is used.
** V_{OL} must be a minimum of 0.8 V less than its complementary output.
† These input levels provide zero noise immunity and should be tested only in a static, noise-free environment.

Maximum Ratings

Power supply voltage (V_{CC}) ..... 7.0 V
Ambient operating temperature (T_A) range ..... 0 to 125 °C
Storage temperature (Tstg) range ..... −40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

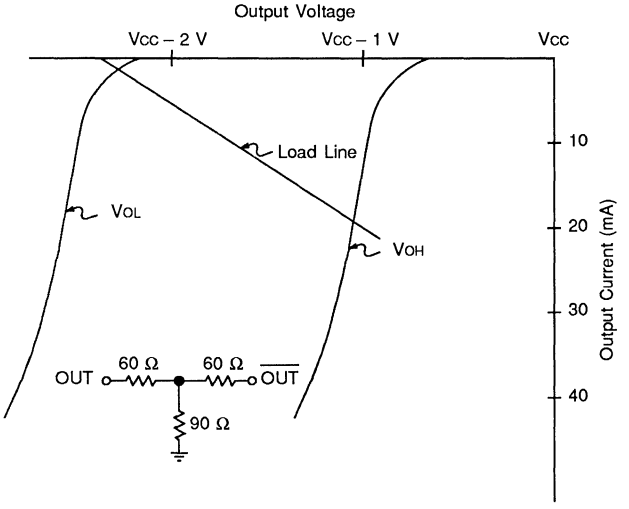


Figure 2. Driver Output Current — Voltage Characteristics (Y-Load)

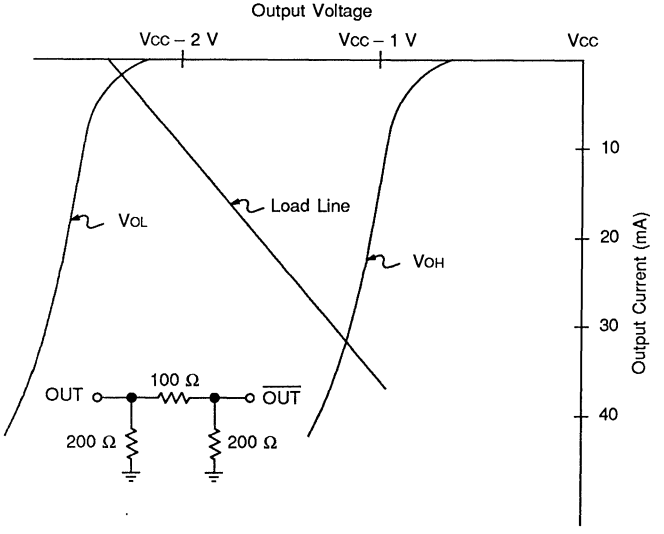


Figure 3. Driver Output Current — Voltage Characteristics (π-Load)

Network

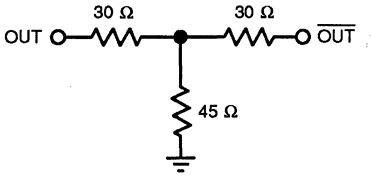


Figure 4. Parametric Test Circuit

Timing Characteristics (See Figures 6 and 7)

T_A = 25 °C V_{CC} = 5 V, timing management test circuit (shown in Figure 5) connected to output.

Symbol	Description	Typ	Max	Unit
	Propagation delay:			
t_{PLH}	input high (low) to output high	3.0	6.0	ns
t_{PHL}	input low (high) to output low	3.0	6.0	ns
	Disable time:*			
t_{PHZ}	high to high impedance	30	50	ns
t_{PLZ}	low to high impedance	30	50	ns
	Enable time:*			
t_{PZH}	high impedance to high	35	40	ns
t_{PZL}	high impedance to low	35	40	ns
tskew	Output skew, $\lvert t_{PLH} - t_{PHL} \rvert$	0.2	0.5	ns
Δtskew	Difference between drivers	0.3	—	ns

* The device is disabled when E = 0 and $\overline{E}$ = 1; all other combinations of E and $\overline{E}$ enable the device.

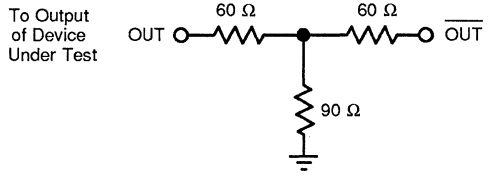


Figure 5. Timing Management Test Circuit

Timing Diagrams

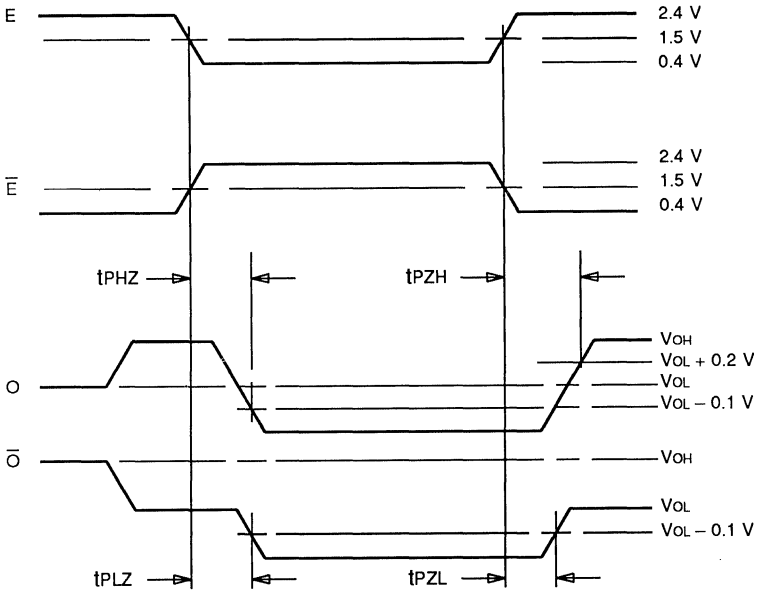


Figure 6. Enable and Disable Timing

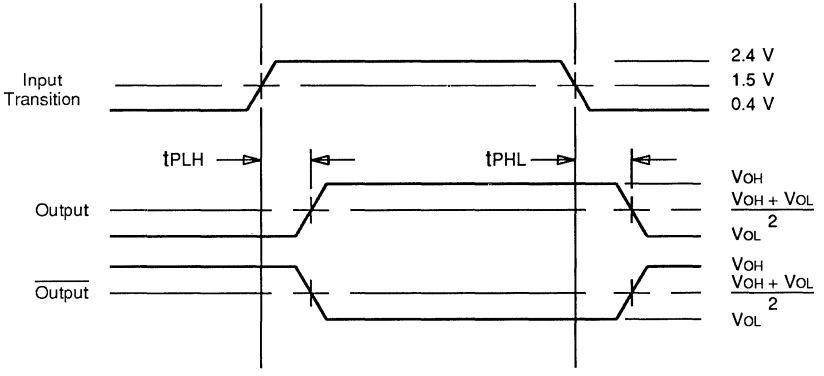


Figure 7. Propagation Delay

41LK, 41LL, and 41LM Dual Differential Line Driver-Receiver Pairs

Features

Device

- Single 5 V supply
- 0 to 85 °C operating temperature
- Meets ESDI standards

Driver

- Two line drivers per package
- Complementary outputs from each line driver
- Maximum propagation delay, 6.0 ns
- No line loading when V_{CC} = 0 V
- Minimum output short-circuit current , 100 mA
- Output skew 0.2 ns, typical

Receiver

- Two line receivers per package
- Complementary inputs for each line receiver
- Maximum propagation delay, 7.0 ns
- 0.20 V input sensitivity
- Common mode rejection of ±4 V
- TTL- and ECL-compatible inputs

Description

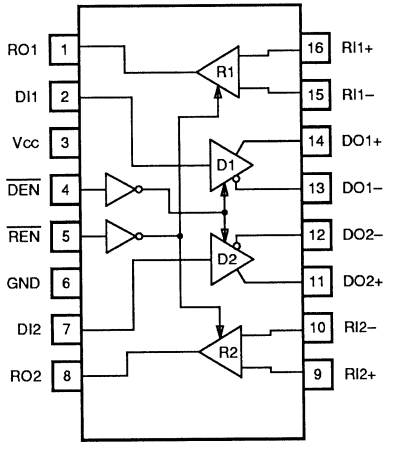
The 41LK, 41LL, and 41LM devices are dual differential line driver-receiver pairs that are compatible with the 41LG Quad Line Driver and 41LF Quad Line Receiver devices. These dual pair devices consist of two line receivers with differential ECL-to-TTL converters, two line drivers with TTL-to-differential ECL converters, and individual 3-state enabling circuitry for the driver and receiver pairs. This allows serial data and a control clock to be transmitted and received on a single integrated circuit. The typical propagation delays for the driver and receiver of these OXIL-technology devices are 3.0 ns and 4.0 ns, respectively.

The 41LK device is intended for use where the minimization of electromagnetic interference is required, and it has characteristics similar to those of the 41LG and 41LF devices. The 41LL device has internal 200-Ω discharge resistors on each driver output and is equivalent to the NSC DS8923A. The 41LM device has internal resistor terminations for both the driver (200 Ω) and receiver (100 Ω), eliminating the need for external resistors, and it is intended for use with 100-Ω impedance (Z) twisted-pair or flat cable.

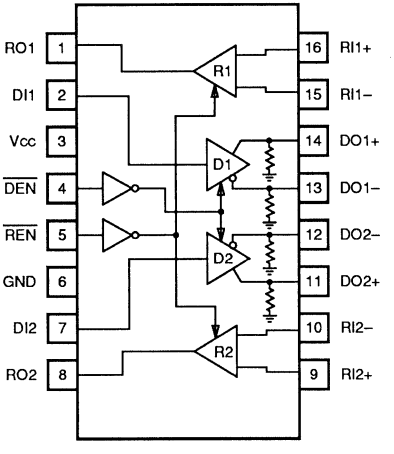
The dual differential line driver-receiver pairs are available in a 16-pin plastic DIP (41LK, 41LL, and 41LM), SOJ package (1041LK, 1041LL, and 1041LM), or SOIC (1141LK, 1141LL, 1141LM) package.

User Information

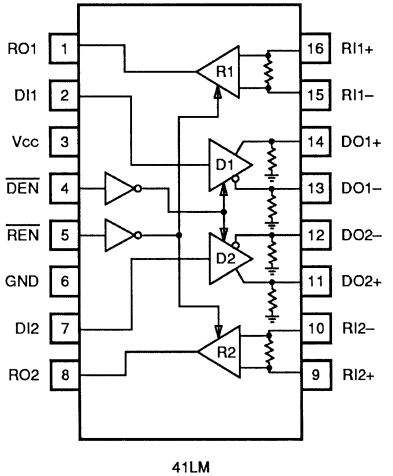
Pin Descriptions



41LK
1041LK
1141LK



41LL
1041LL
1141LL



41LM
1041LM
1141LM

$\overline{DEN}$	$\overline{REN}$	DO1	DO2	RO1	RO2
0	0	Active	Active	Active	Active
1	0	High-Z	High-Z	Active	Active
0	1	Active	Active	High-Z	High-Z
1	1	High-Z	High-Z	High-Z	High-Z

Figure 1. Pin Function Diagrams and Output Enable Table

Characteristics

Electrical Characteristics

T_A = 0 to 85 °C, V_{CC} = 5 V ± 0.5 V

Device

Parameter	Sym	Min	Typ	Max	Unit
Power supply current, V_{CC} = 5.5 V:					
41LK					
all outputs disabled	I_{CC}	—	40	70	mA
all outputs enabled	I_{CC}	—	25	45	mA
41LL and 41LM					
all outputs disabled	I_{CC}	—	60	90	mA
all outputs enabled	I_{CC}	—	90	135	mA

Driver

Output voltage test circuit connected to output (see Figures 2 and 3).

Parameter	Sym	Min	Typ	Max	Unit
Output voltages, V_{CC} = 4.5 V:					
low	V_{OL}	—	—	V_{OH} – 0.8*	V
high	V_{OH}	3.0	—	—	V
high-Z, I_{OH} = –1.0 mA	V_{OZ}	—	2.0	V_{OL} – .05	V
high-Z, V_{CC} = 4.75 V	V_{OZ}	—	2.0	V_{OL} – 0.2	V
Input voltages:					
low, V_{CC} = 5.5 V	V_{IL}**	—	—	0.7	V
high, V_{CC} = 4.5 V	V_{IH}**	2.0	—	—	V
clamp, V_{CC} = 4.5 V, I_{IN} = –18.0 mA	V_{IK}	—	—	–1.5	V
Output current					
short-circuit	I_{SC}	–100	–200	–300	mA
Input currents, V_{CC} = 5.5 V:					
low, V_{IN} = 0.4 V	I_{IL}	—	—	–400	μA
high, V_{IN} = 2.7 V	I_{IH}	—	—	20	μA
reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	μA
Differential output resistor (41LL, 41LM)	R_O	—	200	—	Ω

* V_{OL} must be a minimum of 0.8 V less than its complementary output.
** The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.

Receiver

Output voltage test circuit connected to output (see Figure 4).

Parameter	Sym	Min	Typ	Max	Unit
Output voltage, V_{CC} = 4.5 V:					
low, I_{OL} = 8 mA	V_{OL}	—	—	0.5	V
high, I_{OH} = −400 μA	V_{OH}	2.5	—	—	V
Enable input voltages:					
low, V_{CC} = 5.5 V	V_{IL}*	—	—	0.7	V
high, V_{CC} = 4.5 V	V_{IH}*	2.0	—	—	V
Differential input voltages,** V_O = V_{OL} or V_{OH}					
−0.80 V < V_{IH} < 7.2 V, −1.2 V < V_{IL} < 6.8 V	V_{TH}*	0.20	0.1	—	V
Output currents, V_{CC} = 5.5 V:					
off-state (high-Z), V_O = 0.4 V	I_{OZL}	—	—	−20	μA
off-state (high-Z), V_O = 2.4 V	I_{OZH}	—	—	20	μA
short-circuit	I_{SC}	−25.0	—	−100	mA
Enable input currents, V_{CC} = 5.5 V:					
low, V_{IN} = 0.4 V	I_{IL}	—	—	−400	μA
high, V_{IN} = 2.7 V	I_{IH}	—	—	20	μA
reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	μA
Differential input currents (41LK, 41LL):					
low, V_{IN} = −1.2 V	I_{IL}	—	—	−1.0	mA
high, V_{IN} = 7.2 V	I_{IH}	—	—	1.0	mA
Differential input impedance (41LM)					
measured between RI+ and RI−	RI	—	105	—	Ω

* The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.

** The input of unused differential input pairs should be biased to V_{CC}. No protection resistor is required.

Maximum Ratings

Power supply voltage (V_{CC}) ..... 7.0 V
Ambient operating temperature (T_A) range ..... 0 to 125 °C
Storage temperature (Tstg) range ..... −40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

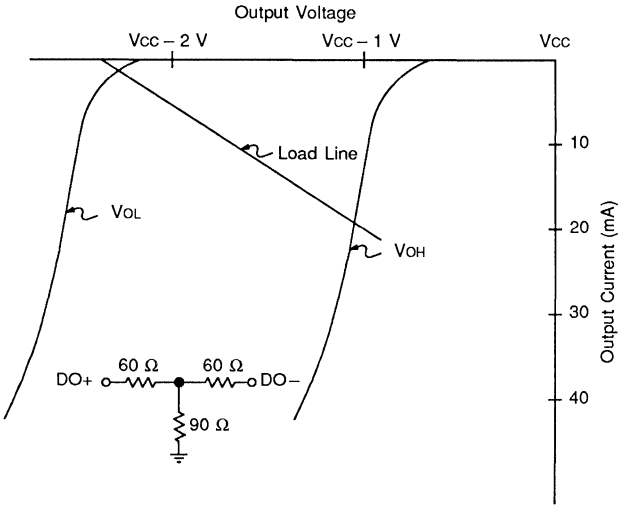
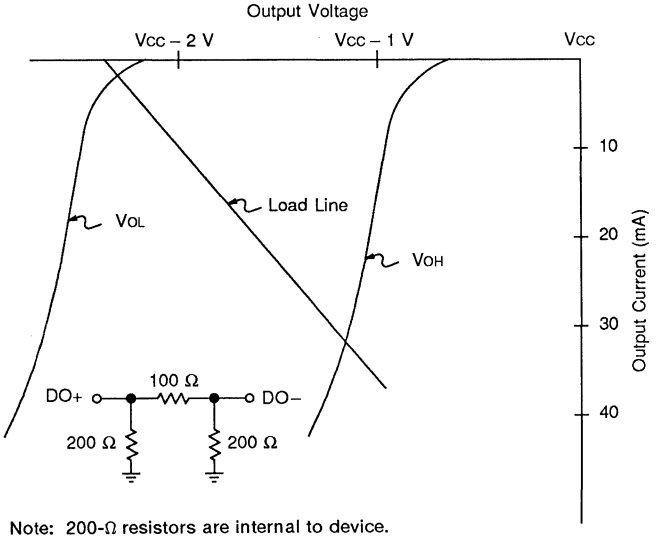
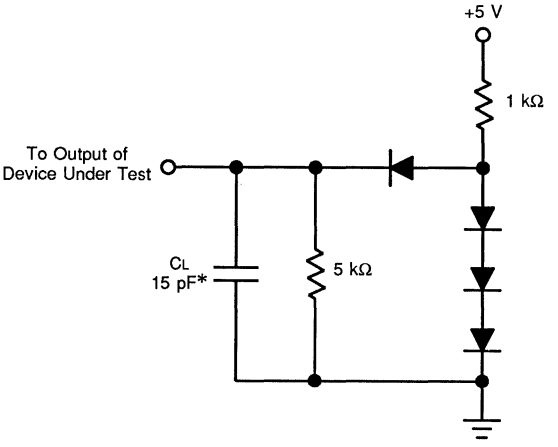


Figure 2. 41LK Driver Output Current — Voltage Characteristics (Y-Load)



Note: 200-Ω resistors are internal to device.

Figure 3. 41LL and 41LM Driver Output Current — Voltage Characteristics (π-Load)



Note: All 458E or 1N4148 diodes.
* Includes probe and jig capacitances.

Figure 4. Output Voltage and Propagation Delay Test Circuit

Timing Characteristics

Driver (See Figures 7 and 8)

T_A = 25 °C, V_{CC} = 5 V, timing management test circuit connected to output (see Figures 5 and 6).

Symbol	Description	Typ	Max	Unit
	Propagation delay:			
t_{PLH}	input high to output high	3.0	6.0	ns
t_{PHL}	input low to output low	3.0	6.0	ns
	Disable time:			
t_{PHZ}	high to high impedance	20	—	ns
t_{PLZ}	low to high impedance	20	—	ns
	Enable time:			
t_{PZH}	high impedance to high	20	—	ns
t_{PZL}	high impedance to low	20	—	ns
tskew	Output skew, $\lvert t_{PLH} - t_{PHL} \rvert$	0.2	0.5	ns
Δtskew	Difference between drivers	0.3	—	ns

Receiver (See Figures 9 and 10)

T_A = 25 °C, V_{CC} = 5 V, propagation delay test circuit connected to output (see Figure 4).

Symbol	Description	Typ	Max	Unit
	Propagation delay:			
t_{PLH}	input high (low) to output high	3.5	7.0	ns
t_{PHL}	input low (high) to output low	4.5	7.0	ns
	Disable time:			
t_{PHZ}	high to high impedance	20	—	ns
t_{PLZ}	low to high impedance	20	—	ns
	Enable time:			
t_{PZH}	high impedance to high	20	—	ns
t_{PZL}	high impedance to low	20	—	ns

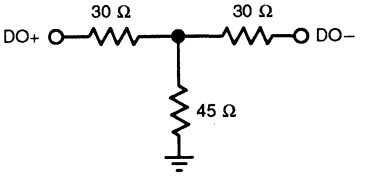


Figure 5. 41LK Timing Management Test Circuit

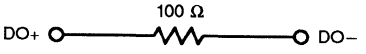


Figure 6. 41LL and 41LM Timing Management Test Circuit

Timing Diagrams

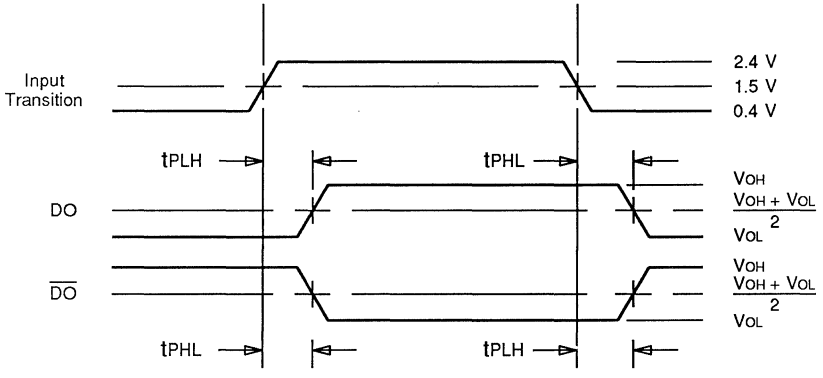


Figure 7. Driver Propagation Delay Timing

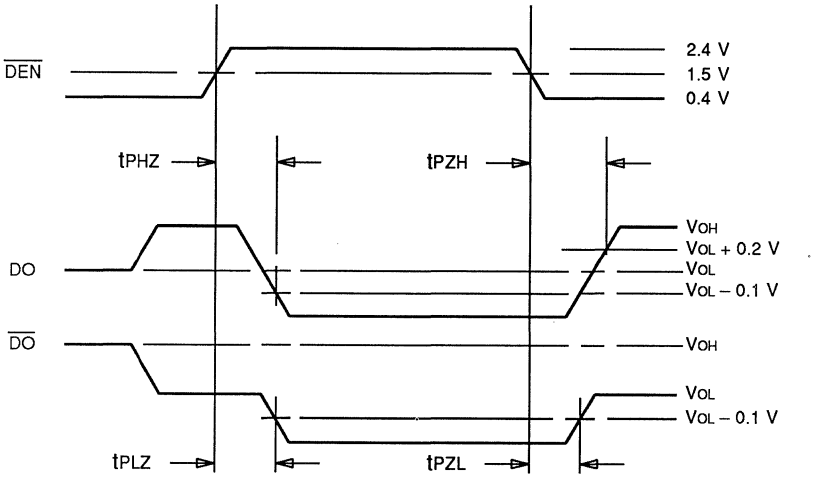


Figure 8. Driver Enable and Disable Timing

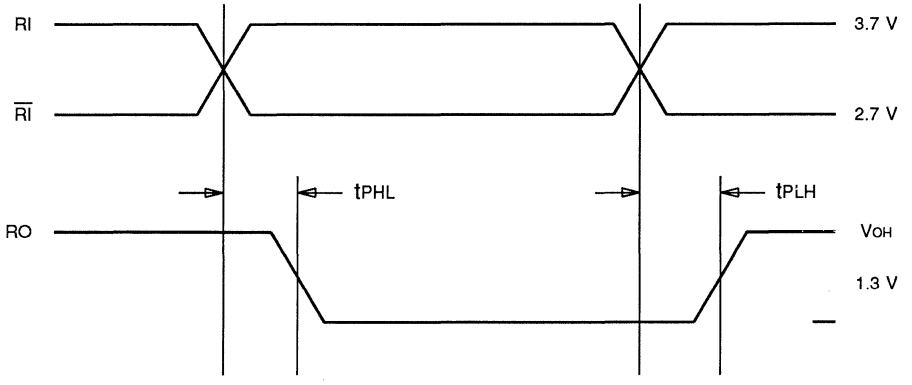


Figure 9. Receiver Propagation Delay Timing

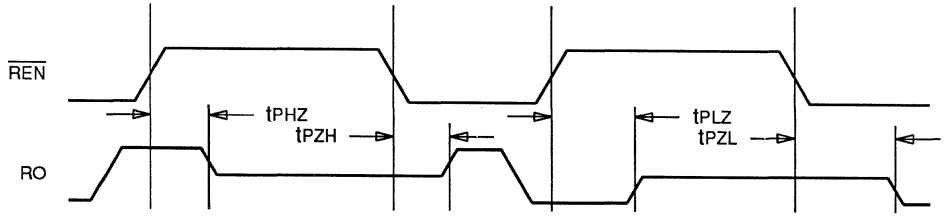


Figure 10. Receiver Enable and Disable Timing

T7274A Quad Differential Line Driver

Features

- Four line drivers per package
- Complementary outputs from each line driver
- 24-mA drive capability
- High output drive for 100-Ω, 110-Ω, and 150-Ω lines
- 2.0-ns minimum and 4.75-ns maximum propagation delays
- 0.1-ns output skew, typical
- 140 Mb/s data rate
- 300-mW maximum power dissipation
- Single 5 V supply
- 0 to 85 °C operating temperature

Description

The T7274A Quad Differential Line Driver integrated circuit is a single-input-to-balanced-output converter that drives differential transmission lines. The input requires typical CMOS signals, and the output has typical CMOS voltage swings and can drive 100-Ω, 110-Ω, and 150-Ω twisted pair lines through a resistor attenuation network.

This CMOS device is similar to the general-trade 26LS31 device; however, it has decreased power consumption and generates lower levels of electromagnetic interference (EMI).

The T7274A line driver is compatible with many line receivers, including the AT&T T7275B and 41LF devices and the general-trade 26LS32 device. The quad differential line driver is available in a 16-pin plastic DIP and small-outline J-lead (SOJ) package.

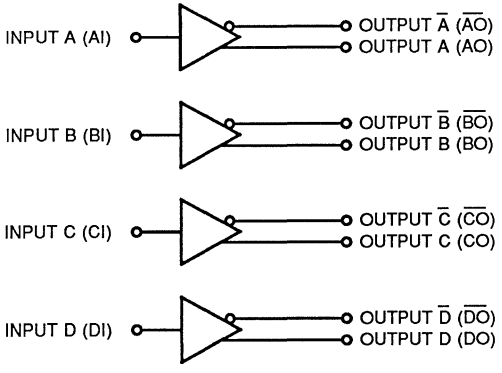


Figure 1. Logic Diagram

User Information

Pin Descriptions

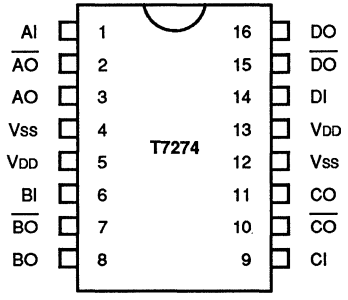


Figure 2. Pin Function Diagram

Table 1. Pin Descriptions

Symbol	Type	Name
AI	I	A-line driver input
$\overline{AO}$	O	Inverted A-line driver output
AO	O	A-line driver output
BI	I	B-line driver input
$\overline{BO}$	O	Inverted B-line driver output
BO	O	B-line driver output
CI	I	C-line driver input
$\overline{CO}$	O	Inverted C-line driver output
CO	O	C-line driver output
DI	I	D-line driver input
$\overline{DO}$	O	Inverted D-line driver output
DO	O	D-line driver output
VSS	—	Ground pins
VDD	—	5 V supply pins

Characteristics

Electrical Characteristics

T_A = 0 to 85 °C, V_{DD} = 5.0 V ± 0.25 V

Parameter	Sym	Min	Typ	Max	Unit
Output voltages, V_{DD} = 4.75 V:*					
low, I_{OL} = +12.5 mA	V_{OL}	—	—	0.5	V
high, I_{OH} = –12.5 mA	V_{OH}	4.25	—	—	V
Output Impedance	—	—	20	40	Ω
Input voltages:**					
low	V_{IL}	—	—	1.0	V
high	V_{IH}	3.75	—	—	V
threshold	V_{TH}	—	$V_{DD}/2$	—	V
Output currents, short-circuit	I_{SC}	–100	—	–200	mA
Input currents, V_{DD} = 5.25 V:					
low, V_{IN} = 0.5 V	I_{IL}	—	—	–1.0	μA
high, V_{IN} = 5.25 V	I_{IH}	—	—	100	μA
Power supply current, V_{DD} = 5.25 V:					
DC conditions	I_{DD}	—	0.25	0.5	mA
100 Mb/s	I_{DD}	—	75	80	mA

* I_{OL} and I_{OH} can increase to 25 mA. The reduced V_{OL} and V_{OH} are computed from the output impedance.
** Each input has typically 100 kΩ to V_{SS}. Thus, a no connect input is pulled low.

Maximum Ratings

Power supply voltage (V_{DD}) ..... 7.0 V
Ambient operating temperature (T_A) range ..... 0 to 85 °C
Storage temperature (Tstg) range ..... −40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

T_A = 0 to 85 °C, V_{DD} = 5.0 V ± 0.25 V, test circuit connected to output (see Figure 3).*

Symbol	Description	Min	Typ	Max	Unit
	Propagation delay, input to output:				
t_{PD}	AO, BO, CO, and DO	2.0	3.0	4.75	ns
$t_{\overline{PD}}$	$\overline{AO}$, $\overline{BO}$, $\overline{CO}$, and $\overline{DO}$	2.0	3.0	4.75	ns
tskew	Difference between propagation delays $\lvert t_{PD} - t_{\overline{PD}} \rvert$	—	100	300	ps
t_{PWD}	Pulse width distortion, $\lvert t_{IN} - t_{OUT} \rvert$	—	200	500	ps
tr, tf	Rise and fall time (10% to 90%)	—	1.5	3.0	ns
t_{IN}	Input pulse width	7	—	—	ns

* Input rise and fall times (10% to 90%) of less than 4 ns are necessary to guarantee maximum propagation delay, pulse width distortion, and skew characteristics.

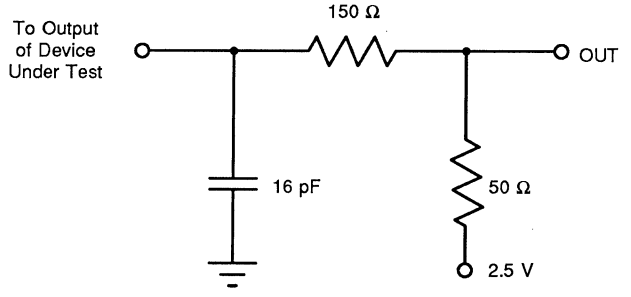


Figure 3. Timing Test Circuit

Timing Diagram

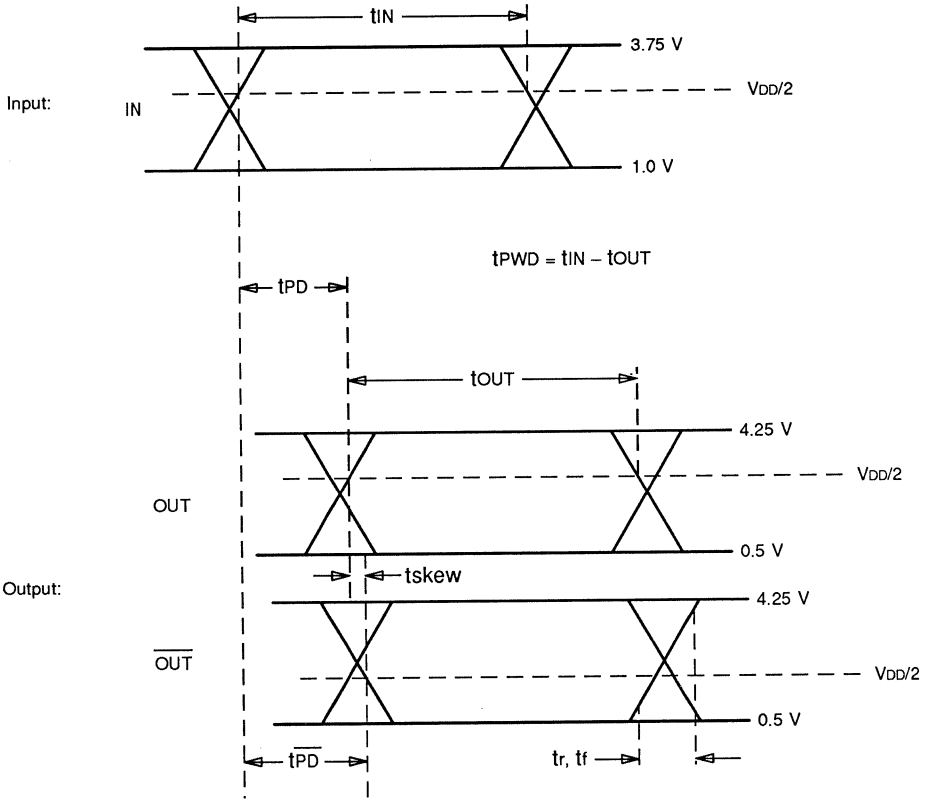


Figure 4. Timing Waveforms

T7275B Quad Differential Line Receiver

Features

- Low pulse width distortion
- 140-Mb/s data rate
- 800-mW maximum power dissipation
- 8.0-ns maximum propagation delay
- 0.6 V input sensitivity
- ±1 V common mode rejection
- 120-Ω HIC line-to-line input
- 7800-Ω SIC input
- Single 5 V supply
- 0 to 85 °C operating temperature

Description

The T7275B Quad Differential Line Receiver integrated circuit is a quad differential input to CMOS output line receiver. It is functionally an ECL-level-to-CMOS converter. Direct interfacing to ECL signals is possible by AC coupling through a capacitor. The CMOS technology device is similar to the general-trade 26LS32 device; however, it has increased speed and decreased power consumption. By having four receivers in one T7275B device, circuit board package count is reduced. The average propagation delay is 5 ns and the common mode operating range is ±1 V. Input dc offset is less than 50 mV. The inputs typically have 10 mV of hysteresis.

The T7275B line receiver is compatible with many line drivers, including the AT&T T7274A and 41LG devices, and the general-trade 26LS31 device. The quad differential line receiver is available in a 16-pin plastic DIP and small-outline J-lead (SOJ) package.

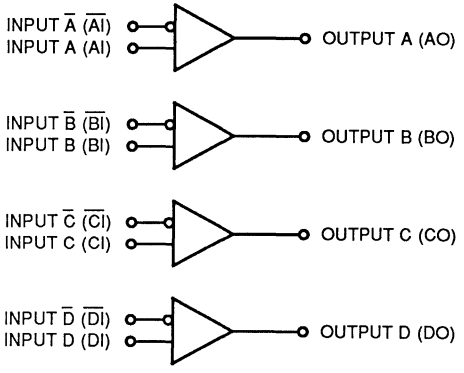


Figure 1. Logic Diagram

User Information

Pin Descriptions

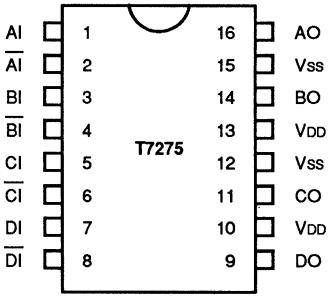


Figure 2. Pin Function Diagram

Table 1. Pin Descriptions

Symbol	Type	Name
AI	I	A-line receiver input
$\overline{AI}$	I	Inverted A-line receiver input
AO	O	A-line receiver output
BI	I	B-line receiver input
$\overline{BI}$	I	Inverted B-line receiver input
BO	O	B-line receiver output
CI	I	C-line receiver input
$\overline{CI}$	I	Inverted C-line receiver input
CO	O	C-line receiver output
DI	I	D-line receiver input
$\overline{DI}$	I	Inverted D-line receiver input
DO	O	D-line receiver output
VSS	—	Ground pins
VDD	—	5 V supply pins

Characteristics

Electrical Characteristics

T_A = 0 to 85 °C, V_{DD} = 5.0 V ± 0.25 V

Parameter	Sym	Min	Typ	Max	Unit
Output voltages, V_{DD} = 4.75 V:*					
low, I_{OL} = +12.5 mA	V_{OL}	—	—	0.5	V
high, I_{OH} = –12.5 mA	V_{OH}	4.25	—	—	V
Output impedance	—	—	15	30	Ω
Differential input voltages:** V_O = V_{OL} or V_{OH}					
–2.1 V < V_{CM} < 2.9 V	V_{TH}	0.3	0.6	—	V
Output currents, short-circuit	I_{SC}	–150.0	—	–300.0	mA
Differential Input currents:					
low	I_{IL}	—	—	1.0	μA
high	I_{IH}	—	—	1.0	μA
Power supply current, V_{DD} = 5.25 V DC conditions†	I_{DD}	0.0	12.0	20.0	mA

* I_{OL} and I_{OH} can increase to 25 mA. The reduced V_{OL} and V_{OH} are computed from the output impedance.
** Operation with 1 V < V_{CM} < 4 V is possible, but with relaxed propagation delay and pulse width distortion characteristics.
† Pulling all inputs below 0.6 V powers down the device. All outputs are then equal to V_{DD}.

Maximum Ratings

Power supply voltage (V_{DD}) ..... 7.0 V
Ambient operating temperature (T_A) range ..... 0 to 85 °C
Storage temperature (T_{stg}) range ..... −40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

T_A = 0 to 85 °C, V_{DD} = 5.0 V ± 0.25 V, test circuit connected to output* (see Figure 3).*

Symbol	Description	Min	Typ	Max	Unit
	Propagation delay (AI, BI, CI, and DI) (see Figure 4):				
t_{PHH}	input high to output high	3.5	5.0	8.0	ns
t_{PLL}	input low to output low	3.5	5.0	8.0	ns
	Propagation delay ($\overline{AI}$, $\overline{BI}$, $\overline{CI}$, and $\overline{DI}$) (see Figure 4):				
t_{PHL}	input high to output low	3.5	5.0	8.0	ns
t_{PLH}	input low to output high	3.5	5.0	8.0	ns
t_{PWD}	Pulse width distortion, $\lvert t_{IN} - t_{OUT} \rvert$	—	100	500	ps
t_r,t_f	Rise and fall times (10% to 90%)	—	1.5	3.0	ns
t_{IN}	Input pulse width	7	—	—	ns

* Input rise and fall times (10% to 90%) of less than 3 ns are necessary to guarantee maximum propagation delay and pulse width distortion characteristics.

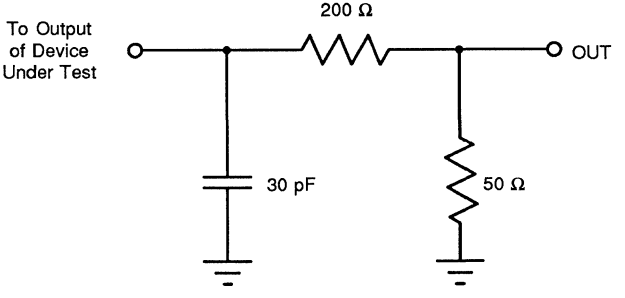
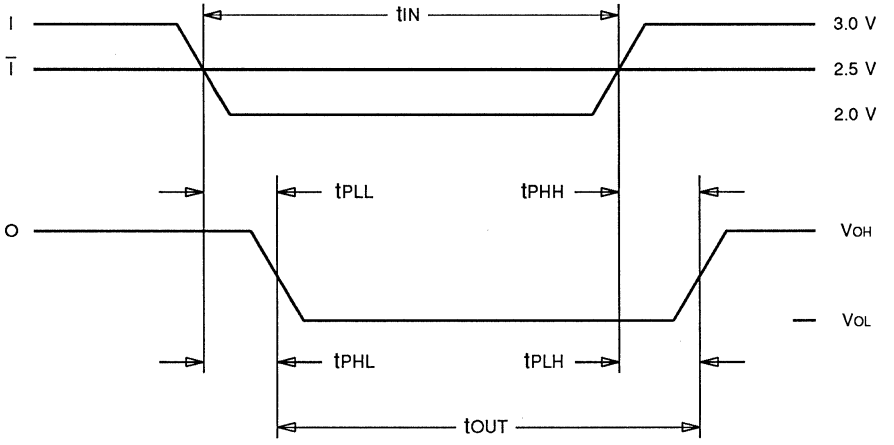


Figure 3. Output Voltage and Propagation Delay Test Circuit

Timing Diagram



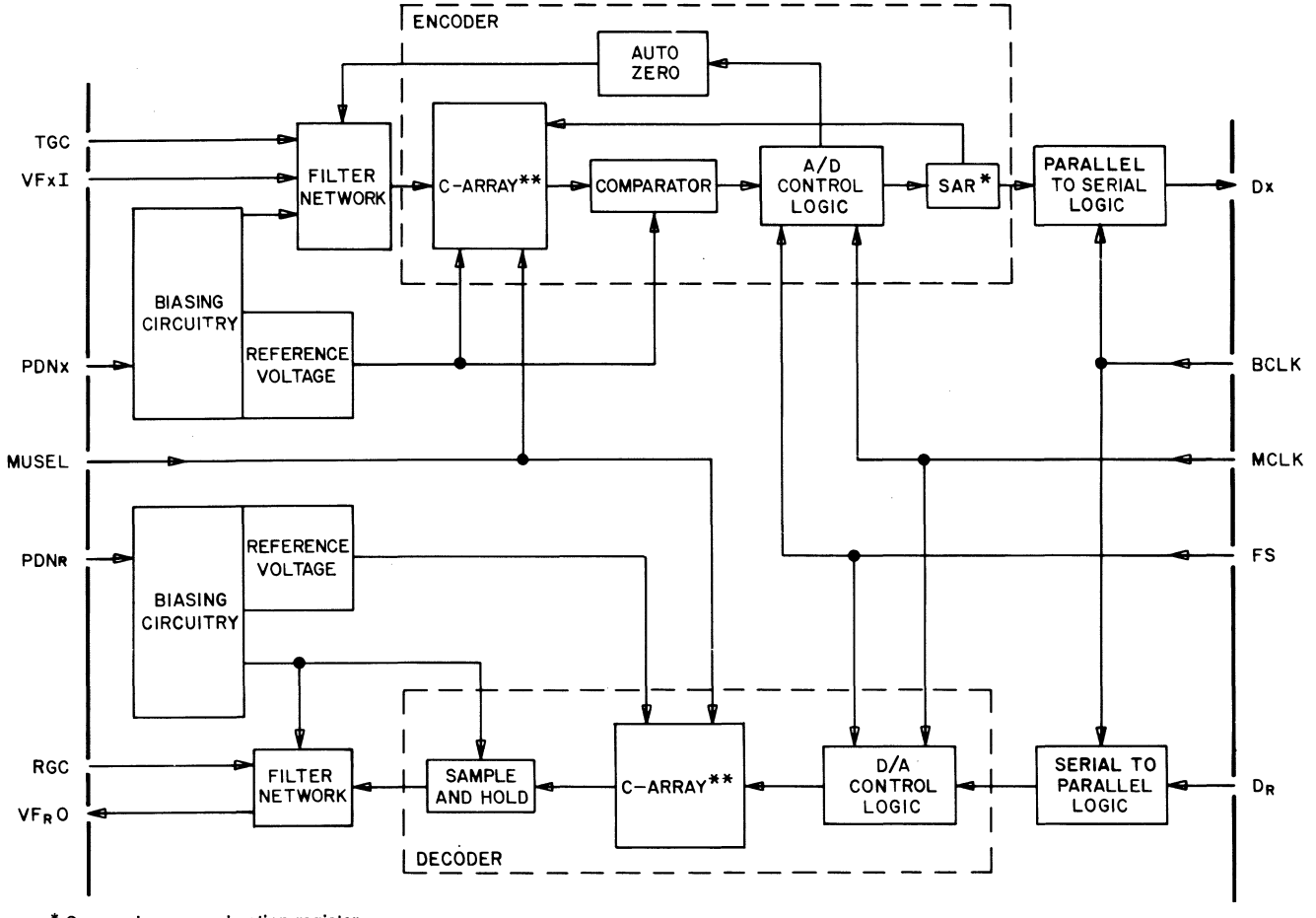
T7500 PCM Codec with Filters

Features

- AT&T/CCITT-compatible
- Pin-selectable μ-law or A-law operation
- Pin-selectable transmit and receive gain
- Variable data rate (128 kHz to 4.096 MHz)
- On-chip voltage reference
- TTL-compatible I/O
- No external components required
- ± 5 V supply
- Latch-up free CMOS technology
- Low power dissipation
  - 20-mW typical power-down
  - 80-mW typical operation

Description

The T7500 PCM Codec with Filters is a single-chip integrated circuit that provides analog-to-digital and digital-to-analog conversion, as well as the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed system. The T7500 device is available in an 18-pin plastic DIP or a 20-pin plastic small-outline J-lead (SOJ) package for surface mounting.



* Successive approximation register.
** Capacitor array.

Figure 1. Block Diagram

User Information

Pin Descriptions

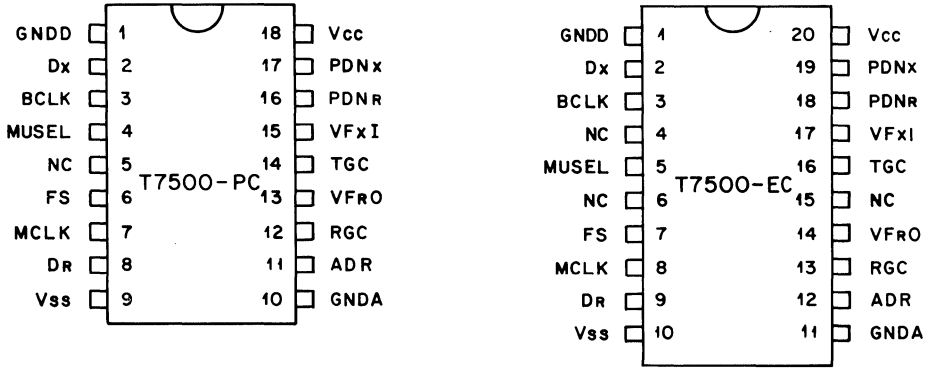


Figure 2. Pin Function Diagrams

Table 1. Pin Descriptions

Symbol	Type	Name/Function
GNDD	—	**Ground (Digital).**
Dx	O	**Data Transmit.** Eight-bit μ-law or A-law PCM inverted binary output.
BCLK	I	**Bit Clock.** PCM is transmitted and received at a rate defined by this input clock (128 kHz—4.096-MHz).
MUSEL	I	**μ-law Select.** A high (1) or no connection on this pin results in μ-law conversion. Apply a low (0) to this pin for A-law encodings.
NC	—	**No Connection.**
FS	I	**Frame Synchronization.** An 8-kHz timing pulse is applied to this pin to initiate A/D and D/A conversion processes.
MCLK	I	**Master Clock.** 2.048-MHz
DR	I	**Data Receive.** This is the 8-bit μ-law or A-law PCM inverted binary input.
GNDA	—	**Ground (Analog).**

Table 1. Pin Descriptions (Continued)

Symbol	Type	Name/Function
VSS	—	**–5 V Supply (± 5%).**
ADR	I	**Address.** A low or no connection on this pin enables the FS pulse. It is used for channel selection when more than one codec is used on a PCM bus.
RGC	I	**Receive Gain Control.** A low or no connection on this pin sets the gain to 0 dB (0 output TLP); a high on this pin sets the receive gain to +3 dB ± 0.1 dB (+3 output TLP). When high, the gain is set with respect to the gain measured at 0 dB setting.
VFRO	O	**Voice Frequency Receive Output.** The maximum load permitted on this pin is 20 kΩ in parallel with 50 pF.
TGC	I	**Transmit Gain Control.** A high or no connection on this pin sets the transmit gain to 0 dB (0 input TLP); a low sets the transmit gain to –3 dB ± 0.1 dB (+3 input TLP). When low, the gain is set with respect to the gain measured at 0 dB setting.
VFXI	I	**Voice Frequency Transmit Input.** Analog input to the transmit filters. The input impedance on this pin is greater than 400 kΩ.
PDNR	I	**Power-Down Receive.** A high on this pin causes power-down of receive side. During receive-side power-down, VFRO is grounded through a low impedance and the receive-side analog circuitry is disabled. A low or no connection allows normal receive-side operation.
PDNX	I	**Power-Down Transmit.** A high on this pin causes power-down of transmit side. A transmit power-down causes the DX buffer to go into a high-impedance state and all encoder analog circuitry to be disabled. A low or no connection allows normal transmit-side operation.
VCC	—	**+5 V Supply (± 5%).**

Overview

The T7500 PCM Codec is a synchronous device with a common master clock and synchronization input that drives both the transmit and receive sections. Device operation requires three logic inputs: MCLK, FS, and BCLK.

On power-up, the codec becomes active only after receiving a FS and ADR signal. The serial transfer of data to DR and from DX proceeds at a rate determined by BCLK (see Figure 4).

The digital output returns to a high-impedance state upon completion of this process and remains in this state until another set of synchronization and address signals is received. This allows the device to be used with a shared PCM bus (up to 64 channels at 4.096 MHz).

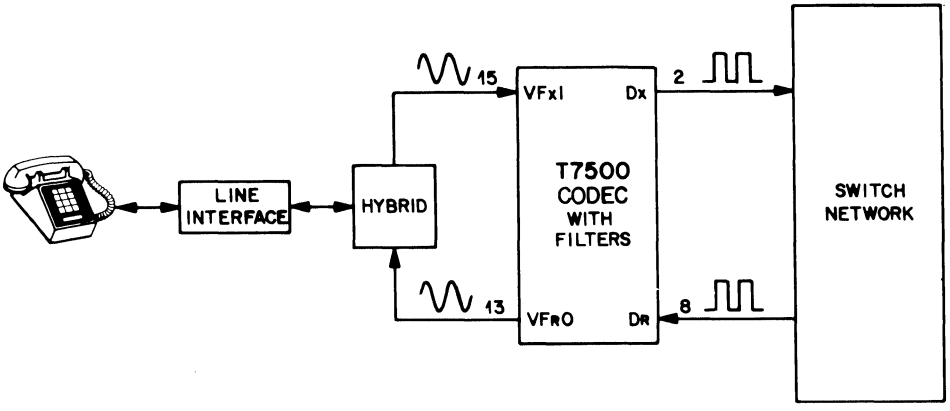


Figure 3. PCM System Block Diagram

The T7500 codec has a power-down mode that reduces power consumption and heat dissipation when the device is inactive. Two pins are used for this power-down option. A high applied to PDNR disables the receive side of the device; PDNx performs the same function on the transmit side of the device. Each side can be independently disabled. When the receive side is powered-down, output VFRO is grounded through a low impedance and all receive-side analog circuitry is disabled. Transmit power-down results in output Dx going into a high-impedance state and all transmit-side analog circuitry being disabled. The device is activated by applying a low to both leads.

This device implements either μ-law or A-law PCM encoding. MUSEL is used to determine the type of encoding. Inverted binary format is used for μ-law encoding. Alternate digit inversion is used for A-law transmission.

Separate gain controls provide gain settings for the transmit and receive sections. Either 0 dB or –3 dB gain can be selected for the transmit side and either 0 dB or +3 dB for the receive side.

On-chip voltage referencing is provided, eliminating the need for external circuitry and gain trimming.

Characteristics

DC Characteristics

T_A = 0 to 70 °C; V_{CC} = +5 V ± 5%; V_{SS} = –5 V ± 5%; GNDA = 0 V; GNDD = 0 V; 0TLP, unless otherwise specified. Typical values are for T_A = 25 °C and nominal power supply values.

Table 2. Digital Interface

Symbol	Parameter	Min	Max	Unit	Test Condition
I_{IL}	Low-level input current	–20	—	μA	$GNDD \leq V_{IN} \leq V_{IL}$
I_{IH}	High-level input current	—	20	μA	$V_{IH} \leq V_{IN} \leq V_{CC}$
V_{IL}	Input low voltage	—	0.8	V	—
V_{IH}	Input high voltage	2.0	—	V	—
V_{OL}	Output low voltage	—	0.4	V	—
V_{OH}	Output high voltage	2.4	—	V	—
C_I	Digital input capacitance	—	5	pF	—
I_L	Output leakage current	–50	50	μA	—

Table 3. Power Dissipation*

Symbol	Parameter	Min	Typ	Max	Unit
I_{CC1}	V_{CC} operating current	—	8.5	15	mA
I_{SS1}	V_{SS} operating current	—	–7.5	–13	mA
I_{CC0}	V_{CC} power-down current	—	2.0	7.0	mA
I_{SS0}	V_{SS} power-down current	—	–2.0	–4.0	mA
V_{CC}	Positive operating voltage	4.75	5	5.25**	V
V_{SS}	Negative operating voltage	–4.75	–5	–5.25**	V
P_1	Operating power dissipation	—	80	147	mW
P_0	Power-down dissipation	—	20	55	mW

* All measurements made at fBCLK = 2.048 MHz, outputs loaded.
** Absolute maximum ratings are V_{CC} = +7.5 V, V_{SS} = –7.5 V. Exceeding these values may result in permanent internal damage.

Table 4. Analog Interface — Transmit Filter Input Stage

Symbol	Parameter	Min	Typ	Max	Unit
R_I	Input resistance @ VFXI	0.4	1.1	—	MΩ
V_{OFF}	Input offset voltage @ VFXI	—	—	20	mV
C_L	Load capacitance @ VFXI	—	20	40	pF

Table 5. Analog Interface — Receive Filter Driver Amplifier Stage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_O	Output resistance @ V_{FRO} for voice frequencies	—	50	—	Ω	—
V_{OFF}	Output DC offset @ V_{FRO}	—	50	—	mV	Relative to GNDA
C_L	Load capacitance @ V_{FRO1}	—	—	50	pF	—
V_O	Maximum voltage output (swing across R_L):					
	μ-law	−2.229	—	2.229	V	RGC = high
	A-law	−2.229	—	2.229	V	(+3TLP)
	μ-law	−1.578	—	1.578	V	RGC = low
	A-law	−1.572	—	1.572	V	(0TLP)
R_L	Load resistance @ V_{FRO}	20	—	—	kΩ	—

Timing Characteristics

Table 6. Clock Section

Symbol	Parameter	Min	Typ	Max	Unit
tBCHBCH*	Bit clock period	.244	—	7.8	μs
tBCHBCL	Bit clock pulse width	.4tBCHBCH	.5tBCHBCH	.6tBCHBCH	—
tMCHMCH**	Master clock period	—	488	—	ns
tMCHMCL	Master clock pulse width	.4tMCHMCH	.5tMCHMCH	.6tMCHMCH	—

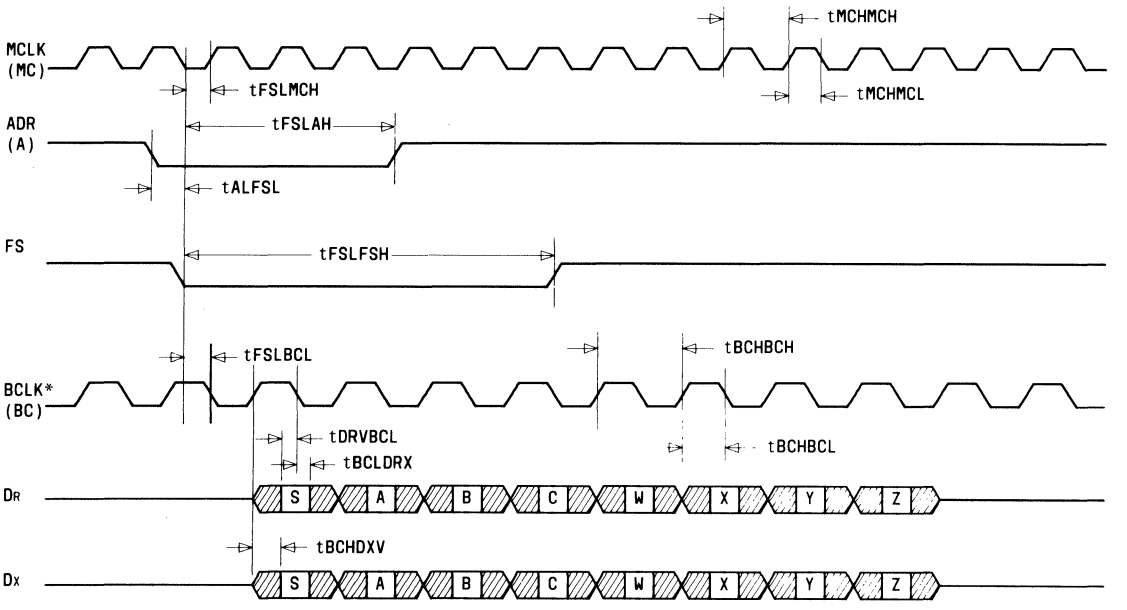
* BCLK ranges from 128 kHz to 4.096 MHz.
** 2.048 MHz.

Table 7. Data Section

Symbol	Parameter	Min	Typ	Max	Unit
tFSLMCH	Sync set-up time in reference to MC	90	.5tMCHMCH	tMCHMCH	ns
tFSLAH*	Address hold time	1.5tBCHBCH	3tBCHBCH	—	—
tALFSL	Address set-up time	10	.5tBCHBCH	—	ns
tFSLFSH**	Sync pulse width	1.5tBCHBCH	2tBCHBCH	63	μs
tFSLBCL	Sync set-up time	75	200	tBCHBCH − 50	ns
tDRVBCL	DR set-up time	50	200	—	ns
tBCLDRX	DR hold time	50	300	—	ns
tBCHDXV†	DX delay time	30	80	150	ns

* Max = constant low.
** Negative logic sense.
† DX max load ≤ 300 pF plus 1 medium-power TTL load.

Timing Diagram



* BCLK ranges from 128 kHz to 4.096 MHz. It determines ADR, FS, DR, and DX timing.

Figure 4. Input/Output Timing

AC Characteristics — Transmission Parameters

Table 8. Gain and Dynamic Range

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
GE	Encoder milliwatt response (transmit gain tolerance):					Signal input = .7746 Vrms VCC and VSS are ± 5% TA = 0 to 70 °C
	μ-law	−0.15	±0.08	0.15	dBm0	
	A-law	−0.18	±0.08	±0.18	dBm0	
GD	Digital milliwatt response (receive gain tolerance):					VCC and VSS are ± 5% TA = 0 to 70 °C
	μ-law	−0.15	±0.08	0.15	dBm0	
	A-law	−0.18	±0.08	0.18	dBm0	

Table 9. Gain Tracking — Reference Level = 1.02 kHz, 0 dBm

Symbol	Parameter	Min	Max	Unit	Test Conditions
$G_{TX\mu}$	Transmit gain tracking error (sinusoidal input, μ-law)	–0.25 –0.50	0.25 0.50	dB dB	3 to –37 dBm0 –37 to –50 dBm0
G_{TXA}	Transmit gain tracking error (sinusoidal input, A-law)	–0.25 –0.50	0.25 0.50	dB dB	3 to –37 dBm0 –37 to –50 dBm0
$G_{TR\mu}$	Receive gain tracking error (sinusoidal input, μ-law)	–0.25 –0.50	0.25 0.50	dB dB	3 to –37 dBm0 –37 to –50 dBm0
G_{TRA}	Receive gain tracking error (sinusoidal input, A-law)	–0.25 –0.50	0.25 0.50	dB dB	3 to –37 dBm0 –37 to –50 dBm0

Table 10. Distortion

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
D_{XS}	Transmit signal to distortion (sinusoidal input = 1.02 kHz):					
	μ-law	36	—	—	dB	$0 \leq VFxI \leq -30$ dBm0
	A-law	35	—	—	dB	
	μ-law	30	—	—	dB	–40 dBm0
	A-law	29	—	—	dB	
	μ-law	25	—	—	dB	–45 dBm0
	A-law	25	—	—	dB	
D_{RS}	Receive signal to distortion (sinusoidal input = 1.02 kHz):					
	μ-law	36	—	—	dB	$0 \leq D_R \leq -30$ dBm0
	A-law	35	—	—	dB	
	μ-law	30	—	—	dB	–40 dBm0
	A-law	29	—	—	dB	
	μ-law	25	—	—	dB	–45 dBm0
	A-law	25	—	—	dB	
D_{XSF}	Transmit single frequency (distortion products)	— —	—	–28 –40	dBm0 dBm0	0 ≤ input ≤ 2 MHz .2 ≤ input ≤ 3.4 kHz
D_{RSF}	Receive single frequency (distortion products)	— —	—	–28 –40	dBm0 dBm0	0 ≤ input ≤ 2 MHz .2 ≤ input ≤ 3.4 kHz
D_{XD}	Transmit absolute delay	—	340	—	μs	—
D_{RD}	Receive absolute delay	—	240	—	μs	—
D_{DAA}	Delay distortion (analog-to-analog)	— — — — — —	250 60 20 20 50 220	— — — — — —	μs μs μs μs μs μs	f = 500 Hz f = 1 kHz f = 1.5 kHz f = 2 kHz f = 2.5 kHz f = 3 kHz

Table 11. Noise

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
FXC	Transmit idle channel noise (C-message weighted)	— —	14 —	18 23	dBrnC0 dBrnC0	μ-law A-law
FRC	Receive idle channel noise (C-message weighted)	— —	9 —	13 15	dBrnC0 dBrnC0	μ-law A-law
FXP	Transmit idle channel noise (psophometric weighted)	—	–69	–67	dBm0p	—
FRP	Receive idle channel noise (psophometric weighted)	—	–81	–75	dBm0p	—
PSRXCC	VCC power supply rejection (transmit channel)	–30	–35	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at DX
PSRXSS	VSS power supply rejection (transmit channel)	–30	–35	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at DX
PSRRCC	VCC power supply rejection (receive channel)	–30	–35	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at VFRO
PSRRSS	VSS power supply rejection (receive channel)	–30	–35	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at VFRO
FCXR	Crosstalk (transmit to receive, single-ended outputs): μ-law A-law	 — —	 — —	 –71 –70	 dB dB	VFXI = 0 dBm0; 1.02-kHz signal measured at VFR; DR = idle code
FCRX	Crosstalk (receive to transmit, single-ended outputs): μ-law A-law	 — —	 — —	 –71 –70	 dB dB	DR = 0 dBm0; VFXI = GNDA; 1.02-kHz signal measured at DX

Transmit Filter Transfer Characteristics

Table 12. Transmit Gain Relative to Gain at 1.02 kHz (GRX)*

Frequency (Hz)	Min	Typ	Max	Unit
16.67	—	–35	–30	dB
50	—	–33	–30	dB
60	—	–40	–30	dB
200	–1.8	–0.5	0	dB
300 to 3000	–0.125	±0.04	0.125	dB
3140	–0.57	0.01	0.125	dB
3380	–0.885	–0.7	0.015	dB
3980	—	–15.6	–13.3	dB
4600 and above	—	—	–32	dB

* 0 dBm0 signal input at VFxI.

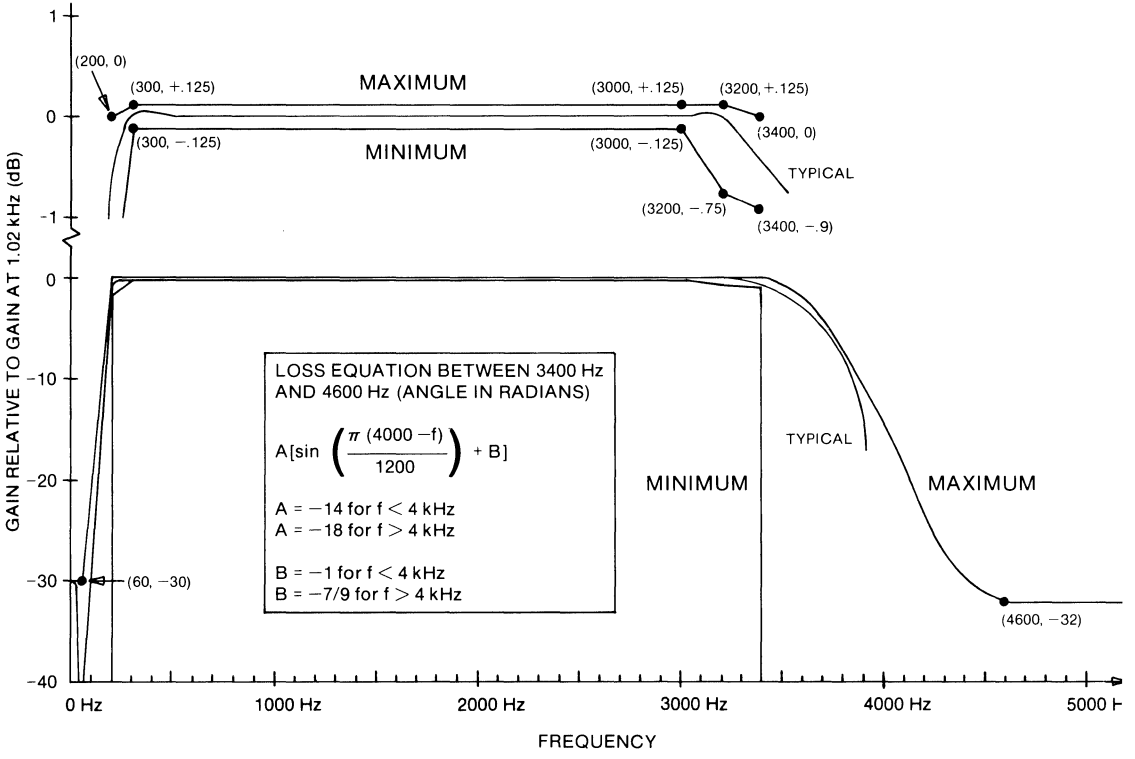


Figure 5. Transmit Filter Characteristics

Receive Filter Transfer Characteristics

Table 13. Receive Gain Relative to Gain at 1.02 kHz (GRX)*

Frequency (Hz)	Min	Typ	Max	Unit
Below 3000	–0.125	±0.04	0.125	dB
3140	–0.57	±0.04	0.125	dB
3380	–0.885	–0.58	–0.015	dB
3980	—	–15.7	–13.3	dB
4600 and above	—	—	–28	dB

* 0 dBm0 signal input at D_R.

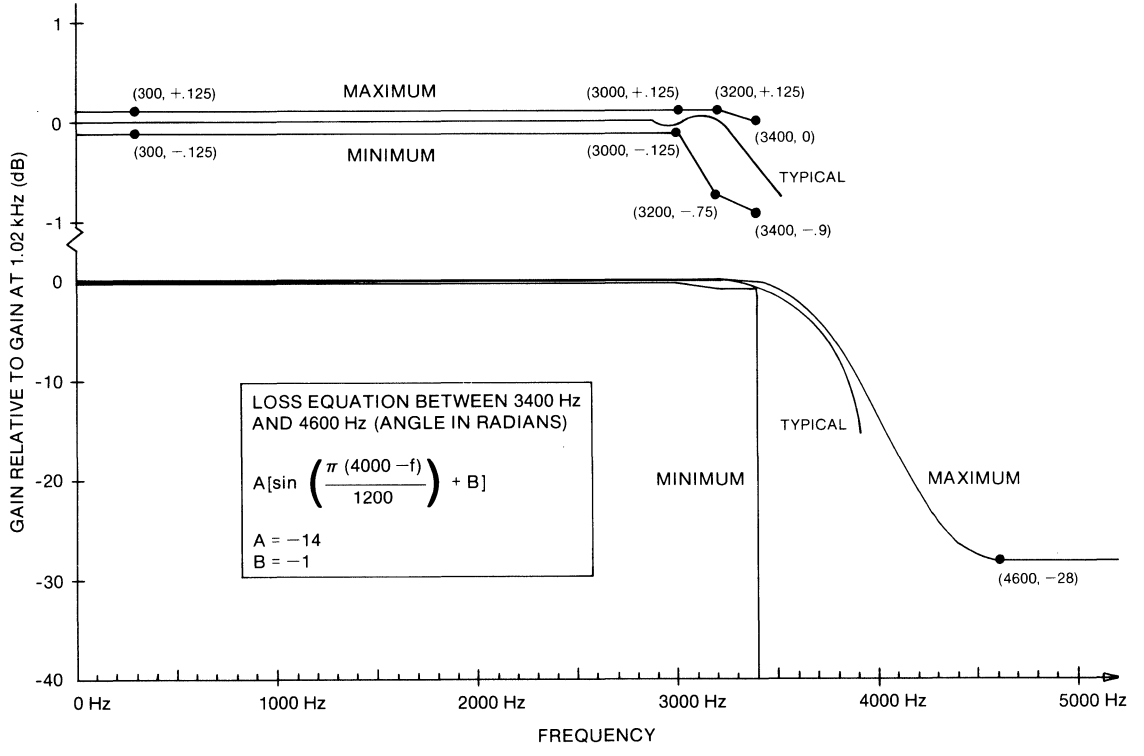


Figure 6. Receive Filter Characteristics

T7512 Dual PCM Codec with Filters

Features

- AT&T/CCITT-compatible
- Pin-selectable μ-law or A-law operation
- Transmit and receive gain control with external resistors
- Two timing modes
  - Fixed data rate mode (2.048 MHz)
  - Variable data rate mode (128 kHz to 2.048 MHz)
- On-chip voltage reference
- Differential output amplifier
- Single 5 V power supply
- TTL-compatible digital I/O
- Low-power CMOS technology

Description

The T7512 Dual PCM Codec with Filters integrated circuit provides two channels of analog-to-digital and digital-to-analog conversion as well as the transmit and receive filtering necessary to interface two voice telephone circuits to a time-division multiplexed system. The T7512 Codec is fabricated using low-power CMOS technology and requires a single 5 V supply. The device is available in a 28-pin plastic DIP or small-outline J-lead (SOJ) package for surface mounting.

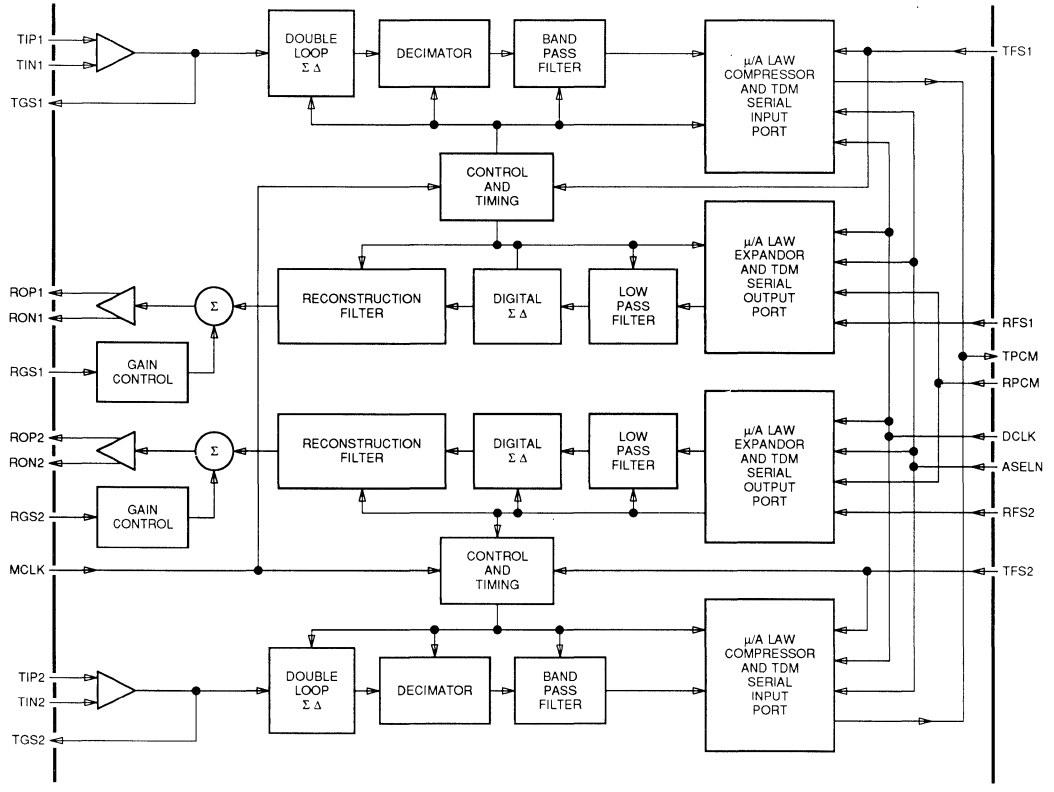


Figure 1. Block Diagram

User Information

Pin Descriptions

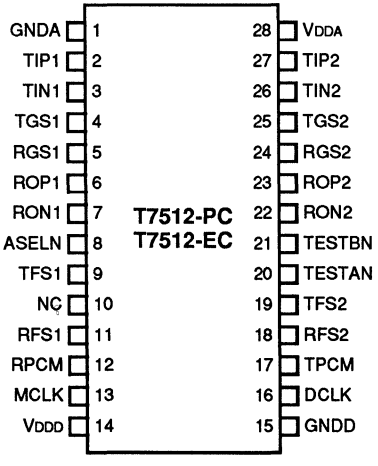


Figure 2. Pin Function Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Description
1	GNDA	—	**Analog Ground.** Ground reference (0 V) for internal analog circuitry. This pin and GNDD must be connected to the system ground.
2	TIP1	I	**Transmit Input (Positive) — Channel 1.** Noninverting analog input-to-input operational amplifier.
3	TIN1	I	**Transmit Input (Negative) — Channel 1.** Inverting analog input-to-input operational amplifier.
4	TGS1	O	**Transmit Gain Setting — Channel 1.** Output terminal of input operational amplifier. This pin should be connected to external gain control network of external resistors.
5	RGS1	I	**Receive Gain Setting — Channel 1.** Input to the gain setting network on the output power amplifier. The transmission level can be adjusted over a 12 dB range, depending on the voltage at RGS1.
6	ROP1	O	**Receive Output (Positive) — Channel 1.** Noninverting output of the power amplifier.
7	RON1	O	**Receive Output (Negative) — Channel 1.** Inverting output of the power amplifier.
8	ASELN	I	**A-law Selection (Negative-Assertion).** A low on this pin selects A-law operation; a high selects μ-law operation. An internal pull-up resistor is included so that, if ASELN is not connected, μ-law is automatically selected.
9	TFS1	I	**Transmit Frame Synchronization — Channel 1.** 8-kHz frame synchronization clock for transmit channel 1.
10	NC	—	**No Connection.** Not internally connected.
11	RFS1	I	**Receive Frame Synchronization — Channel 1.** 8-kHz frame synchronization clock for receive channel 1.
12	RPCM	I	**Receive PCM Data.** PCM data is clocked in on this lead on eight consecutive transitions of MCLK in fixed data rate mode (DCLK in variable data rate mode). The receive data for both channel 1 and channel 2 are input to this pin in a time-division multiplexed manner, as controlled by RFS1 and RFS2.
13	MCLK	I	**Master Clock.** 2.048-MHz master clock; also used as data clock for fixed data rate mode.
14	V_{DDD}	—	**Digital Power Supply.** 5 V power supply for all internal digital logic. Not internally connected to V_{DDA}.
15	GNDD	—	**Digital Ground.** Ground reference (0 V) for internal digital logic. This pin and GNDA must be connected to the system ground.
16	DCLK	I	**Data Clock.** A low on this pin selects the fixed data rate mode. In the variable rate mode, DCLK is the data clock for the transmit and receive channels for both channel 1 and channel 2.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Description
17	TPCM	O*	**Transmit PCM Data.** PCM data is clocked out on this lead on eight consecutive transitions of MCLK in fixed data rate mode (DCLK in variable data rate mode). The transmit data for both channel 1 and channel 2 are output on this pin in a time-division multiplexed manner, as controlled by TFS1 and TFS2.
18	RFS2	I	**Receive Frame Synchronization — Channel 2.** 8-kHz frame synchronization clock for receive channel 2.
19	TFS2	I	**Transmit Frame Synchronization — Channel 2.** 8-kHz frame synchronization clock for transmit channel 2.
20	TESTAN	I	**Test Pin A.** This pin is used for testing purposes. It should either be tied high or not connected. An internal pull-up resistor is included.
21	TESTBN	I	**Test Pin B.** This pin is used for testing purposes. It should either be tied high or not connected. An internal pull-up resistor is included.
22	RON2	O	**Receive Output (Negative) — Channel 2.** Inverting output of the power amplifier.
23	ROP2	O	**Receive Output (Positive) — Channel 2.** Noninverting output of the power amplifier.
24	RGS2	I	**Receive Gain Setting — Channel 2.** Input to the gain setting network on the output power amplifier. The transmission level can be adjusted over a 12 dB range, depending on the voltage at RGS2.
25	TGS2	O	**Transmit Gain Setting — Channel 2.** Output terminal of input operational amplifier. This pin should be connected to the external gain control network of the external resistors.
26	TIN2	I	**Transmit Input (Negative) — Channel 2.** Inverting analog input to uncommitted input operational amplifier.
27	TIP2	I	**Transmit Input (Positive) — Channel 2.** Noninverting analog input to uncommitted input operational amplifier.
28	V_{DDA}	—	**Analog Power Supply.** 5 V power supply for all internal analog circuitry. Not internally connected to V_{DDD}.

* Output is 3-stated.

Overview

The T7512 Dual PCM Codec with Filters provides analog-to-digital and digital-to-analog conversion for two voice channels. Transmit channel 1 and transmit channel 2 each convert an analog input to a companded digital PCM output. Receive channel 1 and receive channel 2 each convert a companded digital PCM input to an analog output.

Four separate 8-kHz frame synchronization signals control the input and output timing of the two channels. TFS1 and RFS1 control the timing of transmit channel 1 and receive channel 1, and TFS2 and RFS2 control the timing of transmit channel 2 and receive channel 2. The PCM data input to both receive channel 1 and receive channel 2 is time-division multiplexed on a single input (RPCM), and the

time slot of each channel is determined by RFS1 and RFS2. Data is input to RPCM serially, starting with the most significant bit (the sign bit). The PCM data output from both transmit channel 1 and transmit channel 2 is time-division multiplexed on a single output (TPCM), and the time slot of each channel is determined by TFS1 and TFS2. Data is output to TPCM serially, starting with the most significant bit (the sign bit).

Device operation requires application of a continuous 2.048-MHz master clock (MCLK). Operation of channel 1 requires application of both an 8-kHz transmit frame synchronization pulse (TFS1) and an 8-kHz receive frame synchronization pulse (RFS1). Operation of channel 2 requires application of both TFS2 and RFS2. The frame synchronization signals must be submultiples of MCLK. After applying power to the device, channel 1 becomes active after receiving four frames of TFS1, and channel 2 becomes active after receiving four frames of TFS2. (Since TFS is at 8 kHz, one frame is 125 μs.) Both channels should be activated during power-up to ensure that the device is properly initialized. Until channel 1 or channel 2 becomes active, its analog outputs (ROP1 or 2 and RON1 or 2) are floating and the TPCM output remains 3-stated. Once a channel becomes active, the internal analog circuitry is settled and conversion begins. The channel can be deactivated by removing its TFS signal (TFS = logic 0) for seven frames. The channel then powers down and draws a reduced power supply current (see Table 3). The channel can later be reactivated by applying TFS for four frames. Channel 1 and channel 2 can be deactivated independently, but the transmit and receive channels cannot be independently disabled by removal of only the TFS or RFS signal. Although both the TFS and RFS signals must be applied to operate a channel, these signals can be offset from one another by an arbitrary number of MCLK cycles.

The T7512 device allows two modes of data transmission: fixed rate or variable rate. The fixed data rate mode is selected when the data clock (DCLK) is a logic low and the master clock (MCLK) is used to clock input and output data. The TFS signal must be high for one master clock period to enable the channel to transmit PCM data serially onto TPCM on the next eight consecutive transitions of MCLK (see Figure 5). The RFS signal must be high for one master clock period to enable the channel to receive PCM data serially into RPCM on the next eight consecutive transitions of MCLK (see Figure 6).

The variable data rate mode allows the use of any frequency from 128 kHz to 2.048 MHz for (DCLK). When TFS makes a transition from low to high, the channel transmits PCM data on the next eight consecutive transitions of DCLK. If TFS remains high, transmission continues and, if it remains high for more than eight clock pulses of DCLK, the sample bits are repeated as long as TFS remains high (see Figure 7). When RFS makes a transition from low to high, the channel receives PCM data on the next eight consecutive transitions of DCLK. If RFS remains high, reception continues and, if it remains high for more than eight clock pulses of DCLK, sample bits continue to be input as long as RFS remains high (see Figure 8).

Since the device operates with only a single 5 V supply, the analog input and output signals swing at an internally generated midpoint reference level, not at ground. Therefore, it is necessary to use voice-quality capacitors to perform level shifting between the device reference and the system reference. It is also necessary that the digital input signal applied at RPCM not be a dc signal (besides idle), as oscillations may occur at the receive analog output.

The input of the transmit section uses an uncommitted input operational amplifier for each channel. The amp has a common mode range from 1.3 V to 4.3 V and a voltage gain of 100,000. The user has access to the inverting and noninverting inputs and to the feedback output to control the gain setting and hybrid interface. A gain of up to 20 dB can be accomplished without performance degradation (see Figure 3). The feedback load impedance, R1 + R2, must be greater than 10 kΩ in parallel with less than 50 pF. The input signal must be coupled through a voice-quality 0.1-μF capacitor with a 20% tolerance. The input op-amp can also be set to unity gain by connecting TGS to TIN.

The output of the receive section uses a differential output power amplifier for each channel. The output driver voltage ranges from 0.7 V to 3.7 V and provides both inverting and noninverting outputs. The gain is controlled by the feedback signal RGS and, when connected to ROP, the maximum attenuation of 12 dB is provided. Unity gain is obtained when RGS is connected to RON. Figure 4

shows a resistor network with the center tap connected to the input RGS. The gain can be adjusted within the 12 dB range by varying the resistor ratio R1:R2. The voice-quality 0.1-μF capacitors shown in Figure 4 are used to block the dc reference level at the ROP and RON output swings.

The ASELN pin is used for selecting either μ-law or A-law PCM encoding. Inverted binary format is used for μ-law encoding; alternate digit inversion is used for A-law transmission. A logic high selects μ-law operation and a logic low on ASELN selects A-law operation. If ASELN is not connected, an internal pull-up resistor automatically selects μ-law operation.

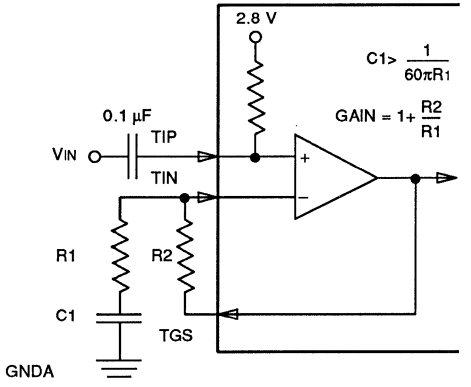
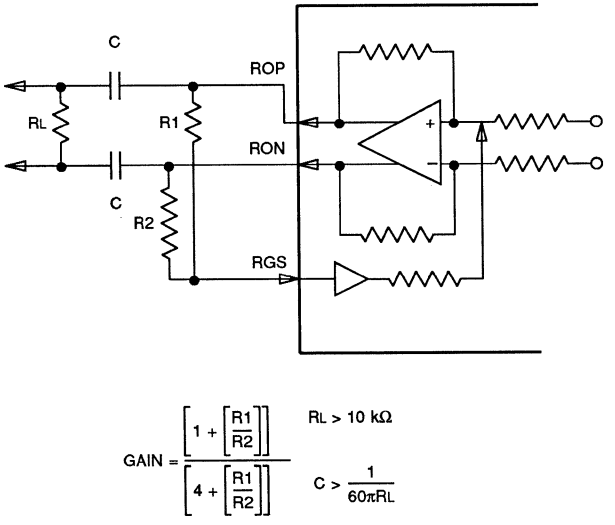


Figure 3. Uncommitted Operational Amplifier



$$GAIN = \frac{\left[1 + \left[\frac{R1}{R2}\right]\right]}{\left[4 + \left[\frac{R1}{R2}\right]\right]} \qquad R_L > 10\ k\Omega \qquad C > \frac{1}{60\pi R_L}$$

Figure 4. Differential Output Power Amplifier

Characteristics

DC Characteristics

T_A = 0 to 70 °C, V_{DDA} = 5 V ± 5%, V_{DDD} = 5 V ± 5%, GNDA = 0 V, GNDD = 0 V, unless otherwise specified. The input/output analog signals are 0 dBm0 at 1.02 kHz, the digital inputs are digital milliwatt at 1.02 kHz, the input and output amplifiers are set to unity gain, and the analog output is measured single-ended, unless otherwise specified. Typical values are for T_A = 25 °C and nominal power supply values.

Table 2. Digital Interface

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low-level input current	—	—	10	μA	V_{IL} = 0 V
I_{IH}	High-level input current	—	—	10	μA	V_{IH} = 5.5 V
V_{IL}	Input low voltage	—	—	0.8	V	—
V_{IH}	Input high voltage	2.0	—	—	V	—
V_{OL}	Output low voltage	—	—	0.4	V	I_{OL} = 5.1 mA
V_{OH}	Output high voltage	2.4	—	—	V	I_{OH} = –6.1 mA
C_I	Digital input capacitance	—	—	5	pF	—
	Output 3-state leakage current:					
I_{OZL}	low	—	—	30	μA	V_{OL} = 0 V
I_{OZH}	high	—	—	–30	μA	V_{OH} = 5.5 V

Table 3. Power Dissipation

Symbol	Parameter	Min	Typ	Max	Unit
I_{DDA2}	V_{DDA} operating current (both channels active)	—	30	35	mA
I_{DDD2}	V_{DDD} operating current (both channels active)	—	5	8	mA
P_2	Power dissipation (V_{DDA} and V_{DDD}; both channels active)	—	175	225	mW
I_{DDA1}	V_{DDA} operating current (one channel active, one channel inactive)	—	16	20	mA
I_{DDD1}	V_{DDD} operating current (one channel active, one channel inactive)	—	5	7	mA
P_1	Power dissipation (V_{DDA} and V_{DDD}; one channel active, one channel inactive)	—	105	142	mW
I_{DDA0}	V_{DDA} operating current (both channels inactive)	—	4	6	mA
I_{DDD0}	V_{DDD} operating current (both channels inactive)	—	2	3	mA
P_0	Power dissipation (V_{DDA} and V_{DDD}; both channels inactive)	—	30	47	mW
V_{DDA}	Analog operating voltage	4.75	5.0	5.25	V
V_{DDD}	Digital operating voltage	4.75	5.0	5.25	V

Maximum Ratings

Analog power supply voltage (V_{DDA}) ..... 7.5 V
Digital power supply voltage (V_{DDD}) ..... 7.5 V

Maximum ratings are defined as the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

Table 4. Analog Interface — Transmit Filter Input Stage

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
I_L	Input leakage current TIN1, TIN2	—	—	100	nA	$1.3\ V \leq V_{IN} \leq 4.3\ V$
R_I	Input resistance: TIN1, TIN2 TIP1, TIP2	 10 160	 — 200	 — —	 MΩ kΩ	 — —
C_{IL}	Input load capacitance TGS1, TGS2	—	—	20	pF	—
CMRR	Common mode rejection ratio TIP1, TIN1, TIP2, and TIN2	55	—	—	dB	$1.3\ V \leq V_{IN} \leq 4.3\ V$
A_O	DC open-loop voltage gain TGS1, TGS2	10,000	100,000	—	—	—
f_C	Open-loop unity gain bandwidth TGS1, TGS2	—	5	—	MHz	—

Table 5. Analog Interface — Receive Filter Driver Amplifier Stage

Symbol	Parameter	Min	Typ	Max	Unit
R_O	Output resistance for voice frequencies*	—	1	—	Ω
VO_{OFF}	Output DC offset between ROP1 or 2 and RON1 or 2, respectively	—	50	—	mV
C_{OL}	Output load capacitance*	—	—	50	pF
V_O	Maximum voltage output swing across R_L	0.7	—	3.7	V
R_L	Load resistance*	10	—	—	kΩ

* Measured at ROP1 or RON1, and ROP2 or RON2.

AC Characteristics — Transmission Parameters

Table 6. Gain and Dynamic Range

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
G_E	Encoder milliwatt response (transmit gain tolerance)	–0.18	±0.04	0.18	dBm0	Signal input = .7364 Vrms
G_D	Digital milliwatt response (receive gain tolerance)	–0.18	±0.04	0.18	dBm0	Signal input = .7364 Vrms

Table 7. Gain Tracking (Reference Level = 0 dBm0)

Symbol	Parameter	Min	Max	Unit	Test Conditions
$G_{TX\mu}$	Transmit gain tracking error (sinusoidal input; μ-law)	— —	±0.25 ±0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0
G_{TXA}	Transmit gain tracking error (sinusoidal input; A-law)	— —	±0.25 ±0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0
$G_{TR\mu}$	Receive gain tracking error (sinusoidal input; μ-law)	— —	±0.25 ±0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0
G_{TRA}	Receive gain tracking error (sinusoidal input; A-law)	— —	±0.25 ±0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0

Table 8. Noise

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
F_{XC}	Transmit idle channel noise (C-message weighted)	— —	16 —	18 23	dBrnC0 dBrnC0	μ-law A-law
F_{RC}	Receive idle channel noise (C-message weighted)	— —	7 —	11 13	dBrnC0 dBrnC0	μ-law A-law
F_{XP}	Transmit idle channel noise (psophometric weighted)	—	—	–67	dBm0p	A-law
F_{RP}	Receive idle channel noise (psophometric weighted)	—	—	–77	dBm0p	A-law
PSR_{XDDA}	V_{DDA} power supply rejection (transmit channel)	–50	–55	—	dB	Idle channel; 200-mVpp signal on supply; 0 kHz to 50 kHz; measured at TPCM
PSR_{XDDD}	V_{DDD} power supply rejection (transmit channel)	–50	–55	—	dB	Idle channel; 200-mVpp signal on supply; 0 kHz to 50 kHz; measured at TPCM
PSR_{RDDA}	V_{DDA} power supply rejection (receive channel)	–30	–35	—	dB	Idle channel; 200-mVpp signal on supply; 0 kHz to 50 kHz; measured at ROP1 or 2

Table 8. Noise (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
PSR_{RDDD}	V_{DDD} power supply rejection (receive channel)	–30	–35	—	dB	Idle channel; 200-mVpp signal on supply; 0 kHz to 50 kHz; measured at ROP1 or 2
FC_{XR}	Crosstalk (transmit channel 1 or 2 to receive channel 1 or 2)	—	—	–71	dB	0 dBm0 1.02 kHz at TIP1 or 2; RPCM = idle code; measured at ROP1 or 2 at 1.02 kHz
FC_{RX}	Crosstalk (receive channel 1 or 2 to transmit channel 1 or 2)	—	—	–71	dB	1.02 kHz DmW* on RPCM; TIP1 or 2 = GNDA; measured at TPCM at 1.02 kHz
FC_{XX}	Crosstalk (transmit channel 1 or 2 to transmit channel 2 or 1, respectively)	—	—	–71	dB	0 dBm0 1.02 kHz at TIP1 or 2; TIP2 or 1 = GNDA; measured at TPCM channel 2 or 1 at 1.02 kHz
FC_{RR}	Crosstalk (receive channel 1 or 2 to receive channel 2 or 1, respectively)	—	—	–71	dB	RPCM (channel 1 or 2) = DmW* at 1.02 kHz; RPCM (channel 2 or 1) = idle; measured at ROP2 or 1 at 1.02 kHz

* DmW = digital milliwatt.

Table 9. Distortion

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
D_{XS}	Transmit signal to distortion (sinusoidal input)	36	—	—	dB	0 to –30 dBm0
		30	—	—	dB	–30 to –40 dBm0
		25	—	—	dB	–40 to –45 dBm0
D_{RS}	Receive signal to distortion (sinusoidal input)	36	—	—	dB	0 to –30 dBm0
		30	—	—	dB	–30 to –40 dBm0
		25	—	—	dB	–40 to –45 dBm0
D_{XSF}	Transmit single frequency (distortion products)	—	—	–28	dBm0	0 ≤ input ≤ 2 MHz
		—	—	–40	dBm0	.2 ≤ input ≤ 3.4 kHz
D_{RSF}	Receive single frequency (distortion products)	—	—	–28	dBm0	0 ≤ input ≤ 2 MHz
		—	—	–40	dBm0	.2 ≤ input ≤ 3.4 kHz
D_{XD}	Transmit absolute delay	—	320	—	μs	Fixed data rate
D_{RD}	Receive absolute delay	—	280	—	μs	Fixed data rate
D_{DAA}	Delay distortion (analog to analog)	—	190	—	μs	f = 500 Hz
		—	30	—	μs	f = 1 kHz
		—	10	—	μs	f = 1.5 kHz
		—	50	—	μs	f = 2 kHz
		—	80	—	μs	f = 2.5 kHz
		—	250	—	μs	f = 3 kHz

Table 10. Transmit Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
16.67	–40	–40	–40	dB
50	–43	–43	–43	dB
60	–43	–43	–43	dB
200	–.25	–.18	–.11	dB
300 to 3000	–.125	.04	.125	dB
3140	.00	.08	.15	dB
3380	–.25	–.18	–.11	dB
3980	–15.6	–15.8	–16	dB
4600 and above	–38	—	—	dB

Table 11. Receive Gain Relative to Gain at 1.02 kHz

Frequency (Hz)	Min	Typ	Max	Unit
Below 3000	–0.125	±0.04	0.125	dB
3140	–0.15	±0.04	0.125	dB
3380	–0.89	–0.7	–0.6	dB
3980	–15	–15	–15	dB
4600 and above	–28	—	—	dB

AC Characteristics — Timing Parameters

Table 12. Clock Section (See Figures 5 and 6)

Symbol	Parameter	Min	Typ	Max	Unit
tMCHMCH	MCLK period	488	—	—	ns
tMCHMCL	MCLK pulse width	220	244	268	ns
tMCR	MCLK rise time	5	—	30	ns
tMCF	MCLK fall time	5	—	30	ns

Table 13. Transmit Section, Fixed Date Rate Mode (See Figure 5)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tMCHTPV	TPCM delay time	0	—	145	ns	0 < CLOAD < 100 pF
tMCLTPZ	Data float on TS exit	60	—	190	ns	0 < CLOAD < 100 pF
tMCHTFH	Frame sync delay	0	—	100	ns	—
tTFHTFL	Frame sync width	488	—	—	ns	—

Table 14. Receive Section, Fixed Data Rate Mode (See Figure 6)

Symbol	Parameter	Min	Typ	Max	Unit
tMCHRFH	Frame sync delay	10	—	100	ns
tRFHRFL	Frame sync width	488	—	—	ns
tRPVMCL	RPCM set-up time	10	—	100	ns
tMCLRPV	RPCM hold time	60	—	—	ns

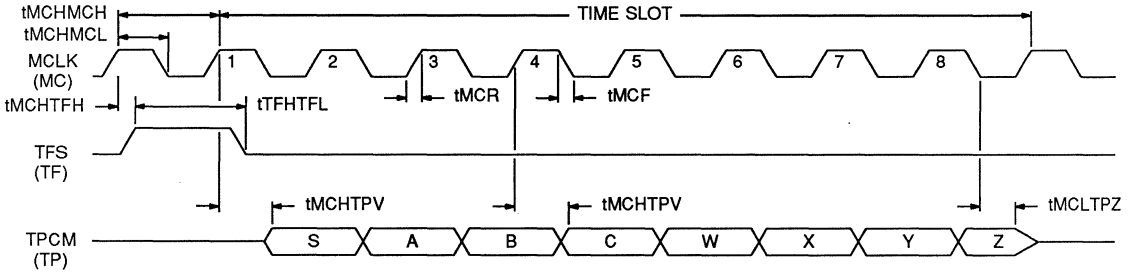


Figure 5. Fixed Data Rate Transmit Timing

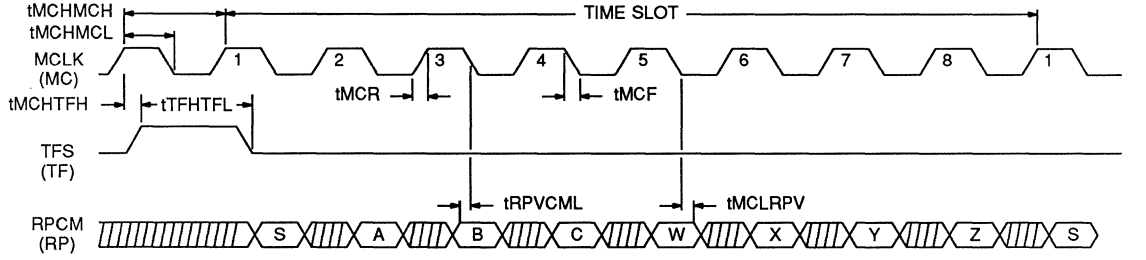


Figure 6. Fixed Data Rate Receive Timing

Table 15. Transmit Section, Variable Data Rate Mode (See Figure 7)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tTFHDCH	Time-slot delay from DCLK	–80	—	80	ns	—
tMCHTFH	Frame sync delay from MCLK	0	—	100	ns	—
tDCHTPV	TPCM delay from DCLK	0	—	100	ns	0 < CLOAD < 100 pF
tTFHTPA	Time slot to TPCM active	0	—	50	ns	0 < CLOAD < 100 pF
tTFLTPX	Time slot to TPCM inactive	0	—	80	ns	0 < CLOAD < 100 pF
tTFHTPV	TPCM delay from TFS	0	—	140	ns	—

Variable Data Rate Timing

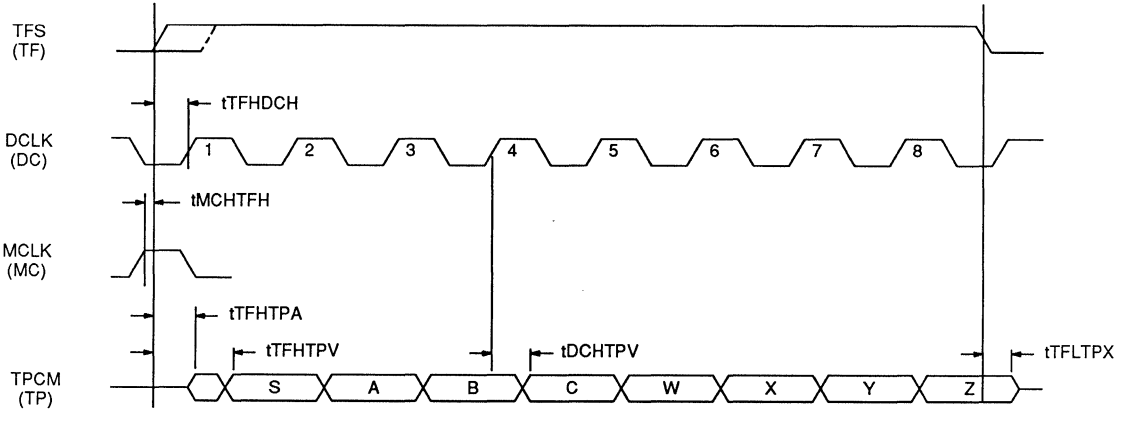


Figure 7. Variable Data Rate Transmit Timing

Table 16. Receive Section, Variable Data Rate Mode (See Figure 8)

Symbol	Parameter	Min	Typ	Max	Unit
tRFHDCH	Time-slot delay from DCLK	–80	—	80	ns
tMCHRFH	Frame sync delay	0	—	100	ns
tRPVDC	RPCM set-up time	10	—	—	ns
tDCRPX	RPCM hold time	60	—	—	ns
tDCHDCH	DCLK period	488	—	7812	ns
tDCLRFL	Time-slot end receive time	0	—	—	ns

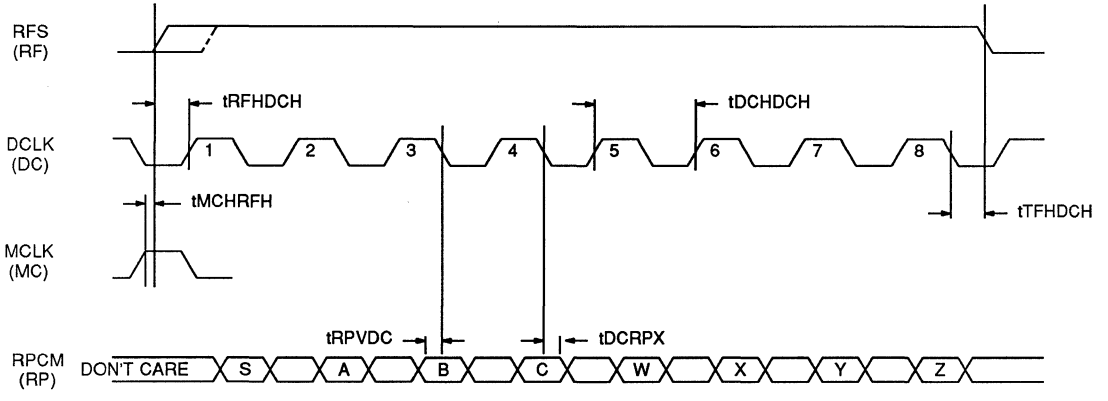


Figure 8. Variable Data Rate Receive Timing

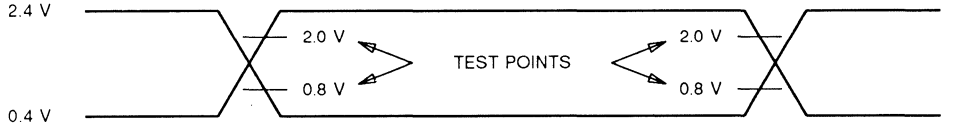


Figure 9. AC Testing Input/Output Waveform

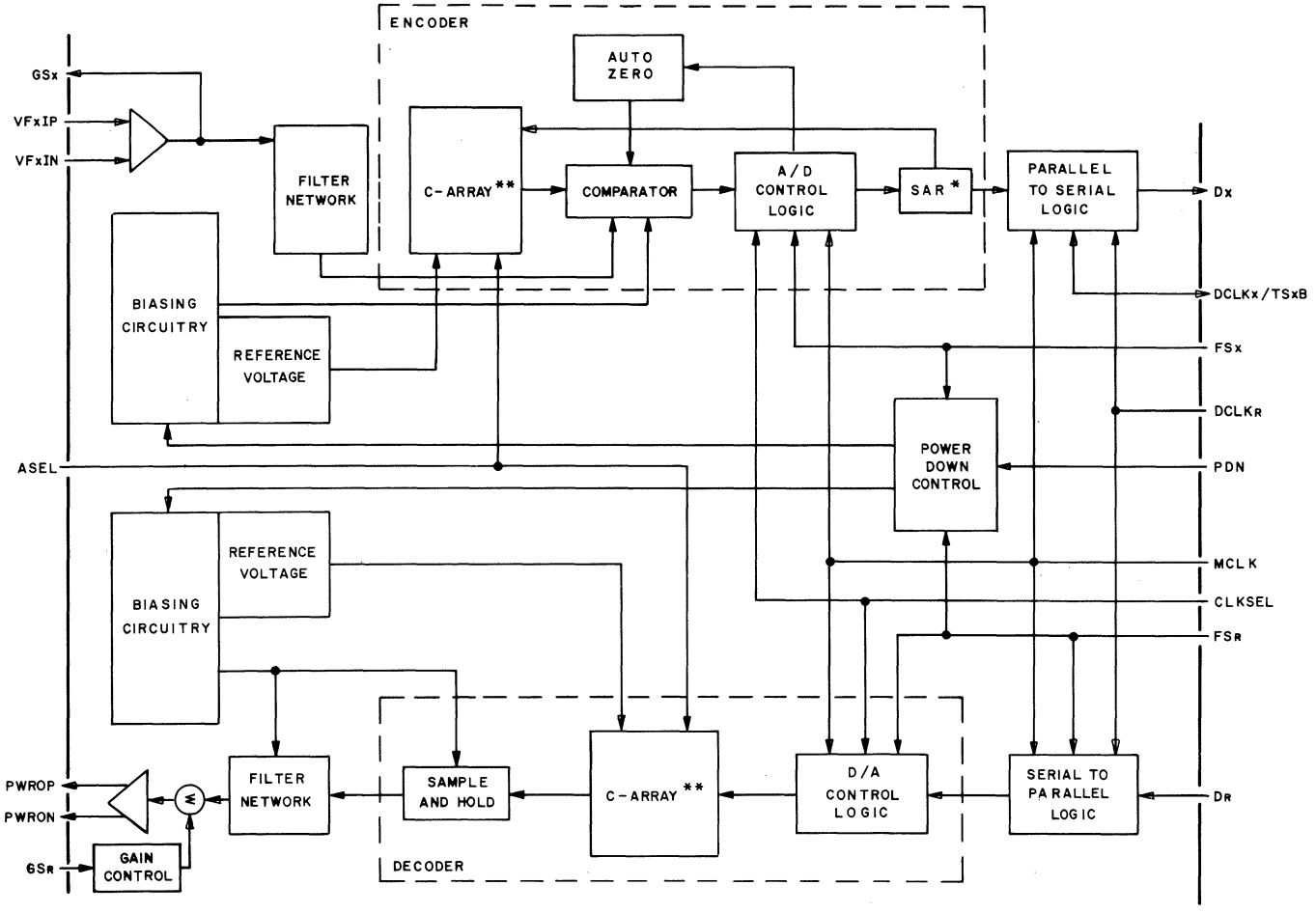
T7513 PCM Codec with Filters

Features

- AT&T/CCITT-compatible
- Pin-selectable μ-law or A-law operation
- Differential or single-ended analog input and output with gain setting
- Direct interface with transformer or electronic hybrids
- Variable data rate mode (64 kHz to 2.048 MHz)
- Outstanding noise performance
- On-chip precision voltage references
- No external components required
- $\pm$5 V operation
- CMOS technology for low power consumption
- Direct replacement for the industry-standard 2913 device
- Pin-selectable master clock rates of 2.048 MHz or 1.536 MHz

Description

The T7513 PCM Codec with Filters is a single-chip integrated circuit that provides analog-to-digital and digital-to-analog conversion; in addition, it provides the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed system. The T7513 device is available in a 20-pin plastic DIP or small-outline J-lead (SOJ) package for surface mounting.

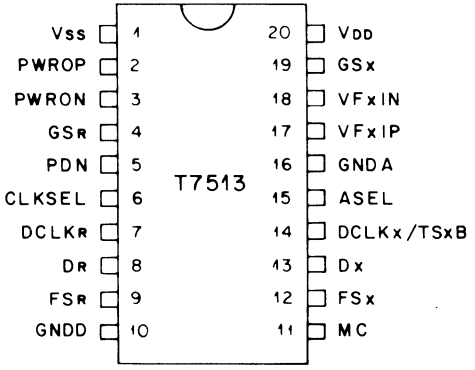


* Successive approximation register.
** Capacitor array.

Figure 1. Block Diagram

User Information

Pin Descriptions



Sym	Pin	Sym	Pin
ASEL	15	GSR	4
CLKSEL	6	GSx	19
DR	8	MC	11
Dx	13	PDN	5
DCLKR	7	PWRON	3
DCLKx/TSxB	14	PWROP	2
FSR	9	VDD	20
FSx	12	VSS	1
GNDA	16	VFxIN	18
GNDD	10	VFxIP	17

Figure 2. Pin Function Diagram (Both Packages) and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	VSS	—	**−5 V Supply** (± 5%).
2	PWROP	O	**Noninverting Output of Receive Power Amplifiers.** This pin can drive transformer hybrids or high-impedance loads directly in either a differential or single-ended configuration.
3	PWRON	O	**Inverting Output of Receive Power Amplifiers.** Functionally identical and complementary to PWROP.
4	GSR	I	**Receive Gain Setting Input.** Gain can be adjusted from 0 dB to −12 dB by using a resistive divider between PWROP and PWRON to vary the voltage at GSR.
5	PDN	I	**Power-Down Input.** A TTL-low on this pin places both the transmit and receive sections of the chip in power-down mode. When high or floating, the device functions normally.
6	CLKSEL	I	**Clock Select Input.** Must be tied to VDD (1.536 MHz) or VSS (2.048 MHz) to reflect the frequency applied to the MC input.
7	DCLKR	I	**Receive Data Clock.** When tied to VSS, fixed data rate operation is selected. When not tied to VSS, DCLKR is the TTL-level receive data clock, which operates at data rates from 64 kHz to 2.048 MHz.
8	DR	I	**Receive PCM Input.** On this input, data is clocked in on the first eight consecutive negative transitions of DCLKR (variable data rate mode) or MC (fixed data rate mode) following the rising edge of FSR.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
9	FS_R	I	**8-kHz Receive Frame Synchronization Clock.** In fixed data rate mode, FS_R must be high for a minimum of one MC cycle. In variable data rate mode, it must be held high for eight $DCLK_R$ cycles. The receive channel automatically enters the power-down mode whenever FS_R is TTL-low for approximately 300 ms.
10	GNDD	—	**Digital Ground.** Internally separate from GNDA.
11	MC	I	**TTL-Level Master Clock Input.** The MC frequency must be 2.048 MHz or 1.536 MHz, depending on the voltage at the CLKSEL input. In the fixed data rate mode, this input also acts as the transmit and receive data clock.
12	FSx	I	**8-kHz Transmit Frame Synchronization Clock.** Operates independently of, but in a manner analogous to, FS_R. The transmit channel automatically enters the power-down mode whenever FSx has been TTL-low for approximately 300 ms.
13	Dx	O	**Transmit PCM Output.** Data is clocked out on this lead on the first 8 consecutive positive transitions of DCLKx (in variable data rate mode) or MC (in fixed data rate mode) following the rising edge of FSx. Dx remains in a high-impedance state unless the transmit time slot is activated by the rising edge of FSx.
14	DCLKx/ TSxB	I/O	**Transmit Data Clock/Time-Slot Enable Strobe.** In variable data rate mode, DCLKx is a TTL-level input, which operates between 64 kHz and 2.048 MHz as the transmit data clock. In fixed mode, this pin is an open-drain output providing a time-slot enable strobe for use with an external 3-state buffer.
15	ASEL	I	**μ-law/A-law Select Input.** When tied to V_{SS}, A-law operation is selected. When tied to V_{DD} or GNDD, μ-law companding is selected.
16	GNDA	—	**Analog Ground.** Internally separate from GNDD.
17	VFxIP	I	**Noninverting Analog Input to Operational Amplifier.** Noninverting analog input to the uncommitted operational amplifier at the transmit filter input.
18	VFxIN	I	**Inverting Analog Input to Operational Amplifier.** Inverting analog input to the uncommitted operational amplifier at the transmit filter input.
19	GSx	O	**Output of Transmit Side Operational Amplifier.** Output of the transmit side uncommitted operational amplifier. Internally, this node is the positive input to the transmit differential filters.
20	V_{DD}	—	**+5 V Supply ($\pm$ 5%).**

Overview

The T7513 Codec is a synchronous device with a common master clock and independent synchronization and data timing signals for the transmit and receive channels. Permissible master clock frequencies are 2.048 MHz or 1.536 MHz. The chosen MC frequency must be reflected in the setting of the CLKSEL input. Data transfer on the Dx and D_R lines is initiated by a rising edge on the associated FS input; the data rate is determined by DCLK or by MC, depending on the mode of operation selected.

The variable rate data mode is selected by connecting DCLKx and DCLKR to the transmit and receive data clocks, respectively. In this mode, DCLKx and DCLKR are independent, asynchronous clocks that may vary in frequency from 64 kHz to 2.048 MHz and that need to be synchronized to MC only at the beginning of each frame. Data transmission on the Dx lead is initiated on the rising edge of FSx, with bit timing being determined by DCLKx. FSx is required to be high for a minimum of eight DCLKx cycles in order that the full data word be transmitted. Receive data transfer on the DR input is controlled by FSR and DCLK in an analogous but independent manner.

The fixed data rate mode is selected by strapping DCLKR to VSS. In the fixed data rate mode, data I/O is synchronized by the FSR and FSx inputs, but bit timing for both channels is determined by MC. The only available bit rates are 2.048 MHz or 1.536 MHz. FSR and FSx can operate independently and must be high for a minimum of one MC cycle. While in the fixed data rate mode, the DCLKx pin becomes an open-drain output that can be used to enable an external 3-state Dx buffer. (The internal Dx buffer continues to automatically enter a high-impedance mode whenever Dx is inactive.)

The T7513 Codec incorporates two power-down modes, which reduce power consumption and heat dissipation when the device is inactive. The entire chip can be put in power-down mode by placing a TTL-low signal on the PDN input. Additionally, the transmit and receive sides of the device power down independently whenever the frame synchronization signal for that side has been low for approximately 300 ms.

The T7513 device implements either μ-law or A-law PCM encoding. A-law operation is selected by strapping the ASEL input to VSS. For μ-law operation, ASEL should be tied to either VDD or GNDD. Alternate digit inversion is used for A-law transmission.

To overcome the inherently noisy nature of A-law companding, the T7513 incorporates an encoder squelch circuit that is enabled when A-law operation is selected. This circuit clamps the sign bit of the encoder output high after eight consecutive frames in which the magnitude of the encoded signal has been equal to ± 1 LSB. Squelching is immediately disengaged whenever the encoder output exceeds 1 LSB in magnitude. The squelch circuit is disabled during μ-law operation.

Zero transmission level points in Table 2 are specified relative to the digital milliwatt sequence prescribed by CCITT recommendation G.711 for a codec configured with unity gain, single-ended input (GSx tied VFxIN, input at VFxIP) and maximum gain, single-ended output (GSR tied to PWRON and output measured between PWROP and GNDA). Under these conditions, an analog input of 1.064 Vrms applied to VFxIP produces a 0 dBm digital code at Dx, while a 0 dBm code input at DR produces an output of 1.503 Vrms at PWROP.

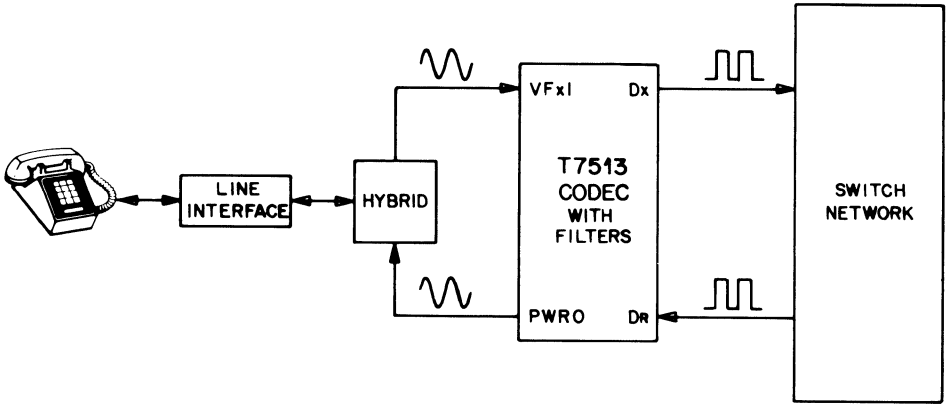


Figure 3. PCM System Block Diagram

Table 2. Zero Transmission Level Points

Symbol	Parameter	Value	Unit	Test Conditions
0TLP1X	Zero transmission level point (transmit channel at 0 dBm0, μ-law)	2.76 1.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
0TLP2X	Zero transmission level point (transmit channel at 0 dBm0, A-law)	2.79 1.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
0TLP1R	Zero transmission level point (receive channel at 0 dBm0, μ-law)	5.76 4.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
0TLP2R	Zero transmission level point (receive channel at 0 dBm0, A-law)	5.79 4.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω

Analog Input

The analog input section of the T7513 Codec includes an uncommitted input amplifier to provide maximum flexibility in interfacing with transmission systems. Possible applications include 2-to-4-wire conversion and/or gain adjustment. A schematic of the input circuit is shown in Figure 4. Note that a conventional single-ended unity gain configuration is achieved by simply connecting GSx to VFxIN and applying the analog signal between VFxIP and GNDA. The load impedance to ground at the GSx output should be greater than 10 kΩ in parallel with less than 50 pF.

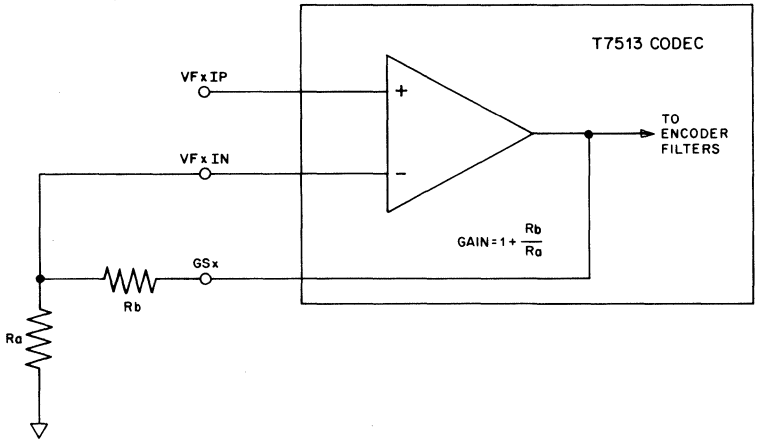


Figure 4. Analog Inputs

Analog Output

The analog output of the T7513 device is provided via a set of low-impedance, complementary outputs, PWROP and PWRON. Either of the outputs can be used as a single-ended output to drive loads as low as 300 Ω or, alternatively, the outputs can be used together to provide a 600-Ω differential drive capability. Receive gain is set by interpolating the voltage at the buffered, high-impedance GSR input between the voltages at the PWROP and PWRON nodes with a resistive divider network. Gain varies from 0 dB to −12 dB, according to the relationship shown in the equation

$$A = \left[\frac{1 + \left(\frac{R1}{R2}\right)}{4 + \left(\frac{R1}{R2}\right)}\right]$$

where R1 and R2 are connected as shown in Figure 5 and the output is taken single-ended. Note that maximum gain (A = 1) is achieved with GSR tied to PWRON (R1/R2 = ∞) and that minimum output (A = 1/4) is achieved by connecting GSR to PWROP (R1/R2 = 0). For proper device operation, it is recommended that R1 and R2 be chosen such that R1 + R2 > 10 kΩ and that the parallel combination of R1 and R2 is less than 100 kΩ.

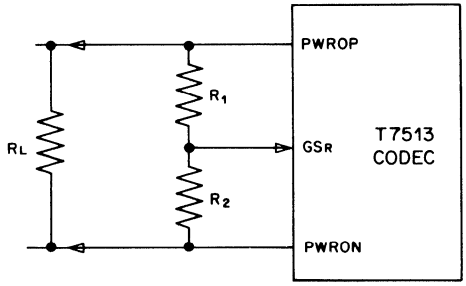


Figure 5. Analog Outputs

Characteristics

Except where indicated, minimum and maximum specifications are end-of-life limits as used for reliability testing. T7513 Codecs are required to meet these limits after undergoing an accelerated aging regimen that simulates 40 years of product life. Production test limits are tighter than indicated to guarantee full-rated performance after aging.

For all tests: T_A = 0 to 85 °C, V_{DD} = 5 V ± 5%, V_{SS} = –5 V ± 5% and GNDA = GNDD = 0 V, unless otherwise noted. Typical values are for T_A = 25 °C and nominal supply values.

DC Characteristics

Table 3. Digital Interface

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low-level input current	–20	—	—	μA	GNDD ≤ V_{IN} ≤ V_{IL}
I_{IH}	High-level input current	—	—	20	μA	V_{IH} ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input low voltage	—	—	0.8	V	—
V_{IH}	Input high voltage	2.0	—	—	V	—
V_{OL}	Output low voltage	—	—	0.4	V	—
V_{OH}	Output high voltage	2.4	—	—	V	—
C_I	Digital input capacitance	—	—	5	pF	—
I_L	Output leakage current	–50	—	50	μA	—

Table 4. Power Dissipation

Symbol	Parameter	Min	Typ	Max	Unit
I_{DD1}	V_{DD} operating current	—	11.5	16	mA
I_{SS1}	V_{SS} operating current	—	–10.5	–15	mA
I_{DD0}	V_{DD} power-down current	—	2.5	4.5	mA
I_{SS0}	V_{SS} power-down current	—	–1.5	–3.0	mA
V_{CC}	Positive operating voltage	4.75	5.0	5.25**	V
V_{SS}	Negative operating voltage	–4.75	–5.0	–5.25**	V
P_1	Operating power dissipation	—	110	155	mW
P_0	Power-down dissipation	—	20	37	mW

* All measurements are made at fMC = fDCLK = 2.048 MHz, outputs unloaded.
** Absolute maximum ratings are V_{DD} = +7.5 V, V_{SS} = –7.5 V. Exceeding these values may result in permanent internal damage.

Table 5. Analog Interface — Transmit Filter Input Stage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input leakage current, VFxI+, VFxI–	—	—	100	nA	$-2.17\ V \leq V_{IN} \leq 2.17\ V$
R_{IXI}	Input resistance, VFxI+, VFxI–	10	—	—	MΩ	—
V_{OSXI}	Input offset voltage, VFxI+, VFxI–	—	—	25	mV	—
CMRR	Common mode rejection, VFxI+, VFxI–	55	—	—	dB	$-2.17\ V \leq V_{IN} \leq 2.17\ V$
A_{VOL}	DC open-loop voltage gain, GSx	5000	—	—	—	—
fC	Open-loop unity gain bandwidth, GSx	— —	1 1	— —	MHz MHz	— —
C_{LXI}	Load capacitance, GSx	—	—	50	pF	—
R_{LXI}	Minimum load resistance, GSx	10	—	—	kΩ	—

Table 6. Analog Interface — Receive Filter Driver Amplifier Stage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output resistance, PWRO+, PWRO–	—	1	—	Ω	—
V_{OSRA}	Single-ended output DC offset, PWRO+, PWRO–	—	±30	±150	mV	Relative to GNDA
C_{LRA}	Load capacitance, PWRO+, PWRO–	—	—	100	pF	—

AC Characteristics — Transmission Parameters

Unless otherwise noted, the analog input is a 0 dBm0, 1020-Hz sine wave; the input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020-Hz sine wave through an ideal encoder. The receive output is measured single-ended, maximum gain configuration. All output levels are (sin x)/x corrected. Specifications are for synchronous operation.

Note: Unity gain input amplifier: GSx is connected to VFx1–, signal input VFx1+; maximum gain output amplifier: GSR is connected to PWRO–, output to PWRO+.

Table 7. Gain and Dynamic Range

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
EmW	Encoder milliwatt response (transmit gain tolerance)	–0.15	±0.04	0.15	dBm0	Signal input of 1.064 Vrms, μ-law; signal input of 1.068 Vrms, A-law; ± 5% supplies, 0 to 85 °C
DmW	Digital milliwatt response (receive gain tolerance)	–0.15	±0.04	0.15	dBm0	Measured relative to 0TLPR; PCM input of 0 dBm0, 1020 kHz; ± 5% supplies, 0 to 85 °C

Table 8. Gain Tracking — Reference Level = 1.02 kHz, 0 dBm0

Symbol	Parameter	Min	Max	Unit	Test Conditions
GT1x	Transmit gain tracking error (sinusoidal input, μ-law)	–0.25 –0.50	0.25 0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0
GT2x	Transmit gain tracking error (sinusoidal input, A-law)	–0.25 –0.50	0.25 0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0
GT1R	Receive gain tracking error (sinusoidal input, μ-law)	–0.25 –0.50	0.25 0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0
GT2R	Receive gain tracking error (sinusoidal Input, A-law)	–0.25 –0.50	0.25 0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0

Table 9. Distortion

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
SDx	Transmit signal to distortion (sinusoidal input = 1.02 kHz):					
	μ-law	36	—	—	dB	3 ≤ VFxI ≤ –30 dBm0
	A-law	35	—	—	dB	
	μ-law	30	—	—	dB	–30 < VFxI ≤ –40 dBm0
	A-law	29	—	—	dB	
	μ-law	25	—	—	dB	–40 < VFxI ≤ –45 dBm0
	A-law	25	—	—	dB	
SDR	Transmit signal to distortion (sinusoidal input = 1.02 kHz):					
	μ-law	36	—	—	dB	3 ≤ DR ≤ –30 dBm0
	A-law	35	—	—	dB	
	μ-law	30	—	—	dB	–30 < DR ≤ –40 dBm0
	A-law	29	—	—	dB	
	μ-law	25	—	—	dB	–40 < DR ≤ –45 dBm0
	A-law	25	—	—	dB	
DPx	Transmit single frequency	—	—	–28	dBm0	0 ≤ input ≤ 2 MHz
	distortion products	—	—	–40	dBm0	.2 ≤ input ≤ 3.4 kHz
DPR	Receive single frequency	—	—	–28	dBm0	0 ≤ input ≤ 2 MHz
	distortion products	—	—	–40	dBm0	.2 ≤ input ≤ 3.4 kHz
DAX	Transmit absolute delay	—	340	—	μs	—
DAR	Receive absolute delay	—	100	—	μs	—
DDAA	Delay distortion	—	200	—	μs	f = 500 Hz
	(analog-to-analog)	—	60	—	μs	f = 1 kHz
		—	60	—	μs	f = 1.5 kHz
		—	100	—	μs	f = 2 kHz
		—	150	—	μs	f = 2.5 kHz
		—	340	—	μs	f = 3 kHz
—	Intermodulation (end-to-end)	—	–50	–35	dB	CCITT G.712 (8.1)
—	Intermodulation (end-to-end)	—	–60	–49	dBm0	CCITT G.712 (8.2)
—	Spurious out-of-band	—	–35	–25	dBm0	CCITT G.712 (7.1)
	signals (end-to-end)	—	–35	–25	dBm0	CCITT G.712 (7.1)

Table 10. Noise

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
NXC	Transmit idle channel noise (C-message weighted)	— —	— 1	18 15	dBrnC0 dBrnC0	μ-law, EOL* μ-law, BOL*
NRC	Receive idle channel noise (C-message weighted)	—	4	13	dBrnC0	μ-law
NXP	Transmit idle channel noise (psophometric weighted)	—	–69	–67	dBm0p	A-law
NXR	Receive idle channel noise (psophometric weighted)	—	–81	–75	dBm0p	A-law
PSRR1	VDD power supply rejection (transmit channel)	–30	–35	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at Dx
PSRR2	VSS power supply rejection (transmit channel)	–30	–35	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at Dx
PSRR3	VDD power supply rejection (receive channel)	–30	–35	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at PWROP
PSRR4	VSS power supply rejection (receive channel)	–30	–35	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at PWROP
CTXR	Crosstalk (transmit to receive, single-ended outputs) μ-law	—	—	–70	dB	VFxIP = 2.76 dBm0; 1.02-kHz signal measured at PWROP, DR = idle code
CTRX	Crosstalk (receive to transmit single-ended outputs) μ-law	—	—	–70	dB	DR = 0 dBm0; 1.02-kHz signal measured at DX VFxIP = GNDA; 1.02-kHz signal measured at Dx

* EOL = end of life; BOL = beginning of life. See the introduction to the Characteristics section.

Receive Filter Transfer Characteristics (Figure 6)

Table 11. Receive Gain Relative to Gain at 1.02 kHz (GRR)*

Frequency (Hz)	Min	Typ	Max	Unit
Below 3000	−0.125	±0.04	0.125	dB
3140	−0.57	±0.04	0.125	dB
3380	−0.885	−0.58	−0.015	dB
3980	—	−15.7	−13.3	dB
4600 and above	—	—	−28	dB

* 0 dBm0 signal input at DR.

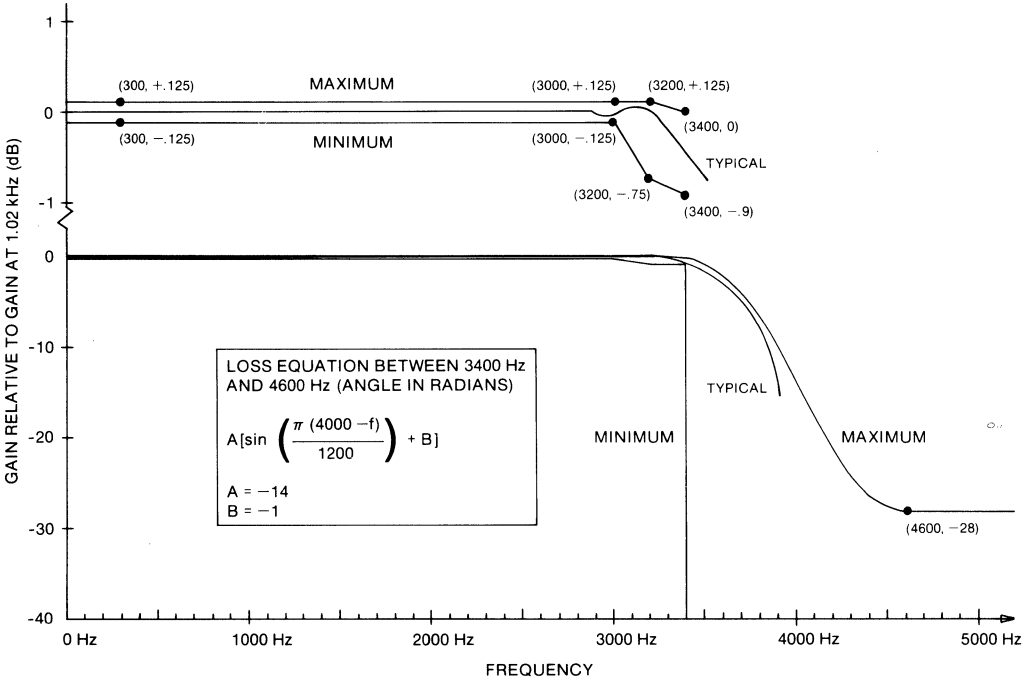


Figure 6. Receive Filter Characteristics

Table 12. Transmit Filter Transfer Characteristics (Figure 7)
Transmit Gain Relative to Gain at 1.02 kHz (GRX)*

Frequency (Hz)	Min	Typ	Max	Unit
16.67	—	–35	–30	dB
50	—	–33	–30	dB
60	—	–40	–30	dB
200	–1.8	–0.5	0	dB
300 to 3000	–0.125	±0.04	0.125	dB
3140	–0.57	0.01	0.125	dB
3380	–0.885	–0.7	0.015	dB
3860	—	–9.9	–8.98	dB
4600 and above	—	—	–32	dB

* 0 dBm0 signal input at VFxIP.

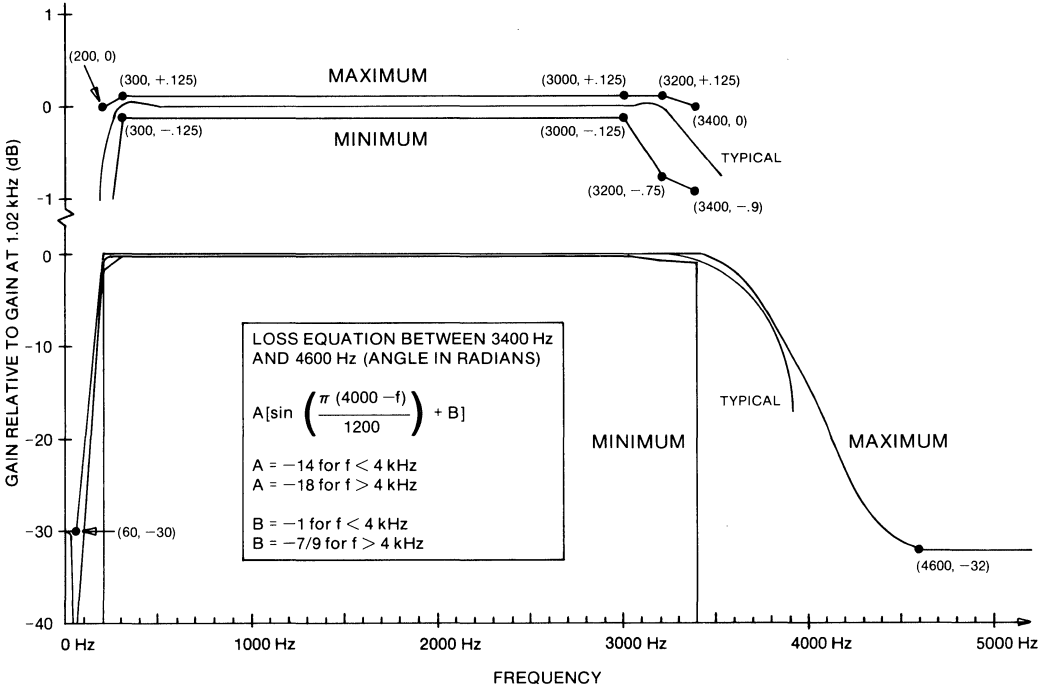


Figure 7. Transmit Filter Characteristics

Timing Characteristics

Table 13. Clock Section (Figures 8, 9, 10, and 11)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tMCHMCH	Clock period, MC	488	—	—	ns	fMC = 2.048 MHz
tMCHMCL1	Clock pulse width, MC	220	—	—	ns	—
tDCLK	Data clock pulse width	220	—	—	ns	64 kHz ≤ fDCLK ≤ 2.048 MHz
tCDC	Clock duty cycle, MC	45	50	55	%	—
tMCH1MCH2, tMCL2MCL1	Clock rise and fall time	5	—	30	ns	—

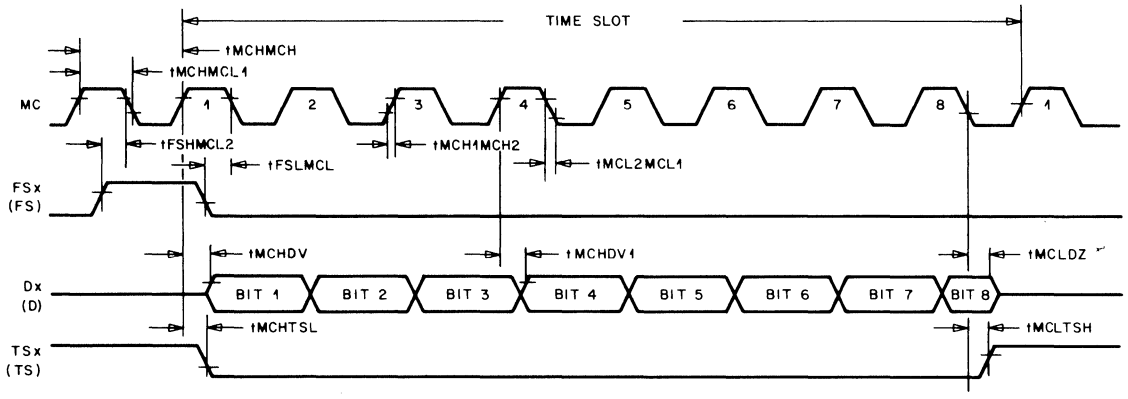
Table 14. Transmit Section, Fixed Data Rate Mode* (Figure 8)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tMCHTDV	Data enabled on TS entry	0	—	145	ns	0 < CLOAD < 250 pF
tMCHDV1	Data delay from MC	0	—	145	ns	0 < CLOAD < 250 pF
tMCLDZ	Data float on TS exit	60	—	215	ns	CLOAD = 0
tMCHTSL	Time-slot X to enable	0	—	145	ns	0 < CLOAD < 250 pF
tMCLTSH	Time-slot X to disable	60	—	215	ns	CLOAD = 0
tFSHMCL2	Frame sync delay	100	—	tMCHMCH – 100	ns	—

* Timing parameters tMCHTSV, tMCLDZ, and tMCLTSH are referenced to a high-impedance state.

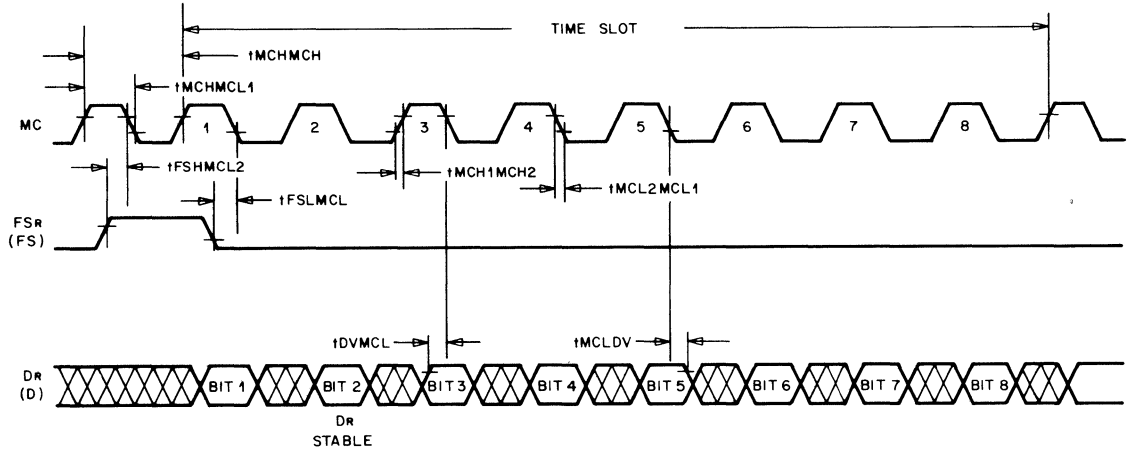
Table 15. Receive Section, Fixed Data Rate Mode (Figure 9)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tDVMCL	Receive data set-up	10	—	—	ns	—
tMCLDV	Receive data hold	60	—	—	ns	—
tFSLMCL	Frame sync delay	100	—	tMCHMCH – 100	ns	—



Note: All timing parameters referenced to V_{IH} and V_{IL} except tMCHTSV, tMCTSH, tMCLDZ, which reference a high-impedance state.

Figure 8. Fixed Data Rate Transmit Timing



Note: All timing parameters referenced to V_{IH} and V_{IL}.

Figure 9. Fixed Data Rate Receive Timing

Table 16. Transmit Section, Variable Data Rate Mode (Figure 10)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tFSHDCL	Time-slot delay from DCLKx*	140	—	tDX – 140	ns	—
tFSHMCL	Frame sync delay	100	—	tMCHMCH – 100	ns	—
tDCHDV	Data delay from DCLKx	0	—	100	ns	0 < CLOAD < 250 pF
tFSHDV	Time slot to Dx active**	0	—	50	ns	0 < CLOAD < 250 pF
tFSLDX	Time slot to Dx inactive**	0	—	80	ns	0 < CLOAD < 250 pF
tDX	Data clock period	488	—	15620	ns	64 kHz < fDCLKx < 2.048 MHz
tFSHDV1	Data delay from FSx	0	—	140	ns	—

* tFSLX minimum requirements override tFSHDCL maximum spec for 64-kHz operation.
** Timing parameters tFSHDY and tFSLDX are referenced to a high-impedance state.

Table 17. Receive Section, Variable Data Rate Mode (Figure 11)

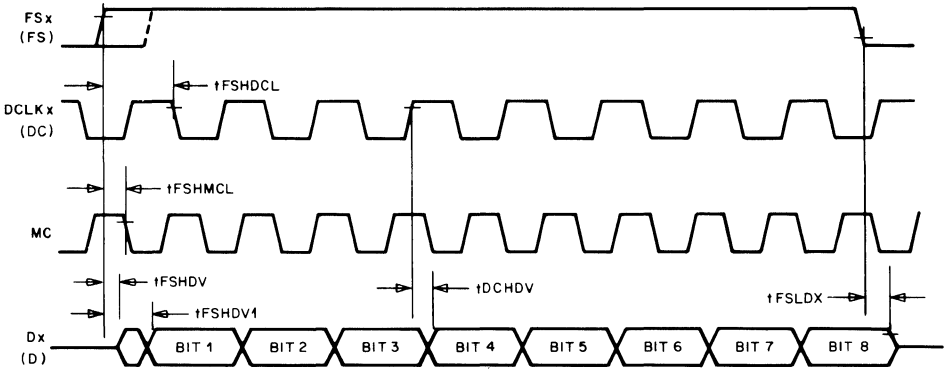
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tFSHDCL	Time-slot delay from DCLKR*	140	—	tDR – 140	ns	—
tFSHMCL	Frame sync delay	100	—	tMCHMCH – 100	ns	—
tDVDCL	Data set-up time	10	—	—	ns	—
tDCLDX	Data hold time	60	—	—	ns	—
tDR	Data clock period	488	—	15620	ns	64 kHz < fDCLKx < 2.048 MHz
tDCLFSL	Time-slot end receive time	60	—	—	ns	—

* tFSLR minimum requirements override tFSHDCL maximum spec for 64-kHz operation.

Table 18. 64-kHz Operation, Variable Data Rate Mode

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tFSLX*	Transmit frame sync minimum downtime	488	—	—	ns	FSx is TTL-high for remainder of frame
tFSLR**	Receive frame sync minimum downtime	1952	—	—	ns	FSR is TTL-high for remainder of frame
tDCLK	Data clock pulse width	—	—	10	μs	—

* tFSLX minimum requirements override tFSHDCL maximum spec for 64-kHz operation.
** tFSLR minimum requirements override tFSHDCL maximum spec for 64-kHz operation.



Note: All timing parameters referenced to VIH and VIL except tFSHDA and tFSLDX, which reference a high-impedance state.

Figure 10. Variable Data Rate Transmit Timing

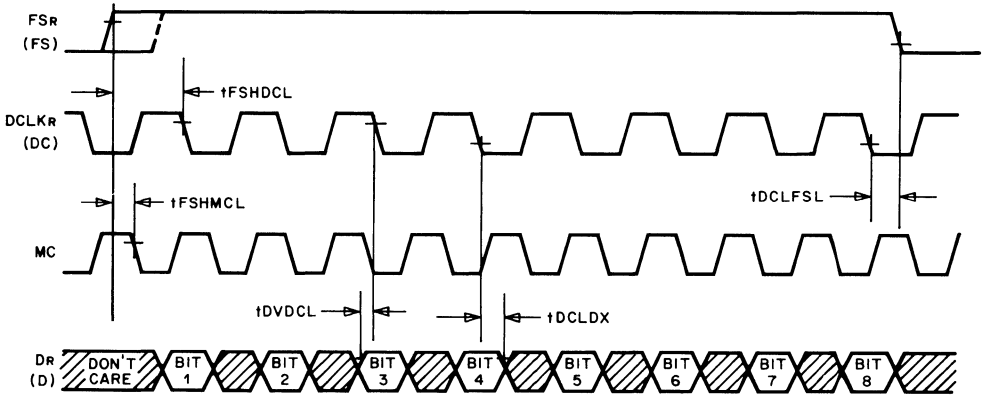


Figure 11. Variable Data Rate Receive Timing

Note: AC testing – inputs are driven at 2.4 V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at 2.0 V for a logic 1 and 0.8 V for a logic 0.

Figure 12. AC Testing Input/Output Waveform

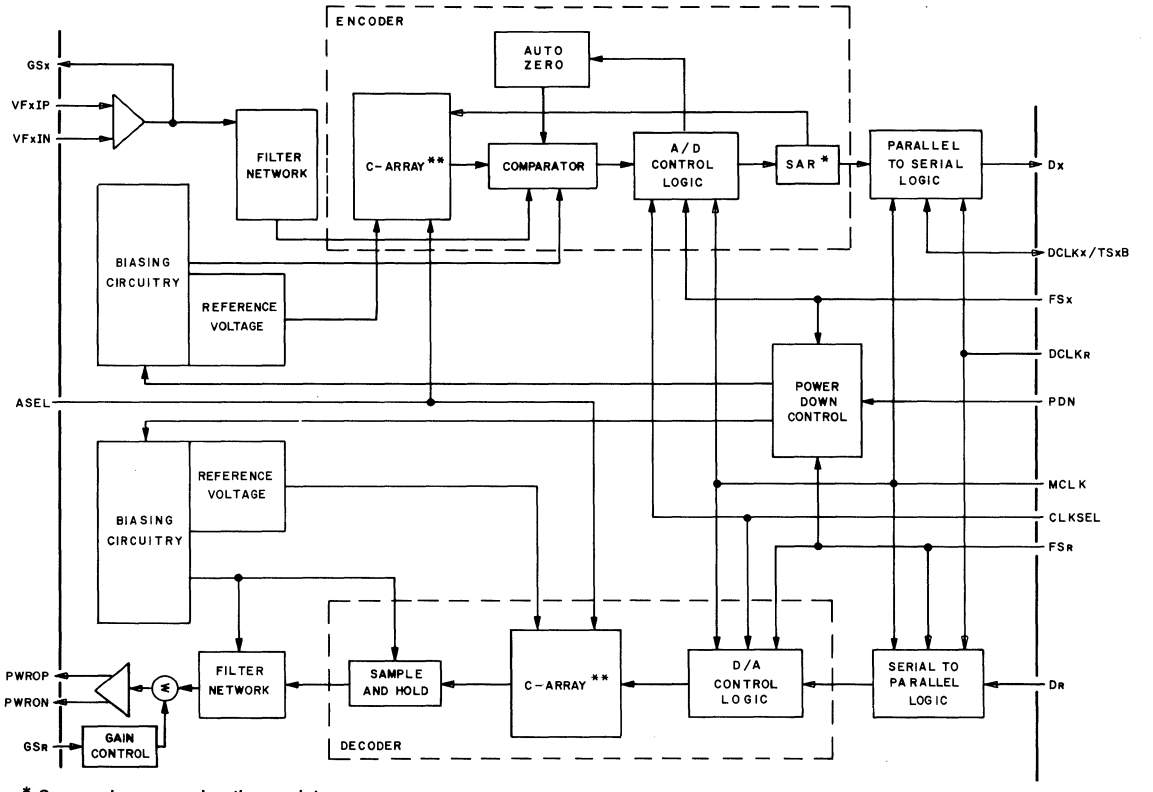
T7513A PCM Codec with Filters

Features

- Direct replacement for the industry-standard 2913 device
- Low-power, latchup-free CMOS technology
  - 65-mW typical operating power dissipation
  - 5-mW typical power-down dissipation
- Differential architecture for high noise immunity and PSRR
- Pin-selectable master clock rates of 2.048 MHz, 1.544 MHz, or 1.536 MHz
- Two timing modes
  - Fixed data rate: 2.048 MHz, 1.544 MHz, or 1.536 MHz
  - Variable data rate: 64 kHz to 2.048 MHz
- On-chip sample and hold, autozero, and precision voltage reference – no external components required
- Excellent noise performance
- Pin-selectable μ-law or A-law operation

Description

The T7513A PCM Codec with Filters is a single-chip integrated circuit that provides analog-to-digital and digital-to-analog conversion; in addition, it provides the transmit and receive filtering necessary to interface a voice telephone circuit to a time-division multiplexed system. The T7513A is a direct replacement for the T7513, offering enhanced functionality and significantly reduced power consumption. The T7513A is available in a 20-pin plastic DIP or small outline J-lead (SOJ) package for surface mounting.

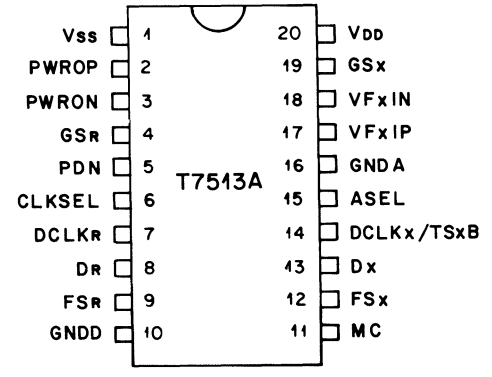


* Successive approximation register.
** Capacitor array.

Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
ASEL	15	GSR	4
CLKSEL	6	GSx	19
DR	8	MC	11
Dx	13	PDN	5
DCLKR	7	PWRON	3
DCLKx/TSxB	14	PWROP	2
FSR	9	VDD	20
FSx	12	Vss	1
GNDA	16	VFxIN	18
GNDD	10	VFxIP	17

Figure 2. Pin Function Diagram (Both Packages) and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	V_{SS}	—	**–5 V Supply (± 5%).**
2	PWROP	O	**Noninverting Output of Receive Power Amplifiers.** Can drive transformer hybrids or high-impedance loads directly in either a differential or single-ended configuration.
3	PWRON	O	**Inverting Output of Receive Power Amplifiers.** Functionally identical and complementary to PWROP.
4	GS_R	I	**Receive Gain Setting Input.** Gain can be adjusted from 0 dB to –12 dB by varying the voltage at GS_R.
5	PDN	I	**Power Down Input.** A TTL-low on this pin places both the transmit and receive sections of the chip in power-down mode. When high or floating, the device functions normally.
6	CLKSEL	I	**Clock Select Input.** Must be tied to V_{SS} (2.048 MHz), GNDD (1.544 MHz), or V_{DD} (1.536 MHz) to reflect the frequency applied to the MC input.
7	$DCLK_R$	I	**Receive Data Clock.** When tied to V_{SS}, fixed data rate operation is selected. When not tied to V_{SS}, $DCLK_R$ is the TTL-level receive data clock, which operates at data rates from 64 kHz to 2.048 MHz.
8	D_R	I	**Receive PCM Input.** Data is clocked in on this input on the first eight consecutive negative transitions of $DCLK_R$ (variable data rate mode) or MC (fixed data rate mode) following the rising edge of FS_R.
9	FS_R	I	**8-kHz Receive Frame Synchronization Clock.** In fixed data rate mode, FS_R must be high for a minimum of one MC cycle. In variable data rate mode, it must be held high for a minimum of eight $DCLK_R$ cycles.
10	GNDD	—	**Digital Ground.** Internally separate from GNDA.
11	MC	I	**TTL-Level Master Clock Input.** MC frequency must be 2.048 MHz, 1.544 MHz, or 1.536 MHz, depending on the voltage at the CLKSEL input. In the fixed data rate mode, this input also acts as the transmit and receive data clock.
12	FS_X	I	**8-kHz Transmit Frame Synchronization Clock.** Operates independently of, but in a manner analogous to, FS_R.
13	D_X	O	**Transmit PCM Output.** Data is clocked out on this lead on the first eight consecutive positive transitions of $DCLK_X$ (in variable data rate mode) or MC (in fixed data rate mode) following the rising edge of FS_X. D_X remains in a high-impedance state unless the transmit time slot is activated by the rising edge of FS_X.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
14	DCLKx/ TSxB	I/O	**Transmit Data Clock/Time-Slot Enable Strobe.** In variable data rate mode, DCLKx is a TTL-level input that operates between 64 kHz and 2.048 MHz as the transmit data clock. In fixed data rate mode, this pin is an open-drain output providing a time-slot enable strobe for use with an external 3-state buffer.
15	ASEL	I	**μ-law/A-law Select Input.** When tied to VSS, A-law operation is selected. When tied to VCC or GNDD, μ-law companding is selected.
16	GNDA	—	**Analog Ground.** Internally separate from GNDD.
17	VFxIP	I	**Noninverting Analog Input to Operational Amplifier.** Noninverting analog input to the uncommitted operational amplifier at the transmit filter input.
18	VFxIN	I	**Inverting Analog Input to Operational Amplifier.** Inverting analog input to the uncommitted operational amplifier at the transmit filter input.
19	GSx	O	**Output of Transmit Side Operational Amplifier.** Output of the transmit side uncommitted operational amplifier. Internally, this node is the positive input to the transmit differential filters.
20	VDD	—	**+5 V Supply ($\pm$ 5%).**

General Operation

System Reliability Features

The T7513A Codec is powered-up whenever the following criteria are met: VDD and VSS power supply voltages are applied, all required clocks are active (MC for fixed data rate mode; MC, DCLKx, and DCLKR for variable data rate mode), a TTL-high is applied to PDN, and both the FSx and FSR synchronization are applied.

On the transmit channel, the digital outputs Dx and TSxB are held in a high-impedance state for approximately 500 μs after power-up. After this delay, during which the control circuits are initialized, the digital outputs are functional and occur in the proper time slot.

The encoder analog circuitry includes an autozero circuit that requires about 60 ms to reach an equilibrium value after power-up. Thus, although the digital outputs are active after approximately four frames, the PCM output is not initially a valid representation of the analog input.

To further protect the integrity of the PCM highway, the T7513A includes a lost clock detection circuit, which places the Dx and TSxB outputs in a high-impedance state approximately 20 μs after an interruption of MC.

Power-Down and Standby Modes

The T7513A device provides two power-down modes of operation that reduce power consumption when the device is inactive. Full power-down mode is activated by placing a TTL-low signal on the PDN input. In this mode power consumption is reduced to approximately 5 mW. Standby mode is automatically entered whenever both FSx and FSR have been TTL-low for approximately 300 ms. Reactivating either or both of the frame sync signals restores full operation. Standby power is approximately 10 mW.

During both power-down and standby operation, the digital outputs DX and TSXB and the analog outputs PWROP and PWRON enter a high-impedance state. The digital outputs become active immediately upon exiting standby or within approximately 500 μs after leaving power-down. In both cases, approximately 60 ms is required to recover analog functionality.

Digital Interface

The T7513A digital interface uses a common master clock and independent synchronization and timing signals for the transmit and receive channels. Permissible master clock frequencies are 2.048 MHz, 1.544 MHz, or 1.536 MHz. The chosen MC frequency must be reflected in the setting of the CLKSEL input. Two operating modes are provided for the PCM interface: fixed data rate and variable data rate.

The variable data rate mode is selected by connecting DCLKX and DCLKR to the system transmit and receive data clocks, respectively. In this mode, DCLKX and DCLKR are independent, asynchronous clocks that may vary in frequency from 64 kHz to 2.048 MHz and that need to be synchronized to MC only at the beginning of each frame. Data transmission on the DX lead is initiated on the rising edge of FSX, with bit timing being determined by DCLKX. FSX is required to be high for a minimum of eight DCLKX cycles in order for the full PCM word be transmitted; if FSX is held higher longer than eight cycles, the DX data is repeated as long as FSX is high. Receive data transfer is initiated on the rising edge of the FSR pulse, with bit timing being controlled by DCLKR. Variable data rate timing is illustrated in Figures 10 and 11.

The fixed data rate mode is selected by strapping DCLKR to VSS. In the fixed data rate mode, data I/O is synchronized by the FSX and FSR inputs, but data timing for both channels is controlled by MC. Because bit timing is determined by MC, the only available bit rates are 2.048 MHz, 1.544 MHz, and 1.536 MHz. FSX and FSR must be high for a minimum of one MC cycle and can be operated independently. While in the fixed data rate mode, the DCLKX pin becomes an open-drain output that can be used to enable an external 3-state buffer. The internal DX buffer continues to automatically enter a high-impedance state whenever DX is inactive. Fixed data rate timing is illustrated in Figures 8 and 9.

Companding Laws

The T7513A device supports both μ-law and A-law operation. A-law operation is selected by strapping the ASEL input to VSS. For μ-law operation, ASEL should be tied to either VDD or GNDD; it should never be left floating. Alternate digit inversion is used for A-law transmission.

To overcome the inherently noisy nature of A-law companding, the T7513A incorporates an encoder squelch circuit that is enabled when A-law operation is selected. This circuit clamps the sign bit of the encoder output high after eight consecutive frames in which the magnitude of the encoded signal has been equal to ±1 LSB. Squelching is immediately disengaged whenever the encoder output exceeds 1 LSB in magnitude. The squelch circuit is disabled during μ-law operation.

Transmission Levels

Zero transmission level points in Table 2 are specified relative to the digital milliwatt sequence prescribed by CCITT recommendation G.711 for a codec configured with unity gain, single-ended input (GSX tied to VFXIN, input at VFXIP) and maximum gain, single-ended output (GSR tied to PWRON, output measured between PWROP and GNDA). Under these conditions, an analog input of 1.064 Vrms applied to VFXIP produces a 0 dBm digital code, while a 0 dBm code input at DR produces an output of 1.503 Vrms at PWROP.

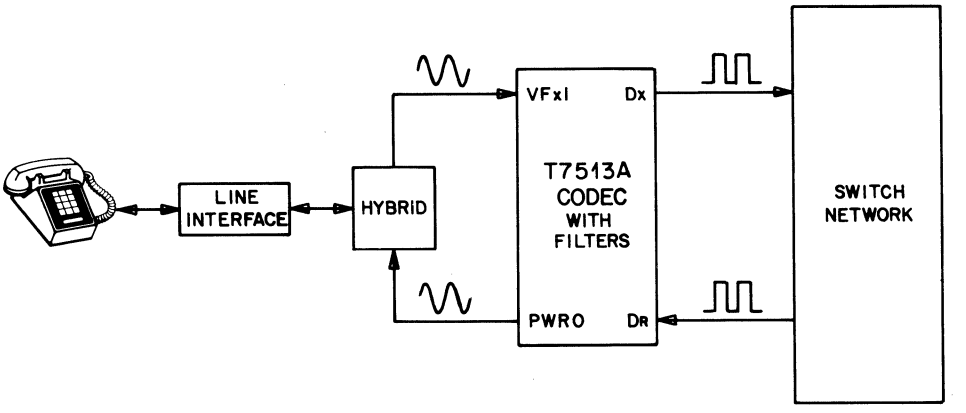


Figure 3. PCM System Block Diagram

Table 2. Zero Transmission Level Points

Symbol	Parameter	Value	Unit	Test Condition
0TLP1X	Zero transmission level point (transmit channel at 0 dBm0, μ-law)	2.76 1.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
0TLP2X	Zero transmission level point (transmit channel at 0 dBm0, A-law)	2.79 1.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
0TLP1R	Zero transmission level point (receive channel at 0 dBm0, μ-law)	5.76 4.00	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω
0TLP2R	Zero transmission level point (receive channel at 0 dBm0, A-law)	5.79 4.03	dBm dBm	Referenced to 600 Ω Referenced to 900 Ω

Analog Input

The analog input section of the T7513A device includes an uncommitted input amplifier to provide maximum flexibility in interfacing with transmission systems. Possible applications include 2-to-4-wire conversion and/or gain adjustment. A schematic of the input circuit is shown in Figure 4. Note that a conventional single-ended unity gain configuration is achieved by simply connecting GSx to VFxIN and applying the analog signal between VFxIP and GNDA. The load impedance to ground at the GSx output should be greater than 10 kΩ in parallel with less than 50 pF.

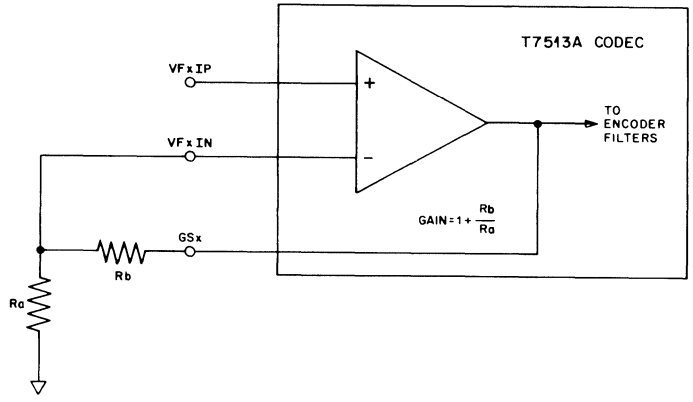


Figure 4. Analog Inputs

Analog Output

The analog output of the T7513A device is provided via a set of low-impedance complementary outputs, PWROP and PWRON. Either of the outputs can be used as a single-ended output to drive loads as low as 300 Ω or, alternatively, the outputs can be used together to provide a 600-Ω differential drive capability. Receive gain is set by interpolating the voltage at the buffered, high-impedance GSR input between the voltages at the PWROP and PWRON nodes with a resistive divider network. Gain varies from 0 dB to −12 dB, according to the relationship shown in the equation:

$$A = \left[\frac{1 + \left(\frac{R1}{R2}\right)}{4 + \left(\frac{R1}{R2}\right)}\right]$$

where R1 and R2 are connected as shown in Figure 5 and the output is taken single-ended. Note that maximum gain (A = 1) is achieved with GSR tied to PWRON (R1/R2 = ∞) and that minimum output (A = 1/4) is achieved by connecting GSR to PWROP (R1/R2 = 0). For proper device operation, it is recommended that R1 and R2 be chosen such that R1 + R2 > 10 kΩ and that the parallel combination of R1 and R2 is less than 100 kΩ.

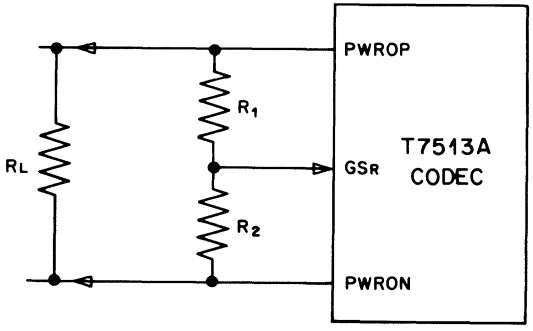


Figure 5. Analog Outputs

Network

Characteristics

Except where noted, minimum and maximum specifications are end-of-life limits as used for reliability testing. T7513A Codecs are required to meet these limits after undergoing an accelerated aging regimen that simulates 40 years of product life. Production test limits are tighter than indicated to guarantee full-rated performance after aging.

For all tests: T_A = 0 to 85 °C, V_{CC} = 5 V ± 5%, V_{SS} = –5 V ± 5%, and GNDA = GNDD = 0 V, unless otherwise noted. Typical values are for T_A = 25 °C and nominal supply values.

DC Characteristics

Table 3. Digital Interface

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{IL}	Low-level input current	–20	—	—	μA	GNDD ≤ V_{IN} ≤ V_{IL}
I_{IH}	High-level input current	—	—	20	μA	V_{IH} ≤ V_{IN} ≤ V_{CC}
V_{IL}	Input low voltage	—	—	0.8	V	—
V_{IH}	Input high voltage	2.0	—	—	V	—
V_{OL}	Output low voltage	—	—	0.4	V	—
V_{OH}	Output high voltage	2.4	—	—	V	—
C_I	Digital input capacitance	—	—	5	pF	—
I_L	Output leakage current	–50	—	50	μA	—

Table 4. Power Dissipation*

Symbol	Parameter	Min	Typ	Max	Unit
I_{DD1}	V_{DD} operating current	—	7	9	mA
I_{SS1}	V_{SS} operating current	—	6	8	mA
I_{DD0}	V_{DD} power-down current	—	0.5	1	mA
I_{SS0}	V_{SS} power-down current	—	0.5	1	mA
V_{CC}	Positive operating voltage	4.75	5.0	5.25**	V
V_{SS}	Negative operating voltage	–4.75	–5.0	–5.25**	V
P_1	Operating power dissipation	—	65	85	mW
P_0	Power-down dissipation	—	5	10	mW

* All measurements are made at fMC = fDCLK = 2.048 MHz, outputs unloaded.
** Absolute maximum ratings are V_{DD} = +7.5 V, V_{SS} = –7.5V. Exceeding these values may result in permanent internal damage.

Table 5. Analog Interface — Transmit Filter Input Stage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{BX1}	Input leakage current, VFxI+, VFxI–	—	—	100	nA	$-2.17\ V \leq V_{IN} \leq 2.17\ V$
R_{IXI}	Input resistance, VFxI+, VFxI–	10	—	—	MΩ	—
V_{OSXI}	Input offset voltage, VFxI+, VFxI–	—	—	25	mV	—
CMRR	Common mode rejection, VFxI+, VFxI–	55	—	—	dB	$-2.17\ V \leq V_{IN} \leq 2.17\ V$
A_{VOL}	DC open-loop voltage gain, GSx	5000	—	—	—	—
fC	Open-loop unity gain bandwidth, GSx	—	1	—	MHz	—
C_{LXI}	Load capacitance, GSx	—	—	50	pF	—
R_{LXI}	Minimum load resistance, GSx	10	—	—	kΩ	—

Table 6. Analog Interface — Receive Filter Driver Amplifier Stage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{ORA}	Output resistance, PWRO+, PWRO–	—	1	—	Ω	—
V_{OSRA}	Single-ended output DC offset, PWRO+, PWRO–	—	±30	±150	mV	Relative to GNDA
C_{LRA}	Load capacitance, PWRO+, PWRO–	—	—	100	pF	—

AC Characteristics — Transmission Parameters

Unless otherwise noted, the analog input is a 0 dBm0, 1020-Hz sine wave; the input amplifier is set for unity gain, noninverting. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1020-Hz sine wave through an ideal encoder. The receive output is measured single-ended, maximum gain configuration. All output levels are (sin x)/x corrected. Specifications are for synchronous operation.

Note: Unity gain input amplifier: GSx is connected to VFx1–, signal input VFx1+; maximum gain output amplifier: GS_R is connected to PWRO–, output to PWRO+.

Table 7. Gain and Dynamic Range

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
EmW	Encoder milliwatt response (transmit gain tolerance)	–0.15	±0.04	0.15	dBm0	Signal input of 1.064 Vrms, μ-law; signal input of 1.068 Vrms, A-law; ± 5% supplies, 0 to 85 °C
DmW	Digital milliwatt response (receive gain tolerance)	–0.15	±0.04	0.15	dBm0	Measured relative to 0TLPR; PCM input of 0 dBm0, 1020 kHz; ± 5% supplies, 0 to 85 °C
—	Relative gain PWROP to PWRON	—	±0.01	—	dB	D_R = 0 dBm0, f = 300—3400 Hz
—	Relative phase PWROP to PWRON	—	±0.25	—	Deg	D_R = 0 dBm0, f = 300—3500 Hz

Table 8. Gain Tracking — Reference Level = 1.02 kHz, 0 dBm0

Symbol	Parameter	Min	Max	Unit	Test Conditions
GT1X	Transmit gain tracking error (sinusoidal input, μ-law)	–0.25 –0.50	0.25 0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0
GT2X	Transmit gain tracking error (sinusoidal input, A-law)	–0.25 –0.50	0.25 0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0
GT1R	Receive gain tracking error (sinusoidal input, μ-law)	–0.25 –0.50	0.25 0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0
GT2R	Receive gain tracking error (sinusoidal input, A-law)	–0.25 –0.50	0.25 0.50	dB dB	+3 to –37 dBm0 –37 to –50 dBm0

Table 9. Distortion

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
SDX	Transmit signal to distortion (sinusoidal input = 1.02 kHz):					
	μ-law	36	—	—	dB	3 ≤ VFXI ≤ –30 dBm0
	A-law	35	—	—	dB	
	μ-law	30	—	—	dB	–30 < VFXI ≤ –40 dBm0
	A-law	29	—	—	dB	
	μ-law	25	—	—	dB	–40 < VFXI ≤ –45 dBm0
	A-law	25	—	—	dB	
SDR	Transmit signal to distortion (sinusoidal input = 1.02 kHz):					
	μ-law	36	—	—	dB	3 ≤ DR ≤ –30 dBm0
	A-law	35	—	—	dB	
	μ-law	30	—	—	dB	–30 < DR ≤ –40 dBm0
	A-law	29	—	—	dB	
	μ-law	25	—	—	dB	–40 < DR ≤ –45 dBm0
	A-law	25	—	—	dB	
DPX	Transmit single frequency	—	—	–28	dBm0	0 ≤ input ≤ 2 MHz
	distortion products	—	—	–40	dBm0	.2 ≤ input ≤ 3.4 kHz
DPR	Receive single frequency	—	—	–28	dBm0	0 ≤ input ≤ 2 MHz
	distortion products	—	—	–40	dBm0	.2 ≤ input ≤ 3.4 kHz
DAX	Transmit absolute delay	—	340	—	μs	—
DAR	Receive absolute delay	—	100	—	μs	—
DDAA	Delay distortion	—	200	—	μs	f = 500 Hz
	(analog-to-analog, measure	—	60	—	μs	f = 1 kHz
	relative to minimum)	—	60	—	μs	f = 1.5 kHz
		—	100	—	μs	f = 2 kHz
		—	150	—	μs	f = 2.5 kHz
		—	340	—	μs	f = 3 kHz
—	Intermodulation (end-to-end)	—	–50	–35	dB	CCITT G.712 (8.1)
—	Intermodulation (end-to-end)	—	–60	–49	dBm0	CCITT G.712 (8.2)
—	Spurious out-of-band signals	—	–35	–25	dBm0	CCITT G.712 (7.1)
	(end-to-end)	—	–35	–25	dBm0	CCITT G.712 (7.1)

Table 10. Noise

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
NXC	Transmit idle channel noise (C-message weighted)	— —	— 1	18 15	dBrnC0 dBrnC0	μ-law, EOL* μ-law, BOL*
NRC	Receive idle channel noise (C-message weighted)	—	4	13	dBrnC0	μ-law
NXP	Transmit idle channel noise (psophometric weighted)	—	–69	–67	dBm0p	A-law
NXR	Receive idle channel noise (psophometric weighted)	—	–81	–75	dBm0p	A-law
PSRR1	VDD power supply rejection (transmit channel)	–30	–45	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at Dx.
PSRR2	VSS power supply rejection (transmit channel)	–30	–45	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at Dx.
PSRR3	VDD power supply rejection (receive channel)	–30	–45	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at PWROP.
PSRR4	VSS power supply rejection (receive channel)	–30	–45	—	dB	Idle channel; 100-mVpp, 1.02-kHz signal on dc supply; measured 1.02-kHz signal at PWROP.
CTXR	Crosstalk (transmit to receive, single-ended outputs) μ-law	— —	 –90	 –70	 dB	VFxIP = 2.76 dBm0; 1.02-kHz signal measured at PWROP, DR = idle code
CTRX	Crosstalk (receive to transmit single-ended outputs) μ-law	— —	 –90	 –70	 dB	DR = 0 dBm0; 1.02-kHz signal measured at DX VFxIP = GNDA; 1.02-kHz signal measured at Dx

* EOL = end of life; BOL = beginning of life. See the introduction to the Characteristics section.

Receive Filter Transfer Characteristics (Figure 6)

Table 11. Receive Gain Relative to Gain at 1.02 kHz (GRR)*

Frequency (Hz)	Min	Typ	Max	Unit
Below 3000	–0.125	±0.04	0.125	dB
3140	–0.57	±0.04	0.125	dB
3380	–0.885	–0.58	–0.015	dB
3860	—	–10.7	–8.98	dB
4600 and above	—	—	–28	dB

* 0 dBm0 signal input at DR.

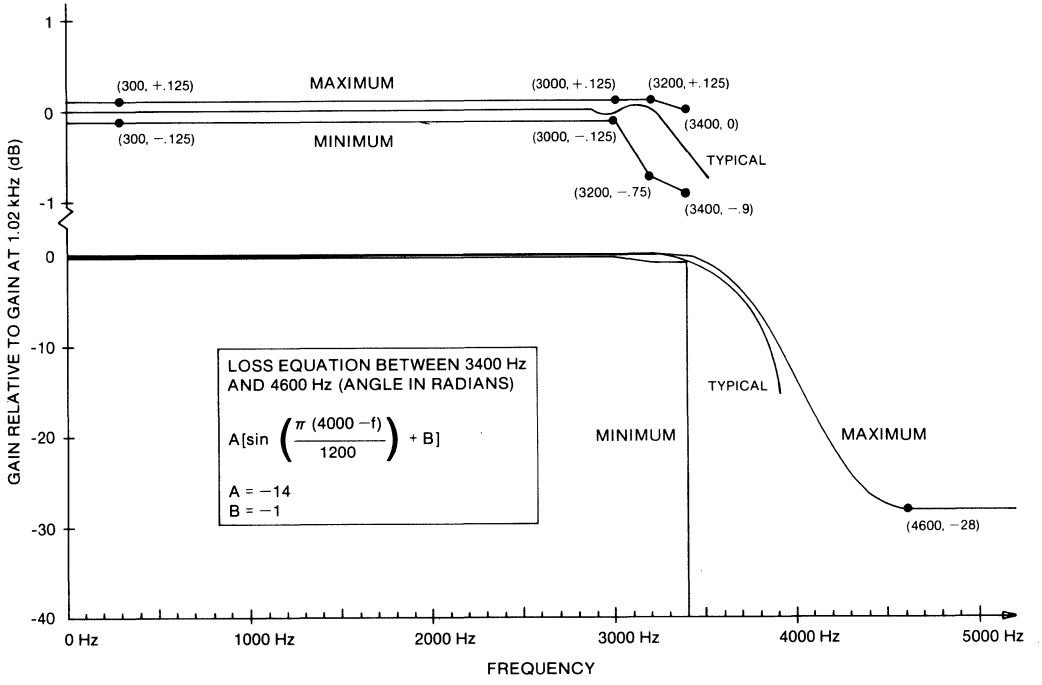


Figure 6. Receive Filter Characteristics

Transmit Filter Transfer Characteristics (Figure 7)

Table 12. Transmit Gain Relative to Gain at 1.02 kHz (GRX)*

Frequency (Hz)	Min	Typ	Max	Unit
16.67	—	–35	–30	dB
50	—	–33	–30	dB
60	—	–40	–30	dB
200	–1.8	–0.5	–0.125	dB
300 to 3000	–0.125	±0.04	0.125	dB
3140	–0.57	0.01	0.125	dB
3380	–0.885	–0.7	0.015	dB
3860	—	–9.9	–8.98	dB
4600 and above	—	—	–32	dB

* 0 dBm0 signal input at VFxIP.

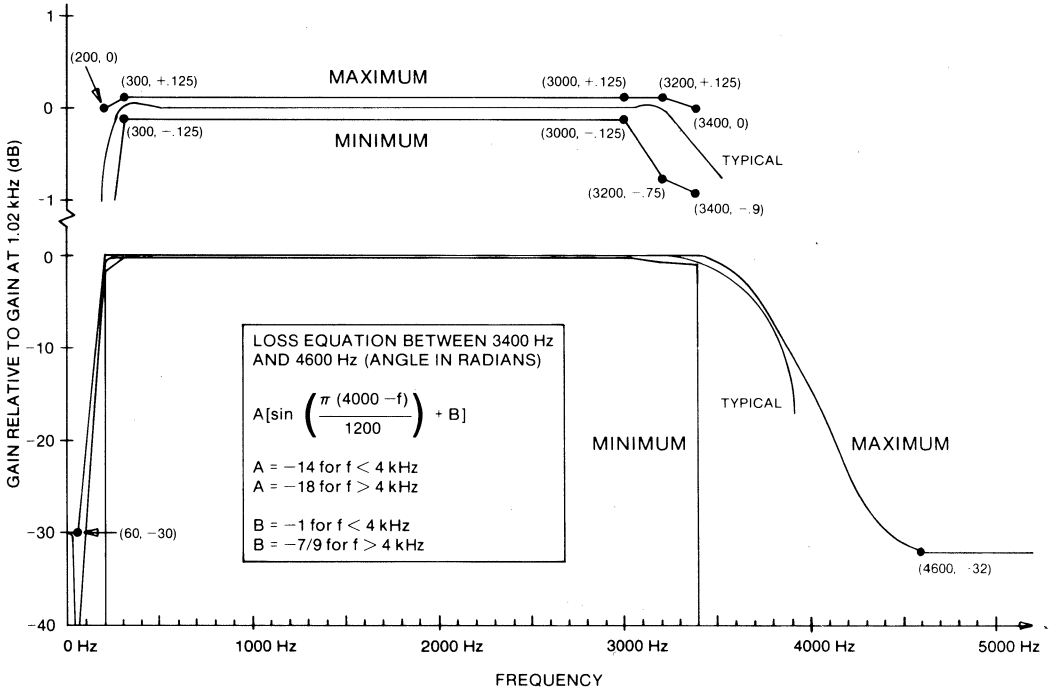


Figure 7. Transmit Filter Characteristics

Timing Characteristics

Table 13. Clock Section (Figures 8, 9, 10, and 11)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tMCHMCH	Clock period, MC	488	—	—	ns	fMC = 2.048 MHz
tMCHMCL1	Clock pulse width, MC	220	—	—	ns	—
tDCLK	Data clock pulse width	220	—	—	ns	64 kHz ≤ fDCLK ≤ 2.048 MHz
tCDC	Clock duty cycle, MC	40	50	60	%	—
tMCH1MCH2, tMCL2MCL1	Clock rise and fall time	5	—	30	ns	—

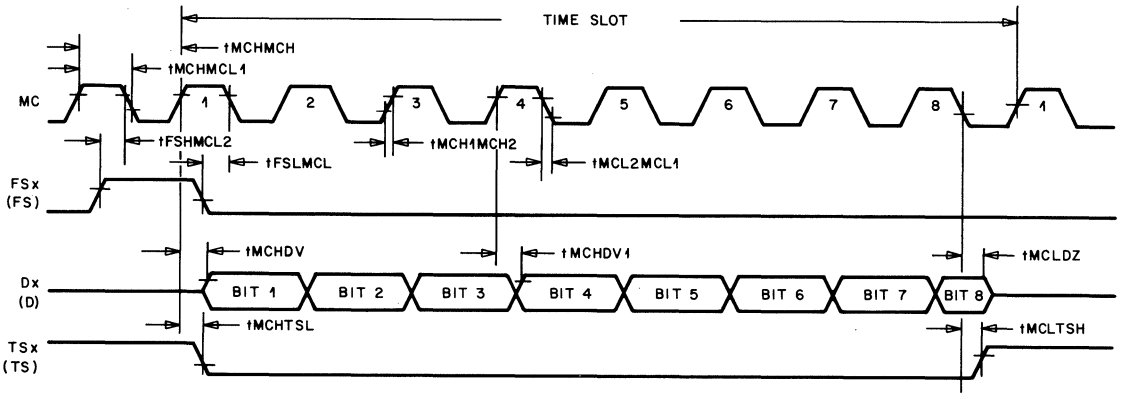
Table 14. Transmit Section, Fixed Data Rate Mode* (Figure 8)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tMCHTDV	Data enabled on TS entry	0	—	145	ns	0 < CLOAD < 250 pF
tMCHDV1	Data delay from MC	—	—	145	ns	0 < CLOAD < 250 pF
tMCLDZ	Data float on TS exit	60	—	215	ns	CLOAD = 0
tMCHTSL	Time-slot X to enable	0	—	145	ns	0 < CLOAD < 250 pF
tMCLTSH	Time-slot X to disable	60	—	215	ns	CLOAD = 0
tFSHMCL2	Frame sync delay	100	—	tMCHMCH – 100	ns	—

* Timing parameters tMCHTSV, tMCLDZ, and tMCLTSH are referenced to a high-impedance state.

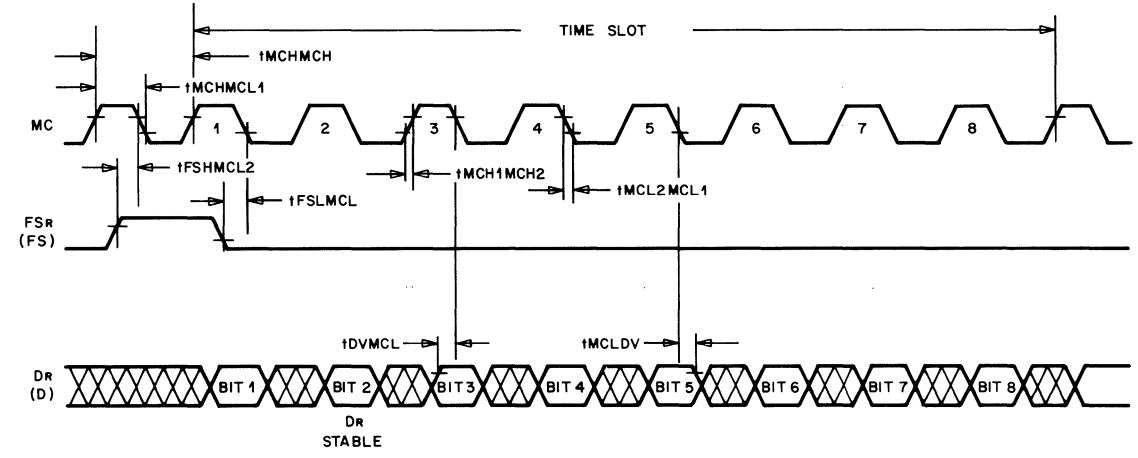
Table 15. Receive Section, Fixed Data Rate Mode (Figure 9)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tDVMCL	Receive data set-up	10	—	—	ns	—
tMCLDV	Receive data hold	60	—	—	ns	—
tFSLMCL	Frame sync delay	100	—	tMCHMCH – 100	ns	—



Note: All timing parameters referenced to VIH and VIL except tMCHTSV, tMCLTSH, tMCLDZ, which reference a high-impedance state.

Figure 8. Fixed Data Rate Transmit Timing



Note: All timing parameters referenced to VIH and VIL.

Figure 9. Fixed Data Rate Receive Timing

Table 16. Transmit Section, Variable Data Rate Mode (Figure 10)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tFSHDCL	Time-slot delay from DCLKx*	140	—	tDX – 140	ns	—
tFSHMCL	Frame sync delay	100	—	tMCHMCH – 100	ns	—
tDCHDV	Data delay from DCLKx	0	—	100	ns	0 < CLOAD < 250 pF
tFSHDV	Time slot to Dx active**	0	—	50	ns	0 < CLOAD < 250 pF
tFSLDX	Time slot to Dx inactive**	0	—	80	ns	0 < CLOAD < 250 pF
tDX	Data clock period	488	—	15620	ns	64kHz < fDCLKx < 2.048 MHz
tFSHDV1	Data delay from FSx	0	—	140	ns	—

* tFSLX minimum requirements override tFSHDCL maximum spec for 64-kHz operation.
** Timing parameters tFSHDY and tFSLDX are referenced to a high-impedance state.

Table 17. Receive Section, Variable Data Rate Mode (Figure 11)

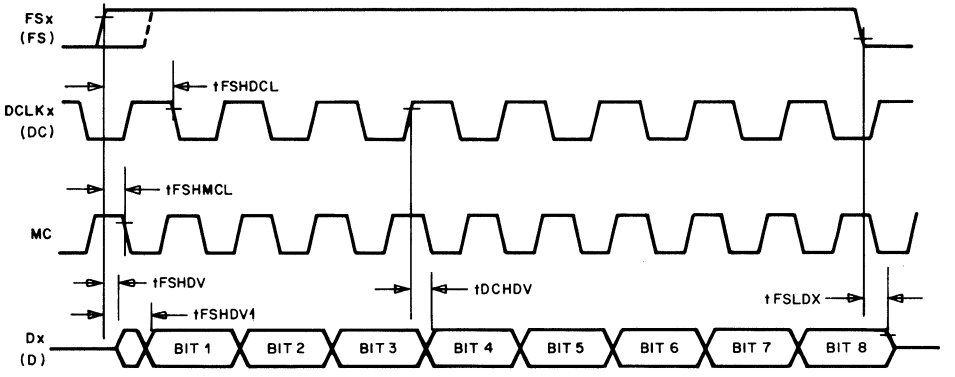
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tFSHDCL	Time-slot delay from DCLKR*	140	—	tDR – 140	ns	—
tFSHMCL	Frame sync delay	100	—	tMCHMCH – 100	ns	—
tDVDCL	Data set-up time	10	—	—	ns	—
tDCLDX	Data hold time	60	—	—	ns	—
tDR	Data clock period	488	—	15620	ns	64 kHz < fDCLKx < 2.048 MHz
tDCLFSL	Time-slot end receive time	60	—	—	ns	—

* tFSLR minimum requirements override tFSHDCL maximum spec for 64-kHz operation.

Table 18. 64-kHz Operation, Variable Data Rate Mode

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
tFSLX*	Transmit frame sync minimum downtime	488	—	—	ns	FSx is TTL-high for remainder of frame
tFSLR**	Receive frame sync minimum downtime	1952	—	—	ns	FSR is TTL-high for remainder of frame
tDCLK	Data clock pulse width	—	—	10	μs	—

* tFSLX minimum requirements override tFSHDCL maximum spec for 64-kHz operation.
** tFSLR minimum requirements override tFSHDCL maximum spec for 64-kHz operation.



Note: All timing parameters referenced to V_{IH} and V_{IL} except tFSHDAV and tFSLDX, which reference a high-impedance state.

Figure 10. Variable Data Rate Transmit Timing

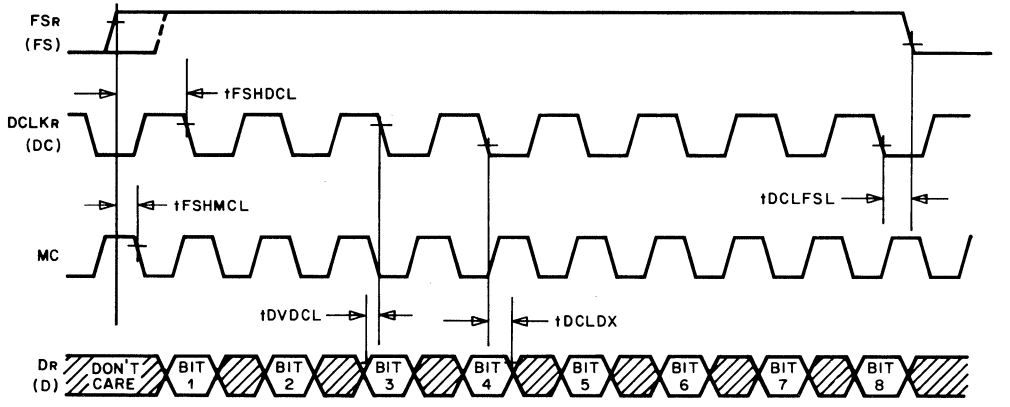
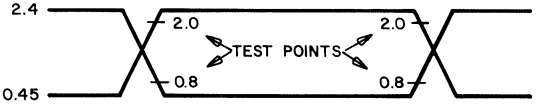


Figure 11. Variable Data Rate Receive Timing



Note: AC testing – Inputs are driven at 2.4 V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at 2.0 V for a logic 1 and 0.8 V for a logic 0.

Figure 12. AC Testing Input/Output Waveform

T7520 High-Precision PCM Codec with Filters

Features

- Encoder and decoder with on-chip filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 120-mW nominal power
- Independent transmit and receive power-down
- Easy interface to a DSP device
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- 16-bit PCM in 2's complement binary data format (LSB first)
- Gain selection – transmit: 0 or –3 dB
  receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved PSRR

Description

The T7520 High-Precision PCM Codec with Filters integrated circuit performs A/D and D/A conversion with 15-bit resolution and 10-bit linearity. The device provides on-chip anti-aliasing and reconstruction filters and a precision voltage reference. The device is designed for use in signal processing applications that require PCM data with a higher resolution than that of PCM μ-law data. The T7520 Codec is a linear device with 16-bit PCM I/O data in 2's complement binary format. Typical applications include the use of this codec with echo cancelers, digital signal processors, and in data sets. The T7520 Codec is manufactured using CMOS technology and is available in a 24-pin hermetic ceramic DIP.

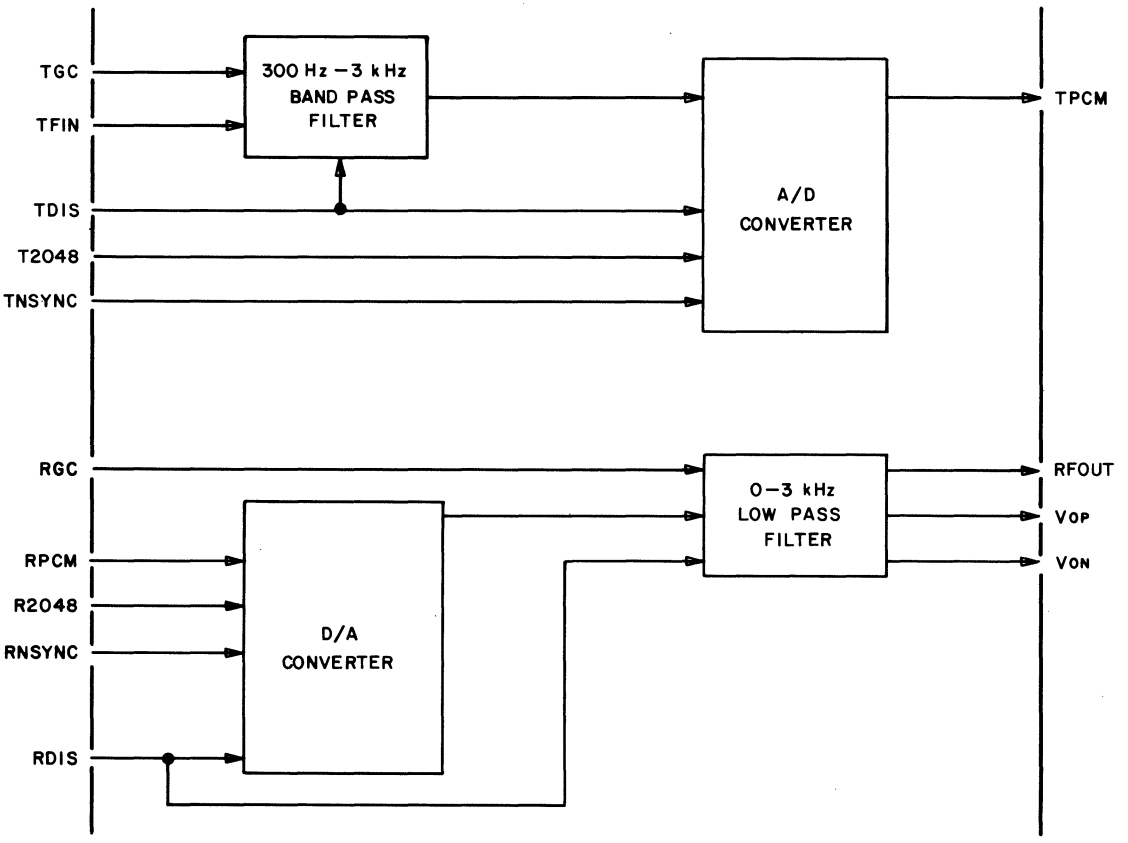
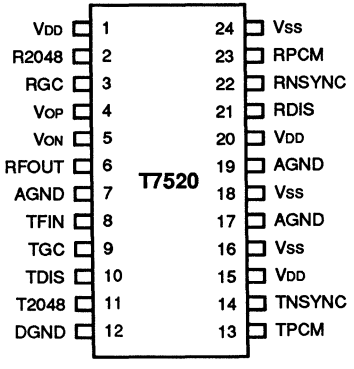


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
AGND	7, 17, 19	TFIN	8
DGND	12	TGC	9
RDIS	21	TNSYNC	14
RFOUT	6	TPCM	13
RGC	3	T2048	11
RNSYNC	22	VDD	1, 15, 20
RPCM	23	VON	5
R2048	2	VOP	4
TDIS	10	VSS	16, 18, 24

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Symbol	Type	Name/Function
V_{DD}	—	**+5 V Supply (± 5%).**
R2048	I	**Receive Clock.** 2.048 MHz.
RGC	I	**Receive Gain Control.** A high on the pin sets the receive gain to +3 dB; a low or no connection sets the gain to 0 dB.
V_{OP}	O	**Positive Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
V_{ON}	O	**Negative Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
RFOUT	O	**Receive Filter Output.** A 16-bit digital milliwatt sequence reconstructed by the filter produces a 1.547 Vp signal (when RGC = 1). The load resistance must be greater than 20 kΩ in parallel with less than 50 pF.
AGND	—	**Ground (Analog).**
TFIN	I	**Transmit Voice Frequency.** For best results, TFIN should be driven from a low-impedance source.
TGC	I	**Transmit Gain Control.** A high on this pin sets the transmit gain to –3 dB; a low or no connection sets the gain to 0 dB.
TDIS	I	**Transmit Disable.** A high on this pin disables the transmit side; a low or no connection enables the transmit side.
T2048	I	**Transmit Clock.** 2.048 MHz.
DGND	—	**Ground (Digital).**
TPCM	O	**Transmit PCM.** This pin is used for the A/D 16-bit 2's complement binary PCM (LSB first) output. This pin is 3-stated when inactive.
TNSYNC	I	**Transmit Synchronization.** An accurate timing pulse (negative going edge trigger) used to start the transmission of the 16 bits of data out of the TPCM. The pulse should be low for at least one transmit data clock period after timing edge A (see Figure 14).
V_{SS}	—	**–5 V Supply (± 5%).**
RDIS	I	**Receive Disable.** A high on this pin disables the receive side; a low or no connection enables the receive side.
RNSYNC	I	**Receive Synchronization.** An accurate timing pulse (negative going edge trigger) is used to start the reading of the 16 bits of data into the RPCM. The pulse should remain low for at least one receive data clock period after timing edge A (see Figure 14).
RPCM	I	**Receive PCM.** This pin is used for the D/A 16-bit PCM 2's complement binary (LSB first) input.
NC	—	**No Connection.**

CAUTION: Cavity cover is internally connected to AGND.

Application Hints

The T7520 High-Precision PCM Codec is a high-performance subsystem. The conditions necessary to achieve reliable codec performance are outlined below.

Supply Routing (See Figure 3)

All the V_{DD} pins must to tied together to avoid excessive substrate currents in the chip.

All the V_{SS} pins must be tied together.

All the analog pins (AGND) must be tied together.

Supply Decoupling

The codec is a sampled data system. As such, noise on the supply lines near multiples of the 8-kHz sample rate are aliased into the codec passband (300 Hz to 3 kHz). For full dynamic range, the noise at the codec pins must be kept below 1 mVrms and 100 mVp (especially those noise components over 100 kHz).

The dominant noise source in many systems is the switching power supply, which typically has significant noise energy extending up into the MHz range. The power busing from the supply to the codec (in a well-designed ground plane system) has an impedance lower than that of most bypass capacitors. Therefore, simply adding bypass capacitors across the codec supply lines does not reduce the power supply noise that feeds into the codec. To keep the noise out of the codec, the codec must be isolated (decoupled) from the noise. The proper decoupling scheme is shown in Figure 3. The 3-Ω to 5-Ω decoupling resistors in series with V_{DD} and V_{SS} with the 10-μF tantalum or low ESR aluminum capacitor form a low-pass filter (–3 dB at a frequency of about 5 kHz). The 0.2-μF ceramic capacitors (located as close to the indicated pins as possible) bypass the high-frequency noise and codec-generated noise.

Fully Synchronous Operation

The transmit and receive paths can be run from separate clocks (Figure 4a), but doing so increases the codec noise floor and can result in various clicks, pops, and squeals in the voice band as separate clocks slide past each other in phase. Do not configure clocks in the manner shown in Figure 4a.

It is strongly recommended that the transmit (T2048) and receive (R2048) master clock lines be tied together, as shown in Figure 4b. The TNSYNC and RNSYNC lines need not be tied together, but it is critical that their sync frequencies be exactly 1/256 of the master clock. The sync clocks must also be locked in phase so that the TNSYNC and T2048 clock edges line up and the RNSYNC and R2048 clock edges line up. This relationship is shown in Figure 4b by the logic blocks run off the master clock, which drives the codec sync inputs. The timing can be generated by software (in a DSP device, for example), but the sync timing must stay solid with respect to the master clock.

The best noise performance is achieved by using the fully synchronous timing shown in Figure 4c. The transmit and receive paths use the same master and sync clocks, and the sync is directly derived from the master clock.

I/O Routing

This codec has a dynamic range of over 80 dB. The routing of the analog input (TFIN) and outputs (RFOUT, V_{OP}, and V_{ON}) must be kept away from noise sources, especially signal-dependent digital lines.

To help reduce coupling into the transmit path, TFIN should be driven from a low-impedance source.

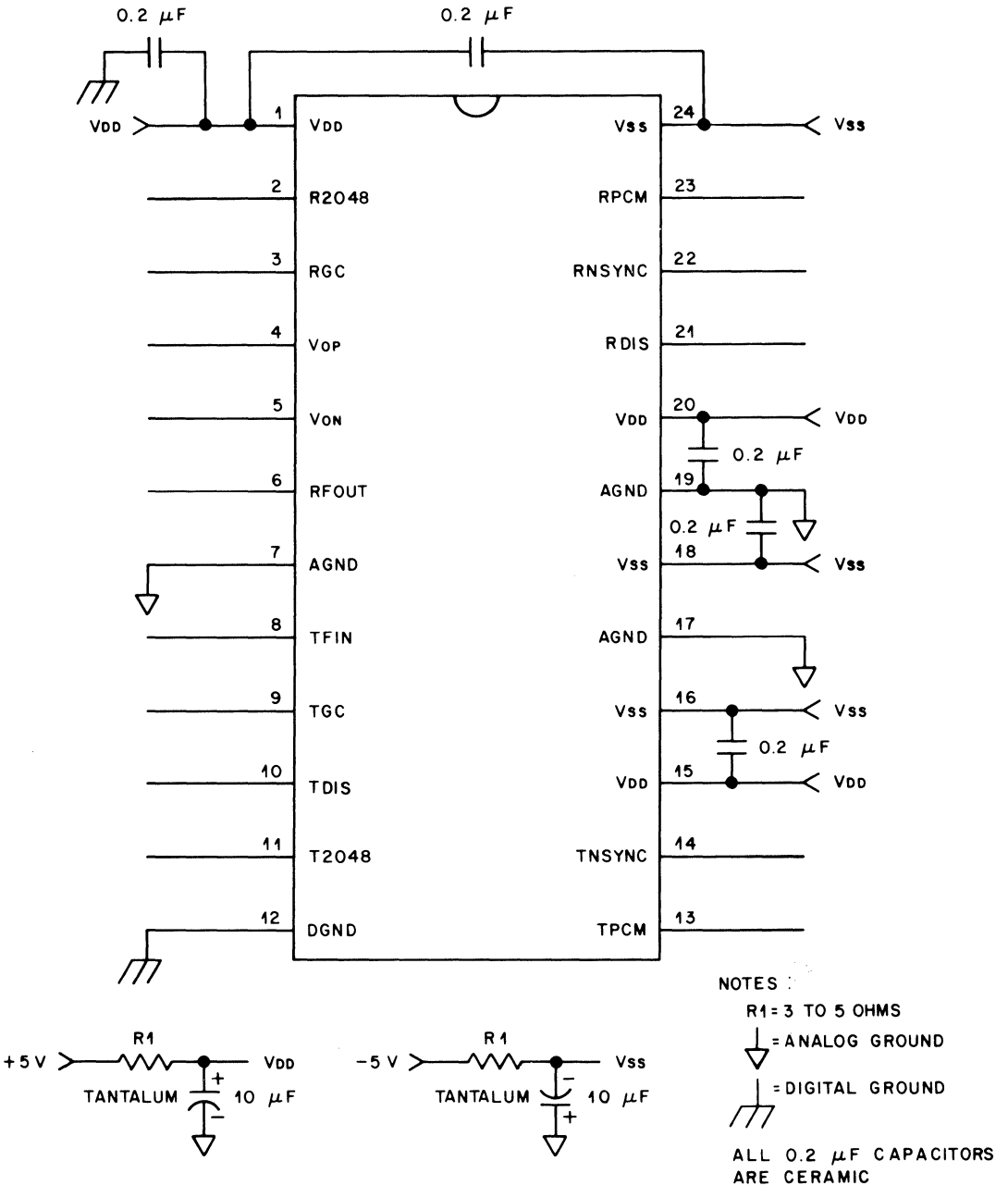
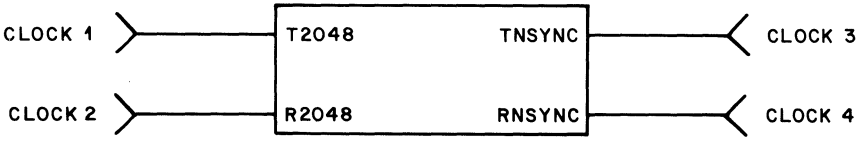
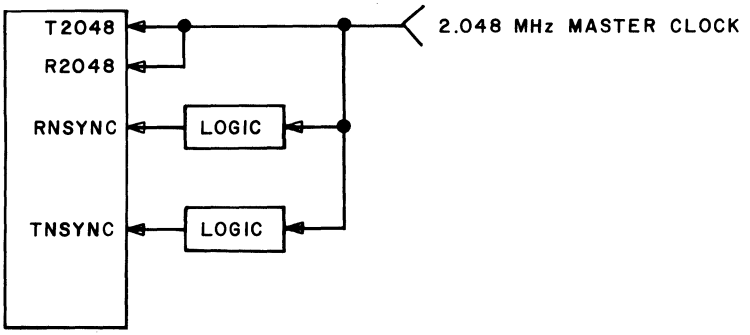


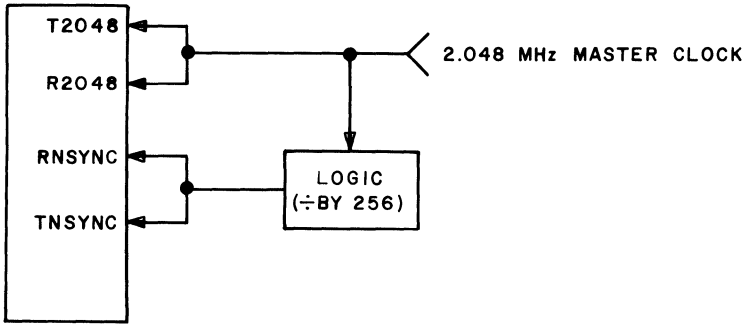
Figure 3. Codec Supply Decoupling



a. Not Recommended (Do Not Do This)



b. Acceptable Chip TIming (Better, but Not Optimum)



c. Recommended Chip Timing (Optimum)

Figure 4. Chip Timing Schemes

Characteristics

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = –5 V ± 5%

Parameter	Limits			Unit
	Min	Typ	Max	
Power disspation:				
active, DIS = 0	50	120	200	mW
inactive, DIS = 1	—	15	40	mW
Analog overload at 1 kHz				
TGC = RGC = 1	±2.191	2.229	±2.268	Vp
Absolute gain (gain contrast) at 1.02 kHz,				
full-scale – 3dB, TGC = RGC = 0	–0.15	—	0.15	dB
Gain tracking (transmit or receive) at 1.02 kHz,				
full-scale = 0 dB, –3 dB reference:				
0 dB to –40 dB	—	—	±0.2	dB
–40 dB to –53 dB	—	—	±0.4	dB
Signal-to-distortion (transmit or receive) at				
1.02 kHz, full-scale = 0dB:				
0 dB to –25 dB	60	—	—	dB
–40 dB	45	—	—	dB
–45 dB	40	—	—	dB
Transmit idle channel noise				
TGC 1 = 1 or 0	—	9	13	dBrnC
Receive idle channel noise:				
RGC = 1	—	6	9	dBrnC
RGC = 0	—	3	6	dBrnC
Power supply rejection (end-to-end):				
1 kHz	35	—	—	dB
0-kHz to 100-kHz white noise	30	—	—	dBC
Absolute delay (end-to-end) at 1 kHz	—	—	575	μs

Note: 0 dBm = 90 dB = 0.775 Vrms (into 600 Ω).

Analog Interface

TFIN: Rin > 35 kΩ and Cin < 10 pF
RFOUT: ac impedance < 300 Ω, maximum current 150 μA

Any input can be between V_{SS} and V_{DD} without damaging the chip.

Digital Interface

All inputs: TTL-compatible, Iin < 15 μA, < 5-pF loading
TPCM: Capable of driving a 50-pF capacitance to TTL voltage levels at 2.048 Mb/s

Any input can be between V_{SS} and V_{DD} without damaging the chip.

Table 2. Overload (1.00 kHz) Compression

Input/Overload Level (dB)	Maximum Increased Loss (dB) Relative to Overload –3 dB
0	0.2
3	1.8
6	4.6

Note: The filter responses scale linearly with master clock.

In the following tables and associated figures, the ac characteristics assume that the master clock (T2048, R2048) is 2.048 MHz ± 100 ppm.

Table 3. Frequency Response*

Freq (Hz)	Transmit Loss (dB)	Receive Loss (dB)
50—60	≥ 20	±0.2
200	0.1 to 1.8	–0.05 to +0.2
300—3000	±0.125	±0.125
3200	–0.125 to +0.75	–0.125 to +0.75
3400	0.2 to 0.9	0.2 to 0.9
4000	>14	>14
4600 and above	>32	>28
3400—4600	$> 14 \left[\sin \left(\frac{\pi (4000 - f)}{1200} \right) - 1 \right]$	$> 14 \left[\sin \left(\frac{\pi (4000 - f)}{1200} \right) - 1 \right]$
4000—4600	$> 18 \left[\sin \left(\frac{\pi (4000 - f)}{1200} \right) - \frac{7}{9} \right]$	

* See Figures 5 through 9 for response curves.

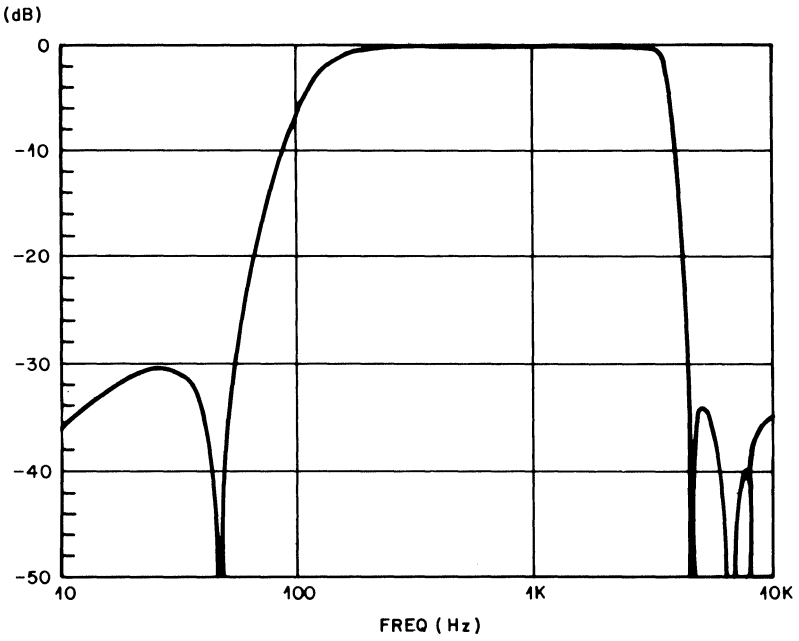


Figure 5. Transmit Path Frequency Response

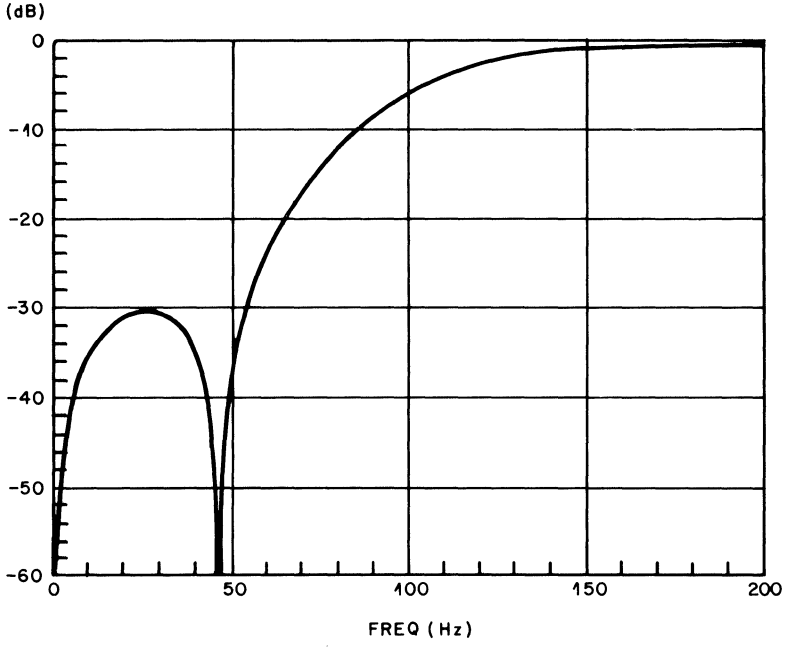


Figure 6. Transmit Path Low Frequency Response

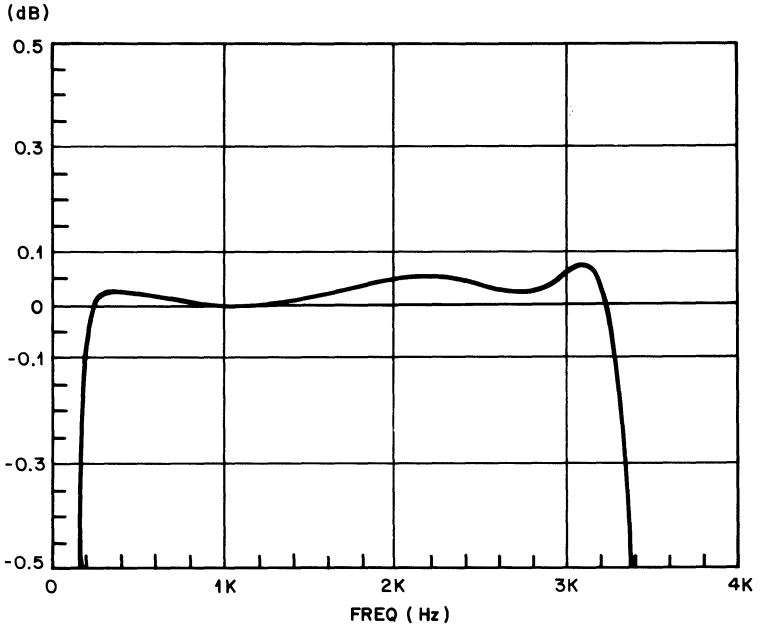


Figure 7. Transmit Path Voice Band Response

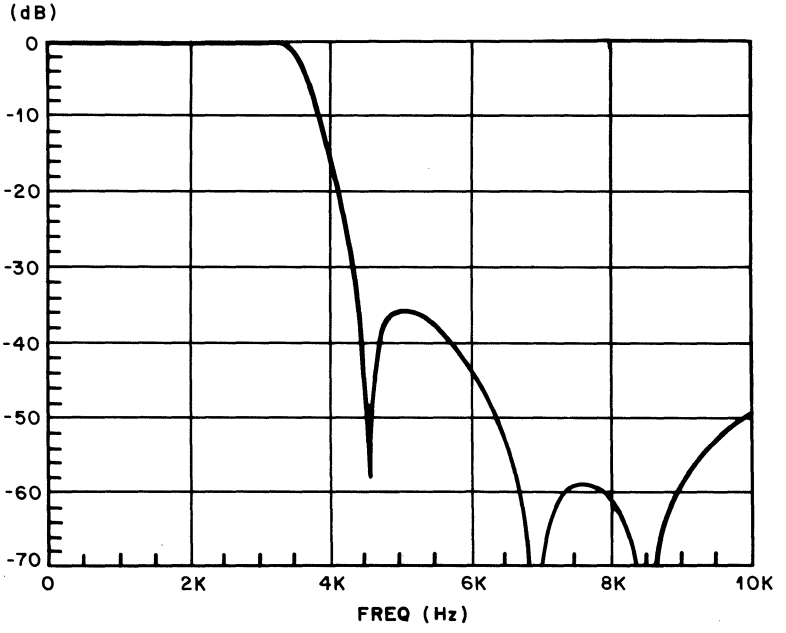


Figure 8. Receive Path Frequency Response

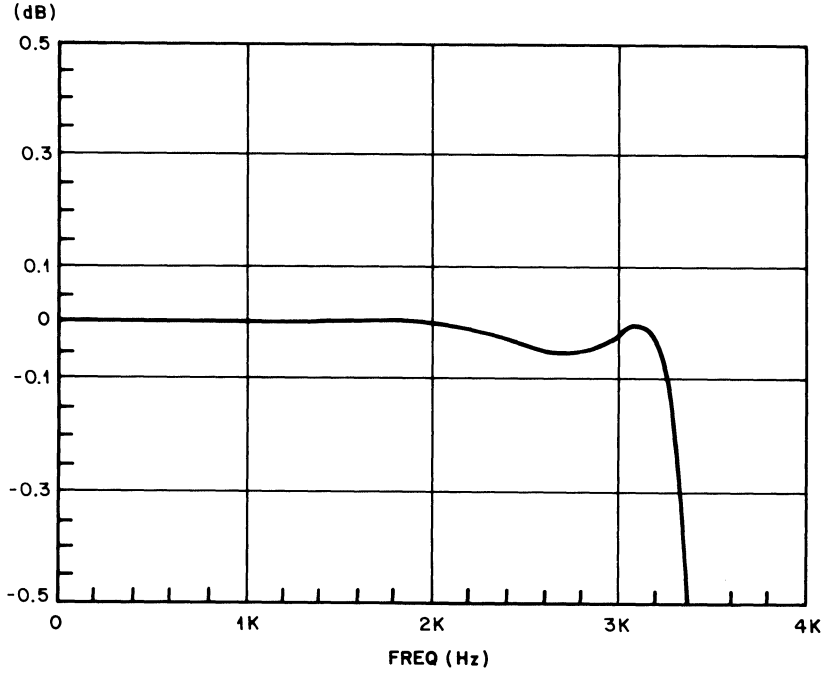


Figure 9. Receive Path Voice Band Response

Table 4. Phase and Delay Distortion (End-to-End)*

Freq (Hz)	Phase Deviation from Linearity (Radians)	Delay Distortion (μs, max)
Below 500	$-4.17 + 0.0046f \leq PD \leq 4.17 - 0.0046f$	—
500—700		300
700—2000	Between semicircles of radius 0.92 radians (1150 Hz) centered at $\pm$ 0.95 radians and 1850 Hz	75
2000—2500		150
2500—2700		200
2700—3000		375
3000 and above	$-11.65 + 0.0042f \leq PD \leq 11.65 - 0.0042f$	—

* See Figures 10, 11, and 12 for group delay curves.

Intrachannel Crosstalk (200 Hz to 3400 Hz) < –71 dB

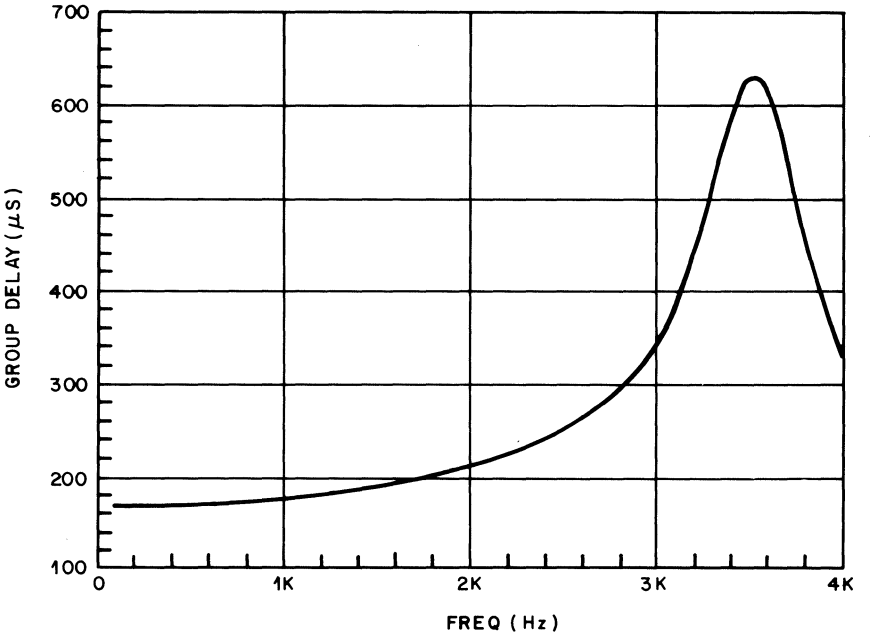


Figure 10. Receive Path Group Delay Response

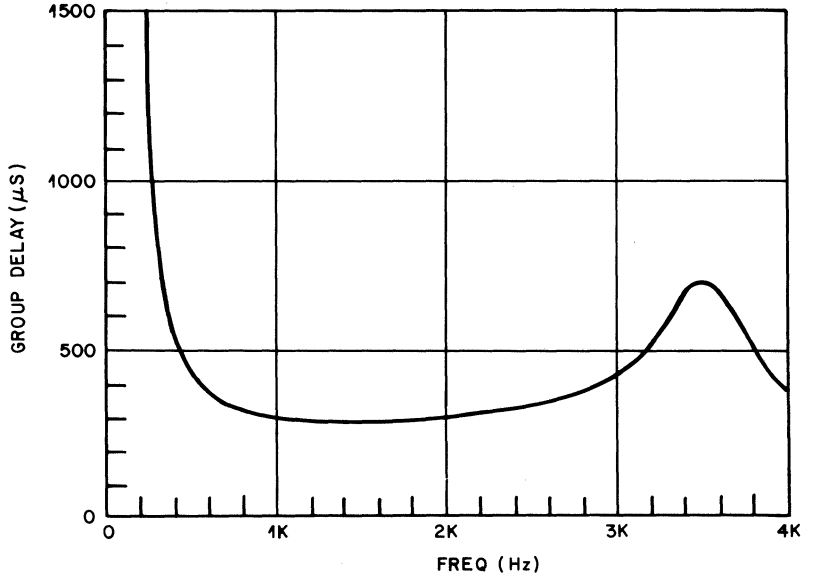


Figure 11. Transmit Path Group Delay Response

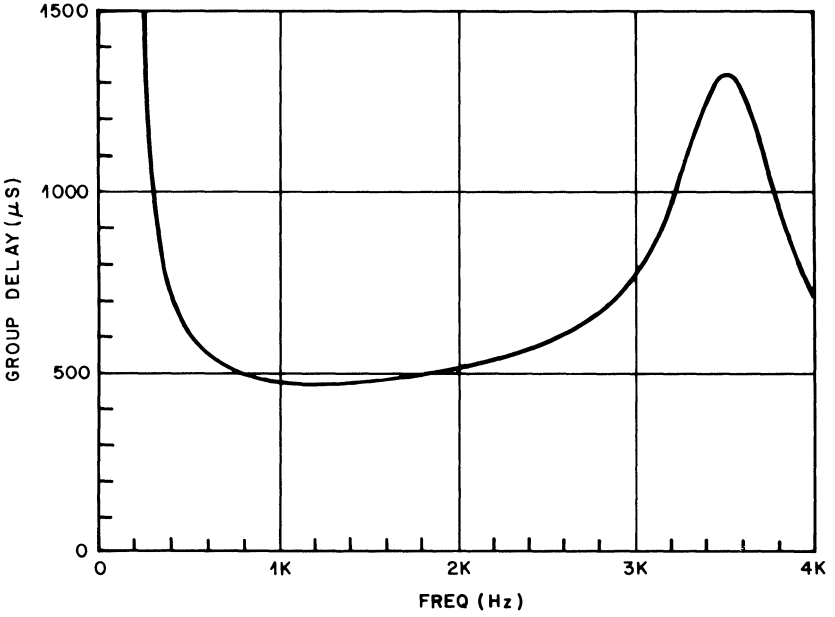


Figure 12. End-to-End Group Delay

Table 5. Single Frequency Distortion*

Input/ Max Input (dB)	Input Frequency (Hz)	S/(N+D) (In the 0-kHz to 4-kHz Band) (dB)
0	200 to 3400	60
–10		60
–20		60
–30		55
–40		45

* See Figure 13 for S/(N + D) curve.

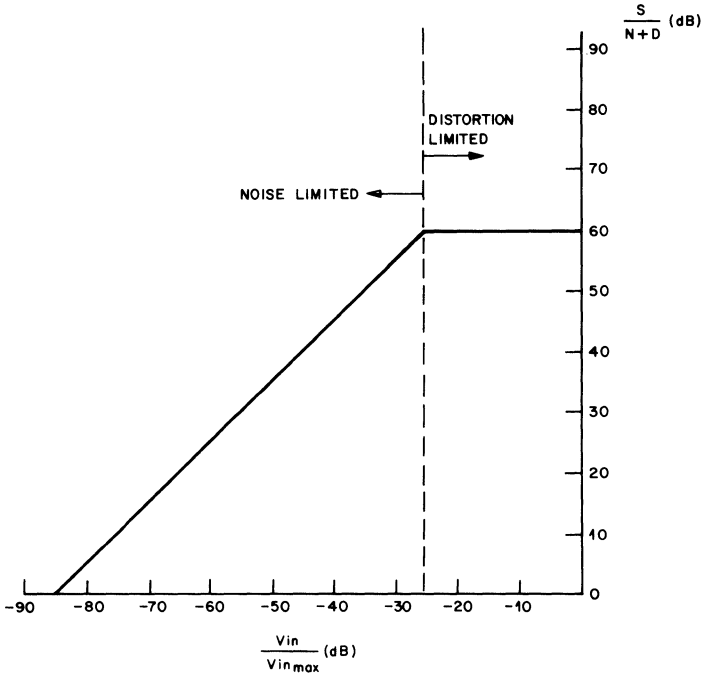


Figure 13. Signal-to-Impairment Characteristic of the Transmit and Receive Paths

Table 6. Intermodulation Distortion (4-Tone Method; Input = –13 dBm0)

r2 < 60 dB below input r3 < 60 dB below input

Transmit (Encoder)	Gain	Input Voltage at 1 kHz Corresponding to: Digital mW Out of TPCM	Overload (+3.174 dBm0)	Unit
TGC = 0	0 dB	1.095	1.578	Vp
TGC = 1	–3.00 dB	1.547	2.229	Vp

Receive (Decoder)	Gain	Output Voltage at 1 kHz Corresponding to: Digital mW Into RPCM	Overload (+3.174 dBm0)	Unit
RGC = 1	–3.00 dB	1.547	2.229	Vp
RGC = 0	0 dB	1.095	1.578	Vp

Timing Characteristics

The timing requirements are shown in Figure 14, with expanded details in Figure 15. The duty cycle of T2048 and R2048 must be between 45% and 55%. The encoder and decoder can operate back-to-back if RNSYNC = TNSYNC and R2048 = T2048.

Symbol	Parameter	Capacitance	Min	Max	Unit
tCKLSYL	Synchronization delay	—	10	tCLK – 75	ns
tCKLSYH	Synchronization hold	—	0*	*	ns
tCKHTPV	Transmit prop delay	50 pF	0	140	ns
tRSVCKL	Receive set-up time	—	50	—	ns
tCKLRSX	Receive hold time	—	0	—	ns

* Each synchronization pulse should be low for a minimum of 1 clock cycle after timing edge A, with a maximum of 50% duty cycle. Note that the internal operation of the encoder or decoder is initiated by the first data clock edge that goes negative (timing edge A in Figure 14) after TNSYNC or RNSYNC has gone low.

Timing Diagrams

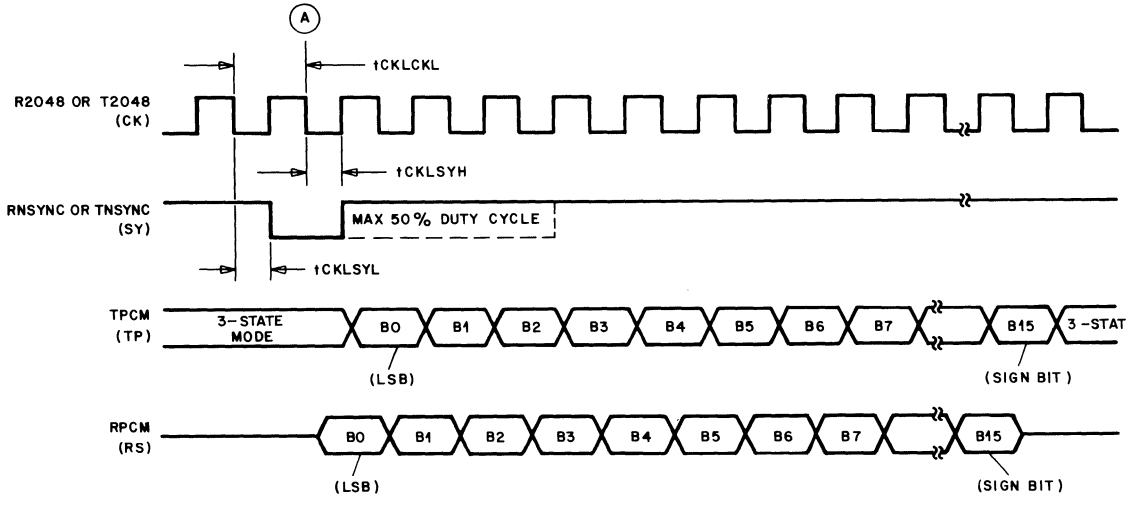


Figure 14. I/O Timing

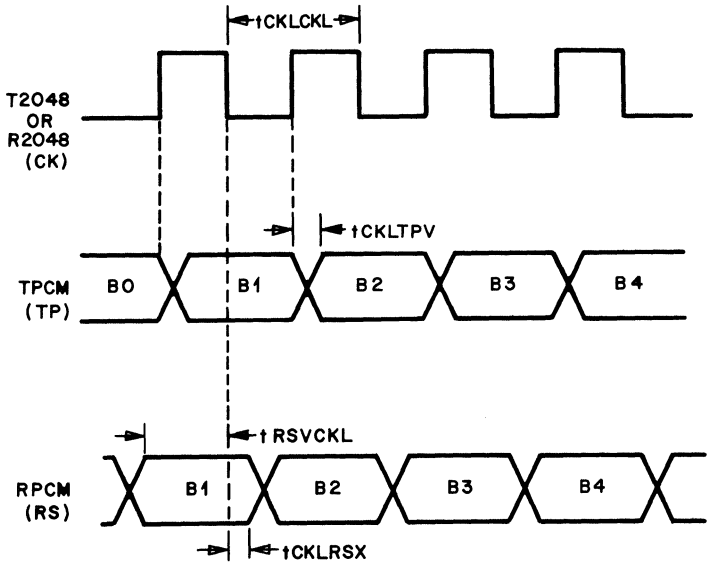


Figure 15. I/O Timing (Enlarged Section)

T7521 High-Precision PCM Codec without Filters

Features

- A/D and D/A with on-chip D/A filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 100-mW nominal power
- Independent transmit and receive power-down
- Easy interface to a DSP device
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- 16-bit PCM in 2's complement binary data format (LSB first)
- Gain selection – receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved PSRR

Description

The T7521 High-Precision PCM Codec without Filters integrated circuit performs A/D and D/A conversion with 15-bit resolution and 10-bit linearity. The device provides an on-chip reconstruction filter and a precision voltage reference. The device is designed for use in signal processing applications that require PCM data with a higher resolution than that of PCM μ-law data. The T7521 Codec is a linear device with 16-bit PCM I/O data in 2's complement binary format. Typical applications include the use of this codec with echo cancelers, digital signal processors, and in data sets. An optional transmit filter for this device can be supplied by the user. The T7521 Codec is manufactured using CMOS technology and is available in a 24-pin hermetic ceramic DIP.

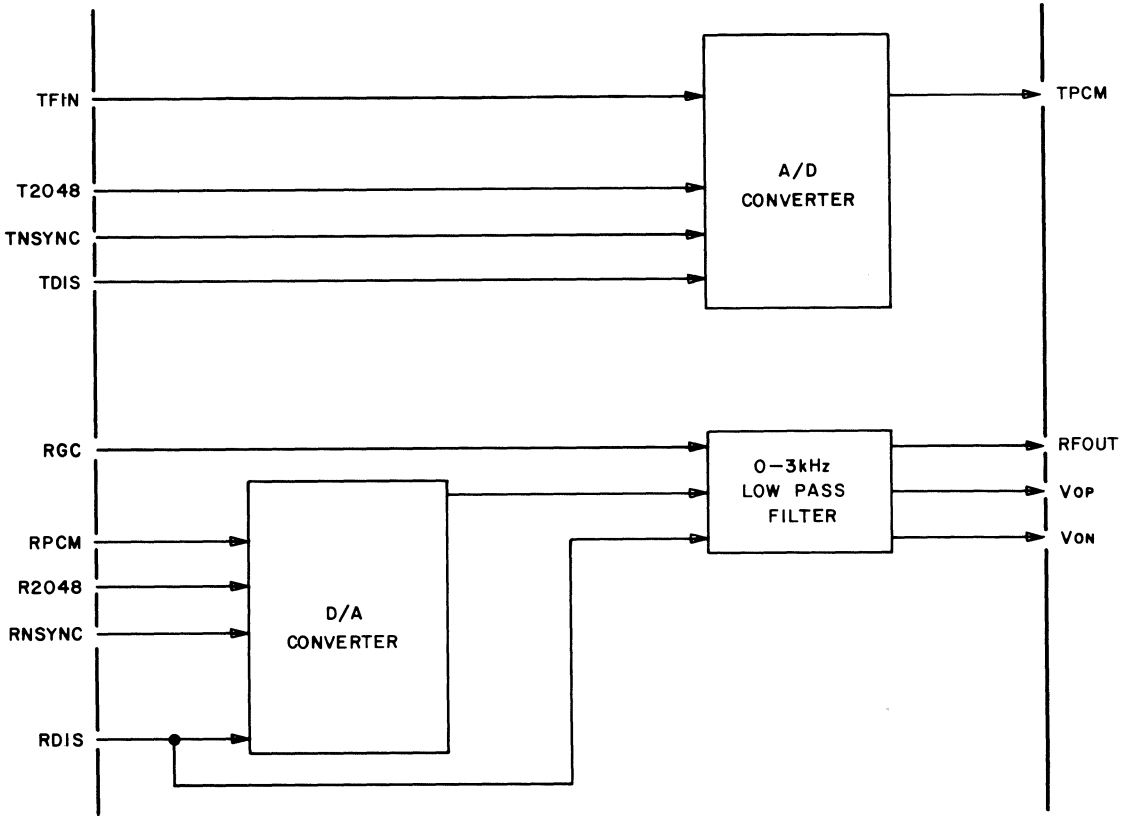
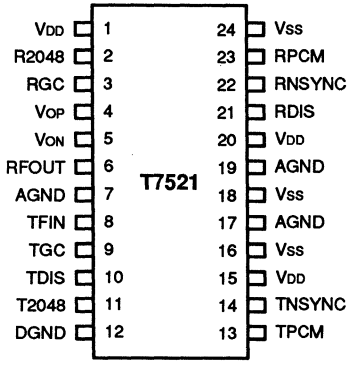


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
AGND	7, 17, 19	TFIN	8
DGND	12	TGC	9
RDIS	21	TNSYNC	14
RFOUT	6	TPCM	13
RGC	3	T2048	11
RNSYNC	22	VDD	1, 15, 20
RPCM	23	VON	5
R2048	2	VOP	4
TDIS	10	VSS	16, 18, 24

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Symbol	Type	Name/Function
VDD	—	**+5 V Supply (± 5%).**
R2048	I	**Receive Clock.** 2.048 MHz.
RGC	I	**Receive Gain Control.** A high on the pin sets the receive gain to +3 dB; a low or no connection sets the gain to 0 dB.
VOP	O	**Positive Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
VON	O	**Negative Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
RFOUT	O	**Receive Filter Output.** A 16-bit digital milliwatt sequence reconstructed by the filter produces a 1.547 Vp signal (when RGC = 1). The load resistance must be greater than 20 kΩ in parallel with less than 50 pF.
AGND	—	**Ground (Analog).**
TFIN	I	**Transmit Voice Frequency.** For best results, TFIN should be driven from a low-impedance source.
TGC	I	**Transmit Gain Control.** Option not used on this chip. Leave the TGC pin unconnected; do not use this pin as a signal tie point.
TDIS	I	**Transmit Disable.** A high on this pin disables the transmit side; a low or no connection enables the transmit side.
T2048	I	**Transmit Clock.** 2.048 MHz.
DGND	—	**Ground (Digital).**
TPCM	O	**Transmit PCM.** This pin is used for the A/D 16-bit 2's complement binary PCM (LSB first) output. This pin is 3-stated when inactive.
TNSYNC	I	**Transmit Synchronization.** An accurate timing pulse (negative going edge trigger) used to start the transmission of the 16 bits of data out of the TPCM. The pulse should be low for at least one transmit data clock period after timing edge A (see Figure 9).
VSS	—	**–5 V Supply (± 5%).**
RDIS	I	**Receive Disable.** A high on this pin disables the receive side; a low or no connection enables the receive side.
RNSYNC	I	**Receive Synchronization.** An accurate timing pulse (negative going edge trigger) is used to start the reading of the 16 bits of data into the RPCM. The pulse should remain low for at least one receive data clock period after timing edge A (see Figure 9).
RPCM	I	**Receive PCM.** This pin is used for the D/A 16-bit PCM 2's complement binary (LSB first) input.
NC	—	**No Connection.**

CAUTION: Cavity cover is internally connected to AGND.

Application Hints

The T7521 High-Precision PCM Codec is a high-performance subsystem. The conditions necessary to achieve reliable codec performance are outlined below.

Supply Routing (See Figure 3)

All the V_{DD} pins must be tied together to avoid excessive substrate currents in the chip.

All the V_{SS} pins must be tied together.

All the analog ground pins (AGND) must be tied together.

Supply Decoupling

The codec is a sampled data system. As such, noise on the supply lines near multiples of the 8-kHz sample rate are aliased into the codec passband (300 Hz to 3 kHz). For full dynamic range, the noise at the codec pins must be kept below 1 mVrms and 100 mVp (especially those noise components over 100 kHz).

The dominant noise source in many systems is the switching power supply, which typically has significant noise energy extending up into the MHz range. The power busing from the supply to the codec (in a well-designed ground plane system) has an impedance lower than that of most bypass capacitors. Therefore, simply adding bypass capacitors across the codec supply lines does not reduce the power supply noise that feeds into the codec. To keep the noise out of the codec, the codec must be isolated (decoupled) from the noise. The proper decoupling scheme is shown in Figure 3. The 3- to 5-Ω decoupling resistors in series with V_{DD} and V_{SS} with the 10-μF tantalum or low ESR aluminum capacitor form a low-pass filter (–3 dB at a frequency of about 5 kHz). The 0.2-μF ceramic capacitors (located as close to the indicated pins as possible) bypass the high-frequency noise and codec-generated noise.

Fully Synchronous Operation

The transmit and receive paths can be run from separate clocks (Figure 4a), but doing so increases the codec noise floor and can result in various clicks, pops, and squeals in the voice band as separate clocks slide past each other in phase. Do not configure clocks in the manner shown in Figure 4a.

It is strongly recommended that the transmit (T2048) and receive (R2048) master clock lines be tied together, as shown in Figure 4b. The TNSYNC and RNSYNC lines need not be tied together, but it is critical that their sync frequencies be exactly 1/256 of the master clock. The sync clocks must also be locked in phase so that the TNSYNC and T2048 clock edges line up and the RNSYNC and R2048 clock edges line up. This relationship is shown in Figure 4b by the logic blocks run off the master clock, which drives the codec sync inputs. The timing can be generated by software (in a DSP device, for example), but the sync timing must stay solid with respect to the master clock.

The best noise performance is achieved by using the fully synchronous timing shown in Figure 4c. The transmit and receive paths use the same master and sync clocks, and the sync is directly derived from the master clock.

I/O Routing

This codec has a dynamic range of over 80 dB. The routing of the analog input (TFIN) and outputs (RFOUT, V_{OP}, and V_{ON}) must be kept away from noise sources, especially signal-dependent digital lines.

To help reduce coupling into the transmit path, TFIN should be driven from a low-impedance source.

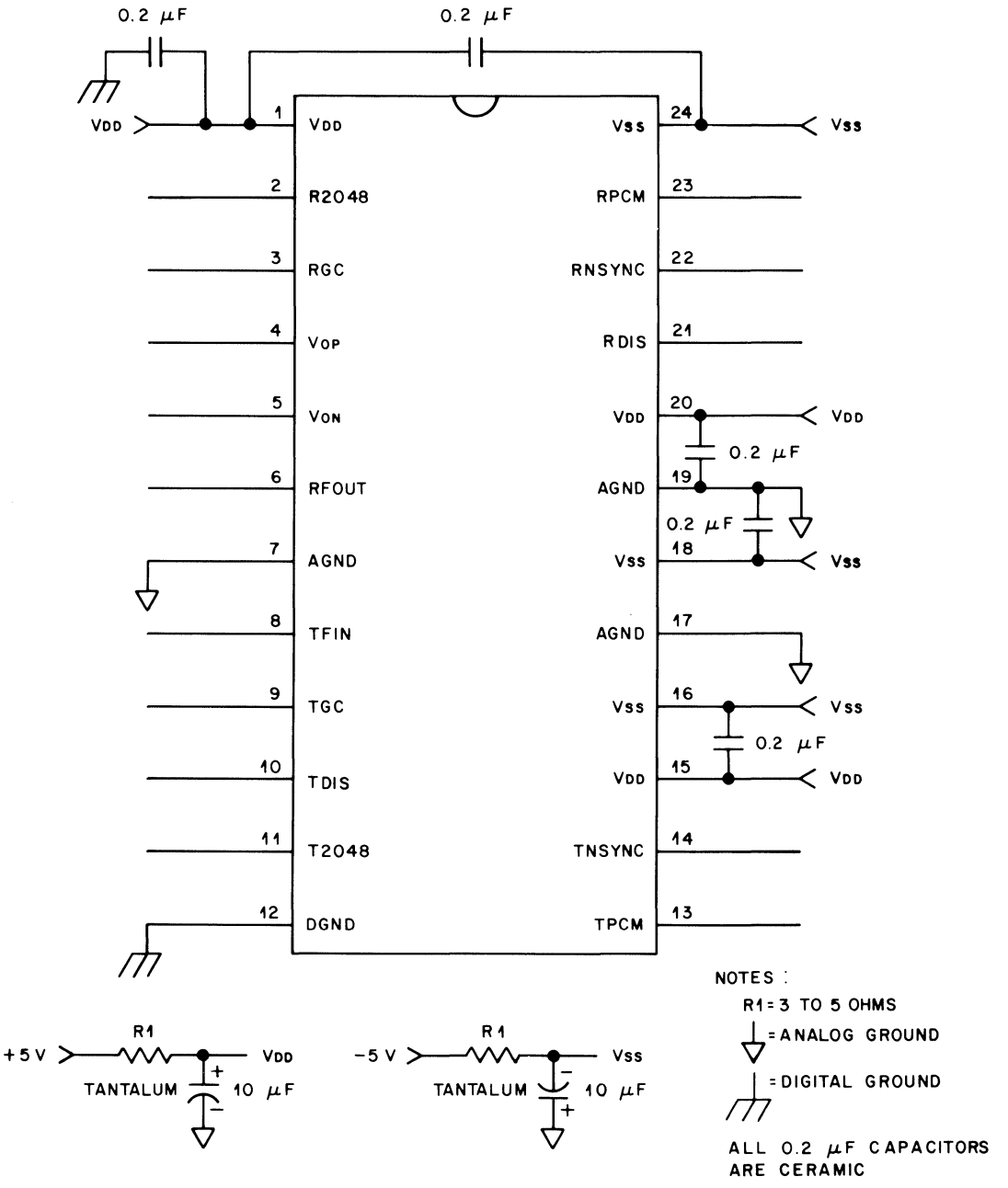
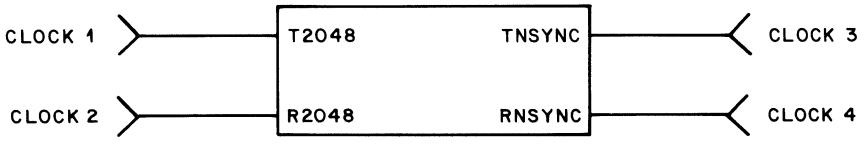
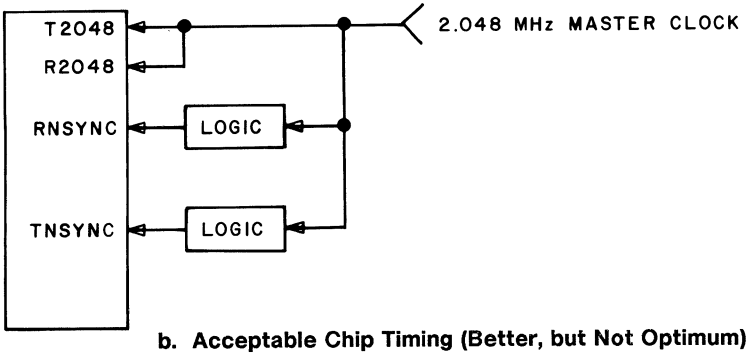


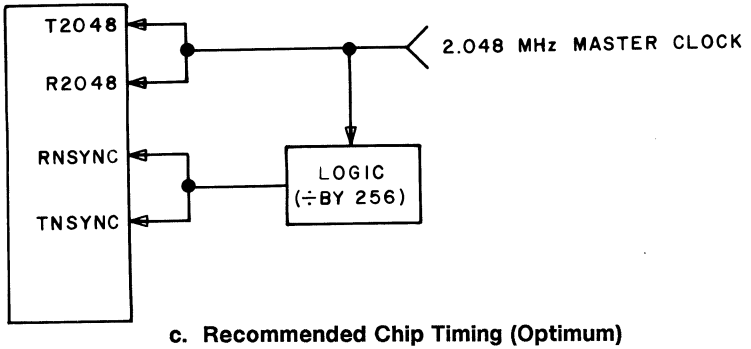
Figure 3. Codec Supply Decoupling



a. Not Recommended (Do Not Do This)



b. Acceptable Chip Timing (Better, but Not Optimum)



c. Recommended Chip Timing (Optimum)

Figure 4. Chip Timing Schemes

Miscellaneous

The TFIN pin must have a dc path to ground. If the A/D signal source is ac-coupled to the A/D, a resistor must be connected from TFIN to analog ground.

The A/D input must be driven from a fast-settling source (0.1% in 6 μs). The input impedance is 100 kΩ in parallel with 80 pF.

Characteristics

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = –5 V ± 5%

Parameter	Limits			Unit
	Min	Typ	Max	
Power disspation:				
active, TDIS = RDIS = 0	50	100	200	mW
inactive, TDIS = RDIS = 1	—	20	40	mW
Receive analog overload at 1 kHz				
RGC = 1	±2.191	±2.229	±2.268	Vp
Transmit (A/D) overload at 1 kHz	±2.70	±2.75	±2.80	Vp
Absolute gain (gain contrast) at 1.02 kHz,				
full-scale – 3 dB, RGC = 0	–0.15	—	0.15	dB
Gain tracking (transmit or receive) at 1.02 kHz,				
full-scale = 0 dB, –3 dB reference:				
0 dB to –40 dB	—	—	±0.2	dB
–40 dB to –53 dB	—	—	±0.4	dB
Signal-to-distortion at 1.02 kHz, full-scale = 0 dB:				
0 dB to –30 dB	60	—	—	dB
–40 dB	45	—	—	dB
–45 dB	40	—	—	dB
Transmit idle channel noise	—	8	14	dBrnC
Receive idle channel noise:				
RGC = 1	—	6	9	dBrnC
RGC = 0	—	3	6	dBrnC
Power supply rejection (end-to-end):				
1 kHz	35	—	—	dB
0-kHz to 100-kHz white noise	30	—	—	dBC
Absolute delay (end-to-end) at 1 kHz	—	—	575	μs

Note: 0 dBm = 90 dB = 0.775 Vrms (into 600 Ω).

Analog Interface

TFIN: Rin > 100 kΩ, Cin < 100 pF
RFOUT: ac impedance < 300 Ω, maximum current 150 μA

Any input can be between V_{SS} and V_{DD} without damaging the chip.

Digital Interface

All inputs: TTL-compatible, Iin < 15 μA, < 5-pF loading
TPCM: Capable of driving a 50-pF capacitance to TTL voltage levels at 2.048 Mb/s

Any input can be between V_{SS} and V_{DD} without damaging the chip.

Table 2. Overload (1.00 kHz) Compression (Receive, RGC = 1)

Input/Overload Level (dB)	Maximum Increased Loss (dB) Relative to Overload –3 dB
0	0.2
3	1.8
6	4.6

Note: The filter responses scale linearly with the master clock.

In the following tables and associated figures, the ac characteristics assume that the master clock (R2048) is 2.048 MHz ± 100 ppm.

Table 3. Frequency Response*

Freq (Hz)	Receive Loss (dB)
200	–0.05 to +0.2
300—3000	±0.125
3200	–0.125 to +0.75
3400	0.2 to 0.9
4000	>14
4600	>28
3400—4600	$> 14 \left[\sin \left(\frac{\pi (4000 - f)}{1200} \right) - 1 \right]$

* See Figures 5 and 6 for receive response curves.

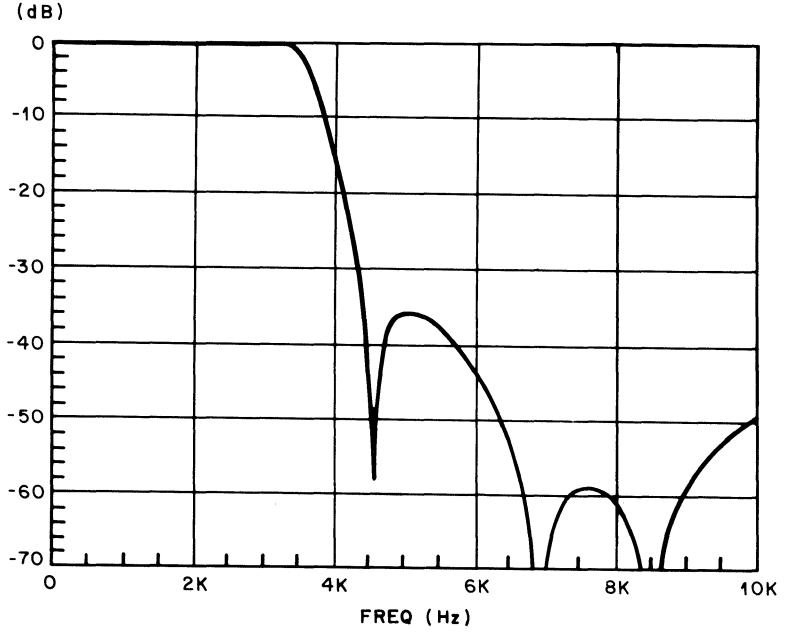


Figure 5. Receive Path Frequency Response

Table 4. Phase and Delay Distortion (End-to-End)*

Freq (Hz)	Phase Deviation from Linearity (Radians)	Delay Distortion (μs, max)
Below 500	$-4.17 + 0.0046f \leq PD \leq 4.17 - 0.0046f$	—
500—700		300
700—2000	Between semicircles of radius 0.92 radians (1150 Hz) centered at $\pm$ 0.95 radians and 1850 Hz	75
2000—2500		150
2500—2700		200
2700—3000		375
3000 and above	$-11.65 + 0.0042f \leq PD \leq 11.65 - 0.0042f$	—

* See Figures 6 and 7 for group delay curves.

Intrachannel Crosstalk (200 Hz to 3400 Hz) < −71 dB

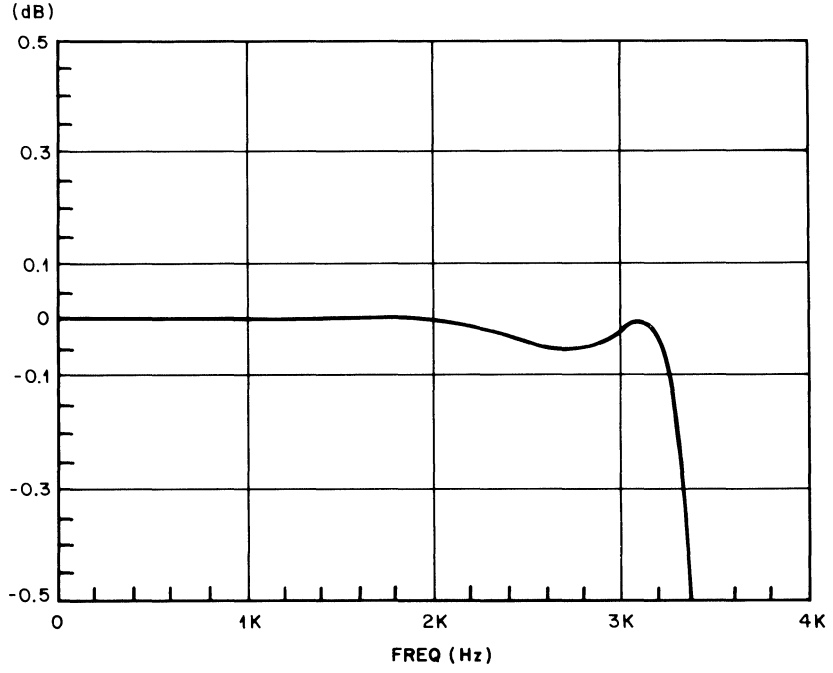


Figure 6. Receive Path Voice Band Response

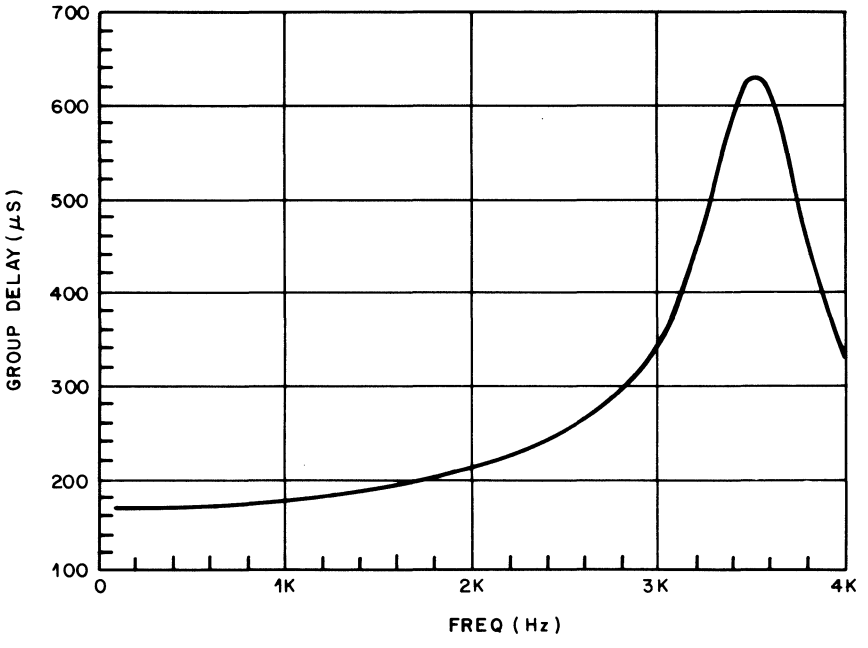


Figure 7. Receive Path Group Delay Response

Table 5. Single Frequency Distortion*

Input/ Max Input (dB)	Input Frequency (Hz)	S/(N+D) (In the 0-kHz to 4-kHz Band) (dB)
0	0 to 4000	60
–10		60
–20		60
–30		55
–40		45

* See Figure 8 for S/(N + D) curve.

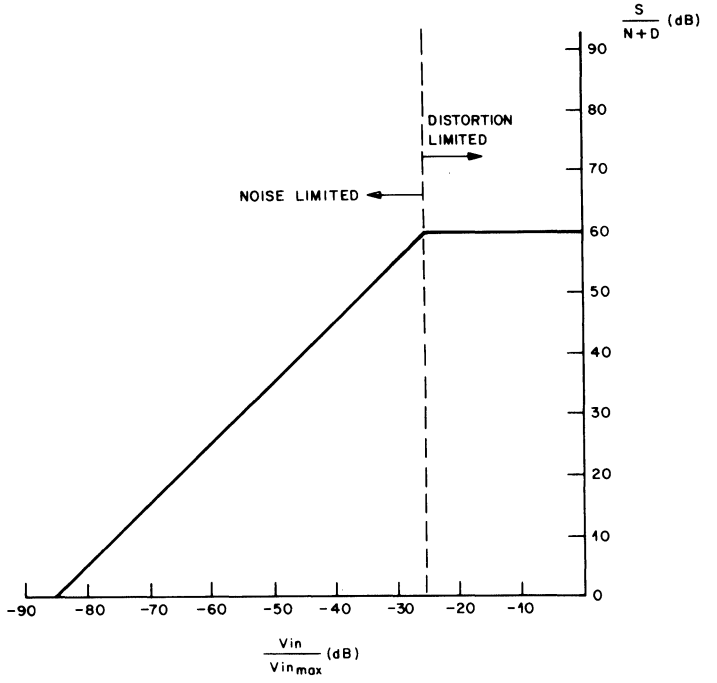


Figure 8. Signal-to-Impairment Characteristic of the Transmit and Receive Paths

Table 6. Intermodulation Distortion (4-Tone Method; Input = –13 dBm0)

r2 < 60 dB below input r3 < 60 dB below input

Transmit (A/D)	Gain	Input Voltage at 1 kHz Corresponding to:		
		Digital mW Out of TPCM	Overload (+3.174 dBm0)	Unit
—	0 dB	1.908	2.75	Vp

Receive (Decoder)	Gain	Output Voltage at 1 kHz Corresponding to:		
		Digital mW Into RPCM	Overload (+3.174 dBm0)	Unit
RGC = 1	3.00 dB	1.547	2.229	Vp
RGC = 0	0 dB	1.095	1.578	Vp

Timing Characteristics

The timing requirements are shown in Figure 9, with expanded details in Figure 10. The duty cycle of T2048 and R2048 must be between 45% and 55%. The encoder and decoder can operate back-to-back if RNSYNC = TNSYNC and R2048 = T2048.

Symbol	Parameter	Capacitance	Min	Max	Unit
tCKLSYL	Synchronization delay	—	10	tCLK – 75	ns
tCKLSYh	Synchronization hold	—	0*	*	ns
tCKHTPV	Transmit prop delay	50 pF	0	140	ns
tRSVCKL	Receive set-up time	—	50	—	ns
tCKLRSX	Receive hold time	—	0	—	ns

* Each synchronization pulse should be low for a minimum of 1 clock cycle after timing edge A, with a maximum of 50% duty cycle. Note that the internal operation of the encoder or decoder is initiated by the first data clock edge that goes negative (timing edge A in Figure 9) after TNSYNC or RNSYNC has gone low.

Timing Diagrams

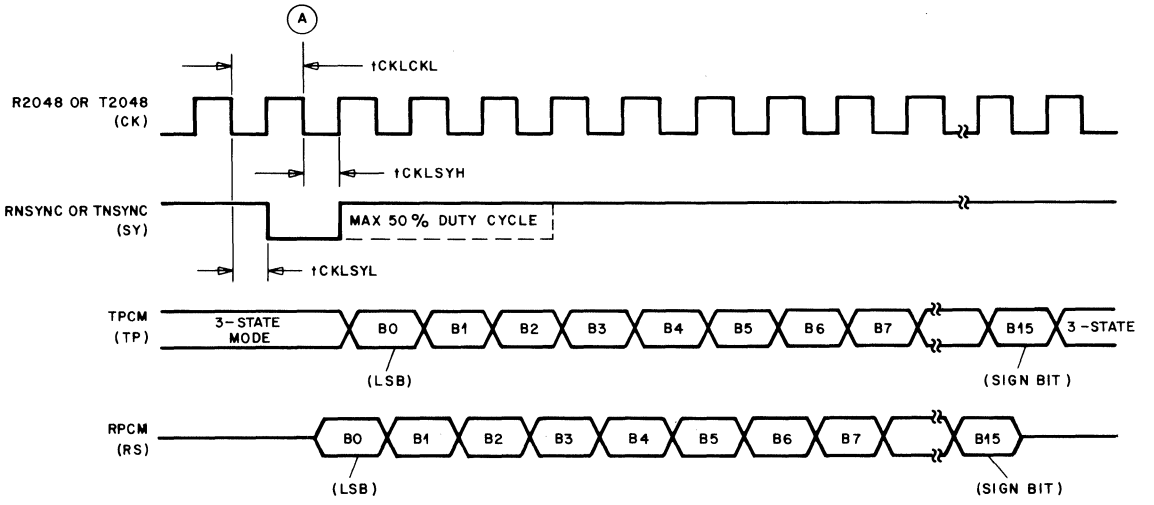


Figure 9. I/O Timing

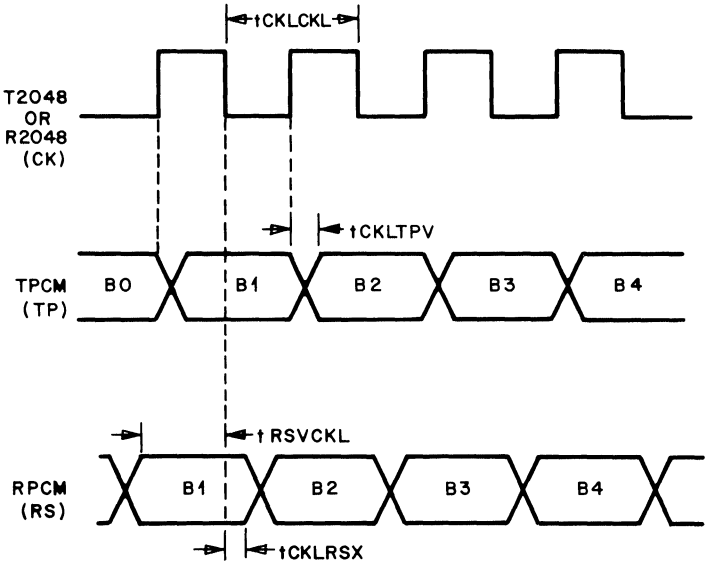


Figure 10. I/O Timing (Enlarged Section)

T7522 High-Precision PCM Codec with Filters

Features

- Encoder and decoder with on-chip filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 120-mW nominal power
- Easy interface to a DSP device
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- 16-bit PCM in 2's complement binary data format (LSB or MSB first)
- Gain selection – transmit: 0 or –3 dB
  receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved PSRR
- A/D filters can be bypassed; A/D has sample and hold built in

Description

The T7522 High-Precision PCM Codec with Filters integrated circuit performs A/D and D/A conversion with 15-bit resolution and 10-bit linearity. The device provides anti-aliasing and reconstruction filters and a precision voltage reference. The device is designed for use in signal processing applications that require PCM data with a higher resolution than that of PCM μ-law data. The T7522 Codec is a linear device with 16-bit PCM I/O data in 2's complement binary format. Typical applications include the use of this codec with echo cancelers, digital signal processors, and in data sets. This chip has selectable LSB or MSB first I/O and the A/D filters can be bypassed. The T7522 Codec is manufactured using CMOS technology and is available in a 24-pin hermetic ceramic DIP.

The T7522 Codec can replace the T7520A and T7521A in applications not requiring independent A/D and D/A power-down options and is recommended for all new designs. Designs requiring the independent A/D and D/A power-down options should use the T7523 Codec.

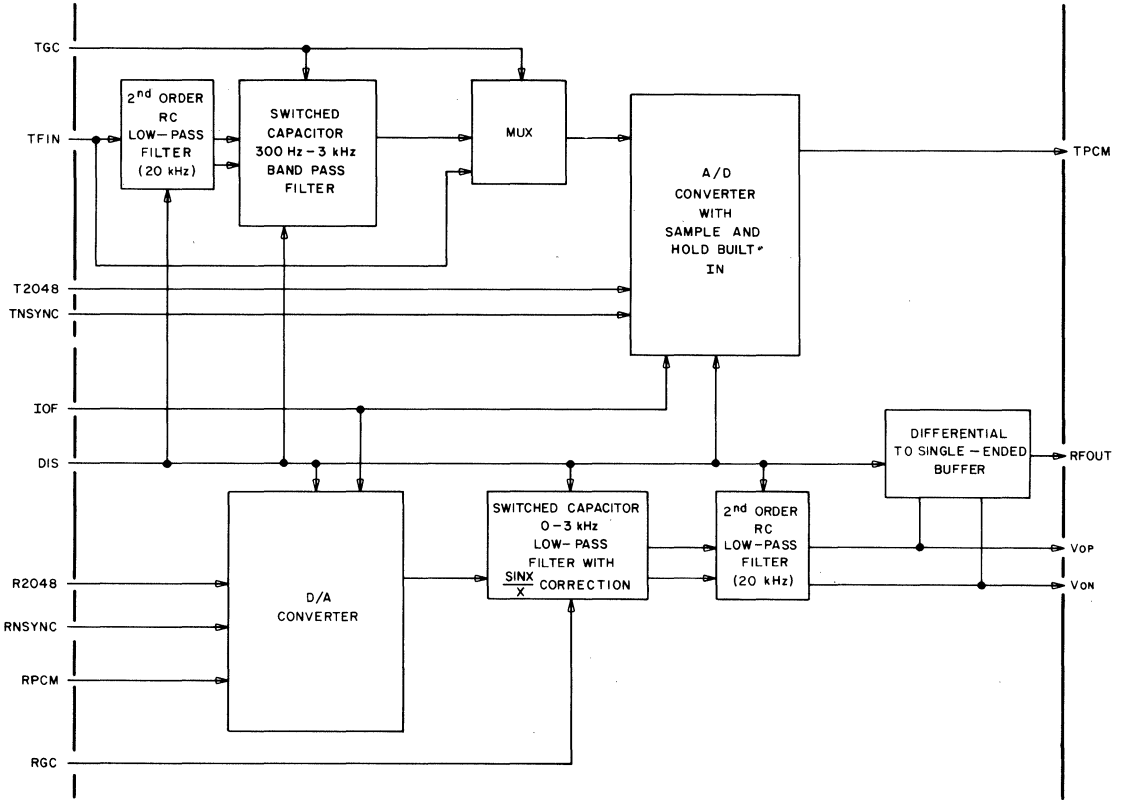
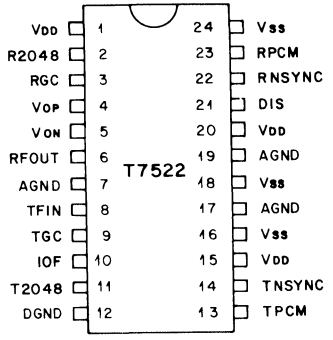


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
AGND	7, 17, 19	TFIN	8
DGND	12	TGC	9
DIS	21	TNSYNC	14
IOF	10	TPCM	13
RFOUT	6	T2048	11
RGC	3	VDD	1, 15, 20
RNSYNC	22	VON	5
RPCM	23	VOP	4
R2048	2	VSS	16, 18, 24

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Symbol	Type	Name/Function
VDD	—	**+5 V Supply (± 5%).***
R2048 (D/A)	I	**Receive Clock.** 2.048 MHz.
RGC (D/A)	I	**Receive Gain Control.** A high on this pin sets the receive gain to +3 dB; a low or no connection sets the gain to 0 dB.
VOP (D/A)	O	**Positive Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
VON (D/A)	O	**Negative Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
RFOUT (D/A)	O	**Receive Filter Output.** A 16-bit digital milliwatt reconstructed by the filter produces a 1.547 Vp signal (when RGC is high). The load resistance must be greater than 20 kΩ in parallel with less than 50 pF.
AGND	—	**Ground (Analog).**
TFIN (A/D)	I	**Transmit Voice Frequency.** For best results, TFIN should be driven from a low-impedance source. When TGC = VSS, the transmit filter is bypassed and TFIN must be driven from a low-impedance, low-noise, fast-settling (0.1% settling in 6 μs) source. A fast-settling op amp is recommended.
TGC (A/D)	I	**Transmit Gain Control.** A high on this pin sets the transmit gain to –3 dB; a low or no connection sets the gain to 0 dB. To bypass the bandpass filter, tie TGC to VSS.
IOF	I/O	**Input/Output Format.** A high sets I/O format to MSB first; a low or no connection sets the I/O format to LSB first.

Table 1. Pin Descriptions (Continued)

Symbol	Type	Name/Function
T2048 (A/D)	I	**Transmit Clock.** 2.048 MHz.
DGND	—	**Ground (Digital).**
TPCM (A/D)	O	**Transmit PCM.**** This pin is used for the 16-bit 2's complement binary PCM (LSB or MSB first) output. (See IOF for PCM format.) This pin is open (3-stated) when inactive.
TNSYNC (A/D)	I	**Transmit Synchronization.**† An accurate timing pulse (negative going edge trigger) is used to start the transmission of the 16 bits of data out of the TPCM. The pulse should be low for at least one transmit data clock period after timing edge A (see Figure 14).
VSS	—	**–5 V Supply (± 5%).***
DIS	I	**Chip Disable.** A high on this pin disables (powers down) the chip; a low or no connection enables the chip.
RNSYNC (D/A)	I	**Receive Synchronization.**† An accurate timing pulse (negative going edge trigger) is used to start the reading of the 16 bits of data into the RPCM. The pulse should remain low for at least one receive data clock period after timing edge A (see Figure 14).
RPCM (D/A)	I	**Receive PCM.**** This pin is used for the 16-bit PCM 2's complement binary (LSB or MSB first) input. (See IOF for PCM format.)
NC	—	**No Connection.**

CAUTION: Cavity cover is internally connected to AGND.
Note: Input high = TTL high (1); low = TTL low (0).
* Both VDD and VSS must be bypassed to analog ground as close to the package as possible with capacitor values greater than 0.2 μF. Best idle channel noise has been obtained by using 10-μF tantalum capacitors.
** The T7522 Codec is a 15-bit coder. The LSB of TPCM is zero added to the end of the output word. The full 16 bits of the RPCM are read in, but only the 15 MSBs are directly used by the D/A converter.
† The synchronization pulse should be low for at least one T2048/R2048 clock period after timing edge A. See Figure 14.

Application Hints

The T7522 High-Precision PCM Codec is a high-performance subsystem. The conditions necessary to achieve reliable codec performance are outlined below.

Supply Routing (See Figure 3)

All the VDD pins must be tied together to avoid excessive substrate currents in the chip.

All VSS pins must be tied together.

All the analog ground pins (AGND) must be tied together.

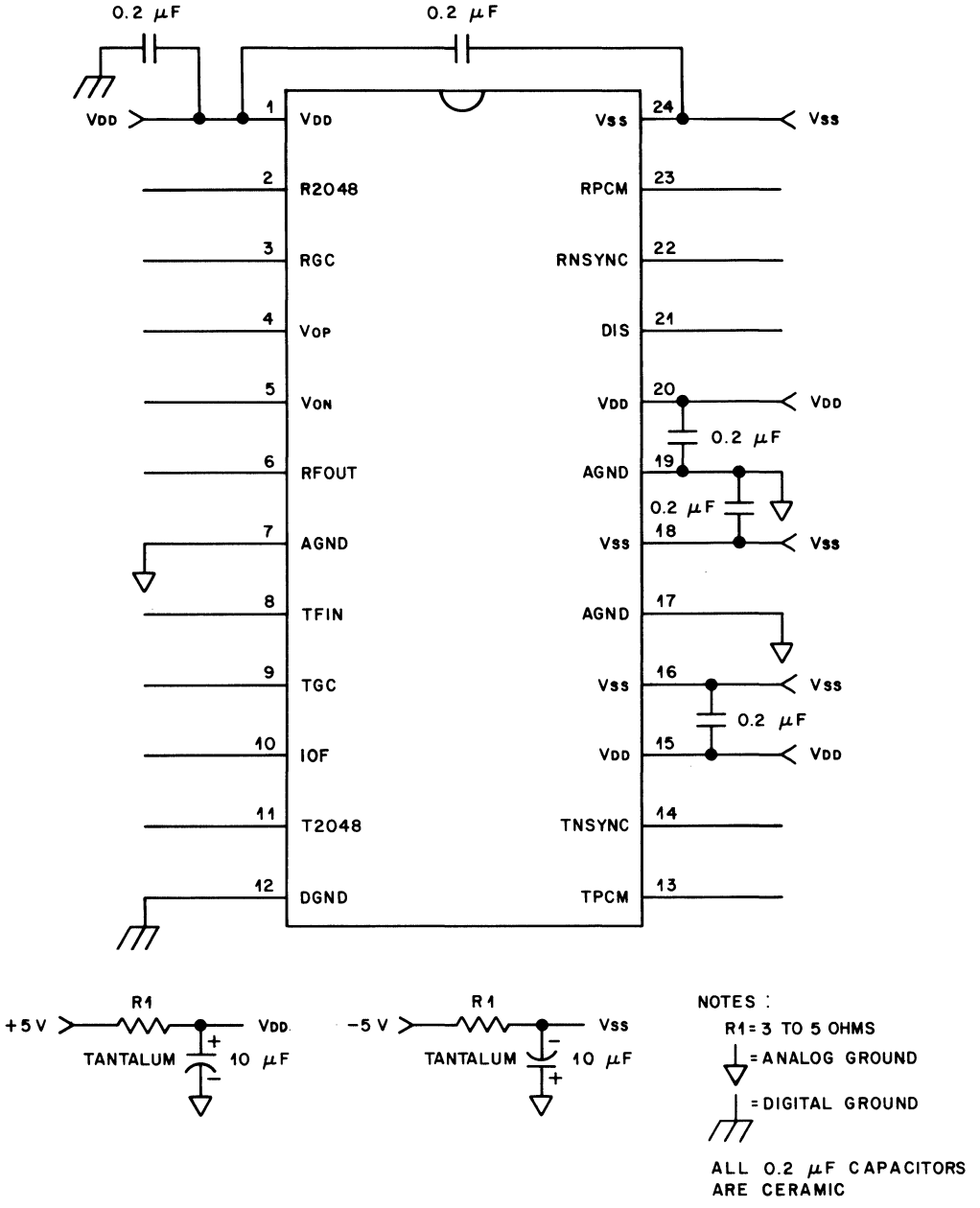


Figure 3. Codec Supply Decoupling

Supply Decoupling

The codec is a sampled data system. As such, noise on the supply lines near multiples of the 8-kHz sample rate are aliased into the codec passband (300 Hz to 3 kHz). For full dynamic range, the noise at the codec pins must be kept below 1 mVrms and 100 mVp (especially those noise components over 100 kHz).

The dominant noise source in many systems is the switching power supply, which typically has significant noise energy extending up into the MHz range. The power busing from the supply to the codec (in a well-designed groundplane system) has an impedance lower than that of most bypass capacitors. Therefore, simply adding bypass capacitors across the codec supply lines does not reduce the power supply noise that feeds into the codec. To keep the noise out of the codec, the codec must be isolated (decoupled) from the noise. The proper decoupling scheme is shown in Figure 3. The 3-Ω to 5-Ω decoupling resistors in series with V_{DD} and V_{SS} with the 10-μF tantalum or low ESR aluminum capacitor form a low-pass filter (–3 dB at a frequency of about 5 kHz). The 0.2-μF ceramic capacitors (located as close to the indicated pins as possible) bypass the high-frequency noise and codec-generated transients.

Fully Synchronous Operation

The transmit and receive paths can be run from separate clocks (Figure 4a). Doing so increases the codec noise floor and can result in various clicks, pops, and squeals in the voice band as separate clocks slide past each other in phase. Do not configure clocks in the manner shown in Figure 4a.

It is strongly recommended that the transmit (T2048) and receive (R2048) master clock lines be tied together, as shown in Figure 4b. The TNSYNC and RNSYNC lines need not be tied together, but it is critical that their sync frequencies be exactly 1/256 of the master clock and satisfy the timing constraints shown in Figure 14. This relationship is shown in Figure 4b by the logic blocks run off the master clock, which drives the codec sync inputs. The timing can be generated by software (in a DSP device, for example); however, the sync timing must be consistent with that shown in Figure 14.

The best performance is achieved by using the fully synchronous timing shown in Figure 4c. The transmit and receive paths use the same master and sync clocks, and the sync is directly derived from the master clock.

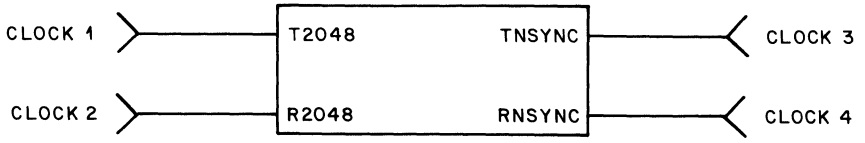
I/O Routing

This codec has a dynamic range of over 80 dB. The routing of the analog input (TFIN) and outputs (RFOUT, VOP, and VON) must be kept away from noise sources, especially signal-dependent digital lines.

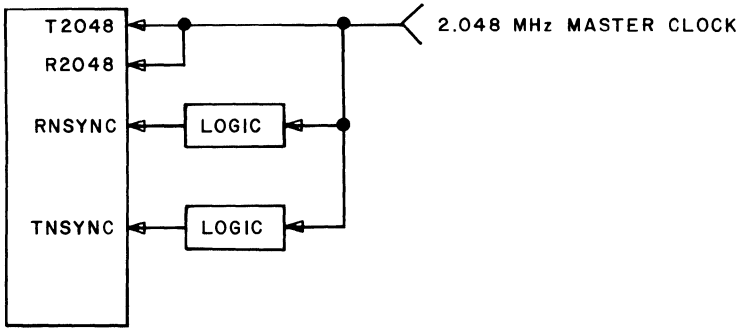
To help reduce coupling into the transmit path, TFIN should be driven from a low-impedance source.

Miscellaneous

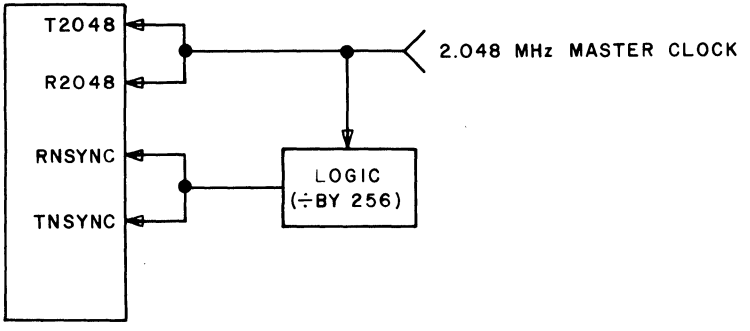
The TFIN pin must have a dc path to ground. If the signal source is ac-coupled to the codec, a resistor must be connected from TFIN to AGND. When TGC = V_{SS} (A/D filter bypassed), drive TFIN with a fast-settling (0.1% in 6 μs), low-impedance source.



a. Not Recommended (Do Not Do This)



b. Acceptable Chip Timing (Better, but Not Optimum)



c. Recommended Chip Timing (Optimum)

Figure 4. Chip Timing Schemes

Definitions

Analog sine wave levels:	0 dBm = 90 dBrn = 0.775 Vrms = 1.095 Vp into 600 Ω
0 dBm0 at TFIN and TPCM:	An analog sine wave input at TFIN of 1.095 Vp (TGC = 0) or 1.547 Vp (TGC = 1) and the corresponding digital output word at TPCM
0 dBm0 at RPCM and RFOUT:	A digital sine wave input at RPCM and the corresponding analog output of 1.095 Vp (RGC = 0) or 1.547 Vp (RGC = 1) at RFOUT
Overload or clipping levels:	3.174 dBm0 at all I/Os

All noise and distortion measurements given in dBrn or dB are flat weighted and integrated over the 300-Hz to 3400-Hz frequency band. Where the specification unit has "C" appended to it, C message weighting has been used.

Characteristics

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = –5 V ± 5%

Parameter	Limits			Unit
	Min	Typ	Max	
Analog overload at 1.02 kHz:				
transmit (A/D), receive (D/A)				
TGC = RGC = 0	±1.551	±1.578	±1.606	Vp
TGC = RGC = 1	±2.161	±2.229	±2.299	Vp
transmit (A/D)				
TGC = V_{SS}	±2.641	±2.75	±2.863	Vp
Supply current (I_{DD}, I_{SS}):				
DIS = 0	—	—	20	mA
DIS = 1	—	—	0.1	mA
Absolute gain at 1.02 kHz				
0 dBm0 signal (3.174 dB below overload)				
TGC = RGC = 0	—	—	±0.15	dB
Gain tracking (gain linearity error) at 1.02 kHz				
0 dBm0 reference:				
0 dBm0 to –40 dBm0	—	—	±0.2	dB
–40 dBm0 to –53 dBm0	—	—	±0.4	dB
Idle channel noise:				
transmit (A/D) measured at TPCM				
TGC = 0 or 1	—	—	15	dBrn
	—	—	12	dBrnC
TGC = V_{SS}	—	—	12	dBrn
	—	—	9	dBrnC
transmit (A/D) referred to TFIN				
TGC = 0	—	—	15	dBrn
	—	—	12	dBrnC
TGC = 1	—	—	18	dBrn
	—	—	15	dBrnC
TGC = V_{SS}	—	—	16	dBrn
	—	—	14	dBrnC

Parameter	Limits			Unit
	Min	Typ	Max	
Idle channel noise:				
receive (D/A) measured at RFOUT				
RGC = 0 or 1	—	—	11	dBrn
	—	—	8	dBrnC
receive (D/A) referred to RPCM				
RGC = 0	—	—	11	dBrn
	—	—	8	dBrnC
RGC = 1	—	—	8	dBrn
	—	—	5	dBrnC
DC offset:				
transmit (A/D) measured at TPCM				
TGC = 0 or 1	—	—	±330	LSBs*
TGC = V_{SS}	—	—	±30	LSBs*
transmit (A/D) referred to TFIN				
TGC = V_{SS}	—	—	±5	mV
TGC = 1	—	—	±45	mV
TGC = 0	—	—	±32	mV
receive (D/A) measured at RFOUT				
RGC = 0 or 1	—	—	±140	mV
Power supply rejection ratio (PSRR) at 3140 Hz:				
transmit				
V_{DD}	30	—	—	dB
V_{SS}	33	—	—	dB
receive				
V_{DD}	30	—	—	dB
V_{SS}	33	—	—	dB
Absolute delay (end-to-end) at 1 kHz	—	—	575	μs

* Offset in A/D LSBs. The 15-bit A/D output is filled out to 16 bits by appending a 0 to the LSB. Multiply the offset (in LSBs) by two when referring to the full 16-bit word.

Analog Interface

TFIN: Rin > 1 MΩ and Cin < 10 pF, when TGC = logic 1 or 0
Rin > 1 MΩ and Cin < 100 pF, when TGC = V_{SS}
RFOUT: ac impedance < 300 Ω, max current 150 μA

Any input can be connected between V_{SS} and V_{DD} without damaging the chip.

Digital Interface

All inputs: TTL-compatible, Iin < 20 μA, < 5-pF loading
TPCM: Capable of driving a 50-pF capacitance to TTL voltage levels at 2.048 Mb/s

Any input can be connected between V_{SS} and V_{DD} without damaging the chip.

Table 2. Overload (1.02 kHz) Compression

Input/Overload Level	Minimum Output Relative to 0 dBm0 Input (dB)
–3.17 dB = 0.0 dBm0	Reference
0.0 dB = 3.17 dBm0	3.17 – 0.2 = 2.97
3.0 dB = 6.17 dBm0	6.17 – 1.8 = 4.37
6.0 dB = 9.17 dBm0	9.17 – 4.6 = 4.57

In the following tables and associated figures, the ac characteristics assume that the master clock (T2048, R2048) is 2.048 MHz ± 100 ppm.

Note: The filter responses scale linearly with the master clock.

Table 3. Frequency Response Relative to Gain at 1.02 kHz*

Freq (Hz)	Transmit Loss (dB)	Receive Loss (dB)
50—60	≥ 20	±0.2
100	–0.2 to +7	±0.2
200	0.1 to 1.8	±0.2
300—3140	±0.125	±0.125
3200	–0.125 to +0.75	–0.125 to +0.75
3400	0.2 to 0.9	0.2 to 0.9
4000	>14	>14
4600 and above	>32	>28
3400—4000	$> 14 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - 1 \right]$	$> 14 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - 1 \right]$
4000—4600	$> 18 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - \frac{7}{9} \right]$	

* See Figures 5 through 9 for response curves.

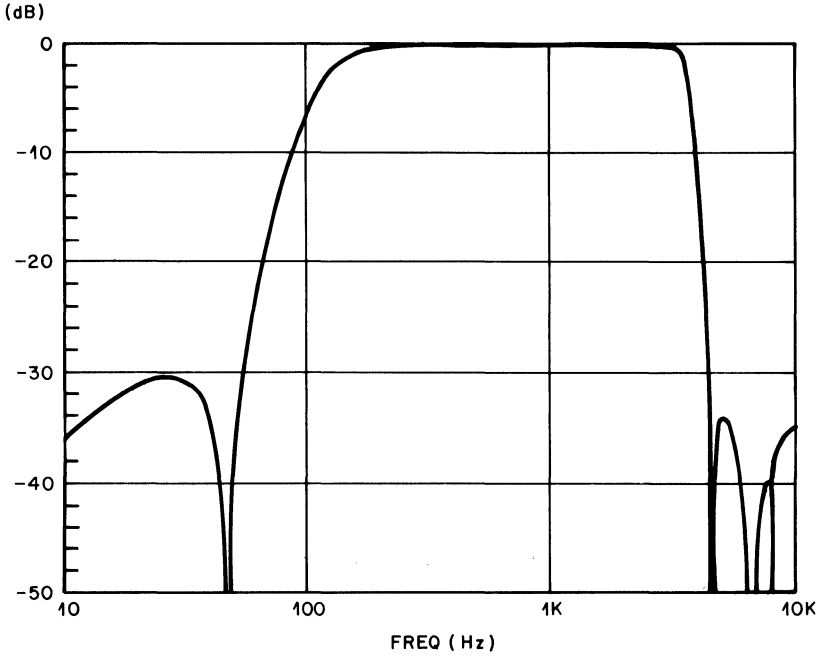


Figure 5. Transmit Path Frequency Response

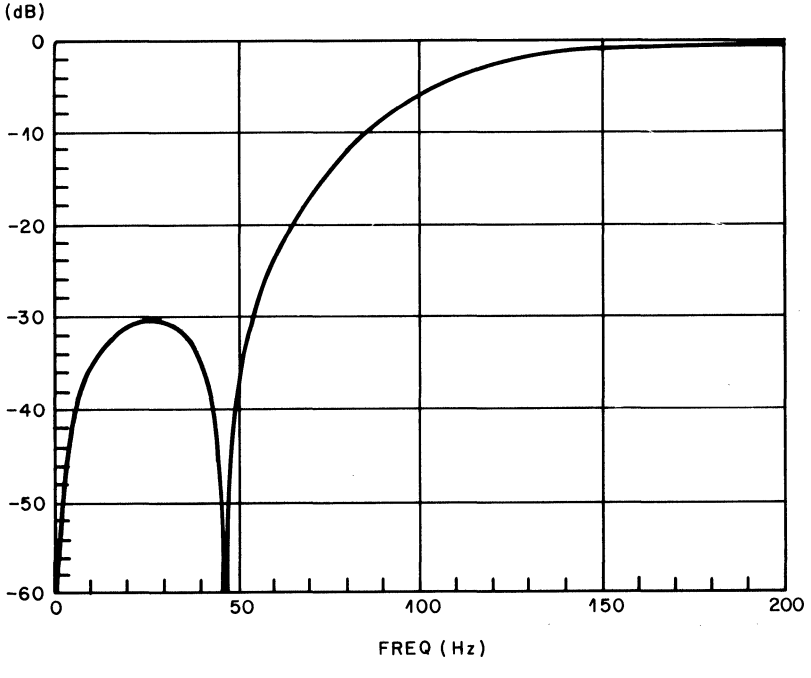


Figure 6. Transmit Path Low-Frequency Response

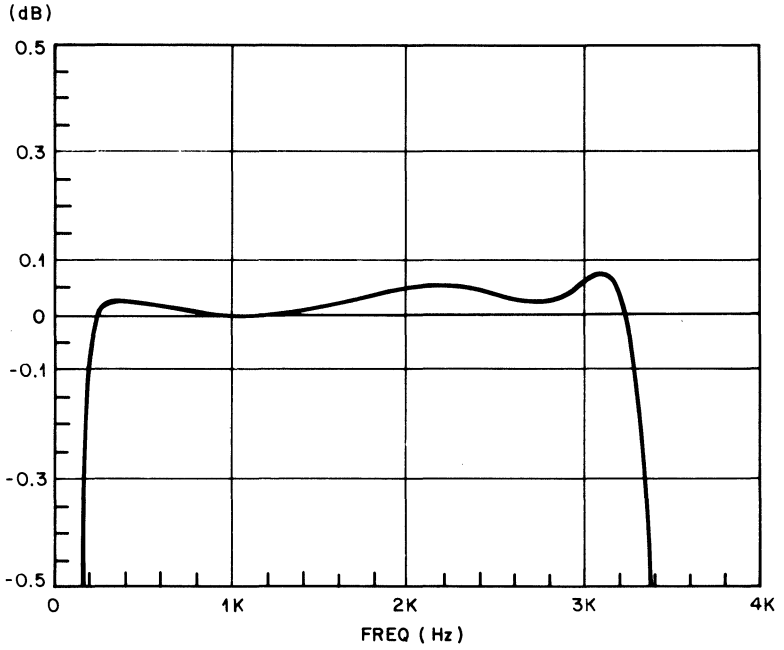


Figure 7. Transmit Path Voice Band Response

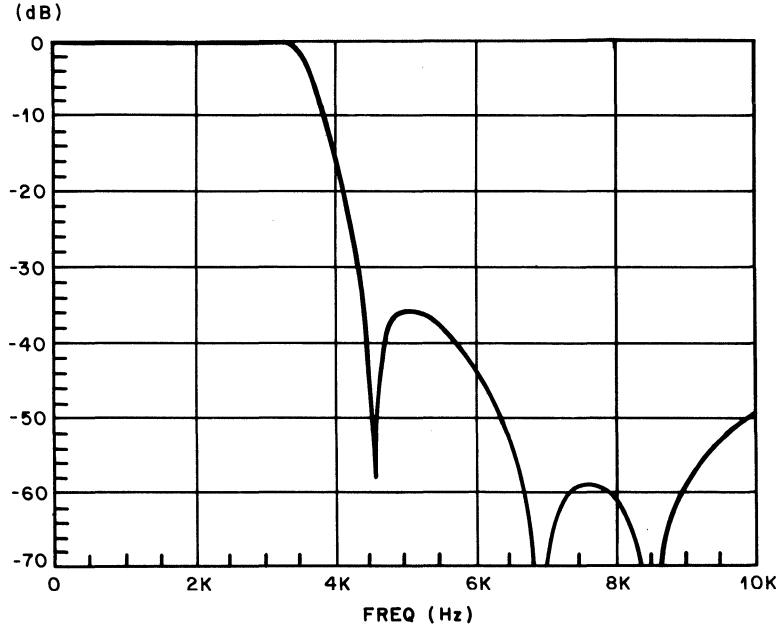


Figure 8. Receive Path Frequency Response

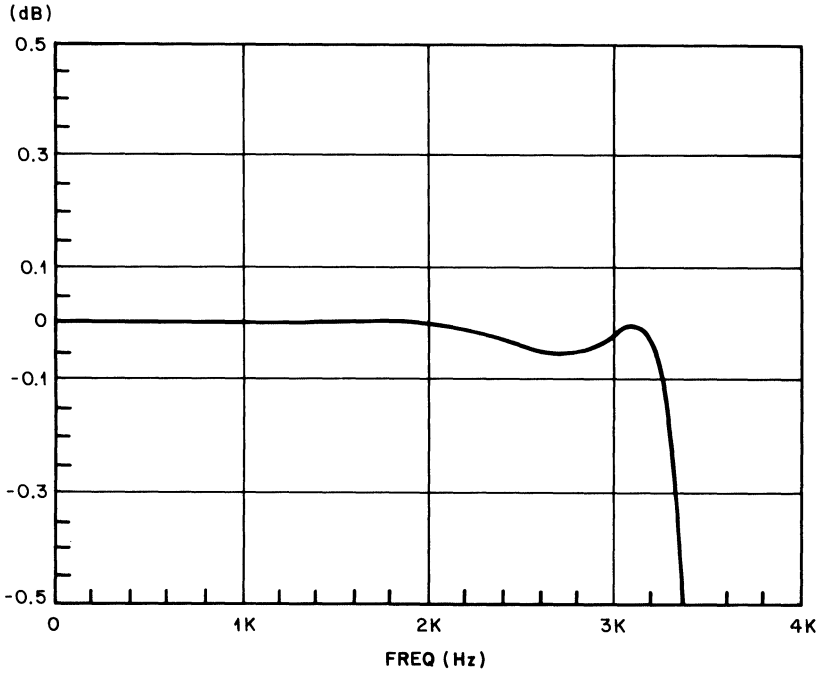


Figure 9. Receive Path Voice Band Response

Table 4. Phase and Delay Distortion (End-to-End)*

Freq (Hz)	Phase Deviation from Linearity (Radians)	Delay Distortion (μs, max)
Below 500	$-4.17 + 0.0046f \leq PD \leq 4.17 - 0.0046f$	—
500—700		300
700—2000	Between semicircles of radius 0.92 radians (1150 Hz) centered at ± 0.95 radians and 1850 Hz	75
2000—2500		150
2500—2700		200
2700—3000		375
3000 and above	$-11.65 + 0.0042f \leq PD \leq 11.65 - 0.0042f$	—

* See Figures 10, 11, and 12 for group delay curves.

Intrachannel Crosstalk (200 Hz to 3400 Hz) < –75 dB

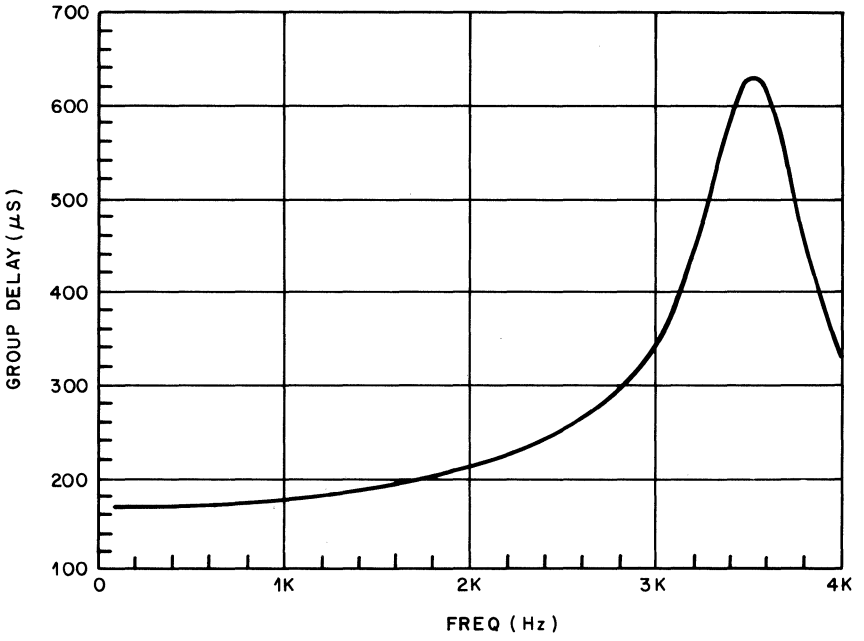


Figure 10. Receive Path Group Delay Response

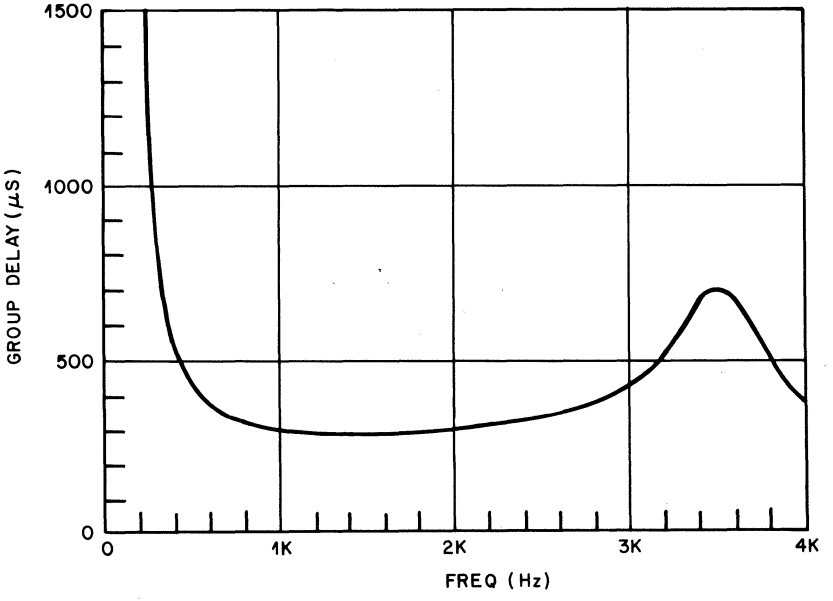


Figure 11. Transmit Path Group Delay Response

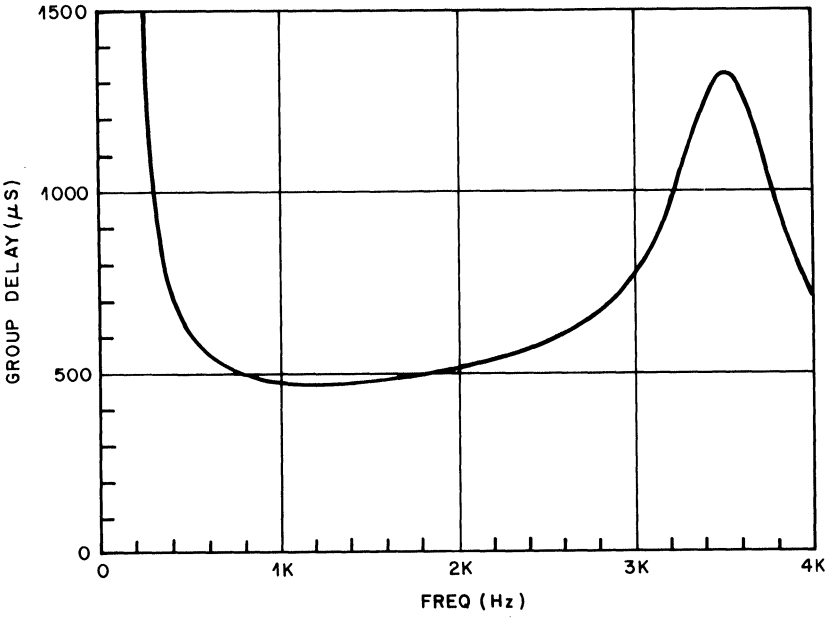
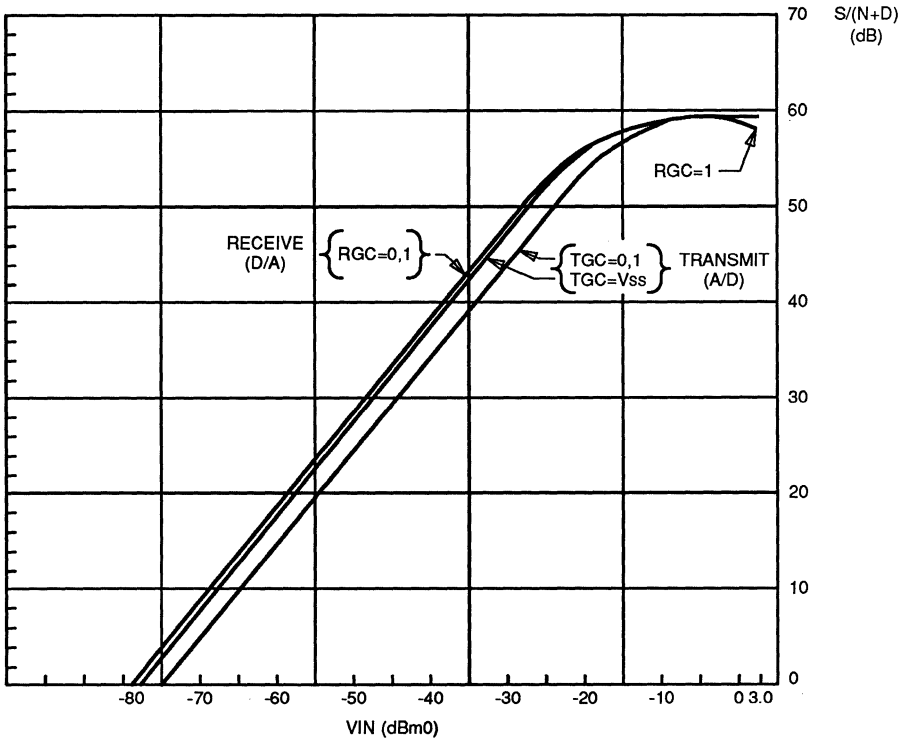


Figure 12. End-to-End Group Delay

Table 5. Single Frequency Distortion Measured at TPCM or RFOUT*

Digital Signal Level (TPCM, RPCM) (dBm0)	Input Frequency (Hz)	S/(N+D) (300-Hz—3400-Hz Band)							
		Receive (D/A)				Transmit (A/D)			
		RGC = 0		RGC = 1		TRC = 0,1		TGC = Vss	
		(dB)	(dBC)	(dB)	(dBC)	(dB)	(dBC)	(dB)	(dBC)
3	300 to 3400	60	60	55	55	60	60	60	60
0		60	60	59	59	60	60	60	60
–7		59	60	59	60	59	60	59	60
–17		58	59	58	59	56	57	57	58
–27		51	53	51	53	48	50	50	52
–37		42	44	42	44	38	40	41	43
–47		32	34	32	34	28	30	31	33

* See Figure 13 for S/(N+D) curve.



Note: Measured at TPCM for transmit (A/D) path and at RFOUT for receive (D/A) path.

Figure 13. Signal-to-Impairment Characteristics of the Transmit and Receive Paths

Transmit (Encoder)	Gain	Input Voltage at 1 kHz Corresponding to: Digital mW Out of TPCM	Overload (+3.174 dBm0)	Unit
TGC = 0	0 dB (reference)	1.095	1.578	Vp
TGC = 1	–3.00 dB ± 0.12 dB	1.547	2.229	Vp
TGC = Vss	–4.82 dB ± 0.20 dB	1.908	2.750	Vp

Receive (Decoder)	Gain	Output Voltage at 1 kHz Corresponding to: Digital mW Into RPCM	Overload (+3.174 dBm0)	Unit
RGC = 1	3.00 dB ± 0.12 dB	1.547	2.229	Vp
RGC = 0	0 dB (reference)	1.095	1.578	Vp

Timing Characteristics

The timing requirements are shown in Figure 14, with expanded details in Figure 15. The duty cycle of T2048 and R2048 must be between 45% and 55%. The encoder and decoder can operate back-to-back if RNSYNC = TNSYNC and R2048 = T2048.

Symbol	Parameter	Capacitance	Min	Max	Unit
tCKLSYL	Synchronization delay	—	10	tCLK – 75	ns
tCKLSYH	Synchronization hold	—	0*	*	ns
tCKHTPV	Transmit prop delay	50 pF	0	140	ns
tRSVCKL	Receive set-up time	—	100	—	ns
tCKLRSX	Receive hold time	—	0	—	ns

* Each synchronization pulse should be low for a minimum of 1 clock cycle after timing edge A, with a maximum of 50% duty cycle. Note that the internal operation of the encoder or decoder is initiated by the first data clock edge that goes negative (timing edge A in Figure 14) after TNSYNC or RNSYNC has gone low.

Timing Diagrams

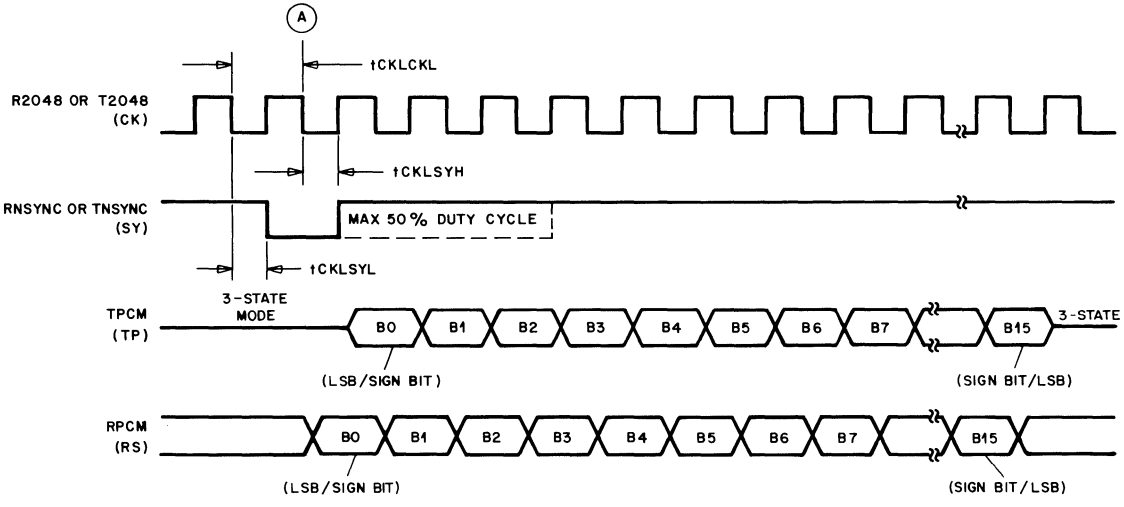


Figure 14. I/O Timing

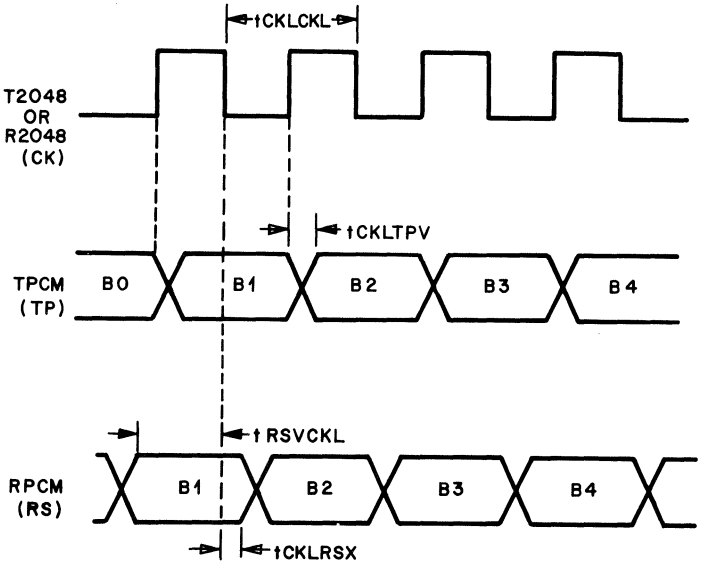


Figure 15. I/O Timing (Enlarged Section)

T7523 High-Precision PCM Codec with Filters

Features

- Encoder and decoder with on-chip filters
- On-chip precision-trimmed reference voltages
- Charge redistribution and switched capacitor techniques
- ±5 V power supplies, with 120-mW nominal power
- Independent transmit and receive power-down
- Easy interface to industry-standard DSP devices
- Sync deglitching circuitry on-chip
- 3-state TTL-output bus
- 16-bit PCM in 2's complement binary data format (LSB first I/O)
- Gain selection – transmit: 0 or –3 dB
  receive: +3 or 0 dB
- Guaranteed monotonic to 15 bits
- Balanced filters for improved power supply rejection ratio (PSRR)
- A/D filters can be bypassed; A/D has sample and hold built in

Description

The T7523 High-Precision PCM Codec with Filters integrated circuit performs A/D and D/A conversion with 15-bit resolution and 10-bit linearity. The device is designed for use in signal processing applications that require PCM data with a higher resolution than that of PCM μ-law data. The T7523 Codec is a linear device with 16-bit PCM I/O data in 2's complement binary format (LSB first). Typical applications include the use of this codec with echo cancelers, digital signal processors, and in data sets. The T7523 Codec is manufactured using CMOS technology and is available in a 24-pin hermetic ceramic DIP.

The T7523 Codec is a pin-for-pin replacement and upgrade for the T7520A and T7521A Codecs, and is recommended for all new designs. Applications requiring MSB first PCM I/O should use the T7522 Codec.

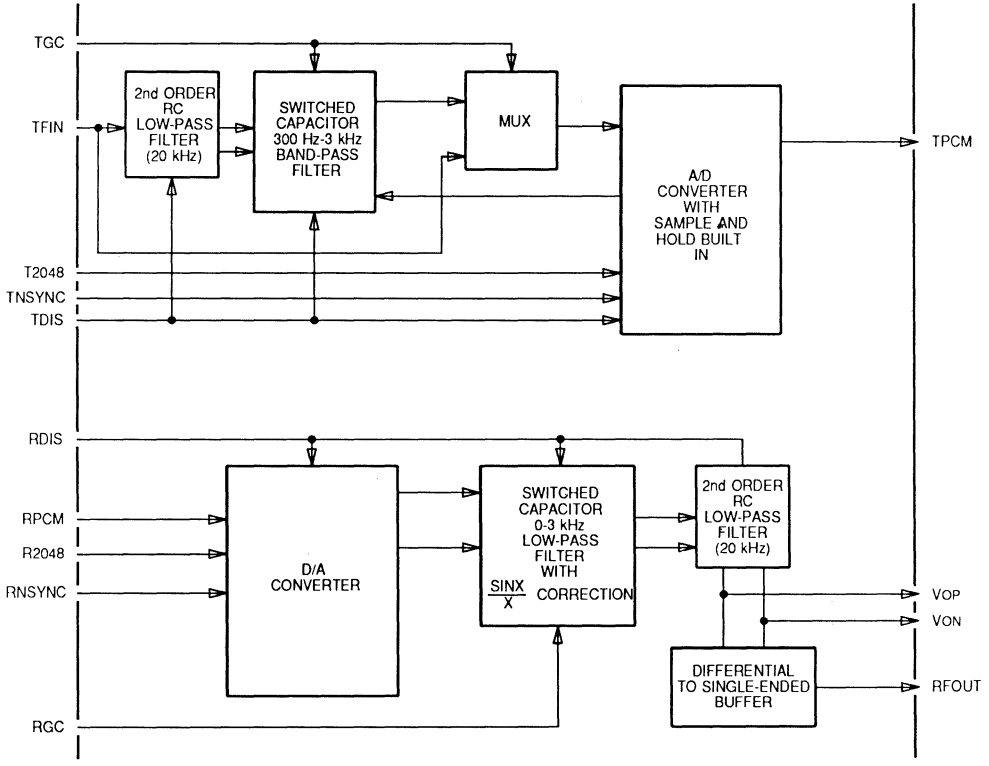
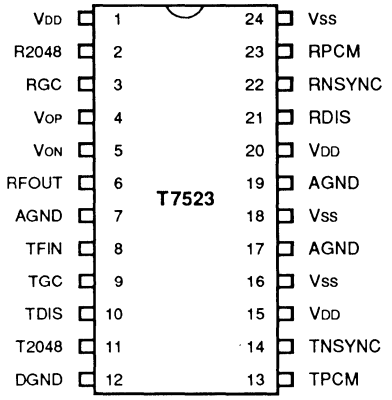


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
AGND	7, 17, 19	TFIN	8
DGND	12	TGC	9
RDIS	21	TNSYNC	14
RFOUT	6	TPCM	13
RGC	3	T2048	11
RNSYNC	22	VDD	1, 15, 20
RPCM	23	VON	5
R2048	2	VOP	4
TDIS	10	VSS	16, 18, 24

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Symbol	Type	Name/Function
VDD	—	**+5 V Supply (± 5%).***
R2048 (D/A)	I	**Receive Clock.** 2.048 MHz.
RGC (D/A)	I	**Receive Gain Control.** A high on the pin sets the receive gain to +3 dB; a low or no connection sets the gain to 0 dB.
VOP (D/A)	O	**Positive Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
VON (D/A)	O	**Negative Receive Filter Balanced Output.** Rload must be greater than 100 kΩ in parallel with less than 10 pF.
RFOUT (D/A)	O	**Receive Filter Output.** A single-ended version of VON and VOP. The load resistance must be greater than 20 kΩ in parallel with less than 50 pF.
AGND	—	**Ground (Analog).**
TFIN (A/D)	I	**Transmit Voice Frequency.** For best results, TFIN should be driven from a low-impedance source. When TGC = VSS, the transmit filter is bypassed and TFIN must be driven from a low-impedance, low-noise, fast-settling (0.1% settling in 6 μs) source. A fast-settling op amp is recommended.
TGC (A/D)	I	**Transmit Gain Control.** A high on this pin sets the transmit gain to –3 dB; a low or no connection sets the gain to 0 dB. To bypass the transmit filter, tie TGC to VSS.
TDIS (A/D)	I	**Transmit Disable.** A high on this pin disables (powers down) the transmit (A/D) path; a low or no connection enables the transmit side.

Table 1. T7523 Codec Pin Descriptions (Continued)

Symbol	Type	Name/Function
T2048 (A/D)	I	**Transmit Clock.** 2.048 MHz.
DGND	—	**Ground (Digital).**
TPCM (A/D)	O	**Transmit PCM.**** This pin is used for the A/D 16-bit 2's complement binary PCM (LSB first) output. This pin is 3-stated when inactive.
TNSYNC (A/D)	I	**Transmit Synchronization.**† An accurate timing pulse (negative going edge trigger) is used to start the transmission of the 16 bits of data out of the TPCM. The pulse should be low for at least one transmit data clock period after timing edge A (see Figure 14).
VSS	—	**–5 V Supply (± 5%).***
RDIS (D/A)	I	**Receive Disable.** A high on this pin disables (powers down) the receive (D/A) path; a low or no connection enables the receive side.
RNSYNC (D/A)	I	**Receive Synchronization.**† An accurate timing pulse (negative going-edge trigger) is used to start reading the 16 bits of data into the RPCM. The pulse should remain low for at least one receive data clock period after timing edge A (see Figure 14).
RPCM (D/A)	I	**Receive PCM.**** This pin is used for the D/A 16-bit PCM 2's complement binary (LSB first) input.

CAUTION: Cavity cover is internally connected to AGND.

Note: Input high = TTL high (1); low = TTL low (0).

* Both VDD and VSS must be bypassed to analog ground as close to the package as possible with capacitor values greater than 0.2 μF. Best idle channel noise has been obtained by using 10-μF tantalum capacitors.

** The T7523 Codec is a 15-bit coder. The LSB of TPCM is 0 added to the end of the output word. The full 16 bits of the RPCM are read in, but only the 15 MSBs are directly used by the D/A converter.

† The synchronization pulse should be low for at least one T2048/R2048 clock period after timing edge A. See Figure 14.

Application Hints

The T7523 High-Precision PCM Codec is a high-performance subsystem. The conditions necessary to achieve reliable codec performance are outlined below.

Supply Routing (See Figure 3)

All the VDD pins must be tied together to avoid excessive substrate currents in the chip.

All the VSS pins must be tied together.

All the analog pins (AGND) must be tied together.

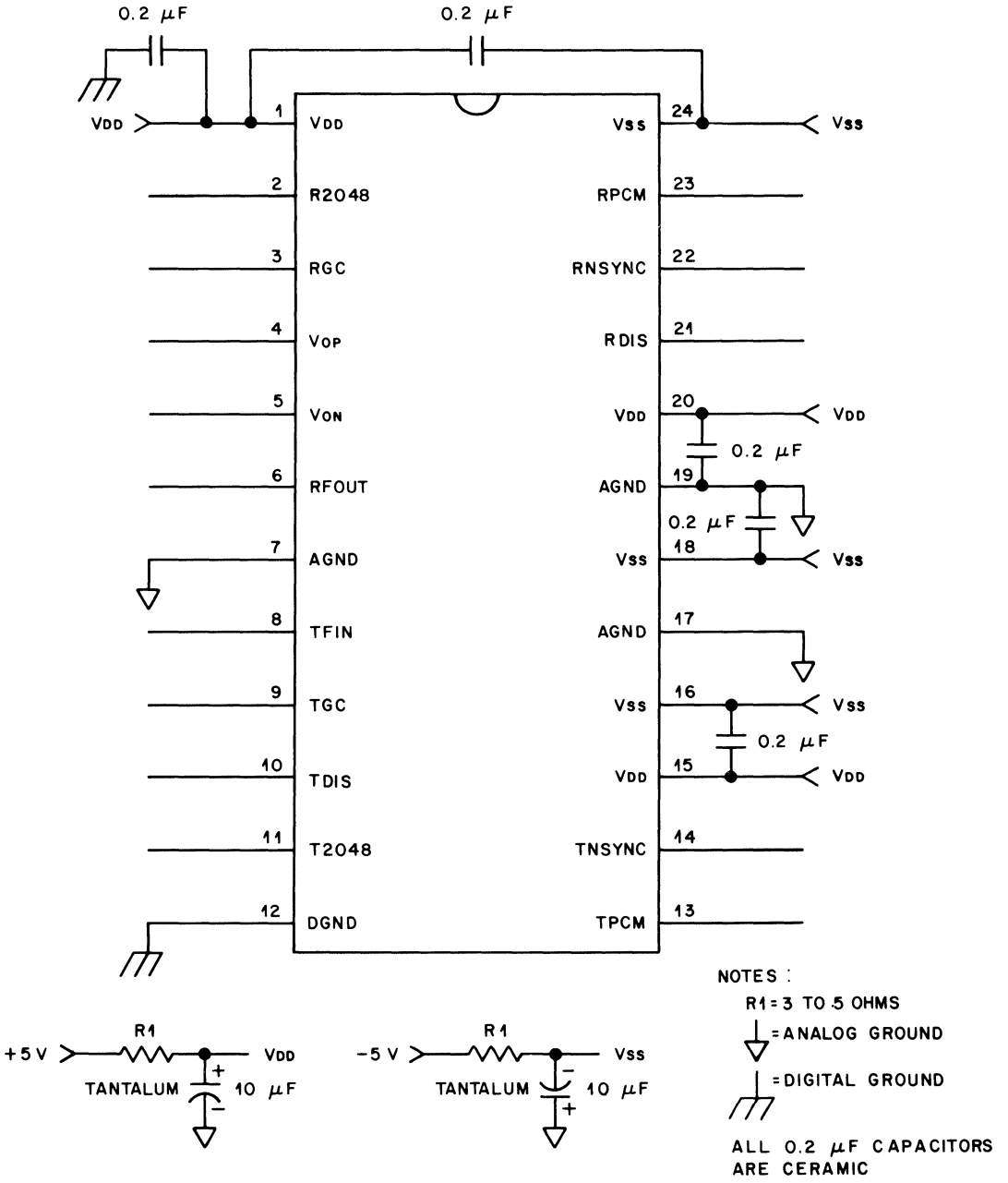


Figure 3. Codec Supply Decoupling

Supply Decoupling

The codec is a sampled data system. As such, noise on the supply lines near multiples of the 8-kHz sample rate are aliased into the codec passband (300 Hz to 3 kHz). For full dynamic range, the noise at the codec pins must be kept below 1 mVrms and 100 mVp (especially those noise components over 100 kHz).

The dominant noise source in many systems is the switching power supply, which typically has significant noise energy extending up into the MHz range. The power busing from the supply to the codec (in a well-designed groundplane system) has an impedance lower than that of most bypass capacitors. Therefore, simply adding bypass capacitors across the codec supply lines does not reduce the power supply noise that feeds into the codec. To keep the noise out of the codec, the codec must be isolated (decoupled) from the noise. The proper decoupling scheme is shown in Figure 3. The 3-Ω to 5-Ω decoupling resistors in series with V_{DD} and V_{SS} with the 10-μF tantalum or low ESR aluminum capacitor form a low-pass filter (–3 dB at a frequency of about 5 kHz). The 0.2-μF ceramic capacitors (located as close to the indicated pins as possible) bypass the high-frequency noise and codec-generated transients.

Fully Synchronous Operation

The transmit and receive paths can be run from separate clocks (Figure 4a). Doing so increases the codec noise floor and can result in various clicks, pops, and squeals in the voice band as separate clocks slide past each other in phase. Do not configure clocks in the manner shown in Figure 4a.

The transmit (T2048) and receive (R2048) master clock lines should be tied together, as shown in Figure 4b. The TNSYNC and RNSYNC lines need not be tied together, but it is critical that their sync frequencies be exactly 1/256 of the master clock and satisfy the timing constraints shown in Figure 14. This relationship is shown in Figure 4b by the logic blocks run off the master clock, which drives the codec sync inputs. The timing can be generated by software (in a DSP device, for example); however, the sync timing must stay locked to the master clock and satisfy the timing shown in Figure 14.

The best performance is achieved by using the fully synchronous timing scheme shown in Figure 4c. The transmit and receive paths use the same master and sync clocks, and the sync is derived directly from the master clock.

I/O Routing

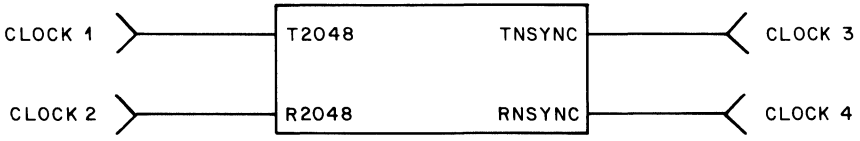
This codec has a dynamic range of over 80 dB. The routing of the analog input (TFIN) and outputs (RFOUT, V_{OP}, and V_{ON}) must be kept away from noise sources, especially signal-dependent digital lines.

To help reduce coupling into the transmit path, TFIN should be driven from a low-impedance source.

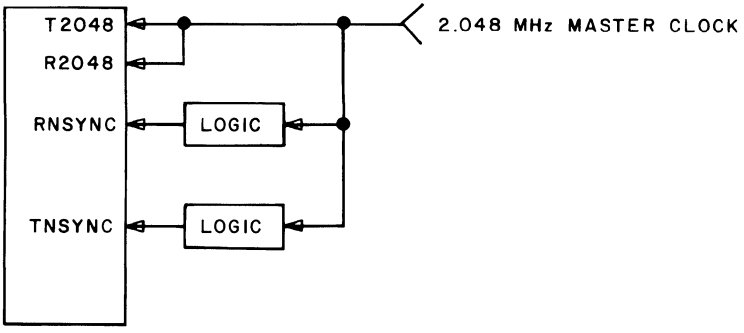
Miscellaneous

The TFIN pin must have a dc path to ground. If the signal source is ac-coupled to TFIN, a resistor must be connected from TFIN to AGND. A low-impedance signal source minimizes stray coupling into TFIN.

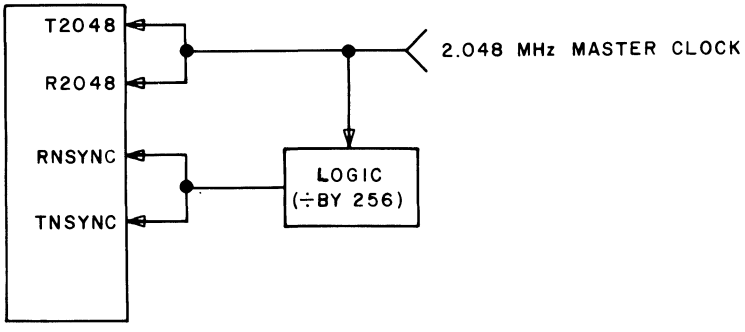
When TGC = V_{SS} (filter bypassed), drive TFIN with a fast-settling source (0.1% in 6 μs). The input impedance is 1 MΩ in parallel with 80 pF. An external sample and hold (S/H) is not needed, since the A/D has one built in.



a. Not Recommended (Do Not Do This)



b. Acceptable Chip Timing (Better, but Not Optimum)



c. Recommended Chip Timing (Optimum)

Figure 4. Chip Timing Schemes

Definitions

Analog sine wave levels:	0 dBm = 90 dBrn = 0.775 Vrms = 1.095 Vp into 600 Ω
0 dBm0 at TFIN and TPCM:	An analog sine wave input at TFIN of 1.095 Vp (TGC = 0) or 1.547 Vp (TGC = 1) and the corresponding digital output word at TPCM
0 dBm0 at RPCM and RFOUT:	A digital sine wave input at RPCM and the corresponding analog output of 1.095 Vp (RGC = 0) or 1.547 Vp (RGC = 1) at RFOUT
Overload or clipping levels:	3.174 dBm0 at all I/Os

All noise and distortion measurements given in dBrn or dB are flat weighted and integrated over the 300-Hz to 3400-Hz frequency band. Where the specification unit has "C" appended to it, C message weighting has been used.

Characteristics

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = –5 V ± 5%

Parameter	Limits			Unit
	Min	Typ	Max	
Analog overload at 1.02 kHz:				
transmit (A/D), receive (D/A)				
TGC = RGC = 0	±1.551	±1.578	±1.606	Vp
TGC = RGC = 1	±2.161	±2.229	±2.299	Vp
transmit (A/D)				
TGC = V_{SS}	±2.641	±2.75	±2.863	Vp
Supply current (I_{DD}, I_{SS}):				
TDIS = RDIS = 0	—	—	20	mA
RDIS = 1 (D/A) off, TDIS = 0	—	—	12	mA
TDIS = 1 (A/D) off, RDIS = 0	—	—	8	mA
TDIS = RDIS = 1 (chip off)	—	—	0.1	mA
Absolute gain at 1.02 kHz				
0 dBm0 signal (3.174 dB below overload)				
TGC = RGC = 0	—	—	±0.15	dB
Gain tracking (gain linearity error) at 1.02 kHz				
0 dBm0 reference:				
0 dBm0 to –40 dBm0	—	—	±0.2	dB
–40 dBm0 to –53 dBm0	—	—	±0.4	dB
Idle channel noise:				
transmit (A/D) measured at TPCM				
TGC = 0 or 1	—	—	15	dBrn
	—	—	12	dBrnC
TGC = V_{SS}	—	—	12	dBrn
	—	—	9	dBrnC
transmit (A/D) referred to TFIN				
TGC = 0			15	dBrn
	—	—	12	dBrnC
TGC = 1	—	—	18	dBrn
	—	—	15	dBrnC
TGC = V_{SS}	—	—	16	dBrn
	—	—	14	dBrnC

Parameter	Limits			Unit
	Min	Typ	Max	
Idle channel noise:				
receive (D/A) measured at RFOUT				
RGC = 0 or 1	—	—	11	dBrn
	—	—	8	dBrnC
receive (D/A) referred to RPCM				
RGC = 0	—	—	11	dBrn
	—	—	8	dBrnC
RGC = 1	—	—	8	dBrn
	—	—	5	dBrnC
DC offset:				
transmit (A/D) measured at TPCM				
TGC = 0 or 1	—	—	±330	LSBs*
TGC = V_{SS}	—	—	±30	LSBs*
transmit (A/D) referred to TFIN				
TGC = V_{SS}	—	—	±5	mV
TGC = 1	—	—	±45	mV
TGC = 0	—	—	±32	mV
receive (D/A) measured at RFOUT				
RGC = 0 or 1	—	—	±140	mV
Power supply rejection ratio (PSRR) at 3140 Hz:				
transmit				
V_{DD}	30	—	—	dB
V_{SS}	33	—	—	dB
receive				
V_{DD}	30	—	—	dB
V_{SS}	33	—	—	dB
Absolute delay (end-to-end) at 1 kHz	—	—	575	μs

* Offset in A/D LSBs. The 15-bit A/D output is filled out to 16 bits by appending a 0 to the LSB. Multiply the offset (in LSBs) by two when referring to the full 16-bit word.

Analog Interface

TFIN: Rin > 1 MΩ and Cin < 10 pF, when TGC = logic 1 or 0
Rin > 1 MΩ and Cin < 80 pF, when TGC = V_{SS}
RFOUT: ac impedance < 300 Ω, max current 150 μA

Any input can be connected between V_{SS} and V_{DD} without damaging the chip.

Digital Interface

All inputs: TTL-compatible, Iin < 20 μA, < 5-pF loading
TPCM: Capable of driving a 50-pF capacitance to TTL voltage levels at 2.048 Mb/s

Any input can be connected between V_{SS} and V_{DD} without damaging the chip.

Table 2. Overload (1.02 kHz) Compression

Input/Overload Level	Minimum Output Relative to 0 dBm0 Input (dB)
–3.17 dB = 0.0 dBm0	Reference
0.0 dB = 3.17 dBm0	3.17 – 0.2 = 2.97
3.0 dB = 6.17 dBm0	6.17 – 1.8 = 4.37
6.0 dB = 9.17 dBm0	9.17 – 4.6 = 4.57

In the following tables and associated figures, the ac characteristics assume that the master clock (T2048, R2048) is 2.048 MHz ± 100 ppm.

Note: The filter responses scale linearly with master clock.

Table 3. Frequency Response Relative to Gain at 1.02 kHz*

Freq (Hz)	Transmit Loss (dB)	Receive Loss (dB)
50—60	≥20	±0.2
100	–0.2 to +7	±0.2
200	0.1 to 1.8	±0.2
300—3140	±0.125	±0.125
3200	–0.125 to +0.75	–0.125 to +0.75
3400	0.2 to 0.9	0.2 to 0.9
4000	>14	>14
4600 and above	>32	>28
3400—4600	$> 14 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - 1 \right]$	$> 14 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - 1 \right]$
4000—4600	$> 18 \left[\sin \left(\frac{\pi(4000 - f)}{1200} \right) - \frac{7}{9} \right]$	

* See Figures 5 through 9 for response curves.

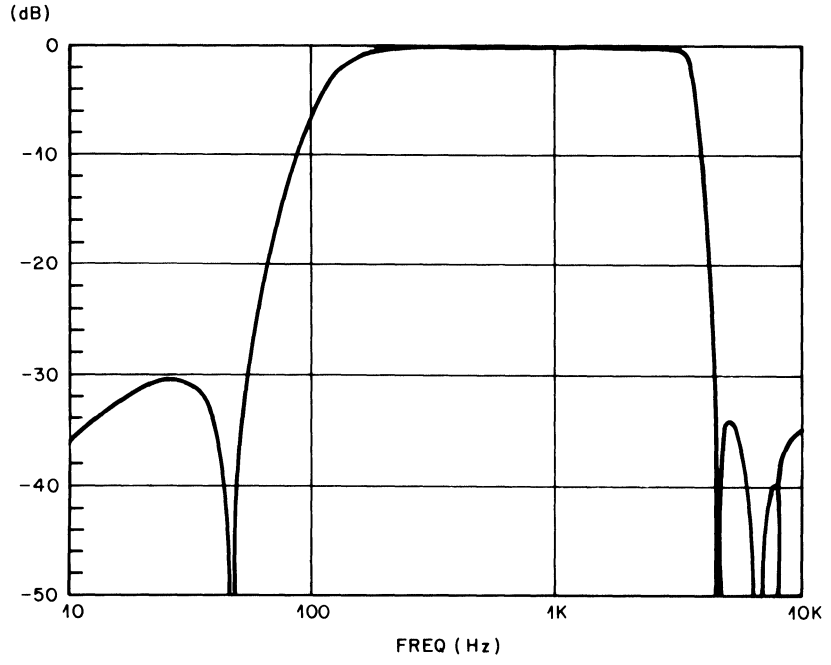


Figure 5. Transmit Path Frequency Response

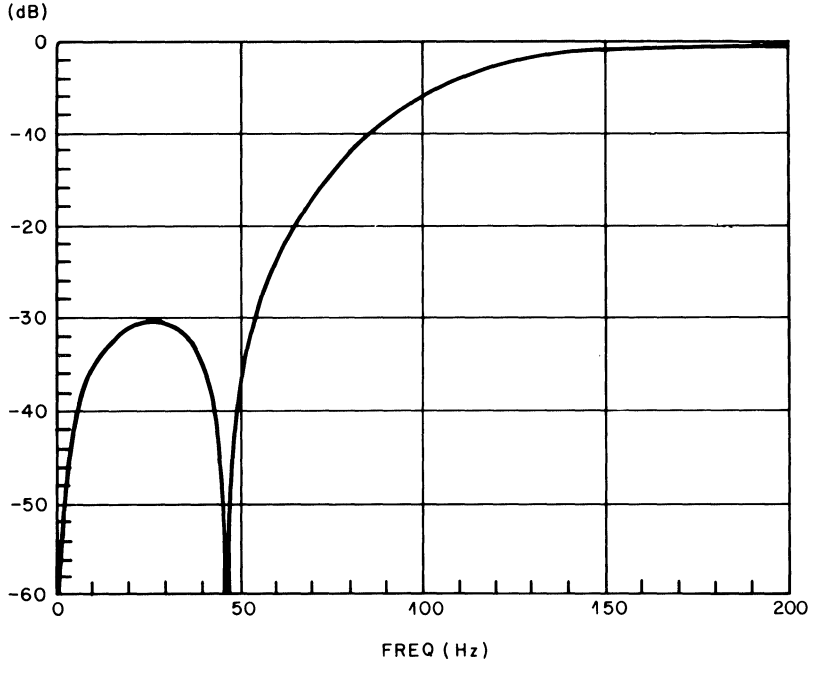


Figure 6. Transmit Path Low-Frequency Response

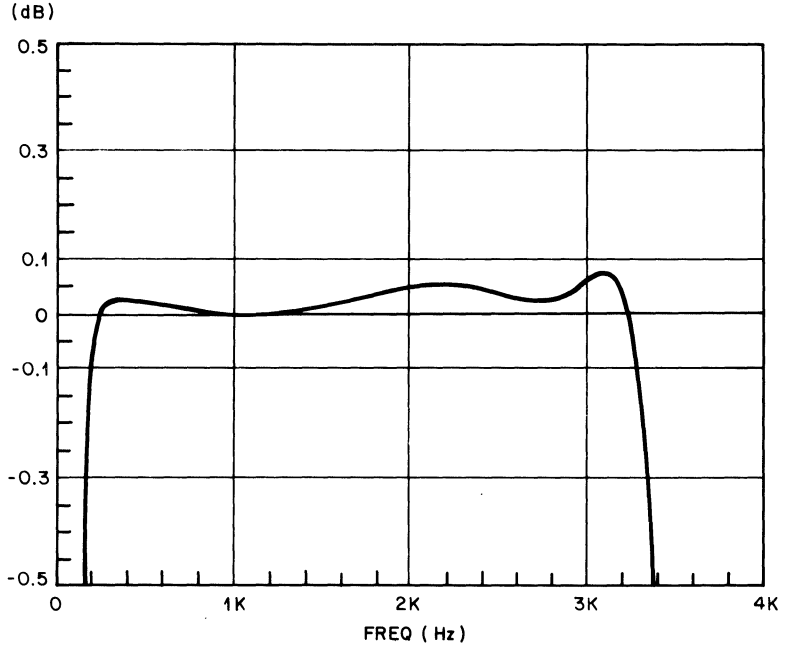


Figure 7. Transmit Path Voice Band Response

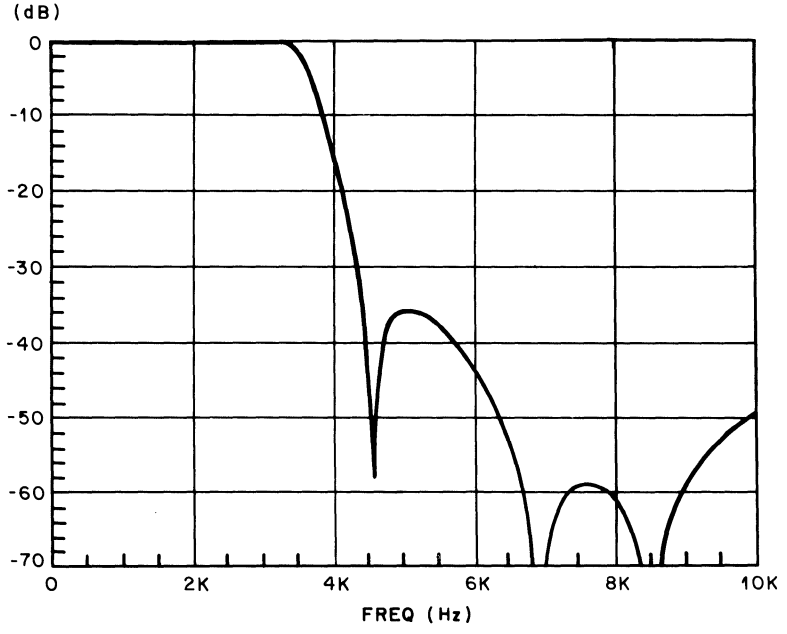


Figure 8. Receive Path Frequency Response

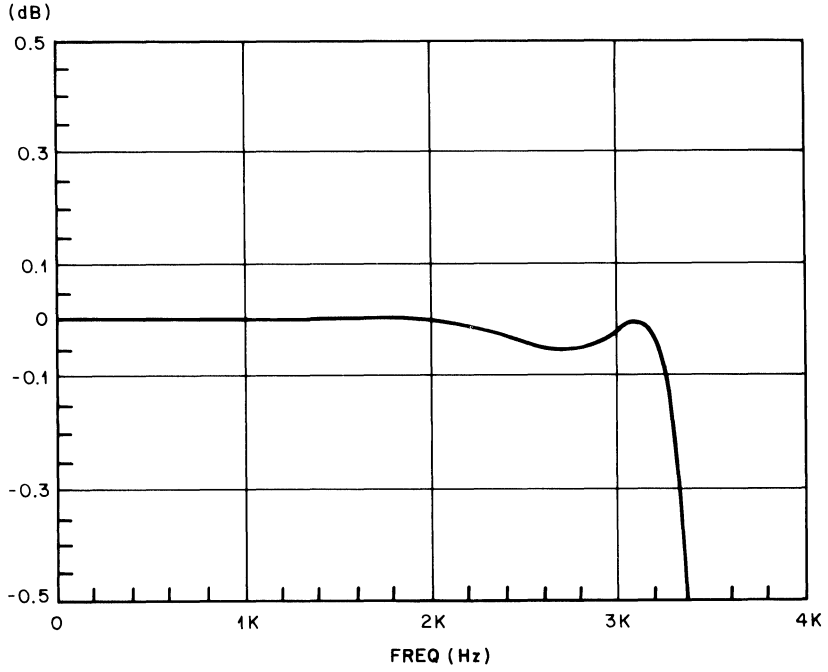


Figure 9. Receive Path Voice Band Response

Table 4. Phase and Delay Distortion (End-to-End)*

Freq (Hz)	Phase Deviation from Linearity (Radians)	Delay Distortion (μs, max)
Below 500	$-4.17 + 0.0046f \leq PD \leq 4.17 - 0.0046f$	—
500—700		300
700—2000	Between semicircles of radius 0.92 radians (1150 Hz) centered at ± 0.95 radians and 1850 Hz	75
2000—2500		150
2500—2700		200
2700—3000		375
3000 and above	$-11.65 + 0.0042f \leq PD \leq 11.65 - 0.0042f$	—

* See Figures 10, 11, and 12 for group delay curves.

Transmit←→Receive Crosstalk (200 Hz to 3400 Hz) < −75 dB

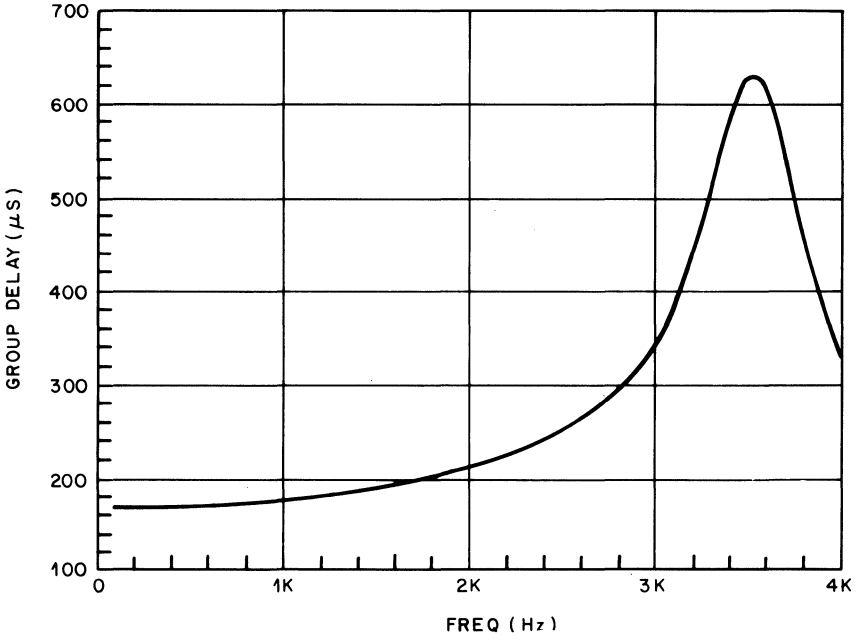


Figure 10. Receive Path Group Delay Response

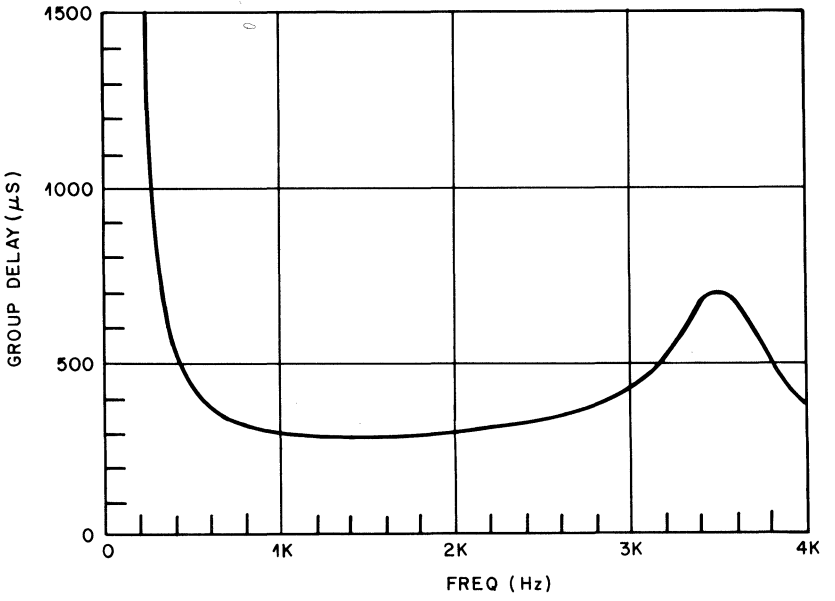


Figure 11. Transmit Path Group Delay Response

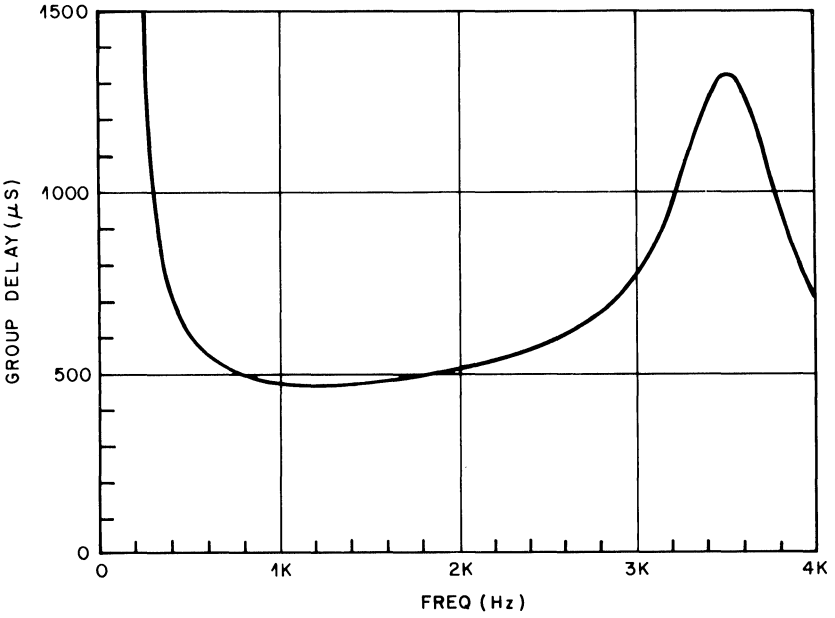
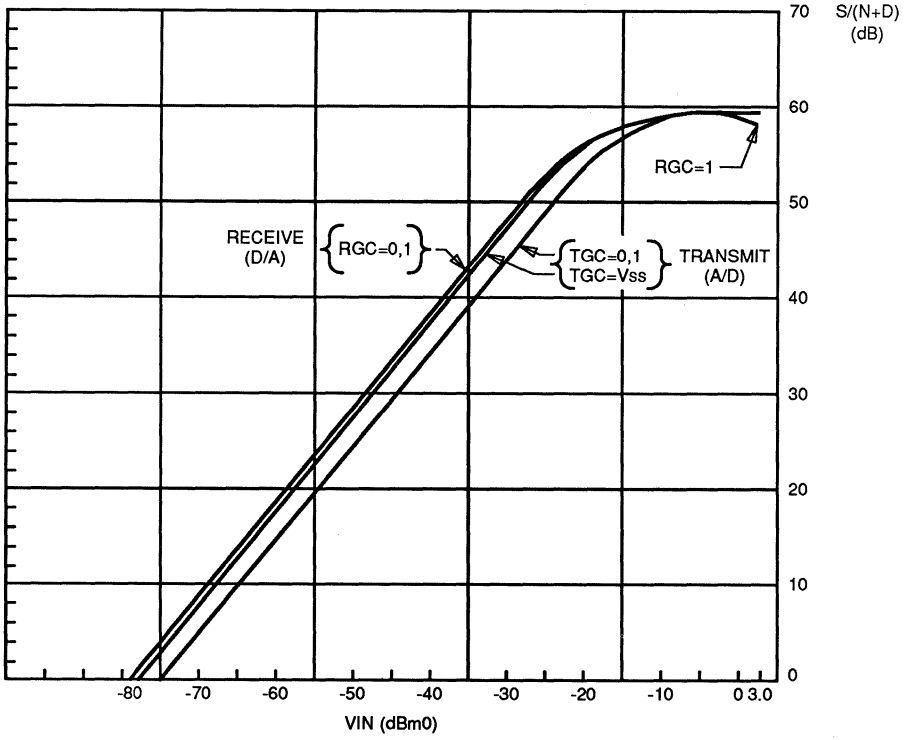


Figure 12. End-to-End Group Delay

Table 5. Single Frequency Distortion Measured at TPCM or RFOUT*

Digital Signal Level (TPCM, RPCM) (dBm0)	Input Frequency (Hz)	S/N+D (300-Hz to 3400-Hz Band)							
		Receive (D/A)				Transmit (A/D)			
		RGC = 0		RGC = 1		TGC = 0, 1		TGC = Vss	
		(dB)	(dBC)	(dB)	(dBC)	(dB)	(dBC)	(dB)	(dBC)
3	300 to 3400	60	60	55	55	60	60	60	60
0		60	60	59	59	60	60	60	60
–7		59	60	59	60	59	60	59	60
–17		58	59	58	59	56	57	57	58
–27		51	53	51	53	48	50	50	52
–37		42	44	42	44	38	40	41	43
–47		32	34	32	34	28	30	31	33

* See Figure 13 for S/N+D curves.



Note: Measured at TPCM for transmit (A/D) path, and at RFOUT for the receive (D/A) path.

Figure 13. Signal-to-Impairment Characteristic of the Transmit and Receive Paths

Transmit (Encoder)	Gain	Input Voltage at 1 kHz Corresponding to: Digital mW Out of TPCM	Overload (+3.174 dBm0)	Unit
TGC = 0	0 dB (reference)	1.095	1.578	Vp
TGC = 1	–3.00 dB ± 0.12 dB	1.547	2.229	Vp
TGC = Vss	–4.82 dB ± 0.20 dB	1.908	2.750	Vp

Receive (Decoder)	Gain	Output Voltage at 1 kHz Corresponding to: Digital mW Into RPCM	Overload (+3.174 dBm0)	Unit
RGC = 1	3.00 dB ± 0.12 dB	1.547	2.229	Vp
RGC = 0	0 dB (reference)	1.095	1.578	Vp

Timing Characteristics

The timing requirements are shown in Figure 14, with expanded details in Figure 15. The duty cycle of T2048 and R2048 must be between 45% and 55%. The encoder and decoder can operate back-to-back if RNSYNC = TNSYNC and R2048 = T2048.

Symbol	Parameter	Capacitance	Min	Max	Unit
tCKLSYL	Synchronization delay	—	10	tCLK – 75	ns
tCKLSYH	Synchronization hold	—	0*	*	ns
tCKHTPV	Transmit prop-delay	50 pF	0	140	ns
tRSVCKL	Receive set-up time	—	100	—	ns
tCKLRSX	Receive hold time	—	0	—	ns

* Each synchronization pulse should be low for a minimum of 1 clock cycle after timing edge A, with a maximum of 50% duty cycle. Note that the internal operation of the encoder or decoder is initiated by the first data clock edge that goes negative (timing edge A in Figure 14) after TNSYNC or RNSYNC has gone low.

Timing Diagrams

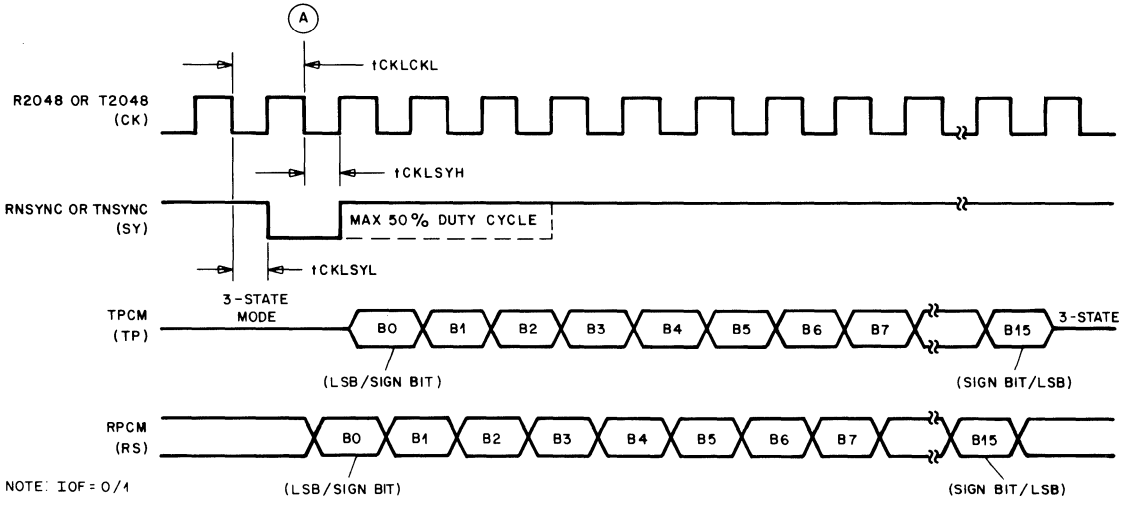


Figure 14. I/O Timing

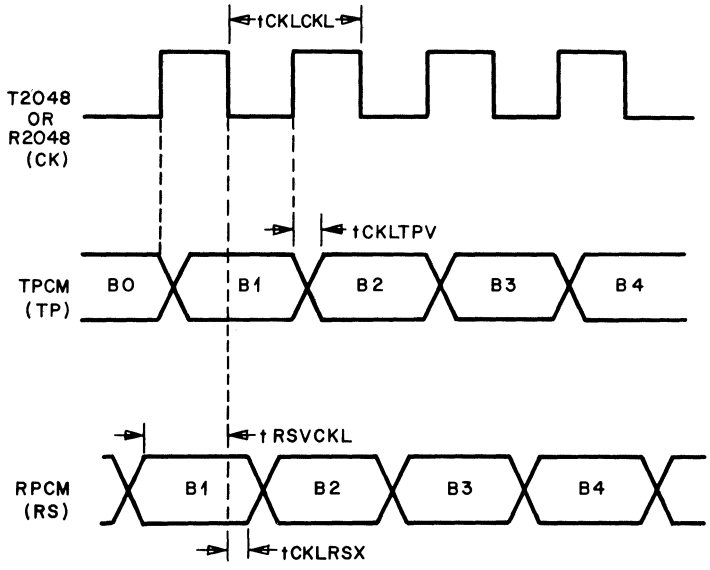


Figure 15. I/O Timing (Enlarged Section)

Custom Codecs

PCM codecs with filters for specific applications can be custom designed by the addition of analog and/or digital polycells to our basic codec chips. Custom codecs can be provided in a number of different device packages, which have already been designed and manufactured to meet the requirements of:

- *5ESS* Switching Equipment
- D5 Channel Banks
- *SLC* 96 Series 5 Carrier System

For information on how to obtain custom codecs to meet your system's particular requirements, contact your AT&T Account Manager or call:

1-800-372-2447.

3. Data Communications

T7000A Digital Encryption Processor

Features

- Programmable DES ciphering modes
  - Electronic codebook (ECB)
  - Cipher block chaining (CBC)
  - 1-, 8-, or 64-bit cipher feedback (CFB)
  - Output feedback (OFB)
- Ciphering rates of 235,000 operations/s for any of the DES modes.
- Data throughput of 1.882 Mbytes/s using 64-bit DES output block
- On-chip RAM and ROM program memory
- Flags readable on the data bus or independent output pins
- Four sets of key and initial value registers
- Separate plain text and cipher text parallel (8-bit) ports
- Separate plain text and cipher text serial ports
- Separate serial key input port
- ECB program available in ROM

Description

The T7000A Digital Encryption Processor (DEP) is a programmable integrated circuit that provides a low-cost, high-security, cryptographic system for encrypting and decrypting digital signals. It is manufactured using CMOS technology, requires a single 5 V supply, and is supplied in a 40-pin plastic DIP. It implements four data encryption standard (DES) modes and is capable of performing multiple encryption operations or multiplexed key and initial value ciphering.

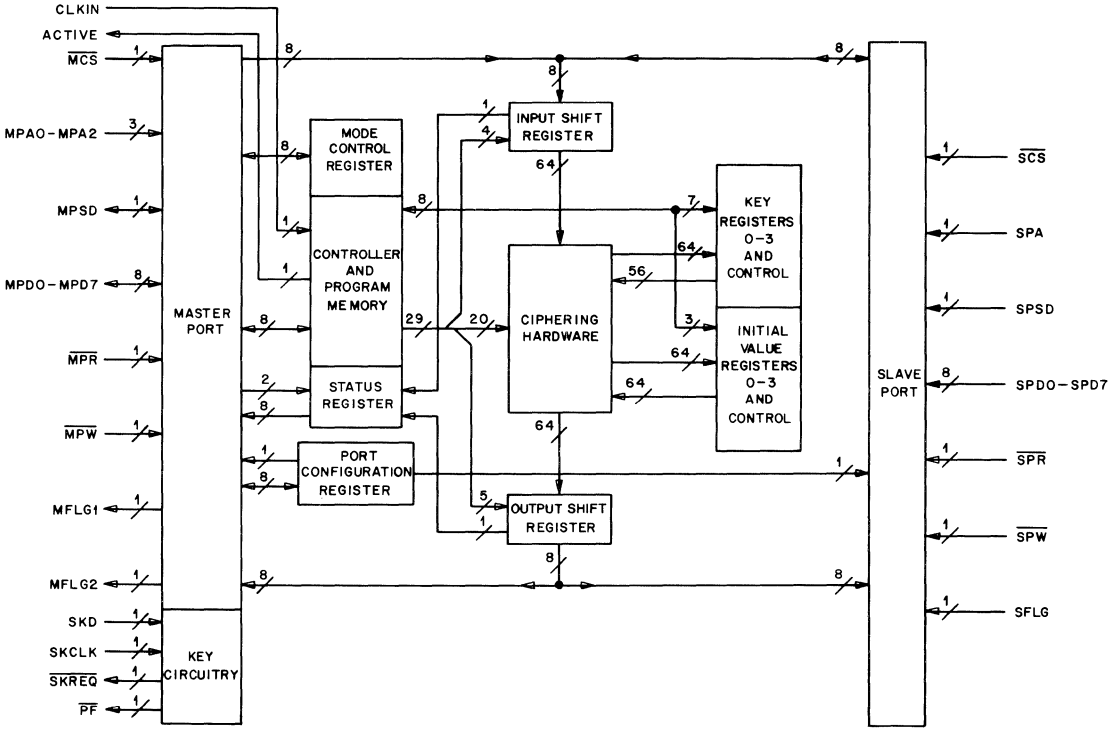
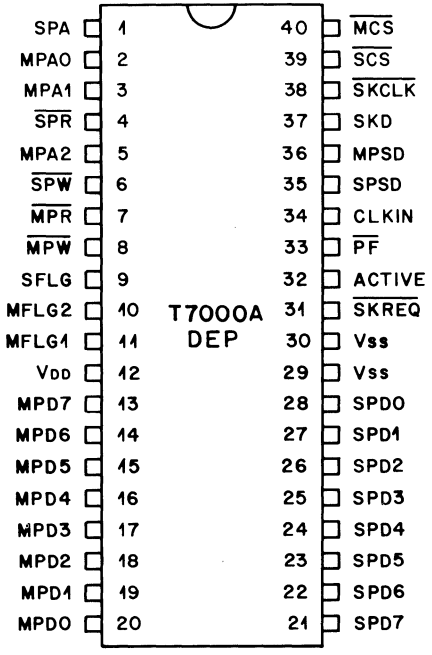


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
ACTIVE	32	SCS	39
CLKIN	34	SFLG	9
MCS	40	SKCLK	38
MFLG1	11	SKD	37
MFLG2	10	SKREQ	31
MPA0	2	SPA	1
MPA1	3	SPD0	28
MPA2	5	SPD1	27
MPD0	20	SPD2	26
MPD1	19	SPD3	25
MPD2	18	SPD4	24
MPD3	17	SPD5	23
MPD4	16	SPD6	22
MPD5	15	SPD7	21
MPD6	14	SPR	4
MPD7	13	SPSD	35
MPR	7	SPW	6
MPSD	36	VDD	12
MPW	8	Vss	29
PF	33	Vss	30

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	SPA	I	**Slave Port Address.** When high (1), the contents of the status register can be read, but not written, to the slave port data bus. When low (0), either the input shift register (ISR) or output shift register (OSR) is accessed, depending on the port configuration programmed.
2 3	MPA0 MPA1	I I	**Master Port Address Bits 0 and 1.** Used with MPA2 (pin 5) for internal register selection.
4	SPR	I	**Slave Port Read (Active Low).** Used with SPA (pin 1) to read from the output shift register (if the slave port is programmed as an output) or from the status register. Data is available on the slave port data bus following the falling edge of the read pulse and remains on the bus as long as SPR is low. SPW (pin 6) should be held high during the read pulse.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
5	MPA2	I	**Master Port Address Bit 2.** Used with MPA0 and MPA1 (pins 2 and 3) for internal register selection.
6	$\overline{\text{SPW}}$	I	**Slave Port Write (Active Low).** Used with SPA (pin 1) to write to the input shift register if the slave port has been programmed as an input. The data input is latched on the rising edge of the write pulse. $\overline{\text{SPR}}$ (pin 4) should be held high during the write pulse.
7	$\overline{\text{MPR}}$	I	**Master Port Read (Active Low).** Used with the master port address bus to read one of the internal registers. Data is available on the master port data bus following the falling edge of the read pulse and remains on the bus as long as $\overline{\text{MPR}}$ is low. $\overline{\text{MPW}}$ (pin 8) should be held high during the read pulse.
8	$\overline{\text{MPW}}$	I	**Master Port Write (Active Low).** This lead is used with the master port address bus to write to one of the internal registers. The data input is latched into the addressed register on the rising edge of the write pulse. The $\overline{\text{MPR}}$ lead should be held high during the write pulse.
9	SFLG	O	**Slave Flag.** This output indicates the status of either the input or output shift register, depending on the port configuration programmed (see Table 5). If the slave port is programmed as an input, the slave flag reflects the contents of the ISRFULL flag (status register, bit 4). If the slave port is programmed as an output, the slave flag reflects the contents of the OSREMPTY flag (status register, bit 5). Both of these conditions can be read from the status register.
10	MFLG2	O	**Master Flag 2.** This output indicates the status of the ISRFULL flag (status register, bit 4). This condition may also be read from the status register (see Table 5).
11	MFLG1	O	**Master Flag 1.** This output indicates the status of either the input or output shift register, depending on the port configuration programmed (see Table 5). If the master port is programmed as an input, this lead reflects the contents of the ISRFULL flag (status register, bit 4). If the master port is programmed as an output, this pin indicates the status of the OSREMPTY flag (status register, bit 5). If the master port is programmed as both input and output, this pin indicates the status of the OSRFULL flag and MFLG2 (pin 10) indicates the status of the ISRFULL flag. The status of the input and output shift register can also be read from the status register.
12	V_{DD}	—	**5 V Supply.**
13	MPD7	I/O	**Master Port Data Bit 7.** Bidirectional, 18-bit master port I/O bus.
14	MPD6		**Master Port Data Bit 6.**
15	MPD5		**Master Port Data Bit 5.**
16	MPD4		**Master Port Data Bit 4.**
17	MPD3		**Master Port Data Bit 3.**
18	MPD2		**Master Port Data Bit 2.**
19	MPD1		**Master Port Data Bit 1.**
20	MPD0		**Master Port Data Bit 0.**

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
21	SPD7	I/O	**Slave Port Data Bit 7.** Bidirectional, 8-bit slave port I/O bus.
22	SPD6		**Slave Port Data Bit 6.**
23	SPD5		**Slave Port Data Bit 5.**
24	SPD4		**Slave Port Data Bit 4.**
25	SPD3		**Slave Port Data Bit 3.**
26	SPD2		**Slave Port Data Bit 2.**
27	SPD1		**Slave Port Data Bit 1.**
28	SPD0		**Slave Port Data Bit 0.**
29	V_{SS}	—	**Ground.**
30	V_{SS}	—	**Ground.**
31	$\overline{SKREQ}$	O	**Serial Key Request (Active Low).** This output indicates that the DEP is expecting a key input. Active when IO SERIAL ACT is programmed. The condition of this flag can be read from the status register.
32	ACTIVE	O	**Active.** This output flag is set by the microcode instruction IO ACT.
33	$\overline{PF}$	O	**Parity Fail (Active Low).** When this output is low it indicates that one or more key input bytes had even parity. This flag is set on the 8th $\overline{MPW}$ pulse (pin 8) when the key is loaded through the parallel master port and on the 64th SKCLK pulse (pin 38) when the key is loaded serially. The status of this flag can be read from the status register.
34	CLKIN	I	**Clock Input.** The clock signal input at this lead determines all internal timing. A microcode instruction is executed every two clock cycles. The master and slave ports' read and write signals do not have to be synchronous with this clock signal. The frequency range of this clock is 10 kHz to 8 MHz.
35	SPSD	I/O	**Slave Port Serial Data.** Used to write data to the input shift register or read data from the output shift register, depending on the programmed port configuration. The first bit read or written is the most significant. When this port is selected by the port configuration register, slave port signals $\overline{SPW}$, $\overline{SPR}$, and SFLG (pins 6, 4, and 9) are used for control. This port cannot be used to read or write to any of the other six registers.
36	MPSD	I/O	**Master Port Serial Data.** Used to write data to the input shift register or read data from the output shift register, depending on the programmed port configuration. The first bit read or written is the most significant. When this port is selected by the port configuration register and master port address 0 is addressed, master port signals $\overline{MPW}$, $\overline{MPR}$, MFLG1, and MFLG2 (pins 8, 7, 11, and 10) are used for control.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
37	SKD	I	**Serial Key Data.** This input port is used to load key variables serially. The data on this pin is latched into key memory on the falling edge of the serial key clock during the execution of a serial load key program. The key is entered with the most significant bit first and every 8th bit is treated as an odd parity bit. A parity failure does not prevent the 56-bit key from being loaded.
38	SKCLK	I	**Serial Key Clock.** This clock is used to latch key data into key memory on the falling edge of the clock. The key input circuitry is inhibited after the 64th clock is received.
39	$\overline{SCS}$	I	**Slave Chip Select (Active Low).** This input enables the slave port inputs and outputs. When high, all slave port outputs are placed in a high-impedance state. The $\overline{SPW}$, $\overline{SPR}$, SPSD, and SPD0—SPD7 signals are affected.
40	$\overline{MCS}$	I	**Master Chip Select (Active Low).** This input enables the master port input and output leads. When high, all master port outputs are placed in a high-impedance state and all inputs are disabled. The $\overline{MPW}$, $\overline{MPR}$, MPSD, and MPD0—MPD7 signals are affected.

Overview

Figure 1 is a block diagram of the DEP device. There are three major sections: the ciphering hardware and peripheral circuitry, the controller and program memory, and the ports.

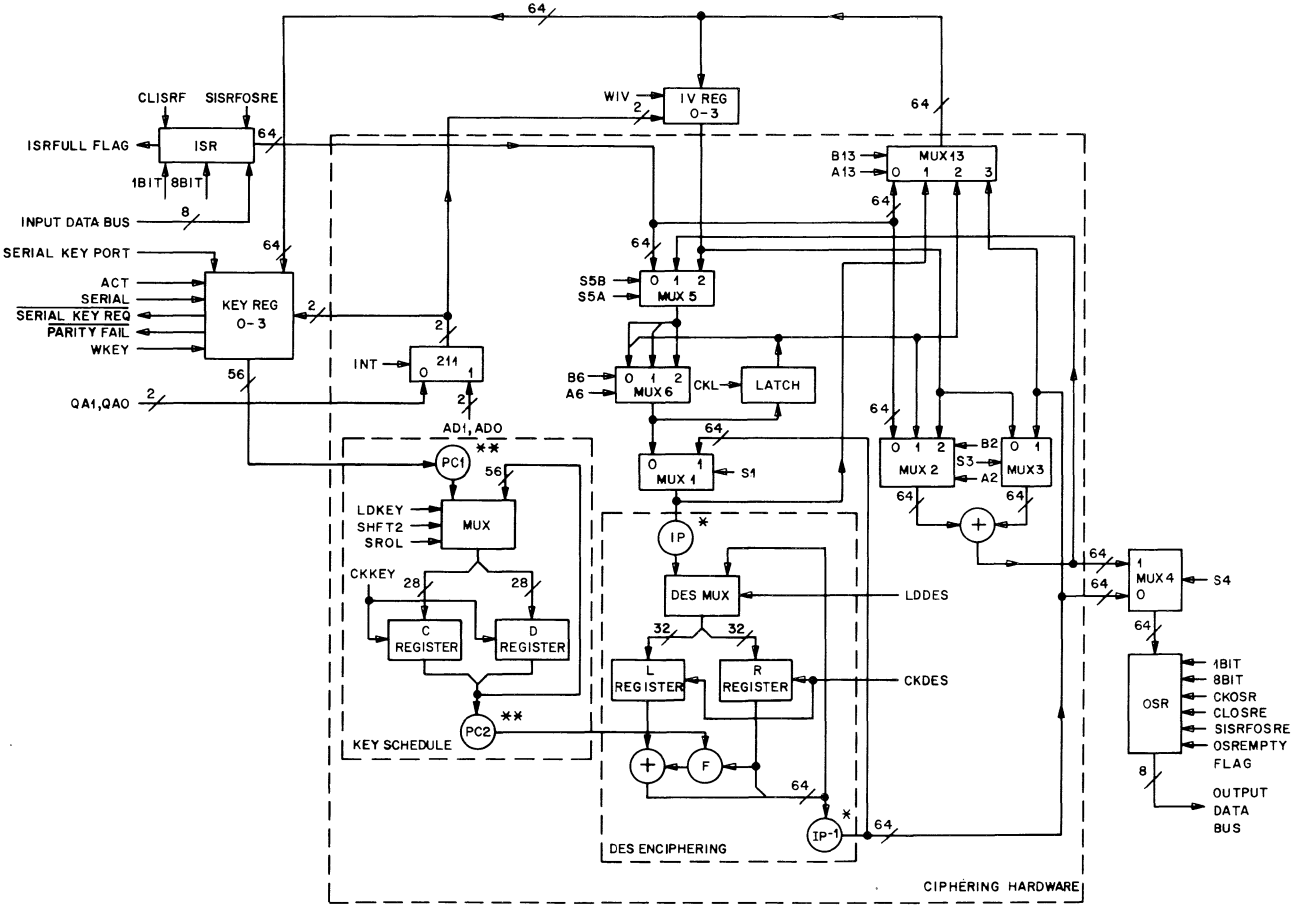
The ciphering hardware contains a high-speed hardware implementation of the National Bureau of Standards Data Encryption Algorithm (DEA) and the necessary hardware to configure the DES operating modes (see Figure 3). Both the key schedule and DES enciphering circuitry are part of the DEA algorithm. The remaining circuitry (seven multiplexers, an exclusive-OR gate, and a latch) is used for the DES operating modes. An input shift register, four key registers, four initial value registers, and an output shift register support the ciphering hardware.

An internal hardware controller executes a 22-bit machine instruction every two clock cycles, thereby setting up the ciphering multiplexers and clocking the appropriate registers. Within the controller, a program counter is used to address the machine instruction stored in either RAM or ROM program memory. On-chip ROM (29 X 22 bits) contains a subroutine controlling the DES hardware, a load initial value program, a load key program, a serial load key program, and an ECB encrypt and decrypt program. These short programs are located at hexadecimal address 00 through 1c (see Figure 5). User-accessible on-chip RAM (32 X 22 bits) allows the user to tailor the ciphering operation to meet system requirements and thus eliminates the need for external hardware. These ciphering programs must start at hex address 20 and cannot exceed hex address 3F.

Master and slave ports are provided so that the plain text and cipher text can be on separate buses. These ports have both serial and 8-bit parallel bidirectional data buses. When using the 8-bit parallel data bus, master or slave, the most significant data or key byte should be written/read first. In the serial mode, the most significant bit is written/read first.

Registers

Eight addressable internal registers control device operation. Table 2 shows the register assignments for both the master and slave ports during either a read or write operation.



* Initial Permutation.
** Permuted Choice.

Figure 3. Ciphering Hardware Block Diagram

Table 2. Register Assignments

Master Port (MP)		
Address	**Register**	**Size (Bytes)**
0 (write)	Input shift	8
0 (read)	Output shift	8
1 (read/write)	Status	1
2 (read/write)	Port configuration	1
3 (read/write)	Mode control	1
4 (read/write)	M1	1
5 (read/write)	M2	1
6 (read/write)	M3	1
Slave Port (SP)		
Address	**Register**	**Size (Bytes)**
0 (write)	Input shift	8
0 (read)	Output shift	8
1 (read)	Status	1

Input and Output Shift Registers. Both registers (master or slave port address 0) can be accessed from MPD, MPSD, SPD, or SPSD. The input shift register is a 64-bit, write-only, shift register. The output shift register is a 64-bit, read-only, shift register. The port configuration register controls which port, master or slave, is associated with the input or output shift register. These shift registers are used to input and output data and normally are not accessed until the other registers are loaded.

If a parallel port is used, 8 bytes are read or written to empty or load these registers, except when the 1- or 8-bit cipher feedback (CFB) mode has been programmed. In these cases, a single byte is expected. For 1-bit CFB, only the most significant bit of the byte is used.

If a serial port is used, 64 bits are read or written to empty or load these registers, except when the 1- or 8-bit CFB mode has been programmed. One bit is expected for 1-bit CFB and eight bits for 8-bit CFB.

Status Register. This register (master or slave port address 1) can be read or written from the master port data bus but only read from the slave port data bus (see Figure 4).

Bits 1 and 0 (QA1, QA0) are read/write address lines that are used to select key and initial value register pairs 0—3 when the microcode instruction bit, INT, is not set. Key and initial value registers are matched sets, e.g., 00 selects key register 0 and initial value register 0 (see Table 3). The values are loaded into these registers by executing the appropriate program in ROM.

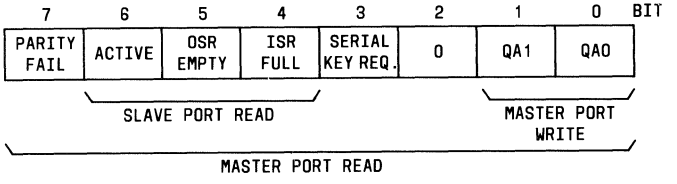


Figure 4. Status Register

Table 3. Key and Initial Value Register Addresses

Bits		Key and Initial Value Register Number
QA1	QA0	
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 of this register is not used.

Bit 3 is a read-only, active-high, serial key request (SKREQ) flag. The complement of this flag ($\overline{\text{SKREQ}}$) is available at output pin 31. SKREQ is microcode-controlled and goes active when the SERIAL and ACT instructions are executed simultaneously.

Bit 4 is a read-only, active-high, input shift register full (ISRFULL) flag. This flag appears on an output pin, the specific pin (MFLG1 , MFLG2 , or SFLG) being determined by the port configuration. An active signal indicates that the ISR is full and additional information written to that register will be ignored. The ISRFULL flag is set automatically whenever the mode control register is written or after the microcode instruction SISRFOSRE is executed. It is cleared by microcode instruction CLISRF.

Bit 5 is a read-only, active-high, output shift register empty (OSREMPTY) flag. This flag appears on an output pin, the specific pin (MFLG1 or SFLG) being determined by the port configuration. An active signal indicates that the OSR is empty and additional attempts to read that register will be ignored. OSREMPTY is set automatically whenever the mode control register is written or after the microcode instruction SISRFOSRE is executed. It is cleared by the microcode instruction CLOSRE.

Bit 6 is a read-only, active-high, activity (ACTIVE) flag. This flag appears on output pin 32 (ACTIVE). It is set by the microcode instruction IO ACT and indicates processor activity. The ACTIVE flag has no effect on device operation.

Bit 7 is a read-only, active-high, parity fail flag. The complement of this flag is available at output pin 33 ($\overline{\text{PF}}$). This flag is latched whenever the WKEY instruction is executed. An active condition indicates that one or more of the key bytes entered had even parity. Device operation is not inhibited by the parity fail flag.

Port Configuration Register. This register (master port address 2) is a read/write register accessible only through the master port data bus. Table 4 defines the possible port configurations and associated hex code for data encryption and decryption.

Table 4. Port Configuration (MP Address = 2)

Port Type	Input	Output	Hex Code*	
			Encrypt	Decrypt
Parallel	MPD	SPD	04	84
Parallel	SPD	MPD	11	91
Parallel	MPD	MPD	01	81
Serial	MPSD	SPSD	28	A8
Serial	SPSD	MPSD	62	E2
Parallel to serial	MPD	SPSD	08	88
Serial to parallel	SPSD	MPD	61	E1

* The most significant bit in the hex code for the port configuration is an input flag. It is tested by the microcode mnemonic LT?. In the microcode for the standard modes given in this document, this bit is tested to determine the order in which the DES key schedule should be used (encrypt or decrypt).

The conditions indicated by the master and slave port flags are determined by the port configuration (see Table 5).

Bit 7 of the port configuration register is an input flag that is tested by microcode instruction LT?. This bit can be used to indicate the order in which the key schedule is used (encrypt or decrypt) or as a general-purpose conditional jump.

Table 5. Master and Slave Port Flag Conditions

Port Configuration		Flag Condition		
Input	Output	MFLG1	MFLG2	SFLG
MPD or MPSD	SPD or SPSD	ISRFULL	—	OSREMPTY
SPD or SPSD	MPD or MPSD	OSREMPTY	—	ISRFULL
MPD	MPD	OSREMPTY	ISRFULL	—

Mode Control and M1, M2, and M3 Registers. The mode control register (master port address 3) is a read/write register accessible only through the master port data bus. This register is used to address on-chip memory for read/write operations and to begin program execution. Only the six least significant bits are used in this register.

To run a microcode program, write the starting address for the set of instructions to be executed into the mode control register. On the next instruction cycle, load this address into a program counter to begin execution.

To read/write the program memory, load the address of the instruction into the mode control register and read/write one of the three hex bytes (M1, M2, or M3) that make up an instruction on a subsequent $\overline{\text{MPR}}/\overline{\text{MPW}}$ pulse. Use the master port address bus to select M1, M2, or M3.

The M1, M2, and M3 registers (master port addresses 4—6, respectively) are accessible only through the master port data bus. These three bytes define a 22-bit microcode instruction stored in on-chip program memory. The two most significant bits of register M3 are not used.

Operation

It is important to use the following operating sequence with the DEP. Deviations from this sequence (e.g., loading the key before loading the ciphering program) may cause unpredictable results:

1. Load the ciphering program.
2. Configure the ports.
3. Load key and initial value register data.
4. Execute the program.

Loading the Ciphering Program. Microcode instructions can be entered for any of the DES mode programs (Figures 6—8), multiple programs, multiplexed programs, or the user's own unique cipher program. Thirty-two 22-bit instructions, starting at hex address 20, can be entered. Microcode instructions are loaded into RAM, a byte at a time, through the master port data bus to the address designated by the mode control register. The microcode address is written to the mode control register (MP address 3) and then followed by the three hex bytes (M1, M2, and M3). These three bytes (MP addresses 4—6, respectively) constitute a 22-bit instruction.

Configuring the Ports. Data flow, port selection, and the DES key schedule selection (encrypt and decrypt) are programmed by writing the appropriate hex code to the port configuration register (MP address 2). Table 4 shows the various port configuration options.

Loading Key and Initial Value Register Data. There are four key and initial value registers that must be externally loaded. A key/initial value register address is written to the status register (see Tables 2 and 3 and Figure 4) and the load initial value program or one of the two load key programs is executed. The following is a description of the load key and load initial value programs. The assembly language listings for these programs are shown in Figure 5.

After the starting address of the load initial value program (hex address 06) is written to the mode control register, the ISRFULL flag becomes inactive and the ACTIVE flag goes active. The eight initial value bytes can then be written to the input shift register through the master port data bus. After the eighth byte is written, the ISRFULL flag goes active and the content of the input shift register is copied to the addressed initial value register. The next internal machine instruction clears the ACTIVE flag.

After the starting address of the parallel load key program (hex address 0B) is written to the mode control register, the ISRFULL flag becomes inactive and the ACTIVE flag goes active. The eight key bytes can then be written to the input shift register through the master port data bus. After the eighth byte is written, the ISRFULL flag goes active and the content of the input shift register is copied to the addressed key register. Coincident with the program's WKEY instruction, the PARITY FAIL flag is set active high if any of the key bytes entered had even parity. The next internal machine instruction clears the ACTIVE flag.

After the starting address of the serial load key program (hex address 10) is written to the mode control register, the ACTIVE and serial key request (SKREQ) flags become active. The 64-bit key must then be clocked into the input shift register through the serial key port. After the last bit is entered, the content of the input shift register is copied into the addressed key register. One internal machine instruction cycle after the key is entered, the ACTIVE and SKREQ flags become inactive. Coincident with the program's WKEY instruction, the PARITY FAIL flag is set active high if any of the key bytes entered had even parity.

Executing the Program. After the microcode program is loaded, the desired port configuration is set up, and the key and initial value registers are loaded, the device is ready to begin a ciphering operation. The starting address of the microcode program is written to the mode control register. On the next internal machine cycle, this address is loaded into a program counter and execution begins. To execute the ECB mode, no microcode has to be loaded since it already exists in ROM. For this DES mode, step 1 should be omitted.

Input and output to the DEP device does not have to be synchronous with the input clock. The ISRFULL and OSREMPTY flags signal the host processor to write and read data. When these flags are

inactive, data can be loaded into the input shift register and read from the output shift register by the port associated with these registers. These flags, tested in program memory by conditional machine instructions, determine when to start or stop ciphering data. A typical ciphering program contains the following steps:

1. Multiplexer set-up
2. Wait for input data
3. DES subroutine call
4. Wait until previous output data has been read
5. Latch output data and return to step 2.

DES Mode Descriptions

The DEP is capable of performing all four DES operating modes: electronic codebook; cipher block chaining; 1-, 8-, or 64-bit cipher feedback; and output feedback. Code for the ECB mode is stored in ROM, beginning at location hexadecimal 12. The DEP can be programmed for the other modes via the RAM. Each mode can be used independently, combined with another mode, or used with multiple keys. For a detailed description of the DES modes refer to *Federal Information Processing Standards Publication 81*.

Electronic Codebook (ECB) Mode. This mode is used primarily to encrypt or decrypt keys or initial values through the use of a master key. It is a direct implementation of the DES algorithm. A 64-bit input data block results in a 64-bit output block. Consecutive data blocks are cryptographically independent. Figure 5b contains the assembly language listing for the ECB mode, beginning at hexadecimal address 12.

Cipher Block Chaining (CBC) Mode. This mode uses the DES algorithm in a 64-bit feedback mode, which results in consecutive output data blocks being cryptographically dependent. This dependence provides an error-extension characteristic useful in protecting against an active system attack. Figure 6 contains the assembly language listing for the CBC mode.

Cipher Feedback (CFB) Mode. This mode is an additive stream cipher in which the DES algorithm is used to generate pseudorandom blocks. This mode provides cryptographic dependence of data blocks and error-extension. It is not necessary for the input block to be 64 bits; it may be 1, 8, or 64 bits. If the 1- or 8-bit mode is selected, a DES operation must be performed for every input bit or byte; consequently, the data rate is reduced by a factor of 64 or 8, respectively. Figure 7 contains the assembly language listings for 1-, 8-, and 64-bit CFB modes.

Output Feedback (OFB) Mode. This mode uses the DES algorithm as a pseudorandom number generator. Encryption and decryption are identical operations, and the security of the algorithm is dependent on the proper management of the initial value blocks. This mode has no error-extension property: a 1-bit transmission error results in a 1-bit decryption error. This is an important property when transmitting over a noisy channel. Figure 8 contains the assembly language listing for the OFB mode.

These standard DES modes, after set-up, can be executed in a minimum of 17 instructions. With an 8-MHz input clock, the instruction period is 250 ns, yielding a maximum of 235,000 ciphering operations/s. If the entire output block (all 64 bits) is used, the data throughput rate is 1.882 Mbytes/s.

Multiple encryption can be easily implemented with the DEP device. By using different keys, any of the previously mentioned DES modes can be cascaded to provide multiple encryption.

Figure 9 contains the assembly language listing for the ECB mode using 3 keys for encryption and decryption. Decryption is similar to encryption except that the key schedules are used in reverse order, e.g., the last key register used for encrypting is used first for decrypting.

In addition to using the four DES operating modes, the multiple modes, and the multiplexed modes, the user can choose to program a unique encryption method.

Figure 5b contains an assembly language listing (in ROM) for the ECB DES mode. Figures 6—9 contain assembly language listings for three DES modes and multiple-key ECB. Each listing in Figures 6—9 begins at RAM hexadecimal address 20. When combining programs, program labels may have to be changed to prevent incorrect addressing. Duplicate code in some programs can be combined.

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
DES Subroutine				
0	c2	1f	0	:00 LDDES CKDES CKKEY
1	42	10	5	:01 CKDES CKKEY LLC 5
2	52	11	2	:02 CKDES SHFT2 CKKEY ILC 02
3	42	10	5	CKDES CKKEY LLC 5
4	52	11	4	:03 CKDES SHFT2 CKKEY ILC 03
5	42	13	0	CKDES CKKEY RET 0
Load Initial Value				
6	1	b	3	B6 IO LDMP ACT DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
7	1	1a	0	CLISRF ADD
8	0	15	8	:10 ISRFT? 10
9	0	3c	0	WIV CLEAR
a	0	14	a	:20 GTO 20
Parallel Load Key				
b	1	b	3	B6 IO LDMP ACT DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
c	1	1a	0	:25 CLISRF ADD
d	0	15	d	:30 ISRFT? 30
e	8	1c	0	WKEY CLEAR
f	0	14	f	:40 GTO 40
Serial Load Key				
10	1	b	7	B6 IO LDMP SERIAL ACT DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
11	0	14	c	GTO 25

Figure 5a. ROM Programs

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
ECB Encrypt or Decrypt				
12	1	c	0	B6 CLEAR DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
13	7	18	15	LDKEY CKKEY CLISRF LT? 100
14	2	19	1	CKKEY SROL SHFTR
15	0	15	15	:100 ISRFT? 100
16	c3	12	1	CLISRF LDDES CKDES CKKEY SUB 01
17	0	17	1a	ISRFOSRET? 120
18	0	16	18	:110 OSRET? 110
19	0	d4	15	CLOSRE CKOSR GTO 100
1a	c3	d2	1	:120 CLISRF CLOSRE CKOSR LDDES CKDES CKKEY SUB 01
1b	0	17	1a	:130 ISRFOSRET? 120
1c	0	14	18	GTO 110

Figure 5b. ROM Programs

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
CBC Encrypt				
20	3	c	0	S5A B6 CLEAR DES INPUT = ISR^IV OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR^IV
21	7	18	23	LDKEY CKKEY CLISRF LT? 200
22	2	19	1	CKKEY SROL SHFTR
23	0	15	23	:200 ISRFT? 200
24	c3	12	1	CLISRF LDDES CKDES CKKEY SUB 01
25	13	4	2c	:210 S3 S5A B6 GTO 130 DES INPUT = ISR^DESOUT OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR^DESOUT
26	0	15	26	:100 ISRFT? 100
27	c3	12	1	CLISRF LDDES CKDES CKKEY SUB 01
28	0	17	2b	ISRFOSRET? 120
29	0	16	29	:110 OSRET? 110
2a	0	d4	26	CLOSRE CKOSR GTO 100
2b	c3	d2	1	:120 CLISRF CLOSRE CKOSR LDDES CKDES CKKEY SUB 01
2c	0	17	2b	:130 ISRFOSRET? 120
2d	0	14	29	GTO 110
CBC Decrypt				
2e	7	1c	0	LDKEY CKKEY CLISRF CLEAR
2f	59	48	31	B2 S3 S4 B6 B13 LT? 250 DES INPUT = ISR OSR INPUT = IV^DESOUT IV INPUT = Qn LATCH INPUT = ISR
30	2	19	1	CKKEY SROL SHFTR
31	0	15	31	:250 ISRFT? 250
32	e3	12	1	CLISRF CKL LDDES CKDES CKKEY SUB 01
33	0	17	36	ISRFOSRET? 230
34	0	16	34	:220 OSRET? 220
35	0	f4	31	CLOSRE CKOSR WIV GTO 250
36	e3	f2	1	:230 CLISRF CKL WIV CLOSRE CKOSR LDDES CKDES CKKEY SUB 01
37	0	17	36	ISRFOSRET? 230
38	0	14	34	GTO 220

Figure 6. Assembly Language Listing for CBC Mode

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
64-bit CFB Encrypt				
20	1d	c	0	S3 S4 S5B B6 CLEAR DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
21	7	12	0	LDKEY CKKEY CLISRF SUB 00
22	1b	4	24	S3 S4 S5A B6 GTO 102 DES INPUT = ISR^DESOUT OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = ISR^DESOUT
23	e3	d2	1	:101 LDDES CKDES CKL CKKEY CLISRF CLOSRE CKOSR SUB 01
24	0	17	23	:102 ISRFOSRET? 101
25	0	14	24	GTO 102
64-bit CFB Decrypt				
26	1d	c	0	S3 S4 S5B B6 CLEAR DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
27	7	12	0	LDKEY CKKEY CLISRF SUB 00
28	19	4	24	S3 S4 B6 GTO 102 DES INPUT = ISR OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = ISR
8-bit CFB Encrypt				
29	1d	b	10	S3 S4 S5B B6 IO 8BIT DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
2a	27	12	0	CKL LDKEY CKKEY CLISRF SUB 00
2b	1a	84	24	S3 S4 S5A A6 GTO 102 DES INPUT = Qn<<8 | | ISR^DESOUT OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<8 | | ISR^DESOUT

Figure 7a. Assembly Language Listing for 1-, 8-, and 64-Bit CFB Modes

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
8-bit CFB Decrypt				
2c	1d	b	10	S3 S4 S5B B6 IO 8BIT DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
2d	27	12	0	CKL LDKEY CKKEY CLISRF SUB 00
2e	18	84	24	S3 S4 A6 GTO 102 DES INPUT = Qn<<8 | | ISR OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<8 | | ISR
1-bit CFB Encrypt				
2f	1d	b	8	S3 S4 S5B B6 IO 1BIT DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
30	27	12	0	CKL LDKEY CKKEY CLISRF SUB 00
31	1a	4	24	S3 S4 S5A GTO 102 DES INPUT = Qn<<1 | | ISR^DESOUT OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<1 | | ISR^DESOUT
1-bit CFB Decrypt				
32	1d	b	8	S3 S4 S5B B6 IO 1BIT DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
33	27	12	0	CKL LDKEY CKKEY CLISRF SUB 00
34	18	4	24	S3 S4 GTO 102 DES INPUT = Qn<<1 | | ISR OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<1 | | ISR

Figure 7b. Assembly Language Listing for 1-, 8-, and 64-Bit CFB Modes

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
OFB Encrypt and Decrypt				
20	1d	c	0	S3 S4 S5B B6 CLEAR DES INPUT = IV OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = IV
21	7	12	0	LDKEY CKKEY CLISRF SUB 00
22	98	4	24	S1 S3 S4 GTO 102 DES INPUT = DESOUT OSR INPUT = ISR^DESOUT IV INPUT = ISR LATCH INPUT = Qn<<1 | | ISR
23	e3	d2	1	:101 LDDES CKDES CKL CKKEY CLISRF CLOSRE CKOSR SUB 01
24	0	17	23	:102 ISRFOSRET? 101
25	0	14	24	GTO 102

Figure 8. Assembly Language Listing for OFB Mode

ADDRESS	22-Bit Instruction M1	M2	M3	Program Mnemonics
Subroutine for ECB with 3 Keys				
20	0	19	0	:20 SROL SHFTL
21	c6	18	24	LDDES CKDES LDKEY CKKEY LT? 25
22	2	1f	0	CKKEY
23	0	19	1	SROL SHFTR
24	2	14	1	:25 CKKEY GTO 01
3 Key ECB Encrypt				
/*				
25	1	1c	0	CLISRF CLEAR
26	1	a	1	:100 B6 ADD INT DES INPUT = ISR OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
27	0	15	27	:110 ISRFT? 110
28	1	12	20	CLISRF SUB 20
29	81	a	3	B6 S1 ADD INT ADD0 DES INPUT = DESOUT OSR INPUT = DESOUT IV INPUT = ISR LATCH INPUT = ISR
2a	0	12	20	SUB 20
2b	0	1a	5	ADD INT ADD1
2c	0	12	20	SUB 20
2d	0	16	2d	:140 OSRET? 140
2e	0	d4	26	CLOSRE CKOSR GTO 100

Figure 9a. Assembly Language Listing for the ECB Mode Using 3 Keys

3 Key ECB Decrypt

```
2f   1  1c   0   CLISRF CLEAR
30   1   a   5   :200 B6 ADD INT ADD1
                   DES INPUT = ISR    OSR INPUT = DESOUT
                   IV INPUT = ISR     LATCH INPUT = ISR
31   0  15  31   :210 ISRFT? 210
32   1  12  20   CLISRF SUB 20
33  81   a   3   B6 S1 ADD INT ADD0
                   DES INPUT = DESOUT    OSR INPUT = DESOUT
                   IV INPUT = ISR     LATCH INPUT = ISR
34   0  12  20   SUB 20
35   0  1a   1   ADD INT
36   0  12  20   SUB 20
37   0  16  37   :240 OSRET? 240
38   0  d4  30   CLOSRE CKOSR GTO 200
```

Figure 9b. Assembly Language Listing for the ECB Mode Using 3 Keys

Instruction Set

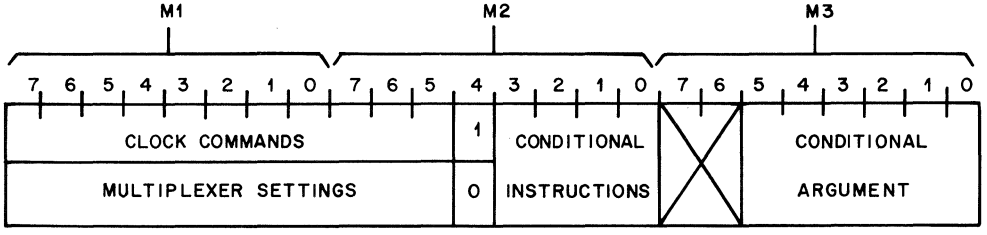


Figure 10. 22-Bit Instruction Diagram

Bytes M1, M2, and M3 constitute a 22-bit instruction. Bit 4 of byte M2 determines which set of instructions are used in bits 0—7 of byte M1 and bits 5—7 of byte M2. If bit 4 of byte M2 is high, the clock command instructions are used. If this bit is low, the multiplexer setting instructions are used.

Bits 0—3 of byte M2 are decoded to one of thirteen conditional instructions. With the exception of RET and CLEAR, these instructions use the third byte, M3, as an argument. A description of each instruction is given in Table 6.

The timing diagram for the instruction set is shown in Figure 14. An instruction is executed every two clock cycles. The ciphering rate can be computed by multiplying the number of instructions in the ciphering operation by twice the CLKIN period.

Table 6. Instruction Set — Clock Commands and Multiplexer Settings

Clock Commands (M2, Bit 4 = 1)			
Byte	**Bit**	**Mnemonic**	**Description**
M1	7	LDDES	Enables the DES multiplexer to receive the output from MUX 1 when high or from the DES itself when low.
M1	6	CKDES	Clocks the DES L and R registers.
M1	5	CKL	Clocks the latch register.
M1	4	SHFT2	Enables the key circuitry to rotate 2 positions when high and 1 position when low.
M1	3	WKEY	Latches the key register currently addressed.
M1	2	LDKEY	Enables the key schedule C and D registers to be loaded from the addressed key register when high. When low, the contents of the C and D registers can be rotated 1 or 2 positions, left or right, depending on the state of the instructions SHFT2, SROL, and CKKEY. These two registers are used in the key schedule generation for the DES algorithm.
M1	1	CKKEY	Clocks the key schedule C and D registers.
M1	0	CLISRF	Clears the ISRFULL flag and allows data to be written into the ISR.
M2	7	CLOSRE	Clears the OSREMPTY flag and allows data to be read from the OSR.
M2	6	CKOSR	Clocks the output from MUX 4 into the OSR.
M2	5	WIV	Writes the output of MUX 13 into the initial value memory.
Multiplexer Settings (M2, Bit 4 = 0)			
M1	7	S1	Selects the input line for MUX 1. A low selects input line 0; a high selects input line 1.
M1 M1	6 5	B2 A2	Selects the input line for MUX 2: **B2 A2 Input Line** 0 0 0 0 1 1 1 0 2 1 1 Illegal An error occurs if both B2 and A2 are high.
M1	4	S3	Selects the input line for MUX 3. A low selects input line 0; a high selects input line 1.
M1	3	S4	Selects the input line for MUX 4. A low selects input line 0; a high selects input line 1.
M1 M1	2 1	S5B S5A	Selects the input line for MUX 5: **S5B S5A Input Line** 0 0 0 0 1 1 1 0 2 1 1 Illegal An error occurs if both S5B and S5A are high.

Table 6. Instruction Set — Clock Commands and Multiplexer Settings (Continued)

Multiplexer Settings (M2, Bit 4 = 0) (Continued)			
Byte	**Bit**	**Mnemonic**	**Description**
M1 M2	0 7	B6 A6	Selects the input line for MUX 6: **B6 A6 Input Line** 0 0 0 0 1 1 1 0 2 1 1 Illegal An error occurs if both B6 and A6 are high.
M2 M2	6 5	B13 A13	Selects the input line for MUX 13: **B13 A13 Input Line** 0 0 0 0 1 1 1 0 2 1 1 3

Table 7. Instruction Set — Conditional Instructions

M2 Bits					
3	**2**	**1**	**0**	**Mnemonic**	**Description**
0	0	0	0	LLC	Loads the loop counter with the least significant nibble in M3. There is only one loop counter.
0	0	0	1	ILC	Decrements the loop counter and jumps to the address in M3 if the loop counter is not 0.
0	0	1	0	SUB	The current program counter instruction address is incremented and latched before the program jumps to the address specified by M3. Only one level of subroutine call is allowed.
0	0	1	1	RET	Return from subroutine. The program jumps to the address latched when the preceding SUB command is executed.
0	1	0	0	GTO	The program jumps to the address in M3.
0	1	0	1	ISRFT?	If the ISR is not full, the program jumps to the address specified by M3.
0	1	1	0	OSRET?	If the OSR is not empty, the program jumps to the address specified by M3.
0	1	1	1	ISRFOSRET?	If the ISR is full and the OSR is empty, the program jumps to the address specified by M3.
1	0	0	0	LT?	If bit 7 of the port configuration register is low, the program jumps to the instruction address in M3. This bit can be used to select the order in which the key schedule is used (encrypt or decrypt).

Table 7. Instruction Set — Conditional Instructions (Continued)

M2 Bits							
3	2	1	0	Mnemonic	M3 Bit	Mnemonic	Description
1	1	1	1	UI	—	—	Unconditional increment to next instruction.
1	1	0	1	—	—	—	Not used.
1	1	1	0	—	—	—	Not used.
1	0	0	1	SROL	0 = 1	SHFTR	Latches a right-key schedule rotation.
					0 = 0	SHFTL	Latches a left-key schedule rotation.
1	0	1	0	ADD	2 1	ADD1 ADD0	Latches the key/initial value register address: **ADD1 ADD0 Reg Pair** 0 0 0 0 1 1 1 0 2 1 1 3
					0	INT	A high specifies the internal key/initial value address bus; a low specifies the key/initial value address specified by bits 0 and 1 of the status register.
1	0	1	1	IO	5	SISRFOSRE	A high sets both the ISRFULL flag and the OSREMPTY flag active.
					4 3	8BIT 1BIT	Selects 1-, 8-, or 64-bit CFB mode: **1-Bit 8-Bit CFB Mode** 0 0 64-bit 0 1 8-bit 1 0 1-bit 1 1 Illegal
					2	SERIAL	Sets the key circuitry for a serial key input when high and parallel key input when low.
					1	LDMP	A high sets the input circuitry to receive data from the master port regardless of the conditions programmed in the port configuration register.
					0	ACT	A high sets both the ACTIVE flag in the status register and output pin 32.
1	1	0	0	CLEAR	NA	NA	Initializes control logic in the DEP. Specifically, this instruction clears the following bits: ACT, LDMP, SERIAL, 1BIT, 8BIT, INT, ADD0, ADD1, SHFTL, SHFTR. This instruction is typically used in the first line of a program.

NA = not applicable.

Characteristics

Clocks

CLKIN: 10 kHz to 8 MHz
SKCLK: 10 kHz to 1.6 MHz

On-Chip Memory

ROM: 29 X 22 bits (hex address 00—1C)
RAM: 32 X 22 bits (hex address 20—3F)

ROM Address Map	
Address	**Program**
00	DES hardware subroutine
06	Load initial value
0B	Parallel load key
10	Serial load key
12	ECB encrypt or decrypt

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply current	I_{DD}	—	—	90	mA	0 °C, V_{DD} = 5.5 V
Input voltage:						
low	V_{IL}	—	—	0.8	V	—
high	V_{IH}	2.0	—	—	V	—
Output voltage:						
low	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
high	V_{OH}	2.4	—	—	V	I_{OH} = 400 μA
Power dissipation	PD	—	0.3	0.5	W	0 °C, V_{DD} = 5.5 V
		—	—	0.4	W	70 °C, V_{DD} = 5.5 V

Maximum Ratings

Voltage (V_{SS}) range on any pin with respect to ground .....–0.5 to V_{DD} + 0.5 V
Storage temperature (Tstg) range .....–65 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Max	Unit
tAVRL	Address set-up time (read)	70	—	ns
tAVWL	Address set-up time (write)	70	—	ns
tCLKINHCLKINH	CLKIN period	0.125	100	μs
tDVWH	Data valid to write pulse rising edge	80	—	ns
tPCHPCH	Instruction period	2tCLKINHCLKINH	—	ns
tRHDX	Read pulse to data bus float	—	80	ns
tRHFLGH	Last read pulse to rising $\overline{\text{MFLG}}$ or $\overline{\text{SFLG}}$	—	80	ns
tRHRH	$\overline{\text{MPR}}$ or $\overline{\text{SPR}}$ period	2tCLKINHCLKINH	—	ns
tRLDV	Read pulse to data valid	—	70	ns
tSKCLKHSKCLKH	SKCLK period	0.625	—	μs
tSKCLKLSKDX	Serial key data hold time	70	—	ns
tSKCLKLSKREQH	Last falling serial key clock to rising serial key request	—	4tCLKINHCLKINH + tWHFLGH	ns
tSKDVSKCLKL	Serial key data set-up time	70	—	ns
tSKREQLSKCLKL	Serial key request to first falling serial key clock	4tCLKINHCLKINH	—	ns
tWHDX	Write pulse data hold	15	—	ns
tWHFLGH	Last write pulse to rising $\overline{\text{MFLG}}$ or $\overline{\text{SFLG}}$	—	60	ns
tWHWH	$\overline{\text{MPW}}$ or $\overline{\text{SPW}}$ period	2tCLKINHCLKINH	—	ns

Timing Diagram Nomenclature

Term	Definition	Term	Definition	Term	Definition
ADR	Address	M1D	M1 data	PD	Port data
CD	Cipher data	M2D	M2 data	SD	Status data
MD	Mode data	M3D	M3 data	UD	Unciphered data (plain text)

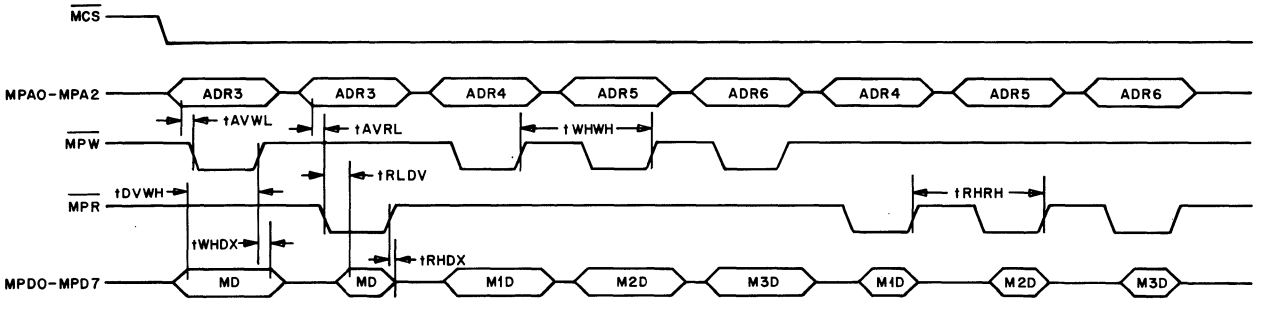


Figure 11. Memory Load Timing

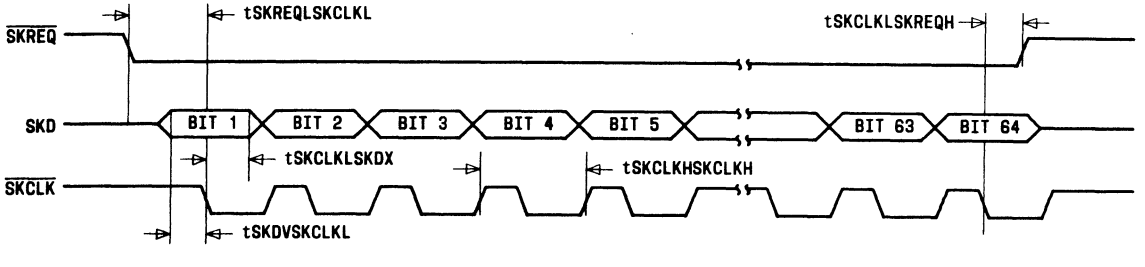
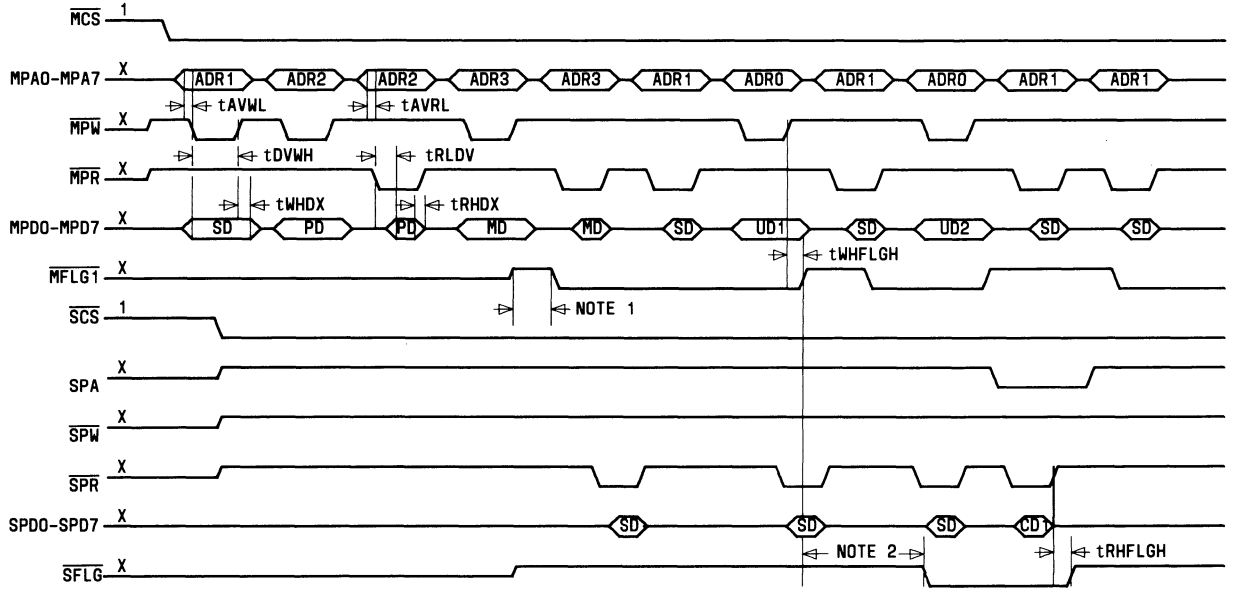


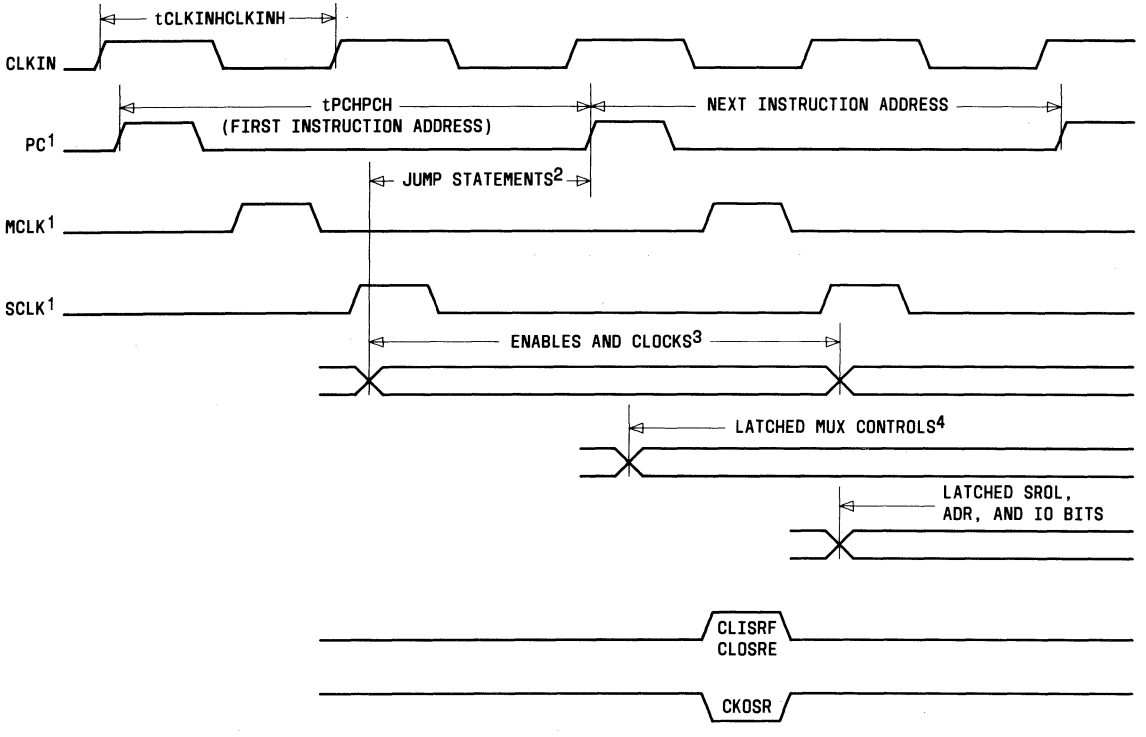
Figure 12. Serial Key Timing



Notes:

[1] This time is determined by the number of program instructions executed before instruction CLISRF.
[2] This time is determined by the number of program instructions executed between the time MFLG1 goes high and instruction CLOSRE executes (ciphering algorithm time).

Figure 13. 8-bit CFB Mode Timing with the Master Port Configured for Input and the Slave Port as an Output



Notes:

1 PC (Program Counter), MCLK, and SCLK are internal nonoverlapping clocks generated from CLKIN.
2 LLC, ILC, SUB, RET, GTO, ISRFT?, OSRET?, ISRFOSRET?, LT?
3 LDDES, CKDES, CKL, SHFT2, WKEY, LDKEY, CKKEY, WIV.
4 S1, A2, B2, S3, S4, S5A, S5B, A6, B6, A13, B13.

Figure 14. Internal Machine Instruction Timing

T7001 Random Number Generator

Features

- On-chip or external high-frequency oscillator source option
- On-chip or external jitter oscillator source option
- Generation of a 536-bit random number available in 8-bit bytes
- Internal verification of RNG output on the data bus
- Data ready and alarm output flags readable from the data bus or independent output pins, allowing either processor interrupt or processor polled configuration
- Internal 4-bit statistical "run-up" test with programmable limits (elementary randomness check)
- External access to generated statistics

Description

The T7001 Random Number Generator (RNG) integrated circuit produces random bits based on the phase jitter of a free-running oscillator. The output data stream is truly random, not pseudo-random. The T7001 RNG is processed in CMOS technology, requires a single 5 V supply, and is supplied in a 32-pin plastic DIP.

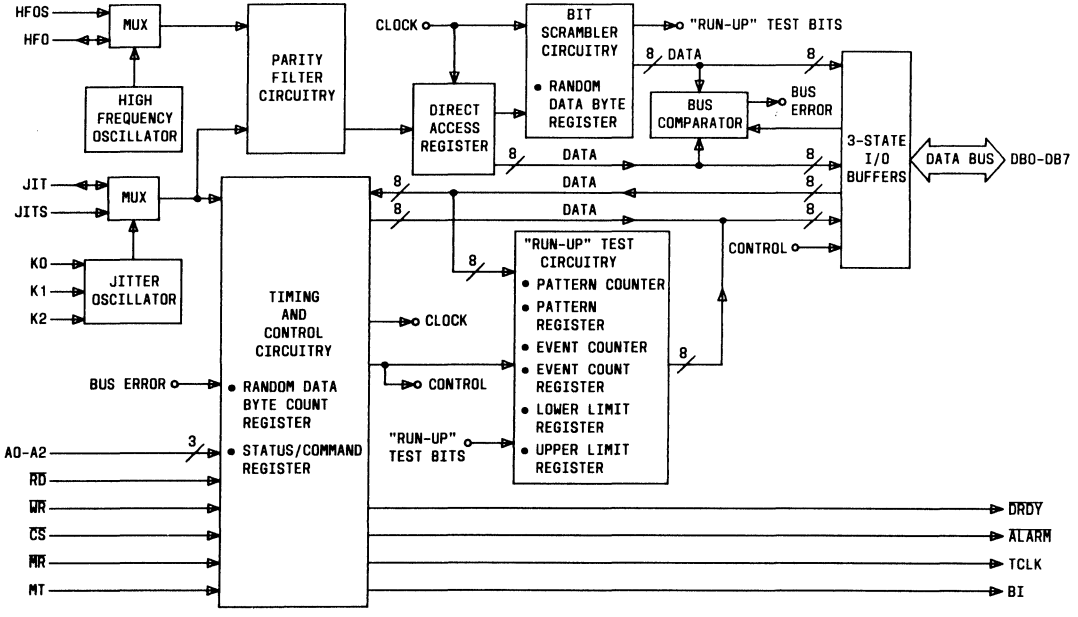
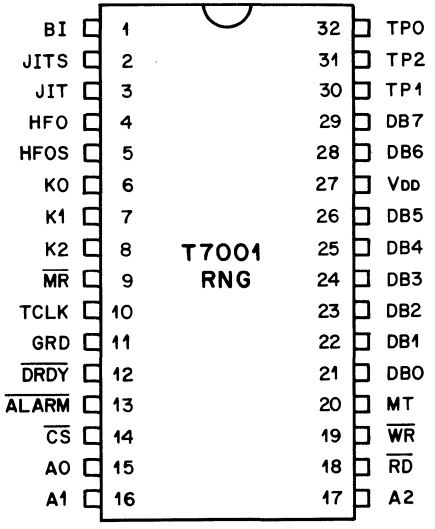


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
A0	15	HFO	4
A1	16	HFOS	5
A2	17	JIT	3
ALARM	13	JITS	2
BI	1	K0	6
CS	14	K1	7
DB0	21	K2	8
DB1	22	MR	9
DB2	23	MT	20
DB3	24	RD	18
DB4	25	TCLK	10
DB5	26	TP0	30
DB6	28	TP1	31
DB7	29	TP2	32
DRDY	12	VDD	27
GRD	11	WR	19

Figure 2. Pin Function Diagram and Alphabetical List of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	BI	O	**Test Pin.** Output of the positive edge triggered sampling D-type flip-flop, which has the high-frequency oscillator (HFO) as its data input and the jitter oscillator (JIT) as its clock. It may be used to verify that both HFO and JIT are working properly.
2	JITS	I	**Jitter Select.** Determines the jitter signal source for the device. When low (0), the internal jitter oscillator is used. When high (1), an external jitter oscillator signal is expected at JIT (pin 3).
3	JIT	I/O	**Jitter.** Output of the internal jitter oscillator when JITS (pin 2) is low. When JITS is high, this pin is an input for an external jitter oscillator.
4	HFO	I/O	**High-Frequency Oscillator.** Output of the internal high-frequency oscillator when HFOS (pin 5) is low. This pin is the input for an external high-frequency oscillator signal when HFOS is high.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
5	HFOS	I	**High-Frequency Oscillator Select.** Determines the high-frequency signal source for the device. When low, the internal high-frequency oscillator (8 MHz) is selected. When high, an external oscillator signal is expected at HFO (pin 4).
6 7 8	K0 K1 K2	I	**On-Chip Jitter Oscillator Frequency Control.** A resistor (R) is connected between K0 and K1 and a capacitor (C) is connected between K0 and K2 to control the frequency of the on-chip jitter oscillator. The approximate frequency is determined by the equation: $f = \frac{1}{2.2\ RC}$
9	$\overline{MR}$	I	**Master Reset.** This active-low input resets the device when $\overline{CS}$ (pin 14) is active. A master reset puts the command bits in the status/command register in the inactive state and clears the random data-byte, event count, and random data-byte count registers. The pattern lower-limit and upper-limit registers are unaffected by a master reset.
10	TCLK	O	**Test Clock.** This output is used with the direct access register to monitor the random data byte at the input to the 536-bit shift register. Random data is latched into the register on the rising edge of TCLK (pin 10) and can be read after this edge. When the internal random bit generator (with jitter oscillator set to 1 kHz) is used, the TCLK period is approximately 32 ms. When a different oscillator frequency or an external random-bit generator is used, the TCLK period is computed by multiplying the JIT input (pin 2) period by 32.
11	GRD	—	**Ground.**
12	$\overline{DRDY}$	O	**Data Ready.** This active-low flag indicates that the "run-up" test was passed and that a 67-byte random number is stored in the random data-byte register. This flag may also be read from the status/command register. The $\overline{DRDY}$ flag goes inactive following the 67th $\overline{RD}$ pulse (pin 18) if the random data-byte register (address 0) is addressed.
13	$\overline{ALARM}$	O	**Alarm.** This active-low flag indicates either a "run-up" test failure or a bus error. Both of these conditions may be read from the status/command register. This flag can be cleared only by a master reset.
14	$\overline{CS}$	I	**Chip Select.** This active-low input enables $\overline{RD}$ (pin 18), $\overline{WR}$ (pin 19), $\overline{MR}$ (pin 9), and the address bits (pins 15, 16, and 17). When inactive, the data bus output buffers are held in a high-impedance state regardless of the state of any other input.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
15 16 17	A0 A1 A2	I	**Address Bus Bit 0.** **Address Bus Bit 1.** **Address Bus Bit 2.**
18	$\overline{RD}$	I	**Read.** This active-low input is used to read one of the eight internal registers. Data appears on the data bus following the falling edge of this signal and remains on the bus as long as $\overline{RD}$ is low. $\overline{WR}$ (pin 19) should be held high (inactive) during a read operation.
19	$\overline{WR}$	I	**Write.** This active-low input is used to write to one of three internal registers. The data is latched into the addressed register on the rising edge of the write pulse. $\overline{RD}$ (pin 18) should be held high (inactive) during a write operation.
20	MT	I	**Manufacture Test.** This pin must be grounded for device operation.
21 22 23 24 25 26	DB0 DB1 DB2 DB3 DB4 DB5	I/O	**Data Bus Bit 0.** **Data Bus Bit 1.** **Data Bus Bit 2.** Bidirectional **Data Bus Bit 3.** 3-state I/O leads. **Data Bus Bit 4.** **Data Bus Bit 5.**
27	V_{DD}	—	**5 V Supply.**
28 29	DB6 DB7	I/O	**Data Bus Bit 6.** Bidirectional **Data Bus Bit 7.** 3-state I/O leads.
30 31 32	TP0 TP1 TP2	—	**Manufacture Test Point.** No connection.

Overview

Random bits are generated in a positive edge triggered D-type flip-flop via the sampling of a high-frequency square wave by a pulse stream with a relatively high randomly varying period (low randomly varying frequency). This flip-flop is part of the parity filter circuitry shown in Figure 1. Groups of samples from the D-type flip-flop are fed through a parity filter, the output from which is fed into a bit scrambler. The bit scrambler receives these bits, performs exclusive-OR operations with previous bits, and sends the results to the random data-byte register.

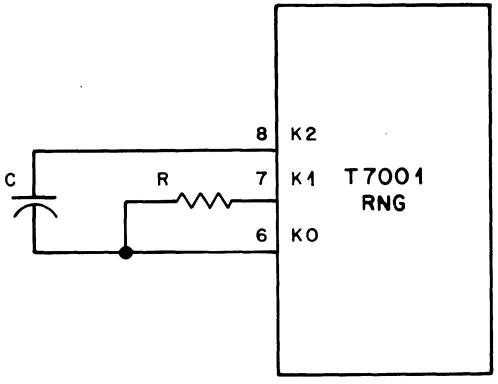
The sources of both the high-frequency and the jitter (low frequency) signals are user-selectable. HFOS (pin 5) determines the high-frequency signal source. A low on this pin selects the internal 8-MHz oscillator and configures HFO (pin 4) as an output for monitoring the signal. A high on HFOS configures HFO as an input pin for an externally generated high-frequency signal. In critical applications, it is recommended that an externally generated high-frequency signal be used. Weak coupling or interaction between the low-frequency clock signal and the internal 8-MHz oscillator has been observed and this may affect the randomness of the number produced. The use of an external high-frequency square-wave oscillator, preferably crystal-controlled, substantially reduces any possibility of coupling.

JITS (pin 2) determines the source of the jitter oscillator signal. A low on this pin selects the internal jitter oscillator and configures JIT as an output for monitoring the signal. The frequency of this oscillator is determined by an RC network at K0, K1, and K2. The equation for calculating the approximate frequency is:

$$f = \frac{1}{2.2\ RC}$$

where R must be $\geq$ 2 kΩ.

A high on the JITS pin configures JIT (pin 3) as an input for an externally generated signal. Figure 3 shows the RC network connections.



R = Resistor value in kΩ.
C = Capacitor value in μF.

Figure 3. RC Network

A "run-up" test compares (1000 times) the last four bits in the random data-byte register with a 4-bit pattern. If the number of times these two patterns match is outside the upper and lower limits programmed by the user during device initialization, the test fails and an alarm condition results. The result of this test (the number of times the patterns matched) can be read from the event counter register.

The random data byte register is a 536-bit (67- byte) shift register. After the random number is generated, the register is read a byte at a time, using one read pulse per byte (67 read pulses).

During a read of the random data-byte register, the external bus data is compared with the register data. If there is any discrepancy, a bus error results and device operation is halted. The bus error flag state may be read from the status/command register or the output $\overline{\text{ALARM}}$ pin. This error indicates a hardware failure, improper device operation, or a bus contention problem.

Data ready ($\overline{\text{DRDY}}$) and alarm output flags are readable from either the data bus or independent output pins. This feature allows configuration of either processor interrupt or processor polled systems.

Registers

There are eight addressable registers. Five are read-only registers and three are read/write registers. Table 2 contains the register assignments for the RNG.

Table 2. Register Assignments

Address		Register	Size (Bits)
0	(read)	Random data byte	536
1	(read/write)	Status/command	8
2	(read)	Event count	8
3	(read)	Pattern	4
4	(read/write)	Lower limit	8
5	(read/write)	Upper limit	8
6	(read)	Random data-byte counter	8
7	(read)	Direct access	8

Random Data-Byte Register (Address 0). This read-only shift register stores the random number. Sixty-seven $\overline{RD}$ pulses are used to read the random number. The device remains inactive until all 67 bytes are read or until a master reset is issued.

Status/Command Register (Address 1). This read/write register (see Figure 4) must be written before certain device operations can begin.

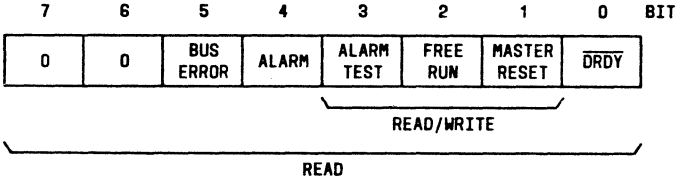


Figure 4. Status/Command Register

Bit 0 is a read-only, active-low, data ready flag is used to indicate that a run-up test has passed and that a 67-byte random number is stored in the random data-byte register. This flag remains active until all 67 random data bytes have been read, a bus error is detected, or a master reset is issued. This information is also available on output $\overline{DRDY}$.

Bit 1 is a read/write, active-high, master reset command. When active, a master reset condition exists until this bit is cleared by a low pulse on the external $\overline{MR}$ or by writing a 0 to this bit.

Bit 2 is a read/write, active-high, free-run command. In the inactive state, the device executes a single run-up test and halts operation. If the test passes, the $\overline{DRDY}$ flag goes active and all 67 random data bytes must be read (or a master reset issued) before a second run-up test begins.

If bit 2 is active (set), the device continually executes run-up tests. The $\overline{DRDY}$ flag goes active after the first run-up test passes and remains active until a failure occurs. Although it is a bad practice, data can be read from the random data-byte register continuously during run-up tests. To maximize randomness, data should be read only when the $\overline{DRDY}$ flag is active. When the first $\overline{RD}$ pulse accesses the random data-byte register, the current run-up test halts. After the 67th $\overline{RD}$ pulse, the run-up tests start again. Bit 2 can be set at any time during device operation. An external master reset ($\overline{MR}$) pulse clears bit 2, but an internal master reset (bit 1) has no affect.

Bit 3 is a read/write, active-high, alarm test command (ALRMT). If active, a known sequence of 0s and 1s is automatically loaded into the random data-byte register, producing known event counts for the run-up test. The generated counts are given in Table 3. This test is used to check the run-up and alarm circuitry or to produce a known pattern in the random data-byte register that can be read if desired. These run-up test counts and random data-byte patterns (see Table 3) are not user-selectable.

In order for this test to operate correctly, the device must first be cleared by using the internal master reset command (set bit 1). Then, on a subsequent write cycle, the internal master reset command bit must be cleared simultaneously with the setting of the alarm test bit, i.e., writing the hexadecimal sequence 0A, 08 to the status/command register. Bit 3 is cleared by an external master reset. Internal master reset has no effect.

Table 3. Alarm Test Register Data

Pattern (Hex)	Event Count (Hex)	Random Data-Byte Register					
		Byte Number	Byte (Hex)	Byte Number	Byte (Hex)	Byte Number	Byte (Hex)
0	A0	1	71	24	A1	47	B0
1	21	2	F0	25	C8	48	E0
2	4E	3	EC	26	73	49	A1
3	25	4	A1	27	B0	50	C9
4	55	5	58	28	E8	51	61
5	3B	6	73	29	A1	52	B0
6	15	7	F0	30	C8	53	A2
7	4E	8	EC	31	73	54	A1
8	28	9	A1	32	B0	55	C9
9	52	10	58	33	E0	56	61
A	42	11	73	34	A1	57	B0
B	38	12	F0	35	C8	58	A2
C	1D	13	E8	36	73	59	A1
D	3F	14	A1	37	B0	60	C9
E	47	15	58	38	E0	61	41
F	2A	16	73	39	A1	62	B0
		17	B0	40	C8	63	A2
		18	E8	41	61	64	A9
		19	A1	42	B0	65	C9
		20	58	43	E0	66	41
		21	73	44	A1	67	B0
		22	B0	45	C9		
		23	E8	46	61		

Bit 4 is a read-only, active-high, alarm flag. The complement of this flag is available at $\overline{\text{ALARM}}$ (pin 13). An active alarm flag indicates that either a run-up test has failed or that a bus error has been detected. This flag can be cleared only by a master reset.

Bit 5 is a read-only, active-high, bus error flag. It becomes active if there is a discrepancy between the data in the random data byte register and the data appearing externally on the eight-bit bidirectional data bus during a random data-byte read operation. An active bus error flag causes $\overline{\text{ALARM}}$ to go low and bit 4 of the command/status register to go high. This condition can be cleared only by a master reset.

Bits 6 and 7 are always low and are unused.

Event Count Register (Address 2). This read-only register stores the hex event count from the most recently completed run-up test. It is an 8-bit register with a maximum displayable count of 255 (hex FF). A reading of less than 255 indicates the actual event count obtained during the last run-up test; a reading of 255 indicates an event count of 255 or more. This register is cleared by a master reset.

Pattern Register (Address 3). This read-only register stores the 4-bit hex pattern associated with the most recently completed run-up test. A pattern counter is incremented at the completion of every successful run-up test. If the run-up test fails, the pattern counter is not changed and the test is repeated following a master reset. A master reset does not affect this counter or the pattern register (address 3). The counter assumes an arbitrary state during power-up and increments from there.

Lower-Limit Register (Address 4). This read/write register stores the hex lower limit associated with the run-up test and must be written before proper operation of the device can begin.

Upper-Limit Register (Address 5). This read/write register stores the hex upper limit associated with the run-up test and must be written before proper operation of the device can begin.

Random Data-Byte Counter Register (Address 6). This read-only down counter register keeps track of the number of random bytes left in the random data-byte register. Following an active data ready signal, this register is preset to hex 43 (decimal 67). After the 67 random data bytes have been read, this register is at hex 0 and remains there until the next active data ready signal.

Direct Access Register (Address 7). This read-only register, in conjunction with TCLK, allows the user to continually monitor the random data byte at the input to the 536-bit shift register. The random data is latched into this register on the rising edge of the TCLK signal and can be read after this edge.

Data read from this register has not been subjected to the bit scrambler and may have high bit-to-bit correlation. Thus, this data should not be used in place of data obtained from the random data-byte register, but should be used only for device monitoring and/or testing.

Operation

The upper- and lower-limit registers and the status/command register, which control device operation, must be written by the host processor before proper operation begins. Figure 6 shows the timing of a basic write cycle.

After the controlling processor has initialized the T7001 device, random number generation is initiated by an external $\overline{MR}$ pulse. Random bits are then generated and fill the 536-bit (67-byte) random data-byte register. Following the initial fill, a run-up test is executed.

During a run-up test, the last four bits in the random data-byte register are compared to the contents of a 4-bit pattern counter. If the bit patterns match, the event count register is incremented. At the end of 1000 non-overlapping, 4-bit tests on a fixed pattern, the result accumulated in the event counter is compared to the contents of the upper- and lower-limit registers. If the event count is outside the stored limits, the test fails. It takes approximately 18 seconds to execute a run-up test if the low-frequency jitter oscillator is set to 1 kHz. If a different frequency is used, the testing time may be computed by multiplying the jitter oscillator period by 18160.

If the random bits are independent, with P(1) = P(0) = 0.5, the probability of any 4-bit pattern is 0.0625 and the expected event count for 1000 samples is 62.5. The event count has a binomial distribution with a standard deviation of 7.65. Using the normal approximation to the binomial distribution, the probability of a test failing can readily be computed. For example, if the limits are set at plus or minus twice the standard deviation, the probability of the test failing is 0.0456 (taken from the table of values for the Standard Normal Distribution Function). At plus or minus three times the standard deviation, the probability of the test failing is 0.0026. The upper and lower limits are stored as binary numbers in the upper- and lower-limit registers. Since the upper- and lower-limit registers are eight bits in length, the largest value that can be stored in the upper-limit register is hexadecimal FF, while the smallest number that can be stored in the lower-limit register is hexadecimal 00. If these maximum and minimum values are used for the upper and lower limits of the run-up test, the test is inoperative, i.e., the test never fails.

If the run-up test is inoperative, there is no automatic warning or check of device malfunction such as high-frequency oscillator failure. Low-frequency oscillator failure is detected by cessation of device operation since that oscillator is used to clock the entire device. Detection of high-frequency oscillator failure occurs only when the run-up test is operative. If a run-up test is initiated with a master reset and the high-frequency oscillator is stuck either high or low, the event count register contains either hexadecimal FF or 00 at the end of the test. Thus, if the upper- and lower-limit registers were set to hexadecimal FE and 01, respectively, the run-up test would fail. The chance of a fully operational device failing under these conditions is $1 - 6.22 \times 10^{-16}$. Thus, in order to be warned of device malfunction, the run-up test should always be kept operative. If, for some reason, the user wants to make the test inoperative, it is best to set the run-up test upper and lower limits to FE and 01, respectively. These limits effectively remove the run-up test but maintain the warning of gross malfunction, i.e., high-frequency oscillator failure.

If the run-up test passes, the $\overline{\text{DRDY}}$ flag goes active and the host processor can address the random data-byte register to read the 67 bytes. Figure 8 shows the timing required for successive random data-byte read cycles to completely empty the random data-byte register. At the end of the 67th read pulse, the device begins generating the next 67-byte random number. If the run-up test fails, the $\overline{\text{DRDY}}$ flag remains inactive, the alarm flag goes active, and repeated attempts to read the random data yield the same byte. The alarm condition can be cleared only by a master reset. Although the random data-byte register can be accessed during a run-up test, this is not a good practice. During the run-up test, bits are scrambled in a way that removes bit-to-bit correlation between successively generated samples at the front-end D-type flip-flop. The scrambling process is not complete until the run-up test has finished.

Characteristics

Clocks

HFO (internal): 8 MHz

HFO (external): 12 MHz, maximum

Jitter (internal): Determined by RC (see Figure 5); R should be greater than 2 kΩ; frequency, f_{JIT}, should be much lower than the frequency of HFO, f_{HFO}, i.e., $4000\ f_{JIT} < f_{HFO}$

Jitter (external): Frequency, f_{JIT}, should be much lower than the frequency of HFO, f_{HFO}, i.e., $4000\ f_{JIT} < f_{HFO}$

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 10%, GRD = 0 V

Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Supply current	I_{DD}	—	5.5	14	mA	T = 20 °C, V_{DD} = 5.5 V, voltage on inputs and I/O pins = V_{DD}
		—	20	50	mA	T = 20 °C, V_{DD} = 5.5 V, voltage on inputs and I/O pins = 2.0 V
Input leakage	I_L	—	—	±10	μA	V_{IN} = V_{DD} to 0.0 V
Input voltage:						
low	V_{IL}	0	—	0.6	V	—
high	V_{IH}	2.2	—	V_{DD}	V	—
Output voltage:						
low	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 μA
high	V_{OH}	2.4	—	—	V	I_{OH} = –40 μA
Power dissipation	PD	—	30.25	77	mW	T = 20 °C, V_{DD} = 5.5 V, voltage on inputs and I/O pins = 2.0 V
		—	110	275	mW	T = 20 °C, V_{DD} = 5.5 V, voltage on inputs and I/O pins = 2.0 V

Maximum Ratings

DC supply voltage (V_{DD}) range ..... 5 V ± 10%
Operating temperature (T_A) range ..... 0 to 70 °C
Storage temperature (Tstg) range ..... –65 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

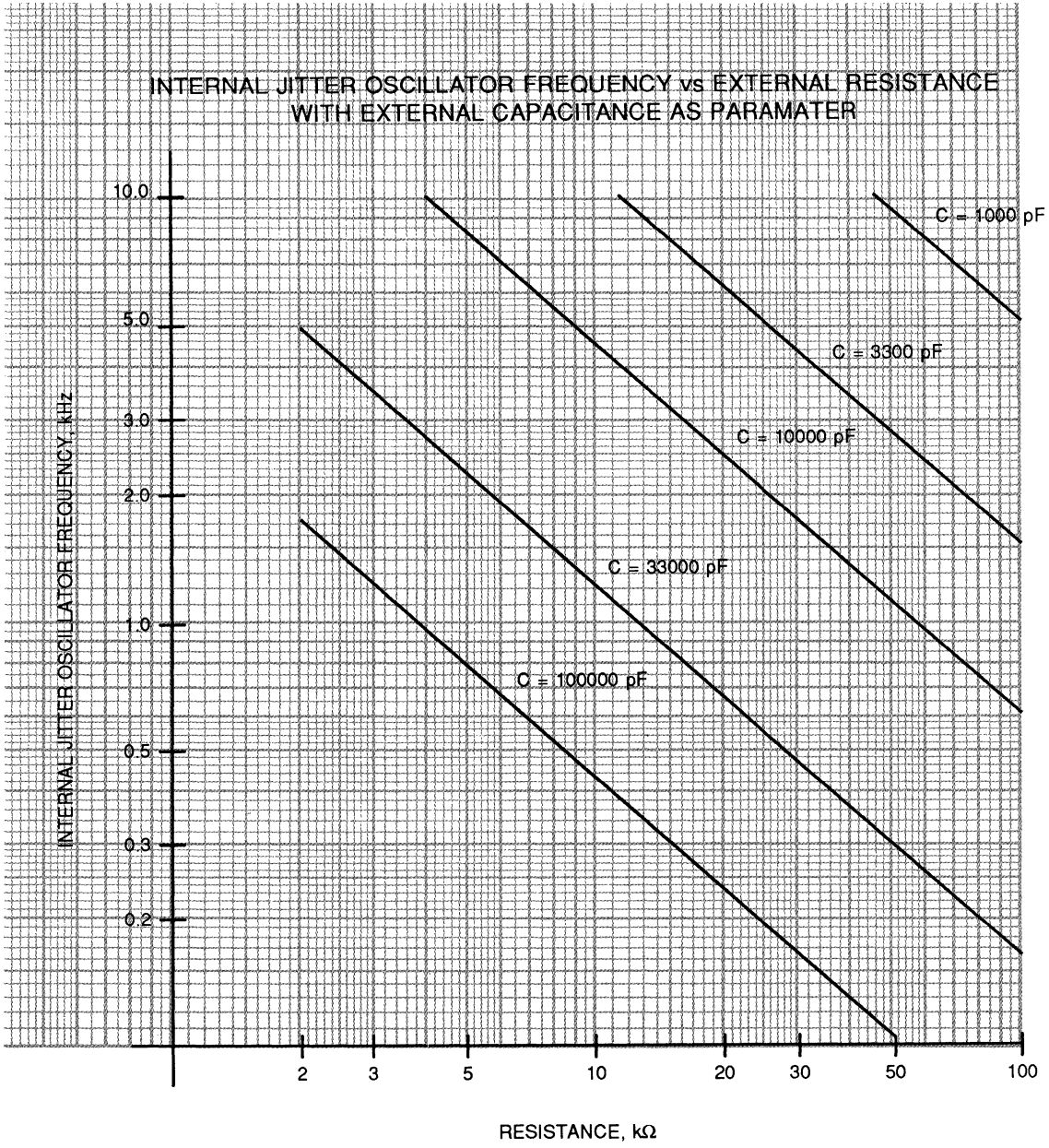


Figure 5. RC Network Selection Diagram

Timing Characteristics

Symbol	Description	Min	Max	Unit	Test Conditions
tAVRDL	Address to $\overline{RD}$ set-up time	50	—	ns	—
tAVWRL	Address to $\overline{WR}$ set-up time	50	—	ns	—
tCSLRDL	$\overline{CS}$ to $\overline{RD}$ set-up time	50	—	ns	—
tCSLWRL	$\overline{CS}$ to $\overline{WR}$ set-up time	50	—	ns	—
tDBVWRH	$\overline{WR}$ edge to data bus set-up time	400	—	ns	—
tMRLMRH	$\overline{MR}$ pulse width time	1.0	—	μs	—
tRDHAX	$\overline{RD}$ to address hold time	50	—	ns	—
tRDHCSH	$\overline{RD}$ to $\overline{CS}$ hold time	70	—	ns	—
tRDHDBZ	$\overline{RD}$ to data bus 3-state time	10	100	ns	—
tRDLDBV	$\overline{RD}$ to data delay time	—	260	ns	C_L = 100 pF
tRDLRDH	$\overline{RD}$ pulse width time	400	—	ns	—
tWRHAX	$\overline{WR}$ to address hold time	50	—	ns	—
tWRHCSH	$\overline{WR}$ to $\overline{CS}$ hold time	70	—	ns	—
tWRHDBX	Data hold time for $\overline{WR}$	35	—	ns	—
tWRLWRH	$\overline{WR}$ pulse width time	400	—	ns	—

Timing Diagrams

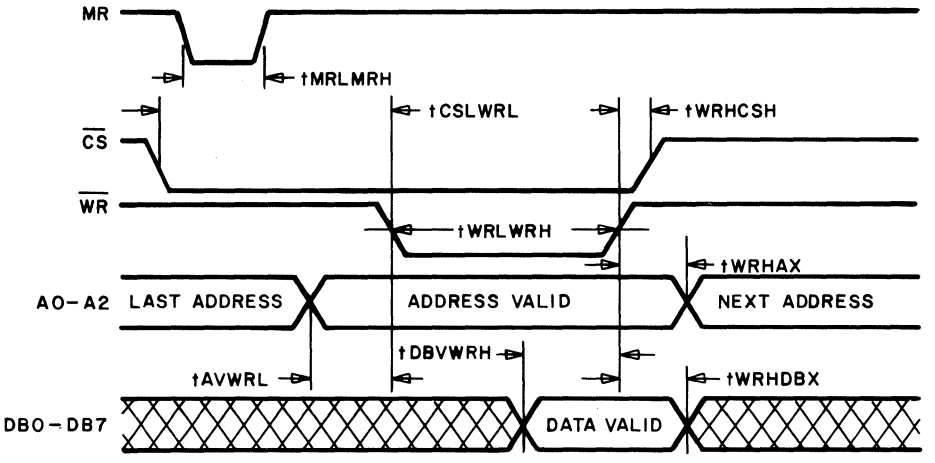


Figure 6. Write Cycle Timing

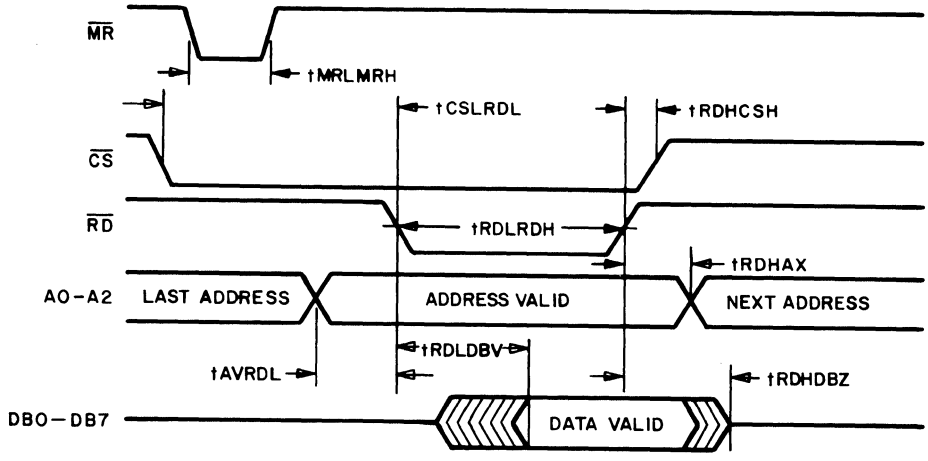
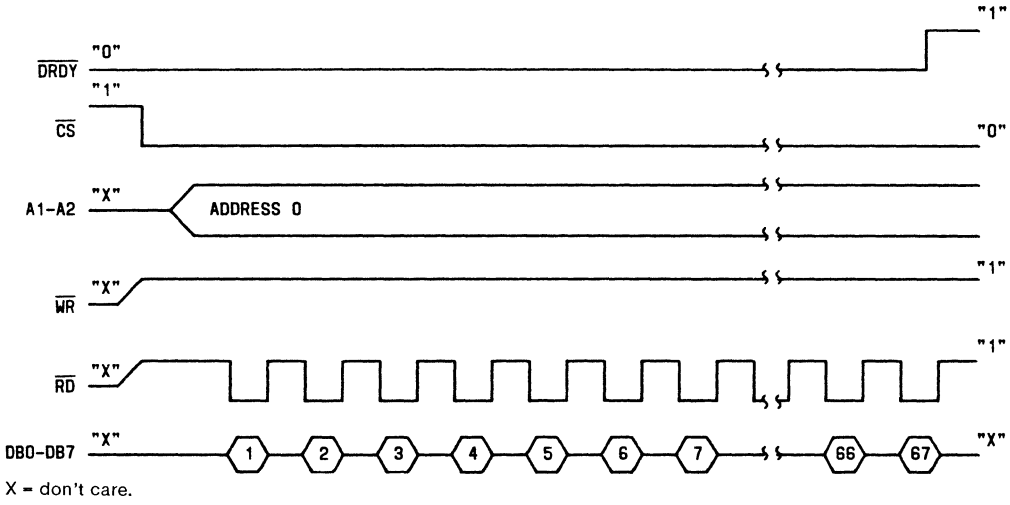
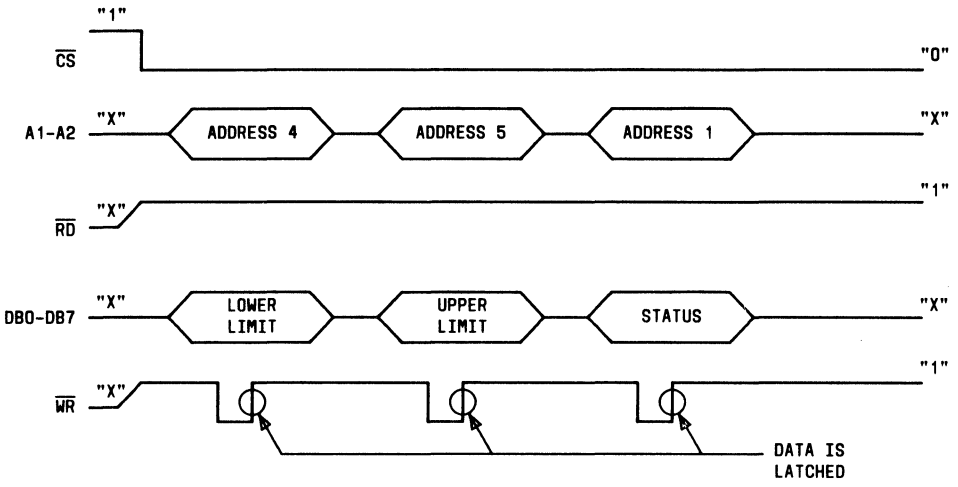


Figure 7. Read Cycle Timing



X = don't care.

Figure 8. Random Data-Byte Register Read Operations Timing



X = don't care.

Figure 9. Lower- and Upper-Limit Registers and Status/Command Register Write Operation Timing

T7002 Bit Slice Multiplier and T7003 BSM Extender

Features

- Cascadable circuit design with 292 bits on T7002 and 298 bits on a T7003
- Microprocessor compatible interface
- Calculate A x B (mod M)
- Exponentiate [B^{exp}] (mod M) under the control of a host processor
- Exponentiate at a rate of 27 ms for 512-bit operation
- Useful in public-key cryptography
- 1.5-micron CMOS design packaged in a standard 68-pin plastic leaded chip carrier

Description

The T7002 Bit Slice Multiplier (BSM) and T7003 BSM Extender form a cascadable circuit consisting of one T7002 chip followed by one or more T7003 chips. The T7002 BSM chip handles 292 multiplication bits, and each cascaded T7003 BSM Extender chip increases the bit length by 298 bits. The T7002 and T7003 circuit is designed as a microprocessor peripheral with only the T7002 chip interfacing with the host processor. Under the control of the processor, the T7002 and T7003 circuit may be used for calculating such mathematical equations as a modular exponentiation [B^{exp}] (mod M). Since the T7002 and T7003 circuit performs modular operations, it is very useful in cryptographic applications. The T7002 and the T7003 chips are manufactured using 1.5-micron CMOS technology, require a 5 V supply, and are packaged in a 68-pin plastic leaded chip carrier.

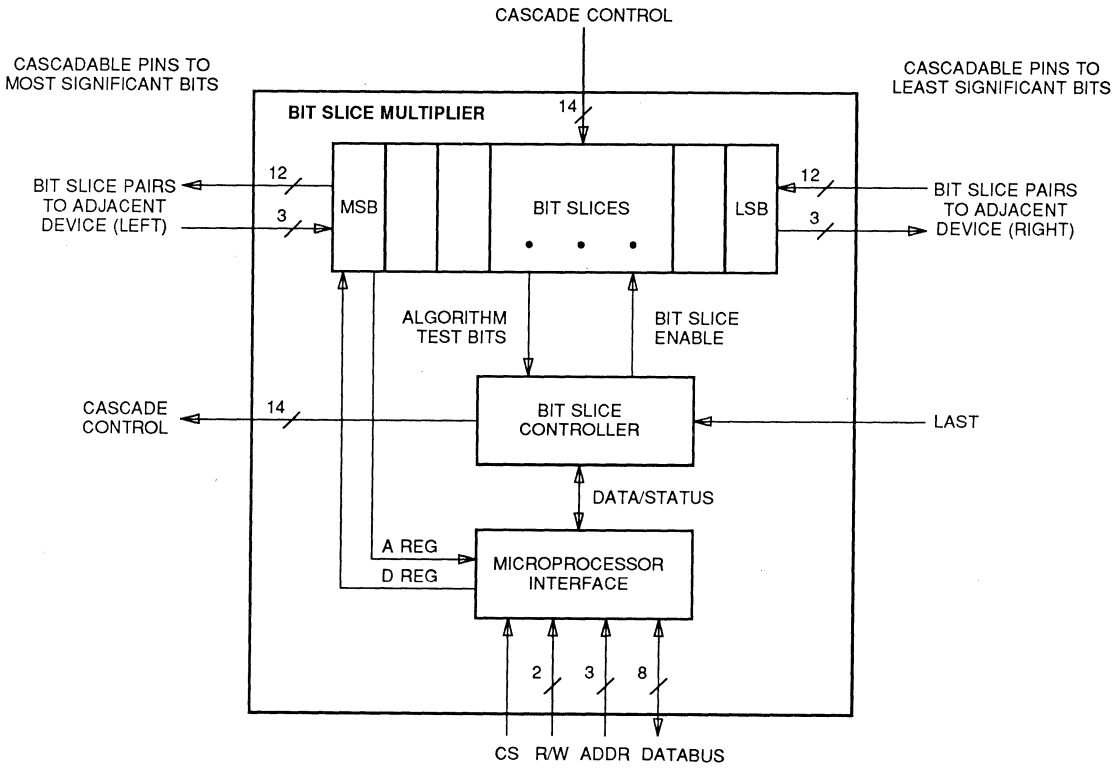


Figure 1. Block Diagram

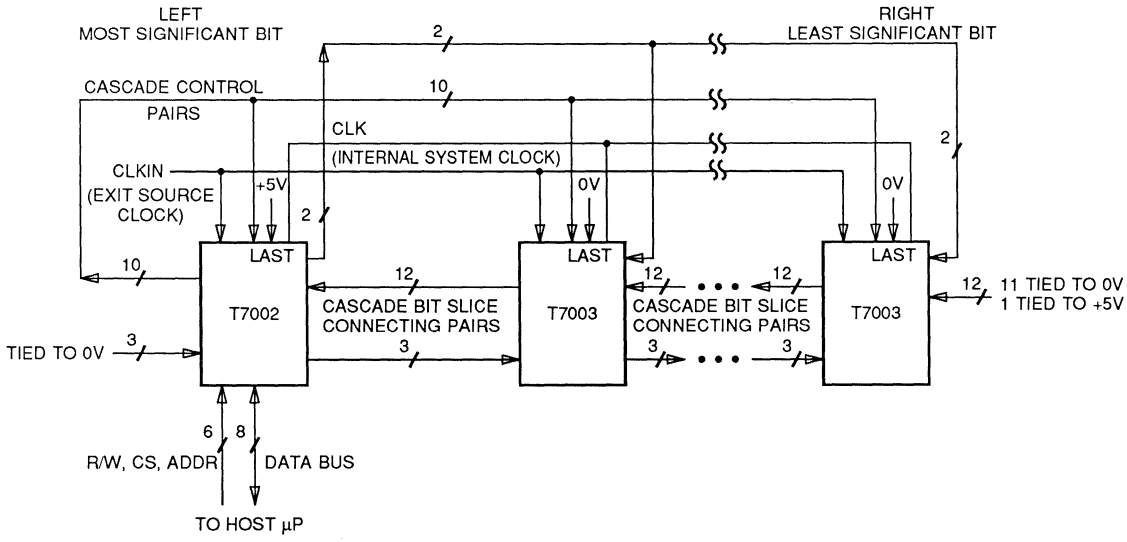


Figure 2. Cascade Block Diagram

T7100A X.25 Protocol Controller

Features

- 5-MHz clock (max)
- 250-kb/s serial data rate (max)
- 8-bit data bus
- 16-bit address bus
- Six bidirectional address leads for accessing internal registers
- Link initialization and supervision
- Error detection and automatic recovery via packet retransmission
- Automatic appending and testing of 16-bit frame check sequence (FCS) field
- Zero-bit insertion and deletion (for data transparency)
- Programmable address field
- Modulo-8 frame sequence numbering
- 3-bit programmable window size (k)
- Four independently programmable timers (T1—T4)
- Wait-state generator (on DMA side) for slow memory
- Triple-channel DMA with standard interface
- Programmable retransmission counter (N2)
- Password exchange mechanism for dial-up operation
- Daisy-chain DMA structure for easy expansion to multiple XPC-8 applications
- Transmit and receive data buffers accessed indirectly through a look-up table
- Memory error service via external parity checking circuitry
- Programmable bus interface to enable the XPC-8 to be configured for a Motorola or Intel bus
- Two independent test configurations (far-end loopback and near-end loopback) to verify XPC-8 operation and physical level services
- 3-state output buffers to assist in system diagnostics
- Programmable flag-fill option that specifies the minimum number of flags between frames

Description

The T7100A X.25 Protocol Controller (XPC-8) integrated circuit is a level 2 protocol controller with an 8-bit data bus. It is a single-chip VLSI device fabricated using NMOS silicon gate technology, requires a single 5 V supply, and is available in a 48-pin ceramic DIP. The XPC-8 implements the data link control functions defined in the X.25 packet switching communication standard. It satisfies the X.25 link level (level 2) requirements for a balanced link access procedure (LAPB) for data interchange over a synchronous full-duplex serial data link. The XPC-8 also is in compliance with CCITT X.25 1980 and ISO 7776 (which is at the draft international standard (DIS) level). The protocol controller is byte-oriented, with a maximum transmit and receive data rate of 250 kb/s. All inputs and outputs are TTL-compatible.

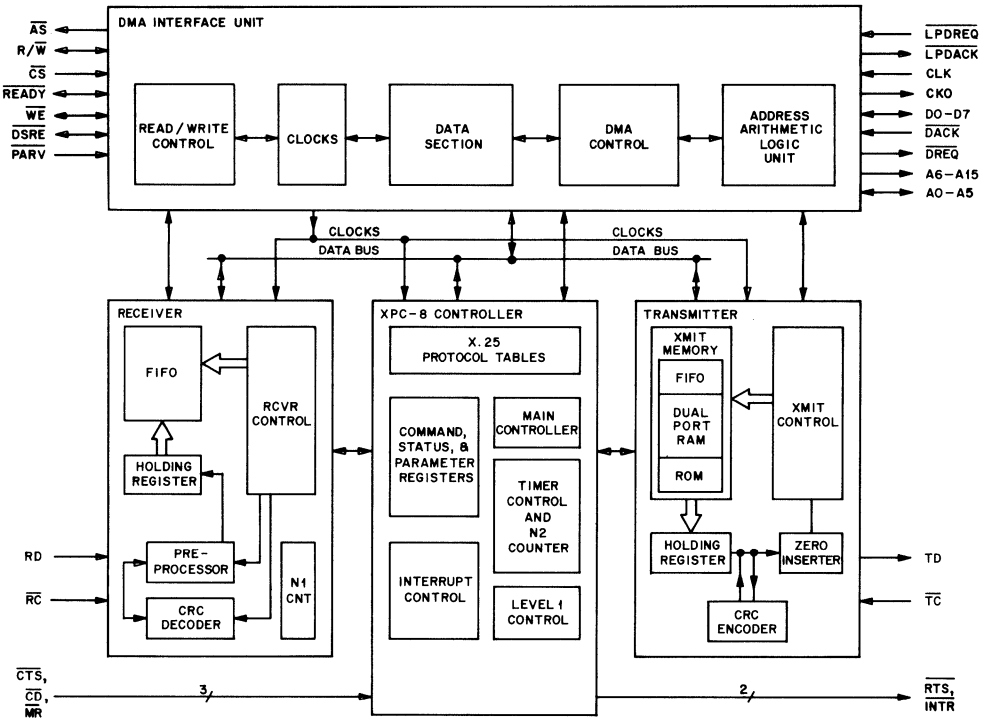
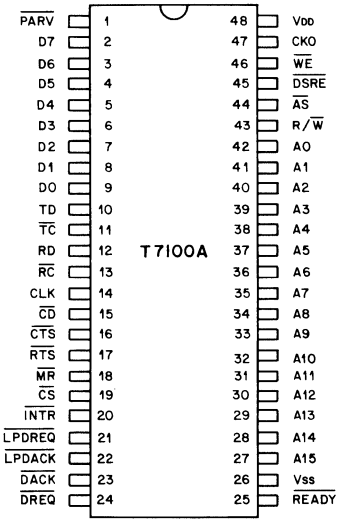


Figure 1. Block Diagram

User Information

Pin Descriptions



Sym	Pin	Sym	Pin	Sym	Pin
A0	42	$\overline{AS}$	44	$\overline{DSRE}$	45
A1	41	$\overline{CD}$	15	$\overline{INTR}$	20
A2	40	CKO	47	$\overline{LPDACK}$	22
A3	39	CLK	14	$\overline{LPDREQ}$	21
A9	38	$\overline{CS}$	19	$\overline{MR}$	18
A5	37	$\overline{CTS}$	16	$\overline{PARV}$	1
A6	36	D0	9	$\overline{RC}$	13
A7	35	D1	8	RD	12
A8	34	D2	7	$\overline{READY}$	25
A9	33	D3	6	$\overline{RTS}$	17
A10	32	D4	5	R/$\overline{W}$	43
A11	31	D5	4	$\overline{TC}$	11
A12	30	D6	3	TD	10
A13	29	D7	2	VDD	48
A14	28	$\overline{DACK}$	23	VSS	26
A15	27	$\overline{DREQ}$	24	$\overline{WE}$	46

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	$\overline{PARV}$	I	**Parity Valid (Active Low).** Notifies the XPC-8 that external parity checking circuitry has detected an error on an attempted DMA read or write operation. If this occurs on two consecutive attempts to run a bus cycle, a hard parity error (HPE) interrupt is generated (see Tables 7 and 8).
2—9	D7—D0	I/O*	**8-Bit Data Bus.** Used by the host CPU to access XPC-8 on-chip registers. Used by the XPC-8 during DMA operations to access system memory.
10	TD	O	**Transmit Data.** XPC-8 serial data output lead.
11	$\overline{TC}$	I	**Transmit Clock (Active Low).** Data is transmitted at this frequency.
12	RD	I	**Receive Data.** XPC-8 serial data input lead.
13	$\overline{RC}$	I	**Receive Clock (Active Low).** Data is received at this frequency.
14	CLK	I	**Master Clock Input.** Controls internal chip sequencing. The clock input must have a minimum frequency of 250 kHz ($f_{CLK} \geq 17\ f_{RC}$ and $f_{CLK} \geq 17\ f_{TC}$) and a maximum frequency of 5 MHz.

* Indicates 3-state output capability during normal operations.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
15	$\overline{CD}$	I	**Carrier Detect (Active Low).** Indicates that the level 1 interface (e.g., a modem) is receiving and modulating a usable signal. Transitions on this signal cause interrupts (see Table 8). The state of the $\overline{CD}$ lead does not otherwise affect XPC-8 operation.
16	$\overline{CTS}$	I	**Clear-To-Send (Active Low).** Indicates to the XPC-8 that the level 1 interface is ready. The data link does not come up until $\overline{CTS}$ is low. $\overline{CTS}$ must remain low while the link is up or an interrupt occurs (see Table 8) and the XPC-8 enters an inactive state until $\overline{CTS}$ is re-asserted (low).
17	$\overline{RTS}$	O	**Request-To-Send (Active Low).** Indicates that the XPC-8 is requesting the physical link. $\overline{RTS}$ remains low while the link is up.
18	$\overline{MR}$	I	**Master Reset (Active Low).** Resets the XPC-8 and selects either the Motorola or the Intel bus configuration. When low, all XPC-8 outputs are in the 3-state condition.
19	$\overline{CS}$	I	**Chip Select (Active Low).** Must be low to allow access to internal XPC-8 registers. When low, R/$\overline{W}$, $\overline{WE}$, $\overline{DSRE}$, and A0—A5 become inputs; $\overline{READY}$ becomes an output.
20	$\overline{INTR}$	O	**Interrupt Request (Active Low).** Indicates that the XPC-8 is requesting interrupt service. This lead goes high when the CPU reads the interrupt register.
21	$\overline{LPDREQ}$	I	**Low Priority DMA Request (Active Low).** Used to daisy-chain DMA requests in systems that use more than one XPC-8 without a bus arbiter. If daisy-chain DMA is not being used, $\overline{LPDREQ}$ must be tied high (5 V).
22	$\overline{LPDACK}$	O	**Low Priority DMA Acknowledge (Active Low).** When the host CPU drives this pin low, it grants the XPC-8 use of the system bus. $\overline{AS}$, $\overline{DSRE}$, R/$\overline{W}$, $\overline{WE}$, and the address pins become outputs.
24	$\overline{DREQ}$	O	**DMA Request (Active Low).** The XPC-8 pulls this pin low to request use of the system bus.
25	$\overline{READY}$	I/O*	**Ready (Active Low).** This pin is pulled low by the XPC-8 when a CPU read or write to an on-chip register is completed. During DMA cycles, the XPC-8 executes wait states until this lead is pulled low, indicating that the current read or write access has been completed.
26	V_{SS}	—	**Ground.**
27—36	A15—A6	O*	**16-Bit Address Bus.** When $\overline{CS}$ is low, A0—A5 are used in the input mode to address the internal registers of the XPC-8. All 16 address lines are used to access system memory during DMA cycles.
37—42	A5—A0	I/O*	

* Indicates 3-state output capability during normal operations.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
43	R/$\overline{W}$	I/O*	**Read or Write (Active Low).** Indicates whether the next data transfer performed is a read (high) or a write (low). This signal can also be used to control the direction of external bidirectional buffers placed on the data leads.
44	$\overline{AS}$	O*	**Address Strobe (Active Low).** This signal is used for both Motorola and Intel read and write operations. When low, it indicates that a valid memory address is currently on the address leads.
45	$\overline{DSRE}$	I/O*	**Data Strobe or Read Enable (Active Low).** The mode of this signal is determined during master reset. In a Motorola bus configuration, $\overline{DSRE}$ is a data strobe; in an Intel bus configuration, $\overline{DSRE}$ is a read enable.
46	$\overline{WE}$	I/O*	**Write Enable (Active Low).** This signal goes low when the XPC-8 performs a DMA write operation in either Intel or Motorola bus modes. For Intel bus mode, $\overline{WE}$ is used as an input when the CPU accesses the internal XPC-8 registers ($\overline{CS}$ = 0). For Motorola bus mode, $\overline{WE}$ should be connected to VDD through an external resistor (10 kΩ typical value). It should not be connected directly to VDD since damage may occur when $\overline{WE}$ switches to an output during DMA operations.
47	CKO	O	**Clock Output.** Buffered internal clock that runs at half the frequency of the input clock.
48	VDD	—	**5 V Supply.**

* Indicates 3-state output capability during normal operation.

Overview

The XPC-8 performs complete link level control according to the X.25 data communications protocol. It generates supervisory and unnumbered frames automatically without intervention by the host (CPU). The CPU must initialize the XPC-8 and supply buffers for the data fields of received and transmitted information frames. It is notified of important events via interrupts. The XPC-8 contains a transmitter, a receiver, an XPC-8 controller, and an interface unit (see Figure 1).

Architecture

Transmitter

The transmitter constructs frames on command from the XPC-8 controller. It handles the transmission of continuous flags, aborts, and idle channel indications automatically. It contains a transmitter controller, 4-byte first-in-first-out (FIFO) buffer, RAM, ROM, holding register, cyclic redundancy check (CRC) encoder, and zero inserter. The FIFO is used for temporary storage of data delivered from host memory to the transmitter by the interface unit via direct memory access (DMA). The transmitter memory (RAM/ROM) is used to store the various bytes needed to construct a frame. Frames are formed by sequentially loading the holding register with bytes read from the transmitter memory and FIFO, serially shifting these bytes through the zero inserter and, finally, sending the bit stream on the transmit data (TD) lead. Data is shifted on the falling edge of the transmit clock ($\overline{TC}$). The CRC encoder calculates the frame check sequence (FCS) and appends it to the control field, or to the data field for frames with data. The zero inserter performs bit stuffing to ensure data transparency.

Receiver

The receiver processes incoming data and notifies the XPC-8 controller of received frames and other link conditions. It contains a preprocessor, receiver controller, 6-byte FIFO, and CRC decoder. The preprocessor detects flags, aborts, and idle conditions on the data link and removes the 0s inserted for data transparency. Frames are identified and checked for proper format by the receiver controller. Data received as part of the information field of a frame is loaded into the FIFO. The interface unit, informed of the presence of received data, is responsible for reading FIFO data and writing it to system memory.

Frames are checked for errors by means of the FCS in the CRC decoder. The XPC-8 acts only on frames that are received error-free; frames received with errors are discarded. Frames with addresses other than the programmed command or response address are also discarded.

Interface Unit

The interface unit provides the interface between the host CPU and the XPC-8 transmitter and receiver via triple-channel DMA. It consists of four sections: an address arithmetic logic unit (AALU), a data section, a read/write controller, and a DMA controller.

The AALU contains four registers (not user-accessible) that are used to calculate and store the buffer pointers and byte counters for the transmit and receive channels. A fifth register is used to implement a third DMA channel for the processing of received acknowledgments. The additional channel enables the host to use its memory more efficiently by freeing the transmit data buffers as acknowledgments are received for them; therefore, data throughput is increased as a result of this extra DMA channel.

The read/write controller generates the control signals needed to access data from the host memory, while the data section routes the data from the host memory to various XPC-8 internal locations. The DMA controller coordinates the actions of the other three sections and connects them to the XPC-8 controller. Under command of the XPC-8 controller, the DMA controller is instructed to open data buffers for the transmitter and receiver in system memory. The locations of these data buffers are specified by the TLOOK and RLOOK table elements that the host CPU supplies.

When data is available for the transmitter, the read-write controller fetches bytes of data from system memory and routes them through the data section to the transmitter FIFO. The DMA continues to load bytes of data into the transmitter FIFO until the FIFO is full. The transmitter signals the interface unit for more data when two bytes or less remain in the FIFO. The loading process ends when the number of bytes specified in the TLOOK element has been loaded into the transmitter FIFO. The TLOOK element corresponding to the frame being sent is then placed in the unacknowledged state.

The reverse process is used for the receiver. The DMA controller instructs the read-write controller to write bytes of received data to system memory via the data section when the receiver FIFO contains two or more bytes of data. The interface unit continues to write data until it is notified by the receiver of an error-free end-of-frame condition. It then finishes writing the remaining bytes of data, updates the RLOOK element with the number of bytes received, and places the element into the frame complete state. If the receiver reports an error condition at the end of the frame, the RLOOK element is untouched and remains in the ready state.

XPC-8 Controller

The XPC-8 controller handles the interface between the transmitter, the receiver, and the interface unit, and contains all the logic needed to implement the X.25 protocol. Specific tasks of the XPC-8 controller include configuring the link as specified by the parameter and command registers, maintaining the status registers, directing the interface unit to acquire receive or transmit data buffers, directing the transmitter to send specific frames, managing timing functions, and using a set of interrupts to notify the host CPU of certain data link conditions.

Principles of Operation

CPU Interface

The CPU has access to 27 internal XPC-8 registers, which it uses to configure and monitor the XPC-8. The CPU configures the XPC-8 by writing the command and parameter registers. Status information, used to monitor XPC-8 operations, is accessed by reading one of the eight status registers. Special events are encoded in the interrupt register, which can then be accessed by the CPU.

Each register is assigned a unique address and can be accessed by providing the proper Motorola or Intel read/write cycle while the XPC-8 is selected ($\overline{CS}$ is low). Table 2 lists the XPC-8 register addresses.

Table 2. XPC-8 Register Addresses

Register Name	Symbol	Address (Hex)
Command register	CR	00
Status register 0	SR0	01
Status register 1	SR1	02
Status register 2	SR2	03
Status register 3	SR3	04
Status register 4	SR4	05
Status register 5	SR5	06
Status register 6	SR6	07
Status register 7	SR7	08
Interrupt register	IR	09
Parameter register 0	PR0	0A
Parameter register 1	PR1	0B
Parameter register 2	PR2	0C
Parameter register 3	PR3	0D
Parameter register 4	PR4	0E
Parameter register 5	PR5	0F
Parameter register 6	PR6	10
Parameter register 7	PR7	11
Parameter register 8	PR8	12
Parameter register 9	PR9	13
Parameter register 10	PR10	14
Parameter register 11	PR11	15
Parameter register 12	PR12	16
Parameter register 13	PR13	17
Parameter register 14	PR14	18
Parameter register 15	PR15	19
Parameter register 16	PR16	1A

XPC-8 Registers

The XPC-8 registers are divided into four types: command, status, interrupt, and parameter.

Command Register. This read/write register controls 7 XPC-8 functions: send permission, receive permission, mandatory disconnect, active/passive link initialization, password exchange mode, password verification, and link disconnect mode (see Table 3).

Status Registers. These 8 read-only registers contain such information as the present state of the XPC-8, V(S), V(R), NA, and LNA (see Figure 3 and Tables 4, 5, and 6).

Interrupt Register. This read-only register contains a 5-bit interrupt code and a lost interrupt (LSTIN) bit. It is backed by a 4-byte FIFO buffer whose output is automatically loaded into the interrupt register as soon as the contents of the register have been read by the CPU. If the 4-byte buffer overflows, the LSTIN bit of this register is set. The LSTIN bit is cleared as soon as the interrupt register is read. A zero-interrupt code indicates that all of the outstanding interrupts have been read by the host (see Tables 7 and 8).

Parameter Registers. These 17 write-only registers specify system constants and modes of operation. Examples include timer values, window size, TLOOK starting address, command and response address, and test modes. Parameter registers 1—16 can be written only when the logical link is disconnected and MDISC = 1 (see Figure 4 and Table 9).

Table 3. Command Register Definitions

Bit	7	6	5	4	3	2	1	0
Field	DISCMOD	PWOK2	PWOK1	PWXCH	ACT/PAS	RECR	MDISC	SEND

Bit	Symbol	Name/Description
0	SEND	**Send.** Controls the transmission of packets. If 0, it inhibits the XPC-8 from sending new packets; if 1, it enables the XPC-8 to send new packets. Retransmissions occur automatically, regardless of the SEND bit state. SEND is cleared during a valid reset or if a hard parity error occurs during a transmit channel DMA operation (see Table 8).
1	MDISC	**Mandatory Disconnect.** If 0, logical link establishment is permitted; if 1, the logical link goes to a logically disconnected state, and the XPC-8 responds to all inquiries with a disconnected mode (DM) frame and idles (transmit all 1s) between frames. MDISC is set during a valid reset.
2	RECR	**Receiver Ready.** Indicates to the XPC-8 the availability of receive data buffers in system memory. If 0, no receive data buffers are available; if 1, receive data buffers have been allocated and are available. RECR is cleared during a valid reset if a hard parity error (see Table 8) occurs during a receive channel DMA operation or a receiver overrun occurs.
3	ACT/PAS	**Active/Passive.** Specifies the XPC-8 action during link set-up. If 1, the XPC-8 actively pursues link set-up; if 0, the XPC-8 passively awaits link set-up. ACT/PAS is cleared during a valid reset.
4	PWXCH	**Password Exchange.** Specifies whether the XPC-8 should actively pursue a password exchange (PWXCH = 1) or passively await the initiation of a password exchange by a remote DTE (PWXCH = 0). PWXCH is cleared during a valid reset.
5	PWOK1	**Password Verified.** These bits are used by the host CPU to notify the XPC-8 of the results of its received password examination. These bits are cleared during a valid reset and are interpreted in conjunction with PWXCH (bit 4) as: **Code** (**b6 b5 b4**) — **Condition** 0 1 0 — Valid password command received 0 1 1 — Valid password response received 1 0 0 — Valid password command not received 1 0 1 — Valid password response not received
6	PWOK2	

Table 3. Command Register Definitions (Continued)

Bit	Symbol	Name/Description
7	DISCMOD	**Disconnect Mode.** Specifies which of two states the XPC-8 assumes when logically disconnected. If 0, the XPC-8 responds to all inquiries (command frames with their poll bits set) with a DM frame while logically disconnected. This implies that link set-up can be successfully pursued only from the local side of the link. If 1, the XPC-8 responds to all inquiries as specified by the X.25 protocol. In this case, link set-up can be successfully pursued from either side of the link. DISCMOD is set during a valid reset.

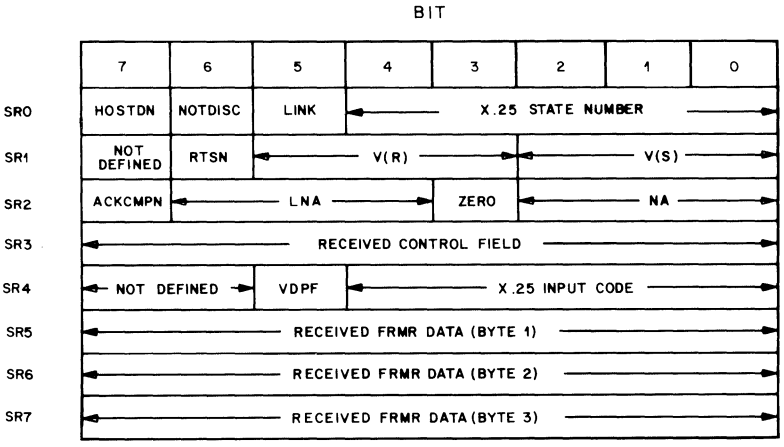


Figure 3. Status Registers

Table 4. Status Registers

Reg	Bit	Symbol	Name/Description
0	0—4	XST	**X.25 State Number.** Indicates the present state of the X.25 protocol (see Table 5).
0	5	LINK	**Link Status.** Indicates whether the XPC-8 has entered the information transfer phase. If 0, the XPC-8 has not entered this phase and information transfer is not permitted; if 1, the XPC-8 is in the information transfer phase (X.25 state $\geq$ S6).
0	6	NOTDISC	**Not Disconnected.** Indicates whether a logical link exists between two level 2 entities. If 0, the logical link is disconnected; if 1, the logical link is connected and the level 2 entities are communicating (X.25 state $\geq$ S4).
0	7	$\overline{\text{HOSTD}}$	**Host Done (Active Low).** Indicates whether the host CPU has reassigned transmit and receive data buffers in preparation for link reinitialization. If 0, the host has completed all transmit data buffer reassignments; if 1, the host must reassign transmit and receive data buffers before link reinitialization is permitted. This bit is cleared when the CPU writes to status register 0. Bits 0—6 of status register 0 cannot be written and $\overline{\text{HOSTD}}$ can only be cleared. It is the act of writing to this register that clears $\overline{\text{HOSTD}}$.

Table 4. Status Registers (Continued)

Reg	Bit	Symbol	Name/Description
1	0—2	V(S)	**Send State Variable.** Denotes the sequence number of the next in-sequence I frame to be transmitted. V(S) is used to index into the TLOOK table to indicate the TLOOK element that describes the next packet to be transmitted.
1	3—5	V(R)	**Receive State Variable.** Denotes the sequence number of the next in-sequence I frame to be received. V(R) is used to index into the RLOOK table to indicate the RLOOK element that describes the receive data buffer for the next received packet.
1	6	$\overline{\text{RST}}$	**Request to Send (Active Low).** If 0, the XPC-8 is requesting to use the physical link.
1	7	—	**Reserved.** This bit is used for testing purposes.
2	0—2	NA	**Next Acknowledge Expected.** Contains the sequence number of the earliest unacknowledged packet. If there are no outstanding packets, NA = V(S).
2	3	—	**Zero.** This bit is not used and must be cleared.
2	4—6	LNA	**Last Next Acknowledge Expected.** When NA is updated, the old value of NA is saved here. NA and LNA can be used to determine how many transmit data buffers have been acknowledged by the remote DXE and subsequently freed by the XPC-8.
2	7	$\overline{\text{ACKCMP}}$	**Acknowledgments Complete (Active Low).** To prepare for logical link reinitialization, the CPU must reallocate transmit buffers. Before reallocation begins, the CPU should check $\overline{\text{ACKCMP}}$ to be sure that the interface unit has finished processing all received acknowledgments. If 0, the interface unit has processed all the acknowledgments received from the remote DXE and the CPU can begin transmit buffer reallocation; if 1, received acknowledgments are still being processed.
3	0—7	RCF	**Received Control Field.** Holds the control field of the most recently received error-free frame.
4	0—4	XCT	**X.25 Input Code.** Contains an encoding of what the X.25 protocol considers its most recent input stimulus (see Table 6).
4	5	VDPF	**Valid Poll/Final.** Indicates whether the poll/final bit of the last error-free frame received was a 1 or a 0.
4	6—7	—	**Reserved.** These bits are used for testing purposes.
5—7	0—7	FRMRDF	**Received Frame Reject (FRMR) Data Field.** Registers 5, 6, and 7 hold the first, second, and third bytes, respectively, of the data field contained in the received FRMR frame.

Table 5. Status Register 0 — Bits 0—4 (XST)

State Number b4	b3	b2	b1	b0	State	Name
0	0	0	0	0	S0	Super logical disconnect
0	0	0	0	1	S1	Logical disconnect
0	0	0	1	0	S2a	Awaiting XID command
0	0	0	1	1	S2b	Awaiting XID response
0	0	1	0	0	S3	Link set-up
0	0	1	1	1	S4	Frame rejected
0	0	1	0	1	S5	Disconnect request
0	0	1	1	0	S6	Information transfer
0	1	0	0	0	S7	REJ frame sent
0	1	0	0	1	S8	Waiting for acknowledgment
1	0	0	0	1	S9	Station busy
0	1	0	1	0	S10	Remote station busy
0	1	1	1	1	S11	States 9 and 10
1	0	0	0	0	S12	States 8 and 9
0	1	0	1	1	S13	States 8 and 10
1	1	0	1	0	S14	States 8, 9, and 10
1	1	0	1	1	S15	States 7 and 9
0	1	1	0	0	S16	States 7 and 10
0	1	1	0	1	S17	States 7, 9, and 10

Table 6. Status Register — 4 Bits 0—4 (XCT)

Input Code	Description	Input Code	Description
0	Local stop	14	RNR command frame received
1	Local start	15	I frame received
2	TI expired	16	UA received
3	T4 expired	17	FRMR received
4	Unrecognized frame	18	DM received
5	Valid XID command received	19	SABM received
6	Station busy	20	Invalid N(R)
7	I frame available (code seen after reset)	21	Valid XID response
		22	T2 expired
8	Busy condition clears	24	Idle link detected for T3
9	Invalid N(S)	25	N2 exceeded
10	Initiate password exchange	26	DISC received
11	Wait for password exchange	28	REJ response received
12	REJ command frame received	29	RR response received
13	RR command frame received	30	RNR response received

Table 7. Interrupt Register

Bit	7	6	5	4	0
Field	LSTIN	ZERO	ZERO	INTERRUPT CODE	

Bit	Symbol	Name/Description
0—4	—	**Interrupt Code.** This 5-bit number can take on any value from 0 to 27. Each value indicates a different interrupt condition, as described in Table 8.
5—6	—	**Zero.** These bits are not used and must be cleared.
7	LSTIN	**Lost Interrupt.** A 1 in this bit position indicates the loss of one or more interrupt codes due to the overflow of the interrupt FIFO. This bit is cleared upon reading the interrupt register.

Table 8. Interrupt Register Codes

Code	Symbol	Name/Description
0	NULL	**Null.** No interrupt conditions are outstanding.
1	SABM	**Set Asynchronous Balanced Mode Received.** An SABM command frame was received while the XPC-8 was in the information transfer phase.
2	UA	**Unnumbered Acknowledge Received.** An unnumbered acknowledgment frame was received while the XPC-8 was in the information transfer phase.
3	DM	**Disconnect Mode.** A DM frame was received.
4	FRMRR	**Frame Reject Received.** A frame reject (FRMR) frame was received. The data field of the FRMR is stored in status registers 5—7.
5	DISC	**Disconnect.** A disconnect (DISC) frame was received while the XPC-8 was in the information transfer phase.
6	IDLNK	**Idle Link.** An idle link condition has prevailed for a period in excess of T3.
7	N2EXC	**N2/C2 Counter Exceeded.** If this interrupt occurs during a password exchange, it should be interpreted as a C2 counter exceeded condition. Otherwise, it should be interpreted as an N2 counter exceeded condition.
8	RF1P	**Received Final Bit Before Poll.** A response frame with its final bit set was received without having transmitted a command frame with its poll bit set.
9	LK01	**Logical Link Up.** The XPC-8 has entered the information transfer phase (the logical link has come up).
10	LK10	**Logical Link Down.** The XPC-8 has left the information transfer phase (the logical link has gone down).
11	XIDR	**XID Received.** An XID frame was received and its data field placed in system memory.
12	NOXIDR	**No XID Received.** An XID command frame was transmitted and an XID response frame was not received for a period of T4.
13	FRMRXW	**Frame Reject Transmitted (W = 1).** A frame reject was transmitted because a frame was received with an invalid control field.

Table 8. Interrupt Register Codes (Continued)

Code	Symbol	Name/Description
14	FRMRXX	**Frame Reject Transmitted (X = 1, W = 1).** A frame reject was transmitted because a frame was received whose control field is considered invalid because the frame contains an information field that is not permitted, or because the frame is a supervisory or unnumbered frame of incorrect length.
15	FRMRXY	**Frame Reject Transmitted (Y = 1).** A frame reject was transmitted because the information field received exceeded the maximum established capacity set by parameter N1.
16	FRMRXZ	**Frame Reject Transmitted (Z = 1).** A frame reject was transmitted because the control field received contained an invalid N(R).
17	PKR	**Packet Received.** The XPC-8 has received an I frame and stored its information field in system memory.
18	XBA	**Transmitted Block Acknowledged.** The XPC-8 has received and processed acknowledgments for one or more previously transmitted I frames.
19	RCVOVR	**Receiver Overrun.** The receiver FIFO data buffer has overflowed because information field data bytes were being received faster than the interface unit could store them in system memory. The receiver FIFO is 6 bytes deep.
20	XUNDR	**Transmitter Underrun.** The transmitter FIFO data buffer has underflowed because information field data bytes were being transmitted faster than the interface unit could replenish the FIFO with data read from system memory. If the transmitter FIFO is empty when more data is needed for transmission, the transmitter aborts the frame and generates this interrupt. The XPC-8 attempts to retransmit the information frame if the SEND bit remains set. The host CPU may discontinue retransmission attempts by clearing the SEND bit. The transmitter FIFO is 4 bytes deep.
21	RLKNRDY	**RLOOK Not Ready.** The XPC-8 has read the RLOOK table element referenced by V(R) and it was not ready (i.e., RECRDY = 0). The XPC-8 goes to a station busy state.
22	CTSLST	**Clear-to-Send Lost.** The clear-to-send ($\overline{CTS}$) input has gone high while the XPC-8 was in the information transfer phase.
23	CARFND	**Carrier Found.** The carrier detect ($\overline{CD}$) signal from the physical link has been established (went low).
24	CARLST	**Carrier Lost.** The carrier detect ($\overline{CD}$) signal from the physical link has been lost (went high).
25	NOAD	**No Address.** The TLOOK starting address is 0 (not a valid starting address).
26	HPE	**Hard Parity Error.** The XPC-8 was notified of a parity error, via the $\overline{PARV}$ pin, on each of two attempts to complete a DMA read or write cycle. If the error occurred during a transmit channel DMA operation, the SEND bit of the command register is cleared. If the error occurred during a receive channel DMA operation, the RECR bit of the command register is cleared.
27	NULIF	**Null I Frame Received.** An I frame without an information field was received. The XPC-8 treats null I frames as any other I frame except that it generates this interrupt.

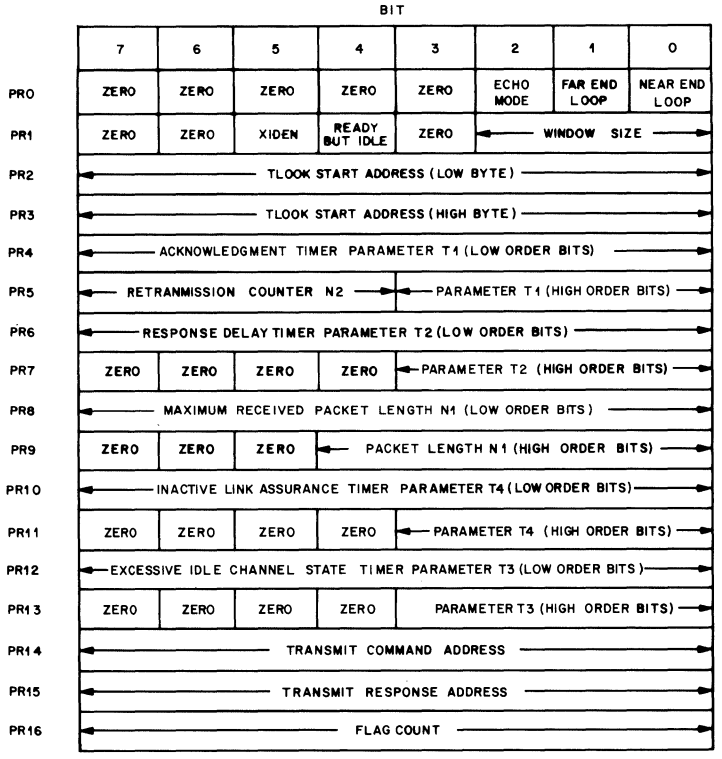


Figure 4. Parameter Registers

Table 9. Parameter Register Definitions

Reg	Bit	Symbol	Name/Description
0	0	NELT	**Near-End Loop Test.** Setting this bit causes the XPC-8 to enter the near-end loopback test mode.
0	1	FELT	**Far-End Loop Test.** Setting this bit causes the XPC-8 to enter the far-end loopback test mode.
0	2	ECHO	**Echo Mode.** Setting this bit causes the XPC-8 to transmit what it receives unaltered (i.e., the RD and TD pins are internally connected).
0	3—7	—	**Zero.** These bits must be cleared.
1	0—2	k	**Window Size.** Maximum allowable number of outstanding I frames. An outstanding I frame is any frame that has not been acknowledged by the remote DXE (either DTE or DCE). The window size must not equal 0.
1	3	—	**Reserved.** This bit must be cleared.
1	4	RDYIDL	**Ready But Idle.** The bit has meaning only when the logical link is disconnected and MDISC = 0. If RDYIDL is 0, the XPC-8 sends flags between frames; if 1, the XPC-8 idles between frames.
1	5	XIDEN	**XID Enable.** Setting this bit enables the password exchange mechanism.
1	6—7	—	**Zero.** These bits must be cleared.

Table 9. Parameter Register Definitions (Continued)

Reg	Bit	Symbol	Name/Description
2—3	0—7	TLOOKSA	**TLOOK Table Starting Address.** Indicates the starting address in system memory of the first element in the transmitter look-up TLOOK table. The address must not equal 0.
4	0—7	T1 (low byte)	**Acknowledgment Timer Parameter.** T1 is the maximum time that the XPC-8 waits for an acknowledgment. The period of the T1 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T1} = 32{,}768 \times \frac{\text{T1 parameter}}{f_{CKO}}$.
5	0—3	T1 (high bits)	
5	4—7	N2	**Transmission and Retransmission Counter.** The maximum allowable number of transmissions and retransmissions of a frame without receiving an acceptable response.
6	0—7	T2 (low byte)	**Response Timer Parameter.** T2 is the maximum time that the XPC-8 waits before responding to an inquiry from the remote DXE. The period of the T2 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T2} = 32{,}768 \times \frac{\text{T2 parameter}}{f_{CKO}}$.
7	0—3	T2 (high bits)	
7	4—7	—	**Zero.** These bits must be cleared.
8	0—7	N1 (low byte)	**Maximum Received Packet Length.** The maximum number of bytes that the receiver accepts in the information field of a frame before rejecting the received frame.
9	0—4	N1 (high bits)	
9	5—7	—	**Zero.** These bits must be cleared.
10	0—7	T4 (low byte)	**Inactive Link Assurance Timer Parameter.** During intervals when the T1 timing function is not performed (i.e., there are no outstanding unacknowledged I frames or P-bit frames), an appropriate S-format command frame with the P-bit set is transmitted every T4 time units to verify the status of the remote DXE. The period of the T4 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T4} = 32{,}768 \times \frac{\text{T4 parameter}}{f_{CKO}}$.
11	0—3	T4 (high bits)	
11	4—7	—	**Zero.** These bits should be cleared.
12	0—7	T3 (low byte)	**Excessive Idle Channel State Timer Parameter.** T3 specifies the amount of time that the XPC-8 accepts the reception of an idle condition before taking alternate actions. The period of the T3 timer is a function of the system clock (CKO) and is calculated as follows: $\text{period of T3} = 32{,}768 \times \frac{\text{T3 parameter}}{f_{CKO}}$.
13	0—3	T3 (high bits)	
13	4—7	—	**Zero.** These bits must be cleared.
14	0—7	TCA	**Transmit Command Address.** Address field of the command frames transmitted by the XPC-8 (the station address of the far end of the link).

Table 9. Parameter Register Definitions (Continued)

Reg	Bit	Symbol	Name/Description
15	0—7	TRA	**Transmit Response Address.** Address field of the response frames transmitted by the XPC-8 (the station address of this station).
16	0—7	FLGCNT	**Flag Count.** Specifies the minimum number of extra flags between frames. The value of FLGCNT is cleared on reset. A value of 0 causes the minimum number of flags between frames to default to 1. FLGCNT is a special feature of the XPC-8 and is not part of the X.25 protocol.

Bus and I/O Logic

Bits A0—A5 of the address bus are bidirectional and are used to access the 27 internal registers. When the XPC-8 is selected, R/$\overline{W}$, $\overline{WE}$, $\overline{DSRE}$, and address lines A0—A5 become inputs; $\overline{READY}$ becomes an output.

DMA operations are controlled by the interface unit. The XPC-8 uses DMA to access system memory to read and write TLOOK table elements, RLOOK table elements, and data fields of information frames. A daisy-chain DMA priority scheme can be implemented for multiple XPC-8 applications.

The data bus can be configured to be either Motorola or Intel compatible. Master reset is used for bus mode selection.

XPC-8 Master Reset

When the master reset ($\overline{MR}$) is low, all outputs are put into the high-impedance state and the parameter registers except for the TLOOK starting address (parameter registers 2 and 3) = 0 are cleared. The command register is set to 82H (DISCMOD = 1, MDISC = 1, all other bits = 0).

In addition, the master reset is used to choose between the Intel and Motorola bus modes. A reset pulse must be held low for at least six cycles of CKO to be considered a valid reset request. Glitch protection circuitry guarantees that glitches of less than one CLK period are ignored. If a single valid reset request is provided, the XPC-8 bus is configured for the Motorola bus standard. If a second valid reset request is provided within 30 cycles of CKO, the XPC-8 switches to the Intel bus standard. $\overline{MR}$ must be held high for at least six cycles of CKO after a reset pulse before the XPC-8 can recognize a second reset pulse. Any reset pulses occurring after the 30 cycles of CKO are interpreted as a new reset sequence (see Figure 11).

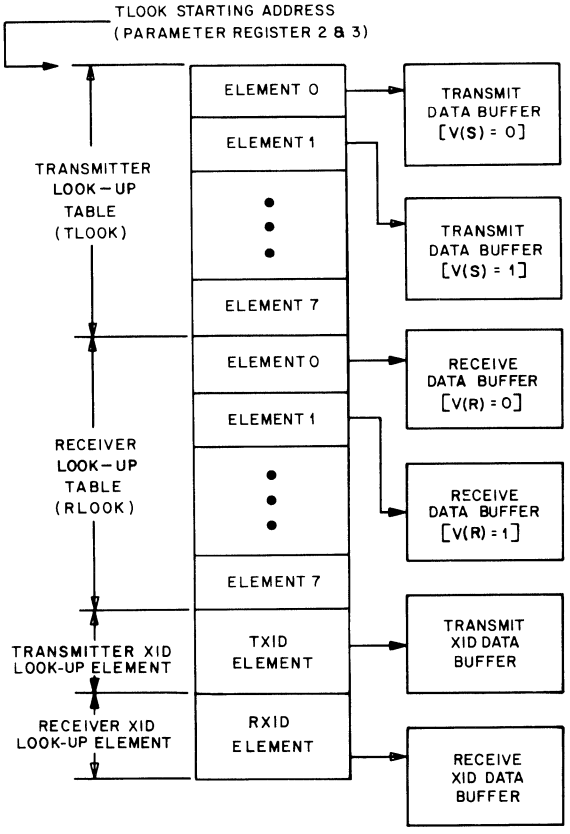
Transmitter and Receiver Look-Up Tables

System memory contains data buffers that store transmit and receive data. The pointers used to access these buffers are stored in look-up tables in system memory. The location of data to be transmitted is described by pointers in the transmitter look-up table (TLOOK) elements and the location of data to be received is described by pointers in the receiver look-up table (RLOOK) elements. Figure 5 is a diagram of the system memory interface.

The TLOOK table is a block of eight 8-byte elements in system memory that starts at the TLOOK starting address (parameter registers 2 and 3). Each element in the TLOOK table describes a buffer corresponding to one packet of data to be transmitted by the XPC-8. The TLOOK list of elements is a modulo-8 circular queue. Figure 6 and Table 10 present the bit assignments and descriptions for the TLOOK elements.

The RLOOK table is a block of eight 8-byte elements in system memory that immediately follows the TLOOK table. Each element in the RLOOK table describes a buffer corresponding to one packet to be received by the XPC-8. The RLOOK list of elements is also a circular queue. Figure 7 and Table 11 present the bit assignments and descriptions for the RLOOK elements.

In addition to the two look-up tables described above, there are two single-element look-up tables (TXID and RXID) that are used only during password exchange. They are located in system memory immediately following the RLOOK elements. The TXID and RXID look-up tables are used to describe the transmit password and receive password data buffers, respectively. Their format is identical to that of the TLOOK and RLOOK elements.



Note: Each element has 8 bytes of data.

Figure 5. XPC-8/CPU System Memory Interface

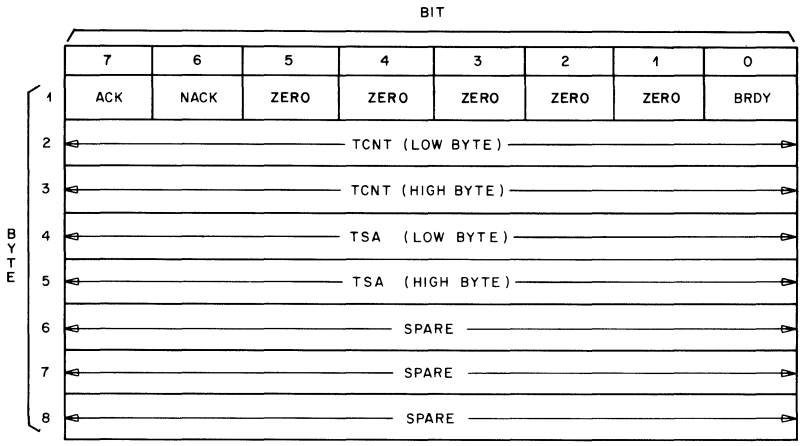


Figure 6. TLOOK Element

Table 10. TLOOK Element Definitions

Reg	Bit	Symbol	Name/Description
1	0	BRDY	**Buffer Ready.** Setting this bit indicates to the XPC-8 that data associated with this element is ready to be transmitted. BRDY should be the last bit of the TLOOK element to be set by the CPU after preparing a buffer. The SEND bit of the command register should then be set to command the XPC-8 to begin transmitting packets. The XPC-8 clears BRDY and sets NACK after all of the data associated with this element has been accessed by DMA and loaded into the transmitter FIFO.
1	1—5	—	**Zero.** These bits should be cleared.
1	6	NACK	**Not Acknowledged.** The XPC-8 sets NACK and clears BRDY after all the data associated with this look-up element has been accessed and loaded into the transmitter FIFO. The XPC-8 clears this bit when the frame associated with this element has been acknowledged.
1	7	ACK	**Acknowledged.** The XPC-8 sets ACK and clears NACK when an acknowledgment is received for the packet associated with this look-up element. An XBA interrupt is generated to notify the CPU of one or more acknowledgments.
2	0—7	TCNT (low byte)	**Transmit Count.** The number of bytes in a transmit data packet is specified by this 16-bit number. The X.25 protocol standard limits the number of bytes in an information field to 4 K + 4 (including the packet header) and, therefore, bits 6 and 7 of byte 3 should always be cleared.
3	0—7	TCNT (high byte)	
4	0—7	TSA (low byte)	**Transmit Start Address.** This 16-bit number is the location in system memory of the first byte of transmit data associated with this TLOOK element.
5	0—7	TSA (high byte)	
6—8	0—7	—	**Reserved.** Not used.

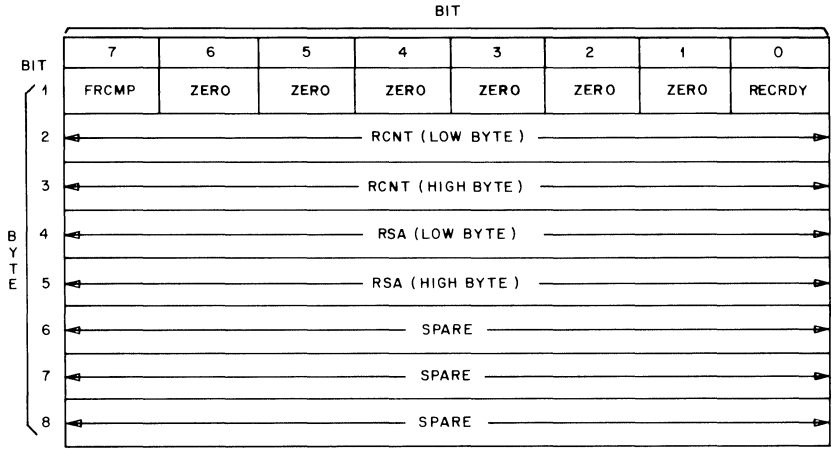


Figure 7. RLOOK Element

Table 11. RLOOK Element Definitions

Reg	Bit	Symbol	Name/Description
1	0	RECRDY	**Receiver Ready.** Setting this bit indicates to the XPC-8 that the data buffer associated with this element is ready to receive data. The receive start address field of the RLOOK element should be specified before the CPU sets the RECRDY bit. After the XPC-8 receives a valid packet and stores the information field in the buffer associated with the look-up element, it clears RECRDY and sets FRCMP.
1	1—6	—	**Zero.** These bits should be cleared.
1	7	FRCMP	**Frame Complete.** When a valid packet is received, the XPC-8 writes the receive count, clears RECRDY, and sets FRCMP. A PKR interrupt is used to notify the CPU of the received packet.
2	0—7	RCNT (low byte)	**Receiver Count.** This 16-bit number specifies how many bytes of system memory have been filled by the receive packet. The XPC-8 writes this location after a valid information frame has been received and written to system memory without error.
3	0—7	RCNT (high byte)	
4	0—7	RSA (low byte)	**Receive Start Address.** This 16-bit number specifies the address in system memory of the first byte of receive data in the packet. This address is written only by the CPU.
5	0—7	RSA (high byte)	
6—8	0—7	—	**Reserved.** Not used.

DMA Operation

DMA on the XPC-8 is used to read and write data fields of I frames, data fields of XID frames, and the TLOOK and RLOOK tables in system memory. To initiate a DMA cycle, the XPC-8 requests the use of the data bus by forcing $\overline{\text{DREQ}}$ low. The host CPU signifies that the bus is available for use by the XPC-8 by forcing $\overline{\text{DACK}}$ low. This allows $\overline{\text{DSRE}}$, $\overline{\text{WE}}$, R/$\overline{\text{W}}$, $\overline{\text{AS}}$, and A0—A15 to become outputs.

Once the XPC-8 has control of the system bus, it expects to have use of the bus until it finishes its DMA operations. The XPC-8 holds the system bus for a maximum of 5 read or write cycles.

Slow memory handshaking is provided through the $\overline{\text{READY}}$ input. A read or a write continues until $\overline{\text{READY}}$ goes low. A DMA write cycle must not extend more than 100 μs.

Parity checks are not performed on-chip. The results of any off-chip parity checking schemes should be supplied through $\overline{\text{PARV}}$. $\overline{\text{PARV}}$ is sampled on the falling edge of the CKO cycle following the detection of valid $\overline{\text{READY}}$. If $\overline{\text{PARV}}$ is sampled low, parity is assumed to be valid. If $\overline{\text{PARV}}$ is high, the XPC-8 makes a second attempt to complete the read or write operation. If the second attempt also fails, a hard parity error interrupt is generated and DMA operations halts. $\overline{\text{PARV}}$ should be tied low if parity is not being checked.

A priority DMA scheme can be implemented with no additional hardware in a daisy-chain fashion for multiple XPC-8 applications. The $\overline{\text{DREQ}}$ of the lowest priority XPC-8 is tied to the $\overline{\text{LPDREQ}}$ input of the next highest priority XPC-8. The $\overline{\text{DREQ}}$ of the highest priority XPC-8 is tied to the $\overline{\text{BUSREQUEST}}$ input of the CPU. The $\overline{\text{BUSGRANT}}$ output of the CPU is tied to the $\overline{\text{DACK}}$ of the highest priority XPC-8. The $\overline{\text{LPDACK}}$ of the highest priority XPC-8 is tied to $\overline{\text{DACK}}$ of the next highest priority XPC-8 and this continues until the lowest priority XPC-8 is reached. The $\overline{\text{LPDREQ}}$ of the lowest priority XPC-8 must be tied high (see Figure 8).

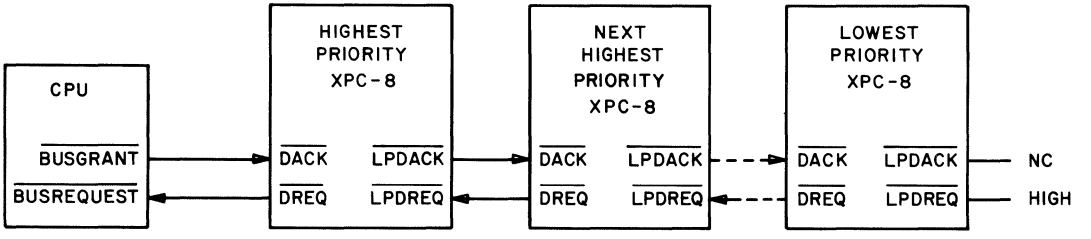


Figure 8. DMA Priority Scheme Interconnection

Test Modes

The XPC-8 has four test modes: near-end loopback, far-end loopback, echo, and output 3-state.

The near-end loopback test permits the XPC-8 to talk to itself. The transmitter output and receiver input are internally connected while in this mode of operation. The receiver automatically interchanges the command and response addresses to allow the protocol to function properly.

The far-end loopback test is used to check the near-end XPC-8 and the data link. The local XPC-8 is placed in far-end loopback test mode, while the remote XPC-8 is placed in echo mode. The receiver in the local XPC-8 interchanges the command and response addresses. Data arriving at the remote XPC-8, which is in the echo mode, is internally routed without CPU or XPC-8 intervention to the transmitter data output.

Output buffers are 3-stated whenever $\overline{\text{MR}}$ is forced low. This feature should be used during board testing/debugging.

Characteristics

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input voltage:					
low	V_{IL}	—	0.8	V	—
high	V_{IH}	2.2*	—	V	—
Output voltage:					
low	V_{OL}	—	0.4	V	I_{OL} = 2.2 mA
high	V_{OH}	2.4	—	V	I_{OH} = −400 μA
Power supply current	I_{DD}	—	460	mA	—
Output off current:					
low	I_{OZL}	—	−10	μA	V_{OL} = 200 mV
high	I_{OZH}	—	10	μA	V_{OH} = 5.25 V
Power dissipation	PD	—	2.2	W	V_{DD} = 5.0 V

* MOS input level.

Maximum Ratings

Voltage range on any pin with respect to ground ..... −0.5 to +7 V
Ambient operating temperature (T_A) range ..... 0 to 70 °C
Storage temperature (Tstg) range ..... 0 to 85 °C
Power dissipation (PD) ..... 2.5 W

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Table 12. DMA Timing

Symbol	Description	Min	Max	Unit
tCKOHASH	$\overline{AS}$ release offset	—	125	ns
tCKOHASL	$\overline{AS}$ offset	—	102	ns
tCKOLAV	Address settle time	—	92	ns
tCKOLAZ	Address disable offset	—	160	ns
tCKOHCKOH	CKO period	400	8000	ns
tCKOLDRH	$\overline{DREQ}$ release offset	—	95	ns
tCKOLDRL	$\overline{DREQ}$ offset	—	140	ns
tCKOHDV	Data valid offset	—	200	ns
tCKOHREH	$\overline{RE}$ release offset	—	160	ns
tCKOLDSH	$\overline{DS}$ release offset (write)	—	100	ns
tCKOHDSH	$\overline{DS}$ release offset (read)	—	160	ns

Table 12. DMA Timing (Continued)

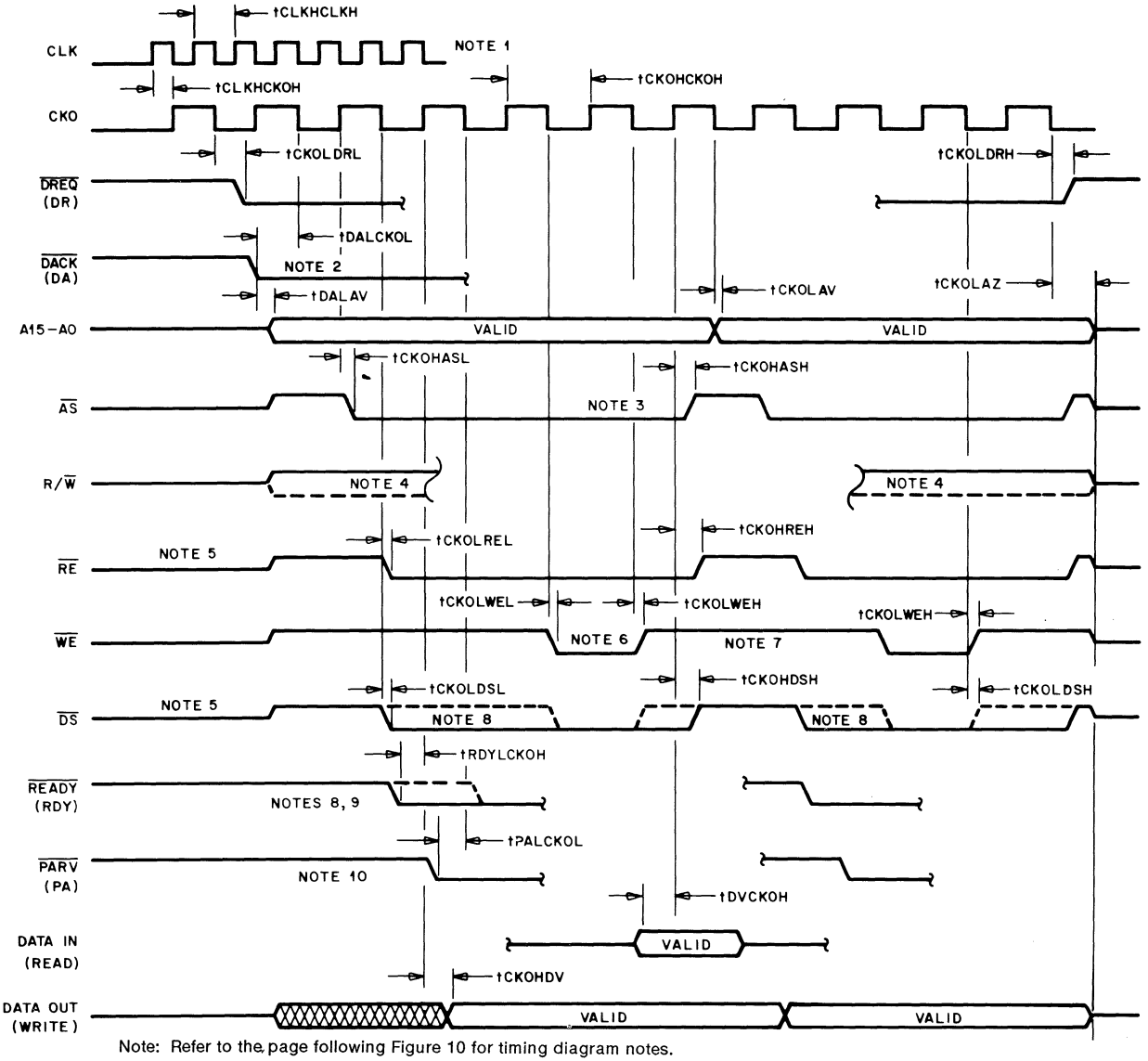
Symbol	Description	Min	Max	Unit
tCKOLDSL	$\overline{DS}$ low offset (Motorola, read)	—	44	ns
tCKOLDSL	$\overline{DS}$ low offset (Motorola, write)	—	44	ns
tCKOLREL	$\overline{RE}$ low offset (Intel, read)	—	44	ns
tCKOLWEH	$\overline{WE}$ release offset	—	70	ns
tCKOLWEL	$\overline{WE}$ low offset (Intel, write)	—	34	ns
tCLKHCKOH	CLK offset	—	130	ns
tCLKHCLKH	CLK period	200	4000	ns
tDALAV	Address enable offset	—	135	ns
tDALCKOL	$\overline{DACK}$ set-up time	230	—	ns
tDVCKOH	Data set-up time	170	—	ns
tPALCKOL	$\overline{PARV}$ set-up time	180	—	ns
tRDYLCKOH	$\overline{READY}$ set-up time	145	—	ns

Table 13. CPU Read and Write Timing

Symbol	Description	Min	Max	Unit
tAVCSL	Address valid before $\overline{CS}$ low (address set-up)	0	—	ns
tDSLDV	$\overline{DS}$ low to data valid (access time)	—	150	ns
tRELDV	$\overline{RE}$ low to data valid (access time)	—	150	ns
tDSHDZ	$\overline{DS}$ high to data 3-state	—	190	ns
tREHDZ	$\overline{RE}$ high to data 3-state	—	190	ns
tCKOHRDYH	$\overline{READY}$ release offset (read)	—	250	ns
tCKOHRDYH	$\overline{READY}$ release offset (write)	—	345	ns
tCKOHRDYL	$\overline{READY}$ active offset (read)	—	160	ns
tCKOHRDYL	$\overline{READY}$ active offset (write)	—	160	ns
tCSLCKOL	$\overline{CS}$ set-up time	390	—	ns
tDSHRWV	$\overline{DS}$ release to R/$\overline{W}$ change	50	—	ns
tRWVDSL	R/$\overline{W}$ release to $\overline{DS}$ change	90	—	ns
tDSHCKOL	$\overline{DS}$ release set-up time	390	—	ns
tDSLCKOL	$\overline{DS}$ set-up time	212	—	ns
tDSHAX	$\overline{DS}$ high to address change	0	—	ns
tAVDSL	Address valid Before $\overline{DS}$ low (address set-up)	0	—	ns
tDVCKOH	Data set-up time	0	—	ns
tDXCKOH	Data hold time	155	—	ns
tREHCKOL	$\overline{RE}$ release set-up time	390	—	ns
tRELCKOL	$\overline{RE}$ set-up time	212	—	ns
tREHAX	$\overline{RE}$ high to address change	0	—	ns
tAVREL	Address valid before $\overline{RE}$ low (address set-up)	0	—	ns
tWEHCKOL	$\overline{WE}$ release set-up time	280	—	ns
tWELCKOL	$\overline{WE}$ set-up time	250	—	ns
tWEHAX	$\overline{WE}$ high to address change	0	—	ns
tAVWEL	Address valid before $\overline{WE}$ low (address set-up)	0	—	ns

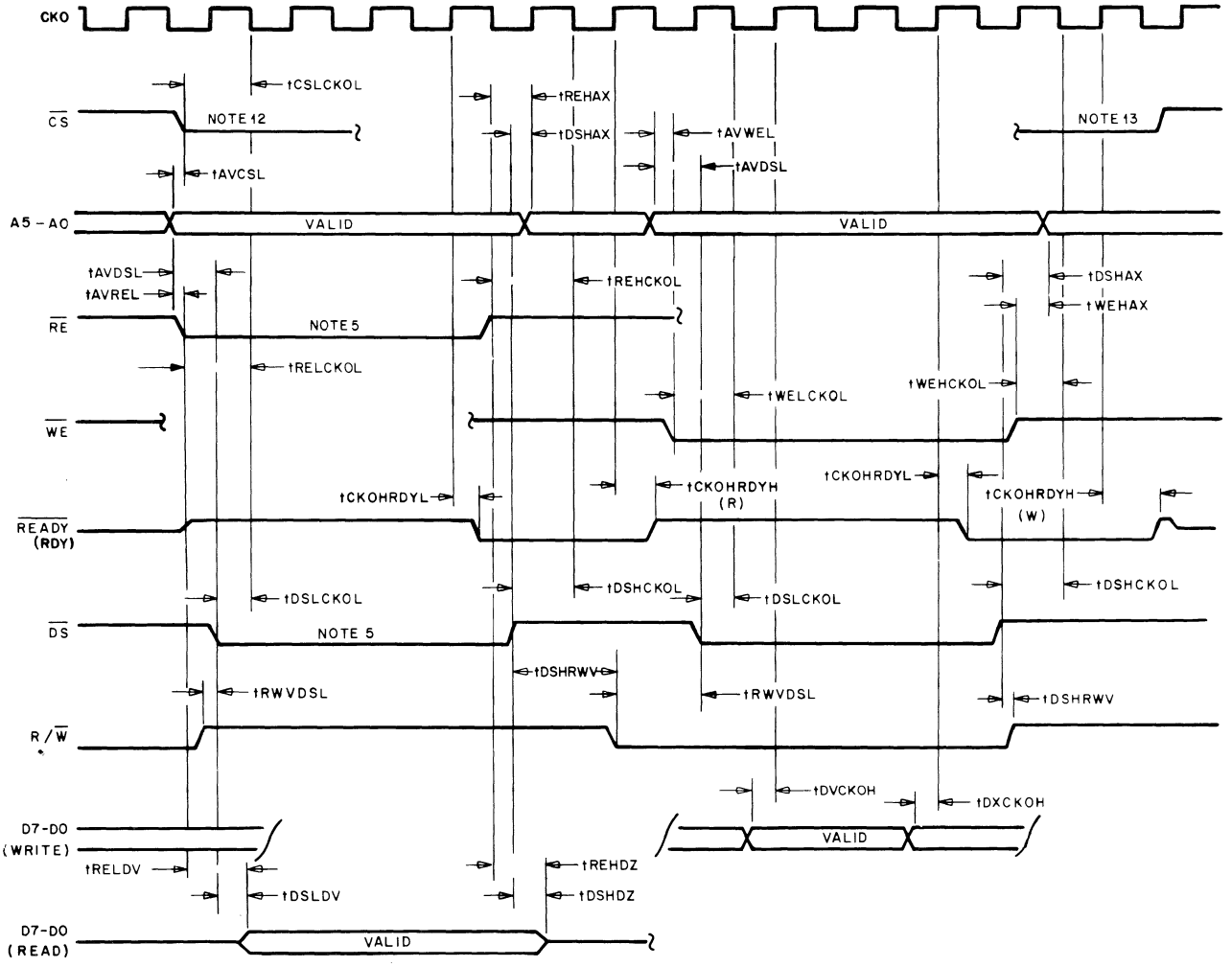
Table 14. Reset Timing

Symbol	Description	Min	Max	Unit
tMRHMRH	Time allowed for switching to Intel bus mode (Intel)	—	30tCKOHCKOH	—
tMRHMRL	Time between reset pulses (Intel)	6tCKOHCKOH	—	—
tMRLMRH	Valid reset time (Motorola and Intel)	6tCKOHCKOH	—	—
tPU	Power-up delay time (Motorola and Intel)	40tCKOHCKOH	—	—



Note: Refer to the page following Figure 10 for timing diagram notes.

Figure 9. DMA Timing Diagram

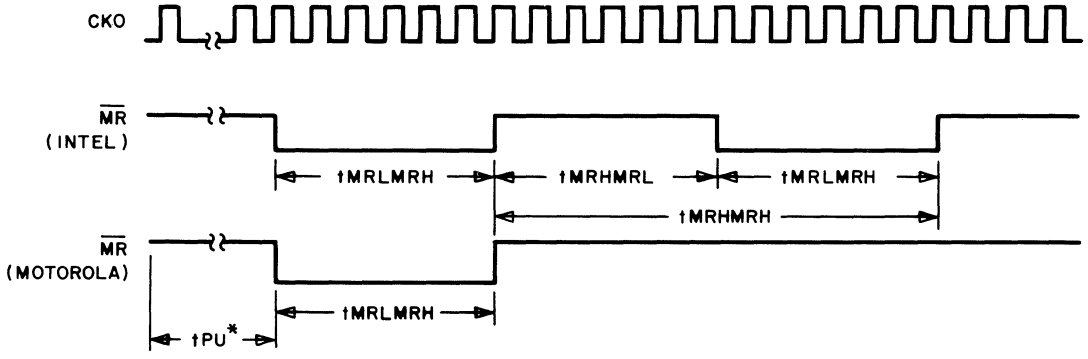


Note: Refer to the page following Figure 10 for timing diagram notes.

Figure 10. CPU Read and Write Cycles

Timing Diagram Notes for Figures 9 and 10

1. CLK must have a duty cycle of between 45% and 55%.
2. $\overline{DACK}$ is sampled on every falling edge of CKO until it tests low.
3. Read or write cycles can extend for one extra CKO cycle to allow for internal synchronization.
4. R/$\overline{W}$ is valid by the first falling edge of $\overline{AS}$. The dotted line is for write cycle only. Entire DMA cycle is for either a read or a write.
5. $\overline{DS}$ and $\overline{RE}$ are multiplexed on the same pin. $\overline{RE}$ is selected for the Intel bus configuration; $\overline{DS}$ is selected for the Motorola bus configuration.
6. The write cycle must not be extended (using $\overline{READY}$) for more than 100 μs.
7. If a $\overline{PARV}$ error occurs, the trailing edge of $\overline{WE}$ is concurrent with the trailing edge of $\overline{AS}$.
8. The dotted line is for write only.
9. $\overline{READY}$ is sampled on every rising edge of CKO until it tests low.
10. $\overline{PARV}$ is sampled on the falling edge of CKO following the detection of a valid $\overline{READY}$.
11. During TLOOK and RLOOK element reads, the read cycles are extended an additional two CKO cycles.
12. Due to internal synchronization, there may be an extra CKO cycle inserted before the falling edge of $\overline{READY}$.
13. Forcing $\overline{CS}$ high while executing a read or write cycle ends that cycle.



* Time required from power-up to the first reset.

Figure 11. Motorola and Intel Reset Sequences

T7102A-X.25/X.75 Protocol Controller

Features

- 24-bit address bus to address a 16-Mbyte address space
- Dual-channel DMA with standard interface, including DMA request, DMA acknowledge, DMA read, and DMA write
- Independently programmable T1 and T4 timers
- Programmable retransmission counter
- Transmit and receive buffers accessed indirectly through a look-up table
- Programmable modulo-8 or modulo-128 frame sequence numbering
- Programmable window size (transmit and receive)
- Selectable 16-bit (CRC-CCITT) or 32-bit polynomial for frame checking sequence (FCS)
- Wait-state generator (on DMA side) for slow memory
- Programmable interframe flag fill
- Error detection and automatic recovery via packet retransmission
- Link initialization and supervision
- Independently programmable transmit and receive window size
- Password exchange mechanism for dial-up operation
- Programmable for X.25 or X.75 operation
- Supports 8-bit or 16-bit data buses
- Intel, Motorola, or *WE* 32100 Microprocessor DMA interface (data bus)
- Sixteen programmable event counters, with optional interrupt capability
- Daisy-chain DMA structure for priority-controlled CPU interfaces
- Two independent test modes (far-end loopback and near-end loopback) to verify the XPC and its link
- Optional parity generation and checking across data bus interface on all DMA operations
- Six bidirectional address leads for accessing 51 internal XPC registers
- 2-MHz clock
- Single 5 V supply

Description

The T7102A X.25/X.75 Protocol Controller (XPC) integrated circuit is an X.25/X.75 level 2 protocol controller. It is a single-chip LSI device available in a 70-pin pin-grid-array (PGA) package and is fabricated using N-channel silicon gate MOS technology. The T7102A XPC implements an augmented X.25 level 2 data communications standard for packet switching. The device satisfies the X.25 link level (level 2) requirements for a balanced link access procedure (LAPB) for data interchange over a synchronous full-duplex serial data link. The device also implements X.75 level 2 protocol, which is used in internetwork applications. The protocol controller is bit-oriented, with a maximum transmit and receive speed of 333 kb/s. A set of programmable registers controls and records vital events during data transmission.

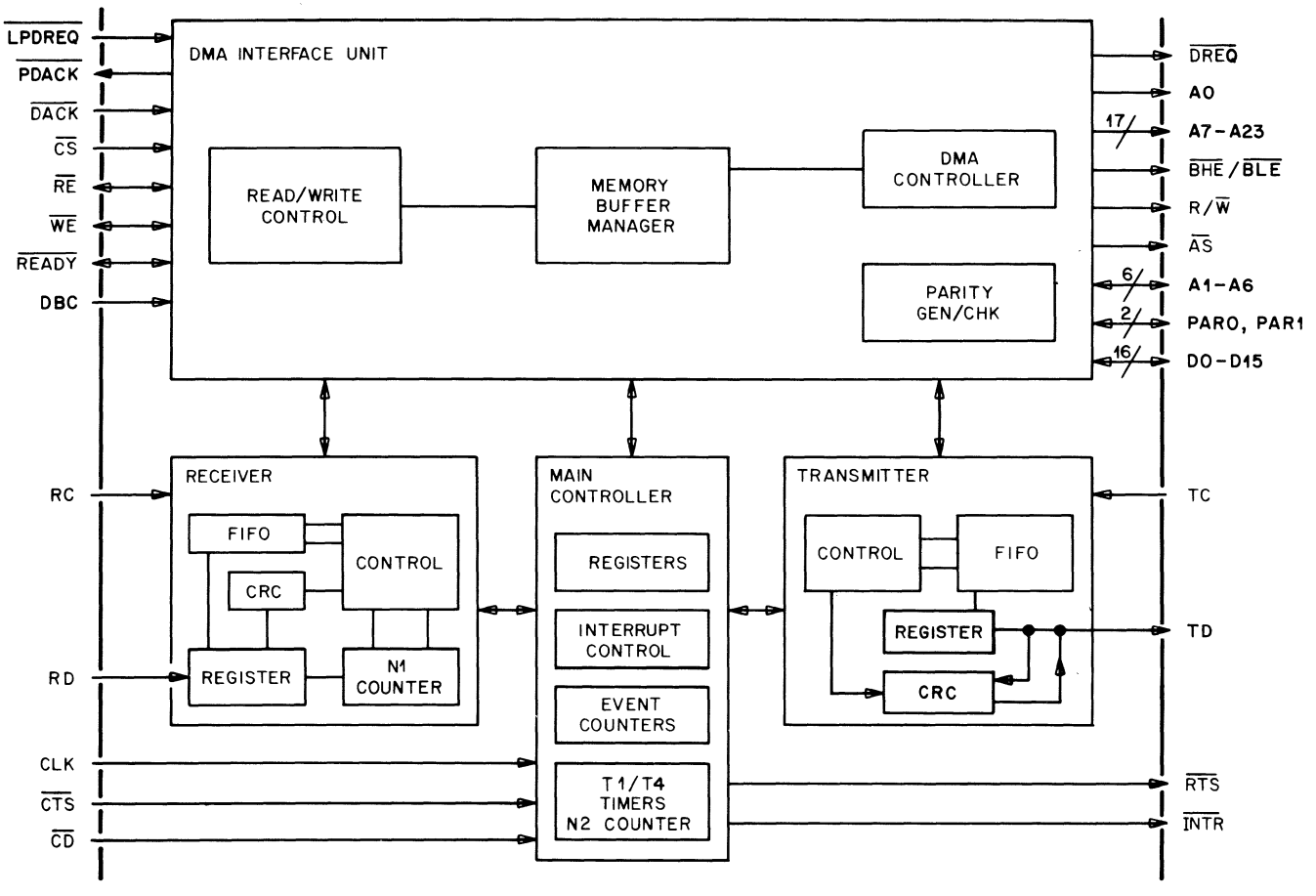
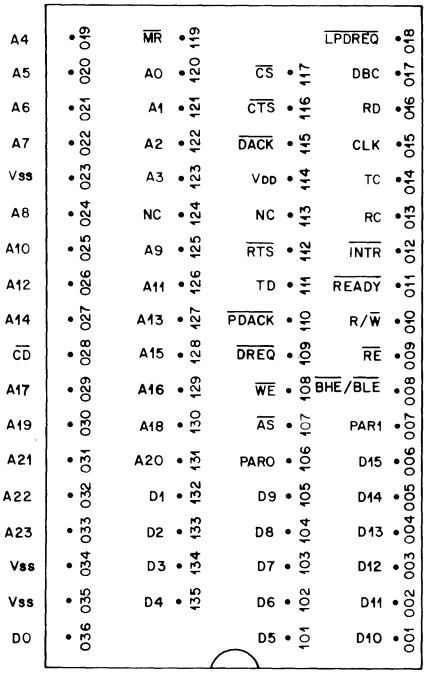


Figure 1. Block Diagram

User Information

Pin Descriptions



Sym	Pin	Sym	Pin	Sym	Pin
A0	120	A23	33	D15	6
A1	121	$\overline{AS}$	107	$\overline{DACK}$	115
A2	122	$\overline{BHE}$/	8	DBC	17
A3	123	$\overline{BLE}$		$\overline{DREQ}$	109
A4	19	$\overline{CD}$	28	$\overline{INTR}$	12
A5	20	CLK	15	$\overline{LPDREQ}$	18
A6	21	$\overline{CTS}$	116	$\overline{MR}$	119
A7	22	$\overline{CS}$	117	PAR0	106
A8	24	D0	36	PAR1	7
A9	125	D1	132	$\overline{PDACK}$	110
A10	25	D2	133	RC	13
A11	126	D3	134	RD	16
A12	26	D4	135	$\overline{RE}$	9
A13	127	D5	101	$\overline{READY}$	11
A14	27	D6	102	$\overline{RTS}$	112
A15	128	D7	103	R/$\overline{W}$	10
A16	129	D8	104	TC	14
A17	29	D9	105	TD	111
A18	130	D10	1	VDD	114
A19	30	D11	2	Vss	23,34,
A20	131	D12	3		35
A21	31	D13	4	$\overline{WE}$	108
A22	32	D14	5		

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	D10	I/O*	**Data Bus Bit 10.**
2	D11		**Data Bus Bit 11.** If DBC (pin 17) is high, a 16-bit data bus (pins 1—6,
3	D12		**Data Bus Bit 12.** 36, 101—105, and 132—135) is used; if DBC is low,
4	D13		**Data Bus Bit 13.** an 8-bit data bus (pins 36, 101—103, and 132—135)
5	D14		**Data Bus Bit 14.** is used.
6	D15		**Data Bus Bit 15.**
7	PAR1	I/O*	**Parity on High Data Byte.** Parity generation and checking of high byte of data bus. Valid only during DMA operations.
8	$\overline{BHE}$/$\overline{BLE}$	O*	**Byte High Enable (Active Low).** The XPC uses this line to control access to the high data byte when it has a 16-bit data bus. Access is to the low data byte in the Motorola configuration (see Table 18).
9	$\overline{RE}$	I/O*	**Read Enable (Active Low).** An input during CPU access of XPC registers; an output during DMA read cycles.

* Indicates 3-state condition.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
10	R/$\overline{W}$	O*	**Read or Write (Active Low).** If low, the XPC wants to write to main memory; if high, the XPC wants to read from main memory. Not used during internal XPC register read/write operations.
11	$\overline{READY}$	I/O*	**Ready (Active Low).** This signal is used as an input during DMA read and write cycles to allow slow memory to be accessed. During DMA operations, $\overline{RE}$ and $\overline{WE}$ (pins 9 and 108) remain low as long as $\overline{READY}$ is held high. During CPU read/write operations of internal XPC registers, $\overline{READY}$ is an output. It goes low to signal the CPU that the read/write operation is complete.
12	$\overline{INTR}$	O	**Interrupt Request (Active Low).** This signal indicates that the XPC is requesting service. It returns high when the CPU reads the interrupt register.
13	RC	I	**Receive Clock.** Data is received at this frequency.
14	TC	I	**Transmit Clock.** Data is transmitted at this frequency.
15	CLK	I	**Clock.** This pin controls the internal sequencing of the chip. The clock must be a square wave with a minimum frequency of 250 kHz and a maximum frequency of 2 MHz ($f_{CLK} \geq 6f_{RC}$ and $f_{CLK} \geq 6f_{TC}$).
16	RD	I	**Receive Data.** Serial data input line.
17	DBC	I	**Data Bus Configuration.** This pin must be wired to V_{SS} or V_{DD} to configure the XPC data bus for 8-bit or 16-bit operation, respectively.
18	$\overline{LPDREQ}$	I	**Low-Priority DMA Request (Active Low).** This pin is used to daisy-chain DMA requests in systems without a bus arbiter that use more than one XPC. Tie high on lowest priority XPC in the daisy chain.
19	A4	I/O*	If $\overline{CS}$ (pin 117) is low, A1—A6 (pins 19—21 and 121—123) are inputs used to address the XPC internal registers; if $\overline{CS}$ is high, all pins of the 24-bit address bus (pins 19—22, 24—27, 29—33, 120—123, and 125—131) are outputs used to address system memory. **Address Bus Bit 4.**
20	A5	I/O*	**Address Bus Bit 5.**
21	A6	I/O*	**Address Bus Bit 6.**
22	A7	O*	**Address Bus Bit 7.**
23	V_{SS}	O	**Ground.**
24	A8	O*	**Address Bus Bit 8.**
25	A10		**Address Bus Bit 10.**
26	A12		**Address Bus Bit 12.** See description of pins 19—22.
27	A14		**Address Bus Bit 14.**
28	$\overline{CD}$	I	**Carrier Detect (Active Low).** $\overline{CD}$ generates two interrupts to notify the host of level 1 activity. No further processing is done by the XPC.
29	A17	O*	**Address Bus Bit 17.**
30	A19		**Address Bus Bit 19.**
31	A21		**Address Bus Bit 21.** See description of pins 19—22.
32	A22		**Address Bus Bit 22.**
33	A23		**Address Bus Bit 23.**
34	V_{SS}	—	**Ground.**

* Indicates 3-state condition.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
35	VSS	—	**Ground.**
36	D0	I/O*	**Data Bus Bit 0.** See description of pins 1—6.
101	D5		**Data Bus Bit 5.**
102	D6		**Data Bus Bit 6.**
103	D7		**Data Bus Bit 7.**
104	D8		**Data Bus Bit 8.**
105	D9		**Data Bus Bit 9.**
106	PAR0	I/O*	**Parity on Low Data Byte.** Parity generation and checking of low byte of data bus. Valid only during DMA operations.
107	$\overline{AS}$	O*	**Address Strobe (Active Low).** The XPC uses this signal during DMA operations to indicate that it has placed a valid address on the address bus.
108	$\overline{WE}$	I/O*	**Write Enable (Active Low).** Used as an input during CPU access of XPC registers. Output during DMA write cycles.
109	$\overline{DREQ}$	O	**DMA Request (Active Low).** A low on this pin indicates to the CPU that the XPC needs the address bus and the data bus for DMA cycles.
110	$\overline{PDACK}$	O	**Propagated DMA Acknowledge (Active Low).** This pin is used to daisy-chain acknowledgments in systems using more than one XPC. $\overline{PDACK}$ output of one XPC connects to $\overline{DACK}$ input of the next lower priority XPC.
111	TD	O	**Transmit Data.** XPC serial data output line.
112	$\overline{RTS}$	O	**Request to Send (Active Low).** When asserted, this signal indicates to level 1 that the XPC is ready to transmit either data or flags over the link. $\overline{RTS}$ remains low while the link is up.
113	NC	—	**No Connection.**
114	VDD	—	**5 V Supply.**
115	$\overline{DACK}$	I	**DMA Acknowledge (Active Low).** When this signal is low, the CPU indicates that the XPC has been granted system buses. All floating outputs of the XPC then become TTL drivers. $\overline{DACK}$ must remain low until $\overline{DREQ}$ (pin 19) is removed.
116	$\overline{CTS}$	I	**Clear to Send (Active Low).** Level 1 interface notifies the XPC that the data set is ready to send by asserting this signal. The link cannot come up until $\overline{CTS}$ is asserted. $\overline{CTS}$ must remain asserted when the link is up.
117	$\overline{CS}$	I	**Chip Select (Active Low).** $\overline{CS}$ must be asserted to allow access to internal registers of the XPC. When $\overline{CS}$ is asserted, $\overline{RE}$, $\overline{WE}$, and A1—A6 become inputs and $\overline{READY}$ becomes an output.
119	$\overline{MR}$	I	**Master Reset (Active Low).** When this pin is asserted, all command, status, and parameter register bits are cleared (0) except for the mandatory disconnect (MDISC) and the DISCMODE bits in command register 0, which are set (1). $\overline{MR}$ must be high for at least two clock (CLK) periods after power-on. The minimum low time for reset is 1.5 CLK periods. All outputs are 3-stated when both $\overline{MR}$ and $\overline{CS}$ are low.

* Indicates 3-state condition.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
120	A0	O*	**Address Bus Bit 0.**
121	A1	I/O*	**Address Bus Bit 1.**
122	A2	I/O*	**Address Bus Bit 2.** See description of pins 19—22.
123	A3	I/O*	**Address Bus Bit 3.**
124	NC	—	**No Connection.**
125	A9	O*	**Address Bus Bit 9.**
126	A11		**Address Bus Bit 11.**
127	A13		**Address Bus Bit 13.**
128	A15		**Address Bus Bit 15.** See description of pins 19—22.
129	A16		**Address Bus Bit 16.**
130	A18		**Address Bus Bit 18.**
131	A20		**Address Bus Bit 20.**
132	D1	I/O*	**Data Bus Bit 1.**
133	D2		**Data Bus Bit 2.**
134	D3		**Data Bus Bit 3.** See description of pins 1—6.
135	D4		**Data Bus Bit 4.**

* Indicates 3-state condition.

Overview

The T7102A XPC performs complete link level control according to X.25 and X.75 data communications protocols. The device generates supervisory and unnumbered frames automatically, without intervention by the host. The host must supply buffers for the data fields of received and transmitted information frames. It is notified of important events via interrupts. The XPC contains a transmitter, receiver, controller, and an interface unit, as shown in Figure 1.

Architecture

Transmitter

The transmitter constructs frames on command from the main controller. The transmitter contains a transmitter controller, 4-byte FIFO (first-in first-out) buffer, holding register, cyclic redundancy check (CRC) encoder, and zero inserter. The transmitter handles the transmission of continuous flags, aborts, or idle channel indications automatically. Bit stuffing is implemented to ensure data transparency.

The transmitter FIFO and the transmitter holding register control the flow of information from main memory to the data link. The transmitter FIFO is used as temporary storage for data delivered from memory to the transmitter by the DMA controller. The DMA controller can read two bytes of data at a time from main memory and place them into the transmitter FIFO. The transmitter holding register is loaded in a parallel fashion from the transmitter FIFO. The various bytes needed to construct a frame are also loaded into the holding register. When the data is ready to be transmitted, it is shifted out serially through the transmit data (TD) lead on the negative edge of the transmit clock (TC).

The CRC encoder calculates the frame check sequence (FCS) and appends it to the data field, or to the control field for frames without data. The FCS is calculated over the address, control, and data fields. The zero inserter performs bit stuffing to ensure data transparency.

Receiver

The receiver processes incoming data and notifies the controller of received frames and other link conditions. The receiver contains a preprocessor, receiver controller, 4-byte FIFO, receiver register, and CRC decoder. The preprocessor detects flags, aborts, and idle conditions on the data link, and deletes the 0s that were added for data transparency. Receive data (RD) is latched on the positive edge of the receive clock (RC). Frames are identified and checked for proper format by the receiver controller.

The information field of a frame is loaded into the FIFO and is DMAed to memory by the interface unit.

The frame is checked for transmission errors by means of the CRC. The XPC acts on frames received error-free and discards frames received with errors. The XPC maintains the number of link errors in the counter registers.

Controller

The controller interprets results from the receiver, transmitter, and internal registers, and implements the actions of the protocol. The X.25/X.75 protocol block contains the logic used to implement the entire X.25/X.75 level 2 protocol. Specific tasks of the main controller include configuring the link as specified by the parameter and command registers, maintaining the status registers, analyzing received frames and taking appropriate action, logging certain events in the bank of 16 event counters, directing the transmitter to send specific commands or responses, directing the interface unit to acquire receive and transmit data buffers, managing timing directions, and using a set of interrupts to notify the host of data link conditions.

DMA Interface Unit

The interface unit provides the interface between main memory and the transmitter and receiver via 2-channel DMA. It consists of a data bus selector, parity generator and checker, address controller, read/write machine, data section, and DMA controller.

The data bus selector controls the width of the external data bus and data byte ordering. The external data bus can be set at either 8-or 16-bits wide by strapping DBC (pin 17) to V_{SS} or V_{DD}, respectively. The internal data bus is 8 bits wide. Data byte ordering is accomplished via parameter register 14, bit 0.

Parity is generated and checked for each byte of the data bus during DMA operations if parity is enabled. Parity is not checked or generated when the host accesses the XPC registers.

The address controller calculates and stores the addresses for the elements and buffer pointers for the transmit and receive channels.

The read/write machine generates the control signals to access data from memory, while the data section routes the data from memory to the transmit FIFO and from the receive FIFO to memory.

The DMA controller, on request from the controller, opens data buffers for the transmitter and receiver and controls the sequencing of the other sections.

A DMA priority scheme can be implemented in a daisy-chain fashion with no additional hardware for multiple XPC applications.

Loopback Test Control

The loopback test control connects the RD and TD pins, as required by the near-end loopback test, far-end loopback test, or echo mode.

Principles of Operation

CPU Interface

The CPU interface is used to specify commands to the XPC and to receive status information from the XPC. The XPC is a peripheral device that accepts commands from the CPU and provides interrupts and results to the CPU when necessary. Through the CPU interface, the CPU loads the command, parameter, and counter registers with the characteristics of the serial interface. The XPC provides status information and interrupts via the status and interrupt registers. The CPU accesses these registers via bits A1—A6 of the address bus. When $\overline{CS}$ is asserted, $\overline{RE}$, $\overline{WE}$, and A1—A6 become inputs and $\overline{READY}$ becomes an output. Only the low-order byte of the data bus is used for register read/write operations. The XPC ignores the upper byte during write operations and forces a 3-state condition on the upper data byte during read operations. The registers always appear on D0—D7, regardless of the byte ordering that is selected. Table 2 lists the register addresses for the XPC.

Master Reset

When the master reset ($\overline{MR}$) is asserted, the parameter registers are cleared, the command register is set to 82H (DISCMODE = 1, MDISC = 1), and the interrupt register is cleared. Status registers 9—13 and the counter registers are not initialized. $\overline{MR}$ must be high for at least two CLK periods after power-up. The minimum low time for reset is 1.5 CLK periods.

When the XPC detects a reset, it performs an internal reset sequence that requires eight CLK periods. After the reset sequence, the XPC enters a set-up state in which the CPU can configure the parameter and counter registers. While in the set-up state, the XPC transmits 1s and ignores any frames that are received. The XPC exits the set-up state and enters the operational state when the CPU clears MDISC in the command register.

In order to change parameter register values, either the XPC must be placed in the set-up state by a reset or the MDISC bit must be set while the XPC is in the operational state. An exception to this is parameter register 0, which can be configured only in the set-up state.

$\overline{MR}$ is also used with $\overline{CS}$ to provide board isolation capabilities. If $\overline{CS}$ is low when $\overline{MR}$ is asserted, $\overline{INTR}$, $\overline{RTS}$, TD, $\overline{DREQ}$, and $\overline{DACK}$ are placed in a high-impedance state; if $\overline{CS}$ is high when $\overline{MR}$ is asserted, these pins are not put in a high-impedance state. All other outputs are placed in a high-impedance state when $\overline{MR}$ is asserted, regardless of the state of $\overline{CS}$.

Registers

The XPC contains 51 addressable registers for controlling and observing its operational mode. The registers are divided into five types: command, status, interrupt, parameter, and counter.

Command Register. This register controls seven XPC functions: send, receive, mandatory disconnect, active or passive link initialization, password exchange, password verification, and disconnect. The command register can be written to at any time.

Status Registers. These 14 registers report the state of the XPC, input conditions, and other vital information regarding the XPC to the CPU, e.g., the values of the state variables V(S) and V(R).

Interrupt Register. This register's lower six bits present an encoded reason for a particular interrupt issued to the CPU; for example, packet received, parity error, idle link detected, and frame reject. This register is backed up by a 4-word FIFO, which enables several interrupts to occur before the CPU can service the XPC. Bit 7 contains a lost interrupt bit, which is independent of the LSTIN bit in status register 0 and is implicitly cleared after a read of the interrupt register. If no interrupts are pending, the interrupt register contains 00H.

Parameter Registers. These 17 registers determine system constants and the mode of operation, for example, the period of the T1 and T4 timers and the address of the TLOOK table. The XPC can also be put into a test mode to test either itself or itself and the link. These registers can be written to only when MDISC is set. An exception to this is parameter register 0, which can be configured only in the set-up state.

Counter Registers. These 18 down-counter registers monitor 16 different events on the data link; for example, the number of rejected frames received, the number of times timer T1 expired, and the number of parity errors generated. The counter registers can be written to at any time.

Table 2. XPC Register Address Offsets

Address				Address			
Hex	Dec	Status*	Name	Hex	Dec	Status*	Name
00	0	R/W	Command register	34	52	R/W	Parameter register 10
02	2	R	Status register 0	36	54	R/W	Parameter register 11
04	4	R	Status register 1	38	56	R/W	Parameter register 12
06	6	R	Status register 2	3A	58	R/W	Parameter register 13
08	8	R	Status register 3	3C	60	R/W	Parameter register 14
0A	10	R	Status register 4	3E	62	R/W	Parameter register 15
0C	12	R	Status register 5	40	64	R/W	Counter register 0
0E	14	R	Status register 6	42	66	R/W	Counter register 1
10	16	R	Status register 7	44	68	R/W	Counter register 2
12	18	R	Status register 8	46	70	R/W	Counter register 3
14	20	R	Status register 9	48	72	R/W	Counter register 4
16	22	R	Status register 10	4A	74	R/W	Counter register 5
18	24	R	Status register 11	4C	76	R/W	Counter register 6
1A	26	R	Status register 12	4E	78	R/W	Counter register 7
1C	28	R	Status register 13	50	80	R/W	Counter register 8
1E	30	R	Interrupt register	52	82	R/W	Counter register 9
20	32	R	Parameter register 0	54	84	R/W	Counter register 10
22	34	R/W**	Parameter register 1	56	86	R/W	Counter register 11
24	36	R/W	Parameter register 2	58	88	R/W	Counter register 12
26	38	R/W	Parameter register 3	5A	90	R/W	Counter register 13
28	40	R/W	Parameter register 4	5C	92	R/W	Counter register 14
2A	42	R/W	Parameter register 5	5E	94	R/W	Counter register 15
2C	44	R/W	Parameter register 6	60	96	R/W	Counter register 16
2E	46	R/W	Parameter register 7	62	98	R/W	Counter register 17
30	48	R/W	Parameter register 8	64	100	R/W	Parameter register 16
32	50	R/W	Parameter register 9				

* Read/write (R/W) or read-only (R) status.
** Parameter registers can be written only when MDISC is set.

Table 3. Command Register Definitions

Bit	7	6	5	4	3	2	1	0
Field	DISCMODE	PWOK2	PWOK1	PWXCH	ACT/PAS	RECR	MDISC	SEND

Bit	Symbol	Name/Description
0	SEND	**Send.** Controls transmission of packets. If cleared, inhibits XPC from sending new packets; if set, enables XPC to send new packets. The XPC clears this bit if the link goes down or if the next transmit element is not ready. Retransmissions occur automatically, regardless of the send bit state.
1	MDISC	**Mandatory Disconnect.** Selects whether the XPC brings the link up or remain disconnected. If cleared, the XPC brings the link up; if set, the XPC transmits all 1s during fill times and remains disconnected. If the XPC is in the information transfer phase when MDISC is set, it transmits a DISC frame and exits the information transfer phase. Interrupt generation is disabled when MDISC is set and NOTDISC (status register 0) is cleared. MDISC is set during a master reset (see Table 4).
2	RECR	**Receiver Ready.** Indicates availability of receiver buffers. If cleared, no receiver buffers are available. If set, receiver buffers are allocated and available. The XPC clears this bit if the receiver overruns, if the buffer chain segment is not ready, or if the receive element referenced by V(R) is not ready. If cleared while the XPC is in the information transfer phase, the XPC enters the station busy state and ignores all incoming I frames.
3	ACT/PAS	**Active/Passive.** Specifies XPC action in the disconnected phase. If cleared, the XPC passively awaits link set-up; if set, the XPC actively initiates link set-up (see Table 4).
4	PWXCH	**Password Exchange.** Determines which end of the link initiates password exchange. If cleared, the other end of link initiates password exchange; if set, the XPC initiates password exchange.
5, 6	PWOK1, PWOK2	**Password Verified.** Enables the host to notify the XPC about the correct action to take in response to a received password. Bits 4, 5, and 6 are interpreted as: **Code** (b6 b5 b4) — **Condition** 0 1 0 — Valid password command received 0 1 1 — Valid password response received 1 0 0 — Valid password command not received 1 0 1 — Valid password response not received
7	DISCMODE	**Disconnect Mode.** Specifies a disconnected state. DISCMODE is set during a master reset. DISCMODE must be set for passive link initialization and must be cleared for XID operation (see Table 4).

Table 4. Disconnected Phase Operation

Protocol State	XIDEN[1]	DISCMODE	ACT/PAS[2]	MDISC	Description
S0	0	x	x	1[3]	Does not respond to received frames until MDISC is cleared.[4] Responds to P-bit frame with DM final.[5]
S0	0	0	0	0	Responds to P-bit frame with DM final.[6]
S1	0	1	0	0	Link can be initialized by remote DXE.
x	0	x	1	0	Initiates link set-up.
S0	1	0	0	0	Waits for XID transfer.
S0	1	0	1	0	Initiates XID transfer.
S0	1	0	x	1	Does not respond to received frames until MDISC is cleared.
x	1	1	x	x	Do not use.

Note: x = don't care.
1 Password enable bit in parameter register 1.
2 Use PWXCH instead of ACT/PAS if XIDEN is 1.
3 Interframe fill is idle (all 1s).
4 MDISC not yet cleared after reset.
5 MDISC previously cleared after reset.
6 Interframe fill is flags.

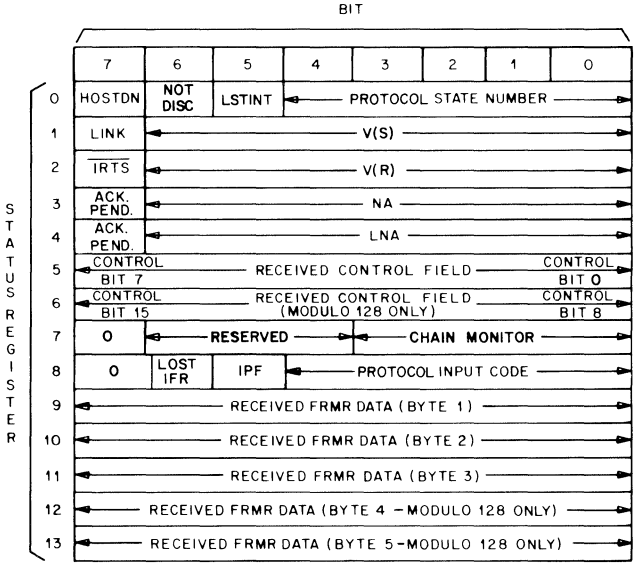


Figure 3. Status Registers

Table 5. Status Registers

Reg	Bit	Symbol	Name/Description
0	0—4	PSN	**Protocol State Number.** Encoding of protocol state (see Table 6).
0	5	LSTINT	**Lost Interrupt.** Indicates if interrupts were lost. If cleared, no interrupts were lost. If set, interrupt register FIFO overflowed and interrupts were lost. This bit is implicitly cleared after a read of status register 0.
0	6	NOTDISC	**Not Disconnected.** This bit is cleared if the XPC is disconnected or in XID phase. It is set when the device is in the link set-up or information transfer phase (protocol state $\geq$ S3). Interrupt generation is disabled when NOTDISC is cleared and MDISC (command register) is set.
0	7	$\overline{\text{HOSTD}}$	**Host Done (Active Low).** Allows the internal host done bit to be monitored in the event that the interrupt informing the host of a link-down condition was lost. If set, the host must reassign transmit and receive buffers before link reinitialization is permitted. The XPC sets this bit when an SABM frame is received while the XPC is in the information transfer phase (LINK = 1) or when the XPC exits the information transfer phase (LINK = 0). This bit is cleared by writing to status register 0 or parameter register 1.
1	0—6	V(S)	**Send State Variable.** The sequence number, N(S), of the next I frame to be transmitted and an index into the TLOOK table to access the buffer containing data for that frame.
1	7	LINK	**Link.** Indicates the status of the transmission link. If cleared, information transfer is not possible; if set, the XPC is in the information transfer phase (protocol state S6).
2	0—6	V(R)	**Receive State Variable.** The expected value of the sequence number, N(S), of the next I frame to be received and an index into the RLOOK table for the receiver buffer associated with that packet.
2	7	$\overline{\text{IRTS}}$	**Internal Request to Send.** Indicates that the XPC wants to acquire the link. If cleared, XPC wants link; if set, XPC does not want link.
3	0—6	NA	**Next Acknowledgment Expected.** Number of earliest unacknowledged packet. If no outstanding packets, NA = V(S).
3	7	ACKPEND	**Acknowledgments Pending.** This bit is set when the DMA has received acknowledgment processing to do. When all appropriate TLOOK elements have been updated, this bit is cleared. Before the host clears $\overline{\text{HOSTD}}$ or reallocates transmit buffers, it must check that this bit is cleared.
4	0—6	LNA	**Last Next Acknowledgment Expected.** Whenever NA is updated, the old value of NA is saved here. NA and LNA can be used to determine how many transmit data buffers have been acknowledged by the remote DXE and subsequently freed by the XPC.
4	7	ACKPEND	**Acknowledgment Pending.** See ACKPEND description above.

Table 5. Status Registers (Continued)

Reg	Bit	Symbol	Name/Description
5	0—7	RCF	**Received Control Field.** Holds the control field of the most recently received error-free frame.
6	0—7	RCF	**Received Control Field.** Holds the second byte of the control field in modulo-128 mode only. If in modulo-8 (normal sequencing), this register is always cleared.
7	0—3	CHMON	**Chain Monitor.** Indicates which chain segment of the receiver buffer is currently being used.
7	4—6	—	**Reserved.** These bits are for internal use and should be masked when reading status register 7.
7	7	—	**Zero.** This bit is always 0.
8	0—4	PIC	**Protocol Input Code.** Contains an encoding of what the protocol considers to be its most recent input stimulus (see Table 7).
8	5	IPF	**Internal Poll/Final Bit.** Last poll/final bit upon which the XPC has acted. This bit is used in conjunction with the protocol input code.
8	6	LSTIFR	**Lost I-Frame.** Cleared for normal operation; set if an I frame is received but no receive buffers are available or if a receiver overrun occurs. This bit is cleared when the XPC exits the station busy condition.
8	7	—	**Zero.** This bit is always 0.
9—11	0—7	RFDF	**Received Frame Project (FRMR) Data Field.** Holds the first, second, and third bytes of data field contained in a received FRMR frame. These registers contain random data until the first FRMR is received.
12, 13	0—7	RFDF	**Received Frame Project (FRMR) Data Field.** Holds the fourth and fifth byte of data field in FRMR frame (modulo-128 only). If in modulo-8 (normal sequencing), these registers always contain random data.

Table 6. Status Register 0 — Protocol State Number Encoding

State Number							
Hex	b4	b3	b2	b1	b0	State	Description
00	0	0	0	0	0	S0	Logically disconnected
01	0	0	0	0	1	S1	Logically disconnected
02	0	0	0	1	0	S2a	Awaiting XID command
03	0	0	0	1	1	S2b	Awaiting XID response
04	0	0	1	0	0	S3	Link set-up initiated
07	0	0	1	1	1	S4	Frame rejected
05	0	0	1	0	1	S5	Disconnect request
06	0	0	1	1	0	S6	Information transfer

Table 6. Status Register 0 — Protocol State Number Encoding (Continued)

State Number						State	Description
Hex	b4	b3	b2	b1	b0		
08	0	1	0	0	0	S7	REJ frame sent
09	0	1	0	0	1	S8	Waiting acknowledgment
11	1	0	0	0	1	S9	Station busy
0A	0	1	0	1	0	S10	Remote station busy
0F	0	1	1	1	1	S11	S9 and S10
10	1	0	0	0	0	S12	S8 and S9
0B	0	1	0	1	1	S13	S8 and S10
1A	1	1	0	1	0	S14	S8, S9, and S10
1B	1	1	0	1	1	S15	S7 and S9
0C	0	1	1	0	0	S16	S7 and S10
0D	0	1	1	0	1	S17	S7, S9, and S10

Table 7. Status Register 8 — Input Code

Input Code*	Description
0	Local stop – disconnect link
1	Local start – initiate link set-up
2	Busy condition clears
3	Valid XID command received
4	T1 expired
5	T3/T4 expired
6	Station has become busy
7	I frame available (reset condition also)
8	Invalid N(S) in last received I frame (X.75)
9	Unrecognized frame received
10	I frame received
11	RNR command received
12	REJ command received
13	RR command received
14	SABM received
15	DISC received
16	UA received
17	FRMR received
18	DM received
19	Valid XID response received
20	Idle link detected for T3
21	Incorrect N(S) in last received I frame
23	N2 exceeded
24	Invalid N(R) in last received I frame
26	Initiate password exchange
27	RNR response received
28	REJ response received
29	RR response received
30	Wait for password exchange

* This code is represented as a binary number in the 5-bit protocol input code field in the status register.

Table 8. Interrupt Vector Register

Bit	7	6	5	4	3	2	1	0
Field	LOST INTERRUPT	0	INT5	INT4	INT3	INT2	INT1	INT0

Code*	Interrupt	Name/Description
1	SABM	**Link Reset Received.** An SABM or SABME command frame was received while the XPC was in the information transfer phase. The link is reinitialized when $\overline{\text{HOSTD}}$ is cleared.
2	UA	**UA Received While Link is Up.** The XPC initializes the link because an unnumbered response frame was received acknowledging an unnumbered command never sent. The link is reinitialized when $\overline{\text{HOSTD}}$ has been cleared. If in the X.75 mode, a FRMR frame is sent.
3	DM	**DM Received.** The XPC attempts to initialize the link if it is in active mode because it received an unsolicited, unnumbered response frame indicating that the far end of the link is in a disconnected state. If in the X.75 mode, a FRMR frame is sent.
4	FRMRR	**Frame Reject (FRMR) Received.** The interrupt is issued after data is stored in status registers 9—13.
5	DISC	**Received DISC While Link is Up.** This interrupt occurs when a disconnect command is received while the XPC is in the information transfer phase, causing the link to go down.
6	IDLINK	**Idle Link Detected.** If the XPC detects 15 or more contiguous 1s, it starts timer T3 if T1 is not running. If a flag is not detected before timer T3 expires, an idle link is reported and this interrupt is issued. If timer T1 is running, the XPC waits for T1 to finish before starting T3.
7	N2EXC	**N2/C2 Counter was Exceeded.** If in the active mode, the XPC attempts to initialize the link because the maximum number of retransmissions (N2) was exceeded. If the XPC is in the password exchange mode, this counter is interpreted as the C2 counter.
8	RF1P	**F = 1 Received Without Sending P = 1.** This interrupt occurs when a response frame with its final bit set was received but the XPC did not send a command frame with poll bit set. In the X.25 mode, the frame is discarded; in the X.75 mode, the XPC sends a FRMR frame to begin link reset procedures.
9	LK01	**Link Is Up.** The XPC goes from the disconnected or link set-up state to the information transfer phase (the logical link has come up).
10	XIDRCVD	**XID Frame Received.** An XID frame was received and its data field was placed in main memory.
11	NOXIDR	**No XID Response.** An XID command was transmitted and no response was received in time T4.

* The code is represented as a binary number in the lower 6 bits of the interrupt vector register. Bit 7 of the interrupt register contains a copy of the lost interrupt bit and is implicitly cleared after the interrupt register is read. Bit 6 is always 0.

Table 8. Interrupt Vector Register (Continued)

Code*	Interrupt	Name/Description
12	FRMRX–W	**Frame Reject Transmitted – W = 1.**** Receipt of command or response that is invalid or not implemented and cannot be corrected by retransmission.
13	FRMRX–X	**Frame Reject Transmitted – X = 1.**** Receipt of S or U frame with an information field that is not permitted.
14	FRMRX–Y	**Frame Reject Transmitted – Y = 1.**** Receipt of an I frame with an information field that exceeds the maximum established length, N1.
15	FRMRX–Z	**Frame Reject Transmitted – Z = 1.**** Receipt of an invalid N(R).
16	PKR	**Packet Received.** This interrupt is issued after the XPC has received an I frame and stored its data field in main memory. V(R) points to the next element in the RLOOK table after this interrupt is issued.
17	XBA	**Transmitted Block Acknowledged.** Issued when the XPC receives acknowledgment for one or more previously transmitted I frames.
18	RCVOVR	**Receiver Overrun.** The receiver FIFO buffer overflowed because new characters were being brought in faster than DMA could save them in main memory. The receiver FIFO is 4-bytes deep. The XPC clears the RECR bit in the command register when issuing this interrupt.
19	XUNDR	**Transmitter Underrun.** The transmitter FIFO buffer became empty during transmission and frame was aborted. If the send bit is set, the XPC attempts to retransmit the I frame. The transmit FIFO is 4-bytes deep.
20	PPROB	**Parity Error.** If the DMA reads a main memory location and an error is detected, it reads that location again. This interrupt is issued if the error is repeated. If an I frame is in transmission, it is aborted.
21	RLKNRDY	**Receiver Look-Up (RLOOK) Table Not Ready.** The XPC read the RLOOK element referenced by V(R) and found that the RECRDY bit is cleared. It clears the RECR bit in the command register when issuing this interrupt.
22	LDCHM	**Going to Next Chain Segment.** The DMA has filled a buffer segment and automatically transfers (chains) to the next segment.
23	BFOVF	**Buffer Overflow (Next Chain Segment Not Ready).** The DMA has read the transfer address before transferring to the next buffer and it was 0. This interrupt occurs only for the receive buffers. XPC clears the RECR bit in the command register when issuing this interrupt.
24	BADIFLD	**Received I Field is Not an Integral Number of Bytes.** The length of the data field of a received I frame is not an integral number of bytes and the XPC is in byte mode. Bit 5 of byte 0 of the RLOOK element is set.
25	CTSLST	**Clear-to-Send-Lost.** Clear-to-send ($\overline{CTS}$) input on the XPC went high. The XPC goes into inactive state until $\overline{CTS}$ goes low.
26	ODAD	**Odd Address.** The TLOOK starting address is odd and the data bus is set for 16-bit operation. The XPC sets MDISC and goes into the set-up state.

* The code is represented as a binary number in the lower 6 bits of the interrupt vector register. Bit 7 of the interrupt register contains a copy of the lost interrupt bit and is implicitly cleared after the interrupt register is read.

** W, X, Y, and Z are bits in the information field of a frame reject response that indicates the reason that a frame is being frame rejected. The XPC automatically generates this response.

Table 8. Interrupt Vector Register (Continued)

Code*	Interrupt	Name/Description
27	NOAD	**No Address.** The TLOOK starting address is 0. The XPC sets MDISC and goes into the set-up state.
28	RCOVF	**Receiver Counter Overflowed.** A data field longer than the maximum 4096 bytes permitted by DMA was received.
29	LK10	**Link is Down.** The XPC goes to a link set-up or disconnected state. $\overline{\text{HOSTD}}$ must be cleared to resume normal operation.
30	CTSACQ	**Clear-to-Send Acquired.** $\overline{\text{CTS}}$ input went low.
31	RCLST	**Receive Carrier Lost.** $\overline{\text{CD}}$ input went high. The XPC takes no further action.
32	CO**	**Countout in Counters 0 and 1.** Register addresses 64 and 66.
33	CO	**Countout in Counter 17.** Register address 98.
34	CO	**Countout in Counters 2 and 3.** Register addresses 68 and 70.
35	CO	**Countout in Counter 16.** Register address 96.
36	CO	**Countout in Counter 4.** Register address 72.
37	CO	**Countout in Counter 5.** Register address 74.
38	CO	**Countout in Counter 6.** Register address 76.
39	CO	**Countout in Counter 7.** Register address 78.
40	CO	**Countout in Counter 8.** Register address 80.
41	CO	**Countout in Counter 9.** Register address 82.
42	CO	**Countout in Counter 10.** Register address 84.
43	CO	**Countout in Counter 11.** Register address 86.
44	CO	**Countout in Counter 12.** Register address 88.
45	CO	**Countout in Counter 13.** Register address 90.
46	CO	**Countout in Counter 14.** Register address 92.
47	CO	**Countout in Counter 15.** Register address 94.
48	RCACQ	**Receive Carrier Acquired.** $\overline{\text{CD}}$ input went low. The XPC takes no further action.

* The code represented as a binary number in the lower 6 bits of the interrupt vector register. Bit 7 of the interrupt register contains a copy of the lost interrupt bit and is implicitly cleared after the interrupt register is read.

** Interrupt on count-out bit in parameter register 1 must be set for the CO interrupts to occur.

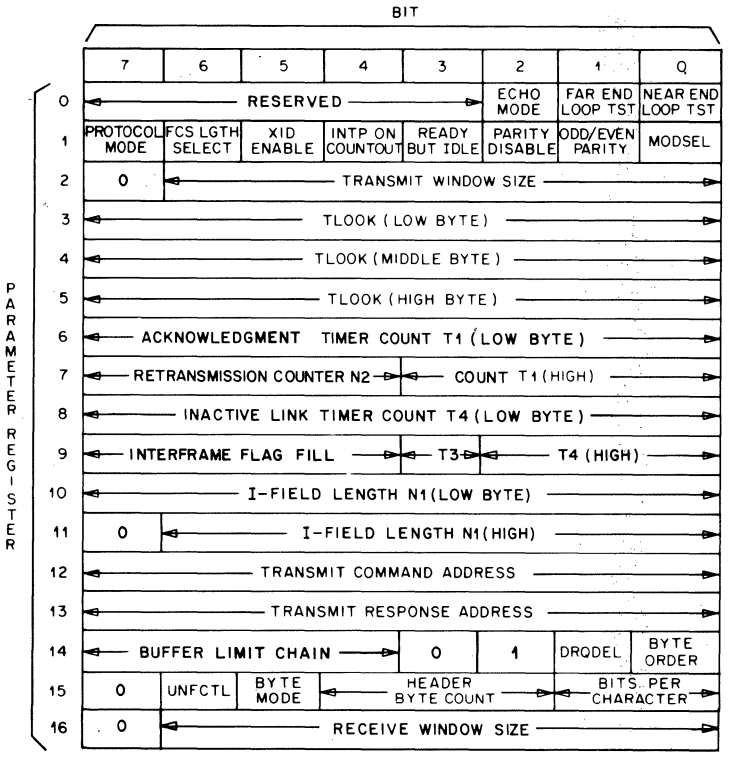


Figure 4. Parameter Registers

Table 9. Parameter Registers

Reg	Bit	Symbol	Name/Description
0	0	NELT*	**Near-End Loop Test.** Setting this bit causes the XPC to enter the near-end loopback test mode. TD and RD are internally tied together; the XPC transmits 1s on TD. Both RC and TC must be applied and must be synchronized with each other. $\overline{\text{CTS}}$ must be low.
0	1	FELT*	**Far-End Loop Test.** Setting this bit causes the XPC, in conjunction with link controller at far-end of loop, to enter the far-end loopback test. The remote station must be in echo mode. Both RC and TC must be applied. $\overline{\text{CTS}}$ must be low.
0	2	ECHMOD*	**Echo Mode.** Setting this bit causes data coming into receive data (RD) input to appear at transmitter data (TD) output. The XPC takes no action on received frames. Neither RC nor TC need be applied.
0	3—7	—	**Reserved.** These bits are for internal use and are not writable. They should be masked when reading parameter 0.
1	0	MODSEL	**Modulus Select.** If cleared, selects modulo-8, normal sequence numbering; if set, selects modulo-128, extended sequence numbering.

* These bits cause the specified action only if set after a chip reset and before MDISC is cleared. Only one of these bits can be set for the specified action to occur.

Table 9. Parameter Registers (Continued)

Reg	Bit	Symbol	Name/Description
1	1	PARSTAT	**Status of XPC Parity.** If cleared, even parity; if set, odd parity.
1	2	PARDSB	**Parity Disable.** Setting this bit disables the parity generation and checking capability. The parity pins should not be connected if parity is disabled.
1	3	RDYIDL	**Ready But Idle.** If cleared, the XPC transmits a continuous stream of flags when logically disconnected and not sending frames; if set, the XPC transmits a continuous stream of 1s as interframe fill when logically disconnected.
1	4	INTCO	**Interrupt On Count-Out.** If this bit is set, the XPC issues an interrupt if any of the counter registers are decremented to 0.
1	5	PWDENBL	**Password Enable.** Setting this bit causes the XPC to require a password exchange with far end of link before the link set-up is allowed.
1	6	FCSLEN	**FCS Length Select.** If cleared, XPC uses standard 16-bit CRC generator polynomial; if set, XPC uses 32-bit CRC generator polynomial.
1	7	PROTMOD	**Protocol Mode.** If this bit is set, the XPC is in the X.75 mode; if this bit is cleared, the device is in the X.25 mode.
2	0—6	k	**Transmit Window Size.** Maximum allowable number of outstanding I frames (must not equal 0). An outstanding I frame is considered to be any I frame acknowledged by the remote DXE. Valid values are 1—7 for modulo-8 and 1—127 for modulo-128.
2	7	—	**Zero.** This bit is always 0.
3—5	0—7	TLOOK	**Transmitter Look-Up Table Pointer.** Starting address in main memory of the first element of the transmitter look-up table.
6	0—7	T1 (low byte)	**T1 Timer Period.** This number is proportional to period of the T1 timer: $\text{T1 Count}_{\text{(Decimals)}} = \frac{\text{fCLK(Hz)}}{16384} \times \text{T1 PERIOD}_{\text{(Seconds)}}$. It is the maximum time the XPC waits for an acknowledgment.
7	0—3	T1 (high bits)	
7	4—7	N2	**X.25 Retransmission Counter.** Valid values are 1—15, which determine the maximum number of transmissions and retransmissions of a frame allowed without receiving an acceptable response.
8	0—7	T4 (low byte)	**T4 Timer Period.** A number proportional to period of the T4 timer: $\text{T4 Count}_{\text{(Decimals)}} = \frac{\text{fCLK(Hz)}}{16384} \times \text{T4 PERIOD}_{\text{(Seconds)}}$. Maximum time a station allows without frames being exchanged on data link. This parameter is also used a part of the pseudo-T3 timer.
9	0—2	T4 (high bits)	

Table 9. Parameter Registers (Continued)

Reg	Bit	Symbol	Name/Description
9	3	T3	**Maximum Idle Time.** Maximum time a station receives an idle condition before resetting the link: If T3 = 0, the period of T3 = the period of T4. If T3 = 1, the period of T3 = T4 period + $\frac{2^{25}}{fCLK(Hz)}$.
9	4—7	FLGFIL	**Interframe Flag Fill.** A weighted code specifying the minimum number of flags to be inserted between frames (see Table 1).
1	0—7	N1 (low byte)	**Maximum I Field Length.** The XPC rejects any I frame whose I Field length exceeds N1 bits.
11	0—6	N1 (high bits)	
11	7	—	**Zero.** This bit is always 0.
12	0—7	TCA	**Transmit Command Address.** Address field of command frames transmitted by the XPC. Address of local station.
13	0—7	TRA	**Transmit Response Address.** Address field of response frames transmitted by the XPC. Address of far-end station.
14	0	BYTORD	**Byte Order.** If cleared, the Intel data bus convention is used for DMA: D7—D0 is even byte; D15—D8 is odd byte. If set, the Motorola data bus convention is used for DMA: D7—D0 is odd byte; D15—D8 is even byte. $\overline{BHE}$ becomes $\overline{BLE}$ when this bit is set (see Figure 9 and Table 18).
14	1	DRQDEC	**DMA Request Delay.** If this bit is set, the DMA logic waits for $\overline{DACK}$ to go high before reasserting $\overline{DREQ}$; if this bit is clear, the DMA logic does not wait for $\overline{DACK}$ to go high before reasserting $\overline{DREQ}$.
14	2	—	**One.** This bit is always 1.
14	3	—	**Zero.** This bit is always 0.
14	4—7	LIMIT	**Limit.** Size of buffer segments for both receiver and transmitter. Buffer segments must be sized in 64-byte multiples: Limit = $\frac{\text{BUFFER SEGMENT}}{64} - 1$. Maximum buffer segment = 64(1+15) = 1024 bytes.
15	0,1	BPC	**Bits Per Character.** Characters are 5—8 bits in length and are right-justified, with 0s in the most significant bits (see Table 11).
15	2—4	HBC	**Header Byte Count.** Data field of an I frame may consist of a number of characters proceeded by some 8-bit header bytes. This field specifies number of 8-bit bytes in header (see Table 12).
15	5	BYTMOD	**Byte Mode.** If 0, a received fractional byte length data field is permitted; if 1, received I frames must be an integral number of 8-bit bytes.

Table 9. Parameter Registers (Continued)

Reg	Bit	Symbol	Name/Description
15	6	UNFCTL	**Unnumbered Control Field Length.** Used in modulo-128 operation only. If cleared, the unnumbered control field is two bytes; if set, the unnumbered control field is one byte.
15	7	—	**Zero.** This bit is always 0.
16	0—6	rk	**Receive Window Size.** Used in X.75 mode only. The maximum allowable number of packets that can be received before an acknowledgment must be sent. Valid values are 1—7 for modulo-8 and 1—127 for modulo-128.
16	7	—	**Zero.** This bit is always 0.

Main Memory

Main memory contains data buffers that store transmit and receive data. The pointers used to access these buffers are stored in look-up tables in main memory. The location of data to be transmitted is referenced by pointers in the transmitter look-up table (TLOOK) elements, and the location of data to be received is referenced by pointers in the receiver look-up table (RLOOK) elements.

Table 10. Interframe Flag Fill

Flag Fill Parameter	Minimum Number of Flags
0	1
1	2
2	4
3	6
4	16
5	18
6	2
7	22
8	64
9	66
10	68
11	70
12	80
13	82
14	84
15	86

Table 11. Bits Per Character Encoding

Parameter Register 15		Number of Bits per Character
b1	b0	
0	0	8
0	1	7
1	0	6
1	1	5

Table 12. Header Byte Count

Parameter Register 15			Number of Header Bytes
b4	b3	b2	
0	0	0	7
0	0	1	6
0	1	0	5
0	1	1	4
1	0	0	3
1	0	1	2
1	1	0	1
1	1	1	0

Table 13. Counter Registers

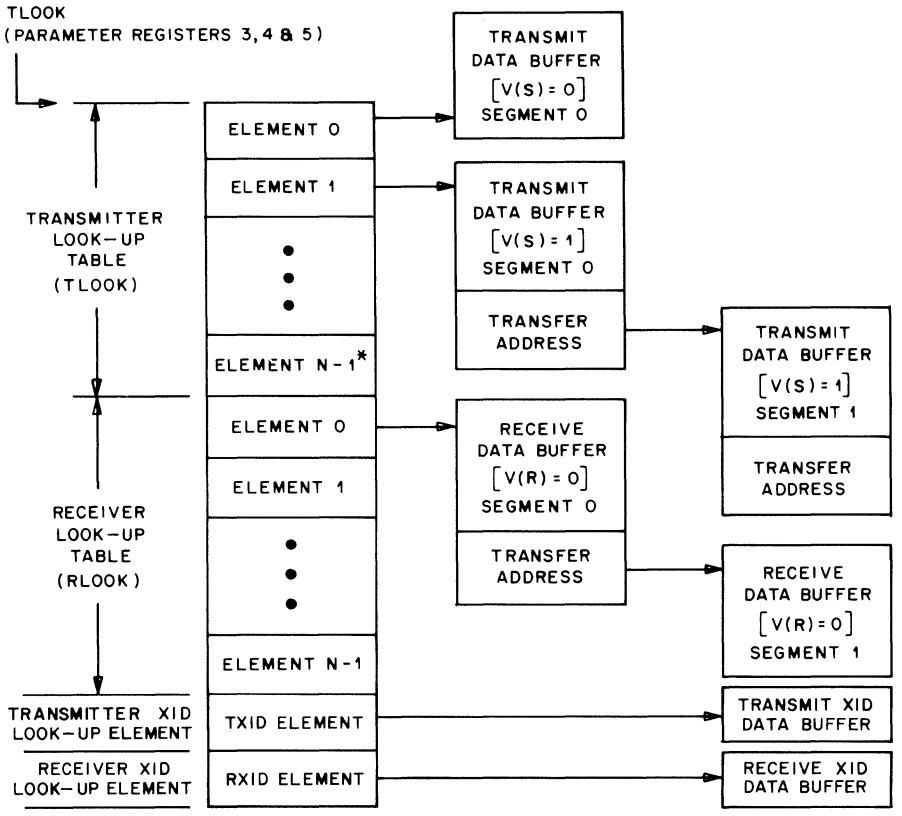
Counter	Register Number	Description of Event Counted
	64	Supervisory and unnumbered frames received (low byte)
1	66	Supervisory and unnumbered frames received (high byte)
2	68	Supervisory and unnumbered frames sent (low byte)
3	70	Supervisory and unnumbered frames sent (high byte)
4	72	REJ frames received
5	74	REJ frames sent
6	76	RNR frames received
7	78	RNR frames sent
8	80	I frames retransmitted
9	82	Number of times T1 expired
1	84	Null packets received
11	86	Short frames received
12	88	I fields greater than N1 received
13	90	Bad frame check sequences received
14	92	Invalid addresses received
15	94	Invalid control fields received
16	96	Number of aborts received
17	98	Number of parity errors

The TLOOK table is a list of N 8-byte elements in main memory starting at address TLOOK (stored in parameter registers 3, 4, and 5). N is either 8 or 128 and is determined by the modulus select bit in parameter register 1. Each element in the TLOOK table describes the buffers corresponding to one packet of data to be transmitted by the XPC. The TLOOK list of elements is a circular queue, with element number V(S) at the head.

The RLOOK table is a list of N 8-byte elements in main memory immediately following the TLOOK table. Each element in the RLOOK table describes the buffers corresponding to one packet of data to be received by the XPC. The RLOOK list of elements is a circular queue also, with the element number V(R) at the head.

The XID table is a list of two 8-byte elements in main memory immediately following the RLOOK table. Element 0 is the transmit look-up element (TXID) and element 1 is the receive look-up (RXID) element. These elements are identical to the TLOOK and RLOOK elements, respectively.

When buffer chaining is used and a transfer address of 0 is encountered, the buffer is considered to have ended. Transfer addresses immediately follow the buffers in main memory and are three bytes long (low, middle, and high bytes). Buffer segments must be sized in multiples of 64 bytes. The maximum buffer segment is 1024 bytes. The XPC determines the size of the buffer segment from the limit field in parameter register 14.



Note: Each element consists of 8 bytes. Each transfer address consists of 3 bytes.
* N is either 8 or 128, depending on the sequence numbering modulo select.

Figure 5. Main Memory Configuration

DMA Operation

The XPC uses a dual-channel DMA to read and write the data fields of the I and XID frames and the TLOOK and RLOOK tables. The full 16-bit data bus is used for this operation when the DBC pin is connected to V_{DD}. An 8-bit data bus (lower byte of data bus) is used when DBC is connected to V_{SS}.

When the XPC is configured for an 8-bit data bus, DMA can begin on even-or odd-byte boundaries for the RLOOK and TLOOK tables and buffers. The XPC reads and writes one byte at a time; the upper data byte (D15—D8) is not used.

When the XPC is configured for a 16-bit data bus, DMA must begin on even-word address boundaries for the RLOOK and TLOOK tables and buffers. $\overline{BHE}/\overline{BLE}$ from the DMA controller is used to access the odd byte of a 16-bit word. $\overline{BHE}/\overline{BLE}$ allows individual selection of even bytes (A0 = 0, $\overline{BHE}/\overline{BLE}$ = 1) or both odd and even bytes as words (A0 = 0, $\overline{BHE}/\overline{BLE}$ = 0).

When BYTORD is high, the data bus is configured in the Motorola mode. $\overline{BHE}$ is then considered to be $\overline{BLE}$. The odd byte appears on D7—D0 (see Figure 9 and Table 18).

To initiate a DMA bus cycle, the XPC requests the use of the bus by forcing $\overline{DREQ}$ low. The host CPU indicates that the bus is available by forcing $\overline{DACK}$ low. This allows $\overline{RE}$, $\overline{WE}$, R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$, A0—A23, and $\overline{AS}$ to become outputs and $\overline{READY}$ to become an input. Once the DMA has control of the bus, it expects to have use of the bus until it has finished its DMA operation. For some operations, the DMA can request the use of the bus within two CLK periods after it has relinquished bus control. For those applications where $\overline{DACK}$ is quick enough to respond within two CLK periods, DRQDEL in parameter register 14 can be cleared. If $\overline{DACK}$ is slow to respond, DRQDEL must be set high.

Slow memory handshaking is provided through the $\overline{READY}$ input. The DMA holds a read or write until it samples $\overline{READY}$ low.

When instructed to open a transmit element, the DMA calculates the address of the particular TLOOK element from the TLOOK base address and the value of V(S), and proceeds to read the bytes of the element. If the BRDY bit in the first byte is 0, the DMA aborts the TLOOK read. The XPC clears the SEND bit in the command register and information transmission is suspended. If BRDY is high, the DMA continues to read the TLOOK element, placing the transmit count in a byte counter and the transmit buffer pointer in an address counter register. The DMA then fetches the data to be transmitted from memory and routes it to the transmitter FIFO. The transmitter signals the DMA for more data when the transmit FIFO contains two bytes or less. The loading process ends when the number of bytes specified by the transmit count has been loaded into the transmit FIFO. The DMA then places this TLOOK element in the not-acknowledged state by setting the NACK bit and clearing the BRDY bit in the element. The TLOOK element is available for retransmission when in this configuration.

When an acknowledgment is received, the DMA clears the NACK bit and sets the ACK bit of all the TLOOK elements whose information buffers have been acknowledged. The DMA then issues an XBA interrupt to indicate that the data associated with one or more TLOOK elements has been acknowledged. The host can then reallocate the TLOOK elements to send more information frames.

When instructed to open a receive element, the DMA calculates the address of the particular RLOOK element from the TLOOK base address and the value of V(R) and proceeds to read the bytes of the element. If the RECRDY bit in the first byte is 0, the DMA aborts the RLOOK read. The XPC clears the RECR bit in the command register and any information frames that are received are discarded. If RECRDY is high, the DMA continues to read the RLOOK element, placing the receive buffer pointer in an address counter register.

When the receive FIFO contains two or more bytes of data, the DMA routes the data from the FIFO and writes it out to memory. The DMA continues to write data to memory until it is notified by the receiver of an end-of-frame condition. At this time, the DMA flushes out the receive FIFO and updates the RLOOK element with the number of bytes received and places the element in the frame-complete state. The DMA then issues a PKR interrupt, notifying the host that an information frame was received and that the data was placed in memory. The host can then reinitialize the RLOOK element in anticipation of receiving more information frames.

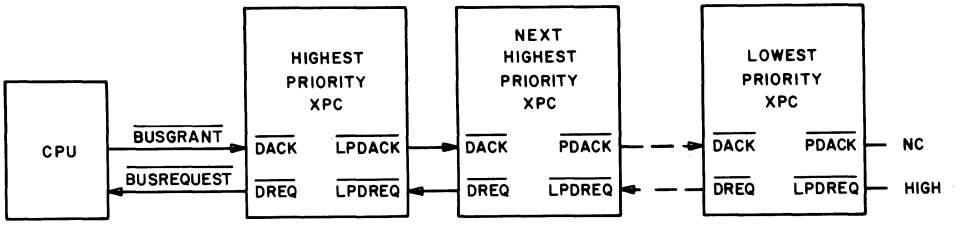


Figure 6. DMA Priority Scheme Interconnection

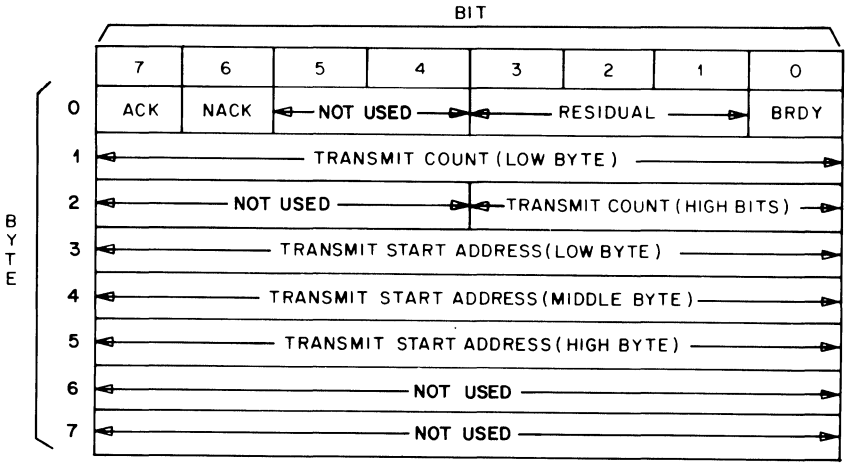


Figure 7. TLOOK Element Layout

The DMA accesses the transmit and receive buffers two bytes at a time when configured for 8-bit data buses and one word at a time when configured for 16-bit data buses. If the number of bytes in the buffer is odd, the last access is a single byte access.

A priority DMA bus arbitration scheme can be implemented with no additional hardware by using a daisy chain for multiple XPC applications. The $\overline{\text{DREQ}}$ pin of the lowest priority XPC is tied to the $\overline{\text{LPDREQ}}$ input of the next highest priority XPC. $\overline{\text{DREQ}}$ for the highest priority XPC is tied to the HOLD input of the CPU. The hold acknowledge output of the CPU is tied to the $\overline{\text{DACK}}$ of the highest priority XPC. The $\overline{\text{PDACK}}$ of the highest priority XPC is tied to $\overline{\text{DACK}}$ of the next highest priority XPC and this continues until the lowest priority XPC is reached. The $\overline{\text{LPDREQ}}$ input of the lowest priority XPC must be tied high.

CAUTION: When resetting an XPC in a chain, $\overline{\text{CS}}$ must be held high for that XPC. If $\overline{\text{CS}}$ is low when the XPC is reset, the outputs are 3-stated and the propagated request and acknowledge signals are disrupted.

Table 14. TLOOK Elements

Byte	Bit	Symbol	Name/Description
0	0	BRDY	**Buffer Ready.** Setting this bit tells the XPC that data associated with this element is ready to be transmitted. BRDY is the last bit to be set by CPU. After all the data of a frame has been accessed, the XPC clears the BRDY bit and sets the NACK bit of the associated element. If the NACK bit is set, BRDY also indicates that the buffer is available to the XPC for retransmission.
0	1—3	TRRES	**Residual.** The XPC allows the CPU to select the number of bits that should be transmitted from the last byte of data (see Table 17.) When in byte mode, there should be no residual bits.
0	4, 5	—	**Spare.** Not used.
0	6	NACK	**Not Acknowledged.** The XPC sets this bit after all the data has been accessed; the XPC clears this bit when the packet associated with this element is acknowledged.

Table 14. TLOOK Elements (Continued)

Byte	Bit	Symbol	Name/Description
0	7	ACK	**Acknowledged.** The XPC sets this bit when a packet associated with this element becomes acknowledged and generates an XBA interrupt to the CPU. Only then may the CPU reuse this buffer.
1 2	0—7 0—3	TRCNT	**Transmit Count.** The number of bytes in a data packet associated with this element is acknowledged and generates an XBA interrupt to the CPU.
2	4—7	—	**Spare.** Not used.
3—5	0—7	TRSA	**Transmit Start Address.** This 24-bit number is the location in main memory of the first byte of data in the packet associated with this element.
6, 7	0—7	—	**Spare.** Not used.

Table 15. TLOOK Residual Field

TLOOK Element Byte 0			Bits Transmitted From Last Memory Byte
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1	0	0	4
1	0	1	3
1	1	0	2
1	1	1	1

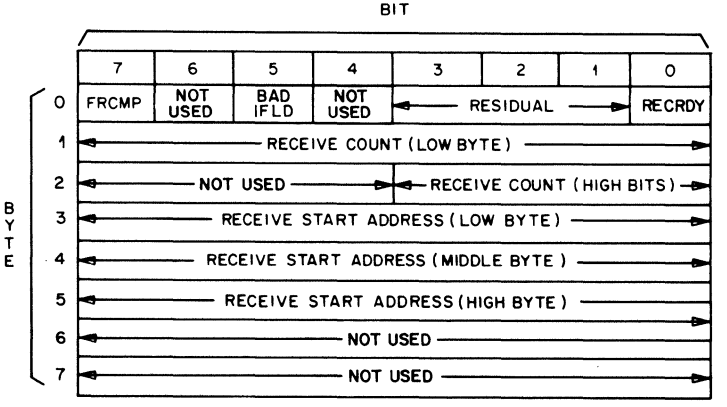


Figure 8. RLOOK Element Layout

Table 16. RLOOK Elements

Byte	Bit	Symbol	Name/Description
0	0	RECRDY	**Receiver Ready.** Setting this bit tells the XPC that the data buffer associated with this element is ready to receive data. All fields of the RLOOK element should be initialized before the CPU sets the RECRDY bit. After the XPC receives a valid packet and stores it in memory, it clears the RECRDY bit of the associated element.
0	1—3	RCVRES	**Residual Bits.** After the XPC receives a frame, it writes the number of bits stored in the last byte into the residual bits field (see Table 19).
0	4	—	**Spare.** Not used.
0	5	BADIFLD	**Bad Information Field.** A fractional byte length frame was received and stored in the buffer pointed to by this element. The XPC also generates a BADIFLD interrupt. This bit is set only if the XPC is in byte mode.
0	6	—	**Spare.** Not used.
0	7	FRCMP	**Frame Complete.** When a valid I frame is received, the XPC writes the receive count, clears RECRDY, and sets FRCMP. A PKR interrupt is generated to notify the CPU of the received packet.
1	0—7	RCVCNT	**Receiver Count.** This 12-bit number specifies how many bytes of memory have been filled by the packet. The XPC writes this after the I frame has been received.
2	4—7	—	**Spare.** Not used.
3—5	0—7	RCVSA	**Receive Start Address.** This 24-bit address is the location in main memory of the first byte of received data for the packet.
6, 7	0—7	—	**Spare.** Not used.

Table 17. RLOOK Residual Field

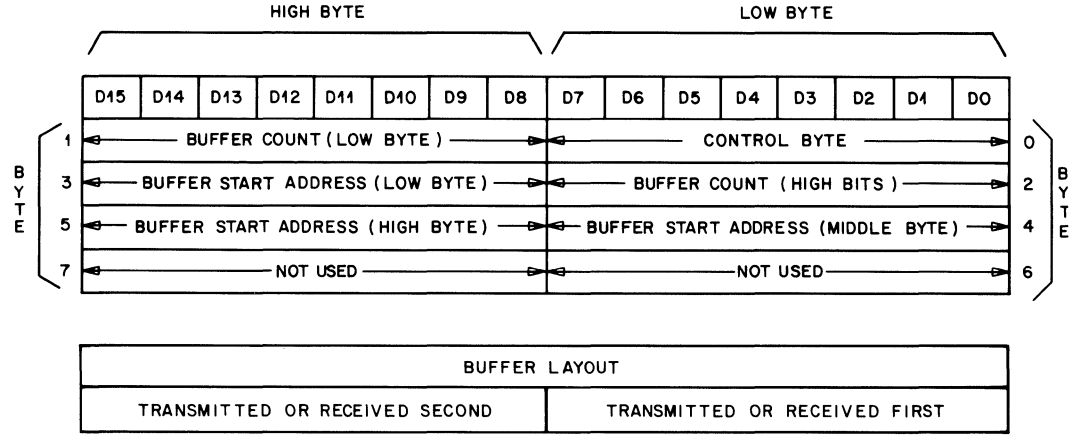
RLOOK Byte 0			Received Bits in Last Memory Character Bits per Character*			
b3	b2	b1	8	7	6	5
0	0	0	8	7	6	5
0	0	1	1	1	1	1
0	1	0	2	2	2	2
0	1	1	3	3	3	3
1	0	0	4	4	4	4
1	0	1	5	5	5	x
1	1	0	6	6	x	x
1	1	1	7	x	x	x

* x = don't care.

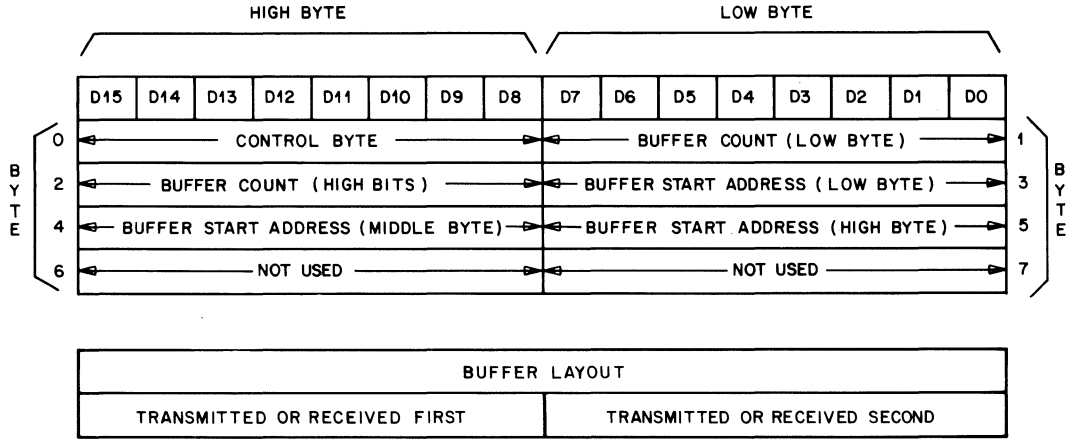
Table 18. Intel and Motorola Modes*

Bits		Mode	Read		Write	
BYTORD	$\overline{BHE}/\overline{BLE}$		D15—D8	D7—D0	D15—D8	D7—D0
0	0	Intel	Input	Input	Output	Output
0	1	Intel	3-state	Input	3-state	Output
1	0	Motorola	Input	Input	Output	Output
1	1	Motorola	Input	3-state	Output	3-state

* DBC = 1; AO = 0.



a. Receive or Transmit Element in Intel Mode (BYTORD = 0)



b. Receive or Transmit Element in Motorola Mode (BYTORD = 1)

Note: The above figures explain how the elements are laid out in memory for each value of BYTORD in 16-bit mode (DBC = 1).

Figure 9. Receive or Transmit Element Layout

Characteristics

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 0.25%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input voltage:					
low	V_{IL}	−0.5	0.8	V	—
high	V_{IH}	2.0	V_{DD}	V	—
Output voltage:					
low	V_{OL}	—	0.45	V	I_{OL} = 1.7 mA
high	V_{OH}	2.4	—	V	I_{OH} = −400 μA
Power supply current	I_{DD}	—	400	mA	—
Input current					
high	I_{IH}	—	10	μA	V_{IH} = 5.25 V
Output float current:					
low	I_{OZL}	—	−10	μA	V_{OL} = 0.4 V
high	I_{OZH}	—	10	μA	V_{OH} = 5.25 V
Power dissipation	PD	—	2.0	W	V_{DD} = 5.0

Maximum Ratings

Ambient operating temperature (T_A) range ..... 0 to 70 °C
Storage temperature (Tstg) range ..... −65 to +125 °C
Voltage range on any pin with respect to ground ..... −0.5 to +7 V
Power dissipation (PD) ..... 2.8 W

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Max	Unit
Clock Timing (Figure 10)				
tCKHCKL	CLK high time	240	3760	ns
tCKLCKH	CLK low time	240	3760	ns
tCKHCKH	CLK period (sum of tCKHCKL and tCKLCKH)	500	4000	ns
Receive Clock Timing (Figure 11)				
tRCHRCL	RC high time	3tCKHCKH	—	—
tRCLRCH	RC low time	3tCKHCKH	—	—
tRCHRDX	RD hold time	1.5CKHCKH	—	—
tRDVRCH	RD set-up time	1.5CKHCKH	—	—

Symbol	Description	Min	Max	Unit
	Transmit Clock Timing (Figure 12)			
tTCHTCL	TC high time	3tCKHCKH	—	—
tTCLTCH	TC low time	3tCKHCKH	—	—
tTCLTDX	TD transition delay	tCKHCKH	2.5tCKHCKH	—
	Reading XPC Registers (Figure 13)			
tAVREL	Address set-up time	0	—	ns
tREHAX	Address hold time	0	—	ns
tCSLREL	$\overline{CS}$ set-up time	0	—	ns
tREHCSX	$\overline{CS}$ hold time	0	—	ns
tCKHRYL	$\overline{READY}$ wait propagation time	tCKHCKLMIN + tCKLRYL + 10 ns	13.5tCKHCKH + tCKLRYL	—
tCKLRYL	$\overline{READY}$ transition delay	0	265	ns
tREHRYH	$\overline{READY}$ hold time after $\overline{RE}$ goes high	210	—	ns
tREHREL	Interoperation delay time	tCKHCKH	—	—
tRELCKH	$\overline{RE}$ set-up time for ready wait propagation	120	—	ns
tDVCKL	Data valid set-up time for event counter registers	25	—	ns
tCSLDV	Time to data valid for nonevent counter registers	50	250	ns
tCSHDZ	Data hold time	0	—	ns
tAVDX	Data hold time	0	—	ns
tCSHRYX	$\overline{READY}$ hold time after $\overline{CS}$ goes high	0	50	ns
	Writing XPC Registers (Figure 14)			
tAVWEL	Address set-up time	0	—	ns
tRYLAX	Address hold time	0	—	ns
tCSLWEL	$\overline{CS}$ set-up time	0	—	ns
tRYLCSX	$\overline{CS}$ hold time	0	—	ns
tWELDV	Data set-up time	—	tCKHCKLMIN	—
tRYLDX	Data hold time	0	—	ns
tWELCKH	$\overline{WE}$ set-up time for ready wait propagation	140	—	ns
tRYLWEH	$\overline{WE}$ hold time	0	—	ns
tCKHRYL	$\overline{READY}$ wait propagation time	3tCKHCKH + tCKLRYL	13.5tCKHCKH + tCKLRYL	—
tCKLRYL	$\overline{READY}$ transition delay	0	265	ns
tWEHRYH	$\overline{READY}$ hold time after $\overline{WE}$ goes high	245	—	ns

Symbol	Description	Min	Max	Unit
	Writing XPC Registers (Figure 14)			
tWEHWEL	Interoperation delay time	tCKHCKH	—	—
tCSHRYX	$\overline{\text{READY}}$ hold time after $\overline{\text{CS}}$ goes high	0	50	ns
	DMA Read Cycle (Figure 15)			
tCKLDRL	$\overline{\text{DREQ}}$ transition delay	—	265	ns
tCKHDRH	$\overline{\text{DREQ}}$ transition delay	—	175	ns
tDALCKL	$\overline{\text{DACK}}$ set-up time	160	—	ns
tDRHDAH	$\overline{\text{DACK}}$ response time to removal of $\overline{\text{DREQ}}$: DRQDEL = 0 DRQDEL = 1	 0 0	 tCKHCKH —	 — ns
tDALRWV	R/$\overline{\text{W}}$, $\overline{\text{BHE}}$/$\overline{\text{BLE}}$ delay time from $\overline{\text{DACK}}$ low	—	200	ns
tCKLAV	Address valid delay time from CLK low	—	325	ns
tCKHASL	$\overline{\text{AS}}$ transition delay	—	160	ns
tCKHASH	$\overline{\text{AS}}$ transition delay	—	185	ns
tCKLREL	$\overline{\text{RE}}$ transition delay	—	125	ns
tCKHREH	$\overline{\text{RE}}$ transition delay	—	190	ns
tRYLCKH	$\overline{\text{READY}}$ set-up time	70	—	ns
tWELDV	Data set-up time	—	$t_{CKHCKL_{MIN}}$	—
tRYLDX	Data hold time	0	—	ns
tWELCKH	$\overline{\text{WE}}$ set-up time for ready wait propagation	140	—	ns
tRYLWEH	$\overline{\text{WE}}$ hold time	0	—	ns
tCKHRYL	$\overline{\text{READY}}$ wait propagation time	3tCKHCKH + tCKLRYL	13.5tCKHCKH + tCKLRYL	—
tCKLRYL	$\overline{\text{READY}}$ transition delay	0	265	ns
tWEHRYH	$\overline{\text{READY}}$ hold time after $\overline{\text{WE}}$ goes high	245	—	ns
tWEHWEL	Interoperation delay time	tCKHCKH	—	—
tCSHRYX	$\overline{\text{READY}}$ hold time after $\overline{\text{CS}}$ goes high	0	50	ns
tCKLDRL	$\overline{\text{DREQ}}$ transition delay	—	265	ns
tCKHDRH	$\overline{\text{DREQ}}$ transition delay	—	175	ns
tDALCKL	$\overline{\text{DACK}}$ set-up time	160	—	ns
tDRHDAH	$\overline{\text{DACK}}$ response time to removal of $\overline{\text{DREQ}}$ DRQDEL = 0 DRQDEL = 1	 0 0	 tCKHCKH —	 — ns

Symbol	Description	Min	Max	Unit
	DMA Read Cycle (Figure 15)			
tDALRWV	R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ delay time from $\overline{DACK}$ low	—	200	ns
tCKLAV	Address valid delay time from CLK low	—	325	ns
tCKHASL	$\overline{AS}$ transition delay	—	160	ns
tCKHASH	$\overline{AS}$ transition delay	—	185	ns
tCKLREL	$\overline{RE}$ transition delay	—	125	ns
tCKHREH	$\overline{RE}$ transition delay	—	190	ns
tCKLRYH	$\overline{READY}$ hold time	50	—	ns
tDVCKL	Data set-up time without parity with parity	 50 120	 — —	 ns ns
tCKHDX	Data hold time	130	—	ns
tRELREH	Minimum read strobe	1.5tCKHCKH	—	—
tCKHRWZ	R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ hold time	0	220	ns
tCKHAZ	Address hold time	0	290	ns
tCKHASZ	$\overline{AS}$ hold time	0	220	ns
tCKHREZ	$\overline{RE}$ hold time	0	220	ns
	DMA Multiple Byte Read Operation (Figure 16)			
tASHASL	Address transition and set-up time	—	tCKHCKH	—
tREHREL	Delay time between read operations			
tCKLDRH*	DMA bus access time: DBC = 0 DBC = 1	 4.5tCKHCKH** 4.5tCKHCKH**	 19.5tCKHCKH† 10.5tCKHCKH††	 — —
	DMA Write Cycle (Figure 17)			
tCKLDRL	$\overline{DREQ}$ transition delay	—	265	ns
tCKHDRH	$\overline{DREQ}$ transition delay	—	175	ns
tDALCKL	$\overline{DACK}$ set-up time	140	—	ns
tDRHDAH	$\overline{DACK}$ response time to removal of $\overline{DREQ}$: DRQDEL = 0 DRQDEL = 1	 0 0	 tCKHCKH —	 — ns
tDALRWV	R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ delay time from $\overline{DACK}$ low	—	200	ns
tCKLAV	Address valid delay time from CLK low	—	325	ns
tCKASL	$\overline{AS}$ transition delay	—	160	ns

Symbol	Description	Min	Max	Unit
DMA Write Cycles (Figure 17)				
tCKHASH	$\overline{AS}$ transition delay	—	185	ns
tCKLWEL	$\overline{WE}$ transition delay	—	135	ns
tCKLWEH	$\overline{WE}$ transition delay	—	180	ns
tRYLCKL	$\overline{READY}$ set-up time	35	—	ns
tCKLRYH	$\overline{READY}$ hold time	60	—	ns
tCKLDV	Data valid delay time	—	260	ns
tCKLDX	Data hold time	tCKHCKH	—	—
tWELWEH	Minimum write strobe	tCKHCKH	—	—
tCKHRWZ	R/$\overline{W}$, $\overline{BHE}$/$\overline{BLE}$ hold time	0	220	ns
tCKHAZ	Address hold time	0	290	ns
tCKHASZ	$\overline{AS}$ hold time	0	220	ns
tCKHWEZ	$\overline{WE}$ hold time	0	220	ns
tCKHDZ	Data time to 3-state	—	0	ns
DMA Multiple Write Operation (Figure 18)				
tCKLBEH	$\overline{BHE}$/$\overline{BLE}$ transition delay	—	210	ns
tASHASL	Address transition and set-up time	tCKHCKH	2tCKHCKH	—
tWEHWEL	Delay time between write operations	2tCKHCKH	3tCKHCKH	—
tCKLDRH*	DMA bus access time: DBC = 0 DBC = 1	 4.5tCKHCKH** 4.5tCKHCKH**	 11.5tCKHCKH† 8.5tCKHCKH††	 — —
DMA Daisy Chain Timing (Figure 19)				
tLDLCKL	$\overline{LPDREQ}$ set-up time to be sampled low	70	—	ns
tCKLDRL	$\overline{DREQ}$ transition delay after $\overline{LPDREQ}$ is sampled low	—	265	ns
tDALPDL	$\overline{PDACK}$ transition delay after $\overline{DACK}$ goes low	—	170	ns
tLDHDRH	$\overline{DREQ}$ transition delay after $\overline{LPDREQ}$ goes high	—	140	ns
DRQDEL = 0: tLDHCKL	$\overline{LPDREQ}$ set-up time to be sampled high	75	—	ns
tCKLDRL	$\overline{DREQ}$ transition delay after $\overline{LPDREQ}$ is sampled high and XPC is requesting bus time	tCKHCKH	—	—
tCKLPDH	$\overline{PDACK}$ transition delay after $\overline{LPDREQ}$ is sampled high	—	160	ns

Symbol	Description	Min	Max	Unit
	DMA Daisy Chain Timing (Figure 19)			
tCKLDRL	Delay time between XPC relinquishing bus and requesting bus due to lower priority XPC	tCKHCKH	—	—
tDRHDAH	$\overline{DACK}$ response time to removal of $\overline{DREQ}$	0	tCKHCKH	—
DRQDEL = 1: tLDHPDH	$\overline{PDACK}$ transition delay after $\overline{LPDREQ}$ goes high	—	410	ns
tDAHCKL	$\overline{DACK}$ set-up time to be sampled high	20	—	ns
tCKLDRL	$\overline{DREQ}$ transition delay after $\overline{DACK}$ is sampled high	—	220	ns
	Interrupt Timing (Figure 20)			
tCKLINTL	Interrupt transition delay	0	140	ns
tREHINTH	Interrupt transition delay	0	150	ns
tINTHINTL	Time before next interrupt	1.5tCKHCKH	—	—
	Reset Timing (Figure 21)			
tCKLMRL	Time before asserting $\overline{MR}$ after power-on	2tCKHCKH	—	—
tMRLMRH	Reset pulse width	1.5tCKHCKH	—	—

* No parity errors and no wait states generated.
** 1-byte or word read.
† 6-byte read
†† 3-word read.

Symbol	Description	Min	Typ	Max	Unit
	Transmit Element Acknowledgement (Figure 22)				
tCKLDRH	DMA bus access time*	—	8.5tCKHCKH	—	—
tCKLRWL	R/$\overline{W}$ transition delay	0	—	160	ns
tASHASL	Address transition and set-up time	—	3tCKHCKH	—	—
tREHWEL	Interoperation delay time	—	3.5tCKHCKH	—	—

* No parity errors and no wait states generated.

Timing Diagrams

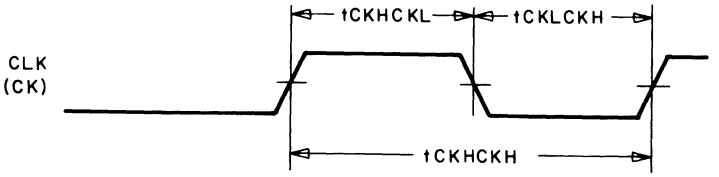
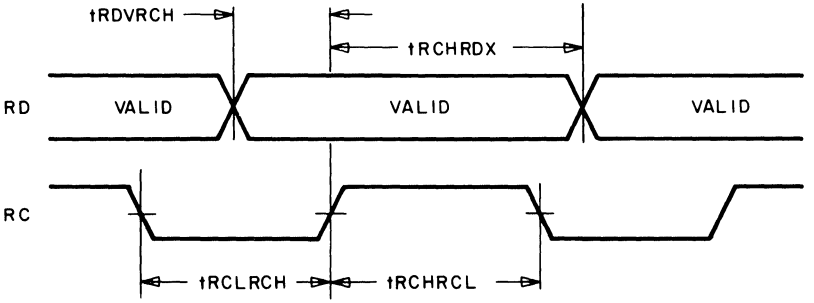


Figure 10. Clock Timing



Note: When in loopback modes and TC is tied to RC, the maximum delay on TD (tTCLTDX) meets the minimum RD set-up time (tRDVRCH) up to the maximum fTC = 6fCLK and fRC = 6fCLK.

Figure 11. Receive Clock Timing

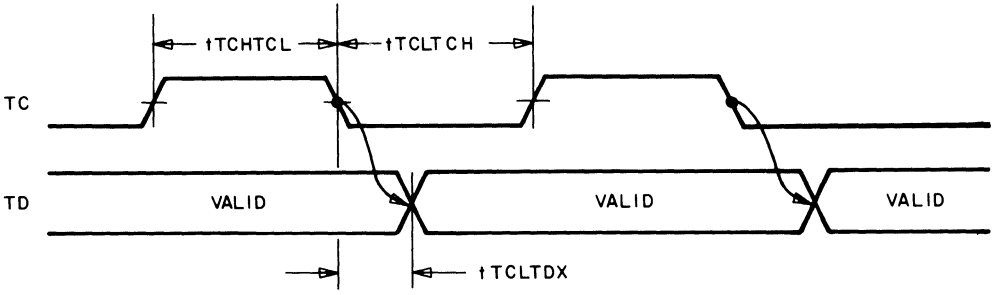
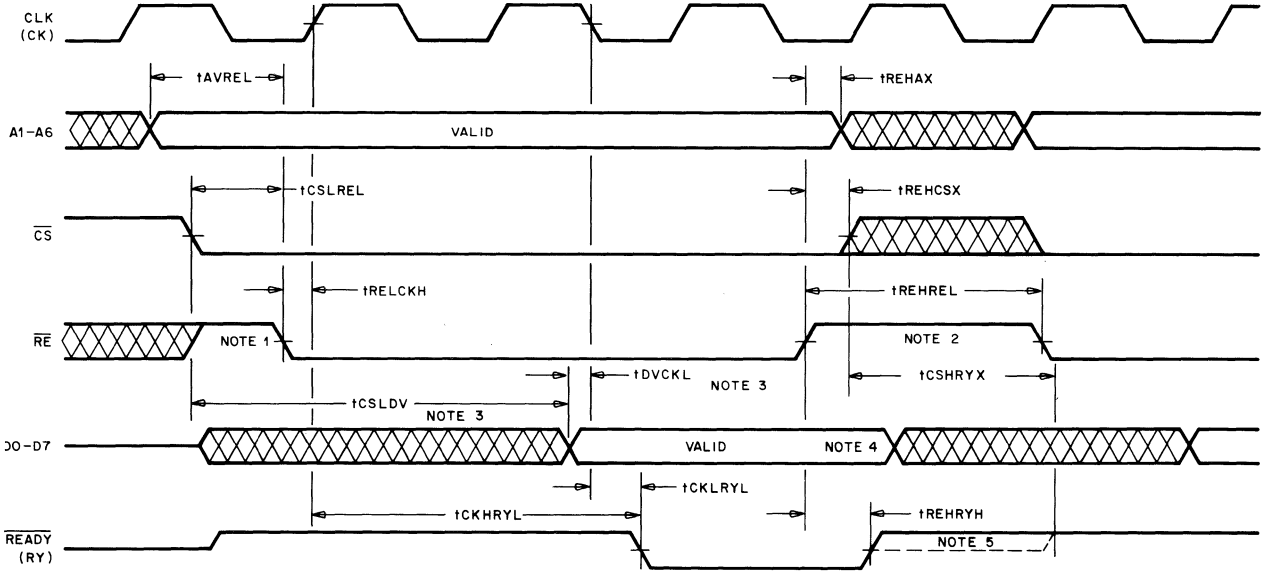
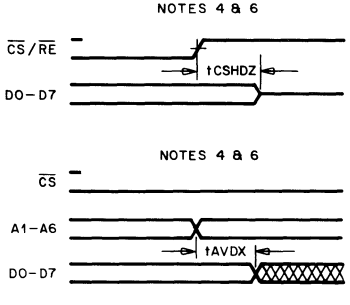


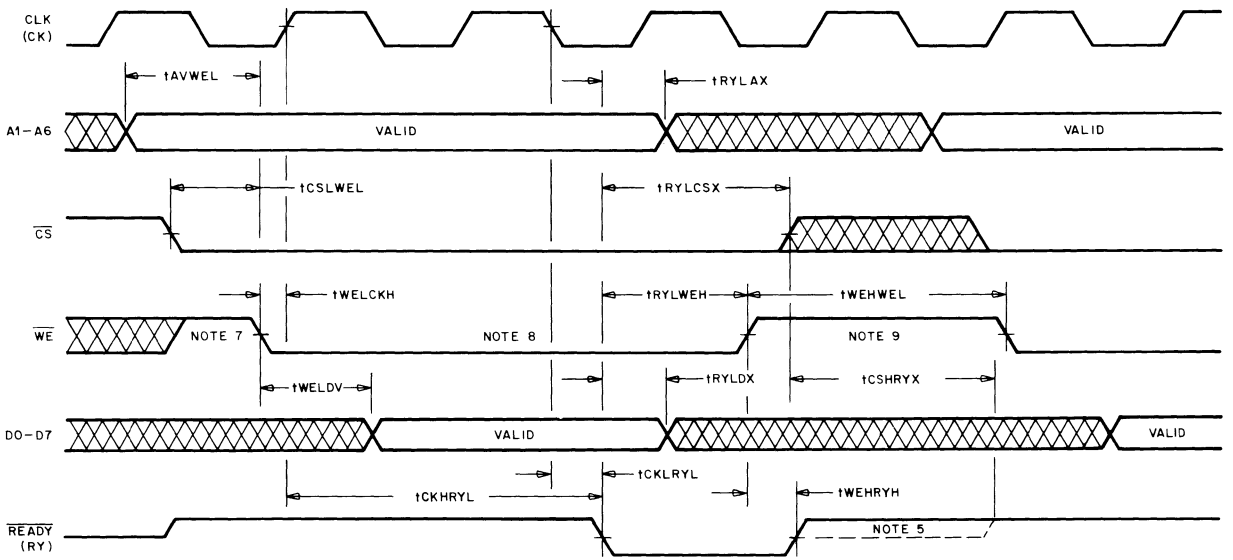
Figure 12. Transmit Clock Timing





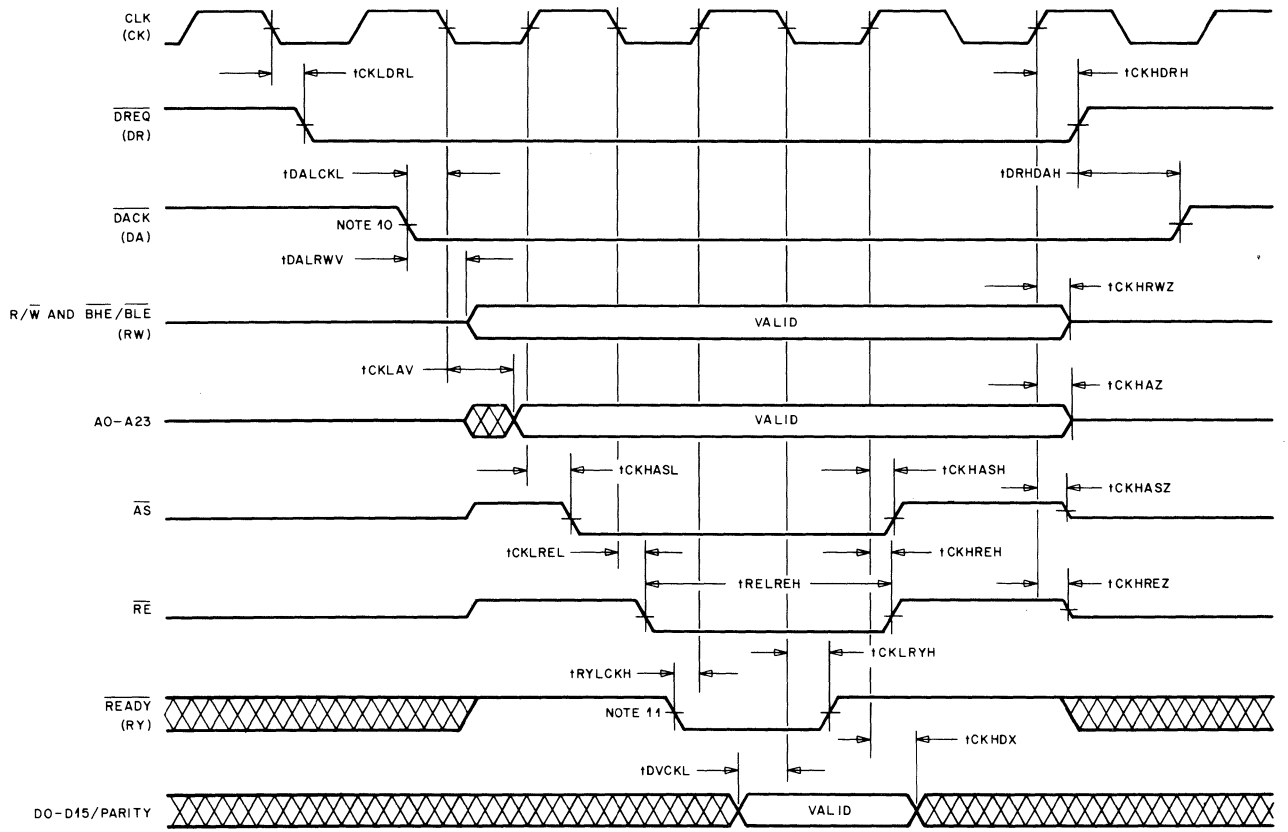
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 13. Reading XPC Registers



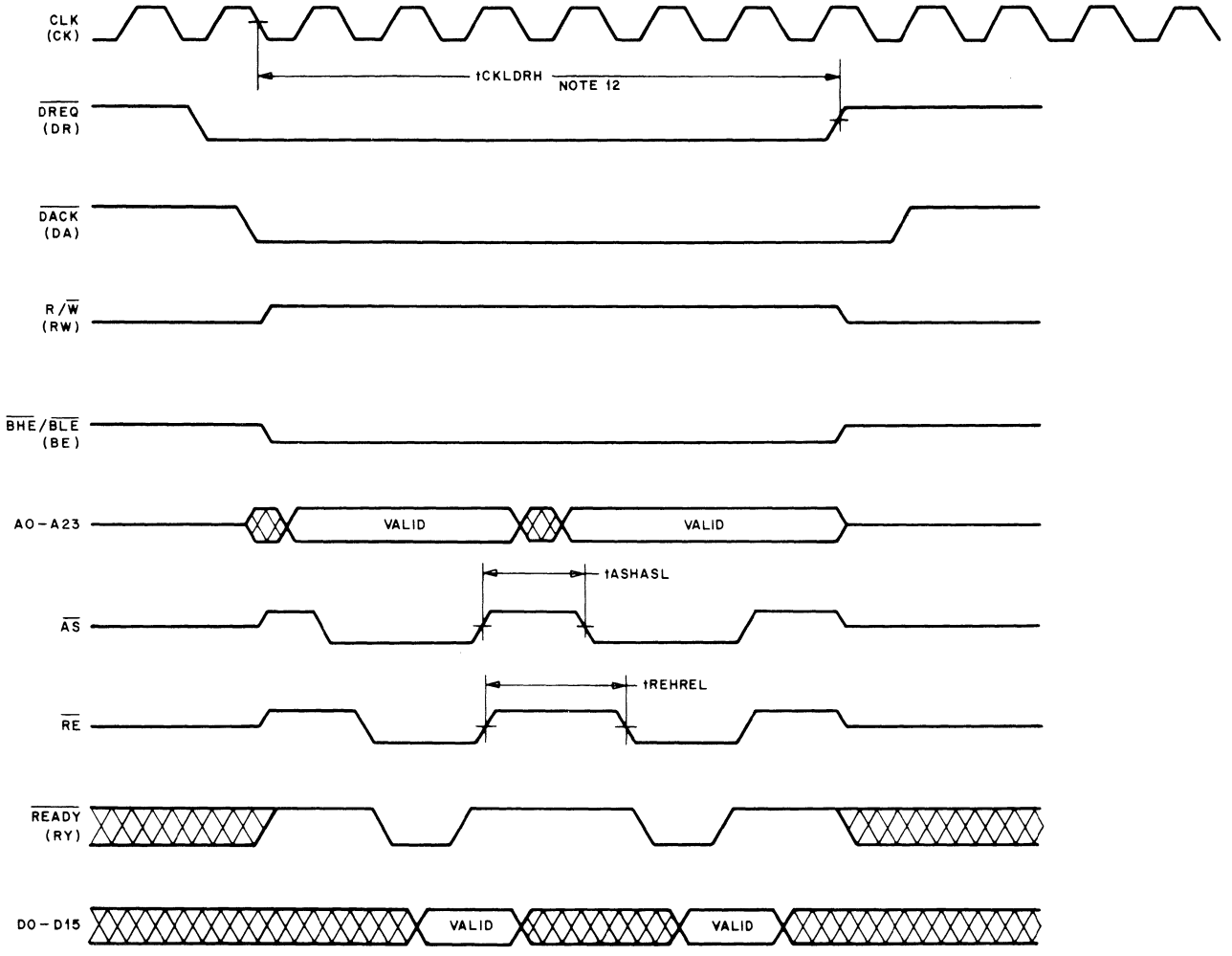
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 14. Writing XPC Registers



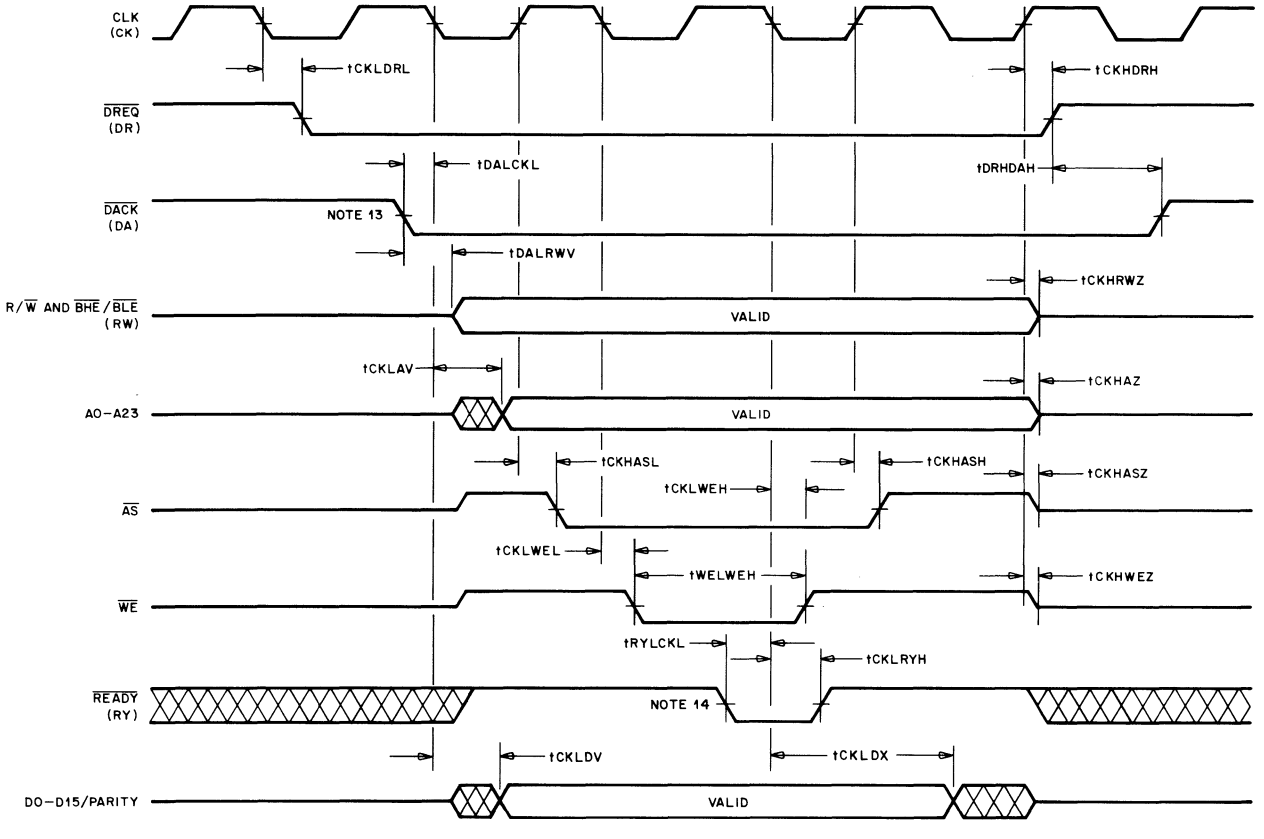
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 15. DMA Read Cycle



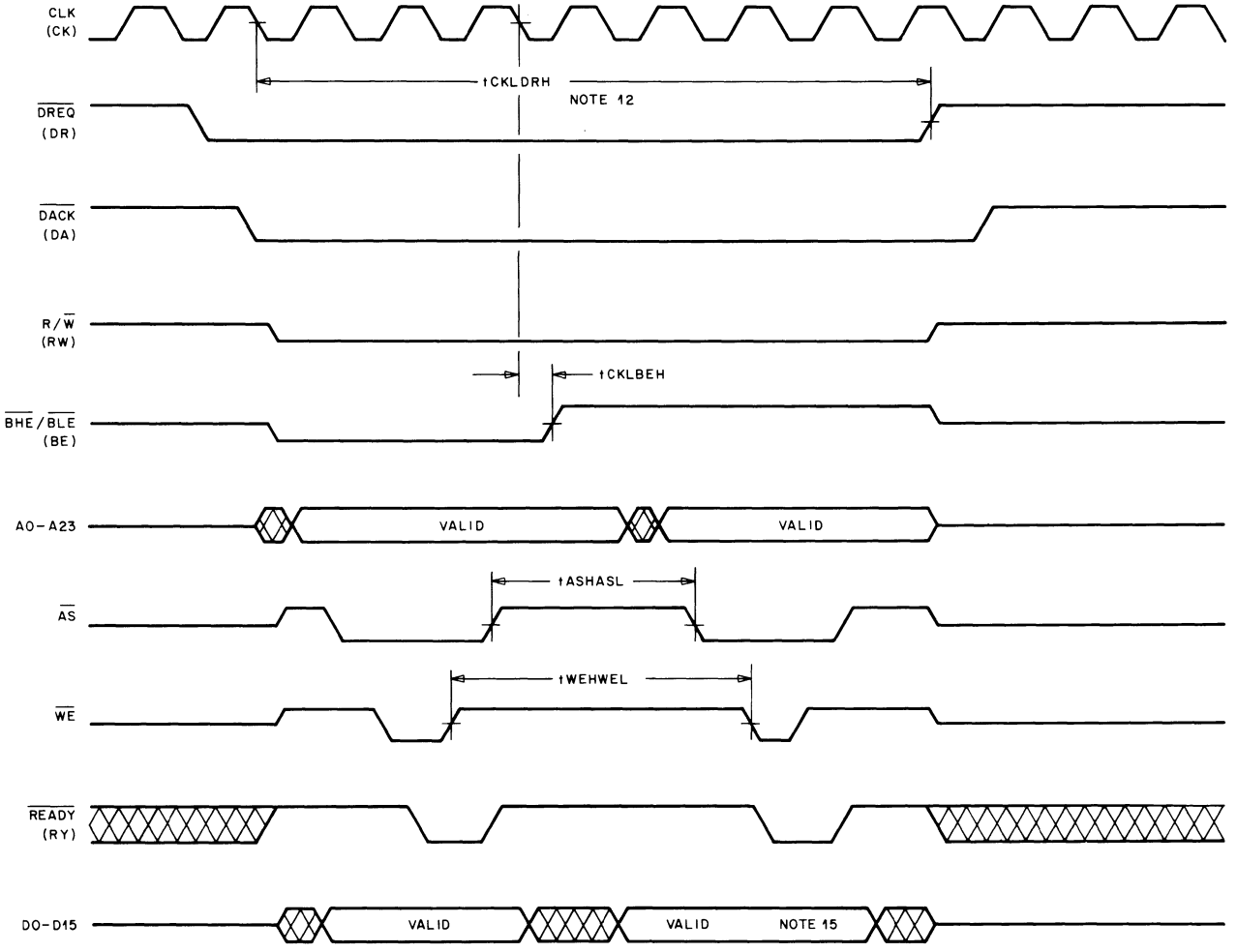
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 16. DMA Multiple Byte Read Operation



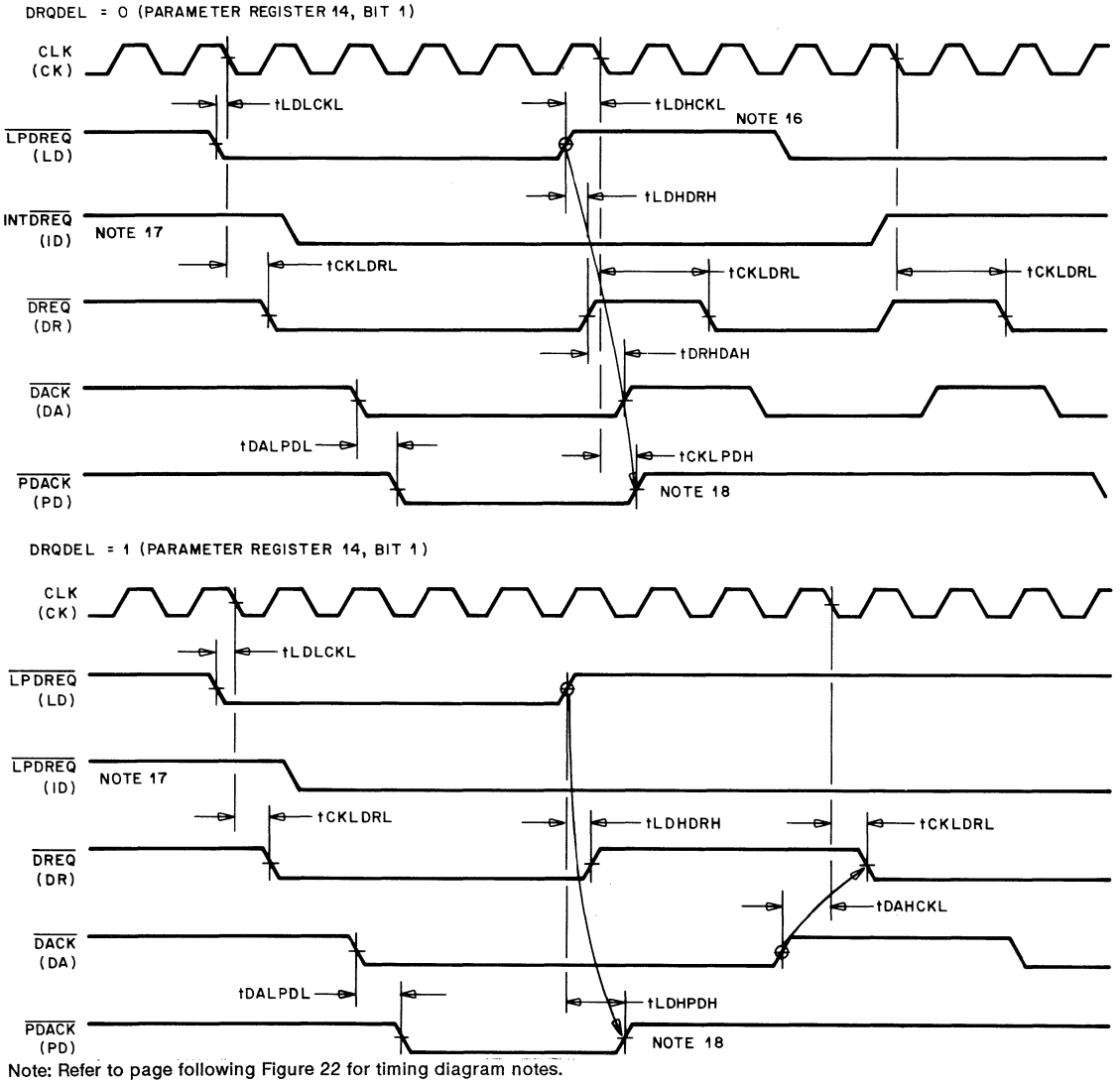
Note: Refer to page following Figure 22 for timing diagram notes.

Figure 17. DMA Write Cycle



Note: Refer to page following Figure 22 for timing diagram notes.

Figure 18. DMA Multiple Byte Write Operation



Note: Refer to page following Figure 22 for timing diagram notes.

Figure 19. DMA Daisy Chain Timing Between Any 2 XPC Devices

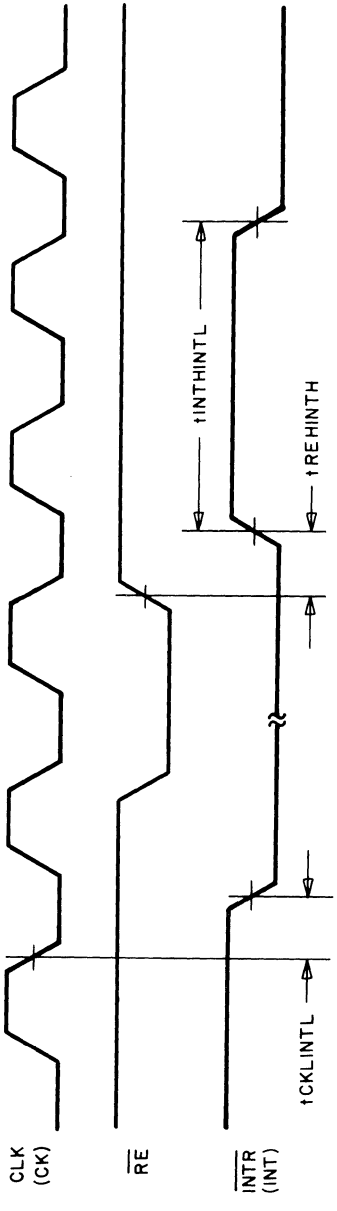


Figure 20. Interrupt Timing

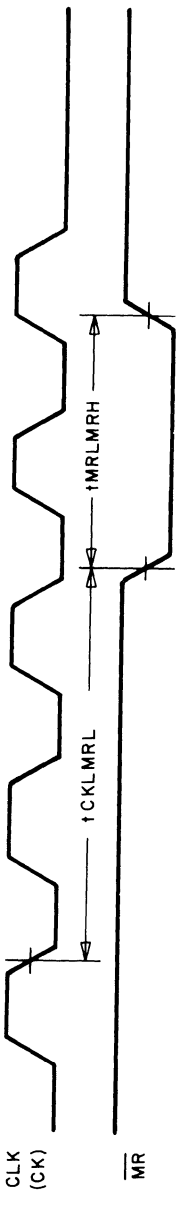
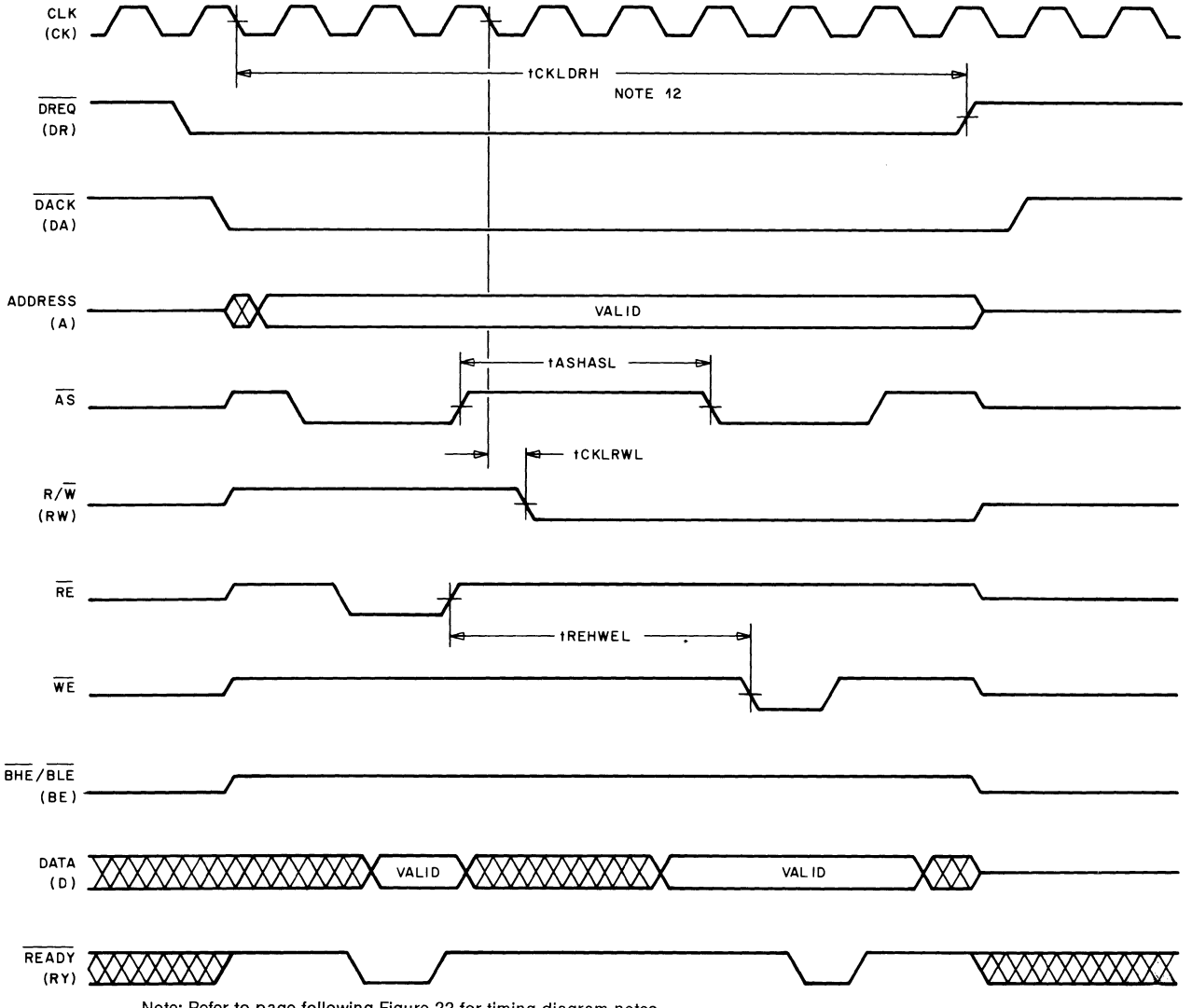


Figure 21. Reset Timing



Note: Refer to page following Figure 22 for timing diagram notes.

Figure 22. Transmit Element Acknowledgment (Read-Modify-Write)

Timing Diagram Notes

1. $\overline{RE}$ is sampled on the rising edge of CLK. Ready wait propagation does not begin until $\overline{RE}$ is sampled low.
2. tREHREL is also the minimum time before a write can occur.
3. When reading nonevent counter registers, tCSLDV should be used. tDVCKL is the time before the clock edge on which $\overline{READY}$ goes low that the event counter data is valid. tDVCKL should be used only when reading event counter registers.
4. Data remains on the data bus until $\overline{RE}$ goes high or the address changes. Data can change while $\overline{READY}$ is low and should be latched externally with the $\overline{READY}$ signal.
5. If $\overline{CS}$ is high, the XPC does not drive the $\overline{READY}$ pin.
6. $\overline{CS}$ can go high or remain low during an interoperation period.
7. $\overline{WE}$ is sampled on the rising edge of CLK. Ready-wait propagation does not begin until $\overline{WE}$ is sampled low.
8. The register is written some time within $\overline{WE}$ low window.
9. tWEHWEL is also the minimum time before a read can occur.
10. $\overline{DACK}$ is sampled on the falling edge of CLK. The read cycle does not begin until $\overline{DACK}$ is sampled low.
11. $\overline{READY}$ is sampled on the rising edge of CLK. The DMA enters a wait state until $\overline{READY}$ is sampled low.
12. tCKLDRH begins on the first falling edge of CLK after $\overline{DACK}$ is sampled low.
13. $\overline{DACK}$ is sampled on the falling edge of CLK. The write cycle does not begin until $\overline{DACK}$ is sampled low.
14. $\overline{READY}$ is sampled on the falling edge of CLK. The DMA enters a wait state until $\overline{READY}$ is sampled low.
15. D8—D15 (Intel mode: BYTORD = 0) or D0—D7 (Motorola mode: BYTORD = 1) is not valid if $\overline{BHE}/\overline{BLE}$ is high.
16. $\overline{LPDREQ}$ is sampled on the falling edge of CLK. tCKLDRL is measured from the edge on which $\overline{LPDREQ}$ is sampled high.
17. $\overline{INTDREQ}$ is the XPC internal DMA request. It is shown to illustrate the timing between two XPC devices.
18. The removal of $\overline{PDACK}$ is a function of $\overline{LPDREQ}$. $\overline{DACK}$ does not propagate from the CPU to remove $\overline{PDACK}$.

T7110 Synchronous Protocol Data Formatter with Serial Interface

Features

Host Interface

- Compatible with AT&T's *WE* 32100 Microprocessor and with Intel's iAPX86 and Motorola's MC68000 microprocessor series
- On-chip 16-channel DMA memory address generator with buffer manager, interrupt controller, and 4.1-Mbyte/s maximum data transfer rate
- Wait-state generator
- 16-bit data and 20-bit address buses
- Bus error handling
- Transmit and receive buffers accessible through memory-mapped look-up elements
- Parallel interrupts with full handshaking

Serial Interface

- 8-channel multiplexed serial input/output
- Automatic flag transmission and detection
- Zero-bit insertion and deletion
- CRC generation and detection, using CCITT-16 polynomial
- Detection of transmitter underrun and receiver overrun
- Abort/idle detection and transmission
- 2.048-Mb/s continuous serial data rate; 4.096-Mb/s maximum instantaneous data rate
- Up to 8 Kbytes per frame
- Programmable data inversion
- Near-end loop test and echo modes

Description

The T7110 Synchronous Protocol Data Formatter with Serial Interface (SPYDER-S) integrated circuit is a synchronous packet data communications controller device. It uses bit-synchronous (HDLC/SDLC) protocols to interface data link level lines with 16-bit or 32-bit microprocessor systems. All inputs and outputs of the T7110 SPYDER-S are TTL-compatible. The device is fabricated using CMOS technology, requires a single 5 V supply, and is available in a 68-pin postmolded plastic leaded chip carrier.

Note: A colon is used to separate symbol names that vary according to the microprocessor used. The symbol preceeding the colon refers to an iAPX86 interface (modes M2 and M3); the symbol following the colon refers to an MC68000 or *WE* 32100 Microprocessor interface (mode M4).

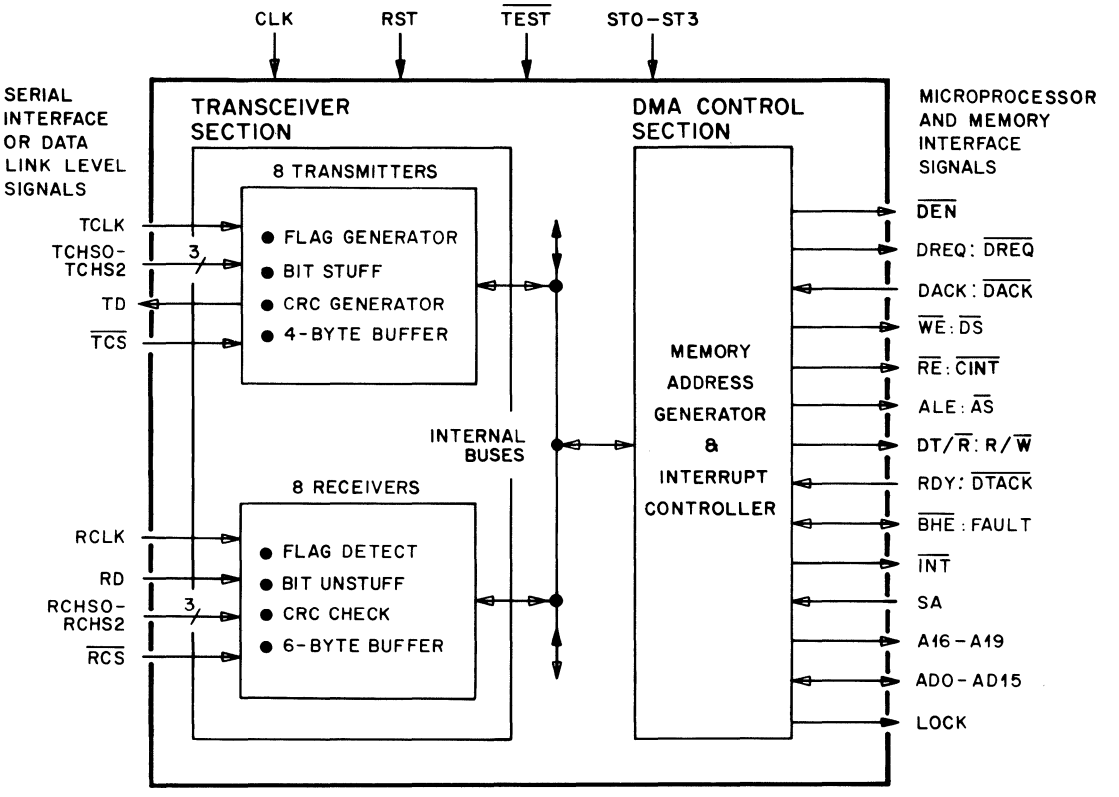


Figure 1. Simplified Block Diagram

T7111A Synchronous Packet Data Formatter

Features

Host Interface

- Compatible with 8088 and 80188 microprocessor-based systems and 8051 microcontroller
- Compatible with 8237 and 8257 DMA controllers in extended write mode
- Simple register control interface
- Wait-state initiator (80188)
- Receiver end-of-frame interrupt
- Programmable receive and transmit queue interrupts with variable fill levels
- Programmable receive and transmit DMA requests with variable fill levels

Serial Interface

- Full-duplex serial receive and transmit data lines
- Separate receive and transmit clocks
- 4 Mb/s maximum data rate
- Seven-byte receive queue
- Four-byte transmit queue
- Programmable request-to-send/clear-to-send handshaking
- Near- and far-end loop test modes
- Automatic flag transmission and detection
- Data metering via programmable interframe spacing
- Zero-bit insertion and deletion for data transparency
- CRC-CCITT 16-bit polynomial generation and check with inhibit option
- Abort/idle detection and transmission
- Detection of transmitter underrun and receiver overrun
- Optional inversion of serial bit streams

Description

The T7111A Synchronous Packet Data Formatter (ANT) integrated circuit is used to interface serial data link level lines, which use HDLC bit-synchronous protocol, to 8-bit microprocessor or microcontroller systems. All inputs and outputs of the T7111A ANT are TTL-compatible. It is implemented using CMOS technology and requires a single 5 V supply. The device is available in a 28-pin plastic DIP or small-outline J-lead (SOJ) package.

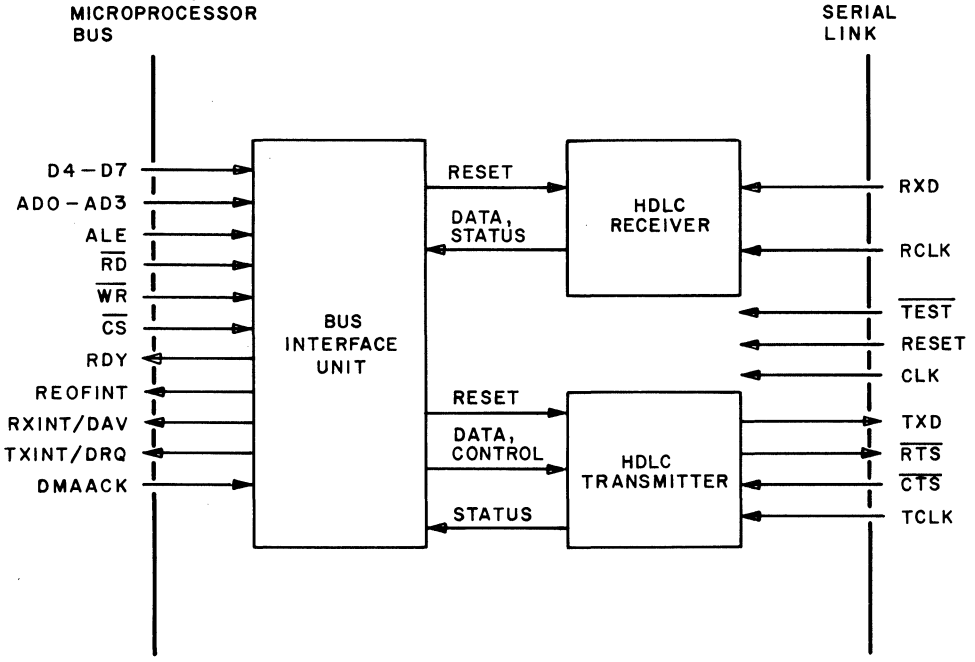
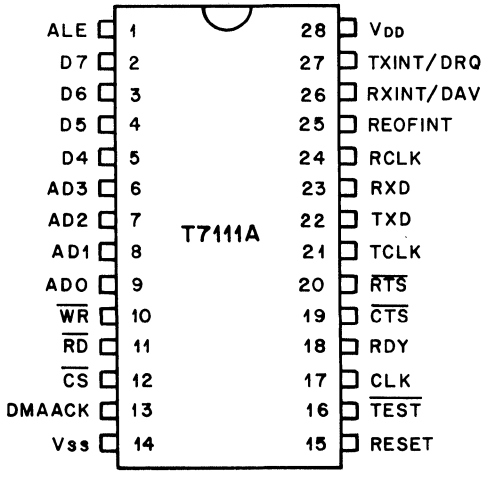


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
AD0	9	RD	11
AD1	8	RDY	18
AD2	7	REOFINT	25
AD3	6	RESET	15
ALE	1	RTS	20
CLK	17	RXD	23
CS	12	RXINT/DAV	26
CTS	19	TCLK	21
D4	5	TEST	16
D5	4	TXD	22
D6	3	TXINT/DRQ	27
D7	2	VDD	28
DMAACK	13	Vss	14
RCLK	24	WR	10

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	ALE	I	**Address Latch Enable.** When high, address inputs AD0—AD3 are latched on the falling edge of ALE.
2	D7	I/O	**Data Bus Bit 7.**
3	D6	I/O	**Data Bus Bit 6.**
4	D5	I/O	**Data Bus Bit 5.**
5	D4	I/O	**Data Bus Bit 4.**
			Bidirectional data bus
6	AD3	I/O	**Address/Data Bus Bit 3.**
7	AD2	I/O	**Address/Data Bus Bit 2.**
8	AD1	I/O	**Address/Data Bus Bit 1.**
9	AD0	I/O	**Address/Data Bus Bit 0.**
			Bidirectional, multiplexed address/data bus.
10	$\overline{WR}$	I	**Write Strobe (Active Low).** Write strobe is driven low by the microprocessor during a write access. Data is latched on the low-to-high transition of $\overline{WR}$.
11	$\overline{RD}$	I	**Read Strobe (Active Low).** Read strobe is driven low by the microprocessor during a read access. The ANT does not drive the data bus until $\overline{RD}$ is low.
12	$\overline{CS}$	I	**Chip Select (Active Low).** Must be low for the duration of a read or write pulse to ensure correct operation. $\overline{CS}$ should be asserted only during ANT read or write cycles; $\overline{CS}$ is not required for DMA transfers.
13	DMAACK	I	**DMA Acknowledge.** DMAACK functions as a secondary chip select during DMA cycles. Its assertion state is determined by the acknowledge polarity (ACKPOL) bit in the master configuration (MC) register. When DMAACK is active, the ANT's data bus is enabled. If DAV and $\overline{RD}$ are asserted, the ANT responds with a byte from the receiver queue; if DRQ and $\overline{WR}$ are asserted, the ANT latches a byte into the transmitter queue. If neither DAV (pin 26) nor DRQ (pin 27) is asserted, DMAACK is ignored.
14	V_{SS}	—	**Ground.**
15	RESET	I	**Reset.** When high for at least four clock cycles, all internal processes are terminated and the ANT returns to its idle state. All output pins are 3-stated while RESET remains active.
16	$\overline{TEST}$	I	**Test Mode.** Used to 3-state output pins during board testing. When unconnected, this pin is held high by an internal pull-up.
17	CLK	I	**System Clock.** 2-MHz to 8-MHz system clock input. The ANT can operate synchronously with the 8051, 8088, and 80188. If operating asynchronously, reference the System Clock section.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
18	RDY	O*	**Ready.** When high, indicates to 80188 microprocessor systems that the ANT is ready to complete a read or write transfer. Also used to insert wait-states into microprocessor read cycles. This output should be left unconnected when using 8051 microcontrollers or 8088 microprocessors. Reference RDY timing characteristics and the READ/WRITE Cycle and System Clock sections before connecting RDY to a particular microprocessor.
19	$\overline{CTS}$	I	**Clear-to-Send (Active Low).** Can be programmed to perform clear-to-send handshaking with a physical link controller when the level one control (LOC) bit in the MC register is set (1).
20	$\overline{RTS}$	O*	**Request-to-Send (Active Low).** Can be programmed to perform request-to-send handshaking with a physical link controller when the LOC bit in the MC register is set.
21	TCLK	I	**Transmit Data Clock.** Frequency is CLK/2 (pin 17), with a maximum of 4 MHz. Data is output on the falling edge of TCLK. There is no minimum TCLK frequency.
22	TXD	O*	**Transmit Data.** Serial data output. Can be inverted by setting the INV bit in the transmitter control (TC) register. Data is transmitted with least significant bit first.
23	RXD	I	**Receive Data.** Serial data input. Can be inverted by setting the INV bit in the TC register. The first bit received is the least significant bit on the data bus.
24	RCLK	I	**Receive Data Clock.** Frequency is CLK/2 (pin 17), with a maximum of 4 MHz. Data is sampled on the rising edge of RCLK. There is no minimum RCLK frequency.
25	REOFINT	O**	**Receiver End-of-Frame Interrupt.** When enabled and asserted, indicates that the receiver has detected the end of a frame. Assertion state is determined by the REOFPOL bit in the MC register. REOFINT is enabled by the REOFENB bit in the DIC register.
26	RXINT/DAV	O**	**Receiver Interrupt/Data Available.** Assertion state is determined by the D/IPOL bit in the MC register. When the DMA/I bit in the MC register is cleared (0), RXINT/DAV functions as an interrupt. RXINT is asserted when the number of bytes in the receiver queue equals or exceeds the setting of the RFL bits in the DIC register, unless it is disabled via the RDIENB bit in the DIC register. When the DMA/I bit in the MC register is set, RXINT/DAV functions as a DMA request. DAV is asserted when the number of bytes available is equal to the RFL; DAV is negated when the receiver queue is empty, unless it is disabled via the RDIENB bit in the DIC register.

* Indicates a 3-state condition.
** Open drain – pull-up resistor across output = 1000-Ω minimum.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
27	TXINT/ DRQ	O**	**Transmitter Interrupt/Data Request.** The assertion state is determined by the D/IPOL bit in the MC register. When bit DMA/I in the MC register is cleared, TXINT/DRQ functions as an interrupt. TXINT is asserted when the number of empty bytes in the transmitter queue equals or exceed the setting of the TEL bits in the DIC register, unless it is disabled via the TDIENB bit in the DIC register. When bit DMA/I in the MC register is set, TXINT/DRQ functions as a DMA request. DRQ is asserted when a number of empty bytes equal to the TEL are available; DRQ is negated when the transmitter queue is full, unless it is disabled via the TDIENB bit in the DIC register.
28	V_{DD}	—	**5 V Supply.**

Note: The ANT should be placed close to the microprocessor and a large ground plane should be provided.
* Indicates a 3-state condition.
** Open drain – pull-up resistor across output = 1000-Ω minimum.

Registers

The T7111A Synchronous Packet Data Formatter (ANT) contains 12 user-accessible registers. Access to the internal registers is through the bidirectional AD0—AD3 and D4—D7 pins. The four address bits are used to select the 8-bit registers. The registers are either read-only or write-only. Writing to a read-only register may result in the loss of data or status information. Reading from a write-only register causes the ANT to return an indeterminate value on the data bus. All reserved bits in a write-only register should be cleared; all reserved bits in a read-only register contain indeterminate values.

Table 2. Registers

Address	Symbol	Access Type	Name/Function
0000	IS	Write	**Interframe Spacing.** The value in this register, 0—255, determines the number of flags (TC register bit IDL = 0) or octets of 1s (IDL bit = 1) transmitted between frames.
0001	TS	Read	**Transmitter Status.** Indicates status of transmitter (see Table 3). Underrun status conditions are held until the TS register is read.

Table 2. Registers (Continued)

Address	Symbol	Access Type	Name/Function
0010	TC	Write	**Transmitter Control.** Controls termination of frames, loop tests, serial data inversion, and request-to-send handshaking. Inhibits CRC generation by simultaneously setting bits ABT and FC (see Table 4). On a reset, all bit values are cleared except for IDL. Setting IDL causes the transmitter to default to its idle state.
0011	TD	Write	**Transmitter Data.** Writes a byte, with a value in the range of 0—255, to the transmitter queue. Writing to TD removes the transmitter from its idle state. The transmit queue is cleared on a hardware, master, or transmitter reset.
0100	TR	Write	**Transmitter Reset.** A write to this address resets the transmitter and clears both TXINT in the interrupt register and the transmitter DMA request. The receiver and MC and DIC registers are not affected.
0101	RS	Read	**Receiver Status.** Indicates status of receiver. Overrun status conditions are held until RS is read (see Table 5). All bits are cleared on reset. Reading the RS register clears the REOF interrupt.
0110	RR	Write	**Receiver Reset.** A write to this address resets the receiver. The transmitter and the MC and DIC registers are not affected. RXINT and REOFINT in the interrupt register and the receiver DMA request are cleared.
0111	RD	Read	**Receiver Data.** Reads a byte, with a value in the range of 0—255, from the receiver queue. The receiver queue is cleared on a hardware, master, or receiver reset, or on an overrun.
1000	MC	Write	**Master Configuration.** These bits determine the configuration of selected pins regarding functionality, assertion state, and transmitter and receive enabling (see Table 6). All bits are cleared on a hardware or master reset.
1001	DIC	Write	**DMA/Interrupt Configuration.** These bits determine the configuration of DMA requests and interrupts (see Table 7). All bits are cleared on a hardware or master reset.
1010	IR	Read	**Interrupt.** Indicates which interrupts are currently active (see Table 8). Reading this register clears the REOF interrupt.
1100	MR	Write	**Master Reset.** A write to this address resets the chip.

Table 3. TS Register Bit Assignments (Read-Only)

Bit	Symbol	Name/Function
1, 0	DF1, DF0	**Encoded Transmission Queue Status.** **DF1** **DF0** **Meaning** 0 0 No data requested indicates queue is full or transmitter is not ready to accept new data 0 1 Request byte indicates queue has space for one more byte 1 0 Indicates transmitter underrun 1 1 Request word indicates queue has space for two more bytes
2	DONE	**Done.** When bits LOC and ACR in the MC register are set, this bit is set after the last bit of a closing flag or an abort sequence is sent to indicate the completed transmission of a frame. It is the inverse of the RTS bit in the TC register; hence, it is the value of the $\overline{RTS}$ pin.
7—3	—	**Reserved.**

Table 4. TC Register Bit Assignments (Write-Only)

Bit	Symbol	Name/Function
0	COU	**Close on Underrun.** Instructs the transmitter to close the frame normally in the underrun state, i.e., with CRC and closing flag. Must be set at least two TCLK cycles before underrun occurs. If this bit is set, the FC bit is not necessary.
1	RTS	**Request-to-Send.** If the LOC bit in the MC register is set, setting this bit activates the $\overline{RTS}$ pin; clearing this bit deactivates the $\overline{RTS}$ pin.
2	INV	**Invert.** When set, transmit and receive data streams are inverted.
3	FC	**Frame Close.** Instructs the transmitter to close the frame with CRC (ABT = 0) or without CRC (ABT = 1) after queue clears. If the COU bit is set, this bit is not necessary. Once set, this bit cannot be cleared via software. It is cleared automatically when the last data byte for this frame is transmitted.

Table 4. TC Register Bit Assignments (Write-Only) (Continued)

Bit	Symbol	Name/Function
4	ABT	**Abort.** Instructs transmitter to abort current frame. When setting abort, COU bit must be cleared. Once set, this bit cannot be cleared via software. It is cleared automatically when the abort sequence begins.
5	IDL	**Idle.** When set, instructs transmitter to enter the idle state when the queue is empty. This bit is set whenever a reset occurs. When set, octets of 1s are continuously transmitted; when clear, flags (01111110) are continuously transmitted when the queue is empty.
6	FELT	**Far-End Loop Test.** Places transmitter in far-end loop test mode. All received bits are retransmitted transparently.
7	NELT	**Near-End Loop Test.** Places transmitter in near-end loop test mode. All transmitted bits are looped back to the receiver.

Table 5. RS Register Bit Assignments (Read-Only)

Bit	Symbol	Name/Function
1, 0	DF1, DF0	**Encoded Receiver Queue Status.** **DF1 DF0 Meaning** 0 0 Null, queue empty 0 1 Byte available in queue 1 0 Receiver overrun 1 1 Two or more bytes available in queue
2	BBC	**Bad Byte Count.** When set, indicates that a nonintegral number of bytes have been received.
3	BFRM	**Bad Frame.** When set, indicates that the CRC is not correct. It is set when two or less bytes from a complete frame remain in the queue.
4	GFRM	**Good Frame.** When set, indicates that the CRC is correct. It is set when two or less bytes from a complete frame remain in the queue.
5	IDL	**Idle.** When set indicates that the idle sequence (fifteen 1s) is detected.
6	ABT	**Abort.** When set, indicates that the abort sequence (01111111) is detected after three or more data or CRC bytes have been received.
7	LLI	**Lost Local Interrupt.** This bit is set if there is a change of status (end-of-frame, idle, abort, or overrun) before the first receiver status or outstanding data has been read.

Table 6. MC Register Bit Assignments (Write-Only)

Bit	Symbol	Name/Function
0	ACKPOL	**Acknowledge Polarity.** Determines the assertion state of the DMAACK pin. When cleared, DMAACK is active-low; when set, DMAACK is active-high.
1	REOFPOL	**Receiver End-of-Frame Interrupt Polarity.** Determines the assertion state of the REOF interrupt. When cleared, REOF is active-low; when set, REOF is active-high.
2	D/IPOL	**DMA/Interrupt Polarity.** Determines the assertion state of the RXINT/DAV and TXINT/DRQ pins. When cleared, both are active-low; when set, both are active-high.
3	DMA/I	**DMA/Interrupt.** Determines the function of the RXINT/DAV and TXINT/DRQ bits. When cleared, they are interrupts; when set, they are DMA requests.
4	ACR	**Auto-Clear RTS.** When the ACR and the LOC bits are set, the ANT automatically clears RTS in the TC register at the conclusion of the current frame. When ACR is clear, bit RTS must be cleared via software. If the ACR feature is used, the IS register must have a value of at least 1 to prevent shared flags between frames.
5	LOC	**Level One Control.** When cleared, $\overline{\text{CTS}}$ (pin 19) and $\overline{\text{RTS}}$ (pin 20) are disabled and the level one control function is not implemented. When set, both $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$ must be active for data to be transmitted.
6	TENB	**Transmitter Enable.** When set, allows data to be output via TXD (pin 22); when cleared, TCLK is ignored and TXD is 3-stated.
7	RENB	**Receiver Enable.** When set, allows data to be input via RXD (pin 23); when cleared, the RXD input is ignored and the internal state of the receiver is not affected.

Table 7. DIC Register Bit Assignments (Write-Only)

Bit	Symbol	Name/Function
1, 0	TEL1, TEL0	**Transmitter Empty Level.** Establishes the number of empty bytes in the transmitter queue that triggers a transmitter interrupt or DMA request. These bits are encoded as: 00 4 bytes empty (default) 01 1 or more bytes empty 10 2 or more bytes empty 11 3 or more bytes empty

Table 7. DIC Register Bit Assignments (Write-Only) (Continued)

Bit	Symbol	Name/Function
3, 2	RFL1, RFL0	**Receiver Fill Level.** Establishes the number of bytes in the receiver queue that triggers a receiver interrupt of DMA request. These bits are encoded as: 00 4 bytes available (default) 01 1 or more bytes available 10 2 or more bytes available 11 3 or more bytes available
4	REOFENB	**Receiver End-of-Frame Interrupt Enable.** When MENB and REOFENB are set, REOFINT (pin 25) is enabled. Disabling the REOFINT does not clear the existing interrupt.
5	TDIENB	**Transmitter DMA/Interrupt Enable.** When MENB and TDIENB are set, TXINT/DRQ (pin 27) is enabled. Disabling TXINT/DRQ does not clear the existing interrupt.
6	RDIENB	**Receiver DMA/Interrupt Enable.** When MENB and RDIENB are set, RXINT/DAV (pin 26) is enabled. Disabling the RXINT/DAV does not clear the existing interrupt.
7	MENB	**Master Enable.** When cleared, disables all DMA and interrupt outputs; when set, along with TDIENB, RDIENB or REOFENB, all DMA and interrupt outputs are enabled.

Table 8. I Register Bit Assignments (Read-Only)

Bit	Symbol	Name/Function
0—4	—	**Reserved.**
5	REOFINT	**Receiver End-of-Frame Interrupt.** When set, indicates that the receiver end-of-frame interrupt is asserted. This bit is independent of the interrupt enable bits in the DIC register; therefore, this bit remains set if the interrupt enable bits are disabled. This bit is cleared after this register, or the RS register, is read.
6	TXINT	**Transmitter Interrupt.** When set, indicates that the transmitter queue interrupt is asserted. This bit is independent of the interrupt enable bits in the DIC register; therefore, this bit remains set if the interrupt enable bits are disabled.
7	RXINT	**Receiver Interrupt.** When set, indicates that the receiver queue interrupt is asserted. This bit is independent of the interrupt enable bits in the DIC register; therefore, this bit remains set if the interrupt enabled bits are disabled.

Operation

The T7111A Synchronous Packet Data Formatter operates with a system clock frequency of 2 MHz to 8 MHz. The frequency of operation is dependent upon the host microprocessor operating frequency but does not have to be synchronous with it. See the Read/Write Cycles section for a complete description. Serial data is transmitted on TXD (pin 22) and output on the high-to-low transition of TCLK. It can be transmitted when $\overline{RTS}$ and $\overline{CTS}$ are active (low) if the LOC bit in the MC register is set; otherwise, these pins are ignored. Serial data is received from RXD (pin 23) and sampled on the rising edge of RCLK (see Figure 3).

16-bit Polynomial Cyclic Redundancy Check (CRC-CCITT) and Generation with Inhibit Option

As the transmitter shifts serial data out for a frame, it computes the 16-bit CRC-CCITT pattern. The frame close (FC) bit in the transmitter control (TC) register is set by the host processor after the last data byte is written to the TD register, unless the COU bit has been set. Both the DF0 and DF1 bits in the transmitter status (TS) register are cleared to stop the transmitter from requesting data. When the last data byte has been transmitted and the CRC has begun, the transmitter is ready to accept new data and sets the DF0 and DF1 status bits (word request). After the CRC pattern is transmitted, a flag is appended to the pattern and data for a new frame, if available, is transmitted. The CRC pattern is not appended to the data if the abort bit is set at the same time as the FC. The transmitter closes the frame with a flag after the last data byte. When the CRC option is not in use, the IDL bit in the TC register must be cleared.

As the receiver shifts the serial data input for a frame, it computes the CRC pattern. When the closing flag is received, the last two data bytes received are assumed to be CRC and are cleared from the queue. If no more than two bytes from the frame remain in the queue, the receiver sets either the GFRM or BFRM status bit, depending on whether or not the CRC matches. If the BFRM bit is set, the remaining data must still be read out from the queue.

Abort/Idle Detection and Transmission

When the receiver recognizes the abort sequence (seven successive 1s), data from the current frame and the CRC are cleared; data from a following frame is written to the queue after a flag is recognized. If an abort sequence is received when less than three complete bytes have been received, the abort bit is not set. If three or more bytes have been received, but there is outstanding data or an outstanding end-of-frame condition from a previous frame in the queue, the lost local interrupt (LLI) bit is set. When the receiver recognizes the idle sequence (15 successive 1s), the IDL bit in the RS register is set and remains set as long as the link is idle.

When the ABT bit in the TC register is set, the transmitter is instructed to abort the current frame. The transmitter shifts out the rest of the current data byte and then transmits the abort sequence. The queue and the CRC generator are cleared and the transmitter is ready to accept data from a new frame. If no new data is written and the IDL bit in the TC register is set, the transmitter is in the idle state, where it continuously transmits octets of 1s until data is available. If no new data is written and the IDL bit is cleared, the transmitter transmits flags until data is available.

The value of the IDL bit also determines the interframe spacing pattern. If it is set, the number of octets of 1s equal to the interframe spacing value is transmitted between the closing and opening flags of successive frames. When the transmitter is idling and data is written to the TD register, the number of octets of 1s equal to the interframe spacing value is transmitted before that frame. The first byte written signals the start of the interframe spacing count.

Transmitter Underrun and Receiver Overrun Detection

During transmission of a frame, the transmitter underruns if neither the FC bit nor the COU bit in the TC register is set by the time the last data byte is shifted out. The abort sequence follows the last byte shifted out during underrun. If the queue is empty, the transmitter transmits flags (IDL = 0) or octets of 1s (IDL = 1) following the abort sequence.

The underrun condition is reflected in the transmitter status bits. Writes to the FC bit and the TD register are ignored until the status is read. A write to the ABT bit clears the underrun status. After the status has been read, the transmission queue status bits, DF0 and DF1, are set to "word requested." If the ACR bit is set, RTS is deactivated at the end of the abort sequence.

If the 7-byte limit on the receive queue is exceeded, i.e., data is received faster than it is read out, the receiver enters the overrun state. The receiver queue status bits, DF0 and DF1, reflect the overrun condition.

On an overrun, the receiver queue is cleared and cannot be read until the RS register is read. Received data from a subsequent frame can be written to the queue. If a second overrun occurs before the first status is read, no more data is accepted until after the status is read and LLI is set. After the overrun status is read, the status reflects the number of bytes currently available in the queue.

Automatic Flag Transmission and Detection with Programmable Interframe Spacing

When data is written to the transmit queue, the transmitter automatically generates an opening flag before it transmits the data. When the FC bit in the TC register is set, a closing flag is appended to the frame after the CRC pattern. If the queue is not empty when the closing flag is sent, the next frame begins immediately. If the interframe spacing value is 0, a single flag serves the dual role of closing and opening flag for the two frames. If two separate flags are required, the interframe spacing value should be set. When IDL = 0, the number of flags equal to the interframe spacing value is transmitted after the closing flag and before the data for the next frame. If IDL = 1, the octets of 1s equal to the interframe spacing value is transmitted after the closing flag and before the opening flag for the next frame. After the transmitter is reset, if data is in the transmit queue, it transmits one flag before the first frame and appends the IS value of flags or octets of 1s after the closing flag. When two successive flags occur, a full 16 bits are transmitted, i.e., 0111111001111110.

The receiver recognizes the pattern 01111110 as a flag. Two successive flags may or may not share the intermediate zero bit and still be recognized, i.e., 0111111001111110 or 011111101111110. When the receiver queue is empty and it recognizes a flag, it begins to format the subsequent bits into bytes until it recognizes another flag or an abort sequence. The bytes are stored in the 7-byte receiver queue. When the closing flag is recognized, the last two bytes are cleared from the queue for the CRC pattern. The GFRM, BFRM, or BBC bits in the RS register are set when two or less bytes from the frame remain in the receiver queue. If a second frame is received before the receiver status or outstanding data from the first frame is read, the LLI bit in the RS register is set and the data from the second frame is cleared from the queue.

Zero-Bit Insertion and Deletion

During transmission, when five successive 1s occur in either the data or CRC, the transmitter automatically inserts a 0 bit after the fifth 1, regardless of the value of the next bit. When five successive 1s followed by a 0 are received, the 0 is assumed to have been inserted by the transmitter and is ignored. This eliminates the possibility of misinterpreting data or CRC patterns as flag, abort, or idle patterns.

Request-to-Send/Clear-to-Send Level One Functions

The $\overline{\text{RTS}}$ and $\overline{\text{CTS}}$ pins can be programmed to perform request-to-send/clear-to-send handshaking with a physical link controller. When the level one control (LOC) bit in the MC register is set, the specified protocols are performed. The host processor must set, by software, the RTS bit in the TC register when it is ready to begin transmission of a new frame. The $\overline{\text{RTS}}$ pin is activated when the RTS bit is set.

The RTS bit is cleared (causing the $\overline{RTS}$ pin to become inactive) upon a hardware (pin 15 asserted), a software, or transmitter reset. In addition, if autoclear RTS is active (ACR = 1), the RTS bit is cleared when one of the following conditions occurs:

- End of the closing flag of a normal frame
- End of the abort sequence of an aborted frame
- End of the abort sequence after an underrun.

If the ACR feature is used, the interframe spacing register must be set to a value of at least 1. This is necessary to ensure separate closing and opening flags. RTS is cleared at the end of the closing flag. When the transmitter is reactivated, a number of flags equal to the setting of the IS register are transmitted before the first data byte. If the abort bit is set while the transmitter is sending the opening flag of the frame, the abort pattern is not transmitted. RTS clears as soon as this bit is set, causing transmission to stop. The next time RTS is set, the remaining bits of the flag are sent before the new frame begins.

If the ANT device is not in the autoclear RTS (ACR = 0) mode, the only condition that clears RTS, other than the reset conditions, is a write to the RTS bit in the TC register.

When the LOC bit in the MC register is set, the clear-to-send ($\overline{CTS}$) input pin is enabled. When $\overline{CTS}$ is enabled, the level one controller responds to the assertion of $\overline{RTS}$ with the assertion of $\overline{CTS}$ when the physical link is available for transmission by the ANT device. The ANT device responds by transmitting data as long as both $\overline{RTS}$ and $\overline{CTS}$ are active (low). If the queue is empty, the transmitter transmits either flags or octets of 1s until data is available. When $\overline{CTS}$ is enabled but inactive (high), the transmitter is disabled from transmitting anything across the serial interface and the TXD (pin 22) is 3-stated.

The DONE bit in the TS register reflects the state of the $\overline{RTS}$ pin. DONE is cleared when $\overline{RTS}$ is asserted low; it is set when $\overline{RTS}$ is negated. It is used by the host processor to determine whether RTS can be set for the transmission of another frame. If ACR = 1 and RTS is set for another frame before it is cleared from the previous frame, RTS is cleared at the end of the first frame, but the output is not reasserted unless set via software.

Near-End and Far-End Loop Test Modes

When the NELT bit in the TC register is set, the ANT device is in the near-end loop test mode. In this mode, all data that is transmitted on the TD line is looped-back internally to the receiver. The receiver cannot distinguish between the looped-back data and data received normally; therefore, all status, configuration, and interrupt conditions function as usual.

Setting the FELT bit in the TC register puts the ANT device in the far-end loop test mode. In this mode, all received data is echoed by the transmitter in a "dumb" fashion, while the receiver functions as usual.

Read/Write Cycle

To perform a read or write operation, the chip select ($\overline{CS}$) pin must be low (active) for the duration of the read or write pulse.

Write cycles never have wait states inserted. The ANT is always ready to accept data as long as the trailing edges of the $\overline{WR}$ pulses are separated by at least three ANT clock cycles, the write pulse meets the minimum width requirement, and the data is set-up to the rising edge of the $\overline{WR}$ pulse (see Figure 4).

Read cycles can have wait states inserted. On read cycles without wait states, RDY is driven high on the falling edge of $\overline{RD}$. (see Figure 5). If a wait state is inserted, RDY is driven low on the falling edge of RD and is driven high on the rising edge of CLK in the next cycle. A single wait state is inserted under the following conditions:

- If a read access to the TS register immediately follows a write to one of the transmitter registers (see Figure 6), or
- If a read to the RS register immediately follows a read of the RD register (see Figure 7).

On all other read cycles, no wait states are needed.

The RDY signal is only needed for the 80188 Microprocessor. In 8051 or 8088 systems, the accesses described above should be avoided in the code by inserting a single NOP. This is not sufficient for the 80188 if the on-board DMA controllers are accessing the ANT. In this case, a status read may immediately follow a DMA data transfer without any intervening clock cycles.

In systems using 8237 or 8257 DMA controllers, wait states are not needed and the RDY signal can be left unconnected. If RDY is used, the DMA controllers should be configured for extended write mode to allow the RDY signal time to be driven high.

System Clock

The 8051 microcontroller requires a clock input from a crystal or a square-wave source. If a crystal is used, the ANT must be clocked asynchronously; if a square-wave source is used, the ANT can be clocked synchronously or asynchronously. If the ANT is clocked asynchronously, the relationship between the period of the microcontroller's clock (t8051) and the ANT's clock (tANT) is given by:

$$tANT \leq 5t8051 - 245 \text{ ns}$$

For example, to be compatible with an 8051 microcontroller operating with a 12-MHz clock, the ANT requires an input clock of at least 6 MHz.

The 8088 microprocessor requires a square-wave clock input with a 33% duty cycle. The ANT should be supplied with the same clock input and operate synchronously with the microprocessor. The ANT is compatible with a 33% duty cycle clock at 8 MHz (as specified for the 8088 microprocessor), i.e., minimum clock high time of 44 ns.

The 80188 microprocessor requires a clock input from either a crystal or a square-wave source. The microprocessor provides a 50% duty cycle square-wave output of one-half the frequency of the clock input. The microprocessor's clock output should be the ANT's system clock input.

The ANT can operate asynchronously with the microprocessor; however, the $\overline{RD}$ low to data valid parameter, tRELDBV, of one ANT clock cycle plus 70 ns and the $\overline{WR}$ pulse width, tWRLWRH, of one ANT clock cycle plus 35 ns must be considered. If this specification cannot be met, wait states must be inserted in the ANT read and write cycles. The RDY signal cannot be used for this purpose. Either the wait states must be programmed in the processor, or external RDY logic must be provided. Wait states are inserted only in the read accesses described in the previous section (see Figures 6 and 7). During any other read access, RDY is driven high on the falling edge of the $\overline{RD}$ strobe and no wait states are inserted. Reference the timing characteristics of RDY before connecting RDY to a particular microprocessor.

DMA Read/Write

When the DMA/I bit in the MC register is set, RXINT/DAV and TXINT/DRQ function as DMA request pins. Their assertion state, along with that of DMAACK, is determined by the status of D/IPOL (bit 2) and ACKPOL (bit 0), respectively, in the MC register. DAV is asserted when the receiver queue fill level is equal to or greater than the setting of the RFL bits (2,3) in the DMA/interrupt configuration (DIC) register. It remains asserted until the queue is empty. DRQ is asserted when the transmitter queue has room to accommodate a number of bytes equal to or greater than the setting of the TEL bits (0,1) in the DIC register. It remains asserted until the queue is full.

If DAV is asserted and a DMAACK is received, the ANT drives a byte of data from the receiver queue onto the bus after the read strobe ($\overline{RD}$) signal is asserted (low). Once the $\overline{RD}$ strobe goes low, data is valid by 70 ns after the next falling edge of CLK (see Figure 8).

If DRQ is asserted and a DMAACK signal is received, the ANT latches a byte of data from the bus into the transmitter queue on the low-to-high transition of the write strobe ($\overline{WR}$) signal. The ANT is always ready to accept data if the timing requirements are met (see Figure 9). DMAACK must be active for the duration of the read or write pulse to ensure correct operation. $\overline{CS}$ and the address bus inputs are not needed for the DMA transfers.

Interrupts

The ANT device can be programmed to provide three separate interrupts: receiver, transmitter, and receiver end-of-frame. The interrupts are enabled by setting the appropriate bits in the DIC register: RDIENB (bit 6), TDIENB (bit 5) and REOFENB (bit 4), respectively. The assertion state of the bits is determined by the value of the appropriate bits in the MC register. REOFINT becomes active upon reception of the last bit of the closing flag of a frame, the last bit of an abort sequence, or upon overrun, providing there are no outstanding data bytes or status bits from a previous frame. If data or status is outstanding, the second frame is lost and the LLI bit in the RS register is set. REOFINT remains asserted until the I register or the RS register is read, unless disabled via the DIC register.

When the DMA/I bit in the MC register is cleared, RXINT/DAV and TXINT/DRQ function as interrupts. RXINT is asserted when the receiver queue fill level is equal to or greater than the setting of the RFL bits in the DIC register. RXINT is not asserted when the queue overruns, but REOFINT is asserted. TXINT is asserted upon underrun or when the transmitter queue has enough empty slots to accommodate a number of bytes equal to or greater than the setting of the TEL bits in the DIC register. Once the FC bit has been set, TXINT is negated until the transmission of that frame is complete. TXINT remains asserted if the queue underruns. When servicing the TXINT, the TS register must be read before data is written into the TD register.

Reset

The reset signal must be held high for at least four clock cycles to reset the ANT device. All registers are cleared on reset, except the IDL bit in the TC register. The receive and transmit queues are cleared also. All output pins are 3-stated for as long as the reset signal is held high. The ANT device is guaranteed to be fully reset within 3 clock cycles after the high-to-low transition of reset. A write to the master reset address (1100) has the same effect as a hardware reset. The ANT device is fully reset within 3 clock cycles of the low-to-high transition of the $\overline{WR}$ pulse.

A write to the receiver reset address (0110) resets the receiver only. The RS register and the receive queue are cleared. The transmitter, MC, and DIC registers are not affected. The receiver queue and end-of-frame interrupts in the interrupt register and the receiver DMA request are also cleared. The receiver is fully reset within 3 cycles of the low-to-high transition of the $\overline{WR}$ pulse.

A write to the transmitter reset address (0100) resets the transmitter. The TS register and transmitter queue are cleared along with the transmitter interrupt in the interrupt register and the the transmitter DMA request. The receiver and the MC and DIC registers are not affected by this write. The transmitter is fully reset within 3 cycles after the low-to-high transition of the $\overline{WR}$ pulse.

Characteristics

Clocks

System clock input: 2—8 MHz
Transmit data clock: Maximum frequency = CLK/2; no minimum frequency
Receive data clock: Maximum frequency = CLK/2; no minimum frequency

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Supply current	I_{DD}	—	55	mA	T_A = 0 °C
Input current:					
high	I_{IH}	—	7.5	μA	V_{IH} = 5.5 V
low	I_{IL}	—	7.5	μA	V_{IL} = 0 V
Input current (bidirectional pins):					
high	I_{IH}	—	–37.5	μA	V_{IH} = 5.5 V
low	I_{IL}	—	37.5	μA	V_{IL} = 0 V
Output 3-state (leakage current):					
high	I_{OZH}	—	–30	μA	V_{OH} = 5.5 V
low	I_{OZL}	—	30	μA	V_{OL} = 0 V
Input voltage:					
high	V_{IH}	2.0	—	V	—
low	V_{IL}	—	0.8	V	—
Output voltage:					V_{DD} = 4.5 V
high	V_{OH}	2.4	—	V	I_{OH} = –2.4 mA
low	V_{OL}	—	0.4	V	I_{OL} = 2.4 mA
Power dissipation	PD	—	80	mW	V_{DD} = 5.5 V T = 70 °C CLK = 8 MHz TCLK = RCLK = 4 MHz

Maximum Ratings

DC supply voltage (V_{DD}) ..... 7 V
Input voltage (V_I) range ..... V_{SS} – 0.5 to V_{DD} + 0.5 V
Ambient operating temperature (T_A) range ..... 0 to 70 °C
Storage temperature (Tstg) range ..... –40 to +125 °C

Maximum ratings are defined as the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Table 9. Timing Characteristics for Serial Transmit and Receive Data Cycle (See Figure 3)

Symbol	Description	Min	Max	Unit
tCLLCLL	CLK period	125	500	ns
tTCHTCH	TCLK period	2tCLLCLL	—	ns
tTCHTCL	TCLK high	65	—	ns
tTCLTCH	TCLK low	65	—	ns
tTCHRTL	TCLK high to $\overline{RTS}$ low	—	40	ns
tTCHRTH	TCLK high to $\overline{RTS}$ high	—	50*	ns
tCTLTCL	$\overline{CTS}$ set-up to TCLK low	25	—	ns
tCTHTCL	$\overline{CTS}$ set-up to TCLK low	25	—	ns
tTCLTDV	TCLK low to data valid	—	65	ns
tRCHRCH	RCLK period	2tCLLCLL	—	ns
tRDVRCH	RXD set-up to RCLK high	20	—	ns
tRCHRDX	RXD hold after RCLK high	10	—	ns

* In ACR mode with a TCLK frequency of greater than 1/4 of the CLK frequency, the maximum tTCHRTH is 165 ns.

Table 10. Timing Characteristics for ANT Write Cycle (See Figure 4)

Symbol	Description	Min	Max	Unit
tCLLCLL	CLK period	125	500	ns
tCLHCLL	CLK high	44	—	ns
tCLLCLH	CLK low	48	—	ns
tCSLWRL	$\overline{CS}$ set-up to $\overline{WR}$ low	10	—	ns
tWRHCSH	$\overline{CS}$ hold after $\overline{WR}$ high	20	—	ns
tWRLWRH	$\overline{WR}$ pulse width	100*	—	ns
tWRLRYH	$\overline{WR}$ low to RDY high	—	35	ns
tWRHRYZ	$\overline{WR}$ high to RDY high-Z	—	20	ns
tDBVALL	Address set-up to ALE low	28	—	ns
tALLDBX	Address hold after ALE low	0	—	ns
tDBVWRH	Data set-up to $\overline{WR}$ high	30	—	ns
tWRHDBX	Data hold after $\overline{WR}$ high	10	—	ns

* If the ANT is operating asynchronously with the microprocessor, the minimum tWRLWRH is tCLLCLL + 35 ns.

Table 11. Timing Characteristics for ANT Read Cycle (See Figures 5, 6, and 7)

Symbol	Description	Min	Max	Unit
tCLLCLL	CLK period	125	500	ns
tCLHCLL	CLK high	44	—	ns
tCLLCLH	CLK low	48	—	ns
tCSLREL	$\overline{CS}$ set-up to RD low	10	—	ns
tREHCSH	$\overline{CS}$ hold after $\overline{RD}$ high	20	—	ns
tCLHRYH	CLK high to RDY high	—	35	ns
tREHRYZ	$\overline{RD}$ high to RDY high-Z	—	20	ns
tALLDBX	Address hold after ALE low	0	—	ns
tDBZREL	Data bus high-Z to $\overline{RD}$ low	0	—	ns
tRELDBX	$\overline{RD}$ low to data bus driven	—	60	ns
tCLLDBV	CLK low to data valid	—	70*	ns
tREHDBZ	$\overline{RD}$ high to data bus high-Z	—	30	ns
tRELRYV	$\overline{RD}$ low to RDY valid	—	35	ns
tRELDBV	$\overline{RD}$ low to data valid	—	tCLLCLL + 70**	ns
tWRHREL	$\overline{WR}$ high to $\overline{RD}$ low	—	3tCLLCLL†	ns
tREHREL	$\overline{RD}$ high to $\overline{RD}$ low	—	3tCLLCLL††	ns

* Synchronous operation.
** Asynchronous operation.
† This specification refers only to the accesses shown in Figure 6.
†† This specification refers only to the accesses shown in Figure 7.

Table 12. Timing Characteristics for DMA Read Cycles (See Figure 8)

Symbol	Description	Min	Max	Unit
tCLLCLL	CLK period	125	500	ns
tCLHDAH	CLK high to DAV high	—	120*	ns
tRELDAL	$\overline{RD}$ low to DAV low	—	60	ns
tDAHDMH	DAV high to DMAACK high	0	—	ns
tDMHREL	DMAACK high to $\overline{RD}$ low	20	—	ns
tRELREH	$\overline{RD}$ pulse width	tCLLCLL + 70	—	ns
tREHDML	DMAACK hold after $\overline{RD}$ high	10	—	ns
tRELREL	DMA read interval	3tCLLCLL	—	ns
tRELRYH	$\overline{RD}$ low to RDY high	—	35	ns
tRELDBV	$\overline{RD}$ low to data valid	tCLLCLL	2tCLLCLL + 70	ns
tREHRYZ	$\overline{RD}$ high to RDY high-Z	—	20	ns
tREHDBZ	$\overline{RD}$ high to data high-Z	—	30	ns
tRELDBX	$\overline{RD}$ low to data driven	—	60	ns
tCLLDBV	CLK low to data valid	—	70	ns

* Pull-up resistor = 1 kΩ.

Table 13. Timing Characteristics for DMA Write Cycles (See Figure 9)

Symbol	Description	Min	Max	Unit
tCLLCLL	CLK period	125	500	ns
tCLHDRH	CLK high to DRQ high	—	120*	ns
tWRLDRL	$\overline{WR}$ low to DRQ low	—	56	ns
tDRHDMH	DRQ high to DMAACK high	0	—	ns
tDMHWRL	DMAACK high to $\overline{WR}$ low	20	—	ns
tWRLWRH	$\overline{WR}$ pulse width	100**	—	ns
tWRHWRH	DMA write intervals	3tCLLCLL	—	ns
tWRHDML	DMAACK hold after $\overline{WR}$ high	10	—	ns
tWRLRYH	$\overline{WR}$ low to RDY high	—	20	ns
tWRHRYZ	$\overline{WR}$ high to RDY high-Z	—	20	ns
tDBVWRH	Data set-up to $\overline{WR}$ high	30	—	ns
tWRHDBX	Data hold after $\overline{WR}$ high	10	—	ns

* Pull-up resistor = 1 kΩ.
** If RDY is used, DMA controller should be configured for extended write mode.

Table 14. Timing Characteristics for Interrupts

Symbol	Description	Min	Max	Unit
tCLHRFL	CLK high to REOFINT low	—	55	ns
tCLHRFH	CLK high to REOFINT high	—	110*	ns
tCLHRIL	CLK high to RXINT low	—	55	ns
tCLHRIH	CLK high to RXINT high	—	120*	ns
tCLHTIL	CLK high to TXINT low	—	55	ns
tCLHTIH	CLK high to TXINT high	—	120*	ns

* Pull-up resistor = 1 kΩ.

Timing Diagrams

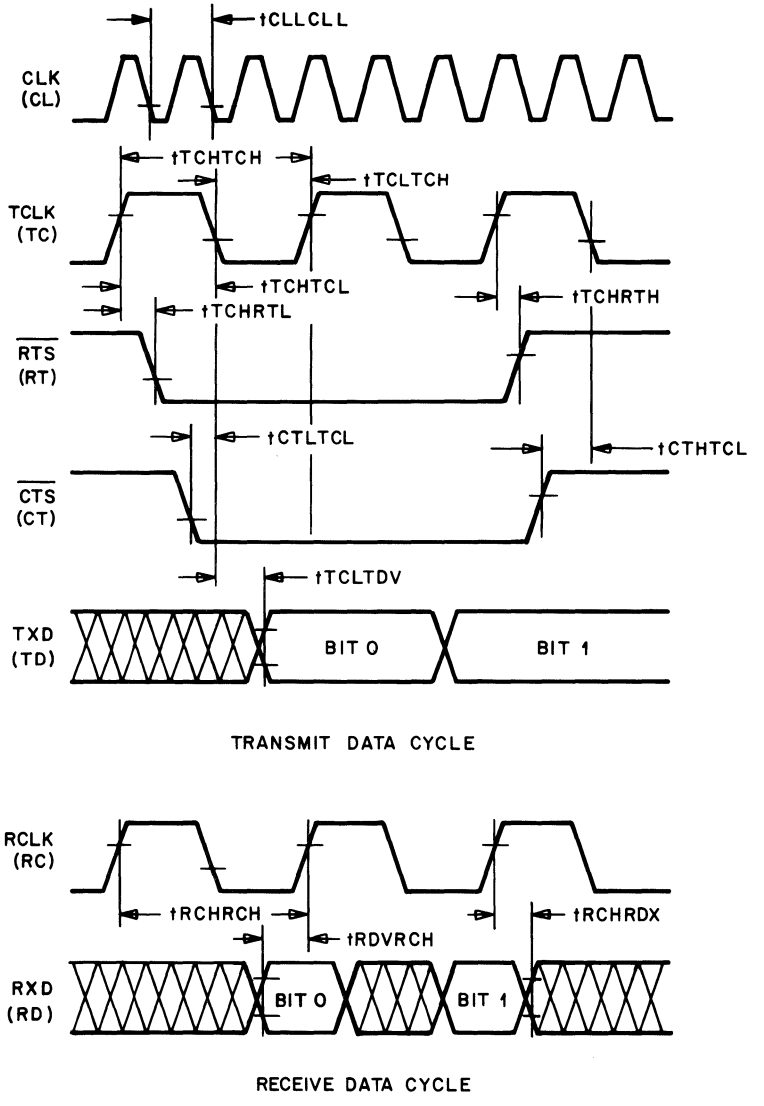


Figure 3. Serial Transmit and Receive Data Cycle

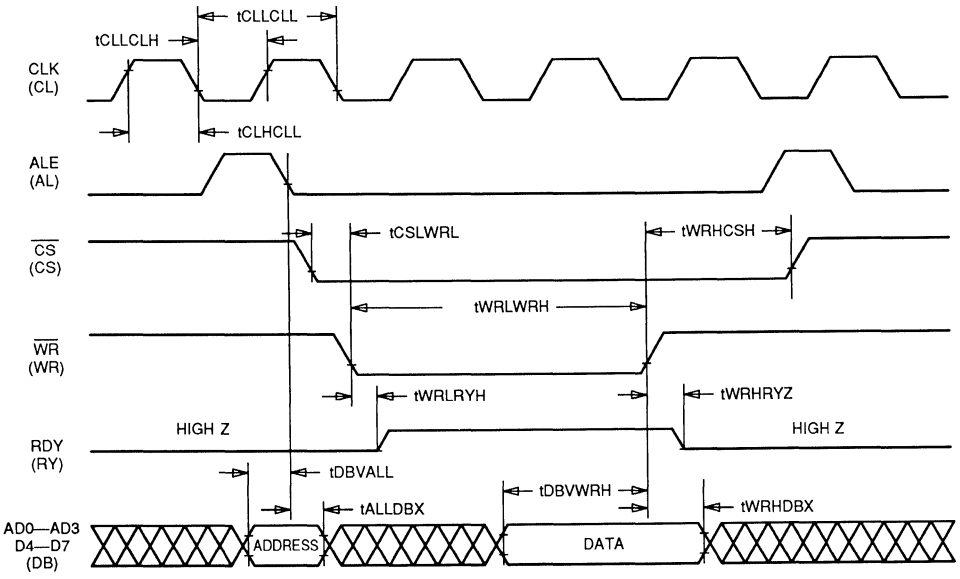


Figure 4. Write Cycle

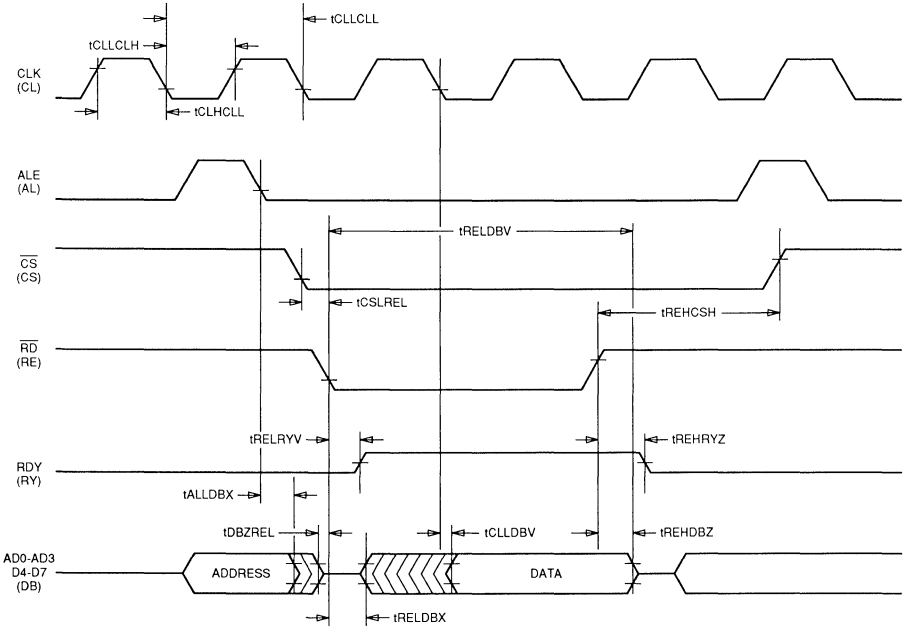
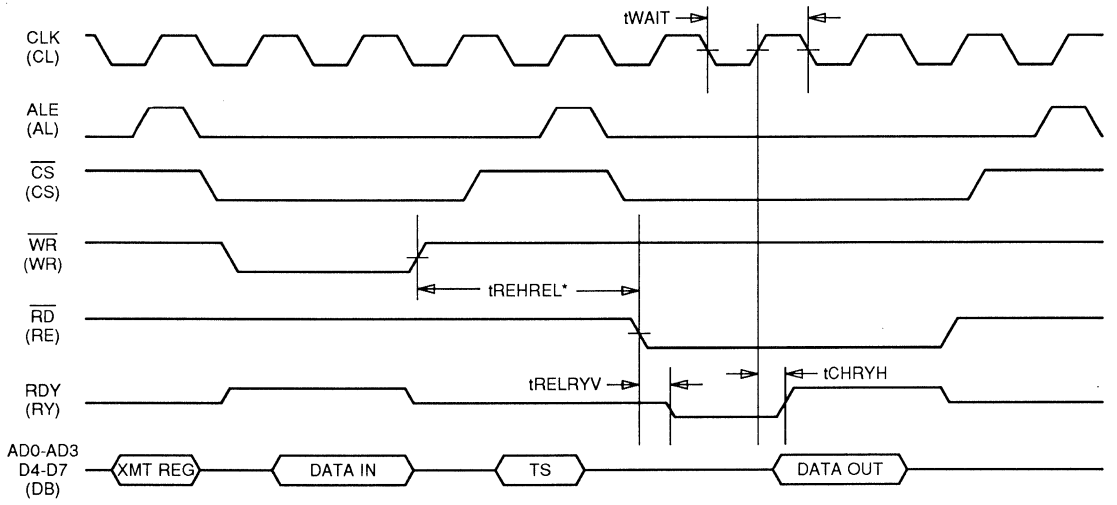
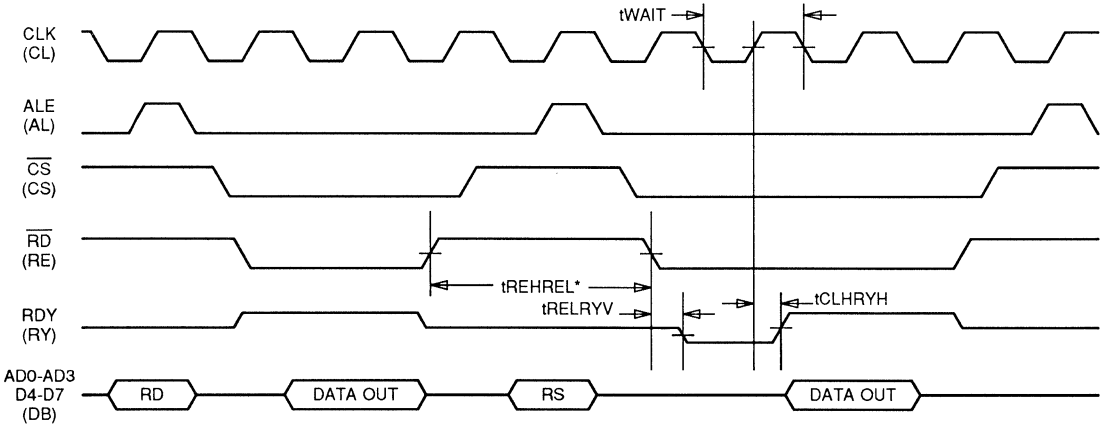


Figure 5. Read Cycle



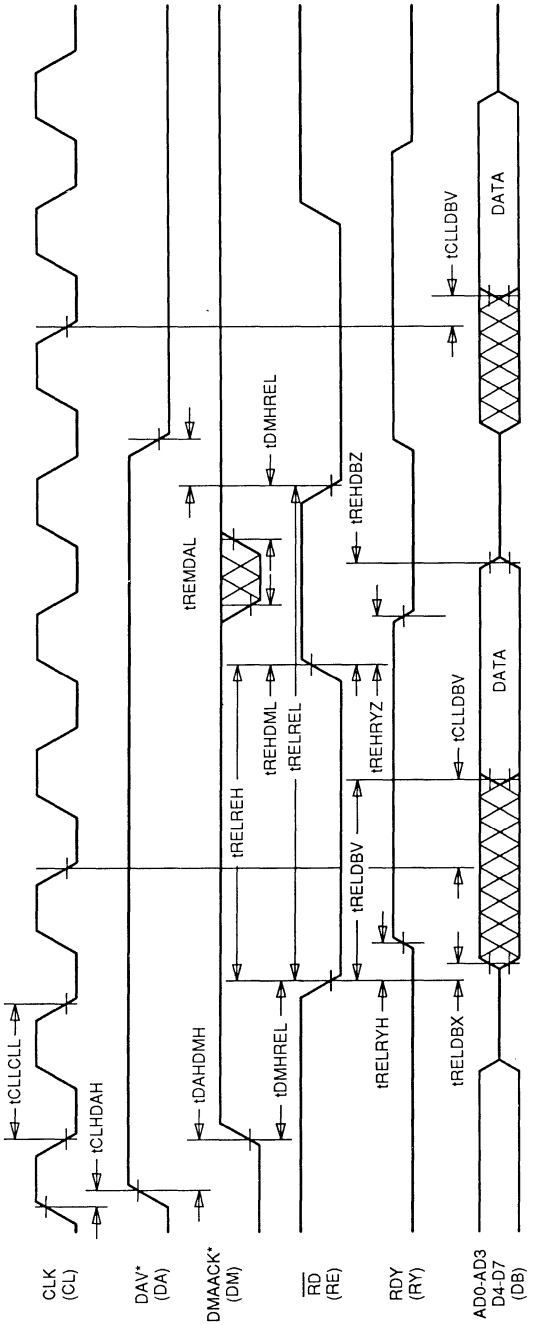
* Three clock cycles are required between these accesses to avoid a wait-state.

Figure 6. Read Cycle with Wait State (TS Read Access Immediately Following Transmit Register Write Access)



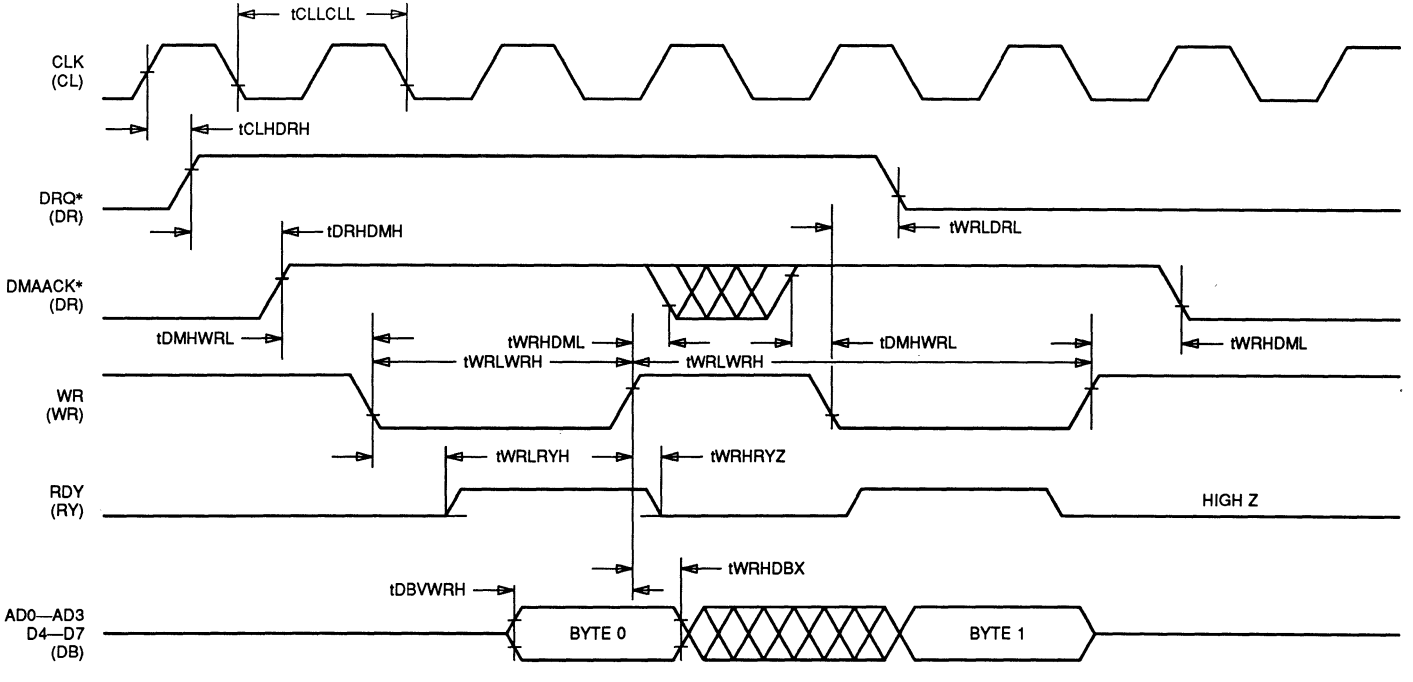
* Three clock cycles are required between these accesses to avoid a wait-state.

Figure 7. Read Cycle with Wait State (RS Read Access Immediately Following RD Read Access)



* DAV and DMAACK shown as active-high.

Figure 8. Consecutive DMA Read Cycles



* DRQ and DMAACK shown as active-high.

Figure 9. Consecutive DMA Write Cycles

T7112 Asynchronous Receiver/Transmitter Interface

Features

- Full-duplex asynchronous transmitter/receiver interface
- Six receive and four transmit data buffers
- Programmable data format
  - 8 data bits
  - 7 data bits plus parity
  - Odd, even, one, zero, no parity
  - 1 or 2 stop bits (transmit)
- Parity, framing, and overrun error detection
- Speed matching (autobaud capability)
- 10-bit start/stop serial data
- DTR/DSR general-purpose I/O pins
- Transmit/receive FIFO status bits indicate FIFO levels
- On-chip baud rate generator
- TTL-compatible with 3-statable outputs
- Flexible polling capabilities
- Interrupt on empty level of transmit FIFO
- Interrupt on fill level of receive FIFO
- Interrupt on receive break detect
- Interrupt on error conditions
- Single 5 V power supply

Description

The T7112 Asynchronous Receiver/Transmitter Interface (ARTI) integrated circuit is an asynchronous, single-channel, full-duplex receiver/transmitter interface for terminals and modems. The ARTI device is compatible with the bus protocol and timing specifications of the 8051 microcontroller and the 8088 and 80188 microprocessors. It can be used in a poll- or interrupt-driven system. The transmitter has four buffers and the receiver has six buffers to reduce the interrupt overhead and the potential for overruns. The speed matching feature of this device allows it to detect and automatically adjust to the received baud rate. The device is implemented in low-power CMOS technology and is available in a 24-pin plastic DIP (T7112-PC) or a 28-pin plastic small outline J-lead SOJ package (T7112-EC).

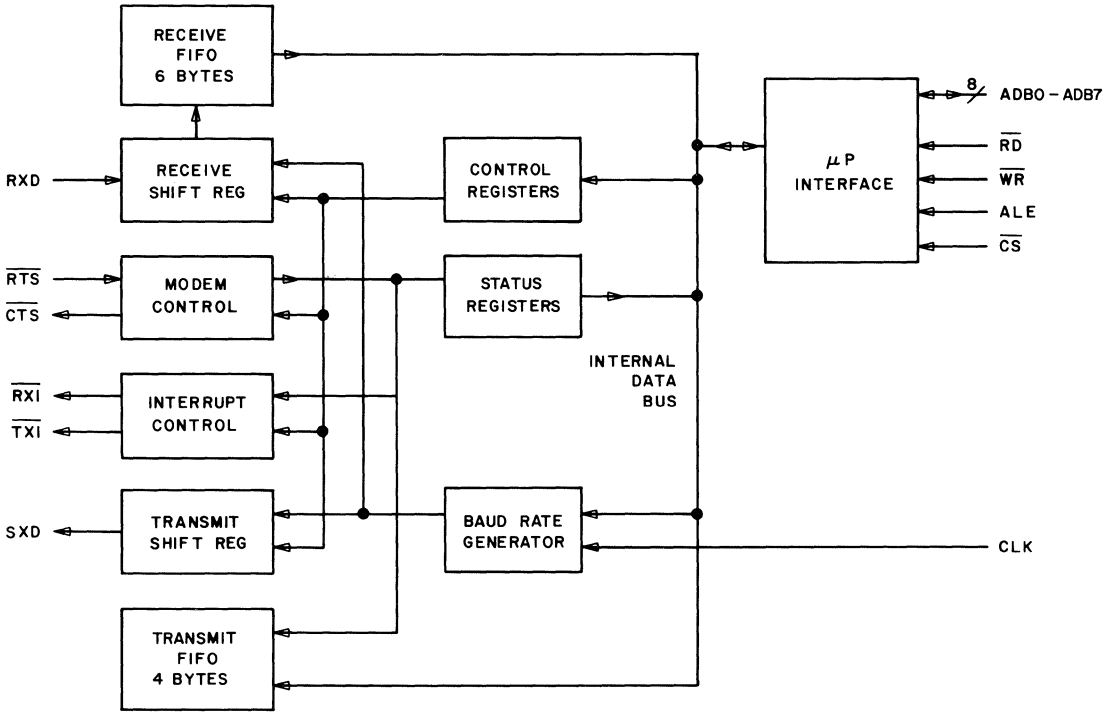
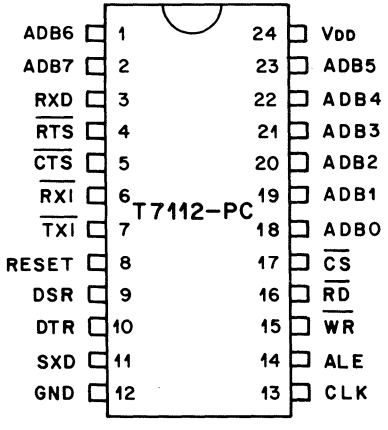


Figure 1. Block Diagram

User Information

Pin Descriptions



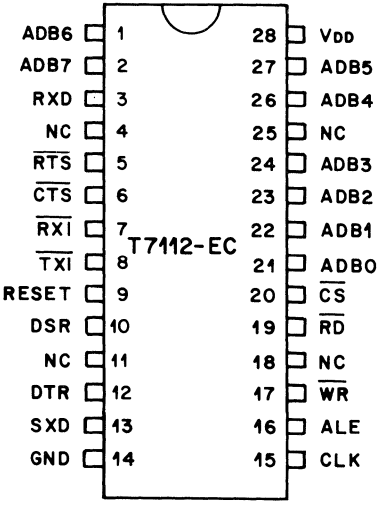


Figure 2. Pin Function Diagrams

Table 1. Pin Descriptions

Symbol	Type	Name/Function
ADB0—ADB7	I/O	**Address/Data Bus Bits 0—7.** These eight bidirectional leads are the microprocessor address/data bus.
RXD	I	**Receive Data.** Serial receive data input.
$\overline{RTS}$	I	**Request-to-Send.** When the ARTI is in the DCE mode and the CTS/RTS control is enabled, this active-low input requests transmission of data to the ARTI. When the ARTI is in the DTE mode, this input enables transmission from the ARTI. When the CTS/RTS control is not enabled, the RTS is an inverting general-purpose input.
$\overline{CTS}$	O	**Clear to Send.** When the ARTI is configured in the DCE mode and CTS/RTS control is enabled, this active-low output indicates that the ARTI is ready to receive data. When enabled in the DTE mode, this output indicates there is transmit data to be sent. When the CTS/RTS control is disabled, the CTS output is a general-purpose inverting output.
$\overline{RXI}$	O	**Receive Interrupt Output.** This output is active-low and remains active for at least one master clock period. It is 3-stated when not on. It must be pulled high with an external resistor to achieve proper logic levels. It can be wire-ANDed with the $\overline{TXI}$ output for a common interrupt to the microprocessor.
$\overline{TXI}$	O	**Transmit Interrupt Output.** This output is active-low and remains active for at least one master clock period. It is 3-stated when not on. It must be pulled high with an external resistor to achieve the proper logic levels. It can be wire-ANDed with the $\overline{RXI}$ output for a common interrupt to the microprocessor.
RESET	I	**Reset.** This active-high input resets the ARTI. All outputs are 3-stated and ADB0—ADB7 are configured as inputs.
DSR	O	**Data Set Ready.** General-purpose noninverting output from the ARTI.
DTR	I	**Data Terminal Ready.** General-purpose noninverting input to the ARTI.
SXD	O	**Serial Transmit Data.**
GND	—	**Ground Reference.**
CLK	I	**Master Clock Input.**
ALE	I	**Address Latch Enable.** In all modes, this signal indicates that a valid address is on the address/data bus.
$\overline{WR}$	I	**Write Input (Active Low).**
$\overline{RD}$	I	**Read Input (Active Low).**
$\overline{CS}$	I	**Chip Select (Active Low).**
V_{DD}	—	**5 V Power Supply.**

Overview

The T7112 ARTI provides a communication link between an 8-bit microprocessor (8088, 80188, or 8051) and a serial asynchronous peripheral. The operation is similar to that of a standard UART except that there are FIFOs at both the transmit and the receive side instead of the usual single register. Programmable interrupt capability is provided.

Registers

Set-up of the ARTI device is done by the processor writing In addition to data, the ARTI© device provides registers to be read that contain error, set-up, and FIFO status.

Table 2. Write/Read Registers*

Write Registers									
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Reg**	**Address (Hex)**
d7	d6	d5	d4	d3	d2	d1	d0	0	00
RXEN	TXEN	PAREN	EV/ODD	PEO/10	P1/0	BRGEN	CTS	1	01
DTE/ DCE	CTS/ RTSHAND	BKGEN	INTEN	TXIEN	RXIEN	STBT	1	2	02
br7	br6	br5	br4	br3	br2	br1	br0	3	03
DSR	RESET	TXRST	RXRST	SPMAT	br10	br9	br8	4	04
TDFB	TDFA	RDFC	RDFB	RDFA	ERRINT	RTSINT	BKINT	5	05
Read Registers									
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Reg**	**Address (Hex)**
d7	d6	d5	d4	d3	d2	d1	d0	0	00
RXCH	RFSC	RFSB	RFSA	TXCH	TFSb	TFSa	1	1	01
BKDET	RTS	$\overline{\text{RXINT}}$	$\overline{\text{TXINT}}$	RXOR	TXUR	FRERR	PARERR	2	02
br7	br6	br5	br4	br3	br2	br1	br0	3	03
DTR	AS	1	1	SPMAT	br10	br9	br8	4	04

* The default condition for all bits is 0, except for the DSR, RDFA, $\overline{\text{RXINT}}$, $\overline{\text{TXINT}}$, TXCH, and TXUR bits.

Write Registers

Unless otherwise noted, all bits of the write registers are cleared (0) by either a hardware reset (RESET input = 1) or a device software reset (RESET bit D6 of register 4 = 1).

Write Register 0. This register contains the transmit data byte from the microprocessor. Bit D7 is ignored if the parity is enabled.

Table 3. Write Register 0 (Address = 00 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
d7	d6	d5	d4	d3	d2	d1	d0	Transmit data byte

Write Register 1. This register contains a control byte.

The receiver is enabled when RXEN is set (1) and disabled when RXEN is cleared. The receiver does not load a byte of data into the FIFO if RXEN is changed to 0 while that byte of data is being received. If RXEN is changed from a 0 to 1 while a valid character is in the receive shift register, that data byte is loaded into the receive FIFO. If another byte of data begins to be received before RXEN = 1, the previous byte is lost. RXEN must be set if DTE/DCE of write register 2 is 0 and CTS/RTSHAND of write register 2 is 1. RXRST does not clear this bit.

Table 4. Write Register 1 (Address = 01 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
RXEN	TXEN	PAREN	EV/ODD	PEO/10	P1/0	BRGEN	CTS	Control

The transmitter is enabled when TXEN is set and disabled when TXEN is cleared. The transmitter finishes sending a character if this bit is cleared while in the process of sending the character. This bit must be set when DTE/DCE and CTS/RTSHAND of write register 2 are set. TXRST does not clear this bit.

The PAREN bit enables parity when set and disables parity when cleared. This bit controls parity generation for transmit data and parity checking for receive data. Also, when this bit is set, the D7 data bit in the transmit FIFO is ignored and replaced by the appropriate parity bit.

When EV/ODD is set, this bit generates even parity for transmit data if PAREN and PEO/10 of this register are set. Received data is also checked for even parity in this mode. When EV/ODD is cleared, odd parity is generated and verified if PAREN and PEO/10 are set.

When PEO/10 is set, this bit generates even or odd parity if PAREN of this register is set. When cleared and PAREN is 1, a 1 or 0 parity bit is generated and verified.

When parity is enabled and PEO/10 of this register is a 0, the parity bit generated and verified is a 1 or 0, according to the state of the P1/0 bit.

The PAREN, EV/ODD, PEO/10, and P1/0 bits that determine the parity settings are summarized in Table 5.

Table 5. Parity Bits

PAREN	EV/ODD	PEO/10	P1/0	Mode
0	X	X	X	No parity
1	X	0	0	Zero parity
1	X	0	1	One parity
1	0	1	X	Odd parity
1	1	1	X	Even parity

The BRGEN bit enables the internal baud rate generator when set and disables the baud rate generator when cleared.

The CTS bit is inverted and appears at the $\overline{CTS}$ output pin if it is in EIA flow control mode or manual mode (CTS/RTSHAND of write register 2 is cleared).

Write Register 2. This register contains a control byte.

When the DTE/DCE bit is set and CTS/RTSHAND of this register is set, the CTS/RTS I/O acts as a DTE interface. The $\overline{RTS}$ input to the ARTI device goes low when the external device can receive data. The $\overline{CTS}$ output from the ARTI device goes low in this mode when there is one or more bytes of data in the transmit FIFO and the TXEN bit is set. When the DTE/DCE bit is cleared and CTS/RTSHAND of this register is set, the CTS/RTS I/O acts as a DCE interface. In this mode, the $\overline{RTS}$ input of the ARTI device goes low when the external device requests to transmit data to the ARTI device. The $\overline{CTS}$ output of the ARTI device goes low in response to the $\overline{RTS}$ input going low when the RXEN bit is set and there is room in the receive FIFO. When CTS/RTSHAND is cleared and DTE/DCE is set, the ARTI is in EIA flow control mode. In this mode, $\overline{CTS}$ is a general-purpose output under the control of register 1 bit D0. The transmitter waits until $\overline{RTS}$ is asserted. The receiver operates the same as in manual mode.

Table 6. Write Register 2 (Address = 02 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
DTE/DCE	CTS/RTSHAND	BKGEN	INTEN	TXIEN	RXIEN	STBT	1	Control

When the CTS/RTSHAND bit is set, the $\overline{RTS}$ input and $\overline{CTS}$ output of the ARTI device cause transmitter and receiver control as previously described. When CTS/RTSHAND and DTE/DCE are cleared, the $\overline{RTS}$ is a general-purpose inverting input and the $\overline{CTS}$ is a general-purpose inverting output from the ARTI device. The transmitter continues to send data until it is disabled or the FIFO is empty and the receiver continues receiving data until it is disabled. Table 7 summarizes the control mode settings.

Table 7. Control Modes

DTE/DCE	CTS/RTSHAND	Mode
0	0	MANUAL
0	1	DCE
1	0	EIA
1	1	DTE

When the BKGEN bit is set, a break is generated from the transmitter if the appropriate transmitter controls have been enabled. If this bit is set in the process of transmitting a character, the break begins after the stop bit of that character has been transmitted. The break is removed when this bit is cleared or a hardware- or software-generated reset occurs. Data can be loaded into the transmit FIFO even if this bit is set. Breaks are sent in multiples of 10 bits. Data can be loaded into the transmit FIFO even if this bit is set.

INTEN, when set, enables the $\overline{TXI}$ and $\overline{RXI}$ interrupt outputs from the ARTI device if they have been previously set. When cleared, all interrupts are disabled.

TXIEN, when set, enables the transmit interrupts. This set-up includes the condition for the transmit queue interrupt status (if set in write register 5) and the $\overline{RTS}$ input interrupt (if set in write register 5).

RXIEN, when set, enables the receive interrupts. This set-up includes the condition for the receive queue interrupt status, break detect, receive parity error, and receive frame error interrupt enables all set in write register 5.

When the STBT bit is set, two stop bits are generated by the transmitter. When cleared, one stop bit is generated. This bit does not affect the definition of framing error on the receiver. The receiver looks for only 1 stop bit.

The D0 bit must be set. A hardware or device software reset sets this bit.

Write Register 3. This register stores the lower eight of eleven bits for the baud rate generator.

Table 8. Write Register 3 (Address = 03 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
br7	br6	br5	br4	br3	br2	br1	br0	Lower byte of baud rate generator

Write Register 4. This register contains reset, control, and baud rate generator bits.

DSR is the noninverted DSR output of the ARTI device. A hardware or device software reset sets this bit.

Table 9. Write Register 4 (Address = 04 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
DSR	RESET	TXRST	RXRST	SPMAT	br10	br9	br8	Reset, control, and baud rate generator

The RESET bit, when set, has the same effect as a high on the RESET input pin of the ARTI device, except that the ARTI outputs are not 3-stated and the microprocessor bus (ADB0—ADB7) operates normally. This bit is self-clearing after the intended software reset has been completed. This bit is cleared when a high level on the RESET input pin is detected. Four master clock cycles are required to complete the internal reset function.

When TXRST is set, it causes a transmitter reset, clearing the transmit queues, status bits, and shift register but not the control bits. This bit is self-clearing, with a wait of at least four master clock cycles needed.

When RXRST is set, it causes a receiver reset, clearing the receiver queues, status bits, and shift register. This bit is self-clearing, with a wait of at least four master clock cycles needed.

SPMAT is set in speed matching mode and cleared by the falling edge of the start-bit pulse. The speed matching interrupt is a latched type. If interrupts are enabled, this bit, although self-clearing after the interrupt occurs, must be written as a 0 to clear the latched speed matching interrupt output.

Bits D2—D0 contain br10, br9, and br8, the upper three (most significant) bits of the internal baud rate generator counter.

Write Register 5. This register contains interrupt bits and queues.

TDFB and TDFA determine the status of the transmit data queue that causes the $\overline{\text{TXI}}$ interrupt output and $\overline{\text{TXINT}}$ status bit from the ARTI device to go low if the interrupts are enabled. Table 11 describes the $\overline{\text{TXI}}$ interrupt corresponding to the TDFA and TDFB bits.

Table 10. Write Register 5 (Address = 05 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
TDFB	TDFA	RDFC	RDFB	RDFA	ERRINT	RTSINT	BKINT	Queues and interrupts

Table 11. $\overline{\text{TXI}}$ Interrupts

TDFB	TDFA	$\overline{\text{TXI}}$ Interrupt
0	0	Interrupt if queue is empty
0	1	Interrupt if three or more bytes can be written
1	0	Interrupt if two or more bytes can be written
1	1	Interrupt if one or more byte(s) can be written

RDFC, RDFB, and RDFA determine when the $\overline{\text{RXI}}$ interrupt output and the $\overline{\text{RXINT}}$ status bit of the ARTI device goes low if the $\overline{\text{RXI}}$ interrupt is enabled. A hardware or device software reset clears bits RDFC and RDFB and sets bit RDFA. Table 12 describes the $\overline{\text{RXI}}$ interrupt corresponding to these bits.

Table 12. $\overline{\text{RXI}}$ Interrupts

RDFC	RDFB	RDFA	$\overline{\text{RXI}}$ Interrupt
0	0	0	Enables the receive interrupt at the end of start bit during speed matching
0	0	1	Interrupt if one or more bytes are available
0	1	0	Interrupt if two or more bytes are available
0	1	1	Interrupt if three or more bytes are available
1	0	0	Interrupt if four or more bytes are available
1	0	1	Interrupt if five or more bytes are available
1	1	0	Interrupt if six bytes are available (full)
1	1	1	Used as a test mode in factory testing

ERRINT enables the error interrupt when set. An error interrupt causes the $\overline{\text{RXI}}$ interrupt output and the $\overline{\text{RXINT}}$ status bit of the ARTI device to go low if there was a parity error, framing error, or the receive queue was in an overrun condition (six bytes were stored to fill the receive queue and another receive byte overwrote the last byte).

RTSINT, when set, causes the $\overline{\text{TXI}}$ interrupt output and the $\overline{\text{TXINT}}$ status bit of the ARTI device to go low when the $\overline{\text{RTS}}$ input to the ARTI device goes low in the DCE mode.

BKINT, when set, causes the $\overline{\text{RXI}}$ interrupt output and the $\overline{\text{RXINT}}$ status bit of the ARTI device to go low when a break is detected by the receiver.

Read Registers

Unless otherwise noted, all bits of the read registers are cleared by either a hardware or device software reset.

Read Register 0. This register contains the receive data byte, the most significant data byte from the receive queue when read by the microprocessor.

Table 13. Read Register 0 (Address = 00 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
d7	d6	d5	d4	d3	d2	d1	d0	Receive data byte

Read Register 1. This register contains the status of the transmit and receive queues.

RXCH, when set, indicates that one or more receive bytes are available.

Table 14. Read Register 1 (Address = 01 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
RXCH	RFSC	RFSB	RFSA	TXCH	TFSb	TFSa	1	Transmit and receive queue status

RFSA, RFSB, and RFSC indicate the number of receive bytes in the receive queue. They indicate to bits RDFC, RDFB, and RDFA of write register 5 (Table 10) how many bytes are available for the interrupt settings.

TXCH, when set, indicates that there is one or more bytes of transmit queue space available. A hardware or a device software reset sets this bit (transmit FIFO is empty after a reset).

TFSa and TFSb indicate the number of available queue bytes that are empty in the transmit buffers. Table 15 summarizes the bit settings of TFSa and TFSb.

Table 15. Available Transmit Queue Bytes

TFSb	TFSa	Number of Empty Bytes
0	0	4
0	1	3
1	0	2
1	1	1

Read Register 2. Read register 2 contains status bits.

BKDET, when set, indicates that the receiver has detected a break condition. (A break condition is reception of ten or more low logic levels in a row.) The RXEN control bit of write register 1 (Table 4) must be set to detect a break condition.

Table 16. Read Register 2 (Address = 02 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
BKDET	RTS	$\overline{\text{RXINT}}$	$\overline{\text{TXINT}}$	RXOR	TXUR	FRERR	PARERR	Status bits

RTS is the inverted $\overline{\text{RTS}}$ input to the ARTI device regardless of the control mode that was set previously.

$\overline{\text{RXINT}}$, when cleared, indicates a receive interrupt condition. RXIEN is 1 regardless of whether INTEN is enabled. This permits increased polling flexibility when external interrupts are not used. A hardware or device software reset sets this bit.

$\overline{\text{TXINT}}$, when cleared, indicates a transmit interrupt condition. TXIEN is set regardless of whether INTEN is enabled. This permits increased polling flexibility when external interrupts are not used. A hardware or device software reset sets this bit.

RXOR, when set, indicates a receiver overrun condition. This condition cannot occur in the DCE mode (Table 7).

TXUR, when set, indicates that the transmitter has sent all the bytes in the transmitter queue and that the transmit shift register is empty. The AS bit in register 4 indicates an empty shift register. A hardware or device software reset sets this bit.

FRERR, when set, indicates that a valid stop bit was not detected.

PARERR, when set, indicates that a parity error has occurred if the parity was previously enabled.

Read Register 3. This read register contains br7—br0, which reflect the lower byte of the baud rate generator stored in write register 3.

Table 17. Read Register 3 (Address = 03 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
br7	br6	br5	br4	br3	br2	br1	br0	Lower byte of baud rate generator

Read Register 4. Read register 4 reflects the most significant bits of the baud rate generator and contains the DTR input.

Table 18. Read Register 4 (Address = 04 Hex)

D7	D6	D5	D4	D3	D2	D1	D0	Function
DTR	AS	1	1	SPMAT	br10	br9	br8	DTR and baud rate generator

DTR reflects the noninverted logic level of the DTR input to the ARTI device.

When AS is set, the data is in either the transmit FIFO or the shift register. When it is a 0, the ARTI device has sent all the data (both the FIFO and the register are empty).

When SPMAT is set, the ARTI device is in speed matching mode. In this mode, the transmitter is disabled and the 16-bit baud rate clock counter is initialized to 32760 base 10 automatically. This bit is self-clearing and is cleared after the start bit is detected.

Bits D2, D1, and D0 contain br10, br9, and br8, which reflect the three most significant bits of the baud rate generator stored in write register 4 (Table 9).

Baud Rate Generator and Master Clock

The internal baud rate generator is an 11-bit binary counter used to send transmit data and sample receive data. It divides the CLK input to the ARTI device by the binary number loaded into write registers 3 and 4 plus one. Its output is actually 16 times the desired baud rate. Figure 3 is a block diagram of the baud rate generator.

The equations for programming the baud rate registers are

$$\text{Baud rate} = \text{CLK}/[(N+1)16]$$

or

$$\text{CLK} = \text{Baud rate}[(N+1)16]$$

where baud rate is desired data rate, CLK is the input clock frequency to the ARTI device, and N is the 11-bit number (except 0) of the baud rate counter.

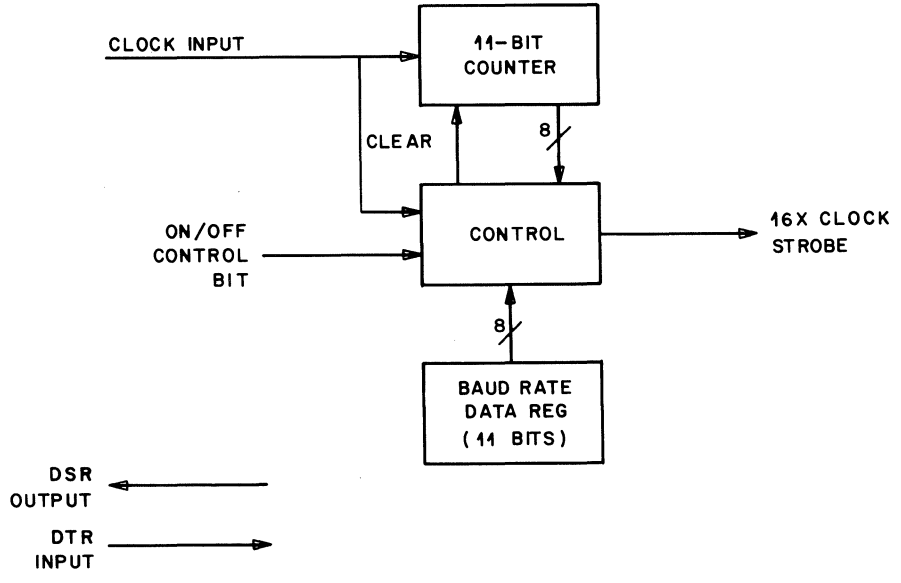


Figure 3. Baud Rate Generator

The extra 1 in the dividend is for clearing and for providing a proper strobe, since the counter is clocked from the master clock into the ARTI device.

The proper method of changing the baud rate frequency is first to disable the baud rate generator, then to write the new time constant to the br0—br10 data bits, and finally to enable the baud rate generator. The baud rate time constant can be changed while enabled. This set-up can be useful when readjusting the baud rate generator frequency in the speed matching mode.

The clock frequency supplied to the ARTI device must be chosen carefully because the baud rate is directly affected by this frequency and the microprocessor timing requirements are based on the relationship between the CLK input and the microprocessor control and data bus signals. When an 8088 microprocessor is used, the ARTI device clock should be the same as the microprocessor clock. When an 8051/8031 (or 8052/8032) microprocessor is used, a clock frequency 75% of the 8051 crystal frequency, or greater, should be used. This set-up ensures proper internal timing for read and write commands.

The maximum input clock frequency to the ARTI device is 8.00 MHz and the duty cycle of the clock must be at least 30%.

Transmitter

A block diagram of the transmitter section of the ARTI device is shown in Figure 4.

The order of data transmission from the ARTI device is the start bit (a logic level 0) first; then d0, d1, d2, d3, d4, d5, d6, d7 (or the parity bit); and the stop bit(s) (a logic level 1) last.

There are four transmit registers that act as a FIFO. Transmit data written to the ARTI device from the microprocessor is steered to the most significant vacant register. As data is transmitted, bytes are shifted until the registers are empty. If parity is enabled, the D7 bit (most significant bit) of data is set or cleared to produce the proper parity before it is loaded into the transmit register.

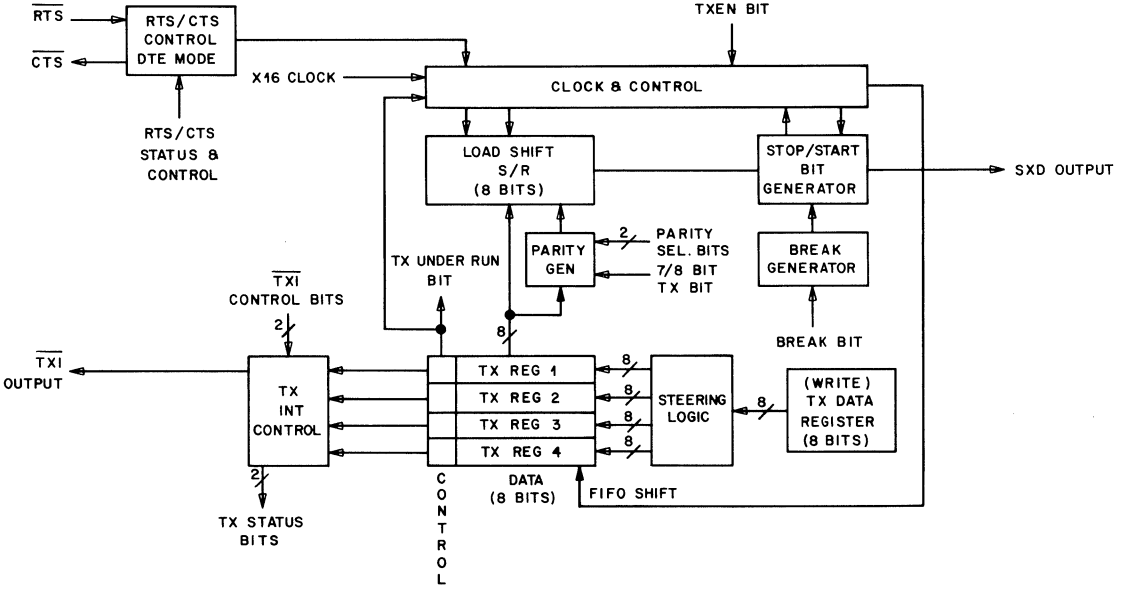


Figure 4. Transmit Circuit

The transmit shift register inserts a logic 0 start bit before the data byte and a logic 1 stop bit after the data byte to complete the 10-bit serial frame. One or two stop bits may be transmitted, depending on the status of the STBT bit in write register 2.

Status bits associated with each register are set when that register is loaded with a data byte. These status bits are used to check transmit status and to control transmit interrupts.

The break generation forces the serial data output to a 0 if the break bit is set in write register 2 and there is no serial transmission in progress. If a character is being transmitted, the break takes place after the stop bits of that character transmission, even if there are more data bytes in the transmit FIFO. The data in the FIFO is stored until the break is removed. Data can be written to the FIFO while in the break mode. BKGEN must last at least 10 bit periods before being cleared by the processor. Longer break outputs are in increments of 10 bit periods. That is, if the break bit was enabled by the microprocessor for 35 bit periods, the break output from the ARTI device would be 40 bit periods.

The clock and control section is used to control the shift register and the data registers. The clock (16 times the baud rate) from the baud rate generator is used as the transmit control frequency. Each bit of data transmission is 16-baud-rate-clock pulses long. When a character has been transmitted, the control circuit checks for additional data to be transmitted. If there is none, the serial output goes high. If there is more data, the least significant byte of the transmit FIFO is loaded into the shift register.

Serial transmission can be enabled by one of two methods. When CTS/RTS transmitter control is disabled, only the TXEN bit must be set to enable data transmission. If the CTS/RTS transmitter control is enabled, as in the DTE mode or EIA flow control mode, the $\overline{RTS}$ input to the ARTI device must be cleared and the TXEN must be set.

In the DTE mode, the ARTI device acts as a DTE interface to an external serial receiver. In the CTS/RTS mode, the $\overline{CTS}$ output of the ARTI device goes low when there is a byte of data to be transmitted. The external device clears the $\overline{RTS}$ input to the ARTI device when it can accept a byte of data. The ARTI device, sensing the low $\overline{RTS}$, then transmits the data if the TXEN bit has been set, or is subsequently set. If the TXEN bit is cleared or the $\overline{RTS}$ input goes high during data transmission, the data transmission is stopped after the byte has been transmitted.

To abort data transmission, the TXRST bit must be set. This set-up forces the SXD output high and clears the transmit registers and status bits. TXEN must be cleared by the microprocessor.

The transmit interrupt control consists of a 4- to 2-bit encoder and a comparator. When the interrupt number is less than or equal to the number of free data byte locations in the transmit registers, the $\overline{TXI}$ output and the $\overline{TXINT}$ status bit of the ARTI device go low if the interrupts are enabled. The two outputs of the encoder can be read directly in read register 1 to indicate the number of free data byte locations.

Receiver

The receiver block diagram is shown in Figure 5.

The order in which the ARTI device receives data is the start bit (logic level 0) first; d0, d1, d2, d3, d4, d5, d6, d7 (or the parity bit) next; and the stop bit(s) (logic level 1) last.

The receiver consists of a shift register and six receive registers.

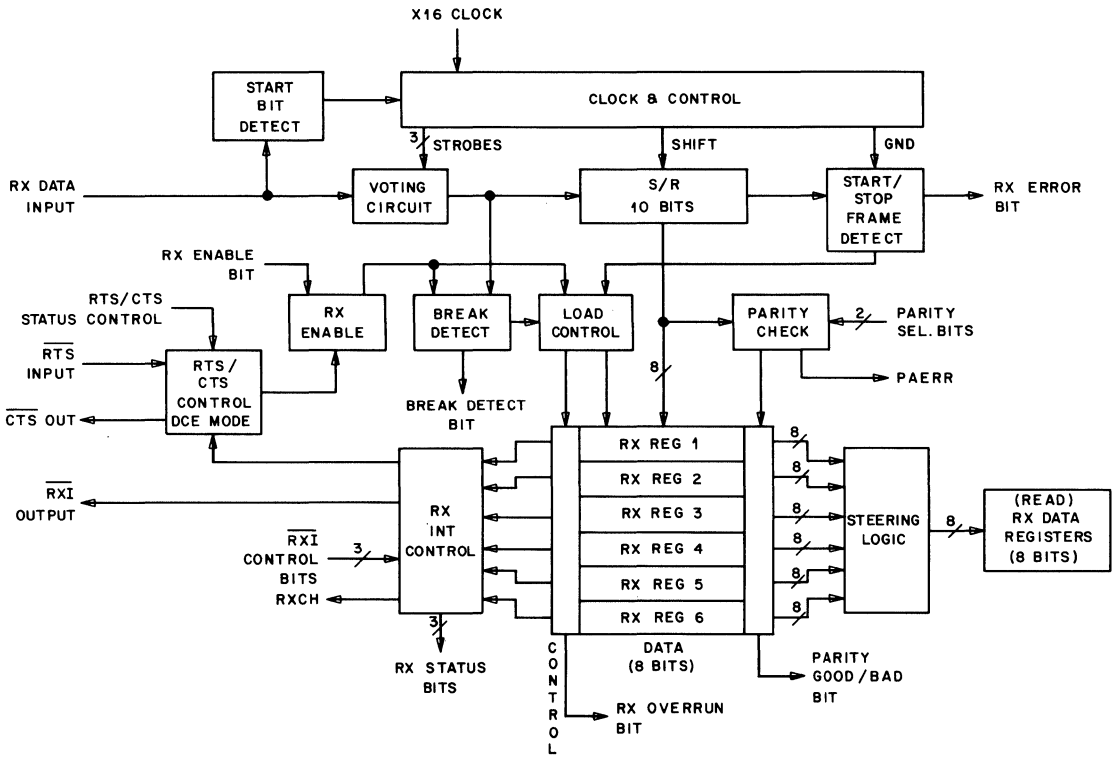


Figure 5. Receive Circuit

The RXD input of the ARTI device goes to a voting circuit, which samples each receive bit in the middle of the bit period. This sampling involves latching the receive data at each of the middle three clock strobes and comparing the three latched logic levels. A majority wins. For example, if two highs and a low are detected, the output of the voting circuit is high. This type of sampling increases the noise immunity of the receiver.

To begin data reception, a start bit detector is used to detect the presence of a low at the input to the receiver. The output from the start bit detector enables the clock and control circuit and the voting circuit.

After the voting circuit, the receive data is loaded into the receive shift register. The clock and control circuit controls the rate at which the serial data is loaded. The shift register is 10 bits long to permit start- and stop-bit verification before the received data byte is loaded into one of the receive registers.

The receive enable circuit determines whether data should be transferred from the receive shift register to the receive FIFO. If in the manual mode, EIA flow control mode, or DTE mode, a byte is properly received and stored in FIFO if RXEN = 1 and a valid start bit is received. In the CTS/RTS handshake DCE mode, data is loaded only if an empty register is available. In all cases, if RXEN = 0, loading is inhibited.

In the CTS/RTS handshake mode, the ARTI device acts as a DCE interface to an external serial transmitter. When the external transmitter wants to transmit a byte of data, it clears the $\overline{RTS}$ input to the ARTI device. The ARTI device clears the $\overline{CTS}$ output when it is able to accept data, RXEN is set, and less then six bytes of data are stored in the receive registers. The external serial transmitter then transmits data to the ARTI device. The receiver is disabled if all six bytes of the receive register are full in this mode.

After a byte is received, the stop bit is checked for a 1. If parity is not enabled and the stop bit is valid, the byte is loaded into the least significant byte of the receive register. If the stop bit is not valid, the error bit associated with that byte is set but the byte is still loaded. If the $\overline{RXI}$ interrupt is enabled for frame error conditions, the $\overline{RXI}$ output and the $\overline{RXINT}$ status bit go low. If read register 2 is read and the erroneous data byte is the most significant in the receive register, the FRERR bit is set. After reading the erroneous data, this bit is reset.

If parity is enabled and the erroneous data byte is the most significant in the receive register, the PARERR bit is set in read register 2. Also, if the $\overline{RXI}$ interrupt is enabled for error conditions, the $\overline{RXI}$ output and the $\overline{RXINT}$ status bit go low to indicate the parity error. The data byte is still loaded into the receive data register.

If an attempt is made to store more than six bytes in the receive registers, the RXOR bit in read register 2 is set. This set-up cannot occur when the ARTI device is in the DCE mode with the RTS/CTS mode enabled because in that mode of operation the receiver is disabled when the receive queue is full. A receive overrun condition causes the $\overline{RXI}$ interrupt output and the $\overline{RXINT}$ status bit to go low for at least one master clock period if the ERRINT interrupt has been enabled.

On a receive overrun condition, the least significant byte (last byte received) in the receive FIFO is written over by the new receive data and the RXOR status bit is set. The most significant bytes of the receive FIFO are not affected by the overrun condition and are not changed until the overrun condition is cleared by reading a byte of data from the FIFO or by a receiver reset.

The break detect circuit senses when a break has occurred. (A break is defined as 10 or more low-level bit periods in a row.) Although during normal data reception a break would cause ten 0s to be loaded into the receive shift register, the break detect circuit inhibits error conditions from being set. Although it does not load the data from the shift register into the data register, it sets the BKDET status bit. Once a break is detected, the only way to reset the BKDET bit is the valid reception of a 1. The break circuitry also prevents the first reception of a 1 after a break from causing the control circuitry to think that a valid stop bit was detected and thus loading a byte of data into the receive register.

Associated with each byte of receive data is a status bit that goes to a 6- to 3-bit encoder. The three RX status bits produced by the encoder indicate how many data bytes are in the receive register and can be read in read register 1 as the RFSC, RFSB, and RFSA status bits.

The RX status bits are also used by the receive interrupt control circuit. When they are equal to or greater than those programmed in write register 5 and the $\overline{RXI}$ interrupt is enabled, the $\overline{RXI}$ output and the $\overline{RXINT}$ status bit of the ARTI device both go low for at least one master clock period.

The RXCH bit in read register 1 is set when one or more bytes of data have been stored in the receive FIFO.

Data bytes can be read at any time via the microprocessor interface to the ARTI device. The data byte that is read is the most significant byte of the receive queue. The steering logic ensures that the proper byte is read even though a byte may be ready to be transferred from the receive shift register to the receive FIFO.

Microprocessor Interface

The microprocessor interface shown in Figure 6 is detailed in the timing section. This interface consists of the read ($\overline{RD}$), write ($\overline{WR}$), chip select ($\overline{CS}$), address latch enable (ALE), and eight address/data bus (ADB0—ADB7) signals. The timing of the ARTI device allows the use of an 8-MHz 8088 microprocessor without wait states if the timing requirements are met. It is recommended that the ARTI device run from the same clock as the 8088 microprocessor to ensure proper read and write access timing.

An 8051 or 8052 microcontroller can be used with the ARTI device if the ARTI clock frequency is less then 75% of the 8051 clock frequency.

Speed Matching

Speed matching, a unique feature of the ARTI device, permits the microprocessor to determine the baud rate of a receive serial input stream (RXD) quickly. It measures the duration of RXD's first low pulse and assumes that it is one start bit. Thus, the algorithm requires d0 (the first data bit received) to be a 1.

To set the ARTI device in speed matching mode, the microprocessor must set write register 4, bit D3 to D1. The 1-to-0 transition on RXD automatically clears the SPMAT bit. It is recommended that TXRST (bit D5) also be set to prevent unexpected data transmission before the baud rate is determined. Optionally, an interrupt can be programmed in write register 5, bits D5—D3.

The result of the measurement can be a combination of three events or, potentially, an error condition. If the RXD low pulse is greater than 72 system clock (CLK) periods and is less than 32775 CLK periods, an estimate of N is loaded into the baud rate generator. This estimate can be read through read registers 3 and 4 just after RXD goes high. Furthermore, this estimate is used to receive the subsequent data bits.

The second event is a programmable latched receiver interrupt ($\overline{RXI}$). The interrupt occurs at the end of the RXD's first low pulse, thereby indicating that the baud rate generator is available for reading and, possibly, for updating the baud registers while the serial input stream is being received. To program the ARTI device to provide this interrupt, clear bits D5—D3 to 000 in write register 5. The speed matching interrupt is a latched type. If interrupts are enabled, this bit, although self-clearing after the interrupt occurs, must be written as a 0 to clear the latched speed matching interrupt output. Using this interrupt to update the baud registers while the serial input stream is being received is recommended for applications in which RXD suffers from more than 3% jitter and correct first-character reception is important. Correcting the measured estimate of N in the baud rate generator can ensure proper reception of later bits. The speed matching interrupt is cleared by writing a zero to bit D3 of register 4.

The third event is a break detection. This event is mutually exclusive of the first two. When in speed matching mode, a break is detected if the first RXD low pulse exceeds 32776 system clock periods in duration. The break is signaled according to the ARTI device's current break handling configuration. No estimate of the N is loaded into the baud rate generator in this case and the end of RXD = low is not signaled by the interrupt pulse described above.

An error condition can result if the first low pulse of RXD is less than 72 system clock periods in duration. The ARTI device loads the baud rate generator, but with a useless value (N = all 1s or $N \leq 4$). The interrupt occurs if programmed. The rest of the data word is not received correctly. Unusually short RXD pulses can load the baud rate generator with 0, thereby disabling the transmitter and receiver.

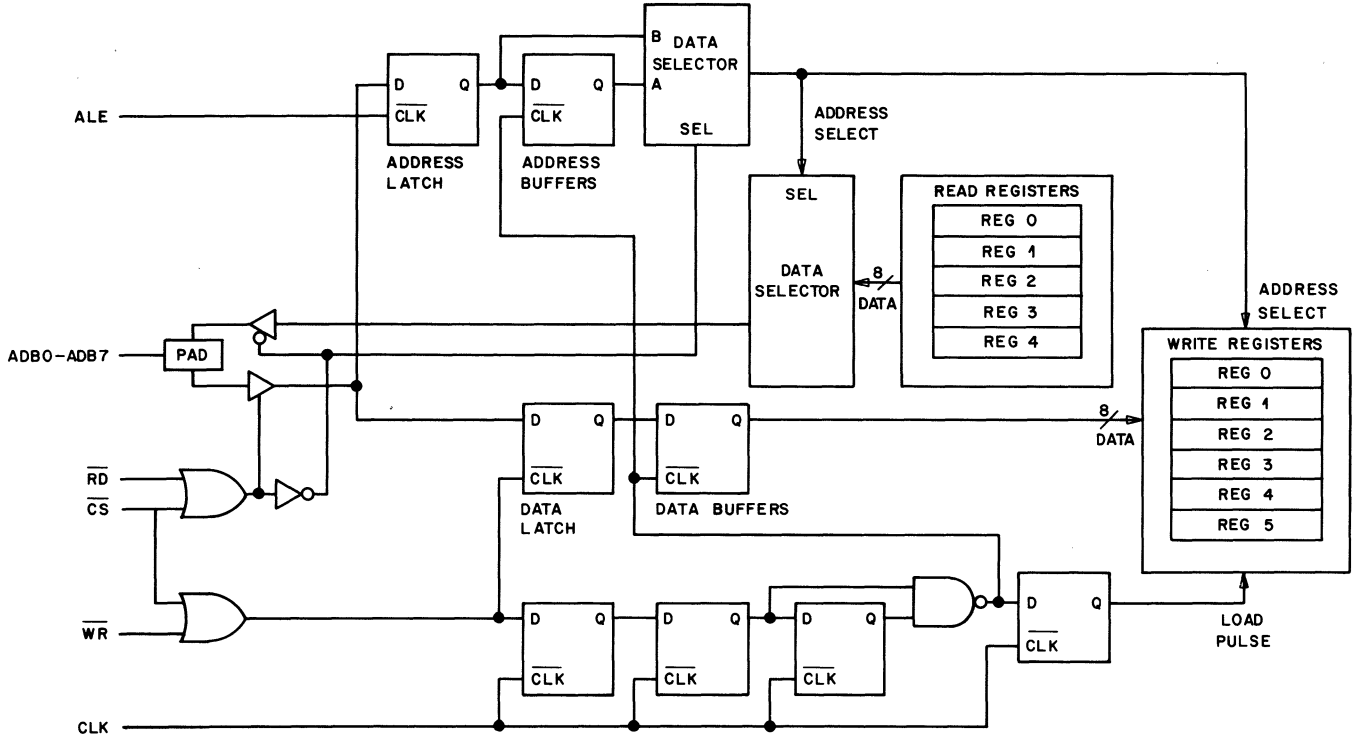


Figure 6. Microprocessor Interface

Testing

All outputs of the ARTI device are 3-stated when the RESET input is at a logic high. The address/data bus signals are configured as inputs in this condition. This test mode is used during GenRad in-circuit PWB testing to prevent damage to the ARTI output buffers while they are being back-driven.

The RESET input to the ARTI clears the receive and transmit registers and the status bits, and sets the control bits to their default conditions. The RESET function is typically used during circuit power-up. In addition, certain test modes should not be active during normal operation:

Test A: Bit 0 of write register 2 = 1
Test B: Bit 3 of write register 4 = 1

Characteristics

Electrical Characteristics

T_C = 0 to 70 °C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Condition
Input voltage:					
low	V_{IL}	0.0	0.8	V	—
high	V_{IH}	2.0	V_{DD}	V	—
Output voltage:					
low	V_{OL}	—	0.4	V	I_{OL} = 2.4 mA
high	V_{OH}	2.4	—	V	I_{OH} = −0.4 mA
Input load current	I_{LC}	0.0	−10	μA	—
3-state output leakage current	I_O	−40.0	40	μA	—
Input capacitance	C_I	—	20	pF	—
Bus capacitance	Ctotal	—	125	pF	—
Rise time	tr	—	20	ns	—
Fall time	tf	—	20	ns	—
Power dissipation	PD	—	150	mW	—

Maximum Ratings

Storage temperature (Tstg) range ..... −55 to +125 °C
Operating temperature (T_C) range ..... 0 to 70 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Table 19. ARTI and 8088 (80188) Microprocessor Interface Timing (See Figure 7)

Symbol	Description	Min*	Max*	Unit
tCLCL	CLK cycle period	125	500	ns
tCHCL	CLK low time	68	—	ns
tCLCH	CLK high time	44	—	ns
tCSL	Chip select delay	—	100	ns
tCLLH	ALE active delay	—	50 (35)	ns
tCHLL	ALE inactive delay	—	55 (35)	ns
tLHLL	ALE width	58 (90)	—	ns
tCLAV	Address valid delay	10 (5)	60 (55)	ns
tAVAL	Address valid to ALE low	28 (30)	—	ns
tLLAX	Address hold to ALE inactive	34 (30)	—	ns
tCLAX	Address hold time	10	—	ns
tDVCL	Data in set-up time	20	—	ns
tCLRL	$\overline{RD}$ active delay	10	100 (70)	ns
tAZRL	Address float to read active	0	—	ns
tCVCTV	Control active delay 1	10	70	ns
tCLDX	Data in hold time	10	—	ns
tWHDX	Data hold after $\overline{WR}$	38 (85)	—	ns
tCLRH	$\overline{RD}$ inactive delay	10	80 (55)	ns
tCVCTX	Control inactive delay	10 (5)	70 (55)	ns
tWLWH	$\overline{WR}$ width	210	—	ns
tRLRH	$\overline{RD}$ width	200	—	ns
tRHAV	$\overline{RD}$ inactive to next address	—	85	ns

* Numbers in parenthesis are for 80188 microprocessor only.

Table 20. ARTI and 8051 Microcontroller Interface Timing (See Figures 8 and 9)

Symbol	Description	Min	Max	Unit
tLLRL	ALE low to $\overline{RD}$ low	137.5	217.5	ns
tLLWL	ALE low to $\overline{WR}$ low	137.5	217.5	ns
tRLRH	$\overline{RD}$ pulse width	375	—	ns
tRHLH	$\overline{RD}$ high to ALE high	22.5	102.5	ns
tWHLH	$\overline{WR}$ high to ALE high	22.5	102.5	ns
tCSL	Chip select delay	—	100	ns
tAVLL	Address valid to ALE low	7.5	—	ns
tLLAX	Address hold after ALE low	27.5	—	ns
tRLAZ	RD low to address float	—	10	ns
tRLDV	RD low to valid data in	—	147.5	ns
tRHDX	Data hold after $\overline{RD}$	0	—	ns
tRHDZ	Data float after $\overline{RD}$	—	55	ns
tDVWL	Data valid to $\overline{WR}$ transition	2.5	—	ns
tWLWH	$\overline{WR}$ pulse width	275	—	ns
tWHQX	Data hold after $\overline{WR}$	12.5	—	ns

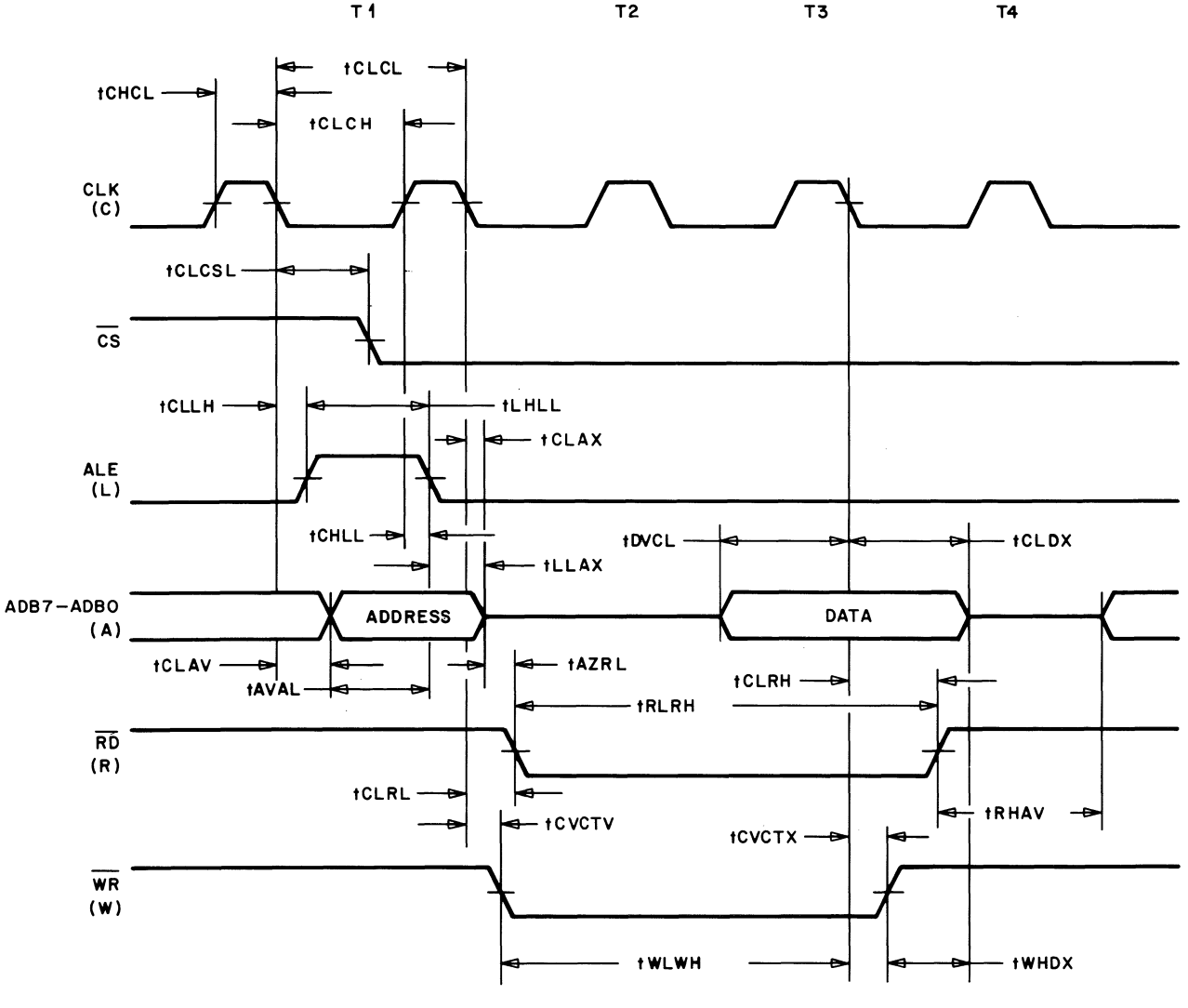


Figure 7. ARTI/8088 (80188) Microprocessor Interface Timing

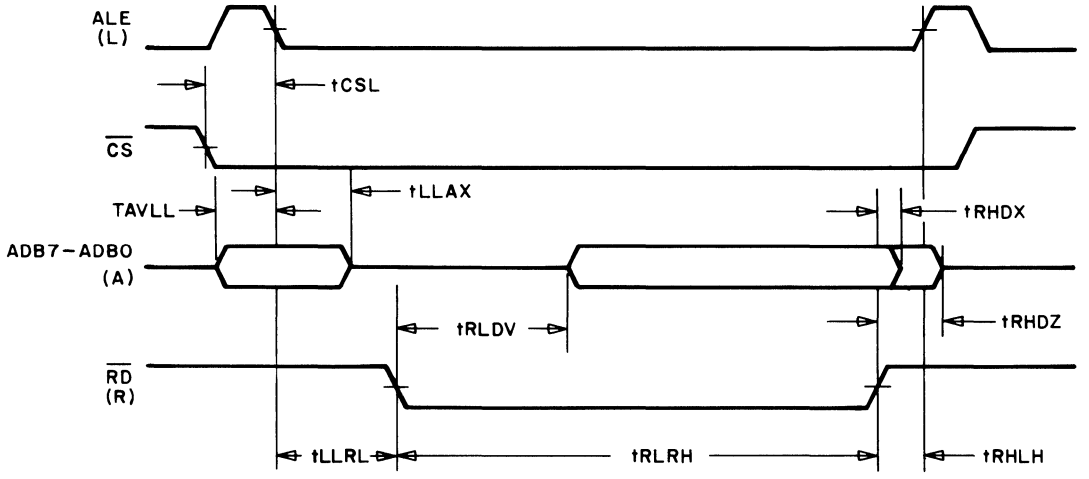


Figure 8. Read Cycle

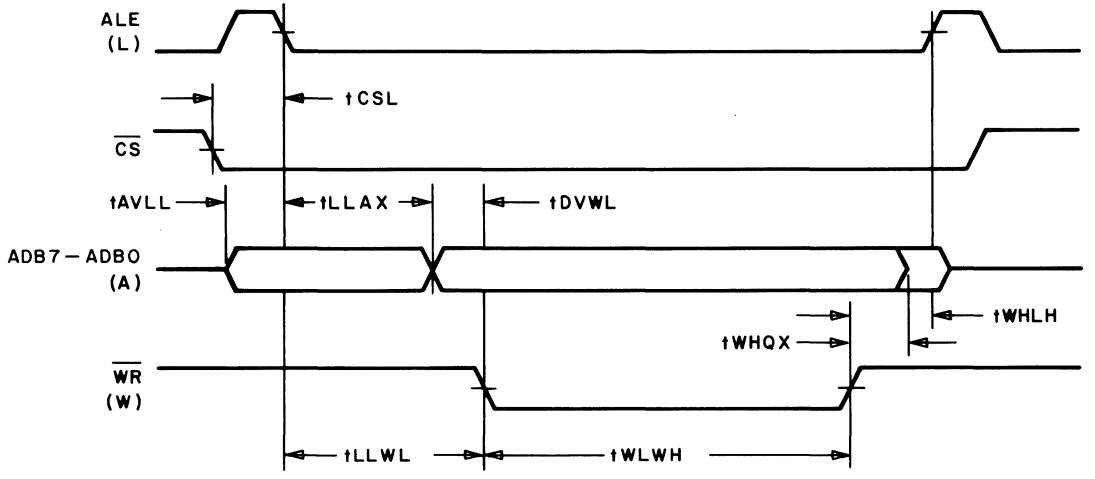


Figure 9. Write Cycle

T7115 Synchronous Protocol Data Formatter

Features

Serial Interface

- 32-channel (full-duplex) multiplexed serial input/output supports the T1/DS1 24 channel and the CEPT 32 channel modes
- Automatic flag transmission and detection
- Flag stuffing up to 2047 flags
- Flag adjustment for the synchronous rate adaption
- Full, partial, or no CRC generation and checking
- Zero-bit insertion and deletion
- Abort/idle detection and transmission
- Short and long frame detection
- 2-mb/s continuous serial data rate
- Dynamic channel allocation (or channel concatenation) supports DS0, H0, H11, and H12 channels
- Bit rate control on each channel
- Channel inversion
- Transparent mode (no protocol) supports ECMA 102 and CCIT I.463 RA2 rate adaption standards
- Loopback mode
- DMA CRC for relay mode

Host Interface

- Compatible with 16-bit or 32-bit microprocessor systems
- On-chip 64-channel DMA memory address generator and buffer manager
- Interrupt queue (up to 4096 interrupts)
- Nonmultiplexed 16-bit data and 24-bit address (16 Mbytes) buses
- Transmit and receive buffers accessible through memory-mapped look-up tables

Description

The T7115 Synchronous Protocol Data Formatter (SPYDER-T) integrated circuit is a synchronous packet data communications controller device. All inputs and outputs of the T7115 SPYDER-T are TTL-compatible. The device is fabricated using CMOS technology, requires a single 5 V supply, and is available in a 68-pin plastic chip carrier.

The SPYDER-T reads data from a shared memory, performs the low-level formatting functions, and transmits to a serial data bus in a time-division-multiplexed manner that supports up to 32 channels. Similarly, the SPYDER-T receives serial data bus performs the deformatting functions, and stores the raw data in the shared memory on a channel-by-channel basis.

The device transmits and receives the serial data at the primary rate of 2.048 Mbps for the CEPT 32-channel European mode and 1.544 Mbps for the T1/DS1 24-channel North American mode. Two or more time slots can be concatenated to create super channels. These time slots do not have to be adjacent.

The SPYDER-T also provides nonprotocol and transparent DMA functions on selected channels. The on-chip DMA controller allows the direct transfer of packet data (up to 8191 bytes) between the shared memory and the SPYDER-T for up to 32 full-duplex channels without host processor intervention. The SPYDER-T and the host processor exchange all commands and messages through the shared memory.

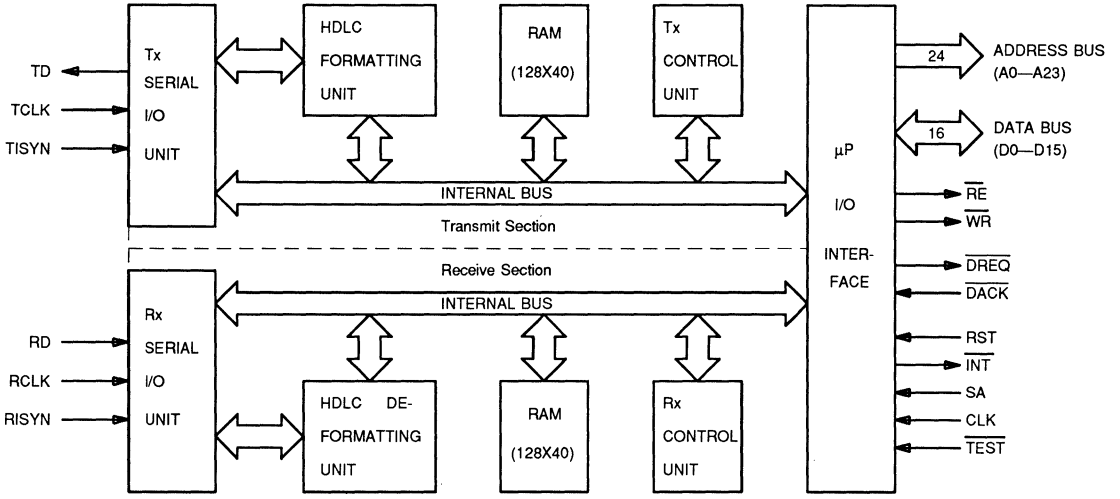


Figure 1. SPYDER-T Block Diagram

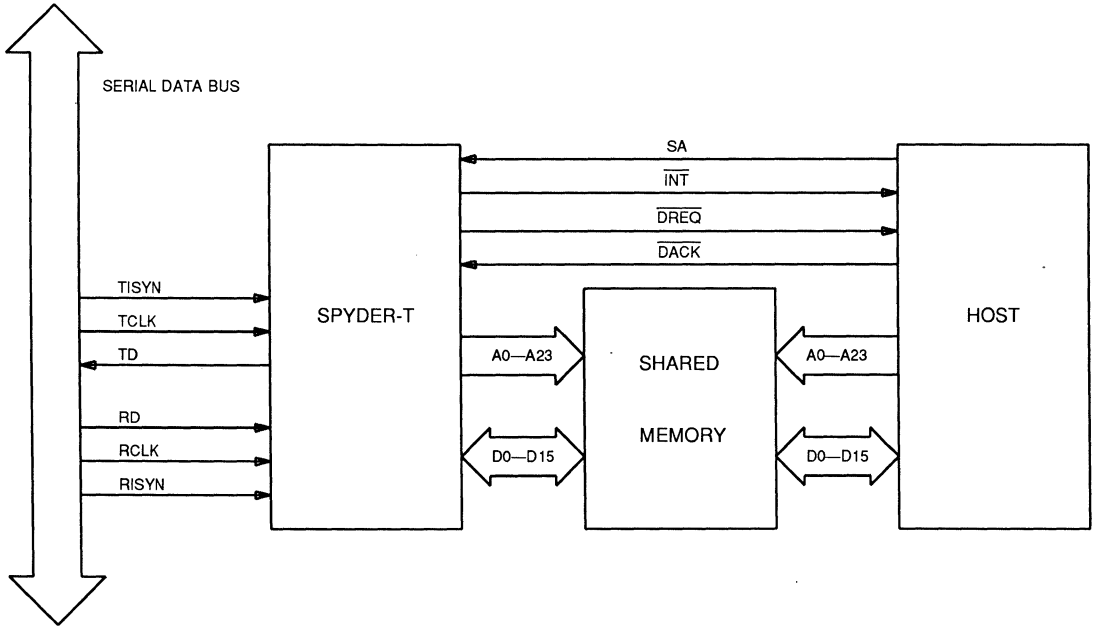


Figure 2. Typical SPYDER-T Application

4. ISDN Basic Rate

T7250A User Network Interface for Terminal Equipment

Features

- Supports CCITT Recommendation I.430 for ISDN Basic Access (2B+D) at the S/T reference point in terminal equipment
- Built-in deeply buffered HDLC formatter for D channel
- Interchangeable B channels
- Optional B-channel inversion
- Power-up reset
- Programmable 0.127 second – 2.032 second multifunction timer
- Local and remote loopback test modes
- All outputs are 3-statable
- Parallel microprocessor interface with separate address and data leads, programmable interrupt polarity, and maskable interrupts
- Programmable clock and synchronization signals allow for interfacing with codecs, HDLC controllers, and rate adapters
- Transmitter and receiver each interface to a 2.5:1 transformer
- TTL/CMOS-compatible I/O
- Crystal or clock input acceptable – no external circuitry required for crystal

Description

The T7250A User Network Interface for Terminal Equipment (UNITE) provides the line interface in terminal equipment used for basic access service offered by the Integrated Services Digital Network (ISDN). The device conforms to the CCITT Recommendation I.430 for point-to-multipoint configurations. Priority, contention resolution, multiframing, and activation/deactivation processes are fully supported. Recommendation I.430 impedance and voltage requirements can be met with a simple line interface circuit. An HDLC formatter and a sophisticated queue manager are provided to simplify the D-channel interface.

The T7250A device is manufactured using CMOS technology and is available in either a 40-pin plastic DIP or 44-pin plastic leaded chip carrier. The 44-pin chip carrier provides two features that the 40-pin DIP package does not: a 16-kHz or an 8-kHz clock and a 6.144-MHz or 192-kHz system clock. The T7250A device uses a 5 V supply and has a nominal power consumption of 55 mW.

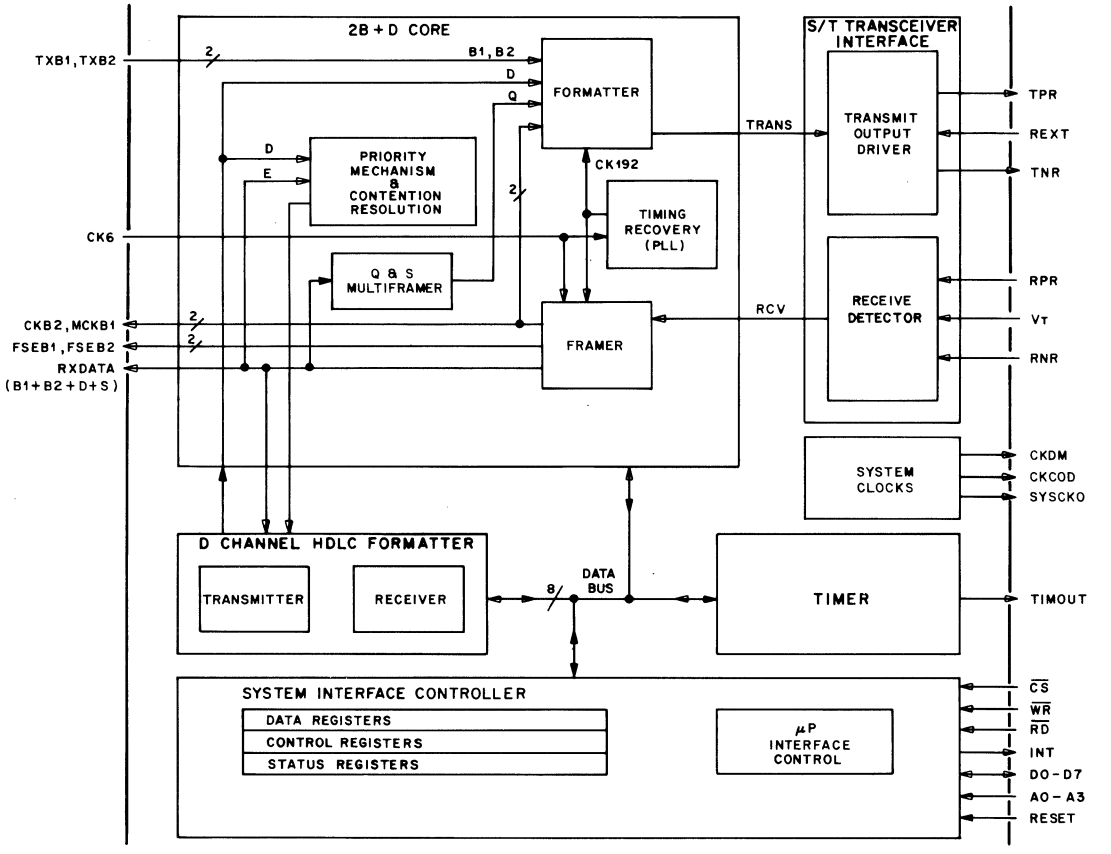


Figure 1. Block Diagram

T7252A User Network Interface Termination for Switches

Features

- 4-wire 192-kb/s line interface for point-to-point and point-to-multipoint (passive bus) arrangements at the ISDN S/T reference point
- CCITT Recommendation I.430 basic access B1, B2, and D (2B+D) channels separated from and combined into 192-kb/s stream
- Two transmit/receive serial highways with assignable time slots for voice or data transfer
- Programmable offset and edge-selection bits for organization of serial highways
- Compatible with AMD and Intel dual PCM highways for configurations requiring 32 or 64 time slots
- Selectable speeds on serial highways: 256 kHz (4 time slots) to 4.096 MHz (64 time slots)
- Fully adaptive timing for the analog receiver in all link configurations, with automatic level switching between two sampling thresholds
- Parallel microprocessor interface with either multiplexed or demultiplexed address/data lines and maskable interrupts
- All digital input/outputs are TTL-compatible (except the two crystal inputs)
- Memory-mapped registers to control time-slot assignment, activation/deactivation, 14 local/remote loopback modes, and interrupts
- Capability of direct microprocessor control of the B1, B2, or D channel through the microprocessor interface
- On-chip digital divider for 192-kHz clock derivation from a user-supplied 6.144-MHz clock, crystal, or CMOS oscillator
- Supports multiframing for S- and Q-channel operation
- Power-down mode of operation with less than 25-mW power dissipation
- High-impedance outputs for board-level testing

Description

The T7252A User Network Interface Termination for Switches (UNITS) is a silicon integrated circuit that provides the user with level 1 network termination (NT) functions in the Integrated Services Digital Network (ISDN). The UNITS device provides full-duplex 2B+D communication at 192 kb/s over a 4-wire digital subscriber loop. Channels B1 and B2 are 64-kb/s voice or data channels, and the D channel is a 16-kb/s control or data channel. All point-to-point and point-to-multipoint (passive bus) configurations are supported as defined in the 1986 version of CCITT Recommendation I.430 and the November, 1986, Draft US Specification for the Basic Rate Interface Physical Layer. The T7252A UNITS communicates with a switching network over a user-configured time-division multiplexed (TDM) highway called the concentration highway. A generic microprocessor interface is also provided.

The T7252A UNITS is manufactured using low-power 1.25-micron CMOS technology and is available in either a 44-pin plastic leaded chip carrier or a 40-pin plastic DIP. The T7252A UNITS uses a 5 V power supply and has a maximum power consumption of less than 100 mW.

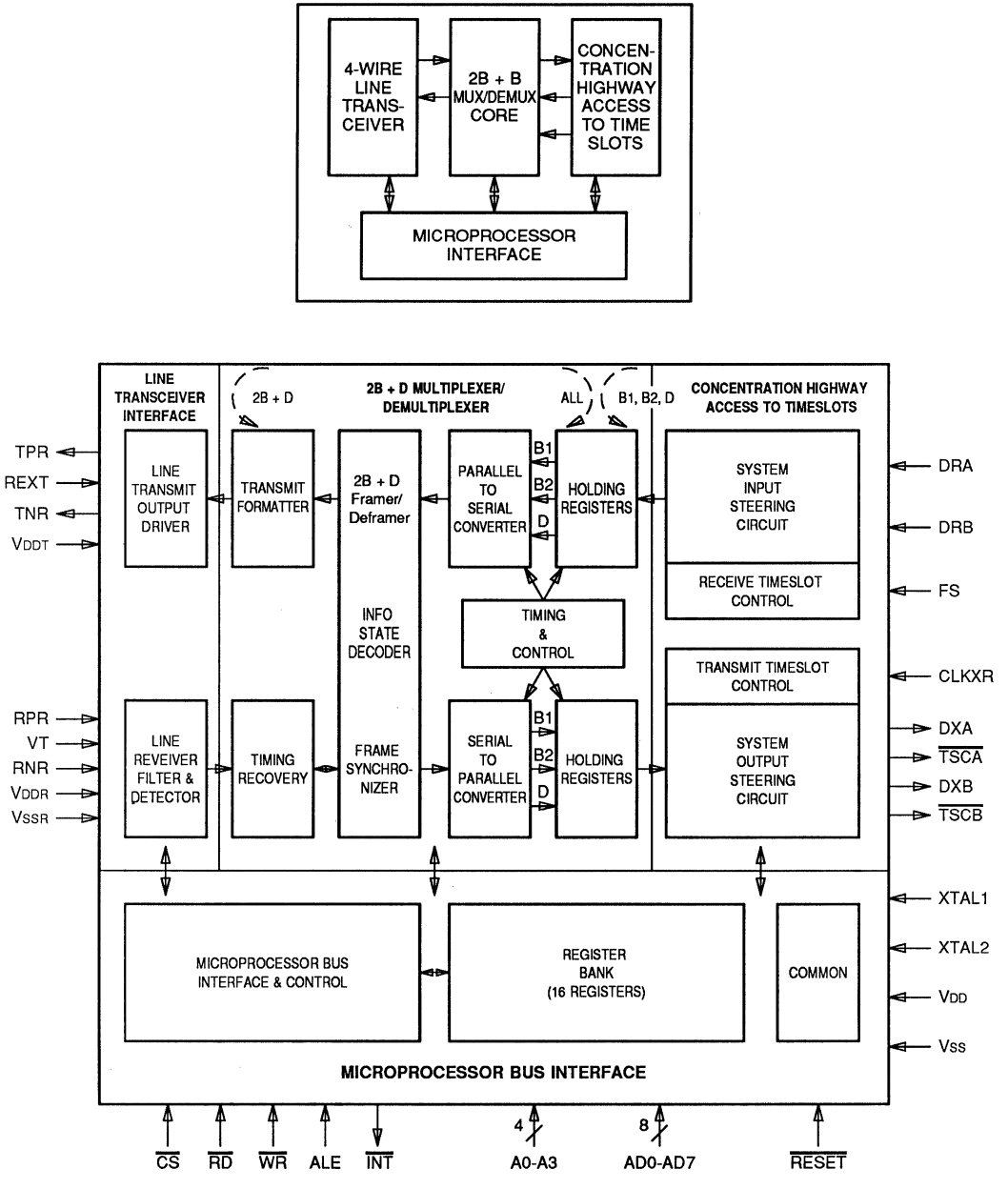
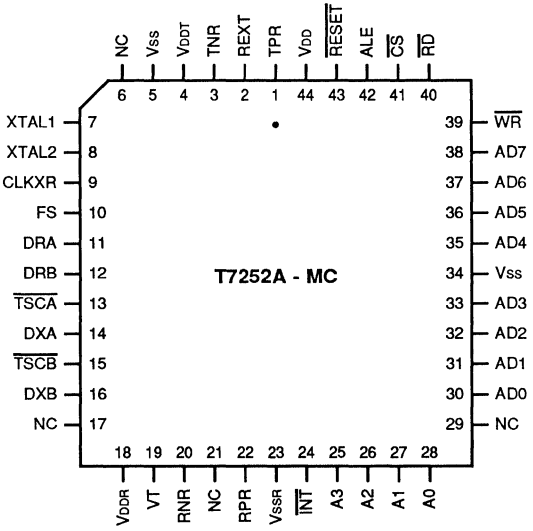


Figure 1. Block Diagrams

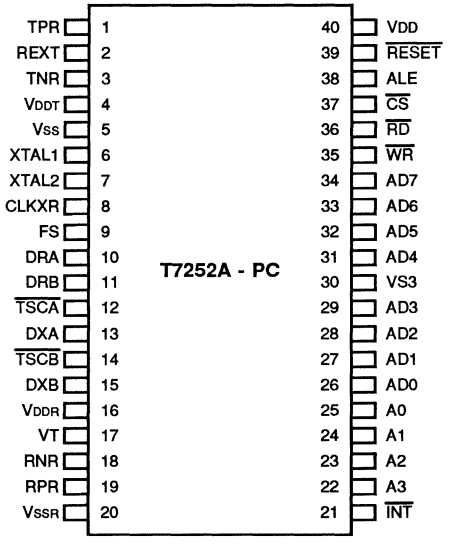
User Information

Pin Description



Symbol	Pin	Symbol	Pin
NC	6,17	RNR	20
	21,29	RPR	22
A0—A3	28—25	TNR	3
AD0—AD7	30—38	TPR	1
ALE	42	TSCA	13
CLKXR	9	TSCB	15
CS	41	VDD	44
DRA	11	VDDR	18
DRB	12	VDDT	4
DXA	14	VSS	5
DXB	16	VSS	34
FS	10	VSSR	23
INT	24	VT	19
RD	40	WR	39
RESET	43	XTAL1	7
REXT	2	XTAL2	8

Figure 2. Pin Function Diagram and Alphabetical Listing of Pin Symbols for PLCC



Symbol	Pin	Symbol	Pin
A0—A3	25—22	RPR	19
AD0—AD7	26—34	TNR	3
ALE	38	TPR	1
CLKXR	8	TSCA	12
CS	37	TSCB	14
DRA	10	VDD	40
DRB	11	VDDR	16
DXA	13	VDDT	4
DXB	15	VSS	5
FS	9	VSS	30
INT	21	VSSR	20
RD	36	VT	17
RESET	39	WR	35
REXT	2	XTAL1	6
RNR	18	XTAL2	7

Figure 3. Pin Function Diagram and Alphabetical Listing of Pin Symbols for 40-pin DIP

Table 1. Pin Descriptions

PLCC	DIP	Symbol	Type	Name/Function
1	1	TPR	O	**Transmit Positive Rail.** Positive output of analog transmitter, which uses alternate space inversion (ASI) coding.
2	2	REXT	I	**External Resistor.** This 2 kΩ ± 1% resistor fixes the transformer turns ratio for the transmitter to 2.5:1.* This ratio offers the optimum balance between power consumption, capacitance on the line, and ability to clamp line voltage surges. The other side of the resistor should be connected to V_{DDT}.
3	3	TNR	O	**Transmit Negative Rail.** Negative output of analog transmitter.
4	4	V_{DDT}	—	**Line Transmitter 5 V Supply.** Analog power supply for the subscriber line transmitter.
5	5	V_{SS}	—	**Digital Ground.**
6	—	NC	—	**No Connection.**
7	6	XTAL1	I	**Primary Crystal Input.** XTAL1 accepts a 6.144-MHz clock, oscillator, or crystal input. If this master frequency is supplied from a crystal, the XTAL2 input must also be used. The overall stability of the 6.144-MHz signal, as seen at the XTAL1/2 input(s), must be ± 250 ppm. Since this two-pin crystal oscillator circuit is designed for CMOS levels, a pull-up resistor is recommended if XTAL1 is driven from a TTL-compatible output. The 6.144-MHz input can be asynchronous with respect to the CLKXR and FS inputs.
8	7	XTAL2	I	**Secondary Crystal Input.** If the 6.144-MHz master frequency is supplied from a crystal, the XTAL2 pin must be used for the second crystal input. If a 6.144-MHz clock or oscillator is provided on XTAL1, XTAL2 should be left unconnected (floating).
9	8	CLKXR	I	**Transmit/Receive Highway Clock.** This clock controls the rate at which information is sent or received on both the transmit and receive highway bit streams. For n time slots in a TDM frame, CLKXR = n X 64 kHz, where n normally equals 4, 8, 16, 32, or 64. **Note:** It is recommended that CLKXR be pulled up by an external resistor to ensure a quick low-to-high transition to more than 4 V.

* The two transmitter outputs, TNR and TPR, connect to the secondary (or 2.5) side of the transformer.

Table 1. Pin Descriptions (Continued)

PLCC	DIP	Symbol	Type	Name/Function
10	9	FS	I	**Frame Synchronization.** This positive pulse signal marks the beginning of a concentration highway frame every 125 μs (8 kHz). Individual slots are assigned relative to the detection of FS. This pulse is also used by the 4-wire line transceiver to align for link frames. Because of this, the FS input must have an overall 8-kHz stability of $\pm$ 100 ppm and meet a maximum peak-to-peak jitter specification of 160 ns. In addition, FS must be phase-locked to CLKXR to eliminate the possibility of an occasional slipped or extra bit over long intervals. **CAUTION:** If FS and CLKXR do not have a guaranteed correlation, CLKXR may slide relative to the FS pulse, which then could be detected on an incorrect CLKXR edge.
11	10	DRA	I	**Data Received on Highway A.** Serial time-slot information is received on this highway at the CLKXR clock rate. The data is expected to be stable according to the following options: a) on a positive or negative CLKXR edge; b) after a 0- to 7-bit period delay; c) after a 0- to 63-time-slot delay; d) with bit 0 or bit 7 arriving first. Options a—d are under the programmable control of the user. **Note:** It is recommended that DRA be pulled up by an external resistor to prevent random data patterns from propagating through the T7252A UNITS if reception happens to be inadvertently enabled.
12	11	DRB	I	**Data Received on Highway B.** Serial time-slot information is received on this highway at the CLKXR clock rate. The data is expected to be stable under the same options described for DRA. These options are explained in detail in Table 3. **Note:** It is recommended that DRB be pulled up by an external resistor to prevent random data patterns from propagating through the the T7252A UNITS if reception happens to be inadvertently enabled.
13	12	$\overline{\text{TSCA}}$	O	**Time-Slot Control for Highway A.** This active-low signal can be used to enable external 3-stating bus drivers to drive serial time-slot information onto highway A at specified times. $\overline{\text{TSCA}}$ returns to a 3-state condition when it is not active.

Table 1. Pin Descriptions (Continued)

PLCC	DIP	Symbol	Type	Name/Function
14	13	DXA	O	**Data Transmitted on Highway A.** At specified times, the T7252A UNITS drives serial time-slot information onto this highway at the CLKXR clock rate. The data is driven according to the following options: a) on a positive or negative CLKXR edge; b) after a 0- to 7-bit period delay; c) after a 0- to 63-time-slot delay; d) with bit 0 or bit 7 arriving first. Options a—d are under the programmable control of the user. DXA returns to a 3-state condition when it is not driving the bus. **Note:** It is recommended that DXA be pulled up by an external resistor to prevent random data patterns from propagating through other devices when DXA is not enabled (3-stated).
15	14	$\overline{\text{TSCB}}$	O	**Time-Slot Control for Highway B.** This active-low signal is used to enable external 3-stating bus drivers to drive serial time-slot information onto highway B at specified times. $\overline{\text{TSCB}}$ returns to a 3-state condition when it is not active.
16	15	DXB	O	**Data Transmitted on Highway B.** At specified times, the T7252A UNITS drives serial time-slot information onto this highway at the CLKXR clock rate. The data is driven according to the same options described for DXA. These options are explained in detail in Table 3. DXB returns to a 3-state condition when it is not driving the bus. **Note:** It is recommended that DXB be pulled up by an external resistor to prevent random data patterns from propagating through other devices when DXB is not enabled (3-stated).
17	—	NC	—	**No Connection.**
18	16	V_{DDR}	—	**Line Receiver 5 V Supply.** Analog power supply for the subscriber line receiver.
19	17	VT	I	**Line Receiver Center Tap.** A 0.1-μF decoupling capacitor should be tied from this pin to analog ground to provide a clean voltage reference level for the receiver.
20	18	RNR	I	**Receive Negative Rail.** Negative input of analog receiver, which accepts an alternate space inversion (ASI) stream from the secondary of a 2.5:1 transformer.*
21	—	NC	—	**No Connection.**
22	19	RPR	I	**Receive Positive Rail.** Positive input of analog receiver, which accepts an alternate space inversion (ASI) stream from the secondary of a 2.5:1 transformer.

* The two receiver inputs, RNR and RPR, connect to the secondary (or 2.5) side of the transformer.

Table 1. Pin Descriptions (Continued)

PLCC	DIP	Symbol	Type	Name/Function
23	20	VSSR	—	**Line Receiver Analog Ground.** Analog ground for the subscriber line receiver. VSSR is not internally connected to other grounds.
24	21	$\overline{INT}$	O	**Interrupt.** This active-low interrupt signal may be generated when specified conditions are flagged in the interrupt register. The interrupt signal remains active until the microprocessor concludes a read of the interrupt status register. After such a read completes, $\overline{INT}$ returns to a 3-state condition if no new interrupt conditions occurred during the read cycle.
25—28	22—25	A3—A0	I	**Address Bus.** These four address leads allow control of the chip by a microprocessor that employs separate address and data leads. They are used to select the internal registers (defined in Table 2). If a multiplexed address/data bus is used, A0—A3 must be stable prior to the falling edge of address latch enable (ALE). For a microprocessor with nonmultiplexed buses, ALE must be tied high and A0—A3 must remain stable throughout the register access. A0 is the LSB.
29	—	NC	—	**No Connection.**
30—33 35—38	26—29 31—34	AD0—AD7	I/O	**Address/Data Bus.** These pins provide an 8-bit bi-directional, noninverting, 3-stating bus. AD0—AD7 are used either as a multiplexed address/data bus or as a data-only bus. The bus direction is controlled by the logic states of $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$. During read or write cycles, a microprocessor using a multiplexed bus sends address information on AD0—AD3, synchronized to the ALE signal. During read cycles, data is sent by the T7252A UNITS and received by the microprocessor on these lines; during write cycles, data is transmitted by the microprocessor on these lines. When $\overline{CS}$ is not active, AD0—AD7 are placed in a high-impedance state (3-stated). AD0 is the LSB. **Note:** If addresses are multiplexed on the bus, the separate address lines, A0—A3, must be strapped either to AD0—AD3 or to a transparently latched or buffered version of these leads. Other multiplexed address leads can be tied to A0—A3 if a different addressing scheme is desired.
34	30	VSS	—	**Digital Ground.**
39	35	$\overline{WR}$	I	**Write.** This signal controls when data is written to the registers. When $\overline{CS}$ and $\overline{WR}$ are low, valid data is to be supplied by the microprocessor on lines AD0—AD7. The T7252A UNITS latches the data on the rising edge of $\overline{WR}$.

Table 1. Pin Descriptions (Continued)

PLCC	DIP	Symbol	Type	Name/Function
40	36	$\overline{RD}$	I	**Read.** This signal is used to read data from the registers. When $\overline{CS}$ and $\overline{RD}$ are low, the T7252A UNITS makes the requested data to be read by the microprocessor available on lines AD0—AD7.
41	37	$\overline{CS}$	I	**Chip Select.** This signal must be active for the T7252A UNITS to enable the data bus so that the internal registers can be read from or written to. The on-chip registers can be selected when this signal is low.
42	38	ALE	I	**Address Latch Enable.** A high-to-low transition on this pin is used to load an internal latch with the address on pins A0—A3. The internal address follows A0—A3 when ALE is high and freezes on the last latched state of A0—A3 when ALE goes low.
43	39	$\overline{RESET}$	I	**Reset.** A low on this pin resets the device and forces a high-impedance 3-state condition on all outputs. All register bits are forced to their default state (see Table 4). After a low-to-high transition on this pin, the T7252A UNITS must receive a frame pulse on the FS pin, with an operational 6.144-MHz master clock, to be released fully from reset.
44	40	V_{DD}	—	**Digital 5 V Supply.**

Overview

CCITT Recommendation I.430 describes the layer 1, or physical layer, connection of ISDN equipment at the S/T interface. Specified parameters include voltage levels, impedance templates, bit timing and coding, and other electrical characteristics. These details apply only to the basic access link between a network termination (for example, a digital switch) and either another network termination (NT) or a variable number of subscriber terminal equipment (TE) endpoints. The complementary interface between the link and the switch fabric internal to an NT is not subject to standardization. The T7252A UNITS chip features a unique TDM highway architecture that facilitates high-speed information transfer between multiple chips residing on a single bus.

Figure 1 provides two block diagrams of the T7252A UNITS. Functionally, the chip can be divided into four sections: the 4-wire line transceiver interface, the 2B+D multiplex/demultiplex core, the concentration highway access time-slot (CHATS) interface, and the microprocessor interface. The line transceiver interface handles transmissions to and from the CCITT I.430 4-wire link. The core interprets the frames received from the line transceiver and generates frames to be transmitted onto the link. It exchanges full-duplex 2B+D information with the CHATS interface, which provides access to the serial highways for the B1, B2, and D channels. The microprocessor interface is the window through which the T7252A UNITS is configured and controlled.

The T7252A UNITS requires three clock/framing signals. A 6.144-MHz $\pm$ 250 ppm master clock must be supplied on the XTAL1 pin. A frame synchronization (FS) pulse and concentration highway clock (CLKXR) are also needed. The CLKXR speed, which determines serial highway timing, is at the discretion of the user, but the FS pulse must be 8 kHz $\pm$ 100 ppm, with a maximum peak-to-peak jitter of 160 ns. These stability limits on FS, used to bound both link and highway frames, stem from specifications in Recommendation I.430. In addition, the master clock should have a nominal 50% duty cycle to minimize the jitter of the 192-kHz clock internally derived to control link transmissions.

4-Wire Line Transceiver Interface

The 4-wire line transceiver interface supports the encoding and decoding of the 2B+D stream in the alternate space inversion (also known as pseudoternary) line-code signal format (see Figure 4). Transmission occurs over four wires, normally 26 AWG or larger twisted pairs, between the NT and the TE(s).* The transceiver interface contains an analog transmitter and receiver, which are to be connected to external 2.5:1 transformers. The line driver, a voltage-limited current source, collects the 2B+D signals from the multiplex/demultiplex core, frames the channels, and transmits the stream to the TE(s). The line receiver performs filtering, timing recovery, frame synchronization, and threshold slicing, recovering the 2B+D signals from the TE(s) and passing them to the core. In accordance with the CCITT Recommendation I.430, the transceiver supports point-to-point and point-to-multipoint (passive bus) applications. Multiframe and activation/deactivation procedures are also provided, under the control of the microprocessor interface.

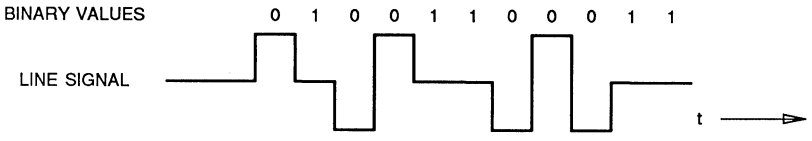


Figure 4. Alternate Space Inversion (ASI) Code

2B+D Multiplex/Demultiplex Core Interface

The 2B+D multiplex/demultiplex core interface receives the 192-kb/s subscriber stream from the line receiver and extracts the B- and D-channel information. The channels are saved in holding registers for transfer to time slots on one of two serial, full-duplex highways (described below). Conversely, to send 2B+D information to the subscriber line, the bits are first received from the interface to the two highways, placed into a basic access frame, and then routed to the line transmitter for transmission at 192 kb/s. No HDLC termination is performed on any B or D channel. The multiplex/demultiplex core uses a 192-kHz clock, derived from the 6.144-MHz master clock via a digital divider, for its link timing in both directions.

Concentration Highway Access Time-Slot (CHATS) Interface

The CHATS interface can be configured to meet a variety of system interfaces. It supports two pairs of transmit and receive paths (buses), which connect the T7252A UNITS and a digital switching network via 8-bit time slots that can carry voice, data, or control channels. The transmission speed on these highways depends on the bit rate of the highway clock (CLKXR). For example, with a 2.048-MHz clock, 32 time slots are supported in each direction on each serial pair; with a 4.096-MHz clock, 64 time slots are supported in each direction on each full-duplex highway. CHATS deciphers the highways' clock rate directly from the number of clock edges between frame synchronization pulses. Time slots are programmable for the B1, B2, and D transmit/receive paths to and from the digital switch. In addition, highway bit and time-slot offsets, plus clock edges, are fully programmable. The capability to swap the order of the bits in a highway time slot is also included. All highway-configuration registers must be supervised by a microprocessor.

Microprocessor Interface

The microprocessor interface allows parallel asynchronous input/output access to the on-chip registers that control the operation of the device. A general-purpose microprocessor can read or write

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* A basic access link can also connect one NT to another. In the interest of brevity, consider this case implicit when the text describes interaction between the NT and the TE(s).

the registers via either multiplexed or demultiplexed address and data lines, at the designer's discretion. During a register read, the T7252A UNITS latches data to be transmitted to the microprocessor bus, ensuring that data changes occurring within the read cycle do not pass to the bus. Register accesses are sufficiently fast that wait states should not generally be required. The T7252A UNITS also provides a maskable interrupt signal. It may be activated on detection of a link error, the start of a transmitted multiframe, a change in the received INFO state, and/or a change in state of the received Q bits.

Registers

The microprocessor interface, used to control and monitor the device, can be configured to be compatible with microprocessors having multiplexed or demultiplexed address/data buses. The on-chip registers occupy 16 locations in the memory map of the controlling microprocessor. They are accessed under the control of the following signals: address select (A0—A3 or AD0—AD3), address latch enable (ALE), chip select ($\overline{CS}$), read ($\overline{RD}$), write ($\overline{WR}$), and data (AD0—AD7).

Register bit assignments are shown in Table 2, bit functions are described in detail in Table 3; and register bit polarities and reset states are summarized in Table 4. Registers 0—4 specify operational parameters (clock edges, synchronization offsets, loop control, and channel-insertion control) for the dual concentration highway transmit and receive paths. Registers 5 and 6 allow the microprocessor to insert or remove channel information directly. For example, they can be used during chip testing or to place one of the channels (B1, B2, or D) under microprocessor, rather than hardware, control. Interrupt masks and other controls are provided in register 7. Four bits in register 8 supply the Q bits received in the last superframe interval, with another four bits controlling the NT-to-TE S channel. Registers 9—14 are time-slot and highway-assignment registers for the transmission and reception of B1-, B2-, and D-channel information. Register 15 is the interrupt status register.

The following describes each register in detail:

Register 0 (R0) – contains the concentration highway transmitted bit offset (with a range of 0—7), clock edge (rising or falling), and leading bit (low or high) specifications, plus the frame edge parameter (the transition of CLKXR on which to sample FS).

Register 1 (R1) – contains the received bit offset, clock edge, and leading bit fields, plus a fixed timing bit, which alters the sampling characteristics of the 4-wire receiver.

Register 2 (R2) – includes the transmitted time-slot offset bits (with a range of 0—63), plus the soft reset (RST) and power-up/-down (PWRUD) bits.

Register 3 (R3) – holds the received time-slot offset and the OPEN bit, which can be used to disable the concentration highway when changing register contents. R3 also has a TEST bit, which can put the T7252A UNITS into a special mode for manufacturing purposes.

Register 4 (R4) – contains the loopback and exchange fields. The following loopbacks are supported: transparent and nontransparent loops of B1, B2, D, and 2B+D at ISDN reference points 2 and 3; loops of B1, B2, B1+B2, and 2B+D at ISDN reference points B1 and C1; and no loop in transparent and nontransparent mode (i.e., transmitter on and transmitter off). The exchange control registers allow B1, B2, or D to be supplied or extracted via the microprocessor interface. If the D channel is chosen, only bits 1 and 0 of R5 and/or R6 are meaningful, with bit 0 being the first bit transmitted to or received from the link.

Register 5 (R5) – is the exchange byte to be transmitted to the 4-wire link. It is write-only. When read, it returns internal test points for chip verification after fabrication.

Register 6 (R6) – is the exchange byte received from the link. It is read-only.

Register 7 (R7) – contains interrupt masks and the transmit signal field. The following interrupt conditions can be masked by bits in this register: interrupt (the ORed sum of the other conditions), link error (missing or extra bipolar violations), received signal change (new received INFO state), start of multiframe (on the transmit side), and Q-bits state change (new 4-bit Q field received in the last multiframe). These mask bits prevent activation of the interrupt lead when the specific condition

occurs; they do not prevent the interrupt bits in R15 from being set. The other field in R7, transmit signal, specifies whether all 0s or the INFO 0, 2, or 4 pattern is to be transmitted.

Register 8 (R8) – supplies the four Q bits received in the last multiframe and holds the S bits to be transmitted in the next four link frames. The S bits can be written and read; the Q bits are read-only.

Register 9—11 (R9—R11) – contain the concentration highway transmit time-slot number and bus enable bits (A and/or B) for the B1, B2, and D channels. The T7252A UNITS does not transmit in a given time slot if two or all three channels are programmed for that same time slot. D-channel bits are transmitted in time-slot bits 0 and 1 or 6 and 7, with bit 0 or bit 7 being the first bit received from the 4-wire link.

Register 12—14 (R12—R14) – contain the receive time-slot number, a bus selection bit, and a bus enable bit. Only one bus (A or B) can be selected per channel. If two or all three channels are set to the same time slot, the input pin(s) is ignored, causing 1s to be received. The D-channel bits are received in time-slot bits 0 and 1 or 6 and 7, with bit 0 or bit 7 being transmitted onto the 4-wire link first.

Register 15 (R15) – collects the interrupt bits and the received signal field. The interrupts are the same as described for R7 above, and each is set when the appropriate interrupt condition occurs, regardless of the state of its mask bit. The received signal bits report receipt of bit pattern INFO 0, 1, or 3. R15 is read-only.

Modifications to the various registers take effect at different points, depending on the specific register field. Changes made to R0—R3 and R9—R14 begin at an FS pulse, except for alterations to OPEN, RST, and PWRUD. When OPEN is cleared or PWRUD is set, the effect is immediate. When the reverse occurs, the chip opens or activates at an FS pulse. RST follows the same strategy. When R4 is modified, the change is synchronized with the beginning of the transmitted frame on the 4-wire link. R5 cannot be written within a window of 200 ns after the rising edge of each FS pulse or the contents do not propagate correctly onto the link. Writes at all other times are allowed. The same window applies to reads of R6 and writes of R8 (the S bits). New transmit signal states begin with the I.430 transmitted frame. All other R7 changes are immediate. Writes to the S bits in R8 are copied internally, as shown in Table 3. New interrupt conditions in R15 and changes to the Q bits in R8 occur within the 200-ns window after the rising edges of FS.

A few miscellaneous characteristics of the registers should be noted:

- After an external reset, all registers are programmed to the initial state described in Table 4. Spare bits are read as 0s and are read-only. Soft resets, invoked by setting the RST bit, do not alter the register contents, except for the secondary effects on status bits.
- Reads of R15 clear all interrupt status bits but do not affect the received signal field. New interrupts that occur during an R15 read are detected and retained, except for those whose status bits were already set in the register prior to the beginning of the read. These interrupts are assumed to have been passed to the microprocessor during the read and are cleared.
- If the contents of a time-slot control register (R9—R14) are altered when OPEN is set, and if the channel controlled by that register is being transmitted onto or received from the concentration highway at the time of the register write, the appropriate output (DXA and/or DXB) or input (DRA or DRB) is disabled. Depending on the register in question, for the duration of the time slot either the output pin(s) 3-states immediately or the input pin is ignored, causing 1s to be received. The time-slot numbers programmed in these registers must be less than the maximum number of time slots available on the concentration highway; otherwise, the corresponding channel is not transmitted/received.
- If an exchange register (R5 and/or R6) is to be used during normal operation, an 8-kHz interrupt to the microprocessor is necessary for information to be supplied to or read from the register at the correct rate. In addition, for the S field in R8 to be loaded continuously with new information by the microprocessor, the new data must be written at 1-ms intervals.

Table 2. Register Bit Assignments

Name	Main Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R0	Highway configuration transmit	FE	spare	spare	XLBIT	XCE	XBOFF2—0		
R1	Highway configuration receive	FT	spare	spare	RLBIT	RCE	RBOFF2—0		
R2	Time-slot offset transmit	RST	PWRUD	XTSOFF5—0					
R3	Time-slot offset receive	OPEN	TEST	RTSOFF5—0					
R4	Loopback and exchange control	XXCHNG1—0		RXCHNG1—0		LOOPBCK3—0			
R5	Transmit byte exchange	XXBYTE							
R6	Receive byte exchange	RXBYTE							
R7	Interrupt and TS control	MASK	LERRM	TS1—0		RSCM	SOMM	QSCM	spare
R8	S and Q Bits	S3—0				Q3—0			
R9	Transmit B1 time slot	XB1A	XB1B	XB1TS5—0					
R10	Transmit B2 time slot	XB2A	XB2B	XB2TS5—0					
R11	Transmit D time slot	XDA	XDB	XDTS5—0					
R12	Receive B1 time slot	RB1EN	RB1AB	RB1TS5—0					
R13	Receive B2 time slot	RB2EN	RB2AB	RB2TS5—0					
R14	Receive D time slot	RDEN	RDAB	RDTS5—0					
R15	Interrupt status	INT	LERR	RS1—0		RSC	SOM	QSC	spare

Notes:

The first letter "X" indicates the transmit direction (concentration highway to the switch complex for the concentration highway interface; NT to TE(s) for the line transceiver).

The first letter "R" indicates the receive direction (concentration highway from the switch complex for the concentration highway interface; TE(s) to NT for the line transceiver), except for the RST bit.

Offsets and edge selections apply to both highway A and highway B.

All multiple-bit fields in the registers are encoded with the field's most significant bit in the highest register bit position (e.g., XBOFF2 is bit 2 in R0).

Spare bits are 0s when read.

Table 3. Register Bit Definitions

Name	Bit	Symbol	Name/Function
R0	0—2	XBOFF	**Transmitted Bit Offset.** These three bits provide a fixed offset, relative to the framing strobe, FS, for the first bit transmitted in each time slot on either highway A or B. The offset is the number of CLKXR clock periods by which the first bit transmission on DXA or DXB is delayed. All subsequent transmissions also follow this offset.
R0	3	XCE	**Transmitted Bit Clock Edge.** When this bit is set, bits are transmitted on DXA and/or DXB on the rising edge of the reference clock CLKXR; when this bit is cleared, the falling edge of CLKXR is used.
R0	4	XLBIT	**Transmitted Leading Bit.** This option allows the order of bytes to be reversed as they pass through UNITS. When this bit is set, the first or low bit (bit 0) received in a channel on the 4-wire link is transmitted first in a highway time slot; when this bit is cleared, the last or high bit 7 is transmitted first. For time slots carrying D-channel information, only highway time-slot bits 0 and 1 or 7 and 6 carry the actual D bits from the link; the other six bits are set. The XLBIT field does not affect the contents of either of the exchange registers (R5 and R6).
R0	5,6	—	**Spare.**
R0	7	FE	**Frame Edge.** When this bit is set, the frame synchronization strobe, FS, is sampled on the negative edge of the bit clock (CLKXR); when this bit is set to cleared, FS is sampled on the positive edge of CLKXR. **Note:** The FE bit is not specific to the transmit direction of the dual concentration highway. It is placed in this register because of space considerations only.
R1	0—2	RBOFF	**Received Bit Offset.** These three bits provide a fixed offset, relative to FS, for the first bit received in each time slot on either highway A or B. The offset is the number of CLKXR clock periods by which the first bit reception on DXA or DXB is delayed. All subsequent receptions also follow this offset.
R1	3	RCE	**Received Bit Clock Edge.** When this bit is set, bits are received from DRA or DRB on the rising edge of the bit clock (CLKXR); when this bit is cleared, the falling edge of CLKXR is used.
R1	4	RLBIT	**Received Leading Bit.** This option allows the order of bytes to be reversed as they pass through UNITS. When this bit is set, the first or low bit (bit 0) received in a time slot on the highway is the first bit transmitted in the appropriate channel on the 4-wire link. When this bit is cleared, the last or high bit (bit 7) is transmitted on the link first. For time slots carrying D-channel information, only bits 0 and 1 or 7 and 6 are expected to carry the actual D bits on the highway; the other six bits are ignored. The RLBIT field does not affect the contents of either of the exchange registers (R5 and R6).

Table 3. Register Bit Definitions (Continued)

Name	Bit	Symbol	Name/Function
R1	5,6	—	**Spare.**
R1	7	FT	**Fixed Timing.** Although the 4-wire receiver is designed to use adaptive timing with all possible link configurations, a fixed-timing option is also provided. When this bit is cleared, the adaptive mode is employed to synchronize to the received bit stream. When this bit is set, the received stream is sampled 4.2 μs after the leading edge of each 192-kHz transmit bit interval. **Note:** The FT bit is not specific to the receive direction of the dual concentration highway. It is placed in this register because of space considerations only.
R2	0—5	XTSOFF	**Transmit Time-Slot Offset.** The value in these six bits defines the time-slot delay on DXA or DXB between the selected frame synchronization (FS) edge and the beginning of a new virtual transmit TDM (time-division multiplexed) frame on the dual concentration highway. If the clock rate supplied on the CLKXR pin is lower than 4.096 MHz, any unnecessary upper bits should be cleared. The values in R9—R11 relate to the new, offset transmit TDM frame, not the frame defined by FS.*
R2	6	PWRUD	**Power-Up/-Down.** This bit allows the microprocessor to put the T7252A UNITS in a power-down, or standby, mode. When PWRUD is set, putting the chip in standby, clocks are cut from all circuitry except the 4-wire receiver and a small portion of the core block, all digital input buffers except $\overline{CS}$, A0—A3, and ALE are disabled, and all output drivers are 3-stated. The chip continues to monitor the link for an activation sequence from the TE(s) and interrupts the controlling microprocessor if activity is detected. If the $\overline{CS}$ pin is activated, the microprocessor-interface buffers are enabled for the duration of the register access, then disabled again when $\overline{CS}$ returns to the high state. The power-down mode cuts the power consumption of the device by 50% to 75%, depending on traffic-based driver activity prior to entering the standby mode. When the PWRUD bit is cleared, the chip is in normal mode. When the chip powers up on a high-to-low transition of PWRUD, an automatic soft reset is performed to initialize the device before beginning operation (see the RST bit). **Note:** PWRUD is not specific to the transmit direction of the dual concentration highway. It is placed in this register because of space considerations only.

* The actual beginning of the virtual transmit TDM frame is located at an offset equal to [XBOFF + (8 X TSOFF)].

Table 3. Register Bit Definitions (Continued)

Name	Bit	Symbol	Name/Function
R2	7	RST	**Soft Reset.** The RST bit, when set, causes a soft reset of the device, initializing UNITS in the same manner as the $\overline{\text{RESET}}$ pin. Internal circuits assume their default state, and all UNITS output drivers 3-state. However, unlike the external reset, a soft reset does not alter the register contents, which retain their values and do not go to the configuration shown in Table 4. The only exception is R15. When RST is cleared, UNITS is not in a soft reset condition. After the RST bit is cleared, an FS pulse and an active 6.144-MHz clock are needed to release UNITS from the soft reset. **Note:** RST is not specific to the transmit direction of the dual concentration highway. It is placed in this register because of space considerations only.
R3	0—5	RTSOFF	**Received Time-Slot Offset.** The value in these six bits defines the time-slot delay on DRA or DRB between the selected frame synchronization (FS) edge and the beginning of a new virtual receive TDM (time-division multiplexed) frame on the dual concentration highway. If the clock rate supplied on the CLKXR pin is lower than 4.096 MHz, any unnecessary upper bits should be cleared. The values in R12—R14 relate to the new, offset receive TDM frame, not the frame defined by FS.*
R3	6	TEST	**Test Mode.** When this bit is set, UNITS enters a test mode for manufacturing testing purposes. All UNITS users should clear this bit for normal operation. **Note:** TEST is not specific to the receive direction of the dual concentration highway. It is placed in this register because of space considerations only.
R3	7	OPEN	**Open or Close the Concentration Highway.** The OPEN bit can be used to disable the concentration highway when changing register contents. This allows the controlling microprocessor to write registers to the desired configuration before UNITS is permitted to begin functioning normally. After the chip is initially released from external reset, all highway drivers are 3-stated until OPEN is set, after which normal highway operation is enabled on either the first or second FS pulse received. Reception from the highways is also disabled until OPEN is set, causing all 1s to appear in information channels on the link. If OPEN is set and later cleared, the concentration highway drivers again 3-state and the input buffers become disabled, with operation resuming in the same manner when OPEN is returned to one. The OPEN bit does not affect the 4-wire transmitter. **Note:** OPEN is not specific to the receive direction of the dual Concentration Highway. It is placed in this register because of space considerations only.

* The actual beginning of the virtual receive TDM frame is located at an offset equal to [RBOFF + (8 RTSOFF)].

Table 3. Register Bit Definitions (Continued)

<table>
<tr><th>Name</th><th>Bit</th><th>Symbol</th><th>Name/Function</th></tr>
<tr><td>R4</td><td>0—3</td><td>LOOPBCK</td><td>
Loopback Control. These four bits encode 16 different, exclusive loopback configurations, which provide a superset of the CCITT I.430 requirements. Figure 5 shows the loopbacks specified in Recommendation 1.430. The following miscellaneous items apply to the table below:

Transparent means that the analog transmitter is on, and non-transparent means that the analog transmitter is 3-stated for the channels looped (sending all 1s on the 4-wire interface).
For encoding 0100, the link E bits follow the highway D bits, not the link D bits sent from the TE, since the latter are discarded during this loopback.
For encoding 1000, the INFO 0 line state appears on the 4-wire interface.
For loop B1/C1, the looped channels are inserted in NT-to-TE frames in the appropriate bit positions only (the full TE-to-NT stream is not looped for encoding 1100).
No channels are examined by UNITS during any of these loopbacks.

<table>
<tr><th>b3—b0</th><th>Meaning</th></tr>
<tr><td>0000</td><td>Transmitter 3-stated</td></tr>
<tr><td>0001</td><td>Transparent, loop 2/3, B1 looped</td></tr>
<tr><td>0010</td><td>Transparent, loop 2/3, B2 looped</td></tr>
<tr><td>0011</td><td>Transparent, loop 2/3, D looped</td></tr>
<tr><td>0100</td><td>Transparent, loop 2/3, 2B+D looped</td></tr>
<tr><td>0101</td><td>Nontransparent, loop 2/3, B1 looped</td></tr>
<tr><td>0110</td><td>Nontransparent, loop 2/3, B2 looped</td></tr>
<tr><td>0111</td><td>Nontransparent, loop 2/3, D looped</td></tr>
<tr><td>1000</td><td>Nontransparent, loop 2/3, 2B+D looped</td></tr>
<tr><td>1001</td><td>Loop B1/C1, B1 looped</td></tr>
<tr><td>1010</td><td>Loop B1/C1, B2 looped</td></tr>
<tr><td>1011</td><td>Loop B1/C1, B1 and B2 looped</td></tr>
<tr><td>1100</td><td>Loop B1/C1, 2B+D looped</td></tr>
<tr><td>1101</td><td>Spare</td></tr>
<tr><td>1110</td><td>Spare</td></tr>
<tr><td>1111</td><td>Transparent, no loopback (normal operation)</td></tr>
</table>
</td></tr>
</table>

Table 3. Register Bit Definitions (Continued)

Name	Bit	Symbol	Name/Function
R4	4,5	RXCHNG	**Received Byte Exchange Control.** The encoding in these two bits specifies the channel to be extracted from the 2B+D stream received by the 4-wire receiver and installed in R6, as shown in the following table. If desired, the selected channel can also be transmitted on highway A or B under the control of R9, R10, or R11. **b1—b0** **Meaning** 00 B1 exchanged 01 B2 exchanged 10 D exchanged 11 D exchanged
R4	6,7	XXCHNG	**Transmitted Byte Exchange Control.** The encoding in these two bits specifies which channel in the 2B+D stream transmitted by the 4-wire transmitter is to be supplied through register R5. When an exchange is desired, the contents of R5 are installed in the selected transmit channel. If R5 is not updated between occurrences of the channel on the 4-wire interface, the last byte written to R5 is repeated. Transmitted byte exchanges have priority over channel specifications in R12, R13, or R14 and also over loopbacks. The bit encodings for the XXCHNG bits are: **b1—b0** **Meaning** 00 No exchange 01 B1 exchanged 10 B2 exchanged 11 D exchanged
R5	0—7	XXBYTE	**Transmitted Byte Exchange.** A byte loaded by the microprocessor into this register can be installed as B1-, B2-, or D-channel information to be transmitted to the 4-wire interface. The channel selected for exchange with the microprocessor is controlled by the XXCHNG bits in register R4. If R5 is not updated between occurrences of the channel on the 4-wire interface, the last byte written to R5 is repeated. Transmitted byte exchanges have priority over channel specifications in R12, R13, or R14. If the D channel is chosen, only bits 1 and 0 of R5 are meaningful, with bit 0 being the first D bit transmitted onto the link. The upper six bits are ignored. This register is write-only as an exchange register. When read, it returns internal test points for chip verification after fabrication. The controlling microprocessor can test R5 by putting UNITS into a loopback of the appropriate channel at ISDN reference point 2/3, writing R5, and reading the contents of R6, the received byte exchange register.

Table 3. Register Bit Definitions (Continued)

Name	Bit	Symbol	Name/Function
R6	0—7	RXBYTE	**Received Byte Exchange.** This register is continually loaded with the contents of the channel specified by the RXCHNG bits in R4. The specified channel is extracted from the 2B+D stream collected by the 4-wire receiver, and then installed in R6. If desired, the selected channel can also be transmitted on highway A or B under the control of R9, R10, or R11. If the D channel is chosen, only bits 1 and 0 of R6 are meaningful, with bit 0 being the first D bit received from the link. The upper six bits are set. This register is read-only.
R7	0		**Spare.**
R7	1	QSCM	**Q-Bits State Change Mask.** When this bit is set, the QSC bit in R15 does not cause an interrupt; when this bit is cleared, the QSC interrupt is enabled.
R7	2	SOMM	**Start of Multiframe Mask.** When this bit is set, the SOM bit in R15 does not cause an interrupt; when this bit is cleared, the SOM interrupt is enabled.
R7	3	RSCM	**Receive Signal Change Mask.** When this bit is set, the RSC bit in R15 does not cause an interrupt; when this bit is cleared, the RSC interrupt is enabled.
R7	4,5	TS	**Transmit Signal.** These two bits encode the INFO state to be transmitted onto the 4-wire interface, as follows: **b1—b0** — **Meaning** 00 — INFO 0 – All 1s transmitted (no frames) 01 — Test pattern – All 0s transmitted 10 — INFO 2 – Valid frames with 0s in B1,B2,D,E,A,S,M 11 — INFO 4 – Valid frames with normal channel traffic to the TE INFO 0 indicates to the TE that it can deactivate (power down). INFO 2 is an intermediate activation state and INFO 4 is normal operation. When encoding "10" is written, the INFO 2 line state is always forced to commence with the first frame of a superframe soon after the next FS pulse. This fact can be used to synchronize multiframes between multiple UNITS devices. Multiframe continuity is not maintained when falling from INFO 4 to INFO 2, and a change from INFO 2 to INFO 4 does not begin a new multiframe.
R7	6	LERRM	**Link Error Mask.** When this bit is set, the LERR bit in R15 does not cause an interrupt; when this bit is cleared, the LERR interrupt is enabled.
R7	7	MASK	**Interrupt Mask.** When this bit is set, no interrupts are generated on the $\overline{\text{INT}}$ pin; when this bit is cleared, interrupts may occur.

Table 3. Register Bit Definitions (Continued)

Name	Bit	Symbol	Name/Function
R8	0—3	Q	**Multiframe Q Bits.** These four bits reflect the four Q bits (Q3—Q0) received in the last completed multiframe (superframe). If any of the four Q bits in the last received multiframe differs from the Q bits of the previous multiframe, an interrupt is generated through the QSC bit in R15. This field is loaded soon after the last Q bit arrives in each multiframe, several link frames prior to the beginning of the next multiframe. All four Q bits are installed at the same time; they do not shift into Q3—Q0 as they arrive. These bits are read-only.
R8	4—7	S	**S Channel.** This field supplies the S bits to be transmitted in the next four link frames. The four register bits are copied internally once every four link frames, just after the FS pulse. Bit S0 is then sent in the S bit position in the first link frame, with bits S1, S2, and S3 following in the next three frames. If R8 has been reloaded in the interim, the next four S bits are again copied from R8 at the beginning of the following frame. If new bits have not been written to R8 during these four frames, the four S bits just sent are repeated in the same order. No feedback on the status of S channel is provided.
R9	0—5	XB1TS	**Transmit B1 Time Slot.** These six bits, ranging in value from 0 to 63, define the transmit time-slot number for B1-channel information on the chosen highway (A or B). The value relates to the virtual transmit TDM frame as offset by the XTSOFF field in R2 and the XBOFF field in R0, not the frame defined by FS.
R9	6	XB1B	**Transmit B1 on Concentration Highway B.** When this bit is set, channel B1 is transmitted on highway B; when this bit is cleared, channel B1 does not appear on highway B, and the DXB pin remains 3-stated during the time slot given in XB1TS.
R9	7	XB1A	**Transmit B1 on Concentration Highway A.** When this bit is set, channel B1 is transmitted on highway A; when this bit is cleared, channel B1 does not appear on highway A, and the DXA pin remains 3-stated during the time slot given in XB1TS.
R10	0—5	XB2TS	**Transmit B2 Time Slot.** These six bits, ranging in value from 0 to 63, define the transmit time-slot number for B2-channel information on the chosen highway (A or B). The value relates to the virtual transmit TDM frame.
R10	6	XB2B	**Transmit B2 on Concentration highway B.** When this bit is set, channel B2 is transmitted on highway B; when this bit is cleared, channel B2 does not appear on highway B, and the DXB pin remains 3-stated during the time slot given in XB2TS.
R10	7	XB2A	**Transmit B2 on Concentration Highway A.** When this bit is set, channel B2 is transmitted on highway A; when this bit is cleared, channel B2 does not appear on highway A, and the DXA pin remains 3-stated during the time slot given in XB2TS.

Table 3. Register Bit Definitions (Continued)

Name	Bit	Symbol	Name/Function
R11	0—5	XDTS	**Transmit D Time Slot.** These six bits, ranging in value from 0 to 63, define the transmit time-slot number for D-channel information on the chosen highway (A or B). If the XLBIT flag is set, the two D-channel bits appear in highway time-slot bits 1 and 0 (the latter being the first bit received from the 4-wire link), with the remaining bits in the time slot set to one. If XLBIT is cleared, the first D bit received from the link is placed in bit 7 of the time slot, the second D bit is assigned to bit 6, and the remaining bits are set. The value of XDTS relates to the virtual transmit TDM frame.
R11	6	XDB	**Transmit D on Concentration Highway B.** When this bit is set, channel D is transmitted on highway B; when this bit is cleared, channel D does not appear on highway B, and the DXB pin remains 3-stated during the time slot given in XDTS.
R11	7	XDA	**Transmit D on Concentration Highway A.** When this bit is set, channel D is transmitted on highway A; when this bit is cleared, channel D does not appear on highway A, and the DXA pin remains 3-stated during the time slot given in XDTS.
R12	0—5	RB1TS	**Receive B1 Time Slot.** These six bits, ranging in value from 0 to 63, define the receive time-slot number for B1-channel information on the chosen highway (A or B). The value relates to the virtual receive TDM frame as offset by the RTSOFF field in R3 and the RBOFF field in R1, not the frame defined by FS.
R12	6	RB1AB	**Receive B1 Concentration Highway A or B.** When this bit is set, highway B is selected for serial reception; when this bit is cleared, highway A is chosen.
R12	7	RB1EN	**Receive B1 Reception Enable.** When this bit is set, B1-channel information is received on the chosen highway and time slot; when this bit is cleared, no B1 reception occurs, the time slot is ignored and all 1s are transmitted to the TE in the B1 fields.
R13	0—5	RB2TS	**Receive B2 Time Slot.** These six bits, ranging in value from 0 to 63, define the receive time-slot number for B2-channel information on the chosen highway (A or B). The value relates to the virtual receive TDM frame.
R13	6	RB2AB	**Receive B2 Concentration Highway A or B.** When this bit is set, highway B is selected for serial reception; when this bit is cleared, highway A is chosen.
R13	7	RB2EN	**Receive B2 Reception Enable.** When this bit is set, B2-channel information is received on the chosen highway and time slot; when this bit is cleared, no B2 reception occurs, the time slot is ignored, and all 1s are transmitted to the TE in the B2 fields.

Table 3. Register Bit Definitions (Continued)

Name	Bit	Symbol	Name/Function
R14	0—5	RDTS	**Receive D Time Slot.** These six bits, ranging in value from 0 to 63, define the receive time-slot number for D-channel information on the chosen highway (A or B). If RLBIT is set, the time slot is assumed to hold the two D bits in bit 1 and bit 0, and the latter bit is transmitted first onto the link. If RLBIT is cleared, the two D bits are obtained from time-slot bits 7 and 6, with the bit in position 7 passing onto the link first. In either case, the other six bits of the time slot are ignored. The value of RDTS relates to the virtual receive TDM frame.
R14	6	RDAB	**Receive D Concentration Highway A or B.** When this bit is set, highway B is selected for serial reception; when this bit is cleared, highway A is chosen.
R14	7	RDEN	**Receive D Reception Enable.** When this bit is set, D-channel information is received on the chosen highway and time slot; when this bit is cleared, no D reception occurs, the time slot is ignored, and all 1s are transmitted to the TE in the D fields.
R15	0		**Spare.**
R15	1	QSC	**Q-bits State Change.** This bit becomes active when the set of four Q bits received in a multiframe differs from the set of Q bits received in the previous superframe. QSC is set if such a change is detected, and a hardware interrupt signal may be generated (depending on the state of the QSCM and MASK bits in R7). Note that this interrupt can occur only once per superframe (a maximum of once per 20 link frames).
R15	2	SOM	**Start of Multiframe.** The SOM bit activates before UNITS transmits the framing (F) bit of a link frame that begins a multiframing interval to the TE. This interrupt is not enabled unless the transmit signal field in R7 is programmed to INFO 2 or INFO 4. SOM is set when a superframe begins, and a hardware interrupt signal may be generated (depending on the state of the SOMM and MASK bits in R7). Note that this interrupt can occur only on superframe boundaries (once per 20 link frames).*
R15	3	RSC	**Receive Signal Change.** This bit flags a change in the received line information pattern (INFO state) to either INFO 0, 1, or 3 from one of the other two INFO states. RSC is set when such a change occurs, and a hardware interrupt signal may be generated (depending on the state of the RSCM and MASK bits in R7).

* If the transmit signal field in R7 is set to INFO 2 during a soft reset, the first SOM interrupt when the chip resumes operation occurs one FS period earlier than normal. All subsequent SOM interrupts appear at the correct link-frame boundary.

Table 3. Register Bit Definitions (Continued)

Name	Bit	Symbol	Name/Function
R15	4,5	RS	**Receive Signal.** These two bits specify the line information pattern (INFO state) currently being received. They are not affected by the RSCM bit in R7 and continually reflect one of the following status conditions: **b1—b0** **Meaning** 00 INFO 0 – No synchronization achieved and less than four zeros received per link frame 01 INFO 1 – No synchronization achieved and at least four zeros received per link frame 10 INFO 3 – Synchronization achieved** 11 Illegal encoding – not used
R15	6	LERR	**Link Error.** The LERR bit becomes valid when one or more link errors are detected on the 4-wire interface. Such link errors consist of either missing or extra bipolar violations that cause no loss of framing. If and while framing is lost, LERR is disabled so that it cannot be set, although a logic 1 state existing prior to the loss of framing is maintained. LERR is set when a link error is detected, and a hardware interrupt signal may be generated (depending on the state of the LERRM and MASK bits in R7).
R15	7	INT	**Interrupt.** This bit is a logical OR of the QSC, SOM, RSC, and LERR bits. It can be used when the controlling microprocessor prefers to poll interrupts rather than use the hardware interrupt. It is set whenever one of the four interrupt conditions occurs. If the MASK bit in R7 is cleared, a hardware interrupt signal is generated; if the MASK bit is set, no hardware interrupt occurs.

** The recognition of INFO 3 is the sole indicator of synchronization, so changes to and from INFO 3 in the RS field also mark achievement or loss of framing.

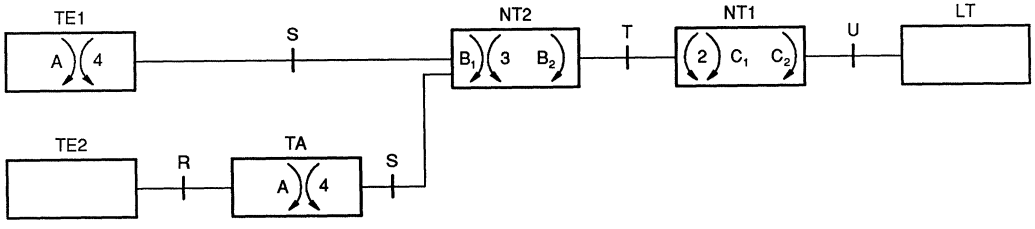


Figure 5. CCITT I.430 Loopback Configurations

Table 4. T7252A UNITS Register Bit Polarities and Reset States

Name	Main Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R0	Highway configuration transmit	0=r;1=f FE	spare	spare	0=h;1=l XLBIT	0=f;1=r XCE	XBOFF2—0		
R1	Highway configuration receive	0=a;1=f FT	spare	spare	0=h;1=l RLBIT	0=f;1=r RCE	RBOFF2—0		
R2	Time-slot offset transmit	0=o;1=r RST	0=u;1=d PWRUD	XTSOFF5—0					
R3	Time-slot offset receive	0=c;1=o OPEN	0=n;1=t TEST	RTSOFF5—0					
R4	Loopback and exchange control	XXCHNG1—0		RXCHNG1—0		LOOPBCK3—0			
R5	Transmit byte exchange	XXBYTE							
R6	Receive byte exchange	RXBYTE							
R7	Interrupt and TS control	1=d;0=e MASK	0=e;1=d LERRM	TS1—0		0=e;1=d RSCM	0=e;1=d SOMM	0=e;1=d QSCM	spare
R8	S and Q Bits	S3—0				Q3—0			
R9	Transmit B1 time slot	0=d;1=e XB1A	0=d;1=e XB1B	XB1TS5—0					
R10	Transmit B2 time slot	0=d;1=e XB2A	0=d;1=e XB2B	XB2TS5—0					
R11	Transmit D time slot	0=d;1=e XDA	0=d;1=e XDB	XDTS5—0					
R12	Receive B1 time slot	0=d;1=e RB1EN	0=a;1=b RB1AB	RB1TS5—0					
R13	Receive B2 time slot	0=d;1=e RB2EN	0=a;1=b RB2AB	RB2TS5—0					
R14	Receive D time slot	0=d;1=e RDEN	0=a;1=b RDAB	RDTS5—0					
R15	Interrupt status	0=n;1=y INT	0=n;1=y LERR	RS1—0		0=n;1=y RSC	0=n;1=y SOM	0=n;1=y QSC	spare

The initial or reset state of each field is 0, except for the MASK bit in R7, which is set on external reset, and R5, which is not guaranteed. The following is a key to the polarity abbreviations:

a – adaptive or bus A
b – bus B
c – closed
d – down or disabled
e – enabled
f – falling or fixed
h – high bit in channel
l – low bit in channel
n – normal or no
o – operational or open
r – rising or reset
t – test
u – up
y – yes

Functional Description

Basic Access Operation

The AT&T T7252A UNITS transfers the subscriber line 2B+D information as a 192-kb/s full-duplex signal grouped into frames of 48 bits with a period of 250 μs. Thirty-six of the forty-eight bits sent in each direction convey user information (two 8-bit occurrences of each of the two B channels and four D-channel bits). The remaining 12 bits per frame are used for framing, control, dc balance, and maintenance. The two frame structures are shown in Figure 6.

In the bit stream transmitted from the terminal endpoint (TE) to the network termination (NT), four bits are used for framing (F and FA, each with a dc balancing bit, L), eight L bits are used to balance the 32 B-channel bits, and four bits are D-channel bits. Conversely, for the NT-to-TE transmission, four bits (F with balancing bit L, FA, and N) are used for framing, one M bit for marking the start of a 20-frame superframe, four E bits for forming an echo channel for retransmission of the D-channel bits received from the terminal, one L bit for balancing the contents of the entire frame, and one bit for indicating when bit synchronization is achieved between TE and NT as part of the INFO 4 state. One S bit remains as a spare channel. With a zero-length subscriber loop, the TE-to-NT stream is (A = 1) delayed by two bit times relative to NT-to-TE frames.

The alternate space inversion (AS1) line code used for the 2B+D transmission is also known as pseudo-ternary, since a logical 1, or mark, is represented by the absence of a pulse, and a logical 0, or space, is represented by an alternately positive or negative pulse.* The framing procedure uses line-code violations to establish synchronization. Since the last space of any frame is a positive pulse with respect to the transmitter, and because the F bit is also defined to be a positive pulse (see Figure 6), the first bit of each frame represents a coding violation. In addition, the second bit of each frame, a balance bit, is a negative pulse, and the next space in the frame is forced to be negative, causing another violation. All other pulses follow the alternating convention. In the TE-to-NT direction, in at least four of five frames, this second violation occurs within 13 bits of the F bit. The T7252A UNITS continues transmitting when it loses synchronization at the receiver.

The reason for the variable distribution of the second line-code violation in the TE-to-NT stream lies in the technique used for multiframing. Every 20 frames, the "M" bit in the NT-to-TE direction is set, with the FA bit being set every five frames. The TE recognizes these states and, in returned frames immediately corresponding to those in which the NT set the FA bit, replaces the FA bit it sends to the NT with a Q bit (Q1—Q4). Q1 is returned for each frame in which both the M and FA bits were set by the NT, with Q2—Q4 following at 5-frame intervals.

* The terms *positive* and *negative* do not necessarily imply voltage polarity, since wiring integrity from the NT to the TE(s) is not required.

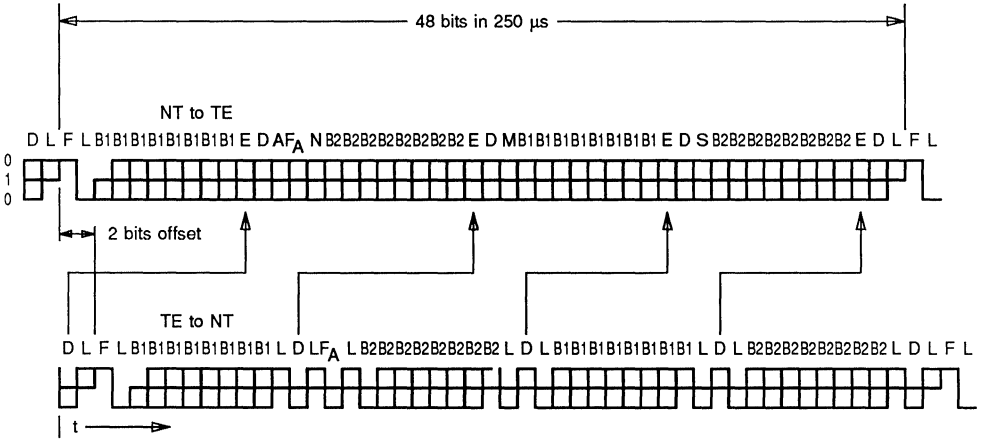


Figure 6. ISDN Basic Access Physical Level Frame Structure

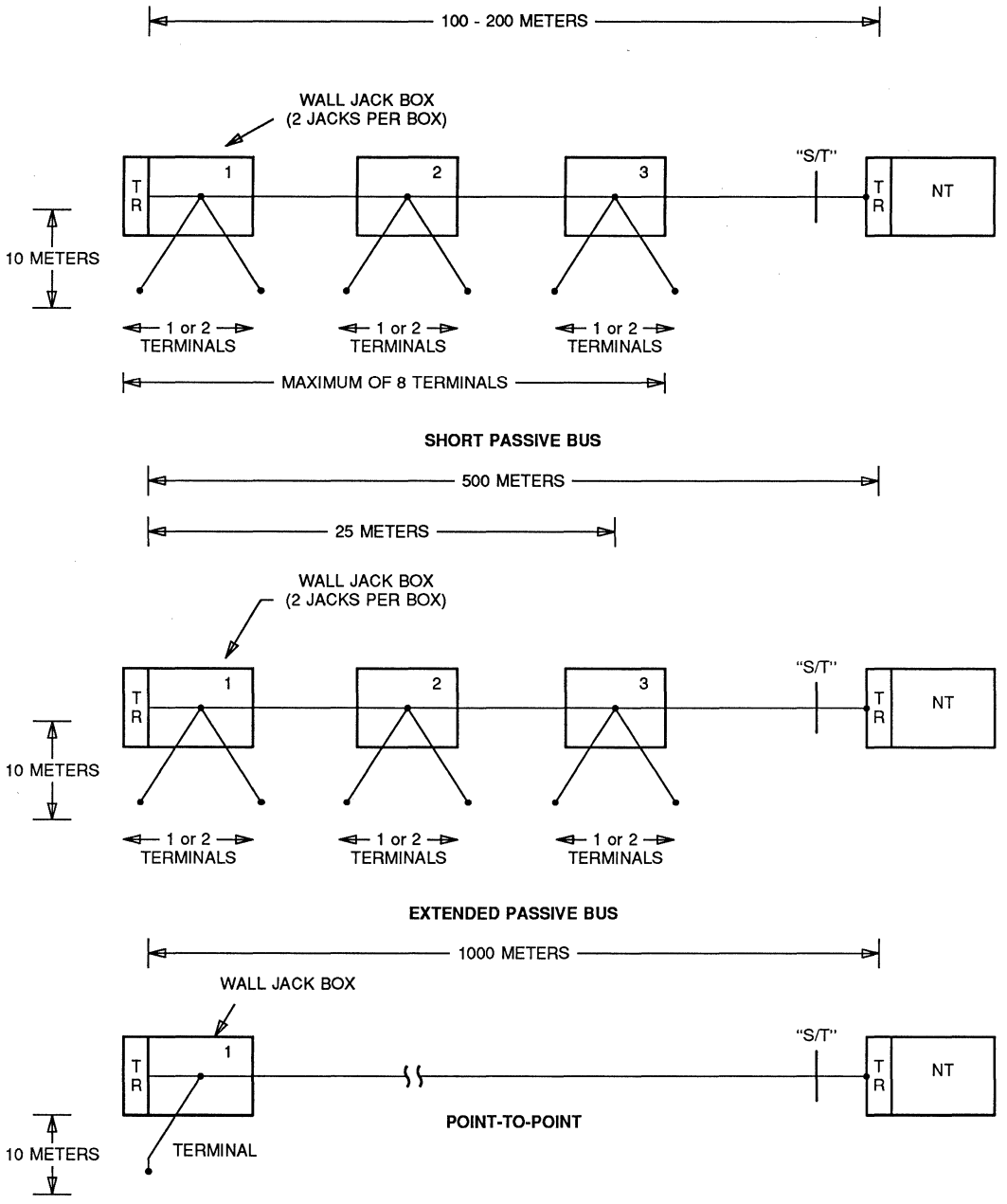


Figure 7. Representative Basic Access Bus Configurations Supported by the T7252A UNITS

Table 5. Definition of INFO State Signals

Signals from NT to TE		Signals from TE to NT	
INFO 0	No signal	INFO 0	No signal
		INFO 1	A continuous signal with the following pattern: Positive ZERO, negative ZERO, six ONEs (see Figure 8)
INFO 2	Frame with all bits of B, D, and D-echo channels set to binary ZERO; bit A set to binary ZERO; N and L bits set according to the normal coding rules		
INFO 4	Frames with operational data on B, D, and D-echo channels; Bit A set to binary ONE	INFO 3	Synchronized frames with operational data on B and D channels

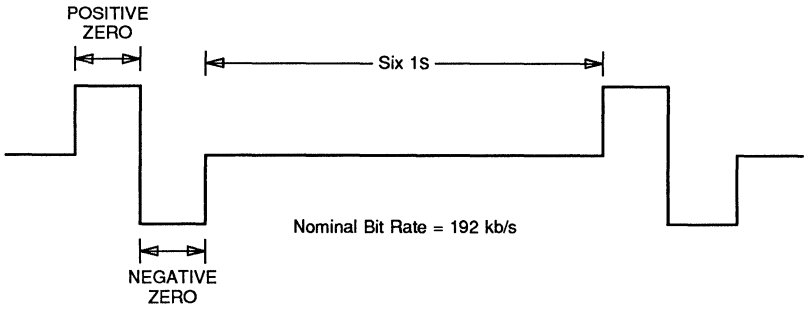


Figure 8. INFO 1 State Signal

Line Transceiver

The transceiver for the 4-wire I.430 interface consists of two sections with separate power and grounds. The line transmitter and the line receiver are essentially stand-alone designs, except for limited sharing of timing and control circuits. Both expect to interact with external 2.5:1 transformers.

The line transmitter is a voltage-limited current source that fully conforms to I.430 specifications. New transmit link frames begin shortly after the reception of a frame synchronization (FS) pulse, and the individual bits are timed by an internal 192-kHz clock derived from the master clock supplied on the XTAL1/XTAL2 pins. Table 6 summarizes the mechanism used by the transmitter to send the ASI code through the transmit transformer. ASI is a differential strategy, with positive and negative rails connecting to the transformer. Current flows through the transformer only when there is a voltage difference on the two rails. As shown in the table, when a logic 1 (mark) is being sent, meaning that no current is desired, both rails go to a 3-stated condition. When a positive ZERO (space) is transmitted, the positive rail rises to a logic high, and the negative rail is grounded. The reverse occurs for a negative ZERO. Both rails are never driven to the same logic value.

The line receiver is a more complex circuit. Since the link length to the subscriber(s) is variable, as is the number of TEs on the loop, the receiver must be sufficiently intelligent to adjust for widely varying input waveforms. The T7252A UNITS receiver is designed to use a single adaptive timing mode to synchronize to all signals conforming to the I.430 templates. All link configurations, including extended passive bus, short passive bus, and point-to-point are supported with this one mode. The adaptive timing circuit can also operate with round-trip cable delays of 0 μs to 42 μs. This means that if the line transmitter and the line receiver are directly connected externally in an immediate loopback configuration, the receiver can extract the 2B+D information correctly from the transmitted stream. Alternatively, designers desiring a fixed timing mode for configurations with a total round-trip cable delay of approximately 2 μs can invoke this fixed strategy through the register set. When the T7252A UNITS uses fixed timing, the input stream is sampled 4.2 μs after the leading edge of each 192-kHz transmit bit interval.

The T7252A UNITS receiver automatically adjusts the voltage threshold used to determine reception of a space. When ten consecutive pulses of at least 500 mVp arrive on the positive lead of the receiver, the sampling threshold is raised to 225 mV. If, after the threshold is increased, two consecutive pulses on the positive lead fall below 500 mV, the sampling level is returned to 160 mV, which is also the default value.

The interval required for the receiver to synchronize to the received stream is approximately 5 to 60 link frames (1.25 to 15 ms). The receiver can achieve framing only when the INFO 3 pattern appears on the link. A 3-frame delay is provided when recognizing new line INFO states. INFO 1 is identified by receipt of at least four 0s per frame with no frame synchronization. INFO 3 is indicated when the receiver is able to achieve framing. INFO 0 is reported for all other cases.

Table 6. Transmission Code

Positive Rail	Negative Rail	Current	Logic
Z*	Z*	0	1
1	0	+1	0
0	1	–1	0

* Z = 3-state condition.

Concentration Highway

Port boards in a digital switch generally share a common architecture (Figure 9). Depending on the particular port and switch, a control block may route information channels either to a circuit switch or a packet switch. On the other side of the port board, subscriber lines are terminated by line interfaces. A synchronous (TDM) highway is a convenient way to merge and pass information between the line interfaces and the switch. To distinguish the TDM highway supported by the T7252A UNITS from other TDM buses within the switch, this local TDM bus is called the concentration highway.

The concentration highway is defined as a data-transport interface used to carry bit streams back and forth between T7252A UNITS devices and the switch. It has the following characteristics:

- Two pairs of transmit and receive paths to carry channels in 8-bit time slots.
- Programmable definition of highways through offset and clock-edge options.
- An 8-kHz framing signal to synchronize each direction of data flow.
- A flexible number of time slots in each 125-μs frame (for example, 4 time slots with a 256-kHz clock, 32 time slots with a 2.048-MHz clock, or 64 time slots with a 4.096-MHz clock).
- Arbitrary assignment and grouping of time slots for higher bandwidth applications.
- Ability to merge transmit and receive highways for direct transfer between multiple T7252A UNITS.
- Compatible with Intel and AMD PCM highways.

Data is transmitted (DX) or received (DR) on one of two transport groups: A or B. The user-supplied clock rate (CLKXR) determines the number of time slots on the transmit or receive paths. Individual time slots are referenced to the frame synchronization (FS) pulse. Time-slot control signals ($\overline{\text{TSCA}}$, $\overline{\text{TSCB}}$) can be used to enable optional external buffers to drive the DXA or DXB output lines.

T7252A UNITS allows the user to control the definition of the concentration highway completely, including the phase of the transmit and receive streams relative to the framing strobe, FS. Each path can be independently configured in terms of bit and time-slot offsets and the clock edges used. After the positive frame pulse is detected on the selected clock edge, the first information bit to be sent in a concentration highway frame (as adjusted by the bit and time-slot offsets) immediately follows on the clock edge chosen for data transmission. Figure 10 gives an example of how this flexibility can be used to adapt the concentration highway to any desired TDM architecture.

Although the concentration highway can be reduced to a single dedicated bus per chip, more common applications place multiple devices on shared highways. In such cases, the recommendation in Table 1 for pull-up resistors on XTAL1, CLKXR, DRA, DRB, DXA, and DXB shrinks to one pull-up resistor for each bused signal (data or clock), not each device pin.

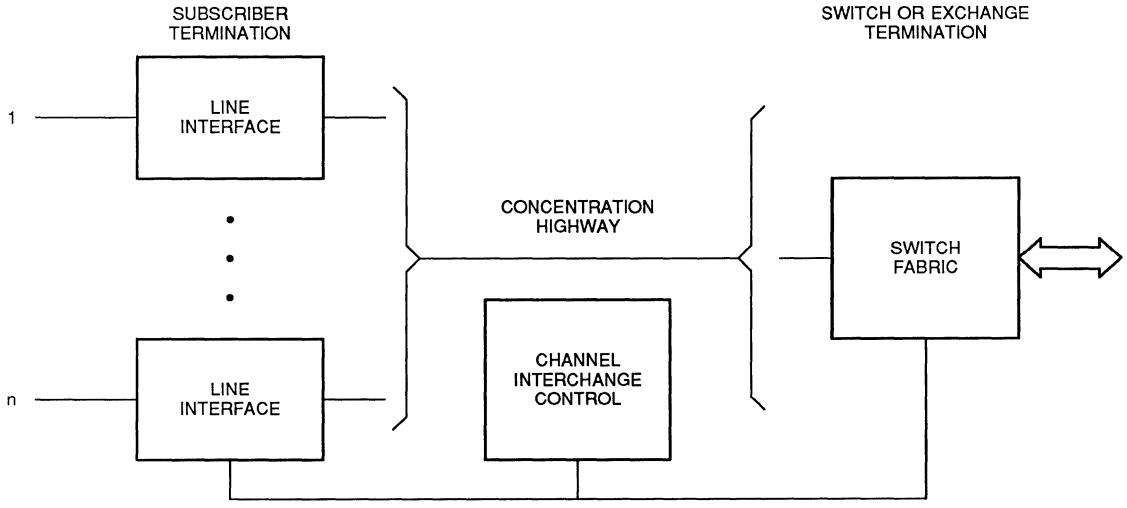
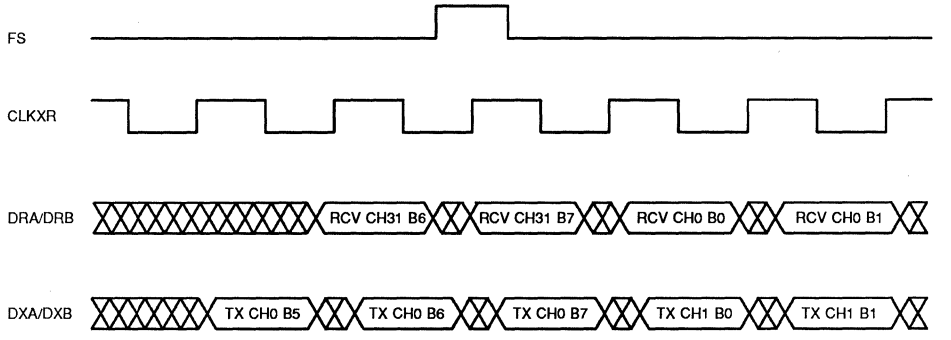


Figure 9. Generic Port Board Architecture in a Digital Switch



TX = Transmit RCV = Receive CH = Channel B = Bit

Figure 10. Sample Concentration Highway Configuration Using Offsets

Applications

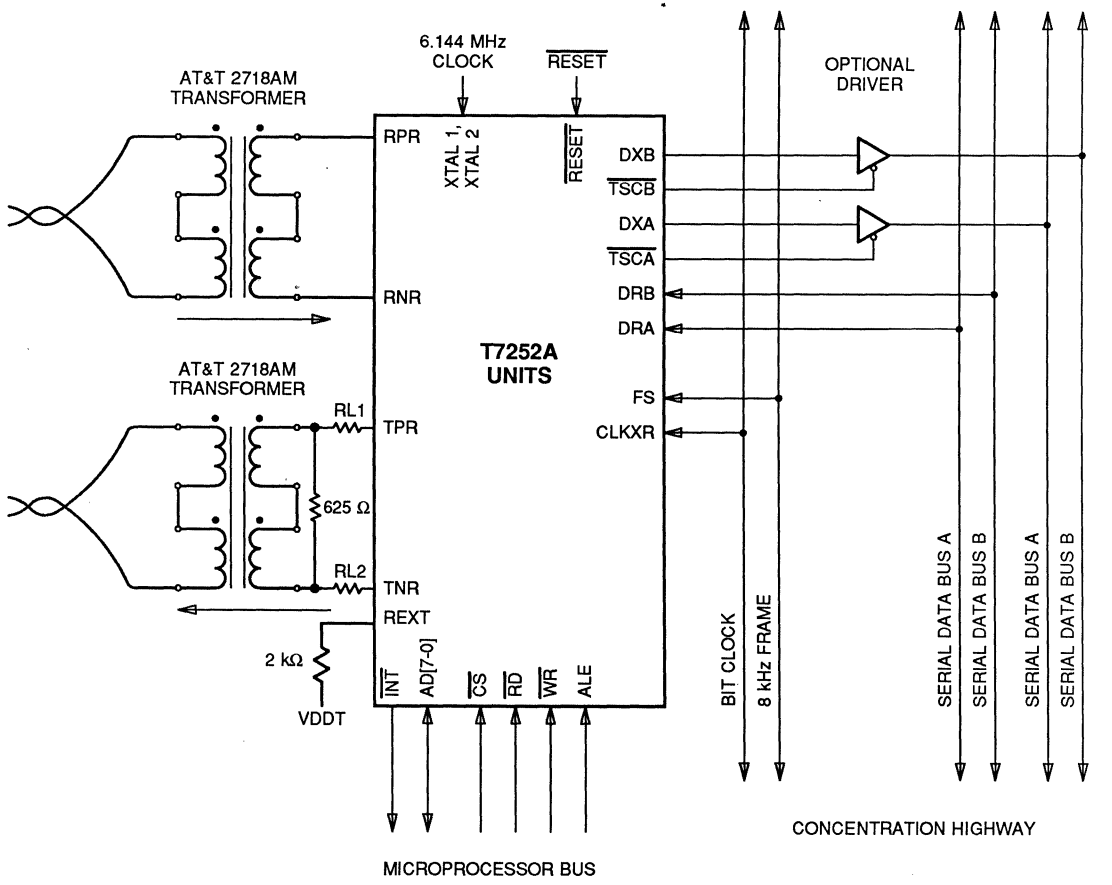


Figure 11. The T7252A UNITS Chip with Its Key Interfaces

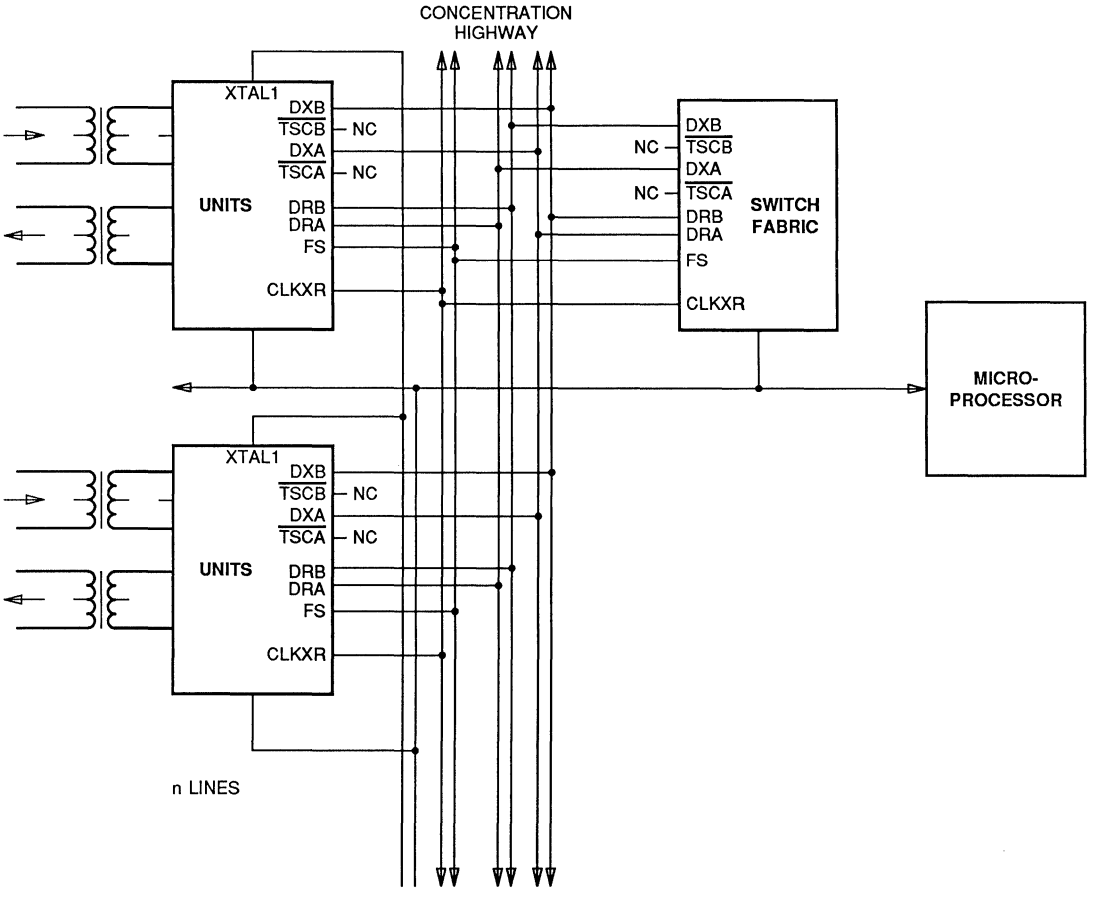


Figure 12. Concept Diagram to Connect T7252A UNITS Devices via the Concentration Highway to a Switch Fabric

Pseudo-SLD Operation

Intel's subscriber line datalink (SLD) interface offers a half-duplex, 512-kb/s, 3-lead communication scheme. The T7252A UNITS represents the slave or downstream partner in a conversation, receiving four 8-bit time slots from the master in the first half of the SLD frame, and then transmitting four time slots to the master in the second half of the frame. This technique provides 256 kb/s in each direction, organized as four channels (B1, B2, control, and signaling, in that order). The three leads normally used by SLD interfaces are:

- Serially linked data (SLD) – the 512-kb/s bi-directional data lead, clocked by SCL. SLD data is updated on the rising edge of SCL and latched on its falling edge, with the most significant bit being transmitted first
- Subscriber clock (SCL) – a 33% or 50% duty-cycle clock supplied by the master
- Subscriber direction (SDIR) – an 8-kHz signal from the master controlling frame synchronization and data direction.

The operation of the T7252A UNITS as an SLD slave is shown in Figure 13. The SLD lead from the master is split into one concentration highway transmit pin and a receive pin, with SCL connecting to CLKXR and SDIR to FS. The use of highway A for transmission and highway B for reception is arbitrary. The B1 and B2 channels are received from the master in the first two concentration highway time slots. The T7252A UNITS transmits its B1 and B2 bytes in time-slots 4 and 5. The D-channel bits can be obtained from bits 1 and 0 in the S channel, although D-channel information is better passed via the data exchange registers, R5 and R6, in the T7252A UNITS register set.

The control channel and the remainder of the signaling channel are ignored. The T7252A UNITS is not fully compatible with SLD control and signaling bit definitions.

The suggested register assignments for the SLD mode are given in Table 7.

The following list summarizes the suggested operation of the T7252A UNITS in the SLD mode:

- CLKXR = 512 kHz for eight time slots
- Concentration highway replicated eight times for eight lines
- SLD control and service channels (time-slots 2 and 3) not necessary and not interpreted by the T7252A UNITS
- D-channel access available through the microprocessor interface
- Two out of eight time slots in each direction used for B1 and B2.

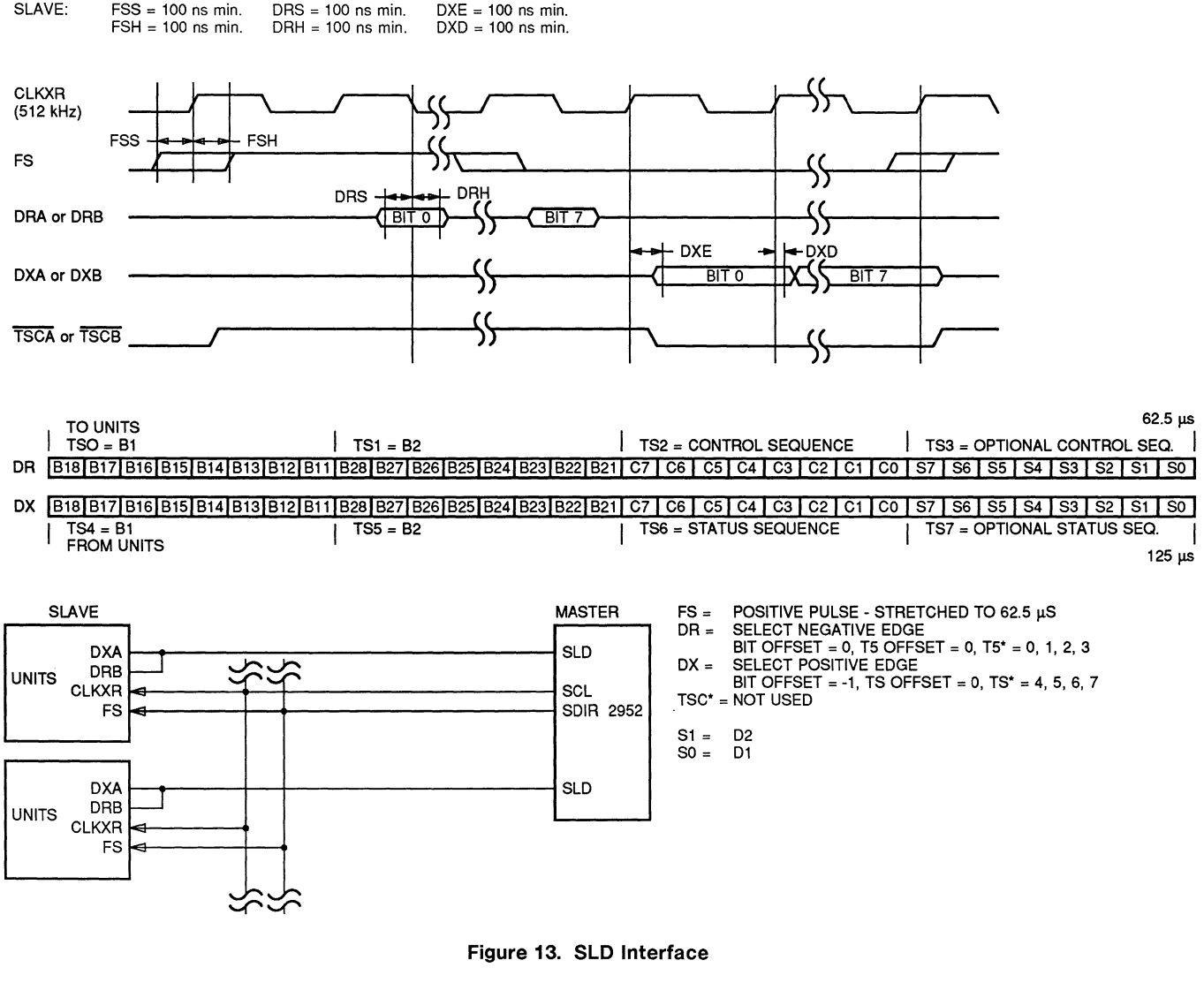


Figure 13. SLD Interface

Table 7. Suggested T7252A UNITS Register Bit Assignments for SLD Mode

Name	Main Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R0	Highway configuration transmit	1 FE	spare	spare	0 XLBIT	1 XCE	−1 XBOFF2—0		
R1	Highway configuration receive	0 FT	spare	spare	0 RLBIT	0 RCE	0 RBOFF2—0		
R2	Time slot offset transmit	0 RST	0 PWRUD	0 XTSOFF5—0					
R3	Time slot offset receive	1 OPEN	0 TEST	0 RTSOFF5—0					
R4	Loopback and exchange control	11 XXCHNG1—0		11 RXCHNG1—0		1111 LOOPBCK3—0			
R5	Transmit byte exchange	N/A XXBYTE							
R6	Receive byte exchange	N/A RXBYTE							
R7	Interrupt and TS control	0 MASK	0 LERRM	any TS1—0		0 RSCM	0 SOMM	0 QSCM	spare
R8	S and Q bits	N/A S3—0				N/A Q3—0			
R9	Transmit B1 time slot	1 XB1A	0 XB1B	4 XB1TS5—0					
R10	Transmit B2 time slot	1 XB2A	0 XB2B	5 XB2TS5—0					
R11	Transmit D time slot	0 XDA	0 XDB	0 XDTS5—0					
R12	Receive B1 time slot	1 RB1EN	1 RB1AB	0 RB1TS5—0					
R13	Receive B2 time slot	1 RB2EN	1 RB2AB	1 RB2TS5—0					
R14	Receive D time slot	0 RDEN	1 RDAB	0 RDTS5—0					
R15	Interrupt status	N/A INT	N/A LERR	N/A RS1—0		N/A RSC	N/A SOM	N/A QSC	spare

Characteristics — Preliminary

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5 %, V_{SSR} = 0 V; typical values at T_A = 25 °C, V_{DD} = 5 V

Table 8. DC — Power Supply (Average Over 1 ms)

Parameter	Sym	Min	Typ	Max	Unit
Power supply current:	I_{CC}	—	—	—	—
power down	—	—	4.4	5	mA
normal (quiescent INFO0)	—	—	11	—	mA
normal (active INFO2)	—	—	17	20	mA
Digital ground	V_{SSR}	–0.1	—	0.1	V

Table 9. DC — Digital

Parameter	Sym	Min	Typ	Max	Unit
Input current	I_I	—	—	±10	μA
Output current:*					
low	I_{OL}	—	5.1	—	mA
		—	2.9	—	mA
high	I_{OH}	—	–7.4	—	mA
		—	–4.5	—	mA
Input voltage:					
low	V_{IL}	–.3	—	.8	V
high	V_{IH}	2	—	V_{DD} + .3	V
Output voltage:**					
low	V_{OL}	—	—	.4	V
high	V_{OH}	2.4	—	—	V
Input capacitance	C_I	—	—	4	pF
Output capacitance	C_O	—	—	5	pF

* For pins DXA, DXB, AD0—7, $\overline{TSCA}$, $\overline{TSCB}$, $\overline{INT}$.
** The given output voltages are guaranteed at a maximum of 80% of the typical output current values.

Table 10. DC — Analog

Parameter	Sym	Min	Typ	Max	Unit	Operating Conditions
Receive differential space (zero) voltage*	VRDS	200	—	3000	mV	—
Threshold:**						
low	VTL	—	160	—	mVp	—
high	VTH	—	225	—	mVp	—
switching	VTS	—	500	—	mVp	RPR – RNR
Transmit differential space (zero) voltage	VTDS	1688 —	1875 —	2062 3000	mV mV	RL = 50 RL = 2500
Impedance per pin	ZIO	—	60	—	kΩ	—
Capacitance per pin	CIO	—	10	—	pF	—
Resistance between TPR and TNR	RPN	200	—	—	Ω	Transmitter 3-stated
Capacitance between TPR and TNR	CPN	—	20	—	pF	—
Output current	IAO	5.4	6	6.6	mA	RL = 312.5

* Measured on the secondary (device or 2.5) side of the required 2.5:1 transformer.
** Measured on the primary (line or 1) side of the required 2.5:1 transformer.

Table 11. DC — XTAL1, XTAL2

Description	Min	Typ	Max	Unit
Input voltage:				
high	4	—	—	V
low	—	—	.4	V
External capacitive load on crystal (i.e., 56 pF to ground on each leg of crystal)	—	30	—	pF

Maximum Ratings

Case operating temperature (T_C) ..... 0 to 85 °C
Storage temperature (T_{STG}) range ..... –55 to +125 °C

When V_{DD} relative to V_{SS} is $\leq$ +6.1 V:
voltage on any pin (digital – low, V_{DL}) ..... V_{SS} – .3 V
voltage on any pin (digital – high, V_{DH}) ..... V_{DD} + .3 V

When V_{DD} relative to V_{SS} is > +6.1 V:
voltage on any pin (digital – low, V_{DL}) ..... > V_{SS}
voltage on any pin (digital – high, V_{DH}) ..... < V_{DD}

Maximum V_{DD} relative to V_{SS} (V_{DS}) ..... +7 V
Power dissipation (PD) ..... 500 mW

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human body model (HBM) and a charged device model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

Human Body Model ESD Threshold	
Device	**Voltage**
T7252A	> 900 V

Timing Characteristics

Table 12. AC — Concentration Highway

Symbol	Description	Min	Max	Unit
tCKLCKL	CLKXR period	.244	3.9	μs
—	CLKXR duty cycle[1]	30	70	%
—	CLKXR rise/fall time[2]	—	20	ns
tFSHCKH	Frame sync set-up time	50	CLKXRT – 30	ns
tCKHFSH	Frame sync hold time	30	CLKXRT – 50	ns
—	Frame sync high[3]	0.08	125 – tCKLCKL	ns
—	Frame sync 8-kHz stability	–100	+100	ppm
—	Frame sync peak-to-peak jitter	0	160	ns
tCKLTSL	Delay to $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$[4, 5] falling edge	—	NT + 70	ns
tCKLTSH	Delay to $\overline{\text{TSCA}}$[4] or $\overline{\text{TSCB}}$ 3-state	(N + 8)T + 5	—	ns
tCKLDXV	Data transmit enable time[5]	—	60	ns
tCKHDXV	Data transmit hold time	5	—	ns
tDRVCKH	Data receive set-up time	25	—	ns
tCKHDRV	Data receive hold time	5	—	ns

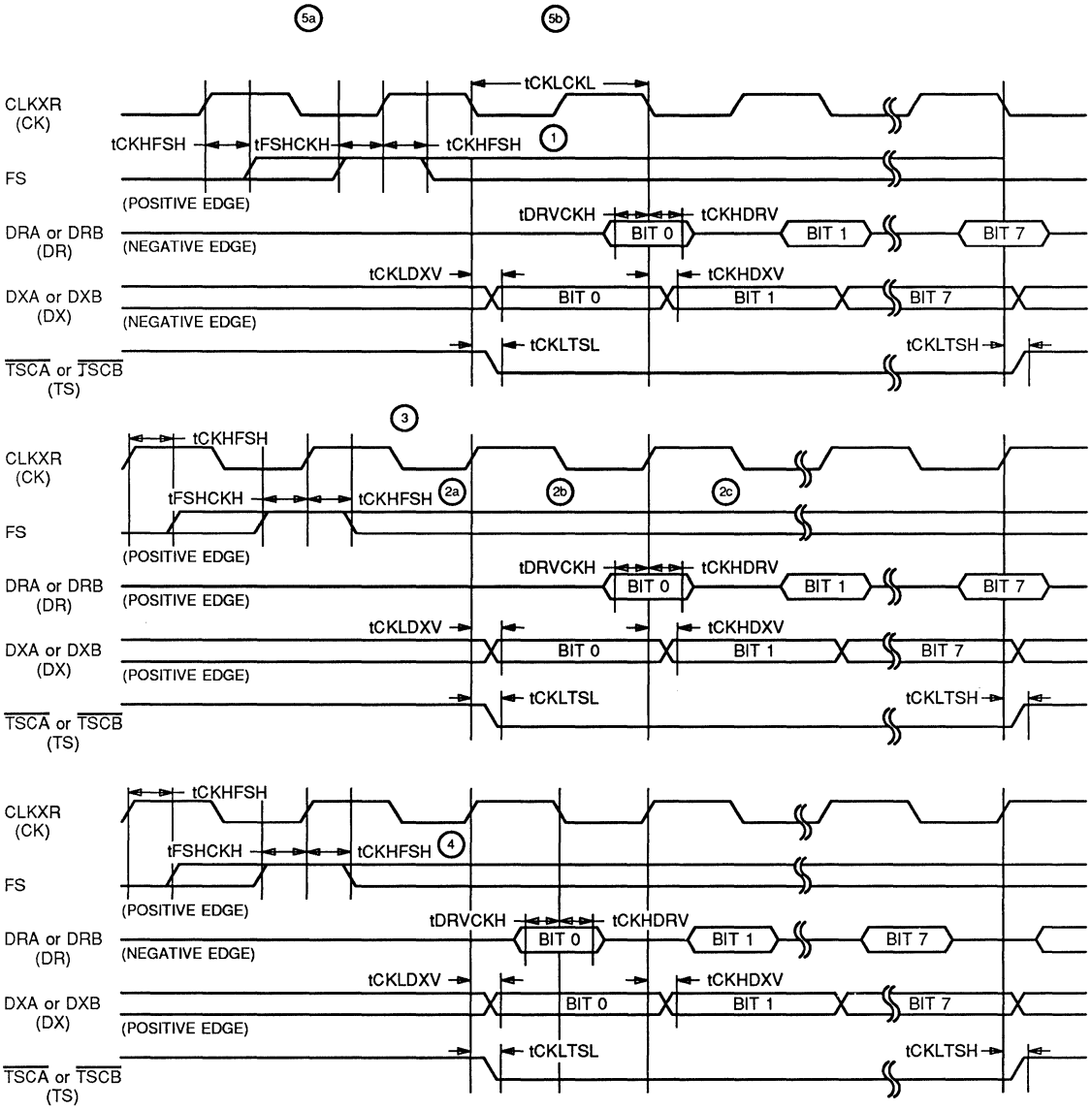
[1] The other specifications listed in this table must also be met for the duty cycle chosen.
[2] tCLKXR must rise quickly to greater than 4 V. A pull-up resistor is recommended when this signal is heavily loaded.
[3] An FS pulse can span many CLKXR periods. Only the first selected CLKXR edge after a rising FS edge marks a frame boundary; all subsequent CLKXR edges while the given FS pulse is high have no effect on frame detection.
[4] N = total offset due to time-slot and bit offsets; T = one CLKXR bit period.
[5] 50-pF load.

Table 13. Derating Factors for Propagation Delays

Symbol	Added Delay per 50-pF Loading Increment	Unit
tCKHTSL	30	ns
tCKLDXV	20	ns

Table 14. AC — XTAL1, XTAL2

Description	Min	Typ	Max	Unit
6.144-MHz stability	–250	—	250	ppm
Duty cycle	40	—	60	%
Rise or fall time	—	—	10	ns



Notes:
1. Edge if DR* on positive edge.
2a—c. Edges if FS on negative edge, DX*/TSC* on negative edge, and DR* on negative edge, respectively.
3,4. Edge if FS on negative edge.
5a—b. Edge if FS on negative edge and DR* on positive edge, respectively.
6. Bits D through 7 are shown with zero offsets (DRA, DRB, DXA, DXB).

Figure 14. Concentration Highway Data Transport Timing

AC — Microprocessor Interface

Symbol	Description	Min	Typ	Max	Unit
tAVCSL	Address valid to ALE or $\overline{CS}$ low	20	—	—	ns
tCSLAV	Address hold after ALE or $\overline{CS}$ low	30	—	—	ns
tCSHCSL	ALE or $\overline{CS}$ pulse width high	20	—	—	ns
tWRLWRH	$\overline{WR}$ pulse width	100	—	—	ns
tAVWRH	Data set-up to $\overline{WR}$ high	20	—	—	ns
tWRHAV	Data hold after $\overline{WR}$ high	30	—	—	ns
—	Cycle delay after $\overline{WR}$ high	488	—	—	ns
tRDLRDH	$\overline{RD}$ pulse width	170	—	—	ns
tRDLDV	$\overline{RD}$ low to valid data*	—	—	80	ns
tRDHDV	Data float after $\overline{RD}$ high	0	—	—	ns
tRDHDX	Data hold after $\overline{RD}$ high	0	—	—	ns
tCSLWRL	ALE or $\overline{CS}$ low to $\overline{WR}$ low	50	—	—	ns
tCSLRDL	ALE or $\overline{CS}$ low to $\overline{RD}$ low	100	—	—	ns
tWRHCSH	$\overline{RD}$ or $\overline{WR}$ high to ALE or $\overline{CS}$ high	43	—	—	ns
—	FS high to $\overline{INT}$ low**	100	—	370	ns

* 50-pF load; derating factor is 13 ns of added delay per 50-pF increment.
** 50-pF load; derating factor is 30 ns of added delay per 50-pF increment.

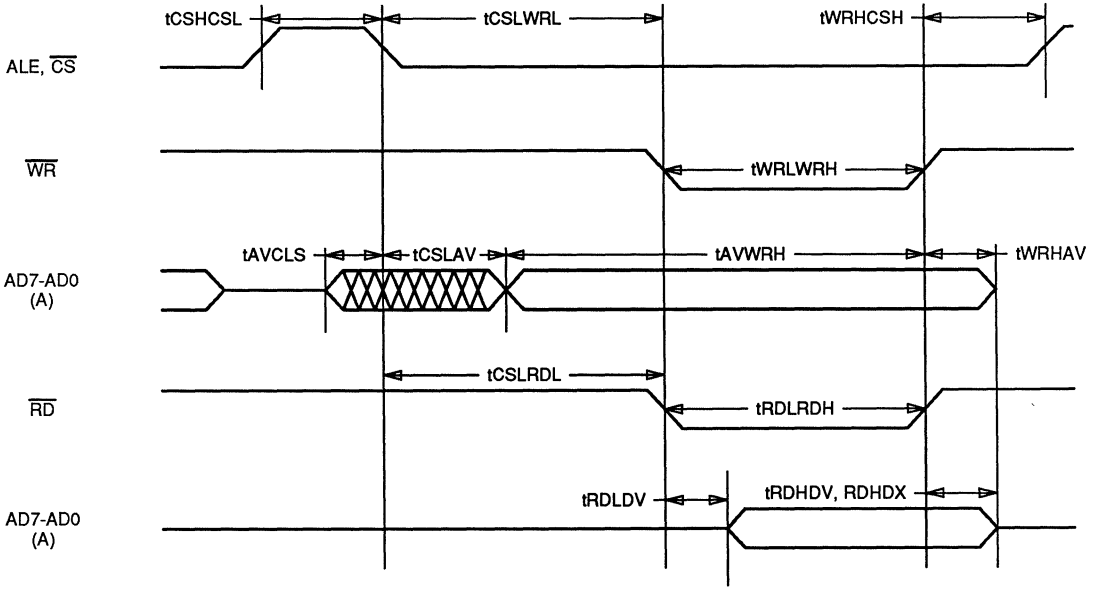


Figure 15. Microprocessor Interface Timing

AC — $\overline{\text{RESET}}$ Pulse

Description	Min	Unit
$\overline{\text{RESET}}$ pulse width low	100	ns

AC — Analog Transmitter

Description	Min	Typ	Max	Unit	Comments
Impedance in TPR, TNR loop	180	200	220	Ω	$RL_1 + RL_2 + R_{TRANSFORMER}$ (see Figure 11)
Terminating resistor (device side)	594	625	656	Ω	—
Load time constant	—	—	.5	μs	R_L = 300 Ω, C_L = 1500 pF
Damping time constant	—	—	1.5	μs	—
Transmit space (zero) rise time	—	—	400	ns	—

Note: Analog parameters not specified conform to or exceed the requirements of CCITT Recommendation I.430 and the Draft US Specification (November 1986).

T7260 and T7261 ISDN U-Interface Basic Access Transceiver Chip Set

Features

- U-interface for 2-wire operation
- Pin-selectable for central office (CO) switch and network termination (NT) applications
- 144-kb/s full-duplex using echo cancellation (EC)
- Alternate mark inversion (AMI) line code
- Digital I/O via the AT&T K-interface
- On-chip balanced line driver
- Balanced continuous time filters
- Adaptive equalization and automatic gain control (AGC)
- Power-down option
- LED driver to signal loss of framing
- Decision feedback equalizer (DFE) for increased tolerance to bridged taps
- EC and DFE reset pins for external power-up reset

Description

The AT&T T7260 and T7261 ISDN U-Interface Basic Access Transceiver (U-BAT) chip set is a pair of silicon integrated circuits providing full-duplex 2B+D communication on a 2-wire digital subscriber loop. The T7260 and T7261 devices perform line transceiver functions at either the central office (CO) switch or at the network termination (NT) and operate at a data transfer rate of 144 kb/s. Adaptive echo cancellation and equalization techniques provide a loss budget of 38 dB. The T7260 requires both a +5 V and –5 V supply; the T7261 requires only a 5 V supply. Both are manufactured in CMOS technology and are packaged in 44-pin plastic leaded chip carriers (PLCC).

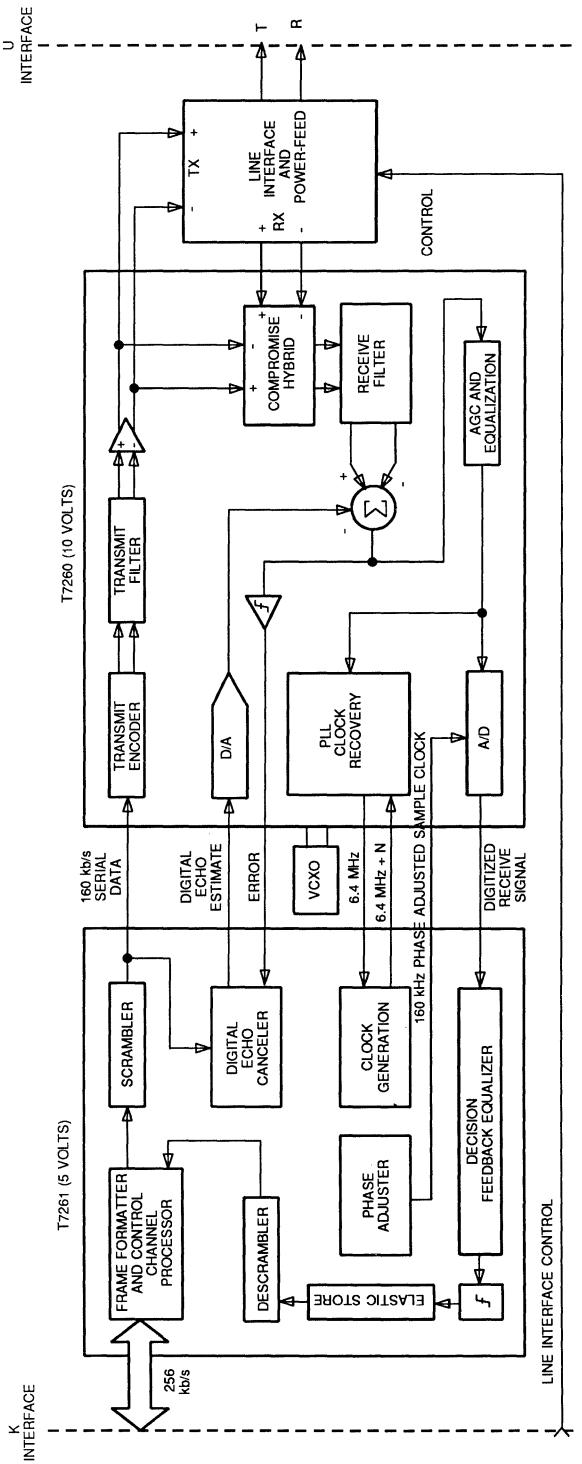


Figure 1. T7260 and T7261 Basic Access ISDN U–Interface Block Diagram

5. ISDN Primary Rate/T1

229FB Maintenance Buffer

Features

- 8-bit interface bus
- Microprocessor access to control/report streams
- Ten general-purpose latched outputs
- Two error-source latched inputs
- Preprocessing counters on facility error conditions updated by the framer
- Built-in operational testing capability
- TTL-compatible

Description

The 229FB Maintenance Buffer integrated circuit provides the microprocessor interface for the serial report and control streams of the T7229 (replaces the 229CG) or 229GB Primary Access Framer, 257AU Receive Synchronizer, and 257AL Transmit Formatter. It also processes facility alarms received from the framer and provides additional latched inputs and outputs for microprocessor use. The maintenance buffer is manufactured using depletion-mode NMOS technology, requires a single 5 V supply, and is available in a 40-pin plastic DIP.

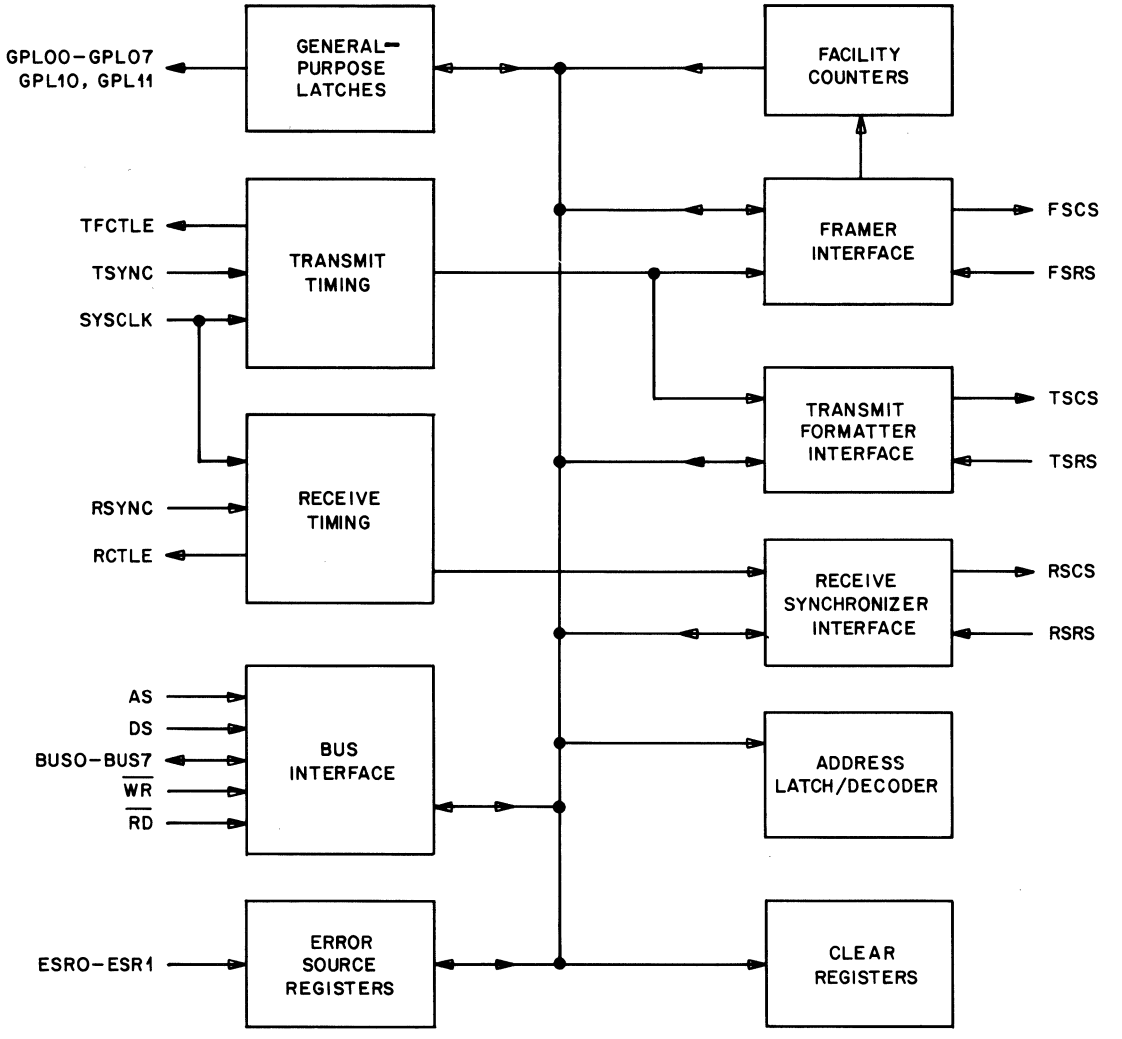
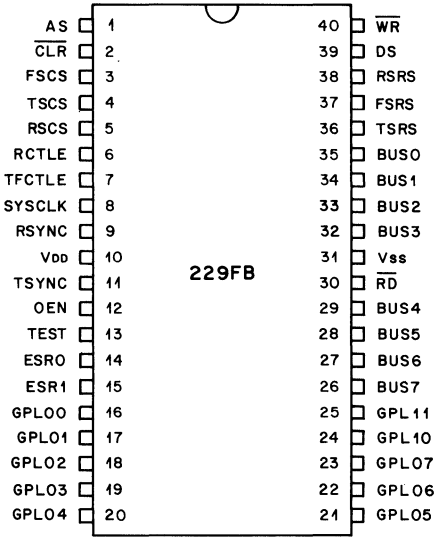


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
AS	1	$\overline{RD}$	30
BUS0—BUS3	35—32	RSCS	5
BUS4—BUS7	29—26	RSRS	38
$\overline{CLR}$	2	RSYNC	9
DS	39	SYSCLK	8
ESR0	14	TEST	13
ESR1	15	TFCTLE	7
FSCS	3	TSCS	4
FSRS	37	TSRS	36
GPL00—GPL07	16—23	TSYNC	11
GPL10	24	VDD	10
GPL11	25	VSS	31
OEN	12	$\overline{WR}$	40
RCTLE	6		

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	AS	I	**Address Select.** When high, bits BUS0—BUS7 are used as an address.
2	$\overline{CLR}$	I	**Clear.** This active-low pin clears all output registers.
3	FSCS	O	**Framer Serial Control Stream.** Microprocessor control information is output to the T7229 or 229GB Framer on this pin at a 1.024-Mb/s rate.
4	TSCS	O	**Transmit Serial Control Stream.** Microprocessor control information is output to the 257AL Transmit Formatter on this pin at a 1.024-Mb/s rate.
5	RSCS	O	**Receive Serial Control Stream.** Microprocessor control information is output to the 257AU Receive Synchronizer on this pin at a 1.024-Mb/s rate.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
6	RCTLE	O	**Receive Control Enable.** A high on this pin indicates to the 257AU Receive Synchronizer that control information is being sent on RSCS.
7	TFCTLE	O	**Transmit and Framer Control Enable.** A high on this pin indicates to the 257AL Transmit Formatter and T7229 or 229GB Framer that control information is being sent on TSCS and FSCS.
8	SYSCLK	I	**System Clock.** This is the 4.096-MHz clock input.
9	RSYNC	I	**Receive Synchronization.** 8-kHz pulse rate.
10	V_{DD}	—	**5 V Supply.**
11	TSYNC	I	**Transmit Synchronization.** 8-kHz pulse rate.
12	OEN	I	**Output Enable.** This active-high input enables all outputs except the address/data bus outputs. When low, output pins 3—7 and 16—25 are in a 3-state condition.
13	TEST	I	**Test.** Ground this pin for device operation.
14 15	ESR0 ESR1	I	**Error Source Register Bits 0 and 1.** These two inputs can be used by the microprocessor for monitoring external device status.
16 17 18 19 20 21 22 23 24 25	GPL00 GPL01 GPL02 GPL03 GPL04 GPL05 GPL06 GPL07 GPL10 GPL11	O	**General-Purpose Latch Bits.** These ten outputs can be used by the microprocessor to control various digital facility interface (DFI) functions.
26 27 28 29	BUS7 BUS6 BUS5 BUS4	I/O	**Address/Data Bus Bit 7.** **Address/Data Bus Bit 6.** **Address/Data Bus Bit 5.** **Address/Data Bus Bit 4.**
30	$\overline{RD}$	I	**Read.** After the desired register address has been written, a low pulse on this pin places the appropriate register data on the address/data bus.
31	V_{SS}	—	**Ground.**

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
32 33 34 35	BUS3 BUS2 BUS1 BUS0	I/O	**Address/Data Bus Bit 3.** **Address/Data Bus Bit 2.** **Address/Data Bus Bit 1.** **Address/Data Bus Bit 0.**
36	TSRS	I	**Transmit Formatter Serial Report Stream.** Status information from the 257AL Transmit Formatter is serially input on this pin at a 1.024-Mb/s rate.
37	FSRS	I	**Framer Serial Report Stream.** Status information from the T7229 or 229GB Framer is serially input on this pin at a 1.024-Mb/s rate.
38	RSRS	I	**Receive Synchronizer Serial Report Stream.** Status information from the 257AU Receive Synchronizer is serially input on this pin at a 1.024-Mb/s rate.
39	DS	I	**Data Select.** When high, the information on BUS0—BUS7 represents data.
40	$\overline{WR}$	I	**Write.** This active-low input is used to address and write data into the registers.

Operation

The 229FB Maintenance Buffer is part of the digital facility interface (DFI) unit that provides a flexible, multimode, line-side interface to a PBX or host computer.

Within the DFI, the 229FB Maintenance Buffer provides the interface between an on-board DFI microcomputer and the serial report and control streams of the 257AU Receive Synchronizer, 257AL Transmit Formatter, and T7229 or 229GB Framer. The maintenance buffer also performs preprocessing of alarms from the framer, controls external devices through general-purpose output latches, and monitors and reports external device status. Figure 3 illustrates the use of the 229FB Maintenance Buffer within the DFI.

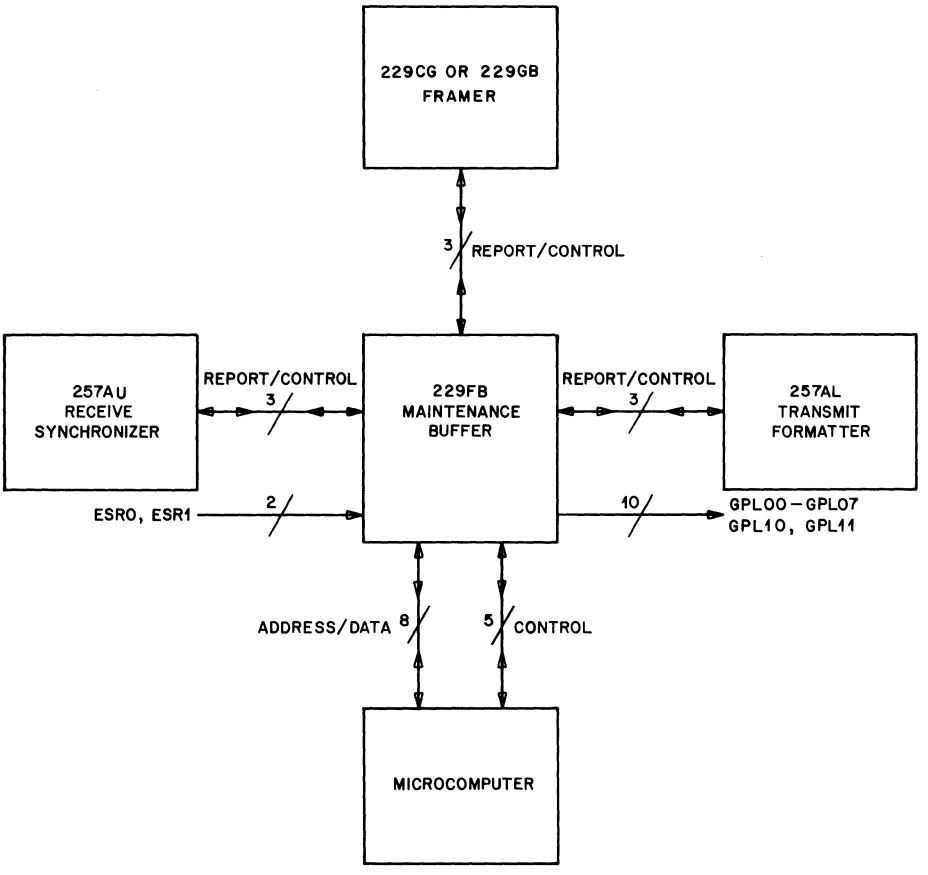


Figure 3. Interface Structure

The 229FB Maintenance Buffer contains 31 addressable registers. Table 2 lists the registers and their characteristics and functions.

Access to the internal registers is achieved by using the bidirectional, multiplexed address/data bus (BUS0—BUS7). The bus is controlled by the address select (AS), data select (DS), read strobe ($\overline{RD}$), and write strobe ($\overline{WR}$).

When accessing the device, AS and DS must be in opposite states. Both inputs are held low when the device is not being accessed. The address/data bus (BUS0—BUS7) is used as an address bus when AS is active (high) and as a data bus when DS is active (high).

Accessing an internal register is a two-step process. First, the register address is put on BUS0—BUS7 while AS is held high and DS low. The address is written into the maintenance buffer by holding $\overline{WR}$ low and $\overline{RD}$ high.

The address/data bus is then switched to the data mode by holding AS low and DS high. For a read operation, $\overline{RD}$ is held low. For a write operation, the data is placed onto BUS0—BUS7 and $\overline{WR}$ is held low.

Table 2. Maintenance Buffer Registers

Address	Name	Access Type	Length (Bits)	Function
1	RSDAA	Read	8	Receive synchronizer report byte storage
2	RSDAB	Read	4	
3	RSEA	Read	8	
4	RSOA	Read	8	
5	RSCONT	Write	8	Receive synchronizer control byte storage
6	TFDA	Read	8	Transmit formatter report byte storage
7	TFEA	Read	8	
8	TFOA	Read	8	
9	TFCONT	Write	8	Transmit formatter control byte storage
10	FRFA	Read	8	Framer report byte storage
11	FRDA	Read	8	
12	FREA	Read	8	
13	FROA	Read	8	
14	FRAA	Read	8	
15	FRAMA	Read	8	
16	FRCONT	Write	8	Framer control byte storage
17	FRFS	Read	8	Framer alarm counter
18	LFV	Read	5	
19	FAS	Read	9	
20	LFAS	Read	5	
21	CFAS	Read	5	
22	LMAS/CRC	Read	5	
23	RMA	Read	5	
24	RFA	Read	5	
25	RFE	Read	9	
26	AIS	Read	8	
27	CLEAR	Write	7	Register reset
28	GPL0	Read/write	8	General-purpose latch
29	GPL1/ESR	Read/write	5	General-purpose latch and error-source register
30	BLKTST1	Read/write	8	Block and test register
31	BLKTST2	Read/write	8	Block and test register

Selected maintenance buffer registers can be cleared or blocked from receiving data by setting appropriate bits in the CLEAR and BLKTST registers, respectively. Table 3—5 list the bit assignments for these registers.

Table 3. CLEAR Register Bit Assignments

Bit	Name	Register Cleared
0	RSCLR	1, 3, 4
1	TFCLR	6, 7, 8
2	FRCLR	11, 12, 13, 14, 15
3	RSFCLR	2
4	FRFCLR	10, 17—24, 26
5	RFECLR	25
6	ESRCLR	29 (bits 2 and 3)

Table 4. BLKTST1 Register Bit Assignments

Bit	Name	Register Cleared
0	RSBL0	Block register 1 (RSDAA)
1	RSBL1	Block register 2 (RSDAB)
2	RSBL2	Block register 3 (RSEA)
3	RSBL3	Block register 4 (RSOA)
4	TFBL0	Block register 6 (TFDA)
5	TFBL1	Block register 7 (TFEA)
6	TFBL2	Block register 8 (TFOA)
7	3MSSET	Initialize 3-ms timing (vector testing only)

Table 5. BLKTST2 Register Bit Assignments

Bit	Name	Register Cleared
0	FRBL0	Block register 10 (FRFA)
1	FRBL1	Block register 11 (FRDA)
2	FRBL2	Block register 12 (FREA)
3	FRBL3	Block register 13 (FROA)
4	FRBL4	Block register 14 (FRAA)
5	FRBL5	Block register 15 (FRAMA)
6	RLPEN	Receive loopback mode
7	TLPEN	Transmit loopback mode

Registers 1—16 (see Table 2) of the maintenance buffer are used as interface registers between the serial report and control streams of the 257AU Receive Synchronizer, 257AL Transmit Formatter, T7229 or 229GB Framer, and the on-board DFI microcomputer.

Serial report and control streams are each organized into frames of sixteen 8-bit bytes. The transmission rate for both the serial report and control streams is 1.024-Mb/s.

Each device control stream uses only one byte of control information, which is updated once per frame and repeated 16 times within a frame. Maintenance buffer registers RSCONT, TFCONT, and FRCONT (see Table 2) are reserved for storing the control bytes for the receive synchronizer, transmit formatter, and framer, respectively.

Control bytes are first written into the selected register by the external microcomputer and then serially output to the appropriate device by the maintenance buffer. RCTLE provides a control enable for the receive synchronizer; TFCTLE provides a control enable for both the transmit formatter and the framer.

One restriction should be noted when writing the control registers: There should be a time period of at least one frame between two write accesses to the same control registers, since the control information is updated once every frame. If the second write information is written into the buffer before the first write information has a chance to be sent out on the control stream, the first write information is lost.

Receive Synchronizer Interface

The 257AU Receive Synchronizer serial report stream contains a device alarm, facility status, exercise audit, and option audit byte. These four bytes are arranged into a serial report stream, as illustrated in Figure 4. They are transmitted four times in succession by the receive synchronizer to form a 16-byte serial report frame. The start of each frame is signaled to the 229FB Maintenance Buffer by assertion of RSYNC.

The four report bytes transmitted by the receive synchronizer are updated at the start of each transmitted frame. The maintenance buffer stores each received byte, four times a frame, in the corresponding registers, as listed in Table 6.

Table 6. 257AU Receive Synchronizer Serial Report Byte Storage

Report Bit	Storage Register
Device alarm	RSDAA (register 1)
Facility status	RSDAB (register 2)
Exercise audit	RSEA (register 3)
Option audit	RSOA (register 4)

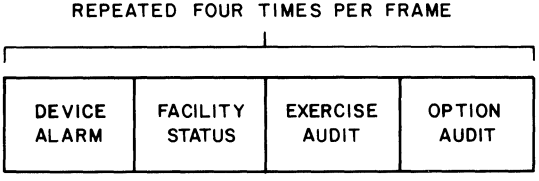


Figure 4. 257AU Receive Synchronizer Serial Report Stream Format

Registers 1 and 2, used for storing device alarm and facility status report bytes, consist of SR-type latches. Individual latches, except for bit 0 of register 1, are set if an incoming report bit is a 1. All of the latched bits remain latched until cleared by the maintenance buffer, regardless of subsequent bit transmissions. This allows capture and report to the external microcomputer of transient alarms.

Bit 0 of register 1 receives the inverted form of the transmitted report bit. This bit is set by the receive synchronizer for the no-alarm condition and is cleared to indicate a loss-of-clock alarm. Inverting this bit insures that both the RSDAA and RSDAB registers contain all 0s when no alarms exist.

Audit registers RSEA and RSOA consist of D-type latches. These registers reflect the current status of each received report byte.

The serial control stream byte for the receive synchronizer is shifted out of an internal recirculating 8-bit shift register 16 times a frame by the maintenance buffer. The shift register is loaded at the start of each frame from RSCONT, register 5. Loading of the serial control stream byte into the shift register is inhibited when DS is high and RSCONT is being updated. Shift register loading resumes when DS is cleared.

The receive synchronizer serial report and control stream interface circuits can be checked by looping back the control stream into the report stream. Loopback is enabled by setting bit 6 of BLKTST2. Setting this bit disables RSRS and internally connects the control stream output to the report stream registers. These registers can then be read to verify operation of the control and report stream circuits.

Transmit Formatter Interface

The 257AL Transmit Formatter serial report stream contains an alarm, exercise audit, and option audit byte. These three bytes are arranged into a serial report stream, as illustrated in Figure 5. These four bytes (note that the alarm byte is repeated) are transmitted by the transmit formatter four times in succession to form a 16-byte serial report frame.

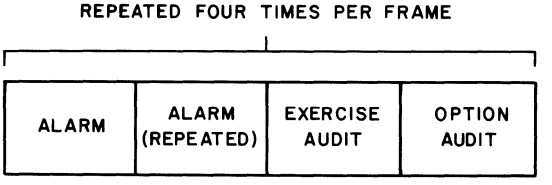


Figure 5. 257AL Transmit Formatter Serial Report Stream Format

The start of both the transmit formatter and framer serial report frames are signaled to the maintenance buffer by assertion of TSYNC. During the first half-frame, the maintenance buffer stores each received transmit formatter report byte (except for the repeated alarm bytes) in the corresponding registers, as listed in Table 7.

Table 7. 257AL Transmit Formatter Report Byte Storage

Report Byte	Storage Register
Device alarm	TFDA (register 6)
Exercise audit	TFEA (register 7)
Option audit	TFOA (register 8)

Register 6, used for storing the alarm report byte, consists of SR-type latches. Bit 0 of the received alarm byte is inverted so that this register contains all 0s if no alarm conditions exist. Transient alarms are latched until externally cleared.

Audit registers TFEA and TFOA consist of D-type latches. These registers reflect the current status of each received report byte.

The serial control stream byte for the transmit formatter is shifted out of an internal recirculating 8-bit shift register 16 times a frame by the maintenance buffer. The shift register is loaded at the start of each frame from TFCONT, register 9. Loading of the serial control stream byte into the shift register is inhibited when DS is high and TFCONT is being updated. Shift register loading resumes when DS is cleared.

The transmit formatter serial report and control stream interface circuits can be checked by looping back the control stream into the report stream. Loopback is enabled by setting bit 7 of BLKTST2, register 31. Setting this bit disables TSRS and RSRS, and internally connects the control stream output to the report stream registers. During the first half-frame, the transmit formatter control stream is looped back into the serial report stream. The framer serial control stream is looped back into the serial report stream during the second half-frame. The report stream registers can then be read to verify operation of the serial control and report stream circuits.

Framer Interface

The T7229 or 229GB Framer serial report stream contains a facility alarm, device alarm, exercise audit, option audit, action audit, and action mask audit byte. These six bytes are arranged into a serial report stream, as illustrated in Figure 6. The eight bytes (note the inclusion of two null bytes) are transmitted by the framer twice in succession to form a 16-byte serial report frame.

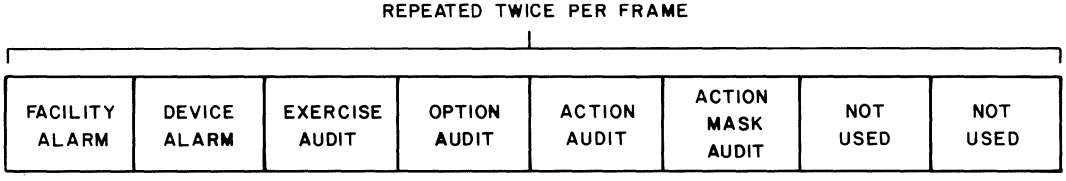


Figure 6. T7229 Framer Serial Stream Format

The start of both the framer and transmit formatter serial report frames are signaled to the maintenance buffer by assertion of TSYNC. During the second half-frame, the maintenance buffer stores each received framer report byte in the corresponding registers, as listed in Table 8.

Table 8. T7229 Framer Report Byte Storage

Report Byte	Storage Register
Facility alarm	FRFA (register 10)
Device alarm	FRDA (register 11)
Exercise audit	FREA (register 12)
Option audit	FROA (register 13)
Action audit	FRAA (register 14)
Action mask audit	FRAMA (register 15)

Registers 10 and 11 use SR-type latches to capture transient alarm indications. Unlike the receive synchronizer and transmit formatter interface circuits, there is no inversion on the first bit of the framer serial report stream. Audit registers 2—15 use D-type latches and do not retain transient data.

The serial control stream byte for the framer is shifted out of an internal recirculating 8-bit shift register 16 times a frame by the maintenance buffer. The shift register is loaded at the start of each frame from TFCONT, register 16. Loading of the serial control stream byte into the shift register is inhibited when DS is high and TFCONT is being updated. Shift register loading resumes when DS is cleared.

The framer serial report and control stream interface circuits can be checked by looping back the control stream into the report stream. Loopback is enabled by setting bit 7 of BLKTST2. Setting this bit disables TSRS and RSRS, and internally connects the control stream output to the report stream registers. During the first half-frame, the transmit formatter control stream is looped back into the serial report stream. The framer serial control stream is looped back into the serial report stream during the second half-frame. The report stream registers can then be read to verify operation of the serial control and report stream circuits.

Facility Alarm Counters

The facility alarm byte of the framer serial report stream contains status information on the digital facility being reported to the DFI. Individual bits of this report byte are counted and stored by the maintenance buffer in alarm counter registers 18—26 (see Table 2). Table 9 shows the correspondence between the eight alarm registers and the individual bits of the facility alarm byte.

Table 10 lists the appropriate facility alarm bit conditions that cause alarm counter registers 18—26 to be incremented. As indicated in this table, four of the facility alarm bits are filtered for a 3-ms period before the corresponding alarm counter registers (registers 18, 20, 21, and 24) are updated. The remaining five alarm registers are updated directly from the received alarm bits at the frame sampling rate of 125 μs.

Each alarm count register has an associated threshold value, which is listed in Table 11. When a register's count equals or exceeds its threshold value, a corresponding bit in register 17 is set. Bits 0—5 and 7 of register 17 correspond to registers 18—23 and 25, respectively. When the framer is in extended-frame format (Fe) mode, bit 6 corresponds to register 25; for all other modes, it is controlled by register 24.

Table 9. Alarm Register Characteristics

Register	Max Count	Alarm Bit Counted
18	16	0
19	384	1
20	16	2
21	16	3
22	24	4
23	24	5
24	16	6
25	511	6
26	192	7

Table 10. Facility Alarm Bit Processing

Line Format Violation (LFV). Register 18 is incremented by one if facility alarm bit 0 is set one or more frames in a 3-ms period.
Frame Alignment Signal (FAS) Error. Register 19 is incremented by one for every frame in which facility alarm bit 1 is set. Register 19 is a 9-bit counter, but only the upper eight facility alarm bits are readable. The microcomputer must multiply the count read by two.
Loss-of-Frame Alignment Signal (LFAS). Register 20 is incremented by one if facility alarm bit 2 is set for one or more times in a 3-ms period.
Change-of-Frame Alignment Signal (CFAS). Register 21 is incremented by one if facility alarm bit 3 is set for one or more frames in a 3-ms period.
Loss-of-Multiframe Alignment Signal (LMAS) or Cyclic Redundancy Check (CRC) Error. Register 22 is incremented during each frame that facility alarm bit 4 is set. This facility alarm bit is used to report LMAS and CRC errors for CEPT and DS1 modes, respectively. The fastest rate at which these alarms can occur on the facility is 2 ms in CEPT mode and 3 ms in DS1 mode.
Remote Multiframe Alignment (RMA) Error. Register 23 is incremented by one when facility alarm bit 5 is set and the framer is in CEPT mode. The maximum rate at which this facility alarm bit can be set is 2 ms.
Remote Frame Alarm (RFA). Register 24 is incremented by one when facility alarm bit 6 is set for all frames during a 3-ms period and the framer is not in extended-frame format (Fe) mode.
Remote Frame Alarm, Fe Mode (RFE). Register 25 is incremented by one for each frame that has facility alarm bit 6 set when the framer is in the extended-frame format (Fe) mode. Any frame with facility alarm bit 6 not set clears this register. When a count of 511 is reached, the counter retains its count until facility alarm bit 6 is a 0. Only the upper eight facility alarm bits of this 9-bit counter are readable (the microcomputer must multiply by two).
Alarm Indication Signal (AIS). Register 26 is incremented by one when facility alarm bit 7 is set.

Table 11. Register Threshold Values

Register	Threshold	Register	Threshold
18—22	1	24	4
		25	498
23	22	26	180

All alarm count registers are disabled while being read. Once an alarm count register's address has been latched into the maintenance buffer, the counter is not incremented while DS is active (high).

General-Purpose Latch and Error-Source Registers

Registers 28 and 29 are general-purpose latch and error-source registers. Register 28 and bits 0 and 1 of register 29 consist of D-type latches. GPL00—GPL07 contain the current state of bits 0—7 of register 28, respectively. The bit assignments for register 29 are given in Table 12. The state of bits 0 and 1 of this register are output on GPL10 and GPL11, respectively.

Table 12. Register 29 (GPL1/ESR) Bit Assignments

Bit	Name	Access
0	GPL10	Read/write
1	GPL11	Read/write
2	ESR0	Read/write*
3	ESR1	Read/write*
4	ESR test	Write*

* When bit 4 is set, ESR0 and ESR1 are disconnected from the external pins and can be set by writing to bits 2 and 3, respectively. This mode is used for device testing purposes.

The error-source inputs are latched by using two SR-type latches. ESR0 and ESR1 are input to these two latches when bit 4 of register 29 is zero. Setting bit 4 of register 29 causes these two latches to be disconnected from ESR0 and ESR1 and connected to bits 2 and 3 of register 29, respectively.

Register Initialization

In addition to the clearing capabilities provided by register 27 (see Table 3), driving $\overline{CLR}$ low clears registers 5, 9, 16, and 27—31. The following procedure, using $\overline{CLR}$, initializes the maintenance buffer:

1. Drive $\overline{CLR}$ low for a minimum of 200 ns and then high.
2. Write all 1s to register 27, wait a minimum of 1 μs, and then write all 0s to this register.
3. Write all 0s to the address/data bus.

Characteristics

Electrical Characteristics

T_A = 0 to 85 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Supply current	I_{DD}	—	—	150	mA
Input voltages:					
high	V_{IH}	2.4	—	—	V
low	V_{IL}	—	—	0.8	V

Parameter	Symbol	Min	Typ	Max	Unit
Output voltages:					
high	V_{OH}	2.4	—	—	V
low	V_{OL}	—	—	0.4	V
Input current:					
high	I_{IH}	20	—	—	μA
low	I_{IL}	—	—	20	μA
Output current:					
high	I_{OH}	—	—	0.2	mA
low	I_{OL}	—	—	2.2	mA
Power dissipation	PD	—	380	750	mW

Maximum Ratings

DC supply voltage (V_{DD}) range ..... −0.5 to +7 V
Power dissipation (PD) ..... .75 W
Storage temperature (Tstg) range ..... −40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Table 13. Output Loading

Pin	Name	Current	Capacitance
3—5	FSCS, TSCS, RSCS	1 LSTTL load	70 pF
6	RCTLE	1 LSTTL load	70 pF
7	TFCTLE	1 LSTTL load	90 pF
16—25	GPL00—GPL07, GPL10, GPL11	2 LSTTL loads	90 pF
26—29 32—35	BUS0—BUS3 BUS4—BUS7	2 LSTTL loads	250 pF

Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit
tASHWRL	Address select set-up time	200	—	—	ns
tWRHASL	Address select hold time	200	—	—	ns
tDSHWRL	Data select set-up time (write)	200	—	—	ns
tWRHDSL	Data select hold time (write)	200	—	—	ns
tWRLWRL	Address to data time (write)	2.4	—	—	μs
tWRLWRH	Write pulse width	300	—	—	ns
tAVWRH	Address set-up time	250	—	—	ns
tWRHAX	Address hold time	40	—	—	ns
tDVWRH	Data set-up time	250	—	—	ns

Symbol	Description	Min	Typ	Max	Unit
tWRHDX	Data hold time (write)	40	—	—	ns
tDSHRDL	Data select set-up time (read)	200	—	—	ns
tRDHDSL	Data select hold time (read)	200	—	—	ns
tWRLRDL	Address to data time (read)	2.4	—	—	μs
tRDLRDH	Read pulse width	300	—	—	ns
tRDLDV	Read delay time	—	—	200	ns
tRDHDX	Data hold time (read)	0	—	100	ns
tRDLRDH	Read pulse width	300	—	—	ns
tSCHSCH	System clock period	241	244	247	ns
tSCHSCL	Duty cycle	—	50*	—	%
tSYHSYL	TSYNC and RSYNC pulse width	232	244	256	ns
tSYHSCH	TSYNC and RSYNC set-up time	80	—	—	ns
tSCHSYL	TSYNC and RSYNC hold time	100	—	—	ns
tCHCL	RCTLE and TFCTLE pulse width	—	7.8	—	μs
tRSYHRSYH	RSYNC period	—	125	—	μs
tRCHRCH	RCTLE period	—	125	—	μs
tSCHRSV	Report stream bit delay	—	—	244	ns
tSCHCSV	Control stream bit delay	—	—	244	ns
tSCHCH	Control delay	—	—	244	ns
tTSYHTSYH	TSYNC period	—	125	—	μs
tTFCHTFCH	TFCTLE period	—	125	—	μs
tESHESL	ESR0 and ESR1 pulse width	200	—	—	ns
tCRLCRH	CLR pulse width	200	—	—	ns
tWRHGPDV	GPL data valid time	—	—	1	μs

* ±10%

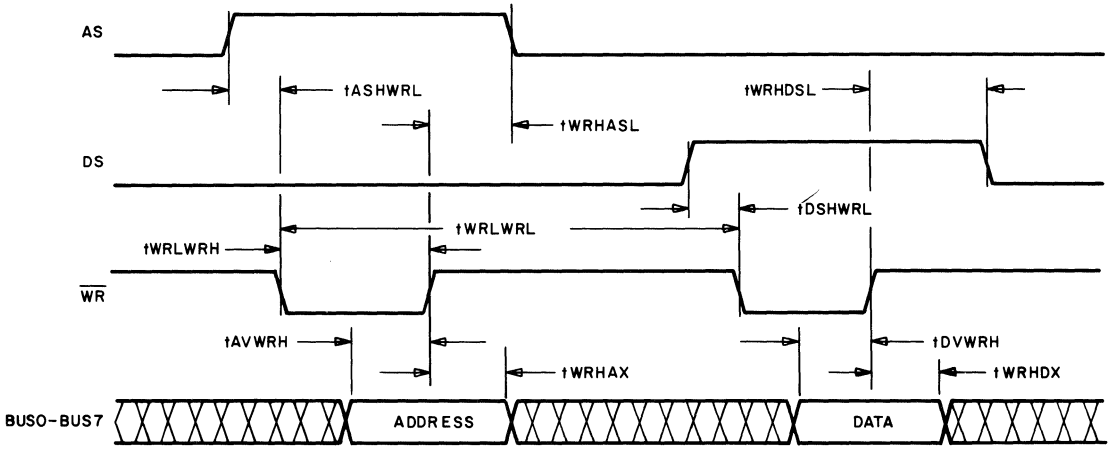


Figure 7. Data Write Timing

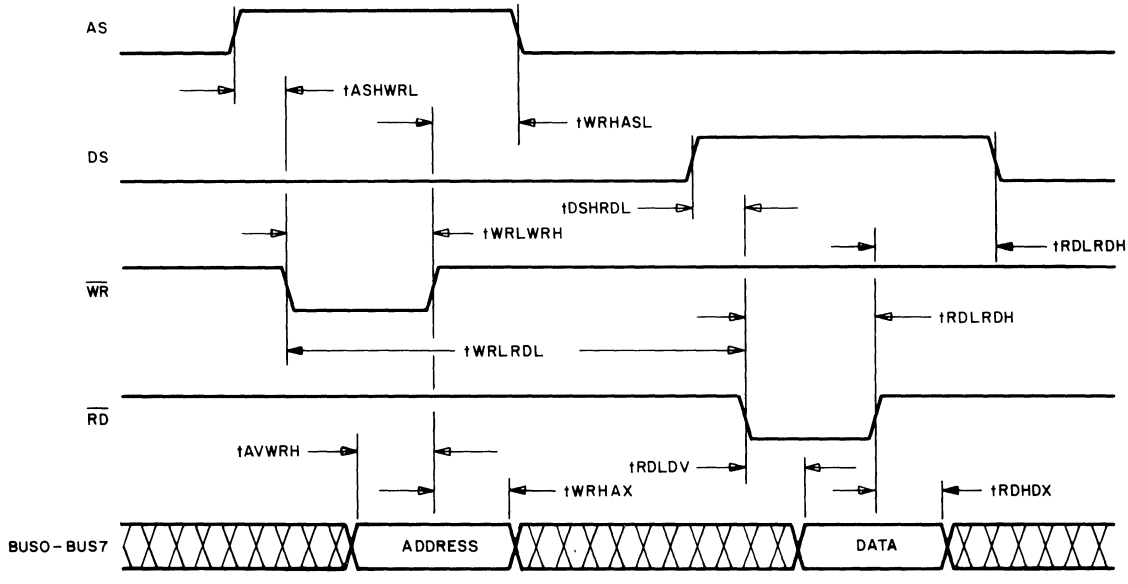


Figure 8. Data Read Timing

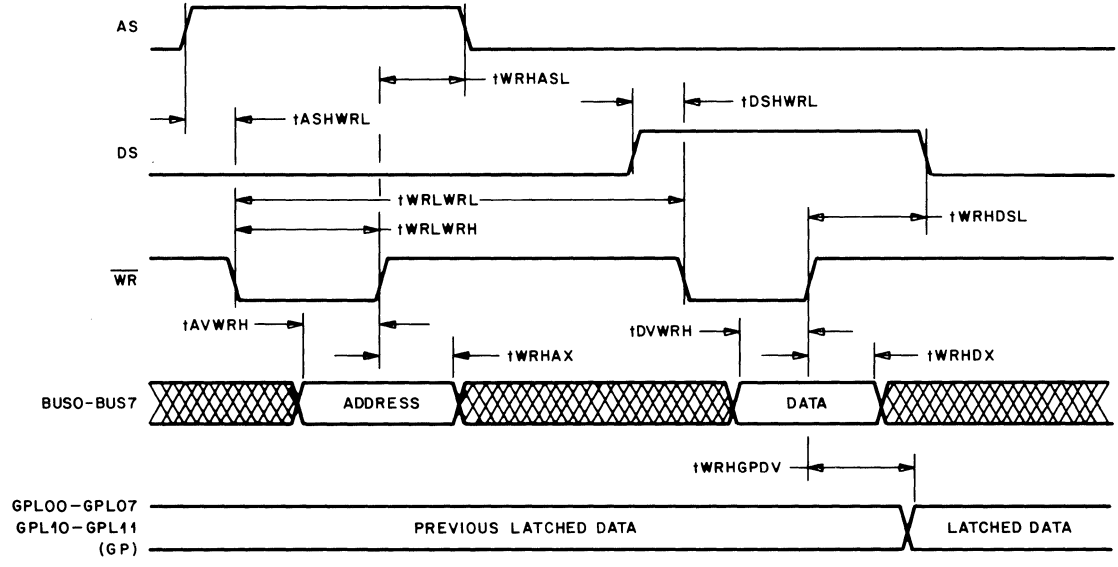


Figure 9. General-Purpose Latch Timing

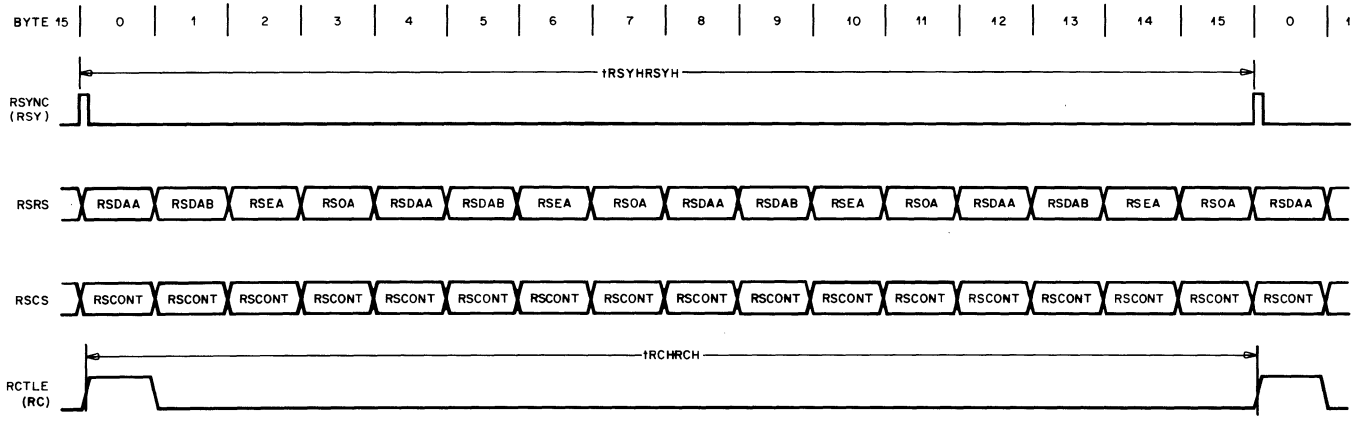


Figure 10. Receive Synchronizer Report/Control Stream Timing

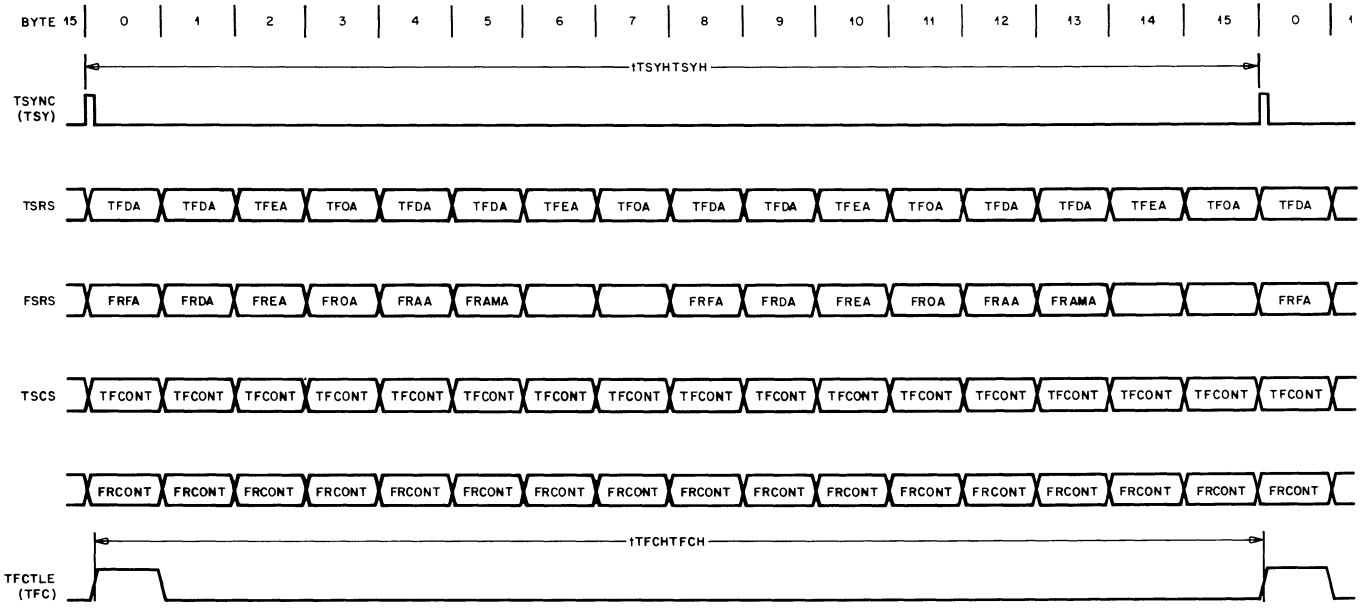


Figure 11. Transmit Formatter and Framer Report/Control Stream Timing

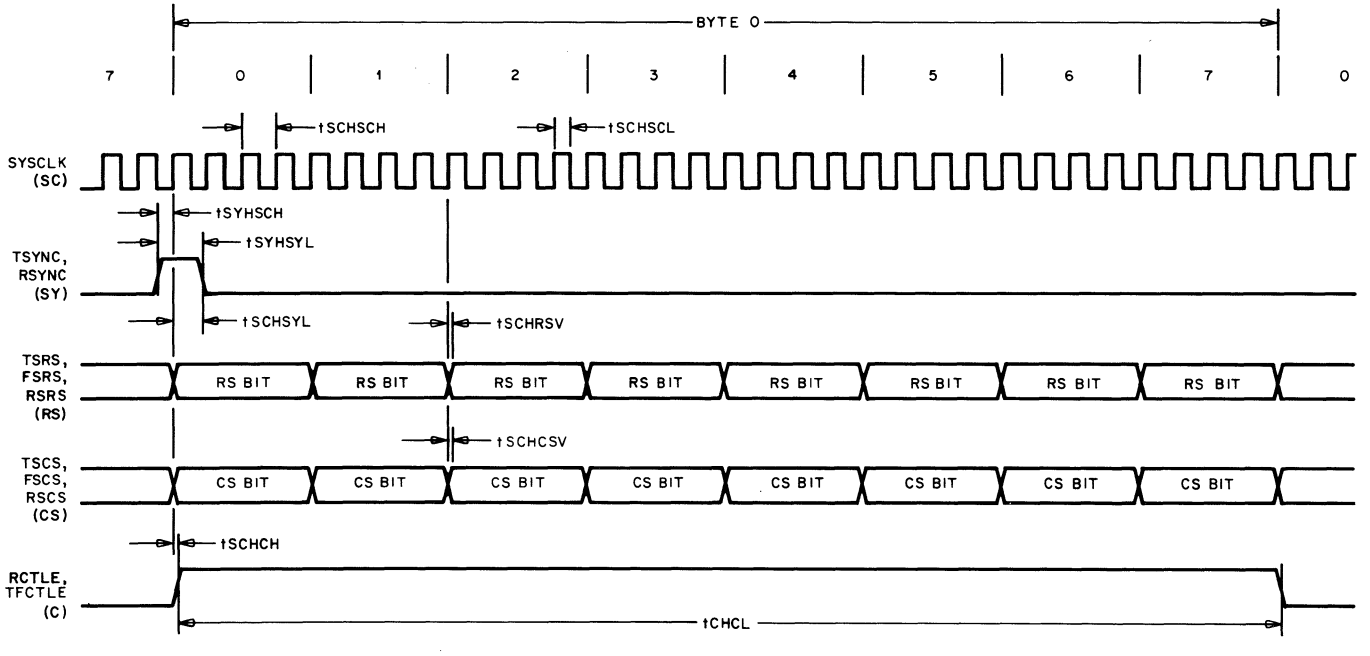


Figure 12. Detail Report/Control Stream Timing

229GB Primary Access Framer

Features

- Bipolar and B8ZS line format capability
- Multiple DS1 TDM frame formats
  - Independent formats – D4 channel bank (D4), *SLC* 96 Carrier (SL), extended superframe (ESF), and digital data system T1 digital multiplexer (DDS)
  - Auxiliary signaling format – DMI bit-oriented signaling (BOS)
- Off-line, defensive, and fast frame synchronization
- SL, ESF, and DDS facility data link insertion and extraction
- Remote frame/multiframe alarm activation and detection
- Transmission performance monitoring capability:
  - Bipolar and B8ZS violations
  - Frame alignment signal (frame bit) errors
  - Loss-of-frame/loss-of-multiframe alignment
  - CRC-6 errors (ESF mode)
  - Change-of-frame alignment

Description

The 229GB Primary Access Framer integrated circuit provides the line format and frame format interfaces for DS1 (1.544 Mb/s) digital carrier systems. It performs in-line and off-line frame-oriented functions in both the receive and transmit directions. The 229GB Framer is TTL-compatible and is packaged in a 40-pin ceramic DIP.

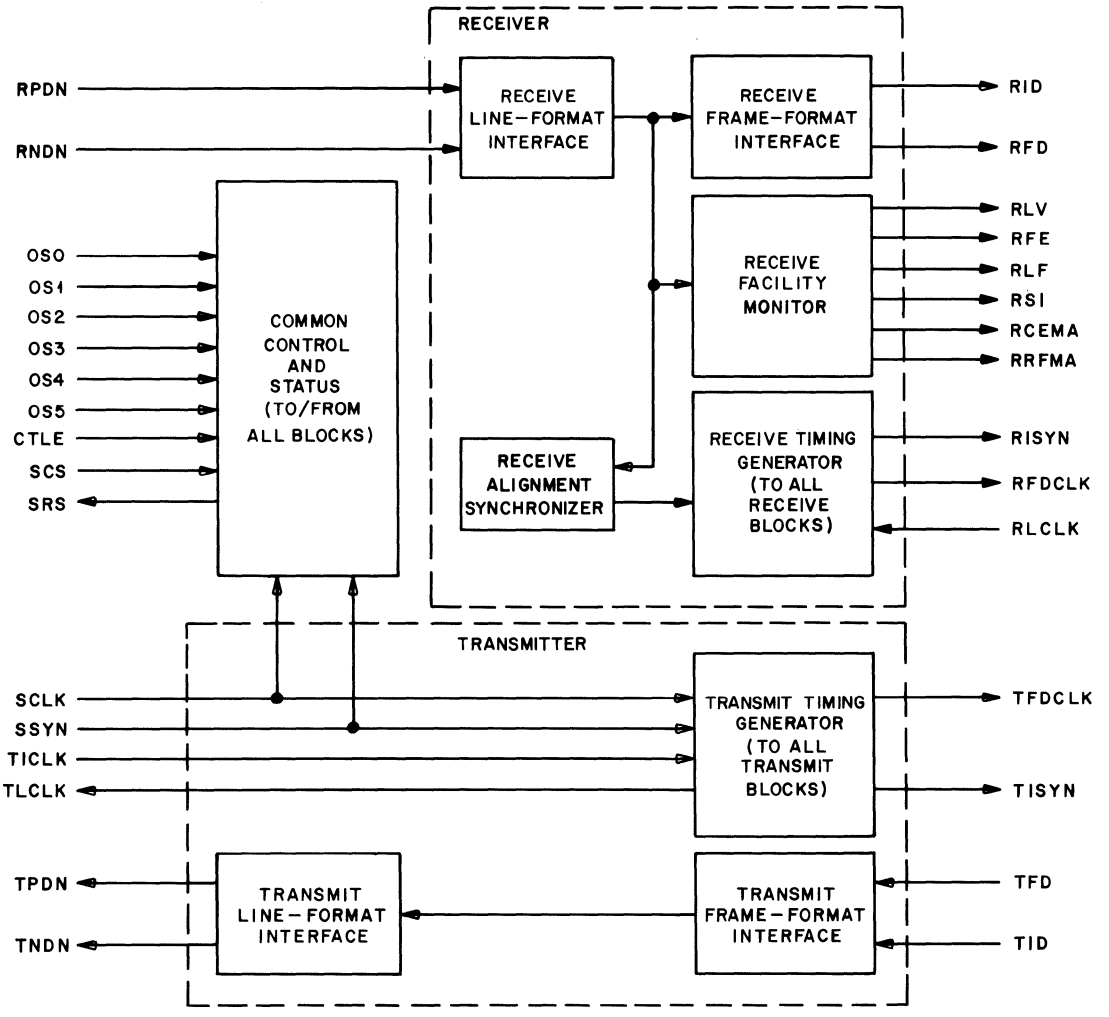
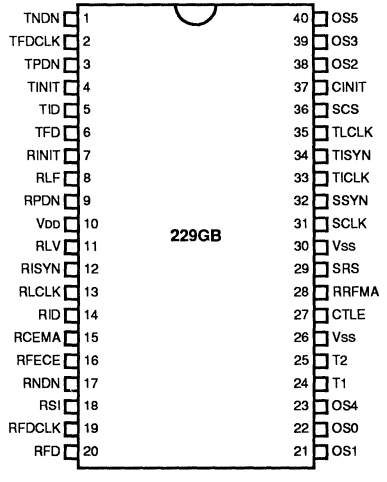


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin	Symbol	Pin
CINIT	37	RISYN	12	TFD	6
CTLE	27	RLCLK	13	TFDCLK	2
OS0	22	RLF	8	TICLK	33
OS1	21	RLV	11	TID	5
OS2	38	RNDN	17	TINIT	4
OS3	39	RPDN	9	TISYN	34
OS4	23	RRFMA	28	TLCLK	35
OS5	40	RSI	18	TNDN	1
RCEMA	15	SCLK	31	TPDN	3
RFD	20	SCS	36	VDD	10
RFDCLK	19	SRS	29	VSS	26
RFECE	16	SSYN	32	VSS	30
RID	14	T1	24		
RINIT	7	T2	25		

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	TNDN	O	**Transmit Negative-Rail Data Inverted.** 1.544-Mb/s dual-rail pseudoternary (bipolar or B8ZS) TDM data.
2	TFDCLK	O	**Transmit Facility Data Link Clock.** Reference clock for transmit facility data link data on pin 6. In DDS mode, this is an 8-kHz clock signal; in SL and ESF modes, this is a 4-kHz clock signal.
3	TPDN	O	**Transmit Positive-Rail Data Inverted.** 1.544-Mb/s dual-rail pseudoternary (bipolar or B8ZS) TDM data.
4	TINIT	I	**Transmit Initialization.** Manufacturing test pin. Ground this pin for normal operation. Setting pins 4, 7, and 37 puts all transmit output pins in a high-impedance, 3-state mode.
5	TID	I	**Transmit Interdevice Data.** 1.544-Mb/s unipolar TDM source data.
6	TFD	I	**Transmit Facility Data Link Data.** 8-kb/s data in the DDS mode; 4-kb/s in the SL and ESF modes. Data link source data is strobed in by negative transitions of TFDCLK (pin 2).

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
7	RINIT	I	**Receive Initialization.** Manufacturing test pin. Ground this pin for normal operation. Setting pins 4, 7, and 37 puts all receive section output pins in a high-impedance, 3-state mode.
8	RLF	O	**Receive Loss-of-Frame Alignment.** This pin is set upon loss-of-frame and/or loss-of-multiframe alignment.
9	RPDN	I	**Receive Positive-Rail Data Inverted.** 1.544-Mb/s dual-rail pseudoternary (bipolar or B8ZS) TDM data. Tie this pin and RNDN (pin 17) together for unipolar TDM received data.
10	V_{DD}	—	**5 V Supply.**
11	RLV	O	**Receive Line Format Violations.** This pin is set for each receive line format violation.
12	RISYN	O	**Receive Interdevice Synchronization.** A 488-ns pulse repeated at 3-ms intervals. Transitions on this pin occur only on negative transitions of RLCLK (pin 13).
13	RLCLK	I	**Receive Line Clock.** 1.544 MHz.
14	RID	O	**Receive Interdevice Data.** 1.544-Mb/s unipolar TDM output data. Transitions on this pin occur only on negative transitions of RLCLK (pin 13).
15	RCEMA	O	**Receive CRC-6 Errors/Loss-of-Multiframe Alignment.** This pin is set upon detection of a receive cyclic redundancy check error in ESF non-BOS mode or loss-of-multiframe alignment in the BOS mode.
16	RFECE	O	**Receive Frame Alignment Signal Error/CRC-6 Errors.** This pin is set upon detection of a frame alignment signal (frame bit) error in the non-BOS mode or upon a receive cyclic redundancy check error in ESF BOS mode.
17	RNDN	I	**Receive Negative-Rail Data Inverted.** 1.544-Mb/s dual-rail pseudoternary (bipolar or B8ZS) TDM data.
18	RSI	O	**Receive Signaling Inhibit.** This pin is set by a framing error, loss-of-frame alignment, and/or loss-of-multiframe alignment.
19	RFDCLK	O	**Receive Facility Data Link Clock.** Reference clock for receive facility data link data on pin 20. In DDS mode, this is an 8-kHz clock signal; in SL and ESF modes, this is a 4-kHz clock signal.
20	RFD	O	**Receive Facility Data Link Data.** 8-kb/s data in DDS mode; 4-kb/s data in SL and ESF modes.
21 22 23	OS1 OS0 OS4	I	**Option Selects 1, 0, and 4.** Option selection pins. Options can also be selected by using the serial control stream (pin 36).

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
24	T1	I	**Test 1.** For manufacturing purposes only. Must be grounded for normal operation.
25	T2	I	**Test 2.** For manufacturing purposes only. Must be grounded for normal operation.
26	Vss	—	**Ground.**
27	CTLE	I	**Control Enable.** Control lead to enable loading of serial control stream (pin 36).
28	RRFMA	O	**Receive Remote Frame and Multiframe Alarm.** This pin is set upon a receive remote frame alarm and cleared otherwise.
29	SRS	O	**Serial Report Stream.** The serial report stream is output at a 1-Mb/s rate. SRS contains one byte for facility reports, one byte for device alarms, and four bytes for auditing the option, exercise, action, and action-mask control fields. Each of these six bytes is repeated twice per frame; the remaining four bytes are padded with 0s. Facility and alarm bytes are updated once a frame; the remaining four control bytes are updated twice a frame.
30	Vss	—	**Ground.**
31	SCLK	I	**System Clock.** 4.096 MHz.
32	SSYN	I	**System Synchronization.** 8 kHz system synchronization pulse of 244-ns duration. This pin is strobed on positive transitions of both SCLK (pin 31) and TICLK (pin 33).
33	TICLK	I	**Transmit Interdevice Clock.** 1.544 MHz.
34	TISYN	O	**Transmit Interdevice Synchronization.** This pin, which establishes frame alignment, is a bit interval pulse asserted every 3 ms.
35	TLCLK	O	**Transmit Line Clock.** 1.544 MHz.
36	SCS	I	**Serial Control Stream.** SCS accepts 8-bit control bytes at a 1-Mb/s rate. Control bytes determine options, consequent actions (channel squelch, non-BOS FDL squelch remote alarm insertion, etc.), action masks, and maintenance exercises. A control byte is shifted in on SCS while CTLE (pin 27) is set.
37	CINIT	I	**Control Initialization.** Manufacturing test pin. Ground this pin for normal operation. Setting pins 4, 7, and 37 puts all control and report pins in a high-impedance, 3-state mode.
38 39 40	OS2 OS3 OS5	I	**Option Selects 2, 3, and 5.** Option selection pin. Options can also be selected by using the serial control stream (pin 36).

Overview

The 229GB Framer is part of an LSI DS1 chip set that includes the 257AU Receive Synchronizer, the 257AL Transmit Formatter, and the 229FB Maintenance Buffer. The 229GB Framer was developed as an alternative to the T7229 (replaces the 229CG) Framer. The 229GB Framer makes it easier to implement an interface to support DMI bit-oriented signaling (BOS). In non-BOS applications, the 229GB Framer has all the functional capabilities of the T7229 Framer except that it does not support the CEPT (2.048 Mb/s) digital carrier systems. The 229GB Framer performs in-line data processing, off-line terminal frame and signaling frame synchronization, and transmission facility and system fault monitoring.

The functional operation of the 229GB Framer is discussed in terms of Figure 1. The circuit is divided into three main blocks: transmitter, receiver, and common control and status.

Transmitter

The transmit section of the 229GB Framer consists of the transmit timing generator (TTG), transmit frame format interface (TFFI), and transmit line format interface (TLFI). The TFFI accepts a unipolar, time-division multiplex (TDM) signal on TID and a unipolar facility data link bit stream on TFD. TID is clocked by a 1.544-MHz timing signal input on TICLK and must be synchronized to the 3-ms interval pulse output on TISYN. The FDL bit stream on TFD must be clocked by the 4-MHz or 8-MHz timing signal output on TFDCLK.

The TDM signal on TID must be formatted with customer data and signaling already in place in channel words 1—24, but with a pseudorandom maintenance pattern in the framing bit (F bit) positions. According to the selected mode, the TFFI overwrites the F bits with the terminal framing (Ft or Fe) or signaling framing (Fs) pattern, the CRC-6 check bits, and/or the FDL bit stream. The TFFI also inserts the remote frame (yellow) alarm (RFA) in the FDL bit positions in the ESF mode and generates the CRC-6 check bits.

In general, the TFFI is transparent to channel words 1—24. When requested, however, it can overwrite the words as follows:

- D4 RFA, zero-code suppression (ZCS), and maintenance squelch patterns in all words.
- DDS frame alignment pattern and FDL and RFA bits in word-24.
- BOS multiframe alignment signal (MAS) and remote multiframe alarm (RMA) in word-24.

The TLFI converts the unipolar TDM signal from the TFFI to a dual-rail bipolar signal and, in the B8ZS mode, replaces strings of 0s with the B8ZS violation code. The resulting dual-rail TDM signal is output on TPDN and TNDN.

The TTG generates TISYN in fixed relationship to a 125-μs interval system sync pulse input on SSYN. It also generates TFDCLK, a 1.544-MHz timing signal output on TLCLK, and all internal synchronization signals. Finally, in the SL mode, it synchronizes to the Fs pattern that must be embedded in the FDL bit stream on TFD.

Receiver

The receive section of the 229GB Framer comprises the receive timing generator (RTG), the receive frame format interface (RFFI), the receive line format interface (RLFI), the receive alignment synchronizer (RAS), and the receive facility monitor (RFM). The RFFI accepts a dual-rail TDM signal on RPDN and RNDN. These inputs are clocked by a 1.544-MHz timing signal input on RLCLK. The TDM signal is converted to a unipolar signal and, in the B8ZS mode, instances of the B8ZS violation code are replaced by strings of 0s. The RLFI detects violations of either the bipolar or B8ZS codes and reports them to the RFM. The TDM output signal is distributed among the RFFI, RAS, and RFM sections.

The RFFI first extracts the FDL bit stream from the F bits in the TDM signal and then overwrites the F bits with the pseudorandom pattern (PRP). In general, the RFFI is transparent to channel words 1—24. When requested, however, it can overwrite all words with a maintenance squelch pattern. In the DDS mode, facility error information from the RFM section is autonomously inserted in the RFA bit position of word-24. The RFFI outputs the processed unipolar TDM signal on RID and the extracted FDL bit stream on RFD. RID is clocked by the 1.544-MHz timing signal input on RLCLK and is synchronized to the 3-ms interval pulse output on RISYN. The FDL bit stream on RFD is clocked by the 4-MHz or 8-MHz timing signal output on RFDCLK.

The RFM section monitors the TDM signal for facility trouble conditions and alarms. Detected trouble conditions and alarms are forwarded to the common control and status block and to dedicated status output leads (RLV, RFECE, RLF, RCEMA, RRFMA, and RSI). Detected loss-of-alignment conditions are reported to the RAS section.

The RAS section establishes terminal frame alignment in all modes, superframe alignment in the D4, SL, and ESF modes, and signaling multiframe alignment in the BOS mode. It operates in a fast, off-line, defensive mode for terminal frame synchronization; the search for the frame alignment pattern and/or sequence (FAS) covers all possible alignment phases simultaneously. When a single candidate FAS is found, alignment is adjusted to the phase of that FAS. To avoid synchronization to a random data pattern, the search cannot be satisfied until at least 24 bits of the candidate FAS have been examined. The search does not affect the operation of the other sections of the receiver until the decision is made that a new frame alignment is required. Consequently, an error burst does not force a loss of alignment.

To avoid alignment to a fixed data or signaling pattern that emulates the FAS, the RAS does not adjust alignment to a new phase if more than one candidate FAS is present. When static emulators last for more than 100 ms in the ESF mode, the synchronizer aligns successively to each candidate FAS (at 200 ms per candidate) until an alignment with the correct CRC-6 pattern is found. This on-line trial-and-error mode is not possible in the D4, DDS, SL, and CEPT modes.

The RTG generates RISYN in fixed relation to the TDM signal output on RID, RFDCLK in fixed relation to the FDL bit stream output on RFD, and all internal synchronization signals.

Common Control and Status

The principal control access to the 229GB Framer is the 1.024-Mb/s serial control stream (SCS) input on pin 36. The SCS is used for provisioning, maintenance exercises, and requests for the application of squelch patterns and remote alarms. It is enabled by the control stream enable (CTLE) input on pin 27. The mode of the device can also be controlled via the external option input leads, OS0—OS5.

The 1.024-Mb/s serial report stream (SRS), output on pin 29, carries reports from the RFM section, reports from fault monitoring circuits distributed throughout the device, and audits of the current control state.

The SCS and SRS are clocked at the 1.024-Mb/s rate by a submultiple of the 4.096-MHz timing signal input on SCLK. The bit boundaries in both the SCS and the SRS and the byte and block boundaries in the SRS are synchronized to the system sync pulse input on SSYN.

Functional Description

Line Format Processing

The transmitter line format processing converts the frame-formatted TDM bit stream into a dual-rail bipolar signal or a modified bipolar output signal (B8ZS). In the bipolar mode, binary 1s in the TDM bit stream become pulses of alternating polarity transmitted between the two output rails, TPDN and TNDN; binary 0s are transmitted as null pulses. Note that the outputs are active-low, (i.e., a pulse corresponds to a binary 0 and no pulse corresponds to a binary 1). In the B8ZS mode, the bipolar

algorithm is modified to guarantee at least one pulse for every 8 transmitted bits by substituting a bipolar violation code (BPV) for blocks of 8 successive 0s, as illustrated in Table 2. The transmitter generates BPVs by sending the BPV pulse to the same output rail as the last preceding bipolar pulse.

Table 2. B8ZS Substitution Code

Before B8ZS	00000000
After B8ZS	000VB0VB

The receiver line format processing is complementary to the transmitter processing. Input pulses on RPDN and RNDN, also active-low, become binary 1s on the TDM output bit stream; missing pulses become binary 0s. In the B8ZS mode, the processing circuit recognizes valid violation codes and replaces them with the correct number of binary 0s.

Frame Format Processing

The 229GB Framer supports four DS1 TDM frame formats: D4 channel bank (D4), *SLC* 96 Carrier System (SL), extended superframe (ESF), and digital data system T1 digital multiplexer (DDS). It also supports the auxiliary word-24 bit-oriented signaling (BOS) multiframe format that can be used with the D4, *SLC* Carrier, and ESF formats to convert them from robbed-bit to bit-oriented signaling.

Table 3. DS1 TDM Frame Formats

DS1 TDM Format	Signaling-Bit Identification
D4	12-frame superframe
SL	12-frame superframe
ESF	24-frame superframe
DDS	No signaling
BOS	24-frame multiframe

The 229GB Framer does not insert or recognize channel data or signaling bits. It superposes and recognizes synchronization and control information.

There are two levels of frame format processing: data level and frame level. Data level processing overwrites bits in specified data words, time slots, or the facility data link (FDL) with new information. Frame level processing affects the framing bits and word-24 in the DDS and BOS modes.

Data Level Processing. The 229GB Framer operation is transparent to message channels and to embedded or formatted signaling bits. However, it has the capability to overwrite certain bits in channel words. The majority of this type of processing is for consequent actions, i.e., inserting remote alarms or squelching the data with specific bit patterns in response to detected trouble conditions. Consequent action capabilities are discussed in the Responses to Facility Trouble and Alarms section.

An additional data level processing capability is zero-code suppression (ZCS), which can be implemented when the Is density requirements are not met transparently (e.g., with B8ZS). ZCS consists of setting bit 7 in any word containing all 0s that is to be transmitted. The framer must apply ZCS or squelch patterns to all words simultaneously, or to none, with one exception: the application of AIS to received word-24 in the BOS mode. Table 4 defines the specific ZCS and maintenance patterns.

The transmitter also generates two types of remote alarm: remote frame alarm (RFA), i.e., yellow alarm and remote multiframe alarm (RMA). Table 5 defines the remote alarms.

Squelch patterns and remote alarms can be turned on by explicit external order or can be enabled for automatic activation; ZCS is activated only by external order. In cases where simultaneous squelch and remote alarm patterns affect the same bit, the remote alarm patterns take precedence. The B8ZS option overrides the ZCS option.

Patterns inserted by the transmitter appear in the dual-rail bipolar output signal; patterns inserted by the receiver appear on the RID and RFD leads.

Table 4. ZCS and Maintenance (Squelch) Patterns

Words 1—24	Format	Location	B1	B2	B3	B4	B5	B6	B7	B8
ZCS	Non-DDS	XMTR	0	0	0	0	0	0	1	0
Idle code	Non-DDS	XMTR	0	1	1	1	1	1	1	1
UC code	DDS	XMTR	0	0	0	1	1	0	0	0
MOS code	DDS	RCVR	0	0	0	1	1	0	1	0
AIS code	Non-DDS	RCVR	1	1	1	1	1	1	1	1

Table 5. Remote Alarms

Alarm	Format	Definition
RFA	D4	Bit 2 of all words in each frame is cleared
	DDS	Bit 6 of word-24 in each frame is cleared
	SL	Not processed by the 229GB Framer
	ESF	An alternating pattern of eight 1s and eight 0s on the FDL
RMA	BOS	Bit 6 of word-24 in frame-24 is cleared

Frame Level Processing. Frame level processing affects the framing bits. A pseudorandom pattern (PRP) is embedded for maintenance purposes in the input data on TID and the output data on RID in all modes. The pattern repeats in the framing bit positions at 24-frame intervals. At the dual-rail bipolar inputs and outputs, the framing bit positions contain the standard framing, data link, and CRC bits (Table 6). Additional framing information is contained in word-24 in the DDS and BOS modes (Tables 7 and 8).

The transmitter has several functions in frame level processing. It the PRP in the TDM input and the superframe F-bit (Fs) sequence in the SL FDL input for errors. It generates the Ft and Fs or Fe bits in the D4, DDS, and ESF modes and generates the Ft pattern and synchronizes to the Fs pattern on the FDL input in the SL mode. The transmitter generates and inserts the ESF CRC-6 check bits as required and copies the SL and ESF FDL input data to the FDL bits.

The receiver synchronizes to the Ft and Fs or Fe bits and then checks the Ft, Fs or Fe, and CRC-6 check bits for errors. The SL and ESF FDL bits are copied to the FDL output. The receiver inserts the PRP in the TDM output. Table 6 summarizes the assignment of framing bits. Word-24 processing takes place in the DDS mode and the BOS mode. Table 7 summarizes word-24 processing in the DDS mode. The transmitter sets FAS to the correct pattern and sets the RFA bit for "no alarm" or clears the RFA bit for "alarm."

The transmitter copies the FDL input data to the FDL bits in the DDS FDL mode, and the receiver routes the FDL bit to the FDL output. The receiver synchronizes to the FAS pattern while checking the FAS bits for errors. It checks the RFA bit for an alarm condition and overwrites the RFA bit with the logical OR of the current Table 8 summarizes the word-24 bits processed in the BOS mode. The transmitter sets or clears the Fm and MAS bits to the correct pattern, and the receiver synchronizes to these patterns. The transmitter clears the RMA bit for "alarm" and sets the RMA bit for "no alarm." and the receiver synchronizes to these patterns. The transmitter clears the RMA bit for "alarm" and sets the RMA bit for "no alarm."

DDS, D4, SL			ESF			
FRs	Ft	Fs or FDL*	FRe	FDL*	CRC	Fe
1	1		1	D		
2		0 or D	2		C1	
3	0		3	D		
4		0 or D	4			0
5	1		5	D		
6		1 or D	6		C2	
7	0		7	D		
8		1 or D	8			0
9	1		9	D		
10		1 or D	10		C3	
11	0		11	D		
12		0 or D	12			1
1	1		13	D		
2		0 or D	14		C4	
3	0		15	D		
4		0 or D	16			0
5	1		17	D		
6		1 or D	18		C5	
7	0		19	D		
8		1 or D	20			1
9	1		21	D		
10		1 or D	22		C6	
11	0		23	D		
12		0 or D	24			1

* D = FDL input data.

Table 6. Word-24 Bits Processed in the DDS Mode

Word-24	B1	B2	B3	B4	B5	B6	B7	B8
FAS	1	0	1	1	1	—	—	0
RFA	—	—	—	—	—	0/1	—	—
FDL	—	—	—	—	—	—	D*	—

* D = FDL input data.

Table 8. Word-24 Bits Processed in the BOS Mode

Word-24	B1	B2	B3	B4	B5	B6	B7	B8
Fm	—	—	—	—	—	—	0/1	—
MAS	—	—	1	1	0	—	—	1
RMA	—	—	—	—	—	0/1	—	—
AIS Code	1	1	1	1	1	1	1	1

Alignment and Synchronization

The 229GB Framer uses bit sequences and bit patterns to establish alignment in the received and transmitted signals. Bit sequences are composed of individual bits spaced at frame or multiple-frame intervals. Bit patterns are multiple bits in a single frame. Table 9 contains the bit sequences and patterns used to establish alignment.

The terminal frame (Ft) and superframe (Fs) sequences alternate in the F-bit positions. The SL Fs bits occur in only 2 out of every 6 superframes. Frame and superframe alignment are established simultaneously by the ESF Fe bits.

The DDS FAS provides fast frame synchronization. The BOS Fm bits are the principal multiframe alignment reference, while the BOS MAS is useful only as an existence check. The PRP is used for interdevice maintenance only.

Table 9. Bit Sequences and Patterns Used to Establish Alignment

Name	Format	Location	Pattern	Alignment
Ft Bits	Non-ESF	Every 2nd F bit	01	Frame
Fs Bits	D4, SL	Every 2nd F bit	001110	Superframe
Fe Bits	ESF	Every 4th F bit	001011	Frame, superframe
Fm Bits	BOS	Every word-24, bit 7	0xFFFFFE	Multiframe
FAS	DDS	Every word-24, bits 1—5, 8	101110	Frame
MAS	BOS	Frame-24, word-24, bits 3—5, 8	1101	Multiframe
PRP	All	Every F bit	0xF8DD42	Interdevice

Interdevice Synchronization

The 229GB internal timing generators provide external 24-frame syncs (TISYN and RISYN) for interdevice synchronization. These syncs define the phase of the TDM signals on TID and RID, respectively. Normally, the transmitter is locked in frame synchronization to the input system sync pulse (SSYN), but has an arbitrary superframe or multiframe phase. In the SL mode, however, the transmitter is forced to synchronize to the transmit FDL input on TFD because this data stream has the Fs alignment sequence embedded in it. The receive interdevice sync is locked to the frame and superframe/multiframe phases determined by the receive alignment synchronizer.

In the non-BOS mode, interdevice synchronizations identify frame and superframe alignment; in the BOS mode, they define word-24 multiframe alignment. In all cases, they also define the phase of the interdevice PRP embedded in the framing bit positions. The relationship of the PRP to the frame and superframe patterns (non-BOS mode) is shown in Table 10 and the word-24 multiframe pattern (BOS mode) is shown in Table 11.

Table 10. Interdevice Alignment in Non-BOS Modes

Bits	Bit Sequence*
Ft	1x0x1x0x1x0x1x0x1x0x1x0x
Fs	x0x0x1x1x1x0x0x0x1x1x1x0
Fe	xxx0xxx0xxx1xxx0xxx1xxx1
Fm	xxxxxxxxxxxxxxxxxxxxxxxx
PRP	111110001101110101000010

* x = don't care.

Table 11. Interdevice Alignment in BOS Modes

Bits	Bit Sequence*
Ft	xxxxxxxxxxxxxxxxxxxxxxxx
Fs	xxxxxxxxxxxxxxxxxxxxxxxx
Fe	xxxxxxxxxxxxxxxxxxxxxxxx
Fm	111111111111111111111110
PRP	111110001101110101000010

* x = don't care.

Link Synchronization

When a loss-of-frame alignment (LFA) condition is detected by the receiver, the alignment synchronizer activates but the normal receiver functions continue to operate at the previously determined frame alignment. After the synchronization circuit determines that a new alignment is required, the receiver circuits are forced to that new alignment. The defensive mode of the synchronization circuit inhibits realignment when repetitive data patterns emulate the FAS pattern. Synchronization cannot occur until all emulators disappear and only one candidate for the correct frame alignment position remains.

In the ESF mode only, an on-line search procedure starts when an emulator has inhibited synchronization for 100 ms. The synchronization circuit selects one of the multiple candidate positions and checks for a correct CRC-6 pattern at this time. If the CRC-6 pattern does not match, the next candidate position is tried. The procedure repeats until the correct position is found. Each CRC-6 check takes 100 ms and each synchronization attempt takes an additional 100 ms.

When there are no emulators, the internal memory needed to implement the defensive algorithm leads to very fast synchronization; however, to avoid false reframes, the search does not end until at least 24 FAS-bit positions have been examined.

In the D4 and SL modes, the receiver has the ability to inhibit superframe synchronization and to terminate the LFA condition after terminal frame synchronization. This capability must be used with the D4 BOS and SL BOS modes. The control of superframe synchronization has not been tied to BOS mode selection; therefore, when the D4 BOS or SL BOS modes are selected, action control bit AC3 must be set.

Signaling frame synchronization is not required in the DDS mode. It is accomplished concurrently with terminal frame synchronization in ESF mode and by a separate Fs resynchronizer in the D4 and SL modes.

Tables 12—15 summarize the mean times and criteria for loss and recovery of alignment. See Tables 16 and 17 for defintions of FER, CER, LFA, and LMA. Ft:Fs indicates that the Ft and Fs patterns are interleaved

Table 12. Mean Recovery-of-Alignment Time

Alignment	Format	Mean Time*
Frame	DDS D4, SL	0.75 ms 6 ms
Superframe	D4 Ft:Fs SL	4.5 ms 21 ms
Frame/superframe	ESF	12 ms
Multiframe	BOS	9 ms

* Assumes no line errors and no frame emulators.

Table 13. Recovery-of-Alignment Criteria

Alignment	Format	Recovery Indication	Recovery Criterion
Frame	DDS	LFA off	The first unique correct combination of an Ft/Fs sequence and FAS pattern that exists for at least 6 consecutive frames
	D4 Ft	LFA off	The first unique correct Ft sequence that exists for at least 24 consecutive Ft intervals (48 frames)
	D4 Ft:Fs, SL	None	The first unique correct Ft sequence that exists for at least 24 consecutive Ft intervals (48 frames)
	ESF	LFA off	The first unique correct Fe sequence that exists for at least 24 consecutive Fe intervals (96 frames)
Superframe	D4, SL	LFA off	The first correct Fs sequence that exists for 2 consecutive superframes
Extended superframe	ESF	LFA off	Recovery of frame alignment
Multiframe	BOS	LMA off	The first correct combination of an FM sequence and MAS pattern that exists for 2 consecutive multiframes

Table 14. Mean Loss-of-Alignment Time

Alignment	Format	Mean Time*	
		True (Maximum)	False (Minimum)
Frame	DDS	—	—
Frame/superframe	D4, SL ESF LFA ESF LCC	1.1 ms 2.1 ms 96 ms	1.4 min 2.8 min 132 ms
Multiframe	BOS	—	—

* True times assume a 0.5 error rate; false times assume a 0.001 error rate.

Table 15. Loss-of-Alignment Criteria

Alignment	Format	Loss Indication	Loss Criterion
Frame	DDS D4, SL ESF	LFA on LFA on LFA on	4 FERs in 12 consecutive frames 2 FERs in 4 consecutive Ft bits 2 FERs in 4 consecutive Fe bits
Superframe	D4, SL	LFA on	Loss-of-frame alignment
Frame/superframe	ESF	LFA on	32 consecutive CERs (LCC)
Multiframe	BOS	LMA on	4 MERs in 1 multiframe or bit 7 = 1 in 2 consecutive MAS words

Facility Trouble and Alarm Processing

Fault and Alarm Detection

The criteria used to detect transmission facility faults and alarms fall into two categories: events and conditions. Event criteria activate the fault or alarm indication for each separate occurrence of the event. Condition criteria require algorithmic processing of a number of events to activate the fault or alarm indication. The indication persists until deactivated by a different event. Table 16 lists the event-activated faults and alarms detected by the 229GB Framer.

With the exception of LFVs, all event indications remain activated for one frame (125 μs). LFV indications remain activated for one TDM bit interval (648 ns).

Table 17 lists the fault and alarm conditions detected by the 229GB Framer. Condition indications remain activated for the duration of the condition.

Table 16. Transmission Facility Fault and Alarm Events

Name	Symbol	Format	Activation Criterion
Line-format violations	LFV	Bipolar	Any BPV
		B8ZS	Any BPV not in a valid violation code
Frame-alignment error	FER	D4, SL	An error in an Ft bit
		ESF	An error in an Fe bit
		DDS	An error in an Ft, Fs, or word-24, FAS bit
Multiframe alignment error	MER	BOS	An error in an Fm or frame-24, word-24, MAS bit
Change of frame alignment	CFA	All	Synchronization at a new frame alignment
CRC-6 errors	CER	ESF	One or more CRC-6 check bits in error in any extended superframe
Remote multiframe alarm	RMA	BOS	A frame-24, word-24, bit 6 (RMA) bit = 0
Remote frame alarm	RFA	DDS	A word-24, bit 6 (RFA) bit = 0
		D4	Bit 2 of all words in one frame = 0
Alarm indication signal	AIS	All	Less than three 0s in a two-frame interval

Table 17. Transmission Facility Fault and Alarm Conditions

Name	Symbol	Format	Activation Criterion
Loss-of-frame alignment	LFA	DDS	4 FERs in 12 consecutive frames
		D4, SL	2 FERs in 4 consecutive Ft bits
		ESF	2 FERs in 4 consecutive Fe bits
Loss-of-multiframe alignment	LMA	BOS	4 MERs in 1 multiframe or bit 7 = 1 in 2 consecutive MAS word
Remote frame alarm	RFA	ESF	A repeating 0x00FF pattern in the FDL after an initial 0x00 or 0xFF startup sequence
Continuing remote frame alarm	CRFA	D4 BOS	An RFA in two successive frames

Responses to Facility Trouble and Alarms

Consequent action is a CCITT term that covers responses to the detection of trouble or alarm conditions. The 229GB Framer provides two types of consequent actions: demand and automatic. Demand consequent actions are invoked by external command only; automatic consequent actions are hardware-implemented responses triggered by the detection of specific events or conditions. There are two categories of automatic consequent actions: standard and optional. Standard actions are mandatory; optional actions can be enabled or disabled by external command. Table 18 summarizes the demand consequent action capabilities of the 229GB Framer. Table 19 summarizes the automatic consequent actions.

Table 18. Demand Consequent Actions Capabilities

Name	Symbol	Format	Action
Receive signaling inhibit	RSINH	All	RSI output lead = 1
Transmit TDM squelch	XCHSQ	DDS	T1DM UC code to words 1—23
	—	Others	Idle code to all words
Transmit RFA	XRFAL	DDS	All word-24, bit 6 (RFA bit) = 0
		D4	Bit 2 of all words = 0
		ESF	Repeating 0x00ff pattern to FDL
Transmit RMA	XRMAL	BOS	All frame-24, word-24, bit 6 (RMA bit) = 0
Receive TDM squelch	RCHSQ	DDS	T1DM MOS code to words 1—23
Receive word-24 squelch	RSGSQ	BOS	AIS to word-24

Table 19. Automatic Consequent Actions

Action	Format	Trigger	Type
RSINH	All	FER, LFA	Standard
RSINH	BOS	MER, LMA	Standard
RSINH	D4 BOS	CRFA	Optional
RCHSQ	All	LFA	Optional
RSGSQ	BOS	RSINH	Optional

The receiver side of the framer activates receive signaling inhibit (RSIGN) for a one-frame interval after each detected FER and/or MER and for the duration of each LFA and/or LMA condition. In the D4 BOS mode, it activates RSINH for the duration of each CRFA condition if the automatic response is enabled.

Each time a signaling bit is received, the receive synchronizer transfers that bit's previous value to back-up storage. When the RSI lead is set (RSINH is activated), the receive synchronizer freezes the signaling states at the back-up values and maintains this state for 32 frames after the RSI lead is cleared (RSINH is deactivated). The RSGSQ capability is a means of passing on the RSINH function in applications that do not use the signaling extraction capabilities of the receive synchronizer.

System Status Monitoring

Device Duplication and Match Alarms

The principal technique used for internal device fault monitoring are duplication and match circuitry. This technique checks output signals for internally generated errors and checks synchronizers and facility monitor detectors for algorithm failures. Table 20 lists the 229GB Framer duplication and match alarms. Table 21 lists the interface signal checks performed by the framer.

Table 20. Device Duplication and Match Alarms

Symbol	Format	Activation Criterion
TDNMM	All	Transmit TDM output data mismatch
TFDCMM	Non-D4	Transmit FDL output clock mismatch
RIDMM	All	Receive TDM output data mismatch
RFDMM	Non-D4	Receive FDL output data mismatch
RFDCMM	Non-D4	Receive FDL output clock mismatch
RSSPMM	D4, SL	Receive superframe synchronizer pulse mismatch
LFVDMM	All	LFV detector output mismatch
FERDMM	All	FER detector output mismatch
LMADMN	BOS	LMA detector output mismatch
RMADMM	BOS	RMA detector output mismatch
RFADMM	All	RFA detector output mismatch
AISDMM	All	AIS detector output mismatch

Table 21. Device Interface Fault-Condition Alarms

Symbol	Format	Activation Criterion
TPRPER	All	Transmit pseudorandom pattern error on TID
TLOSA	SL	Transmit loss-of-superframe alignment on TFD
TLOCLK	All	Transmit loss-of-clock on TICLK
RLOCLK	All	Receive loss-of-clock on RLCLK
SCSPER	All	Control stream parity error on SCS

Diagnostic Exercises

The 229GB Framer provides five categories of diagnostic exercises to ensure that the device can detect and/or report faults and alarms. Exercises 1—6, which do not affect service, check the system fault detection circuits without affecting normal operation. Exercises 8, 9, and 13—15 check the facility monitor circuits but do not affect normal data processing. Exercise 11 effects data processing by forcing the receiver input data stream to all 0s. The null exercise, 0, clears any other exercise and its responses. Exercises 7, 10, and 12 have no function. The response time for any exercise depends on the fault or alarm condition that it forces.

Table 22 lists the system status exercises and their expected responses. Tables 23 and 24 list the facility status exercises and their expected responses for non-BOS and BOS modes. Two exercises are required to fully check most duplicate and match circuits. The response to an exercise that does not affect service and that checks a facility monitor circuit may be inhibited when the corresponding facility fault or alarm indication is activated.

Table 22. System Status Exercise Responses

Exercise	Format	Activated Response	
		Report Bit	Reported Condition
0	All	None	None (clears all fault and alarm indications)
1	All	SR1, SR2	TLOCLK, LFVDMM
	All	SR3, SR4[1]	FERDMM, RFADMM
	Non-D4	SR5, SR7[2]	TFDCMM, TDNMM
2	All	SR1, SR2	TLOCLK, LFVDMM
	All	SR3, SR4[1]	FERDMM, RFADMM
	Non-D4	SR7[2]	TDNMM
3, 4	All	SR1	TLOPRP
	All	SR3[3], SR4	LMADMM, RMADMM
	All	SR7	TDMNN
5	All	SR1	RLOCLK
	All	SR3	RSSPMM
	All	SR4	AISDMM
	All	SR5	RFDCMM
	Non-D4	SR6[2]	RFDMM
	All	SR7	RIDMM
6	All	SR1	RLOCLK
	All	SR3	RSSPMM
	All	SR4	AISDMM
External	SL	SR0[4]	TLOSA
	All	SR2[5]	SCSPER

[1] May not respond if exercised during an RFA condition.
[2] May not respond if exercised while the FDL is inactive.
[3] May not respond if exercised during an LMA condition.
[4] TLOSA may be exercised by sending an incorrect Fs pattern to the FDL.
[5] SCSPER may be exercised by sending bad parity on the SCS.

Table 23. Facility Status Exercise Responses in Non-BOS Modes

Exercise	Format	Activated Response		
		Report Bit	Report Lead	Reported Condition
0	All	None	None	None
8	All	FR0	RLV	LFV
	ESF	FR4	RCEMA	CER
	ESF	FR5	None	LCC*
	D4, DDS	FR6	RRFMA	RFA
	ESF	FR6	RRFMA	CRFA
9	All	FR7	None	AIS
11	All	FR1	RFECE	FER
	All	FR2	RLF	LFA
	ESF	FR4	RCEMA	CER
	D4, DDS	FR6	RRFMA	RFA
	All	None	RSI	FER, LFA
13	All	FR1	RFECE	FER
	All	FR2	RLF	LFA
14	All	FR1	RFECE	FER
	All	FR2	RLF	LFA
	DDS, ESF	FR3	None	CFA
15	ESF	FR3*, **	None	CFA
	ESF	FR5	None	LCC

* Response may require more than 150 ms to activate.
** Response activates only if an FAS emulator is present.

Table 24. Facility Status Exercise Responses in BOS Modes

Exercise	Format	Activated Response		
		Report Bit	Report Lead	Reported Condition
0	All	None	None	None
8	All	FR0	RLV	LFV
	ESF	FR1	RFECE	CER
	ESF	FR6	RRFMA	CRFA
	All	FR5	RRFMA	RMA
	D4, DDS	FR6	RRFMA	RFA
9	All	FR7	None	AIS
11	Non-ESF	FR1	RFECE	FER
	ESF	FR1	RFECE	CER
	All	FR2	RFL	LFA
	All	FR4	RCEMA	LMA
	All	FR5	RRFMA	RMA
	D4, DDS	FR6	RRFMA	RFA
	All	None	RSI	FER, LFA
	All	None	RSI	MER, LMA
	D4 BOS	None	RSI	CRFA*
13	Non-ESF	FR1	RFECE	FER
	ESF	FR1	RFECE	CER
	All	FR2	RLF	LFA
	All	FR4	RCEMA	LMA
14	Non-ESF	FR1	RFECE	FER
	ESF	FR1	RFECE	CER
	All	FR2	RLF	LFA
	DDS, ESF	FR3	None	CFA
	BOS	FR4	RCEMA	LMA
15	ESF	FR3**	None	CFA

* Responds only when action control bit AC2 is set.
** Response may require more than 150 ms to activate. Response activates only if an FAS emulator is present.

Control and Status

Serial Control Stream

Control and maintenance commands to the 229GB Framer are input on SCS at a 1.024-Mb/s rate. The commands are organized into groups of 8-bit bytes and are accepted on SCS when CTLE is held high. The last eight bits entered are stored as a command byte; preceding bits are ignored. Once a command has been entered, it remains in effect until explicitly changed. Command bytes may have an arbitrary phase in relation to SSYN. Control bytes consist of four types: option, exercise, consequent action, and action control bytes.

As illustrated in Figure 3, each control byte consists of eight bits, labeled CB0—CB7. CB7 (MSB) is a parity bit that forces odd parity across the entire byte. Control bits 4, 5, and 6 (CB4—CB6) determine the control byte type.

An option byte is selected when CB6 = 0. For this byte, bit positions CB0—CB5 are relabeled OP0—OP5, respectively, and are used to select individual 229GB Framer options. BOS mode is selected when OP0 = 1. OP1—OP5 are used to select line format and frame format structures, as listed in Table 25.

In the DDS TDM mode, FDL processing is inactive; in the DDS FDL mode, FDL data is copied to and from word-24, bit 7.

Table 25. Option-Byte Bit Assignments

OP5*	OP4*	OP3*	OP2*	OP1*	OP0*	Word-24	ZCS	Line Format	Frame Format
x	x	0	x	x	0	Transparent			
x	x	0	x	x	1	BOS	—	—	—
x	x	1	x	x	x	DDS FAS word			
x	x	x	0	0	x	—	Off	—	—
x	x	x	1	0	x		On		
x	x	x	x	0	x	—	—	Bipolar	—
x	x	x	x	1	x			B8ZS	
0	0	0	x	x	x				D4
1	0	0	x	x	x				SL
x	1	0	x	x	x	—	—	—	ESF
x	0	1	x	x	x				DDS TDM
x	1	1	x	x	x				DDS FDL

* x = don't care.

Tables 26—29 list the exercise, consequent action, and action control bit assignments.

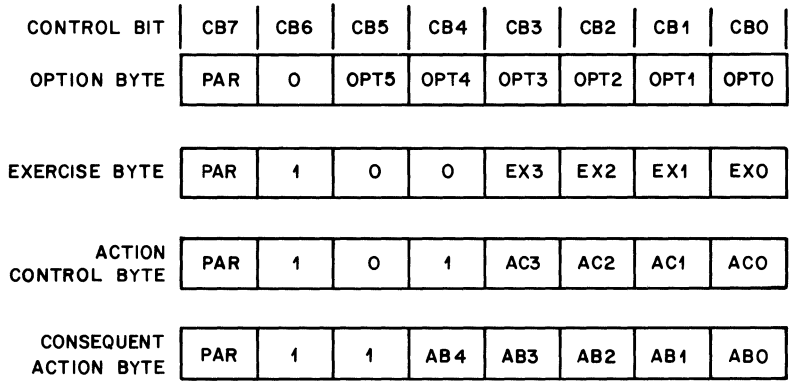


Figure 3. Control Byte Formats

Table 26. Exercise-Byte Bit Assignments

EX3	EX2	EX1	EX0	Exercise Number
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
1	0	0	0	8
1	0	0	1	9
1	0	1	1	11
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 27. Demand Consequent-Action-Byte Bit Assignments in Non-BOS Modes

AB4*	AB3*	AB2*	AB1*	AB0*	DDS	D4	SL	ESF
x	x	x	x	1	RCHSQ	RCHSQ	RCHSQ	RCHSQ
x	x	x	1	x	RDLSQ	—	RDLSQ	RDLSQ
x	x	1	x	x	XRFAL	XRFAL	—	XRFAL
x	1	x	x	x	XDLSQ	—	—	XDLSQ
1	x	x	x	x	XCHSQ	XCHSQ	XCHSQ	XCHSQ

* x = don't care.

Table 28. Demand Consequent-Action-Byte Bit Assignments in BOS Modes

AB4*	AB3*	AB2*	AB1*	AB0*	D4 BOS	SL BOS	ESF BOS
x	x	x	x	1	RCHSQ	RCHSQ	RCHSQ
x	x	x	1	x	RSGSQ	RSGSQ	RSGSQ
x	x	1	x	x	XRFAL	—	XRFAL
x	1	x	x	x	XRMAL	XRMAL	XRMAL
1	x	x	x	x	XCHSQ	XCHSQ	XCHSQ

* x = don't care.

Table 29. Action-Control-Byte Bit Assignments

AC3*	AC2*	AC1*	AC0*	Format	Action	Trigger
x	x	x	1	All	RCHSQ	LFA
x	x	1	x	BOS	RSGSQ	RSINH
x	1	x	x	D4 BOS	RSINH	CRFA
1	x	x	x	D4, SL	Inhibit super-frame sync	N/A

* x = don't care.

In the 229GB Framer, the action control byte is used to control the optional automatic consequent actions and to inhibit superframe synchronization in the D4 BOS and SL BOS modes. Bits AC0, AC1, and/or AC2 must be set to enable the consequent actions; bit AC3 must be set when the D4 BOS or SL BOS mode is selected. All unused bits should be cleared.

Status Report Mechanisms. Facility fault and alarm reports are available on both the serial report stream bits (FR0—FR7) and on the external report leads. System status alarms are reported only on the report stream. For maintenance purposes, the report stream provides a means of auditing the contents of the device's internal control registers previously set or cleared by serial control commands and/or option select pins. The device outputs the serial report stream on SRS at a 1.024-Mb/s rate in fixed relationship to SSYN.

A serial report stream contains six report byte types (illustrated in Figure 4), organized into a serial report frame consisting of 16 bytes (illustrated in Figure 5).

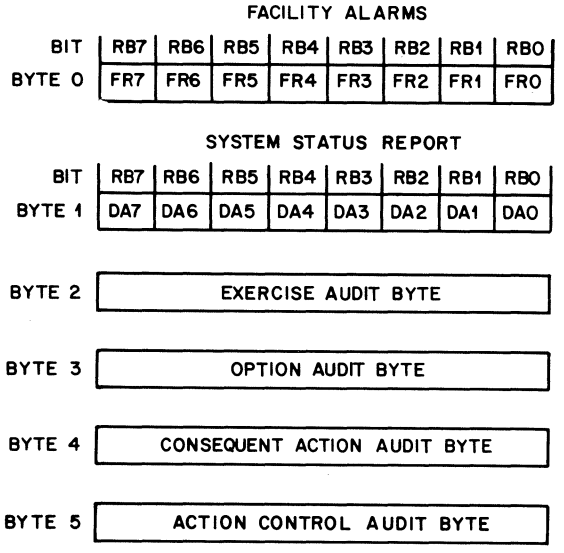


Figure 4. Report Byte Formats

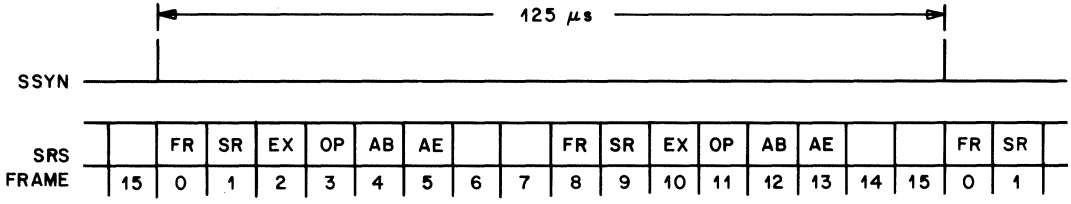


Figure 5. Serial Report Stream Frame Format

A facility report byte is transmitted at the start of each frame. The next five bytes consist of a system status (device alarms) report, exercise audit, option audit, consequent action audit, and action control audit byte, respectively. Two null bytes, all 0s, are then transmitted, followed by the retransmission of the previous eight bytes. The lower-order bit is transmitted first for each byte output on SRS. (See Tables 30—32.)

The second report mechanism in the 229GB Framer is the dedicated report lead. (See Tables 33 and 34.)

Table 30. Facility Status Report-Byte Bit Assignments in Non-BOS Modes

FR7*	FR6*	FR5*	FR4*	FR3*	FR2*	FR1*	FR0*	Format	Report
x	x	x	x	x	x	x	1	All	LFV
x	x	x	x	x	x	1	x	All	FER
x	x	x	x	x	1	x	x	All	LFA
x	x	x	x	1	x	x	x	All	CFA
x	x	x	1	x	x	x	x	ESF	CER
x	x	1	x	x	x	x	x	ESF	LCC
x	1	x	x	x	x	x	x	D4, DDS	RFA
								ESF	CRFA
1	x	x	x	x	x	x	x	All	AIS

* x = don't care.

Table 31. Facility Status Report-Byte Bit Assignments in BOS Modes

FR7*	FR6*	FR5*	FR4*	FR3*	FR2*	FR1*	FR0*	Format	Report
x	x	x	x	x	x	x	1	All	LFV
x	x	x	x	x	x	1	x	Non-ESF	FER
								ESF	CER
x	x	x	x	x	1	x	x	All	LFA
x	x	x	x	1	x	x	x	All	CFA
x	x	x	1	x	x	x	x	All	LMA
x	x	1	x	x	x	x	x	All	RMA
x	1	x	x	x	x	x	x	D4	RFA
								ESF	CRFA
1	x	x	x	x	x	x	x	All	AIS

* x = don't care.

Table 32. System Status Report-Byte Bit Assignments

SR7*	SR6*	SR5*	SR4*	SR3*	SR2*	SR1*	SR0*	Format	Report
x	x	x	x	x	x	x	1	SL	TLOSA
x	x	x	x	x	x	1	x	All	TPRPER, TLOCLK RLOCLK
x	x	x	x	x	1	x	x	All	SCSPER, LFVDMM
x	x	x	x	1	x	x	x	All	FERDMM
								D4, SL	RSSPMM
								BOS	LMADMM
x	x	x	1	x	x	x	x	All	AISDMM, RFADMM
								BOS	RMADMM
x	x	1	x	x	x	x	x	Non-D4	TFDCMM, RFDCMM
x	1	x	x	x	x	x	x	Non-D4	RFDMM
1	x	x	x	x	x	x	x	All	TDNMM, RIDMM

* x = don't care.

Table 33. Facility Status Report-Lead Assignments in Non-BOS Modes

Report Lead	Format	Report
RLV	All	LFV
RFECE	All	FER
RLF	All	LFA
RCEMA	ESF	CER
RRFMA	D4, DDS	RFA
	ESF	CRFA
RSI	All	FER, LFA

Table 34. Facility Status Report-Lead Assignments in BOS Modes

Report Lead	Format	Report
RLV	All	LFV
RFECE	Non-ESF	FER
	ESF	CER
RLF	All	LFA
RCEMA	BOS	LMA
RRFMA	D4	RFA
	ESF	CRFA
	All	RMA
RSI	All	FER, LFA
	All	MER, LMA
	D4	CRFA*

* Responds only when action control bit AC2 is set.

Characteristics

Clocks

Clock	Period	Tolerance	Unit	Duty Cycle*	Mode
RLCLK	648	100 ± 2%	ns	50 ± 5%	All
RICLK	648	100 ± 1%	ns	50 ± 8%	All
SCLK	244	100 ± 1%	ns	50 ± 5%	All
RFDCLK	125	—	μs	50 ± 1%	DDS
	250	—	μs	25 ± 1%	SL, ESF
TFDCLK	125	—	μs	50 ± 1%	DDS
	250	—	μs	75 ± 1%	SL, ESF

* Duty cycle = zero-level duration/(clock period)*100.

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, GRD = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Supply current	I_{DD}	—	140	295	mA
Input current:					
low	I_{IL}	—	—	–20	μA
high	I_{IH}	20	—	—	μA
Output current:					
low	I_{OL}	—	—	2.2	mA
high	I_{OH}	—	—	0.2	mA
Input voltage:					
low	V_{IL}	—	—	0.7	V
high	V_{IH}	2.4	—	—	V
Output voltage:					
low	V_{OL}	—	—	0.4	V
high	V_{OH}	2.4	—	—	V
Power dissipation	PD	—	0.7	1.4	W

Maximum Ratings

DC supply voltage (V_{DD}) range ..... –0.5 to +7 V
Power dissipation (PD) ..... 2 W
Storage temperature (Tstg) range ..... –40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit	Mode
tSCHTCH	Skew time SCLK to TICLK	–122	10	142	ns	All
tSSHSSL	SSYN pulse duration	—	244	—	ns	All
tSSHTCH	Pulse set-up time SSYN to TICLK	40	—	—	ns	All
tTCHSSL	Pulse hold time TICLK to SSYN	50	—	—	ns	All
tSSHSCH	Pulse set-up time SSYN to SCLK	40	—	—	ns	All
tSCHSSL	Pulse hold time SCLK to SSYN	70	—	—	ns	All
tRPVRCH	Data set-up time RPDN to RLCLK	236	—	—	ns	All
tRNVRCH	Data set-up time RNDN to RLCLK	236	—	—	ns	All

Symbol	Description	Min	Typ	Max	Unit	Mode
tRCHRPX	Data hold time RLCLK to RPDN	286	—	—	ns	All
tRCHRNX	Data hold time RLCLK to RNDN	286	—	—	ns	All
tRCLRDV	Propagation delay RLCLK to RID	0	—	180	ns	All
tRCLRSH	Propagation delay RLCLK to RISYN	0	—	180	ns	All
tRCLRSL	Propagation delay RLCLK to RISYN	0	—	180	ns	All
tTDVTCH	Data set-up time TID to TICLK	149	—	—	ns	All
tTCHTDX	Data hold time TICLK to TID	269	—	—	ns	All
tTCLTSV	Propagation delay TICLK to TISYN	0	—	180	ns	All
tTCHTPV	Propagation delay TICLK to TPDN	0	—	190	ns	All
tTCHTNV	Propagation delay TICLK to TNDN	0	—	190	ns	All
tTCHTLL	Propagation delay TICLK to TLCLK	0	—	150	ns	All
tTCLTLH	Propagation delay TICLK to TLCLK	0	—	150	ns	All
tRKLRFV	Skew time RFDCLK to RFD	−4	0	4	µs	All
tTKLTKL	TFDCLK clock period	124	125	126	µs	DDS
tTKLTKL	TFDCLK clock period	248	250	252	µs	SL, ES
tTKHTKL	TFDCLK duty cycle	24	25	26	%	All
tTFVTKH	Data set-up time TFD to TFDCLK	2	—	—	µs	All
tTKHTFX	Data hold time TFDCLK to TFD	2	—	—	µs	All
tCSVCSV	SCS time-slot period	—	976	—	ns	All
tSRVSRV	SRS time-slot period	—	976	—	ns	All
tCSVSCH	Data set-up time SCS to SCLK	244	—	—	ns	All
tCEVSCH	Data set-up time CTLE to SCLK	244	—	—	ns	All
tSCHCSX	Data hold time SCLK to SCS	244	—	—	ns	All
tSCHCEX	Data hold time SLCK to CTLE	244	—	—	ns	All
tSCHSRV	Propagation delay SCLK to SRS	0	—	300	ns	All
tRCLRVV	Propagation delay RLCLK to RLV	0	—	250	ns	All
tRCLREV	Propagation delay RLCLK to RFECE	0	—	2	µs	All
tRCLRLV	Propagation delay RLCLK to RLF	0	—	2	µs	All
tRCLRAV	Propagation delay RLCLK to RCEMA	0	—	2	µs	All
tRCLRMV	Propagation delay RLCLK to RRFMA	0	—	2	µs	All
tRCLRIV	Propagation delay RLCLK to RSI	0	—	2	µs	All

Timing Diagrams

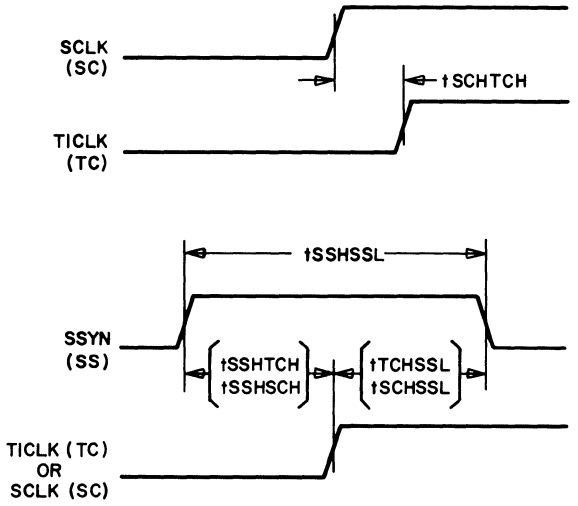


Figure 6. Clock Signals

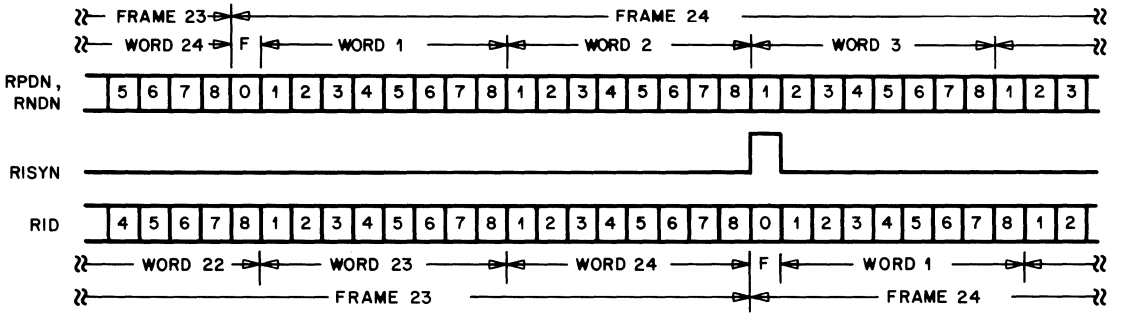


Figure 7. Receiver TDM Timing (DS1 Mode)

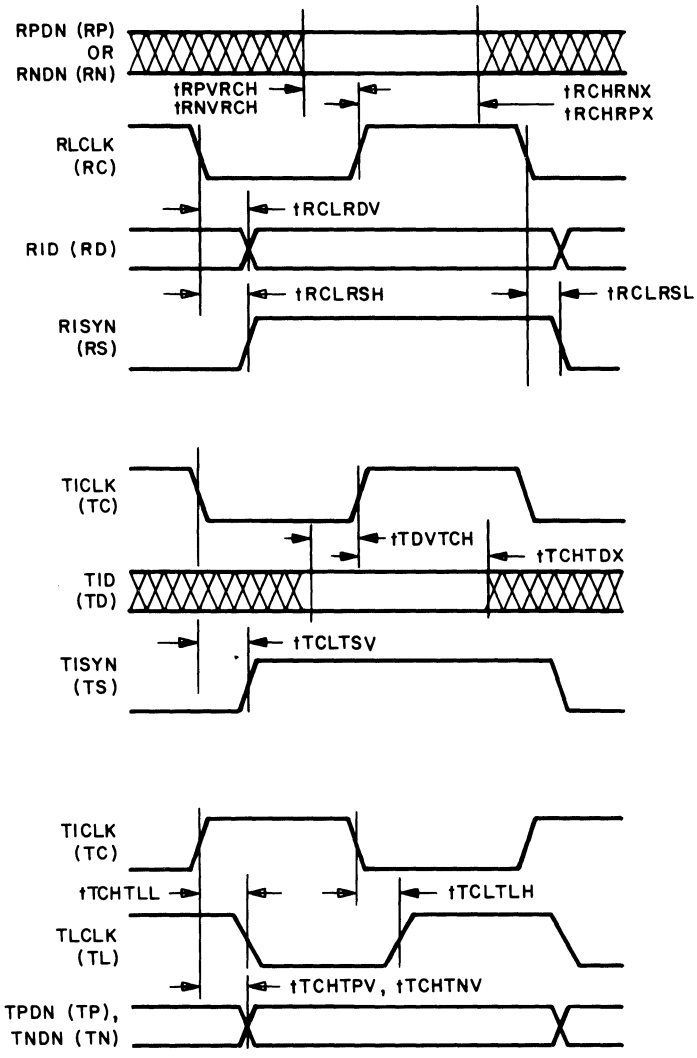


Figure 8. Line Rate I/O Signals

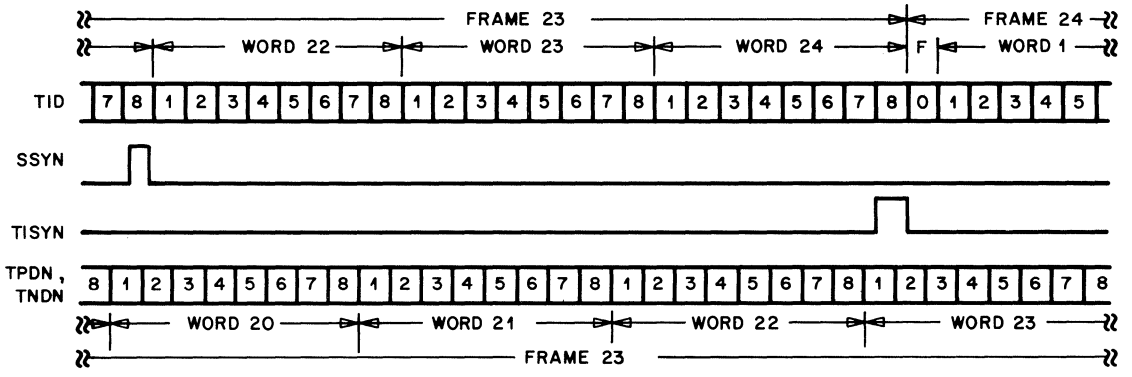
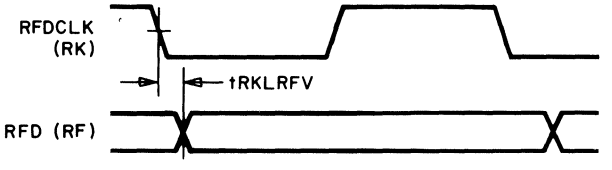


Figure 9. Transmitter TDM Timing (DS1 Mode)



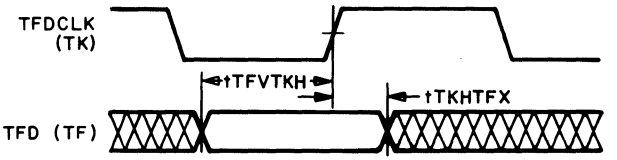


Figure 10. Facility Data Link Clocks and Data

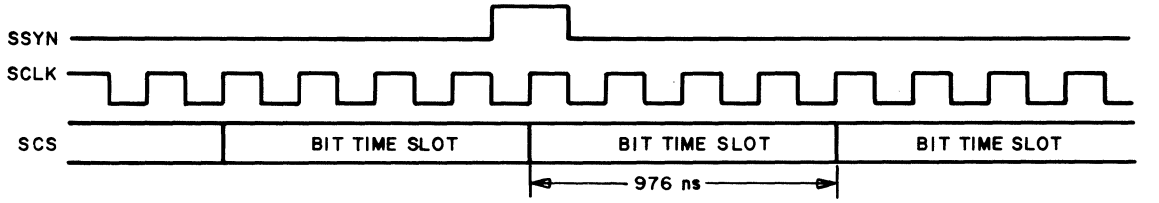


Figure 11. Serial Control Stream Bit Timing

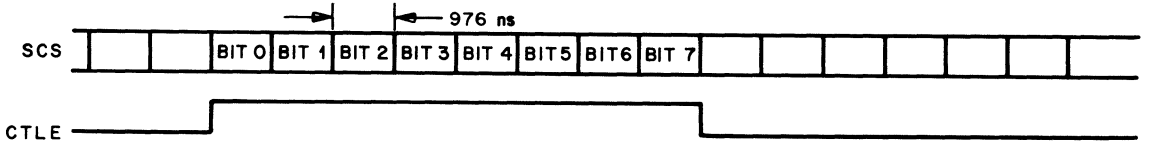


Figure 12. Serial Control Stream Byte Timing

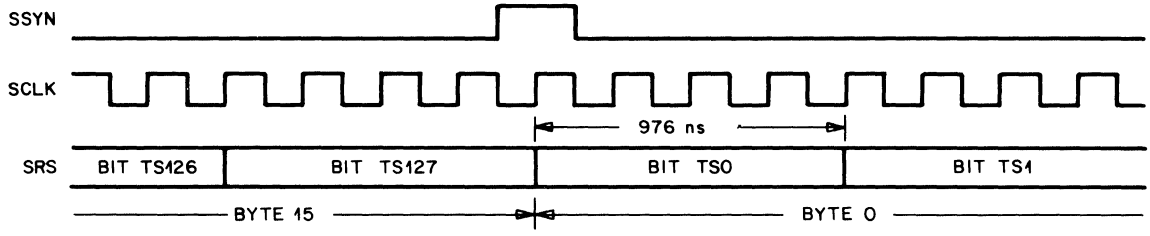


Figure 13. Serial Report Stream Bit Timing

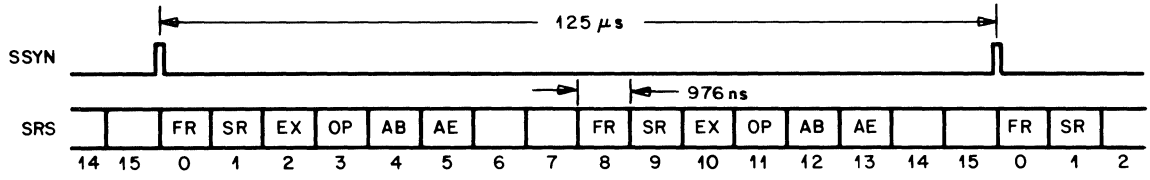


Figure 14. Serial Report Stream Frame Timing

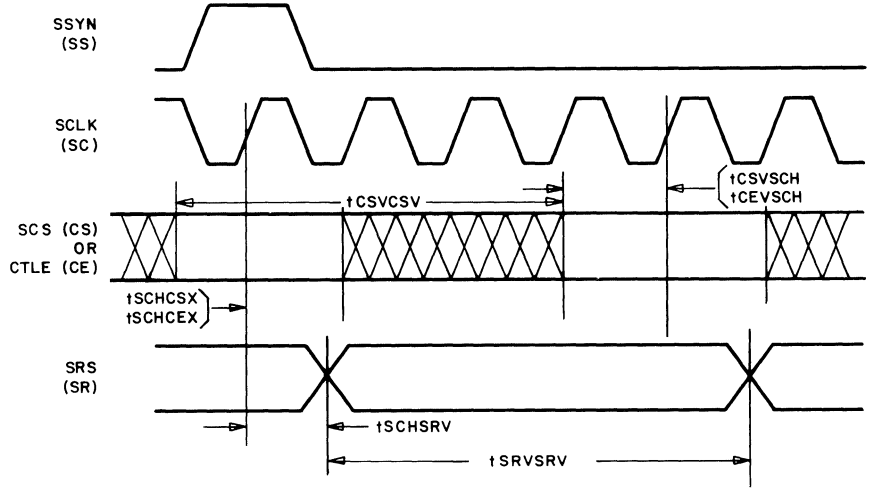


Figure 15. Serial Stream I/O

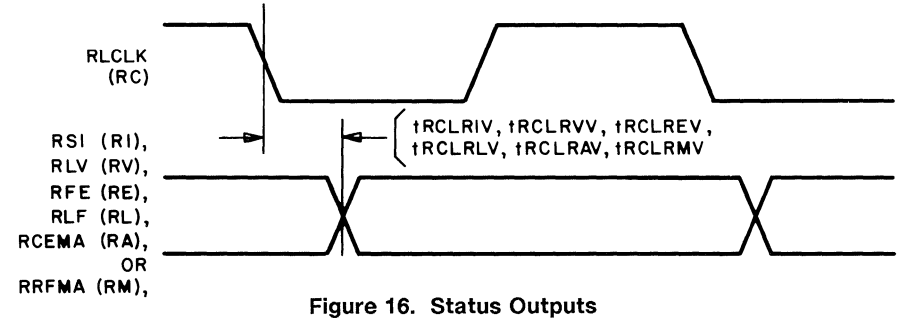


Figure 16. Status Outputs

257AL Transmit Formatter

Features

- 2-, 4-, 16-state signaling or inhibit signaling
- Selectable DS1 (1.544 Mb/s) or CEPT (2.048 Mb/s) formats
- Variable F-bit and parity-bit delays
- TTL-compatible

Description

The 257AL Transmit Formatter integrated circuit converts 14 bits of parallel data (8 traffic bits, 5 signaling bits, and 1 parity bit) into a serial stream. It is manufactured using NMOS technology, requires a single 5 V supply, and is available in a 32-pin plastic DIP.

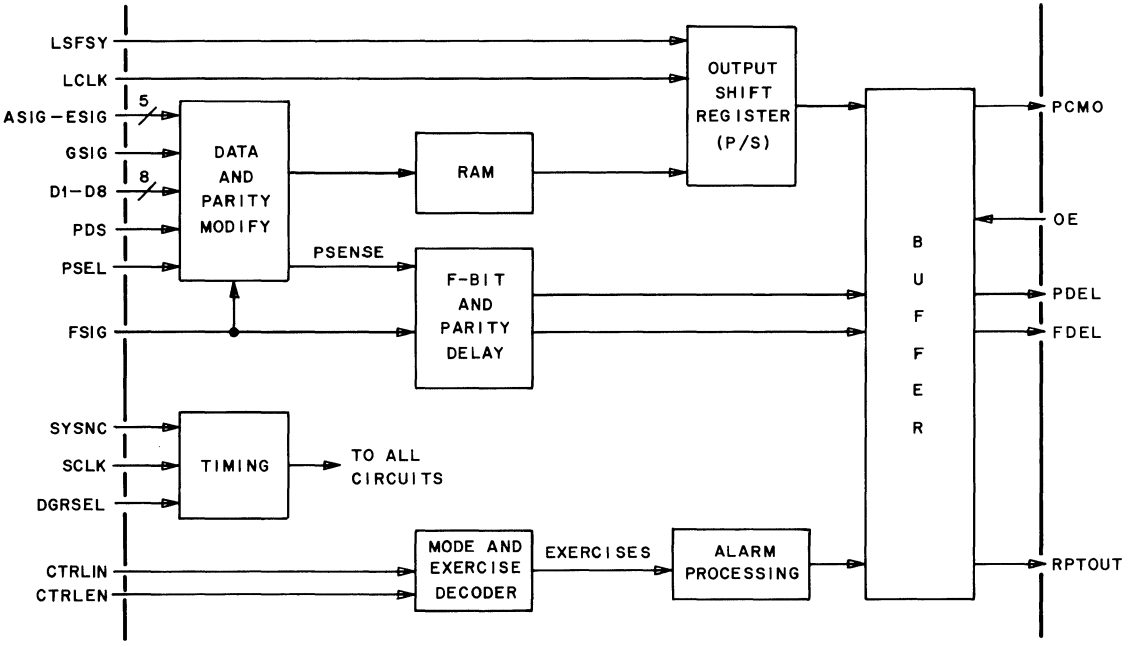
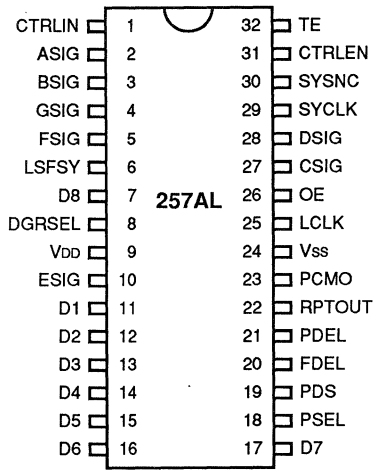


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
ASIG	2	LCLK	25
BSIG	3	LSFSY	6
CSIG	27	OE	26
CTRLEN	31	PCMO	23
CTRLIN	1	PDEL	21
D1—D7	11—17	PDS	19
D8	7	PSEL	18
DGRSEL	8	RPTOUT	22
DSIG	28	SYCLK	29
ESIG	10	SYSNC	30
FDEL	20	$\overline{TE}$	32
FSIG	5	VDD	9
GSIG	4	Vss	24

Figure 2. Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	CTRLIN	I	**Serial Control Stream.** Control information is input on this pin at a rate of 1.024 MHz. This information determines input and output formats.
2 3	ASIG BSIG	I I	**A Signaling Bit.** **B Signaling Bit.**
4 5	GSIG FSIG	I I	**G and F Signaling Control Bits.** These bits control insertion in the robbed digit-8 modes.
6	LSFSY	I	**Line Superframe Synchronization.** A high pulse on this pin identifies the first frame of a superframe in DS1 mode and a multiframe in CEPT mode. This is a line-side timing signal transmitted by the framer.
7	D8	I	**Data Bit 8.** Eighth bit of parallel data from the system is input on this pin.
8	DGRSEL	I	**Di-Group Select.** Used only in DS1 (1.024 MHz) burst output mode to select input data. This pin must be held high or left unconnected for all other modes.
9	VDD	—	**5 V Supply.**
10	ESIG	I	**E Signaling Bit.**

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
11—17	D1—D7	I	**Data Bits 1—7.** Parallel data from the system is received on these 7 pins.
18	PSEL	I	**Parity Selection.** A high on this pin inverts the delayed parity sense bit, PDEL.
19	PDS	I	**Parity.** Parity over data and signaling bits.
20	FDEL	O	**Delayed Signaling Control Bit.**
21	PDEL	O	**Parity Sense Bit.**
22	RPTOUT	O	**Serial Report Stream.** Serial output of internal alarm status at a 1.024-MHz rate.
23	PCMO	O	**PCM Output.** Serial output stream to the framer. PCMO uses on-line timing.
24	V_{SS}	—	**Ground.**
25	LCLK	I	**Line Clock.** The transmit line clock is input on this pin. It is 1.544 MHz for DS1 systems, 2.048 MHz for CEPT systems.
26	OE	I	**Output Enable.** A high enables all outputs; a low 3-states all outputs.
27 28	CSIG DSIG	I I	**C Signaling Bit.** **D Signaling Bit.**
29	SYCLK	I	**System Clock.** This 4.096-MHz clock provides the timing used throughout this device.
30	SYSNC	I	**System Frame Synchronization.** A high pulse on this pin marks the first channel of data in each frame. SYSNC uses system-side timing.
31	CTRLEN	I	**Control Enable.** The serial control stream, SCS, is shifted into the transmit formatter while this input is high.
32	$\overline{TE}$	I	**Test Enable.** When low, the device is in test mode. For normal operation, this pin must be tied high or left unconnected.

Operation

The 257AL Transmit Formatter is part of an LSI digital facility interface (DFI) chip set that also includes the T7229 (replaces the 229CG) or 229GB Primary Access Framer and the 257AU Receive Synchronizer. The transmit formatter converts eight bits of parallel traffic data and five bits of signaling data into a serial bit output stream.

The transmit formatter operates in either DS1 or CEPT mode. In both modes, parallel traffic data is input on D1—D8 and signaling information on ASIG—ESIG. A system synchronization pulse, input on SYSNC, marks the first channel of data in each frame. DS1 and CEPT frame formats are listed in Table 2.

Table 2. Input Frame Formats

DS1 Uniform Stuffing Format. Twenty-four traffic channels are contained within a 32-time-slot frame. The input is divided into eight groups of four time slots each, with three traffic time slots and one stuffed (idle) time slot per group. Each time slot is 3.90625 μs in duration.
DS1 Burst Stuffing Format. Twenty-four traffic channels are contained within the first 24 time slots of a 32-time-slot frame. The last eight time slots contain an idle code. Each time slot is 3.90625 μs in duration.
DS1 1.024-MHz Burst Input Format. Twenty-four traffic channels are contained within a 128-time-slot frame. DGRSEL is asserted when the 24th traffic channel burst is present. Each time slot is 976.5625 ns in duration.
CEPT Format. Thirty-two traffic channels are contained within a 32-time-slot frame. Each time slot is 3.90625 μs in duration.

Table 3. Selection of Uniform Stuffing Idle Time Slots

MD1	MD0	Pattern Number	Stuffed Time Slots
0	0	0	0, 4, 8, 12, 16, 20, 24, 28
0	1	1	1, 5, 9, 13, 17, 21, 25, 29
1	0	2	2, 6, 10, 14, 18, 22, 26, 30
1	1	3	3, 7, 11, 15, 19, 23, 27, 31

DS1 Mode

Figure 3 illustrates the DS1 mode idle code bit pattern. The eight time slots selected for idle code insertion are determined by the state of bits MD0 and MD1 of the option select control byte input on TSCS, as listed in Table 3.

In DS1 mode, the output bit stream is based on a 24-frame superframe. Each frame consists of 193 bits organized as one framing bit followed by twenty-four 8-bit (one byte) time slots. In this mode, the serial bit stream is output on PCMO at a 1.544-Mb/s rate. Superframe alignment with the framer is established by a 3-ms synchronization signal input on LSFSY.

The pseudorandom bit pattern illustrated in Figure 4 is inserted into the frame bit positions of the serial bit stream output on PCMO.

In DS1 mode, the A—E signaling bits are inserted into the output data bit stream, using either robbed-bit or common-channel signaling formats, as selected by the option control byte input on SCS.

	TRAFFIC BITS								SIGNALING BITS					PARITY
BIT	D1	D2	D3	D4	D5	D6	D7	D8	A	B	C	D	E	P
CODE	0	1	1	1	1	1	1	1	0	0	0	0	1	P

Figure 3. DS1 Mode Idle Code

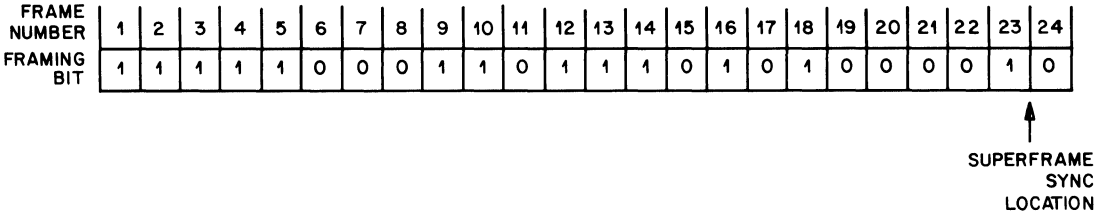


Figure 4. DS1 Mode Pseudorandom Framing Pattern

The robbed-bit format used in DS1 mode consists of substituting the appropriate signaling bit (A, B, C, or D) into bit 8 of each time slot during frames 6, 12, 18, and 24. The E signaling bit is not used in this mode. The inserted signaling bit is determined on a per-channel basis from the states of FSIG and GSIG, as listed in Table 4.

The robbed-bit format used in the DS1 *SLC* 96 Carrier System mode consists of substituting the appropriate logical combination of the signaling bits (A, B, C, or D) into bit 8 of each time slot during frames 6, 12, 18, and 24. The E signaling bit is not used in this mode. The F and G bits must be set to F = 1 and G = 0 for this mode to function properly. The inserted signaling bit for each channel follows one of two sequences, as listed in Table 5.

In DS1 mode common-channel signaling (RSM) format, time-slot 24 of each output frame is used to transmit the signaling bits for all other channels, as listed in Table 6. The F bit must be 0 and the G bit 1 for this mode to operate properly.

CEPT Mode

In CEPT mode, the output serial bit stream is transmitted on PCMO at a rate of 2.048 Mb/s. Multiframe alignment is established by a 2-ms synchronization signal input on LSFSY.

In CEPT mode, the output serial bit stream is based on a 16-frame multiframe. Each frame consists of thirty-two 8-bit (one byte) time slots. Traffic data for channels 1—15 is contained in time-slots 1—15, respectively; traffic data for channels 16—30 is contained in time-slots 17—31, respectively. The contents of time-slots 0 and 16 are dependent on the signaling mode. Tables 7 and 8 list the interdevice data formats output by the transmit formatter for the CEPT signaling modes. The F and G bits must be in either of two states for these modes to operate properly. If F = 0 and G = 0, the A—D signaling bits for each channel are inserted in time-slot 16 and the E bit (RSM mode only) is inserted in time-slot 0 in the appropriate frames. If F = 0 and G = 1, time-slot 16 is transparent to the transmit formatter; the A—D signaling bits are not inserted in time-slot 16. However, the E bit is inserted in time-slot 0 if the mode is RSM.

Table 4. DS1 Robbed-Bit Signaling Mode Selection and Bit Insertion

FSIG	GSIG	Signaling Mode	Frame Number 6	12	18	24
0	0	16-state	A	B	C	D
0	1	Inhibit	—	—	—	—
1	0	4-state	A	B	A	B
1	1	2-state	A	A	A	A

Table 5. DS1 *SLC* 96 Carrier System Signaling Insertion

Frame Number	Inserted Signaling Bit	
6	A	A or C
12	B	B or D
18	A or C	A
24	B or C	B

Table 6. DS1 Mode Common-Channel Signaling RSM Format

Frame Number	Time-Slot-24 Bits*							
	8	7	6	5	4	3	2	1
1	E1	1	0	D1	C1	B1	A1	A13
2	E2	1	0	D2	C2	B2	A2	A14
3	E3	1	0	D3	C3	B3	A3	A15
4	E4	1	0	D4	C4	B4	A4	A16
5	E5	1	0	D5	C5	B5	A5	A17
6	E6	1	0	D6	C6	B6	A6	A18
7	E7	1	0	D7	C7	B7	A7	A19
8	E8	1	0	D8	C8	B8	A8	A20
9	E9	1	0	D9	C9	B9	A9	A21
10	E10	1	0	D10	C10	B10	A10	A22
11	E11	1	0	D11	C11	B11	A11	A23
12	E12	1	0	D12	C12	B12	A12	A24
13	E13	1	0	D13	C13	B13	A13	A1
14	E14	1	0	D14	C14	B14	A14	A2
15	E15	1	0	D15	C15	B15	A15	A3
16	E16	1	0	D16	C16	B16	A16	A4
17	E17	1	0	D17	C17	B17	A17	A5
18	E18	1	0	D18	C18	B18	A18	A6
19	E19	1	0	D19	C19	B19	A19	A7
20	E20	1	0	D20	C20	B20	A20	A8
21	E21	1	0	D21	C21	B21	A21	A9
22	E22	1	0	D22	C22	B22	A22	A10
23	E23	1	0	D23	C23	B23	A23	A11
24	E24	1	0	D24	C24	B24	A24	A12

* A*i*—E*i* denote per-channel signaling bits, where *i* denotes channel number.

Table 7. Interdevice Formats for All CEPT Modes Except RSM

Frame Number	Time-Slot-0 Bit* 8 7 6 5 4 3 2 1	Time-Slot-16 Bits** 8	7	6	5	4	3	2	1
0	x x x x x 1 x x	x	x	x	x	x	x	x	x
1	x x x x x 1 x x	D16	C16	B16	A16	D1	C1	B1	A1
2	x x x x x 1 x x	D17	C17	B17	A17	D2	C2	B2	A2
3	x x x x x 1 x x	D18	C18	B18	A18	D3	C3	B3	A3
4	x x x x x 1 x x	D19	C19	B19	A19	D4	C4	B4	A4
5	x x x x x 0 x x	D20	C20	B20	A20	D5	C5	B5	A5
6	x x x x x 0 x x	D21	C21	B21	A21	D6	C6	B6	A6
7	x x x x x 0 x x	D22	C22	B22	A22	D7	C7	B7	A7
8	x x x x x 1 x x	D23	C23	B23	A23	D8	C8	B8	A8
9	x x x x x 1 x x	D24	C24	B24	A24	D9	C9	B9	A9
10	x x x x x 0 x x	D25	C25	B25	A25	D10	C10	B10	A10
11	x x x x x 1 x x	D26	C26	B26	A26	D11	C11	B11	A11
12	x x x x x 1 x x	D27	C27	B27	A27	D12	C12	B12	A12
13	x x x x x 1 x x	D28	C28	B28	A28	D13	C13	B13	A13
14	x x x x x 0 x x	D29	C29	B29	A29	D14	C14	B14	A14
15	x x x x x 1 x x	D30	C30	B30	A30	D15	C15	B15	A15

* x = transparent to transmit formatter.
** A*i*—D*i* denote per-channel signaling bits, where *i* denotes channel number.

Table 8. Interdevice Formats for CEPT RSM Mode

Frame Number	Time-Slot-0 Bits* 8	7	6	5	4 3 2 1	Time-Slot-16 Bits** 8	7	6	5	4	3	2	1
0	x	x	x	x	x 1 x x	x	x	x	x	x	x	x	x
1	E17	E16	E1	E0	x 1 x x	D16	C16	B16	A16	D1	C1	B1	A1
2	x	x	x	x	x 1 x x	D17	C17	B17	A17	D2	C2	B2	A2
3	E19	E18	E3	E2	x 1 x x	D18	C18	B18	A18	D3	C3	B3	A3
4	x	x	x	x	x 1 x x	D19	C19	B19	A19	D4	C4	B4	A4
5	E21	E20	E5	E4	x 0 x x	D20	C20	B20	A20	D5	C5	B5	A5
6	x	x	x	x	x 0 x x	D21	C21	B21	A21	D6	C6	B6	A6
7	E23	E22	E7	E6	x 0 x x	D22	C22	B22	A22	D7	C7	B7	A7
8	x	x	x	x	x 1 x x	D23	C23	B23	A23	D8	C8	B8	A8
9	E25	E24	E9	E8	x 1 x x	D24	C24	B24	A24	D9	C9	B9	A9
10	x	x	x	x	x 0 x x	D25	C25	B25	A25	D10	C10	B10	A10
11	E27	E26	E11	E10	x 1 x x	D26	C26	B26	A26	D11	C11	B11	A11
12	x	x	x	x	x 1 x x	D27	C27	B27	A27	D12	C12	B12	A12
13	E29	E28	E13	E12	x 1 x x	D28	C28	B28	A28	D13	C13	B13	A13
14	x	x	x	x	x 0 x x	D29	C29	B29	A29	D14	C14	B14	A14
15	E31	E30	E15	E14	x 1 x x	D30	C30	B30	A30	D15	C15	B15	A15

* x = transparent to transmit formatter.
** A*i*—E*i* denote per-channel signaling bits, where *i* denotes channel number.

Serial Control Stream

The serial control stream (CTRLIN) input is shifted into the device at a 1.024-MHz rate while the control enable input (CTRLEN) is high (1), as illustrated in Figure 6. When CTRLEN goes low (0), the last eight bits of CTRLIN are latched in the device if the total the total number of 1s in the eight bits is odd. If the total number of 1s is even, bit 5 of the serial report stream (RPTOUT) alarm byte is set (1) and the data is not latched.

CTRLEN may occur at any time, independent of the system frame synchronization (SYSNC) pulse, as illustrated in Figures 7 and 8.

The latched control word is stored in one of two registers: if bit 6 is low, the word is internally stored in the mode register; if bit 6 is high, the word is internally stored in the exercise register. The contents of these registers determine the behavior of the device, as shown in Table 9.

Table 9. Valid Inputs for Mode and Exercise Registers

Bit	0	1	2	3	4	5	6	7
Mode	MD0	MD1	MD2	MD3	MD4	MD5	0	PY
Exercise	0	0	0	EX0	EX1	EX2	1	PY

Note: The PY bit is the last bit received.

Mode Register Decoding

The various operating modes of the 257AL Transmit Formatter are determined by the contents of the mode register, as shown in Tables 10 and 11. The MD4 determines whether the device is configured for DS1 or CEPT line formats.

In CEPT mode, which is selected when OPT4 is 1, bits MD0 and MD1 are not used, and bits MD2 and MD3 determine the specific submodes, as listed in Table 11.

In both DS1 and CEPT modes, bit MD5 controls the delay times for outputs FDEL and PDEL. A 28-time-slot delay is selected when MD5 is set, and a 23-time-slot delay is selected when MD5 is cleared.

Exercise Register Decoding

Exercise register bits EX0 and EX1 determine the interpretation of the device alarm register bits. In normal operation, all alarm bits, except DAO, are cleared; a high on the alarm or status bit represents an alarm condition. The effect of the exercise bits on each of the alarm and status bits is listed in Table 12. Device alarm bit DA0 is not affected by the exercises. Device alarm bit DA5 is exercised by sending an order with bad input parity. EX2 has no effect on the transmit formatter.

Table 10. DS1 Mode Option Bit Assignment (OPT4 = 0)

MD3	MD2	MD1	MD0	Mode	Stuff Pattern*	Allowable Signaling
0	0	0	0	Burst output	—	2-, 4-, 16-state, robbed digit
0	0	0	1	Burst stuffing	—	2-, 4-, 16-state, robbed digit
0	0	1	0	Unused	—	—
0	0	1	1	Burst stuffing	—	4-state *SLC* 96 Carrier System
0	1	0	0	Uniform stuffing	0	2-, 4-, 16-state, robbed digit
0	1	0	1	Uniform stuffing	1	2-, 4-, 16-state, robbed digit
0	1	1	0	Uniform stuffing	2	2-, 4-, 16-state, robbed digit
0	1	1	1	Uniform stuffing	3	2-, 4-, 16-state, robbed digit
1	0	0	0	Uniform stuffing	0	RSM
1	0	0	1	Uniform stuffing	1	RSM
1	0	1	0	Uniform stuffing	2	RSM
1	0	1	1	Uniform stuffing	3	RSM
1	1	0	0	Uniform stuffing	0	4-state *SLC* 96 Carrier System
1	1	0	1	Uniform stuffing	1	4-state *SLC* 96 Carrier System
1	1	1	0	Uniform stuffing	2	4-state *SLC* 96 Carrier System
1	1	1	1	Uniform stuffing	3	4-state *SLC* 96 Carrier System

* Stuff patterns are listed in Table 3.

Table 11. CEPT Mode Option Bit Assignments (OPT4 = 1)

MD3	MD2	Mode	Allowable Signaling
0	0	Unused	—
0	1	32 channel	16-state
1	0	32 channel	RSM
1	1	Unused	—

Table 12. Effect of Exercise Bits on Device Alarm Facility Status Bits

Exercise		Alarm*			
EX1	EX0	DA1	DA2	DA3	DA4
0	0	—	—	—	—
0	1	Inv	1	Inv	Inv
1	0	Inv	1	Inv	Inv
1	1	—	—	—	—

* "—" = exercise has no effect; Inv = exercise inverts the state of the bit.

Serial Report Stream

The serial report stream (RPTOUT) is a 1.024-MHz output used to report device alarm conditions and facility and device status information, as illustrated in Figure 11. The stream is divided into sixteen 8-bit bytes. The system frame synchronization (SYSNC) input identifies the boundary between bit 7 of byte 5 and bit 0 of byte 0, as illustrated in Figures 12 and 13. The data is updated once per frame and repeats four times per frame.

The device alarm bits, transmitted during bytes 0, 1, 4, 5, 8, 9, 12, and 13, are defined in Table 13. A high in any bit position except bit 0 or a low in bit 0 indicates an alarm condition. The contents of the exercise register are transmitted in bytes 2, 6, 10, and 14; the contents of the mode register are transmitted in bytes 3, 7, 11, and 15. The definitions of these bits are given in Table 14.

Table 13. Device Alarm — Bit Definitions (Bytes 0, 1, 4, 5, 8, 9, 12, 13)

Bit	Alarm
0	Logic one
1	Superframe synchronization error
2	Internal parity error
3	Input data parity error
4	Input idle code error
5	Control stream input parity error
6	Not used
7	Not used

Table 14. Exercise and Mode Bytes — Bit Definitions

Bit	Exercise Bytes (2, 6, 10, 14)	Mode Bytes (3, 7, 11, 15)
0	Logic 0	MD0
1	Logic 0	MD1
2	Logic 0	MD2
3	EX0	MD3
4	EX1	MD4
5	EX2	MD5
6	Logic 1	Logic 0
7	Parity	Parity

Characteristics

Clocks

Clock	Frequency	Period	Pulse Width	Duty Cycle	Mode
LCLK	1.544 MHz	648 ns	—	50% ± 5%	DS1
	2.048 MHz	488 ns	—	50% ± 5%	CEPT
SYCLK	4.096 MHz	244 ns	—	50% ± 5%	All
LSFSY	—	3 ms	648 ns	—	DS1
	—	2 ms	488 ns	—	CEPT
SYSNC	—	125 μs	244 ns	—	All

Electrical Characteristics

T_A = 0 to 85 °C, V_{DD} = 5 V ± .25 V, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit
Input voltages:				
high	V_{IH}	2.4	—	V
low	V_{IL}	—	0.8	V
Output voltages:				
high	V_{OH}	2.4	—	V
low	V_{OL}	—	0.4	V
Output current:				
high	I_{OH}	200	—	μA
low	I_{OL}	−2.0	—	mA
high-Z	I_{OZ}	—	40	μA

Maximum Ratings

Voltage on any pin with respect to ground ..... 6.0 V
Storage temperature (Tstg) range ..... −65 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Max	Unit	Mode	Figure
tLSHLCH	Line sync set-up time	80	—	ns	All	5
tLCHLSL	Line sync hold time	60	—	ns	All	5
tLCLLDV	Line data propagation delay	—	120	ns	All	5
tLCLLDX	Line data hold time	50	—	ns	All	5
tSNHSCH	System sync set-up time	60	—	ns	All	5
tSCHSNL	System sync hold time	60	—	ns	All	5
tSCHCIV	Serial control stream set-up time	0	400	ns	All	6
tSCHROV	Skew time SCLK to RPTOUT	0	244	ns	All	11
tSCHDSH	DGRSEL set-up time	—	200	ns	All	9
tSCHDSL	DGRSEL hold time	600	—	ns	All	9
tSCHDV	Data set-up time	—	400	ns	All	9
tDXSCH	Data hold time	100	—	ns	All	9, 10
tSNHDV	Data set-up time	—	3.3	μs	All	9, 10

Timing Diagrams

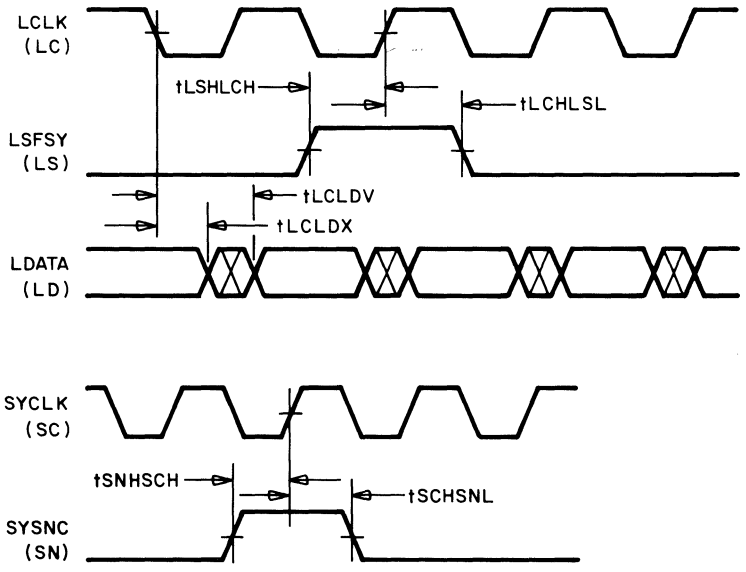


Figure 5. Clock and Data Timing

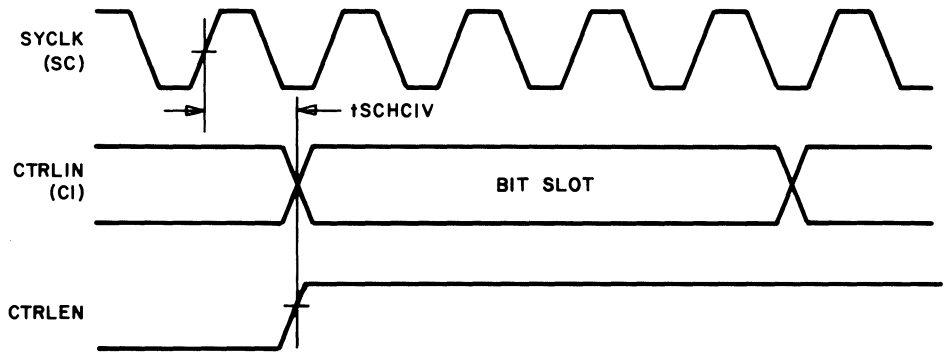


Figure 6. Serial Control Stream Input

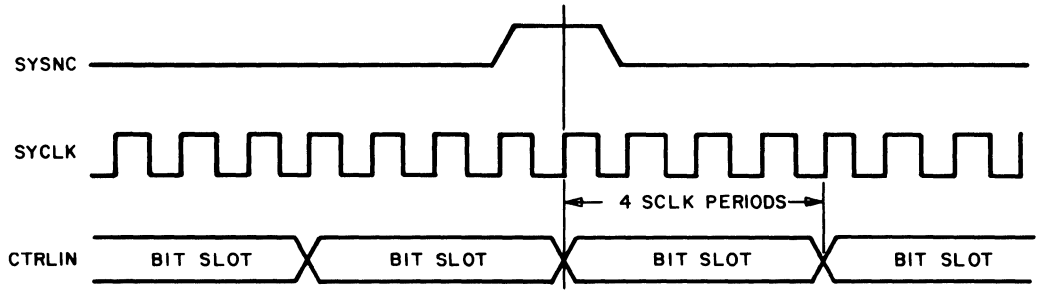


Figure 7. Serial Control Stream Bit Timing

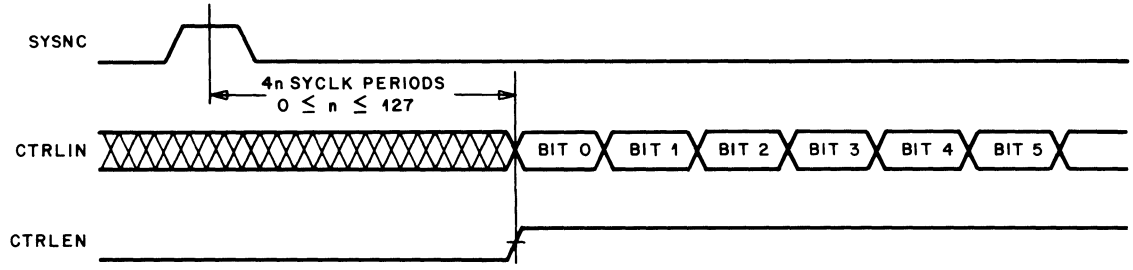


Figure 8. Serial Control Stream Byte Timing

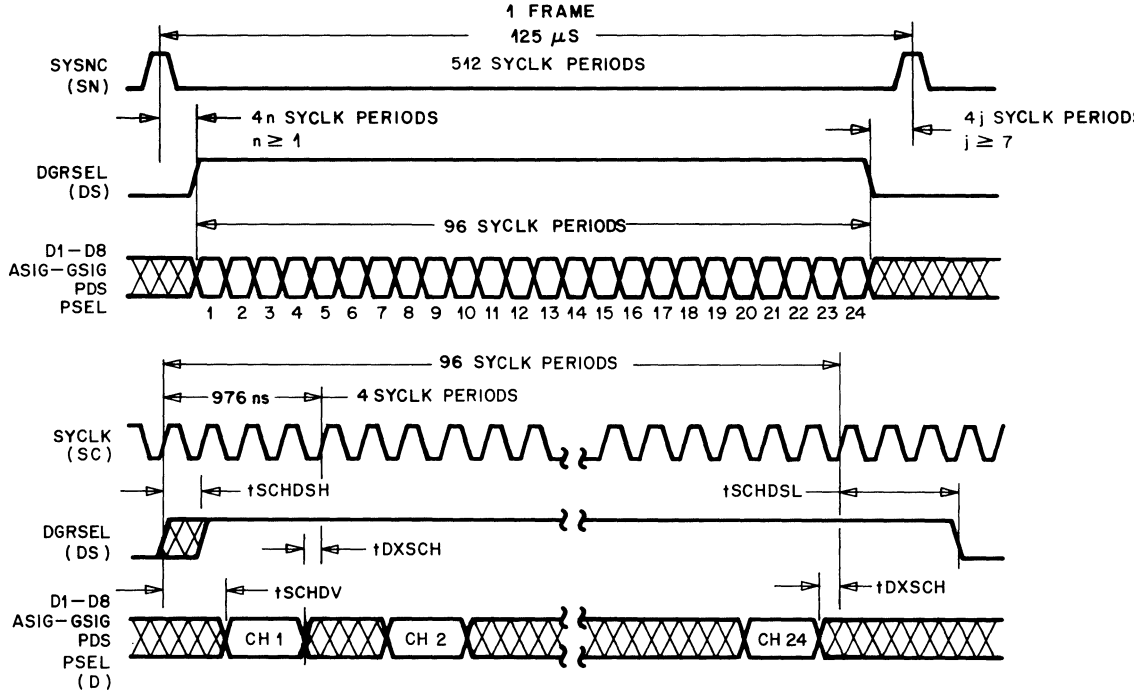


Figure 9. Input Timing for DS1 Burst Mode

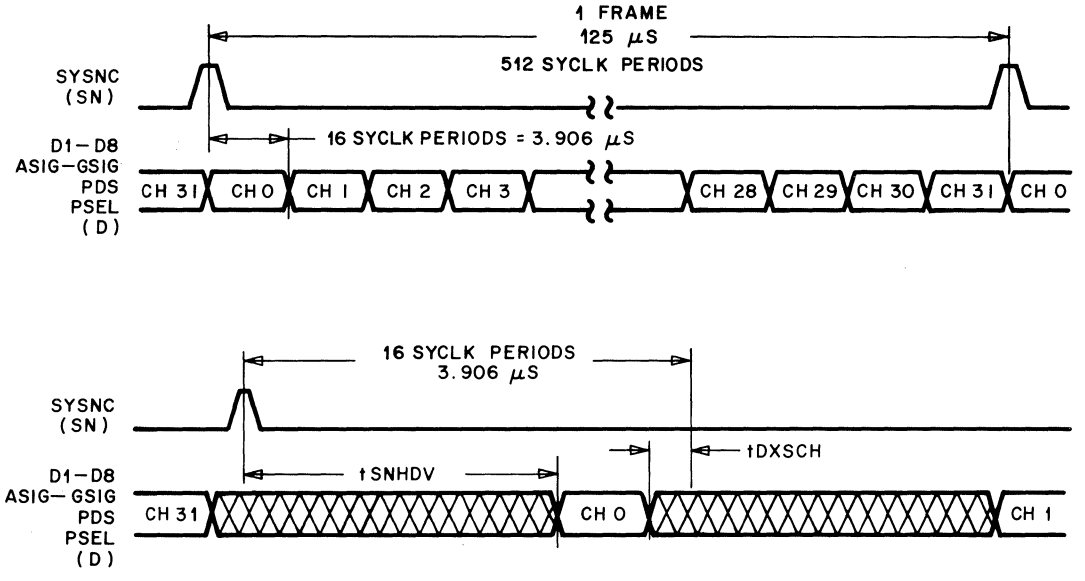


Figure 10. Input Timing for All Other Modes

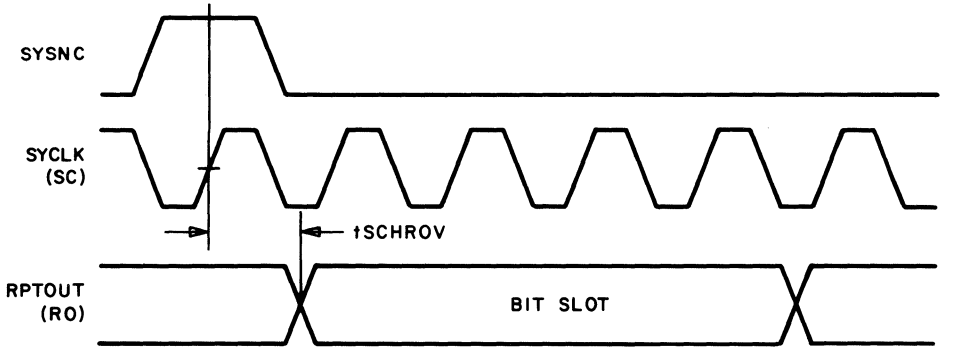


Figure 11. Serial Report Stream Output

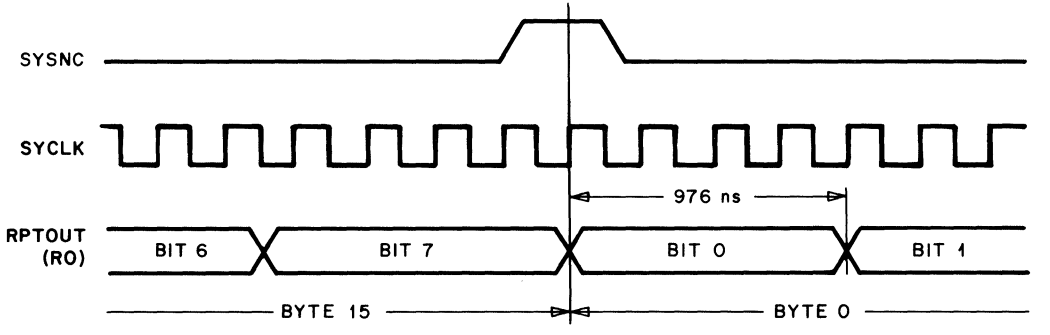


Figure 12. Serial Report Stream Bit Timing

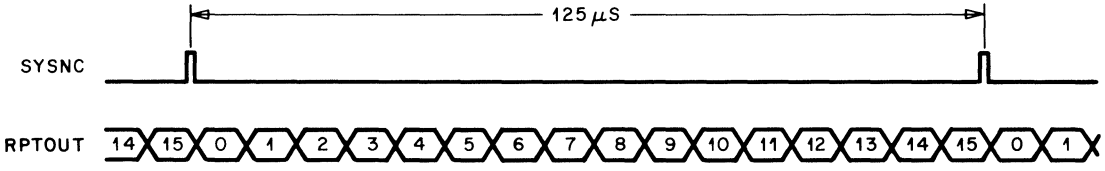


Figure 13. Serial Report Stream Byte Timing

257AU Receive Synchronizer

Features

- Selectable DS1 (1.544 Mb/s) or CEPT (2.048 Mb/s) formats
- 4- or 16-state RSM signal extraction
- Internal maintenance circuits
- Single 5 V supply
- TTL-compatible inputs and outputs

Description

The 257AU Receive Synchronizer (RS) is part of an LSI digital facility interface chip set that also includes the 257AL Transmitter Formatter and the T7229 (replaces the 229CG) or 229GB Primary Access Framer. The 257AU Receive Synchronizer performs serial-to-parallel conversion, slip compensation, and signaling extraction on the serial data received from the framer. The receive synchronizer is manufactured using NMOS technology and is available in a 32-pin plastic DIP.

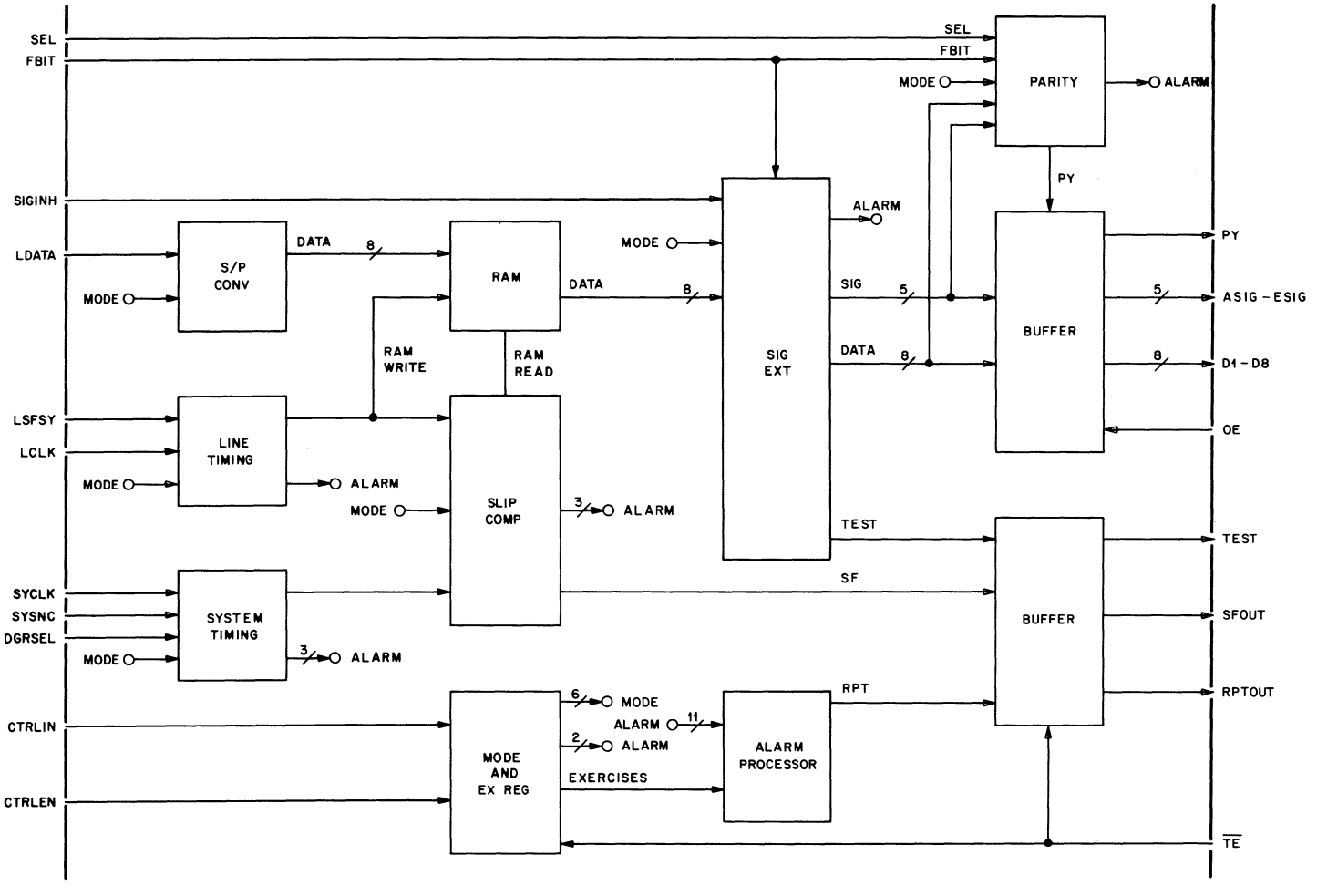


Figure 1. Block Diagram

User Information

Pin Descriptions

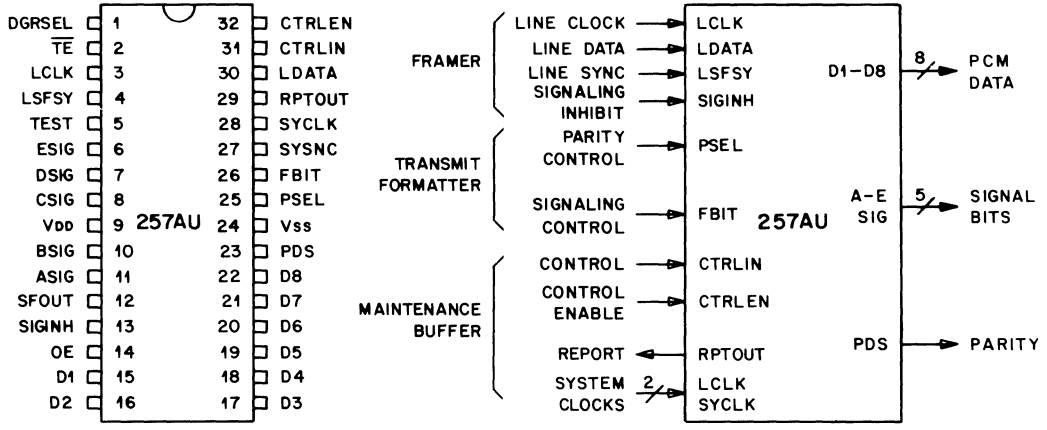


Figure 2. Pin Function and Functional Symbol Diagrams

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	DGRSEL	I	**Di-Group Select.** This pin is used only in DS1 1.024-MHz burst output mode to enable data output. It must be tied high or left disconnected for all other modes.
2	$\overline{TE}$	I	**Test Enable.** This pin is used only for device and circuit pack testing. When low, the device is in the test mode, which 3-states the SFOUT, TEST, and RPTOUT outputs. For normal operation, this pin must be tied high or left disconnected.
3	LCLK	I	**Line Clock.** Line clock from receive converter (1.544 MHz in DS1 mode and 2.048 MHz in CEPT mode). Clock is transmitted by the framer.
4	LSFSY	I	**Line Superframe Sync.** A high pulse on this pin identifies the first frame of a superframe in DS1 mode and a multiframe in CEPT mode. The pulse is transmitted by the framer.
5	TEST	O	**Test Output.** For manufacturing purposes only. Not used for normal operation.
6 7 8	ESIG DSIG CSIG	O	**E Signaling Bit.** **D Signaling Bit.** Outputs (system timing). **C Signaling Bit.**
9	VDD	—	**5 V Supply.**

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
10	BSIG	O	**B Signaling Bit.** Outputs (system timing).
11	ASIG		**A Signaling Bit.**
12	SFOUT	O	**Superframe Output.** Slip-compensated pulse that identifies output frame 1.
13	SIGINH	I	**Signaling Inhibit.** When high, signaling extraction is inhibited until 32 frames after SIGINH (pin 13) returns low. The last extracted signaling value is output while signaling extraction is inhibited. This input is supplied by the framer.
14	OE	I	**Output Enable.** A high or no connection enables the D1—D8 (pins 15—22), ASIG—ESIG (pins 6—8, 10, and 11), and PDS (pin 23) outputs. A low 3-states these outputs.
15 16 17 18 19 20 21 22	D1 D2 D3 D4 D5 D6 D7 D8	O	**Data Bit 1.** **Data Bit 2.** **Data Bit 3.** **Data Bit 4.** Parallel data is output to the system **Data Bit 5.** from these pins (system timing). **Data Bit 6.** **Data Bit 7.** **Data Bit 8.**
23	PDS	O	**Parity.** Parity output over D1—D8, ASIG—ESIG, and FBIT.
24	V_{SS}	—	**Ground.**
25	PSEL	I	**Parity Selection.** A high on this pin sets PDS for even parity and a low sets PDS for odd parity. This signal is supplied on system timing on a per-channel basis.
26	FBIT	I	**Frame Signaling Bit.** DS1 mode signaling extraction control bit on system timing on a per-channel basis. Not used in CEPT mode.
27	SYSNC	I	**System Frame Sync.** An 8-kHz pulse stream. A high pulse on this pin marks the first traffic channel in each frame.
28	SYCLK	I	**System Clock.** This 4.096-MHz clock provides device timing.
29	RPTOUT	O	**Serial Report Output.** Serial output of internal status at a 1.024-MHz rate.
30	LDATA	I	**Line Data.** Serial input data stream from the framer (line timing).
31	CTRLIN	I	**Serial Control Input.** Control information is input on this pin at a 1.024-MHz rate. This information determines the input and output formats.
32	CTRLEN	I	**Control Enable.** The serial control stream is shifted into the receive synchronizer while this input is high.

Operation

The 257AU Receive Synchronizer performs serial-to-parallel conversion, slip compensation, and signaling extraction on the serial data from the T7229 or 229GB Framers. The device monitors the integrity of the data from the framer by checking for the presence of a unique signal embedded in the serial input data. The data output from the receive synchronizer is formatted as a 14-bit parallel word for each channel. A word consists of 8 data, 5 signaling, and 1 parity bits. The receive synchronizer has internal maintenance circuits that continuously monitor the operation of all its circuits.

The receive synchronizer operates in either the 1.544-MHz DS1 mode or the 2.048-MHz CEPT mode. In the DS1 mode, the device recognizes 4-/16-state robbed digit-8 or RSM/DMI word-24 signaling. In CEPT mode, it recognizes word-16 or RSM (words 0, 16) signaling.

The major functional blocks of the 257AU device are shown in Figure 1.

Timing

The system clock (SYCLK) frequency is 4.096 MHz, the 512th harmonic of the sampling frequency. The system frame sync pulse (SYSN) is one clock period wide, with the rising edge of the clock occurring at the center of the sync pulse. The frame sync period is 125 μs, which corresponds to the 8-kHz sampling frequency, as illustrated in Figure 16.

The system timing circuit generates two internal 1.024-MHz signals, GBC21 and GBC31, which define 128 system time slots per frame. The four edges produced by these signals divide each time slot into 244-ns-wide phases, labeled 0, 4, 8, and 12, respectively. All signal transitions, except those controlled by line timing, occur at one of these phases. All output timing specifications are referenced to the rising edge of the 4.096-MHz clock frequency.

The line clock (LCLK) frequency is 1.544 MHz (193rd harmonic of the sampling frequency) for DS1 applications and 2.048 MHz (256th harmonic of the sampling frequency) for CEPT applications. The rising edge of the line clock occurs at the center of the line superframe sync pulse (LSFSY), which is one clock period wide. The superframe sync pulse is 24 frames (3 ms) for DS1 applications and 16 frames (2 ms) for CEPT applications, as illustrated in Figures 8 and 4.

Although the system clock and line clock frequencies are synchronous (both are harmonics of the sampling frequency), the phase relationship between them is arbitrary. Timing signals from each timing circuit are sent to the slip circuit, which maintains the difference between the clocks within prescribed limits.

The line timing circuit uses both the LCLK and LSFSY inputs to generate the line timing signals. They are used for shifting data through the serial-to-parallel converter and for writing data into RAM.

The system timing circuit generates the timing signals used throughout the rest of the device. These signals are derived from both the SYCLK and SYSYN inputs.

Data Path

The serial input data on the LDATA input is converted into 8-bit parallel data and written into RAM under control of both the line clock and slip-compensation circuit. The RAM, in conjunction with its write and read control circuits and the slip circuit, provides a maximum two-frame delay to the traffic signals passing through the device.

The slip circuit maintains the delay through the RAM in the range of 0 through 2 frames. This is accomplished by deleting an entire frame of data whenever the delay approaches two frames and by repeating an entire frame of data whenever the delay approaches 0. The limits on the closeness of the delay to 0 or 2 frames are mode-dependent. Slip-compensated superframe sync is output on SFOUT, as illustrated in Figure 3.

The signaling extraction circuit samples the data at the RAM output and stores the signaling bits for each channel in five primary storage registers. While the primary registers are being updated, previously stored signaling data is transferred to five secondary registers. The RAM output data values are not changed.

In the DS1 mode 4-state robbed-digit signaling format, the receive synchronizer extracts the signaling bits from the RAM output, stores their values in the primary registers, updates the secondary registers, and replaces the extracted signaling bits at the RAM output with 1s.

Under normal conditions, primary register signaling data for each channel and the corresponding channel data from the RAM output are written to the output data bus. The write operation is controlled by both the system clock and the state of the DGRSEL input. The signaling extraction process halts if the SIGINH input becomes active; it remains in a halt condition until 32 frames after the SIGINH input goes inactive. While in the halt state, the signaling data written to the output data bus is taken from the secondary registers. In this state, the primary registers are updated from the secondary registers. This ensures that the signaling data output to the output data bus does not change when the signaling extraction process is resumed.

The receive synchronizer computes odd parity over the eight data (D1—D8) and five signaling (ASIG—ESIG) output bits on the output data bus. Parity is output on the PDS and is modified on a per-channel basis by the data on the PSEL and FBIT inputs. If either the PSEL or the FBIT inputs separately go high (1), the output parity is changed to even. The 257AU device has the option of excluding the ESIG bit from the parity computation; the 257AS device did not have this option.

The 14-bit (D1—D8, ASIG—ESIG, and PDS) parallel output bus is enabled by a logic high on the OE input. A logic low (0) on the OE input 3-states the bus.

Maintenance Features and Mode Selection

The 257AU Receive Synchronizer uses internal parity and other comparison circuits to monitor the operation of the device. Since the normal state of these circuits is "no alarm," external exercises are required to force an alarm condition to verify the alarm's operation. Alarms are reported on the serial output report stream (RPTOUT).

Figure 3. SFOUT Timing

Exercise and mode selection orders are routed to the respective exercise or mode registers when the $\overline{TE}$ and CTRLEN inputs are high (1). The $\overline{TE}$ input has an internal pull-up resistor, so it may be left unconnected.

When the $\overline{TE}$ input is low and CTRLEN input is high, serial data on the CTRLIN input is routed to an internal test register. This feature is provided to facilitate chip and circuit pack testing. A low on $\overline{TE}$ also 3-states the RPTOUT, SFOUT, and TEST outputs.

Operating Modes

The 257AU Receive Synchronizer operates in several modes, which are defined by the framing and signaling formats of the line input signals (LDATA, LSFSY, and LCLK) and the format of the output data bus (D1—D8, ASIG—ESIG, and PDS). Available data output and signaling formats are listed in Table 2 for both DS1 and CEPT line formats.

Table 2. Available Output Formats

Line Formats	Signaling Formats	Output Formats
CEPT	Word-16 RSM (word 0, 16)	256-kHz uniform
DS1	Robbed digit-8 RSM/DMI (word-24)	Uniform stuffing Burst stuffing 1.024-MHz burst

CEPT Mode

Line Format for CEPT Mode. The CEPT line format for the serial data input on LDATA consists of a 16-frame (0—15) superframe in which each frame comprises 256 time slots (0—255). The 256 time slots are formatted as 32 words of 8 bits each (digits 1—8).

A pulse on the line superframe sync input (LSFSY) locates digit 1 of word 0 in frame 0 of the serial data input (LDATA). The nominal sync pulse width is one clock period. The rising edge of the clock (LCLK) occurs at the center of the sync pulse. The superframe period is 2 μs. The frame period is 125 μs, which corresponds to the 8-kHz channel sampling rate. The line clock frequency, 2.048 MHz, is the 256th harmonic of the 8-kHz sampling frequency.

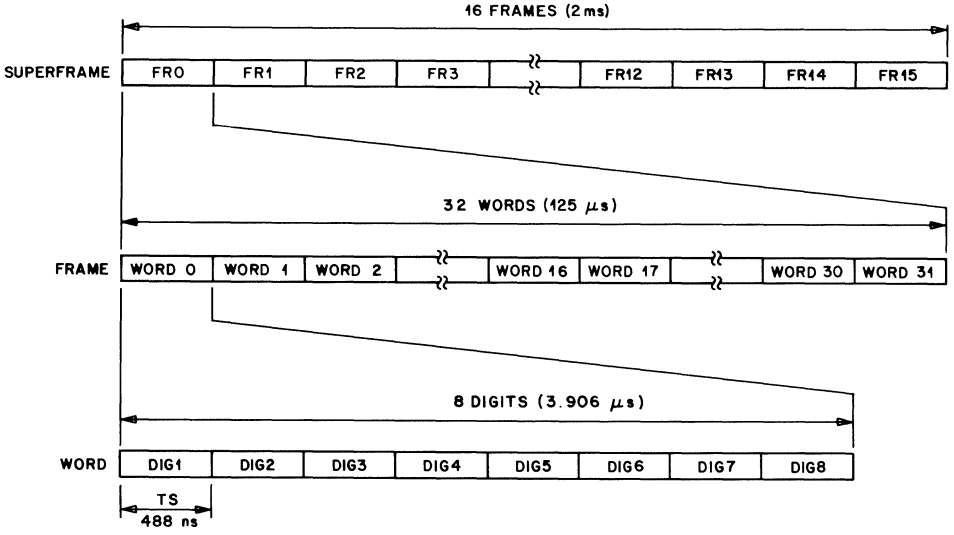


Figure 4. CEPT Line Format

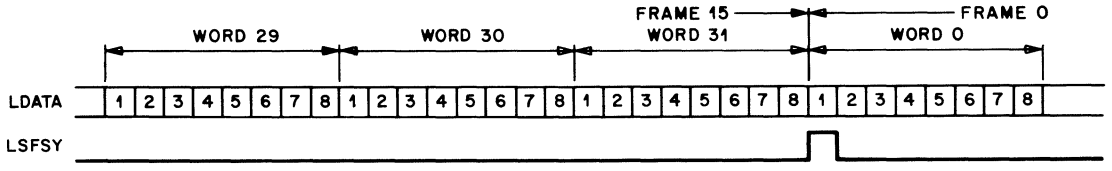


Figure 5. CEPT Clock and Data Relationships

The first word in each frame (word 0) carries framing and control information and a unique bit pattern used for maintenance of the transmission path between the framer and the receive synchronizer. Word 0 also carries the E signaling bits in the RSM formats for all channels. The remaining 31 words carry traffic or signaling data.

The maintenance pattern, which is carried in digit 3 of word 0, repeats every 16 frames, as shown in Table 3.

Table 3. Maintenance Pattern — Bit 3 of Word 0

Frame Number	0	1	2	3	4	5	6	7
Bit Pattern	1	1	1	1	1	0	0	0
Frame Number	8	9	10	11	12	13	14	15
Bit Pattern	1	1	0	1	1	1	0	1

Signaling Formats for CEPT Mode. The CEPT mode supports two signaling formats: word-16 and RSM (words 0, 16). In both formats, all bits for channels 1—15 and 17—31 in every frame are allocated to traffic; bits for channel 16 in every frame are allocated to signaling data.

Table 4. CEPT Word-16 Signaling Format

Frame Number	Bit Use in Channel 16*							
	1	2	3	4	5	6	7	8
0	x	x	x	x	x	x	x	x
1	A1	B1	C1	D1	A17	B17	C17	D17
2	A2	B2	C2	D2	A18	B18	C18	D18
3	A3	B3	C3	D3	A19	B19	C19	D19
4	A4	B4	C4	D4	A20	B20	C20	D20
5	A5	B5	C5	D5	A21	B21	C21	D21
6	A6	B6	C6	D6	A22	B22	C22	D22
7	A7	B7	C7	D7	A23	B23	C23	D23
8	A8	B8	C8	D8	A24	B24	C24	D24
9	A9	B9	C9	D9	A25	B25	C25	D25
10	A10	B10	C10	D10	A26	B26	C26	D26
11	A11	B11	C11	D11	A27	B27	C27	D27
12	A12	B12	C12	D12	A28	B28	C28	D28
13	A13	B13	C13	D13	A29	B29	C29	D29
14	A14	B14	C14	D14	A30	B30	C30	D30
15	A15	B15	C15	D15	A31	B31	C31	D31

* A, B, C, and D = signaling bits for channels 1—15, 17—31; x = don't care.

For word-16 format, the A, B, C, and D signaling bits for each channel are extracted from the data in channel 16. The signaling for two channels is extracted every frame and the ESIG bit is cleared for all channels in this format. The word-16 format is illustrated in Table 4.

The RSM format supports the E signaling bits in addition to supporting A, B, C, and D. The E signaling bits for four channels are extracted from digits 5—8 of channel 0 every odd-numbered frame, as is illustrated in Table 5. The RSM word-16 format is the same as the non-RSM word-16 format.

Output Format in CEPT Mode. In the CEPT mode, 32 parallel 8-bit words are sequentially read from the RAM for each frame. These bits are combined with the five signaling bits and the parity bit to form the 14-bit parallel output. Each channel occupies four system time slots and the system sync pulse defines the location of channel 0. Since 32 words from the serial-to-parallel converter are written into the RAM every frame, there is a one-to-one correspondence between input word numbers and output channel numbers.

Table 5. CEPT Word-0 (RSM) Signaling Format

Frame Number	Bit Use in Channel 0*			
	5	6	7	8
0	x	x	x	x
1	x	E1	x	E17
2	x	x	x	x
3	E2	E3	E18	E19
4	x	x	x	x
5	E4	E5	E20	E21
6	x	x	x	x
7	E6	E7	E22	E23
8	x	x	x	x
9	E8	E9	E24	E25
10	x	x	x	x
11	E10	E11	E26	E27
12	x	x	x	x
13	E12	E13	E28	E29
14	x	x	x	x
15	E14	E15	E30	E31

* E the RSM E = signaling bits for channels 1—15, 17—31; x = don't care.

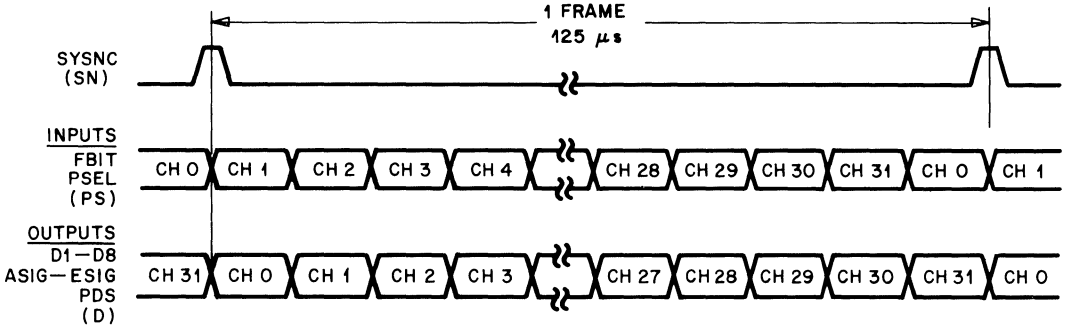


Figure 6. Input/Output Timing (All Modes Except DS1 Burst Output Mode) for an Entire Frame

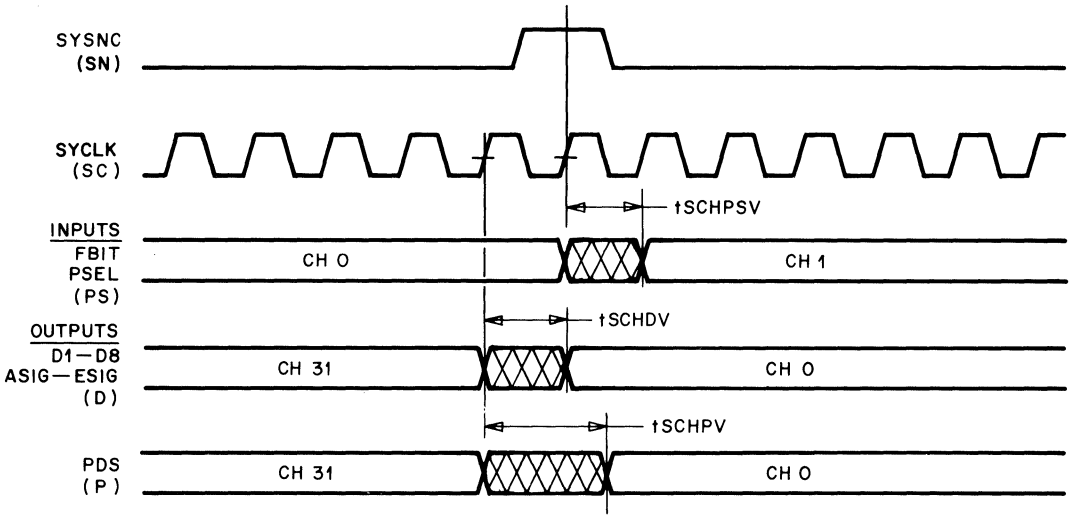


Figure 7. Detailed Input/Output Timing (All Modes Except DS1 Burst Output Mode) for a System Frame Sync Pulse

DS1 Mode

Line Format for DS1 Mode. The DS1 line format for the serial data (LDATA) consists of a 24-frame superframe in which each frame consists of 193 time slots. The first time slot in a frame contains a framing bit, which is used for aligning the transmitted data between the framer and the receive synchronizer. The remaining 192 time slots, formatted as 24 words of 8 bits, carry traffic and signaling data.

The line superframe sync pulse (LSFSY) identifies the position of the framing bit in frame 24 of LDATA, as shown in Figure 9. The nominal sync pulse width is one clock period. The rising edge of the clock, LCLK, occurs at the center of the sync pulse. The superframe period is 3 ms. The frame period is 125 μs, which corresponds to the 8-kHz channel sampling rate. The line frequency, 1.544 MHz, is the 193rd harmonic of the 8-kHz sampling frequency.

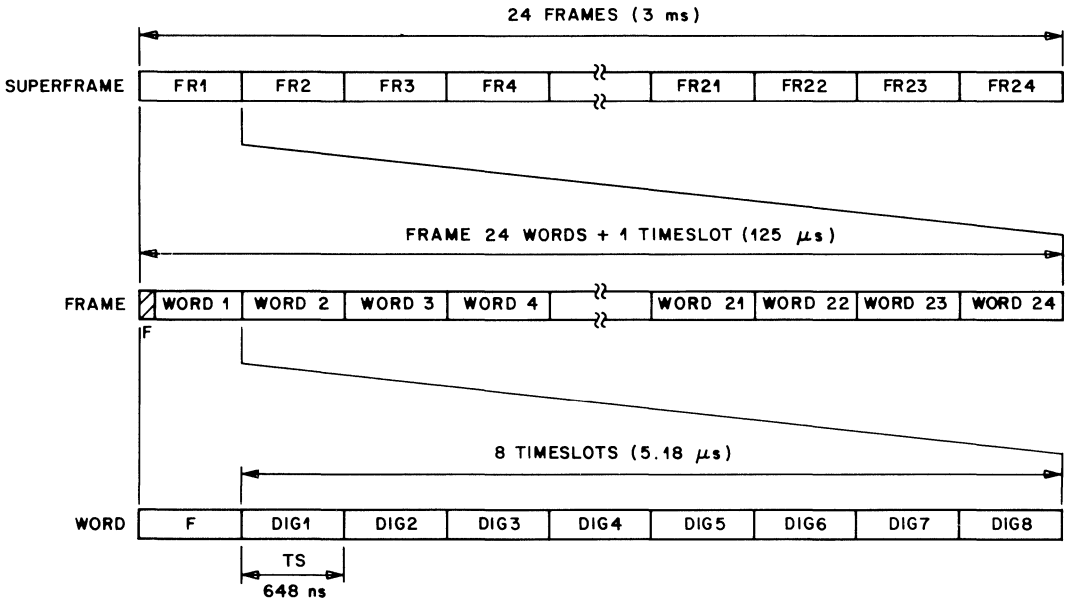


Figure 8. DS1 Line Format

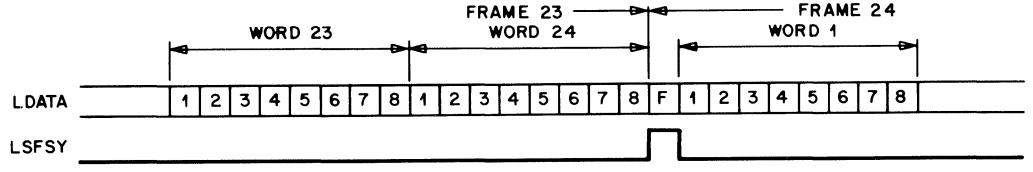


Figure 9. DS1 Clock and Data Relationship

The framing bit pattern for the DS1 mode is shown in Table 6.

Table 6. DS1 Mode F-bit Pattern

Frame	1	2	3	4	5	6	7	8	9	10	11	12
F-bit	1	1	1	1	1	0	0	0	1	1	0	1
Frame	13	14	15	16	17	18	19	20	21	22	23	24
F-bit	1	1	0	1	0	1	0	1	1	0	1	0

Signaling Formats for DS1 Mode. The DS1 mode supports two signaling formats: robbed digit-8 and RSM/DMI word-24.

In the robbed digit-8 signaling format, all bits in every frame, except frames 6, 12, 18, and 24, are dedicated to traffic data. For these frames, digits 1—7 carry traffic data, while digit 8 is "robbed" to carry the signaling data. For the channels that have the FBIT input low (0), the A, B, C, and D signaling bits are extracted from digit 8 during frames 6, 12, 18, and 24, respectively. For the channels that have the FBIT input high, the C and D signaling bits are in a 0 state, the A signaling bit is extracted from digit 8 during frames 6 and 18, and the B signaling bit is extracted during frames 12 and 24. The E signaling bit is cleared for all channels in this mode. This format is shown in Table 7. In those frames in which signaling is extracted, digit 8 is set.

In the DS1 mode word-24 RSM/DMI signaling format, channels 1—23 in each frame contain traffic data. The signaling information is carried in channel 24, as listed in Table 8. In this mode, the A signaling bit is updated every 12 frames and the other 4 signaling bits are updated every 24 frames.

Table 7. DS1 Robbed Digit-8 Signaling Format

Frame Number	Bit Use in Each Word		
	Traffic Digits	Signaling*	
		FBIT = 1	FBIT = 0
1	1—8		
2	1—8		
3	1—8		
4	1—8		
5	1—8		
6	1—7	Digit 8 = A	Digit 8 = A
7	1—8		
8	1—8		
9	1—8		
10	1—8		
11	1—8		
12	1—7	Digit 8 = B	Digit 8 = B
13	1—8		
14	1—8		
15	1—8		
16	1—8		
17	1—8		
18	1—7	Digit 8 = A	Digit 8 = C
19	1—8		
20	1—8		
21	1—8		
22	1—8		
23	1—8		
24	1—7	Digit 8 = B	Digit 8 = D

* If FBIT = 1, then 4-state signaling (A, B); if FBIT = 0, then 18-state signaling (A, B, C, D).

Output Formats in DS1 Modes. The DS1 mode supports three output formats: uniform stuffing, burst stuffing, and 1.024-MHz burst output. In all DS1 modes, 24 words per frame are written into the RAM.

In the two stuffing formats, 32 words are read from the RAM and signaling registers every frame at a rate of 256 kHz. The eight extra words, called "stuffed words," have a fixed data pattern, 01111111, and signaling pattern, 00001. Since there are eight more output words than there are channels, a one-to-one correspondence between output words and output channels does not exist.

Table 8. DS1 Word-24 RMS/DMI Signaling Format

Frame Number	Bit Use in Word-24*							
	1	2	3	4	5	6	7	8
1	A13	A1	B1	C1	D1	x	1	E1
2	A14	A2	B2	C2	D2	x	1	E2
3	A15	A3	B3	C3	D3	x	1	E3
4	A16	A4	B4	C4	D4	x	1	E4
5	A17	A5	B5	C5	D5	x	1	E5
6	A18	A6	B6	C6	D6	x	1	E6
7	A19	A7	B7	C7	D7	x	1	E7
8	A20	A8	B8	C8	D8	x	1	E8
9	A21	A9	B9	C9	D9	x	1	E9
10	A22	A10	B10	C10	D10	x	1	E10
11	A23	A11	B11	C11	D11	x	1	E11
12	x	A12	B12	C12	D12	x	1	E12
13	A1	A13	B13	C13	D13	x	1	E13
14	A2	A14	B14	C14	D14	x	1	E14
15	A3	A15	B15	C15	D15	x	1	E15
16	A4	A16	B16	C16	D16	x	1	E16
17	A5	A17	B17	C17	D17	x	1	E17
18	A6	A18	B18	C18	D18	x	1	E18
19	A7	A19	B19	C19	D19	x	1	E19
20	A8	A20	B20	C20	D20	x	1	E20
21	A9	A21	B21	C21	D21	x	1	E21
22	A10	A22	B22	C22	D22	x	1	E22
23	A11	A23	B23	C23	D23	x	1	E23
24	A12	1	1	1	0	RMA	0	x

* A, B, C, and D = signaling bits for channels 1—23; x = don't care.

DS1 Burst Stuffing Output Format. In the burst stuffing format, there is a one-to-one correspondence between the first 24 output channel numbers and the 24 output words. The eight stuffed words are output in a burst at the end of every frame. The word-to-channel correspondence is shown in Table 9.

DS1 Uniform Stuffing Output Formats. In the uniform stuffing format, the eight stuffed words are uniformly distributed throughout the frame. In this format, four distributions are possible and all four are implemented. The word-to-channel correspondence is shown in Table 9.

Table 9. DS1 Output Formats — Channel Mappings

Format	Output Word Number*															
Channel number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Burst stuff	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Uniform stuff 0	s	1	2	3	s	4	5	6	s	7	8	9	s	10	11	12
Uniform stuff 1	1	s	2	3	4	s	5	6	7	s	8	9	10	s	11	12
Uniform stuff 2	1	2	s	3	4	5	s	6	7	8	s	9	10	11	s	12
Uniform stuff 3	1	2	3	s	4	5	6	s	7	8	9	s	10	11	12	s
Channel number	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Burst stuff	17	18	19	20	21	22	23	24	s	s	s	s	s	s	s	s
Uniform stuff 0	s	13	14	15	s	16	17	18	s	19	20	21	s	22	23	24
Uniform stuff 1	13	s	14	15	16	s	17	18	19	s	20	21	22	s	23	24
Uniform stuff 2	13	14	s	15	16	17	s	18	19	20	s	21	22	23	s	24
Uniform stuff 3	13	14	15	s	16	17	18	s	19	20	21	s	22	23	24	s

* s = a stuffed word.

DS1 1.024-MHz Burst Output. In the burst output format, 24 words are read from the RAM and signaling registers every frame in a 1.024-MHz burst. The burst is controlled by system timing and the signal on the DGRSEL input. In this format, the RAM and signaling registers are read sequentially at a 1.024-MHz rate while the DGRSEL input is in the high state. This input should remain high for 23.324 μs (24 x 0.976 μs) to allow all the words to be read. The DGRSEL input must be low when SYSYN is high, as indicated in Figure 10. Stuffed words are not used by this output format.

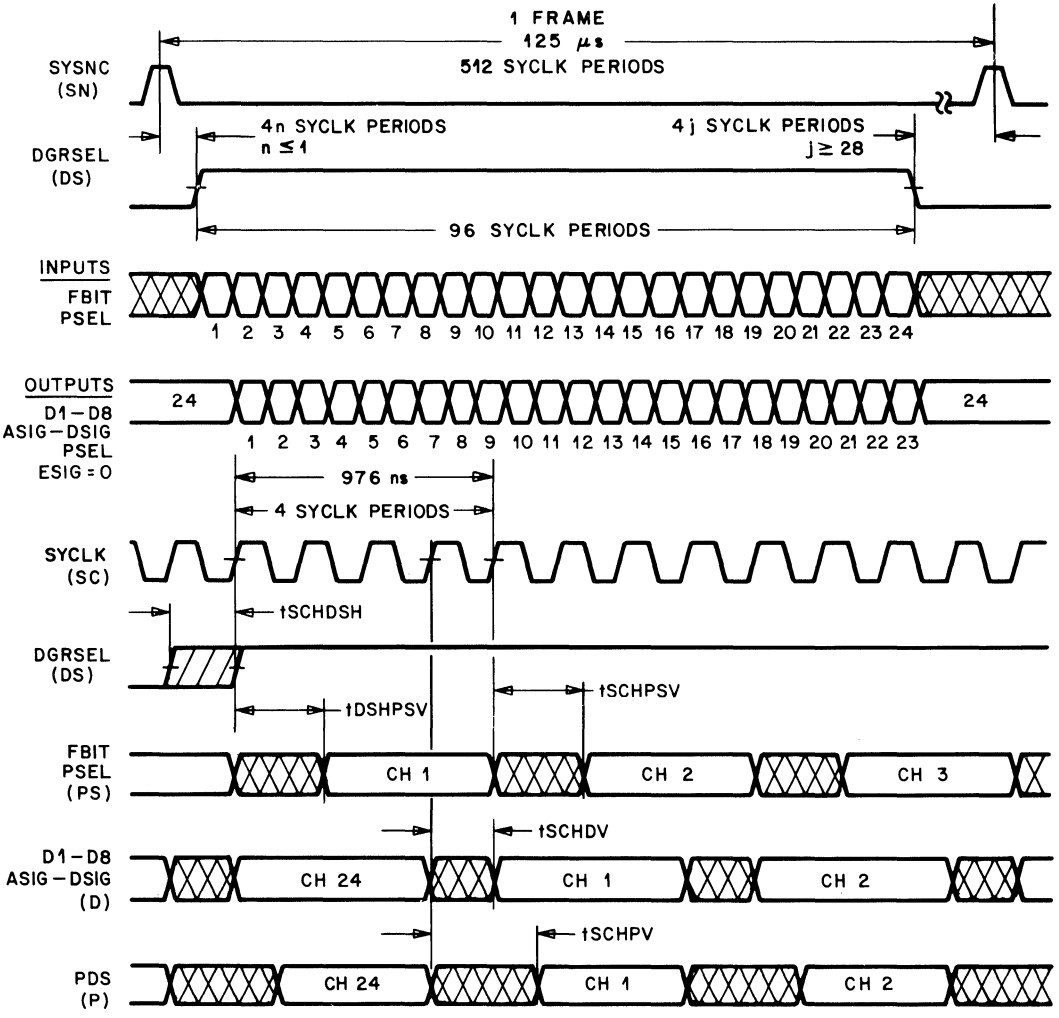


Figure 10. Input/Output Timing for DS1 Burst Output Mode

Serial Report Stream

The serial report stream, RPTOUT, is a 1.024-MHz output used to report device alarm conditions and facility and device status information, as illustrated in Figure 11. The stream is divided into sixteen 8-bit bytes. The frame sync input, SYSYN, identifies the boundary between bit 7 of byte 16 and bit 0 of byte 0, as illustrated in Figures 12 and 13. The data is updated once per frame and repeats 4 times per frame.

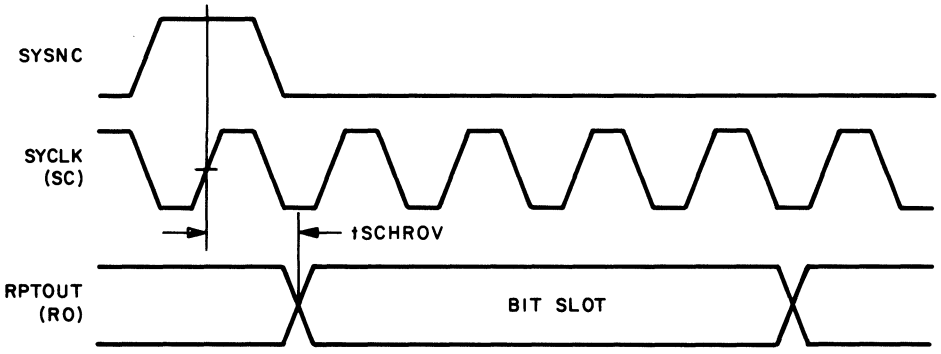


Figure 11. Serial Report Stream Output

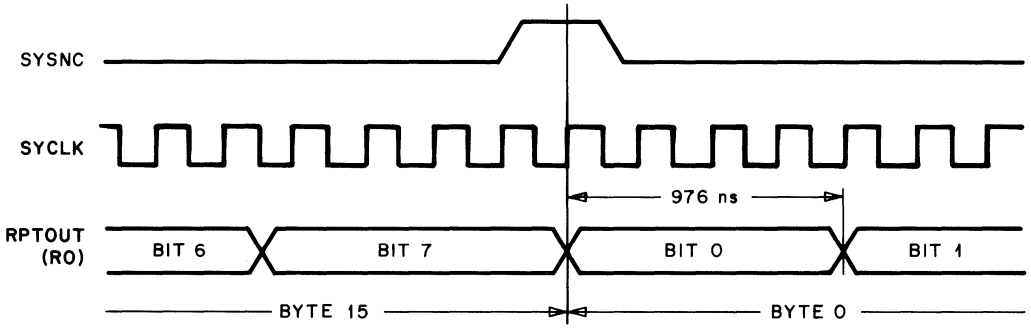


Figure 12. Serial Report Stream Bit Timing

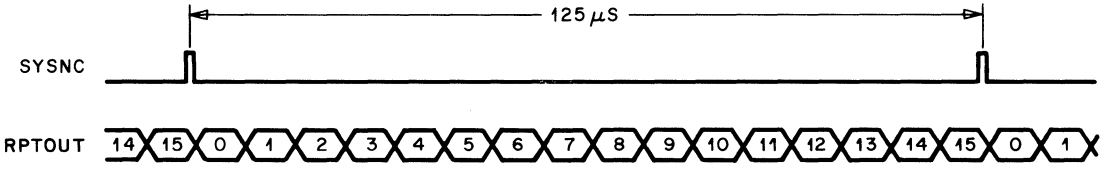


Figure 13. Serial Report Stream Byte Timing

The device alarm bits, transmitted during bytes 0, 4, 8, and 12 are defined in Table 10. A high in any bit position except bit 0 or a low in bit 0 indicates an alarm condition. Device alarm bits DA2, DA3, DA5, DA7 do not respond to alarm conditions if the device is in the signaling inhibit state (facility status bit FS1 = high). The facility status bits, transmitted during bytes 1, 5, 9, and 13, are defined in Table 11. The FS2 and FS3 do not respond to alarm conditions if the device is in the signaling inhibit state. The contents of the exercise register are transmitted in bytes 2, 6, 10, and 14. The contents of the mode register are transmitted in bytes 3, 7, 11, and 15. The definitions of these bits are given in Table 12.

Table 10. Device Alarm — Bit Definitions (Bytes 0, 4, 8, 12)

Bit	Definition
DA0	Always set
DA1	Signaling parity error
DA2	Pseudorandom maintenance pattern error
DA3	RAM parity error
DA4	Channel counter error
DA5	Stuff circuit error (DS1 mode only)
DA6	Control stream input parity error
DA7	Frame counter error

Table 11. Facility Status Bytes — Bit Definitions (Bytes 1, 5, 9, 13)

Bit	Definition
FS0	Always cleared
FS1	Signaling extraction inhibited
FS2	Negative slip occurred
FS3	Positive slip occurred
FS4—FS7	Always cleared

Table 12. Exercise and Mode Bytes — Bit Definitions

Bit	Exercise Bytes (2, 6, 10, 14)	Mode Bytes (3, 7, 11, 15)
0	Logic 0	MD0
1	Logic 0	MD1
2	Logic 0	MD2
3	EX0	MD3
4	EX1	MD4
5	EX2	MD5
6	Logic 1	Logic 0
7	Parity	Parity

Serial Control Stream

The serial control input stream, CTRLIN, is shifted into the device at a 1.024-MHz rate while the control enable input (CTRLEN) is high, as illustrated in Figure 14. When CTRLEN goes low, the last eight bits of CTRLIN are latched in the device if the total number of 1s in the eight bits is odd. If the total number of 1s is even, bit 6 of the serial report stream (RPOUT) alarm byte is set and the data is not latched.

CTRLEN may be occur at any time, independent of SYSYN, as illustrated in Figures 15 and 16.

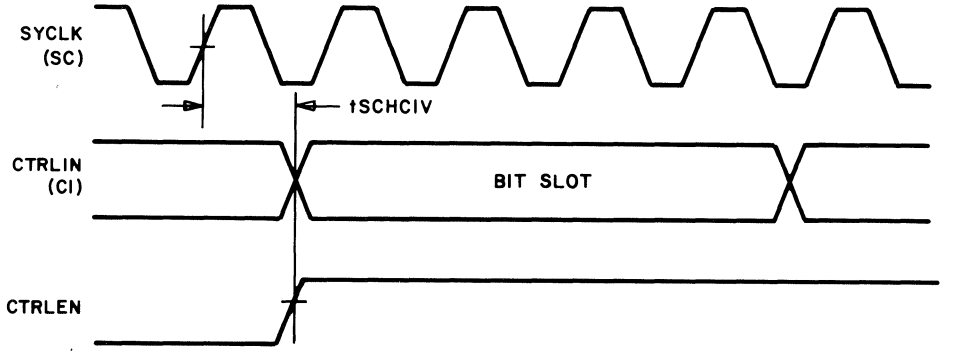


Figure 14. Serial Control Stream Input

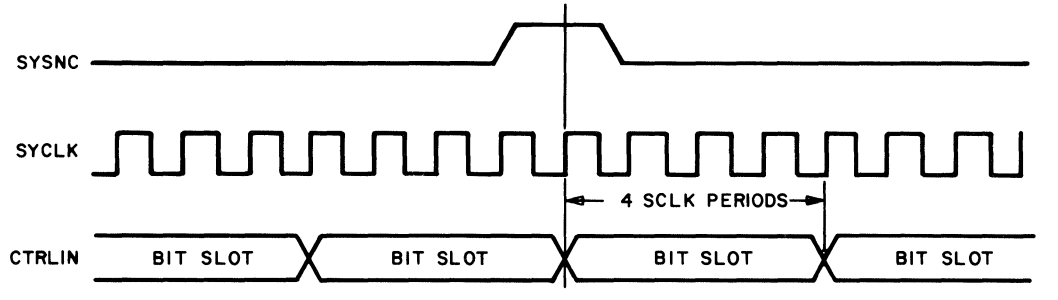


Figure 15. Serial Control Stream Bit Timing

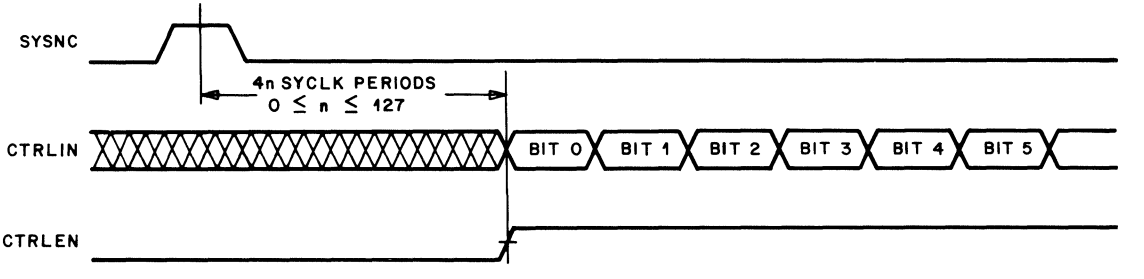


Figure 16. Serial Control Stream Byte Timing

The latched control word is stored in either of two registers: if bit 6 is a low, the word is internally stored in the mode register; if bit 6 is a high, the word is internally stored in the exercise register. The contents of these registers determine the behavior of the device, as shown in Table 13.

Table 13. Valid Inputs for Mode and Exercise Registers

Bit	0	1	2	3	4	5	6	7
Mode	MD0	MD1	MD2	MD3	MD4	MD5	0	PY
Exercise	0	0	0	EX0	EX1	EX2	1	PY

Note: The PY bit is the last bit received.

Mode Register Decoding

The various operating modes of the receive synchronizer are determined by the contents of the mode register, as shown in Table 14. The MD4 determines whether the device is configured for DS1 or CEPT line formats.

MD5 is used to define how parity is computed in the DS1 robbed digit-8 mode. If MD5 is low, the E signaling bit is excluded from the computation of output data parity, PY. If MD5 is high, the E signaling bit is included in the parity computation. MD5 is a "don't care" for all other modes. MD5 is not used in the 257AS device.

Table 14. Mode Register Decoding

MD0*	MD1*	MD2*	MD3*	MD4*	Line Format	Signaling Format	Output Format
0	x	0	0	0	DS1	Robbed digit-8	1.024-MHz burst
1	x	0	0	0	DS1	Robbed digit-8	Burst stuff
0	0	1	x	0	DS1	Robbed digit-8	Uniform stuff 0
0	1	1	x	0			Uniform stuff 1
1	0	1	x	0			Uniform stuff 2
1	1	1	x	0			Uniform stuff 3
0	0	0	1	0	DS1	RSM	Uniform stuff 0
0	1	0	1	0			Uniform stuff 1
1	0	0	1	0			Uniform stuff 2
1	1	0	1	0			Uniform stuff 3
x	x	0	1	1	CEPT	RSM	—
x	x	1	x	1		Word-16	—

* x = don't care. Any combination not included in the table is invalid.

Exercise Register Decoding

Exercise register bits EX0, EX1, and EX2 determine the interpretation of the device alarm and facility status register bits. In normal operation, all alarm and status bits, except DAO, are cleared and a high on the alarm or status bit represents an alarm condition. The effect of the exercise bits on each of the alarm and status bits is listed in Table 15. Device alarm bit DA0 is not affected by the exercises. Device alarm bit DA6 is exercised by sending an order with bad input parity.

Design Notes

Signaling extraction remains inhibited and device alarm bits DA2, DA3, DA5, and DA7 do not respond to alarm conditions for an additional 32 frames after the high-to-low transition on SIGINH (pin 13). This design assumes that a valid line superframe sync pulse, LSFSY (pin 4), has been received prior to the high-to-low transition on SIGINH. The T7229 and 229GB Framers release signaling inhibit as soon as they establish valid framing. This can occur prior to the first superframe sync pulse for the new frame alignment. Therefore, any design using these framers should maintain a high state on input SIGINH until after the first occurrence of the superframe sync pulse following the release of signaling inhibit by the framer.

Table 15. Effect of Exercise Bits on Device Alarm Facility Status Bits

Exercise			Alarm*						Status		
EX2	EX1	EX0	DA1	DA2	DA3	DA4	DA5	DA7	FS1	FS2	FS3
0	0	0	—	—	—	—	—	—	—	—	—
0	0	1	Inv	1	Inv	Inv	1**	1	—	—	—
0	1	0	Inv	1	Inv	Inv	—	1	—	—	—
0	1	1	—	0	—	—	1**	0	—	—	—
1	0	0	—	—	—	—	—	—	1†	—	—
1	0	1	Inv	1	Inv	Inv	1**	1	—		
1	1	0	Inv	1	Inv	Inv	—	1	—	—	—
1	1	1	—	0	—	—	1**	0	1	1	1

Notes:
— = Exercise has no effect.
Inv = Exercise inverts the state of the bit.
1 = Exercise forces bit high.
0 = Exercise forces bit low.

* Device alarm bits DA2, DA3, DA5, and DA7 do not respond to exercise if the device is in the signaling inhibit state (facility status bit FS1 = high (1)).
** Exercise is effective only in DS1 mode.
† This exercise is service-affecting. It inhibits signaling extraction.

Characteristics

Clocks

Clock	Frequency	Period	Pulse Width	Duty Cycle	Mode
LCLK	1.544 MHz	—	—	50% ± 5%	DS1
	2.048 MHz	—	—	50% ± 5%	CEPT
SCLK	4.096 MHz	—	—	50% ± 5%	All
LSFSY	—	3 ms	648 ns	—	DS1
	—	2 ms	488 ns	—	CEPT
SYSNC	—	125 μs	244 ns	—	All

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit
Input voltages:				
high	V_{IH}	2.4	—	V
low	V_{IL}	—	0.8	V
Output voltages:				
high	V_{OH}	2.4	—	V
low	V_{OL}	—	0.4	V
Output current:				
high	I_{OH}	200	—	µA
low	I_{OL}	–2.0	—	mA
high-Z	I_{OZ}	—	40	µA

Maximum Ratings

Voltage (V_{DD}) on any pin with respect to ground ..... 6.0 V
Power dissipation (PD) ..... 900 mW at 0 °C
Storage temperature (Tstg) range..... –65 to +145 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Max	Unit	Mode	Fig
tLSHLCH	Line sync set-up time	80	—	ns	All	17
tLCHLSL	Line sync hold time	80	—	ns	All	17
tLDVLCH	Data set-up time	80	—	ns	All	17
tSNHSCH	System sync set-up time	60	—	ns	All	17
tSCHSNL	System sync hold time	0	—	ns	All	17
tSCHCIV	Serial control input set-up time	0	244	ns	All	14
tSCHROV	Propagation delay SCLK to RPTOUT	0	244	ns	All	11
tSCHDSH	DGRSEL set-up time	—	244	ns	*	10
tSCHPSV	FBIT and PSEL set-up time	—	244	ns	All	7, 10
tSCHDV	Data and signaling delay time	—	244	ns	All	7, 10
tSCHPV	PDS delay time	—	344	ns	All	7, 10

* DS1 burst output.

Timing Diagram

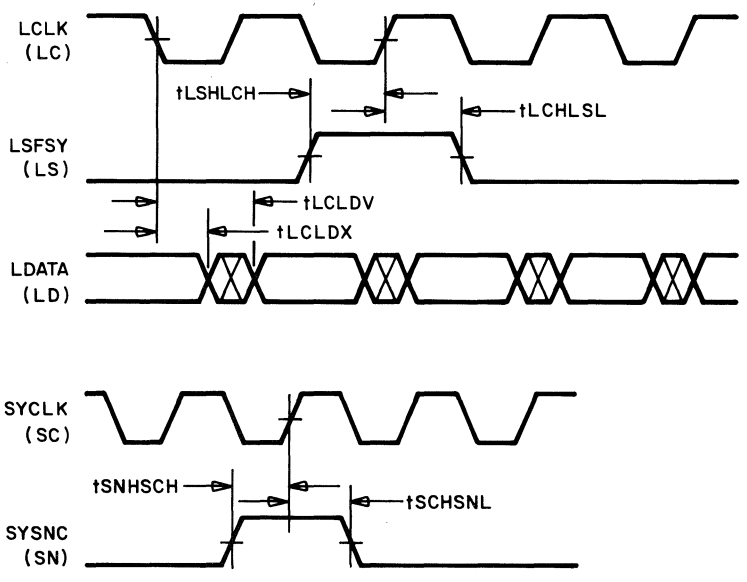


Figure 17. Clock and Data Timing

606HM Transmit Converter

Features

- Accommodates either single-rail or dual-rail unipolar input
- Provides the required overshoot on the trailing edge of the DS1 output pulse
- Contains 5 selectable equalizers
- Provides the line loopback function
- Transmits all 1s when the bank loopback is enabled

Description

The 606HM Transmit Converter hybrid integrated circuit (HIC) drives the line between a terminal or channel bank to a digital cross-connect (DSX) at either the DS1 rate (1.544 MHz) or the DS1C rate (3.152 MHz). It is available in a 40-pin ceramic HIC DIP.

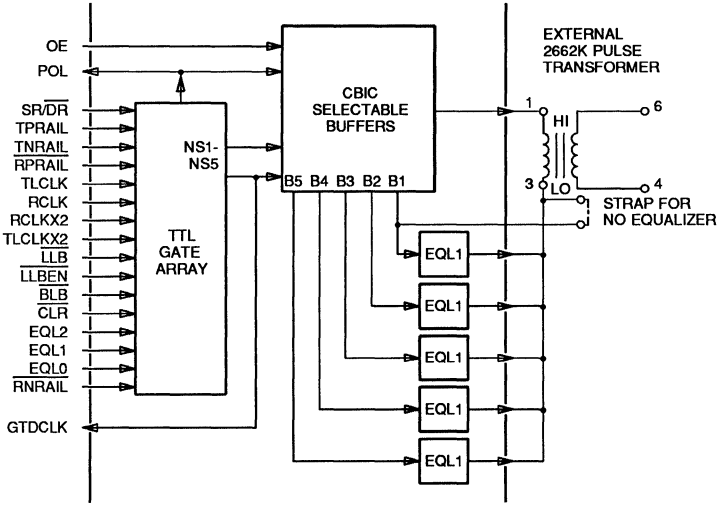
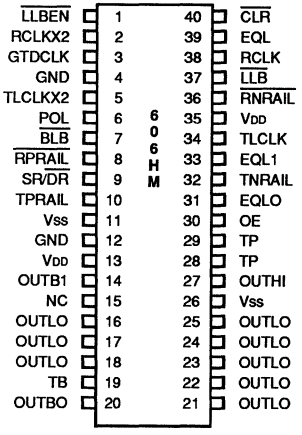


Figure 1. Transmit Converter Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
$\overline{BLB}$	7	POL	6
$\overline{CLR}$	40	RCLK	38
ELQ0	31	RCLKX2	2
ELQ1	33	$\overline{RNRAIL}$	36
ELQ2	39	$\overline{RPRAIL}$	8
GND	4, 12	SR/$\overline{DR}$	9
GTDCLK	3	TLCLK	34
$\overline{LLB}$	37	TLCLKX2	5
$\overline{LLBEN}$	1	TNRAIL	32
NC	15	TP	19, 28,
OE	30		29
OUTB1	14	TPRAIL	10
OUTHI	27	VDD	13, 35
OUTLO	16—18, 20—25	VSS	11, 26

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	$\overline{LLBEN}$	I	**Line Loopback Enable (Active Low).** When $\overline{LLBEN}$ and $\overline{LLB}$ are low, input data appears on $\overline{RPRAIL}$ (pin 8) and $\overline{RNRAIL}$ (pin 36).
2	RCLKX2	I	**Receive Clock X 2.** Frequency is two times RCLK: 3.088 MHz for DS1 operation or 6.304 MHz for DS1C operation. Used with RCLK in line loopback mode.
3	GTDCLK	O	**Gated Clock.**
4	GND	—	**Ground.**
5	TLCLKX2	I	**Transmit Line Clock X 2.** Frequency is two times TLCLK: 3.088 MHz for DS1 operation or 6.304 MHz for DS1C operation. Used with TLCLK in normal transmitter operation and bank loopback operation.
6	POL	O	**Polarity.**
7	$\overline{BLB}$	I	**Bank Loopback (Active Low).** When low, output data are all 1s. All other input data is ignored.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
8	$\overline{\text{RPRAIL}}$	I	**Receive Positive Rail (Active Low).** Single-rail or dual-rail unipolar data input line. Used in line loopback mode.
9	SR/$\overline{\text{DR}}$	I	**Single Rail/Dual Rail.** Selects either single-rail or dual-rail unipolar data input.
10	TPRAIL	I	**Transmit Positive Rail.** Single-rail or dual-rail unipolar data input line. Used in normal mode.
11	V_{SS}	—	**–5 V Supply.**
12	GRD	—	**Ground.**
13	V_{DD}	—	**+5 V Supply.**
14	OUTB1	O	**Output B1.** Connect to output of B1 Buffer.
15	NC	—	**No Connection.**
16 17 18	OUTLO	O	**Output LO.** Connect to LO on transformer.
19	TP	O	**Test Point.** Not connected during normal operation.
20 21 22 23 24 25	OUTLO	O	**Output LO.** Connect to LO on transformer.
26	V_{SS}	—	**–5 V Supply.**
27	OUTHI	O	**Output HI.** Connect to HI on transformer.
28	TP	O	**Test Point.** Not connected during normal operation.
29	TP	O	**Test Point.** Not connected during normal operation.
30	OE	I	**Overshoot Enable.** High for DS1 operation; low for DS1C operation.
31	EQL0	I	**Equalizer Select 0.** Set according to the decoder truth table (Table 2). This is the LSB.
32	TNRAIL	I	**Transmit Negative Rail.** Single-rail or dual-rail unipolar data input line. Used in normal mode.
33	EQL1	I	**Equalizer Select 1.** Set according to the decoder truth table (Table 2).
34	TLCLK	I	**Transmit Line Clock.** 1.544 MHz for DS1 operation; 3.152 MHz for DS1C operation. Used with TLCLKX2 in normal transmitter operation and bank loopback operation.
35	V_{DD}	—	**+5 V Supply.**

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
36	$\overline{\text{RNRAIL}}$	I	**Receive Negative Rail (Active Low).** Single-rail or dual-rail unipolar data input line used in line loopback mode.
37	$\overline{\text{LLB}}$	I	**Line Loopback (Active Low).** When $\overline{\text{LLB}}$ and $\overline{\text{LLBEN}}$ are low, the device is in line loopback mode.
38	RCLK	I	**Receive Clock.** Either 1.544 MHz for DS1 operation or 3.152 MHz for DS1C operation. In conjunction with RCLKX2, provides clock for line loopback mode.
39	EQL2	I	**Equalizer Select 2.** Set according to the decoder truth table (Table 2). This is the MSB.
40	$\overline{\text{CLR}}$	I	**Clear.** Held high during normal operation.

Operation

The functional block diagram of the 606HM Transmit Converter is shown in Figure 1. The complete transmit converter consists of the 606HM and a transformer, which is needed for impedance matching and powering the line.

The three major functional areas of the transmit converter are logic, buffering, and equalization. The three equalizer inputs (EQL0, EQL1, and EQL2) permit selection of the appropriate on-board equalizer to compensate for cable lengths up to 655 feet from the DSX. In the band loopback mode, the transmit converter generates an "all 1s" pattern. It can also provide the line loopback function, which allows testing of the line at the DSX.

The equalizers are selected via a 3-bit binary word that turns on the appropriate B*i* (*i* = 1—5) buffer. The selection is based on the length of cable between the channel bank and the DSX, as follows:

Cable Length in Feet	Equalizer
0 to 133	1
133 to 266	2
266 to 399	3
399 to 533	4
533 to 655	5

EQL0, EQL1, and EQL2 should be set according to the decoder truth table given in Table 2. A no-equalizer condition requires an external strap, as shown in Figure 1.

The transmit converter operates in normal, line loopback, or bank loopback mode. Figure 3 shows how the transmit converter accommodates dual-rail unipolar input in the normal mode. Data is entered via TPRAIL and TNRAIL. If the incoming bit on both rails is 0, OUTLO and OUTHI are 0. Incoming 1s are represented by alternating high and low pulses on the output; a high pulse on the output represents an incoming 1 on TPRAIL; a low pulse on the output represents an incoming 1 on TNRAIL; and two successive low or high pulses represent a violation. Data is accepted on the rising edge of the 1.544-MHz TLCK.

$\overline{\text{LLBEN}}$ and $\overline{\text{LLB}}$ must be low to transmit data in the line loopback mode. Data is entered via $\overline{\text{RPRAIL}}$ and $\overline{\text{RNRAIL}}$ in the line loopback mode the same way as data is entered via TPRAIL and TNRAIL in the normal mode, except the $\overline{\text{RPRAIL}}$ and $\overline{\text{RNRAIL}}$ inputs are active low. Data is accepted on the falling edge of the 1.544-MHz RCLK.

When $\overline{BLB}$ is low, the transmit converter operates in the bank loopback mode, TPRAIL and TNRAIL inputs are ignored, and the device transmits all 1s to indicate to the far end that maintenance is being performed.

Table 2. Equalizer Select Truth Table

EQL2	EQL1	EQL0	Equalizer
0	0	0	Invalid
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Invalid
1	1	1	Invalid

Characteristics

Clocks

Receive clock: 1.544 MHz (DS1) or 3.152 MHz (DS1C)
Receive clock X 2: 3.088 MHz (DS1) or 6.304 MHz (DS1C)
Transmit line clock: 1.544 MHz (DS1) or 3.152 MHz (DS1C)
Transmit line clock X 2: 3.088 MHz (DS1) or 6.304 MHz (DS1C)

Electrical Characteristics

T_A = 0 to 85 °C, V_{DD} = +5 V ± 0.25 V, V_{SS} = –5 V ± 0.25 V, GND = 0 V

Parameter	Symbol	Min	Max	Unit
Supply current	I_{DD}		200	mA
Input current:				
high	I_{IH}	—	40	μA
low	I_{IL}	—	–1.6	mA
Input voltage:				
high	V_{IH}	2.2	—	V
low	V_{IL}	—	0.8	V
Output (at DSX) voltage:				
high	V_{OH}	2.4	—	V
low	V_{OL}	—	0.6	V
Power dissipation	PD	—	1.6	W

Maximum Ratings

Voltage range on any pin with respect to ground ..... –0.5 to +7 V
Ambient operating temperature (TA) range ..... 0 to 85 °C
Storage temperature (Tstg) range ..... –40 to +90 °C
Power dissipation (PD) ..... 1.5 W

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

DS1/DS1C Transmit Converter

Table 3. Output Pulse Transformer Operating Conditions

Ambient temperature	0 to 85 °C
Primary pulse amplitude	4.6 V
Primary load	54 Ω (min)
Pulse width:	
DS1	324 ns
DS1C	159 ns
Repetition rate:	
DS1	1.544 MHz
DS1C	3.152 MHz

Table 4. Output Pulse Transformer Requirements

Turns ratio: 1—3 to 4—6	1:1.36 CT
Maximum rise time (20% to 80%)	35 ns
Maximum fall time	35 ns
Maximum overshoot	5%
Maximum backswing	5%
Maximum droop	1%
Maximum height of an insulated case	0.460 in

Timing Characteristics and Requirements

Table 5. Normal Mode I/O Format (See Figure 3)

Symbol	Description	Min	Typ	Max	Unit
Requirements					
tTPRHTPRL:	TPRAIL high				
DS1		647	647	648	ns
DS1C		316	316	317	ns
tTC2HTC2H:	TLCLKX2 period				
DS1		324	324	324	ns
DS1C		158	158	158	ns
tTLCHTLCH:	TLCLK period				
DS1		647	647	648	ns
DS1C		316	316	317	ns
Characteristics					
tOUTHOUTL:	OUTLO and OUTHI high				
DS1		294	324	354	ns
DS1C		128	158	188	ns
tTPRHOUTH:	TPRAIL high to OUTLO and OUTHI high				
DS1		323	323	324	ns
DS1C		157	157	158	ns

Note: DS1 corresponds to a line frequency of 1.544 MHz ± 50 ppm; DS1C corresponds to a line frequency of 3.152 MHz ± 30 ppm.

Table 6. Line Loopback Mode I/O Format (See Figure 4)

Symbol	Description	Min	Typ	Max	Unit
Requirements					
tRPRLRPRH:	RPRAIL low				
DS1		647	647	648	ns
DS1C		316	316	317	ns
tRC2HRC2H:	RCLKX2 period				
DS1		324	324	324	ns
DS1C		158	158	158	ns
tRCHRCH:	RCLK period				
DS1		647	647	648	ns
DS1C		316	316	317	ns
Characteristics					
tOUTLOUTH:	OUTLO and OUTHI low				
DS1		294	324	354	ns
DS1C		128	158	188	ns

Note: DS1 corresponds to a line frequency of 1.544 MHz ± 50 ppm; DS1C corresponds to a line frequency of 3.152 MHz ± 30 ppm.

Table 7. Bank Loopback Mode I/O Format (See Figure 5)

Symbol	Description	Min	Typ	Max	Unit
Requirements					
tTNRHTNRL:	TNRAIL high				
DS1		647	647	648	ns
DS1C		316	316	317	ns
tTC2HTC2H:	TLCLKX2 period				
DS1		324	324	324	ns
DS1C		158	158	158	ns
tTLCHTLCH:	TLCLK period				
DS1		647	647	648	ns
DS1C		316	316	317	ns
Characteristics					
tOUTHOUTL:	OUTLO and OUTHI high				
DS1		294	324	354	ns
DS1C		128	158	188	ns
tOUTLOUTH:	OUTLO and OUTHI low				
DS1		294	324	353	ns
DS1C		128	158	188	ns

Note: DS1 corresponds to a line frequency of 1.544 MHz ± 50 ppm; DS1C corresponds to a line frequency of 3.152 MHz ± 30 ppm.

Timing Diagrams

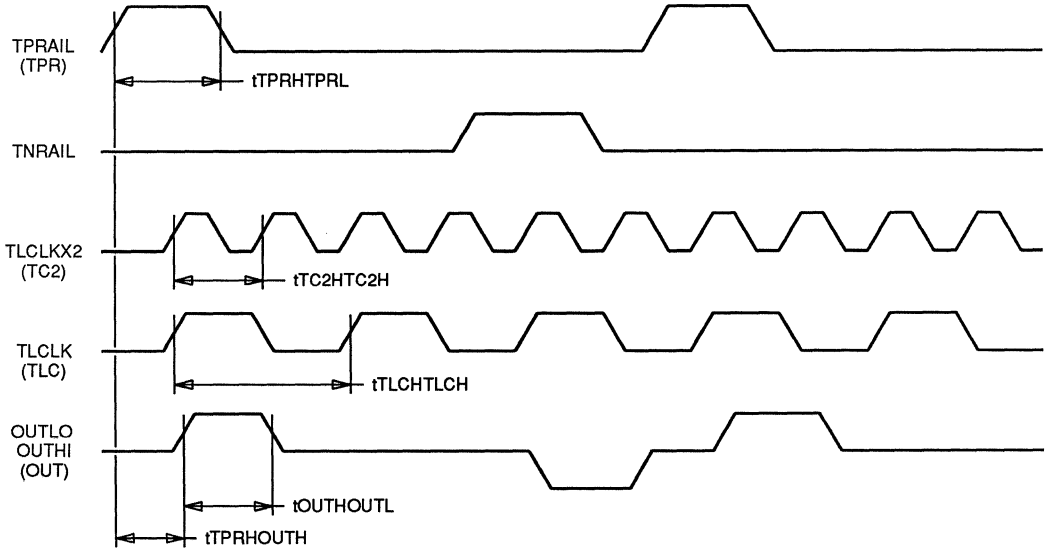


Figure 3. Normal Mode I/O Format

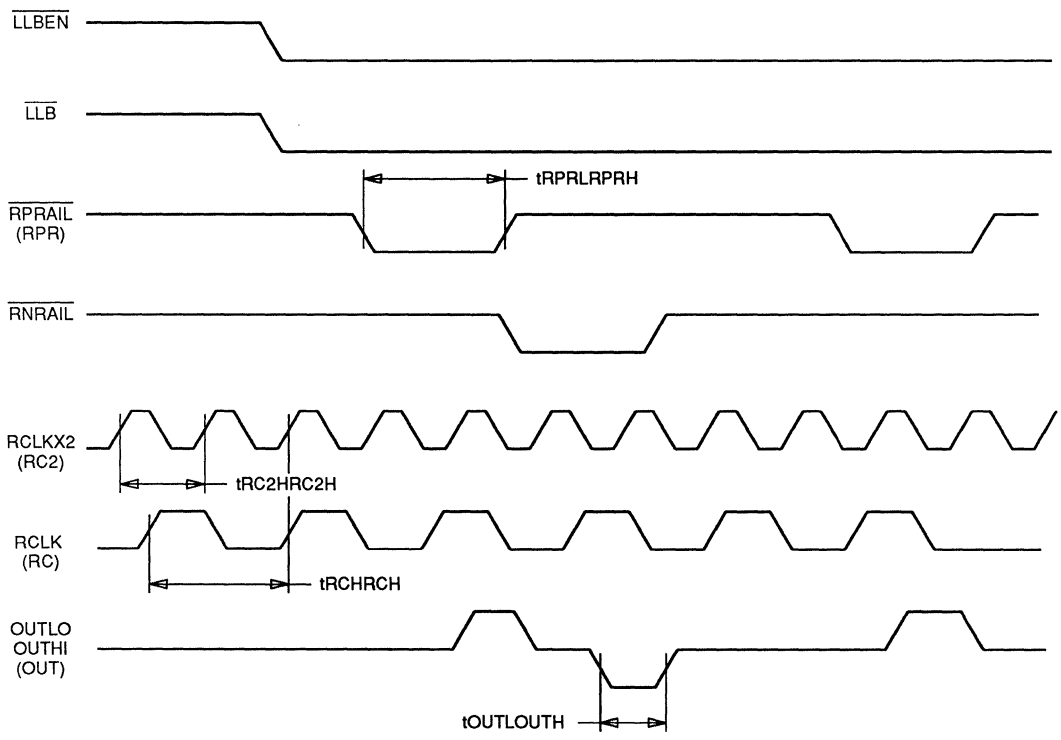


Figure 4. Line Loopback Mode I/O Format

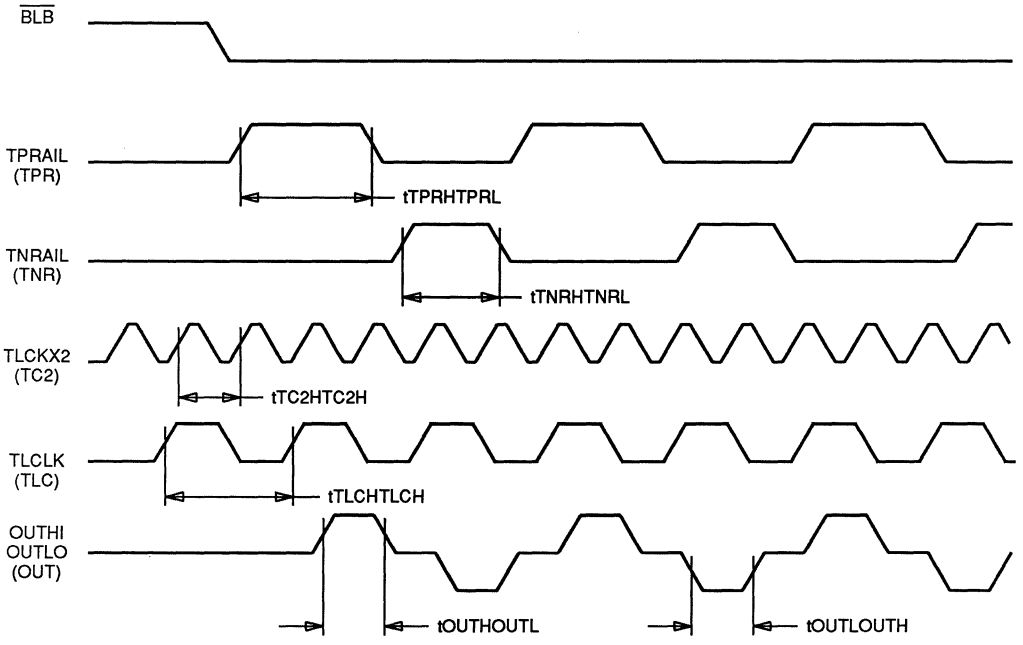


Figure 5. Bank Loopback Mode I/O Format

630AG Receive Converter

Features

- Data loopback mode
- Automatic output shutdown
- Dual-rail PCM output
- Internal phase-locked loop
- Unipolar clock output
- TTL-compatible output

Description

The 630AG Receive Converter hybrid integrated circuit (HIC) extracts clock and PCM information from the incoming bipolar digital line and regenerates unipolar clock and dual-rail PCM signals at its output for DS1 applications. A data loopback capability and an automatic output shutdown mechanism are provided. The 630AG Receive Converter is available in a 20-pin ceramic HIC DIP and requires a single 5 V supply.

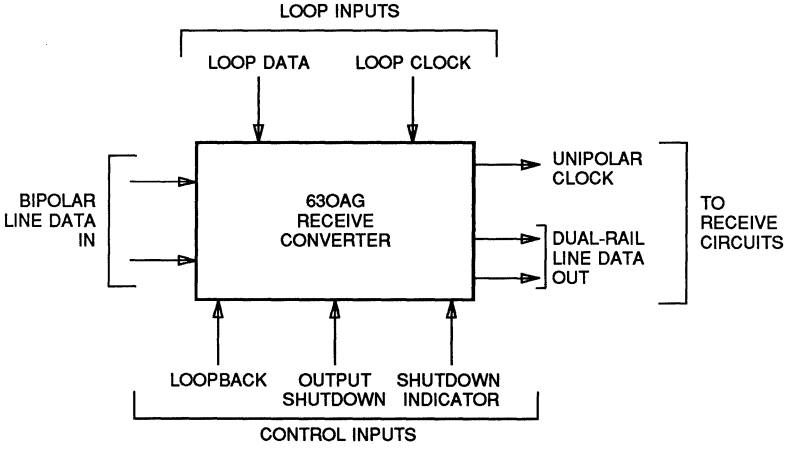
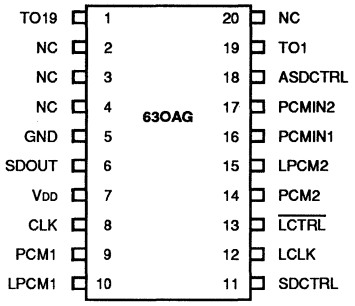


Figure 1. Receive Converter Simplified Functional Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
ASDCTRL	18	PCM1	9
CLK	8	PCM2	14
GND	5	PCMIN1	16
LCLK	12	PCMIN2	17
$\overline{\text{LCTRL}}$	13	SDCTRL	11
LPCM1	10	SDOUT	6
LPCM2	15	TO1	19
NC	2—4,	TO19	1
	20	VDD	7

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	TO19	—	**Connect to Pin 19.**
2 3 4	NC	—	**No Connection.**
5	GND	—	**Ground.**
6	SDOUT	O	**Shutdown Output.** When high, indicates output shutdown.
7	VDD	—	**5 V Supply.**
8	CLK	O	**Recovered Clock.** 1.544-MHz square-wave clock output.
9	PCM1	O	**Line Data Output 1.** In conjunction with PCM2 (pin 14), provides dual-rail output.
10	LPCM1	I	**Loop Line Data 1.** When high, input for data loopback mode is looped back to the input via LPCM1 and LPCM2 (pin 15).
11	SDCTRL	I	**Shutdown Control.** When tied to ASDCTRL (pin 18), turns off the clock and PCM outputs if there is a loss of incoming signal. This feature is disabled by tying SDCTRL high.
12	LCLK	I	**Loop Clock.** Clock signal used in loopback mode.
13	$\overline{\text{LCTRL}}$	I	**Loop Control.** When low, inputs LPCM1 and LPCM2 are inverted and looped back to outputs PCM1 and PCM2.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
14	PCM2	O	**Line Data Output 2.** In conjunction with PCM1 (pin 9), provides dual-rail output.
15	LPCM2	I	**Loop Line Data Input 2.** When high, input for data loopback mode is looped back to the input via LPCM2 and LPCM1 (pin 10).
16	PCMIN1	I	**Line Data Input 1.** Bipolar line data input from the digital line.
17	PCMIN2	I	**Line Data Input 2.** Bipolar line data input from the digital line.
18	ASDCTRL	O	**Automatic Shutdown Control.** Active when tied to SDCTRL (pin 11). Turns off the clock and PCM outputs if there is a loss of incoming signal.
19	TO1	—	**Connect to Pin 1.**
20	NC	—	**No Connection.**

Operation

The primary functions of the 630AG Receive Converter (RCV) are to extract clock and PCM information from the incoming 1.544-MHz bipolar digital line and to regenerate unipolar clock and dual-rail PCM signals.

The incoming signal is applied to the RCV at PCMIN1 and PCMIN2. A transformer and resistor network is needed to provide the proper impedance match to the 100-Ω twisted-pair line (see Figure 3). The RCV converts this bipolar signal to a dual-rail, 100% duty cycle, TTL-compatible signal. The dual-rail output is required to detect bipolar violations. The nominal bipolar signal measured at pins 16 and 17 is 6 Vpp, with the minimum and maximum values at 2 Vpp and 12 Vpp, respectively.

The RCV contains a phase-locked loop (PLL) to extract the clock from the line signal. The extracted clock appears at CLK. The PLL free-running frequency is preadjusted to 1.544 MHz. In order for the RCV to lock onto the incoming signal, there must be a minimum density of at least one 1 every 16 bits (i.e., a maximum of fifteen 0s in a row).

Timing for the dual rail signal is shown in Figure 4. If the incoming PCM bit is a 0, both rails are high. Incoming 1s are represented by a low pulse on one rail only, with the low pulse alternating between the two rails for successive incoming data bits that are equal to 1. Two successive low pulses on the same rail represents a bipolar violation. Data is accepted on the falling edge of the 1.544-MHz clock.

An automatic output shutdown mechanism is incorporated to turn off the clock and PCM outputs if there is a loss of incoming signal. This feature is enabled by tying SDCTRL to ASDCTRL and is disabled by tying SDCTRL high.

Approximately 400 μs after the last 1 has been received, the voltage level on ASDCRTL is 0. If the automatic output shutdown mechanism is being used (SDCTRL tied to ASDCTRL), the clock stops and SDOUT goes high, indicating that a shutdown condition exists.

For maintenance purposes, a data loopback feature is provided. A low at the $\overline{\text{LCTRL}}$ input puts the 630AG in loopback mode. When the receive converter is in the loopback mode, the clock signal is taken from LCLK and is not extracted from the incoming data. The data entered via LPCM1 and LPCM2 is the inverse of the data output on PCM1 and PCM2. The automatic output shutdown feature is not available in the loopback mode.

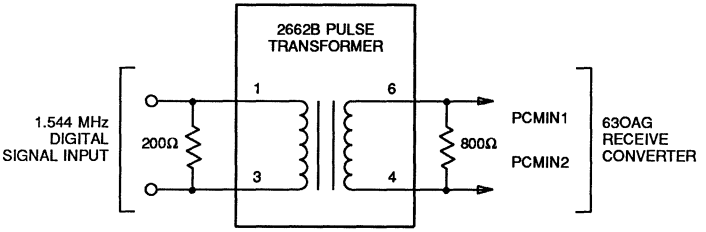


Figure 3. Transformer and Resistor Network

Characteristics

Clocks

Recovered clock: 1.544 MHz
Loop clock: 1.544 MHz

Electrical Characteristics

T_A = 0 to 85 °C, V_{DD} = 5 V ± 0.5 V, GND = 0 V

Parameter	Symbol	Min	Max	Unit
Supply current	I_{DD}	—	80	mA
Input current:				
high	I_{IH}	—	40	μA
low	I_{IL}	—	−1.6	mA
Output current:				
high	I_{OH}	—	−0.4	mA
low	I_{OL}	—	3	mA
Input voltage:				
high	V_{IH}	2.2	V_{DD}	V
low	V_{IL}	—	0.8	V
Output voltage:				
high	V_{OH}	2.4	V_{DD}	V
low	V_{OL}	—	0.6	V
Power dissipation	PD	—	400	mW

Maximum Ratings

Voltage range on any pin with respect to ground ..... −0.5 to +7 V
Ambient operating temperature (T_A) range ..... 0 to 85 °C
Storage temperature (Tstg) range ..... −40 to +90 °C
Power dissipation (PD) ..... 400 mW

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

The external leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics and Requirements

Table 2. Normal Mode I/O Format (See Figure 4)

Symbol	Description	Min	Typ	Max	Unit
Requirements					
tLDIHLDIL	Line data input high	294	324	354	ns
tCLKHCLKH	CLK period*	647	647	648	ns
Characteristics					
tASDLCLKO	ASDCTRL low to CLK off	—	0	—	μs
tLDIHPCM1L	LDI high to PCM1 low	—	324	—	ns
tPCMPW	PCM1 pulse width	647	647	648	ns
tASDLSDOH	ASD low to SDOUT high	—	0	—	μs
tLDILASDL	Input data zero to ASDL low	—	400	—	μs

* This corresponds to a line frequency of 1.544 MHz ± 50 ppm.

Table 3. Loopback Mode I/O Format (See Figure 5)

Symbol	Description	Min	Typ	Max	Unit
Requirements					
tLCLKHLCLKH	Loop CLK period	647	647	648	ns
tLPCM1HLPCM1L	LPCM1 high	647	647	648	ns

Timing Diagrams

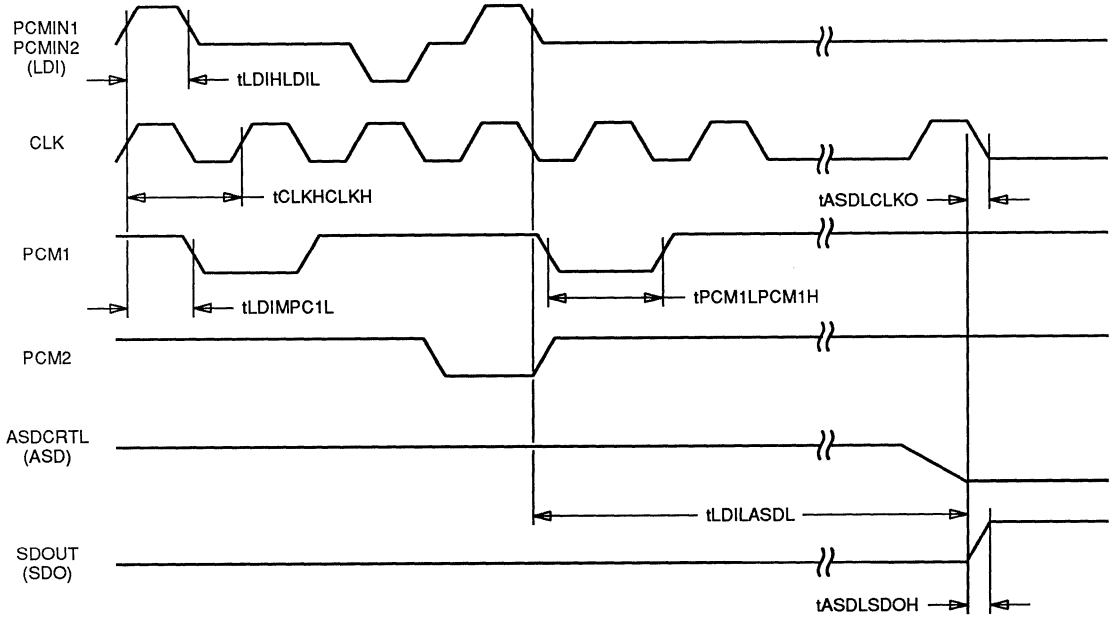


Figure 4. Normal Mode I/O Format

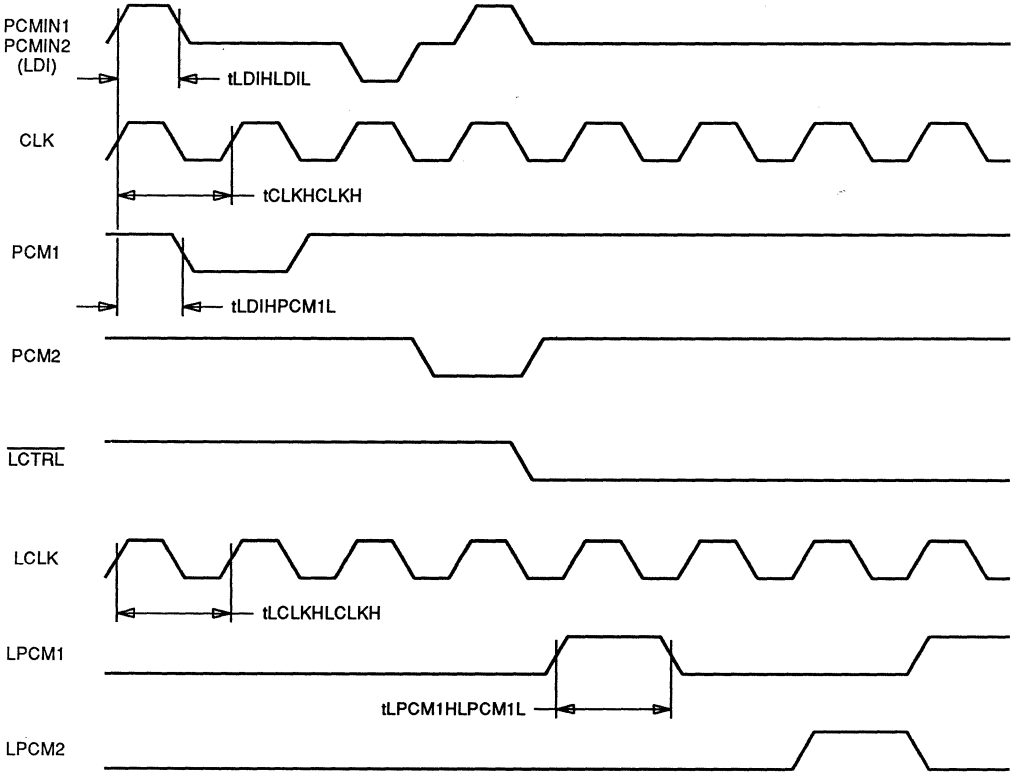


Figure 5. Loopback Mode I/O Format

630AJ Receive Converter

Features

- Data loopback mode
- Automatic output shutdown
- Dual-rail PCM output
- Internal phase-locked loop
- Unipolar clock output
- TTL-compatible output

Description

The 630AJ Receive Converter hybrid integrated circuit (HIC) extracts clock and PCM information from the incoming bipolar digital line and regenerates unipolar clock and dual-rail PCM signals at its output for DS1E applications. A data loopback capability and an automatic output shutdown mechanism are provided. The 630AJ Receive Converter is available in a 20-pin ceramic HIC DIP and requires a single 5 V supply.

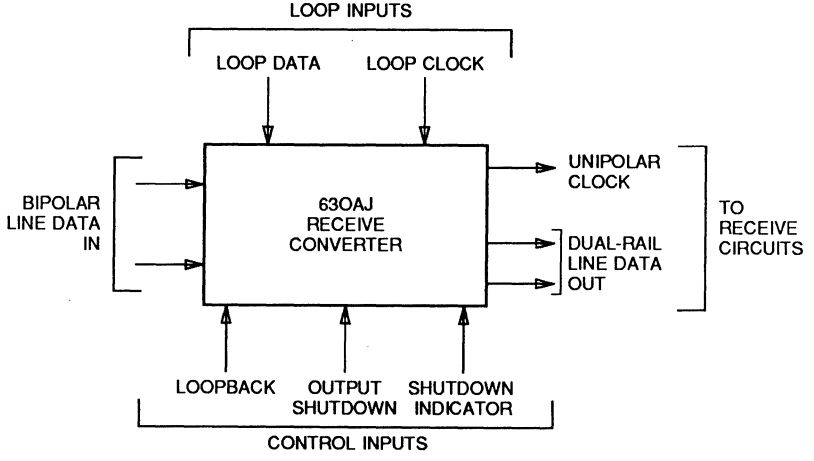
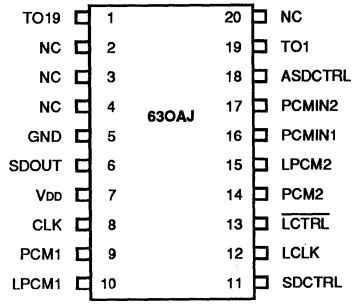


Figure 1. Simplified Functional Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
ASDCTRL	18	PCM1	9
CLK	8	PCM2	14
GND	5	PCMIN1	16
LCLK	12	PCMIN2	17
$\overline{\text{LCTRL}}$	13	SDCTRL	11
LPCM1	10	SDOUT	6
LPCM2	15	TO1	19
NC	2—4, 20	TO19	1
		VDD	7

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	TO19	—	**Connect to Pin 19.**
2 3 4	NC	—	**No Connection.**
5	GND	—	**Ground.**
6	SDOUT	O	**Shutdown Output.** When high, indicates output shutdown.
7	VDD	—	**5 V Supply.**
8	CLK	O	**Recovered Clock.** 2.048-MHz square-wave clock output.
9	PCM1	O	**Line Data Output 1.** In conjunction with PCM2 (pin 14), provides dual-rail output.
10	LPCM1	I	**Loop Line Data 1.** When high, input for data loopback mode is looped back to the input via LPCM1 and LPCM2 (pin 15).
11	SDCTRL	I	**Shutdown Control.** When tied to ASDCTRL (pin 18), turns off the clock and PCM outputs if there is a loss of incoming signal. This feature is disabled by tying SDCTRL high.
12	LCLK	I	**Loop Clock.** Clock signal used in loopback mode.
13	$\overline{\text{LCTRL}}$	I	**Loop Control.** When low, inputs LPCM1 and LPCM2 are inverted and looped back to outputs PCM1 and PCM2.

Table 1. 630AJ Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
14	PCM2	O	**Line Data Output 2.** In conjunction with PCM1 (pin 9), provides dual-rail output.
15	LPCM2	I	**Loop Line Data Input 2.** When high, input for data loopback mode is looped back to the input via LPCM2 and LPCM1 (pin 10).
16	PCMIN1	I	**Line Data Input 1.** Bipolar line data input from the digital line.
17	PCMIN2	I	**Line Data Input 2.** Bipolar line data input from the digital line.
18	ASDCTRL	O	**Automatic Shutdown Control.** Active when tied to SDCTRL (pin 11). Turns off the clock and PCM outputs if there is a loss of incoming signal.
19	TO1	—	**Connect to Pin 1.**
20	NC	—	**No Connection.**

Operation

The primary functions of the 630AJ Receive Converter (RCV) are to extract clock and PCM information from the incoming 2.048-MHz bipolar digital line and to regenerate unipolar clock and dual-rail PCM signals.

The incoming signal is applied to the RCV at PCMIN1 and PCMIN2. A transformer and resistor network is needed to provide the proper impedance match to the 100-Ω twisted-pair line (see Figure 3). The RCV converts this bipolar signal to a dual-rail, 100% duty cycle, TTL-compatible signal. The dual-rail output is required to detect bipolar violations. The nominal bipolar signal measured at pins 16 and 17 is 6 Vpp, with the minimum and maximum values at 2 Vpp and 12 Vpp, respectively.

The RCV contains a phase-locked loop (PLL) to extract the clock from the line signal. The extracted clock appears at CLK. The PLL free-running frequency is preadjusted to 2.048 MHz. In order for the RCV to lock onto the incoming signal, there must be a minimum density of at least one 1 every 16 bits (i.e., a maximum of fifteen 0s in a row).

Timing for the dual rail signal is shown in Figure 4. If the incoming PCM bit is a 0, both rails are high. Incoming 1s are represented by a low pulse on one rail only, with the low pulse alternating between the two rails for successive incoming data bits that are equal to 1. Two successive low pulses on the same rail represents a bipolar violation. Data is accepted on the falling edge of the 2.048-MHz clock.

An automatic output shutdown mechanism is incorporated to turn off the clock and PCM outputs if there is a loss of incoming signal. This feature is enabled by tying SDCTRL to ASDCTRL and is disabled by tying SDCTRL high.

Approximately 400 μs after the last 1 has been received, the voltage level on ASDCRTL is 0. If the automatic output shutdown mechanism is being used (SDCTRL tied to ASDCTRL), the clock stops and SDOUT goes high, indicating that a shutdown condition exists.

For maintenance purposes, a data loopback feature is provided. A low at the $\overline{\text{LCTRL}}$ input puts the 630AJ in loopback mode. When the receive converter is in the loopback mode, the clock signal is taken from LCLK and is not extracted from the incoming data. The data entered via LPCM1 and LPCM2 is the inverse of the data output on PCM1 and PCM2. The automatic output shutdown feature is not available in the loopback mode.

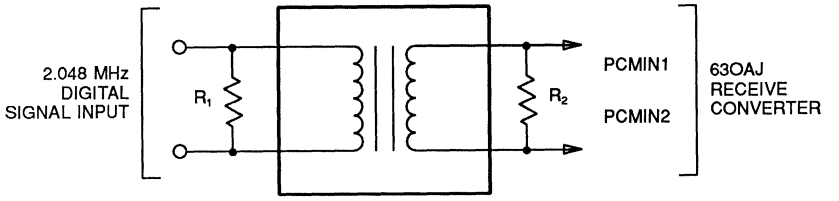


Figure 3. Transformer and Resistor Network

Characteristics

Clocks

Recovered clock: 2.048 MHz
Loop clock: 2.048 MHz

Electrical Characteristics

T_A = 0 to 85 °C, V_{DD} = 5 V ± 0.5 V, GND = 0 V

Parameter	Symbol	Min	Max	Unit
Supply current	I_{DD}	—	80	mA
Input current:				
high	I_{IH}	—	40	μA
low	I_{IL}	—	−1.6	mA
Output current:				
high	I_{OH}	—	−0.4	mA
low	I_{OL}	—	3	mA
Input voltage:				
high	V_{IH}	2.2	V_{DD}	V
low	V_{IL}	—	0.8	V
Output voltage:				
high	V_{OH}	2.4	V_{DD}	V
low	V_{OL}	—	0.6	V
Power dissipation	PD	—	400	mW

Maximum Ratings

Voltage range on any pin with respect to ground ..... −0.5 to +7 V
Ambient operating temperature (T_A) range ..... 0 to 85 °C
Storage temperature (Tstg) range ..... −40 to +90 °C
Power dissipation (PD) ..... 400 mW

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

The external leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics and Requirements

Table 2. Normal Mode I/O Format (See Figure 4)

Symbol	Description	Min	Typ	Max	Unit
Requirements					
tLDIHLDIL	Line data input high	221	244	267	ns
tCLKHCLKH	CLK period*	488	488	489	ns
Characteristics					
tASDLCLKO	ASDCTRL low to CLK off	—	0	—	μs
tLDIHPCM1L	LDI high to PCM1 low	—	244	—	ns
tPCMPW	PCM1 pulse width	488	488	489	ns
tASDLSDOH	ASD low to SDOUT high	—	0	—	μs
tLDILASDL	Input data zero to ASDL low	—	400	—	μs

* This corresponds to a line frequency of 2.048 MHz ± 50 ppm.

Table 3. Loopback Mode I/O Format (See Figure 5)

Symbol	Description	Min	Typ	Max	Unit
Requirements					
tLCLKHLCLKH	Loop CLK period	488	488	489	ns
tLPCM1HLPCM1L	LPCM1 high	488	488	489	ns

Timing Diagrams

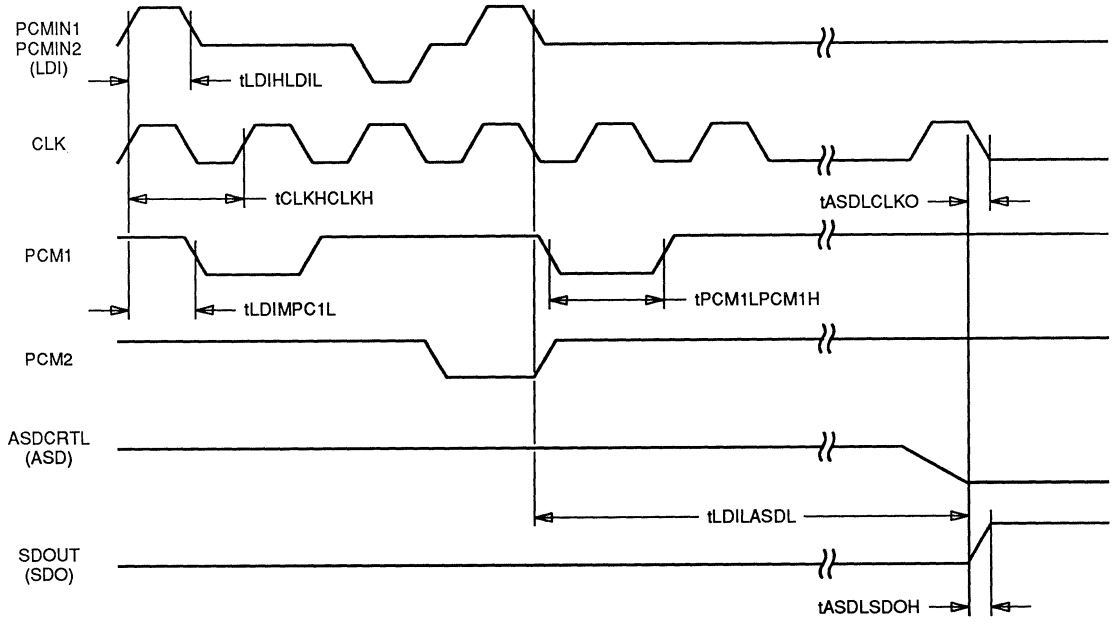


Figure 4. Normal Mode I/O Format

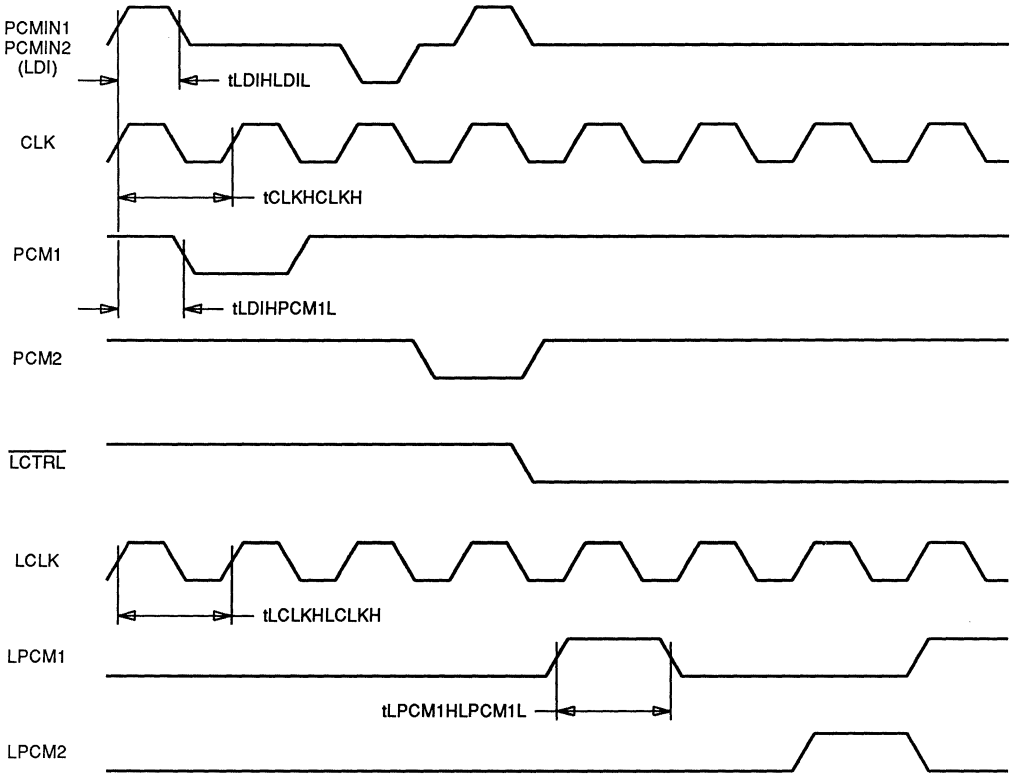


Figure 5. Loopback Mode I/O Format

LC1046A Digital Signaling Interface

Features

- Fully-integrated DS1/DS1C line interface
- Complies with *Compatibility Bulletin 119* (*CB119*) and *PUB 43802* specifications
- On-chip transmit equalization
- Monolithic clock recovery
- Pin-selectable B8ZS encoder and decoder
- Loopback modes for fault isolation
- Multiple link status and alarm features
- Minimal external circuitry required

Description

The LC1046A Digital Signaling Interface (DSI) is an integrated circuit that provides a line interface between the DS1 or DS1C cross-connect (DSX) and terminal equipment circuits for cable distances of up to 655 feet for 22-gauge plastic insulated cable (PIC). It performs receive pulse regeneration, timing recovery, and transmit pulse shaping and equalization functions. The LC1046A DSI device is manufactured using 1.75-micron CMOS technology and is available in a 28-pin plastic DIP or small-outline J-lead (SOJ) package for surface mounting. The digital circuitry is shown in Figure 1. The analog circuitry is shown in Figure 6.

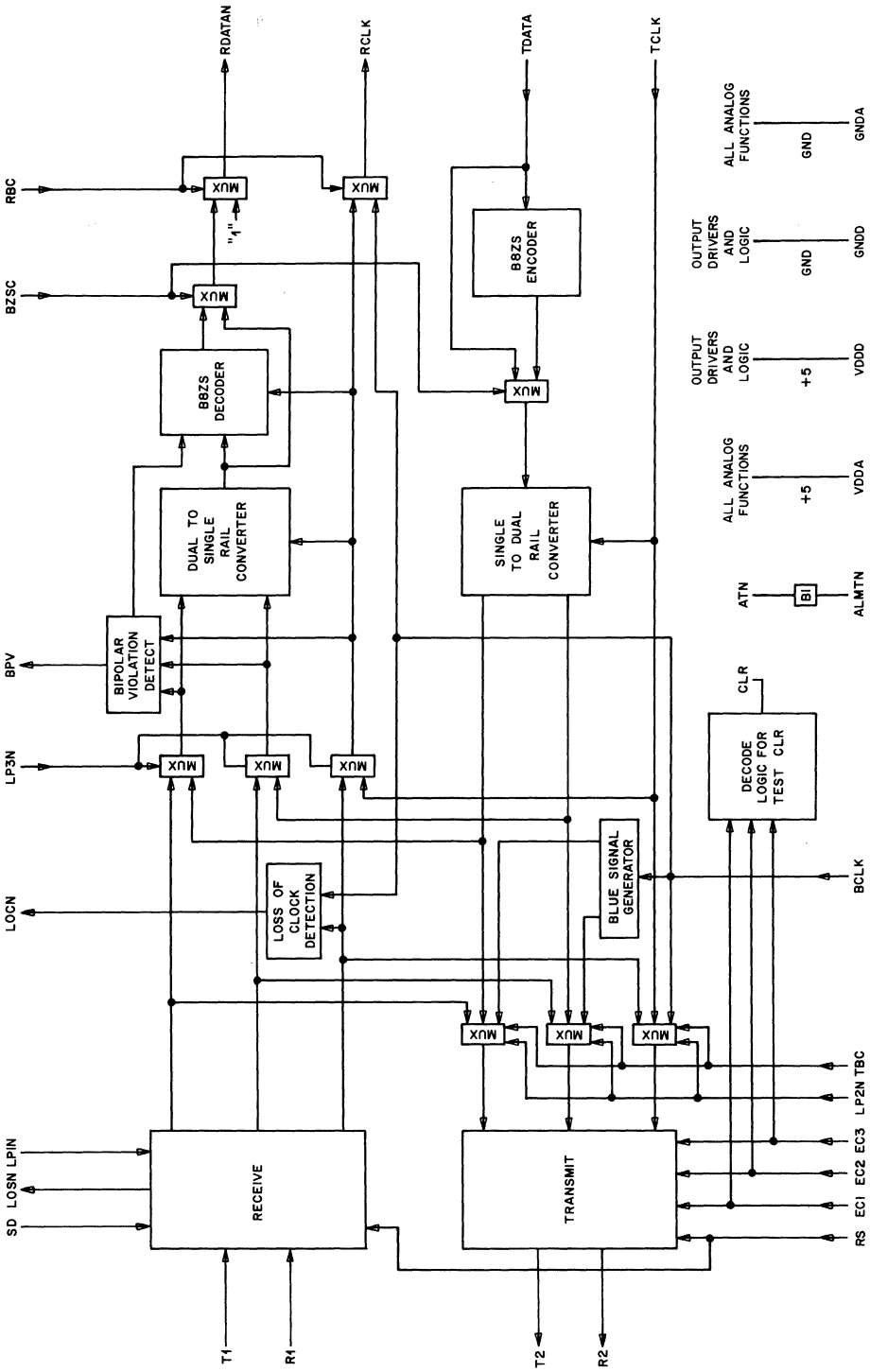


Figure 1. Block Diagram

User Information

Pin Descriptions

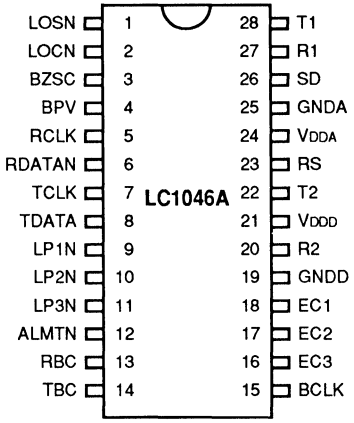


Figure 2. Pin Function Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	LOSN	O	**Loss-of-Signal Not.** This pin is cleared (0) upon loss of the data signal at the receiver inputs.
2	LOCN	O	**Loss-of-Clock Not.** This pin is cleared when SD = 1 and LOSN = 0, indicating that a loss of clock has occurred. When LOCN = 0, no transitions occur on RCLK and RDATAN outputs. A valid clock must be present at BCLK for this function to operate properly.
3	BZSC	I	**B8ZS Enable.** This pin is set (1) when inserting a B8ZS substitution code on the transmit side and when removing the substitution code on the receive side.
4	BPV	O	**Bipolar Violation.** This pin is set upon detection of a bipolar violation on the receive-side input after removal of the legal B8ZS substitution code.
5	RCLK	O	**Receive Clock.** Output receive clock signal to the terminal equipment.
6	RDATAN	O	**Receive Data Not.** 1.544-Mb/s inverted unipolar output data (DS1) or 3.152-Mb/s data (DS1C). This data has a 100% duty cycle.
7	TCLK	I	**Transmit Clock.** DS1 input clock signal (1.544 MHz ± 130 ppm) or DS1C input clock signal (3.152 MHz ± 30 ppm).
8	TDATA	I	**Transmit Data.** 1.544-Mb/s unipolar input data (DS1) or 3.152-Mb/s data (DS1C).

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
9	LP1N	I	**Loopback 1 Enable Not.** This pin is cleared for a full local loopback (transmit converter output to receive converter input). Most of the transmit and receive analog circuitry is exercised in this loopback.
10	LP2N	I	**Loopback 2 Enable Not.** This pin is cleared for a remote loopback (DSX to DSX). In loopback 2, a high on TBC (pin 14) inserts the blue signal on the transmit side.
11	LP3N	I	**Loopback 3 Enable Not.** This pin is cleared for a digital local loopback. Only the transmit and receive digital sections are exercised in this loopback.
12	ALMTN	I	**Alarm Test Enable Not.** This pin is cleared, forcing LOSN = 0, LOCN = 0, and BPV = 1 for testing without affecting data transmission.
13	RBC	I	**Receive Blue Control.** This pin is set to insert the blue signal on the receive side.
14	TBC	I	**Transmit Blue Control.** This pin is set to insert the blue signal on the transmit side. This control has priority over a loopback 2 if both are operated.
15	BCLK	I	**Blue Clock.** DS1 blue clock signal (1.544 MHz ± 130 ppm) or DS1C blue clock signal (3.152 MHz ± 30 ppm) input. This clock is independent of the transmit clock.
16	EC3	I	**Equalizer Control 3.*** One of three control leads for selecting transmit equalizers.
17	EC2	I	**Equalizer Control 2.*** One of three control leads for selecting transmit equalizers.
18	EC1	I	**Equalizer Control 1.*** One of three control leads for selecting transmit equalizers.
19	GNDD	—	**Digital Ground.**
20	R2	O	**Transmit Bipolar Ring.** Negative bipolar transmit output.
21	V_{DDD}	—	**5 V Digital Supply (± 10%).**
22	T2	O	**Transmit Bipolar Tip.** Positive bipolar transmit output.
23	RS	I	**Rate Select.** This pin is cleared for DS1 operation and set for DS1C operation.
24	V_{DDA}	—	**5 V Analog Supply (± 10%).**
25	GNDA	—	**Analog Ground.**
26	SD	I	**Shutdown Enable.** This pin is set, forcing RCLK and RDATAN high and LOCN low if a loss of signal is detected (LOSN = 0).
27	R1	I	**Receive Bipolar Ring.** Negative bipolar receive input.
28	T1	I	**Receive Bipolar Tip.** Positive bipolar receive input.

* See Table 2.

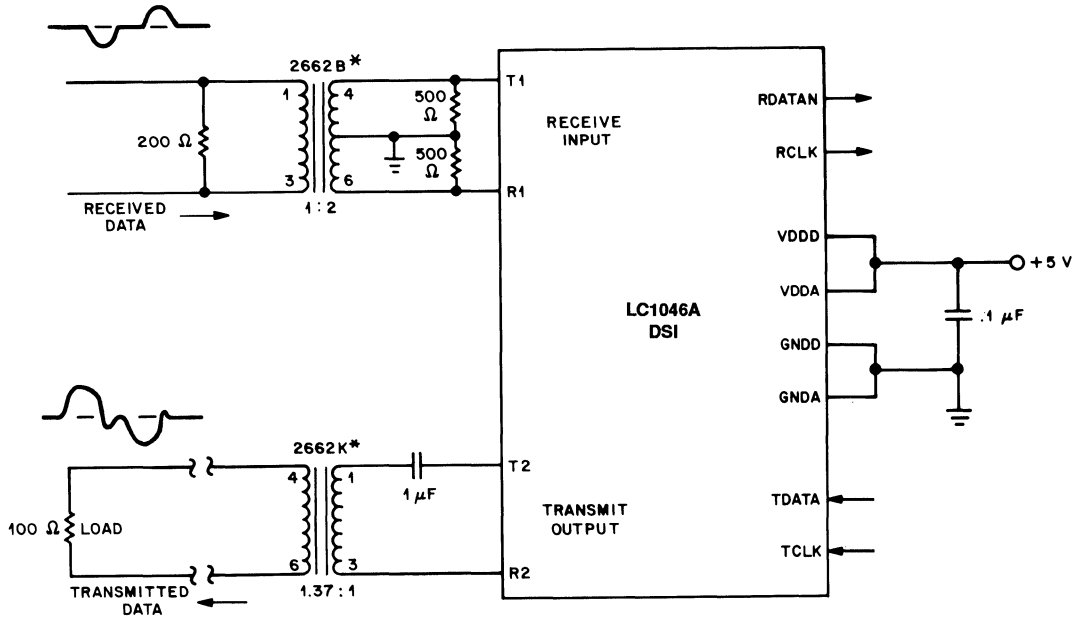
Table 2. Equalizer Control*

Distance to DSX (Ft.)** (Applies only to 22-Ga. PIC (ABAM) Cable)	Maximum Cable Loss (dB at 772 kHz)	EC1	EC2	EC3
0—133	.6	0	0	0
133—267	1.2	0	0	1
267—400	1.8	0	1	0
400—533	2.4	0	1	1
533—655	3	1	0	0
Test clear	—	1	0	1

* Other bit combinations represent test modes – not to be used for normal operation.
** Use maximum loss figures for other cable types.

Overview

The LC1046A is a fully-integrated digital signaling interface (DSI) that requires only two line interface transformers, three input termination resistors, and one capacitor to provide a bidirectional line interface between a DS1 or DS1C cross-connect (DSX) and terminal equipment. A typical application diagram is shown in Figure 3. This device is specified for use with 22-gauge plastic insulated ABAM cable, as well as other cable types. The circuit is divided into three main blocks: transmit converter, receive converter, and logic. The transmit and receive converters process information signals through the device in the transmit and receive directions, respectively; the logic is the control and status interface for the device.



* A step-up transformer is used.

Figure 3. Typical Application Diagram for Bipolar Signal Interfacing

Transmit Converter

The line interface transmission format is return-to-zero, bipolar alternate mark inversion (AMI), requiring transmission and sensing of alternately positive and negative pulses. The transmit converter accepts unipolar data and clock, and converts the signal to a balanced bipolar data signal. Binary 1s in the data stream become pulses of alternating polarity transmitted between the two output rails, T2 and R2. Binary 0s are transmitted as null pulses. All necessary transmit pulse shaping is done on-chip, eliminating the need for external shaping networks. This is done by shaping the pulses at the bipolar output (T2, R2) according to the selected equalizer control (EC1—EC3) inputs (see Table 2).

The output pulse waveform consists of four distinct levels: overshoot, pulse, backswing, and tail. They are produced by a high-speed D/A converter and are driven onto the line by using low-impedance output buffers. There are five different pulse shapes, corresponding to 133-foot increments of cable, that are obtained by setting the appropriate equalizer control inputs. The entire transmit analog path is fully differential, which guarantees symmetrical positive and negative pulses. The resulting pulses meet the amplitude, rise and fall time, overshoot, undershoot, template, and power requirements for the office DSX cross-connect as given in *Compatibility Bulletin 119*. A typical DS1 output waveform at the DSX relative to the *CB119* template is shown in Figure 4, and a typical output waveform at the transformer secondary is shown in Figure 5. The analog circuitry is shown in Figure 6.

The clock multiplier uses a phase-lock loop to produce the high-speed timing waveforms needed by the D/A converter. The clock multiplier also eliminates the need for the tightly controlled transmit clock duty cycle usually required in discrete implementations. Transmitter specifications are given in Table 3.

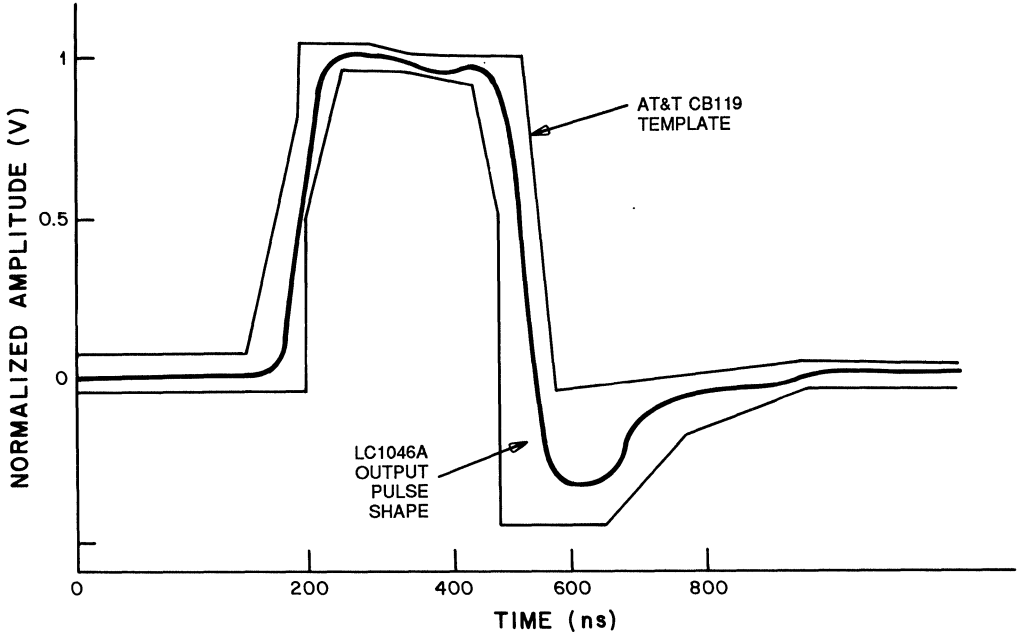
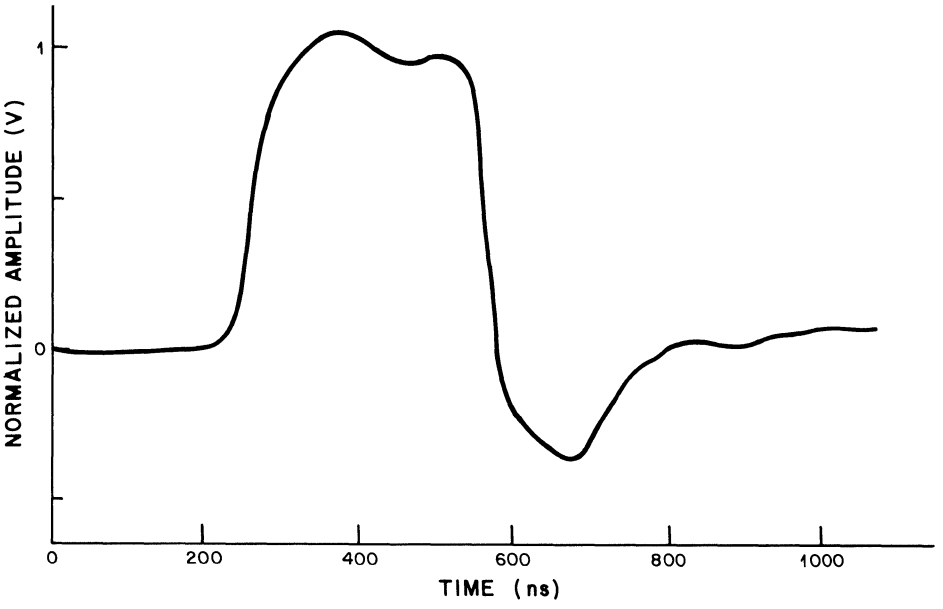


Figure 4. Typical DS1 Output Waveform at DSX



Note: EC1 = 0, EC2 = 1, EC3 = 0.

Figure 5. Typical DS1 Output Waveform at Transformer Secondary

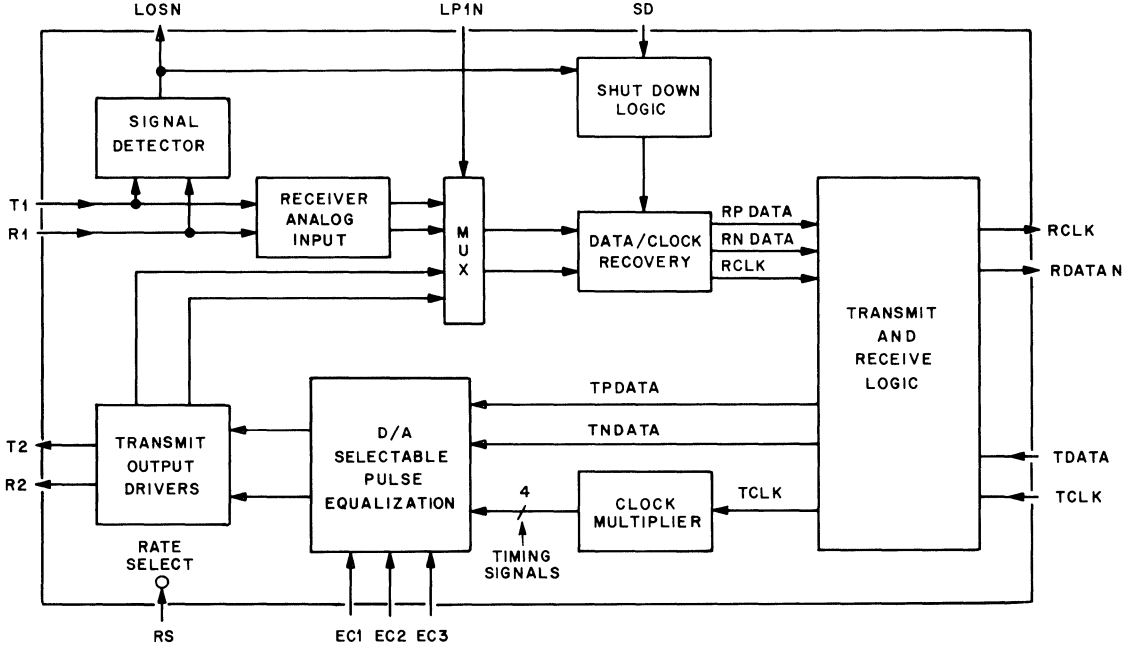


Figure 6. Analog Block Diagram

Table 3. Transmitter Specifications

Parameter	Min	Typ	Max	Unit
Output pulse amplitude (at the DSX):				
DS1	2.4	3.0	3.6	V
DS1C	2.3	3.0	3.7	V
Pulse width (50%):				
DS1	330	350	370	ns
DS1C	139	159	179	ns
Output power levels:				
DS1				
2-kHz band at 772 kHz	12.6	16.5	18.5	dBm
2-kHz band at 1544 kHz	−29	−39	—	dB*
DS1C				
10-kHz band at 1576 kHz	14.5	16.5	18.5	dBm
10-kHz band at 3152 kHz	−29	−39	—	dB**
Positive/negative pulse imbalance	—	—	0.5	dB
Rise/fall time (20%—80%), DS1C	—	—	50	ns
Overshoot, DS1C	—	—	10	%†
Zero level, DS1C	—	—	10	%†
Rise/fall time imbalance, DS1C	—	—	20	ns
Output termination	95	100	105	Ω
Output transformer turns ratio (2662K type)	1:1.30	1:1.37	1:1.44	—

* Below the power at 772 kHz.
** Below the power at 1576 kHz.
† Percentage of the pulse amplitude.

Receive Converter

The receive converter accepts bipolar input signals (T1, R1), coupled through a receive transformer, from the cross-connect over a maximum of 655 feet of 22-gauge PIC (ABAM) cable. The received signal is rectified while the amplitude and rise time are restored. These input signals are peak-detected and sliced by the receiver front-end, producing the digital signals PDATA and NDATA (Figure 6). The timing is extracted by means of phase-locked loop (PLL) circuitry that locks an internal, free-running, current-controlled oscillator (ICO) to the 1.544-MHz (DS1 signal) or 3.152-MHz (DS1C signal) component.

The PLL employs a 3-state phase detector and a low-voltage/temperature coefficient, current-controlled oscillator (ICO). The ICO free-running frequency is trimmed to within ± 2.5% of the data rate at wafer probe, with V_{DD} = 5.0 V and T_A = 25 °C. For all operating conditions (see the Operating Conditions section), the free-running oscillator frequency deviates from the data rate by less than ± 7%, alleviating the problem of harmonic lock.

Due to the clock output of the receive converter being derived from the ICO, a free-running clock can be present at the output of the receive converter without data being present at the input. A shutdown pin (SD) is provided to block this clock if desired, eliminating the free-running clock upon loss of the input signal. Table 4 is a truth table showing the shutdown operation under various conditions.

The PLL is designed to accommodate large amounts of input jitter with high power supply rejection for operation in noisy environments. Low jitter sensitivity to power supply noise allows compact line card layouts employing many DSIs on one board. The minimum input jitter tolerance, as specified in AT&T *Publication 43802* (*PUB 43802*), and the measured DSI jitter tolerance are shown for both the DS1 and DS1C rates in Figures 7 and 8, respectively. Receiver specifications are shown in Table 5.

Table 4. Shutdown Operation Truth Table

Inputs				Outputs		
LP1N	SD	Input Signal	Loopback Signal*	LOSN	LOCN	Receive Side
1	0	Normal	x	1	1	Normal
1	0	No signal	x	0	1	Free-running VCO
1	1	Normal	x	1	1	Normal
1	1	No signal	x	0	0	No output
0	0	Normal	Normal	1	1	Normal loopback
0	0	Normal	No signal	1	1	Free-running VCO
0	0	No signal	Normal	0	1	Normal loopback
0	0	No signal	No signal	0	1	Free-running VCO
0	1	Normal	Normal	1	1	Normal loopback
0	1	Normal	No signal	1	1	Free-running VCO
0	1	No signal	Normal	0	0	No output
0	1	No signal	No signal	0	0	No output

* x = don't care.

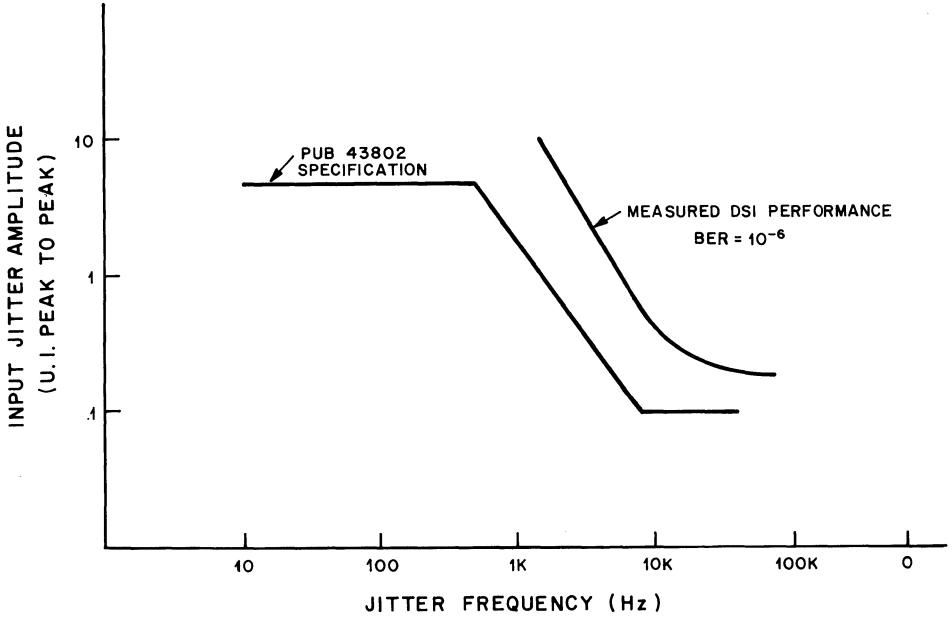


Figure 7. DS1 Jitter Tolerance

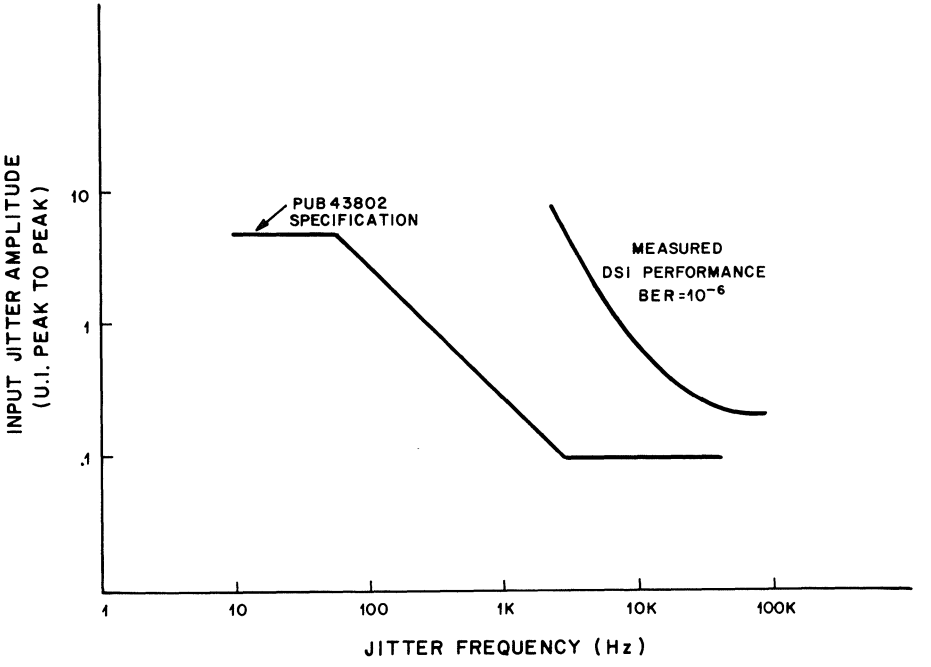


Figure 8. DS1C Jitter Tolerance

Table 5. Receiver Specifications

Parameter	Min	Typ	Max	Unit
Receiver sensitivity (at input of device)	1.0	—	—	Vp
PLL jitter:*				
DS1				
3dB bandwidth	—	20	—	kHz
peaking	—	1.4	—	dB
DS1C				
3dB bandwidth	—	18	—	kHz
peaking	—	1.4	—	dB
V_{DD} noise (BER = 10^{-9})**	—	0.8	—	Vpp
Input density (1s)†	12.5	—	—	%
ICO free-running frequency error	—	—	± 7	%
Input transformer turns ratio (2662B type)	1:1.9	1:2.0	1:2.1	—
Input termination	—	100	—	Ω

* Transfer characteristics (1/8 input).
** The point of maximum sensitivity is a sine wave at 11 kHz (pseudorandom data).
† The maximum number of consecutive 0s = 15.

Digital Logic

The logic provides alarms, optional B8ZS coding, blue signal insertion circuits, and maintenance loopbacks. It also performs dual-rail to single-rail conversion of the data.

Alarms. A loss-of-signal alarm occurs when the input signal amplitude is below the threshold needed for clock recovery. A loss-of-signal indicator in the receive front-end detects the loss of sufficient amplitude at R1 and T1. The LOSN alarm is triggered if the input data is approximately 0.5 V in amplitude. Hysteresis (250mV) is provided to prevent LOSN chattering.

An independent loss-of-clock output (LOCN) is also provided so that loss-of-clock is detected when the shutdown option is in effect. LOSN and LOCN can be wire-ORed to produce a single alarm.

A bipolar violation output is included, giving an alarm each time a violation (two or more successive 1s on a rail) occurs. The violation alarm output is held in a latch for one cycle of the internal clock (RCLK). In the B8ZS mode, bipolar violations within the legal substitution code are not detected and, therefore, do not produce an alarm.

An alarm test pin (ALMTN) is provided to test the alarm outputs, LOSN, LOCN, and BPV. Clearing this pin forces the alarm outputs to the alarm state without affecting data transmission.

B8ZS Option. The LC1046A DSI contains a B8ZS encoder and decoder that can be selected by setting the BZSC pin. This allows the encoder to substitute a zero-substitution code for eight consecutive 0s detected in the data stream, as illustrated in Table 6. A "V" represents a violation of bipolar code and a "B" represents a bipolar pulse of correct polarity. The decoder detects the zero-substitution code and reinserts eight 0s in the data stream.

Table 6. B8ZS Substitution Code

Before B8ZS	00000000
After B8ZS	000VB0VB

Blue Signal Generators. There are two blue signal generators in this device. One substitutes an all-1s blue signal on the RDATAN output toward the terminal equipment. The other substitutes a bipolar all-1s blue signal for the bipolar data out of the transmit converter to keep line repeaters active.

Loopback Paths. The DSI has three independent loopback paths, which are activated by clearing the respective control inputs, LP1N, LP2N, or LP3N. Loopback 1 bridges the data stream from the transmit converter (transmit converter included) to the input of the receive converter. This maintenance loop includes most of the internal circuitry.

Loopback 2 provides a loopback of data and recovered clock from the bipolar inputs (T1, R1) to the bipolar outputs of the transmit converter (T2, R2). The receive front-end, receive PLL, and transmit driver circuitry are all exercised. This loop can be used to isolate failures between systems.

Loopback 3 loops the data stream as in loopback 1 but bypasses the transmit and receive converters. The blue signal can be transmitted towards the DSX when in this loopback. Loopbacks 2 and 3 can be operated simultaneously to provide transmission loops in both directions.

Characteristics

Logic Interface Electrical Characteristics

T_A = −40 to +85 °C; V_{DD} = 5 V ± 10%

Parameter	Symbol	Min	Max	Unit
Input voltage:				
low	V_{IL}	GNDD	0.8	V
high	V_{IH}	2.0	V_{DDD}	V
Output voltage:				
low	V_{OL}	GNDD	0.4	V
high	V_{OH}	2.4	V_{DDD}	V
Input capacitance	C_I	—	20	pF
Load capacitance	C_L	—	40	pF
Source current	Isource	—	80	μA
Sink current	Isink	—	2.0	mA

Internal pull-up resistors are provided on the following input leads: LP1N, LP2N, LP3N, and ALMTN. Internal pull-down devices are provided on the following leads: SD, RBC, BZSC, TBC, RS, EC1, EC2, and EC3. The internal pull-up or pull-down devices require the input to source or sink to be no more than 20 μA.

Operating Conditions

−40 °C ≤ T_A ≤ +85 °C, except as noted

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	VDD	4.5	5.0	5.5	V
Power dissipation*	PD	—	300	400	mW

* Measurement conditions with 50% 1s on the transmit side, T_A = 25 °C, and equalizer settings: EC1 = 0, EC2 = 1, EC3 = 0 (V_{DD} = 5 V).

Maximum Ratings

DC supply voltage (V_{DD}) range ..... −0.5 to +6.5 V
Power dissipation (PD) ..... 1 W
Storage temperature (Tstg) range ..... −65 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

Timing Characteristics

All duty cycle and timing relationships are referenced to a TTL 1.4 V threshold level.

Loss-of-Clock Indication Timing. The clock leaving must be absent 5.18 μs (DS1) or 2.54 μs (DS1C) to guarantee a loss-of-clock indication. However, it is possible to produce a loss-of-clock indication if the clock is absent for 2.59 μs (DS1) or 1.27 μs (DS1C), depending on the timing relationship of the interruption with respect to the timing cycle.

The clock returning must be present 5.18 μs (DS1) or 2.54 μs (DS1C) to guarantee a normal condition on the loss-of-clock pin (LOCN). However, the loss-of-clock indication can return to normal immediately, depending on the timing relationship of the signal return with respect to the timing cycle.

Symbol	Description	Min	Typ	Max	Unit
tTCLTCL	TCLK clock period	*	647.7**	*	ns
tTCHTCL	TCLK duty cycle	40	50	60	%
tTDVTCL	Data set-up time, TDATA to TCLCK	50	—	—	ns
tTCLTDV	Data hold time, TCLK to TDATA	40	—	—	ns
tr	Clock rise time	—	—	40†	ns
tf	Clock fall time	—	—	40†	ns
tRCHRDV	Data hold time, RCLK to RDATAN, BPV:				
	DS1	227	—	—	ns
	DS1C	111	—	—	ns
tRDVRCH	Data set-up time, RDATAN, BPV to RCLK:				
	DS1	187	—	—	ns
	DS1C	113	—	—	ns
tRCLRDV	Propagation delay, RCLK to RDATAN	—	—	40	ns

* A tolerance of ± 130 ppm.
** 317.3 at DS1C rate.
† 20 at DS1C rate.

Timing Diagrams

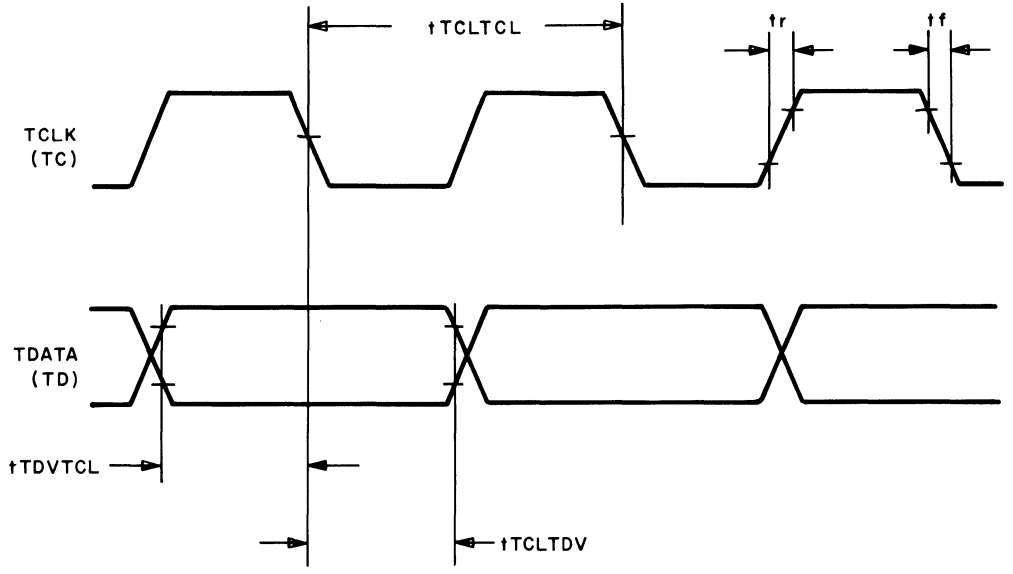


Figure 9a. Timing Diagram

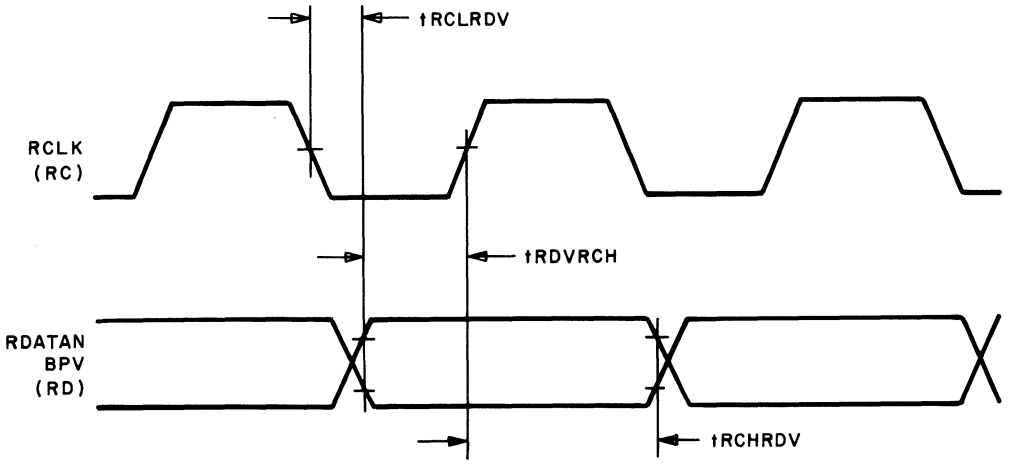


Figure 9b. Timing Diagram

LC1135B Digital Signaling Interface

Features

- Fully-integrated 2.048-Mb/s line interface
- Complies with CCITT specifications G.703 and G.823
- Pin-selectable 75-Ω or 120-Ω operation
- Monolithic clock recovery
- Minimal external circuitry required
- Low power dissipation – 75 mW for 120-Ω twisted pair and 78 mW for 75-Ω coaxial, typical operating conditions
- Pin-selectable HDB3 encoder and decoder
- Loopback modes for fault isolation
- Multiple link-status and alarm features

Description

The LC1135B Digital Signaling Interface (DSI) is an integrated circuit that provides a 2.048-Mb/s line interface to either twisted-pair or coaxial cable as specified in CCITT requirements G.703 and G.823. It performs receive pulse regeneration, timing recovery, and transmit pulse driving functions. The DSI device is manufactured using 1.75-micron CMOS technology and is available in a 28-pin plastic DIP or small-outline J-lead (SOJ) package for surface mounting. The digital circuitry is shown in Figure 1. The analog circuitry is shown in Figure 6.

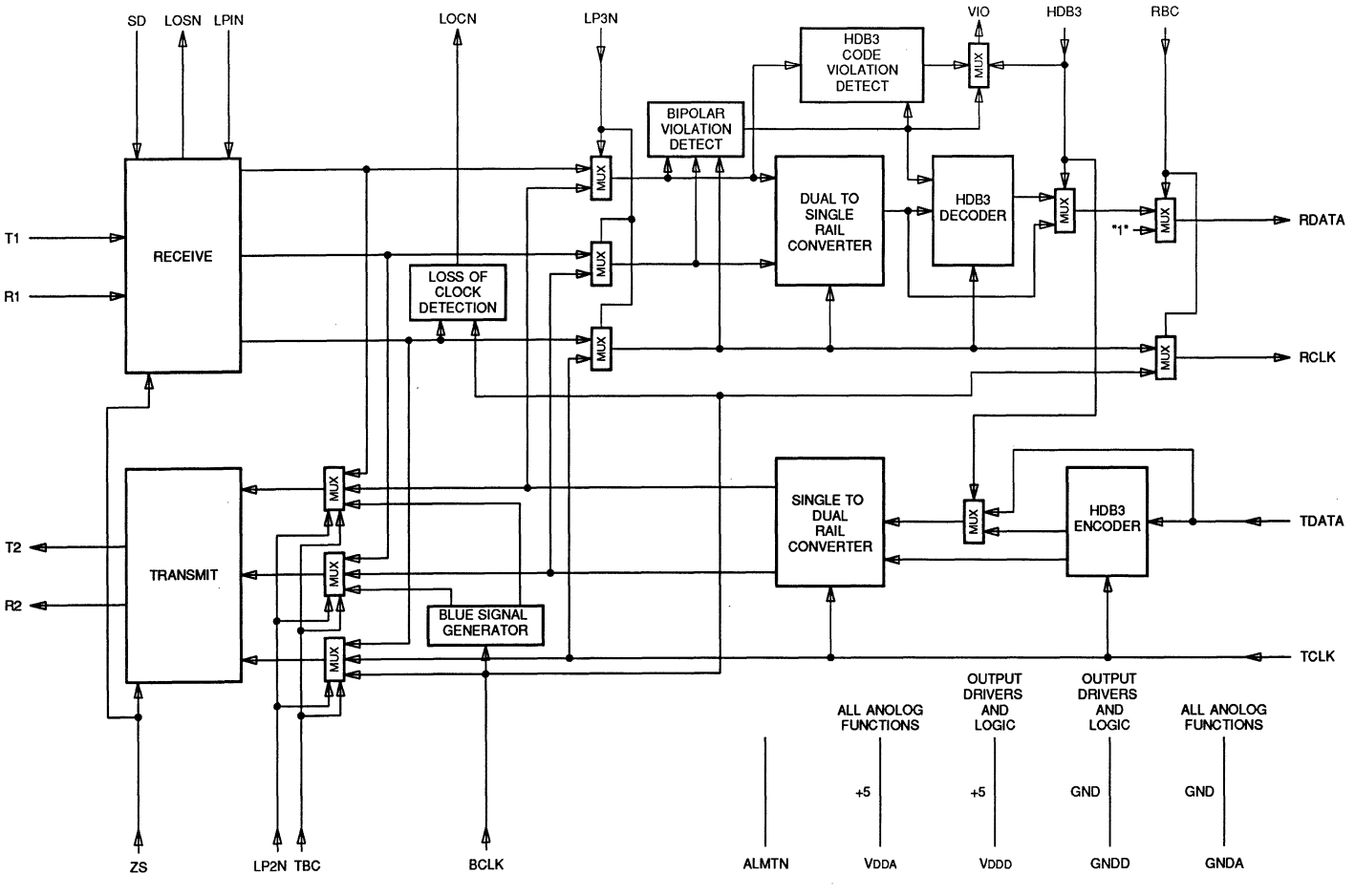


Figure 1. Block Diagram

User Information

Pin Descriptions

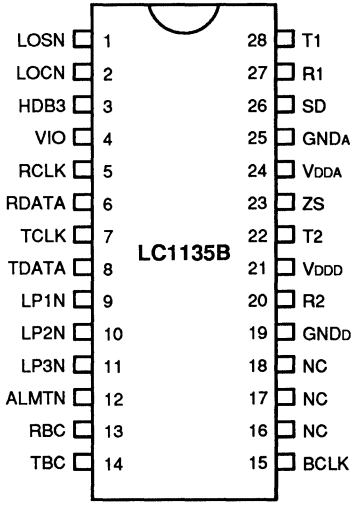


Figure 2. Pin Function Diagram

Table 1. Pin Descriptions

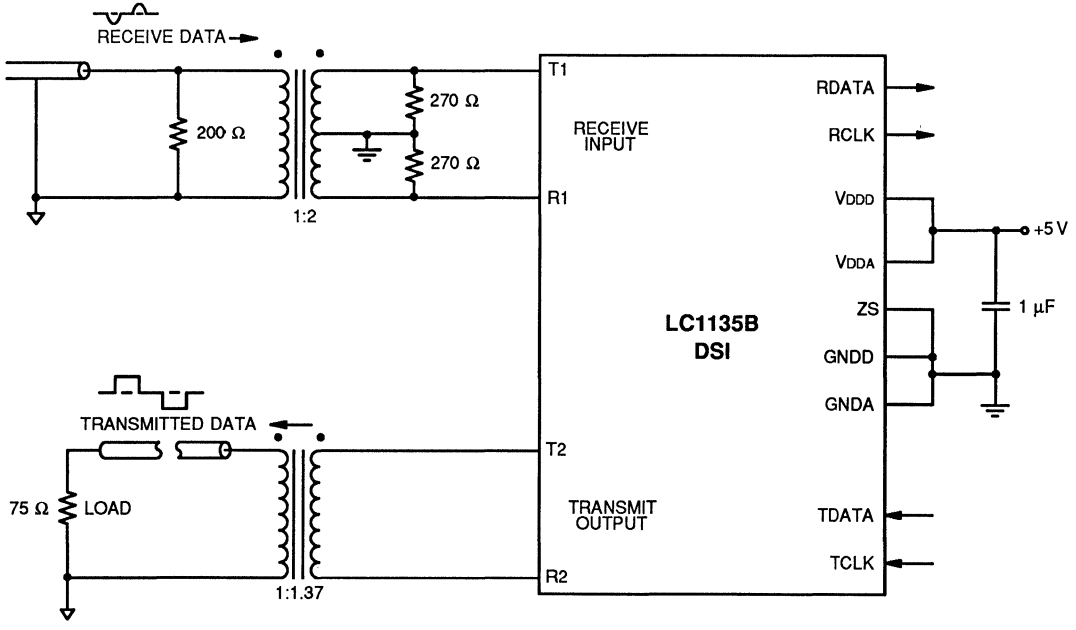
Pin	Symbol	Type	Name/Function
1	LOSN	O	**Loss of Signal Not.** This pin is cleared (0) upon loss of the data signal at the receiver inputs.
2	LOCN	O	**Loss of Clock Not.** This pin is cleared when SD = 1 and LOSN = 0, indicating that a loss of clock has occurred. When LOCN = 0, no transitions occur on RCLK and RDATA outputs. A valid clock must be present at BCLK for this function to operate properly.
3	HDB3	I	**HDB3 Enable.** This pin is set (1) when inserting an HDB3 substitution code on the transmit side and when removing the substitution code on the receive side.
4	VIO	O	**Violation.** If HDB3 = 0, bipolar violations on the receive-side input are detected, causing VIO to be set; if HDB3 = 1, HDB3 code violations cause VIO to be set.
5	RCLK	O	**Receive Clock.** Output receive clock signal to the terminal equipment.
6	RDATA	O	**Receive Data.** 2.048-Mb/s unipolar output data, with a 100% duty cycle.
7	TCLK	I	**Transmit Clock.** Input clock signal (2.048 MHz ± 50 ppm).
8	TDATA	I	**Transmit Data.** 2.048-Mb/s unipolar input data.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
9	LP1N	I	**Loopback 1 Enable Not.** This pin is cleared for a full local loopback (transmit converter output to receive converter input). Most of the transmit and receive analog circuitry is exercised in this loopback.
10	LP2N	I	**Loopback 2 Enable Not.** This pin is cleared for a remote loopback. In loopback 2, a high on TBC (pin 14) inserts the blue signal on the transmit side.
11	LP3N	I	**Loopback 3 Enable Not.** This pin is cleared for a digital local loopback. Only the transmit and receive digital sections are exercised in this loopback.
12	ALMTN	I	**Alarm Test Enable Not.** This pin is cleared, forcing LOSN = 0, LOCN = 0, and VIO = 1, for testing without affecting data transmission.
13	RBC	I	**Receive Blue Control.** This pin is set to insert the blue signal on the receive side.
14	TBC	I	**Transmit Blue Control.** This pin is set to insert the blue signal on the transmit side. This control has priority over a loopback 2 if both are operated.
15	BCLK	I	**Blue Clock.** Blue clock signal (2.048 MHz ± 50 ppm) input. This clock is independent of the transmit clock.
16 17 18	NC	—	**No Connection.**
19	GNDD	—	**Digital Ground.**
20	R2	O	**Transmit Bipolar Ring.** Negative bipolar transmit output.
21	V_{DDD}	—	**5 V Digital Supply (± 10%).**
22	T2	O	**Transmit Bipolar Tip.** Positive bipolar transmit output.
23	ZS	I	**Impedance Select.** This pin is cleared for 75-Ω coaxial cable operation and set for 120-Ω shielded twisted-pair operation.
24	V_{DDA}	—	**5 V Analog Supply (± 10%).**
25	GNDA	—	**Analog Ground.**
26	SD	I	**Shutdown Enable.** This pin is set, forcing RCLK high and RDATA low, and LOCN low if a loss of signal is detected (LOSN = 0).
27	R1	I	**Receive Bipolar Ring.** Negative bipolar receive input.
28	T1	I	**Receive Bipolar Tip.** Positive bipolar receive input.

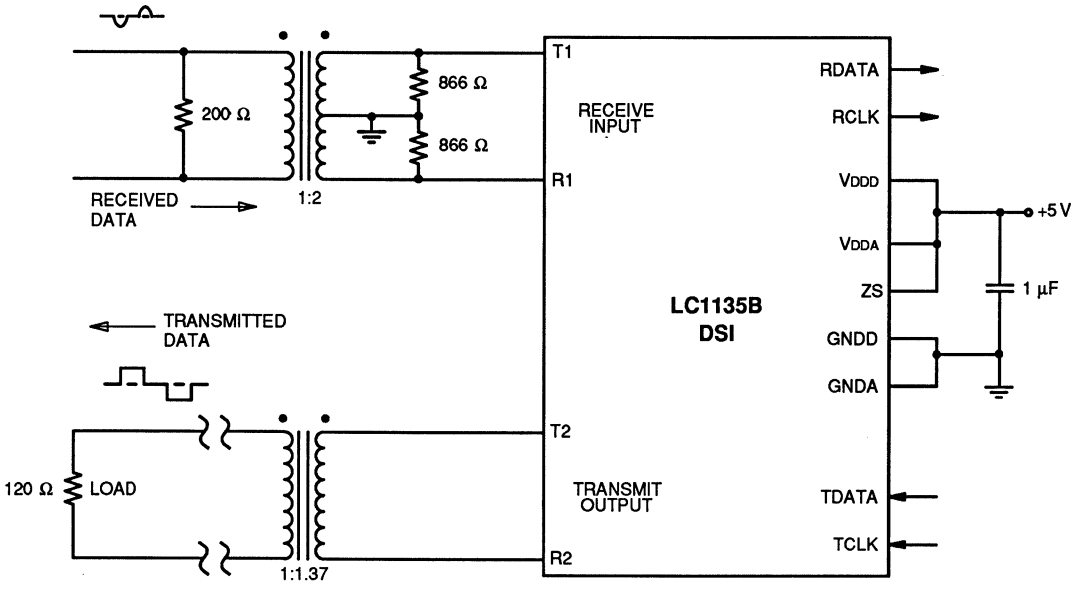
Overview

The LC1135B DSI is a fully integrated digital signaling interface that requires only two line interface transformers and three input termination resistors to provide a bidirectional line interface between a 2.048-Mb/s CEPT datalink and terminal equipment. Typical application diagrams are shown in Figures 3 and 4 for 75-Ω coaxial cable and 120-Ω shielded twisted-pair operation, respectively. The circuit is divided into three main blocks: transmit converter, receive converter, and logic. The transmit and receive converters process information signals through the device in the transmit and receive directions, respectively; the logic is the control and status interface for the device.



Note: AT&T 2741 series pulse transformers are recommended.

Figure 3. Typical Application Diagram for Coaxial Environment



Note: AT&T 2741 series pulse transformers are recommended.

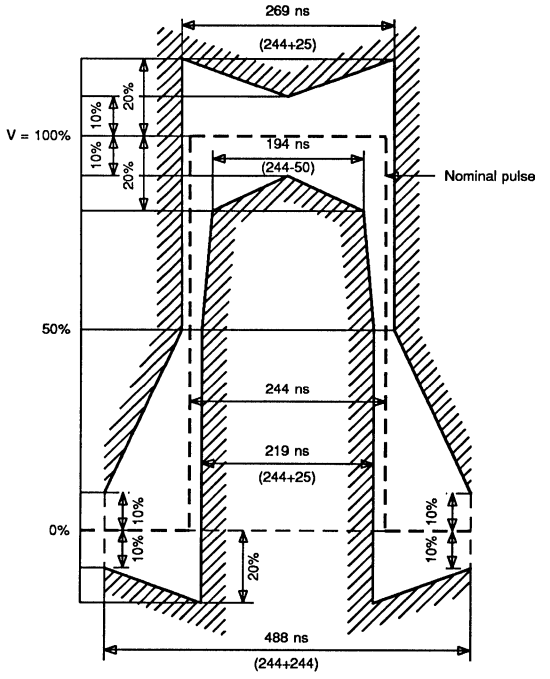
Figure 4. Typical Application Diagram for Shielded Twisted-Pair Environment

Transmit Converter

The line interface transmission format is return-to-zero, bipolar alternate mark inversion (AMI), requiring transmission and sensing of alternately positive and negative pulses. The transmit converter accepts unipolar data and clock, and converts the signal to a balanced bipolar data signal. Binary 1s in the data stream become pulses of alternating polarity transmitted between the two output rails, T2 and R2. Binary 0s are transmitted as null pulses.

The output pulse waveform is nominally rectangular. The pulses are produced by a high-speed D/A converter and are driven onto the line by low-impedance output buffers. The positive and negative pulses meet CCITT specification G.703 template requirements. The normalized pulse template is shown in Figure 5. The analog circuitry is shown in Figure 6.

The clock multiplier shown in Figure 6 uses a phase-locked loop to produce the high-speed timing waveforms needed to produce a well-controlled pulse width. The clock multiplier eliminates the need for the tightly controlled transmit clock duty cycle usually required in discrete implementations. Transmitter specifications are given in Table 2.



Note: V corresponds to the nominal peak value.

Figure 5. CCITT G.703 Pulse Template

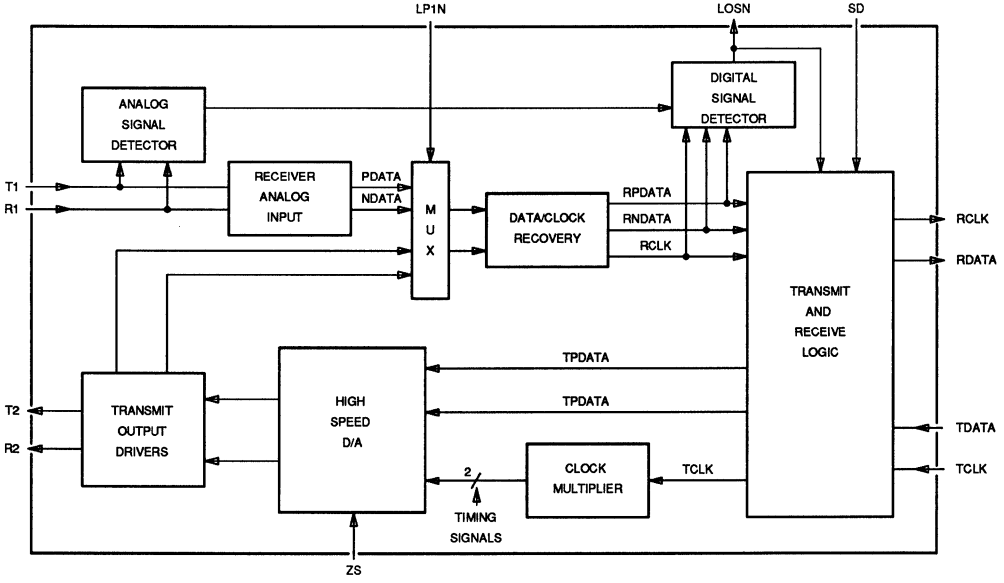


Figure 6. Analog Block Diagram

Table 2. Transmitter Specifications

Parameter	Min	Typ	Max	Unit
Output pulse amplitude:				
into 75 Ω (ZS = 0)	2.14	2.37	2.6	V
into 120 Ω (ZS = 1)	2.7	3.0	3.3	V
Pulse width (50%)	219	244	269	ns
Positive/negative pulse imbalance	—	—	± 5	%*
Zero level	—	—	10	%*
Output transformer turns ratio	1.30:1	1.37:1	1.44:1	—

* Percentage of the pulse amplitude.

Receive Converter

The receive converter accepts bipolar input signals (T1, R1), with a maximum of 6 dB loss at 1024 kHz, through the interconnecting cable. The received signal is rectified while the amplitude and rise time are restored. These input signals are peak-detected and sliced by the receiver front-end, producing the digital signals PDATA and NDATA (Figure 6). The timing is extracted by means of phase-locked loop (PLL) circuitry that locks an internal, free-running, current-controlled oscillator (ICO) to the 2.048-MHz component.

The PLL employs a 3-state phase detector and a low-voltage/temperature coefficient, current-controlled oscillator (ICO). The ICO free-running frequency is trimmed to within ± 2.5% of the data rate at wafer probe, with V_{DD} = 5.0 V and T_A = 25 °C. For all operating conditions (see the Operating Conditions section), the free-running oscillator frequency deviates from the data rate by less than ± 7%, alleviating the problem of harmonic lock.

Due to the clock output of the receive converter being derived from the ICO, a free-running clock can be present at the output of the receive converter without data being present at the input. A shutdown pin (SD) is provided to block this clock if desired, eliminating the free-running clock upon loss of the input signal.

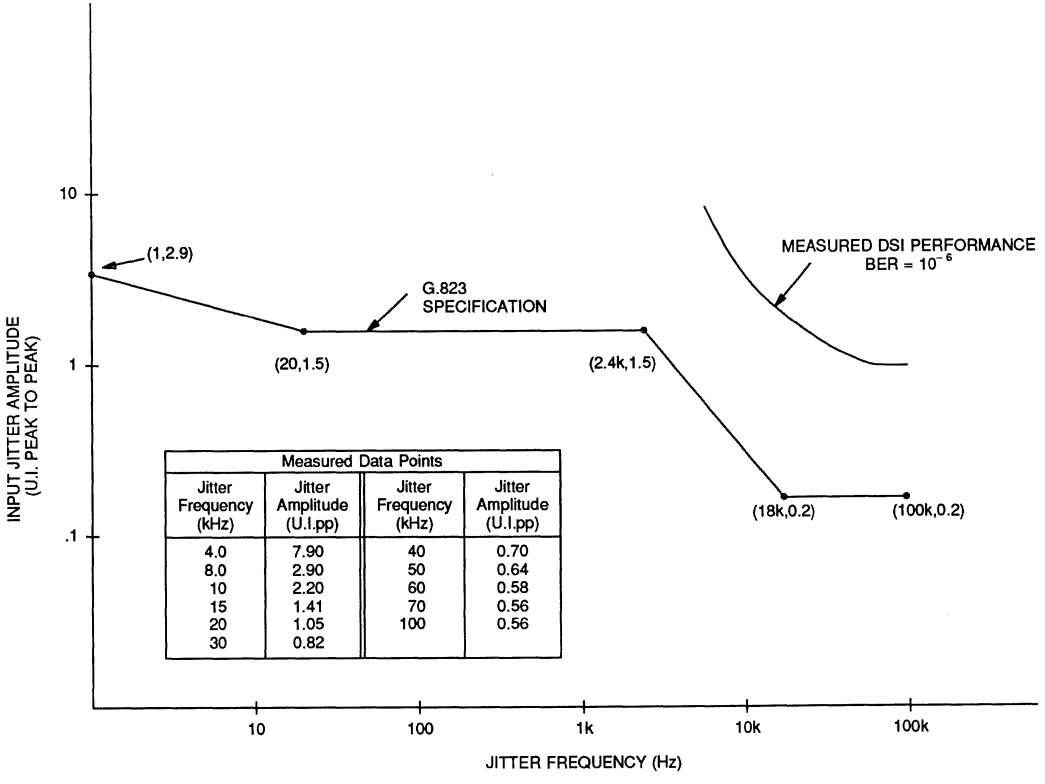
Two methods of loss-of-signal detection are used in the DSI chip. The analog signal detector shown in Figure 6 uses the output of the receiver peak detector to determine if a signal is present at T1 and R1. If the input amplitude drops below 0.5 V, the analog detector output becomes active. Hysteresis (250 mV) is provided in the analog detector to eliminate LOSN chattering. In addition, the digital signal detector counts 0s in the recovered data. If more than 32 consecutive 0s occur, the digital signal detector becomes active. In normal operation, the detector outputs are ORed together to form LOSN; however, in loopback 1, only the digital signal detector is used to monitor the looped signal. Table 3 describes the operation of the shutdown, LOSN, and LOCN functions in normal operation and in loopback 1.

The PLL is designed to accommodate large amounts of input jitter with high power supply rejection for operation in noisy environments. Low jitter sensitivity to power supply noise allows compact line card layouts employing many DSIs on one board. The minimum input jitter tolerance, as specified in CCITT specification G.823, and the measured DSI jitter tolerance is shown in Figure 7. Receiver specifications are shown in Table 4.

Table 3. Shutdown, LOSN and LOCN Truth Table*

Inputs					Outputs			
LP1N	SD	ALMTN	Input Signal at T1 R1	Loopback 1 Signal	LOSN	LOCN	Receive Side	Active LOS Detectors
1	0	1	Active	x	1	1	Normal	Analog & digital
1	0	1	No signal	x	0	1	Free-running ICO	Analog & digital
1	1	1	Active	x	1	1	Normal	Analog & digital
1	1	1	No signal	x	0	0	No output	Analog & digital
0	0	1	x	Active	1	1	Normal loopback	Digital only
0	0	1	x	No signal	0	1	Free-running ICO	Digital only
0	1	1	x	Active	1	1	Normal loopback	Digital only
0	1	1	x	No signal	0	0	No output	Digital only
x	x	0	x	x	0	0	Unaffected	x

* x = don't care.



Measured Data Points

Jitter Frequency (kHz)	Jitter Amplitude (U.I.pp)	Jitter Frequency (kHz)	Jitter Amplitude (U.I.pp)
4.0	7.90	40	0.70
8.0	2.90	50	0.64
10	2.20	60	0.58
15	1.41	70	0.56
20	1.05	100	0.56
30	0.82		

Figure 7. Random Input Data Jitter Tolerance (HDB3 Encoded)

Table 4. Receiver Specifications

Parameter	Min	Typ	Max	Unit
Receiver sensitivity (at input of device)	1.0	—	—	Vp
PLL:*				
3 dB bandwidth	—	33	—	kHz
peaking	—	1.2	—	dB
V_{DD} noise (BER = 10^{-9})**	—	>1.0	—	Vpp
ICO free-running frequency error	—	—	± 7	%
Input transformer turns ratio	1:1.9	1:2.0	1:2.1	—

* Transfer characteristics (1/8 input).
** The point of maximum sensitivity is a sine wave at 11 kHz (pseudorandom data).

Digital Logic

The logic provides alarms, optional HDB3 coding, blue signal insertion circuits, and maintenance loopbacks. It also performs dual-rail to single-rail conversion of the data.

Alarms. An independent loss-of-clock output (LOCN) is provided so that loss-of-clock is detected when the shutdown option is in effect. LOSN and LOCN can be wire-ORed to produce a single alarm.

A bipolar violation output is included if HDB3 = 0, giving an alarm each time a violation (two or more successive 1s on a rail) occurs. The violation alarm output is held in a latch for one cycle of the internal clock (RCLK). In the HDB3 mode, HDB3 code violations are detected and produce an alarm.

An alarm test pin (ALMTN) is provided to test the alarm outputs, LOSN, LOCN, and VIO. Clearing this pin forces the alarm outputs to the alarm state without affecting data transmission.

HDB3 Option. The DSI contains a HDB3 encoder and decoder that can be selected by setting the HDB3 pin. This allows the encoder to substitute a zero-substitution code for four consecutive 0s detected in the data stream, as illustrated in Table 5. A "V" represents a violation of the HDB3 code and a "B" represents a bipolar pulse of correct polarity. The decoder detects the zero-substitution code and reinserts four 0s in the data stream.

Case 1: Preceding mark has a polarity opposite the polarity of the preceding violation and is not a violation itself.

Case 2: Preceding mark has a polarity the same as the the polarity of the preceding violation or is a violation itself.

Table 5. HDB3 Substitution Code

	Case 1	Case 2
Before HDB3	0000	0000
After HDB3	000V	B00V

Blue Signal Generators. There are two blue signal generators in the device. One substitutes an all-1s blue signal on the RDATA output toward the terminal equipment. The other substitutes a bipolar all-1s blue signal for the bipolar data out of the transmit converter to keep line repeaters active.

Loopback Paths. The DSI has three independent loopback paths, which are activated by clearing the respective control inputs, LP1N, LP2N, or LP3N. Loopback 1 bridges the data stream from the transmit converter (transmit converter included) to the input of the receive converter. This maintenance loop includes most of the internal circuitry.

Loopback 2 provides a loopback of data and recovered clock from the bipolar inputs (T1, R1) to the bipolar outputs of the transmit converter (T2, R2). The receive front-end, receive PLL, and transmit driver circuitry are all exercised. This loop can be used to isolate failures between systems.

Loopback 3 loops the data stream as in loopback 1 but bypasses the transmit and receive converters. The blue signal can be transmitted when in this loopback. Loopbacks 2 and 3 can be operated simultaneously to provide transmission loops in both directions.

Characteristics

Logic Interface Electrical Characteristics

T_A = −40 to +85 °C; V_{DD} = 5 V ± 10%

Parameter	Symbol	Min	Max	Unit
Input voltage:				
low	V_{IL}	GNDD	0.8	V
high	V_{IH}	2.0	V_{DDD}	V
Output voltage:				
low	V_{OL}	GNDD	0.4	V
high	V_{OH}	2.4	V_{DDD}	V
Input capacitance	C_I	—	20	pF
Load capacitance	C_L	—	40	pF
Source current	Isource	—	80	μA
Sink current	Isink	—	2.0	mA

Internal pull-up resistors are provided on the following input leads: LP1N, LP2N, LP3N, and ALMTN. Internal pull-down devices are provided on the following leads: SD, RBC, HDB3, TBC, and ZS. The internal pull-up or pull-down devices require the input to source or sink to be no more than 20 μA.

Operating Conditions

− 40 °C ≤ T_A ≤ +85 °C, except as noted

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Power dissipation:*					
75 Ω (ZS = 0)	PD	—	78	89	mW
120 Ω (ZS = 1)	PD	—	75	86	mW

* Measurement conditions with 50% 1s in both transmit and receive paths, T_A = 25 °C, V_{DD} = 5 V.

Maximum Ratings

DC supply voltage (V_{DD}) range ..... –0.5 to +6.5 V
Power dissipation (PD) ..... 1 W
Storage temperature (Tstg) range ..... –65 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

Timing Characteristics

All duty cycle and timing relationships are referenced to a TTL 1.4 V threshold level.

Loss-of-Clock Indication Timing. The clock leaving must be absent 3.91 μs to guarantee a loss-of-clock indication. It is possible to produce a loss-of-clock indication if the clock is absent for 1.95 μs, depending on the timing relationship of the interruption with respect to the timing cycle.

The clock returning must be present 3.91 μs to guarantee a normal condition on the loss-of-clock pin (LOCN). The loss-of-clock indication can return to normal immediately, depending on the timing relationship of the signal return with respect to the timing cycle.

Symbol	Description	Min	Typ	Max	Unit
tTCLTCL	TCLK clock period	*	488	*	ns
tTCHTCL	TCLK duty cycle	40	50	60	%
tTDVTCL	Data set-up time, TDATA to TCLCK	50	—	—	ns
tTCLTDV	Data hold time, TCLK to TDATA	40	—	—	ns
tr	Clock rise time (10%—90%)	—	—	40	ns
tf	Clock fall time (10%—90%)	—	—	40	ns
tRCHRDV	Data hold time, RCLK to RDATA, VIO	171	—	—	ns
tRDVRCH	Data set-up time, RDATA, VIO to RCLK	131	—	—	ns
tRCLRDV	Propagation delay, RCLK to RDATA	—	—	40	ns

* A tolerance of ± 50 ppm.

Timing Diagrams

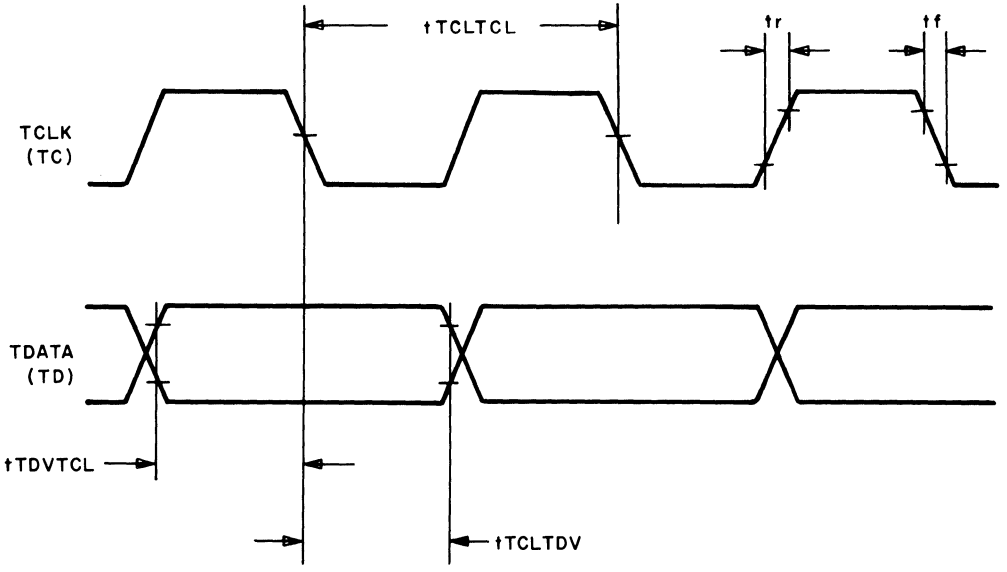


Figure 8a. Timing Diagram

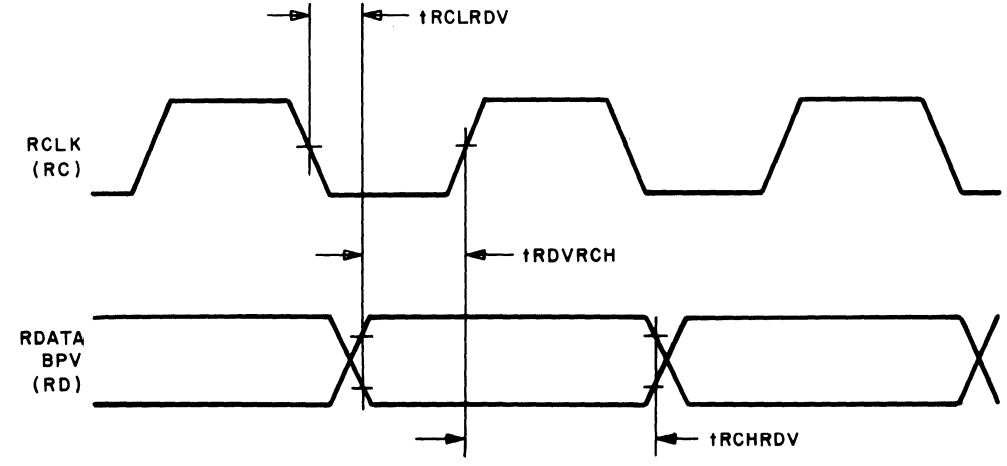


Figure 8b. Timing Diagram

T7229 Primary Access Framer

Features

- Multiple line format capability
  - AMI and HDB3 (CEPT)
  - Bipolar and B8ZS
- Multiple DS1 TDM frame formats
  - Independent formats – D4, *SLC* Carrier, ESF, and DDS T1DM (DS1
  - CCITT 30-channel format with optional TS-16 signaling (CEPT)
- Off-line, defensive, and fast frame synchronization
- *SLC* Carrier, ESF, and DDS T1DM facility data link insertion and extraction
- Remote frame/multiframe alarm activation and detection
- AIS detection
- Transmission performance monitoring capability:
  - Bipolar, B8ZS, AMI, and HDB3 violations
  - Frame alignment signal (frame bit) errors
  - Loss-of-frame/loss-of-multiframe alignment
  - CRC-6 errors (ESF mode)
  - Change-of-frame alignment

Description

The T7229 Framer integrated circuit provides the line format and frame format interfaces for DS1 (1.544 Mb/s) and CEPT (2.048 Mb/s) digital carrier systems. It performs in-line and off-line frame-oriented functions in both the receive and transmit directions. The T7229 Framer is TTL-compatible and is manufactured using CMOS technology. It is available in a 40-pin plastic DIP and a 44-pin plastic leaded chip carrier (PLCC) for surface mounting.

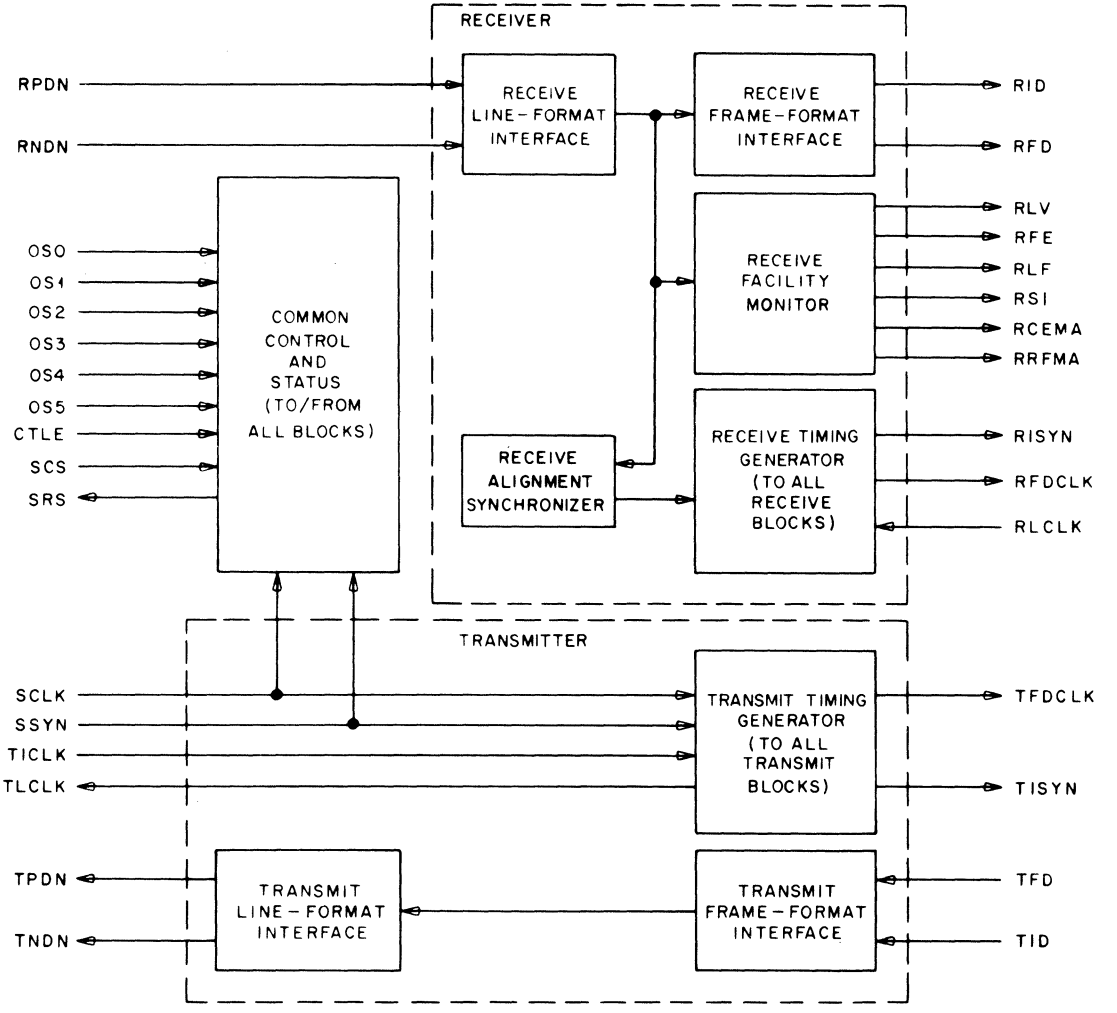


Figure 1. Block Diagram

User Information

Pin Descriptions

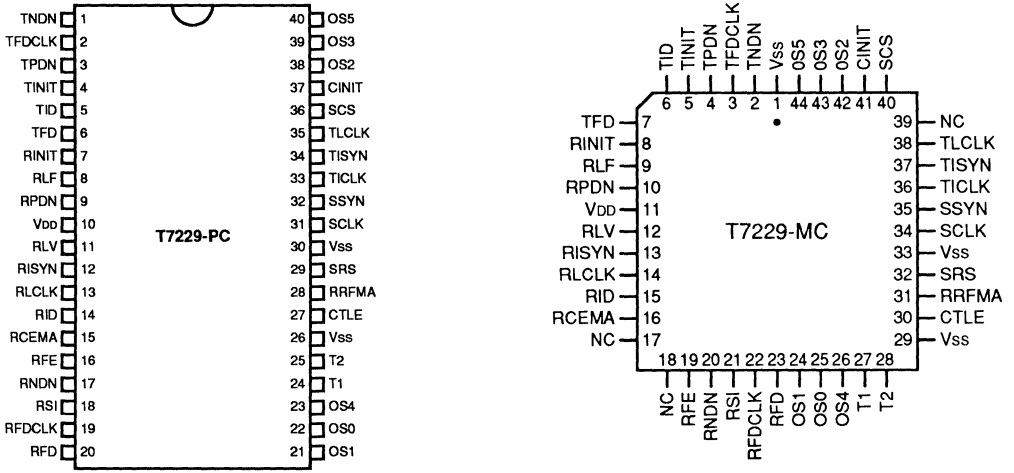


Figure 2. 40-Pin Plastic DIP and 44-Pin PLCC Pin Function Diagrams

Table 1. Pin Descriptions

Pin (DIP)	Pin (PLCC)	Symbol	Type	Name/Function
—	1	VSS	—	**Ground.**
1	2	TNDN	O	**Transmit Negative-Rail Data Inverted.** 1.544-Mb/s (DS1) or 2.048-Mb/s (CEPT) dual-rail pseudoternary (bipolar, B8ZS, AMI, or HDB3) TDM data.
2	3	TFDCLK	O	**Transmit Facility Data Link Clock.** Reference clock for transmit facility data link data on pin 6. In DDS mode, this is an 8-kHz clock signal; in *SLC* Carrier, ESF, and IRSM modes, this is a 4-kHz clock signal.
3	4	TPDN	O	**Transmit Positive-Rail Data Inverted.** 1.544-Mb/s (DS1) or 2.048-Mb/s (CEPT) dual-rail pseudoternary (bipolar, B8ZS, AMI, or HDB3) TDM data.
4	5	TINIT	I	**Transmit Initialization.** Manufacturing test pin. Ground this pin for normal operation. Setting (1) TINIT, RINIT, and CINIT puts all transmit output pins in a high-impedance, 3-state mode.
5	6	TID	I	**Transmit Interdevice Data.** 1.544-Mb/s (DS1) or 2.048-Mb/s (CEPT) unipolar TDM source data.
6	7	TFD	I	**Transmit Facility Data Link Data.** 8-kb/s data in the DDS mode. 4-kb/s data in the *SLC* Carrier, ESF, and IRSM modes. Data link source data is strobed in by negative transitions of TFDCLK.

Table 1. Pin Descriptions (Continued)

Pin (DIP)	Pin (PLCC)	Symbol	Type	Name/Function
7	8	RINIT	I	**Receive Initialization.** Manufacturing test pin. Ground this pin for normal operation. Setting TINIT, RINIT, and CINIT puts all receive section output pins in a high-impedance, 3-state mode.
8	9	RLF	O	**Receive Loss-of-Frame Alignment.** This pin is set upon loss-of-frame and/or loss-of-multiframe alignment.
9	10	RPDN	I	**Receive Positive-Rail Data Inverted.** 1.544-Mb/s (DS1) or 2.048-Mb/s (CEPT) dual-rail pseudoternary (bipolar, B8ZS, AMI, or HDB3) TDM data. Tie RPDN and RNDN together for unipolar TDM received data.
10	11	V_{DD}	—	**5 V Supply.**
11	12	RLV	O	**Receive Line Format Violations.** This pin is set for each receive line format violation.
12	13	RISYN	O	**Receive Interdevice Synchronization.** A 648-ns (DS1 mode) or 488-ns (CEPT mode) pulse repeated at 3-ms intervals in DS1 mode; 2-ms intervals in CEPT mode. Transitions of RISYN occur on negative transitions of RLCLK.
13	14	RLCLK	I	**Receive Line Clock.** 1.544-MHz (DS1) or 2.048-MHz (CEPT) clock signal.
14	15	RID	O	**Receive Interdevice Data.** 1.544-Mb/s (DS1) or 2.048-Mb/s (CEPT) unipolar TDM output data. Transitions of RID occur on negative transitions of RLCLK.
15	16	RCEMA	O	**Receive CRC-6 Errors/Loss-of-Multiframe Alignment.** This pin is set upon a received cyclic redundancy check error in DS1 ESF mode, or loss-of-multiframe alignment in CEPT mode.
—	17	NC	—	**No Connection.**
—	18	NC	—	**No Connection.**
16	19	RFE	O	**Receive Frame Alignment Signal Error.** This pin is set upon detection of frame alignment signal (frame bit) error.
17	20	RNDN	I	**Receive Negative-Rail Data Inverted.** 1.544-Mb/s (DS1) or 2.048-Mb/s (CEPT) dual-rail pseudoternary (bipolar, B8ZS, AMI, or HDB3) TDM data.
18	21	RSI	O	**Receive Signaling Inhibit.** This pin is set by a framing error, loss-of-frame alignment or loss-of-multiframe alignment.
19	22	RFDCLK	O	**Receive Facility Data Link Clock.** Reference clock for receive facility data link data on RFD. In DDS mode, this is an 8-kHz clock signal; in *SLC* Carrier, ESF, and IRSM modes, this is a 4-kHz clock signal.
20	23	RFD	O	**Receive Facility Data Link Data.** 8-kb/s data in DDS mode; 4-kb/s data in *SLC* Carrier, ESF, and IRSM modes.
21 22 23	24 25 26	OS1 OS0 OS4	I	**Option Selects 1, 0, and 4.** Option selection pins. Option can also be selected by using the serial control stream (SCS).

Table 1. Pin Descriptions (Continued)

Pin (DIP)	Pin (PLCC)	Symbol	Type	Name/Function
24	27	T1	I	**Test 1.** For manufacturing purposes only. Must be grounded for normal operation.
25	28	T2	I	**Test 2.** For manufacturing purposes only. Must be grounded for normal operation.
26	29	Vss	—	**Ground.**
27	30	CTLE	I	**Control Enable.** Control lead to enable loading of serial control stream (SCS).
28	31	RRFMA	O	**Receive Remote Frame and Multiframe Alarm.** This pin is set upon a received remote frame alarm and cleared otherwise.
29	32	SRS	O	**Serial Report Stream.** The serial report stream is output at a 1-Mb/s bit rate. SRS contains one byte for facility reports, one byte for device alarms, and four bytes for auditing the option, exercise, action, and action-mask control fields. Each of these six bytes is repeated twice per frame; the remaining four bytes are padded with 0s. Facility and alarm bytes are updated once a frame; the remaining four control bytes are updated twice a frame.
30	33	Vss	—	**Ground.**
31	34	SCLK	I	**System Clock.** 4.096-MHz system clock.
32	35	SSYN	I	**System Synchronization.** 8-kHz system synchronization pulse of 244-ns duration. SSYN is strobed on positive transitions of both SCLK and TICLK.
33	36	TICLK	I	**Transmit Interdevice Clock.** 1.544-MHz (DS1 mode) or 2.048-MHz (CEPT mode).
34	37	TISYN	O	**Transmit Interdevice Synchronization.** This pin, which establishes frame alignment, is a bit interval pulse set every 3 ms in DS1 mode and every 2 ms in the CEPT mode.
35	38	TLCLK	O	**Transmit Line Clock.** 1.544-MHz (DS1 mode) or 2.048-MHz (CEPT mode).
—	39	NC	—	**No Connection.**
36	40	SCS	I	**Serial Control Stream.** SCS accepts 8-bit control bytes at a 1-Mb/s rate. Control bytes determine options, consequent actions (channel squelch, FDL squelch remote-alarm insertion, etc.), action masks, and maintenance exercises. A control byte is shifted in on SCS while CTLE is set.
37	41	CINIT	I	**Control Initialization.** Manufacturing test pin. Ground this pin for normal operation. Setting TINIT, RINIT, and CINIT puts all control and report pins in a high-impedance, 3-state mode.
38 39 40	42 43 44	OS2 OS3 OS5	I	**Option Selects 2, 3, and 5.** Option selection pin. Options can also be selected by using the serial control stream (SCS).

Overview

The T7229 Framer is part of an LSI DS1 chip set that also includes the 257AU Receive Synchronizer, the 257AL Transmit Formatter, and the 229FB Maintenance Buffer. The framer performs in-line data processing, off-line terminal frame and signaling frame synchronization, transmission facility monitoring, and system fault monitoring.

The functional operation of the T7229 Framer is discussed in terms of Figure 1. The circuit is divided into three main blocks: transmitter, receiver, and common control and status. The transmitter and receiver process information signals passing through the device in the transmit and receive directions, respectively; the common control and status block is the control and status interface for the device.

Transmitter

The transmit section of the T7229 Framer consists of the transmit timing generator (TTG), transmit frame format interface (TFFI), and transmit line format interface (TLFI). The TFFI accepts a unipolar, time-division multiplex (TDM) signal on TID and a unipolar facility data link bit stream on TFD. TID is clocked either by a 1.544-MHz (DS1 mode) or 2.048-MHz (CEPT mode) timing signal input on TICLK, and must be synchronized to the 3-ms (DS1 mode) or 2-ms (CEPT mode) interval pulse output on TISYN. The FDL bit stream on TFD must be clocked by the 4-kHz or 8-kHz timing signal output on TFDCLK.

The TDM signal on TID must be formatted with customer data and signaling already in place in the channel time slots, but with a pseudorandom maintenance pattern in the framing bit (F-bit) positions in the DS1 mode and in TS0 in the CEPT mode. According to the selected DS1 mode, the TFFI overwrites the F bits with the terminal framing (Ft or Fe) or signaling framing (Fs) pattern, the CRC-6 check bits, and/or the FDL bit stream. The TFFI also inserts the remote-frame (yellow) alarm (RFA) in the FDL bit positions in the extended superframe (ESF) mode and generates the CRC-6 check bits. In the CEPT mode, the TFFI overwrites TS0 with the FAS pattern and the RFA bit and, when requested, sets the I and N bits. It can also set the TS16 RMA bit and X bits.

In general, the TFFI is transparent to the channel time slots. When requested, however, it can overwrite the words as follows:

- D4 RFA, zero-code suppression (ZCS) and maintenance squelch patterns in all words.
- DDS frame alignment pattern, FDL bits and RFA in word-24.

The TLFI converts the unipolar TDM signal from the TFFI to a dual-rail bipolar signal and, in the B8ZS or HDB3 mode, replaces strings of 0s with the B8ZS or HDB3 violation codes. The resulting dual-rail TDM signal is output on TPDN and TNDN.

The TTG generates TISYN in fixed relation to a 125-μs interval system sync pulse input on SSYN. It also generates TFDCLK, a 1.544-MHz (DS1 mode) or 2.048-MHz (CEPT mode) timing signal output on TLCLK, and all internal synchronization signals. Finally, in the *SLC* Carrier mode (SL mode), it synchronizes to the Fs pattern that must be embedded in the FDL bit stream on TFD.

Receiver

The receive section of the T7229 Framer comprises the receive timing generator (RTG), the receive frame format interface (RFFI), the receive line format interface (RLFI), the receive alignment synchronizer (RAS), and the receive facility monitor (RFM). The RFFI accepts a dual-rail TDM signal on RPDN and RNDN. These inputs are clocked by a 1.544-MHz (DS1 mode) or 2.048-MHz (CEPT mode) timing signal input on RLCLK. The TDM signal is converted to unipolar and, in the B8ZS or HDB3 mode, instances of the B8ZS or HDB3 violation code are replaced by strings of 0s. The RLFI detects violations of the bipolar, B8ZS, or HDB3 codes and reports them to the RFM. The TDM output signal is distributed among the RFFI, the RAS, and the RFM sections.

The RFFI first extracts the FDL bit stream from the F bits in the TDM signal and then overwrites the F bits of DS1 or bit 3 of TS0 with the pseudorandom pattern (PRP). In general, the RFFI is transparent to the channel time slots. When requested or authorized, however, it can overwrite all words with a

maintenance squelch pattern. In the DDS mode, facility error information from the RFM section is autonomously inserted in the RFA bit position of word-24. The RFFI outputs the processed unipolar TDM signal on RID and the extracted FDL bit stream on RFD. RID is clocked by the 1.544-MHz (DS1 mode) or 2.048-MHz (CEPT mode) receive line clock (RLCLK) and is synchronized to the 3-ms (DS1 mode) or 2-ms (CEPT mode) interval pulse output on RISYN. The FDL bit stream on RFD is clocked by the 4-kHz or 8-kHz timing signal output on RFDCLK.

The RFM section monitors the TDM signal for facility trouble conditions and alarms. Detected trouble conditions and alarms are forwarded to the common control and status block and to dedicated status output leads (RLV, RFE, RLF, RCEMA, RRFMA, and RSI). Detected loss-of-alignment conditions are reported to the RAS section.

The RAS section establishes terminal frame alignment in all modes, superframe alignment in the D4, SL, and ESF modes, and multiframe alignment in the CEPT mode. It operates in a fast, off-line, defensive mode for terminal frame synchronization; the search for the frame alignment pattern and/or sequence (FAS) covers all possible alignment phases simultaneously. When a single candidate FAS is found, alignment is adjusted to the phase of that FAS. To avoid synchronization to a random data pattern, the search cannot be satisfied until at least 24 bits of the candidate FAS have been examined. The search does not affect the operation of the other sections of the receiver until the decision is made that a new frame alignment is required. Consequently, an error burst does not force a loss of alignment.

To avoid alignment to a fixed data or signaling pattern that emulates the FAS, the RAS does not adjust alignment to a new phase if more than one candidate FAS is present. When static emulators last for more than 100 ms in the ESF mode, the synchronizer aligns successively to each candidate FAS (at 200 ms per candidate) until an alignment with the correct CRC-6 pattern is found. This on-line trial-and-error mode is not possible in the D4, DDS, SL, and CEPT modes.

The RTG generates RISYN in fixed relation to the TDM signal output on RID, RFDCLK in fixed relation to the FDL bit stream output on RFD, and all internal synchronization signals.

Common Control and Status

The principle control access to the T7229 Framer is the 1.024-Mb/s serial control stream input on SCS. The SCS is used for provisioning, maintenance exercises, and requests for the application of squelch patterns and remote alarms. It is enabled by the control stream enable input on CTLE. The mode of the device can also be controlled via the external option input leads, OS0—OS5.

The 1.024-Mb/s serial report stream, output on SRS, carries reports from the RFM section, reports from fault-monitoring circuits distributed throughout the device, and audits of the current control state.

The SCS and SRS are clocked at the 1.024-Mb/s rate by a submultiple of the 4.096-MHz timing signal input on SCLK. The bit boundaries in both the SCS and the SRS and the byte and block boundaries in the SRS are synchronized to the system sync pulse input on SSYN.

Functional Description

Line Format Processing

The transmitter line format interface processing converts the frame-formatted TDM bit stream into a dual-rail bipolar signal or a modified bipolar output signal (B8ZS or HDB3). In the bipolar and AMI modes, binary 1s in the TDM bit stream become pulses of alternating polarity transmitted between the two output rails, TPDN and TNDN; binary 0s are transmitted as null pulses. Note that the outputs are active-low (i.e., a pulse corresponds to a binary 0 and no pulse corresponds to a binary 1). In the B8ZS and HDB3 modes, the bipolar algorithm is modified to guarantee at least 1 pulse for every 8 transmitted bits by substituting a bipolar violation code (BPV) for blocks of 8 or 4 successive 0s, as illustrated in Tables 2 and 3. The transmitter generates BPVs by sending the BPV pulse to the same output rail as the last preceding bipolar pulse.

Table 2. B8ZS Substitution Code

Before B8ZS	0 0 0 0 0 0 0 0
After B8ZS	0 0 0 V B 0 V B

Table 3. HDB3 Substitution Code

Before HDB3	0 0 0 0
After HDB3	X 0 0 V

The receiver line format interface processing is complementary to the transmitter processing. Input pulses on RPDN and RNDN, also active-low, become binary 1s on the TDM output bit stream; missing pulses become binary 0s. In the B8ZS and HDB3 modes, the processing circuit recognizes valid violation codes and replaces them with the correct number of binary 0s.

Frame Format Processing

Frame format refers to the organization of information as it is time-division multiplexed within the transmitted signal. The common elements in DS1 and CEPT frame format structures are the 8-bit word or time slot and the 125-μs frame.

In the DS1 structure, a frame contains 24 words (192 bits) preceded by one framing bit. A superframe contains 12 frames and an extended superframe 24, as illustrated in Figure 3. When robbed-bit signaling is used, the superframes identify frames 6, 12, 18 and 24, which contain signaling information. The T7229 Framer supports four DS1 TDM frame formats: D4 channel bank (D4), *SLC* 96 Carrier System (SL), extended superframe (ESF), and digital data system (DDS) T1 digital multiplexer (T1DM).

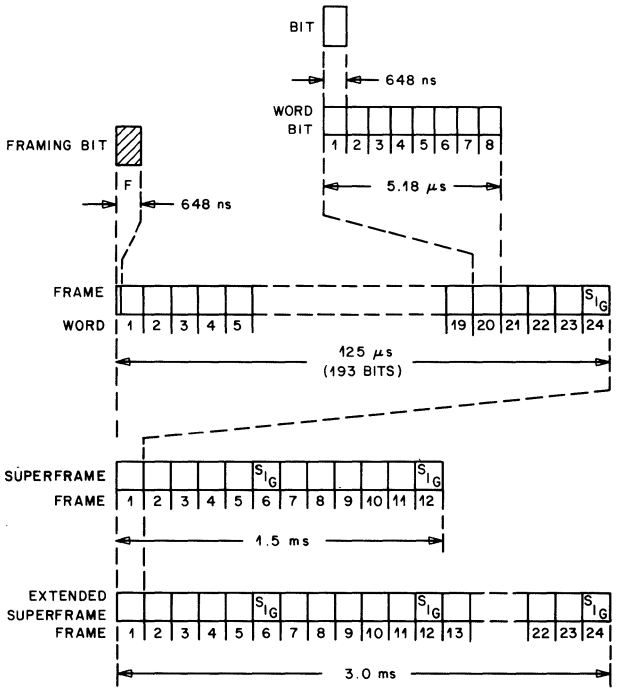


Figure 3. Domestic Frame Format Structure

In the CEPT structure, a frame consists of 32 time slots (256 bits). In each frame, time slot 0 (TS0) is reserved for frame alignment and control information, while time slot 16 (TS16) can be used for per-channel signaling (PCS) information. In the latter case, TS16 is formatted in a 16-frame multiframe. Figure 4 illustrates the basic CEPT frame format structure. The T7229 Framer supports the common-channel signaling (CCS) mode, the per-channel signaling phase 0 (PCS0) and phase 1 (PCS1) modes, and the CEPT remote-switching module (IRSM) mode. The CCS mode is used when TS16 does not contain a PCS channel; otherwise, the PCS0 and PCS1 modes are used. Phase 0 means that the transmitter aligns the TS16 multiframe alignment signal (MAS) word with the TS0 frame alignment signal (FAS) word. In the PCS1 mode, the transmitter aligns the MAS word with the TS0 not-word.

Table 4 lists the DS1 TDM formats and Table 5 the CEPT TDM formats supported by the T7229 Framer.

There are two levels of frame format interface processing: data level and frame level. Data level processing overwrites bits in specified data words and time slots or the facility data link (FDL) with new information. Frame level processing affects the framing bits, word-24 in the DDS mode, and TS0 in the CEPT modes.

Table 4. DS1 TDM Frame Formats

DS1 TDM Format	Symbol	Signaling-Bit Identification
D4 channel bank	D4	12-frame superframe
SLC 96 Carrier	SL	12-frame superframe
Extended superframe	ESF	24-frame superframe
DDS T1DM	DDS	No signaling

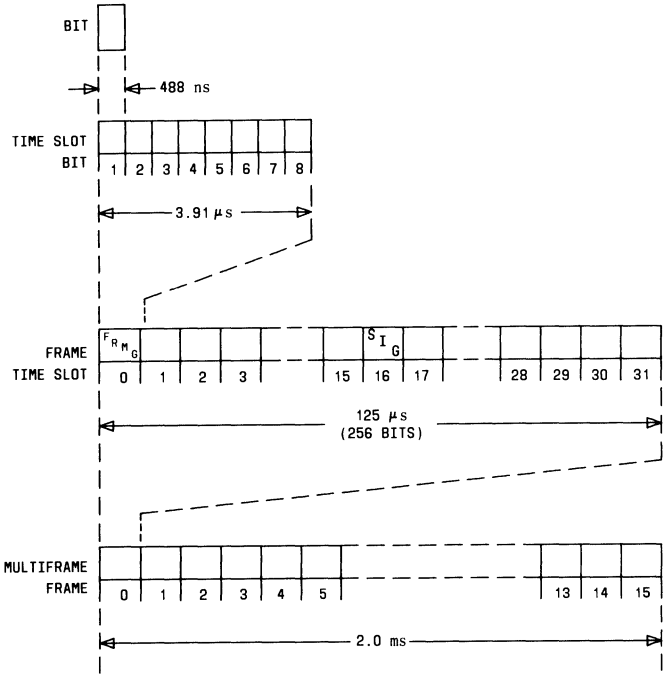


Figure 4. CEPT Frame Format Structure

Table 5. CEPT Frame Formats

CEPT TDM Format	Designated Symbol	Signaling-Bit Identification
Common-channel signaling	CCS	No signaling
Per-channel signaling	PCS0, PCS1	16-frame multiframe
CEPT RSM	IRSM	16-frame multiframe

Data Level Processing. The T7229 Framer operation is transparent to message channels and to embedded or formatted signaling bits. However, it has the capability to overwrite certain bits in channel words. The majority of this type of processing is for consequent actions, i.e., inserting remote alarms or squelching the data with specific bit patterns in response to detected trouble conditions. Consequent action capabilities are discussed in the Responses to Facility Trouble and Alarms section.

An additional data level processing capability is DS1 zero-code suppression (ZCS), which can be implemented when the 1s density requirements are not met transparently (e.g., with B8ZS). ZCS consists of setting bit 7 in any word to be transmitted that contains all 0s. The T7229 Framer must apply ZCS or squelch patterns to all words simultaneously. Table 6 defines the specific ZCS and maintenance patterns.

Table 6. Domestic ZCS and Maintenance (Squelch) Patterns

Words 1—24	Format	Location	B1	B2	B3	B4	B5	B6	B7	B8
ZCS	DS1 non-DDS	XMTR	0	0	0	0	0	0	1	0
Idle code	DS1 non-DDS	XMTR	0	1	1	1	1	1	1	1
UC code	DDS	XMTR	0	0	0	1	1	0	0	0
MOS code	DDS	RCVR	0	0	0	1	1	0	1	0
AIS code	Non-DDS	RCVR	1	1	1	1	1	1	1	1

The transmitter also generates two types of remote alarms: remote frame alarm (RFA), i.e., yellow alarm, and remote multiframe alarm (RMA). Table 7 defines the remote alarms.

Table 7. Remote Alarms

Alarm	Format	Definition
RFA	D4	Bit 2 of all words in each frame cleared
	DDS	Bit 6 of word-24 in each frame cleared
	SL	Not processed by the T7229
	ESF	An alternating pattern of eight 1s and eights 0s on the FDL
RMA	CEPT	Bit 6 of TS16 MAS word set

Squelch patterns and remote alarms can be turned on by explicit external order or can be enabled for automatic activation; ZCS is activated only by external order. In cases where simultaneous squelch and remote alarm patterns affect the same bit, the remote alarm takes precedence. The B8ZS option overrides the ZCS option.

Patterns inserted by the transmitter appear in the dual-rail bipolar output signal; patterns inserted by the receiver appear on the RID and RFD leads.

Frame Level Processing. Frame level processing affects the framing bits, the DDS word-24 pattern and the CEPT FAS word, MAS word, and not-word. A pseudorandom pattern (PRP) is embedded for maintenance purposes in the input data on TID and the output data on RID in all modes. In the DS1 mode, the pattern repeats in the framing bit positions at 24-frame intervals; in the CEPT mode, it repeats in bit 3 of TS0 at 16-frame intervals. The CEPT pattern is a truncated version of the DS1 pattern.

At the dual-rail bipolar inputs and outputs, the DS1 framing bit positions contain the standard framing, data link, and CRC bits defined in Table 8. Additional DS1 framing information is contained in word-24 in the DDS mode (Table 11). TS0 in the CEPT mode contains the FAS, RFA, and control bits, as shown in Table 9.

The transmitter has several functions in frame level processing. In the DS1 mode, it checks the PRP in the TDM input for errors and the superframe F-bit (Fs) sequence in the *SLC* Carrier FDL input for errors. It generates the Ft and Fs or Fe bits in the D4, DDS, and ESF modes, and generates the Ft pattern and synchronizes to the Fs pattern on the FDL input in the SL mode. The transmitter generates and inserts the ESF CRC-6 check bits as required and copies the *SLC* Carrier and ESF FDL input data to the FDL bits.

The receiver synchronizes to the Ft and Fs or Fe bits and then checks the Ft, Fs or Fe, and CRC-6 check bits for errors. The *SLC* Carrier and ESF FDL bits are copied to the FDL output. The receiver inserts the PRP in the TDM output. Table 8 summarizes the assignment of DS1 framing bits.

In CEPT modes, the transmitter inserts the FAS pattern in the TS0 FAS word, inserts the spoiler bit (bit 2 = 1) in the TS0 not-word, manages the I and N control bits in TS0, and manages the X control bits in TS16 (when used). The receiver overwrites bit 3 of TS0 with the PRP and manages the X control bits in TS16 (when used).

Table 8. DS1 Framing Bit Assignments

DDS, D4, SL			ESF			
FRs	**Ft**	**Fs or FDL***	**FRe**	**FDL***	**CRC**	**Fe**
1	1		1	D		
2		0 or D	2		C1	
3	0		3	D		
4		0 or D	4			0
5	1		5	D		
6		1 or D	6		C2	
7	0		7	D		
8		1 or D	8			0
9	1		9	D		
10		1 or D	10		C3	
11	0		11	D		
12		0 or D	12			1

* D = FL input data.

Table 8. DS1 Framing Bit Assignments (Continued)

DDS, D4, SL			ESF			
FRs	Ft	Fs or FDL*	FRe	FDL*	CRC	Fe
1	1		13	D		
2		0 or D	14		C4	
3	0		15	D		
4		0 or D	16			0
5	1		17	D		
6		1 or D	18		C5	
7	0		19	D		
8		1 or D	20			1
9	1		21	D		
10		1 or D	22		C6	
11	0		23	D		
12		0 or D	24			1

* D = FDL input data.

Table 9. CEPT TS0 Bit Assignments

FAS word	I	0	0	1	1	0	1	1
Not-word	I	RFA	1	N0	N1	N2	N3	N4

The T7229 Framer provides two options for handling the I, N, and X control bits: transparent and nontransparent. In the nontransparent mode, the transmitter sets all control bits to binary 1s and the receiver ignores all control bits. In the transparent mode, the transmitter receives all control bits in TS0 on TID and the receiver returns all control bits in TS0 on RID. In the PCS mode, the transmitter transfers the X control bits from TS0 to TS16 and the receiver does the reverse transfer. To distinguish the FAS word from the not-word, the transmitter synchronizes to the alternating 0 and 1 pattern in bit 2 of TS0.

Table 10 shows the combined format of TS0 as it appears on TID and RID. The dashes indicate bits that are irrelevant to the transmitter and receiver. Note that the X bits are updated at 2-ms intervals (every multiframe).

Table 10. Internal Time-Slot-0 Format (Control-Bit Transparency)

FAS word	I	0	—	—	—	X0	X1
Not-word	I	1	—	N0	N1	N2	N3

The IRSM mode is a hybrid: the nontransparent mode is used for the I and X control bits, control bits N1 through N4 are treated transparently, and control bit N0 is used for the FDL.

Table 11 summarizes word-24 processing in the DDS mode. The transmitter sets the frame alignment signal (FAS) to the correct pattern. It sets the remote frame alarm (RFA) bit for "no alarm" or clears the RFA bit for "alarm". The transmitter copies the FDL input data to the FDL bits in the DDS FDL mode and the receiver routes the FDL bit to the FDL output. The receiver synchronizes to the FAS pattern while checking the FAS bits for errors. It checks the RFA bit for an alarm condition and overwrites the RFA bit with the logical OR of the current framing error and loss-of-frame alignment status.

Table 11. Word-24 Bits Processed in the DDS Mode

Word 24	B1	B2	B3	B4	B5	B6	B7	B8
FAS	1	0	1	1	1	—	—	0
RFA	—	—	—	—	—	0/1	—	—
FDL	—	—	—	—	—	—	D	—

Alignment and Synchronization

The T7229 Framer uses bit sequences and bit patterns to establish alignment in the received and transmitted signals. Bit sequences are composed of individual bits spaced at frame or multiple-frame intervals. Bit patterns are multiple bits in a single frame. Table 12 contains the bit sequences and patterns used to establish alignment.

The terminal frame (Ft) and superframe (Fs) sequences alternate in the F-bit positions. The SL Fs bits occur in only two out of every six superframes. Frame and superframe alignment is established simultaneously by the ESF Fe bits. The DDS and CEPT frame alignment signals (FAS) provide fast frame synchronization.

Table 12. Bit Sequences and Patterns Used to Establish Alignment

Name	Format	Location	Pattern	Alignment
Ft bits	Non-ESF	Every 2nd F bit	01	Frame
Fs bits	D4 & SL	Every 2nd F bit	001110	Superframe
Fe bits	ESF	Every 4th F bit	001011	Frame, superframe
FAS	DDS	Every word-24 (bits 1—5, 8)	101110	Frame
PRP	All DS1	Every F bit (bits 2 to 8)	0xF8DD42	Interdevice
FAS	CEPT	Every FAS word	0011011	Frame
FAS	CEPT	Every not-word (bit 2)	1	Frame
PRP	CEPT	Every TS0 (bit 3)	0xF8DD	Interdevice

Interdevice Synchronization

The T7229 Framer internal timing generators provide external 24-frame syncs (TISYN and RISYN) for interdevice synchronization. These syncs define the phase of the TDM signals on TID and RID, respectively. Normally, the transmitter is locked in frame synchronization to the input system sync pulse (SSYN), but has arbitrary superframe or multiframe phase. In the SL mode, however, the transmitter is forced to synchronize to the transmit FDL input on TFD because this data stream has the Fs-alignment sequence embedded in it. The receive interdevice sync is locked to the frame and superframe/multiframe phase determined by the receive alignment synchronizer.

Interdevice synchronizations identify frame and superframe alignment and define the phase of the interdevice PRP embedded in the framing bit positions. The relationship of the PRP to the DS1 frame and superframe patterns is shown in Table 13.

Table 13. DS1 Interdevice Alignment

Bit	Bit Sequence*
Ft	1x0x1x0x1x0x1x0x1x0x1x0x
Fs	x0x0x1x1x1x0x0x0x1x1x1x0
Fe	xxx0xxx0xxx1xxx0xxx1xxx1
Fm	xxxxxxxxxxxxxxxxxxxxxxxx
PRP	111110001101110101000010

* x = don't care.

Link Synchronization

When a loss-of-frame alignment (LFA) condition is detected by the receiver, the alignment synchronizer activates but the normal receiver functions continue to operate at the previously determined frame alignment. After the synchronization circuit determines that a new alignment is required, the receiver circuits are forced to that new alignment. The defensive mode of the synchronization circuit inhibits realignment when repetitive data patterns emulate the FAS pattern.

In the ESF mode only, an on-line search procedure starts when an emulator has inhibited synchronization for 100 ms. The synchronization circuit selects one of the multiple candidate positions and checks for a correct CRC-6 pattern at this time. If the CRC-6 pattern does not match, the next candidate position is tried. The procedure repeats until the correct position is found. Each CRC-6 check takes 100 ms and each synchronization attempt takes an additional 100 ms.

When there are no emulators, the internal memory needed to implement the defensive algorithm leads to very fast synchronization; however, to avoid false reframes, the search does not end until at least 24 FAS-bit positions have been examined.

In the DS1, D4, and SL modes and in the CEPT PCS modes, signaling frame synchronization is performed off-line, but no special defensive or fast algorithms are used. The D4/SL synchronization uses the standard D4 algorithm, while the PCS synchronization conforms to CCITT standards. Signaling frame synchronization is not required in the DDS mode. It is accomplished concurrently with terminal frame synchronization in the ESF mode, by a separate Fs resynchronizer in the D4 and SL modes, and by a separate multiframe resynchronizer in the CEPT modes.

Tables 14—17 summarize the mean times and criteria for loss and recovery of alignment. Recovery time calculations assume no line error. True loss-of-alignment time calculations assume a 0.5 error rate; false loss-of-alignment time conditions assume a 10^{-3} error rate. See Tables 18 and 19 for definitions of FER, CER, LFA, and LMA.

Table 14. Mean Recovery-of-Alignment Time

Alignment	Format	Mean Time*
Frame	DDS	0.75 ms
	D4 & SL	6 ms
	CEPT	1 ms
Superframe	D4-Ft/Fs	4.5 ms
	SL	21 ms
Frame/superframe	ESF	12 ms
Multiframe	CEPT	2 ms

* Assumes no line errors and no emulators.

Table 15. Recovery-of-Alignment Criteria

Alignment	Format	Recovery Indication	Recovery Criterion
Frame	DDS	LFA off	The first unique correct combination of an Ft/Fs sequence and FAS pattern that exists for at least 6 consecutive frames
	D4-Ft	LFA off	The first unique correct Ft sequence that exists for at least 24 consecutive Ft intervals (48 frames)
	D4-Ft/Fs & SL	None	The first unique correct Ft sequence that exists for at least 24 consecutive Ft intervals (48 frames)
	ESF	LFA off	The first unique correct Fe sequence that exists for at least 24 consecutive Fe intervals (96 frames)
Superframe	D4 & SL	LFA off	The first correct Fs sequence that exists for 2 consecutive superframes
Extended superframe	ESF	LFA off	Recovery-of-frame alignment
Multiframe	CEPT	LMA off	The first correct instance of an MAS pattern that exists for 2 consecutive multiframes

Table 16. Mean Loss-of-Alignment Time

Alignment	Format	Mean Time*	
		True (Max)	False (Min)
Frame	DDS	—	—
Frame/superframe	D4 & SL	1.1 ms	1.4 min
	ESF (LFA)	2.1 ms	2.8 min
	ESF (LCC)	96 ms	132 ms
Multiframe	CEPT	4 ms	2.1 min

* Max times are for a 0.5 error rate; min times are for a 0.001 error rate.

Table 17. Loss-of-Alignment Criteria

Alignment	Format	Loss Indication	Loss Criterion
Frame	DDS	LFA on	4 FERs in 12 consecutive frames
	D4 & SL	LFA on	2 FERs in 4 consecutive Ft bits
	ESF	LFA on	2 FERs in 4 consecutive Fe bits
Superframe	D4 & SL	LFA on	Loss-of-frame alignment
Frame/superframe	ESF	LFA on	32 consecutive CERs (LCC)
Multiframe	CEPT	LMA on	2 consecutive MAS errors or TS16 = 0 in 2 consecutive multiframes

Facility Trouble and Alarm Processing

Fault and Alarm Detection

The criteria used to detect transmission facility faults and alarms fall into two categories: events and conditions. Event criteria activate the fault or alarm indication for each separate occurrence of the event. Condition criteria require algorithmic processing of a number of events to activate the fault or alarm indication. The indication persists until deactivated by a different event. Table 18 lists the event-activated faults and alarms detected by the T7229 Framer.

With the exception of LFVs and RFAs, all event indications remain activated for one frame (125 μs). LFV indications remain activated for one TDM bit interval (648 ns in DS1 and 488 ns in CEPT), while RFA indications remain activated until the following RFA event slot (125 μs in DDS/D4 and 250 μs in CEPT). The T7229 Framer does not recognize RFA for the *SLC* 96 Carrier mode.

Table 19 lists the fault and alarm conditions detected by the T7229 Framer. Condition indications remain activated for the duration of the condition. The receive signaling inhibit (RSI) fault indication on report lead RSI is a special case. It is the logical OR of FER, LFA, and LMA (in the PCS and IRSM modes) and is used by the 257AU receive synchronizer to prevent false signaling interpretations.

Table 18. Transmission Facility Fault and Alarm Events

Name	Symbol	Format	Activation Criterion
Line format violations	LFV	Bipolar/AMI	Any BPV
		B8ZS/HDB3	Any BPV not in a valid violation code
Frame alignment error	FER	D4 & SL	An error in an Ft bit
		ESF	An error in an Fe bit
		DDS	An error in an Ft, Fs or word-24 FAS bit
		CEPT	An error in a TS0 FAS bit

Table 18. Transmission Facility Fault and Alarm Events (Continued)

Name	Symbol	Format	Activation Criterion
Change-of-frame alignment	CFA	All	Synchronization at a new frame alignment
CRC-6 errors	CER	ESF	One or more CRC-6 check bits in error in any extended superframe
Remote multiframe alarm	RMA	PCS/IRSM	Bit 6 of TS16 MAS word = 1
Remote frame alarm	RFA	DDS	A word-24, bit 6 (RFA bit) = 0
		D4	Bit 2 of all words in one frame = 0
		CEPT	Bit 3 of TS0 not-word = 1
Alarm indication signal	AIS	All	Less than three 0s in a two-frame interval

Table 19. Transmission Facility Fault and Alarm Conditions

Name	Symbol	Format	Activation Criterion
Loss-of-frame alignment	LFA	DDS	4 FERs in 12 consecutive frames
		D4 & SL	2 FERs in 4 consecutive Ft bits
		ESF	2 FERs in 4 consecutive Fe bits
		CEPT	3 or 4 consecutive FERs (optional)
Loss-of-multiframe alignment	LMA	PCS/IRSM	2 consecutive MAS errors or TS16 = 0 in 2 consecutive multiframes
Remote frame alarm	RFA	ESF	A repeating 0x00FF pattern in the FDL after an initial 0x00 or 0xFF start-up sequence

Responses to Facility Trouble and Alarms

Consequent action is a CCITT term that covers responses to the detection of trouble or alarm conditions. The T7229 Framer provides two types of consequent actions: demand and automatic. Demand consequent actions are invoked by external command only; automatic consequent actions are hardware-implemented responses triggered by the detection of specific events or conditions. There are two categories of automatic consequent actions: standard and optional. Standard actions are mandatory; optional actions can be enabled or disabled by external command. Table 20 summarizes the consequent action capabilities of the T7229 Framer.

Table 20. Demand Consequent Actions Capabilities

Name	Symbol	Format	Action
Receive signaling inhibit	RSINH	All	RSI output lead = 1
Transmit TDM squelch	XCHSQ	DDS	T1DM UC code to words 1—23
		Other DS1	Idle code to all words
		CEPT	AIS to TS1—TS31
Transmit RFA	XRFAL	DDS	All word-24, bit 6 (RFA bits) = 0
		D4	Bit 2 of all words = 0
		ESF	Repeating 0x00ff pattern to FDL
		CEPT	Bit 3 of not-word = 1
Transmit RMA	XRMAL	CEPT	Bit 6 of MAS word = 1
Receive TDM squelch	RCHSQ	DDS	T1DM MOS code to words 1—23
Receive TS16 squelch	RSGSQ	CEPT	AIS to TS16

In DS1 modes, consequent actions are activated via a control byte input on SCS. In CEPT modes, however, the CCITT recommends a fast response to certain facility fault conditions. Accordingly, automatic fast responses can be enabled on an optional basis by an SCS consequent-action enable byte. Table 21 summarizes the automatic consequent actions.

Table 21. Automatic Consequent Actions

Action	Format	Trigger	Type
RSINH	All	FER, LFA	Standard
	PCS, IRSM	LMA	
RCHSQ	CEPT	LFA	Optional
RSGSQ	PCS/IRSM	LMA	Optional
XRFAL	CEPT	LFA	Optional
XRMAL	PCS/IRSM	LMA	Optional

The receiver side of the T7229 Framer activates receive signaling inhibit (RSIGN) for a one-frame interval after each detected FER and/or MER and for the duration of each LFA and/or LMA condition.

Each time a signaling bit is received, the receive synchronizer transfers that bit's previous value to back-up storage. When the RSI lead is set (RSINH is activated), the receive synchronizer freezes the signaling states at the back-up values and maintains this state for 32 frames after the RSI lead is cleared (RSINH is deactivated).

The RSGSQ capability is a means of passing on the RSINH function in applications that do not use the signaling extraction capabilities of the receive synchronizer.

System Status Monitoring

Device Duplication and Match Alarms

The principal techniques used for internal device fault monitoring are duplication and match circuitry. This technique checks output signals for internally generated errors and checks synchronizers and facility monitor detectors for algorithm failures. Table 22 lists the T7229 Framer duplication and match operations. Table 23 lists the interface signal checks performed by the framer.

Table 22. Device Duplication and Match Alarms

Symbol	Format	Activation Criterion
TDNMM	All	Transmit TDM output data mismatch
TFDCMM	SLC/DDS/ESF/IRSM	Transmit FDL output clock mismatch
RIDMM	All	Receive TDM output data mismatch
RFDMM	SLC/DDS/ESF/IRSM	Receive FDL output data mismatch
RFDCMM	SLC/DDS/ESF/IRSM	Receive FDL output clock mismatch
RSSPMM	D4 & SL	Receive superframe synchronizer pulse mismatch
LFVDMM	All	LFV detector output mismatch
FERDMM	All	FER detector output mismatch
LMADMM	All	LMA detector output mismatch
RMADMM	All	RMA detector output mismatch
RFADMM	All	RFA detector output mismatch
AISDMM	All	AIS detector output mismatch

Table 23. Device Interface Fault Condition Alarms

Symbol	Format	Activation Criterion
TPRPER	All	Transmit pseudorandom pattern error on TID
TLOSA	SL	Transmit loss-of-superframe alignment on TFD
TLOCLK	All	Transmit loss-of-clock on TICLK
RLOCLK	All	Receive loss-of-clock on RLCLK
SCSPER	All	Control stream parity error on SCS
TLOBA	CEPT	Transmit loss-of-TS0 biframe alignment on TID

Diagnostic Exercises

The T7229 Framer provides a number of diagnostic exercises to ensure that the device can detect and/or report faults and alarms. These exercises fall into five categories. Exercises that do not affect service, 1—6, check the system fault detection circuits without affecting normal operation. Exercises 8, 9, and 13—15, check the facility monitor circuits but do not affect normal data processing. Exercise 11, effects data processing the receiver input data stream to all 0s. The null exercise, 0, clears any other exercise and its responses. Exercises 7, 10, and 12 have no function. The response time for any exercise depends on the fault or alarm condition that it forces. Table 24 lists the system status exercises and their expected responses. Table 25 lists the facility status exercises and their expected responses.

Two exercises are required to fully check most duplicate and match circuits. The response to an exercise that does not affect service and that checks a facility monitor circuit may be inhibited when the corresponding facility fault or alarm indication is activated.

Table 24. System Status Exercise Responses

Exercise	Format	Activated Response	
		Report Bit	Reported Condition
0	All	None	None (clears all fault and alarm indications)
1	All	SR1, SR2	TLOCLK, LFVDMM
	All	SR3, SR4[1]	FERDMM, RFADMM
	Non-D4 DS1/IRSM	SR5, SR7[2]	TFDCMM, TDNMM
2	All	SR1, SR2	TLOCLK, LFVDMM
	All	SR3, SR4[1]	FERDMM, RFADMM
	Non-D4 DS1/IRSM	SR7[2]	TDNMM
3, 4	CEPT transparent	SR0	TLOBA
	All	SR1	TLOPRP
	All	SR3[3], SR4	LMADMM, RMADMM
	All	SR7	TDMNN
5	All	SR1	RLOCLK
	All	SR3	RSSPMM
	All	SR4	AISDMM
	All	SR5	RFDCMM
	Non-D4 DS1/IRSM	SR6[2]	RFDMM
	All	SR7	RIDMM
6	All	SR1	RLOCLK
	All	SR3	RSSPMM
	All	SR4	AISDMM
External	SL	SR0[4]	TLOSA
	All	SR2[5]	SCSPER

[1] May not respond if exercised during an RFA condition.
[2] May not respond if exercised while the FDL is inactive.
[3] May not respond if exercised during an LMA condition.
[4] TLOSA may be exercised by sending an incorrect Fs pattern to the FDL.
[5] SCSPER may be exercised by sending bad parity on the SCS.

Table 25. Facility Status Exercise Responses in Non-BOS Modes

Exercise	Format	Activated Response		
		Report Bit	Report Lead	Reported Condition
0	All	None	None	None
8	All	FR0	RLV	LFV
	ESF	FR4	RCEMA	CER
	ESF	FR5	None	LCC*
	D4 & DDS	FR6	RRFMA	RFA
	ESF	FR6	RRFMA	CRFA
9	PCS/IRSM	FR5	RRFMA	AIS
	CEPT	FR6	RRFMA	RFA
	All	FR7	None	AIS
11	All	FR1	RFE	FER
	All	FR2	RLF	LFA
	ESF	FR4	RCEMA	CER
	PCS/IRSM	FR4	RCEMA	LMA
	D4 & DDS	FR6	RRFMA	RFA
	All	None	RSI	FER, LFA, LMA
13	All	FR1	RFE	FER
	All	FR2	RLF	LFA
	PCS/IRSM	FR4	RCEMA	LMA
14	All	FR1	RFE	FER
	All	FR2	RLF	LFA
	DDS, ESF, & CEPT	FR3	None	CFA
	PCS/IRSM	FR4	RCEMA	LMA
15	ESF	FR3*,**	None	CFA
	ESF	FR5	None	LCC

* Response may require more than 150 ms to activate.
** Response activates only if an FAS emulator is present.

Control and Status

Serial Control Stream

Control and maintenance commands to the T7229 Framer are input on SCS at a 1.024-Mb/s rate. The commands are organized into groups of 8-bit bytes and are accepted on SCS when CTLE is held high. The last eight bits entered are stored as a command byte; preceding bits are ignored. Once a command has been entered, it remains in effect until explicitly changed. Command bytes may have arbitrary phase in relation to system sync (SSYN). Control bytes consist of four types: option, exercise, consequent action, and action control bytes. Figure 5 illustrates the bit assignments for each control type.

As illustrated in Figure 5, each control byte consists of eight bits, labeled CB0 (LSB)—CB7 (MSB). CB7 is a parity bit that forces odd parity across the entire byte. Control bits 4, 5, and 6 (CB4—CB6) determine the control byte type.

An option byte is selected when CB6 = 0. For this byte, bit positions CB0—CB5 are relabeled OP0—OP5, respectively, and are used to select individual T7229 Framer options. DS1 mode is selected when OP0 is low and the remaining option bits, OP1—OP5, are used to select line format and frame format structures, as listed in Table 26. CEPT mode is selected when either OP0 = 1 and/or OS0 = 1. CEPT mode options are listed in Table 27. In CEPT mode, the OS0—OS5 option select leads control the same options listed in Tables 26 and 27 for the respective bit positions OP0—OP5. Although the selected option is determined by the logical OR of the two possible sources of option selections, only one source for option selection should be used.

In CEPT mode, OP2 determines the loss-of-frame alignment error condition. When OP2 = 1, three consecutive frame alignment signal errors activate a loss-of-frame alignment signal (LFA) error. When OP2 = 0, four consecutive frame alignment signal errors are required before an LFA error is reported.

In the DDS-TDM mode, FDL processing is inactive; in the DDS-FDL mode, FDL data is copied to and from word-24, bit 7.

Tables 28—30 list the exercise, consequent action, and action control bit assignments.

CONTROL BIT	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
OPTION BYTE	PAR	0	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0
EXERCISE BYTE	PAR	1	0	0	EX3	EX2	EX1	EX0
ACTION CONTROL BYTE	PAR	1	0	1	AC3	AC2	AC1	AC0
CONSEQUENT ACTION BYTE	PAR	1	1	AB4	AB3	AB2	AB1	AB0

Figure 5. Control Byte Formats

Table 26. DS1 Option-Byte Bit Assignments (OP0 = 0)

OP5*	OP4*	OP3*	OP2*	OP1*	OP0*	Word-24	ZCS	Line Format	Frame Format
x	x	0	x	x	0	Transparent	—	—	—
x	x	1	x	x	x	DDS FAS Word	—	—	—
x	x	x	0	0	x	—	Off	—	—
x	x	x	1	0	x	—	On	—	—
x	x	x	x	0	x	—	—	Bipolar	—
x	x	x	x	1	x	—	—	B8ZS	—
0	0	0	x	x	x	—	—	—	D4
1	0	0	x	x	x	—	—	—	SL
x	1	0	x	x	x	—	—	—	ESF
x	0	1	x	x	x	—	—	—	DDS-TDM
x	1	1	x	x	x	—	—	—	DDS-FDL

* x = don't care.

Table 27. CEPT Mode Option Bit Definitions (OP0 = 1)

OP5*	OP4*	OP3*	OP2*	OP1*	Line Format	FAS Errors	Frame Format	Control Bit Mode
x	x	x	x	0	AMI	—	—	—
x	x	x	x	1	HDB3	—	—	—
x	x	x	0	x	—	4	—	—
x	x	x	1	x	—	3	—	—
x	0	0	x	x	—	—	CCS	—
x	1	0	x	x	—	—	IRSM	—
x	0	1	x	x	—	—	PCS0	—
x	1	1	x	x	—	—	PCS1	—
0	x	x	x	x	—	—	—	Transparent
1	x	x	x	x	—	—	—	All 1s

* x = don't care.

Table 28. Exercise-Byte Bit Assignments

EX3	EX2	EX1	EX0	Exercise Number
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
1	0	0	0	8
1	0	0	1	9
1	0	1	1	11
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 29. Demand Consequent-Action-Byte Bit Assignments

					DS1			CEPT Mode		
AB4*	AB3*	AB2*	AB1*	AB0*	DDS/ESF	D4	SL	CCS	PCS	IRSM
x	x	x	x	1	RCHSQ	RCHSQ	RCHSQ	RCHSQ	RCHSQ	RCHSQ
x	x	x	1	x	RDLSQ	—	RDLSQ	—	RSGSQ	RSGSQ
x	x	1	x	x	XRFAL	XRFAL	—	XFRAL	XRFAL	XRFAL
x	1	x	x	x	XDLSQ	—	—	—	XRMAL	XRMAL
1	x	x	x	x	XCHSQ	XCHSQ	XCHSQ	XCHSQ	XCHSQ	XCHSQ

* x = don't care.

Table 30. Action-Control-Byte Bit Assignments

AC3*	AC2*	AC1*	AC0*	Format	Action	Trigger
x	x	x	1	CEPT	RCHSQ	LFA
x	x	1	x	PCS/IRSM	RSGSQ	LMA
x	1	x	x	CEPT	XRFAL	LFA
1	x	x	x	PCS/IRSM	XRMAL	LMA

* x = don't care.

In the T7229 Framer, the action control byte is used to control the optional automatic consequent actions. Bits AC0, AC1, and/or AC2 must be set to enable the consequent actions. All unused bits should be cleared.

Status Report Mechanisms. Facility fault and alarm reports are available on both the serial report stream bits (FR0—FR7) and on the external report leads. System status alarms are reported only on the report stream. For maintenance purposes, the report stream provides a means of auditing the contents of the device's internal control registers previously set by serial control commands and/or option select pins. The device outputs the serial report stream on SRS at a 1.024-Mb/s rate in fixed relation to system sync (SSYN).

A serial report stream contains six report byte types (illustrated in Figure 6), organized into a serial report stream frame consisting of 16 bytes (as illustrated in Figure 7).

A facility report byte is transmitted at the start of each frame. The next five bytes consist of a system status (device alarms) report, exercise audit, option audit, consequent action audit, and action control audit byte, respectively. Two null bytes, all 0s, are then transmitted, followed by the retransmission of the previous eight bytes. The lower-order bit is transmitted first for each byte output on SRS.

Table 31 lists the facility fault alarm bit status. Table 32 lists the system fault alarm bit assignments.

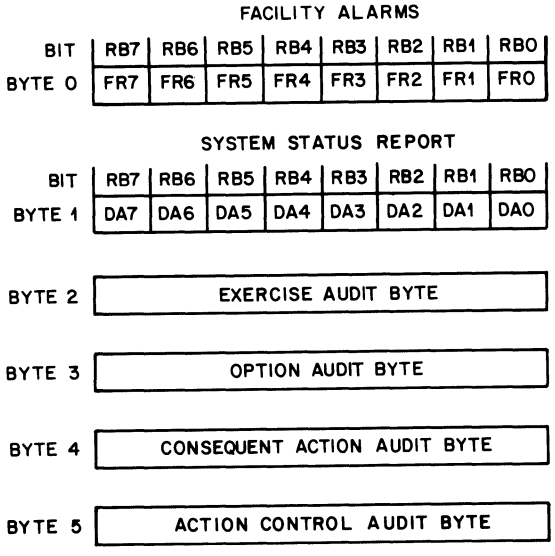


Figure 6. Report Byte Formats

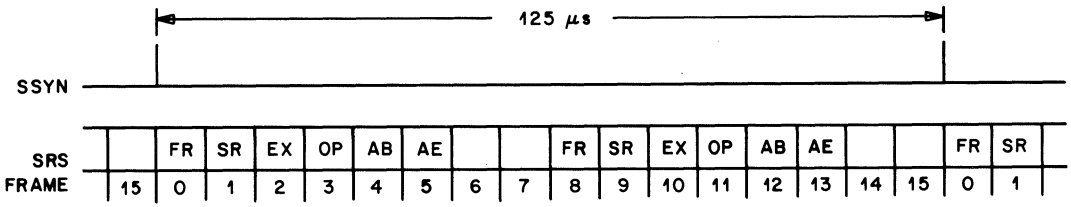


Figure 7. Serial Report Stream Frame Format

Table 31. Facility Status Report-Byte Bit Assignments

FR7*	FR6*	FR5*	FR4*	FR3*	FR2*	FR1*	FR0*	Format	Report
x	x	x	x	x	x	x	1	All	LFV
x	x	x	x	x	x	1	x	All	FER
x	x	x	x	x	1	x	x	All	LFA
x	x	x	x	1	x	x	x	All	CFA
x	x	x	1	x	x	x	x	ESF	CER
								PCS/IRSM	LMA
x	x	1	x	x	x	x	x	ESF	LCC
								PCS/IRSM	RMA
x	1	x	x	x	x	x	x	D4 & DDS	RFA
								ESF	CRFA
1	x	x	x	x	x	x	x	All	AIS

* x = don't care.

Table 32. System Status Report-Byte Bit Assignments

SR7*	SR6*	SR5*	SR4*	SR3*	SR2*	SR1*	SR0*	Format	Report
x	x	x	x	x	x	x	1	SL	TLOSA
								CEPT	TLOBA
x	x	x	x	x	x	1	x	All	TPRPER, TLOCLK, RLOCLK
x	x	x	x	x	1	x	x	All	SCSPER, LFVDMM
x	x	x	x	1	x	x	x	All	FERDMM
								D4 & SL	RSSPMM
								PCS/IRSM	LMADMM
x	x	x	1	x	x	x	x	All	AISDMM, RFADMM
								PCS/IRSM	RMADMM
x	x	1	x	x	x	x	x	Non-D4	TFDCMM, RFDCMM
x	1	x	x	x	x	x	x	Non-D4	RFDMM
1	x	x	x	x	x	x	x	All	TDNMM, RIDMM

* x = don't care.

The second report mechanism in the T7229 Framer is the dedicated report lead. Table 33 shows the assignment of facility fault and alarm reports to these leads.

Table 33. Facility Status Report-Lead Assignments

Report Lead	Format	Report
RLV	All	LFV
RFE	All	FER
RLF	All	LFA
RCEMA	ESF	CER
	PCS/IRSM	LMA
RRFMA	D4 &DDS	RFA
	ESF	CRFA
	PCS/IRSM	RFA, RMA
RSI	PCS/IRSM	FER, LFA, LMA
	All other	FER, LFA

Characteristics

Clocks

Clock	Period	Tolerance	Unit	Duty Cycle*	Mode
RLCLK	648	100 ± 2%	ns	50 ± 5%	DS1
	488	100 ± 2%	ns	50 ± 5%	CEPT
TICLK	648	100 ± 1%	ns	50 ± 8%	DS1
	488	100 ± 1%	ns	50 ± 5%	CEPT
SCLK	244	100 ± 1%	ns	50 ± 5%	All
RFDCLK	125	—	μs	50 ± 1%	DDS
	250	—	μs	25 ± 1%	SL, ESF, IRSM
TFDCLK	125	—	μs	50 ± 1%	DDS
	250	—	μs	75 ± 1%	SL, ESF, IRSM

* Duty cycle = zero-level duration / (clock period)*100.

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Parameter	Sym	Min	Typ	Max	Unit
Supply current	I_{DD}	—	20	30	mA
Input current:					
low	I_{IL}	—	—	–20	μA
high	I_{IH}	20	—	—	μA
Output current:					
low	I_{OL}	—	2.2	—	mA
high	I_{OH}	—	0.2	—	mA
Input voltage:					
low	V_{IL}	—	—	0.8	V
high	V_{IH}	2.1	—	—	V
Output voltage:					
low	V_{OL}	—	—	0.4	V
high	V_{OH}	2.4	—	—	V
Power dissipation	PD	—	100	150	mW

Maximum Ratings

DC supply voltage (V_{DD}) range ..... –0.5 to +7 V
Power dissipation (PD) ..... 300 mW
Storage temperature (Tstg) range ..... –40 to +125 °C

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded or soldered safely at temperatures up to 300 °C.

Timing Characteristics

Symbol	Description	Min	Typ	Max	Unit	Mode
tSCHTCH	Skew time SCLK to TICLK	−122	10	142	ns	All
tSSHSSL	SSYN pulse duration	—	244	—	ns	All
tSSHTCH	Pulse set-up time SSYN to TICLK	40	—	—	ns	All
tTCHSSL	Pulse hold time TICLK to SSYN	35	—	—	ns	All
tSSHSCH	Pulse set-up time SSYN to SCLK	40	—	—	ns	All
tSCHSSL	Pulse hold time SCLK to SSYN	35	—	—	ns	All
tRPVRCH	Data set-up time RPDN to RLCLK	40	—	—	ns	All
tRNVRCH	Data set-up time RNDN to RLCLK	40	—	—	ns	All
tRCHRPX	Data hold time RLCLK to RPDN	35	—	—	ns	All
tRCHRNX	Data hold time RLCLK to RNDN	35	—	—	ns	All
tRCLRDV	Propagation delay RLCLK to RID	0	—	140	ns	All
tRCLRSH	Propagation delay RLCLK to RISYN	0	—	140	ns	All
tRCLRSL	Propagation delay RLCLK to RISYN	0	—	140	ns	All
tTDVTCH	Data set-up time TID to TICLK	40	—	—	ns	All
tTCHTDX	Data hold time TICLK to TID	35	—	—	ns	All
tTCLTSV	Propagation delay TICLK to TISYN	0	—	140	ns	All
tTCHTPV	Propagation delay TICLK to TPDN	0	—	140	ns	All
tTCHTNV	Propagation delay TICLK to TNDN	0	—	140	ns	All
tTCHTLL	Propagation delay TICLK to TLCLK	0	—	100	ns	All
tTCLTLH	Propagation delay TICLK to TLCLK	0	—	140	ns	All
tRKLRFV	Skew time RFDCLK to RFD	−4	0	4	μs	All
tTFVTKH	Data set-up time TFD to TFDCLK	40	—	—	ns	All
tTKHTFX	Data hold time TFDCLK to TFD	35	—	—	ns	All
tCSVCSV	SCS time-slot period	—	976	—	ns	All
tSRVSRV	SRS time-slot period	—	976	—	ns	All
tCSVSCH	Data set-up time SCS to SCLK	40	—	—	ns	All
tCEVSCH	Data set-up time CTLE to SCLK	40	—	—	ns	All
tSCHCSX	Data hold time SCLK to SCS	35	—	—	ns	All
tSCHCEX	Data hold time SLCK to CTLE	35	—	—	ns	All
tSCHSRV	Propagation delay SCLK to SRS	0	—	140	ns	All
tRCLRVV	Propagation delay RLCLK to RLV	0	—	140	ns	All
tRCLREV	Propagation delay RLCLK to RFECE	0	—	140	ns	All
tRCLRLV	Propagation delay RLCLK to RLF	0	—	140	ns	All
tRCLRAV	Propagation delay RLCLK to RCEMA	0	—	140	ns	All
tRCLRMV	Propagation delay RLCLK to RRFMA	0	—	140	ns	All
tRCLRIV	Propagation delay RLCLK to RSI	0	—	210	ns	All

Notes:
A maximum capacitive loading of 80 pF is assumed on all outputs. For higher capacitive loadings the propagation delays would have to be adjusted.
All outputs are capable of sourcing up to 4.50 mA at 2.4 V and sinking up to 2.90 mA at 0.4 V.

Timing Diagrams

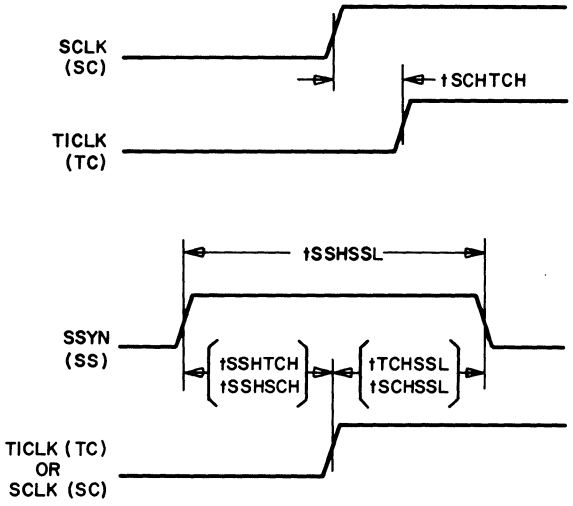


Figure 8. Clock Signals

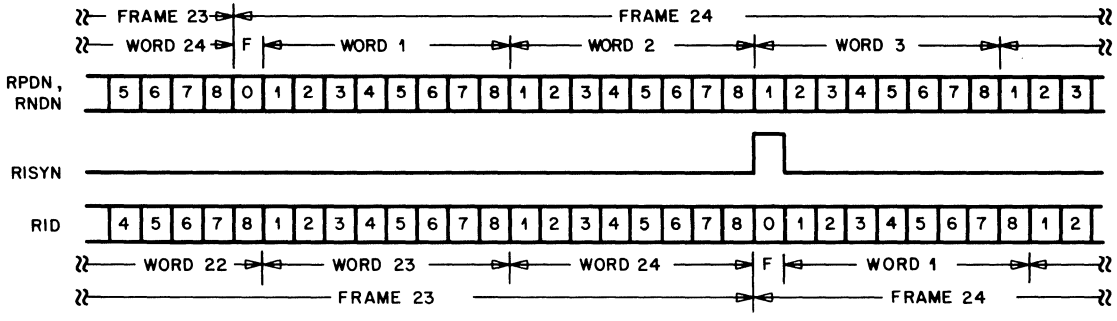


Figure 9. Receiver TDM Timing (DS1 Mode)

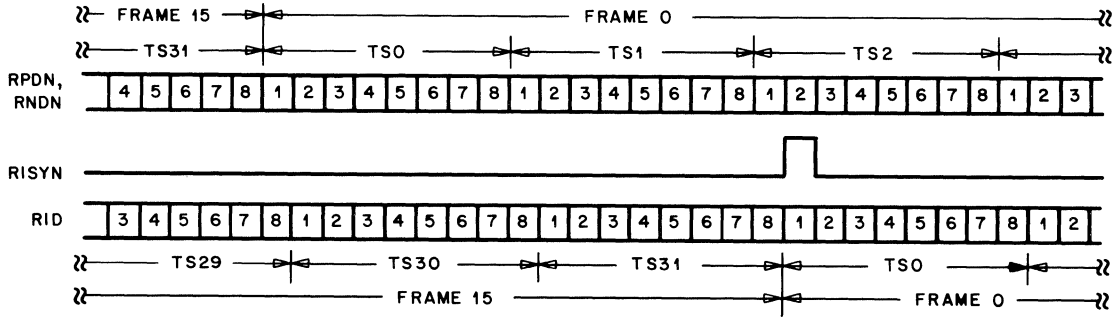


Figure 10. Receiver TDM Timing (CEPT Mode)

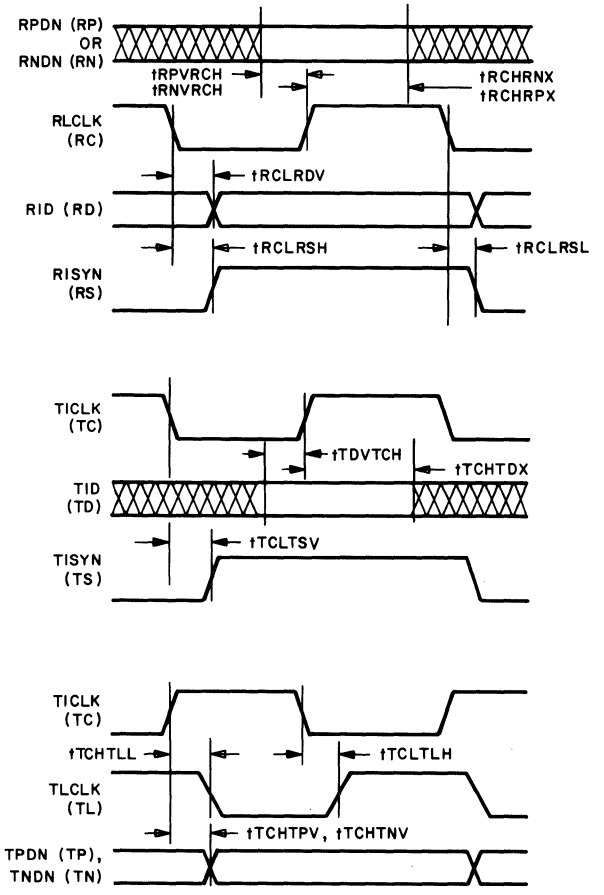


Figure 11. Line Rate I/O Signals

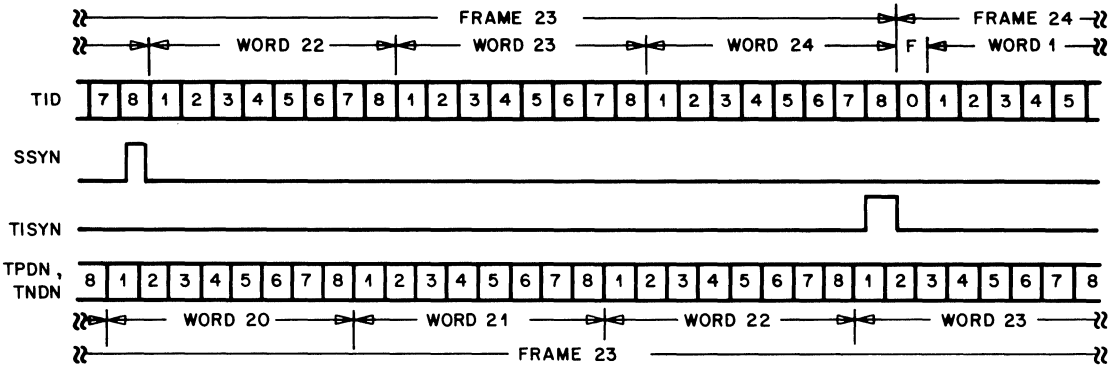


Figure 12. Transmitter TDM Timing (DS1 Mode)

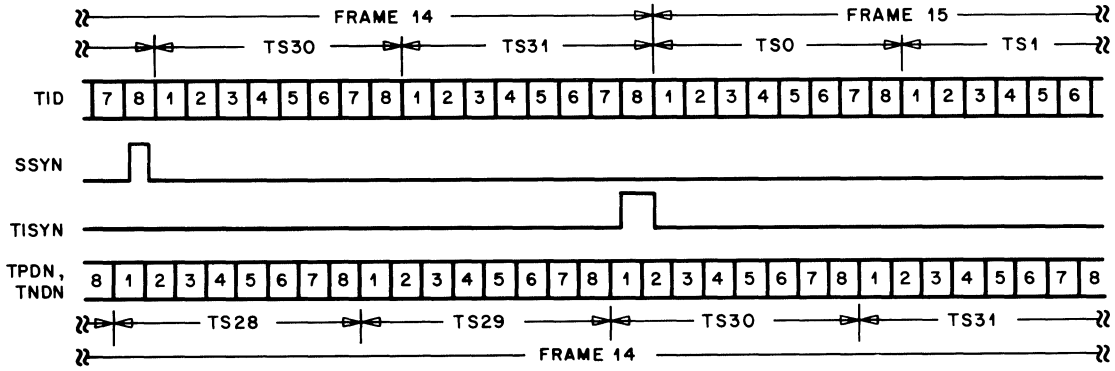


Figure 13. Transmitter TDM Timing (CEPT Mode)

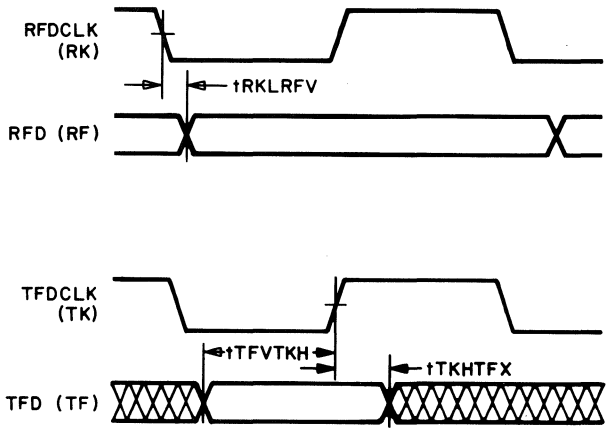


Figure 14. Facility Data Link Clocks and Data

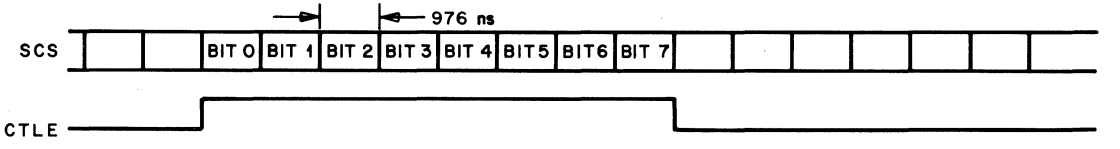


Figure 15. Serial Control Stream Bit Timing

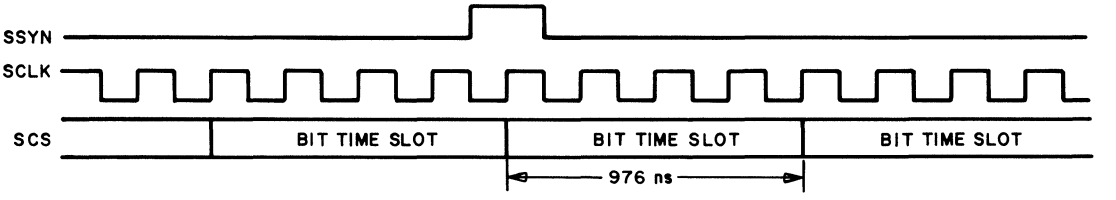


Figure 16. Serial Control Stream Byte Timing

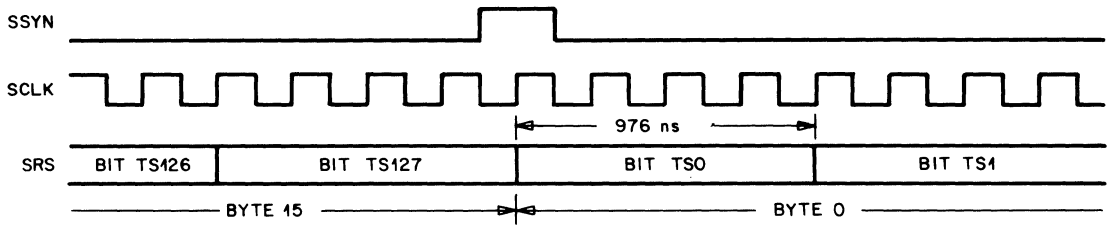


Figure 17. Serial Report Stream Bit Timing

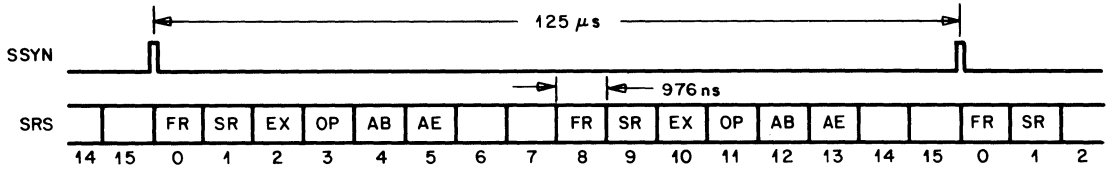


Figure 18. Serial Report Stream Frame Timing

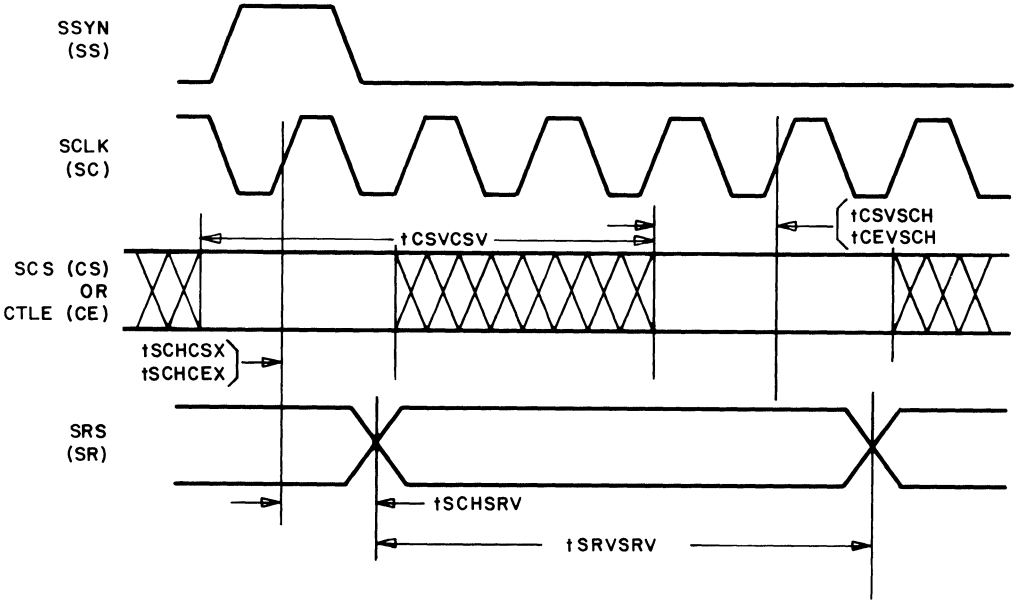


Figure 19. Serial Stream I/O

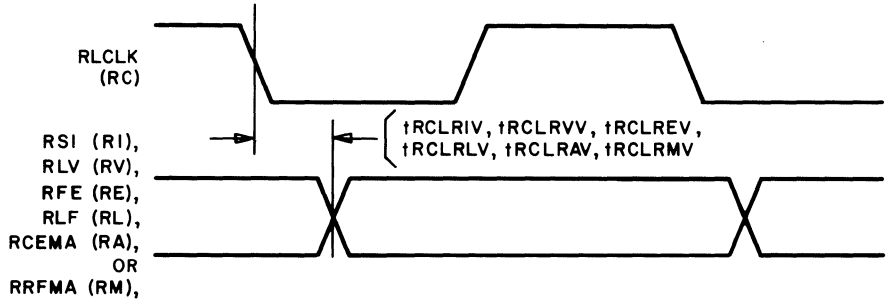


Figure 20. Status Outputs

6. Signal Processing

T7032 Clock Recovery Circuit

Features

- Pin-programmable for 1-MHz to 50-MHz operation
- Fiber and wire applications
- Single 5 V supply
- Only one external component required: 3.58-MHz crystal

Description

The T7032 Clock Recovery Circuit integrated circuit operates over a 1-MHz to 50-MHz frequency range and provides clock recovery, data retiming, and a polynomial-based descrambler. The descrambler can be disabled for those applications where no data scrambler is used. This device accepts TTL-NRZ data from a receiver (optical or electrical), recovers the clock, and retimes the data to the recovered clock. The inputs and outputs are TTL-compatible and the circuit requires a single 5 V supply. The T7032 Clock Recovery Circuit is manufactured using CMOS technology and is available in a 300-mil, 20-pin plastic DIP. The device may be used for many general-purpose clock recovery and retiming applications, such as the *ODL* 50 Lightwave Data Link.

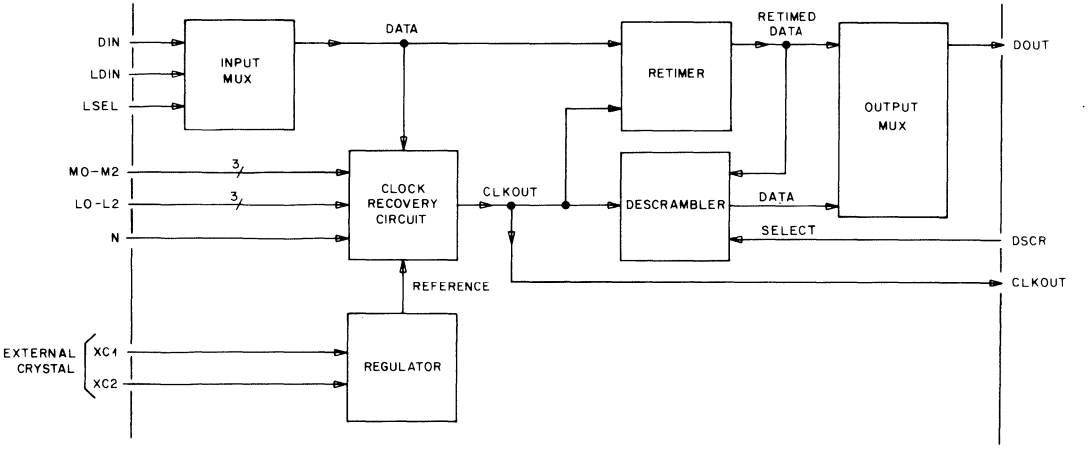
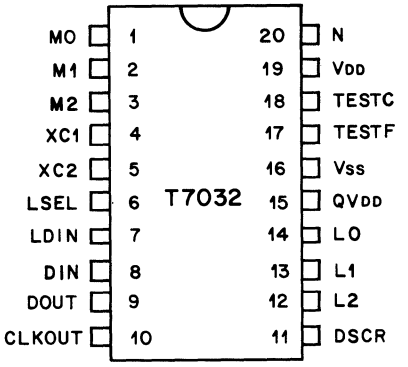


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
CLKOUT	10	M1	2
DIN	8	M2	3
DOUT	9	N	20
DSCR	11	QVDD	15
L0	14	TESTC	18
L1	13	TESTF	17
L2	12	VDD	19
LDIN	7	VSS	16
LSEL	6	XC1	4
M0	1	XC2	5

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1 2 3	M0 M1 M2	I	**Frequency Selects.** These pins, with pins 12—14 and 20, set the operating frequency range of the circuit. See Table 2 for frequency band selection.
4,5	XC1,XC2	I	**XTAL1 and XTAL 2.** Connect a 3.579545-MHz crystal between these pins.
6	LSEL	I	**Alternate Data Select.** Tie to 0 V to select DIN (pin 8) as the data input; tie to 5 V to select LDIN (pin 7) as the data input.
7	LDIN	I	**Alternate Data In.**
8	DIN	I	**Data In.**
9	DOUT	O	**Data Out.** Descrambled serial data output.
10	CLKOUT	O	**Clock Out.**
11	DSCR	I	**Descrambler.*** Tie to 0 V for normal data at DOUT; tie to 5 V for descrambled data at DOUT.
12 13 14	L2 L1 L0	I	**Frequency Selects.** These pins, with pins 1—3 and 20, set the operating frequency range of the circuit. See Table 2 for frequency band selection.

* The descrambler on the T7032 Clock Recovery Circuit can be used in conjunction with the scrambler on the *ODL*® 50 Transmitter. It is an $x^7 + x^4$ polynomial with a built-in counter that should prevent a lock-up of the scrambler by certain periodic patterns. The use of the descrambler is optional when the *ODL* 50 Transmitter is used.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
15	QVDD	—	**Quiet VDD 5 V Supply.** Extra care may be required when filtering this voltage. The required filtering can be supplied with a 10-Ω resistor connected to VDD (pin 19) and a 0.1-μF capacitor connected to ground.
16	VSS	—	**Ground.** 0 V.
17	TESTF	I	**Test F Pin.** Used for manufacturing test purposes; should be tied to 5 V for normal operation.
18	TESTC	I	**Test C Pin.** Used for manufacturing test purposes; should be tied to 5 V for normal operation.
19	VDD	—	**5 V Supply.**
20	N	I	**Frequency Select.** This pin, with pins 1—3 and 12—14, sets the operating frequency range of the circuit. See Table 2 for frequency band selection.

Note: A circuit board ground plane is required for optimum performance.

Overview

The on-chip clock recovery circuit consists of a digital frequency-locked loop and a phase-locked loop, which extract the clock from the positive going edges of the input data. This recovered clock is used with the input data in the retimer section to synchronize the output data (DOUT) with the positive edge of the clock output (CLKOUT). As a pin-selectable option (DSCR), the retimed data can be fed to the on-chip seven-stage descrambler (compatible with the *ODL* 50 Transmitter) and the descrambled data will appear at DOUT (pin 9).

To ensure accurate frequency selection, the T7032 Clock Recovery Circuit uses an external 3.58-MHz crystal in its oscillator reference section. The operating frequency of the device is then determined by the circuit's seven frequency select pins, which are made high (5 V) or low (0 V). (See Table 2.) Special care is required for filtering the 5 V supply (VDD) on pin 15 (QVDD) since voltage variations on this pin may cause excessive jitter on the clock and data outputs.

DIN and LDIN are equivalent inputs. Typically, LDIN is used for the data loopback mode of system operation. For normal operation, TESTC (pin 18) and TESTF (pin 17) must be tied to 5 V. These pins are used only for testing during manufacture.

There are six octave selections that can be chosen from the frequency band selections in Table 2. Nine frequency bands can be selected from each octave. For optimal performance, a frequency of operation that is within the bands set by the seven frequency select pins must be selected.

Noise Properties

Noisy data under worst-case conditions produces a small eye opening and a large amount of phase jitter on the data input. Under these conditions, the T7032 Clock Recovery Circuit recovers the average clock and retimes the data, reducing jitter. Figures 3 and 4 illustrate the improvement of data quality through the circuit. At the limit of sensitivity, the clock recovery circuit imposes a typical noise penalty (noise factor) of < 1 dB.

Table 2. Frequency Band Selections (MHz)

M2	M1	M0	L2	L1	L0	N	Frequency Min	Frequency Max
Octave 6								
0	0	0	0	0	0	1	46.3626	51.2715
0	0	0	0	0	1	0	41.9403	46.3626
0	0	0	0	0	1	1	38.5908	41.9403
0	0	0	0	1	0	0	35.4895	38.5908
0	0	0	0	1	0	1	33.0611	35.4895
0	0	0	0	1	1	0	30.7495	33.0611
0	0	0	0	1	1	1	28.9096	30.7495
0	0	0	1	0	0	0	27.1293	28.9096
0	0	0	1	0	0	1	24.8300	27.1293
Octave 5								
0	0	1	0	0	0	1	23.1720	25.6254
0	0	1	0	0	1	0	20.9617	23.1720
0	0	1	0	0	1	1	19.2876	20.9617
0	0	1	0	1	0	0	17.7376	19.2876
0	0	1	0	1	0	1	16.5239	17.7376
0	0	1	0	1	1	0	15.3685	16.5239
0	0	1	0	1	1	1	14.4490	15.3685
0	0	1	1	0	0	0	13.5592	14.4490
0	0	1	1	0	0	1	12.4100	13.5592
Octave 4								
0	1	0	0	0	0	1	11.5766	12.8024
0	1	0	0	0	1	0	10.4724	11.5766
0	1	0	0	0	1	1	9.6360	10.4724
0	1	0	0	1	0	0	8.8617	9.6360
0	1	0	0	1	0	1	8.2553	8.8617
0	1	0	0	1	1	0	7.6781	8.2553
0	1	0	0	1	1	1	7.2187	7.6781
0	1	0	1	0	0	0	6.7741	7.2187
0	1	0	1	0	0	1	6.2000	6.7741

Table 2. Frequency Band Selections (MHz) (Continued)

M2	M1	M0	L2	L1	L0	N	Frequency Min	Frequency Max
Octave 3								
0	1	1	0	0	0	1	5.7883	6.4012
0	1	1	0	0	1	0	5.2362	5.7883
0	1	1	0	0	1	1	4.8180	5.2362
0	1	1	0	1	0	0	4.4308	4.8180
0	1	1	0	1	0	1	4.1276	4.4308
0	1	1	0	1	1	0	3.8390	4.1276
0	1	1	0	1	1	1	3.6093	3.8390
0	1	1	1	0	0	0	3.3871	3.6093
0	1	1	1	0	0	1	3.1000	3.3871
Octave 2								
1	0	0	0	0	0	1	2.8942	3.2006
1	0	0	0	0	1	0	2.6181	2.8942
1	0	0	0	0	1	1	2.4090	2.6181
1	0	0	0	1	0	0	2.2154	2.4090
1	0	0	0	1	0	1	2.0638	2.2154
1	0	0	0	1	1	0	1.9195	2.0638
1	0	0	0	1	1	1	1.8047	1.9195
1	0	0	1	0	0	0	1.6935	1.8047
1	0	0	1	0	0	1	1.5500	1.6935
Octave 1								
1	0	1	0	0	0	1	1.4564	1.6106
1	0	1	0	0	1	0	1.3175	1.4564
1	0	1	0	0	1	1	1.2123	1.3175
1	0	1	0	1	0	0	1.1149	1.2123
1	0	1	0	1	0	1	1.0386	1.1149
1	0	1	0	1	1	0	0.9660	1.0386
1	0	1	0	1	1	1	0.9082	0.9660
1	0	1	1	0	0	0	0.8522	0.9082
1	0	1	1	0	0	1	0.7800	0.8522

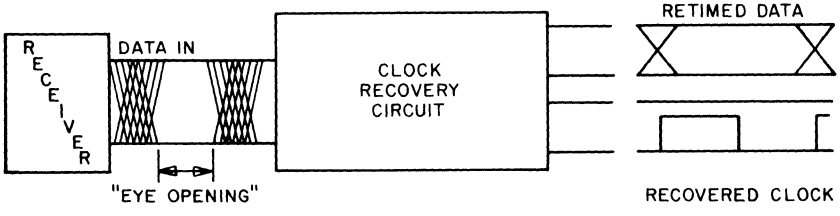


Figure 3. Clock Recovery with Noisy Data

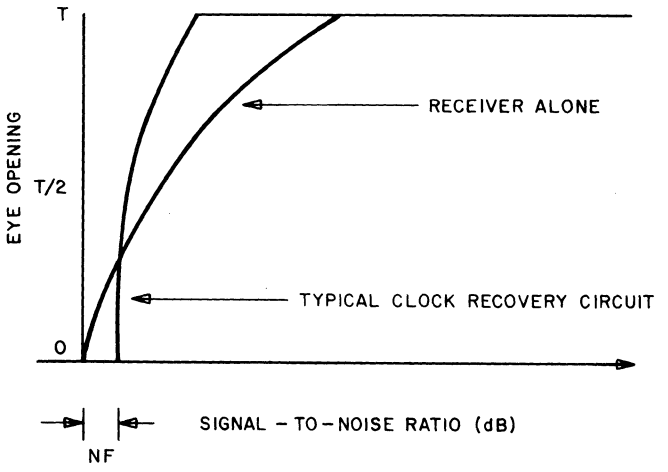


Figure 4. Eye Opening Versus Signal-to-Noise Ratio

Characteristics

A circuit board ground plane is required for optimum performance.

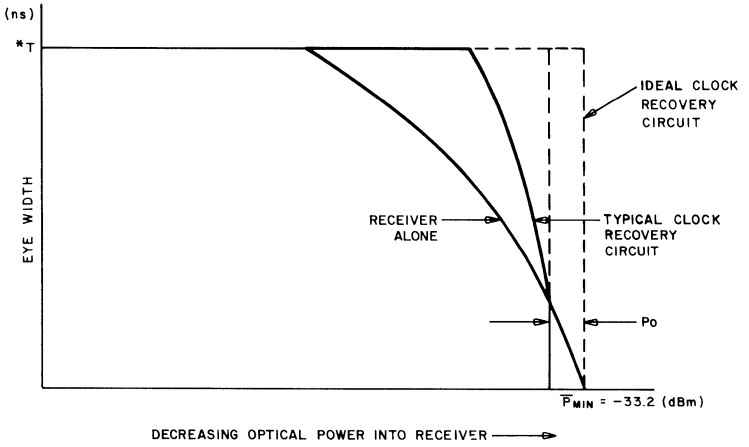
Optical Parameters

Operating temperature, T_A = 0 to 70 °C

Optical parameters for the T7032 Clock Recovery Circuit are given in the following table. The optical parameters shown are based on *ODL* 50 Lightwave Data Link characteristics. Other data link designs may result in different system parameters.

Parameter	Sym	Min	Max	Unit
Optical power penalty (50 Mb/s at 10^{-9} BER)	Po	—	1	dB
Clock output rms jitter (2^7 – 1 pseudorandom word)	°rms	—	5.5	°rms

Two operating modes are shown in Figure 5: the *ODL* 50 Receiver response alone and a typical response using the *ODL* 50 Receiver with the T7032 device to retime and improve data quality. When using the T7032 device, the eye width improves above the intersection of the curves (–32.2 dBm for maximum Po).



Note: The optical parameters shown are based on *ODL* 50 Lightwave Data Link characteristics.
* T = 1/bit rate.

Figure 5. Eye Width Versus Average Incident Optical Power

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit
Output voltage:				
I_{OL} = 4 mA	V_{OL}	—	0.4	V
I_{OH} = −0.4 mA	V_{OH}	2.4	—	V
Output current high	I_{OS}	−25	—	mA
Power supply current drain	I_{DD}	—	60	mA
Input voltages DIN, LDIN, LSEL:				
low	V_{IL}	—	0.8	V
high	V_{IH}	2.0	—	V
All other inputs:				
low	V_{IL}	—	0.5	V
high	V_{IH}	4.5	—	V
Noise factor* (see Figure 4)	NF	—	1	dB

* Measured at typical conditions of V_{DD} = 5 V, 25 °C, 50 Mb/s at 1 x 10^{-9} BER with a data pattern of $2^{23} - 1$.

Maximum Ratings

DC supply voltage (V_{DD}) ..... 6 V
Short-circuit output current (I_{OS}) ..... −100 mA
Power dissipation (PD) ..... 0.5 W
Storage temperature (Tstg) range ..... −40 to +125 °C
Lead soldering temperature and time ..... 240 °C/10 s

Maximum ratings are defined as the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External Reference Crystal Requirements

Frequency: 3.579545 MHz ± 0.05%, 0 to 70 °C
Series resistance: 150 Ω, maximum

Calibrated at 16-pF series capacitance

Timing Characteristics

Parameter	Min	Max	Unit
Data input rise time	—	5	ns
Data output transition*	—	5	ns
Data output jitter**	0	7	°rms
Clock skew (relative to data output)	–3	0	ns

* Transition time is in terms of 10% and 90% values.
** Jitter is in terms of the 50% value for 1010... data input.

Timing Diagram

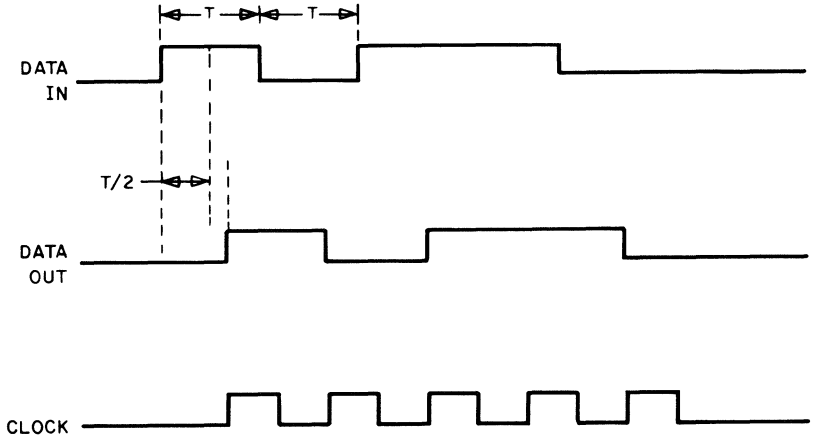


Figure 6. Timing Waveforms

T7033 Clock Recovery Circuit

Features

- Pin-programmable for 1-MHz to 50-MHz operation
- Fiber and wire applications
- Single 5 V supply
- Only one external component required: 3.58-MHz crystal

Description

The T7033 Clock Recovery Circuit integrated circuit operates over a 1-MHz to 50-MHz frequency range and provides clock recovery and data retiming. This device accepts TTL-NRZ data from a receiver (optical or electrical), recovers the clock, and retimes the data to the recovered clock. The inputs and outputs are TTL-compatible and the circuit requires a single 5 V supply. The T7033 Clock Recovery Circuit is manufactured using CMOS technology and it is available in a 300-mil, 20-pin plastic DIP. The device is intended for applications where an internal descrambler is not required.

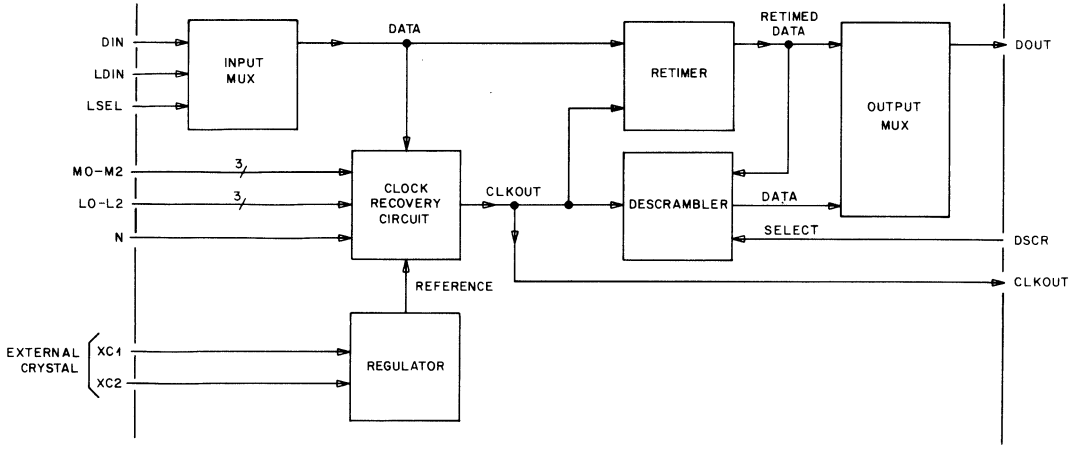
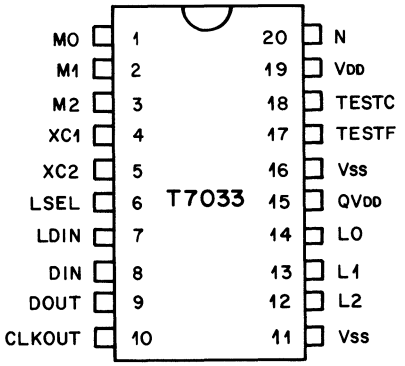


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
CLKOUT	10	M2	3
DIN	8	N	20
DOUT	9	QVDD	15
L0	14	TESTC	18
L1	13	TESTF	17
L2	12	VDD	19
LDIN	7	VSS	11
LSEL	6	VSS	16
M0	1	XC1	4
M1	2	XC2	5

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1 2 3	M0 M1 M2	I	**Frequency Selects.** These pins, with pins 12—14 and 20, set the operating frequency range of the circuit. See Table 2 for frequency band selection.
4,5	XC1,XC2	I	**XTAL1 and XTAL 2.** Connect a 3.579545-MHz crystal between these pins.
6	LSEL	I	**Alternate Data Select.** Tie to 0 V to select data on DIN (pin 8); tie to 5 V for data on LDIN (pin 7).
7	LDIN	I	**Alternate Data In.**
8	DIN	I	**Data In.**
9	DOUT	O	**Data Out.** Serial data output.
10	CLKOUT	O	**Clock Out.**
11	VSS	—	**Ground.** 0 V.
12 13 14	L2 L1 L0	I	**Frequency Selects.** These pins, with pins 1—3 and 20, set the operating frequency range of the circuit. See Table 2 for frequency band selection.

Note: A circuit board ground plane is required for optimum performance.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
15	QVDD	—	**Quiet VDD 5 V Supply.** Extra care may be required when filtering this voltage. The required filtering can be supplied with a 10-Ω resistor connected to VDD (pin 19) and a 0.1-μF capacitor connected to ground.
16	VSS	—	**Ground.** 0 V.
17	TESTF	I	**Test F Pin.** Used for manufacturing test purposes; should be tied to 5 V for normal operation.
18	TESTC	I	**Test C Pin.** Used for manufacturing test purposes; should be tied to 5 V for normal operation.
19	VDD	—	**5 V Supply.**
20	N	I	**Frequency Select.** This pin, with pins 1—3 and 12—14, sets the operating frequency range of the circuit. See Table 2 for frequency band selection.

Note: A circuit board ground plane is required for optimum performance.

Overview

The on-chip clock recovery circuit consists of a digital frequency-locked loop and a phase-locked loop, which extract the clock from the positive going edges of the input data. This recovered clock is used with the input data in the retimer section to synchronize the output data (DOUT) with the positive edge of the clock output (CLKOUT).

To ensure accurate frequency selection, the T7033 Clock Recovery Circuit uses an external 3.58-MHz crystal in its oscillator reference section. The operating frequency of the device is then determined by the circuit's seven frequency select pins, which are made high (5 V) or low (0 V). (See Table 2.) Special care is required for filtering the 5 V supply (VDD) on pin 15 (QVDD) since voltage variations on this pin may cause excessive jitter on the clock and data outputs.

DIN and LDIN are equivalent inputs. Typically, LDIN is used for the data loopback mode of system operation. For normal operation, TESTC (pin 18) and TESTF (pin 17) must be tied to 5 V. These pins are used only for testing during manufacture.

There are six octave selections that can be chosen from the frequency band selections in Table 2. Nine frequency bands can be selected from each octave. For optimal performance, a frequency of operation that is within the bands set by the seven frequency select pins must be selected.

Noise Properties

Noisy data under worst-case conditions produces a small eye opening and a large amount of phase jitter on the data input. Under these conditions, the T7033 Clock Recovery Circuit recovers the average clock and retimes the data, reducing jitter. Figures 3 and 4 illustrate the improvement of data quality through the circuit. At the limit of sensitivity, the clock recovery circuit imposes a typical noise penalty (noise factor) of < 1 dB.

Table 2. Frequency Band Selections (MHz)

M2	M1	M0	L2	L1	L0	N	Frequency Min	Frequency Max
Octave 6								
0	0	0	0	0	0	1	46.3626	51.2715
0	0	0	0	0	1	0	41.9403	46.3626
0	0	0	0	0	1	1	38.5908	41.9403
0	0	0	0	1	0	0	35.4895	38.5908
0	0	0	0	1	0	1	33.0611	35.4895
0	0	0	0	1	1	0	30.7495	33.0611
0	0	0	0	1	1	1	28.9096	30.7495
0	0	0	1	0	0	0	27.1293	28.9096
0	0	0	1	0	0	1	24.8300	27.1293
Octave 5								
0	0	1	0	0	0	1	23.1720	25.6254
0	0	1	0	0	1	0	20.9617	23.1720
0	0	1	0	0	1	1	19.2876	20.9617
0	0	1	0	1	0	0	17.7376	19.2876
0	0	1	0	1	0	1	16.5239	17.7376
0	0	1	0	1	1	0	15.3685	16.5239
0	0	1	0	1	1	1	14.4490	15.3685
0	0	1	1	0	0	0	13.5592	14.4490
0	0	1	1	0	0	1	12.4100	13.5592
Octave 4								
0	1	0	0	0	0	1	11.5766	12.8024
0	1	0	0	0	1	0	10.4724	11.5766
0	1	0	0	0	1	1	9.6360	10.4724
0	1	0	0	1	0	0	8.8617	9.6360
0	1	0	0	1	0	1	8.2553	8.8617
0	1	0	0	1	1	0	7.6781	8.2553
0	1	0	0	1	1	1	7.2187	7.6781
0	1	0	1	0	0	0	6.7741	7.2187
0	1	0	1	0	0	1	6.2000	6.7741

Table 2. Frequency Band Selections (MHz) (Continued)

M2	M1	M0	L2	L1	L0	N	Frequency	
							Min	Max
Octave 3								
0	1	1	0	0	0	1	5.7883	6.4012
0	1	1	0	0	1	0	5.2362	5.7883
0	1	1	0	0	1	1	4.8180	5.2362
0	1	1	0	1	0	0	4.4308	4.8180
0	1	1	0	1	0	1	4.1276	4.4308
0	1	1	0	1	1	0	3.8390	4.1276
0	1	1	0	1	1	1	3.6093	3.8390
0	1	1	1	0	0	0	3.3871	3.6093
0	1	1	1	0	0	1	3.1000	3.3871
Octave 2								
1	0	0	0	0	0	1	2.8942	3.2006
1	0	0	0	0	1	0	2.6181	2.8942
1	0	0	0	0	1	1	2.4090	2.6181
1	0	0	0	1	0	0	2.2154	2.4090
1	0	0	0	1	0	1	2.0638	2.2154
1	0	0	0	1	1	0	1.9195	2.0638
1	0	0	0	1	1	1	1.8047	1.9195
1	0	0	1	0	0	0	1.6935	1.8047
1	0	0	1	0	0	1	1.5500	1.6935
Octave 1								
1	0	1	0	0	0	1	1.4564	1.6106
1	0	1	0	0	1	0	1.3175	1.4564
1	0	1	0	0	1	1	1.2123	1.3175
1	0	1	0	1	0	0	1.1149	1.2123
1	0	1	0	1	0	1	1.0386	1.1149
1	0	1	0	1	1	0	0.9660	1.0386
1	0	1	0	1	1	1	0.9082	0.9660
1	0	1	1	0	0	0	0.8522	0.9082
1	0	1	1	0	0	1	0.7800	0.8522

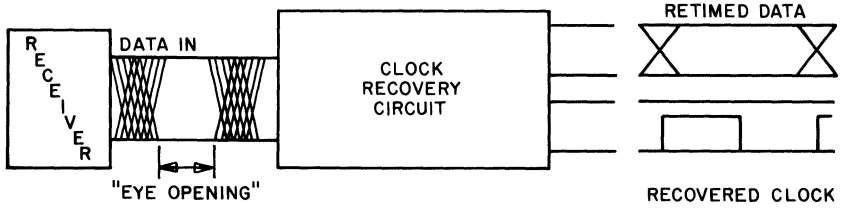


Figure 3. Clock Recovery with Noisy Data

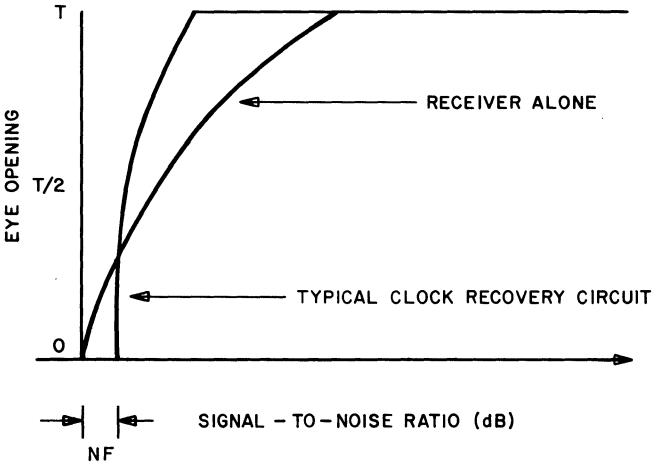


Figure 4. Eye-Opening Versus Signal-to-Noise Ratio

Characteristics

A circuit board ground plane is required for optimum performance.

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit
Output voltage:				
I_{OL} = 4 mA	V_{OL}	—	0.4	V
I_{OH} = –0.4 mA	V_{OH}	2.4	—	V
Output current high	I_{OS}	–25.0	—	mA
Power supply current drain	I_{DD}	—	60	mA
Input voltages DIN, LDIN, LSEL:				
low	V_{IL}	—	0.8	V
high	V_{IH}	2.0	—	V
All other inputs:				
low	V_{IL}	—	0.5	V
high	V_{IH}	4.5	—	V
Noise factor* (see Figure 4)	NF	—	1	dB

* Measured at typical conditions of V_{DD} = 5 V, 25 °C, 50 Mb/s at 1 x 10^{-9} BER with a data pattern of $2^{23} - 1$.

Maximum Ratings

DC supply voltage (V_{DD}) ..... 6 V
Short-circuit output current (I_{OS}) ..... −100 mA
Power dissipation (PD) ..... 0.5 W
Storage temperature (Tstg) range ..... −40 to +125 °C
Lead soldering temperature and time ..... 240 °C/10 s

Maximum ratings are defined as the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External Reference Crystal Requirements

Frequency: 3.579545-MHz ± 0.05%, 0 to 70 °C
Series resistance: 150-Ω, maximum

Calibrated at 16-pF series capacitance

Timing Characteristics

Parameter	Min	Max	Unit
Data input rise time	—	5	ns
Data output transition*	—	5	ns
Data output jitter**	0	7	°rms
Clock skew (relative to data output)	−3	0	ns

* Transition time is in terms of 10% and 90% values.
** Jitter is in terms of the 50% value for 1010... data input.

Timing Diagram

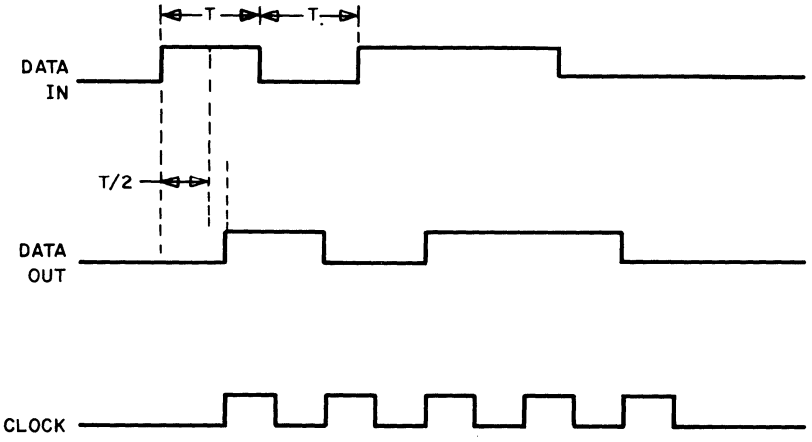


Figure 5. Timing Waveforms

T7034 Clock Recovery Circuit

Features

- Pin-programmable for 25-MHz to 50-MHz operation
- Fiber and wire applications
- Single 5 V supply
- Only one external component required: 3.58-MHz crystal

Description

The T7034 Clock Recovery Circuit integrated circuit operates over a 25-MHz to 50-MHz frequency range and provides clock recovery and data retiming. The device accepts TTL-NRZ data from a receiver (optical or electrical), recovers the clock, and retimes the data to the recovered clock. The inputs and outputs are TTL-compatible and the circuit requires a single 5 V supply. The T7034 Clock Recovery Circuit is manufactured using CMOS technology and is available in a 300-mil, 20-pin plastic DIP. The device is designed for general-purpose clock recovery and retiming applications.

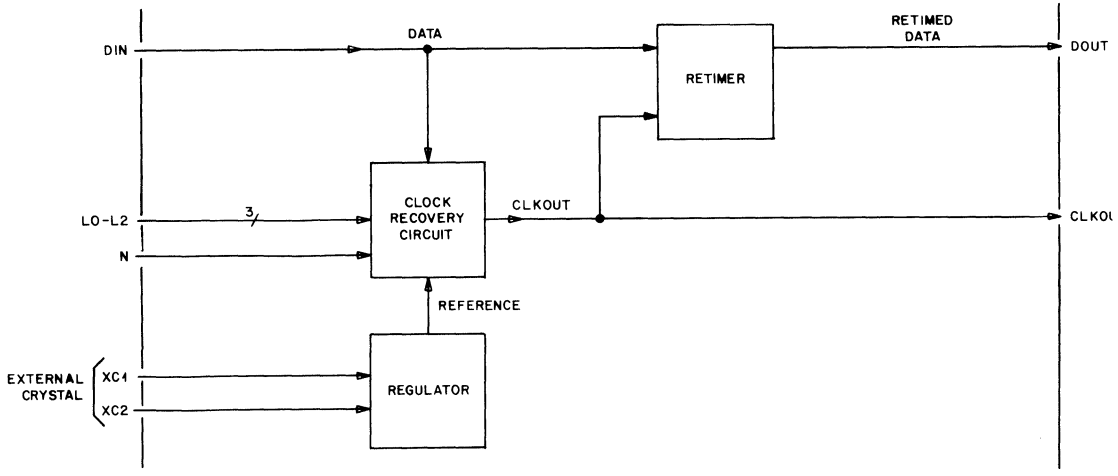
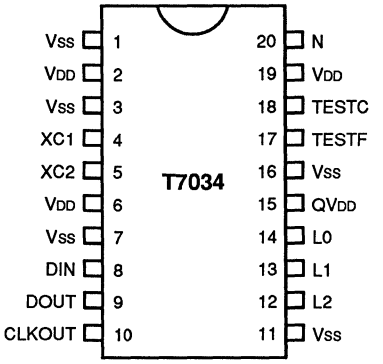


Figure 1. Block Diagram

User Information

Pin Descriptions



Symbol	Pin	Symbol	Pin
CLKOUT	10	VDD	2
DIN	8	VDD	6
DOUT	9	VDD	19
L0	14	VSS	1
L1	13	VSS	3
L2	12	VSS	7
N	20	VSS	11
QVDD	15	VSS	16
TESTC	18	XC1	4
TESTF	17	XC2	5

Figure 2. Pin Function Diagram and Alphabetical Listing of Symbols

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1	VSS	—	**Ground.** 0 V.
2	VDD	—	**5 V Supply.**
3	VSS	—	**Ground.** 0 V.
4	XC1	I	**XTAL1.** Connect a 3.579545-MHz crystal to this pin or an external reference clock.
5	XC2	I	**XTAL2.** Connect a 3.579545-MHz crystal to this pin.
6	VDD	—	**5 V Supply.**
7	VSS	—	**Ground.** 0 V.
8	DIN	I	**Data In.**
9	DOUT	O	**Data Out.**
10	CLKOUT	O	**Clock Out.**
11	VSS	—	**Ground.** 0 V.
12 13 14	L2 L1 L0	I	**Frequency Selects.** These pins, with pin 20, set the operating frequency range of the circuit. See Table 2 for frequency band selection.
15	QVDD	—	**Quiet VDD 5 V Supply.** The required filtering can be supplied with a 5-Ω to 20-Ω resistor connected to VDD (pin 19) and a 0.1-μF capacitor connected to ground.
16	VSS	—	**Ground.** 0 V.
17	TESTF	I	**Test F Pin.** Used for manufacturing test purposes; should be tied to 5 V for normal operation.

Note: A circuit board ground plane is required for optimum performance.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
18	TESTC	I	**Test C Pin.** Used for manufacturing test purposes; should be tied to 5 V for normal operation.
19	VDD	—	**5 V Supply.**
20	N	I	**Frequency Select.** This pin, with pins 12—14, sets the operating frequency range of the circuit. See Table 2 for frequency band selection.

Note: A circuit board ground plane is required for optimum performance.

Overview

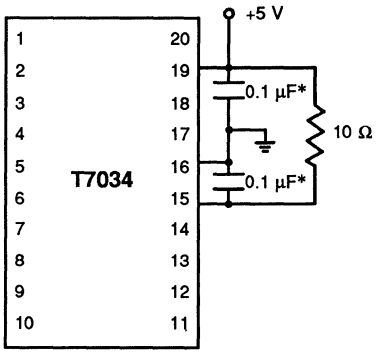
The on-chip clock recovery circuit consists of a digital frequency-locked loop and a phase-locked loop, which extract the clock from the positive going edges of the input data. This recovered clock is used with the input data in the retimer section to synchronize the output data (DOUT) with the positive edge of the clock output (CLKOUT).

To ensure accurate frequency selection, connect a 3.58-MHz crystal or an external TTL reference frequency (fREF) to the clock recovery circuit. The operating frequency of the device is then determined by the circuit's four frequency select pins, which are made high (5 V) or low (0 V). (See Table 2.) Special care is required for filtering the 5 V supply (VDD) on pin 15 (QVDD) since voltage variations on this pin may cause excessive jitter on the clock and data outputs (see Figure 3).

For normal operation, pin 18 (TESTC) and pin 17 (TESTF) must be tied to 5 V. These pins are used only for testing during manufacture.

Table 2. Frequency Band Selections (MHz)

				Frequency	
L2	L1	L0	N	Min	Max
fREF = 3.58 MHz					
0	0	0	1	46.3626	51.2715
0	0	1	0	41.9403	46.3626
0	0	1	1	38.5908	41.9403
0	1	0	0	35.4895	38.5908
0	1	0	1	33.0611	35.4895
0	1	1	0	30.7495	33.0611
0	1	1	1	28.9096	30.7495
1	0	0	0	27.1293	28.9096
1	0	0	1	24.8300	27.1293
fREF = 4.096 MHz					
0	0	1	0	47.98	53.04
0	0	1	1	44.15	47.98
0	1	0	0	40.59	44.15
0	1	0	1	37.82	40.59
0	1	1	0	35.18	37.82
0	1	1	1	33.06	35.18
1	0	0	0	31.02	33.06
1	0	0	1	28.40	31.02



* Place all filter capacitors as close as possible to pins.

Figure 3. Recommended Filtering of VDD and QVDD

Noise Properties

Noisy data under worst-case conditions produces a small eye opening and a large amount of phase jitter on the data input. Under these conditions, the clock recovery circuit recovers the average clock and retimes the data, reducing jitter. Figures 4 and 5 illustrate the improvement of data quality through the circuit. At the limit of sensitivity, the clock recovery circuit imposes a typical noise penalty (noise factor) of < 1 dB.

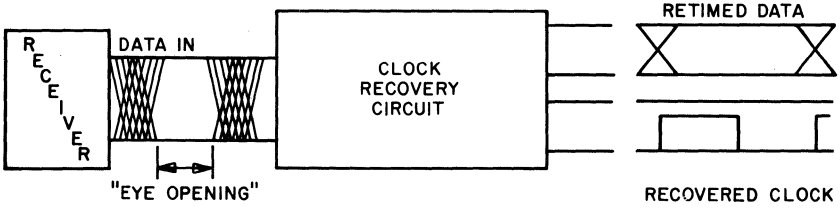


Figure 4. Clock Recovery with Noisy Data

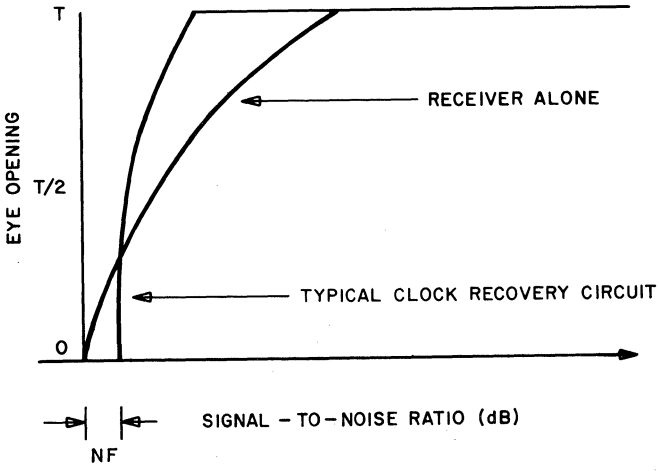


Figure 5. Eye-Opening Versus Increasing Signal-to-Noise Ratio

Characteristics

A circuit board ground plane is required for optimum performance.

Electrical Characteristics

T_A = 0 to 70 °C, V_{DD} = 5 V ± 5%, V_{SS} = 0 V

Parameter	Symbol	Min	Max	Unit
Output voltage:				
I_{OL} = 4 mA	V_{OL}	—	0.4	V
I_{OH} = –0.4 mA	V_{OH}	2.4	—	V
Output current high	I_{OS}	–25	—	mA
Power supply current drain	I_{DD}	—	60	mA
Input voltages, DIN, LDIN, LSEL:				
low	V_{IL}	—	0.8	V
high	V_{IH}	2.0	—	V
All other inputs:				
low	V_{IL}	—	0.5	V
high	V_{IH}	4.5	—	V
Noise factor* (see Figure 5)	NF	—	1	dB

* Measured at typical conditions of V_{DD} = 5 V, 25 °C, 50 Mb/s at 1 x 10^{-9} BER with a data pattern of $2^{23} - 1$.

Maximum Ratings

DC supply voltage (V_{DD}) ..... 6 V
Short-circuit output current (I_{OS}) ..... –100 mA
Power dissipation (PD) ..... 0.5 W
Storage temperature (Tstg) range ..... –40 to +125 °C
Lead soldering temperature and time ..... 240 °C/10 s

Maximum ratings are defined as the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

External Reference Crystal Requirements

Frequency: 3.579545 MHz ± 0.05%, 0 to 70 °C
Series resistance: 150 Ω, maximum

Calibrated at 16-pF series capacitance

Timing Characteristics

Parameter	Min	Max	Unit
Data input rise time	—	5	ns
Data output transition*	—	5	ns
Data output jitter	0	5	°rms
Clock skew (relative to data output)	–3	0	ns

* Transition time is in terms of 10% and 90% values.

Timing Diagram

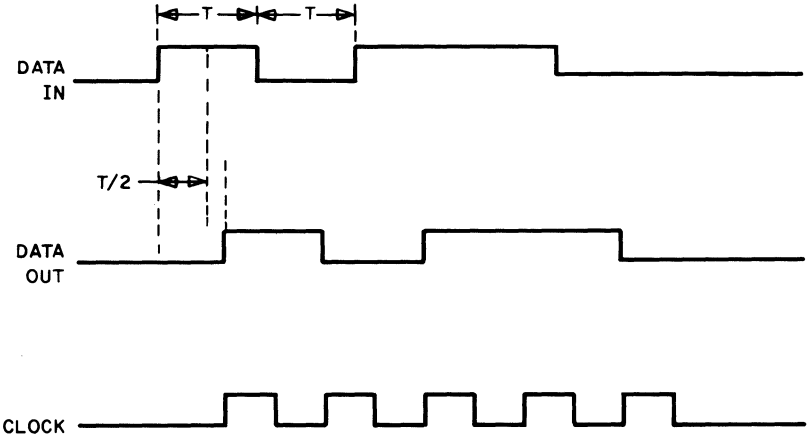


Figure 6. Timing Waveforms

WE DSP16 Digital Signal Processor

Features

- Low-power CMOS technology
- 55-ns and 75-ns instruction cycle parts available
- Military version available
- 16- X 16-bit multiplication and 36-bit accumulation in one instruction cycle
- Two 36-bit accumulators
- Instruction cache for high-speed, ROM-efficient, repetitive operations
- 2048-word ROM, 512-word RAM (on-chip)
- Off-chip ROM expansion to 64K-word
- Serial and parallel I/O ports with multi-processor capability
- Maskable interrupts
- Single 5 V power supply
- Supported by *WE* DSP16-SL Support Software Library and *WE* DSP16-DS Digital Signal Processor Development System

Description

The *WE* DSP16 Digital Signal Processor is a 16-bit high-speed programmable integrated circuit fabricated in low-power CMOS technology. The standard DSP16 device described in this data sheet is packaged in an 84-pin plastic leaded chip carrier. A military version of the DSP16 device is available in a square 133-pin ceramic pin-grid-array package and is described in a separate data sheet. The DSP16 device is a general-purpose building block that can be programmed to perform a wide variety of signal processing functions. It achieves high throughput without programming restrictions or latencies due to its parallel pipelined architecture. The processor has an arithmetic unit capable of a 16 X 16-bit multiplication and 36-bit accumulation or a 32-bit ALU operation in one instruction cycle. Data is supplied by two independent addressing units. The DSP16 device can function in a stand-alone manner, requiring only an external clock.

User Information

Architectural Summary

The DSP16 device contains a data arithmetic unit (DAU) that performs signal processing arithmetic, a ROM address arithmetic unit (XAAU), a RAM address arithmetic unit (YAAU), a 2048 X 16-bit ROM that contains program instructions and fixed data, a 512 X 16-bit RAM for variable data, an instruction cache (CACHE), a serial I/O unit (SIO), and a 16-bit parallel I/O unit (PIO).

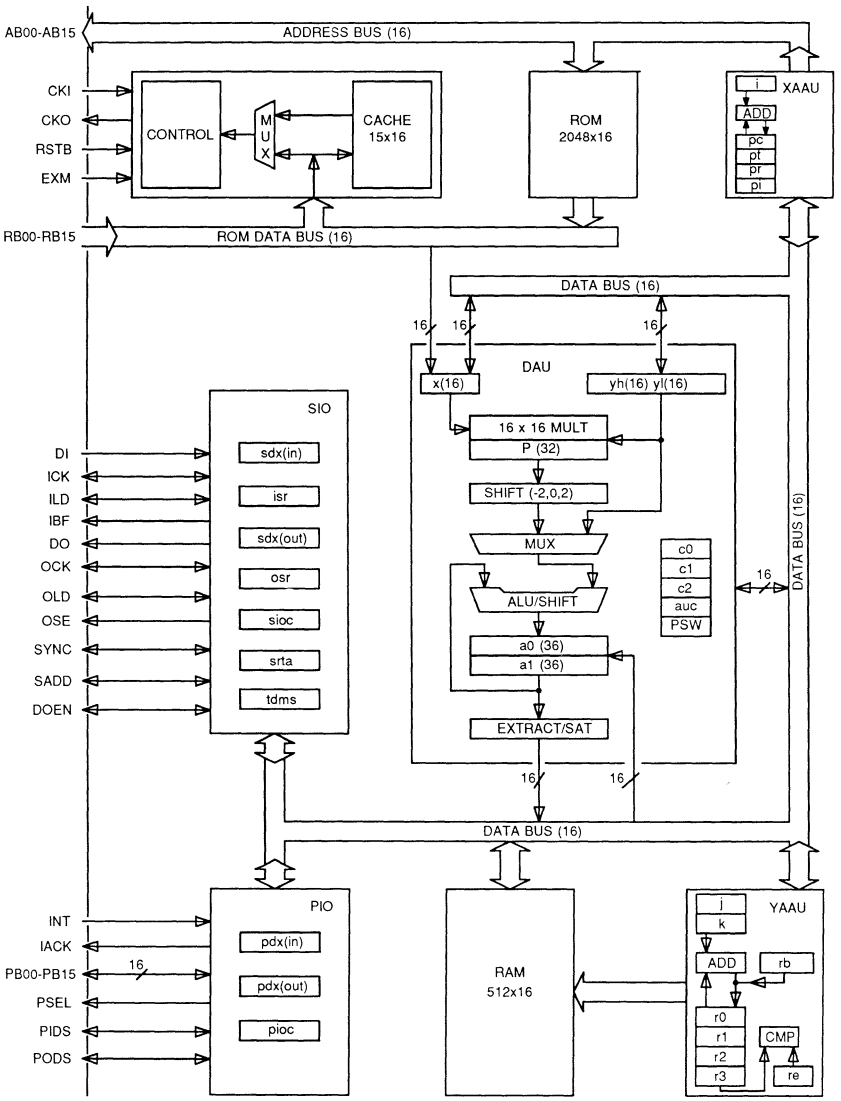
The arithmetic unit contains a 16- X 16-bit parallel multiplier that generates a full 32-bit product in one instruction cycle. The product can be accumulated with one of two 36-bit accumulators. The data in these accumulators can be directly loaded from or stored to memory in two 16-bit words with automatic saturation on overflow. The ALU supports a full set of arithmetic and logical operations on either 16- or 32-bit data. A standard set of ALU conditions can be tested for conditional ALU operations, branches, and subroutine calls. This procedure allows the processor to perform as a powerful 16- or 32-bit microprocessor for logical and control applications.

Two addressing units support high-speed, register-indirect, memory addressing with postmodification of the register. Direct and immediate addressing is supported at the cost of only one additional instruction cycle and ROM location. Four address registers in the YAAU (r0—r3) can be used for either read or write addresses to the RAM without restrictions. Registers j and k provide user-defined post-increments for the addresses. Fixed increments of +1, −1, and +2 are also available. The YAAU also supports a flexible modulo addressing mode for efficient filter implementations. Registers rb and re are used to define the beginning and end of the modulo. Four compound addressing modes are provided to make read/write operations more efficient. In the XAAU, the register pt is used for ROM table look-up, and register i is used to hold a user-defined post-increment. A fixed post-increment of +1 is also available. Register pc is the program counter. Registers pr and pi hold the return address for subroutine calls and interrupts, respectively.

The on-chip memory includes 2048 X 16-bit words of ROM and 512 X 16-bit words of RAM. The ROM can be replaced with up to 64K 16-bit words of external memory for prototyping or for applications that require a large program space or frequent modification.

An on-chip memory cache can be selectively used to store such repetitive operations as those found in a filter section. Up to 15 words in the cache can be repeated up to 127 times with no looping overhead. In addition, operations in the cache that require a ROM access (for example, reading fixed coefficients) execute at twice the normal rate. The cache greatly reduces the need for writing repetitive code in-line and, therefore, conserves ROM storage.

The DSP16 device has both serial and parallel I/O ports. The serial I/O unit is an asynchronous, full duplex, double-buffered channel operating at up to 10 Mbits/s that easily interfaces with other DSP16 devices in a multiple DSP16 environment. Commercially available codecs and time division multiplex (TDM) channels can be interfaced to the DSP16 device with few (if any) additional components. The parallel I/O unit is capable of interfacing to a 16-bit bus containing other DSP16 devices, microprocessors, or peripheral I/O devices. Data rates of up to 18.2 Mbytes/s are obtainable through this port.



Note: See Table 15 for signal name definitions.

Figure 1. Block Diagram

Legend:

16 x 16 Mult	16-bit by 16-bit Multiplier
a0—a1	Accumulators 0—1
ADD	Adder
ALU/SHIFT	Arithmetic Logic Unit/Shifter
auc	Arithmetic Unit Control
c0—c2	Counters 0—2
CMP	Comparator
DAU	Data Arithmetic Unit
i	Increment Register
isr	Input Shift Register
j	Increment Register
k	Increment Register
MUX	Multiplexer
osr	Output Shift Register
p	Product Register
pc	Program Counter
pdx(in)	Parallel I/O Data Transmit Input Register
pdx(out)	Parallel I/O Data Transmit Output Register
pi	Program Interrupt Register
PIO	Parallel I/O Unit
pioc	Parallel I/O Control Register
pr	Program Return Register
psw	Processor Status Word
pt	ROM Table Pointer
r0—r3	RAM Pointer Register 0—3
RAM	Read/Write Memory
rb	Modulo Addressing Register
re	Modulo Addressing Register
ROM	Read-Only Memory
sdx(in)	Serial Data Transmit Input Register
sdx(out)	Serial Data Transmit Output Register
SIO	Serial I/O Unit
sioc	Serial I/O Control Register
srta	Serial Receive/Transmit Address Register
tdms	Serial I/O Time-Division Multiplex Signal Control Register
x	Multiplier Input Register
XAAU	ROM Address Arithmetic Unit
YAAU	Ram Address Arithmetic Unit
yh	y(High) DAU Register
yl	y(Low) DAU Register

The DSP16 device has a maskable interrupt that can be generated by the user or by any of four I/O conditions: input buffer full (IBF), output buffer empty (OBE), parallel input data strobe (PIDS), and parallel output data strobe (PODS).

Note: Branch instructions and cache operations are protected from interrupts.

Instruction Set

The DSP16 processor has five types of instructions: multiply/ALU, special function, control, cache, and data move. The multiply/ALU instructions are the primary instructions used to implement signal processing algorithms. Statements from this group can be combined to generate multiply/accumulate, logical, and other ALU functions and to transfer data between memory and registers in the data arithmetic unit. The special function instructions can be conditionally executed based on flags from the previous ALU operation, the condition of one of the counters, or the value of a randomly set bit in the DSP16 device. The control instructions implement the goto and call commands. Control instructions can also be executed conditionally. Cache instructions are used to implement low-overhead loops, conserve program memory, and decrease the execution time of certain multiply/ALU instructions. Data move instructions are used to transfer data between memory and registers or between accumulators and registers.

The following operators are used in describing the instruction set:

*	16- X 16-bit → 32-bit multiplication (Denotes register-indirect addressing when used as a prefix to an address register)
+	36-bit addition
−	36-bit subtraction
>>	Arithmetic right shift
<<	Logical left shift
|	32-bit bitwise OR
&	32-bit bitwise AND
^	32-bit bitwise EXCLUSIVE OR
:	Compound address swapping

To form a valid multiply/ALU instruction, choose one statement each from the function and transfer columns in Table 1. If either statement is not required, a single statement from either column constitutes a valid instruction. The number of cycles to execute the instruction is a function of the transfer column. (An instruction with no transfer statement executes in one instruction cycle.) All multiply/ALU instructions require 1 word of program memory.

Multiply/ALU Instructions

Note that the function statements and transfer statements in Table 1 are chosen independently. Any function statement may be combined with any transfer statement to form a valid Multiply/ALU instruction.

Table 1. Multiply/ALU Instructions

Function Statements	Transfer Statements†	Transfer Cycles Out/In Cache
p=x*y	y=Y x=X	2/1
aD=p p=x*y	y=aT x=X	2/1
aD=aS+p p=x*y	y[l]=Y	1/1
aD=aS-p p=x*y	aT[l]=Y	1/1
aD=p	x=Y	1/1
aD=aS+p	Y	1/1
aD=aS–p	Y=y[l]	2/2
aD=y	Y=aT[l]	2/2
aD=aS+y	Z: y x=X	2/2
aD=aS–y	Z: y[l]	2/2
aD=aS&y	Z: aT[l]	2/2
aD=aS|y		
aD=aS^y		
aS–y		
aS&y		

† Brackets, [ ], indicate an optional argument and are not part of the instruction syntax. The l argument designates the low 16-bits of aT or y.

Table 2. Replacement Table for Multiply/ALU Instructions

Replace	Value†	Meaning
aD aS aT	a0, a1	One of two DAU accumulators.
X	*pt++,*pt++i	ROM location pointed to by pt. pt is postmodified by +1 and i, respectively.
Y	*rM, *rM++, *rM– –, *rM++j	RAM location pointed to by rM (M = 0, 1, 2, 3). rM is postmodified by 0,+1,–1, or j, respectively.
Z	*rMzp, *rMpz, *rMm2, *rMjk	Read/write compound addressing. rM (M = 0, 1, 2, 3) is used twice. First, post-modified by 0, +1, –1, or j, respectively and, second, postmodified by +1, 0, +2, or k, respectively.

† When loading the upper half of a0, a1, or y, the lower half of the register is cleared if the corresponding CLR bit in the AUC register is zero. See the Register Settings section.

Special Function Instructions

All forms of the special function instructions execute in one instruction cycle:

aD=aS>>1 aD=aS>>4 aD=aS>>8 aD=aS>>16	Arithmetic right shift (sign preserved) of 36-bit accumulators
aD=aS	
aD=–aS	
aD=rnd(aS)	– Round upper 20-bits of accumulator
aDh=aSh+1	– Increment upper half of accumulator (lower half cleared)
aD=aS+1	– Increment accumulator
aD=y	
aD=p	
aD=aS<<1 aD=aS<<4 aD=aS<<8 aD=aS<<16	Logical left shift (sign not preserved) of the lower 32 bits of accumulators (upper 4-bits are sign-bit-extended from bit 31 at the completion of the shift)

The above special functions can be conditionally executed

if CON instruction

and with an event counter

ifc CON instruction

which means:

if CON is true then

```
c1=c1+1
instruction
c2=c1
```

else

```
c1=c1+1
```

Table 3. Replacement Table for Special Function Instructions

Replace	Value	Meaning
aD aS	a0, a1	One of two DAU accumulators
CON	mi, pl, eq, ne, gt, le, lvs, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false	See Table 7 for definitions of mnemonics

Control Instructions

All unconditional control instructions execute in 2 instruction cycles and require one word of program memory; conditional control instructions execute in 3 instruction cycles and require two words of program memory.

```
goto JA
goto pt
call JA
call pt
icall
return      (goto  pr)
ireturn     (goto  pi)
```

The above control instructions, with the exception of ireturn and icall can be conditionally executed. For example:

```
If CON goto JA
```

Table 4. Replacement Table for Control Instructions

Replace	Value	Meaning
CON	mi, pl, eq, ne, gt, le, lvs, mvs, mvc, c0ge, c0lt, c1ge, c1lt, heads, tails, true, false	See Table 7 for definitions of mnemonics
JA	12-bit value	Least significant 12 bits of absolute address within the same 4 K-word memory section

Cache Instructions

Cache instructions require 1 word of program memory. The do instruction executes in one instruction cycle; the redo instruction executes in two instruction cycles. The instruction formats are:

```
do K {inst1, instr2, ..., instrN}
redo K
```

Table 5. Replacement Table for Cache Instructions

Replace	Value	Meaning
K	$2 \leq K \leq 127$	Number of times the instructions are to be executed
NI	$1 \leq N \leq 15$	1 to 15 instructions may be included

Data Move Instructions

Data move instructions execute in two instruction cycles, except immediate loads of YAAU registers which execute in one instruction cycle. Immediate YAAU register loads require one word of program memory. Non-YAAU immediate data move instructions require two words of program memory. All other data move instructions require one word. The data move instructions are:

R = N	aT = R
R = M	aD = R
R = Y	Y = R
R = aS	Z : R

Table 6. Replacement Table for Data Move Instructions

Replace	Value*	Meaning**, †
R	x	DAU register – signed, 16 bits
	y	DAU register – signed, 16 bits
	yl	DAU register – unsigned, 16 bits
	auc	DAU control register – unsigned, 7 bits
	c0	DAU counter 0 – signed, 8 bits
	c1	DAU counter 1 – signed, 8 bits
	c2	DAU counter 2 – signed, 8 bits
	r0	YAAU pointer register – unsigned, 9 bits
	r1	YAAU pointer register – unsigned, 9 bits
	r2	YAAU pointer register – unsigned, 9 bits
	r3	YAAU pointer register – unsigned, 9 bits
	rb	YAAU modulo addressing register – unsigned, 9 bits
	re	YAAU modulo addressing register – unsigned, 9 bits
	j	YAAU increment register – signed, 9 bits
	k	YAAU increment register – signed, 9 bits
	pt	XAAU pointer register – unsigned, 16 bits
	pr	XAAU pointer register – unsigned, 16 bits
	pi	XAAU pointer register – unsigned, 16 bits
	i	XAAU increment register – signed, 12 bits
	psw	Processor status word
	sioc	Serial I/O control register
	sdx	Serial I/O data register
	tdms	Serial I/O TDMS control register
	srta	Serial receive/transmit address
	pioc	Parallel I/O control register
	pdx0	Parallel I/O data register with PSEL = 0 (pin 72)
	pdx1	Parallel I/O data register with PSEL = 1 (pin 72)

* sioc, tdms and srta registers are not readable.

** When signed registers less than 16 bits wide are read, their contents are sign-extended to 16 bits. When unsigned registers less than 16 bits wide are read, their contents are zero-extended to 16 bits.

† Loading an accumulator with a data move instruction does not affect the flags.

Table 6. Replacement Table for Data Move Instructions (Continued)

Replace	Value†	Meaning††,§
aD, aS, aT	a0, a1	High half of accumulator
Y	*rM,*rM++, *rM−−,*rM++j	Same as in multiply/ALU instructions
Z	*rmZp,*rMpz, *rMm2,*rMjk	Same as in multiply/ALU instructions
N	16-bit value	Immediate data
M	9-bit value	Immediate data for YAAU registers

† sioc, tdms, and srta registers are not readable.
†† When signed registers less than 16 bits wide are read, their contents are sign-extended to 16 bits.
When unsigned registers less than 16 bits wide are read, their contents are zero-extended to 16 bits.
§ Loading an accumulator with a data move instruction does not effect the flags.

Conditional Mnemonics

Table 7 lists mnemonics used for conditional execution of special function and control instructions.

Table 7. DSP16 Conditional Mnemonics

Test	Meaning	Test	Meaning
pl	Result is nonnegative (sign bit is bit 35)	mi	Result is negative
eq	Result is equal to zero	ne	Result is not equal to zero
gt	Result is greater than zero	le	Result is less than or equal to zero
lvs	Logical overflow set*	lvc	Logical overflow clear
mvs	Mathematical overflow set**	mvc	Mathematical overflow clear
c0ge	Counter 0 greater than or equal to zero	c0lt	Counter 0 less than zero
c1ge	Counter 1 greater than or equal to zero	c1lt	Counter 1 less than zero
heads	Pseudorandom sequence bit set	tails	Pseudorandom sequence bit clear
true	The condition is always satisfied in an if instruction	false	The condition is never satisfied in an if instruction

* Result is not representable in the 36-bit accumulators.
** Bits 35—31 are not the same.

Register Settings

Tables 8 through 13 show how to set various operating conditions for the DSP16 device.

Note that the following abbreviations are used in the tables:

x = don't care
R = read only
W = read/write

Table 8. Serial I/O Control (SIOC) Register

Bit	9	8	7	6	5	4	3	2	1	0
Field	LD	CLK		MSB	OLD	ILD	OCK	ICK	OLEN	ILEN

Field	Value	Description
LD	0	Active ILD/OLD = ICK ÷ 16, active SYNC = ICK ÷ 128/256*
	1	Active ILD/OLD = OCK ÷ 16, active SYNC = OCK ÷ 128/256*
CLK	0 0	Active clock = CKI ÷ 4
	0 1	Active clock = CKI ÷ 12
	1 0	Active clock = CKI ÷ 16
	1 1	Active clock = CKI ÷ 20
MSB	0	LSB first
	1	MSB first
OLD	0	OLD is an input (passive mode)
	1	OLD is an output (active mode)
ILD	0	ILD is an input (passive mode)
	1	ILD is an output (active mode)
OCK	0	OCK is an input (passive mode)
	1	OCK is an output (active mode)
ICK	0	ICK is an input (passive mode)
	1	ICK is an output (active mode)
OLEN	0	16-bit output
	1	8-bit output
ILEN	0	16-bit input
	1	8-bit input

* See tdms register, SYNC field.

Table 9. Time-Division Multiplex Slot (TDMS) Register

Bit	9	8	7	6	5	4	3	2	1	0
Field	SYNCSP	MODE	TRANSMIT SLOT							SYNC

Field	Value	Description
SYNCSP	0	SYNC = ICK/OCK* ÷ 128**
	1	SYNC = ICK/OCK* ÷ 256
MODE	0	Multiprocessor mode off, DOEN is an input (passive mode)
	1	Multiprocessor mode on, DOEN is an output (active mode)
TRANSMIT SLOT	1xxxxxx	Transmit slot 7
	x1xxxxx	Transmit slot 6
	xx1xxxx	Transmit slot 5
	xxx1xxx	Transmit slot 4
	xxxx1xx	Transmit slot 3
	xxxxx1x	Transmit slot 2
	xxxxxx1	Transmit slot 1
SYNC	1	Transmit slot 0, SYNC is an output (active mode)
	0	SYNC is an input (passive mode)

* See sioc register, LD field.
** Select this mode when in multiprocessor mode.

Table 10. Serial Receive/Transmit Address (SRTA) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	RECEIVE ADDRESS								TRANSMIT ADDRESS							

Field	Value	Description
RECEIVE ADDRESS	1xxxxxxx	Receive address 7
	x1xxxxxx	Receive address 6
	xx1xxxxx	Receive address 5
	xxx1xxxx	Receive address 4
	xxxx1xxx	Receive address 3
	xxxxx1xx	Receive address 2
	xxxxxx1x	Receive address 1
	xxxxxxx1	Receive address 0
TRANSMIT ADDRESS	1xxxxxxx	Transmit address 7
	x1xxxxxx	Transmit address 6
	xx1xxxxx	Transmit address 5
	xxx1xxxx	Transmit address 4
	xxxx1xxx	Transmit address 3
	xxxxx1xx	Transmit address 2
	xxxxxx1x	Transmit address 1
	xxxxxxx1	Transmit address 0

Table 11. Processor Status Word (PSW) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	DAU Flags				X	X	a1[V]	a1[35—32]				a0[V]	a0[35—32]			

Field	Value	Description
DAU Flags	Wxxx	LMI – logical minus when set
	xWxx	LEQ – logical equal when set
	xxWx	LLV – logical overflow when set
	xxxW	LMV – mathematical overflow when set
a1[V]	W	Accumulator 1 (a1) overflow when set
a1[35—32]	Wxxx	Accumulator 1 (a1) bit 35
	xWxx	Accumulator 1 (a1) bit 34
	xxWx	Accumulator 1 (a1) bit 33
	xxxW	Accumulator 1 (a1) bit 32
a0[V]	W	Accumulator 0 (a0) overflow when set
a0[35—32]	Wxxx	Accumulator 0 (a0) bit 35
	xWxx	Accumulator 0 (a0) bit 34
	xxWx	Accumulator 0 (a0) bit 33
	xxxW	Accumulator 0 (a0) bit 32

Table 12. Arithmetic Unit Control (AUC) Register

Bit	6	5	4	3	2	1	0
Field	CLR			SAT		ALIGN	

Field	Value	Description
CLR	1xx	Clearing yl is disabled (enabled when 0)
	x1x	Clearing a1l is disabled (enabled when 0)
	xx1	Clearing a0l is disabled (enabled when 0)
SAT	1x	a1 saturation on overflow is disabled (enabled when 0)
	x1	a0 saturation on overflow is disabled (enabled when 0)
ALIGN	00	p ← (x X y)
	01	p ← (x X y) ÷ 4
	10	p ← (x X y) X 4
	11	Reserved

Table 13. Parallel I/O Control (PIOC) Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	IBF	STROBE		PODS	PIDS	S/C	INTERRUPTS					STATUS				

Field	Value	Description
IBF	R	IBF interrupt status bit (same as bit 4)
STROBE	00 01 10 11	Strobe width of: **PODS PIDS** T* T 2T 2T 3T 3T 4T 4T
PODS	0	PODS is an input (passive mode)
	1	PODS is an output (active mode)
PIDS	0	PIDS is an input (passive mode)
	1	PIDS is an output (active mode)
S/C	0	Not status/control mode
	1	Status/control mode
INTERRUPTS	1xxxx	IBF interrupt enabled (disabled when 0)
	x1xxx	OBE interrupt enabled (disabled when 0)
	xx1xx	PIDS interrupt enabled (disabled when 0)
	xxx1x	PODS interrupt enabled (disabled when 0)
	xxxx1	INT interrupt enabled (disabled when 0)
STATUS	Rxxxx	IBF status bit
	xRxxx	OBE status bit
	xxRxx	PIDS status bit
	xxxRx	PODS status bit
	xxxxR	INT status bit

* T = 2 X tCKIHCKIH. See Figure 3.

Instruction Set Formats

This section defines the hardware-level encoding of the DSP16 device instructions.

Multiply/ALU Instructions

Format 1: Multiply/ALU Read/Write Group:

Field	T					D	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 1a: Multiply/ALU Read/Write Group:

Field	T					$\overline{aT}$	S	F1				X	Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 2: Multiply/ALU Read/Write Group:

Field	T					D	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 2a: Multiply/ALU Read/Write Group:

Field	T					$\overline{aT}$	S	F1				X	Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Special Function Instructions

Format 3: Special Functions

Field	T					D	S	F2				CON				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Control Instructions

Format 4: Branch Direct Group:

Field	T1				JA											
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 5: Branch Indirect Group:

Field	T					B										
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 6: Conditional Branch Qualifier/Software Interrupt (icall):
Note that a branch instruction immediately follows except for a software interrupt (icall).

Field	T					SI						C				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Data Move Instructions

Format 7: Data Move Group:

Field	T					D	R						Y/Z			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 7a: Data Move Group

Field	T					$\overline{aT}$	R					Y			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 8: Data Move (immediate operand - 2 words)

Field	T					D	R					Y			
	Immediate Operand														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Format 9: Short Immediate Group:

Field	T					I	Short Immediate Operand								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Cache Instructions

Format 10: D0 — Redo

Field	T					NI		K							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Field Descriptions

T Field. Specifies the type of instruction.

T	Operation	Format
0000x	goto JA	4
00010	Short imm j, k, rb, re	9
00011	Short imm r0, r1, r2, r3	9
00100	Y=a1 F1	1
00101	Z : aT F1	2a
00110	Y F1	1
00111	aT=Y F1	1a
01000	aT=R	7a
01001	R=a0	7
01010	R=imm	8
01011	R=a1	7
01100	Y=R	7
01101	Z : R	7
01110	Do, redo	10
01111	R=Y	7
1000x	call JA	4
10010	ifc CON F2	3
10011	if CON F2	3
10100	Y=y F1	1
10101	Z : y F1	2
10110	x=Y F1	1
10111	y=Y F1	1
11000	Branch indirect	5
11001	y=a0 x=X F1	1
11010	Cond. branch qualifier	6
11011	y=a1 x=X F1	1
11100	Y=a0 F1	1
11101	Z : y x=X F1	2
11110	Reserved	—
11111	y=Y x=X F1	1

* imm = immediate.

D Field. Specifies a destination accumulator.

D	Register
0	Accumulator 0
1	Accumulator 1

$\overline{aT}$ Field. Specifies transfer accumulator.

$\overline{aT}$	Register
0	Accumulator 1
1	Accumulator 0

S Field. Specifies a source accumulator.

S	Register
0	Accumulator 0
1	Accumulator 1

F1 Field. Specifies the multiply/ALU function.

F1	Operation
0000	aD=p p=x*y
0001	aD=aS+p p=x*y
0010	p=x*y
0011	aD=aS–p p=x*y
0100	aD=p
0101	aD=aS+p
0110	NOP
0111	aD=aS–p
1000	aD=aS|y
1001	aD=aS^y
1010	aS&y
1011	aS–y
1100	aD=y
1101	aD=aS+y
1110	aD=aS&y
1111	aD=aS–y

X Field. Specifies the addressing of ROM data in two-operand multiply/ALU instructions. Specifies the high or low half of an accumulator or the y register in one-operand multiply/ALU instructions.

X	Operation
Two-Operand Multiply/ALU	
0	*pt++
1	*pt++i
One-Operand Multiply/ALU	
0	aTl, yl
1	aTh, yh

Y Field. Specifies the form of register indirect addressing with postmodification.

Y	Operation
0000	*r0
0001	*r0++
0010	*r0––
0011	*r0++j
0100	*r1
0101	*r1++
0110	*r1––
0111	*r1++j
1000	*r2
1001	*r2++
1010	*r2––
1011	*r2++j
1100	*r3
1101	*r3++
1110	*r3––
1111	*r3++j

Z Field. Specifies the form of register indirect compound addressing with postmodification.

Z	Operation
0000	*r0zp
0001	*r0pz
0010	*r0m2
0011	*r0jk
0100	*r1zp
0101	*r1pz
0110	*r1m2
0111	*r1jk
1000	*r2zp
1001	*r2pz
1010	*r2m2
1011	*r2jk
1100	*r3zp
1101	*r3pz
1110	*r3m2
1111	*r3jk

F2 Field. Specifies the special function to be performed.

F2	Operation
0000	aD=aS>>1
0001	aD=aS<<1
0010	aD=aS>>4
0011	aD=aS<<4
0100	aD=aS>>8
0110	aD=aS>>16
0111	aD=aS<<16
1000	aD=p
1001	aDh=aSh+1
1010	Reserved
1011	aD=rnd(aS)
1100	aD=y
1101	aD=aS+1
1110	aD=aS
1111	aD=–aS

C Field. Specifies the condition for special functions and conditional control instructions.

CON	Condition
00000	mi
00001	pl
00010	eq
00011	ne
00100	lvs
00101	lvc
00110	mvs
00111	mvc
01000	heads
01001	tails
01010	c0ge
01011	c0lt
01100	c1ge
01101	c1lt
01110	true
01111	false
10000	gt
10001	le
Other codes	Reserved

B Field. Specifies the type of branch instruction (except software interrupt).

B	Operation
000	return
001	ireturn
010	goto pt
011	call pt
1xx	Reserved

R Field. Specifies the register for data move instructions.

R	Register
000000	r0
000001	r1
000010	r2
000011	r3
000100	j
000101	k
000110	rb
000111	re
001000	pt
001001	pr
001010	pi
001011	i
010000	x
010001	y
010010	yl
010011	auc
010100	psw
010101	c0
010110	c1
010111	c2
011000	sioc
011001	srta
011010	sdx
011011	tdms
011100	pioc
011101	pdx0
011110	pdx1
Other codes	Reserved

I Field. Specifies a register for short immediate data move instructions.

I	Register
00	r0/j
01	r1/k
10	r2/rb
11	r3/re

SI Field. Specifies when the conditional branch qualifier instruction should be interpreted as a software interrupt instruction.

SI	Operation
0	Not a software interrupt
1	Software interrupt

NI Field. Number of instructions to be loaded into the cache. Zero implies redo operation.

K Field. Number of times the NI instructions in cache are to be executed.

JA Field. 12-bit jump address.

Pin Descriptions

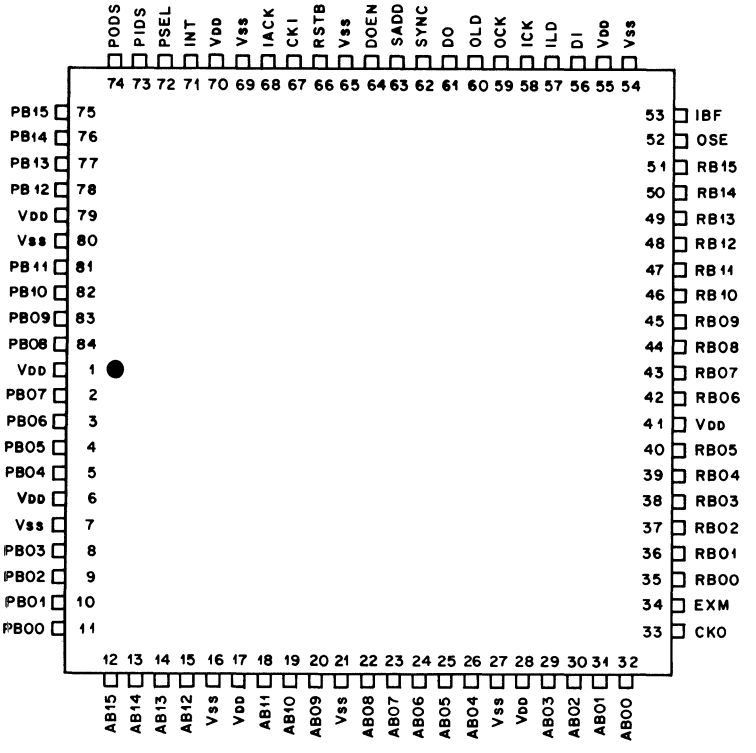


Figure 2. Pin Diagram

Table 14. Pin Names

Symbol	Pin	Symbol	Pin
AB00—AB15	32—29, 26—22, 20—18, 15—12	OLD	60
		OSE	52
CKI	67	PB00—PB15	11—8, 5—2, 84—81, 78—75
CKO	33		
DI	56		
DO	61	PIDS	73
DOEN	64	PODS	74
EXM	34	PSEL	72
IACK	68	RB00—RB15	35—40, 42—51
IBF	53	RSTB	66
ICK	58	SADD	63
ILD	57	SYNC	62
INT	71	VDD	1, 6, 17, 28, 41, 55, 70, 79
OCK	59	VSS	7, 16, 21, 27, 54, 65, 69, 80

In the following table, I = input, O = output, and P = power.

Table 15. Pin Descriptions

Pin	Symbol	Type	Name/Description
1	V_{DD}	P	**5 V Supply.**
2	PB07	I/O*	**Parallel I/O Data Bus — Bit 7.**
3	PB06	I/O*	**Parallel I/O Data Bus — Bit 6.**
4	PB05	I/O*	**Parallel I/O Data Bus — Bit 5.**
5	PB04	I/O*	**Parallel I/O Data Bus — Bit 4.**
6	V_{DD}	P	**5 V Supply.**
7	V_{SS}	P	**Ground.**
8	PB03	I/O*	**Parallel I/O Data Bus — Bit 3.**
9	PB02	I/O*	**Parallel I/O Data Bus — Bit 2.**
10	PB01	I/O*	**Parallel I/O Data Bus — Bit 1.**
11	PB00	I/O*	**Parallel I/O Data Bus — Bit 0.**
12	AB15	O*	**ROM Address Bus — Bit 15.**
13	AB14	O*	**ROM Address Bus — Bit 14.**
14	AB13	O*	**ROM Address Bus — Bit 13.**
15	AB12	O*	**ROM Address Bus — Bit 12.**
16	V_{SS}	P	**Ground.**
17	V_{DD}	P	**5 V Supply.**
18	AB11	O*	**ROM Address Bus — Bit 11.**
19	AB10	O*	**ROM Address Bus — Bit 10.**
20	AB09	O*	**ROM Address Bus — Bit 9.**
21	V_{SS}	P	**Ground.**
22	AB08	O*	**ROM Address Bus — Bit 8.**
23	AB07	O*	**ROM Address Bus — Bit 7.**
24	AB06	O*	**ROM Address Bus — Bit 6.**
25	AB05	O*	**ROM Address Bus — Bit 5.**
26	AB04	O*	**ROM Address Bus — Bit 4.**
27	V_{SS}	P	**Ground.**
28	V_{DD}	P	**5 V Supply.**
29	AB03	O*	**ROM Address Bus — Bit 3.**
30	AB02	O*	**ROM Address Bus — Bit 2.**
31	AB01	O*	**ROM Address Bus — Bit 1.**
32	AB00	O*	**ROM Address Bus — Bit 0.**
33	CKO	O*	**Clock Out.** Buffered clock at half the frequency of CKI.
34	EXM	I	**External Memory.** When low, forces use of internal ROM only for instructions and coefficients. If EXM is high, instructions and coefficients are fetched from external ROM via RB00—RB15 (internal ROM disabled).

* Indicates 3-state condition.

Table 15. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Description
35	RB00	I	**ROM Data Bus — Bit 0.**
36	RB01	I	**ROM Data Bus — Bit 1.**
37	RB02	I	**ROM Data Bus — Bit 2.**
38	RB03	I	**ROM Data Bus — Bit 3.**
39	RB04	I	**ROM Data Bus — Bit 4.**
40	RB05	I	**ROM Data Bus — Bit 5.**
41	V_{DD}	P	**5 V Supply.**
42	RB06	I	**ROM Data Bus — Bit 6.**
43	RB07	I	**ROM Data Bus — Bit 7.**
44	RB08	I	**ROM Data Bus — Bit 8.**
45	RB09	I	**ROM Data Bus — Bit 9.**
46	RB10	I	**ROM Data Bus — Bit 10.**
47	RB11	I	**ROM Data Bus — Bit 11.**
48	RB12	I	**ROM Data Bus — Bit 12.**
49	RB13	I	**ROM Data Bus — Bit 13.**
50	RB14	I	**ROM Data Bus — Bit 14.**
51	RB15	I	**ROM Data Bus — Bit 15.**
52	OSE	O*	**Output Shift Register Empty.** Indicates the end of a serial transmission. OSE is set either by the emptying of the output shift register or by asserting RSTB. OSE is reset by the DSP16 writing a word (two clock cycles after the falling edge of OLD) to the output shift register. If no new word is written by the DSP16, OSE remains high regardless of activity on OLD.
53	IBF	O*	**Input Buffer Full.** IBF is asserted when the input buffer is filled and negated by a read of the buffer. IBF is also negated by asserting RSTB.
54	V_{SS}	P	**Ground.**
55	V_{DD}	P	**5 V Supply.**
56	DI	I	**Data Input.** Serial PCM data latched on rising edge of ICK, either LSB or MSB first, according to the sioc register MSB field.
57	ILD	I/O*	**Input Load.** Falling edge of ILD indicates the beginning of a serial input word. In active mode, ILD is an output; in passive mode, ILD is an input, according to the sioc register ILD field.
58	ICK	I/O*	**Input Clock.** Clock for serial PCM input data. In active mode, ICK is an output; in passive mode, ICK is an input, according to the sioc ICK field.
59	OCK	I/O*	**Output Clock.** Clock for serial PCM output data. In active mode, OCK is an output; in passive mode, OCK is an input, according to the sioc register OCK field.

* Indicates 3-state condition.

Table 15. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Description
60	OLD	I/O*	**Output Load.** Clock for loading the parallel-to-serial converter from the output buffer (obuf). A falling edge of OLD indicates the beginning of a serial output word. In active mode, OLD is an output; in passive mode, OLD is an input, according to the sioc register OLD field.
61	DO	O*	**Data Output.** Serial PCM data output from the output shift register (osr), either LSB or MSB first, according to the sioc register MSB field. DO changes on the rising edges of OCK. DO is 3-stated when DOEN is high.
62	SYNC	I/O*	**Multiprocessor Synchronization.** Typically used in the multiprocessor mode. A falling edge of SYNC indicates the first word of a TDM I/O stream and causes the resynchronization of the active ILD and OLD generators. SYNC is an output when the tdms register SYNC field is set; otherwise, it is an input. SYNC must be tied low if it is not used as an output. When used as an output, SYNC = ILD/OLD ÷ 8 or 16, depending on the setting of the SYNCSP field of the tdms register. This procedure can be used to generate a slow clock for SIO operation.
63	SADD	I/O*	**Serial Address.** An 8-bit serial bit stream typically used for addressing during multiprocessor communication between multiple DSP16 devices. In multiprocessor mode, SADD is an output when the tdms time slot dictates a serial transmission; otherwise, it is an input. SADD is always an output when not in multiprocessor mode. SADD is 3-stated when DOEN is high.
64	DOEN	I/O*	**Data Output Enable (Active Low).** An input when not in the multiprocessor mode. DO and SADD are enabled only if DOEN is low. DOEN is an output when in the multiprocessor mode (tdms register MODE field set). In the multiprocessor mode, DOEN indicates a valid time slot for a serial output.
65	V_{SS}	P	**Ground.**
66	RSTB	I	**Reset.** A high-to-low transition causes entry into the reset state. The sioc, pioc, tdms, rb, and re register bits are cleared. Reset clears external flags IACK and IBF and sets external flag OSE. DAU condition flags and the DAUC register are not affected by reset. All output and bidirectional pins are 3-stated during reset. A low-to-high transition causes execution to begin at ROM location 0.

* Indicates 3-state condition.

Table 15. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Description
67	CKI	I	**Clock In.** Input clock at twice the frequency of internal operations.
68	IACK	O*	**Interrupt Acknowledge.** Interrupt acknowledge signals when an interrupt is being serviced by the DSP16. The IACK remains high until normal instruction operation resumes.
69	VSS	P	**Ground.**
70	VDD	P	**5 V Supply.**
71	INT	I	**Processor Interrupt.** Interrupt to DSP16. INT is acknowledged when the interrupt is enabled by the PIOC register.
72	PSEL	O*	**Peripheral Select.** PSEL is used to specify the logical port to/from which data is to be conveyed. In active mode, PSEL is high (logic 1) when pdx1 is the register specified in the I/O instruction and low when pdx0 is the register specified. PSEL has no meaning when the device is in passive mode.
73	PIDS	I/O*	**Parallel Input Data Strobe (Active low).** In active mode, PIDS is an output. When PIDS is asserted, data may be placed onto the PDB. Upon negation of PIDS, data should be removed from the PDB. PIDS is asserted by the DSP16 device during an active mode read transaction. In passive mode, PIDS is an input. When asserted by an external device, this signal indicates that data is available on the PDB. In both active and passive modes, the trailing edge (low-to-high transition) of PIDS is the sampling point.
74	PODS	I/O*	**Parallel Output Data Strobe (Active low).** In active mode, PODS is an output. When PODS is asserted, data is available on the PDB. PODS is asserted by the DSP16 device during an active mode write transaction. In passive mode, PODS is an input. When PODS is asserted by an external device, the DSP16 device places the contents of its parallel output register (pdx0 or pdx1) onto the PDB.
75	PB15	I/O*	**Parallel I/O Data Bus — Bit 15.**
76	PB14	I/O*	**Parallel I/O Data Bus — Bit 14.**
77	PB13	I/O*	**Parallel I/O Data Bus — Bit 13.**
78	PB12	I/O*	**Parallel I/O Data Bus — Bit 12.**
79	VDD	P	**5 V Supply.**
80	VSS	P	**Ground.**
81	PB11	I/O*	**Parallel I/O Data Bus — Bit 11.**
82	PB10	I/O*	**Parallel I/O Data Bus — Bit 10.**
83	PB09	I/O*	**Parallel I/O Data Bus — Bit 9.**
84	PB08	I/O*	**Parallel I/O Data Bus — Bit 8.**

* Indicates 3-state condition.

Characteristics

Electrical Characteristics

The parameters below are valid for the following conditions: T_C = 0 to 85 °C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, T = 2 X tCKIHCKIH (see Figure 3).

Parameter	Sym	75 ns		55 ns		Unit
		Min	Max	Min	Max	
Input voltage:						
low	V_{IL}	—	0.8	—	0.8	V
high	V_{IH}	2.0	—	2.0	—	V
Output voltage:						
low (I_{OL} = 2.0 mA)	V_{OL}	—	0.4	—	0.4	V
high (I_{OH} = –2.0 mA)	V_{OH}	2.4	—	2.4	—	V
Output current:						
low (V_{OL} = 0.4 V)	I_{OL}	—	2.0	—	2.0	mA
high (V_{OH} = 2.4 V)	I_{OH}	—	–2.0	—	–2.0	mA
Output short circuit current						
V_{OH} = 0 V	I_{OS}	—	–200	—	–200	mA
Output 3-state current:						
high (V_{IH} = 2.0)	I_{OZH}	–75	75	–75	75	μA
low (V_{IL} = 0.8)	I_{OZL}	–75	75	–75	75	μA
Input current:						
high (V_{IH} = 5.5; V_{DD} = 5.5)	I_{IH}	—	25	—	25	μA
low (V_{IL} = 0, V_{SS} = 0)	I_{IL}	—	–25	—	–25	μA
Power supply current						
V_{DD} = 5.5 V	I_{DD}	—	64	—	82	mA
Power dissipation						
V_{DD} = 5.5 V	PD	—	350	—	450	mW
Input capacitance	C_I	—	15	—	15	pF

Maximum Ratings

Voltage range on any pin with respect to ground ..... –0.5 to +6 V
Power dissipation ..... 1 W
Ambient temperature range ..... –40 to +120 °C
Storage temperature range ..... –65 to +150 °C

Maximum ratings are the limiting conditions that can be applied to all variations of circuit and environmental conditions without the occurrence of permanent damage.

External leads can be bonded and soldered safely at temperatures of up to 300 °C.

Chip current in the input buffers is highly dependent on input voltage level. Essentially no DC current is drawn at full CMOS levels but, for levels near the threshold of 1.4 V, high and unstable levels can flow. The table below gives the I_{DD} input buffer current for 43 inputs biased at DC level, V_{IN}. The worst case power assumes 100 mW dissipated by the input buffers. Inputs are protected against electrostatic discharge (ESD) damage with diodes connected to V_{DD} and V_{SS}. Input voltage should not be greater than V_{DD} + 0.5 V or less than V_{SS} – 0.5 V. The power dissipation listed is for unloaded outputs. Total power dissipation can be calculated on the basis of the application by adding $C \cdot V_{DD}^2 \cdot f$ for each output, where C is the load capacitance and f is the output frequency.

IDD Input Buffer Current Versus VIN

VIN (V)	5.0	3.6	2.8	2.4	2.0	1.4	0.8	0.4	0
IDD (ma)	<.2	2.7	28.	36.	36.	*	16.	1.3	<.2

* High and unstable.

Timing Characteristics and Requirements

Timing characteristics refer to the behavior of the device under specified conditions. Timing requirements refer to conditions imposed on the user for proper operation of the device. All timing data is valid for the following conditions unless otherwise specified: TC = 0 to 85 °C, VDD = 5 V ± 10%, VSS = 0 V, T = 2 X tCKIHCKIH, capacitance load on outputs = 50 pF.

External Memory and Clocks

Table 16. Timing Requirements for External ROM and Clocks (See Figure 3)

Description	Symbol	75 ns		55 ns		Unit
		Min	Max	Min	Max	
Clock in period	tCKIHCKIH	37.5	1000	27.5	1000	ns
Clock in low time	tCKILCKIH	15	—	10	—	ns
Clock in high time	tCKIHCKIL	15	—	10	—	ns
External memory set-up	tRBVCKOL	20	—	20	—	ns
External memory hold	tCKOLRBX	0	—	0	—	ns

Table 17. Timing Characteristics for External ROM and Clocks (See Figure 3)

Description	Symbol	75 ns		55 ns		Unit
		Min	Max	Min	Max	
Clock out high delay	tCKIHCKOH	—	20	—	20	ns
Clock out low delay	tCKIHCKOL	—	20	—	20	ns
Address delay time	tCKOLABV	—	5	—	5	ns
Address hold time	tCKOLABX	0	—	0	—	ns

Reset and Interrupts

Table 18. Timing Requirements for Reset and Interrupts (See Figure 4)

Description	Symbol	Min	Max	Unit
RSTB low time	tRSTBLRSTBH	6T	—	ns
INT hold time	tIACKHINTL	0	2T	ns
INT assertion time	tINTHINTL	2T	—	ns

Table 19. Timing Characteristics for Reset and Interrupts
(See Figure 4)

Description	Symbol	Min	Max	Unit
RSTB disable time	tRSTBHOUTZ	—	100	ns
RSTB enable time	tRSTBHOUTV	—	100	ns

Serial I/O (SIO)

Table 20. Timing Requirements for Serial Inputs
(See Figure 5)

Description	Symbol	Min	Max	Unit
Clock period	tICKHICKH	.1	—	μs
Clock low time	tICKLICKH	.040	—	μs
Clock high time	tICKHICKL	.040	—	μs
Load high set-up	tILDHICKH	15	—	ns
Load low set-up	tILDLICKH	15	—	ns
Load high hold	tICKHILDH	0	—	ns
Load low hold	tICKHILDL	0	—	ns
Data set-up	tDIVICKH	12	—	ns
Data hold	tICKHDIX	0	—	ns

Table 21. Timing Characteristics for Serial Input
(See Figure 5)

Description	Symbol	Min	Max	Unit
IBF delay	tICKHIBFH	—	45	ns

Table 22. Timing Requirements for Serial Output
(See Figures 6 and 7)

Description	Symbol	Min	Max	Unit
Clock period	tOCKHOCKH	.1	—	μs
Clock low time	tOCKLOCKH	.040	—	μs
Clock high time	tOCKHOCKL	.040	—	μs
Load high set-up	tOLDHOCKH	15	—	ns
Load low set-up	tOLDLOCKH	15	—	ns
Load high hold	tOCKHOLDH	0	—	ns
Load low hold	tOCKHOLDL	0	—	ns

Table 23. Timing Characteristics for Serial Output*
(See Figures 6 and 7)

Description	Symbol	Min	Max	Unit
Data delay	tOCKHDOV	—	35	ns
Enable data delay	tDOENLDOV	—	35	ns
Disable data delay	tDOENHDOZ	—	35	ns
Data hold	tOCKHDOX	5	—	ns
OSE delay	tOCKHOSEH	—	45	ns
Address delay	tOCKHSADDV	—	35	ns
Address hold	tOCKHSADDX	5	—	ns
Enable delay	tDOENLSADDV	—	35	ns
Disable delay	tDOENHSADDZ	—	35	ns

* Capacitance load on OCK and DO: 100 pF.

Clock Generation (Active Mode)

Table 24. Timing Characteristics for Clock Generation
(See Figures 5—7)

Description	Symbol	Min	Max	Unit
ICK duty cycle	tICKDC	45	55	%
OCK duty cycle	tOCKDC	45	55	%
ILD duty cycle	tILDDC	49.9	50.1	%
OLD duty cycle	tOLDDC	49.9	50.1	%
ILD delay	tICKHILDH tICKHILDL	—	45	ns
OLD delay	tOCKHOLDH tOCKHOLDL	—	45	ns
SYNC duty cycle	tSYNCDC	49.98	50.02	%
SYNC delay	tOCKHSYNCL tOCKHSYNCH	—	35	ns

Multiprocessor Communication

All serial I/O timing requirements and characteristics (except DOEN characteristics) still apply.

Table 25. Timing Requirements for Multiprocessor Communication (See Figure 8)

Description	Symbol	Min	Max	Unit
SYNC set-up	tSYNCHOCKH tSYNCLOCKH	40	—	ns
SYNC hold	tOCKHSYNCH tOCKHSYNCL	0	—	ns
Address set-up	tSADDVOCKH	12	—	ns
Address hold	tOCKHSADDX	0	—	ns

Table 26. Timing Characteristics for Multiprocessor Communication (See Figure 8)

Description	Symbol*	Min	Max	Unit
Data delay (bit 0 only)	tOCKLDOV	—	33	ns
Data disable delay	tOCKHDOZ	—	40	ns
Data hold	tOCKHDOX	5	—	ns
Data delay	tOCKHDOV	—	35	ns
DO valid delay	tOCKHDOENL	—	35	ns
Address delay (bit 0 only)	tOCKLSADDV	—	33	ns
Address disable delay	tOCKHSADDZ	—	40	ns
Address delay	tOCKHSADDV	—	35	ns
Address hold	tOCKHSADDX	5	—	ns
SYNC delay	tOCKHSYNCL tOCKHSYNCH	—	35	ns
SYNC duty cycle	tSYNCDC	49.98	50.02	%

* Capacitance load on ICK, OCK, DO, SYNC, and SADD: 100 pF.
tICKHICKH and tOCKHOCKH are tCKIHCKIH X 4, 12, 16, or 20. See sioc register.
tILDHILDH and tOLDHOLDH are (tICKHICKH or tOCKHOCKH) X 16. See sioc register.
tSYNCHSYNCH is (tICKHICKH or tOCKHOCKH) X (128 or 256). See tdms register.

Parallel I/O (PIO)

Table 27. Timing Requirements for PIO (See Figures 9—13)

Description	Symbol	Min	Max	Unit
PB set-up time	tPDBVPIDSH	15	—	ns
PB hold time	tPIDSHPDBX	0	—	ns
Passive strobe width (read)	tPIDSLPIDSH	T	—	ns
Passive strobe width (write)	tPODSLPODSH	T	—	ns
PODS high between writes	tPODSHPODSL	T	—	ns

Table 28. Timing Characteristics for PIO (See Figures 9—13)

Description	Symbol	Min*				Max	Unit
		00	01	10	11		
PIDS pulse width	tPIDSLPIDSH	T	2T	3T	4T	—	ns
PODS pulse width	tPODSLPODSH	T	2T	3T	4T	—	ns
PSEL hold time PODS	tPODSHPSELX	0	T/2	T/2	T/2	—	ns
PODS high to PIDS low	tPODSHPODSL	20				—	ns
PIDS high to PODS low	tPIDSHPODSL	T				—	ns
PSEL valid before PODS	tPSELVPODSL	T/2 – 10				—	ns
PB hold time	tPODSHPDBX	10				—	ns
PIDS low to PSEL valid	tPIDSLPSELV	—				10	ns
PSEL hold time PIDS	tPIDSHPSELX	25				—	ns
PIDS high (interaccess)	tPIDSHPIDSL	20				—	ns
Data valid after PODS	tPODSLPDBV	—				25	ns

* The pulse widths of PIDS and PODS for those timing specifications having multiple entries under the minimum value column are determined by bits 14 and 13 of the pioc register. See Table 13.

Timing Diagrams

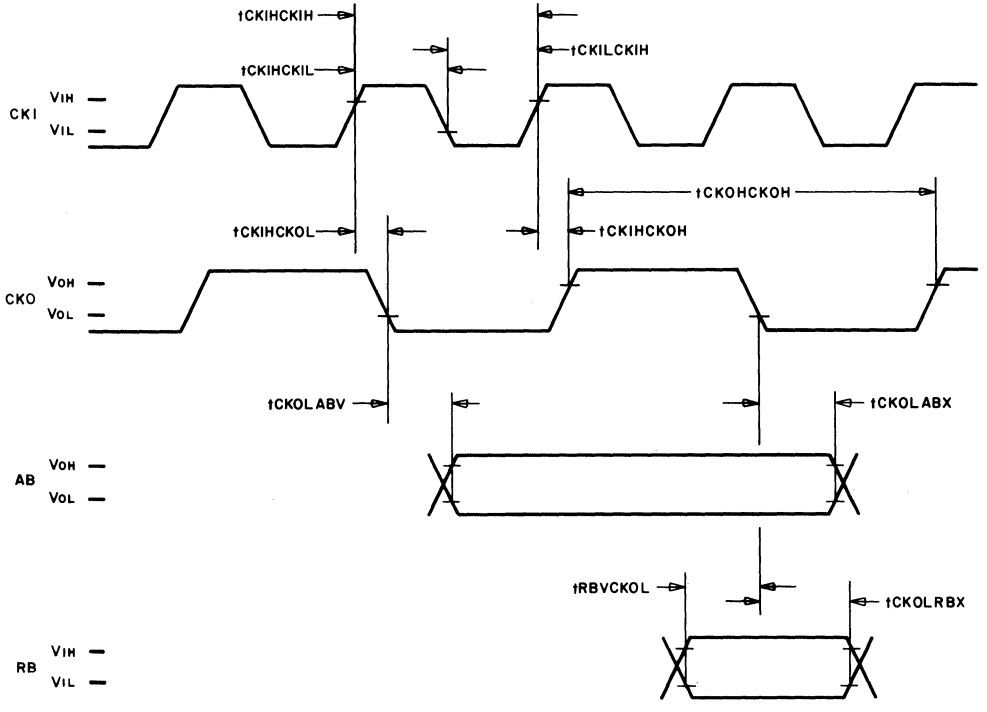
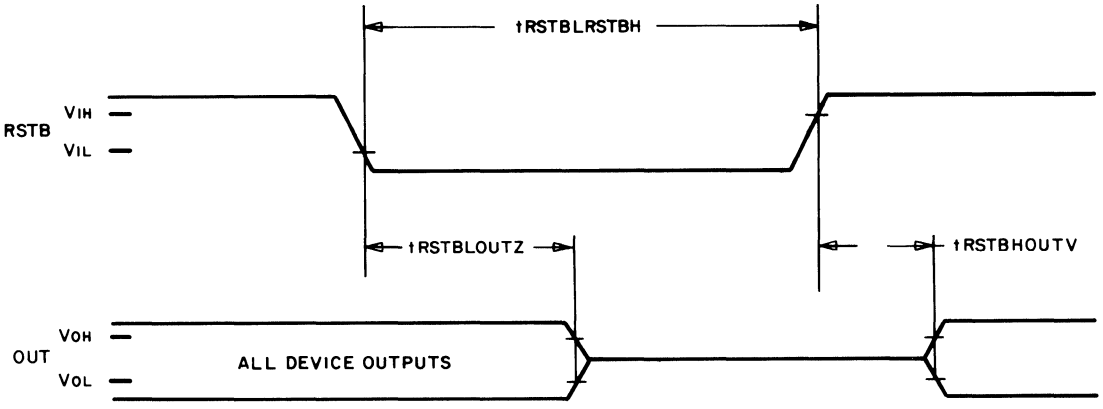
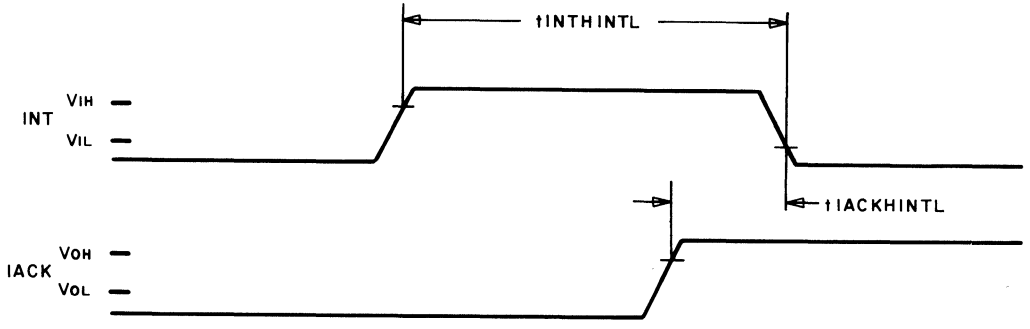


Figure 3. External Memory Interface



A. Reset Timing



B. Interrupt Timing

Figure 4. Reset and Interrupt Timing

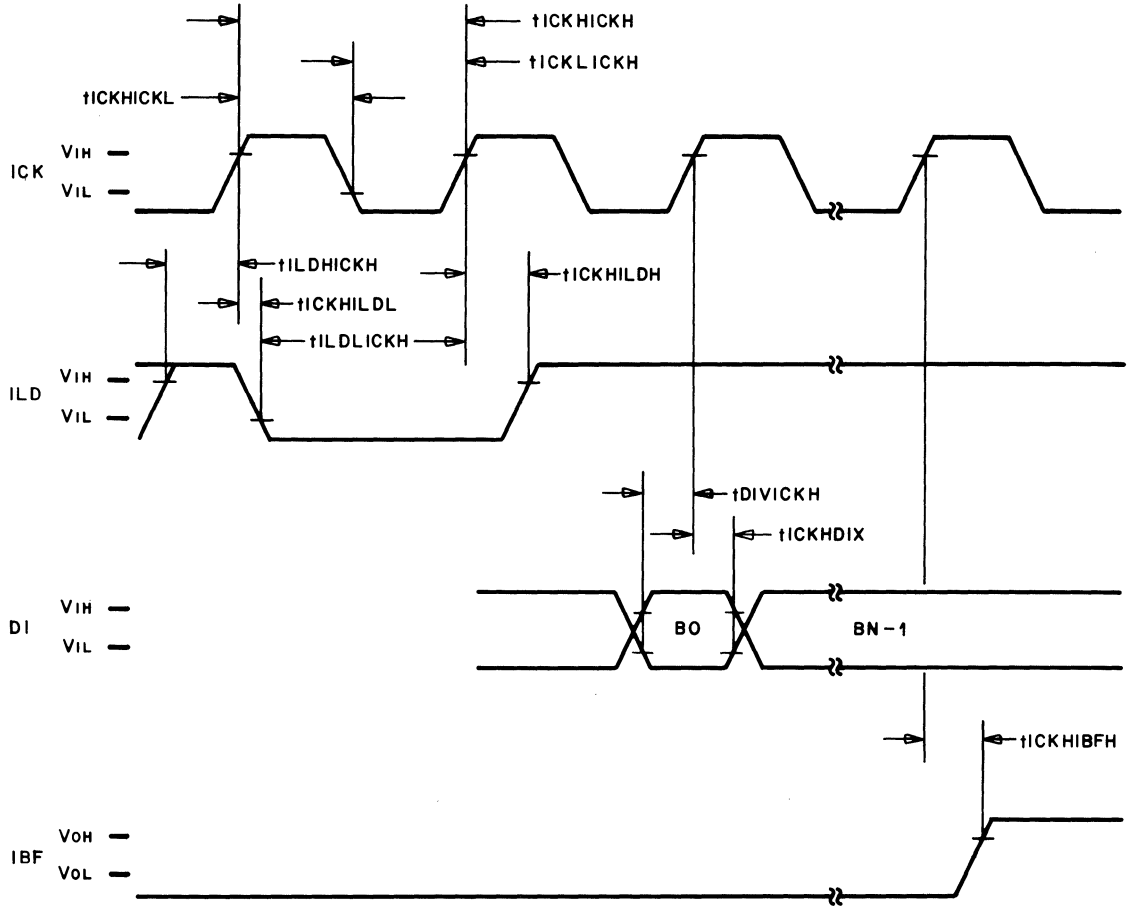


Figure 5. Serial Input Timing

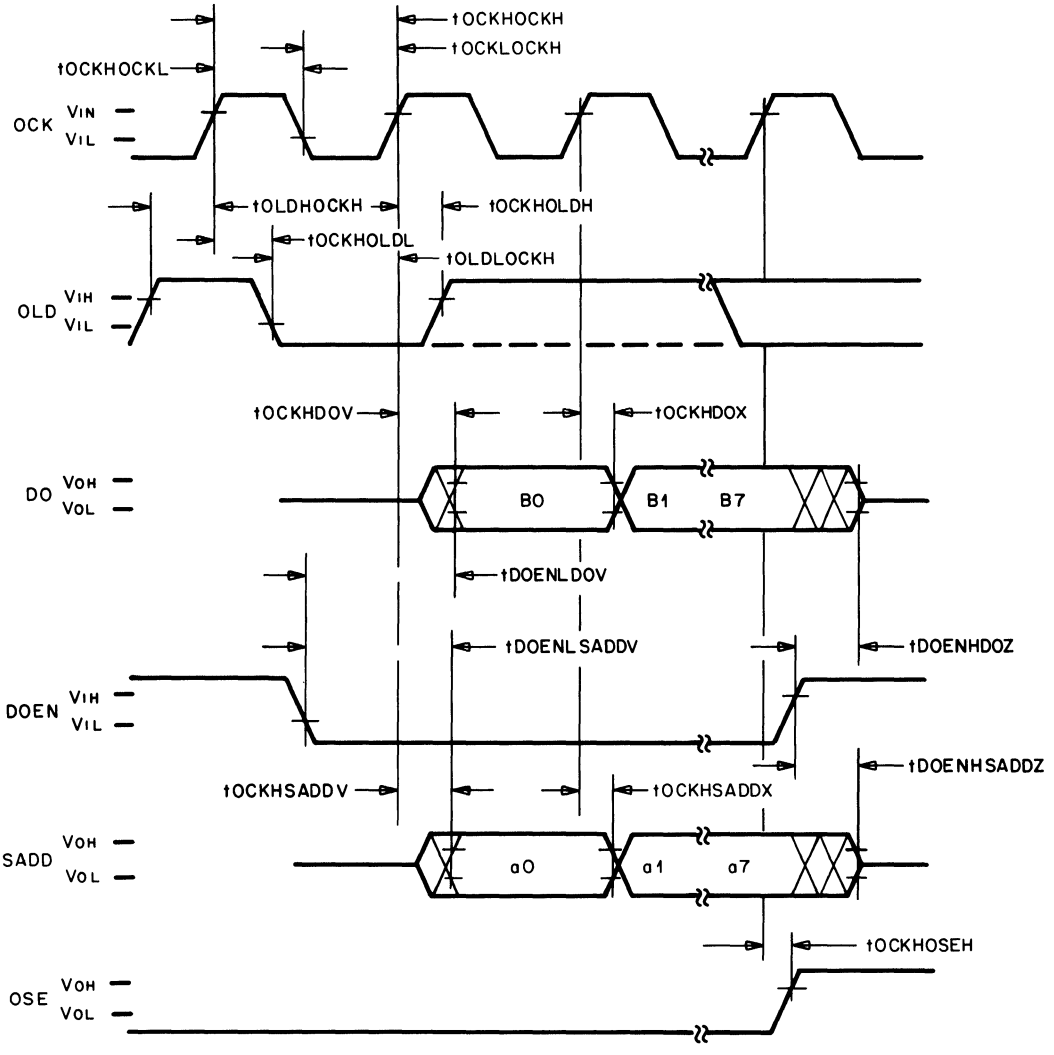


Figure 6. Serial Output Timing — 8 Bits

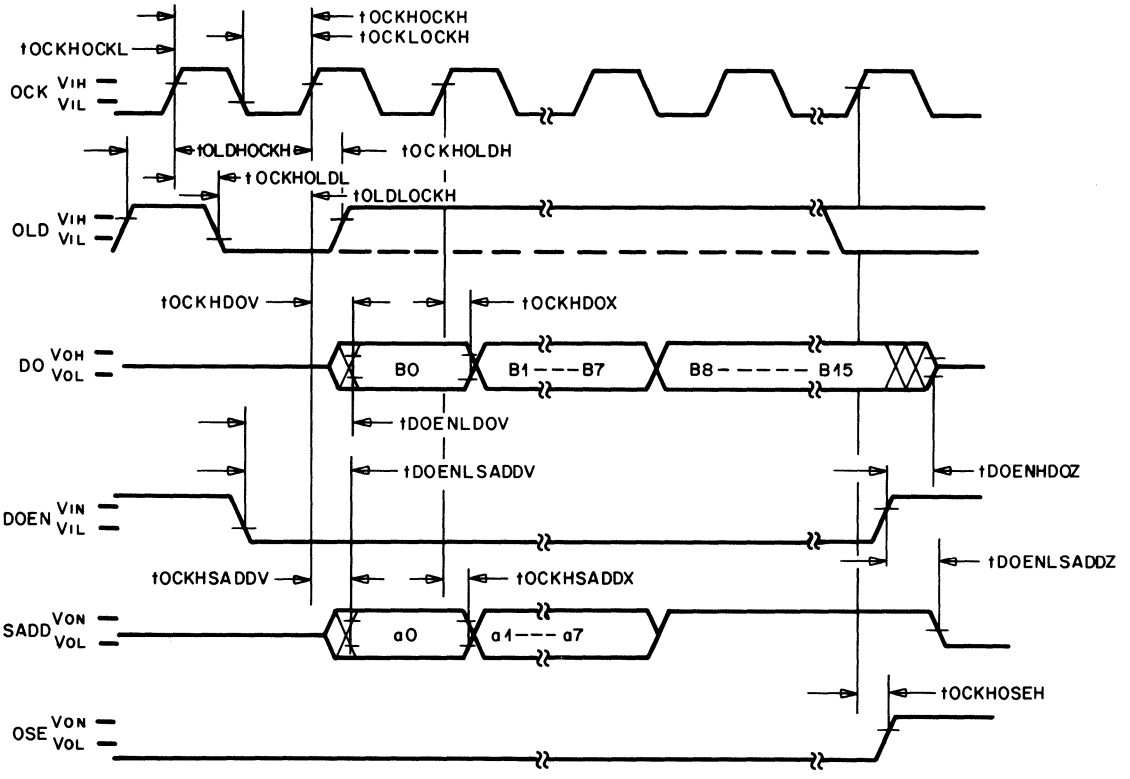
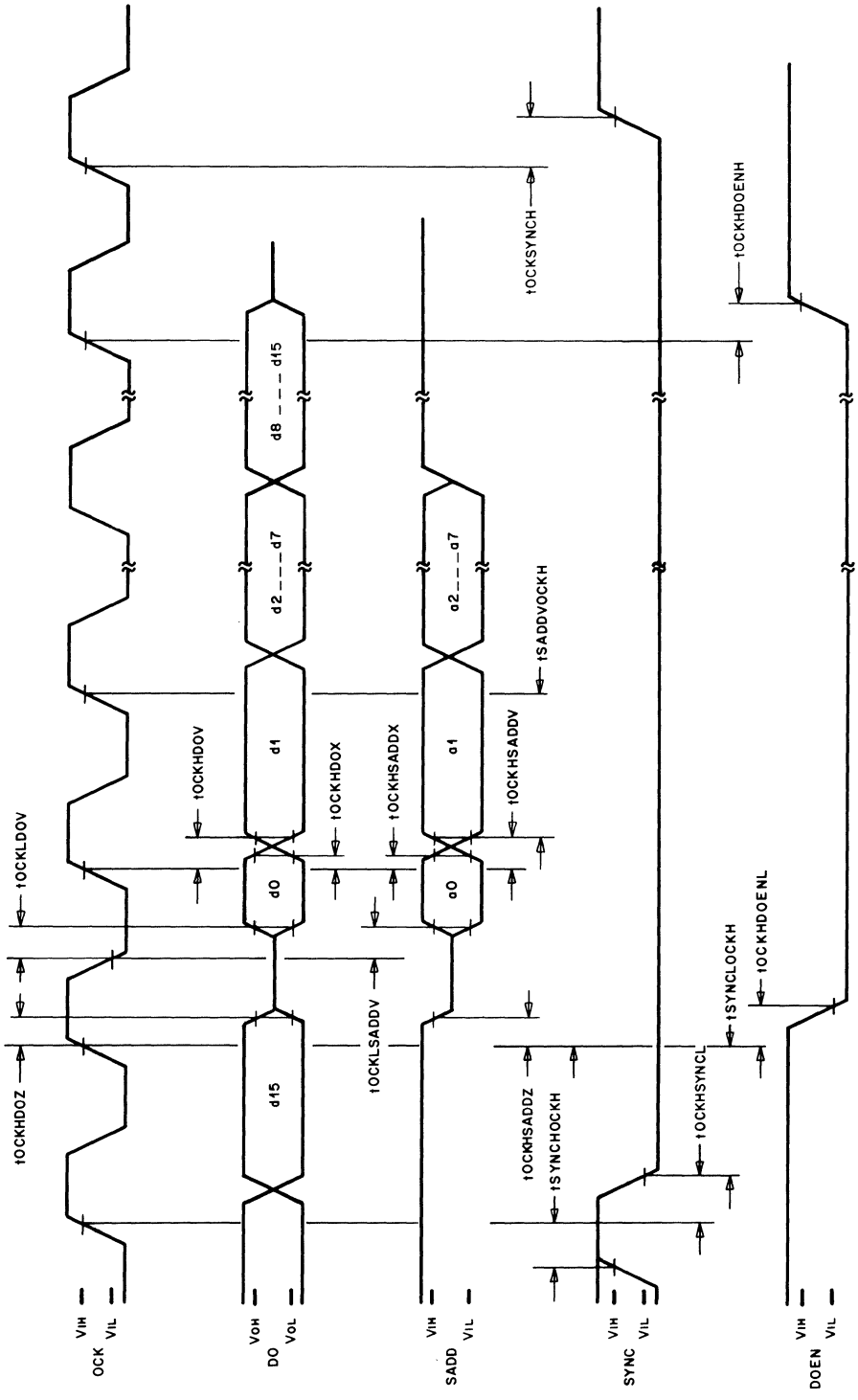


Figure 7. Serial Output Timing — 16 Bits



Note: Sioc register, LD field must be set for multiprocessor operation

Figure 8. Multiprocessor Timing

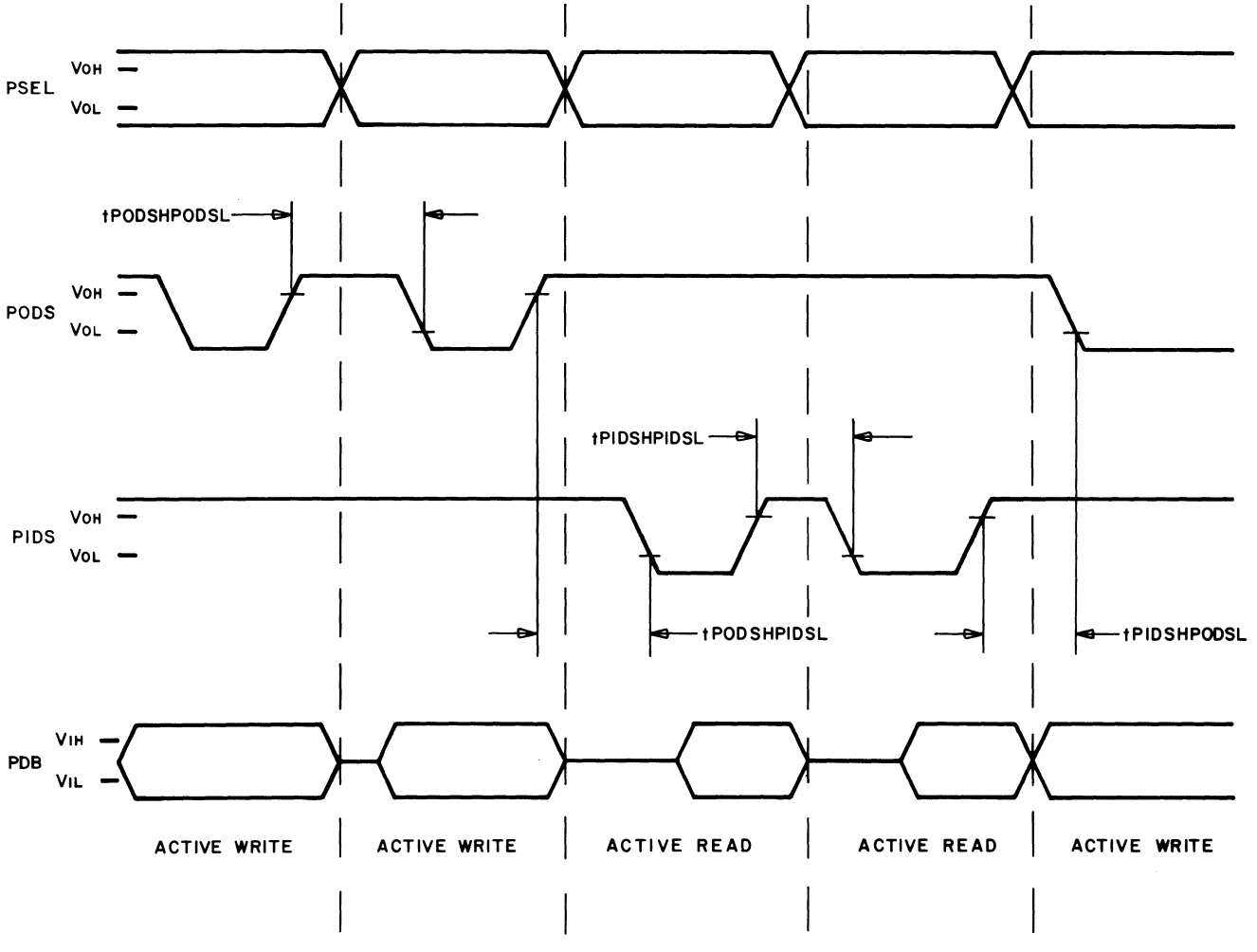


Figure 9. Parallel I/O Interaccess Timing

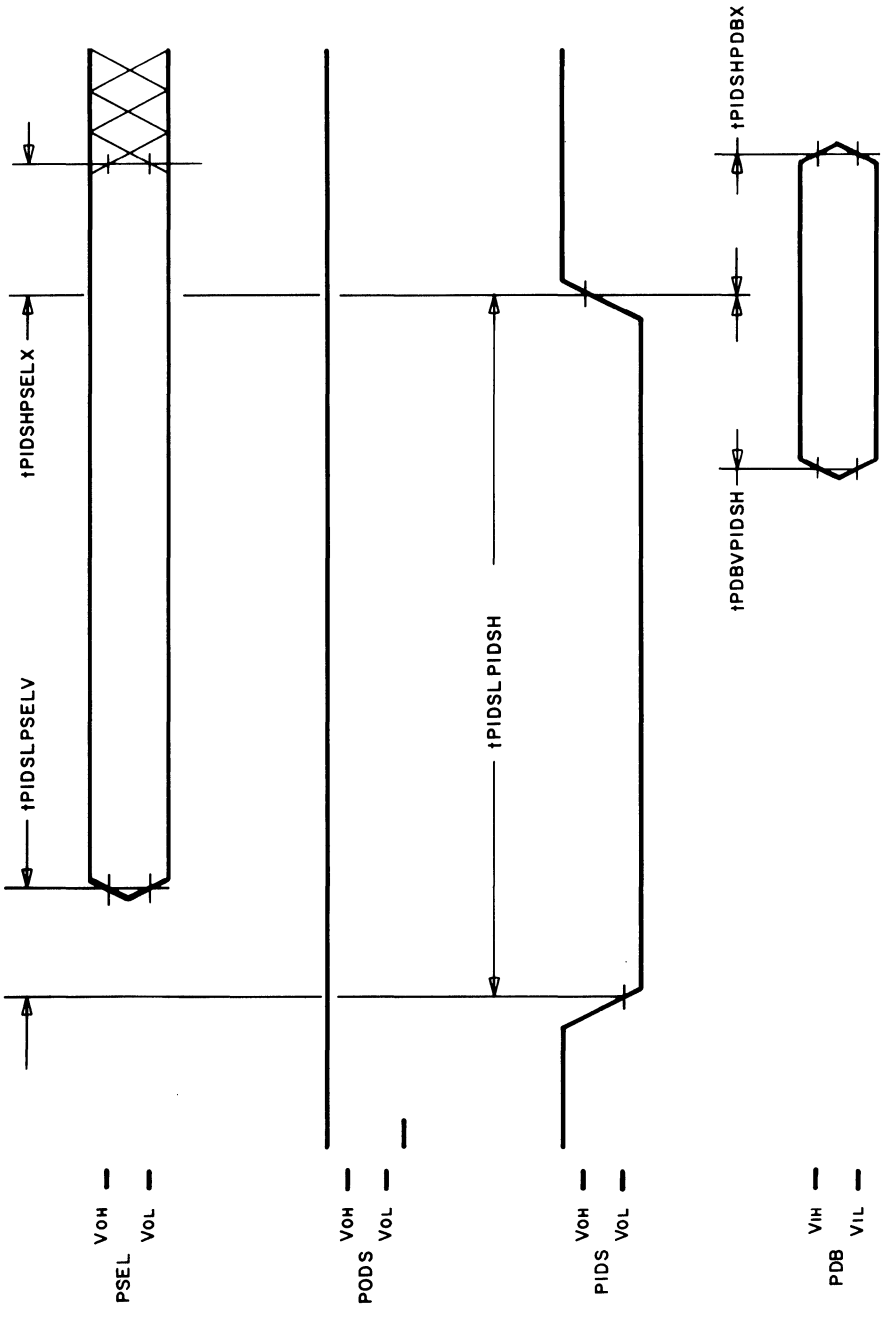


Figure 10. Parallel Active Input Timing

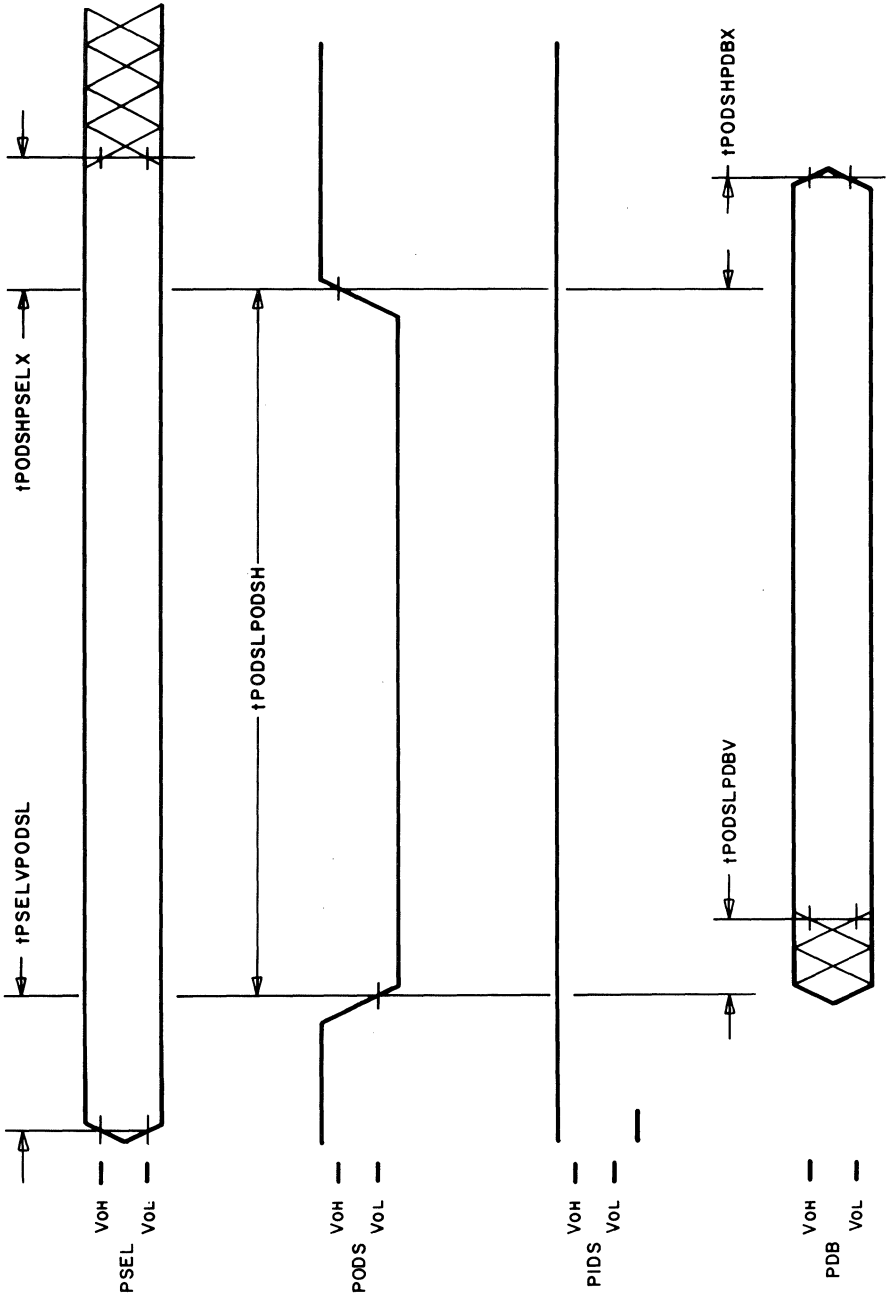


Figure 11. Parallel Active Output Timing

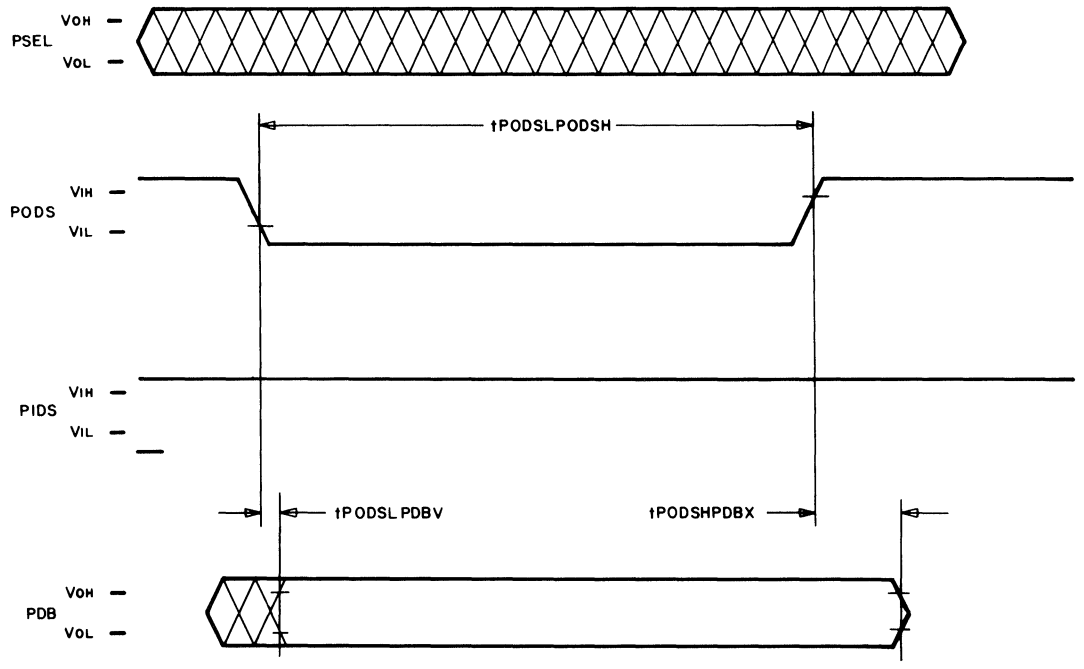


Figure 12. Parallel Passive Output Timing

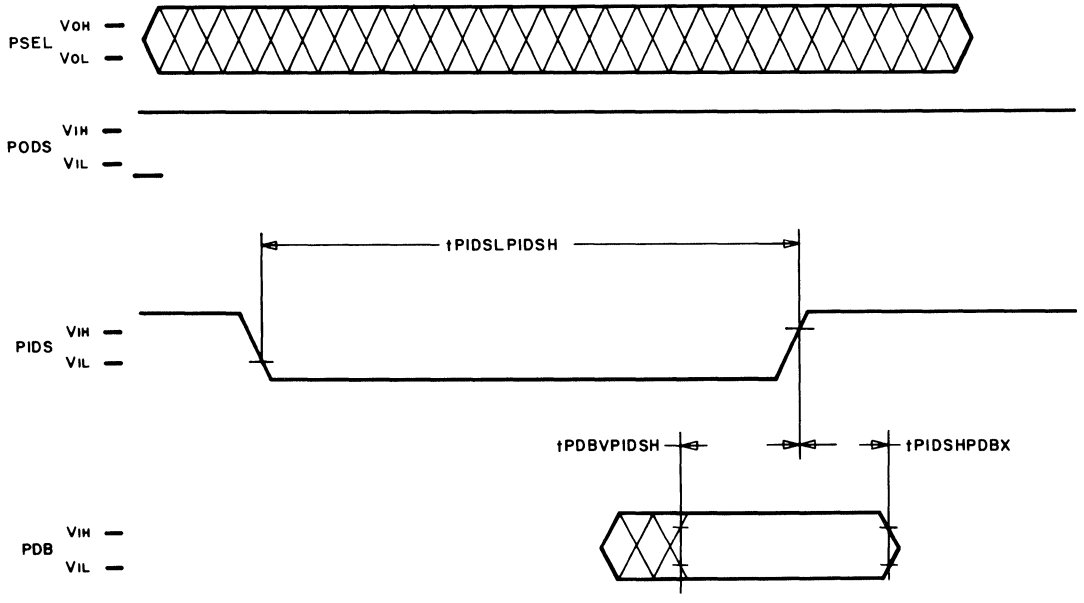


Figure 13. Parallel Passive Input Timing

DSP16 Support

Features

The *WE* DSP16 Digital Signal Processor (DSP) is a 16-bit, high-performance, low-power CMOS integrated circuit that can be programmed to perform a wide variety of signal processing functions. The DSP16 can compute a nonrecursive filter at the rate of 75 ns per tap and a second-order section in 525 ns. For typical signal processing functions, the DSP16 provides up to four times the throughput of previous generation DSPs. The processor is packaged in an 84-pin plastic or ceramic chip carrier. It is the DSP of choice for applications requiring high performance, low power, and low cost.

All DSP16 instructions are 16-bits wide and the assembly language has a C-like syntax. Although some pipelining of DSP16 instructions is necessary to achieve the real-time performance required in many signal processing applications, the degree of pipelining has been reduced from previous generation DSPs to simplify programming. Latency effects have been eliminated.

***WE* DSP16-SL Support Software Library.** The software support tools help to create, test, and debug DSP16 application programs. The support software library runs under either the *UNIX* Operating System or the *MS-DOS* Operating System and provides an integrated assembler and simulator.

Programming aids include breakpoint and single-step capabilities as well as user access to memory and registers. The support software also provides an interface to the DSP16-DS Development System.

***WE* DSP16-DS Digital Signal Processor Development System.** Application system hardware development and software testing is supported by the *WE* DSP16-DS Digital Signal Processor Development System. The development system provides I/O in-circuit emulation to facilitate real-time debugging of user hardware, as well as a simulator accelerator to speed software simulations. Sites are provided in the development system for μ-law/A-law and linear codecs. Up to 16 development systems can be cascaded when developing applications involving multiple DSPs.

The DSP16-DS Digital Signal Processor Development System allows the user to edit, assemble and load programs, as well as to utilize the software simulator. An assembled program can be transferred from the host into the development system's program memory through an RS-232C communications link or through a faster custom parallel interface (100 Kbytes/s) when using an AT&T PC 6300 (or compatible).

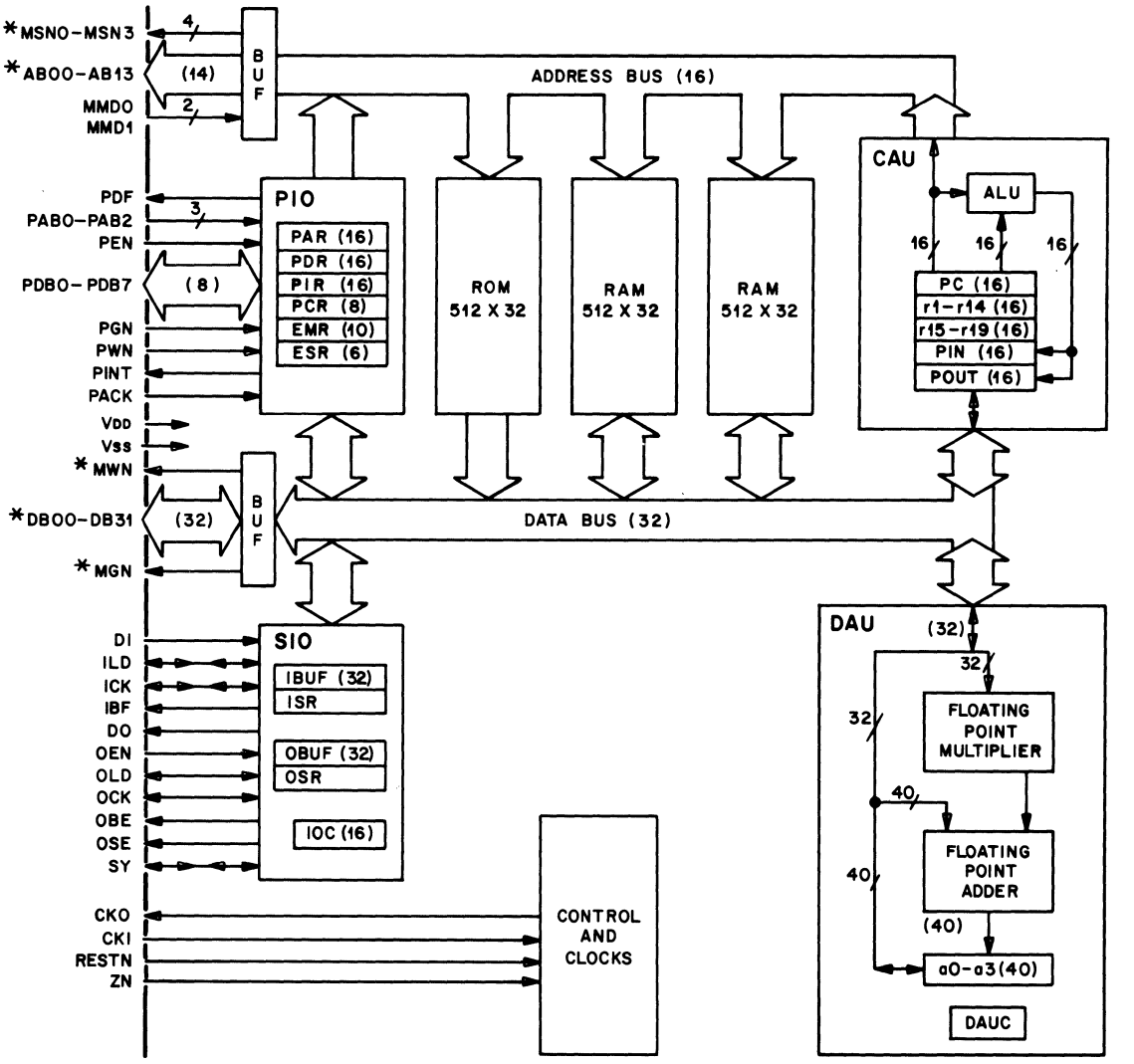
WE DSP32 Digital Signal Processor

Features

- 16-MHz and 25-MHz parts are available
- 2048 bytes ROM, 4096 bytes RAM (on-chip)
- Memory can be addressed as 8-, 16-, or 32-bits
- Four 40-bit accumulators
- Off-chip memory expansion of up to 56 Kbytes (PGA package only)
- Four user-selectable memory organizations
- 32-bit floating-point arithmetic
- 16-bit integer instructions
- Interfaces to a microprocessor without any additional devices
- Serial and parallel I/O ports with DMA options
- Error control logic
- Supported by *WE* DSP32-SL Support Software Library, *WE* DSP32-AL Application Software Library and *WE* DSP32-DS Digital Signal Processor Development System
- Single 5 V power supply required

Description

The *WE* DSP32 Digital Signal Processor integrated circuit is a 32-bit high-speed programmable digital signal processor. The device is available in two versions, 16 MHz or 25 MHz. Both 16-MHz and 25-MHz parts are available in a standard 40-pin DIP or a 100-pin rectangular pin-grid-array (PGA) package. High throughput is achieved by using two execution units, the control arithmetic unit (CAU) and the data arithmetic unit (DAU). The CAU is a 16-bit fixed-point unit for logic and control, and the DAU is a 32-bit floating-point unit for signal processing algorithms. The CAU includes twenty-one 16-bit general-purpose registers and can execute 6.25 million instructions per second at 25 MHz. The DAU contains a floating-point multiplier and adder, and four 40-bit accumulators. The DAU is configured for multiply/accumulate and can perform 12.5 million floating-point computations per second at 25 MHz. The on-chip memory includes 2048 bytes of ROM and 4096 bytes of RAM. Memory can be addressed as 8-, 16-, or 32-bit words and is organized to access 32-bit data at the same speed as 8-bit data. With the 100-pin PGA package, memory can be expanded off-chip with 56 Kbytes of directly accessible data. The device has three I/O ports: a serial port, a parallel port to interface with a microprocessor, and an external memory interface (PGA package only) for memory mapped I/O.



Note: See Tables 21—23 for signal name definitions.
* Available on 100-pin PGA package only.

Legend:

a0—a3	Accumulators 0—3	FPM	Floating-Point Multiplier	PCR	PIO Control Register
ALU	Arithmetic Logic Unit	IBUF	Input Buffer	PDR	PIO Data Register
CAU	Control Arithmetic Unit	IOC	Input/Output Control Register	PIO	Parallel I/O Unit
DAU	Data Arithmetic Unit			PIR	PIO Interrupt Register
DAUC	Data Arithmetic Unit Control Register	ISR	Input Shift Register	r1—r19	Registers 1—19
		OBUF	Output Buffer	PIN	Parallel Input Register
EMR	Error Mask Register	OSR	Output Shift Register	POUT	Parallel Output Register
ESR	Error Source Register	PAR	PIO Address Register	RAM	Read/Write Memory
FPA	Floating-Point Adder	PC	Program Counter	ROM	Read-Only Memory
				SIO	Serial I/O Unit

Figure 1. Block Diagram

User Information

Architectural Summary

The control arithmetic unit (CAU) is used to generate memory addresses and to execute 16-bit integer instructions (see Figure 1). The CAU can execute 6.25 million instructions per second and has twenty-one 16-bit registers, a 16-bit program counter (PC), and an arithmetic logic unit (ALU). All CAU registers are static and do not require refreshing. When addressing 32-bit floating-point operands, registers r1—r14 are used as memory pointers (rP), and r15—r19 are used as increment registers (rI). Register r20, also called PIN (parallel input register), is used as the serial input/output (SIO) DMA input pointer. Register r21, also called POUT (parallel output register), is used as the SIO DMA output pointer. All registers can be general-purpose in the execution of the 16-bit integer operations.

The data arithmetic unit (DAU) is configured for multiply/accumulate operations and is the primary execution unit for signal processing algorithms. The DAU contains a floating-point multiplier and adder, and four 40-bit accumulators (a0—a3). The DAU can perform 6.25 million instructions per second of the form a = b + c * d. The DAU multiplier inputs are 32-bit floating-point numbers; each number is made up of a 24-bit mantissa and an 8-bit exponent. The adder inputs from memory or an accumulator are 8-, 16-, 32-, or 40-bits. The 40-bit input comes from either an accumulator (a0—a3) or the multiplier (32-bits, plus 8 guard bits). The DAU performs floating-point to-and-from 16-bit integer and floating-point to-and-from μ-law and A-law data type conversions.

The DSP32 device has on-chip memory – 2048 bytes of mask-programmable ROM and 4096 bytes of RAM. Data can be 8-, 16-, or 32-bits wide and memory is uniformly byte addressable (see the Memory Addressing section). The RAM is dynamic and is refreshed either automatically or under program control. The ROM can be mask-programmed with application program(s) or constant data. Instructions can also be located in on-chip RAM or external memory. With the PGA package, memory can be expanded off-chip by using standard byte-wide memory devices without any additional interfacing devices. The DSP32 processor can directly address 14K instructions (32-bit words) when using off-chip memory.

The DSP32 memory is divided into two banks – a lower bank (0) and an upper bank (1). Memory access can be made without regard to the upper and lower banks. However, to achieve maximum throughput, memory access must alternate between the two memory banks. As one memory bank is accessed, the other memory bank is addressed. This form of pipelining can reduce the effective memory access time by one-half. Only the lower memory bank address space is expandable off-chip. Therefore, the external address and data buses need to operate at only half the rate of the on-chip buses. Pins MMD0 and MMD1 allow the user to select the location of ROM and RAM in the memory address space.

The serial I/O unit (SIO) is used for serial-to-parallel conversion of input data and parallel-to-serial conversion of output data. Input to the SIO is loaded into the input shift register (ISR) and then into the input buffer (IBUF). Outputs from the SIO are loaded into the output buffer (OBUF) and then into the output shift register (OSR). This double buffering is done so that back-to-back transfers are possible, which allows the DSP32 program to begin a second transfer before the first has been completed. Data widths can be 8-, 16-, or 32-bits. The input/output control (IOC) register in the SIO is used to select various I/O conditions, bit lengths, internal or external clock, and internal or external sync (see Table 2).

The parallel I/O (PIO) unit is used for bidirectional communication between the DSP32 device and an external microprocessor. The external PIO data bus is 8-bits wide, and transfers can be made under program or DMA control. The PIO DMA allows a microprocessor to download a program without interrupting the execution of a DSP32 program in progress. The PIO has three 16-bit registers (PAR, PDR, and PIR), a 10-bit register (EMR), an 8-bit register (PCR), and a 6-bit register (ESR). These registers are used to control PIO transfers and to check for errors.

Memory Addressing

A 32-bit memory location can be addressed as one 32-bit floating-point word, two 16-bit integer words, or four 8-bit byte words. A 32-bit memory address is always divisible by four; a 16-bit memory address is divisible by two.

32-Bit Memory Locations				
32-Bit Floating-Point Word				Memory Address
16-Bit Integer		16-Bit Integer		
Byte	Byte	Byte	Byte	
3	2	1	0	0
7	6	5	4	4
11	10	9	8	8
etc.				

Data Type Memory Select				
Data Type	MSN3	MSN2	MSN1	MSN0
Byte 0	1	1	1	0
Byte 1	1	1	0	1
Byte 2	1	0	1	1
Byte 3	0	1	1	1
Low integer	1	1	0	0
High integer	0	0	1	1
Float	0	0	0	0

Each 32-bit word is organized as four bytes, e.g., 3, 2, 1, 0, where byte 3 is the MSByte (most significant byte) and byte 0 is the LSByte (least significant byte). A 16-bit word is 2 bytes, either 1, 0 with byte 1 the MSByte and byte 0 the LSByte, or 3, 2 with byte 3 the MSByte and byte 2 the LSByte. Memory address 0 can refer to an 8-bit word (byte 0), a 16-bit word (1, 0), or a 32-bit word (3, 2, 1, 0).

Memory addresses 00000—57343 (0x0000—0xDFFF) are in bank 0; memory addresses 57344—65535 (0xE000—0xFFF) are in bank 1. MMD0 and MMD1 are used to select the memory configuration, i.e., the location of the internal RAM and ROM within the address space. Table 1 and Figure 2 show how the memory is configured in the four different memory modes. In all four configurations, the first instruction executed after reset is at address 00000 (0x0000).

100-Pin Rectangular PGA Package

The 14-bit address bus selects a 32-bit word. MSN0—MSN3 (active low) are derived internally according to the data type implied in the instruction and are used to select bytes within that 32-bit word. The two least significant bits of the register pointer (pc, r1—r21) or the direct address determine the values of the memory select lines (MSN0—MSN3). With 56 Kbytes of external memory attached, direct referencing can be made to 65536 bytes, 32768 integers, or 16384 floats. With no external memory, 4096 bytes, 2048 integers, or 1024 floats can be referenced.

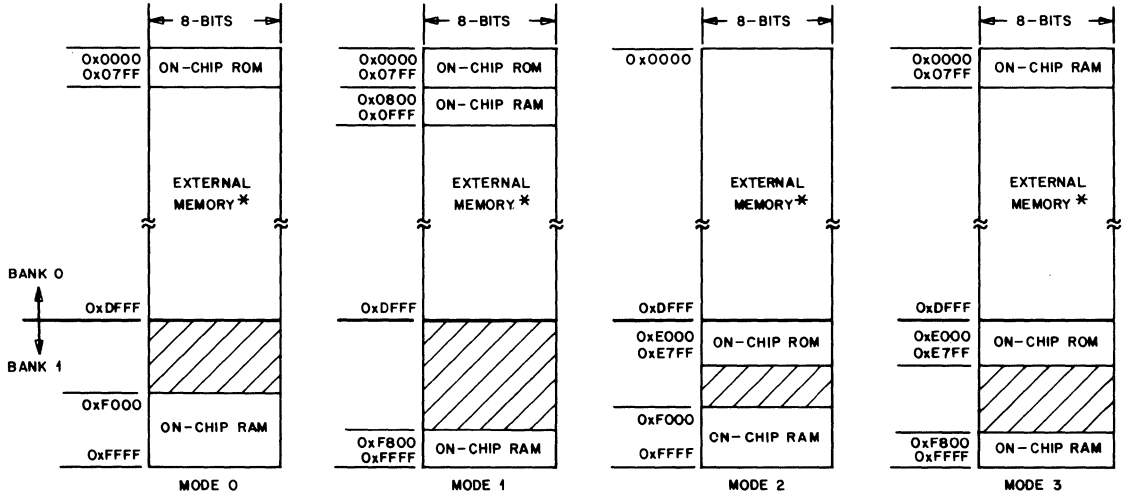
40-Pin DIP

On the 40-pin package, the external memory interface (EMI) is not available, limiting total memory to the 512 32-bit words of ROM and 1024 32-bit words of RAM provided on-chip, which can store 4096 bytes, 2048 integers, or 1024 floats.

Table 1. Memory Configuration Selection

Mode	MMD1	MMD0	Addresses	Assignments
0	0	0	0x0000—0x07FF	On-chip ROM
			0x0800—0xDFFF	External memory*
			0xF000—0xFFFF	On-chip RAM
1	0	1	0x0000—0x07FF	On-chip ROM
			0x0800—0x0FFF	On-chip RAM
			0x1000—0xDFFF	External memory*
			0xF800—0xFFFF	On-chip RAM
2	1	0	0x0000—0xDFFF	External memory*
			0xE000—0xE7FF	On-chip ROM
			0xF000—0xFFFF	On-chip RAM
3	1	1	0x0000—0x07FF	On-chip RAM
			0x0800—0xDFFF	External memory*
			0xE000—0xE7FF	On-chip ROM
			0xF800—0xFFFF	On-chip RAM

* External memory available only on the 100-pin PGA package.



* External memory available only on the 100-pin PGA package.

Figure 2. Memory Address Configurations

Register Operation

The following tables show the register settings for various operating conditions of the *WE* DSP32 Digital Signal Processor.

IOC and DAUC Registers

Tables 2 and 3 show the operating conditions that result after setting the IOC and DAUC registers.

Table 2. IOC Register

Bit	15—13	12	11,10	9	8	7,6	5	4	3,2	1	0
Field	DMA	SAN	OLEN	AOL	AOC	ILEN	AIL	AIC	SLEN	BC	ASY

Bit	Mnemonic	Function
0	ASY	If cleared (0), SY is external; if set (1), SY is internal. If generated internally, SY = {ICK, OCK}/{256, 512, 1024} = IOC[BC]/(32*IOC[SLEN]).
1	BC	If cleared, ICK is used to derive the on-chip load and SY clocks; if set, OCK is used to derive the on-chip load and SY clocks.
3,2	SLEN	These bits select the frequency ratio of the on-chip load clock to the on-chip SY clock: 00 – xx 01 – ratio = 8 10 – ratio = 16 11 – ratio = 32
4	AIC	If cleared, the clock ICK is external; if set, the clock ICK = CKI/8 and is internal.
5	AIL	If cleared, clock ILD is external; if set, clock ILD = {ICK, OCK}/(32) = IOC[BC]/(32) and is internal.
7,6	ILEN	These bits specify the length of the input serial data: 00 – xx 01 – serial input length = 8 bits 10 – serial input length = 16 bits 11 – serial input length = 32 bits
8	AOC	If cleared, OCK is external; if set, OCK = CKI/8 and is internal.
9	AOL	If cleared, OLD is external; if set, OLD = {ICK,OCK}/(32) = IOC[BC]/(32) and is internal.
11,10	OLEN	These bits specify the length of the serial output data: 00 – xx 01 – serial output length = 8 bits 10 – serial output length = 16 bits 11 – serial output length = 32 bits
12	SAN	If cleared, clear sanity; if set, set sanity.

Table 2. IOC Register (Continued)

Bit	Mnemonic	Function
15—13	DMA[2—0]	These bits control DMA mode: 000 – no DMA 001 – input DMA when IBF is high 010 – output DMA when OBE is high 011 – input DMA when IBF is high, output DMA when OBE is high 101 – input and output DMA when IBF is high 110 – input and output DMA when OBE is high 111 – input and output DMA when either IBF or OBE is high

Table 3. DAUC Register Settings

DAUC	Result
xx0	μ-law input conversion
xx1	A-law input conversion
x0x	μ-law output conversion
x1x	A-law output conversion
0xx	No parity check on x operands
1xx	Parity check on x operands

* x = don't care.

PIO Control

The PIO has a processor address bus (PAB0—PAB2) to select the various PIO registers. Table 4 shows the register selection.

Table 4. Register Selection

PAB2—PAB0	Register Selected
000	PAR(l) – lower byte
001	PAR(h) – upper byte
010	PDR(l) – lower byte
011	PDR(h) – upper byte
100	EMR(l) – lower byte; most significant 5 bits
101	EMR(h) – upper byte; most significant 5 bits
110	ESR – most significant 6 bits
111	PCR

Tables 5 and 6 describe PCR and ESR, two of the PIO registers.

The PIO control register (PCR) is an 8-bit register used by an external microprocessor (μP) to set up various controlled transfer modes between the DSP32 device and the microprocessor.

Table 5. PCR Register

Bit	7	6	5	4	3	2	1	0
Field	REF	PIF	PDF	AUTO	DMA	ENI	Intmode	Reset

Bit	Mnemonic	Function
0	Reset	If cleared, halts DSP32 device; if set, runs DSP32 device. Zero-to-one transition initiates reset sequence.
1	Intmode	If cleared, 8-bit PIR interrupt vector; if set, 16-bit PIR interrupt vector.
2	ENI	If cleared, disables PINT due to PIR interrupt; if set, enables PINT due to PIR interrupt.
3	DMA	If cleared, DMA disabled on PIO; if set, DMA enabled on PIO.
4	AUTO	If cleared, PAR not autoincremented on DMA; if set, PAR autoincremented on DMA.
5	PDF	Set when PDR is written to by DSP32 or μP; cleared when PDR is read by DSP32 or μP (read only).
6	PIF	Set when PIR is written to by DSP32 device; cleared when PIR is read by μP (read only).
7	REF	If cleared, enables RAM autorefresh; if set, disables RAM autorefresh.

The error source register (ESR) has 6-bits that can be read only by the external microprocessor. It is cleared after a read. This register is used to store error conditions (bits 3—7) in the DSP32 device.

Table 6. ESR Register

Bit	7	6	5	4	3	2	1	0
Field	LOSY	LOS	ADER	OVE	PE	WPIR	Not Used	

Bit	Mnemonic	Name/Description
0	—	**Not used.**
1	—	**Not used.**
2	WPIR	**PIR Write.** Set when DSP32 device writes to PIR.
3	PE	**Parity Error.** If set, instruction memory parity error.
4	OVE	**Overflow/Underflow Error.** If set, DAU overflow or underflow.
5	ADER	**Addressing Error.** If set, an attempt was made to access a float variable or an integer variable with an address that was not a multiple of 4 or 2, respectively.
6	LOS	**Loss of Sanity.** If set, sanity bit in the IOC register is set and SY changes state from high to low.
7	LOSY	**Loss of Sync.** If set, loss of 8-kHz external sync.

Instruction Set

The DSP32 device has a powerful instruction set for signal processing algorithms, called data arithmetic (DA) instructions. It also supports instructions for logic and control, called control arithmetic (CA) instructions.

DA instructions, which execute in the DAU, perform 32-bit floating-point multiply/accumulate operations for signal processing algorithms. DA instructions also include special functions for such data type conversions as floating-point to-and-from integer and floating-point to-and-from μ-law and A-law.

CA instructions, which execute in the CAU, are 16-bit integer microprocessor instructions that include arithmetic and logic instructions and such control statements as conditional goto and call. CA instructions also include data move statements so that data can be moved between memory, I/O registers, and any of the CAU registers.

Flags

The DSP32 has internal flags that are affected by the results of certain DA, CA, or I/O instructions. These flags, although not directly visible to the user, can be tested by conditional instructions. Table 7 lists the flags, the names used in instructions (see the test column), and the meaning of each flag.

Note: DAU flags are represented with upper case letters, while CAU flags are represented with lower case letters.

Table 7. DSP32 Flags

DAU Flags				
Flag	**Test (State = 1)**	**Meaning**	**Test (State = 0)**	**Meaning**
N	alt	Result is negative	age	Result not negative
Z	aeq	Result is zero	ane	Result not zero
V	avs	Result overflowed	avc	No overflow
U	aus	Result underflowed	auc	No underflow
CAU Flags				
n	mi	Result is negative	pl	Result not negative
z	eq	Result is zero	ne	Result not zero
v	vs	Result overflowed	vc	No overflow
c	cs	Carry or borrow out of MSB	cc	No carry or borrow
I/O Flags				
i	ibf	Input buffer full	ibe	Input buffer empty
o	obf	Output buffer full	obe	Output buffer empty
p	pdf	Parallel data register full	pde	PDR empty
P	pif	Parallel interrupt register full	pie	PIR empty
s	sys	SY (I/O sync pulse) set	syc	SY cleared
b	fbs	Serial I/O frame boundary	fbc	Not SIO frame boundary

For example, for testing the U flag (state is 1) there is an instruction:

if(aus) goto *address*

Flags shown at the end of an instruction indicate which flags are affected by the result of that instruction.

A shown in place of a flag means that the flag is always 0; a dash (–) in place of a flag means that the flag is unaffected by the instruction.

Instructions

The following is the complete DSP32 instruction set, grouped as DA and CA instructions. Where braces, { }, are shown in an instruction, one of the enclosed items must be chosen. Items enclosed in brackets [ ] are optional.

Note: { } and [ ] are not part of the instruction syntax. Parentheses, ( ), are part of the syntax and must appear where shown in an instruction. Lower case letters are part of the syntax. Upper case letters are replaced by immediate data or by a register name (see tables following each instruction group).

Data Arithmetic (DA) Instructions

The DA instructions are divided into two functional groups: multiply/accumulate and special functions.

Table 8. DA Multiply/Accumulate Instructions

Instruction	DAU Flags Affected	Description
[Z=] aN = [–]aM {+,–} Y* X	NZVU	The product of the X and Y fields is added/subtracted to/from the accumulator (aM) and the result is stored in an accumulator (aN). The result can also be output according to the Z field.
aN = [–]aM {+,–} (Z=Y)* X	NZVU	The Y field operand is output according to the Z field. The product of the X and Y fields is added to the accumulator (aM) and the sum is stored in an accumulator (aN).
[Z=] aN = [–]Y {+,–} aM* X	NZVU	The product of the X field and the accumulator (aM) is added/subtracted to/from the Y field. The result is placed in an accumulator (aM) and can also be output according to the Z field.
[Z=] aN = [–]Y* X	NZVU	The product of the X and Y fields is added/subtracted to/from zero. The result is stored in aN and can also be output according to the Z field.
aN = [–](Z=Y)* X	NZVU	The value of the Y field is output according to the Z field. The product of the Y and X fields is stored in an accumulator (aN).
[Z=] aN = [–]Y {+,–}X	NZVU	The sum or difference of the Y and X fields is stored in an accumulator (aN) and the result output according to the Z field. **Note:** X is a multiplier input.
[Z=] aN = [–]Y	NZVU	The value of the Y field is placed in accumulator (aN) and also output according to the Z field.

Table 9. Replacement Table for DA Multiply/Accumulate Instructions

Replace	Value	Meaning
aN, aM, X, Y	a0—a3	One of four DAU accumulators
X,Y,Z	*rP, *rP++, *rP—, *rP++rI	32-bit memory location where rP is a memory pointer (P = 1 – 14) and rI is an increment register (1 = 15 – 19)
X, Y	ibuf	SIO input buffer
Z	obuf	SIO output buffer

Table 10. DA Special Functions

Instruction	DAU Flags Affected	Description
[Z=] aN = ic(Y)	NZ00	Input conversation: μ-law A-law to float
[Z=] aN = oc(Y)	—	Output conversation: float to μ-law A-law
[Z=] aN = float(Y)	NZ00	Conversion: integer to float
[Z=] aN = int(Y)	—	Conversion: float to integer
[Z=] aN = round(Y)	NZVU	Conversion: float(40) to float(32)
[Z=] aN = ifalt(Y)	—	If(alt) then [Z=] aN=Y else [Z=] aN

Table 11. Replacement Table for DA Special Function Instructions

Replace	Value	Meaning
aN, Y	a0—a3	One of four DAU accumulators
Y,Z	*rP, *rP++, *rP—, *rP++rI	Memory location where rP is a memory pointer (P = 1 – 14) and r1 is an increment register (1 = 15 – 19)
Y,Z	pdr	PIO data register
Y	ibuf	SIO input buffer
Z	obuf	SIO output buffer

Control Arithmetic (CA) Instructions

The CA instructions are divided into three functional groups: control, arithmetic/logic, and data move.

Table 12. CA Control Group Instructions

Instruction	Flags Affected	Description
if (CA COND) goto {rH, N, rH+N, rH–N}	None	Conditional branch
if (rM–– >= 0) goto {rH, N, rH+N, rH–N}		Conditional branch
if (DA COND) goto {rH, N, rH+N, rH–N}		Conditional branch
if (IO COND) goto {rH, N, rH+N, rH–N}		Conditional branch
call {rH, N, rH+N, rH–N} (rM)		Call subroutine
return (rM)		Return from subroutine
goto {rH, N, rH+N, rH–N}		Unconditional branch
[L]*nop		No operation

Table 13. Replacement Table for CA Control Group Instructions, CA Conditions (CA COND)

Value	CAU Flags*	Meaning
pl mi	n=0 n=1	Result is nonnegative (plus) Result is negative (minus)
ne eq	z=0 z=1	Result not equal to zero Result equal to zero
vc vs	v=0 v=1	Overflow cleared, no overflow Overflow set, overflowed
cc cs	c=0 c=1	Carry cleared, no carry Carry set, carry
ge lt	n^v=0 n^v=1	Greater than or equal to Less than
gt le	z|(n^v)=0 z|(n^v)=1	Greater than Less than or equal to
hi ls	c|z=0 c|z=1	Greater than (unsigned number) Less than (unsigned number)

* Symbol interpretation: ^ = XOR; | = OR.

Table 14. Replacement Table for CA Control Group Instructions, DA Conditions (DA COND)

Value	DAU Flags	Meaning
ane aeq	Z=0 Z=1	Not equal to zero Equal to zero
age alt	N=0 N=1	Greater than or equal to zero Less than zero
avc avs	V=0 V=1	Overflow cleared, no overflow Overflow set, overflowed
auc aus	U=0 U=1	Underflow cleared, no underflow Underflow set, underflowed
agt ale	N|Z=0 N|Z=1	Greater than zero Less than or equal to zero

Table 15. Replacement Table for CA Control Group Instructions, I/O Conditions (IO COND)

Mnemonic	Condition	Meaning
ibe	ibf=0	Input buffer empty
ibf	ibf=1	Input buffer full
obe	obe=1	Output buffer empty
obf	obe=0	Output buffer full
pde	pdf=0	Parallel data register empty
pdf	pdf=1	Parallel data register full
pie	pif=0	Parallel interrupt register empty
pif	pif=1	Parallel interrupt register full
syc	sy=0	Sync signal low
sys	sy=1	Sync signal high
fbc	fb=0	Serial frame boundary clear
fbs	fb=1	Serial frame boundary set

Table 16. CA Arithmetic/Logic Group Instructions

Instruction	CAU Flags Affected	Description
rD = rH+N	nzvc	Three operand add
rD = rD+rS	nzvc	Add
rD = rD–rS	nzvc	Right subtract
rD–{N,rS}	nzvc	Compare
rD = {N, rS}–rD	nzvc	Left subtract
rD = rD&{N, rS}	nz00	AND
rD&{N, rS}	nz00	Bit test
rD = rD|{N, rS}	nz00	OR
rD = rD^{N, rS}	nz00	XOR
rD = rS/2	nz0c	Arithmetic right shift
rD = rS>>1	0z0c	Logical right shift
rD = –rS	nzvc	Negate
rD = rS*2	nzvc	Arithmetic left shift

Table 17. CA Data Move Group Instructions

Instruction	CAU Flags Affected	Description
rD = N	nz00	—
{ioc, dauc} = VALUE	—	—
{MEM,*N, obuf} = {rSh, rSl}	—	MEM, *N, and obuf are 8-bits
{MEM,*N, obuf, pdr, pir} = rS	—	MEM, *N, and obuf are 16-bits
rD = {MEM,*N, ibuf, pdr}	nz00	MEM, *N, and ibuf are 16-bits
{rDh, rDl} = {MEM,*N, ibuf}	nz00	MEM, *N, and ibuf are 8-bits

Table 18. Replacement Table for All CA Instructions

Replace	Value	Meaning
rH	pc, r1—r21	One of 21 general-purpose CAU registers, or the program counter
rM,rS,rD	r1—r21	One of 21 CAU registers
rDh rSh	r1—r21	High-order bits (8—15) are moved; low-order bits (0—7) are cleared for rDh and remain unchanged for rSh
rDl, rSl	r1—r21	Low-order bits (0—7) are moved; high-order bits are cleared for rDl and remain unchanged for rSl
MEM	*rP, *rP++, *rP– –, *rP++rI (P,I = 1—21)	16-bit or 8-bit memory location
L	Positive integer	—
N	16-bit integer	—
VALUE	16-bit integer or 3-bit integer	VALUE is a 16-bit number for the ioc word and a 3-bit number for dauc word

Summary of Instructions

Tables 19 and 20 list DA and CA instructions, along with the encoding format numbers and the flags. The formats for each instruction are found in the next section.

Table 19. DA Instructions

Instructions	Format	DAU Flags Affected			
Multiply/Accumulate:					
[Z =] aN = [–]aM {+,–} Y* X	3	N	Z	V	U
aN = [–]aM {+,–} (Z=Y)* X	2	N	Z	V	U
[Z =] aN = [–]Y {+,–} aM* X	1	N	Z	V	U
[Z =] aN = [–]Y* X	3	N	Z	V	U
aN = [–](Z=Y)* X	2	N	Z	V	U
[Z =] aN = [–]Y {+,–} X	1	N	Z	V	U
[Z =] aN = [–]Y	1	N	Z	V	U
Special Functions:					
[Z=] aN = ic(Y)	4	N	Z	0	0
[Z=] aN = oc(Y)	4	—	—	—	—
[Z=] aN = float(Y)	4	N	Z	0	0
[Z=] aN = int(Y)	4	—	—	—	—
[Z=] aN = round(Y)	4	N	Z	V	U
[Z=] aN = ifalt(Y)	4	—	—	—	—

Table 20. CA Instructions

Instructions	Format	CAU Flags Affected			
Control Group:					
if (CA COND) goto {rH, N, rH+N, rH–N}	0	—	—	—	—
if (rM– –>=0) goto {rH, N, rH+N, rH–N}	3	—	—	—	—
if (DA COND) goto {rH, N, rH+N, rH–N}	0	—	—	—	—
if (IO COND) goto {rH, N, rH+N, rH–N}	1	—	—	—	—
call {rH, N, rH+N, rH–N} (rM)	4	—	—	—	—
return (rM)	0	—	—	—	—
goto {rH, N, rH+N, rH–N}	0	—	—	—	—
[L]*nop	0	—	—	—	—
Arithmetic Logical Group:					
rD = rH+N	5	n	z	v	c
rD = rD+rS	6a	n	z	v	c
rD = rD–{N, rS}	6a,b	n	z	v	c
rD–{N, rS}	6a,b	n	z	v	c
rD = {N, rS}–rD	6a,b	n	z	v	c
rD = rD&{N, rS}	6a,b	n	z	0	0
rD&{N, rS}	6a,b	n	z	0	0
rD = rD | {N, rS}	6a,b	n	z	0	0
rD = rD^{N, rS}	6a,b	n	z	0	0
rD = rS/2	6a	n	z	0	c
rD = rS>>1	6a	0	z	0	c
rD = –rS	6a	n	z	v	c
rD = rS*2	6a	n	z	v	c
Data Move Group:					
rD = N	5	n	z	0	0
{ioc, dauc} = VALUE	5	—	—	—	—
{MEM, *N, obuf} = {rSh, rSl}	7a,b,c	—	—	—	—
{MEM, *N, obuf, pdr, pir} = rS	7a,b,c	—	—	—	—
rD = {MEM, *N, ibuf, pdr}	7a,b,c	n	z	0	0
{rDh, rDl} = {MEM, *N, ibuf}	7a,b,c	n	z	0	0

DA Instruction Formats

There are four DA instruction formats. Refer to the section on DAU encoding for DA instruction formats for an explanation of each field, except where actual bit values (0, 1) are given.

Format 1.

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	P	0	1	M			—	F	S	N		X	Y	Z

Format 2.

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	P	1	0	M			—	F	S	N		X	Y	Z

Format 3.

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	P	1	1	M			—	F	S	N		X	Y	Z

Format 4.

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	P	1	1	1	1	G				N		—	Y	Z

DAU Encoding for DA Instruction Formats

P Field (Bit 31). Specifies the parity bit. This field maintains an odd number of 1s in the encoding format (odd parity). If the remaining 31 bits of the instruction contain an even number of 1s, the P bit is 1; otherwise, the P bit is 0.

Note: This P field (parity) is not to be confused with the p field used for memory pointers (rP).

G Field. Specifies a data type conversion operation.

G	Operation
0000	ic (input conversion)
0001	oc (output conversion)
0010	float
0011	integer
0100	round
0101	ifalt
0110 0111 1000 1001 1010 1011 1100 1101 1110 1111	Reserved

M Field. Specifies the accumulator used or a constant value.

M	Operand
000	a0
001	a1
010	a2
011	a3
100	0.0
101	1.0
110 111	Reserved

F Field. Specifies sign of operation.

F	Sign
0	+
1	–

N Field. Specifies the accumulator used.

N	Operand
00	a0
01	a1
10	a2
11	a3

S Field. Specifies sign of operation.

S	Sign
0	+
1	–

X, Y, Z Fields. These fields indicate register direct or register indirect modes. The 7-bit fields are divided into two subfields, p and i (pppppiii). Bits 0—2 of the 7-bit field are labeled i; the i subfield specifies an rI register in the CAU. Bits 3—6 are labeled p; the p field specifies an rP register in the CAU.

p Field. Specifies register indirect: *rP, *rP++, *rP—, *rP++rI.

p	Operand
0000	Selects register direct*
0001	r1
0010	r2
0011	r3
0100	r4
0101	r5
0110	r6
0111	r7
1000	r8
1001	r9
1010	r10
1011	r11
1100	r12
1101	r13
1110	r14
1111	Y(p) when Y(p) = X(p) Z(p) when Z(p) = Y(p)

* See i field (p = 0000).

i Field (p = 0000). Specifies a register direct operation: REG. This is a special case of the i field (when p field equals 0).

i	Operand (p = 0000)
000	a0 – X, Y fields only
001	a1 – X, Y fields only
010	a2 – X, Y fields only
011	a3 – X, Y fields only
100	ibuf – X, Y fields only
101	obuf – Z field only
110	pdr – Y, Z fields (special function only)
111	No write, Z field only

i Field (p ≠ 0000). Specifies register indirect: rI, rP++rI.

i	Operand (p ≠ 0000)
000	0
001	r15
010	r16
011	r17
100	r18
101	r19
110	–4(f), –2(i), –1(b)
111	+4(f), +2(i), +1(b)

CA Instruction Formats

There are seven CA instruction formats. Refer to the section on CAU encoding for CA instruction formats for an explanation of each field, except where actual bit values (0, 1) are given.

Formats 0 and 1. Conditional Branch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	0	0	C					G	H					N

Format 2. Reserved

Bit	31	30	29	28	27	26	25	0
Field	P	0	0	0	1	0	Reserved	

Format 3. Loop Counter

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	0	1	1	M					H					N

Format 4. Call

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	1	0	0	M					H					N

Format 5. Three Operand Add

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	1	0	1	D					H					N

Format 6a. Arithmetic/Logic Group — Register Source

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—10	9—5	4—0
Field	P	0	0	1	1	0	0	F				D					—	S	—

Format 6b. Arithmetic/Logic Group — Immediate Operand

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	1	1	0	1	F				D					N

Format 7a. Data Move Group — Direct Memory Address

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	1	1	1	0	T	W		0	H					N

Format 7b. Data Move Group — Pointer Increment, Memory Address

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—10	9—5	4—0
Field	P	0	0	1	1	1	1	T	W		1	H					—	P	I

Format 7c. Data Move Group — I/O

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—10	9—5	4—0
Field	P	0	0	1	1	1	1	T	W		0	H					—	00000	R

CAU Encoding for CA Instruction Formats

P Field (Bit 31). Specifies the parity bit. This field maintains an odd number of 1s in the encoding format (odd parity). If the remaining 31 bits of the instruction have an even number of 1s, the P bit is 1; otherwise, the P bit is 0.

Note: This P field (parity) is not to be confused with the p field used for memory pointers (rP).

C Field. Specifies a CA, DA, or I/O condition.

C	Condition	C	Condition	C	Condition
00xxx	**CA**	**01xxx**	**DA**	**10xxx**	**I/O**
00000	No condition	01000	U	10000	ibf
00001	n	01001	N	10001	obe
00010	z	01010	Z	10010	pdf
00011	v	01011	V	10011	pif
00100	c	01100	N|Z	10100	sy
00101	n^v	01101	Reserved	10101	fb
00110	z|(n^v)	01110	Reserved	10110	Reserved
00111	c|z	01111	Reserved	10111	Reserved

T Field. Specifies the direction of a transfer – to or from a register.

T	Operation
0	Data is moved to a register from memory
1	Data is moved to memory from a register

W Field. Specifies the high or low byte or integer data.

W	Description
00	High byte
01	Low byte
1x	Integer

G Field. Specifies whether to branch if the condition specified in the C Field is true or false.

G	Operation
0	Branch if condition = 0 (false)
1	Branch if condition = 1 (true)

F Field. Specifies the arithmetic/logic group function encoding.

F	Operation
0000	rD=rD+rS
0001	rD=rS*2
0010	rD={N,rS}–rD
0011	Reserved
0100	rD=rD–{N,rS}
0101	rD=–rS
0110	Reserved
0111	rD–{N,rS}
1000	rD=rD^{N,rS}
1001	Reserved
1010	rD=D | {N,rS}
1011	Reserved
1100	rD=rS>>1
1101	rD=rS/2
1110	rD=rD&{N,rS}
1111	rD&{N,rS}

S, D, M, or H Fields. Used for register encoding.

S,D,M, or H	Operand
00000	0
00001	r1
00010	r2
00011	r3
00100	r4
00101	r5
00110	r6
00111	r7
01000	r8
01001	r9
01010	r10
01011	r11
01100	r12
01101	r13
01110	r14
01111	Program counter (pc)
10000	0
10001	r15
10010	r16
10011	r17
10100	r18
10101	r19
10110	–4(f),–2(i),–1(b)
10111	+4(f),+2(i),+1(b)
11000	r20 (pin)
11001	r21 (pout)
11010	dauc
11011	ioc
11100 11101 11110 11111	Reserved

P Field. Specifies a register indirect data move: *rP, *rP++, *rP––, *rP++rI.

P	Operand
00000	Selects format 7C
00001	r1
00010	r2
00011	r3
00100	r4
00101	r5
00110	r6
00111	r7
01000	r8
01001	r9
01010	r10
01011	r11
01100	r12
01101	r13
01110	r14
01111	Reserved
10000	Reserved
10001	r15
10010	r16
10011	r17
10100	r18
10101	r19
10110	Reserved
10111	Reserved
11000	r20 (pin)
11001	r21 (pout)
11010	
11011	
11100	Reserved
11101	
11110	
11111	

I Field. Specifies a register indirect operation.

I	Operand
00000	Reserved
00001	r1
00010	r2
00011	r3
00100	r4
00101	r5
00110	r6
00111	r7
01000	r8
01001	r9
01010	r10
01011	r11
01100	r12
01101	r13
01110	r14
01111	Reserved
10000	0
10001	r15
10010	r16
10011	r17
10100	r18
10101	r19
10110	–2(i), –1(b)
10111	+2(i),+1(b)
11000	r20 (pin)
11001	r21 (pout)
11010	
11011	
11100	Reserved
11101	
11110	
11111	

N Field. Specifies a 16-bit integer included as immediate data or as an address.

R Field (P = 00000). Specifies a register direct operation. This field is valid when the P Field is 0.

R	Operand (P=00000)
00000 00001 00010 00011	Reserved
00100 00101 00110	ibuf obuf pdr
00111 01000 01001 01010 01011 01100 01101 01110 01111 10000 10001 10010 10011 10100 10101	Reserved
10110	pir
10111 11000 11001 11010 11011 11100 11101 11110 11111	Reserved

Pin Descriptions

40-Pin DIP

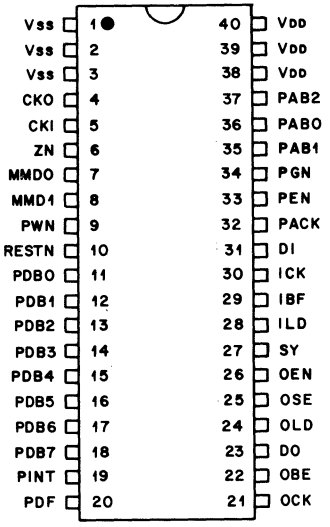


Figure 3. 40-Pin DIP Pin Diagram

Pins by Numerical Order — 40-Pin DIP

In Tables 21—23, I = input, O = output, and P = power. A microprocessor (μP) is used as an example of an external device connected to DSP32 device through the PIO interface.

Table 21. Pin Descriptions by Numerical Order — 40-Pin DIP

Pin	Symbol	Type	Name/Description
1 2 3	Vss	P	**Ground.**
4	CKO	O*	**Clock Out.** Buffered clock at the same frequency as CKI. Synchronizes external devices to the DSP32.
5	CKI	I	**Clock In.** Input clock.
6	ZN	I	**3-State (Active Low).** When active, all DSP32 output pins are 3-stated (high impedance); when not connected, ZN is inactive.
7 8	MMD0 MMD1	I	**Memory Mode — Bits 0 and 1.** Decoded to select the address of on-chip memory (see the Memory Addressing section).
9	PWN	I	**Processor Write Enable (Active Low).** When active, enables on-chip registers to be written to by a μP.
10	RESTN	I	**Reset (Active Low).** Controls the DSP32 run/halt state. A high-to-low transition causes entry into the halt state; a low-to-high transition causes the reset sequence. The reset sequence stores the PC in r14; clears PC, IOC, ESR; and sets EMR to mask all errors. The PCR register bits, except PCR0, are cleared; PCR0 is set. CAU and DAU condition flags and the DAUC register are not affected by reset.

* Indicates 3-state condition.

Table 21. Pin Descriptions by Numerical Order — 40-Pin DIP (Continued)

Pin	Symbol	Type	Name/Description
11	PDB0	I/O*	**Parallel Data Bus — Bit 0.** Bidirectional 8-bit data bus for μP interface. This bus transfers data into and out of the PIO registers for use by a μP.
12	PDB1		**Parallel Data Bus — Bit 1.**
13	PDB2		**Parallel Data Bus — Bit 2.**
14	PDB3		**Parallel Data Bus — Bit 3.**
15	PDB4		**Parallel Data Bus — Bit 4.**
16	PDB5		**Parallel Data Bus — Bit 5.**
17	PDB6		**Parallel Data Bus — Bit 6.**
18	PDB7		**Parallel Data Bus — Bit 7.**
19	PINT	O*	**Processor Interrupt.** Interrupt to μP. PINT is set when a nonmasked error occurs or when the DSP32 writes to PIR and bit 2 of PCR is high; PINT is cleared by reading ESR or PIR.
20	PDF	O*	**Parallel Data Full.** Set when PDR is written to by the DSP32 or a μP; cleared when PDR is read by the DSP32 or a μP.
21	OCK	I/O*	**Output Clock.** Clock for serial PCM output data. In internal mode OCK is an output; in external mode OCK is an input, depending on the I/O format.
22	OBE	O*	**Output Buffer Empty.** Indicates state of serial PCM output buffer (OBUF). OBE is cleared when OBUF is written by the DSP32.
23	DO	O*	**Data Output.** Serial PCM data output from OBUF. 3-stated when $\overline{\text{OEN}}$ is high.
24	OLD	I/O*	**Output Load.** Clock for loading the parallel-to-serial converter from OBUF. In internal mode OLD is an output; in external mode OLD is an input, depending on the I/O format.
25	OSE	O*	**Output Shift Register Empty.** Indicates end of serial transmission. Complement of OLD and delayed by the number of bits in the transmission, as set by the IOC register.
26	OEN	I	**Output Enable (Active Low).** Enables DO as an output. When high, DO is 3-stated.
27	SY	I/O*	**Synchronization.** In internal mode (output), DSP32 provides frame sync; in external mode (input), frame sync is provided to the DSP32.
28	ILD	I/O*	**Input Load.** Clock for loading input buffer from serial-to-parallel converter. In internal mode ILD is an output; in external mode ILD is an input, depending on the I/O format.
29	IBF	O*	**Input Buffer Full.** Indicates state of input buffer (IBUF). IBF is cleared when IBUF is loaded onto the parallel data bus by the DSP32.

* Indicates 3-state condition.

Table 21. Pin Descriptions by Numerical Order — 40-DIP (Continued)

Pin	Symbol	Type*	Name/Description
30	ICK	I/O*	**Input Clock.** Clock for serial PCM input data. In internal mode ICK is an output; in external mode ICK is an input, depending on the I/O format.
31	DI	I	**Data Input.** Serial PCM data into IBUF.
32	PACK	I	**Processor Acknowledge.** Flag from μP acknowledging an interrupt. PACK allows the μP to read PIR register and to reset PINT.
33	PEN	I	**Processor Interface Enable (Active Low).** When active, $\overline{\text{PEN}}$ allows a read from or a write to the processor PIO data bus (PDB).
34	PGN	I	**Processor Read Enable (Active Low).** When active, enables PDB for output and allows the μP to read data from the selected PIO register.
35 36 37	PAB1 PAB0 PAB2	I	**Processor Address Bus — Bits 0—2.** Decoded to select lower or upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
38 39 40	V_{DD}	P	**5 V Supply.**

* Indicates 3-state condition.

100-Pin Rectangular PGA Package

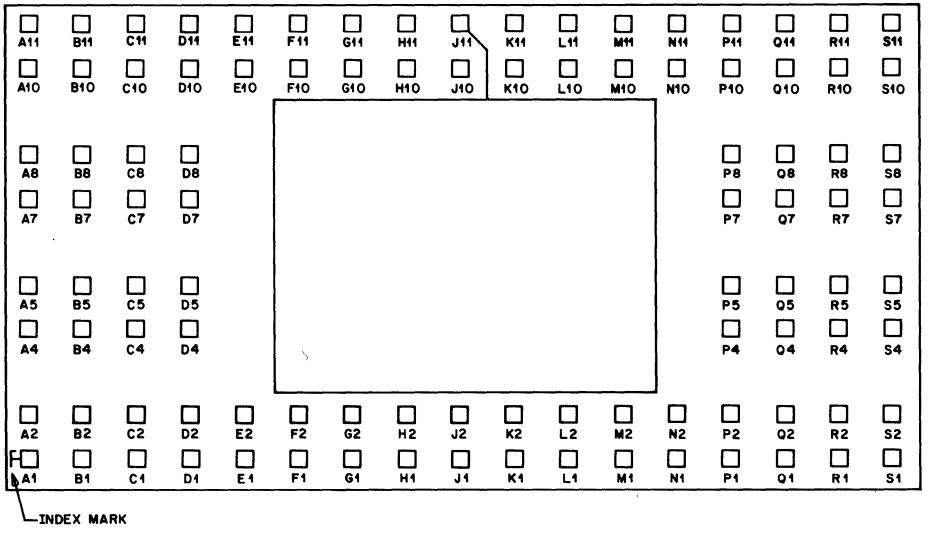


Figure 4. 100-Pin Rectangular PGA Diagram — Top View

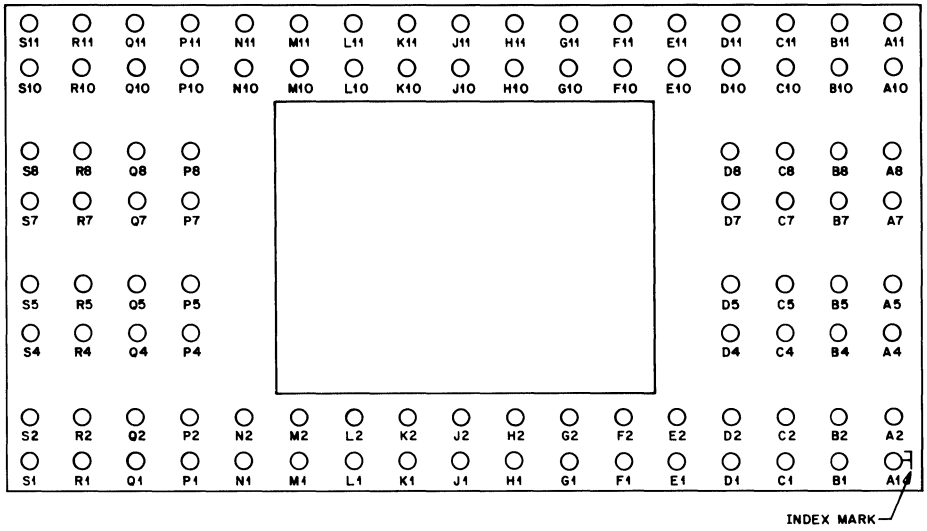


Figure 5. 100-Pin Rectangular PGA Diagram — Bottom View

Pins by Alphanumerical Order — PGA Package

Table 22. Pin Descriptions by Alphanumerical Order — PGA Package

Pin	Symbol	Type	Name/Description
A1	DB00	I/O	**External Memory Data Bus — Bit 00.**
A2	DB01	I/O*	**External Memory Data Bus — Bit 01.**
A4	VSS	P	**Ground.**
A5	MSN1	O*	**Memory Select — Bit 1 (Active Low).** Selects byte 1 of memory addressed by the external memory address bus.
A7	MSN0	O*	**Memory Select — Bit 0 (Active Low).** Selects byte 0 of memory addressed by the external memory address bus.
A8	VSS	P	**Ground.**
A10	AB07	O*	**External Memory Address Bus — Bit 07.**
A11	AB06	O*	**External Memory Address Bus — Bit 06.**
B1	DB02	I/O*	**External Memory Data Bus — Bit 02.**
B2	DB03	I/O*	**External Memory Data Bus — Bit 03.**
B4	MSN3	O*	**Memory Select — Bit 3 (Active Low).** Selects byte 3 of memory addressed by the external memory address bus.
B5	MSN2	O*	**Memory Select — Bit 2 (Active Low).** Selects byte 2 of memory addressed by the external memory address bus.
B7	AB13	O*	**External Memory Address Bus — Bit 13.**
B8	AB12	O*	**External Memory Address Bus — Bit 12.**
B10	AB05	O*	**External Memory Address Bus — Bit 05.**
B11	AB04	O*	**External Memory Address Bus — Bit 04.**

* Indicates 3-state condition.

Table 22. Pin Descriptions by Alphanumerical Order — PGA Package (Continued)

Pin	Symbol	Type	Name/Description
C1	DB04	I/O*	**External Memory Data Bus — Bit 04.**
C2	DB05	I/O*	**External Memory Data Bus — Bit 05.**
C4	—	—	**Not Used.** This pin must be left open.
C5	—	—	**Not Used.** This pin must be left open.
C7	AB11	O*	**External Memory Address Bus — Bit 11.**
C8	AB10	O*	**External Memory Address Bus — Bit 10.**
C10	AB03	O*	**External Memory Address Bus — Bit 03.**
C11	AB02	O*	**External Memory Address Bus — Bit 02.**
D1	DB06	I/O*	**External Memory Data Bus — Bit 06.**
D2	DB07	I/O*	**External Memory Data Bus — Bit 07.**
D4	MGN	O*	**Memory Output Enable (Active Low).** Enables memory output on external memory data bus.
D5	MWN	O*	**Memory Write (Active Low).** Controls data writes to memory.
D7	AB09	O*	**External Memory Address Bus — Bit 09.**
D8	AB08	O*	**External Memory Address Bus — Bit 08.**
D10	AB01	O*	**External Memory Address Bus — Bit 01.**
D11	AB00	O*	**External Memory Address Bus — Bit 00.**
E1	V_{DD}	P	**5 V Supply.** For external memory interface. If external memory is not used, this pin must be connected to V_{SS}.
E2	DB08	I/O*	**External Memory Data Bus — Bit 08.**
E10	CKI	I	**Clock In.** Input clock.
E11	V_{DD}	P	**5 V Supply.**
F1	DB09	I/O*	**External Memory Data Bus — Bit 09.**
F2	DB10	I/O*	**External Memory Data Bus — Bit 10.**
F10	MMD1	I	**Memory Mode — Bit 1.** Decoded with MMD0 to select the address of on-chip memory (see the Memory Addressing section).
F11	MMD0	I	**Memory Mode — Bit 0.** Decoded with MMD1 to select the address of on-chip memory.
G1	DB11	I/O*	**External Memory Data Bus — Bit 11.**
G2	DB12	I/O*	**External Memory Data Bus — Bit 12.**

* Indicates 3-state condition.

Table 22. Pin Descriptions by Alphanumerical Order — PGA Package (Continued)

Pin	Symbol	Type	Name/Description
G10	RESTN	I	**Reset (Active Low).** Controls the DSP32 run/halt state; A high-to-low transition causes entry into the halt state; a low-to-high transition causes the reset sequence. Reset sequence stores PC in r14; clears PC, IOC, ESR; and sets EMR to mask all errors. The PCR register bits, except PCR0, are cleared; PCR0 is set. CAU and DAU condition flags and the DAUC registers are not affected by reset.
G11	ZN	I	**3-State (Active Low).** When active, all DSP32 output pins are 3-stated; when not connected, ZN is inactive.
H1	DB13	I/O*	**External Memory Data Bus — Bit 13.**
H2	DB14	I/O*	**External Memory Data Bus — Bit 14.**
H10	—	—	**Not Used.** This pin must be left open.
H11	CKO	O*	**Clock Out.** Buffered clock at the same frequency as CKI. Synchronizes external devices to the DSP32.
J1	DB15	I/O*	**External Memory Data Bus — Bit 15.**
J2	DB16	I/O*	**External Memory Data Bus — Bit 16.**
J10	—	—	**Not Used.** This pin must be left open.
J11	Vss	P	**Ground.**
K1	DB17	I/O*	**External Memory Data Bus — Bit 17.**
K2	DB18	I/O*	**External Memory Data Bus — Bit 18.**
K10	—	—	**Not Used.** This pin must be left open.
K11	PAB2	I	**Processor Address Bus — Bit 2.** Bit 2 of 3-bit address from μP decoded along with PAB0 (pin L11) and PAB1 (pin L10) to select the lower and upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
L1	DB19	I/O*	**External Memory Data Bus — Bit 19.**
L2	DB20	I/O*	**External Memory Data Bus — Bit 20.**
L10	PAB1	I	**Processor Address Bus — Bit 1.** Bit 1 of 3-bit address from μP decoded along with PAB0 (pin L11) and PAB2 (pin K11) to select the lower or upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
L11	PAB0	I	**Processor Address Bus — Bit 0.** Bit 0 of 3-bit address from μP decoded along with PAB1 (pin L10) and PAB2 (pin K11) to select the lower or upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
M1	DB21	I/O*	**External Memory Data Bus — Bit 21.**
M2	DB22	I/O*	**External Memory Data Bus — Bit 22.**

* Indicates 3-state condition.

Table 22. Pin Descriptions by Alphanumerical Order — PGA Package (Continued)

Pin	Symbol	Type	Name/Description
M10	PWN	I	**Processor Write Enable (Active Low).** When active, enables on-chip registers to be written by a μP.
M11	PGN	I	**Processor Read Enable (Active Low).** When active, enables PDB for output and allows the μP to read data from the selected PIO register.
N1	VDD	P	**5 V Supply.** For external memory interface. If external memory is not used, this pin must be connected to VSS.
N2	DB23	I/O*	**External Memory Data Bus — Bit 23.**
N10	PEN	I	**Processor Interface Enable (Active Low).** When active, PEN allows a read from or a write to the PIO data bus (PDB).
N11	VDD	P	**5 V Supply.**
P1	DB24	I/O*	**External Memory Data Bus — Bit 24.**
P2	DB25	I/O*	**External Memory Data Bus — Bit 25.**
P4	OEN	I	**Output Enable (Active Low).** Enables DO for output. When set, DO is 3-stated.
P5	OBE	O*	**Output Buffer Empty.** Indicates the state of serial PCM output buffer (OBUF). OBE is cleared when OBUF is written to by the DSP32.
P7	DI	I	**Data Input.** Serial PCM data input to IBUF.
P8	PDF	O*	**Parallel Data Full.** Set when PDR is written to by the DSP32 or a μP; cleared when PDR is read by the DSP32 or a μP.
P10	PACK	I	**Processor Acknowledge.** Flag from μP acknowledging interrupt. PACK allows the μP to read PIR register and to reset PINT.
P11	PDB0	I/O*	**Parallel Data Bus — Bit 0.**
Q1	DB26	I/O*	**External Memory Data Bus — Bit 26.**
Q2	DB27	I/O*	**External Memory Data Bus — Bit 27.**
Q4	DO	O*	**Data Output.** Serial PCM data output from OBUF. 3-stated when OEN is set.
Q5	IBF	O*	**Input Buffer Full.** Indicates state of input buffer (IBUF). IBF is cleared when IBUF is loaded onto the data bus by DSP32.
Q7	ILD	I/O*	**Input Load.** Clock for loading input buffer from serial-to-parallel converter. In internal mode ILD is an output; in external mode ILD is an input, depending on the I/O format.

* Indicates 3-state condition.

Table 22. Pin Descriptions by Alphanumerical Order — PGA Package (Continued)

Pin	Symbol	Type	Name/Description
Q8	PINT	O*	**Processor Interrupt.** Interrupt to μP. PINT is set when a nonmasked error occurs, or when the DSP32 writes to PIR and bit 2 of PCR is set; PINT is cleared by reading ESR or PIR.
Q10	PDB2	I/O*	**Parallel Data Bus — Bit 2.**
Q11	PDB1	I/O*	**Parallel Data Bus — Bit 1.**
R1	DB28	I/O*	**External Memory Data Bus — Bit 28.**
R2	DB29	I/O*	**External Memory Data Bus — Bit 29.**
R4	OSE	O*	**Output Shift Register Empty.** Indicates end of serial transmission. Complement of OLD. Delayed by the number of bits in the transmission as set by the IOC register.
R5	SY	I/O*	**Synchronization.** In internal mode (output), DSP32 provides frame sync; in external mode (input), frame sync is provided to the DSP32.
R7	ICK	I/O*	**Input Clock.** Clock for serial PCM input data. In internal mode ICK is an output; in external mode ICK is an input, depending on the I/O format.
R8	PDB7	I/O*	**Parallel Data Bus — Bit 7.**
R10	PDB4	I/O*	**Parallel Data Bus — Bit 4.**
R11	PDB3	I/O*	**Parallel Data Bus — Bit 3.**
S1	DB30	I/O*	**External Memory Data Bus — Bit 30.**
S2	DB31	I/O*	**External Memory Data Bus — Bit 31.**
S4	VSS	P	**Ground.**
S5	OLD	I/O*	**Output Load.** Clock for loading parallel-to-serial converter from OBUF. In internal mode OLD is an output; in external mode OLD is an input, depending on the I/O format.
S7	OCK	I/O*	**Output Clock.** Clock for serial PCM output data. In internal mode OCK is an output; in external mode OCK is an input, depending on the I/O format.
S8	VSS	P	**Ground.**
S10	PDB6	I/O*	**Parallel Data Bus — Bit 6.**
S11	PDB5	I/O*	**Parallel Data Bus — Bit 5.**

* Indicates 3-state condition.

Pins by Functional Group Order

Table 23. Pin Descriptions by Functional Group Order — PGA Package

Pin	Symbol	Type	Name/Description
D11	AB00		External Memory Address Bus — Bit 00.
D10	AB01		External Memory Address Bus — Bit 01.
C11	AB02		External Memory Address Bus — Bit 02.
C10	AB03		External Memory Address Bus — Bit 03.
B11	AB04		External Memory Address Bus — Bit 04.
B10	AB05		External Memory Address Bus — Bit 05.
A11	AB06	O*	External Memory Address Bus — Bit 06.
A10	AB07		External Memory Address Bus — Bit 07.
D8	AB08		External Memory Address Bus — Bit 08.
D7	AB09		External Memory Address Bus — Bit 09.
C8	AB10		External Memory Address Bus — Bit 10.
C7	AB11		External Memory Address Bus — Bit 11.
B8	AB12		External Memory Address Bus — Bit 12.
B7	AB13		External Memory Address Bus — Bit 13.
A1	DB00		External Memory Data Bus — Bit 00.
A2	DB01		External Memory Data Bus — Bit 01.
B1	DB02		External Memory Data Bus — Bit 02.
B2	DB03		External Memory Data Bus — Bit 03.
C1	DB04		External Memory Data Bus — Bit 04.
C2	DB05		External Memory Data Bus — Bit 05.
D1	DB06		External Memory Data Bus — Bit 06.
D2	DB07		External Memory Data Bus — Bit 07.
E2	DB08		External Memory Data Bus — Bit 08.
F1	DB09		External Memory Data Bus — Bit 09.
F2	DB10	I/O*	External Memory Data Bus — Bit 10.
G1	DB11		External Memory Data Bus — Bit 11.
G2	DB12		External Memory Data Bus — Bit 12.
H1	DB13		External Memory Data Bus — Bit 13.
H2	DB14		External Memory Data Bus — Bit 14.
J1	DB15		External Memory Data Bus — Bit 15.
J2	DB16		External Memory Data Bus — Bit 16.
K1	DB17		External Memory Data Bus — Bit 17.
K2	DB18		External Memory Data Bus — Bit 18.
L1	DB19		External Memory Data Bus — Bit 19.
L2	DB20		External Memory Data Bus — Bit 20.
M1	DB21		External Memory Data Bus — Bit 21.
M2	DB22		External Memory Data Bus — Bit 22.

* Indicates 3-state condition.

Table 23. Pin Descriptions by Functional Group Order — PGA Package (Continued)

Pin	Symbol	Type	Name/Description
N2	DB23	I/O*	**External Memory Data Bus — Bit 23.**
P1	DB24		**External Memory Data Bus — Bit 24.**
P2	DB25		**External Memory Data Bus — Bit 25.**
Q1	DB26		**External Memory Data Bus — Bit 26.**
Q2	DB27		**External Memory Data Bus — Bit 27.**
R1	DB28		**External Memory Data Bus — Bit 28.**
R2	DB29		**External Memory Data Bus — Bit 29.**
S1	DB30		**External Memory Data Bus — Bit 30.**
S2	DB31		**External Memory Data Bus — Bit 31.**
F11	MMD0	I	**Memory Mode — Bit 0.** MMD0 and MMD1 are decoded
F10	MMD1		**Memory Mode — Bit 1.** to select the address of on-chip memory (see the memory addressing section).
D4	MGN	O*	**Memory Output Enable (Active Low).** Enables memory output on external memory data bus.
D5	MWN	O*	**Memory Write (Active Low).** Controls data writes to memory.
A7	MSN0	O*	**Memory Select — Bit 0.** MSN0—MSN3 (active low),
A5	MSN1		**Memory Select — Bit 1.** select individual bytes 0, 1, 2, or 3 of
B5	MSN2		**Memory Select — Bit 2.** memory addressed by the external
B4	MSN3		**Memory Select — Bit 3.** memory address bus.
P11	PDB0	I/O*	**Parallel Data Bus — Bit 0.**
Q11	PDB1		**Parallel Data Bus — Bit 1.**
Q10	PDB2		**Parallel Data Bus — Bit 2.**
R11	PDB3		**Parallel Data Bus — Bit 3.**
R10	PDB4		**Parallel Data Bus — Bit 4.**
S11	PDB5		**Parallel Data Bus — Bit 5.**
S10	PDB6		**Parallel Data Bus — Bit 6.**
R8	PDB7		**Parallel Data Bus — Bit 7.**
L11	PAB0	I	**Processor Address Bus — Bit 0.** PAB0—PAB2 are decoded to
L10	PAB1		**Processor Address Bus — Bit 1.** select the lower or upper byte
K11	PAB2		**Processor Address Bus — Bit 2.** of PAR, PDR, or EMR. Also selects ESR/PCR.
P10	PACK	I	**Processor Acknowledge.** Flag from μP acknowledging interrupt. PACK allows the μP to read PIR register and reset PINT.

* Indicates 3-state condition.

Table 23. Pin Descriptions by Functional Group Order — PGA Package (Continued)

Pin	Symbol	Type	Name/Description
N10	PEN	I	**Processor Interface Enable (Active Low).** When active, PEN allows a read from or a write to the PIO data bus (PDB).
M11	PGN	I	**Processor Read Enable (Active Low).** Allows μP to read data from the selected PIO register.
M10	PWN	I	**Processor Write Enable (Active Low).** When active, enables on-chip registers to be written to by a μP.
Q8	PINT	O*	**Processor Interrupt.** Interrupt to μP. PINT is set when a nonmasked error occurs, or when the DSP32 writes to PIR and bit 2 of PCR is set; PINT is cleared by reading ESR or PIR.
P8	PDF	O*	**Parallel Data Full.** Set when PDR is written to by the DSP32 or a μP; cleared when PDR is read by the DSP32 or by a μP.
P7	DI	I	**Data Input.** Serial PCM data in to IBUF.
Q5	IBF	O*	**Input Buffer Full.** Indicates state of input buffer (IBUF). IBF is cleared when IBUF is loaded onto the data bus by DSP32.
R7	ICK	I/O*	**Input Clock.** Clock for serial PCM input data. In internal mode ICK is an output; in external mode ICK is an input, depending on the I/O format.
Q7	ILD	I/O*	**Input Load.** Clock for loading input buffer from serial-to-parallel converter. In internal mode ILD is an output; in external mode ILD is an input, depending on the I/O format.
Q4	DO	O*	**Data Output.** Serial PCM data output from OBUF. 3-stated when OEN is set.
P5	OBE	O*	**Output Buffer Empty.** Indicates the state of serial PCM output buffer (OBUF). OBE is cleared when OBUF is written to by the DSP32.
S7	OCK	I/O*	**Output Clock.** Clock for serial PCM output data. In internal mode OCK is an output; in external mode OCK is an input, depending on the I/O format.
S5	OLD	I/O*	**Output Load.** Clock for loading parallel-to-serial converter from OBUF. In internal mode OLD is an output; in external mode OLD is an input, depending on the I/O format.
R4	OSE	O*	**Output Shift Register Empty.** Indicates end of serial transmission. Complement of OLD. Delayed by the number of bits in the transmission as set by the IOC register.

* Indicates 3-state condition.

Table 23. Pin Descriptions by Functional Group Order — PGA Package (Continued)

Pin	Symbol	Type	Name/Description
P4	OEN	I	**Output Enable (Active Low).** Enables DO for output. When set, DO is 3-stated.
R5	SY	I/O*	**Synchronization.** In internal mode (output), DSP32 provides frame sync; in external mode (input), frame sync is provided to the DSP32.
E10	CKI	I	**Clock In.** Input clock.
H11	CKO	O*	**Clock Out.** Buffered clock at the same frequency as CKI. Synchronizes external devices to the DSP32.
G10	RESTN	I	**Reset (Active Low).** Controls the DSP32 run/halt state. A high-to-low transition causes entry into the halt state; a low-to-high transition causes the reset sequence. Reset sequence stores PC in r14; clears PC, IOC, ESR; and sets EMR to mask all errors. The PCR register bits, except PCR0, are cleared; PCR0 is set. CAU and DAU condition flags and the DAUC registers are to affected by reset.
G11	ZN	I	**3-State (Active Low).** When active, all DSP32 output pins are 3-stated; when not connected, ZN is inactive.
E1 N1	V_{DD}	P	**5 V Supply.** For external memory interface. If external memory is not used, this pin must be connected to V_{SS}.
E11 N11	V_{DD}	P	**5 V Supply.**
A4 S4 A8 S8 J11	V_{SS}	P	**Ground.**
C4 C5 H10 J10 K10	—	—	**Not Used.** These pins must be left open.

* Indicates 3-state condition.

Characteristics

Electrical Characteristics and Requirements

T_C = 0 to 115 °C; V_{SS} = 0 V

Table 24. Input and Output Parameters

Parameter	Sym	16 MHz			25 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply voltage	V_{DD}	4.5	5.0	5.5	4.75	5.0	5.25	V
Input voltage:								
all inputs except ZN								
low	V_{IL}	—	—	.8	—	—	0.8	V
high	V_{IH}	2.4	—	—	2.4	—	—	V
ZN								
low	V_{IL}	—	—	V_{SS}	—	—	V_{SS}	V
high	V_{IH}	Open	—	—	Open	—	—	V
Output voltage:								
low (I_{OL} = 2 mA)	V_{OL}	—	—	0.4	—	—	0.4	V
high (I_{OH} = –0.2 mA)	V_{OH}	2.4	—	—	2.4	—	—	V
Input leakage:								
all inputs except ZN								
low (V_{IL} = 0 V)	I_{IL}	–10	—	—	–10	—	—	μA
high (V_{IH} = 5.5 V)	I_{IH}	—	—	10	—	—	—	μA
high (V_{IH} = 5.25 V)	I_{IH}	—	—	—	—	—	10	μA
ZN								
low (V_{IL} = 0 V)	I_{IL}	–500	—	—	–500	—	—	μA
high (V_{IH} = 5.5 V)	I_{IH}	—	—	20	—	—	—	μA
high (V_{IH} = 5.25 V)	I_{IH}	—	—	—	—	—	20	μA
Input capacitance	C_I	—	—	10	—	—	10	pF
Output offset current:								
low (V_{OL} = 0 V)	I_{OZL}	–20	—	—	–20	—	—	μA
high (V_{OH} = 5.5 V)	I_{OZH}	—	—	20	—	—	—	μA
high (V_{OH} = 5.25 V)	I_{OZH}	—	—	—	—	—	20	μA
Power supply current:	I_{DD}							
T_C = 0 °C								
40-pin package		—	—	550	—	—	550	mA
100-pin package without EMI*		—	—	550	—	—	550	mA
100-pin package with EMI*		—	—	600	—	—	600	mA
T_C = 115 °C								
40-pin package		—	360	420	—	360	420	mA
100-pin package without EMI*		—	360	420	—	360	420	mA
100-pin package with EMI*		—	400	470	—	400	470	mA
Power dissipation:	PD							
T_C = 0 °C								
40-pin package		—	—	3.0	—	—	3.0	W
100-pin package without EMI*		—	—	3.0	—	—	3.0	W
100-pin package with EMI*		—	—	3.3	—	—	3.3	W
T_C = 115 °C								
40-pin package		—	1.8	2.3	—	1.8	2.3	W
100-pin package without EMI*		—	1.8	2.3	—	1.8	2.3	W
100-pin package with EMI*		—	2.0	2.6	—	2.0	2.6	W

* EMI = external memory interface.

Output Drive

The DSP32 device drives into 50 pF with currents of +2.0 mA I_{OL} and –200 μA I_{OH} and still maintains output voltages of 4.0 V (max) V_{OL} and 2.4 V (min) V_{OH}.

RAM Hold Time

The DSP32 device includes an internal mechanism for automatic refresh of the internal RAM. This refresh is always enabled when the device is reset. It consumes 4 periods of CKI every 128 periods, or about 3% of the DSP32 instruction execution time. The refresh can be disabled by setting bit 7 of the PCR register. This is accomplished by using the PIO port subsequent to the reset. If the refresh is disabled, the RAM hold time is guaranteed to be a minimum of 4 ms.

Absolute Maximum Ratings

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

Voltage on any pin with respect to ground ..... –0.5 to +6.5 V
Storage temperature range ..... –65 to +150 °C

Ambient Temperature

The allowable ambient temperature, T_A, in °C can be obtained from the following formula:

$$T_A = T_C - (PD \times \theta_{CA})$$

Where:

T_C = Chip case temperature, °C
PD = Power dissipation, W
θ_{CA} = Thermal resistance, case-to-ambient, °C/W

The maximum ambient temperature for various arrangements with no air flow is given below.

Package Option	PD (W)	θ_{CA} (°C/W)	T_A (°C)
100-pin, PGA:			
with EMI	2.6	19	65
without EMI	2.3	19	71
40-pin DIP:			
no heat sink	2.3	32	41
Aavid 6107 heat sink	2.3	23	62

The maximum allowable ambient temperature can be increased with the use of air flow. The thermal resistance as a factor of air flow is shown in Figure 6. The minimum air flow required for an ambient temperature of 70 °C for various package options is shown below.

Package Option	PD (W)	Air Flow (Ft/Min)
100-pin, PGA:		
with EMI	2.6	80
without EMI	2.3	0
40-pin DIP:		
no heat sink	2.3	370
Aavid 5807 heat sink	2.3	70

Handling Precautions

All MOS devices must be handled with certain precautions in order to avoid damage due to the accumulation of static charge. Although input protection circuitry has been incorporated into the devices to minimize the effect of this static buildup, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting. AT&T employs a human body model and a charged device model for ESD susceptibility testing. Since the failure voltage of electronic devices is dependent on the current and voltage and, hence, the resistance and capacitance, it is important that standard values are employed to establish a reference by which to compare test data. Values of 100 pF and 1500 Ω are the most common and are the values used in the AT&T human body model test circuit. The breakdown voltage for the DSP32 DSP is 900 V, according to the human body model. Test data for the charged device model is available upon request.

Timing Characteristics and Requirements

Device Timing Characteristics and Requirements

V_{DD} = 5 V ± 10% (for 16-MHz part); V_{DD} = 5 V ± 5% (for 25-MHz part); V_{SS} = 0 V; T_C = 0 to 115 °C; C_{LOAD} = 90 pF

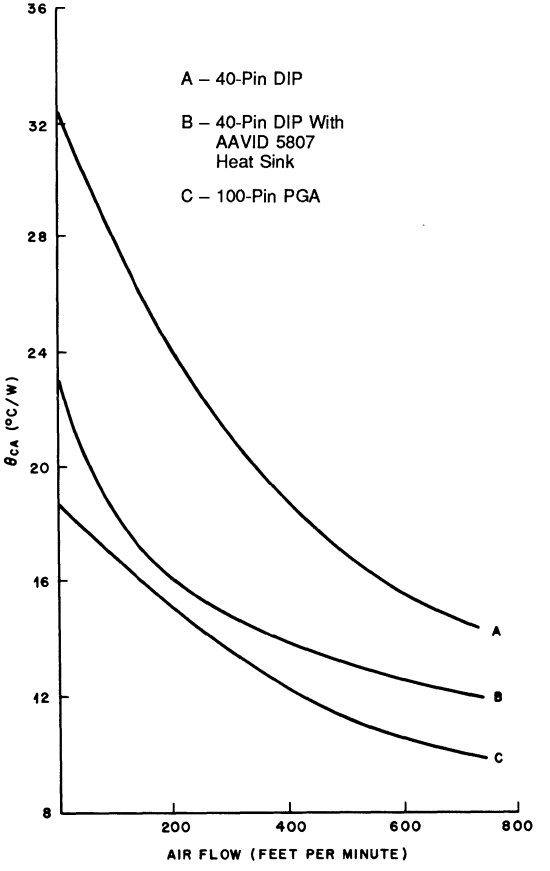


Figure 6. Thermal Resistance

Table 25. Timing Requirements for Clocks (See Figure 7)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Clock in period	tCKILCKIL	61	125	40	125	ns
Clock in low time	tCKILCKIH	27.5	—	18	—	ns
Clock in high time	tCKIHCKIL	27.5	—	18	—	ns

The timing characteristics and requirements for the external memory interfaces of the 16-MHz and 25-MHz parts are specified in different manners. The timing characteristics and specifications for the 16-MHz part are shown in Tables 26—28. The timing characteristics and specifications for the 25-MHz part are shown in Tables 29—31.

Table 26. Direct Timing Characteristics for External Memory Interface (16-MHz Only)

Description	Symbol	Min	Max	Unit	Fig
MGN low delay	tCKILMGNL	10	45	ns	8
MGN high delay	tCKILMGNH	10	45	ns	8
MWN low delay	tCKIHMWNL	15	50	ns	9
MWN high delay	tCKIHMWNH	15	50	ns	9
Clock out low delay	tCKILCKOL	20	55	ns	7
Clock out high delay	tCKIHCKOH	20	55	ns	7
Address valid delay	tCKILAV	20	55	ns	—
Address valid hold	tCKILAX	15	40	ns	—
Data out valid delay	tCKIHDV	—	50	ns	—
Data out hold*	tCKILDZ	30	55	ns	—

* The Z-state termination point is defined as a change of 0.5 V with a load of ± 2 mA.

Table 27. Timing Characteristics for External Memory Interface (16-MHz Only)

Description	Symbol	Min*	Max*	Unit	Fig
Address valid	tAVAX	2T – 20	—	ns	10
Address set-up to read	tAVGL	T – 15	T	ns	10
Address valid to end of read	tAVGH	2T – 15	2T	ns	10
Width of read strobe	tGLGH	T – 10	T + 10	ns	10
Address set-up to write	tAVWL	θL – 25	θL	ns	11
Address valid to end of write	tAVWX	T + θL – 25	T + θL	ns	11
Data set-up to write	tDVWH	T – 25	—	ns	11
Data hold after write**	tWHDZ	θH	—	ns	11
Width of write strobe	tWLWH	T – 10	T + 10	ns	11

* T = tCKILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL.
** The Z-state termination point is defined as a change of 0.5 V with a load of ± 2 mA.

Table 28. Timing Requirements for External Memory Interface (16-MHz Only)

Description	Symbol	Min	Max*	Unit	Fig
Address access	tAVDV	—	2T – 40	ns	10
Data enable	tGLDV	—	T – 20	ns	10
Data set-up	tDVGH	10	—	ns	10
Data disable	tGHDZ	0	θL	ns	10

* T = tCKILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL.

Table 29. Direct Timing Characteristics for External Memory (25-MHz Only)

Description	Symbol	Min	Max	Unit	Fig
MGN low delay	tCKILMGNL	—	35	ns	8
MGN high delay	tCKILMGNH	—	40	ns	8
MWN low delay	tCKIHMWNL	—	40	ns	9
MWN high delay	tCKIHMWNH	—	40	ns	9

Table 30. Timing Characteristics for External Memory (25-MHz Only)

Description	Symbol	Min*	Max*	Unit	Figure
Address set-up to read	tAVGL	T – 15	—	ns	12
Address hold after read	tGHAX	– 15	—	ns	12
Width of read strobe	tGLGH	T – 10	—	ns	12
Address set-up to write	tAVWL	θL – 17	—	ns	13
Address hold after write	tWHAX	0	—	ns	13
Data set-up to write	tDVWH	T – 20	—	ns	13
Data hold after write**	tWHDZ	θH	θH + 20	ns	13
Width of write strobe	tWLWH	T – 10	—	ns	13

* T = tCHILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL.
** The Z-state termination point is defined as a change of 0.5 V with load of ± 2 mA.

Table 31. Timing Requirements for External Memory (25-MHz Only)

Description	Symbol	Min	Max*	Unit	Figure
Address access	tAVDV	—	2T – 30	ns	12
Data enable	tGLDV	—	T – 17	ns	12
Data set-up	tDVGH	10	—	ns	12
Data hold	tGHDX	–10	—	ns	12
Data disable	tGHDZ	—	θL	ns	12

* T = tCKILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL.

Summary of Timing Characteristics for External Memory Interface

To assist in selecting memory devices, the following table summarizes the ac characteristics that must be met by memory devices connected to the DSP32 memory interface.

Table 32. Timing Characteristics for External Memory Interface

Description	16 MHz*	25 MHz*
Read Cycle:		
Read cycle time tAVAX	2T – 20 102 ns (min)	2T – 17 63 ns (min)
Address valid to data valid tAVDV	2T – 40 82 ns (max)	2T – 30 50 ns (max)
Chip select**	2T – 40 82 ns (max)	2T – 30 50 ns (max)
Read pulse width tGLGH	T – 10 51 ns (max)	T – 10 30 ns (max)
Output enable low to output valid tGLDV + tDVGH	T – 20 41 ns (max)	T – 17 23 ns (max)
Output enable high to output high-Z (hold time) tGHDZ	θL 27.5 ns (max)	θL 18 ns (max)
Write Cycle ($\overline{W}$ Controlled):		
Write cycle time tAVAX	2T – 20 102 ns (min)	2T – 17 63 ns (min)
Address valid to end of write tAVWX	T + θL – 25 63.5 ns (min)	T + θL – 17 41 ns (min)
Write pulse width tWLWH	T – 10 51 ns (min)	T – 10 30 ns (min)
Data valid to end of write tDVWH	T – 25 36 ns (min)	T – 20 20 ns (min)
Data hold time	θH 27.5 ns (min)	θH 18 ns (min)

* T = tCKILCKIL (clock in period).
θL = tCKILCKIH (clock in low time).
θH = tCKIHCKIL (clock in high time).
** Same as address access time, assuming MSN0—MSN3 are connected to CS.

Table 33. Timing Requirements for Serial Inputs (See Figure 12)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Clock period	tICKLICKL	122	1000	80	1000	ns
Clock low time	tICKLICKH	50	—	35	—	ns
Clock high time	tICKHICKL	50	—	35	—	ns
Load high set-up	tILDHICKH	40	—	25	—	ns
Load high hold	tICKHILDL	0	—	0	—	ns
Load low set-up	tILDLICKH	40	—	25	—	ns
Load low hold	tICKHILDH	0	—	0	—	ns
Data set-up	tDIVICKH	35	—	25	—	ns
Data hold	tICKHDIX	0	—	0	—	ns

Table 34. Timing Characteristics for Serial Input (See Figure 12)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Input buffer delay	tICKHIBFH	—	75	—	50	ns

Table 35. Timing Requirements for Serial Output (See Figure 15)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Clock period	tOCKLOCKL	122	1000	80	1000	ns
Clock low time	tOCKLOCKH	50	—	35	—	ns
Clock high time	tOCKHOCKL	50	—	35	—	ns
Load high set-up	tOLDHOCKH	40	—	25	—	ns
Load high hold	tOCKHOLDL	0	—	0	—	ns
Load low set-up	tOLDLOCKH	40	—	25	—	ns
Load low hold	tOCKHOLDH	0	—	0	—	ns

Table 36. Timing Characteristics for Serial Output (See Figure 15)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Data delay	tOCKHDOV	—	50	—	35	ns
Data hold	tOCKHDOX	5	—	3	—	ns
Output buffer empty delay	tOCKHOBEH	—	75	—	50	ns
Output shift register delay	tOCKHOSEH	—	75	—	50	ns
Enable delay	tOENLDOV	—	100	—	65	ns
Disable delay*	tOENHDOZ	—	100	—	65	ns

* The Z-state termination point is defined as a change of 0.5 V with a load of ± 2 mA.

Serial I/O (SIO) Timing Characteristics and Requirements

Table 37. Timing Requirements for Serial Clock Generation* (See Figure 16a)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
SY high set-up	tSYHICKH tSYHOCKH	35	—	25	—	ns
SY high hold	tICKHSYL tOCKHSYL	0	—	0	—	ns
SY low set-up	tSYLICKH tSYLOCKH	35	—	25	—	ns
SY low hold	tICKHSYH tOCKHSYH	0	—	0	—	ns

* ICK or OCK is selected by IOC[BC].

Table 38. Timing Characteristics for Serial Clock Generation (See Figures 16a, b, and c)

Description	Symbol	16 MHz		25 MHz		Unit	Fig
		Min	Max	Min	Max		
Internal SY delay*	tICKHSYL tOCKHSYL	—	75	—	50	ns	16b
Internal load delay*	tICKHILDL tOCKHOLDL	—	85	—	60	ns	16b
Internal load/SY delay	tSYLILDL tSYLOLDL	—	50	—	35	ns	16a
Clock period**	tICKHICKH tOCKHOCKH	488	1000	320	1000	ns	16c
Clock low time	tICKLICKH tOCKLOCKH	220	—	144	—	ns	16c
Clock high time	tICKHICKL tOCKHOCKL	220	—	144	—	ns	16c

* ICK or OCK is selected by IOC[BC].
** tICKHICKH and tOCKHOCKH are tCKIHCKIH * 8.

Parallel I/O (PIO) Timing Characteristics and Requirements

Table 39. Timing Requirements for PIO Read Cycle* (See Figure 17)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Address set-up	tPAVPRL	25	—	15	—	ns
PACK set-up	tPACKHPRL	25	—	15	—	ns
Address hold	tPRHPAX	0	—	0	—	ns
PACK hold	tPRHPACKL	0	—	0	—	ns

* A minimum 200-ns interval is required for the start of the read or write cycle following the end of the previous read or write cycle.

Table 40. Timing Characteristics for PIO Read Cycle (See Figure 17)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Access from read*	tPRLPDV	—	100	—	65	ns
Data hold from read**	tPRHPDZ	10	70	—	50	ns

* Read access time is for 150-pF loading on the PDB. With 200-pF loading, the maximum read access time is 130 ns.
** The Z-state termination point is defined as a change of 0.5V with a load of ± 2 mA and 200-pF loading on the PDB.

Table 41. Timing Requirements for PIO Write Cycle* (See Figure 18)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Address set-up	tPAVPWL	25	—	15	—	ns
Address hold	tPWHPAX	0	—	0	—	ns
Write pulse	tPWLPWH	80	—	55	—	ns
Data set-up	tPDVPWH	50	—	35	—	ns
Data hold	tPWHPDX	0	—	0	—	ns

* A minimum 200-ns interval is required for the start of the read or write cycle following the end of the previous read or write cycle.

Table 42. Timing Characteristics for PDF and PINT (See Figures 17 and 18)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
PDF write delay	tPWHPDFH	—	120	—	85	ns
PDF read delay	tPRLPDFL	—	120	—	85	ns
PINT read delay	tPRLPINTL	—	150	—	105	ns
PINT read delay	tPRHPINTL	—	150	—	105	ns

Reset Timing Characteristics and Requirements

When the DSP32 device is powered-up, the dynamic RAM access strobes must be established before internal RAM accesses can be guaranteed. This can be accomplished in one of two ways. If the RAM autorefresh is enabled for a sufficient length of time (512 X tCKILCKIL) before the first internal RAM access, the refresh mechanism establishs the access strobes; otherwise, it is recommended that the DSP32 application program perform four dummy reads of each 512-word bank of internal RAM to establish the access strobes. This recommendation also applies to applications where PIO DMA transfers to internal DSP32 RAM occur after reset.

The DSP32 device can be reset and halted by using either the PCR register or the RESTN pin. The PCR register is externally controlled through the PIO port.

Reset Using the PCR Register. With the RESTN input high, the DSP32 device is halted by writing PCR0 = 0. It must remain halted for at least 22 periods of CKI (T). To bring the device out of halt and then begin execution, set PCR = 0x80, followed by PCR = 0x81. The other PCR bits can be set or cleared according to the application requirements. The timing requirements for the PCR writes are provided in Figure 16.

Reset Using the RESTN Pin. The sequence required to initialize and run the DSP32 device is shown in Figure 17. The first low-to-high transition is required to initialize internal DSP32 registers. The next transition causes the DSP32 to begin execution. The valid address (all low) to the first instruction appears on the external address bus after the time interval. Note that, if the device is reset by using RESTN, the PCR0 = 0 half is overridden and PCR0 is set (PCR1—PCR7 are cleared) after the first low-to-high transition of RESTN. SIO DMA can not be enabled during the first four instruction cycles.

At any time after the initial power-up sequence, the device can be halted by a high-to-low transition of RESTN (see Figure 18). If the user wishes all instructions in the progress to execute to completion, the DSP32 must remain halted for at least 22 periods of CKI(T). The PIO port and the internal RAM refresh mechanism are active during halt. After halt, a single low-to-high transition of RESTN is sufficient to restart the DSP32 device at the first instruction.

Table 43. Reset Timing Requirements for RESTN (See Figures 17 and 18)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
RESTN low set-up	tRSTLCKIH	0	θL	0	θL	ns
RESTN high set-up	tRSTHCKIH	0	θL	0	θL	ns
Interval to PC = 0	tSTART	7T + 20	7T + 55	7T + 13	7T + 37	ns
First RESTN low	tRLOW1	T	—	T	—	ns
First RESTN high	tRHIGH1	T	4T	T	4T	ns
Second RESTN low	tROWL2	22T	100T	22T	100T	ns

* T = tCKILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL .

Timing Diagrams

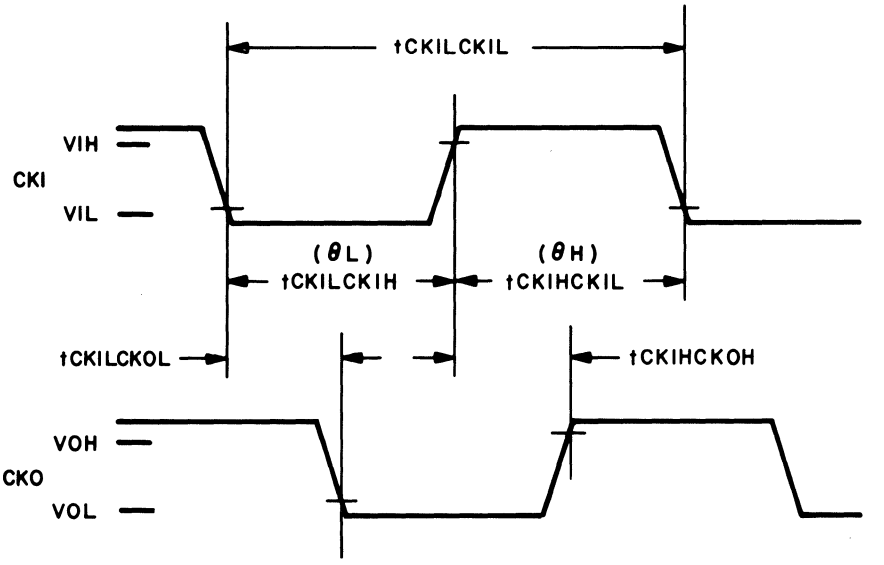


Figure 7. Clocks

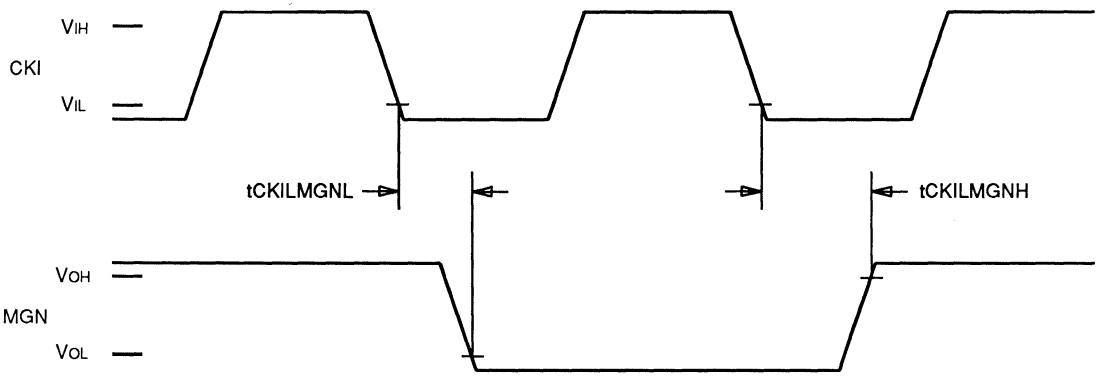


Figure 8. MGN Direct Timing

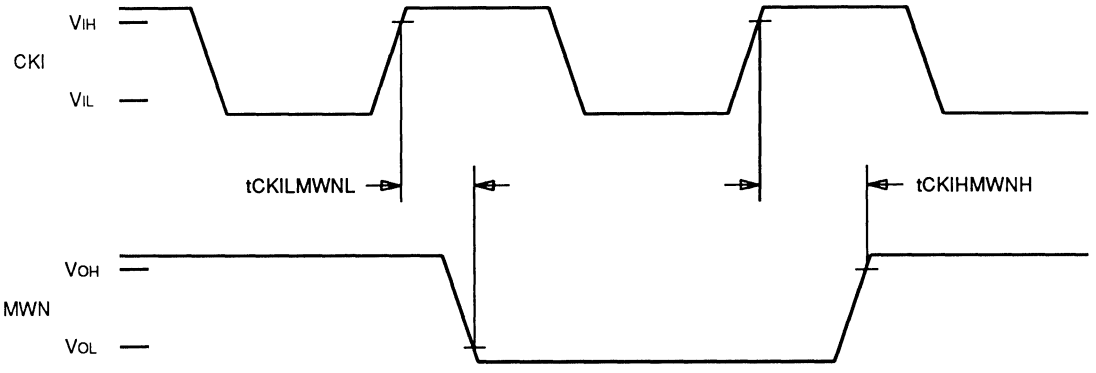


Figure 9. MWN Direct Timing

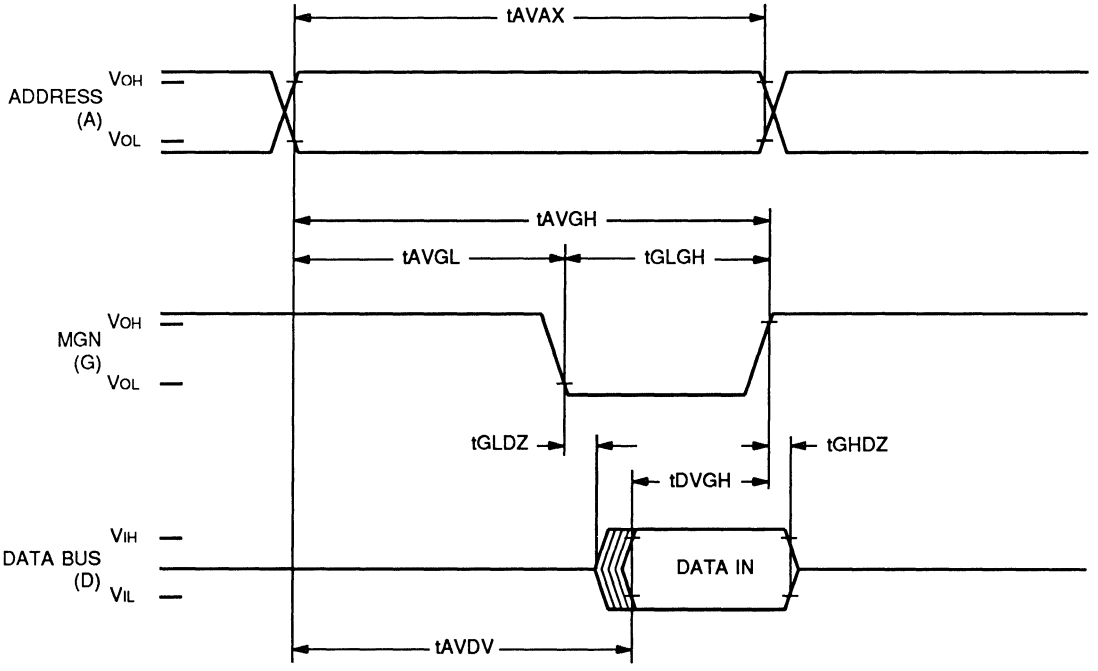


Figure 10. External Memory Read Cycle for 16-MHz Device

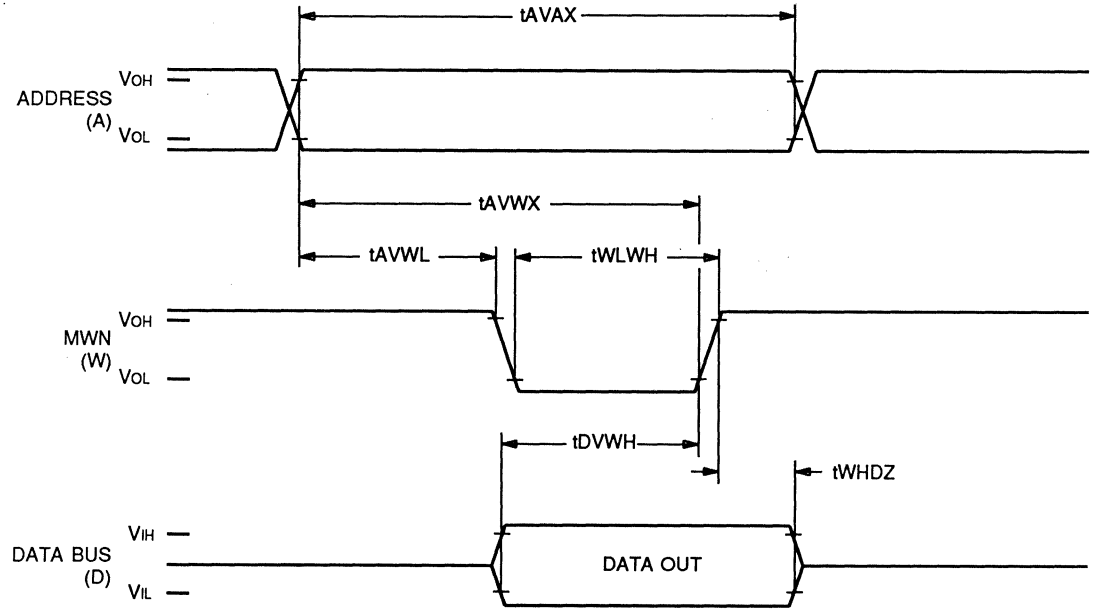


Figure 11. External Memory Write Cycle for 16-MHz Device

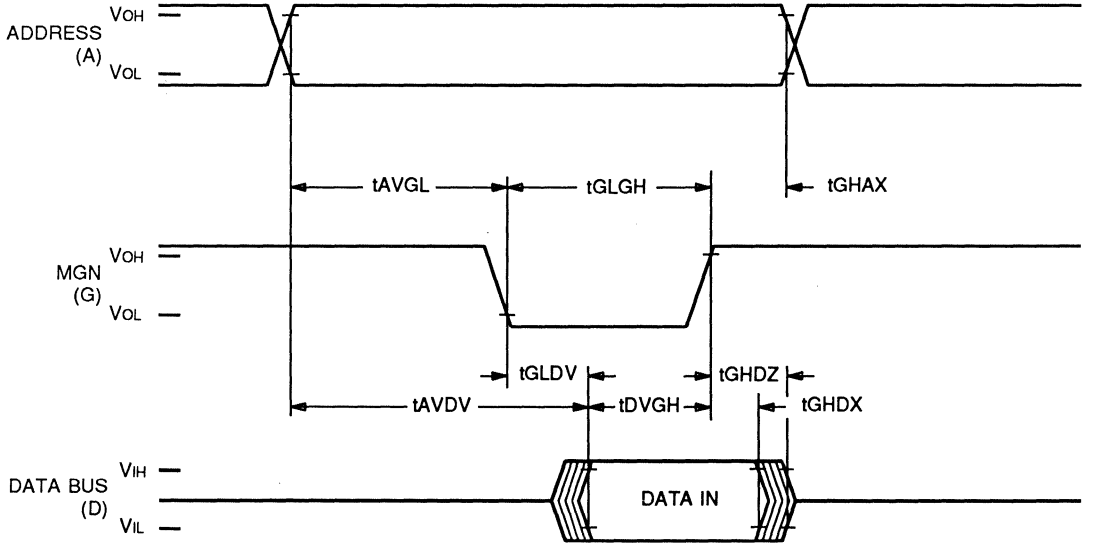


Figure 12. External Memory Read Cycle for 25-MHz Device

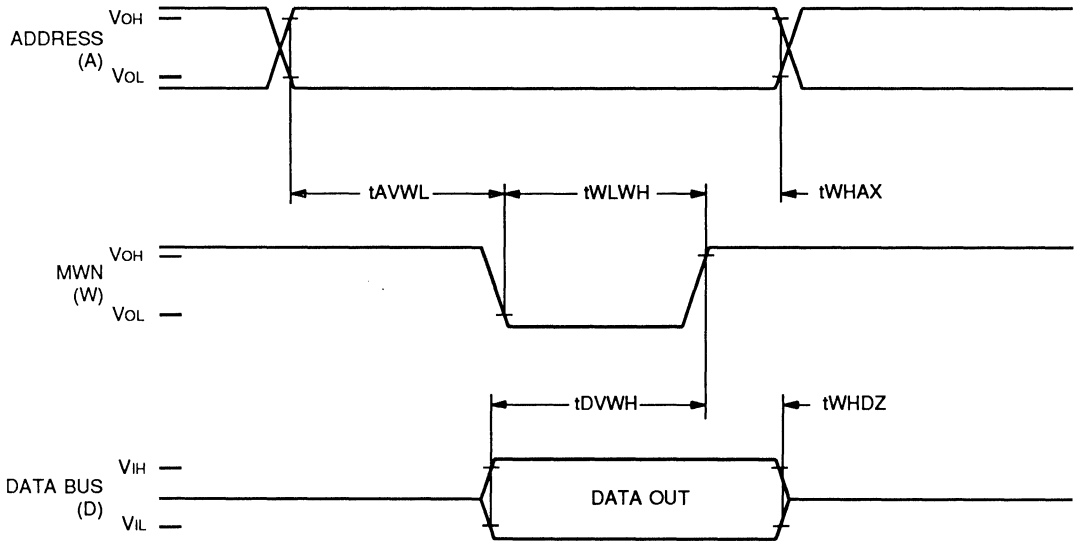


Figure 13. External Memory Write Cycle for 25-MHz Device

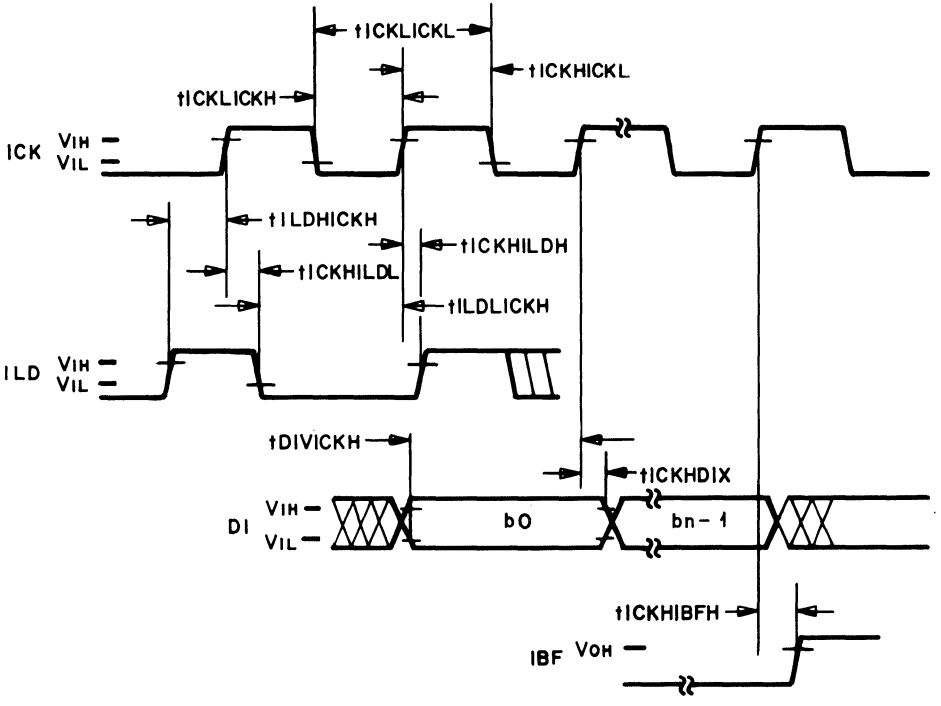


Figure 14. Serial Input Timing

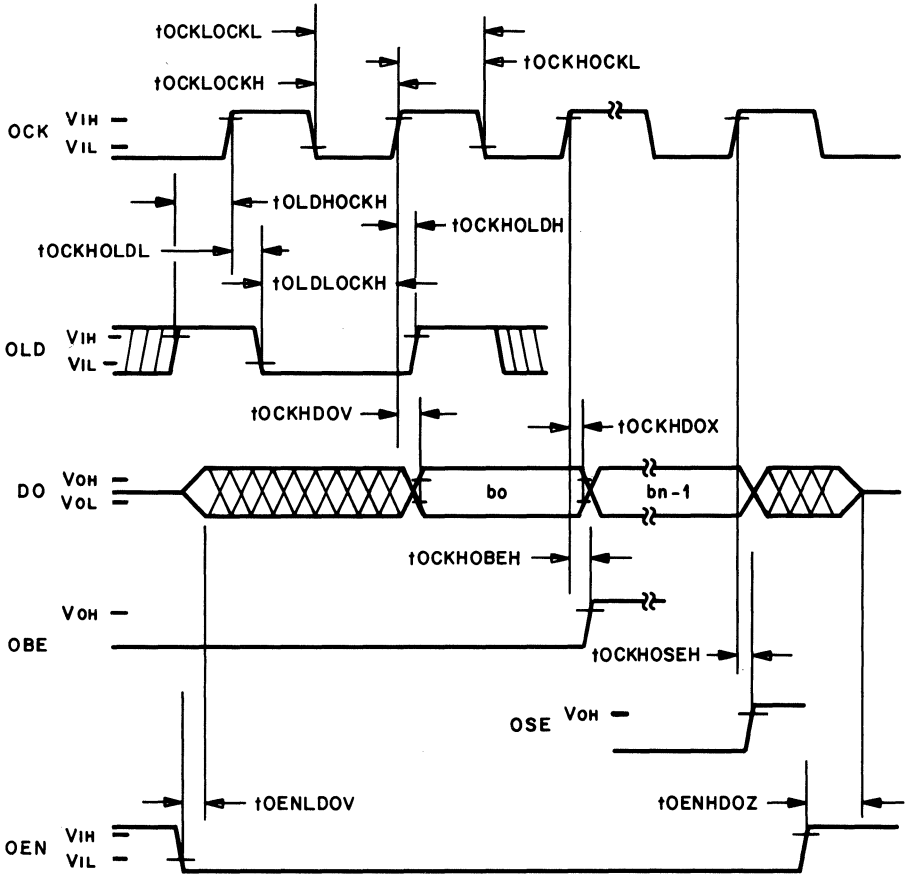
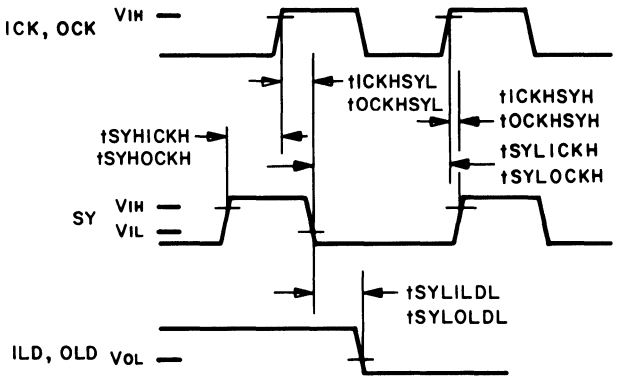
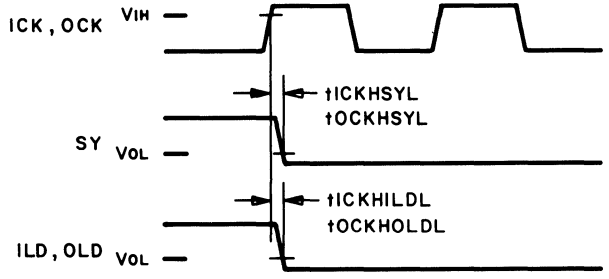


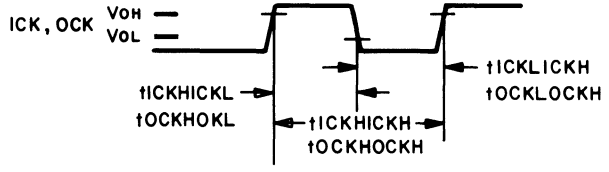
Figure 15. Serial Output Timing



A. External SY, ICK/OCK. Internal ILD/OLD

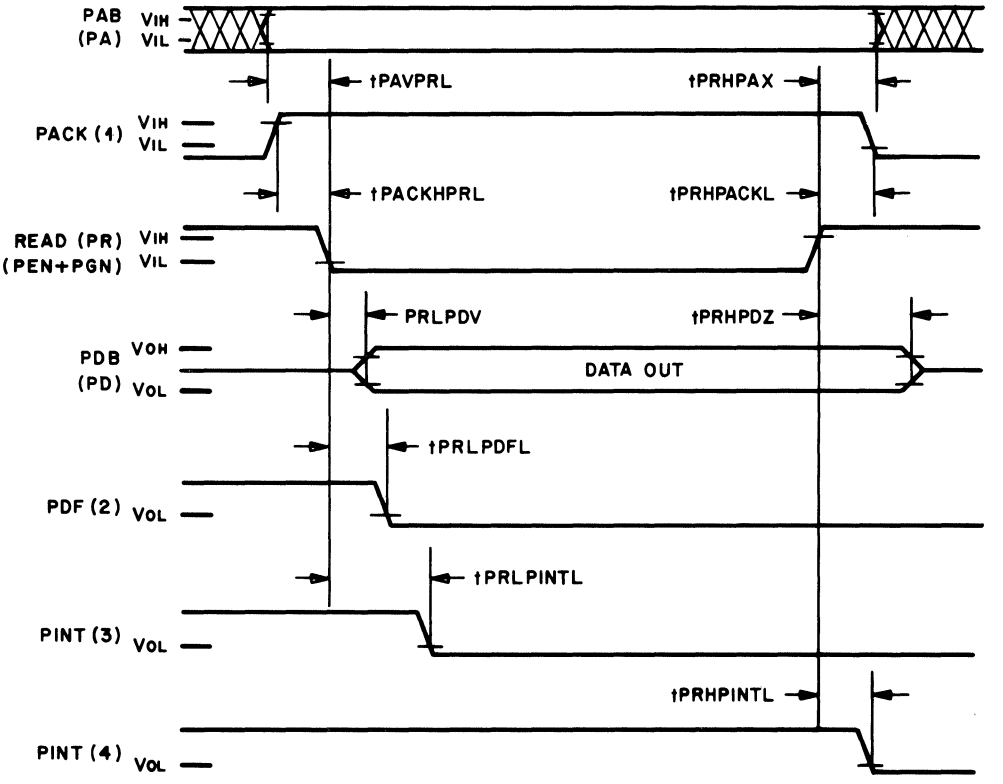


B. Internal ILD/OLD/SY. External ICK/OCK



C. Internal ICK/OCK

Figure 16. I/O Clock Generation Timing



1 PACK used only for PIR read. To read other registers, PACK must be 0.
2 PDF changes only on PAB = 3.
3 PINT changes for the PIR read (if PINT = 1 is caused by loading of the PIR).
4 PINT changes for the ESR read (if PINT = 1 is due to unmasked error).

Figure 17. PIO Timing — Read Cycle

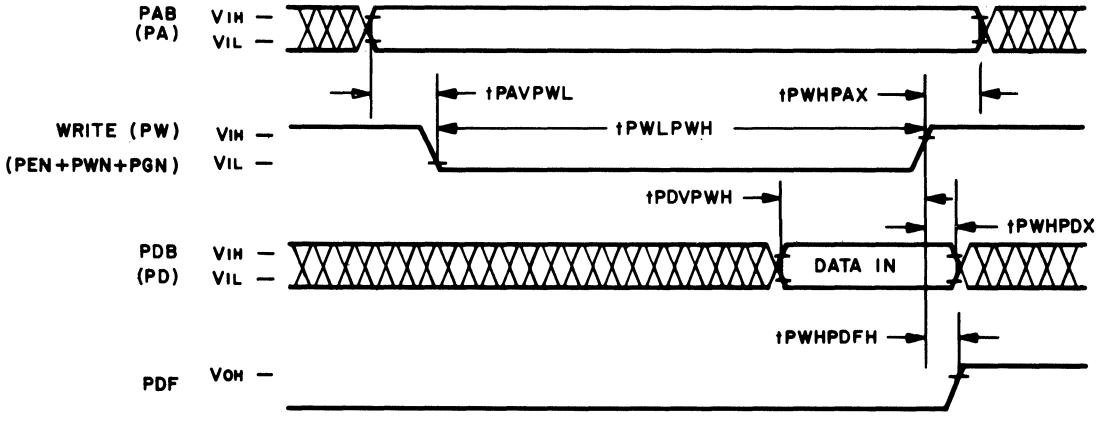


Figure 18. PIO Timing — Write Cycle (PGN High)

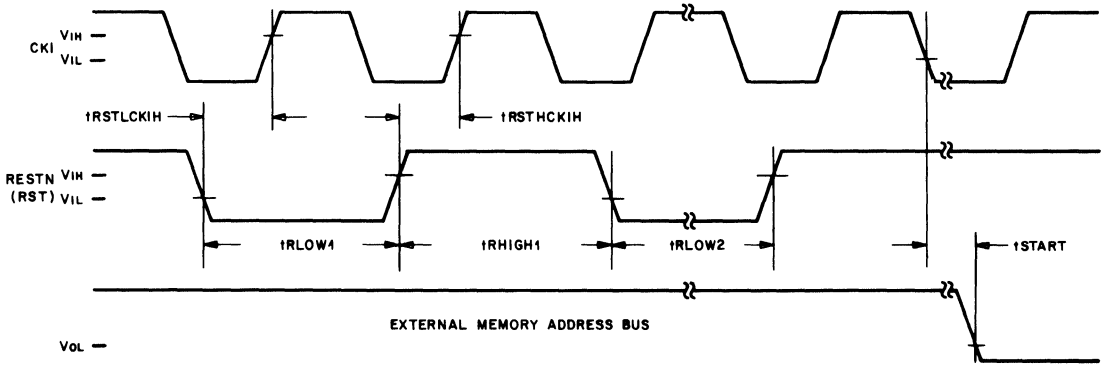


Figure 19. RESTN Initialization Sequence

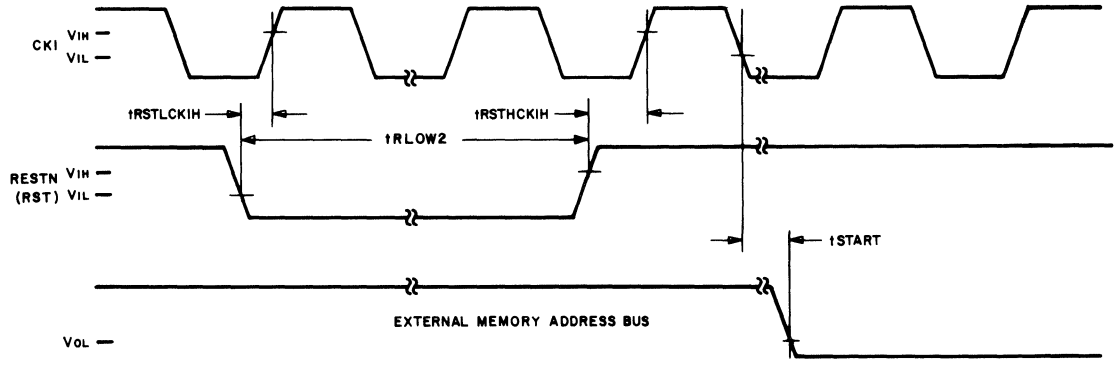


Figure 20. RESTN Halt

WE DSP32C Digital Signal Processor

Features

- 80-ns instruction cycle (50-MHz clock)
- Zero-overhead looping
- 32-bit floating-point arithmetic
- Single-precision IEEE floating-point compatibility
- Four 40-bit accumulators
- Four memory accesses per instruction cycle
- ROM-less device with 6144 bytes of on-chip RAM
- ROM-coded device with 4096 bytes of RAM and 8192 bytes of mask-programmed ROM
- Up to 16 Mbytes of external memory
- Memory can be addressed as 8, 16, or 32 bits
- 16- and 24-bit integer operations
- 16 Mbit/s serial input and output ports with DMA options
- 8- or 16-bit microprocessor interface requiring no additional logic
- Internal and external interrupts
- Error control logic
- Secure ROM
- Carry with reverse add for efficient Fast Fourier Transform implementations
- Support tools include the *WE* DSP32C-CC C Language Compiler, the *WE* DSP32C-SL Support Software Library, and the *WE* DSP32C-DS DSP Development System

Description

The *WE* DSP32C Digital Signal Processor (DSP) is the newest member of AT&T's family of 32-bit floating-point DSPs. It is the right choice for applications requiring floating-point arithmetic, high-throughput, and large amounts of memory. The DSP32C is fabricated in CMOS technology and is upward compatible with the *WE* DSP32 Digital Signal Processor; source code, object code, pin function, and timing specifications (from the DSP32) have been preserved in the DSP32C device. Enhancements include higher operating frequency, lower power requirements, larger external address space, and a hardware interrupt facility.

DSP32 and DSP32C Support

A variety of tools are available to aid in application program development for devices in the DSP32 family of DSPs. The software tools, which run under either the *UNIX* Operating System or the *MS-DOS* Operating System, can be used for both the DSP32 and DSP32C processors. The hardware development systems are specific to each processor.

***WE* DSP32-CC C Language Compiler.** The optimizing C language compiler for the DSP32 family allows application programs to be written in a general high-level language. In applications where preliminary program development is performed by using a high-level language such as C, Fortran, or Pascal, the source-code can be ported to the DSP32C with a minimal amount of time and effort. (Utilities to translate source-files from Fortran or Pascal to C are commercially available.) A symbolic debugger and several libraries of commonly-used arithmetic and signal processing functions are included with the compiler.

***WE* DSP32-SL Support Software Library.** Software tools used to create, test, and debug DSP32C application programs at the assembly language level are included in the DSP32-SL Support Software Library. An assembler, link editor, simulator, and other utilities are also included. The simulator, which has such capabilities as single-stepping, breakpointing, and execution profiling, performs precise simulations of the device – including the timing of synchronous I/O. Program debugging is aided by access to all registers and memory during a simulation. The simulator also serves as an interface to the DSP32C-DS Development System.

***WE* DSP32-AL Application Software Library.** A comprehensive library of commonly-used routines provides efficient, fully-tested, and easy to use routines that can be incorporated without modification into application programs or that can be modified to serve a more specific function. The library routines can be used with both assembly and C language programs. (The library is included with the C compiler.) Most routines include different versions to provide flexibility for dealing with memory and/or speed constraints. Routines are included for the following general topics: arithmetic, matrix arithmetic, filtering, adaptive filtering, FFTs, and graphics/image processing.

***WE* DSP32-DS Development System.** The development system is a single-board unit that supports the features of the software simulator (such as breakpoints) and allows application programs to be run in real-time on a DSP32 device with the same user interface as the software simulator. Up to seven systems can be cascaded to support multiple DSP systems. The development system also allows in-circuit emulation of the application hardware.

***WE* DSP32C-DS Development System.** A personal computer, the DSP32C-DS Development System, and the DSP32-SL Support Software Library form a powerful application development environment. The development system is a PC card that supports the features of the software simulator (such as breakpoints) and allows application programs to be run in real-time on a DSP32C device with the same user interface as the software simulator. Additional hardware modules allow expansion of the DSP32C device memory, in-circuit emulation of application hardware, and development of multi-DSP systems.

7. Application and Technical Note Summaries

The following are abstracts of available application and technical notes. Following the note title is the document identification number. To receive a copy of any note described in these abstracts, contact your AT&T Account Manager or call:

1-800-372-2447

Application Notes

AN-10 Digital Multiplexed Interface Implementation (AP84-33 CMOS)

The AN-10 application note provides a description of the DS1 chip set and its use in a digital multiplexed interface (DMI). DMI provides twenty-three 64-kb/s data channels and a 64-kb/s channel for common-channel signaling. It also provides several data transport formats and supports data rates up to 64 kb/s.

The DS1 chip set, two transformers, and various generations of integrated circuits provide the physical interface for multiplexed data communications over digital facilities between a host computer and a PBX. The device set consists of a T7229 or 229GB Framer, 229FB Maintenance Buffer, 257AL Transmit Formatter, 257AU Receive Synchronizer, 630AG/630AJ Receive Converter, and 606HM Transmit Converter.

A description of the signal path through the devices and the interfacing requirements needed for both the line side and the host system end are provided in the AN-10 application note. Timing generation circuits for the DS1 devices are also presented.

AN-13 RS-232C Compatible Date Encryption Unit (AP86-36 SMOS)

The AN-13 application note describes the design and operation of a low-cost, RS-232C compatible, data encryption unit (DEU) used to encrypt or decrypt digital data. The design of the DEU is based on the AT&T T7000A Digital Encryption Processor (DEP) and the AT&T T7001 Random Number Generator (RNG).

Many advanced electronic communication systems use an unprotected public medium as the communication link between users. These systems are easy to access and can be broken into by an unauthorized user for the purpose of eavesdropping or tampering with the data being sent on the line. The main function of the DEU is to provide secure data communication over a nonsecured public communications link. This is accomplished by encrypting the data before transmission.

The National Bureau of Standards has defined a format for encryption called the Data Encryption Standard (DES). Communication systems that use the DES provide a reasonably high level of security. The T7000A DEP is a high-speed hardware implementation of the DES. In addition to implementing the four DES modes, this programmable device allows multiple or multiplexed ciphering, or the user may program his own unique encryption method. The T7001 RNG generates a truly random (not pseudorandom) output that can be used as encryption keys or initial values.

An overview of both the T7000A and T7001 devices is presented and a description of the DEU and its operation is provided in detail. The AN-13 application note appendices contain all the information needed for this project.

AN-15 Configuring the T7100 X.25 Protocol Controller (XPC-8) (AP86-33 SMOS)

The T7100A X.25 Protocol Controller integrated circuit is an X.25 level 2 protocol controller (XPC-8). It implements the balanced link access procedure (LAPB) for data interchange over a synchronous full-duplex link as defined in the X.25 protocol. The XPC-8 is in compliance with CCITT X.25 1980 and ISO 7776 (at the Draft International Standard [DIS] level). The protocol controller is byte-oriented, with a maximum transmit and receive data rate of 250 kb/s.

The XPC-8 is configured for a specific X.25 application by writing appropriate values for the system parameters into the parameter registers when the XPC-8 is in a set-up state.

The AN-15 application note contains information needed to perform the initialization of the XPC-8. It describes the architecture of the device, different operating modes, major features, and typical initialization code in C language.

AN-16 Polled and Interrupt Mode Operations of the T7111 Synchronous Packet Data Formatter (AP86-34 SMOS)

The AT&T T7111 Synchronous Packet Data Formatter (ANT) integrated circuit is used to interface serial data link level lines by using high-level data link control (HDLC) bit-synchronous protocol with 8-bit microprocessor or microcontroller systems. The ANT is a single-channel, full-duplex, packet data formatter. It has a programmable register set to configure both host and serial link interfaces.

The AN-16 application note contains information needed to utilize the ANT in a variety of system environments. It describes the major features, architecture of the device, and the operation and typical system applications of the T7111 ANT when used in the polled and interrupt modes.

AN-18 DMA Mode Operation of the T7111 Synchronous Packet Data Formatter (AP86-46 SMOS)

The AT&T T7111 Synchronous Packet Data Formatter (ANT) integrated circuit is used to interface serial data link level lines by using high-level data link control (HDLC) bit-synchronous protocol with 8-bit microprocessor or microcontroller systems. The ANT is a single-channel, full-duplex, packet data formatter. It has a programmable register set to configure both host and serial link interfaces.

The AN-18 application note contains information needed to utilize the ANT in a variety of system environments. It describes the major features, architecture of the device, and the operation and typical system applications of the T7111 ANT when used with a 8237 or 8257 DMA Controller.

Technical Notes

Interfacing the T7110 SPYDER-S to a DS1 Signal (TN86-095 SMOS)

This technical note discusses guidelines for interfacing the AT&T T7110 Synchronous Protocol Data Formatter with Serial Interface (SPYDER-S) to a T1/DS1 line at a 1.544 Mb/s serial data rate. Such an interface is required in a digital multiplexed interface (DMI) application or in an ISDN primary rate user-network interface.

229GB Framer Functions for DMI Applications (TN86-07 SMOS)

This technical note describes the functions of the 229GB Framer that are available for digital multiplexed interface (DMI) applications.

The 229GB Framer provides line and frame format interfaces for domestic digital carrier systems. The framer performs in-line and off-line framing functions in both receive and transmit directions.

The 229GB Framer can be used as an alternative to the T7229 Framer. The 229GB and T7229 Framers are designed for use with the 257AL Transmit Formatter, the 257AU Receive Synchronizer, and the 229FB Maintenance Buffer. Both framers are pin-compatible and, except for the 2.048-Mb/s CEPT TDM format provided by the T7229 Framer, have the same non-DMI capabilities. Additionally, the 229GB Framer provides DMI mode options that are not available with the T7229 Framer.

8. Package Information

Throughout this section the following abbreviations are used:

DIP – Dual in-line package
SOJ – Small outline J-lead
SOIC – Small outline gull wing
PLCC – Plastic leaded chip carrier
PGA – Pin grid array

Table 1. Communication Devices by Device Number

Device	Name	Package	Figure
41LF	Quad Differential Line Receiver	16-pin plastic SOJ	3
1041LF		16-pin plastic DIP	1
1141LF		16-pin plastic SOIC	3
41LG	Quad Differential Line Driver	16-pin plastic SOJ	3
1041LG		16-pin plastic DIP	1
1141LG		16-pin plastic SOIC	3
41LK	Dual Differential Line Driver/Receiver Pairs	16-pin plastic SOJ	3
1041LK		16-pin plastic DIP	1
1141LK		16-pin plastic SOIC	3
41LL	Dual Differential Line Driver/Receiver Pairs	16-pin plastic SOJ	3
1041LL		16-pin plastic DIP	1
1141LL		16-pin plastic SOIC	3
41LM	Dual Differential Line Driver/Receiver Pairs	16-pin plastic SOJ	3
1041LM		16-pin plastic DIP	1
1141LM		16-pin plastic SOJ	3
229FB	Maintenance Buffer	40-pin plastic DIP	1
229GB	Framer	40-pin ceramic nonhermetic DIP	2
257AL	Transmit Formatter	32-pin plastic DIP	1
257AU	Receive Synchronizer	32-pin plastic DIP	1
606HM	Transmit Converter	40-pin ceramic HIC DIP	4
630AG	Receive Converter	20-pin ceramic HIC DIP	4
630AJ	Receive Converter	20-pin ceramic DIP	2
T7000A-PC	Digital Encryption Processor	40-pin plastic DIP	1
T7001-PC	Random Number Generator	32-pin plastic DIP	1

Table 1. Communication Devices by Device Number (Continued)

Device	Name	Package	Figure
T7002-MC	Bit Slice Multiplier (BSM)	68-pin PLCC	6
T7003-MC		68-pin PLCC	6
T7032-PC	Clock Recovery Circuit	20-pin plastic DIP	1
T7033-PC	Clock Recovery Circuit	20-pin plastic DIP	1
T7034-PC	Clock Recovery Circuit	20-pin plastic DIP	1
T7100A-BC	X.25 Protocol Controller	48-pin ceramic DIP	2
T7102A-RC	X.25/X.75 Protocol Controller	70-pin ceramic PGA	7
T7110-MC	Synchronous Protocol Data Formatter with Serial Interface (SPYDER)	68-pin PLCC	6
T7111A-EC	Synchronous Packet Data Formatter (ANT)	28-pin plastic SOJ	3
T7111A-PC		28-pin plastic DIP	1
T7112-EC	Asynchronous Receive/ Transmit Interface (ARTI)	28-pin plastic SOJ	3
T7112-PC		24-pin plastic DIP	1
T7115-MC	Synchronous Protocol Data Formatter (SPYDER-T)	68-pin PLCC	6
T7229-PC	Primary Access Framer	40-pin plastic DIP	1
T7250A-MC	User Network Interface for Terminal Equipment (UNITE)	44-pin PLCC	5
T7250A-PC		40-pin plastic DIP	1
T7252-MC	ISDN Basic Access User Network Interface Termination for Switches (UNITS)	44-pin PLCC	5
T7252-PC		40-pin plastic DIP	1
T7260-MC	U-Interface Basic Access Transceiver Chip Set (Analog)	44-pin PLCC	5
T7261-MC	U-Interface Basic Access Transceiver Chip Set (Digital)	44-pin PLCC	5
T7274-EC	Quad Differential Line Driver	16-pin plastic SOJ	3
T7274-PC		16-pin plastic DIP	1
T7275-EC	Quad Differential Line Receiver	16-pin plastic SOJ	3
T7275-PC		16-pin plastic DIP	1
T7500-EC	PCM Codec with Filters	20-pin plastic SOJ	3
T7500-PC		18-pin plastic DIP	1
T7512-EC	Dual PCM Codec with Filters	28-pin plastic SOJ	3
T7512-PC		28-pin plastic DIP	1
T7513-EC	PCM Codec with Filters	20-pin plastic SOJ	3
T7513-PC		20-pin plastic DIP	1

Table 1. Communication Devices by Device Number (Continued)

Device	Name	Package	Figure
T7513A-EE	PCM Codec with Filters	20-pin plastic SOJ	3
T7513A-PE		20-pin plastic DIP	1
T7520-CC	High-Precision PCM Codec with Filters	24-pin ceramic DIP	2
T7521-CC	High-Precision PCM Codec without Filters	24-pin ceramic DIP	2
T7522-CC	High-Precision PCM Codec with Filters	24-pin ceramic DIP	2
T7523-CC	High-Precision PCM Codec with Filters	24-pin ceramic DIP	2
LC1046-AM	Digital Signal Interface	28-pin plastic SOJ	3
LC1046-AG		28-pin plastic DIP	1
LC1135-BM	Digital Signal Interface	28-pin plastic SOJ	3
LC1135-BG		28-pin plastic DIP	1
DSP16	*WE* DSP16 Digital Signal Processor	84-pin PLCC	8
		133-pin ceramic PGA	10
DSP32	*WE* DSP32 Digital Signal Processor	100-pin-ceramic PGA	9
		40-pin ceramic DIP	2
DSP32C	*WE* DSP32C Digital Signal Processor	133-pin ceramic PGA	10

Table 2. Communication Devices by Number of Pins

Pins	Package	Device	Figure
16	Plastic DIP	T7274-PC, T7275-PC, 1041LF, 1041LG, 1041LK, 1041LL, 1041LM	1
	Plastic SOJ	T7274-EC, T7275-EC, 41LF, 41LG, 41LK, 41LL, 41LM	3
	Plastic SOIC	1141LF, 1141LG, 1141LK, 1141LL, 1141LM	3
18	Plastic DIP	T7500-PC	1
20	Plastic DIP	T7032-PC, T7033-PC, T7034-PC, T7513-PC, T7513A-PE	1
	Plastic SOJ	T7500-EC, T7513-EC, T7513A-EE	3
	Ceramic HIC DIP	630AG, 630AJ	4
24	Plastic DIP	T7112-PC	1
	Ceramic DIP	T7520-CC, T7521-CC, T7522-CC, T7523-CC	2
28	Plastic DIP	T7111A-PC, T7512-PC, LC1046-AG, LC1135-BG	1
	Plastic SOJ	T7111A-EC, T7112-EC, T7512-EC, LC1046-AM, LC1135-BM	3
32	Plastic DIP	257AL, 257AU	1
40	Plastic DIP	T7000A-PC, T7229-PC, T7250A-PC	1
	Ceramic DIP	229GB, DSP32	2
	Ceramic HIC DIP	606HM	4
44	PLCC	T7250A-MC, T7252-MC, T7260-MC, T7261-MC	5
48	Ceramic DIP	T7100A-BC	2
68	PLCC	T7002-MC, T7003-MC, T7110-MC, T7115-MC	6
70	Ceramic PGA	T7102A-RC	7
84	PLCC	DSP16	8
100	Ceramic PGA	DSP32	9
133	Ceramic PGA	DSP16, DSP32C	10

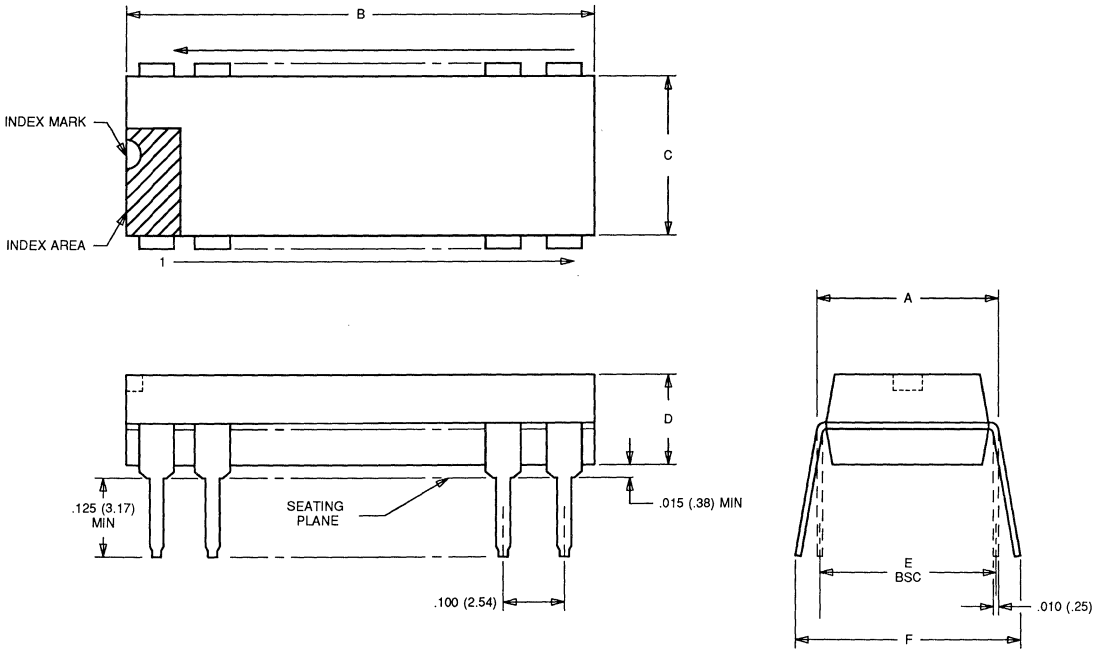
All AT&T telecommunication devices whose device code begins with a T (i.e., T7040-MC) conform to an industry compatible device coding format. These device codes contain information regarding the device's package type and temperature range. This information is located at the end of the device code and is separated from the device number by a dash.

The device's package type is identified by the letter immediately following the dash. The following list gives the package types available and their corresponding letter code:

B = Nonhermetic, ceramic DIP
C = Hermetic, ceramic DIP
E = Small outline
G = Dual-cavity, ceramic DIP
J = Nonhermetic, leadless chip carrier
K = Hermetic, leadless chip carrier
L = Hermetic, ceramic, leaded chip carrier
M = Plastic, leaded chip carrier
N = Nonhermetic, ceramic pin array
P = Plastic DIP
R = Hermetic, ceramic pin array
T = Plastic, leadless chip carrier
U = Nonhermetic, ceramic, leaded chip carrier

The device's operating temperature range is identified by the last letter in the device code. The following list gives the temperature ranges available and their corresponding letter code:

C = 0 to 70 °C (commercial)
E = 0 to 85 °C (extended)
M = Military
L = –40 to +85 °C (outside plant/loop)



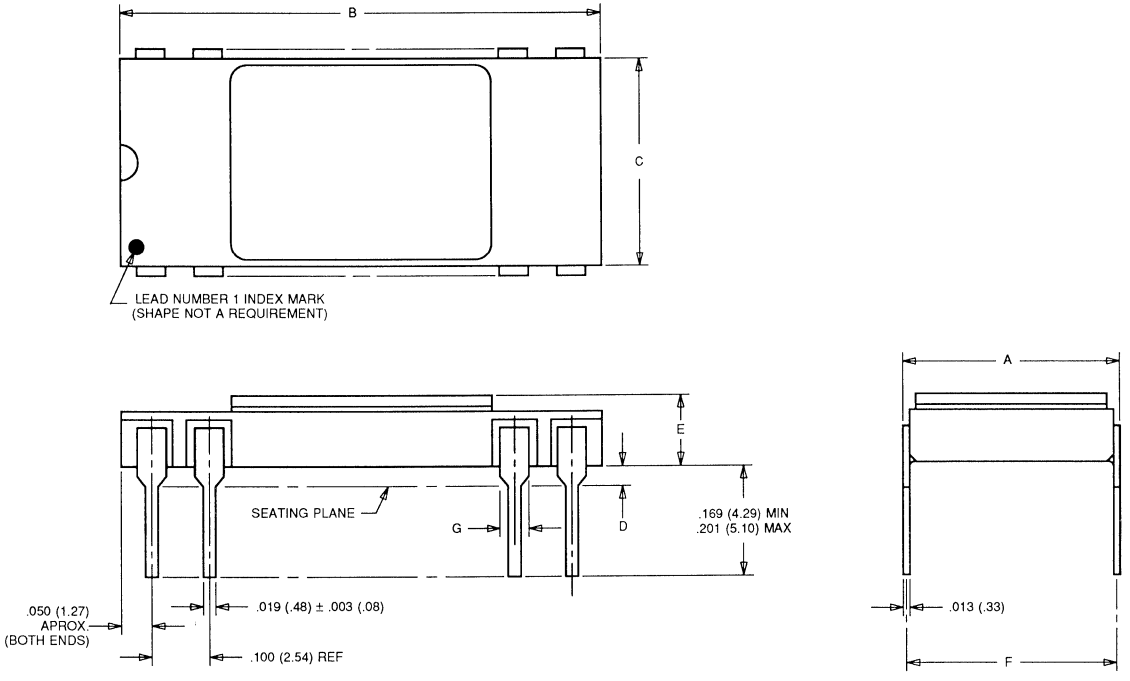
Note: Dimensions are in inches and (millimeters).

Figure 1. Postmolded Plastic DIPs

Table 3. Postmolded Plastic DIP Dimensions

No. Pins	A Max	B Max	C Max	D Max	E BSC	F Max	Notes
16	.320 (8.13)	.795 (20.19)	.265 (6.73)	.140 (3.56)	.300 (7.62)	.400 (10.16)	1, 2, 3
18	.320 (8.13)	.920 (23.37)	.255 (6.48)	.145 (3.68)	.300 (7.62)	.400 (10.16)	1, 2, 3
20	.320 (8.13)	1.040 (26.42)	.255 (6.48)	.140 (3.56)	.300 (7.62)	.400 (10.16)	1, 2, 3
24	.615 (15.62)	1.270 (32.26)	.555 (14.10)	.165 (4.19)	.600 (15.24)	.700 (17.78)	1, 2, 3
28	.615 (15.62)	1.470 (37.34)	.555 (14.10)	.165 (4.19)	.600 (15.24)	.700 (17.78)	1, 2, 3
32	.615 (15.62)	1.580 (40.13)	.555 (14.10)	.165 (4.19)	.600 (15.24)	.700 (17.78)	3, 4
40	.615 (15.62)	2.070 (52.58)	.555 (14.10)	.165 (4.19)	.600 (15.24)	.700 (17.78)	1, 2, 3

Notes:
1 Meets JEDEC standards.
2 Index mark may be semicircular notch or a circular dimple located in index area.
3 Actual dimensions may vary depending on location of assembly, but all meet limits shown in table.
4 Package does not have a JEDEC-approved pin-out.



Note: Dimensions are in inches and (millimeters).

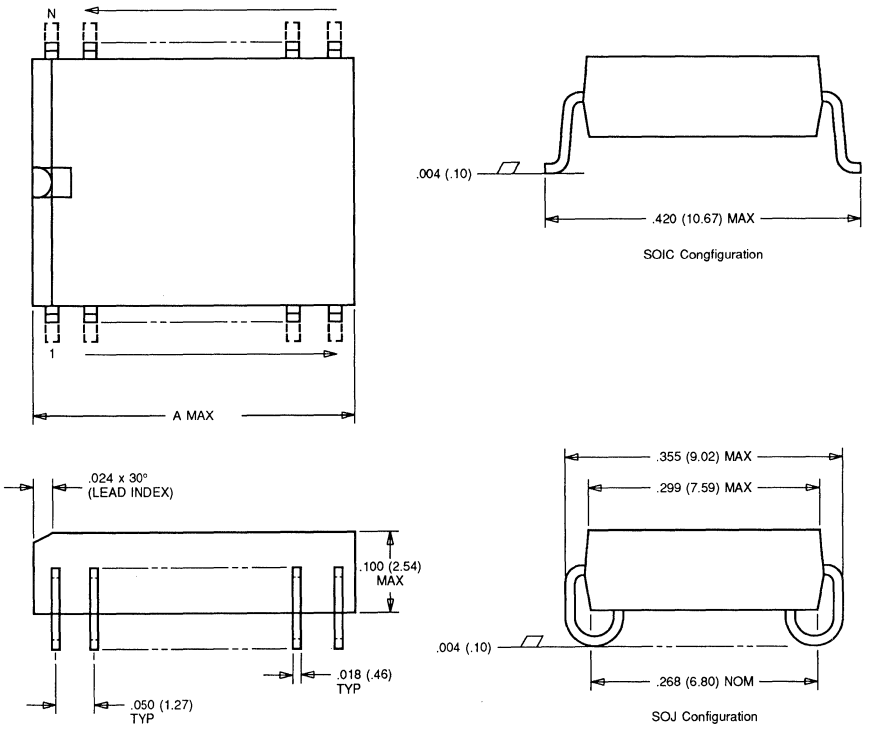
Figure 2. Ceramic DIP — Cavity Up (Facing Away From Printed Wiring Boards)

Table 4. Ceramic DIP Dimensions

No. Pins	A Max	B Max	C Nom	D Approx	E Max	F Nom	G Min
20	.325 (8.25)	1.015 (25.78)	.290 (7.37)	.035 (.89)	.135 (3.43)	.300 (7.62)	.045 (1.14)
24	.620 (15.75)	1.212 (30.78)	.590 (14.99)	.050 (1.27)	.135 (3.43)	.600 (15.24)	.040 (1.02)
40	.620 (15.75)	2.020 (51.31)	.590 (14.99)	.050 (1.27)	.135 (3.43)	.600 (15.24)	.040 (1.02)
48	.620 (15.75)	2.420 (61.47)	.590 (14.99)	.050 (1.27)	.135 (3.43)	.600 (15.24)	.040 (1.02)

Note: Maximum chip size is for chip with pads on two sides.

Caution: For T7520, T7521, and T7522 Codecs, the cavity cover is internally connected to AGND.



Note: Dimensions are in inches and (millimeters).

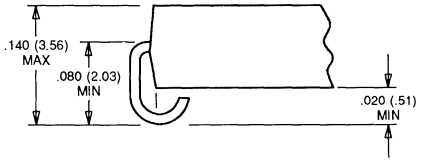
Figure 3a. Plastic SOJ Packages

Table 5. Small-Outline Package Dimensions

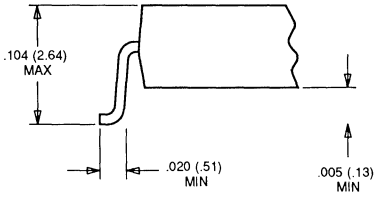
No. Leads	A Max	Lead Configuration*	Max Chip Size L X W
16	.408 (10.36)	$\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$	.200 (5.08) X .190 (4.83)
20	.508 (12.90)	$\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$	.340 (8.64) X .190 (4.83)
28	.708 (17.98)	$\overline{A}$, $\overline{B}$, $\overline{C}$, $\overline{D}$	.350 (8.879) X .190 (4.83)

Notes:

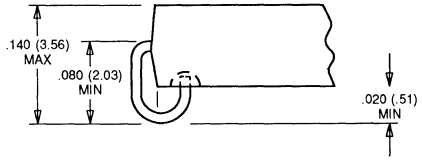
$\overline{C}$, $\overline{D}$ meet JEDEC registered outline TMS 013.
Index mark may be a notch, dimple, or bevel located in zone identified on outline.
Actual dimensions may vary depending on location of assembly but all dimensions meet limits shown in table.
* Package may be provided in any of the indicated lead configurations dependent on location of assembly.



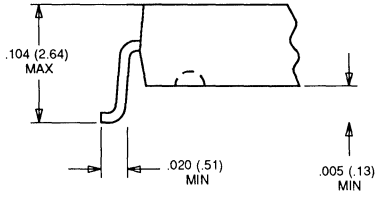
A. DETAIL SOJ



C. DETAIL SOIC



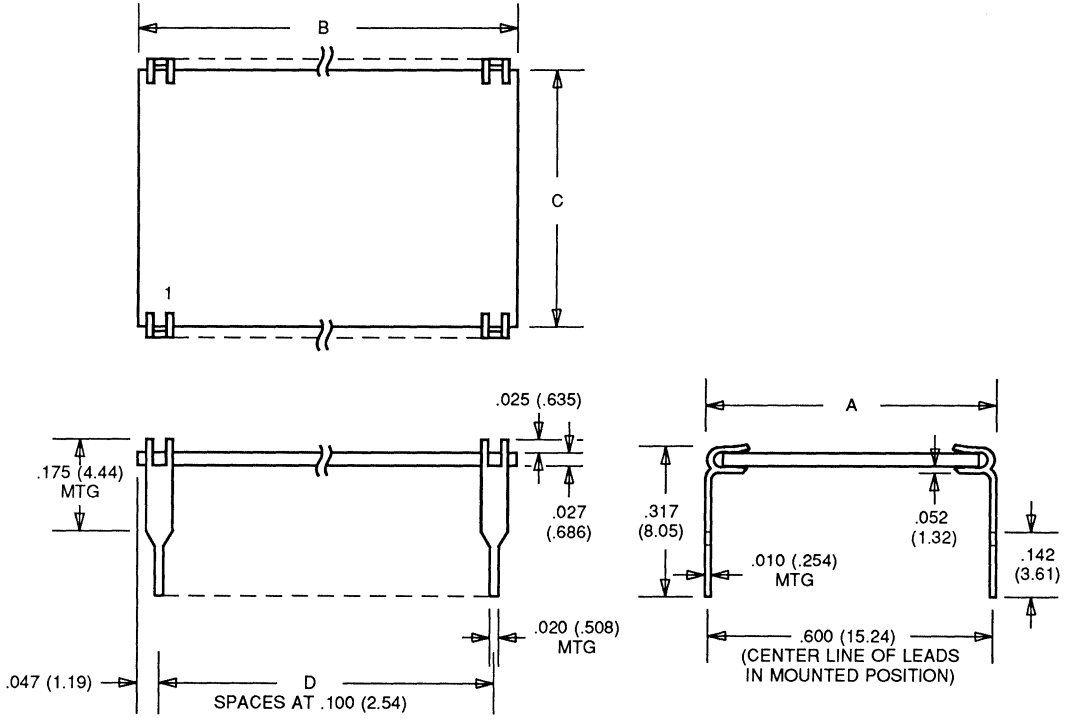
B. DETAIL SOJ



D. DETAIL SOIC

Note: Dimensions are in inches and (millimeters).

Figure 3b. Plastic Small-Outline Lead Configuration Packages

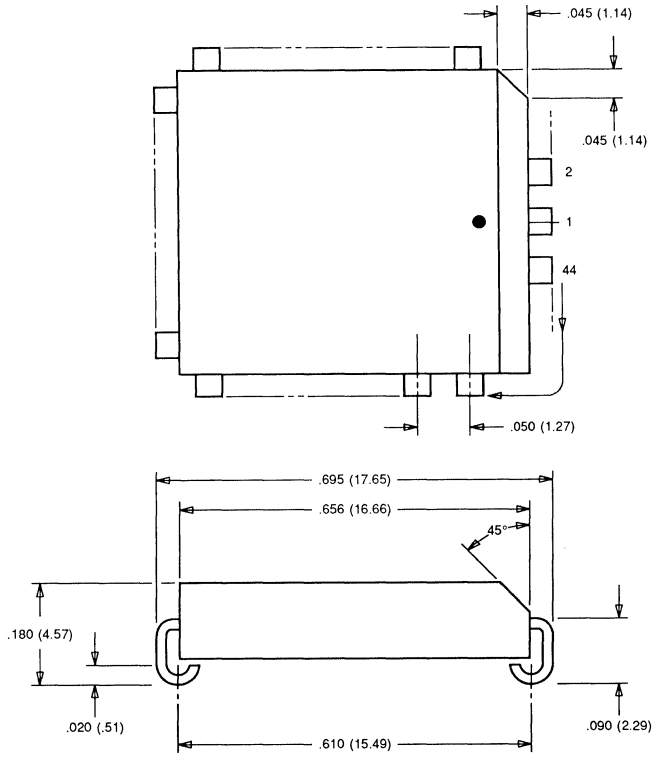


Note: Dimensions are in inches and (millimeters).

Figure 4. Ceramic HIC Packages

Table 6. Ceramic HIC Package Dimensions

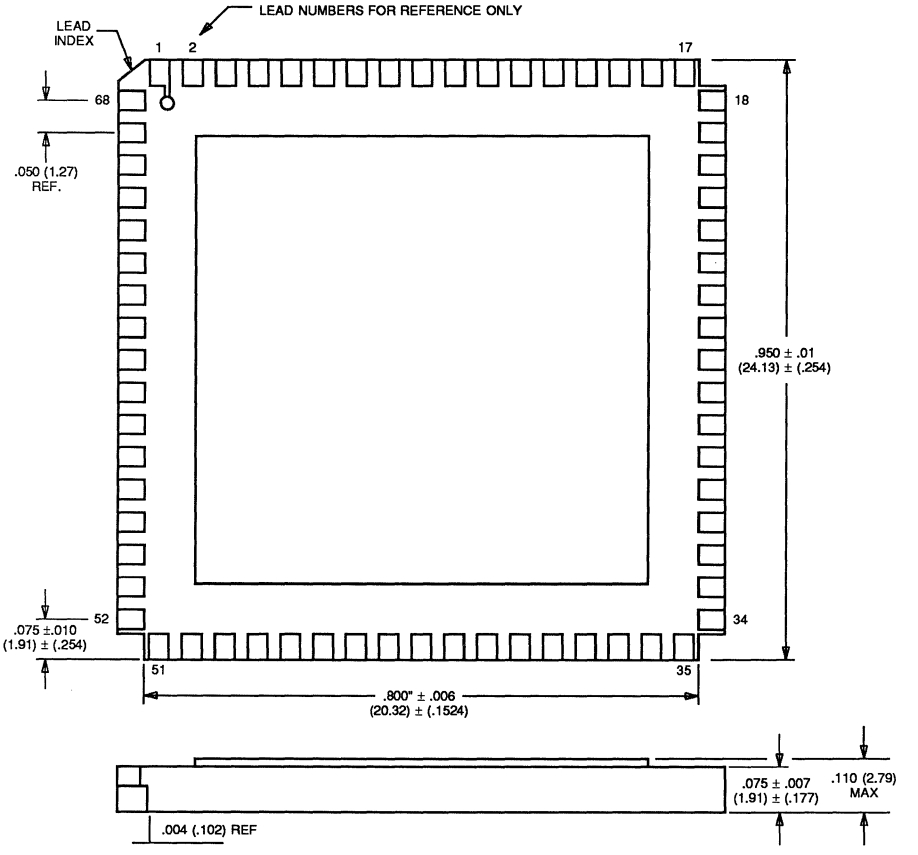
No. Leads	A	B	C
20	.610 (15.49)	.995 (25.27)	.545 (13.84)
40	.610 (15.49)	1.995 (50.67)	.545 (13.84)



Notes:

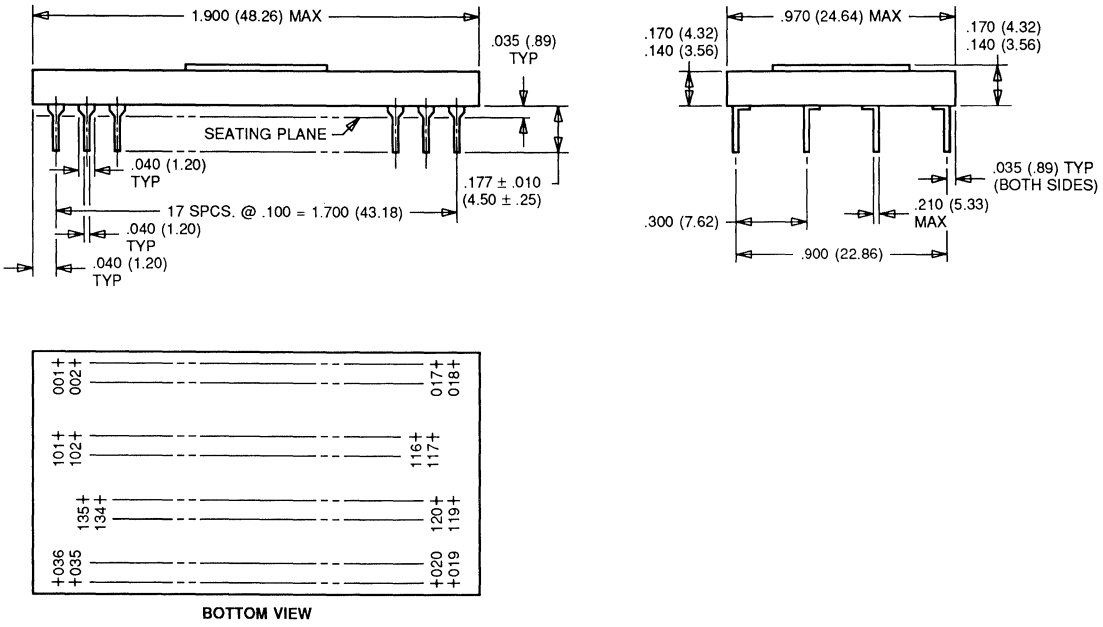
1 All meet JEDEC standards.
2 Pin 1 index mark may be a dimple or numeric located in zone indicated.
3 Dimensions are in inches and (millimeters).

Figure 5. 44-Pin PLCC Package



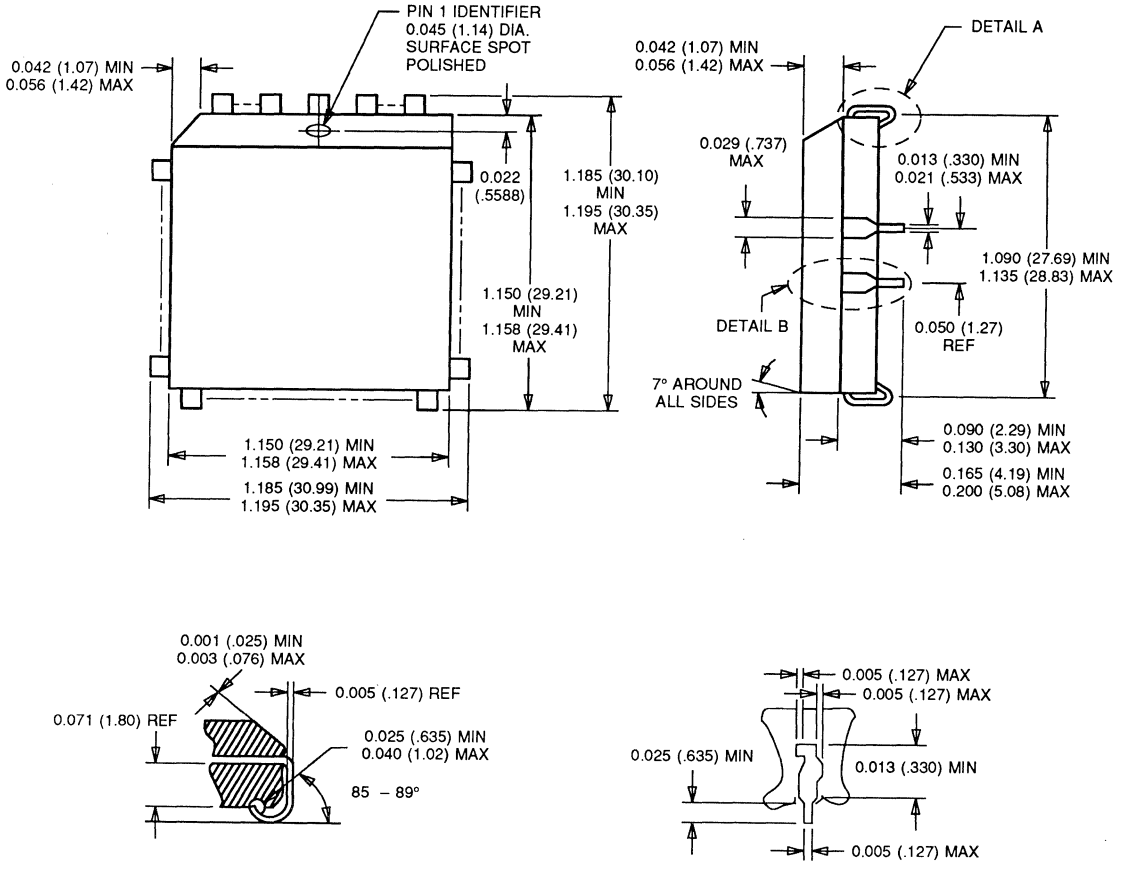
Note: Dimensions are in inches and (millimeters).

Figure 6. 68-Pin PLCC Package



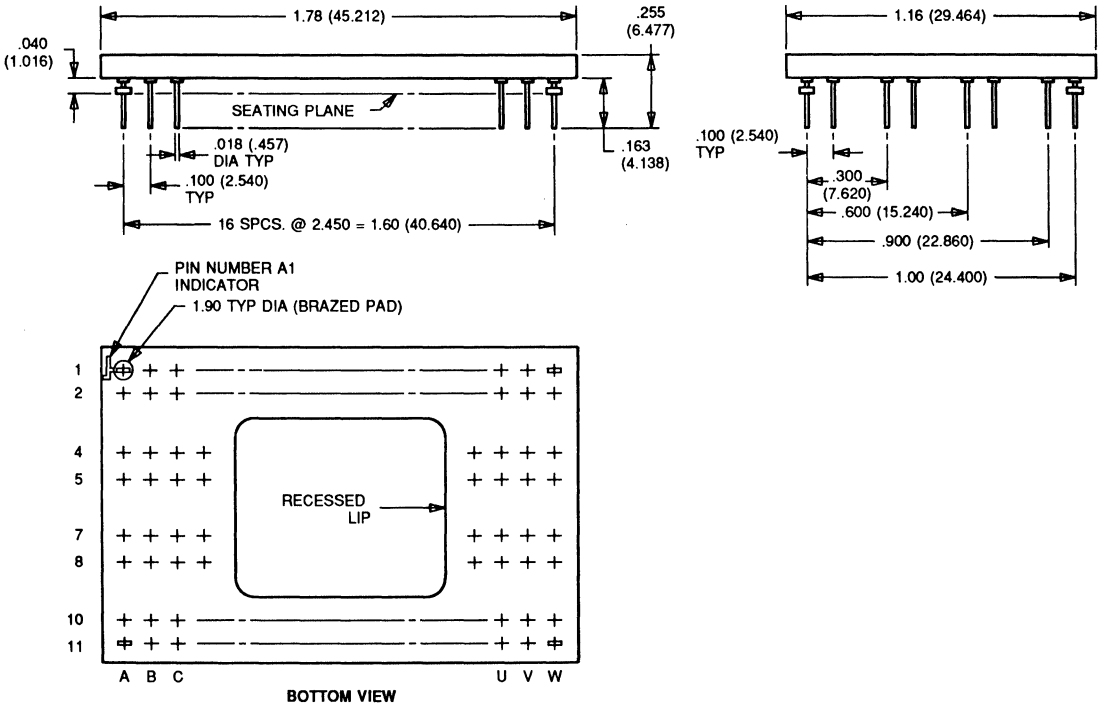
Note: Dimensions are in inches and (millimeters).

Figure 7. 70-Pin Ceramic PGA Package — Cavity Up (Facing Away From Printed Wiring Board)



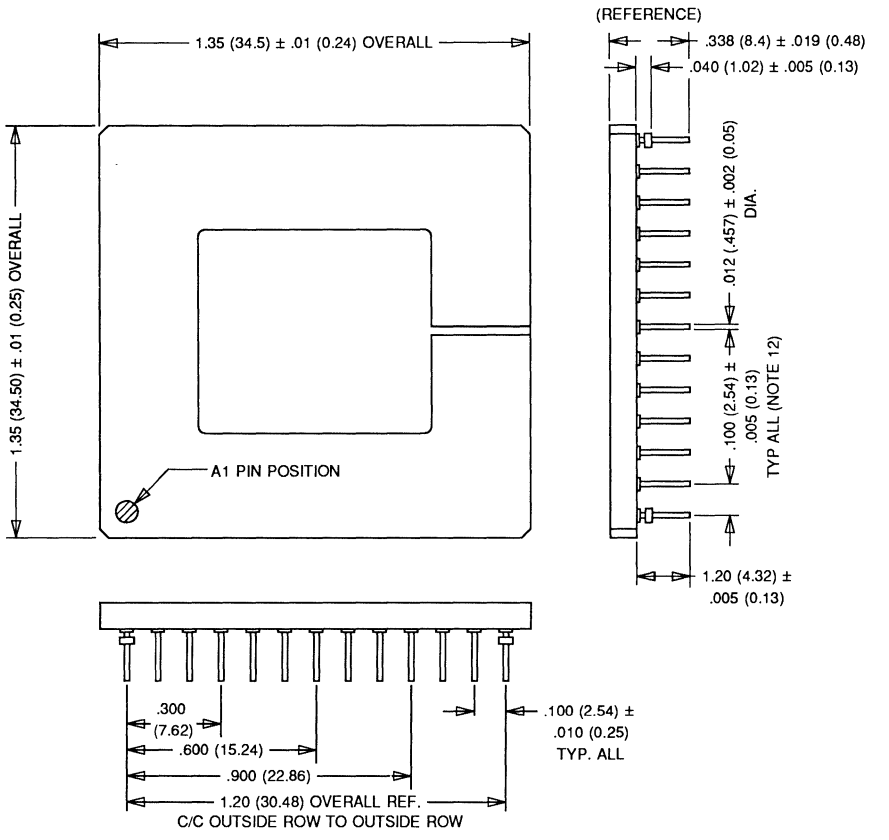
Note: Dimensions are in inches and (millimeters).

Figure 8. 84-Pin PLCC Package



Note: Dimensions are in inches and (millimeters).

Figure 9. 100-Pin Ceramic PGA Package — Cavity Down (Facing Toward PWB)



Note: Dimensions are in inches and (millimeters).

Figure 10. 133-Pin Ceramic PGA Package

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