CYPRESS SEMICONDUCTOR

BiCMOS/CMOS DATA BOOK

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CMOS BiCMOS DATA BOOK

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SEMICONDUCTOR™

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CYPRESS SEMICONDUCTOR

How To Use This Book

This book has been organized by product type, beginning with Product Information. The products are next, starting with SRAMs, then PROMs, EPLDs, FIFOs, Logic, RISC, Modules, and ECL. A section containing military information is next, followed by the BridgeMOS™ product family, and then the Design and Programming Tools section. Quality and Reliability aspects are next, then Thermal Data and Packages. Within each section, data sheets are arranged in order of part number. JEDEC-standard module data sheets are reprinted in full in the appropriate SRAM or Logic sections, and single-page references have been placed in the Modules section. All other module data sheets can be found printed in full in the Modules section, with single-page references in the SRAM and Logic sections.

A Numeric Device Index, included after the Table of Contents, identifies products by numeric order rather than by device type. To further help you in identifying parts, a product line Cross Reference Guide is in the Product Information section. It can be used to find the Cypress part number that is comparable to another manufacturer's part number.

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Table of Contents

Page Number

General Product Information

Static RAMs (Random Access Memory)

Static RAMs (Random Access Memory) (continued)

Static RAMs (Random Access Memory) (continued)

PROMs (Programmable Read Only Memory)

Table of Contents

EPLDs (Erasable Programmable Logic Devices)

FIFOs

PAL is a registered trademark of Advanced Micro Devices, Inc.

Table of Contents

Modules (continued)

ECL

Military Information

BridgeMOS

Design and Programming Tools

Table of Contents

Device Number	Description
7C142	2048 x 8 Dual-Port Static RAM 2-66
7C146	2048 x 8 Dual-Port Static RAM 2-66
7C147	4096 x 1 Static RAM 2-78
7C148	1024 x 4 Static RAM 2-85
7C149	1024 x 4 Static RAM 2-85
7C150	1024 x 4 Static R/W RAM 2-92
7C157	16,384 x 4 Static R/W RAM 2-100
7C161	16,384 x 4 Static R/W RAM Separate I/O 2-116
7C161A	16,384 x 4 Static R/W RAM Separate I/O 2-123
7C162	16,384 x 4 Static R/W RAM Separate I/O 2-116
7C162A	16,384 x 4 Static R/W RAM Separate I/O 2-123
7C164	16,384 x 4 Static R/W RAM 2-137
7C164A	16,384 x 4 Static R/W RAM 2-144
7C166	16,384 x 4 Static R/W RAM with Output Enable 2-137
7C166A	16,384 x 4 Static R/W RAM with Output Enable 2-144
7C167	16,384 x 1 Static R/W RAM 2-153
7C167A	16,384 x 1 Static RAM 2-160
7C168	4096 x 4 Static RAM 2-167
7C168A	4096 x 4 R/W RAM 2-174
7C169	4096 x 4 Static RAM 2-167
7C169A	4096 x 4 R/W RAM 2-174
7C170	4096 x 4 Static R/W RAM with Output Enable 2-183
7C170A	4096 x 4 Static R/W RAM 2-188
7C171	4096 x 4 Static R/W RAM Separate I/O 2-194
7C171A	4096 x 4 Static R/W RAM Separate I/O 2-200
7C172	4096 x 4 Static R/W RAM Separate I/O 2-194
7C172A	4096 x 4 Static R/W RAM Separate I/O 2-200
7C182	8,192 x 9 Static R/W RAM 2-208
7C183	2 x 4096 x 16 Cache RAM 2-213
7C184	2 x 4096 x 16 Cache RAM 2-213
7C185	8,192 x 8 Static R/W RAM 2-226
7C185A	8,192 x 8 Static R/W RAM 2-233
7C186	8,192 x 8 Static R/W RAM 2-226
7C186A	8,192 x 8 Static R/W RAM 2-233
7C187	65,536 x 1 Static R/W RAM 2-241
7C187A	65,536 x 1 Static R/W RAM 2-248
7C189	16 x 4 Static R/W RAM 2-257
7C190	16 x 4 Static R/W RAM 2-257
7C191	65,536 x 4 Static R/W RAM Separate I/O 2-264
7C192	65,536 x 4 Static R/W RAM Separate I/O 2-264
7C194	65,536 x 4 Static R/W RAM 2-271
7C196	65,536 x 4 Static R/W RAM with Output Enable 2-271
7C197	262,144 x 1 Static R/W RAM 2-279
7C198	32,768 x 8 Static R/W RAM 2-286
7C199	32,768 x 8 Static R/W RAM 2-286
7C225	512 x 8 Registered PROM 3-4
7C235	1024 x 8 Registered PROM 3-15
7C245	2048 x 8 Reprogrammable Registered PROM 3-26
7C245A	2048 x 8 Reprogrammable Registered PROM 3-38
7C251	16,384 x 8 Power Switched and Reprogrammable PROM 3-50
7C254	16,384 x 8 Reprogrammable PROM 3-50
7C261	8192 x 8 Power Switched and Reprogrammable PROM 3-60

Device Number **Description**

Section Contents

General Product Information

Page Number

Cypress Semiconductor Background

Cypress Semiconductor was founded in April 1983 with the stated goal of serving the high-performance semiconductor market. This market is served by producing the highest-performance integrated circuits using state-of-the-art processes and circuit design. Cypress is a complete semiconductor manufacturer, performing its own process development, circuit design, wafer fabrication, assembly, and text. The company went public in May 1986 and was listed on the New York Stock Exchange in October 1988.

The initial semiconductor process, a CMOS process employing 1.2-micron geometries, was introduced in March 1984. This process is used in the manufacturing of Static RAMs and Logic circuits. In the third quarter of 1984, a 1.2-micron CMOS EPROM process was introduced for the production of programmable products. At the time of introduction, these processes were the most advanced production processes in the industry. Following the 1.2-micron processes, a 0.8-micron CMOS SRAM process was implemented in the first quarter of 1986, and a 0.8-micron EPROM process in the third quarter of 1987.

In keeping with the strategy of serving the high-performance markets with state-of-the-art integrated circuits, Cypress introduced two new processes in 1989. These were a bipolar submicron process, targeted for ECL circuits, and a BiCMOS process to be used for most types of TTL and ECL circuits.

The circuit design technology used by Cypress is also state of the art. This design technology, along with advanced process technology, allows Cypress to introduce the fastest, highest-performance circuits in the industry. Cypress's products fall into seven families: high-speed Static RAMs, PROMS, Erasable Programmable Logic Devices, Logic, RISC microprocessors, ECL SRAMs and PLDs, and module products. Members of the CMOS Static RAM family include devices in densities of 64 bits to 256K bits, and performance from 7 ns to 35 ns. The various organizations, 16 x 4, 256 x 4 through 256K x 1, 32K x 8, and 64K x 4 provide optimal solutions for applications such as large mainframes, high-speed controllers, communications, and graphics display. Cypress's BiCMOS family of 64K SRAMs in 16K x 4 and 32K x 8 configurations offers speeds as fast as 10 ns.

Cypress's CMOS programmable products consist of high-speed PROMs and Erasable Programmable Logic Devices (EPLDs), both employing an EPROM programming element. Like the high-speed Static RAM family, these products are the natural choice to replace older devices because they provide superior performance at one half of the power consumption. PROM densities range from 4 to 512 kilobits in byte-wide organization. EPLD products range from 20 pins to 68 pins with performance as fast as 125 MHz. To support new programmable products, Cypress introduced the QuickPro™ programming system (CY3000) for PLDs and PROMs, and the PLD ToolKit for PLDs. QuickPro is a development tool that includes a single, IBM PC® compatible add-on board and a software utility program. The PLD ToolKit is a software design tool that assembles and simulates logic functions, generates JEDEC files, and reverse assembles to create source files. Both QuickPro and the PLD ToolKit software are updated via floppy disk, thereby allowing quick support of all Cypress programmable products.

Logic products include circuits such as 4-bit and 16-bit slices, 16 x 16 multipliers and 16-bit microprogrammable ALUs, a family of 1K x 8 and 2K x 8 dual-port SRAMS, as well as a family of FIFOs that range from 64 x 4 to 4K x 9. FIFOs provide the interface between digital information paths of widely varying speeds. This allows the information source to operate at its own intrinsic speed, while the results may be processed or distributed at a speed commensurate with need.

Until 1988, all Cypress products were TTL I/O-compatible. In 1989, Cypress introduced ECL products having access times (propagation delays) of less than 3.5 ns in either of the popular I/O configurations, 100K or 10K/10KH. ECL RAMs include 256 x 4, 1K x 4, and 16K x 4 RAM families with balanced read/write cycles. The ECL PLDs are combinatorial 16P8 and 16P4 devices that can be programmed on QuickPro and other commercially available programming tools. Both the RAMs and PLDs are offered in low-power versions, reducing operating power by 30 to 40 percent while achieving 5-ns access times (RAM) and 6-ns t_{PD} (PLD).

The module family consists of both standard and custom modules incorporating circuits from the other six product families. This capability provides a fast, low-risk solution for designs requiring the ultimate in system performance and density. Several module configurations are available depending on height and board real estate constraints. Modules include Single-In-Line, Dual-In-Line, Dual Single-In-line, Vertical Dual-In-Line, Quad-In-Line, and (Staggered) Zig-Zag-In-Line packages.

Cypress's CY7C600 family of RISC microprocessor products provides state-of-the-art high-performance computing for applications ranging from UNIX-based business computers and workstations to embedded controls. Based on the SPARC™ RISC architecture, the family provides a complete solution with Integer Unit (IU), Floating-Point Unit (FPU), Cache Control and Memory Management Unit (CMU), and Cache RAMs (CRAMs). The family is functionally partitioned to provide a range of features, performance, and price to suit each type of application.

Situated in California's Silicon Valley (San Jose) and Round Rock (Austin), Texas, Cypress houses R&D, design, wafer fabrication, assembly, and administration. The facilities are designed to the most demanding technical and environmental specifications in the industry. At the Texas facility, the entire wafer fabrication area is specified to be a Class 1 environment. This means that the ambient air has less than 1 particle of greater than 0.2 microns in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a ±0.2 degree Fahrenheit tolerance; filtered air is completely exchanged more than 10 times each minute throughout the fab; and critical equipment is situated on isolated slabs to minimize vibration.

Attention to assembly is equally as critical. Cypress assembles and tests 55 packages in the United States at its San Jose, California plant. Assembly is completed in a clean room until the silicon die is sealed in a package. Lead frames are handled in carriers or cassettes through the entire operation. Automated robots remove and replace parts into cassettes. Using sophisticated automated equipment, parts are assembled and tested in less than five days. The Cypress assembly line is the most flexible, automated line in the United States.

The Cypress motto has always been "only the best—the best facilities, the best equipment, the best employees . . . all striving to make the best CMOS, BiCMOS, and bipolar products.

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Cypress Process Technology

In the last decade, there has been a tremendous need for high-performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor has overcome the classically held perceptions that CMOS is a moderate-performance technology.

Cypress initially introduced a 1.2-micron "N" well technology with double-layer poly and a single-layer metal. The process employs lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latch-up characteristics associated with the older CMOS technologies.

Cypress pushed process development to new limits in the areas of PROMs (Programmable Read Only Memory) and EPLDs (Erasable Programmable Logic Devices). Both PROMs and EPLDs have existed since the early 1970s in a bipolar process that employed various fuse technologies and was the only viable high-speed nonvolatile process available. Cypress PROMs and EPLDs use EPROM technology, which has also been in use in MOS (Metal Oxide Silicon) also since the early 1970s. EPROM technology has traditionally emphasized density advantages while forsaking performance. Through improved technology, Cypress has produced the first high-performance CMOS PROMs and EPLDs, replacing their bipolar counterparts.

To maintain our leadership position in CMOS technology, Cypress has introduced a sub-micron technology into production. This process reduces the drawn channel length from the current 1.2 microns to 0.8 microns. This sub-micron breakthrough makes Cypress's CMOS one of the most advanced production processes in the world.

To further enhance the technology from the reliability direction, improvements have been incorporated in the process and design, minimizing electrostatic discharge and input signal clipping problems.

Finally, although not a requirement in the high-performance arena, CMOS technology substantially reduces the power consumption for any device. This improves reliability by allowing the device to operate at a lower die temperature. Now higher levels of integration are possible without trading performance for power. For instance, devices may now be delivered in plastic packages without any impact on reliability.

While addressing the performance issues of CMOS technology, Cypress has not ignored the quality and reliability aspects of technology development. Rather, the traditional failure mechanisms of electrostatic discharge (ESD) and latch-up have been addressed and solved through process and design technology innovation.

ESD-induced failure has been a generic problem for many high-performance MOS and bipolar products. Although in its earliest years, MOS technology experienced oxide reliability failures, this problem has largely been eliminated through improved oxide growth techniques and a better understanding of the ESD problem. The effort to adequately protect against ESD failures is perturbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress has developed ESD protection circuitry specific to 1.2- and 0.8-micron CMOS process technology. Cypress products are designed to withstand voltage and energy levels in excess of 2001 volts and 0.4 milli-joules.

Latch-up, a traditional problem with CMOS technologies, has been eliminated through the use of substrate bias generation techniques, the elimination of the "P" MOS pull-ups in the output drivers, the use of guardring structures and care in the physical layout of the products.

Cypress has also developed additional process innovations and enhancements: the use of multilayer metal interconnections, advanced metal deposition techniques, silicides, exclusive use of plasma for etching and ashing process steps, and 100 percent stepper technology with the world's most advanced equipment.

A wholly owned subsidiary of Cypress, Aspen Semiconductor, has developed both advanced bipolar and BiCMOS technologies augmenting the capabilities of the Cypress CMOS processes. Both the new Bipolar and BiCMOS technologies are based on the Cypress 0.8-micron CMOS process for enhanced manufacturability. Like CMOS, these processes are scalable to take advantage of finer line lithography. Where speed is critical, Cypress BiCMOS allows increased transistor performance. It also allows reduced power in the non-speed critical sections of the design to optimize the speed/power balance. The Bipolar and BiCMOS processes make possible memories and logic operating up to 400 MHz. The drive to maintain process technology leadership has not stopped with the 0.8-micron devices. Cypress is developing fine-line geometries beyond this to insure technology leadership in the next decade.

Cypress technologies have been carefully designed, creating products that are "only the best" in high-speed, excellent reliability, and low power.

Static RAMs

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	Packages	Availability
64	16x4—Inverting	16	CY7C189	t_{AA} = 15,25	55@25	D,L,P	Now
64	16x4—Non-Inverting	16	CY7C190	t_{AA} = 15,25	55@25	D,L,P	Now
64	16x4—Inverting	16	CY74S189	t_{AA} = 35	90@35	D,P	Now
64	16x4—Inverting	16	CY27S03A	t_{AA} = 25,35	90@25	D,L,P	Now
64	16x4—Non-Inverting	16	CY27S07A	t_{AA} = 25,35	90@25	D,L,P	Now
64	16x4—Inverting Low Power	16	CY27LS03M	t_{AA} = 65	38@65	D,L	Now
1K	256x4	22	CY7C122	t_{AA} = 15,25,35	60@25	D,L,P,S	Now
1K	256x4	24S	CY7C123	t_{AA} = 7,9,12	120@7	D,L,P,V	Now
1K	256x4	22	CY9122/91L22	t_{AA} = 25,35,45	120@25	D,P	Now
1K	256x4	22	CY93422A/93L422	t_{AA} = 35,45,60	80@45	D,L,P	Now
4K	4Kx1—CS Power Down	18	CY7C147	t_{AA} = 25,35,45	80/10@35	D,L,P,S	Now
4K	4Kx1—CS Power Down	18	CY2147/21L47	t_{AA} = 35,45,55	125/25@35	D,P	Now
4K	1Kx4—CS Power Down	18	CY7C148	t_{AA} = 25,35,45	80/10@35	D,L,P,S	Now
4K	1Kx4—CS Power Down	18	CY2148/21L48	t_{AA} = 35,45,55	120/20@35	D,P,S	Now
4K	1Kx4	18	CY7C149	t_{AA} = 25,35,45	80@35	D,L,P,S	Now
4K	1Kx4	18	CY2149/21L49	t_{AA} = 35,45,55	120@35	D,P	Now
4K	1Kx4—Separate I/O, Reset	24S	CY7C150	t_{AA} = 10,12,15,25,35	90@12	D,L,P,S	Now
8K	1Kx8—Dual Port	48	CY7C130	t_{AA} = 25,35,45,55	170@25	D,L,P	Now
8K	1Kx8—Dual Port Slave	48	CY7C140	t_{AA} = 25,35,45,55	170@25	D,L,P	Now
8K	1Kx8—Dual Port	52	CY7C131	t_{AA} = 25,35,45,55	170@25	L,J	Now
8K	1Kx8—Dual Port Slave	52	CY7C141	t_{AA} = 25,35,45,55	170@25	L,J	Now
16K	2Kx8—CS Power Down	24S	CY7C128	t_{AA} = 35,45,55	90/20@55	D,L,P,V	Now
16K	2Kx8—CS Power Down	24	CY7C128A	t_{AA} = 20,25,35,45,55	90/20@55	D,L,P,V	Now
16K	2Kx8—CS Power Down	24	CY6116	t_{AA} = 35,45,55	120/20@55	D,L	Now
16K	2Kx8—CS Power Down	24	CY6116A	t_{AA} = 20,25,35,45,55	80/20@55	D,L	Now
16K	2Kx8—CS Power Down	32S	CY6117	t_{AA} = 35,45,55	130/20@55	L	Now
16K	16Kx1—CS Power Down	20	CY7C167	t_{AA} = 25,35,45	50/15@25	D,L,P,V	Now
16K	16Kx1—CS Power Down	20	CY7C167A	t_{AA} = 15,20,25,35,40	50/15@45	D,L,P,V	Now
16K	4Kx4—CS Power Down	20	CY7C168	t_{AA} = 25,35,45	90/15@25	D,L,P,V	Now
16K	4Kx4—CS Power Down	20	CY7C168A	t_{AA} = 15,20,25,35,45	70/15@45	D,L,P,V	Now
16K	4Kx4	20	CY7C169	t_{AA} = 25,35,40	90@25	D,L,P,V	Now
16K	4Kx4	20	CY7C169A	t_{AA} = 15,20,25,35,40	70@45	D,L,P,V	Now
16K	4Kx4—Output Enable	22S	CY7C170	t_{AA} = 25,35,45	90@45	D,L,P,V	Now
16K	4Kx4—Output Enable	22S	CY7C170A	t_{AA} = 15,20,25,35,45	90@45	D,L,P,V	Now
16K	4Kx4—Separate I/O	24S	CY7C171	t_{AA} = 20,25,35,45	90/15@25	D,L,P,V	Now
16K	4Kx4—Separate I/O	24S	CY7C171A	t_{AA} = 15,20,25,35,45	90@45	D,L,P,V	Now
16K	4Kx4—Separate I/O	24S	CY7C172	t_{AA} = 25,35,45	90/15@25	D,L,P,S	Now
16K	4Kx4—Separate I/O	24S	CY7C172A	t_{AA} = 15,20,25,35,45	90@45	D,L,P,V	Now
16K	2Kx8—Dual Port	48	CY7C132	t_{AA} = 25,35,45,55	170@25	D,L,P	Now
16K	2Kx8—Dual Port Slave	48	CY7C142	t_{AA} = 25,35,45,55	170@25	D,L,P	Now
16K	2Kx8—Dual Port	52	CY7C136	t_{AA} = 25,35,45,55	170@25	L,J	Now
16K	2Kx8—Dual Port (Slave)	52	CY7C146	t_{AA} = 25,35,45,55	170@25	L,J	Now
64K	8Kx8—CS Power Down	28S	CY7B185	t_{AA} = 12,15	135/40@15	D,L,P,V	Now
64K	8Kx8—CS Power Down	28	CY7B186	t_{AA} = 12,15	135/40@15	D,L,P,V	Now
64K	8Kx8—CS Power Down	28S	CY7C185A	t_{AA} = 20,25,35,45	120/20@15	D,L,P,V	Now
64K	8Kx8—CS Power Down	28	CY7C186A	t_{AA} = 20,25,35,45	120/20@15	D,P	Now
64K	16Kx4—CS Power Down	22S	CY7B164	t_{AA} = 10,12	120/40@12	D,P,V	Now
64K	16Kx4—CS Power Down	22S	CY7C164A	t_{AA} = 15,20,25,35,45	115/40@15	D,L,P,V	Now
64K	16Kx4—Linear Decode with SCSs	28S	CY7B160	t_{AA} = 12,15	115/40@15	D,P,V	Now
64K	16Kx4—Output Enable	24S	CY7B166	t_{AA} = 10,12	120/40@12	D,P,V	Now
64K	16Kx4—Output Enable	24S	CY7C166A	t_{AA} = 15,20,25,35,45	115/40@15	D,L,P,V	Now
64K	16Kx4—Separate I/O, Transparent Write	28S	CY7B161	t_{AA} = 10,12	120/40@12	D,P,V	Now
64K	16Kx4—Separate I/O	28S	CY7B162	t_{AA} = 10,12	120/40@12	D,P,V	Now
64K	16Kx4—Separate I/O, Transparent Write	28S	CY7C161A	t_{AA} = 15,20,25,35,45	115/40@15	D,L,P,V	Now
64K	16Kx4—Separate I/O	28S	CY7C162A	t_{AA} = 15,20,25,35,45	115/40@15	D,L,P,V	Now
64K	64Kx1—CS Power Down	22S	CY7C187A	t_{AA} = 15,20,25,35,45	90/40@15	D,L,P,V	Now
72K	8Kx9	28S	CY7C182	t_{AA} = 25,35,45,55	170@25	D,P,V	1Q90
128K	8Kx16—Addresses Latched except A12	52	CY7C183	t_{AA} = 25,35,45	220@25	J	Now
128K	8Kx16—Addresses Latched	52	CY7C184	t_{AA} = 25,35,45	220@25	J	Now
256K	16Kx16—SPARC Cache RAM	52	CY7C157	t_{AA} = 20,24,33	250	J,L	Now

Static RAMs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	Packages	Availability
256K	32Kx8—CS Power Down	28	CY7C198	t_{AA} = 25, 35, 45, 55	170/35@25	D, L, P	Now
256K	32Kx8—CS Power Down	28S	CY7C199	t_{AA} = 25, 35, 45, 55	150/35@25	D, L, P, V	Now
256K	64Kx4—CS Power Down	24S	CY7C194	t_{AA} = 25, 35, 45	120/35@25	D, L, P, V	Now
256K	64Kx4—CS Power Down with OE	28S	CY7C196	t_{AA} = 25, 35, 45	120/35@25	D, L, P, V	Now
256K	64Kx4—Separate I/O, Transparent Write	28S	CY7C191	t_{AA} = 25, 35, 45	120/35@25	D, L, P, V	Now
256K	64Kx4—Separate I/O	28S	CY7C192	t_{AA} = 25, 35, 45	120/35@25	D, L, P, V	Now
256K	256Kx1—CS Power Down	24S	CY7C197	t_{AA} = 25, 35, 45	100/35@25	D, L, P, V	Now

ECL SRAMs

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	Packages	Availability
1K	256x4—10K/10KH	24.4	CY10E422	t_{AA} = 3, 5	220	D, L, K, Y	Now
1K	256x4—10K/10KH	24.4	CY10E422L	t_{AA} = 5, 7	150	D, L, J, K	Now
1K	256x4—100K	24.4	CY100E422	t_{AA} = 3, 5	220	D, L, K, Y	Now
1K	256x4—100K	24.4	CY100E422L	t_{AA} = 5, 7	150	D, L, J, K	Now
4K	1024x4—10K/10KH	24.4	CY10E474	t_{AA} = 3, 5	275	D, L, K, Y	Now
4K	1024x4—10K/10KH	24.4	CY10E474L	t_{AA} = 5, 7	190	D, L, J, K	Now
4K	1024x4—100K	24.4	CY100E474	t_{AA} = 3, 5	275	D, L, K, Y	Now
4K	1024x4—100K	24.4	CY100E474L	t_{AA} = 5, 7	190	D, L, J, K	Now
64K	16Kx4—10K/10KH	28.4	CY10E494	t_{AA} = 7, 10, 12	190	D, P, L, K, V	Now
64K	16Kx4—10K/10KH	28.4	CY10E494L	t_{AA} = 10, 12	135	D, P, L, K, V	Now
64K	16Kx4—100K	28.4	CY100E494	t_{AA} = 7, 10, 12	190	D, P, L, K, V	Now
64K	16Kx4—100K	28.4	CY100E494L	t_{AA} = 10, 12	135	D, P, L, K, V	Now

Modules

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	Packages	Availability
256K	64Kx4—SRAM (JEDEC)	24	CYM1220	t_{AA} = 10, 12, 15	325@10	HD	1Q90
256K	32Kx8—SRAM (JEDEC)	28	CYM1400	t_{AA} = 10, 12, 15	375@10	HD	1Q90
256K	16Kx16—SRAM (JEDEC)	40	CYM1610	t_{AA} = 12, 15 t_{AA} = 20, 25, 35, 45, 50	550@12 330@20	HD HD	1Q90 Now
256K	16Kx16—SRAM	36	CYM1611	t_{AA} = 12, 15, 20 t_{AA} = 25, 30, 35, 45	550@12 330@25	HV HV	1Q90 Now
512K	16Kx32—SRAM (JEDEC)	64	CYM1821	t_{AA} = 12, 15 t_{AA} = 20, 25, 35, 45	960@12 720@25	PZ PZ	1Q90 Now
512K	16Kx32—SRAM	88	CYM1822	t_{AA} = 12, 15 t_{AA} = 20, 25, 30, 45, 55	960@12 720@25	HV HV	1Q90 Now
768K	32Kx24—SRAM	56	CYM1720	t_{AA} = 25, 30, 35	330@25	PZ	Now
1M	256Kx4—SRAM (JEDEC)	28	CYM1240	t_{AA} = 25, 35, 45	480@25	HD	Now
1M	128Kx8—SRAM (JEDEC)	32	CYM1420	t_{AA} = 30, 35, 45, 55	210@30	HD	Now
1M	128Kx8—SRAM (JEDEC)	32	CYM1421	t_{AA} = 70, 85	120@70	HD	Now
1M	128Kx8—SRAM	30	CYM1422	t_{AA} = 30, 35, 45, 55	200@30	PS	Now
1M	128Kx8—SRAM (JEDEC)	32	CYM1423	t_{AA} = 45, 55, 70	210@45	PD	Now
1M	64Kx16—SRAM (JEDEC)	40	CYM1620	t_{AA} = 30, 35, 45, 55	340@30	HD	Now
1M	64Kx16—SRAM	40	CYM1621	t_{AA} = 20, 25, 30, 35, 45	1250@20	HD	Now
1M	64Kx16—SRAM	40	CYM1622	t_{AA} = 25, 35, 45	400@25	HV	Now
1M	64Kx16—SRAM (JEDEC)	40	CYM1623	t_{AA} = 70, 85, 100	240@70	HD	Now
1M	64Kx16—SRAM (JEDEC)	40	CYM1624	t_{AA} = 25, 35, 45	500@25	PV	Now
1M	16Kx68—SRAM	104	CYM1910	t_{AA} = 25, 35, 45	1900@25	PV	Now
1M	16Kx68—SRAM	104	CYM1911	t_{AA} = 25, 35, 45	1900@25	PV	Now
2M	256Kx8—SRAM (JEDEC)	60	CYM1441	t_{AA} = 25, 35, 45	960@25	PZ	Now
2M	64Kx32—SRAM	60	CYM1830	t_{AA} = 20, 30, 35, 45, 55	880@25	HD	Now
2M	64Kx32—SRAM (JEDEC)	64	CYM1831	t_{AA} = 25, 30, 35, 45	720@25	PZ, PM	Now
2.25M	256Kx9—SRAM	44	CYM1540	t_{AA} = 30, 35, 45	1125@30	PS, PF	Now
4M	512Kx8—SRAM	36	CYM1460	t_{AA} = 35, 45, 55, 70	625@35	PF, PS	Now
4M	512Kx8—SRAM	36	CYM1461	t_{AA} = 70, 85, 100	150@70	PF, PS	Now
4M	512Kx8—SRAM (JEDEC)	32	CYM1464	t_{AA} = 45, 55, 70	300@45	PD	Now

[odules (continued)

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages	Availability
·M	256Kx16–SRAM	48	CYM1641	t_{AA} = 25, 35, 45, 55	1800 @ 25	HD	Now
·M	64Kx32–SRAM	60	CYM1832	t_{AA} = 25, 35, 45, 55	980 @ 25	PZ	Now
·M	256Kx32–SRAM (JEDEC)	64	CYM1841	t_{AA} = 35, 45, 55	960 @ 35	PZ, PM	1Q90

ROMs

;ize	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages	Availability
·K	512x8–Registered	24S	CY7C255	$t_{SA/CO}$ = 25/12, 30/15	90	D, L, P	Now
;K	1024x8–Registered	24S	CY7C235	$t_{SA/CO}$ = 25/12, 30/15	90	D, L, P	Now
;K	1Kx8	24S	CY7C281	t_{AA} = 30, 45	90	D, L, P	Now
;K	1Kx8	24	CY7C282	t_{AA} = 30, 45	90	D, L, P	Now
.6K	2Kx8–Registered	24S	CY7C245/L	$t_{SA/CO}$ = 25/12, 35/15	100, 60	D, L, P, Q, W, S	Now
6K	2Kx8–Registered	24S	CY7C245A/L	$t_{SA/CO}$ = 15/10, 18/12	60 @ 35	D, L, P, Q, W, S	Now
.6K	2Kx8	24S	CY7C291/L	t_{AA} = 35, 40	90, 60	D, L, P, Q, W, S	Now
.6K	2Kx8	24S	CY7C291A/L	t_{AA} = 25, 30, 35, 50	60 @ 35	D, L, P, Q, W, S	Now
.6K	2Kx8	24	CY7C292/L	t_{AA} = 35, 50	90, 60	D, P	Now
.6K	2Kx8	24	CY7C292A	t_{AA} = 25, 30, 35, 50	60 @ 35	D, P	Now
.6K	2Kx8–CS Power Down	24S	CY7C293A/L	t_{AA} = 25, 30, 35, 50	60/15 @ 35	D, L, P, Q, W, S	Now
ı4K	8Kx8–CS Power Down	24S	CY7C261	t_{AA} = 35, 4045, 55	100/30	D, L, P, Q, W, S	Now
ı4K	8Kx8	24S	CY7C263	t_{AA} = 35, 40, 45, 55	100	D, L, P, Q, W, S	Now
ı4K	8Kx8	24	CY7C264	t_{AA} = 35, 40, 45, 55	100	D, P	Now
ı4K	8Kx8–Registered	28S	CY7C265	$t_{SA/CO}$ = 40/20	80	D, L, P, Q, W, S	Now
ı4K	8Kx8–EPROM Pinout	28	CY7C266	t_{AA} = 55	80/15	D, L, P, Q, W	Now
ı4K	8Kx8–Registered, Diagnostic	28S	CY7C269	$t_{SA/CO}$ = 40/20, 50/25	100	D, L, P, Q, W, S	Now
ı4K	8Kx8–Registered, Diagnostic	32	CY7C268	$t_{SA/CO}$ = 40/20, 50/25	100	D, L, Q, W	Now
28K	16Kx8–CS Power Down	28S	CY7C251	t_{AA} = 45, 55, 65	100/30	D, L, P, Q, W	Now
28K	16Kx8	28	CY7C254	t_{AA} = 45, 55, 65	100	D, P	Now
;56K	32Kx8–CS Power Down	28S	CY7C271	t_{AA} = 45, 55, 65	100/30	D, L, P, Q, W	Now
;56K	32Kx8–EPROM Pinout	28	CY7C274	t_{AA} = 45	120/30	D, L, P, Q, W	Now
;56K	32Kx8–Registered	28S	CY7C277	$t_{SA/CO}$ = 40/20	120/30	D, L, P, Q, W	Now
;56K	32Kx8–Latched	28	CY7C279	t_{AA} = 45	120	D, L, P, Q, W	Now
;12K	64Kx8	28	CY7C286	t_{AA} = 60	120/40	Q, W	1Q90
;12K	64Kx8–Registered	28S	CY7C287	t_{CO} = 20	180	Q, W	1Q90
;12K	64Kx8 with ALE	28S	CY7C285	t_{AA} = 30	180	Q, W	1Q90
;12K	64Kx8 with ALE	32S	CY7C289	t_{AA} = 30	180	Q, W	1Q90

LDs

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA @ ns)	Packages	Availability
ΛL20	16L8	20	PALC16L8/L	t_{PD} = 20	70, 45	D, L, P, Q, V, W	Now
ΛL20	16R8	20	PALC16R8/L	$t_{S/CO}$ = 15/12	70, 45	D, L, P, Q, V, W	Now
ΛL20	16R6	20	PALC16R6/L	$t_{PD/S/CO}$ = 20/20/15	70, 45	D, L, P, Q, V, W	Now
ΛL20	16R4	20	PALC16R4/L	$t_{PD/S/CO}$ = 20/20/15	70, 45	D, L, P, Q, V, W	Now
LD20	18G8–Generic	20	PLDC18G8	$t_{PD/S/CO}$ = 12/12/10	90	D, L, P, Q, V, W	4Q89
LD24	22V10–Macrocell	24S	PALC22V10/L	$t_{PD/S/CO}$ = 25/15/15, 20/12/12	90, 55	D, L, P, Q, W, J, H	Now
LD24	22V10–Macrocell	24S	PALC22V10B	$t_{PD/S/CO}$ = 15/10/10	90, 55	D, L, P, Q, W, J, H	Now
LD24	22V10–Macrocell	24S	PAL22V10C	$t_{PD/S/CO}$ = 10/3.6/7.5, 12/4.5/9.5	190	D, L, P, J	4Q89
LD24	22VP10–Macrocell	24S	PAL22VP10C	$t_{PD/S/CO}$ = 10/3.6/7.5, 12/4.5/9.5	190	D, L, P, J	1Q90
LD24	20G10–Generic	24S	PLDC20G10	$t_{PD/S/CO}$ = 25/15/15	55	D, L, P, Q, W, J, H	Now
LD24	20G10–Generic	24S	PLDC20G10B	$t_{PD/S/CO}$ = 15/12/10	70	D, L, P, Q, W, J, H	Now
LDB24	20G10–Generic	24S	PLDC20G10C	$t_{PD/S/CO}$ = 10/3.6/7.5, 12/4.5/9.5	190	D, L, P, J	2Q90
LD24	20RA10–Asynchronous	24S	PLD20RA10	$t_{PD/S/CO}$ = 20/10/20	80	D, L, P, Q, W, J, H	Now
LD28	7C330–State Machine	28S	CY7C330	f_{MAX}, t_{IS}, t_{CO} = 66 MHz/3 ns/12 ns	130	D, L, P, Q, W, J, H	Now
LD28	7C331–Asynchronous	28S	CY7C331	$t_{PD/S/CO}$ = 20/12/20	120	D, L, P, Q, W, J, H	Now
LD28	7C332–Combinatorial	28S	CY7C332	t_{PD} = 20	120	D, L, P, Q, W, J, H	Now
LD28	7C361–32 Macrocell	28S	CY7C361	f_{MAX} = 125 MHz	140	Q, W, H	2Q90
[AX28	7C344–32 Macrocell	28S	CY7C344	$t_{PD/S/CO}$ = 20/10/15	120	D, L, P, Q, W, J, H	Now

PLDs (continued)

Size	Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	Packages	Availability
MAX40	7C345 – 128 Macrocell	40/44	CY7C345	$t_{PD/S/CO}$ = 30/22/15	150	D, L, P, Q, J, H	3Q89
MAX68	7C342 – 128 Macrocell	68	CY7C342	$t_{PD/S/CO}$ = 30/22/15	150	L, J, G, H, R	Now

ECL PLDs

Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	Packages	Availability
16P8 – 10KH	24	CY10E301	t_{PD} = 3.5, 4	240	D, K, Y	Now
16P8 – 10KH	24	CY10E301L	t_{PD} = 6	70	P, J	Now
16P8 – 100K	24	CY100E301	t_{PD} = 3.5, 4	240	D, K, Y	Now
16P8 – 100K	24	CY100E301L	t_{PD} = 6	70	P, J	Now
16P4 – 10KH	24	CY10E302	t_{PD} = 3, 4	220	D, K, Y	Now
16P4 – 10KH	24	CY10E302L	t_{PD} = 4	70	P, J	Now
16P4 – 100K	24	CY100E302	t_{PD} = 3, 4	220	D, K, Y	Now
16P4 – 100K	24	CY100E302L	t_{PD} = 4	70	P, J	Now

FIFOs

Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	Packages	Availability
64 x 4 – Cascadeable	16	CY3341	1.2, 2 MHz	45	D, P	Now
64 x 4 – Cascadeable	16	CY7C401	5, 10, 15, 25 MHz	75	D, L, P, V	Now
64 x 4 – Cascadeable/OE	16	CY7C403	10, 15, 25 MHz	75	D, L, P, V	Now
64 x 5 – Cascadeable	18	CY7C402	5, 10, 15, 25 MHz	75	D, L, P, V	Now
64 x 5 – Cascadeable/OE	18	CY7C404	10, 15, 25 MHz	75	D, L, P, V	Now
64 x 8 – Cascadeable/OE	28S	CY7C408A	15, 25, 35 MHz	120	D, L, P, V	Now
64 x 9 – Cascadeable	28S	CY7C409A	15, 25, 35 MHz	120	D, L, P, V	Now
512 x 9 – Cascadeable	28	CY7C420	25, 30, 40, 65 ns	100	D, P	Now
512 x 9 – Cascadeable	28S	CY7C421	25, 30, 40, 65 ns	100	D, J, L, P, V	Now
1K x 9 – Cascadeable	28	CY7C424	25, 30, 40, 65 ns	100	D, P	Now
1K x 9 – Cascadeable	28S	CY7C425	25, 30, 40, 65 ns	100	D, J, L, P	Now
2K x 9 – Cascadeable	28	CY7C428	25, 30, 40, 65 ns	100	D, P	Now
2K x 9 – Cascadeable	28S	CY7C429	25, 30, 40, 65 ns	100	D, J, L, P, V	Now
2K x 9 – Bidirectional	28S	CY7C439	30, 40, 65 ns	120	D, J, L, P, V	2Q90
4K x 9 – Cascadeable	28	CY7C432	25, 30, 40, 65 ns	140	D, P	Now
4K x 9 – Cascadeable	28S	CY7C433	25, 30, 40, 65 ns	140	D, J, L, P, V	Now

Logic

Organization	Pins	Part Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	Packages	Availability
2901 – 4-Bit Slice	40	CY7C901	t_{CLK} = 23, 31	70	D, L, P, J	Now
2901 – 4-Bit Slice	40	CY2901	C	140	D, P	Now
4 x 2901 – 16-Bit Slice	64	CY7C9101	t_{CLK} = 30, 40	60	D, L, P, J	Now
29116 – 16-Bit Controller	52	CY7C9116	t_{CLK} = 35, 45, 53, 79, 100	145	D, L, G, J	Now
29116 – 16-Bit Controller	52	CY7C9115	t_{CLK} = 35, 45, 53, 79, 100	145	J	Now
29117 – 16-Bit Controller	68	CY7C9117	t_{CLK} = 35, 45, 53, 79, 100	145	L, G, J	Now
2909 – Sequencer	28	CY7C909	t_{CLK} = 30, 40	55	D, L, P, J	Now
2911 – Sequencer	20	CY7C911	t_{CLK} = 30, 40	55	D, L, P, J	Now
2909 – Sequencer	28	CY2909	A	70	D, P	Now
2911 – Sequencer	20	CY2911	A	70	D, P	Now
2910 – Controller (17-word Stack)	40	CY7C910	t_{CLK} = 40, 50, 93	100	D, L, P, J	Now
2910 – Controller (9-word Stack)	40	CY2910	A	170	D, L, P, J	Now
16 x 16 Multiplier	64	CY7C516	t_{MC} = 38, 45, 55, 75	100 @ 10 MHz	D, L, P, G, J	Now
16 x 16 Multiplier	64	CY7C517	t_{MC} = 38, 45, 55, 75	100 @ 10 MHz	D, L, P, G, J	Now
16 x 16 Multiplier/Accumulator	64	CY7C510	t_{MC} = 45, 55, 65, 75	100 @ 10 MHz	D, L, P, G, J	Now

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[SC

Desc.	Organization	Pins	Part Number	Speed (ns)	ICC/ISB/ICCDR (mA @ ns)	Packages	Availability
U	SPARC 32-bit Integer Unit	207	CY7C601	t_{CYC} = 40, 33, 25 MHz	600	G, B	Now
'PU	Floating-Point Unit (Controller and Processor)	143	CY7C602	t_{CYC} = 33, 25 MHz	400	G, K	Now
:MU	Cache-Controlled Memory Management Unit	243	CY7C604	t_{CYC} = 33, 25 MHz	600	G, K	Now
:MU- 1P	Cache Controller and Multiprocessing Memory Management Unit	243	CY7C605	t_{CYC} = 33, 25 MHz	600	G, K	2Q90
U	SPARC 32-bit Integer Unit for Embedded Control	160	CY7C611	t_{CYC} = 25 MHz	600	G160	Now
:RAM	SPARC Cache RAM	52	CY7C157	t_{CYC} = 33, 24, 20 MHz	250	J, L	Now

esign and Programming Tools

Part Name	Type	Part Number
)uickPro	Programmer	CY3000
)uickPro II	Programmer	CY3300
'LD ToolKit	Design Tool	CY3101
1AX + PLUS	Design Tool	CY3201
)P2 – MAX PLD Programmer	Programmer	CY3202

tes:

e above specifications are for the commercial temperature range of 0°C to 70°C. Military temperature range (–55°C to +125°C) product ocessed to MIL-STD-883 Revision C is also available. Speed and power selections may vary from those above.

mmercial grade product is available in plastic, CERDIP, or LCC. Military grade product is available in CERDIP, LCC, or PGA. F, K, and T :kages are special order only.

power supplies are V_{CC} = 5V ± 10%.

;, 24S, 28S stands for 300 mil. 22-pin, 24-pin, 28-pin, respectively. 28.4 stands for 28-pin 400 mil, 24.4 stands for 24-pin 400 mil.

CC, SOJ, and SOIC packages are available on some products.

K, and T packages are special order only.

\X and MAX+PLUS are trademarks of Altera Corporation.

:kage Code:

= PLASTIC PIN GRID ARRAY	S = SOIC
= CERDIP	T = WINDOWED CERPAK
= FLATPAK	V = SOJ
= PIN GRID ARRAY (PGA)	W = WINDOWED CERDIP
= WINDOWED HERMETIC LCC	X = DICE
= PLCC	HD = HERMETIC DIP
= CERPAK	HV = HERMETIC VERTICAL DIP
= LEADED CHIP CARRIER (LCC)	PF = PLASTIC FLAT SIP
= PLASTIC	PF = PLASTIC SIP
= WINDOWED LCC	PZ = PLASTIC ZIP
= WINDOWED PGA	Y = CERAMIC LCC

Ordering Information

In general, the codes for all products (except modules) follow the format below.

PAL & PLD

PREFIX	DEVICE	SUFFIX	FAMILY
PAL C	16R8	-25 P C	PAL 20
PAL C	16R8	L-35 P C	LOW POWER PAL 20
PAL C	22V10	-25 W C	PAL 24 VARIABLE PRODUCT TERMS
PLD C	20G10	-25 W C	GENERIC PLD 24
CY	7C330	-33 P C	PLD SYNCHRONOUS STATE MACHINE
CY	10E302	-2.5 D C	10K ECL PLD
CY	100E302	-2.5 D C	100K ECL PLD

RAM, PROM, FIFO, μP, ECL

PREFIX	DEVICE	SUFFIX	FAMILY
CY	7C128	-45 D M B	CMOS SRAM
CY	7B185	-15 V C	BiCMOS SRAM
CY	7C245	L-35 P C	PROM
CY	7C404	-25 D M B	FIFO
CY	7C901	-23 P C	μP
CY	10E415	-3 D C	10K ECL SRAM
CY	100E415	-3 F C	100K ECL SRAM

PROCESSING
B = HI REL MIL STD 883C FOR MILITARY PRODUCT
= LEVEL 2 PROCESSING FOR COMMERCIAL PRODUCT
T = SURFACE-MOUNTED DEVICES (V & S PACKAGE) TO BE TAPE AND REELED
R = LEVEL 2 PROCESSING ON TAPE AND REEL DEVICES

TEMPERATURE RANGE
C = COMMERCIAL (0°C TO 70°C)
I = INDUSTRIAL (-40°C TO +85°C)
M = MILITARY (-55°C TO +125°C)

PACKAGE
D = CERDIP
F = FLATPAK
G = PIN GRID ARRAY (PGA)
H = WINDOWED LEADED CHIP CARRIER
J = PLCC
K = CERPAK (GLASS-SEALED FLAT PACKAGE)
L = LEADLESS CHIP CARRIER
P = PLASTIC
Q = WINDOWED LEADLESS CHIP CARRIER
R = WINDOWED PGA
S = SOIC (GULL WING)
T = WINDOWED CERPAK
V = SOIC (J LEAD)
W = WINDOWED CERDIP
X = DICE (WAFFLE PACK)
Y = CERAMIC LEADED CHIP CARRIER

SPEED (ns or MHz)

L = LOW-POWER OPTION
A, B, C = REVISION LEVEL

i.e., CY7C128-35PC, PALC16R8L-25PC

Ordering Information

The codes for module products follow the the format below.

PREFIX	DEVICE	SUFFIX
CYM	1001	H D -120 M B

PROCESSING
B = MILITARY STANDARD 883
= STANDARD

TEMPERATURE RANGE
C = 0°C TO 70°C
I = -40°C TO 85°C
M = -55°C TO 125°C

SPEED

CONFIGURATION
D = DUAL-IN-LINE
G = PIN GRID ARRAY
Q = QUAD-IN-LINE
S = SINGLE-IN-LINE
V = VERTICAL DIP
Z = ZIGZAG-IN-LINE

TYPE
H = HERMETIC
P = PLASTIC

Cypress FSCM #65786

Notes:
PLCC, SOJ, and SOIC packages are available on some products.
MAX and MAX+PLUS are trademarks of Altera Corporation.

CYPRESS	CYPRESS
2147–35C	7C147–35C
2147–45C	2147–35C
2147–45C	7C147–45C
2147–45M+	7C147–45M+
2147–55C	2147–45C
2147–55M	2147–45M
2148–35C	21L48–35C
2148–35C	7C148–35C
2148–35M	7C148–35M
2148–45C	2148–35C
2148–45C	21L48–45C
2148–45M	2148–35M
2148–45M+	7C148–45M+
2148–55C	2148–45C
2148–55C	21L48–55C
2148–55M	2148–45M
2149–35C	21L49–35C
2149–35C	7C149–35C
2149–35M	7C149–35M
2149–45C	21L49–45C
2149–45M	2149–35M
2149–45M	7C149–45M
2149–55C	2149–45C
2149–55C	21L49–55C
2149–55M	2149–45M
21L48–35C	7C148–35C
21L48–45C	21L48–35C
21L48–45C	7C148–45C
21L48–55C	21L48–45C
21L49–35C	7C149–25C
21L49–45C	21L49–35C
21L49–45C	7C149–45C
21L49–55C	21L49–45C
27S03AC	7C189–25C
27S03AM	7C189–25M
27S03C	27S03AC
27S03C	74S189C
27S03M	27S03AM
27S03M	54S189M
27S07AC	7C190–25C
27S07AM	7C190–25M
27S07C	27S07AC
27S07M	27S07AM
27S07M	7C190–25M
2901CC	7C901–31C
2901CM	7C901–32M
2909AC	7C909–40C
2909AM	7C909–40M
2910AC	7C910–50C
2910AM	7C910–51M
2910C	2910AC
2910M	2910AM
2911AC	7C911–40C
2911AM	7C911–40M
3341–2C	7C401–5C+
3341–2M	7C401–10M
3341C	3341–2C
3341M	3341–2M
54S189M	27S03M
6116–35C	6116–35C
6116–45C	6116–35C
6116–45M	6116–45M

CYPRESS	CYPRESS
6116–55C	6116–45C
6116–55M	6116–45M
74S189C	27S03C
7C122–25C	7C122–15C+
7C122–35C	7C122–25C
7C122–35M	7C122–25M
7C123–12C	7C123–7C
7C128–35C	7C128–25C
7C128–35M	7C128–35M
7C128–45C	7C128–35C
7C128–45M	7C128–35M+
7C128–55C	7C128–45C+
7C128–55M	7C128–45M+
7C130–45C	7C130–35C
7C130–45M	7C130–45M
7C130–55C	7C130–45C
7C130–55M	7C130–45M
7C131–45C	7C131–35C
7C131–45M	7C131–45M
7C131–55C	7C131–45C
7C131–55M	7C131–45M
7C132–35C	7C132–35C
7C132–45C	7C132–35C
7C132–55C	7C132–45C
7C132–55M	7C132–45M
7C136–35C	7C136–35C
7C136–45C	7C136–35C
7C136–55C	7C136–45C
7C136–55M	7C136–45M
7C140–35C	7C140–25C
7C140–45C	7C140–35C
7C140–55C	7C140–45C
7C141–35C	7C141–25C
7C141–45C	7C141–35C
7C141–55C	7C141–45C
7C147–35C	7C147–25C+
7C147–35M+	7C147–35M+
7C147–45C	7C147–35C
7C148–25C	7C148–25C
7C148–35C	7C148–25C+
7C148–45C	7C148–35C
7C149–35C	7C149–25C+
7C149–45C	7C149–35C
7C149–45M	7C149–35M
7C150–25C	7C150–15C
7C150–35C	7C150–25C
7C150–35M	7C150–25M
7C167–35C	7C167–25C
7C167–45M	7C167–35M+
7C168–35C	7C168–25C
7C168–45M	7C168–35M+
7C169–35C	7C169–25C
7C169–40M	7C169–35M+
7C170–35C	7C170–25C
7C170–45C	7C170–35C
7C170–45M	7C170–35M
7C171–35C	7C171–25C
7C171–35M	7C171–35M
7C171–45M	7C171–35M+
7C172–35C	7C172–25C
7C172–45M	7C172–35M+
7C186L–45M	7C186–45M

CYPRESS	CYPRESS
7C189–25C	7C189–15C+
7C190–25C	7C190–15C+
7C191–45M	7C191–35M
7C192–45M	7C192–35M
7C194–35C	7C194–25C
7C194–45C	7C194–35C+
7C194–45M	7C194–35M
7C196–35C	7C196–25C
7C196–35M	7C196–35M
7C196–45C	7C196–35C+
7C197–35C	7C197–25C
7C197–45C	7C197–35C+
7C197–45M	7C197–35M
7C198–45C	7C198–35C
7C198–55C	7C198–45C+
7C198–55M	7C198–45M
7C199–45C	7C199–35C
7C199–55C	7C199–45C+
7C199–55M	7C199–45M
7C225–30C	7C225–25C
7C225–30M	7C225–25M
7C225–40C	7C225–30C
7C225–40M	7C225–35M
7C235–40C	7C235–30C
7C245–35C	7C245–25C
7C245–45C	7C245–35C
7C245–45M	7C245–35M
7C245A–25C	7C245A–18C
7C245A–35C	7C245AL–35C
7C245A–35M	7C245A–25M
7C245AL–35C	7C245A–25C+
7C245L–35C	7C245–35C+
7C245L–45C	7C245L–35C
7C251–55C	7C251–45C
7C251–65C	7C251–55C
7C251–65C	7C251–55C
7C251–65M	7C251–55M
7C253–65M	7C253–55M
7C254–45C	7C254–45C
7C254–55C	7C254–45C
7C254–65C	7C254–55C
7C254–65M	7C254–55M
7C261–35C	7C261–35C
7C261–45C	7C261–35C
7C261–45M	7C261–45M
7C261–55C	7C261–45C
7C261–55M	7C261–45M
7C263–35C	7C263–35C
7C263–45C	7C263–35C
7C263–45M	7C263–45M
7C263–55C	7C263–45C
7C263–55M	7C263–45M
7C264–35C	7C264–35C
7C264–45C	7C264–35C
7C264–45M	7C264–45M
7C264–55C	7C264–45C
7C264–55M	7C264–45M
7C268–50C	7C268–40C+
7C268–60C	7C268–50C
7C268–60M	7C268–50M+
7C269–50C	7C269–40C+
7C269–60C	7C269–50C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
– = functionally equivalent.
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

CYPRESS	CYPRESS
7C269-60M	7C269-50M+
7C281-45C	7C281-30C
7C282-45C	7C282-30C+
7C282-45M	7C282-45M
7C291-35C	7C291-25C+
7C291-35M	7C291-35M
7C291-50C	7C291-35C
7C291-50M	7C291-35M
7C291A-35C	7C291AL-35C
7C291A-35M	7C291A-30M
7C291A-50C	7C291AL-50C
7C291A-50M	7C291A-35M
7C291AL-35C	7C291A-25C+
7C291AL-50C	7C291AL-35C
7C291L-35C	7C291-35C+
7C291L-50C	7C291L-35C
7C292-35C	7C292-25C+
7C292-50C	7C292-35C
7C292L-35C	7C292-35C+
7C292L-50C	7C292L-35C
7C293A-35C	7C293AL-35C
7C293A-35M	7C293A-30M
7C293A-50C	7C293AL-50C
7C293A-50M	7C293A-35M
7C293AL-35C	7C293A-20C+
7C293AL-50C	7C293AL-35C
7C401-10C	7C401-15C
7C401-10M	7C401-15M
7C401-5C	7C401-10C
7C402-10C	7C402-15C
7C402-10M	7C402-15M
7C402-5C	7C402-10C
7C403-10C	7C403-15C
7C403-10M	7C403-15M
7C403-15C	7C403-25C
7C403-15M	7C403-25M
7C404-10C	7C404-15C
7C404-10M	7C404-15M
7C404-15C	7C404-25C
7C404-15M	7C404-25M
7C408-15C	7C408-25C
7C408-15M	7C408-25M
7C408-25C	7C408-35C
7C409-15C	7C409-25C
7C409-15M	7C409-25M
7C409-25C	7C409-35C
7C420-40C	7C420-30C
7C420-40M	7C420-30M
7C420-65C	7C420-40C
7C420-65M	7C420-40M
7C421-40C	7C421-30C
7C421-40M	7C421-30M
7C421-65C	7C421-40C
7C421-65M	7C421-40M
7C424-40C	7C424-30C
7C424-40M	7C424-30M
7C424-65C	7C424-40C
7C424-65M	7C424-40M
7C425-40C	7C425-30C
7C425-40M	7C425-30M
7C425-65C	7C425-40C
7C425-65M	7C425-40M

CYPRESS	CYPRESS
7C428-40C	7C428-30C
7C428-40M	7C428-30M
7C428-65C	7C428-40C
7C428-65M	7C428-40M
7C429-40C	7C429-30C
7C429-40M	7C429-30M
7C429-65C	7C429-40C
7C429-65M	7C429-40M
7C510-55C	7C510-45C
7C510-65C	7C510-55C
7C510-65M	7C510-55M
7C510-75C	7C510-65C
7C510-75M	7C510-65M
7C516-45C	7C516-38C
7C516-55C	7C516-45C
7C516-55M	7C516-42M
7C516-75C	7C516-55C
7C516-75M	7C516-55M
7C517-45C	7C517-38C
7C517-55C	7C517-45C
7C517-55M	7C517-42M
7C517-75C	7C517-55C
7C517-75M	7C517-55M
7C901-31C	7C901-23C+
7C901-32M	7C901-27M
7C909-40C	7C909-30C
7C909-40M	7C909-30M
7C910-50C	7C910-40C
7C910-51M	7C910-46M
7C910-93C	7C910-50C
7C910-99M	7C910-51M
7C9101-40C	7C9101-30C
7C9101-45M	7C9101-35M
7C911-40C	7C911-30C
7C911-40M	7C911-30M
9122-25C	7C122-15C
9122-25C	91L22-25C
9122-35C	9122-25C
9122-35C	91L22-35C
9122-45C	93L422C
91L22-25C	7C122-25C
91L22-35C	7C122-35C
91L22-45C	93L422AC
93422AC	7C122-35C
93422AC	9122-35C
93422AM	7C122-35M
93422C	93L422AC
93422M	93422AM
93422M	93L422AM
93L422AC	7C122-35C
93L422AC	91L22-45C
93L422AM	7C122-35M
93L422C	93L422AC
93L422M	93L422AM
PALC16L8-25C	PALC16L8L-25C
PALC16L8-30M	PALC16L8-20M
PALC16L8-35C	PALC16L8-25C
PALC16L8-40M	PALC16L8-30M
PALC16L8L-35C	PALC16L8L-25C
PALC16R4-25C	PALC16R4L-25C
PALC16R4-30M	PALC16R4-20M
PALC16R4-35C	PALC16R4-25C

CYPRESS	CYPRESS
PALC16R4-40M	PALC16R4-30M
PALC16R4L-35C	PALC16R4L-25C
PALC16R6-25C	PALC16R6L-25C
PALC16R6-30M	PALC16R6-20M
PALC16R6-35C	PALC16R6-25C
PALC16R6-40M	PALC16R6-30M
PALC16R6L-35C	PALC16R6L-25C
PALC16R8-25C	PALC16R8L-25C
PALC16R8-30M	PALC16R8-20M
PALC16R8-35C	PALC16R8-25C
PALC16R8-40M	PALC16R8-30M
PALC16R8L-35C	PALC16R8L-25C
PALC22V10-35C	PALC22V10-25C
PALC22V10-40M	PALC22V10-30M
PALC22V10L-25C	PALC22V10-25C
PALC22V10L-35C	PALC22V10L-25C
PLDC20G10-35C	PLDC20G10-25C
PLDC20G10-40M	PLDC20G10-30M

AMD	CYPRESS
PREFIX:Am	PREFIX:CY
PREFIX:SN	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
2130-100C	7C130-55C
2130-120C	7C130-55C
2130-70C	7C130-55C
2147-35C	2147-35C
2147-45C	2147-45C
2147-45M	2147-45M
2147-55C	2147-55C
2147-55M	2147-55M
2147-70C	2147-55C
2147-70M	2147-55M
2148-35C	2148-35C
2148-35M	2148-35M
2148-45C	2148-45C
2148-45M	2148-45M
2148-55C	2148-55C
2148-55M	2148-55M
2148-70C	2148-55C
2148-70M	2148-55M
2149-35C	2149-35C
2149-45C	2149-45C
2149-45M	2149-45M
2149-55C	2149-55C
2149-55M	2149-55M
2149-70C	2149-55C
2149-70M	2149-55M
2167-35C	7C167-35C
2167-35M	7C167-35M
2167-45C	7C167-45C
2167-45M	7C167-45M
2167-55C	7C167-45C
2167-55M	7C167-45M
2167-70C	7C167-45C
2167-70M	7C167-45M
2168-35C	7C168-35C
2168-45C	7C168-45C

AMD	CYPRESS
2168-45M	7C168-45M
2168-55C	7C168-45C
2168-55M	7C168-45M
2168-70C	7C168-45C
2168-70M	7C168-45M
2169-40C	7C169-40C
2169-50C	7C169-40C
2169-50M	7C169-40M
2169-70C	7C169-40C
2169-70M	7C169-40M
21L47-45C	7C147-45C
21L47-55C	7C147-45C
21L47-70C	7C147-45C
21L48-45C	21L48-45C
21L48-55C	21L48-55C
21L48-70C	21L48-55C
21L49-45C	21L49-45C
21L49-55C	21L49-55C
21L49-70C	21L49-55C
27C191-25C	7C292A-25C
27C191-35C	7C291A-25C+
27C191-35C	7C291A-35C
27C191-35C	7C292A-35C
27C191-35C	7C292AL-35C
27C191-35M	7C292A-30M
27C191-45M	7C291A-45M
27C256-55C	7C291A-45M
27C256-90M	7C291A-45M
27C291-25C	7C291A-25C
27C291-35C	7C291AL-35C
27C291-45M	7C291A-35M
27C291A-30M	7C291A-30M
27LS03C	27LS03C
27LS03M	27LS03M+
27LS07C	27S07C+
27LS191C	7C292-35C
27LS291C	7C291-35C
27LS291M	7C291-35M
27PS181AC	7C282-45C
27PS181AM	7C282-45M+
27PS181C	7C282-45C
27PS181M	7C282-45M+
27PS191AC	7C292-50C
27PS191AM	7C292-50M+
27PS191C	7C292-50C
27PS191M	7C292-50M+
27PS281AC	7C281-45C
27PS281AM	7C281-45M+
27PS281C	7C281-45C
27PS281M	7C281-45M+
27PS291AC	7C291-50C
27PS291AM	7C291-50M+
27PS291C	7C291-50C
27PS291M	7C291-50M+
27S03AC	27S03AC
27S03AM	27S03AM
27S03C	27S03C
27S03M	27S03M
27S07AC	27S07AC
27S07AM	27S07AM
27S07C	27S07C
27S07M	27S07M,

AMD	CYPRESS
27S181AC	7C282-30C
27S181AM	7C282-45M
27S181C	7C282-45C
27S181M	7C282-45M
27S191AC	7C292-35C
27S191AM	7C292-50M
27S191C	7C292-50C
27S191M	7C292-50M
27S191SAC	7C292A-20C
27S25AC	7C225-30C
27S25AM	7C225-35M
27S25C	7C225-40C
27S25M	7C225-40M
27S25SAC	7C225-25C
27S25SAM	7C225-35M
27S281AC	7C281-30C
27S281AM	7C281-45M
27S281C	7C281-45C
27S281M	7C281-45M
27S291AC	7C291-35C
27S291AM	7C291-50M
27S291C	7C291-50C
27S291M	7C291-50M
27S291SAC	7C291A-25C
27S291SAM	7C291A-30M
27S35AC	7C235-30C
27S35AM	7C235-40M
27S35C	7C235-40C
27S35M	7C235-40M
27S45AC	7C245-35C
27S45AM	7C245-45M
27S45C	7C245-45C
27S45M	7C245-45M
27S45SAC	7C245-25C
27S45SAM	7C245A-25M-
27S49AC	7C264-40C
27S49AC-45	7C264-45C
27S49AC-45T	7C263-45C
27S49AC-T	7C263-40C
27S49ALM	7C263-45M
27S49C-T	7C263-55C
27S49LM	7C263-55M
27S49AM	7C264-55M
27S49C	7C264-55C
27S49M	7C264-55M
27S51C	7C254-55C
27S51M	7C254-65M
2841AC	3341C
2841AM	3341M
2841C	3341C
2841M	3341M
2901BC	2901CC
2901BM	2901CM
2901CC	2901CC
2901CM	2901CM
2909AC	2909AC
2909AM	2909AM
2909C	2909AC
2909M	2909M
2910-1C	2910C
2910-1M	2910M
2910AC	2910AC

AMD	CYPRESS
2910AM	2910AM
2910C	2910C
2910M	2910M
29116AC	7C9116AC
29116AM	7C9116AM
29116C	7C9116AC
29116M	7C9116AM
29117C	7C9117AC
29117M	7C9117AM
2911AC	2911AC
2911AM	2911AM
2911C	2911AC
2911M	2911M
29510C	7C510-75C
29510M	7C510-75M
29516AM	7C516-55M
29516C	7C516-55C
29516M	7C516-55M
29517AC	7C517-38C
29517C	7C517-55C
29517M	7C517-55M
29701C	27S07C
29701M	27S07M
29703C	27S03C
29703M	27S03M
29C01-1C	7C901-23C+
29C01BA	7C901-32M
29C01BC	7C901-31C
29C01C	7C901-31C
29C01CC	7C901-31C
29C10-1C	7C910-40C
29C101C	7C9101-40C
29C101M	7C9101-35M
29C10ABA	7C910-51M
29C10AC	7C910-50C
29C10AC	7C910-93C
29C116C	7C9116AC
29C116M	7C9116AM
29C117C	7C9117AC
29L116AC	7C9116AC
29L116AM	7C9116AM
29L510C	7C510-75C
29L510M	7C510-75M
29L516C	7C516-75C
29L516M	7C516-75M
29L517C	7C517-75C
29L517M	7C517-75M
3341C	3341C
3341M	3341M
54S189M	54S189M
7201-25C	7C420-25C
7201-25RC	7C421-25C
7201-35C	7C420-30C
7201-35RC	7C421-30C
7201-50C	7C420-40C
7201-50RC	7C421-40C
7201-65C	7C420-65C
7201-65RC	7C421-65C
7202-25C	7C424-25C
7202-25RC	7C425-25C
7202-35C	7C424-30C
7202-35RC	7C425-30C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
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† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

AMD	CYPRESS
7202-50C	7C424-40C
7202-50RC	7C425-40C
7202-65C	7C424-65C
7202-65RC	7C425-65C
7203-25C	7C428-25C
7203-25RC	7C429-25C
7203-35C	7C428-30C
7203-35RC	7C429-30C
7203-50C	7C428-40C
7203-50RC	7C429-40C
7203-65C	7C428-65C
7203-65RC	7C429-65C
7204-25D	7C432-25D
7204-25J	7C433-25LC
7204-25P	7C432-25P
7204-35D	7C432-30D
7204-35J	7C433-30LC
7204-35P	7C432-30P
7204-50D	7C432-40D
7204-50J	7C433-40LC
7204-50P	7C432-40P
7204-65D	7C432-65D
7204-65J	7C433-65LP
7204-65P	7C432-65P
74S189C	74S189C
9122-25C	9122-25C
9122-35C	9122-35C
9122-35M	7C122-35M
9128-100C	6116-55C
9128-120M	6116-55M
9128-150C	6116-55C
9128-150M	6116-55M
9128-200C	6116-55C
9128-200M	6116-55M
9128-70C	6116-55C
9128-90M	6116-55M
9150-20C	7C150-15C
9150-25C	7C150-25C
9150-25M	7C150-25M
9150-35C	7C150-35C
9150-35M	7C150-35M
9150-45C	7C150-35C
9150-45M	7C150-35M
91L22-35C	91L22-35C
91L22-35M	7C122-35M
91L22-45C	91L22-45C
91L22-45M	7C122-35M
91L22-60C	7C122-35C+
91L50-25C	7C150-25C
91L50-35C	7C150-35C
91L50-45C	7C150-35C
93422AC	93422AC
93422AM	93422AM
93422C	93422C
93422M	93422M
93L422AC	93L422AC
93L422AM	93L422AM
93L422C	93L422C
93L422M	93L422M
99C164-35C	7C164-35C+
99C164-45C	7C164-45C+
99C164-45M	7C164-45M+

AMD	CYPRESS
99C164-55C	7C164-45C+
99C164-55M	7C164-45M+
99C164-70C	7C164-45C+
99C164-70M	7C164-45M
99C165-35C	7C166-35C+
99C165-45C	7C166-45C+
99C165-45M	7C166-45M+
99C165-55C	7C166-45C+
99C165-55M	7C166-45M+
99C165-70C	7C166-45C+
99C165-70M	7C166-45M+
99C641-25C	7C187-25C
99C641-35C	7C187-35C
99C641-45C	7C187-45C
99C641-45M	7C187-45M
99C641-55C	7C187-45C
99C641-55M	7C187-45M
99C641-70C	7C187-45C
99C641-70M	7C187-45M
99C68-35C	7C168-35C
99C68-45C	7C168-45C*
99C68-45M	7C168-45M*
99C68-55C	7C168-45C*
99C68-55M	7C168-45M*
99C68-70C	7C168-45C*
99C68-70M	7C168-45M*
99C88H-35C	7C186-35C
99C88H-45C	7C186-45C
99C88H-45M	7C186-45M
99C88H-55C	7C186-55C
99C88H-55M	7C186-55M
99C88H-70C	7C186-55C
99C88H-70M	7C186-55M
99CL68-35C	7C168-35C
99CL68-45C	7C168-45C*
99CL68-45M	7C168-45M*
99CL68-55C	7C168-45C*
99CL6855M	7C168-45M*
99CL68-70C	7C168-45C*
99CL68-70M	7C168-45M*
PAL16L8A-4C	PALC16L8L-35C
PAL16L8A-4M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8ALC	PALC16L8-25C
PAL16L8ALM	PALC16L8-30M
PAL16L8AM	PALC16L8-30M
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8LC	PALC16L8-35C
PAL16L8LM	PALC16L8-40M
PAL16L8M	PALC16L8-40M
PAL16L8QC	PALC16L8L-35C
PAL16L8QM	PALC16L8-40M
PAL16R4A-4C	PALC16R4L-35C
PAL16R4A-4M	PALC16R4-40M
PAL16R4ALC	PALC16R4-25C
PAL16R4ALM	PALC16R4-30M
PAL16R4AM	PALC16R4-30M
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4LC	PALC16R4-35C
PAL16R4LM	PALC16R4-40M

AMD	CYPRESS
PAL16R4M	PALC16R4-40M
PAL16R4QC	PALC16R4L-35C
PAL16R4QM	PALC16R4-40M
PAL16R6A-4C	PALC16R6L-35C
PAL16R6A-4M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6ALC	PALC16R6-25C
PAL16R6ALM	PALC16R6-30M
PAL16R6AM	PALC16R6-30M
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6LC	PALC16R6-35C
PAL16R6LM	PALC16R6-40M
PAL16R6M	PALC16R6-40M
PAL16R6QC	PALC16R6L-35C
PAL16R6QM	PALC16R6-40M
PAL16R8A-4C	PALC16R8L-35
PAL16R8A-4M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8ALC	PALC16R8-25C
PAL16R8ALM	PALC16R8-30M
PAL16R8AM	PALC16R8-30M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8LC	PALC16R8-35C
PAL16R8LM	PALC16R8-40M
PAL16R8M	PALC16R8-40M
PAL16R8QC	PALC16R8L-35
PAL16R8QM	PALC16R8-40M
PAL22V10AC	PALC22V10-25C
PAL22V10AM	PALC22V10-30M
PAL22V10C	PALC22V10-35C
PAL22V10M	PALC22V10-40M

ANALOG DEV	CYPRESS
PREFIX:ADSP	PREFIX:CY
SUFFIX:883B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:E	SUFFIX:L
SUFFIX:F	SUFFIX:F
SUFFIX:G	SUFFIX:G
1010A	7C510-65C+
1010J	7C510-75C+
1010K	7C510-75C+
1010S	7C510-75M+
1010T	7C510-75M+
7C901-27M	7C910-32M
7C901-32M	2901CM

DENSEPAK	CYPRESS
PREFIX:DPS	PREFIX:CYM
1027-25C	1621HD-25C
1027-25C	161HD-25C
1027-35C	1621HD-30C
1027-35C	1621HD-35C
1027-45C	1621HD-45C
1027-55C	1621HD-55C
16X17-25C	1611HV-25C
16X17-25C	1611HV-25C
16X17-35C	1611HV-35C
16X17-35C	1611HV-35C
16X17-45C	1611HV-45C

DENSEPAK	CYPRESS
16X17-45C	1611HV-45C
16X17-55C	1611HV-55C
41288-100C	1421HD-85C
41288-100C	1421HD-100C
41288-70C	1421HD-70C
41288-85C	1421HD-85C
41288-85C	1421HD-85C
6432-45C	1830HD-45C
6432-55C	1830HD-55C
6432-55C	1830HD-55C
8M624-100C	1623HD-85C
8M624-85C	1623HD-100C
8M656-35C	1610HD-35C
8M656-70C	1610HD-70C

EDI	CYPRESS
PREFIX:ED	PREFIX:CYM
816H16C-25	1611HV-25C
816H16C-35	1611HV-35C
816H16C-45	1611HV-45C
8M8128C-100	1421HD-85C
8M8128C-70	1421HD-70C
H816H16C-25CC-	1611HV-25C
H816H16C-35CC-	1611HV-35C
H816H16C-45CC-	1611HV-45C
H816H16C-55CC-	1611HV-45C
H816H64C-35CC	1621HD-35C
H816H64C-35MHR	1621HD-35MB
H816H64C-45CC	1621HD-45C
H816H64C-45MHR	1621HD-45MB
H816H64C-55CC	1621HD-45C
H816H64C-55MHR	1621HD-45MB
H816H64C-70CC	1621HD-45C
H816H64C-70MHR	1621HD-45MB
I8M1664C-100CC	1623HD-100C
I8M1664C-60CC	1623HD-55C
I8M1664C-70CC	1623HD-70C
I8M1664C-85CC	1623HD-85C
I8M8128C-100CB	1420HD-55MB
I8M8128C-100CC	1421HD-85C
I8M8128C-60CB	1420HD-55MB
I8M8128C-60CC	1420HD-55C
I8M8128C-70CB	1421HD-55MB
I8M8128C-70CC	1421HD-70C
I8M8128C-80CC	1421HD-70C
I8M8128C-90CB	1421HD-55MB
I8M8128C-90CC	1421HD-85C

FAIRCHILD	CYPRESS
PREFIX:F	PREFIX:CY
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
SUFFIX:QB	SUFFIX:B
100E422-5	100E422-5C
100E422-7	100E422-7C
10E422-7	10E422-7C
100E474-7	100E474-7C
10E474-7	10E474-7C
1600C45	7C187-45C
1600C55	7C187-45C
1600C70	7C187-45C
1600M55	7C187-45M
1600M70	7C187-45M
1601C55	7C187-45C
1620C35	7C164-35C+
1620M35	7C164-35M
1620M45	7C164-45M
1621C25	7C164-25C+
1622C25	7C166-25C+
1622C35	7C166-35C+
1622M35	7C166-35M
1622M45	7C166-45M
16L8A	PALC16L8-20M
16L8A	PALC16L8-25C
16P8A	PALC16L8-20M
16P8A	PALC16L8-25C-
16R4A	PALC16R4-20M
16R4A	PALC16R4-25C
16R6A	PALC16R6-20M
16R6A	PALC16R6-25C
16R8A	PALC16R8-20M
16R8A	PALC16R8-25C
16RP4A	PALC16R4-20M
16RP4A	PALC16R4-25C
16RP6A	PALC16R6-20M
16RP6A	PALC16R6-25C
16RP8A	PALC16R8-20M
16RP8A	PALC16R8-25C
3341AC	3341C
3341C	3341C
54F189	7C189-25M-
54F219	7C190-25M-
54F413	7C401-15M
54S189M	54S189M
74AC1010-40	7C510-45C
74F189	7C189-25C-
74F219	7C190-25C-
74F413	7C401-15C
74LS189	27LS03C
74S189	74S189C
93422AC	93422AC
93422AM	93422AM
93422C	93422C
93422M	93422M
93475C	2149-45C
93L422AC	93L422AC
93L422AM	93L422AM
93L422C	93L422C
93L422M	93L422M
93Z451AC	7C282-30C
93Z451AM	7C282-45M
93Z451C	7C282-30C
93Z451M	7C282-45M
93Z511C	7C292-35C
93Z511M	7C292-50M
93Z565AC	7C264-45C
93Z565AM	7C264-55M
93Z565C	7C264-55C
93Z565M	7C264-55M
93Z611C	7C292-25C
93Z611M	7C291A-30M
93Z665C	7C264-35C
93Z665M	7C264-45M
93Z667C	7C263-35C
93Z667M	7C261-45M

FUJITSU	CYPRESS
PREFIX:MB	PREFIX:CY
PREFIX:MBM	PREFIX:CY
SUFFIX:F	SUFFIX:F
SUFFIX:M	SUFFIX:P
SUFFIX:Z	SUFFIX:D
100422A-5C	100E422-5C
100422A-7C	100E422-7C
100422AC	100E422-7C
100474A-3C	100E474-3C
100474A-5C	100E474-5C
100474A-7C	100E474-7C
100474AC	100E474-7C
10422A-5C	10E422-5C
10422A-7C	10E422-7C
10422AC	10E422-7C
10474A-3C	10E474-3C
10474A-5C	10E474-5C
10474A-7C	10E474-7C
10474AC	10E474-7C
2147H-35	2147-35C
2147H-45	2147-45C
2147H-55	2147-55C
2147H-70	2147-55C
2148-55L	21L48-55C
2148-70L	21L48-55C
2149-45	2149-45C
2149-55L	21L49-55C
2149-70L	21L49-55C
7132E	7C282-45C
7132E-SK	7C281-45C
7132E-W	7C282-45M
7132H	7C282-45C
7132H-SK	7C281-45C
7132Y	7C282-30C
7132Y-SK	7C281-30C
7138E	7C292-50C
7138E-SK	7C291-50C
7138E-W	7C292-50M
7138H	7C292-35C
7138H-SK	7C291-35C
7138Y	7C292-35C
7138Y-SK	7C291-35C
7144E	7C264-55C
7144E-W	7C264-55M
7144H	7C264-55C
7144Y	7C264-45C
7226RA-20	7C225-30C
7226RA-25	7C225-30C
7232RA-20	7C235-30C
7232RA-25	7C235-30C
7238RA-20	7C245-25C
7238RA-25	7C245-35C
8128-10	7C128-55C
8128-15	7C128-55C
8167-70W	7C167-45M
8167A-55	7C167-45C
8167A-70	7C167-45C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
– = functionally equivalent.
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

FUJTISU	CYPRESS
8168-55	7C168-45C
8168-70	7C168-45C
8168-70W	7C168-45M
8171-55	7C187-45
8171-70	7C187-45C
81C67-35	7C167-35C
81C67-45	7C167-45C
81C67-55W	7C167-45M
81C68-45	7C168-45C
81C68-55W	7C168-45M+
81C71-45	7C187-45C
81C71-55	7C187-45C
81C74-25	7C164-25C
81C74-35	7C164-35C+
81C74-45	7C164-45C
81C75-25	7C166-25C
81C75-35	7C166-35C
81C78-45	7C186-45C
81C78-55	7C186-55C
81C81-45	7C197-45C
81C81-55	7C197-45C
81C84-45	7C194-45C
81C84-55	7C194-45C
81C86-55	7C192-45C+
81C86-70	7C192-45C+
8464L-100	7C185-55C+
8464L-70	7C185-45C+

HARRIS	CYPRESS
PREFIX:HM	PREFIX:CY
PREFIX:HPL	PREFIX:CY
SUFFIX:8	SUFFIX:B
PREFIX:1	SUFFIX:D
PREFIX:9	SIFFOX"F
PREFIX:4	SUFFIX:L
PREFIX:3	SUFFIX:P
16LC8-5	PALC16L8L-35C
16LC8-8	PALC16L8-40M
16LC8-9	PALC16L8-40M
16RC4-5	PALC16R4L-35C
16RC4-8	PALC16R4-40M
16RC4-9	PALC16R4-40M
16RC6-5	PALC16R6L-35C
16RC6-8	PALC16R6-40M
16RC6-9	PALC16R6-40M
16RC8-5	PALC16R8L-35C
16RC8-8	PALC16R8-40M
16RC8-9	PALC16R8-40M
6-76161-2	7C291-50M
6-76161-5	7C291-50C
6-76161A-2	7C291-50M
6-76161A-5	7C291-50C
6-76161B-5	7C291-35C
6-7681-5	7C281-45C
6-7681A-5	7C281-45C
65162-5	6116-55C*
65162-8	6116-55M*
65162-9	6116-55M*
65162B-5	6116-55C*
65162B-8	6116-55M*
65162B-9	6116-55M*
65162C-8	6116-55M*

HARRIS	CYPRESS
65162C-9	6116-55M*
65162S-5	6116-55C*
65162S-9	6116-55M*
65262-8	7C167-45M*
65262-9	7C167-45M*
65262B-8	7C167-45M*
65252B-9	7C167-45M*
65262C-9	7C167-45M*
65262S-9	7C167-45M*
76161-2	7C292-50M
76161A-2	7C292-50M
76161A-5	7C292-50C
76161B-5	7C292-35C
76641-2	7C264-55M
76641-5	7C264-55C
76641A-5	7C264-45C
7681-2	7C282-45M
7681-5	7C282-45C
7681A-5	7C282-45C

HITACHI	CYPRESS
PREFIX:HM	PREFIX:CY
PREFIX:HN	PREFIX:CY
SUFFIX:CG	SUFFIX:L
SUFFIX:G	SUFFIX:D
SUFFIX:P	SUFFIX:P
100422C	100E422-7C
100474-10C	100E474-7C
10047-8C	100E474-7C
100474C	100E474-7C
10422C	10E422-7C
10474-10C	100E474-7C
10474-8C	10E474-7C
10474C	100E474-7C
25089	7C282-45C
25089S	7C282-45C
25169S	7C292-50C
4847	2147-55C
4847-2	2147-45C
4847-3	2147-55C
6116ALS-12	6116-55C*
6116ALS-15	6116-55C*
6116ALS-20	6116-55C*
6116AS-12	6116-55C+
6116AS-15	6116-55C+
6116AS-20	6116-55C+
6147	7C147-45C*
6147-3	7C147-45C*
6147H-35	7C147-35C+
6147H-45	7C147-45C+
6147H-55	7C147-45C+
6147HL-35	7C147-35C*
6147HL-45	7C147-45C*
6147HL-55	7C147-55C*
6148	7C148-45C
6148H-35	21L48-35C
6148H-45	7C148-45C+
6148H-55	7C14845C+
6148HL-35	21L48-35C*
6148HL-45	7C148-45C*
6148HL-55	7C148-45C*
6148L	7C148-45C*

HITACHI	CYPRESS
6167-6	7C167-45C+
6167-8	7C167-45C+
6167H-55	7C167-45C
6167H-70	7C167-45C
6167HL-55	7C167-45C*
6167HL-70	7C167-45C*
6167L-6	7C167-45C*
6167L-8	7C167-45C*
6168H-45	7C168-45C+
6168H-55	7C168-45C+
6168H-70	7C168-45C+
6168HL-45	7C168-45C*
6168HL-55	7C168-45C*
6168HL-70	7C168-45C*
6264-10	7C186-55C+
6264-12	7C186-55C+
6264-15	7C186-55C+
6267-35	7C167-35C+
6267-45	7C167-45C
6268-25	7C168-25C
6268-35	7C168-35C
6287-45	7C187-45C
6287-55	7C187-45C
6287-70	7C187-45C
6288-35	7C164-35C
6288-45	7C164-45C
6288-55	7C164-45C
6716	7C128-25C
6787-30	7C187-25C
6788-25	7C164-25C
6788-30	7C164-25C

INMOS	CYPRESS
PREFIX:IMS	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:P	SUFFIX:P
SUFFIX:S	SUFFIX:D
SUFFIX:W	SUFFIX:L
1203-25	7C147-25C+
1203-35	7C147-35C+
1203-45	7C147-45C+
1203M-35	7C147-35M+
1203M-45	7C147-45M+
1223-25	7C148-25C
1223-35	7C148-35C
1223-45	7C148-45C
1223M-35	7C148-25M+
1223M-45	7C148-45M+
1400-35	7C167-35C
1400-45	7C167-45C
1400-55	7C167-45C
1400M-45	7C167-45M
1400M-55	7C167-45M
1400M-70	7C167-45M
1403-25	7C167-25C
1403-35	7C167-35C+
1403-45	7C167-45C+
1403-55	7C167-45C+
1403LM-35	7C167-35M*
1403M-35	7C167-35M+
1403M-45	7C167-45M+
1403M-55	7C167-45M+

INMOS	CYPRESS
1403M-70	7C167-45M+
1420-45	7C168-35C
1420-55	7C168-45C
1420M-55	7C168-45M+
1420M-70	7C168-45M
1421C-40	7C169-40C
1423-25	7C168-25C+
1423-35	7C168-35C+
1423-40	7C168-45C+
1423M-35	7C168-35M*
1423M-45	7C168-45M*
1423M-55	7C168-45M*
1433-30	7C128-25C+
1433-35	7C128-35C+
1433-45	7C128-45C+
1433-55	7C128-55C+
1433M-35	7C128-35M+
1433M-45	7C128-45M+
1433M-55	7C128-55M+
1600-35	7C187-35C
1600-45	7C187-45C
1600-55	7C187-45C
1600-70	7C187-45C
1600M-45	7C187-45M+
1600M-55	7C187-45M+
1600M-70	7C187-45M+
1601LM-45	7C187-45M+
1601LM-55	7C187-45M+
1601LM-70	7C187-45M+
1620-35	7C164-35C
1620-45	7C164-45C+
1620-55	7C164-45C+
1620-70	7C164-45C+
1620M-45	7C164-45M
1620M-55	7C164-45M
1620M-70	7C164-45M
1624-35	7C166-35C+
1624-45	7C166-45C+
1624-55	7C166-45C+
1624-70	7C166-45C+
1624M-45	7C166-45M
1624M-55	7C166-45M
1624M-70	7C166-45M
1625-25	7C164-25C
1625-35	7C164-35C
1625M-35	7C164-45M
1625M-45	7C164-45M
1630-45	7C186-45C+
1630-55	7C186-55C+
1630-70	7C186-55C+
1630LM-70	7C186-55M
1630M-45	7C186-45M
1630M-55	7C186-55M+
1630M-70	7C186-55M
1800-30	7C197-25C
1800-35	7C197-35C
1800-45	7C197-45C
1800M-35	7C197-35M
1800M-45	7C197-45M
1820-25	7C194-25C
1820-35	7C194-35C
1820-45	7C194-45C

IDT	CYPRESS
PREFIX:IDT	PREFIX:CY
PREFIX:IDT	PREFIX:CYM
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
39C01CB	7C901-32M+
39C01CC	2901CC+
39C01CM	2901CM+
39C01DB	7C901-27M+
39C01DC	7C901-23C+
39C09A	7C909-40C+
39C09AB	7C909-40M
39C10B	7C910-50C-
39C10BB	7C910-51M
39C11A	7C911-40C+
39C11AB	7C911-40M+
49C401	7C9101-40C-
49C401	7C9101-45M-
6116LA120L32	6117-55M
6116LA150L32	6117-55M
6116LA35L32	6117-35M
6116LA45L32	6117-45M
6116LA55L32	6117-55M
6116LA70L32	6117-55M
6116LA90L32	6117-55M
6116SA120L32	6117-55M
6116SA150L32	6117-55M
6116SA35L32	6117-35M
6116SA45L32	6117-45M
6116SA55L32	6117-55M
6116SA70L32	6117-55M
6116SA90L32	6117-55M
6116L120B	6116-55M*
6116L150B	6116-55M*
6116L55	6116-55C*
6116L55B	6116-55M*
6116L70	6116-55C*
6116L70B	6116-55M*
6116L90	6116-55C*
6116L90B	6116-55M*
6116LA120B	6116-55M*
6116LA120TB	7C128-55M*
6116LA35	6116-35C*
6116LA35B	6116-45M*
6116LA35T	7C128-35C*
6116LA35TB	7C128-35M*
6116LA45	6116-45C*
6116LA45B	6116-45M*
6116LA45T	7C128-45C*
6116LA45TB	7C128-45M*
6116LA55	6116-55C*
6116LA55B	6116-55M*
6116LA55T	7C128-55C*
6116LA55TB	7C128-55M*
6116LA70	6116-55C*
6116LA70B	6116-55M*
6116LA70T	7C128-55C*
6116LA70TB	7C128-55M*
6116LA90	6116-55C*
6116LA90B	6116-55M*

IDT	CYPRESS
6116LA90T	7C128-55C*
6116LA90TB	7C128-55M*
6116S120B	6116-55M+
6116S150B	6116-55M+
6116S55	6116-55C+
6116S55B	6116-55M+
6116S70	6116-55C+
6116S70B	6116-55M+
6116S90	6116-55C+
6116S90B	6116-55M+
6116SA120B	6116-55M+
6116SA120TB	7C128-55M+
6116SA35	6116-35C+
6116SA35B	6116-45M+
6116SA35T	7C128-35C+
6116SA35TB	7C128-35M+
6116SA45	6116-45C+
6116SA45B	6116-45M+
6116SA45T	7C128-45C+
6116SA45TB	7C128-45M+
6116SA55	6116-55C+
6116SA55B	6116-55M+
6116SA55T	7C128-55C+
6116SA55TB	7C128-55M+
6116SA70	6116-55C+
6116SA70B	6116-55M+
6116SA70T	7C128-55C+
6116SA70TB	7C128-55M+
6116SA90	6116-55C+
6116SA90B	6116-55M+
6116SA90T	7C128-55C+
6116SA90TB	7C128-55M+
6167L100B	7C167-45M*
6167L55B	7C167-45M*
6167L70B	7C167-45M*
6167L85B	7C167-45M*
6167LA25	7C167-25C*
6167LA35	7C167-35C*
6167LA35B	7C167-35M*
6167LA45	7C167-45C*
6167LA45B	7C167-45M*
6167LA55	7C167-45C*
6167LA55B	7C167-45M*
6167LA70B	7C167-45M*
6167S100B	7C167-45M
6167S45	7C167-45C
6167S55	7C167-45C
6167S55B	7C167-45M
6167S70B	7C167-45M
6167S85B	7C167-45M
6167SA25	7C167-25C+
6167SA35	7C167-35C+
6167SA35B	7C167-35M+
6167SA45	7C167-45C+
6167SA45B	7C167-45M+
6167SA55	7C167-45C+
6167SA55B	7C167-45M+
6167SA70B	7C167-45M+
6168LA100B	7C168-45M*
6168LA85B	7C168-45M*
6168LA25	7C168-25C*
6168LA25B	7C169-25M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
– = functionally equivalent.
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

Product Line Cross Reference

IDT	CYPRESS
6168LA35	7C168-35C*
6168LA35B	7C168-35M*
6168LA45B	7C168-45M*
6168LA55B	7C168-45M*
6168LA70B	7C168-45M*
6168SA100B	7C168-45M+
6168SA70B	7C168-45M
6168SA85B	7C168-45M
6168SA25	7C168-25C+
6168SA25B	7C169-25M
6168SA35	7C168-35C+
6168SA35B	7C168-35M+
6168SA45B	7C168-45M+
6168SA55B	7C168-45M+
6168SA70B	7C168-45M+
61970S25	7C170-25C
61970S35	7C170-35C
61970S35B	7C170-35M
61970S45	7C170-45C
61970S45B	7C170-45M
6198S25	7C196-25C
6198S35	7C196-35C
6198S35B	7C196-35M
6198S45	7C196-45C
6198S45B	7C196-45M
71256S25	7C198-25C
71256S25	7C199-25C*
71256S35	7C198-35C
71256S35	7C199-35C*
71256S35B	7C198-35M
71256S35B	7C199-35M‡
71256S45	7C198-45C
71256S45	7C199-45C†
71256S45B	7C198-45M
71256S45B	7C199-45M‡
71256S55	7C198-55C
71256S55	7C199-55C†
71256S55B	7C198-55M
71256S55B	7C199-55M‡
71257S25	7C197-25C
71257S35	7C197-35C
71257S35B	7C197-35M
71257S45	7C197-45C
71257S45B	7C197-45M
7130L100	7C130-55C*
7130L100B	7C130-55M
7130L120B	7C130-55M
7130L55	7C1309-55C*
7130L70	7C130-55C*
7130L90	7C130-55C*
7130S100	7C130-55C
7130S100B	7C130-55M
7130S120B	7C130-55M
7130S25	7C130-25C
7130S35	7C130-35C
7130S45	7C130-45C
7130S55	7C130-55C
7130S70	7C130-55C
7130S90	7C130-55C
7132L100	7C132-55C*
7132L100B	7C132-55M*
7132L120B	7C132-55M*

IDT	CYPRESS
7132L55	7C132-55C*
7132L70	7C132-55C*
7132L70B	7C132-55M*
7132L90	7C132-55C*
7132L90B	7C132-55M*
7132S100	7C132-55C+
7132S100B	7C132-55M+
7132S120B	7C132-55M+
7132S55	7C132-55C+
7132S70	7C132-55C+
7132S70B	7C132-55M+
7132S90	7C132-55C+
7132S90B	7C132-55M+
71321S25	7C132-25C
71321S35	7C132-35C
71321S45	7C132-45C
7140S25	7C140-25C
7140S35	7C140-35C
7140S45	7C140-45C
7140S55	7C140-55C
7140S70	7C140-55C
7140S90	7C140-55C
71421S25	7C142-25C
71421S35	7C142-35C
71421S45	7C142-45C
71421S55	7C142-55C
71421S70	7C142-55C
71421S90	7C142-55C
7164S35T	7C185-35C
7164S45T	7C185-45C
7164S45TB	7C185-45M
7164S55T	7C185-45M
7164S55TB	7C185-55M
7164S70T	7C185-55C
7164S70TB	7C185-55M
7164S85TB	7C185-55M
7164S35	7C186-35C
7164S45	7C186-45C
7164S45B	7C186-45M
7164S55	7C186-55C
7164S55B	7C186-55M
7164S70	7C186-55C
7164S70B	7C186-55M
7164S85B	7C186-55M
71681L100B	7C171-45M*
71681L45	7C171-45C*
71681L55	7C171-45C*
71681L55B	7C171-45M*
71681L70	7C171-45C*
71681L70B	7C171-45M*
71681L85B	7C171-45M*
71681LA25	7C171-25C*
71681LA35	7C171-35C*
71681LA35B	7C171-35M*
71681LA45	7C171-45C*
71681LA45B	7C171-45M*
71681LA55	7C171-45C*
71681LA55B	7C171-45M*
71681LA70B	7C171-45M*
71681S100B	7C171-45M+
71681S45	7C171-45C+
71681S55	7C171-45C+

IDT	CYPRESS
71681S55B	7C171-45M+
71681S70	7C171-45C+
71681S70B	7C171-45M+
71681S85B	7C171-45M+
71681SA25	7C171-25C+
71681SA35	7C171-35C+
71681SA35B	7C171-35M+
71681SA45	7C171-45C+
71681SA45B	7C171-45M+
71681A55	7C171-45C+
71681SA55B	7C171-45M+
71681SA70B	7C171-45M+
71682L100B	7C172-45M*
71682L45	7C172-45C*
71682L55	7C172-45C*
71682L55B	7C172-45M*
71682L70	7C172-45C*
71682L70B	7C172-45M*
71682L85B	7C172-45M*
71682LA25	7C172-25C*
71682LA35	7C172-35C*
71682LA35B	7C172-35M*
71682LA45	7C172-45C*
71682LA45B	7C172-45M*
71682LA55	7C172-45C*
71682LA55B	7C172-45M*
71682S100B	7C172-45M+
71682S45	7C172-45C+
71682S55	7C172-45C+
71682S55B	7C172-45M+
71682S70	7C172-45C+
71682S70B	7C172-45M+
71682S85B	7C172-45M+
71682SA25	7C172-25C+
71682SA35	7C172-35C+
71682SA35B	7C172-35M+
71682SA45	7C172-45C+
71682SA45B	7C172-45M+
71682SA55	7C172-45C+
71682SA55B	7C172-45M+
7187S30	7C187-25C
7187S35	7C187-35C
7187S35B	7C187-35M
7187S45	7C187-45C
7187S45B	7C187-45M
7187S55	7C187-45C
7187S55B	7C187-45M
7187S70	7C187-45C
7187S70B	7C187-45M
7187S85	7C187-45C
7187S85B	7C187-45M
7188S25	7C194-25C
7188S30	7C164-25C
7188S35	7C164-35C
7188S35	7C194-35C
7188S35B	7C194-35M
7188S45	7C164-45C
7188S45	7C194-45C
7188S45B	7C164-45M
7188S45B	7C194-45M
7188S55	7C164-45C
7188S55B	7C164-45M

Product Line Cross Reference

IDT	CYPRESS
7188S70	7C164-45C
7188S70B	7C164-45M
7188S85B	7C164-45M
71981S25	7C191-25C
71981S35	7C161-35C
71981S35	7C191-35C
71981S35B	7C161-35M
71981S35B	7C191-35M
71981S45	7C161-45C
71981S45	7C191-45C
71981S45B	7C161-45M
71981S45B	7C191-45M
71981S55	7C161-45C
71981S55B	7C161-45M
71981S70	7C161-45C
71981S70B	7C161-45M
71981S85B	7C161-45M
71982S25	7C192-25C
71982S35	7C162-35C
71982S35	7C192-35C
71982S35B	7C162-35M
71982S35B	7C192-35M
71982S45	7C162-45C
71982S45	7C192-45C
71982S45B	7C162-45M
71982S45B	7C192-45M
71982S55	7C162-45C
71982S55B	7C162-45M
71982S70	7C162-45C
71982S70B	7C162-45M
71982S85B	7C162-45M
7198S35	7C166-35C
7198S35B	7C166-35M
7198S45	7C166-45C
7198S45B	7C166-45M
7198S55	7C166-45C
7198S55B	7C166-45M
7198S70	7C166-45C
7198S70B	7C166-45M
7198S85B	7C166-45M
7201LA120	7C420-65C+
7201LA120B	7C420-65M+
7201LA35	7C420-30C+
7201LA40B	7C420-40M+
7201LA50	7C420-40C+
7201LA50B	7C420-40M+
7201LA65	7C420-65C+
7201LA65B	7C420-65M+
7201LA80	7C420-65C+
7201LA80B	7C420-65M+
7201SA120	7C420-65C
7201SA120B	7C420-65M
7201SA35	7C420-30C
7201SA40B	7C420-40M
7201SA50	7C420-40C
7201SA50B	7C420-40M
7201SA65	7C420-65C
7201SA65B	7C420-65M
7201SA80	7C420-65C
7201SA80B	7C420-65M
7201LA25T	7C421-25C
7201LA30TB	7C421-30M

IDT	CYPRESS
7201LA35T	7C421-30C
7201LA40TB	7C421-40M
7201LA50TB	7C421-40M
7201LA65T	7C421-65C
7201LA50T	7C421-40C
7201LA65TB	7C421-65M
7201SA25T	7C421-25C
7201SA30TB	7C421-30M
7201SA35T	7C421-30C
7201SA40TB	7C421-40M
7201SA50T	7C421-40C
7201SA50TB	7C421-40M
7201SA65T	7C421-65C
7201SA65TB	7C421-65M
7202LA120	7C424-65C+
7202LA120B	7C424-65M+
7202LA25	7C424-25C
7202LA35	7C424-30C+
7202LA40B	7C424-40M+
7202LA50	7C424-40C+
7202LA50B	7C424-40M+
7202LA65	7C424-65C+
7202LA65B	7C424-65M+
7202LA80	7C424-65C+
7202LA80B	7C424-65M+
7202SA120	7C424-65C
7202SA120B	7C424-65M
7202SA25	7C424-25C
7202SA35	7C424-30C
7202SA40B	7C424-40M
7202SA50	7C424-40C
7202SA50B	7C424-40M
7202SA65	7C424-65C
7202SA65B	7C424-65M
7202SA80	7C424-65C
7202SA80B	7C424-65M
7202LA25T	7C425-25C
7202LA30TB	7C425-30M
7202LA35T	7C425-30C
7202LA40TB	7C425-40M
7202LA50T	7C425-40C
7202LA50TB	7C425-40M
7202LA65T	7C425-65C
7202LA65TB	7C425-65M
7202SA25T	7C425-25C
7202SA30TB	7C425-30M
7202SA35T	7C425-30C
7202SA40TB	7C425-40M
7202SA50T	7C425-40C
7202SA50TB	7C425-40M
7202SA65T	7C425-65C
7202SA65TB	7C425-65M
7203L50	7C428-40C
7203L50B	7C428-40M
7203L50T	7C429-40C
7203L65	7C428-65C
7203L65B	7C428-65M
7203L65T	7C429-65C
7203S50	7C428-40C
7203S50B	7C428-40M
7203S50T	7C429-40C
7203S65	7C428-65C

IDT	CYPRESS
7203S65B	7C428-65M
7203S65T	7C429-65C
72045S35D	7C432-30D+
72045S35D	7C432-40D+
72045S35J	7C433-30LC+
72045S35P	7C433-30P+
72045S35P	7C433-65P+
72045S40J	7C433-40LMB
72045S50D	7C432-65D+
72045S50J	7C433-40LC+
72045S50P	7C433-40P+
72045S65J	7C433-65LC+
7210-120B	7C510-75M
7210-200B	7C510-75M+
7210-55B	7C510-55M
7210-65B	7C510-65M
7210-75B	7C510-75M
7210-85B	7C510-75M
7210L-45	7C510-45C+
7210L100	7C510-75C+
7210L165	7C510-75C+
7210L55	7C510-55C+
7210L65	7C510-65C+
7210L75	7C510-75C+
7216L120B	7C516-75M+
7216L140	7C516-75C+
7216L185B	7C516-75M+
7216L55	7C516-55C+
7216L55B	7C516-55M+
7216L65	7C516-65C+
7216L65B	7C516-65M
7216L75	7C516-75C+
7216L75B	7C516-75M
7216L90	7C516-75C+
7216L90B	7C516-75M+
7217L120B	7C517-75M+
7217L140	7C517-75C+
7217L185B	7C517-75M+
7217L45	7C517-45C+
7217L55	7C517-55C+
7217L55B	7C517-55M
7217L65	7C517-65C+
7217L65B	7C517-65M
7217L75	7C517-75C+
7217L75B	7C517-75M
7217L90	7C517-75C+
7217L90B	7C517-75M+
7M4016S25C	1641HD-25C
7M4016S35C	1641HD-35C
7M4016S35CB	1641HD-35MB
7M4016S45C	1641HD-45C
7M4016S45CB	1641HD-45MB
7M4016S55C	1641HD-55C
7M4016S55CB	1641HD-55MB
7M4016S70CB	1641HD-55MB
7M4017S40C	1830HD-35C
7N4017S45C	1830HD-45C
7M4017S50C	1830HD-45C
7M4017S50CB	1830HD-45MB
7M4017S55C	1830HD-55C
7M4017S60C	1830HD-55C
7M4017S60CB	1830HD-55MB

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
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– = functionally equivalent.
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

IDT	CYPRESS
7M4017S70C	1830HD-55C
7M4017S70CB	1830HD-55MB
7M624S30C	1621HD-30C
7M624S35C	1621HD-35C
7M624S35CB	1621HD-35MB
7M624S45C	1621HD-45C
7M624S45CB	1621HD-45MB
7M624S55C	1621HD-45C
7M624S55CB	1621HD-45MB
7M624S65C	1621HD-45C
7M624S65CB	1621HD-45MB
7MC4005S20CV	1611HV-20C
7MC4005S25CV	1611HV-25C
7MC4005S25CVB	1611HV-25MB
7MC4005S30CV	1611HV-30C
7MC4005S30CVB	1611HV-30MB
7MC4005S35CV	1611HV-35C
7MC4005S35CVB	1611HV-35MB
7MC4005S45CV	1611HV-45C
7MC4005S45CVB	1611HV-45MB
7MC4005S55CV	1611HV-45C
7MC4005S55CVB	1611HV-45MB
7MC4032S20CV	1822HV-20C
7MC4032S25CV	1822HV-25C
7MC4032S25CVB	1822HV-25MB
7MC4032S30CV	1822HV-30C
7MC4032S30CVB	1822HV-30MB
7MC4032S40CV	1822HV-35C
7MC4032S40CVB	1822HV-35MB
7MC4032S50CV	1822HV-45C
7MC4032S50CVB	1822HV-45MB
7MC4032S70CVB	1822HV-45MB
7MP4008L100S	1461PS-100C
7MP4008L70S	1461PS-70C
7MP4008L85S	1461PS-85C
7MP4008S35S	1460PS-35C
7MP4008S45S	1460PS-45C
7MP4008S55S	1460PS-55C
7MP4008S70S	1460PS-70C
8M624S100CB	1620HD-55MB
8M624S35C	1620HD-35C
8M624S40C	1620HD-35C
8M624S45C	1620HD-45C
8M624S50C	1620HD-45C
8M624S50CB	1620HD-45MB
8M624S60C	1620HD-55C
8M624S60CB	1620HD-55MB
8M624S70C	1620HD-55C
8N624S70CB	1620HD-55MB
8N624S85CB	1620HD-55MB
8M656S40C	1610HD-35C
8M656S50C	1610HD-45C
8M656S50CB	1610HD-45MB
8M656S60C	1610HD-45C
8M656S60CB	1610HD-45MB
8M656S70C	1610HD-45C
8M656S70CB	1610HD-45MB
8M656S85C	1610HD-45C
8M656S85CB	1610HD-45MB
8M824L100C	1421HD-85C
8M824L100N	1421HD-85C
8M824L85C	1421HD-85C

IDT	CYPRESS
8M824L85N	1421HD-85C
8M824S100CB	1420HD-55MB
8M824S100N	1421HD-85C
8M824S35C	1420HD-35C
8M824S40C	1420HD-35C
8M824S45C	1420HD-45C
8M824S45CB	1420HD-45MB
8M824S45N	1423PD-45C
8M824S50C	1420HD-45C
8M824S50CB	1420HD-45MB
8M824S50N	1423PD-45C
8M824S60C	1420HD-55C
8M824S60CB	1420HD-55MB
8M824S60N	1423PD-55C
8M824S70C	1421HD-70C
8M824S70CB	1420HD-55MB
8M824S70N	1423PD-70C
8M824S85CB	1420HD-55MB
8M824S85N	1421HD-85C
8MP624S40S	1626PS-35C
8MP624S45S	1626PS-45C
8MP624S50S	1626PS-45C
8MP624S60S	1626PS-45C
8MP824S40S	1422PS-35C
8MP824S45S	1422PS-45C
8MP824S50S	1422PS-45C
8MP824S60S	1422PS-55C
8MP824S70S	1422PS-55C

INTEL	CYPRESS
PREFIX:D	SUFFIX:D
PREFIX:L	SUFFIX:L
PREFIX:P	SUFFIX:P
SUFFIX:/B	SUFFIX:B
2147H	2147-55C
2147H-1	2147-35C
2147H-2	2147-45C
2147H-3	2147-55C
2147HL	7C147-45C
2148H	2148-55C
2148H-2	2148-45C
2148H-3	2148-55C
2148HL	21L48-55C
2148HL-3	21L48-55C
2149H	2149-55C
2149H-1	2149-35C
2149H-2	2149-45C
2149H-3	2149-55C
2149HL	21L49-55C
51C66-25	7C167-25C-
51C66-30	7C167-25C-
51C66-35	7C167-25C-
51C66-35L	7C167-25C-
51C67-30	7C167-25C+
51C67-35	7C167-35C+
51C67-35L	7C167-35C+
51C68-30	7C168-25C+
51C68-35	7C168-35C+
M2147H-3	7C169-40M
M2148H	2148-55M
M2149H	2149-55M
M2149H-2	2149-45M

INTEL	CYPRESS
M2149H-3	2149-55M

LATTICE	CYPRESS
PREFIX:EE	PREFIX:CY
PREFIX:GAL	PREFIX:CY
PREFIX:ST	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:L	SUFFIX:L
SUFFIX:P	SUFFIX:P
16K4-25	7C168-25C
16K4-35	7C168-35C
16K4-35M	7C168-35M
16K4-45	7C168-45C
16K4-45M	7C168-45M
16K8-35	7C128-35C+
16K8-55	7C128-45C+
16V8-25	PALC16L8-25C
16V8-25	PALC16R4-25C
16V8-25	PALC16R6-25C
16V8-25	PALC16R8-25C
16V8-25L	PALC16L8-25C
16V8-25L	PALC16R4-25C
16V8-25L	PALC16R6-25C
16V8-25L	PALC16R8-25C
16V8-25Q	PALC16L8L-25C
16V8-25Q	PALC16R4L-25
16V8-25Q	PALC16R6L-25
16V8-25Q	PALC16R8L-25
16V8-30	PALC16L8-30M
16V8-30	PALC16R4-30M
16V8-30	PALC16R6-30M
16V8-30	PALC16R8-30M
16V8-30L	PALC16L8-30M
16V8-30L	PALC16R4-30M
16V8-30L	PALC16R6-30M
16V8-30L	PALC16R8-30M
16V8-30Q	PALC16L8-30M
16V8-30Q	PALC16R4-30M
16V8-30Q	PALC16R6-30M
16V8-30Q	PALC16R8-30M
16V8-35	PALC16L8-35C
16V8-35	PALC16R4-35C
16V8-35	PALC16R6-35C
16V8-35	PALC16R8-35C
16V8-35L	PALC16L8-35C
16V8-35L	PALC16R4-35C
16V8-35L	PALC16R6-35C
16V8-35L	PALC16R8-35C
16V8-35Q	PALC16L8L-35C
16V8-35Q	PALC16R4L-35C
16V8-35Q	PALC16R6L-35C
16V8-35Q	PALC16R8L-35C
20V8-25	PLDC20G10-25C
20V8-25L	PLDC20G10-25C
20V8-25Q	PLDC20G10-25C
20V8-35	PLDC20G10-30M
20V8-35	PLDC20G10-35C
20V8-35L	PLDC20G10-30M
20V8-35L	PLDC20G10-35C
20V8-35Q	PLDC20G10-30M
20V8-35Q	PLDC20G10-35C

LATTICE	CYPRESS
64E4-35	7C166-35C
64E4-45	7C155-45C
64E4-55	7C166-45C
64K1-35	7C187-35C
64K1-45	7C187-45C
64K1-45M	7C187-45M
64K1-55	7C187-45C
64K1-55M	7C187-45M
64K4-35	7C164-35C
64K4-45	7C164-45C
64K4-45M	7C164-45M
64K4-55	7C164-45C
64K4-55M	7C164-45M
64K8-35	7C186-35C
64K8-45	7C186-45C
64K8-45	7C264-45C
64K8-45M	7C186-45M
64K8-55	7C186-55C
64K8-55	7C264-55C
64K8-55M	7C186-45M
64K8-70	7C264-55C
L1010-45	7C510-45C+
L1010-65	7C510-65C+
L1010-65B	7C510-65M+
L1010-90	7C510-75C+
L1010-90B	7C510-75M+

MICRON	CYPRESS
PREFIX:MT	PREIFX:CY
5C1601-20C	7C167A-20C
5C1601-25C	7C167A-25C
5C1601-25M	7C167A-25M
5C1601-35C	7C167A-35C
5C1601-35M	7C167A-35M
5C1601-45C	7C167A-45C
5C1601-45M	7C167A-45M
5C1604-20C	7C168A-20C
5C1604-25C	7C168A-25C
5C1604-25M	7C168A-25M
5C1604-35C	7C168A-35C
5C1604-35M	7C168A-35M
5C1604-45C	7C168A-45C
5C1604-45M	7C168A-45M
5C1605-20C	7C170A-20C
5C1605-25C	7C170A-25C
5C1605-25M	7C170A-25M
5C1605-35C	7C170A-35C
5C1605-35M	7C170A-35M
5C1605-45C	7C170A-45C
5C1605-45M	7C170A-45M
5C1606-20C	7C171A-20C
5C1606-25C	7C171A-25C
5C1606-25M	7C171A-25M
5C1606-35C	7C171A-35C
5C1606-35M	7C171A-35M
5C1606-45C	7C171A-45C
5C1606-45M	7C171A-45M
5C1607-20C	7C172A-20C
5C1607-25C	7C172A-25C
5C1607-25M	7C172A-25M
5C1607-35C	7C172A-35C
5C1607-35M	7C172A-35M

MICRON	CYPRESS
5C1607-45C	7C172A-45C
5C1607-45M	7C172A-45M
5C1608-20C	7C128A-20C
5C1608-25C	7C128A-25C
5C1608-25M	7C128A-25M
5C1608-35C	7C128A-35C
5C1608-35M	7C128A-35M
5C1608-45C	7C128A-45C
5C1608-45M	7C128A-45M
5C1608-55C	7C128A-55C
5C1608-55M	7C128A-55M
5C2561-25C	7C197-25C
5C2561-35C	7C197-35C
5C2561-35M	7C197-35M
5C2561-45C	7C197-45C
5C2561-45M	7C197-45M
5C6401-20C	7C187-20C
5C6401-25C	7C187-25C
5C6401-25M	7C187-25M
5C6401-35C	7C187-35C
5C6401-35M	7C187-35M
5C6401-45C	7C187-45C
5C6401-45M	7C187-45M
5C6404-20C	7C164-20C
5C6404-25C	7C164-25C
5C6404-25M	7C164-25M
5C6404-35C	7C164-35C
5C6404-35M	7C164-35M
5C6404-45C	7C164-45C
5C6404-45M	7C164-45M
5C6405-20C	7C166-20C
5C6405-25C	7C166-25C
5C6405-25M	7C166-25M
5C6405-35C	7C166-35C
5C6405-35M	7C166-35M
5C6405-45C	7C166-45C
5C6405-45M	7C166-45M
5C6406-20C	7C161-20C
5C6406-25C	7C161-25C
5C6406-25M	7C161-25M
5C6406-35C	7C161-35C
5C6406-35M	7C161-35M
5C6406-45C	7C161-45C
5C6406-45M	7C161-45M
5C6407-20C	7C162-20C
5C6407-25C	7C162-25C
5C6407-25M	7C162-25M
5C6407-35C	7C162-35C
5C6407-35M	7C162-35M
5C6407-45C	7C162-45C
5C6407-45M	7C162-45M
5C6408-20C	7C185-20C
5C6408-25C	7C185-25C
5C6408-25M	7C185-25M
5C6408-35C	7C185-35C
5C6408-35M	7C185-35M
5C6408-45C	7C185-45C
5C6408-45M	7C185-45M
5C6408-55C	7C185-55C
5C6408-55M	7C185-55M
5C6408W-20C	7C186-20C
5C6408W-25C	7C186-25C

MICRON	CYPRESS
5C6408W-25M	7C186-25M
5C6408W-35C	7C186-35C
5C6408W-35M	7C186-35M
5C6408W-45C	7C186-45C
5C6408W-45M	7C186-45M
5C6408W-55C	7C186-55C
5C6408W-55M	7C186-55M
85C1664-30C	1620HD-30C
85C1664-35C	1620HD-35C
85C1664-45C	1620HD-45C
85C8128-30C	1420HD-30C
85C8128-35C	1420HD-35C
85C8128-45C	1420HD-45C
85C8128-45C	1423PD-45C

MITSUBISHI	CYPRESS
PREFIX:M5M	PREFIX:CY
SUFFIX:AP	SUFFIX:L
SUFFIX:FP	SUFFIX:F
SUFFIX:K	SUFFIX:D
SUFFIX:P	SUFFIX:P
21C67P-35	7C167-35C
21C67P-45	7C167-45C
21C67P-55	7C167-45C
21C68P-35	7C168-35C
21C68P-45	7C168-45C
21C68P-55	7C168-45C
5165L-100	7C186-55C+
5165L-120	7C186-55C+
5165L-70	7C186-55C+
5165P-100	7C186-55C+
5165P-120	7C186-55C+
5165P-70	7C186-55C+
5178P-45	7C186-45C+
5178P-55	7C186-55C+
5187P-25	7C187-25C
5187P-35	7C187-35C
5187P-45	7C187-45C
5187P-55	7C187-45C
5188P-25	7C164-25C
5188P-35	7C164-35C
5188P-45	7C164-45C
5188P-55	7C164-45C

MMI/AMD	CYPRESS
SUFFIX:883B	SUFFIX:B
SUFFIX:F	SUFFIX:F
SUFFIX:J	SUFFIX:D
SUFFIX:L	SUFFIX:L
SUFFIX:N	SUFFIX:P
SUFFIX:SHRP	SUFFIX:B
5381-1	7C282-45M
5381-2	7C282-45M
5381S-1	7C281-45M
5381S-2	7C281-45M
53RA1681AS	7C245-35M-
53RA1681S	7C245-45M-
53RA481AS	7C225-35M
53RA481S	7C225-40M
53R1681AS	7C245-35M-
53RS1681S	7C245-45M-
53RS881AS	7C235-40M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
– = functionally equivalent.
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

MMI/AMD	CYPRESS
53RS881S	7C235-40M-
53S1681	7C292-50M
53S1681AS	7C291-35M
53S1681S	7C291-50M
53S881	7C282-45M
53S881A	7C282-45M
53S881AS	7C281-45M
53S881S	7C281-45M
57401	7C401-10M
57401A	7C401-10M
57402	7C402-10M
57402A	7C402-10M
6381-1	7C282-45C
6381-2	7C282-45C
6381S-1	7C281-45C
6381S-2	7C281-45C
63RA1681AS	7C245-35C-
63RA1681S	7C245-35C-
63RA481AS	7C225-25C
63RA481S	7C225-30C
63RS1681AS	7C245-35C-
63RS1681S	7C245-35C-
63RS881AS	7C235-30C-
63RS881S	7C235-30C-
63S1681	7C292-50C
63S1681A	7C292-35C
63S1681AS	7C291-35C
63S1681S	7C291-50C
63S881	7C281-45C
63S881	7C282-45C
63S881A	7C281-30C
63S881A	7C282-30C
67401	7C401-10C
67401A	7C401-15C
67401B	7C403-25C
67401D	7C403-25C
67402	7C402-10C
67402A	7C402-15C
67402B	7C402-25C
67402D	7C404-25C
67411	7C403-25C
67412	7C402-25C
67L402	7C402-10C
C57401	7C401-10M
C57401A	7C401-10M
C57402	7C402-10M
C57402A	7C402-10M
C67401A	7C401-15C
C67401B	7C403-25C
C67402	7C402-10C
C67402A	7C402-15C
C67402B	7C404-25C
C67L401	7C401-5C
C67401D	7C401-15C
C67402D	7C402-15C
PAL12L10C	PLDC20G10-35C
PAL12L10M	PLDC20G10-40M
PAL14L8C	PLDC20G10-35C
PAL14L8M	PLD20G10-40M
PAL16L6C	PLD20G10-35C
PAL16L6M	PLDC20G10-40M
PAL16L8A-2C	PALC16L8-35C

MMI/AMD	CYPRESS
PAL16L8A-2M	PALC16L8-40M
PAL16L8A-4C	PALC16L8L-35C
PAL16L8A-4M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16L8B-2C	PALC16L8-35C
PAL16L8B-2M	PALC16L8-30M
PAL16L8B-4C	PALC16L8L-35C
PAL16L8B-4M	PALC16L8-40M
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8D-4C	PALC16L8L-25C
PAL16L8D-4M	PALC16L8-30M
PAL16L8M	PALC16L8-40M
PAL16R4A-2C	PALC16R4-35C
PAL16R4A-2M	PALC16R4-40M
PAL16R4A-4C	PALC16R4L-35C
PAL16R4A-4M	PALC16R4-40M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R4B-2C	PALC16R4-25C
PAL16R4B-2M	PALC16R4-30M
PAL16R4B-4C	PALC16R4L-35C
PAL16R4B-4M	PALC16R4-40M
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4D-4C	PALC16R4L-25C
PAL16R4M	PALC16R4-40M
PAL16R6A-2C	PALC16R6-35C
PAL16R6A-2M	PALC16R6-40M
PAL16R6A-4C	PALC16R6L-35C
PAL16R6A-4M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R6B-2C	PALC16R6-25C
PAL16R6B-2M	PALC16R6-30M
PAL16R6B-4C	PALC16R6L-35C
PAL16R6B-4M	PALC16R6-40M
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6D-4C	PALC16R6L-25C
PAL16R6M	PALC16R6-40M
PAL16R8A-2C	PALC16R8-35C
PAL16R8A-2M	PALC16R8-40M
PAL16R8A-4C	PALC16R8L-35C
PAL16R8A-4M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL16R8B-2C	PALC16R8-25C
PAL16R8B-2M	PALC16R8-30M
PAL16R8B-4C	PALC16R8L-35C
PAL16R8B-4M	PALC16R8-40M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8D-4C	PALC1648L-25C
PAL16R8M	PALC16R8-40M
PAL18L4C	PLDC20G10-35C
PAL18L4M	PLDC20G10-40M
PAL20L10AC	PLDC20G10-35C
PAL20L10AM	PLDC20G10-30M
PAL20L10C	PLDC20G10-35C
PAL20L10M	PLDC20G10-40M

MMI/AMD	CYPRESS
PAL20L2C	PLDC20G10-35C
PAL20L2M	PLDC20G10-40M
PAL20L8A-2C	PLDC20G10-35C
PAL20L8A-2M	PLDC20G10-40M
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L8C	PLDC20G10-35C
PAL20L8M	PLDC20G10-40M
PAL20R4A-2C	PLDC20G10-35C
PAL20R4A-2M	PLDC20G10-40M
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M
PAL20R4C	PLDC20G10-35C
PAL20R4M	PLDC20G10-40M
PAL20R6A-2C	PLDC20G10-35C
PAL20R6A-2M	PLDC20G10-40M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R6C	PLDC20G10-35C
PAL20R6M	PLDC20G10-40M
PAL20R8A-2C	PLDC20G10-35C
PAL20R8A-2M	PLDC20G10-40M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL20R8C	PLDC20G10-35C
PAL20R8M	PLDC20G10-40M
PALC22V10/A	PALC22V10-35C
PLE10P8C	7C281-30C
PLE10P8C	7C282-30C
PLE10P8M	7C281-45M
PLE10P8M	7C282-45M
PLE10R8C	7C235-30C-
PLE10R8M	7C235-40M-
PLE11P8C	7C291-35C
PLE11P8M	7C291-35M
PLE11RA8C	7C245-35C-
PLE11RA8M	7C245-35M-
PLE11RS8C	7C245-35C-
PLE11RS8M	7C245-35M-
PLE9R8C	7C225-30C
PLE9R8M	7C225-35M

MOSIAC	CYPRESS
PREFIX:MS	PREFIX:SYM
8128SC-100	1420HD-85C
8128SC-100	1421HD-85C
8128SC-45	1420HD-45C
8128SC-55	1420HD-55C
8128SC-70	1420HD-70C
8128SC-70	1421HD-70C

MOSTEK	CYPRESS
PREFIX:ET	PREFIX:CY
PREFIX:MK	PREFIX:CY
PREFIX:TS	PREFIX:CY
SUFFIX:N	SUFFIX:P
SUFFIX:P	SUFFIX:D
41H67-25	7C167-25C+
41H67-35	7C167-35+
41H68-25	7C168-25C+
41H68-35	7C168-35C+
41H69-25	7C169-25

MOSTEK	CYPRESS
41H69-35	7C169-35C
41L67-25	7C167-25C-
41L67-35	7C167-35-
41L67-45	7C167-35-

MOTOROLA	CYPRESS
PREFIX:MCM	PREFIX:CY
SUFFIX:P	SUFFIX:P
SUFFIX:S	SUFFIX:D
SUFFIX:Z	SUFFIX:L
10422-10C	10E422-7C
1423-45	7C168-45C+
2016H-45	6116-45C
2016H-55	6116-55C
2016H-70	6116-55C
2018-35	7C128-35C
2018-45	7C128-45C
2167H-35	7C167-35C
2167H-45	7C167-45C
2167H-55	7C167-45C
6147-55	7C147-45C*
6147-70	7C147-45C*
6164-45	7C186-45C
6164-55	7C186-55C
6164-70	7C186-55C
6168-35	7C168-35C+
6168-45	7C168-45C+
6168-55	7C168-45C+
6168-70	7C168-45C+
61L47-55	7C147-45C*
61L47-70	7C147-45C*
61L64-45	7C186-45C
61L64-55	7C186-55C
61L64-70	7C186-55C
6268-25	7C168-25C
6268-35	7C168-35C
6269-25	7C169-25C
6269-35	7C169-35C
6270-25	7C170-25C
6270-35	7C170-35C
6270-45	7C170-45C
6287-25	7C187-25C
6287-35	7C187-35C
6287-45	7C187-45C
6288-25C	7C164-25C
6288-35C	7C164-35C
6288-35M	7C164-35M
6288-45M	7C164-45M
6290-25C	7C166-25C
6290-35C	7C166-35C
6290-35M	7C166-35M
6290-45C	7C166-45C
6290-45M	7C166-45M
62L87-25	7C187-25C
62L87-35	7C187-35C+
7681	7C282-45C
7681A	7C282-45C
93422	93422C
93422	93422M
93422A	93422AC
93422A	93422AM
93L422	93L422C

MOTOROLA	CYPRESS
93L422	93L422M
93L422A	93L422AC
93L422A	93L422AM

NATIONAL	CYPRESS
PREFIX:DM	PREFIX:CY
PREIFX:IDM	PREFIX:CY
PREFIX:NMC	PREFIX:CY
SUFFIX:J	SUFFIX:D
SUFFIX:N	SUFFIX:P
100422-10C	100E422-7C
100422-5C	100E422-5C
100422A-7C	100E422-7C
100422AC	100E422-7C
100474A-10C	100E474-7C
100474A-8C	100E474-7C
10422-10C	10E422-7C
10422-5C	10E422-5C
10422A-7C	10E422-7C
10422AC	10E422-7C
1047A-10C	10E474-7C
10474A-8C	10E474-7C
12L10C	PLDC20G10-35C
14L8C	PLDC20G10-35C
14L8M	PLDC20G10-40M
16L6C	PLDC20G10-35C
16L6M	PLDC20G10-40M
18L4C	PLDC20G10-35C
18L4M	PLDC20G10-40M
20L2M	PLDC20G10-40M
2147H	2147-55C
2147H	2147-55M
2147H-1	2147-35C
2147H-2	2147-45C
2147H-3	2147-55C
2147H-3	2147-55M
2147H-3L	7C147-45C
2148H	2148-55C
2148H-2	2148-45C
2148H-3	2148-55C
2148H-3L	21L48-55C
2148HL	21L48-55C
2901A-1C	7C901-31C
2901A-1M	7C901-32M
2901A-2C	7C901-31C
2901A-2M	7C901-32M
2901AC	7C901-31C
2901AM	7C901-32M
2909AC	2909AC
2909AM	2909M
2911AC	2911AC
2911AM	2911M
54S189	54S189M
54S189A	7C189-25M
74S189	74S189C
74S189A	27S03AC
75S07	7C190-25M
75S07A	27S07AM
77LS181	7C282-45M
77S181	7C282-45M
77S181A	7C282-45M
77S191	7C292-50M

NATIONAL	CYPRESS
77S191A	7C292-50M
77S191B	7C292-50M
77S281	7C281-45M
77S281A	7C281-45M
77S291	7C291-50M
77S291A	7C291-50M
77S291B	7C291-50M
77S401	7C401-10M
77S401A	7C401-10M
77S402	7C402-10M
77S402A	7C402-10M
77SR181	7C235-40M
77SR25	7C225-40M
77SR25B	7C225-40M
77ST476	7C225-40M-
77SR476B	7C225-40M-
85S07	27S07C
85S07A	27S07AC
85S07A	7C128-45C+
87LS181	7C282-45C
87S181	7C282-45C
87S191	7C292-50C
87S191A	7C292-35C
87S191B	7C292-35C
87S281	7C281-45C
87S281A	7C281-45C
87S291	7C291-50C
87S291A	7C291-35C
87S291B	7C291-35C
87S401	7C401-10C
87S401A	7C401-15C
87S402	7C402-10C
87S402A	7C402-15C
87SR181	7C235-30C
87S625	7C225-40C
87SR25B	7C225-30C
87SR476	7C225-40C-
87SR476B	7C225-30C-
PAL10016P4-2.5	100E302-2.5C
PAL10016P4-4C	100E302-4C
PAL10016P4-6C	100E302-6C
PAL10016P8-3C	100E301-3C
PAL10016P8-4C	100E301-4C
PAL10016P8-6C	100E301-6C
PAL1016P4-2.5C	10E302-2.5C
PAL1016P4-4C	10E302-4C
PAL1016P4-6C	10E302-6C
PAL1016P8-3C	10E301-3C
PAL1016P8-4C	10E301-4C
PAL1016P8-6C	10E301-6C
PAL16L8A2C	PALC16L8-35C
PAL16L8A2M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16L8B2C	PALC16L8-25C
PAL16L8B2M	PALC16L8-30M
PAL16L8B4C	PALC16L8L-35C
PAL16L8B4M	PALC16L8-40M
PAL16L8BM	PALC16L8-20M
PAL16L8C	PALC16L8-35C
PAL16L8M	PALC16L8-40M
PAL16R4A2C	PALC16R4-35C

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
– = functionally equivalent.
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

NATIONAL	CYPRESS
PAL164A2M	PALC16R4-40M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R4B2C	PALC16R4-25C
PAL16R4B2M	PALC16R4-30M
PAL16R4B4C	PALC16R4L-35C
PAL16R4B4M	PALC16R4-40M
PAL16R4BM	PALC16R4-20M
PAL16R4C	PALC16R4-35C
PAL16R4M	PALC16R4-40M
PAL16R6A2C	PALC16R6-35C
PAL16R6A2M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R6B2C	PALC16R6-25C
PAL16R6B2M	PALC16R6-30M
PAL16R6B4C	PALC16R6L-35C
PAL16R6B4M	PALC16R6-40M
PAL16R6BM	PALC16R6-20M
PAL16R6C	PALC16R6-35C
PAL16R6M	PALC16R6-40M
PAL16R8A2C	PALC16R8-35C
PAL16R8A2M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL16R8B2C	PALC16R8-25C
PAL16R8B2M	PALC16R8-30M
PAL16R8B4C	PALC16R8L-35C
PAL16R8B4M	PALC16R8-40M
PAL16R8BM	PALC16R8-20M
PAL16R8C	PALC16R8-35C
PAL16R8M	PALC16R8-40M
PAL20L10B2C	PLDC20G10-25C
PAL20L10B2M	PLDC20G10-30M
PAL20L10C	PLDC20G10-35C
PAL20L10M	PLDC20G10-40M
PAL20L2C	PLDC20G10-35C
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20L8BC	PLDC20G10-25C
PAL20L8BM	PLDC20G10-30M
PAL20L8C	PLDC20G10-35C
PAL20L8M	PLDC20G10-40M
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M
PAL20R4BC	PLDC20G10-25C
PAL20R4BM	PLDC20G10-30M
PAL20R4C	PLDC20G10-35C
PAL20R4M	PLDC20G10-40M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R6BC	PLDC20G10-25C
PAL20R6BM	PLDC20G10-30M
PAL20R6C	PLDC20G10-35C
PAL20R6M	PLDC20G10-40M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M
PAL20R8BC	PLDC20G10-25C
PAL20R8BM	PLDC20G10-30M
PAL20R8C	PLDC20G10-35C
PAL20R8M	PLDC20G10-40M

NEC	CYPRESS
PREFIX:uPD	PREFIX:CY
SUFFIX:C	SUFFIX:P
SUFFIX:D	SUFFIX:D
SUFFIX:K	SUFFIX:L
SUFFIX:L	SUFFIX:F
100422-10C	100E422-7C
100422-7C	100E422-7C
100474-10C	100E474-7C
100474-8C	100E474-7C
10422-10C	10E422-7C
10422-7C	10E422-7C
10474-10C	10E474-7C
10474-8C	10E474-7C
2147-2	2147-55C
2147-3	2147-55C
2147A-25	7C147-25C
2147A-35	2147-35C
2147A-45	2147-45C
2149	2149-55C
2149-1	2149-45C
2149-2	2149-35C
2167-2	7C167-45C
2167-3	7C167-45C
429	7C292-50C
429-1	7C292-50C
429-2	7C292-50C
429-3	7C292-35C
4311-45	7C167-45C
4311-55	7C167-45C
4361-40	7C187-35C
4361-45	7C187-45C
4361-55	7C187-45C
4361-70	7C187-45C
4362-45	7C164-45C
4362-55	7C164-45C
4362-70	7C164-45C
4363-45	7C166-45C
4363-55	7C166-45C
4363-70	7C166-45C

PERFORMANCE	CYPRESS
PREFIX:P	PREFIX:CY
4C150-12C	7C150-12C
4C150-15C	7C150-15C
4C150-15M	7C150-15M
4C150-20C	7C150-15C
4C150-20M	7C150-15M
4C150-25C	7C150-25C
4C150-25M	7C150-25M
4C150-35M	7C150-35M
4C164P-20C	7C185-20C
4C164DW-20C	7C186-20C
4C164P-25C	7C185-25C
4C164DW-25C	7C186-25C
4C164P-25M	7C185-25M
4C164DW-25M	7C186-25M
4C164P-35C	7C185-35C
4C164DW-35C	7C186-35C
4C164P-35M	7C185-35M
4C164DW-35M	7C186-35M
4C164P-45C	7C185-45C
4C164DW-45C	7C186-45C

PERFORMANCE	CYPRESS
4C164P-45M	7C185-45M
4C164DW-45M	7C186-45M
4C164P-55C	7C185-55C
4C164DW-55C	7C186-55C
4C164P-55M	7C185-55M
4C164DW-55M	7C186-55M
4C1681-25C	7C171-25C
4C1681-35C	7C171-35C
4C1681-35M	7C171-35M
4C1681-45C	7C171-45C
4C1681-45M	7C171-45M
4C1682-25C	7C172-25C
4C1682-35C	7C172-35C
4C1682-35M	7C172-35M
4C1682-45C	7C172-45C
4C1682-45M	7C172-45M
4C169-25C	7C169-25C
4C169-30C	7C169-25C
4C169-35C	7C169-35C
4C169-35M	7C169-35M
4C169-45M	7C169-45M
4C187-20C	7C187-20C
4C187-25C	7C187-25C
4C187-25M	7C187-25M
4C187-35M	7C187-35M
4C188-20C	7C164-20C
4C188-25C	7C164-25C
4C188-25M	7C164-25M
4C188-35C	7C164-35C
4C188-35M	7C164-35M
4C188-45M	7C164-45M
4C1981-20C	7C161-20C
4C1981-25C	7C161-25C
4C1981-25M	7C161-25M
4C1981-35C	7C161-35C
4C1981-35M	7C161-35M
4C1981-45M	7C161-45M
4C1981-55M	7C161-55M
4C1982-20C	7C162-20C
4C1982-25C	7C162-25C
4C1982-25M	7C162-25M
4C1982-35C	7C162-35C
4C1982-35M	7C162-35M
4C1982-45M	7C162-45M
4C1982-55M	7C162-55M
4C198-20C	7C166-20C
4C198-25C	7C166-25C
4C198-25M	7C166-25M
4C198-35C	7C166-35C
4C198-35M	7C166-35M
4C198-45M	7C166-45M
93U422-35C	7C122-15C
93U422-35C	7C122-25C
93U422-35C	7C122-35C
93U422-35M	7C122-25M
93U422-35M	7C122-35M

RAYTHEON	CYPRESS
PREFIX:R	PREFIX:CY
SUFFIX:B	SUFFIX:B
SUFFIX:D	SUFFIX:D
SUFFIX:F	SUFFIX:F

PERFORMANCE	CYPRESS
SUFFIX:L	SUFFIX:L
SUFFIX:S	SUFFIX:S
29631AC	7C282-45C
29631AM	7C282-45M
29631ASC	7C281-45C
29631ASM	7C281-45M
29631C	7C282-45C
29631M	7C282-45M
29631SC	7C281-45C
29631SM	7C281-45M
29633AC	7C282-45C+
29633AM	7C282-45M+
29633ASC	7C281-45C+
29633ASM	7C281-45M+
29633C	7C282-45C+
29633M	7C282-45M+
29633SC	7C281-45C+
29633SM	7C281-45M+
29681AC	7C292-50C
29681AM	7C292-50M
29681ASC	7C291-50C
29681ASM	7C291-50M
29681C	7C292-50C
29681M	7C292-50M
29681SC	7C291-50C
29681SM	7C291-50M
29683AC	7C292-50C+
29683AM	7C292-50M+
29683ASC	7C291-50C+
29683ASM	7C291-50M+
29683C	7C292-50C+
29683M	7C292-50M+
29683SC	7C291-50C+
29683SM	7C291-50M+
29VP864DB	7C264-55M
29VP864SB	7C263-55M
29VS864SB	7C261-55M
39VP864D	7C264-55C
39VP864S	7C263-55C
39VS864S	7C261-55C

SIGNETICS	CYPRESS
PREFIX:N	PREFIX:CY
PREFIX:S	PREFIX:CY
SUFFIX:883B	SUFFIX:B
SUFFIX:F	SUFFIX:D
SUFFIX:G	SUFFIX:L
SUFFIX:N	SUFFIX:P
SUFFIX:R	SUFFIX:F
100422BC	100E422-7C
100422CC	100E422-7C
100474AC	100E474-7C
10422BC	10E422-7C
10422CC	10E422-7C
10474AC	10474-7C
N74S189	74S189C
N82HS641	7C264-55C
N82HS641A	7C264-45C
N82HS641B	7C264-35C
N82LS181	7C282-45C
N82S181	7C282-45C
N82S181A	7C282-45C
N82S181B	7C282-45C
N82S191A-3	7C291-50C
N82S191A-6	7C292-50C
N82S191B-3	7C291-35C
N82S191B-6	7C292-35C
N82S191-3	7C291-50C
N82S191-6	7C292-50C
SS4S189	54S189M
S82HS641	7C264-55M
S82LS181	7C282-45M
S82S181	7C282-45M
S82S181A	7C282-45M
S82S191A-3	7C291-50M
S82S191A-6	7C292-50M
S82S191B-3	7C291-50M
S82S191B-6	7C292-50M
S82S191-3	7C291-50M
S82S191-6	7C292-50M

TI	CYPRESS
PREFIX:JBP	PREFIX:CY
PREFIX:PAL	SUFFIX:P
PREFIX:SN	PREFIX:CY
PREFIX:TBP	PREFIX:CY
PREFIX:TIB	PREFIX:CY
PREFIX:TMS	PREFIX:CY
SUFFIX:F	SUFFIX:F
SUFFIX:J	SUFFIX:L
SUFFIX:N	SUFFIX:D
10016P8-3C	100E301-3C
10016P8-4C	100E301-4C
10016P8-6C	100E301-6C
10H16P8-3C	10E301-3C
10H16P8-4C	10E301-4C
10H16P8-6C	10E301-6C
22V10AC	PALC22V10-25C
22V10AM	PALC22V10-30M
27C291-3	7C291L-35C+
27C291-30	7C291L-35C+
27C291-5	7C291L-50C+
27C291-50	7C291L-50C+
27C292-3	7C292L-35C+
27C292-35	7C292L-35C+
27C292-5	7C292L-50C+
27C292-50	7C292L-50C+
28L166W	7C292-50C
28L86AMW	7C282-45M
28L86AW	7C282-45C
28S166W	7C292-50C
28S86AMW	7C282-45M
28S86AW	7C282-45C
320C601-25	7C601-25
320C601-33	7C601-33
320C602-25	7C602-25
320C602-33	7C602-33
320C604-25	7C604-25
320C604-33	7C604-33
38L165-35C	7C291-35C
38L165-45C	7C291-35C
38L166-35	7C292-35C
38L166-45	7C292-35C
38L85-45C	7C281-45C

TI	CYPRESS
38R165-18C	7C245-25C
38R165-25C	7C245-35C
38R85-15C	7C235-30C
38S165-25C	7C291A-25C
38S165-35C	7C291-35C
38S85-30C	7C281-30C
54HC189	7C189-25M
54HCT189	7C189-25M
54LS189A	27LS03M
54LS219A	7C190-25M+
54S189A	54S189M
7489	7C189-25C
74ACT29116	7C9116AC
74ACT29116-1	7C9116AC
74HC189	7C189-25C
74HC219	7C190-25C
74HCT189	7C189-25C
74LS189A	27LS03C
74LS219A	27S07C+
74S189A	74S189C
74S189B	7C189-25C
HCT9510E	7C510-75C+
HCT9510E-10	7C510-75C+
HCT9510M	7C510-75M+
PAL16L8-20M	PALC16L8-20M
PAL16L8-25C	PALC16L8-25C
PAL16L8-30M	PALC16L8-30M
PAL16L8A-2C	PALC16L8-35C
PAL16L8A-2M	PALC16L8-40M
PAL16L8AC	PALC16L8-25C
PAL16L8AM	PALC16L8-30M
PAL16R4-20M	PALC16R4-20M
PAL16R4-25C	PALC16R4-25C
PAL16R4-30M	PALC16R4-30M
PAL16R4A-2C	PALC16R4-25C
PAL16R4A-2M	PALC16R4-40M
PAL16R4AC	PALC16R4-25C
PAL16R4AM	PALC16R4-30M
PAL16R6-20M	PALC16R6-20M
PAL16R6-25C	PALC16R6-25C
PAL16R6-30M	PALC16R6-30M
PAL16R6A-2C	PALC16R6-25C
PAL16R6A-2M	PALC16R6-40M
PAL16R6AC	PALC16R6-25C
PAL16R6AM	PALC16R6-30M
PAL16R8-20M	PALC16R8-20M
PAL16R8-25C	PALC16R8-25C
PAL16R8-30M	PALC16R8-30M
PAL16R8A-2C	PALC16R8-25C
PAL16R8A-2M	PALC16R8-40M
PAL16R8AC	PALC16R8-25C
PAL16R8AM	PALC16R8-30M
PAL20L10A-2C	PLDC20G10-25C
PAL20L10A-2M	PLDC20G10-30M
PAL20L10AC	PLDC20G10-35C
PAL20L10AM	PLDC20G10-30M
PAL20L8A-2C	PLDC20G10-25C
PAL20L8A-2M	PLDC20G10-30M
PAL20L8AC	PLDC20G10-25C
PAL20L8AM	PLDC20G10-30M
PAL20R4A-2C	PLDC20G10-25C
PAL20R4A-2M	PLDC20G10-30M

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};

+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
– = functionally equivalent.
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

TI	CYPRESS
PAL20R4AC	PLDC20G10-25C
PAL20R4AM	PLDC20G10-30M
PAL20R6A-2C	PLDC20G10-25C
PAL20R6A-2M	PLDC20G10-30M
PAL20R6AC	PLDC20G10-25C
PAL20R6AM	PLDC20G10-30M
PAL20R8A-2C	PLDC20G10-25C
PAL20R8A-2M	PLDC20G10-30M
PAL20R8AC	PLDC20G10-25C
PAL20R8AM	PLDC20G10-30M

TOSHIBA	CYPRESS
PREFIX:P	SUFFIX:P
PREFIX:TMM	PREFIX:CY
SUFFIX:D	SUFFIX:D
2015A-10	7C128-55C+
2015A-12	7C128-55C+
2015A-15	7C128-55C+
2015A-90	7C128-55C+
2018-25	7C128-25C
2018-35	7C128-35C
2018-45	7C128-45C
2018-55	7C128-55C+
2068-25	7C168-25C
2068-35	7C168-35C
2068-45	7C168-45C
2068-55	7C168-45C
2069-35	7C169-35C
2078-35	7C170-35C
2078-45	7C170-45C
2078-55	7C170-45C
2088-35	7C186-35C
2088-45	7C186-45C
2088-55	7C186-55C
315	2147-55C
315-1	2147-55C
55416-35	7C164-35C
55416-45	7C164-45C
55417-25	7C166-25C
55417-35	7C166-35C
55417-45	7C166-45C
5561-45	7C187-45C+
5561-55	7C187-45C+
5561-70	7C187-45C+
5562-35	7C187-35C
5562-45	7C187-45C
5562-55	7C187-45C

TRW	CYPRESS
MPY016HA	7C516-75M
MPY016HC	7C516-75C
MPY016KA	7C516-75M
MPY016KC	7C516-75C
TDC1010A	7C510-75M
TDC1010C	7C510-75C
TMC2010A	7C510-75M+
TMC2010C	7C510-75C+
TMC2110A	7C510-75M
TMC2110C	7C510-75C
TMC216HA	7C516-75M
TMC216HC	7C516-75C+

VTI	CYPRESS
20C18-25	7C128-25C+
20C18-35	7C128-35C+
20C19-25	7C128-25C
20C19-35	7C128-35C
20C68-25	7C168-25C+
20C68-35	7C168-35C+
20C69-25	7C169-25C
20C69-35	7C169-35C
20C69-45	7C169-45C
20C78-25	7C170-25C+
20C78-35	7C170-35C+
20C78-45	7C170-45C+
20C79-25	7C170-25C
20C79-35	7C170-35C
20C79-45	7C170-45C
20C98-35	7C185-35C+
20C98-45	7C185-45C+
20C99-35	7C185-35C
20C99-45	7C185-45C
2130-10C	7C130-55C
2130-12C	7C130-55C
2130-15C	7C130-55C
7132-55	7C132-55C
7132-70	7C132-55C
7132A-35	7C132-35C
7132A-45	7C132-45C
7142-55	7C142-55C
7142-70	7C142-55C
7142A-35	7C142-35C
7142A-45	7C142-45C
7C122-15	7C122-15C
7C122-25	7C122-25C
7C122-35	7C122-35C
VL2010-65	7C510-65C
VL2010-70	7C510-65C
VL2010-90	7C510-75C
VT64KS4-35	7C164-35C
VT64KS4-45	7C164-45C
VT64KS4-55	7C164-45C
VT65KS4-35	7C166-35C
VT65KS4-45	7C166-45C
VT65KS4-55	7C166-45C

WSI	CYPRESS
PREFIX:WS	PREFIX:CY
SUFFIX:C	PREFIX:CY
SUFFIX:D	PREFIX:CY
SUFFIX:M	SUFFIX:P
SUFFIX:P	PREFIX:CY
29C01C	7C901-31C
57C128F-70	7C251-55C
57C128F-70M	7C251-55M+
57C128F-90	7C251-55C
57C128F-90M	7C251-55M+
57C191B-35	7C292-35C
57C191B-35M	7C292-35M
57C191B-45	7C292-35C
57C191B-45M	7C292-35M
57C191-45	7C292-35C
57C191-45M	7C292-35M
57C191-55	7C292-50C
57C191-55M	7C292-50M

WSI	CYPRESS
57C191-70	7C292-50C
57C191-70M	7C292-50M
57C291B-35	7C291-35C
57C291B-35M	7C291-35M
57C291B-45	7C291-35C
57C291B-45M	7C291-35M
57C291-45	7C291-35C
57C291-45M	7C291-35M
57C291-55	7C291-50C
57C291-55M	7C291-50M
57C291-70	7C291-50C
57C291-70M	7C291-50M
57C45-20	7C245A-15C
57C45-25	7C245A-25C
57C45-25M	7C245A-25M
57C45-35	7C245A-35C
57C45-35M	7C245A-35M
57C49B-35	7C264-30C
57C49B-35T	7C261-30C
57C49B-45	7C264-40C
57C49B-45T	7C261-40C
57C49B-55	7C264-45C
57C49B-55T	7C261-45C
57C49B-55TM	7C261-45M
57C49B-55TM	7C264-45M
57C291-55	7C291-50C
57C291-55	7C291-50C
57C49-55	7C264-55C+
57C49-55M	7C264-55M
57C49-70	7C264-55C+
57C49-70M	7C264-55M
57C49-90	7C264-55C+
57C49-90M	7C264-55M
59016C	7C9101-40C
59016C	7C9101-45M
5901C	2901CC+
5901M	2901CM+
5910AC	7C910-40C
5910AM	7C910-46M
59516	7C516-45C
59517	7C517-45C

WEITEK	CYPRESS
1010AC	7C510-75C
1010AM	7C510-75M
1010BC	7C510-75C
1010BM	7C510-75M
1010C	7C510-75C
1010M	7C510-75M
1516AC	7C516-75C
1516AM	7C516-75M
1516BC	7C516-55C
1516BM	7C516-75M
1516C	7C516-75C
1516M	7C516-75M
2010AC	7C510-55C
2010AM	7C510-75M
2010BC	7C510-45C
2010BM	7C510-55M
2010C	7C510-75C
2010DC	7C510-55C
2010DM	7C510-75M

1

WEITEK	CYPRESS
2010M	7C510-75M+
2516AC	7C516-55C
2516AM	7C516-75M
2516C	7C516-75C
2516DC	7C516-45C
2516DM	7C516-55M
2516M	7C516-75M+
2517AC	7C517-55C
2517AM	7C517-75M
2517C	7C517-75C
2517M	7C517-75M+

Note: Unless otherwise noted, product meets all performance specs and is within 10 mA on I_{CC} and 5 mA on I_{SB};
+ = meets all performance specs but may not meet I_{CC} or I_{SB};
* = meets all performance specs except 2V data retention—may not meet I_{CC} or I_{SB};
– = functionally equivalent.
† = SOIC only
‡ = 32-pin LCC crosses to the 7C198M

Section Contents

Static RAMs (Random Access Memory)

Page Number

Static RAMs (Random Access Memory) (continued)

Static RAMs (Random Access Memory) (continued) **Page Number**

CY2147

CYPRESS SEMICONDUCTOR

4096 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **35 ns**
- **Low active power**
  - **690 mW (commercial)**
  - **770 mW (military)**
- **Low standby power**
  - **140 mW**
- **TTL-compatible imputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

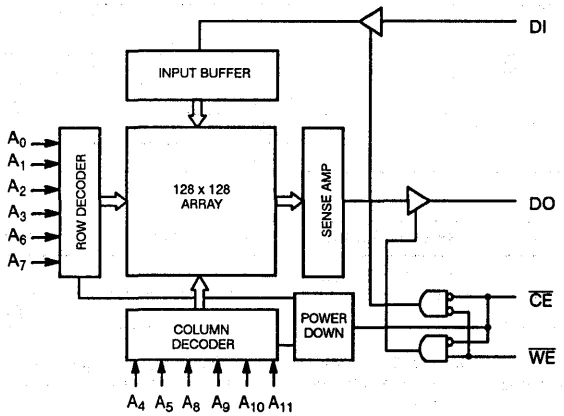
The CY2147 is a high-performance CMOS static RAM organized as 4096 by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY2147 has an automatic power-down feature, reducing the power consumption by 80% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

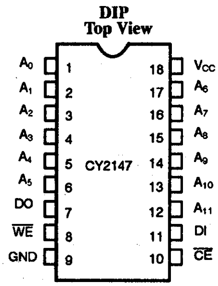
The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



2147-1

Pin Configuration



2147-2

Selection Guide (For higher performance and lower power, refer to CY7C147 data sheet.)

		2147-35	2147-45	2147-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commerical	125	125	125
	Military		140	140
Maximum Standby Current (mA)	Commerical	25	25	25
	Military		25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

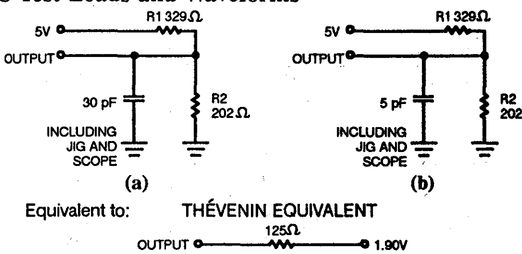
Parameters	Description	Test Conditions		2147 Min.	2147 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		-50	+50	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		125	mA
			Mil		140	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE} \geq V_{IH}$	Com'l		25	mA
			Mil		25	

Capacitance[5]

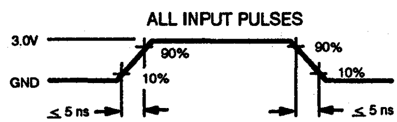
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



2147-3



2147-4

Switching Characteristics Over the Operating Range[2,6]

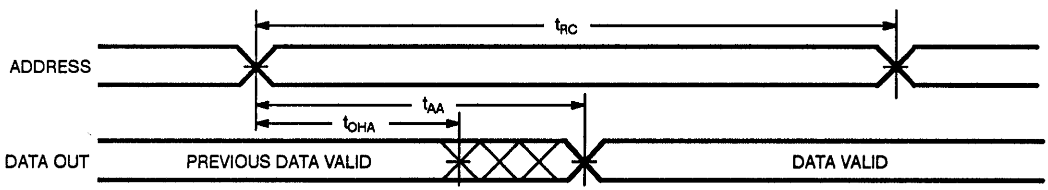
Parameters	Description	2147-35 Min.	2147-35 Max.	2147-45 Min.	2147-45 Max.	2147-55 Min.	2147-55 Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		45		55	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		30		30		30	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		20	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		45		45		ns
t_{AW}	Address Set-Up to Write End	35		45		45		ns
t_{HA}	Address Hold from Write End	0		0		10		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		ns
t_{SD}	Data Set-Up to Write End	20		25		25		ns
t_{HD}	Data Hold from Write End	10		10		10		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		20		25		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7, 8]	0		0		0		ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices.
8. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CE}$ transition low.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

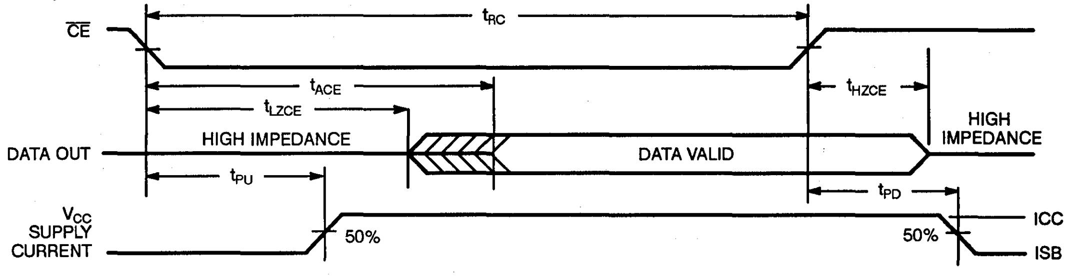
Read Cycle No. 1[10,11]



2147-5

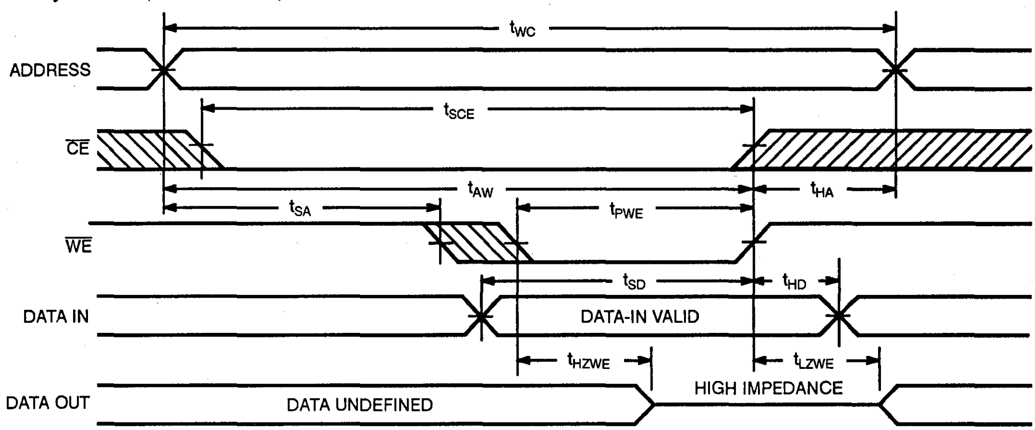
Switching Waveforms

Read Cycle No. 2[10, 12]



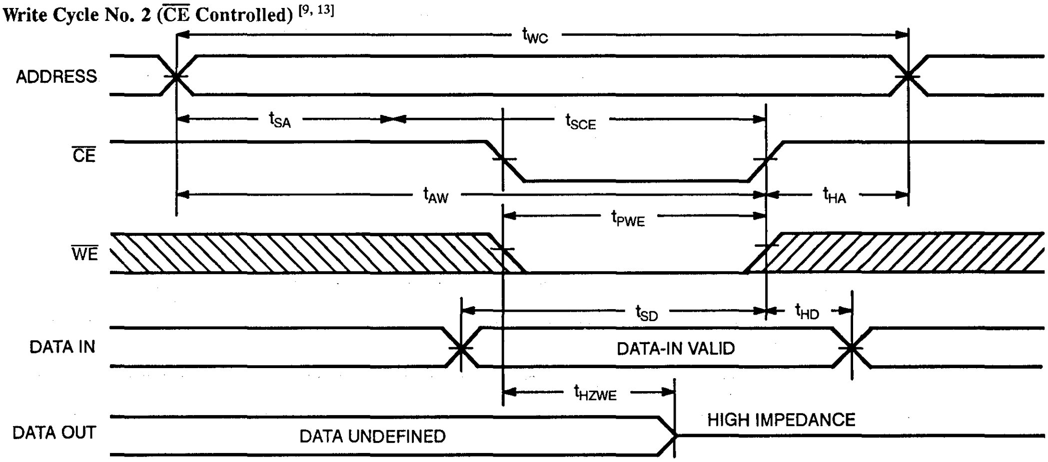
2147-6

Write Cycle No. 1 ($\overline{WE}$ Controlled) [9]



2147-7

Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 13]



2147-8

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C147-35PC	P3	Commercial
	CY7C147-35DC	D4	
45	CY7C147-45PC	P3	Commercial
	CY7C147-45DC	D4	
	CY7C147-45DMB	D4	Military
55	CY7C147-55PC	P3	Commercial
	CY7C147-55DC	D4	
	CY7C147-55DMB	D4	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00023-B

CY2148/CY21L48
CY2149/CY21L49

CYPRESS SEMICONDUCTOR

1,024 x 4 Static R/W RAM

Features

- Automated power-down when deselected (2148)
- CMOS for optimum speed/power
- Low power
  - 660 mW (commercial)
  - 770 mW (military)
- 5-volt power supply ± 10% tolerance both commercial and military
- TTL-compatible inputs and outputs

Functional Description

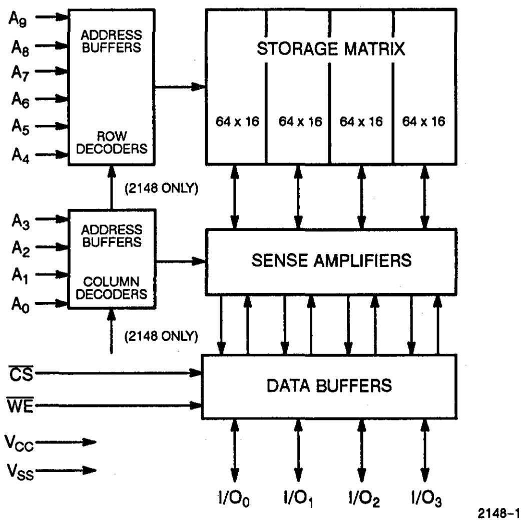
The CY2148 and CY2149 are high-performance CMOS static RAMs organized as 1024 by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The CY2148 and CY2149 are identical except that the CY2148 includes an automatic ($\overline{CS}$) power-down feature. The CY2148 remains in a low-power mode as long as the device remains deselected, i.e., ($\overline{CS}$) is HIGH, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY2149 does not affect the power dissipation of the device.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location addressed by the address present on the address pins (A_0 through A_9).

Reading the device is accomplished by selecting the device, ($\overline{CS}$) active LOW, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins (A_0 through A_9) is present on the four data input/output pins (I/O_0 through I/O_3).

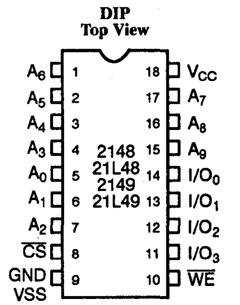
The input/output pins (I/O_0 through I/O_3) remain in a high-impedance state unless the chip is selected and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



2148-1

Pin Configuration



2148-2

Selection Guide (For higher performance and lower power refer to the CY7C148/9 data sheet)

		2148-35 2149-35	21L48-35 21L49-35	2148-45 2149-45	21L48-45 21L49-45	2148-55 2149-55	21L48-55 21L49-55
Maximum Access Time (ns)		35	35	45	45	55	55
Maximum Operating Current (mA)	Commercial	140	120	140	120	140	120
	Military			140		140	

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	−55°C to + 125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		2148 2149 Min.	2148 2149 Max.	21L48 21L49 Min.	21L48 21L49 Max.	Units
I_{OH}	Output HIGH Current	V_{CC} = Min., I_{OH} = −0.4 mA		2.4		2.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	mA
V_{IH}	Input HIGH Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{OH}$, Output Disabled	T_A = 0°C to +125°C	−50	+50	−50	+50	pF
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ Output Open	T_A = 0°C to +70°C		140		120	mA
			T_A = −55°C to +125°C		140			
I_{SB}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ (2148 only)	T_A = 0°C to +70°C		30		20	mA
			T_A = −55°C to +125°C		30			
I_{PO}	Peak Power-On Current[3]	Max. V_{CC}, $\overline{CS} \leq V_{IL}$ (2148 only)	T_A = 0°C to +70°C		50		30	mA
			T_A = −55°C to +125°C		50			
I_{OS}	Output Short Circuit Current[4]	GND $\leq V_O \leq V_{CC}$	T_A = 0°C to +70°C		±275		±275	mA
			T_A = −55°C to +125°C		±350			

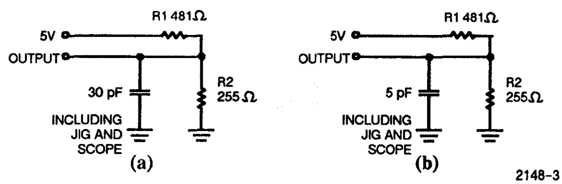
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

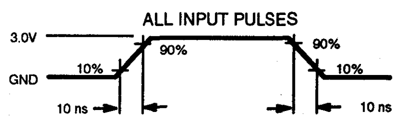
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power up. Otherwise, current will exceed values give (CY2148 only).
4. For test purposes, not more than 1 output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



2148-3



2148-4

Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[2]

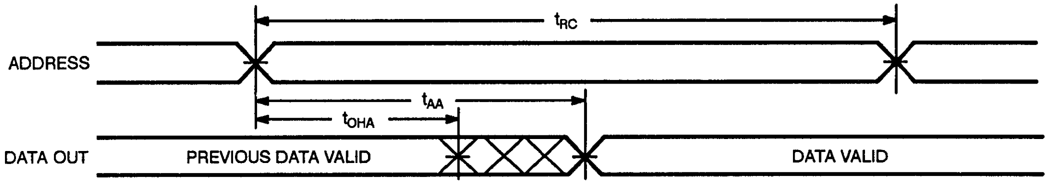
Parameters	Description		2148-35 / 2149-35 Min.	2148-35 / 2149-35 Max.	2148-45 / 2149-45 Min.	2148-45 / 2149-45 Max.	2148-55 / 2149-55 Min.	2148-55 / 2149-55 Max.	Units
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		35		45		55		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			35		45		55	ns
t_{ACS1}[6]	Chip Select LOW to Data Out Valid (CY2148 only)			35		45		55	ns
t_{ACS2}[7]				45		55		65	ns
t_{ACS}	Chip Select LOW to Data Out Valid (CY2149 only)			15		20		25	ns
t_{LZ}[8]	Chip Select LOW to Data Out Valid	2148	10		10		10		ns
		2149	5		5		5		
t_{HZ}[8]	Chp Select HIGH to Data Out Off		0	20	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		5		5		ns
t_{PD}	Chip Select HIGH to Power-Down Delay	2148		30		30		30	ns
t_{PU}	Chip Select LOW to Power-Up Delay	2149	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		35		45		55		ns
t_{WP}[9]	Write Enable LOW to Write Enable HIGH		30		35		40		ns
t_{WR}	Address Hold from Write End		5		5		5		ns
t_{WZ}[8]	Write Enable LOW to Output in High Z		0	10	0	15	0	20	ns
t_{DW}	Data-In Valid to Write Enable HIGH		20		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable LOW		0		0		0		ns
t_{CW}[9]	Chip Select LOW to Write Enable HIGH		30		40		50		ns
t_{OW}[8]	Write Enable HIGH to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		30		35		50		ns

Notes:
6. Chip deselected greater than 55 ns prior to selection.
7. Chip deselected less than 55 ns prior to selection.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in part (b) of AC Test Loads.
9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

2

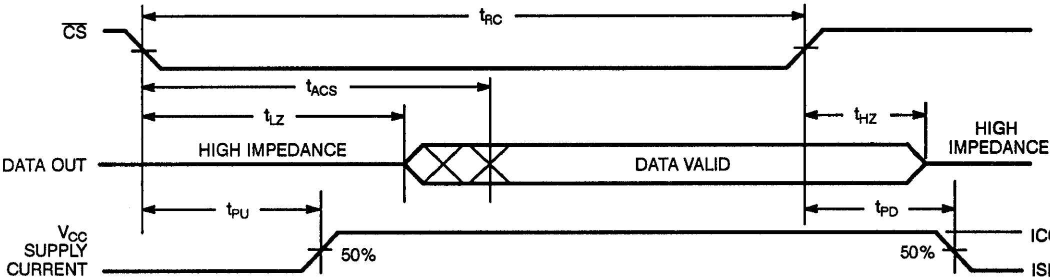
Switching Waveforms

Read Cycle No. 1[10, 11]



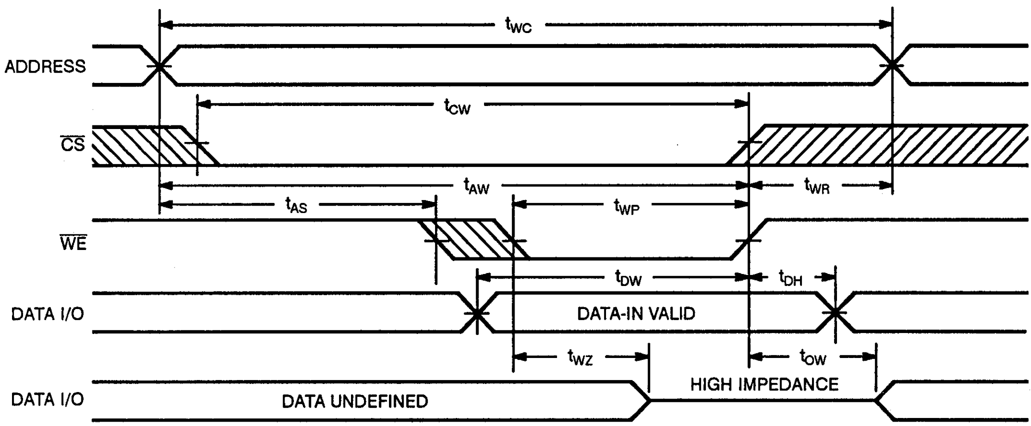
2148-5

Read Cycle No. 2[10, 12]



2148-6

Write Cycle No. 1 ($\overline{WE}$ Controlled)



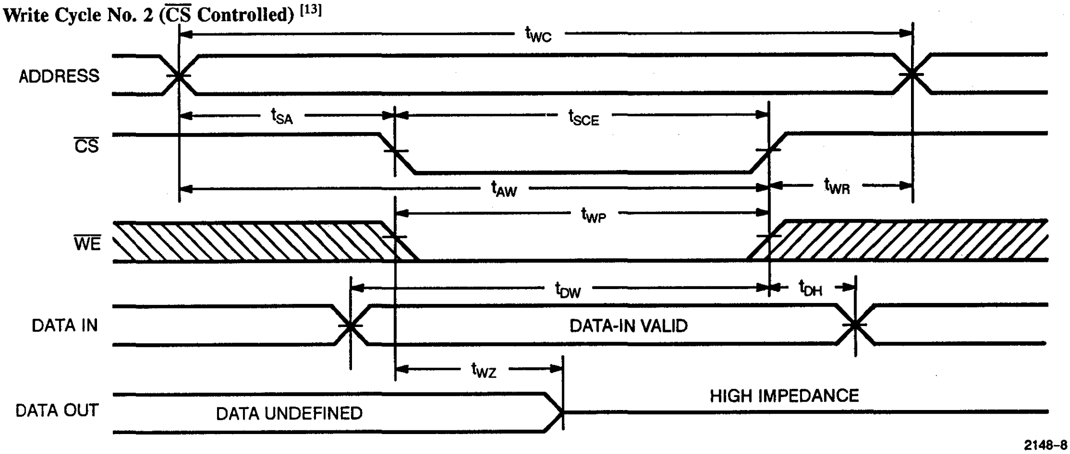
2148-7

Notes:

10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled) [13]



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY2148-35PC	P3	Commercial
	CY2148-35DC	D4	
45	CY2148-45PC	P3	Commercial
	CY2148-45DC	D4	
	CY2148-45DMB	D4	Military
55	CY2148-55PC	P3	Commercial
	CY2148-55DC	D4	
	CY2148-55DMB	D4	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY2149-35PC	P3	Commercial
	CY2149-35DC	D4	
45	CY2149-45PC	P3	Commercial
	CY2149-45DC	D4	
	CY2149-45DMB	D4	Military
55	CY2149-55PC	P3	Commercial
	CY2148-55DC	D4	
	CY2148-55DMB	D4	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY21L48-35PC	P3	Commercial
	CY21L48-35DC	D4	
45	CY21L48-45PC	P3	Commercial
	CY21L48-45DC	D4	
55	CY21L48-55PC	P3	Commercial
	CY21L48-20DC	D4	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY21L49-35PC	P3	Commercial
	CY21L49-35DC	D4	
45	CY21L49-45PC	P3	Commercial
	CY21L49-45DC	D4	
55	CY21L49-55PC	P3	Commercial
	CY21L49-55DC	D4	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
I_{OH}	1, 2, 3
I_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}[14]	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS1}[14]	7, 8, 9, 10, 11
t_{ACS2}[14]	7, 8, 9, 10, 11
t_{ACS}[15]	7, 8, 9, 10, 11
t_{OH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{WP}	7, 8, 9, 10, 11
t_{WR}	7, 8, 9, 10, 11
t_{DW}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11

Notes:
14. CY2148 only.
15. CY2149 only.

Document #: 38-00024-B

CYPRESS SEMICONDUCTOR

2048 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **35 ns**
- **Low active power**
  - **660 mW**
- **Low standby power**
  - **110 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

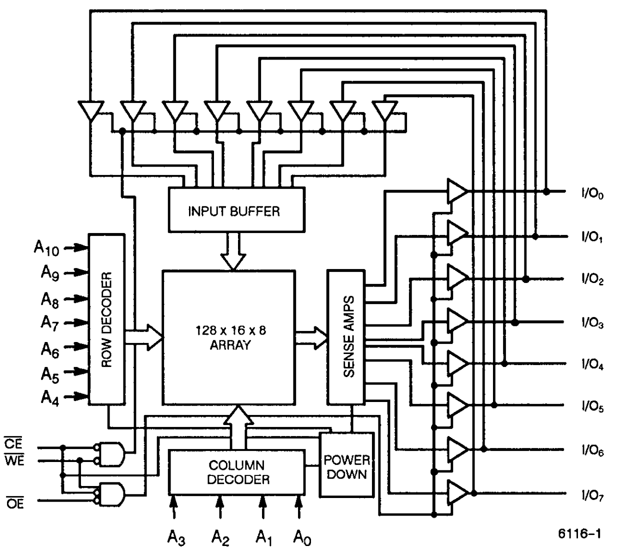
The CY6116 and CY6117 are high-performance CMOS Static RAMs organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY6116 and the CY6117 have an automatic power-down feature, reducing the power consumption by 83% when deselected.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{10}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

The CY6116 and CY6117 utilize a die coat to insure alpha immunity.

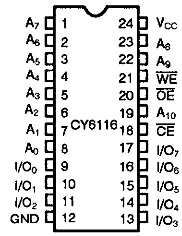
Logic Block Diagram



6116-1

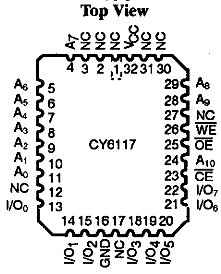
Pin Configurations

DIP/SOJ
Top View



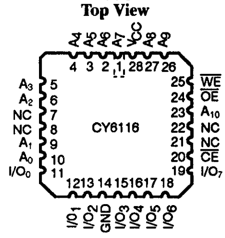
6116-2

LCC
Top View



6116-3

LCC
Top View



6116-4

Selection Guide

		CY6116-35 CY6117-35	CY6116-45 CY6117-45	CY6116-55 CY6117-55
Maximum Access Time (ns)		35	45	55
Maximum Standby Current (mA)	Commercial	120	120	120
	Military	130	130	130
Maximum Standby Current (mA)	Commercial	20	20	20
	Military	20	20	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[2]

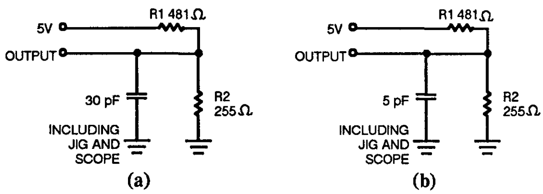
Parameters	Description	Test Conditions		CY6116 CY6117 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled			+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		120	mA
			Mil		130	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$	Com'l		20	mA
			Mil		20	

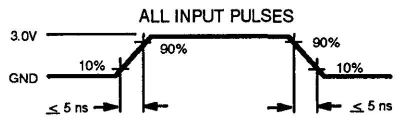
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

6116-5

C6116-6

Switching Characteristics Over the Operating Range[2, 5]

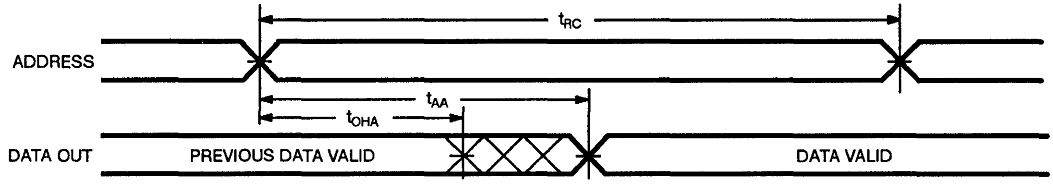
Parameters	Description	7C198-35 7C199-35 Min.	7C198-35 7C199-35 Max.	7C198-45 7C199-45 Min.	7C198-45 7C199-45 Max.	7C198-55 7C199-55 Min.	7C198-55 7C199-55 Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		15		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		25		25	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	30		40		40		ns
t_{AW}	Address Set-Up to Write End	30		40		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		20		25		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		15		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns

Notes:

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. Data I/O pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

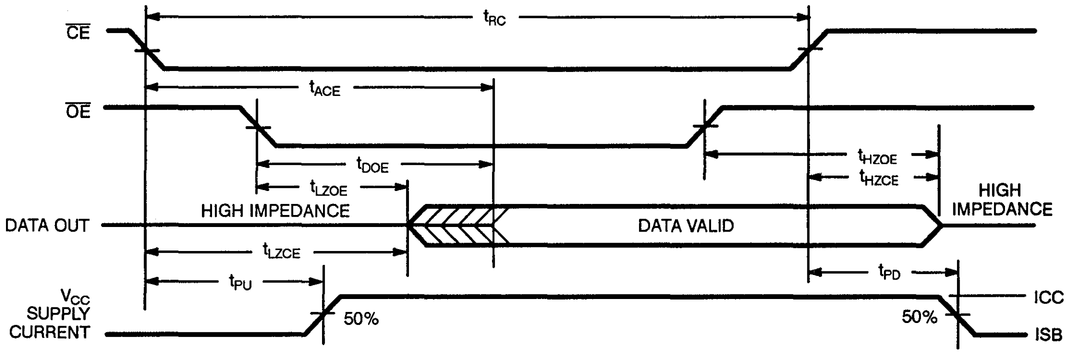
Switching Waveforms

Read Cycle No. 1[9, 10]



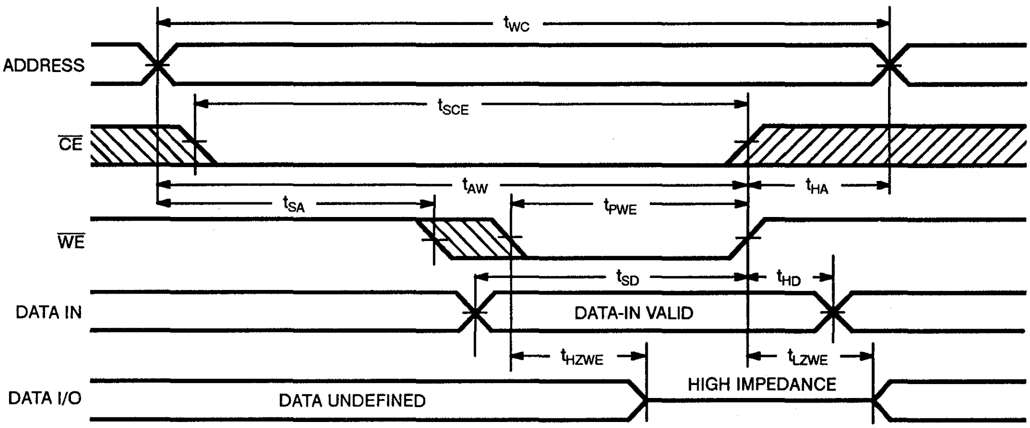
6116–7

Read Cycle No. 2[9, 11]



6116–8

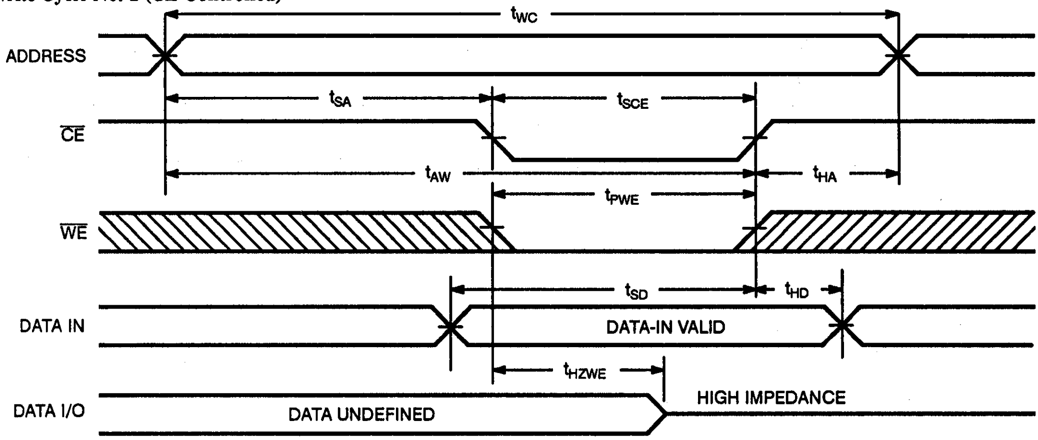
Write Cycle No. 1 (WE Controlled) [8, 12]



6116–9

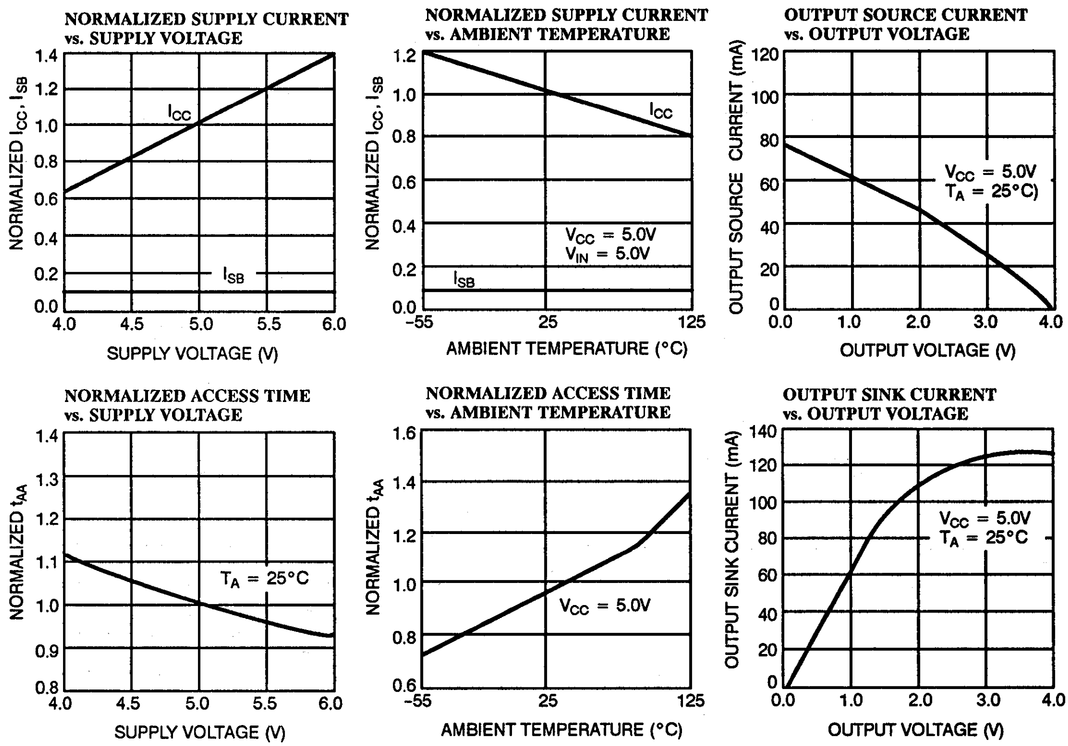
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) [8, 12, 13]



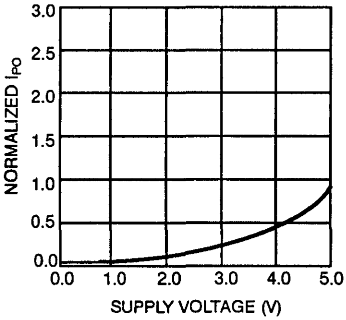
6116-10

Typical DC and AC Characteristics

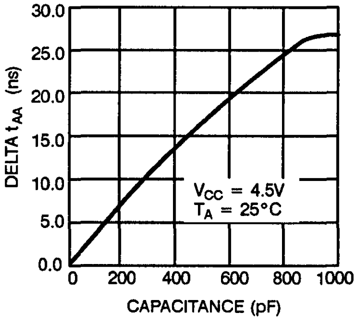


Typical DC and AC Characteristics (continued)

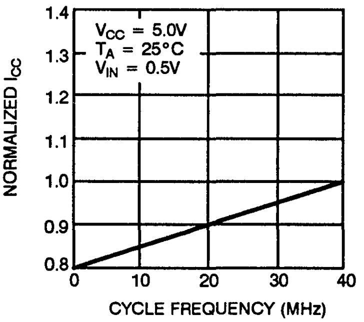
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY6116-35PC	P11	Commercial
	CY6116-35DC	D12	
	CY6116-35LC	L64	
	CY6116-35DMB	D12	Military
	CY6116-35LMB	L64	
45	CY6116-45PC	P11	Commercial
	CY6116-45DC	D12	
	CY6116-45LC	L64	
	CY6116-45DMB	D12	Military
	CY6116-45LMB	L64	
55	CY6116-55PC	P11	Commercial
	CY6116-55DC	D12	
	CY6116-55LC	L64	
	CY6116-55DMB	D12	Military
	CY6116-55LMB	L64	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY6117-35LMB	L55	Military
45	CY6117-45LMB	L55	Military
55	CY6117-55LMB	L55	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00055-C

CYPRESS SEMICONDUCTOR

CY6116A

2048 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **20 ns**
- **Low active power**
  - **550 mW**
- **Low standby power**
  - **110 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY6116A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$), and three-state drivers. The CY6116A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

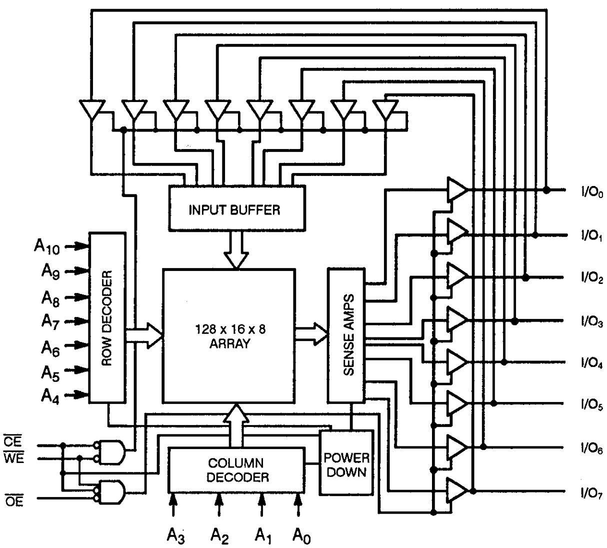
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 thorugh A_{10}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of teh memeory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The CY6116A utilizes a die coat to insure alpha immunity.

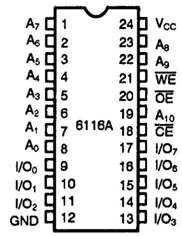
Logic Block Diagram



6116A-1

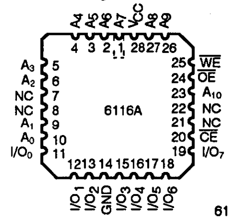
Pin Configurations

DIP/SOJ
Top View



6116A-2

LCC
Top View



6116A-3

Selection Guide

		CY6116A-20	CY6116A-25	CY6116A-35	CY6116A-45	CY6116A-55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	100	100	100	100	80
	Military		125	100	100	100
Maximum Standby Current (mA)	Commercial	40/20	20	20	20	20
	Military		40	20	20	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with
Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12) .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs
in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions			6116A–20 Min.	6116A–20 Max.	6116A–25, 35, 45 Min.	6116A–25, 35, 45 Max.	6116A–55 Min.	6116A–55 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA			2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]				-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$			–10	+ 10	–10	+ 10	–10	+ 10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled			–10	+ 10	–10	+ 10	–10	+ 10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				-300		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l			100		100		80	mA
			Mil	25				125		100	
				35, 45				100			
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ Min. Duty Cycle = 100%	Com'l			40		20		20	mA
			Mil	25				40		20	
				35, 45, 55				100			
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ – 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq$ 0.3V	Com'l			20		20		20	mA
			Mil					20		20	

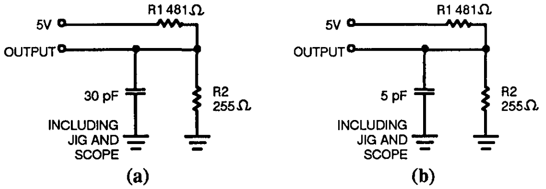
Capacitance[5]

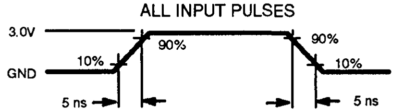
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

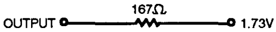
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = –3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



6116A-4

6116A-5

Switching Characteristics Over the Operating Range[2, 6]

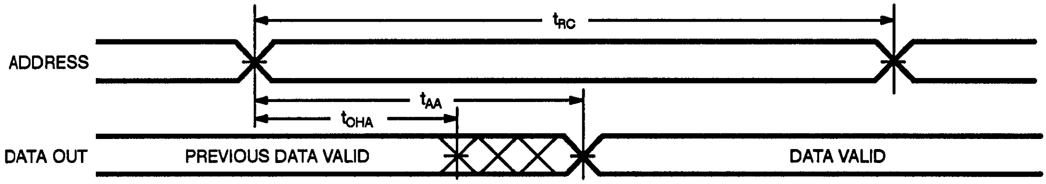
Parameters	Description	6116A-20		6116A-25		6116A-35		6116A-45		6116A-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	20		25		35		45		55		ns
t_{AA}	Address to Data Valid		20		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		20		25		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		12		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		8		10		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		8		10		15		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		20		25		25	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	20		20		25		40		50		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	15		20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	15		20		25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		20		20		25		ns
t_{SD}	Data Set-Up to Write End	10		10		15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		7		7		10		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

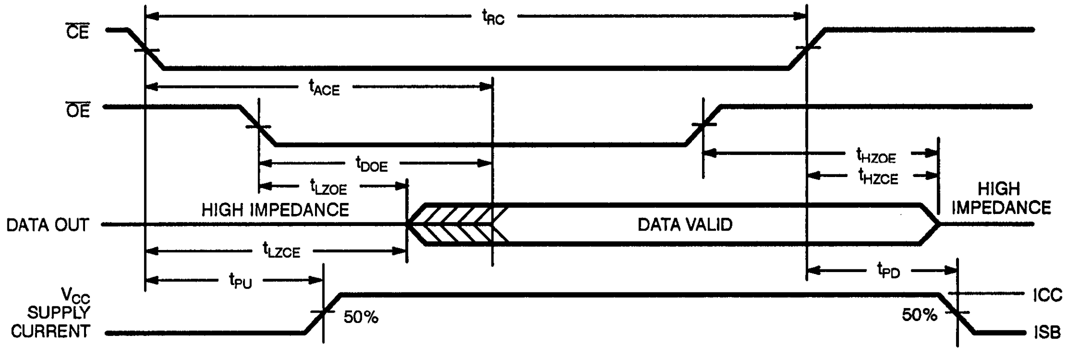
Switching Waveforms

Read Cycle No. 1[10, 11]



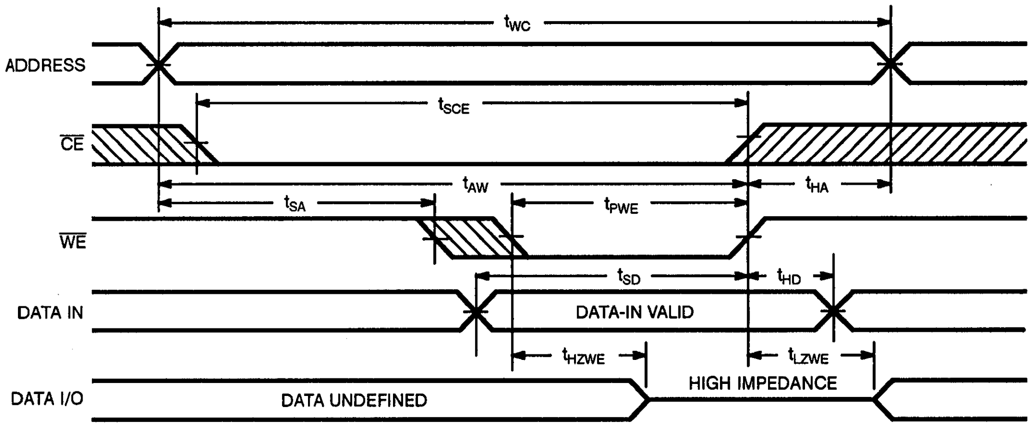
6116A-6

Read Cycle No. 2[10, 12]



6116A-7

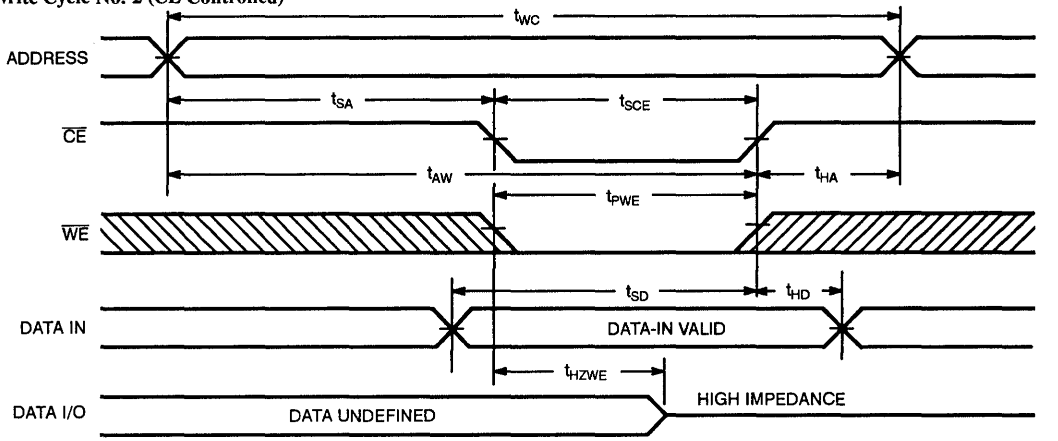
Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) [9, 13]



6116A-8

Switching Waveforms (continued)

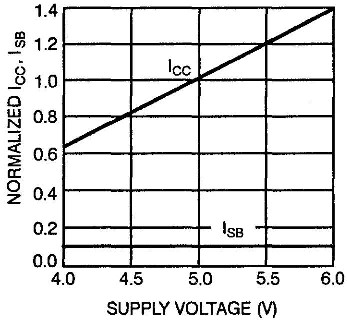
Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 13, 14]



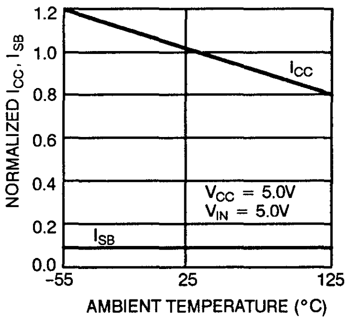
6116A-9

Typical DC and AC Characteristics

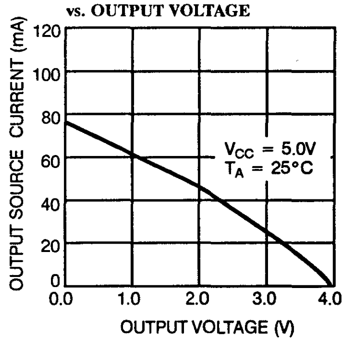
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



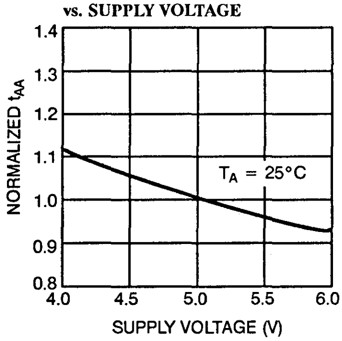
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



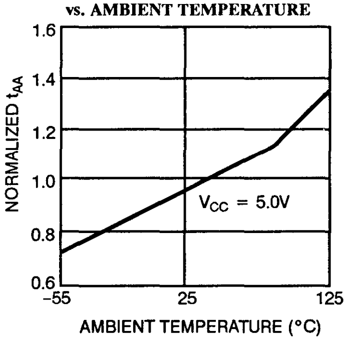
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



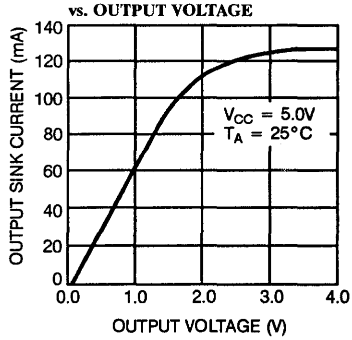
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

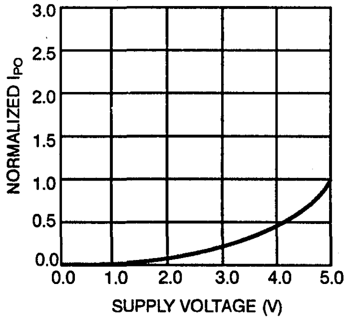


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

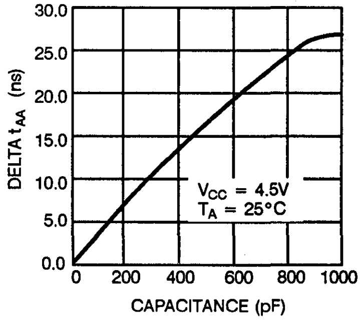


Typical DC and AC Characteristics (continued)

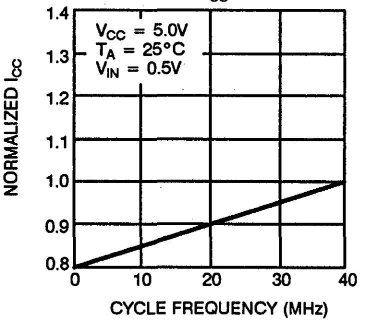
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY6116A-20PC	P11	Commercial
	CY6116A-20DC	D12	
25	CY6116A-25PC	P11	Commercial
	CY6116A-25DC	D12	
	CY6116A-25LC	L64	
	CY6116A-25DMB	D12	Military
	CY6116A-25LMB	L64	
35	CY6116A-35PC	P11	Commercial
	CY6116A-35DC	D12	
	CY6116A-35LC	L64	
	CY6116A-35DMB	D12	Military
	CY6116A-35LMB	L64	
45	CY6116A-45PC	P11	Commercial
	CY6116A-45DC	D12	
	CY6116A-45LC	L64	
	CY6116A-45DMB	D12	Military
	CY6116A-45LMB	L64	
55	CY6116A-55PC	P11	Commercial
	CY6116A-55DC	D12	
	CY6116A-55LC	L64	
	CY6116A-55DMB	D12	Military
	CY6116A-55LMB	L64	

2

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00105

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **15 ns (commercial)**
  - **25 ns (military)**
- **Low power**
  - **330 mW (commercial)**
  - **495 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance, both commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL-compatible inputs and outputs**

Functional Description

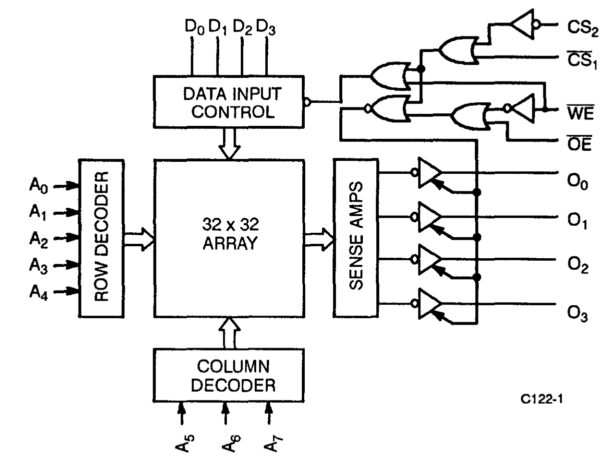
The CY7C122 is a high-performance CMOS static RAM organized as 256 words by 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS}_1$) and write enable ($\overline{WE}$) inputs are LOW and the chip select two (CS_2) input is HIGH, the information on the four data inputs (D_0 to D_3) is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select one ($\overline{CS}_1$) input is LOW, the chip select two input (CS_2) and write enable ($\overline{WE}$) inputs are HIGH, and the output enable ($\overline{OE}$) input is LOW. The information stored in the addressed word is read out on the four non-inverting outputs (O_0 to O_3).

The outputs of the memory go to an active high-impedance state whenever chip select one ($\overline{CS}_1$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

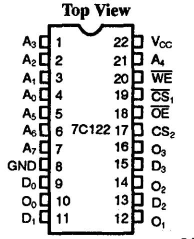
Logic Block Diagram



C122-1

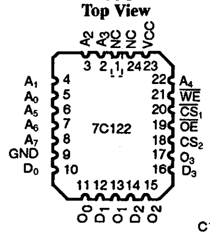
Pin Configurations

DIP
Top View



C122-2

LCC
Top View



C122-3

Selection Guide

		7C122-15	7C122-25	7C122-35
Maximum Access Time (ns)	Commercial	15	25	35
	Military		25	35
Maximum Operating Current (mA)	Commercial	90	60	60
	Military		90	90

2

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 8) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C122-15 Min.	7C122-15 Max.	7C122-25 7C122-35 Min.	7C122-25 7C122-35 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level			2.1	V_{CC}	2.1	V_{CC}	V
V_{IL}	Input LOW Level			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$			10		10	V
V_{CD}	Input Diode Clamp Voltage				Note 3		Note 3	V
I_{OZ}	Output Current (High Z)	$V_{OL} \leq V_{OUT} \leq V_{OH}$, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND	Commercial		−70		−70	mA
			Military		−80		−80	mA
I_{OS}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90		60	mA
			Military				90	mA

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	pF

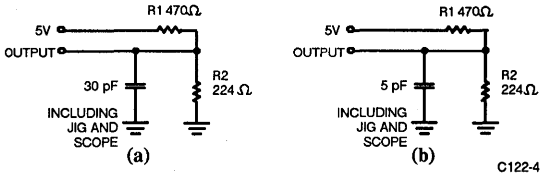
Logic Table[6]

Inputs					Outputs	Mode
$\overline{OE}$	$\overline{CS}_1$	CS_2	$\overline{WE}$	$D_0 - D_3$		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	$O_0 - O_3$	Read Stored Data
X	L	H	L	L	High Z	Write “0”
X	L	H	L	H	High Z	Write “1”
H	L	H	H	X	High Z	Output Disabled

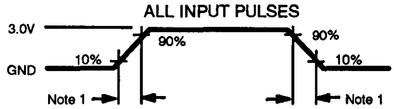
Notes:

1. T_A is the “instant on” case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The CMOS process does not provide a clamp diode. However, the CY7C122 is insensitive to −3V DC input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
4. For test purposes, not more than 1 output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. H = HIGH Voltage, L = LOW Voltage, X = Don’t Care, and High Z = High-Impedance

AC Test Loads and Waveforms

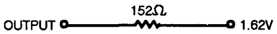


C122-4



C122-5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[7, 8]

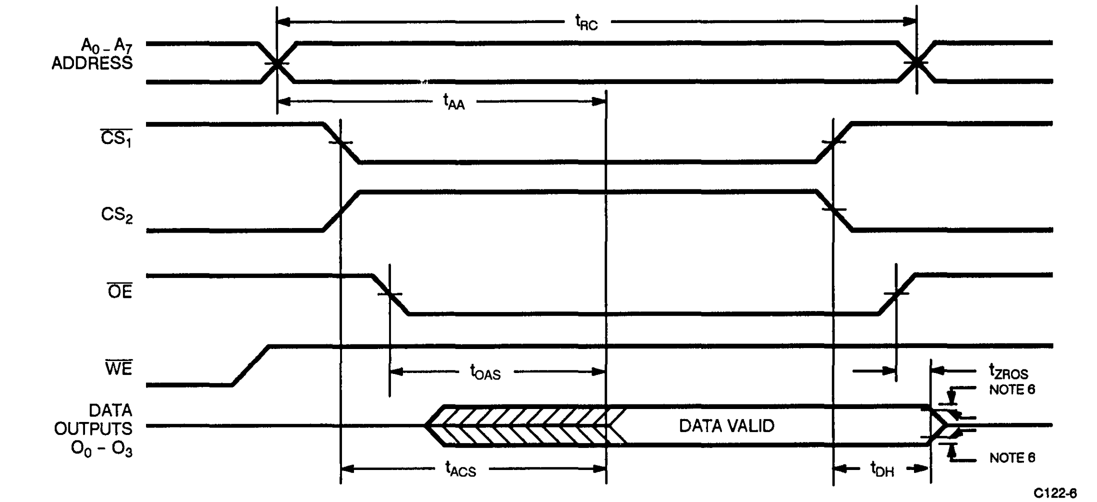
Parameters	Description	7C122-15		7C122-25		7C122-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		25		35		ns
t_{ACS}	Chip Select Time		8		15		25	ns
t_{ZRCS}	Chip Select to High Z[9]		12		20		30	ns
t_{AOS}	Output Enable Time		8		15		25	ns
t_{ZROS}	Output Enable to High Z[8]		12		20		30	ns
t_{AA}	Address Access Time		15		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	15		25		35		ns
t_{ZWS}	Write Disable to High Z[8]		12		20		30	ns
t_{WR}	Write Recovery Time		12		20		25	ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width[6]	11		15		25		ns
t_{WSD}	Data Set-Up Time Prior to Write	0		5		5		ns
t_{WHD}	Data Hold Time After Write	2		5		5		ns
t_{WSA}	Address Set-Up Time[6]	0		5		10		ns
t_{WHA}	Address Hold Time	4		5		5		ns
t_{WSCS}	Chip Select Set-Up Time	0		5		5		ns
t_{WHCS}	Chip Select Hold Time	2		5		5		ns

Notes:

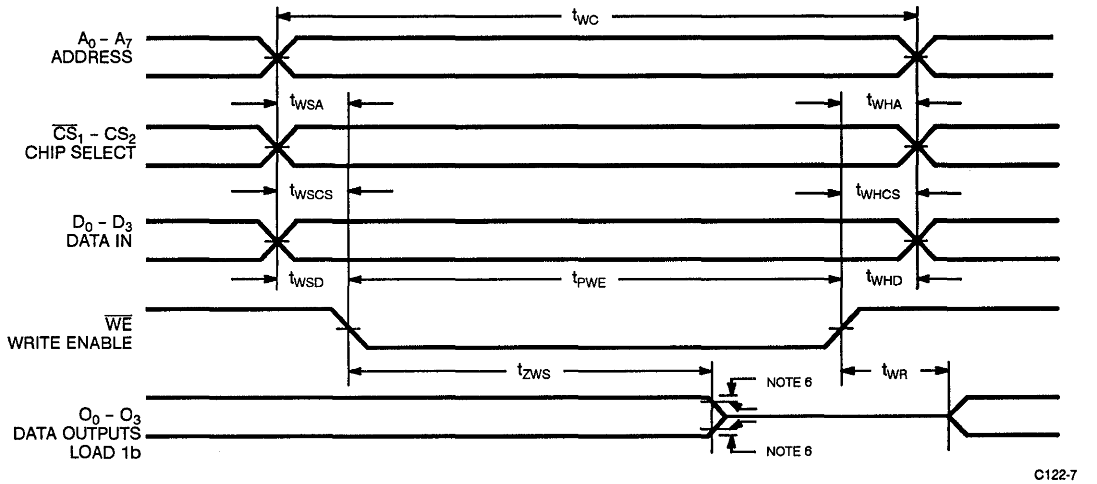
7. t_W measured at t_{WSA} = min.; t_{WSA} measured at t_W = min.
8. Test conditions assume signal transition times of 5 ns or less for the -15 product and 10 ns or less for the -25 and -35 product. Timing reference levels of 1.5V.
9. Transition is measured at steady state HIGH level -500 mV or steady state LOW level +500 mV on the output from 1.5V level on the input with load as shown in part (b) of AC Test Loads.

Switching Waveforms

Read Cycle [10]



Write Cycle [9, 11]

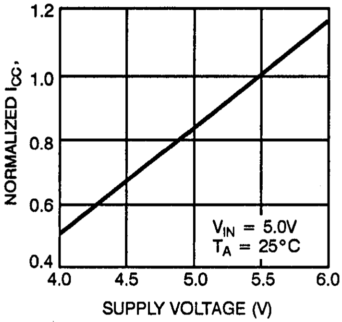


Notes:

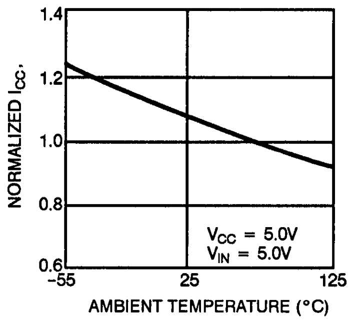
10. Measurements are referenced to 1.5V unless otherwise stated.
11. The timing diagram represents one solution that results in an optimum cycle time. Timing may be changed in varous applications as long as the worst-case limits are not violated.

Typical DC and AC Characteristics

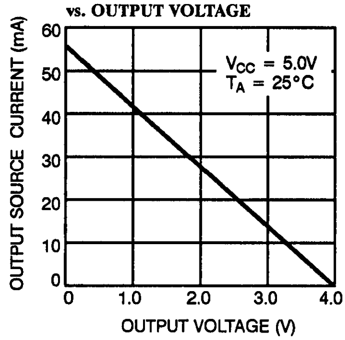
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



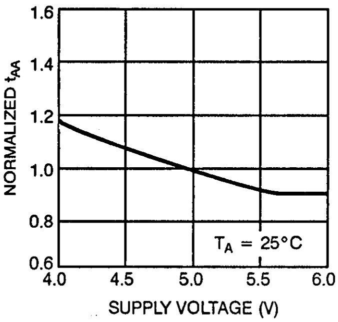
NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE



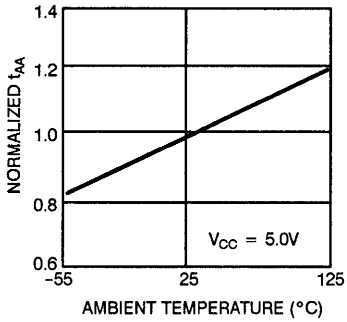
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



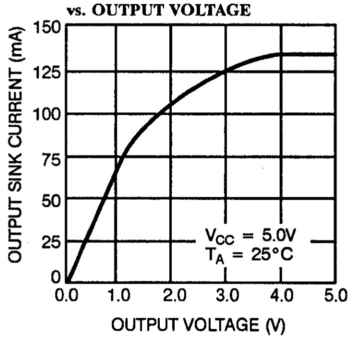
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



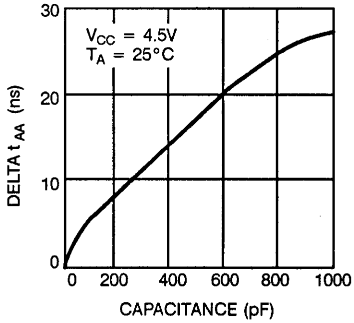
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



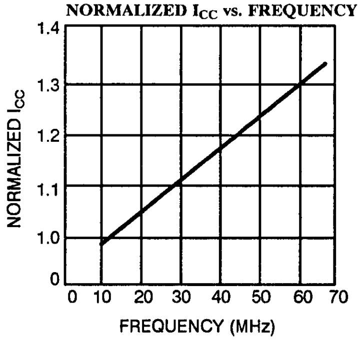
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



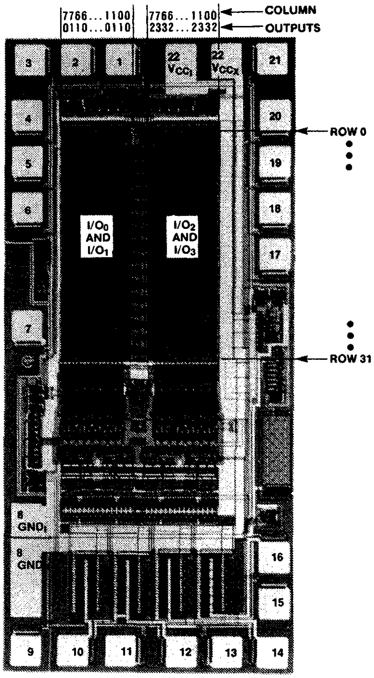
ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



Bit Map



Address Designators

Address Name	Address Function	Pin Number
A_0	AX0	4
A_1	AX1	3
A_2	AX2	2
A_3	AX3	1
A_4	AX4	21
A_5	AY0	5
A_6	AY1	6
A_7	AY2	7

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C122-15PC	P7	Commercial
	CY7C122-15DC	D8	
25	CY7C122-25PC	P7	Commercial
	CY7C122-25DC	D8	
	CY7C122-25LC	L53	
	CY7C122-25DMB	D8	Military
35	CY7C122-35PC	P7	Commercial
	CY7C122-35DC	D8	
	CY7C122-35LC	L53	
	CY7C122-35DMB	D8	Military
	CY7C122-35LMB	L53	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{OCS}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{WR}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{WSD}	7, 8, 9, 10, 11
t_{WHD}	7, 8, 9, 10, 11
t_{WSA}	7, 8, 9, 10, 11
t_{WHA}	7, 8, 9, 10, 11
t_{WSCS}	7, 8, 9, 10, 11
t_{WHCS}	7, 8, 9, 10, 11

Document #: 38-00025-B

CYPRESS SEMICONDUCTOR

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 7 ns (commercial)**
  - **— 10 ns (military)**
- **Low power**
  - **— 660 mW (commercial)**
  - **— 825 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance both commercial and military**
- **TTL-compatible inputs and outputs**
- **24 pin**
- **300-mil package**

Functional Description

The CY7C123 is a high-performance CMOS static RAM organized as 256 words by 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

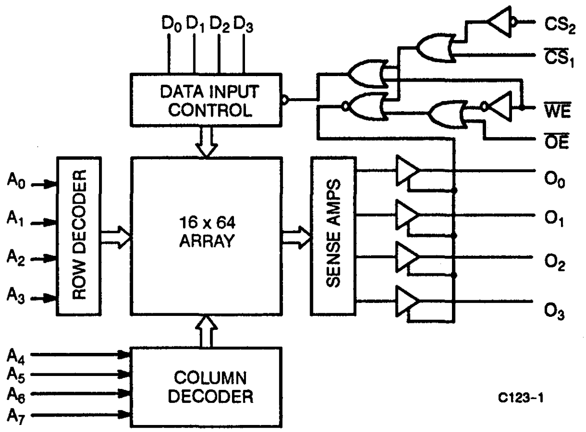
Writing to the device is accomplished when the chip select one ($\overline{CS}_1$) and write enable ($\overline{WE}$) inputs are both LOW and the chip select two input is HIGH. Data on the four data inputs (D_0 through D_3) is written into the memory location specified on the address pins (A_0 through A_7). The outputs are preconditioned so that the write data is present at the outputs when the write cycle is complete. This precondition operation ensures minimum write recovery times by eliminating the "write recovery glitch."

Reading the device is accomplished by taking the chip select one ($\overline{CS}_1$) and output enable ($\overline{OE}$) inputs LOW, while the write enable ($\overline{WE}$) and chip select two ($\overline{CS}_2$) inputs remain HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

The output pins remain in high-impedance state when chip select one ($\overline{CS}_1$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip select two ($\overline{CS}_2$) is LOW.

A die coat is used to insure alpha immunity.

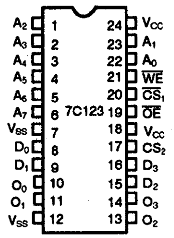
Logic Block Diagram



C123-1

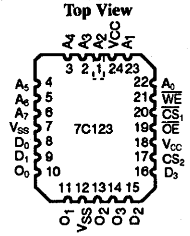
Pin Configurations

SOJ
Top View



C123-2

LCC
Top View



C123-3

Selection Guide

		7C123-7	7C123-9	7C123-10	7C123-12	7C123-15
Maximum Access Time (ns)	Commercial	7	9		12	
	Military			10	12	15
Maximum Operating Current (mA)	Commercial	120	120		120	
	Military			150	150	150

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pins 24 and 18 to Pins 7 and 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C123-7 7C123-9		7C123-10 7C123-15		7C123-12		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −5.2 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Current (High Z)	$V_{SS} \leq V_{OUT} \leq V_{CC}$, Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		120				120	mA
			Military				150		150	mA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	pF

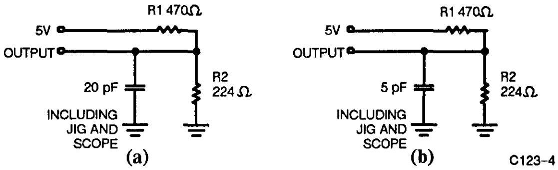
Logic Table[4]

Inputs					Outputs	Mode
$\overline{OE}$	$\overline{CS}_1$	CS_2	$\overline{WE}$	$D_0 - D_3$		
X	H	X	X	X	High Z	Not Selected
X	X	L	X	X	High Z	Not Selected
L	L	H	H	X	$O_0 - O_3$	Read Stored Data
X	L	H	L	L	High Z	Write "0"
X	L	H	L	H	High Z	Write "1"
H	L	H	H	X	High Z	Output Disabled

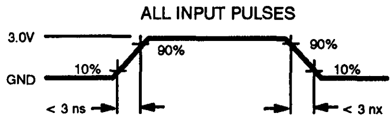
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.
4. H = High Voltage, L = Low Voltage, X = Don't Care, and High Z = High Impedance.

AC Test Loads and Waveforms



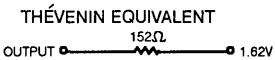
C123-4



C123-5

2

Equivalent to:



Switching Characteristics Over the Operating Range[2]

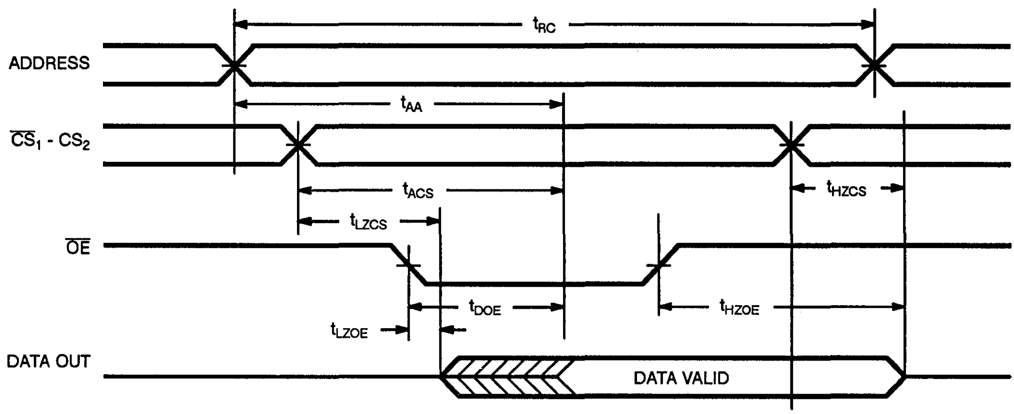
Parameters	Description	7C123-7		7C123-9		7C123-10		7C123-12		7C123-15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	7		9		10		12		15		ns
t_{AA}	Address to Data Valid		7		9		10		12		15	ns
t_{ACS}	Chip Select to Data Valid		7		8		8		8		10	ns
t_{DOE}	$\overline{\text{OE}}$ LOW to Data Valid		7		8		8		8		10	ns
t_{HZCS}	Chip Select to High Z[5, 6]		5		6		6		6.5		8	ns
t_{HZOE}	$\overline{\text{OE}}$ HIGH to High Z[4]		5		6		6		6.5		8	ns
t_{LZCS}	Chip Select to Low Z[4, 5]	2		2		2		2		2		ns
t_{LZOE}	$\overline{\text{OE}}$ LOW to Low Z[4]	2		2		2		2		2		ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	7		9		10		12		15		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z		5.5		6		6		7		8	ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z	2		2		2		2		2		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	5		6.5		7		8		11		ns
t_{SD}	Data Set-Up to Write End	5		6		7		8		11		ns
t_{HD}	Data Hold from Write End	1		1		1		1		1		ns
t_{SA}	Address Set-Up to Write Start	0.5		1		1		2		2		ns
t_{HA}	Address Hold from Write End	1.5		1.5		2		2		2		ns
t_{SCS}	$\overline{\text{CS}}$ LOW to Write End	5		6.5		7		8		11		ns
t_{AW}	Address Set-Up to Write End	5.5		7.5		8		10		13		ns

Notes:

5. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input with load shown in part (b) of AC Test Loads.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.

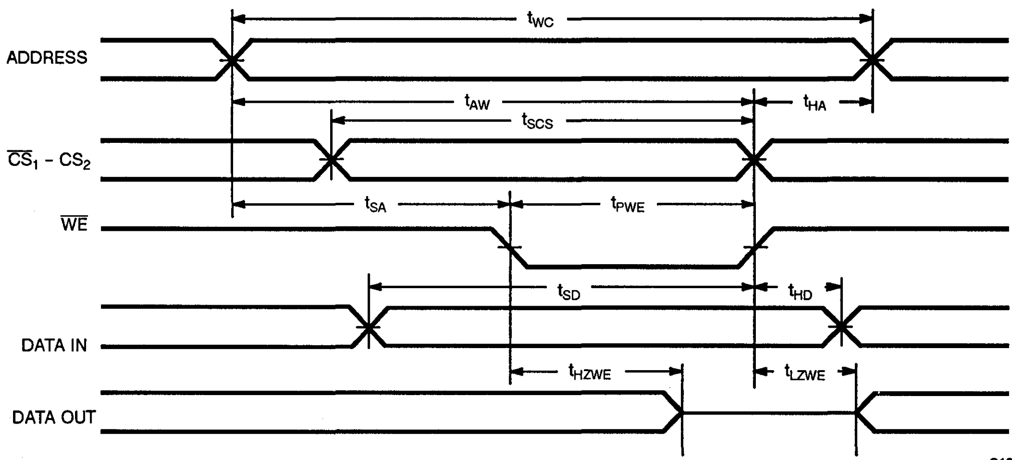
Switching Waveforms

Read Cycle [7, 8]



C123-6

Write Cycle [7, 8]

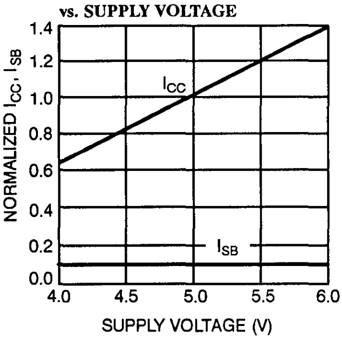


C123-7

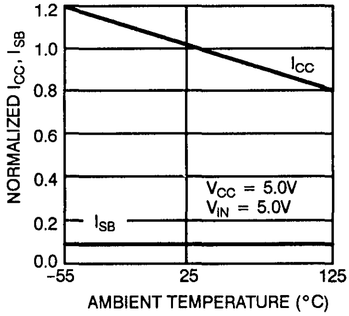
Notes:
7. Measurements are referenced to 1.5V unless otherwise stated.
8. Timing diagram represents one solution that results in an optimum cycle time. Timing may be changed in varous applications as long as the worst case limits are not violated.

Typical DC and AC Characteristics

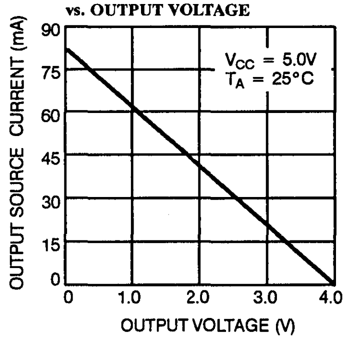
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



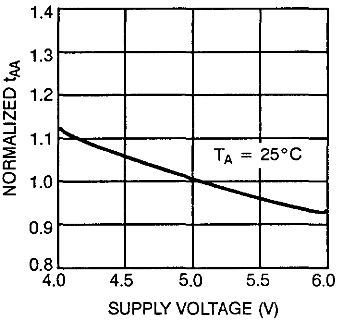
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



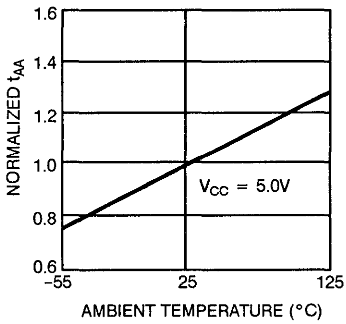
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



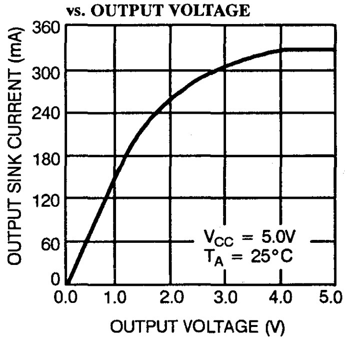
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



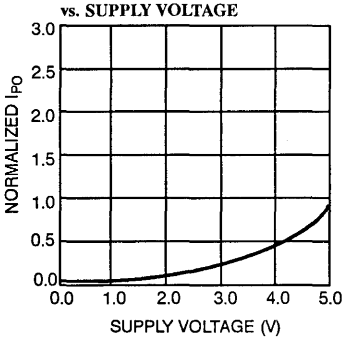
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



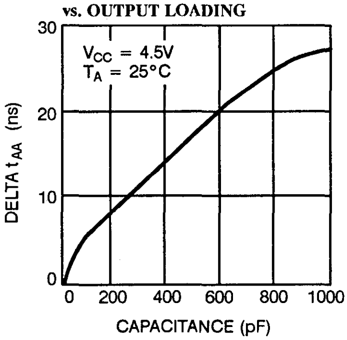
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



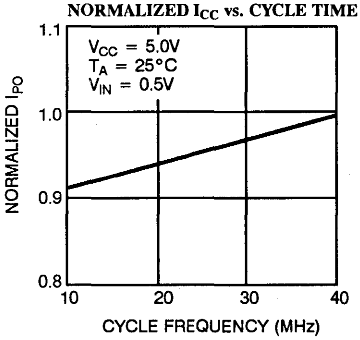
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TOTAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
7	CY7C123-7PC	P13A	Commercial
	CY7C123-7DC	D14	
	CY7C123-7LC	L53	
9	CY7C123-9PC	P13A	Commercial
	CY7C123-9DC	D14	
	CY7C123-9LC	L53	
10	CY7C123-10DMB	D14	Military
	CY7C123-10LMB	L53	
	CY7C123-10KMB	K73	
12	CY7C123-12PC	P13A	Commercial
	CY7C123-12DC	D14	
	CY7C123-12LC	L53	
	CY7C123-12DMB	D14	Military
	CY7C123-12LMB	L53	
	CY7C123-12KMB	K73	
15	CY7C123-15DMB	D14	Military
	CY7C123-15LMB	L53	
	CY7C123-15KMB	K73	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11

Document #: 38-00060-D

7C128: 11/8/89
Revision: 12/27/89

CYPRESS SEMICONDUCTOR

CY7C128

2048 x 8 Static R/W RAM

2

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - 35 ns
- Low active power
  - 660 mW (commercial)
  - 825 mW (military)
- Low standby power
  - 110 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C128 is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY7C128 has an automatic power-down feature, reducing the power consumption by 83% when deselected.

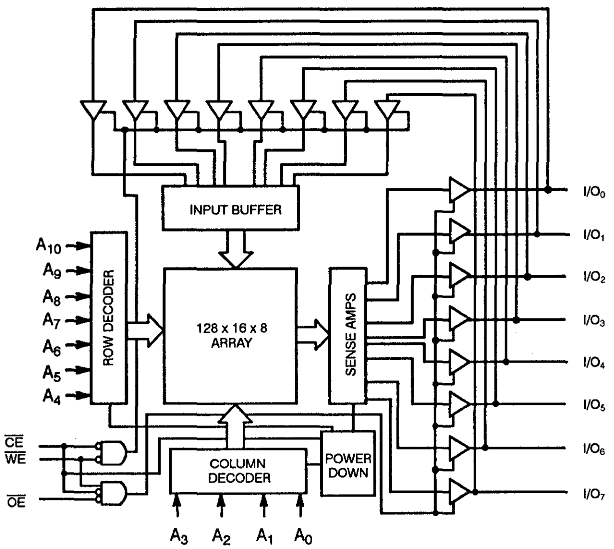
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{10}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

The I/O pins remain in high-impedance state when chip enable ($\overline{CE}$) or output enable ($\overline{OE}$) is HIGH or write enable ($\overline{WE}$) is low.

The 7C128 utilizes a die coat to ensure alpha immunity.

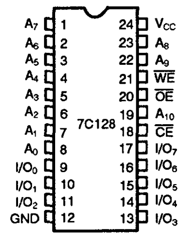
Logic Block Diagram



C128-1

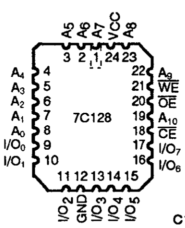
Pin Configurations

DIP/SOJ
Top View



C128-2

LCC
Top View



C128-3

Selection Guide

		7C128-35	7C128-45	7C128-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	90
	Military		130	100
Maximum Standby Current (mA)	Commercial	20	20	20
	Military		20	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions			7C128 Min.	7C128 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA			2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4	V
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$			-10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled			-40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND				-300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l	35, 45		120	mA
				55		90	
			Mil	45		130	
				55		100	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$	Com'l			20	mA
			Mil			20	

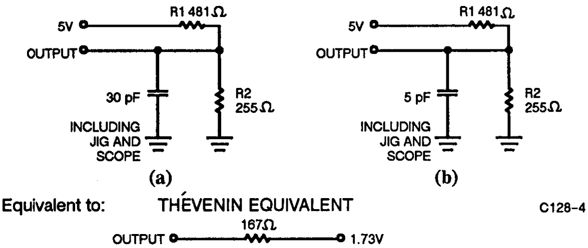
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

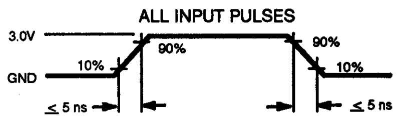
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



C128-4



C128-5

Switching Characteristics Over the Operating Range[2, 5]

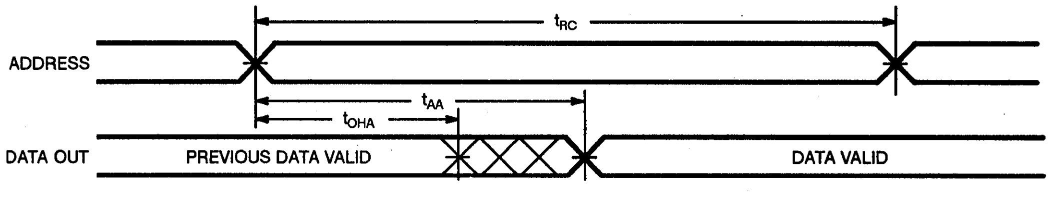
Parameters	Description	7C128-35		7C128-45		7C128-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		15		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		15		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		25		25	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		20		25		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		15		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns

Notes:

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. Data I/O pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

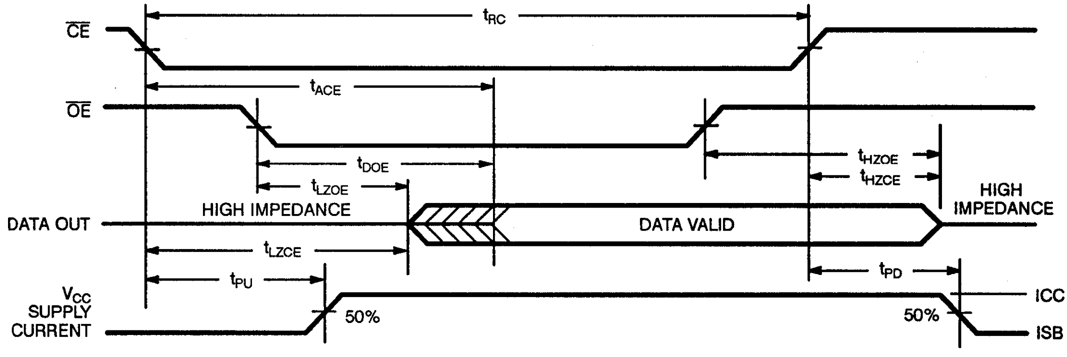
Switching Waveforms

Read Cycle No. 1[9, 10]



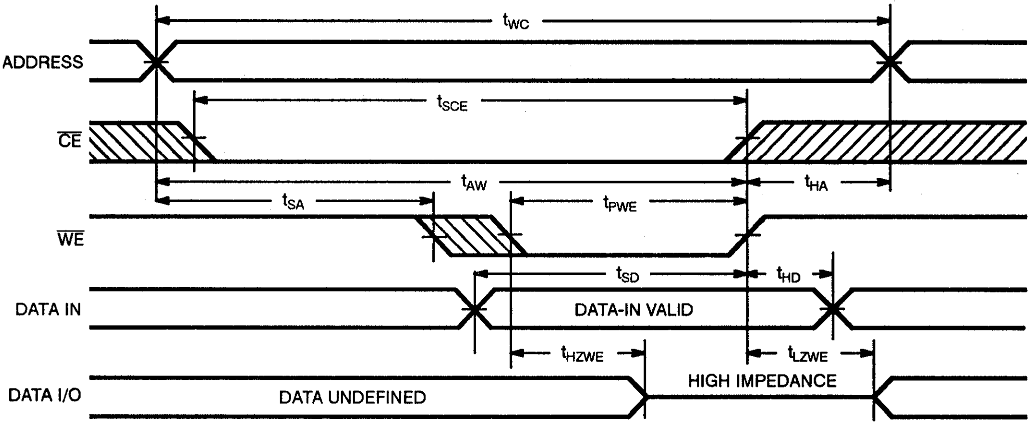
C128-6

Read Cycle No. 2[9, 11]



C128-7

Write Cycle No. 1 ($\overline{WE}$ Controlled) [8, 12]

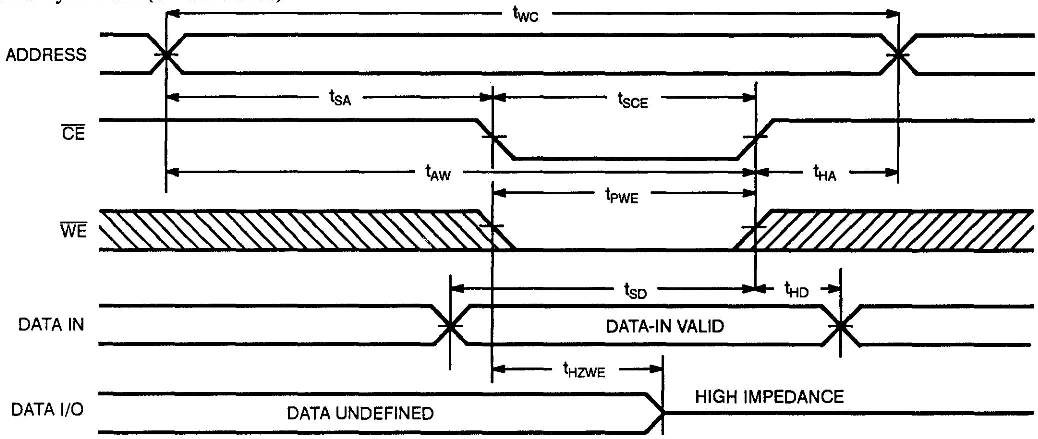


C128-8

2

Switching Waveforms (continued)

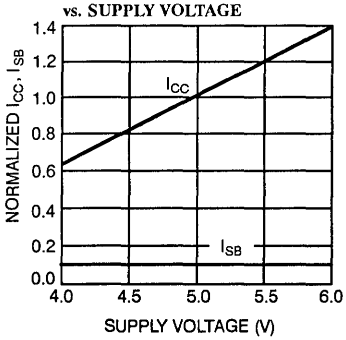
Write Cycle No. 2 ($\overline{CE}$ Controlled) [8, 12, 13]



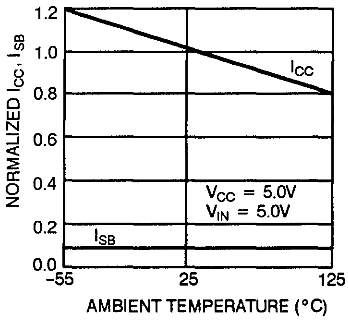
C128-9

Typical DC and AC Characteristics

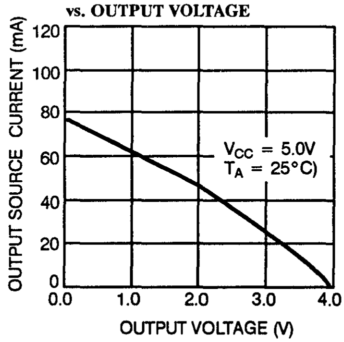
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



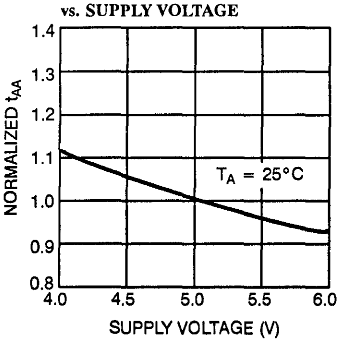
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



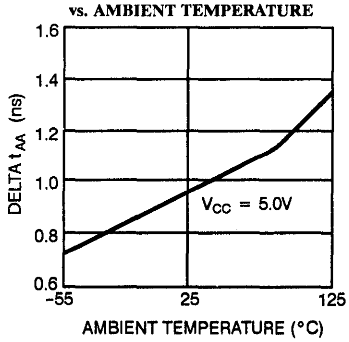
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



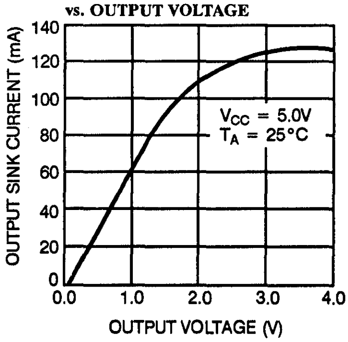
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

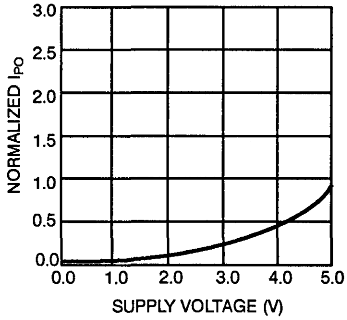


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

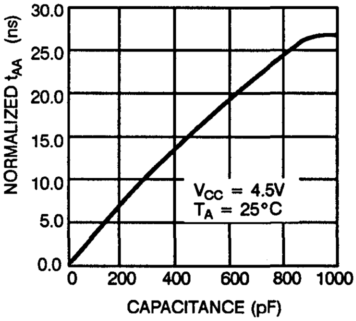


Typical DC and AC Characteristics (continued)

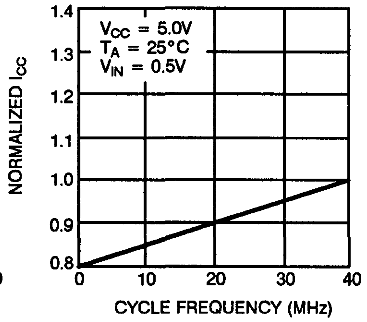
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C128-35PC	P13	Commercial
	CY7C128-35VC	V12	
	CY7C128-35DC	D14	
	CY7C128-35LC	L53	
45	CY7C128-45PC	P13	Commercial
	CY7C128-45VC	V13	
	CY7C128-45DC	D14	
	CY7C128-45LC	L53	
	CY7C128-45DMB	D14	Military
	CY7C128-45LMB	L53	
	CY7C128-45KMB	K73	
55	CY7C128-55PC	P13	Commercial
	CY7C128-55VC	V13	
	CY7C128-55DC	D14	
	CY7C128-55LC	L53	
	CY7C128-55DMB	D14	Military
	CY7C128-55LMB	L53	
	CY7C128-55KMB	K73	

2

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00026-C

CY7C128A

CYPRESS SEMICONDUCTOR

2048 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **15 ns**
- **Low active power**
  - **440 mW (commercial)**
  - **550 mW (military)**
- **Low standby power**
  - **110 mW**
- **SOJ package**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **V_{IH} of 2.2V**

Functional Description

The CY7C128A is a high-performance CMOS static RAM organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$), and active LOW output enable ($\overline{OE}$) and three-state drivers. The CY7C128A has an automatic power-down feature, reducing the power consumption by 83% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW.

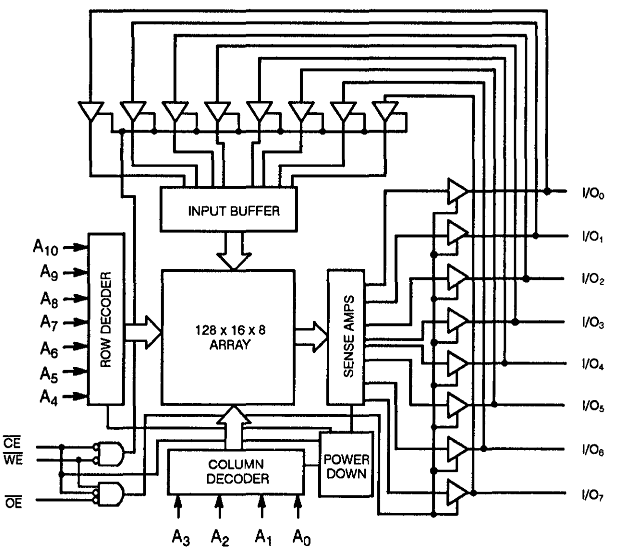
Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{10}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight I/O pins.

The I/O pins remain in high-impedance state when chip enable ($\overline{CE}$) or output enable ($\overline{OE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

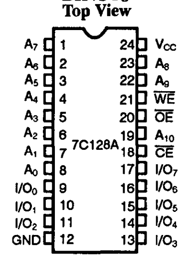
The 7C128A utilizes a die coat to insure alpha immunity.

Logic Block Diagram

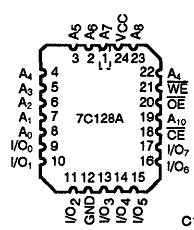


C128A-1

Pin Configurations



C128A-2



C128A-3

Selection Guide

		7C128A-15	7C128A-20	7C128A-25	7C128A-35	7C128A-45	7C128A-55
Maximum Access Time (ns)		15	20	25	35	45	55
Maximum Operating Current (mA)	Commercial	120	100	100	100	100	80
	Military		125	125	100	100	100
Maximum Standby Current (mA)	Commercial	40/40	40/20	20	20	20	20
	Military		40/20	40	20	20	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C128A-15 Min.	7C128A-15 Max.	7C128A-20 Min.	7C128A-20 Max.	7C128A-25, 35, 45 Min.	7C128A-25, 35, 45 Max.	7C128A-55 Min.	7C128A-55 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−0.5	0.8	−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−300		−300		−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		120		100		100		80	mA
			Mil 25				125		125		100	
			Mil 35,45				125		100		100	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Com'l		40		40		20		20	mA
			Mil 25				40		40		20	
			Mil 35,45				40		20		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Com'l		40		20		20		20	mA
			Mil				20		20		20	

Notes:

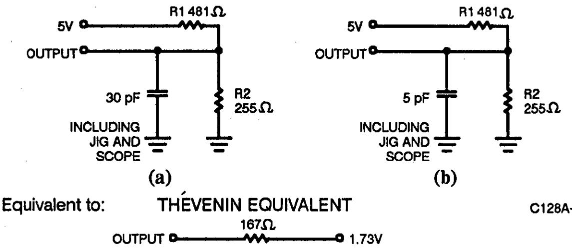
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance[5]

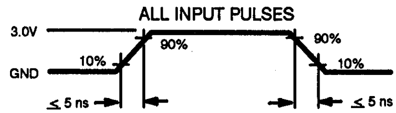
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



C128A-4



C128A-5

Switching Characteristics Over the Operating Range[2,6]

Parameters	Description	7C128A-15		7C128A-20		7C128A-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	15		20		25		ns
t_{AA}	Address to Data Valid		15		20		25	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		8		8		10	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		8		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	15		20		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		ns
t_{AW}	Address Set-Up to Write End	12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		7		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns

Switching Characteristics Over the Operating Range (continued)

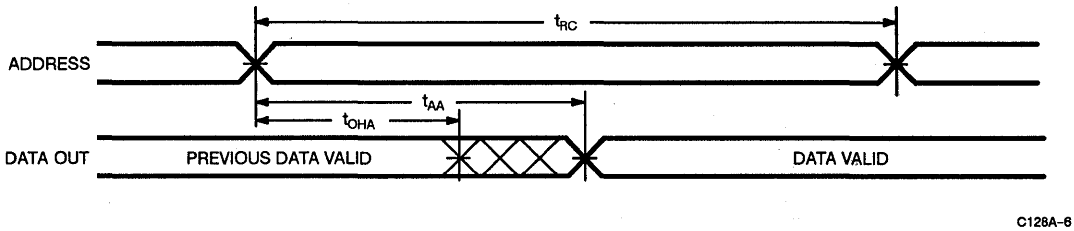
Parameters	Description	7C128A-35		7C128A-45		7C128A-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		15		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		25		25	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	25		40		50		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	25		30		40		ns
t_{AW}	Address Set-Up to Write End	25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		20		25		ns
t_{SD}	Data Set-Up to Write End	15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		10		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns

Notes:

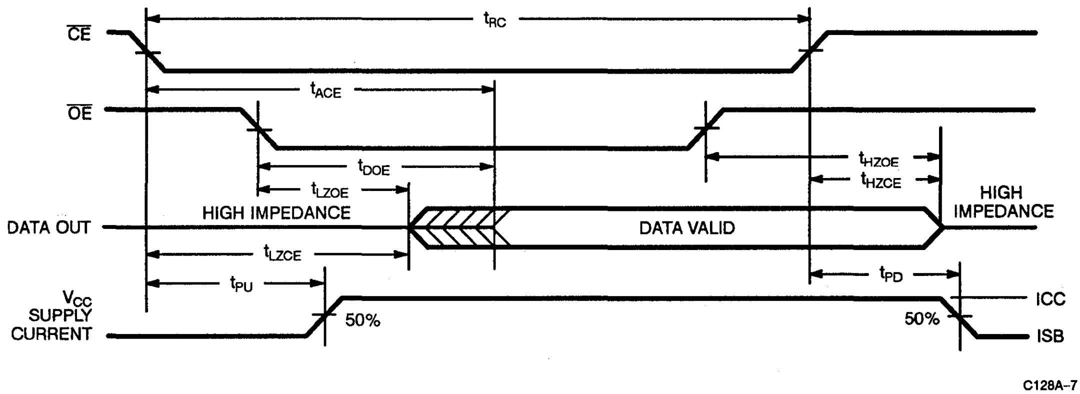
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O pins enter high-impedance state, as shown, when $\overline{OE}$ is held LOW during write.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

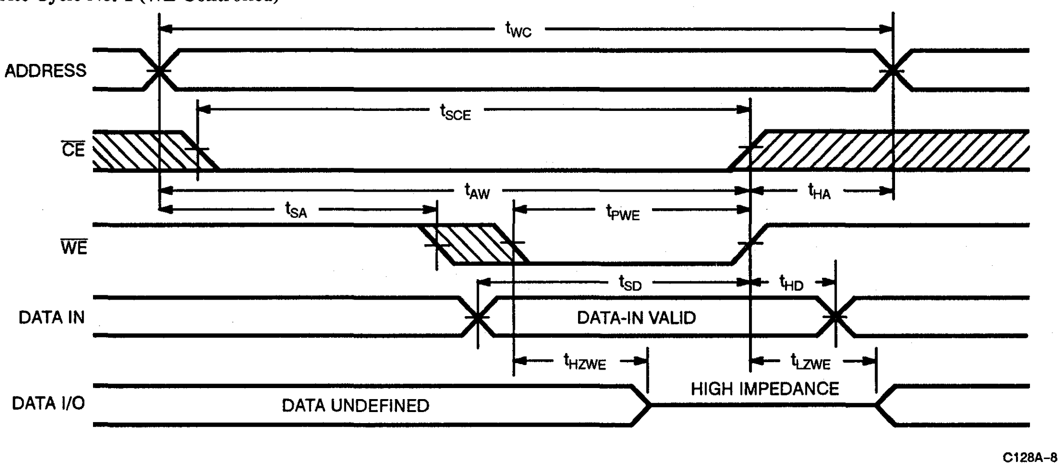
Read Cycle No. 1[10,11]



Read Cycle No. 2[10, 12]

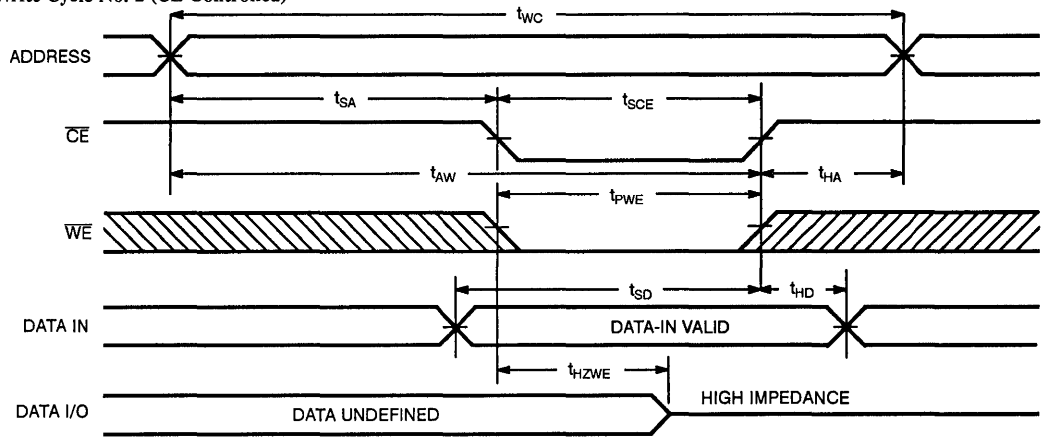


Write Cycle No. 1 ($\overline{WE}$ Controlled) [9, 13]



Switching Waveforms (continued)

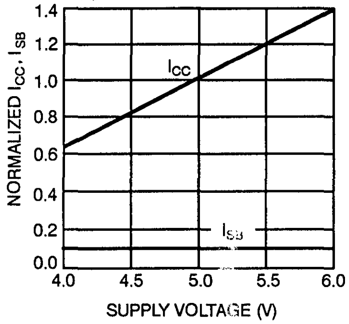
Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 13, 14]



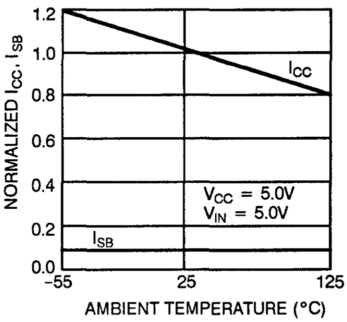
C128A-9

Typical DC and AC Characteristics

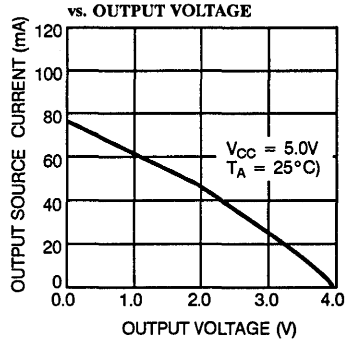
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



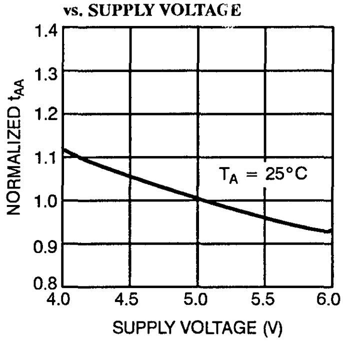
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



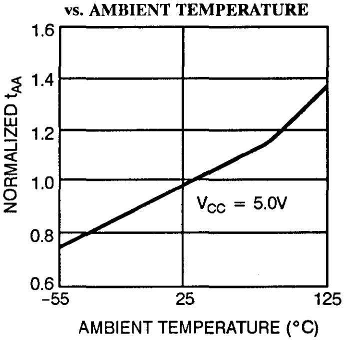
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



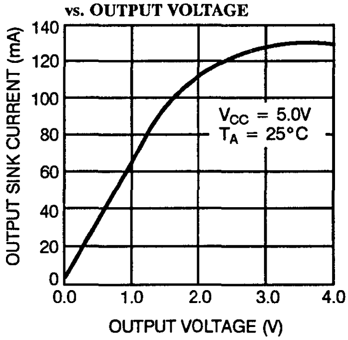
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

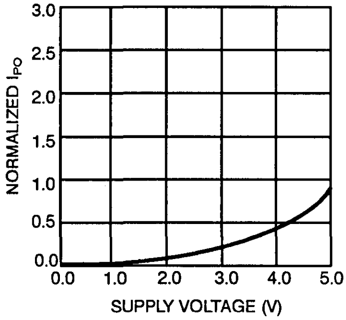


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

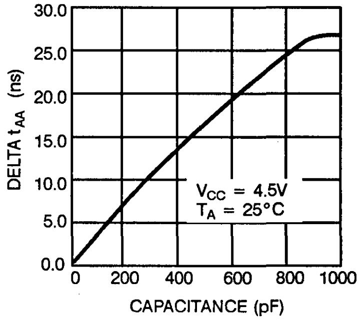


Typical DC and AC Characteristics (continued)

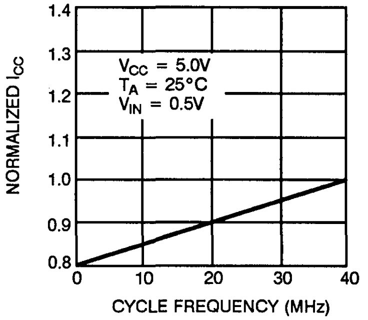
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C128A-15PC	P13	Commercial
	CY7C128A-15VC	V12	
	CY7C128A-15DC	D14	
	CY7C128A-15LC	L53	
20	CY7C128A-20PC	P13	Commercial
	CY7C128A-20VC	V13	
	CY7C128A-20DC	D14	
	CY7C128A-20LC	L53	
	CY7C128A-20DMB	D14	Military
	CY7C128A-20LMB	L53	
	CY7C128A-20KMB	K73	
25	CY7C128A-25PC	P13	Commercial
	CY7C128A-25VC	V13	
	CY7C128A-25DC	D14	
	CY7C128A-25LC	L53	
	CY7C128A-25DMB	D14	Military
	CY7C128A-25LMB	L53	
	CY7C128A-25KMB	K73	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C128A-35PC	P13	Commercial
	CY7C128A-35VC	V12	
	CY7C128A-35DC	D14	
	CY7C128A-35LC	L53	
	CY7C128A-35DMB	D14	Military
	CY7C128A-35LMB	L53	
	CY7C128A-35KMB	K73	
45	CY7C128A-45PC	P13	Commercial
	CY7C128A-45VC	V13	
	CY7C128A-45DC	D14	
	CY7C128A-45LC	L53	
	CY7C128A-45DMB	D14	Military
	CY7C128A-45LMB	L53	
	CY7C128A-45KMB	K73	
55	CY7C128A-55PC	P13	Commercial
	CY7C128A-55VC	V13	
	CY7C128A-55DC	D14	
	CY7C128A-55LC	L53	
	CY7C128A-55DMB	D14	Military
	CY7C128A-55LMB	L53	
	CY7C128A-55KMB	K73	

2

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00094-B

CYPRESS SEMICONDUCTOR

1024 x 8 Dual-Port Static RAM

Features

- 0.8-micron CMOS for optimum speed/power
- Automatic power-down
- TTL-compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- Master CY7C130/CY7C131 easily expands data bus width to 16 or more bits using SLAVE CY7C140/CY7C141
- $\overline{\text{BUSY}}$ output flag on CY7C130/CY7C131; $\overline{\text{BUSY}}$ input on CY7C140/CY7C141
- $\overline{\text{INT}}$ flag for port-to-port communication

Functional Description

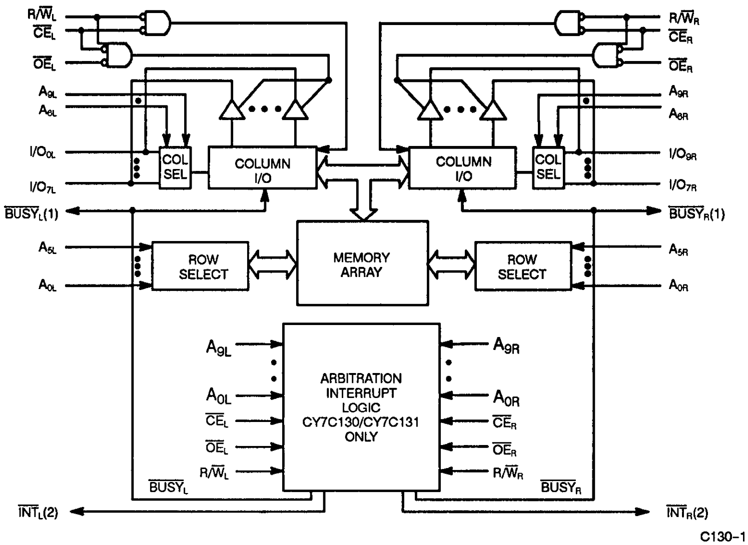
The CY7C130/CY7C131/CY7C140/CY7C141 are high-speed CMOS 1K by 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C130/CY7C131 can be utilized as either a standalone 8-bit dual-port static RAM or as a master dual-port RAM in conjunction with the CY7C140/CY7C141 slave dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$), and output enable ($\overline{\text{OE}}$). Two flags are provided on each port, $\overline{\text{BUSY}}$ and $\overline{\text{INT}}$. $\overline{\text{BUSY}}$ signals that the port is trying to access the same location currently being accessed by the other port. $\overline{\text{INT}}$ is an interrupt flag indicating that data has been placed in a unique location by the other port. An automatic power-down feature is controlled independently on each port by the chip enable ($\overline{\text{CE}}$) pin.

The CY7C130 and CY7C140 are available in both 48-pin DIP and 48-pin LCC. The CY7C131 and CY7C141 are available in both 52-pin LCC and PLCC.

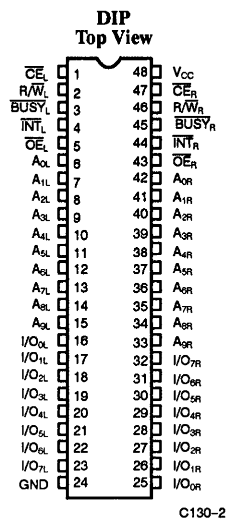
A die coat is used to insure alpha immunity.

Logic Block Diagram



C130-1

Pin Configurations

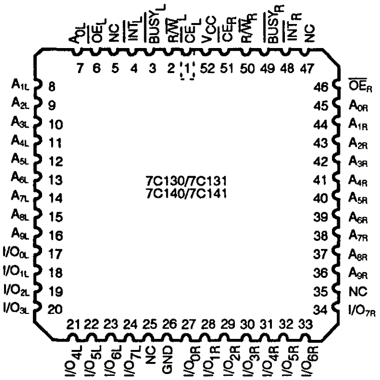


C130-2

Notes:
1. CY7C130/CY7C131 (Master): $\overline{\text{BUSY}}$ is open drain output and requires pull-up resistor. CY7C140/CY7C141 (Slave): $\overline{\text{BUSY}}$ is input.
2. Open drain outputs: pull-up resistor required.

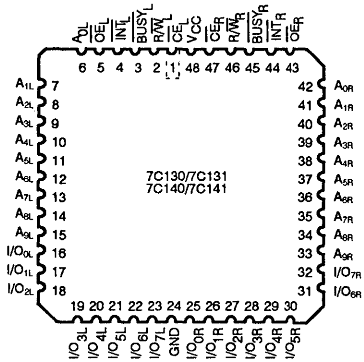
Pin Configurations (continued)

52-Pin LCC/PLCC
Top View



C130-3

48-Pin LCC
Top View



C130-4

2

Selection Guide

		7C130-25 7C131-25 7C140-25 7C141-25	7C130-35 7C131-35 7C140-35 7C141-35	7C130-45 7C131-45 7C140-45 7C141-45	7C130-55 7C131-55 7C140-55 7C141-55
Maximum Access Time (ns)		25	35	45	55
Maximum Operating Current (mA)	Commercial	170	120	90	90
	Military		170	120	120
Maximum Standby Current (mA)	Commercial	65	45	35	35
	Military		65	45	45

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... − 65°C to + 150° °C

Ambient Temperature with Power Applied .... − 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) .... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... − 0.5V to + 7.0V

DC Input Voltage .... − 3.5V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[3]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameters	Description	Test Conditions		7C130-25 7C131-25 7C140-25 7C141-25 Min.	Max.	7C130-35 7C131-35 7C140-35 7C141-35 Min.	Max.	7C130-45, 55 7C131-45, 55 7C140-45, 55 7C141-45, 55 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[5]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-5	+5	-5	+5	-5	+5	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		-5	+5	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND			-350		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE} = V_{IL}$ Outputs Open f = f_{MAX}	Com'l		170		120		90	mA
			Mil				170		120	mA
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ f = f_{MAX}	Com'l		65		45		35	mA
			Mil				65		45	mA
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open f = f_{MAX}	Com'l		115		90		75	mA
			Mil				115		90	mA
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0	Com'l		15		15		15	mA
			Mil				15		15	mA
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Ports Outputs Open, f = f_{MAX}	Com'l		105		85		70	mA
			Mil				105		85	mA

Shaded area contains preliminary information.

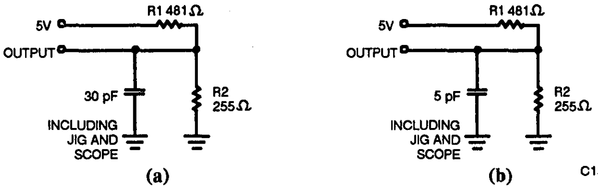
Capacitance[7]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

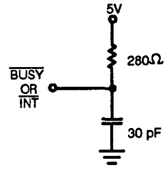
Notes:

3. T_A is the "instant on" case temperature
4. See the last page of this specification for Group A subgroup testing information.
5. $\overline{BUSY}$ and $\overline{INT}$ pins only.
6. Duration of the short circuit should not exceed 30 seconds.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OI}/I_{OH}, and 30-pF load capacitance.
9. t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
11. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referencd to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms

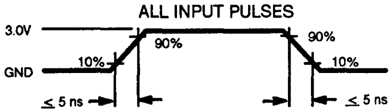


C130-5



BUSY Output Load
(CY7C130/CY7C131 ONLY)

Equivalent to:



C130-6

Switching Characteristics Over the Operating Range[4, 8]

Parameters	Description	7C130-25 7C131-25 7C140-25 7C141-25		7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9]		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[10]	5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		35		35		35	ns
WRITE CYCLE[11]										
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ HIGH to High Z		15		20		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		ns

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range[4, 8] (Continued)

Parameters	Description	7C130-25 7C131-25 7C140-25 7C141-25		7C130-35 7C131-35 7C140-35 7C141-35		7C130-45 7C131-45 7C140-45 7C141-45		7C130-55 7C131-55 7C140-55 7C141-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
BUSY/INTERRUPT TIMING										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20			45		50		ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[12]		20		35		45		55	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		35		45		25	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[12]		20		20		25		25	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		ns
t_{WB}[13]	$\overline{WE}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	$\overline{WE}$ HIGH after $\overline{BUSY}$ HIGH	20		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 14		Note 14		Note 14		Note 14	ns
t_{WDD}	Write Pulse to Data Delay		Note 14		Note 14		Note 14		Note 14	ns
INTERRUPT TIMING										
t_{WINS}	$\overline{WE}$ to $\overline{INTERRUPT}$ Set Time		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[12]		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[12]		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[12]		25		25		35		45	ns

Shaded area contains preliminary information.

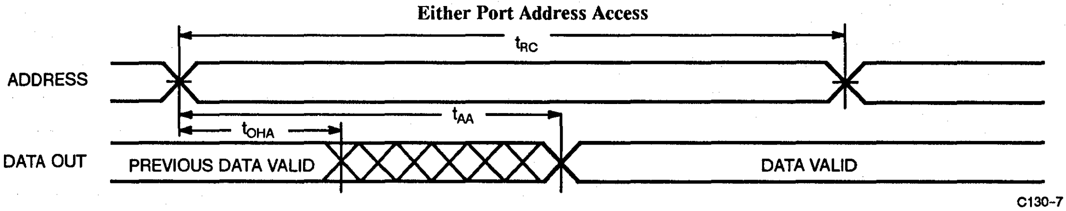
Notes:

12. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
13. CY7C140/CY7C141 only.
14. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address is toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. $\overline{WE}$ for Port B is toggled.
15. $\overline{WE}$ is HIGH for read cycle.
16. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. Data I/O pins enter high-impedance state as shown, when $\overline{OE}$ is held LOW during write.

Switching Waveforms

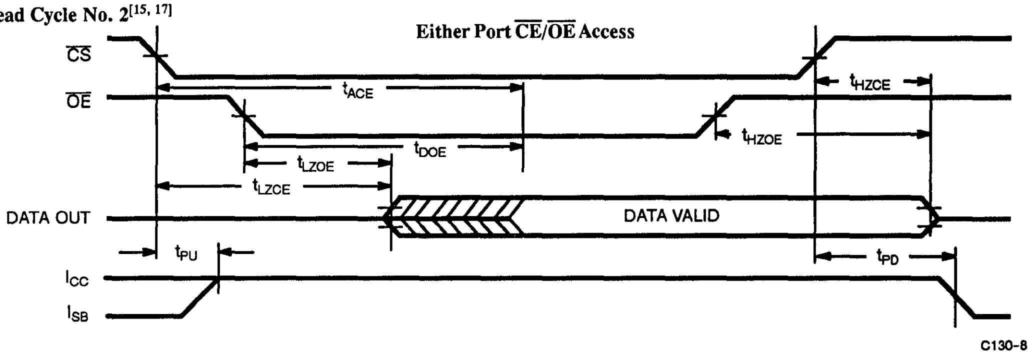
Read Cycle No. 1[15, 16]

Either Port Address Access

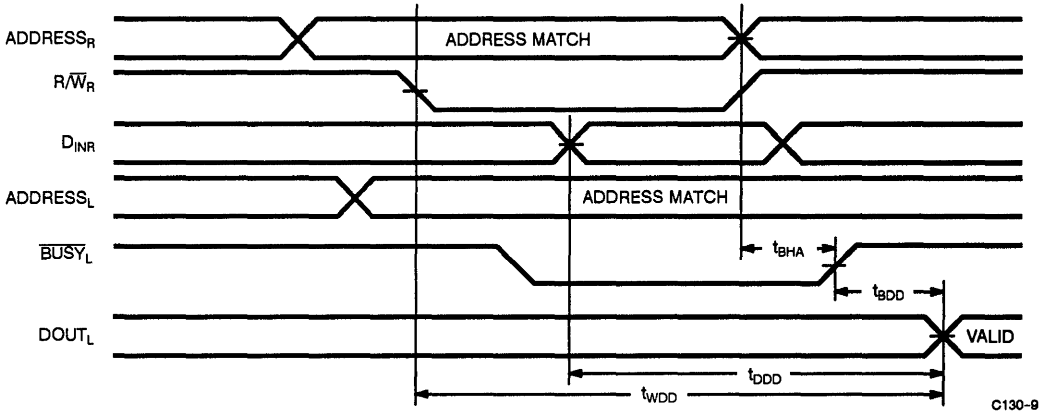


Switching Waveforms (continued)

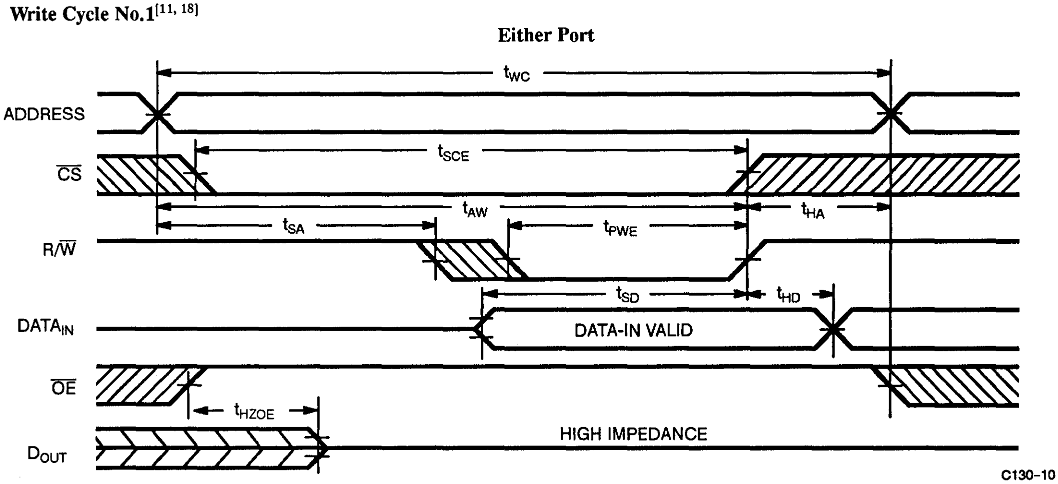
Read Cycle No. 2[15, 17]



Timing Waveform of Read with BUSY[15]

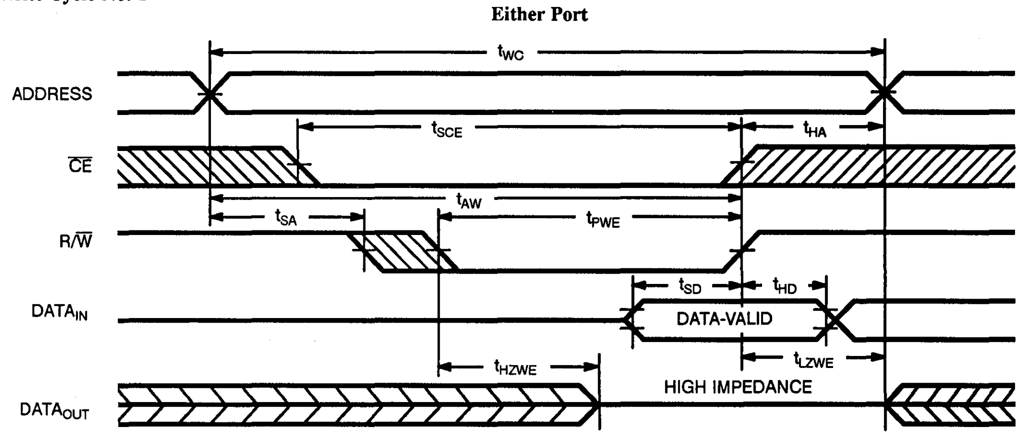


Write Cycle No.1[11, 18]



Switching Waveforms (continued)

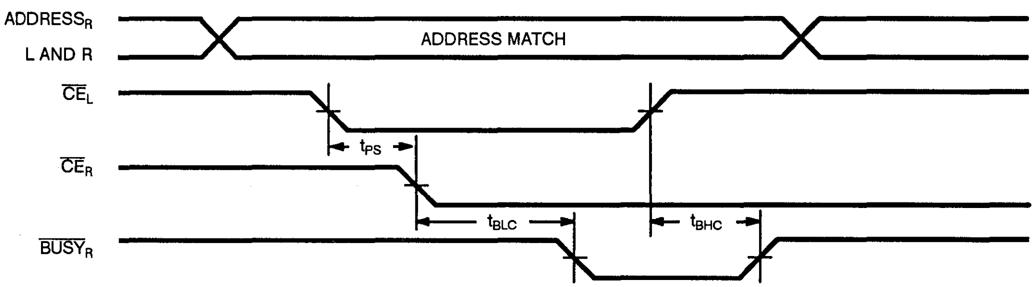
Write Cycle No. 2 [11, 18]



C130–11

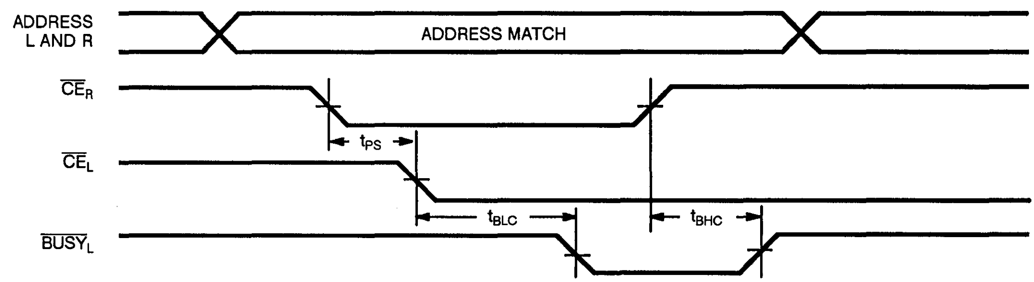
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



C130–12

$\overline{CE}_R$ Valid First:

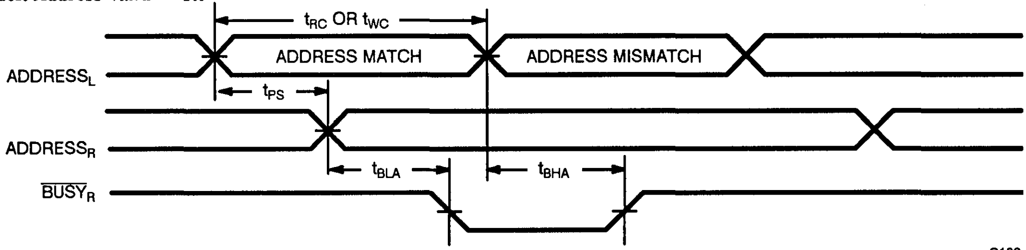


C130–13

Switching Waveforms (continued)

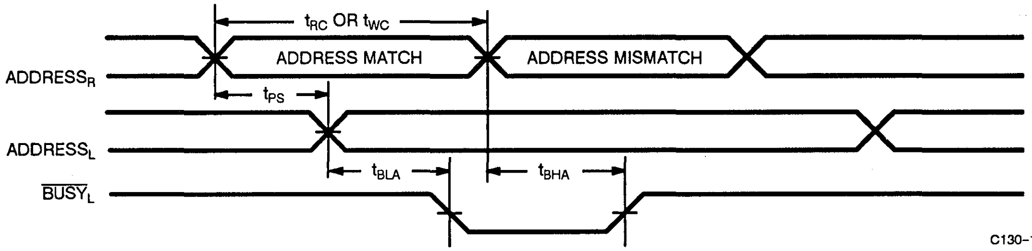
Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:



C130–14

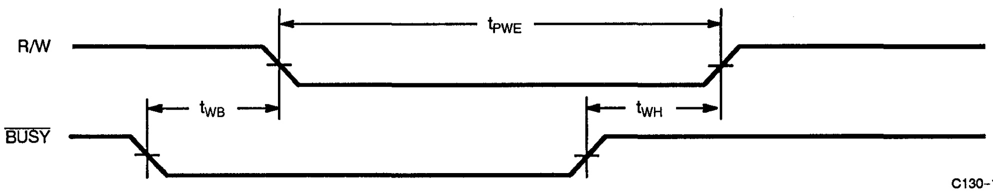
Right Address Valid First:



C130–15

Busy Timing Diagram No. 3

Write with $\overline{\text{BUSY}}$ (Slave: CY7C140/CY7C141)

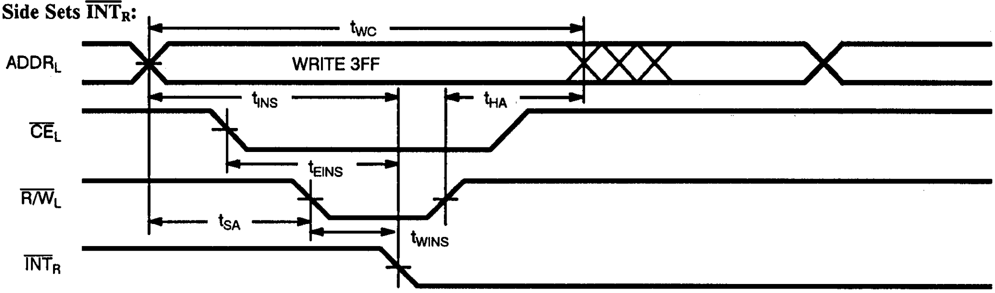


C130–16

Switching Waveforms (continued)

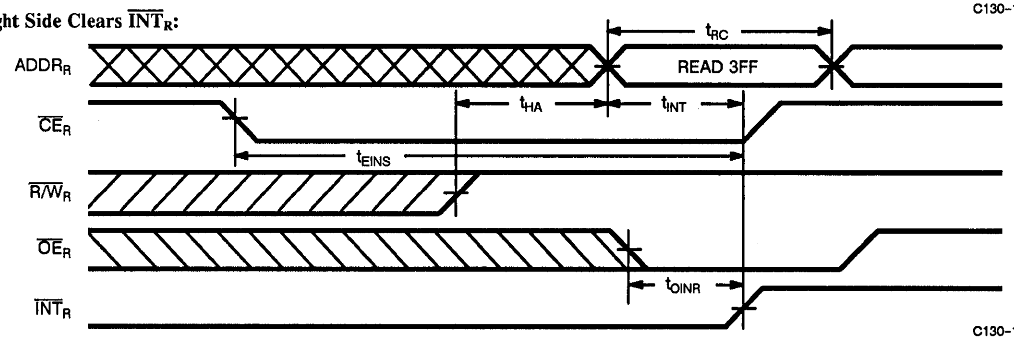
Interrupt Timing Diagrams

Left Side Sets $\overline{INT}_R$:



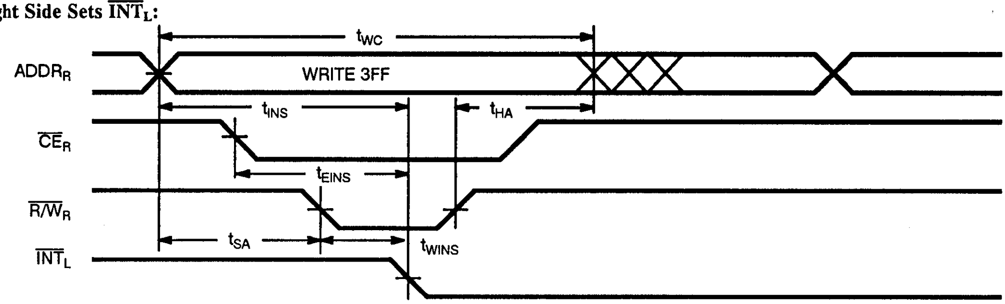
C130–17

Right Side Clears $\overline{INT}_R$:



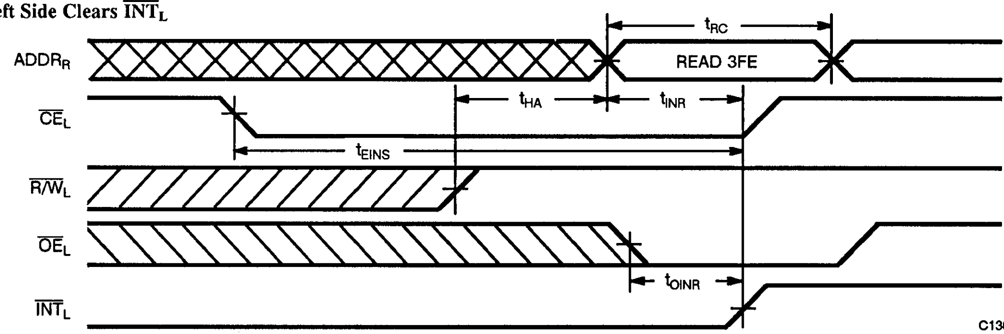
C130–18

Right Side Sets $\overline{INT}_L$:



C130–19

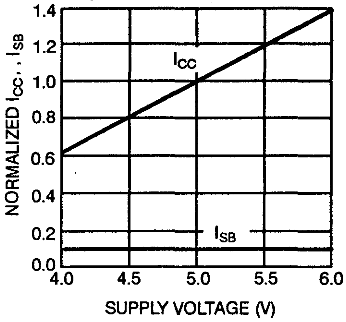
Left Side Clears $\overline{INT}_L$



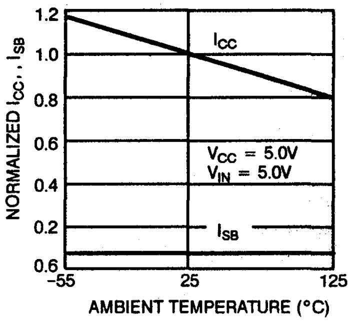
C130–20

Typical DC and AC Characteristics

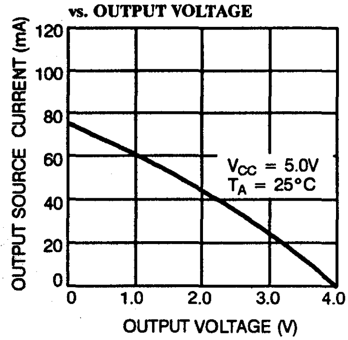
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



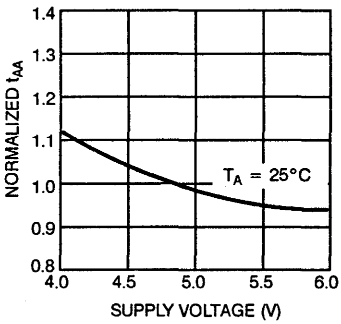
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



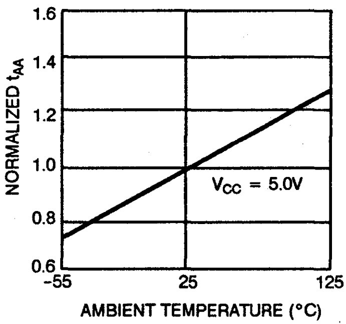
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



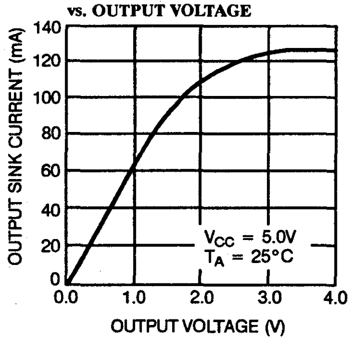
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



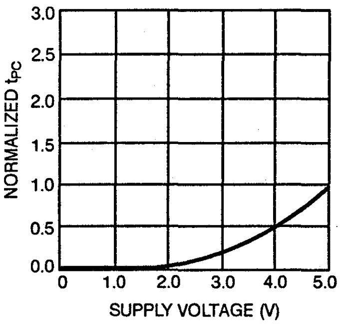
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



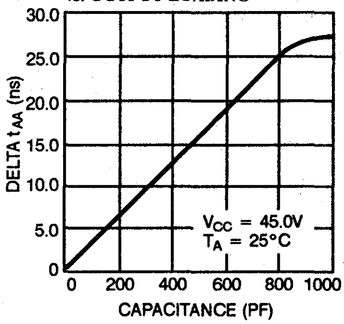
OUTPUT SINN CURRENT vs. OUTPUT VOLTAGE



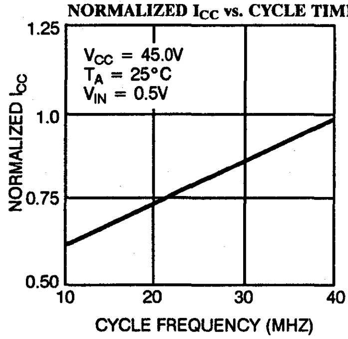
TYPICAL PON EROONCURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CRANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C130-25PC	P25	Commercial
	CY7C130-25DC	D26	
	CY7C130-25LC	L68	
35	CY7C130-35PC	P25	Commercial
	CY7C130-35DC	D26	
	CY7C130-35LC	L68	
	CY7C130-35DMB	D26	Military
	CY7C130-35LMB	L68	
45	CY7C130-45PC	P25	Commercial
	CY7C130-45DC	D26	
	CY7C130-45LC	L68	
	CY7C130-45DMB	D26	Military
	CY7C130-45LMB	L68	
55	CY7C130-55PC	P25	Commercial
	CY7C130-55DC	D26	
	CY7C130-55LC	L68	
	CY7C130-55DMB	D26	Military
	CY7C130-55LMB	L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C140-25PC	P25	Commercial
	CY7C140-25DC	D26	
	CY7C140-25LC	L68	
35	CY7C140-35PC	P25	Commercial
	CY7C140-35DC	D26	
	CY7C140-35LC	L68	
	CY7C140-35DMB	D26	Military
	CY7C140-35LMB	L68	
45	CY7C140-45PC	P25	Commercial
	CY7C140-45DC	D26	
	CY7C140-45LC	L68	
	CY7C140-45DMB	D26	Military
	CY7C140-45LMB	L68	
55	CY7C140-55PC	P25	Commercial
	CY7C140-55DC	D26	
	CY7C140-55LC	L68	
	CY7C140-55DMB	D26	Military
	CY7C140-55LMB	L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C131-25LC	L69	Commercial
	CY7C131-25JC	J69	
35	CY7C131-35LC	L69	Commercial
	CY7C131-35JC	J69	
	CY7C131-35LMB	L69	Military
45	CY7C131-45LC	L69	Commercial
	CY7C131-45JC	J69	
	CY7C131-45LMB	L69	Military
55	CY7C131-55LC	L69	Commercial
	CY7C131-55JC	J69	
	CY7C131-55LMB	L69	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C141-25LC	L69	Commercial
	CY7C141-25JC	J69	
35	CY7C141-35LC	L69	Commercial
	CY7C141-35JC	J69	
	CY7C141-35LMB	L69	Military
45	CY7C141-45LC	L69	Commercial
	CY7C141-45JC	J69	
	CY7C141-45LMB	L69	Military
55	CY7C141-55LC	L69	Commercial
	CY7C141-55JC	L69	
	CY7C141-55LMB	L69	Military

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameters	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[19]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Note:
19. CY7C140 only.

Document #: 38-00027-D

CY7C132/CY7C136
CY7C142/CY7C146

CYPRESS SEMICONDUCTOR

2048 x 8 Dual-Port Static RAM

Features

- 0.8 micron CMOS for optimum speed/power
- Automatic power-down
- TTL-compatible
- Capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation
- MASTER CY7C132/CY7C136 easily expands data bus width to 16 or more bits using SLAVE CY7C142/CY7C146
- BUSY output flag on CY7C132/ CY7C136; BUSY input on CY7C142/CY7C142
- INT flag for port-to-port communication (LCC/PLCC versions)

Functional Description

The CY7C132/CY7C136/CY7C142/ CY7C146 are high-speed CMOS 2K by 8 dual-port static RAMS. Two ports are provided permitting independent access to any location in memory. The CY7C132/ CY7C136 can be utilized as either a standalone 8-bit dual-port static RAM or as a MASTER dual-port RAM in conjunction with the CY7C142/CY7C146 SLAVE dual-port device in systems requiring 16-bit or greater word widths. It is the solution to applications requiring shared or buffered data such as cache memory for DSP, bit-slice, or multiprocessor designs.

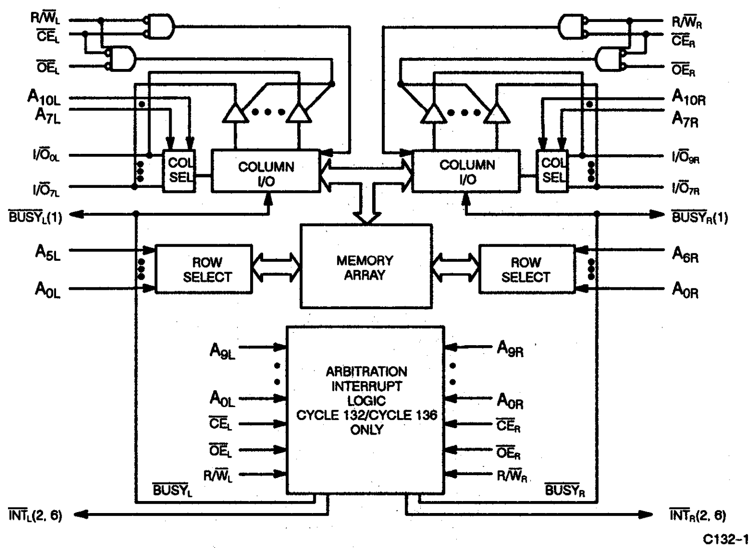
Each port has independent control pins; Chip Enable (CE), Write Enable (WE), and Output Enable (OE). BUSY flags are provided on each port. In addition, an interrupt flag (INT) is provided on each port of the 52-pin LCC or PLCC versions. BUSY signals that the port is trying to access the same location currently be accessed by the other port. On the LCC/PLCC versions, INT is an interrupt flag indicating that data has been placed in a unique location by the other port.

An automatic power-down feature is controlled independently on each port by the Chip Enable (CE) pin.

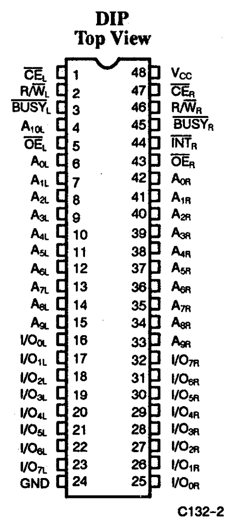
The CY7C132/CY7C142 are available in both 48-pin DIP and 48-pin LCC. The CY7C136/CY7C146 are available in both 52-pin LCC and 52-pin PLCC.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configuration



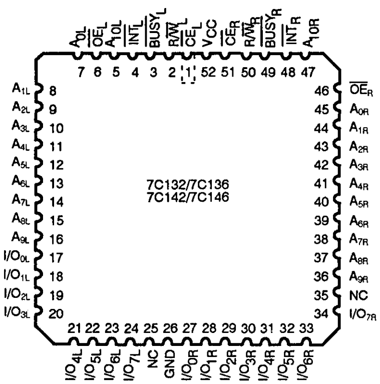
Notes:

1. CY7C132/CY7C136 (Master): BUSY is open drain output and requires pull-up resistor. CY77C142/CY7C146 (Slave): BUSY is input.
2. Open drain outputs; pull-up resitor required.

2

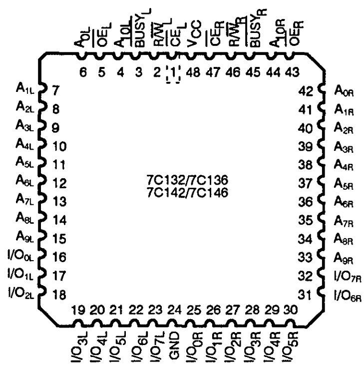
Pin Configurations (continued)

LCC
Top View



C132-3

LCC
Top View



C132-4

Selection Guide

		7C132-25 7C136-25 7C142-25 7C146-25	7C132-35 7C136-35 7C142-35 7C146-35	7C132-45 7C136-45 7C142-45 7C146-45	7C132-55 7C136-55 7C142-55 7C146-55
Maximum Access Time (ns)		25	35	45	55
Maximum Operating Current (mA)	Commerical	170	120	90	90
	Military		170	120	120
Maximum Standby Current (mA)	Commerical	65	45	35	35
	Military		65	45	45

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... − 65°C to + 150°C

Ambient Temperature with Power Applied .... − 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) .... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... − 0.5V to + 7.0V

DC Input Voltage .... − 3.5V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[3]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4]

Parameters	Description	Test Conditions		7C132-25 7C136-25 7C142-25 7C146-25 Min.	7C132-25 7C136-25 7C142-25 7C146-25 Max.	7C132-35 7C136-35 7C142-35 7C146-35 Min.	7C132-35 7C136-35 7C142-35 7C146-35 Max.	7C132-45, 55 7C136-45, 55 7C142-45, 55 7C146-45, 55 Min.	7C132-45, 55 7C136-45, 55 7C142-45, 55 7C146-45, 55 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4		0.4	V
		I_{OL} = 16.0 mA[5]			0.5		0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-5	+5	-5	+5	-5	+5	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		-5	+5	-5	+5	-5	+5	μA
I_{OS}	Output Short Circuit Current[6]	V_{CC} = Max., V_{OUT} = GND			-350		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE} = V_{IL}$, Outputs Open, $f = f_{MAX}$	Com'l		170		120		90	mA
			Mil				170		120	mA
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, $f = f_{MAX}$	Com'l		65		45		35	mA
			Mil				65		45	mA
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, Active Port Outputs Open, $f = f_{MAX}$	Com'l		115		90		75	mA
			Mil				115		90	mA
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0	Com'l		15		15		15	mA
			Mil				15		15	mA
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Ports Outputs Open $f = f_{MAX}$	Com'l		105		85		70	mA
			Mil				105		85	mA

Shaded area contains preliminary information.

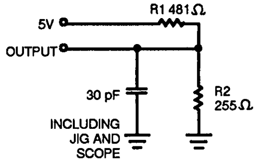
Capacitance[7]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

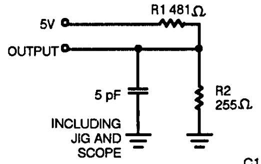
Notes:

3. T_A is the "instant on" case temperature
4. See the last page of this specification for Group A subgroup testing information.
5. $\overline{BUSY}$ and $\overline{INT}$ pins only.
6. Duration of the short circuit should not exceed 30 seconds.
7. Tested initially and after any design or process changes that may affect these parameters.
8. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OI}/I_{OH}, and 30-pF load capacitance.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV form steady state voltage.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referencd to the rising edge of the signal that terminates the write.

AC Test Loads and Waveforms

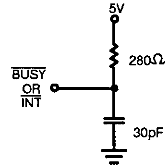


(a)



(b)

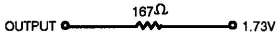
C132-5



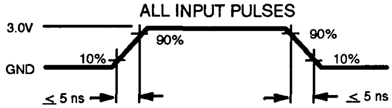
$\overline{BUSY}$ Output Load
(CY7C130/CY7C131 ONLY)

C132-6

Equivalent to: THEVENIN EQUIVALENT



ALL INPUT PULSES



Switching Characteristics Over the Operating Range[4, 8]

Parameters	Description	7C132-25 7C136-25 7C142-25 7C146-25		7C132-35 7C136-35 7C142-35 7C146-35		7C132-45 7C136-45 7C142-45 7C146-45		7C132-55 7C136-55 7C142-55 7C146-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	0		0		0		0		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		30		35		45		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9]		15		20		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[10]	5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9, 10]		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		35		35		35	ns
WRITE CYCLE[11]										
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		35		40		ns
t_{AW}	Address Set-Up to Write End	20		30		35		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		15		20		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		0		ns

Shaded area contains preliminary information.

2

Switching Characteristics Over the Operating Range[4, 8] (continued)

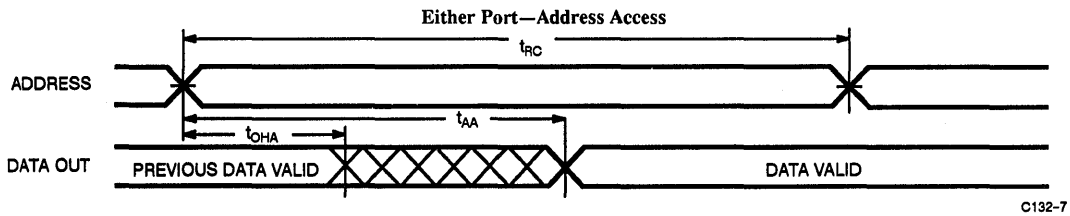
Parameters	Description	7C132-25 7C136-25 7C142-25 7C146-25 Min.	7C132-25 7C136-25 7C142-25 7C146-25 Max.	7C132-35 7C136-35 7C142-35 7C146-35 Min.	7C132-35 7C136-35 7C142-35 7C146-35 Max.	7C132-45 7C136-45 7C142-45 7C146-45 Min.	7C132-45 7C136-45 7C142-45 7C146-45 Max.	7C132-55 7C136-55 7C142-55 7C146-55 Min.	7C132-55 7C136-55 7C142-55 7C146-55 Max.	Units
BUSY/INTERRUPT TIMING										
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		20		20		25		30	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[12]		20		20		25		30	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		20		20		25		30	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[12]		20		20		25		30	ns
t_{PS}	Port Set Up for Priority	5		5		5		5		ns
t_{WB}[13]	$\overline{WE}$ LOW after $\overline{BUSY}$ LOW	0		0		0		0		ns
t_{WH}	$\overline{WE}$ HIGH after $\overline{BUSY}$ HIGH	20		30		35		35		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		25		35		45		45	ns
t_{DDD}	Write Data Valid to Read Data Valid		Note 14		Note 14		Note 14		Note 14	ns
t_{WDD}	Write Pulse to Data Delay		Note 14		Note 14		Note 14		Note 14	ns
INTERRUPT TIMING										
t_{WINS}	$\overline{WE}$ to $\overline{INTERRUPT}$ Set Time		25		25		35		45	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		25		25		35		45	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		25		25		35		45	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[12]		25		25		35		45	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[12]		25		25		35		45	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[12]		25		25		35		45	ns

Shaded area contains preliminary information.

Notes:
12. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
13. CY7C142/CY7C146 only.
14. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the follwoing:
    A. $\overline{BUSY}$ on Port B goes HIGH.
    B. Port B's address toggled.
    C. $\overline{CE}$ for Port B is toggled.
    D. $\overline{WE}$ for Port B is toggled.
15. $\overline{WE}$ is HIGH for read cycle.
16. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
18. Data I/O pins enter high-impedance state, as shown when $\overline{OE}$ is held LOW during write.
19. LCC version only.

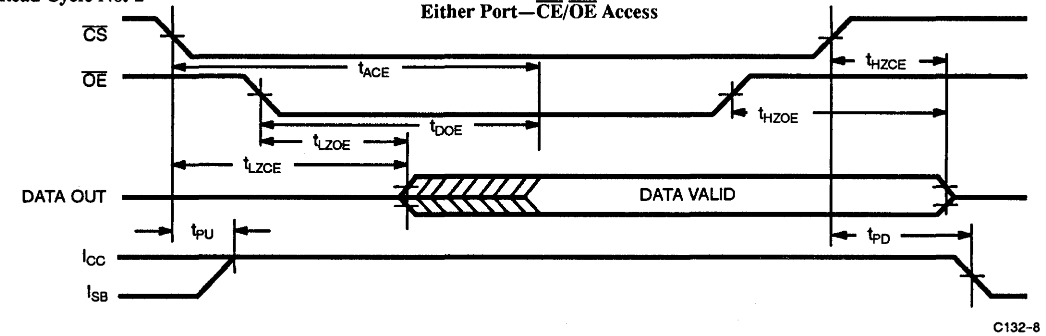
Switching Waveforms

Read Cycle No. 1[15, 16]

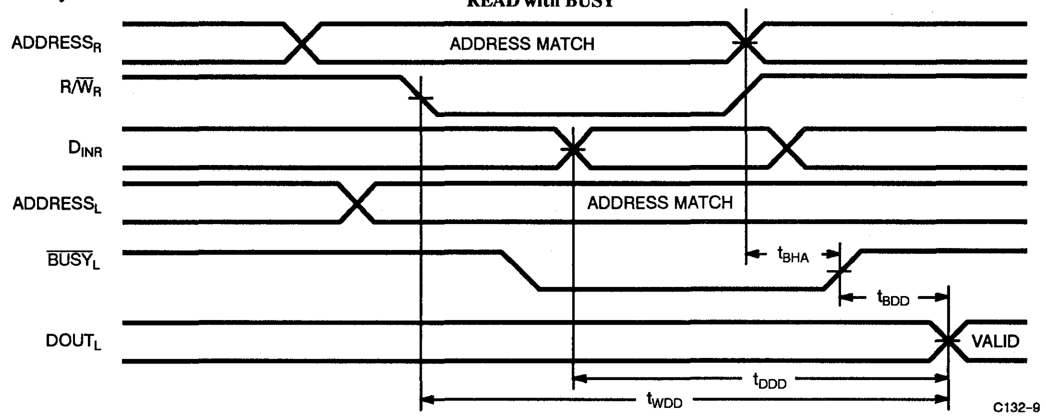


Switching Waveforms (Continued)

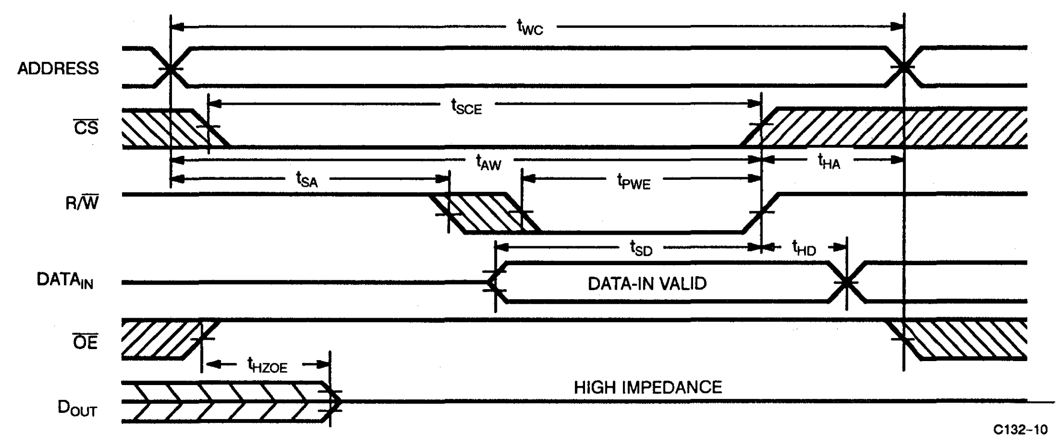
Read Cycle No. 2[15, 17]



Read Cycle No. 3[15]

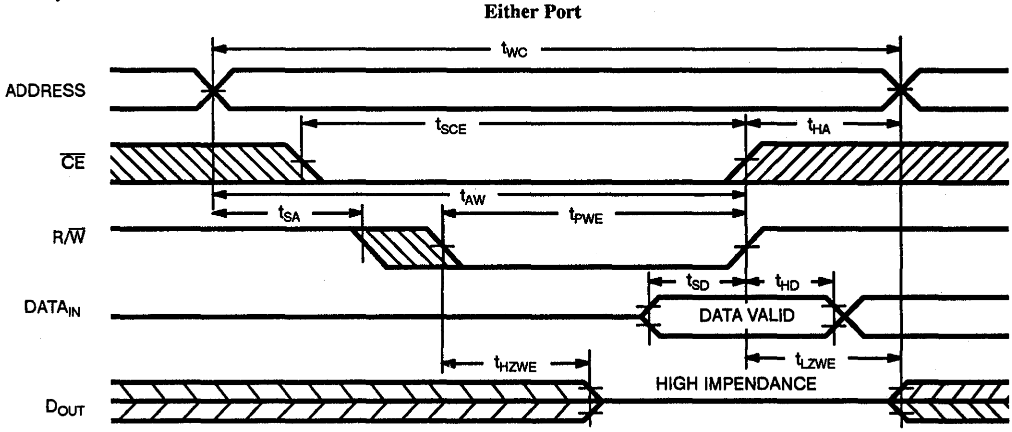


Write Cycle No.1[11, 18]



Switching Waveforms (Continued)

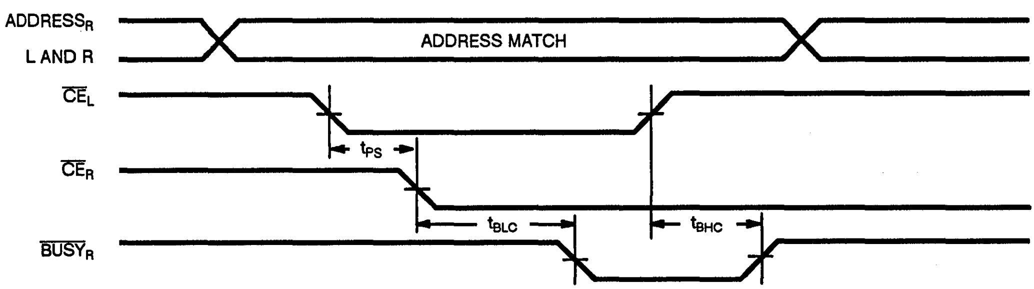
Write Cycle No. 2[11, 18]



C132-11

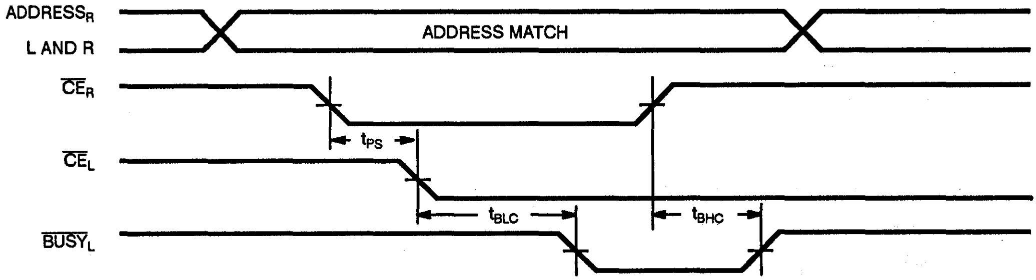
Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



C132-12

$\overline{CE}_R$ Valid First:

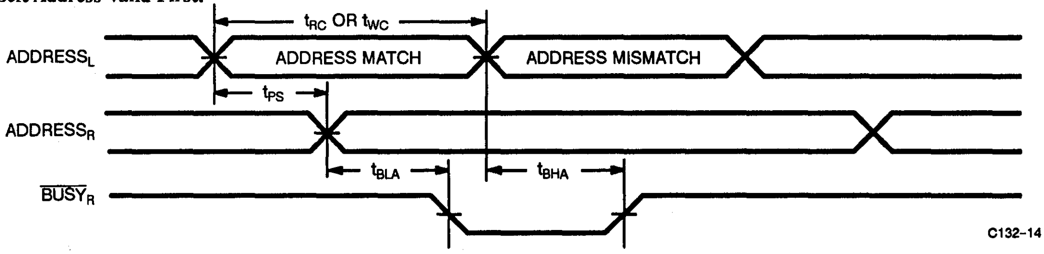


C132-13

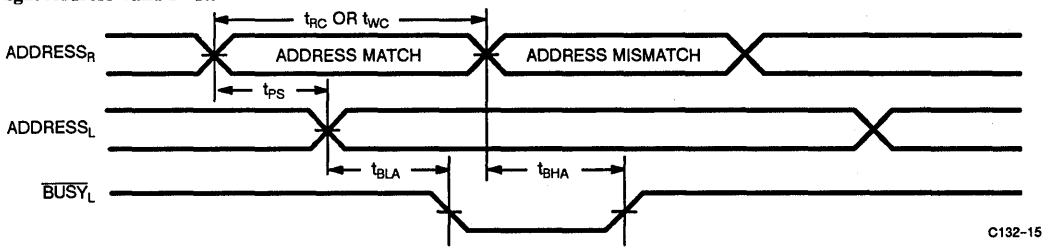
Switching Waveforms (Continued)

Busy Timing Diagram No. 2 (Address Arbitration)

Left Address Valid First:

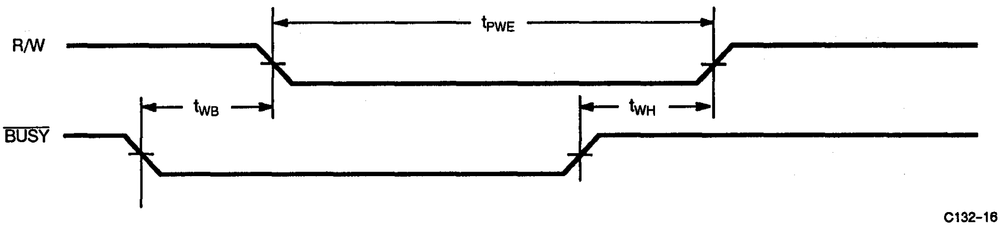


Right Address Valid First:



Busy Timing Diagram No. 3

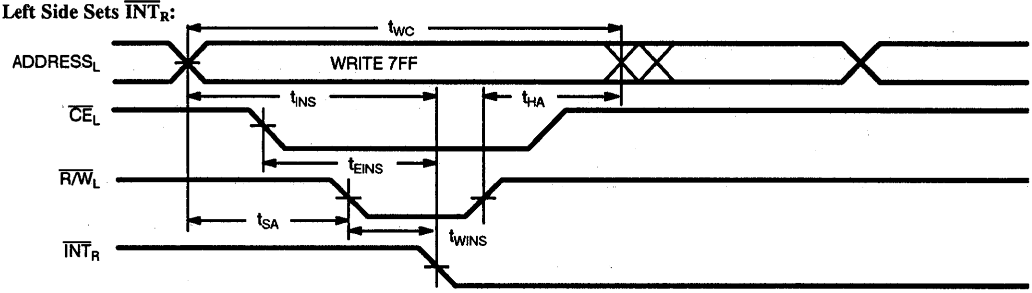
Write with $\overline{\text{BUSY}}$ (Slave: CY7C142/CY7C146)



Switching Waveforms (continued)

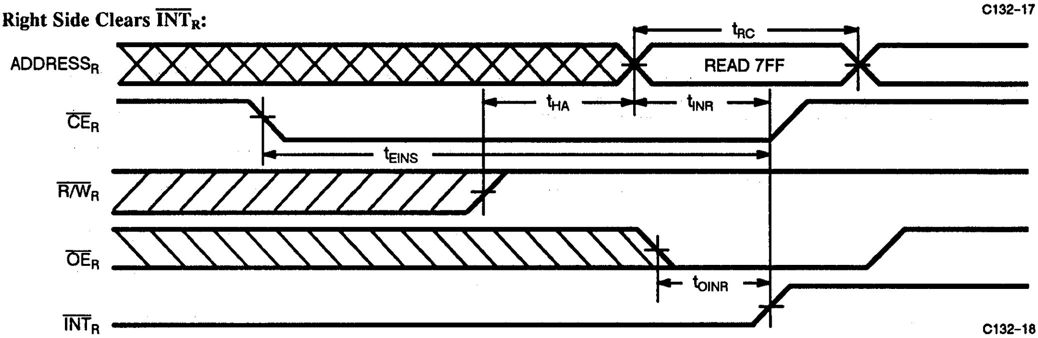
Interrupt Timing Diagrams[19]

Left Side Sets $\overline{\text{INT}}_R$:



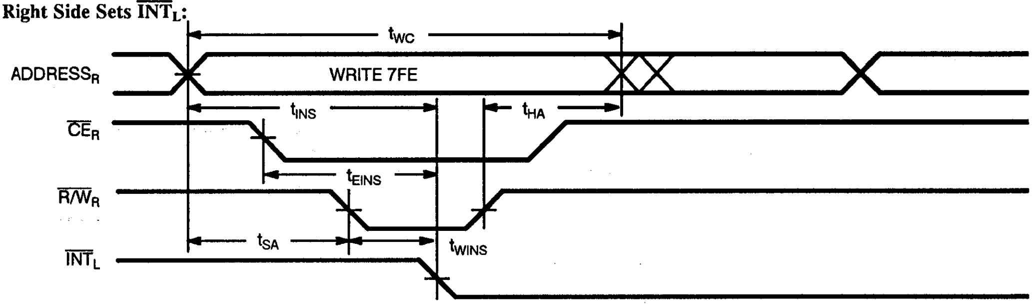
C132–17

Right Side Clears $\overline{\text{INT}}_R$:



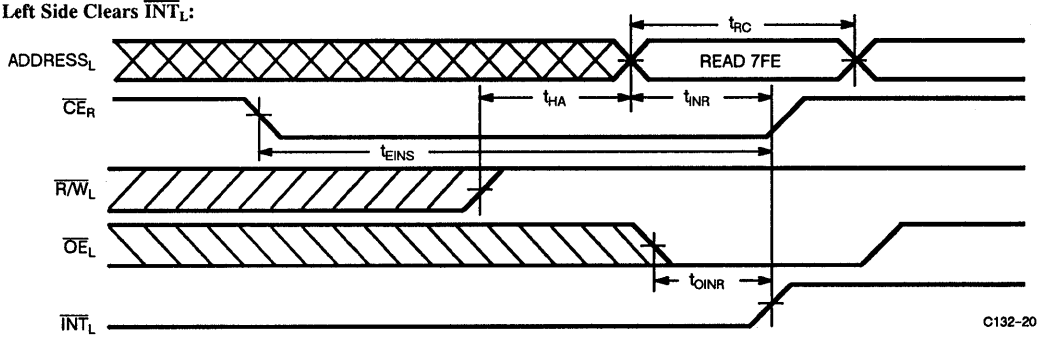
C132–18

Right Side Sets $\overline{\text{INT}}_L$:



C132–19

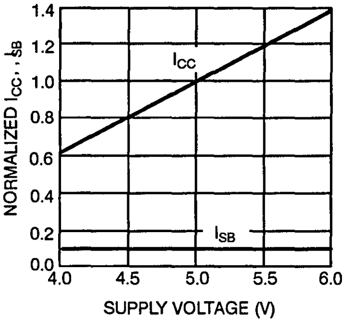
Left Side Clears $\overline{\text{INT}}_L$:



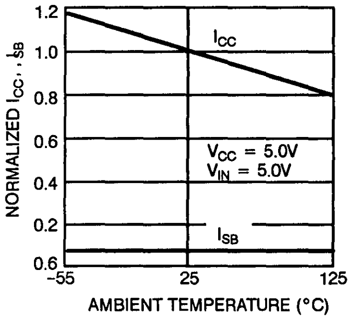
C132–20

Typical DC and AC Characteristics

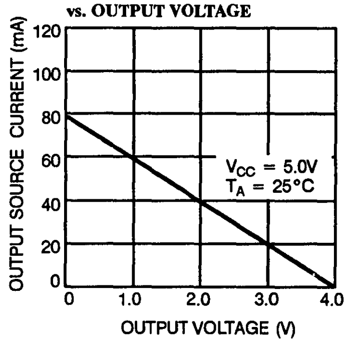
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



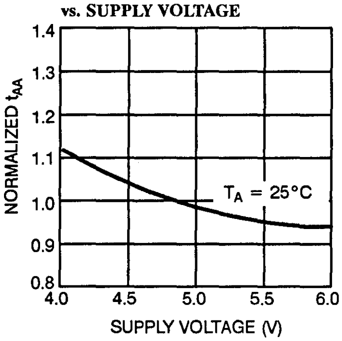
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



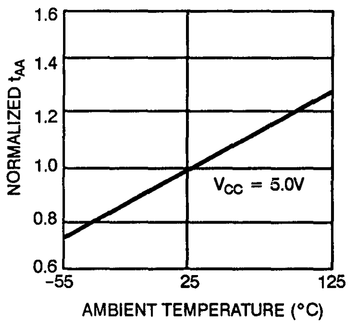
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



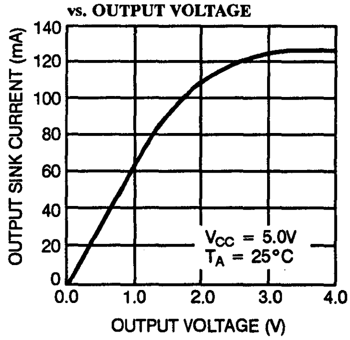
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



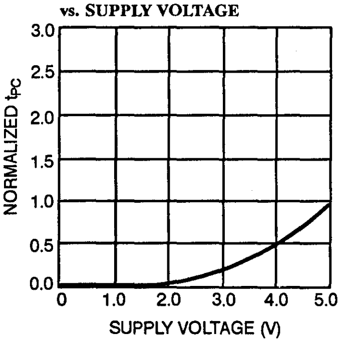
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



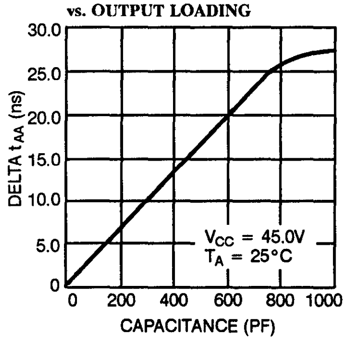
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



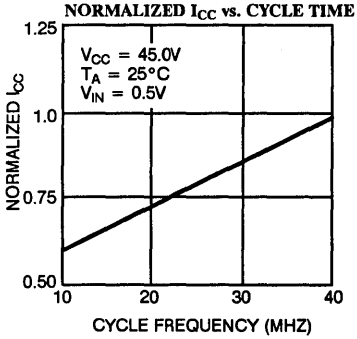
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C132–25PC	P25	Commerical
	CY7C132–25DC	D26	
	CY7C132–25LC	L68	
35	CY7C132–35PC	P25	Commerical
	CY7C132–35DC	D26	
	CY7C132–35LC	L68	
	CY7C132–35DMB	D26	Military
	CY7C132–35LMB	L68	
45	CY7C132–45PC	P25	Commerical
	CY7C132–45DC	D26	
	CY7C132–45LC	L68	
	CY7C132–45DMB	D26	Military
	CY7C132–45LMB	L68	
55	CY7C132–55PC	P25	Commerical
	CY7C132–55DC	D26	
	CY7C132–55LC	L68	
	CY7C132–55DMB	D26	Military
	CY7C132–55LMB	L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C142–25PC	P25	Commerical
	CY7C142–25DC	D26	
	CY7C142–25LC	L68	
35	CY7C142–35PC	P25	Commerical
	CY7C142–35DC	D26	
	CY7C142–35LC	L68	
	CY7C142–35DMB	D26	Military
	CY7C142–35LMB	L68	
45	CY7C142–45PC	P25	Commerical
	CY7C142–45DC	D26	
	CY7C142–45LC	L68	
	CY7C142–45DMB	D26	Military
	CY7C142–45LMB	L68	
55	CY7C142–55PC	P25	Commerical
	CY7C142–55DC	D26	
	CY7C142–55LC	L68	
	CY7C142–55DMB	D26	Military
	CY7C142–55LMB	L68	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C136–25LC	L69	Commerical
	CY7C136–25JC	J69	
35	CY7C136–35LC	L69	Commerical
	CY7C136–35JC	J69	
	CY7C136–35LMB	L69	Military
45	CY7C136–45LC	L69	Commerical
	CY7C136–45JC	J69	
	CY7C136–45LMB	L69	Military
55	CY7C136–55LC	L69	Commerical
	CY7C136–55JC	J69	
	CY7C136–55LMB	L69	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C146–25LC	L69	Commerical
	CY7C146–25JC	J69	
35	CY7C146–35LC	L69	Commerical
	CY7C146–35JC	J69	
	CY7C146–35LMB	L69	Military
45	CY7C146–45LC	L69	Commerical
	CY7C146–45JC	J69	
	CY7C146–45LMB	L69	Military
55	CY7C146–55LC	L69	Commerical
	CY7C146–55JC	L69	
	CY7C146–55LMB	L69	Military

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Parameters	Subgroups
BUSY/INTERRUPT TIMING	
t_{BLA}	7, 8, 9, 10, 11
t_{BHA}	7, 8, 9, 10, 11
t_{BLC}	7, 8, 9, 10, 11
t_{BHC}	7, 8, 9, 10, 11
t_{PS}	7, 8, 9, 10, 11
t_{WINS}	7, 8, 9, 10, 11
t_{EINS}	7, 8, 9, 10, 11
t_{INS}	7, 8, 9, 10, 11
t_{OINR}	7, 8, 9, 10, 11
t_{EINR}	7, 8, 9, 10, 11
t_{INR}	7, 8, 9, 10, 11
BUSY TIMING	
t_{WB}[20]	7, 8, 9, 10, 11
t_{WH}	7, 8, 9, 10, 11
t_{BDD}	7, 8, 9, 10, 11
t_{DDD}	7, 8, 9, 10, 11
t_{WDD}	7, 8, 9, 10, 11

Note:
20. CY7C142 only.

Document #: 38-00061-C

CYPRESS SEMICONDUCTOR

CY7C147

4096 x 1 Static RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 605 mW (military)**
- **Low standby power**
  - **— 55 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

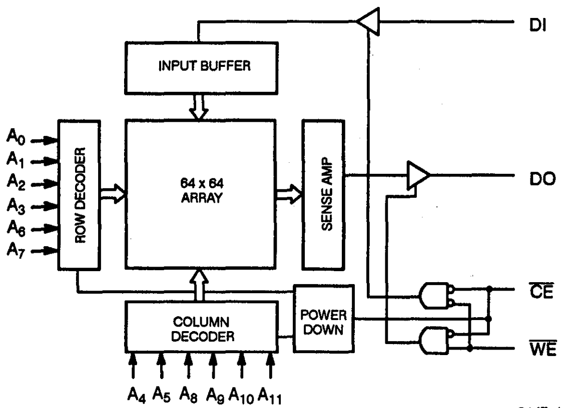
The CY7C147 is a high-performance CMOS static RAMs organized as 4096 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C147 has an automatic power-down feature, reducing the power consumption by 80% when deselected .

Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while ($\overline{WE}$) remains HIGH. Under these condintions, the contents of the location specified on the address pins will appear on the data output (DO) pin.

The output pin remains in a high-impedance state when chip enable is HIGH, or write enable ($\overline{WE}$) is LOW.

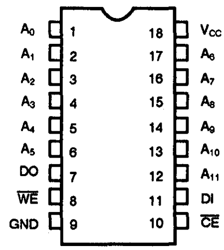
Logic Block Diagram



C147-1

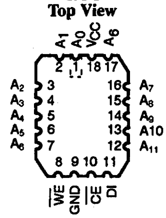
Pin Configurations

DIP
Top View



C147-2

LCC
Top View



C147-3

Selection Guide

		7C147-25	7C147-35	7C147-45
Maximum Access Time (ns)	Commercial	25	35	45
	Military		35	45
Maximum Operating Current (mA)	Commercial	90	80	80
	Military		110	110
Maximum Standby Current (mA)	Commercial	15	10	10
	Military		10	10

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... $-65°C$ to $+150°C$

Ambient Temperature with Power Applied .... $-55°C$ to $+125°C$

Supply Voltage to Ground Potential (Pin 18 to Pin 9) .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs in High Z State .... $-0.5V$ to $+7.0V$

DC Input Voltage .... $-3.0V$ to $+7.0V$

Output Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C147-25 Min.	7C147-25 Max.	7C147-35,45 Min.	7C147-35,45 Max.	Units
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.4		0.4	V
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	V
V_{IL}	Input Low Voltage			-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$ Output Disabled		-50	+50	-50	+50	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		80	mA
			Mil				110	
I_{SB}	Automatic $\overline{CE}$[4] Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$	Com'l		15		10	mA
			Mil				10	

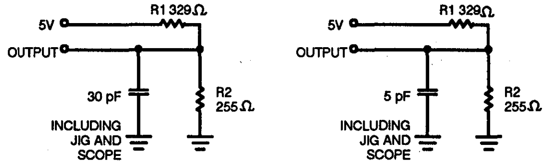
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		6	pF

Notes:

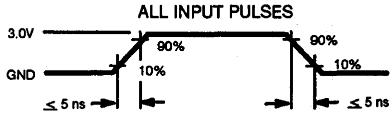
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during VCC power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices.
8. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to intiate a write and either signal can teminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

AC Test Loads and Waveforms



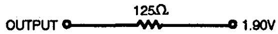
(a) (b)

C168-4



C168-5

Equivalent to: THÉVENIN EQUIVALENT

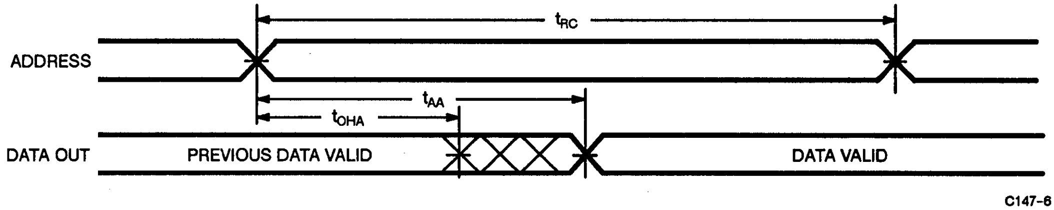


Switching Characteristics Over the Operating Range[6]

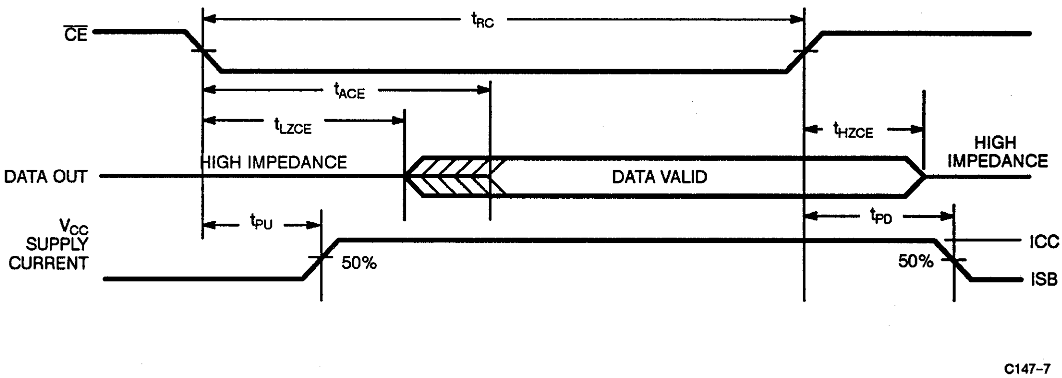
Parameters	Description	7C147-25		7C147-35		7C147-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7,8]		20		30		30	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		20	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	CE LOW to Write End	25		35		45		ns
t_{AW}	Address Set-Up to Write End	25		35		45		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	WE Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	0		10		10		ns
t_{LZWE}	WE HIGH to Low Z[7]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7,8]		15		20		25	ns

Switching Waveforms

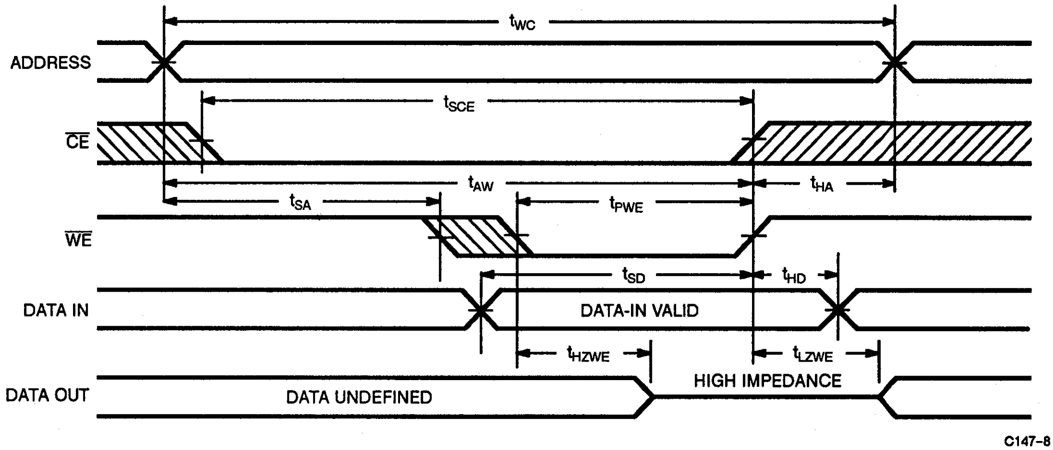
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



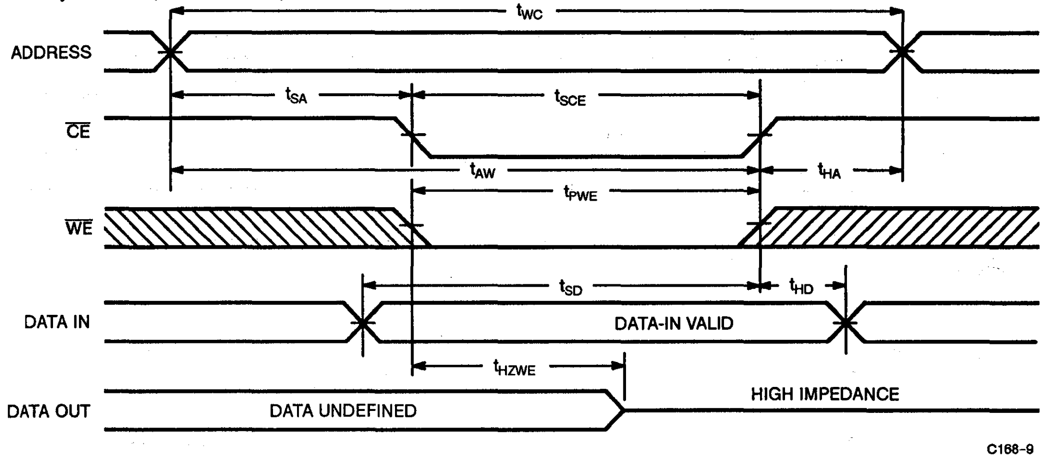
Write Cycle No. 1 ($\overline{WE}$ Controlled)[9]



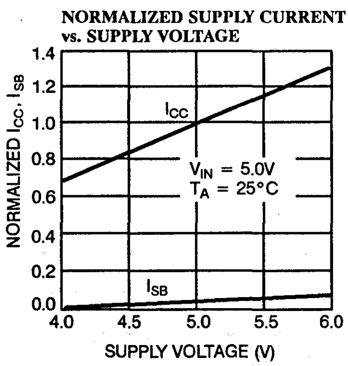
2

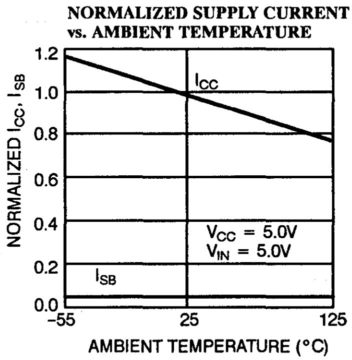
Switching Waveforms (continued)

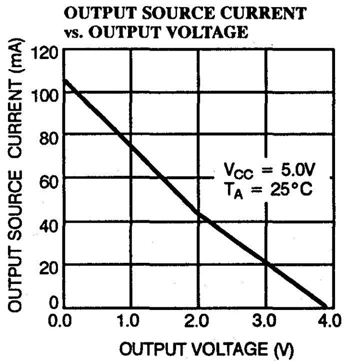
Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 13]

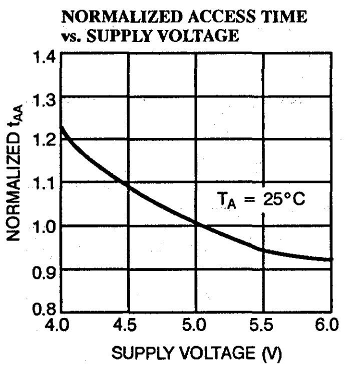


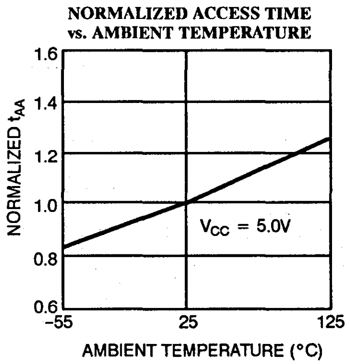
Typical DC and AC Characteristics

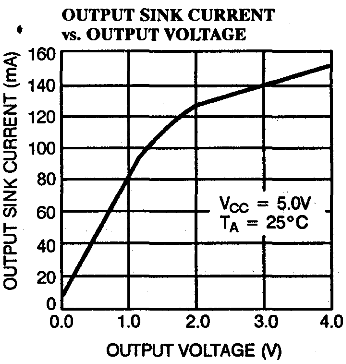




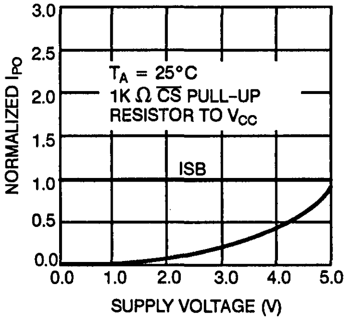




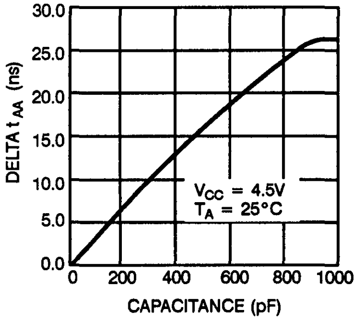




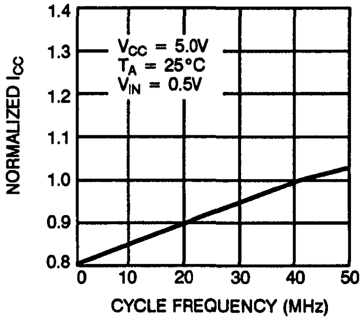
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE (7C148)



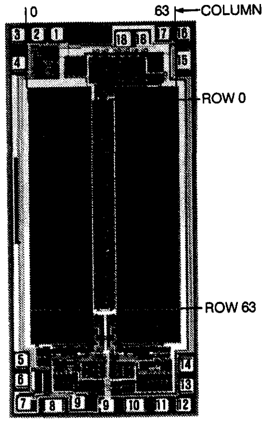
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Bit Map



Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	1
A_1	X_1	2
A_2	X_2	3
A_3	X_3	4
A_4	Y_0	5
A_5	Y_1	6
A_6	X_4	17
A_7	X_5	16
A_8	Y_2	15
A_9	Y_3	14
A_{10}	Y_4	13
A_{11}	Y_5	12

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C147-25PC	P3	Commercial
	CY7C147-25DC	D4	
	CY7C147-25LC	L50	
35	CY7C147-35PC	P3	Commercial
	CY7C147-35DC	D4	
	CY7C147-35LC	L50	
	CY7C147-35DMB	D4	Military
	CY7C147-35KMB	K70	
	CY7C147-35LMB	L50	
45	CY7C147-45PC	P3	Commercial
	CY7C147-45DC	D4	
	CY7C147-45LC	L50	
	CY7C147-45DMB	D4	Military
	CY7C147-45KMB	K70	
	CY7C147-45LMB	L50	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7,8,9,10,11
t_{AA}	7,8,9,10,11
t_{OHA}	7,8,9,10,11
t_{ACE}	7,8,9,10,11
WRITE CYCLE	
t_{WC}	7,8,9,10,11
t_{SCE}	7,8,9,10,11
t_{AW}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{SA}	7,8,9,10,11
t_{PWE}	7,8,9,10,11
t_{SD}	7,8,9,10,11
t_{HD}	7,8,9,10,11

Document #: 38-00030-B

CYPRESS SEMICONDUCTOR

1024 x 4 Static RAM

Features

- **Automatic power-down when deselected (7C148)**
- **CMOS for optimum speed/power**
- **25-ns access time**
- **Low active power**
  - **— 440 mW (commercial)**
  - **— 605 mW (military)**
- **Low standby power (7C148)**
  - **— 82.5 mW (25-ns version)**
  - **— 55 mW (all others)**
- **5-volt power supply ± 10% tolerance, both commercial and military**
- **TTL-compatible inputs and outputs**

Functional Description

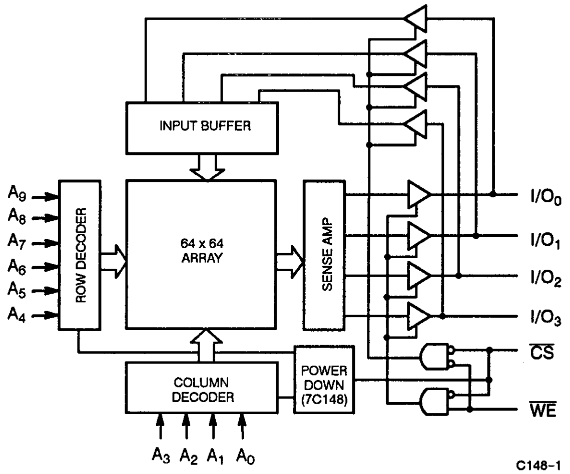
The CY7C148 and CY7C149 are high-performance CMOS static RAMs organized as 1024 by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The CY7C148 remains in a low-power mode as long as the device remains unselected; i.e., ($\overline{CS}$) is HIGH, thus reducing the average power requirements of the device. The chip select ($\overline{CS}$) of the CY7C149 does not affect the power dissipation of the device.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the I/O pins (I/O_0 through I/O_3) is written into the memory locations specified on the address pins (A_0 through A_9).

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data I/O pins.

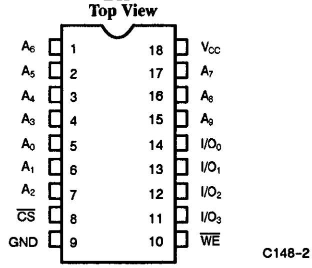
The I/O pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram

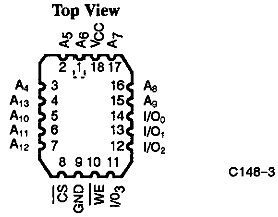


Pin Configurations

DIP
Top View



LCC
Top View



Selection Guide

		7C148-25	7C148-35	7C148-45	7C149-25	7C149-35	7C149-45
Maximum Access Time (ns)		25	35	45	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	80	90	80	80
	Military		110	110		110	110
Maximum Standby Current (mA)	Commercial	15	10	10			
	Military		10	10			

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 18 to Pin 9) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions			7C148/9-25		7C148/9-35,45		Units
					Min.	Max.	Min.	Max.	
I_{OH}	Output High Current	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		V
I_{OL}	Output Low Current	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input High Voltage				2.0	6.0	2.0	6.0	V
V_{IL}	Input Low Voltage				−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$			−10	10	−10	10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$ Output Disabled			−50	50	−50	50	μA
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CS} \leq V_{IL}$, Output Open		Com'l		90		80	mA
				Mil				110	
I_{SB}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CS} \geq V_{IH}$	7C148 only	Com'l		15		10	mA
				Mil				10	
I_{PO}	Peak Power-On Current[3]	Max. V_{CC}, $\overline{CS} \geq V_{IH}$	7C148 only	Com'l		15		10	mA
				Mil				10	
I_{OS}	Output Short Circuit Current[4]	GND $\leq V_O \leq V_{CC}$		Com'l		±275		±275	mA
				Mil				±350	

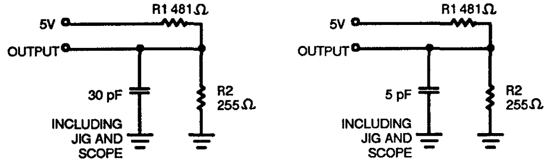
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

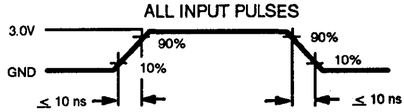
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up. Otherwise current will exceed values given (CY7C148 only).
4. For test purposes, not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Chip deselected greater than 25 ns prior to selection.
7. Chip deselected less than 25 ns prior to selection.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500 mV from steady state voltage with specified loading in part (b) of AC Test Loads.
9. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to intiate a write and either signal can terminate a write by going high. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CS}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

AC Test Loads and Waveforms



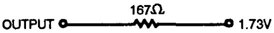
(a) (b) C148-4



C148-5

2

Equivalent to: THÉVENIN EQUIVALENT

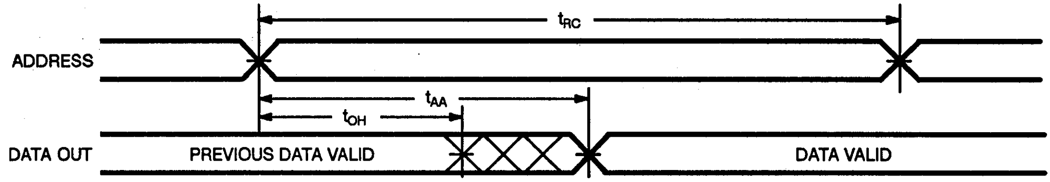


Switching Characteristics Over the Operating Range[2]

Parameters	Description		7C148-25 7C149-25 Min.	Max.	7C148-35 7C149-35 Min.	Max.	7C148-45 7C149-45 Min.	Max.	Units
READ CYCLE									
t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)		25		35		45		ns
t_{AA}	Address Valid to Data Out Valid Delay (Address Access Time)			25		35		45	ns
t_{ACS1}	Chip Select LOW to Data Out Valid (7C148only)			25[6]		35		45	ns
t_{ACS2}				30[7]		35		45	ns
t_{ACS}	Chip Select LOW to Data Out Valid (7C149 only)			15		15		20	ns
t_{LZ}[8]	Chip Select LOW to Data Out On	7C148	8		10		10		ns
		7C149	5		5		5		
t_{HZ}[8]	Chip Select HIGH to Data Out Off		0	15	0	20	0	20	ns
t_{OH}	Address Unknown to Data Out Unknown Time		0		0		5		ns
t_{PD}	Chip Select HIGH to Power-Down Delay	7C148		20		30		30	ns
t_{PU}	Chip Select LOW to Power-Up Delay	7C148	0		0		0		ns
WRITE CYCLE									
t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)		25		35		45		ns
t_{WP}[9]	Write Enable LOW to Write Enable HIGH		20		30		35		ns
t_{WR}	Address Hold from Write End		5		5		5		ns
t_{WZ}[8]	Write Enable to Output in High Z		0	8	0	8	0	8	ns
t_{DW}	Data in Valid to Write Enable HIGH		12		20		20		ns
t_{DH}	Data Hold Time		0		0		0		ns
t_{AS}	Address Valid to Write Enable LOW		0		0		0		ns
t_{CW}[9]	Chip Select LOW to Write Enable HIGH		20		30		40		ns
t_{OW}[8]	Write Enable HIGH to Output in Low Z		0		0		0		ns
t_{AW}	Address Valid to End of Write		20		30		35		

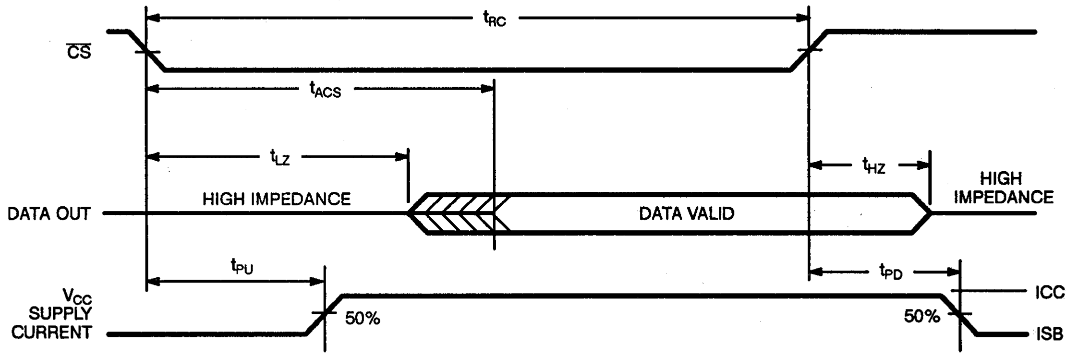
Switching Waveforms

Read Cycle No. 1[10, 11]



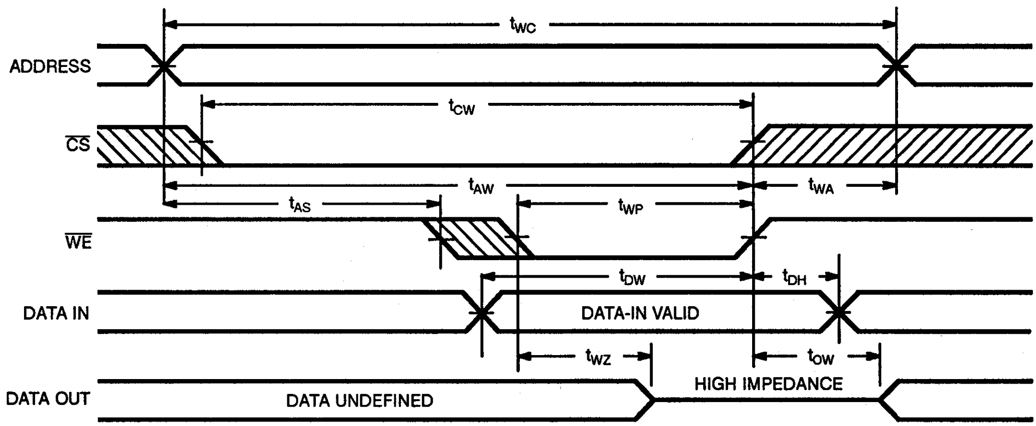
C148-6

Read Cycle No. 2[10, 12]



C148-7

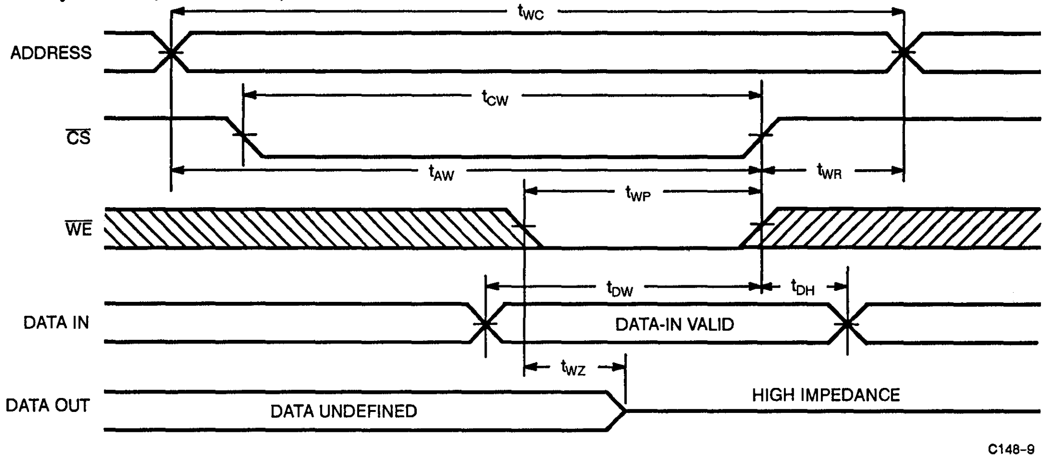
Write Cycle No. 1 ($\overline{WE}$ Controlled)



C148-8

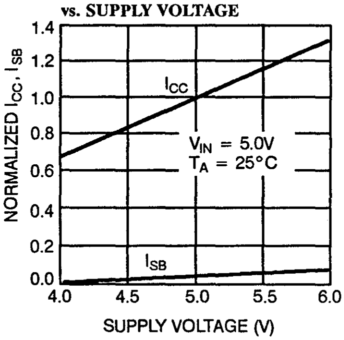
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[13]

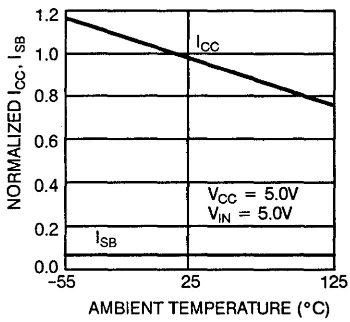


Typical DC and AC Characteristics

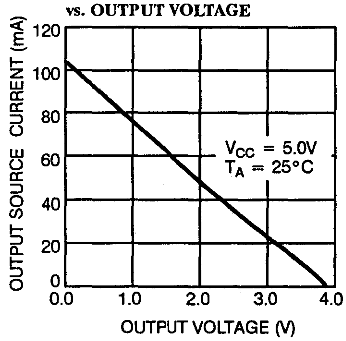
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



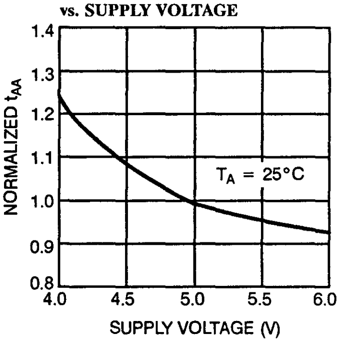
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



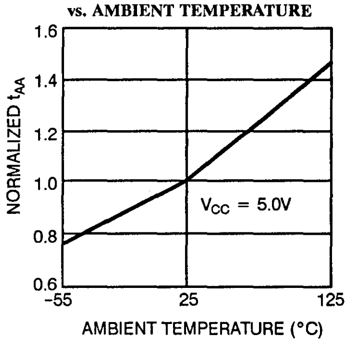
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



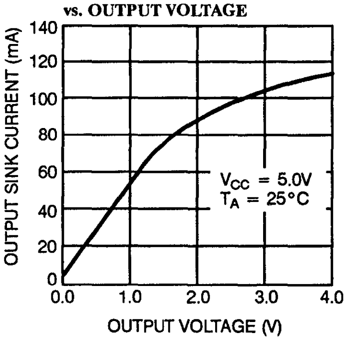
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

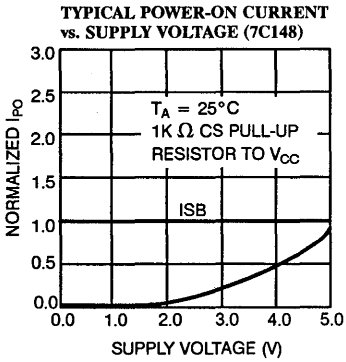


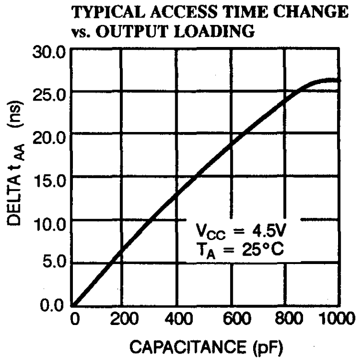
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

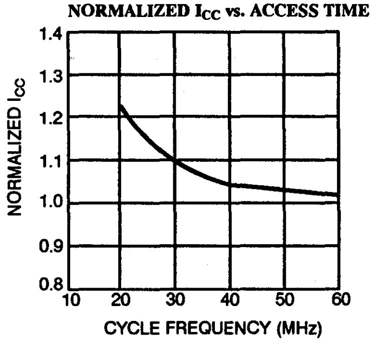


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

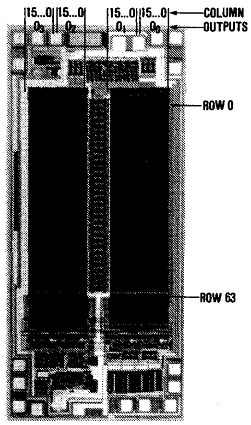








Bit Map



Address Designators

Address Name	Address Function	Pin Number
A_0	Y_0	5
A_1	Y_1	6
A_2	Y_2	7
A_3	Y_3	4
A_4	X_0	3
A_5	X_3	2
A_6	X_2	1
A_7	X_5	17
A_8	X_4	16
A_9	X_1	15

2

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C148-25PC	P3	Commercial
	CY7C148-25DC	D4	
	CY7C148-25LC	L50	
35	CY7C148-35PC	P3	Commercial
	CY7C148-35DC	D4	
	CY7C148-35LC	L50	
	CY7C148-35DMB	D4	Military
	CY7C148-35KMB	K70	
	CY7C148-35LMB	L50	
45	CY7C148-45PC	P3	Commercial
	CY7C148-45DC	D4	
	CY7C148-45LC	L50	
	CY7C148-45DMB	D4	Military
	CY7C148-45KMB	K70	
	CY7C148-45LMB	L50	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C149-25PC	P3	Commercial
	CY7C149-25DC	D4	
	CY7C149-25LC	L50	
35	CY7C149-35PC	P3	Commercial
	CY7C149-35DC	D4	
	CY7C149-35LC	L50	
	CY7C149-35DMB	D4	Military
	CY7C149-35KMB	K70	
	CY7C149-35LMB	L50	
45	CY7C149-45PC	P3	Commercial
	CY7C149-45DC	D4	
	CY7C149-45LC	L50	
	CY7C149-45DMB	D4	Military
	CY7C149-45KMB	K70	
	CY7C149-45LMB	L50	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
I_{OH}	1,2,3
I_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}[14]	1,2,3

Document #: 38-00031-B

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7,8,9,10,11
t_{AA}	7,8,9,10,11
t_{ACS1}[14]	7,8,9,10,11
t_{ACS2}[14]	7,8,9,10,11
t_{ACS}[15]	7,8,9,10,11
t_{OH}	7,8,9,10,11
WRITE CYCLE	
t_{WC}	7,8,9,10,11
t_{WP}	7,8,9,10,11
t_{WR}	7,8,9,10,11
t_{DW}	7,8,9,10,11
t_{DH}	7,8,9,10,11
t_{AS}	7,8,9,10,11
t_{AW}	7,8,9,10,11

Notes:
14. 7C148 only.
15. 7C149 only.

CY7C150

CYPRESS SEMICONDUCTOR

1024 x 4 Static R/W RAM

Features

- **Memory reset function**
- **1024 x 4 static RAM for control store in high-speed computers**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 12 ns (commercial)**
  - **— 15 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 550 mW (military)**
- **Separate inputs and outputs**
- **5-volt power supply ±10% tolerance in both commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **TTL-compatible inputs and outputs**

Functional Description

The CY7C150 is a high-performance CMOS static RAM designed for use in cache memory, high-speed graphics, and data-acquisition applications. The CY7C150 has a memory reset feature that allows the entire memory to be reset in two memory cycles.

Separate I/O paths eliminates the need to multiplex data in and data out, providing for simpler board layout and faster system performance. Outputs are tri-stated during write, reset, deselect, or when output enable ($\overline{OE}$) is held HIGH, allowing for easy memory expansion.

Reset is initiated by selecting the device ($\overline{CS}$ = LOW) and taking the reset ($\overline{RS}$) input LOW. Within two memory cycles all bits are internally cleared to zero. Since chip select must be LOW for the device to be reset, a global reset signal can be employed, with only selected devices being cleared at any given time.

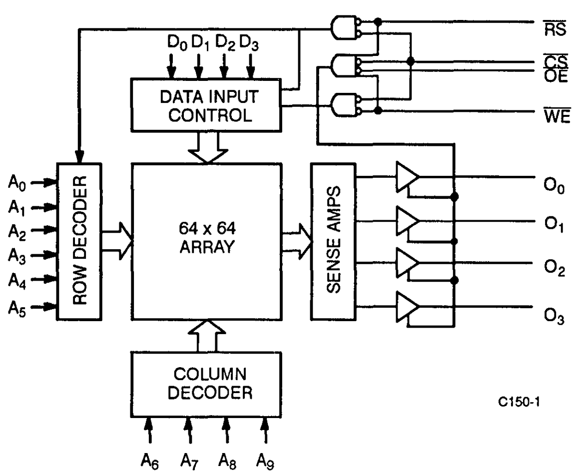
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data inputs (D_0–D_3) is written into the memory location specified on the address pins (A_0 through A_9).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3).

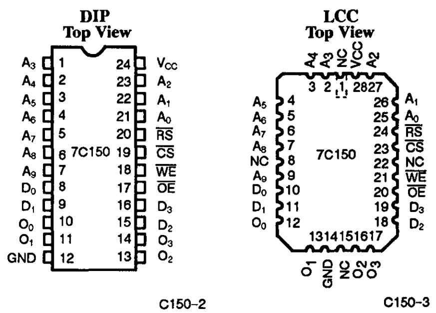
The output pins remain in high-impedance state when chip enable ($\overline{CE}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or reset ($\overline{RS}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C150-10	7C150-12	7C150-15	7C150-25	7C150-35
Maximum Access Time (ns)	Commercial	10	12	15	25	35
	Military		12	15	25	35
Maximum Operating Current (mA)	Commercial	90	90	90	90	90
	Military		100	100	100	100

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

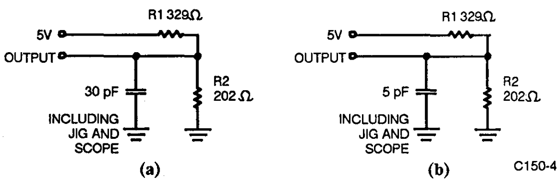
Electrical Characteristics Over the Operating Range[2]

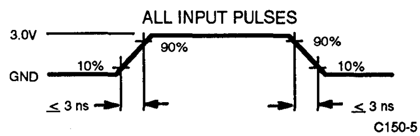
Parameters	Description	Test Conditions		7C150 Min.	7C150 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 5.2 mA		2.4		V
V_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Level			2.0	V_{CC}	V
V_{IL}	Input LOW Level			– 3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-10	+ 10	μA
I_{OZ}	Output Current (High Z)	$V_{OL} \leq V_{OUT} \leq V_{OH}$, Output Disabled		-50	+ 50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		90	mA
			Military		100	mA

Capacitance[4]

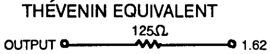
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms





Equivalent to:



Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at a time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Test conditions assume signal transition times of 5 ns or less, timing referenece levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

Switching Characteristics Over the Operating Range[2, 5]

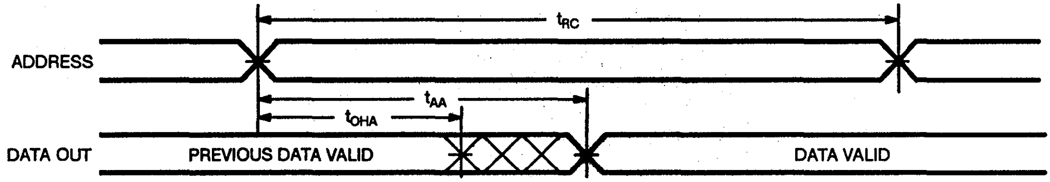
Parameters	Description	7C150-10		7C150-12		7C150-15		7C150-25		7C150-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	10		12		15		25		35		ns
t_{AA}	Address to Data Valid		10		12		15		25		35	ns
t_{OHA}	Output Hold from Address Change	2		2		2		2		2		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		8		10		12		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	0		0		0		0		0		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6, 7]		6		8		11		20		25	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		8		10		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	0		0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		6		8		9		20		25	ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	10		12		15		25		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	6		8		11		15		20		ns
t_{AW}	Address Set-Up to Write End	8		10		13		20		30		ns
t_{HA}	Address Hold from Write End	2		2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		8		11		15		20		ns
t_{SD}	Data Set-Up to Write End	6		8		11		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		6		8		12		20		25	ns
RESET CYCLE												
t_{RRC}	Reset Cycle Time	20		24		30		50		70		ns
t_{SAR}	Address Valid to Beginning of Reset	0		0		0		0		0		ns
t_{SWER}	Write Enable HIGH to Beginning of Reset	0		0		0		0		0		ns
t_{SCSR}	Chip Select LOW to Beginning of Reset	0		0		0		0		0		ns
t_{PRS}	Reset Pulse Width	10		12		15		20		30		ns
t_{HCSR}	Chip Select Hold After End of Reset	0		0		0		0		0		ns
t_{HWER}	Write Enable Hold After End of Reset	8		12		15		30		40		ns
t_{HAR}	Address Hold After End of Reset	10		12		15		30		40		ns
t_{LZRS}	Reset HIGH to Output in Low Z[6]	0		0		0		0		0		ns
t_{HZRS}	Reset LOW to Output in High Z[6, 7]		6		8		12		20		25	ns

Notes:

6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCS}, t_{HZOE}, t_{HZR}, and t_{HZWE} are tested with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be reference to the rising edge of the signal that terminates the write.

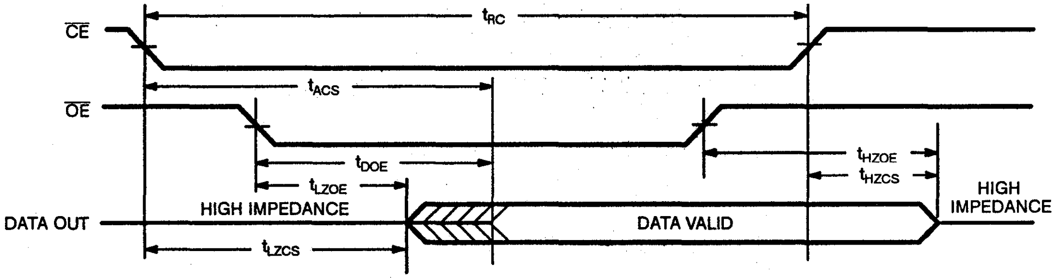
Switching Waveforms

Read Cycle No. 1[9, 10]



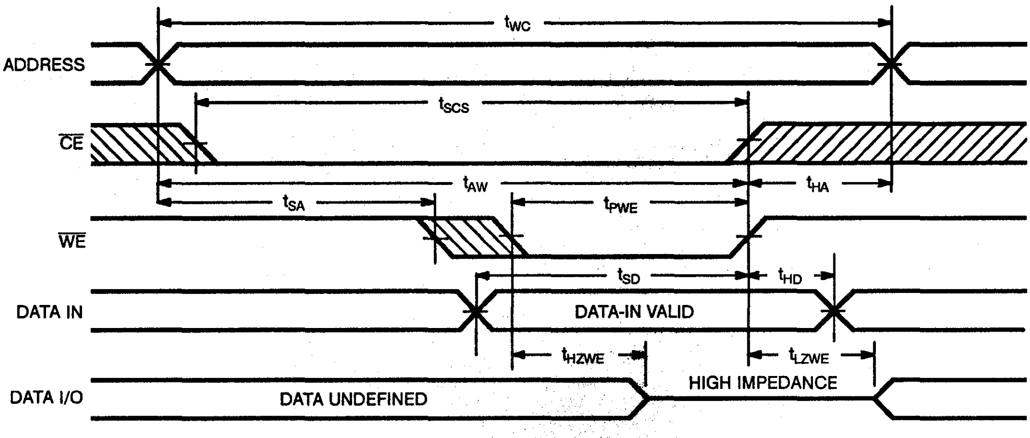
C150-6

Read Cycle No. 2[9, 11]



C150-7

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled) [8]



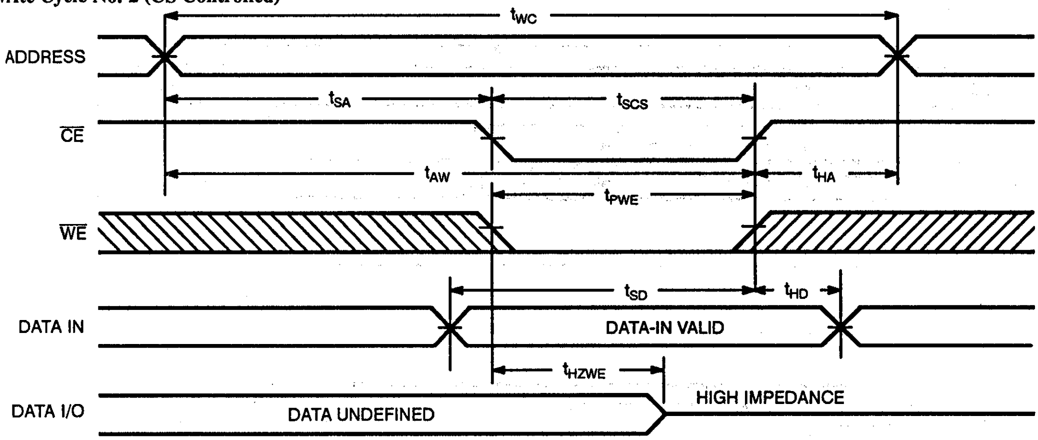
C150-8

Notes:

9. $\overline{\text{WE}}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{\text{CS}}$ and $\overline{\text{OE}}$ = V_{IL}.
11. Address prior to or coincident with $\overline{\text{CS}}$ transition LOW.

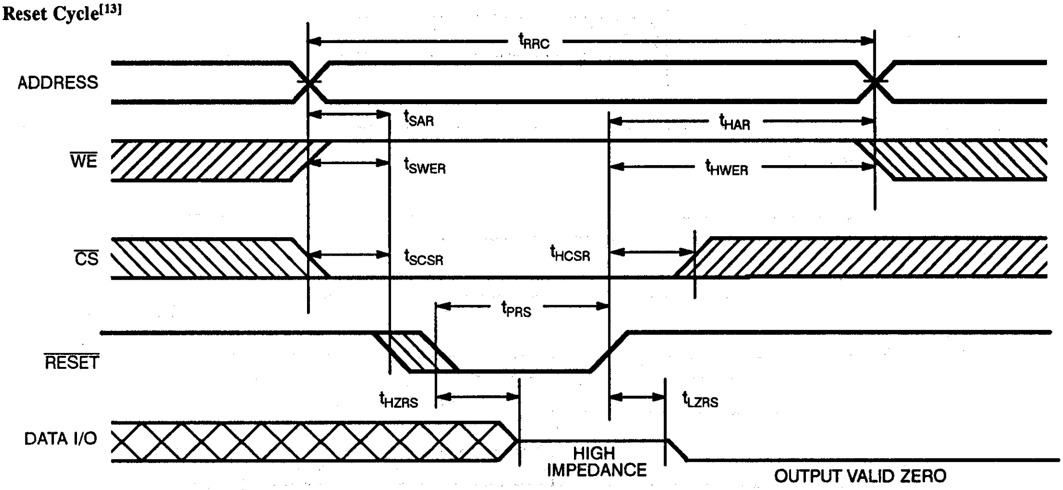
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[8, 12]



C150-9

Reset Cycle[13]



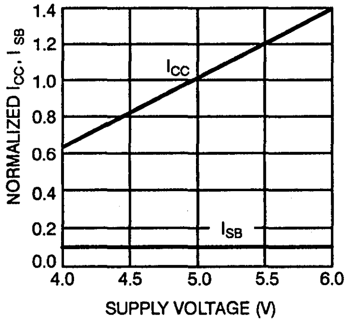
C150-10

Notes:

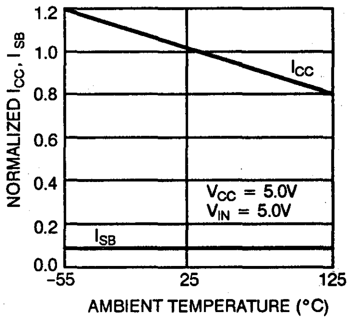
12. If $\overline{CS}$ goes HIGH with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
13. Reset cycle is defined by the overlap of $\overline{RS}$ and $\overline{CS}$ for the minimum reset pulse width.

Typical DC and AC Characteristics

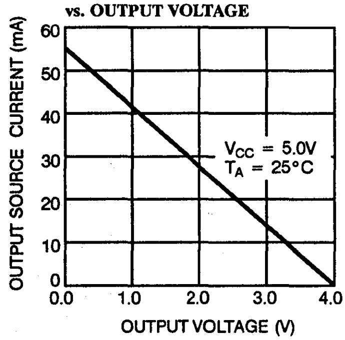
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



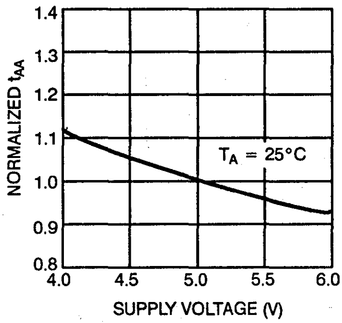
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



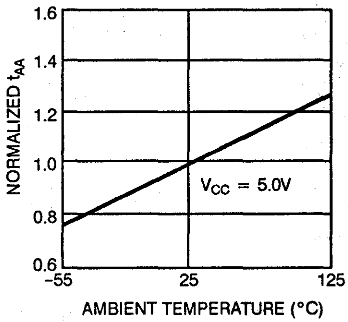
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



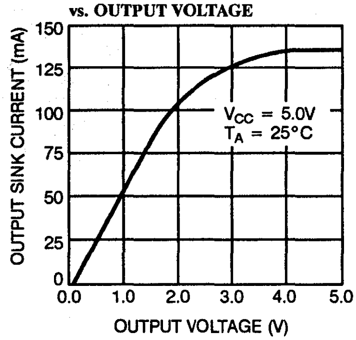
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



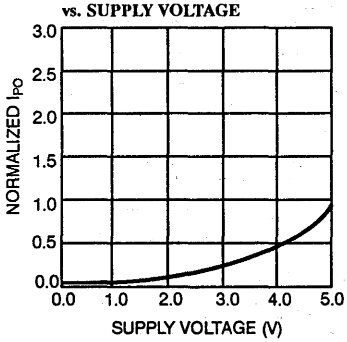
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



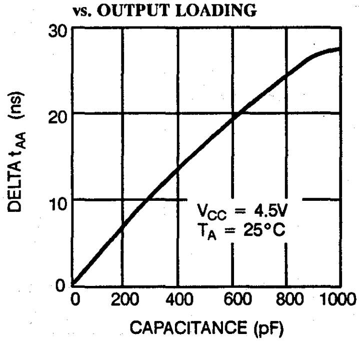
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



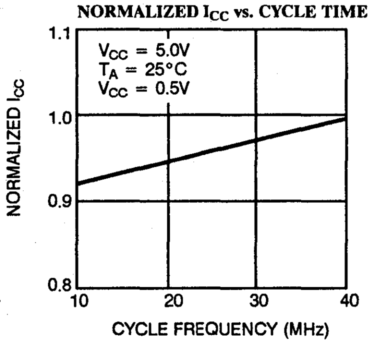
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



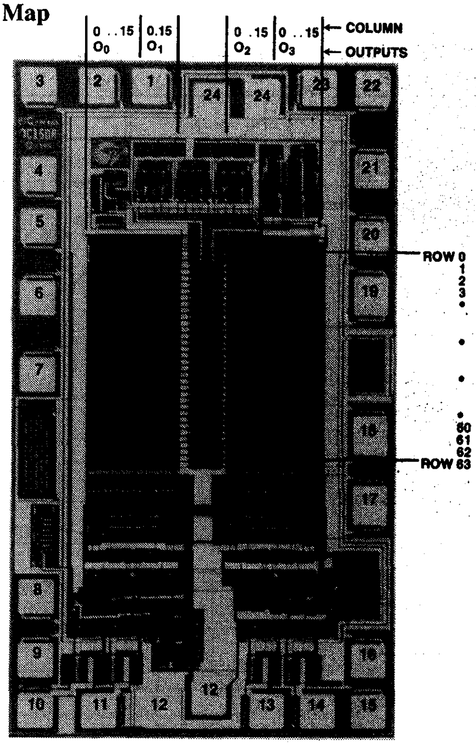
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Bit Map



Address Designators

Address Name	Address Function	Pin Number
A_0	X_0	21
A_1	X_1	22
A_2	X_2	23
A_3	X_3	1
A_4	X_4	2
A_5	X_5	3
A_6	Y_0	4
A_7	Y_1	5
A_8	Y_2	6
A_9	Y_3	7

Truth Table

Inputs				Outputs	Mode
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{RS}$		
H	X	X	X	High Z	Not Selected
L	H	X	L	High Z	Reset
L	L	X	H	High Z	Write
L	H	L	H	O_0—O_3	Read
L	X	H	H	High Z	Output Disable

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7C150-10PC	P13A	Commercial
	CY7C150-10DC	D14	
	CY7C150-10LC	L54	
	CY7C150-10SC	S13	
12	CY7C150-12PC	P13A	Commercial
	CY7C150-12DC	D14	
	CY7C150-12LC	L54	
	CY7C150-12SC	S13	
	CY7C150-12DMB	D14	Military
	CY7C150-12LMB	L54	
15	CY7C150-15PC	P13A	Commercial
	CY7C150-15DC	D14	
	CY7C150-15LC	L54	
	CY7C150-15SC	S13	
	CY7C150-15DMB	D14	Military
	CY7C150-15LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C150-25PC	P13A	Commercial
	CY7C150-25DC	D14	
	CY7C150-25LC	L54	
	CY7C150-25SC	S13	
	CY7C150-25DMB	D14	Military
	CY7C150-25LMB	L54	
35	CY7C150-35PC	P13A	Commercial
	CY7C150-35DC	D14	
	CY7C150-35LC	L54	
	CY7C150-35SC	S13	
	CY7C150-35DMB	D14	Military
	CY7C150-35LMB	L54	

2

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
RESET CYCLE	
t_{RRC}	7, 8, 9, 10, 11
t_{SAR}	7, 8, 9, 10, 11
t_{SWER}	7, 8, 9, 10, 11
t_{SCSR}	7, 8, 9, 10, 11
t_{PRS}	7, 8, 9, 10, 11
t_{HCSR}	7, 8, 9, 10, 11
t_{HWER}	7, 8, 9, 10, 11
t_{HAR}	7, 8, 9, 10, 11

Document #: 38-00028-B

16,384 x 16 Static R/W RAM

Features

- Optimized for use with CY7C600 SPARC product family
- Address and $\overline{WE}$ registers
- CMOS for optimum speed/power
- High speed
  - 20 ns
- Data In and Data Out latches
- Self-timed write
- Common I/O
- Capable of withstanding greater than 2001V electrostatic discharge
- TTL-compatible inputs and outputs

Functional Description

The CY7C157 is a high-performance CMOS static RAM organized as 16,384 x 16 bits. It is intended specifically for use as a high-speed cache memory device with the CY7C600 SPARC™ family of devices. The CY7C157 employs common I/O architecture and a self-timed byte write mechanism.

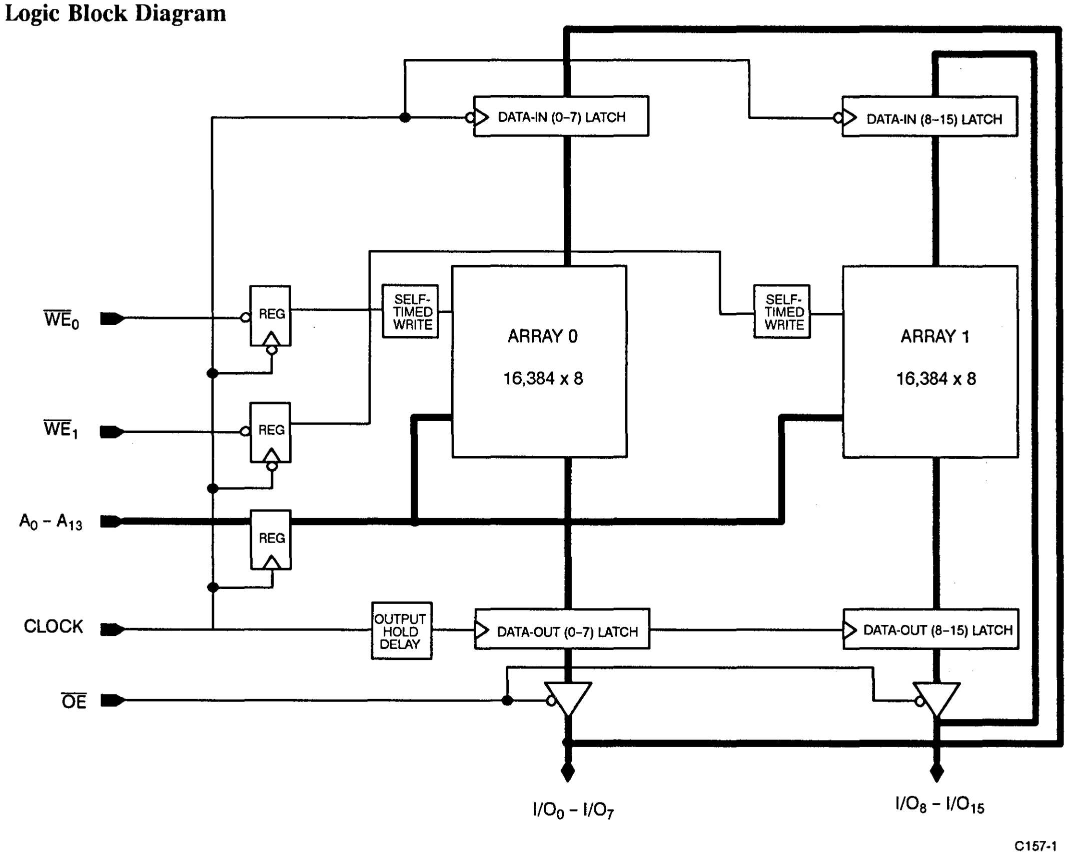
Reading the device is accomplished by taking $\overline{WE}$ HIGH and $\overline{OE}$ LOW. On the rising edge of CLOCK, addresses A_0 through A_{13} are loaded into the input registers. A memory access occurs, and data is held after a read cycle beyond the next rising edge of CLOCK in order to meet the hold time requirements of the microprocessor.

To write the device correctly, $\overline{OE}$ must be taken HIGH. If the falling edge of CLOCK samples either or both of $\overline{WE}_0$ or $\overline{WE}_1$ LOW, a self-timed byte write mechanism is triggered. Data is written from the data-in latch into the memory array at the corresponding address.

Note that the $\overline{OE}$ signal must be HIGH for a proper write because the $\overline{WE}_0$ and $\overline{WE}_1$ signals do not tri-state the outputs.

A die coat is used to insure alpha immunity.

Logic Block Diagram

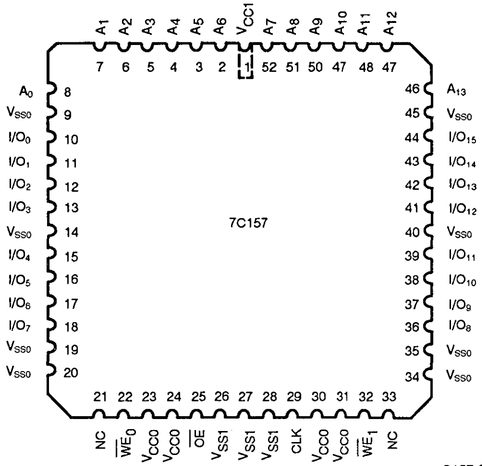


Pin Timing Cross Reference

Pin Name	Timing Reference	Description
Clock	C	Clock Inputs
$A_0 - A_{13}$	A	Address Inputs
$I/O_0 - I/O_{15}$ (Input)	D	Data Inputs
$I/O_0 - I/O_{15}$ (Output)	Q	Data Outputs
$\overline{WE}_0$, $\overline{WE}_1$, $\overline{WE}_X$	W	Write Enable
$\overline{OE}$	G	Output Enable

Pin Diagram

LCC and PLCC
Top View



C157-2

Selection Guide

		7C157-20	7C157-24	7C157-33
Maximum Clock to Output (ns)	Commercial	20	24	33
	Military		24	33
Maximum Output Enable to Output Time (ns)	Commercial	8	10	15
	Military		10	15
Maximum Current (mA)	Commercial	250	250	250
	Military		300	300

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 50 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

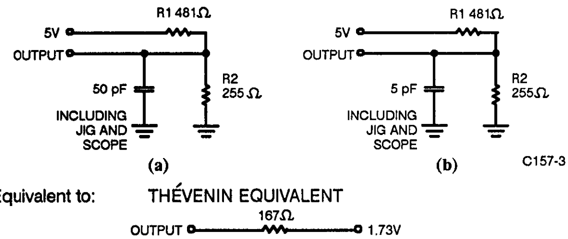
Electrical Characteristics Over the Operating Range[2]

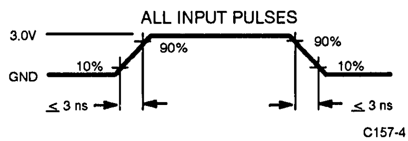
Parameters	Description	Test Conditions		7C157-20 Min.	7C157-20 Max.	7C157-24 Min.	7C157-24 Max.	7C157-33 Min.	7C157-33 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 8.0 mA			0.5		0.5		0.5	V
V_{IH}	Input HIGH Voltage			2.1	V_{CC}	2.1	V_{CC}	2.1	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND < V_I < V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND < V_O < V_{CC}, Output Disabled		−50	+50	−50	+50	−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		250		250		250	mA
			Military				300		300	

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms





Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at a time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

2

Switching Characteristics Over the Operating Range[2, 5]

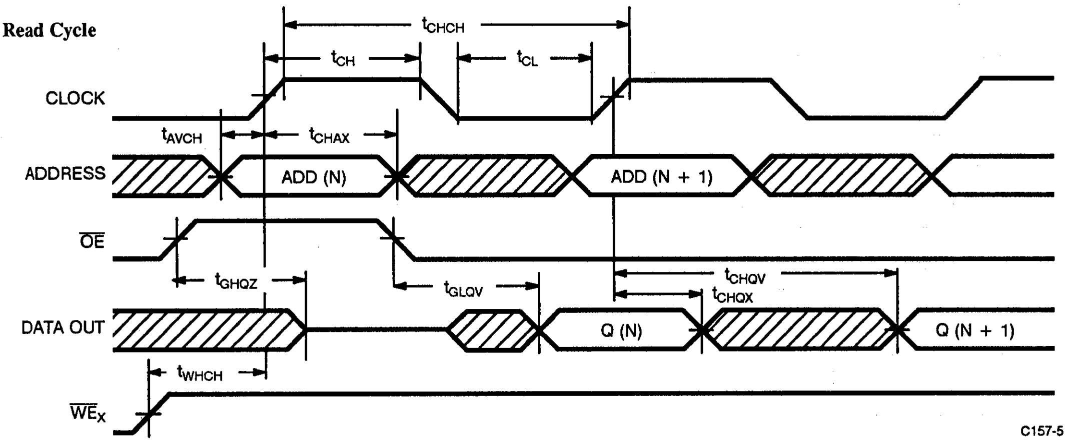
Parameters	Description	7C157-20[6]		7C157-24[6]		7C157-33		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE[7, 8]								
t_{CHCH}	Clock Cycle Time	25		30		40		ns
t_{CH}	Clock HIGH Time	11		13		18		ns
t_{CL}	Clock LOW Time	11		13		18		ns
t_{CHQV}	Clock HIGH to Output Valid		20		24		33	ns
t_{CHQX}	Output Data Hold	5		5		5		ns
t_{WHCH}	$\overline{WE}_X$ HIGH to Next Clock HIGH	2		2		3		ns
t_{GLQV}	$\overline{OE}$ LOW to Output Valid	0	8	0	10	0	15	ns
t_{GHQZ}	$\overline{OE}$ HIGH to Output Tristate	0	8	0	10	0	15	ns
t_{GHCH}	$\overline{OE}$ HIGH to Next Clock HIGH	7		7		7		ns
t_{AVCH}	Address Set-Up	2		2		3		ns
t_{CHAX}	Address Hold	6		6		6		ns
WRITE CYCLE[9]								
t_{CHCH}	Clock Cycle Time[10]	25		30		40		ns
t_{CH}	Clock HIGH Time	11		13		18		ns
t_{CL}	Clock LOW Time	11		13		18		ns
t_{GHQZ}	$\overline{OE}$ HIGH to Output Tristate	0	8	0	10	0	15	ns
t_{GHCH}	$\overline{OE}$ HIGH to Next Clock HIGH	7		7		7		ns
t_{DVCL}	Data in Set-Up to Clock	6		6		7		ns
t_{CLDX}	Data in Hold from Clock	2		2		2		ns
t_{WLCL}	$\overline{WE}_X$ LOW to Clock LOW[11, 12]	2		2		3		ns
t_{CLWH}	Clock LOW to $\overline{WE}_X$ HIGH[11,12]	6		6		7		ns
t_{AVCH}	Address Set-Up	2		2		3		ns
t_{CHAX}	Address Hold	6		6		6		ns

Notes:

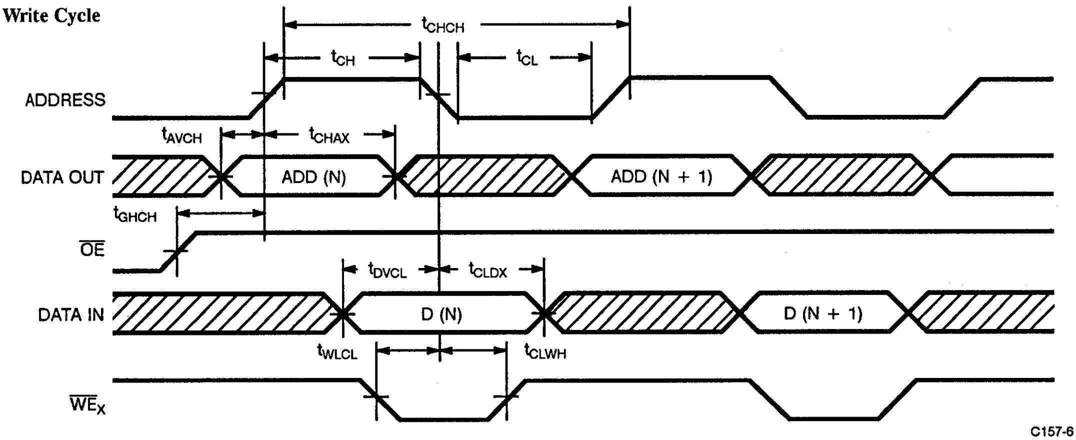
5. Test conditions assume signal transition times of 5 ns or less, timing referenece levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 50-pF load capacitance.
6. Surface mount package only.
7. $\overline{WE}$ is HIGH for read cycle.
8. $\overline{OE}$ is selected (LOW).
9. $\overline{OE}$ must be HIGH for data-in to propagate to latch.
10. t_{GHQZ} is tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
11. Self-Timed Write is triggered on falling edge of registered $\overline{WE}_0$ or $\overline{WE}_1$ signals.
12. X = 0 or 1 for low byte and high byte, respectively.

Switching Waveforms

Read Cycle



Write Cycle



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C157-20LC	L69	Commercial
	CY7C157-20JC	J69	
24	CY7C157-24LC	L69	Commercial
	CY7C157-24JC	J69	
	CY7C157-24LMB	L69	Military
33	CY7C157-33LC	L69	Commercial
	CY7C157-33JC	J69	
	CY7C157-33LMB	L69	Military

Truth Table

Inputs			Outputs
$\overline{OE}$	$\overline{WE_0}$ (↓CLOCK)	$\overline{WE_1}$ (↓CLOCK)	
X	X	X	High Z
H	H	H	High Z
L	H	H	$I/O_0 - I/O_{15}$
H	L	H	$I/O_0 - I/O_7$
H	H	L	$I/O_8 - I/O_{15}$
H	L	L	$I/O_0 - I/O_{15}$

2

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{CHCH}	7, 8, 9, 10, 11
t_{CHQV}	7, 8, 9, 10, 11
t_{GHQZ}	7, 8, 9, 10, 11
t_{CHQX}	7, 8, 9, 10, 11
t_{GHQV}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{CHCH}	7, 8, 9, 10, 11
t_{DVCL}	7, 8, 9, 10, 11
t_{AVCH}	7, 8, 9, 10, 11
t_{CHAX}	7, 8, 9, 10, 11
t_{CLDX}	7, 8, 9, 10, 11
t_{DVWL}	7, 8, 9, 10, 11
t_{WLDX}	7, 8, 9, 10, 11

Document #: 38-00028-B

PRELIMINARY **CY7B160**

CYPRESS SEMICONDUCTOR

Expandable 16,384 x 4 Static RAM

Features

- **High speed**
  - **12 ns t_{AA}**
- **Output Enable ($\overline{OE}$) feature**
- **Five Chip Enables ($\overline{CE}_{1,2,3}$ and $CE_{4,5}$) to expand memory**
- **BiCMOS for optimum speed/power**
- **Low active power**
  - **600 mW**
- **Low standby power**
  - **200 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge.**

Functional Description

The CY7B160 is a high-performance BiCMOS static RAM organized as 16,348 x 4 bits. A memory expansion feature is provided to save access time by eliminating the need for an external decoder when stacking CY7B160s. Five chip enable inputs ($\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$, CE_4, and CE_5) make it easy to increase memory depth with up to four CY7B160s. The primary chip enable ($\overline{CE}_1$) can be used to enable or power down all four devices together while chip enables $\overline{CE}_2$, $\overline{CE}_3$, CE_4, and CE_5 can be used as extra address pins to enable or power down each device individually.

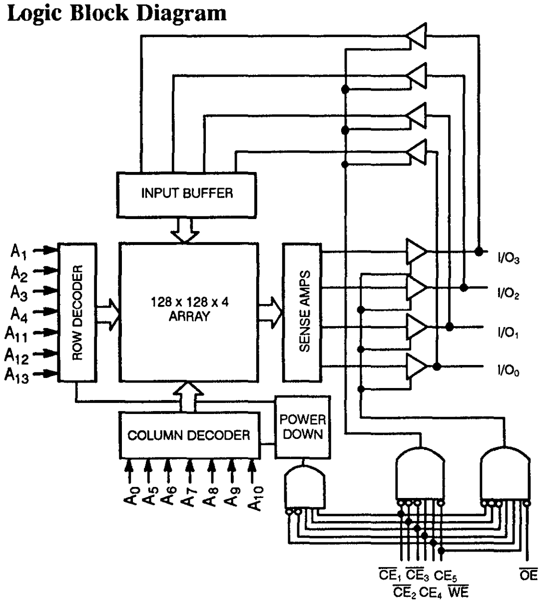
Memory expansion is facilitated by three-state drivers and an active LOW output enable ($\overline{OE}$). The device has a power-down feature, reducing the power consumption by 67% when deselected by any CE input.

Writing to the device is accomplished when $\overline{CE}_{1,2,3}$ and $\overline{WE}$ inputs are LOW while $CE_{4,5}$ inputs are HIGH. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

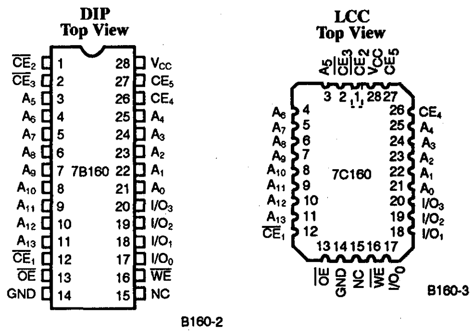
Reading the device is accomplished by taking chip enables $\overline{CE}_{1,2,3}$ LOW and $\overline{OE}$ LOW while write enable ($\overline{WE}$) and chip enables $CE_{4,5}$ remain HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when $\overline{CE}_{1,2,3}$ or $\overline{OE}$ is HIGH, or when $\overline{WE}$ or $CE_{4,5}$ are LOW.

Logic Block Diagram



Pin Configurations



Selection Guide

		7B160–12	7B160–15
Maximum Access Time (ns)		12	15
Maximum Operating Current (mA)	Commercial	120	115
	Military		135
Maximum Standby Current (mA)	Commercial	40	40
	Military		50

Maximum Rating

(Above which the useful life may be impaired. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State......................... −0.5V to +7.0V

DC Input Voltage[1] .... −3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current............................ > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[2]	− 55°C to + 125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[3]

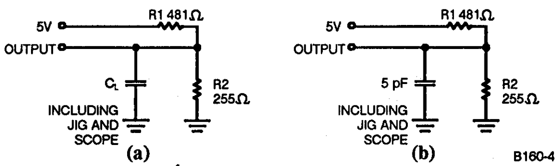
Parameters	Description	Test Conditions		7B160-12 Min.	7B160-12 Max.	7B160-15 Min.	7B160-15 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = − 4.0 mA (Com'l)	2.4		2.4		V
			I_{OH} = − 2.0 mA (Mil)					
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_O \leq V_{CC}$		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled		−10	+10	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA f = f max.	Com'l		120		115	mA
			Mil				135	
I_{SB}	$\overline{CE}$ Power-Down Current	($\overline{CE}_1$, or $\overline{CE}_2$, or $\overline{CE}_3$) $\geq V_{IH}$ or (CE_4 or CE_5) $\leq V_{IL}$	Com'l	40		40		mA
			Mil		50		50	

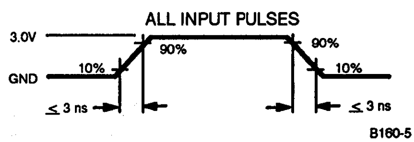
Capacitance[4]

Parameters	Description	Test Conditions	Max.[5]	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
1. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except Cerdip (D22), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.

AC Test Loads and Waveforms





Equivalent to:

Switching Characteristics Over the Operating Range[2, 6]

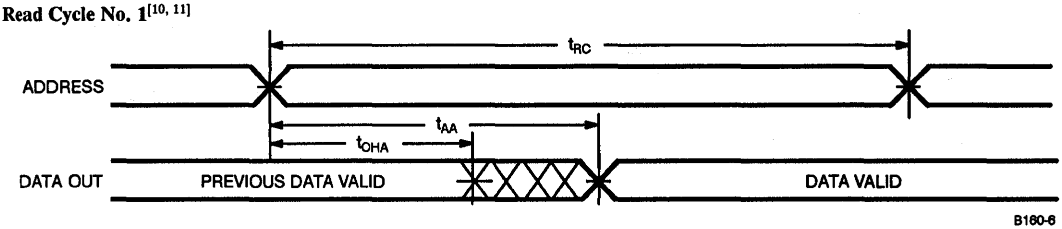
Parameters	Description	7B160-12		7B160-15		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Output Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Data Valid		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		7		8	ns
t_{LZCE}	$\overline{CE}_{1,2,3}$ LOW, $CE_{4,5}$ HIGH to Low Z[8]	3		3		ns
t_{HZCE}	$\overline{CE}_{1,2,3,4,5}$ HIGH to High Z[7, 8]		7		8	ns
WRITE CYCLE[9]						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCE}	$\overline{CE}_{1,2,3}$ LOW and $CE_{4,5}$ HIGH to Write End	8		10		ns
t_{AW}	Address Set-Up to Write End	8		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		ns
t_{SD}	Data Set-Up to Write End	6.5		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]	0	7	0	7	ns

Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and $C_L = 20$ pF.
7. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
8. t_{HZCE}, t_{HZWE}, t_{HZOE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_{1,2,3}$ LOW, $CE_{4,5}$ HIGH, and $\overline{WE}$ LOW. All signals must be in this state to initiate a write and any signal can terminate a write by changing state. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. Data I/O will be high-impedance if $\overline{OE} = V_{IH}$.

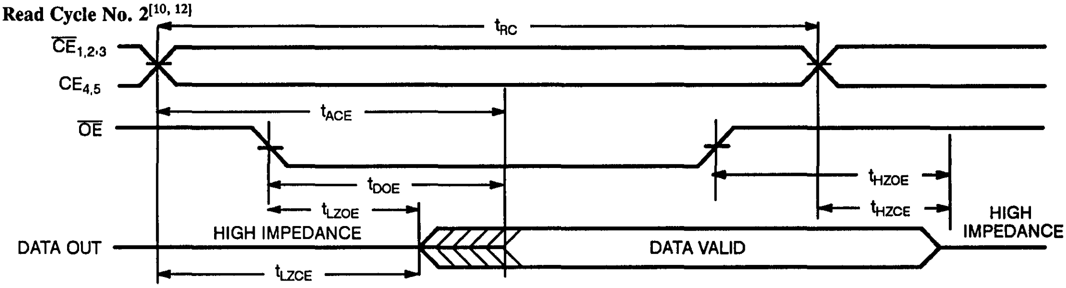
Switching Waveforms

Read Cycle No. 1[10, 11]

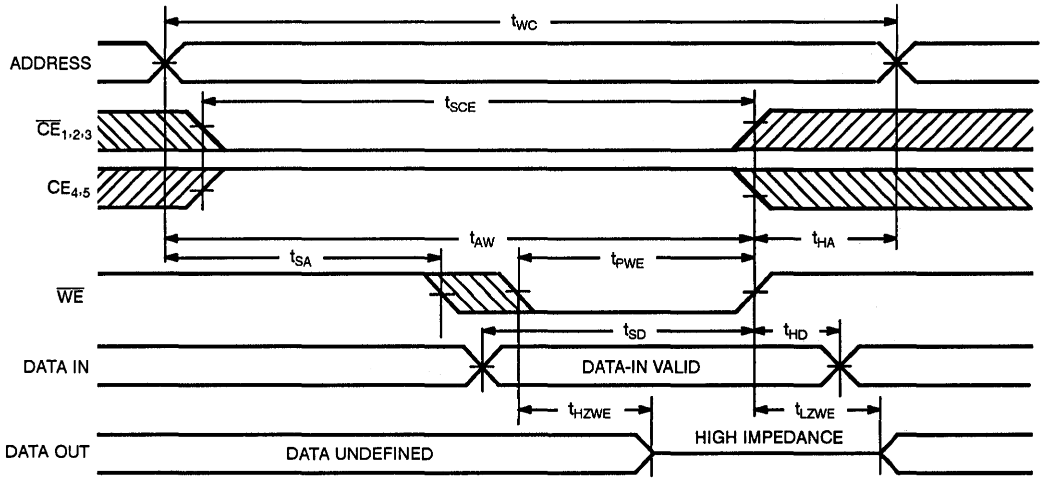


Switching Waveforms (continued)

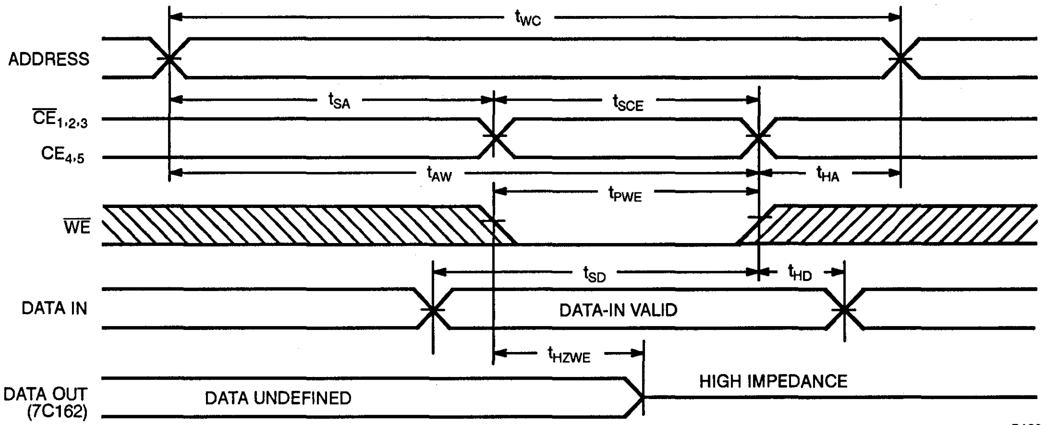
Read Cycle No. 2[10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13]



Write Cycle No. 2 ($\overline{CE}_1$, $\overline{CE}_2$, $\overline{CE}_3$, CE_4, or CE_5 Controlled)[9, 13]



Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$	CE_4	CE_5	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
L	L	L	H	H	H	L	Data Out	Read
L	L	L	H	H	L	X	Data In	Write
L	L	L	H	H	H	H	High Z	Deselect
H	X	X	X	X	X	X	High Z	Deselect Power-Down
X	H	X	X	X	X	X	High Z	Deselect Power-Down
X	X	H	X	X	X	X	High Z	Deselect Power-Down
X	X	X	L	X	X	X	High Z	Deselect Power-Down
X	X	X	X	L	X	X	High Z	Deselect Power-Down

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B160–12VC	V21	Commercial
	CY7B160–12LC	L54	
15	CY7B160–15VC	V21	Commercial
	CY7B160–15DMB	D22	Military
	CY7B160–15LMB	L54	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-A-00021

CYPRESS SEMICONDUCTOR

CY7B161 CY7B162

16,384 x 4 Static RAM Separate I/O

Features

- **High speed**
  - **10 ns t_{AA}**
- **Low active power**
  - **600 mW**
- **Low standby power**
  - **200 mW**
- **Transparent write (7B161)**
- **BiCMOS for optimum speed/power**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge.**

Functional Description

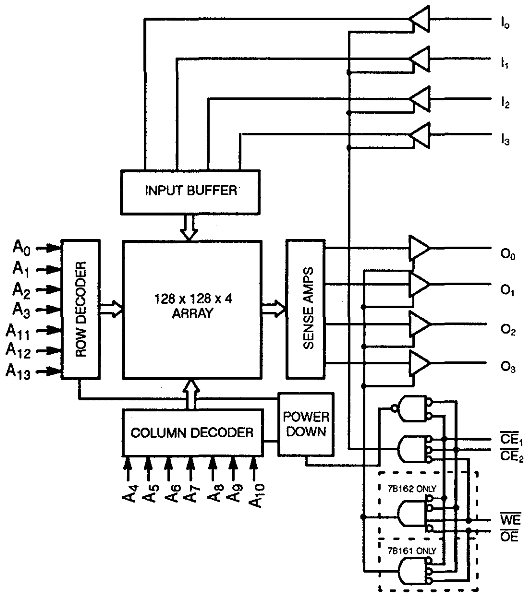
The CY7B161 and CY7B162 are high-performance BiCMOS static RAMs organized as 16,384 by 4 bits with separate I/O. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Easy memory expansion is provided by active LOW chip enables ($\overline{CE_1}$, $\overline{CE_2}$) and three-state drivers. They have a $\overline{CE}$ power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE_1}$, $\overline{CE_2}$) and write enable ($\overline{WE}$) inputs are all LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) and $\overline{OE}$ LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

The output pins remain in high-impedance state when write enable ($\overline{WE}$) is LOW (7B162 only), or one of the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) is HIGH, or $\overline{OE}$ is HIGH.

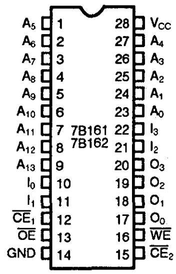
Logic Block Diagram



B161-1

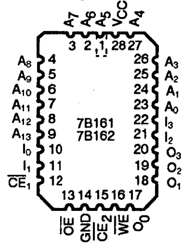
Pin Configurations

DIP Top View



B161-2

LCC Top View



B161-3

Selection Guide

		7B161-10 7B162-10	7B161-12 7B162-12	7B161-15 7B162-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	130	120	
	Military			135
Maximum Standby Current (mA)	Commercial	40	40	
	Military			50

Maximum Rating

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage[1] .... −3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[2]	−55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions			7B161-10 7B162-10 Min.	Max.	7B161-12 7B162-12 Min.	Max.	7B161-15 7B162-15 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = −4.0 mA	Com'l	2.4		2.4		2.4		V
			I_{OH} = −2.0 mA	Mil	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Level[1]				−0.5	0.8	−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$			−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled			−10	+10	−10	+10	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = $f_{max.}$		Com'l		130		120			mA
				Mil						135	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current	$\overline{CE} \geq V_{IH}$		Com'l		40		40			mA
				Mil						50	

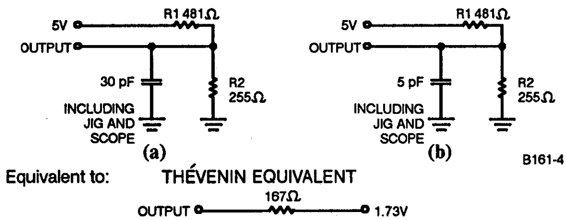
Capacitance[4]

Parameters	Description	Test Conditions	Max.[5]	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

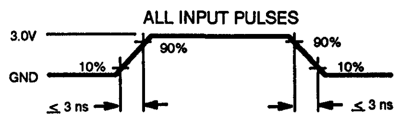
Notes:

1. V_{IL} (min.) = −3.0V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except Cerdip (D22), which has maximums of C_{IN} = 8 pF and C_{OUT} = 9 pF.

AC Test Loads and Waveforms



B161-4



B161-5

Switching Characteristics Over the Operating Range[3, 6, 7]

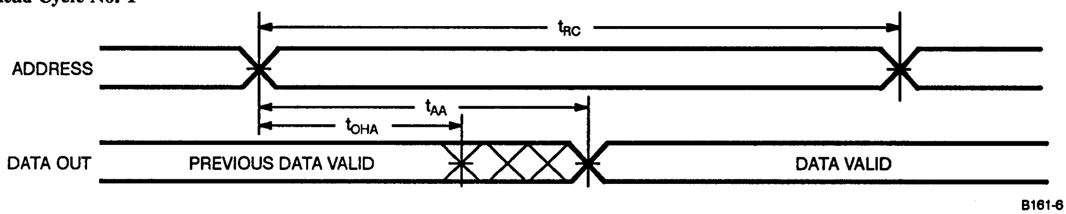
Parameters	Description	7B161-10 7B162-10		7B161-12 7B162-12		7B161-15 7B162-15		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Output Hold from Address Change	2		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		7		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8]		7		7		8	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	2		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		7		7		8	ns
WRITE CYCLE[10]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		8		10		ns
t_{AW}	Address Set-Up to Write End	8		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		8		10		ns
t_{SD}	Data Set-Up to Write End	6		6.5		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[9] (7B162)	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9] (7B162)		7		7		7	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7B161)		10		12		15	ns
t_{ADV}	Data Valid to Output Valid (7B161)		10		12		15	ns

Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and C_L = 20 pF.
7. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms section.
8. t_{HZCE}, t_{HZOE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady state voltage.
9. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CE}_1$ and $\overline{CE}_2$ transtion LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7B162 only).

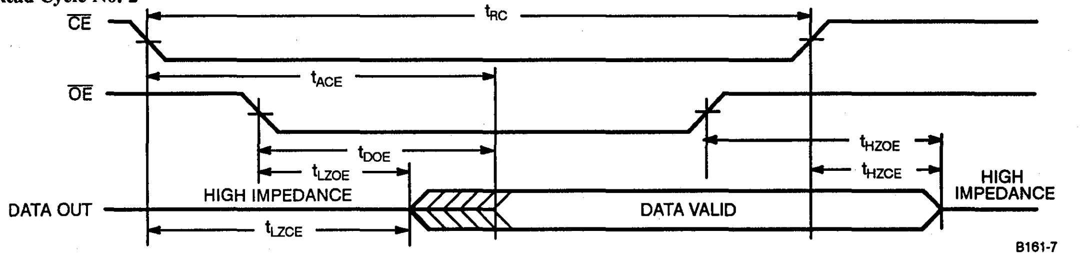
Switching Waveforms[7]

Read Cycle No. 1[11, 12]

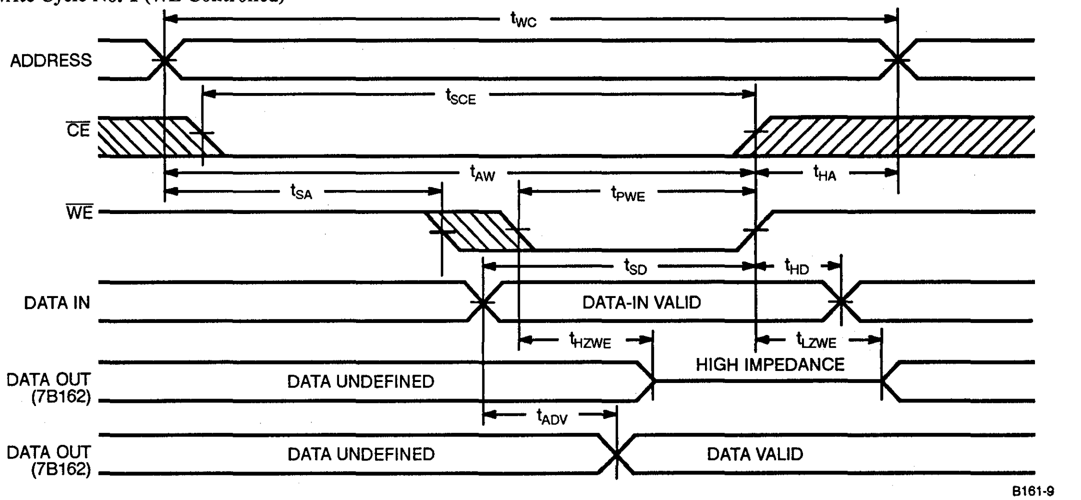


Switching Waveforms[6]

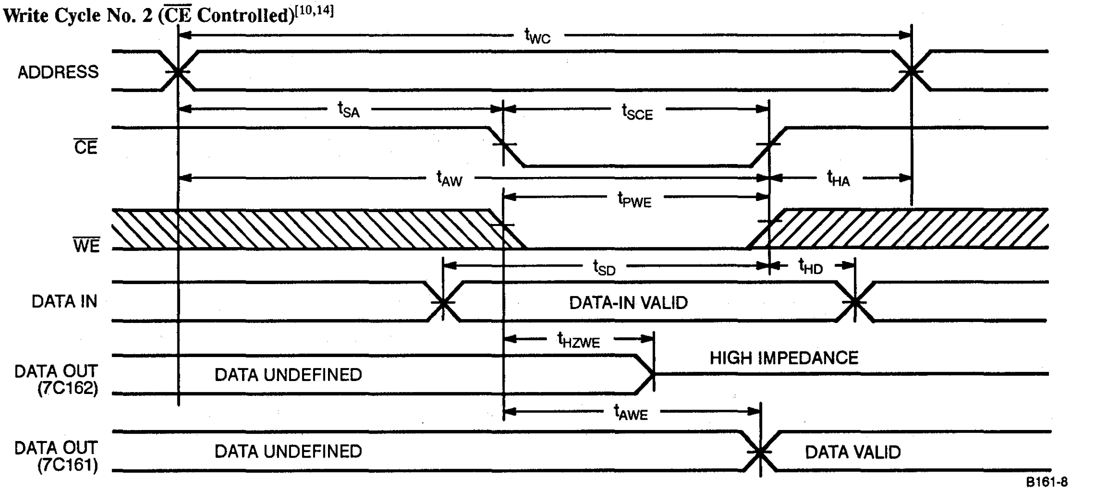
Read Cycle No. 2[11, 13]



Write Cycle No. 1 (WE Controlled)[10]



Write Cycle No. 2 (CE Controlled)[10,14]



7B161 Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Outputs	Inputs	Mode
H	X	X	X	High Z	X	Deselect/Power-Down
X	H	X	X	High Z	X	Deselect/Power-Down
L	L	H	L	Data Out	X	Read
L	L	L	L	Data In	Data In	Write
L	L	L	H	High Z	Data In	Write
L	L	H	H	High Z	X	Deselect

7B162 Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Outputs	Inputs	Mode
H	X	X	X	High Z	X	Deselect/Power-Down
X	H	X	X	High Z	X	Deselect/Power-Down
L	L	H	L	Data Out	X	Read
L	L	L	X	High Z	Data In	Write
L	L	H	H	High Z	X	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7B161–10VC	V21	Commercial
12	CY7B161–12PC	P21	Commercial
	CY7B161–12VC	V21	
	CY7B161–12DC	D22	
15	CY7B161–15DMB	D22	Military
	CY7B161–15LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7B162–10VC	V21	Commercial
12	CY7B162–12PC	P21	Commercial
	CY7B162–12VC	V21	
	CY7B162–12DC	D22	
15	CY7B162–15DMB	D22	Military
	CY7B162–15LMB	L54	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[15]	7, 8, 9, 10, 11
t_{ADV}[15]	7, 8, 9, 10, 11

Note:
15. 7B161 only.

Document #: 38-A-00014-A

CYPRESS SEMICONDUCTOR

16,384 x 4 Static R/W RAM Separate I/O

Features

- Automatic power-down when deselected
- Transparent write (7C161)
- CMOS for optimum speed/power
- High speed
  - 15 ns t_{AA}
- Low active power
  - 633 mW
- Low standby power
  - 220 mW
- TTL compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge.

Functional Description

The CY7C161 and CY7C162 are high-performance CMOS static RAMs organized as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE_1}$, $\overline{CE_2}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 65% when deselected.

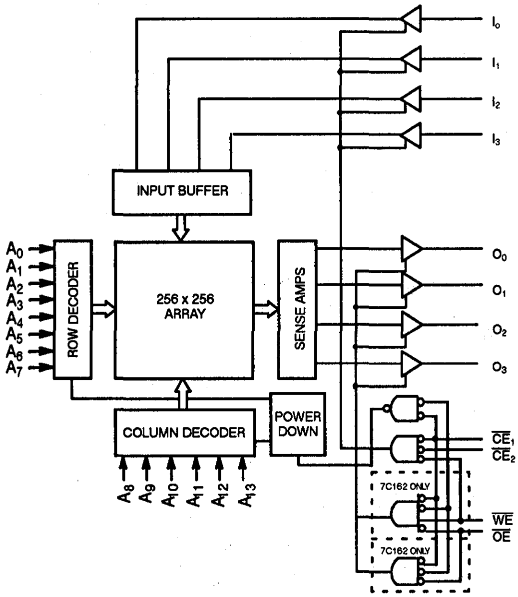
Writing to the device is accomplished when the chip enable ($\overline{CE_1}$, $\overline{CE_2}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C162 only), or one of the chip enables ($\overline{CE_1}$, $\overline{CE_2}$) are HIGH.

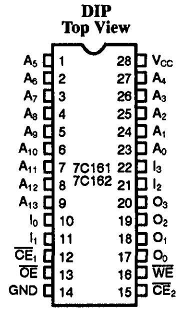
A die coat is used to insure alpha immunity.

Logic Block Diagram

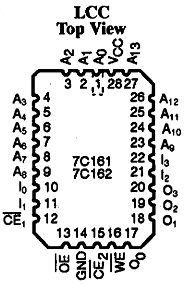


C162-1

Pin Configurations



C162-2



C162-3

Selection Guide

	7C161-20 7C162-20	7C161-25 7C162-25	7C161-35 7C162-35	7C161-45 7C162-45
Maximum Access Time (ns)	20	25	35	45
Maximum Operating Current (mA)	80	70	70	50
Maximum Standby Current (mA)	40/20	20/20	20/20	20/20

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C161-15 7C162-15		7C161-20 7C162-20		7C161-25,35 7C162-25,35		7C161-45 7C162-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		-3.0	0.8	-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	-10	+10	-10	+10	-10	+10	-10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled	-10	+10	-10	+10	-10	+10	-10	+10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND		-350		-350		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		115		80		70		50	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$ Min. Duty Cycle = 100%		40		40		20		20	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		20		20		20		20	mA

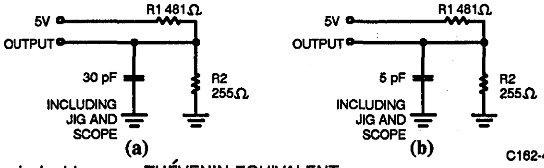
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

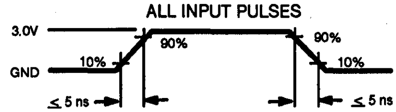
Notes:

1. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested initially and after any design or process changes that may affects these parameters.

AC Test Loads and Waveforms

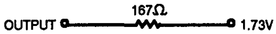


C162-4



C162-5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4, 5]

Parameters	Description	7C161–15 7C162–15 Min.	Max.	7C161–20 7C162–20 Min.	Max.	7C161–25 7C162–25 Min.	Max.	7C161–35 7C162–35 Min.	Max.	7C161–45 7C162–45 Min.	Max.	Units
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		8		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6] (7C162)	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 9] (7C162)		7		7		7		10		15	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C161)		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C161)		15		20		20		30		35	ns

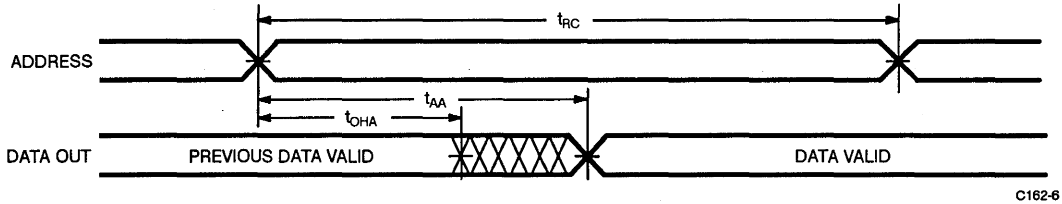
Notes:

4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms sections.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.

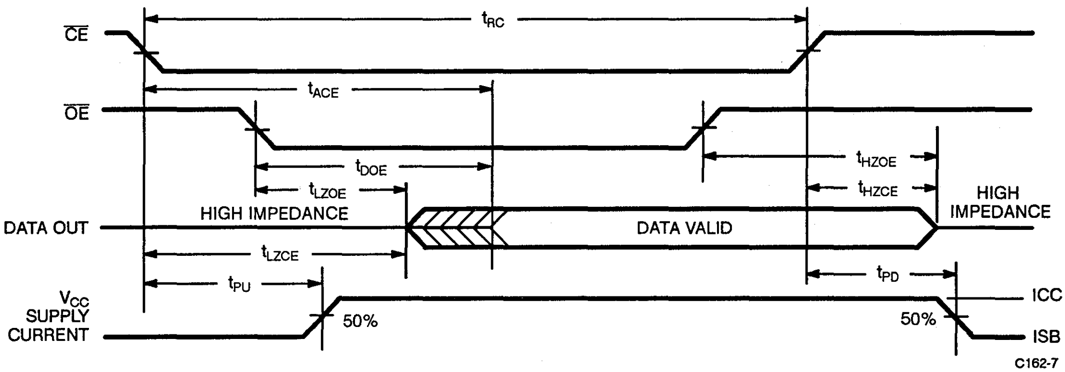
2

Switching Waveforms[7]

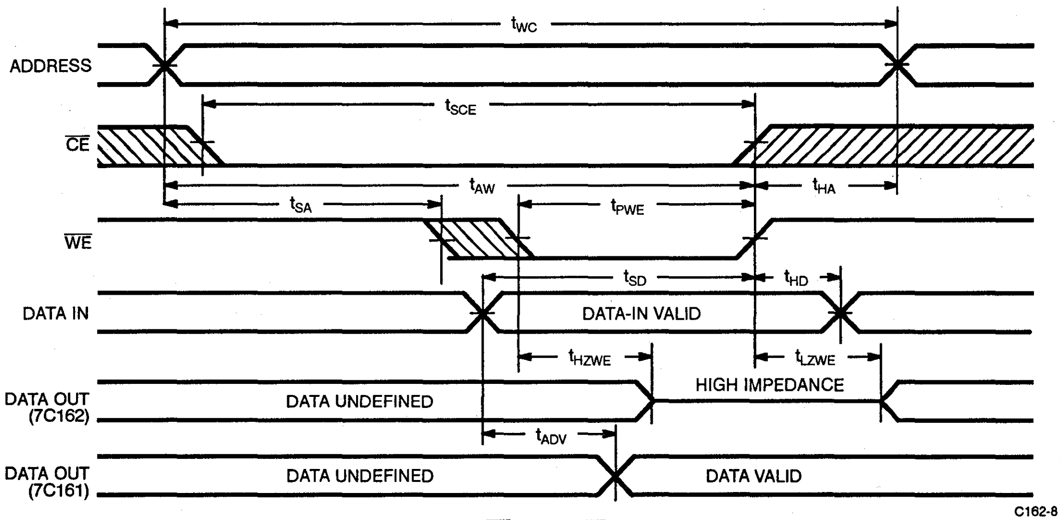
Read Cycle No. 1[9, 10]



Read Cycle No. 2[9, 11]



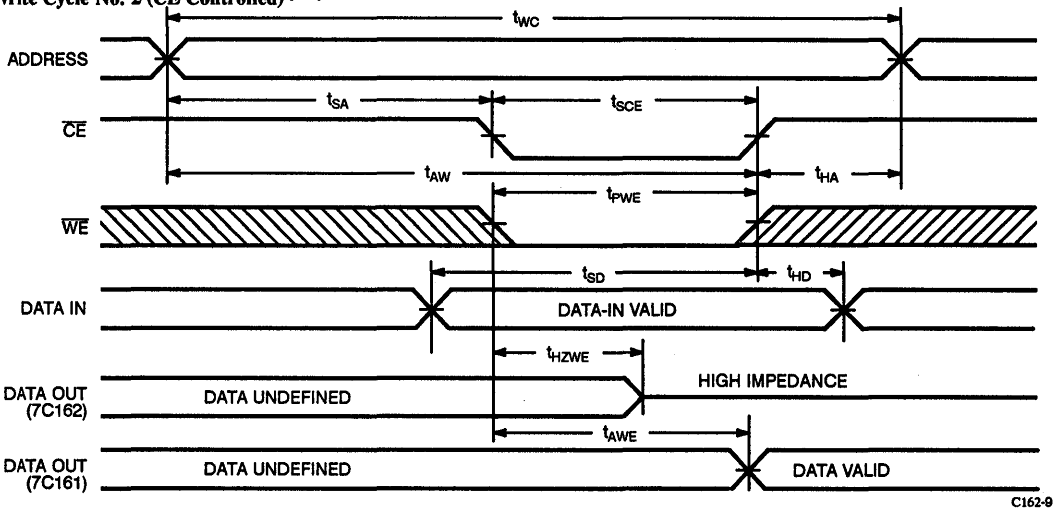
Write Cycle No. 1 (WE Controlled)[8]



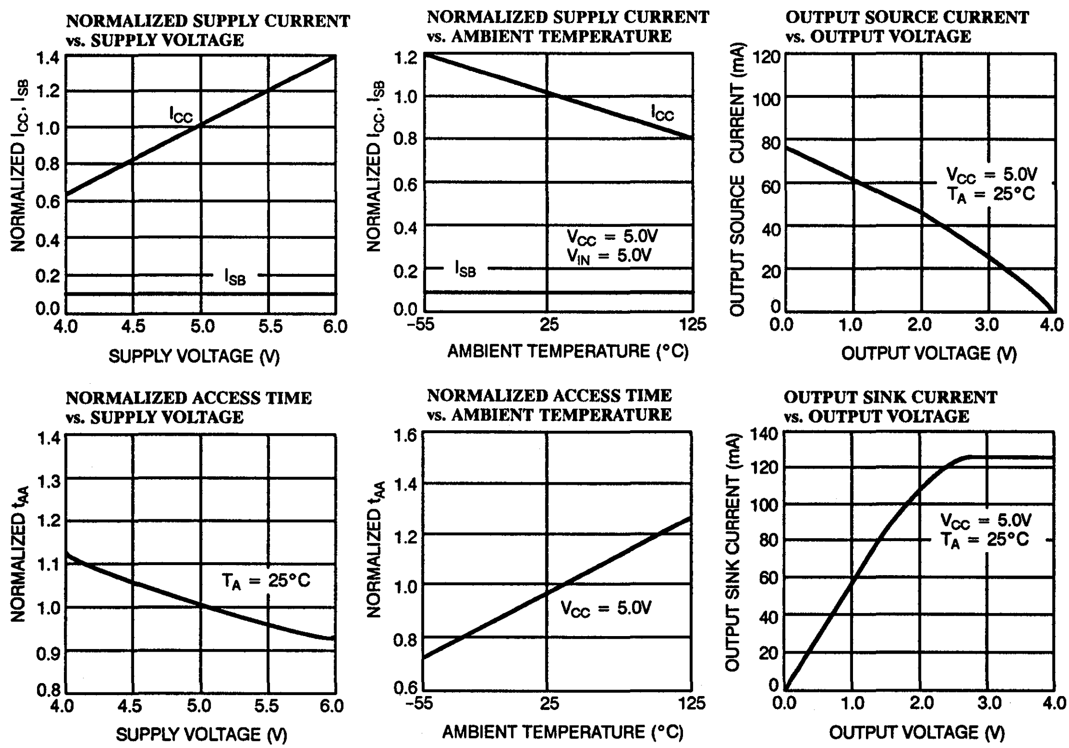
8. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{CE}_2$ transition LOW.
12. if $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C162 only).

Switching Waveforms[7] (continued)

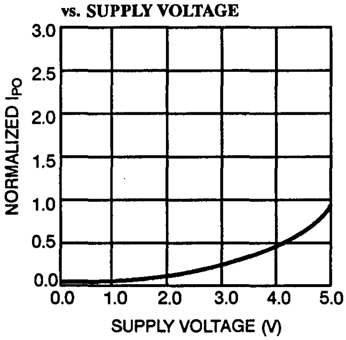
Write Cycle No. 2 ($\overline{CE}$ Controlled) [8,12]

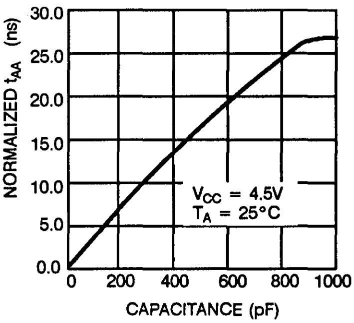


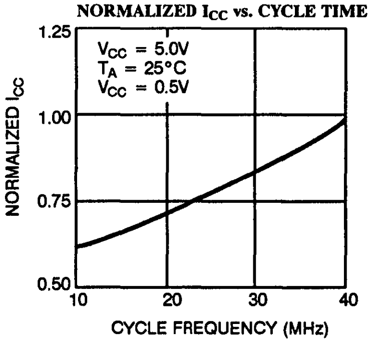
Typical DC and AC Characteristics



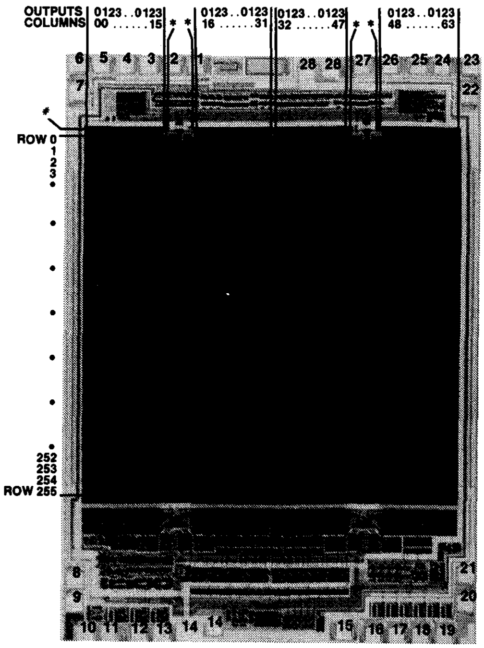
Typical DC and AC Characteristics (continued)







Bit Map



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C161–15PC	P21	Commercial
	CY7C161–15VC	V21	
	CY7C161–15DC	D22	
	CY7C161–15LC	L54	
20	CY7C161–20PC	P21	Commercial
	CY7C161–20VC	V21	
	CY7C161–20DC	D22	
	CY7C161–20LC	L54	
25	CY7C161–25PC	P21	Commercial
	CY7C161–25VC	V21	
	CY7C161–25DC	D22	
	CY7C161–25LC	L54	
35	CY7C161–35PC	P21	Commercial
	CY7C161–35VC	V21	
	CY7C161–35DC	D22	
	CY7C161–35LC	L54	
45	CY7C161–45PC	P21	Commercial
	CY7C161–45VC	V21	
	CY7C161–45DC	D22	
	CY7C161–45LC	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C162–15PC	P21	Commercial
	CY7C162–15VC	V21	
	CY7C162–15DC	D22	
	CY7C162–15LC	L54	
20	CY7C162–20PC	P21	Commercial
	CY7C162–20VC	V21	
	CY7C162–20DC	D22	
	CY7C162–20LC	L54	
25	CY7C162–25PC	P21	Commercial
	CY7C162–25VC	V21	
	CY7C162–25DC	D22	
	CY7C161–25LC	L54	
35	CY7C162–35PC	P21	Commercial
	CY7C162–35VC	V21	
	CY7C162–35DC	D22	
	CY7C162–35LC	L54	
45	CY7C162–45PC	P21	Commercial
	CY7C162–45VC	V21	
	CY7C162–45DC	D22	
	CY7C162–45LC	L54	

Document #: 38–00029

CYPRESS SEMICONDUCTOR

16,384 x 4 Static R/W RAM Separate I/O

Features

- **Automatic power-down when deselected**
- **Transparent write (7C161A)**
- **CMOS for optimum speed/power**
- **High speed**
  - **15 ns t_{AA}**
- **Low active power**
  - **550 mW**
- **Low standby power**
  - **220 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge.**

Functional Description

The CY7C161A and CY7C162A are high-performance CMOS static RAMs organizes as 16,384 by 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enables ($\overline{CE}_1$, $\overline{CE}_2$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 60% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}_1$, $\overline{CE}_2$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

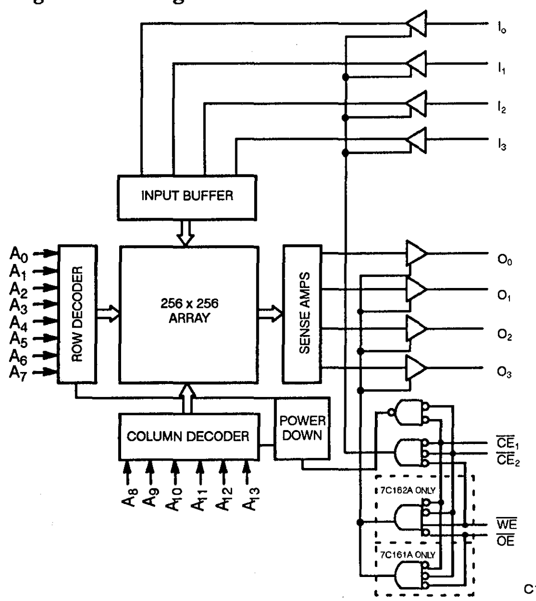
Reading the device is accomplished by taking the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C162A only), or one of the chip enables ($\overline{CE}_1$, $\overline{CE}_2$) are HIGH.

A die coat is used to insure alpha immunity.

2

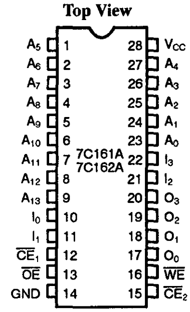
Logic Block Diagram



C161A-1

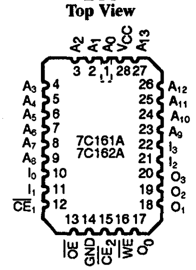
Pin Configurations

DIP
Top View



C161A-2

LCC
Top View



C161A-3

Selection Guide

		7C161A-15 7C162A-15	7C161A-20 7C162A-20	7C161A-25 7C162A-25	7C161A-35 7C162A-35	7C161A-45 7C162A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	100	100	100	100
	Military		100	100	100	100
Maximum Standby Current (mA)	Commercial	40/20	20	30/20	30/20	30/20
	Military		40/20	40/20	30/20	30/20

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

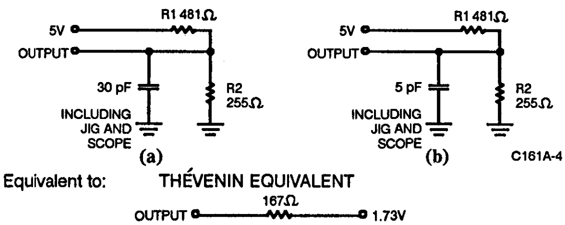
Parameters	Description	Test Conditions		7C161A-15 7C162A-15 Min.	Max.	7C161A-20 7C162A-20 Min.	Max.	7C161A-25 7C162A-25 Min.	Max.	7C161A-35,45 7C162A-35,45 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			-3.0	0.8	-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		− 10	+ 10	− 10	+ 10	-10	+ 10	-10	+ 10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		− 10	+ 10	− 10	+ 10	-10	+ 10	-10	+ 10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			-350		-350		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		115		100		100		100	mA
			Mil				100		100		100	
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Com'l		40		40		30		30	mA
			Mil				40		40		30	
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Com'l		20		20		20		20	mA
			Mil				20		20		20	

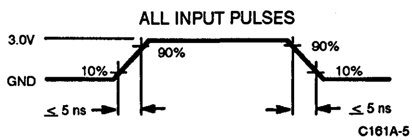
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





2

Switching Characteristics Over the Operating Range[2, 6, 7]

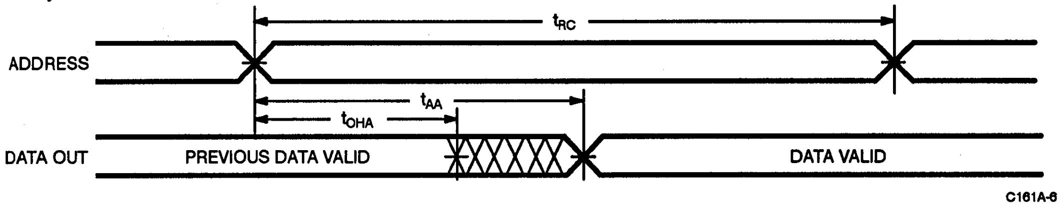
Parameters	Description	7C161A–15 7C162A–15 Min.	Max.	7C161A–20 7C162A–20 Min.	Max.	7C161A–25 7C162A–25 Min.	Max.	7C161A–35 7C162A–35 Min.	Max.	7C161A–45 7C162A–45 Min.	Max.	Units
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to HIGH Z		8		8		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[10]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8] (7C162A)	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9] (7C162A)		7		7		7		10		15	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C161A)		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C161A)		15		20		20		30		35	ns

Notes:

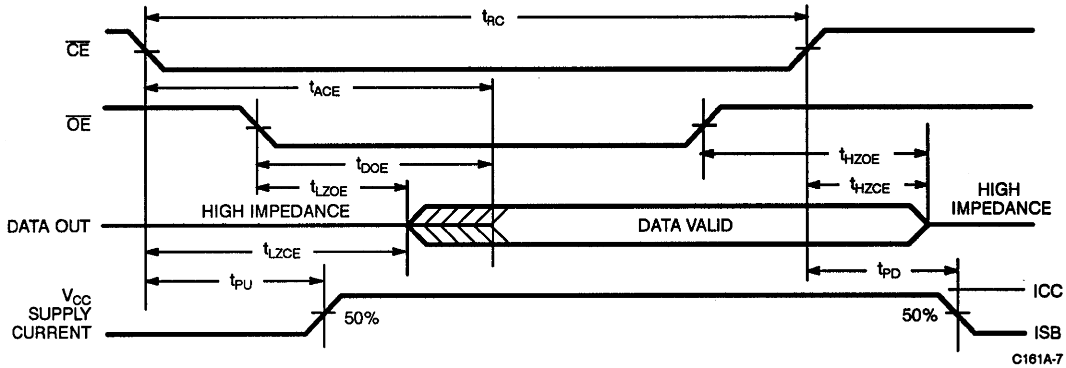
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. Both $\overline{CE}_1$ and $\overline{CE}_2$ are represented by $\overline{CE}$ in the Switching Characteristics and Waveforms sections.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
9. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}_1$, $\overline{CE}_2 = V_{IL}$.
13. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{CE}_2$ transition LOW.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C162A only).

Switching Waveforms[7]

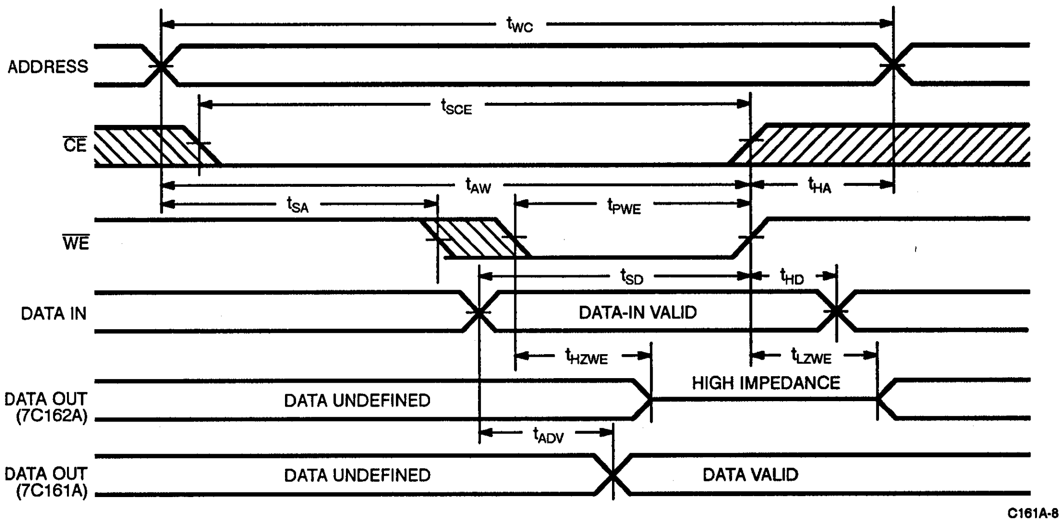
Read Cycle No. 1[11, 12]



Read Cycle No. 2[11, 13]

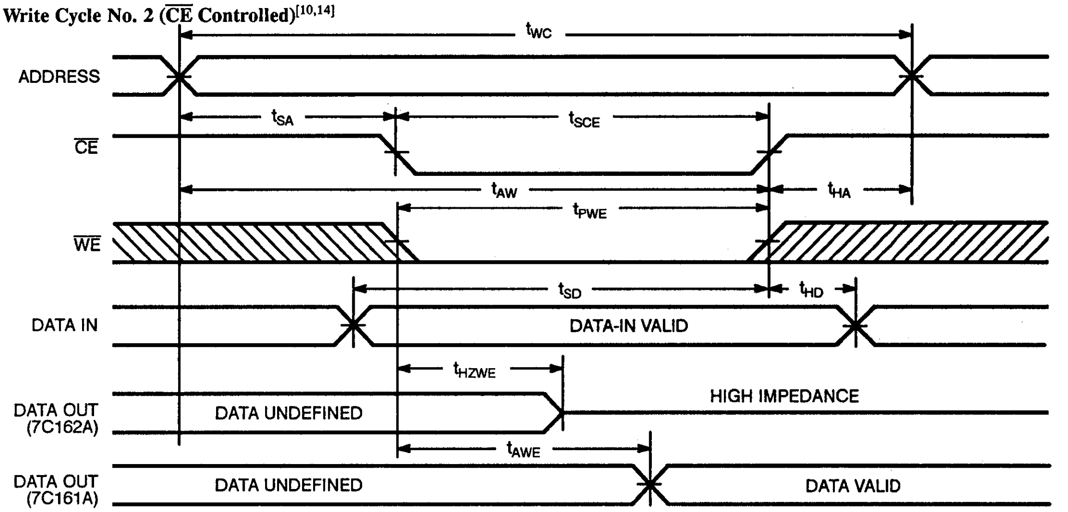


Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



Switching Waveforms (continued)

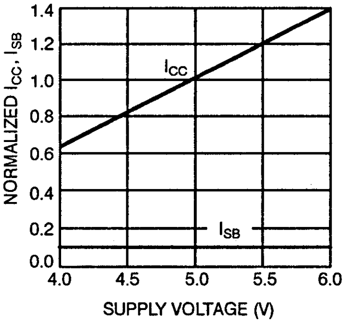
Write Cycle No. 2 ($\overline{CE}$ Controlled)[10,14]



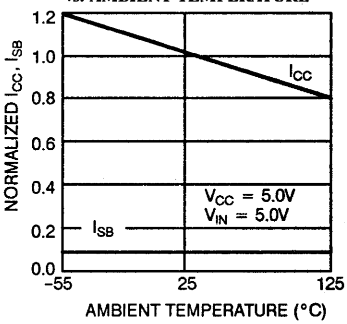
C161A-9

Typical DC and AC Characteristics

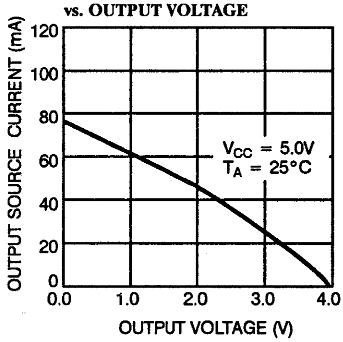
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



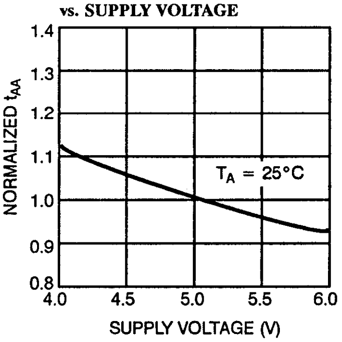
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



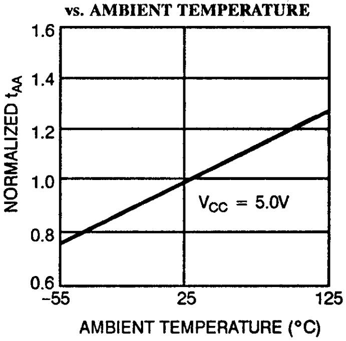
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



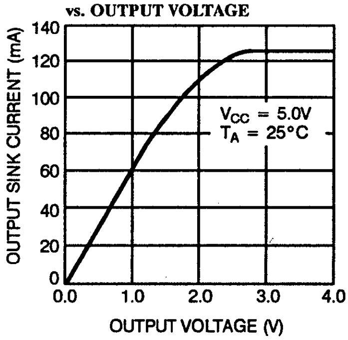
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

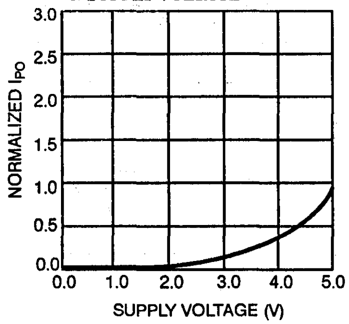


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

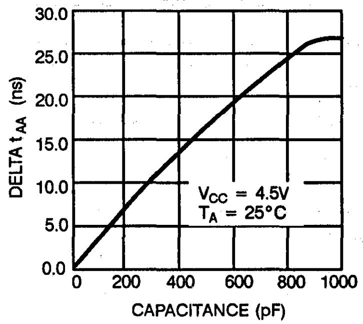


Typical DC and AC Characteristics (continued)

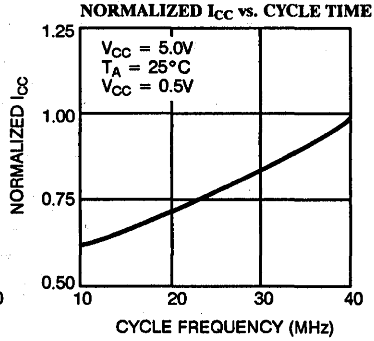
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



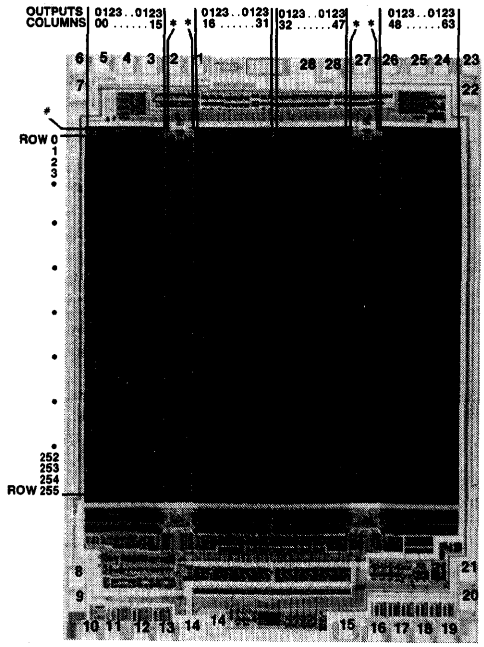
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Bit Map



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y0	6
A11	Y1	7
A12	Y5	8
A13	Y4	9
A0	Y3	23
A1	Y2	24
A2	X0	25
A3	X1	26
A4	X2	27

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C161A–15PC	P21	Commercial
	CY7C161A–15VC	V21	
	CY7C161A–15DC	D22	
	CY7C161A–15LC	L54	
20	CY7C161A–20PC	P21	Commercial
	CY7C161A–20VC	V21	
	CY7C161A–20DC	D22	
	CY7C161A–20LC	L54	
	CY7C161A–20DMB	D22	Military
	CY7C161A–20LMB	L54	
25	CY7C161A–25PC	P21	Commercial
	CY7C161A–25VC	V21	
	CY7C161A–25DC	D22	
	CY7C161A–25LC	L54	
	CY7C161A–25DMB	D22	Military
	CY7C161A–25LMB	L54	
35	CY7C161A–35PC	P21	Commercial
	CY7C161A–35VC	V21	
	CY7C161A–35DC	D22	
	CY7C161A–35LC	L54	
	CY7C161A–35DMB	D22	Military
	CY7C161A–35LMB	L54	
45	CY7C161A–45PC	P21	Commercial
	CY7C161A–45VC	V21	
	CY7C161A–45DC	D22	
	CY7C161A–45LC	L54	
	CY7C161A–45DMB	D22	Military
	CY7C161A–45LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C162A–15PC	P21	Commercial
	CY7C162A–15VC	V21	
	CY7C162A–15DC	D22	
	CY7C162A–15LC	L54	
20	CY7C162A–20PC	P21	Commercial
	CY7C162A–20VC	V21	
	CY7C162A–20DC	D22	
	CY7C162A–20LC	L54	
	CY7C162A–20DMB	D22	Military
	CY7C162A–20LMB	L54	
	CY7C162A–20KMB	K74	
25	CY7C162A–25PC	P21	Commercial
	CY7C162A–25VC	V21	
	CY7C162A–25DC	D22	
	CY7C161A–25LC	L54	
	CY7C162A–25DMB	D22	Military
	CY7C162A–25LMB	L54	
	CY7C162A–25KMB	K74	
35	CY7C162A–35PC	P21	Commercial
	CY7C162A–35VC	V21	
	CY7C162A–35DC	D22	
	CY7C162A–35LC	L54	
	CY7C162A–35DMB	D22	Military
	CY7C162A–35LMB	L54	
	CY7C162A–35KMB	K74	
45	CY7C162A–45PC	P21	Commercial
	CY7C162A–45VC	V21	
	CY7C162A–45DC	D22	
	CY7C162A–45LC	L54	
	CY7C162A–45DMB	D22	Military
	CY7C162A–45LMB	L54	
	CY7C162A–45KMB	K74	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[15]	7, 8, 9, 10, 11
t_{ADV}[15]	7, 8, 9, 10, 11

Notes:
15. 7C161A only.

Document #: 38–00116

16,384 x 4 Static R/W RAM

Features

- **BiCMOS for optimum speed/power**
- **High speed**
  - **10 ns t_{AA}**
- **Low active power**
  - **600 mW**
- **Low standby power**
  - **200 mW**
- **Output Enable ($\overline{OE}$) feature (7B166)**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

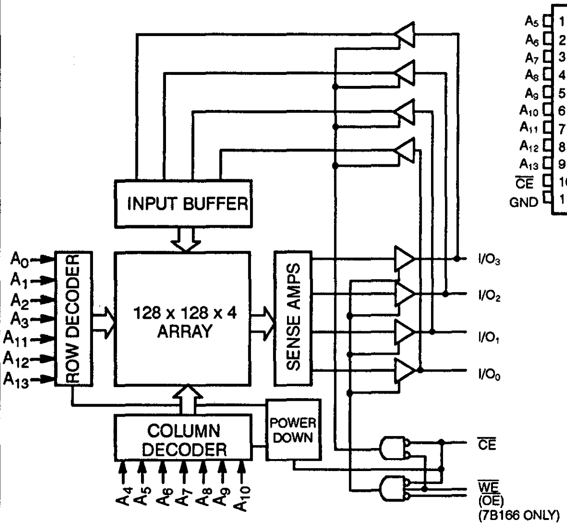
The CY7B164 and CY7B166 are high-performance BiCMOS static RAMs organized as 16,384 x 4 bits. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7B166 has an active LOW output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7B166) while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{WE}$) is LOW (or output enable ($\overline{OE}$) is HIGH for 7B166).

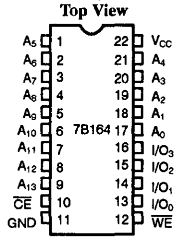
Logic Block Diagram



B164–1

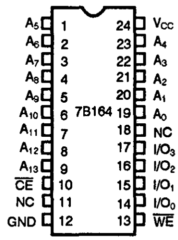
Pin Configurations

DIP
Top View



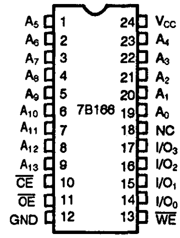
B164-2

SOJ
Top View



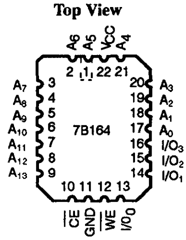
B164-3

DIP/SOJ
Top View



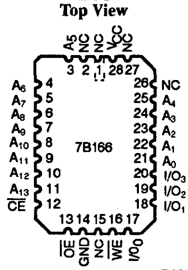
B164-4

LCC
Top View



B164-5

LCC
Top View



B164-6

Selection Guide

		7B164-10 7B166-10	7B164-12 7B166-12	7B164-15 7B166-15
Maximum Access Time (ns)		10	12	15
Maximum Operating Current (mA)	Commercial	130	120	
	Military			135
Maximum Standby Current (mA)	Commercial	40	40	
	Military			50

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

DC Input Voltage[1] .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[2]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions			7B164–10 7B166–10 Min.	7B164–10 7B166–10 Max.	7B164–12 7B166–12 Min.	7B164–12 7B166–12 Max.	7B164–15 7B166–15 Min.	7B164–15 7B166–15 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –4.0 mA	Com'l	2.4		2.4		2.4		V
			I_{OH} = –2.0 mA	Mil							
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			–10	+10	–10	+10	–10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			–10	+10	–10	+10	–10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f max.		Com'l		130		120			mA
				Mil						135	
I_{SB}	$\overline{CE}$ Power-Down Current	$\overline{CE}$ ≥ V_{IH}		Com'l		40		40			mA
				Mil						50	

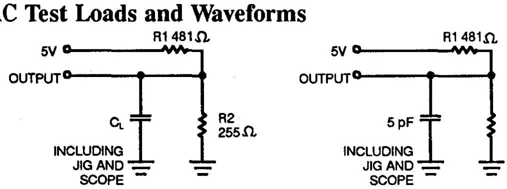
Capacitance[4]

Parameters	Description	Test Conditions	Max.[5]	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

1. V_{IL} (min.) = –3.0V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except CERDIP (D10, D14), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.

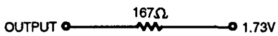
AC Test Loads and Waveforms

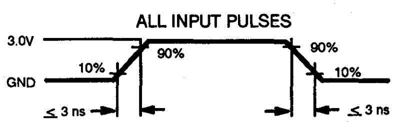


(a) (b)

B164-7

Equivalent to: THÉVENIN EQUIVALENT





B164-8

Switching Characteristics Over the Operating Range[3,6]

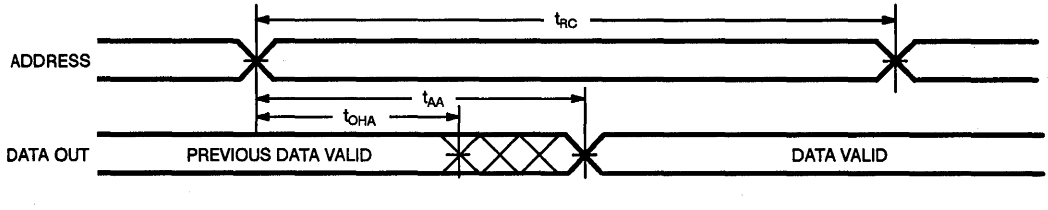
Parameters	Description		7B164–10 7B166–10 Min.	7B164–10 7B166–10 Max.	7B164–12 7B166–12 Min.	7B164–12 7B166–12 Max.	7B164–15 7B166–15 Min.	7B164–15 7B166–15 Max.	Units
READ CYCLE									
t_{RC}	Read Cycle Time		10		12		15		ns
t_{AA}	Address to Data Valid			10		12		15	ns
t_{OHA}	Output Hold from Address Change		2		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7B166		7		7		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	7B166	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]	7B166		7		7		8	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]		2		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]			7		7		8	ns
WRITE CYCLE[9]									
t_{WC}	Write Cycle Time		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		8		8		10		ns
t_{AW}	Address Set-Up to Write End		8		8		10		ns
t_{HA}	Address Hold from Write End		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		8		8		10		ns
t_{SD}	Data Set-Up to Write End		6		6.5		8		ns
t_{HD}	Data Hold from Write End		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		0	7	0	7	0	7	ns

Notes:

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and $C_L = 20$ pF.
7. t_{HZCE}, t_{HZWE}, and t_{HZOE} are specified with $C_L = 5$ pF as in part (b) in AC Test Loads. Transition is measured ± 200 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

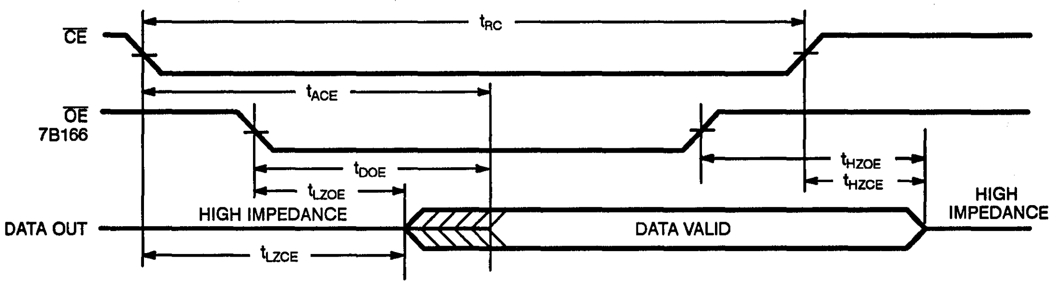
Switching Waveforms

Read Cycle No. 1[10, 11]



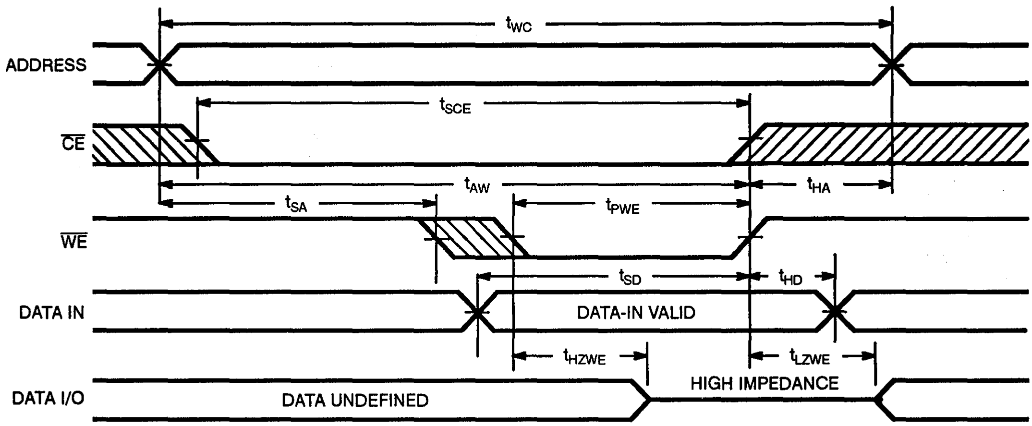
B164–9

Read Cycle No. 2[10, 12]



B164–10

Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13]



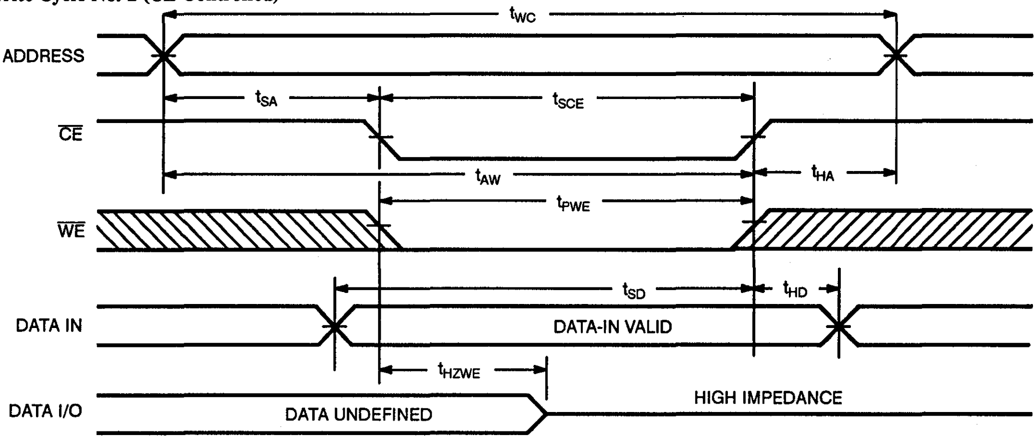
B164–11

Notes:

10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$. (7B166: $\overline{OE} = V_{IL}$ also).
12. Address valid prior to or coincident with $\overline{CE}$ transition low.
13. 7B166 only: Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 (CE Controlled)[9, 13, 14]



7B164 Truth Table

CE	WE	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7B166 Truth Table

CE	WE	OE	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7B164–10VC	V13	Commercial
12	CY7B164–12PC	P9	Commercial
	CY7B164–12VC	V13	
	CY7B164–12DC	D10	
15	CY7B164–15DMB	D10	Military
	CY7B164–15LMB	L52	

Speed (ns)	Ordering Code	Package Type	Operating Range
10	CY7B166–10VC	V13	Commercial
12	CY7B166–12PC	P13	Commercial
	CY7B166–12VC	V13	
	CY7B166–12DC	D14	
15	CY7B166–15DMB	D14	Military
	CY7B166–15LMB	L54	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}[15]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:
15. 7B166 only.

Document #: 38-A-00015-A

CYPRESS SEMICONDUCTOR

CY7C164
CY7C166

16,384 x 4 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **Output Enable ($\overline{OE}$) feature (7C166)**
- **CMOS for optimum speed/power**
- **High speed**
  - **15 ns t_{AA}**
- **Low active power**
  - **633 mW**
- **Low standby power**
  - **220 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

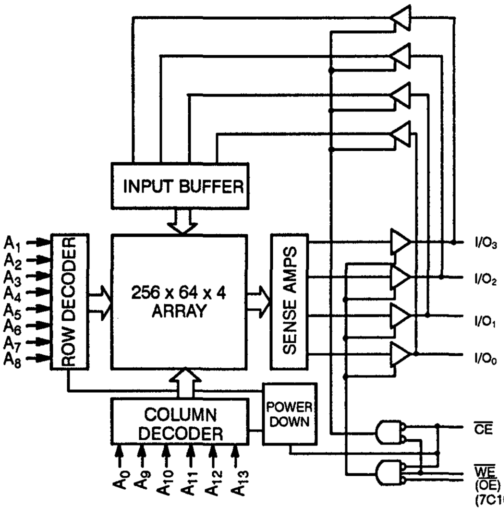
The CY7C164 and CY7C166 are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C166 has an active low output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 65% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW (and the output enable ($\overline{OE}$) is LOW for the 7C166). Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for 7C166), while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{OE}$) is HIGH for 7C166. A die coat is used to insure alpha immunity.

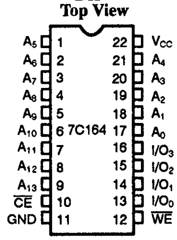
Logic Block Diagram



C164-1

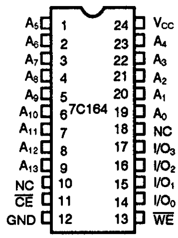
Pin Configurations

DIP
Top View



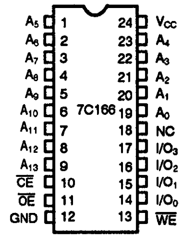
C164-2

SOJ
Top View



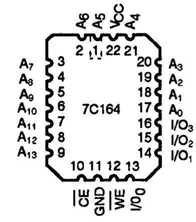
C164-3

DIP/SOJ
Top View



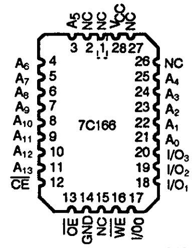
C164-4

LCC
Top View



C164-5

LCC
Top View



C164-6

Selection Guide

	7C164-15 7C166-15	7C164-20 7C166-20	7C164-25 7C166-25	7C164-35 7C166-35	7C164-45 7C166-45
Maximum Access Time (ns)	15	20	25	35	45
Maximum Operating Current (mA)	115	80	70	70	50
Maximum Standby Current (mA)	40/20	40/20	20/20	20/20	20/20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C164-15 7C166-15		7C164-20 7C166-20		7C164-25,35 7C166-25,35		7C164-45 7C166-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		-3.0	0.8	-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	–10	+10	–10	+10	–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND		-350		-350		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		115		80		70		50	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[3]	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%		40		40		20		20	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[3]	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		20		20		20		20	mA

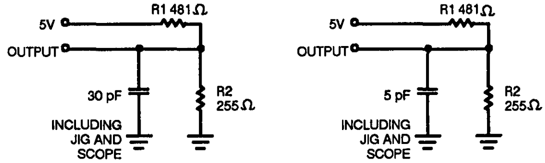
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

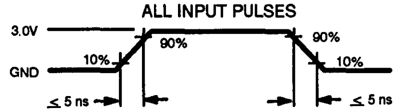
1. V_{IL} min. = –3.0V for pulse durations less than 30 ns.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



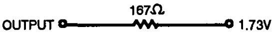
(a) (b)

C164-7



C164-8

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[5]

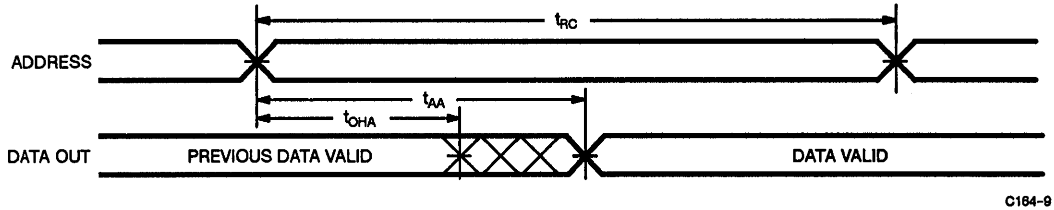
Parameters	Description		7C164-15 7C166-15 Min.	7C164-15 7C166-15 Max.	7C164-20 7C166-20 Min.	7C164-20 7C166-20 Max.	7C164-25 7C166-25 Min.	7C164-25 7C166-25 Max.	7C164-35 7C166-35 Min.	7C164-35 7C166-35 Max.	7C164-45 7C166-45 Min.	7C164-45 7C166-45 Max.	Units
READ CYCLE													
t_{RC}	Read Cycle Time		15		20		25		35		45		ns
t_{AA}	Address to Data Valid			15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change		3		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			15		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	7C166		10		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	7C166	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	7C166		8		8		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]		3		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]			8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down			15		20		20		20		25	ns
WRITE CYCLE[8]													
t_{WC}	Write Cycle Time		15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End		12		15		20		25		30		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End		10		10		10		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]		5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]			7		7		7		10		15	ns

Notes:

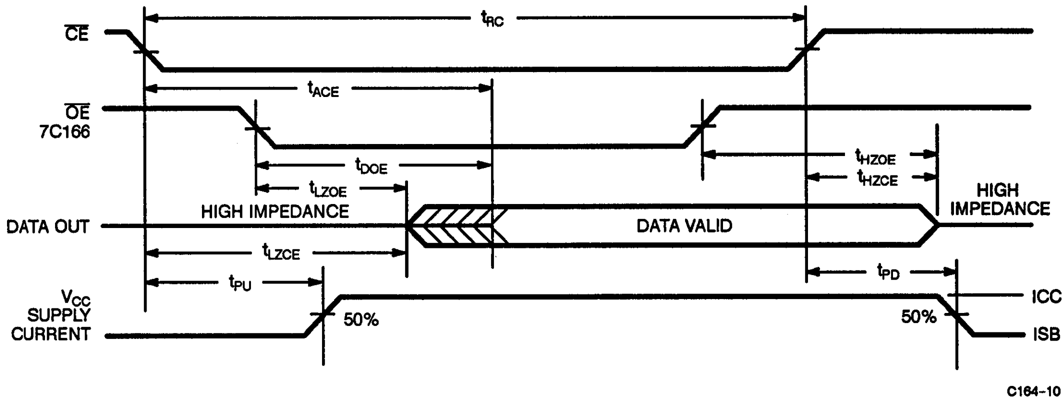
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
7. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

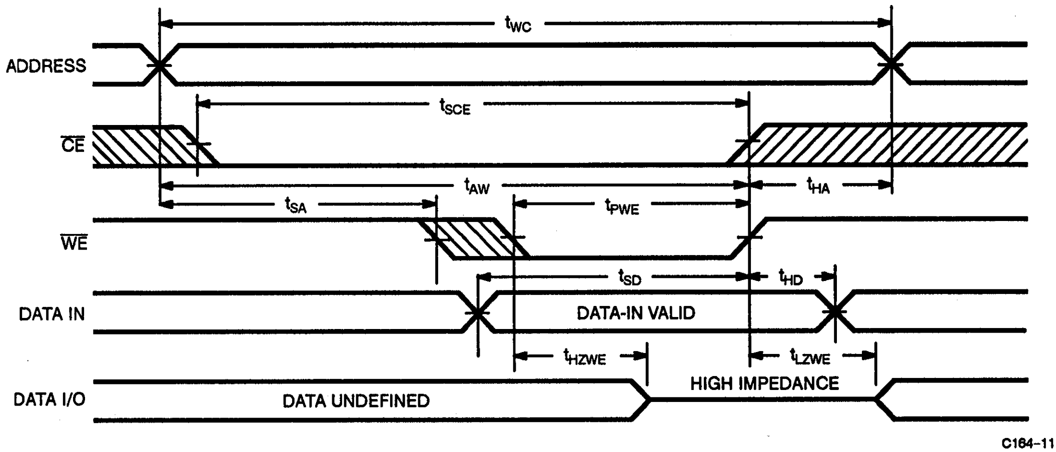
Read Cycle No. 1[9, 10]



Read Cycle No. 2[9, 11]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[8, 12]

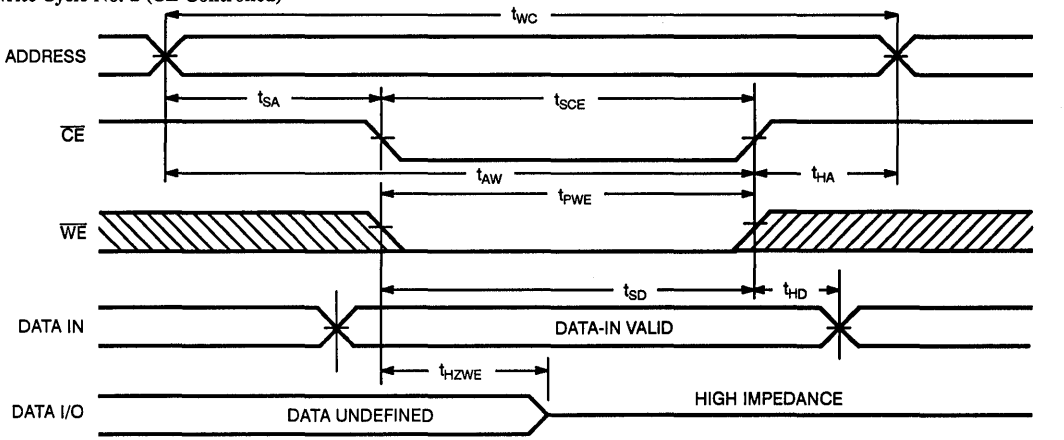


Notes:

9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE} = V_{IL}$. (7C166: $\overline{OE} = V_{IL}$ also).
11. Address valid prior to or coincident with $\overline{CE}$ transition low.
12. 7C166 only: Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

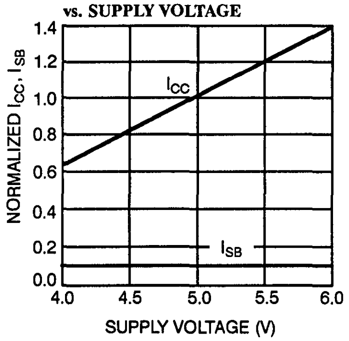
Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 12, 13]



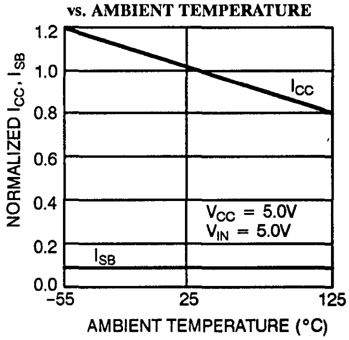
C164-12

Typical DC and AC Characteristics

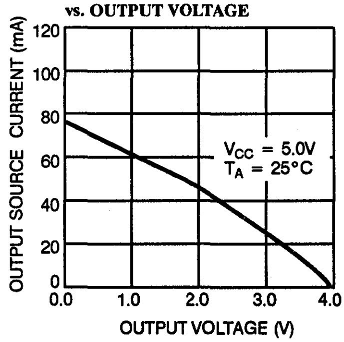
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



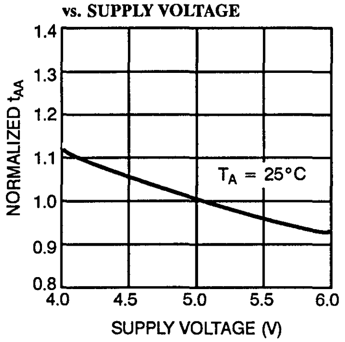
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



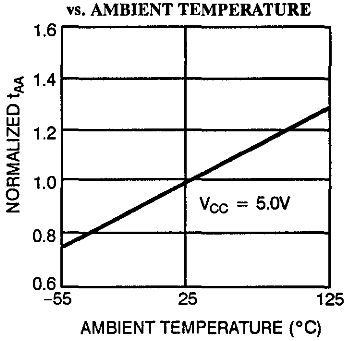
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



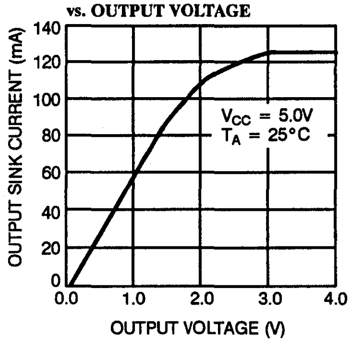
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

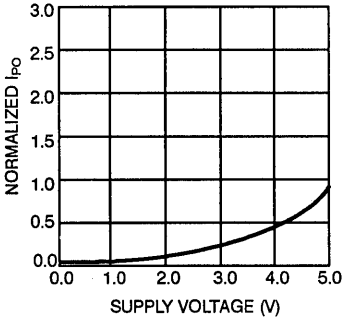


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

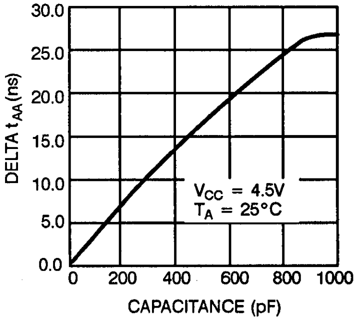


Typical DC and AC Characteristics (continued)

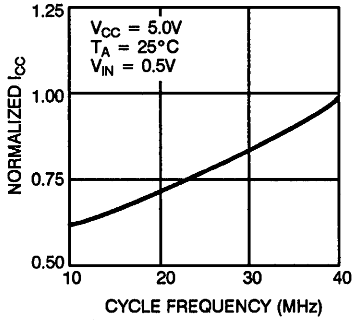
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



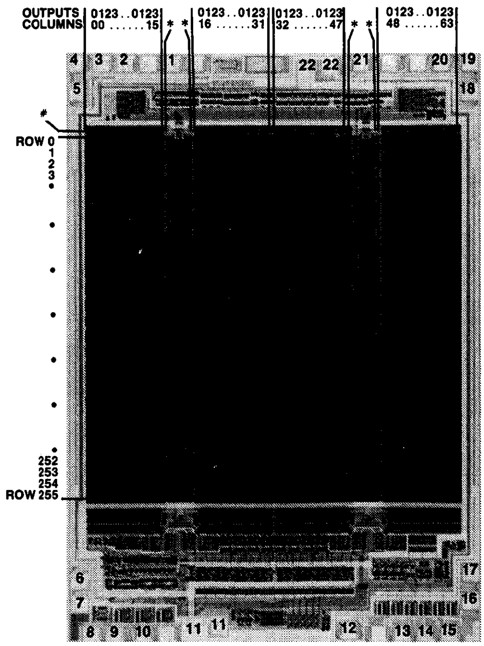
7C164 Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7C164 Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Write

Bit Map



Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y5	6
A11	Y4	7
A12	Y0	8
A13	Y1	9
A0	Y2	17
A1	Y3	18
A2	X0	19
A3	X1	20
A4	X2	21

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C164–15PC	P9	Commercial
	CY7C164–15VC	V13	
	CY7C164–15DC	D10	
	CY7C164–15LC	L52	
20	CY7C164–20PC	P9	Commercial
	CY7C164–20VC	V13	
	CY7C164–20DC	D10	
	CY7C164–20LC	L52	
25	CY7C164–25PC	P9	Commercial
	CY7C164–25VC	V13	
	CY7C164–25DC	D10	
	CY7C164–25LC	L52	
35	CY7C164–35PC	P9	Commercial
	CY7C164–35VC	V13	
	CY7C164–35DC	D10	
	CY7C164–35LC	L52	
45	CY7C164–45PC	P9	Commercial
	CY7C164–45VC	V13	
	CY7C164–45DC	D10	
	CY7C164–45LC	L52	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C166–15PC	P13	Commercial
	CY7C166–15VC	V13	
	CY7C166–15DC	D14	
	CY7C166–15LC	L54	
20	CY7C166–20PC	P13	Commercial
	CY7C166–20VC	V13	
	CY7C166–20DC	D14	
	CY7C166–20LC	L54	
25	CY7C166–25PC	P13	Commercial
	CY7C166–25VC	V13	
	CY7C166–25DC	D14	
	CY7C166–25LC	L54	
35	CY7C166–35PC	P13	Commercial
	CY7C166–35VC	V13	
	CY7C166–35DC	D14	
	CY7C166–35LC	L54	
45	CY7C166–45PC	P13	Commercial
	CY7C166–45VC	V13	
	CY7C166–45DC	D14	
	CY7C166–45LC	L54	

Document #: 38–00032–C

CYPRESS SEMICONDUCTOR

16,384 x 4 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **Output Enable (OE) feature (7C166A)**
- **CMOS for optimum speed/power**
- **High speed**
  - **15 ns t_{AA}**
- **Low active power**
  - **550 mW**
- **Low standby power**
  - **220 mW**
- **TTL-compatible imputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C164A and CY7C166A are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The CY7C166A has an active low output enable (OE) feature. Both devices have an automatic power-down feature, reducing the power consumption by 60% when deselected.

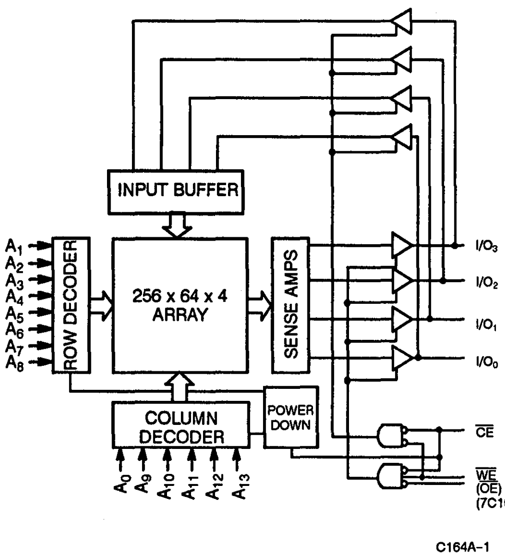
Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW (and the output enable (OE) is LOW for the 7C166A). Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip enable (CE) LOW (and OE LOW for 7C166A), while write enable (WE) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

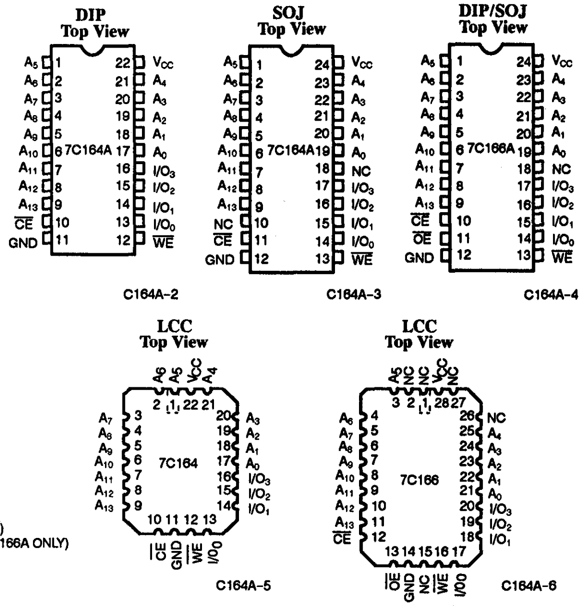
The I/O pins stay in high-impedance state when chip enable (CE) is HIGH, or write enable (OE) is HIGH for 7C166A).

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C164A-15 7C166A-15	7C164A-20 7C166A-20	7C164A-25 7C166A-25	7C164A-35 7C166A-35	7C164A-45 7C166A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	100	100	100	100
	Military		100	100	100	100
Maximum Standby Current (mA)	Commercial	40/20	40/20	30	30	30
	Military		40/20	40/20	30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... − 65°C to + 150°°C

Ambient Temperature with
Power Applied .... − 55°C to + 125°C

Supply Voltage to Ground Potential .... − 0.5V to + 7.0V

DC Voltage Applied to Outputs
in High Z State .... − 0.5V to + 7.0V

DC Input Voltage .... − 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C164A-15 7C166A-15 Min.	7C164A-15 7C166A-15 Max.	7C164A-20 7C166A-20 Min.	7C164A-20 7C166A-20 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		-10	+10	-10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		-10	+10	-10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		115		100	mA
			Mil				100	
I_{SB1}	Automatic $\overline{CE}$[5] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} Min. Duty Cycle = 100%	Com'l		40		40	mA
			Mil				40	
I_{SB2}	Automatic $\overline{CE}$[5] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} − 0.3V V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V	Com'l		20		20	mA
			Mil				20	

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
6. Tested initially and after any design or process changes that may affect these parameters.

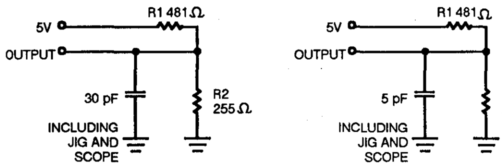
Electrical Characteristics Over the Operating Range[2] (continued)

Parameters	Description	Test Conditions		7C164A-25 7C166A-25 Min.	7C164A-25 7C166A-25 Max.	7C164A-35,45 7C166A-35,45 Min.	7C164A-35,45 7C166A-35,45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		100		100	mA
			Mil		100		100	
I_{SB1}	Automatic $\overline{CE}$[5] Power Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%	Com'l		30		30	mA
			Mil		40		30	
I_{SB2}	Automatic $\overline{CE}$[5] Power Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ - 0.3V $V_{IN} \geq V_{CC}$ - 0.3V or $V_{IN} \leq$ 0.3V	Com'l		20		20	mA
			Mil		20		20	

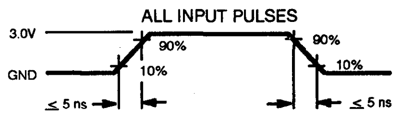
Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms



(a) (b) C164A-7



C164A-8

Equivalent to: THEVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[2,7]

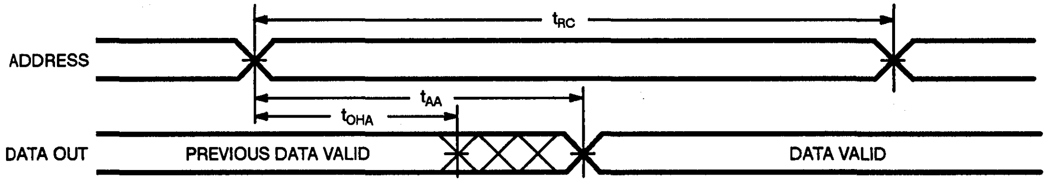
Parameters	Description	7C164A-15 7C166A-15 Min.	Max.	7C164A-20 7C166A-20 Min.	Max.	7C164A-25 7C166A-25 Min.	Max.	7C164A-35 7C166A-35 Min.	Max.	7C164A-45 7C166A-45 Min.	Max.	Units
READ CYCLE												
t_{RC}	Read Cycle Time	20		20		25		35		45		ns
t_{AA}	Address to Data Valid		20		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		20		20		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid 7C166A		10		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z 7C166A	3		3		3		3		3		ns
t_{LZOE}	$\overline{OE}$ HIGH to HIGH Z 7C166A		8		8		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		20		20		25	ns
WRITE CYCLE[10]												
t_{WC}	Write Cycle Time	20		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	15		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	15		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		7		7		7		10		15	ns

Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
9. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}$ = V_{IL}. (7C166: $\overline{OE}$ = V_{IL} also).
13. Address valid prior to or coincident with $\overline{CE}$ transition low.
14. 7C166 only: Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
15. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

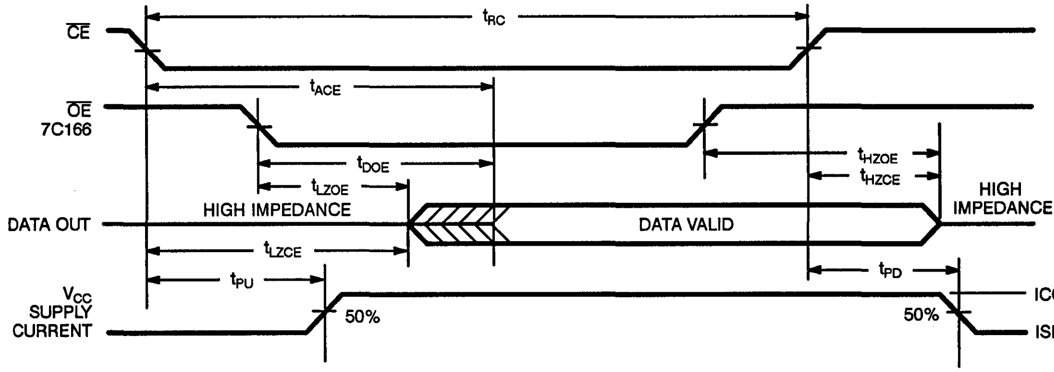
Switching Waveforms

Read Cycle No. 1[11, 12]



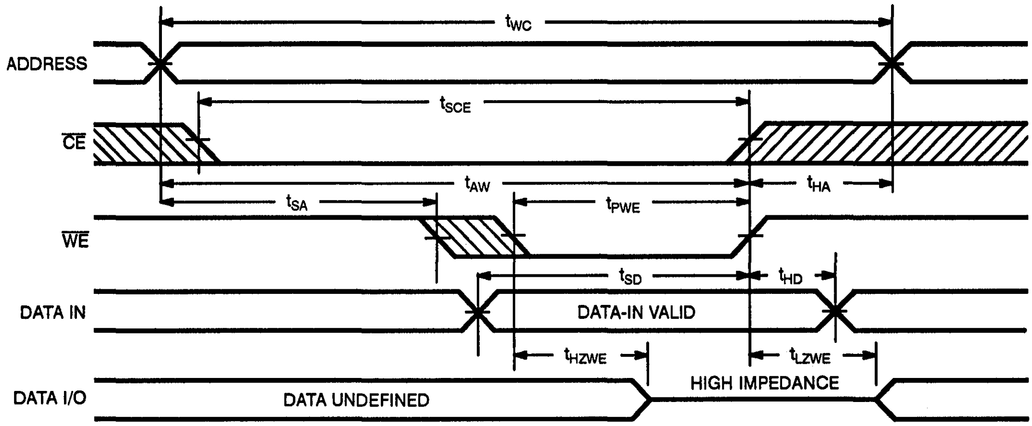
C164A-9

Read Cycle No. 2[11, 13]



C164A-10

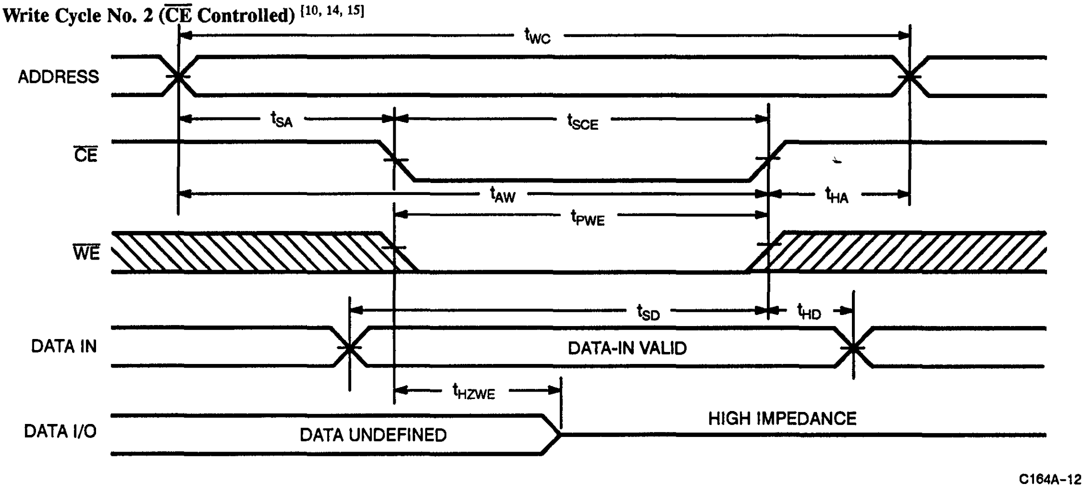
Write Cycle No. 1 (WE Controlled) [10, 14]



C164A-11

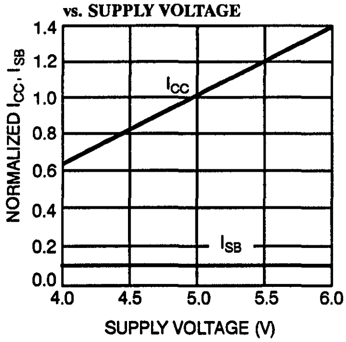
Switching Waveforms (continued)

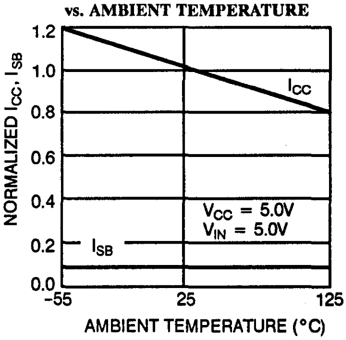
Write Cycle No. 2 ($\overline{CE}$ Controlled) [10, 14, 15]

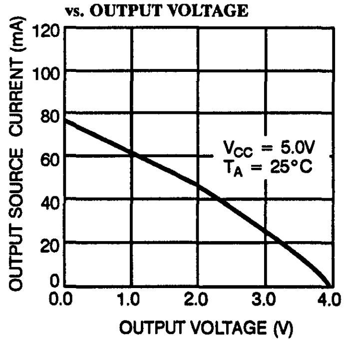


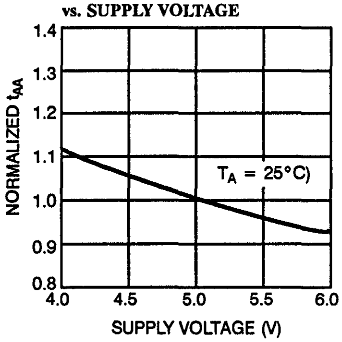
2

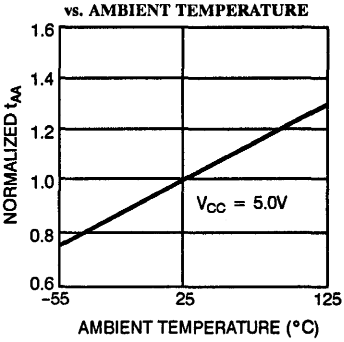
Typical DC and AC Characteristics

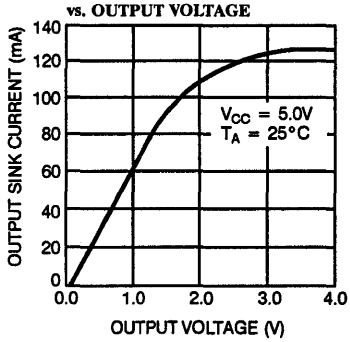




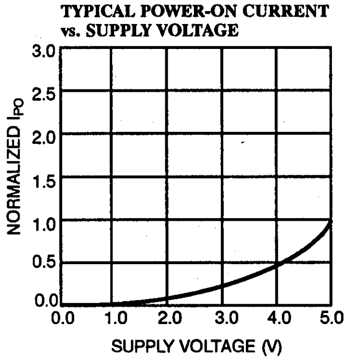


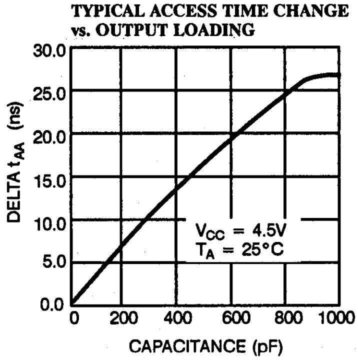


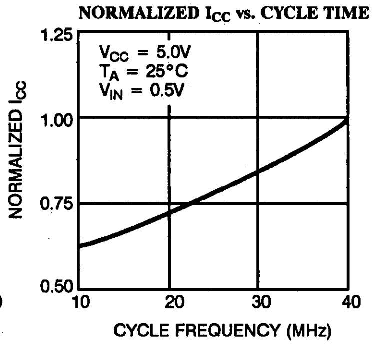




Typical DC and AC Characteristics (continued)







7C164A Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7C166A Truth Table

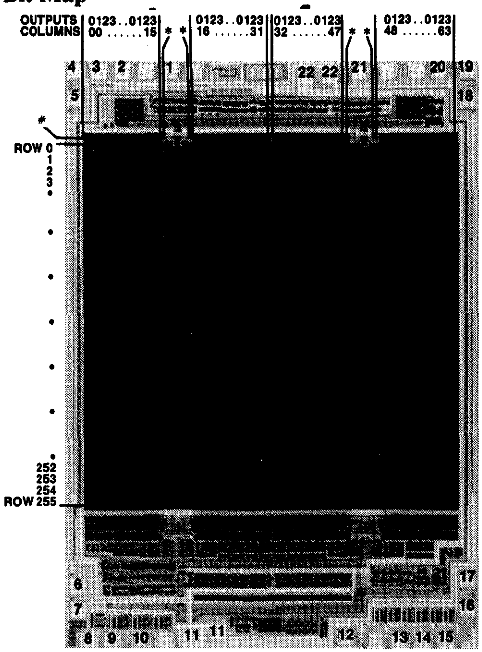
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C164A–15PC	P9	Commercial
	CY7C164A–15VC	V13	
	CY7C164A–15DC	D10	
	CY7C164A–15LC	L52	
20	CY7C164A–20PC	P9	Commercial
	CY7C164A–20VC	V13	
	CY7C164A–20DC	D10	
	CY7C164A–20LC	L52	
	CY7C164A–20DMB	D10	Military
	CY7C164A–20LMB	L52	
	CY7C164A–20KMB	K73	
25	CY7C164A–25PC	P9	Commercial
	CY7C164A–25VC	V13	
	CY7C164A–25DC	D10	
	CY7C164A–25LC	L52	
	CY7C164A–25DMB	D10	Military
	CY7C164A–25LMB	L52	
	CY7C164A–25KMB	K73	
35	CY7C164A–35PC	P9	Commercial
	CY7C164A–35VC	V13	
	CY7C164A–35DC	D10	
	CY7C164A–35LC	L52	
	CY7C164A–35DMB	D10	Military
	CY7C164A–35LMB	L52	
	CY7C164A–35KMB	K73	
45	CY7C164A–45PC	P9	Commercial
	CY7C164A–45VC	V13	
	CY7C164A–45DC	D10	
	CY7C164A–45LC	L52	
	CY7C164A–45DMB	D10	Military
	CY7C164A–45LMB	L52	
	CY7C164A–45KMB	K73	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C166A–15PC	P13	Commercial
	CY7C166A–15VC	V13	
	CY7C166A–15DC	D10	
	CY7C166A–15LC	L52	
20	CY7C166A–20PC	P13	Commercial
	CY7C166A–20VC	V13	
	CY7C166A–20DC	D14	
	CY7C166A–20LC	L54	
	CY7C166A–20DMB	D14	Military
	CY7C166A–20LMB	L54	
	CY7C166A–20KMB	K73	
25	CY7C166A–25PC	P13	Commercial
	CY7C166A–25VC	V13	
	CY7C166A–25DC	D14	
	CY7C166A–25LC	L54	
	CY7C166A–25DMB	D14	Military
	CY7C166A–25LMB	L54	
	CY7C166A–25KMB	K73	
35	CY7C166A–35PC	P13	Commercial
	CY7C166A–35VC	V13	
	CY7C166A–35DC	D14	
	CY7C166A–35LC	L54	
	CY7C166A–35DMB	D14	Military
	CY7C166A–35LMB	L54	
	CY7C166A–35KMB	K73	
45	CY7C166A–45PC	P13	Commercial
	CY7C166A–45VC	V13	
	CY7C166A–45DC	D14	
	CY7C166A–45LC	L54	
	CY7C166A–45DMB	D14	Military
	CY7C166A–45LMB	L54	
	CY7C166A–45KMB	K73	

Bit Map



MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

Document #: 38-00113

Address Designators

Address Name	Address Function	Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y5	6
A11	Y4	7
A12	Y0	8
A13	Y1	9
A0	Y2	17
A1	Y3	18
A2	X0	19
A3	X1	20
A4	X2	21

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}[16]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Note:
16. 7C166A only.

CYPRESS SEMICONDUCTOR

16,384 x 1 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - 25 ns
- Low active power
  - 275 mW
- Low standby power
  - 83 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C167 is a high-performance CMOS static RAM organized as 16,384 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C167 has an automatic power-down feature, reducing the power consumption by 67% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{13}).

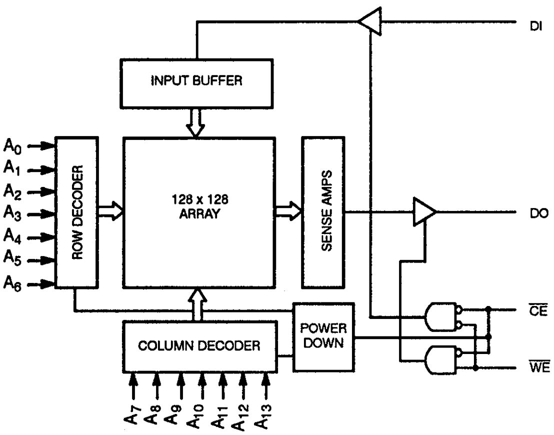
Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The 7C167 utilizes a die coat to insure alpha immunity.

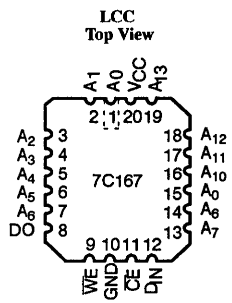
2

Logic Block Diagram

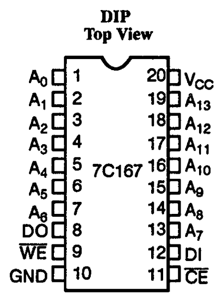


C167-1

Pin Configurations



C167-2



C167-3

Selection Guide

		7C167-25	7C167-35	7C167-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	60	60	50
	Military		60	50

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 26 to Pin 10) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions			7C167-20 Min.	7C167-20 Max.	7C167-35 Min.	7C167-35 Max.	7C167-45 Min.	7C167-45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12.0 mA	Com'l		0.4		0.4		0.4	V
			I_{OL} = 8.0 mA	Mil		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled			−50	+50	−50	+50	−50	+50	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA		Com'l		60		60		50	mA
				Mil						50	
I_{SB}	Automatic $\overline{CE}$[3] Power Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}		Com'l		20		20		15	mA
				Mil						20	

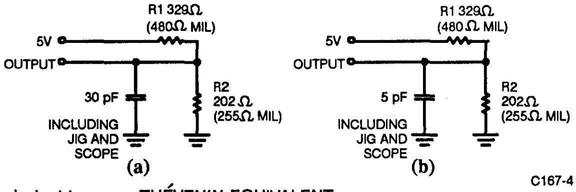
Capacitance[5]

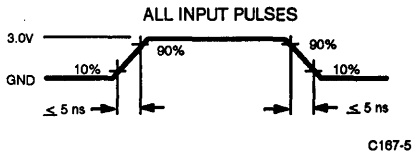
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		6	pF
C_{OUT}	Chip Enable Capacitance		5	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is requited to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
4. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range [2, 6]

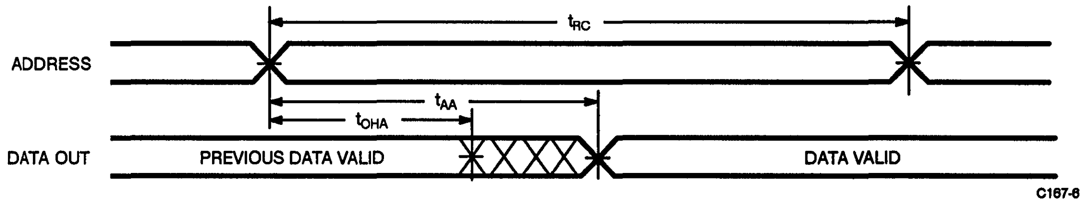
Parameters	Description		7C167-25 Min.	7C167-25 Max.	7C167-35 Min.	7C167-35 Max.	7C167-45 Min.	7C167-45 Max.	Units
READ CYCLE									
t_{RC}	Read Cycle Time	Com'l	25		30		40		ns
		Mil	25		35		40		ns
t_{AA}	Address to Data Valid	Com'l		25		30		40	ns
		Mil				35		40	ns
t_{OHA}	Output Hold from Address Change		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [7]		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [7, 8]			15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down			20		25		30	ns
WRITE CYCLE [9]									
t_{WC}	Write Cycle Time		25		30		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		25		30		40		ns
t_{AW}	Address Set-Up to Write End		25		30		40		ns
t_{HA}	Address Hold from Write End		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		15		20		20		ns
t_{SD}	Data Set-Up to Write End		15		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [7, 8]			15		20		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [7]		0		0		0		ns

Notes:

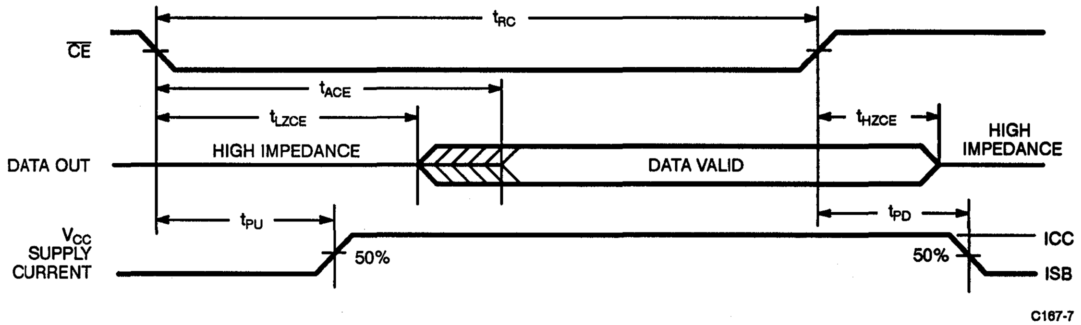
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}$ = V_{IL}.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

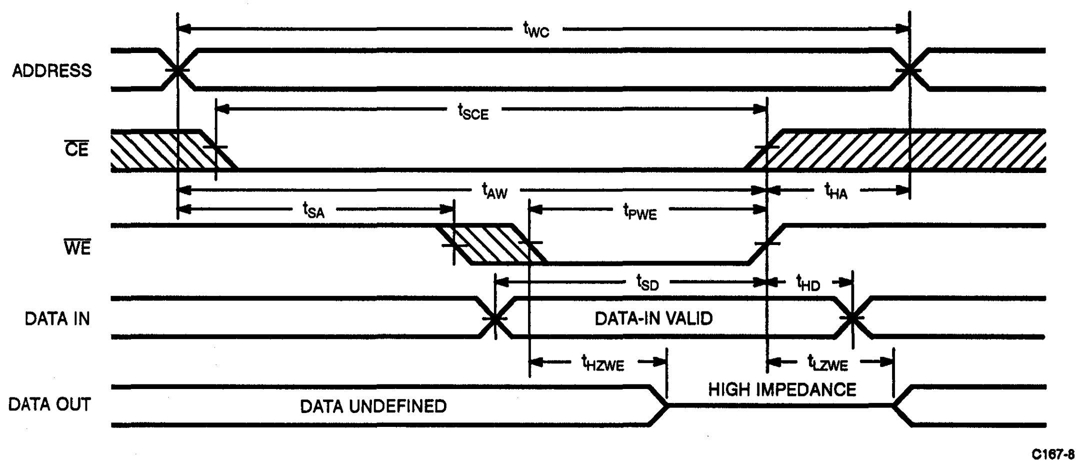
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]

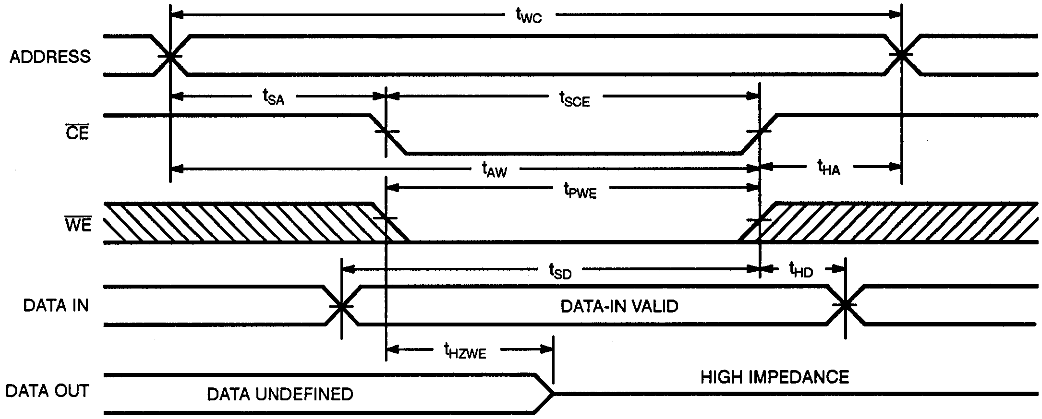


Write Cycle No. 1 (WE Controlled)[9]



Switching Waveforms (continued)

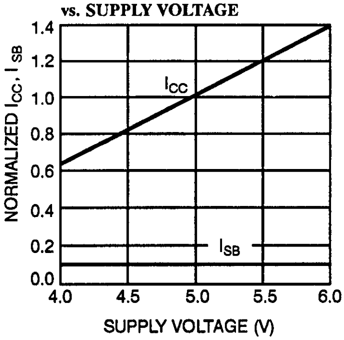
Write Cycle No. 2 (CE Controlled)[9, 13]



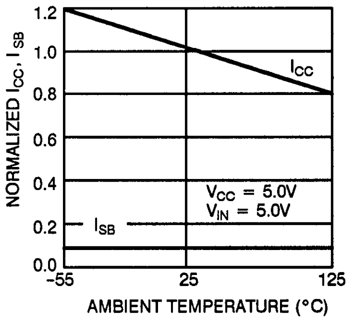
C167-9

Typical DC and AC Characteristics

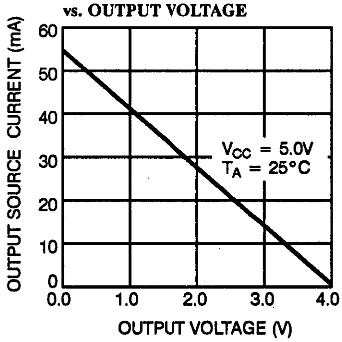
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



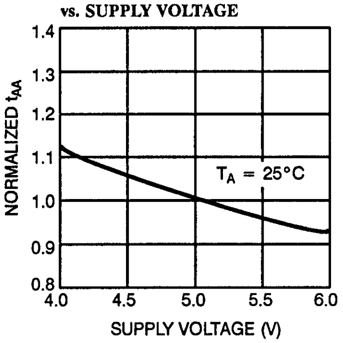
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



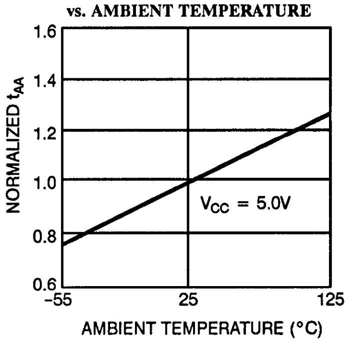
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



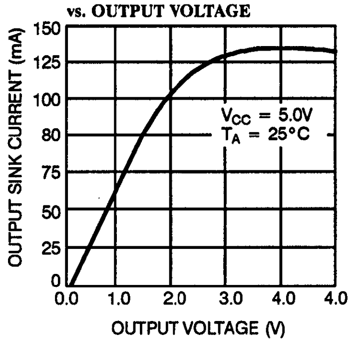
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



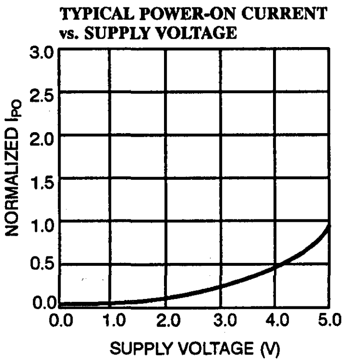
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

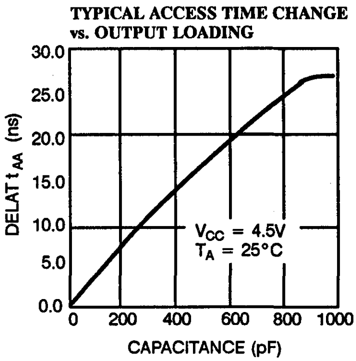


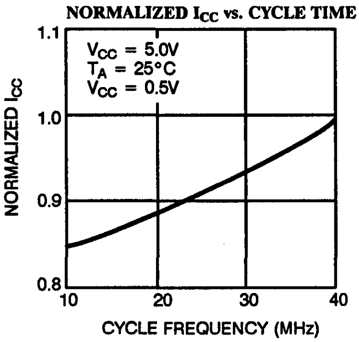
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Typical DC and AC Characteristics (continued)







Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
25	60	CY7C167-25PC	P5	Commercial
		CY7C167-25DC	D16	
		CY7C167-25LC	L51	
		CY7C167-25VC	V5	
35	60	CY7C167-35PC	P5	Commercial
		CY7C167-35DC	D6	
		CY7C167-35LC	L51	
		CY7C167-35VC	V5	
45	50	CY7C167-45PC	P5	Commercial
		CY7C167-45DC	D6	
		CY7C167-45LC	L51	
		CY7C167-45VC	V5	
		CY7C167-45DMB	D6	Military
		CY7C167-45LMB	L51	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00033-D

CY7C167A

16,384 x 1 Static RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **15 ns**
- **Low active power**
  - **275 mW**
- **Low standby power**
  - **83 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **V_{IH} of 2.2V**

Functional Description

The CY7C167A is a high-performance CMOS static RAM organized as 16,384 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C167A has an automatic power-down feature, reducing the power consumption by 67% when deselected.

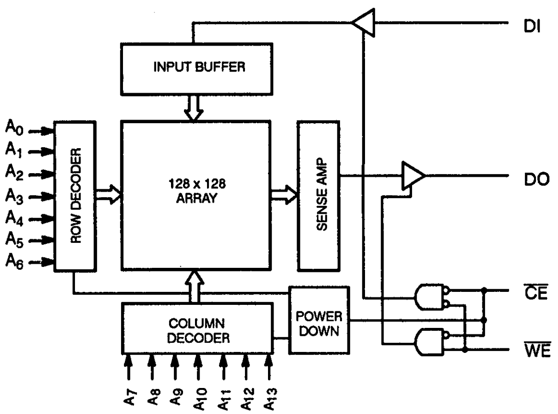
Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while ($\overline{WE}$) remains HIGH. Under these condintions, the contents of the location specified on the address pins will appear on the data output (DO) pin.

The output pin remains in a high-impedance state when chip enable is HIGH, or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

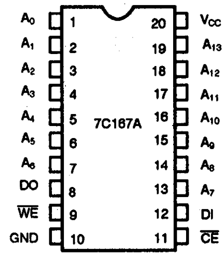
Logic Block Diagram



C167A-1

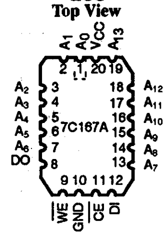
Pin Configurations

DIP
Top View



C167A-2

LCC
Top View



C167A-3

Selection Guide

		7C167A-15	7C167A-20	7C167A-25	7C167A-35	7C167A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	60	60	50
	Military		80	70	60	50

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... − 65°C to + 150°C

Ambient Temperature with Power Applied .... − 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) .... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... − 0.5V to + 7.0V

DC Input Voltage .... − 3.0V to + 7.0V

Output Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C167A-15 Min.	7C167A-15 Max.	7C167A-20 Min.	7C167A-20 Max.	7C167A-25 Min.	7C167A-25 Max.	Units
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2..4		2..4		2..4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 12.0 mA, 8.0 mA Mil			0.4		0.4		0.4	V
V_{IH}	Input High Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage[3]			− 0.5	0.8	− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+ 10	−10	+ 10	−10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	+ 10	−10	+ 10	−10	+ 10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		80		60	mA
			Mil				80		70	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		40		40		20	mA
			Mil				40		20	

Parameters	Description	Test Conditions		7C167A-35 Min.	7C167A-35 Max.	7C167A-45 Min.	7C167A-45 Max.	Units
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2..4		2..4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 12.0 mA, 8.0 mA Mil			0.4		0.4	V
V_{IH}	Input High Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input Low Voltage[3]			− 0.5	0.8	− 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+ 10	−10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	+ 10	−10	+ 10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		60		50	mA
			Mil		60		50	
I_{SB}	Automatic $\overline{CE}$ Power-Down Current[5]	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		20		15	mA
			Mil		20		20	

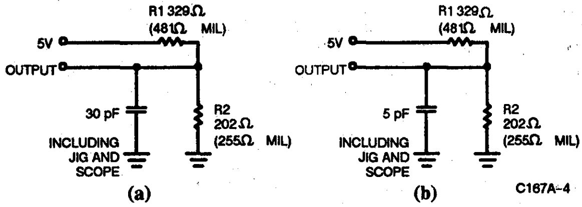
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.

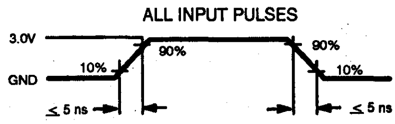
Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 5.0V$	4	pF
C_{OUT}	Output Capacitance		5	pF
C_{CE}	Chip Enable Capacitance		6	pF

AC Test Loads and Waveforms

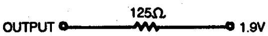


C167A-4



C167A-5

Equivalent to: THÉVENIN EQUIVALENT



Commercial

Military

Switching Characteristics Over the Operating Range[2, 7]

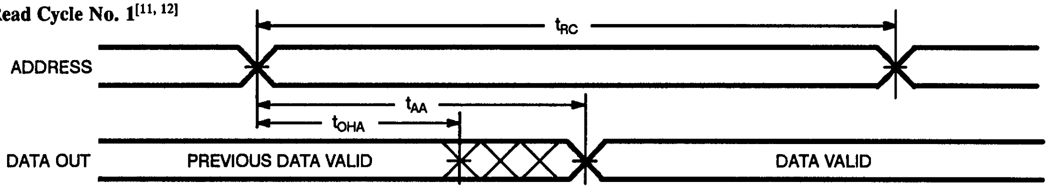
Parameters	Description		7C167A-15		7C167A-20		7C167A-25		7C167A-35		7C167A-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE													
t_{RC}	Read Cycle Time	Com'l	15		20		25		30		40		ns
		Mil			20		25		35		40		ns
t_{AA}	Address to Data Valid	Com'l		15		20		25		30		40	ns
		Mil				20		25		35		40	ns
t_{OHA}	Data Hold from Address Change		5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid			15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]		5		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8, 9]			8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down			15		20		20		20		25	ns
WRITE CYCLE[10]													
t_{WC}	Write Cycle Time		15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End		12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End		12		15		20		25		30		ns
t_{HA}	Address Hold from Write End		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width		12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End		10		10		10		15		15		ns
t_{HD}	Data Hold from Write End		0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]			7		7		7		10		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]		5		5		5		5		5		ns

Notes:

3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during VCC power-up, otherwise I_{SB} will exceed values given.

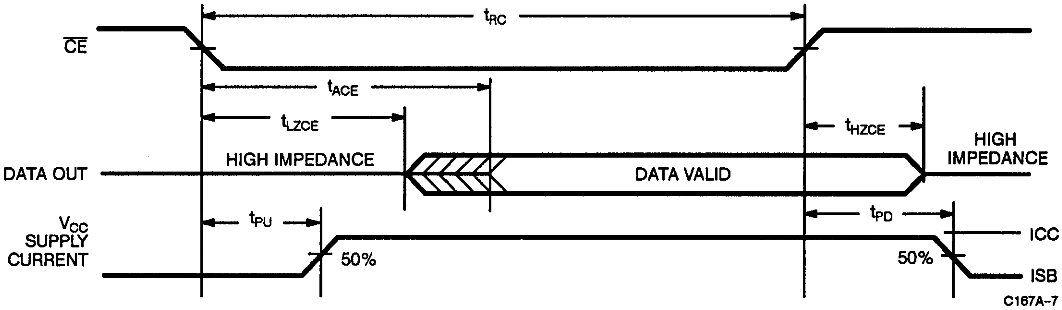
Switching Waveforms

Read Cycle No. 1[11, 12]



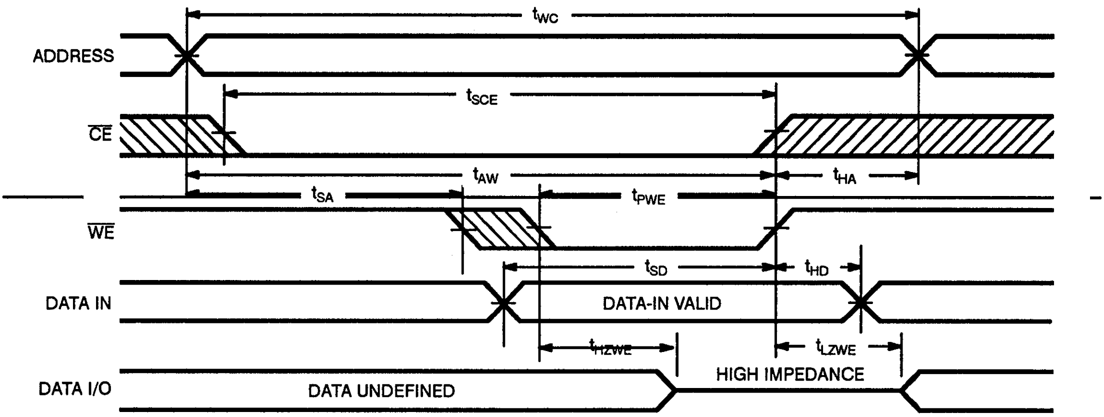
C167A-6

Read Cycle No. 2[11, 13]



C167A-7

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)[10]



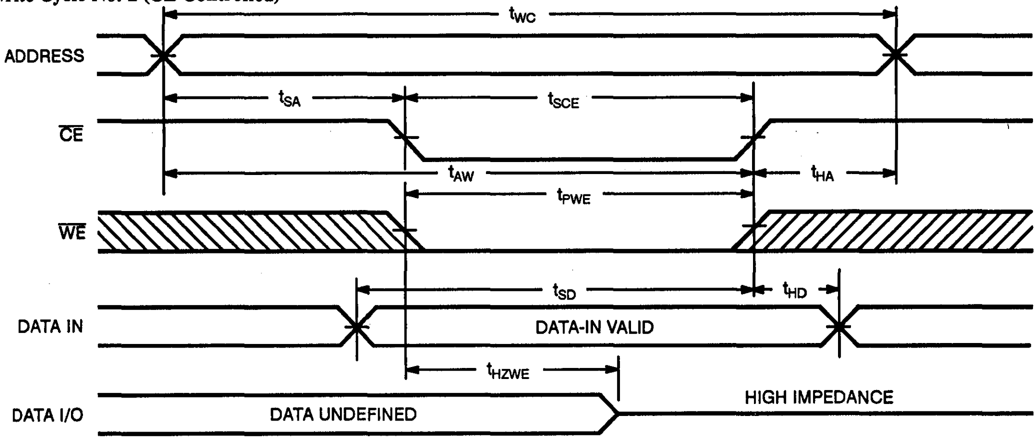
C167A-8

Notes:

6. Tested initially and after any design or process changes that may affect these parameters.
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
9. t_{HZCE} and t_{HZWE} are tested with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{\text{WE}}$ is high for read cycle.
12. Device is continuously selected, $\overline{\text{CE}} = V_{IL}$.
13. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
14. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

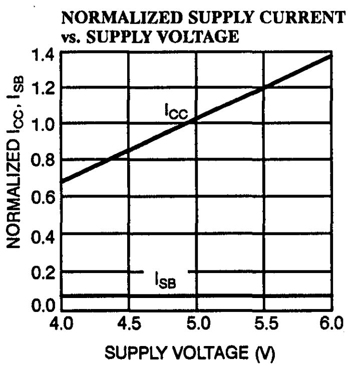
Switching Waveforms (continued)

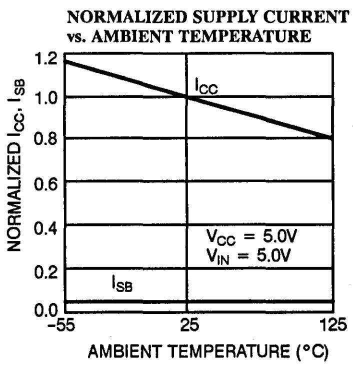
Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 14]

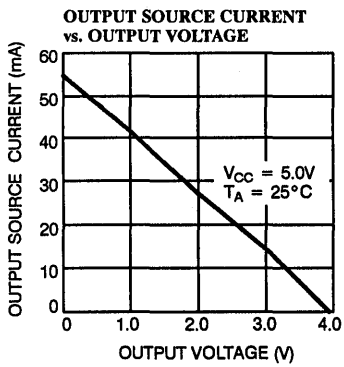


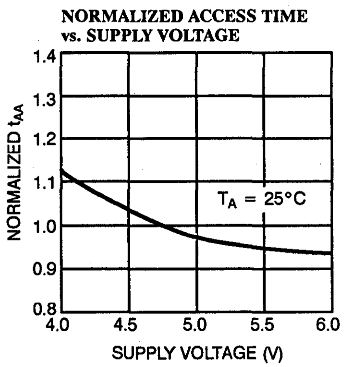
C167A–9

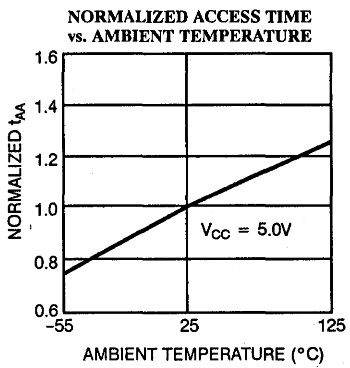
Typical DC and AC Characteristics

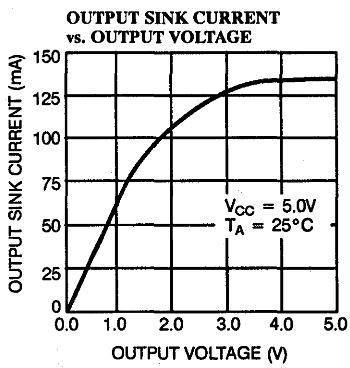






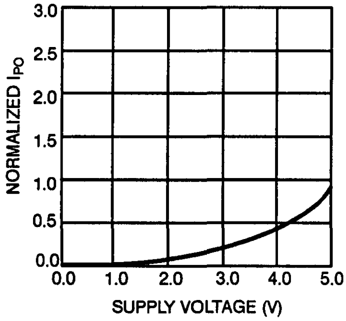




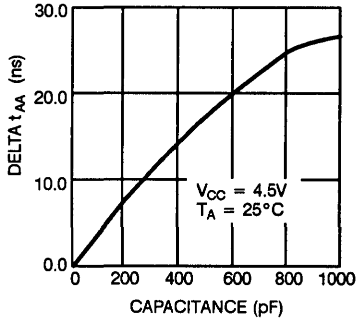


Typical DC and AC Characteristics (continued)

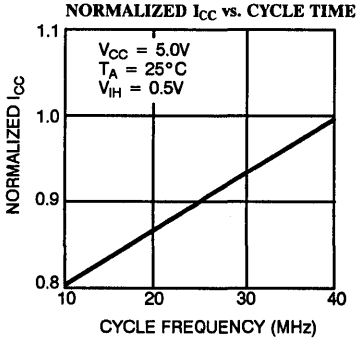
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
15	80	CY7C167A-15PC	P5	Commercial
		CY7C167A-15DC	D6	
		CY7C167A-15VC	V5	
20	80	CY7C167A-20PC	P5	Commercial
		CY7C167A-20DC	D6	
		CY7C167A-20LC	L51	
		CY7C167A-20VC	V5	
		CY7C167A-20DMB	D6	Military
		CY7C167A-20LMB	L51	
		CY7C167A-20KMB	K71	
25	60	CY7C167A-25PC	P5	Commercial
		CY7C167A-25DC	D6	
		CY7C167A-25LC	L51	
		CY7C167A-25VC	V5	
		CY7C167A-25DMB	D6	Military
		CY7C167A-25LMB	L51	
		CY7C167A-25KMB	K71	
35	60	CY7C167A-35PC	P5	Commercial
		CY7C167A-35DC	D6	
		CY7C167A-35LC	L51	
		CY7C167A-35VC	V5	
		CY7C167A-35DMB	D6	Military
		CY7C167A-35LMB	L51	
		CY7C167A-35KMB	K71	
45	50	CY7C167A-45PC	P5	Commercial
		CY7C167A-45DC	D6	
		CY7C167A-45LC	L51	
		CY7C167A-45VC	V5	
		CY7C167A-45DMB	D6	Military
		CY7C167A-45LMB	L51	
		CY7C167A-45KMB	K71	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7,8,9,10,11
t_{AA}	7,8,9,10,11
t_{OHA}	7,8,9,10,11
t_{ACE}	7,8,9,10,11
WRITE CYCLE	
t_{WC}	7,8,9,10,11
t_{SCE}	7,8,9,10,11
t_{AW}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{SA}	7,8,9,10,11
t_{PWE}	7,8,9,10,11
t_{SD}	7,8,9,10,11
t_{HD}	7,8,9,10,11

Document #: 38-00093-B

CY7C168
CY7C169

CYPRESS SEMICONDUCTOR

4096 x 4 Static RAM

2

Features

- **Automatic power-down when deselected (7C168)**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns t_{AA}**
  - **— 15 ns t_{ACE} (7C169)**
- **Low active power**
  - **— 385 mW**
- **Low standby power (7C168)**
  - **— 83 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C168 and CY7C169 are high-performance CMOS static RAMs organized as 4096 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168 has an automatic power-down feature, reducing the power consumption by 77% when deselected .

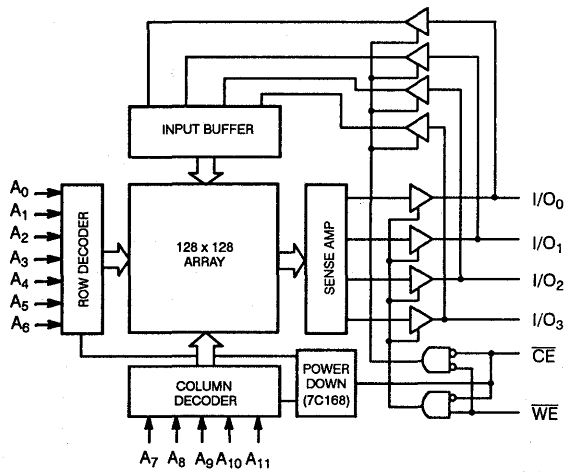
Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while ($\overline{WE}$) remains HIGH. Under these condintions, the contents of the location specified on the address pins will appear on the four data input/output pins (I/O_0 through I/O_3).

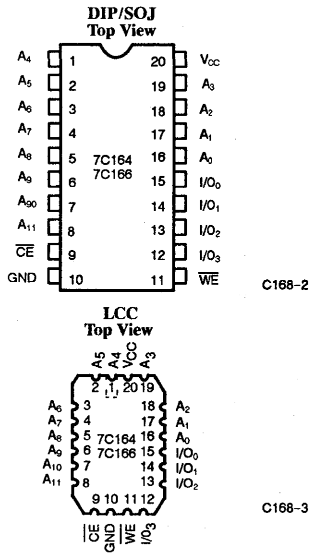
The input/output pins remain in a high-impedance state when chip enable is HIGH, or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C168-25 7C169-25	7C168-35 7C169-35	7C169-40	7C168-45
Maximum Access Time (ns)		25	35	40	45
Maximum Operating Current (mA)	Commercial	90	90	70	70
	Military		90	70	70

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C168-25 7C169-25 Min.	7C168-25 7C169-25 Max.	7C168-35 7C169-35 Min.	7C168-35 7C169-35 Max.	7C168-45 7C169-40 Min.	7C168-45 7C169-40 Max.	Units
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input High Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input Low Voltage			-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-10	10	-10	10	-10	10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$ Output Disabled		-50	50	-50	50	-50	50	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-350		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		70		70	mA
			Mil				90		70	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$	Com'l		20		20		15	mA
			Mil				20		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{CC}$ - .0.3 V	Com'l		11		11		11	mA
			Mil				20		20	

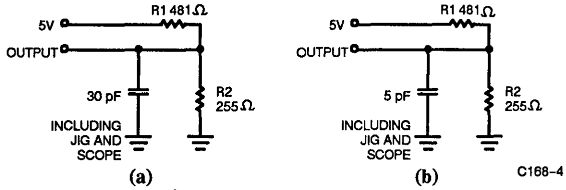
Capacitance[4]

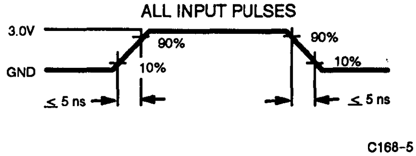
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

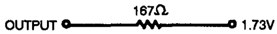
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is high for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition low.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



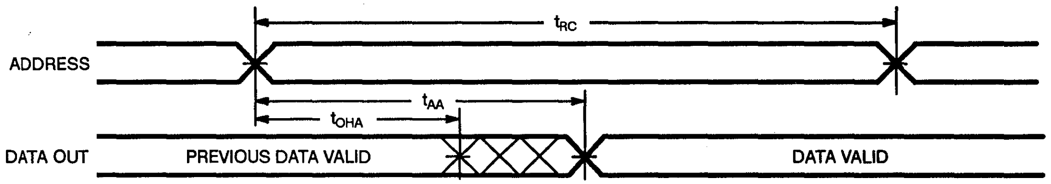
2

Switching Characteristics Over the Operating Range[2,5]

Parameters	Description	7C168-25 7C169-25 Min.	Max.	7C168-35 7C169-35 Min.	Max.	7C169-40 Min.	Max.	7C168-45 Min.	Max.	Units
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		40		45		ns
t_{AA}	Address to Data Valid		25		35		40		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid 7C168		25		35				45	ns
	7C169		15		25		25			ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6,7]		15		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up (7C168)	0		0				0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down (7C168)		25		25				30	ns
t_{RCS}	Read Command Set-Up	0		0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		0		ns
WRITE CYCLE[8]										
t_{WC}	Write Cycle Time	25		35		40		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	25		30		30		35		ns
t_{AW}	Address Set-Up to Write End	20		30		40		35		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		30		35		35		ns
t_{SD}	Data Set-Up to Write End	10		15		15		15		ns
t_{HD}	Data Hold from Write End	0		0		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	6		6		6		6		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6,7]		10		15		20		20	ns

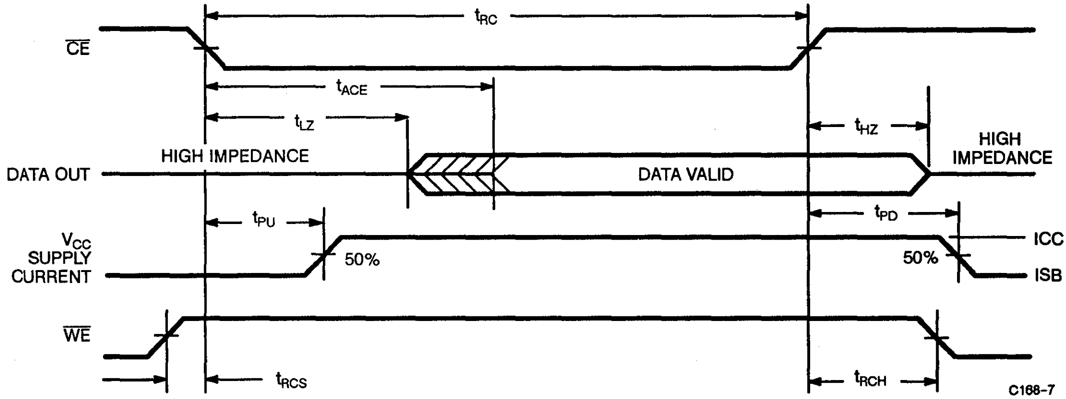
Switching Waveforms

Read Cycle No. 1[9, 10]



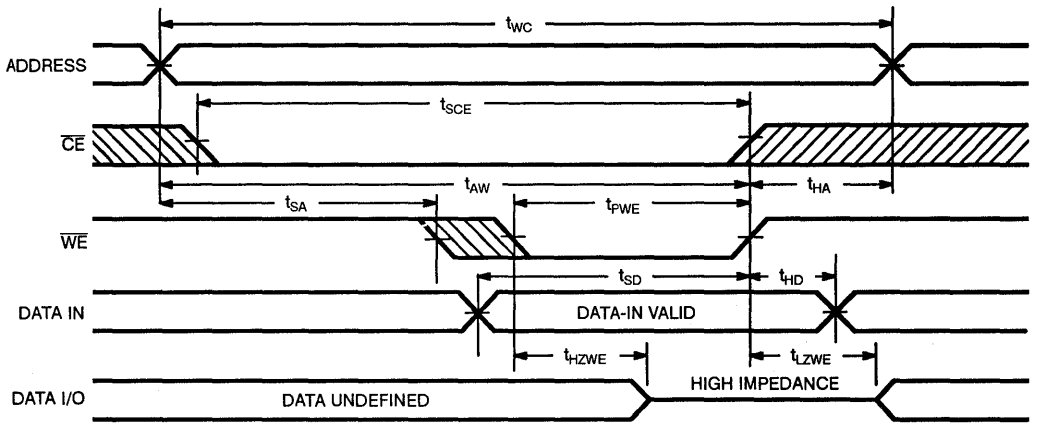
C168-6

Read Cycle[9, 11]



C168-7

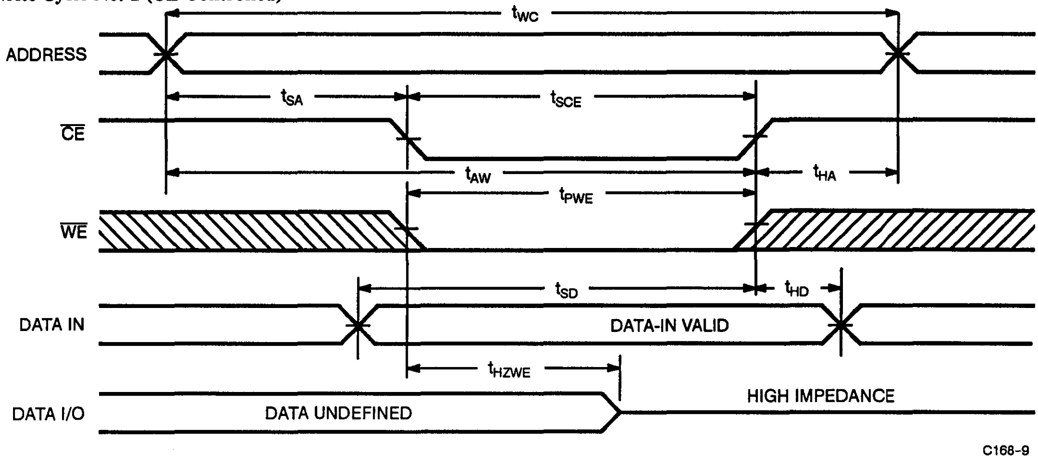
Write Cycle No. 1 (WE Controlled)[8]



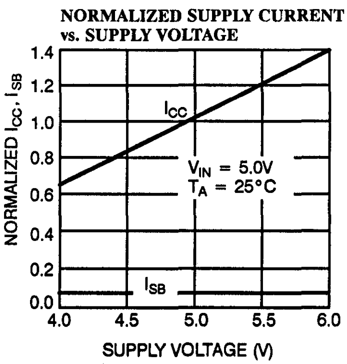
C168-8

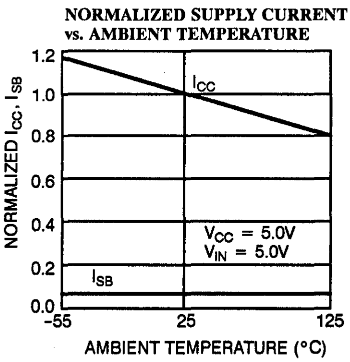
Switching Waveforms (continued)

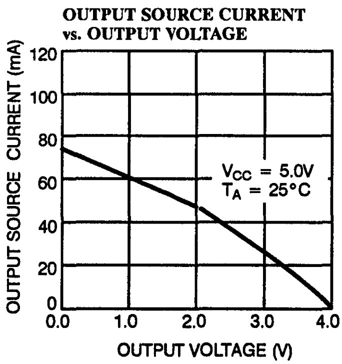
Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 12]

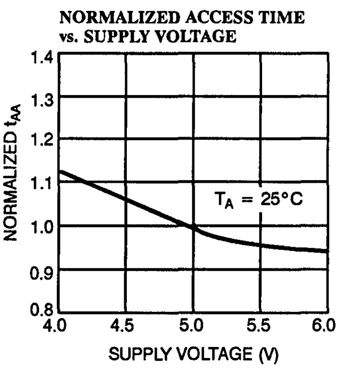


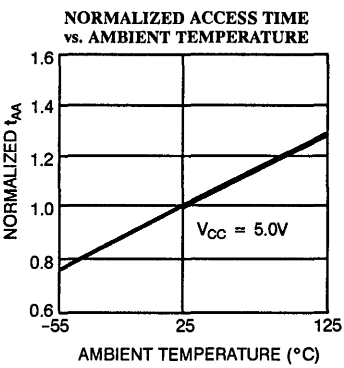
Typical DC and AC Characteristics

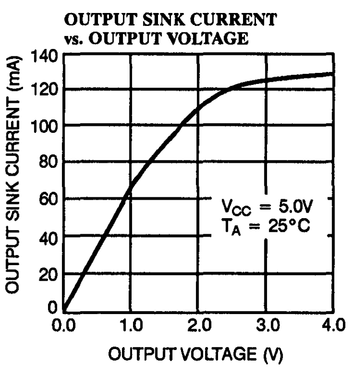




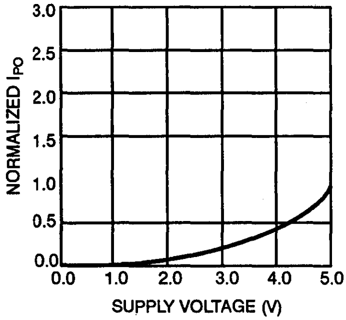


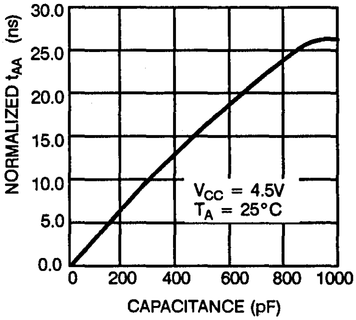


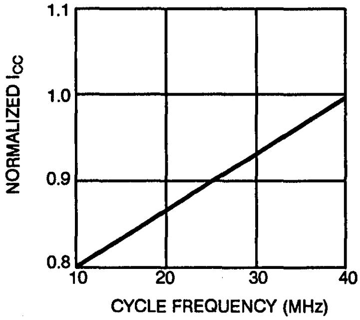




Typical DC and AC Characteristics (continued)







Ordering Information

Speed (ns)	I_{CC} (ns)	Ordering Code	Package Type	Operating Range
25	90	CY7C168-25PC	P5	Commercial
		CY7C168-25DC	D6	
		CY7C168-25LC	L51	
		CY7C168-25VC	V5	
35	90	CY7C168-35PC	P5	Commercial
		CY7C168-35DC	D6	
		CY7C168-35LC	L51	
		CY7C168-35VC	V5	
		CY7C168-35DMB	D6	Military
		CY7C168-35LMB	L51	
45	70	CY7C168-45PC	P5	Commercial
		CY7C168-45DC	D6	
		CY7C168-45LC	L51	
		CY7C168-45VC	V5	
		CY7C168-45DMB	D6	Military
		CY7C168-45LMB	L51	

Speed (ns)	I_{CC} (ns)	Ordering Code	Package Type	Operating Range
25	90	CY7C169-25PC	P5	Commercial
		CY7C169-25DC	D6	
		CY7C169-25LC	L51	
		CY7C169-25VC	V5	
35	90	CY7C169-35PC	P5	Commercial
		CY7C169-35DC	D6	
		CY7C169-35LC	L51	
		CY7C169-35VC	V5	
		CY7C169-35DMB	D6	Military
		CY7C169-35LMB	L51	
40	70	CY7C169-40PC	P5	Commercial
		CY7C169-40DC	D6	
		CY7C169-40LC	L51	
		CY7C169-40VC	V5	
		CY7C169-40DMB	D6	Military
		CY7C169-40LMB	L51	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}[13]	1, 2, 3
I_{SB2}[13]	1, 2, 3

Notes:
13. 7C168 only.

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00034-D

CYPRESS SEMICONDUCTOR

4096 x 4 R/W RAM

Features

- Automatic power–down when deselected (7C168A)
- CMOS for optimum speed/power
- High speed
  - — 15 ns t_{AA}
  - — 10 ns t_{ACE} (7C169A)
- low active power
  - — 385 mW
- Low standby power (7C168)
  - — 83 mW
- TTL-compatible inputs and outputs
- V_{IH} of 2.2V
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C168A and CY7C169A are high-performance CMOS static RAMs organized as 4096 by 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C168A has an automatic power-down feature, reducing the power consumption by 77% when deselected.

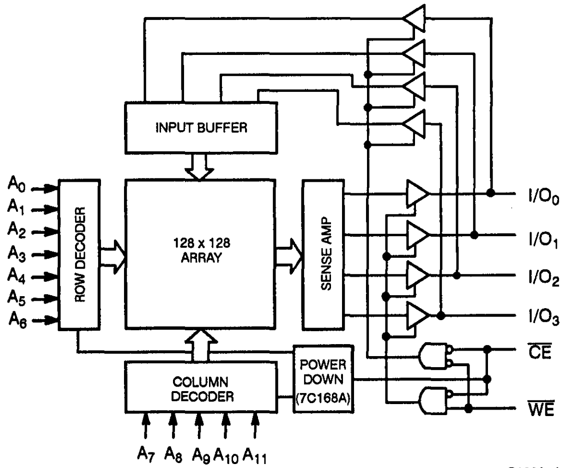
Writing to the device is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the location specified on the address pins will appear on the four data input/output pins (I/O_0 through I/O_3).

The input/output pins remain in a high-impedance state when chip enable is HIGH or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

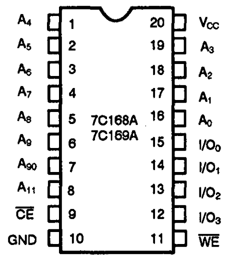
Logic Block Diagram



C168A-1

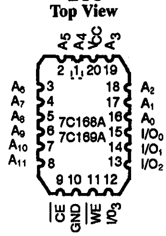
Pin Configurations

DIP
Top View



C168A-2

LCC
Top View



C168A-3

Selection Guide

		7C168A-15 7C169A-15	7C168A-25 7C169A-25	7C168A-25 7C169A-25	7C168A-35 7C169A-35	7C169A-40	7C168A-45
Maximum Access Time (ns)		15	20	25	35	40	45
Maximum Operating Current (mA)	Commercial	115	90	70	70	50	50
	Military		90	80	70	70	70

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 20 to Pin 10) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C168A-15 7C169A-15 Min.	7C168A-15 7C169A-15 Max.	7C168A-20 7C169A-20 Min.	7C168A-20 7C169A-20 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		115		90	mA
			Mil				90	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		40		40	mA
			Mil				40	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ VCC − .0.3 V	Com'l		20		20	mA
			Mil				20	

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

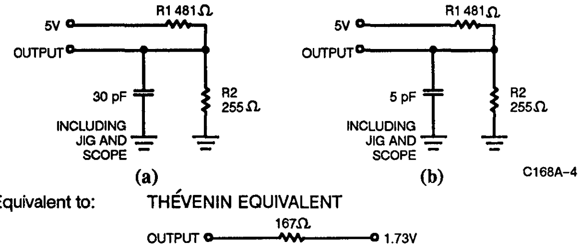
Electrical Characteristics Over the Operating Range[2] (continued)

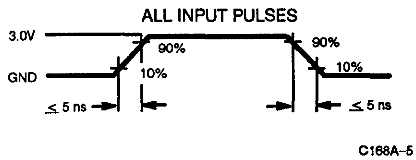
Parameters	Description	Test Conditions		7C168A-25 7C169A-25 Min.	7C168A-25 7C169A-25 Max.	7C168A-35 7C169A-35 Min.	7C168A-35 7C169A-35 Max.	7C168A-45 7C169A-40 Min.	7C168A-45 7C169A-40 Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			-0.5	0.8	-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-10	+10	-10	10	-10	10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$ Output Disabled		-10	+10	-50	50	-50	50	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			-350		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		70		70		50	mA
			Mil		80		70		70	
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$	Com'l		20		20		20	mA
			Mil		20		20		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq$ VCC - .0.3 V	Com'l		20		20		20	mA
			Mil		20		20		20	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms





Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

2

Switching Characteristics Over the Operating Range[3, 6]

Parameters	Description	7C168A-15 7C169A-15 Min.	Max.	7C168A-20 7C169A-20 Min.	Max.	7C168A-25 7C169A-25 Min.	Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	15		20		25		ns
t_{AA}	Address to Data Valid		15		20		25	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
t_{ACE}	Power Supply Current 7C168A		15		20		25	ns
	7C169A		10		12		15	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7, 8]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 9]		8		8		10	ns
t_{PU}	$\overline{CE}$ LOW to Power Up (7C168)	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down (7C168)		15		20		20	ns
t_{RCS}	Read Command Set-Up	0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		ns
WRITE CYCLE[10]								
t_{WC}	Write Cycle Time	15		20		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		ns
t_{AW}	Address Set-Up to Write End	12		15		20		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	7		7		7		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 9]		5		5		5	ns

Notes:

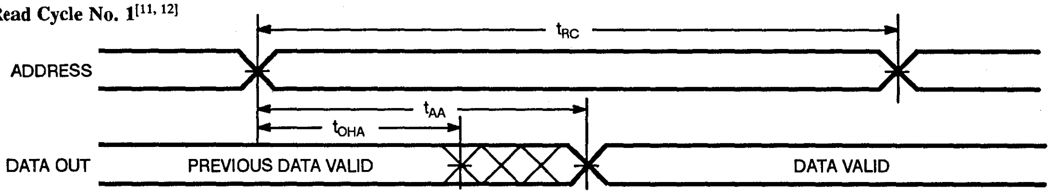
7. At any given temperature and voltage condition, T_{HZ} is less than t_{LZ} for all devices. Transition is measured $\pm$500 mV from steady state voltage with specified loading in part (b) of AC Test Loads and Waveforms.
8. 3-ns minimum for the CY7C169A.
9. t_{HZCE} and t_{HZWE} are tested with C_L = 5 pF as in part (a) of Test Loads and Waveforms. Transition is measured $\pm$500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signal must be LOW to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CE}$ = V_{IL}.
13. Address valid prior to or coincident with $\overline{CE}$ transition low.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Characteristics Over the Operating Range[3, 6] (continued)

Parameters	Description	7C168A-35 7C169A-35 Min.	7C168A-35 7C169A-35 Max.	7C169A-40 Min.	7C169A-40 Max.	7C168A-45 Min.	7C168A-45 Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	35		40		45		ns
t_{AA}	Address to Data Valid		35		40		45	ns
t_{OHA}	Output Hold from Address Change	3		5		5		ns
t_{ACE}	Power Supply Current 7C168A		35		40		45	ns
	Power Supply Current 7C169A		25		25			ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7, 8]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 9]		15		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up (7C168)	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down (7C168)		20		20		25	ns
t_{RCS}	Read Command Set-Up	0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		ns
WRITE CYCLE[10]								
t_{WC}	Write Cycle Time	25		35		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	25		30		30		ns
t_{AW}	Address Set-Up to Write End	25		30		30		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		20		20		ns
t_{SD}	Data Set-Up to Write End	15		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	10		15		15		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 9]		5		5		5	ns

Switching Waveforms

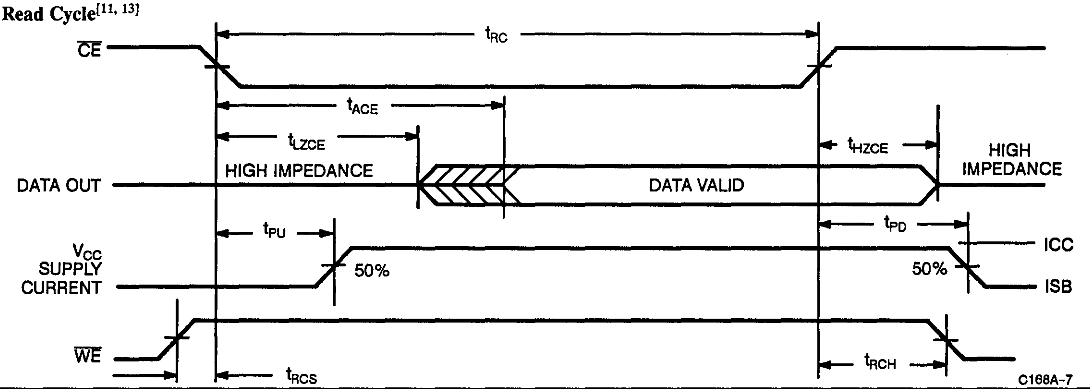
Read Cycle No. 1[11, 12]



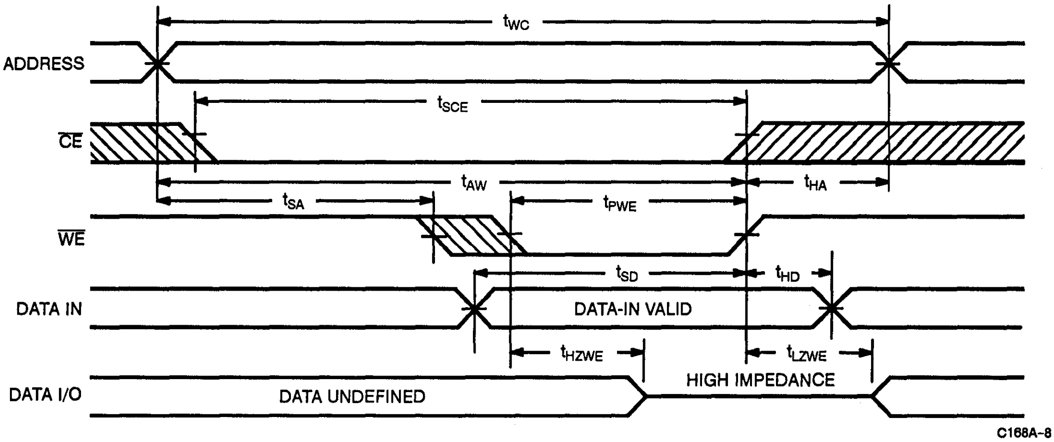
C168A-6

Switching Waveforms (continued)

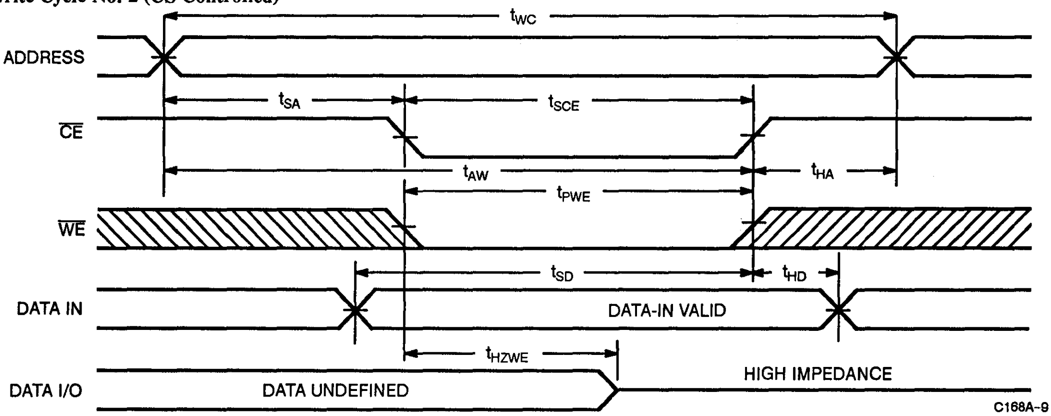
Read Cycle[11, 13]



Write Cycle No. 1 (WE Controlled)[10]

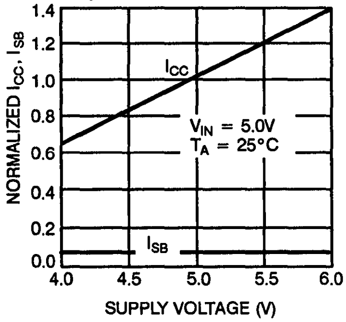


Write Cycle No. 2 (CS Controlled)[10, 14]

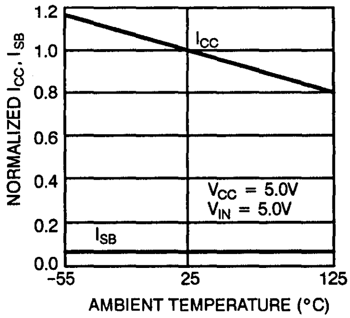


Typical DC and AC Characteristics

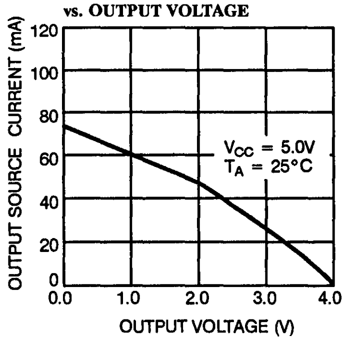
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



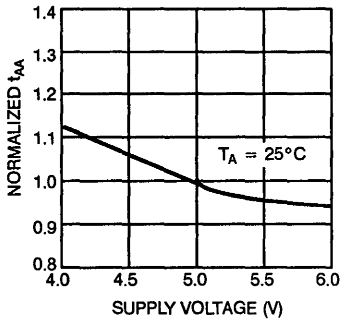
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



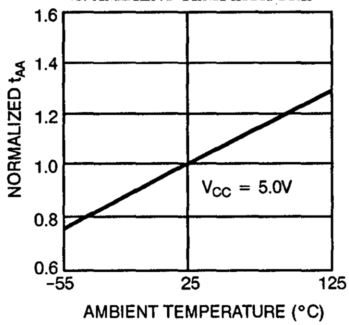
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



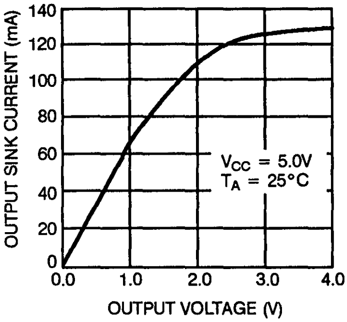
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



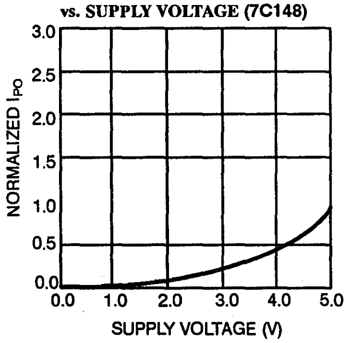
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



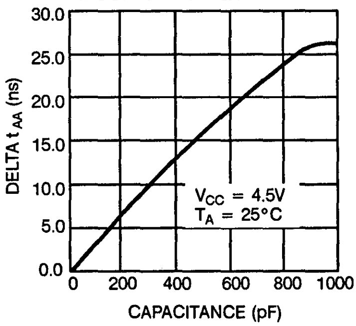
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



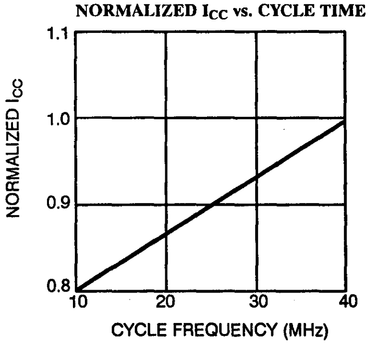
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE (7C148)



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	I_{CC} (ns)	Ordering Code	Package Type	Operating Range
15	115	CY7C168A–15PC	P5	Commercial
		CY7C168A–15DC	D6	
		CY7C168A–15VC	V5	
20	90	CY7C168A–20PC	P5	Commercial
		CY7C168A–20DC	D6	
		CY7C168A–20VC	V5	
		CY7C168A–20DMB	D6	Military
		CY7C168A–20LMB	L51	
		CY7C168A–20FMB	F71	
		CY7C168A–20KMB	K71	
25	70	CY7C168A–25PC	P5	Commercial
		CY7C168A–25DC	D6	
		CY7C168A–25LC	L51	
		CY7C168A–25VC	V5	
	80	CY7C168A–25DMB	D6	Military
		CY7C168A–25LMB	L51	
		CY7C168A–25FMB	F71	
		CY7C168A–25KMB	K71	
35	70	CY7C168A–35PC	P5	Commercial
		CY7C168A–35DC	D6	
		CY7C168A–35LC	L51	
		CY7C168A–35VC	V5	
		CY7C168A–35DMB	D6	Military
		CY7C168A–35LMB	L51	
		CY7C168A–35FMB	F71	
		CY7C168A–35KMB	K71	
45	50	CY7C168A–45PC	P5	Commercial
		CY7C168A–45DC	D6	
		CY7C168A–45LC	L51	
		CY7C168A–45VC	V5	
	70	CY7C168A–45DMB	D6	Military
		CY7C168A–45LMB	L51	
		CY7C168A–45FMB	F71	
		CY7C168A–45KMB	K71	

Speed (ns)	I_{CC} (ns)	Ordering Code	Package Type	Operating Range
15	115	CY7C169A–15PC	P5	Commercial
		CY7C169A–15DC	D6	
		CY7C169A–15VC	V5	
20	90	CY7C169A–20PC	P5	Commercial
		CY7C169A–20DC	D6	
		CY7C169A–20VC	V5	
		CY7C169A–20DMB	D6	Military
		CY7C169A–20LMB	L51	
		CY7C169A–20FMB	F71	
		CY7C169A–20KMB	K71	
25	70	CY7C169A–25PC	P5	Commercial
		CY7C169A–25DC	D6	
		CY7C169A–25LC	L51	
		CY7C169A–25VC	V5	
	80	CY7C169A–25DMB	D6	Military
		CY7C169A–25LMB	L51	
		CY7C169A–25FMB	F71	
		CY7C169A–25KMB	K71	
35	70	CY7C169A–35PC	P5	Commercial
		CY7C169A–35DC	D6	
		CY7C169A–35LC	L51	
		CY7C169A–35VC	V5	
		CY7C169A–35DMB	D6	Military
		CY7C169A–35LMB	L51	
		CY7C169A–35FMB	F71	
		CY7C169A–35KMB	K71	
45	50	CY7C169A–45PC	P5	Commercial
		CY7C169A–45DC	D6	
		CY7C169A–45LC	L51	
		CY7C169A–45VC	V5	
	70	CY7C169A–45DMB	D6	Military
		CY7C169A–45LMB	L51	
		CY7C169A–45FMB	F71	
		CY7C169A–45KMB	K71	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}[15]	1, 2, 3
I_{SB2}[15]	1, 2, 3

Note:
15. 7C168 only.

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00095-D

CYPRESS SEMICONDUCTOR

4096 x 4 Static R/W RAM

Features

- CMOS for optimum speed/power
- High speed
  - 25 ns t_{AA}
  - 15 ns t_{ACS}
- Low active power
  - 495 mW (commercial)
  - 660 mW (military)
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- Output enable

Functional Description

The CY7C170 is a high-performance CMOS static RAM organized as 4096 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$), an active LOW output enable ($\overline{OE}$), and three-state drivers.

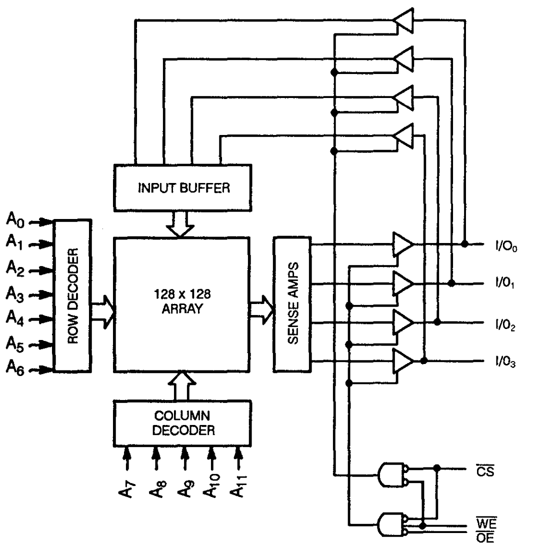
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four I/O pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins stay in high-impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

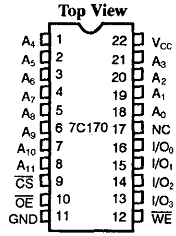
Logic Block Diagram



C170-1

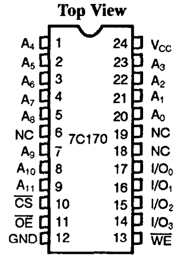
Pin Configurations

DIP
Top View



C170-2

SOJ
Top View



C170-3

Selection Guide

		7C170-25	7C170-35	7C170-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	90	90	90
	Military		120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 11) .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C170 Min.	7C170 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		-50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		90	mA
			Mil		120	mA

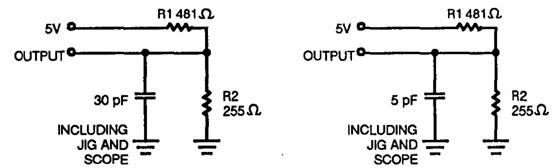
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	pF

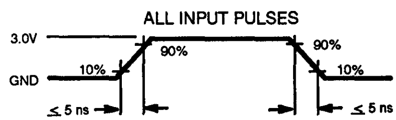
Notes

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

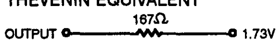


(a) (b) C170-4



C170-5

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2, 5]

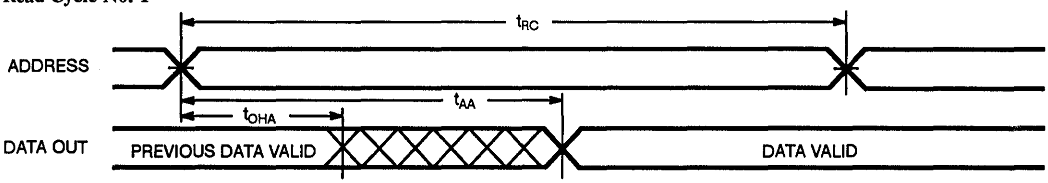
Parameters	Description	7C170A-25		7C170A-35		7C170A-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		15		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		15		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[7]	3		5		5		ns
t_{HZCS}	$\overline{CE}$ HIGH to High Z[6, 7]		15		20		25	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	25		35		40		ns
t_{SCE}	$\overline{CS}$ LOW to Write End	25		35		35		ns
t_{AW}	Address Set-Up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		30		35		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		3		ns
t_{HZWE}	$\overline{WE}$ HIGH to High Z		10		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	6		6		6		ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OI}/I_{OH}, and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCS}, and t_{HZWE} are tested with $C_L = 5pF$ as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referencd to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

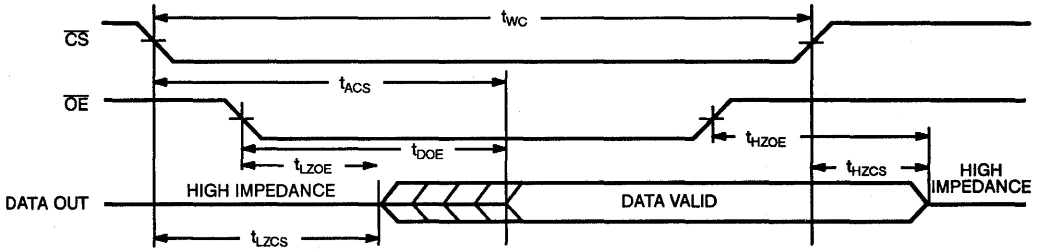
Read Cycle No. 1[9, 10]



C170-6

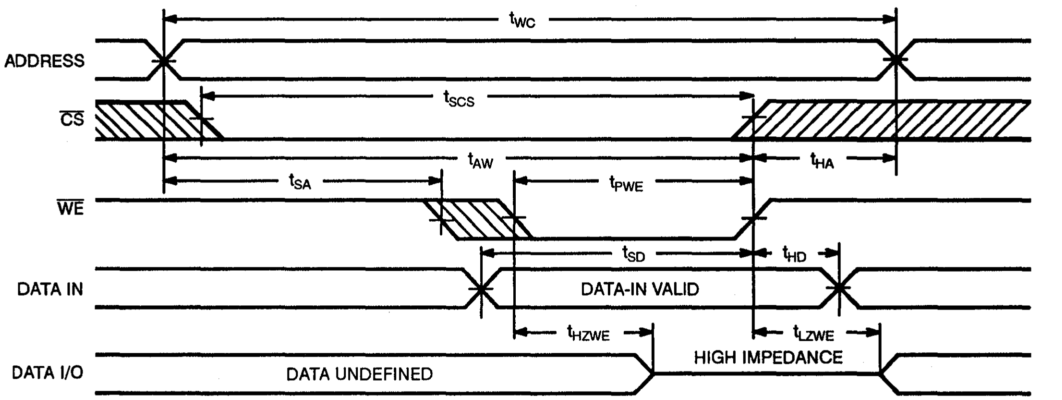
Switching Waveforms (continued)

Read Cycle No. 2[9, 11]



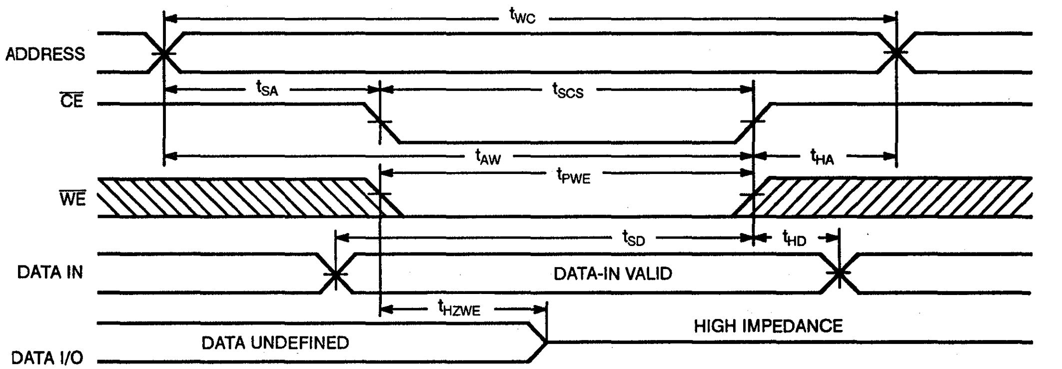
C170-7

Write Cycle No. 1 (WE Controlled)[8, 12]



C170-8

Write Cycle No. 2 (CS Controlled)[8, 12, 13]



C170-9

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C170-25PC	P9	Commercial
	CY7C170-25DC	D10	
	CY7C170-25VC	V13	
35	CY7C170-35PC	P9	Commercial
	CY7C170-35DC	D10	
	CY7C170-35VC	V13	
	CY7C170-35DMB	D10	Military
45	CY7C170-45PC	P9	Commercial
	CY7C170-45DC	D10	
	CY7C170-45VC	V13	
	CY7C170-45DMB	D10	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00035-E

CY7C170A

CYPRESS SEMICONDUCTOR

4096 x 4 Static R/W RAM

Features

- CMOS for optimum speed/power
- High speed
  - 15 ns t_{AA}
  - 10 ns t_{ACS}
- Low active power
  - 495 mW (commercial)
  - 660 mW (military)
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge
- Output enable
- V_{IH} of 2.2V

Functional Description

The CY7C170A is a high-performance CMOS static RAM organized as 4096 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$), an active LOW output enable ($\overline{OE}$) and three-state drivers.

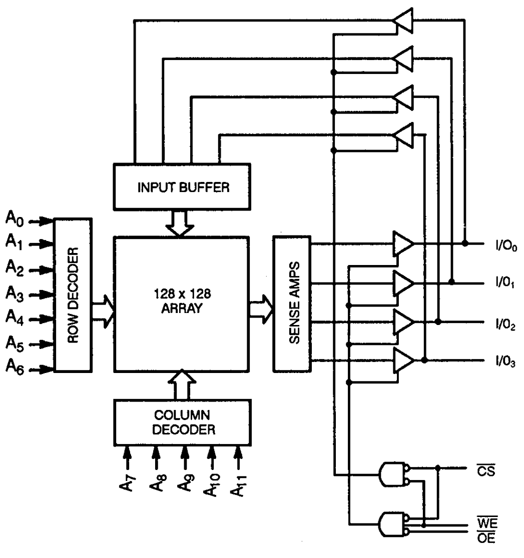
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

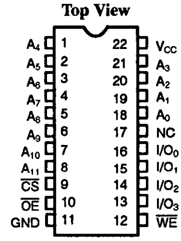
Logic Block Diagram



C170A-1

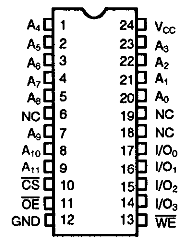
Pin Configurations

DIP
Top View



C170A-2

SOJ
Top View



C170A-3

Selection Guide

		7C170A-15	7C170A-20	7C170A-25	7C170A-35	7C170A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	90	90	90	90
	Military		120	120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°°C

Ambient Temperature with
Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential
(Pin 22 to Pin 21) .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs
in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C170A-15 Min.	7C170A-15 Max.	7C170A-20, 25, 35, 45 Min.	7C170A-20, 25, 35, 45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		-10	+10	-10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		-10	+10	-10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		115		90	mA
			Mil				120	mA

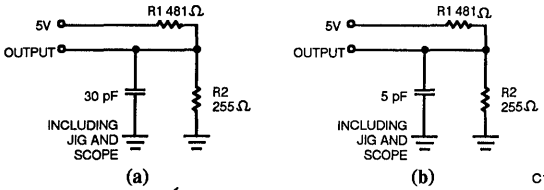
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

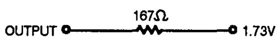
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

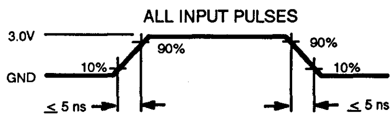
AC Test Loads and Waveforms



C170A-4

Equivalent to: THÉVENIN EQUIVALENT





C170A-5

Switching Characteristics Over the Operating Range[1, 5]

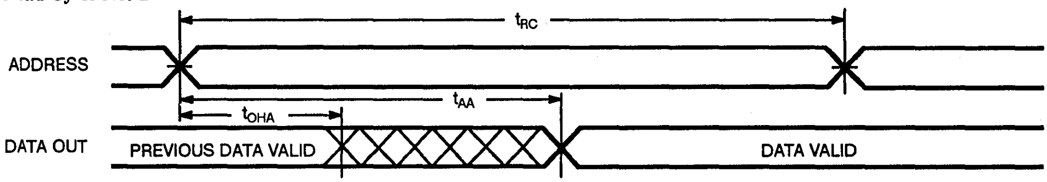
Parameters	Description	7C170A-15		7C170A-20		7C170A-25		7C170A-35		7C170A-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		10		15		15		25		30	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		8		8		10		12		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[7]	5		5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6, 7]		8		8		10		15		15	ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ HIGH to High Z		7		7		7		10		15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OI}/I_{OH}, and 30-pF load capacitance.
6. t_{HZCE} and t_{HZWE} are tested with $C_L = 5pF$ as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are sampled and not 100% tested.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referencd to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
11. Data I/O will be high-impedance if $\overline{OE} = V_{IH}$.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

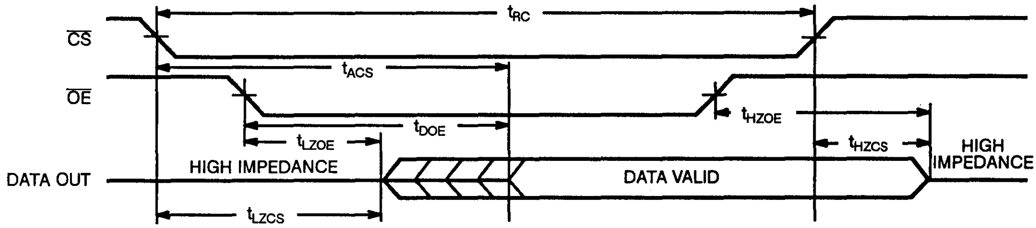
Read Cycle No. 1[9, 10]



C170A-6

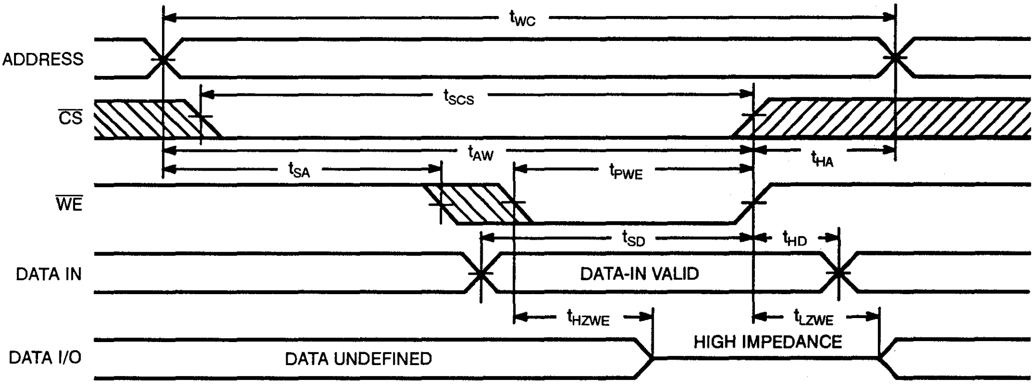
Switching Waveforms (continued)

Read Cycle No. 2[9, 11]



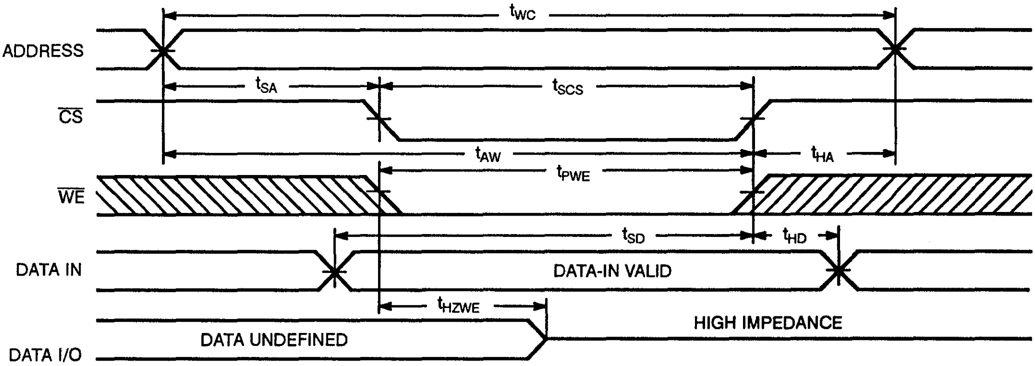
C170A-7

Write Cycle No. 1[8, 12]



C170A-8

Write Cycle No. 2[8, 12, 13]



C170A-9

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C170A–15PC	P9	Commercial
	CY7C170A–15DC	D10	
	CY7C170A–15VC	V13	
20	CY7C170A–20PC	P9	Commercial
	CY7C170A–20DC	D10	
	CY7C170A–20VC	V13	
	CY7C170A–20DMB	D10	Military
	CY7C170A–20KMB	K73	
25	CY7C170A–25PC	P9	Commercial
	CY7C170A–25DC	D10	
	CY7C170A–25VC	V13	
	CY7C170A–25DMB	D10	Military
	CY7C170A–25KMB	K73	
35	CY7C170A–35PC	P9	Commercial
	CY7C170A–35DC	D10	
	CY7C170A–35VC	V13	
	CY7C170A–35DMB	D10	Military
	CY7C170A–35KMB	K73	
45	CY7C170A–45PC	P9	Commercial
	CY7C170A–45DC	D10	
	CY7C170A–45VC	V13	
	CY7C170A–45DMB	D10	Military
	CY7C170A–45KMB	K73	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00096-B

CY7C171
CY7C172

CYPRESS SEMICONDUCTOR

4096 x 4 Static R/W RAM Separate I/O

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **25 ns t_{AA}**
- **Transparent Write (7C171)**
- **Low active power**
  - **385 mW**
- **Low standby power**
  - **83 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C171 and CY7C172 are high-performance CMOS static RAMs organized as 4096 by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

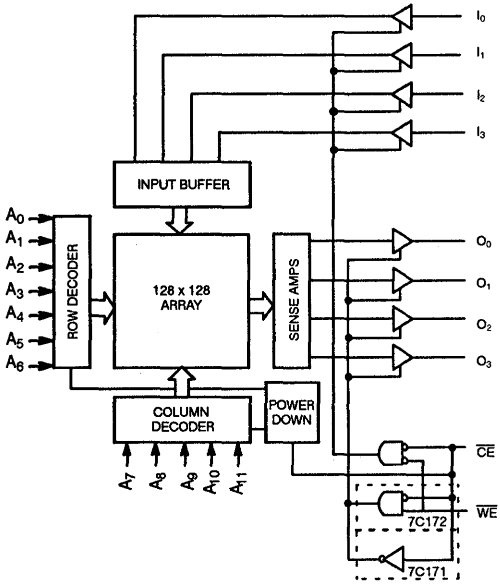
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data output pins (O_0 through O_3).

The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C171 only), or chip enable ($\overline{CE}$) is HIGH.

A die coat is used to insure alpha immunity.

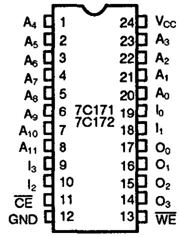
Logic Block Diagram



C171-1

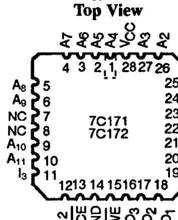
Pin Configurations

DIP/SOJ
Top View



C171-2

LCC
Top View



C171-3

Selection Guide

		7C171-25 7C172-25	7C171-35 7C172-35	7C171-45 7C172-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commerical	90	90	70
	Military		90	70

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with
Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12) .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs
in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C171-25 7C172-25 Min.	Max.	7C171-35 7C172-35 Min.	Max.	7C171-45 7C172-45 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage			– 3.0	0.8	– 3.0	0.8	– 3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		– 10	+ 10	– 10	+ 10	– 10	+ 10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		– 50	+ 50	– 50	+ 50	– 50	+ 50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			– 350		– 350		– 350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		90		90		70	mA
			Mil		90		90		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}	Com'l		20		20		15	mA
			Mil		40		20		20	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V	Com'l		15		15		15	mA
			Mil		40		20		20	mA

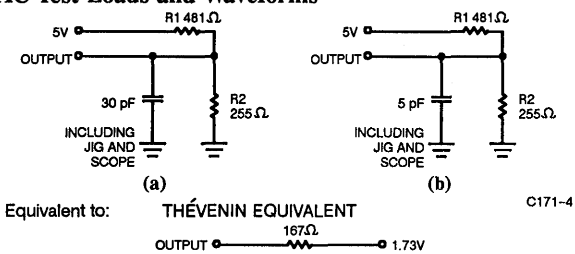
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	pF

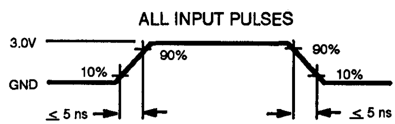
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters

AC Test Loads and Waveforms



C171-4



C171-5

Switching Characteristics Over the Operating Range[2, 5]

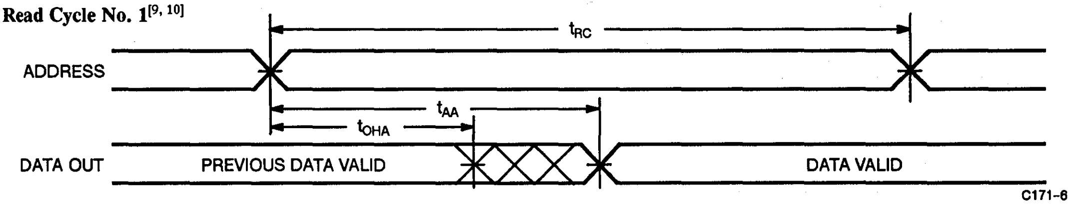
Parameters	Description	7C171-25 7C172-25		7C171-35 7C172-35		7C171-45 7C172-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		10		20		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		25		30	ns
t_{RCS}	Read Command Set-up	0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	25		35		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	25		30		35		ns
t_{AW}	Address Set-Up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6] (7C172)	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7] (7C172)		10		5		20	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C171)		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C171)		25		30		35	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OI}/I_{OH}, and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referencd to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.

Switching Waveforms

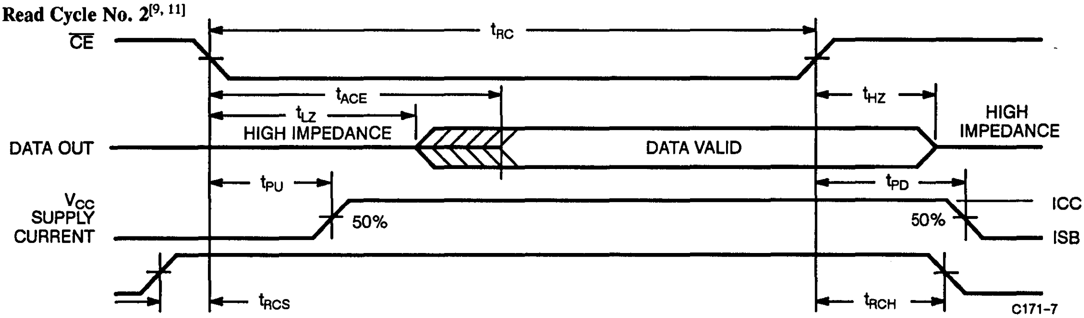
Read Cycle No. 1[9, 10]



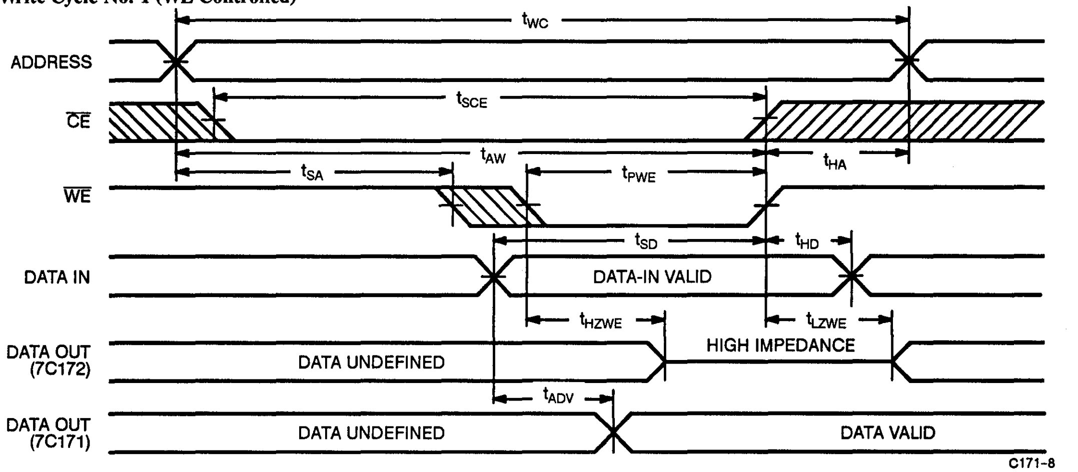
2

Switching Waveforms

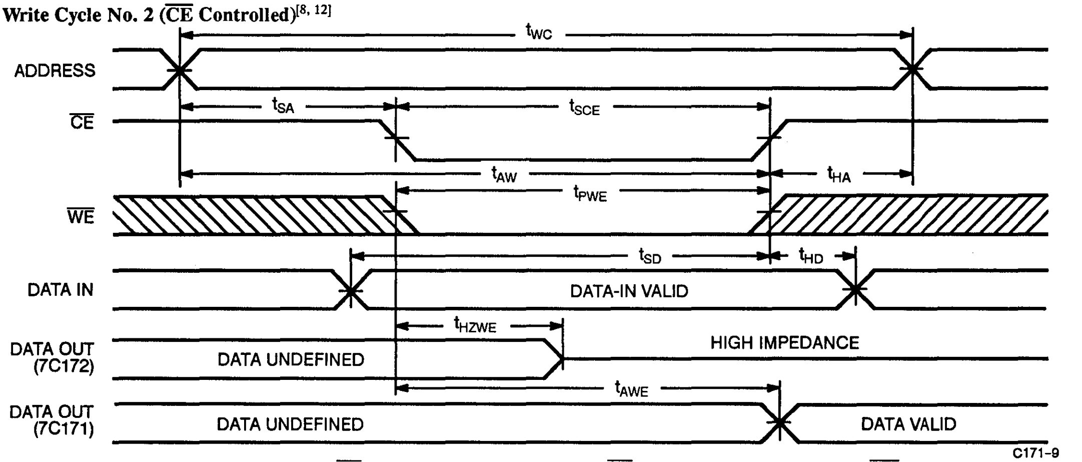
Read Cycle No. 2[9, 11]



Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)[8]



Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)[8, 12]

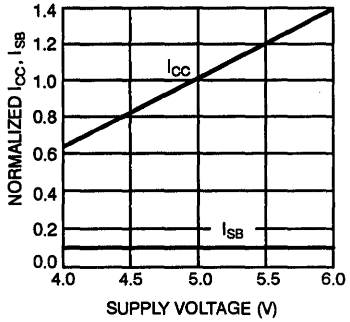


11. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.

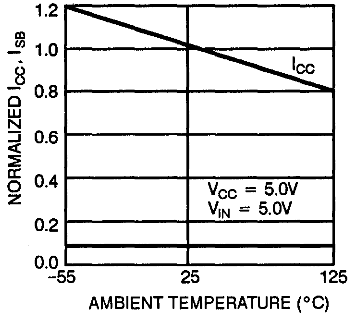
12. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state (7C172).

Typical DC and AC Characteristics

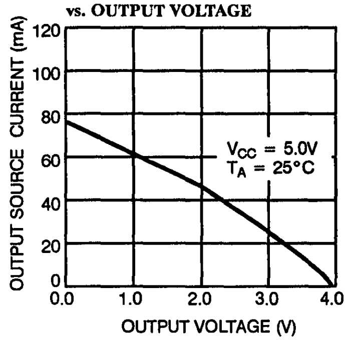
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



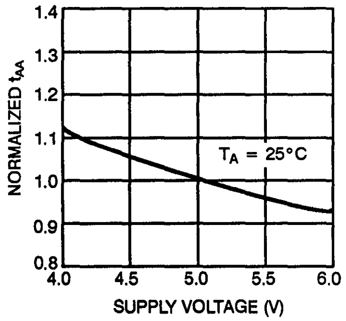
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



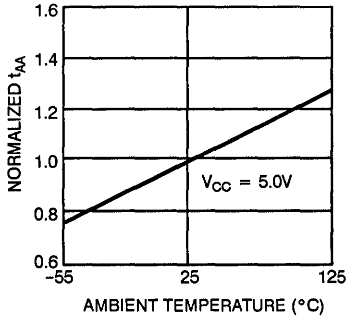
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



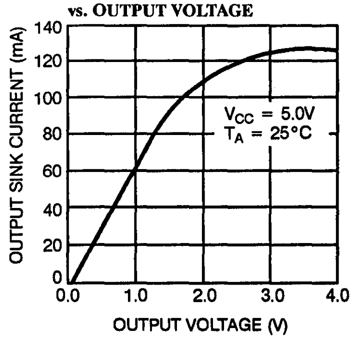
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



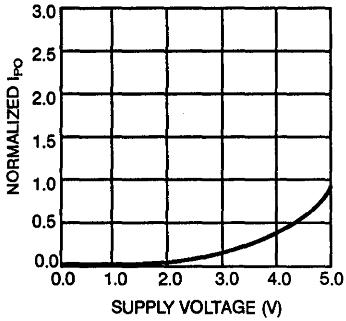
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



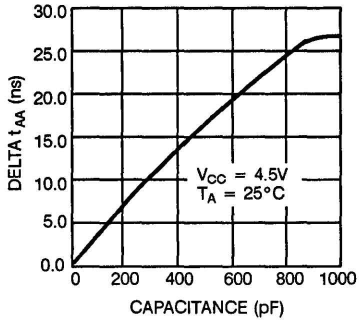
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



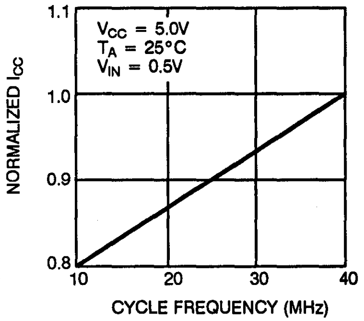
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C171–25PC	P13	Commerical
	CY7C171–25DC	D14	
	CY7C171–25LC	L64	
	CY7C171–25VC	V13	
35	CY7C171–35PC	P13	Commerical
	CY7C171–35DC	D14	
	CY7C171–35LC	L64	
	CY7C171–35VC	V13	
	CY7C171–35DMB	D14	Military
	CY7C171–35LMB	L64	
45	CY7C171–45PC	P13	Commerical
	CY7C171–45DC	D14	
	CY7C171–45LC	L64	
	CY7C171–45VC	V13	
	CY7C171–45DMB	D14	Military
	CY7C171–45LMB	L64	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C172–25PC	P13	Commerical
	CY7C172–25DC	D14	
	CY7C172–25LC	L64	
	CY7C172–25VC	V13	
35	CY7C172–35PC	P13	Commerical
	CY7C172–35DC	D14	
	CY7C172–35LC	L64	
	CY7C172–35VC	V13	
	CY7C172–35DMB	D14	Military
	CY7C172–35LMB	L64	
45	CY7C172–45PC	P13	Commerical
	CY7C172–45DC	D14	
	CY7C172–45LC	L64	
	CY7C172–45VC	V13	
	CY7C172–45DMB	D14	Military
	CY7C172–45LMB	L64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Document #: 38-00036-E

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[13]	7, 8, 9, 10, 11
t_{ADV}[13]	7, 8, 9, 10, 11

Note:
13. 7C171 only.

2

CYPRESS SEMICONDUCTOR

4096 x 4 Static R/W RAM Separate I/O

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **15 ns t_{AA}**
- **Transparent write (7C171A)**
- **Low active power**
  - **375 mW**
- **Low standby power**
  - **93 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C171A and CY7C172A are high-performance CMOS static RAMs organized as 4096 by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

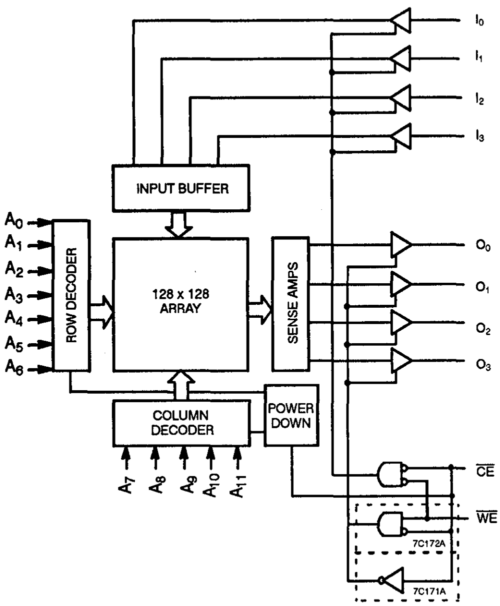
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins remain in a high-impedance state when write enable ($\overline{WE}$) is LOW (7C172A only), or chip enable is HIGH, or ($\overline{OE}$) is HIGH.

A die coat is used to insure alpha immunity.

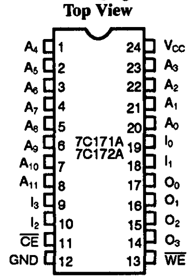
Logic Block Diagram



C171A-1

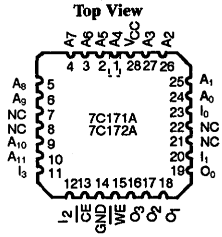
Pin Configurations

DIP/SOJ
Top View



C171A-2

LCC
Top View



C171A-3

Selection Guide

		7C171A-15 7C172A-15	7C171A-20 7C172A-20	7C171A-25 7C172A-25	7C171A-35 7C172A-35	7C171A-45 7C172A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	115	80	70	70	50
	Military		90	80	70	70

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... $-65°C$ to $+150°°C$

Ambient Temperature with Power Applied .... $-55°C$ to $+125°C$

Supply Voltage to Ground Potential .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs in High Z State .... $-0.5V$ to $+7.0V$

DC Input Voltage .... $-3.0V$ to $+7.0V$

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C171A-15 7C172A-15 Min.	Max.	7C171A-20 7C172A-20 Min.	Max.	7C171A-25 7C172A-25 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-10	+10	-10	+10	-10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		-10	+10	-10	+10	-10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-350		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		115		80		70	mA
			Mil				90		80	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%	Com'l		40		40		20	mA
			Mil				40		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Com'l		20		20		20	mA
			Mil				20		20	

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters

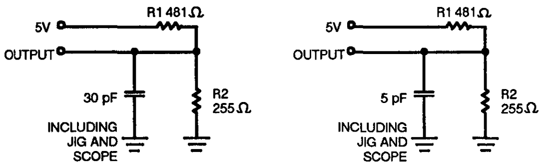
Electrical Characteristics Over the Operating Range [2] (continued)

Parameters	Description	Test Conditions		7C171A-35 7C172A-35		7C171A-45 7C172A-45		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		–10	+10	–10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		70		50	mA
			Mil		70		70	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%	Com'l		20		20	mA
			Mil		20		20	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$ – 0.3V $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq$ 0.3V	Com'l		20		20	mA
			Mil		20		20	

Capacitance[4]

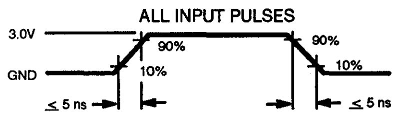
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms



(a) (b)

C171A-4



C171A-5

Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[2, 5]

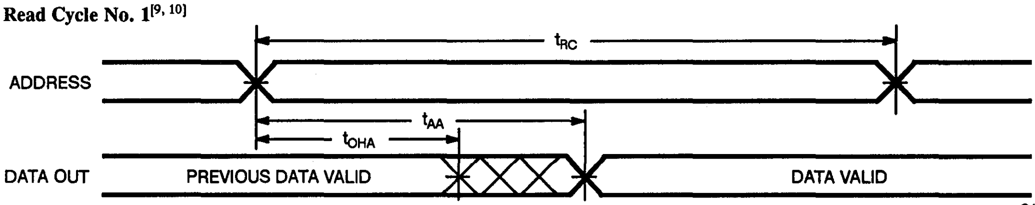
Parameters	Description	7C171A-15 7C172A-15 Min.	7C171A-15 7C172A-15 Max.	7C171A-20 7C172A-20 Min.	7C171A-20 7C172A-20 Max.	7C171A-25 7C172A-25 Min.	7C171A-25 7C172A-25 Max.	7C171A-35 7C172A-35 Min.	7C171A-35 7C172A-35 Max.	7C171A-45 7C172A-45 Min.	7C171A-45 7C172A-45 Max.	Units
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	5		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{LZCE}	$\overline{OE}$ LOW to LOW Z[6]	5		5		5		5		5		ns
t_{HZCE}	$\overline{OE}$ HIGH to HIGH Z[6, 7]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		15		20		20		20		25	ns
t_{RCS}	Read Command Set-up	0		0		0		0		0		ns
t_{RCH}	Read Command Hold	0		0		0		0		0		ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6] (7C172A)	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7] (7C172A)		7		7		7		10		15	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C171A)		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C171A)		15		20		25		30		35	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
7. t_{HZCE} and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referencd to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C172A).

Switching Waveforms

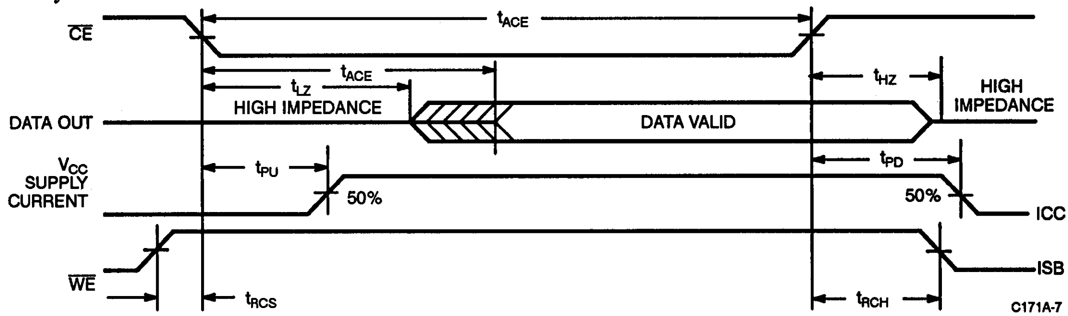
Read Cycle No. 1[9, 10]



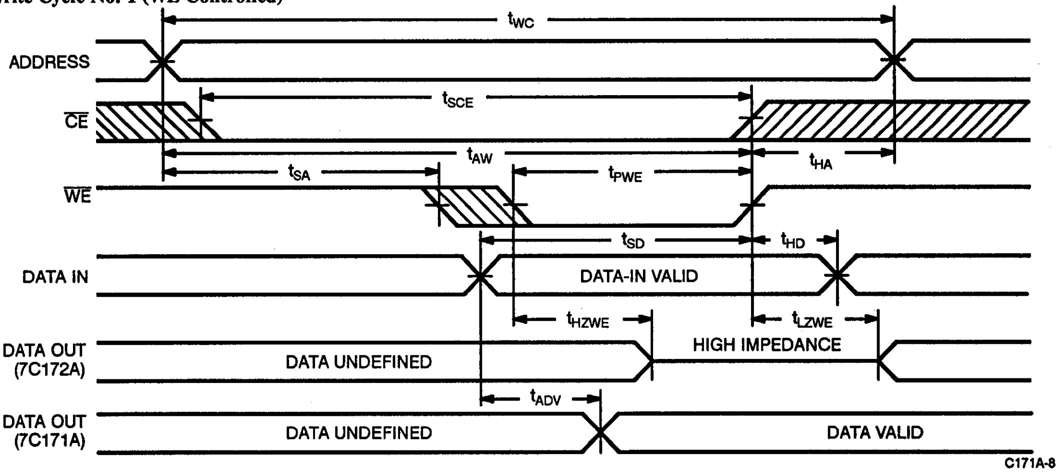
C171A-6

Switching Waveforms

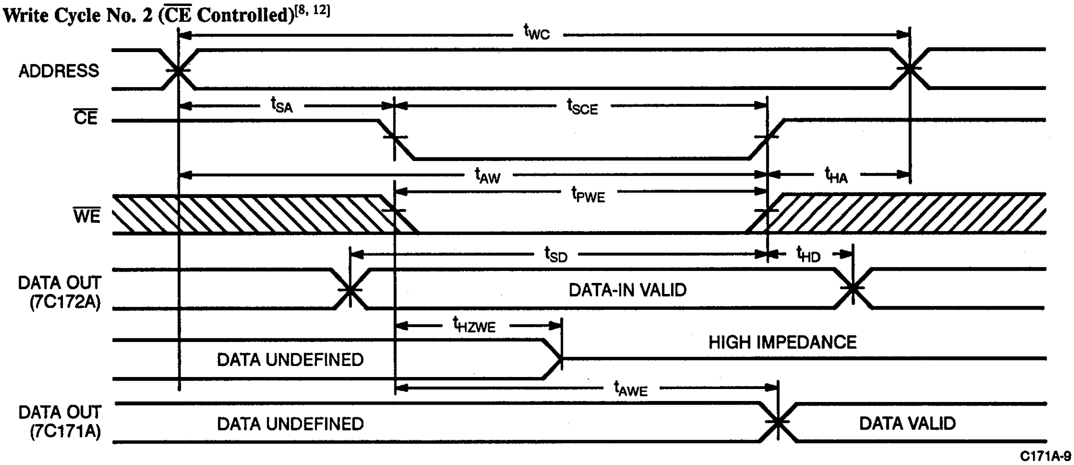
Read Cycle No. 2[9, 11]



Write Cycle No. 1 (WE Controlled)[8]

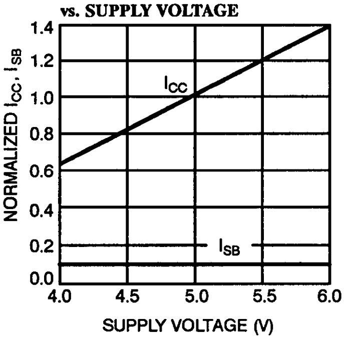


Write Cycle No. 2 (CE Controlled)[8, 12]

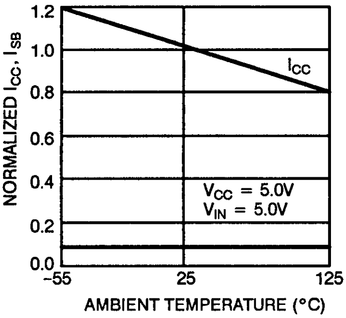


Typical DC and AC Characteristics

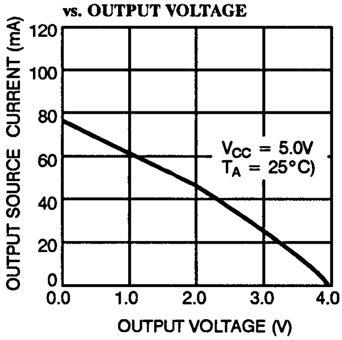
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



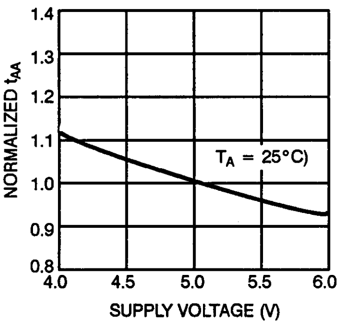
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



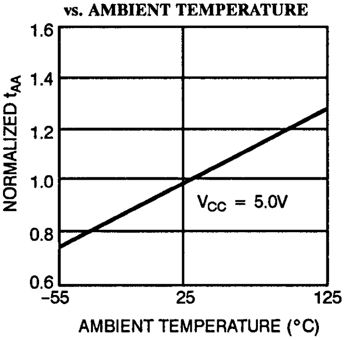
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



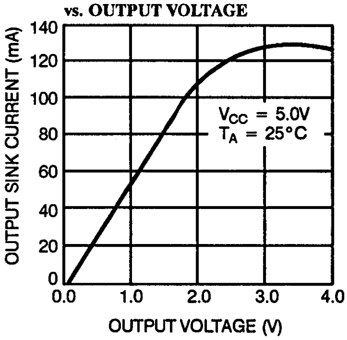
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



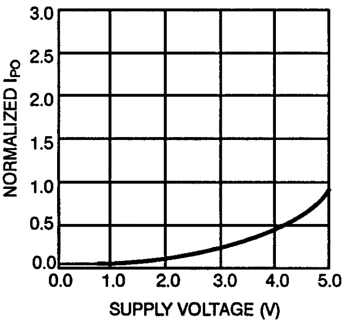
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



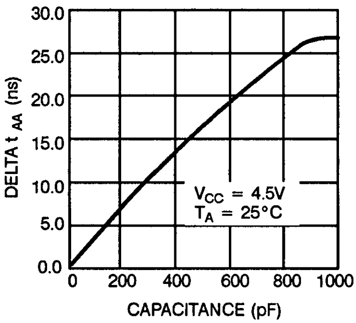
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



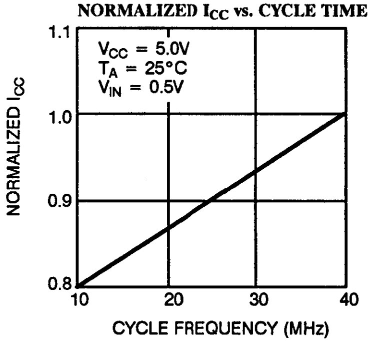
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C171A-15PC	P13	Commercial
	CY7C171A-15DC	D14	
	CY7C171A-15LC	L64	
	CY7C171A-15VC	V13	
20	CY7C171A-20PC	P13	Commercial
	CY7C171A-20DC	D14	
	CY7C171A-20LC	L64	
	CY7C171A-20VC	V13	
	CY7C171A-DMB	D14	Military
	CY7C171A-LMB	L64	
	CY7C171A-KMB	K73	
25	CY7C171A-25PC	P13	Commercial
	CY7C171A-25DC	D14	
	CY7C171A-25LC	L64	
	CY7C171A-25CC	V13	
	CY7C171A-25DMB	D14	Military
	CY7C171A-25LMB	L64	
	CY7C171A-25KMB	K73	
35	CY7C171A-35PC	P13	Commercial
	CY7C171A-35DC	D14	
	CY7C171A-35LC	L64	
	CY7C171A-35VC	V13	
	CY7C171A-35DMB	D14	Military
	CY7C171A-35LMB	L64	
	CY7C171A-35KMB	K73	
45	CY7C171A-45PC	P13	Commercial
	CY7C171A-45DC	D14	
	CY7C171A-45LC	L64	
	CY7C171A-45VC	V13	
	CY7C171A-45DMB	D14	Military
	CY7C171A-45LMB	L64	
	CY7C171A-45KMB	K73	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C172A-15PC	P13	Commercial
	CY7C172A-15DC	D14	
	CY7C172A-15LC	L64	
	CY7C172A-15VC	V13	
20	CY7C172A-20PC	P13	Commercial
	CY7C172A-20DC	D14	
	CY7C172A-20LC	L64	
	CY7C172A-20VC	V13	
	CY7C172A-20DMB	D14	Military
	CY7C172A-20LMB	L64	
	CY7C172A-20KMB	K73	
25	CY7C172A-25PC	P13	Commercial
	CY7C172A-25DC	D14	
	CY7C172A-25LC	L64	
	CY7C172A-25VC	V13	
	CY7C172A-25DMB	D14	Military
	CY7C172A-25LMB	L64	
	CY7C172A-25KMB	K73	
35	CY7C172A-35PC	P13	Commercial
	CY7C172A-35DC	D14	
	CY7C172A-35LC	L64	
	CY7C172A-35VC	V13	
	CY7C172A-35DMB	D14	Military
	CY7C172A-35LMB	L64	
	CY7C172A-35KMB	K73	
45	CY7C172A-45PC	P13	Commercial
	CY7C172A-45DC	D14	
	CY7C172A-45LC	L64	
	CY7C172A-45VC	V13	
	CY7C172A-45DMB	D14	Military
	CY7C172A-45LMB	L64	
	CY7C172A-45KMB	K73	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{RCS}	7, 8, 9, 10, 11
t_{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[13]	7, 8, 9, 10, 11
t_{ADV}[13]	7, 8, 9, 10, 11

Note:
13. 7C171A only.

Document #: 38-00104-B

CYPRESS SEMICONDUCTOR

8,192 x 9 Static R/W RAM

Features

- Fast access time
  - Commercial: 25/35/45/55 ns (max.)
- Low power consumption
  - Active: 935 mW (max.)
- Wide temperature range
  - $-55°C$ to $+125°C$
- 300-mil-width package
- TTL-compatible inputs and outputs
- Asynchronous
- Capable of withstanding greater than 2001V electrostatic discharge
- Single 5V supply

Functional Description

The CY7C182 is a high-speed CMOS static RAM organized as 8,192 by 9 bits and it is manufactured using Cypress's high-performance CMOS technology. Access times as fast as 25 ns are available with maximum power consumption of only 935 mW.

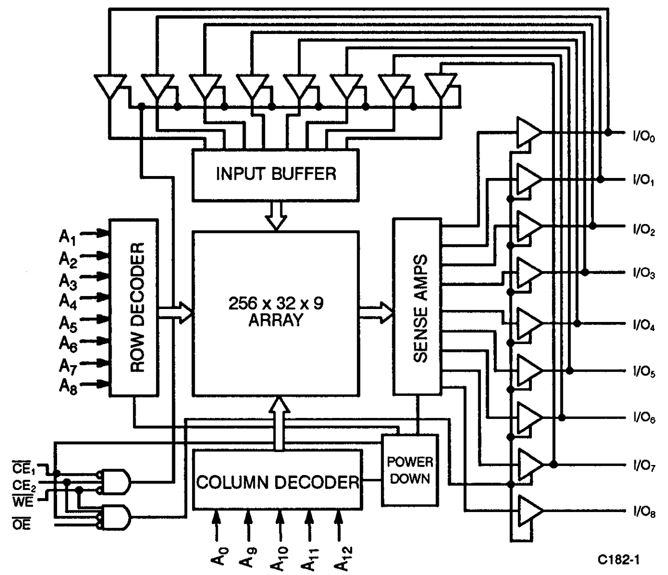
The CY7C182, which is oriented toward cache memory applications, features fully static operation requiring no external clocks or timing strobes. The automatic power-down feature reduces the power consumption by 85% when the circuit is deselected. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE_1}$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW, data on the nine data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE_1}$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the nine data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

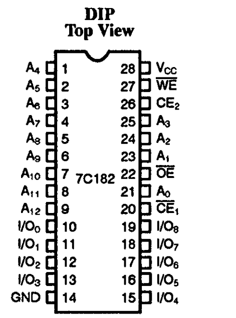
A die coat is used to insure alpha immunity.

Logic Block Diagram



C182-1

Pin Configuration



C182-2

Selection Guide

	7C182-25	7C182-35	7C182-45	7C182-55
Maximum Access Time (ns)	25	35	45	55
Maximum Operating Current (mA)	170	170	170	170
Maximum Standby Current (mA)	25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... − 65°C to + 150°C

Ambient Temperature with Power Applied .... − 55°C to + 125°C

Supply Voltage to Ground Potential .... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... − 0.5V to + 7.0V

DC Input Voltage .... − 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015.2)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C182 Min.	7C182 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} Min., I_{OH} = − 4.0 mA.	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_{IN} \leq V_{CC}$, GND $< V_{OUT} < V_{CC}$, Output Disabled	-10	+10	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND	-10	+10	µA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		-300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} Max., Output Current = 0 mA, f = Max., V_{IN} = V_{CC} or GND		170	mA
I_{SB}	Automatic Power-Down Current	$\overline{CE}_1 \geq V_{IH}$, $CE_2 \leq V_{IL}$		25	mA

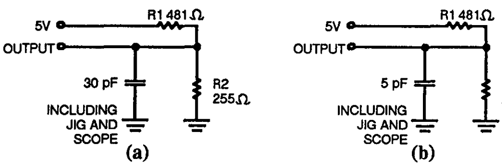
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{IN}	Input Capacitance		5	pF

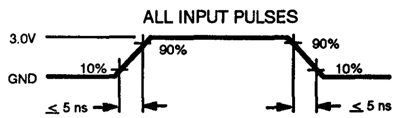
Note:

1. Duration of the short circuit should not exceed 30 seconds. Not more than 1 output should be shorted at one time.
2. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

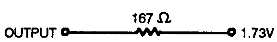


C182-3



C182-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range

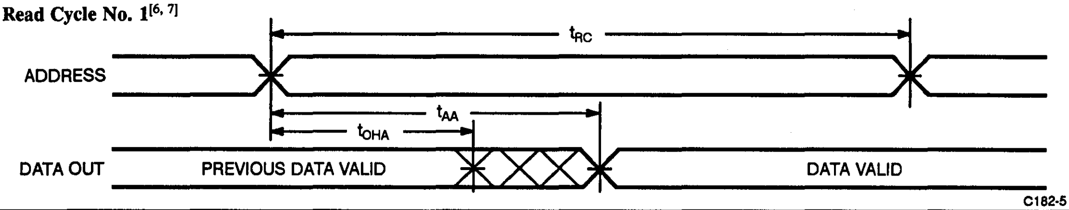
Parameters	Description	7C182-25		7C182-35		7C182-45		7C182-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Address Valid to Low Z	3		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ Access Time		25		35		45		55	ns
t_{ACE2}	CE_2 Access Time		25		25		45		55	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z	5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	5		5		5		5		ns
t_{HZCE1}[3]	$\overline{CE}_1$ HIGH to High Z		20		20		25		25	ns
t_{HZCE2}[3]	CE_2 LOW to High Z		20		20		25		25	
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20		25		25	ns
t_{DOE}	$\overline{OE}$ Access Time		20		20		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		20		25		30	ns
WRITE CYCLE[4]										
t_{WC}	Write Cycle Time	25		35		45		50		ns
t_{SA}	Address Set-Up Time	0		0		0		0		ns
t_{AW}	Address Valid to End of Write	20		30		40		50		ns
t_{SD}	Data Set-Up Time	18		20		25		30		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	20		30		40		50		ns
t_{SCE2}	CE_2 HIGH to Write End	20		30		40		50		ns
t_{HZWE}[5]	Write LOW to High Z[7]		13		15		20		25	ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		35		ns
t_{HA}	Address Hold from End of Write	5		5		5		5		ns
t_{HD}	Data Hold Time	0		0		0		0		ns
t_{LZWE}	Write HIGH to Low Z	3		3		3		3		ns

Notes:

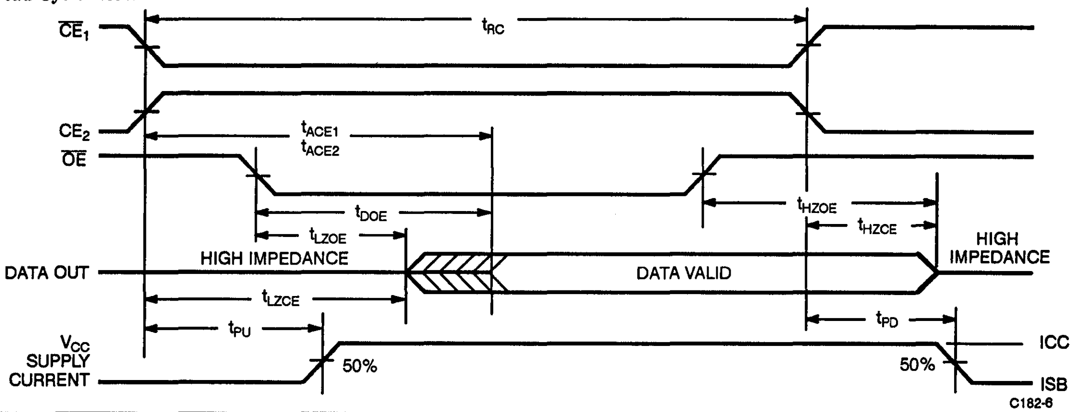
3. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF. Transition is measured ± 500 mV from steady state voltage.
4. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. At any given temperature and voltage condition, t_{LZWE} is less than t_{HZWE} for any given device. These parameters are sampled and not 100% tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$. $CE_2 = V_{IH}$.
8. Address valid prior to or coincident with $\overline{CE}$ transition LOW and CE_2 transition HIGH.
9. If $\overline{CE}_1$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

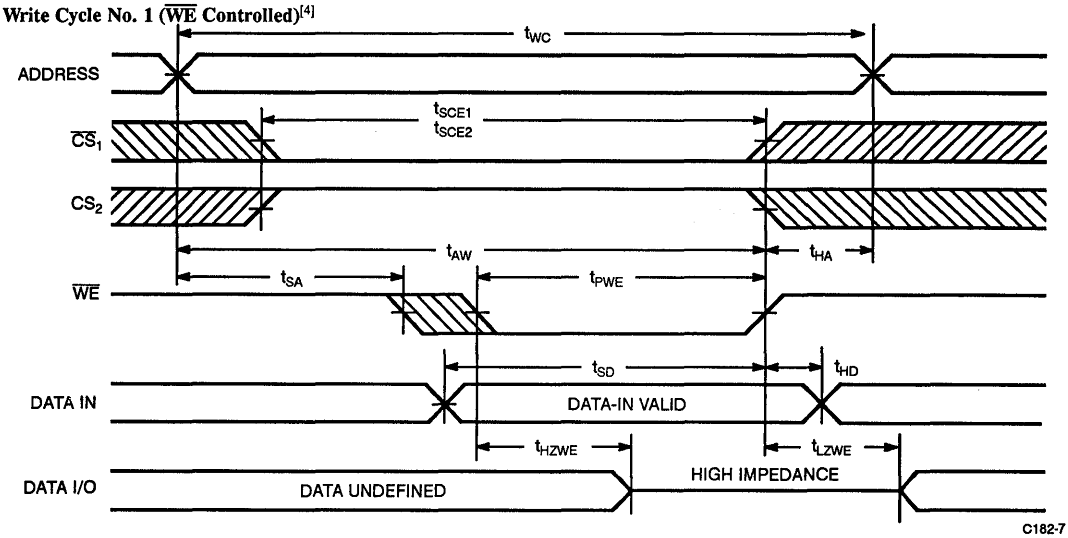
Read Cycle No. 1[6, 7]



Read Cycle No. 2[6, 8]

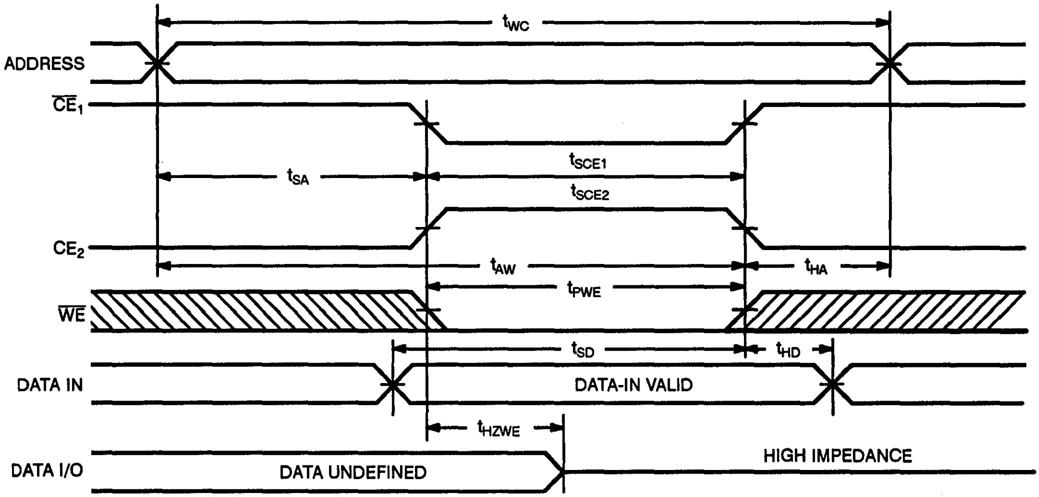


Write Cycle No. 1 ($\overline{WE}$ Controlled)[4]



Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[4, 9]



C182-8

Truth Table

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	Data-In	Data-Out	Mode
H	X	X	X	Z	Z	Deselect/Power-Down
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output Disable
X	L	X	X	Z	Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C182-25PC	P21	Commercial
	CY7C182-25VC	V21	
	CY7C182-25DC	D22	
35	CY7C182-35PC	P21	Commercial
	CY7C182-35VC	V21	
	CY7C182-35DC	D22	
45	CY7C182-45PC	P21	Commercial
	CY7C182-45VC	V21	
	CY7C182-45DC	D22	
55	CY7C182-55PC	P21	Commercial
	CY7C182-55VC	V21	
	CY7C182-55DC	D22	

Document #: 38-00110

CYPRESS SEMICONDUCTOR

2 x 4096 x 16 Cache RAM

Features

- **Pin-programmable into direct-mapped or two-way set associative format**
- **CMOS for optimum speed/power**
- **High speed**
  - **25 ns**
- **Common I/O**
- **Internal address latch**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Compatible with Intel 82385 Cache Controller**

Functional Description

The CY7C183 and CY7C184 are high-performance monolithic CMOS static RAMs that contain 128 kbits organized into either two, two-way set associative blocks of 4K x 16 RAM, or one directly mapped 8K x 16-bit RAM. They are designed specifically for use with the Intel 82385 Cache Controller, and their addresses are latched onthe falling edge of the Address Latch Enable (ALE) signal. When ALE is HIGH, the latch is transparent. The CY7C183 has all address bits latched byt he ALE signal except A_{12}, which is unlatched. A_{12}, which bypasses the latch, has a faster access time. All adress bits are latched by the ALE signal in the CY7C184. The mode pin controls whether they are configured as direct-mapped 8K x 16 or two-way set associative 2 x 4K x 16 RAMs. When mode is HIGH, the circuits are placed in the two-way mode. In the two-way mode, the upper address bit, A_{12} is a "don't care," and is externally wired to ground. When mode is LOW, the circuits are placed in the direct mode.

Writing is accomplished in the two-way mode by taking $\overline{CE}$ LOW and by inserting the respective $\overline{CS}_x$ and $\overline{WE}_x$ signals LOW. $\overline{CS}_0$ enables bits D_0–D_7 while $\overline{CS}_1$ enables bits D_8–D_{15}. $\overline{WE}_A$ enables cache bank A, and $\overline{WE}_B$ enables cache bank B to receive whatever data resides on the data bus. $\overline{OE}_A$ and $\overline{OE}_B$ similarly nable cache banks A and B, respectively, to drive the data bus.

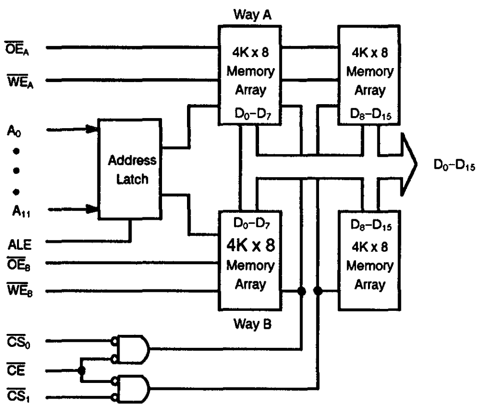
Writing is accomplished, in the direct mode, by tying $\overline{WE}_A$ and $\overline{WE}_B$ together externally, and using A_{12} to determine which 4K x 16 memory bank is selected.

Reading is accomplished in the two-way mode by taking $\overline{CE}$ LOW, inserting the respective $\overline{OE}_x$ and $\overline{CS}_x$ signals LOW and the respective $\overline{WE}_x$ signal HIGH. The contents of the memory location specified on the address pins will appear on the 16 outputs. Activation of $\overline{OE}_A$ and $\overline{OE}_B$ simultaneously will cause both banks to be deselected. Reading is accomplished in the direct mode by tying $\overline{OE}_A$ and $\overline{OE}_B$ together externally. A_{12} will determine which 4K x 16 memory bank is enabled.

2

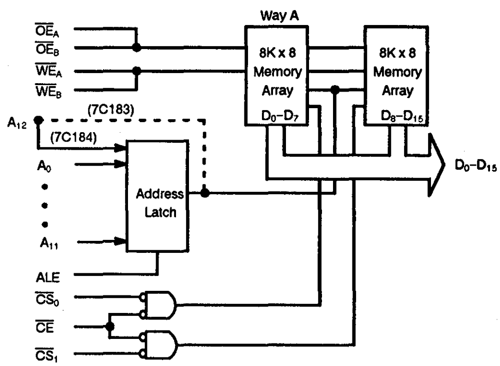
Logic Block Diagrams

TwoWay Set Associative (Mode = HIGH)



C183-1

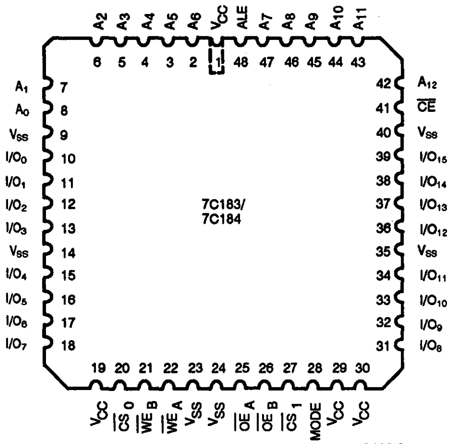
Direct Map (Mode = LOW)



C183-2

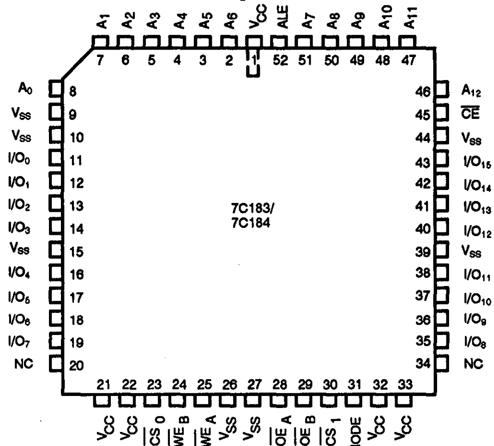
Pin Diagrams

LCC
Top View



C183-3

PLCC
Top View



C183-4

Selection Guide

		7C183-25 7C184-25	7C183-35 7C184-35	7C183-45 7C184-45
Maximum Address Access Time (ns)	Commercial	25	35	45
	Military	25	35	45
Maximum Output Enable Access Time (ns)	Commercial	10	14	16
	Military	125	14	16
Maximum Operating Current (mA)	Commercial	220	170	140
	Military		200	160

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... − 65°C to + 150°C

Ambient Temperature with Power Applied .... − 55°C to + 125°C

Supply Voltage to Ground Potential .... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... − 0.5V to + 7.0V

DC Input Voltage .... − 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

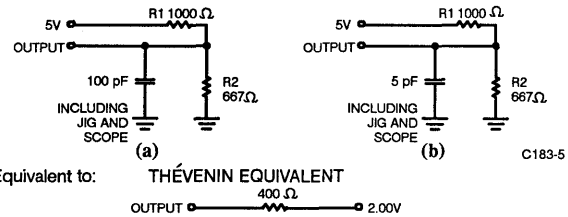
Electrical Characteristics Over the Operating Range[2]

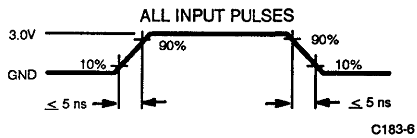
Parameters	Description	Test Conditions		7C183-25 7C184-25 Min.	7C183-25 7C184-25 Max.	7C183-35 7C184-35 Min.	7C183-35 7C184-35 Max.	7C183-45 7C184-45 Min.	7C183-45 7C184-45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled		−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA Read Cycle[4] Duty Cycle = 45%	Com'l		220		170		140	mA
			Mil				200		160	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms





Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. At a given duty cycle, Write Cycle I_{CC} is equal to 1.4 times Read Cycle I_{CC}.
5. Tested initially and after any design or process changes that may affect these parameters.
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

Switching Characteristics Over the Operating Range[2,6]

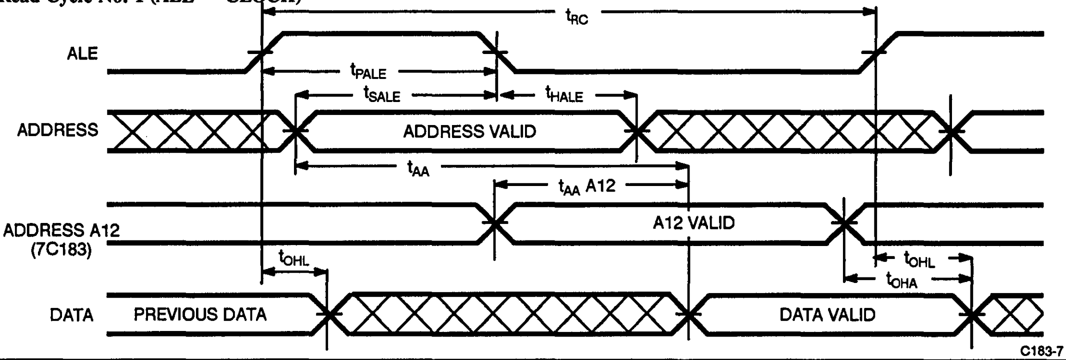
Parameters	Description	7C183-25 7C184-25		7C183-35 7C184-35		7C183-45 7C184-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE[7]								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{AA} A_{12}[8]	Address to Data Valid A_{12}		17		25		35	ns
t_{CE}	Chip Enable to Data Valid		12		15		20	ns
t_{CS}	Chip Select to Data Valid		12		15		20	ns
t_{OE}	Output Enable to Data Valid		10		14		16	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{OHL}	Output Hold from ALE HIGH	3		3		3		ns
t_{LZCE}	Chip Enable to Low Z	3		3		3		ns
t_{LZOE}	Output Enable to Low Z	0		0		0		ns
t_{HZCE}	Chip Enable to High Z		15		25		30	ns
t_{HZOE}	Output Enable to High Z		9		10		12	ns
t_{PALE}	ALE Pulse Width	8		10		12		ns
t_{SALE}	Address Set-Up to ALE Low	4		6		8		ns
t_{HALE}	Address Hold to ALE Low	4		4		4		ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{AW}	Address Set-Up to Write End	20		30		40		ns
t_{SCE}	Chip Enable to Write End	20		25		30		ns
t_{SCS}	Chip Select to Write End	20		25		30		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{PWE}	Write Enable Pulse Width	20		25		30		ns
t_{SA}	Address Set-Up to Write Enable	0		0		0		ns
t_{HA}	Address Hold from Write Enable	0		0		0		ns
t_{LZWE}	Write Enable HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		15		15		20	ns
t_{PALE}	ALE Pulse Width	8		10		12		ns
t_{SALE}	Address Set-Up to ALE Low	4		6		8		ns
t_{HALE}	Address Hold to ALE Low	4		4		4		ns

Notes:

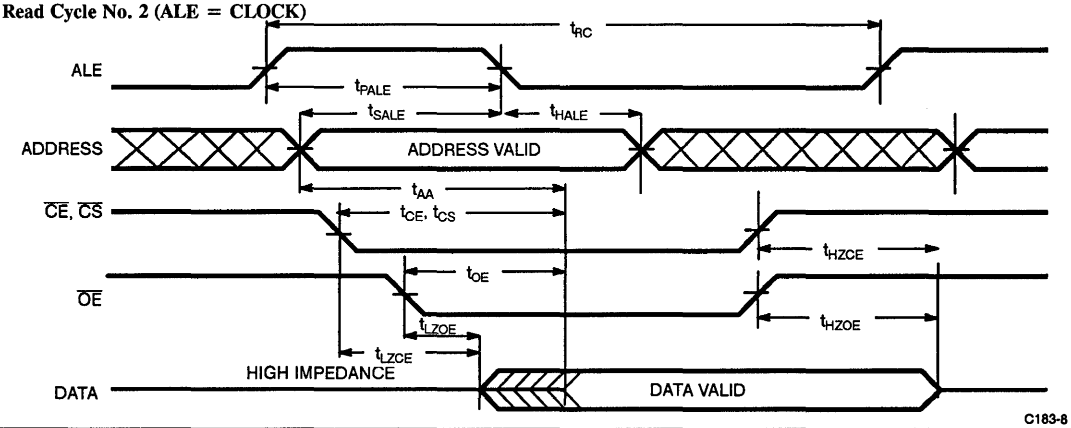
7. Both $\overline{WE}_A$ and $\overline{WE}_B$ must be HIGH for read cycle.
8. CY7C183 only.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$, $\overline{CS}_x$, and $\overline{WE}_x$. All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. Device is continuously selected, $\overline{CE}$ and $\overline{CS}$ are LOW.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. $\overline{WE}$ is HIGH for read cycle.
13. $\overline{OE}$ is deselected (HIGH).

Switching Waveforms

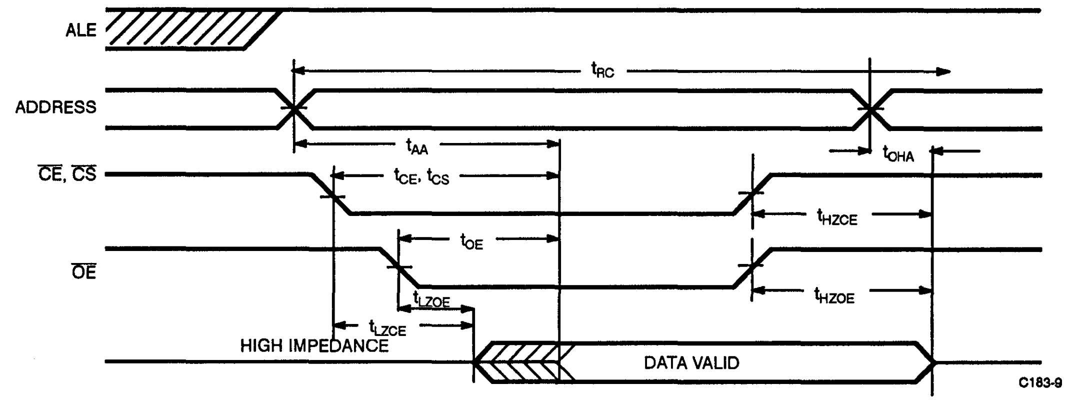
Read Cycle No. 1 (ALE = CLOCK) [10]



Read Cycle No. 2 (ALE = CLOCK)

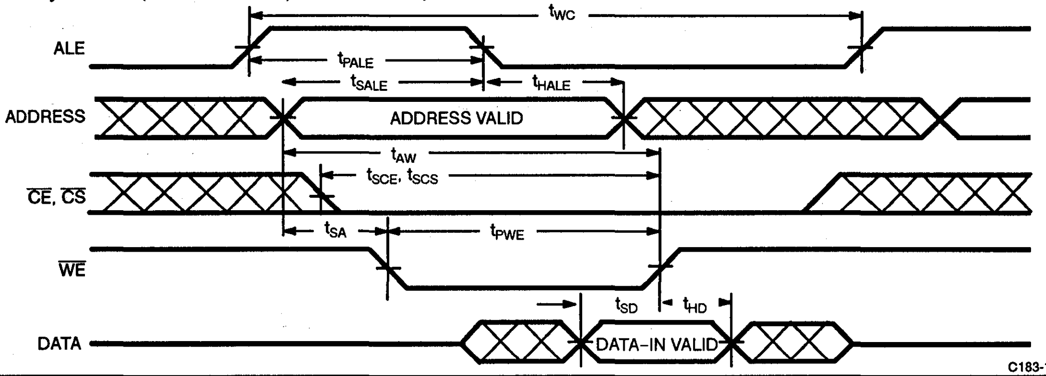


Read Cycle No. 3 (ALE = HIGH) [11, 12]



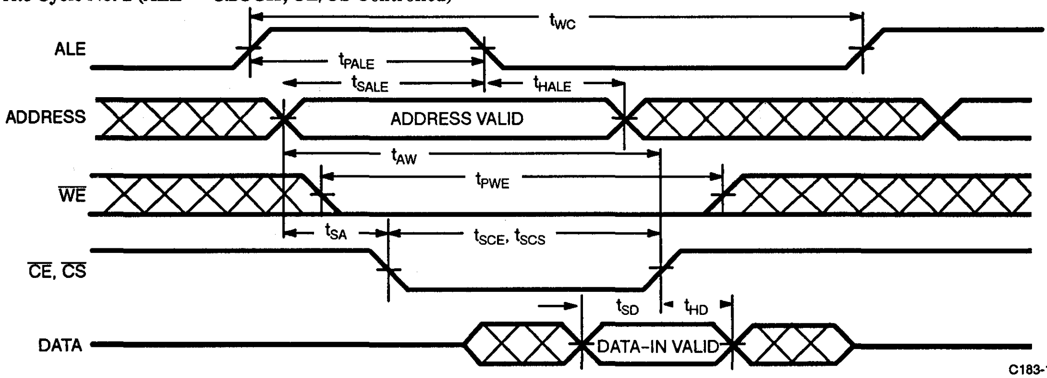
Switching Waveforms (continued)

Write Cycle No. 1 (ALE = CLOCK, $\overline{\text{WE}}$ Controlled) [13]



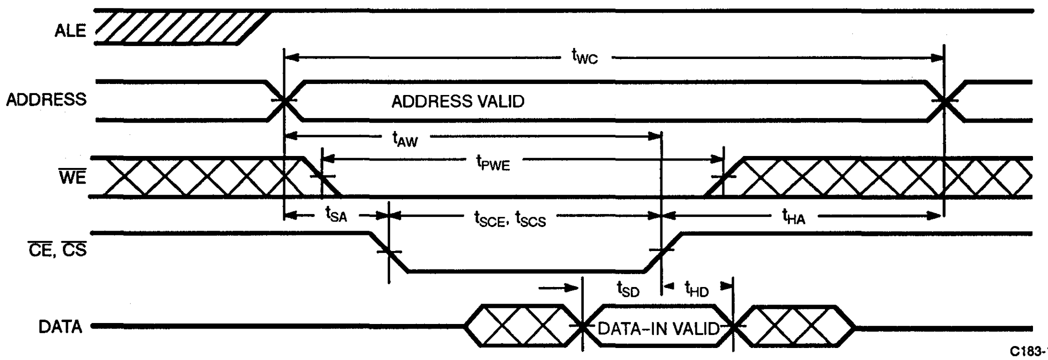
C183-10

Write Cycle No. 2 (ALE = CLOCK, $\overline{\text{CE}}/\overline{\text{CS}}$ Controlled) [13]



C183-11

Write Cycle No. 3 (ALE = HIGH, $\overline{\text{CE}}/\overline{\text{CS}}$ Controlled) [13]



C183-12

Truth Tables

Two-Way Mode (Mode = HIGH)

$\overline{CE}$	$\overline{CS}_0$	$\overline{CS}_1$	$\overline{OE}_A$	$\overline{OE}_B$	$\overline{WE}_A$	$\overline{WE}_B$	Operation	
H	X	X	X	X	X	X	Outputs High Z, Write Disabled	
L	H	H	X	X	X	X	Outputs High Z, Write Disabled	
X	X	X	H	H	X	X	Outputs High Z	
X	X	X	L	L	X	X	Outputs High Z	
L	L	H	L	H	H	H	Read I/O_0–I/O_7	Way A
L	L	H	H	L	H	H	Read I/O_0–I/O_7	Way B
L	H	L	L	H	H	H	Read I/O_8–I/O_{15}	Way A
L	H	L	H	L	H	H	Read I/O_8–I/O_{15}	Way B
L	L	L	L	H	H	H	Read I/O_0–I/O_{15}	Way A
L	L	L	H	L	H	H	Read I/O_0–I/O_{15}	Way B
L	L	H	X	X	L	H	Write I/O_0–I/O_7	Way A
L	L	H	X	X	H	L	Write I/O_0–I/O_7	Way B
L	H	L	X	X	L	H	Write I/O_8–I/O_{15}	Way A
L	H	L	X	X	H	L	Write I/O_8–I/O_{15}	Way B
L	L	L	X	X	L	H	Write I/O_0–I/O_{15}	Way A
L	L	L	X	X	H	L	Write I/O_0–I/O_{15}	Way B
L	L	H	X	X	L	L	Write I/O_0–I/O_7	Way A & B
L	H	L	X	X	L	L	Write I/O_8–I/O_{15}	Way A & B
L	L	L	X	X	L	L	Write I/O20$_{-I/O}$15	Way A & B

Direct Mode (Mode = LOW)

$\overline{CE}$	$\overline{CS}_0$	$\overline{CS}_1$	$\overline{OE}_A$	$\overline{OE}_B$	$\overline{WE}_A$	$\overline{WE}_B$	Operation
H	X	X	X	X	X	X	Outputs High Z, Write Disabled
L	H	H	X	X	X	X	Outputs High Z, Write Disabled
X	X	X	H	H	X	X	Outputs High Z
L	L	H	L	L	H	H	Read I/O_0–I/O_7
L	H	L	L	L	H	H	Read I/O_8–I/O_{15}
L	L	L	L	L	H	H	Read I/O_0–I/O_{15}
L	L	H	X	X	L	L	Read I/O_0–I/O_7
L	H	L	X	X	L	L	Read I/O_8–I/O_{15}
L	L	L	X	X	L	L	Read I/O_0–I/O_{15}

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C183-25JC	J69	Commercial
35	CY7C183-35JC	J69	Commercial
	CY7C183-35LMB	L68	Military
45	CY7C183-45JC	J69	Commercial
	CY7C183-45LMB	L68	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C184-25JC	J69	Commercial
35	CY7C184-35JC	J69	Commercial
	CY7C184-35LMB	L68	Military
45	CY7C184-45JC	J69	Commercial
	CY7C184-45LMB	L68	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00090-A

CYPRESS SEMICONDUCTOR

8,192 x 8 Static RAM

Features

- **BiCMOS for optimum speed/power**
- **High speed**
  - **— 12 ns**
- **Low active power**
  - **— 600 mW**
- **Low standby power**
  - **— 200 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

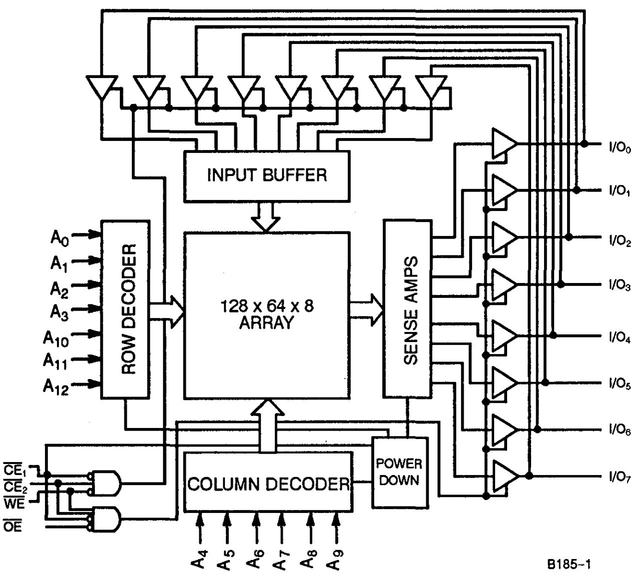
Functional Description

The CY7B185 and CY7B186 are high-performance BiCMOS static RAMs organized as 8,192 words by 8 bits. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have a power-down feature ($\overline{CE}_1$) that reduces the power consumption by 67% when deselected. The CY7B185 is in the space saving 300-mil-wide DIP package and leadless chip carrier. The CY7B186 is in the standard 600-mil-wide package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}_1$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains HIGH. Under these conditions, the contents of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

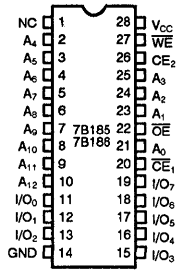
Logic Block Diagram



B185-1

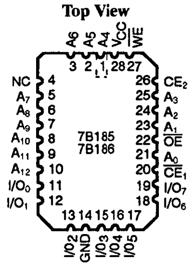
Pin Configurations

DIP
Top View



B185-2

LCC
Top View



B185-3

Selection Guide

		7B185-12 7B186-12	7B185-15 7B186-15
Maximum Access Time (ns)		12	15
Maximum Operating Current (mA)	Commercial	140	135
	Military		145
Maximum Standby Current (mA)	Commercial	40	40
	Military		50

Maximum Rating

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

Input Voltage [1] .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... > 2001V
(Per MIL-STD-883 Method 3015)

Latch-Up Current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military [2]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range [3]

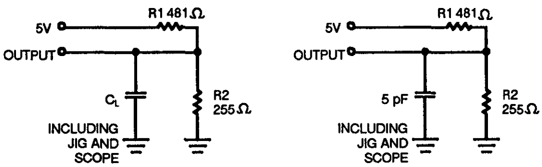
Parameters	Description	Test Conditions			7B185-12 7B186-12 Min.	7B185-12 7B186-12 Max.	7B185-15 7B186-15 Min.	7B185-15 7B186-15 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = – 4.0 mA	Com'l	2.4		2.4		V
			I_{OH} = – 2.0 mA	Mil	2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]				– 0.5	0.8	– 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			– 10	+ 10	– 10	+ 10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled			– 10	+ 10	– 10	+ 10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA f = f max.		Com'l		140		135	mA
				Mil				145	mA
I_{SB}	$\overline{CE}_1$ Power-Down Current	$\overline{CE}_1$ ≥ V_{IH}		Com'l		40		40	mA
				Mil				50	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.[5]	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

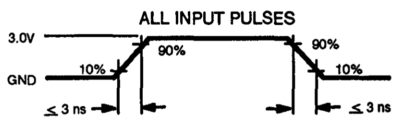
Notes:
1. V_{IL} (min.) = – 3.0V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Tested initially and after any design or process changes that may affect these parameters.
5. For all packages except CERDIP (D16, D22), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.

AC Test Loads and Waveforms



(a) (b)

B185-4



B185-5

Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range [3, 6]

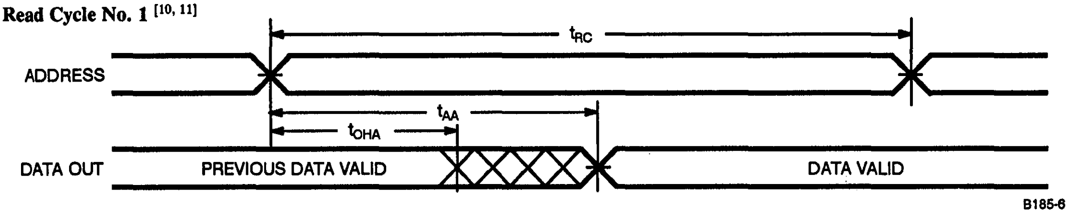
Parameters	Description	7B185-12 7B186-12 Min.	7B185-12 7B186-12 Max.	7B185-15 7B186-15 Min.	7B185-15 7B186-15 Max.	Units
READ CYCLE						
t_{RC}	Read Cycle Time	12		15		ns
t_{AA}	Address to Data Valid		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		12		15	ns
t_{ACE2}	CE_2 HIGH to Data Valid		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [7]		8		8	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z [8]	3		3		ns
t_{LZCE2}	CE_2 HIGH to Low Z [8]	3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z [6, 7] CE_2 LOW to High Z		7		8	ns
WRITE CYCLE[9]						
t_{WC}	Write Cycle Time	12		15		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	8		10		ns
t_{SCE2}	CE_2 HIGH to Write End	8		10		ns
t_{AW}	Address Set-Up to Write End	8		10		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		ns
t_{SD}	Data Set-Up to Write End	6.5		8		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		7		7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		ns

Notes:

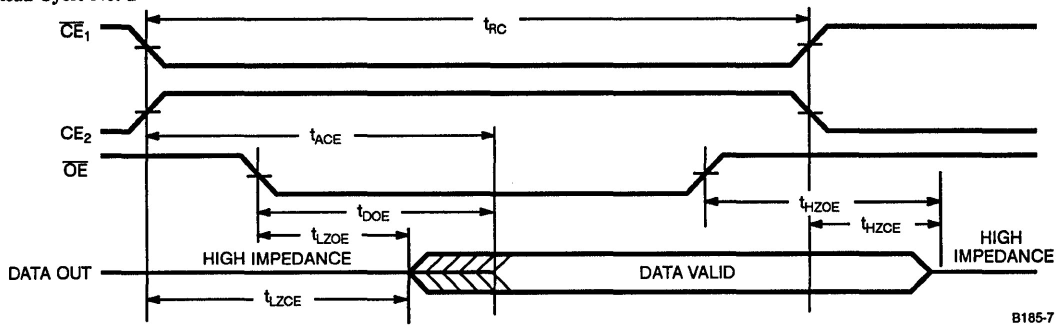
6. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and C_L = 20 pF.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write. All three signals must be active to initiate a write, and either signal can terminate a write by going inactive.

Switching Waveforms

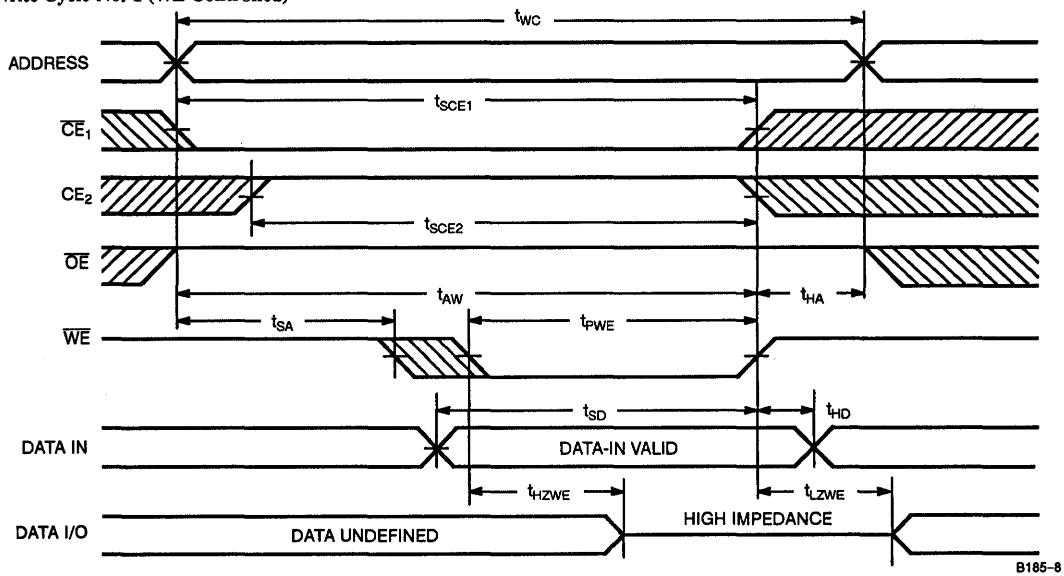
Read Cycle No. 1 [10, 11]



Read Cycle No. 2 [10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [8, 13]



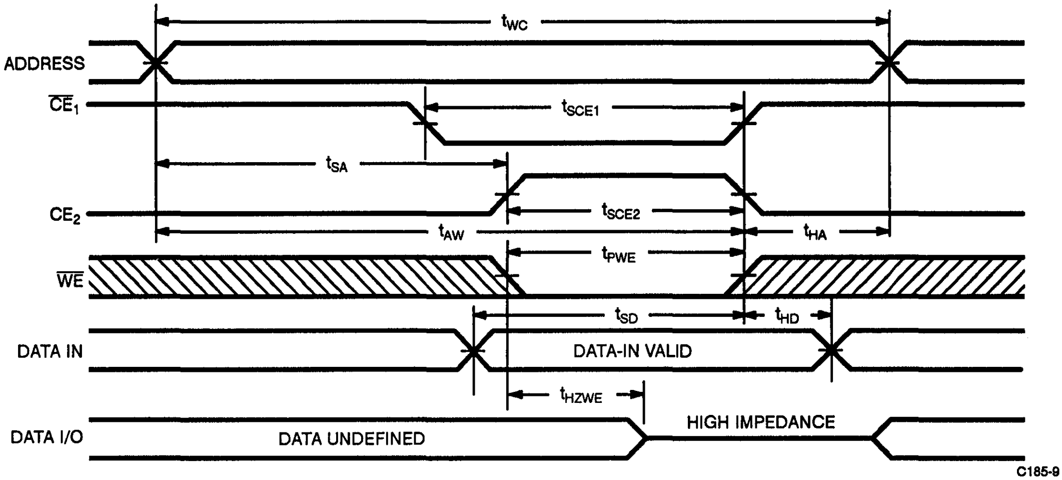
Notes:

10. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}. CE_2 = V_{IH}.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. $\overline{WE}$ is HIGH for read cycle.
13. Data I/O is HIGH impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

2

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [8, 12, 14]



Truth Table

$\overline{\text{CE}}_1$	CE_2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
L	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B185-12PC	P21	Commercial
	CY7B185-12VC	V21	
	CY7B185-12DC	D22	
15	CY7B185-15PC	P21	Commercial
	CY7B185-15VC	V21	
	CY7B185-15DC	D22	
	CY7B185-15DMB	D22	Military
	CY7B185-15LMB	L54	

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7B186-12PC	P15	Commercial
15	CY7B186-15PC	P15	Commercial
	CY7B186-15DMB	D16	Military

Document #: 38-A-00016-A

CY7C185
CY7C186

CYPRESS SEMICONDUCTOR

8,192 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **20 ns**
- **Low active power**
  - **550 mW**
- **Low Standby Power**
  - **110 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

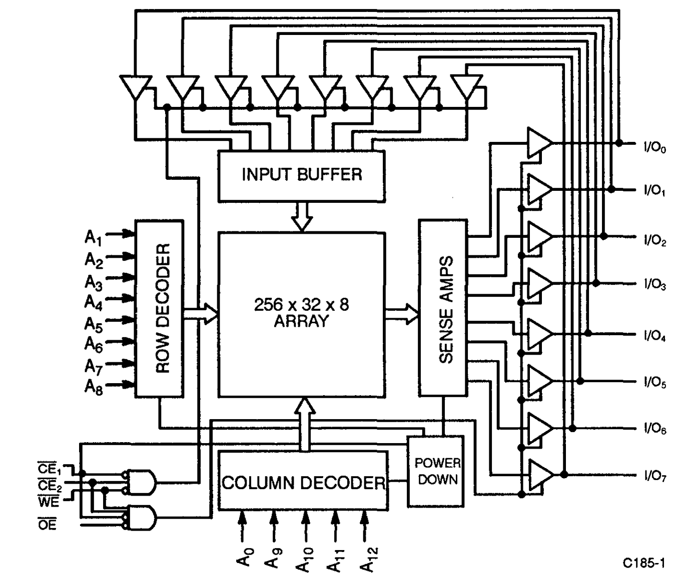
Functional Description

The CY7C185 and CY7C186 are high-performance CMOS static RAMs organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}_1$), an active HIGH chip enable (CE_2), and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have an automatic power-down feature ($\overline{CE}_1$), reducing the power consumption by 73% when deselected. The CY7C185 is in the space-saving 300-mil-wide DIP package and leadless chip carrier. The CY7C186 is in the standard 600-mil-wide package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}_1$ and $\overline{WE}$ inputs are both LOW and CE_2 is HIGH, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}_1$ and $\overline{OE}$ active LOW, CE_2 active HIGH, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to insure alpha immunity.

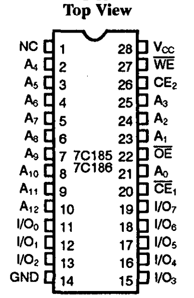
Logic Block Diagram



C185-1

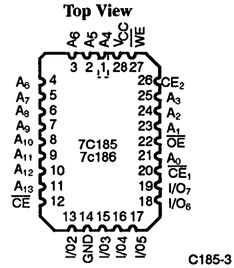
Pin Configurations

DIP
Top View



C185-2

LCC
Top View



C185-3

Selection Guide

	7C185-20 7C186-20	7C185-25 7C186-25	7C185-35 7C186-35	7C185-45 7C186-45	7C185-55 7C186-55
Maximum Access Time (ns)	20	25	35	45	55
Maximum Operating Current (mA)	120	100	100	100	80
Maximum Standby Current (mA)	20/20	20/20	20/20	20/20	20/20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range

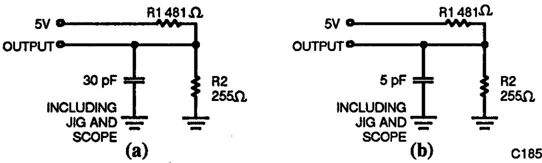
Parameters	Description	Test Conditions	7C185-20 7C186-20		7C185–25,35,45 7C186–25,35,45		7C185-55 7C186-55		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA	2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	-10	+10	-10	+10	-10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled	-10	+10	-10	+10	-10	+10	μA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND		-300		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		120		100		80	mA
I_{SB1}	Automatic $\overline{CE_1}$ Power-Down Current	Max. V_{CC}, $\overline{CE_1} \geq V_{IH}$, Min. Duty Cycle = 100%		20		20		20	mA
I_{SB2}	Automatic $\overline{CE_1}$ Power-Down Current	Max. V_{CC}, $\overline{CE_1} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		20		20		20	mA

Capacitance[3]

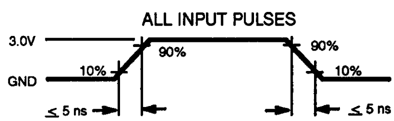
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
1. V_{IL} min. = –3.0V for pulse durations less than 30 ns.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



C185-4



C185-5

Equivalent to:

Switching Characteristics Over the Operating Range[4]

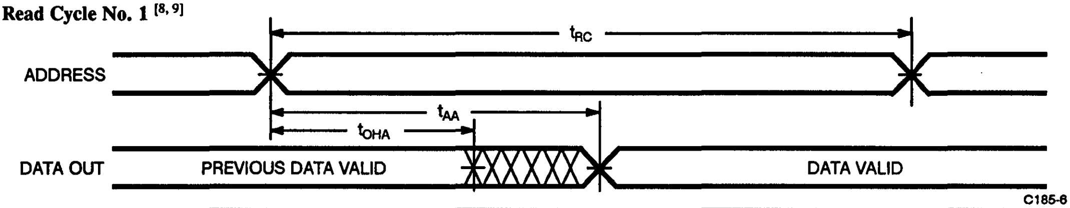
Parameters	Description	7C185-20 7C186-20		7C185-25 7C186-25		7C185-35 7C186-35		7C185-45 7C186-45		7C185-55 7C186-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	20		25		35		45		55		ns
t_{AA}	Address to Data Valid		20		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		20		25		35		45		55	ns
t_{ACE2}	CE_2 HIGH to Data Valid		20		25		25		30		40	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		12		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]		8		10		12		15		20	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[6]	5		5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[7,8] CE_2 LOW to High Z		8		10		15		15		20	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20		20		25		25	ns
WRITE CYCLE[7]												
t_{WC}	Write Cycle Time	20		20		25		40		50		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	15		20		25		30		40		ns
t_{SCE2}	CE_2 HIGH to Write End	15		20		20		25		30		ns
t_{AW}	Address Set-Up to Write End	15		20		25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		20		20		25		ns
t_{SD}	Data Set-Up to Write End	10		10		15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		7		7		10		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

Notes:

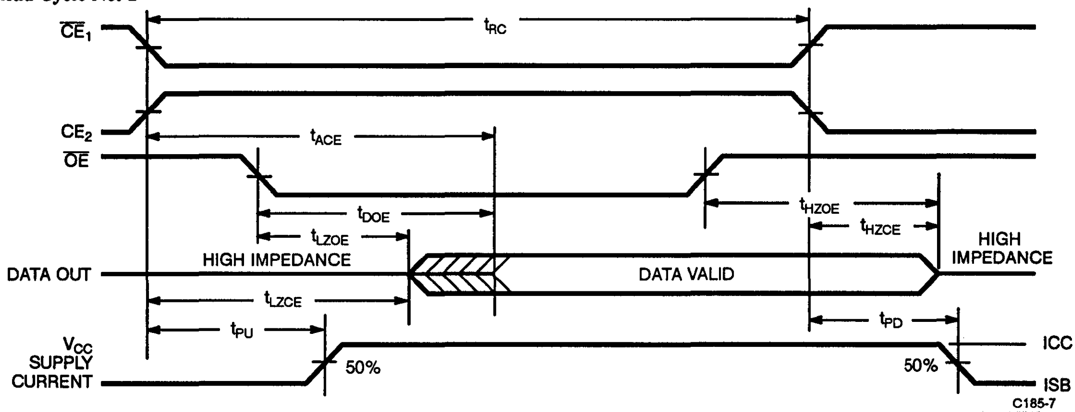
4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$. $CE_2 = V_{IH}$.
9. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
10. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms

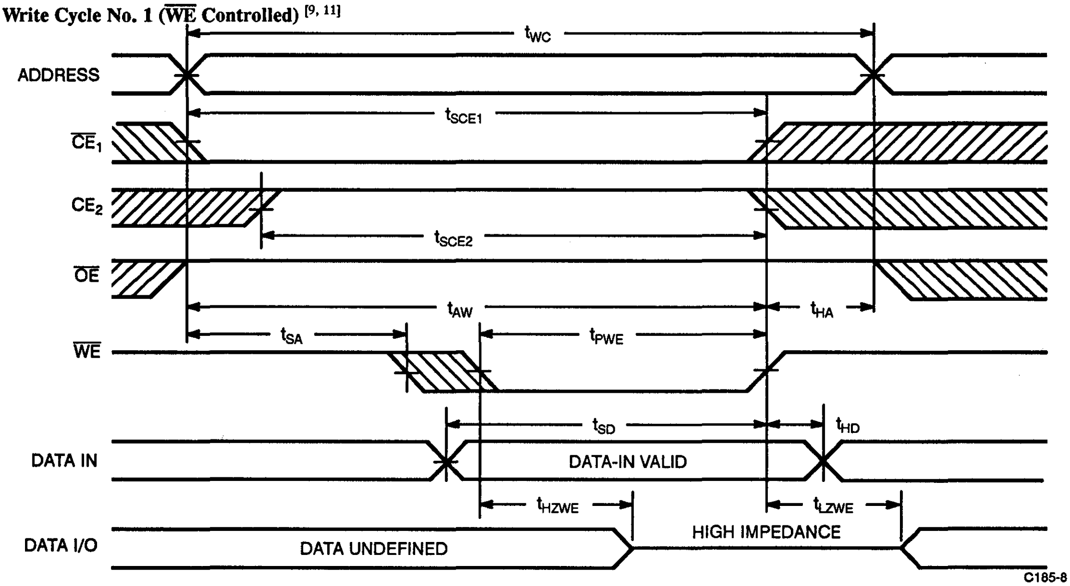
Read Cycle No. 1 [8, 9]



Read Cycle No. 2 [10, 11]



Write Cycle No. 1 ($\overline{WE}$ Controlled) [9, 11]

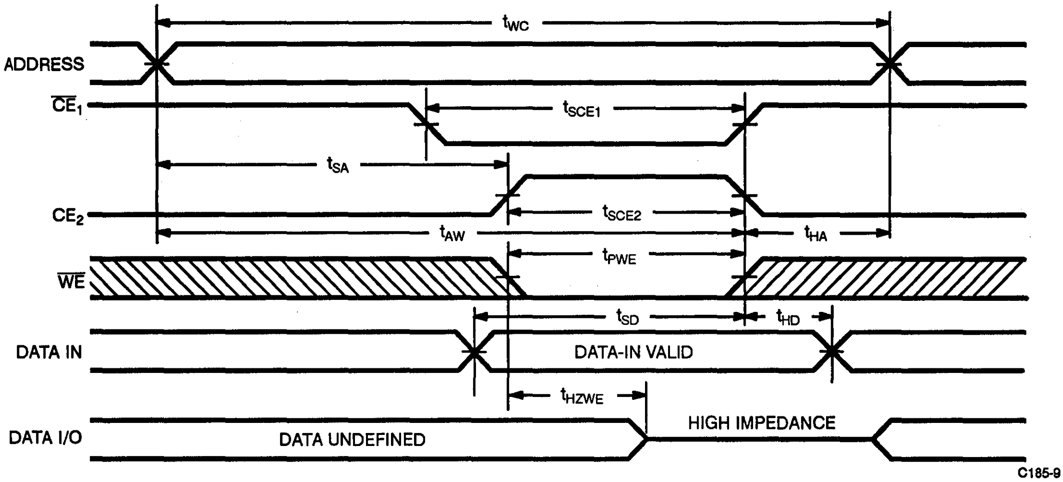


Notes:

11. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

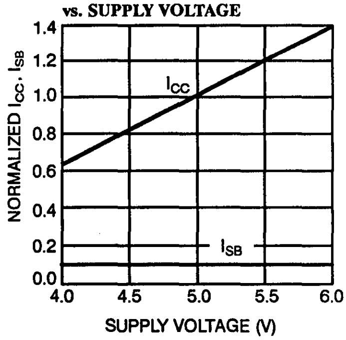
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) [9, 11, 12]

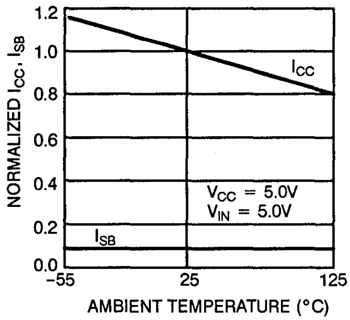


Typical DC and AC Characteristics

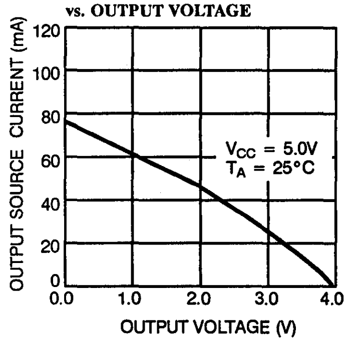
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



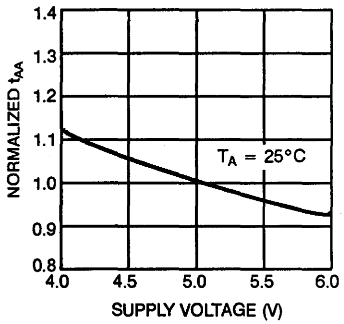
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



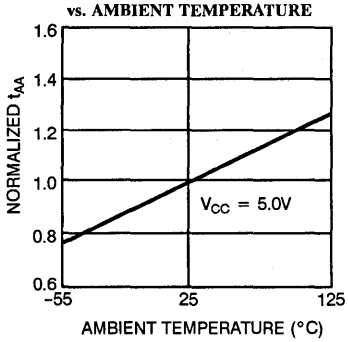
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



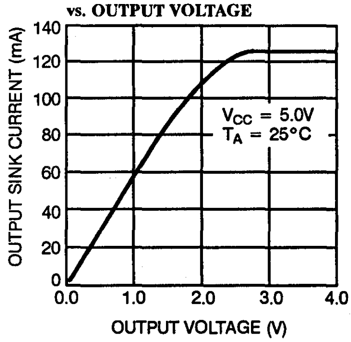
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

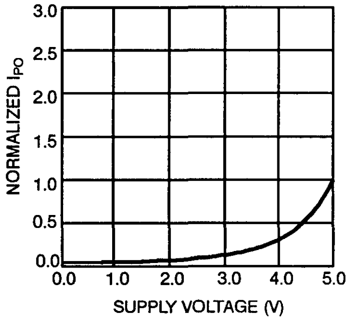


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

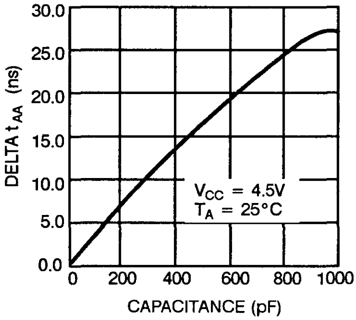


Typical DC and AC Characteristics (continued)

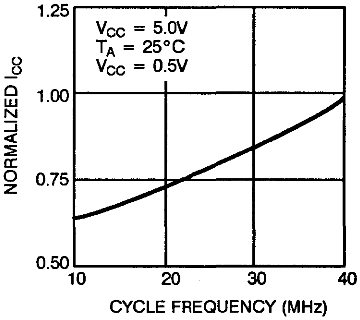
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME

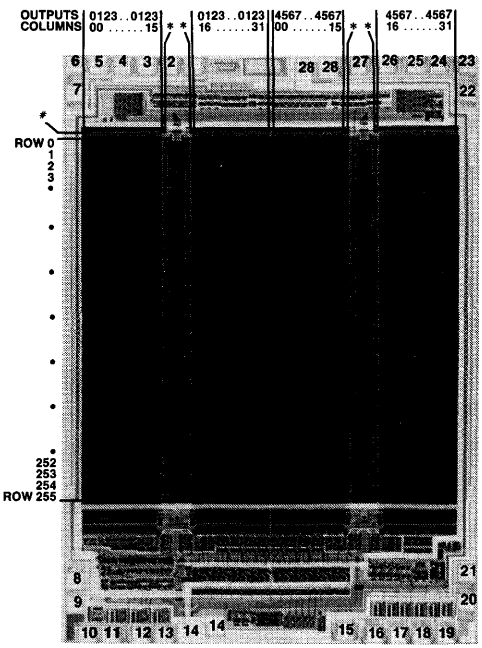


2

Truth Table

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Bit Map



Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C185-20PC	P21	Commercial
	CY7C185-20VC	V21	
	CY7C185-20DC	D22	
	CY7C185-20LC	L54	
25	CY7C185-25PC	P21	Commercial
	CY7C185-25VC	V21	
	CY7C185-25DC	D22	
	CY7C185-25LC	L54	
35	CY7C185-35PC	P21	Commercial
	CY7C185-35VC	V21	
	CY7C185-35DC	D22	
	CY7C185-35LC	L54	
45	CY7C185-45PC	P21	Commercial
	CY7C185-45VC	V21	
	CY7C185-45DC	D22	
	CY7C185-45LC	L54	
55	CY7C185-55PC	P21	Commercial
	CY7C185-55VC	V21	
	CY7C185-55DC	D22	
	CY7C185-55LC	L54	

20	CY7C186-20PC	P15	Commercial
	CY7C186-20DC	D16	
25	CY7C186-25PC	P15	Commercial
	CY7C186-25DC	D16	
35	CY7C186-35PC	P15	Commercial
	CY7C186-35DC	D16	
45	CY7C186-45PC	P15	Commercial
	CY7C186-45DC	D16	
55	CY7C186-55PC	P15	Commercial
	CY7C186-55DC	D16	

Document #: 38-00037-F

CYPRESS SEMICONDUCTOR

8,192 x 8 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **20 ns**
- **Low active power**
  - **688 mW**
- **Low standby Power**
  - **220 mW**
- **TTL-compatible imputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C185A and CY7C186A are high-performance CMOS static RAMs organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE_1}$), an active HIGH chip enable (CE_2), an active LOW output enable ($\overline{OE}$), and three-state drivers. Both devices have an automatic power-down feature ($\overline{CE_1}$), reducing the power consumption by 68% when deselected. The CY7C185A is in the space saving 300-mil-wide DIP package and leadless chip carrier. The CY7C186A is in the standard 600-mil-wide package.

Writing to the device is accomplished when the chip enable one ($\overline{CE_1}$) and write enable ($\overline{WE}$) inputs are both LOW, and the chip enable two (CE_2) input is HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{12}).

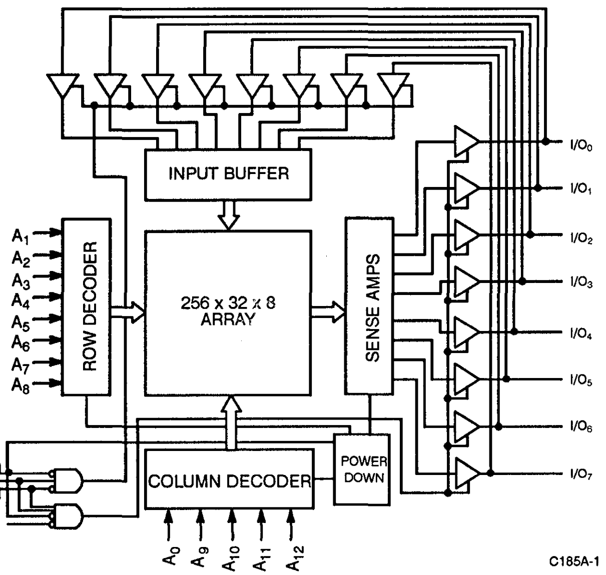
Reading the device is accomplished by taking chip enable one ($\overline{CE_1}$) and output enable ($\overline{OE}$) LOW, while taking write enable ($\overline{WE}$) and chip enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in high-impedance state when chip enable one ($\overline{CE_1}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) or chip enable two (CE_2) is LOW.

A die coat is used to insure alpha immunity.

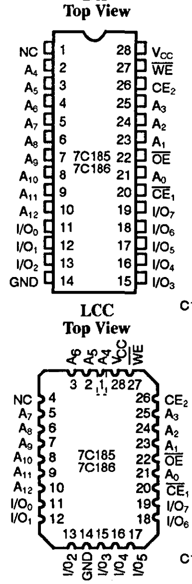
2

Logic Block Diagram



C185A-1

Pin Configurations



C185A-2

C185A-3

Selection Guide

		7C185A-20 7C186A-20	7C185A-25 7C186A-25	7C185A-35 7C186A-35	7C185A-45 7C186A-45	7C185A-55 7C186A-55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	125	125	125	125	125
	Military	135	125	125	125	125
Maximum Standby Current (mA)	Commercial	40/20	30/20	30/20	30/20	30/20
	Military	40/20	40/20	30/20	30/20	30/20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... − 65°C to + 150°C

Ambient Temperature with Power Applied .... − 55°C to + 125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) .... − 0.5V to + 7.0V

DC Voltage Applied to Outputs in High Z State .... − 0.5V to + 7.0V

DC Input Voltage .... − 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C185A-20 7C186A-20		7C185A-25 7C186A-25		7C185A-35,45,55 7C186A-35,45,55		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]			-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		−10	+ 10	−10	+ 10	−10	+ 10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled		−10	+ 10	−10	+ 10	−10	+ 10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND			-300		-300		-300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		125		125		125	mA
			Mil		135		125		125	mA
I_{SB1}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{IH}$, Min. Duty Cycle = 100%	Com'l		40		30		30	mA
			Mil		40		40		30	mA
I_{SB2}	Automatic $\overline{CE}_1$ Power-Down Current	Max. V_{CC}, $\overline{CE}_1 \geq V_{CC}$ -0.3V $V_{IN} \geq V_{CC}$ -0.3V or $V_{IN} \geq$ 0.3V	Com'l		20		20		20	mA
			Mil		20		20		20	mA

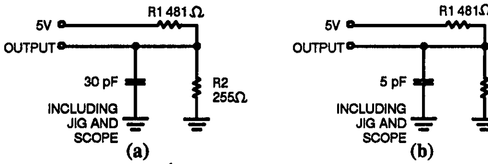
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

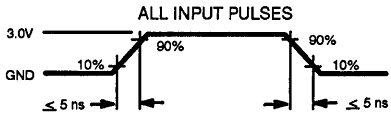
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} (min.) = − 3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after may design or process changes that may affect these parameters.
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}. CE_2 = V_{IH}.
10. Address valid prior to or coincident with $\overline{CE}$ transition low.
11. $\overline{WE}$ is HIGH for read cycle.
12. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
13. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

AC Test Loads and Waveforms



C185A-4



C185A-5

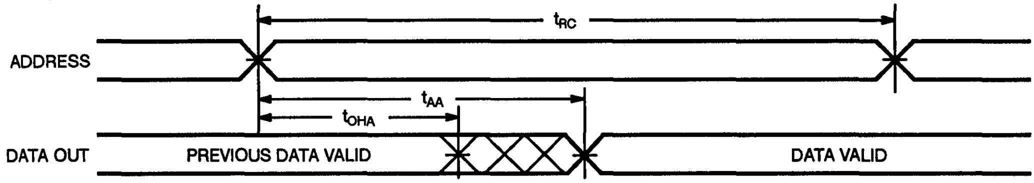
Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[2, 6]

Parameters	Description	7C185A–20 7C186A–20		7C185A–25 7C186A–25		7C185A–35 7C186A–35		7C185A–45 7C186A–45		7C185A–55 7C186A–55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	20		25		35		45		55		ns
t_{AA}	Address to Data Valid		20		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		3		ns
t_{ACE1}	$\overline{CE}_1$ LOW to Data Valid		20		25		35		45		55	ns
t_{ACE2}	CE_2 HIGH to Data Valid		20		25		25		30		40	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		12		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7]		8		10		12		15		20	ns
t_{LZCE1}	$\overline{CE}_1$ LOW to Low Z[8]	5		5		5		5		5		ns
t_{LZCE2}	CE_2 HIGH to Low Z	3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z[7, 8] CE_2 LOW to High Z		8		10		15		15		20	ns
t_{PU}	$\overline{CE}_1$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power-Down		20		20		20		25		25	ns
WRITE CYCLE[9]												
t_{WC}	Write Cycle Time	20		20		25		40		50		ns
t_{SCE1}	$\overline{CE}_1$ LOW to Write End	15		20		25		30		40		ns
t_{SCE2}	CE_2 HIGH to Write End	15		20		20		25		30		ns
t_{AW}	Address Set-Up to Write End	15		20		25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		15		20		20		25		ns
t_{SD}	Data Set-Up to Write End	10		10		15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7]		7		7		10		15		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		5		5		ns

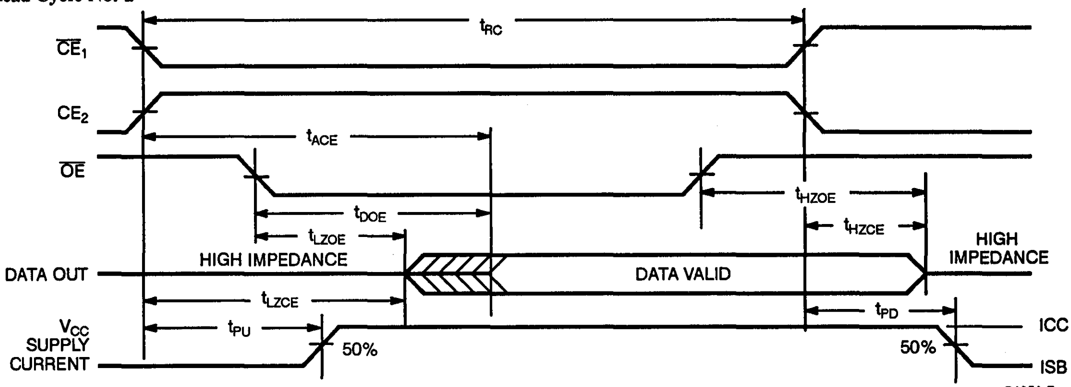
Switching Waveforms

Read Cycle No. 1 [9, 10]



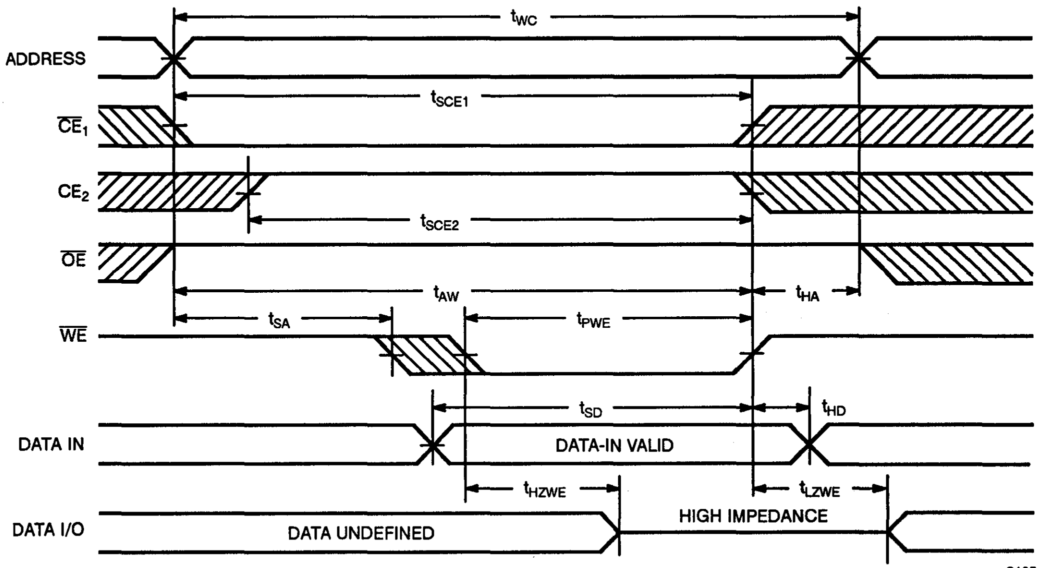
C185A-6

Read Cycle No. 2 [10, 11]



C185A-7

Write Cycle No. 1 ($\overline{WE}$ Controlled) [12, 13]

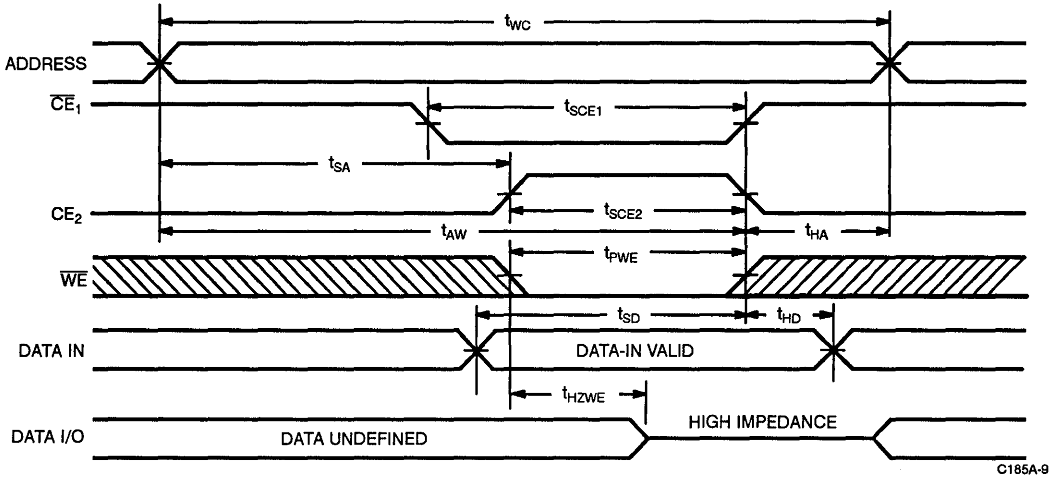


C185A-8

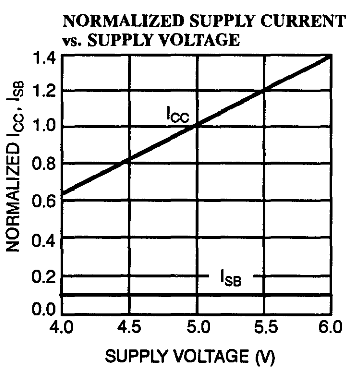
2

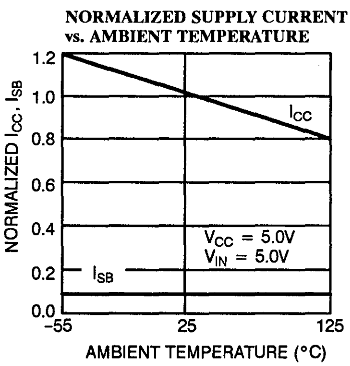
Switching Waveforms (continued)

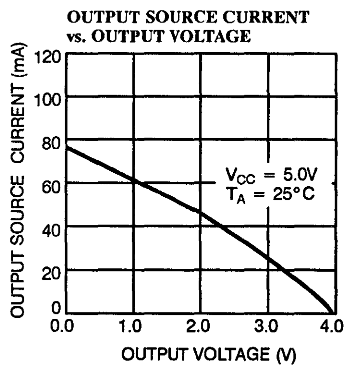
Write Cycle No. 2 ($\overline{CE}$ Controlled) [12, 13, 14]

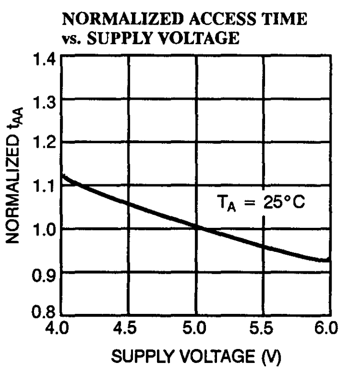


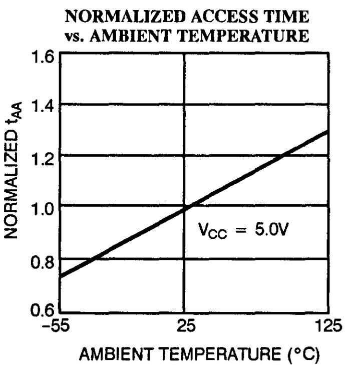
Typical DC and AC Characteristics

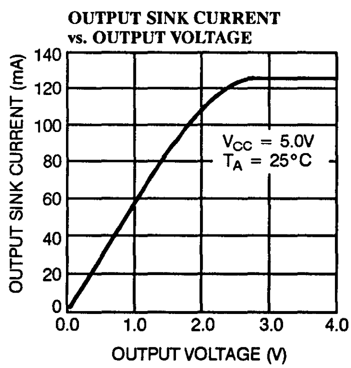




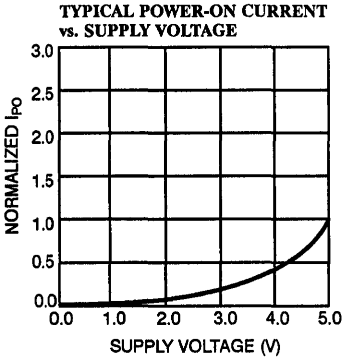


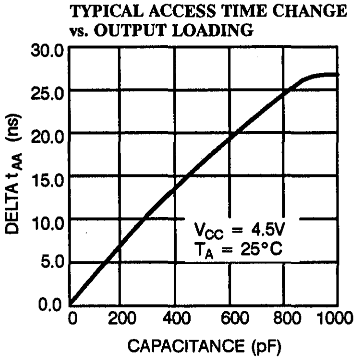


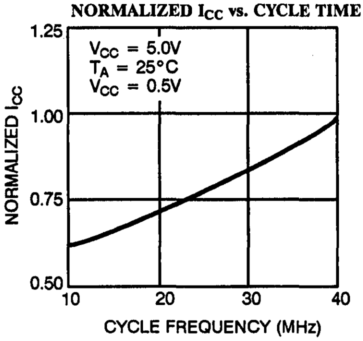




Typical DC and AC Characteristics (continued)







Truth Table

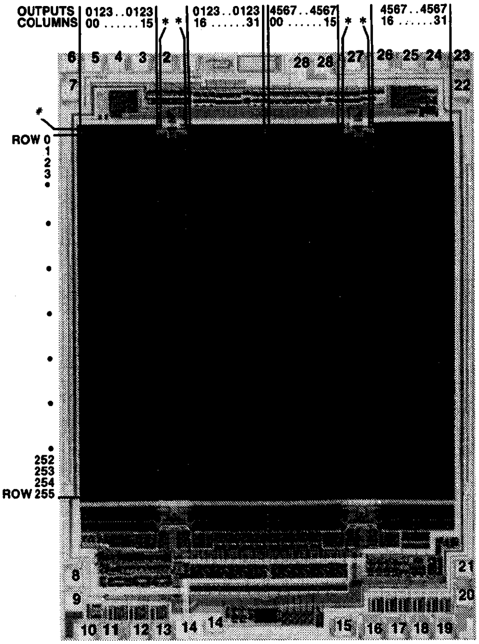
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	L	X	X	High Z	Deselect
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C185A–20PC	P21	Commercial
	CY7C185A–20VC	V21	
	CY7C185A–20DC	D22	
	CY7C185A–20LC	L54	
	CY7C185A–20DMB	D22	Military
	CY7C185A–20LMB	L54	
	CY7C185A–20KMB	K74	
25	CY7C185A–25PC	P21	Commercial
	CY7C185A–25VC	V21	
	CY7C185A–25DC	D22	
	CY7C185A–25LC	L54	
	CY7C185A–25DMB	D22	Military
	CY7C185A–25LMB	L54	
	CY7C185A–25KMB	K74	
35	CY7C185A–35PC	P21	Commercial
	CY7C185A–35VC	V21	
	CY7C185A–35DC	D22	
	CY7C185A–35LC	L54	
	CY7C185A–35DMB	D22	Military
	CY7C185A–35LMB	L54	
	CY7C185A–35KMB	K74	
45	CY7C185A–45PC	P21	Commercial
	CY7C185A–45VC	V21	
	CY7C185A–45DC	D22	
	CY7C185A–45LC	L54	
	CY7C185A–45DMB	D22	Military
	CY7C185A–45LMB	L54	
	CY7C185A–45KMB	K74	
55	CY7C185A–55PC	P21	Commercial
	CY7C185A–55VC	V21	
	CY7C185A–55DC	D22	
	CY7C185A–55LC	L54	
	CY7C185A–55DMB	D22	Military
	CY7C185A–55LMB	L54	
	CY7C185A–55KMB	K74	

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C186A–20PC	P15	Commercial
	CY7C186A–20DC	D16	
	CY7C186A–20DMB	P15	Military
25	CY7C186A–25PC	P15	Commercial
	CY7C186A–25DC	D16	
	CY7C186A–25DMB	D16	Military
35	CY7C186A–35PC	P15	Commercial
	CY7C186A–35DC	D16	
	CY7C186A–35DMB	D16	Military
45	CY7C186A–45PC	P15	Commercial
	CY7C186A–45DC	D16	
	CY7C186A–45DMB	D16	Military
55	CY7C186A–55PC	P15	Commercial
	CY7C186A–55DC	D16	
	CY7C186A–55DMB	D16	Military

Bit Map



Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE1}	7, 8, 9, 10, 11
t_{ACE2}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE1}	7, 8, 9, 10, 11
t_{SCE2}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00114

CY7C187

CYPRESS SEMICONDUCTOR

65,536 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **15 ns**
- **Low active power**
  - **495 mW**
- **Low standby power**
  - **220 mW**
- **TTL compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C187 is a high-performance CMOS static RAM organized as 65,536 words x 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C187 has an automatic power-down feature, reducing the power consumption by 56% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{15}).

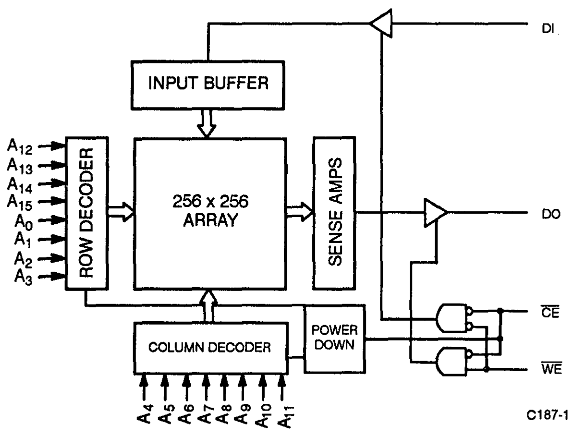
Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The 7C187 utilizes a die coat to insure alpha immunity.

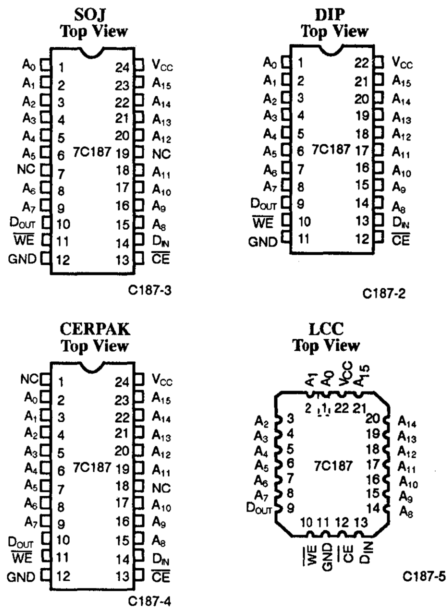
2

Logic Block Diagram



C187-1

Pin Configurations



Selection Guide

	7C18715	7C187-20	7C187-25	7C187-35	7C187-45
Maximum Access Time (ns)	15	20	25	35	45
Maximum Operating Current (mA)	90	80	70	70	50
Maximum Standby Current (mA)	40/20	20/20	20/20	20/20	20/20

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... $-65°C$ to $+150°C$

Ambient Temperature with Power Applied .... $-55°C$ to $+125°C$

Supply Voltage to Ground Potential (Pin 22 to Pin 11) .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs in High Z State .... $-0.5V$ to $+7.0V$

DC Input Voltage .... $-3.0V$ to $+7.0V$

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	7C187-15		7C187-20		7C187-25,35		7C187-45		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA	2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		-3.0	0.8	-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	$GND \leq V_I \leq V_{CC}$	-10	+10	-10	+10	-10	+10	-10	+10	µA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-10	+10	-10	+10	-10	+10	-10	+10	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND		-350		-350		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA		90		80		70		50	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[3]	Max. V_{CC}, $\overline{CE} \geq V_{IH}$		40		40		20		20	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		20		20		20		20	mA

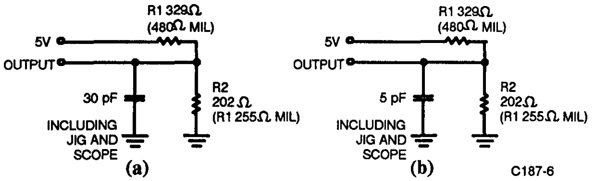
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

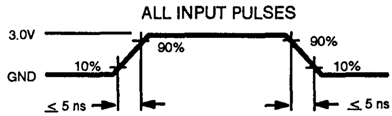
Notes:

1. V_{IL} min. = −3.0V for pulse durations less than 30 ns.
2. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

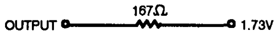


C187-6

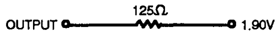


C187-7

Equivalent to: THÉVENIN EQUIVALENT



Military



Commercial

Switching Characteristics Over the Operating Range [5]

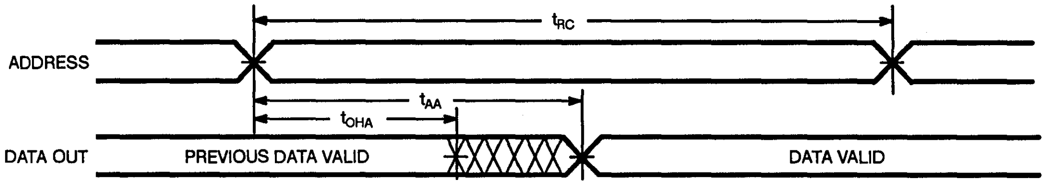
Parameters	Description	7C187-15		7C187-20		7C187-25		7C187-35		7C187-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		5		5		5		5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		5		5		5		5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [7, 8]		8		8		10		15		15	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		15		20		20		20		25	ns
WRITE CYCLE[8]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [8]	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [8, 9]		7		7		7		10		15	ns

Notes:

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
7. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

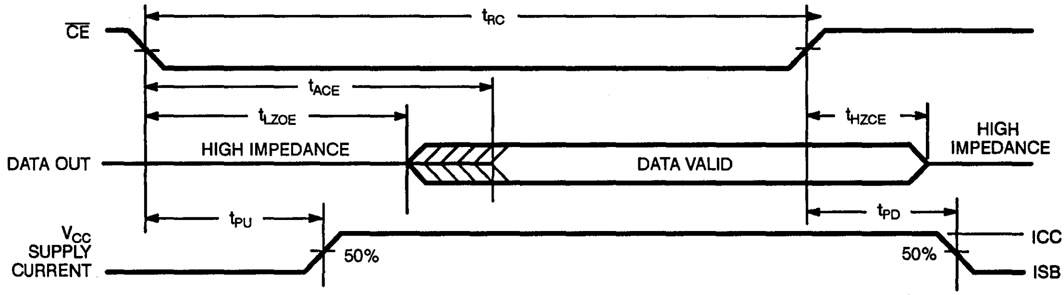
Switching Waveforms

Read Cycle No. 1[9, 10]



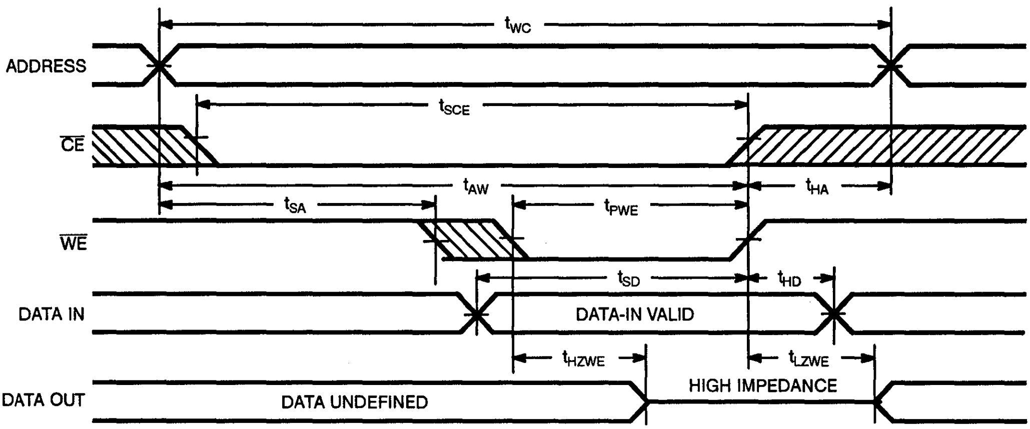
C187-8

Read Cycle No. 2[9, 11]



C187-9

Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



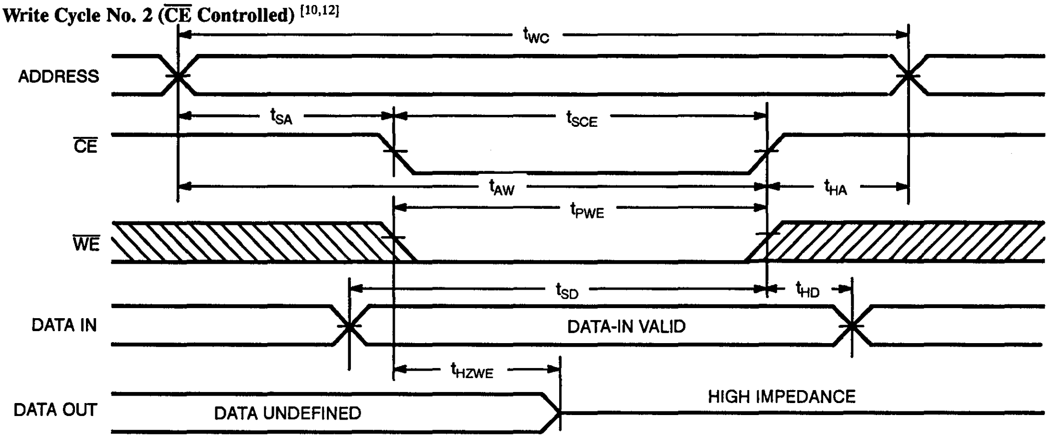
C187-10

Notes:

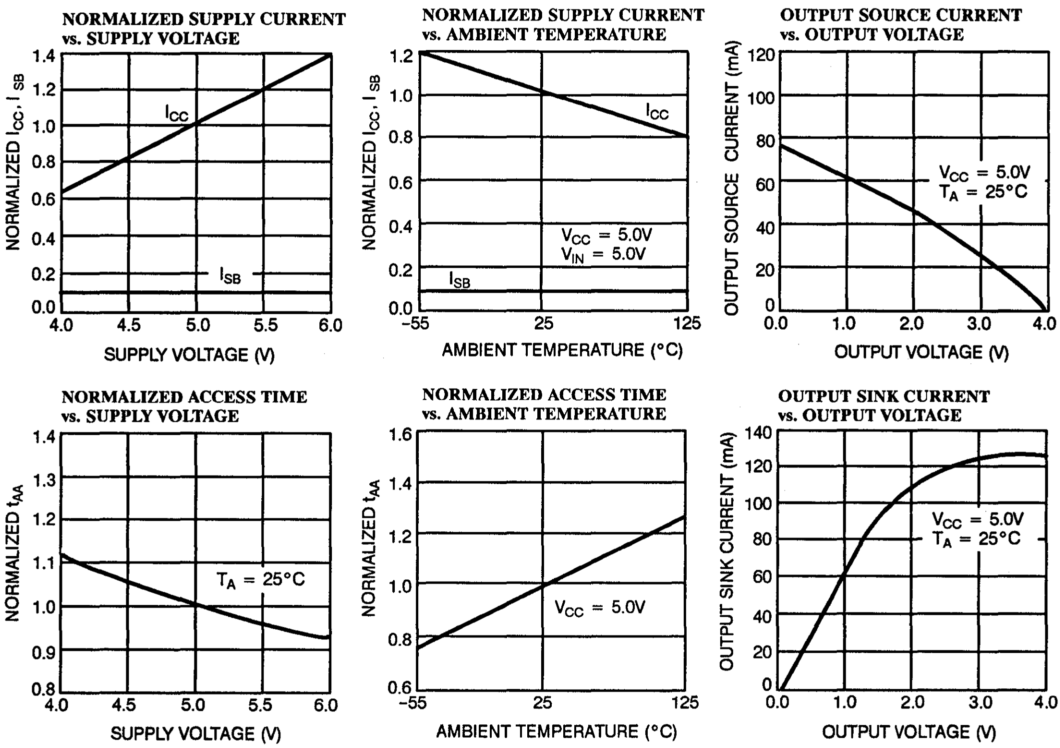
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) [10,12]

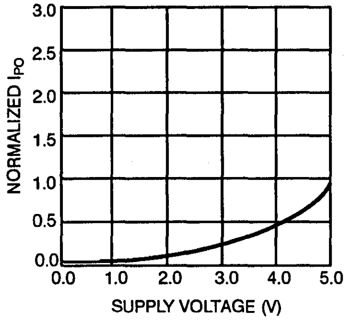


Typical DC and AC Characteristics

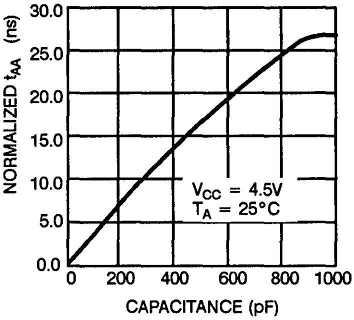


Typical DC and AC Characteristics (continued)

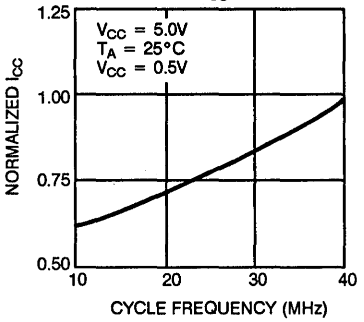
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



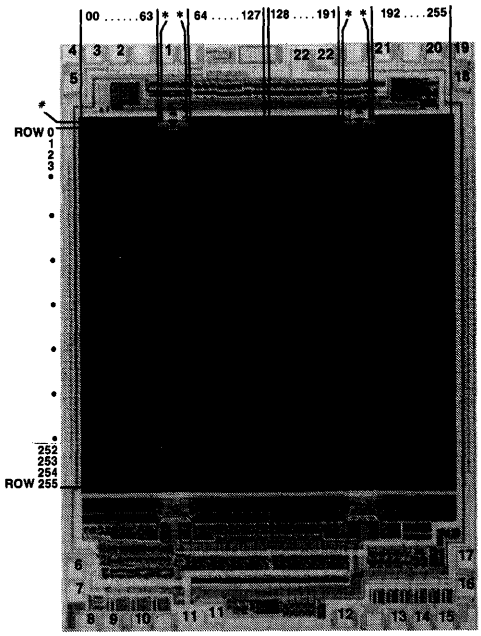
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Bit Map



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C187-15PC	P9	Commercial
	CY7C187-15VC	V13	
	CY7C187-15DC	D10	
	CY7C187-15LC	L52	
20	CY7C187-20PC	P9	Commercial
	CY7C187-20VC	V13	
	CY7C187-20DC	D10	
	CY7C187-20LC	L52	
25	CY7C187-25PC	P9	Commercial
	CY7C187-25VC	V13	
	CY7C187-25DC	D10	
	CY7C187-25LC	L52	
35	CY7C187-35PC	P9	Commercial
	CY7C187-35VC	V13	
	CY7C187-35DC	D10	
	CY7C187-35LC	L52	
45	CY7C187-45PC	P9	Commercial
	CY7C187-45VC	V13	
	CY7C187-45DC	D10	
	CY7C187-45LC	L52	

Document #: 38-00038-G

65,536 x 1 Static R/W RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  - **15 ns**
- **Low active power**
  - **440 mW**
- **Low standby power**
  - **220 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C187A is a high-performance CMOS static RAM organized as 65,536 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C187A has an automatic power-down feature, reducing the power consumption by 50% when deselected.

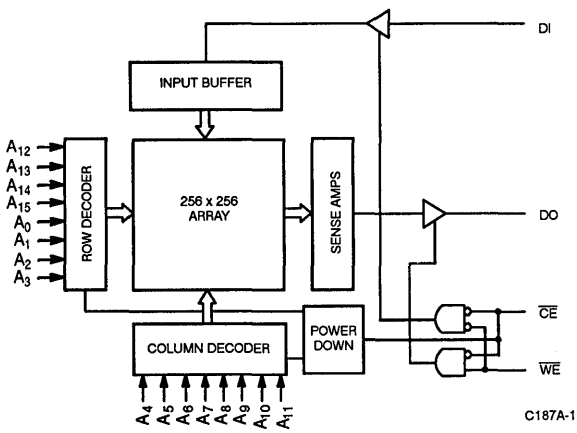
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (DI) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the data output (DO) pin.

The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

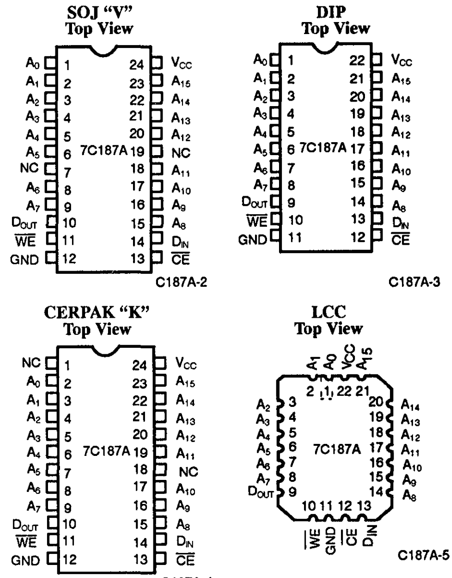
The 7C187A utilizes a die coat to insure alpha immunity.

Logic Block Diagram



C187A-1

Pin Configurations



C187A-2

C187A-3

C187A-4

C187A-5

Selection Guide

		7C187A-15	7C187A-20	7C187A-25	7C187A-35	7C187A-45
Maximum Access Time (ns)		15	20	25	35	45
Maximum Operating Current (mA)	Commercial	90	80	80	80	80
	Military		90	80	80	80
Maximum Standby Current (mA)	Commercial	40/20	40/20	30/20	30/20	30/20
	Military		40/20	40/20	30/20	30/20

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... – 65°C to + 150°C

Ambient Temperature with
Power Applied .... – 55°C to + 125°C

Supply Voltage to Ground Potential
(Pin 22 to Pin 11) .... – 0.5V to + 7.0V

DC Voltage Applied to Outputs
in High Z State .... – 0.5V to + 7.0V

DC Input Voltage .... – 3.0V to + 7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... > 2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	– 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions			7C187A-15 Min.	7C187A-15 Max.	7C187A-20 Min.	7C187A-20 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 8.0 mA	Com'l		0.4		0.4	V
			I_{OL} = 12.0 mA	Mil		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]				-3.0	0.8	-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$			-10	+10	-10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled			-10	+10	-10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA		Com'l		90		80	mA
				Mil				90	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[5]	Max. V_{CC}, $\overline{CE} \geq V_{IH}$		Com'l		40		40	mA
				Mil				40	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[5]	Max. V_{CC}, $\overline{CE} \geq V_{CC}$ - 0.3V, $V_{IN} \geq V_{CC}$ - 0.3V or $V_{IN} \leq$ 0.3V		Com'l		20		20	mA
				Mil				20	

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. V_{IL} min. = -3.0V for pulse durations less than 30 ns.
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
6. Tested initially and after any design or process changes that may affect these parameters.
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.

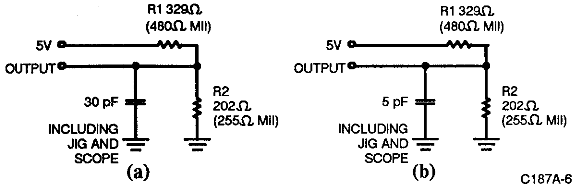
Electrical Characteristics Over the Operating Range[2] (continued)

Parameters	Description	Test Conditions			7C187A-25 Min.	7C187A-25 Max.	7C187A-35, 45 Min.	7C187A-35, 45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA			2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 8.0 mA	Com'l		0.4		0.4	V
			I_{OL} = 12.0 mA	Mil		0.4		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[3]				−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$			−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled			−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = GND				−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA		Com'l		80		80	mA
				Mil		80		80	
I_{SB1}	Automatic $\overline{CE}$ Power Down Current[5]	Max. V_{CC}, $\overline{CE} \geq V_{IH}$		Com'l		30		30	mA
				Mil		40		30	
I_{SB2}	Automatic $\overline{CE}$ Power Down Current[5]	Max. V_{CC}, $\overline{CE} \geq V_{CC}$ − 0.3V, $V_{IN} \geq V_{CC}$ − 0.3V or $V_{IN} \leq$ 0.3V		Com'l		20		20	mA
				Mil		20		20	

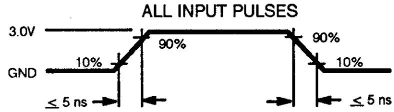
Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms

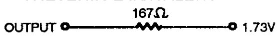


C187A-6

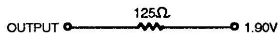


C187A-7

Equivalent to: THÉVENIN EQUIVALENT



Military



Commercial

Switching Characteristics Over the Operating Range[2, 7]

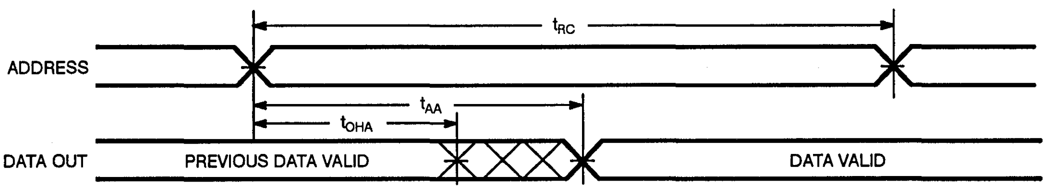
Parameters	Description	7C187A-15		7C187A-20		7C187A-25		7C187A-35		7C187A-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		45		ns
t_{AA}	Address to Data Valid		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{\text{CE}}$ LOW to Data Valid		15		20		25		35		45	ns
t_{LZCE}	$\overline{\text{CE}}$ LOW to Low Z[8]	5		5		5		5		5		ns
t_{HZCE}	$\overline{\text{CE}}$ HIGH to High Z[8, 9]		8		8		10		15		15	ns
t_{PU}	$\overline{\text{CE}}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{\text{CE}}$ HIGH to Power-Down		15		20		20		20		25	ns
WRITE CYCLE[10]												
t_{WC}	Write Cycle Time	15		20		20		25		40		ns
t_{SCE}	$\overline{\text{CE}}$ LOW to Write End	12		15		20		25		30		ns
t_{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	$\overline{\text{WE}}$ Pulse Width	12		15		15		20		20		ns
t_{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z[8]	5		5		5		5		5		ns
t_{HZWE}	$\overline{\text{WE}}$ LOW to High Z[8, 9]		7		7		7		10		15	ns

Notes:

8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
9. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. $\overline{\text{WE}}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{\text{CE}} = V_{IL}$.
13. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
14. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

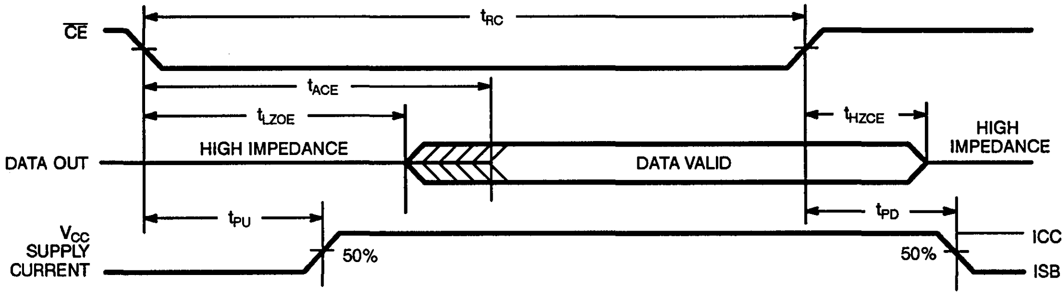
Read Cycle No. 1[11, 12]



C187A-8

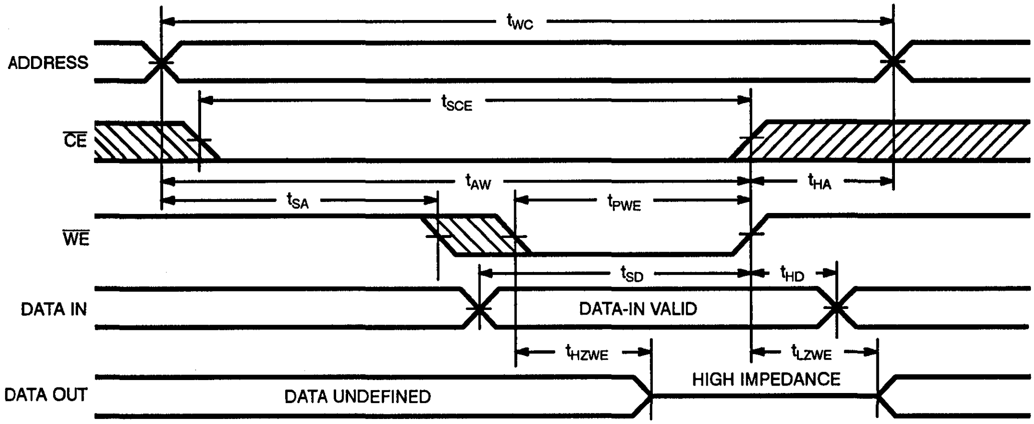
Switching Waveforms

Read Cycle No. 2[11, 13]



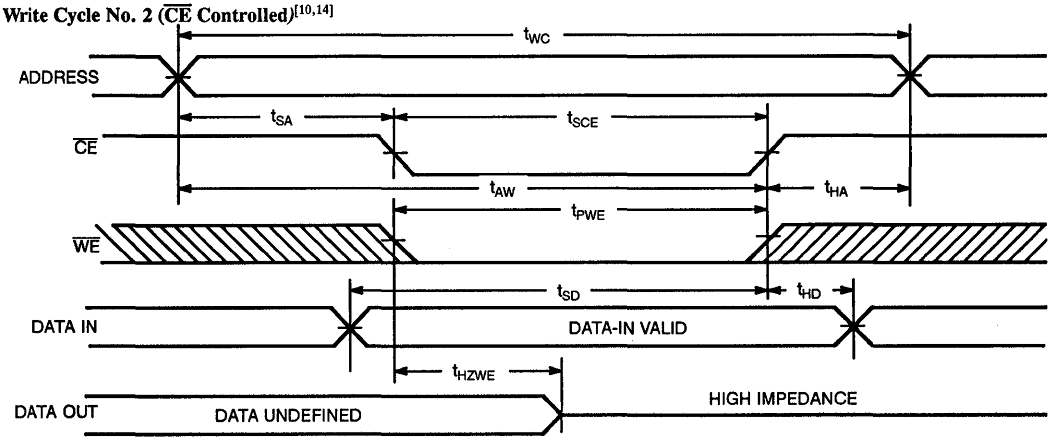
C187A-9

Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



C187A-10

Write Cycle No. 2 ($\overline{CE}$ Controlled)[10,14]

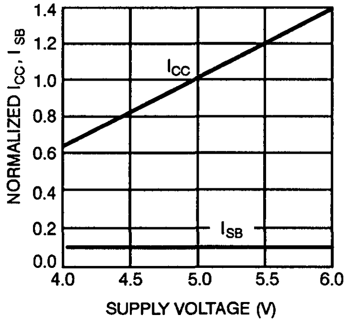


C187-11

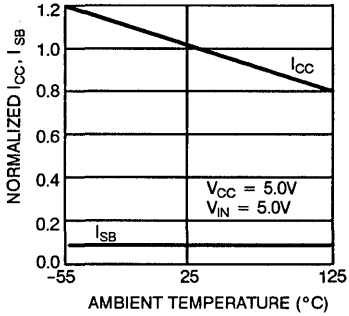
2

Typical DC and AC Characteristics

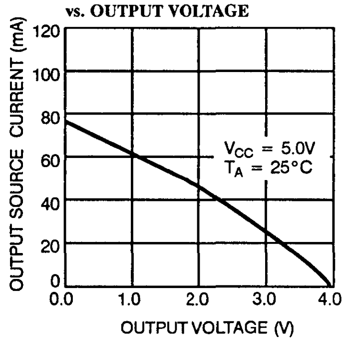
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



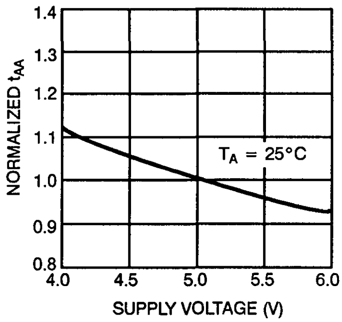
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



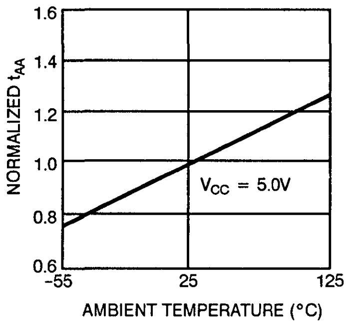
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



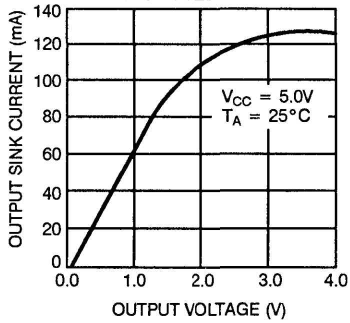
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



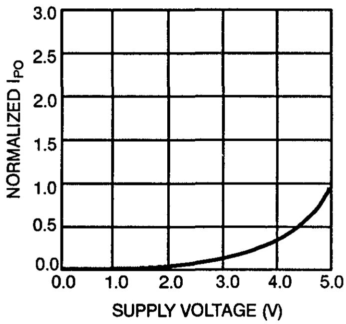
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



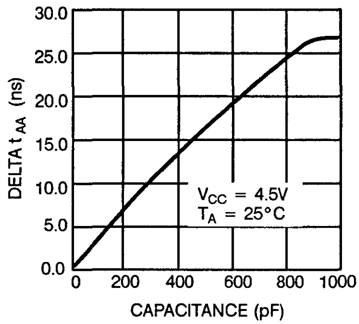
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



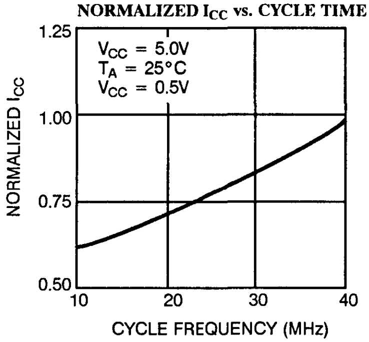
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



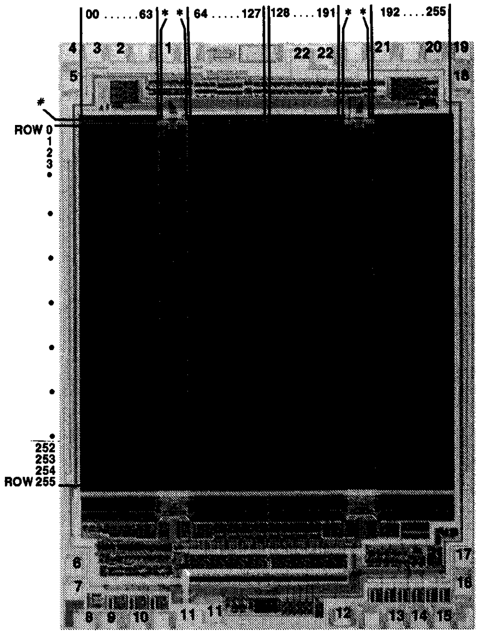
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Bit Map



Address Designators

Address Name	Address Function	Pin Number
A0	X3	1
A1	X4	2
A2	X5	3
A3	X6	4
A4	X7	5
A5	Y7	6
A6	Y6	7
A7	Y2	8
A8	Y3	14
A9	Y1	15
A10	Y0	16
A11	Y4	17
A12	Y5	18
A13	X0	19
A14	X1	20
A15	X2	21

Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C187A-15PC	P9	Commercial
	CY7C187A-15VC	V13	
	CY7C187A-15DC	D10	
	CY7C187A-15LC	L52	
20	CY7C187A-20PC	P9	Commercial
	CY7C187A-20VC	V13	
	CY7C187A-20DC	D10	
	CY7C187A-20LC	L52	
	CY7C187A-20DMB	D10	Military
	CY7C187A-20LMB	L52	
	CY7C187A-20KMB	K73	
25	CY7C187A-25PC	P9	Commercial
	CY7C187A-25VC	V13	
	CY7C187A-25DC	D10	
	CY7C187A-25LC	L52	
	CY7C187A-25DMB	D10	Military
	CY7C187A-25LMB	L52	
	CY7C187A-25KMB	K73	
35	CY7C187A-35PC	P9	Commercial
	CY7C187A-35VC	V13	
	CY7C187A-35DC	D10	
	CY7C187A-35LC	L52	
	CY7C187A-35DMB	D10	Military
	CY7C187A-35LMB	L52	
	CY7C187A-35KMB	K73	
45	CY7C187A-45PC	P9	Commercial
	CY7C187A-45VC	V13	
	CY7C187A-45DC	D10	
	CY7C187A-45LC	L52	
	CY7C187A-45DMB	D10	Military
	CY7C187A-45LMB	L52	
	CY7C187A-45KMB	K73	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00115

CY7C189
CY7C190

CYPRESS SEMICONDUCTOR

16 x 4 Static R/W RAM

Features

- Fully decoded, 16 word x 4-bit high-speed CMOS RAMs
- Inverting outputs CY7C189
- Non-inverting outputs CY7C190
- High speed
  - 15 ns and 25 ns (commercial)
  - 25 ns (military)
- Low power
  - 303 mW at 25 ns
  - 495 mW at 15 ns
- Power supply 5V ± 10%
- Advanced high-speed CMOS processing for optimum speed/power product
- Capable of withstanding greater than 2001V static discharge
- Three-state outputs
- TTL-compatible interface levels

Functional Description

The CY7C189 and CY7C190 are extremely high performance 64-bit static RAMs organized as 16 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The devices are provided with inverting (CY7C189) and non-inverting (CY7C190) outputs.

Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four data inputs (D_0 through D_3) is written into the memory location specified on the address pins (A_0 through A_3). The outputs are preconditioned such that the correct data is present at the data outputs (O_0 through O_3) when the write cycle is complete. This precondition operation insures minimum write recovery times by eliminating the "write recovery glitch."

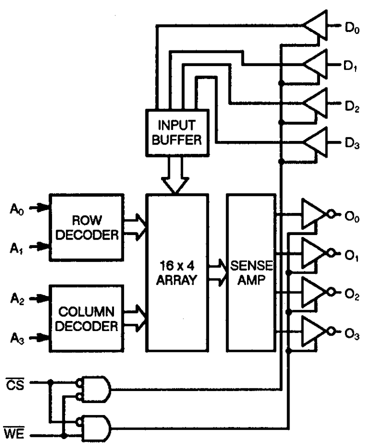
Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3) in inverted (CY7C189) or non-inverted (CY7C190) format.

The four output pins remain in high-impedance state when chip select ($\overline{CS}$) is HIGH or write enable ($\overline{WE}$) is LOW.

2

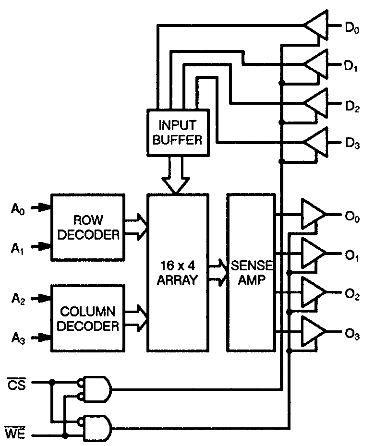
Logic Block Diagram

CY7C189



C189-1

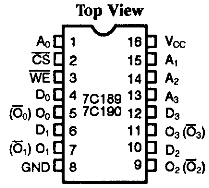
CY7C190



C189-2

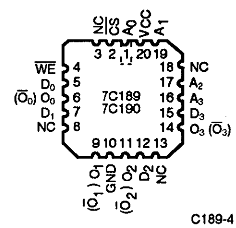
Pin Configurations

DIP
Top View



C189-3

LCC
Top View



C189-4

Selection Guide

		7C189-15 7C190-15	7C189-25 7C190-25
Maximum Access Time (ns)	Commercial	15	25
	Military		25
Maximum Operating Current (mA)	Commercial	90	55
	Military		70

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... $-65°C$ to $+150°C$

Ambient Temperature with Power Applied .... $-55°C$ to $+125°C$

Supply Voltage to Ground Potential (Pin 16 to Pin 8) .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs in High Z State .... $-0.5V$ to $+7.0V$

DC Input Voltage .... $-3.0V$ to $+7.0V$

Output Current, into Outputs (Low) .... 10 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range [2]

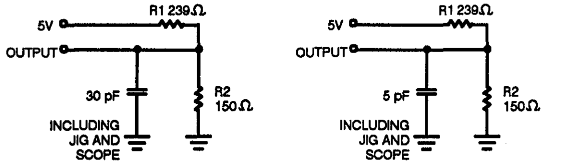
Parameters	Description	Test Conditions		7C189-15 7C190-15 Min.	7C189-15 7C190-15 Max.	7C189-25 7C190-25 Min.	7C189-25 7C190-25 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.45			V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			− 3.0	0.8	− 3.0	0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		− 10	+ 10	− 10	+ 10	μA
V_{CD}	Input Diode Clamp Voltage			Note 3		Note 3		
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$		− 40	+ 40	− 40	+ 40	μA
I_{OS}	Output Short Circuit Current [4]	V_{CC} = Max., V_{OUT} = GND			− 90		− 90	mA
I_{OS}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90		55	mA
			Mil				70	mA

Capacitance[5]

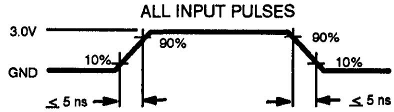
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The CMOS process does not provide a clamp diode. However these devices are insensitive to − 3V DC input levels and − 5V undershoot pulses of less than 5 ns (measured at 50% points).
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

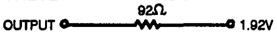


(a) (b) C189-5



C189-6

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2,6]

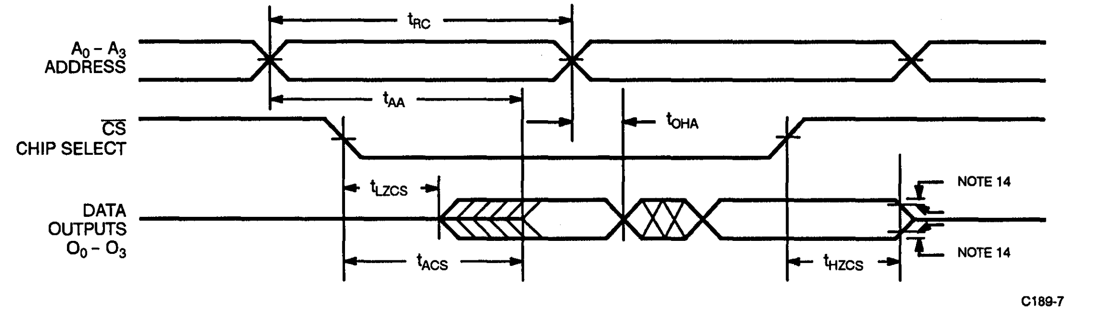
Parameters	Description	7C189-15 7C190-15		7C189-25 7C190-25		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	15		25		ns
t_{AA}	Address to Data Valid[7]		15		25	ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid[7]		12		15	ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[8, 9]		12		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z		12		15	ns
t_{OHA}	Data Hold from Address Change	5		5		
WRITE CYCLE[10, 11]						
t_{WC}	Write Cycle Time	15		20		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		12		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z		12		20	ns
t_{AWE}	$\overline{WE}$ HIGH to Data Valid[7]		12		20	ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		ns
t_{SD}	Data Set-Up to Write End	15		20		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{HA}	Address Hold from Write End	0		0		ns

Notes:

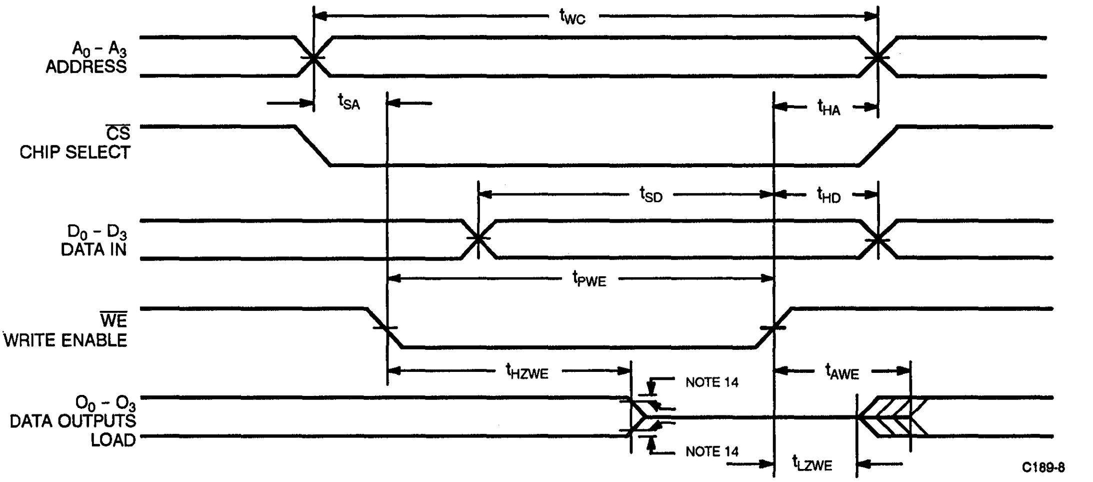
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the spcified I_{OL}/I_{OH}, and 30-pF load capacitance.
7. t_{AA}, t_{ACS}, and t_{AWE} are tested with C_L = 30 pF as in part (a) of AC Test Loads. Timing is referenced to 1.5V on the inputs and outputs.
8. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input.
9. t_{HZCS} and t_{HZWE} are tested with C_L = 5 pF as in part (b) of AC Test Loads.
10. Output is preconditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
11. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate the write.

Switching Waveforms

Read Cycle



Write Cycle [12, 13]

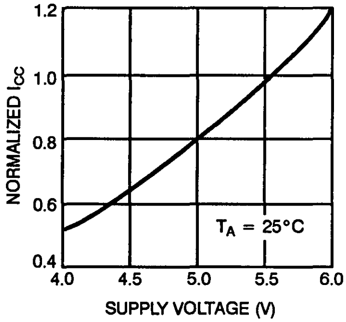


Notes:

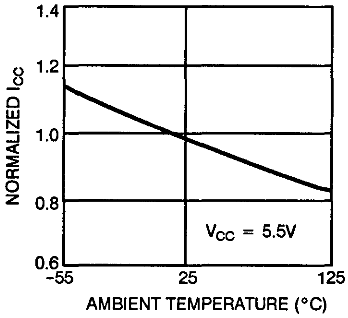
12. All measurements referenced to 1.5V.
13. Timing diagram represents one solution which results in optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violated.
14. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from 1.5V level on the input.

Typical DC and AC Characteristics

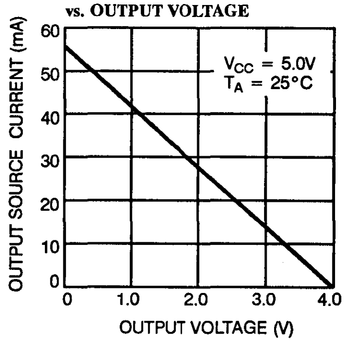
NORMALIZED I_{CC} vs. SUPPLY VOLTAGE



NORMALIZED I_{CC} vs. AMBIENT TEMPERATURE

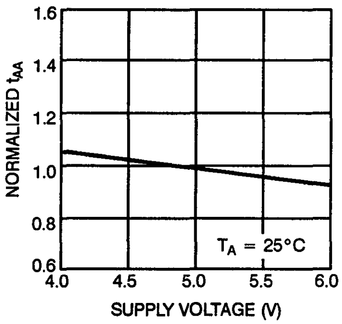


OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

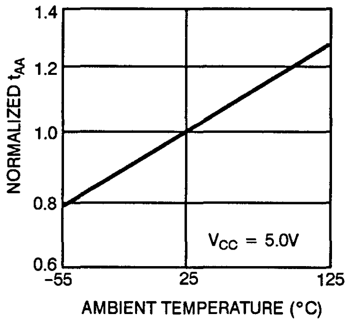


2

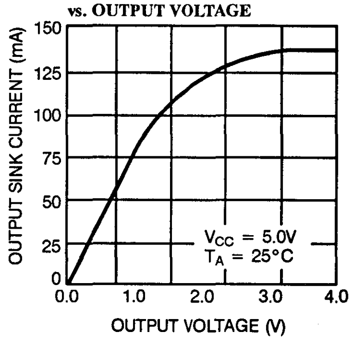
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



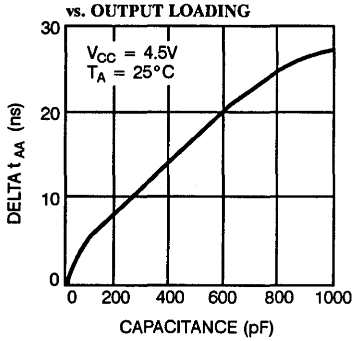
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



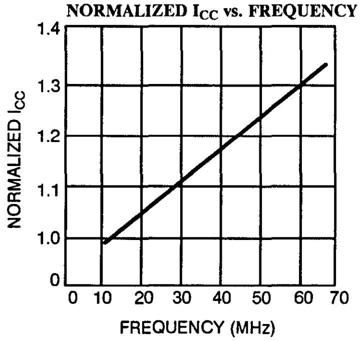
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



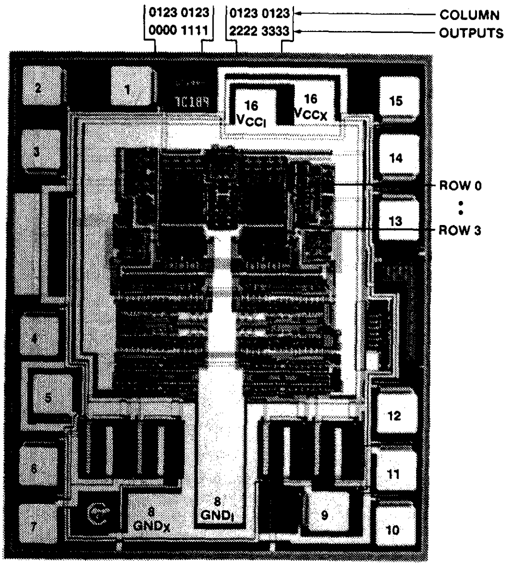
ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



Bit Map



Address Designators

Address Name	Address Function	Pin Number
A_0	AXO	1
A_1	AX1	15
A_2	AY0	14
A_3	AY1	13

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C189-15PC	P1	Commercial
	CY7C189-15DC	D2	
	CY7C189-15LC	L61	
25	CY7C189-25PC	P1	Commercial
	CY7C189-25DC	D2	
	CY7C189-25LC	L61	
	CY7C189-25DMB	D2	Military
	CY7C189-25LMB	L61	

Speed (ns)	Ordering Code	Package Type	Operating Range
15	CY7C190-15PC	P1	Commercial
	CY7C190-15DC	D2	
	CY7C190-15LC	L61	
25	CY7C190-25PC	P1	Commercial
	CY7C190-25DC	D2	
	CY7C190-25LC	L61	
	CY7C190-25DMB	D2	Military
	CY7C190-25LMB	L61	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{AWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11

Document #: 38-00039-B

CY7C191
CY7C192

CYPRESS SEMICONDUCTOR

65,536 x 4 Static R/W RAM Separate I/O

Features

- **Automatic power-down when deselected**
- **Transparent write (7C191)**
- **CMOS for optimum speed/power**
- **High speed**
  - **25 ns t_{AA}**
- **Low active power**
  - **660 mW**
- **Low standby power**
  - **193 mW**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY7C191 and CY7C192 are high-performance CMOS static RAMs organized as 65,536 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 71% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW.

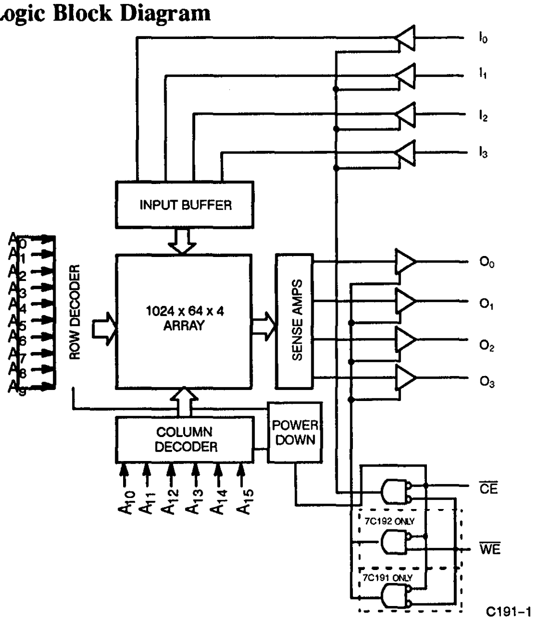
Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while the write enable ($\overline{WE}$) reamins HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C192 only), or chip enable ($\overline{CE}$) is HIGH.

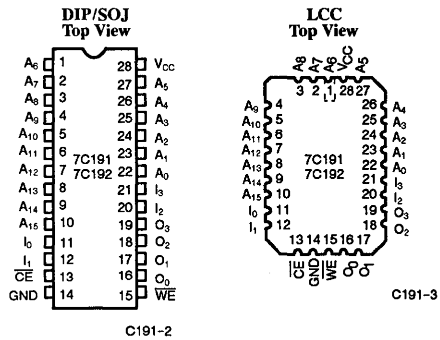
A die coat is used to insure alpha immunity.

Logic Block Diagram



C191-1

Pin Configurations



Selection Guide

		7C191-25 7C192-25	7C191-35 7C192-35	7C191-45 7C192-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	120	120	120
	Military	130	130	130
Maximum Standby Current (mA)		35	35	35

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... $-65°C$ to $+150°C$

Ambient Temperature with Power Applied .... $-55°C$ to $+125°C$

Supply Voltage to Ground Potential (Pin 28 to Pin 14) .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs in High Z State .... $-0.5V$ to $+7.0V$

DC Input Voltage .... $-3.0V$ to $+7.0V$

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C191-25, 35, 45 7C192-25, 35, 45 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			-3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		-10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		-10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		120	mA
			Mil		130	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%			35	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V			20	mA

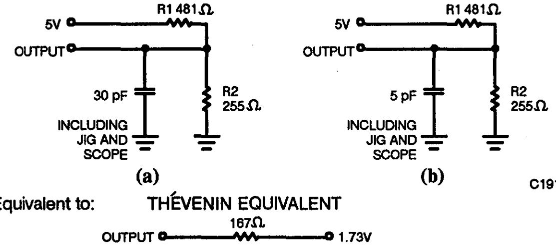
Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

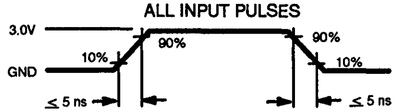
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



C191-4



C191-5

Switching Characteristics Over the Operating Range[2,5]

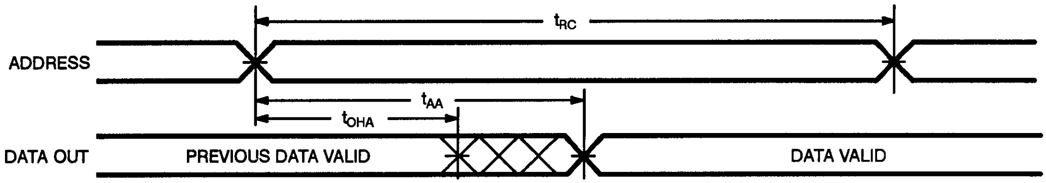
Parameters	Description	7C191-25 7C192-25 Min.	7C191-25 7C192-25 Max.	7C191-35 7C192-35 Min.	7C191-35 7C192-35 Max.	7C191-45 7C192-45 Min.	7C191-45 7C192-45 Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		13		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE[8]								
t_{WC}	Write Cycle Time	20		30		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		40		ns
t_{AW}	Address Set-Up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		17		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z (7C192)[7]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z (7C192[6, 7]		13		15		20	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C191)		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C191)		20		30		35	ns

Notes:

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device. These parameters are guaranteed and not 100% tested.
7. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE} = V_{IL}$. (7C166: $\overline{OE} = V_{IL}$ also).
11. Address valid prior to or coincident with $\overline{CE}$ transition low.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C192 only).

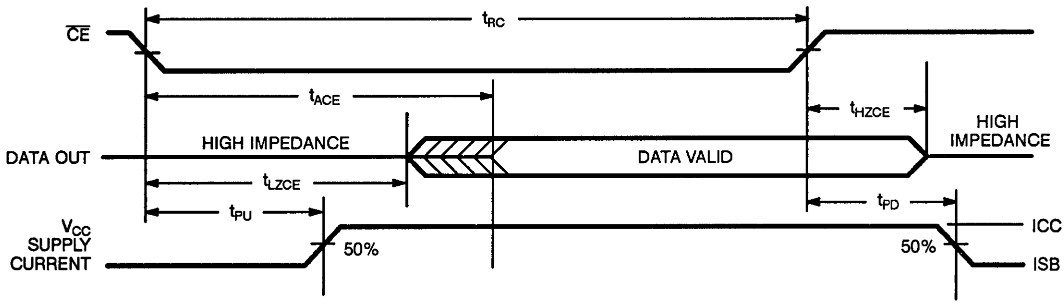
Switching Waveforms

Read Cycle No. 1[9, 10]



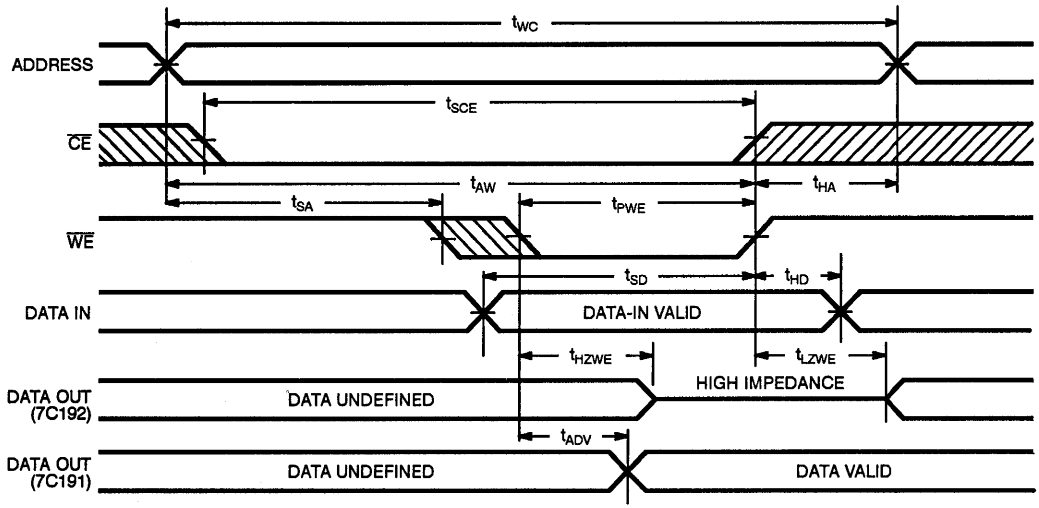
C191–6

Read Cycle No. 2[9, 11]



C191–7

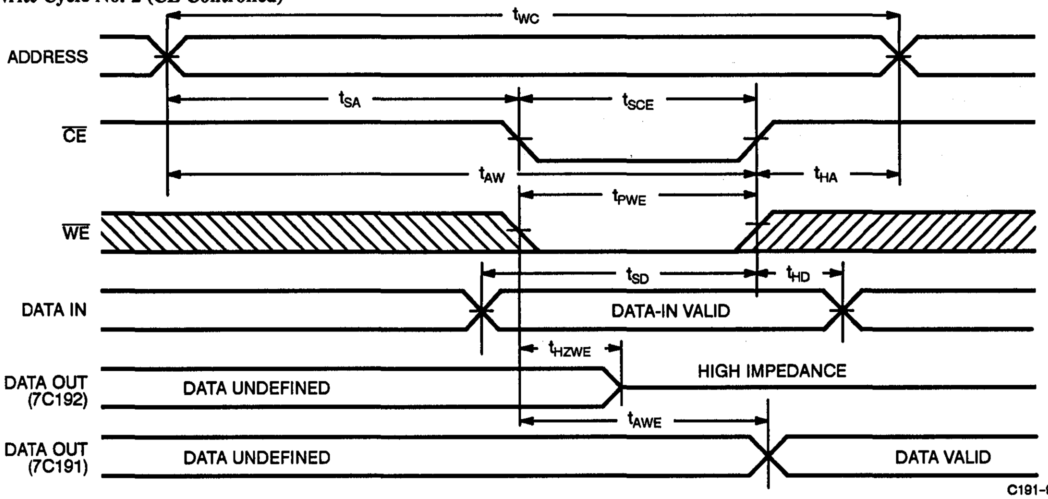
Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]



C191–8

Switching Waveforms (continued)

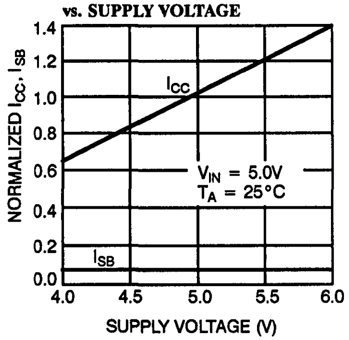
Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 12]



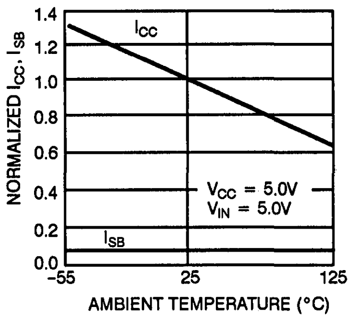
C191-9

Typical DC and AC Characteristics

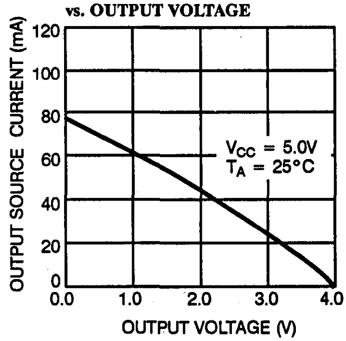
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



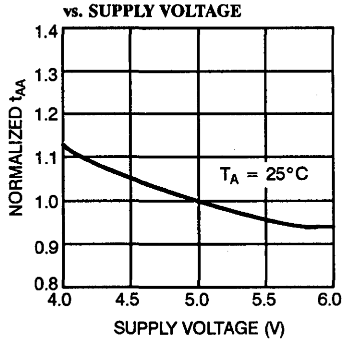
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



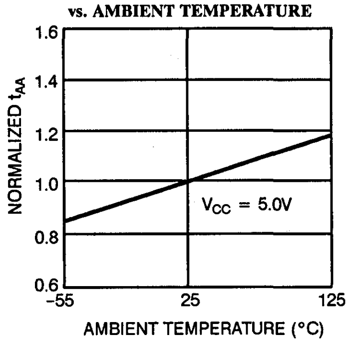
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



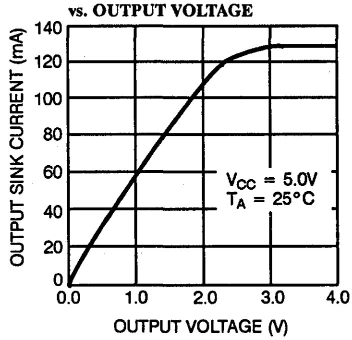
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

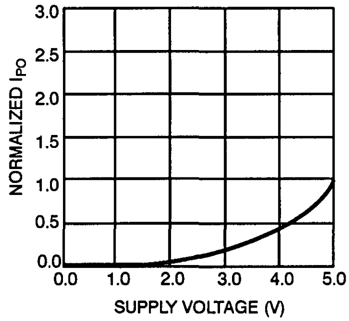


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

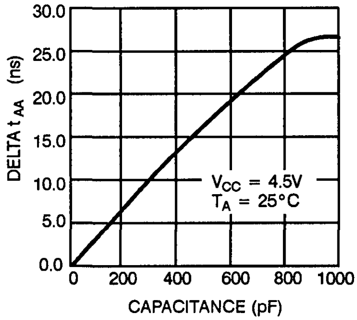


Typical DC and AC Characteristics (continued)

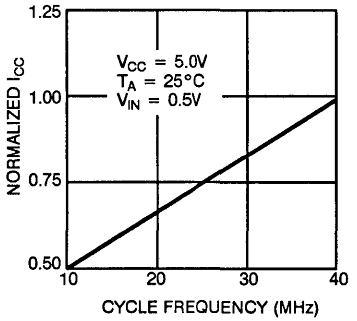
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C191-25PC	P21	Commercial
	CY7C191-25VC	V21	
	CY7C191-25DC	D22	
	CY7C191-25LC	L54	
	CY7C191-25DMB	D22	Military
	CY7C191-25LMB	L54	
	CY7C191-25KMB	K74	
35	CY7C191-35PC	P21	Commercial
	CY7C191-35VC	V21	
	CY7C191-35DC	D22	
	CY7C191-35LC	L54	
	CY7C191-35DMB	D22	Military
	CY7C191-35LMB	L54	
	CY7C191-35KMB	K74	
45	CY7C191-45PC	P21	Commercial
	CY7C191-45VC	V21	
	CY7C191-45DC	D22	
	CY7C191-45LC	L54	
	CY7C191-45DMB	D22	Military
	CY7C191-45LMB	L54	
	CY7C191-45KMB	K74	

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C192-25PC	P21	Commercial
	CY7C192-25VC	V21	
	CY7C192-25DC	D22	
	CY7C192-25LC	L54	
	CY7C192-35DMB	D22	Military
	CY7C192-35LMB	L54	
	CY7C192-35KMB	K74	
35	CY7C192-35PC	P21	Commercial
	CY7C192-35VC	V21	
	CY7C192-35DC	D22	
	CY7C192-35LC	L54	
	CY7C192-35DMB	D22	Military
	CY7C192-35LMB	L54	
	CY7C192-35KMB	K74	
45	CY7C192-45PC	P21	Commercial
	CY7C192-45VC	V21	
	CY7C192-45DC	D22	
	CY7C192-45LC	L54	
	CY7C192-45DMB	D22	Military
	CY7C192-45LMB	L54	
	CY7C192-45KMB	K74	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[13]	7, 8, 9, 10, 11
t_{AVE}[13]	7, 8, 9, 10, 11

Note:
13. 7C191 only

Document #: 38-00076-E

CYPRESS SEMICONDUCTOR

65,536 x 4 Static R/W RAM

Features

- Automatic power-down when deselected
- Output Enable ($\overline{OE}$) feature (7C196)
- CMOS for optimum speed/power
- High speed
  - 25 ns t_{AA}
- Low active power
  - 660 mW
- Low standby power
  - 193 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C194 and CY7C196 are high-performance CMOS static RAMs organized as 65,536 by 4 bits. Easy memory expansion is provided by active LOW chip enable(s) ($\overline{CE}$ on the CY7C194, $\overline{CE}_1$, $\overline{CE}_2$ on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 71% when deselected.

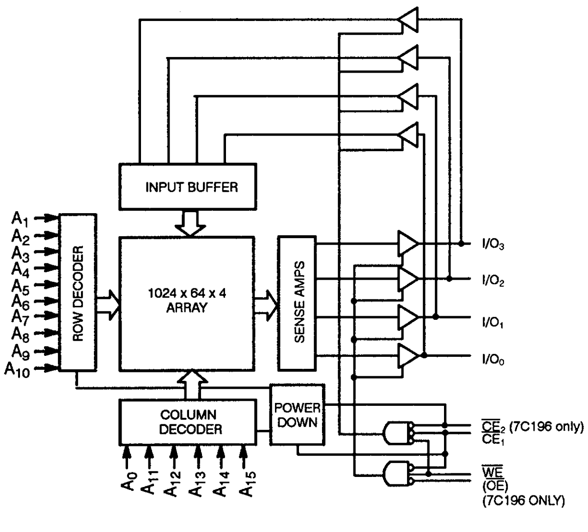
Writing to the device is accomplished when the chip enable(s) ($\overline{CE}$ on the CY7C194, $\overline{CE}_1$, $\overline{CE}_2$ on the CY7C196) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I/O_0 through I/O_3) is written into the memory location, specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable(s) ($\overline{CE}$ on the CY7C194, $\overline{CE}_1$, $\overline{CE}_2$ on the CY7C196) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

A die coat is used to ensure alpha immunity.

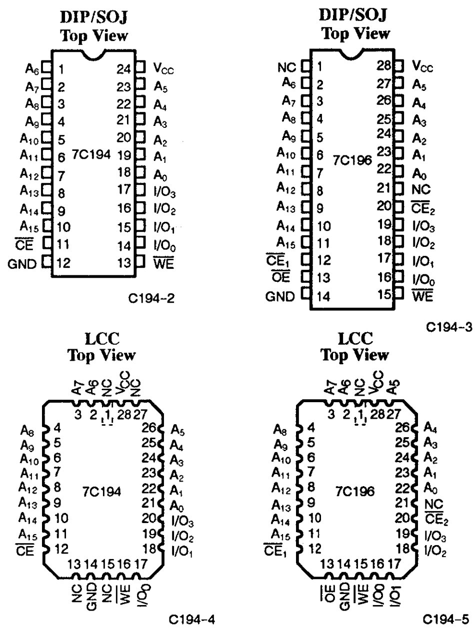
2

Logic Block Diagram



C194-1

Pin Configurations



Selection Guide

		7C194-25 7C196-25	7C194-35 7C196-35	7C194-45 7C196-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	120	120	120
	Military	130	130	130
Maximum Standby Current (mA)		35	35	35

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... $-65°C$ to $+150°C$

Ambient Temperature with Power Applied .... $-55°C$ to $+125°C$

Supply Voltage to Ground Potential .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs in High Z State .... $-0.5V$ to $+7.0V$

DC Input Voltage .... $-3.0V$ to $+7.0V$

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

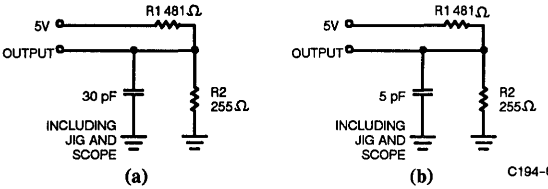
Parameters	Description	Test Conditions		7C194-25, 35, 45 7C196-25, 35, 45 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			-3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-10	+10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		-10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		120	mA
			Mil		130	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%			35	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$			20	mA

Capacitance[5]

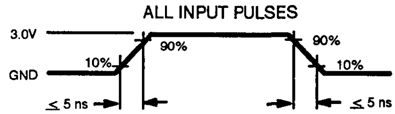
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



C194-6



C194-7

Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[2,6]

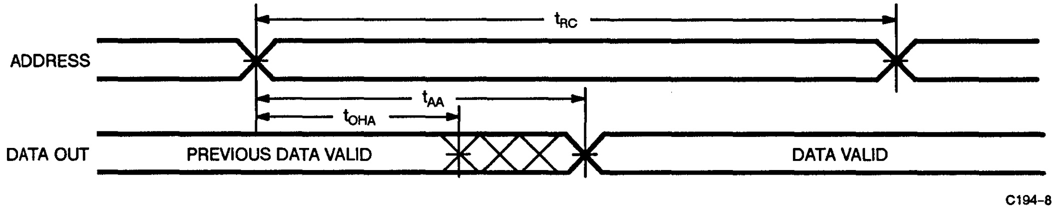
Parameters	Description	7C194-25 7C196-25 Min.	7C194-25 7C196-25 Max.	7C194-35 7C196-35 Min.	7C194-35 7C196-35 Max.	7C194-45 7C196-45 Min.	7C194-45 7C196-45 Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE1}, $_{ACE2}$	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid — 7C196		15		20		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z — 7C196	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z — 7C196		13		15		20	ns
t_{LZCE1}, $_{CE2}$	$\overline{CE}$ LOW to Low Z[7]	3		3		3		ns
t_{HZCE1}, $_{CE2}$	$\overline{CE}$ HIGH to High Z[7, 8]		13		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	20		30		40		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		40		ns
t_{AW}	Address Set-Up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		17		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]	0	13	0	15	0	20	ns

Notes:

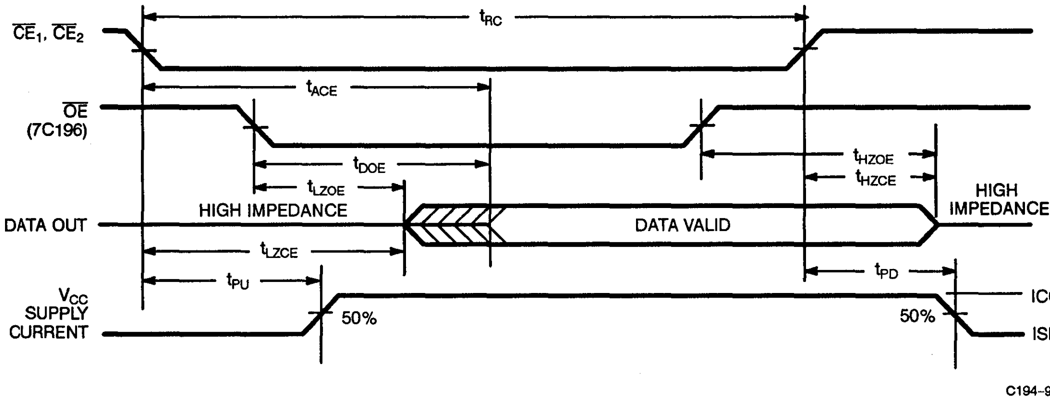
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

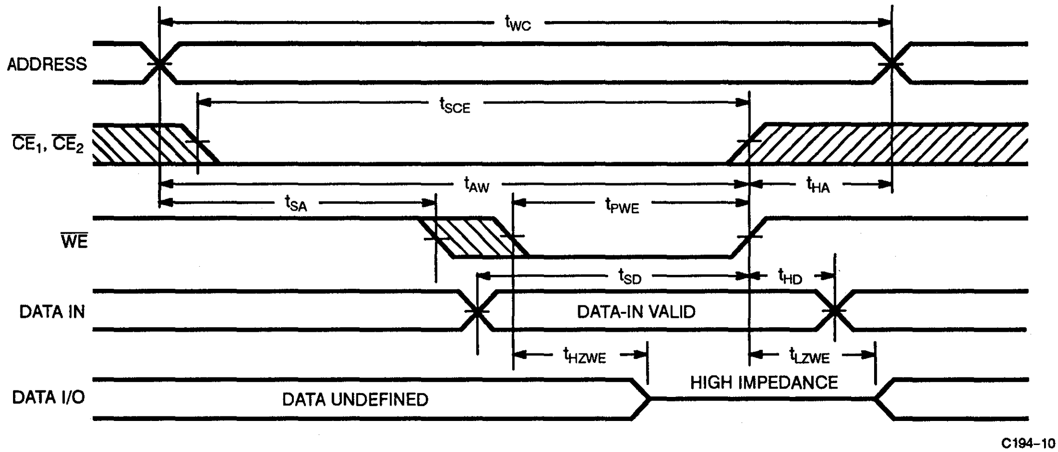
Read Cycle No. 1[10, 11]



Read Cycle No. 2[10, 12]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[9, 13]

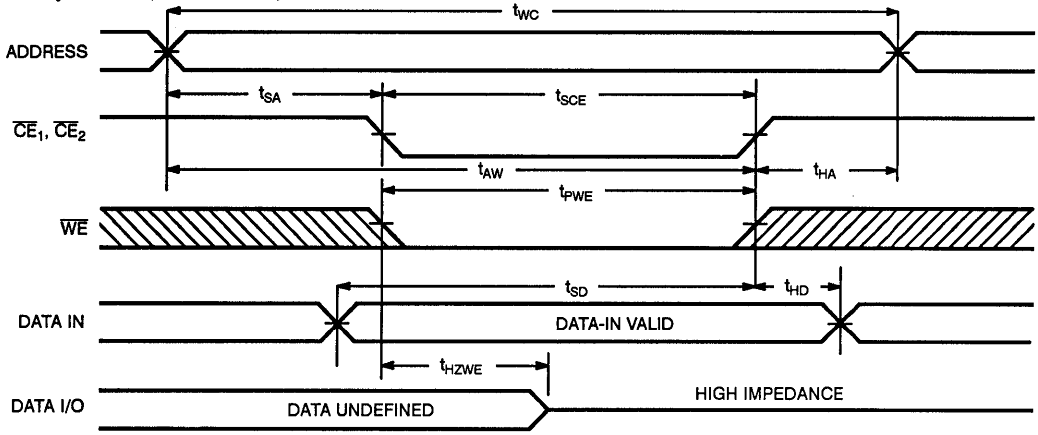


Notes:

10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}_1 = V_{IL}/\overline{CE}_2 = V_{IL}$ (7C196: $\overline{OE} = V_{IL}$, $\overline{CE}_2 = V_{IL}$ also).
12. Address valid prior to or coincident with $\overline{CE}_1$ and $\overline{CE}_2$ transition low.
12. 7C196 only: Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

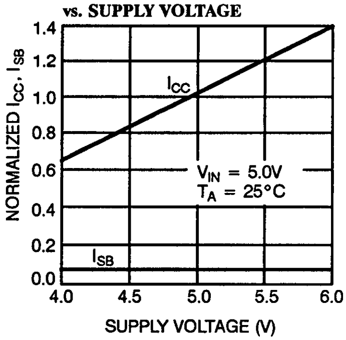
Write Cycle No. 2 ($\overline{CE}$ Controlled)[9, 13, 14]



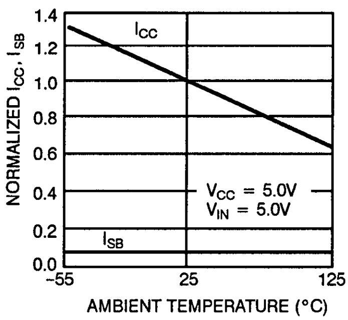
C194–11

Typical DC and AC Characteristics

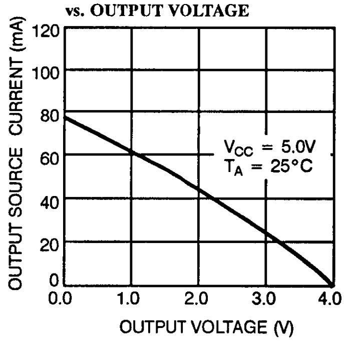
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



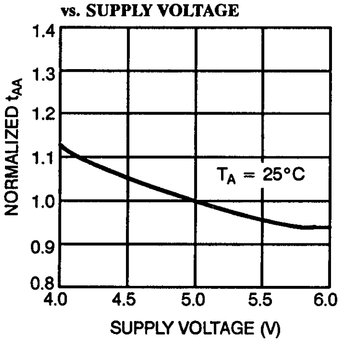
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



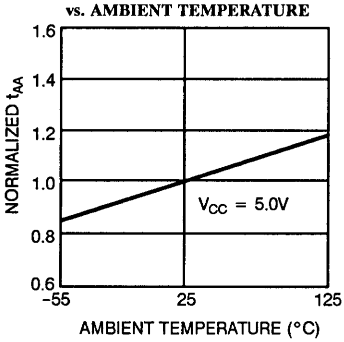
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



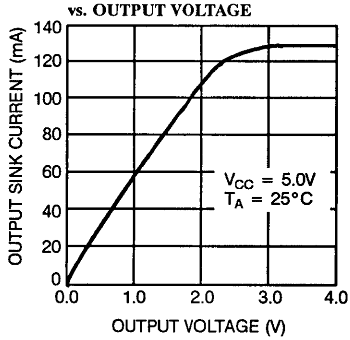
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

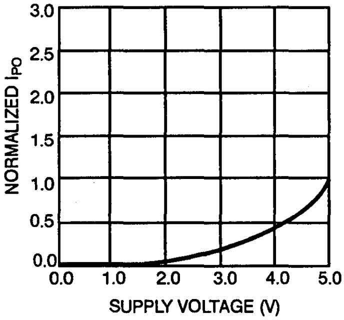


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

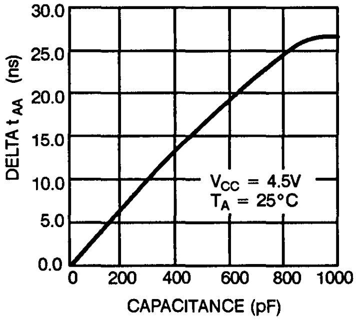


Typical DC and AC Characteristics (continued)

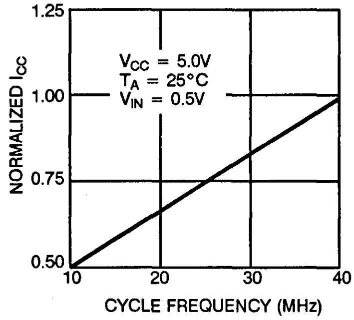
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



7C194 Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7C196 Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	H	X	X		
L	L	H	L	Data Out	Read
L	L	L	X	Data In	Write
L	L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C194-25PC	P13	Commercial
	CY7C194-25VC	V13	
	CY7C194-25DC	D14	
	CY7C194-25LC	L54	
	CY7C194-25DMB	D14	Military
	CY7C194-25LMB	L54	
	CY7C194-25KMB	K73	
35	CY7C194-35PC	P13	Commercial
	CY7C194-35VC	V13	
	CY7C194-35DC	D14	
	CY7C194-35LC	L54	
	CY7C194-35DMB	D14	Military
	CY7C194-35LMB	L54	
	CY7C194-35KMB	K73	
45	CY7C194-45PC	P13	Commercial
	CY7C194-45VC	V13	
	CY7C194-45DC	D14	
	CY7C194-45LC	L54	
	CY7C194-45DMB	D14	Military
	CY7C194-45LMB	L54	
	CY7C194-45KMB	K73	

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C196-25PC	P21	Commercial
	CY7C196-25VC	V21	
	CY7C196-25DC	D22	
	CY7C196-25LC	L54	
	CY7C196-25DMB	D22	Military
	CY7C196-25LMB	L54	
	CY7C196-25KMB	K74	
35	CY7C196-35PC	P21	Commercial
	CY7C196-35VC	V21	
	CY7C196-35DC	D22	
	CY7C196-35LC	L54	
	CY7C196-35DMB	D22	Military
	CY7C196-35LMB	L54	
	CY7C196-35KMB	K74	
45	CY7C196-45PC	P21	Commercial
	CY7C196-45VC	V21	
	CY7C196-45DC	D22	
	CY7C196-45LC	L54	
	CY7C196-45DMB	D22	Military
	CY7C196-45LMB	L54	
	CY7C196-45KMB	K74	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}, $_{ACE2}$	7, 8, 9, 10, 11
t_{DOE}[15]	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}	7, 8, 9, 10, 11
t_{ADV}	7, 8, 9, 10, 11

Note:
15. 7C196 only.

Document #: 38-00081-D

CYPRESS SEMICONDUCTOR

262,144 x 1 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - 25 ns
- Low active power
  - 550 mW
- Low standby power
  - 193 mW
- TTL-compatible imputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C197 is a high-performance CMOS static RAM organized as 262,144 words by 1 bit. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The CY7C197 has an automatic power-down feature, reducing the power consumption by 65% when deselected.

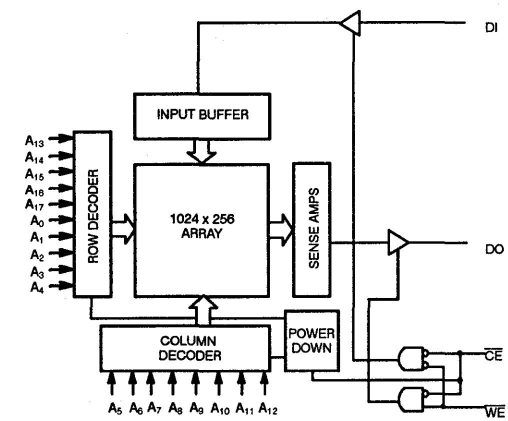
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pin (D_{IN}) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output (D_{OUT}) pin.

The output pin stays in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

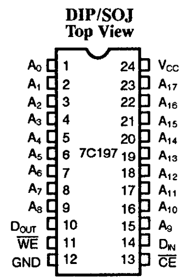
The 7C197 utilizes a die coat to insure alpha immunity.

Logic Block Diagram

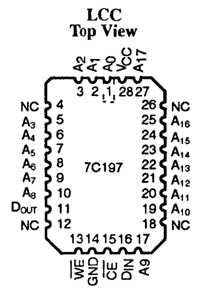


C197-1

Pin Configurations



C197-2



C197-3

Selection Guide

		7C197-25	7C197-35	7C197-45
Maximum Access Current (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	100	100	100
	Military	110	110	110
Maximum Standby Current (mA)		35	35	35

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions			7C197-25, 35, 45 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA			2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA	Mil		0.4	V
			I_{OL} = 12.0 mA	Com'l		0.4	V
V_{IH}	Input HIGH Voltage				2.2	V_{CC}	V
V_{IL}	Input LOW Voltage				−3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$			−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled			−50	+50	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND				−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA		Com'l		100	mA
				Mil		110	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE} \geq V_{IH}$				35	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current[4]	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$				20	mA

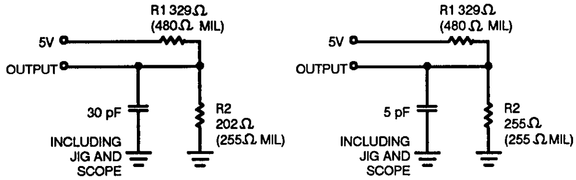
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

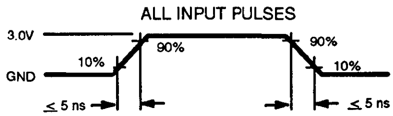
Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



(a) (b) C197-4



C197-5

Equivalent to: THEVENIN EQUIVALENT

Commercial Military

Switching Characteristics Over the Operating Range[2,6]

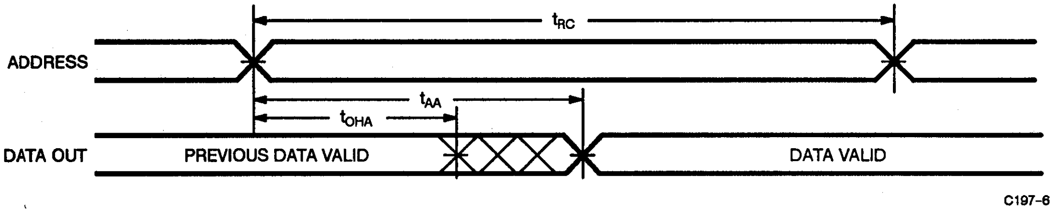
Parameters	Description	7C197-25		7C197-35		7C197-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]	0	13	0	15	0	20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		25		30	ns
WRITE CYCLE[9]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		40		ns
t_{AW}	Address Set-Up to Write End	20		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		17		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]	0	13	0	15	0	20	ns

Notes:

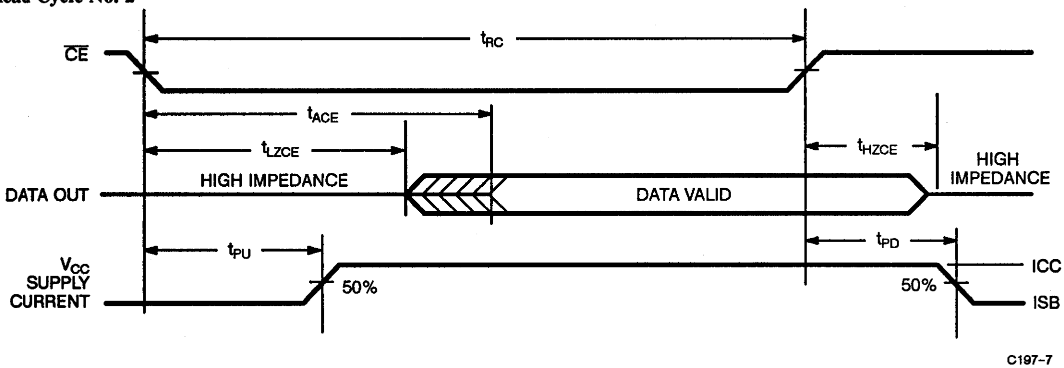
6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads and Waveforms. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

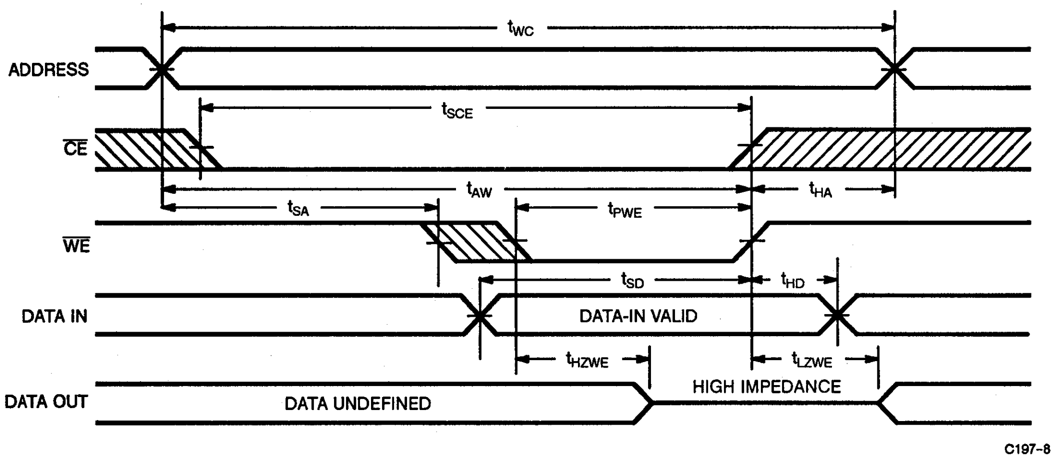
Read Cycle No. 1[10, 11]



Read Cycle No. 2[11]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[10]



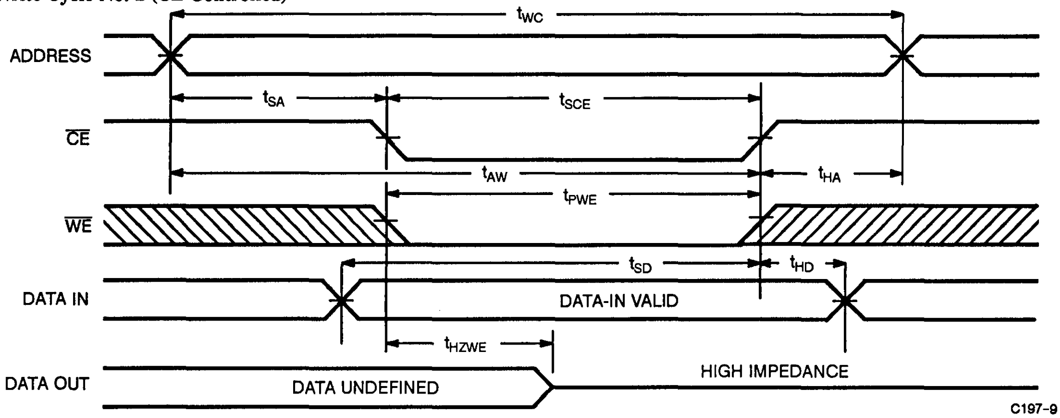
Notes:

10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE} = V_{IL}$.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

2

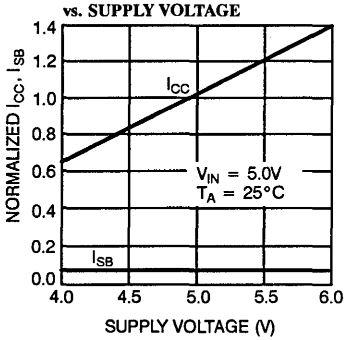
Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[10, 12]

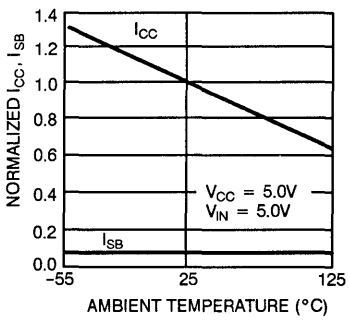


Typical DC and AC Characteristics

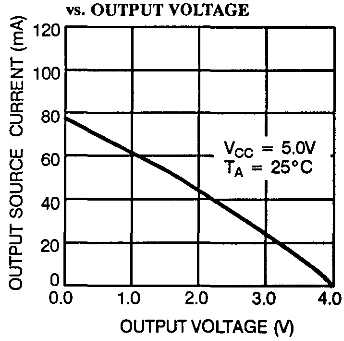
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



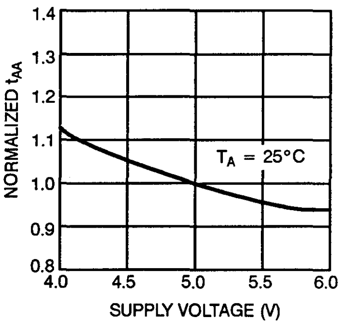
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



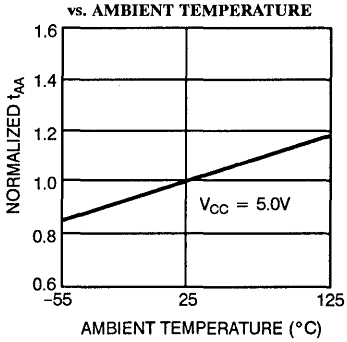
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



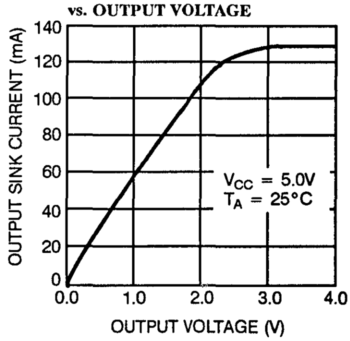
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

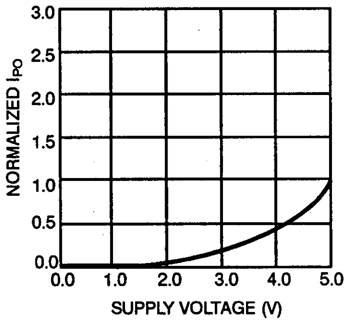


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

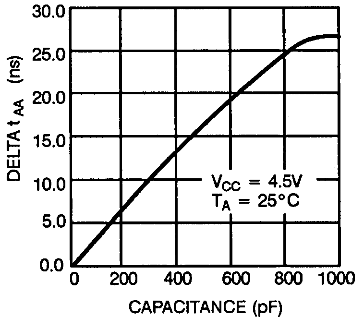


Typical DC and AC Characteristics (continued)

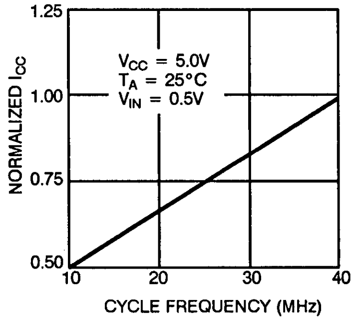
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



7C164 Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C197-25PC	P13	Commercial
	CY7C197-25VC	V13	
	CY7C197-25DC	D14	
	CY7C197-25LC	L54	
	CY7C197-25DMB	D14	Military
	CY7C197-25LMB	L54	
	CY7C197-25KMB	K73	
35	CY7C197-35PC	P13	Commercial
	CY7C197-35VC	V13	
	CY7C197-35DC	D14	
	CY7C197-35LC	L54	
	CY7C197-35DMB	D14	Military
	CY7C197-35LMB	L54	
	CY7C197-35KMB	K73	
45	CY7C197-45PC	P13	Commercial
	CY7C197-45VC	V13	
	CY7C197-45DC	D14	
	CY7C197-45LC	L54	
	CY7C197-45DMB	D14	Military
	CY7C197-45LMB	L54	
	CY7C197-45KMB	K73	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00078-E

CYPRESS SEMICONDUCTOR

32,768 x 8 Static R/W RAM

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
  - 25 ns
- Low active power
  - 825 mW
- Low standby power
  - 193 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

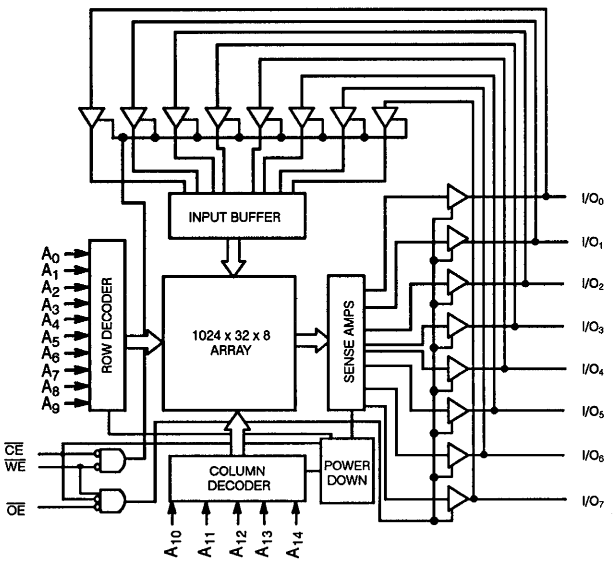
Functional Description

The CY7C198 and CY7C199 are high-performance CMOS static RAMs organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. Both devices have an automatic power-down feature, reducing the power consumption by 77% when deselected. The CY7C199 is in the space-saving 300-mil-wide DIP package and leadless chip carrier. The CY7C198 is in the standard 600-mil-wide package.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

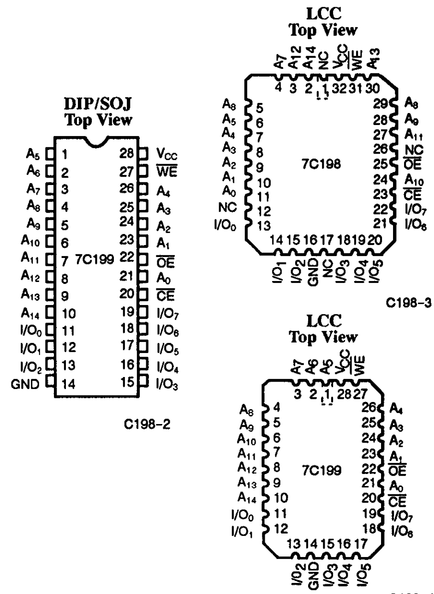
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram



C198-1

Pin Configurations



C198-2 C198-3 C198-4

Selection Guide

		7C198-25 7C199-25	7C198-35 7C199-35	7C198-45 7C199-45	7C198-55 7C199-55
Maximum Access Time (ns)		25	35	45	55
Maximum Operating Current (mA)	Commercial	170	150	150	150
	Military		160	160	160
Maximum Standby Current (mA)		35	35	35	35

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[2]

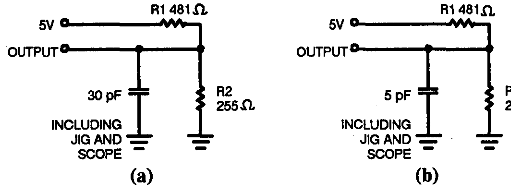
Parameters	Description	Test Conditions		7C198-25 7C199-25		7C198-35, 45, 55 7C199-35, 45, 55		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	Automatic $\overline{CE}$ Power-Down Current	V_{CC} = Max. I_{OUT} = 0 mA	Com'l		170		150	mA
			Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%			35		35	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V_{CC}, $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$			20		20	mA

Capacitance[4]

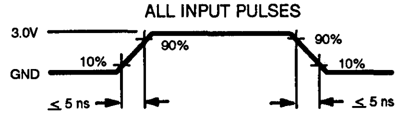
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	pF

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

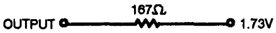


C198-5



C198-6

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[2,5]

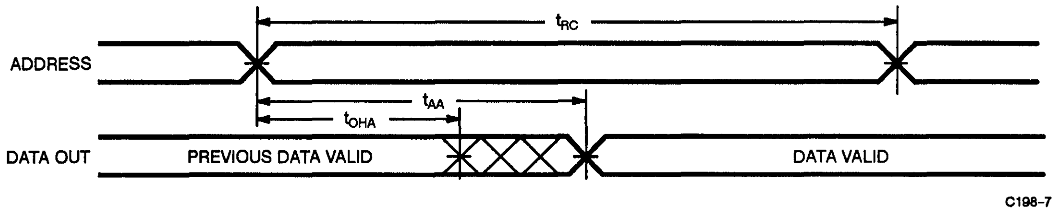
Parameters	Description	7C198-25 7C199-25		7C198-35 7C199-35		7C198-45 7C199-45		7C198-55 7C199-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		20		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6]		13		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6,7]		13		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		25		25	ns
WRITE CYCLE[8]										
t_{WC}	Write Cycle Time	25		35		45		50		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	20		30		40		50		ns
t_{AW}	Address Set-Up to Write End	20		30		40		50		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		40		ns
t_{SD}	Data Set-Up to Write End	15		17		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6]		13		15		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		3		ns

Notes:

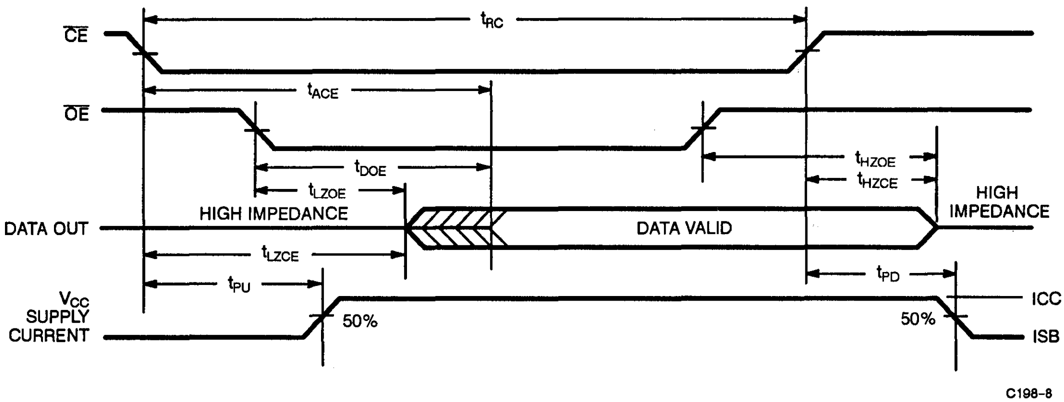
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

Switching Waveforms

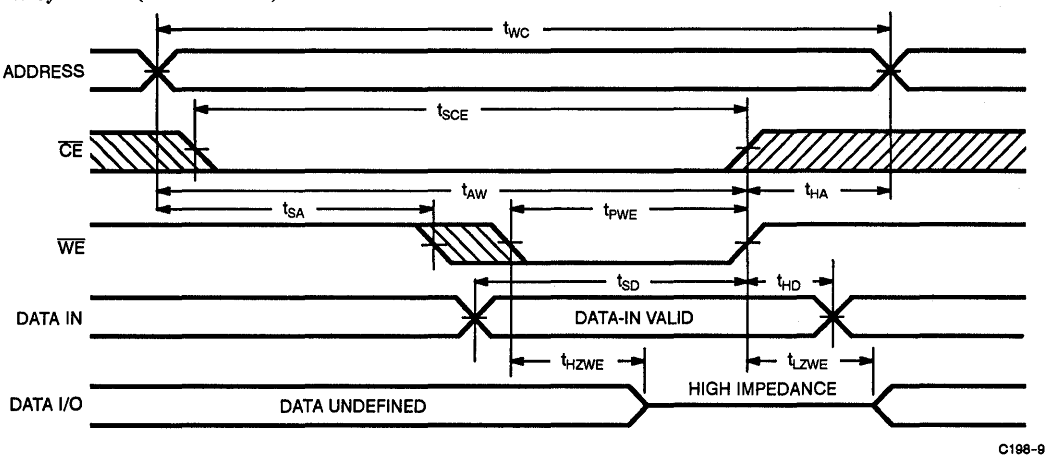
Read Cycle No. 1[9,10]



Read Cycle No. 2[10, 11]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[8, 12]

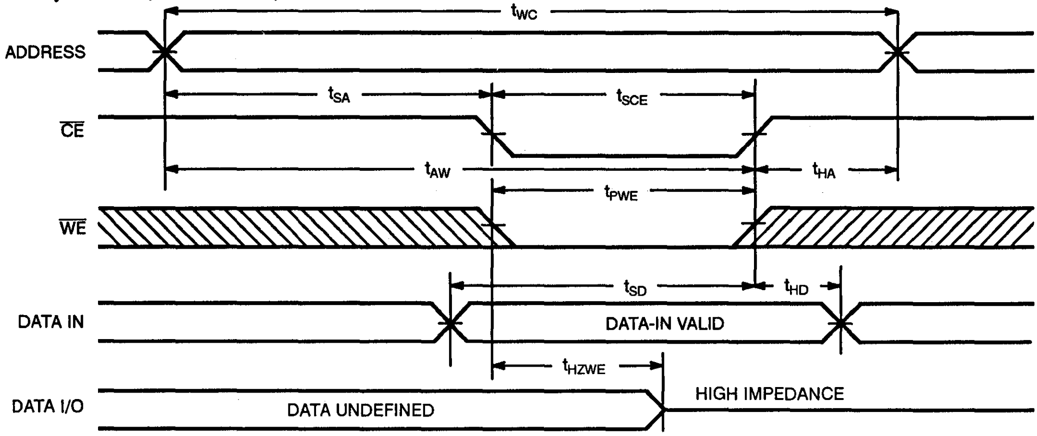


Notes:

9. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CE}$ transition low.
11. $\overline{WE}$ is HIGH for read cycle.
12. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

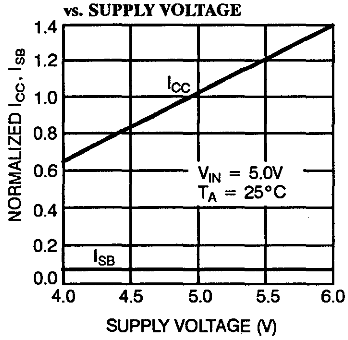
Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 12, 13]



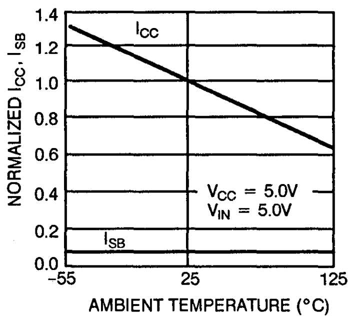
C198–10

Typical DC and AC Characteristics

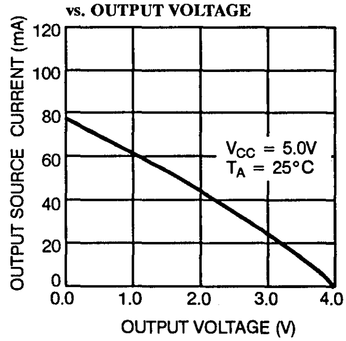
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



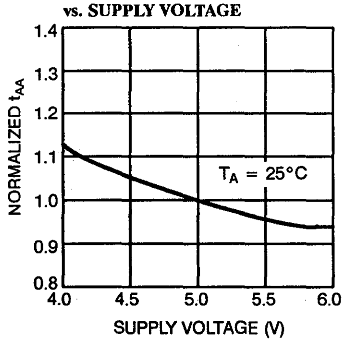
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



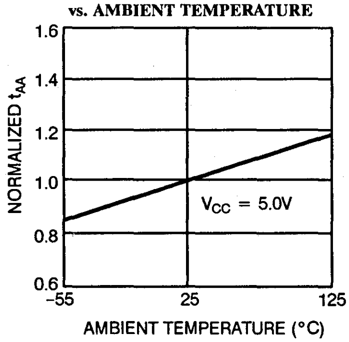
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



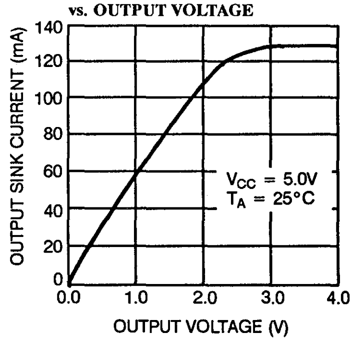
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



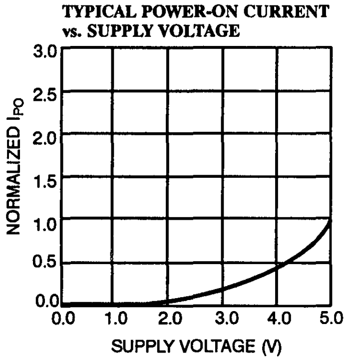
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE

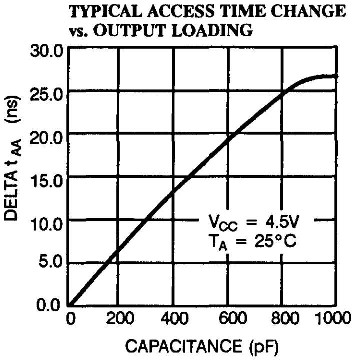


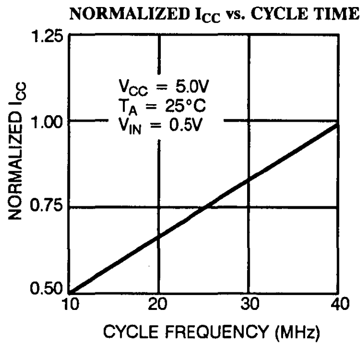
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



Typical DC and AC Characteristics (continued)







Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C198-25PC	P15	Commercial
	CY7C198-25DC	D16	
35	CY7C198-35PC	P15	Commercial
	CY7C198-35DC	D16	
	CY7C198-35DMB	D16	Military
	CY7C198-35LMB	L55	
45	CY7C198-45PC	P15	Commercial
	CY7C198-45DC	D16	
	CY7C198-45DMB	D16	Military
	CY7C198-45LMB	L55	
55	CY7C198-55PC	P15	Commercial
	CY7C198-55DC	D16	
	CY7C198-55DMB	D16	Military
	CY7C198-55LMB	L55	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C199-25PC	P21	Commercial
	CY7C199-25VC	V21	
	CY7C199-25DC	D22	
	CY7C199-25LC	L54	
35	CY7C199-35PC	P21	Commercial
	CY7C199-35VC	V21	
	CY7C199-35DC	D22	
	CY7C199-35LC	L54	
	CY7C199-35DMB	D22	Military
	CY7C199-35LMB	L54	
	CY7C199-35KMB	K74	
45	CY7C199-45PC	P13	Commercial
	CY7C199-45VC	V13	
	CY7C199-45DC	D14	
	CY7C199-45LC	L54	
	CY7C199-45DMB	D14	Military
	CY7C199-45LMB	L54	
	CY7C199-45KMB	K74	
55	CY7C199-55PC	P13	Commercial
	CY7C199-55VC	V13	
	CY7C199-55DC	D14	
	CY7C199-55LC	L54	
	CY7C199-55DMB	D14	Military
	CY7C199-55LMB	L54	
	CY7C199-55KMB	K74	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{OS}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB1}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11

Document #: 38-00077-F

CYPRESS SEMICONDUCTOR

16 x 4 Static R/W RAM

Features

- **Fully decoded, 16 word x 4-bit high-speed CMOS RAMs**
- **Inverting outputs 27S03, 27LS03, 74S189**
- **Non-inverting outputs 27S07**
- **High speed**
  - **25 ns**
- **Low power**
  - **210 mW (27LS03)**
- **Power supply 5V ± 10%**
- **Advanced high-speed CMOS processing for optimum speed/power product**
- **Capable of withstanding greater than 2001V static discharge**
- **Three-state outputs**
- **TTL-compatible inteface levels**

Functional Description

These devices are high-performance 64-bit static RAMs organized as 16 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and three-state outputs. The devices are provided with inverting and non-inverting outputs.

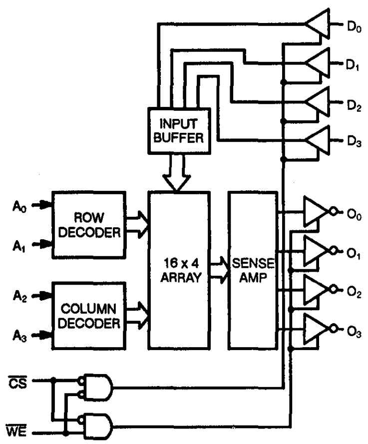
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs (D_0 through D_3) is written into the memory location specified on the address pins (A_0 through A_3). The outputs are preconditioned so that the write data is present at the outputs when the write cycle is complete. This precondition operation ensures minimum write recovery times by eliminating the "write recovery glitch."

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four output pins (O_0 through O_3) in inverted or non-inverted (CY27S07) format.

The output pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

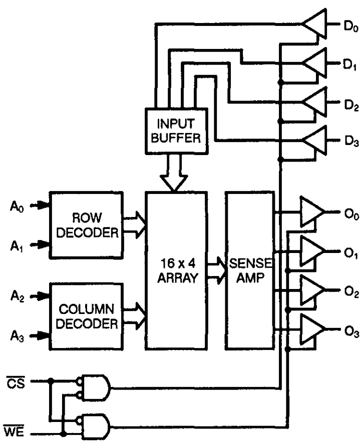
Logic Block Diagram

27S03, 27LS03, 74S189



S189-1

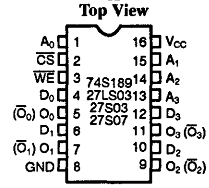
27S07



S189-2

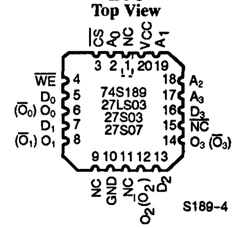
Pin Configurations

DIP
Top View



S189-3

LCC
Top View



S189-4

Selection Guide (For higher performance and lower power, refer to the CY7C189/90 data sheet.)

		27S03A 27S07A	27S03, 27S07 74S189	27LS03
Maximum Access Time (ns)	Commercial	25	35	
	Military	25	35	65
Maximum Operating Current (mA)	Commercial	90	90	
	Military	100	100	38

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... − 65°C to + 150°C

Ambient Temperature with
Power Applied .... − 55°C to + 125°C

Supply Voltage to Ground Potential
(Pin 16 to Pin 8) .... − 0.5V to + 7.0V

DC Voltage Applied to Outputs
in High Z State .... − 0.5V to + 7.0V

DC Input Voltage .... − 3.0V to + 7.0V

Output Current, into Outpus (Low) .... 10 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military[1]	− 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range [2]

Parameters	Description	Test Conditions		74S189, 27S03, 27S07 Min.	74S189, 27S03, 27S07 Max.	27LS03 Min.	27LS03 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.45			V
		V_{CC} = Min., I_{OL} = 8.0 mA					0.45	
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			− 3.0	0.8	− 3.0	0.8	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$		− 10	+ 10	− 10	+ 10	μA
V_{CD}	Input Diode Clamp Voltage			Note 3		Note 3		
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$		− 40	+ 40	− 40	+ 40	μA
I_{OS}	Output Short Circuit Current [4]	V_{CC} = Max., V_{OUT} = GND			− 90		− 90	mA
I_{OS}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		90			mA
			Mil		100		38	mA

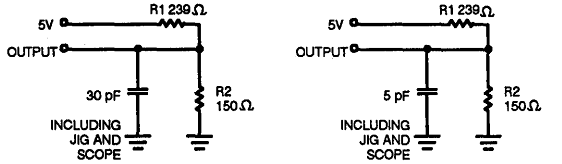
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	pF

Notes:

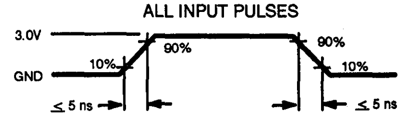
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. The CMOS process does not provide a clamp diode. However these devices are insensitive to − 3V DC input levels and − 5V undershoot pulses of less than 5 ns (measured at 50% points).
4. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



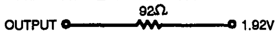
(a) (b)

S189-5



S189-6

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [2,6]

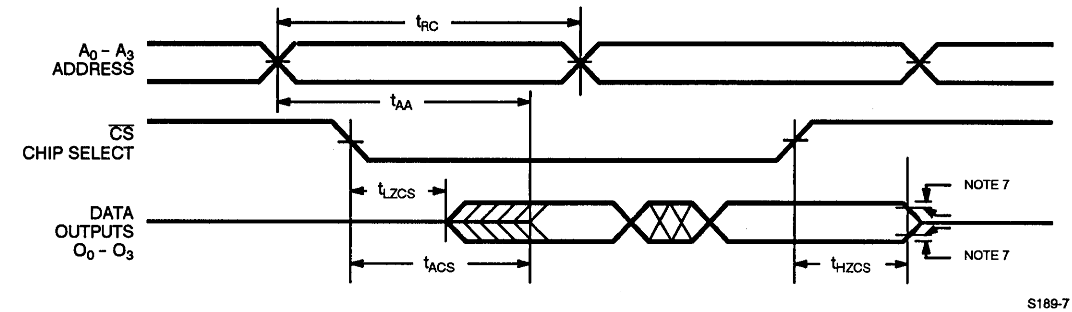
Parameters	Description	27S03A 27S07A		27S03 27S07		74S189		27LS03		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		35		65		ns
t_{AA}	Address to Data Valid [7]		25		35		35		65	ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid [7]		15		17		22		35	ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [8, 9, 10]		15		20		17		35	ns
WRITE CYCLE [6, 11, 12]										
t_{WC}	Write Cycle Time	25		35		35		65		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SCS}	$\overline{CS}$ Set-Up to Write Start					0				ns
t_{HCS}	$\overline{CS}$ Hold from Write End					0				ns
t_{SD}	Data Set-Up to Write End	20		25		20		55		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		20		55		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [8, 9, 10]		20		25		20		35	ns
t_{AWE}	$\overline{WE}$ HIGH to Output Valid [7]		20		35		30		35	ns

Notes:

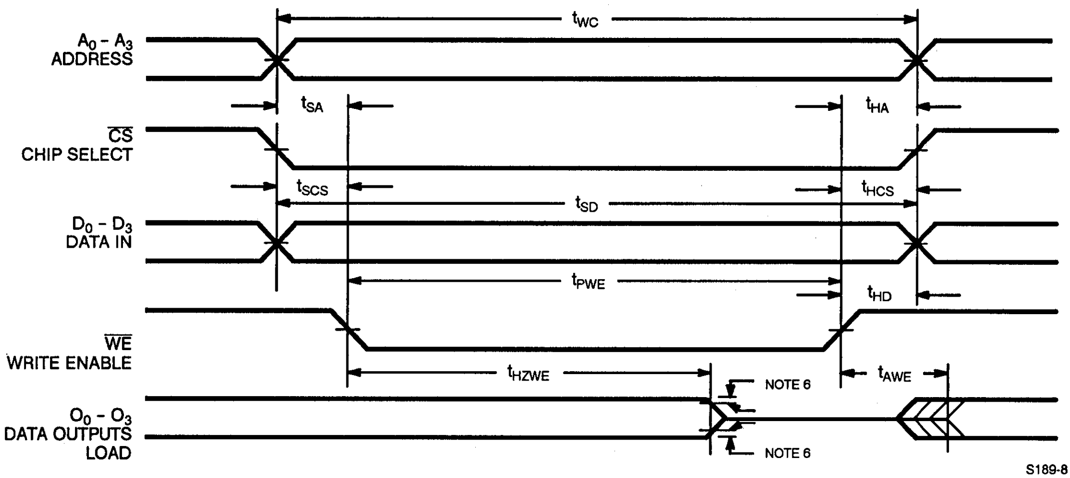
6. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the spcified I_{OL}/I_{OH} and 30-pF load capacitance.
7. t_{AA}, t_{ACS}, and t_{AWE} are tested with $C_L = 30$ pF as in part (a) of AC Test Loads. Timing is referenced to 1.5V on the inputs and outputs.
8. Transition is measured at steady-state HIGH level − 500 mV or steady-state LOW level + 500 mV on the output from 1.5V level on the input.
9. t_{HZCS} and t_{HZWE} are tested with $C_L = 5$ pF as in part (b) of AC Test Loads.
10. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
11. Output is preconditioned to data in (inverted or non-inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
12. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminates the write.

Switching Waveforms

Read Cycle



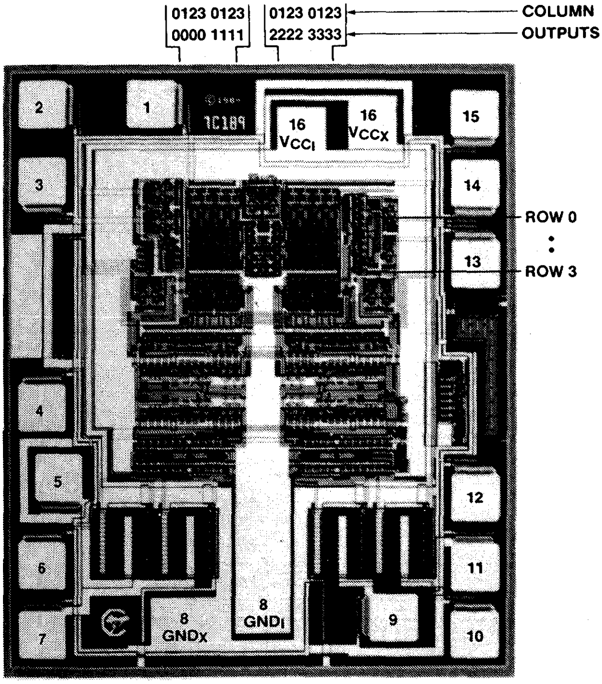
Write Cycle [13, 14]



Notes:

13. All measurements referenced to 1.5V.
14. Timing diagram represents one solution which results in optimum cycle time. Timing may be changed in various applications as long as the worst case limits are not violate.

Bit Map



Address Designators

Address Name	Address Function	Pin Number
A_0	AXO	1
A_1	AX1	15
A_2	AY0	14
A_3	AY1	13

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY27S03APC	P1	Commercial
	CY27S03ADC	D2	
	CY27S03ALMB	L61	Military
	CY27S03ADMB	D2	
35	CY27S03PC	P1	Commercial
	CY27S03DC	D2	
	CY27S03LC	L61	
	CY27S03LMB	L61	Military
	CY27S03DMB	D2	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY27S07APC	P1	Commercial
	CY27S07ADC	D2	
	CY27S07ALMB	L61	Military
	CY27S07ADMB	D2	
35	CY27S07PC	P1	Commercial
	CY27S07DC	D2	
	CY27S07LC	L61	
	CY27S07LMB	L61	Military
	CY27S07DMB	D2	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY74S189PC	P1	Commercial
	CY74S189DC	D2	

Speed (ns)	Ordering Code	Package Type	Operating Range
65	CY27LS03LMB	L61	Military
	CY27LS03DMB	D2	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{ACS}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SCS}	7, 8, 9, 10, 11
t_{HCS}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{AWE}	7, 8, 9, 10, 11

Document #: 38-00041-C

CY93422A/93L422A
CY93422/93L422

CYPRESS SEMICONDUCTOR

256 x 4 Static R/W RAM

Features

- **256 x 4 static RAM for control stores in high-speed computers**
- **Processed with high-speed CMOS for optimum speed/power**
- **Separate inputs and outputs**
- **Low power**
  - **— Standard power:**
    660 mW (commercial)
    715 mW (military
  - **— Low power:**
    440 mW (commercial)
    495 mW (military)
- **5-volt power supply ±10% tolerance both commercial and military**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

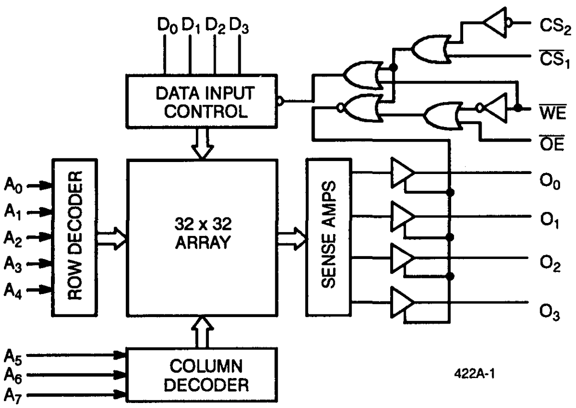
The CY93422 is a high-performance CMOS static RAM organized as 256 by 4 bits. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS}_1$) input, an active HIGH chip select two (CS_2) input, and three-state outputs.

An active LOW write enable input ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS}_1$) and write enable ($\overline{WE}$) inputs are LOW and the chip select two (CS_2) input is HIGH, the information on the four data inputs (D_0 to D_3) is written into the addressed memory word and the output circuitry is preconditioned so that the correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS}_1$) input LOW, the chip select two input (CS_2) and write enable ($\overline{WE}$) inputs HIGH, and the output enable input ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the four noninverting outputs (O_0 to O_3).

The outputs of the memory go to an active high-impedance state whenever chip select one ($\overline{CS}_1$) is HIGH, chip select two (CS_2) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

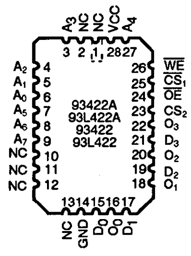
Logic Block Diagram



422A-1

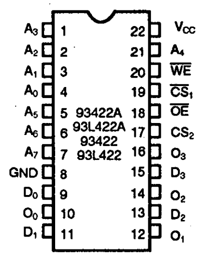
Pin Configuration

LCC
Top View



422A-2

DIP
Top View



422A-3

Selection Guide (For higher performance and lower power, refer to the CY7C122 data sheet.)

		93422A	93L422A	93422	93L422
Maximum Access Time (ns)	Commercial	35	45	45	60
	Military	45	55	60	75
Maximum Operating Current (mA)	Commercial	120	80	120	80
	Military	130	90	130	90

Maximum Rating

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 8) .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Output State .... –0.5V to $+V_{CC}$ Max.

DC Input Voltage .... –0.5V to +5.5V

Output Current into Outputs (Low) .... 20 mA

DC Input Current .... –30 mA to +5.0 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 10%
Military[1]	–55°C to +125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		93422 93422A Min.	93422 93422A Max.	93L422 93L422A Min.	93L422 93L422A Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –5.2 mA		2.4		2.4		V
V_{OL}	Output LOW Current	V_{CC} = Min., I_{OL} = 8.0 mA			0.45		0.45	V
V_{IH}	Input HIGH Level[3]	Guaranteed Input Logical HIGH Voltage for all Inputs		2.1		2.1		V
V_{IL}	Input LOW Level[3]	Guaranteed Input Logical LOW Voltage for all Inputs			0.8		0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4V			–300		–300	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 4.5V			40		40	µA
I_{SC}	Output Short Circuit Current[4]	V_{CC} = Max., V_{OUT} = 0.0V			–90		–90	mA
I_{CC}	Power Supply Current	All Inputs = GND V_{CC} = Max.	T_A = 125°C		110		70	mA
			T_A = 75°C		110		70	
			T_A = 0°C		120		80	
			T_A = –55°C		130		90	
V_{CL}	Input Clamp Voltage			See Note 5		See Note 5		
I_{CEX}	Output Leakage Current	V_{OUT} = 2.4V			50		50	µA
		V_{OUT} = 0.5V, V_{CC} = Max.		–50		–50		

Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{OUT}	Output Capacitance		7	pF

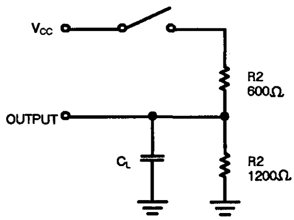
Function Table[7]

Inputs CS_2	Inputs $\overline{CS_1}$	Inputs $\overline{WE}$	Inputs $\overline{OE}$	Inputs D_n	Outputs O_n	Mode
L	X	X	X	X	High Z	Not Selected
X	H	X	X	X	High Z	Not Selected
H	L	H	H	X	High Z	Output Disable
H	L	H	L	X	Selected Data	Read Data
H	L	L	X	L	High Z	Write "0"
H	L	L	X	H	High Z	Write "1"

Notes:

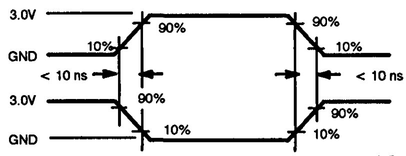
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

AC Test Loads and Waveforms



(a)

422A-4



422A-5

Commercial Switching Characteristics Over the Operating Range[8, 9]

Parameters	Description	93422A		93L422A		93422		93L422		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH(A)}$[10] $t_{PHL(A)}$	Delay from Address to Output (Address Access Time)		35		45		45		60	ns
t_{PZH} ($\overline{CS}_1$, CS_2) t_{PZH} ($\overline{CS}_1$, CS_2)	Delay from Chip Select to Active Output and Correct Data		25		30		30		35	ns
t_{PZH} ($\overline{WE}$) t_{PZL} ($\overline{WE}$)	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		25		40		40		45	ns
t_{PZH} ($\overline{OE}$) t_{PZL} ($\overline{OE}$)	Delay from Output Enable to Active Output and Correct Data		25		30		30		35	ns
t_S (A)	Set-Up Time Address (Prior to Initiation of Write)	5		5		10		5		ns
t_h (A)	Hold Time Address (After Terminiation of Write)	5		5		5		5		ns
t_S (DI)	Set-Up Time Data Input (Prior to Initiation of Write)	5		5		5		5		ns
t_h (DI)	Hold Time Data Input (After Terminitation of Write)	5		5		5		5		ns
t_S ($\overline{CS}_1$, CS_2)	Set-Up Time Chip Select (Prior to Initiation of Write)	5		5		5		5		ns
t_h ($\overline{CS}_1$, CS_2)	Hold Time Chip Select (After Termination of Write)	5		5		5		5		ns
t_{pw} ($\overline{WE}$)	Minimum Write Enable Pulse Width to Insure Write	20		40		30		45		ns
t_{PHZ} ($\overline{CS}_1$, CS_2) t_{PLZ} ($\overline{CS}_1$, CS_2)	Delay from Chip Select to Inactive Output (High Z)		30		40		30		45	ns
t_{PHZ} ($\overline{WE}$) t_{PLZ} ($\overline{WE}$)	Delay from Write Enable to Inactive Output (High Z)		30		40		30		45	ns
t_{PHZ} ($\overline{OE}$) t_{PLZ} ($\overline{OE}$)	Delay from Output Enable to Inactive Output (High Z)		30		40		30		45	ns

Military Switching Characteristics Over the Operating Range[8, 9]

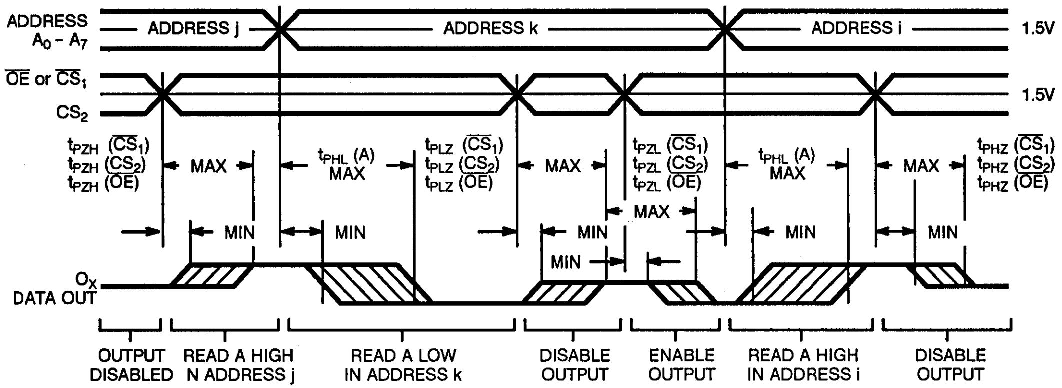
Parameters	Description	93422A		93L422A		93422		93L422		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{PLH(A)}$[10] $t_{PHL(A)}$	Delay from Address to Output (Address Access Time)		45		55		60		75	ns
t_{PZH} ($\overline{CS}_1$, CS_2) t_{PZL} ($\overline{CS}_1$, CS_2)	Delay from Chip Select to Active Output and Correct Data		35		40		45		45	ns
t_{PZH} ($\overline{WE}$) t_{PZL} ($\overline{WE}$)	Delay from Write Enable to Active Output and Correct Data (Write Recovery)		40		45		50		50	ns
t_{PZH} ($\overline{OE}$) t_{PZL} ($\overline{OE}$)	Delay from Output Enable to Active Output and Correct Data		35		40		45		45	ns
t_S (A)	Set-Up Time Address (Prior to Initiation of Write)	5		10		10		10		ns
t_h (A)	Hold Time Address (After Terminiation of Write)	5		5		5		10		ns
t_S (DI)	Set-Up Time Data Input (Prior to Initiation of Write)	5		5		5		5		ns
t_h (DI)	Hold Time Data Input (After Terminitation of Write)	5		5		5		5		ns
t_S ($\overline{CS}_1$, CS_2)	Set-Up Time Chip Select (Prior to Initiation of Write)	5		5		5		5		ns
t_h ($\overline{CS}_1$, CS_2)	Hold Time Chip Select (After Termination of Write)	5		5		5		10		ns
t_{ph} ($\overline{WE}$)	Minimum Write Enable Pulse Width to Insure Write	35		40		40		45		ns
t_{PHZ} ($\overline{CS}_1$, CS_2) t_{PLZ} ($\overline{CS}_1$, CS_2)	Delay from Chip Select to Inactive Output (High Z)		35		40		45		45	ns
t_{PHZ} ($\overline{WE}$) t_{PLZ} ($\overline{WE}$)	Delay from Write Enable to Inactive Output (High Z)		40		40		45		45	ns
t_{PHZ} ($\overline{OE}$) t_{PLZ} ($\overline{OE}$)	Delay from Output Enable to Inactive Output (High Z)		35		40		45		45	ns

Notes:

4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. The CMOS process does not provide a clamp diode. However, the CY93422 is insensitive to −3V DC input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
6. Tested initially and after any design or process changes that may affect these parameters.
7. H = High Voltage Level, L = Low Voltage Level, X = Don't Care. High Z implies outputs are disabled or off. This condition is defined as a high-impedance state for the CY93422.
8. V_{CC} = 5V ± 10% and T_A = 0°C to + 75°C unless otherwise noted.
9. t_{PZH} ($\overline{WE}$), t_{PZH} ($\overline{CS}_1$, CS_2), and t_{PZH} ($\overline{OE}$) are measured with S_1 open, C_L = 15 pF, and with both the input and output timing referenced to 1.5V. t_{PZL} ($\overline{WE}$), t_{PZL} ($\overline{CS}_1$, CS_2), and t_{PZL} ($\overline{OE}$) are measured with S_1 closed, C_L = 15 pF, and with both the input and output timing referenced to 1.5V. t_{PHZ} ($\overline{WE}$), t_{PHZ} ($\overline{CS}_1$, CS_2), and t_{PHZ} ($\overline{OE}$) are measured with S_1 open, $C_L \le 5$ pF, and are measured between the 1.5V level on the input to the V_{OH} − 500 mV level on the output. t_{PLZ} ($\overline{WE}$), t_{PLZ} ($\overline{CS}_1$, CS_2), and t_{PLZ} ($\overline{OE}$) are measured with S_1 closed and $C_L \le 5$ pF, and are measured between the 1.5V level on the input and the V_{OL} +500 mV level on the output.
10. $t_{PLH(A)}$ and $t_{PHL(A)}$ are tested with S_1 closed and C_L = 15 pF with both input and output timing referenced to 1.5V.
11. Switching delays from the address, output enable, and chip select inputs to the data output. The CY93422 disabled output in the "OFF" condition is represented by a single center line.

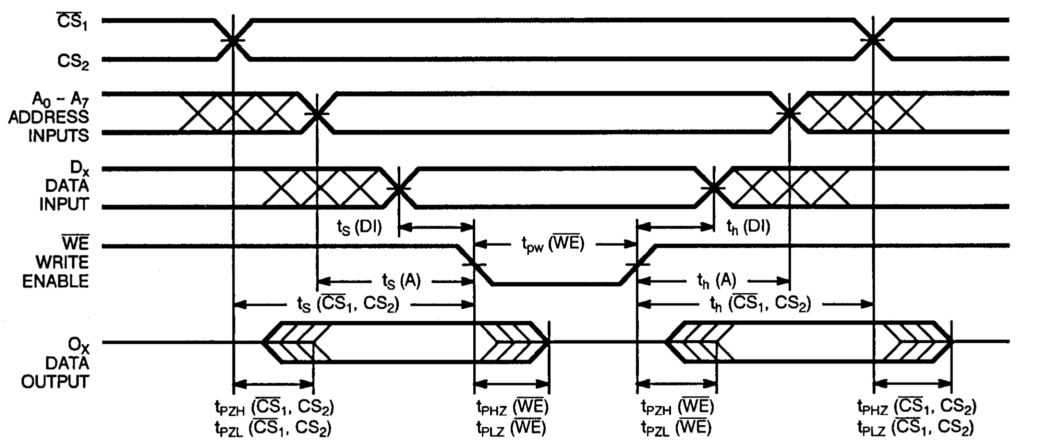
Switching Waveforms

Read Cycle[11]



422A-6

Write Cycle (with $\overline{OE}$ = LOW)



422A-7

Ordering Information

Speed (ns)	Ordering Code		Package Type	Operating Range
	Standard Power	Low Power		
35	CY93422APC		P7	Commercial
	CY93422ADC		D8	
	CY93422ALC		L54	
45	CY93422PC	CY93L422APC	P7	Commercial
	CY93422DC	CY93L422ADC	D8	
	CY93422LC	CY93L422ALC	L54	
	CY93422ADMB		D8	Military
	CY93422ALMB		L54	
55		CY93L422ADMB	D8	Military
		CY93L422ALMB	L54	
60		CY93L422PC	P7	Commercial
		CY93L422DC	D8	
		CY93L422LC	L54	
	CY93422DMB		D8	Military
	CY93422LMB		L54	
75		CY93L422DMB	D8	Military
		CY93L422LMB	L54	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
$t_{PLH(A)}$	7, 8, 9, 10, 11
$t_{PHL(A)}$	7, 8, 9, 10, 11
t_{PZH} ($\overline{CS}_1$, CS_2)	7, 8, 9, 10, 11
t_{PZL} ($\overline{CS}_1$, CS_2)	7, 8, 9, 10, 11
t_{PZH} ($\overline{WE}$)	7, 8, 9, 10, 11
t_{PZL} ($\overline{WE}$)	7, 8, 9, 10, 11
t_{PZH} ($\overline{OE}$)	7, 8, 9, 10, 11
t_{PZL} ($\overline{OE}$)	7, 8, 9, 10, 11
t_S (A)	7, 8, 9, 10, 11
t_h (A)	7, 8, 9, 10, 11
t_s (DI)	7, 8, 9, 10, 11
t_h (DI)	7, 8, 9, 10, 11
t_S ($\overline{CS}_1$, CS_2)	7, 8, 9, 10, 11
t_h ($\overline{CS}_1$, CS_2)	7, 8, 9, 10, 11
t_{pw} ($\overline{WE}$)	7, 8, 9, 10, 11

Document #: 38-00022-C

CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1220**

64K x 4 SRAM Module

Features

- **Very high speed 256K SRAM module**
  - **Access time of 10 nsec.**
- **300-mil-wide hermetic DIP package**
- **Low active power**
  - **1.8W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **On-chip decode for speed and density**
- **JEDEC pinout—compatible with 7C194 monolithic SRAMs**
- **Small PCB footprint**
  - **0.36 sq. in.**

Functional Description

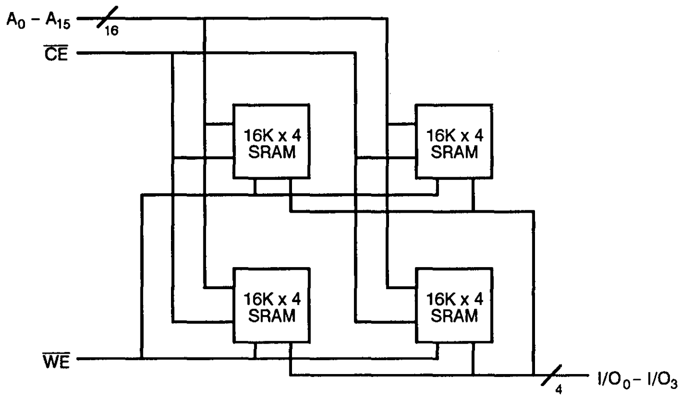
The CYM1220 is an extremely high performance 256-kilobit static RAM module organized as 65,536 words by 4 bits. This module is constructed using four 16K x 4 static RAMs in LCC packages mounted on a 300-mil-wide ceramic substrate. Extremely high speed and density are achieved by using BiCMOS SRAMs containing internal address decoding logic.

Writing to the module is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I/O_0 through I/O_3) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{15}) will appear on the four output pins (I/O_0 through I/O_3).

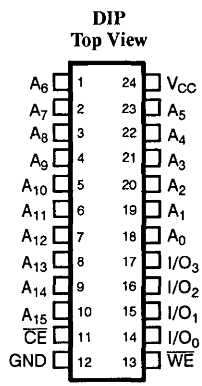
The data output pins remain in a high-impedance state unless the module is selected and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1220-1

Pin Configuration



1220-2

Selection Guide

		1220HD-10	1220HD-12	1220HD-15	1220HD-20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	325	325	325	
	Military		375	375	375
Maximum Standby Current (mA)	Commercial	200	200	200	
	Military		250	250	250

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... -65°C to +150°C

Ambient Temperature with Power Applied .... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... -0.5V to +7.0V

DC Input Voltage .... -0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		CYM1220HD Min.	CYM1220HD Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			-0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-20	+20	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		-20	+20	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE} \leq V_{IL}$	Commercial		325	mA
			Military		375	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	V_{CC} = Max., $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%	Commercial		200	mA
			Military		250	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	V_{CC} = Max., $\overline{CE} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V	Commercial		200	mA
			Military		250	

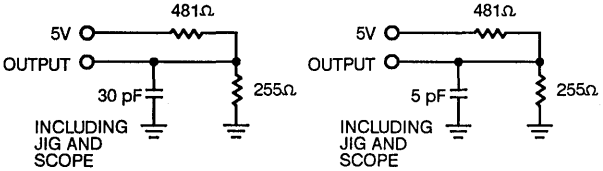
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	25	pF
C_{OUT}	Output Capacitance		30	pF

Notes:

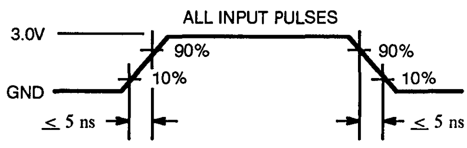
1. $V_{IL(MIN)}$ = -3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



(a) (b)

1220-3



1220-4

Switching Characteristics Over the Operating Range [3]

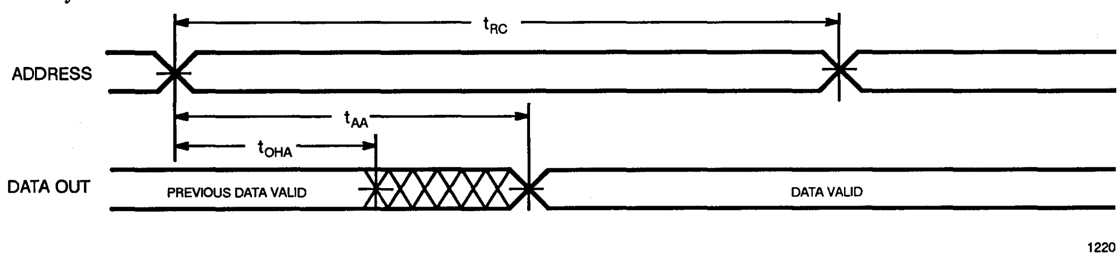
Parameters	Description	1220HD-10 Min.	1220HD-10 Max.	1220HD-12 Min.	1220HD-12 Max.	1220HD-15 Min.	1220HD-15 Max.	1220HD-20 Min.	1220HD-20 Max.	Units
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z	2		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[4]		6		8		8		8	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		10		12		15		20	ns
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		10		12		15		ns
t_{AW}	Address Set-up to Write End	8		10		12		15		ns
t_{HA}	Address Hold from Write End	1		1		1		1		ns
t_{SA}	Address Set-up from Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		12		15		ns
t_{SD}	Data Set-Up to Write End	8		10		10		10		ns
t_{HD}	Data Hold from Write End	1		1		1		1		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [4]	0	5	0	7	0	7	0	10	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CE} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{CE}$ transition low.
9. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

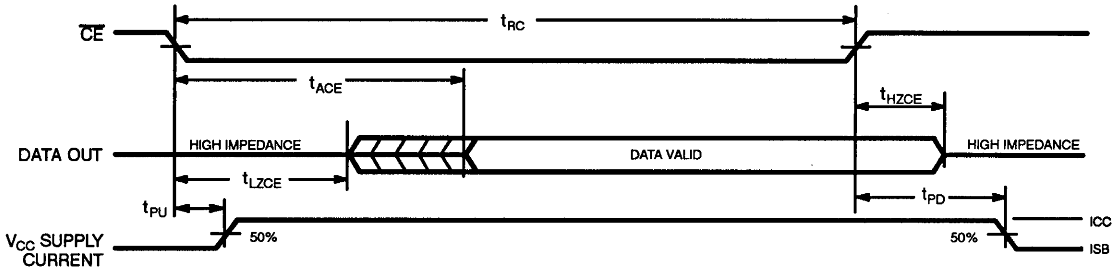
Switching Waveforms

Read Cycle No. 1[6, 7]



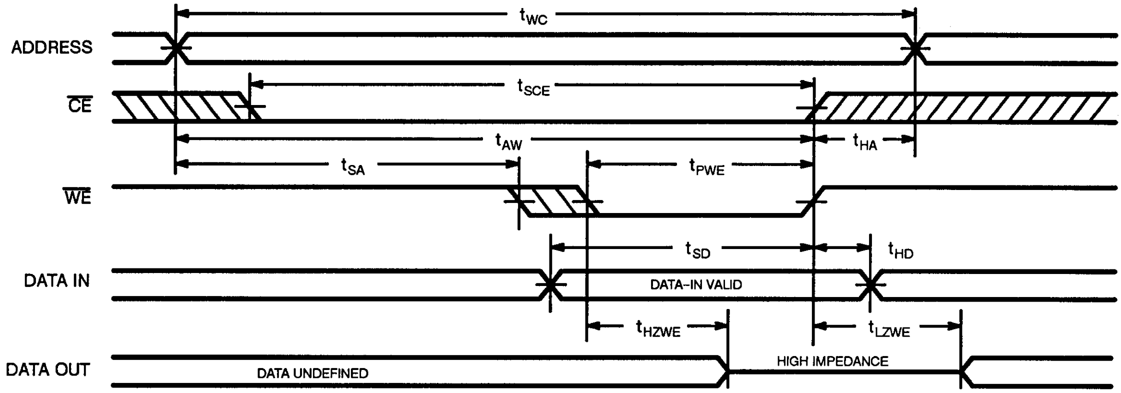
Switching Waveforms (continued)

Read Cycle No. 2[6, 8]



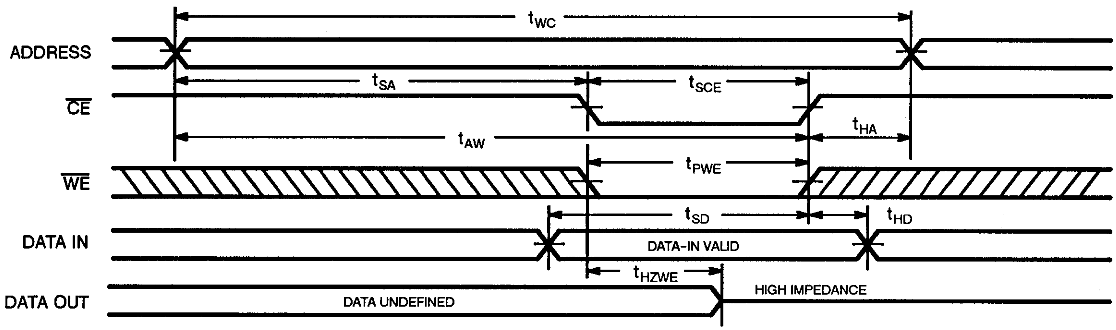
1220-6

Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



1220-7

Write Cycle No. 2 ($\overline{CE}$ Controlled)[5, 9]



1220-8

Truth Table

$\overline{CE}$	$\overline{WE}$	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read Word
L	L	Data In	Write Word

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
10	CYM1220HD-10C	HD08	Commercial
12	CYM1220HD-12C	HD08	Commercial
	CYM1220HD-12MB		Military
15	CYM1220HD-15C	HD08	Commercial
	CYM1220HD-15MB		Military
20	CYM1220HD-20MB	HD08	Military

Document #: 38-00025

CYPRESS SEMICONDUCTOR

256K X 4 SRAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 25 ns**
- **Low active power**
  - **— 2.6W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of 0.3 in.**
- **Small PCB footprint**
  - **— 0.56 sq. in.**

Functional Description

The CYM1240 is a very high performance 1-megabit static RAM module organized as 256K words by 4 bits. This module is constructed using four 256K x 1 static RAMs in LCC packages mounted on a ceramic substrate with pins. It is socket-compatible with monolithic 256K x 4 SRAMs.

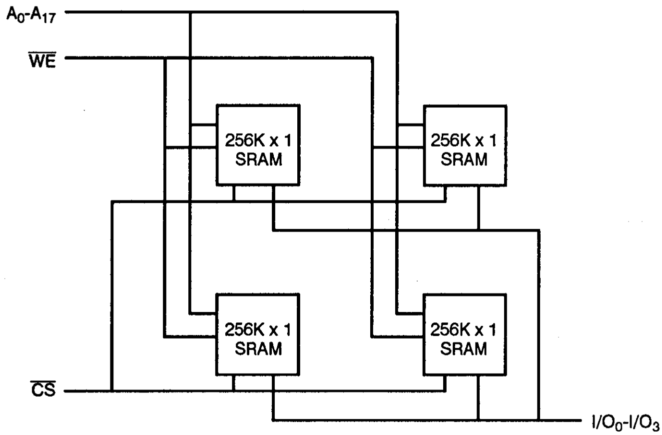
Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins ($I/O_0 - I/O_3$) of the device is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) low while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{17}) will appear on the appropriate data input/output pins ($I/O_0 - I/O_3$).

The data input/output pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or when write enable ($\overline{WE}$) is LOW.

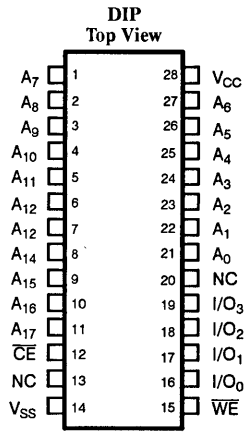
2

Logic Block Diagram



1240-1

Pin Configuration



1240-2

Selection Guide

		1240HD-25	1240HD-35	1240HD-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	480	480	480
	Military	480	480	480
Maximum Standby Current (mA)	Commercial	160	160	160
	Military	160	160	160

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... -65°C to +150°C

Ambient Temperature with
Power Applied .... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... -0.5V to +7.0V

DC Input Voltage .... -0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1240HD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]		-0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	-20	+20	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	-60	+60	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		480	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		160	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		80	mA

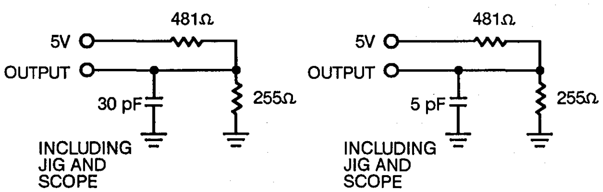
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		25	pF

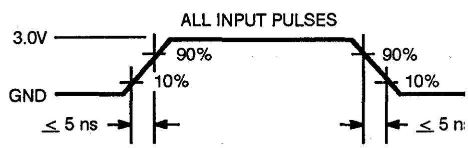
Notes:

1. $V_{IL(MIN)} = -3.0V$ for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



(a) (b) 1240-3



1240-4

Switching Characteristics Over the Operating Range[3]

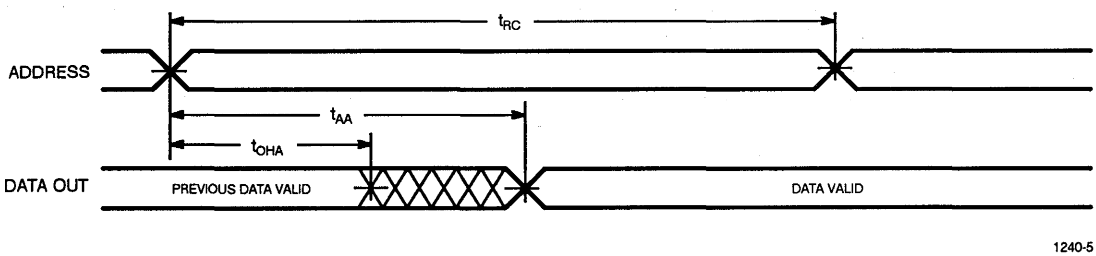
Parameters	Description	1240HD-25		1240HD-35		1240HD-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]		15		25		25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		35		ns
t_{AW}	Address Set-Up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	5		5		5		ns
t_{SA}	Address Set-Up from Write Start	0		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	15	0	25	0	25	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{CS}$ transition low.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

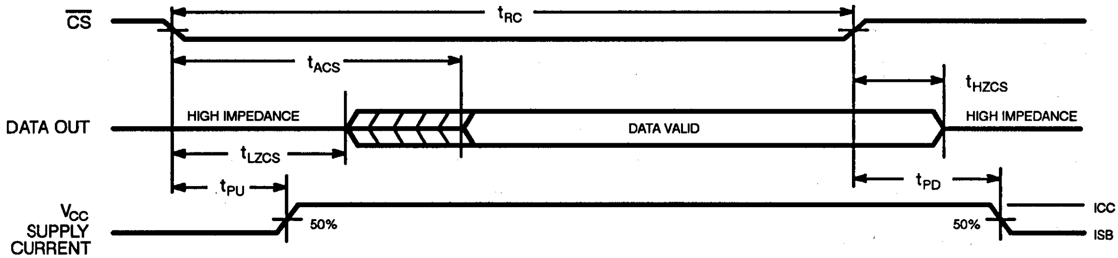
Switching Waveforms

Read Cycle No. 1[6, 7]



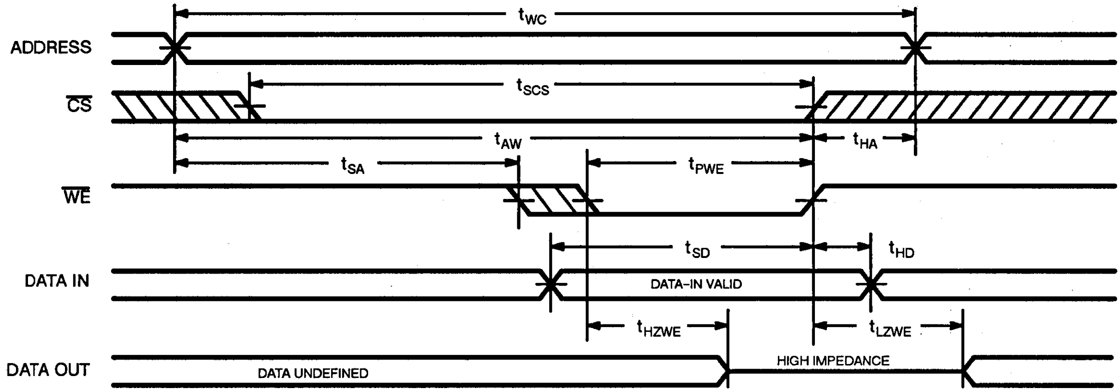
Switching Waveforms (continued)

Read Cycle No. 2[6, 8]



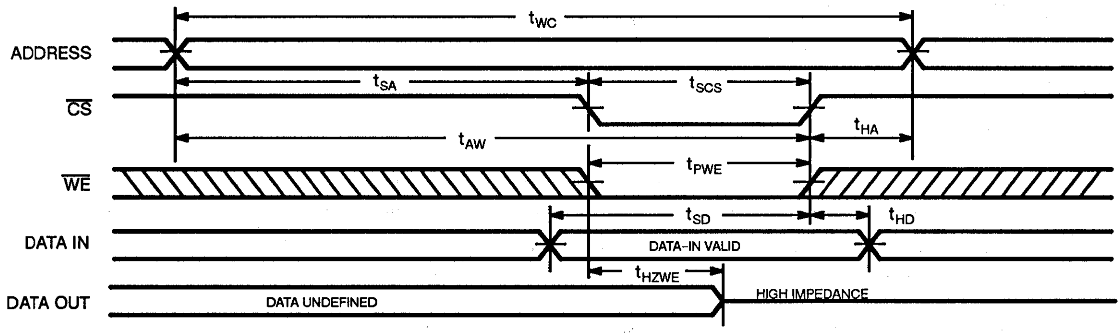
1240-6

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)[5]



1240-7

Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled)[5, 9]



1240-8

Truth Table

$\overline{CS}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read Word
L	L	Data In	Write Word

Ordering Information

Speed	Ordering Code	Operating Range
25	CYM1240HD-25C	Commercial
	CYM1240HD-25MB	Military
35	CYM1240HD-35C	Commercial
	CYM1240HD-35MB	Military
45	CYM1240HD-45C	Commercial
	CYM1240HD-45MB	Military

Document #: 38-M-00029

CYPRESS SEMICONDUCTOR

32K x 8 SRAM Module

Features

- **Very high speed 256K SRAM module**
  - **Access time of 10 nsec.**
- **300-mil-wide hermetic DIP package**
- **Low active power**
  - **2.1W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **On-chip decode for speed and density**
- **JEDEC pinout—compatible with 7C199 monolithic SRAMs**
- **Small PCB footprint**
  - **0.42 sq. in.**

Functional Description

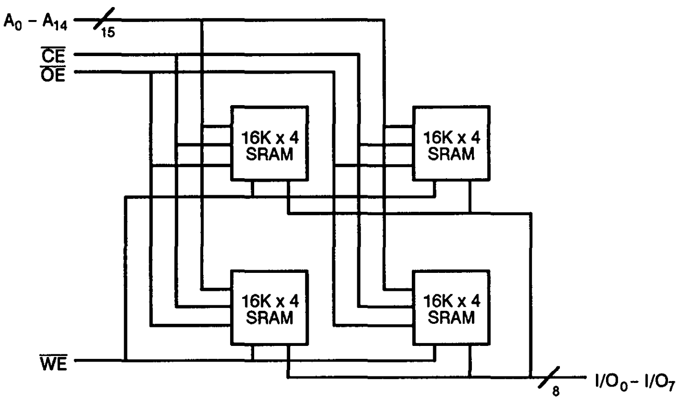
The CYM1400 is an extremely high performance 256-kilobit static RAM module organized as 32,768 words by 8 bits. This module is constructed using four 16K x 4 static RAMs in LCC packages mounted on a 300-mil-wide ceramic substrate. Extremely high speed and density are achieved by using BiCMOS SRAMs containing internal address decoding logic.

Writing to the module is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{14}) will appear on the eight output pins (I/O_0 through I/O_7).

The data output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

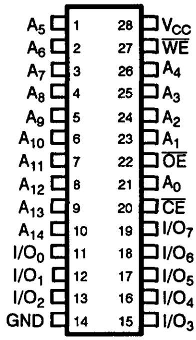
Logic Block Diagram



1400-1

Pin Configuration

DIP
Top View



1400-2

Selection Guide

		1400HD-10	1400HD-12	1400HD-15	1400HD-20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	375	375	375	
	Military		425	425	425
Maximum Standby Current (mA)	Commercial	200	200	200	
	Military		250	250	250

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		CYM1220HD Min.	CYM1220HD Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]			−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−20	+20	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CE}$ ≤ V_{IL}	Commercial		375	mA
			Military		425	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current	V_{CC} = Max., $\overline{CE}$ ≥ V_{IH}, Min. Duty Cycle = 100%	Commercial		200	mA
			Military		250	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current	V_{CC} = Max., $\overline{CE}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V	Commercial		200	mA
			Military		250	

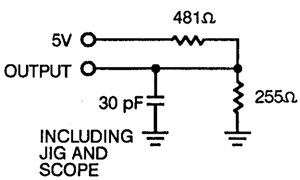
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	25	pF
C_{OUT}	Output Capacitance		30	pF

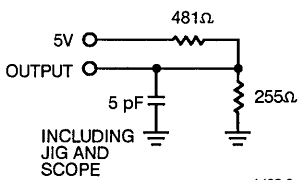
Notes:

1. $V_{IL(MIN)}$ = −3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms

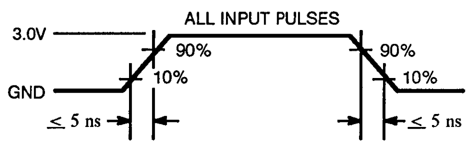


(a)



(b)

1400-3



1400-4

Switching Characteristics Over the Operating Range [3]

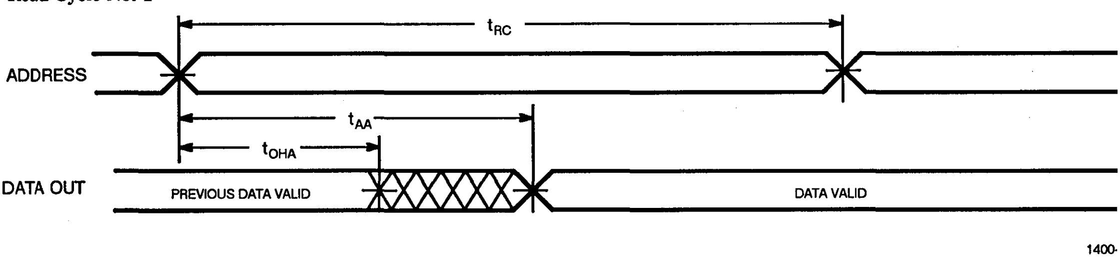
Parameters	Description	1400HD-10		1400HD-12		1400HD-15		1400HD-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	10		12		15		20		ns
t_{AA}	Address to Data Valid		10		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		3		3		3		ns
t_{ACS}	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		9		9		9	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z	2		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[4]		6		8		8		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	10		12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	8		10		12		15		ns
t_{AW}	Address Set-Up to Write End	8		10		12		15		ns
t_{HA}	Address Hold from Write End	1		1		1		1		ns
t_{SA}	Address Set-Up from Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	8		10		12		15		ns
t_{SD}	Data Set-Up to Write End	8		10		10		10		ns
t_{HD}	Data Hold from Write End	1		1		1		1		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [4]	0	5	0	7	0	7	0	10	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CE} = V_I$.
8. Address valid prior to or coincident with $\overline{CE}$ transition low.
9. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

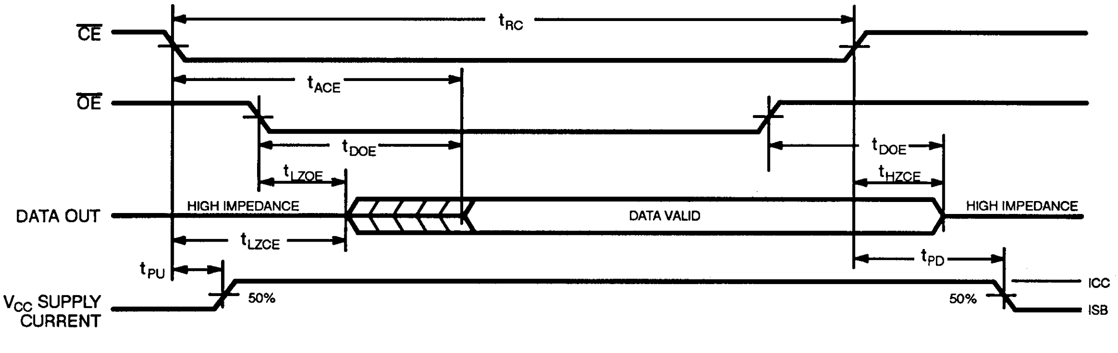
Switching Waveforms

Read Cycle No. 1[6, 7]



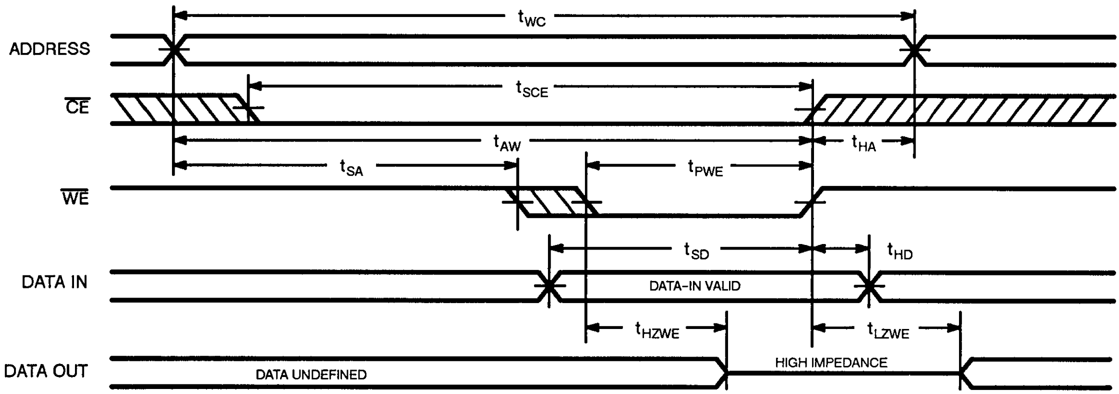
Switching Waveforms (continued)

Read Cycle No. 2 [6, 8]



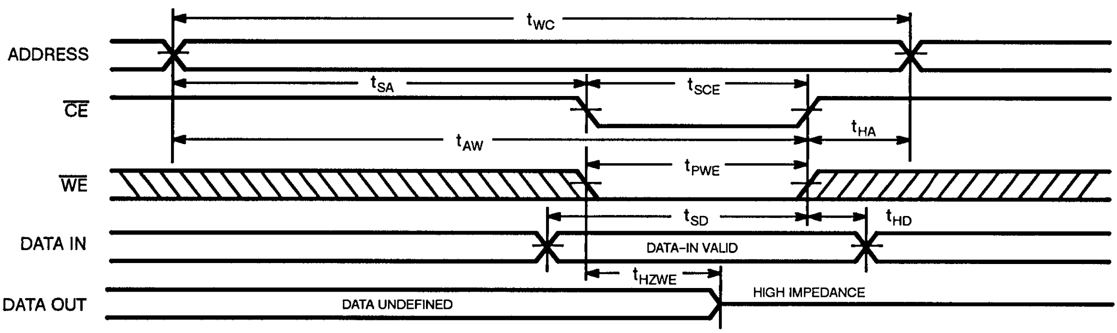
1400-6

Write Cycle No. 1 ($\overline{WE}$ Controlled) [5]



1400-7

Write Cycle No. 2 ($\overline{CE}$ Controlled) [5, 9]



1400-8

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
10	CYM1400HD-10C	HD09	Commercial
12	CYM1400HD-12C	HD09	Commercial
	CYM1400HD-12MB		Military
15	CYM1400HD-15C	HD09	Commercial
	CYM1400HD-15MB		Military
20	CYM1400HD-20MB	HD09	Military

Document #: 38-M-00022-A

CYM1420

128K x 8 Static RAM Module

CYPRESS SEMICONDUCTOR

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 30 ns**
- **32-pin, 0.6-in.-wide DIP package**
- **JEDEC-compatible pinout**
- **Low active power**
  - **— 1.2W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial and military temperature ranges**

Functional Description

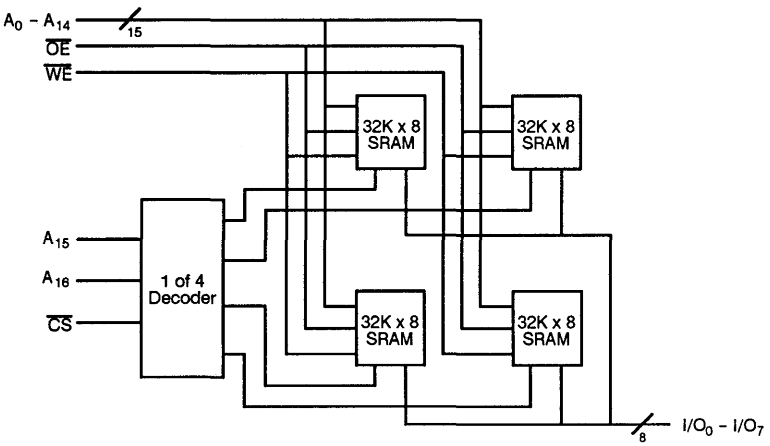
The CYM1420 is a very high performance 1-megabit static RAM module organized as 128K words by 8 bits. The module is constructed using four 32K x 8 static RAMs in leadless chip carriers mounted onto a double-sided multilayer ceramic substrate. A decoder is used to interpret the higher-order addresses A_{15} and A_{16} and to select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$), and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

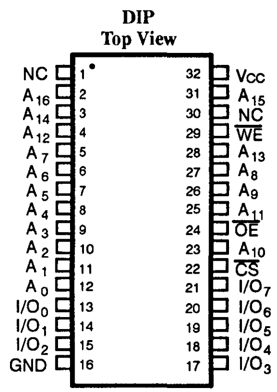
2

Logic Block Diagram



1420-1

Pin Configuration



1420-2

Selection Guide

		1420HD-30	1420HD-35	1420HD-45	1420HD-55
Maximum Access Time (ns)		30	35	45	55
Maximum Operating Current (mA)	Commercial	210	210	210	210
	Military			210	210
Maximum Standby Current (mA)	Commercial	140	140	140	140
	Military			140	140

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1420HD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−15	+15	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−15	+15	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ = V_{IL}		210	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V		80	mA

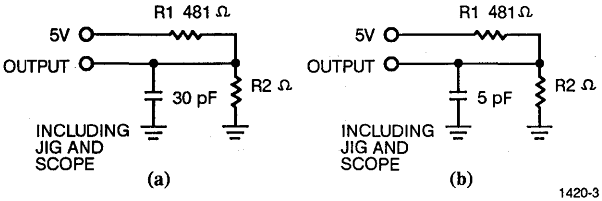
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		40	pF

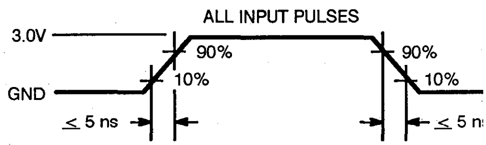
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

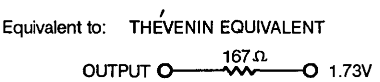
AC Test Loads and Waveforms



1420-3



1420-4



Switching Characteristics Over the Operating Range [4]

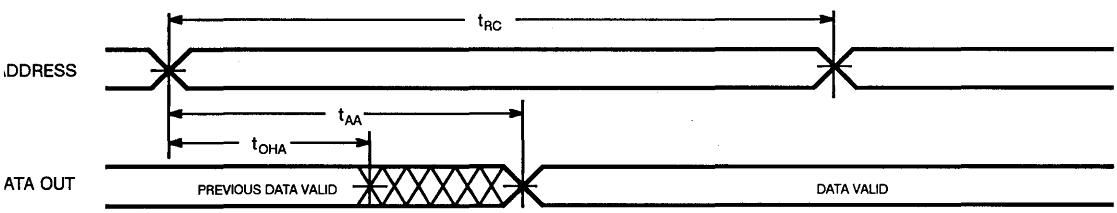
Parameters	Description	1420HD-30		1420HD-35		1420HD-45		1420HD-55		Unit
		MIn.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	30		35		45		55		ns
t_{AA}	Address to Data Valid		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		18		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		20		20		25	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		20		20		20		25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		30		35		45		55	ns
WRITE CYCLE [7]										
t_{WC}	Write Cycle Time	30		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	25		30		40		45		ns
t_{AW}	Address Set-Up to Write End	25		30		40		45		ns
t_{HA}	Address Hold from Write End	5		5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		25		25		30		ns
t_{SD}	Data Set-Up to Write End	18		18		20		25		ns
t_{HD}	Data Hold from Write End	3		3		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	15	0	15	0	15	0	25	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms [10]

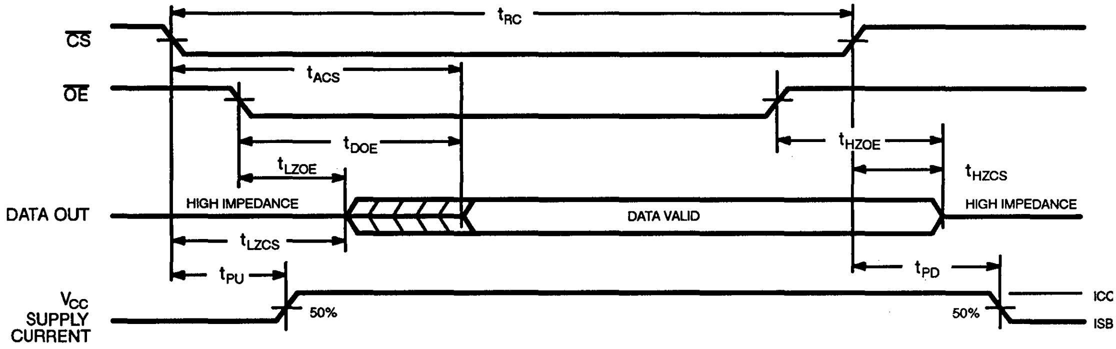
Read Cycle No. 1 [8, 9]



1420-5

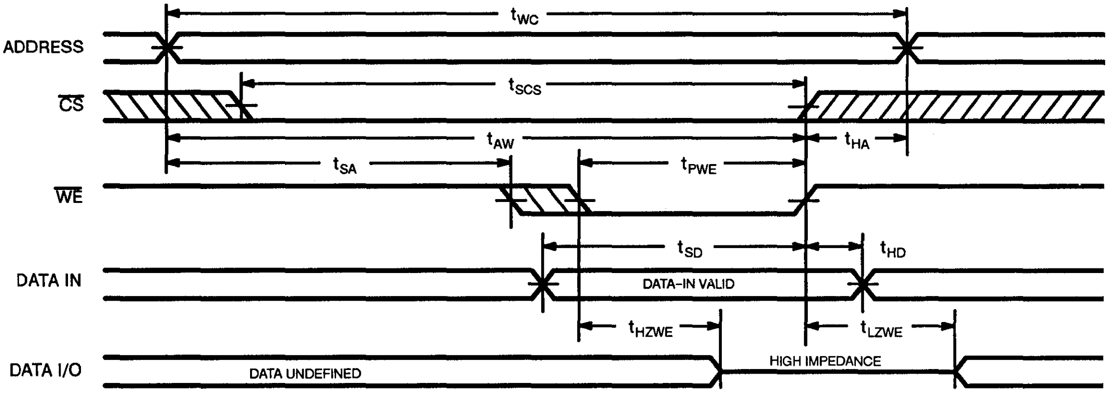
Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



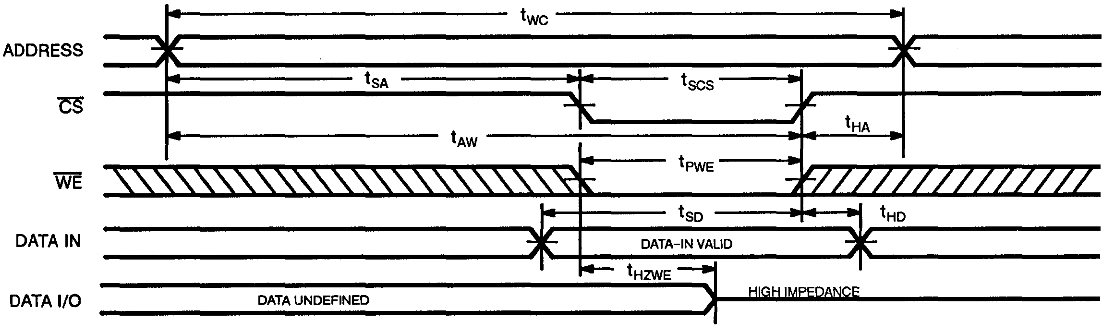
1420-6

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7, 11]



1420-7

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11, 12]



1420-8

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

2

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
30	CYM1420HD-30C	HD04	Commercial
35	CYM1420HD-35C	HD04	Commercial
45	CYM1420HD-45C	HD04	Commercial
	CYM1420HD-45MB	HD04	Military
55	CYM1420HD-55C	HD04	Commercial
	CYM1420HD-55MB	HD04	Military

Document #: 38-M-00001-A

128K x 8 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 70 ns**
- **32-pin, 0.6-in.-wide DIP package**
- **JEDEC-compatible pinout**
- **Low active power**
  - **660 mW (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **2V data retention (L version)**

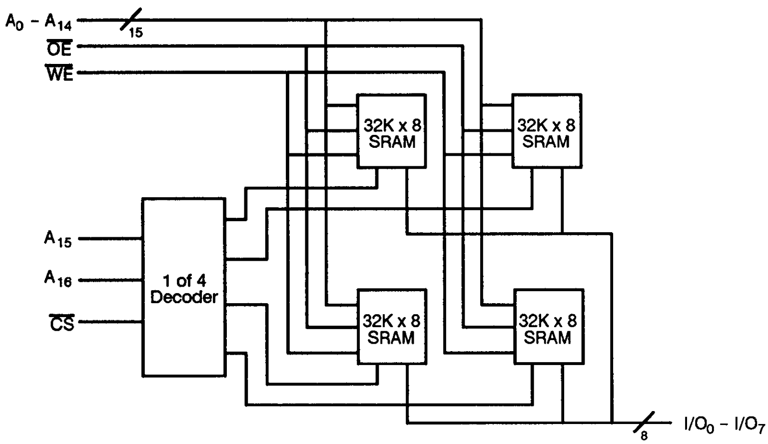
Functional Description

The CYM1421 is a high-performance 1-megabit static RAM module organized as 128K words by 8 bits. The module is constructed using four 32K x 8 static RAMs in leadless chip carriers mounted onto a double sided multilayer ceramic substrate. A decoder is used to interpret the higher-order addresses A_{15} and A_{16} and select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$), and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

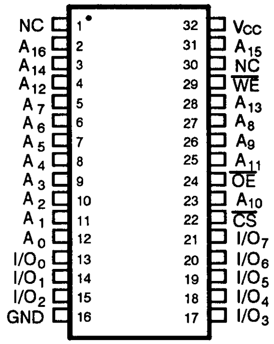
Logic Block Diagram



1421-1

Pin Configuration

DIP
Top View



1421-2

Selection Guide

		1421HD-70	1421HD-85
Maximum Access Time (ns)		70	85
Maximum Operating Current (mA)	Commercial	120	120
Maximum Standby Current (mA)	Commercial	70	70

ɅMaximum Ratings

Above which the useful life may be impaired)

ˌtorage Temperature .... -65°C to +150°C

ʌmbient Temperature with
ʼower Applied .... -10°C to +70°C

ˌupply Voltage to Ground Potential .... -0.3V to +7.0V

ƆC Voltage Applied to Outputs
n High Z State........................... -0.3V to +7.0V

ƆC Input Voltage .... -0.3V to +7.0V

Ɔutput Current into Outputs (Low) .... 50 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

2

Ǝlectrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1421HD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −1.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ = V_{IL}		120	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		70	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		20	mA

Ͻapacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		40	pF

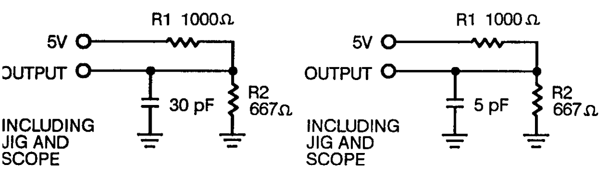
otes:

. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.

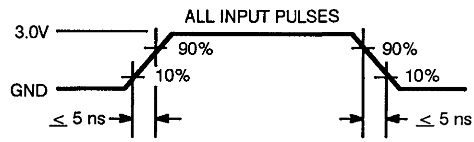
3. Tested on a sample basis.

ʌC Test Loads and Waveforms



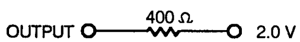
(a) (b)

1421-3



1421-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

Parameters	Description	1421HD-70		1421HD-85		Units
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	70		85		ns
t_{AA}	Address to Data Valid		70		85	ns
t_{OHA}	Data Hold from Address Change	5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		70		85	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		40		50	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		30		35	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		35		35	ns
WRITE CYCLE [7]						
t_{WC}	Write Cycle Time	70		85		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	65		75		ns
t_{AW}	Address Set-Up to Write End	65		75		ns
t_{HA}	Address Hold from Write End	10		15		ns
t_{SA}	Address Set-Up to Write Start	25		25		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		35		ns
t_{SD}	Data Set-Up to Write End	20		20		ns
t_{HD}	Data Hold from Write End	10		10		ns
t_{LZWE}	$\overline{WE}$ LOW to Low Z[6]	5		5		ns
t_{HZWE}	$\overline{WE}$ HIGH to High Z[5, 6]	0	45	0	50	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

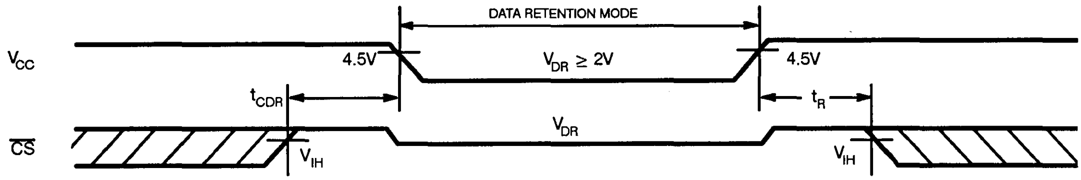
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1421		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			250	mA
t_{CDR} [13]	Chip Deselect to Data Retention Time		0		ns
t_R [13]	Operation Recovery Time		t_{RC} [12]		ns

Notes:

12. t_{RC} = Read Cycle Time.
13. Guaranteed, not tested.

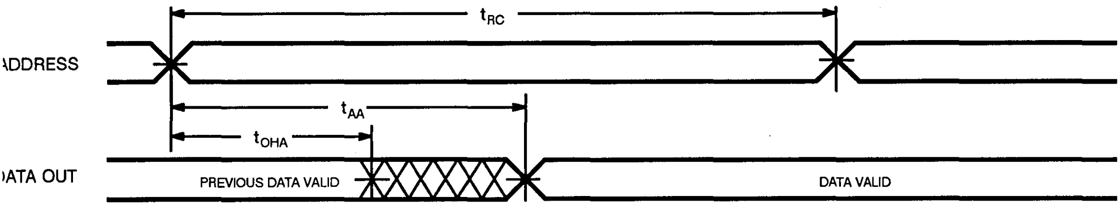
Data Retention Waveform



1421-5

Switching Waveforms [10]

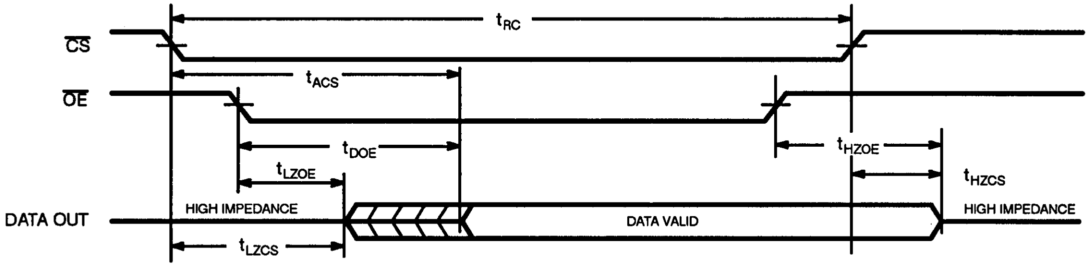
Read Cycle No. 1 [8, 9]



1421-6

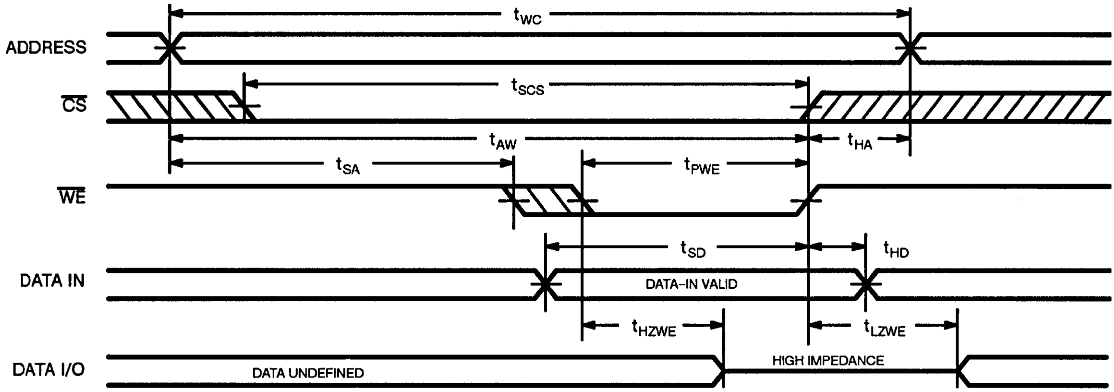
Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



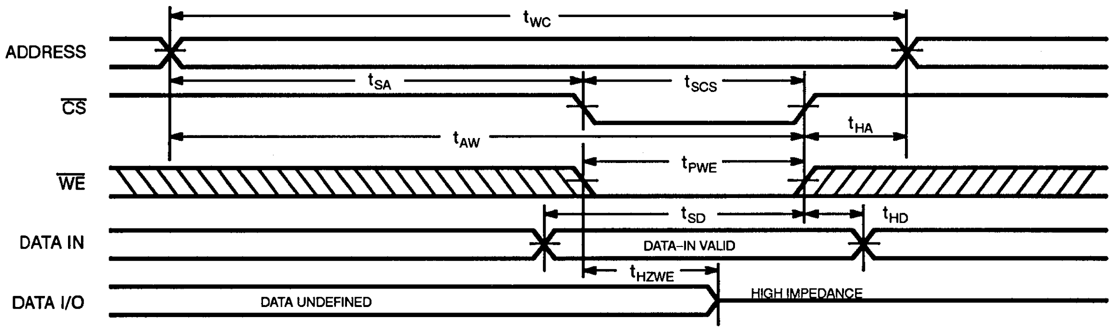
1421-7

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7, 11]



1421-8

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11, 14]



1421-9

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

2

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
70	CYM1421HD-70C	HD04	Commercial
	CYM1421LHD-70C	HD04	
85	CYM1421HD-85C	HD04	Commercial
	CYM1421LHD-85C	HD04	

Document #: 38-M-00002-A

CYPRESS SEMICONDUCTOR

128K x 8 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 30 ns**
- **Low active power**
  - **1.1W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.65 in.**
- **Small PCB footprint**
  - **0.8 sq. in.**

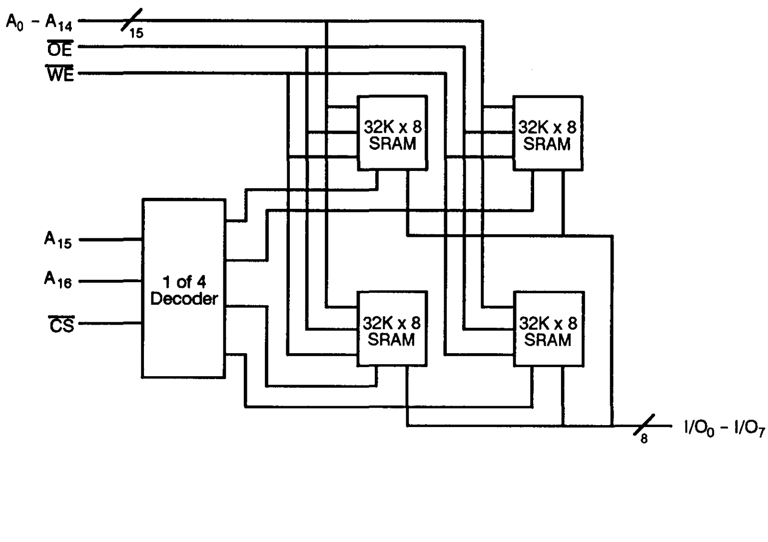
Functional Description

The CYM1422 is a high-performance 1-megabit static RAM module organized as 128K words by 8 bits. This module is constructed using four 32K x 8 static RAMs in SOICs mounted onto a single sided multilayer epoxy laminate board with pins. A decoder is used to interpret the higher-order address A_{15} and A_{16} and select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

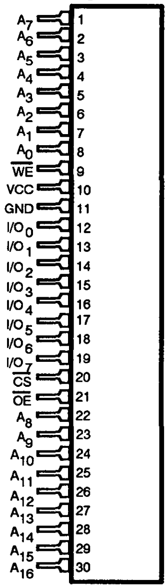
Logic Block Diagram



1422-1

Pin Configuration

SIP
Component Side



1422-2

Selection Guide

	1422PS-30	1422PS-35	1422PS-45	1422PS-55
Maximum Access Time (ns)	30	35	45	55
Maximum Operating Current (mA)	200	200	200	200
Maximum Standby Current (mA)	140	140	140	140

128K x 8 Static RAM Module

2

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 45 ns**
- **32-pin, 0.6-inch-wide DIP package**
- **JEDEC-compatible pinout**
- **Low active power**
  - **— 1.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial temperature range**
- **Small PCB footprint**
  - **— 1.1 sq. in.**

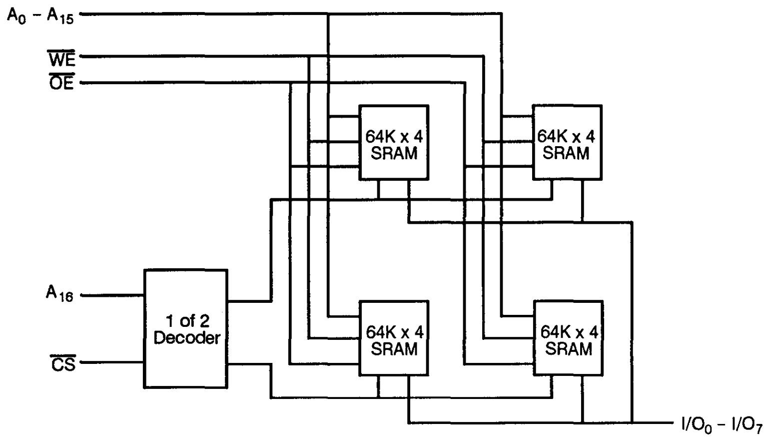
Functional Description

The CYM1423 is a high-performance 1-megabit static RAM module organized as 128K words by 8 bits. This module is constructed using four 64K x 4 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins. A decoder is used to interpret the higher-order address and select two of the four RAMs.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{16}) will appear on the eight input/output pins (I/O_0 through I/O_7).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

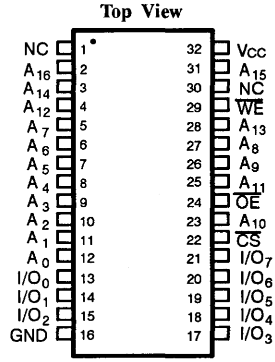
Logic Block Diagram



1423-1

Pin Configuration

DIP
Top View



1423-2

Selection Guide

	1423PD-45	1423PD-55	1423PD-70
Maximum Access Time (ns)	45	55	70
Maximum Operating Current (mA)	210	210	210
Maximum Standby Current (mA)	80	80	80

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −45°C to +150°C

Ambient Temperature with
Power Applied .... −10°C to +85°C

Supply Voltage to Ground Potential .... −0.3V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... −0.3V to +7.0V

DC Input Voltage .... −0.3V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1423PD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
I_{IX}	Input Load Current	GND < $V_I \leq V_{CC}$	−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		210	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		80	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{CC}$ − 0.2V, $V_{IN} \geq V_{CC}$ − 0.2V or $V_{IN} \leq$ 0.2V		80	mA

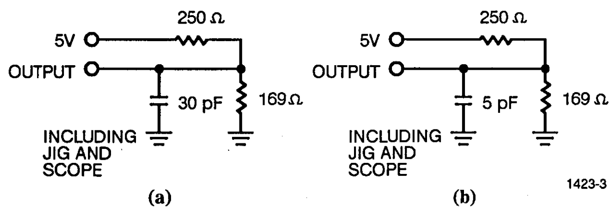
Capacitance[1]

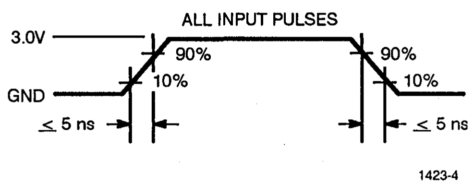
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		25	pF

Note:

1. Tested on a sample basis.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range [2]

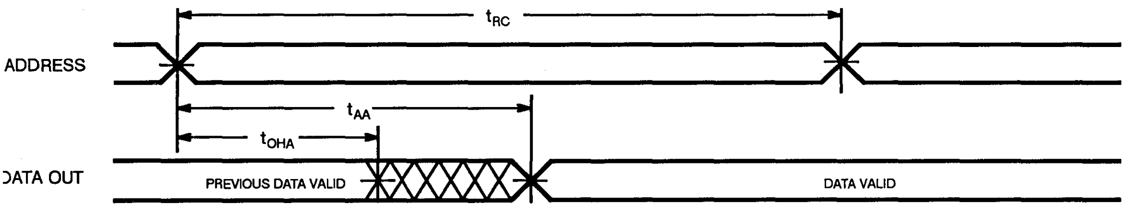
Parameters	Description	1423PD-45		1423PD-55		1423PD-70		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		20		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		25		30	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[3]		20		25		30	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	40		45		60		ns
t_{AW}	Address Set-Up to Write End	40		45		60		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up from Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		35		40		ns
t_{SD}	Data Set-Up to Write End	35		35		40		ns
t_{HD}	Data Hold from Write End	2		2		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]	0	15	0	25	0	30	ns

Notes:

2. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
3. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. $\overline{WE}$ is HIGH for read cycle.
6. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CS}$ transition low.
8. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

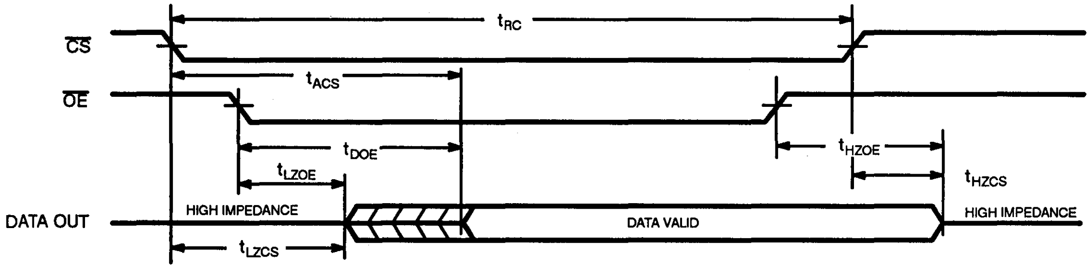
Read Cycle No. 1[5, 6]



1423-5

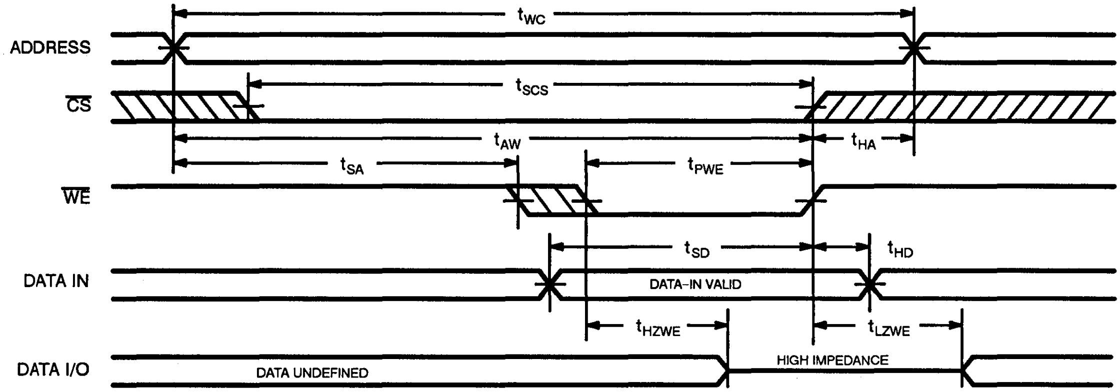
Switching Waveforms (continued)

Read Cycle No. 2 [5, 7]



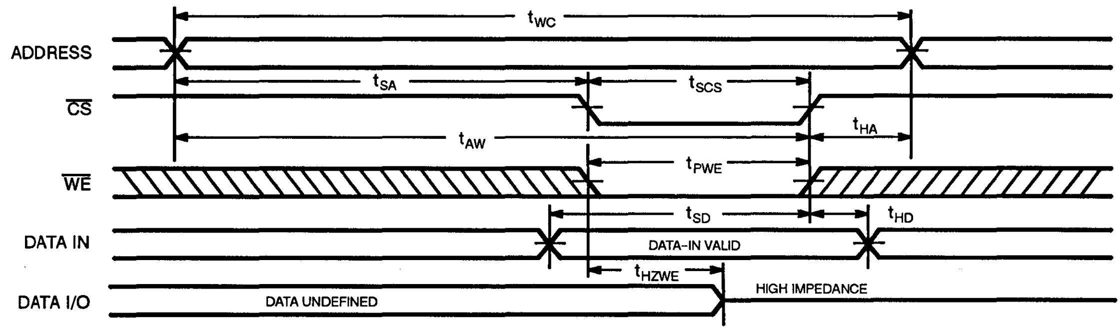
1423-6

Write Cycle No. 1 (WE Controlled) [4, 8]



1423-7

Write Cycle No. 2 (CS Controlled) [4, 8, 9]



1423-8

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
45	CYM1423PD-45C	PD01	Commercial
55	CYM1423PD-55C	PD01	Commercial
70	CYM1423PD-70C	PD01	Commercial

Document #: 38-M-00026

2

CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1441**

256K x 8 SRAM Module

Features

- **High-density 2-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 25 ns**
- **Low active power**
  - **— 5.3W (max.)**
- **SMD technology**
- **Separate Data I/O**
- **60-pin ZIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .5 in.**
- **Small PCB footprint**
  - **— 1.17 sq. in.**

Functional Description

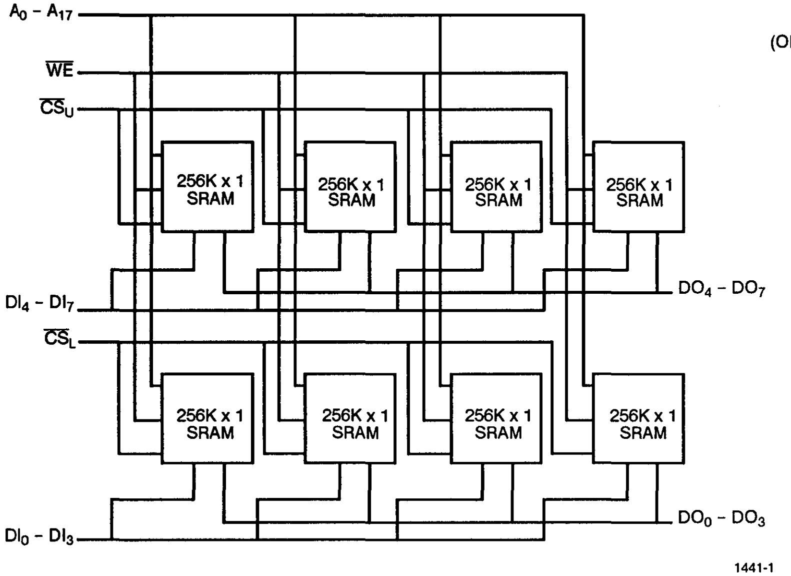
The CYM1441 is a very high performance 2-megabit static RAM module organized as 256K words by 8 bits. This module is constructed using eight 256K x 1 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins. Two chip selects ($\overline{CS}_L$ and $\overline{CS}_U$) are used to independently enable the upper and lower 4 bits of the data word.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input pins (DI_0 through DI_7) of the device is written into the memory location specified on the address pins (A_0 through A_{17}).

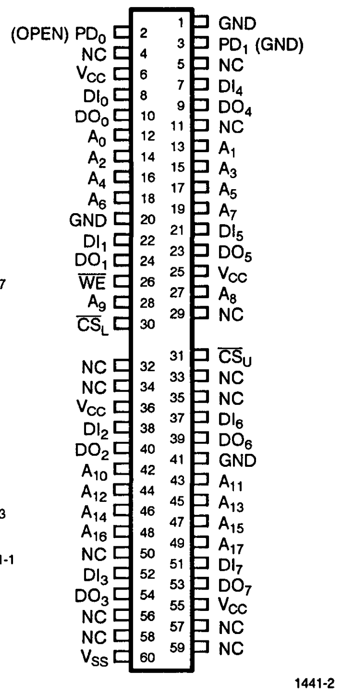
Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) low, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{17}) will appear on the appropriate data output pins (DO_0 through DO_7).

The data output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

	1441PZ-25	1441PZ-35	1441PZ-45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	960	960	960
Maximum Standby Current (mA)	320	320	320

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

CYM1460

512K x 8 Static RAM Module

2

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 35 ns**
- **Low active power**
  - **— 3.4W (max.)**
- **Double-sided SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile version (PF)**
  - **— Max. height of .345 in.**
- **Small footprint SIP version (PS)**
  - **— PCB layout area of 1.2 sq. in.**

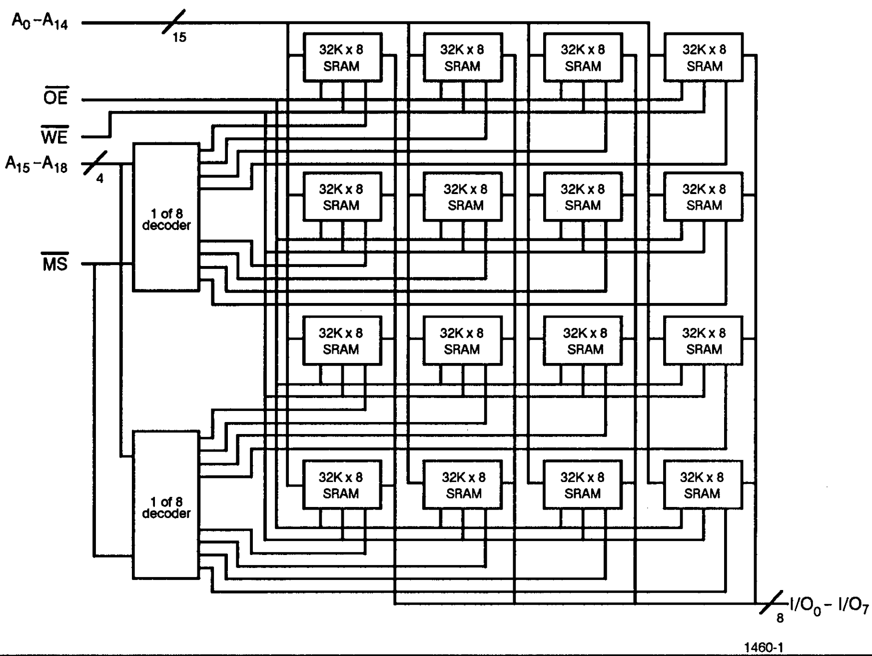
Functional Description

The CYM1460 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed from sixteen 32K x 8 SRAMs in plastic surface mount packages on an epoxy laminate board with pins. Two choices of pins are available for vertical (PS) or horizontal (PF) through-hole mounting. On-board decoding selects one of the sixteen SRAMs from the high-order address lines, keeping the remaining fifteen devices in standby mode for minimum power consumption.

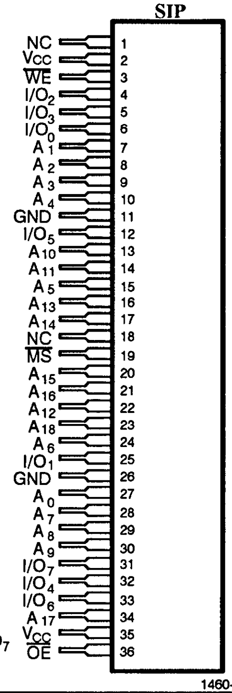
An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{MS}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{MS}$ and $\overline{OE}$, active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

	1460PS-35 1460PF-35	1460PS-45 1460PF-45	1460PS-55 1460PF-55	1460PS-70 1460PF-70
Maximum Access Time (ns)	35	45	55	70
Maximum Operating Current (mA)	625	625	625	625
Maximum Standby Current (mA)	560	560	560	560

this is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYM1461

CYPRESS SEMICONDUCTOR

512K x 8 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 70 ns**
- **Low active power**
  - **825 mW (max.)**
- **Double-sided SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile version (PF)**
  - **Max. height of .315 in.**
- **Small footprint SIP version (PS)**
  - **PCB layout area of 1.5 sq. in.**
- **2V data retention (L version)**

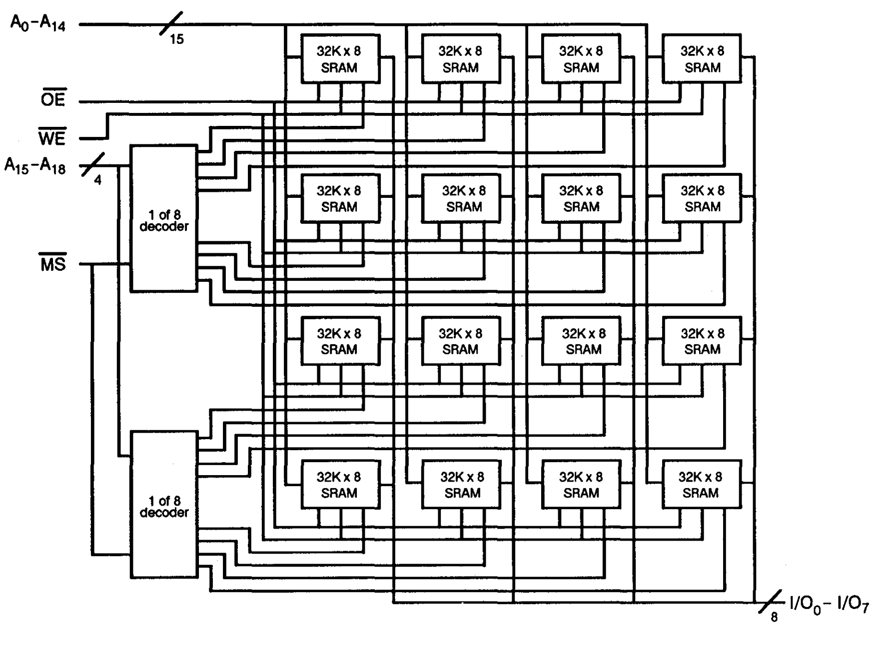
Functional Description

The CYM1461 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed from sixteen 32K x 8 SRAMs in plastic surface mount packages on an epoxy laminate board with pins. Two choices of pins are available for vertical (PS) or horizontal (PF) through-hole mounting. On-board decoding selects one of the sixteen SRAMs from the high-order address lines keeping the remaining fifteen devices in standby mode for minimum power consumption.

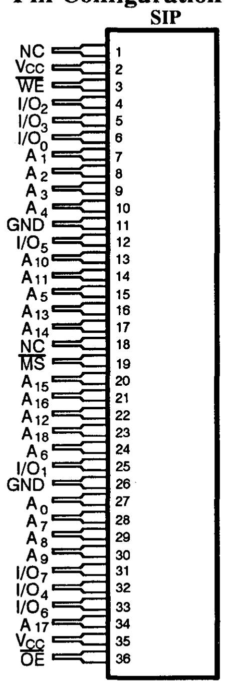
An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{MS}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{MS}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

	1461PS-70 1461PF-70	1461PS-85 1461PF-85	1461PS-100 1461PF-100
Maximum Access Time (ns)	70	85	100
Maximum Operating Current (mA)	150	150	150
Maximum Standby Current (mA)	50	50	50

CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1464**

512K x 8 SRAM Module

2

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 45 ns**
- **Low active power**
  - **— 1.65W (max.)**
- **JEDEC-compatible pinout**
- **32-pin, 0.6-inch-wide DIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .34 in.**
- **Small PCB footprint**
  - **— 0.98 sq. in.**

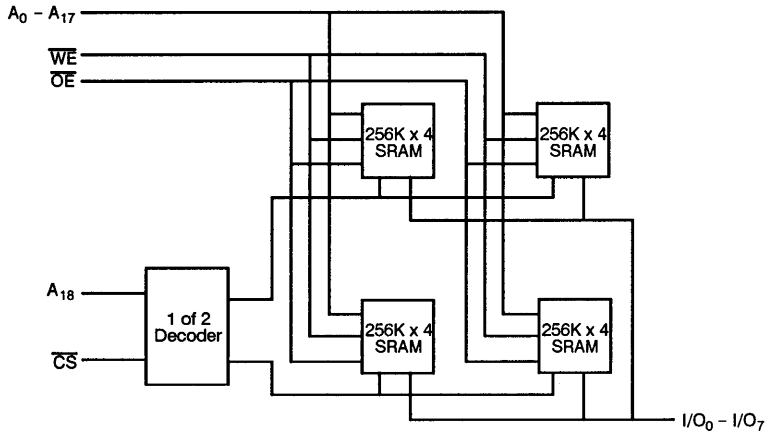
Functional Description

The CYM1464 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 256K x 4 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins. A decoder is used to interpret the higher-order address (A_{18}) and to select two of the four RAMs.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

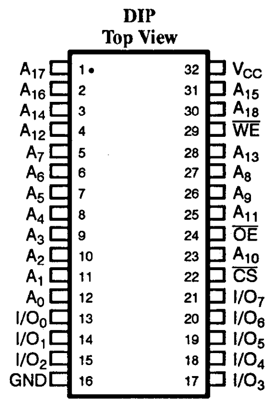
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1464-1

Pin Configuration



1464-2

Selection Guide

	1464PD-45	1464PD-55	1464PD-70
Maximum Access Time (ns)	45	55	70
Maximum Operating Current (mA)	300	300	300
Maximum Standby Current (mA)	240	240	240

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −55°C to +125°C

Ambient Temperature with
Power Applied .... −10°C to +85°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1464PD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]		−0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	−10	10	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	−10	10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		300	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		10	mA

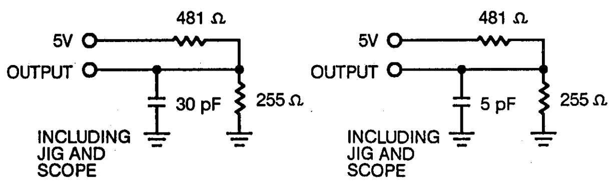
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		30	pF

Note:

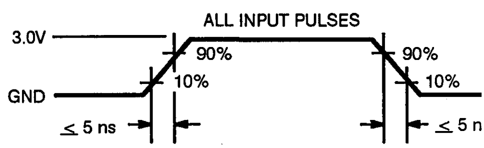
1. $V_{IL(MIN)}$ = −3.0V for pulse widths less than 20 ns.

AC Test Loads and Waveforms



1464-3

(a) (b)



1464-

Switching Characteristics Over the Operating Range [3]

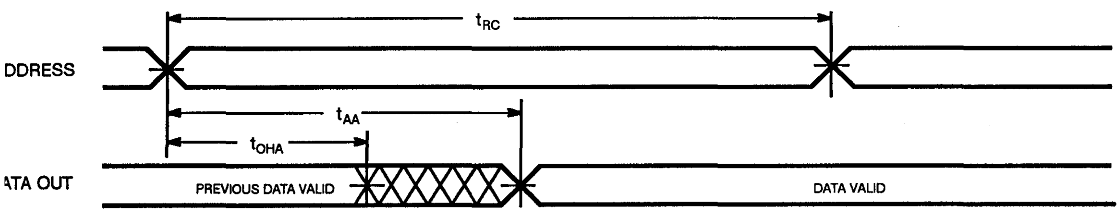
Parameters	Description	1464PD-45		1464PD-55		1464PD-70		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z	0	15	0	15	0	15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]	0	20	0	20	0	20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		45		55		70	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	40		50		60		ns
t_{AW}	Address Set-Up to Write End	40		50		60		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up from Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		40		50		ns
t_{SD}	Data Set-Up to Write End	25		35		45		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [4]		15		20		25	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured +500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{CS}$ transition low.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

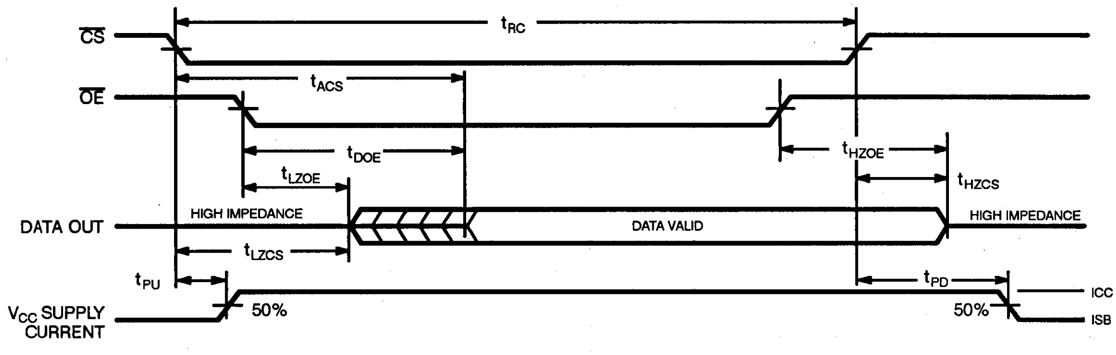
Read Cycle No. 1[6, 7]



1464-5

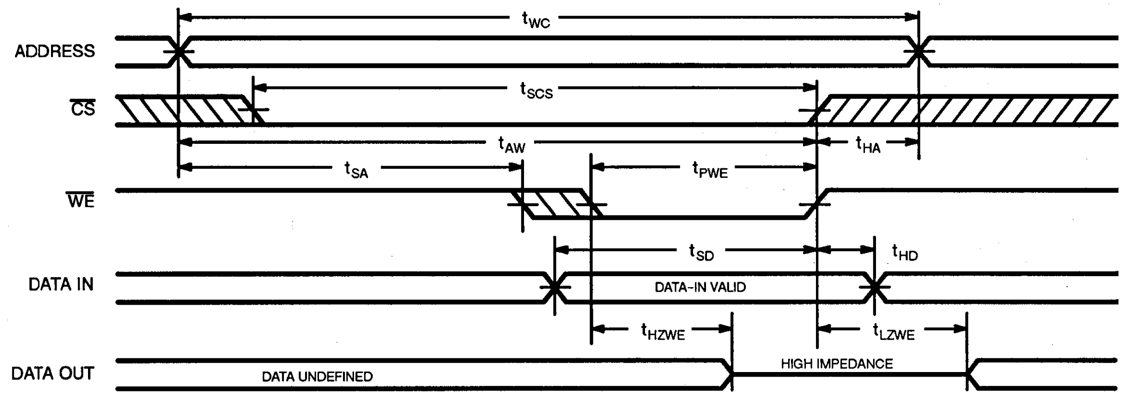
Switching Waveforms (continued)

Read Cycle No. 2 [6, 8]



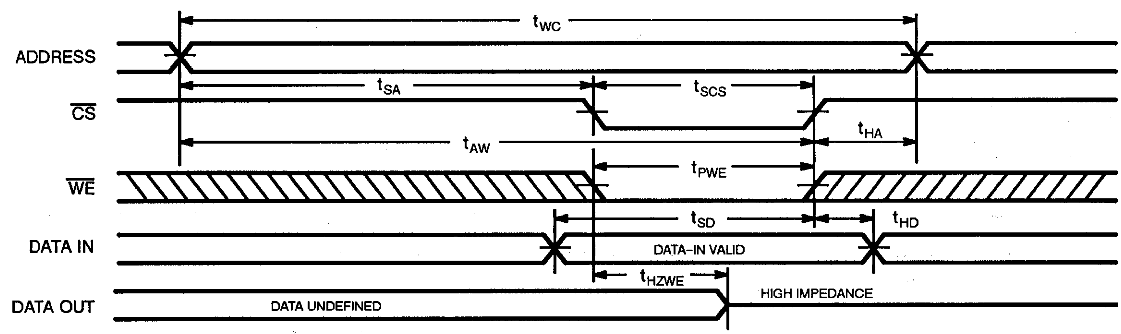
1464-6

Write Cycle No. 1 ($\overline{WE}$ Controlled) [5]



1464-7

Write Cycle No. 2 ($\overline{CS}$ Controlled) [5, 9]



1464-8

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

2

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
45	CYM1464PD-45C	PD02	Commercial
55	CYM1464PD-55C	PD02	Commercial
70	CYM1464PD-70C	PD02	Commercial

Document #: 38-M-00030

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

CYM1540

256K x 9 Buffered SRAM Module with Separate I/O

Features

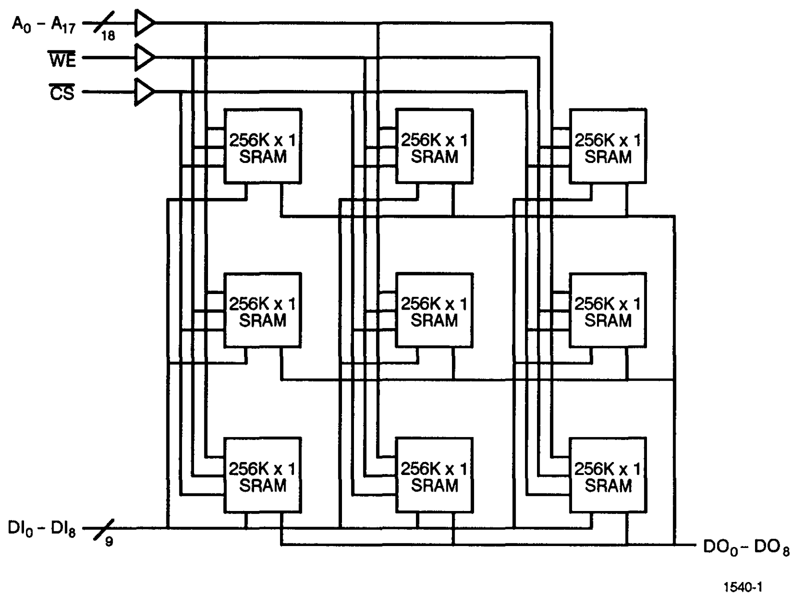
- **High-density 2-megabit SRAM module with parity**
- **High-speed CMOS SRAMs**
  - **Access time of 30 ns**
- **Buffered address and control inputs**
- **Low active power**
  - **6.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .52 in.**
- **Small PCB footprint**
  - **1.6 sq. in.**

Functional Description

The CYM1540 is a very high performance 2-megabit static RAM module organized as 256K words by 9 bits. This module is constructed using nine 256K x 1 static RAMs in SOJ packages mounted on an epoxy laminate board with pins. Input buffers are provided on the address and control lines to reduce input capacitance and loading.

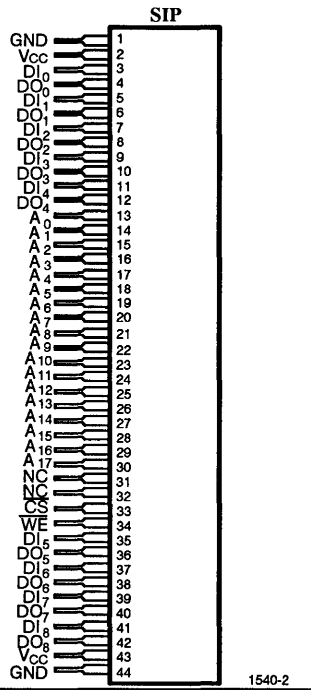
Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the data input pins (DI_0 through DI_8) of the device is written into the memory location specified on the address pins (A_0 through A_{17}). Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{17}) will appear on the appropriate data output pins (DO_0 through DO_8). The data output pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or when write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



1540-1

Pin Configuration



1540-2

Selection Guide

	1540PF-30 1540PS-30	1540PF-35 1540PS-35	1540PF-45 1540PS-45
Maximum Access Time (ns)	30	35	45
Maximum Operating Current (mA)	1125	1125	1125
Maximum Standby Current (mA)	350	350	350

CYPRESS SEMICONDUCTOR

CYM1610

16K x 16 Static RAM Module

Features

- High-density 256-kbit SRAM module
- High-speed CMOS SRAMs
  - Access time of 12 ns
- Low active power
  - 3W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of .215 in.
- Small PCB footprint
  - 1.2 sq. in.
- JEDEC-defined pinout
- Independent byte select
- 2V data retention (L version)

Functional Description

The CYM1610 is a high-performance 256-kbit static RAM module organized as 16K words by 16 bits. This module is constructed from four 16K x 4 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins.

Selecting the device is achieved by a chip select input pin as well as two byte select pins ($\overline{UB}$, $\overline{LB}$) for independently selecting upper or lower byte for read or write operations.

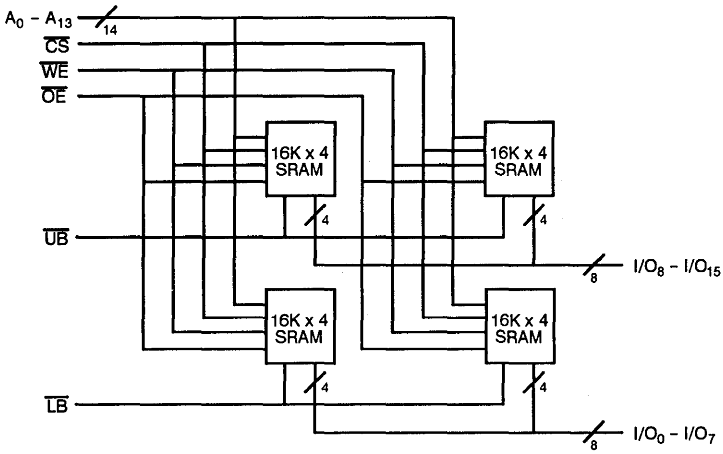
Writing to the memory module is accomplished when the chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and write enable ($\overline{WE}$) inputs are LOW. Data on the input/output pins of the selected byte (I/O_8 – I/O_{15}, I/O_0 – I/O_7) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high-impedance state when chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

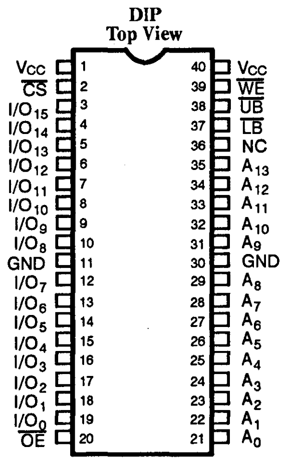
2

Logic Block Diagram



1610-1

Pin Configuration



1610-2

Selection Guide

		1610HD-12	1610HD-15	1610HD-20	1610HD-25	1610HD-35	1610HD-45	1610HD-50
Maximum Access Time (ns)		12	15	20	25	35	45	50
Maximum Operating Current (mA)	Com'l	550	550	330	330	330	330	330
	Mil		550	550	360	330	330	330
Maximum Standby Current (mA)	Com'l	250	250	60	60	60	60	60
	Mil		250	250	60	60	60	60

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... -65°C to +150°C

Ambient Temperature with Power Applied .... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... -0.5V to +7.0V

DC Input Voltage .... -0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	1610HD-12 1610HD-15 1610HD-20M		1610HD-20C 1610HD-25 1610HD-35 1610HD-45 1610HD-50		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	-15	+15	-15	+15	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	-15	+15	-15	+15	μA
I_{OS}	Output Short Circuit Current [1]	V_{CC} = Max., V_{OUT} = GND		-350		-350	mA
I_{CCx16}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$, $\overline{UB}$, & $\overline{LB}$ = V_{IL}		550		330	mA
I_{CCx8}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}		350		200	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		250		60	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} - 0.3V, V_{IN} ≥ V_{CC} - 0.3V or V_{IN} ≤ 0.3V		—		60	mA

Shaded area contains preliminary information.

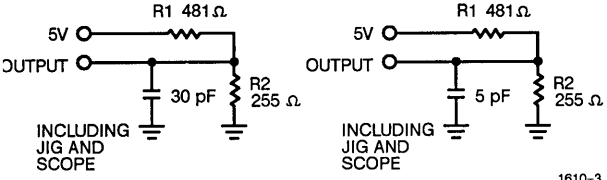
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		25	pF

Notes:

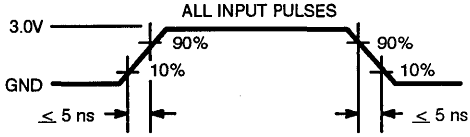
1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the CE input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms



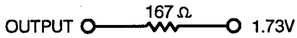
(a) (b)

1610-3



1610-4

Equivalent to: THEVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

Parameters	Description	1610HD-12		1610HD-15		1610HD-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		2		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		8		8		8	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE [7]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Set-Up to Write End	10		12		15		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	7	0	7	0	7	ns

Shaded area contains preliminary information.

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Characteristics Over the Operating Range (continued) [4]

Parameters	Description	1610HD-25		1610HD-35		1610HD-45		1610HD-50		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		50		ns
t_{AA}	Address to Data Valid		25		35		45		50	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45		50	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		15		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		10		15		15		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		40		50	ns
WRITE CYCLE [7]										
t_{WC}	Write Cycle Time	25		35		45		50		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	22		25		35		45		ns
t_{AW}	Address Set-Up to Write End	22		25		30		40		ns
t_{HA}	Address Hold from Write End	3		3		3		3		ns
t_{SA}	Address Set-Up to Write Start	4		4		4		4		ns
t_{PWE}	$\overline{WE}$ Pulse Width	18		25		30		30		ns
t_{SD}	Data Set-Up to Write End	13		15		15		20		ns
t_{HD}	Data Hold from Write End	3		5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]	0	7	0	12	0	12	0	15	ns

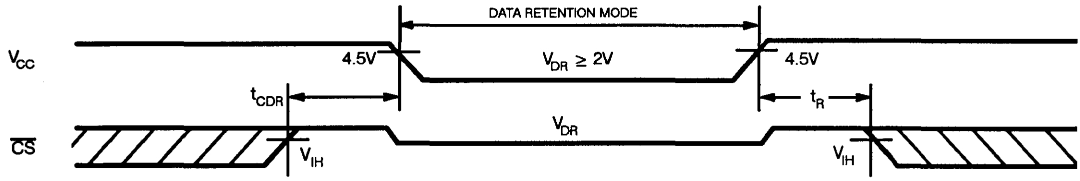
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1610		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			4	mA
t_{CDR} [14]	Chip Deselect to Data Retention Time		0		ns
t_R [14]	Operation Recovery Time		t_{RC} [13]		ns
I_{LI} [14]	Input Leakage Current			8	μA

Notes:

13. t_{RC} = Read Cycle Time.
14. Guaranteed, not tested.

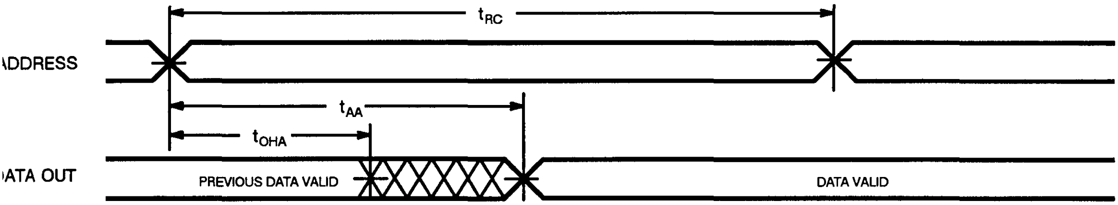
Data Retention Waveform



1610-5

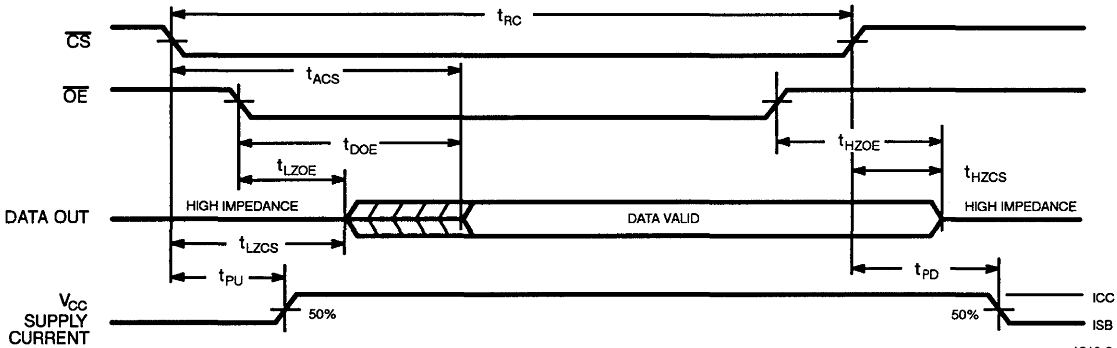
Switching Waveforms [10]

Read Cycle No. 1 [7, 8]



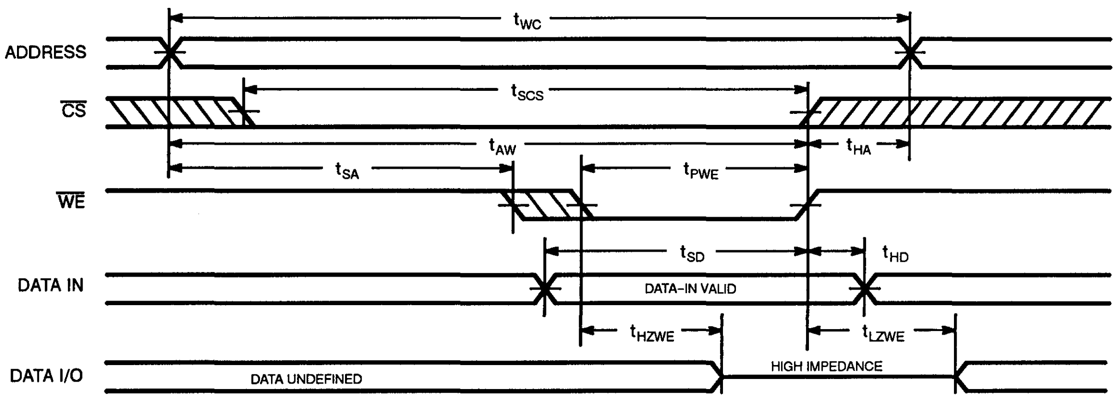
1610-6

Read Cycle No. 2 [8, 10]



1610-8

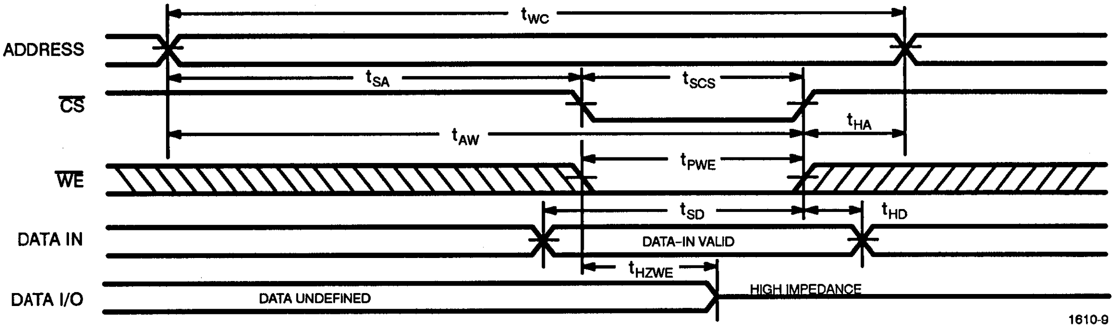
Write Cycle No. 1 (WE Controlled) [7, 11]



1610-7

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 11, 12]



1610-9

Truth Table

$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Input/Outputs	Mode
H	X	X	X	X	High Z	Deselect/Power-Down
L	H	H	X	X	High Z	Deselect/Power-Down
L	L	L	L	H	Data Out_{0-15}	Read Word
L	H	L	L	H	Data Out_{0-7}	Read Lower Byte
L	L	H	L	H	Data Out_{8-15}	Read Upper Byte
L	L	L	X	L	Data In_{0-15}	Write Word
L	H	L	X	L	Data In_{0-7}	Write Lower Byte
L	L	H	X	L	Data In_{8-15}	Write Upper Byte
L	L	L	H	H	High Z	Deselect
L	H	L	H	H	High Z	Deselect
L	L	H	H	H	High Z	Deselect

Document #: 38-M-00006-A

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
12	CYM1610HD-12C	HD01	Commercial
15	CYM1610HD-15C	HD01	Commercial
	CYM1610HD-15MB	HD01	Military
20	CYM1610HD-20C	HD01	Commercial
	CYM1610LHD-20C	HD01	
	CYM1610HD-20MB	HD01	Military
25	CYM1610HD-25C	HD01	Commercial
	CYM1610LHD-25C	HD01	
	CYM1610HD-25MB	HD01	Military
	CYM1610LHD-25MB	HD01	
35	CYM1610HD-35C	HD01	Commercial
	CYM1610LHD-35C	HD01	
	CYM1610HD-35MB	HD01	Military
	CYM1610LHD-35MB	HD01	
45	CYM1610HD-45C	HD01	Commercial
	CYM1610LHD-45C	HD01	
	CYM1610HD-45MB	HD01	Military
	CYM1610LHD-45MB	HD01	
50	CYM1610HD-50C	HD01	Commercial
	CYM1610LHD-50C	HD01	
	CYM1610HD-50MB	HD01	Military
	CYM1610LHD-50MB	HD01	

Shaded area contains preliminary information.

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

CYM1611

16K x 16 Static RAM Module

Features

- **High-density 256-kbit SRAM module**
- **High speed**
  - **— Access time of 12 ns**
- **16-bit-wide organization**
- **Low active power**
  - **— 1.8W (max.) at 25 ns**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of 0.5 in.**
- **Small PCB footprint**
  - **— 0.4 sq. in.**
- **2V data retention (L version)**

Functional Description

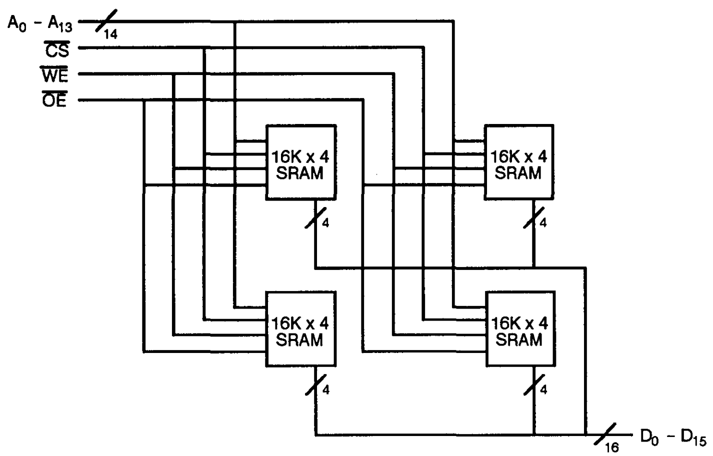
The CYM1611 is a very high performance 256-kbit static RAM module organized as 16K words by 16 bits. The module is constructed from four 16K x 4 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. A vertical DIP format minimizes board space (footprint = 0.4 sq. in.) while still keeping a maximum height of 0.5 in.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (D_0 through D_{15}) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the sixteen data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

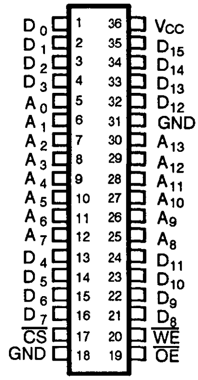
Logic Block Diagram



1611-1

Pin Configuration

VDIP
Top View



1611-2

Selection Guide

		1611HV-12	1611HV-15	1611HV-20	1611HV-25	1611HV-30	1611HV-35	1611HV-45
Maximum Access Time (ns)		12	15	20	25	30	35	45
Maximum Operating Current (mA)	Commercial	550	550	330	330	330	330	330
	Military		550	550	330	330	330	330
Maximum Standby Current (mA)	Commercial	250	250	80	80	80	80	80
	Military		250	250	80	80	80	80

Shaded area contains preliminary information.

CYPRESS SEMICONDUCTOR

64K x 16 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 30 ns**
- **40-pin, 0.6-inch-wide DIP package**
- **JEDEC-compatible pinout**
- **Low active power**
  - **— 1.9W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial and military temperature ranges**

Functional Description

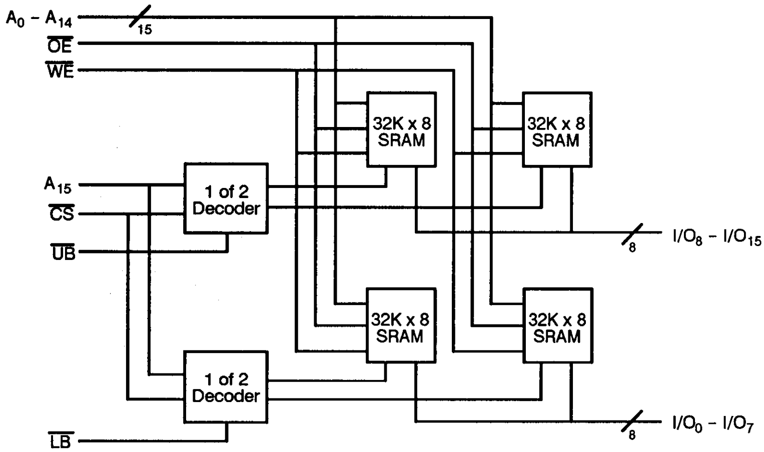
The CYM1620 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 32K x 8 static RAMs in leadless chip carriers mounted onto a double-sided multilayer ceramic substrate. A decoder is used to interpret the higher-order address A_{15} and select one of the two pairs of RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins of the selected byte (I/O_8 - I/O_{15}, I/O_0 - I/O_7) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

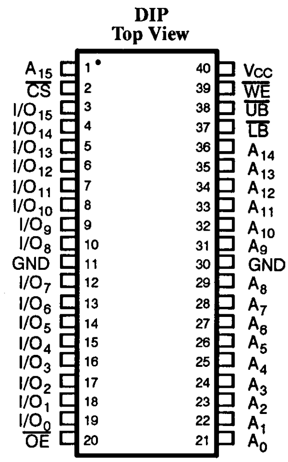
The input/output pins remain in a high-impedance state when chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



1620-1

Pin Configuration



1620-2

Selection Guide

		1620HD-30	1620HD-35	1620HD-45	1620HD-55
Maximum Access Time (ns)		30	35	45	55
Maximum Operating Current (mA)	Commercial	340	340	340	340
	Military			340	340
Maximum Standby Current (mA)	Commercial	140	140	140	140
	Military			140	140

Maximum Ratings

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied .... –55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	–55°C to +125°C	5V ± 10%

2

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1620HD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		–0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–15	+15	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	–15	+15	µA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		–300	mA
I_{CCx16}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$, $\overline{UB}$, & $\overline{LB}$ = V_{IL}		340	mA
I_{CCx8}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}		200	mA
I_{SB1}	Automatic $\overline{CS}$[2] Power Down Current	Max. V_{CC} $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		140	mA
I_{SB2}	Automatic $\overline{CS}$[2] Power Down Current	Max. V_{CC}, $\overline{CS} \geq V_{CC}$ – 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq$ 0.3V		80	mA

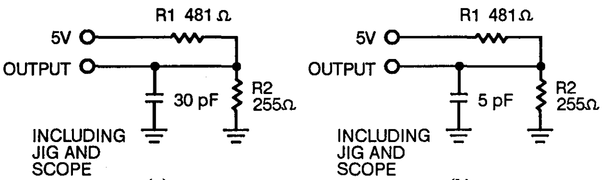
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz,	35	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0V	40	pF

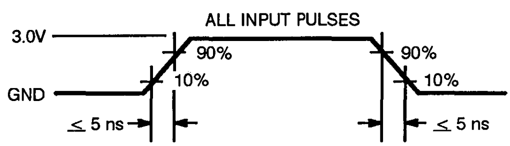
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

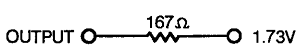


1620-3



1620-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

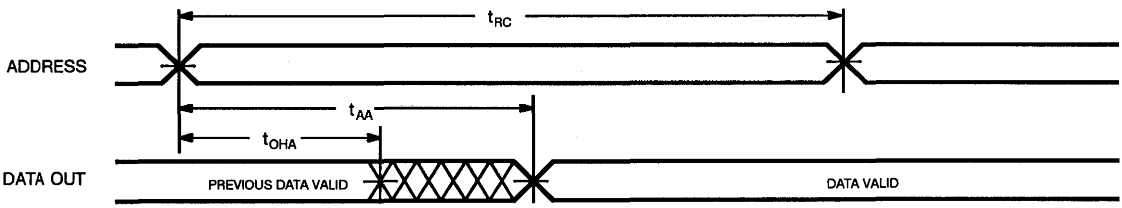
Parameters	Description	1620HD-30		1620HD-35		1620HD-45		1620HD-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	30		35		45		55		ns
t_{AA}	Address to Data Valid		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		18		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		20		20		25	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		20		20		20		25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		30		35		45		55	ns
WRITE CYCLE[7]										
t_{WC}	Write Cycle Time	30		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	25		30		40		45		ns
t_{AW}	Address Set-Up to Write End	25		30		40		45		ns
t_{HA}	Address Hold from Write End	5		5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		25		25		30		ns
t_{SD}	Data Set-Up to Write End	18		18		20		25		ns
t_{HD}	Data Hold from Write End	3		3		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]	0	15	0	15	0	15	0	25	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.

Switching Waveforms [10]

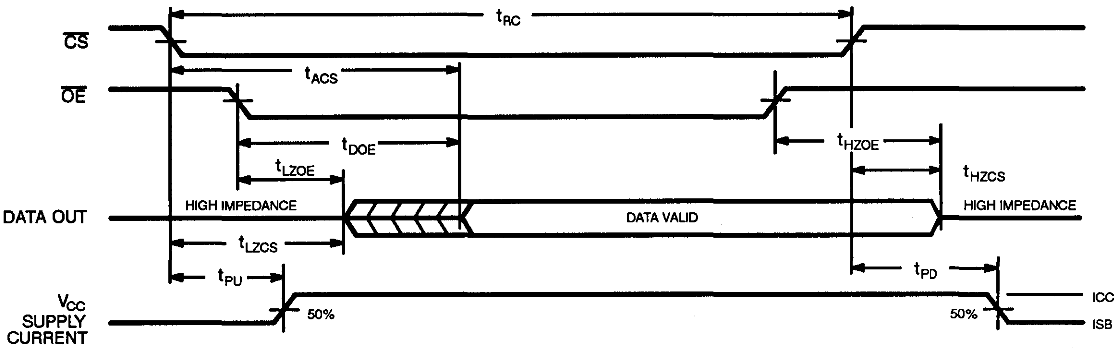
Read Cycle No. 1[8, 9]



1620-

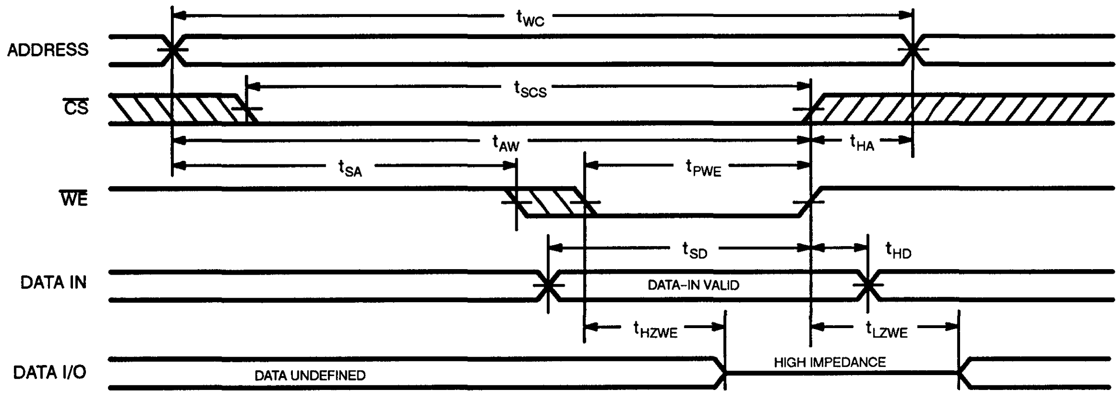
Switching Waveforms (continued)

Read Cycle No. 2 [8, 10]



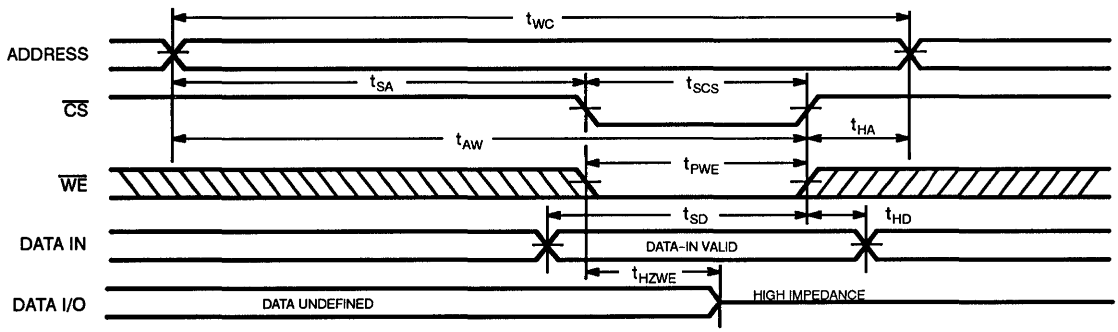
1620-6

Write Cycle No. 1 (WE Controlled) [7, 11]



1620-7

Write Cycle No. 2 (CS Controlled) [7, 11, 12]



1620-8

Truth Table

$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Input/Outputs	Mode
H	X	X	X	X	High Z	Deselect/Power-Down
L	H	H	X	X	High Z	Deselect/Power-Down
L	L	L	L	H	Data Out_{0-15}	Read
L	H	L	L	H	Data Out_{0-7}	Read Lower Byte
L	L	H	L	H	Data Out_{8-15}	Read Upper Byte
L	L	L	X	L	Data In_{0-15}	Write
L	H	L	X	L	Data In_{0-7}	Write Lower Byte
L	L	H	X	L	Data In_{8-15}	Write Upper Byte
L	L	L	H	H	High Z	Deselect
L	H	L	H	H	High Z	Deselect
L	L	H	H	H	High Z	Deselect

Document #: 38-M-00008-A

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
30	CYM1620HD-30C	HD03	Commercial
35	CYM1620HD-35C	HD03	Commercial
45	CYM1620HD-45C	HD03	Commercial
	CYM1620HD-45MB	HD03	Military
55	CYM1620HD-55C	HD03	Commercial
	CYM1620HD-55MB	HD03	Military

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYM1621

CYPRESS SEMICONDUCTOR

64K x 16 Static RAM Module

2

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Customer configurable**
  - **x4, x8, x16**
- **Low active power**
  - **6.8W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .270 in.**
- **Small PCB footprint**
  - **2 sq. in.**
- **2V data retention (L version)**

Functional Description

The CYM1621 is a high-performance 1-megabit static RAM module organized as 64K words by 16 bits. This module is constructed from sixteen 64K x 1 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. Four separate $\overline{CS}$ pins are used to control each 4-bit nibble of the 16-bit word. This feature permits the user to configure this module as either 256K x 4, 128K x 8 or 64K x 16 organization through external decoding and appropriate pairing of the outputs.

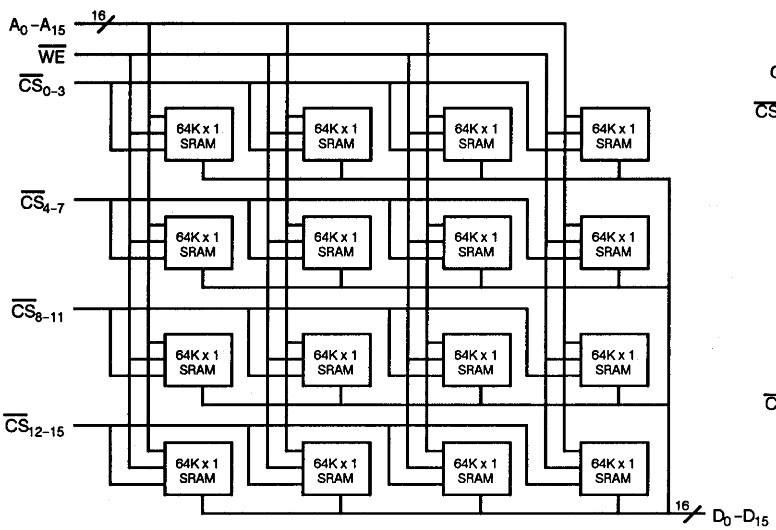
Writing to the device is accomplished when the chip select ($\overline{CS}_{XX}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the data lines (D_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip select ($\overline{CS}_{XX}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data lines (D_X).

The data output is in the high-impedance state when chip enable ($\overline{CS}_{XX}$) is HIGH or write enable ($\overline{WE}$) is LOW.

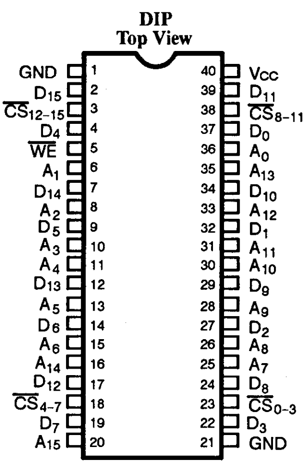
Power is consumed in each 4-bit nibble only when the appropriate $\overline{CS}$ is enabled, thus reducing power in the x4 or x8 mode.

Logic Block Diagram



1621-1

Pin Configuration



1621-2

Selection Guide

		1621HD-20	1621HD-25	1621HD-30	1621HD-35	1621HD-45
Maximum Access Time (ns)		20	25	30	35	45
Maximum Operating Current (mA)	Commercial	1250	1250	1250	1250	1250
	Military		1250	1250	1250	1250
Maximum Standby Current (mA)	Commercial	320	320	320	320	320
	Military		320	320	320	320

64K x 16 SRAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **2.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Pinout-compatible with CYM1611 and CYM1624**
- **Low profile**
  - **Max. height of .50 in.**
- **Small PCB footprint**
  - **0.5 sq. in.**

Functional Description

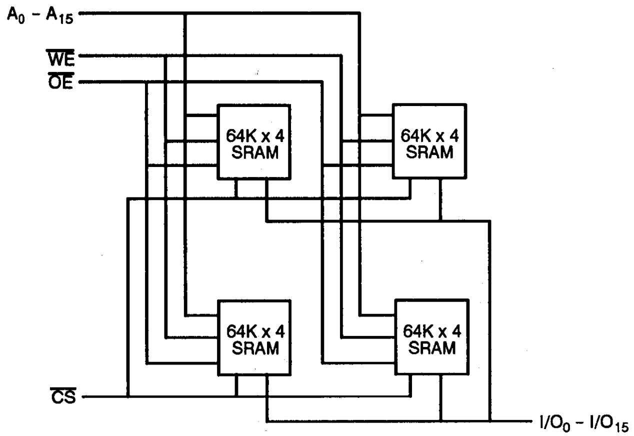
The CYM1622 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. This module is constructed using four 64K x 4 static RAMs in LCC packages mounted on a ceramic substrate with pins. The pinout of this module is compatible with two other Cypress modules (CYM1611 and CYM1624) to maximize system flexibility.

Writing to the module is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (I/O_0 through I/O_{15}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable $\overline{OE}$) low, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{15}) will appear on the appropriate data input/output pins (I/O_0 through I/O_{15}).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

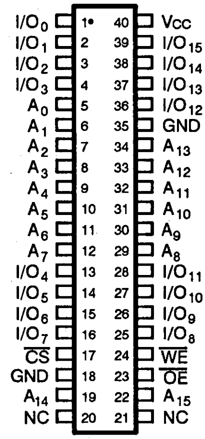
Logic Block Diagram



1622-1

Pin Configuration

Plastic VDIP
Top View



1622-2

Selection Guide

	1622HV-25	1622HV-35	1622HV-45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	400	400	400
Maximum Standby Current (mA)	140	140	140

CYM1623

CYPRESS SEMICONDUCTOR

64K x 16 Static RAM Module

Features

- High-density 1-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 70 ns
- 40-pin, 0.6-in.-wide DIP package
- JEDEC-compatible pin-out
- Low active power
  - 1.3W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- 2V data retention (L version)

Functional Description

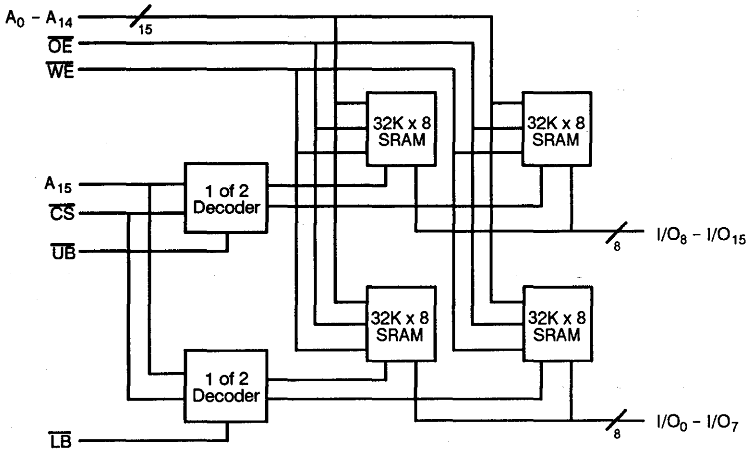
The CYM1623 is a high-performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 32K x 8 static RAMs in leadless chip carriers mounted onto a double-sided multilayer ceramic substrate. A decoder is used to interpret the higher-order address A_{15} and to select one of the two pairs of RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins of the selected byte ($I/O_8 - I/O_{15}$, $I/O_0 - I/O_7$) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

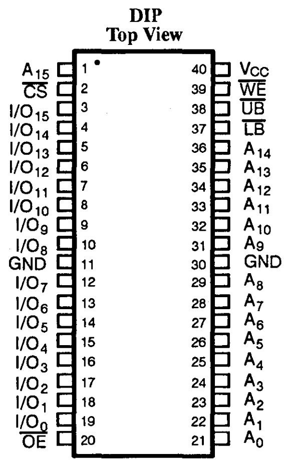
The input/output pins remain in a high-impedance state when chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



1623-1

Pin Configuration



1623-2

Selection Guide

		1623HD-70	1623HD-85	1623HD-100
Maximum Access Time (ns)		70	85	100
Maximum Operating Current (mA)	Commercial	240	240	240
Maximum Standby Current (mA)	Commercial	70	70	70

Maximum Ratings

(Above which the useful life may be impaired.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −10°C to +70°C

Supply Voltage to Ground Potential .... −0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.3V to +7.0V

DC Input Voltage .... −0.3V to +7.0V

Output Current into Outputs (Low) .... 50 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1623HD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −1.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	μA
I_{CCx16}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$, $\overline{UB}$, & $\overline{LB}$ = V_{IL}		240	mA
I_{CCx8}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}		120	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		70	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		20	mA

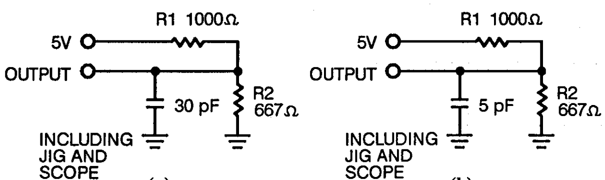
Capacitance [3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		40	pF

Notes:

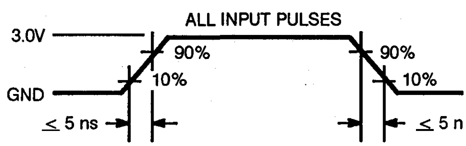
1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms



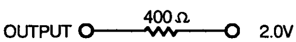
(a) (b)

1623-5



1623-6

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

Parameters	Description	1623HD-70		1623HD-85		1623HD-100		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	70		85		100		ns
t_{AA}	Address to Data Valid		70		85		100	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		70		85		100	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		40		50		60	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		35		35		40	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		35		35		40	ns
WRITE CYCLE [7]								
t_{WC}	Write Cycle Time	70		85		100		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	65		75		90		ns
t_{AW}	Address Set-Up to Write End	65		75		90		ns
t_{HA}	Address Hold from Write End	10		15		15		ns
t_{SA}	Address Set-Up to Write Start	25		25		30		ns
t_{PWE}	$\overline{WE}$ Pulse Width	60		70		80		ns
t_{SD}	Data Set-Up to Write End	30		35		35		ns
t_{HD}	Data Hold from Write End	10		10		15		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]	0	30	0	35	0	40	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.

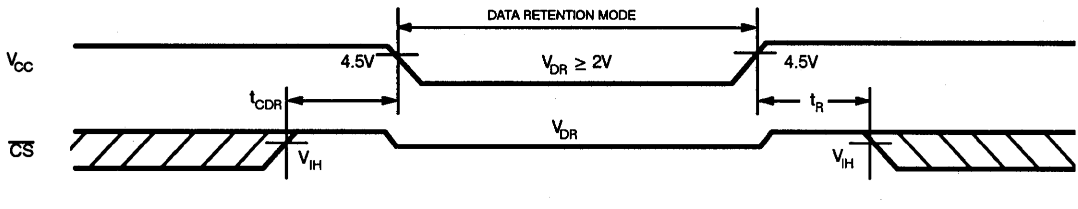
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1623 Min.	CYM1623 Max.	Units
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			250	mA
t_{CDR} [13]	Chip Deselect to Data Retention Time		0		ns
t_R [13]	Operation Recovery Time		t_{RC} [12]		ns

Notes:

12. t_{RC} = Read Cycle Time.
13. Guaranteed, not tested.
14. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

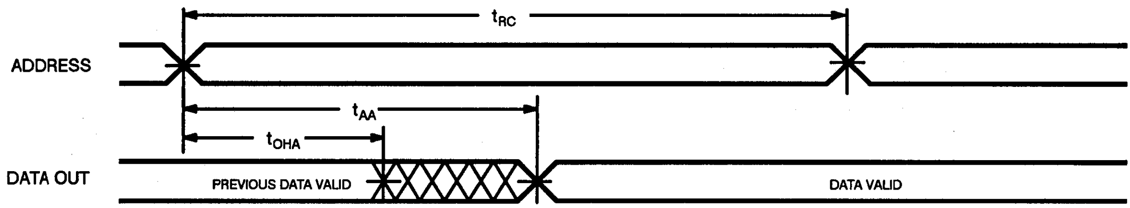
Data Retention Waveform



1623-7

Switching Waveforms [10]

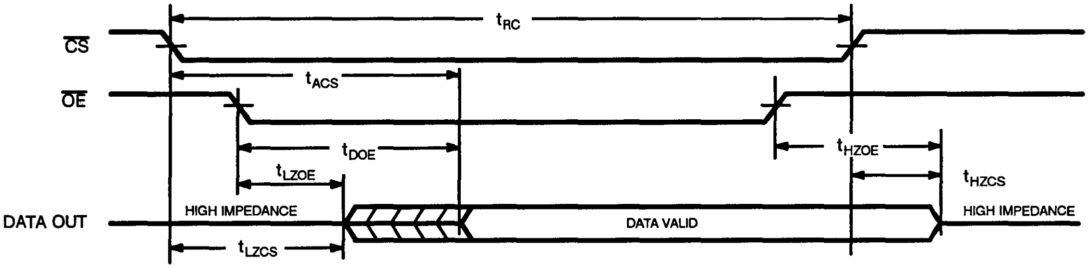
Read Cycle No. 1[8, 9]



1623-8

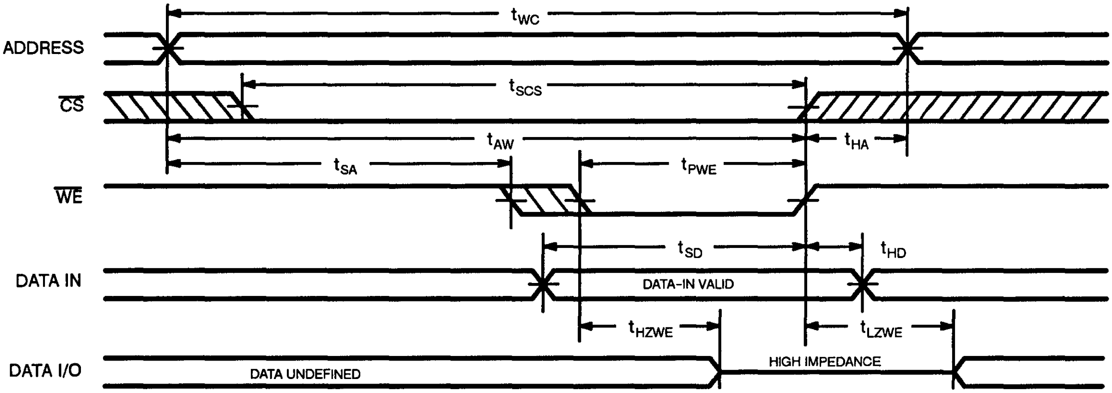
Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



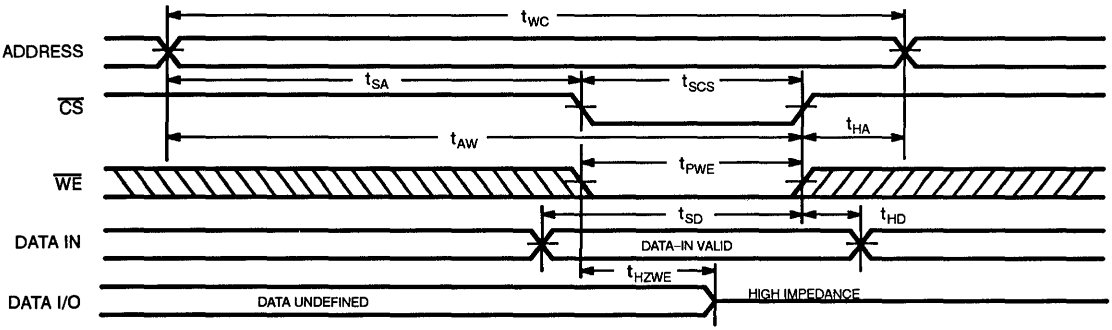
1623-9

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)[7, 11]



1623-10

Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled)[7, 11, 14]



1623-11

2

Truth Table

$\overline{CS}$	$\overline{UB}$	$\overline{LB}$	$\overline{OE}$	$\overline{WE}$	Input/Outputs	Mode
H	X	X	X	X	High Z	Deselect/Power-Down
L	H	H	X	X	High Z	Deselect/Power-Down
L	L	L	L	H	Data Out_{0-15}	Read
L	H	L	L	H	Data Out_{0-7}	Read Lower Byte
L	L	H	L	H	Data Out_{8-15}	Read Upper Byte
L	L	L	X	L	Data In_{0-15}	Write
L	H	L	X	L	Data In_{0-7}	Write Lower Byte
L	L	H	X	L	Data In_{8-15}	Write Upper Byte
L	L	L	H	H	High Z	Deselect
L	H	L	H	H	High Z	Deselect
L	L	H	H	H	High Z	Deselect

Document #: 38-M-00011-A

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
70	CYM1623HD-70C	HD03	Commercial
	CYM1623LHD-70C	HD03	
85	CYM1623HD-85C	HD03	Commercial
	CYM1623LHD-85C	HD03	
100	CYM1623HD-100C	HD03	Commercial
	CYM1623LHD-100C	HD03	

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYM1624

CYPRESS SEMICONDUCTOR

64K x 16 SRAM Module

2

Features

- High-density 1-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 25 ns
- Low active power
  - 2.75W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Pin layout compatible with CYM1611 and CYM1622
- Low profile
  - Max. height of .54 in.
- Small PCB footprint
  - 0.7 sq. in.

Functional Description

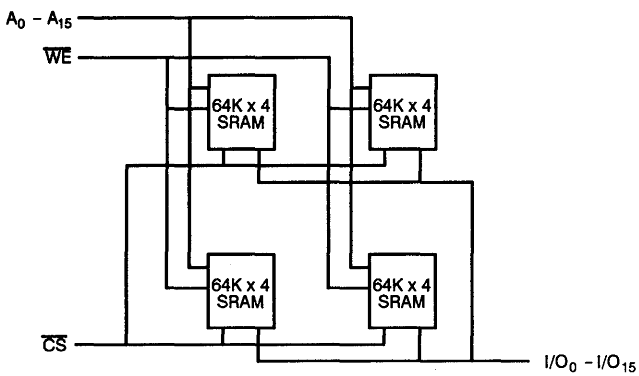
The CYM1624 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. This module is constructed using four 64K x 4 static RAMs in SOJ packages mounted on an epoxy laminate board with pins. The pinout of this module is compatible with two other Cypress modules (CYM1611 and CYM1622) to maximize system flexibility.

Writing to the module is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (I/O_0 through I/O_{15}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{15}) will appear on the appropriate data input/output pins (I/O_0 through I/O_{15}).

The data input/output pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or when write enable ($\overline{WE}$) is LOW.

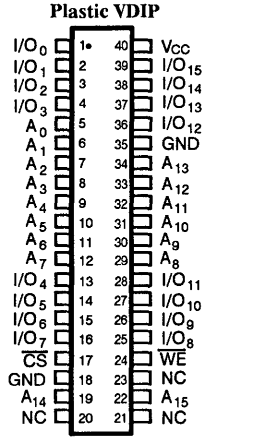
Logic Block Diagram



1624-1

Pin Configuration

Plastic VDIP



1624-2

Selection Guide

	1624PV-25	1624PV-35	1624PV-45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	500	500	500
Maximum Standby Current (mA)	160	160	160

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

CYM1641

256K x 16 Static RAM Module

Features

- High-density 4-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 25 ns
- Customer configurable
  - x4, x8, x16
- Low active power
  - 10W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of .300 in.
- Small PCB footprint
  - 2.2 sq. in.

Functional Description

The CYM1641 is a high-performance 4-megabit static RAM module organized as 256K words by 16 bits. This module is constructed from sixteen 256K x 1 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. Four separate $\overline{CS}$ pins are used to control each 4-bit nibble of the 16-bit word. This feature permits the user to configure this module as either 1M x 4, 512K x 8 or 256K x 16 organization through external decoding and appropriate pairing of the outputs.

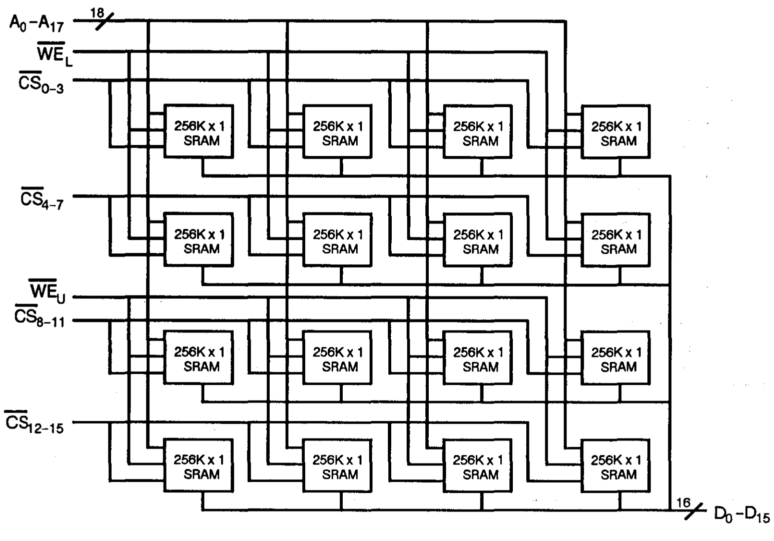
Writing to the device is accomplished when the chip select ($\overline{CS}_{xx}$) and write enable ($\overline{WE}_{U,L}$) inputs are both LOW. Data on the data lines (D_X) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip select ($\overline{CS}_{xx}$) LOW, while write enable ($\overline{WE}_{U,L}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data lines (D_X).

The data output is in the high-impedance state when chip enable ($\overline{CS}_{xx}$) is HIGH or write enable ($\overline{WE}_{U,L}$) is LOW.

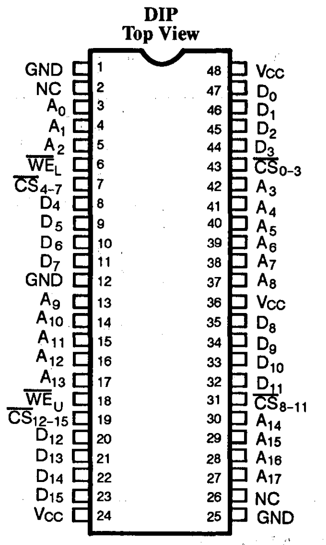
Power is consumed in each 4-bit nibble only when the appropriate $\overline{CS}$ is enabled, thus reducing power in the x4 or x8 mode.

Logic Block Diagram



1641-1

Pin Configuration



1641-2

Selection Guide

		1641HD-25	1641HD-35	1641HD-45	1641HD-55
Maximum Access Time (ns)		25	35	45	55
Maximum Operating Current (mA)	Commercial	1800	1800	1800	1800
	Military		1800	1800	1800
Maximum Standby Current (mA)	Commercial	560	560	560	560
	Military		560	560	560

32K x 24 SRAM Module

Features

- **High-density 768-kbit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **56-pin, 0.5-inch-high ZIP package**
- **Low active power**
  - **1.8W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial temperature range**
- **Small PCB footprint**
  - **0.66 sq. in.**

Functional Description

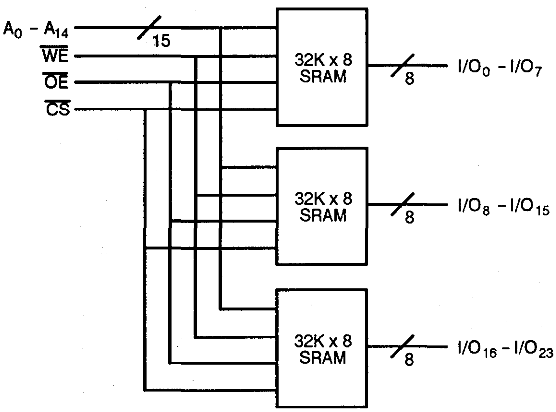
The CYM1720 is a high-performance 768-kbit static RAM module organized as 32K words by 24 bits. This module is constructed using three 32K x 8 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_0 through I/O_{23}) of the device is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{14}) will appear on the input/output pins (I/O_0 through I/O_{23}).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

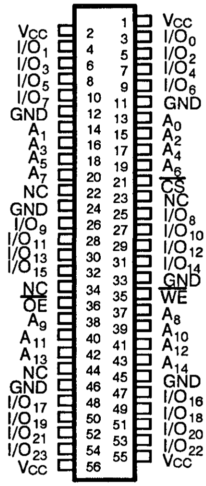
Logic Block Diagram



1720-1

Pin Configuration

ZIP
Top View



1720-2

Selection Guide

	1720PZ-25	1720PZ-30	1720PZ-35
Maximum Access Time (ns)	25	30	35
Maximum Operating Current (mA)	330	330	330
Maximum Standby Current (mA)	60	60	60

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

CYM1821

16K x 32 Static RAM Module

Features

- High-density 512-kbit SRAM module
- High-speed CMOS SRAMs
  - Access time of 12 ns
- Low active power – 4W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of .50 in.
- Small PCB footprint
  - 1.0 sq. in.
- JEDEC-compatible pinout
- 2V data retention (L version)

Functional Description

The CYM1821 is a high-performance 512-kbit static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 SRAM SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$ and $\overline{CS_4}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

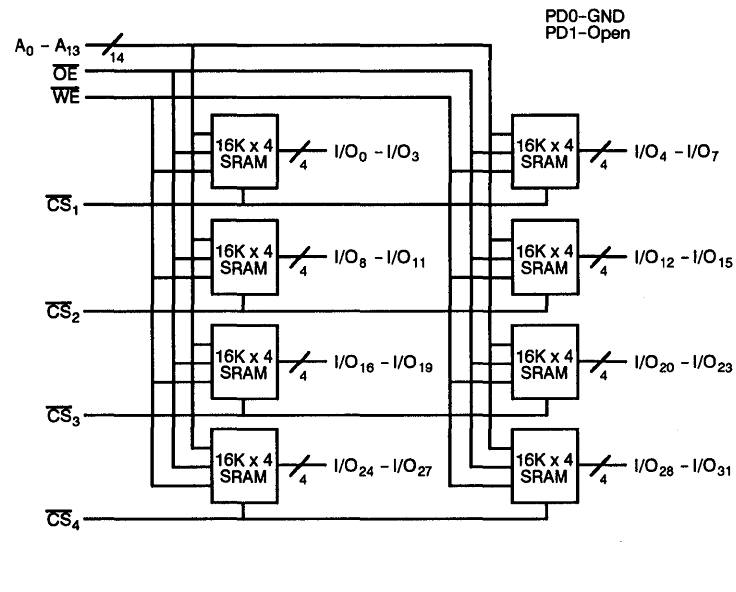
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS_N}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip selects ($\overline{CS_N}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

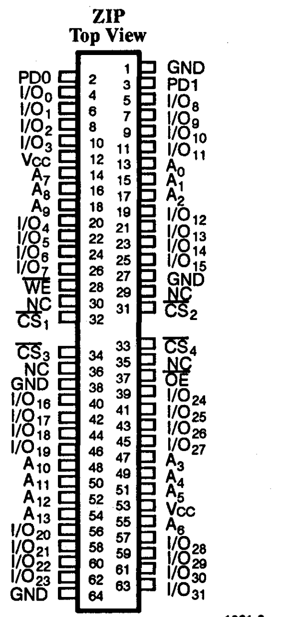
Two pins (PD0 and PD1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

Logic Block Diagram



1821-1

Pin Configuration



1821-2

Selection Guide

	1821PZ-12	1821PZ-15	1821PZ-20	1821PZ-25	1821PZ-35	1821PZ-45
Maximum Access Time (ns)	12	15	20	25	35	45
Maximum Operating Current (mA)	960	960	720	720	720	720
Maximum Standby Current (mA)	450	450	160	160	160	160

Shaded area contains preliminary information.

16K x 32 Static RAM Module with Separate I/O

eatures

- High-density 512K-bit SRAM module
- High-speed CMOS SRAMs
  - — Access time of 12 ns
- Low active power
  - — 5.3W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - — Max. height of .52 in.
- Small PCB footprint
  - — 1.0 sq. in.
- 2V data retention (L version)

Functional Description

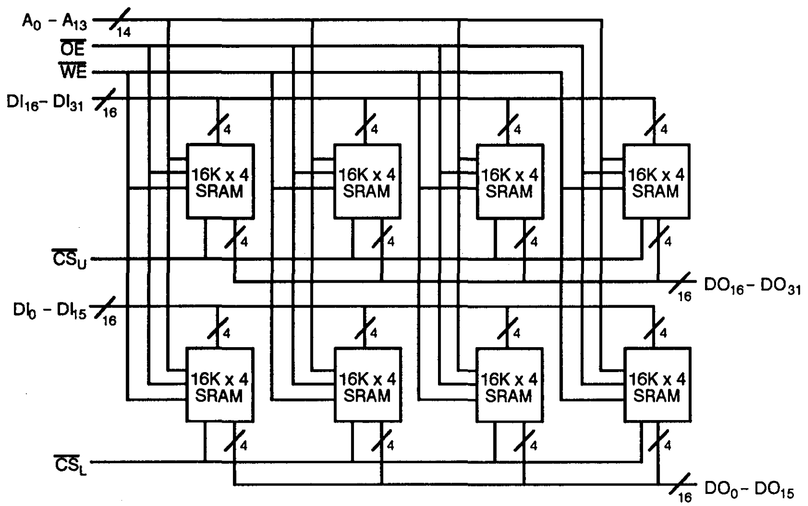
The CYM1822 is a high-performance 512-kbit static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 separate I/O SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. Two chip selects ($\overline{CS}_U$ and $\overline{CS}_L$) are used to independently enable the upper and lower 16-bit data words.

Writing to the device is accomplished when the chip selects ($\overline{CS}_U$ and/or $\overline{CS}_L$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pins (DI_X) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_U$ and/or $\overline{CS}_L$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output pins (DO_X).

The output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, the appropriate chip selects are HIGH, or $\overline{OE}$ is HIGH.

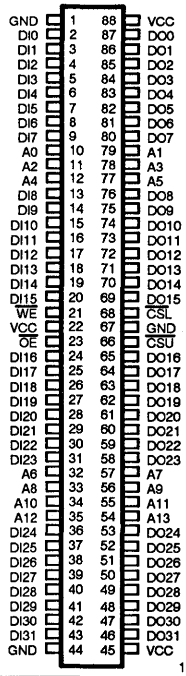
Logic Block Diagram



1822-1

Pin Configuration

VDIP



1822-2

election Guide

		1822HV-12	1822HV-15	1822HV-20	1822HV-25	1822HV-30	1822HV-35	1822HV-45
Maximum Access Time (ns)		12	15	20	25	30	35	45
Maximum Operating Current (mA)	Commercial	960	960	720	720	720	720	720
	Military		960	960	720	720	720	720
Maximum Standby Current (mA)	Commercial	450	450	160	160	160	160	160
	Military		450	450	160	160	160	160

haded area contains preliminary information.

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

CYM1830

64K x 32 Static RAM Module

Features

- High-density 2-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 25 ns
- Independent byte and word controls
- Low active power
  - 4.8W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of .270 in.
- Small PCB footprint
  - 1.8 sq. in.

Functional Description

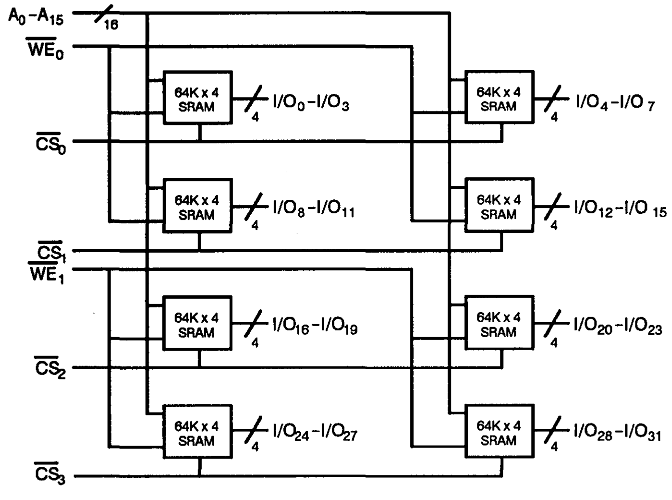
The CYM1830 is a high-performance 2-megabit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in LCC packages mounted on a ceramic substrate with pins. Four chip selects ($\overline{CS_0}$ $\overline{CS_1}$, $\overline{CS_2}$ and $\overline{CS_3}$) are used to independently enable the four bytes. Two write enables ($\overline{WE_0}$ and $\overline{WE_1}$) are used to independently write to either upper or lower 16-bit word of RAM. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects and write enables.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS_X}$) and write enable ($\overline{WE_X}$) inputs are both LOW. Data on the input/output pins ($\overline{I/O_X}$) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects ($\overline{CS_X}$) LOW, while write enables($\overline{WE_X}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ($\overline{I/O_X}$).

The Data input/output pins stay in the high-impedance state when write enables ($\overline{WE_X}$) are LOW, or the appropriate chip selects are HIGH.

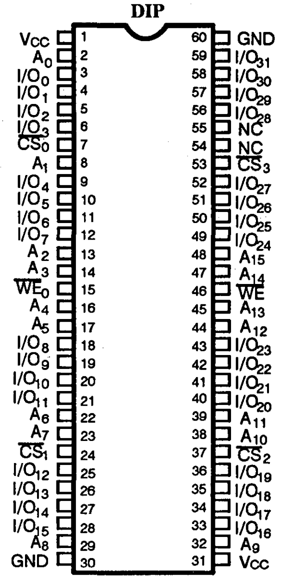
Logic Block Diagram



1830-1

Pin Configuration

DIP



1830-2

Selection Guide

		1830HD-25	1830HD-30	1830HD-35	1830HD-45	1830HD-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Commercial	880	880	880	880	880
	Military			880	880	880
Maximum Standby Current (mA)	Commercial	320	320	320	320	320
	Military			320	320	320

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

CYM1831

64K x 32 Static RAM Module

Features

- **High-density 2M-bit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 25 ns**
- **Low active power**
  - **— 4W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .50 in.**
- **Small PCB footprint**
  - **— 1.2 sq. in.**
- **JEDEC-compatible pinout**

Functional Description

The CYM1831 is a high-performance 2-Mbit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$ and $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

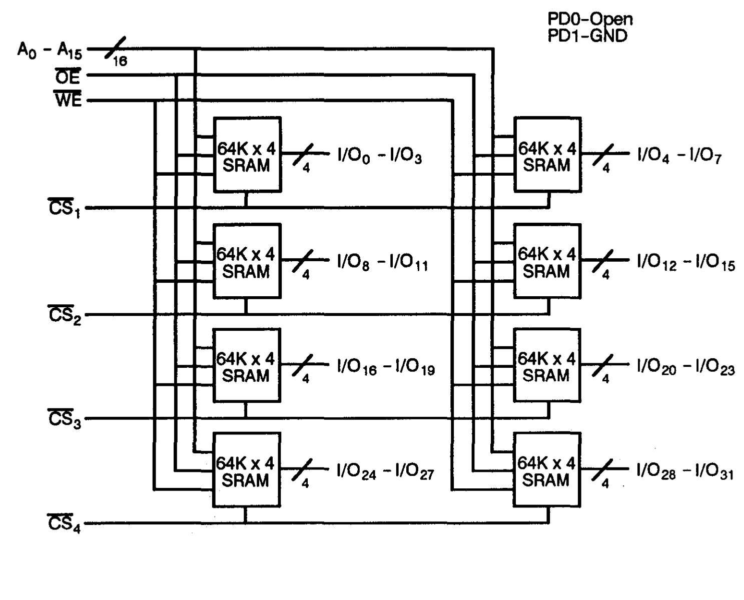
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}_N$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_N$) LOW and output enable ($\overline{OE}$) low, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

Two pins (PD0 and PD1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

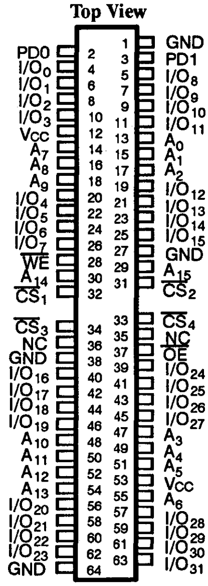
Logic Block Diagram



1831-1

Pin Configuration

ZIP
Top View



1831-2

Selection Guide

	1831PM-25 1831PZ-25	1831PM-30 1831PZ-30	1831PM-35 1831PZ-35	1831PM-45 1831PZ-45
Maximum Access Time (ns)	25	30	35	45
Maximum Operating Current (mA)	720	720	720	720
Maximum Standby Current (mA)	160	160	160	160

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

CYM1832

64K x 32 Static RAM Module

Features

- **High-density 2-Mbit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 25 ns**
- **Low active power**
  - **— 5.4W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .50 in.**
- **Small PCB footprint**
  - **— 1.0 sq. in.**

Functional Description

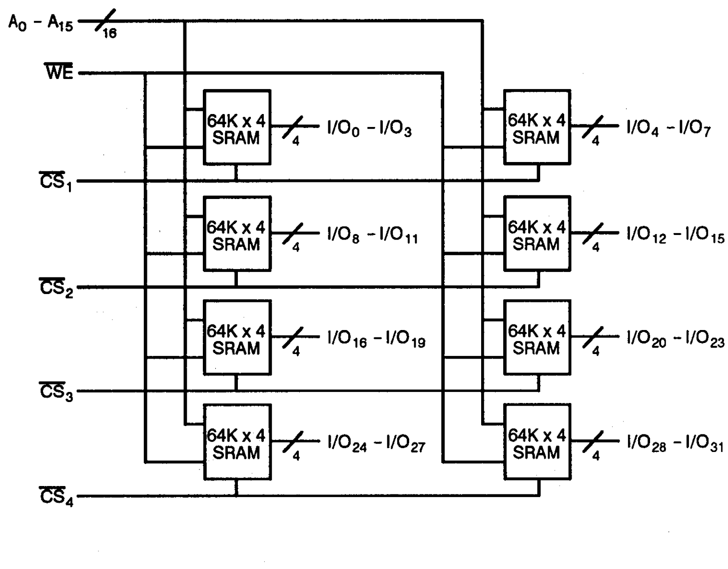
The CYM1832 is a high-performance 2-Mbit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, and $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}_N$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_N$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

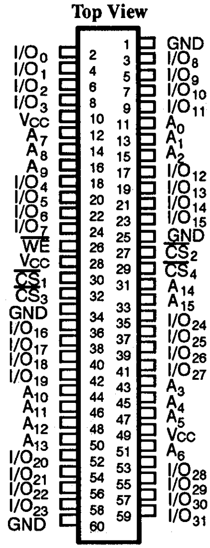
Logic Block Diagram



1832-1

Pin Configuration

ZIP
Top View



1832-2

Selection Guide

	1832PZ-25	1832PZ-35	1832PZ-45	1832PZ-55
Maximum Access Time (ns)	25	35	45	55
Maximum Operating Current (mA)	980	980	980	980
Maximum Standby Current (mA)	240	240	240	240

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1841**

256K x 32 Static RAM Module

Features

- **High-density 8-Mbit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 35 ns**
- **Low active power**
  - **— 5.3W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .58 in.**
- **Small PCB footprint**
  - **— 1.3 sq. in.**
- **JEDEC-compatible pinout**

Functional Description

The CYM1841 is a high-performance 8-Mbit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$, $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

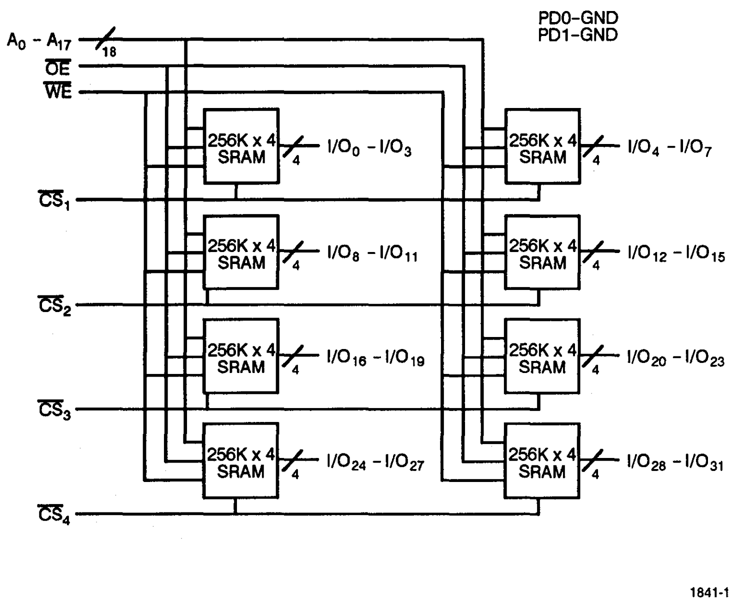
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}_N$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_x) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_N$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_x).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

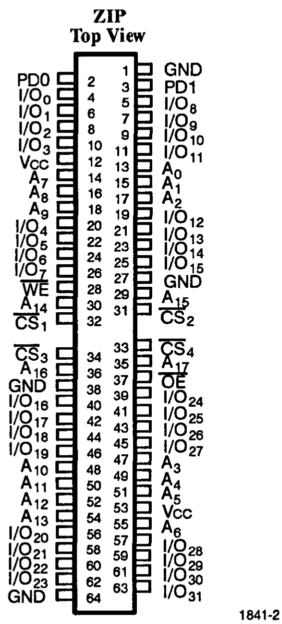
Two pins (PD0 and PD1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

Logic Block Diagram



1841-1

Pin Configuration



1841-2

Selection Guide

	1841PM-35 1841PZ-35	1841PM-45 1841PZ-45	1841PM-55 1841PZ-55
Maximum Access Time (ns)	35	45	55
Maximum Operating Current (mA)	960	960	960
Maximum Standby Current (mA)	480	480	480

This is a partial data sheet. For complete data sheet, see Section 8, Modules.

CYPRESS SEMICONDUCTOR

16K x 68 SRAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **10.4W (max.)**
- **SMD technology**
- **Registered address inputs**
- **Four completely independent memory banks**
- **Small PCB footprint**
  - **1.9 sq. in.**

Functional Description

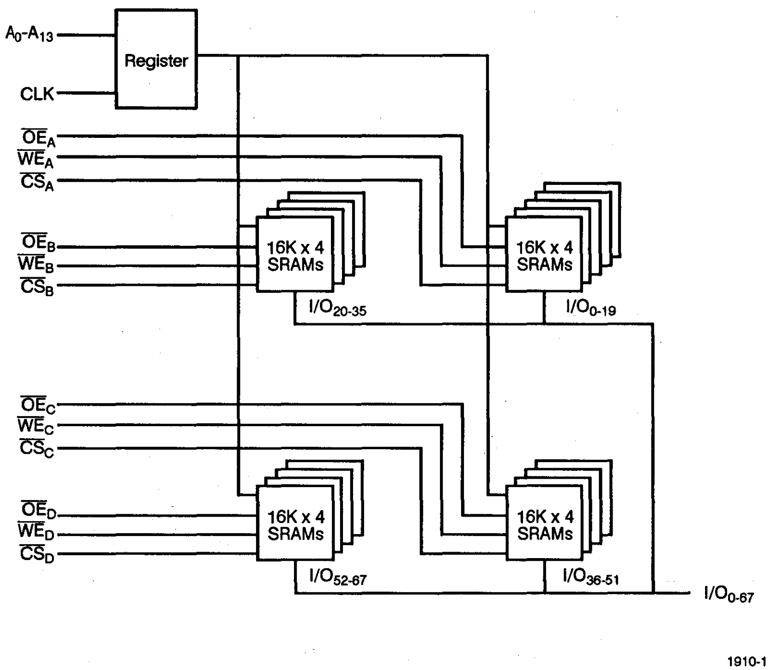
The CYM1910 is a very high performance 1-megabit static RAM module organized as 16K words by 68 bits. This module is constructed using seventeen 16K x 4 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins. The memory is organized as three banks of 16K x 16 and one of 16K x 20, each of which has its own chip select, write enable, and output enable signals.

Writing to the module is accomplished when the appropriate chip select ($\overline{CS}_x$) and write enable ($\overline{WE}_x$) inputs are both LOW. Data on the appropriate input/output pins (I/O_{nn}) of the device is written into the memory location specified by the content of the address register. The address register is loaded on the rising edge of the clock signal (CLK).

Reading the device is accomplished by taking chip select ($\overline{CS}_x$) and output enable ($\overline{OE}_x$) low while $\overline{WE}_x$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified by the contents of the address register will appear on the appropriate data input/output pins (I/O_{nn}).

The data input/output pins remain in a high-impedance state when chip select ($\overline{CS}_x$) or output enable ($\overline{OE}_x$) is HIGH, or when write enable ($\overline{WE}_x$) is LOW.

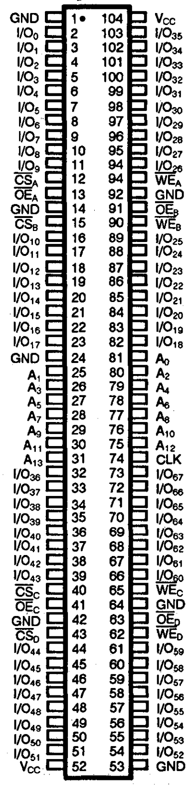
Logic Block Diagram



1910-1

Pin Configuration

Plastic VDIP
Top View



1910-2

CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1911**

16K x 68 SRAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **10.4W (max.)**
- **SMD technology**
- **Latched address inputs**
- **Four completely independent memory banks**
- **Small PCB footprint**
  - **1.9 sq. in.**

Functional Description

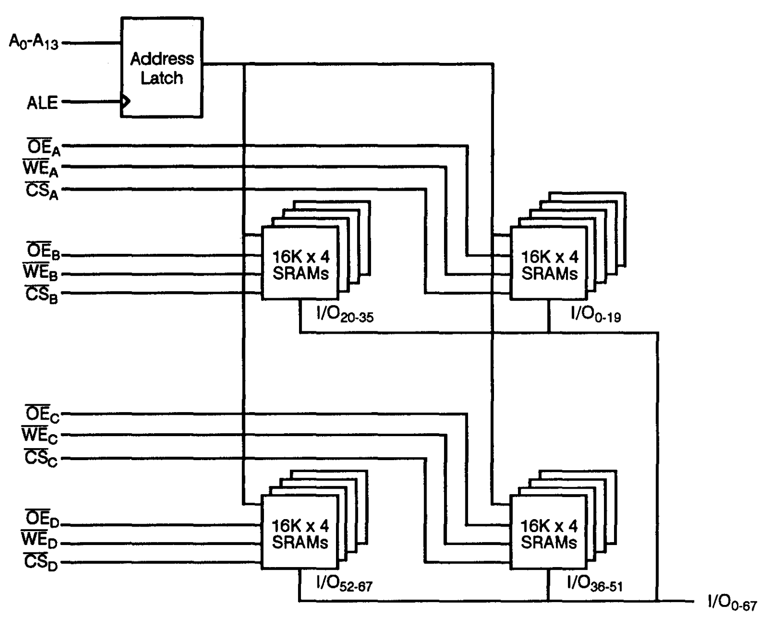
The CYM1911 is a very high performance 1-megabit static RAM module organized as 16K words by 68 bits. This module is constructed using seventeen 16K x 4 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins. The memory is organized as three banks of 16K x 16 and one of 16K x 20, each of which has its own chip select, write enable, and output enable signals.

Writing to the module is accomplished when the appropriate chip select ($\overline{CS_X}$) and write enable ($\overline{WE_X}$) inputs are both LOW. If Latch Enable (ALE) is HIGH, data on the appropriate input/output pins (I/O_{nn}) of the device is written into the memory location specified on the address pins (A_0 through A_{13}). If ALE is LOW, data is written into the address specified by the contents of the address latch. The value in this latch is updated on the falling edge of ALE.

Reading the device is accomplished by taking chip select ($\overline{CS_X}$) and output enable ($\overline{OE_X}$) LOW while $\overline{WE_X}$ remains inactive or HIGH. If Latch Enable (ALE) is HIGH, the contents of the memory location specified on the address pins (A_0 through A_{13}) will appear on the appropriate data input/output pins (I/O_{nn}). If ALE is LOW, the contents of the memory location specified by the value in the address latch will appear on I/O_{nn}.

The data input/output pins remain in a high-impedance state when chip select ($\overline{CS_X}$) or output enable ($\overline{OE_X}$) is HIGH, or when write enable ($\overline{WE_X}$) is LOW.

Logic Block Diagram



1911-1

Pin Configuration

Plastic VDIP

Signal	Pin	Pin	Signal
GND	1	104	V_{CC}
I/O_0	2	103	I/O_{35}
I/O_1	3	102	I/O_{34}
I/O_2	4	101	I/O_{33}
I/O_3	5	100	I/O_{32}
I/O_4	6	99	I/O_{31}
I/O_5	7	98	I/O_{30}
I/O_6	8	97	I/O_{29}
I/O_7	9	96	I/O_{28}
I/O_8	10	95	I/O_{27}
I/O_9	11	94	I/O_{26}
$\overline{CS_A}$	12	94	$\overline{WE_A}$
$\overline{OE_A}$	13	92	GND
GND	14	91	$\overline{OE_B}$
$\overline{CS_B}$	15	90	$\overline{WE_B}$
I/O_{10}	16	89	I/O_{25}
I/O_{11}	17	88	I/O_{24}
I/O_{12}	18	87	I/O_{23}
I/O_{13}	19	86	I/O_{22}
I/O_{14}	20	85	I/O_{21}
I/O_{15}	21	84	I/O_{20}
I/O_{16}	22	83	I/O_{19}
I/O_{17}	23	82	I/O_{18}
GND	24	81	A_0
A_1	25	80	A_2
A_3	26	79	A_4
A_5	27	78	A_6
A_7	28	77	A_8
A_9	29	76	A_{10}
A_{11}	30	75	A_{12}
A_{13}	31	74	ALE
I/O_{36}	32	73	I/O_{67}
I/O_{37}	33	72	I/O_{66}
I/O_{38}	34	71	I/O_{65}
I/O_{39}	35	70	I/O_{64}
I/O_{40}	36	69	I/O_{63}
I/O_{41}	37	68	I/O_{62}
I/O_{42}	38	67	I/O_{61}
I/O_{43}	39	66	I/O_{60}
$\overline{CS_C}$	40	65	$\overline{WE_C}$
$\overline{OE_C}$	41	64	GND
GND	42	63	$\overline{OE_D}$
$\overline{CS_D}$	43	62	$\overline{WE_D}$
I/O_{44}	44	61	I/O_{59}
I/O_{45}	45	60	I/O_{58}
I/O_{46}	46	59	I/O_{57}
I/O_{47}	47	58	I/O_{56}
I/O_{48}	48	57	I/O_{55}
I/O_{49}	49	56	I/O_{54}
I/O_{50}	50	55	I/O_{53}
I/O_{51}	51	54	I/O_{52}
V_{CC}	52	53	GND

1911-2

Section Contents

PROMs (Programmable Read Only Memory) **Page Number**

1: Product Line Overview

The Cypress CMOS family of PROMs span 4K to 512K bit densities, three functional configurations, and are all byte-wide. The product line is available in both 0.3 and 0.6 inch wide dual-in-line plastic and CERDIP as well as LCC and PLCC packages. The programming technology is EPROM and therefore windowed packages are available in both dual-in-line and LCC configurations, providing erasable products. These byte-wide products are available in registered versions at the 512, 1K, 2K, 8K, 32K, and 64K by 8 densities and in non-registered versions at the 1K, 2K, 8K, 16K, 32K, and 64K by 8 densities. The registered devices operate in either synchronous or asynchronous output enable modes and may have an initialize feature to preload the pipeline register. The 8K by 8 registered devices feature a diagnostic shadow register which allows the pipeline register to be loaded or examined via a serial path.

Cypress PROMs perform at the level of their bipolar equivalents or beyond with reduced power levels of CMOS technology. They are capable of 2001 volts of ESD and operate with 10% power supply tolerances.

2: Technology Introduction

Cypress PROMs are executed in an "N" well CMOS EPROM process. Densities of 128K and under with the exception of the "A" series devices use the 1.2 micron PROM I technology. The 16K "A" series devices and the future 256K PROMs use the 0.8 micron PROM II technology with a single ended memory cell. The process provides basic gate delays of 235 picoseconds for a fanout of one at a power consumption of 45 femto joules. The process provides the basis for the development of LSI products that outperform the fastest bipolar products currently available.

Although CMOS static RAMs have challenged bipolar RAMs for speed, CMOS EPROMs have always been a factor of three to ten times slower than bipolar fuse PROMs. There have been two major limitations on CMOS EPROM speed; 1) the single transistor EPROM cell is inherently slower than the bipolar fuse element, and 2) CMOS EPROM technologies have been optimized for cell programmability and density, almost always at the expense of speed. In the Cypress CMOS EPROM technology, both of the aforementioned limitations have been overcome to create CMOS PROMs with performance superior to PROMs implemented in bipolar technology.

In all Cypress PROMs, speed and programmability are optimized independently by separating the read and write transistor functions. Also, for the first time a substrate bias generator is employed in an EPROM technology to improve performance and raise latchup immunity to greater than 200 mA. The result is a CMOS EPROM technology that challenges bipolar fuse technology for both density and speed. In addition, at higher densities, performance and density surpasses the best that bipolar can provide. Limitations of devices implemented in the bipolar fuse technology such as PROGRAMMING YIELD, POWER DISSIPATION and HIGHER DENSITY PERFORMANCE are eliminated or greatly reduced using Cypress CMOS EPROM technology.

3: Design Approach

A. Four Transistor Differential Memory Cell

The 4K, 8K, and 16K PROM (except "A" version) use an N-Well CMOS technology along with a new differential four transistor EPROM cell that is optimized for speed. The area of the four transistor cell is 0.43 square mils and the die size is 19,321 square mils for the 2K by 8 PROM (*Figure 1*). The floating gate cell is optimized for high read current and fast programmability. This is accomplished by separating the read and program transistors (*Figure 2*). The program transistor has a separate implant to maximize the generation and collection of hot electrons while the read transistor implant dose is chosen to provide a large read current. Both the n and p channel peripheral transistors have self-aligned, shallow, lightly doped drain (LDD) junctions. The LDD structure reduces overlap capacitance for speed improvement and minimizes hot electron injection for improved reliability. Although common for NMOS static and dynamic RAMs, an on-chip substrate bias generator is used for the first time in an EPROM technology. The results are improved speed, greater than 200 mA latch-up immunity and high parasitic field inversion voltages during programming.

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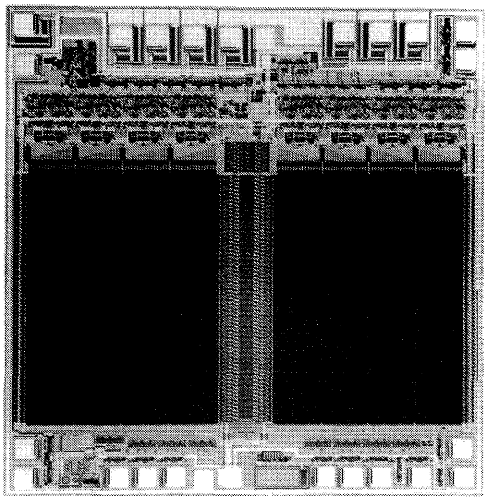

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Figure 1

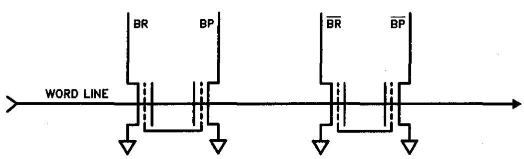

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Figure 2. Non-volatile cell optimized for speed and programmability

Access times of less than 35 ns at 16K densities and 30 ns at 4K and 8K densities over the full operating range are achieved by using differential design techniques and by to-

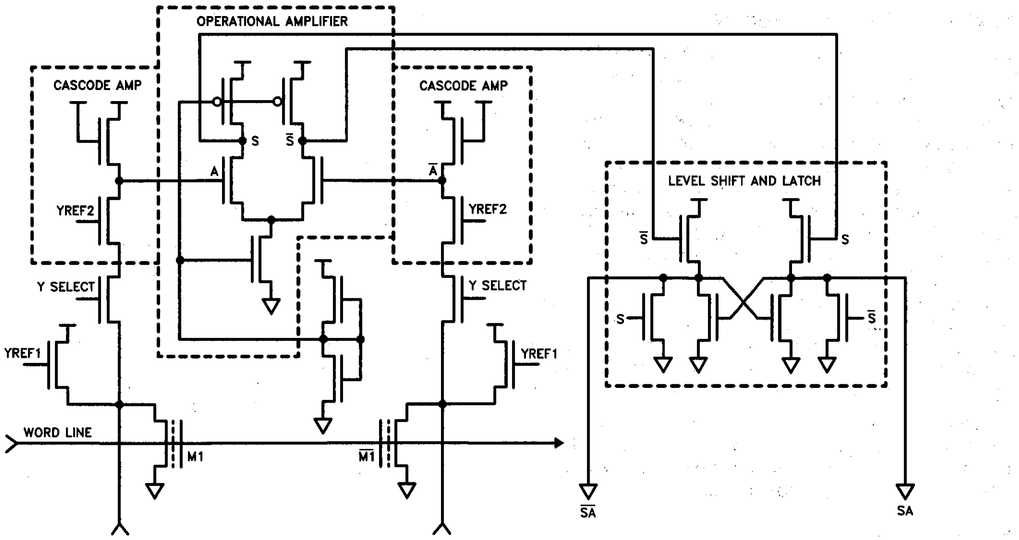


Figure 3. Differential sensing

tally separating the read and program paths. This allows the read path to be optimized for speed. The X and Y decoding paths are predecoded to optimize the power-delay product. A differentail sensing scheme and the four transistor cell are used to sense bit-line swings as low as 100 mV at high speed. The sense amplifier (*Figure 3*) consists of three stages of equal gain. A gain of 4 per stage was found to be optimum. The Cascode stage amplifies the bit line swings and feeds them into a differential amplifier. The output of the differential amplifier is further amplified and voltages shifted by a level shifter and latch. This signal is then fed into an output buffer having a TTL fan-out of ten.

B. Two Transistor Memory Cell

The Cypress 64K and greater density PROMs use a two transistor memory cell. This cell uses a single ended sensing scheme with the exception of the 256K device which uses a differential sensing circuit. This combination allows for a more compact design and reduced manufacturing costs. This is an excellent compromise between performance and high density, allowing the development of devices with performance of 35 ns and 45 ns access times at densities from 64K to 256K bits and 25 ns for the "A" series 16K using the PROM II technology. This two transistor cell still uses the high speed read transistor and the optimized EPROM transistor for performance and reliable programming. The sense amplifier uses a reference voltage on one input and the read transistor on the other, instead of two read transistors. This single ended sensing is a more conventional technique and has the effect of causing an erased device to contain all "0"s.

4: Programming

A. Differential Memory Cells

Cypress PROMs are programmed a BYTE at a time by applying 12 to 14 volts on one pin and the desired logic levels to input pins. Both logic "ONE" and logic "ZERO" are programmed into the differential cell. A BIT is programmed by applying 12 to 14 volts on the control gate and 9 volts on the drain of the floating gate write transistor. This causes hot electrons from the channel to be injected onto the floating gate thereby raising the threshold voltage. Because the read transistor shares a common floating gate with the program transistor, the threshold of the read transistor is raised from about 1 volt to greater than 5 volts resulting in a transistor that is turned "OFF" when selected in a read mode of operation. Since both sides of the differential cell are at equal potential before programming, a threshold shift of 100 mV is enough to be determined as the correct logic state. Because an unprogrammed cell has neither a ONE nor a ZERO in it before programming, a special BLANK CHECK mode of operation is implemented. In this mode the output of each half of the cell is compared against a fixed reference which allows distinction of a programmed or unprogrammed cell. A MARGIN mode is also provided to monitor the thresholds of the individual BITs allowing the monitoring of the quality of programming during the manufacturing operation.

B. Single Ended Memory Cells

The programming mechanism of the EPROM transistor in a single ended memory cell is the same as its counterpart in a double ended memory cell. The difference is that only ones "1"s are programmed in a single ended cell. A "1" applied to the I/O pin during programming causes an erased EPROM transistor to be programmed while a "0" allows the EPROM transistor to remain unprogrammed.

5: Erasability

For the first time at PROM speeds, Cypress PROMs using CMOS EPROM technology offer reprogrammability when packaged in windowed CERDIP. This is available at densities of 16K and larger, both registered and non-registered.

Wavelengths of light less than 4000 Angstroms begin to erase Cypress PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity $\times$ exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 30–35 minutes. The industry EPROM erasure standard is 15 Wsec/cm^2. Cypress EPROMs require $1^2/_3$ longer erase times.

The PROM needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Some devices are sensitive to photo-electric effects during programming. Cypress recommends covering the windows of reprogrammable devices during programming.

6: Reliability

The CMOS EPROM approach to PROMs has some significant benefits to the user in the area of programming and functional yield. Since a cell may be programmed and erased multiple times, CMOS PROMs from Cypress can be tested 100% for programmability during the manufacturing process. Because each CMOS PROM contains a PHANTOM array, both the functionality and performance of the devices may be tested after they are packaged thus assuring the user that not only will every cell program, but that the product performs to the specification.

CYPRESS SEMICONDUCTOR

512 x 8 Registered PROM

Features

- CMOS for optimum speed/power
- High speed
  - — 25 ns max set-up
  - — 12 ns clock to output
- Low power
  - — 495 mW (commercial)
  - — 660 mW (military)
- Synchronous and asynchronous output enables
- On-chip edge-triggered registers
- Buffered Common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs
- EPROM technology, 100% programmable
- Slim, 300 mil, 24 pin plastic or hermetic DIP, or 28 pin LCC
- 5V ±10% V_{CC}, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 1500V static discharge

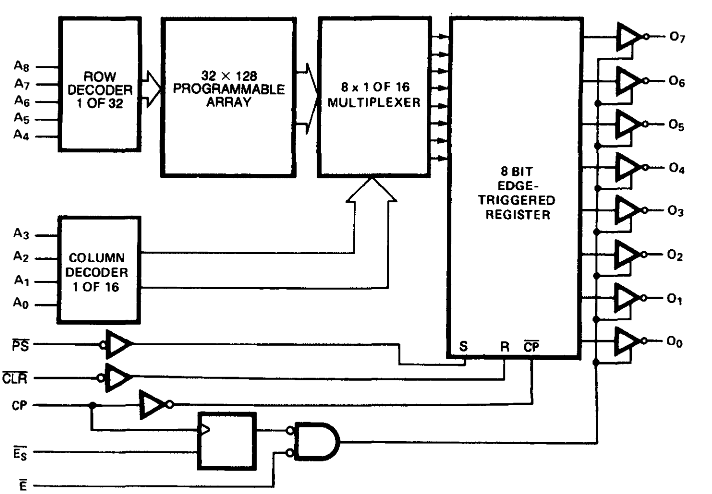
Product Characteristics

The CY7C225 is a high performance 512 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP and 28 pin Leadless Chip Carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C225 replaces bipolar devices and offers the advantages of lower power, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C225 has asynchronous PRESET and CLEAR functions.

Logic Block Diagram



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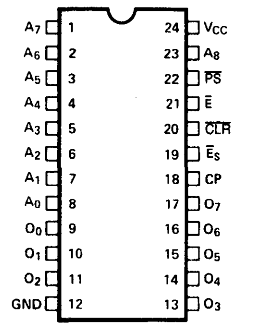
Pin Configurations



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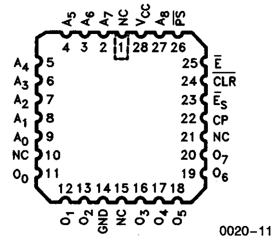

0020-11

Selection Guide

		7C225-25	7C225-30	7C225-35	7C225-40
Maximum Set-up Time (ns)		25	30	35	40
Maximum Clock to Ouput (ns)		12	15	20	25
Maximum Operating Current (mA)	Commercial	90	90		90
	Military		120	120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 14.0V

Static Discharge Voltage .... >1500V (Per MIL-STD-883 Method 3015)

Latch-up Current......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[6]	−55°C to +125°C	5V ±10%

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Electrical Characteristics Over Operating Range[7]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = −16 mA V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All inputs[2]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 1				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[4]		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[3]		−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = Max.	Commercial		90	mA
			Military		120	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF

Notes:

1. The CMOS process does not provide a clamp diode. However, the CY7C225 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. Tested initially and after any design or process changes that may affect these parameters.
6. T_A is the "instant on" case temperature.
7. See the last page of this specification for Group A subgroup testing information.

Switching Characteristics Over Operating Range[7, 8]

Parameters	Description	7C225-25		7C225-30		7C225-35		7C225-40		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	25		30		35		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		20		25	ns
t_{PWC}	Clock Pulse Width	10		15		20		20		ns
t_{SES}	$\overline{E}_S$ Setup to Clock HIGH	10		10		10		10		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	0		5		5		5		ns
t_{DP}, t_{DC}	Delay from $\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ to Valid Output		20		20		20		20	ns
t_{RP}, t_{RC}	$\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ Recovery to Clock HIGH	15		20		20		20		ns
t_{PWP}, t_{PWC}	$\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ Pulse Width	15		20		20		20		ns
t_{COS}	Valid Output from Clock HIGH[1]		20		20		25		30	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		20		20		25		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW[2]		20		20		25		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		20		20		25		30	ns

Notes:

1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b*.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.
8. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms[5, 6, 7]

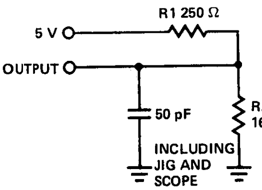

Figure 1a

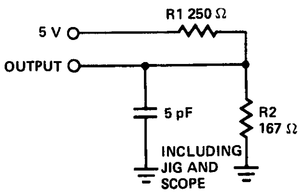

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Figure 1b

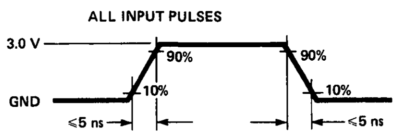

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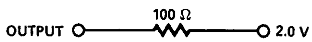
Figure 2

Equivalent to:

THÉVENIN EQUIVALENT



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Functional Description

The CY7C225 is a CMOS electrically Programmable Read Only Memory organized as 512 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C225 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables, and $\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ inputs.

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high impedance state. Data is read by applying the memory location to the address inputs (A_0–A_8) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Functional Description (Continued)

Regardless of the condition of $\overline{E}$, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable ($\overline{E}_S$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{E}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C225 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C225 has buffered asynchronous $\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ input ($\overline{\text{INIT}}$). The initialize function is useful during power-up and time-out sequences.

Applying a LOW to the $\overline{\text{PRESET}}$ input causes an immediate load of all ones into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). Applying a LOW to the $\overline{\text{CLEAR}}$ input, resets the flip-flops to all zeros. The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high impedance state. In order to enable the outputs a clock must occur and the $\overline{E}_S$ input pin must be LOW at least a setup time prior to the clock LOW to HIGH transition. The $\overline{E}$ input may then be used to enable the outputs.

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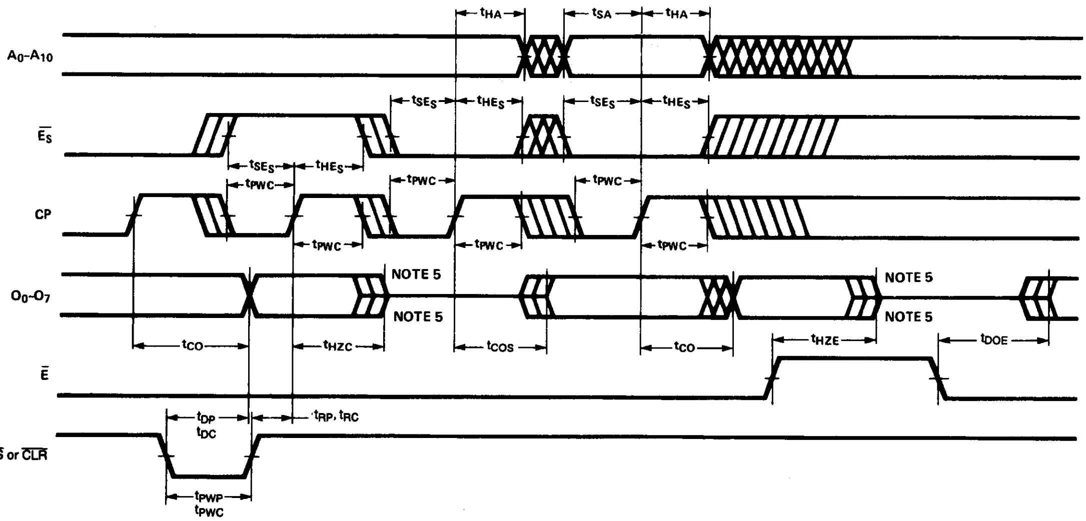
Switching Waveforms



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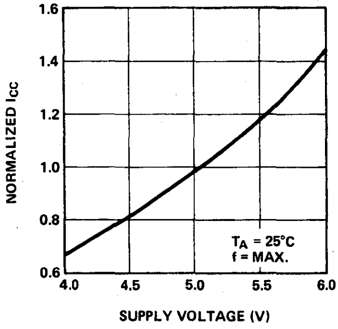
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

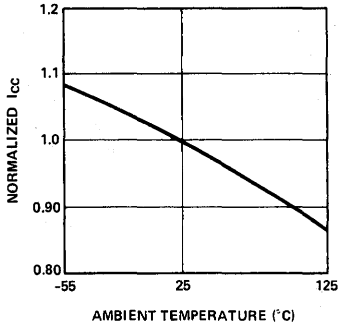
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b*.

Typical DC and AC Characteristics

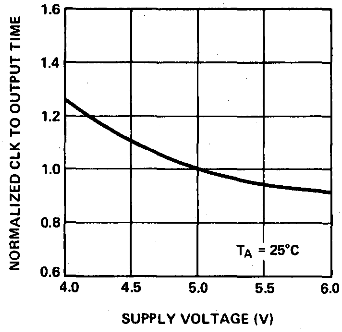
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



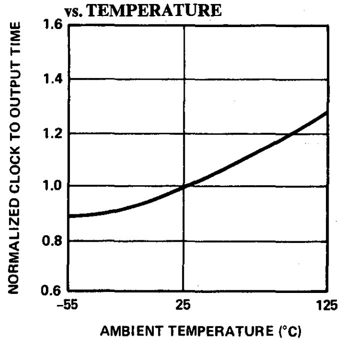
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



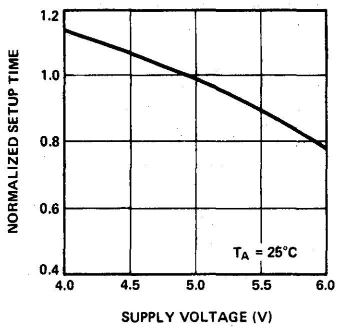
CLOCK TO OUTPUT TIME vs. V_{CC}



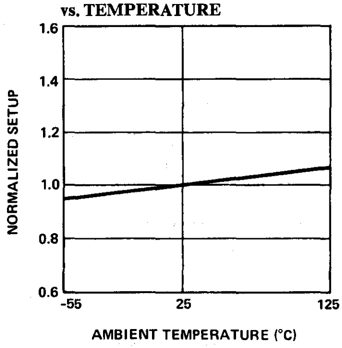
CLOCK TO OUTPUT TIME vs. TEMPERATURE



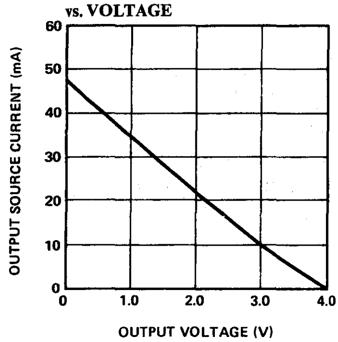
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



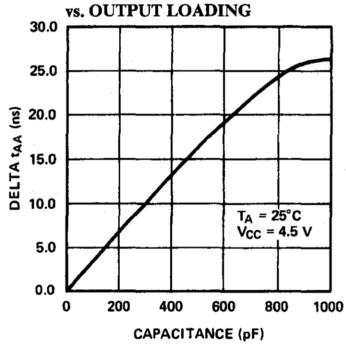
NORMALIZED SETUP TIME vs. TEMPERATURE



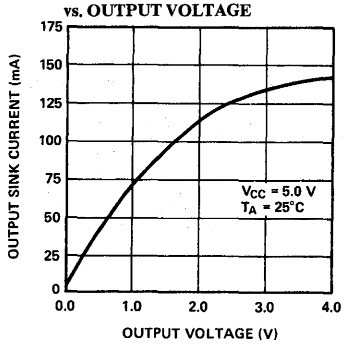
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



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Device Programming

Overview:

There is a programmable function contained in the 7C225 CMOS 512 x 8 Registered PROM; the 512 x 8 array. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped.

The 512 x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	50		ns
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function[1]					Outputs (9–11,13–17)
	Read or Output Disable	CP	$\overline{E}_S$	$\overline{CLR}$	$\overline{E}$	$\overline{PS}$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{E}$	$\overline{PS}$	
	Pin	(18)	(19)	(20)	(21)	(22)	
Read[2,3]		X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Data Out
Output Disable[5]		X	V_{IH}	V_{IH}	X	V_{IH}	High Z
Output Disable		X	X	V_{IH}	V_{IH}	V_{IH}	High Z
$\overline{CLEAR}$		X	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Zeros
$\overline{PRESET}$		X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Ones
Program[4]		V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	Data In
Program Verify[4]		V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	Data Out
Program Inhibit[4]		V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	High Z
Intelligent Program[4]		V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	Data In
Blank Check Ones[4]		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	Ones
Blank Check Zeros[4]		V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	Zeros

Notes:
1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. Pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. Pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.

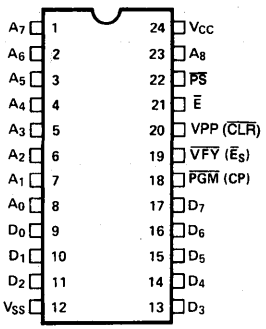


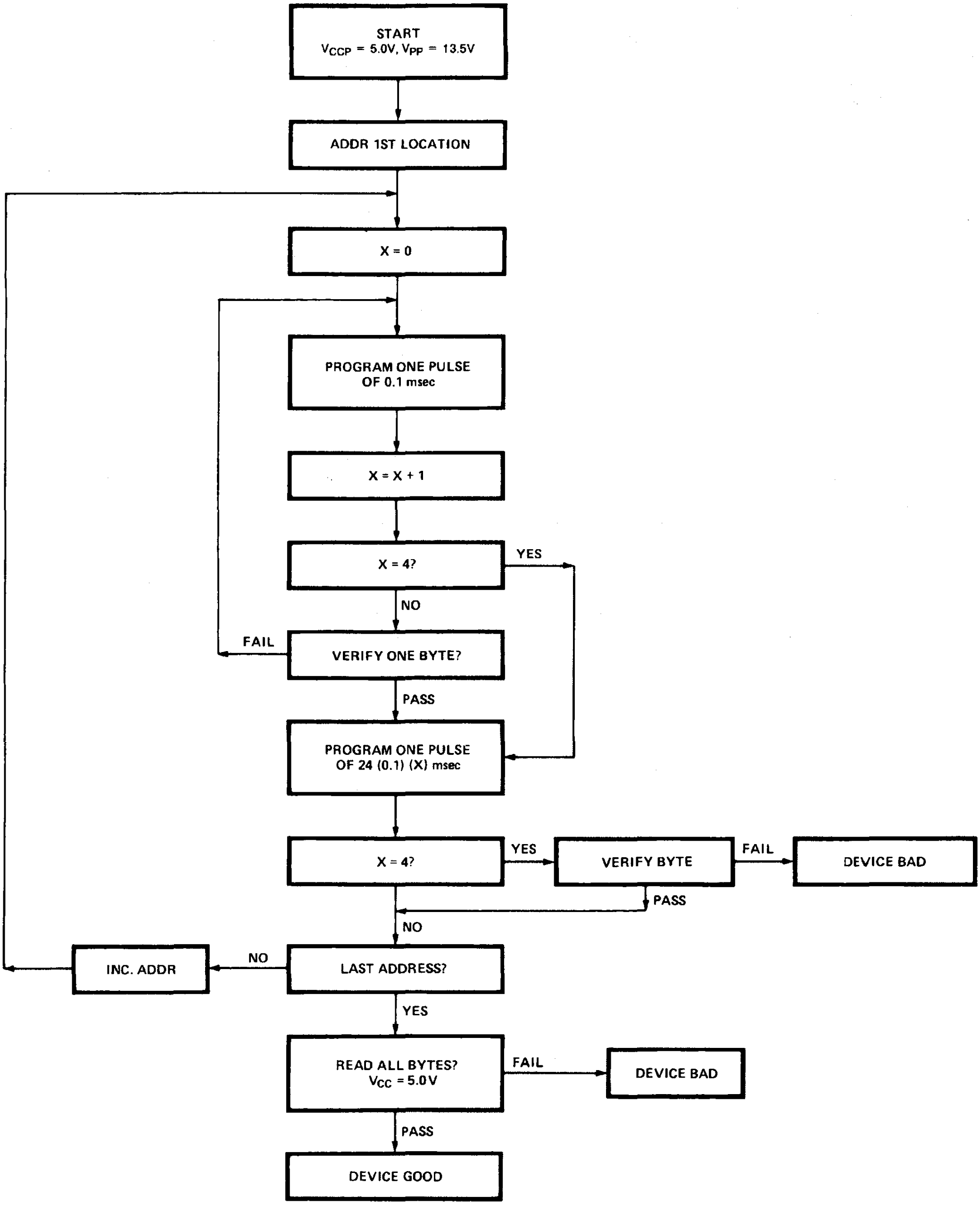
Figure 3. Programming Pinouts

The CY7C225 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4*.

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.



0020–9

Figure 4. Programming Flowchart

Programming Sequence 512 x 8 Array

Power the device for normal read mode operation with pin 18, 19, 20 and 21 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figure 5*. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 511. A device is considered virgin if all locations are respectively "1's" and "0's" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

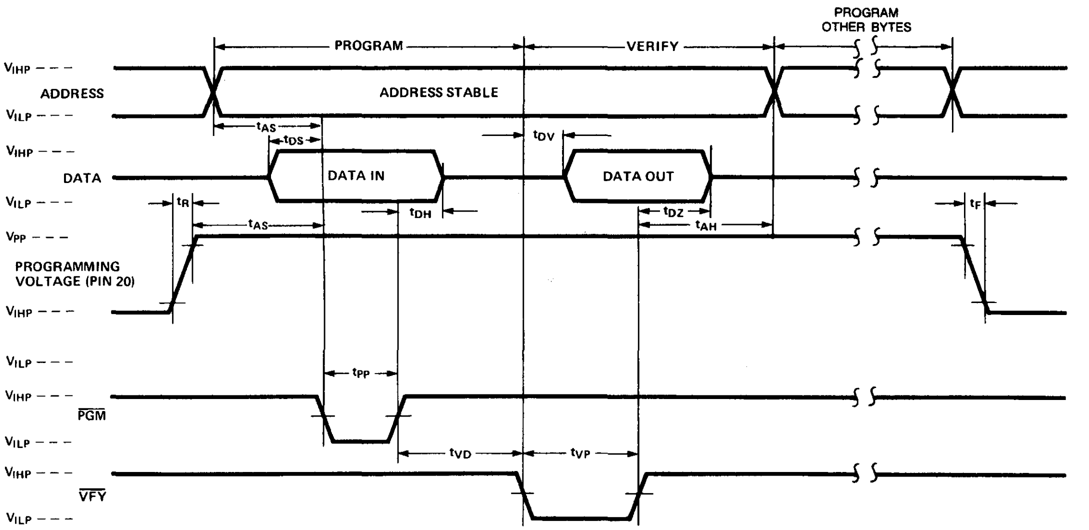


Figure 5. PROM Programming Waveforms

Ordering Information

Speed ns t_{SA}	Speed ns t_{CO}	Ordering Code	Package Type	Operating Range
25	12	CY7C225-25PC CY7C225-25DC CY7C225-25LC	P13 D14 L64	Commercial
30	15	CY7C225-30PC CY7C225-30DC CY7C225-30LC	P13 D14 L64	Commercial
		CY7C225-30DMB CY7C225-30LMB	D14 L64	Military
35	20	CY7C225-35DMB CY7C225-35LMB	D14 L64	Military
40	25	CY7C225-40PC CY7C225-40DC CY7C225-40LC	P13 D14 L64	Commercial
		CY7C225-40DMB CY7C225-40LMB	D14 L64	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{SA}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{CO}	7,8,9,10,11
t_{DP}	7,8,9,10,11
t_{RP}	7,8,9,10,11

Document #: 38-00002-B

![CYPRESS SEMICONDUCTOR]

CY7C235

1024 x 8 Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 25 ns max set-up**
  - **— 12 ns clock to output**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **Synchronous and asynchronous output enables**
- **On-chip edge-triggered registers**
- **Programmable asynchronous register ($\overline{INIT}$)**
- **EPROM technology, 100% programmable**
- **Slim, 300 mil, 24 pin plastic or hermetic DIP or 28 pin LCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding greater than 1500V static discharge**

Product Characteristics

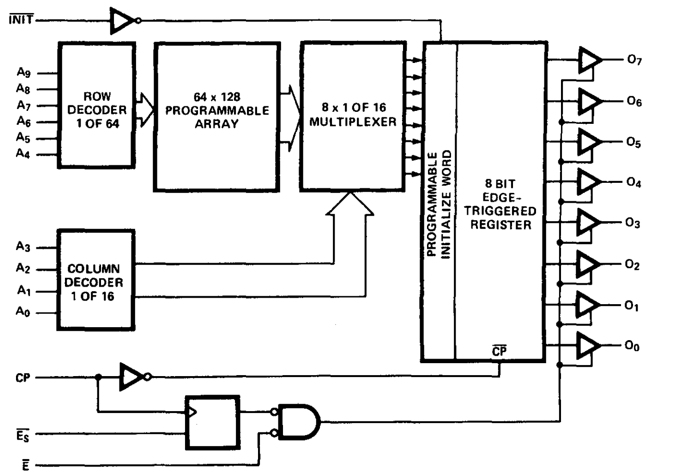
The CY7C235 is a high performance 1024 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP or 28-pin Leadless Chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C235 replaces bipolar devices and offers the advantages of lower power, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C235 has an asynchronous initialize function ($\overline{INIT}$). This function acts as a 1025th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

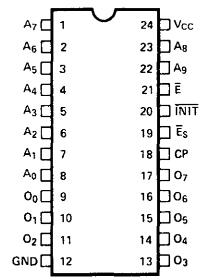
3

Logic Block Diagram

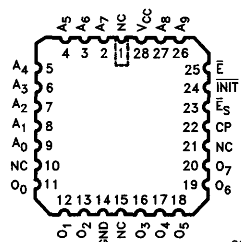


0005-1

Pin Configurations



0005-2



0005-12

Selection Guide

		7C235-25	7C235-30	7C235-40
Maximum Set-up Time (ns)		25	30	40
Maximum Clock to Output (ns)		12	15	20
Maximum Operating Current (mA)	Commercial	90	90	90
	Military		120	120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to + 125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12 for DIP)............. −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage
(Pins 7, 18, 20 for DIP) 14.0V

Static Discharge Volume .... > 1500V
(Per MIL-STD-883 Method 3015)

Latch-up Current......................... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[6]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[7]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[2]		2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[2]			0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 1				
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[4]		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[3]		−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = Max.	Commercial		90	mA
			Military		120	

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. The CMOS process does not provide a clamp diode. However, the CY7C235 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. Tested initially and after any design or process changes that may affect these parameters.
6. T_A is the "instant on" case temperature.
7. See the last page of this specification for Group A subgroup testing information.

Switching Characteristics Over Operating Range[4, 8]

Parameters	Description	7C235-25		7C235-30		7C235-40		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	25		30		40		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		20	ns
t_{PWC}	Clock Pulse Width	12		15		20		ns
t_{SES}	$\overline{E}_S$ Setup to Clock HIGH	10		10		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		ns
t_{DI}	Delay from $\overline{\text{INIT}}$ to Valid Output		25		25		35	ns
t_{RI}	$\overline{\text{INIT}}$ Recovery to Clock HIGH	20		20		20		ns
t_{PWI}	$\overline{\text{INIT}}$ Pulse Width	20		20		25		ns
t_{COS}	Inactive to Valid Output from Clock HIGH[1]		20		20		25	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		20		20		25	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW[2]		20		20		25	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		20		20		25	ns

Notes:
1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state High level −500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b.*
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.
8. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms [5, 6, 7]

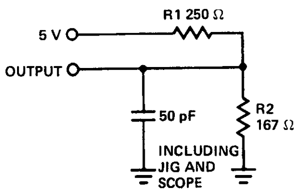


Figure 1a

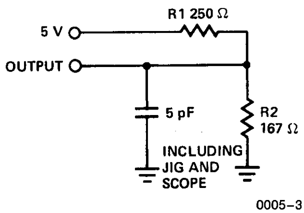


Figure 1b

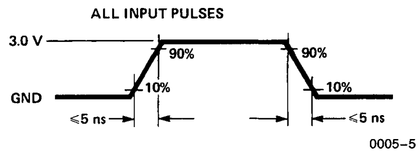
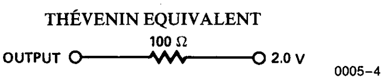


Figure 2

Equivalent to:



Functional Description

The CY7C235 is a CMOS electrically Programmable Read Only Memory organized as 1024 word x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C235 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with synchronous ($\overline{E}_S$) and asynchronous ($\overline{E}$) output enables and asynchronous initialization ($\overline{\text{INIT}}$).

Upon power-up, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high impedance state. Data is read by applying the memory location to the address input (A_0–A_9) and a logic LOW to the enable ($\overline{E}_S$) input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7) provided the asynchronous enable ($\overline{E}$) is also LOW.

The outputs may be disabled at any time by switching the asynchronous enable ($\overline{E}$) to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

Functional Description (Continued)

Regardless of the condition of $\overline{\text{E}}$, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable ($\overline{\text{E}_\text{S}}$) input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state if $\overline{\text{E}}$ is LOW. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C235 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

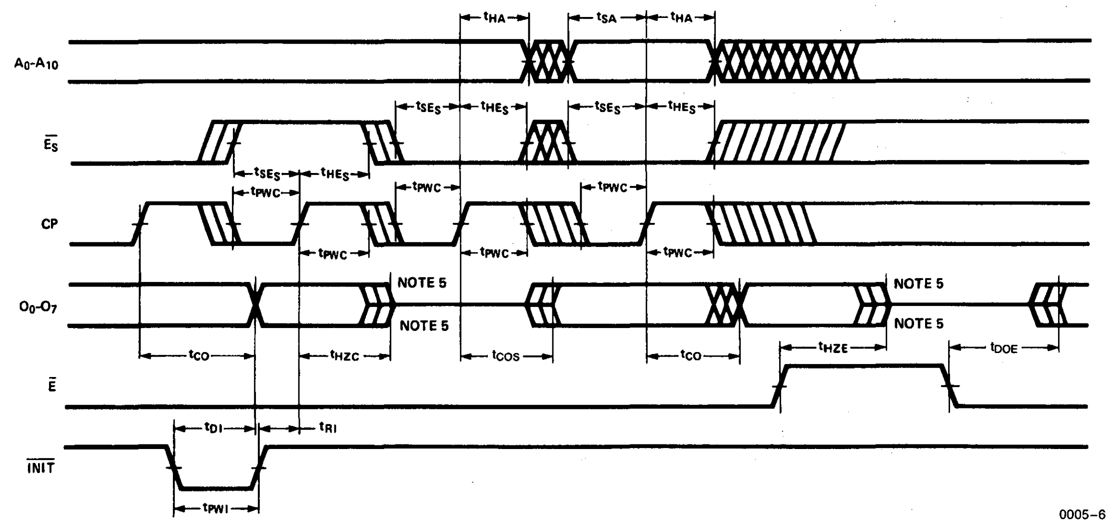
The CY7C235 has an asynchronous initialize input ($\overline{\text{INIT}}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 1025th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating $\overline{\text{INIT}}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{\text{INIT}}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{\text{INIT}}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{\text{E}}$) LOW.

When power is applied the (internal) synchronous enable flip-flop will be in a state such that the outputs will be in the high impedance state. In order to enable the outputs, a clock must occur and the $\overline{\text{ES}}$ input pin must be LOW at least a setup time prior to the clock LOW to HIGH transition. The $\overline{\text{E}}$ input may then be used to enable the outputs.

When the asynchronous initialize input, $\overline{\text{INIT}}$, is LOW, the data in the initialize byte will be asynchronously loaded into the output register. It will not, however, appear on the output pins until they are enabled, as described in the preceding paragraph.

Switching Waveforms



0005-6

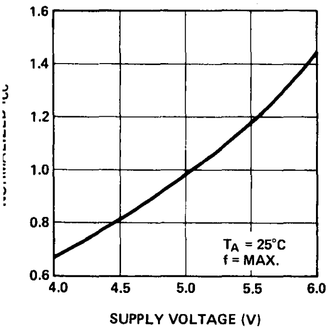
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

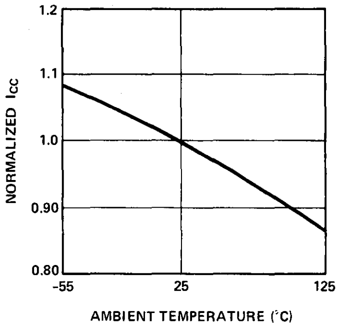
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b*.

Typical DC and AC Characteristics

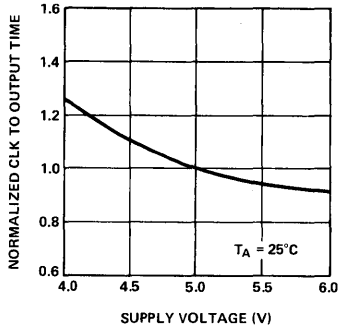
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



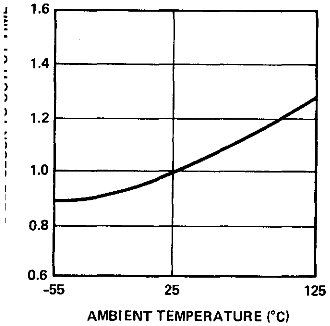
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



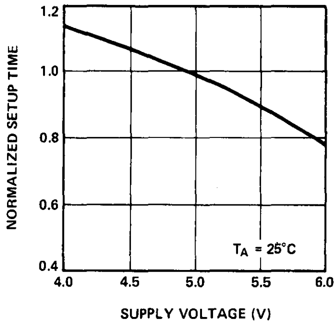
NORMALIZED CLOCK TO OUTPUT TIME vs. V_{CC}



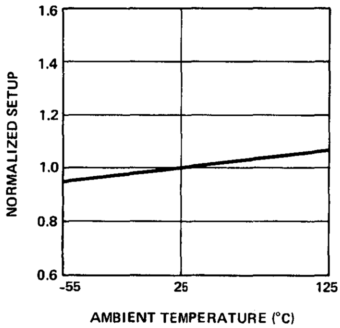
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



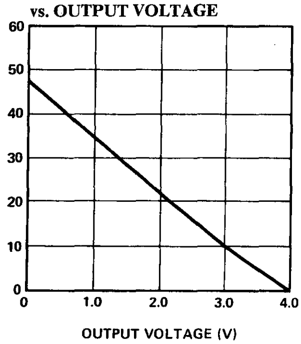
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



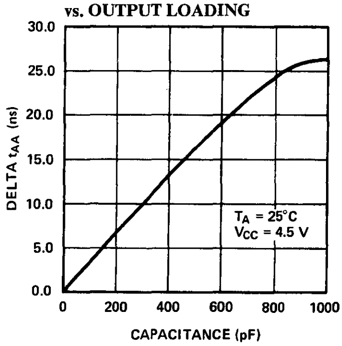
NORMALIZED SETUP TIME vs. TEMPERATURE



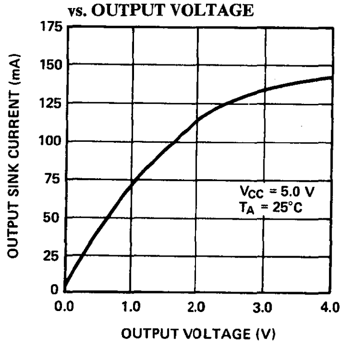
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0005-7

Device Programming

Overview:

There are two independent programmable functions contained in the 7C235 CMOS 1K x 8 Registered PROM; the 1K x 8 array, and the INITIAL BYTE. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally through the use of the initialize function. The 1K x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

		Pin Function						
Mode	**Read or Output Disable**	**A_2**	**CP**	**$\overline{E}_S$**	**$\overline{INIT}$**	**$\overline{E}$**	**A_1**	**Outputs (9–11, 13–17) DIP**
	Other	**A_2**	**$\overline{PGM}$**	**$\overline{VFY}$**	**V_{PP}**	**$\overline{E}$**	**A_1**	
	(DIP) Pin	**(6)**	**(18)**	**(19)**	**(20)**	**(21)**	**(7)**	
Read[2,3]		X	X	V_{IL}	V_{IH}	V_{IL}	X	Data Out
Output Disable[5]		X	X	V_{IH}	V_{IH}	X	X	High Z
Output Disable		X	X	X	V_{IH}	V_{IH}	X	High Z
Initialize[6]		X	X	X	V_{IL}	V_{IL}	X	1025th word
Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	X	Data In
Program Verify[1,4]		X	V_{IHP}	V_{ILP}	V_{PP}	V_{IHP}	X	Data Out
Program Inhibit[1,4]		X	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	X	High Z
Intelligent Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	X	Data In
Program Initial Byte[4]		V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	V_{IHP}	V_{PP}	Data In
Blank Check Ones[1,4]		X	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	X	Ones
Blank Check Zeros[1,4]		X	V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	X	Zeros

Notes:
1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. Pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. Pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.
6. LOW to HIGH clock transition required to enable outputs.

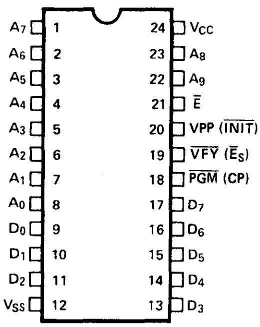


Figure 3. Programming Pinouts

The CY7C235 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

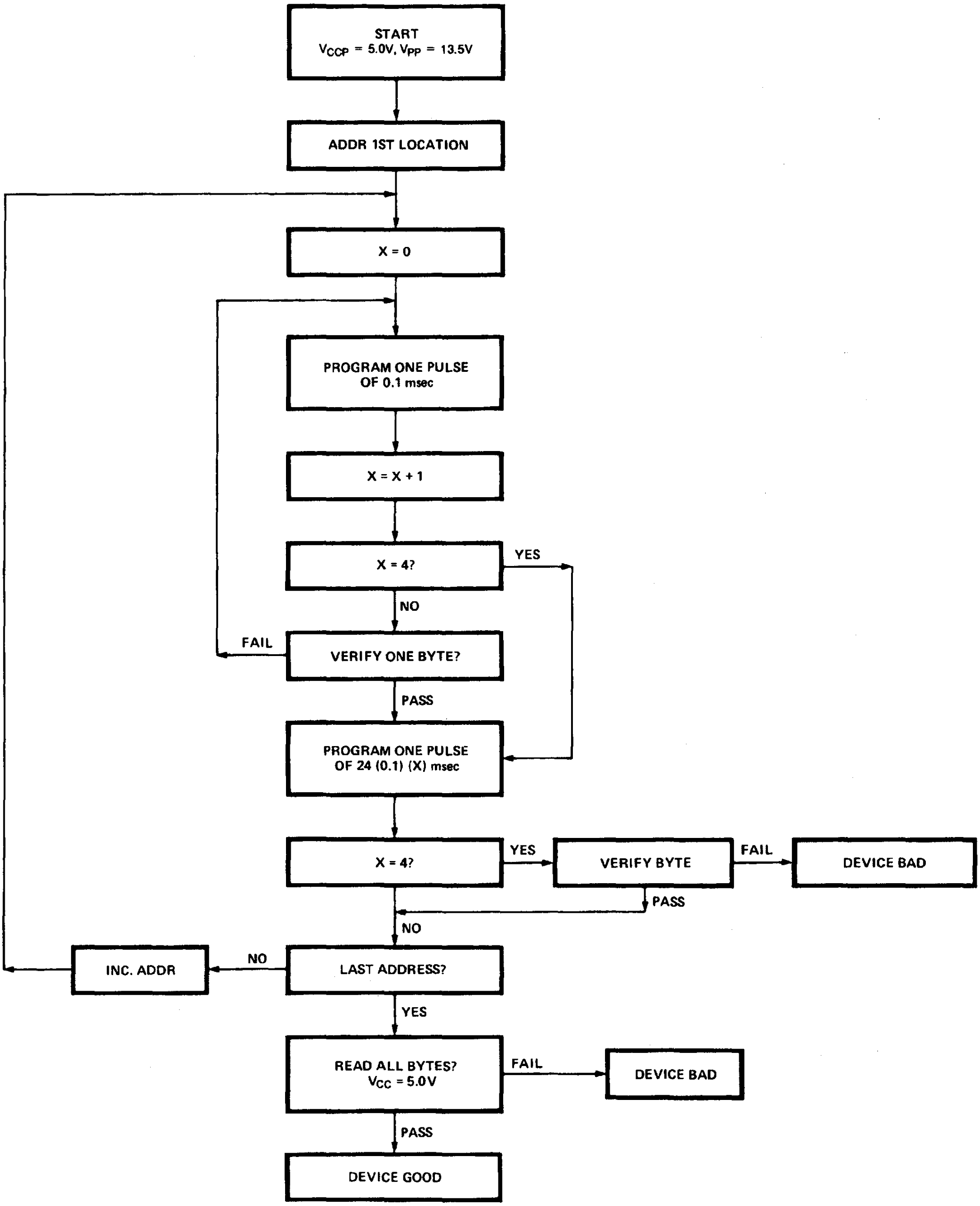


Figure 4. Programming Flowchart

Programming Sequence 1K x 8 Array

Power the device for normal read mode operation with pin 18, 19, 20 and 21 at V_{IH}. Per *Figure 6* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 6* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

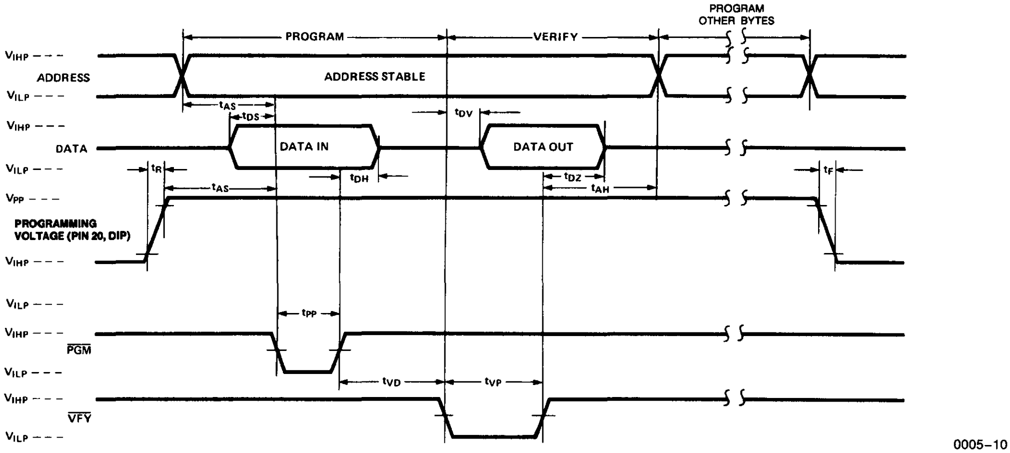


Figure 5. PROM Programming Waveforms

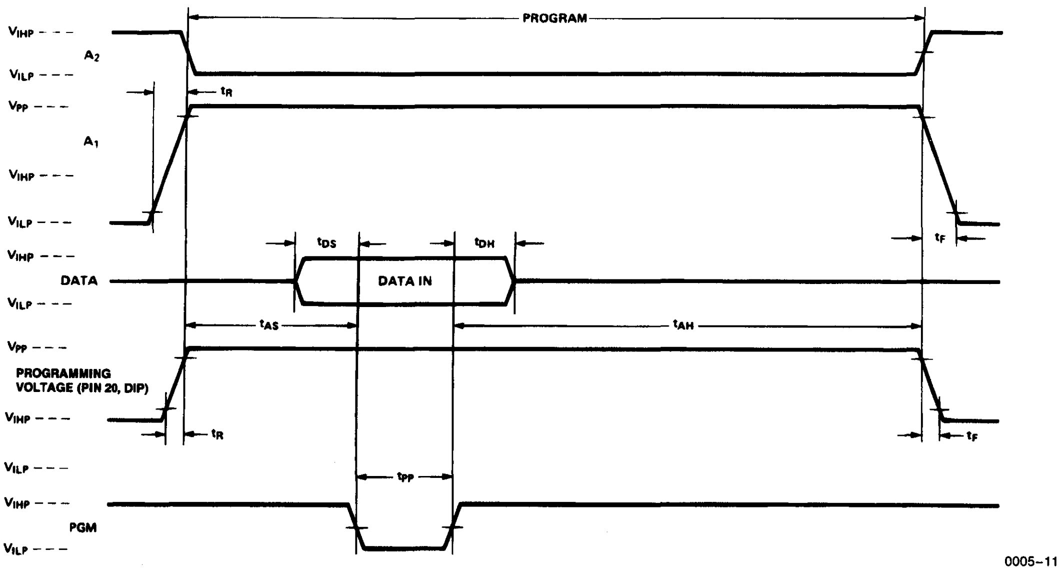


Figure 6. Initial Byte Programming Waveforms

Programming the Initial Byte

The CY7C235 registered PROM has a 1025th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 1025th byte. This byte is programmed in a similar manner to the 1024 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has V_{PP} on A_1 pin 7, and V_{ILP} on A_2, pin 6, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

Bit Map Data

Programmer Address		RAM Data
Decimal	Hex	Contents
0	0	Data
•	•	•
•	•	•
•	•	•
1023	3FF	Data
1024	400	Init Byte

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 1023. A device is considered virgin if all locations are respectively "1's" and "0's" when addresses in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

Ordering Information

Speed ns		Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}			
25	12	CY7C235-25PC	P13	Commercial
		CY7C235-25DC	D14	
30	15	CY7C235-30PC	P13	
		CY7C235-30DC	D14	
		CY7C235-30JC	J64	
		CY7C235-30DMB	D14	Military
		CY7C235-30LMB	L64	
40	20	CY7C235-40PC	P13	Commercial
		CY7C235-40DC	D14	
		CY7C235-40DMB	D14	Military
		CY7C235-40LMB	L64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

3

Switching Characteristics

Parameters	Subgroups
t_{SA}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{CO}	7,8,9,10,11

Document #: 38-00003-B

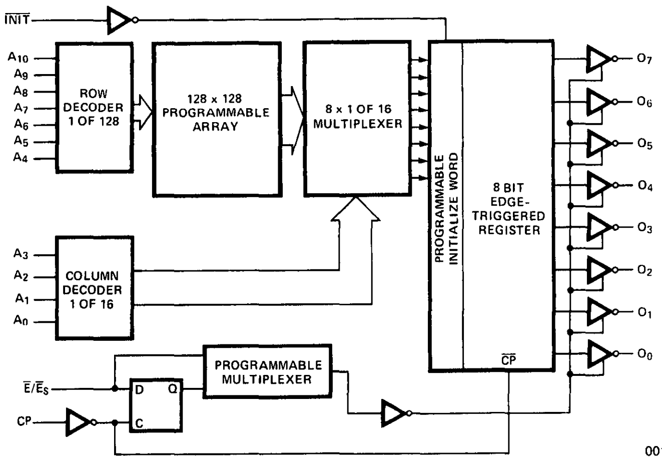
CYPRESS SEMICONDUCTOR

Reprogrammable 2048 x 8 Registered PROM

Features

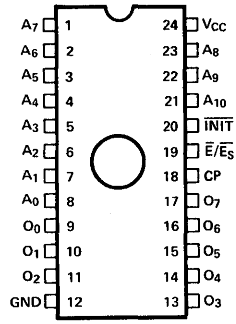
- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - 25 ns max set-up
  - 12 ns clock to output
- Low power
  - 330 mW (commercial) for −35 ns, −45 ns
  - 660 mW (military)
- Programmable synchronous or asynchronous output enable
- On-chip edge-triggered registers
- Programmable asynchronous register ($\overline{\text{INIT}}$)
- EPROM technology, 100% programmable
- Slim, 300 mil, 24 pin plastic or hermetic DIP
- 5V ±10% V_{CC}, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2000V static discharge

Logic Block Diagram

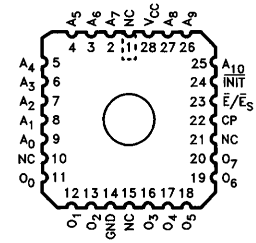


0016–1

Pin Configurations



0016–2



0016–13

Selection Guide

			7C245-25	7C245-35	7C245-45
Maximum Setup Time (ns)			25	35	45
Maximum Clock to Output (ns)			12	15	25
Maximum Operating Current (mA)	STD	Commercial	90	90	90
		Military		120	120
	L	Commercial		60	60

Product Characteristics

The CY7C245 is a high performance 2048 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C245 replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C245 has an asynchronous initialize function ($\overline{\text{INIT}}$). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure......................... 7258 Wsec/cm²

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[7]	−55°C to +125°C	5V ±10%

3

Electrical Characteristics Over Operating Range[6]

Parameters	Description	Test Conditions		7C245L-35, 45 Min.	7C245L-35, 45 Max.	7C245-25 Min.	7C245-25 Max.	7C245-35, 45 Min.	7C245-35, 45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[1]		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[1]			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 5		Note 5						
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[3]		−40	+40	−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[2]		−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = Max.	Commercial		60		90		90	mA
			Military						120	

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4. Tested initially and after any design or process changes that may affect these parameters.
5. The CMOS process does not provide a clamp diode. However, the CY7C245 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
6. See the last page of this specification for Group A subgroup testing information.
7. T_A is the "instant on" case temperature.

Switching Characteristics Over Operating Range[8]

Parameters	Description	7C245-25		7C245-35		7C245-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	25		35		45		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		12		15		25	ns
t_{PWC}	Clock Pulse Width	15		20		20		ns
t_{SES}	$\overline{E}_S$ Setup to Clock HIGH	12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		ns
t_{DI}	Delay from $\overline{\text{INIT}}$ to Valid Output		20		20		35	ns
t_{RI}	$\overline{\text{INIT}}$ Recovery to Clock HIGH	15		20		20		ns
t_{PWI}	$\overline{\text{INIT}}$ Pulse Width	15		20		25		ns
t_{COS}	Valid Output from Clock HIGH[1]		15		20		30	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		15		20		30	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW[2]		15		20		30	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		15		20		30	ns

Notes:

1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b*.
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.
8. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms[5, 6, 7]

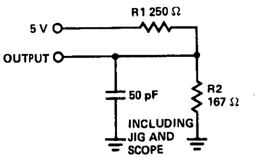
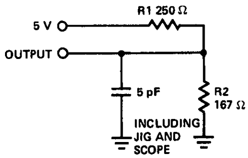
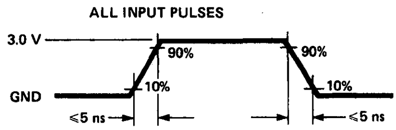


Figure 1a



0016-3

Figure 1b

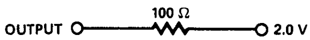


0016-5

Figure 2

Equivalent to:

THÉVENIN EQUIVALENT



0016-4

Functional Description

The CY7C245 is a CMOS electrically Programmable Read Only Memory organized as 2048 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245 incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$) output enable and asynchronous initialization ($\overline{\text{INIT}}$).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ($\overline{E}_S$ or $\overline{E}$). If the synchronous enable ($\overline{E}_S$) has been programmed, the register will be in the set condition causing the outputs (O_0-O_7) to be in the OFF or high impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or high impedance state only if the enable ($\overline{E}$) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A_0-A_{10}) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0-O_7).

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a

Functional Description (Continued)

logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C245 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

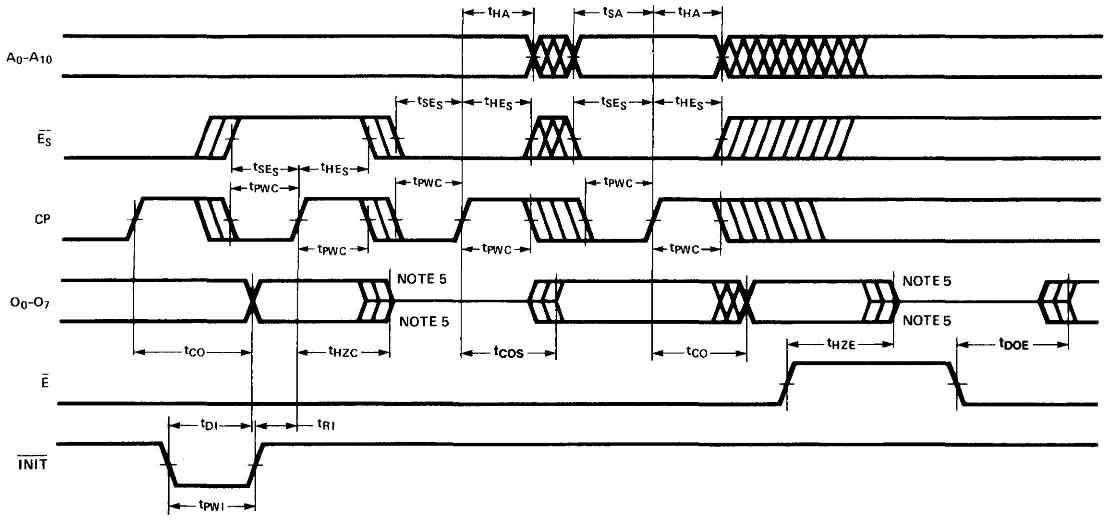
System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245 has an asynchronous initialize input ($\overline{INIT}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

3

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

Switching Waveforms



0016-6

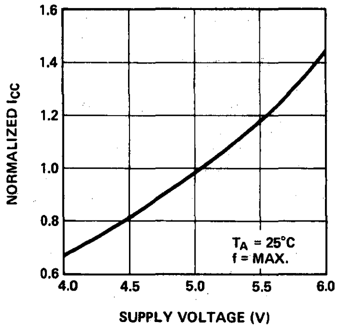
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

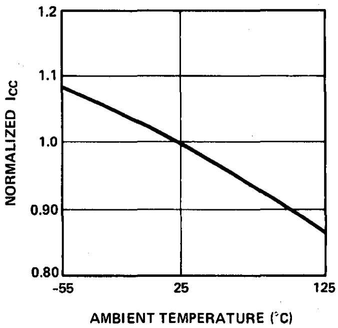
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level − 500 mV or steady state LOW level + 500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b*.

Typical DC and AC Characteristics

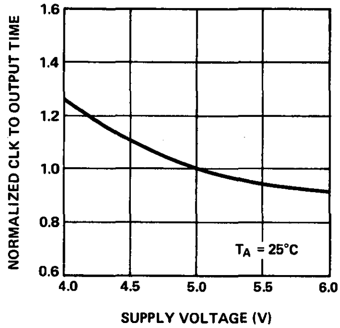
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



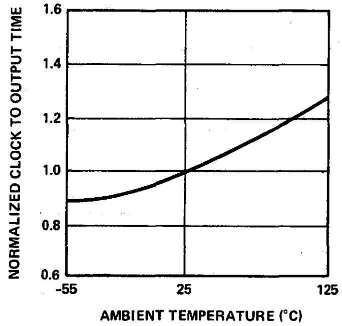
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



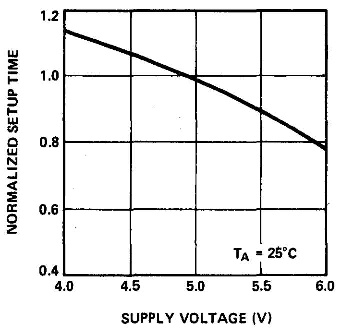
CLOCK TO OUTPUT TIME vs. V_{CC}



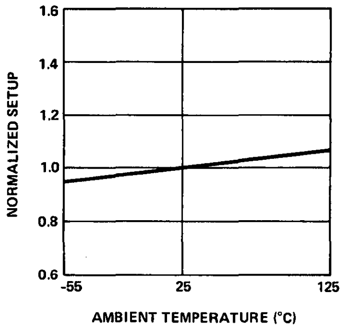
CLOCK TO OUTPUT TIME vs. TEMPERATURE



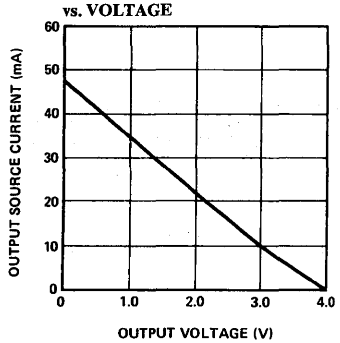
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



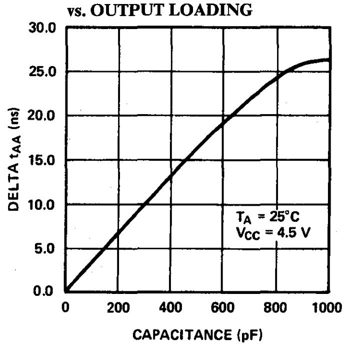
NORMALIZED SETUP TIME vs. TEMPERATURE



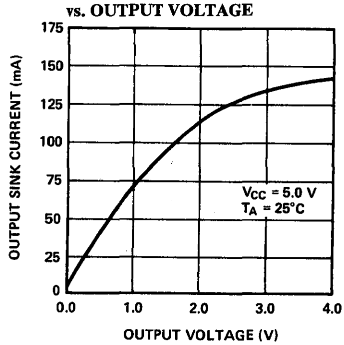
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0016–7

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C245. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating the exposure time would be approximately 30–35 minutes. The 7C245 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm² is the recommended maximum dosage.

Device Programming

OVERVIEW:

There are three independent programmable functions contained in the 7C245 CMOS 2K x 8 Registered PROM; the 2K x 8 array, the initial byte, and the synchronous enable bit. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. This erased state manifests itself differently in each case. The erased state for ENABLE bit is the "ASYNCHRONOUS ENABLE" mode. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally thru the use of the initialize function. The 2K x 8 array uses a differential memory cell, with differential sensing techniques. In the erased state the cell contains neither a one nor a zero. The erased state of this array may be verified by using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see Table 3.

3

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	12.0	13.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

Notes:

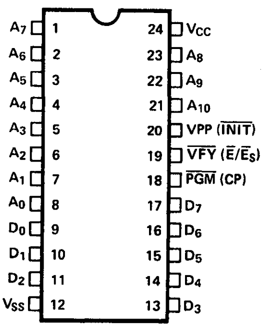
1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function					Outputs (9–11, 13–17)
	Read or Output Disable	A_2	CP	$\overline{E}/\overline{E_S}$	$\overline{INIT}$	A_1	
	Other	A_2	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	A_1	
	Pin	(6)	(18)	(19)	20	(7)	
Read[2,3]		X	X	V_{IL}	V_{IH}	X	Data Out
Output Disable[5]		X	X	V_{IH}	V_{IH}	X	High Z
Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Verify[1,4]		X	V_{IHP}	V_{ILP}	V_{PP}	X	Data Out
Program Inhibit[1,4]		X	V_{IHP}	V_{IHP}	V_{PP}	X	High Z
Intelligent Program[1,4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Synch Enable[4]		V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	High Z
Program Initial Byte[4]		V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	Data In
Blank Check Ones[1,4]		X	V_{PP}	V_{ILP}	V_{ILP}	X	Ones
Blank Check Zeros[1,4]		X	V_{PP}	V_{IHP}	V_{ILP}	X	Zeros

Notes:
1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. If the registered device is being operated in a synchronous mode, pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. If the registered device is being operated in a synchronous mode, pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.



0016–8

Figure 3. Programming Pinouts

The CY7C245 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

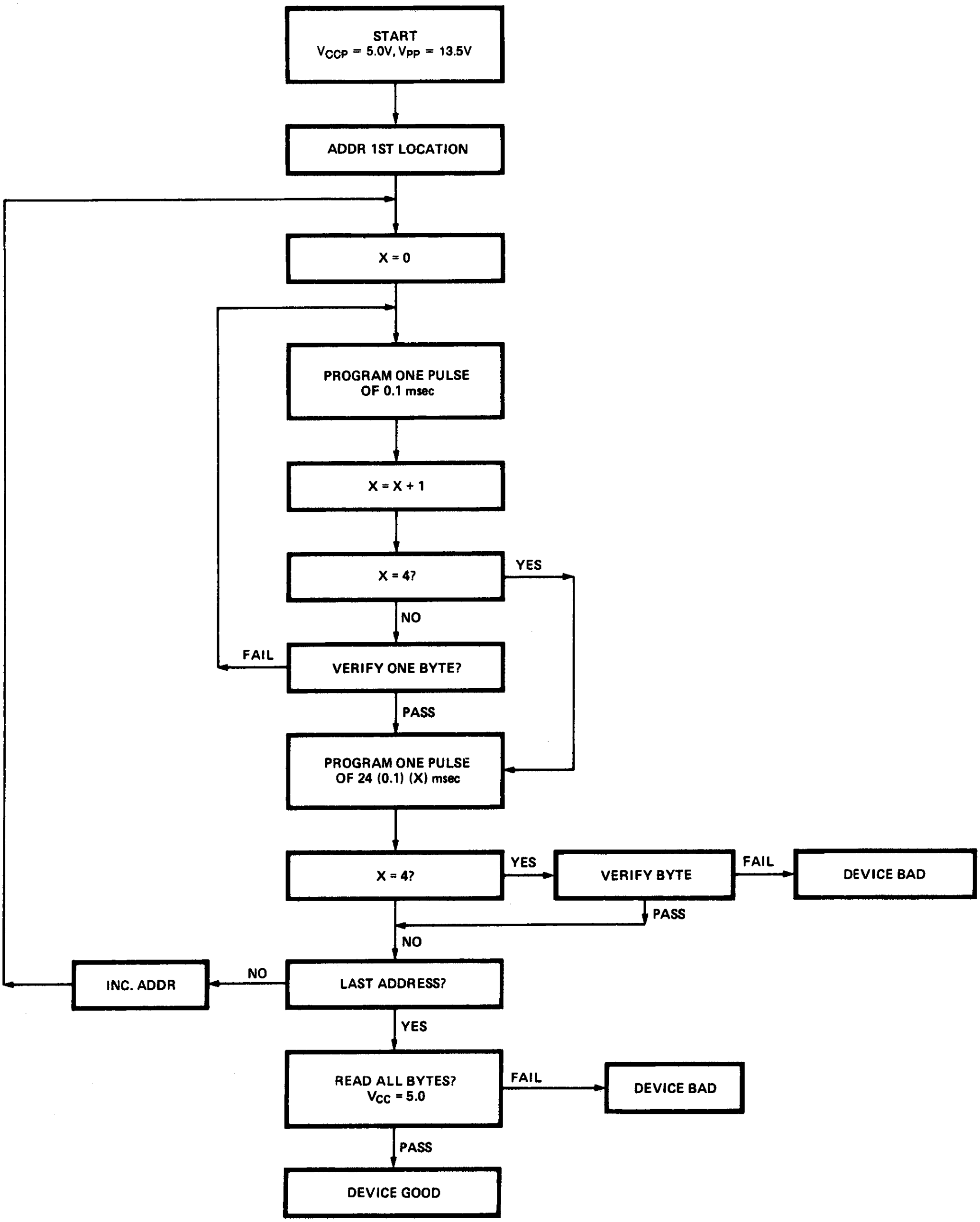
Bit Map Data

Programmer	Address	RAM Data
Decimal	Hex	Contents
0	0	DATA
•	•	•
•	•	•
•	•	•
2047	7FF	DATA
2048	800	INIT BYTE
2049	801	CONTROL BYTE

Control Byte

00 Asynchronous output enable (default state)
01 Synchronous output enable

3



0016–9

Figure 4. Programming Flowchart

Programming Sequence 2K x 8 Array

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24X the sum of the previous programming pulses before advancing to the next address to repeat the process.

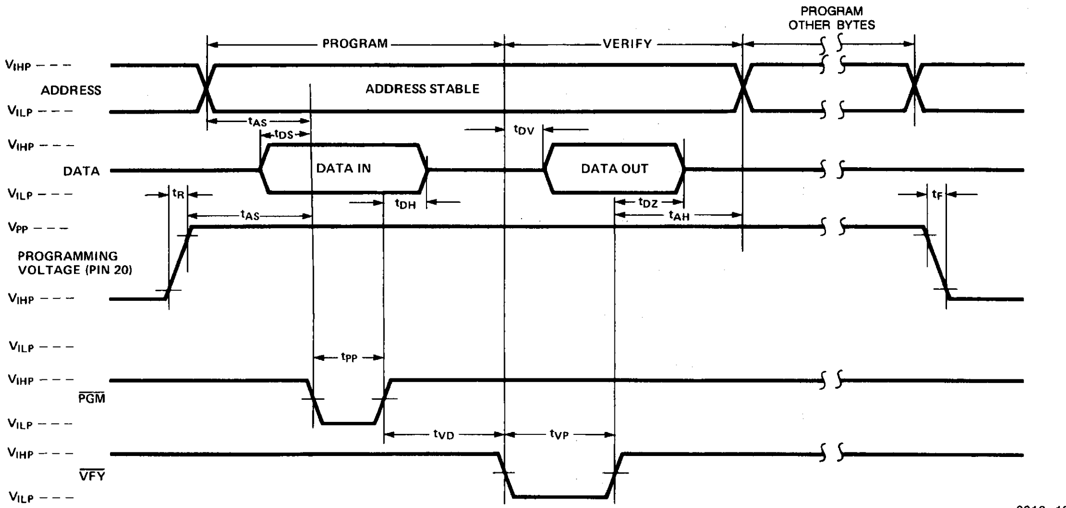


Figure 5. PROM Programming Waveforms

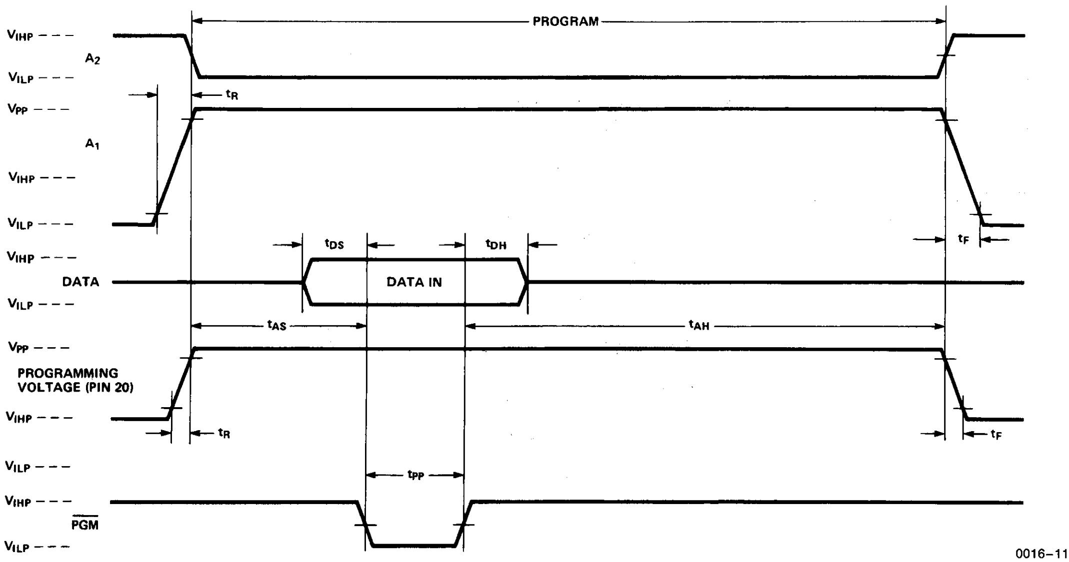


Figure 6. Initial Byte Programming Waveforms

Programming the Initialization Byte

The CY7C245 registered PROM has a 2049th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 2049th byte. This byte is programmed in a similar manner to the 2048 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has V_{PP} on A_1 pin 7, and V_{ILP} on A_2, pin 6, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

Programming Synchronous Enable

The CY7C245 provides for both a synchronous and asynchronous enable function. The device is delivered in an asynchronous mode of operation and only requires that the user alter the device if synchronous operation is required. The determination of the option is accomplished thru the use of an EPROM cell which is programmed only if synchronous operation is required. As with the INITIAL byte, this function is addressed thru the use of a supervoltage. Per Table 3, V_{PP} is applied to pin 7 (A_1) with pin 6 (A_2) at V_{IHP}. This addresses the cell that programs synchronous enable. Programming the cell is accomplished with a 10 ms program pulse on pin 18 ($\overline{PGM}$) but does not require any data as there is no choice as to how synchronous enable may be programmed, only if it is to be programmed.

3

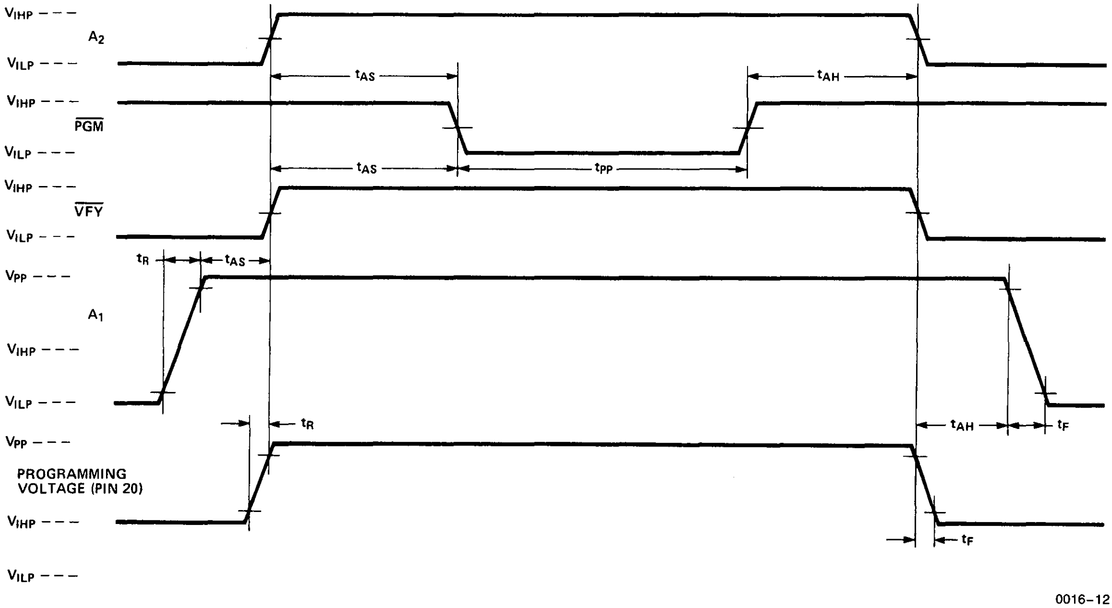


Figure 7. Program Synchronous Enable

Verification of Synchronous Enable

Verification of the synchronous enable function is accomplished operationally. Power the device for read operation with pin 20 at V_{IH}, cause clock pin 18 to transition from V_{IL} to V_{IH}. The output should be in a High Z state. Take pin 20, $\overline{ENABLE}$, to V_{IL}. The outputs should remain in a high Z state. Transition the clock from V_{IL} to V_{IH}, the outputs should now contain the data that is present. Again set pin 19 to V_{IH}. The output should remain driven. Clocking pin 18 once more from V_{IL} to V_{IH} should place the outputs again in a High Z state.

Blank Check

A virgin device contains neither one's nor zero's because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 2047. A device is considered virgin if all locations are respectively "1's" and "0's" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both one's and zero's. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

Ordering Information

Speed (ns)		I_{CC} mA	Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}				
25	12	90	CY7C245-25PC	P13	Commercial
			CY7C245-25WC	W14	
35	15	60	CY7C245L-35PC	P13	Commercial
			CY7C245L-35WC	W14	
		90	CY7C245-35PC	P13	
			CY7C245-35SC	S13	
			CY7C245-35WC	W14	
			CY7C245-35LC	L64	
		120	CY7C245-35DMB	D14	Military
			CY7C245-35QMB	Q64	
			CY7C245-35WMB	W14	
			CY7C245-35LMB	L64	

Speed (ns)		I_{CC} mA	Ordering Code	Package Type	Operating Range
t_{SA}	t_{CO}				
45	25	60	CY7C245L-45PC	P13	Commercial
			CY7C245L-45WC	W14	
		90	CY7C245-45PC	P13	
			CY7C245-45SC	S13	
			CY7C245-45WC	W14	
			CY7C245-45LC	L64	
		120	CY7C245-45WMB	W14	Military
			CY7C245-45LMB	L64	
			CY7C245-45DMB	D14	
			CY7C245-45QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{SA}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{CO}	7,8,9,10,11

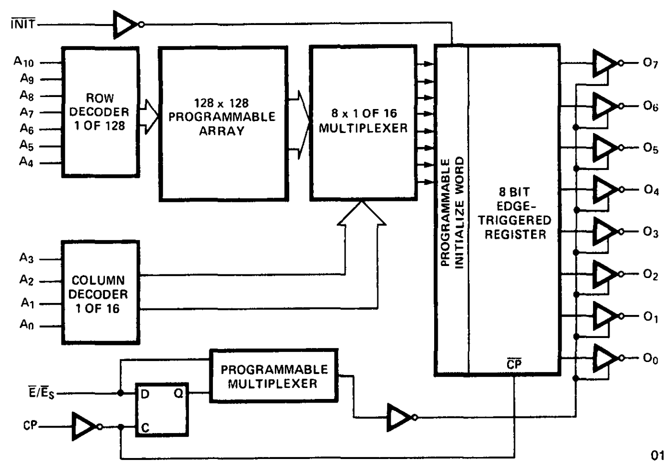
Document #: 38-00004-D

Reprogrammable 2048 x 8 Registered PROM

Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - 15 ns max set-up
  - 10 ns clock to output
- Low power
  - 330 mW (commercial) for −35 ns
  - 660 mW (military)
- Programmable synchronous or asynchronous output enable
- On-chip edge-triggered registers
- Programmable asynchronous register ($\overline{\text{INIT}}$)
- EPROM technology, 100% programmable
- Slim, 300 mil, 24 pin plastic or hermetic DIP
- 5V ±10% V_{CC}, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2000V static discharge

Logic Block Diagram



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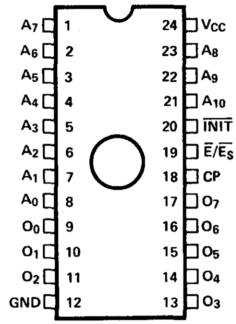
Pin Configurations



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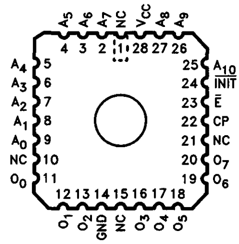

0121-3

Selection Guide

			7C245A-15	7C245A-18	7C245A-25	7C245A-35
Maximum Setup Time (ns)			15	18	25	35
Maximum Clock to Output (ns)			10	12	12	15
Maximum Operating Current (mA)	STD	Commercial	120	120	90	90
		Military		120	120	120
	L	Commercial				60

Product Characteristics

The CY7C245A is a high performance 2048 word by 8 bit electrically Programmable Read Only Memory packaged in a slim 300 mil plastic or hermetic DIP. The ceramic package may be equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C245A replaces bipolar devices and offers the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet AC specification limits.

The CY7C245A has an asynchronous initialize function ($\overline{INIT}$). This function acts as a 2049th 8-bit word loaded into the on-chip register. It is user programmable with any desired word or may be used as a PRESET or CLEAR function on the outputs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12)................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure......................... 7258 Wsec/cm^2

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[4]	−55°C to +125°C	5V ±10%

3

Electrical Characteristics Over Operating Range[7]

Parameters	Description	Test Conditions		7C245A-15, 18		7C245A-25, 35		7C245AL-35		Units
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA V_{IN} = V_{IH} or V_{IL}		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}			0.4		0.4		0.4	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[1]		2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[1]			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
V_{CD}	Input Clamp Diode Voltage	Note 5		Note 5						
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled[3]		−40	+40	−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[2]		−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	GND ≤ V_{IN} ≤ V_{CC} V_{CC} = Max.	Commercial		120		90		60	mA
			Military		120		120			

Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
4. T_A is the "instant on" case temperature.
5. The CMOS process does not provide a clamp diode. However, the CY7C245A is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
6. Tested initially and after any design or process changes that may affect these parameters.
7. See the last page of this specification for Group A subgroup testing information.

Switching Characteristics Over Operating Range[8]

Parameters	Description	7C245A-15		7C245A-18		7C245A-25		7C245A-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{SA}	Address Setup to Clock HIGH	15		18		25		35		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		0		ns
t_{CO}	Clock HIGH to Valid Output		10		12		12		15	ns
t_{PWC}	Clock Pulse Width	10		12		15		20		ns
t_{SE_S}	$\overline{E}_S$ Setup to Clock HIGH	10		10		12		15		ns
t_{HE_S}	$\overline{E}_S$ Hold from Clock HIGH	5		5		5		5		ns
t_{DI}	Delay from $\overline{\text{INIT}}$ to Valid Output		15		20		20		20	ns
t_{RI}	$\overline{\text{INIT}}$ Recovery to Clock HIGH	10		15		15		20		ns
t_{PWI}	$\overline{\text{INIT}}$ Pulse Width	10		15		15		20		ns
t_{COS}	Valid Output from Clock HIGH[1]		15		15		15		20	ns
t_{HZC}	Inactive Output from Clock HIGH[1, 3]		15		15		15		20	ns
t_{DOE}	Valid Output from $\overline{E}$ LOW[2]		12		15		15		20	ns
t_{HZE}	Inactive Output from $\overline{E}$ HIGH[2, 3]		15		15		15		20	ns

Notes:
1. Applies only when the synchronous ($\overline{E}_S$) function is used.
2. Applies only when the asynchronous ($\overline{E}$) function is used.
3. Transition is measured at steady state High level − 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input with loads shown in *Figure 1b.*
4. Tests are performed with rise and fall times of 5 ns or less.
5. See *Figure 1a* for all switching characteristics except t_{HZ}.
6. See *Figure 1b* for t_{HZ}.
7. All device test loads should be located within 2″ of device outputs.
8. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms[4, 5, 6, 7]

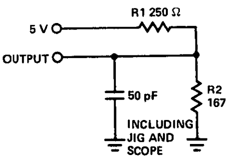

Figure 1a

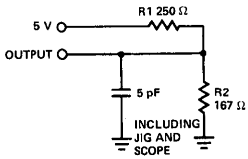

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Figure 1b

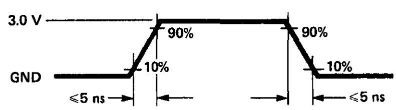

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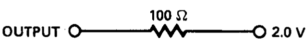
Figure 2

Equivalent to:

THÉVENIN EQUIVALENT



0121-6

Functional Description

The CY7C245A is a CMOS electrically Programmable Read Only Memory organized as 2048 words x 8-bits and is a pin-for-pin replacement for bipolar TTL fusible link PROMs. The CY7C245A incorporates a D-type, master-slave register on chip, reducing the cost and size of pipelined microprogrammed systems and applications where accessed PROM data is stored temporarily in a register. Additional flexibility is provided with a programmable synchronous ($\overline{E}_S$) or asynchronous ($\overline{E}$) output enable and asynchronous initialization ($\overline{\text{INIT}}$).

Upon power-up the state of the outputs will depend on the programmed state of the enable function ($\overline{E}_S$ or $\overline{E}$). If the synchronous enable ($\overline{E}_S$) has been programmed, the register will be in the set condition causing the outputs (O_0–O_7) to be in the OFF or high impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or high impedance state only if the enable ($\overline{E}$) input is at a HIGH logic level. Data is read by applying the memory location to the address inputs (A_0–A_{10}) and a logic LOW to the enable input. The stored data is accessed and loaded into the master flip-flops of the data register during the address set-up time. At the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops, which drive the output buffers, and the accessed data will appear at the outputs (O_0–O_7).

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a

Functional Description (Continued)

logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C245A decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

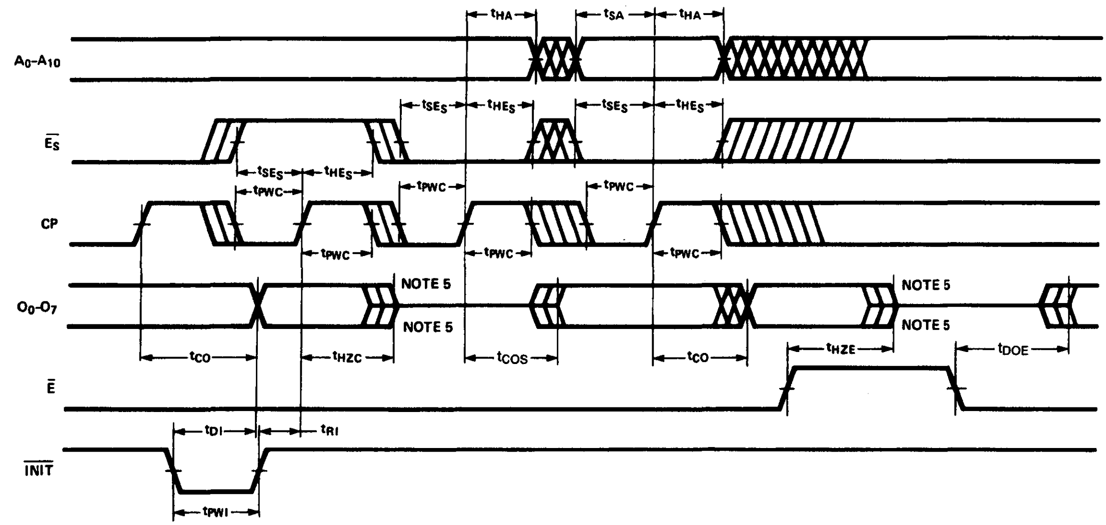
System timing is simplified in that the on-chip edge triggered register allows the PROM clock to be derived directly from the system clock without introducing race conditions. The on-chip register timing requirements are similar to those of discrete registers available in the market.

The CY7C245A has an asynchronous initialize input ($\overline{\text{INIT}}$). The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 2049th 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating $\overline{\text{INIT}}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{\text{INIT}}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{\text{INIT}}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register, independent of all other inputs, including the clock (CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

3

Switching Waveforms



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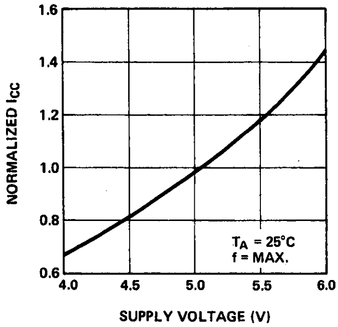
Notes on Testing

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

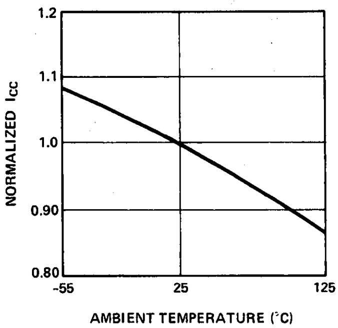
1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level −500 mV or steady state LOW level + 500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b.*

Typical DC and AC Characteristics

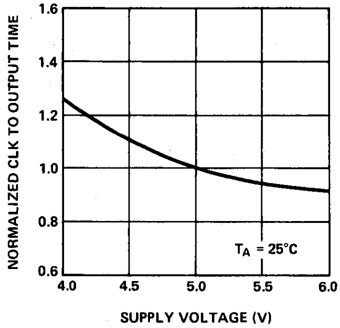
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



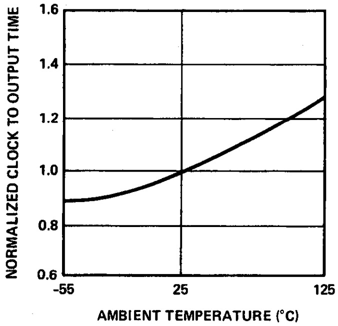
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



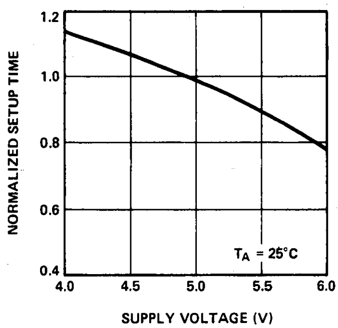
CLOCK TO OUTPUT TIME vs. V_{CC}



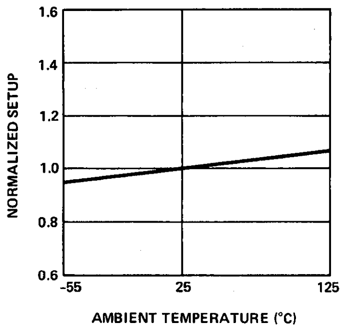
CLOCK TO OUTPUT TIME vs. TEMPERATURE



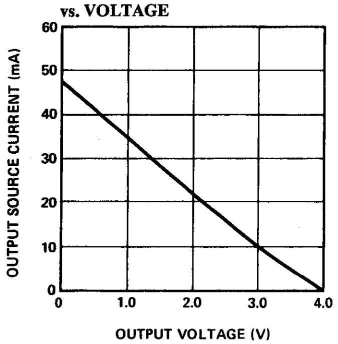
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



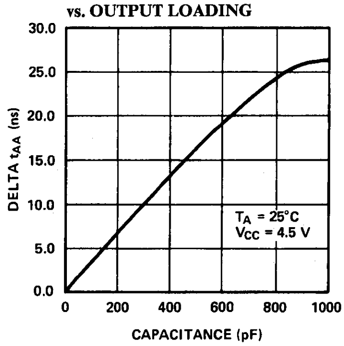
NORMALIZED SETUP TIME vs. TEMPERATURE



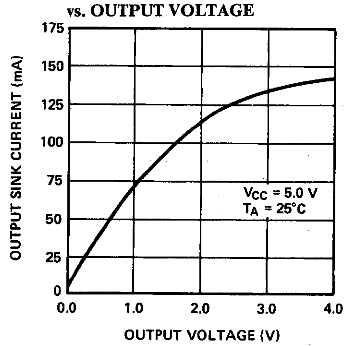
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0121–9

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C245A. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 30–35 minutes. The 7C245A needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Device Programming

OVERVIEW:

There are three independent programmable functions contained in the 7C245A CMOS 2K x 8 Registered PROM; the 2K x 8 array, the initial byte, and the synchronous enable bit. All of the programming elements are "EPROM" cells, and are in an erased state when the device is shipped. This erased state manifests itself differently in each case. The erased state for ENABLE bit is the "ASYNCHRONOUS ENABLE" mode. The erased state for the "INITIAL BYTE" is all "0's" or "LOW". The "INITIAL BYTE" may be accessed operationally thru the use of the initialize function. The erased state for the 2K x 8 array is all "0's" or "LOW".

DC Programming Parameters T_A = 25°C

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	12.0	13.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0		V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters T_A = 25°C

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	200	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify HIGH to High Z		1.0	μs

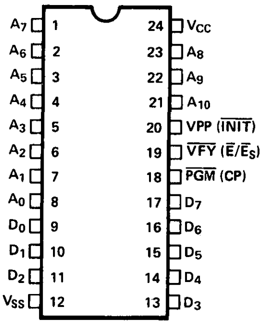
Notes:
1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function[1]					Outputs (9–11, 13–17)
	Read or Output Disable	A_3	CP	$\overline{E}/\overline{E_S}$	$\overline{INIT}$	A_0	
	Other	A_3	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	A_0	
	Pin	(5)	(18)	(19)	20	(8)	
Read[2,3]		X	X	V_{IL}	V_{IH}	X	Data Out
Output Disable[5]		X	X	V_{IH}	V_{IH}	X	High Z
Program[4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Verify[4]		X	V_{IHP}	V_{ILP}	V_{PP}	X	Data Out
Program Inhibit[4]		X	V_{IHP}	V_{IHP}	V_{PP}	X	High Z
Intelligent Program[4]		X	V_{ILP}	V_{IHP}	V_{PP}	X	Data In
Program Synch Enable[4]		V_{IHP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	High Z
Program Initial Byte[4]		V_{ILP}	V_{ILP}	V_{IHP}	V_{PP}	V_{PP}	Data In

Notes:
1. X = Don't care but not to exceed V_{PP}.
2. During read operation, the output latches are loaded on a "0" to "1" transition of CP.
3. If the registered device is being operated in a synchronous mode, pin 19 must be LOW prior to the "0" to "1" transition on CP (18) that loads the register.
4. During programming and verification, all unspecified pins to be at V_{ILP}.
5. If the registered device is being operated in a synchronous mode, pin 19 must be HIGH prior to the "0" to "1" transition on CP (18) that loads the register.



0121-10

Figure 3. Programming Pinouts

The CY7C245A programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the $\overline{PGM}$ pulse (t_{PP}) is 0.2 msec which will then be followed by a longer overprogram pulse of 4 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.2 msec pulses applied before verification occurs. Up to ten 0.2 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

Bit Map Data

Programmer Address		RAM Data
Decimal	Hex	Contents
0	0	DATA
•	•	•
•	•	•
•	•	•
2047	7FF	DATA
2048	800	INIT BYTE
2049	801	CONTROL BYTE

Control Byte

00 Asynchronous output enable (default state)
01 Synchronous output enable

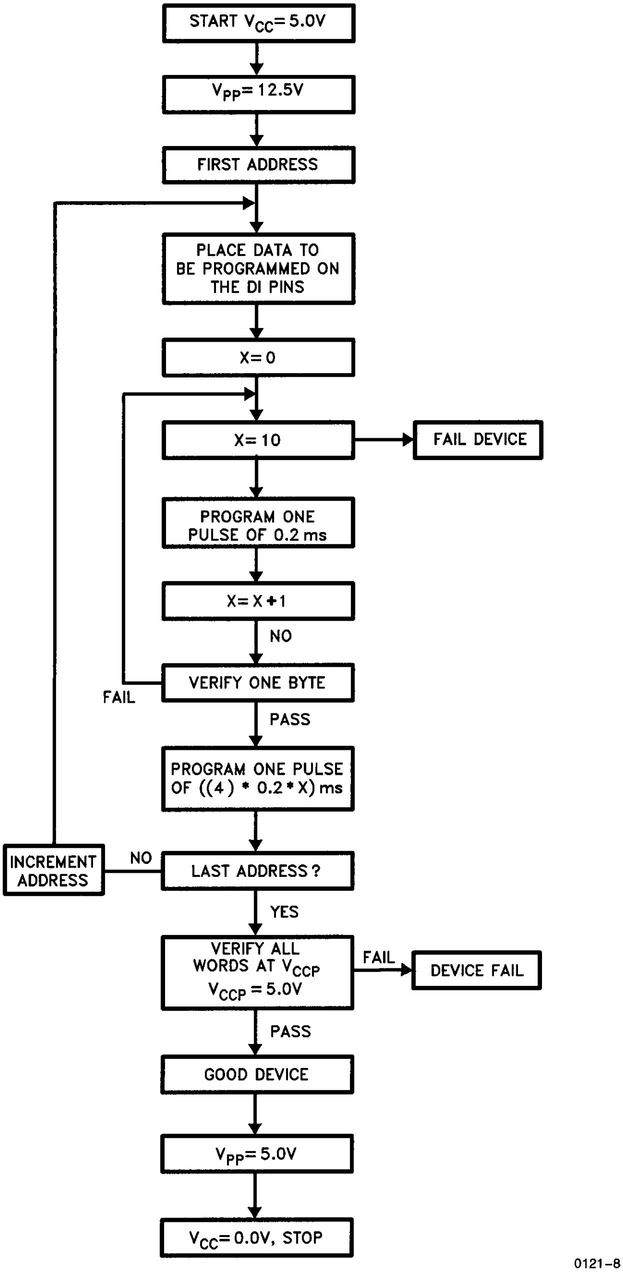


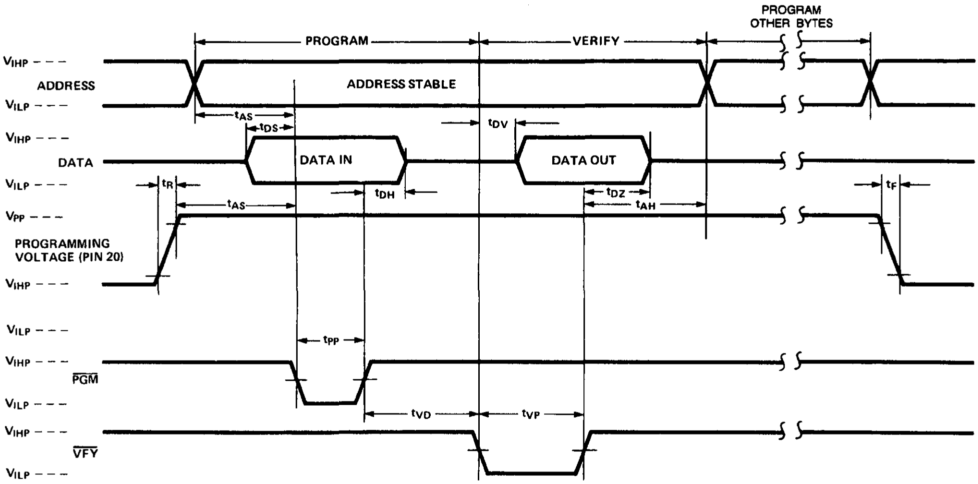
Figure 4. Programming Flowchart

Programming Sequence 2K x 8 Array

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see *Figures 5* and *6*. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

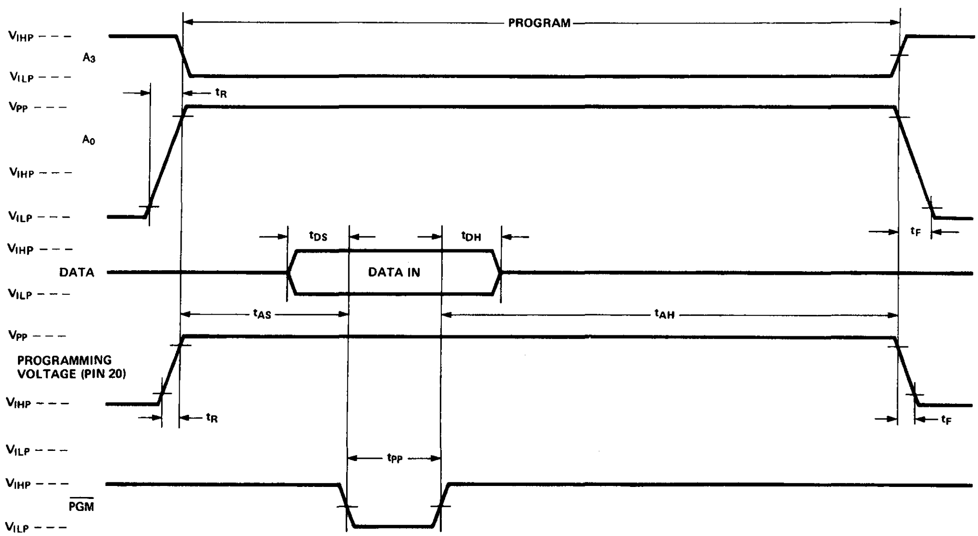
If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 200 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 10 times. When the location verifies, one additional programming pulse should be applied of duration 4X the sum of the previous programming pulses before advancing to the next address to repeat the process.



0121-11

Figure 5. PROM Programming Waveforms



0121-12

Figure 6. Initial Byte Programming Waveforms

Programming the Initialization Byte

The CY7C245A registered PROM has a 2049th byte of data used to initialize the value of the register. This initial byte is value "0" when the part is received. If the user desires to have a value other than "0" for register initialization, this must be programmed into the 2049th byte. This byte is programmed in a similar manner to the 2048 normal bytes in the array except for two considerations. First, since all of the normal addresses of the part are used up, a super voltage will be used to create additional effective addresses. The actual address has V_{PP} on A_0 pin 8, and V_{ILP} on A_3, pin 5, per Table 3. The programming and verification of "INITIAL BYTE" is accomplished operationally by performing an initialize function.

Programming Synchronous Enable

The CY7C245A provides for both a synchronous and asynchronous enable function. The device is delivered in an asynchronous mode of operation and only requires that the user alter the device if synchronous operation is required. The determination of the option is accomplished thru the use of an EPROM cell which is programmed only if synchronous operation is required. As with the INITIAL byte, this function is addressed thru the use of a supervoltage. Per Table 3, V_{PP} is applied to pin 8 (A_0) with pin 5 (A_3) at V_{IHP}. This addresses the cell that programs synchronous enable. Programming the cell is accomplished with a 10 ms program pulse on pin 18 ($\overline{PGM}$) but does not require any data as there is no choice as to how synchronous enable may be programmed, only if it is to be programmed.

3

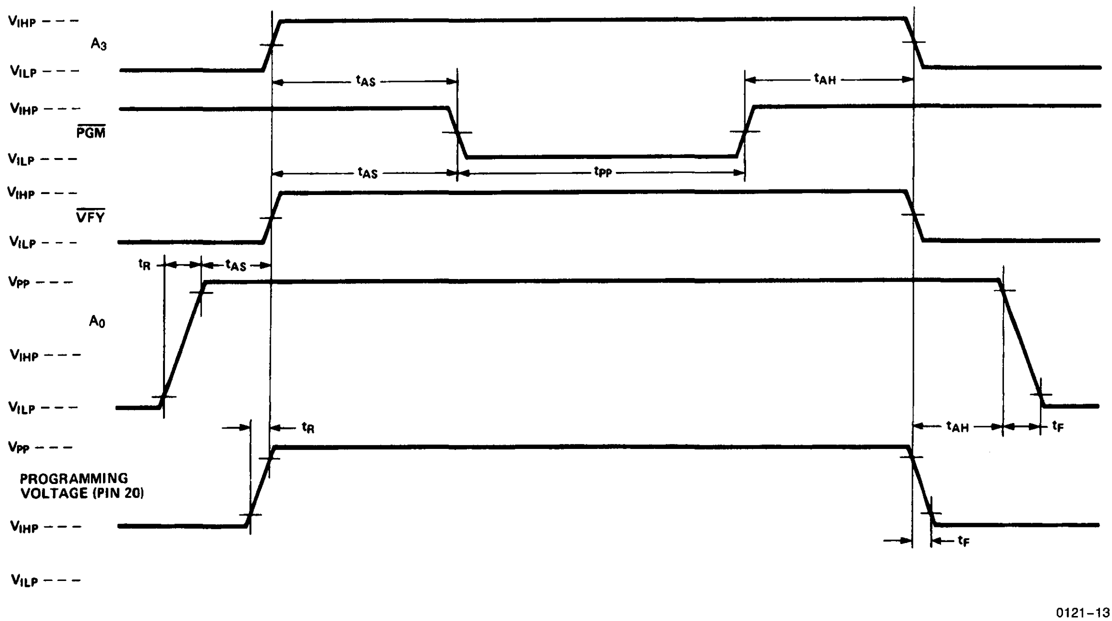


Figure 7. Program Synchronous Enable

Verification of Synchronous Enable

Verification of the synchronous enable function is accomplished operationally. Power the device for read operation with pin 20 at V_{IH}, cause clock pin 18 to transition from V_{IL} to V_{IH}. The output should be in a High Z state. Take pin 20, $\overline{ENABLE}$, to V_{IL}. The outputs should remain in a high Z state. Transition the clock from V_{IL} to V_{IH}, the outputs should now contain the data that is present. Again set pin 19 to V_{IH}. The output should remain driven. Clocking pin 18 once more from V_{IL} to V_{IH} should place the outputs again in a High Z state.

Blank Check

A virgin device contains all zeros. To blank check this PROM, use the verify mode to read locations 0 thru 2047. A device is considered virgin if all locations are "0's" when addressed.

Ordering Information

Speed (ns) t_{SA}	Speed (ns) t_{CO}	I_{CC} mA	Ordering Code	Package Type	Operating Range
15	10	120	CY7C245A-15PC	P13	Commercial
			CY7C245A-15WC	W14	
18	12	120	CY7C245A-18PC	P13	Commercial
			CY7C245A-18WC	W14	
			CY7C245A-18DMB	D14	Military
			CY7C245A-18QMB	Q64	
			CY7C245A-18WMB	W14	
			CY7C245A-18LMB	L64	
25	15	90	CY7C245A-25PC	P13	Commercial
			CY7C245A-25SC	S13	
			CY7C245A-25WC	W14	
			CY7C245A-25LC	L64	
		120	CY7C245A-25DMB	D14	Military
			CY7C245A-25QMB	Q64	
			CY7C245A-25WMB	W14	
			CY7C245A-25LMB	L64	

Speed (ns) t_{SA}	Speed (ns) t_{CO}	I_{CC} mA	Ordering Code	Package Type	Operating Range
35	20	60	CY7C245AL-35PC	P13	Commercial
			CY7C245AL-35WC	W14	
		90	CY7C245A-35PC	P13	
			CY7C245A-35SC	S13	
			CY7C245A-35WC	W14	
			CY7C245A-35LC	L64	
		120	CY7C245A-35WMB	W14	Military
			CY7C245A-35LMB	L64	
			CY7C245A-35DMB	D14	
			CY7C245A-35QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

3

Switching Characteristics

Parameters	Subgroups
t_{SA}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{CO}	7,8,9,10,11

Document #: 38-00004-B

CY7C251
CY7C254

CYPRESS SEMICONDUCTOR

16,384 x 8 PROM Power Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 45 ns (commercial)**
  - **— 55 ns (military)**
- **Low power**
  - **— 550 mW (commercial)**
  - **— 660 mW (military)**
- **Super low standby power (7C251)**
  - **— Less than 165 mW when deselected**
  - **— Fast access: 50 ns**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

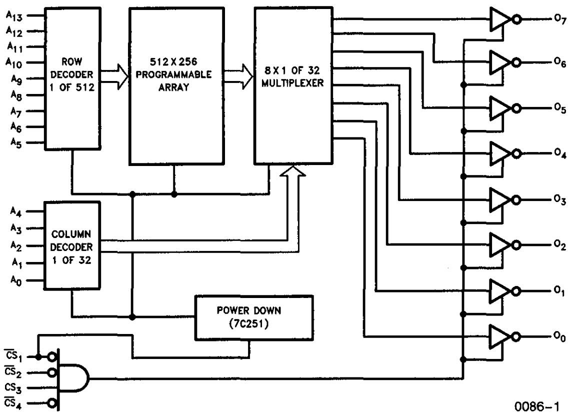
Product Characteristics

The CY7C251 and CY7C254 are high performance 16,384 word by 8 bit CMOS PROMs. When deselected, the 7C251 automatically powers down into a low power stand-by mode. It is packaged in the 300 mil wide package. The 7C254 is packaged in 600 mil wide packages and does not power down when deselected. The 7C251 and 7C254 reprogrammable CERDIP packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C251 and CY7C254 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing all four chip selects in their active states. The contents of the memory location addressed by the address lines (A_0–A_{13}) will become available on the output lines (O_0–O_7).

Logic Block Diagram



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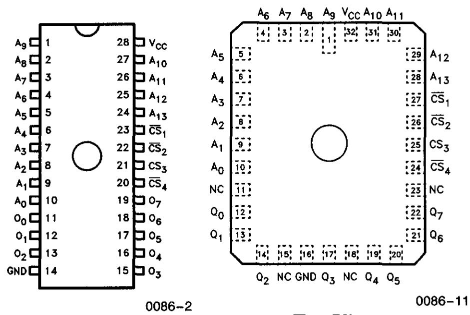
Pin Configurations



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0086-11

Top View

Selection Guide

		7C251-45 7C254-45	7C251-55 7C254-55	7C251-65 7C254-65
Maximum Access Time (ns)		45	55	65
Maximum Operating Current (mA)	Commercial	100	100	100
	Military		120	120
Standby Current (mA) (7C251 only)	Commercial	30	30	30
	Military		35	35

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pin 22) 13.5V

Static Discharge Voltage ....>2001V (per MIL-STD-883, Method 3015)

Latchup Current ....>200 mA

UV Exposure ....7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[5]	−55°C to +125°C	5V ±10%

3

Electrical Characteristics Over the Operating Range[6]

Parameters	Description	Test Conditions		7C251-45 7C254-45 Min.	7C251-45 7C254-45 Max.	7C251-55,65 7C254-55,65 Min.	7C251-55,65 7C254-55,65 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.5		0.5	V
V_{IH}	Input HIGH Level[1]			2.0		2.0		V
V_{IL}	Input LOW Level[1]				0.8		0.8	V
I_{IX}	Input Current	GND ≥ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		Note 2		
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V I_{OUT} = 0 mA	Commercial		100		100	mA
			Military				120	mA
I_{SB}	Standby Supply Current (7C251)	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH} I_{OUT} = 0 mA	Commercial		30		30	mA
			Military				35	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C251 and CY7C254 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. T_A is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.

Switching Characteristics Over the Operating Range[6, 7]

Parameters	Description	7C251-45 7C254-45		7C251-55 7C254-55		7C251-65 7C254-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		45		55		65	ns
t_{HZCS_1}	Chip Select Inactive to High Z[8, 9]		25		30		35	ns
t_{HZCS_2}	Chip Select Inactive to High Z (7C251, $\overline{CS}_1$ Only)[8]		50		60		70	ns
t_{ACS_1}	Chip Select Active to Output Valid[9]		25		30		35	ns
t_{ACS_2}	Chip Select Active to Output Valid (7C251, $\overline{CS}_1$ Only)		50		60		70	ns
t_{PU}	Chip Select Active to Power Up (7C251)	0		0		0		ns
t_{PD}	Chip Select Inactive to Power Down (7C251)		50		60		70	ns

AC Test Loads and Waveforms

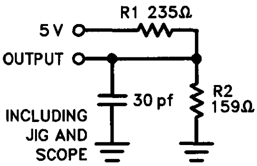

Figure 1a

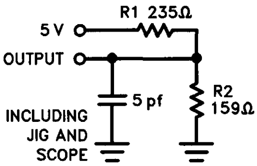

Figure 1b

0086-4

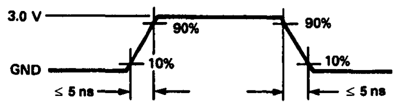

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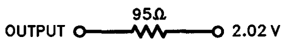
Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



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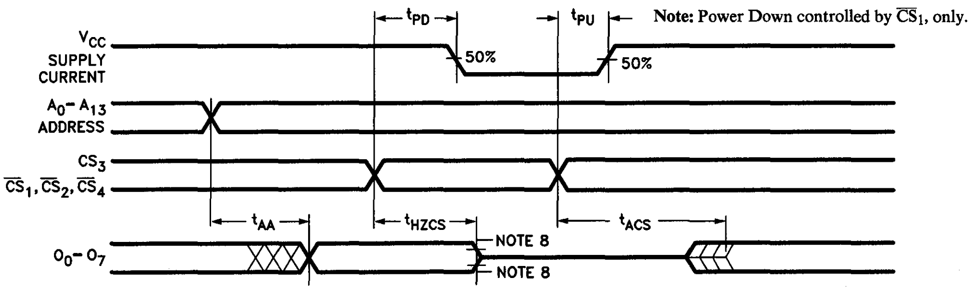


0086-7

Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*
8. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input.
9. t_{HZCS_1} and t_{ACS_1} refers to 7C254 (all chip selects); and 7C251 ($\overline{CS}_2$, CS_3 and $\overline{CS}_4$ only).

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C251 and 7C254 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C251 or 7C254 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W×sec/cm^2 is the recommended maximum dosage.

Device Programming

The CY7C251 and CY7C254 all program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 128K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

Programming Pinout

The Programming Pinout of all three devices are shown in Figure 3 below, and are identical. The programming mode is entered by raising the pin 22 to V_{PP}. The addressed location is programmed and verified with the application of a $\overline{PGM}$ and $\overline{VFY}$ pulse applied to pins 23 and 21 respectively. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.

Programming And Blankcheck

Blankcheck

Blankcheck is accomplished by performing a verify cycle ($\overline{VFY}$ toggles on each address), sequencing through all memory address locations, where all the data read will be "0"s.

Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing V_{PP} on pin 22. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location, placing the data to be programmed into a location on the data pins, and clocking the $\overline{PGM}$ signal from V_{IHP} to V_{ILP} and back to V_{IHP} with a pulse width of 200 μs. The data is removed from the data pins and the content of the location is then verified by taking the $\overline{VFY}$ signal from V_{IHP} to V_{ILP}, comparing the output with the desired data and then returning $\overline{VFY}$ to V_{IHP}. If the contents are correct, a second overprogram pulse of 4 times the original 200 μs is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200 μs pulse is applied to $\overline{PGM}$ with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed. After all locations are programmed, they should be verified at V_{CCP} = 5.0V.

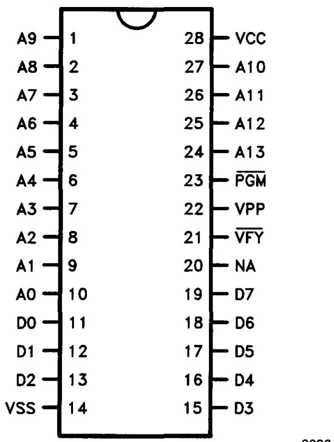


Figure 3. Programming Pinout (DIP Package)

Operating Modes

Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 14 bit field, 4 chip select bits, and the contents of the addressed location appear on the data out pins.

Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage V_{PP} on pin 22. Pin 23 becomes an active LOW program ($\overline{PGM}$) signal and pin 21 becomes an active LOW verify ($\overline{VFY}$) signal. Pins 21 and 23 should never be active LOW at the same time. The PROGRAM mode exists when $\overline{PGM}$ is LOW, and $\overline{VFY}$ is HIGH. The VERIFY mode exists when the reverse is true, $\overline{PGM}$ HIGH and $\overline{VFY}$ LOW and the PROGRAM INHIBIT mode is entered with both $\overline{PGM}$ and $\overline{VFY}$ HIGH. PROGRAM INHIBIT is specifically provided to allow data to be placed on and removed from the data pins without conflict.

Blankcheck

Blankcheck mode is identical to PROGRAM VERIFY and is entered in the same manner as described above.

Programming Sequence

The flowchart in Figure 4 is a detailed description of the intelligent programming cycle used to program the devices covered in this specification. Of particular importance are the areas of power sequencing used to enter and exit the programming operation. This flowchart combined with the timing diagrams AC and DC parameters accurately describe this complete operation.

The timing diagram in Figure 5 contains all of the timing information necessary for describing the relations required for programming the devices covered in this specification. Some of the information pertains to each cycle of programming as specified in Figure 4, and some pertains only to entry and exit from the programming mode of operation.

T_P, T_{PD} and T_{HP} refer to the entry and exit from the programming mode of operation. Note that this is referenced to $\overline{PGM}$ and $\overline{VFY}$ operations.

T_{DS}, T_{AS}, T_{AH} and T_{DH} refer to the required setup and hold times for the address and data for $\overline{PGM}$ and $\overline{VFY}$ operations. These parameters must be adhered to, in all operations, including V_{FY}. This precludes the option then of verifying the device by holding the V_{FY} signal LOW, and sequencing the addresses.

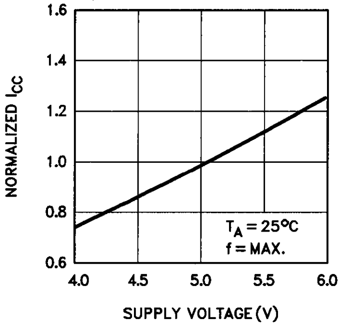
Table 1. Operating Modes

Mode		Pin Function				Outputs (11–13, 15–19)
	Read or Output Disable	$\overline{CS}_4$	CS_3	$\overline{CS}_2$	$\overline{CS}_1$	
	Other	N/A	$\overline{VFY}$	V_{PP}	$\overline{PGM}$	
	Pin Number	(20)	(21)	(22)	(23)	
Read		V_{IL}	V_{IH}	V_{IL}	V_{IL}	Data Out
Output Disable[1]		X	X	X	V_{IH}	High Z
Output Disable[1]		X	X	V_{IH}	X	High Z
Output Disable[1]		X	V_{IL}	X	X	High Z
Output Disable[1]		V_{IH}	X	X	X	High Z
Program		X	V_{IHP}	V_{PP}	V_{ILP}	Data In
Program Verify		X	V_{ILP}	V_{PP}	V_{IHP}	Data Out
Program Inhibit		X	V_{IHP}	V_{PP}	V_{IHP}	High Z
Blank Check		X	V_{ILP}	V_{PP}	V_{IHP}	Data Out

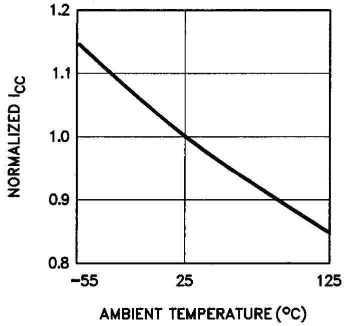
Note:
1. X = Don't care but not to exceed V_{CC} + 5%.

Typical AC and DC Characteristics

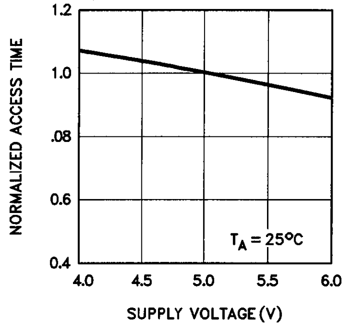
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



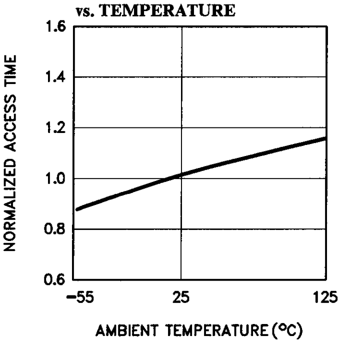
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



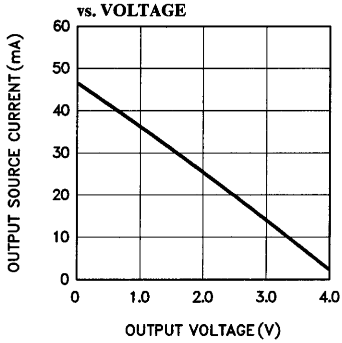
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



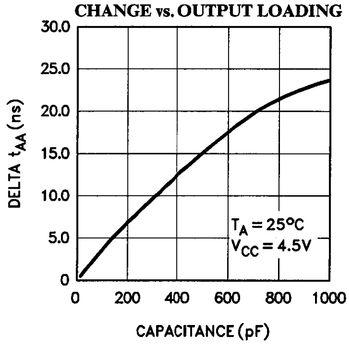
NORMALIZED ACCESS TIME vs. TEMPERATURE



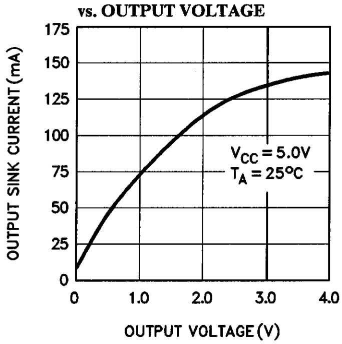
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0086–12

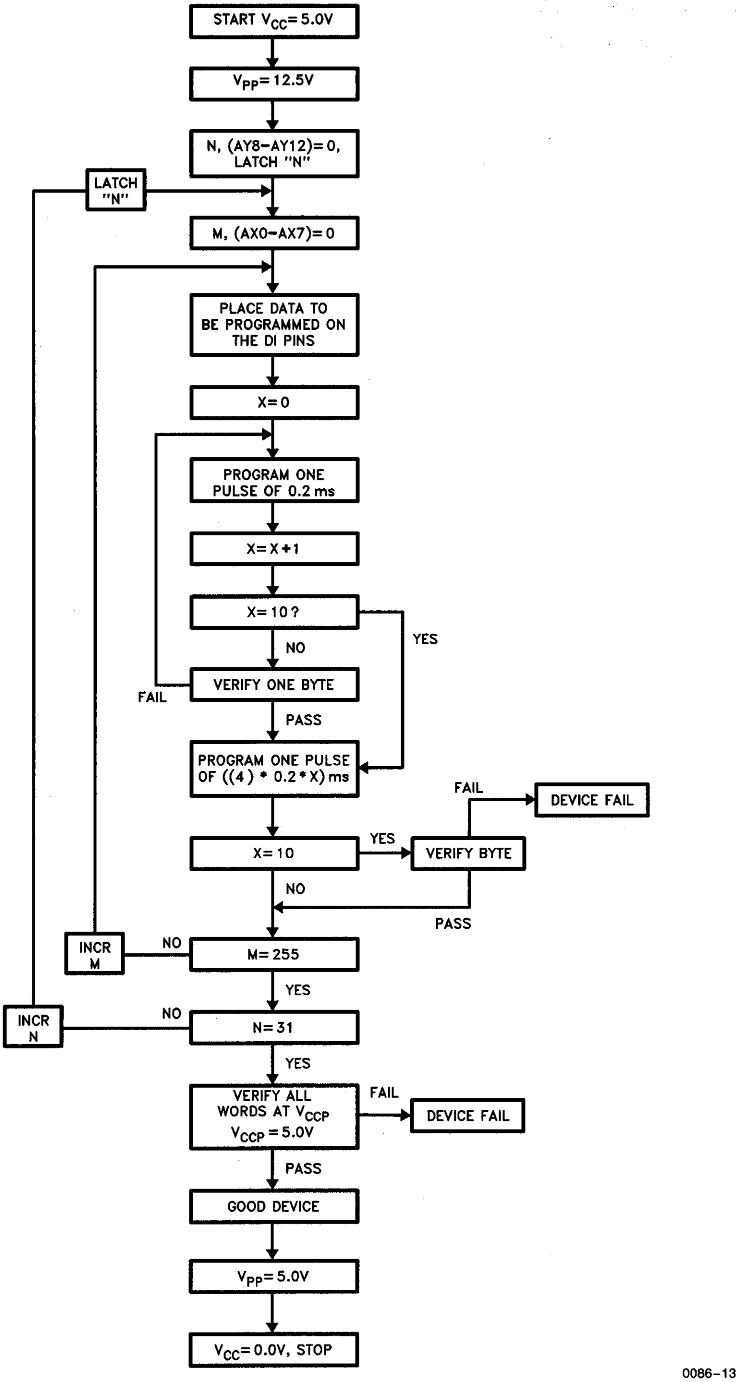


Figure 4. Programming Flowchart

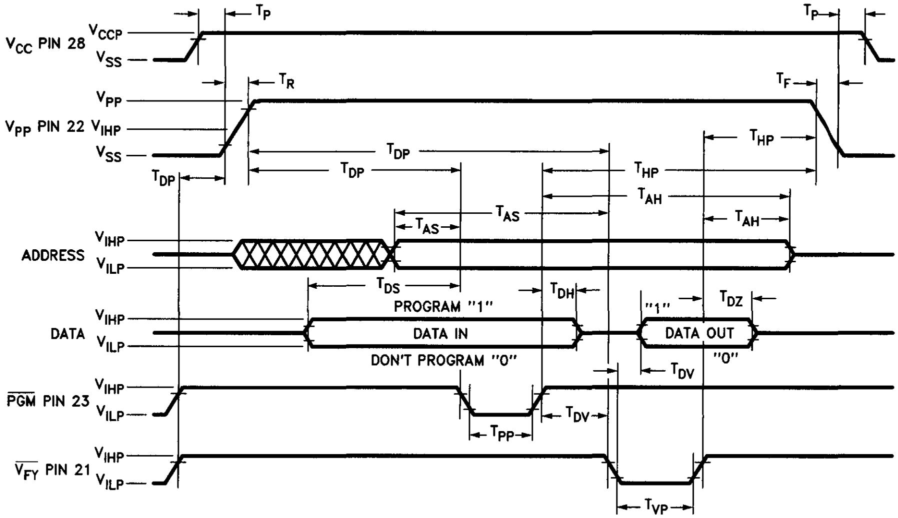


Figure 5. Programming Waveforms

Note: Power, V_{PP} and V_{CC} should not be cycled for each program verify cycle but remain static during programming.

Table 2. DC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	12.0	13.0	V
V_{CCP}	Power Supply Voltage During Programming	4.75	5.25	V
I_{PP}	V_{PP} Supply Current		50	mA
V_{IHP}	Input High Voltage During Programming	3.0	V_{CCP}	V
V_{ILP}	Input Low Voltage During Programming	−3.0	0.4	V
V_{OH}	Output High Voltage	2.4		V
V_{OL}	Output Low Voltage		0.4	V

Table 3. AC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
t_{AS}	Address Setup Time to $\overline{PGM}/\overline{VFY}$	1.0		μs
t_{AH}	Address Hold Time from $\overline{PGM}/\overline{VFY}$	1.0		μs
t_{DS}	Data Setup Time to $\overline{PGM}$	1.0		μs
t_{DH}	Data Hold Time $\overline{PGM}$	1.0		μs
t_{PP}	Program Pulse Width	0.2	10	ms
$t_{R, F}$	V_{PP} Rise and Fall Time	100		ns
t_{DV}	Delay to Verify	1.0		μs
t_{VD}	Verify to Data Out		1.0	μs
t_{VH}	Data Hold Time from Verify		1.0	μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DZ}	Verify to High Z		1.0	μs
t_{DP}	Delay to Function	1.0		μs
t_{HP}	Hold from Function	1.0		μs
t_P	Power Up/Down	20.0		ms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
45	CY7C251-45PC	P21	Commercial
	CY7C251-45WC	W22	
	CY7C254-45WC	W16	
	CY7C254-45PC	P15	
	CY7C254-45DC	D16	
55	CY7C251-55PC	P21	
	CY7C251-55WC	W22	
	CY7C254-55WC	W16	
	CY7C254-55PC	P15	
	CY7C254-55DC	D16	
	CY7C251-55WMB	W22	Military
	CY7C251-55DMB	D22	
	CY7C254-55WMB	W16	
	CY7C254-55DMB	D16	
65	CY7C251-65PC	P21	Commercial
	CY7C251-65WC	W22	
	CY7C254-65WC	W16	
	CY7C254-65PC	P15	
	CY7C254-65DC	D16	
	CY7C251-65WMB	W22	Military
	CY7C251-65DMB	D22	
	CY7C251-65LMB	L55	
	CY7C251-65QMB	Q55	
	CY7C254-65WMB	W16	
	CY7C254-65LMB	L55	
	CY7C254-65QMB	Q55	
	CY7C254-65DMB	D16	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}[2]	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7,8,9,10,11
t_{ACS1}[1]	7,8,9,10,11
t_{ACS2}[2]	7,8,9,10,11

Notes:
1. 7C254 and 7C251 ($\overline{CS}_2$, CS_3 and $\overline{CS}_4$ only).
2. 7C251 ($\overline{CS}_1$ only).

Document #: 38-00056-C

8192 x 8 PROM Power Switched and Reprogrammable

Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - — 30 ns (commercial)
  - — 35 ns (military)
- Low power
  - — 550 mW (commercial)
  - — 660 mW (military)
- Super low standby power (7C261)
  - — Less than 200 mW when deselected
  - — Fast access: 30 ns
- EPROM technology 100% programmable
- Slim 300 mil or standard 600 mil packaging available
- 5V ±10% V_{CC}, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding >2000V static discharge

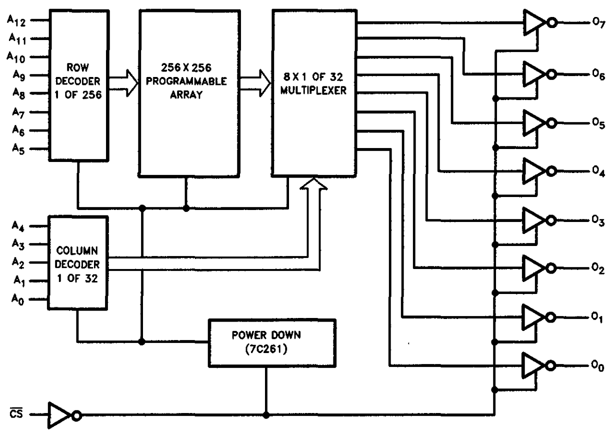
Product Characteristics

The CY7C261, CY7C263 and CY7C264 are high performance 8192 word by 8 bit CMOS PROMs. When deselected, the 7C261 automatically powers down into a low power standby mode. It is packaged in the 300 mil wide package. The 7C263 and 7C264 are packaged in 300 mil and 600 mil wide packages respectively and do not power down when deselected. The reprogrammable CERDIP packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C261, CY7C263 and CY7C264 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

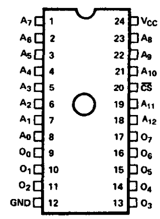
Reading is accomplished by placing an active LOW signal on $\overline{CS}$. The contents of the memory location addressed by the address lines (A_0–A_{12}) will become available on the output lines (O_0–O_7).

Logic Block Diagram



0052-1

Pin Configurations



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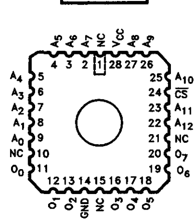

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Selection Guide

		7C261-30 7C263-30 7C264-30	7C261-35 7C263-35 7C264-35	7C261-40 7C263-40 7C264-40	7C261-45 7C263-45 7C264-45	7C261-55 7C263-55 7C264-55
Maximum Access Time (ns)		30	35	40	45	55
Maximum Operating Current (mA)	Commercial	120	100	100	100	100
	Military		120		120	120
Standby Current (mA) (7C261 only)	Commercial	40	30	30	30	30
	Military		30		30	30

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12)................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage
(Pin 19 DIP, Pin 23 LCC) 13.0V

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015)

Latchup Current .... >200 mA

UV Exposure .... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[5]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[6]

Parameters	Description	Test Conditions		7C261-30 7C263-30 7C264-30		7C261-35 7C263-35 7C264-35		7C261-40 7C263-40 7C264-40		7C261-45, 55 7C263-45, 55 7C264-45, 55		Units
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	Commercial			2.4		2.4		2.4		V
			Military							2.4		V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	Commercial	2.4								V
			Military			2.4						V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA	Commercial				0.4		0.4		0.4	V
			Military								0.4	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA	Commercial		0.4							V
			Military				0.4					V
V_{IH}	Input HIGH Level[1]			2.0		2.0		2.0		2.0		V
V_{IL}	Input LOW Level[1]				0.8		0.8		0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2								
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−40	+40	−40	+40	−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V	Commercial		120		100		100		100	mA
			Military				120				120	mA
I_{SB}	Standby Supply Current (7C261)	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, I_{OUT} = 0 mA	Commercial		40		30		30		30	mA
			Military				40				30	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C261, CY7C263 & CY7C264 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. T_A is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.

Switching Characteristics Over the Operating Range[5, 6]

Parameters	Description	7C261-30 7C263-30 7C264-30		7C261-35 7C263-35 7C264-35		7C261-40 7C263-40 7C264-40		7C261-45 7C263-45 7C264-45		7C261-55 7C263-55 7C264-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		30		35		40		45		55	ns
t_{HZCS1}	Chip Select Inactive to High Z[8]		25		25		25		30		35	ns
t_{HZCS2}	Chip Select Inactive to High Z (7C261)[8]		30		30		35		45		55	ns
t_{ACS1}	Chip Select Active to Output Valid		20		20		25		30		35	ns
t_{ACS2}	Chip Select Active to Output Valid (7C261)		35		40		45		45		55	ns
t_{PU}	Chip Select Active to Power Up (7C261)	0		0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power Down (7C261)		30		35		40		45		55	ns

AC Test Loads and Waveforms

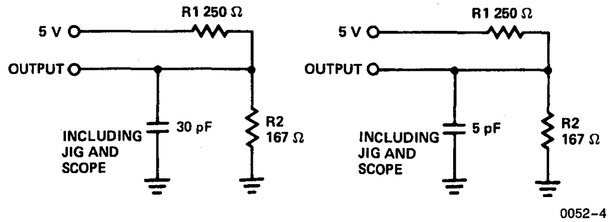


Figure 1a

Figure 1b

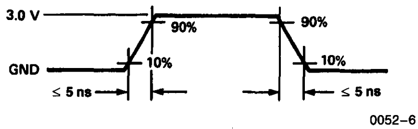
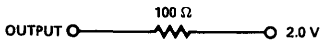
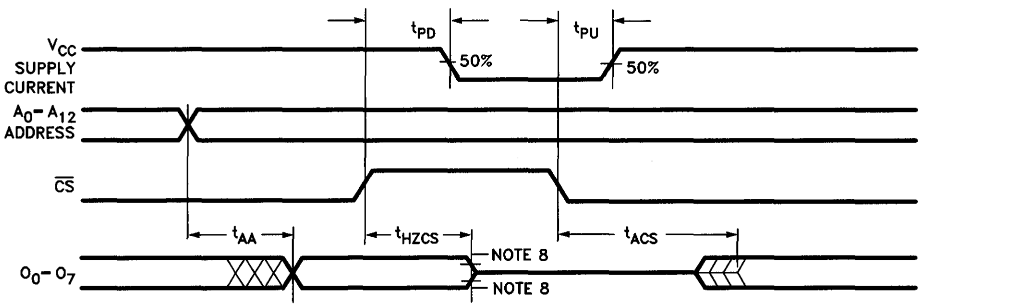


Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT





Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*
8. t_{HZCS} is tested using the load shown in *Figure 1b.* The transition time is measured from 1.5V on the CS low to high transition to the output transition through the ± 500 mV level respective to the 2.0V bias voltage (V_{THZCSL} = 1.5V, V_{THZCSH} = 2.5V).

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C261 or 7C263 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm^2 is the recommended maximum dosage.

Device Programming

The CY7C261, CY7C263 & CY7C264 all program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 64K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

Programming Pinout

The Programming Pinout of all three devices are shown in Figure 3 below, and are identical. The programming mode is entered by raising the pin 19 to V_{PP}. In this mode, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched and held in an onboard register, while the lower 8 address bits are presented on the same pins for selecting one of 256 memory bytes. The addressed location is programmed and verified with the application of a $\overline{\text{PGM}}$ and $\overline{\text{VFY}}$ pulse applied to pins 22 and 23 respectively. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.

Programming And Blankcheck

Addressing During Programming and Blankcheck

Addressing to these devices in all modes of operation other than normal read operation is accomplished by multiplexing the upper 5 address bits with the lower 8. The address designations for the lower 8 addressing bits is AX0 through AX7 and the upper 5 address bits are designated AY8 through AY12. This allows sufficient pins for an intelligent programming algorithm to be implemented without the need to switch high voltage signals during the blankcheck, programming, and verification operation.

Addressing while in these modes is accomplished by placing the upper 5 bits of address on pins 8, 7, 6, 5, and 4 with the least significant bit on pin 8. These address bits are loaded into an onboard register by clocking pin 21, the latch signal, from V_{ILP} to V_{IHP} and back to V_{ILP}. The lower 8 address bits are then placed on pins 8 through 1, with the least significant bit on pin 8. The upper 5 bits remain in the onboard latch until a new value is loaded or power is removed from the device. All 256 bytes addressed by the lower 8 bits may be accessed by sequencing the lower 8 addresses without changing the upper 5 bits or relatching the value in the onboard register.

Blankcheck

Blankcheck is accomplished by performing a verify cycle, sequencing through all memory address locations, where all the data read will be "0"s.

3

Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing V_{PP} on pin 19. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location as described above, placing the data to be programmed into a location on the data pins, and clocking the $\overline{\text{PGM}}$ signal from V_{IHP} to V_{ILP} and back to V_{IHP} with a pulse width of 200 μs. The data is removed from the data pins and the content of the location is then verified by taking the $\overline{\text{VFY}}$ signal from V_{IHP} to V_{ILP}, comparing the output with the desired data and then returning $\overline{\text{VFY}}$ to V_{IHP}. If the contents are correct, a second overprogram pulse of 4 times the original 200 μs is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200 μs pulse is applied to $\overline{\text{PGM}}$ with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the

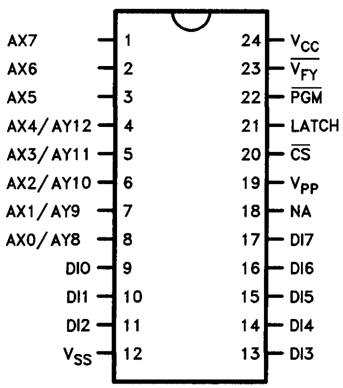


Figure 3. Programming Pinout (DIP Package)

location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed. After all locations are programmed, they should be verified at V_{CCP} = 5.0V.

Operating Modes

Read

Read is the normal operating mode for a programmed device. In this mode, all signals are normal TTL levels. The PROM is addressed with a 13 bit field, a chip select, (active LOW), is applied to the $\overline{CS}$ pin, and the contents of the addressed location appear on the data out pins.

Program, Program Inhibit, Program Verify

These modes are entered by placing a high voltage V_{PP} on pin 19, with pins 18 and 20 set to V_{ILP}. In this state, pin 21 becomes a latch signal, allowing the upper 5 address bits to be latched into an onboard register, pin 22 becomes an active LOW program ($\overline{PGM}$) signal and pin 23 becomes an active LOW verify ($\overline{VFY}$) signal. Pins 22 and 23 should never be active LOW at the same time. The PROGRAM mode exists when $\overline{PGM}$ is LOW, and $\overline{VFY}$ is HIGH. The VERIFY mode exists when the reverse is true, $\overline{PGM}$ HIGH and $\overline{VFY}$ LOW and the PROGRAM INHIBIT mode is entered with both $\overline{PGM}$ and $\overline{VFY}$ HIGH. PROGRAM INHIBIT is specifically provided to allow data to be placed on and removed from the data pins without conflict.

Blankcheck

Blankcheck mode is identical to PROGRAM VERIFY and is entered in the same manner as described above.

Programming Sequence

The flowchart in Figure 4 is a detailed description of the intelligent programming cycle used to program the devices covered in this specification. Of particular importance are the areas of power sequencing used to enter and exit the programming operation. This flowchart combined with the timing diagrams AC and DC parameters accurately describe this complete operation. Note should be taken of the inner and outer addressing loops which allow 256 bytes to be programmed each time the onboard register containing the upper 5 address bits is loaded.

The timing diagram in Figure 5 contains all of the timing information necessary for describing the relations required for programming the devices covered in this specification. Some of the information pertains to each cycle of programming as specified in the inner loops of Figure 5, some for the outer loop where the upper address is advanced, and some pertains only to entry and exit from the programming mode of operation.

In particular, the timing sequence associated with the Latch signal on pin 21 and addresses AY8 through AY12 pertain only to the outer loop where the upper 5 (N in the flow chart) address bits are incremented.

T_P, T_{PD} and T_{HP} refer to the entry and exit from the programming mode of operation. Note that this is referenced to LATCH, $\overline{PGM}$ and $\overline{VFY}$ operations.

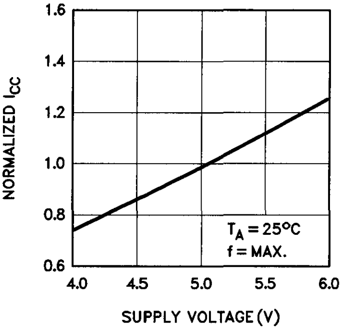
T_{DS}, T_{AS}, T_{AH} and T_{DH} refer to the required setup and hold times for the address and data for $\overline{PGM}$ and $\overline{VFY}$ operations. These parameters must be adhered to, in all operations, including V_{FY}. This precludes the option then of verifying the device by holding the V_{FY} signal LOW, and sequencing the addresses.

Table 1. Operating Modes

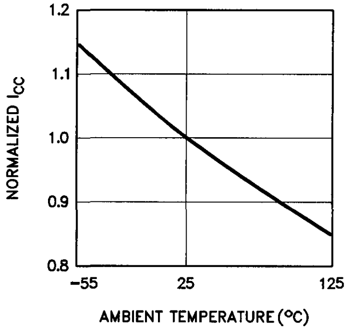
Mode	Pins 1 thru 3 A7–A5, AX7–AX5	Pins 4 thru 8 A4–A0, AX4–AX0 AY12–AY8	Pins 9 thru 11 D0 thru D2	Pins 13 thru 17 D3 thru D7	Pin 18	Pin 19	Pin 20	Pin 21	Pin 22	Pin 23
Read	A7 thru A5	A4 thru A0	DO0 thru DO2	DO3 thru DO7	A12	A11	$\overline{CS}$	A10	A9	A8
Program	AX7 thru AX5	AX4 thru AX0 AY12–AY8	DI_0 thru DI_2 Input	DI_3 thru DI_7 Input	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{ILP}	V_{IHP}
Program Inhibit	AX7 thru AX5	AX4 thru AX0 AY12–AY8	High Z	High Z	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{IHP}	V_{IHP}
Program Verify	AX7 thru AX5	AX4 thru AX0 AY12–AY8	DO0 thru DO2 Output	DO3 thru DO7 Output	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{IHP}	V_{ILP}
Blank Check	AX7 thru AX5	AX4 thru AX0 AY12–AY8	DI_0 thru DI_2 Output	DI_3 thru DI_7 Output	V_{ILP}	V_{PP}	V_{ILP}	LAT	V_{IHP}	V_{ILP}

Typical AC and DC Characteristics

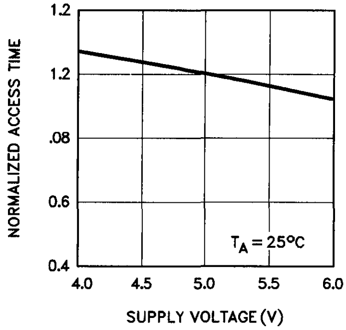
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



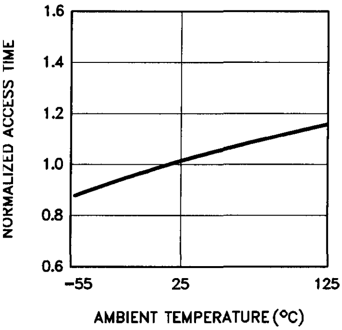
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



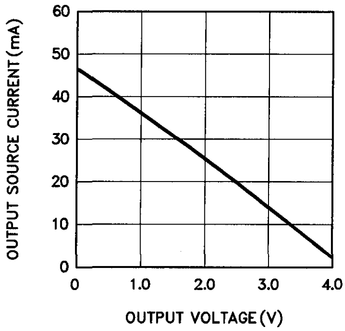
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



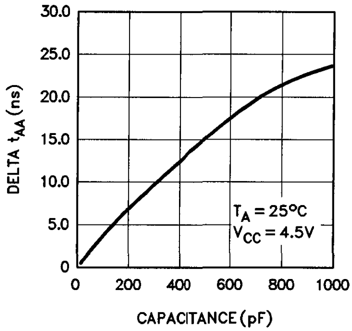
NORMALIZED ACCESS TIME vs. TEMPERATURE



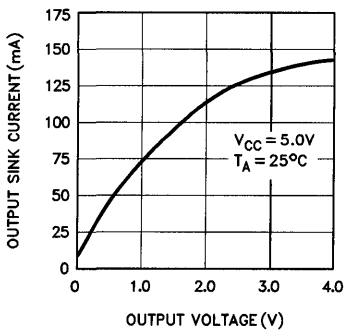
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



0052–11

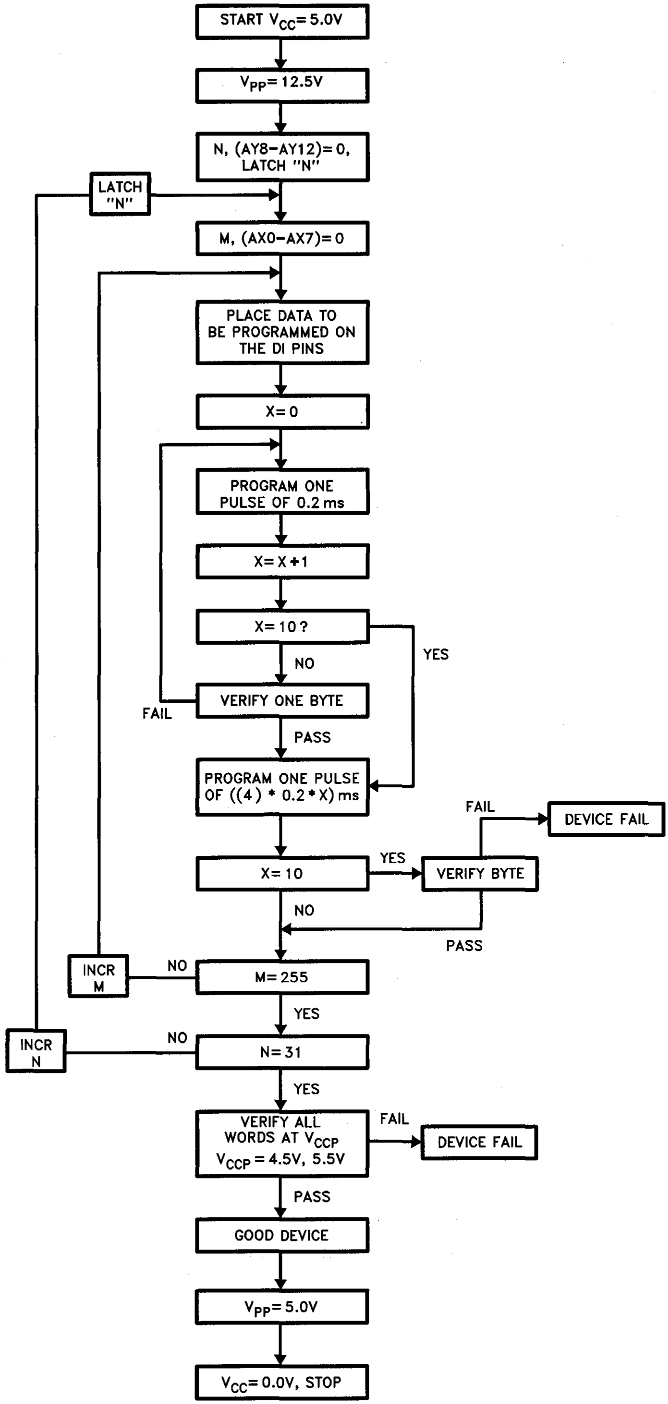


Figure 4. Programming Flowchart

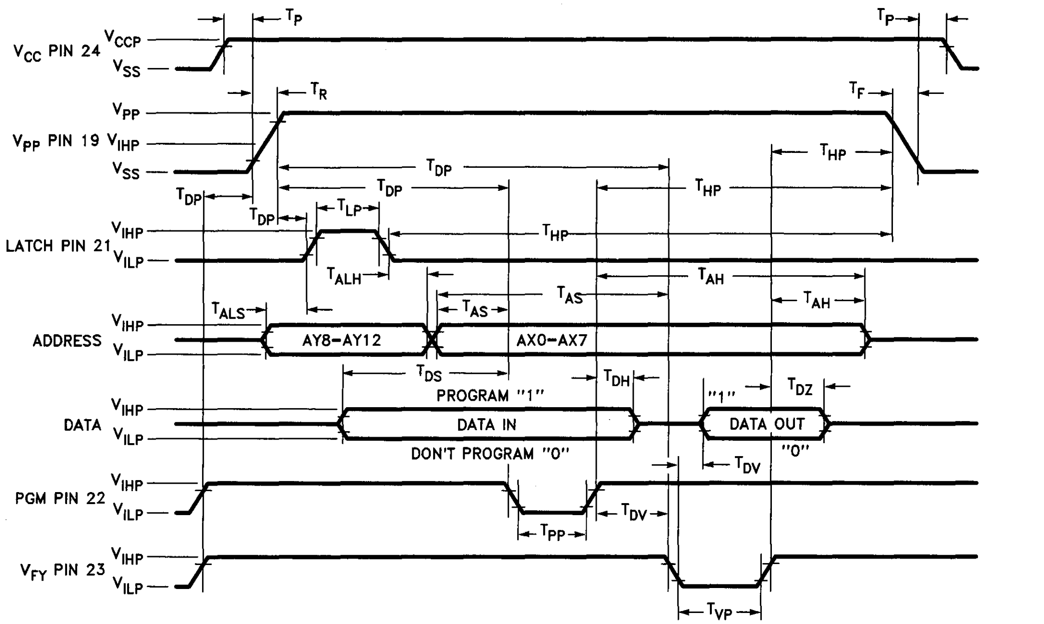


Figure 5. Programming Waveforms

Note: Power, V_{PP} and V_{CC} should not be cycled for each program verify cycle but remain static during programming.

Table 2. DC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	12.0	13.0	V
V_{CCP}	Power Supply Voltage During Programming	4.75	5.25	V
I_{PP}	V_{PP} Supply Current		50	mA
V_{IHP}	Input High Voltage During Programming	4.75	5.25	V
V_{ILP}	Input Low Voltage During Programming	−3.0	0.4	V
V_{OH}	Output High Voltage	2.4		V
V_{OL}	Output Low Voltage		0.4	V

Table 3. AC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
T_{AS}	Address Setup Time to $\overline{PGM}/\overline{VFY}$	1.0		μs
T_{AH}	Address Hold Time from $\overline{PGM}/\overline{VFY}$	1.0		μs
T_{DS}	Data Setup Time to $\overline{PGM}$	1.0		μs
T_{DH}	Data Hold Time $\overline{PGM}$	1.0		μs
T_{PP}	Program Pulse Width	0.2	10	ms
$T_{R,F}$	V_{PP} Rise and Fall Time	100		ns
T_{ALS}	Address Setup Time to Latch	1.0		μs
T_{ALH}	Address Hold Time from Latch	1.0		μs
T_{LP}	Latch Pulse Width	1.0		μs
T_{DV}	Delay to Verify	1.0		μs
T_{VD}	Verify to Data Out		1.0	μs
T_{VH}	Data Hold Time from Verify		1.0	μs
T_{VP}	Verify Pulse Width	2.0		μs
T_{DZ}	Verify to High Z		1.0	μs
T_{DP}	Delay to Function	1.0		μs
T_{HP}	Hold From Function	1.0		μs
T_P	Power Up/Down	20.0		ms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C261-30PC	P13	Commercial
	CY7C261-30WC	W14	
	CY7C263-30PC	P13	
	CY7C263-30WC	W14	
	CY7C264-30PC	P11	
	CY7C264-30WC	W12	
	CY7C264-30DC	D12	
35	CY7C261-35PC	P13	Commercial
	CY7C261-35WC	W14	
	CY7C263-35PC	P13	
	CY7C263-35WC	W14	
	CY7C264-35PC	P11	
	CY7C264-35WC	W12	
	CY7C264-35DC	D12	
	CY7C261-35WMB	W14	Military
	CY7C261-35DMB	D14	
	CY7C261-35LMB	L64	
	CY7C261-35QMB	Q64	
	CY7C263-35WMB	W14	
	CY7C263-35DMB	D14	
	CY7C263-35LMB	L64	
	CY7C263-35QMB	Q64	
	CY7C264-35DMB	D12	
	CY7C264-35WMB	W12	
40	CY7C261-40PC	P13	Commercial
	CY7C261-40WC	W14	
	CY7C263-40PC	P13	
	CY7C263-40WC	W14	
	CY7C264-40PC	P11	
	CY7C264-40DC	D12	
	CY7C264-40WC	W12	

Speed (ns)	Ordering Code	Package Type	Operating Range
45	CY7C261-45PC	P13	Commercial
	CY7C261-45WC	W14	
	CY7C263-45PC	P13	
	CY7C263-45WC	W14	
	CY7C264-45PC	P11	
	CY7C264-45DC	D12	
	CY7C264-45WC	W12	
	CY7C261-45WMB	W14	Military
	CY7C261-45DMB	D14	
	CY7C261-45LMB	L64	
	CY7C261-45QMB	Q64	
	CY7C263-45WMB	W14	
	CY7C263-45DMB	D14	
	CY7C263-45LMB	L64	
	CY7C263-45QMB	Q64	
	CY7C264-45DMB	D12	
	CY7C264-45WMB	W12	
55	CY7C261-55PC	P13	Commercial
	CY7C261-55WC	W14	
	CY7C263-55PC	P13	
	CY7C263-55WC	W14	
	CY7C264-55PC	P11	
	CY7C264-55DC	D12	
	CY7C264-55WC	W12	
	CY7C261-55WMB	W14	Military
	CY7C261-55DMB	D14	
	CY7C261-55LMB	L64	
	CY7C261-55QMB	Q64	
	CY7C263-55WMB	W14	
	CY7C263-55DMB	D14	
	CY7C263-55LMB	L64	
	CY7C263-55QMB	Q64	
	CY7C264-55DMB	D12	
	CY7C264-55WMB	W12	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}[2]	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7,8,9,10,11
t_{HZCS1}[1]	7,8,9,10,11
t_{HZCS2}[2]	7,8,9,10,11
t_{ACS1}[1]	7,8,9,10,11
t_{ACS2}[2]	7,8,9,10,11

Notes:
1. 7C263 and 7C264 only.
2. 7C261 only.

Document #: 38-00005-F

CYPRESS SEMICONDUCTOR

64K Registered PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— 40 ns max set-up**
  - **— 20 ns clock to output**
- **Low power**
  - **— 550 mW (commercial)**
  - **— 660 mW (military)**
- **On-chip edge-triggered registers**
  - **— Ideal for pipelined microprogrammed systems**
- **EPROM technology**
  - **— 100% programmable**
  - **— Reprogrammable (7C265W)**
- **5V ±10% V_{CC}, commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **Slim, 300 mil 28 pin plastic or hermetic DIP**

Functional Description

The CY7C265 is a 64K Registered PROM. It is organized 8192 words by 8 bits wide, and has a Pipeline Output Register. In addition, the device features a Programmable Initialize Byte which may be loaded into the Pipeline Register with the Initialize signal. The Programmable Initialize Byte is the 8193rd byte in the PROM and its value is programmed at time of use.

Packaged in 28 pins, the PROM has 13 Address Signals (A_0 through A_{12}), 8 Data Out Signals (O_0 through O_7), $\overline{E}/\overline{I}$, (Enable or Initialize) and CLOCK.

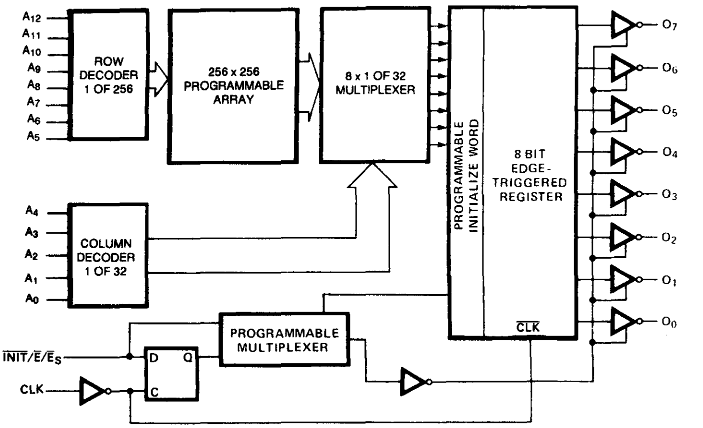
CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the Pipeline Register on each rising edge. The data will appear on the Outputs if they are enabled. One pin on the CY7C265 is programmed to perform either the Enable or the Initialize function.

If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable to a logic LOW.

If the synchronous enable ($\overline{E}_S$) is being used, the outputs will go to the OFF or high impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the subsequent positive clock edge will

3

Logic Block Diagram



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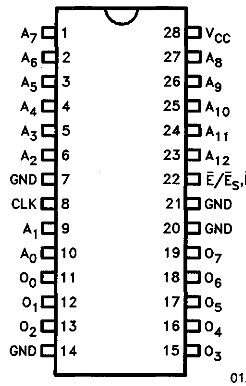
Pin Configurations



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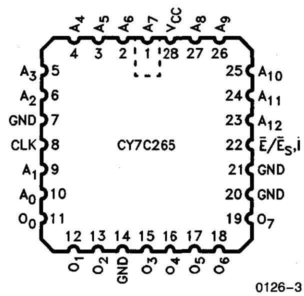

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Selection Guide

		7C265-40	7C265-50	7C265-60
Maximum Set-Up Time (ns)		40	50	60
Maximum Clock to Output (ns)		20	25	25
Maximum Operating Current (mA)	Commercial	100	80	80
	Military		120	100

Functional Description (Continued)

return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change since no change in the output will occur until the next low to high transition of the clock. This unique feature allows the CY7C265 decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

If the $\overline{E}/\overline{I}$ pin is used for $\overline{INIT}$ (asynchronous) then the outputs are permanently enabled. The initialize function is useful during power-up and time-out sequences and can facilitate implementation of other sophisticated functions such as a built-in "jump start" address. When activated the initialize control input causes the contents of a user programmed 8193rd 8-bit word to be loaded into the on-chip register. Each bit is programmable and the initialize function can be used to load any desired combination of "1"s and "0"s into the register. In the unprogrammed state, activating $\overline{INIT}$ will generate a register CLEAR (all outputs LOW). If all the bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the pipeline register and onto the outputs. The $\overline{INIT}$ LOW disables clock and must return HIGH to enable CLOCK independent of all other inputs, including the clock.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latchup Current .... >200 mA

UV Exposure .... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to 70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Commercial Min.	Commercial Max.	Military Min.	Military Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12 mA (I_{OL} = 8 mA for Military)			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}			10		10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled			40		40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	7C265-40		100			mA
			7C265-50		80		120	
			7C265-60		80		100	

Capacitance[3]

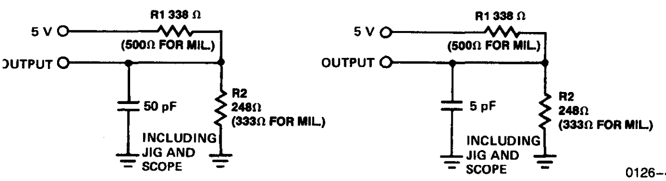
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C, f = 1\ MHz$ $V_{CC} = 5.0V$	5	pF
C_{OUT}	Output Capacitance		8	

Switching Characteristics Over the Operating Range[2]

Parameters	Description	7C265-40		7C265-50		7C265-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	40		50		60		ns
t_{HA}	Address Hold from Clock	0		0		0		ns
t_{CO}	Clock to Output Valid		20		25		25	ns
t_{PW}	Clock Pulse Width	15		20		20		ns
t_{SES}	ES Set-Up to Clock (Sync Enable Only)	15		15		15		ns
t_{HES}	ES Hold from Clock	5		5		5		ns
t_{DI}	Init to Out Valid		25		35		35	ns
t_{RI}	Init Recovery to Clock	20		25		25		ns
t_{PWI}	Init Pulse Width	25		35		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		20		25		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		20		25		25	ns
t_{DOE}	Output Valid from $\overline{E}$ Low (Async. Mode)		20		25		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ High (Async. Mode)		20		25		25	ns

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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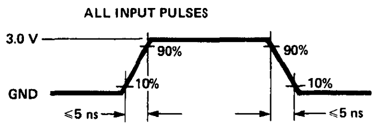

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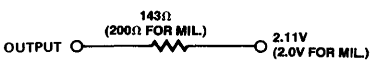

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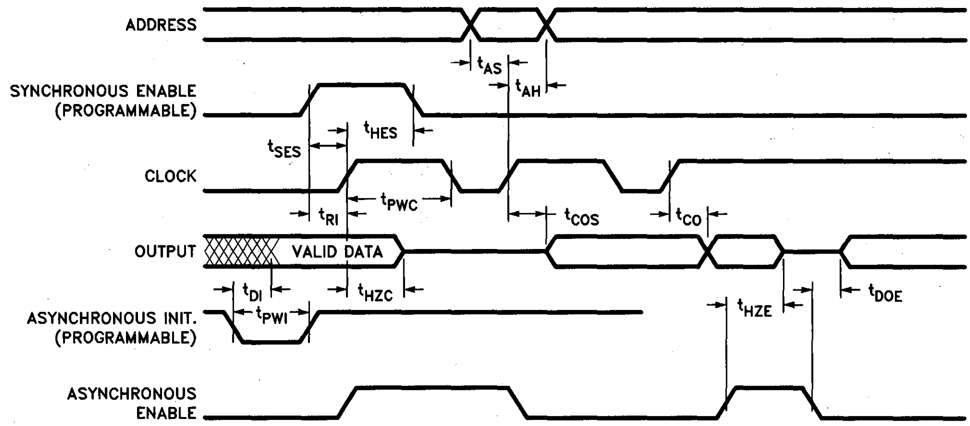
Switching Waveforms



Notes on Testing:

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b.*

Device Programming

The CY7C265 utilizes an intelligent programming algorithm to assure consistent programming quality. These 64K PROMs use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

Programming Pinout

The Programming Pinout is shown in *Figure 3.* The programming mode is entered by putting 12.5V on the V_{PP} pin. The addressed location is programmed and verified with the application of a $\overline{PGM}$ and $\overline{VFY}$ pulse. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.

Programming and Blankcheck (Memory Bits)

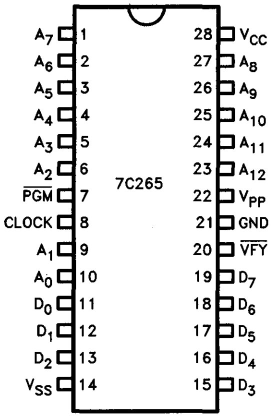
Blankcheck

Blankcheck is accomplished by performing a verify cycle ($\overline{VFY}$ toggles on each address), sequencing through all memory address locations, where all the data read will be "0"s. (Refer to mode table for pin states)

Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing 12.5V on V_{PP}. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location as described above, placing the data to be programmed into a location on the data pins, and clocking the $\overline{PGM}$ signal from V_{IHP} to V_{ILP} and back to V_{IHP} with a pulse width of 200 μs. The data is removed from the data pins and the content of the location is then verified by taking the $\overline{VFY}$ signal from V_{IHP} to V_{ILP}, comparing the output with the desired data and then returning $\overline{VFY}$ to V_{IHP}. If the contents are correct, a second overprogram pulse of 4 times the original 200 μs is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200 μs pulse is applied to $\overline{PGM}$ with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the

Programming and Blankcheck (Memory Bits) (Continued)



0126-8

Figure 3. 7C265 Programming Pinout

location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed.

After all locations are programmed, they should be verified at V_{CCP} = 5.0V.

Programming Algorithm for the Architecture

The CY7C265 offers a limited selection of programmed architecture. Programming these features should be done with a single 10 ms wide pulse in place of the intelligent algorithm mainly because these features are verified operationally, not with the $\overline{VFY}$ pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C265 architecture V_{PP} is applied to pins 3, 9 and 22. Specific choice of a particular mode will depend on the states of the other pins during programming so it is important that the condition of the other pins be met as set forth in the mode table. The same considerations with respect to power up and power down apply during architecture programming as during intelligent programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling $\overline{PGM}$ from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

To check whether a 7C265 has been programmed as output enable or initialize enable, pin 22 ($\overline{E}/\overline{I}$) should be pulled LOW followed by a LOW to HIGH transition on pin 8 (CLOCK). The data read at the outputs is stored and complement data is shifted into the shadow register. A shift from shadow to pipeline is performed and the CLOCK is again pulled from LOW to HIGH. At this point, if the new data read is data-complement, the device has been programmed as Output enable while if the new data read-true then the device is programmed as Initialize enable. The configuration of the Initialize byte can be read directly by pulling $\overline{E}/\overline{I}$ from HIGH to LOW.

3

Mode Table

Mode Select	P2 A6	P3 A5	P26 A9	P6 A2	P7 $\overline{PGM}$	P8 CLK	P9 A1	P10 A0	P20 $\overline{VFY}$	P24 A11	P22 $\overline{E}/\overline{I}$ V_{PP}	P23 A12
Normal Read	A6	A5	A9	A2	L	L/H	A1	A0	HI Z	A11	H/L	A12
Program (Memory)	A6	A5	A9	A2	L	L	A1	A0	H	A11	V_{PP}	A12
Program Verify	A6	A5	A9	A2	H	L	A1	A0	L	A11	V_{PP}	A12
Program Inhibit	A6	A5	A9	A2	H	L	A1	A0	H	A11	V_{PP}	A12
Async. Enable Read	A6	A5	A9	A2	L	L	A1	A0	HI Z	A11	L	A12
Sync. Enable Read	A6	A5	A9	A2	L	L/H	A1	A0	HI Z	A11	L	A12
Async. Init. Read	A6	A5	A9	A2	L	L	A1	A0	HI Z	A11	L	A12
Program Sync. Enable[1]	H	V_{PP}	A9	H	L	L	V_{PP}	L	H	H	V_{PP}	H
Program Initialize[2]	H	V_{PP}	A9	L	L	L	V_{PP}	L	H	H	V_{PP}	L
Program Initial Byte	H	V_{PP}	A9	L	L	L	V_{PP}	H	H	L	V_{PP}	A12

Notes:
1. Default is Async. Enable.
2. Default is Enable.

DC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	12.0	13.0	V
V_{CCP}	Power Supply Voltage During Programming	4.75	5.25	V
I_{PP}	V_{PP} Supply Current		50	mA
V_{IHP}	Input High Voltage During Programming	3.0		V
V_{ILP}	Input Low Voltage During Programming	−3.0	0.4	V
V_{OH}	Output High Voltage	2.4		V
V_{OL}	Output Low Voltage		0.4	V

AC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
t_{PP}	Program Pulse Width (Per Byte)		10.0	ms
t_{AS}	Address Set-Up Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_{DS}	Data Set-Up Time	1.0		μs
$t_{R,F}$	V_{PP} Rise and Fall Time	1.0		μs
t_{DV}	Delay to Verify	1.0		μs
t_{VD}	Verify to Data Out		1.0	μs
t_{VH}	Data Hold Time from Verify		1.0	μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DZ}	Verify to High Z		1.0	μs

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY7C265 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 $Wsec/cm^2$. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The CY7C265 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 $Wsec/cm^2$ is the recommended maximum dosage.

Bit Map Data

Programmer Address		RAM Data
Decimal	Hex	Contents
0	0	DATA
•	•	•
•	•	•
•	•	•
8191	1FFF	DATA
8192	2000	INIT BYTE
8193	2001	CONTROL BYTE

Control Byte

00 Asynchronous output enable (default condition)
01 Synchronous output enable
02 Asynchronous initialize

3

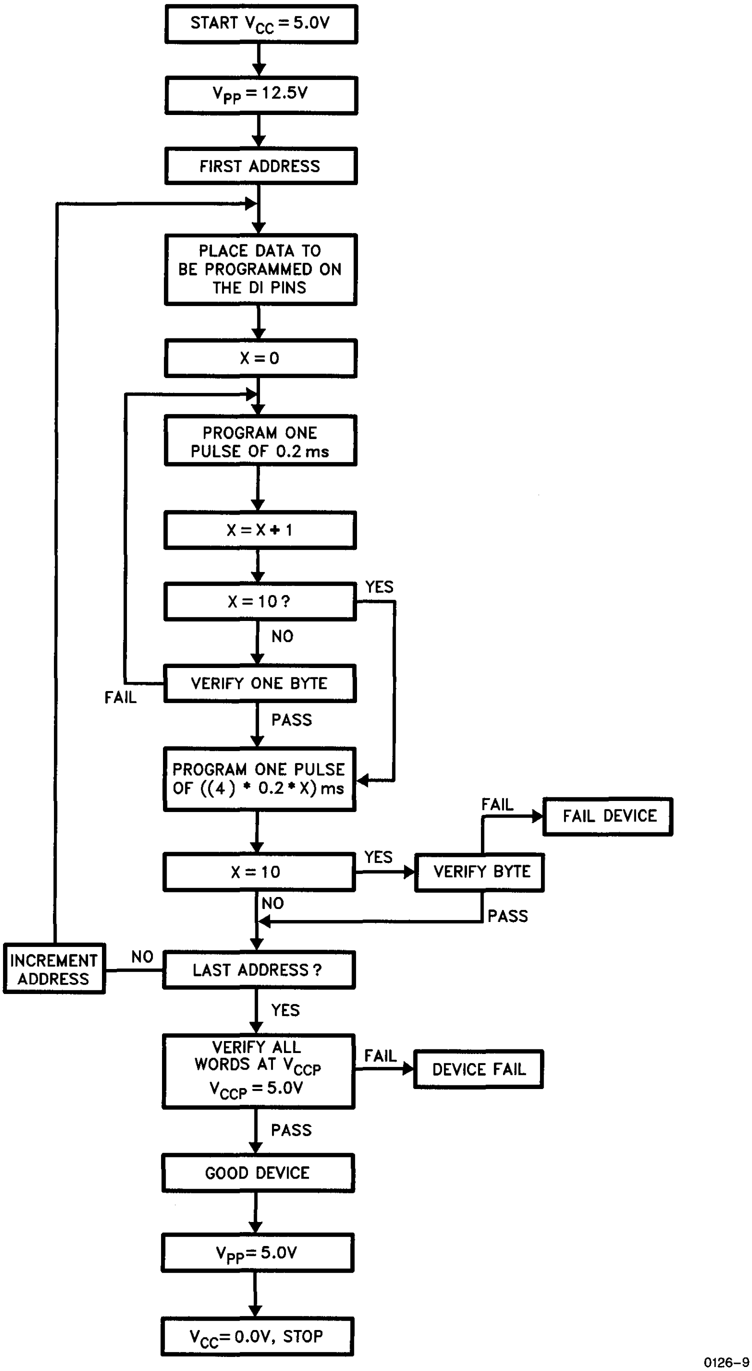


Figure 4. Programming Flowchart

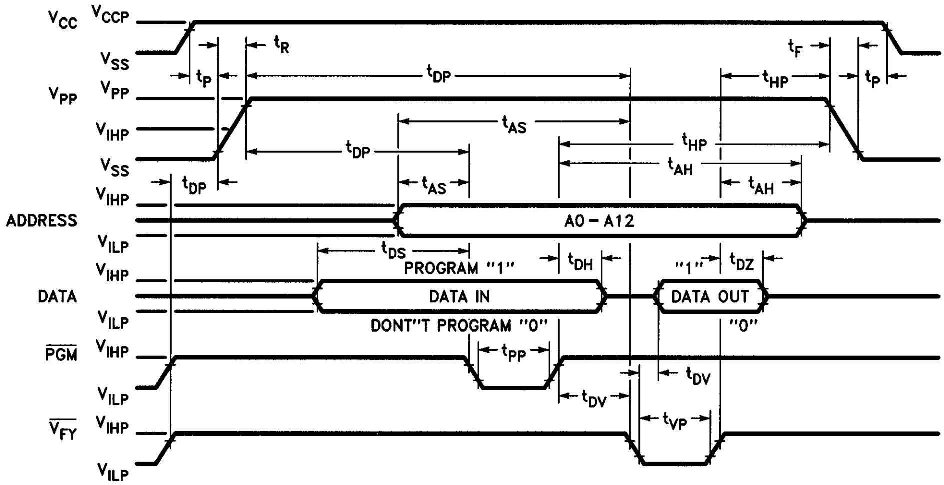
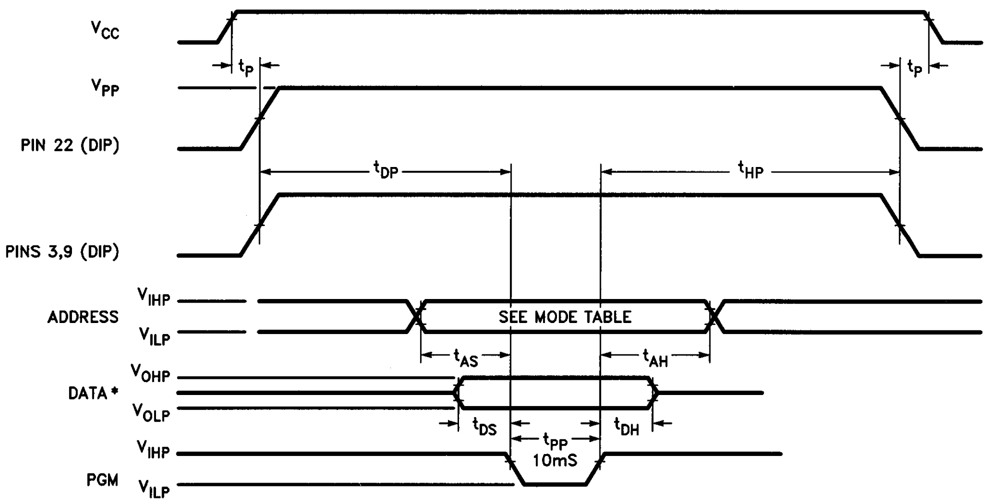


Figure 5. Programming Waveforms (Memory)

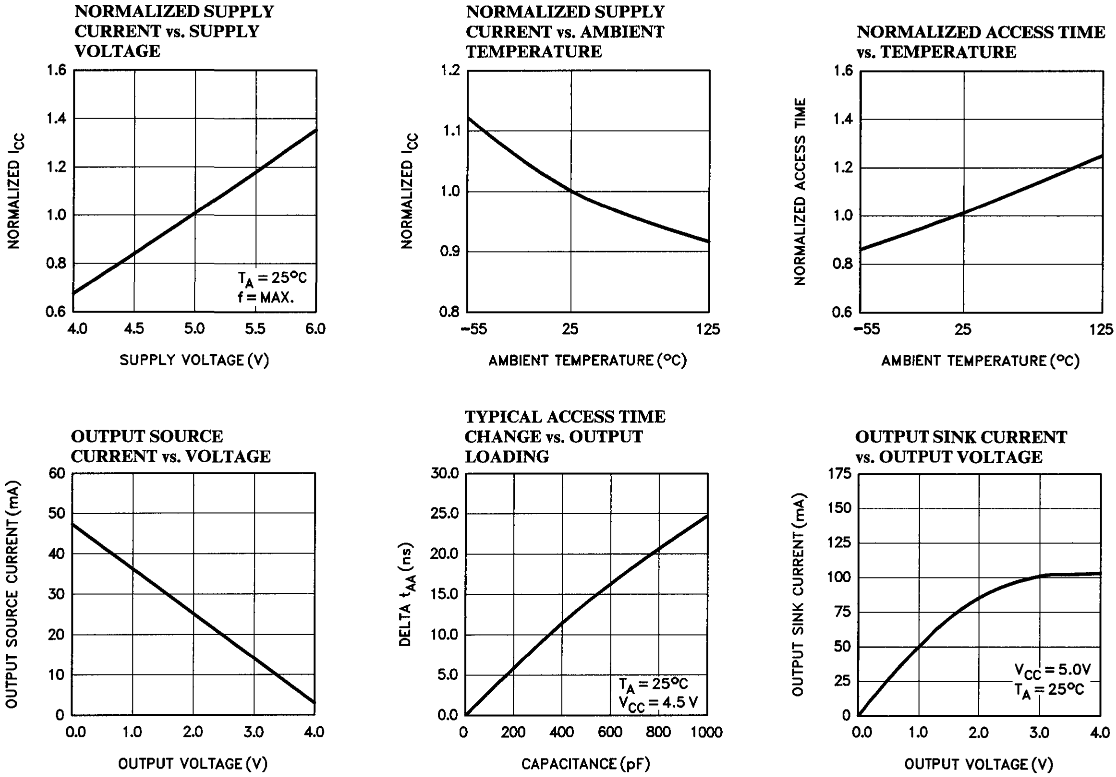
Note:
Power, V_{PP} and V_{CC} should not be cycled for each program verify cycle but remain static during programming.



*Data required on I/O's only during initial programming.

Figure 6. Programming Waveforms for the Architecture

Typical DC and AC Characteristics



0126–12

Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
40	100	CY7C265-40PC	P21	Commercial
		CY7C265-40DC	D22	
		CY7C265-40WC	W22	
50	80	CY7C265-50PC	P21	
		CY7C265-50DC	D22	
		CY7C265-50WC	W22	
	120	CY7C265-50DMB	D22	Military
		CY7C265-50WMB	W22	
		CY7C265-50LMB	L64	
		CY7C265-50QMB	Q64	

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
60	80	CY7C265-60PC	P21	Commercial
		CY7C265-60DC	D22	
		CY7C265-60WC	W22	
	100	CY7C265-60DMB	D22	Military
		CY7C265-60WMB	W22	
		CY7C265-60LMB	L64	
		CY7C265-60QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AS}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{CO}	7,8,9,10,11
t_{PW}	7,8,9,10,11
t_{SES}	7,8,9,10,11
t_{HES}	7,8,9,10,11
t_{COS}	7,8,9,10,11

Document #: 38-00084-A

CYPRESS SEMICONDUCTOR

8192 x 8 PROM Power Switched and Reprogrammable

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— 55 ns (commercial)**
  - **— 55 ns (military)**
- **Low power**
  - **— 440 mW (commercial)**
  - **— 495 mW (military)**
- **Super low standby power**
  - **— Less than 85 mW when deselected**
- **EPROM technology 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for EPROMs**
- **Capable of withstanding >2000V static discharge**

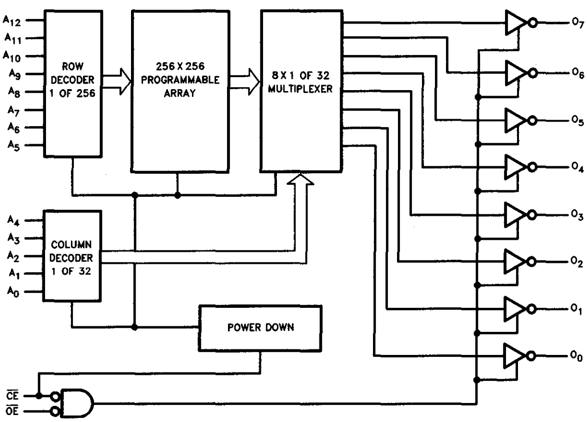
Product Characteristics

The CY7C266 is a high performance 8192 word by 8 bit CMOS PROM. When deselected, the 7C266 automatically powers down into a low power stand-by mode. It is packaged in the 600 mil wide package. The reprogrammable CERDIP packages are equipped with an erasure window; when exposed to UV light, these PROMs are erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C266 is a plug-in replacement for EPROM devices. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

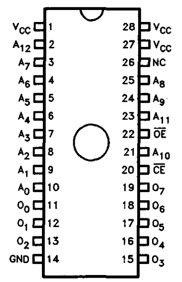
Reading is accomplished by placing an active LOW signal on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0-A_{12}) will become available on the output lines (O_0-O_7).

Logic Block Diagram

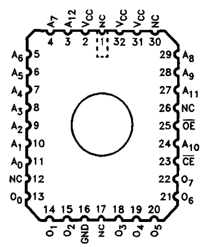


0137-1

Pin Configurations



0137-2



0137-3

Selection Guide

		7C266-55
Maximum Access Time (ns)		55
Maximum Operating Current (mA)	Commercial	80
	Military	90
Standby Current (mA)	Commercial	15
	Military	15

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14)................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage 14.0V

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latchup Current .... >200 mA

UV Exposure .... 7258 Wsec/cm²

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[5]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[6]

Parameters	Description	Test Conditions		7C266-55 Min.	7C266-55 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input HIGH Level[1]			2.0		V
V_{IL}	Input LOW Level[1]				0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC1}	Power Supply Current[8]	CMOS Inputs: GND ±0.3V or V_{CC} ±0.3V	Commercial		20	mA
			Military		30	mA
I_{CC2}	Power Supply Current[8]	TTL Inputs V_{IL} ≤ 0.8V, V_{IH} ≥ 2.0V	Commercial		25	mA
			Military		35	mA
I_{SB1}	Standby Supply Current[7]	$\overline{CE}$ = V_{CC} ±0.3V CMOS Inputs (GND or V_{CC}) ±0.3V	Commercial		15	mA
			Military		15	mA
I_{SB2}	Standby Supply Current[7]	TTL Inputs V_{IL} ≤ 0.8V, V_{IH} ≥ 2.0V	Commercial		15	mA
			Military		15	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:
1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C266 is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. T_A is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.
7. AC power component add 1 mA/MHz, V_{CC} = max, I_{OUT} = 0.
8. AC power component add 3 mA/MHz, V_{CC} = max, I_{OUT} = 0.

Switching Characteristics Over the Operating Range[5, 6, 9]

Parameters	Description	7C266-55		Units
		Min.	Max.	
t_{AA}	Address to Output Valid		55	ns
t_{HZCE}	Chip Enable Inactive to High Z[10]		55	ns
t_{HZOE}	Output Enable Inactive to High Z[10]		20	ns
t_{AOE}	Output Enable Active to Output Valid		20	ns
t_{ACE}	Chip Enable Active to Output Valid		55	ns
t_{OHA}	Data Hold from Address Change	3		ns

AC Test Loads and Waveforms

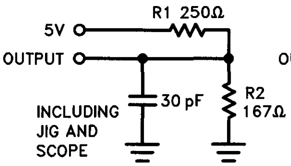
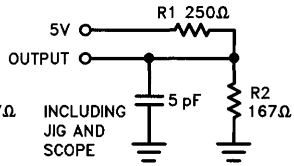
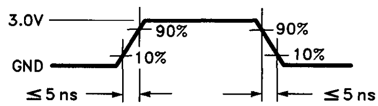


Figure 1a



0137-4

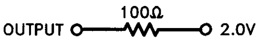
Figure 1b



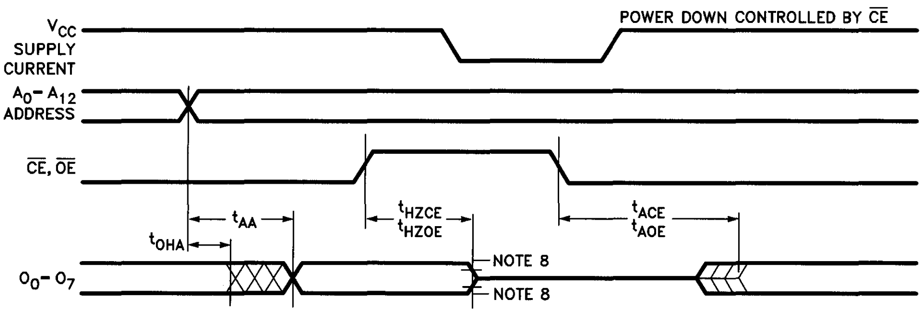
0137-5

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0137-6



0137-7

Notes:

9. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*

10. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the devices in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C266 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high intensity UV light for an extended period of time. 7258W×sec/cm^2 is the recommended maximum dosage.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
55	CY7C266-55PC	P15	Commercial
	CY7C266-55WC	W16	
	CY7C266-55DC	D16	
	CY7C266-55WMB	W16	Military
	CY7C266-55DMB	D16	
	CY7C266-55LMB	L55	
	CY7C266-55QMB	Q55	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7,8,9,10,11
t_{HZOE}	7,8,9,10,11
t_{HZCE}	7,8,9,10,11
t_{AOE}	7,8,9,10,11
t_{ACE}	7,8,9,10,11

Document #: 38-00086-C

CYPRESS SEMICONDUCTOR

64K Registered Diagnostic PROM

Features

- **CMOS for optimum speed/power**
- **High speed**
  - **40 ns max set-up**
  - **20 ns clock to output**
- **Low power**
  - **550 mW (commercial)**
  - **660 mW (military)**
- **On-chip edge-triggered registers**
  - **Ideal for pipelined microprogrammed systems**
- **On-chip diagnostic shift register**
  - **For serial observability and controllability of the output register**
- **EPROM technology**
  - **100% programmable**
  - **Reprogrammable (7C269W)**
- **5V ±10% V_{CC}, commercial and military**
- **Capable of withstanding greater than 2001V static discharge**
- **Slim, 300 mil 28 pin plastic or hermetic DIP (7C269)**

Functional Description

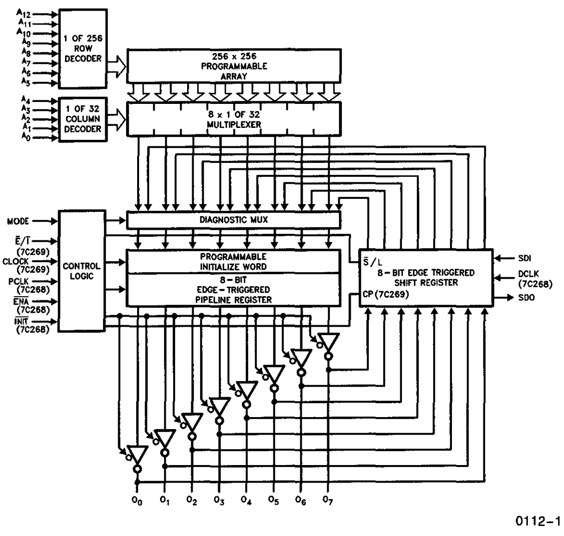
The CY7C268 and CY7C269 are 64K Registered Diagnostic PROMs. They are both organized 8192 words by 8 bits wide, and have both a Pipeline Output Register and an Onboard Diagnostic Shift Register. In addition, both devices feature a Programmable Initialize Byte which may be loaded into the Pipeline Register with the Initialize signal. The Programmable Initialize Byte is the 8193rd byte in the PROM and its value is programmed at time of use.

The 7C268 has 32 pins and features full diagnostic capabilities while the 7C269 provides limited diagnostics and is available in a space efficient 28 pin package. This allows the designer to optimize his design for either board area efficiency with the 7C269, or combine the 7C268 with other diagnostic products with the standard interface.

CY7C268: The 7C268 provides 13 address signals (A_0 through A_{12}), 8 data out signals (O_0 through O_7), $\overline{ENA}$ (enable), PCLK (pipeline clock) and $\overline{INIT}$ (initialize) for control. The full standard featured diagnostics of the 7C268 utilizes the SI and SO (shift in and shift out), MODE and DCLK signals. These signals allow serial data to be shifted into and out of the Diagnostic Shift Register at the same time the Pipeline Register is used for normal operation. The MODE signal is used to control the transfer of the information in the Diagnostic Register to the Pipeline Register or the data on the Output Bus into the Diagnostic Register. The data on the Output Bus may be provided from the Pipeline Register or an external source.

When the MODE signal is LOW, the PROM operates in a normal pipeline mode. The contents of the addressed memory location is loaded into the Pipeline Register on the rising edge of PCLK. The outputs are enabled with the $\overline{ENA}$ signal either synchronously or asynchronously, depending on how the device is configured when programmed. If programmed for asynchronous enable, $\overline{ENA}$ LOW enables

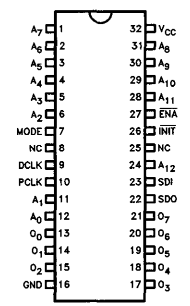
Logic Block Diagram



0112-1

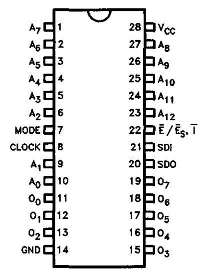
Pin Configurations

CY7C268

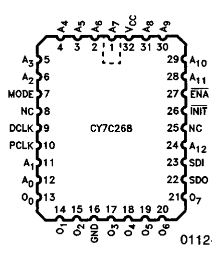


0112-2

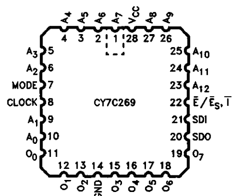
CY7C269



0112-3



0112-4



0112-5

Selection Guide

		7C268/9-40	7C268/9-50	7C268/9-60
Maximum Set-up Time (ns)		40	50	60
Maximum Clock to Output (ns)		20	25	25
Maximum Operating Current (mA)	Commercial	100	80	80
	Military		120	100

Functional Description (Continued)

the outputs. If configured for synchronous enable, $\overline{ENA}$ LOW during the rising edge of PCLK will enable the outputs synchronously with PCLK. $\overline{ENA}$ HIGH during the rising edge of PCLK will synchronously disable the outputs. The asynchronous Initialize signal $\overline{INIT}$ transfers the Initialize Byte into the Pipeline Register on a HIGH to LOW transition. $\overline{INIT}$ LOW disables PCLK and needs to transition back to a HIGH in order to enable PCLK. DCLK shifts data into SI and out of SO on each rising edge.

When MODE is HIGH, the rising edge of the PCLK signal loads the Pipeline Register with the contents of the Diagnostic Register. Similarly, DCLK, in this mode, loads the Diagnostic Register with the information on the Data Output Pins. The information loaded will be either the contents of the Pipeline Register if the outputs are enabled, or data on the bus, if the outputs are disabled (in a high impedance state).

CY7C269: This product is optimized for applications that require diagnostics in a minimum amount of board area. Packaged in 28 pins, the PROM has 13 Address Signals (A_0 through A_{12}), 8 Data Out Signals (O_0 through O_7), $\overline{E}/\overline{I}$, (Enable or Initialize) and CLOCK (pipeline and diagnostic clock). Additional diagnostic signals consist of MODE, SI (shift in) and SO (shift out). Normal pipelined operation and Diagnostic operation are mutually exclusive.

When the MODE signal is LOW, the 7C269 operates in a normal pipelined mode. CLOCK functions as a pipeline clock, loading the contents of the addressed memory location into the Pipeline Register on each rising edge. The data will appear on the Outputs if they are enabled. One pin on the 7C269 is programmed to perform either the Enable or the Initialize function. If the $\overline{E}/\overline{I}$ pin is used for a $\overline{INIT}$ (Asynchronous Initialize) function, the outputs are permanently enabled and the Initialize Word is loaded into the Pipeline Register on a High to LOW transition of the $\overline{INIT}$ signal. The $\overline{INIT}$ LOW disables CLOCK and must return high to re-enable CLOCK. If the $\overline{E}/\overline{I}$ pin is used for an enable signal, it may be programmed for either synchronous or asynchronous operation. This enable function then operates exactly the same as the 7C268.

When the MODE signal is HIGH, the 7C269 operates in the diagnostic mode. The $\overline{E}/\overline{I}$ signal becomes a secondary mode signal designating whether to shift the Diagnostic Shift Register or to load either the Diagnostic Register or the Pipeline Register. If $\overline{E}/\overline{I}$ is HIGH, CLOCK performs the function of DCLK, shifting SI into the least significant location of the Diagnostic Register and all bits one location toward the most significant location on each rising edge. The contents of the most significant location in the Diagnostic Register are available on the SO pin.

If the $\overline{E}/\overline{I}$ signal is LOW, SI becomes a direction signal; transferring the contents of the Diagnostic Register into the Pipeline Register when SI is LOW. When SI is HIGH, the contents of the Output pins are transferred into the Diagnostic Register. Both transfers occur on a LOW to HIGH transition of the CLOCK. If the Outputs are enabled, the contents of the Pipeline Register are transferred into the Diagnostic Register. If the Outputs are disabled, an external source of data may be loaded into the Diagnostic Register. In this condition, the SO signal is internally driven to be the same as the SI signal thus propagating the "direction of transfer information" to the next device in the string.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latchup Current .... >200 mA

UV Exposure .... 7258 Wsec/c

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to 70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Commercial		Military		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12 mA (I_{OL} = 8 mA for Military)			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0		2.0		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}			10		10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC} Output Disabled			40		40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND			90		90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	7C268/9-40		100			mA
			7C268/9-50		80		120	
			7C268/9-60		80		100	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Switching Characteristics Over the Operating Range[2]

Parameters	Description	7C268-40 7C269-40		7C268-50 7C269-50		7C268-60 7C269-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AS}	Address Set-Up to Clock	40		50		60		ns
t_{HA}	Address Hold from Clock	0		0		0		ns
t_{CO}	Clock to Output Valid		20		25		25	ns
t_{PW}	Clock Pulse Width	15		20		20		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock (Sync Enable Only)	15		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock	5		5		5		ns
t_{DI}	$\overline{\text{INIT}}$ to Out Valid		25		35		35	ns
t_{RI}	$\overline{\text{INIT}}$ Recovery to Clock	20		25		25		ns

Switching Characteristics Over the Operating Range[3] (Continued)

Parameters	Description	7C268-40 7C269-40		7C268-50 7C269-50		7C268-60 7C269-60		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PWI}	Init Pulse Width	25		35		35		ns
t_{COS}	Output Valid from Clock (Sync. Mode)		20		25		25	ns
t_{HZC}	Output Inactive from Clock (Sync. Mode)		20		25		25	ns
t_{DOE}	Output Valid from $\overline{E}$ Low (Async. Mode)		20		25		25	ns
t_{HZE}	Output Inactive from $\overline{E}$ High (Async. Mode)		20		25		25	ns

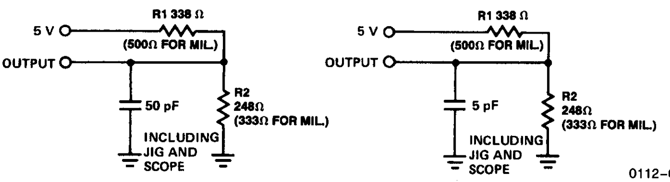
3

Diagnostic Mode Switching Characteristics Over the Operating Range[2]

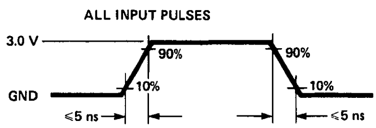
Parameters	Description	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
t_{SSDI}	Set-Up SDI to Clock	30		35		ns
t_{HSDI}	SDI Hold from Clock	0		0		ns
t_{DSDO}	SDO Delay from Clock		30		40	ns
t_{DCL}	Minimum Clock Low	25		25		ns
t_{DCH}	Minimum Clock High	25		25		ns
t_{SM}	Set-Up to Mode Change	25		30		ns
t_{HM}	Hold from Mode Change (7C269)	0		0		ns
t_{MS}	Mode to SDO		25		30	ns
t_{SS}	SDI to SDO		40		45	ns
t_{SO}	Data Set-Up to DCLK	25		30		ns
t_{HO}	Data Hold from DCLK	10		15		ns

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Tested initially and after any design or process changes that may affect these parameters.

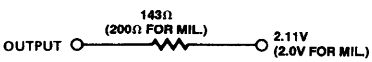
AC Test Loads and Waveforms



0112-6



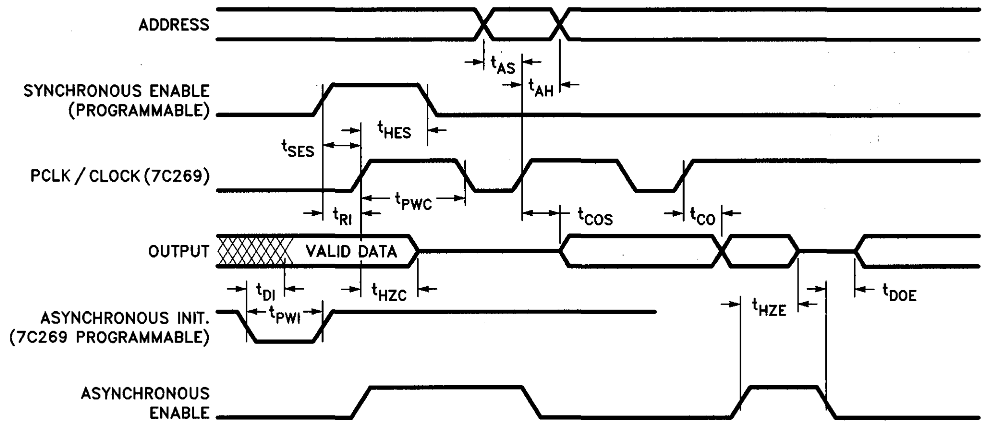
0112-7



0112-8

Switching Waveforms 7C268, 7C269

Pipeline Operation (Mode = 0)



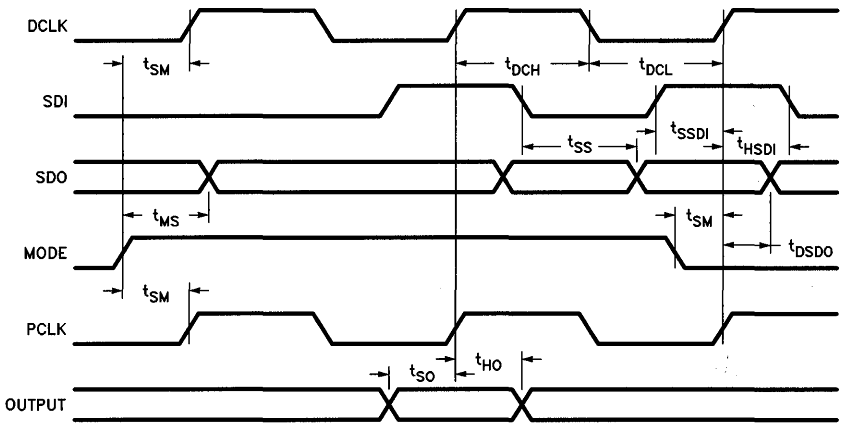
0112-9

Notes on Testing:

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device V_{CC} and ground terminals. Multiple capacitors are recommended, including a 0.1 μF or larger capacitor and a 0.01 μF or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.
4. Output levels are measured at 1.5V reference levels.
5. Transition is measured at steady state HIGH level −500 mV or steady state LOW level +500 mV on the output from the 1.5V level on inputs with load shown in *Figure 1b.*

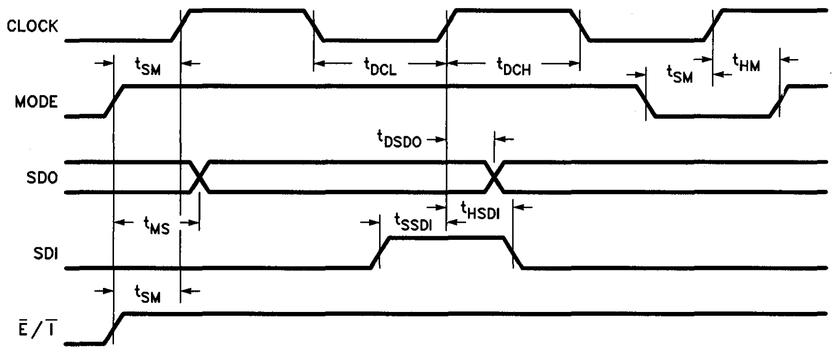
7C268 Diagnostic Waveforms



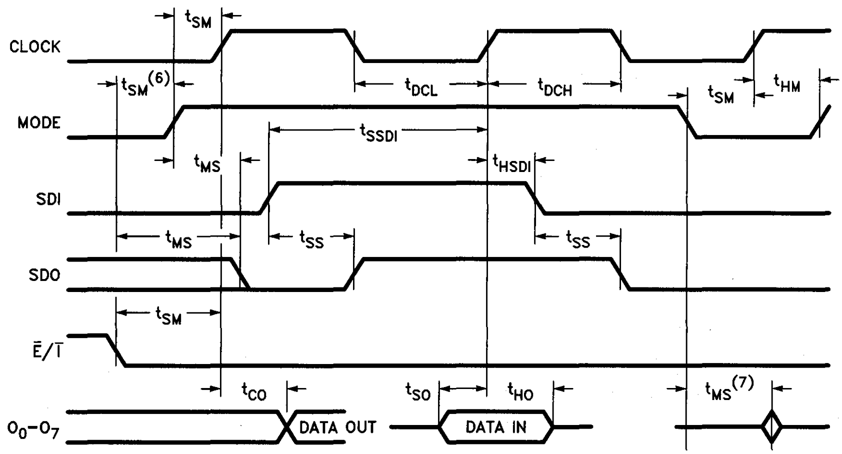
0112-10

Switching Waveforms (Continued)

7C269 Diagnostic Application (Shifting the Shadow Register)



7C269 Diagnostic Application (Parallel Data Transfer)



Notes:

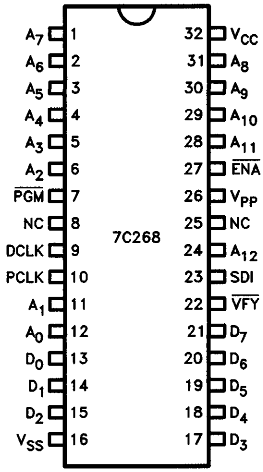
6. Asynchronous enable mode only.
7. The mode transition to HIGH latches the asynchronous enable state. If the enable state is changed and held before leaving the diagnostic mode (mode H → L) then the output impedance change delay is t_{MS}.

Device Programming

The CY7C268 and CY7C269 program identically. They utilize an intelligent programming algorithm to assure consistent programming quality. These 64K PROMS use a single ended memory cell design. In an unprogrammed state, the memory contains all "0"s. During programming, a "1" on a data-in pin causes the addressed location to be programmed, and a "0" causes the location to remain unprogrammed.

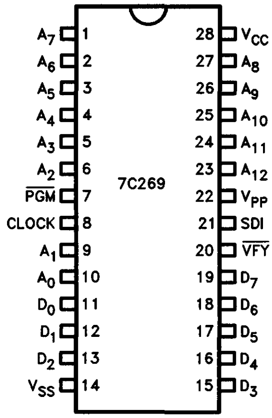
Programming Pinout

The Programming Pinout of both devices is shown in *Figures 3a* and *3b.* The programming mode is entered by putting 12.5V on the V_{PP} pin. The addressed location is programmed and verified with the application of a $\overline{PGM}$ and $\overline{VFY}$ pulse. Entering and exiting the programming mode should be done with care. Proper sequencing as described in the dialog on the programming algorithm and shown in the timing diagram and programming flow chart must be implemented.



0112-13

Figure 3a. 7C268 Programming Pinout



0112-14

Figure 3b. 7C269 Programming Pinout

Programming and Blankcheck (Memory Bits)

Blankcheck

Blankcheck is accomplished by performing a verify cycle ($\overline{\text{VFY}}$ toggles on each address), sequencing through all memory address locations, where all the data read will be "0"s. (Refer to mode table for pin states)

Programming Algorithm

Programming is accomplished with an intelligent algorithm. The sequence of operations is to enter the programming mode by placing 12.5V on V_{PP}. This should be done after a minimum delay from power up, and be removed prior to power down by the same delay (see the timing diagram and AC specifications for details). Once in this mode, programming is accomplished by addressing a location as described above, placing the data to be programmed into a location on the data pins, and clocking the $\overline{\text{PGM}}$ signal from V_{IHP} to V_{ILP} and back to V_{IHP} with a pulse width of 200 µs. The data is removed from the data pins and the content of the location is then verified by taking the $\overline{\text{VFY}}$ signal from V_{IHP} to V_{ILP}, comparing the output with the desired data and then returning $\overline{\text{VFY}}$ to V_{IHP}. If the contents are correct, a second overprogram pulse of 4 times the original 200 µs is delivered with the data to be programmed again on the data pins. If the data is not correct, a second 200 µs pulse is applied to $\overline{\text{PGM}}$ with the data to be programmed on the data pins. The compare and overprogram operation is repeated with an overprogram pulse width 4 times the sum of the initial program pulses. This operation is continued until the location is programmed or 10 initial program pulses have been attempted. If on the 10th attempt, the location fails to verify, an overprogram pulse of 8 ms is applied, and the content of the location is once more verified. If the location still fails to verify, the device is rejected. Once a location verifies successfully, the address is advanced to the next location, and the process is repeated until all locations are programmed.

After all locations are programmed, they should be verified at V_{CCP} = 5.0V.

Programming Algorithm for the Architecture

Both the 7C268 and 7C269 offer a limited selection of programmed architecture. Programming these features should be done with a single 10 ms wide pulse in place of the intelligent algorithm mainly because these features are verified operationally, not with the $\overline{\text{VFY}}$ pin. Architecture programming is implemented by applying the supervoltage to two additional pins during programming. In programming the 7C269 architecture V_{PP} is applied to pins 3, 9 and 22 while in programming the 7C268 architecture V_{PP} is applied to pins 3, 11, 26. Specific choice of a particular mode will depend on the states of the other pins during programming so it is important that the condition of the other pins be met as set forth in the mode table. The same considerations with respect to power up and power down apply during architecture programming as during intelligent programming. Once the supervoltages have been established and the correct logic states exist on the other device pins, programming may begin. Programming is accomplished by pulling $\overline{\text{PGM}}$ from HIGH to LOW and then back to HIGH with a pulse width equal to 10 ms.

To check whether a 7C269 has been programmed as output enable or initialize enable, pin 22 ($\overline{\text{E}}/\overline{\text{I}}$) should be pulled LOW followed by a LOW to HIGH transition on pin 8 (CLOCK). The data read at the outputs is stored and complement data is shifted into the shadow register. A shift from shadow to pipeline is performed and the CLOCK is again pulled from LOW to HIGH. At this point, if the new data read is data-complement, the device has been programmed as Output enable while if the new data read-true then the device is programmed as Initialize enable and the configuration of the Initialize byte can be read directly by pulling $\overline{\text{E}}/\overline{\text{I}}$ from HIGH to LOW.

Mode Table 7C268

Mode Select	P2 A6	P3 A5	P30 A9	P6 A2	P7 MD $\overline{\text{PGM}}$	P9 DCLK	P10 PCLK	P11 A1	P12 A0	P22 SDO $\overline{\text{VFY}}$	P23 SDI	P24 A12	P26 $\overline{\text{INT}}$ V_{PP}	P27 $\overline{\text{E}/\text{E}_S}$	P28 A11
Normal Read[2]	A6	A5	A9	A2	L	X	L/H	A1	A0	SDO	X	A12	H	H/L	A11
Load SR to PR[2]	A6	A5	A9	A2	H	L	L/H	A1	A0	SDI	X	A12	H	X	A11
Load Output to SR	A6	A5	A9	A2	H	L/H	L	A1	A0	SDI	L	A12	H	H	A11
Shift Shadow[2]	A6	A5	A9	A2	L	L/H	L	A1	A0	SDO	DIN	A12	H	X	A11
Program (Memory)	A6	A5	A9	A2	L	L	L	A1	A0	H	L	A12	V_{PP}	H	A11
Program Verify	A6	A5	A9	A2	H	L	L	A1	A0	L	L	A12	V_{PP}	H	A11
Program Inhibit	A6	A5	A9	A2	H	L	L	A1	A0	H	L	A12	V_{PP}	H	A11
Async. Enable Read	A6	A5	A9	A2	L	L	X	A1	A0	SDO	L	A12	H	H/L	A11
Sync. Enable Read	A6	A5	A9	A2	L	L	L/H	A1	A0	SDO	L	A12	H	H/L	A11
Async. Init. Read	A6	A5	A9	A2	L	L	X	A1	A0	SDO	L	A12	L	L	A11
Program Sync. Enable[1]	H	V_{HH}	X	H	L	L	L	V_{HH}	L	H	L	H	V_{PP}	H	H
Program Initial Byte	H	V_{HH}	X	L	L	L	L	V_{HH}	H	H	L	X	V_{PP}	H	L

Notes:

1. Default is Async. Enable.
2. For the asynchronous enable operation, the data out is enabled by bringing $\overline{\text{E}}$ LOW. For the synchronous enable operation, data out is enabled on the first LOW to HIGH clock transition after $\overline{\text{E}}$ is brought LOW. When $\overline{\text{E}}$ goes from LOW to HIGH (enable to disable) the outputs will go to the high impedance state (after a propagation delay) immediately if the asynchronous enable was programmed. If the synchronous enable was selected, a LOW to HIGH clock transition is required.

Mode Table 7C269

Mode Select	P2 A6	P3 A5	P26 A9	P6 A2	P7 MD $\overline{\text{PGM}}$	P8 CLK	P9 A1	P10 A0	P21 SDI	P20 SDO $\overline{\text{VFY}}$	P24 A11	P22 $\overline{\text{E}}/\overline{\text{I}}$ V_{PP}	P23 A12
Normal Read	A6	A5	A9	A2	L	L/H	A1	A0	X	HI Z	A11	H/L	A12
Load SR to PR[3]	A6	A5	A9	A2	H	L/H	A1	A0	L	SDI	A11	L	A12
Load Output to SR[3]	A6	A5	A9	A2	H	L/H	A1	A0	H	SDI	A11	L	A12
Shift Shadow[3]	A6	A5	A9	A2	H	L/H	A1	A0	DIN	SDO	A11	H	A12
Program (Memory)	A6	A5	A9	A2	L	L	A1	A0	X	H	A11	V_{PP}	A12
Program Verify	A6	A5	A9	A2	H	L	A1	A0	X	L	A11	V_{PP}	A12
Program Inhibit	A6	A5	A9	A2	H	L	A1	A0	X	H	A11	V_{PP}	A12
Async. Enable Read	A6	A5	A9	A2	L	L	A1	A0	X	HI Z	A11	L	A12
Sync. Enable Read	A6	A5	A9	A2	L	L/H	A1	A0	X	HI Z	A11	L	A12
Async. Init. Read	A6	A5	A9	A2	L	L	A1	A0	X	HI Z	A11	L	A12
Program Sync. Enable[1]	H	V_{HH}	A9	H	L	L	V_{HH}	L	X	H	H	V_{PP}	H
Program Initialize[2]	H	V_{HH}	A9	L	L	L	V_{HH}	L	X	H	H	V_{PP}	L
Program Initial Byte	H	V_{HH}	A9	L	L	L	V_{HH}	H	X	H	L	V_{PP}	A12

Notes:

1. Default is Async. Enable.
2. Default is Enable.
3. If $\overline{\text{I}}$ selected, outputs always enabled. If $\overline{\text{E}}$ selected, during diagnostic operation the data outputs will remain in the state they were in when the mode was entered. When enabled, the data outputs will reflect the outputs of the pipeline register. Any changes in the data in the pipeline register will appear on the data output pins.

DC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	12.0	13.0	V
V_{CCP}	Power Supply Voltage During Programming	4.75	5.25	V
I_{PP}	V_{PP} Supply Current		50	mA
V_{IHP}	Input High Voltage During Programming	3.0		V
V_{ILP}	Input Low Voltage During Programming	−3.0	0.4	V
V_{OH}	Output High Voltage	2.4		V
V_{OL}	Output Low Voltage		0.4	V

AC Programming Parameters $T_A = 25°C$

Parameter	Description	Min.	Max.	Units
t_{PP}	Program Pulse Width (Per Byte)		10.0	ms
t_{AS}	Address Set-up Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_{DS}	Data Set-up Time	1.0		μs
$t_{R,F}$	V_{PP} Rise and Fall Time	1.0		μs
t_{DV}	Delay to Verify	1.0		μs
t_{VD}	Verify to Data Out		1.0	μs
t_{VH}	Data Hold Time from Verify		1.0	μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DZ}	Verify to High Z		1.0	μs

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C268 and 7C269 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 $Wsec/cm^2$. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C268 or 7C269 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 $Wsec/cm^2$ is the recommended maximum dosage.

Bit Map Data

Programmer Address		RAM Data
Decimal	Hex	Contents
0	0	DATA
•	•	•
•	•	•
•	•	•
8191	1FFF	DATA
8192	2000	INIT BYTE
8193	2001	CONTROL BYTE

Control Byte

00 Asynchronous output enable (default condition)
01 Synchronous output enable
02 Asynchronous initialize (CY7C269 only)

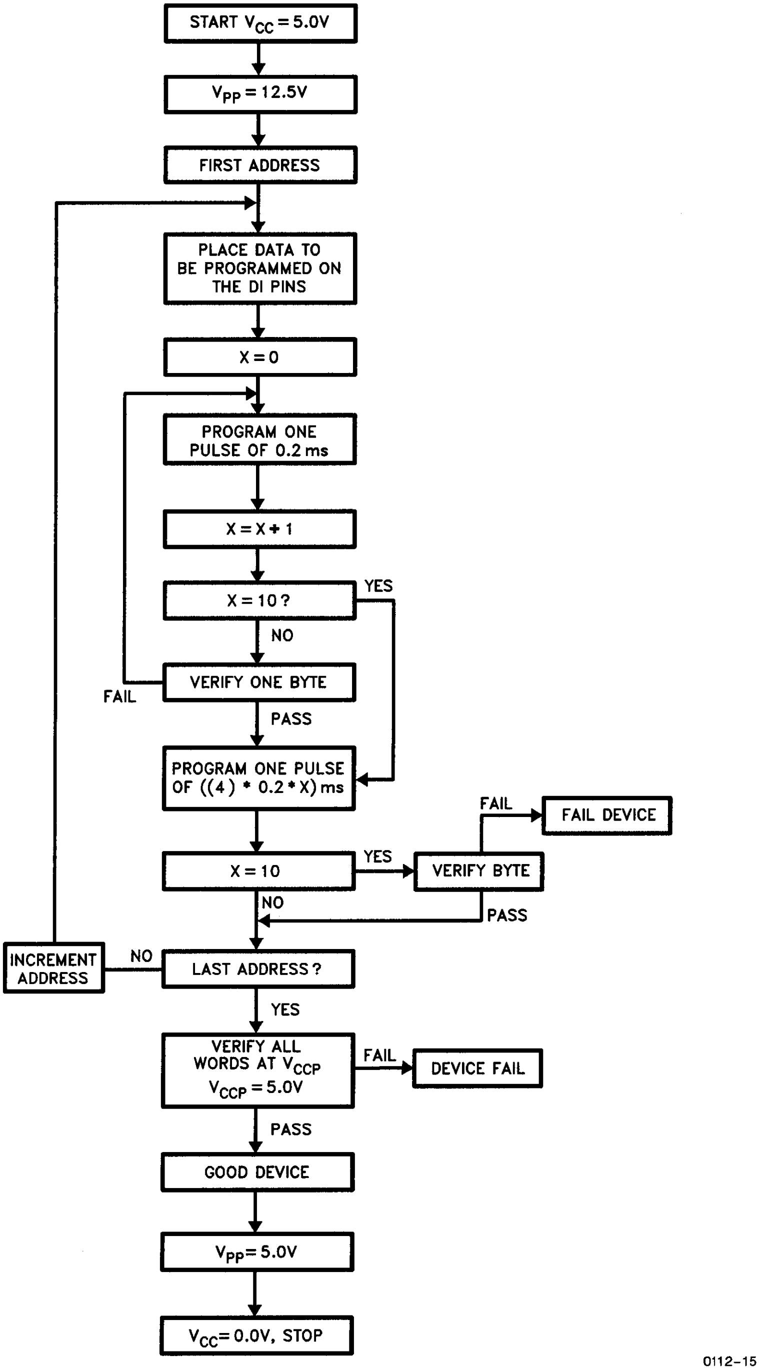
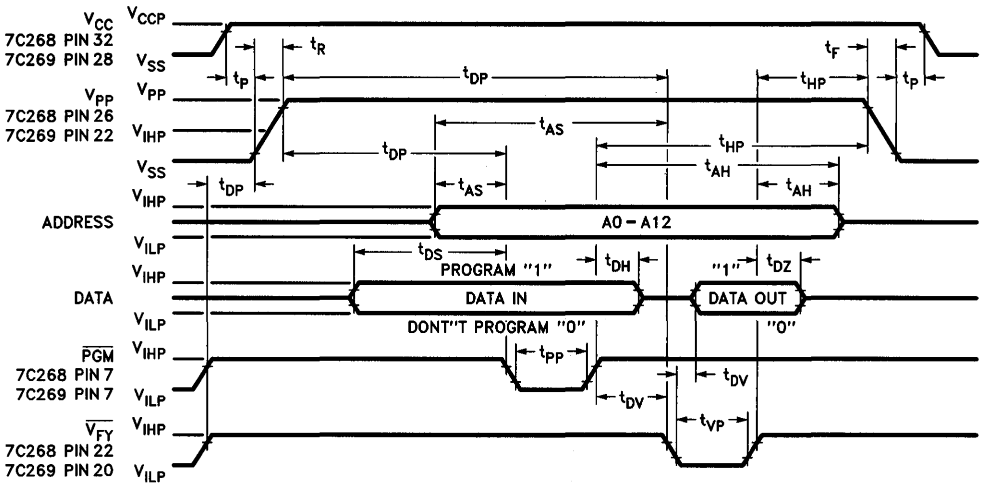


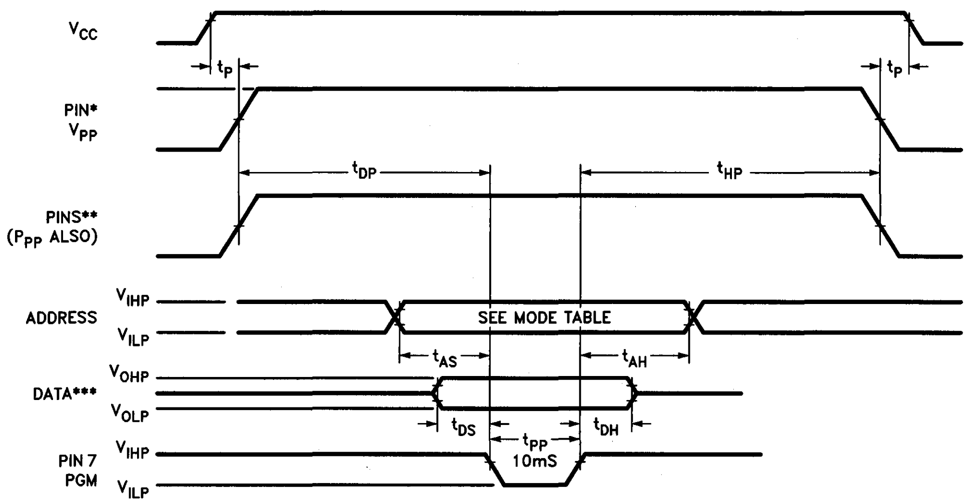
Figure 4. Programming Flowchart



0112–16

Figure 5. Programming Waveforms (Memory)

Note:
Power, V_{PP} and V_{CC} should not be cycled for each program verify cycle but remain static during programming.



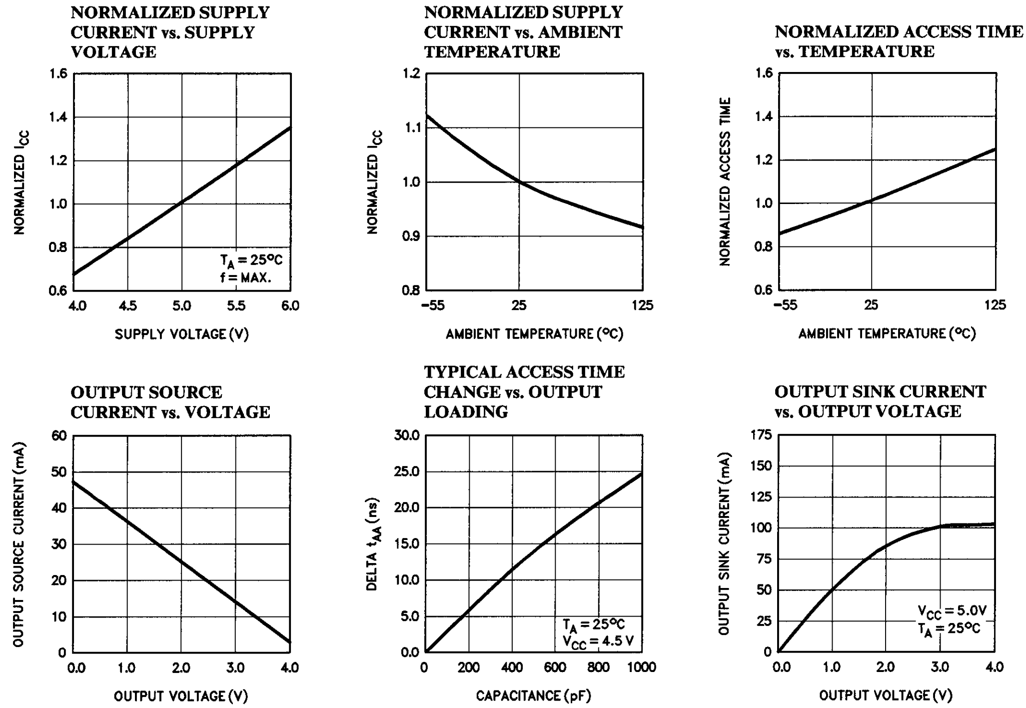
0112–17

*7C268-pin 26
7C269-pin 22
**7C268-pins 3, 11
7C269-pins 3, 9

***Data required on I/O's only during initial byte programming

Figure 6. Programming Waveforms for the Architecture CY7C268 and CY7C269

Typical DC and AC Characteristics



0112–18

Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
40	100	CY7C268-40DC	D20	Commercial
		CY7C268-40WC	W20	
		CY7C269-40PC	P21	
		CY7C269-40DC	D22	
		CY7C269-40WC	W22	
50	80	CY7C268-50DC	D20	
		CY7C268-50WC	W20	
		CY7C269-50PC	P21	
		CY7C269-50DC	D22	
		CY7C269-50WC	W22	
	120	CY7C268-50DMB	D20	Military
		CY7C268-50WMB	W20	
		CY7C268-50LMB	L55	
		CY7C268-50QMB	Q55	
		CY7C269-50DMB	D22	
		CY7C269-50WMB	W22	
		CY7C269-50LMB	L64	
		CY7C269-50QMB	Q64	

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
60	80	CY7C268-60DC	D20	Commercial
		CY7C268-60WC	W20	
		CY7C269-60PC	P21	
		CY7C269-60DC	D22	
		CY7C269-60WC	W22	
	100	CY7C268-60DMB	D20	Military
		CY7C268-60WMB	W20	
		CY7C268-60LMB	L55	
		CY7C268-60QMB	Q55	
		CY7C269-60DMB	D22	
		CY7C269-60WMB	W22	
		CY7C269-60LMB	L64	
		CY7C269-60QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AS}	7,8,9,10,11
t_{HA}	7,8,9,10,11
t_{CO}	7,8,9,10,11
t_{PW}	7,8,9,10,11
t_{SES}	7,8,9,10,11
t_{HES}	7,8,9,10,11
t_{COS}	7,8,9,10,11

Diagnostic Mode Switching Characteristics

Parameters	Subgroups
t_{SSDI}	7,8,9,10,11
t_{HSDI}	7,8,9,10,11
t_{DSDO}	7,8,9,10,11
t_{DCL}	7,8,9,10,11
t_{DCH}	7,8,9,10,11
t_{HM}[1]	7,8,9,10,11
t_{MS}	7,8,9,10,11
t_{SS}	7,8,9,10,11

Note:
1. 7C269 only.

Document #: 38-00069-A

CY7C271
CY7C274

CYPRESS SEMICONDUCTOR

32,768 x 8 PROM Power Switched and Reprogrammable

Features

- CMOS for optimum speed/power
- Windowed for reprogrammability
- High speed
  - — 35 ns (commercial)
  - — 45 ns (military)
- Low power
  - — 660 mW (commercial)
  - — 715 mW (military)
- Super low standby power
  - — Less than 165 mW when deselected
- EPROM technology 100% programmable
- 5V ±10% V_{CC}, commercial and military
- TTL compatible I/O
- Slim 300 mil package (7C271)
- Direct replacement for bipolar PROMs
- Capable of withstanding > 2001V static discharge

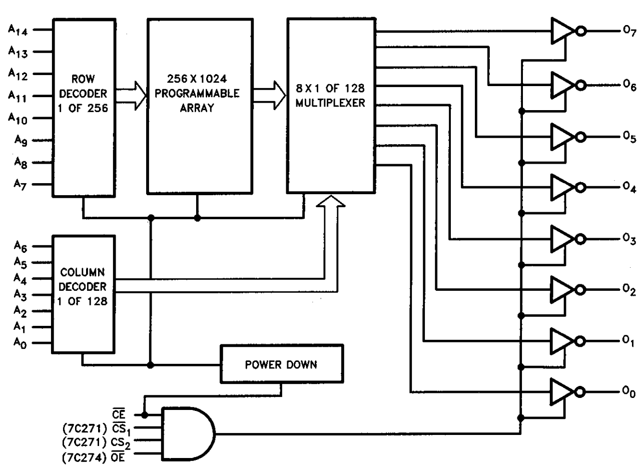
Product Characteristics

The CY7C271 and CY7C274 are high performance 32,768 word by 8 bit CMOS PROMS. When disabled ($\overline{CE}$ HIGH), the 7C271/274 automatically powers down into a low power standby mode. The CY7C271 is packaged in the 300 mil slim package. The CY7C274 is packaged in the industry standard 600 mil package. Both the 7C271 and 7C274 are available in a CERDIP package equipped with an erasure window to provide for reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C271 and CY7C274 offer the advantage of lower power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading the 7C271 is accomplished by placing active LOW signals on $\overline{CS}_1$ and $\overline{CE}$, and an active HIGH on CS_2. Reading the 7C274 is accomplished by placing active LOW signals on $\overline{OE}$ and $\overline{CE}$. The contents of the memory location addressed by the address lines (A_0–A_{14}) will become available on the output lines (O_0–O_7).

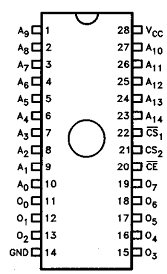
Logic Block Diagram



0102-1

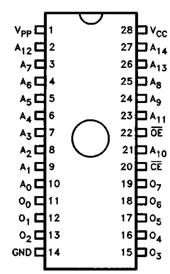
Pin Configurations

CY7C271

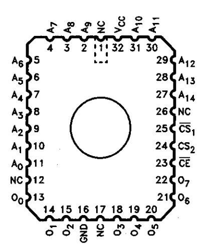


0102-2

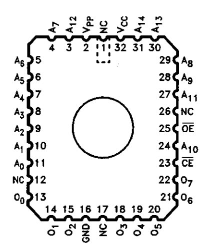
CY7C274



0102-10



0102-3



0102-11

Selection Guide

		7C271-35 7C274-35	7C271-45 7C274-45	7C271-55 7C274-55
Maximum Access Time (ns)		35	45	55
Maximum Operating Current (mA)	Commercial	120	120	120
	Military		130	130
Standby Current (mA)	Commercial	30	30	30
	Military		40	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage 13.0V

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latchup Current .... >200 mA

UV Exposure .... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[4]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[5]

Parameters	Description	Test Conditions		7C271-35, 45, 55 7C274-35, 45, 55 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA*			0.4	V
V_{IH}	Input HIGH Level[1]			2.0	V_{CC}	V
V_{IL}	Input LOW Level[1]				0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−40	+40	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = 2.0V I_{OUT} = 0 mA	Commercial		120	mA
			Military		130	mA
I_{SB}	Standby Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH} I_{OUT} = 0 mA	Commercial		30	mA
			Military		40	mA

*6.0 mA military

Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	

Notes:
1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C271 and CY7C274 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. T_A is the "instant on" case temperature.
5. See the last page of this specification for Group A subgroup testing information.
6. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[5, 7]

Parameters	Description	7C271-35 7C274-35		7C271-45 7C274-45		7C271-55 7C274-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		35		45		55	ns
t_{HZCS}	Chip Select Inactive to High Z[8] ($\overline{CS}_1$ and CS_2–7C271 Only)		25		30		30	ns
t_{ACS}	Chip Select Active to Output Valid ($\overline{CS}_1$ and CS_2–7C271 Only)		25		30		30	ns
t_{HZOE}	Output Enable Inactive to High Z[8] ($\overline{OE}$–7C274 Only)		25		25		30	ns
t_{OE}	Output Enable Active to Output Valid ($\overline{OE}$–7C274 Only)		25		25		30	ns
t_{HZCE}	Chip Enable Inactive to High Z[8] ($\overline{CE}$ Only)		40		50		60	ns
t_{ACE}	Chip Enable Active to Output Valid ($\overline{CE}$ Only)		40		50		60	ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		40		50		60	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

3

AC Test Loads and Waveforms

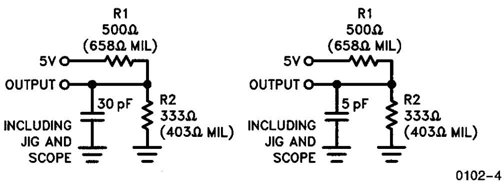


Figure 1a　　Figure 1b

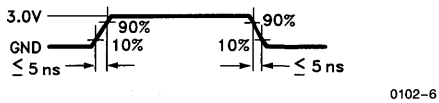
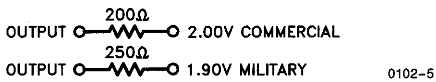
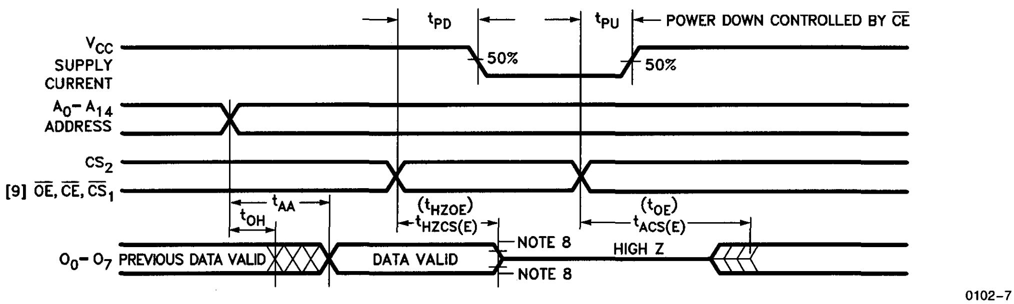


Figure 2. Input Pulses

Equivalent to:　THÉVENIN EQUIVALENT





Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b.*
8. $t_{HZCS(E)}$ and t_{HZOE} are tested with the load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5 level on the input.
9. CS_2 and $\overline{CS}_1$ are used on the 7C271 only. $\overline{OE}$ is used on the 7C274 only.

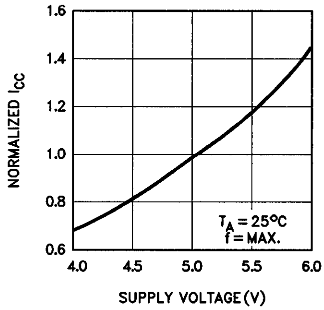
Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C271 and 7C274 in the windowed package. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

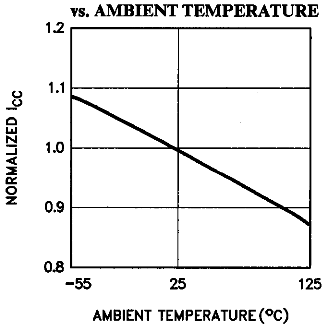
The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) or 25 Wsec/cm². For an ultraviolet lamp with a 12 mW/cm² power rating the exposure time would be approximately 45 minutes. The 7C271 and 7C274 need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm² is the recommended maximum dosage.

Typical DC and AC Characteristics

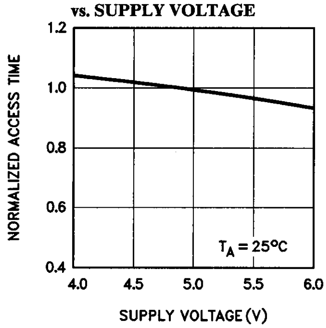
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



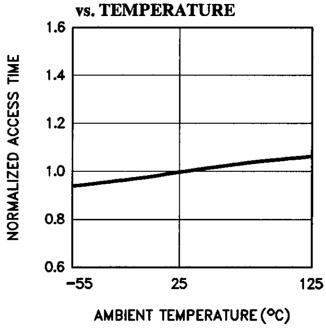
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



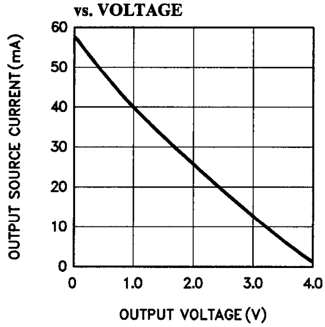
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



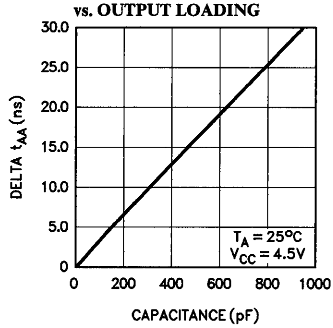
NORMALIZED ACCESS TIME vs. TEMPERATURE



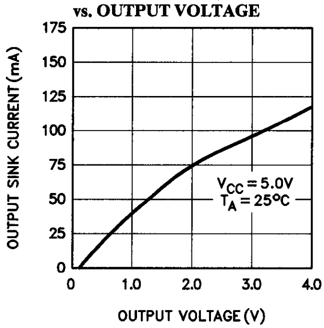
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



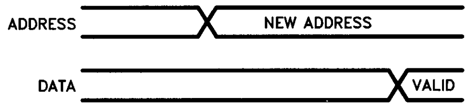
0102–13

Read Mode Table

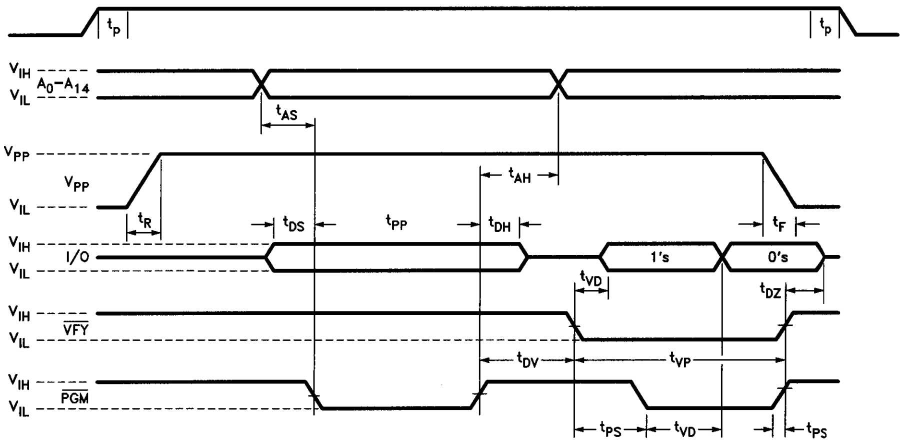
Part	V_{PP}	PGM	VFY
7C271	V_{IL}	V_{IH}	V_{IL}
7C274	V_{IL}	V_{IL}	V_{IL}

Reading PROMs

Below are timing diagrams for the final read of the PROMs. Use 1 μs timing for pulse widths and overlaps.



0102–15



0102–9

Figure 4. PROM Programming Waveforms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C271-35PC	P21	Commercial
	CY7C271-35WC	W22	
45	CY7C271-45PC	P21	Commercial
	CY7C271-45WC	W22	
	CY7C271-45DMB	D22	Military
	CY7C271-45WMB	W22	
	CY7C271-45LMB	L55	
	CY7C271-45QMB	Q55	
55	CY7C271-55PC	P21	Commercial
	CY7C271-55WC	W22	
	CY7C271-55DMB	D22	Military
	CY7C271-55WMB	W22	
	CY7C271-55LMB	L55	
	CY7C271-55QMB	Q55	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C274-35PC	P15	Commercial
	CY7C274-35WC	W16	
45	CY7C274-45PC	P15	Commercial
	CY7C274-45WC	W16	
	CY7C274-45DMB	D16	Military
	CY7C274-45WMB	W16	
	CY7C274-45LMB	L55	
	CY7C274-45QMB	Q55	
55	CY7C274-55PC	P15	Commercial
	CY7C274-55WC	W16	
	CY7C274-55DMB	D16	Military
	CY7C274-55WMB	W16	
	CY7C274-55LMB	L55	
	CY7C274-55QMB	Q55	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7,8,9,10,11
t_{ACS}[1]	7,8,9,10,11
t_{OE}[2]	7,8,9,10,11
t_{ACE}	7,8,9,10,11

Notes:
1. 7C271 only.
2. 7C274 only.

Document #: 38-00068-D

CY7C277
CY7C279

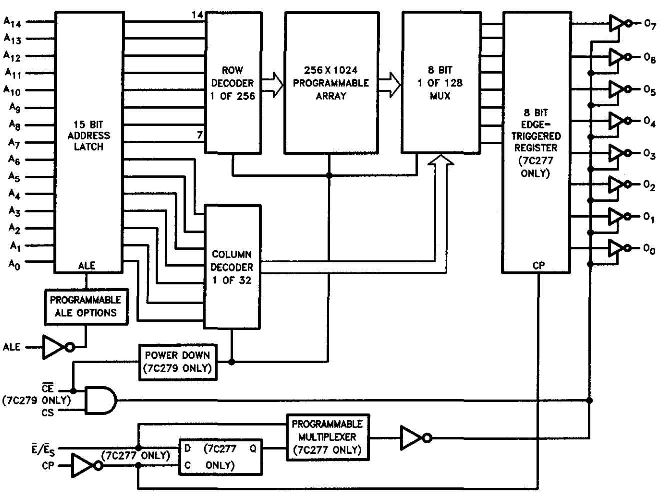
CYPRESS SEMICONDUCTOR

Reprogrammable 32,768 x 8 Registered PROM

Features

- Windowed for reprogrammability
- CMOS for optimum speed/power
- High speed
  - — 30 ns max set-up
  - — 15 ns clock to output
- Low power
  - — 660 mW (commercial)
  - — 715 mW (military)
- Programmable address latch enable input
- Programmable synchronous or asynchronous output enable (7C277)
- On-chip edge-triggered registers
- EPROM technology, 100% programmable
- Slim 300 mil, 28-pin plastic or hermetic DIP
- 5V ±10% V_{CC}, commercial and military
- TTL compatible I/O
- Direct replacement for bipolar PROMs
- Capable of withstanding greater than 2000V static discharge

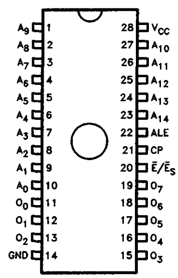
Logic Block Diagram



0136-1

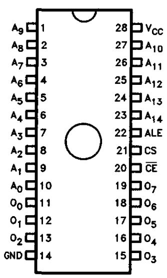
Pin Configurations

CY7C277



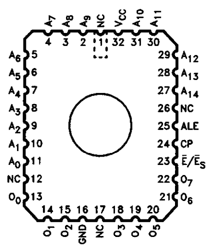
0136-2

CY7C279



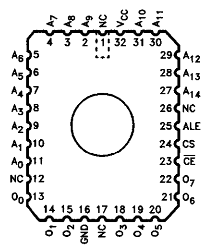
0136-3

LCC Pinout



0136-4

LCC Pinout



0136-5

Selection Guide

		7C279-35	7C277-30	7C279-45	7C277-40	7C279-55	7C277-50
Maximum Access Time (ns)		35		45		55	
Maximum Setup Time (ns)			30		40		50
Maximum Clock to Output (ns)			15		20		25
Maximum Operating Current (mA)	Commercial	120	120	120	120	120	120
	Military			130	130	130	130
Maximum Standby Current (mA)	Commercial	30		30		30	
	Military			40		40	

Product Characteristics

The CY7C277 and CY7C279 are high performance 32,768 word by 8 bit CMOS PROMs. When deselected, the 7C279 automatically powers down into a low power standby mode. The 7C277 and the 7C279 both are packaged in the slim 28 pin 300 mil package. The ceramic package may be equipped with an erasure window; when exposed to UV light, the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide algorithms.

The CY7C277 and CY7C279 offer the advantages of lower power, reprogrammability, superior performance and high programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the project will meet DC and AC specification limits.

On the 7C277, the outputs are pipelined through a master-slave register. On the rising edge of CP, data is loaded into the 8 bit edge triggered output register. The $\overline{E}/\overline{E}_S$ provides a programmable bit to select between asynchronous and synchronous operation. The default condition is asynchronous. When the asynchronous mode is selected, the $\overline{E}/\overline{E}_S$ pin is sampled continuously and operates as an output enable. If the synchronous mode is selected, then the $\overline{E}/\overline{E}_S$ pin is sampled only when CP is HIGH. Enabling the outputs in this mode is accomplished by bringing the $\overline{E}_S$ pin LOW and pulsing the CP HIGH to latch the output enable state. The 7C277 also provides a programmable bit to enable the ADDRESS LATCH ENABLE (ALE) pin. If this bit is not programmed, then the device will ignore the ALE pin. If the ALE function is selected, the user may define the polarity of the ALE signal with the default being a positive ACTIVE signal.

On the 7C279, address registers are provided to easily interface with the Cypress 7C601 and other microprocessors that clock their addresses. A programmable bit is provided to select between Latched and Registered address inputs. The default is registered inputs, which will sample the address on the RISING EDGE of ALE and latch the address into the address register. The Latched address option will recognize any address changes while the ALE pin is ACTIVE and latch the address into the address registers on the FALLING EDGE of ALE. If the latched address option is selected, then another programmable bit is provided for the user to select the polarity that will define ALE ACTIVE, with the default being positive polarity.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).................. −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage.................. −3.0V to +7.0V

DC Program Voltage (Pins 7, 18, 20) 13.0V

UV Erasure.........................7258 Wsec/cm^2

Static Discharge Voltage ....>2001V (Per MIL-STD-883 Method 3015)

Latchup Current ....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[2]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[3]

Parameters	Description	Test Conditions		7C277-30 7C279-35		7C277-40, 50 7C279-45, 55		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level[4]			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Level[4]				0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Clamp Diode Voltage			Note 5				
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled[6]		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.0V[7]		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IH} = 2.0V I_{OUT} = 0 mA	Commercial		120		120	mA
			Military				130	
I_{SB}[11]	Standby Supply Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH} I_{OUT} = 0 mA	Commercial		30		30	mA
			Military				40	

Capacitance[8]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C, f = 1\ MHz$ $V_{CC} = 5.0V$	8	pF
C_{OUT}	Output Capacitance		8	

Notes:
1. The 7C279 only has a standby mode.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
5. The CMOS process does not provide a clamp diode. However, the CY7C277 and CY7C279 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
6. For devices using the synchronous enable,the device must be clocked after applying these voltages to perform this measurement.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
8. Tested initially and after any design or process changes that may affect these parameters.

3

Switching Characteristics Over Operating Range[8]

Parameters	Description	7C277-30		7C277-40		7C277-50		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AL}	Address Setup to ALE Active	5		10		10		ns
t_{LA}	Address Hold from ALE Inactive	10		10		15		ns
t_{LL}	ALE Pulse Width	10		10		15		ns
t_{SA}	Address Setup to Clock HIGH	30		40		50		ns
t_{HA}	Address Hold from Clock HIGH	0		0		0		ns
t_{SES}	$\overline{E}_S$ Setup to Clock HIGH	12		15		15		ns
t_{HES}	$\overline{E}_S$ Hold from Clock HIGH	5		10		10		ns
t_{CO}[14]	Clock HIGH to Output Valid		15		20		25	ns
t_{PWC}	Clock Pulse Width	15		20		20		ns
t_{LZC}	Output Low Z from Clock HIGH		20		20		30	ns
t_{HZC}[14, 9]	Output High Z from Clock HIGH		20		20		30	ns
t_{LZE}	Output Low Z from $\overline{E}$ LOW		20		20		30	ns
t_{HZE}[15, 9]	Output High Z from $\overline{E}$ HIGH		20		20		30	ns

Switching Characteristics Over Operating Range[8] (Continued)

Parameters	Description	7C279-35		7C279-45		7C279-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}[12]	Clock to Output Valid		35		45		55	ns
t_{HZCS}	Chip Select Inactive to High Z		25		30		30	ns
t_{ACS}	Chip Select Active to Output Valid		25		30		30	ns
t_{AR}	Address Register Setup to ALE Active	3		10		10		ns
t_{RA}	Address Hold from ALE Active	6		10		10		ns
t_{ADH}	Data Hold from ALE Active	5		5		5		ns
t_{PU}	Chip Enable Active to Power Up	0		0		0		ns
t_{PD}	Chip Enable Inactive to Power Down		40		50		60	ns
t_{OH}[12]	Output Hold from Address Change	0		0		0		ns
t_{PWA}	Address Register Pulse Width		10		20		30	ns

Notes:

9. t_{HZCS} and t_{HZE} are tested wtih the load shown in *Figure 1b*. Transition is measured at steady state high level −500 mV or steady state low level +500 mV on the output from the 1.5V level on the input.
10. These parameters apply to the 7C277 only.
11. These parameters apply to the 7C279 only.
12. t_{AA} and t_{OH} apply only when the latched mode is selected.
13. Tests are performed with rise and fall times of 5 ns or less.
14. Applies only when the synchronous ($\overline{E}_S$) function is used.
15. Applies only when the asynchronous ($\overline{E}$) function is used.
16. See *Figure 1a* for all switching characteristics except t_{HZCS} and t_{HZE}.
17. See the last page of this specification for Group A subgroup testing information.
18. All device test loads should be located within 2″ of device outputs.

AC Test Loads and Waveforms[9, 16, 18]

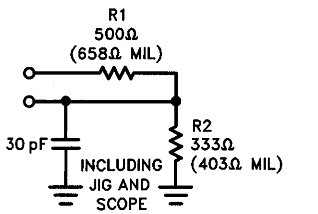


Figure 1a

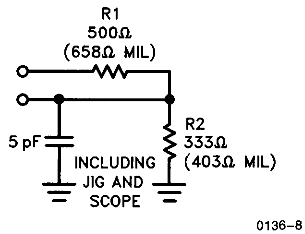


Figure 1b

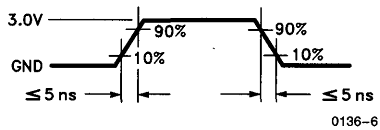
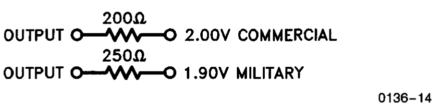


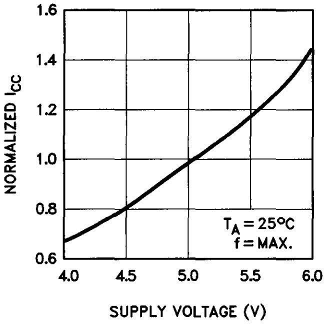
Figure 2

Equivalent to: THÉVENIN EQUIVALENT

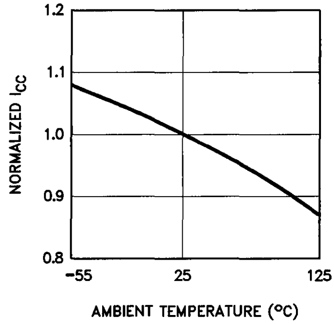


Typical DC and AC Characteristics

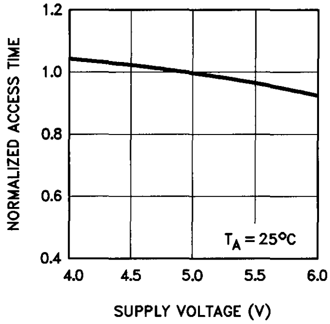
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



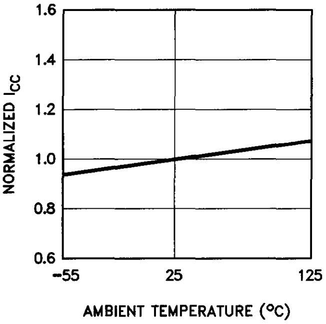
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



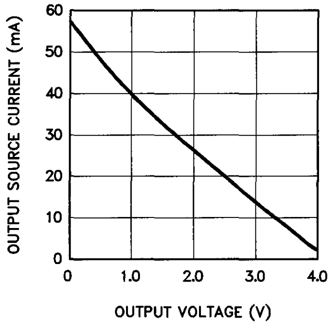
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



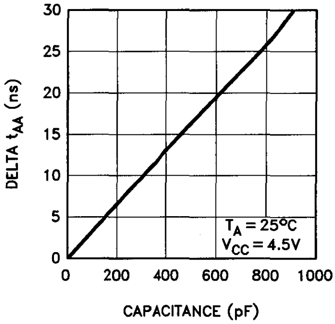
NORMALIZED ACCESS TIME vs. TEMPERATURE



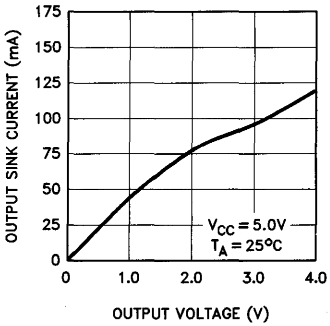
OUTPUT SOURCE CURRENT vs. VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING

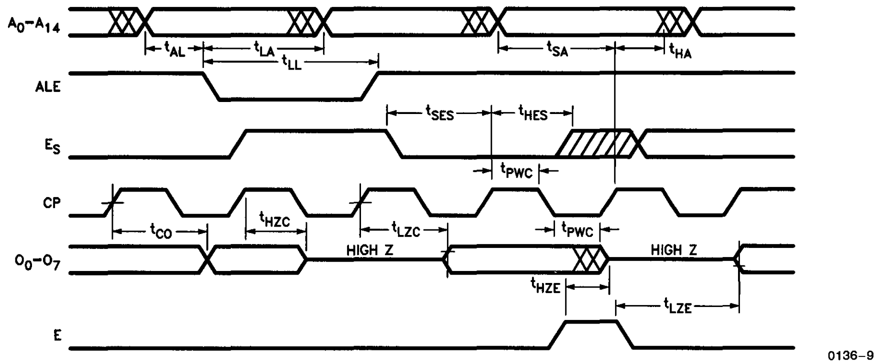


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



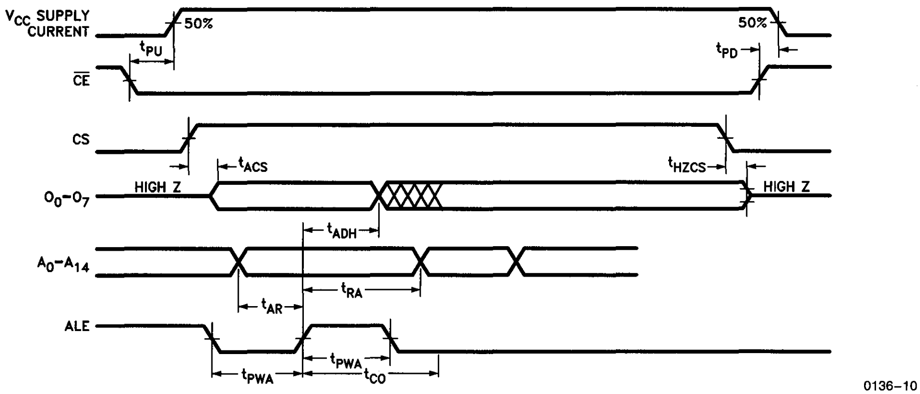
0136–15

Timing Diagram (7C277)



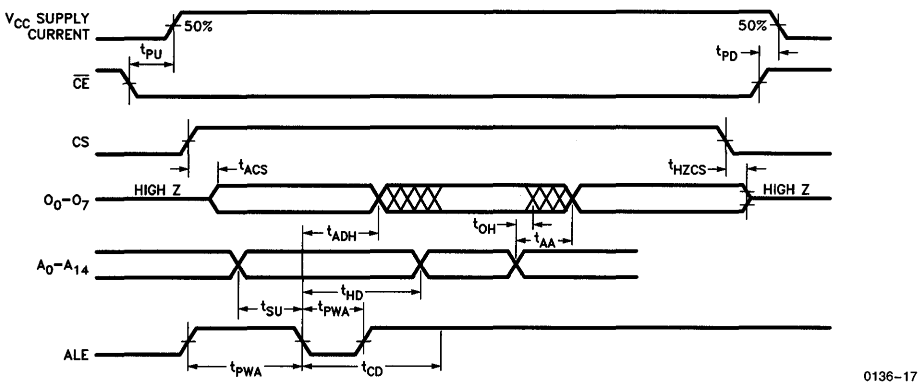
Timing Diagram (7C279)

Registered



Note:
ALE is shown with positive polarity.

Positive ALE



Note:
Negative ALE is a programmable option.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C277 and 7C279. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 45 minutes. The 7C277 and 7C279 need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Device Programming

There are several independent programmable functions contained in the 7C277 and 7C279 CMOS 32K x 8 registered PROM. Both devices have the 32K x 8 array and a programmable ALE function. The 7C277 also contains a programmable synchronous function ($\overline{E}/\overline{E}_S$).

All of the programming elements are EPROM cells and are in an erased state when they are shipped. This erased state manifests itself differently in each case. The erased state for the synchronous function is ASYNCHRONOUS mode. The erased state for the ALE function is: Registered inputs on the 7C279 and no ALE function on the 7C277. In the erased state, the memory location contains neither a one nor a zero. The erased state of the device can be verified by using the BLANK CHECK ONES and BLANK CHECK ZEROS function (see mode table).

To choose the ALE function, the ALE bit must be programmed. This is done by raising A_9 to V_{PP}, taking A_{14} LOW and pulsing $\overline{PGM}$ LOW. When the ALE function is chosen, it is active with positive polarity. To choose negative polarity, A_9 must be at V_{PP}, A_{14} must be raised HIGH and $\overline{PGM}$ must be pulsed LOW. The 7C277 comes with a synchronous option. To choose this option, the SYN bit must be programmed. This is done by taking A_{14} to V_{PP} and pulsing $\overline{PGM}$ LOW.

To verify these special bits, A_{14} must be at V_{PP} and the V_{PP} must be held LOW with $\overline{PGM}$ held HIGH and $\overline{CE}$ LOW. The ALE bit is read on I/O_1, the polarity bit is read on I/O_2 and the synchronous bit is read on I/O_0.

3

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}[1]	Programming Voltage	12.0	13.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input High Voltage	3.0	V_{CCP}	V
V_{ILP}	Input Low Voltage		0.4	V
V_{OH}[2]	Output High Voltage	2.4		V
V_{OL}[2]	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width	0.1	10	ms
t_{AS}	Address Setup Time to $\overline{PGM}/\overline{VFY}$	1.0		μs
t_{DS}	Data Setup Time to $\overline{PGM}$	1.0		μs
t_{AH}	Address Hold Time from $\overline{PGM}/\overline{VFY}$	1.0		μs
t_{DH}	Data Hold Time from $\overline{PGM}$	1.0		μs
t_R, t_F[3]	V_{PP} Rise and Fall Time	1.0		μs
t_{VD}	Verify to Data Out		5.0	μs
t_{VP}	Verify Pulse Width	12.0		μs
t_{DV}	Delay to Verify	1.0		μs
t_{DZ}	Verify HIGH to High Z		1.0	μs
t_P	Power Up/Down	20.0		ms
t_{PS}	$\overline{VFY}$ Setup/Hold to $\overline{PGM}$		1.0	μs

Notes:
1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Mode Table

Mode	Read	A_9	A_{14}	ALE	CP-7C277 CS-7C279	$\overline{E}/\overline{E}_S$-7C277 $\overline{CE}$-7C279	A_0-A_8 $A_{10}-A_{13}$	Data
	Program	A_9	A_{14}	V_{PP}	$\overline{PGM}$	$\overline{VFY}$	A_0-A_8 $A_{10}-A_{13}$	Data
Read		A	A	V_{IL}	V_{IH}	V_{IL}	A	Out
Program		A	A	V_{PP}	V_{IL}	V_{IH}	A	In
Program SYN Bit		X	V_{PP}	V_{PP}	V_{IL}	V_{IH}	X	X
Program ALE Bit		V_{PP}	V_{IL}	V_{PP}	V_{IL}	V_{IH}	X	X
Program ALE Low Polarity		V_{PP}	V_{IH}	V_{PP}	V_{IL}	V_{IH}	X	X
Program Verify[1]		A	A	V_{PP}	V_{IH}, V_{IL}	V_{IL}	A	Out
Program Inhibit		A	A	V_{PP}	V_{IH}	V_{IH}	A	X
Blank Check 0, 1[2]		A	A	V_{IH}, V_{IL}	V_{PP}	V_{PP}	A	Out
Verify Special Bits		X	V_{PP}	V_{IL}	V_{IH}	V_{IL}	X	Out

Notes:

1. During program verify $\overline{PGM}$ must first be held HIGH to verify ones and then LOW to verify zeros.
2. To blank check zeros, V_{PP} is held to V_{IH} and all ones should be read on the outputs. To blank check ones, V_{PP} is held to V_{IL} and all zeros should be read on the outputs.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C277-30PC	P21	Commercial
	CY7C277-30WC	W22	
	CY7C279-35PC	P21	
	CY7C279-35WC	W22	
45	CY7C277-40PC	P21	Commercial
	CY7C277-40WC	W22	
	CY7C279-45PC	P21	
	CY7C279-45WC	W22	
	CY7C277-40DMB	D22	Military
	CY7C277-40WMB	W22	
	CY7C277-40LMB	L55	
	CY7C277-40QMB	Q55	
	CY7C279-45DMB	D22	
	CY7C279-45WMB	W22	
	CY7C279-45LMB	L55	
	CY7C279-45QMB	Q55	
55	CY7C277-50 PC	P21	Commercial
	CY7C277-50WC	W22	
	CY7C279-55PC	P21	
	CY7C279-55 WC	W22	
	CY7C277-50DMB	D22	Military
	CY7C277-50WMB	W22	
	CY7C277-50LMB	L55	
	CY7C277-50QMB	Q55	
	CY7C279-55DMB	D22	
	CY7C279-55WMB	W22	
	CY7C279-55LMB	L55	
	CY7C279-55QMB	Q55	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}[11]	1,2,3

Switching Characteristics

Device	Parameters	Subgroups
7C277	t_{SA}	7,8,9,10,11
	t_{HA}	7,8,9,10,11
	t_{CO}	7,8,9,10,11
7C279	t_{AR}	7,8,9,10,11
	t_{RA}	7,8,9,10,11
	t_{DHA}	7,8,9,10,11

Note:
11. These parameters apply to the 7C279 only.

Document #: 38-00085-A

CY7C281
CY7C282

CYPRESS SEMICONDUCTOR

1024 x 8 PROM

Features

- **CMOS for optimum speed/ power**
- **High speed**
  - **— 30 ns (commercial)**
  - **— 45 ns (military)**
- **Low power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300 or standard 600 mil DIP or 28 pin LCC**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding > 1500V static discharge**

Product Characteristics

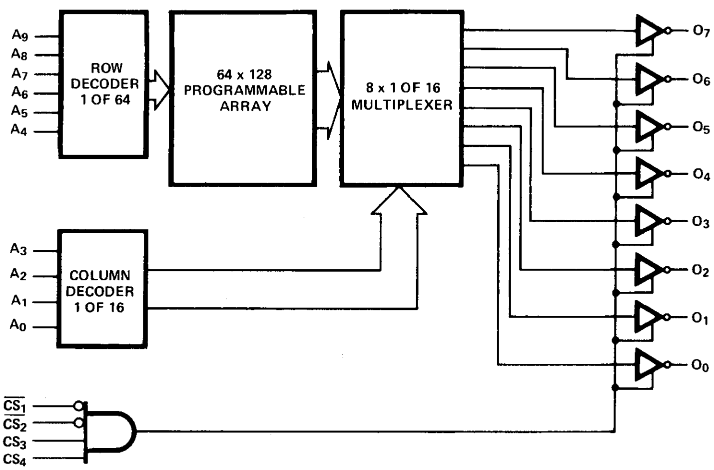
The CY7C281 and CY7C282 are high performance 1024 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil and 600 mil wide packages respectively. The CY7C281 is also available in a 28 pin leadless chip carrier. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C281 and CY7C282 are plug-in replacements for bipolar devices and offer the advantages of lower power, superior performance and programming yield. The EPROM cell requires only 13.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercized prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$ and $\overline{CS}_2$, and active HIGH signals on CS_3 and CS_4. The contents of the memory location addressed by the address lines ($A_0 - A_9$) will become available on the output lines ($O_0 - O_7$).

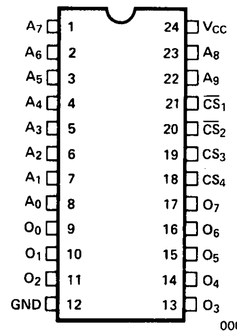
3

Logic Block Diagram

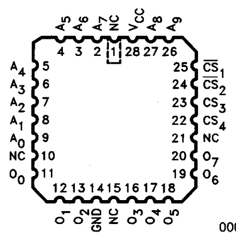


0009–1

Pin Configurations



0009–2



0009–3

Selection Guide

		7C281-30 7C282-30	7C281-45 7C282-45
Maximum Access Time (ns)		30	45
Maximum Operating Current (mA)	Commercial	100	90
	Military		120

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 14.0V

Static Discharge Voltage .... >1500V (per MIL-STD-883, Method 3015)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C281-30 7C282-30		7C281-45 7C282-45		Units
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Level[3]			2.0		2.0		V
V_{IL}	Input LOW Level[3]				0.8		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 4		Note 4		
I_{OZ}	Output Leakage Current	V_{OL} ≤ V_{OUT} ≤ V_{OH}, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[5]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		100		90	mA
			Military				120	mA

Capacitance[6]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. The CMOS process does not provide a clamp diode. However, the CY7C281 & CY7C282 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
5. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
6. Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics Over the Operating Range[2, 7]

Parameters	Description	CY7C281-30 CY7C282-30		CY7C281-45 CY7C282-45		Units
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		30		45	ns
t_{HZCS}	Chip Select Inactive to High Z[8]		20		25	ns
t_{ACS}	Chip Select Active to Output Valid		20		25	ns

AC Test Loads and Waveforms

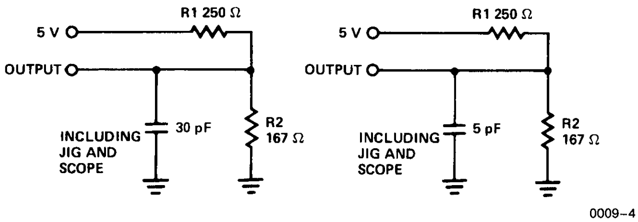


Figure 1a **Figure 1b**

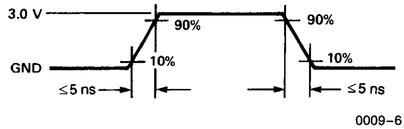
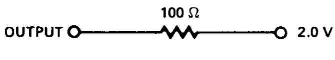
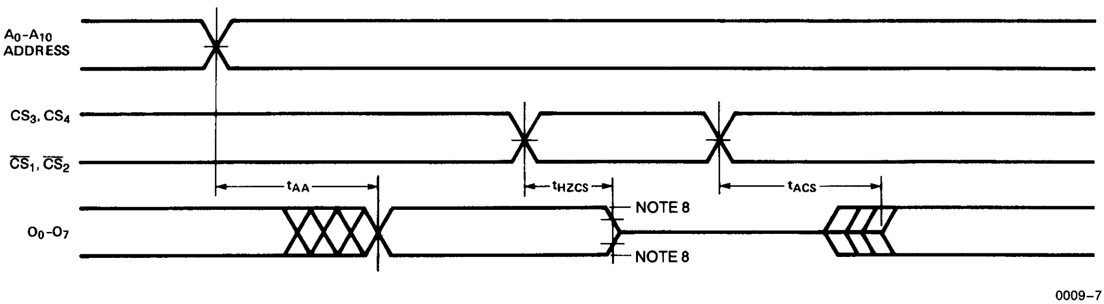


Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



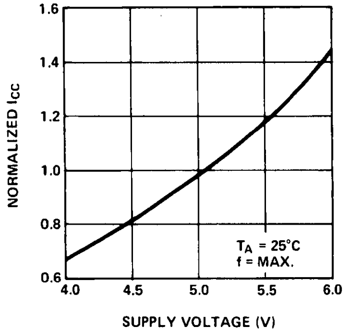


Notes:

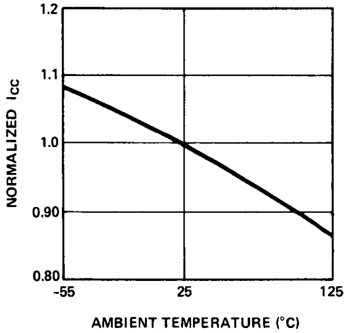
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figure 1a, 1b*.
8. t_{HZCS} is tested with load shown in *Figure 1b*. Transition is measured at steady state High level + 500 mV or steady state Low level + 500 mV on the output from the 1.5V level on the input.

Typical DC and AC Characteristics

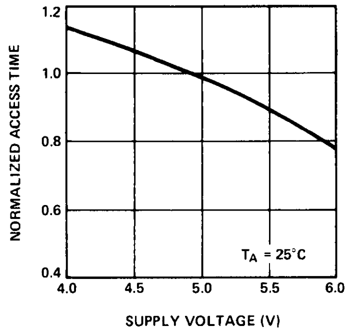
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



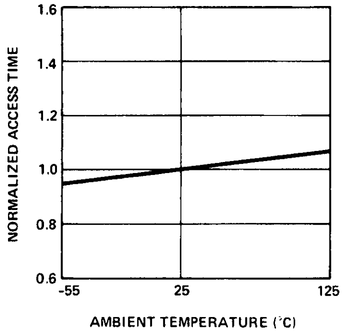
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



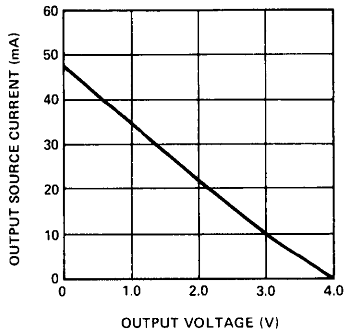
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



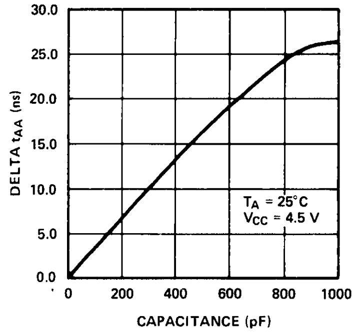
NORMALIZED ACCESS TIME vs. TEMPERATURE



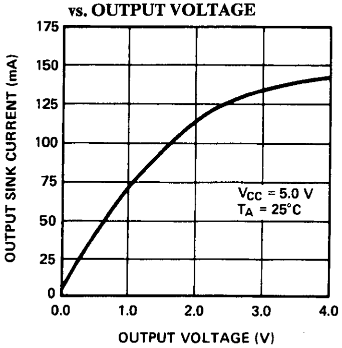
OUTPUT SOURCE CURRENT vs. VOLTAGE



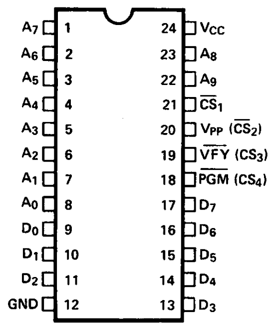
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



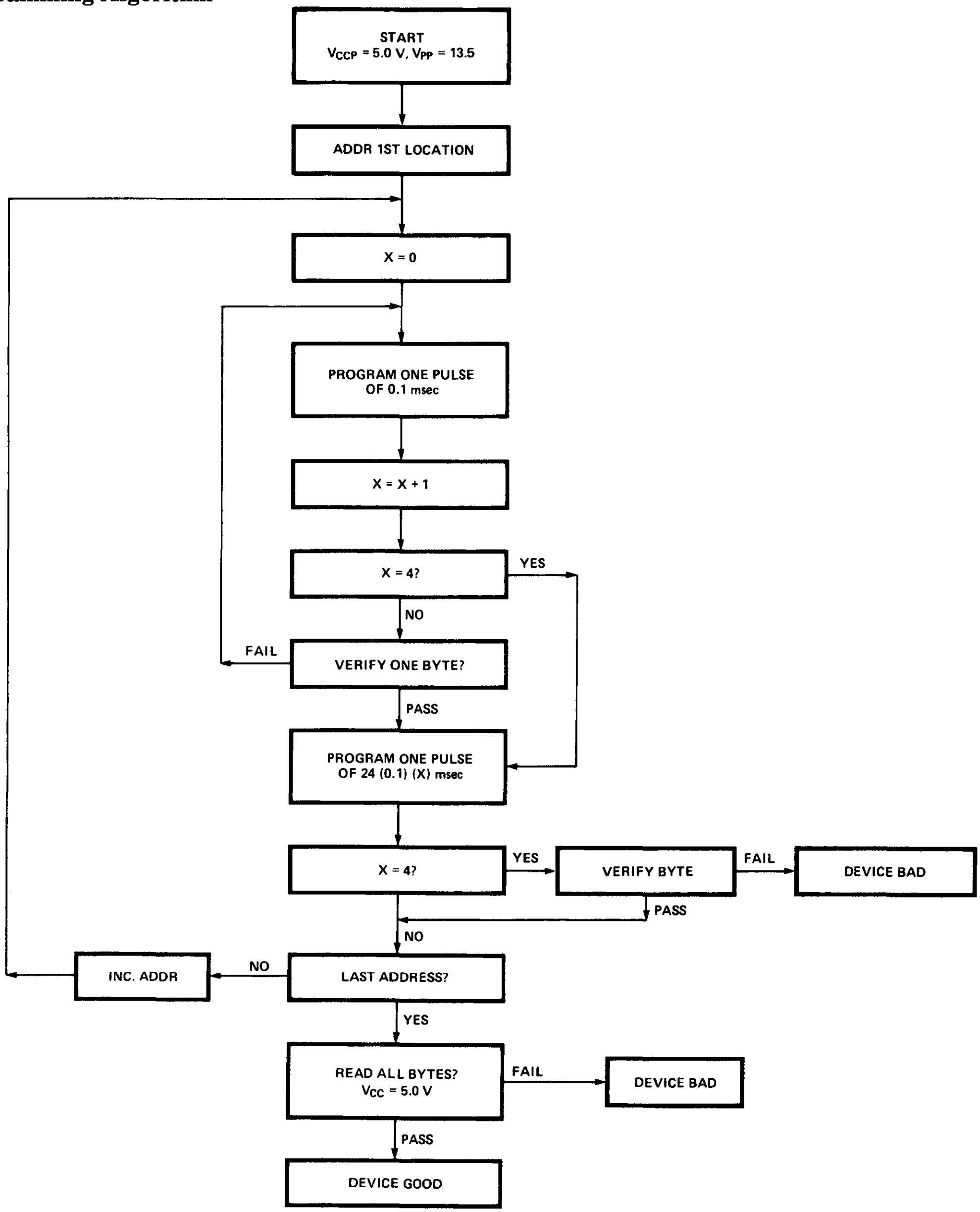
0009–8



0009–9

Figure 3. Programming Pinout

Programming Algorithm



The CY7C281 and CY7C282 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at V_{CC} = 5.0. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

Figure 4. Programming Flowchart

Programming Information

The 7C281 and 7C282 1K x 8 CMOS PROMs are implemented with a differential EPROM memory cell. The PROMS are delivered in an erased state, containing neither "1s" nor "0s". This erased condition of the array may be assessed using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see below.

Blank Check

A virgin device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In both of these modes, address and read locations 0 thru 1023. A device is considered virgin if all locations are respectively "1s" and "0s" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is neccessary to program both ones and zeros. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage[1]	13.0	14.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input HIGH Voltage	3.0		V
V_{ILP}	Input LOW Voltage		0.4	V
V_{OH}	Output HIGH Voltage[2]	2.4		V
V_{OL}	Output LOW Voltage[2]		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width[3]	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F	V_{PP} Rise and Fall Time[3]	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify to High Z		1.0	μs

Notes:
1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function				Outputs
	Read or Output Disable	CS_4	CS_3	$\overline{CS_2}$	$\overline{CS_1}$	Outputs
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	$\overline{CS_1}$	(9–11, 13–17)
	Pin Number	(18)	(19)	(20)	(21)	
Read		V_{IH}	V_{IH}	V_{IL}	V_{IL}	Data Out
Output Disable[4]		X	X	V_{IH}	X	High Z
Output Disable[4]		X	V_{IL}	X	X	High Z
Output Disable[4]		V_{IL}	X	X	X	High Z
Output Disable[4]		X	X	X	V_{IH}	High Z
Program		V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	Data In
Program Verify		V_{IHP}	V_{ILP}	V_{PP}	V_{ILP}	Data Out
Program Inhibit		V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	High Z
Intelligent Program		V_{ILP}	V_{IHP}	V_{PP}	V_{ILP}	Data In
Blank Check Ones		V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	Ones
Blank Check Zeros		V_{PP}	V_{IHP}	V_{ILP}	V_{ILP}	Zeros

Notes:
4. X = Don't care but not to exceed V_{CC} + 5%.
5. During programming and verification, all unspecified pins to be at V_{ILP}.

3

Programming Sequence 1K x 8

Power the device for normal read mode operation with pin 18, 19, 20, and 21 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Tables 3 and 4. Again per *Figure 5* address program and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24 × the sum of the previous programming pulses before advancing to the next address to repeat the process.

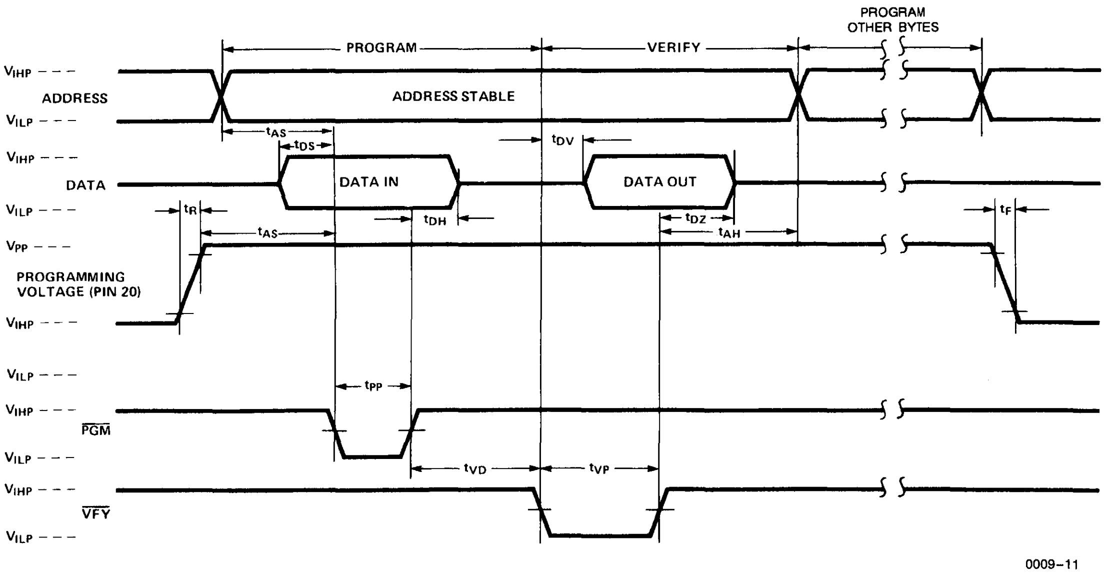


Figure 5. Programming Waveforms

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30 ns	CY7C281-30PC	P13	Commercial
	CY7C282-30PC	P11	
	CY7C281-30DC	D14	
	CY7C281-30LC	L64	
	CY7C282-30DC	D12	
45 ns	CY7C281-45PC	P13	Commercial
	CY7C282-45PC	P11	
	CY7C281-45DC	D14	
	CY7C281-45LC	L64	
	CY7C282-45DC	D12	
	CY7C281-45DMB	D14	Military
	CY7C281-45LMB	L64	
	CY7C282-45DMB	D12	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7,8,9,10,11
t_{ACS}	7,8,9,10,11

Document #: 38-00006-B

CYPRESS SEMICONDUCTOR

65,536 x 8 PROM Reprogrammable Fast Column Access

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **Unique fast column access**
  - **— 20 ns t_{AA} (commercial)**
  - **— 30 ns t_{AA} (military)**
- **WAIT signal**
- **Chip select decoding**
- **EPROM technology, 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL-compatible I/O**
- **Slim 300-mil package**
- **Capable of withstanding > 2001V static discharge**

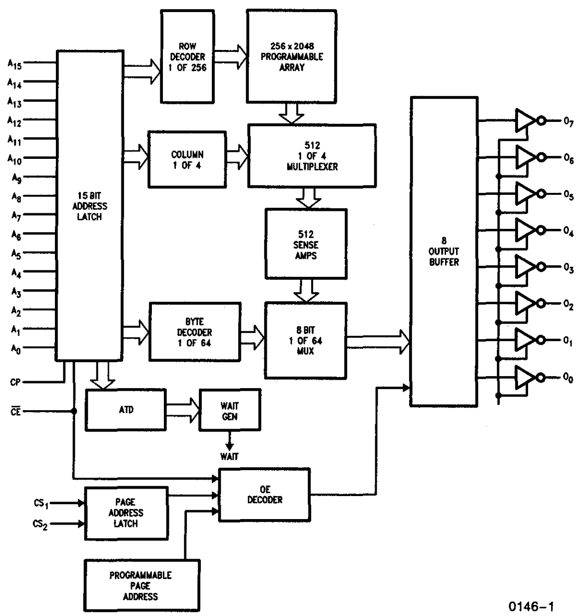
Product Characteristics

The CY7C285 and the CY7C289 are high-performance 65,536 x 8 bit CMOS PROMs. The CY7C285 is available in a 28-pin 300-mil package. It features a unique fast column access feature which will allow access times as fast as 25 ns for each byte in a 64-byte page. There are 1024 pages in the device. The access time when changing pages will be 75 ns. In order to easily facilitate the use of the fast column access feature, a WAIT signal will be generated to advise the processor of a page change. The CY7C289 also incorporates the fast column access feature and adds through the use of the ALE option either synchronous address registers or asynchronous address latches. The CY7C289 is particularly well-suited to support applications using the CY7C601 as well as other RISC or CISC microprocessors. It is available in a 32-pin 300-mil package.

The CY7C285 and CY7C289 offer the advantage of low power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading the CY7C285 is accomplished by placing an active LOW signal on the CS pin. Reading the CY7C289 is accomplished by placing an active LOW signal on the CE pin and by placing active HIGH signals on the CS_1 or CS_2 pins as appropriate. The contents of the memory location addressed by the address lines (A_0–A_{15}) will become available on the output lines (O_0–O_7).

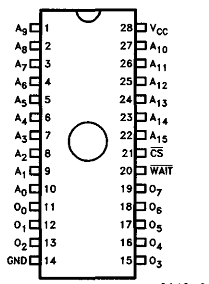
Logic Block Diagram



0146-1

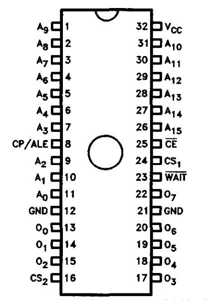
Pin Configurations

CY7C285



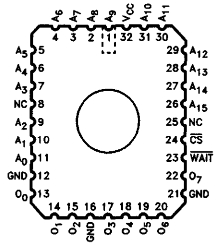
0146-2

CY7C289



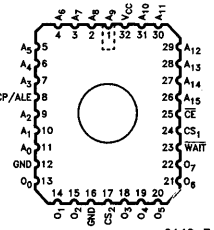
0146-6

LCC Pinout



0146-3

LCC Pinout



0146-7

Selection Guide

	Description		7C289-65	7C285-75	7C289-75
Maximum Access Time (ns)	Page Access Time		65	75	75
	Column Access Time		20	25	25
Maximum Operating Current (mA)		Commercial	180	180	180
		Military		200	200

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V
(7C285: Pin 28 to Pin 14)
(7C289: Pin 32 to Pin 16)

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage 13.0V
(7C285: Pins 21, 22)
(7C289: Pins 24, 26)

UV Exposure .... 7258 Wsec/cm²

Static Discharge Voltage .... >2001V
(per MIL-STD-883, Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[4]

Parameters	Description	Test Conditions		7C285-65, 75 7C289-65, 75		Units
				Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}[1]	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}[1]	Input LOW Voltage				0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		180	mA
			Military		200	mA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C285 and CY7C289 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. Tested initially and after any design or process changes that may affect these parameters.
4. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms[5, 6]

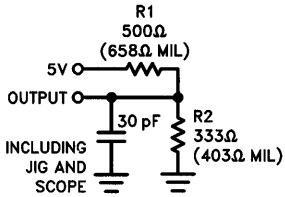
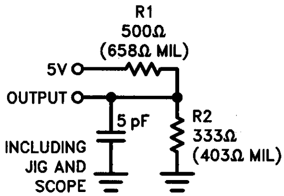
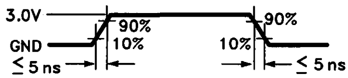


Figure 1a



0146-8

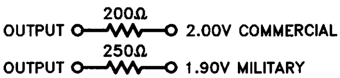
Figure 1b



0146-9

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0146-10

Notes:

5. R1 is a resistor connected from the output to V_{CC} and R2 is connected between the output and ground for testing purposes.
6. Note that R1 and R2 for 7C289 will be 961Ω and 510Ω for commercial and 1250Ω and 588Ω for military.

Switching Characteristics Over the Operating Range (7C285)

Parameters	Description	7C285-75		7C285-85		Units
		Min.	Max.	Min.	Max.	
t_{RAC}	Slow Address Access Time (A_6–A_{15})		75		85	ns
t_{CAA}	Fast Address Access Time (A_0–A_5)		25		35	ns
t_{HZCS}	Output Tristate from $\overline{CS}$		20		25	ns
t_{ACS}	Output Valid from $\overline{CS}$		20		25	ns
t_{WD}	Wait Delay from First Slow Address Change		30		35	ns
t_{DW}	Wait Hold from Data Valid	0		0		ns
t_{WW}	Wait Recovery from Last Address Change		110		120	ns
t_{PWD}	Wait Pulse Width	12		15		ns

Switching Characteristics Over the Operating Range (7C289)

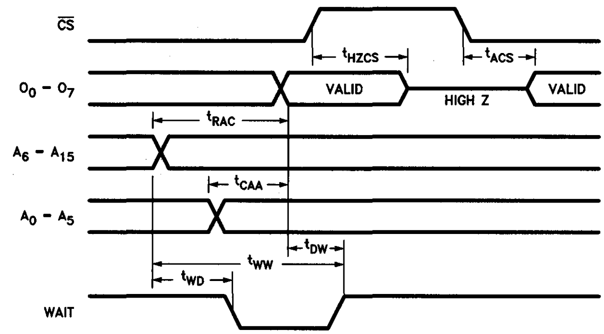
Parameters	Description		7C289-65		7C289-75		Units
			Min.	Max.	Min.	Max.	
t_{RAC1}	Slow Address Access Time (A_6-A_{15})			65		75	ns
t_{CAA1}	Fast Address Access Time (A_0-A_5)			20		25	ns
t_{AR1}	Reg. Address Set-Up Time		2		4		ns
t_{RA1}	Reg. Address Hold Time		6		6		ns
t_{AR2}	Reg. Address Set-Up Time		8		10		ns
t_{RA2}	Reg. Address Hold Time		2		4		ns
t_{HZCS}	Output Tristate from Clock HIGH			20		20	ns
t_{ACS}	Output Valid from Clock HIGH			20		20	ns
t_{PWA}	Address Reg. Pulse Width		10		15		ns
t_{ADH}	Data Hold Time	Commercial	5		5		ns
		Military			7		
t_{SCE}	Chip Enable Set-Up		2		4		ns
t_{HCE}	Chip Enable Hold		6		6		ns
t_{WD1}	Wait Delay from Clock LOW		0	19	0	25	ns
t_{WD3}	Wait Delay from Clock HIGH		0	16	0	20	ns
t_{RAC2}[7]	Slow Address Access Time (A_6-A_{15})			65		75	ns
t_{CAA2}[7]	Fast Address Access Time (A_0-A_5)			25		30	ns
t_{ACE}[7]	Output Valid from $\overline{CE}$			20		25	ns
t_{HZCE}[7]	Output Tristate from $\overline{CE}$			20		25	ns
t_{AL}[7]	Address Set-Up Time		5		8		ns
t_{LA}[7]	Address Hold Time		10		12		ns
t_{LL}[7]	ALE Pulse Width		10		12		ns
t_{PWD}[7]	Wait Pulse Width		10		12		ns
t_{WD2}[7]	Wait Delay from First Slow Address Change			25		30	ns
t_{DW2}[7]	Wait Hold from Data Valid		0		0		ns
t_{WW2}[7]	Wait Recovery from Last Address Change			100		110	ns

Note:

7. Parameters for 7C289 with ALE option enabled.

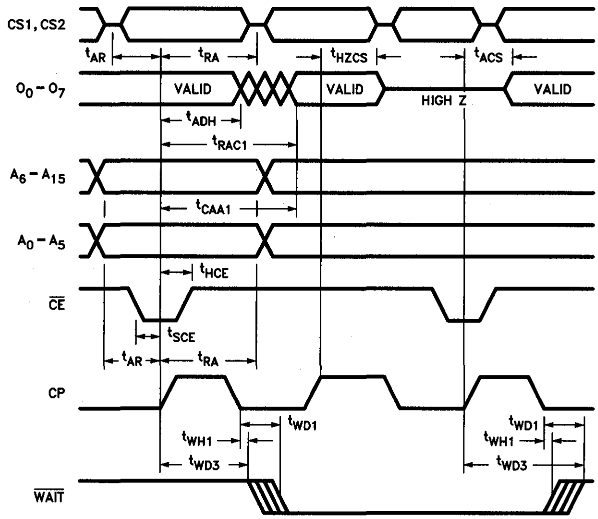
3

Switching Waveform (7C285)



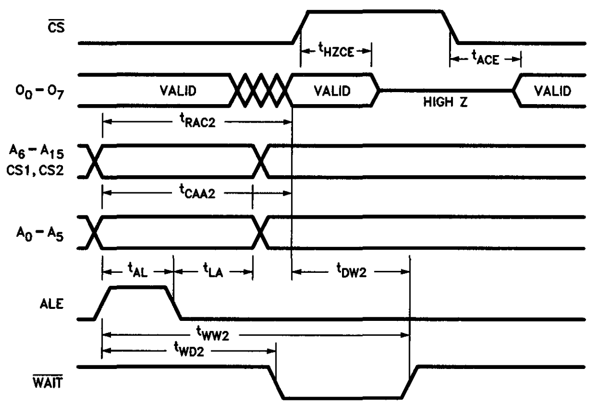
0146–11

Switching Waveform (7C289)



0146–12

ALE Option Waveform



0146–13

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
65	CY7C285-65PC	P21	Commercial
	CY7C285-65WC	W22	
75	CY7C285-75PC	P21	Commercial
	CY7C285-75WC	W22	
	CY7C285-75DMB	D22	Military
	CY7C285-75WMB	W22	
	CY7C285-75LMB	L55	
	CY7C285-75QMB	Q55	

Speed (ns)	Ordering Code	Package Type	Operating Range
65	CY7C289-65WC	W16	Commercial
75	CY7C289-75WC	W16	Commercial
	CY7C289-75DMB	D32	Military
	CY7C289-75WMB	W32	
	CY7C289-75LMB	L55	
	CY7C289-75QMB	Q55	

3

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}[8]	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7,8,9,10,11
t_{ACS}	7,8,9,10,11
t_{ACE}[8]	7,8,9,10,11

Note:
8. CY7C289 only.

Document #: 38-00097-B

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C286
CY7C287

65,536 x 8 PROM Reprogrammable Registered

Features

- **CMOS for optimum speed/power**
- **Windowed for reprogrammability**
- **High speed**
  - **— t_{SU} = 55 ns (7C287)**
  - **— t_{CO} = 20 ns (7C287)**
  - **— t_{AA} = 60 ns (7C286)**
- **Low power**
  - **— 120 mA active (7C286)**
  - **— 40 mA standby**
- **EPROM technology, 100% programmable**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Slim 300 mil package (7C287)**
- **Capable of withstanding > 2001V static discharge**

Product Characteristics

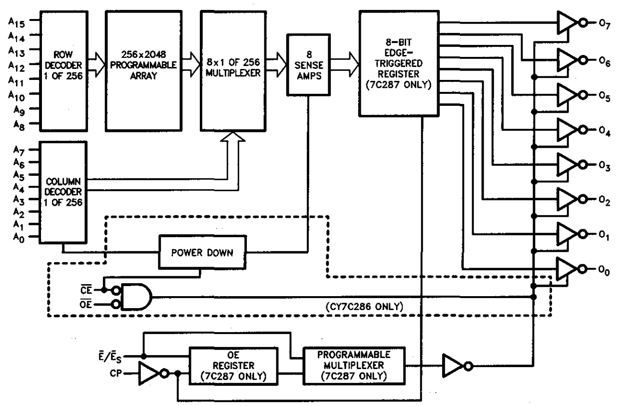
The CY7C286 and the CY7C287 are high performance 65,536 by 8 bit CMOS PROMs. The CY7C286 is configured in the JEDEC standard 512K EPROM pinout. It is available in a 28-pin, 600 mil package. Power consumption on the CY7C286 will be 120 mA in the active mode and 40 mA in the standby mode. Access time is 60 ns. The CY7C287 has registered outputs and operates in the synchronous mode. It is available in a 28-pin, 300 mil package. The address setup time is 55 ns and the time from clock high to output valid is 20 ns. Both the CY7C286 and CY7C287 are available in a CERDIP package equipped with an erasure window to provide reprogrammability. When exposed to UV light, the PROM is erased and can be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C286 and CY7C287 offer the advantage of low power, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading the CY7C286 is accomplished by placing active LOW signals on the $\overline{OE}$ and $\overline{CE}$ pins. Reading the CY7C287 is accomplished by placing an active low signal on $\overline{E}/\overline{E}_S$. The contents of the memory location addressed by the address line (A_0–A_{15}) will become available on the output lines (O_0–O_7).

3

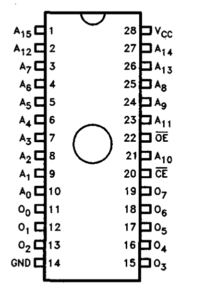
Logic Block Diagram



0151-1

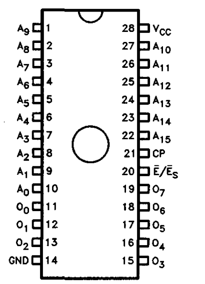
Pin Configurations

CY7C286



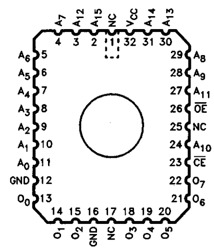
0151-6

CY7C287



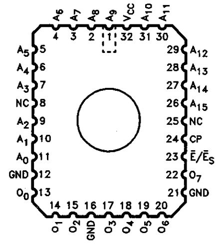
0151-2

LCC Pinout



0151-7

LCC Pinout



0151-4

Selection Guides

		7C286-60	7C286-70
Maximum Access Time (ns)		60	70
Maximum Operating Current (mA)	Commercial		90
	Military		120

		7C287-55	7C287-65
Maximum Set-up Time (ns)		55	65
Maximum Clock to Output (ns)		20	25
Maximum Operating Current (mA)	Commercial	160	150
	Military		200

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V (Pin 28 to Pin 14)

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 21, 22) 13.0V

UV Exposure .... 7258 Wsec/cm^2

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[4]

Parameters	Description	Test Conditions		7C286-60, 70 7C287-55, 65 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}[1]	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}[1]	Input LOW Voltage				0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		−20	−90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		120	mA
			Military		150	mA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		8	

Notes:
1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C286 and CY7C287 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. Tested initially and after any design or process changes that may affect these parameters.
4. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms[5, 6]

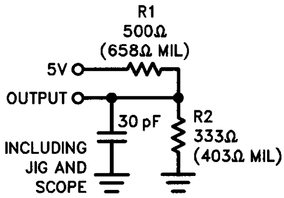
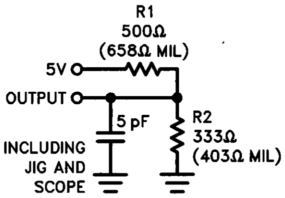
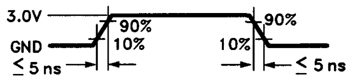


Figure 1a



0151-8

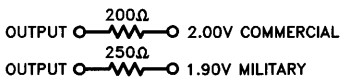
Figure 1b



0151-9

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0151-10

Notes:

5. R1 is a resistor connected from the output to V_{CC} and R2 is connected between the output and ground for testing purposes.
6. Note that R1 and R2 for 7C289 will be 961Ω and 510Ω for commercial and 1250Ω and 588Ω for military.

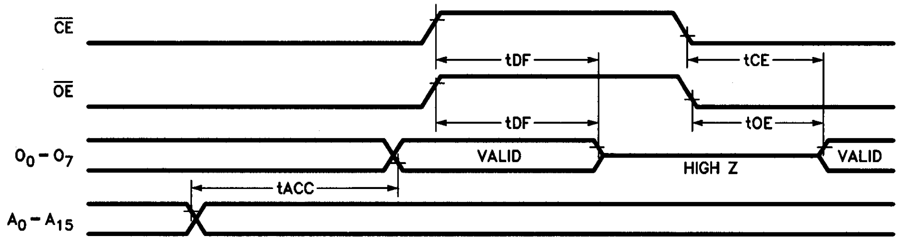
Switching Characteristics Over the Operating Range (7C286)

Parameters	Description		7C286-60 Min.	7C286-60 Max.	7C286-70 Min.	7C286-70 Max.	Units
t_{ACC}	Address Access Time			60		70	ns
t_{CE}	Output Valid from $\overline{CE}$	Commercial		60		70	ns
		Military				80	
t_{OE}	Output Valid from $\overline{OE}$			20		25	ns
t_{DF}	Output Tristate from $\overline{CE}/\overline{OE}$			20		25	ns
t_{PU}	Chip Enable to Power Up		0		0		ns
t_{PD}	Chip Disable to Power Down			50		60	ns

Switching Characteristics Over the Operating Range (7C287)

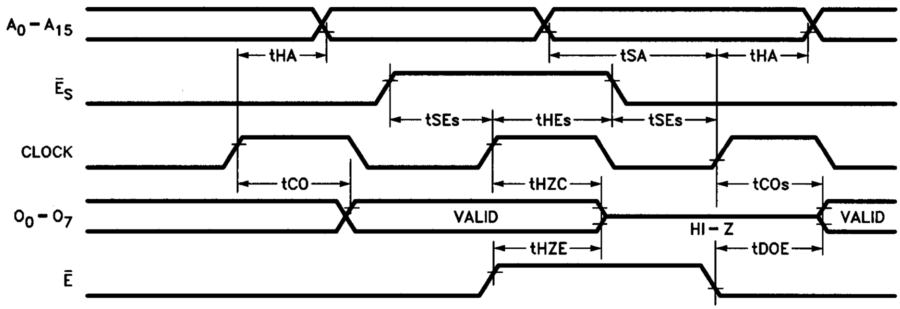
Parameters	Description	7C287-55 Min.	7C287-55 Max.	7C287-65 Min.	7C287-65 Max.	Units
t_{SA}	Address Set-Up to Clock HIGH	55		65		ns
t_{HA}	Address Hold from Clock HIGH	0		0		ns
t_{CO}	Clock HIGH to Output Valid		20		25	ns
t_{HZE}	Output Tristate from $\overline{E}$		20		25	ns
t_{DOE}	Output Valid from $\overline{E}$		20		25	ns
t_{PWC}	Clock Pulse Width	20		25		ns
t_{SES}	$\overline{E}_S$ Set-Up to Clock HIGH	15		18		ns
t_{HES}	$\overline{E}_S$ Hold from to Clock HIGH	8		10		ns
t_{HZC}	Output Tristate from CLK/$\overline{E}_S$		25		30	ns
t_{COS}	Output Valid from CLK/$\overline{E}_S$		25		30	ns

Switching Waveform (7C286)



0151-11

Switching Waveform (7C287)



0151-12

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
60	CY7C286-60PC	P21	Commercial
	CY7C286-60WC	W22	
70	CY7C286-70PC	P21	Commercial
	CY7C286-70WC	W22	
	CY7C286-70DMB	D22	Military
	CY7C286-70WMB	W22	
	CY7C286-70LMB	L55	
	CY7C286-70QMB	Q55	

Speed (ns)	Ordering Code	Package Type	Operating Range
55	CY7C287-55PC	P21	Commercial
	CY7C287-55WC	W22	
65	CY7C287-65PC	P21	Commercial
	CY7C287-65WC	W22	
	CY7C287-65DMB	D22	Military
	CY7C287-65WMB	W22	
	CY7C287-65LMB	L55	
	CY7C287-65QMB	Q55	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}	1,2,3

Switching Characteristics

Device	Parameters	Subgroups
7C287	t_{SA}	7,8,9,10,11
	t_{HA}	7,8,9,10,11
	t_{CO}	7,8,9,10,11
7C286	t_{AA}	7,8,9,10,11
	t_{CE}	7,8,9,10,11
	t_{DHA}	7,8,9,10,11

Document #: 38-00103-B

CYPRESS SEMICONDUCTOR

Reprogrammable 2048 x 8 PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 35 ns (commercial)**
  - **— 35 ns (military)**
- **Low power**
  - **— 330 mW (commercial)**
  - **— 413 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2000V static discharge**

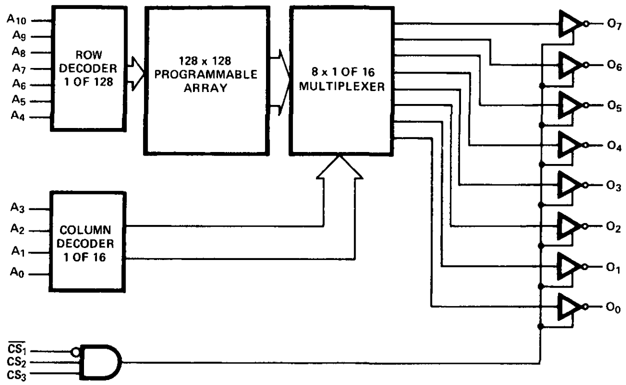
Product Characteristics

The CY7C291 and CY7C292 are high performance 2048 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil and 600 mil wide plastic and hermetic DIP packages respectively. The 300 mil ceramic DIP package is equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C291 and CY7C292 are plug-in replacements for bipolar devices and offer the advantages of lower power, reprogrammability, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

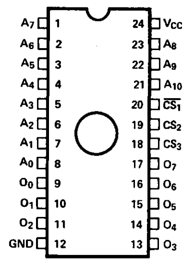
Reading is accomplished by placing an active LOW signal on $\overline{CS}_1$, and active HIGH signals on CS_2 and CS_3. The contents of the memory location addressed by the address lines (A_0–A_{10}) will become available on the output lines (O_0–O_7).

Logic Block Diagram

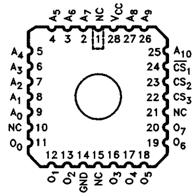


0008–1

Pin Configurations



0008–2



0008–3

Window available on 300 mil cerdip only

Selection Guide

			7C291-35 7C292-35	7C291-50 7C292-50
Maximum Access Time (ns)			35	50
Maximum Operating Current (mA)	STD	Commercial	90	90
		Military	120*	120
	L	Commercial	60	60

*7C291 only

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V (Pin 24 to Pin 12)

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Program Voltage (Pins 18, 20) 13.0V

UV Exposure .... 7258 Wsec/cm^2

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[6]	−55°C to + 125°C	5V ±10%

3

Electrical Characteristics Over the Operating Range[5]

Parameters	Description	Test Conditions		7C291L-35, 50 7C292L-35, 50 Min.	7C291L-35, 50 7C292L-35, 50 Max.	7C291-35, 50 7C292-35, 50 Min.	7C291-35, 50 7C292-35, 50 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4		0.4	V
V_{IH}[1]	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}[1]	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		Note 2		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−40	+40	−40	+40	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		60		90	mA
			Military*				120	mA

* −35: 7C291 only

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C291 and CY7C292 are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. See the last page of this specification for Group A subgroup testing information.
6. T_A is the "instant on" case temperature.

Switching Characteristics Over the Operating Range[5, 7]

Parameters	Description	7C291-35 7C292-35		7C291-50 7C292-50		Units
		Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		35		50	ns
t_{HZCS}	Chip Select Inactive to High Z[8]		25		25	ns
t_{ACS}	Chip Select Active to Output Valid		25		25	ns

AC Test Loads and Waveforms

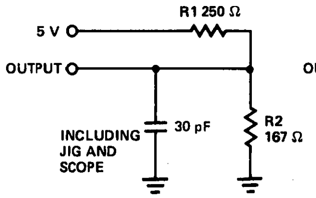
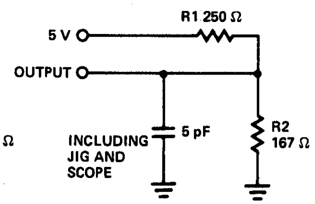
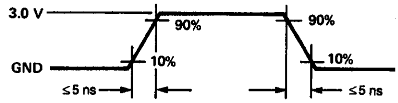


Figure 1a



0008-4

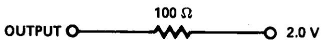
Figure 1b



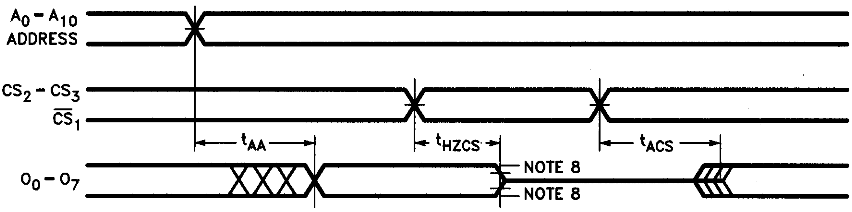
0008-6

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0008-5



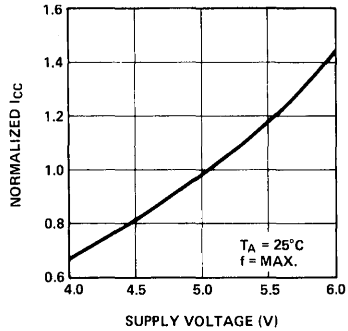
0008-7

Notes:

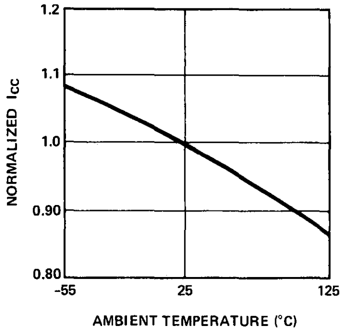
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figures 1a, 1b.*
8. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input.

Typical DC and AC Characteristics

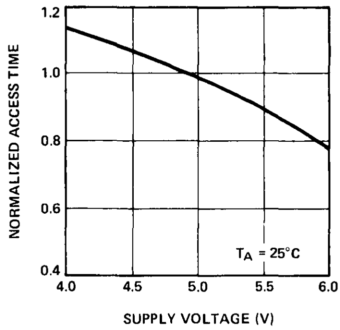
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

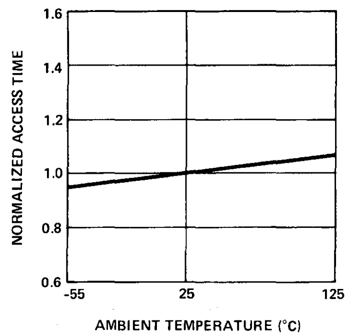


NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

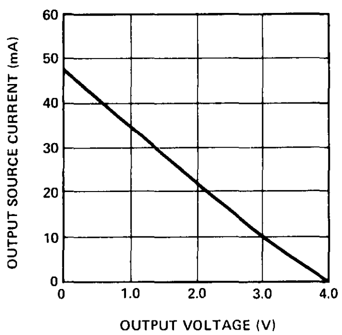


3

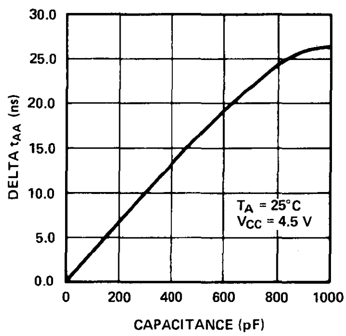
NORMALIZED ACCESS TIME vs. TEMPERATURE



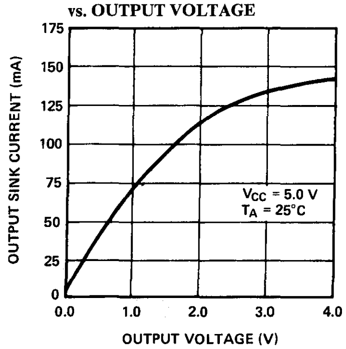
OUTPUT SOURCE CURRENT vs. VOLTAGE



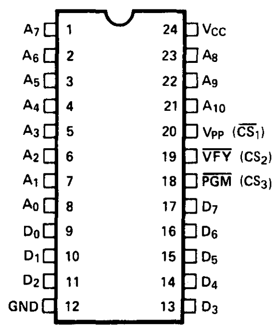
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



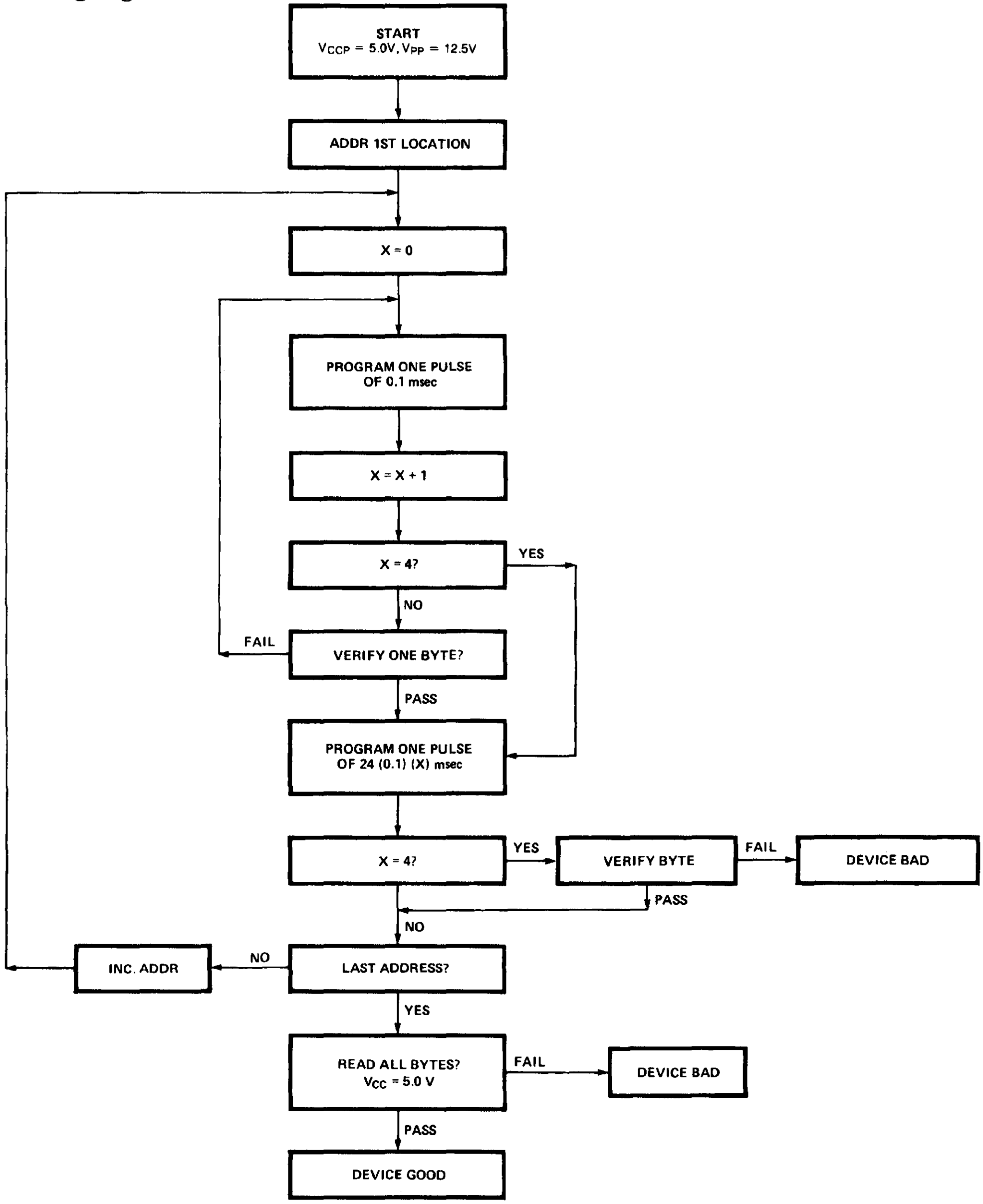
0008–8



0008–9

Figure 3. Programming Pinout

Programming Algorithm



0008–10

The CY7C291 and CY7C292 programming algorithm allows significantly faster programming than the "worst case" specification of 10 msec.

Typical programming time for a byte is less than 2.5 msec. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t_{PP}) is 0.1 msec which will then be followed by a longer overprogram pulse of 24 (0.1) (X) msec. X is an iteration counter and is equal to the NUMBER of the initial 0.1 msec pulses applied before verification occurs. Up to four 0.1 msec pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 5.0V.

Figure 4. Programming Flowchart

Programming Information

The 7C291 and 7C292 2K x 8 CMOS PROMs are implemented with a differential EPROM memory cell. The PROMs are delivered in an erased state, containing neither "1s" nor "0s". This erased condition of the array may be assessed using the "BLANK CHECK ONES" and "BLANK CHECK ZEROS" function, see below.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the 7C291. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 30-35 minutes.

The 7C291 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm^2 is the recommended maximum dosage.

Blank Check

A virgin device contains neither ones nor zeros because of the differential cell used for high speed. To verify that a PROM is unprogrammed, use the two blank check modes provided in Table 3. In each of these modes, the locations 0 thru 2047 should be addressed and read. A device is considered virgin if all locations are respectively "1s" and "0s" when addressed in the "BLANK ONES AND ZEROS" modes.

Because a virgin device contains neither ones nor zeros, it is necessary to program both ones and zeros. It is recommended that all locations be programmed to ensure that ambiguous states do not exist.

3

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage[1]	12.0	13.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input HIGH Voltage	3.0		V
V_{ILP}	Input LOW Voltage		0.4	V
V_{OH}	Output HIGH Voltage[2]	2.4		V
V_{OL}	Output LOW Voltage[2]		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width[3]	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F	V_{PP} Rise and Fall Time[3]	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify to High Z		1.0	μs

Notes:
1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function			Outputs (9–11, 13–17)
	Read or Output Disable	CS_3	CS_2	$\overline{CS_1}$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	
	Pin Number	(18)	(19)	(20)	
Read		V_{IH}	V_{IH}	V_{IL}	Data Out
Output Disable[4]		X	X	V_{IH}	High Z
Output Disable[4]		X	V_{IL}	X	High Z
Output Disable[4]		V_{IL}	X	X	High Z
Program		V_{ILP}	V_{IHP}	V_{PP}	Data In
Program Verify		V_{IHP}	V_{ILP}	V_{PP}	Data Out
Program Inhibit		V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		V_{ILP}	V_{IHP}	V_{PP}	Data In
Blank Check Ones		V_{PP}	V_{ILP}	V_{ILP}	Ones
Blank Check Zeros		V_{PP}	V_{IHP}	V_{ILP}	Zeros

Notes:
4. X = Don't care but not to exceed V_{CC} + 5%.
5. During programming and verification, all unspecified pins to be at V_{ILP}.

Programming Sequence 2K x 8

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Table 3. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 100 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 4 times. When the location verifies, one additional programming pulse should be applied of duration 24 x the sum of the previous programming pulses before advancing to the next address to repeat the process.

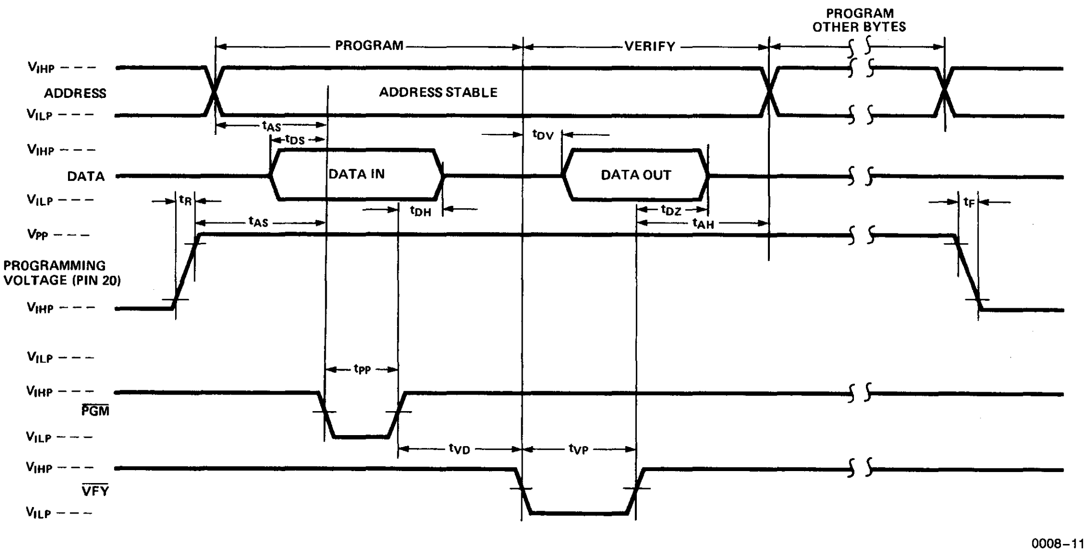


Figure 5. Programming Waveforms

Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
35	60	CY7C291L-35PC	P13	Commercial
		CY7C291L-35WC	W14	
	90	CY7C291-35PC	P13	
		CY7C291-35SC	S13	
		CY7C291-35WC	W14	
		CY7C291-35LC	L64	
	120	CY7C291-35WMB	W14	Military
		CY7C291-35DMB	D14	
50	60	CY7C291L-50PC	P13	Commercial
		CY7C291L-50WC	W14	
	90	CY7C291-50PC	P13	
		CY7C291-50SC	S13	
		CY7C291-50WC	W14	
		CY7C291-50LC	L64	
	120	CY7C291-50WMB	W14	Military
		CY7C291-50DMB	D14	
		CY7C291-50LMB	L64	
		CY7C291-50QMB	Q64	

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
35	60	CY7C292L-35PC	P11	Commercial
		CY7C292L-35DC	D12	
	90	CY7C292-35PC	P11	
		CY7C292-35DC	D12	
50	60	CY7C292L-50PC	P11	Commercial
		CY7C292L-50DC	D12	
	90	CY7C292-50PC	P11	
		CY7C292-50DC	D12	
	120	CY7C292-50DMB	D12	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7,8,9,10,11
t_{ACS}	7,8,9,10,11

Document #: 38-00007-C

CYPRESS SEMICONDUCTOR

Reprogrammable 2048 x 8 PROM

Features

- **Windowed for reprogrammability**
- **CMOS for optimum speed/power**
- **High speed**
  - **— 20 ns (commercial)**
  - **— 25 ns (military)**
- **Low power**
  - **— 600 mW (commercial)**
  - **— 660 mW (military)**
- **Low standby power**
  - **— 165 mW (commercial)**
  - **— 220 mW (military)**
- **EPROM technology 100% programmable**
- **Slim 300 mil or standard 600 mil packaging available**
- **5V ±10% V_{CC}, commercial and military**
- **TTL compatible I/O**
- **Direct replacement for bipolar PROMs**
- **Capable of withstanding >2001V static discharge**

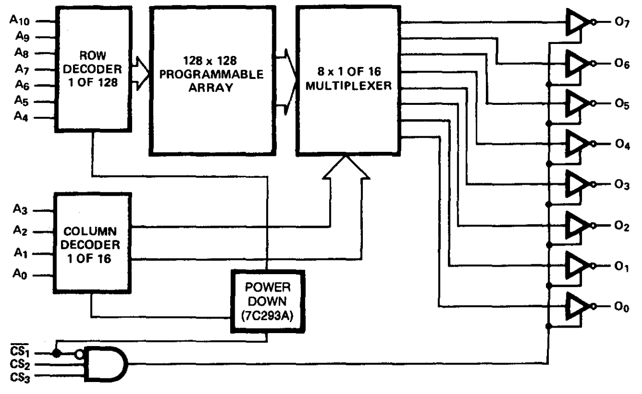
Product Characteristics

The CY7C291A, CY7C292A, and CY7C293A are high performance 2048 word by 8 bit CMOS PROMs. They are functionally identical, but are packaged in 300 mil (7C291A, 7C293A) and 600 mil wide plastic and hermetic DIP packages (7C292A). The CY7C293A has an automatic power down feature which reduces the power consumption by over 70% when deselected. The 300 mil ceramic DIP package is equipped with an erasure window; when exposed to UV light the PROM is erased and can then be reprogrammed. The memory cells utilize proven EPROM floating gate technology and byte-wide intelligent programming algorithms.

The CY7C291A, CY7C292A, and CY7C293A are plug-in replacements for bipolar devices and offer the advantages of lower power, reprogrammability, superior performance and programming yield. The EPROM cell requires only 12.5V for the supervoltage and low current requirements allow for gang programming. The EPROM cells allow for each memory location to be tested 100%, as each location is written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that after customer programming the product will meet DC and AC specification limits.

Reading is accomplished by placing an active LOW signal on $\overline{CS_1}$, and active HIGH signals on CS_2 and CS_3. The contents of the memory location addressed by the address lines (A_0–A_{10}) will become available on the output lines (O_0–O_7).

Logic Block Diagram



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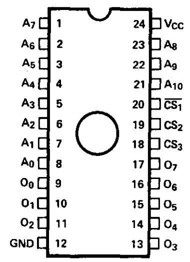
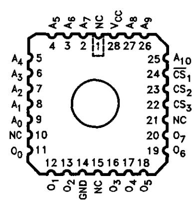
Pin Configurations



0120-2



0120-3

Window available on 7C291A and 7C293A only.

Selection Guide

			7C291A-20 7C292A-20 7C293A-20	7C291A-25 7C292A-25 7C293A-25	7C291A-30 7C292A-30 7C293A-30	7C291A-35 7C292A-35 7C293A-35	7C291A-50 7C292A-50 7C293A-50
Maximum Access Time (ns)			20	25	30	35	50
Maximum Operating Current (mA)	STD	Commercial	120	90		90	90
		Military		120	120	90	90
	L	Commercial				60	60
Standby Current (mA) 7C293A Only		Commercial	40	30		30	30
		Military		40	40	40	40

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . −65°C to +150°C

Ambient Temperature with Power Applied . . . . −55°C to +125°C

Supply Voltage to Ground Potential . . . . −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State. . . . . −0.5V to +7.0V

DC Input Voltage . . . . −3.0V to +7.0V

DC Program Voltage 13.0V

UV Exposure . . . . 7258 Wsec/cm^2

Static Discharge Voltage . . . . >2001V (per MIL-STD-883, Method 3015)

Latchup Current . . . . >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[5]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range[6]

Parameters	Description	Test Conditions		7C291A-20 7C292A-20 7C293A-20		7C291A-25 7C292A-25 7C293A-25		7C291A-30 7C292A-30 7C293A-30		7C291AL-35, 50 7C292AL-35, 50 7C293AL-35, 50		7C291A-35, 50 7C292A-35, 50 7C293A-35, 50		Units
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = −16.0 mA			0.4		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8		0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	μA
V_{CD}	Input Diode Clamp Voltage			Note 2		Note 2		Note 2		Note 2		Note 2		
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		−20	−90	−20	−90	−20	−90	−20	−90	−20	−90	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		120		120				60		90	mA
			Military				120		90				90	mA
I_{SB}	Standby Supply Current (7C293A Only)	V_{CC} = Max., $\overline{CS_1}$ ≥ V_{IH}	Commercial		40		40				30		30	mA
			Military				40		40				40	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		8	

Notes:

1. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. The CMOS process does not provide a clamp diode. However, the CY7C291A, CY7C292A and CY7C293A are insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. T_A is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.

Switching Characteristics Over the Operating Range[6, 7]

Parameters	Description	7C291A-20 7C292A-20 7C293A-20		7C291A-25 7C292A-25 7C293A-25		7C291A-30 7C292A-30 7C293A-30		7C291A-35 7C292A-35 7C293A-35		7C291A-50 7C292A-50 7C293A-50		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		20		25		30		35		50	ns
t_{HZCS_1}	Chip Select Inactive to High Z[8]		15		20		20		25		25	ns
t_{ACS_1}	Chip Select Active to Output Valid		15		20		20		25		25	ns
t_{HZCS_2}	Chip Select Inactive to High Z[9] (7C293A $\overline{CS}_1$ Only)		22		27		32		35		45	ns
t_{ACS_2}	Chip Select Active to Output Valid (7C293A $\overline{CS}_1$ Only)[9]		22		27		32		35		45	ns
t_{PU}	Chip Select Active to Power Up (7C293A $\overline{CS}_1$ Only)	0		0		0		0		0		ns
t_{PD}	Chip Select Inactive to Power Down (7C293A $\overline{CS}_1$ Only)		22		27		32		35		45	ns

AC Test Loads and Waveforms

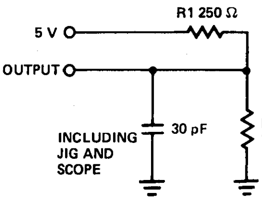
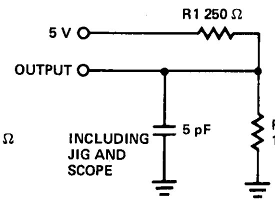
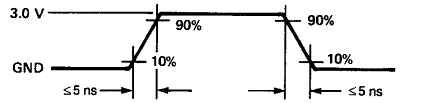


Figure 1a



0120-4

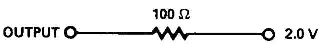
Figure 1b



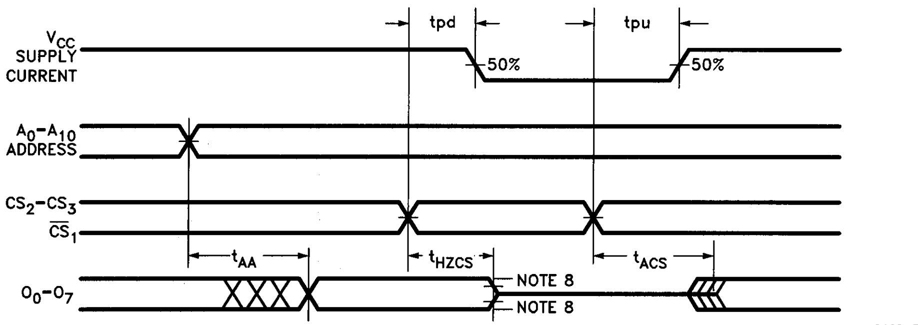
0120-5

Figure 2. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0120-6



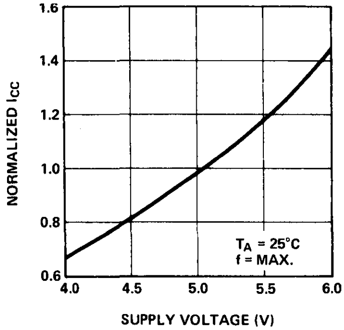
0120-7

Notes:

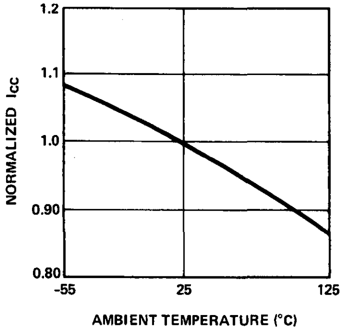
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, output loading of the specified I_{OL}/I_{OH} and loads shown in *Figures 1a, 1b.*
8. t_{HZCS} is tested with load shown in *Figure 1b.* Transition is measured at steady state High level −500 mV or steady state Low level +500 mV on the output from the 1.5V level on the input.
9. t_{HZCS_2} and t_{ACS_2} refer to 7C293A $\overline{CS}_1$ only.

Typical DC and AC Characteristics

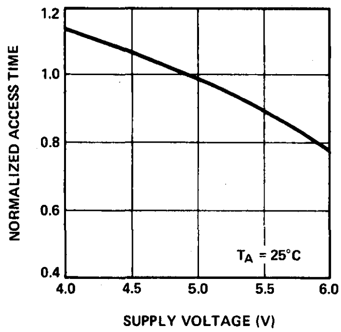
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



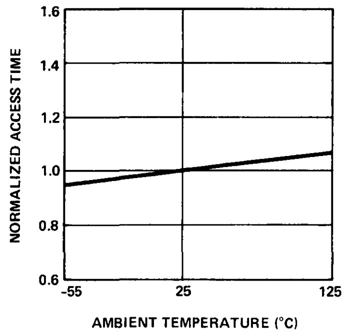
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



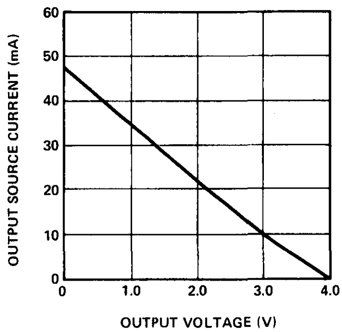
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



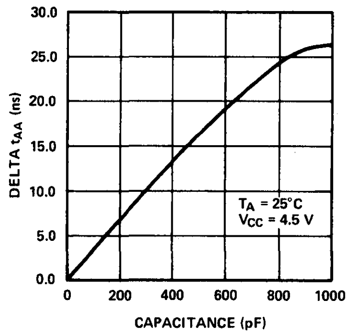
NORMALIZED ACCESS TIME vs. TEMPERATURE



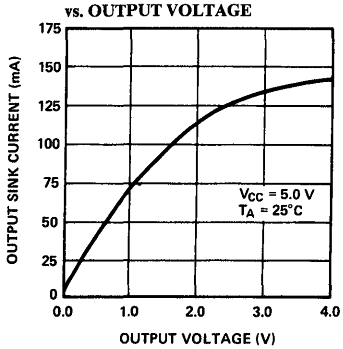
OUTPUT SOURCE CURRENT vs. VOLTAGE



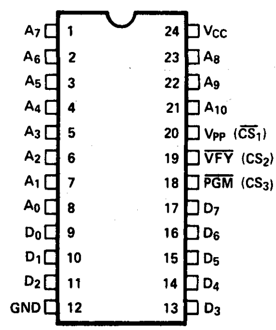
TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



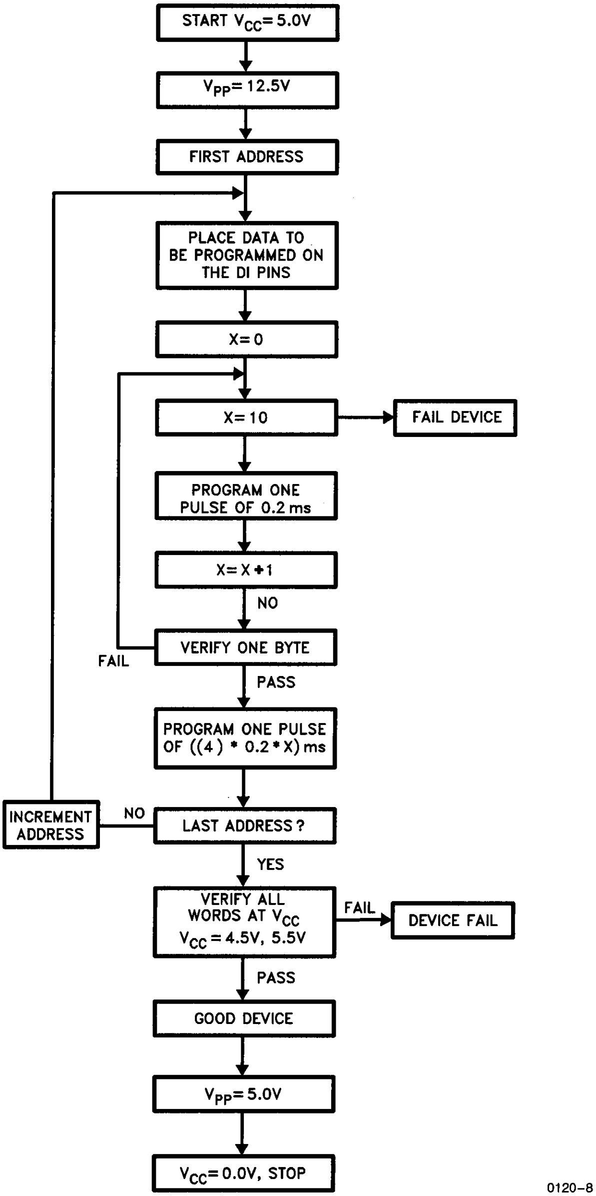
0120-9



0120-10

Figure 3. Programming Pinout

Programming Algorithm



The CY7C291A, CY7C292A and CY7C293A programming algorithm allows significantly faster programming than the “worst case” specification of 10 ms.

Typical programming time for a byte is 1.0 ms. The use of EPROM cells allows factory testing of programmed cells, measurement of data retention and erasure to ensure reliable data retention and functional performance. A flowchart of the algorithm is shown in *Figure 4.*

The algorithm utilizes two different pulse types: initial and overprogram. The duration of the PGM pulse (t_{PP}) is 0.2 ms which will then be followed by a longer overprogram pulse of 4 (0.2) (X) ms. X is an iteration counter and is equal to the NUMBER of the initial 0.2 ms pulses applied before verification occurs. Up to 10 (0.2) ms pulses are provided before the overprogram pulse is applied.

The entire sequence of program pulses and byte verification is performed at V_{CCP} = 5.0V. When all bytes have been programmed all bytes should be compared (Read mode) to original data with V_{CC} = 4.5V and 5.5V.

Figure 4. Programming Flowchart

Programming Information

The 7C291A, 7C292A and 7C293A 2K x 8 CMOS PROMs are implemented with a single ended EPROM memory cell. The PROMs are delivered in an erased state, containing "0s". To verify that a PROM is unprogrammed, use the verify mode provided in Table 3. The locations 0 thru 2047 should be addressed and read.

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase these PROMs. For this reason, an opaque label should be placed over the window if the PROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating the exposure time would be approximately 30-35 minutes.

These PROMs need to be within 1 inch of the lamp during erasure. Permanent damage may result if the PROM is exposed to high intensity UV light for an extended period of time. 7258W × sec/cm^2 is the recommended maximum dosage.

DC Programming Parameters $T_A = 25°C$

Table 1

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage[1]	12.0	13.0	V
V_{CCP}	Supply Voltage	4.75	5.25	V
V_{IHP}	Input HIGH Voltage	3.0		V
V_{ILP}	Input LOW Voltage		0.4	V
V_{OH}	Output HIGH Voltage[2]	2.4		V
V_{OL}	Output LOW Voltage[2]		0.4	V
I_{PP}	Programming Supply Current		50	mA

AC Programming Parameters $T_A = 25°C$

Table 2

Parameter	Description	Min.	Max.	Units
t_{PP}	Programming Pulse Width[3]	100	10,000	μs
t_{AS}	Address Setup Time	1.0		μs
t_{DS}	Data Setup Time	1.0		μs
t_{AH}	Address Hold Time	1.0		μs
t_{DH}	Data Hold Time	1.0		μs
t_R, t_F	V_{PP} Rise and Fall Time[3]	1.0		μs
t_{VD}	Delay to Verify	1.0		μs
t_{VP}	Verify Pulse Width	2.0		μs
t_{DV}	Verify Data Valid		1.0	μs
t_{DZ}	Verify to High Z		1.0	μs

Notes:
1. V_{CCP} must be applied prior to V_{PP}.
2. During verify operation.
3. Measured 10% and 90% points.

Mode Selection

Table 3

Mode		Pin Function			Outputs (9–11, 13–17)
	Read or Output Disable	CS_3	CS_2	$\overline{CS_1}$	
	Other	$\overline{PGM}$	$\overline{VFY}$	V_{PP}	
	Pin Number	(18)	(19)	(20)	
Read		V_{IH}	V_{IH}	V_{IL}	Data Out
Output Disable[4]		X	X	V_{IH}	High Z
Output Disable[4]		X	V_{IL}	X	High Z
Output Disable[4]		V_{IL}	X	X	High Z
Program		V_{ILP}	V_{IHP}	V_{PP}	Data In
Program Verify		V_{IHP}	V_{ILP}	V_{PP}	Data Out
Program Inhibit		V_{IHP}	V_{IHP}	V_{PP}	High Z
Intelligent Program		V_{ILP}	V_{IHP}	V_{PP}	Data In

Notes:
4. X = Don't care but not to exceed V_{CC} + 5%.
5. During programming and verification, all unspecified pins to be at V_{ILP}.

3

Programming Sequence 2K x 8

Power the device for normal read mode operation with pin 18, 19 and 20 at V_{IH}. Per *Figure 5* take pin 20 to V_{PP}. The device is now in the program inhibit mode of operation with the output lines in a high impedance state; see Table 3. Again per *Figure 5* address, program, and verify one byte of data. Repeat this for each location to be programmed.

If the brute force programming method is used, the pulse width of the program pulse should be 10 ms, and each location is programmed with a single pulse. Any location that fails to verify causes the device to be rejected.

If the intelligent programming technique is used, the program pulse width should be 200 μs. Each location is ultimately programmed and verified until it verifies correctly up to and including 10 times. When the location verifies, one additional programming pulse should be applied of duration 4 x the sum of the previous programming pulses before advancing to the next address to repeat the process.

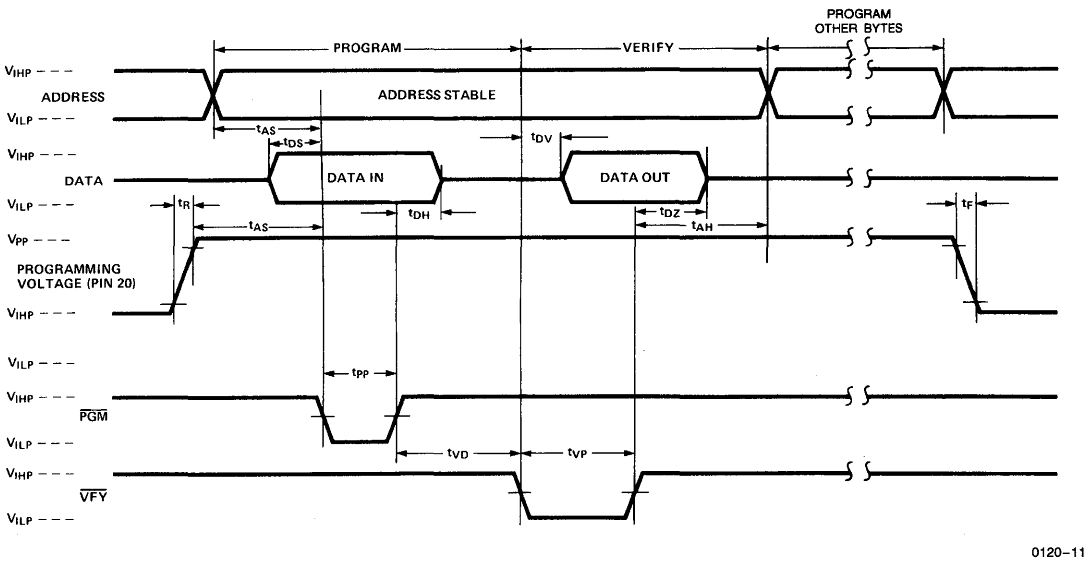


Figure 5. Programming Waveforms

Ordering Information

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
20	120	CY7C291A-20PC	P13	Commercial
		CY7C291A-20WC	W14	
		CY7C292A-20PC	P11	
		CY7C292A-20DC	D12	
		CY7C293A-20PC	P13	
		CY7C293A-20WC	W14	
25	120	CY7C291A-25PC	P13	Commercial
		CY7C291A-25WC	W14	
		CY7C292A-25PC	P11	
		CY7C292A-25DC	D12	
		CY7C293A-25PC	P13	
		CY7C293A-25WC	W14	
		CY7C291A-25DMB	D14	Military
		CY7C291A-25WMB	W14	
		CY7C291A-25LMB	L64	
		CY7C291A-25QMB	Q64	
		CY7C292A-25DMB	D12	
		CY7C293A-25DMB	D14	
		CY7C293A-25WMB	W14	
		CY7C293A-25LMB	L64	
		CY7C293A-25QMB	Q64	
30	120	CY7C291A-30DMB	D14	Military
		CY7C291A-30WMB	W14	
		CY7C291A-30LMB	L64	
		CY7C291A-30QMB	Q64	
		CY7C292A-30DMB	D12	
		CY7C293A-30DMB	D14	
		CY7C293A-30WMB	W14	
		CY7C293A-30LMB	L64	
		CY7C293A-30QMB	Q64	
35	60	CY7C291AL-35PC	P13	Commercial
		CY7C291AL-35WC	W14	
		CY7C292AL-35PC	P11	
		CY7C293AL-35PC	P13	
		CY7C293AL-35WC	W14	
	90	CY7C291A-35PC	P13	Commercial
		CY7C291A-35DC	D14	
		CY7C291A-35WC	W14	
		CY7C291A-35LC	L64	

Speed (ns)	I_{CC} (mA)	Ordering Code	Package Type	Operating Range
35	90	CY7C292A-35PC	P11	Commercial
		CY7C292A-35DC	D12	
		CY7C293A-35PC	P13	
		CY7C293A-35DC	D14	
		CY7C293A-35WC	W14	
		CY7C293A-35LC	L64	
	120	CY7C291A-35DMB	D14	Military
		CY7C291A-35WMB	W14	
		CY7C291A-35LMB	L64	
		CY7C291A-35QMB	Q64	
		CY7C292A-35DMB	D12	
		CY7C293A-35DMB	D14	
		CY7C293A-35WMB	W14	
		CY7C293A-35LMB	L64	
		CY7C293A-35QMB	Q64	
50	60	CY7C291AL-50PC	P13	Commercial
		CY7C291AL-50WC	W14	
		CY7C292AL-50PC	P11	
		CY7C293AL-50PC	P13	
		CY7C293AL-50WC	W14	
	90	CY7C291A-50PC	P13	Commercial
		CY7C291A-50DC	D14	
		CY7C291A-50WC	W14	
		CY7C291A-50LC	L64	
		CY7C292A-50PC	P11	
		CY7C292A-50DC	D12	
		CY7C293A-50PC	P13	
		CY7C293A-50DC	D14	
		CY7C293A-50WC	W14	
		CY7C293A-50LC	L64	
	120	CY7C291A-50DMB	D14	Military
		CY7C291A-50WMB	W14	
		CY7C291A-50LMB	L64	
		CY7C291A-50QMB	Q64	
		CY7C292A-50DMB	D12	
		CY7C293A-50DMB	D14	
		CY7C293A-50WMB	W14	
		CY7C293A-50LMB	L64	
		CY7C293A-50QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3
I_{SB}[2]	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{AA}	7,8,9,10,11
t_{ACS1}[1]	7,8,9,10,11
t_{ACS2}[2]	7,8,9,10,11

Notes:
1. 7C291A and 7C292A only.
2. 7C293A only.

Document #: 38-00075-C

Introduction

PROMs or Programmable Read Only Memories have existed since the early 1970's and continue to provide the highest speed non-volatile form of semiconductor memory available. Until the introduction of CMOS PROMs from Cypress, all PROMs were produced in bipolar technology, because bipolar technology provided the highest possible performance at an acceptable cost level. All bipolar PROMs use a fuse for the programming element. The fuses are in tact when the product is delivered to the user, and may be programmed or written once with a pattern and used or read infinitely. The fuses are literally blown using a high current supplied by a Programming System. Since the fuses may only be blown or programmed once, they may not be programmed during test. In addition, since they may not be programmed until the user determines the pattern, they may not be completely tested prior to shipment from the supplier. This inability to completely test, results in less than 100% yield during programming and use by the customer for two reasons. First, some percentage of the product fails to program. These devices fall out during the programming operation, and although a nuisance are easily identified. Additional yield is lost because the device fails to perform even though it programs correctly. This failure is normally due to the device being too slow. This is a more subtle failure, and can only be found by 100% post program AC testing, or even worse by trouble shooting an assembled board or system.

Cypress CMOS PROMs use an EPROM programming mechanism. This technology has been in use in MOS technologies since the early 1970s. However, as with most MOS technologies the emphasis has been on density, not performance. CMOS at Cypress is as fast as or faster than Bipolar and coupled with EPROM, becomes a viable alternative to bipolar PROMs from a performance point-of-view. In the arena of programming, EPROM has some significant advantages over fuse technology. EPROM cells are programmed by injecting charge on an isolated gate which permanently turns off the transistor. This mechanism can be reversed by irradiating the device with ultraviolet light. The fact that programming can be erased, totally changes the testing and programming situation and philosophy. All cells can be programmed during the manufacturing process and then erased prior to packaging and subsequent shipment. While these cells are programmed, the performance of each cell in the memory can be tested allowing the shipment of devices that program every time, and will perform as specified when programmed. In addition when these devices are supplied in a windowed package they can be programmed and erased indefinitely providing the designer a RE-PROGRAMMABLE PROM for development.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation and when charged with electrons, the transistor is permanently turned off. When uncharged (the transistor is unprogrammed) the device may be turned on and off normally with the control gate. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device repeatedly if necessary to assure programming function and performance.

Two Transistor Cells

In order to provide an EPROM cell that is as fast as the fuse technology employed in bipolar processes, Cypress uses a two transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor, biasing it off.

Differential Memory Cells

In the 4K (CY7C225); 8K (CY7C235, CY7C281, CY7C282); and 16K (CY7C245, CY7C291, CY7C292) CMOS PROMs, Cypress employs a differential memory cell and sense amplifier technique. Higher density devices such as the 7C261, 7C263, 7C264 or 7C269 64K PROMs employ a single ended Cell and sense amplifier technique similar to the approach used in more conventional EPROMs.

In a conventional high density EPROM a single EPROM transistor is used to switch the input to one side of a differential sense amplifier. The other side of the sense amplifier is biased at an intermediate level with a dummy cell. An unprogrammed EPROM transistor will conduct and drive the sense amplifier to a logic "0". A programmed EPROM transistor will not conduct, and consequently drives the sense amplifier to a logic "1". A conventional EPROM cell therefore is delivered with a specific state "0" or "1" in it depending on the number of inversions after the sense amplifier and can always be programmed to the opposite state. Access time in this conventional approach is heavily dependent on the time the selected EPROM transistor takes to move the input of the sense amplifier from a quiescent condition to the threshold that the dummy cell is biasing the second input to the sense amplifier. This bias is several volts, and requires a significant delay before the sense amplifier begins to react.

Cypress PROMs employ a true differential cell approach, with EPROM cells attached to both inputs of the sense amplifier. As indicated above, the read transistor which is optimized for speed is actually the transistor attached to the sense amplifier. In the erased state, both EPROM transistors conduct when selected eccentrically biasing the input of the sense amplifier at the same level. If the inputs were at identical levels, the output of the sense amplifier would be in a mestastable condition or, neither a "1" nor "0". In actual practice the natural bias and high gain of the sense amplifier combine to cause the output to favor one or the other stable conditions. The difference between the two conditions is however only a few millivolts and the memory cell should be considered to contain neither a "1" nor a "0". As a result of this design approach, the memory cell must be programmed to either a "1" or a "0" depending on the desired condition and the conventional BLANK

CHECK mechanism is invalid. The benefit of the approach however is that only a small differential signal from the cell begins the sense amplifier switching and the access time of the memory is extremely fast.

Single Ended Memory Cells

Although a more conventional approach, single ended memory cells and sensing techniques offer a superior trade-off between die size and performance than the differential cell for devices of 64K densities and above. The Single ended technique employed by Cypress uses a dummy cell for the reference voltage thus providing a reference that tracks the programmed cell in process related parameters, power supply and temperature induced variations. The Memory cell used is a second generation two transistor cell derived from earlier work at the 16K density level. It has an optimized READ transistor that is matched to the sense amplifier, and a second transistor optimized for programming. The floating gates of the two transistors that make up a memory cell are connected electrically so that the charge programmed onto one device controls the threshold of the second transistor.

Unlike the differential memory approach, the erased single ended device contains all "0"s and on the the ones are programmed. Therefore a "1" on the data pins during programming causes a "1" to be programmed into the addressed location.

Programming Algorithm

Byte Addressing and Programming

All Cypress CMOS PROMs are addressed and programmed on a byte basis unlike the bipolar products that they replace. The address lines used to access the memory in a read mode are the same for programming, and the address map is identical. The information to be programmed into each byte is presented on the data out pins during the programming operation and the data is read from these same pins for verification that the byte has been programmed.

Blank Check for Differential Cells

Since a differential cell contains neither a "1" nor a "0" before it is programmed, the conventional BLANK CHECK is not valid. For this reason, all Cypress CMOS PROMs contain a special BLANK CHECK mode of operation. Blank check is performed by separately examining the "0" and "1" sides of the differential memory cell to determine whether either side has been independently programmed. This is accomplished in two passes one comparing the "0" side of the differential cell against a reference voltage applied to the opposite side of the sense amplifier and then repeating this operation for the "1"s side of the cell. The modes are called BLANK CHECK ONES, and BLANK CHECK ZEROS. These modes are entered by the application of a supervoltage to the device.

Blank Check for Single Ended Cells

Single ended cells BLANK CHECK in a conventional manner. An erased device contains all "0"s and a programmed call will contain a "1". Cypress PROMs that use the single ended approach provide a specific mode to perform the BLANK CHECK which also provides the verify function. This makes the need to switch high voltages unnecessary during the program verify operation. See specific data sheets for details.

Programming the Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a READ and a WRITE pin in the programming mode. These are active low signals and cause the data on the output pins to be written into the addressed memory location in the case of the WRITE signal or read out of the device in the case of the READ signal. When both the READ and WRITE signals are high, the outputs are disabled and in a high impedance state. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location with the WRITE signal. Verification of data is accomplished by reading the information on the output pins while the READ signal is active.

The timing for actual programming is supplied in the unique programming specification for each device.

Special Features

Depending on the specific CMOS PROM in question, additional features that require programming may be available to the designer. Two of these features are a Programmable INITIAL BYTE and Programmable SYNCHRONOUS/ASYNCHRONOUS ENABLE available in some of the registered devices. Like programming the array, these features make use of EPROM cells and are programmed in a similar manner, using supervoltages. The specific timing and programming requirements are specified in the data sheet of the device employing the feature.

Programming Support

Programming support for Cypress CMOS PROMs is available from a number of programmer manufacturers, some of which are listed below.

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA
98073-9746
(206) 881-6444

Data I/O 29B Unipak II				
Cypress Part Number	Generic Part Number	Family Code and Pinout		Revision
CY7C225	27S25	F0	B6	V12
CY7C235	27S35	F0	B5	V09
CY7C245	27S45A	F0	B0	V09
CY7C261/3/4	27S49	EF	31	V11
CY7C281/2	27S281/181	EE	B4	V09
CY7C291/2	27S291/191	F2	AF	V09

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118

Stag PPZ Zm2000			
Cypress Part Number	**Generic Part Number**	**Family Code and Pinout**	**Revision**
CY7C225	27S25	Menu Driven	Rev 21
CY7C235	27S35		Rev 21
CY7C245	27S45A		Rev 24
CY7C281/2	27S281/181		Rev 21
CY7C291/2	27S291/191		Rev 21

Cypress Semiconductor, Inc.
3901 North First St.
San Jose, CA 95134
(408) 943-2600

Cypress CY3000 QuickPro Rev. PROM 2.10		
Cypress Part Number	**Generic Part Number**	**Family Code and Pinout**
CY7C225	Menu Driven	Menu Driven
CY7C235		
CY7C245		
CY7C261/3/4		
CY7C268		
CY7C269		
CY7C281/2		
CY7C291/2		

Section Contents

EPLDs (Erasable Programmable Logic Devices)

Page Number

Introduction to CMOS EPLDs

Cypress EPLD Family Features

Cypress Semiconductor's EPLD family offers the user the next generation in Erasable Programmable Logic Devices (EPLD) based on our high performance 0.8μ CMOS process. These devices offer the user the power saving of a CMOS-based process, with delay times equivalent to those previously found only in bipolar devices. No fuses are used in Cypress' EPLD family, rather all devices are based on an EPROM cell to facilitate programming. By using an EPROM cell instead of fuses, programming yields of 100% can be expected since all devices are functionally tested and erased prior to packaging. Therefore, no programming yield loss can be expected by the user.

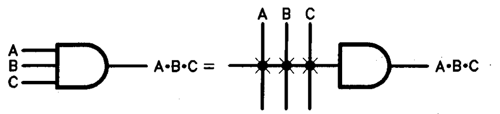
The EPROM cell used by Cypress serves the same purpose as the fuse used in most bipolar PLD devices. Before programming, the AND gates or Product Terms are connected via the EPROM cells to both the true and complement inputs. When the EPROM cell is programmed, the inputs from a gate or Product Term are disconnected. Programming alters the transistor threshold of each cell so that no conduction can occur, which is equivalent to disconnecting the input from the gate or Product Terms. This is similar to "blowing" the fuses of a bipolar device which disconnects the input gate from the Product Term. Selective programming of each of these EPROM cells enables the specific logic function to be implemented by the user.

The programmability of Cypress' EPLDs allows the users to customize every device in a number of ways to implement their unique logic requirements. Using EPLDs in place of SSI or MSI components results in more effective utilization of boardspace, reduced cost and increased reliability. The flexibility afforded by these EPLDs allows the designer to quickly and effectively implement a number of logic functions ranging from random logic gate replacement to complex combinatorial logic functions.

The EPLD family implements the familiar "sum of products" logic by using a programmable AND array whose output terms feed a fixed OR array. The sum of these can be expressed in a Boolean transfer function and is limited only by the number of product terms available in the AND-OR array. A variety of different sizes and architectures are available. This allows for more efficient logic optimization by matching input, output and product terms to the desired application.

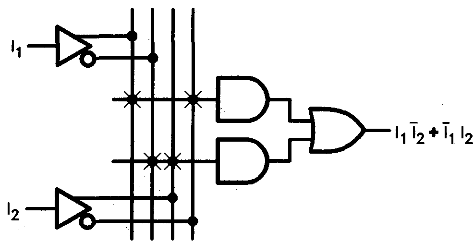
EPLD Notation

To reduce confusion and to have an orderly way of representing the complex logic networks, logic diagrams are provided for the various part types. In order to be useful, Cypress logic diagrams employ a common logic convention that is easy to use. *Figure 1* shows the adopted convention. In *Figure 1*, an "x" represents an unprogrammed EPROM cell that is used to perform the logical AND operation upon the input terms. The convention adopted does not imply that the input terms are connected on the common line that is indicated. A further extension of this convention is shown in *Figure 2* which shows the implementation of a simple transfer function. The normal logic representation of the transfer function logic convention is shown in *Figure 3*.



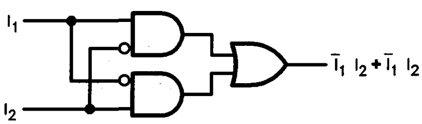
0024-1

Figure 1



0024-2

Figure 2



0024-3

Figure 3

PLD Circuit Configurations

Cypress EPLDs have several different output configurations that cover a wide spectrum of applications. The available output configurations offer the user the benefits of both lower package counts and reduced costs when used. This approach allows the designer to select a PLD that best fits the needs of his application. An example of some of the configurations that are available are listed below.

Programmable I/O

Figure 4 illustrates the programmable I/O offered in the Cypress EPLD family which allows product terms to directly control the outputs of the device. One product term is used to directly control the three-state output buffer, which then gates the summation of the remaining terms to the output pin. The output of this summation can be fed back into the PLD as an input to the array. This programmable I/O feature allows the PLD to drive the output pin when the three-state output is enabled or, the I/O pin can be used as an input to the array when the three-state output is disabled.

Registered Outputs with Feedback

Figure 5 illustrates the registered outputs offered on a number of the Cypress EPLDs which allow any of these circuits to function as a state sequencer. The summation of the product terms is stored in the D-type output flip-flop on the rising edge of the system clock. The Q output of the flip-flop can then be gated to the output pin by enabling the three-state output buffer. The output of the flip-flop can also be fed back into the array as an input term. The output feedback feature allows the PLD to remember and then alter its function based upon that state. This circuit can be used to execute such functions as counting, skip, shift and branch.

Programmable Macro Cell

The Programmable Macro Cell, illustrated in Figure 10, provides the capability of defining the architecture of each output individually. Each of the potential outputs may be specified to be "REGISTERED" or "COMBINATORIAL". Polarity of each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "ARRAY" configurable "OUTPUT ENABLE" for each potential output. This feature allows the outputs to be reconfigured as inputs on an individual basis or alternately used as a bidirectional I/O controlled by the programmable array.

Buried Register Feedback

The CY7C330 and CY7C331 EPLDs provide registers which may be "buried" or "hidden" by electing feedback of the register output. These buried registers, which are useful in state machines, may be implemented without sacrificing the use of the associated device pin as an input. In previous PLDs, when the feedback path was activated, the input pin-path to the logic array was blocked. The proprietary CY7C330 reprogrammable synchronous state machine macrocell illustrates, in Figure 7, the shared input multiplexer, which provides an alternative input path for the I/O pin associated with a buried macrocell register. Each pair of macrocells shares an input multiplexer and as long as alternate macrocells are buried, up to six of the twelve output registers can be buried without the loss of any I/O pins as inputs. The CY7C330 also contains four dedicated hidden macrocells with no external output, illustrated in Figure 8, that are used as additional state registers for creating high-performance state machines.

Asynchronous Register Control

Cypress also offers EPLDs which may be used in asynchronous systems in which register clock, set and reset are controlled by the outputs of the product term array. The clock signal is created by the processing of external inputs and/or internal feedback by the logic of the product term array which is then routed to the register clock. The register set and reset are similarly controlled by product term outputs and can be triggered at any time independent of the register clock in response to external and/or feedback inputs processed by the logic array. The proprietary CY7C331 Asynchronous Registered EPLD, for which the I/O macrocell is illustrated in Figure 9, is an example of such a device. The register clock, set and reset functions of the CY7C331 are all controlled by product terms and enable their respective functions dependent only on input signal timing and combinatorial delay through the device logic array.

Input Register Cell

Other Cypress EPLDs provide input register cells which allow capture for processing of short duration inputs which would not otherwise be present at the inputs for sufficient time to allow the device to respond. Both the proprietary CY7C330 Reprogrammable Synchronous State Machine and the proprietary CY7C332 Combinatorial EPLD provide these input register cells which are shown in Figure 11. The clock for the input register may be provided from one of two external clock input pins selectable by a configuration bit, C4, dedicated for this purpose for each input register. This choice of input register clock allows signals to be captured and processed from two independent system sources each controlled by its own independent clock. These input register cells are provided within I/O macrocells, as well as, for dedicated input pins.

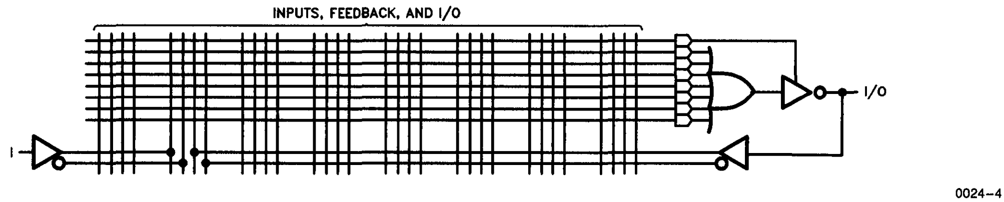


Figure 4. Programmable I/O

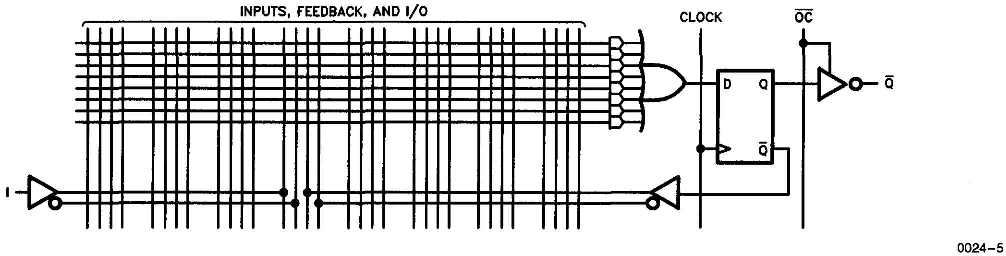


Figure 5. Registered Outputs with Feedback

4

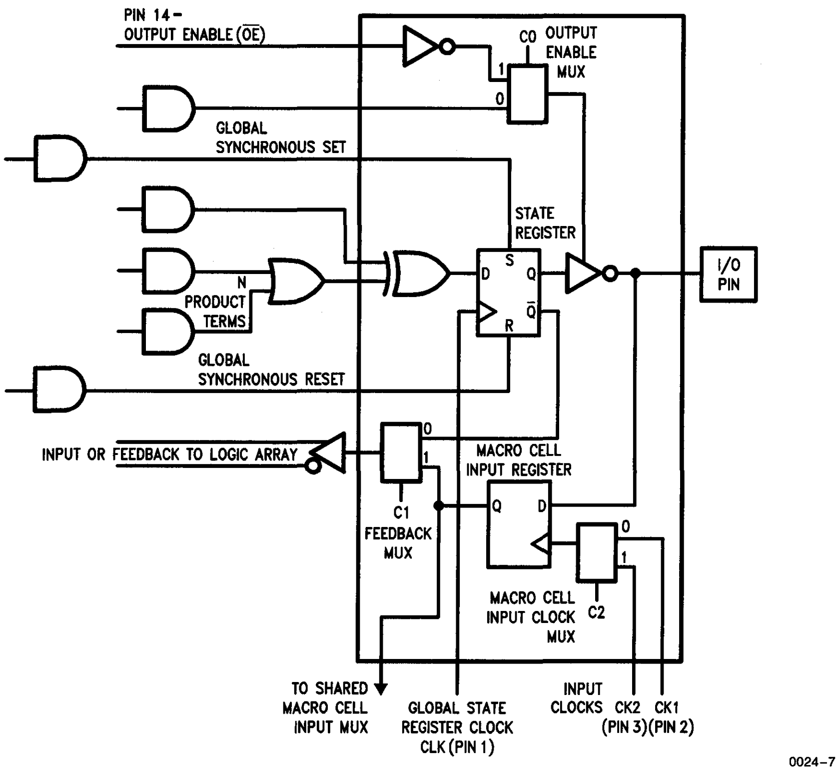


Figure 6. CY7C330 I/O Macro Cell

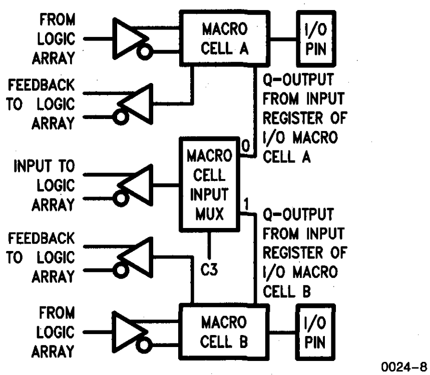


Figure 7. CY7C330 I/O Macro Cell Pair Shared Input MUX

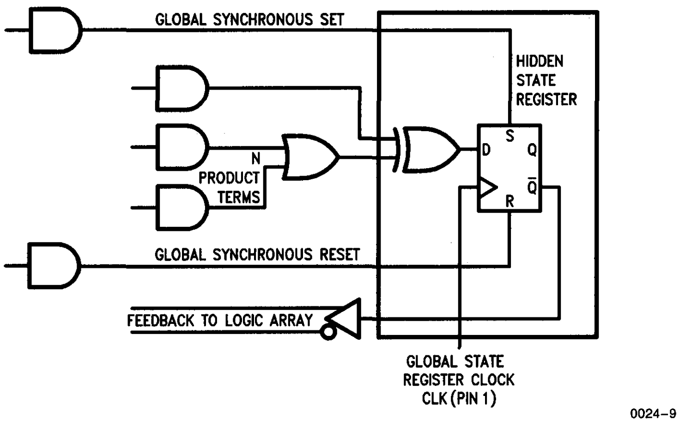


Figure 8. CY7C330 Hidden State Register Macro Cell

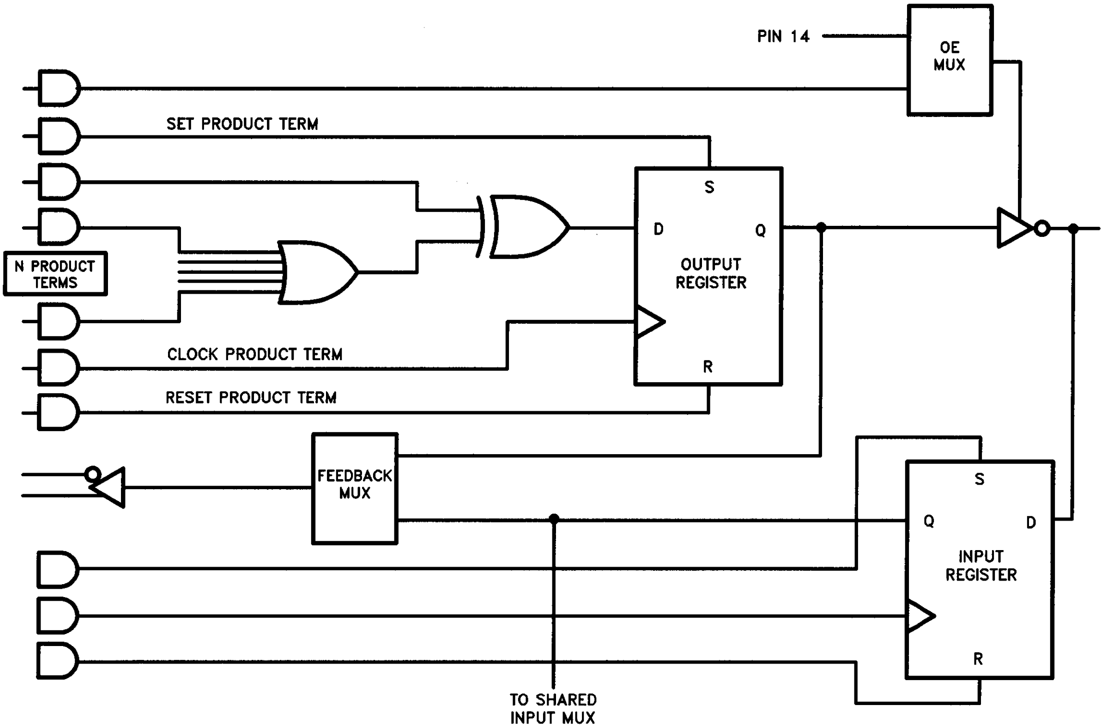


Figure 9. CY7C331 Registered Asynchronous Macrocell

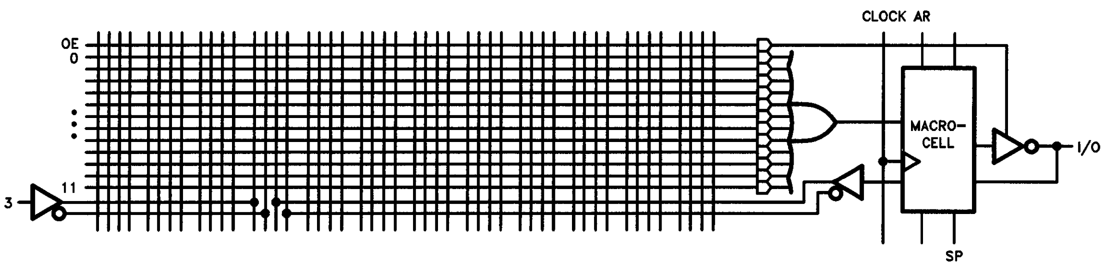


Figure 10. Programmable Macro Cell

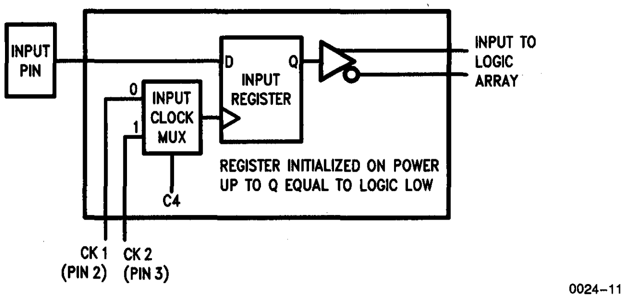


Figure 11. CY7C330 Dedicated Input Cell

PAL® C 20 Series

Reprogrammable CMOS PAL® C 16L8, 16R8, 16R6, 16R4

CYPRESS SEMICONDUCTOR

Features

- **CMOS EPROM technology for reprogrammability**
- **High performance at quarter power**
  - **— t_{PD} = 25 ns**
  - **— t_S = 20 ns**
  - **— t_{CO} = 15 ns**
  - **— I_{CC} = 45 mA**
- **High performance at military temperature**
  - **— t_{PD} = 20 ns**
  - **— t_S = 20 ns**
  - **— t_{CO} = 15 ns**
  - **— I_{CC} = 70 mA**
- **Commercial and military temperature range**
- **High reliability**
  - **— Proven EPROM technology**
  - **— >1500V input protection from electrostatic discharge**
  - **— 100% AC/DC tested**
  - **— 10% power supply tolerances**
  - **— High noise immunity**
  - **— Security feature prevents pattern duplication**
  - **— 100% programming and functional testing**

Functional Description

Cypress PAL C Series 20 devices are high speed electrically programmable and UV erasable logic devices produced in a proprietary "N" well CMOS EPROM process. These devices utilize the sum of products (AND-OR) structure providing users the ability to program custom logic functions serving unique requirements.

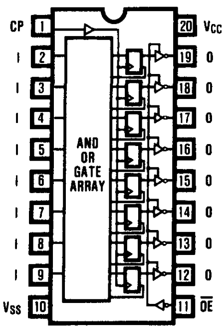
PALs are offered in 20-pin plastic and ceramic DIP, Plastic SOJ, and ceramic LCC packages. The ceramic package can be equipped with an erasure window; when exposed to UV light, the PAL is erased and can then be reprogrammed.

Before programming, AND gates or PRODUCT TERMS are connected via EPROM cells to both TRUE and COMPLEMENT inputs. Programming an EPROM cell disconnects an INPUT TERM from a PRODUCT TERM. Selective programming of these cells allows a specific logic function to be implemented in a PAL C device. PAL C devices are supplied in four functional configurations, desig-

4

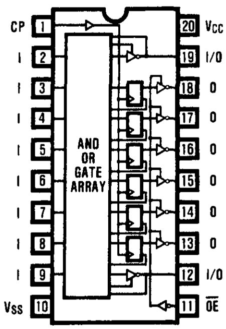
Logic Symbols and DIP and SOJ Pinouts

16R8



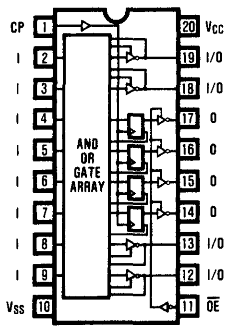
0038-1

16R6



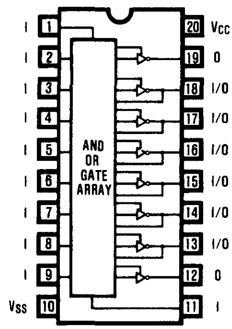
0038-2

16R4



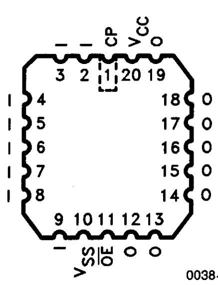
0038-3

16L8

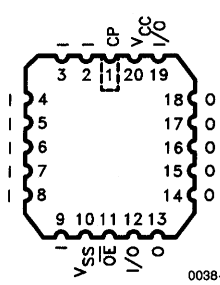


0038-4

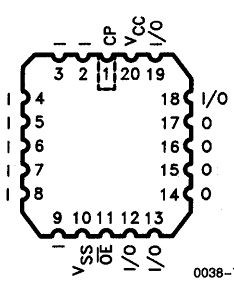
LCC Pinouts



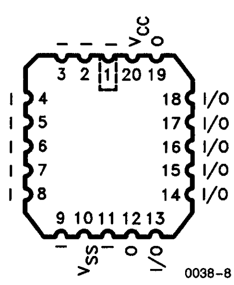
0038-5



0038-6



0038-7



0038-8

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Functional Description (Continued)

nated 16R8, 16R6, 16R4 and 16L8. These eight devices have potentially 16 inputs and 8 outputs configurable by the user. Output configurations of 8 registers, 8 combinatorial, 6 registers and 2 combinatorial as well as 4 registers and 4 combinatorial are provided by the four functional variations of the product family. All combinatorial outputs on the 16R6 and 16R4 as well as 6 of the combinatorial outputs on the 16L8 may be used as optional inputs. All registered outputs have the $\overline{Q}$ bar side of the register fed back into the main array. The registers are automatically initialized on power up to Q output LOW and $\overline{Q}$ output HIGH. All unused inputs should be tied to ground.

All PAL C devices feature a SECURITY function which provides the user protection for the implementation of proprietary logic. When invoked, the contents of the normal array may no longer be accessed in the verify mode. Because EPROM technology is used as a storage mechanism, the content of the array is not visible under a microscope. The PAL C device also contains a PHANTOM ARRAY used for functional and performance testing. The content of this array is always accessible, even when security is invoked.

Cypress PAL C products are produced in an advanced 1.2 micron "N" well CMOS EPROM technology. The use of this proven EPROM technology is the basis for a superior product with inherent advantages in reliability, testability, programming and functional yield. EPROM technology has the inherent advantage that all programmable elements may be programmed, tested and erased during the manufacturing process. This also allows the device to be 100% functionally tested during manufacturing. An ability to preload the registers of registered devices during the testing operation makes the testing easier and more efficient. The PHANTOM ARRAY and PHANTOM operating mode allow the device to be tested for functionality and performance after it has been packaged. Combining these inherent and designed-in features, an extremely high degree of functionality, programmability and assured AC performance are provided and testing becomes an easy task.

The REGISTER PRELOAD allows the user to initialize the registered devices to a known state prior to testing the device, significantly simplifying and shortening the testing procedure.

The PHANTOM MODE of operation provides a completely separate operating mode where the functionality of the device along with its AC performance may be ascertained. The user need not be encumbered by programmed cells in the normal operating mode. This PHANTOM MODE of operation allows additional input lines to be programmed to operate the PAL C device, exercising the device functionally and allowing AC performance measurements to be made. The PHANTOM MODE of operation acknowledges only the INPUT TERMS shown shaded in the functional block diagrams. Likewise, the normal PHANTOM INPUT TERMS do not exist in the normal mode of operation. During the final stages of manufacturing, some cells in the PHANTOM ARRAY are programmed for final AC and functional testing. These cells remain programmed, and may be used at incoming inspection to verify both functional and AC performance.

Commercial and Industrial Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)		t_{PD} (ns)		t_S (ns)		t_{CO} (ns)	
				L	COM'L/IND	-25	-35	-25	-35	-25	-35
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	45	70	25	35	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	—	—	20	30	15	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional								
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	45	70	25	35	20	30	15	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional								

Military Selection Guide

Generic Part Number	Logic	Output Enable	Outputs	I_{CC} (mA)	t_{PD} (ns)			t_S (ns)			t_{CO} (ns)		
					-20	-30	-40	-20	-30	-40	-20	-30	-40
16L8	(8) 7-wide AND-OR-Invert	Programmable	(6) Bidirectional (2) Dedicated	70	20	30	40	—	—	—	—	—	—
16R8	(8) 8-wide AND-OR	Dedicated	Registered Inverting	70	—	—	—	20	25	35	15	20	25
16R6	(6) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(2) 7-wide AND-OR-Invert	Programmable	Bidirectional										
16R4	(4) 8-wide AND-OR	Dedicated	Registered Inverting	70	20	30	40	20	25	35	15	20	25
	(4) 7-wide AND-OR-Invert	Programmable	Bidirectional										

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 20 to Pin 10)..................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) ....24 mA

DC Programming Voltage 14.0V

UV Exposure 7258 Wsec/cm2

Static Discharge Voltage ....>1500V
(per MIL-STD-883 Method 3015)

Latchup Current ....>200 mA

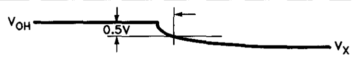
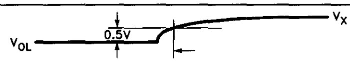
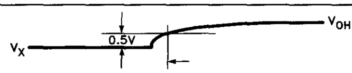
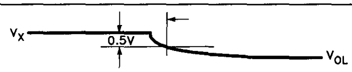
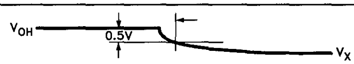
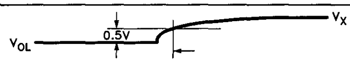
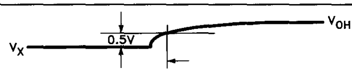
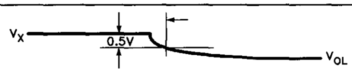
Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[7]	−55°C to +125°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)[6]

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Commercial/Industrial	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Commercial/Industrial		0.4	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logic HIGH[1] Voltage for all Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[1] Voltage for all Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$			−10	10	μA
V_{PP}	Programming Voltage	I_{PP} = 50 mA Max.			13.0	14.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]				−300	mA
I_{CC}	Power Supply Current	All Inputs = GND, V_{CC} = Max., I_{OUT} = 0 mA[5]		"L"		45	mA
				COM'L/IND		70	mA
				MIL		70	mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$			−100	100	μA

Table 1

Parameter	V_X	Output Waveform—Measurement Level
$t_{PXZ}(-)$	1.5V	 0038-26
$t_{PXZ}(+)$	2.6V	 0038-27
$t_{PZX}(+)$	V_{thc}	 0038-28
$t_{PZX}(-)$	V_{thc}	 0038-29
$t_{ER}(-)$	1.5V	 0038-26
$t_{ER}(+)$	2.6V	 0038-27
$t_{EA}(+)$	V_{thc}	 0038-28
$t_{EA}(-)$	V_{thc}	 0038-29

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C, f = 1$ MHz	7	pF
C_{OUT}	Output Capacitance	$V_{IN} = 0, V_{CC} = 5.0V$	7	

Switching Characteristics PAL C 20 Series Over Operating Range[4, 6, 8]

Parameters	Description	Commercial/Industrial				Military						Units
		-25		-35		-20		-30		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{EA}	Input to Output Enable 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{ER}	Input to Output Disable 16L8, 16R6, 16R4		25		35		20		30		40	ns
t_{PZX}	Pin 11 to Output Enable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{PXZ}	Pin 11 to Output Disable 16R8, 16R6, 16R4		20		25		20		25		25	ns
t_{CO}	Clock to Output 16R8, 16R6, 16R4		15		25		15		20		25	ns
t_S	Input or Feedback Setup Time 16R8, 16R6, 16R4	20		30		20		25		35		ns
t_H	Hold Time 16R8, 16R6, 16R4	0		0		0		0		0		ns
t_P	Clock Period	35		55		35		45		60		ns
t_W	Clock Width	15		20		12		20		25		ns
f_{MAX}	Maximum Frequency		28.5		18		28.5		22		16.5	MHz

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT} = 0.5V$ has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. *Figure 1a* test load used for all parameters except t_{EA}, t_{ER} t_{PZX} and t_{PXZ}. *Figure 1b* test load used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
5. $I_{CC(AC)}$ = (0.6 mA/MHz) × (Operating Frequency in MHz) + $I_{CC(DC)}$. $I_{CC(DC)}$ is measured with an unprogrammed device.
6. See the last page of this specification for Group A subgroup testing information.
7. T_A is the "instant on" case temperature.
8. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to $V_{OH} - 0.5V$ for an enabled HIGH output or $V_{OL} + 0.5V$ for an enabled LOW output. Please see Table 1 for waveforms and measurement reference levels.

AC Test Loads and Waveforms

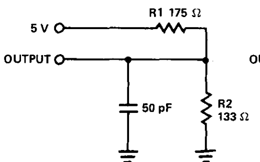


Figure 1a. Commercial

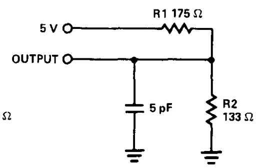
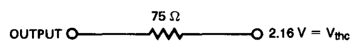


Figure 1b. Commercial

0038–11

Equivalent to:
THÉVENIN EQUIVALENT COMMERCIAL



0038–10

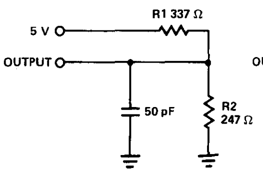


Figure 1c. Military

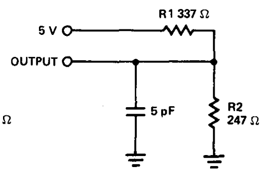
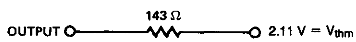


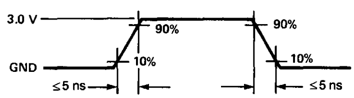
Figure 1d. Military

0038–9

Equivalent to:
THÉVENIN EQUIVALENT MILITARY



0038–12



0038–13

Figure 2

Switching Waveforms

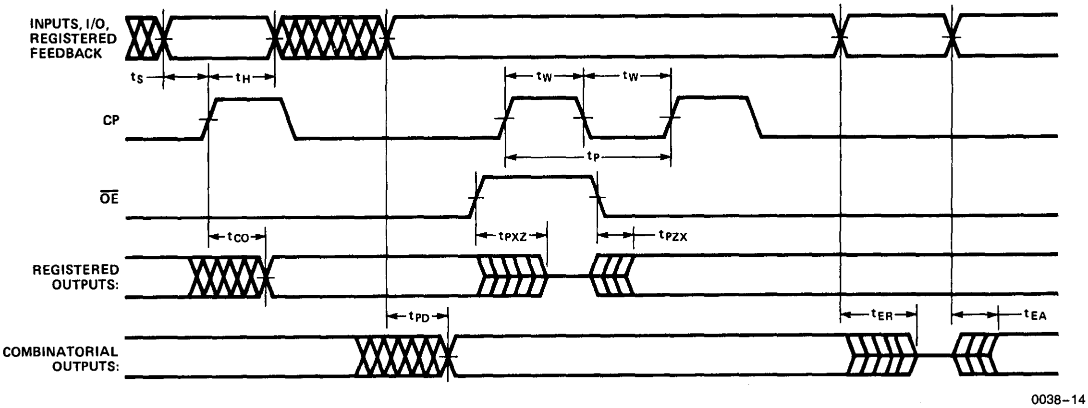


Figure 3

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PAL C device. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs which may cause "blank" check failures or "verify errors" when programming "windowed" parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity x exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure would be approximately 35 minutes. The PAL C device needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming

PAL C devices are programmed a BYTE at a time using a voltage to transfer electrons to a floating gate. The array programmed is addressed as memory of 256 bytes, using address Tables 5 and 6. These addresses are supplied to the device over Pins 2 through 9. The data to be programmed is supplied on data inputs D0 through D7 (Pins 19 through 12 inclusive). In the unprogrammed state, all inputs are connected to product terms. A "1" on a data line causes a cell to be programmed, disconnecting an INPUT TERM from a PRODUCT TERM. During verify, an unprogrammed cell causes a "1" to appear on the output, while a programmed cell will appear as a "0". Table 4 describes the operating modes of the device and the programming waveforms are described in *Figures 6* through *9*. The actual sequence required to program a cell is described in *Figure 5* and applies for programming either standard or phantom portions of the array. The security bit should be programmed using a single 10 ms pulse, and verified per *Figure 9.*

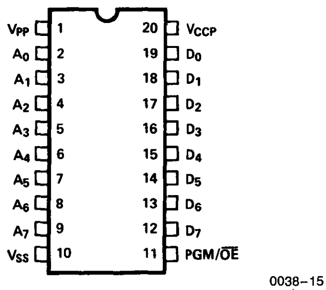


Figure 4. Programming Pin Configuration

DC Programming Parameters Ambient Temperature = 25°C

Table 2

Parameter	Description	Min.	Max.	Units	Notes
V_{PP}	Programming Voltage	13.0	14.0	V	
V_{CCP}	Supply Voltage During Programming	4.75	5.25	V	
V_{IHP}	Programming Input High Voltage	3.0		V	
V_{ILP}	Programming Input Low Voltage		0.4	V	
V_{OH}	Output High Voltage	2.4		V	1
V_{OL}	Output Low Voltage		0.4	V	1
I_{PP}	Programming Supply Current		50	mA	

AC Programming Parameters Ambient Temperature = 25°C

Table 3

Parameter	Description	Min.	Max.	Units	Notes
t_{PP}	Programming Pulse Width	100	10,000	μs	2
t_S	Setup Time	1.0		μs	
t_H	Hold Time	1.0		μs	
t_r, t_f	V_{PP} Rise and Fall Time	1.0		μs	2
t_{VD}	Delay to Verify	1.0		μs	
t_{VP}	Verify Pulse Width	2.0		μs	
t_{DV}	Verify to Data Valid	20.0		μs	
t_{DZ}	Verify to High Z		1.0	μs	

Table 4

Pin Name	V_{PP}	PGM/$\overline{OE}$	A1	A2	A3	A4	A5	D7–D0	Notes
Pin Number	(1)	(11)	(3)	(4)	(5)	(6)	(7)	(12–19)	
Operating Modes									
PAL	X	X	X	X	X	X	X	Programmed Function	3, 4
Program PAL	V_{PP}	V_{PP}	X	X	X	X	X	Data In	3, 5
Program Inhibit	V_{PP}	V_{IHP}	X	X	X	X	X	High Z	3, 5
Program Verify/Blank Check	V_{PP}	V_{ILP}	X	X	X	X	X	Data Out	3, 5, 11
Phantom PAL	X	X	X	X	X	V_{PP}	X	Programmed Function	3, 6
Program Phantom PAL	V_{PP}	V_{PP}	X	X	X	X	V_{PP}	Data In	3, 7
Phantom Program Inhibit	V_{PP}	V_{IHP}	X	X	X	X	V_{PP}	High Z	3, 7
Phantom Program Verify	V_{PP}	V_{ILP}	X	X	X	X	V_{PP}	Data Out	3, 7
Program Security Bit	V_{PP}	V_{PP}	V_{PP}	X	X	X	X	High Z	3, 8
Verify Security Bit	X	X	Note 9	V_{PP}	X	X	X	High Z	3
Register Preload	X	X	X	X	V_{PP}	X	X	Data In	3, 10

Notes:

1. During verify operation
2. Measured at 10% and 90% points
3. $V_{SS} < X < V_{CCP}$
4. All "X" inputs operational per normal PAL function.
5. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address Tables 5 and 6.
6. All "X" inputs operational per normal PAL function except that they operate on the function that occupies the phantom array.
7. Address inputs occupy Pins 2 thru 9 inclusive, for both programming and verification see programming address Tables 5 and 6. Pin 7 is used to select the phantom mode of operation and must be taken to V_{PP} before selecting phantom program operation with V_{PP} on Pin 1.
8. See *Figure 8* for security programming sequence.
9. The state of Pin 3 indicates if the security function has been invoked or not. If Pin 3 = V_{OL} security is in effect, if Pin 3 = V_{OH}, the data is unsecured and may be directly accessed.
10. For testing purposes, the output latch on the 16R8, 16R6 and 16R4 may be preloaded with data from the appropriate associated output line.
11. It is necessary to toggle Pin 11 ($\overline{OE}$) HIGH during all address transitions while in the Program Verify or Blank Check mode.

The programmable array is addressed as a basic 256 by 8 memory structure with a duplication of the phantom array located at the same addresses as columns 0, 1, 2 and 3. The ability to address the phantom array as differentiated from the first 4 columns of the normal array is accomplished by taking Pin 7 to V_{PP} and entering the phantom mode of operation as shown in Tables 4 and 6. In either case, phantom or normal, product terms are addressed in groups of 8 per Table 5. Notice that this is accomplished by modulo 8 selecting every eighth product term starting with 0, 8, 16, 24, 32, 40, 48 and 56 corresponding to PROGRAMMED DATA INPUT on D0 through D7 respectively and incrementing each product term by one until all 64 PRODUCT TERMS are addressed. Each of the INPUT TERMS is addressed 8 times corresponding to the 8 groups of individual product terms addressed before being incremented.

Table 5

Product Term Addresses										
Binary Addresses			Line Number							
Pin Numbers										
(4)	(3)	(2)								
V_{ILP}	V_{ILP}	V_{ILP}	0	8	16	24	32	40	48	56
V_{ILP}	V_{ILP}	V_{IHP}	1	9	17	25	33	41	49	57
V_{ILP}	V_{IHP}	V_{ILP}	2	10	18	26	34	42	50	58
V_{ILP}	V_{IHP}	V_{IHP}	3	11	19	27	35	43	51	59
V_{IHP}	V_{ILP}	V_{ILP}	4	12	20	28	36	44	52	60
V_{IHP}	V_{ILP}	V_{IHP}	5	13	21	29	37	45	53	61
V_{IHP}	V_{IHP}	V_{ILP}	6	14	22	30	38	46	54	62
V_{IHP}	V_{IHP}	V_{IHP}	7	15	23	31	39	47	55	63
			D0	D1	D2	D3	D4	D5	D6	D7
			Programmed Data Input							

Table 6

Input Term Addresses					
Input Term Numbers	Binary Addresses				
	Pin Numbers				
	(9)	(8)	(7)	(6)	(5)
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
2	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
3	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
5	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
6	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
7	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
8	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
9	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
11	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
12	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
13	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
15	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}
16	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
17	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}

Input Term Addresses					
Input Term Numbers	Binary Addresses				
	Pin Numbers				
	(9)	(8)	(7)	(6)	(5)
18	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
19	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
20	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
21	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
22	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
23	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
24	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
25	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
26	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
27	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
28	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
29	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
30	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
31	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}
P0	V_{ILP}	V_{ILP}	V_{PP}	X	X
P1	V_{ILP}	V_{IHP}	V_{PP}	X	X
P2	V_{IHP}	V_{ILP}	V_{PP}	X	X
P3	V_{IHP}	V_{IHP}	V_{PP}	X	X

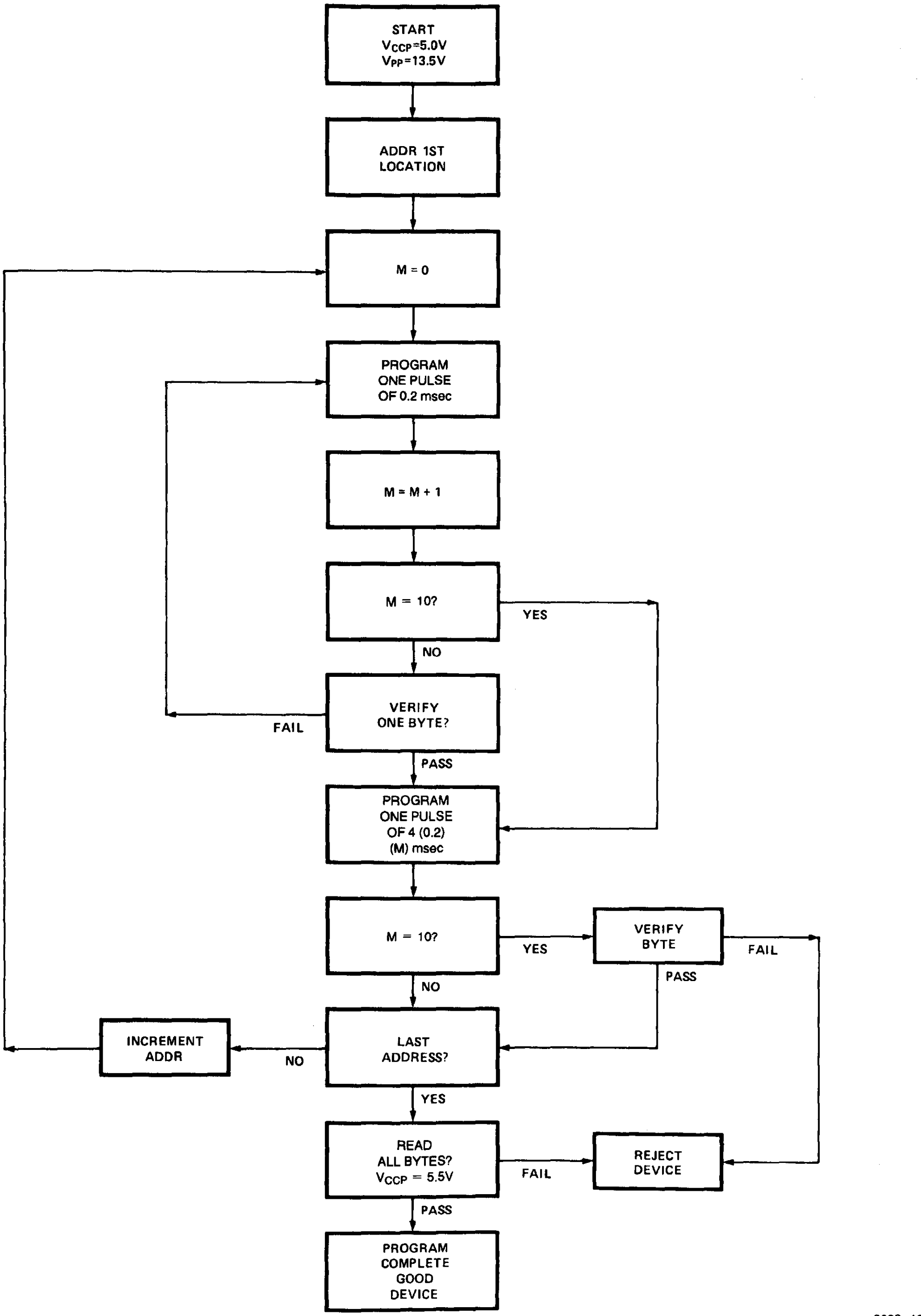
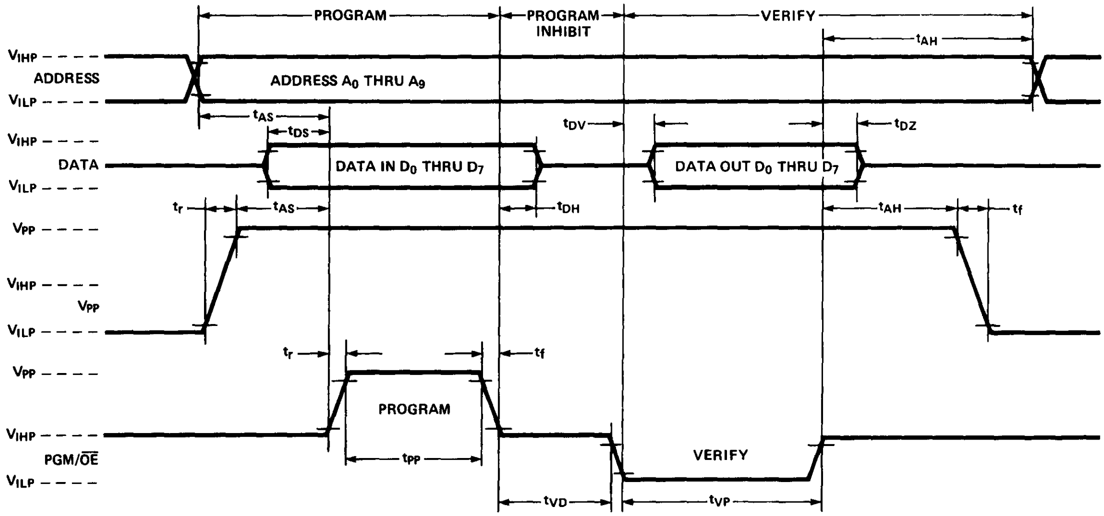
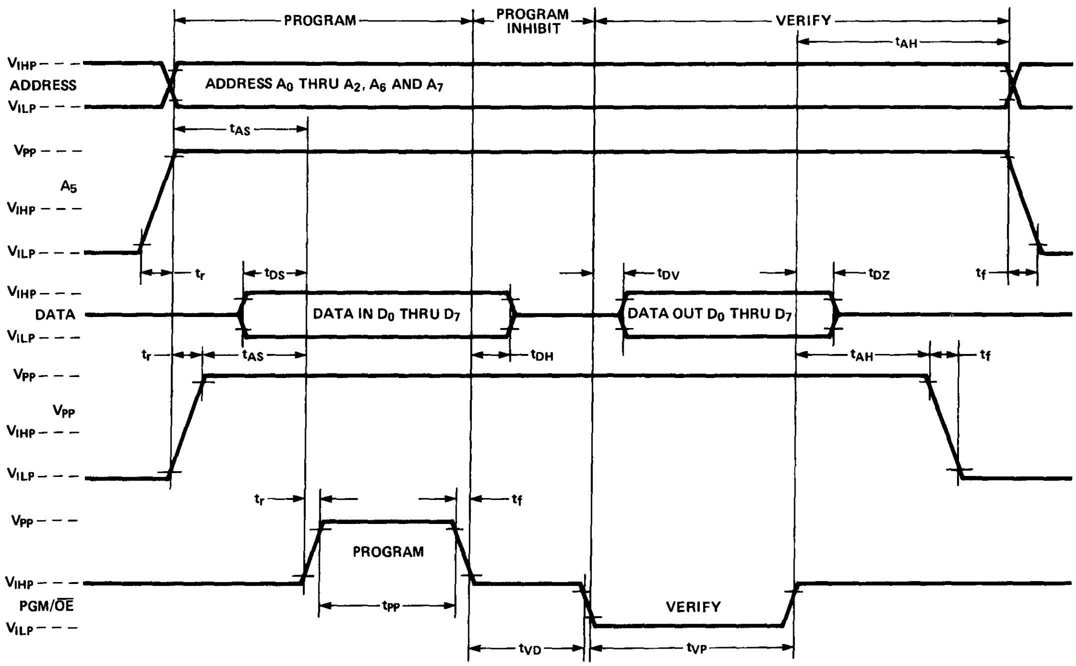


Figure 5. Programming Flowchart



0038–17

Figure 6. Programming Waveforms Normal Array



0038–18

Figure 7. Program Waveforms Phantom Array

4

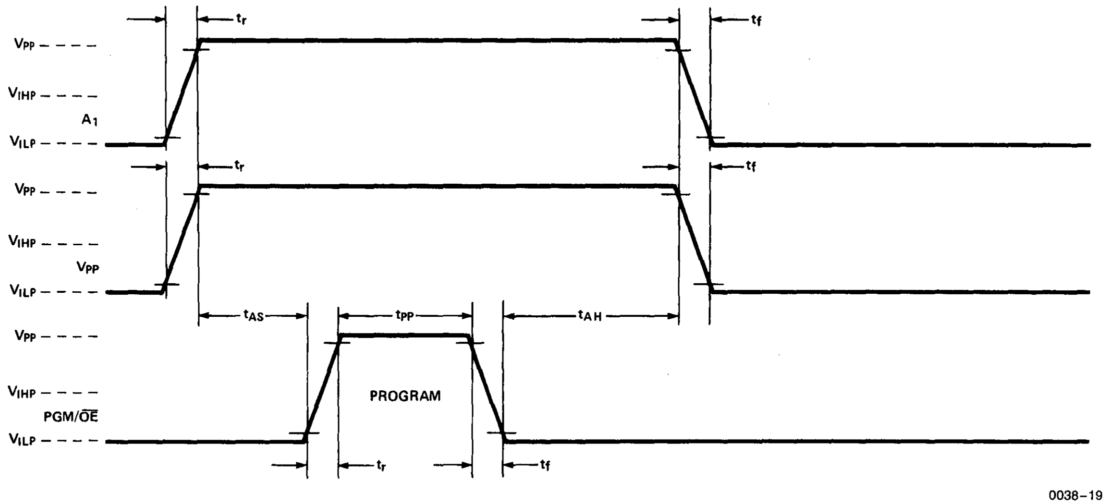


Figure 8. Activating Program Security

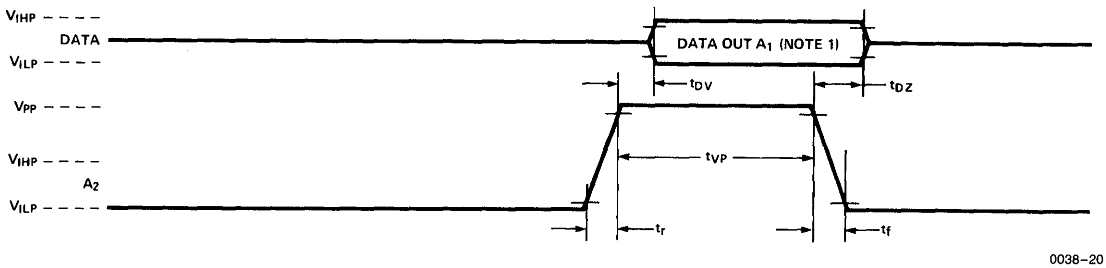
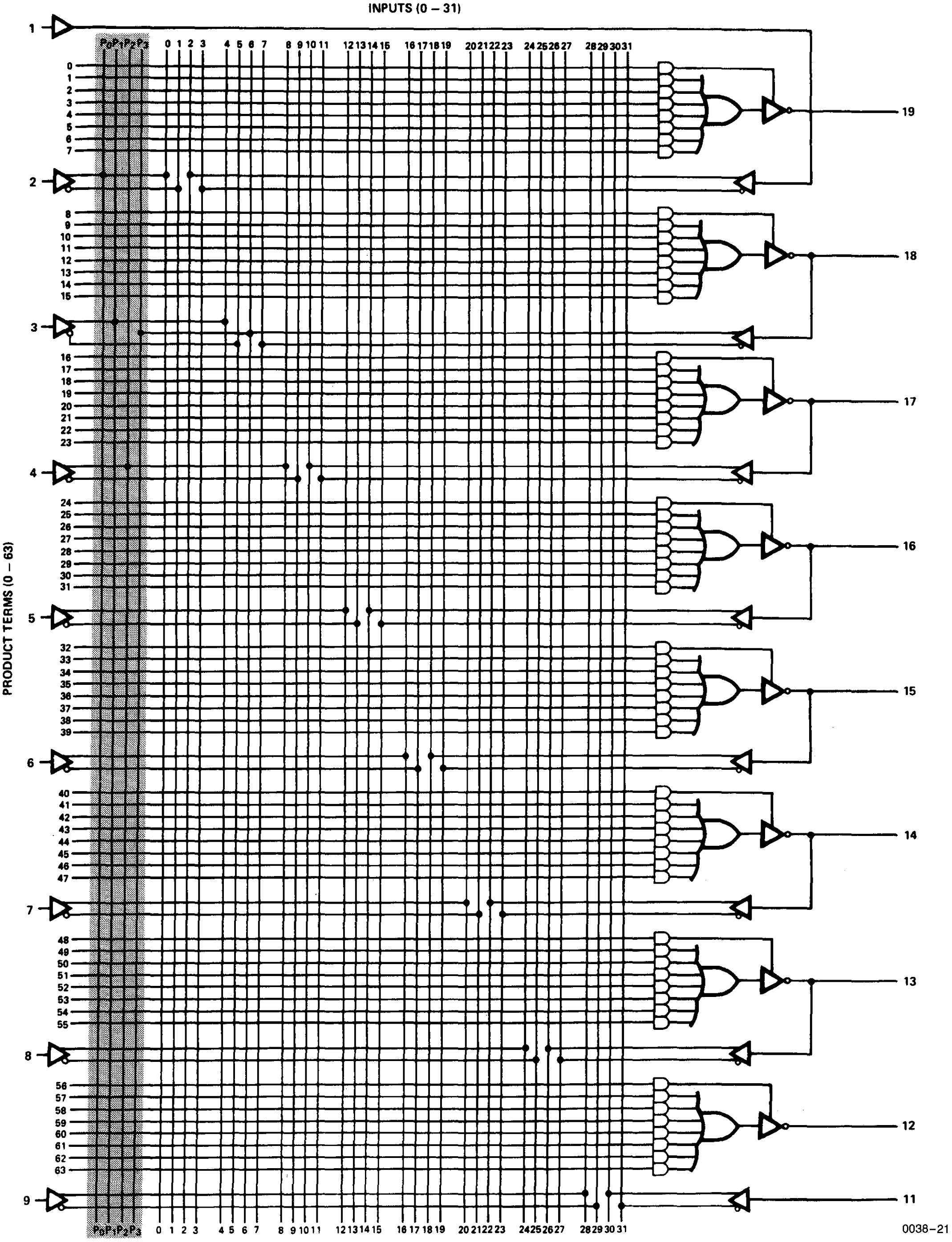


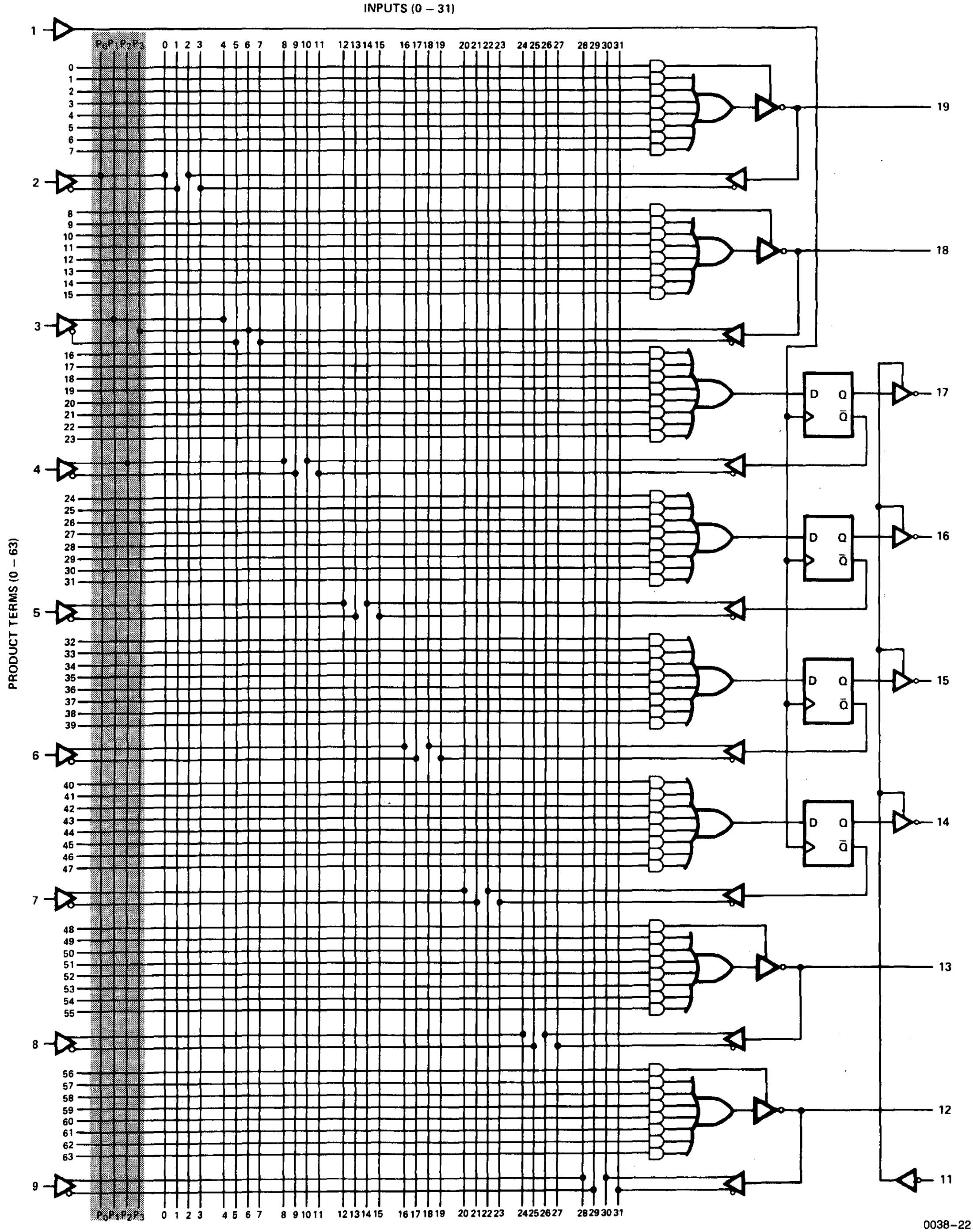
Figure 9. Verify Program Security

Functional Logic Diagram PAL C 16L8

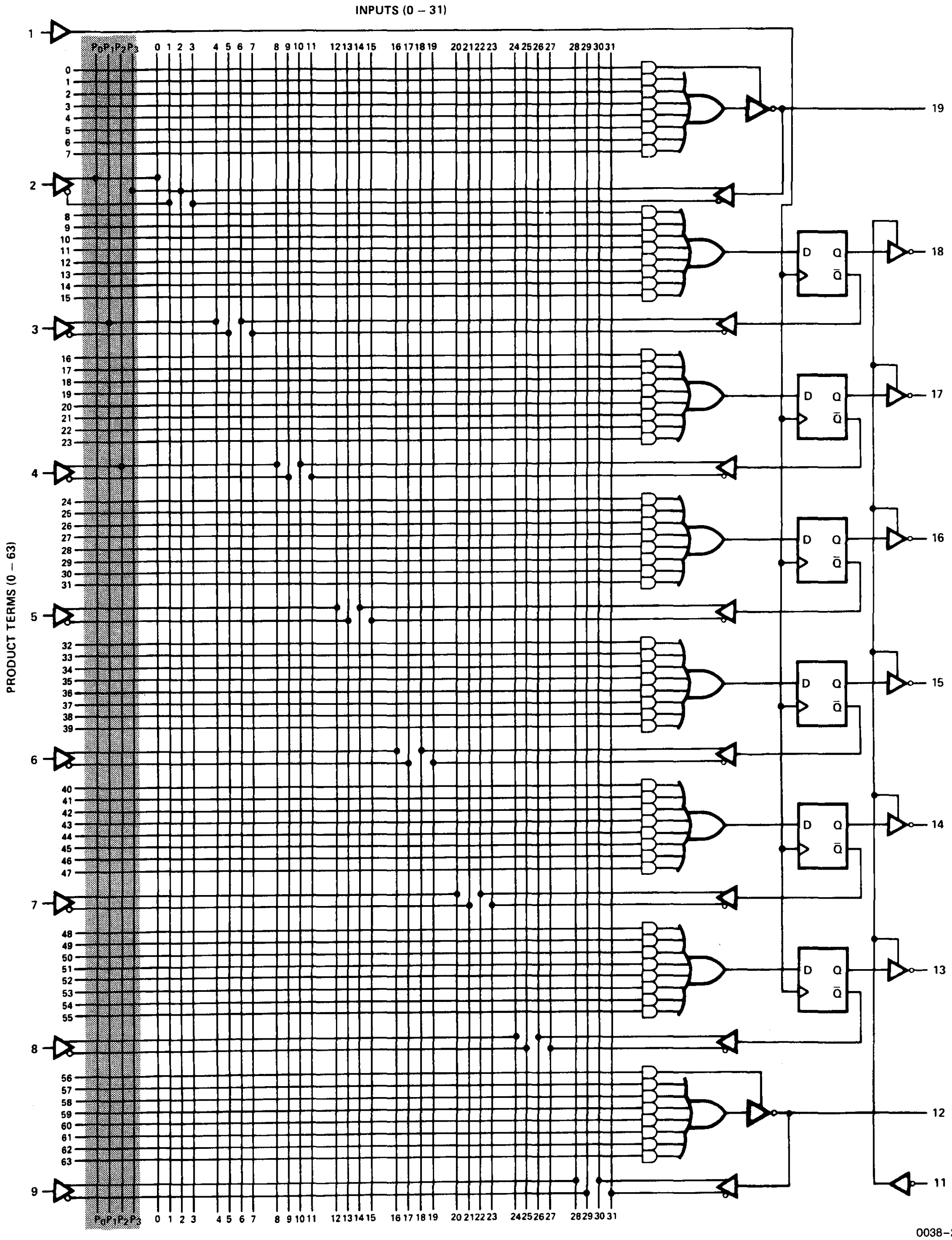


4

Functional Logic Diagram PAL C 16R4

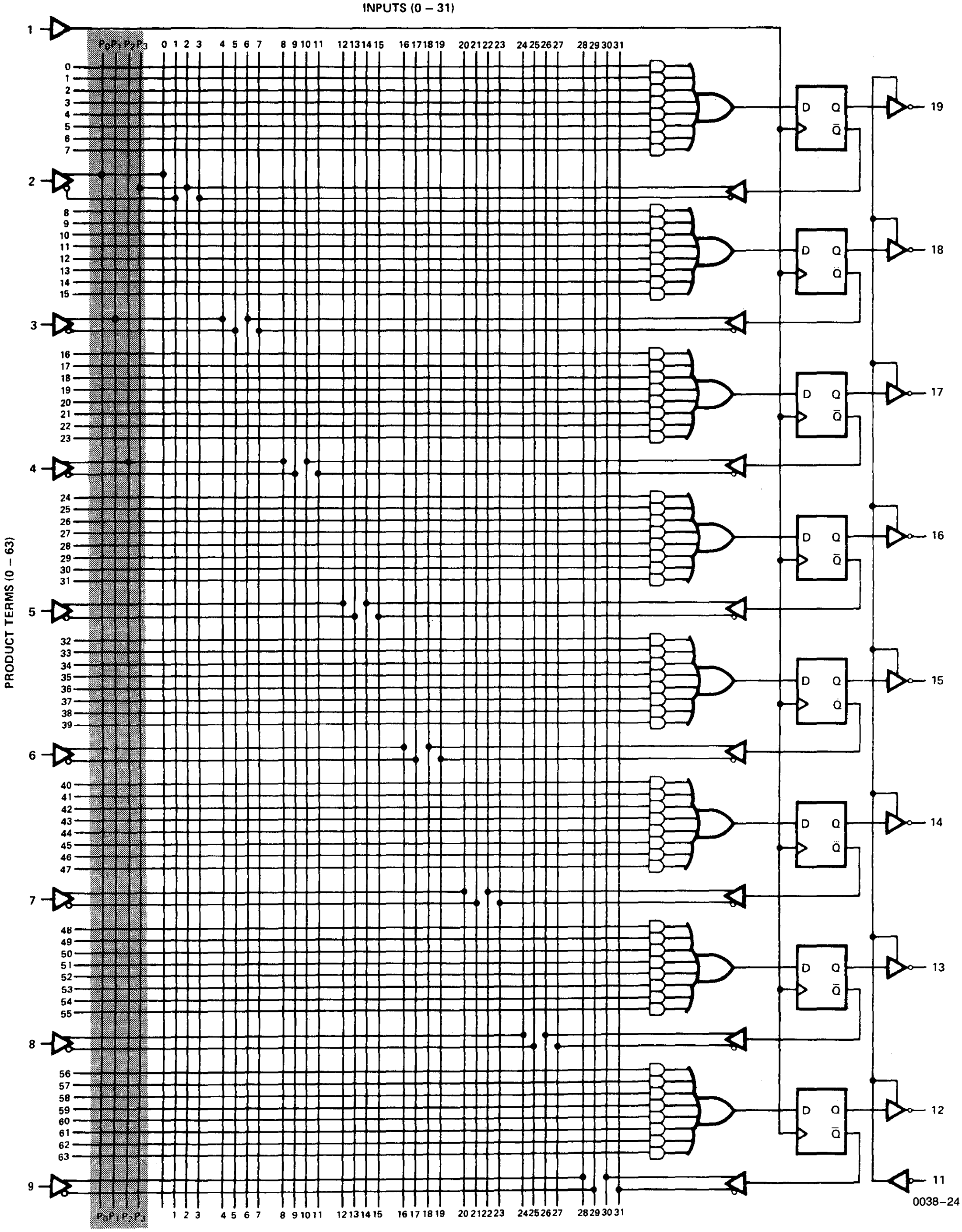


Functional Logic Diagram PAL C 16R6



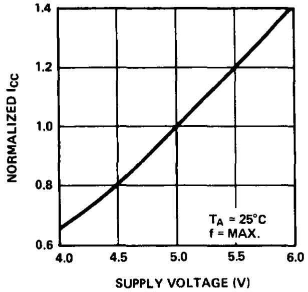
0038–23

Functional Logic Diagram PAL C 16R8

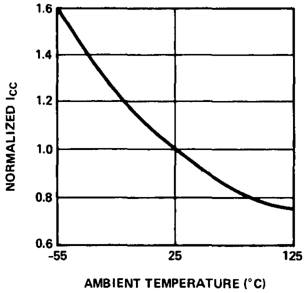


Typical DC and AC Characteristics

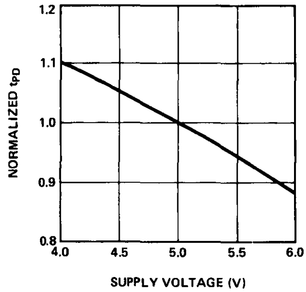
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE

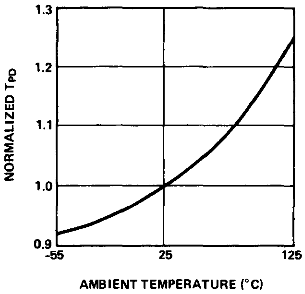


NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE

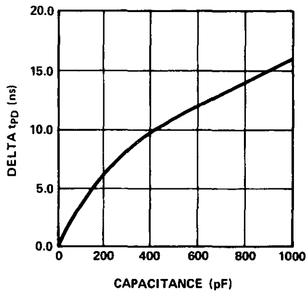


4

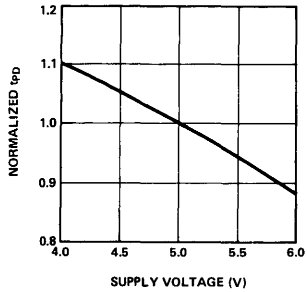
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



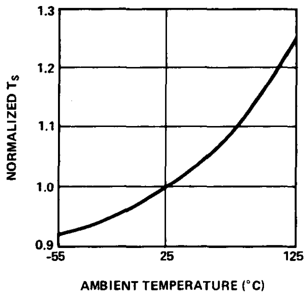
DELTA PROPAGATION TIME vs. OUTPUT LOADING



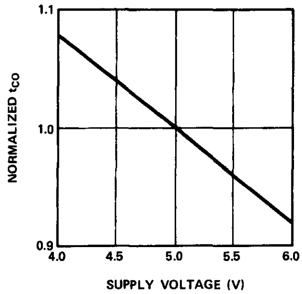
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



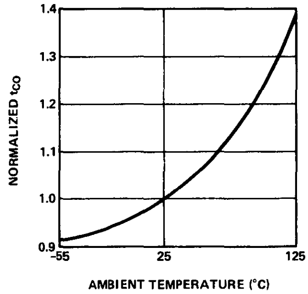
NORMALIZED SETUP TIME vs. TEMPERATURE



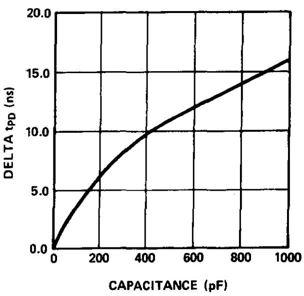
NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



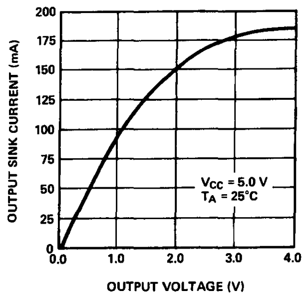
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



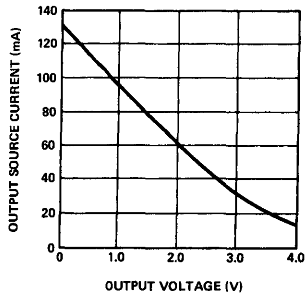
DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



0038-25

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package	Operating Range
20	—	—	70	PAL C 16L8-20DMB	D6	Military
				PAL C 16L8-20LMB	L61	
				PAL C 16L8-20WMB	W6	
				PAL C 16L8-20KMB	K71	
				PAL C 16L8-20QMB	Q61	
25	—	—	45	PAL C 16L8L-25PC	P5	Commercial
				PAL C 16L8L-25VC	V5	
				PAL C 16L8L-25LC	L61	
				PAL C 16L8L-25WC	W6	
			70	PAL C 16L8-25PC/PI	P5	
				PAL C 16L8-25VC/VI	V5	
				PAL C 16L8-25LC	L61	
				PAL C 16L8-25WC/WI	W6	
30	—	—	70	PAL C 16L8-30DMB	D6	Military
				PAL C 16L8-30LMB	L61	
				PAL C 16L8-30WMB	W6	
				PAL C 16L8-30KMB	K71	
				PAL C 16L8-30QMB	Q61	
35	—	—	45	PAL C 16L8L-35PC	P5	Commercial
				PAL C 16L8L-35VC	V5	
				PAL C 16L8L-35LC	L61	
				PAL C 16L8L-35WC	W6	
			70	PAL C 16L8-35PC/PI	P5	
				PAL C 16L8-35VC/VI	V5	
				PAL C 16L8-35LC	L61	
				PAL C 16L8-35WC/WI	W6	
40	—	—	70	PAL C 16L8-40DMB	D6	Military
				PAL C 16L8-40LMB	L61	
				PAL C 16L8-40WMB	W6	
				PAL C 16L8-40KMB	K71	
				PAL C 16L8-40QMB	Q61	
20	20	15	70	PAL C 16R4-20DMB	D6	Military
				PAL C 16R4-20LMB	L61	
				PAL C 16R4-20WMB	W6	
				PAL C 16R4-20KMB	K71	
				PAL C 16R4-20QMB	Q61	
25	20	15	45	PAL C 16R4L-25PC	P5	Commercial
				PAL C 16R4L-25VC	V5	
				PAL C 16R4L-25LC	L61	
				PAL C 16R4L-25WC	W6	
			70	PAL C 16R4-25PC/PI	P5	
				PAL C 16R4-25VC/VI	V5	
				PAL C 16R4-25LC	L61	
				PAL C 16R4-25WC/WI	W6	

Ordering Information (Continued)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package	Operating Range
30	25	20	70	PAL C 16R4-30DMB	D6	Military
				PAL C 16R4-30LMB	L61	
				PAL C 16R4-30WMB	W6	
				PAL C 16R4-30KMB	K71	
				PAL C 16R4-30QMB	Q61	
35	30	25	45	PAL C 16R4L-35PC	P5	Commercial
				PAL C 16R4L-35VC	V5	
				PAL C 16R4L-35LC	L61	
				PAL C 16R4L-35WC	W6	
			70	PAL C 16R4-35PC/PI	P5	
				PAL C 16R4-35VC/VI	V5	
				PAL C 16R4-35LC	L61	
				PAL C 16R4-35WC/WI	W6	
40	35	25	70	PAL C 16R4-40DMB	D6	Military
				PAL C 16R4-40LMB	L61	
				PAL C 16R4-40WMB	W6	
				PAL C 16R4-40KMB	K71	
				PAL C 16R4-40QMB	Q61	
20	20	15	70	PAL C 16R6-20DMB	D6	Military
				PAL C 16R6-20LMB	L61	
				PAL C 16R6-20WMB	W6	
				PAL C 16R6-20KMB	K71	
				PAL C 16R6-20QMB	Q61	
25	20	15	45	PAL C 16R6L-25PC	P5	Commercial
				PAL C 16R6L-25VC	V5	
				PAL C 16R6L-25LC	L61	
				PAL C 16R6L-25WC	W6	
			70	PAL C 16R6-25PC/PI	P5	
				PAL C 16R6-25VC/VI	V5	
				PAL C 16R6-25LC	L61	
				PAL C 16R6-25WC/WI	W6	
30	25	20	70	PAL C 16R6-30DMB	D6	Military
				PAL C 16R6-30LMB	L61	
				PAL C 16R6-30WMB	W6	
				PAL C 16R6-30KMB	K71	
				PAL C 16R6-30QMB	Q61	
35	30	25	45	PAL C 16R6L-35PC	P5	Commercial
				PAL C 16R6L-35VC	V5	
				PAL C 16R6L-35LC	L61	
				PAL C 16R6L-35WC	W6	
			70	PAL C 16R6-35PC/PI	P5	
				PAL C 16R6-35VC/VI	V5	
				PAL C 16R6-35LC	L61	
				PAL C 16R6-35WC/WI	W6	

Ordering Information (Continued)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package	Operating Range
40	35	25	70	PAL C 16R6-40DMB	D6	Military
				PAL C 16R6-40LMB	L61	
				PAL C 16R6-40WMB	W6	
				PAL C 16R6-40KMB	K71	
				PAL C 16R6-40QMB	Q61	
—	20	15	70	PAL C 16R8-20DMB	D6	Military
				PAL C 16R8-20LMB	L61	
				PAL C 16R8-20WMB	W6	
				PAL C 16R8-20KMB	K71	
				PAL C 16R8-20QMB	Q61	
—	20	15	45	PAL C 16R8L-25PC	P5	Commercial
				PAL C 16R8L-25VC	V5	
				PAL C 16R8L-25LC	L61	
				PAL C 16R8L-25WC	W6	
			70	PAL C 16R8-25PC/PI	P5	
				PAL C 16R8-25VC/VI	V5	
				PAL C 16R8-25LC	L61	
				PAL C 16R8-25WC/WI	W6	
—	25	20	70	PAL C 16R8-30DMB	D6	Military
				PAL C 16R8-30LMB	L61	
				PAL C 16R8-30WMB	W6	
				PAL C 16R8-30KMB	K71	
				PAL C 16R8-30QMB	Q61	
—	30	25	45	PAL C 16R8L-35PC	P5	Commercial
				PAL C 16R8L-35VC	V5	
				PAL C 16R8L-35LC	L61	
				PAL C 16R8L-35WC	W6	
			70	PAL C 16R8-35PC/PI	P5	
				PAL C 16R8-35VC/VI	V5	
				PAL C 16R8-35LC	L61	
				PAL C 16R8-35WC/WI	W6	
—	35	25	70	PAL C 16R8-40DMB	D6	Military
				PAL C 16R8-40LMB	L61	
				PAL C 16R8-40WMB	W6	
				PAL C 16R8-40KMB	K71	
				PAL C 16R8-40QMB	Q61	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
V_{PP}	1,2,3
I_{CC}	1,2,3
I_{OZ}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{PD}	9,10,11
t_{PZX}	9,10,11
t_{CO}	9,10,11
t_S	9,10,11
t_H	9,10,11

Document #: 38-00001-C

CYPRESS SEMICONDUCTOR

CMOS Generic 20 Pin Programmable Logic Device

Features

- **Fast**
  - **— Commercial: t_{PD} = 12 ns, t_{CO} = 10 ns, t_S = 12 ns**
  - **— Military: t_{PD} = 15 ns, t_{CO} = 12 ns, t_S 15 ns**
- **Low power**
  - **— I_{CC} max.: 110 mA**
- **Commercial and military temperature range**
- **User-programmable output cells**
  - **— Selectable for registered or combinatorial operation**
  - **— Output polarity control**
  - **— Output enable source selectable from pin 11 or product term**
- **Generic architecture to replace standard logic functions including: 10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2, 10P8, 12P6, 14P4, 16P2, 16H8, 16L8, 16P8, 16R8, 16R6, 16R4, 16RP8, 16RP6, 16RP4, 18P8, 16V8**
- **Eight product terms and one OE product term per output**
- **CMOS EPROM technology for reprogrammability**
- **Highly reliable**
  - **— Uses proven EPROM technology**
  - **— Fully AC and DC tested**
  - **— Security feature prevents logic pattern duplication**
  - **— >2000V input protection for electrostatic discharge**

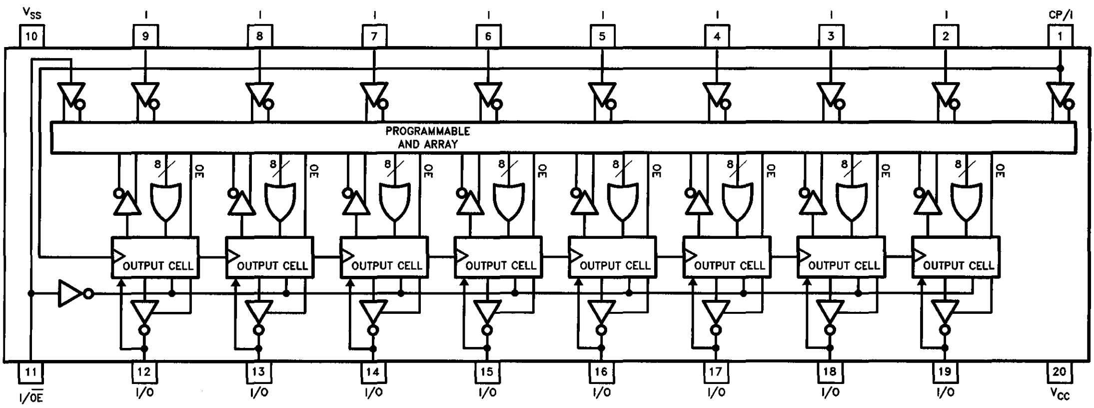
Functional Description

Cypress PLD devices are high speed electrically programmable Logic Devices. These devices utilize the sum of products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be

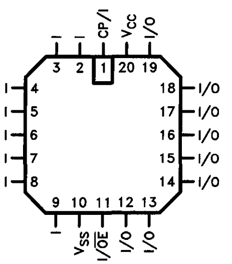
Logic Symbol, DIP and SOJ Pinout

18G8



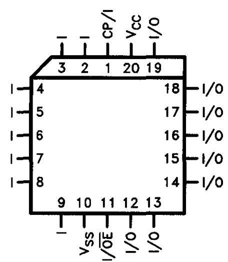
0139-1

LCC Pinout



0139-2

PLCC Pinout



0139-3

Selection Guide

Generic Part Number	I_{CC} (mA)		t_{PD} (ns)		t_S		t_{CO}	
	Com	Mil	Com	Mil	Com	Mil	Com	Mil
18G8-12	90		12		12		10	
18G8-15	90	110	15	15	12	15	12	12
18G8-15L	70		15		12		12	
18G8-20		110		20		20		15

Functional Description (Continued)

connected to either the true or complement or disconnected from both true and complement inputs.

Cypress PLD C 18G8 uses an advanced 0.8 micron CMOS technology and a proven EPROM cell as the programmable element. This technology and the inherent advantage of being able to program and erase each cell enhances the reliability and testability of the circuit. This reduces the burden on the customer to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

18G8 Functional Description

The PLD C 18G8 is a generic 20 pin device that can be programmed to logic functions which include but are not limited to: 10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2, 10P8, 12P6, 14P4, 16P2, 16H8, 16L8, 16P8, 16R8, 16R6, 16R4, 16RP8, 16RP6, 16RP4, 18P8, 16V8. Thus, the PLD C 18G8 provides significant design, inventory and programming flexibility over dedicated 20 pin devices. It is executed in a 20 pin 300 mil molded DIP and a 300 mil windowed Cerdip. It provides up to 18 inputs and 8 outputs. When the windowed CERDIP is exposed to UV light, the 18G8 is erased and then can be reprogrammed.

The Programmable Output Cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with "REGISTERED" or "COMBINATORIAL" outputs, "ACTIVE HIGH" or "ACTIVE LOW" outputs, and "PRODUCT TERM" or "PIN 11" generated output enables. Four Architecture Bits determine the configurations as shown in Table 1. A total of sixteen different configurations are possible. The default or unprogrammed state is REGISTERED/ACTIVE/LOW/Pin 11 OE. The entire Programmable Output Cell is shown in *Figure 1.*

The architecture bit 'C1' controls the REGISTERED/COMBINATORIAL option. In either "COMBINATORIAL" or "REGISTERED" configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. Any unused inputs should be tied to ground. In either "REGISTERED" or "COMBINATORIAL" configuration, the output of the register may be fed back to the array. This allows the creation of state machines by providing storage and feedback of the current system state. The register is clocked by the signal from Pin 1. The register is initialized on power up to Q output LOW and $\overline{Q}$ output HIGH.

In both the Combinatorial and Registered configurations, the source of the "OUTPUT ENABLE" signal can be individually chosen with architecture bit 'C2'. The OE signal may be generated within the array, or from the external $\overline{OE}$ pin (Pin 11). The Pin 11 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for "OUTPUT POLARITY". The output can be either Active HIGH or Active LOW. This option is controlled by architecture bit 'C0'.

Along with this increase in functional density, the Cypress PLD C 18G8 provides lower power operation through the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. The phantom array allows the 18G8 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PLD C 18G8 at incoming inspection before committing the device to a specific function through programming.

Programmable Output Cell

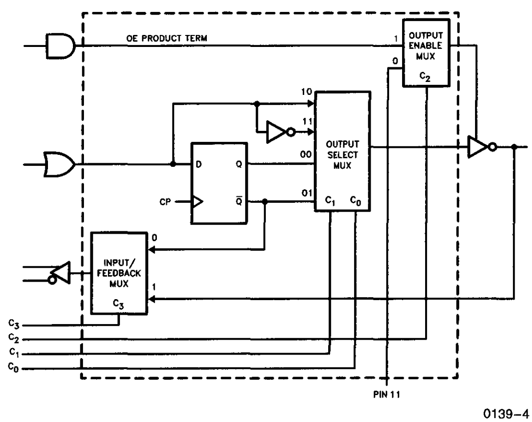


Figure 1

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 24 mA

DC Programming Voltage 13.0V

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±5%
Military[7]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)[7]

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Commercial	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA	Commercial		0.5	V
			I_{OL} = 12 mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH[1] Voltage for all Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[1] Voltage for all Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$			−10	10	μA
V_{PP}		Programming Voltage @ I_{PP} = 50 mA Max.			12.0	13.0	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]			−30	−90	mA
I_{CC}	Power Supply Current	V_{IN} = 0 V_{CC} = Max., I_{OUT} = 0 mA	Commercial -15L			70	mA
			Commercial -12, -15			90	
			Military			110	
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−40	40	μA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{IN} = 2.0V, V_{CC} = 5.0V	8	

AC Test Loads and Waveforms (Commercial)

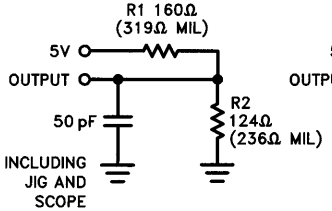


Figure 2a

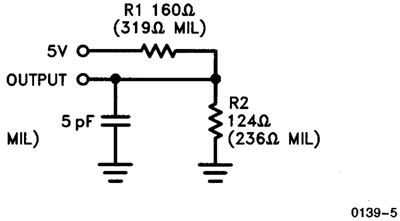
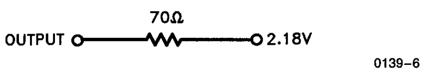
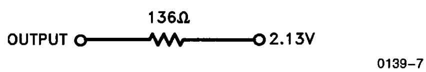


Figure 2b

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



Equivalent to: THÉVENIN EQUIVALENT (Military)



Configuration Table[8]

Table 1

C_3	C_2	C_1	C_0	Configuration
0	0	0	0	Active LOW, Registered Mode, Registered Feedback, Pin 11 OE
0	0	0	1	Active HIGH, Registered Mode, Registered Feedback, Pin 11 OE
0	0	1	0	Active LOW, Combinatorial Mode, Registered Feedback, Pin 11 OE
0	0	1	1	Active HIGH, Combinatorial Mode, Registered Feedback, Pin 11 OE
0	1	0	0	Active LOW, Registered Mode, Registered Feedback, Product Term OE
0	1	0	1	Active HIGH, Registered Mode, Registered Feedback, Product Term OE
0	1	1	0	Active LOW, Combinatorial Mode, Registered Feedback, Product Term OE
0	1	1	1	Active HIGH, Combinatorial Mode, Registered Feedback, Product Term OE
1	0	0	0	Active LOW, Registered Mode, Pin Feedback, Pin 11 OE
1	0	0	1	Active HIGH, Registered Mode, Pin Feedback, Pin 11 OE
1	0	1	0	Active LOW, Combinatorial Mode, Pin Feedback, Pin 11 OE
1	0	1	1	Active HIGH, Combinatorial Mode, Pin Feedback, Pin 11 OE
1	1	0	0	Active LOW, Registered Mode, Pin Feedback, Product Term OE
1	1	0	1	Active HIGH, Registered Mode, Pin Feedback, Product Term OE
1	1	1	0	Active LOW, Combinatorial Mode, Pin Feedback, Product Term OE
1	1	1	1	Active HIGH, Combinatorial Mode, Pin Feedback, Product Term OE

4

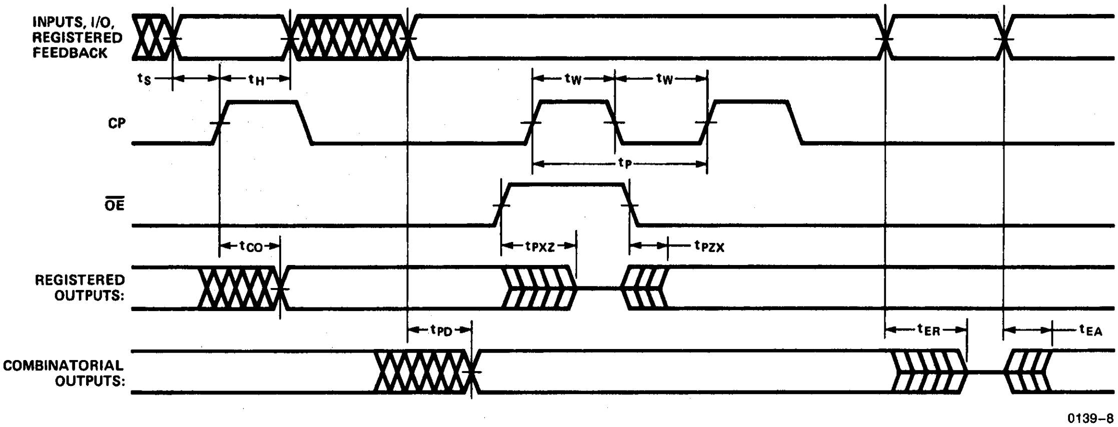
Switching Characteristics PLD C 18G8 Over Operating Range[4, 7, 9]

Parameters	Description	Commercial				Military				Units
		−12		−15, −15L		−15		−20		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		12		15		15		20	ns
t_{EA}	Input to Output Enable		12		15		15		20	ns
t_{ER}	Input to Output Disable		12		15		15		20	ns
t_{PZX}	Pin 11 to Output Enable		10		12		12		15	ns
t_{PXZ}	Pin 11 to Output Disable		10		10		10		15	ns
t_{CO}	Clock to Output		10		12		12		15	ns
t_S	Input or Feedback Setup Time	12		12		15		20		ns
t_H	Hold Time	0		0		0		0		ns
t_P[5]	Clock Period	22		24		27		35		ns
t_{WH}	Clock High Time	7		8		9		10		ns
t_{WL}	Clock Low Time	8		9		10		11		ns
f_{MAX}[6]	Maximum Frequency	45.5		41.6		37.0		28.6		MHz

Notes:

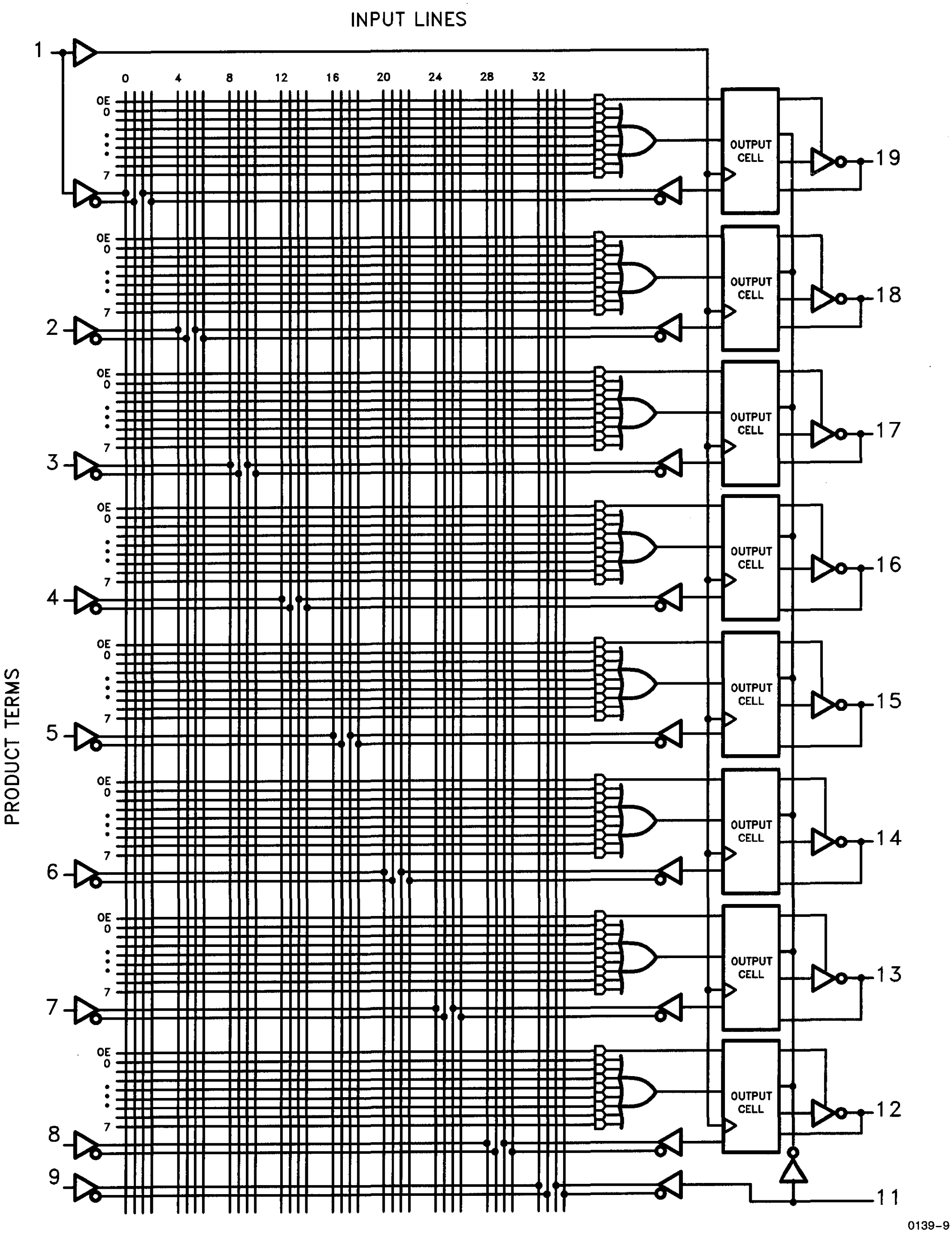
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT} = 0.5V$ has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. *Figure 2a* test load used for all parameters except t_{ER}, t_{PZX} and t_{PXZ}. *Figure 2b* test load used for t_{ER}, t_{PZX} and t_{PXZ}.
5. t_P, minimum guaranteed clock period is that guaranteed for state machine operation and is calculated from $t_P = t_S + t_{CO}$. The minimum guaranteed period for registered data path operation (no feedback) can be calculated as the greater of $(t_{WH} + t_{WL})$ or $(t_S + t_H)$.
6. f_{MAX}, minimum guaranteed operating frequency, is that guaranteed for state machine operation and is calculated from $f_{MAX} = 1/(t_S + t_{CO})$. The minimum guaranteed f_{MAX} for registered data path operation (no feedback) can be calculated as the lower of $1/(t_{WH} + t_{WL})$ or $1/(t_S + t_H)$.
7. T_A is the "instant on" case temperature.
8. In the virgin or unprogrammed state, a configuration bit location is in the "0" state.
9. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to $V_{OH} - 0.5V$ for an enabled HIGH output or $V_{OL} + 0.5V$ for an enabled LOW output.

Switching Waveform



Note:
For more information regarding PLD devices, refer to the Application Brief in the Appendix.

Functional Logic Diagram PLD C 18G8



Ordering Information

I_{CC} (mA)	Speed (ns)	Ordering Code	Package Type	Operating Range
90	12	PLD C 18G8-12PC	P5	Commercial
		PLD C 18G8-12WC	W6	
		PLD C 18G8-12VC	V5	
		PLD C 18G8-12JC	J61	
70	15	PLD C 18G8L-15PC	P5	Commercial
		PLD C 18G8L-15WC	W6	
		PLD C 18G8L-15VC	V5	
		PLD C 18G8L-15JC	J61	
90	15	PLD C 18G8-15PC	P5	Commercial
		PLD C 18G8-15WC	W6	
		PLD C 18G8-15VC	V5	
		PLD C 18G8-15JC	J61	
110	15	PLD C 18G8-15DMB	D6	Military
		PLD C 18G8-15WMB	W6	
		PLD C 18G8-15LMB	L61	
110	20	PLD C 18G8-20DMB	D6	Military
		PLD C 18G8-20WMB	W6	
		PLD C 18G8-20LMB	L61	

Document #: 38-00080-A

PLD C 20G10B/PLD C 20G10

CMOS Generic 24 Pin Reprogrammable Logic Device

Features

- **Fast**
  - **Commercial: t_{PD} = 15 ns, t_{CO} = 10 ns, t_S = 12 ns**
  - **Military: t_{PD} = 20 ns, t_{CO} = 15 ns, t_S = 15 ns**
- **Low power**
  - **I_{CC} max.: 70 mA, Commercial**
  - **I_{CC} max.: 100 mA, Military**
- **Commercial and military temperature range**
- **User-programmable output cells**
  - **Selectable for registered or combinatorial operation**
  - **Output polarity control**
  - **Output enable source selectable from pin 13 or product term**
- **Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2 and 20V8**
- **Eight product terms and one OE product term per output**
- **CMOS EPROM technology for reprogrammability**
- **Highly reliable**
  - **Uses proven EPROM technology**
  - **Fully AC and DC tested**
  - **Security feature prevents logic pattern duplication**
  - **>2000V input protection for electrostatic discharge**
  - **±10% power supply voltage and higher noise immunity**

Functional Description

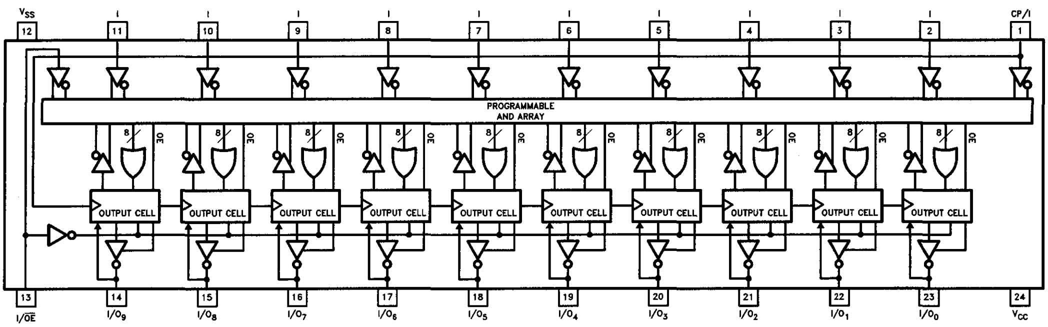
Cypress PLD devices are high speed electrically programmable Logic Devices. These devices utilize the sum of products (AND-OR) structure providing users the ability to program custom logic functions for unique requirements.

In an unprogrammed state the AND gates are connected via EPROM cells to both the true and complement of every input. By selectively programming the EPROM cells, AND gates may be connected to either the true or complement or disconnected from both true and complement inputs.

Cypress PLD C 20G10 uses an advanced 0.8 micron CMOS technology and a proven EPROM cell as the pro-

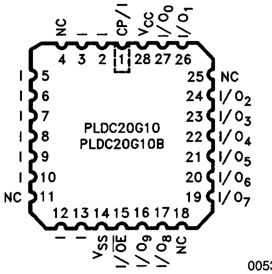
Logic Symbol

20G10



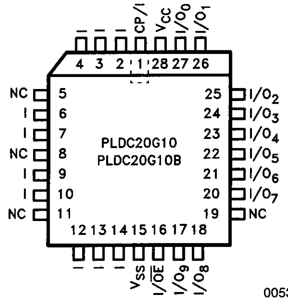
0053-15

LCC Pinout



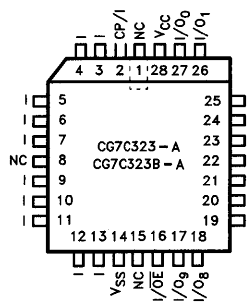
0053-17

STD PLCC Pinout



0053-26

JEDEC PLCC Pinout[16]



0053-41

Selection Guide

Generic Part Number	I_{CC}			t_{PD}		t_S		t_{CO}	
	L	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
20G10B-15	—	70	—	15	—	12	—	10	—
20G10B-20	—	70	100	20	20	12	15	12	15
20G10B-25	—	—	100	—	25	—	18	—	15
20G10-25	—	55	—	25	—	15	—	15	—
20G10-30	—	—	80	—	30	—	20	—	20
20G10-35	—	55	—	35	—	30	—	25	—
20G10-40	—	—	80	—	40	—	35	—	25

Functional Description (Continued)

grammable element. This technology and the inherent advantage of being able to program and erase each cell enhances the reliability and testability of the circuit. This reduces the burden on the customer to test and to handle rejects.

A preload function allows the registered outputs to be preset to any pattern during testing. Preload is important for testing the functionality of the Cypress PLD device.

20G10 Functional Description

The PLD C 20G10 is a generic 24 pin device that can be programmed to logic functions which include but are not limited to: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2 and 20V8. Thus, the PLD C 20G10 provides significant design, inventory and programming flexibility over dedicated 24 pin devices. It is executed in a 24 pin 300 mil molded DIP and a 300 mil windowed Cerdip. It provides up to 22 inputs and 10 outputs. When the windowed CERDIP is exposed to UV light, the 20G10 is erased and then can be reprogrammed.

The Programmable Output Cell provides the capability of defining the architecture of each output individually. Each of the 10 output cells may be configured with "REGISTERED" or "COMBINATORIAL" outputs, "ACTIVE HIGH" or "ACTIVE LOW" outputs, and "PRODUCT TERM" or "PIN 13" generated output enables. Three Architecture Bits determine the configurations as shown in Table 1 and in *Figures 2* through *9*. A total of eight different configurations are possible, with the two most common shown in *Figure 4* and *Figure 6*. The default or unprogrammed state is REGISTERED/ACTIVE LOW/PRODUCT TERM OE as shown in *Figure 2*. The entire Programmable Output Cell is shown in *Figure 1*.

The architecture bit 'C1' controls the REGISTERED/COMBINATORIAL option. In the "COMBINATORIAL" configuration, the output can serve as an I/O pin, or if the output is disabled, as an input only. Any unused inputs should be tied to ground. In the "REGISTERED" configuration, the output of the register is fed back to the array. This allows the creation of control-state machines by providing the next state. The register is clocked by the signal from Pin 1. The register is initialized on power up to Q output LOW and $\overline{Q}$ output HIGH.

In both the Combinatorial and Registered configurations, the source of the "OUTPUT ENABLE" signal can be individually chosen with architecture bit 'C2'. The OE signal may be generated within the array, or from the external $\overline{OE}$ pin (Pin 13). The Pin 13 allows direct control of the outputs, hence having faster enable/disable times.

Each output cell can be configured for "OUTPUT POLARITY". The output can be either Active HIGH or Active LOW. This option is controlled by architecture bit 'CO'.

Along with this increase in functional density, the Cypress PLD C 20G10 provides lower power operation through the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. The phantom array allows the 20G10 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PLD C 20G10 at incoming inspection before committing the device to a specific function through programming.

Programmable Output Cell

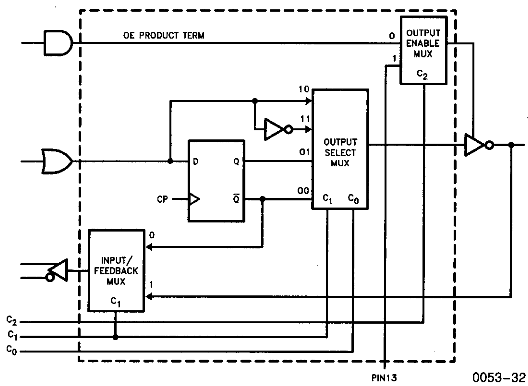


Figure 1

Configuration Table

Table 1

Figure	C_2	C_1	C_0	Configuration
2	0	0	0	Product Term OE/Registered/Active LOW
3	0	0	1	Product Term OE/Registered/Active HIGH
6	0	1	0	Product Term OE/Combinatorial/Active LOW
7	0	1	1	Product Term OE/Combinatorial/Active HIGH
4	1	0	0	Pin 13 OE/Registered/Active LOW
5	1	0	1	Pin 13 OE/Registered/Active HIGH
8	1	1	0	Pin 13 OE/Combinatorial/Active LOW
9	1	1	1	Pin 13 OE/Combinatorial/Active HIGH

Registered Output Configurations

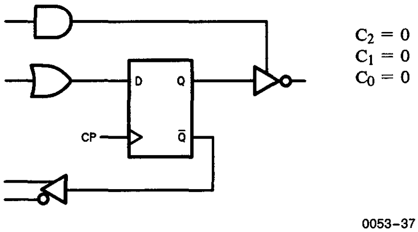


Figure 2. Product Term OE/Active LOW

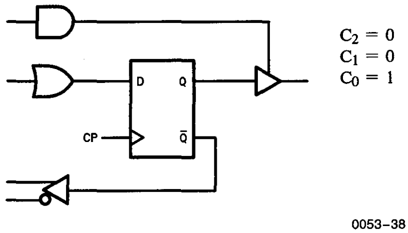


Figure 3. Product Term OE/Active HIGH

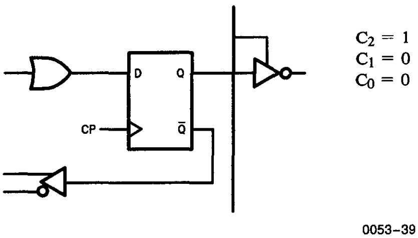


Figure 4. Pin 13 OE/Active LOW

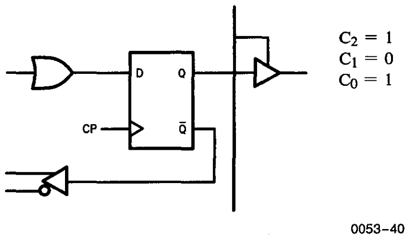


Figure 5. Pin 13 OE/Active HIGH

Combinatorial Output Configurations[5]

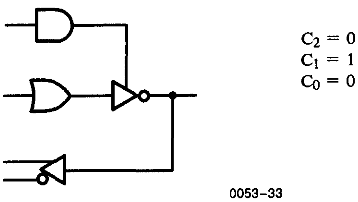


Figure 6. Product Term OE/Active LOW

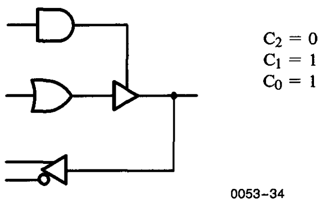


Figure 7. Product Term OE/Active HIGH

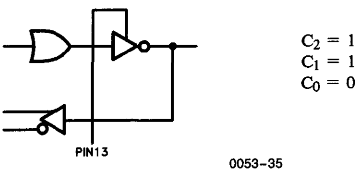


Figure 8. Pin 13 OE/Active LOW

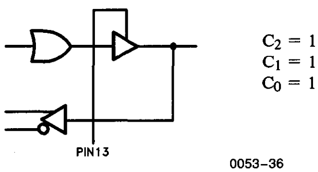


Figure 9. Pin 13 OE/Active HIGH

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 16 mA

DC Programming Voltage
- PLD C 20G10B and CG7C323B-A 13.0V
- PLD C 20G10 and CG7C323-A 14.0V

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[7]	−55°C to +125°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)[6]

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -3.2$ mA	COM'L/IND	2.4		V
			$I_{OH} = -2$ mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 16$ mA	COM'L/IND		0.5	V
			$I_{OL} = 12$ mA	Military			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH[1] Voltage for all Inputs			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW[1] Voltage for all Inputs				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$			−10	10	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]				−90	mA
I_{CC}	Power Supply Current	$0 \leq V_{IN} \leq V_{CC}$ V_{CC} = Max., I_{OUT} = 0 mA Unprogrammed Device	COM'L/IND -15, -20			70	mA
			COM'L/IND -25, -35			55	
			Military -20, -25			100	
			Military -30, -40			80	
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$			−100	100	μA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C, f = 1\ MHz$	4	pF
C_{OUT}	Output Capacitance	$V_{IN} = 0, V_{CC} = 5.0V$	7	

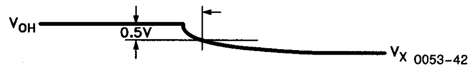
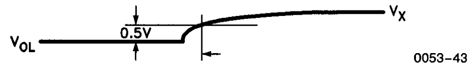
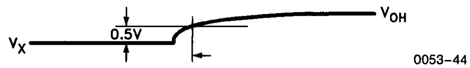
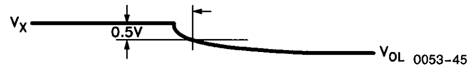
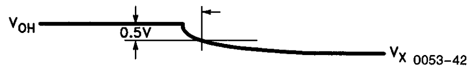
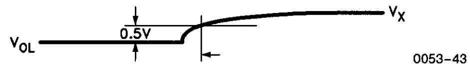
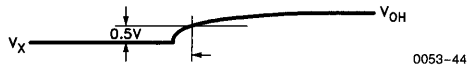
Switching Characteristics PLD C 20G10 Over Operating Range[4, 6]

Parameters	Description	Commercial								Military								Units
		B-15		B-20		-25		-35		B-20		B-25		-30		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[14]		15		20		25		35		20		25		30		40	ns
t_{EA}	Input to Output Enable Delay		15		20		25		35		20		25		30		40	ns
t_{ER}	Input to Output Disable Delay[9]		15		20		25		35		20		25		30		40	ns
t_{PZX}	$\overline{OE}$ Input to Output Enable Delay		12		15		20		25		17		20		25		25	ns
t_{PZX}	$\overline{OE}$ Input to Output Disable Delay		12		15		20		25		17		20		25		25	ns
t_{CO}	Clock to Output Delay[14]		10		12		15		25		15		15		20		25	ns
t_S	Input or Feedback Setup Time	12		12		15		30		15		18		20		35		ns
t_H	Input Hold Time	0		0		0		0		0		0		0		0		ns
t_P	External Clock Period ($T_{CO} + t_S$)	22		24		30		55		30		33		40		60		ns
t_{WH}	Clock Width HIGH[3,8]	8		10		12		17		12		14		16		22		ns
t_{WL}	Clock Width LOW[3,8]	8		10		12		17		12		14		16		22		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	45.4		41.6		33.3		18.1		33.3		30.3		25.0		16.6		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[11]	62.5		50.0		41.6		29.4		41.6		35.7		31.2		22.7		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[12]	66.6		45.4		35.7		20.8		33.3		32.2		28.5		18.1		MHz
t_{CF}	Register Clock to Feedback Input[13]		3.0		10		13		18		13		13		15		20	ns

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT} = 0.5V$ has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. *Figure 11a* test load used for all parameters except t_{ER}, t_{PZX} and t_{PXZ}. *Figure 11b* test load used for t_{ER}, t_{PZX} and t_{PXZ}. See *Figure 10* for waveforms.
5. Bidirectional I/O configurations are possible only when the combinatorial output option is selected.
6. See the last page of this specification for Group A subgroup testing information.
7. T_A is the "instant on" case temperature.
8. Tested by periodically sampling production product.
9. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous high level has fallen to 0.5 volts below V_{OH} Min. or a previous low level has risen to 0.5 volts above V_{OL} Max. Please see *Figure 10* for enable and disable waveforms and measurement reference levels.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feed back can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feed back can operate. This parameter is tested periodically by sampling production product.
13. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see note 12 above) minus t_S.
14. This specification is guaranteed for all device outputs changing state in a given access cycle.

Test Waveforms

Parameter	V_X	Output Waveform—Measurement Level
$t_{PXZ}(-)$	1.5V	
$t_{PXZ}(+)$	2.6V	
$t_{PZX}(+)$	V_{thc}	
$t_{PZX}(-)$	V_{thc}	
$t_{ER}(-)$	1.5V	
$t_{ER}(+)$	2.6V	
$t_{EA}(+)$	V_{thc}	
$t_{EA}(-)$	V_{thc}	

AC Test Loads and Waveforms (Commercial)

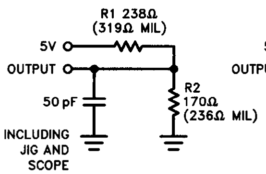


Figure 11a

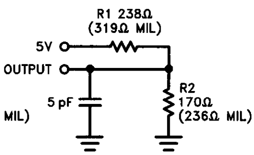
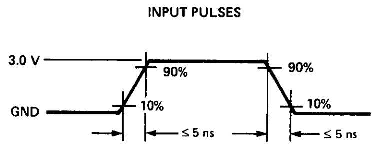


Figure 11b

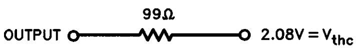
0053-6



0053-8

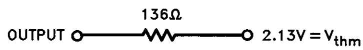
Figure 12

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



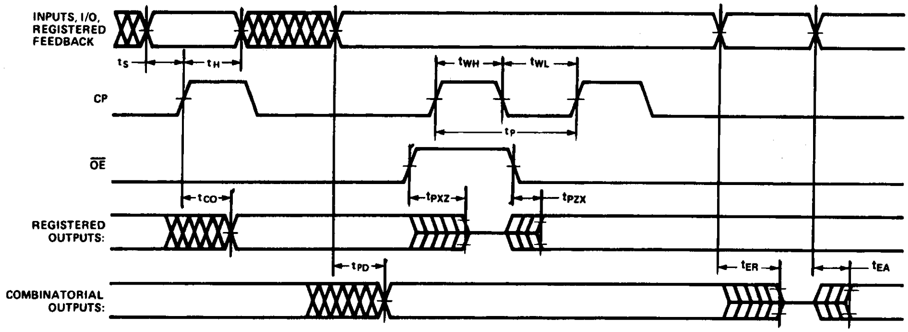
0053-7

Equivalent to: THÉVENIN EQUIVALENT (Military)



0053-24

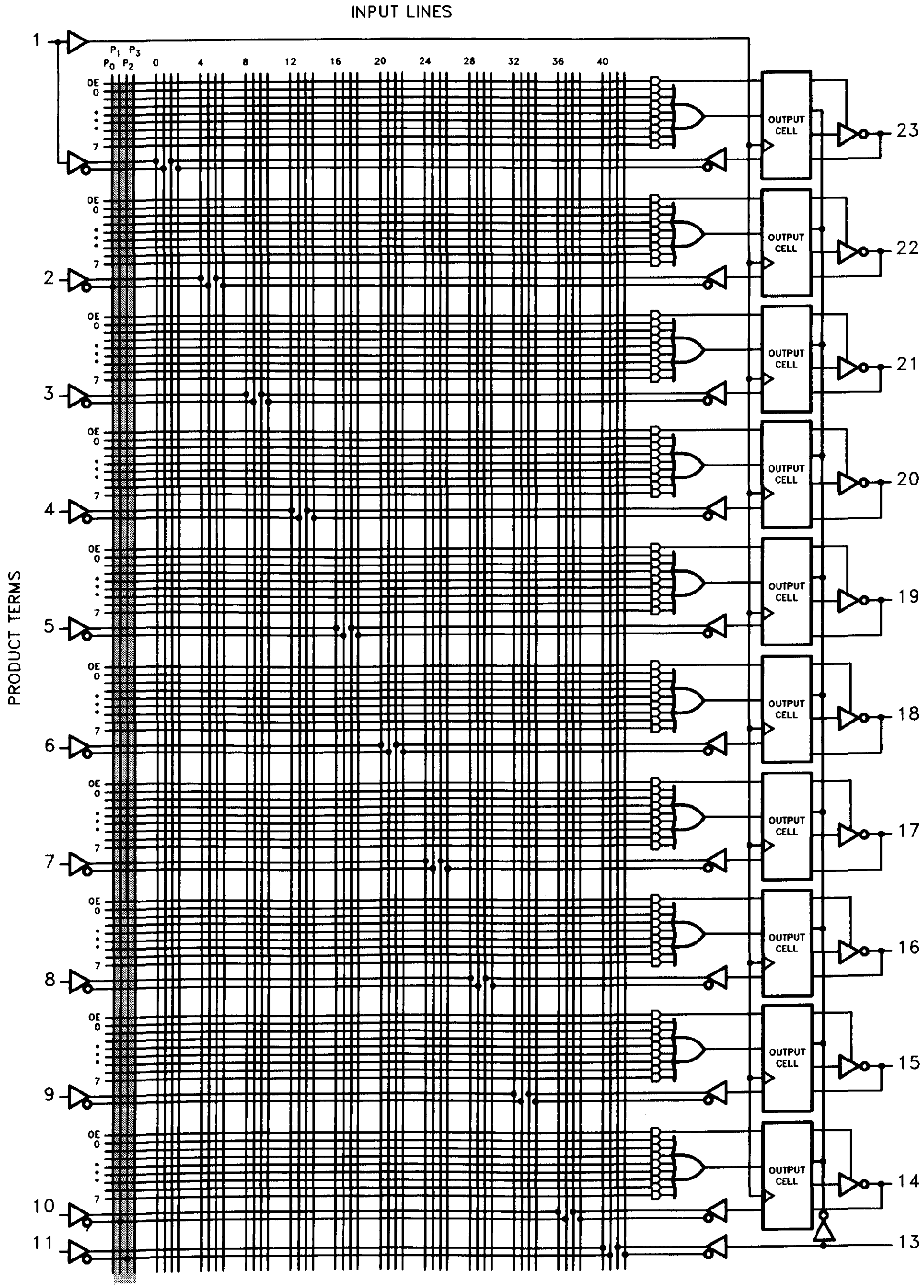
Switching Waveforms



0053-9

Note:
For more information regarding PLD devices, refer to the Application Brief in the Appendix.

Functional Logic Diagram PLD C 20G10



0053–23

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PLD C 20G10. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs which may cause "blank" check failures or "verify errors" when programming "windowed" parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure would be approximately 35 minutes. The PLD C 20G10 needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Device Programming

The PLD C 20G10 can be programmed on inexpensive conventional PROM/EPROM programmers with appropriate personality or socket adapters and the CY3000 QuickPro programmer. Once the PLD device is programmed, one additional location can be programmed to prohibit logic pattern verification. This security feature gives the user additional protection to safeguard his proprietary logic. This feature is highly reliable and due to EPROM technology it is impossible to visually read the programmed cell locations.

The PLD C 20G10 has multiple programmable functions. In addition to the normal array, a "PHANTOM" array, "TOP and BOTTOM TEST" and a "SECURITY" feature are programmable. The PLD C 20G10 security mechanism, when invoked, prevents access to the "NORMAL" and "TOP/BOTTOM TEST" array. The "PHANTOM" array feature is still accessible, allowing programming and verification of the pattern in the "PHANTOM" array. Functional operation of all other features is allowed regardless of the state of the "SECURITY BIT". In addition, the device contains 10 programmable output cells which are programmed to configure the device functionality for each specific application.

The logic array is divided into a "NORMAL" array and a "PHANTOM" array. The normal array is used to configure the device to perform a specific function as required by the user, and the phantom array is provided as a test array for Cypress' testing the device prior to user programming thus assuring a reliable, thoroughly tested product. The "PHANTOM" array contains four additional columns connected to input pins 2 (TRUE), 7 (INVERTING), 10 (TRUE) and 11 (TRUE). These inputs may be programmed to be connected to all normal product terms. This allows all sense amplifiers and programmable output cells to be exercised for both functionality and performance after assembly and prior to shipment. These features are in addition to the normal array. They do not affect normal operation, allowing the user full programming of the normal array, while allowing the device to be fully tested.

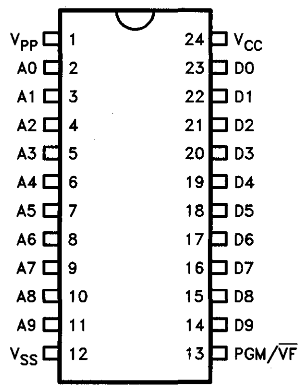
The "TOP TEST" and "BOTTOM TEST" feature, allow connection of all input terms to either pin 23 or 13. These locations may be programmed and subsequently exercised in the "TOP TEST" and "BOTTOM TEST" mode. Like the Phantom array above, this feature has no effect in the normal mode of operation. Cells in the PHANTOM ARRAY, TOP TEST, and BOTTOM TEST areas are programmed at Cypress during the manufacturing operation, and they therefore will be programmed when received in a non-windowed package by the user. Consequently, the user will normally have no need to program these cells.

The architecture bits C_0, C_1 and C_2 are used to configure each programmable output cell individually. C_0 selects output polarity, C_1 selects the combinatorial or registered mode of operation and C_2 selects the source of output enable. If the registered mode of operation is selected, the feedback path is automatically selected to be from the register. In the combinatorial mode the feedback path is automatically selected to be from the I/O pin. In this combinatorial mode, the output from the array may be fed into the array or if the output is deselected using the output enable product term the pin may be used as an external input. There is not a mode where the I/O pin may be used as a combinatorial output or an input pin, while the register is used as a state register. The architecture bits are programmed as a separate item during normal programming. An I/O pin is configured to be an input by programming the output cell into a combinatorial mode and disabling the ouput with the output enable product term.

Pinout

The PLD C 20G10 PROGRAMMING pinout is shown in *Figure 13*. In the Programming pinout configuration, the device may be programmed and verified for the NORMAL mode of operation and also programmed, verified and operated in PHANTOM and TEST modes. These special modes of operation are achieved through the use of supervoltages applied to certain pins. Care should be exercised when entering and exiting these modes, paying specific attention to both the operating modes as specified in Table 1 and the sequencing of the supervoltages as shown in the timing diagrams.

Programming Pinout



0053-27

Figure 13

Programming Algorithm

With the exception of the Security bit, all arrays are programmed in a similar manner. The data to be programmed is represented by a "1" or "0" on the I/O pins. A "1" indicates that an unprogrammed location is to be programmed and a "0" indicates that an unprogrammed location is to remain unprogrammed. All locations to be programmed are addressed as row and column locations. Table 2 "Operating Modes" along with Tables 3 through 6 provide the specific address for each addressed location to be programmed along with mode selection information for both programming and operation in the "PHANTOM" and "TEST" modes.

When programming the security bit, a supervoltage on pin 3 is used as data with a programming pulse on pin 13. Verification is controlled with a supervoltage on pins 4 and the data out on pin 3.

20G10 JEDEC Map

The 20G10 JEDEC Map is organized as follows: the EPROM fuses for the product terms and input lines are located between 0000 and 3959 (decimal). The architecture bits are located between locations 3960 and 3989. Location 3960 is the Polarity Bit (CO), location 3961 is the Registered/Combinatorial Bit (C1), and location 3962 is the Output Enable Bit (C2) for output pin 23. Locations 3963, 3964, and 3965 are the architecture bit locations for output pin 22. This pattern repeats for output pins 21, 20, 19, 18, 17, 16, 15, and 14.

Operating Modes

Table 2 describes the operating and programming modes of the PLD C 20G10. The majority of the programming modes function with a PROGRAM, PROGRAM INHIBIT and PROGRAM VERIFY sequence. The exception is the Security Program operation, which shows no program inhibit function. Two timing diagrams are provided for these two different methodologies of programming in *Figures 15 & 16.* Tables 3 through 6 are used as indicated to provide the individual addresses of the various arrays and cells to be programmed. There are 5 operating modes in addition to the programming modes for the PAL C 22V10. These provide NORMAL operation, PHANTOM operation, TOP TEST, BOTTOM TEST and a register preload feature for testing.

In the normal operating mode, all signals are TTL levels and the device functions as it is internally programmed in the NORMAL array. In the PHANTOM mode of operation, the device operates logically as a function of the contents of the PHANTOM array. In this mode pins 2, 10 & 11 are non-inverting inputs and pin 7 is an inverting input. The programmable output cells function as they are programmed for normal operation. If the programmable output cells have not yet been programmed, they are in a registered inverting configuration. The PHANTOM mode is invoked by placing a supervoltage V_{PP} on pin 6. Care should be exercised when entering and leaving this mode that the supervoltage is applied no sooner than 20 ms after the V_{CC} is stable, and removed a minimum of 20 ms before V_{CC} is removed.

TOP and BOTTOM TEST

The TOP TEST and BOTTOM TEST modes are entered and exited in the same manner, with the same concern for power sequencing, but the supervoltage is applied to pins 9 & 10 respectively. In these modes an extra product term controls an output pin. TOP TEST controls pin 23, and BOTTOM TEST controls pin 14. These product terms are controlled by the normal device inputs, and allow testing of all input structures.

Preload

Finally for testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage V_{PP}, which puts the output drivers in a high impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A "0" on the I/O pin preloads the register with a "0" and a "1" preloads the register with a "1". The actual signal on the output pin will be the inversion of the input data. The data on the I/O pins is then removed, and pin 8 returned to a normal TTL voltage. Again care should be exercised to power sequence the device properly.

Operating Modes

Table 2

Operating Modes: Feature	Function	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 17	Pin 20	Pins 15, 16, 18, 19, 21 & 22	Pin 23
Main Array Product	Program	V_{PP}											V_{PP}	Data In				
	Program Inhibit	V_{PP}	Table 3						Table 4				V_{IHP}	High Z				
	Program Verify[3]	V_{PP}											V_{ILP}	Data Out				
Output Enable Product Terms	Program	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}	Table 3						V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	Data Out				
Top Test, Bottom Test Notes	Program	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	Data In	Data In	Data In	V_{ILP}	Data In
	Program Inhibit	V_{PP}	Table 3						V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	High Z	High Z	High Z	High Z	High Z
	Program Verify	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	Data Out	Data Out	Data Out	Driven	Data Out
Architecture Bits	Program	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}			V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	Table 5		V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}			V_{PP}	V_{ILP}	Data Out				
Security Bit	Program	V_{PP}	V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
	Verify	V_{ILP}	V_{ILP}	Data Out	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	Driven Outputs				
PAL Mode Operation	Normal	CP/I	I	I	I	I	I	I	I	I	I	I	I	I/O				
	Phantom	CP/I	I	NA	NA	NA	V_{PP}	I	NA	NA	I	I	NA	Output				
	Top Test	I	I	I	I	I	I	I	I	V_{PP}	I	I	I	NA				Out
	Bottom Test	I	I	I	I	I	I	I	I	I	V_{PP}	I	I	Out	NA			
	Reg Preload	Notes	NA	NA	NA	NA	NA	NA	V_{PP}	NA	NA	NA	V_{ILP}	Data In				
Phantom Array Product Terms	Program	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}					V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{ILP}	V_{ILP}	Table 6		V_{ILP}	V_{PP}	Table 4				V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}					V_{ILP}	Data Out				
Phantom Output Enable Product Terms	Program	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{ILP}	V_{ILP}	Table 6		V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{ILP}	V_{IL}			V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	Data Out				

Notes:

1. DATA IN and DATA OUT for programming Synchronous Set, Asynchronous Reset, TOP TEST and BOTTOM TEST is programmed and verified on the following pins.
   Pin 14 = BOTTOM TEST
   Pin 17 = Synchronous Set
   Pin 20 = Asynchronous Reset
   Pin 23 = TOP TEST
2. The preload clock on pin 1 loads the Registers on a LOW going HIGH transition.
3. It is necessary to toggle $\overline{OE}$ (Pin 13) HIGH during all address transitions while in the program verify/blank check mode.

Input Term Addresses

Table 3 is used during the programming and verification of the main array, output enable, asynchronous reset, synchronous preset, TOP and BOTTOM TEST as shown in Table 2. It provides the addressing for the 44 normal input term columns which are connected with an EPROM transistor to the product terms.

Input Term Addresses

Table 3

Input Term	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
8	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
9	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
11	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
12	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
13	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
15	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
16	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
17	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
18	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
19	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
20	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
21	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
22	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
23	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
24	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
25	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
26	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
27	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
28	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
29	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
30	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
31	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
32	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
33	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
34	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
35	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
36	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
37	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
38	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
39	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
40	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
41	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
42	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
43	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}

Product Term Addresses

Table 4 is used for the programming of the "PHANTOM" and normal array. It provides the addressing for the 8 product terms associated with each input.

Product Term Addresses

Table 4

Product Term	Pin 8	Pin 9	Pin 10	Pin 11
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}

Architecture Bit Addressing

Table 5 provides the addressing for the architecture bits used to control the configuration of the individual Programmable Output Cells. In the unprogrammed state, the Programmable Output Cells are in a registered, active low or inverting configuration with output enable controlled from the product term. They are programmed with a "1" on the pin associated with the Programmable Output Cells and the appropriate address as shown in Table 5. Each architecture bit that is not to be programmed, requires a "0" on the I/O pin associated with the Programmable Output Cells.

Architecture Bit Addressing

Table 5

Architecture Bit	Pin 9	Pin 10
Output Polarity C0	V_{ILP}	V_{ILP}
Register/ Combinatorial Output C1	V_{IHP}	V_{ILP}
Product Term/ Pin 13 Output Enable C2	V_{ILP}	V_{IHP}

Phantom Input Term Addressing

Phantom input terms are addressed as columns P0 thru P3 and represent inputs from pins 2, 7, 10 and 11 respectively. Pin 7 is inverted, and the remaining 3 are normal non-inverting. This PHANTOM array allows the output structures to be tested. They are only present in PHANTOM modes of operation.

Phantom Input Term Addresses

Table 6

Phantom Input Term	Pin 4	Pin 5
P0	V_{ILP}	V_{ILP}
P1	V_{IHP}	V_{ILP}
P2	V_{ILP}	V_{IHP}
P3	V_{IHP}	V_{IHP}

Programming Flow Chart

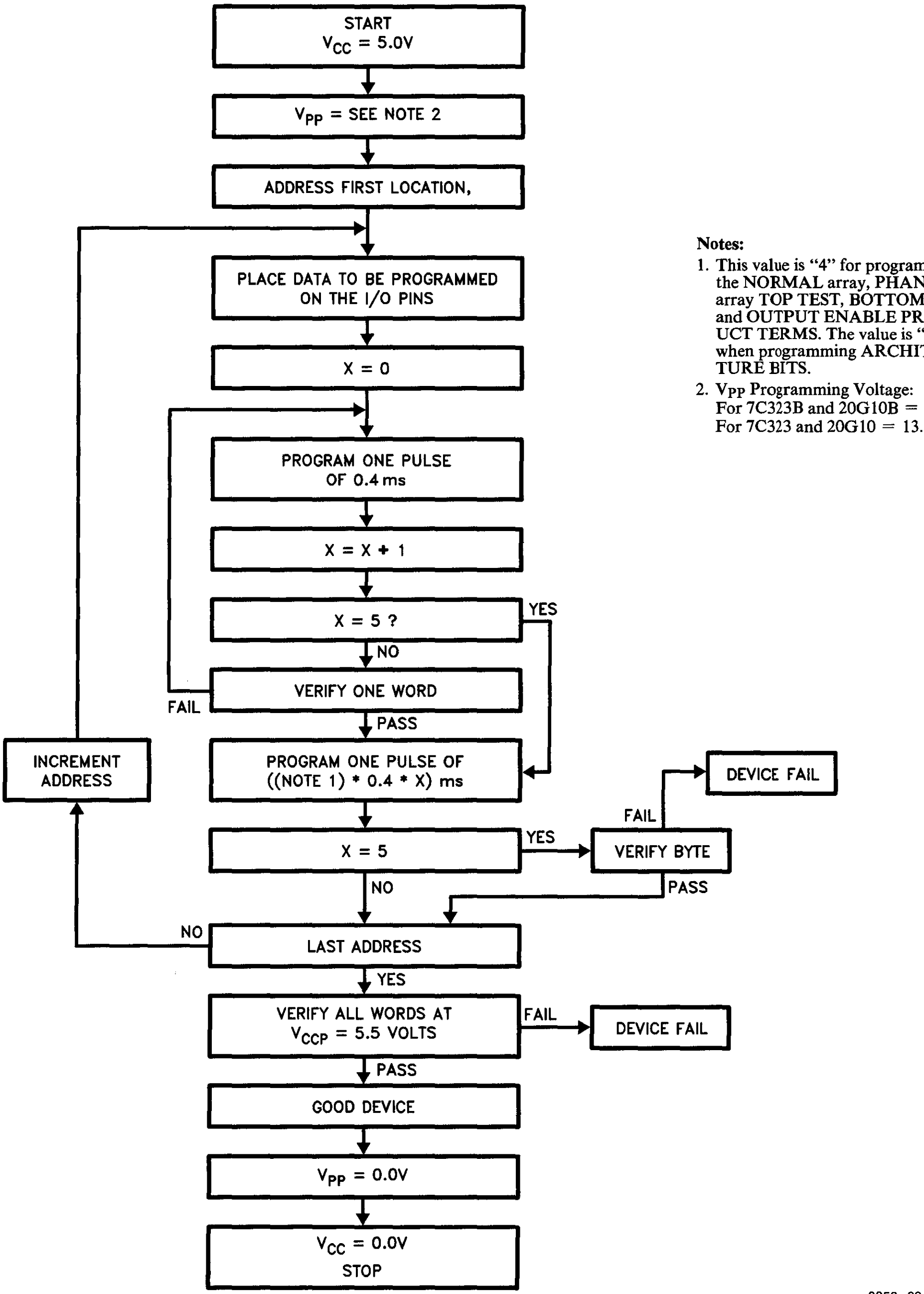
The programming flow chart describes the sequence of operations for programming the NORMAL and PHANTOM arrays, the NORMAL and PHANTOM output enable product terms, the set and preset product terms, the Top Test product term, the Bottom Test product term, and the architecture bits. The exact sequencing and timing of the signals is shown in the "Array Programming Timing Diagram".

The logical sequence to program the device is described in detail in the flow chart below, and should be followed exactly for optimum intelligent programming that both minimizes programming time and realizes reliable programming. Particular attention should be paid to the application of V_{CC} prior to V_{PP}, and removal of V_{PP} prior to V_{CC}. See *Figure 14* and Table 8 for specific timing and AC requirements. Notice that all programming is accomplished without switching V_{PP} on pin 1 and that after programming and verifying all locations individually, the programmed locations should be verified one final time.

The normal word programming cycle, programs and verifies a word at a time as shown in the programming flowchart, *Figure 13* and timing diagram *Figure 14.* After all locations are programmed, the flowchart requires a verify of all words. There is no independent timing diagram for this operation, rather *Figure 14* also provides the correct timing information for this operation. When performing this verify only operation, eliminate the program portion of the cycle but maintain the setup and hold timing relative to the verify pulse. Under no circumstances should the verify signal be held low and the addresses toggled.

Note that the overprogram pulse in step 10 of the programming flowchart is a variable, "4" times the initial value when programming the NORMAL, PHANTOM, TOP TEST, BOTTOM TEST and OUTPUT ENABLE product terms and "8" times the initial value when programming the ARCHITECTURE BITS.

Programming Flowchart



Notes:

1. This value is "4" for programming the NORMAL array, PHANTOM array TOP TEST, BOTTOM TEST and OUTPUT ENABLE PRODUCT TERMS. The value is "8" when programming ARCHITECTURE BITS.
2. V_{PP} Programming Voltage:
   For 7C323B and 20G10B = 12.5V
   For 7C323 and 20G10 = 13.5V.

Figure 14

4

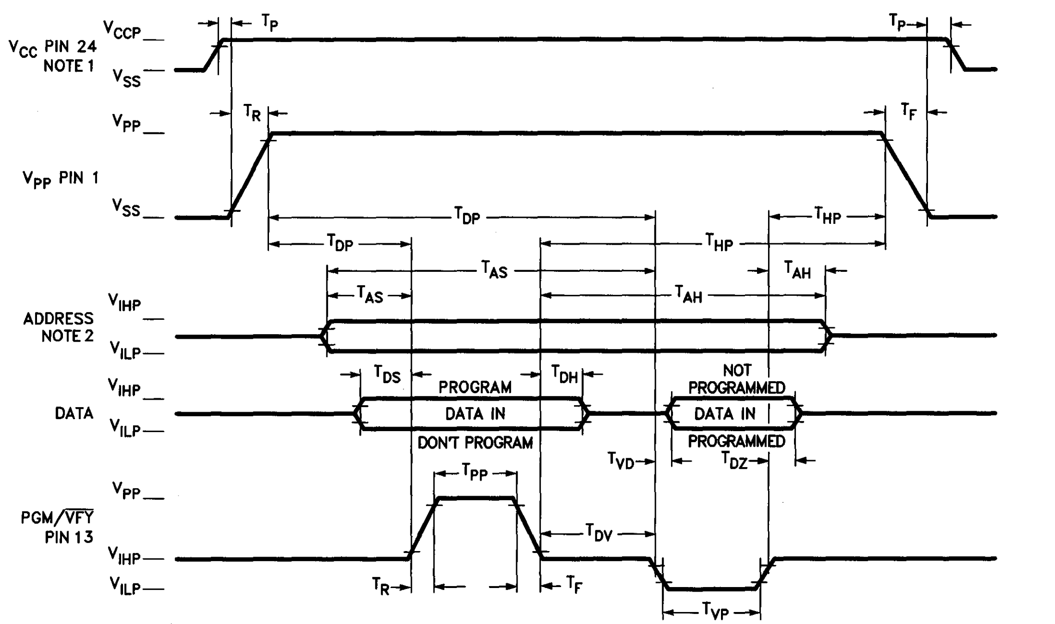
Timing Diagrams

Programming timing diagrams are provided for two cases, programming of all cells except the SECURITY BIT and programming the SECURITY BIT.

Array

Programming the NORMAL and PHANTOM arrays and output enables, reset, preset, architecture bits and the top/bottom test features uses the timing diagram in *Figure 15.* ADDRESS refers to all applicable information in Tables 2 through 6 that is not specifically referenced in the timing diagram. DATA IN is provided on the I/O pins and DATA OUT is verified on the same pins. A "1" (V_{IHP}) on an I/O pin causes the addressed location to be programmed. A "0" on the I/O pin leaves the addressed location to be unprogrammed. All setup hold and delay times must be met, and in particular the sequence of operations should be strictly followed. During verify only operation it is not acceptable to hold PGM/VFY low and sequence addresses, as it violates address setup and hold times. Proper sequencing of all power and supervoltages is essential, to reliable programming of the device as improper sequencing could result in device damage.

Programming Waveforms



Notes:

1. Power, V_{PP} & V_{CC} should not be cycled for each program/verify cycle, but may remain static during programming.
2. For programming $\overline{OE}$ Product Terms & Architecture bits, Pin 11 (A9) must go to V_{PP} and satisfy T_{AS} and T_{AN}.

Figure 15

Security Cell

The security cell is programmed independently per the timing diagram in *Figure 16,* and the information in Table 2. Note again that proper sequencing of power and programming signals is required. Data in is represented as a supervoltage on pin 3 and verified as a TTL signal output on the same pin. A "0" on pin 3 indicates that the security bit has been programmed, and a "1" indicates that security bit has not been programmed. Security is programmed with a single 50 ms pulse on pin 13. A supervoltage on pin 4 is used to verify security after V_{PP} has been removed from pin 1.

Programming Waveforms Security Cell

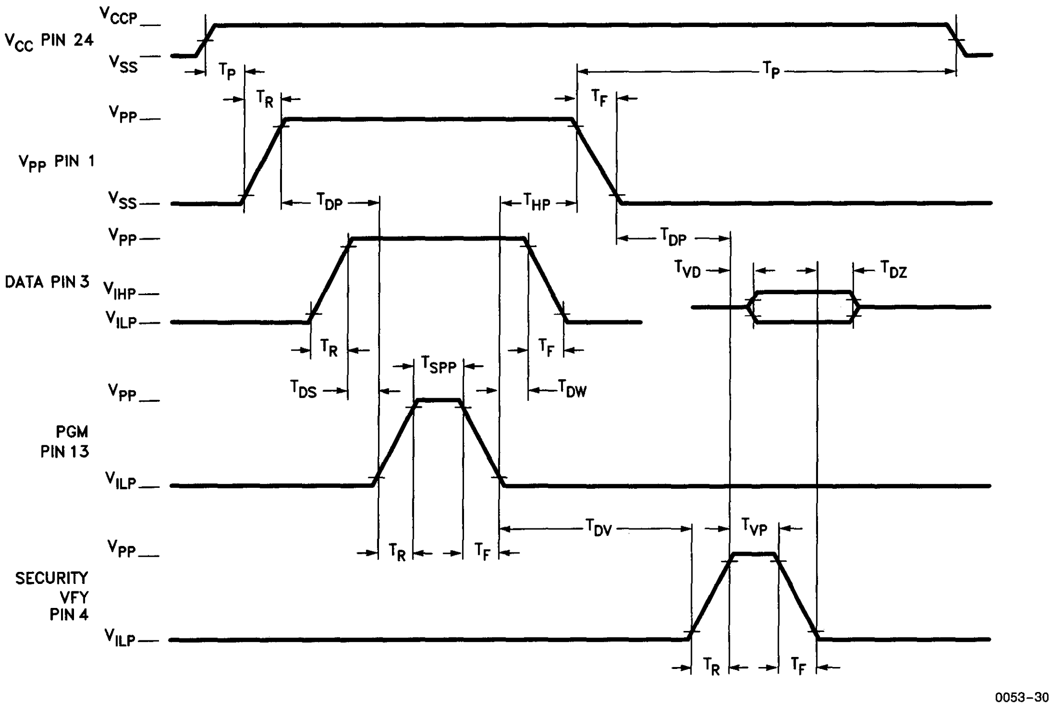


Figure 16

DC Programming Parameters $T_A = 25°C$

Table 7

Parameter	Description	Min.	Max.	Units
V_{PP} for PLD C 20G10B and for CG7C323B-A	Programming Voltage	12.0	13.0	Volts
V_{PP} for PLD C 20G10 and for CG7C323-A	Programming Voltage	13.0	14.0	Volts
V_{CCP}	Supply Voltage During Programming	4.75	5.25	Volts
V_{IHP}	Input HIGH Voltage During Programming	3.0	V_{CCP}	Volts
V_{ILP}	Input LOW Voltage During Programming	−3.0	0.4	Volts
V_{OH}	Output HIGH Voltage	2.4		Volts
V_{OL}	Output LOW Voltage		0.4	Volts
I_{PP}	Programming Supply Current		40	mA

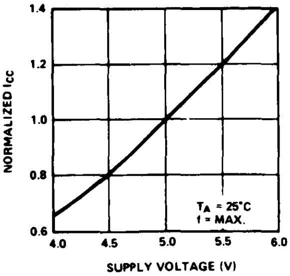
AC Programming Parameters

Table 8

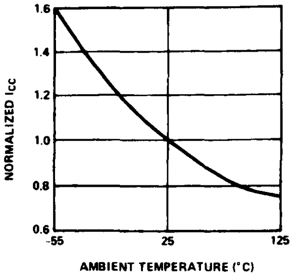
Parameter	Description	Min.	Max.	Units
T_P	Delay to Programming Voltage	20		ms
T_{DP}	Delay to Program	1		μs
T_{HP}	Hold from Program or Verify	1		μs
$T_{R,F}$	V_{PP} Rise & Fall Time	50		ns
T_{AS}	Address Setup Time	1		μs
T_{AH}	Address Hold Time	1		μs
T_{DS}	Data Setup Time	1		μs
T_{DH}	Data Hold Time	1		μs
T_{PP}	Programming Pulsewidth	0.4	10	ms
T_{SPP}	Programming Pulsewidth for Security	50		ms
T_{DV}	Delay from Program to Verify	2		μs
T_{VD}	Delay to Data Out		1	μs
T_{VP}	Verify Pulse Width	2		μs
T_{DZ}	Verify to High Z		1	μs

Typical DC and AC Characteristics

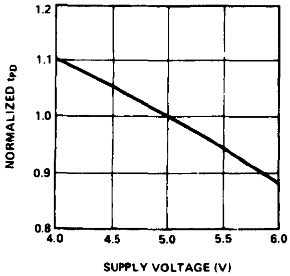
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



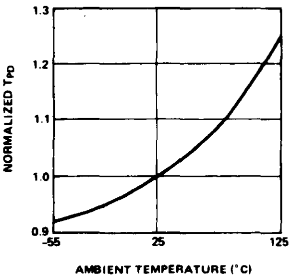
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



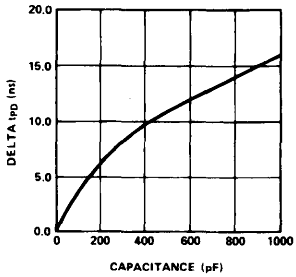
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



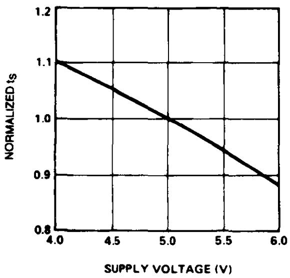
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



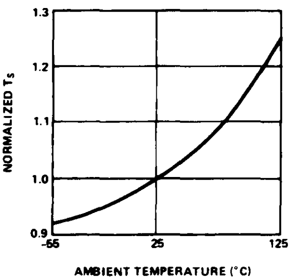
DELTA PROPAGATION TIME vs. OUTPUT LOADING



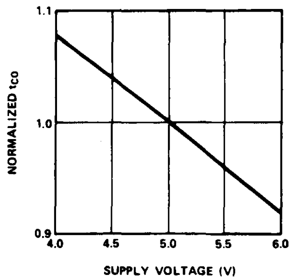
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



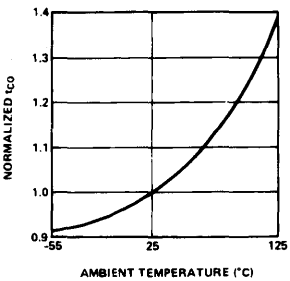
NORMALIZED SETUP TIME vs. TEMPERATURE



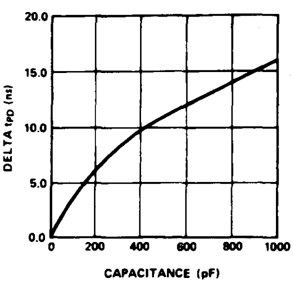
NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



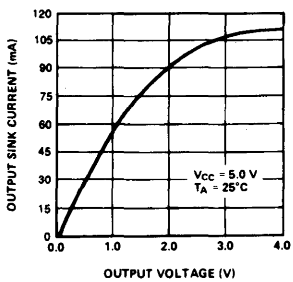
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



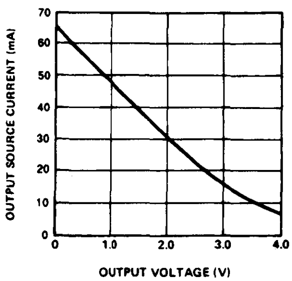
DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



0053–31

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	I_{CC} (mA)	Ordering Code	Package	Operating Range
15	12	10	70	PLD C 20G10B-15PC/PI	P13	Commercial/ Industrial
				PLD C 20G10B-15WC/WI	W14	
				PLD C 20G10B-15JC/JI*	J64	
				PLD C 20G10B-15HC	H64	
				CG7C323B-A15JC/JI[15]	J64	
				CG7C323B-A15HC	H64	
20	12	12	70	PLD C 20G10B-20PC/PI	P13	Commercial/ Industrial
				PLD C 20G10B-20WC/WI	W14	
				PLD C 20G10B-20JC/JI	J64	
				PLD C 20G10B-20HC	H64	
				CG7C323B-A20JC/JI[15]	J64	
				CG7C323B-A20HC	H64	
20	15	15	100	PLD C 20G10B-20DMB	D14	Military
				PLD C 20G10B-20WMB	W14	
				PLD C 20G10B-20LMB	L64	
25	15	15	55	PLD C 20G10-25PC/PI	P13	Commercial/ Industrial
				PLD C 20G10-25WC/WI	W14	
				PLD C 20G10-25JC/J1	J64	
				PLD C 20G10-25HC	H64	
				CG7C323-A25JC/J1[15]	J64	
				CG7C323-A25HC	H64	
25	18	15	100	PLD C 20G10B-25DMB	D14	Military
				PLD C 20G10B-25WMB	W14	
				PLD C 20G10B-25LMB	L64	
30	20	20	80	PLD C 20G10-30DMB	D14	Military
				PLD C 20G10-30WMB	W14	
				PLD C 20G10-30LMB	L64	
35	30	25	55	PLD C 20G10-35PC/PI	P13	Commercial/ Industrial
				PLD C 20G10-35WC/WI	W14	
				PLD C 20G10-35JC/JI	J64	
				PLD C 20G10-35HC	H64	
				CG7C323-A35JC/JI[15]	J64	
				CG7C323-A35HC	H64	
40	35	25	80	PLD C 20G10-40DMB	D14	Military
				PLD C 20G10-40WMB	W14	
				PLD C 20G10-40LMB	L64	

Note:

15. The CG7C323 is the PLDC20G10 packaged in the JEDEC compatible 28 pin PLCC pinout. Pin function and pin order is identical for both PLCC pinouts. The principle difference is in the location of the "no connect" or NC pins.

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
V_{PP}	1,2,3
I_{CC}	1,2,3
I_{OZ}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7,8,9,10,11
t_{PZX}	7,8,9,10,11
t_{CO}	7,8,9,10,11
t_S	7,8,9,10,11
t_H	7,8,9,10,11

Document #: 38-00019-D

CYPRESS SEMICONDUCTOR

Reprogrammable Asynchronous CMOS Logic Device

Features

- Advanced user programmable macro cell
- CMOS EPROM technology for reprogrammability
- Up to 20 input terms
- 10 programmable I/O macro cells
- Output macro cell programmable as combinatorial or asynchronous D-type registered output
- Product term control of register clock, reset and set and output enable
- Register preload and power-up reset
- Four uncommitted product terms per output macro cell
- Fast
  - Commercial
    t_{PD} = 20 ns
    t_{CO} = 20 ns
    t_{SU} = 10 ns
  - Military
    t_{PD} = 25 ns
    t_{CO} = 25 ns
    t_{SU} = 15 ns
- Low power
  - I_{CC} max = 80 mA Commercial
  - I_{CC} max = 100 mA Military
- High reliability
  - Proven EPROM technology
  - $>$2001V input protection
  - 100% programming and functional testing
- Windowed DIP, windowed LCC, DIP, LCC, PLCC available

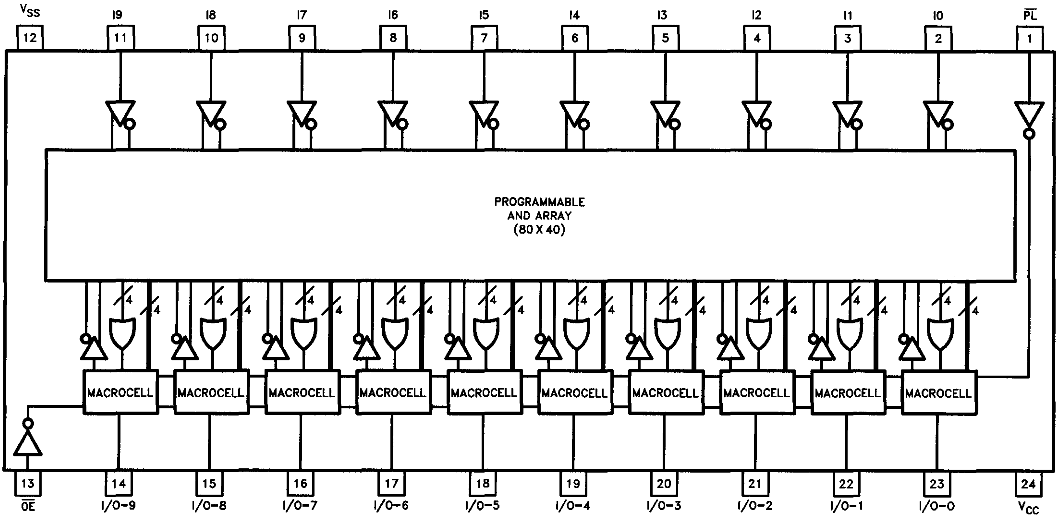
Functional Description

The Cypress PLD C 20RA10 is a high performance, second generation programmable logic device employing a flexible macro cell structure which allows any individual output to be configured independently as a combinatorial output or as a fully asynchronous D-type registered output.

The Cypress PLD C 20RA10 provides lower power operation with superior speed performance than functionally equivalent bipolar devices through the use of high performance 0.8 micron CMOS manufacturing technology.

The PLD C 20RA10 is packaged in a 24 pin 300 mil molded DIP, a 300 mil windowed cerdip, and a 28 lead square leadless chip carrier and provides up to 20 inputs and 10 outputs. When the windowed device is exposed UV light, the 20RA10 is erased and then can be reprogrammed.

Block Diagram and DIP Pinout



0118-1

Macro Cell Architecture

Figure 1 illustrates the architecture of the 20RA10 macro cell. The cell dedicates three product terms for fully asynchronous control of the register set, reset and clock functions, as well as, one term for control of the output enable function.

The output enable product term output is "AND'ed" with the input from pin 13 to allow either product term or hard wired external control of the output or a combination of control from both sources. If product term only control is selected, it is automatically chosen for all outputs since, for this case, the external output enable pin must be tied LOW. The active polarity of each output may be programmed independently for each output cell and is subsequently fixed. *Figure 2* illustrates the output enable options available.

When an I/O cell is configured as an output, combinatorial only capability may be selected by forcing the set and reset product term outputs to be HIGH under all input conditions. This is achieved by programming all input term programming cells for these two product terms. *Figure 3* illustrates the available output configuration options.

An additional four uncommitted product terms are provided in each output macro cell as resources for creation of user defined logic functions.

Programmable I/O

Because any of the 10 I/O pins may be selected as a input, the device input configuration programmed by the user may vary from a total of nine programmable plus ten dedicated inputs (a total of nineteen inputs) and one output down to a ten input, ten output configuration with all ten programmable I/O cells configured as outputs. Each input pin available in a given configuration is available as an input to the four control product terms and four uncommitted product terms of each programmable I/O macro cell that has been configured as an output.

An I/O cell is programmed as an input by tying the output enable pin, pin 13, HIGH or by programming the output enable product term to provide a LOW, thereby disabling the output buffer, for all possible input combinations.

When utilizing the I/O macro cell as an output, the input path functions as a feedback path allowing the output signal to be fed back as an input to the product term array. When the output cell is configured as a registered output, this feed back path may be used to feed back the current output state to the device inputs to provide current state control of the next output state as required for state machine implementation.

Preload and Power-up Reset

Functional testability of programmed devices is enhanced by inclusion of register preload capability which allows the state of each register to be set by loading each register from an external source prior to exercising the device. Testing of complex state machine designs is simplified by the ability to load an arbitrary state without cycling through long test vector sequences to reach the desired state. Recovery from illegal states can be verified by loading illegal states and observing recovery. Preload of a particular register is accomplished by impressing the desired state on the register output pin and lowering the signal level on the preload control pin (pin 1) to a logic LOW level. If the specified preload set up, hold and pulse width minimums have been observed, the desired state is loaded into the register. To insure predictable system initialization, all registers are preset to a logic LOW state upon power up, thereby setting the active LOW outputs to a logic HIGH.

4

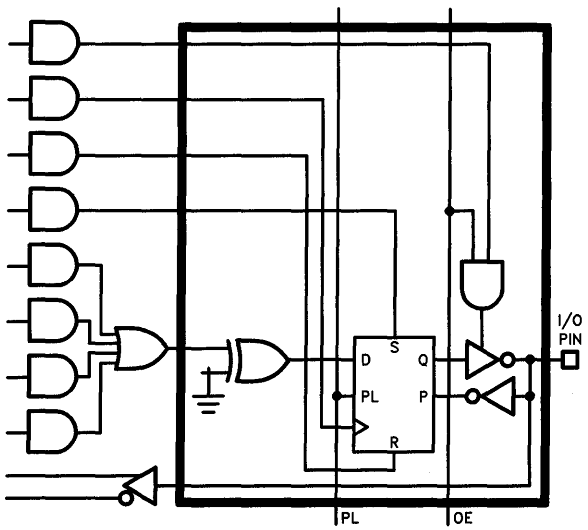
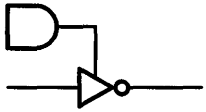


Figure 1. PLD C 20RA10 Macro Cell

Output Always Enabled

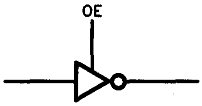
0118-13

Programmable



0118-14

Hard-Wired



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Combination of Programmable and Hard-Wired

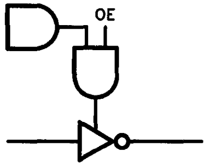

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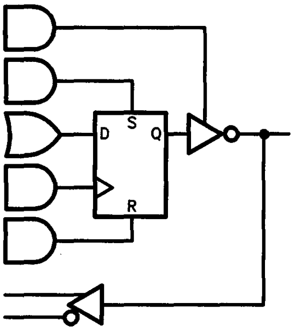
Figure 2. Four Possible Output Enable Alternatives for the PLD C 20RA10

Registered/Active LOW



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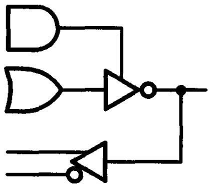
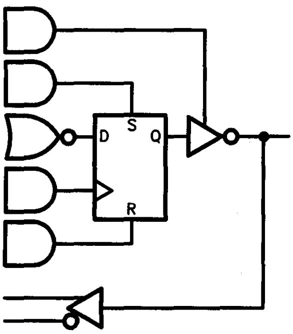
Combinatorial/Active LOW



0118-18

Registered/Active HIGH



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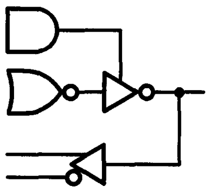
Combinatorial/Active HIGH



0118-20

Figure 3. Four Possible Macro Cell Configurations for the PLD C 20RA10

Selection Guide

Generic Part Number	t_{PD} ns		t_{SU} ns		t_{CO} ns		I_{CC} mA	
	Com	Mil	Com	Mil	Com	Mil	Com	Mil
20RA10-20	20	—	10	—	20	—	80	—
20RA10-25	—	25	—	15	—	25	—	100
20RA10-30	30	—	15	—	30	—	80	—
20RA10-35	—	35	—	20	—	35	—	100

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 24 to Pin 12).................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (LOW) .... 16 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883 Method 3015)

Latchup Current .... >200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[5]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[6]

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	$I_{OH} = -3.2$ mA	COM'L	2.4		V
			$I_{OH} = -2$ mA	MIL			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	$I_{OL} = 8$ mA			0.5	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[1]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[1]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]			−30	−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		COM'L		80	mA
				MIL		100	mA

Capacitance[3]

Parameters	Description	Test Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		8	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. *Figure 4a* test load used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}. *Figure 4b* test load used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
5. T_A is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.
7. The parameters t_{ER} and t_{PXZ} are measured as the delay from the input disable logic threshold transition to $V_{OH} - 0.5V$ for an enabled HIGH output or $V_{OL} + 0.5V$ for an enabled LOW output. Please see Table 1 for waveforms and measurement reference levels.

Switching Characteristics PLD C 20RA10 Over Operating Range[4, 6, 7]

Parameters	Description	Commercial				Military				Units
		−20		−30		−25		−35		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Non-Registered Output		20		30		25		35	ns
t_{EA}	Input to Output Enable		25		30		30		35	ns
t_{ER}	Input to Output Disable		25		30		30		35	ns
t_{PZX}	Pin 13 to Output Enable		15		20		20		25	ns
t_{PXZ}	Pin 13 to Output Disable		15		20		20		25	ns
t_{CO}	Clock to Output		20		30		25		35	ns
t_{SU}	Input or Feedback Setup Time	10		15		15		20		ns
t_H	Hold Time	0		5		0		5		ns
t_P	Clock Period	30		45		40		55		ns
t_{WH}	Clock Width HIGH	13		20		18		25		ns
t_{WL}	Clock Width LOW	13		20		18		25		ns
f_{MAX}	Maximum Frequency	33.3		22.2		25.0		18.1		MHz
t_S	Input to Asynchronous Set		20		35		25		40	ns
t_R	Input to Asynchronous Reset		25		40		30		45	ns
t_{AR}	Asynchronous Set/Reset Recovery Time	20		30		25		35		ns
t_{WP}	Preload Pulse Width	30		35		35		40		ns
t_{SUP}	Preload Setup Time	20		25		25		30		ns
t_{HP}	Preload Hold Time	20		25		25		30		ns

AC Test Loads and Waveforms (Commercial)

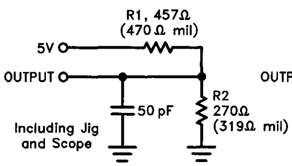


Figure 4a

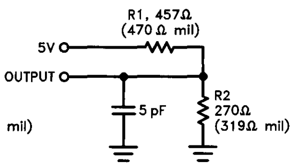
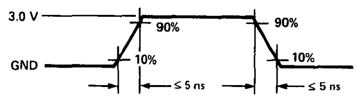


Figure 4b

0118-6

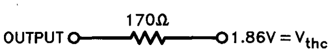
INPUT PULSES



0118-7

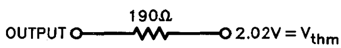
Figure 5

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



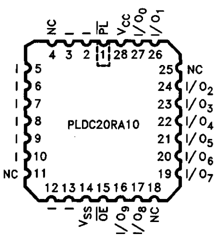
0118-8

Equivalent to: THÉVENIN EQUIVALENT (Military)



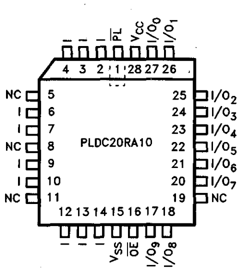
0118-9

LCC Pinout



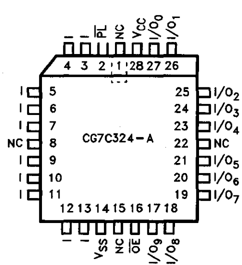
0118-21

STD PLCC and HLCC Pinout



0118-22

JEDEC PLCC and HLCC Pinout[8]

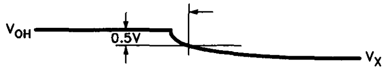
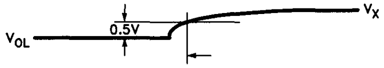
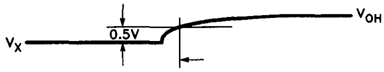
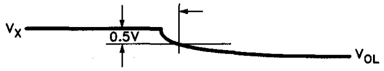
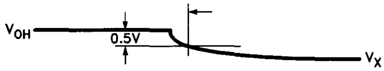
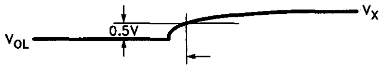
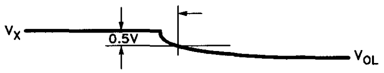


0118-27

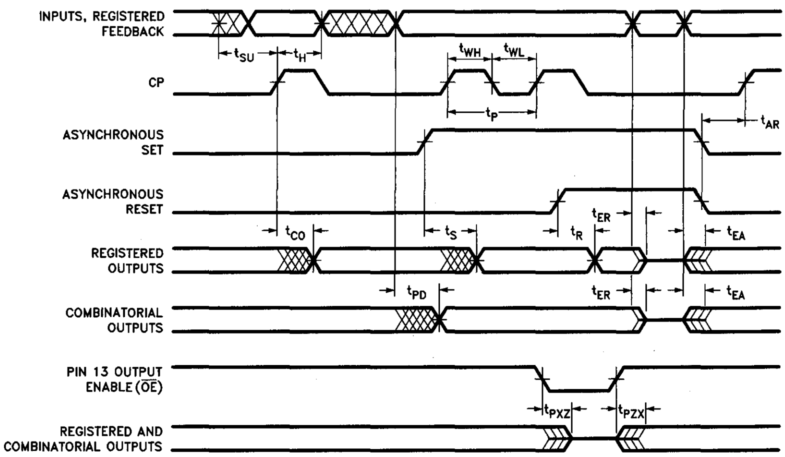
Note:

8. The CG7C324 is the PLDC20RA10 packaged in the JEDEC compatible 28-pin PLCC pinout. Pin function and pin order is identical for both PLCC pinouts. The principle difference is in the location of the "no connect" or NC pins.

Table 1

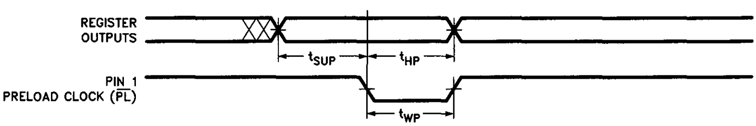
Parameter	V_X	Output Waveform—Measurement Level
$t_{PXZ}(-)$	1.5V	 0118-23
$t_{PXZ}(+)$	2.6V	 0118-24
$t_{PZX}(+)$	V_{thc}	 0118-25
$t_{PZX}(-)$	V_{thc}	 0118-26
$t_{ER}(-)$	1.5V	 0118-23
$t_{ER}(+)$	2.6V	 0118-24
$t_{EA}(+)$	V_{thc}	 0118-25
$t_{EA}(-)$	V_{thc}	 0118-26

Switching Waveforms



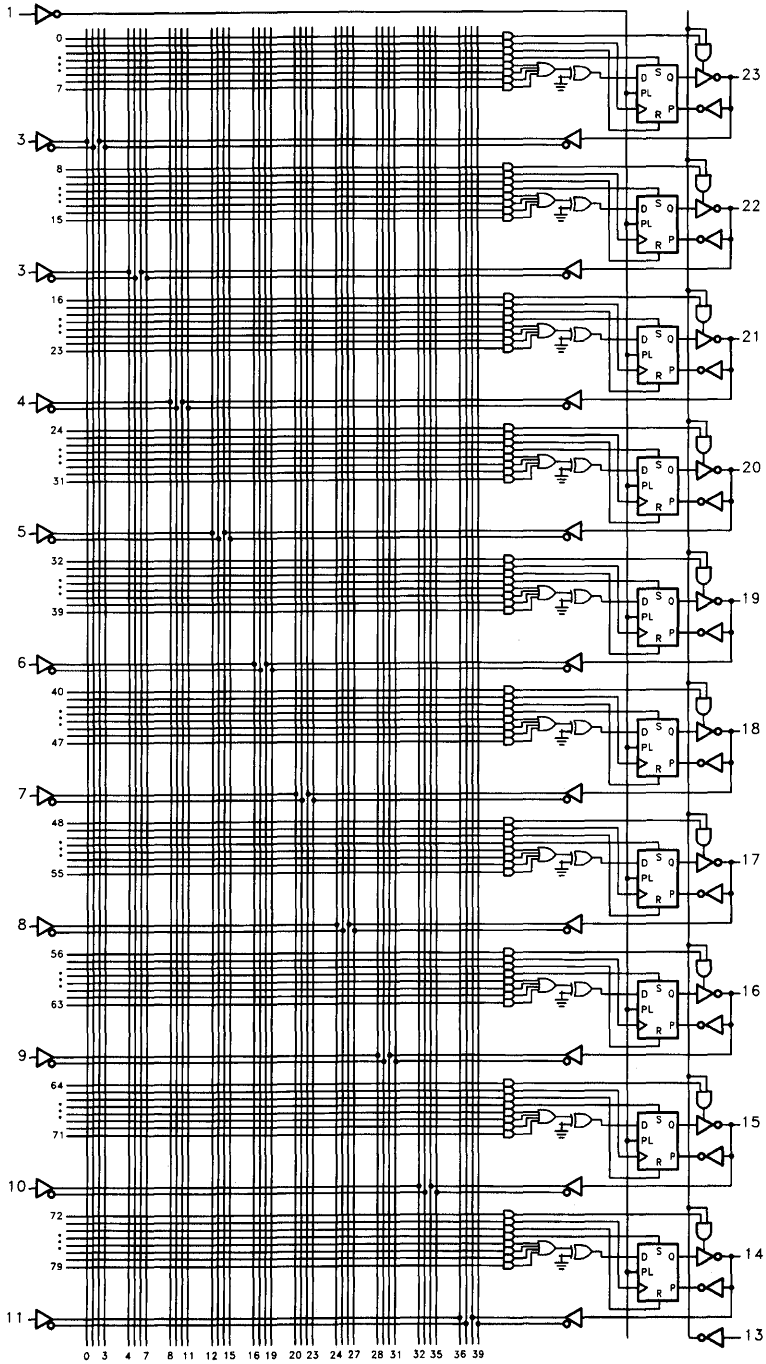
0118-10

Preload Switching Waveforms



0118-12

Functional Logic Diagram PLD C 20RA10



0118–11

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_{SU} (ns)	t_{CO} (ns)	Ordering Code	Package	Operating Range
80	20	10	20	PLD C 20RA10-20PC	P13	Commercial
				PLD C 20RA10-20WC	W14	
				PLD C 20RA10-20JC	J64	
				PLD C 20RA10-20HC	H64	
				CG7C324-A20JC	J64	
				CG7C324-A20HC	H64	
100	25	15	25	PLD C 20RA10-25DMB	D14	Military
				PLD C 20RA10-25WMB	W14	
				PLD C 20RA10-25HMB	H64	
				PLD C 20RA10-25LMB	L64	
				PLD C 20RA10-25QMB	Q64	
80	30	15	30	PLD C 20RA10-30PC	P13	Commercial
				PLD C 20RA10-30WC	W14	
				PLD C 20RA10-30JC	J64	
				PLD C 20RA10-30HC	H64	
				CG7C324-A30JC	J64	
				CG7C324-A30HC	H64	
100	35	20	35	PLD C 20RA10-35DMB	D14	Military
				PLD C 20RA10-35WMB	W14	
				PLD C 20RA10-35HMB	H64	
				PLD C 20RA10-35LMB	L64	
				PLD C 20RA10-35QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7,8,9,10,11
t_{PZX}	7,8,9,10,11
t_{CO}	7,8,9,10,11
t_{SU}	7,8,9,10,11
t_H	7,8,9,10,11

Document #: 38-00073-B

PAL C 22V10B/PAL C 22V10

Reprogrammable CMOS PAL® Device

Features

- Advanced second generation PAL architecture
- Low power
  - — 55 mA max "L"
  - — 90 mA max standard
  - — 120 mA max military
- CMOS EPROM technology for reprogrammability
- Variable product terms
  - — 2 × (8 thru 16) product terms
- User programmable macro cell
  - — Output polarity control
  - — Individually selectable for registered or combinatorial operation
  - — "15" commercial & industrial
    - 10 ns t_{CO}
    - 10 ns t_S
    - 15 ns t_{PD}
    - 50 MHz
  - — "20" military
    - 15 ns t_{CO}
    - 17 ns t_S
    - 20 ns t_{PD}
    - 31 MHz
- Up to 22 input terms and 10 outputs
- Enhanced test features
  - — Phantom array
  - — Top Test
  - — Bottom Test
  - — Preload
- High reliability
  - — Proven EPROM technology
  - — >2000V input protection
  - — 100% programming and functional testing
- Windowed DIP, windowed LCC, DIP, LCC, PLCC available

Functional Description

The Cypress PAL C 22V10 is a CMOS second generation Programmable Logic Array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the "Programmable Macro Cell".

The PAL C 22V10 is executed in a 24 pin 300 mil molded DIP, a 300 mil windowed Cerdip, a 28 lead square ceramic leadless chip carrier, a 28 lead square plastic leaded chip carrier and provides up to 22 inputs and 10 outputs. When the windowed CERDIP is exposed to UV light, the 22V10 is erased and then can be reprogrammed. The Programmable Macro Cell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified to be "REGISTERED" or "COMBINATORIAL". Polarity of

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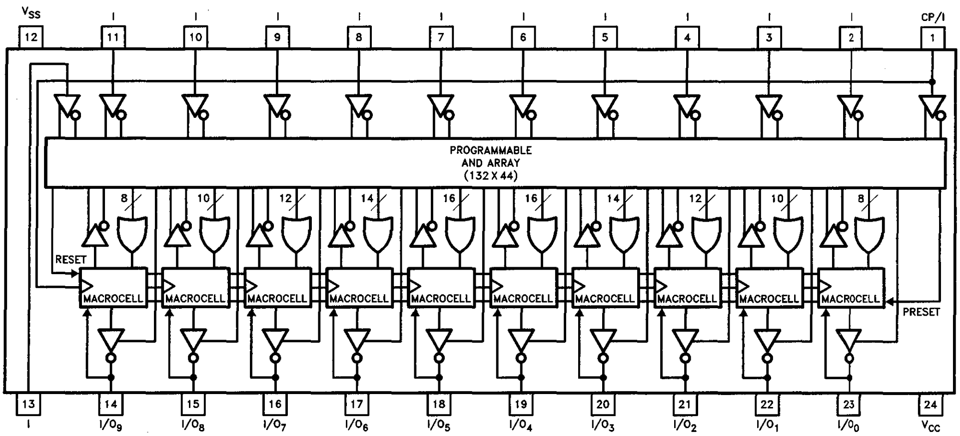
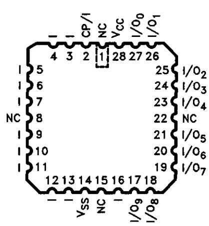
4

Logic Symbol and Pinout



0023-1

LCC and PLCC Pinout



0023-10

Functional Description (Continued)

each output may also be individually selected allowing complete flexibility of output configuration. Further configurability is provided through "ARRAY" configurable "OUTPUT ENABLE" for each potential output. This feature allows the 10 outputs to be reconfigured as inputs on an individual basis or alternately used as a combination I/O controlled by the programmable array.

The PAL C 22V10 features a "VARIABLE PRODUCT TERM" architecture. There are 5 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. By providing this variable structure the PAL C 22V10 is optimized to the configurations found in a majority of applications without creating devices that burden the product term structures with unuseable product terms and lower performance.

Additional features of the Cypress PAL C 22V10 include a synchronous PRESET and an asynchronous RESET product term. These product terms are common to all MACRO CELLS eliminating the need to dedicate standard product terms for initialization functions. The device automatically resets on power-up.

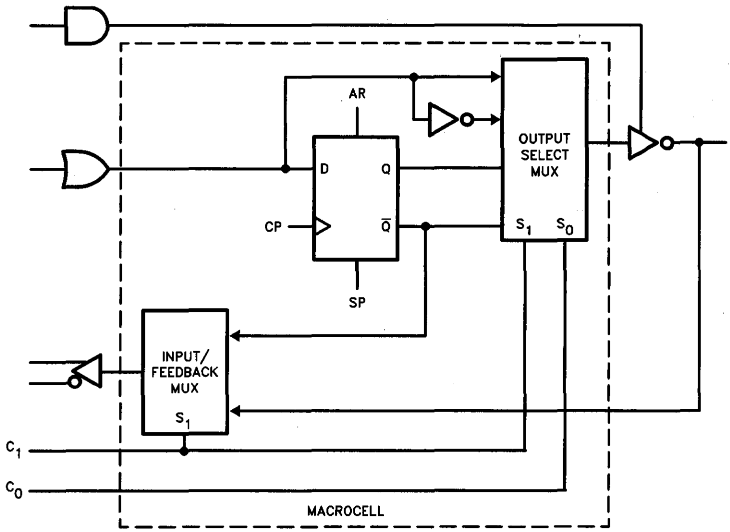
The PAL C 22V10 featuring programmable macro cells and variable product terms provides a device with the flexibility to implement logic functions in the 500 to 800 gate array complexity. Since each of the 10 output pins may be individually configured as inputs on a temporary or permanent basis, functions requiring up to 21 inputs and only a single output down to 12 inputs and 10 outputs are possible. The 10 potential outputs are enabled through the use of product terms. Any output pin may be permanently selected as an output or arbitrarily enabled as an output and an input through the selective use of individual product terms associated with each output. Each of these outputs is achieved through an individual programmable macro cell. These macro cells are programmable to provide a combinatorial or registered inverting or non-inverting output. In a registered mode of operation, the output of the register is fed back into the array providing current status information to the array. This information is available for establishing the next result in applications such as control-state-machines. In a combinatorial configuration, the combinatorial output or, if the output is disabled, the signal present on the I/O pin is made available to the array. The flexibility provided by both programmable macro cell product term control of the outputs and variable product terms allows a significant gain in functional density through the use of programmable logic.

Along with this increase in functional density, the Cypress PAL C 22V10 provides lower power operation thru the use of CMOS technology, increased testability with a register preload feature and guaranteed AC performance through the use of a phantom array. This phantom array (P_0–P_3) and the "TOP TEST" and "BOTTOM TEST" features allow the 22V10 to be programmed with a test pattern and tested prior to shipment for full AC specifications without using any of the functionality of the device specified for the product application. In addition, this same phantom array may be used to test the PAL C 22V10 at incoming inspection before committing the device to a specific function through programming. PRELOAD facilitates testing programmed devices by loading initial values into the registers.

Configuration Table 1

Registered/Combinatorial		
C_1	C_0	Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

Macrocell



0023-2

Selection Guide

Generic Part Number	I_{CC1} mA			t_{PD} ns		t_S ns		t_{CO} ns	
	"L"	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil	Com/Ind	Mil
22V10B-15		90	—	15	—	10	—	10	—
22V10B-20	—	—	120	—	20	—	17	—	15
22V10-20		90	—	20	—	12	—	12	—
22V10-25	55	90	100	25	25	15	18	15	15
22V10-30		—	100	—	30	—	20	—	20
22V10-35	55	90	—	35	—	30	—	25	—
22V10-40		—	100	—	40	—	30	—	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 24 to Pin 12).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 16 mA

UV Exposure .... 7258 Wsec/cm^2

DC Programming Voltage
PAL C 22V10B............................ 13.0V
PAL C 22V10............................ 14.0V

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[6]	−55°C to +125°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

Electrical Characteristics Over Operating Range[5]

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH1}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	COM'L/IND	2.4		V
			I_{OH} = −2 mA	MIL			
V_{OH2}	HIGH Level CMOS Output Voltage[3]	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100 μA		V_{CC} − 1.0V		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	COM'L/IND		0.5	V
			I_{OL} = 12 mA	MIL			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[1]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[1]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open in Programmed Device		"L"		55	mA
				COM'L/IND		90	mA
				MIL		100	mA
				MIL-20		120	mA

Notes:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. *Figure 1a* test load used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}. *Figure 1b* test load used for t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}.
5. See the last page of this specification for Group A subgroup testing information.
6. T_A is the "instant on" case temperature.

Capacitance[3]

Parameters	Description	Test Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		8	pF

Switching Characteristics PAL C 22V10[4, 5]

Parameters	Description	Commercial & Industrial								Military								Units
		B-15		-20		-25		-35		B-20		-25		-30		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[13]		15		20		25		35		20		25		30		40	ns
t_{EA}	Input to Output Enable Delay		15		20		25		35		20		25		25		40	ns
t_{ER}	Input to Output Disable Delay[8]		15		20		25		35		20		25		25		40	ns
t_{CO}	Clock to Output Delay[14]		10		12		15		25		15		15		20		25	ns
t_S	Input or Feedback Setup Time	10		12		15		30		17		18		20		30		ns
t_H	Input Hold Time	0		0		0		0		0		0		0		0		ns
t_P	External Clock Period ($t_{CO} + t_S$)	20		24		30		55		32		33		40		55		ns
t_{WH}	Clock Width HIGH[3]	6		10		12		17		12		14		16		22		ns
t_{WL}	Clock Width LOW[3]	6		10		12		17		12		14		16		22		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[9]	50.0		41.6		33.3		18.1		31.2		30.3		25.0		18.1		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[3, 10]	83.3		50.0		41.6		29.4		41.6		35.7		31.2		22.7		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[11]	80.0		45.4		35.7		20.8		33.3		32.2		28.5		20.0		MHz
t_{CF}	Register Clock to Feedback Input [12]		2.5		10		13		18		13		13		15		20	ns
t_{AW}	Asynchronous Reset Width	15		20		25		35		20		25		30		40		ns
t_{AR}	Asynchronous Reset Recovery Time	10		20		25		35		20		25		30		40		ns
t_{AP}	Asynchronous Reset to Registered Output Delay		20		25		25		35		25		25		30		40	ns
t_{SPR}	Synchronous Preset Recovery Time	10		20		25		35		20		25		30		40		ns
t_{PR}	Power Up Reset Time[15]	1.0		1.0		1.0		1.0		1.0		1.0		1.0		1.0		µs

Notes:

7. This parameter is sample tested periodically with the device clocked at f_{MAX} external (f_{MAX1}) with all registers cycling on each cycle and outputs disabled (in high Z state).
8. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous high level has fallen to 0.5 volts below V_{OH} Min. or a previous low level has risen to 0.5 volts above V_{OL} Max. Please see *Figure 4* for enable and disable test waveforms and measurement reference levels.
9. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feed back can operate.
10. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feed back can operate. This parameter is tested periodically by sampling production product.
12. This parameter is calculated from the clock period at f_{MAX} internal ($1/f_{MAX3}$) as measured (see note 11 above) minus t_S.
13. This specification is guaranteed for all device outputs changing state in a given access cycle. See *Figure 3* for the minimum guaranteed negative correction which may be subtracted from t_{PD} for cases in which fewer outputs are changing state per access cycle.
14. This specification is guaranteed for all device outputs changing state in a given access cycle. See *Figure 3* for the minimum guaranteed negative correction which may be subtracted from t_{CO} for cases in which fewer outputs are changing state per access cycle.
15. The registers in the PAL C 22V10 have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in *Figure 5* must be satisfied.
16. The clock signal input must be in a valid LOW state (V_{IN} less than 0.8V) or a valid HIGH state (V_{IN} greater than 2.4V) prior to occurrence of the 10% level on the monotonically rising power supply voltage as shown in *Figure 5*. In addition, the clock input signal must remain stable in that valid state as indicated until the 90% level on the power supply voltage has been reached. The clock signal may transition LOW to HIGH to clock in new data or to execute a synchronous preset after the indicated delay ($t_{PR} + t_S$) has been observed.

4

AC Test Loads and Waveforms (Commercial)

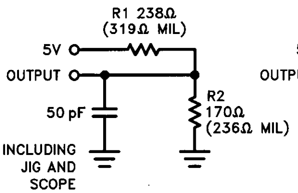


Figure 1a

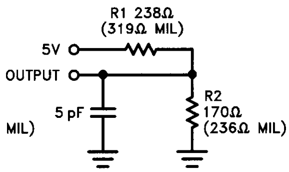


Figure 1b

0023-11

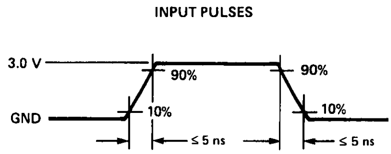
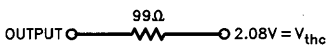


Figure 2

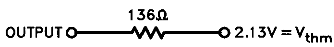
0023-12

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



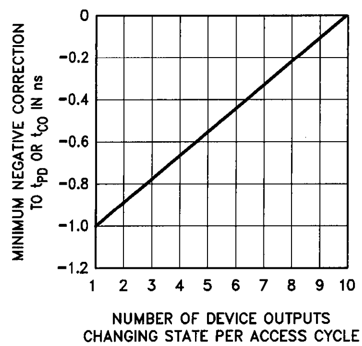
0023-13

Equivalent to: THÉVENIN EQUIVALENT (Military)



0023-14

Minimum Negative Correction to t_{PD} and t_{CO} vs. Number of Outputs Switching



0023-20

Figure 3

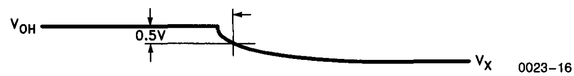
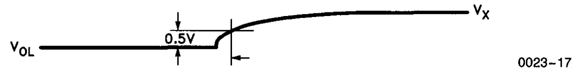
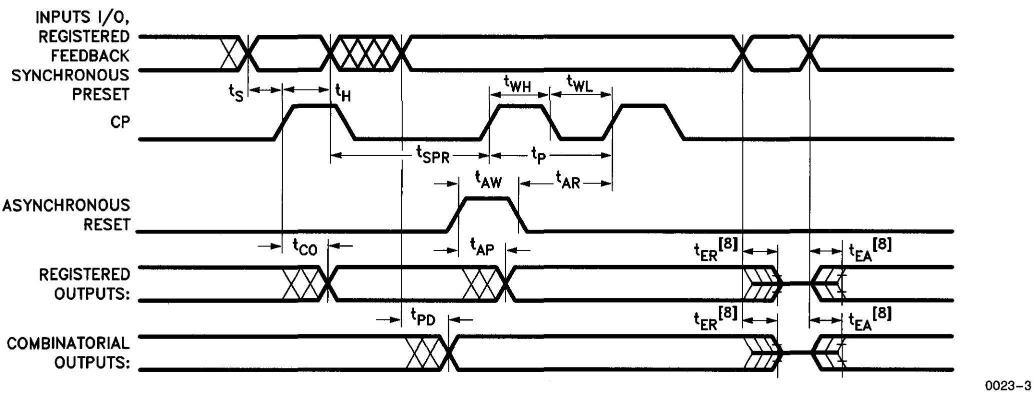
Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	
$t_{ER(+)}$	2.6V	
$t_{EA(+)}$	V_{thc}	
$t_{EA(-)}$	V_{thc}	

Figure 4. Test Waveforms

Switching Waveform



Power-Up Reset Waveform[15, 16]

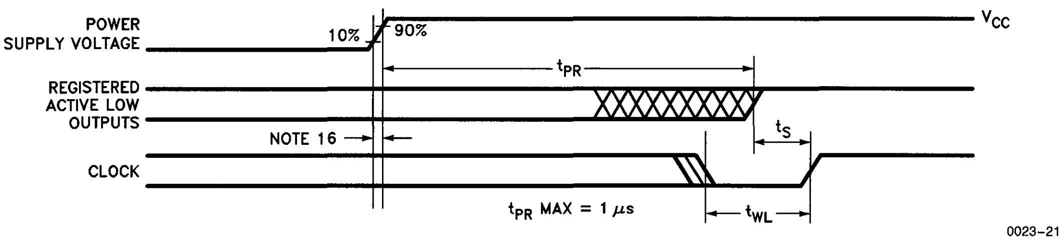
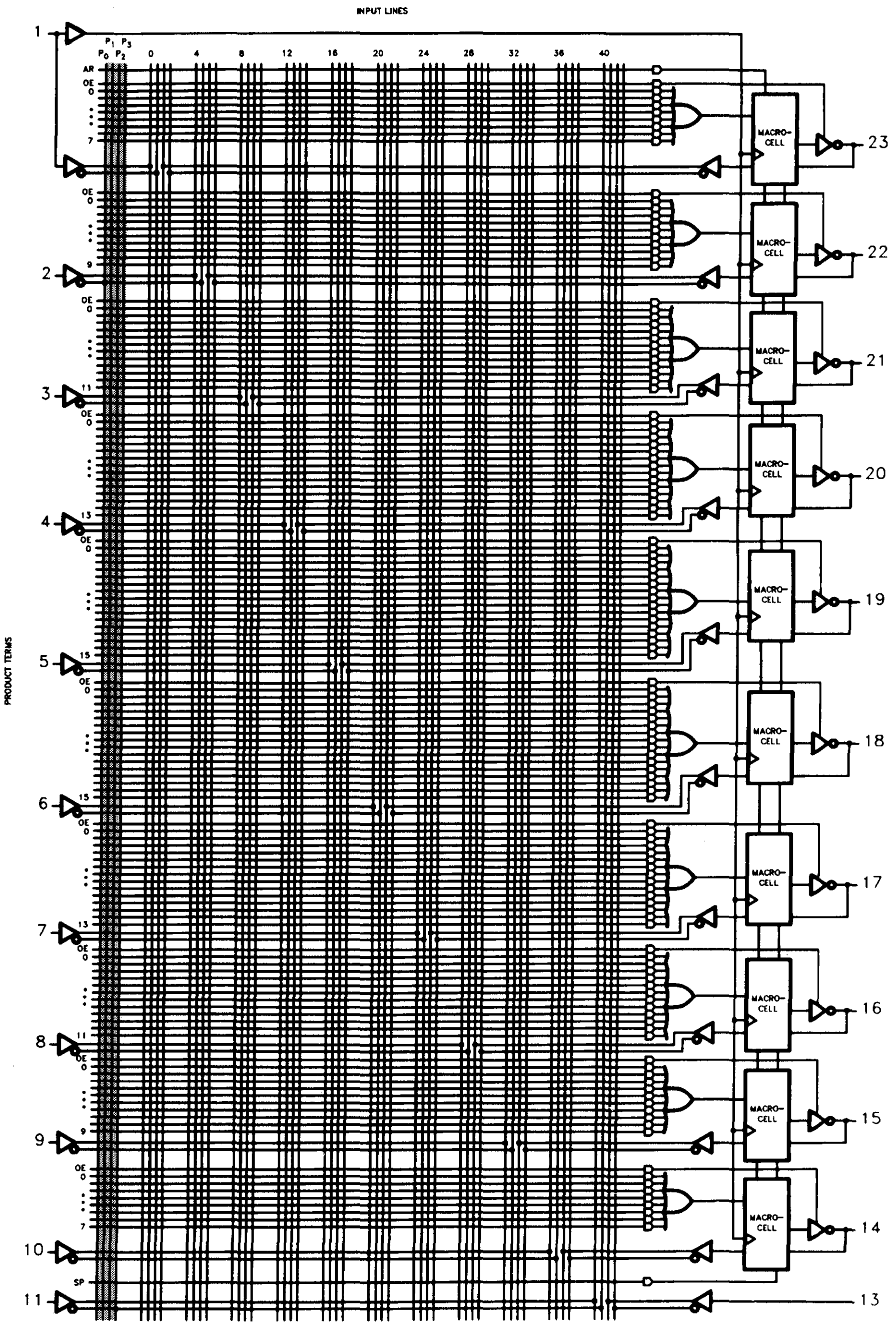


Figure 5

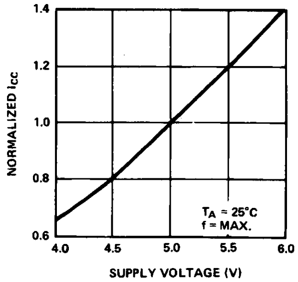
Functional Logic Diagram PAL C 22V10



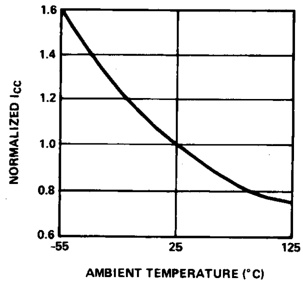
0023-4

Typical DC and AC Characteristics

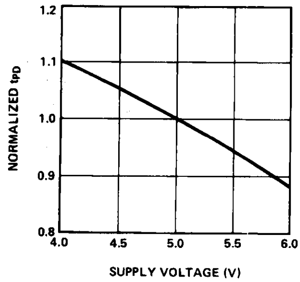
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. SUPPLY VOLTAGE



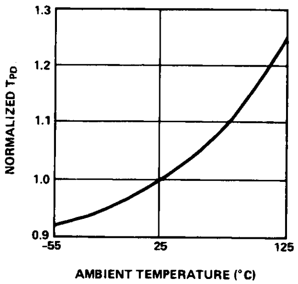
NORMALIZED STANDBY SUPPLY CURRENT (I_{CC1}) vs. AMBIENT TEMPERATURE



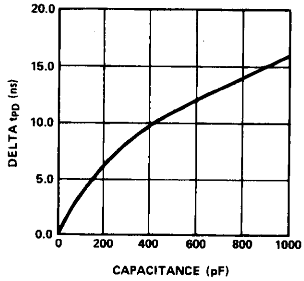
NORMALIZED PROPAGATION DELAY vs. SUPPLY VOLTAGE



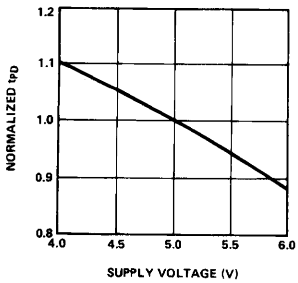
NORMALIZED PROPAGATION DELAY vs. TEMPERATURE



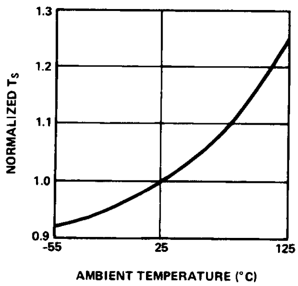
DELTA PROPAGATION TIME vs. OUTPUT LOADING



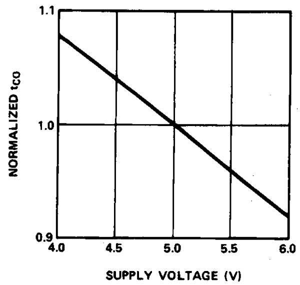
NORMALIZED SETUP TIME vs. SUPPLY VOLTAGE



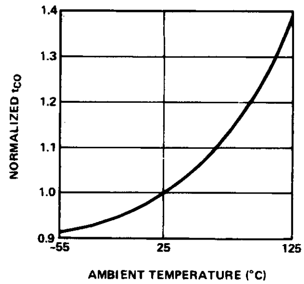
NORMALIZED SETUP TIME vs. TEMPERATURE



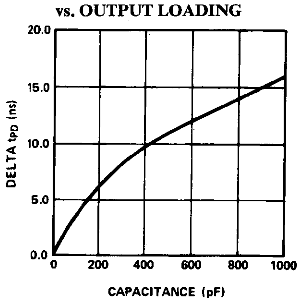
NORMALIZED CLOCK TO OUTPUT TIME vs. SUPPLY VOLTAGE



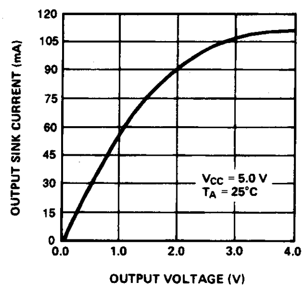
NORMALIZED CLOCK TO OUTPUT TIME vs. TEMPERATURE



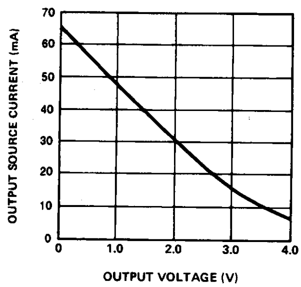
DELTA CLOCK TO OUTPUT TIME vs. OUTPUT LOADING



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. VOLTAGE



0023–15

Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the PAL C 22V10. For this reason, an opaque label should be placed over the window if the device is exposed to sunlight or fluorescent lighting for extended periods of time. In addition, high ambient light levels can create hole-electron pairs which may cause "blank" check failures or "verify errors" when programming "windowed" parts. This phenomenon can be avoided by use of an opaque label over the window during programming in high ambient light environments.

The recommended dose for erasure is ultraviolet light with a wavelength of 2537 Angstroms for a minimum dose (UV intensity × exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure would be approximately 35 minutes. The PAL C 22V10 needs to be placed within 1 inch of the lamp during erasure. Permanent damage may result if the device is exposed to high intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Device Programming

The PAL C 22V10 has multiple programmable functions. In addition to the normal array, a "PHANTOM" array, "TOP and BOTTOM TEST" and a "SECURITY" feature are programmable. The PAL C 22V10 security mechanism, when invoked, prevents access to the "NORMAL" and "TOP/BOTTOM TEST" array. The "PHANTOM" array feature is still accessible, allowing programming and verification of the pattern in the "PHANTOM" array. Functional operation of all other features is allowed regardless of the state of the "SECURITY BIT". In addition, the device contains 10 MACROCELLS which are programmed to configure the device functionality for each specific application.

The logic array is divided into a "NORMAL" array and a "PHANTOM" array. The normal array is used to configure the device to perform a specific function as required by the user, and the phantom array is provided as a test array for Cypress' testing the device prior to user programming thus assuring a reliable, thoroughly tested product. The "PHANTOM" array contains four additional columns connected to input pins 2 (TRUE), 7 (INVERTING), 10 (TRUE) and 11 (TRUE). These inputs may be programmed to be connected to all normal product terms. This allows all sense amplifiers and macrocells to be exercised for both functionality and performance after assembly and prior to shipment. These features are in addition to the normal array. They do not affect normal operation, allowing the user full programming of the normal array, while allowing the device to be fully tested.

The "TOP TEST" and "BOTTOM TEST" feature, allow connection of all input terms to either pin 23 or 13. These locations may be programmed and subsequently exercised in the "TOP TEST" and "BOTTOM TEST" mode. Like the Phantom array above, this feature has no effect in the normal mode of operation. Cells in the PHANTOM ARRAY, TOP TEST, and BOTTOM TEST areas are programmed at Cypress during the manufacturing operation, and they therefore will be programmed when received in a non-windowed package by the user. Consequently, the user will normally have no need to program these cells.

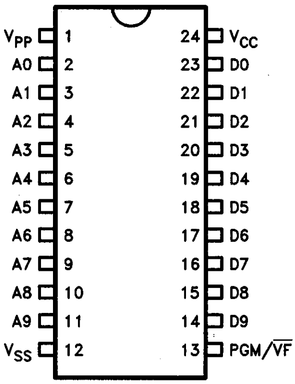
The Cypress PAL C 22V10 contains 10 identical MACROCELLS which may be individually configured. Each MACROCELL is associated with a single I/O pin and through the architecture bits, each associated pin may be permanently configured as an input, an output or be used as both input and output as a function of the logical function in the array. Each MACROCELL consists of a type "D" latch, an output multiplexer, a feedback multiplexer and a tristatable output driver that is controlled by a unique product term. The clock is common to all MACROCELLS, and comes from pin 1 of the device. Each register also has an asynchronous reset and a synchronous preset. These are each driven by product terms. These product terms are common to all MACROCELLS allowing all registers to either be asynchronously reset or synchronously preset by a logical function in the array. The device is automatically reset at power up. A preload feature allows the registers to be preloaded with any state for testing.

The architecture bits C0 and C1 are used to configure each MACROCELL individually. C0 selects the polarity of the output and C1 selects the combinatorial or registered mode of operation. If the registered mode of operation is selected, the feedback path is automatically selected to be from the register. In the combinatorial mode the feedback path is automatically selected to be from the I/O pin. In this combinatorial mode, the output from the array may be fed into the array or if the output is deselected using the output enable product term the pin may be used as an external input. There is not a mode where the I/O pin may be used as a combinatorial output or an input pin, while the register is used as a state register. The architecture bits are programmed as a separate item during normal programming. An I/O pin is configured to be an input by programming the MACROCELL into a combinatorial mode and disabling the ouput with the output enable product term.

Pinout

The PAL C 22V10 PROGRAMMING pinout is shown in *Figure 6*. In the Programming pinout configuration, the device may be programmed and verified for the NORMAL mode of operation and also programmed, verified and operated in PHANTOM and TEST modes. These special modes of operation are achieved through the use of supervoltages applied to certain pins. Care should be exercised when entering and exiting these modes, paying specific attention to both the operating modes as specified in Table 1 and the sequencing of the supervoltages as shown in the timing diagrams.

Programming Pinout



0023-6

Figure 6

Programming Algorithm

With the exception of the Security bit, all arrays are programmed in a similar manner. The data to be programmed is represented by a "1" or "0" on the I/O pins. A "1" indicates that an unprogrammed location is to be programmed and a "0" indicates that an unprogrammed location is to remain unprogrammed. All locations to be programmed are addressed as row and column locations. Table 1 "Operating Modes" along with Tables 2 through 5 provide the specific address for each addressed location to be programmed along with mode selection information for both programming and operation in the "PHANTOM" and "TEST" modes.

When programming the security bit, a supervoltage on pin 3 is used as data with a programming pulse on pin 13. Verification is controlled with a supervoltage on pins 4 and the data out on pin 3.

Operating Modes

Table 1 describes the operating and programming modes of the PAL C 22V10. The majority of the programming modes function with a PROGRAM, PROGRAM INHIBIT and PROGRAM VERIFY sequence. The exception is the Security Program operation, which shows no program inhibit function. Two timing diagrams are provided for these two different methodologies of programming in *Figures 8* & *9*. Tables 2 through 5 are used as indicated to provide the individual addresses of the various arrays and cells to be programmed. There are 5 operating modes in addition to the programming modes for the PAL C 22V10. These provide NORMAL operation, PHANTOM operation, TOP TEST, BOTTOM TEST and a register preload feature for testing.

In the normal operating mode, all signals are TTL levels and the device functions as it is internally programmed in the NORMAL array. In the PHANTOM mode of operation, the device operates logically as a function of the contents of the PHANTOM array. In this mode pins 2, 10 & 11 are non-inverting inputs and pin 7 is an inverting input. The MACROCELLS function as they are programmed for normal operation. If the MACROCELLS have not yet been programmed, they are in a registered inverting configuration. The PHANTOM mode is invoked by placing a supervoltage V_{PP} on pin 6. Care should be exercised when entering and leaving this mode that the supervoltage is applied no sooner than 20 ms after the V_{CC} is stable, and removed a minimum of 20 ms before V_{CC} is removed.

TOP and BOTTOM TEST

The TOP TEST and BOTTOM TEST modes are entered and exited in the same manner, with the same concern for power sequencing, but the supervoltage is applied to pins 9 & 10 respectively. In these modes an extra product term controls an output pin. TOP TEST controls pin 23, and BOTTOM TEST controls pin 14. These product terms are controlled by the normal device inputs, and allow testing of all input structures.

Preload

Finally for testing of programmed functions, a preload feature allows any or all of the registers to be loaded with an initial value for testing. This is accomplished by raising pin 8 to a supervoltage V_{PP}, which puts the output drivers in a high impedance state. The data to be loaded is then placed on the I/O pins of the device and is loaded into the registers on the positive edge of the clock on pin 1. A "0" on the I/O pin preloads the register with a "0" and a "1" preloads the register with a "1". The actual signal on the output pin will depend on the output polarity selected when the MACROCELL is programmed. The data on the I/O pins is then removed, and pin 8 returned to a normal TTL voltage. Again care should be exercised to power sequence the device properly.

Operating Modes

Table 1

Operating Modes: Feature	Operating Modes: Function	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 17	Pin 20	Pins 15, 16, 18, 19, 21 & 22	Pin 23
Main Array Product	Program	V_{PP}	Table 2						Table 3				V_{PP}	Data In				
	Program Inhibit	V_{PP}											V_{IHP}	High Z				
	Program Verify[3]	V_{PP}											V_{ILP}	Data Out				
Output Enable Product Terms	Program	V_{PP}	Table 2						V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	Data Out				
Sync Set, Async Reset, Top Test, Bottom Test Notes	Program	V_{PP}	Table 2						V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	Data In	Data In	Data In	V_{ILP}	Data In
	Program Inhibit	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	High Z	High Z	High Z	High Z	High Z
	Program Verify	V_{PP}							V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	Data Out	Data Out	Data Out	Driven	Data Out
Architecture Bits	Program	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	Table 4		V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}			V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}			V_{PP}	V_{ILP}	Data Out				
Security Bit	Program	V_{PP}	V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
	Verify	V_{ILP}	V_{ILP}	Data Out	V_{PP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	Driven Outputs				
PAL Mode Operation	Normal	CP/I	I	I	I	I	I	I	I	I	I	I	I	I/O				
	Phantom	NA	I	NA	NA	NA	V_{PP}	I	NA	NA	I	I	NA	Output				
	Top Test	I	I	I	I	I	I	I	I	V_{PP}	I	I	I	NA				Out
	Bottom Test	I	I	I	I	I	I	I	I	I	V_{PP}	I	I	Out	NA			
	Reg Preload	Notes	NA	NA	NA	NA	NA	NA	V_{PP}	NA	NA	NA	V_{ILP}	Data In				
Phantom Array Product Terms	Program	V_{PP}	V_{ILP}	V_{ILP}	Table 5		V_{ILP}	V_{PP}	Table 3				V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}					V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}					V_{ILP}	Data Out				
Phantom Output Enable Product Terms	Program	V_{PP}	V_{ILP}	V_{ILP}	Table 5		V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{PP}	Data In				
	Program Inhibit	V_{PP}	V_{ILP}	V_{ILP}			V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{IHP}	High Z				
	Program Verify	V_{PP}	V_{ILP}	V_{IL}			V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{PP}	V_{ILP}	Data Out				

Notes:

1. DATA IN and DATA OUT for programming Synchronous Set, Asynchronous Reset, TOP TEST and BOTTOM TEST is programmed and verified on the following pins.
   Pin 14 = BOTTOM TEST
   Pin 17 = Synchronous Set
   Pin 20 = Asynchronous Reset
   Pin 23 = TOP TEST
2. The preload clock on pin 1 loads the Registers on a LOW going HIGH transition.
3. It is necessary to toggle $\overline{OE}$ (Pin 13) HIGH during all address transitions while in the program verify/blank check mode.

Input Term Addresses

Table 2 is used during the programming and verification of the main array, output enable, asynchronous reset, synchronous preset, TOP and BOTTOM TEST as shown in Table 1. It provides the addressing for the 44 normal input term columns which are connected with an EPROM transistor to the product terms.

Input Term Addresses

Table 2

Input Term	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
8	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
9	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
11	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
12	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
13	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
15	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
16	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
17	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
18	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
19	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
20	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
21	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
22	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
23	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
24	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
25	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
26	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
27	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
28	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
29	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
30	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
31	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
32	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
33	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
34	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
35	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
36	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
37	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
38	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
39	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
40	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
41	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
42	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
43	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}

Product Term Addresses

Table 3 is used for the programming of the "PHANTOM" and normal array. It provides the addressing for the up to 16 product terms associated with each input. Notice that the number of product terms varies from 8 to 16 and back to 8 from the top to the bottom output. In Table 3, product term "0" refers to the top product term associated with the MACROCELLS on pins 18 and 19, while address 15 refers to the bottom or last product term associated with the same pins. In the same manner, the 8 product terms associated with pins 14 and 23 are addressed as "0" through "7". The balance of the product terms associated with the remaining I/O pins are addressed as "0" through "10", "12" and "14".

Product Term Addresses

Table 3

Product Term	Pin 8	Pin 9	Pin 10	Pin 11
0	V_{ILP}	V_{ILP}	V_{ILP}	V_{ILP}
1	V_{IHP}	V_{ILP}	V_{ILP}	V_{ILP}
2	V_{ILP}	V_{IHP}	V_{ILP}	V_{ILP}
3	V_{IHP}	V_{IHP}	V_{ILP}	V_{ILP}
4	V_{ILP}	V_{ILP}	V_{IHP}	V_{ILP}
5	V_{IHP}	V_{ILP}	V_{IHP}	V_{ILP}
6	V_{ILP}	V_{IHP}	V_{IHP}	V_{ILP}
7	V_{IHP}	V_{IHP}	V_{IHP}	V_{ILP}
8	V_{ILP}	V_{ILP}	V_{ILP}	V_{IHP}
9	V_{IHP}	V_{ILP}	V_{ILP}	V_{IHP}
10	V_{ILP}	V_{IHP}	V_{ILP}	V_{IHP}
11	V_{IHP}	V_{IHP}	V_{ILP}	V_{IHP}
12	V_{ILP}	V_{ILP}	V_{IHP}	V_{IHP}
13	V_{IHP}	V_{ILP}	V_{IHP}	V_{IHP}
14	V_{ILP}	V_{IHP}	V_{IHP}	V_{IHP}
15	V_{IHP}	V_{IHP}	V_{IHP}	V_{IHP}

Architecture Bit Addresssing

Table 4 provides the addressing for the architecture bits used to control the configuration of the individual MACROCELLS. In the unprogrammed state, the MACROCELLS are in a registered, active low or inverting configuration. They are programmed with a "1" on the pin associated with the MACROCELL and the appropriate address as shown in Table 4. Each architecture bit that is not to be programmed, requires a "0" on the I/O pin associated with the MACROCELL.

Architecture Bit Addresssing

Table 4

Architecture Bit	Pin 9	Pin 10
Output Polarity C0	V_{ILP}	V_{ILP}
Register/ Non-Register Output C1	V_{IHP}	V_{ILP}

Phantom Input Term Addressing

Phantom input terms are addressed as columns P0 thru P3 and represent inputs from pins 2, 7, 10 and 11 respectively. Pin 7 is inverted, and the remaining 3 are normal non-inverting. This PHANTOM array allows the output structures to be tested. They are only present in PHANTOM modes of operation.

Phantom Input Term Addresses

Table 5

Phantom Input Term	Pin 4	Pin 5
P0	V_{ILP}	V_{ILP}
P1	V_{IHP}	V_{ILP}
P2	V_{ILP}	V_{IHP}
P3	V_{IHP}	V_{IHP}

4

Programming Flow Chart

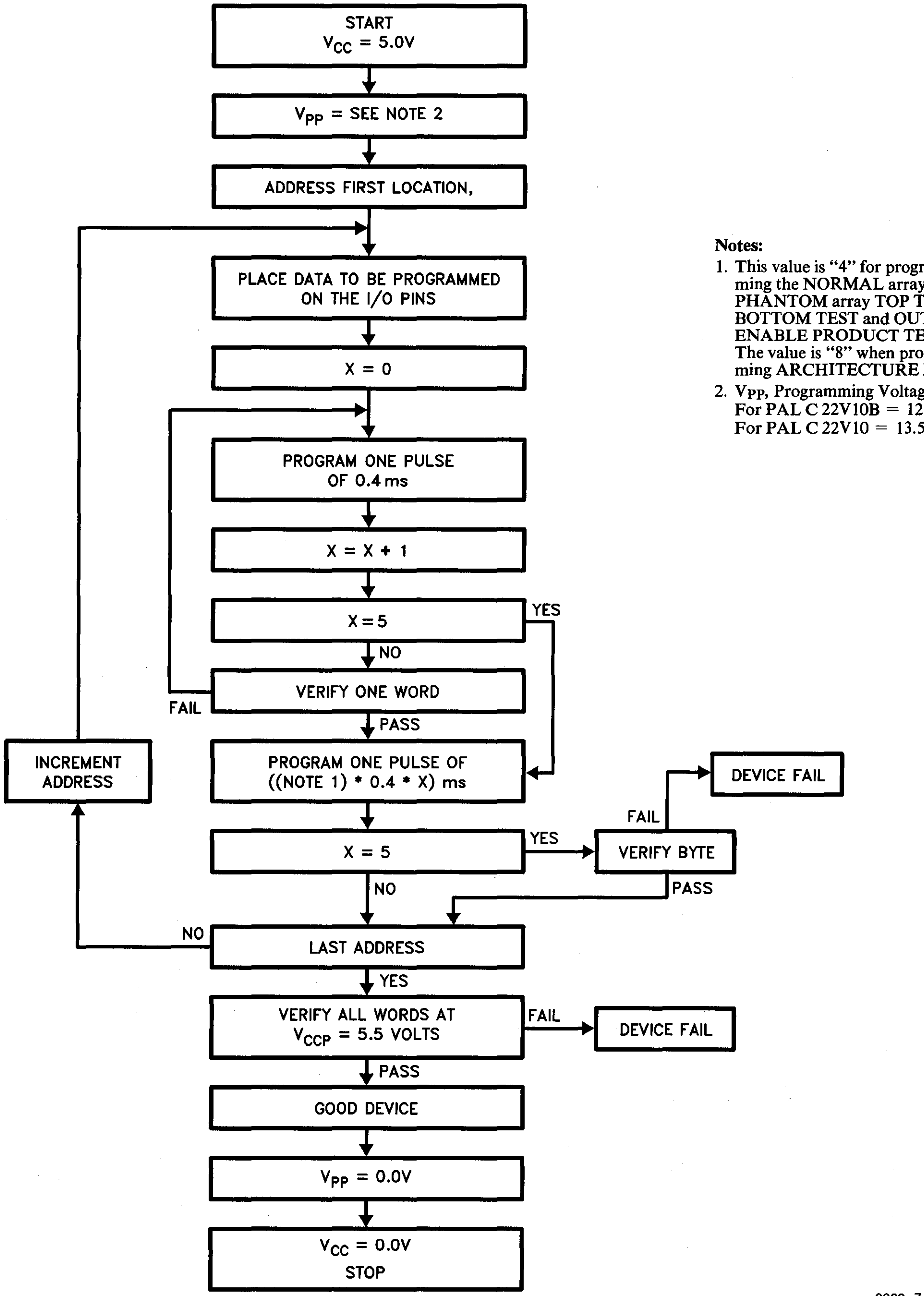
The programming flow chart describes the sequence of operations for programming the NORMAL and PHANTOM arrays, the NORMAL and PHANTOM output enable product terms, the set and preset product terms, the Top Test product term, the Bottom Test product term, and the architecture bits. The exact sequencing and timing of the signals is shown in the "Array Programming Timing Diagram".

The logical sequence to program the device is described in detail in the flow chart below, and should be followed exactly for optimum intelligent programming that both minimizes programming time and realizes reliable programming. Particular attention should be paid to the application of V_{CC} prior to V_{PP}, and removal of V_{PP} prior to V_{CC}. See *Figure 8* and Table 7 for specific timing and AC requirements. Notice that all programming is accomplished without switching V_{PP} on pin 1 and that after programming and verifying all locations individually, the programmed locations should be verified one final time.

The normal word programming cycle, programs and verifies a word at a time as shown in the programming flowchart, *Figure 7* and timing diagram *Figure 8*. After all locations are programmed, the flowchart requires a verify of all words. There is no independent timing diagram for this operation, rather *Figure 8* also provides the correct timing information for this operation. When performing this verify only operation, eliminate the program portion of the cycle but maintain the setup and hold timing relative to the verify pulse. Under no circumstances should the verify signal be held low and the addresses toggled.

Note that the overprogram pulse in step 10 of the programming flowchart is a variable, "4" times the initial value when programming the NORMAL, PHANTOM, TOP TEST, BOTTOM TEST and OUTPUT ENABLE product terms and "8" times the initial value when programming the ARCHITECTURE BITS.

Programming Flowchart



Notes:

1. This value is "4" for programming the NORMAL array, PHANTOM array TOP TEST, BOTTOM TEST and OUTPUT ENABLE PRODUCT TERMS. The value is "8" when programming ARCHITECTURE BITS.
2. V_{PP}, Programming Voltage:
   For PAL C 22V10B = 12.5V
   For PAL C 22V10 = 13.5V

Figure 7

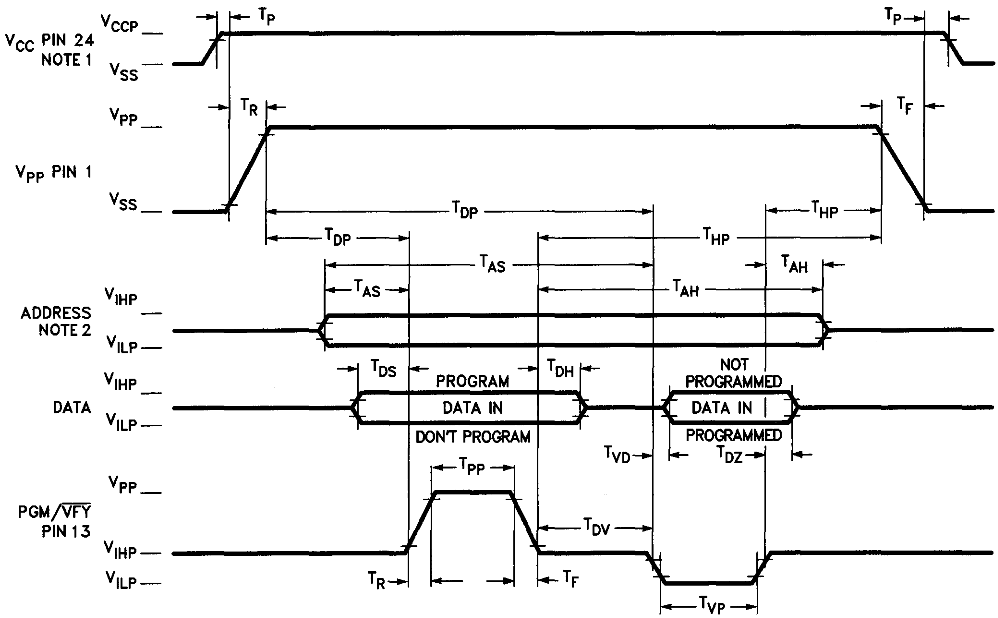
Timing Diagrams

Programming timing diagrams are provided for two cases, programming of all cells except the SECURITY BIT and programming the SECURITY BIT.

Array

Programming the NORMAL and PHANTOM arrays and output enables, reset, preset, architecture bits and the top/bottom test features uses the timing diagram in *Figure 8.* ADDRESS refers to all applicable information in Tables 1 through 5 that is not specifically referenced in the timing diagram. DATA IN is provided on the I/O pins and DATA OUT is verified on the same pins. A "1" (V_{IHP}) on an I/O pin causes the addressed location to be programmed. A "0" on the I/O pin leaves the addressed location to be unprogrammed. All setup hold and delay times must be met, and in particular the sequence of operations should be strictly followed. During verify only operation it is not acceptable to hold PGM/VFY low and sequence addresses, as it violates address setup and hold times. Proper sequencing of all power and supervoltages is essential, to reliable programming of the device as improper sequencing could result in device damage.

Programming Waveforms



Notes:

1. Power, V_{PP} & V_{CC} should not be cycled for each program/verify cycle, but may remain static during programming.
2. For programming $\overline{OE}$ Product Terms & Architecture bits, Pin 11 (A9) must go to V_{PP} and satisfy T_{AS} and T_{AN}.

Figure 8

Security Cell

The security cell is programmed independently per the timing diagram in *Figure 9*, and the information in Table 1. Note again that proper sequencing of power and programming signals is required. Data in is represented as a supervoltage on pin 3 and verified as a TTL signal output on the same pin. A "0" on pin 3 indicates that the security bit has been programmed, and a "1" indicates that security bit has not been programmed. Security is programmed with a single 50 ms pulse on pin 13. A supervoltage on pin 4 is used to verify security after V_{PP} has been removed from pin 1.

Programming Waveforms Security Cell

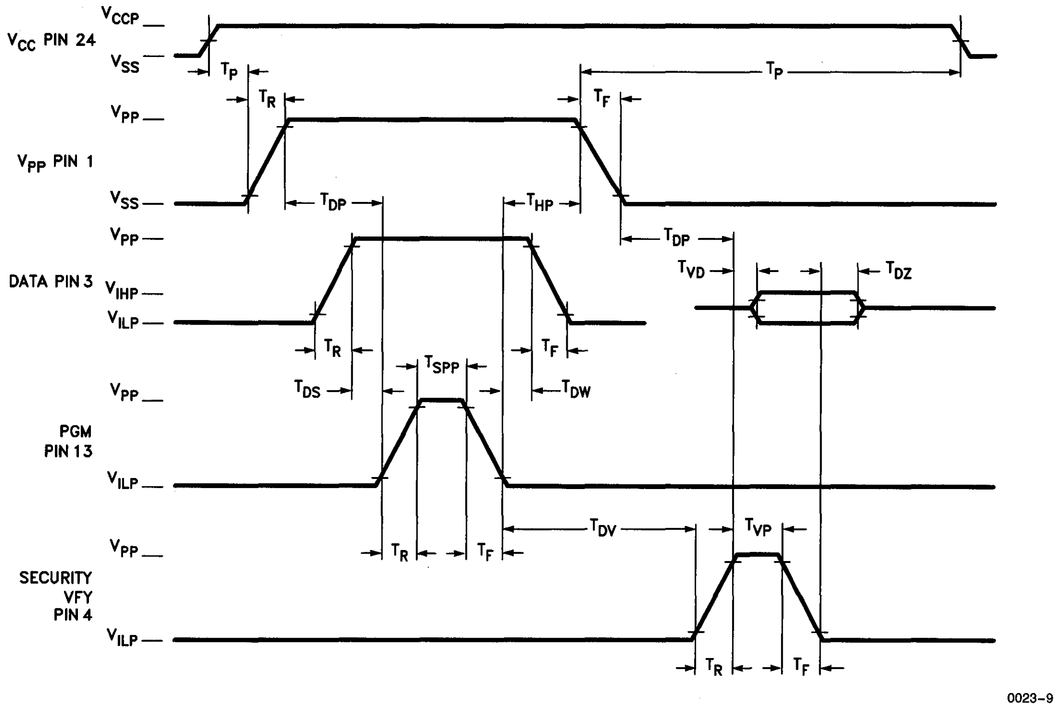


Figure 9

DC Programming Parameters $T_A = 25°C$

Table 6

Parameter	Description	Min.	Max.	Units
V_{PP} for PAL C 22V10B	Programming Voltage	12.0	13.0	Volts
V_{PP} for PAL C 22V10	Programming Voltage	13.0	14.0	Volts
V_{CCP}	Supply Voltage During Programming	4.75	5.25	Volts
V_{IHP}	Input HIGH Voltage During Programming	3.0	V_{CCP}	Volts
V_{ILP}	Input LOW Voltage During Programming	−3.0	0.4	Volts
V_{OH}	Output HIGH Voltage	2.4		Volts
V_{OL}	Output LOW Voltage		0.4	Volts
I_{PP}	Programming Supply Current		40	mA

AC Programming Parameters

Table 7

Parameter	Description	Min.	Max.	Units
T_P	Delay to Programming Voltage	20		ms
T_{DP}	Delay to Program	1		μs
T_{HP}	Hold from Program or Verify	1		μs
$T_{R,F}$	V_{PP} Rise & Fall Time	50		ns
T_{AS}	Address Setup Time	1		μs
T_{AH}	Address Hold Time	1		μs
T_{DS}	Data Setup Time	1		μs
T_{DH}	Data Hold Time	1		μs
T_{PP}	Programming Pulsewidth	0.4	10	ms
T_{SPP}	Programming Pulsewidth for Security	50		ms
T_{DV}	Delay from Program to Verify	2		μs
T_{VD}	Delay to Data Out		1	μs
T_{VP}	Verify Pulse Width	2		μs
T_{DZ}	Verify to High Z		1	μs

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operating Range
90	15	10	10	PAL C 22V10B-15PC/PI	P13	Commercial/Industrial
				PAL C 22V10B-15WC/WI	W14	
				PAL C 22V10B-15JC/JI	J64	
				PAL C 22V10B-15HC	H64	
90	20	12	12	PAL C 22V10-20PC/PI	P13	Commercial/Industrial
				PAL C 22V10-20WC/WI	W14	
				PAL C 22V10-20JC/JI	J64	
				PAL C 22V10-20HC	H64	
120	20	17	15	PAL C 22V10B-20DMB	D14	Military
				PAL C 22V10B-20WMB	W14	
				PAL C 22V10B-20HMB	H64	
				PAL C 22V10B-20LMB	L64	
				PAL C 22V10B-20QMB	Q64	
				PAL C 22V10B-20KMB	K73	
55	25	15	15	PAL C 22V10L-25PC	P13	Commercial
				PAL C 22V10L-25WC	W14	
				PAL C 22V10L-25JC	J64	
				PAL C 22V10L-25HC	H64	
90	25	15	15	PAL C 22V10-25PC/PI	P13	Commercial/Industrial
				PAL C 22V10-25WC/WI	W14	
				PAL C 22V10-25JC/JI	J64	
				PAL C 22V10-25HC	H64	
100	25	18	15	PAL C 22V10-25DMB	D14	Military
				PAL C 22V10-25WMB	W14	
				PAL C 22V10-25HMB	H64	
				PAL C 22V10-25LMB	L64	
				PAL C 22V10-25QMB	Q64	
				PAL C 22V10-25KMB	K73	
100	30	20	20	PAL C 22V10-30DMB	D14	Military
				PAL C 22V10-30WMB	W14	
				PAL C 22V10-30HMB	H64	
				PAL C 22V10-30LMB	L64	
				PAL C 22V10-30QMB	Q64	
				PAL C 22V10-30KMB	K73	
55	35	30	25	PAL C 22V10L-35PC	P13	Commercial
				PAL C 22V10L-35WC	W14	
				PAL C 22V10L-35JC	J64	
				PAL C 22V10L-35HC	H64	
90	35	30	25	PAL C 22V10-35PC/PI	P13	Commercial/Industrial
				PAL C 22V10-35WC/WI	W14	
				PAL C 22V10-35JC/JI	J64	
				PAL C 22V10-35HC	H64	
100	40	30	25	PAL C 22V10-40DMB	D14	Military
				PAL C 22V10-40WMB	W14	
				PAL C 22V10-40HMB	H64	
				PAL C 22V10-40LMB	L64	
				PAL C 22V10-40QMB	Q64	
				PAL C 22V10-40KMB	K73	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7,8,9,10,11
t_{CO}	7,8,9,10,11
t_S	7,8,9,10,11
t_H	7,8,9,10,11

Document #: 38-00020-D

Universal PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **10-ns t_{PD}, 90-MHz, f_{MAX}**
- **BiCMOS technology**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **8 to 16 per output**
- **10 user-programmable output macrocells**
  - **Output polarity control**
  - **Registered or combinatorial operation**
  - **2 new feedback paths (PAL22VP10C)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **Proven Ti-W fuse technology**
  - **AC and DC tested at the factory**
  - **> 2001V input protection**
- **Standard 300-mil PDIP and CDIP packages**
- **PLCC and LCC packages with additional V_{CC} and V_{SS} pins for improved performance**
- **Security Fuse**

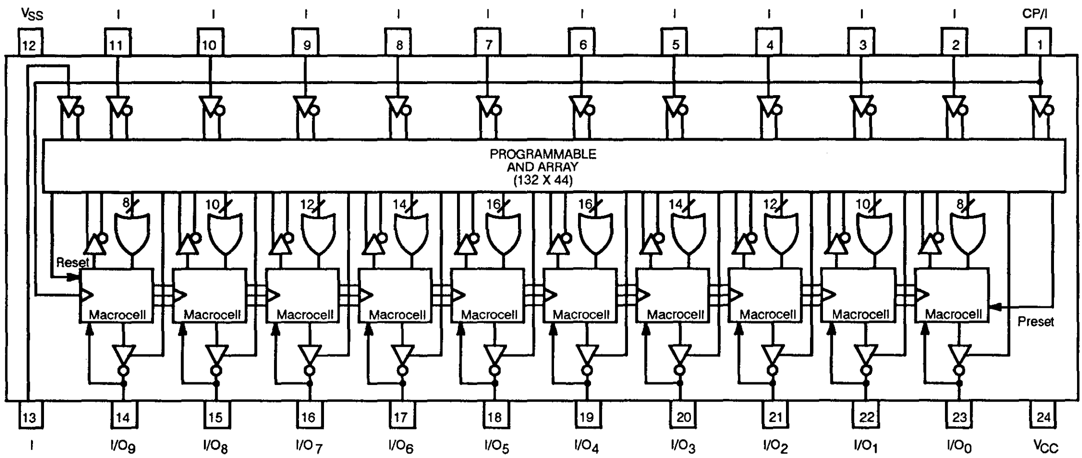
Functional Description

The Cypress PAL22V10C and PAL22VP10C are second-generation Programmable Array Logic devices. Developed by Aspen Semiconductor, a subsidiary of Cypress, using BiCMOS process and Ti-W fuses, the PAL22V10C and PAL22VP10C use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

Both the PAL22V10C and PAL22VP10C provide 12 dedicated input pins and 10 I/O pins (see Logic Symbol). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The "OUTPUT ENABLE" product term available on each I/O allows this selection.

The PAL22V10C and PAL22VP10C feature variable product term architecture, where 8 to 16 product terms are allocated to each output (see Logic Symbol for details). This structure permits more applications to be implemented with these devices than with other PAL devices that have fixed number of product terms for each output.

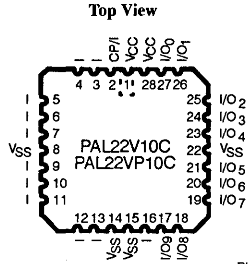
Logic Block Diagram



PIOF-1

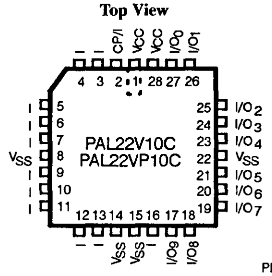
Pin Configurations

LCC
Top View



PIOF-2

PLCC
Top View



PIOF-3

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Functional Description (continued)

Additional features include common synchronous PRESET and asynchronous RESET product terms. They eliminate the need to use standard product terms for initialization functions.

Both the PAL22V10C and PAL22VP10C automatically reset on power-up. In addition, the PRELOAD capability allows the output registers to be set to any desired state during testing.

A security fuse is provided on each of these two devices to prevent copying of the device fuse pattern.

With the programmable macrocells and variable product term architecture, the PAL22V10C and PAL22VP10C can implement logic functions in the 700 to 800 gate array complexity, with the inherent advantages of programmable logic.

Programmable Macrocell

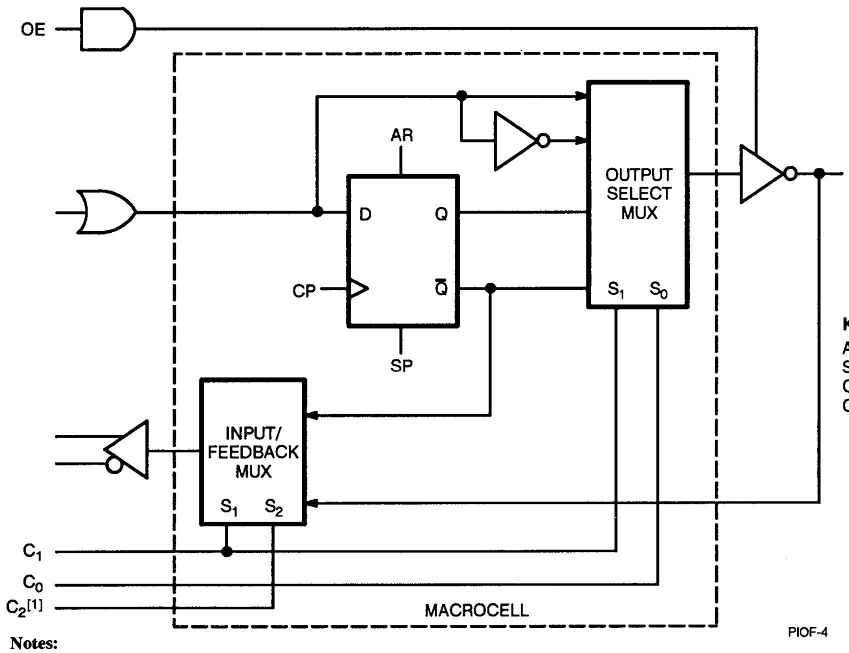
The PAL22V10C and PAL22VP10C each has 10 programmable output macro cells (see Macrocell). On the PAL22V10C two fuses (C1 and C0) can be programmed to configure output in one of four ways. Accordingly each output can be "REGISTERED" or "COMBINATORIAL" with an active HIGH or active LOW polarity. The feedback to the array is also from this output (see *Figure 1*). An additional fuse (C2) in the PAL22VP10C provides for two additional feedback paths (see *Figure 2*).

Programming

The PAL22V10C and PAL22VP10C can be programmed using the QuickPro II programmer available from Cypress Semiconductor and also with Data I/O programmers. Please contact your local Cypress representative for further information.

4

Macrocell

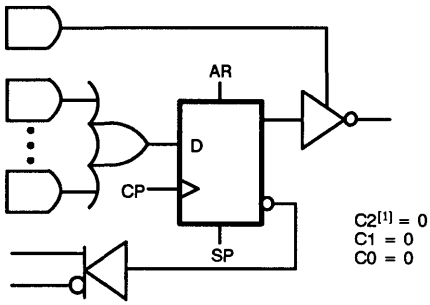


Key:
AR = Asynchronous RESET
SP = Synchronous PRESET
OE = Output Enable
CP = Clock Pulse

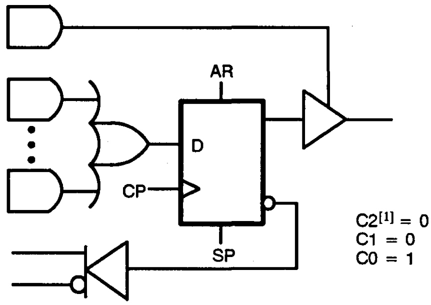
Notes:
1. PAL22VP10C only

Table 1. Output Macrocell Configuration

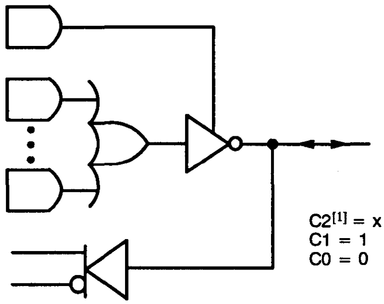
C2[1]	C1	C0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
x	1	0	Combinatorial	Active LOW	I/O
x	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O[1]
1	0	1	Registered	Active HIGH	I/O[1]



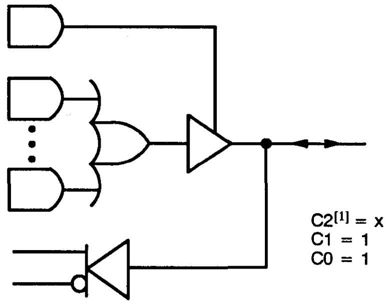
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

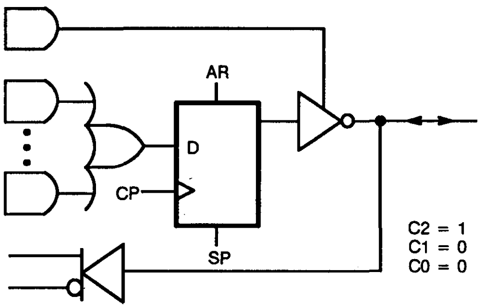


I/O FEEDBACK, COMBINATORIAL, ACTIVE-LOW OUTPUT

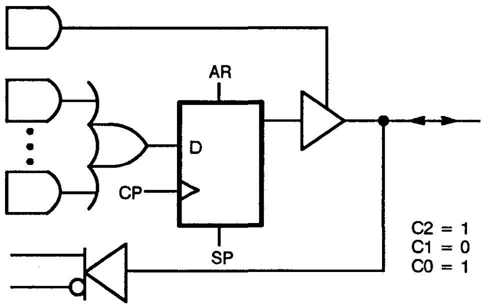


I/O FEEDBACK, COMBINATORIAL, ACTIVE-HIGH OUTPUT

Figure 1. PAL22V10C and PAL22VP10C Macrocell Configurations



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

Figure 2. Additional Macrocell Configurations for the PAL22VP10C

Selection Guide

			22V10C-10 22VP10C-10	22V10C-12 22VP10C-12	22V10C-15 22VP10C-15
I_{CC} (mA)	Com'l		190	190	
	Mil				190
t_{PD} (ns)	Com'l		10	12	
	Mil				15
t_S (ns)	Com'l		3.6	4.5	
	Mil				7.5
t_{CO} (ns)	Com'l		7.5	9.5	
	Mil				10
f_{MAX} (MHz)	Com'l		90	71	
	Mil				57

4

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... -65°C to +150°C

Ambient Temperature with
Power Applied .... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... -0.5V to V_{CC} Max

DC Input Voltage .... -0.5V to +5.5V

DC Input Current .... -30 mA to +5 mA
(Except during programming)

DC Programming Voltage 10V

Static Discharge Voltage .... >2001V
(per MIL-STD-883 Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ± 5%
Military[6]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.2 mA	Com'l	2.4		V
			I_{OH} = -2 mA	Mil			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[2]			2.0		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[2]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$, V_{CC} = Max.			-250	50	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \leq V_{OUT} \leq V_{CC}$			-100	100	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[3]			-30	-90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		Com'l		190	mA
				Mil		190	mA

Notes:

2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
4. Tested initially and after any design or process changes that may affect these parameters.
5. AC test load used for all parameters except where noted.
6. T_A is the "instant on" case temperature.

Switching Characteristics PAL22V10C/PAL22VP10C[5]

Parameters	Description	Commercial						Military				Units
				-10		-12				-15		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[13]				10		12				15	ns
t_{EA}	Input to Output Enable Delay				10		12				15	ns
t_{ER}	Input to Output Disable Delay[8]				10		12				15	ns
t_{CO}	Clock to Output Delay[13]				7.5		9.5				10	ns
t_S	Input or Feedback Set-Up Time			3.6		4.5				7.5		ns
t_H	Input Hold Time			0		0				0		ns
t_P	External Clock Period ($t_{CO} + t_S$)			11.1		14				17.5		ns
t_{WH}	Clock Width HIGH[4]			2.5		3				6		ns
t_{WL}	Clock Width LOW[4]			2.5		3				6		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[9]			90		71				57		MHz
f_{MAX2}	Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[4, 10]			200		166				83		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[11]			100		83				66		MHz
t_{CF}	Register Clock to Feedback Input[12]				6.4		7.5				7.5	ns
t_{AW}	Asynchronous Reset Width			10		12				15		ns
t_{AR}	Asynchronous Reset Recovery Time			6		7				10		ns
t_{AP}	Asynchronous Reset to Registered Output Delay				12		14				20	ns
t_{SPR}	Synchronous Preset Recovery Time			6		7				10		ns
t_{PR}	Power-Up Reset Time[14]			1.0		1.0				1.0		µs

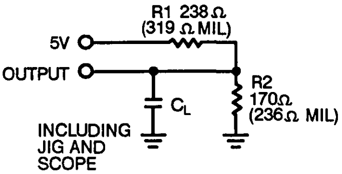
Notes:

7. This parameter is sample tested periodically with the device clocked at f_{MAX} external (f_{MAX1}) with all registers cycling on each cycle and outputs disabled (in high Z state).
8. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous high level has fallen to 0.5 volts below V_{OH} Min. or a previous low level has risen to 0.5 volts above V_{OL} Max.
9. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
10. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
12. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see note 11) minus t_S.
13. This specification is guaranteed for all device outputs changing state in a given access cycle.
14. The registers in the PAL22V10C/PAL22VP10C have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

Capacitance[4]

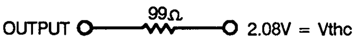
Parameters	Description	Typ.	Max.	Units
C_{IN}	Input Capacitance	11		pF
C_{OUT}	Output Capacitance	9		pF

AC Test Loads and Waveforms



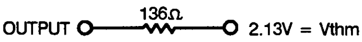
Specification	C_L	Package	Measurement Level
t_{PD}, t_{CO}, t_{CF}	15 pF	PDIP, CDIP	1.5V
	50 pF	PLCC, LCC	
t_{EA}	15 pF	PDIP, CDIP	See t_{EA} Waveform
	50 pF	PLCC, LCC	
t_{ER}	5 pF	All	See t_{ER} Waveform

Equivalent to: THÉVENIN EQUIVALENT



Commercial PIOF-5

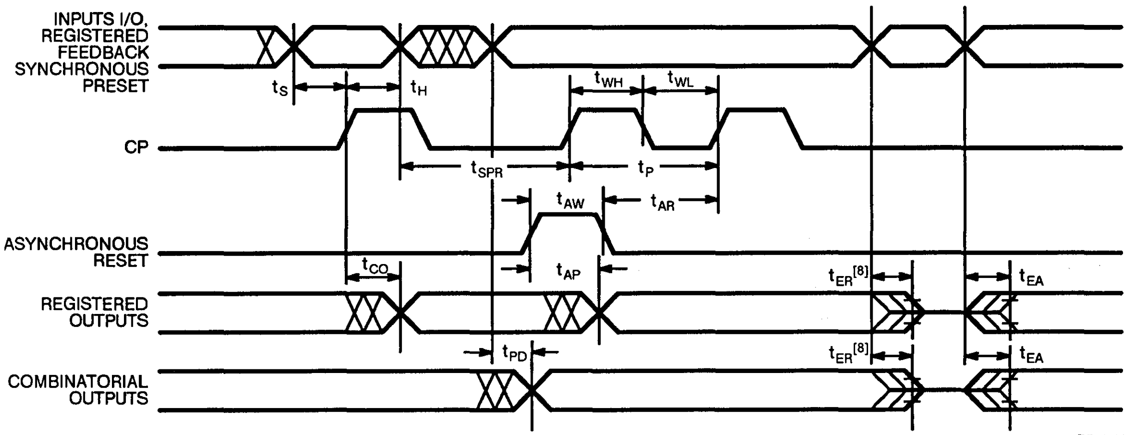
Equivalent to: THÉVENIN EQUIVALENT



Military PIOF-6

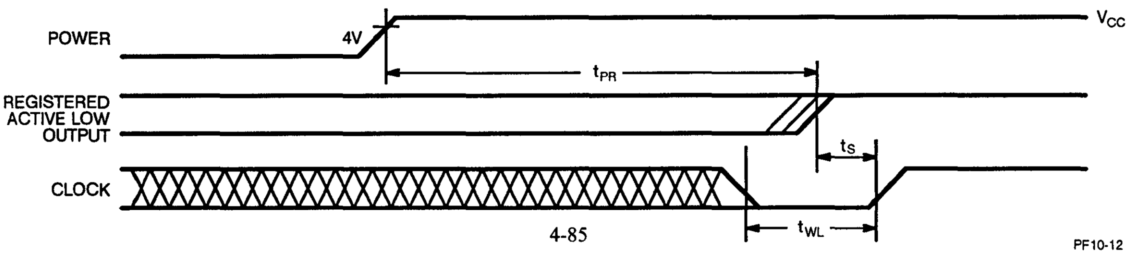
Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	V_{OH} 0.5V V_X PIOF-7
$t_{ER(+)}$	2.6V	V_{OL} 0.5V V_X PIOF-8
$t_{EA(+)}$	V_{thc}	V_X 0.5V V_{OH} PIOF-9
$t_{EA(-)}$	V_{thc}	V_X 0.5V V_{OL} PIOF-10

Switching Waveform



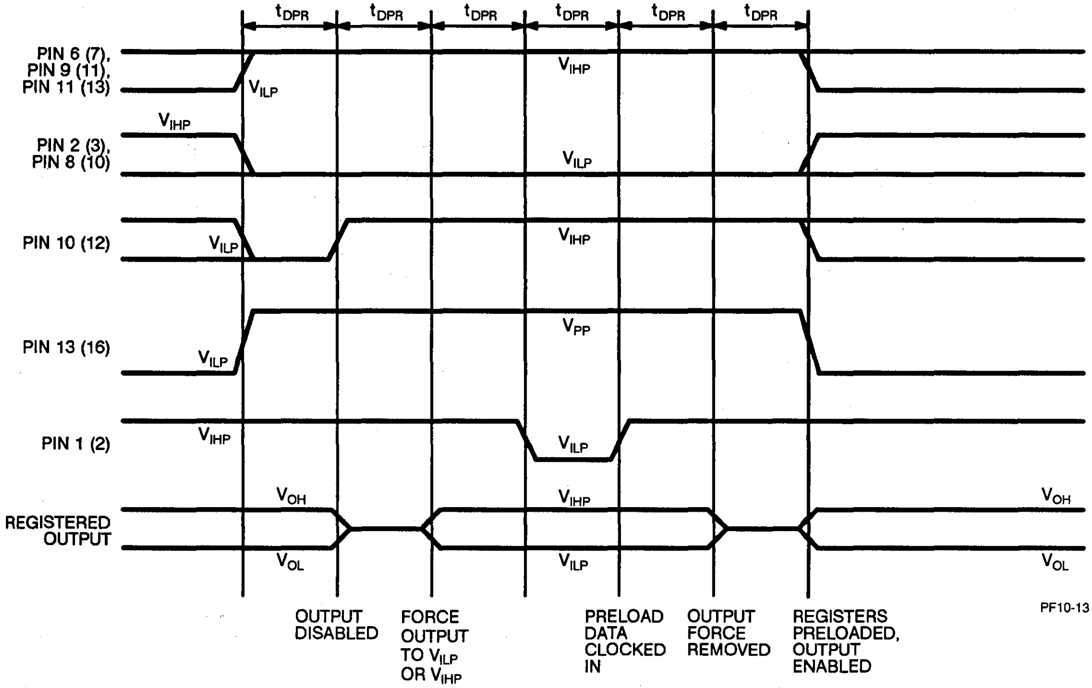
PF10-11

Power-Up Reset Waveform [14]



PF10-12

Preload Waveform

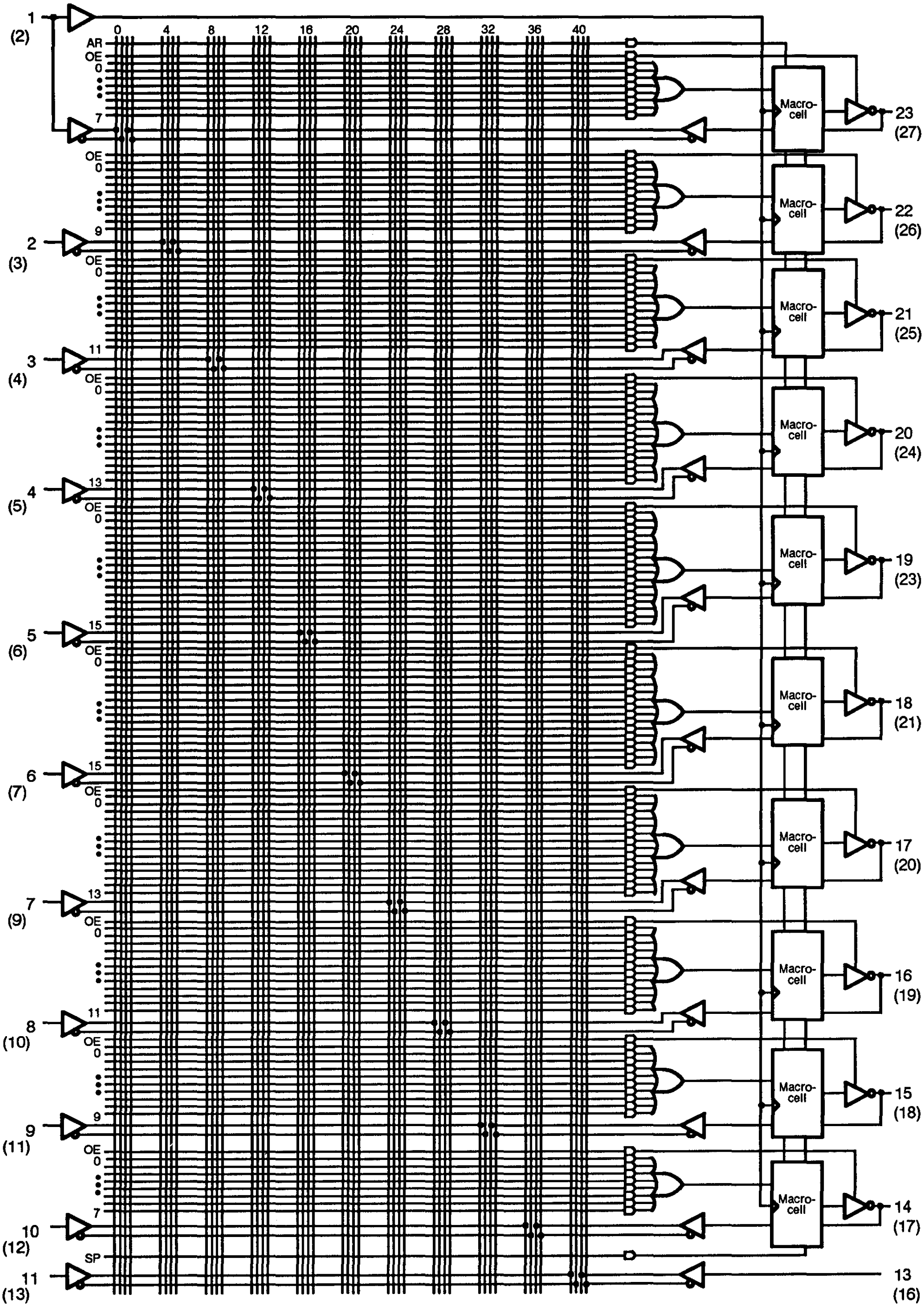


DIP (PLCC, LCC) Pinouts

Forced level on register pin during preload	Register Q output state after preload
V_{IHP}	High
V_{ILP}	Low

Name	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR}	Delay for Preload	1		µs
V_{ILP}	Input Low Voltage	0	0.4	V
V_{IHP}	Input High Voltage	3	4.75	V

Functional Logic Diagram for PAL22V10C/PAL22VP10C



DIP (PLCC and LCC) Pinouts

P10C-14

Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Type	Operating Range
190	10	90	PAL22V10C-10PC	P13	Commercial
			PAL22V10C-10DC	D14	
			PAL22V10C-10JC	J64	
			PAL22VP10C-10PC	P13	
			PAL22VP10C-10DC	D14	
			PAL22VP10C-10JC	J64	
	12	71	PAL22V10C-12PC	P13	Commercial
			PAL22V10C-12DC	D14	
			PAL22V10C-12JC	J64	
			PAL22VP10C-12PC	P13	
			PAL22VP10C-12DC	D14	
			PAL22VP10C-12JC	J64	
	15	57	PAL22V10C-15DMB	D14	Military
			PAL22V10C-15LMB	L64	
			PAL22VP10C-15DMB	D14	
			PAL22VP10C-15LMB	L64	

Document #: 38-A-00020A

CY7C330

CMOS Programmable Synchronous State Machine

CYPRESS SEMICONDUCTOR

Features

- 12 I/O macro cells each having:
  - registered, three-state I/O pins
  - input register clock select multiplexer
  - feed back multiplexer
  - output enable (OE) multiplexer
- All twelve macro cell state registers can be hidden
- User configurable state registers—JK, RS, T, or D
- Input multiplexer per pair of I/O macro cells allows I/O pin associated with a hidden macro cell state register to be saved for use as an input
- 4 dedicated hidden registers
- 11 dedicated, registered inputs
- 3 separate clocks—2 inputs, 1 output
- Common (PIN 14 controlled) or product term controlled output enable for each I/O pin
- 256 product terms—32 per pair of macro cells, variable distribution
- Global, synchronous, product term controlled, state register set and reset—inputs to product term are clocked by input clock
- 66 MHz operation
  - 3 ns input setup and 12 ns clock to output
  - 15 ns input register clock to state register clock
- Low power
  - 130 mA I_{CC}
- 28 pin 300 mil DIP, LCC
- Erasable and reprogrammable

Product Characteristics

The CY7C330 is a high-performance, eraseable, programmable, logic device (EPLD) whose architecture has been optimized to enable the user to easily and efficiently construct very high performance synchronous state machines.

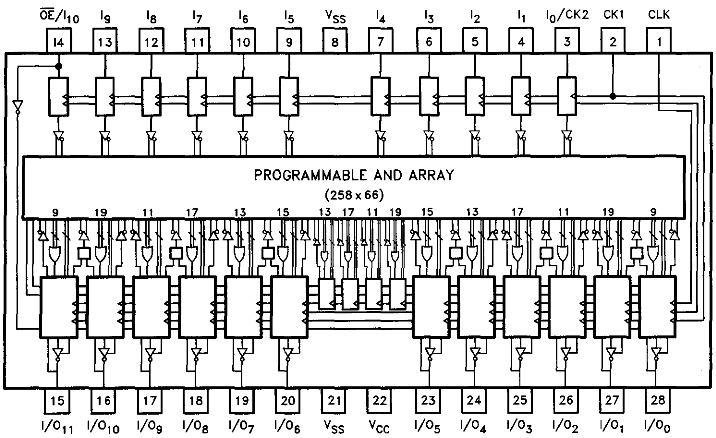
The unique architecture of the CY7C330, consisting of the user-configurable output macrocell, bi-directional I/O capability, input registers, and three separate clocks, enables the user to design high performance state machines that can communicate either with each other or with microprocessors over bi-directional parallel busses of user-definable widths.

The three separate clocks permit independent, synchronous state machines to be synchronized to each other. The two input clocks, C1, C2, enable the state machine to sample input signals that may be generated by another system and that may be available on its bus for a short period of time.

The user-configurable state register flip-flops enable the designer to designate JK, RS, T, or D type devices, so that the number of product terms required to implement the logic is minimized.

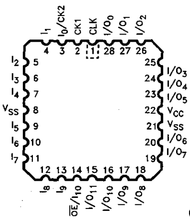
4

Block Diagram and DIP Pinout



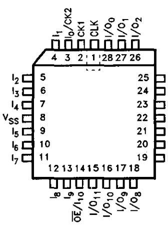
0101-1

LCC Pinout



0101-14

PLCC Pinout



0101-15

Selection Guide

		CY7C330-66	CY7C330-50	CY7C330-40	CY7C330-33	CY7C330-28
Maximum Operating Frequency (MHz)	Commercial	66.6	50.0		33.3	
	Military		50.0	40.0		28.5
Power Supply Current I_{CC1} (mA)	Commercial	140	130		130	
	Military		160	150		150

Product Characteristics (Continued)

The major functional blocks of the CY7C330 are (1) the input registers and (input) clock multiplexers, (2) the EPROM (AND) cell array, (3) the twelve I/O macrocells and (4) the four hidden registers.

Input Registers and Clock Multiplexers

There are a total of eleven dedicated Input Registers. Each Input Register consists of a D flip-flop and a clock multiplexer. The clock multiplexer is user-programmable to select either CK1 or CK2 as the clock for the flip-flop. CK2 and $\overline{OE}$ can alternatively be used as inputs to the array. The twenty-two outputs of the registers (i.e. the Q and $\overline{Q}$ outputs of the input registers) drive the array of EPROM cells.

An architecture configuration bit (C4) is reserved for each Dedicated Input Register cell to allow selection of either input clock CK1 or CK2 as the input register clock for each Dedicated Input Cell. If the CK2 clock is not needed that input may also be used as a general purpose array input. In this case the Input Register for this input can only be clocked by input clock CK1. *Figure 1* illustrates the Dedicated Input Cell composed of input register, Input Clock Multiplexer, and architecture configuration bit C4 which determines the input clock selected.

I/O Macro Cell

The logic diagram of the CY7C330 I/O macro cell is shown in *Figure 2.* There are a total of twelve indentical macro cells.

Each macro cell consists of:

— An Output State Register which is clocked by the global state counter clock, CLK (PIN 1). The State Register can be configured as a D, JK, RS, or T flip-flop (default is a D-type flip-flop). Polarity can be controlled in the D flip-flop implementation by use of the exclusive or function. Data is sampled on the LOW to HIGH clock transition. All of the State Registers have a common reset and set which are controlled synchronously by Product Terms which are generated in the EPROM cell array.

— A Macro Cell Input Register which may be clocked by either the CK1 or CK2 input clock as programmed by the user by use of architecture configuration bit C2 which controls the I/O Macro Cell Input Clock Multiplexer. The Macro Cell Input Registers are initialized on power up such that all of the Q outputs are at logic LOW level and the $\overline{Q}$ outputs are at a logic HIGH level.

— An Output Enable Multiplexer (OE), which is user-programmable, by architecture configuration bit C0, to select either the common $\overline{OE}$ signal from pin 14 or, for each cell individually, the signal from the Output Enable product term associated with each macro cell. The Output Enable input signal to the array product term is clocked through the input register by the selected input register clock, CK1 or CK2.

— An input Feed Back Multiplexer which is user-programmable to select either the output of the State Register or the output of the Macro Cell Input Register to be fed back into the array. This option is programmed by architecture configuration bit C1. If the output of the Macro Cell Input Register is selected by the Feed Back Multiplexer, the I/O pin becomes bi-directional.

Macro Cell Input Multiplexer

Each pair of I/O macro cells share a Macro Cell Input Multiplexer which selects the output of one or the other of the pair's input registers to be fed to the input array. This multiplexer is shown in *Figure 2.* The Macro Cell Input Multiplexer allows the input pin of a macro cell, for which the state register has been hidden by feeding back its input to the input array, to be preserved for use as an input pin. This is possible as long as the other macro cell of the pair is not needed as a input or does not require State Register feed back. The input pin input register output which would normally be blocked by the hidden State Register feed back can be routed to the array input path of the companion macro cell for use as array input.

State Registers

By use of the exclusive or gate the State Register may be configured as a JK, RS or T Register. The default is a D-Type register. For the D-Type register, the exclusive or function can be used to select the polarity or the register output.

The set and reset of the State Register are global synchronous signals which are controlled by the logic of two global product terms for which input signals are clocked through the input registers by either of the input clocks, CK1 or CK2.

Hidden Registers

In addition to the twelve macro cells, which contain a total of twenty-four registers, there are four hidden registers whose outputs are not brought out to the device output pins. The Hidden State Register Macro Cell is shown in *Figure 3.*

The four hidden registers are clocked by the same clock as the macrocell state registers. All of the hidden register flip-flops have a common, synchronous set, S, as well as a common, synchronous reset, R, which over-ride the data at the D input. The S and R signals are PRODUCT TERMS that are generated in the array and are the same signals used to preset and reset the state register flip-flops.

Macrocell Product Term Distribution

Each pair of macrocells has a total of thirty-two product terms. Two product terms of each macrocell pair are used for the output enables (OEs) for the two output pins. Two product terms are also used as one input to each of the two exclusive OR gates in the macrocell pair. The number of product terms available to the designer is then $32 - 4 = 28$ for each macrocell pair. These product terms are divided between the macro cell state register flip-flops as shown in Table 1.

Table 1. Product Term Distribution

Macro Cell	Pin No.	Product Terms
0	28	9
1	27	19
2	26	11
3	25	17
4	24	13
5	23	15
6	20	15
7	19	13
8	18	17
9	17	11
10	16	19
11	15	9

Product Characteristics (Continued)

Hidden State Register Product Term Distribution

Each pair of hidden registers also has a total of 32 product terms. Two product terms are used as one input to each of the exclusive OR gates. However, because the register outputs do not go to any output pins, output enable product terms are not required. Therefore, 30 product terms are available to the designer for each pair of hidden registers. The product term distribution for the four hidden registers are shown in Table 2.

Table 2. Hidden State Register Product Term Distribution

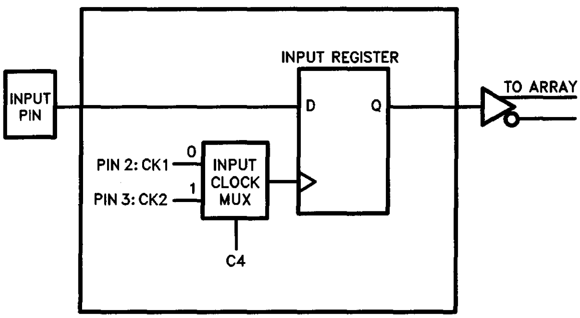
Hidden Register Cell	Product Terms
0	19
1	11
2	17
3	13

Architecture Configuration Bits

The architecture configuration bits are used to program the multiplexers. The function of the architecture bits is outlined below.

Table 3. Architecture Configuration Bits

Architecture Configuration Bit		Number of Bits	Value	Function
C0	Output Enable Select MUX	12 Bits, 1 Per I/O Macro Cell	0—Virgin State	Output Enable Controlled by Product Term
			1—Programmed	Output Enable Controlled by Pin 14
C1	State Register Feed Back MUX	12 Bits, 1 Per I/O Macro Cell	0—Virgin State	State Register Output is Fed Back to Input Array
			1—Programmed	I/O Macro Cell is Configured as an Input and Output of Input Register is Fed to Array
C2	I/O Macro Cell Input Register Clock Select MUX	12 Bits, 1 Per I/O Macro Cell	0—Virgin State	CK1 Input Register Clock (Pin 2) is Connected to I/O Macro Cell Input Register Clock Input
			1—Programmed	CK2 Input Register Clock (Pin 3) is Connected to I/O Macro Cell Input Register Clock Input
C3	I/O Macro Cell Pair Input Select MUX	6 Bits, 1 Per I/O Macro Cell Pair	0—Virgin State	Selects Data from I/O Macro Cell Input Register of Macro Cell A of Macro Cell Pair
			1—Programmed	Selects Data from I/O Macro Cell Input Register of Macro Cell B of Macro Cell Pair
C4	Dedicated Input Register Clock Select MUX	11 Bits, 1 Per Dedicated Input Cell	0—Virgin State	CK1 Input Register Clock (Pin 2) is Connected to Dedicated Input Register Clock Input
			1—Programmed	CK2 Input Register Clock (Pin 3) is Connected to Dedicated Input Register Clock Input



0101-5

Figure 1. Dedicated Input Cell

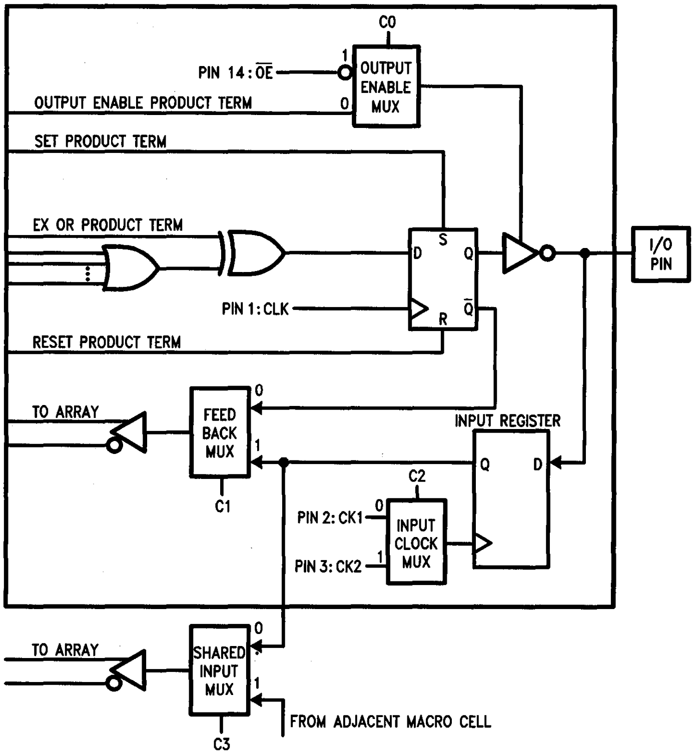


Figure 2. I/O Macro Cell and Shared Input Multiplexer

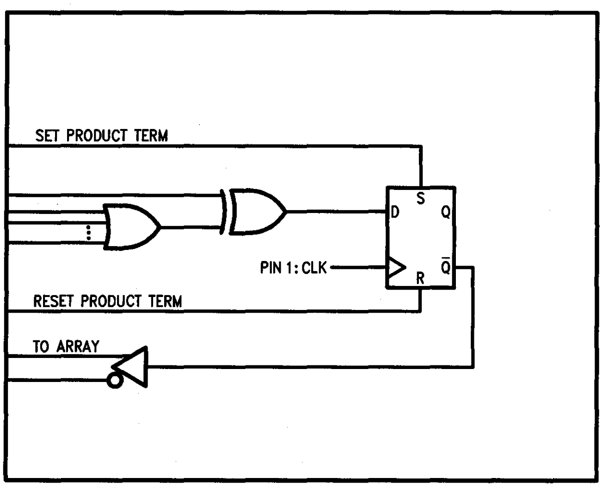


Figure 3. Hidden State Register Macro Cell

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 12 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015)

Latchup Current .... >200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[5]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[6]

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −3.2 mA	COM'L	2.4		V
			I_{OH} = −2 mA	MIL			
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 12 mA	COM'L		0.5	V
			I_{OL} = 8 mA	MIL			
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs[1]			2.2		V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs[1]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max. $V_{SS} \le V_{OUT} \le V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		COM'L (-66 MHz)		140	mA
				COM'L		130	mA
				MIL (-50 MHz)		160	mA
				MIL		150	mA
I_{CC2}	Power Supply Current at Frequency [3,7]	V_{CC} = Max. Outputs Disabled (in High Z State) Device Operating at f_{MAX} External (f_{MAX1})		COM'L (-33 MHz & -50 MHz)		160	mA
				COM'L (-66 MHz)[15]		180	mA
				MIL (-28 MHz & -40 MHz)		180	mA
				MIL (-50 MHz)[15]		200	mA

Capacitance[3]

Parameters	Description	Test Conditions	Min	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		8	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. *Figure 4a* test load used for all parameters except t_{CEA}, t_{CER}, t_{PZX} and t_{PXZ}. *Figure 4b* test load for t_{CEA}, t_{CER}, t_{PZX}, t_{PXZ}.
5. T_A is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.
7. This parameter is sample tested periodically.
8. This parameter is measured as the time after output register disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous high level has fallen to 0.5V below V_{OH} Min or a previous low level has risen to 0.5V above V_{OL} Max. Please see *Figure 6* for enable and disable test waveforms and measurement reference levels.
9. This parameter is measured as the time after output register clock input that the previous output data state remains stable on the output.
10. This difference parameter is designed to guarantee that any CY7C330 output fed back to its own inputs externally or internally will satisfy the input register minimum input hold time. This parameter is guaranteed for a given individual device and is tested by a periodic sampling of production product.
11. This specification is intended to guarantee feeding of this signal to another 33X family input register cycled by the same clock with sufficient output data stable time to insure that the input hold time minimum of the following input register is satisfied. This parameter difference specification is guaranteed by periodic sampling of production product of CYC330 and CY7C332. This difference parameter is guaranteed to be met only for devices at the same ambient temperature and V_{CC} supply voltage.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feed back can operate.
13. This specification indicates the guaranteed maximum frequency at which an individual input or output register can be cycled.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with only internal feedback can operate. This parameter tested periodically on a sample basis.

Switching Characteristics Over the Operating Range[4, 6]

Parameters	Description	Commercial						Military						Units
		-66		-50		-33		-50		-40		-28		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{IS}	Input or Feedback Setup Time to Input Register Clock	3		5		10		5		5		10		ns
t_{OS}	Input Register Clock to Output Register Clock	15		20		30		20		25		35		ns
t_{CO}	Output Register Clock to Output Delay		12		15		20		15		20		25	ns
t_{IH}	Input Register Hold Time	5		5		5		5		5		5		ns
t_{CEA}	Input Register Clock To Output Enable Delay		20		20		30		20		25		35	ns
t_{CER}	Input Register Clock to Output Disable Delay[8]		20		20		30		20		25		35	ns
t_{PZX}	Pin 14 Enable to Output Enable Delay		20		20		30		20		25		35	ns
t_{PXZ}	Pin 14 Disable to Output Disable Delay[8]		20		20		30		20		25		35	ns
t_{WH}	Input or Output Clock Width High[3, 7]	6		8		12		8		10		15		ns
t_{WL}	Input or Output Clock Width Low[3, 7]	6		8		12		8		10		15		ns
t_P	External Clock Period ($t_{CO} + t_{IS}$) Input and Output Clock Common	15		20		30		20		25		35		ns
t_{OH}	Output Data Stable Time from Synchronous Clock Input[9]	3		3		3		3		3		3		ns
$t_{OH}-t_{IH}$	Output Data Stable Time This Device Minus I/P Reg Hold Time Same Device[10]	0		0		0		0		0		0		ns
$t_{OH}-t_{IH}$ 33X	Output Data Stable Time Minus I/P Reg Hold Time 7C330 & 7C332[11]	0		0		0		0		0		0		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_{IS})$)[12]	66.6		50.0		33.3		50.0		40.0		28.5		MHz
f_{MAX2}	Maximum Register Toggle Frequency ($1/(t_{WH} + t_{WL})$)[7, 13]	83.3		62.5		41.6		62.5		50.0		33.3		MHz
f_{MAX3}	Internal Maximum Frequency[14]	74.0		57.0		37.0		57.0		45.0		30.0		MHz

AC Test Loads and Waveforms (Commercial)

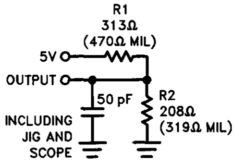
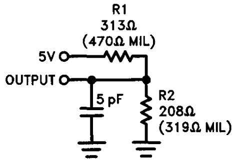
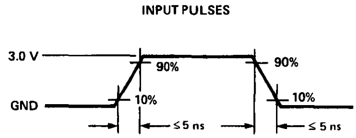


Figure 4a



0101-9

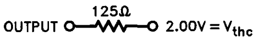
Figure 4b



0101-10

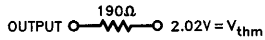
Figure 5

Equivalent to: THEVENIN EQUIVALENT (Commercial)



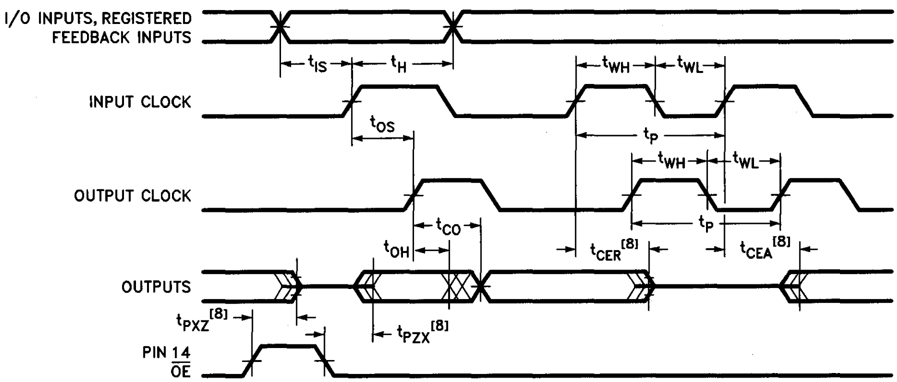
0101-11

Equivalent to: THEVENIN EQUIVALENT (Military)

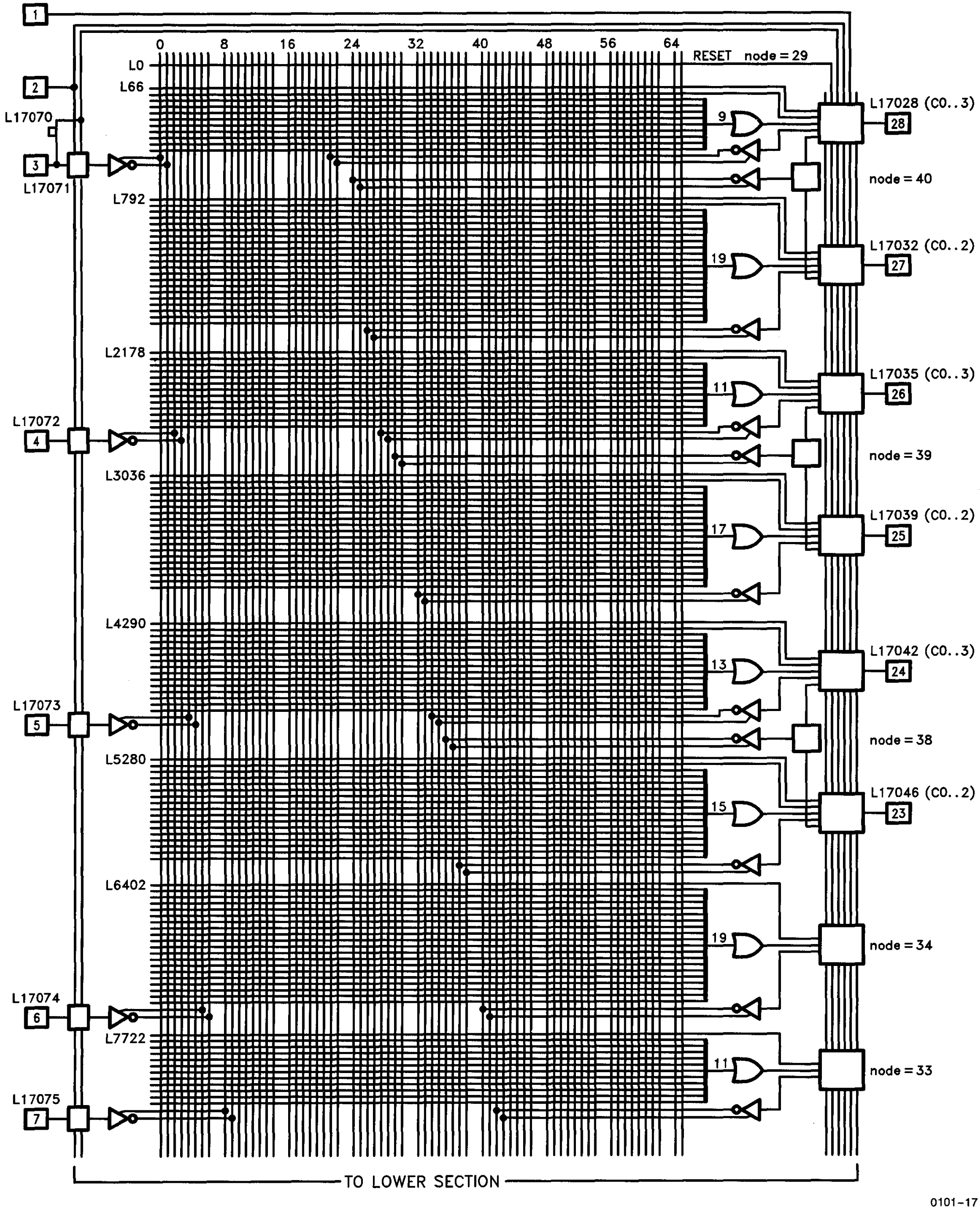


0101-12

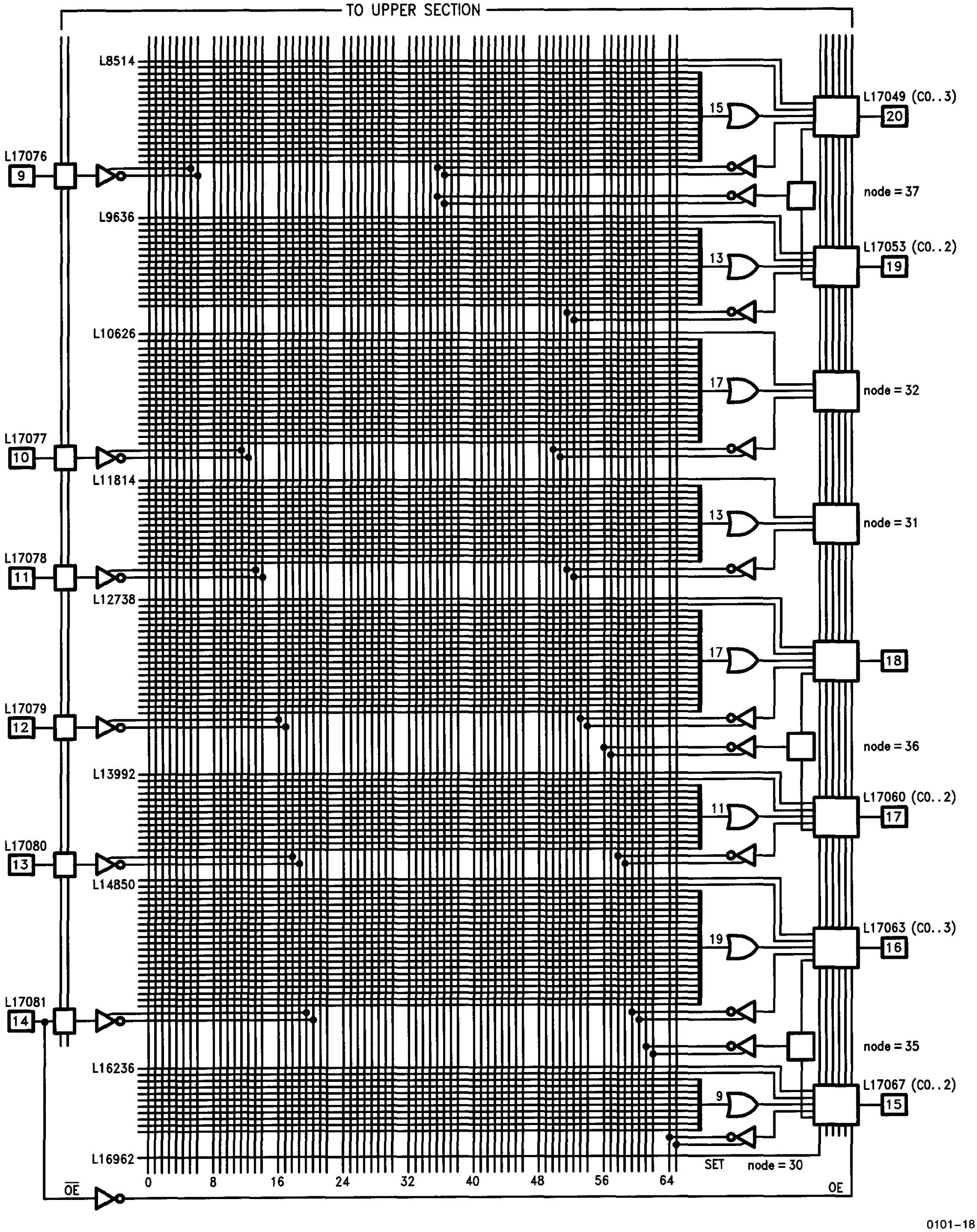
Switching Waveforms



0101-13



CY7C330 Block Diagram (Page 1 of 2)



CY7C330 Block Diagram (Page 2 of 2)

4

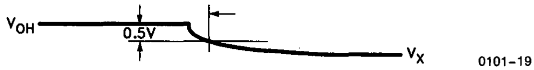
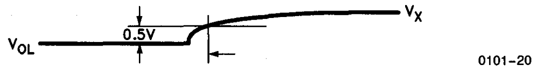
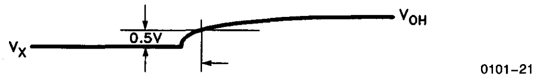
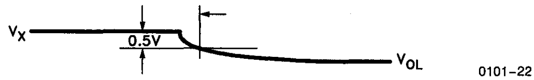
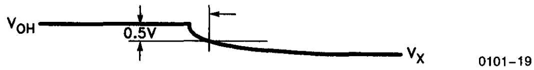
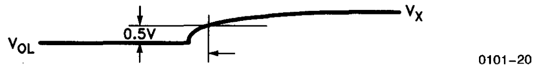
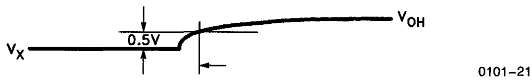
Parameter	V_x	Output Waveform—Measurement Level
$t_{PXZ}(-)$	1.5V	
$t_{PXZ}(+)$	2.6V	
$t_{PZX}(+)$	V_{thc}	
$t_{PZX}(-)$	V_{thc}	
$t_{CER}(-)$	1.5V	
$t_{CER}(+)$	2.6V	
$t_{CEA}(+)$	V_{thc}	
$t_{CEA}(-)$	V_{thc}	

Figure 6. Test Waveforms

Ordering Information

f_{max} (MHz)	I_{CC1} (mA)	Ordering Code	Package	Operating Range
66.6	140	CY7C330-66PC	P21	Commercial
		CY7C330-66WC	W22	
		CY7C330-66JC	J64	
		CY7C330-66HC	H64	
50	160	CY7C330-50DMB	D22	Military
		CY7C330-50WMB	W22	
		CY7C330-50HMB	H64	
		CY7C330-50LMB	L64	
		CY7C330-50TMB	T74	
		CY7C330-50QMB	Q64	
50	130	CY7C330-50PC	P21	Commercial
		CY7C330-50WC	W22	
		CY7C330-50JC	J64	
		CY7C330-50HC	H64	
40	150	CY7C330-40DMB	D22	Military
		CY7C330-40WMB	W22	
		CY7C330-40HMB	H64	
		CY7C330-40LMB	L64	
		CY7C330-40TMB	T74	
		CY7C330-40QMB	Q64	
33.3	130	CY7C330-33PC	P21	Commercial
		CY7C330-33WC	W22	
		CY7C330-33JC	J64	
		CY7C330-33HC	H64	
28.5	150	CY7C330-28DMB	D22	Military
		CY7C330-28WMB	W22	
		CY7C330-28HMB	H64	
		CY7C330-28LMB	L64	
		CY7C330-28TMB	T74	
		CY7C330-28QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{ISU}	7,8,9,10,11
t_{OSU}	7,8,9,10,11
t_{CO}	7,8,9,10,11
t_H	7,8,9,10,11
t_{CEA}	7,8,9,10,11
t_{PZX}	7,8,9,10,11

Document #: 38-00064-C

CY7C331
Asynchronous Registered EPLD

Features

- 12 I/O macrocells each having:
  - One state Flip-Flop with an XOR sum or products input
  - One feedback Flip-Flop with input coming from the I/O pin
  - Independent (product term) set, reset, and clock inputs on all registers
  - Asynchronous bypass capability on all registers, under product term control (r = s = 1)
  - Global or local output enable on tristate I/O
  - Feedback from either register to the array
- 192 product terms with variable distribution to macrocells
- 13 inputs, 12 feedback I/O pins, plus 6 shared I/O macrocell feedbacks for a total of 31 true and complementary inputs
- High speed: 20 t_{PD} ns maximum
- Security bit
- Space saving 28 pin slim-line DIP package; also available in 28 pin PLCC
- Low power
  - 90 mA typical I_{CC} quiescent
  - 180 mA I_{CC} maximum
  - UV-Eraseable and reprogrammable
  - Programming and operation 100% testable

Product Characteristics

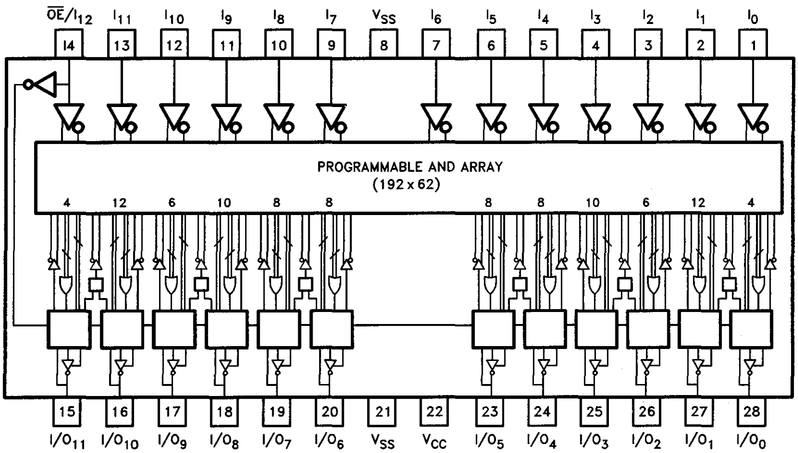
The CY7C331 is the most versatile PLD available for asynchronous designs. Central resources include 12 full D-type Flip-Flops with separate set, reset and clock capability. For increased utility, XOR gates are provided at the D-inputs and the product term allocation per Flip-Flop is variably distributed.

I/O Resources

Pins 1 through 7 and 9 through 14 serve as array inputs; pin 14 may also be used as a global output enable for the I/O macrocell tristate outputs. Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be managed as inputs or outputs depending on the configuration and the macrocell OE terms.

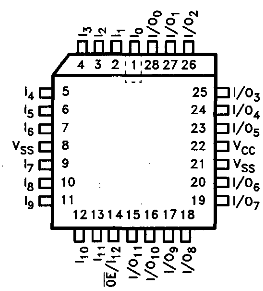
4

Block Diagram and DIP Pinout



0100-1

PLCC Pinout



0100-2

Selection Guide

Generic Part Number	I_{CC1} mA		t_{PD} ns		t_S ns		t_{CO} ns	
	Com	Mil	Com	Mil	Com	Mil	Com	Mil
CY7C331-20	130		20		12		20	
CY7C331-25	120	160	25	25	12	15	25	25
CY7C331-30		150		30		15		30
CY7C331-35	120		35		15		35	
CY7C331-40		150		40		20		40

I/O Resources (Continued)

It should be noted that there are two ground connections (pins 8 and 21) which, together with V_{CC} (pin 22) are located centrally on the package. The reason for this placement and dual ground structure is to minimize the ground-loop noise when the outputs are driving simultaneously into a heavy capacitive load.

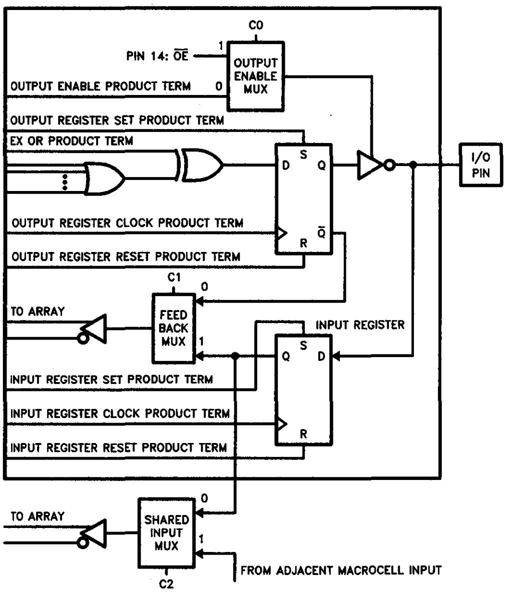


Figure 1. Macrocell

The CY7C331 has 12 macrocells. Each macrocell has two D-type Flip-Flops. One is fed from the array, and one is fed from the I/O pin. For each Flip-Flop there are 3 dedicated product terms driving the R, S, and Clock inputs respectively. Each macrocell has one input to the array and for each pair of macrocells there is one shared input to the array. The macrocell input to the array may be configured to come from the 'Q' output of either Flip-Flop.

The D-type Flip-Flop which is fed from the array (i.e., the state Flip-Flop) has a logical XOR function on its input which combines a single product term with a sum (OR) of a number of product terms. The single product term is used to set the polarity of the output or to implement toggling (by including the current output in the product term).

The R and S inputs to the Flip-Flops override the current setting of the 'Q' output. The S input sets 'Q' true and the R input 'resets' 'Q' (sets it false). If both R and S are asserted (true) at once, then the output will follow the input ('Q' = 'D').

Table 1

R	S	Q
1	0	0
0	1	1
1	1	D
R-S Truth Table		

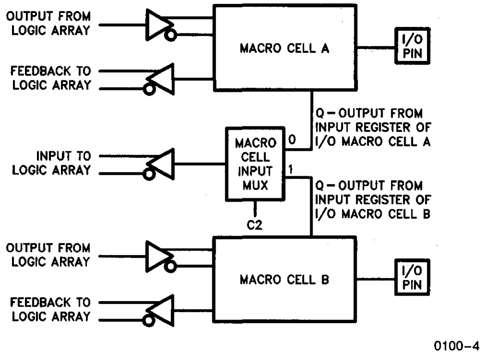


Figure 2. Shared Input Multiplexer

Shared Input Multiplexer

The input associated with each pair of macrocells may be configured by the shared input multiplexer to come from either macrocell; the 'Q' output of the Flip-Flop coming from the I/O pin is used as the input signal source.

Product Term Distribution

The product terms are distributed to the macrocells such that 32 product terms are distributed between two adjacent macrocells. The pairing of macrocells is the same as it is for the shared inputs. 8 of the product terms are used in each macrocell for set, reset, clock, OE and the upper part of the XOR gate. This leaves 16 product terms per pair of macrocells to be divided between the sum-of-product inputs to the two state registers. The following table shows the I/O pin pairing for shared inputs, and the product term (P-Term) allocation to macrocells associated with the I/O pins.

Table 2

Macrocell	Pin Number	Product Terms
0	28	4
1	27	12
2	26	6
3	25	10
4	24	8
5	23	8
6	20	8
7	19	8
8	18	10
9	17	6
10	16	12
11	15	4

The CY7C331 is configured by three arrays of configuration bits (C0, C1, C2). For each macrocell, there is one C0 bit and one C1 bit. For each pair of macrocells, there is one C2 bit.

There are 12 C0 bits. If C0 is programmed for a macrocell, then the tristate enable (OE) will be controlled by pin 14 (the global OE). If C0 is not programmed, then the OE product term for that macrocell will be used.

There is one C1 bit for each macrocell. The C1 bit selects input for the product term (PT) array from either the state register (if the bit is unprogrammed) or the input register.

I/O Resources (Continued)

There are 6 C2 bits, providing one C2 bit for each pair of macrocells. The C2 bit controls the shared input Multiplexer (Mux); if the C2 bit is not programmed, then the input to the product term array comes from the upper macrocell (A). If the C2 bit is programmed, then the input comes from the lower macrocell (B).

The timing diagrams for the CY7C331 cover state register, input register, and various combinational delays. Since internal clocks are the outputs of product terms, all timing is from the transition of inputs causing the clock transition.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Group Potential (Pin 22 to Pins 8 or 21) .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 12 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015)

Latchup Current .... >200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[5]	−55°C to +125°C	5V ±10%

4

Electrical Characteristics Over the Operating Range[6]

Parameters	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	$I_{OH} = -3.2$ mA	Commercial	2.4		V
			$I_{OH} = -2$ mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	$I_{OL} = 12$ mA	Commercial		0.5	V
			$I_{OL} = 8$ mA	Military			
V_{IH}	Input HIGH Level	Guaranteed HIGH Input, all Inputs[1]			2.2		V
V_{IL}	Input LOW Level	Guaranteed LOW Input, all Inputs[1]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$, $< V_{CC}$ = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} < V_{OUT} < V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open		Commercial (-20)		130	mA
				Commercial		120	mA
				Military (-25)		160	mA
				Military		150	mA
I_{CC2}	Power Supply Current at Frequency[19]	V_{CC} = Max. Outputs Disabled (in HIGH Z State) Device Operating at f_{MAX} External (f_{MAX1})		Commercial		180	mA
				Military		200	mA

Capacitance[3]

Parameters	Description	Test Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		8	

Notes:
1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. *Figure 3a* test load used for all parameters except t_{PZXI}, t_{PXZI}, t_{PZX} and t_{PXZ}. *Figure 3b* test load for t_{PZXI}, t_{PXZI}, t_{PZX} and t_{PXZ}. *Figure 3c* shows test waveforms and measurement levels.
5. T_A is the "instant on" case temperature.
6. See the last page of this specification for Group A subgroup testing information.

Switching Characteristics[6]

Parameters	Description	Commercial						Military						Units
		-20		-25		-35		-25		-30		-40		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		20		25		35		25		30		40	ns
t_{ICO}	Input Register Clock to Output Delay[8]		35		40		55		45		50		65	ns
t_{IOH}	Output Data Stable Time from Input Clock[8]	5		5		5		5		5		5		ns
t_{IS}	Input or Feedback Setup Time to Input Register Clock[8]	2		2		2		5		5		5		ns
t_{IH}	Input Register Hold Time from Input Clock[8]	11		13		15		13		15		20		ns
t_{IAR}	Input to Input Register Asynchronous Reset Delay[8]		35		40		55		45		50		65	ns
t_{IRW}	Input Register Reset Width[8]	35		40		55		45		50		65		ns
t_{IRR}	Input Register Reset Recovery Time[8]	35		40		55		45		50		65		ns
t_{IAS}	Input to Input Register Asynchronous Set Delay[8]		35		40		55		45		50		65	ns
t_{ISW}	Input Register Set Width[8]	35		40		55		45		50		65		ns
t_{ISR}	Input Register Set Recovery Time[8]	35		40		55		45		50		65		ns
t_{WH}	Input & Output Clock Width High[8, 9, 12]	12		15		20		15		20		25		ns
t_{WL}	Input & Output Clock Width Low[8, 9, 12]	12		15		20		15		20		25		ns
f_{MAX1}	Maximum Frequency with Feedback in Input Registered Mode $(1/(t_{ICO} + t_{IS}))$[13]	27.0		23.8		17.5		20.0		18.1		14.2		MHz
f_{MAX2}	Maximum Frequency Data Path in Input Registered Mode (Lower of $1/t_{ICO}$, $1/(t_{WH} + t_{WL})$ or $1/(t_{IS} + t_{IH})$)[8]	28.5		25.0		18.1		22.2		20.0		15.3		ns
$t_{IOH}-t_{IH}$ 33X	Output Data Stable from Input Clock Minus Input Register Input Hold Time for 7C330 and 7C332[15, 18]	0		0		0		0		0		0		ns
t_{CO}	Output Register Clock to Output Delay[9]		20		25		35		25		30		40	ns
t_{OH}	Output Data Stable Time from Output Clock[9]	3		3		3		3		3		3		ns
t_S	Output Register Input Set Up Time to Output Clock[9]	12		12		15		15		15		20		ns
t_H	Output Register Input Hold Time from Output Clock[9]	8		8		10		10		10		12		ns
t_{OAR}	Input to Output Register Asynchronous Reset Delay[9]		20		25		35		25		30		40	ns
t_{ORW}	Output Register Reset Width[9]	20		25		35		25		30		40		ns
t_{ORR}	Output Register Reset Recovery Time[9]	20		25		35		25		30		40		ns
t_{OAS}	Input to Output Register Asynchronous Set Delay[9]		20		25		35		25		30		40	ns
t_{OSW}	Output Register Set Width[9]	20		25		35		25		30		40		ns
t_{OSR}	Output Register Set Recovery Time[9]	20		25		35		25		30		40		ns
t_{EA}	Input to Output Enable Delay[4, 10]		25		25		35		25		30		40	ns
t_{ER}	Input to Output Disable Delay[4, 10]		25		25		35		25		30		40	ns
t_{PZX}	Pin 14 to Output Enable Delay[4, 10]		20		20		30		20		25		35	ns
t_{PXZ}	Pin 14 to Output Disable Delay[4, 10]		20		20		30		20		25		35	ns
f_{MAX3}	Maximum Frequency with Feedback in Output Registered Mode $(1/(t_{CO} + t_S))$[14, 17]	31.2		27.0		20.0		25.0		22.2		16.6		MHz
f_{MAX4}	Max. Frequency Data Path in Output Registered Mode (Lower of $1/t_{CO}$, $1/(t_{WH} + t_{WL})$ or $1/(t_S + t_H)$)[9]	41.6		33.3		25.0		33.3		25.0		20.0		MHz
$t_{OH}-t_{IH}$ 33X	Output Data Stable from Output Clock Minus Input Register Input Hold Time for 7C330 and 7C332[16, 18]	0		0		0		0		0		0		ns
f_{MAX5}	Maximum Frequency Pipelined Mode[12, 17]	35.0		30.0		22.0		28.0		23.5		18.5		MHz

Notes:

7. Refer to *Figure 5* configuration 1.
8. Refer to *Figure 5* configuration 2.
9. Refer to *Figure 5* configuration 3.
10. Refer to *Figure 5* configuration 4.
11. Refer to *Figure 5* configuration 5.
12. Refer to *Figure 5* configuration 6.
13. Refer to *Figure 6* configuration 7.
14. Refer to *Figure 6* configuration 8.
15. Refer to *Figure 7* configuration 9.
16. Refer to *Figure 7* configuration 10.
17. This specification is intended to guarantee that a state machine configuration created with internal or external feedback can be operated with output register and input register clocks controlled by the same source. These parameters are tested by periodic sampling of production product.
18. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C331. This specification is met for the devices noted operating at the same ambient temperature and at the same power supply voltage. These parameters are tested periodically by sampling of production product.

AC Test Loads and Waveforms

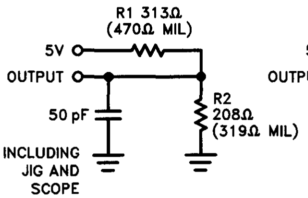


Figure 3a

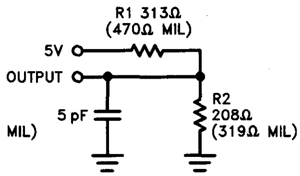
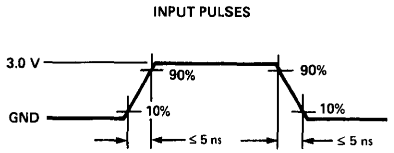


Figure 3b

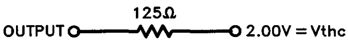
0100–5



0100–6

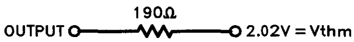
Figure 4

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



0100–7

Equivalent to: THÉVENIN EQUIVALENT (Military)



0100–8

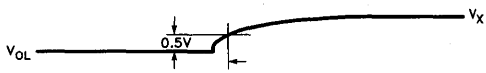
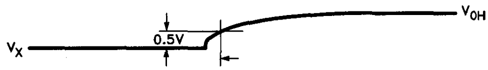
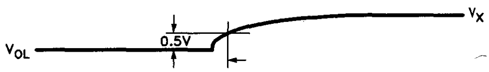
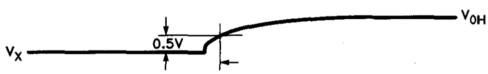
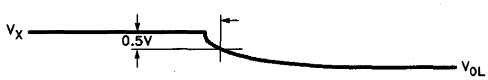
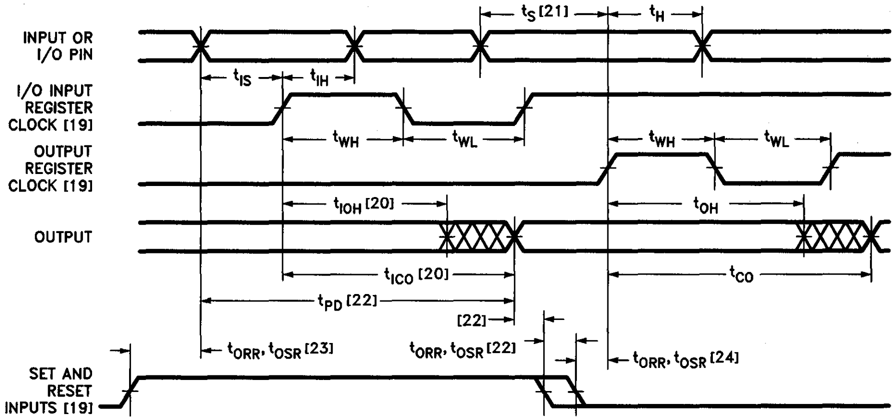
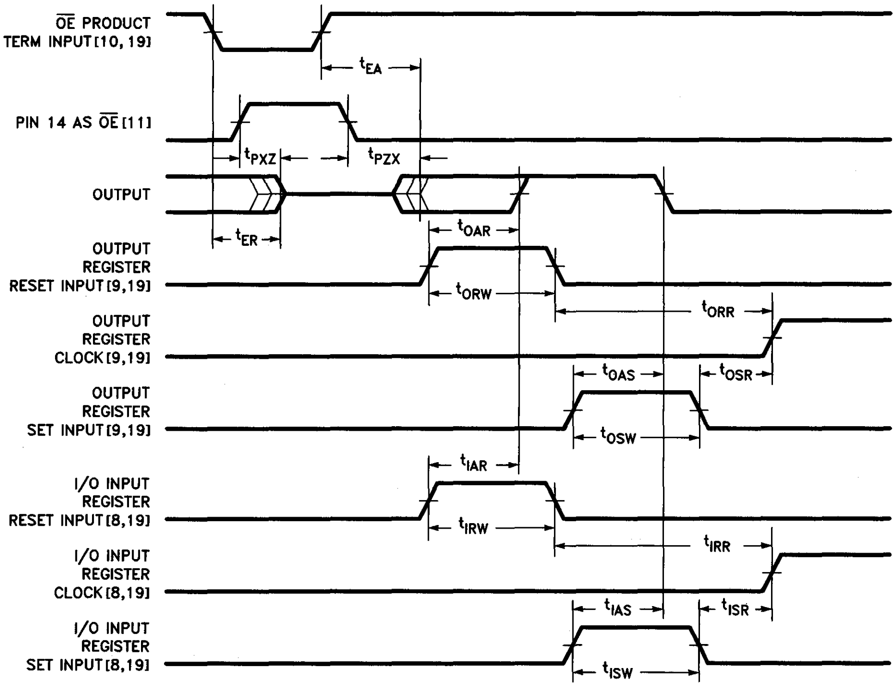
Parameters	V_X	Output Waveform—Measurement Level
$t_{PXZ}(-)$	1.5V	 V_{OH} 0.5V V_X 0100–16
$t_{PXZ}(+)$	2.6V	 V_X 0.5V V_{OL} 0100–17
$t_{PZX}(+)$	V_{thc}	 V_{OH} 0.5V V_X 0100–18
$t_{PZX}(-)$	V_{thc}	 V_X 0.5V V_{OL} 0100–19
$t_{ER}(-)$	1.5V	 V_{OH} 0.5V V_X 0100–16
$t_{ER}(+)$	2.6V	 V_X 0.5V V_{OL} 0100–17
$t_{EA}(+)$	V_{thc}	 V_{OH} 0.5V V_X 0100–18
$t_{EA}(-)$	V_{thc}	 V_X 0.5V V_{OL} 0100–19

Figure 3c. Test Waveforms and Measurement Levels

Switching Waveforms



0100–9



0100–10

Notes:

19. Because these input signals are controlled by product terms, active input polarity may be of either polarity. Internal active input polarity has been shown for clarity.
20. Output register is set in Transparent Mode. Output register Set and Reset inputs are in a HIGH state.
21. Dedicated input or input register set in Transparent Mode. Input register Set and Reset inputs are in a HIGH state.
22. Combinatorial Mode. Reset and Set inputs of the input and output registers should remain in a HIGH state at least until the output responds at t_{PD}. When returning Set and Reset inputs to a LOW state, one of these signals should go LOW a MINIMUM of t_{OSR} (Set input) or t_{ORR} (Reset input) prior to the other. This guarantees predictable register states upon exit from Combinatorial Mode.
23. When entering the Combinatorial Mode, input and output register Set and Reset inputs must be stable in a HIGH state a MINIMUM of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to application of logic input signals.
24. When returning to the input and/or output Registered Mode, register Set and Reset inputs must be stable in a LOW state a MINIMUM of t_{ISR} or t_{IRR} and t_{OSR} or t_{ORR} respectively prior to the application of the register clock input.

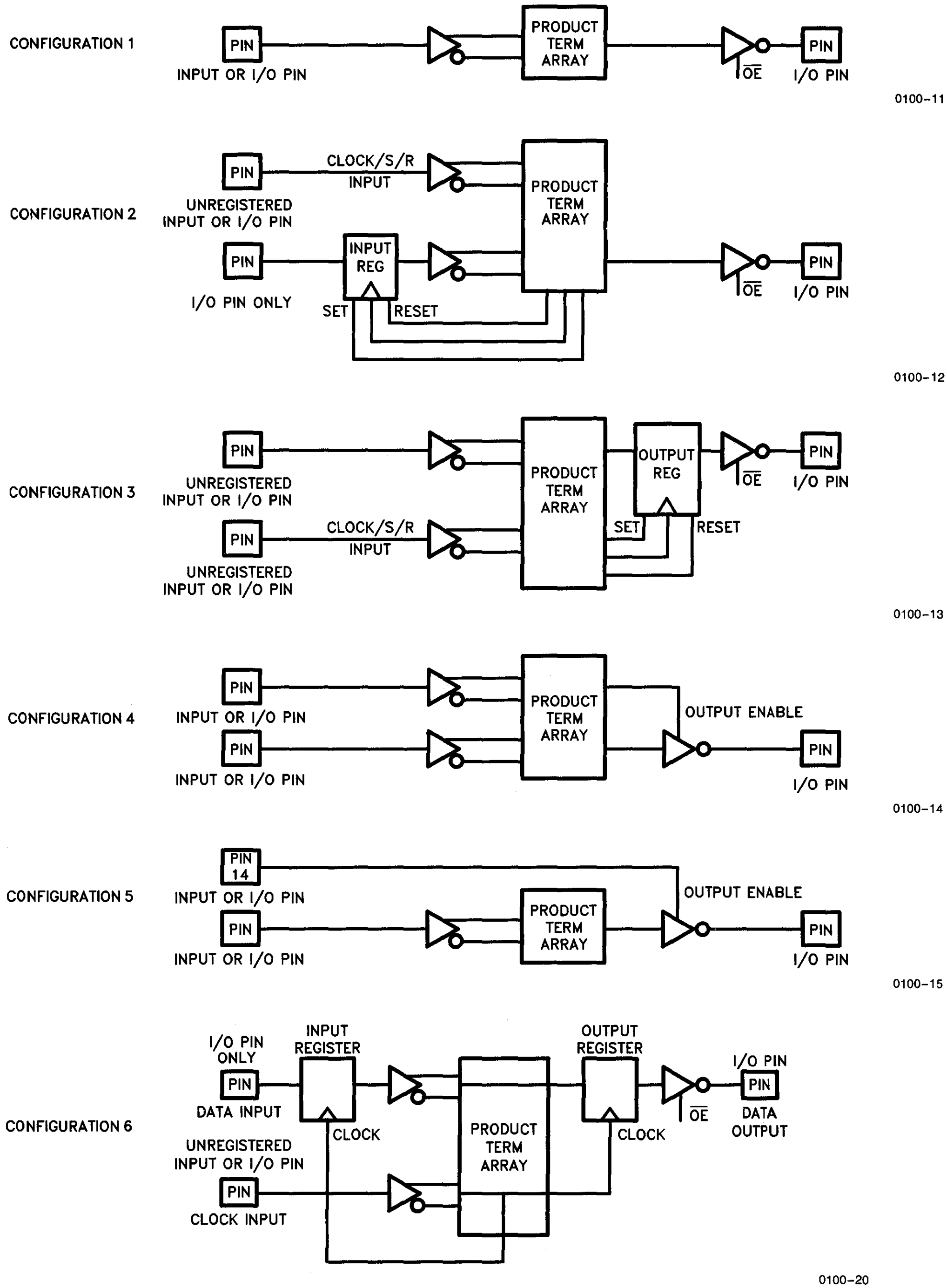
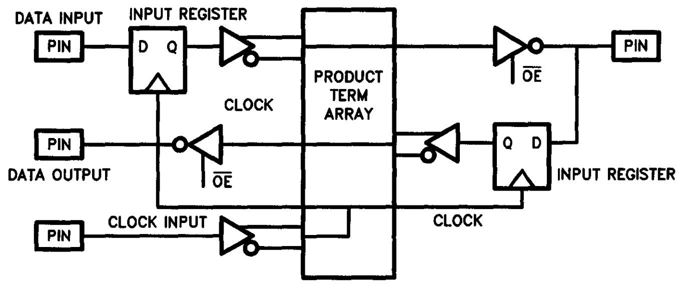


Figure 5. Timing Configurations

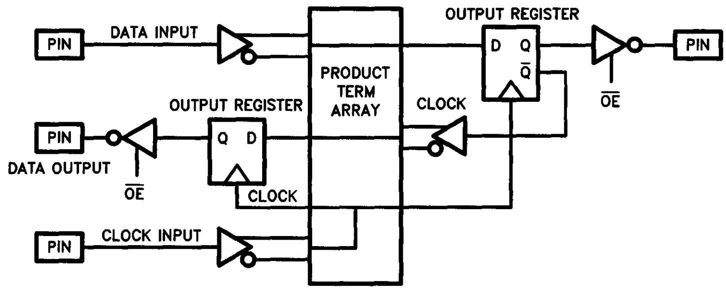
4

CONFIGURATION 7



0100–21

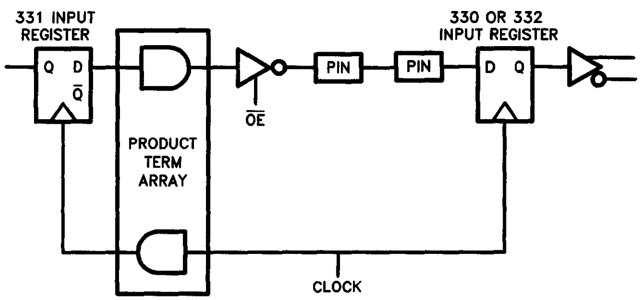
CONFIGURATION 8



0100–22

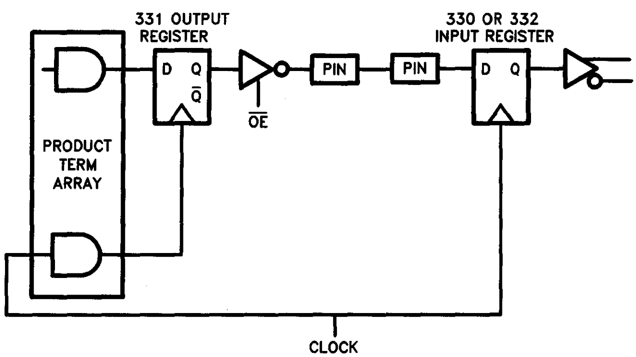
Figure 6

CONFIGURATION 9



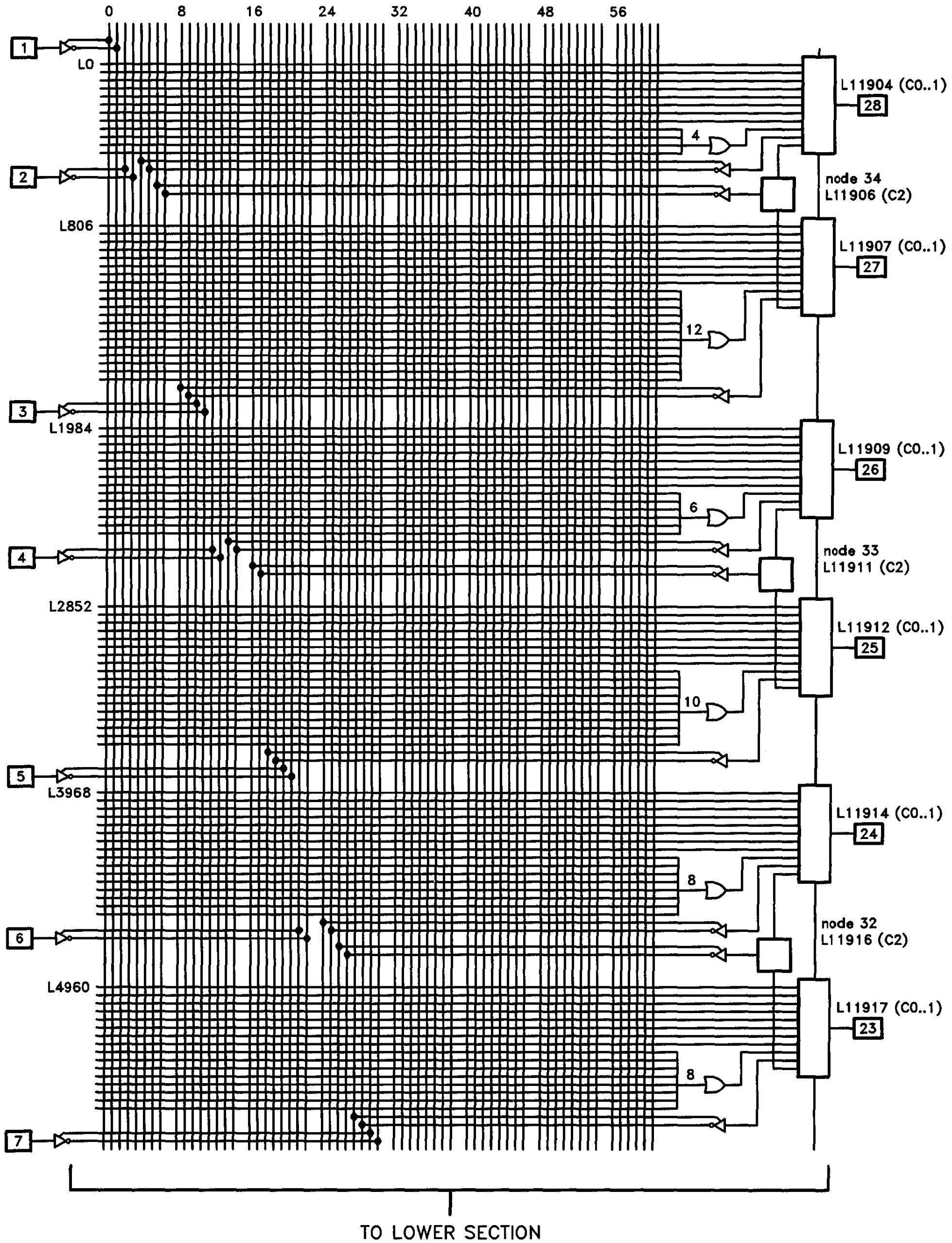
0100–23

CONFIGURATION 10

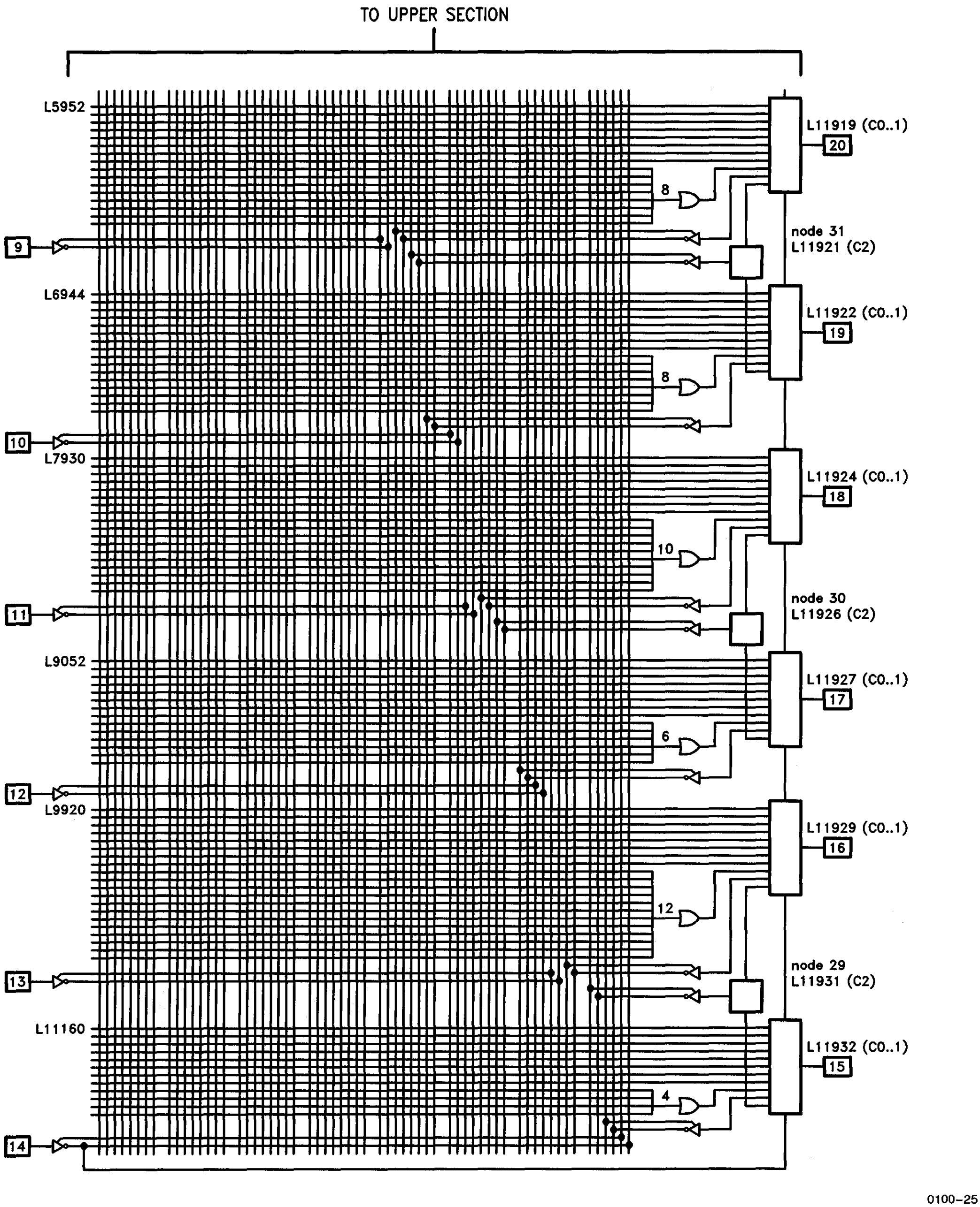


0100–26

Figure 7



CY7C331 Logic Diagram (Upper Half)



CY7C331 Logic Diagram (Lower Half)

Ordering Information

I_{CC1} (mA)	t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package Type	Operating Range
130	20	12	20	CY7C331-20PC	P21	Commercial
				CY7C331-20WC	W22	
				CY7C331-20JC	J64	
				CY7C331-20HC	H64	
160	25	15	25	CY7C331-25DMB	D22	Military
				CY7C331-25WMB	W22	
				CY7C331-25HMB	H64	
				CY7C331-25LMB	L64	
				CY7C331-25TMB	T74	
				CY7C331-25QMB	Q64	
120	25	12	25	CY7C331-25PC	P21	Commercial
				CY7C331-25WC	W22	
				CY7C331-25JC	J64	
				CY7C331-25HC	H64	
150	30	15	30	CY7C331-30DMB	D22	Military
				CY7C331-30WMB	W22	
				CY7C331-30HMB	H64	
				CY7C331-30LMB	L64	
				CY7C331-30TMB	T74	
				CY7C331-30QMB	Q64	
120	35	15	35	CY7C331-35PC	P21	Commercial
				CY7C331-35WC	W22	
				CY7C331-35JC	J64	
				CY7C331-35HC	H64	
150	40	20	40	CY7C331-40DMB	D22	Military
				CY7C331-40WMB	W22	
				CY7C331-40HMB	H64	
				CY7C331-40LMB	L64	
				CY7C331-40TMB	T74	
				CY7C331-40QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC1}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{IS}	7,8,9,10,11
t_{IH}	7,8,9,10,11
t_{WH}	7,8,9,10,11
t_{WL}	7,8,9,10,11
t_{CO}	7,8,9,10,11
t_{PD}	7,8,9,10,11
t_{IAR}	7,8,9,10,11
t_{IAS}	7,8,9,10,11
t_{PXZ}	7,8,9,10,11
t_{PZX}	7,8,9,10,11
t_{ER}	7,8,9,10,11
t_{EA}	7,8,9,10,11
t_S	7,8,9,10,11
t_H	7,8,9,10,11

Document #: 38-00066-C

CY7C332

Registered Combinatorial EPLD

CYPRESS SEMICONDUCTOR

Features

- 12 I/O macrocells each having:
  - Registered, latched, or transparent array input
  - A choice of two clock sources
  - Global or local output enable (OE)
  - Up to 19 product terms (PT) per output
  - Product term (PT) output polarity control
- 192 product terms with variable distribution to macrocells
  - An average of 14 PT's per macrocell sum node
  - Up to 19 PT's maximum for select nodes
- 2 clock inputs with configureable polarity control
- 13 input macrocells, each having:
  - Complementary input
  - Register, latch, or transparent access
  - Two clock sources
- 20 ns max. delay
- Low power
  - 120 mA typical I_{CC} quiescent
  - 180 mA max.
  - Power saving "Miser Bit" feature
- Security fuse
- 28 pin slim-line package; also available in 28 pin PLC
- UV-Eraseable and reprogrammable
- Programming and operation 100% testable

Product Characteristics

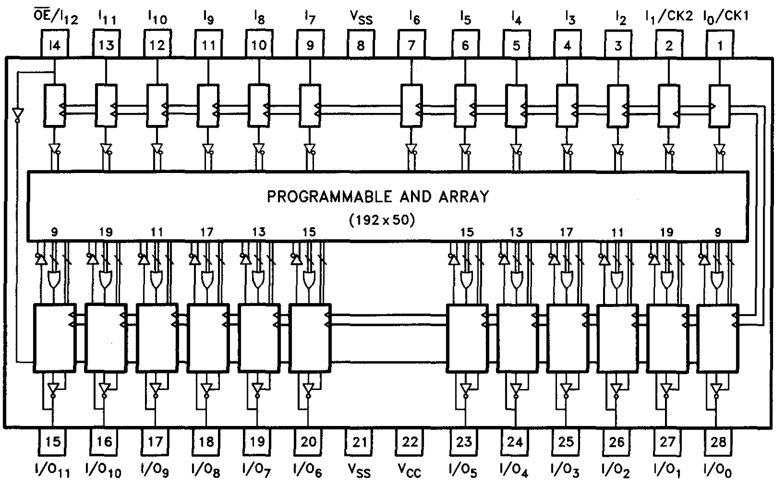
The CY7C332 is a versatile combinatorial PLD with I/O registers onboard. There are 25 array inputs; each has a macrocell which may be configured as a register, latch or simple buffer. Outputs have polarity and tristate control product terms. The allocation of product terms to I/O macrocells is varied so that functions of up to 19 product terms can be accommodated.

I/O Resources

Pins 1 through 7 and 9 through 14 function as dedicated array inputs. Pins 1 and 2 function as input clocks as well as normal inputs. Pin 14 functions as a global output enable as well as a normal input.

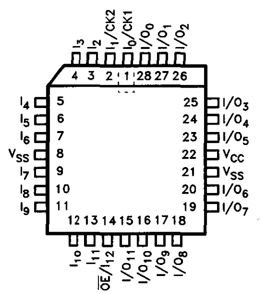
4

Block Diagram and Pinout



0134-1

LCC and PLCC Pinout

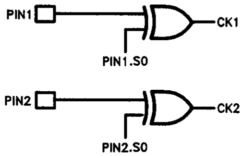


0134-2

Selection Guide

Generic Part Number	I_{CC1} mA		t_{ICO}/t_{PD} ns		t_{IS} ns	
	Com	Mil	Com	Mil	Com	Mil
7C332-15	130		18/15		3	
7C332-20	120	160	20	23/20	3	4
7C332-25	120	150	25	25	3	4
7C332-30		150		30		4

I/O Resources (Continued)

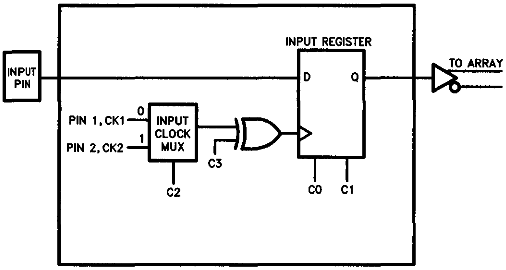


0134-3

Figure 1. CK1 and CK2

Pins 15 through 20 and 23 through 28 are connected to I/O macrocells and may be combinatorial outputs as well as registered or direct inputs.

Input Macrocell



0134-4

Figure 2. Input Macrocell

C3	C2	C1	C0	Input Register Option
X	X	0	0	Combinatorial
X	X	0	1	Illegal
0	0	1	1	Registered, CLK1, Rising Edge
0	1	1	1	Registered, CLK2, Rising Edge
1	0	1	1	Registered, CLK1, Fallling Edge
1	1	1	1	Registered, CLK2, Falling Edge
0	0	1	0	Latched, CLK1, High Asserted
0	1	1	0	Latched, CLK2, High Asserted
1	0	1	0	Latched, CLK1, Low Asserted
1	1	1	0	Latched, CLK2, Low Asserted

There are 13 input macrocells, corresponding to pins 1 through 7 and 9 through 14. Each macrocell has a clock which is selected to come from either pin 1 or pin 2 by configuration bit C2. Pins 1 and 2 are clocks as well as normal inputs. There is no C2 configuration bit for either of these two input macrocells. Macrocells connected to pins 1 and 2 do not have a clock choice, but each has a clock coming from the other pin.

Each input macrocell can be configured as a register, latch or a simple buffer (transparent path) to the product term array. For a register the configuration bit, C0, is 1 (programmed) and C1 is 1. For a Latch, C0 is 0 and C1 is 1. If both C0 and C1 are 0 (unprogrammed) then the macrocell is completely transparent.

Configuration bit C3 determines the clock edge on which the register is triggered or the polarity for which the latch is asserted. This clock polarity can be programmed independently for each input register. These configuration options are available on all inputs, including those in the I/O macrocell.

If C3 is 0 (unprogrammed), the clock will be rising edge triggered (register mode) or high asserted (latch mode).

If C3 is 1 (programmed), the clock will be falling edge triggered (register mode) or low asserted (latch mode).

I/O Macrocell

There are 12 I/O macrocells corresponding to pins 15 through 20 and 23 through 28. Each macrocell has a tristate output control, an XOR product term to dynamically control polarity, and a configureable feedback path.

For each I/O macrocell, the tristate control for the output may be configured two ways. If the configuration bit, C4, is a 1 (programmed), then the global OE signal is selected. Otherwise, the OE product term is used.

For each I/O macrocell, the input/feedback path may be configured as a register, latch, or shunt. There are two configuration bits per I/O macrocell which configure the feedback path. These are programmed in the same way as for the input macrocells.

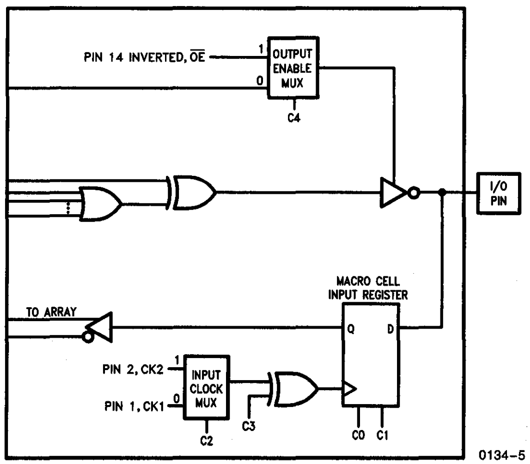
For each I/O macrocell, the input register clock (or Latch Enable) which is used for the input/feedback path may be selected as pin 1 (select bit, C2, not programmed) or pin 2 (select bit, C2, programmed).

Array Allocation to Output Macrocell

The number of product terms in each output macrocell sum is position dependent. The table below summarizes the allocation:

Table 1

Macrocell	Pin Number	Product Terms
0	28	9
1	27	19
2	26	11
3	25	17
4	24	13
5	23	15
6	20	15
7	19	13
8	18	17
9	17	11
10	16	19
11	15	9



0134-5

Figure 3. I/O Macrocell

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pins 8 and 21).............. −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 12 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current.......................... >200 mA

DC Programming Voltage 13.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military[5]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Commercial	2.4		V
			I_{OH} = −2 mA	Military			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA	Commercial		0.5	V
			I_{OL} = 8 mA	Military			
V_{IH}	Input LOW Level	Guaranteed HIGH Input, all Inputs[1]			2.2		V
V_{IL}	Input LOW Level	Guaranteed LOW Input, all Inputs[1]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$, V_{CC} = Max.			−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} < V_{OUT} < V_{CC}$			−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]			−30	−90	mA
I_{CC1}	Standby Power Supply Current	V_{CC} = Max., V_{IN} = GND Outputs Open		Commercial		120	mA
				Commercial -15		130	mA
				Military		150	mA
				Military -20		160	mA
I_{CC2}	Power Supply Current at Frequency[6,8]	V_{CC} = Max. Outputs Disabled (In High Z State) Device Operating at f_{MAX} External (f_{MAX1})		Commercial		180	mA
				Military		200	mA

Capacitance[3]

Parameters	Description	Test Conditions	Min.	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz		7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz		8	

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
3. Tested initially and after any design or process changes that may affect these parameters.
4. *Figure 4a* test load used for all parameters except t_{EA}, t_{ER}, t_{PZX} and t_{PXZ}. *Figure 4b* test load for t_{EA}, t_{ER}, t_{PZX}, t_{PXZ}. *Figure 4c* shows test waveforms and measurement reference levels.
5. T_A is the "instant on" case temperature.
6. Tested by periodic sampling of production product.

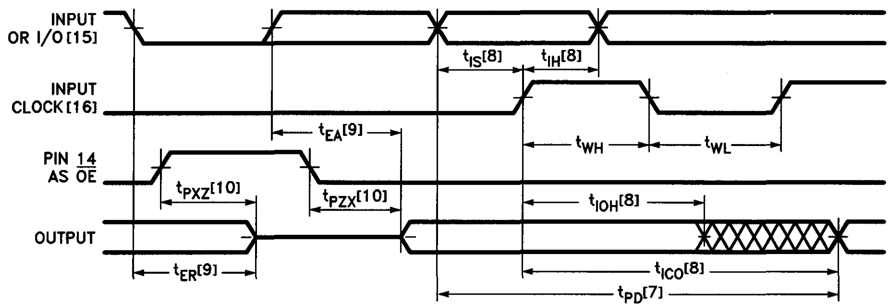
Switching Characteristics Over the Operating Range[1]

Parameters	Description	Commercial						Military						Units
		-15[14]		-20		-25		-20[14]		-25		-30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[7]		15		20		25		20		25		30	ns
t_{ICO}	Input Register Clock to Output Delay[8]		18		20		25		23		25		30	ns
t_{IS}	Input or Feedback Setup Time to Input Register Clock[8]	3		3		3		4		4		4		ns
t_{IH}	Input Register Hold Time[8]	3		3		3		4		4		4		ns
t_{EA}	Input to Output Enable Delay[4, 9]		20		20		25		25		25		30	ns
t_{ER}	Input to Output Disable Delay[4, 9]		20		20		25		25		25		30	ns
t_{PZX}	Pin 14 Enable to Output Enable Delay[4, 10]		15		15		20		20		20		25	ns
t_{PXZ}	Pin 14 Disable to Output Disable Delay[4, 10]		15		15		20		20		20		25	ns
t_{WH}	Input Clock Width High[6, 8]	9		10		10		10		10		12		ns
t_{WL}	Input Clock Width Low[6, 8]	9		10		10		10		10		12		ns
t_{IOH}	Output Data Stable Time from Input Register Clock Input[8, 14]	3		3		3		3		4		4		ns
$t_{IOH}-t_{IH}$	Output Data Stable Time This Device Minus I/P Reg Hold Time Same Device[11, 12, 14]	0		0		0		0		0		0		ns
$t_{OH}-t_{IH}$ 33X	Output Data Stable Time Minus I/P Reg Hold Time 7C330 & 7C332 Device[13, 14]	0		0		0		0		0		0		ns
t_{PE}	External Clock Period (t_{ICO} + t_{IS})[8]	21		23		28		27		29		34		ns
f_{MAX1}	Maximum External Operating Frequency ($1/(t_{ICO} + t_{IS})$)[8]	47.6		43.4		35.7		37		34.4		29.4		MHz
f_{MAX2}	Maximum Frequency Data Path[8]	55.5		50.0		40.0		50.0		40.0		33.3		MHz

Notes:

7. Refer to *Figure 6* configuration 1.
8. Refer to *Figure 6* configuration 2.
9. Refer to *Figure 6* configuration 3.
10. Refer to *Figure 6* configuration 4.
11. Refer to *Figure 6* configuration 5.
12. This specification is intended to guarantee that configuration 5 of *Figure 6* with input registered feedback can be operated with all input register clocks controlled by the same source. These parameters are tested by periodic sampling of production product.
13. This specification is intended to guarantee interface compatibility of the other members of the CY7C330 family with the CY7C332. This specification is met for the devices noted operating at the same ambient temperature and at the same power supply voltage. These parameters are tested periodically by sampling of production product.
14. Preliminary specifications.

Switching Waveforms



0134-10

Notes:

15. Because OE can be controlled by the $\overline{OE}$ product term, input signal polarity for control of OE can be of either polarity. Internally the product term $\overline{OE}$ signal is active high.
16. Since the input register clock polarity is programmable, the input clock may be rising or falling edge triggered.

AC Test Loads and Waveforms (Commercial)

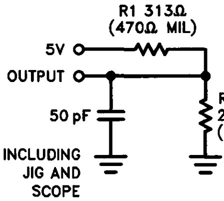
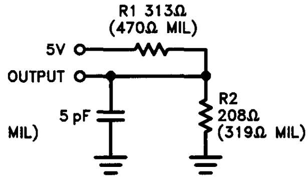
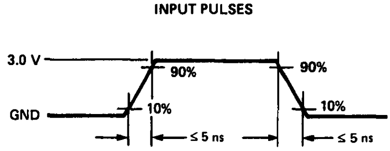


Figure 4a



0134-6

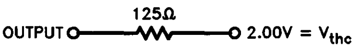
Figure 4b



0134-7

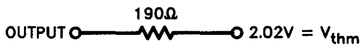
Figure 5. Input Pulses

Equivalent to: THÉVENIN EQUIVALENT (Commercial)



0134-8

Equivalent to: THÉVENIN EQUIVALENT (Military)



0134-9

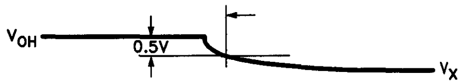
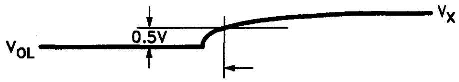
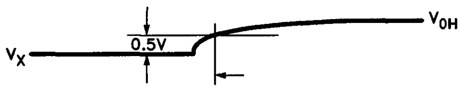
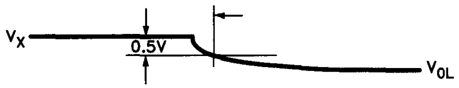
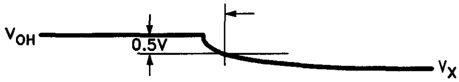
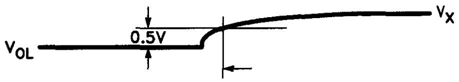
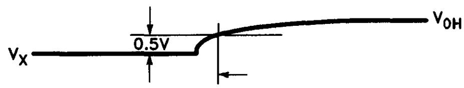
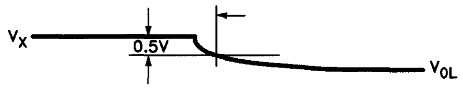
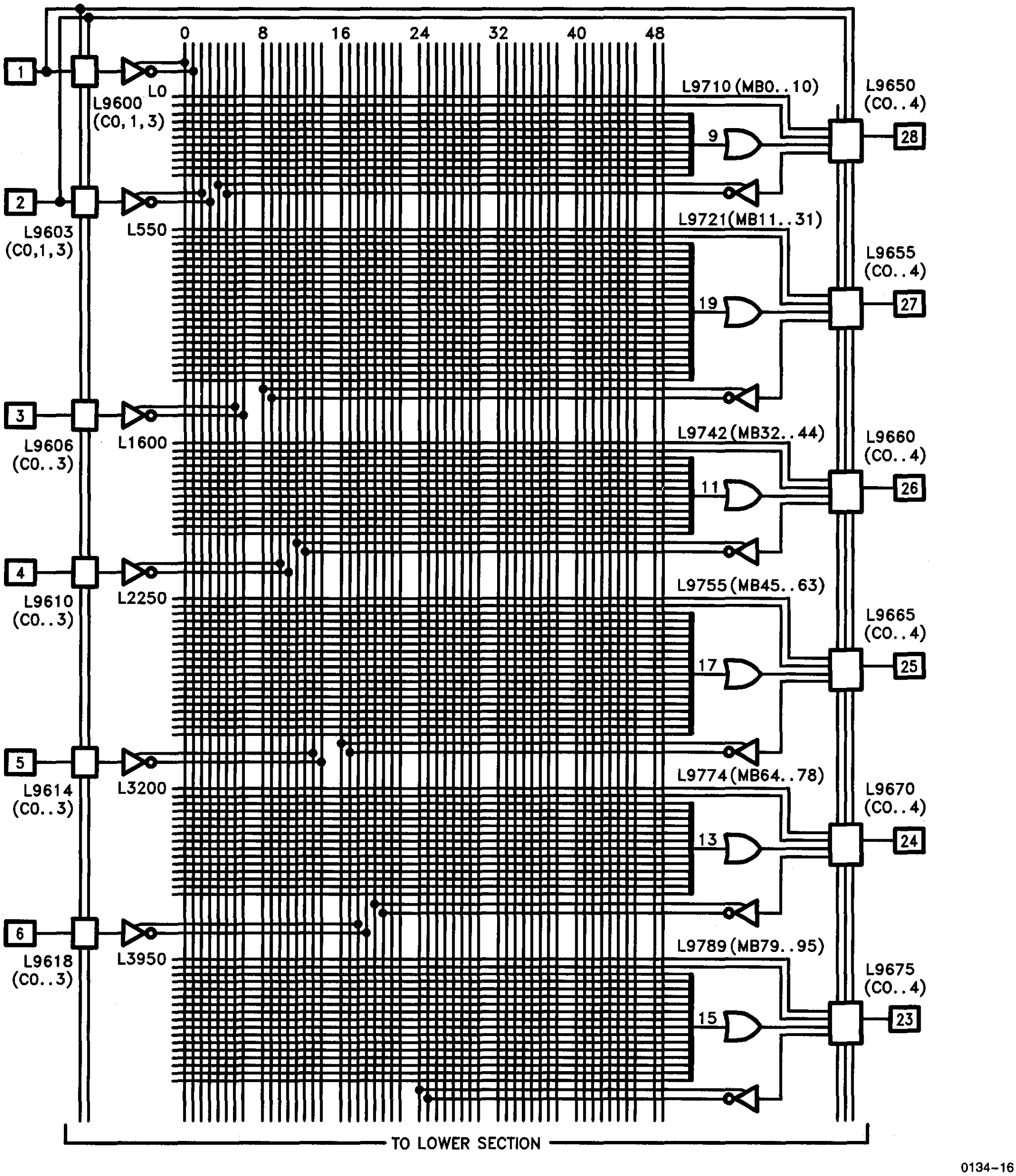
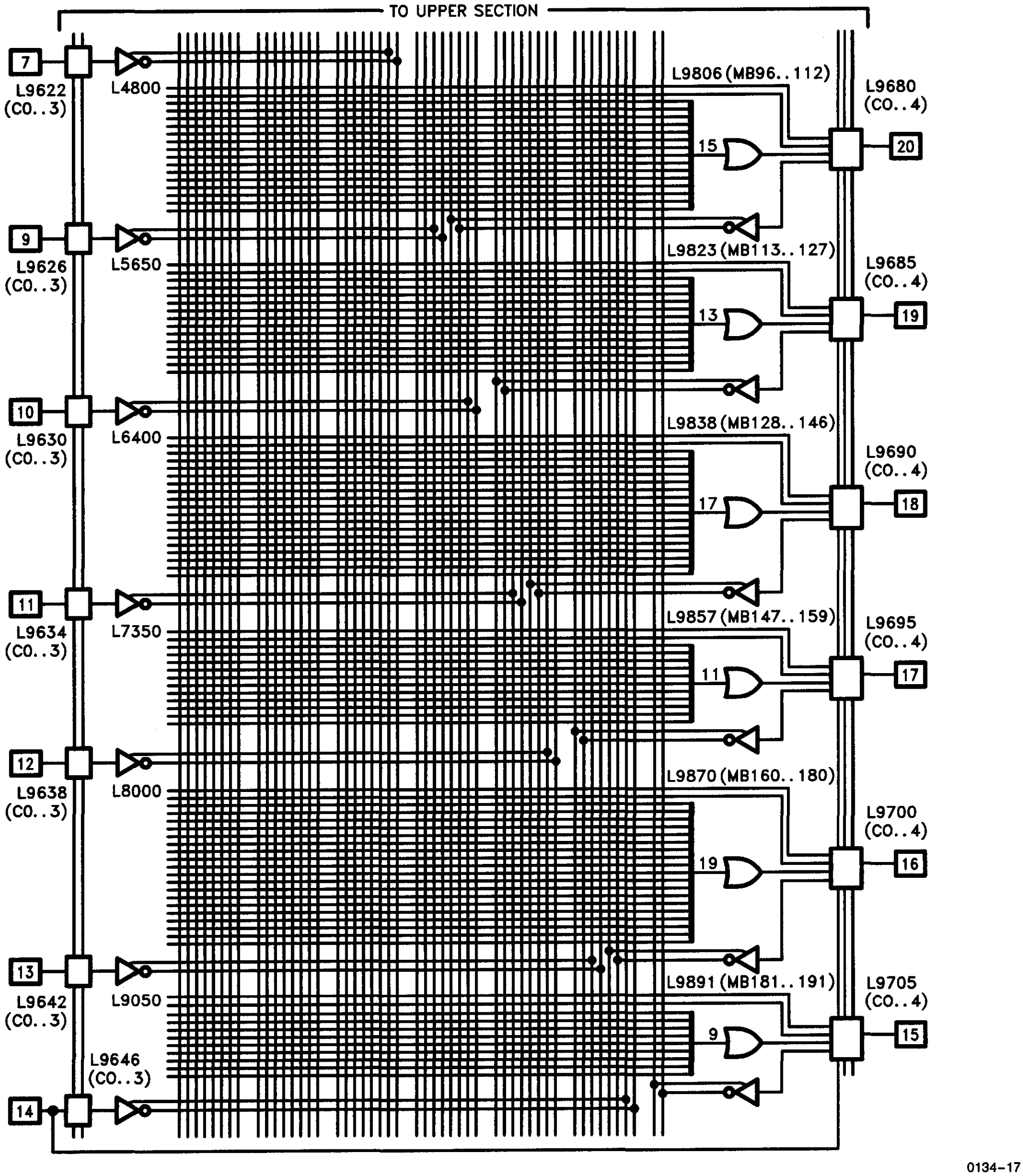
Parameter	V_X	Output Waveform—Measurement Level
t_{PXZ} (−)	1.5V	 0134-12
t_{PXZ} (+)	2.6V	 0134-13
t_{PZX} (+)	V_{thc}	 0134-14
t_{PZX} (−)	V_{thc}	 0134-15
t_{ER} (−)	1.5V	 0134-12
t_{ER} (+)	2.6V	 0134-13
t_{EA} (+)	V_{thc}	 0134-14
t_{EA} (−)	V_{thc}	 0134-15

Figure 4c. Test Waveforms and Measurement Levels



CY7C332 Logic Diagram (Upper Half)



CY7C332 Logic Diagram (Lower Half)

4

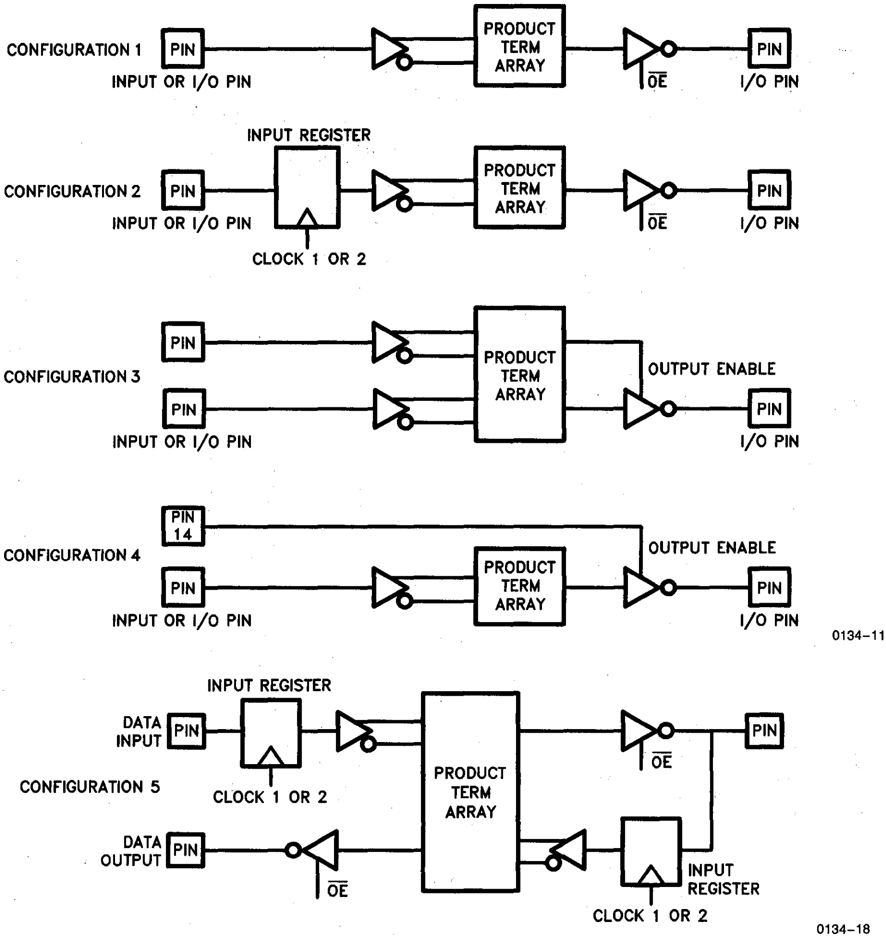


Figure 6. Timing Configurations

Ordering Information

I_{CC1} (max)	t_{ICO}/t_{PD} (ns)	t_{IS} (ns)	t_{IH} (ns)	Ordering Code	Package Type	Operating Range
120	18/15	3	3	CY7C332-15PC	P21	Commercial
				CY7C332-15WC	W22	
				CY7C332-15JC	J64	
				CY7C332-15HC	H64	
120	20	3	3	CY7C332-20PC	P21	Commercial
				CY7C332-20WC	W22	
				CY7C332-20JC	J64	
				CY7C332-20HC	H64	
160	23/20	4	4	CY7C332-20DMB	D22	Military
				CY7C332-20WMB	W22	
				CY7C332-20HMB	H64	
				CY7C332-20LMB	L64	
				CY7C332-20TMB	T74	
				CY7C332-20QMB	Q64	
120	25	3	3	CY7C332-25PC	P21	Commercial
				CY7C332-25WC	W22	
				CY7C332-25JC	J64	
				CY7C332-25HC	H64	
150	25	4	4	CY7C332-25DMB	D22	Military
				CY7C332-25WMB	W22	
				CY7C332-25HMB	H64	
				CY7C332-25LMB	L64	
				CY7C332-25TMB	T74	
				CY7C332-25QMB	Q64	
150	30	4	4	CY7C332-30DMB	D22	Military
				CY7C332-30WMB	W22	
				CY7C332-30HMB	H64	
				CY7C332-30LMB	L64	
				CY7C332-30TMB	T74	
				CY7C332-30QMB	Q64	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{CC1}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{IS}	7,8,9,10,11
t_{IH}	7,8,9,10,11
t_{WH}	7,8,9,10,11
t_{WL}	7,8,9,10,11
t_{ICO}	7,8,9,10,11
t_{PD}	7,8,9,10,11
t_{PXZ}	7,8,9,10,11
t_{PZX}	7,8,9,10,11
t_{ER}	7,8,9,10,11
t_{EA}	7,8,9,10,11

Document #: 38-00067-C

6-ns BiCMOS PAL® with Input Registers

Features

- Very high performance address decoder
  - t_{CO} = 6 ns
  - f_{MAX} = 125 MHz
- 12 input registers
- 8 outputs
- 2 product terms per output
- Asynchronous output enable
- Advanced BiCMOS technology
- Available in 28-pin 300-mil PDIP and CERDIP, and in PLCC and LCC packages

Functional Description

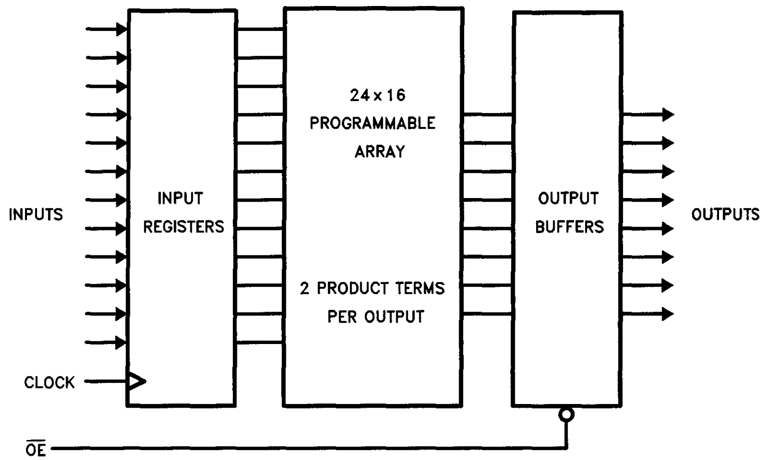
The CY7C336 is a 6-ns address decoder specially designed to interface with high-performance RISC processors and fast state machines. Twelve input registers capture data at the rising edge of the clock signal and forward the information to the 24 by 16 programmable array.

Each of the eight outputs has two product terms, one of which is used to enable the inverting buffer associated with the respective output. In addition, all outputs can be placed in a tri-stated condition via an output enable signal.

Six centrally located power pins are assigned to the CY7C336 to improve noise margins. A wide variety of package types including 28-pin 300-mil plastic and ceramic DIPs, LCCs, and PLCCs will be available.

4

Logic Block Diagram



PAL® is a registered trademark of Monolithic Memories, Inc.

Document #: 38-00134

CYPRESS SEMICONDUCTOR

7-ns PAL® with Input Registers

Features

- **Very high performance programmable logic device for high-speed interface circuits**
  - **— t_{CO} = 7 ns**
  - **— f_{MAX} = 111 MHz**
- **12 input registers**
- **8 outputs**
- **4 product terms per output**
- **Asynchronous output enable**
- **Advanced BiCMOS technology**
- **Available in 28-pin 300-mil PDIP and CERDIP, and in PLCC and LCC packages**

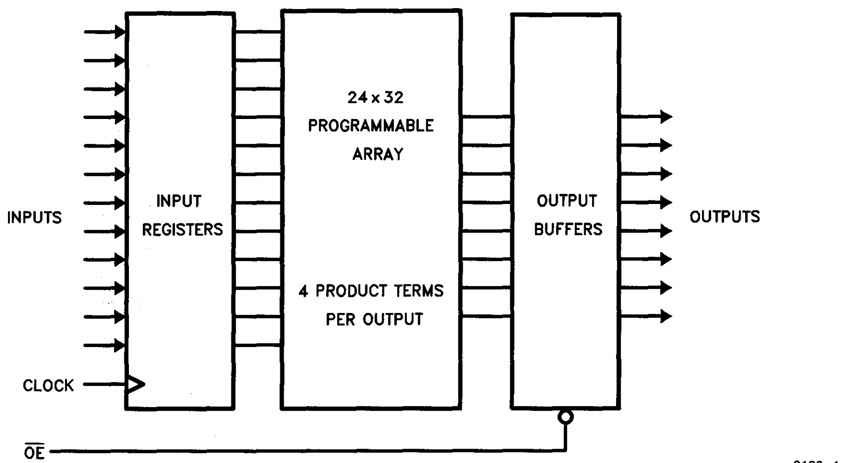
Functional Description

The CY7C337 is a 7-ns programmable logic device specially designed to interface with high-performance RISC processors and fast state machines. Twelve input registers capture data at the rising edge of the clock signal and forward the information to the 24 by 32 programmable array.

Each of the eight outputs has four product terms to support functions which require higher degrees of logic complexity. All outputs can be placed in a tri-stated condition via an output enable signal.

Six centrally located power pins are assigned to the CY7C337 to improve noise margins. A wide variety of package types including 28-pin 300-mil plastic and ceramic DIPs, LCCs, and PLCCs will be available.

Logic Block Diagram



PAL® is a registered trademark of Monolithic Memories, Inc.

Document #: 38-00139

CYPRESS SEMICONDUCTOR

6-ns BiCMOS PAL® with Output Latches

Features

- Very high performance address decoder with latched outputs
  - t_{PD} = 6 ns
  - t_{LO} = 5.5 ns
- 12 inputs
- 8 latched outputs
- 2 product terms per output
- Asynchronous output enable
- Advanced BiCMOS technology
- Available in 28-pin 300-mil PDIP and CERDIP, and in PLCC and LCC packages

Functional Description

The CY7C338 is a 6-ns programmable logic device specially designed to interface with high-performance general-purpose processors and fast state machines. Data presented at the eight inputs are processed by the 24 by 16 programmable array and delivered to eight output latches.

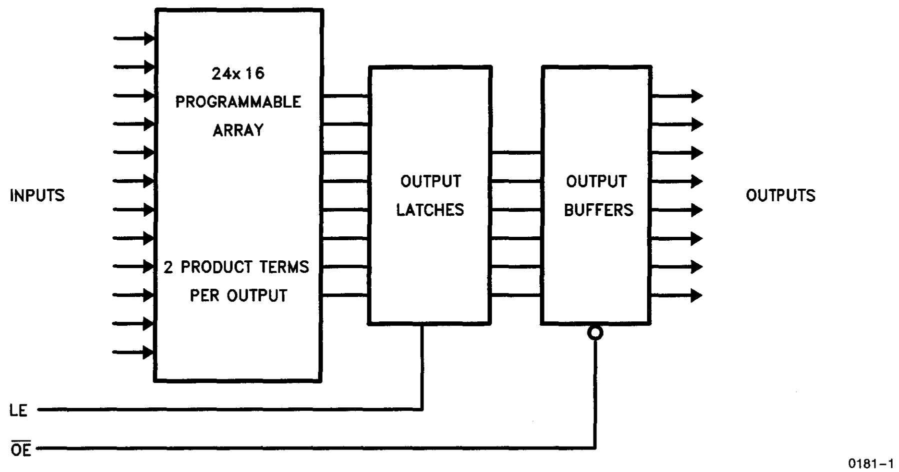
Each of the eight outputs has two product terms, one of which is used to enable the inverting buffer associated with the respective output. In addition, all outputs can be placed in a tri-stated condition via an output enable signal.

The output latches are controlled by the Latch Enable (LE) input. The latches are transparent as long as LE is HIGH; latch contents are frozen on the HIGH to LOW transition of the LE signal.

Six centrally located power pins are assigned to the CY7C338 to improve noise margins. A wide variety of package types including 28-pin 300-mil plastic and ceramic DIPs, LCCs, and PLCCs will be available.

4

Logic Block Diagram



Document #: 38-00133

CYPRESS SEMICONDUCTOR

7-ns BiCMOS PAL® with Output Latches

Features

- **Very high performance programmable logic device for high-speed interface circuits**
  - **— t_{PD} = 7 ns**
  - **— t_{LO} = 5.5 ns**
- **12 inputs**
- **8 latched outputs**
- **4 product terms per output**
- **Asynchronous output enable**
- **Advanced BiCMOS technology**
- **Available in 28-pin 300-mil PDIP and CERDIP, and in PLCC and LCC packages**

Functional Description

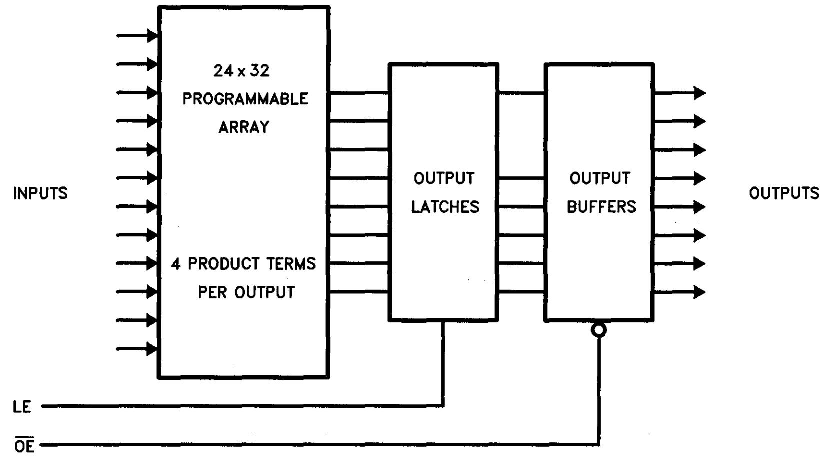
The CY7C339 is a 7-ns programmable logic device specially designed to interface with high-performance general-purpose processors and fast state machines. Data presented at the twelve inputs are processed by the 24 by 32 programmable array and delivered to eight output latches.

Each of the eight outputs has four product terms to support functions which require higher degrees of logic complexity. All outputs can be placed in a tri-stated condition via an output enable signal.

The output latches are controlled by the Latch Enable (LE) input. The latches are transparent as long as LE is HIGH; latch contents are frozen on the HIGH to LOW transition of the LE signal.

Six centrally located power pins are assigned to the CY7C339 to improve noise margins. A wide variety of package types including 28-pin 300-mil plastic and ceramic DIPs, LCCs, and PLCCs will be available.

Logic Block Diagram



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Document #: 38-00138

Multiple Array MatriX High Density EPLDs

Features

- **Erasable, user-configurable CMOS EPLDs capable of implementing high density custom logic functions**
- **Advanced 0.8 micron double-metal CMOS EPROM technology**
- **Multiple Array MatriX Architecture optimized for speed, density and straightforward design implementation**
  - **Typical clock frequency = 50 MHz**
  - **Programmable Interconnect Array (PIA) simplifies routing**
  - **Flexible Macrocells increase utilization**
  - **Programmable clock control**
  - **Expander product terms implement complex logic functions**
- **MAX+PLUS™ development system eases design**
  - **Runs on IBM PC/AT™ and compatible machines**
  - **Hierarchical schematic capture with 7400 series TTL and custom Macrofunctions**
  - **State machine and Boolean entry**
  - **Graphical delay path calculator**
  - **Automatic error location**
  - **Timing simulation**
  - **Graphical interactive entry of waveforms**

General Description

The Cypress Multiple Array MatriX (MAX™) family of EPLDs provides a user-configurable, high-density solution to general purpose logic integration requirements. With the combination of innovative architecture and state of the art process, the MAX EPLDs offer LSI density, without sacrificing speed.

The MAX architecture makes it ideal for replacing large amounts of TTL SSI and MSI logic. For example, a 74161 counter utilizes only 3% of the 128 Macrocells available in the CY7C342. Similarly, a 74151 8 to 1 multiplexer consumes less than one percent of the over 1,000 product terms in the CY7C342. This allows the designer to replace 50 or more TTL packages with just one MAX EPLD. The family comes in a range of densities, shown below. By standardizing on a few MAX building blocks, the designer can replace hundreds of different 7400 series part numbers currently used in most digital systems.

The family is based on an architecture of flexible Macrocells grouped together into Logic Array Blocks (LABs). Within the LAB is a group of additional product terms called Expander Product Terms. These Expanders are used and shared by the Macrocells, allowing complex functions, up to 35 product terms, to be easily implemented in a single Macrocell. A Programmable Interconnect Array (PIA) globally routes all signals within devices containing more than one LAB. This architecture is fabricated on the Cypress advanced 0.8 micron double layer metal CMOS EPROM process, yielding devices with significantly higher integration density and system clock speed than the largest of previous generation EPLDs.

The density and flexibility of the CY7C340 family is accessed using the MAX+PLUS development system. A PC based design system, MAX+PLUS is optimized specifically for the CY7C340 family architecture, providing efficient design processing. A hierarchical schematic entry mechanism is used to capture the design. State Machine, Truth Table and Boolean Equation entry mechanisms are also supported, and may be mixed with schematic capture. The powerful Design Processor performs minimization and logic synthesis, then automatically fits the design into the desired EPLD. Design verification is done using a timing simulator, which provides full A.C. simulation, along with an interactive graphic waveform editor package to speed waveform creation and debugging. During design processing a sophisticated automatic error locator shows exactly where the error occurred by popping the designer back into the schematic at the exact error location.

MAX Family Members

Feature	CY7C344	CY7C343	CY7C345	CY7C342
Macrocells	32	64	128	128
MAX Flip-Flops	32	64	128	128
MAX Latches[1]	64	128	256	256
MAX Inputs[2]	23	35	35	59
MAX Outputs	16	28	28	52
Packages	28H, J 28W, D	44H, J 40W, D	44H, J 40W, D	68H, J 68R

Key: D— DIP H— Windowed Ceramic Leaded Chip Carrier J— J-Lead Chip Carrier R— Pin Grid Array W— Windowed Ceramic DIP

Notes:
1. When all Expander Product Terms are used to implement latches.
2. With one output.

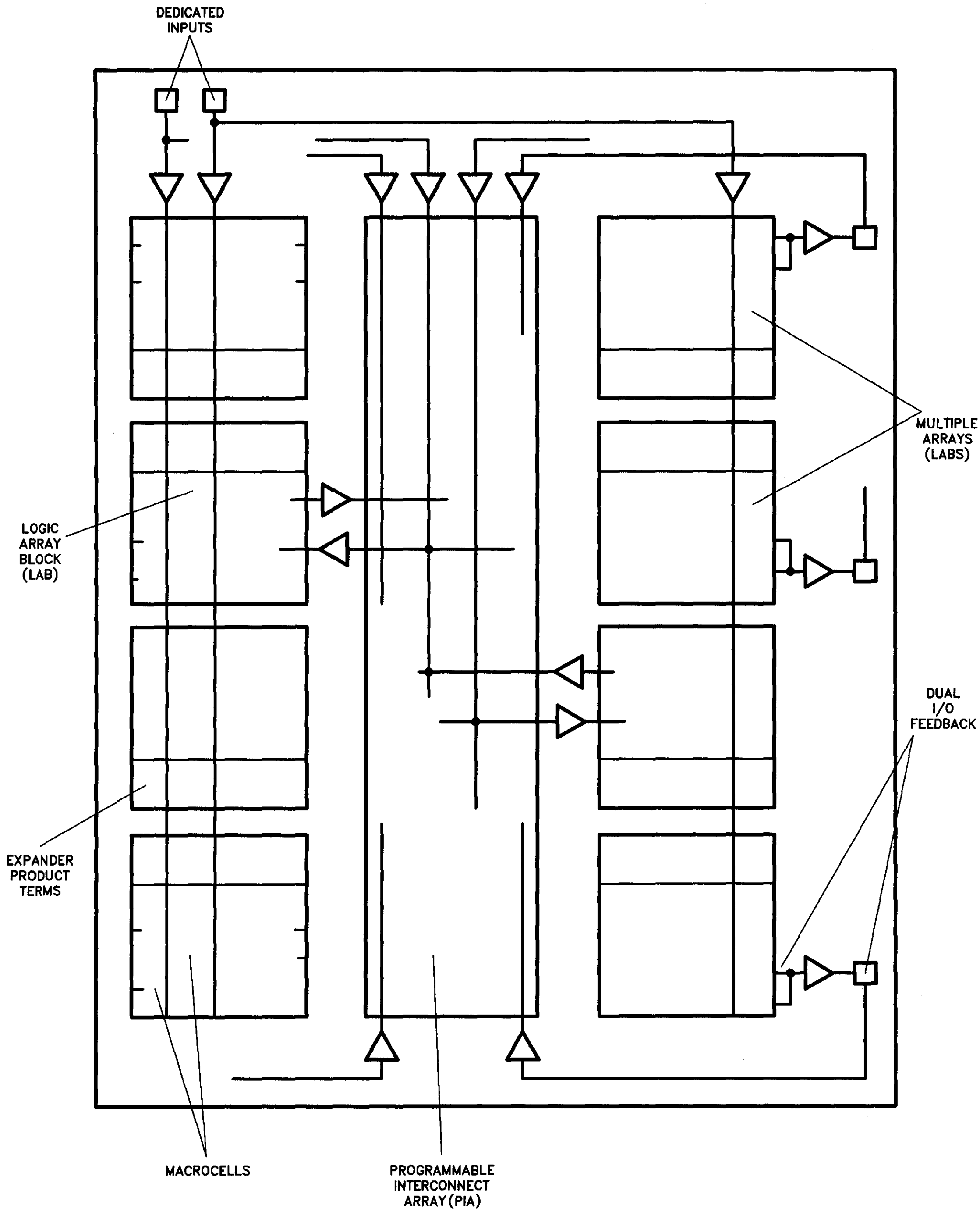


Figure 1. Key MAX Features

Functional Description

The Logic Array Block

The Logic Array Block, shown in *Figure 2*, is the heart of the MAX architecture. It consists of a Macrocell Array, Expander Product Term Array, and an I/O Block. The number of Macrocells, Expanders, and I/O vary, depending upon the device used. Global feedback of all signals is provided within an LAB, giving each functional block complete access to the LAB resources. The LAB itself is fed by the Programmable Interconnect Array and dedicated input bus. The feedbacks of the Macrocells and I/O pins feed the PIA, providing access to them by other LABs in the device. The CY7C340 family EPLDs having a single LAB use a global bus, and a PIA is not needed.

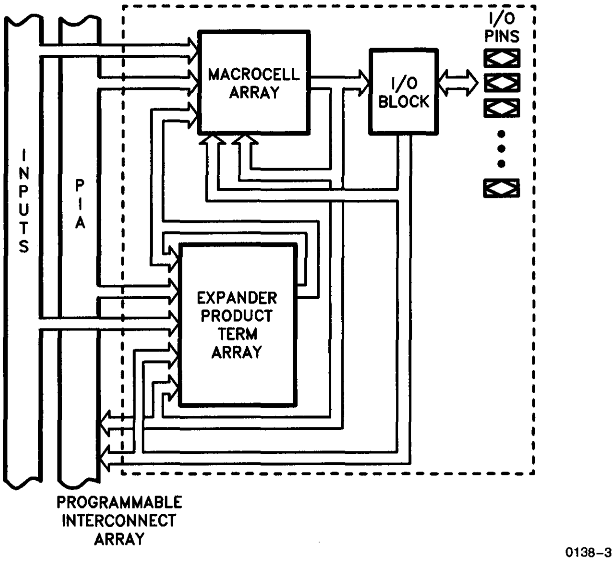


Figure 2. LAB Block Diagram

Functional Description (Continued)

The MAX Macrocell

Traditionally, PLDs have been divided into either PLA (programmable AND, programmable OR), or PAL™ (programmable AND, fixed OR) architectures. PLDs of the latter type provide faster input-to-output delays, but can be inefficient due to fixed allocation of product terms. Statistical analysis of PLD logic designs has shown that 70% of all logic functions (per Macrocell) require 3 product terms or less.

The Macrocell structure of MAX has been optimized to handle variable product term requirements. As shown in *Figure 3*, each Macrocell consists of a product term array and a configurable register. In the Macrocell, combinatorial logic is implemented with 3 product terms OR'ed together, which then feeds an XOR gate. The second input to the XOR gate is also controlled by a product term, providing the ability to control active high or active low logic and to implement T- and JK-type flip-flops. The MAX+PLUS software will also use this gate to implement complex mutually exclusive-OR arithmetic logic functions, or to do DeMorgan's Inversion, reducing the number of product terms required to implement a function.

If more product terms are required to implement a given function, they may be added to the Macrocell from the Expander Product Term Array. These additional product terms may be added to any Macrocell, allowing the designer to build gate intensive logic, such as address decoders, adders, comparators, and complex state machines, without using extra Macrocells.

The register within the Macrocell may be programmed for either, D, T, JK, or SR operation. It may alternately be configured as a flow-through latch for minimum input to output delays, or by-passed entirely for purely combinatorial logic. In addition, each register supports both asynchronous preset and clear, allowing asynchronous loading of counters or shift registers, as found in many standard TTL functions. These registers may be clocked with a synchronous system clock, or clocked independently from the logic array.

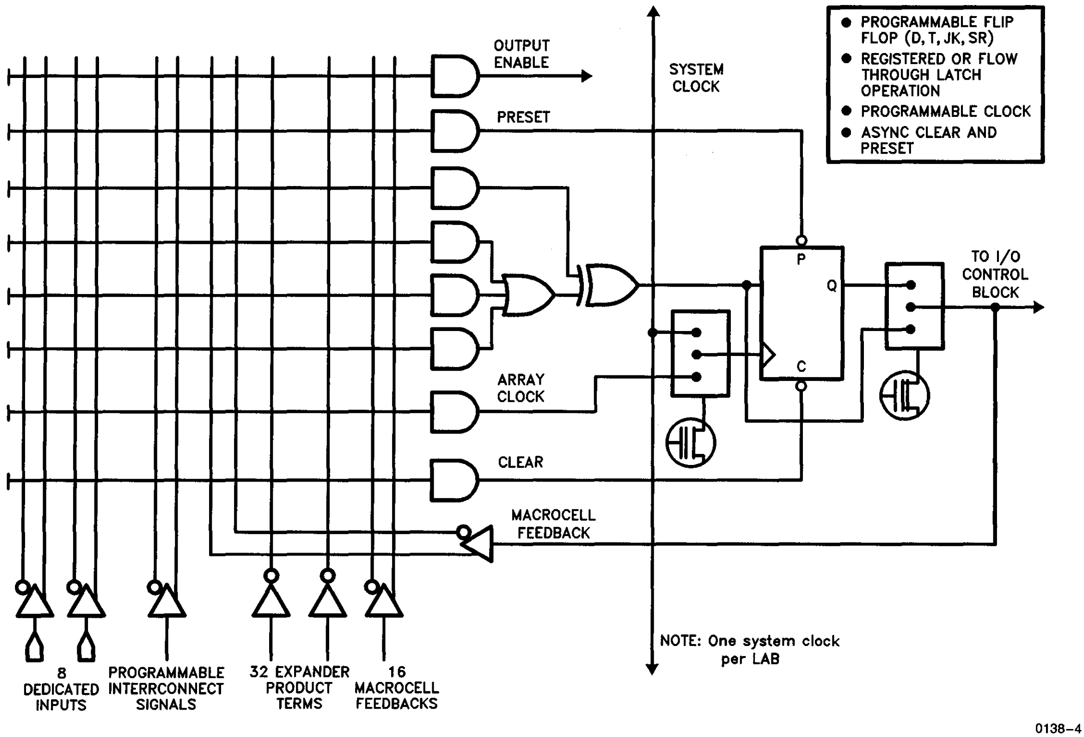


Figure 3. Macrocell Block Diagram

Functional Description (Continued)

Expander Product Terms

The Expander Product Terms, as shown in *Figure 4*, are fed by the Dedicated Input Bus, the Programmable Interconnect Array, the Macrocell Feedback, Expanders themselves, and the I/O pin feedbacks. The outputs of the Expanders then go to each and every product term in the Macrocell Array. This allows Expanders to be "shared" by the product terms in the Logic Array Block. One Expander may feed all Macrocells in the LAB, or even multiple product terms in the same Macrocell. Since these Expanders feed the secondary product terms (Preset, Clear, Clock, and Output Enable) of each Macrocell, complex logic functions may be implemented without utilizing another Macrocell. Likewise, Expanders may feed and be shared by other Expanders, to implement complex multi-level logic and input latches.

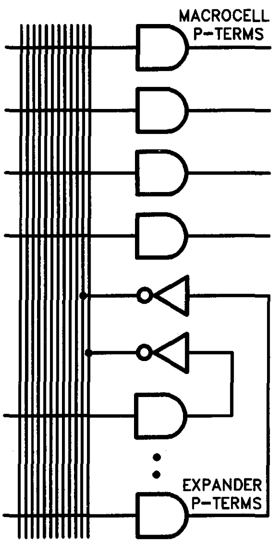


Figure 4

The I/O Block

Separate from the Macrocell Array is the I/O Control Block of the LAB. *Figure 5* shows the I/O block diagram. The tristate buffer is controlled by a Macrocell product term, and drives the I/O pad. The input of this buffer comes from a Macrocell within the associated LAB. The feedback path from the I/O pin may feed other blocks within the LAB, as well as PIA.

By decoupling the I/O pins from the flip-flops, all the registers in the LAB are "buried", allowing the I/O pins to be used as dedicated outputs, Bi-directional outputs or as additional dedicated inputs. Therefore, applications requiring many buried flip-flops, such as counters, shift registers, and state machines, no longer consume both the Macrocell register and the associated I/O pin, as in earlier devices.

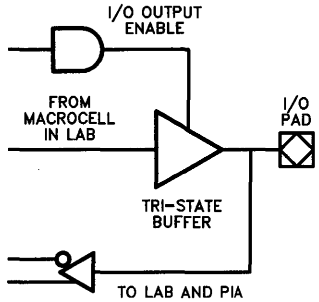


Figure 5. I/O Control

The Programmable Interconnect Array

A major problem which has limited PLD density and speed has been signal routing, i.e. getting signals from one Macrocell to another. For smaller devices, a single array is used and all signals are available to all Macrocells. But, as the devices increase in density, the number of signals being routed becomes very large, increasing the amount of silicon used for interconnections. Also, because the signal must be global, the added loading on the internal connection path reduces the overall speed performance of the device. The MAX architecture solves these problems. It is based on the concept of small, flexible Logic Array Blocks, which, in the larger devices, are interconnected by a Programmable Interconnect Array, or PIA.

The Programmable Interconnect Array solves interconnect limitations by routing only the signals needed by each LAB. The architecture is designed so that every signal on the chip is within the PIA. The PIA is then programmed to give each LAB access to the signals that it requires. Consequently, each LAB receives only the signals needed. This effectively solves any routing problems that may arise in a design, without degrading the performance of the device. Unlike masked or programmable gate arrays, which induce variable delays dependent on routing, the PIA has a fixed delay from point to point. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic.

4

MAX + PLUS™ Development System

General Description

The MAX + PLUS Development System represents a complete hardware and software solution for implementing designs in the Cypress CY7C340 family of EPLDs.
MAX + PLUS is a sophisticated Computer Aided Design (CAD) system that includes design entry, design simulation, and device programming. Hosted on an IBM PC/AT or compatible machine. MAX + PLUS gives the designer the tools to quickly and efficiently implement complex logic designs. A block diagram is shown in *Figure 10.*

Designs are entered in MAX + PLUS using a hierarchical graphic editor. This editor has such features as multiple windows, multiple zoom levels, unlimited hierarchy levels, symbol editing, and a library of 7400 series devices in addition to basic SSI gate and register primitives. Also available is a Timing Calculator, in which the designer may pick two places in the schematic, and the software will display typical timing between those two points. Boolean Equation, Netlist, State Machine, and Truth Table entry mechanisms may be used in conjunction with the graphic editor, giving added flexibility to the design environment.

In addition to a hierarchical design environment, MAX + PLUS has a sophisticated processing engine to exploit the CY7C340 family architecture. MAX + PLUS uses an advanced logic synthesizer and heuristic rules to process a design into a file for programming and/or simulation.

MAX + PLUS features a powerful event-driven simulator which displays typical timing results in an interactive waveform editor display. In this waveform editor, input vector waveforms may be directly modified and a new simulation run immediately.

Unlike most design environments, MAX + PLUS is unified,with all sections controlled by the Supervisor and Data Base Manager. By unifying the software, MAX + PLUS can offer an automatic error locator. If a design rule has been violated,the error processor will list an error message, the probable cause, and pop the designer into the schematic to the exact node where the mistake was made.

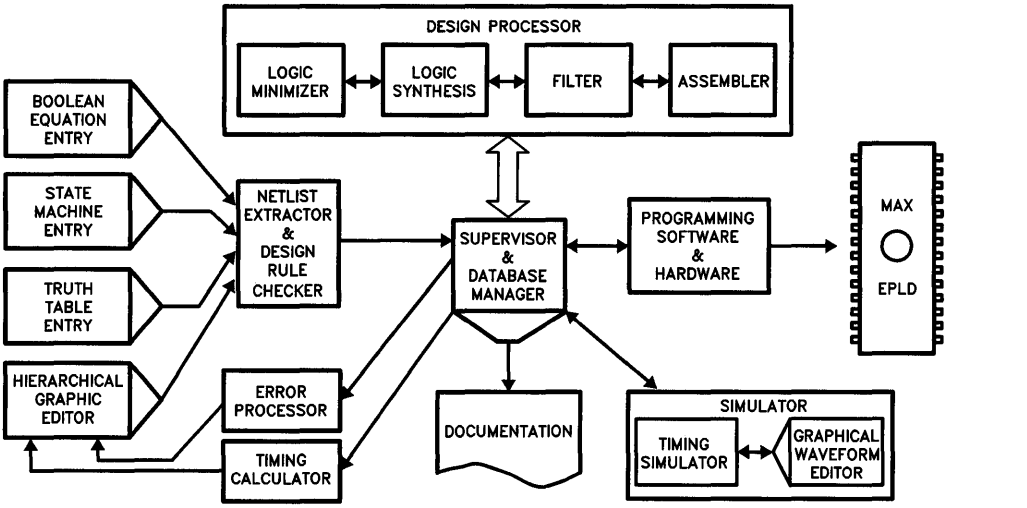


Figure 10. MAX + PLUS Block Diagram

MAX + PLUS Development System (Continued)

Design Entry

Design entry is easily accomplished with MAX + PLUS. MAX + PLUS provides multiple entry mechanisms, including traditional Boolean equation entry. Also available are State Machine and Truth Table entry, using a high-level state machine language. Because the CY7C340 family of EPLDs offer the designer large amounts of logic capability, a Hierarchical Graphic Editor has been provided to ease the design process.

Graphic Editor

The hierarchical design approach used by the graphic editor allows the designer to work with either a top-down or a bottom-up approach. The top down method allows the designer to start with a high level block diagram, and then move down and design each block individually. The bottom up method allows the simulation and verification of small building blocks, which may then be pieced together into a final design.

The Graphic Editor is mouse driven and uses pull down menus or single keystrokes to enter commands. Aiding in the design task is a library of 7400 series MSI and SSI logic gates. The designer may use these and/or create his own custom symbols. Custom functions are easily created in the hierarchy by first designing the function. Then a symbol is made, which represents that schematic. In this way a custom function may be used in multiple places in the current design, or saved and used in subsequent designs.

The function of any symbol created may be defined using graphic entry, state machine, Boolean, or truth table descriptions. This provides a wide range of flexibility for the designer, allowing Boolean equations to be combined with state machine entry in a hierarchical schematic.

The timing calculator within the graphic editor gives the designer instant feedback concerning timing delays inherent in a path. By placing two probes on different parts of the schematic, the designer immediately knows the worst case timing of the processed design. This is a valuable addition for design debugging and documentation.

Design Processor

After the design is entered, a push of the mouse button invokes the powerful MAX + PLUS processor. First a netlist is extracted from the complete hierarchical design. During the extraction process, design rules are checked for any errors, and if errors are found, the error processor leads the designer directly to the schematic location where the error occurred. The extracted design is placed in the database, and the design is ready to be processed.

The versatile MAX architecture, with its Expander Product Terms and mutual exclusivity, requires a dedicated processor to take optimal advantage of the MAX features, one that does much more than simplify logic. The logic synthesizer in MAX + PLUS uses several knowledge-based synthesis rules to factor and map logic onto the multi-level MAX architecture. It will then choose the mapping aproach that ensures the most efficient use of the silicon resources. The synthesizer will also remove any unused logic or registers from the design.

The next module in the design processor is the fitter. Its function is similar to a placement and router used in semicustom gate arrays. Using heuristic rules, it takes the synthesized design and optimally places it within the chosen CY7C340 EPLD. With the larger devices, it also routes the signals across the Programmable Interconnect Array, freeing the designer from interconnection issues.

Timing Simulator

Rounding out the software offering is a powerful timing simulator to aid in the verification and debugging of designs. The simulator is a graphical, event driven software package that yields true, worst case timings based upon user-defined input vectors.

Waveforms may be viewed using a Graphical Waveform Editor, which allows graphical definitions and editing of input waveforms. The designer can define his input waveform using the mouse to draw the actual waveform as a function of time. There are also powerful waveform editing commands, all menu driven, to aid in the development of the input vectors. Such options as pre-defining, copying and repeating waveforms are all available to the user. If graphical definition is not desired, there is a powerful vector description language for developing input vectors.

The simulator itself has all the capabilities one would expect from this type of design environment. Observing buried nodes, accessing flip-flop control inputs, and initializing and forcing nodes to specified values are all available within the timing simulator. The user may also specify breakpoints during the simulation itself, and execute subroutines dependent upon the breakpoints. All of these tools aid the designer in verifying and debugging the design, even before breadboarding.

The simulator also has advanced A.C. timing detection. The software will warn the user when setup and hold times to flip flops are being violated, and when there is oscillation present in the simulation. Also, the user may define a minimum pulse width, in which any pulse within the design that is smaller than a certain size will be classified as a glitch and the designer will be informed.

Supervisor and Error Processor

All facets of the MAX + PLUS system are overseen by the Supervisor and Data Base Manager. By tying all of the software together, the designer has a unified operational environment. All the software has the same "look and feel", so that complex commands and languages are not needed.

Automatic error processing is an added benefit of this approach. If an error occurs during the processing of the design, the software will automatically tell the user what the error is, and the probable cause.

Then, by pressing a single key, the software will automatically go the schematic in the graphic editor and pinpoint the location of the error.

CYPRESS SEMICONDUCTOR

192 Macrocell MAX™ EPLDs

Features

- **192 macrocells in 12 LABs**
- **8 dedicated inputs, 64 bidirectional I/O pins**
- **Programmable interconnect array**
- **384 expander product terms**
- **Available in 84-pin JLCC, PLCC, and PGA**

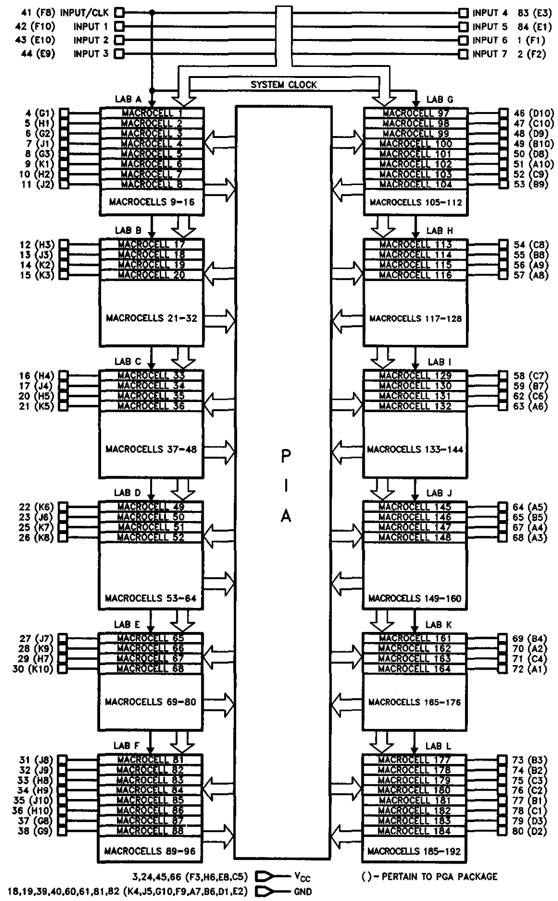
Functional Description

The CY7C341 is an Erasable Programmable Logic Device (EPLD) in which CMOS EPROM cells are used to configure logic functions within the device. The MAX architecture is 100% user configurable, allowing the devices to accommodate a variety of independent logic functions.

The 192 macrocells in the CY7C341 are divided into 12 Logic Array Blocks (LABs), 16 per LAB. There are 384 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

The speed and density of the CY7C341 allows it to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multi-function chips. With greater than 37 times the functionality of 20-pin PLDs, the CY7C341 allows the replacement of over 75 TTL devices. By replacing large amounts of logic, the CY7C341

Logic Block Diagram



0183–1

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Functional Description (Continued)

reduces board space, part count, and increases system reliability.

Each LAB contains 16 macrocells. In LABs A, F, G and L, 8 macrocells are connected to I/O pins and 8 are buried, while for LABs B, C, D, E, H, I, J and K, 4 macrocells are connected to I/O pins and 12 are buried. Moreover, in addition to the I/O and buried macrocells, there are 32 single product term logic expanders in each LAB. Their use greatly enhances the capability of the macrocells without increasing the number of product terms in each macrocell.

Logic Array Blocks

There are 12 logic array blocks in the CY7C341. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C341 provides 8 dedicated inputs, one of which may be used as a system clock. There are 64 I/O pins which may be individually configured for input, output, or bidirectional data flow.

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

4

Timing Delays

Timing delays within the CY7C341 may be easily determined using MAX+PLUS™ software or by the model shown in *Figure 3*. The CY7C341 has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the MAX+PLUS software provides a timing simulator.

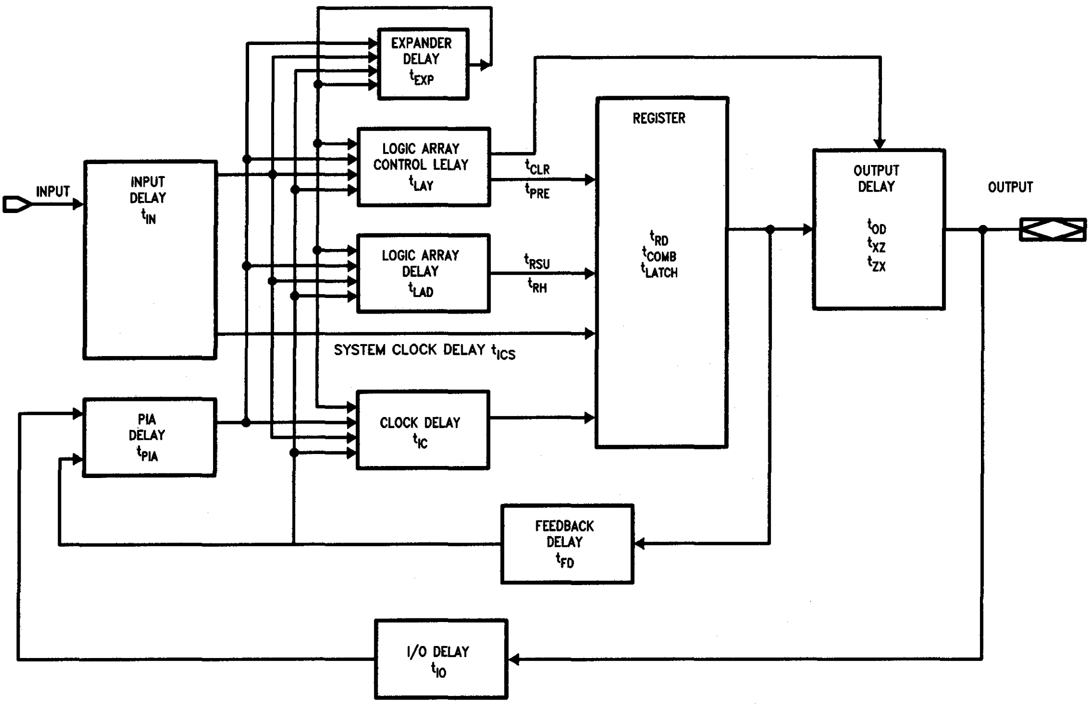


Figure 3. CY7C341 Internal Timing Model

Design Recommendations

For proper operation, input and output pins must be constrained to the range GND (V_{IN} or V_{OUT}) V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Design Security

The CY7C341 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a propriety design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

The CY7C341 is fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C342
CY7C345

128-Macrocell MAX™ EPLDs

Features

CY7C342

- **128 macrocells in 8 LABs**
- **8 dedicated inputs, 52 bidirectional I/O pins**
- **Programmable interconnect array**
- **Available in 68-pin HLCC, PLCC, and PGA**

CY7C345

- **128 macrocells in 8 LABs**
- **8 dedicated inputs, 28 bidirectional I/O pins**
- **256 expander product terms**
- **Programmable interconnect array**
- **Available in 44-pin HLCC or PLCC**

Functional Description

The CY7C342 and CY7C345 are Erasable Programmable Logic Devices (EPLDs) in which CMOS EPROM cells are used to configure logic functions within the devices. The MAX architecture is 100% user configurable, allowing the devices to accommodate a variety of independent logic functions.

The 128 macrocells in the CY7C342 are divided into 8 Logic Array Blocks (LABs), 16 per LAB. There are 256 expander product terms, 32 per LAB, to be used and shared by the macrocells within each LAB. Each LAB is interconnected with a programmable interconnect array, allowing all signals to be routed throughout the chip.

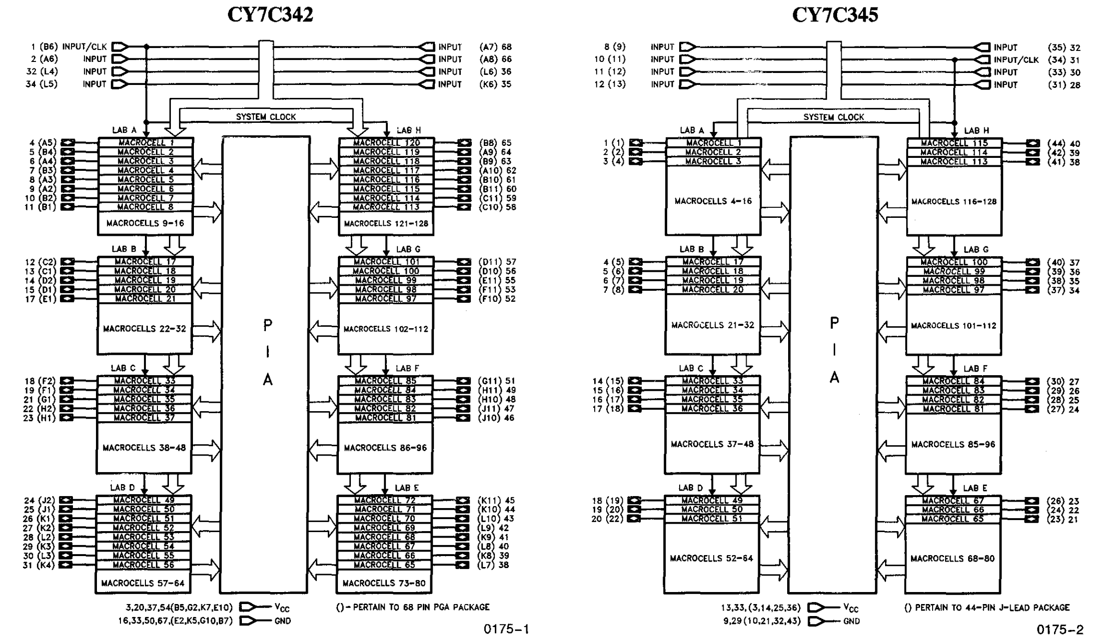
The speed and density of the CY7C342 allows it to be used in a wide range of applications, from replacement of large amounts of 7400 series TTL logic, to complex controllers and multi-function chips. With greater than 25 times the functionality of 20-pin PLDs, the CY7C342 allows the replacement of over 50 TTL devices. By replacing large amounts of logic, the CY7C342 reduces board space, part count, and increases system reliability.

The CY7C345 packs the same LSI density of the CY7C342 into a smaller, 40-pin DIP or 44-pin HLCC package. Designed for applications in which large amounts of logic must be packed into a very small area, the CY7C345 is ideally suited for applications which require large amounts of buried logic.

It has the same number of macrocells and expanders as the CY7C342, and a programmable interconnect array to allow communications between the LABs. Each LAB has an I/O block, with LABs A, D, E and H having four bidirectional tri-stateable I/O pins, and the rest having three I/O pins. Like all other EPLDs in the MAX family, these I/O pins support dual feedback. In this way any macrocells may be buried, with only the output of macrocells needed off-chip connected to I/O pins.

4

Logic Block Diagrams



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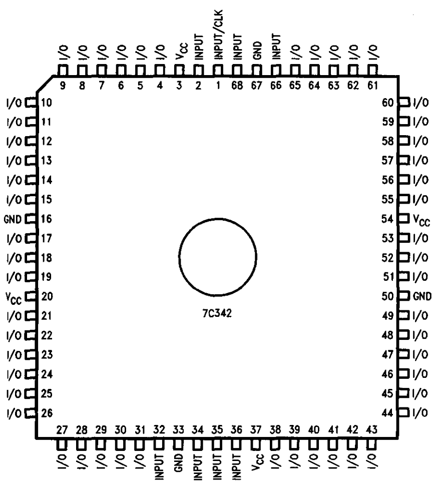
Selection Guide

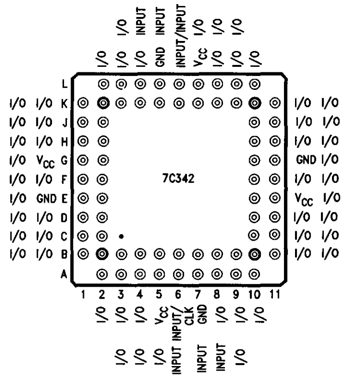
		7C342-30 7C345-30	7C342-35 7C345-35	7C342-40 7C345-40
Maximum Access Time (ns)		30	35	40
Maximum Operating Current (mA)	Commercial	310	310	
	Military		320	320
Maximum Standby Current (mA)	Commercial	200	200	
	Military		240	240

Pin Configurations

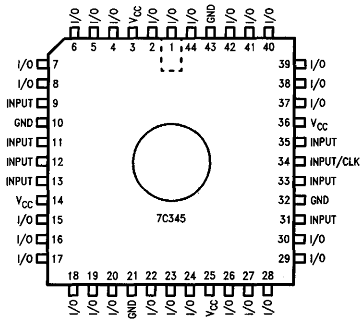


0175-3

PGA
Bottom View



0175-4



0175-6

Logic Array Blocks

There are eight logic array blocks in the CY7C342 and CY7C345. Each LAB consists of a macrocell array containing 16 macrocells, an expander product term array containing 32 expanders, and an I/O block. The LAB is fed by the programmable interconnect array and the dedicated input bus. All macrocell feedbacks go to the macrocell array, the expander array, and the programmable interconnect array. Expanders feed themselves and the macrocell array. All I/O feedbacks go to the programmable interconnect array so that they may be accessed by macrocells in other LABs as well as the macrocells in the LAB in which they are situated.

Externally, the CY7C342 provides eight dedicated inputs, one of which may be used as a system clock. There are 52 I/O pins which may be individually configured for input, output, or bidirectional data flow.

The CY7C345 is internally identical to the CY7C342, but is packaged in a 40-pin DIP or 44-pin J-lead package. It has 8 dedicated inputs, and pin #31 may be used as a system clock. There are 28 I/O pins which may be individually configured for input, output, or bidirectional flow.

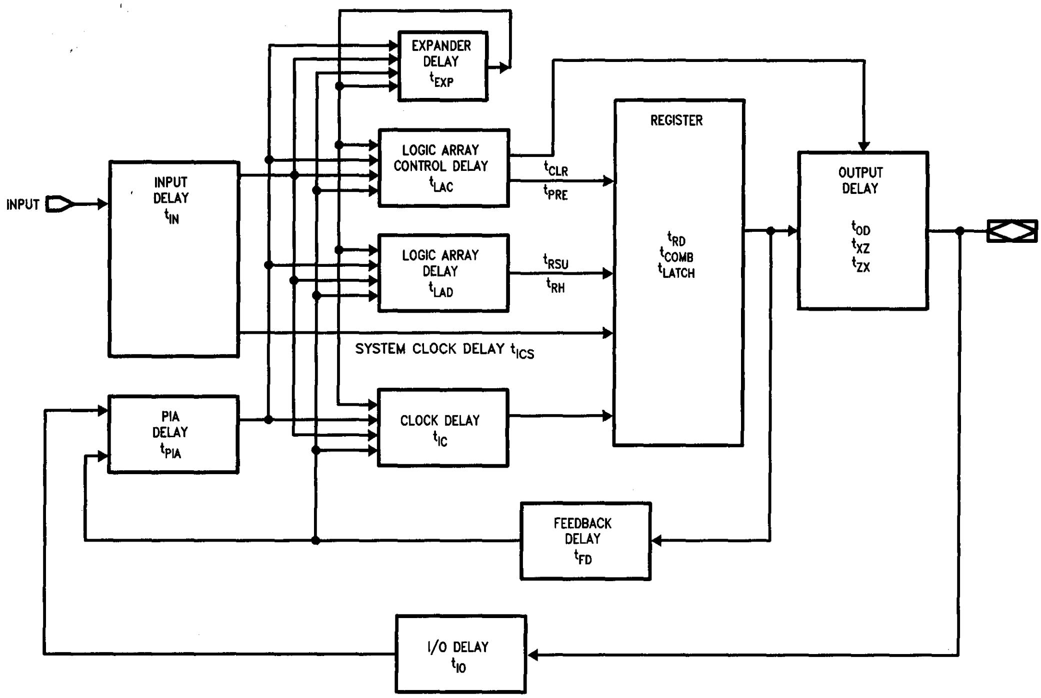


Figure 3. CY7C342/CY7C345 Internal Timing Model

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C342 and CY7C345 may be easily determined using MAX+PLUS™ software or by the model shown in *Figure 3*. The CY7C342 and CY7C345 have fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the MAX+PLUS software provides a timing simulator.

Design Recommendations

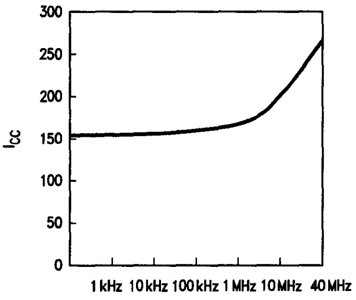
Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C342 and CY7C345 contain circuitry to protect device pins from high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

4

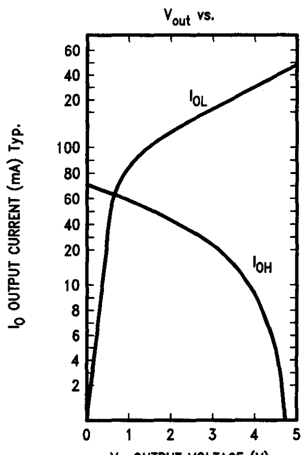
Design Security

The CY7C342 and CY7C345 contain a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a propriety design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.



0175-9

Figure 4. I_{CC} vs f_{MAX}



0175-8

Figure 5. Output Drive Current

The CY7C342 and CY7C345 are fully functionally tested and guaranteed through complete testing of each programmable EPROM bit and all internal logic elements thus ensuring 100% programming yield.

The erasable nature of these devices allows test programs to be used and erased during early stages of the production flow. The devices also contain on-board logic test circuitry to allow verification of function and AC specification once encapsulated in non-windowed packages.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from a straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on dedicated input pins. The parameter t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on the dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set up time. If $(t_{AS2} + t_{AH})$ is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C342.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... 0°C to +70°C

Maximum Junction Temperature (Under Bias) .... 150°C

Supply Voltage to Ground Potential .... −2.0V to +7.0V

Maximum Power Dissipation .... 2500 mW

DC V_{CC} or GND Current .... 500 mA

DC Output Current, per Pin .... −25 mA to +25 mA

DC Input Voltage[1] .... −2.0V to +7.0V

DC Program Voltage................ −2.0V to +13.5V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to +125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−30	−90	mA
I_{CC_1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		200	mA
			Military		240	mA
I_{CC_2}	Power Supply Current[3]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[3]	Commercial		310	mA
			Military		320	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	12	

Notes:

1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. This parameter is measured with device programmed as a 16-bit counter in each LAB. This parameter is tested periodically by sampling production material.
4. *Figure 1a* test load used for all parameters except t_{ER} and t_{EA}. *Figure 1b* test load used for t_{ER} and t_{EA}. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[4]

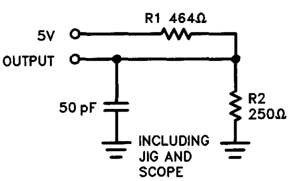
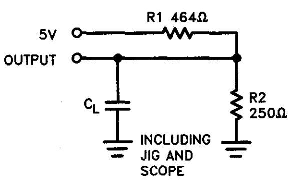


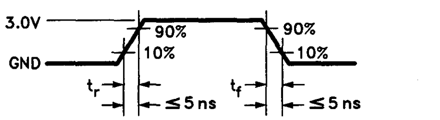
Figure 1a



0175-10

Figure 1b

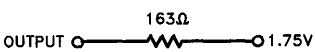
Input Pulses



0175-11

Figure 2

Equivalent to: THÉVENIN EQUIVALENT (Commercial/Military)



0175-12

External Synchronous Switching Characteristics[4] Over Operating Range

Parameters	Description		CY7C342-30 CY7C345-30 Min.	CY7C342-30 CY7C345-30 Max.	CY7C342-35 CY7C345-35 Min.	CY7C342-35 CY7C345-35 Max.	CY7C342-40 CY7C345-40 Min.	CY7C342-40 CY7C345-40 Max.	Units
t_{PD1}	Dedicated Input to Combinatorial Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{PD2}	I/O Input to Combinatorial Output Delay[6]	Com'l		45		55			ns
		Mil				55		65	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[7]	Com'l		44		55			ns
		Mil				55		65	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[8]	Com'l		60		75			ns
		Mil				75		90	
t_{EA}	Input to Output Enable Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{ER}	Input to Output Disable Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l		16		20			ns
		Mil				20		23	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[9]	Com'l		35		42			ns
		Mil				42		50	
t_{S1}	Dedicated Input or Feedback Setup Time to Synchronous Clock Input[5, 10]	Com'l	22		25				ns
		Mil			25		28		
t_{S2}	I/O Input Setup Time to Synchronous Clock Input[5]	Com'l	39		45				ns
		Mil			45		52		
t_H	Input Hold Time from Synchronous Clock Input[5]	Com'l	0		0				ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{WL}	Synchronous Clock Input Low Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{RW}	Asynchronous Clear Width[5]	Com'l	30		35				ns
		Mil			35		40		
t_{RR}	Asynchronous Clear Recovery Time[5]	Com'l	30		35				ns
		Mil			35		40		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{PW}	Asynchronous Preset Width[5]	Com'l	30		35				ns
		Mil			35		40		
t_{PR}	Asynchronous Preset Recovery Time[5]	Com'l	30		35				ns
		Mil			35		40		
t_{PO}	Asynchronous Preset to Registered Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{CF}	Synchronous Clock to Local Feedback Input[11]	Com'l		3		6			ns
		Mil				6		9	
t_P	External Synchronous Clock Period ($t_{CO1} + t_{S1}$)	Com'l	38		45				ns
		Mil			45		51		

External Synchronous Switching Characteristics[4] Over Operating Range (Continued)

Parameters	Description		CY7C342-30 CY7C345-30 Min.	CY7C342-30 CY7C345-30 Max.	CY7C342-35 CY7C345-35 Min.	CY7C342-35 CY7C345-35 Max.	CY7C342-40 CY7C345-40 Min.	CY7C342-40 CY7C345-40 Max.	Units
f_{MAX1}	External Feedback Maximum Frequency $(1/(t_{CO1} + t_{S1}))$[12]	Com'l	26.3		22.2				MHz
		Mil			22.2		19.6		
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $1/(t_{S1} + t_{CF})$ or $(1/t_{CO1})$[13]	Com'l	40.0		32.2				MHz
		Mil			32.2		28.5		
f_{MAX3}	Data Path Maximum Frequency, least of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S1} + t_H))$ or $(1/t_{CO1})$[14]	Com'l	45.4		40.0				MHz
		Mil			40.0		33.3		
f_{MAX4}	Maximum Register Toggle Frequency $(1/(t_{WL} + t_{WH})$[15]	Com'l	50.0		40.0				MHz
		Mil			40.0		33.3		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[16]	Com'l	3		3				ns
		Mil			3		3		

Notes:

5. This specification is a measure of the delay from input signal applied to a dedicated input, (68-pin PLCC input pin 1, 2, 32, 34, 35, 66, or 68) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.

   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.

   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added to the comparable delay for a dedicated input. If expanders are used add the maximum expander delay t_{EXP} to the overall delay for the comparable delay without expanders.
6. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
7. This specification is a measure of the delay from an input signal applied to a dedicated input, (68-pin PLCC input pin 1, 2, 32, 34, 35, 36, 66, or 68) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic.
8. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
9. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
10. If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S2} for synchronous operation and t_{AS2} for asynchronous operation.
11. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
12. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs. All feedback is assumed to be local originating within the same LAB.
13. This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$.
14. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes data input signals are applied to dedicated input pins and no expander logic is used. If any of the data inputs are I/O pins, t_{S2} is the appropriate t_S for calculation.
15. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to the dedicated clock input pin.
16. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

4

External Asynchronous Switching Characteristics[4] Over Operating Range

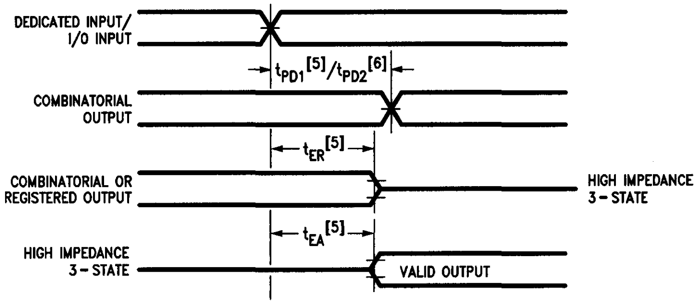
Parameters	Description		CY7C342-30 CY7C345-30 Min.	CY7C342-30 CY7C345-30 Max.	CY7C342-35 CY7C345-35 Min.	CY7C342-35 CY7C345-35 Max.	CY7C342-40 CY7C345-40 Min.	CY7C342-40 CY7C345-40 Max.	Units
t_{ACO_1}	Asynchronous Clock Input to Output Delay[5]	Com'l		30		35			ns
		Mil				35		45	
t_{ACO_2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[17]	Com'l		46		55			ns
		Mil				55		64	
t_{AS_1}	Dedicated Input or Feedback Setup Time to Asynchronous Clock Input[5]	Com'l	10		10				ns
		Mil			10		10		
t_{AS_2}	I/O Input Setup Time to Asynchronous Clock Input[5]	Com'l	27		30				ns
		Mil			30		33		
t_{AH}	Input Hold Time from Asynchronous Clock Input[5]	Com'l	15		15				ns
		Mil			15		15		
t_{AWH}	Asynchronous Clock Input High Time[5]	Com'l	25		30				ns
		Mil			30		35		
t_{AWL}	Asynchronous Clock Input Low Time[5]	Com'l	25		30				ns
		Mil			30		35		
t_{ACF}	Asynchronous Clock to Local Feedback Input[18]	Com'l		18		22			ns
		Mil				22		26	
t_{AP}	External Asynchronous Clock Period ($t_{ACO_1} + t_{AS_1}$) or ($t_{AWH} + t_{AWL}$)	Com'l	50		60				ns
		Mil			60		70		
f_{MAXA_1}	External Feedback Maximum Frequency in Asynchronous Mode ($1/t_{AP}$)[19]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA_2}	Maximum Internal Asynchronous Frequency[22]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA_3}	Data Path Maximum Frequency in Asynchronous Mode[21]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA_4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[20]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[23]	Com'l	15		15				ns
		Mil			15		15		

Notes:

17. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to the dedicated clock input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
18. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register setup time, t_{AS_1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
19. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.
20. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
21. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS_1} + t_{AH})$ or $1/t_{ACO_1}$. It asssumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO_1}$.
This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB. This parameter is tested periodically by sampling production material.
23. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input applied to an external dedicated input pin.

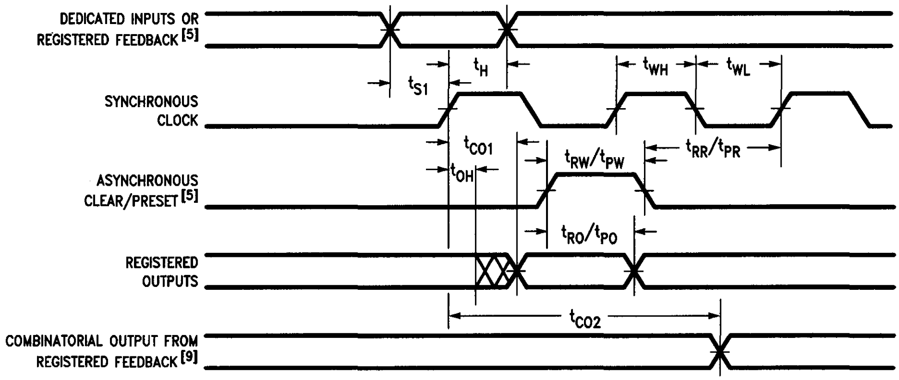
Switching Waveforms

External Combinatorial



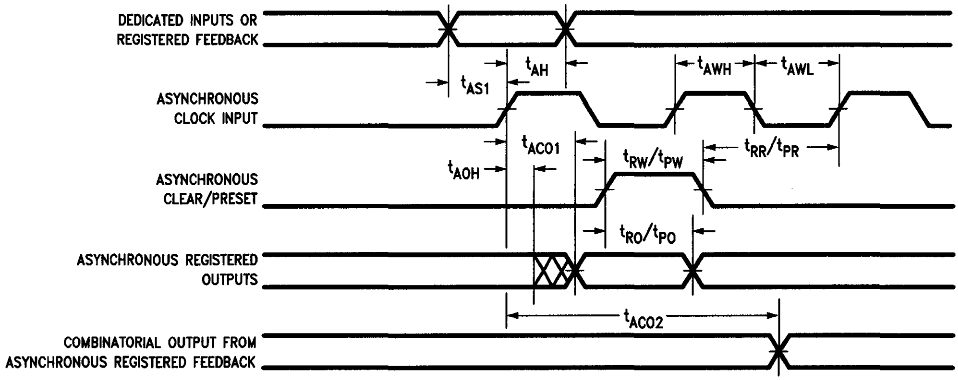
0175-13

External Synchronous



0175-14

External Asynchronous



0175-15

4

Internal Switching Characteristics[1] Over Operating Range

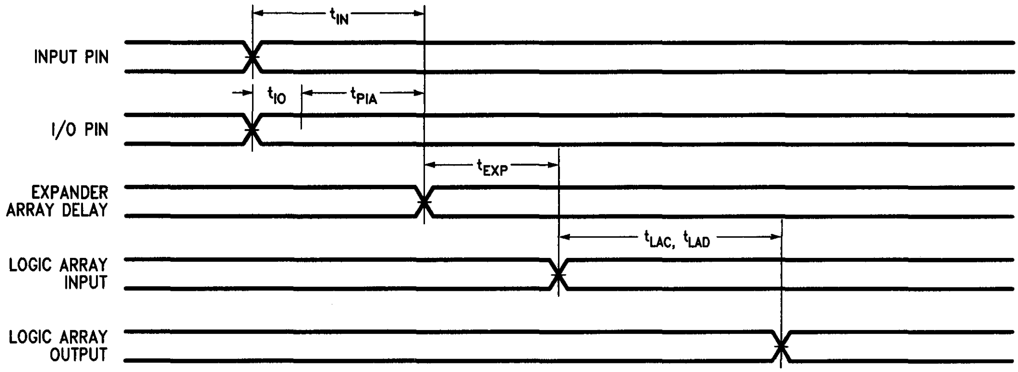
Parameters	Description		CY7C342-30 CY7C345-30 Min.	CY7C342-30 CY7C345-30 Max.	CY7C342-35 CY7C345-35 Min.	CY7C342-35 CY7C345-35 Max.	CY7C342-40 CY7C345-40 Min.	CY7C342-40 CY7C345-40 Max.	Units
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		7		9			ns
		Mil				9		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		6		9			ns
		Mil				9		12	
t_{EXP}	Expander Array Delay	Com'l		14		20			ns
		Mil				20		25	
t_{LAD}	Logic Array Data Delay	Com'l		14		16			ns
		Mil				16		18	
t_{LAC}	Logic Array Control Delay	Com'l		12		13			ns
		Mil				13		14	
t_{OD}	Output Buffer and Pad Delay[24]	Com'l		5		6			ns
		Mil				6		7	
t_{ZX}	Output Buffer Enable Delay[25]	Com'l		11		13			ns
		Mil				13		15	
t_{XZ}	Output Buffer Disable Delay[26]	Com'l		11		13			ns
		Mil				13		15	
t_{RSU}	Register Setup Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil			10		12		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	8		10				ns
		Mil			10		12		
t_{LATCH}	Flow Through Latch Delay	Com'l		4		4			ns
		Mil				4		4	
t_{RD}	Register Delay	Com'l		2		2			ns
		Mil				2		2	
t_{COMB}	Transparent Mode Delay[27]	Com'l		4		4			ns
		Mil				4		4	
t_{CH}	Clock High Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{CL}	Clock Low Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{IC}	Asynchronous Clock Logic Delay	Com'l		16		18			ns
		Mil				18		20	
t_{ICS}	Synchronous Clock Delay	Com'l		2		3			ns
		Mil				3		4	
t_{FD}	Feedback Delay	Com'l		1		2			ns
		Mil				2		3	
t_{PRE}	Asynchronous Register Preset Time	Com'l		6		7			ns
		Mil				7		8	
t_{CLR}	Asynchronous Register Clear Time	Com'l		6		7			ns
		Mil				7		8	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	6		7				ns
		Mil			7		8		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	6		7				ns
		Mil			7		8		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l		16		20			ns
		Mil				20		24	

Notes:

24. t_{OD} is specified with $C_L = 35$ pF.
25. t_{ZX} is specified with $C_L = 35$ pF. Sample tested only for an output change of 500 mV.
26. t_{XZ} is specified with $C_L = 5$ pF.
27. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

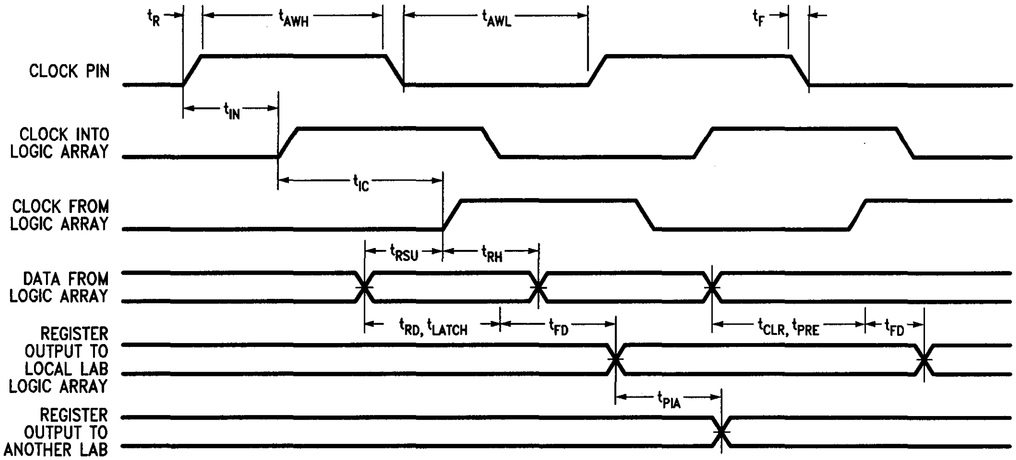
Switching Waveforms (Continued)

Internal Combinatorial



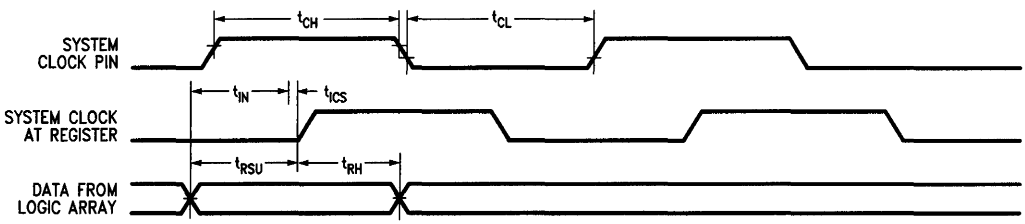
0175-16

Internal Asynchronous



0175-17

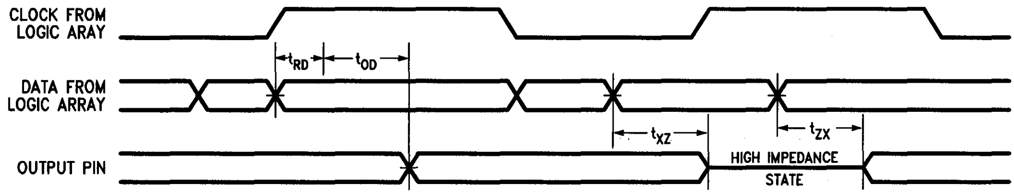
Internal Synchronous



0175-18

Switching Waveforms (Continued)

Internal Synchronous



0175–19

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C342-30HC	H81	Commercial
	CY7C342-30JC	J81	
	CY7C342-30RC	R68	
	CY7C342-30GC	G68	
35	CY7C342-35HC	H81	Commercial
	CY7C342-35JC	J81	
	CY7C342-35RC	R68	
	CY7C342-35GC	G68	
	CY7C342-35HMB	H81	Military
	CY7C342-35RMB	R68	
40	CY7C342-40HC	H81	Commercial
	CY7C342-40JC	J81	
	CY7C342-40RC	R68	
	CY7C342-40GC	G68	
	CY7C342-40HMB	H81	Military
	CY7C342-40RMB	R68	

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C345-30HC	H67	Commercial
	CY7C345-30JC	J67	
35	CY7C345-35HC	H67	Commercial
	CY7C345-35JC	J67	
	CY7C345-35HMB	H67	Military
40	CY7C345-40HC	H67	Commercial
	CY7C345-40JC	J67	
	CY7C345-40HMB	H67	Military

CYPRESS SEMICONDUCTOR

64-Macrocell MAX™ EPLD

Features

- **64 MAX macrocells in 4 LABs**
- **8 dedicated inputs, 28 three-stateable, bidirectional I/O pins**
- **Programmable interconnect array**
- **Available in 44-pin HLCC, PLCC**

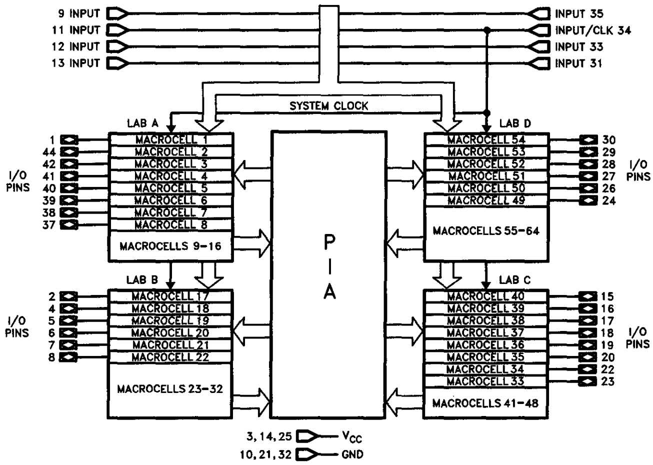
Functional Description

The CY7C343 is a high-performance, high-density erasable programmable logic device, available in 44-pin PLCC and HLCC packages.

The CY7C343 contains 64 highly flexible macrocells and 128 expander product terms. These resources are divided into four Logic Array Blocks (LABs) connected through the Programmable Interconnect Array (PIA). There are 8 dedicated input pins, one of which doubles as a clock pin if needed. The CY7C343 also has 28 I/O pins, each connected to a macrocell (eight for LABs A and C and six for LABs B and D). The remaining 36 macrocells are used for embedded logic.

The CY7C343 is excellent for a wide range of applications both synchronous and asynchronous.

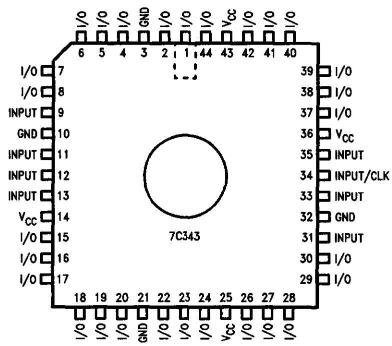
Logic Block Diagram



0185-1

Pin Configuration

HLCC
Top View



0185-2

Selection Guide

		7C343-30	7C343-35	7C343-40
Maximum Access Time (ns)		30	35	40
Maximum Operating Current (mA)	Commercial	155	155	
	Military		160	160
Maximum Standby Current (mA)	Commercial	100	100	
	Military		120	120

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . −65°C to +150°C

Ambient Temperature with
Power Applied . . . . 0°C to +70°C

Maximum Junction Temperature
(Under Bias) . . . . 150°C

Supply Voltage to Ground Potential . . . . −2.0V to +7.0V

Maximum Power Dissipation . . . . 2500 mW

DC V_{CC} or GND Current . . . . 500 mA

DC Output Current, per Pin . . . . −25 mA to +25 mA

DC Input Voltage[1] . . . . −2.0V to +7.0V

DC Program Voltage. . . . . −2.0V to +13.5V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to +125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−30	−90	mA
I_{CC1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		100	mA
			Military		120	mA
I_{CC2}	Power Supply Current[3]	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[3]	Commercial		155	mA
			Military		160	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	12	

Notes:

1. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
2. Typical values are for T_A = 25°C and V_{CC} = 5V.
3. Measured with device programmed as a 16-bit counter in each LAB. This parameter is tested periodically by sampling production material.
4. *Figure 1a* test load used for all parameters except t_{ER} and t_{EA}. *Figure 1b* test load used for t_{ER} and t_{EA}. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[4]

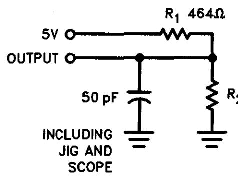
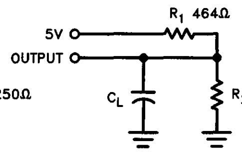
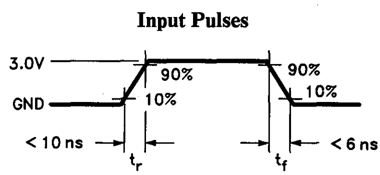


Figure 1a



0185-4

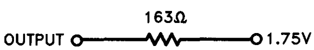
Figure 1b



0185-5

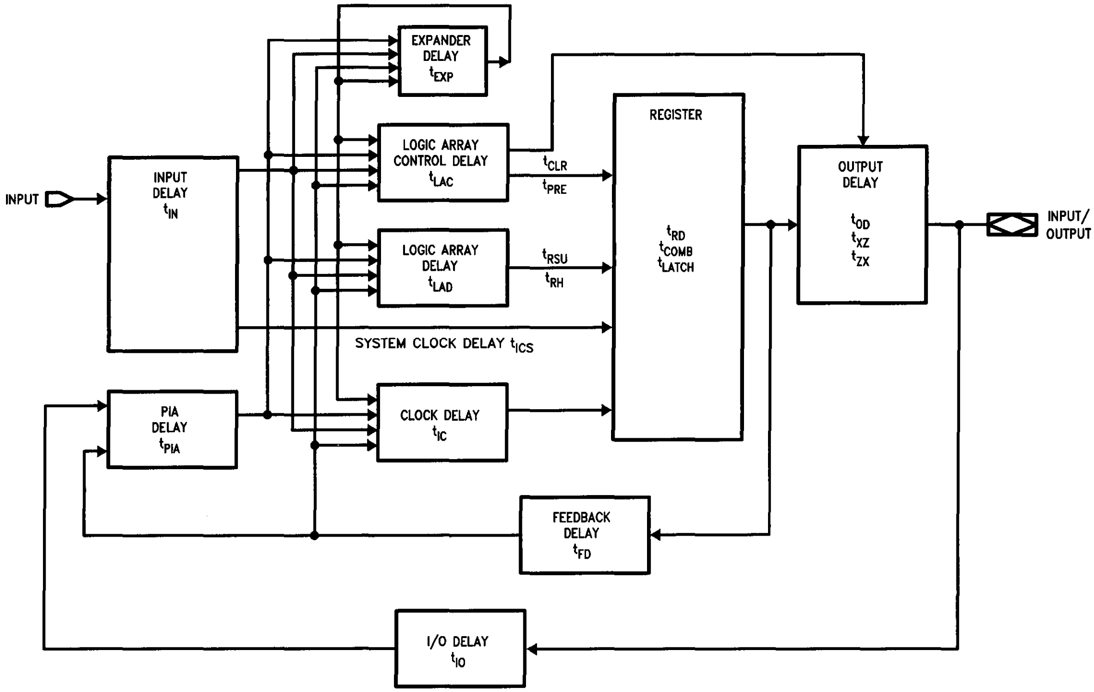
Figure 2

Equivalent to: THÉVENIN EQUIVALENT (Commercial/Military)



0185-6

CY7C343 Timing Model



0185–3

4

Programmable Interconnect Array

The Programmable Interconnect Array (PIA) solves interconnect limitations by routing only the signals needed by each logic array block. The inputs to the PIA are the outputs of every macrocell within the device and the I/O pin feedback of every pin on the device.

Unlike masked or programmable gate arrays, which induce variable delay dependent on routing, the PIA has a fixed delay. This eliminates undesired skews among logic signals, which may cause glitches in internal or external logic. The fixed delay, regardless of programmable interconnect array configuration, simplifies design by assuring that internal signal skews or races are avoided. The result is ease of design implementation, often in a single pass, without the multiple internal logic placement and routing iterations required for a programmable gate array to achieve design timing objectives.

Timing Delays

Timing delays within the CY7C343 may be easily determined using MAX + PLUS™ software or by the model shown in *Figure 3*. The CY7C343 has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the MAX + PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C343 contains circuitry to protect device pins from high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND (V_{IN} or V_{OUT}) V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device. Decoupling capacitors should have good frequency response, such as monolithic ceramic types.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders add the maximum expander delay t_{EXP} to the overall delay. Similarly, there is an additional t_{PIA} delay for an input from an I/O pin when compared to a signal from a straight input pin.

When calculating synchronous frequencies, use t_{S1} if all inputs are on the input pins. t_{S2} should be used if data is applied at an I/O pin. If t_{S2} is greater than t_{CO1}, $1/t_{S2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO1}$, or $1/(t_{EXP} + t_{S1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS2} must be used as the required set up time. If $(t_{AS2} + t_{AH})$ is greater than t_{ACO1}, $1/(t_{AS2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO1}$, or $1/(t_{EXP} + t_{AS1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C343.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

External Synchronous Switching Characteristics[4] Over Operating Range

Parameters	Description		CY7C343-30 Min.	CY7C343-30 Max.	CY7C343-35 Min.	CY7C343-35 Max.	CY7C343-40 Min.	CY7C343-40 Max.	Units
t_{PD1}	Dedicated Input to Combinatorial Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{PD2}	I/O Input to Combinatorial Output Delay[6]	Com'l		45		55			ns
		Mil				55		65	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[7]	Com'l		47		55			ns
		Mil				55		62	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[8]	Com'l		64		72			ns
		Mil				72		80	
t_{EA}	Input to Output Enable Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{ER}	Input to Output Disable Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l		16		20			ns
		Mil				20		23	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[9]	Com'l		40		45			ns
		Mil				45		50	
t_{S1}	Dedicated Input or Feedback Setup Time to Synchronous Clock Input[5, 10]	Com'l	22		25				ns
		Mil			25		28		
t_{S2}	I/O Input Setup Time to Synchronous Clock Input[5]	Com'l	39		42				ns
		Mil			42		45		
t_H	Input Hold Time from Synchronous Clock Input[5]	Com'l	0		0				ns
		Mil			0		0		
t_{WH}	Synchronous Clock Input High Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{WL}	Synchronous Clock Input Low Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{RW}	Asynchronous Clear Width[5]	Com'l	30		35				ns
		Mil			35		40		
t_{RR}	Asynchronous Clear Recovery Time[5]	Com'l	30		35				ns
		Mil			35		40		
t_{RO}	Asynchronous Clear to Registered Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{PW}	Asynchronous Preset Width[5]	Com'l	30		35				ns
		Mil			35		40		
t_{PR}	Asynchronous Preset Recovery Time[5]	Com'l	30		35				ns
		Mil			35		40		
t_{PO}	Asynchronous Preset to Registered Output Delay[5]	Com'l		30		35			ns
		Mil				35		40	
t_{CF}	Synchronous Clock to Local Feedback Input[11]	Com'l		3		6			ns
		Mil				6		9	
t_P	External Synchronous Clock Period ($t_{CO1} + t_{S1}$)	Com'l	37		43				ns
		Mil			45		51		

4

External Synchronous Switching Characteristics[4] Over Operating Range (Continued)

Parameters	Description		CY7C343-30		CY7C343-35		CY7C343-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX1}	External Maximum Frequency $(1/(t_{CO1} + t_{S1}))$[12]	Com'l	27.0		23.2				MHz
		Mil			22.2		19.6		
f_{MAX2}	Internal Local Feedback Maximum Frequency, lesser of $1/(t_{S1} + t_{CF})$ or $(1/t_{CO1})$[13]	Com'l	40.0		32.2				MHz
		Mil			33.3		28.5		
f_{MAX3}	Data Path Maximum Frequency, least of $(1/(t_{WL} + t_{WH}))$, $(1/(t_{S1} + t_H))$ or $(1/t_{CO1})$[14]	Com'l	45.4		40.0				MHz
		Mil			40.0		30.0		
f_{MAX4}	Maximum Register Toggle Frequency $1/(t_{WL} + t_{WH})$[15]	Com'l	50.0		40.0				MHz
		Mil			40.0		30.0		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[16]	Com'l	3		3				ns
		Mil			3		3		

Notes:

5. This specification is a measure of the delay from input signal applied to a dedicated input, (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
   When this note is applied to any parameter specification it indicates that the signal (data, asynchronous clock, asynchronous clear, and/or asynchronous preset) is applied to a dedicated input only and no signal path (either clock or data) employs expander logic.
   If an input signal is applied to an I/O pin an additional delay equal to t_{PIA} should be added.
   If expanders are used add the maximum expander delay t_{EXP} to the overall delay.
6. This specification is a measure of the delay from input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
7. This specification is a measure of the delay from an input signal applied to a dedicated input, (44-pin PLCC input pin 9, 11, 12, 13, 31, 33, 34, or 35) to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
8. This specification is a measure of the delay from an input signal applied to an I/O macrocell pin to any output. This delay assumes expander terms are used to form the logic function and includes the worst case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
9. This specification is a measure of the delay from synchronous register clock to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used, register is synchronously clocked and all feedback is within the same LAB. This parameter is tested periodically by sampling production material.
10. If data is applied to an I/O input for capture by a macrocell register, the I/O pin input set-up time minimums should be observed. These parameters are t_{S1} for synchronous operation and t_{AS2} for asynchronous operation.
11. This specification is a measure of the delay associated with the internal register feedback path. This is the delay from synchronous clock to LAB logic array input. This delay plus the register set-up time, t_{S1}, is the minimum internal period for an internal synchronous state machine configuration. This delay is for feedback within the same LAB. This parameter is tested periodically by sampling production material.
12. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which a state machine configuration with external feedback can operate. It is assumed that all data inputs and feedback signals are applied to dedicated inputs.
13. This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{CO1}$. All feedback is assumed to be local, originating within the same LAB.
14. This frequency indicates the maximum frequency at which the device may operate in data path mode. This delay assumes data input signals are applied to dedicated inputs and no expander logic is used.
15. This specification indicates the guaranteed maximum frequency, in synchronous mode, at which an individual output or buried register can be cycled.
16. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Asynchronous Switching Characteristics[4] Over Operating Range

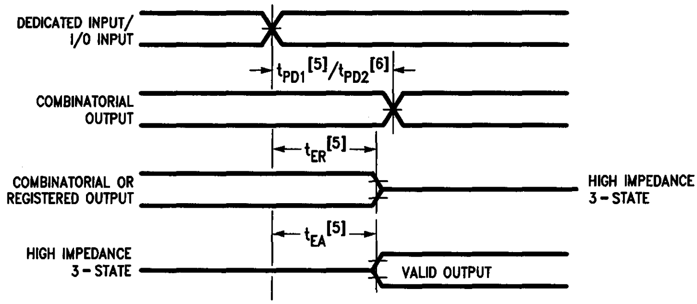
Parameters	Description		CY7C343-30		CY7C343-35		CY7C343-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACO1}	Asynchronous Clock Input to Output Delay[5]	Com'l		30		35			ns
		Mil		30		35		45	
t_{ACO2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[17]	Com'l		50		60			ns
		Mil				60		70	
t_{AS1}	Dedicated Input or Feedback Setup Time to Asynchronous Clock Input[5]	Com'l	10		10				ns
		Mil			10		10		
t_{AS2}	I/O Input Setup Time to Asynchronous Clock Input[5]	Com'l	27		30				ns
		Mil			30		33		
t_{AH}	Input Hold Time from Asynchronous Clock Input[5]	Com'l	15		15				ns
		Mil			15		15		
t_{AWH}	Asynchronous Clock Input High Time[5]	Com'l	25		30				ns
		Mil			30		35		
t_{AWL}	Asynchronous Clock Input Low Time[5]	Com'l	25		30				ns
		Mil			30		35		
t_{ACF}	Asynchronous Clock to Local Feedback Input[18]	Com'l		18		22			ns
		Mil				22		26	
t_{AP}	External Asynchronous Clock Period ($t_{ACO1} + t_{AS1}$) or ($t_{AWH} + t_{AWL}$)	Com'l	50		60				ns
		Mil			60		70		
f_{MAXA1}	External Maximum Frequency in Asynchronous Mode ($1/t_{AP}$)[19]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA2}	Maximum Internal Asynchronous Frequency[22]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA3}	Data Path Maximum Frequency in Asynchronous Mode[21]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
f_{MAXA4}	Maximum Asynchronous Register Toggle Frequency ($1/(t_{AWH} + t_{AWL})$)[20]	Com'l	20		16.6				MHz
		Mil			16.6		14.2		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[23]	Com'l	15		15				ns
		Mil			15		15		

Notes:

17. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the register output signal to the input of the LAB logic array and then to a combinatorial output. This delay assumes no expanders are used in the logic of combinatorial output or the asynchronous clock input. The clock signal is applied to a dedicated input pin and all feedback is within a single LAB. This parameter is tested periodically by sampling production material.
18. This specification is a measure of the delay associated with the internal register feedback path for an asynchronous clock to LAB logic array input. This delay plus the asynchronous register setup time, t_{AS1}, is the minimum internal period for an internal asynchronously clocked state machine configuration. This delay is for feedback within the same LAB, assumes no expander logic in the clock path and assumes that the clock input signal is applied to a dedicated input pin. This parameter is tested periodically by sampling production material.
19. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that all data inputs, clock inputs, and feedback signals are applied to dedicated inputs and that no expander logic is employed in the clock signal path or data path.
20. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to an external dedicated input pin.
21. This frequency is the maximum frequency at which the device may operate in the asynchronously clocked data path mode. This specification is determined by the least of $1/(t_{AWH} + t_{AWL})$, $1/(t_{AS1} + t_{AH})$ or $1/t_{ACO1}$. It asssumes data and clock input signals are applied to dedicated input pins and no expander logic is used.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. This parameter is determined by the lesser of $(1/(t_{ACF} + t_{AS}))$ or $(1/(t_{AWH} + t_{AWL}))$. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO1}$.
    This specification assumes no expander logic is utilized, all data inputs and clock inputs are applied to dedicated inputs, and all state feedback is within a single LAB. This parameter is tested periodically by sampling production material.
23. This parameter indicates the minimum time that the previous register output data is maintained on the output after an asynchronous register clock input.

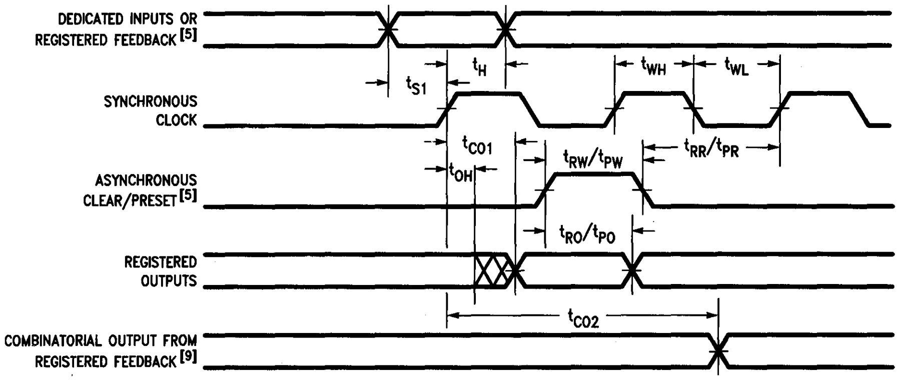
Switching Waveforms

External Combinatorial



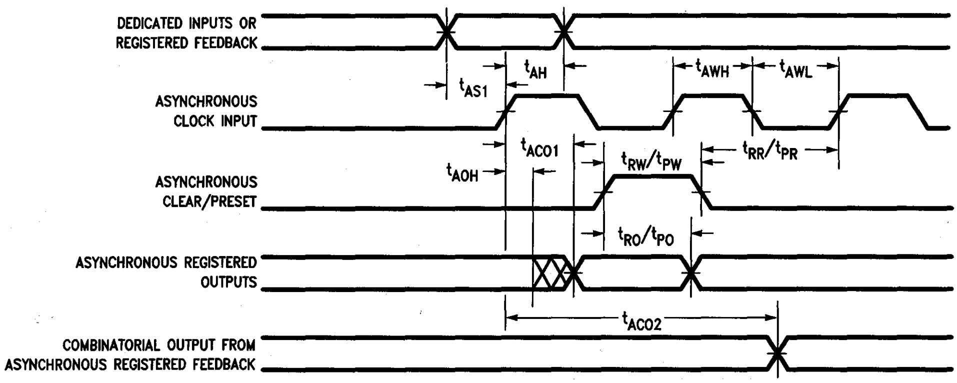
0185-7

External Synchronous



0185-8

External Asynchronous



0185-9

Internal Switching Characteristics[1] Over Operating Range

Parameters	Description		CY7C343-30 Min.	CY7C343-30 Max.	CY7C343-35 Min.	CY7C343-35 Max.	CY7C343-40 Min.	CY7C343-40 Max.	Units
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		7		9			ns
		Mil				9		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		5		7			ns
		Mil				7		9	
t_{EXP}	Expander Array Delay	Com'l		14		20			ns
		Mil				20		25	
t_{LAD}	Logic Array Data Delay	Com'l		14		16			ns
		Mil				16		18	
t_{LAC}	Logic Array Control Delay	Com'l		12		13			ns
		Mil				13		14	
t_{OD}	Output Buffer and Pad Delay[24]	Com'l		5		6			ns
		Mil				6		7	
t_{ZX}	Output Buffer Enable Delay[25]	Com'l		11		13			ns
		Mil				13		15	
t_{XZ}	Output Buffer Disable Delay[26]	Com'l		11		13			ns
		Mil				13		15	
t_{RSU}	Register Setup Time Relative to Clock Signal at Register	Com'l	8		8				ns
		Mil			8		8		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	8		12				ns
		Mil			12		14		
t_{LATCH}	Flow Through Latch Delay	Com'l		4		4			ns
		Mil				4		4	
t_{RD}	Register Delay	Com'l		2		2			ns
		Mil				2		2	
t_{COMB}	Transparent Mode Delay[27]	Com'l		4		4			ns
		Mil				4		4	
t_{CH}	Clock High Time	Com'l	10		12.5				ns
		Mil			12.5		15		
t_{CL}	Clock Low Time	Com'l	10		12.5				ns
		Mil			12.5		15		

Notes:

24. t_{OD} is specified with $C_L = 35$ pF.
25. t_{ZX} is specified with $C_L = 35$ pF. Sample tested only for an output change of 500 mV.
26. t_{XZ} is specified with $C_L = 5$ pF.
27. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

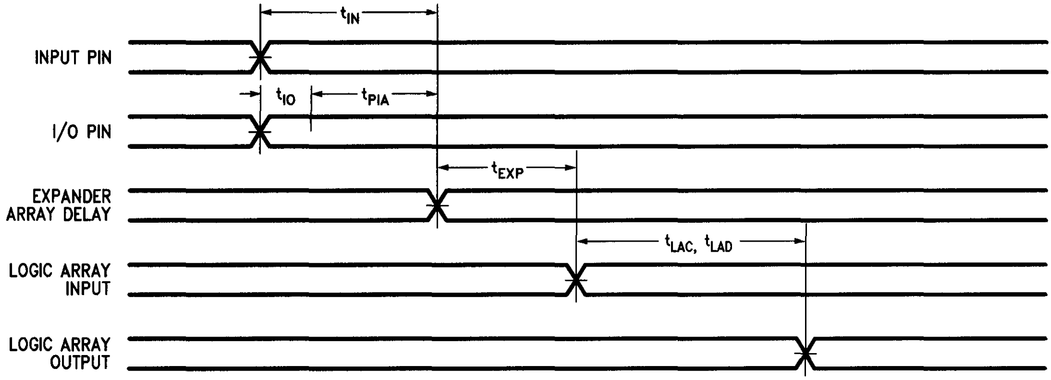
4

Internal Switching Characteristics[19] Over Operating Range (Continued)

Parameters	Description		CY7C343-30		CY7C343-35		CY7C343-40		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IC}	Asynchronous Clock Logic Delay	Com'l		16		18			ns
		Mil				18		20	
t_{ICS}	Synchronous Clock Delay	Com'l		2		3			ns
		Mil				3		4	
t_{FD}	Feedback Delay	Com'l		1		2			ns
		Mil				2		3	
t_{PRE}	Asynchronous Register Preset Time	Com'l		6		7			ns
		Mil				7		8	
t_{CLR}	Asynchronous Register Clear Time	Com'l		6		7			ns
		Mil				7		8	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	6		7				ns
		Mil			7		8		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	6		7				ns
		Mil			7		8		
t_{PIA}	Programmable Interconnect Array Delay Time	Com'l		16		20			ns
		Mil				20		24	

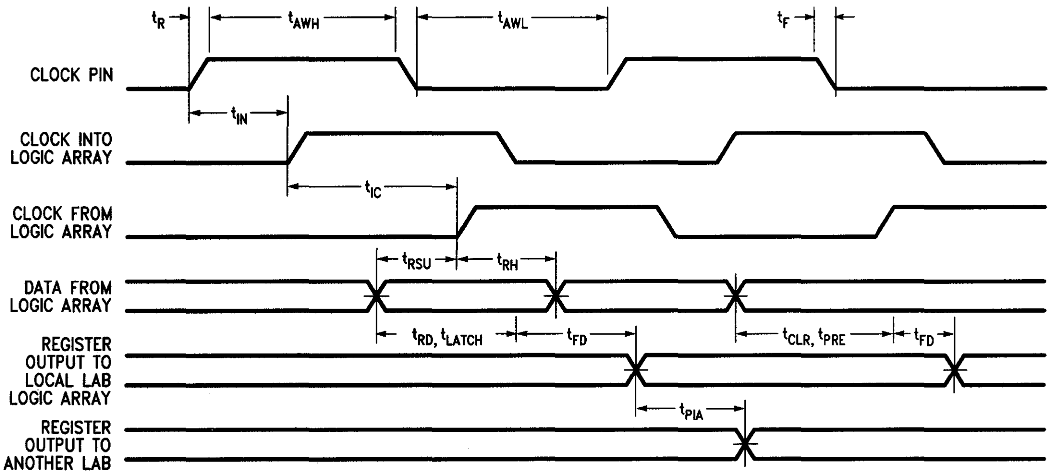
Switching Waveforms

Internal Combinatorial



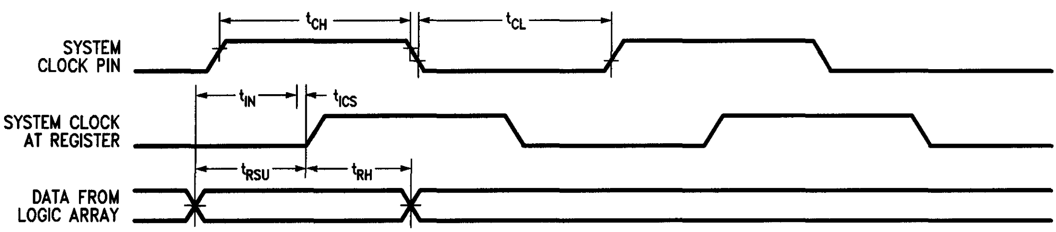
0185–10

Internal Asynchronous



0185–11

Internal Synchronous

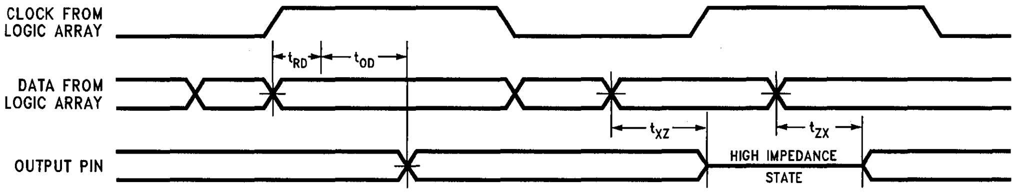


0185–12

4

Switching Waveforms (Continued)

Output Mode



0185–13

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C343-30HC	H67	Commercial
	CY7C343-30JC	J67	
35	CY7C343-35HC	H67	Commercial
	CY7C343-35JC	J67	
	CY7C343-35HMB	H67	Military
40	CY7C343-40HMB	H67	Military

Document #: 38-00128

CYPRESS SEMICONDUCTOR

32-Macrocell MAX™ EPLD

Features

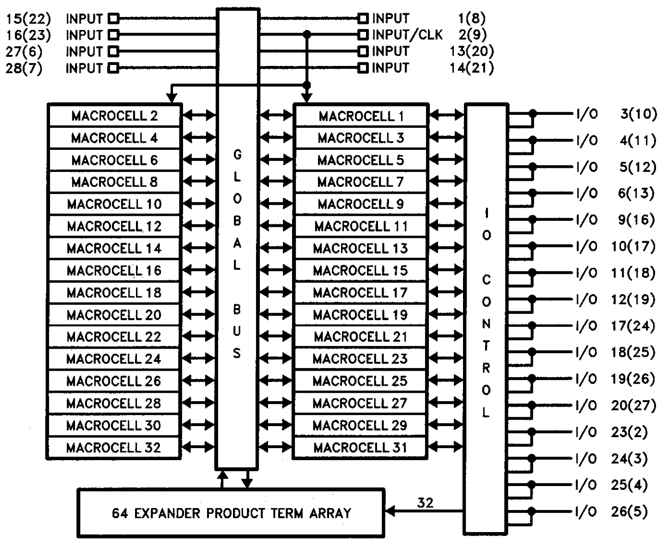
- **High-performance, high-density replacement for TTL, 74HC, and custom logic**
- **32 macrocells, 64 expander product terms in one LAB**
- **8 dedicated inputs, 16 I/O pins**
- **28-pin 300-mil DIP, Cerdip or 28-pin HLCC, PLCC package**

Functional Description

Available in a 28-pin 300-mil DIP or windowed J-leaded ceramic chip carrier (HLCC), the CY7C344 represents the densest EPLD of this size. 8 dedicated inputs and 16 bi-directional I/O pins communicate to one logic array block. In the CY7C344 LAB there are 32 macrocells and 64 expander product terms. Even if all of the I/O pins are driven by macrocell registers, there are still 16 "buried" registers available. All inputs, macrocells, and I/O pins are interconnected within the LAB.

The speed and density of the CY7C344 makes it a natural for all types of applications. With just this one device, the designer can implement complex state machines, registered logic, and combinatorial "glue" logic, without using multiple chips. This architectural flexibility allows the CY7C344 to replace multi-chip TTL solutions, whether they are synchronous, asynchronous, combinatorial, or all three.

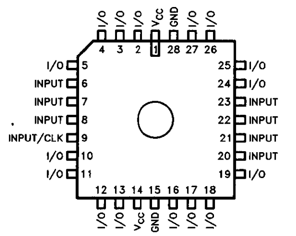
Logic Block Diagram[1]



0184-1

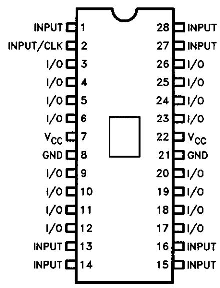
Pin Configurations

HLCC
Top View



0184-2

Cerdip
Top View



0184-3

Selection Guide

		7C344-20	7C344-25	7C344-35
Maximum Access Time (ns)		20	25	30
Maximum Operating Current (mA)	Commercial	200	200	
	Military		220	220
Maximum Standby Current (mA)	Commercial	150	150	
	Military		170	170

Note:

1. Figures in ( ) are for J-leaded packages.

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... 0°C to +70°C

Maximum Junction Temperature (Under Bias) .... 150°C

Supply Voltage to Ground Potential .... −2.0V to +7.0V

Maximum Power Dissipation .... 1500 mW

DC V_{CC} or GND Current .... 500 mA

DC Output Current, per Pin .... −25 mA to +25 mA

DC Input Voltage[2] .... −2.0V to +7.0V

DC Program Voltage................ −2.0V to +13.5V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±5%
Industrial	−40°C to +85°C	5V ±10%
Military	−55°C to +125°C (Case)	5V ±10%

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA			0.45	V
V_{IH}	Input HIGH Level			2.2	V_{CC}+0.3	V
V_{IL}	Input LOW Level			−0.3	0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	V_O = V_{CC} or GND		−40	+40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		−30	−90	mA
I_{CC_1}	Power Supply Current (Standby)	V_I = V_{CC} or GND (No Load)	Commercial		150	mA
			Military		170	mA
I_{CC_2}	Power Supply Current	V_I = V_{CC} or GND (No Load) f = 1.0 MHz[4]	Commercial		200	mA
			Military		220	mA

Capacitance

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 2V, f = 1.0 MHz	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V, f = 1.0 MHz	12	

Notes:

2. Minimum DC input is −0.3V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns.
3. Typical values are for T_A = 25°C and V_{CC} = 5V.
4. Measured with device programmed as a 16-bit counter. This parameter is tested periodically by sampling production material.
5. *Figure 1a* test load used for all parameters except t_{ER} and t_{EA}. *Figure 1b* test load used for t_{ER} and t_{EA}. All external timing parameters are measured referenced to external pins of the device.

AC Test Loads and Waveforms[5]

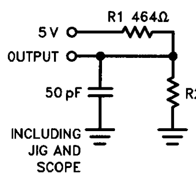
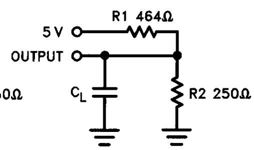


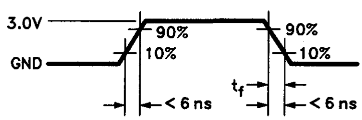
Figure 1a



0184-5

Figure 1b

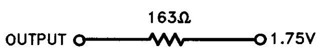
Input Pulses



0184-6

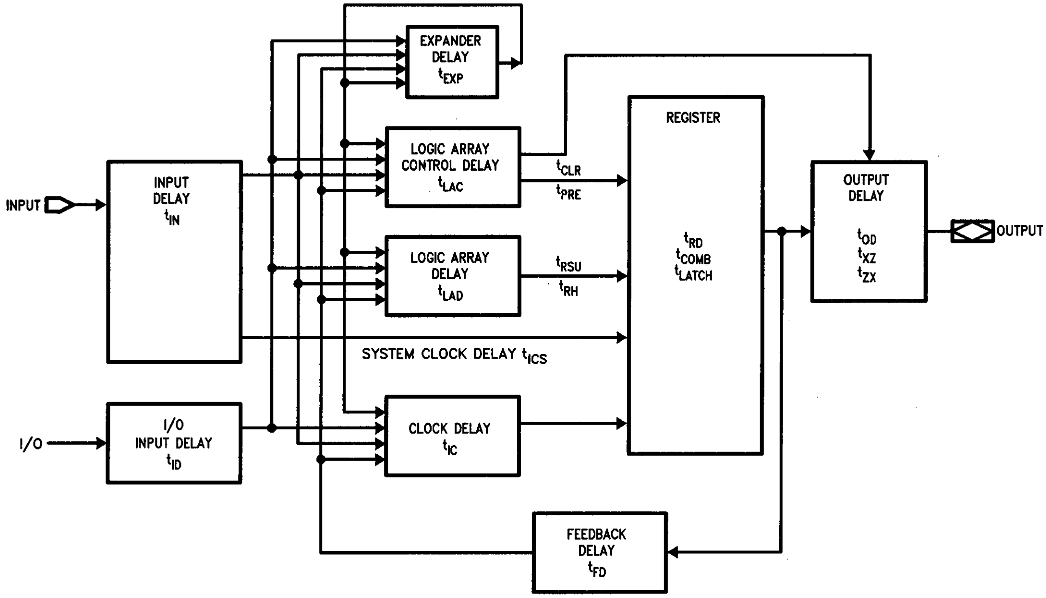
Figure 2

Equivalent to: THÉVENIN EQUIVALENT (Commercial/Military)



0184-7

CY7C344 Timing Model



0184–4

Timing Delays

Timing delays within the CY7C344 may be easily determined using MAX+PLUS™ software or by the model shown in *Figure 3*. The CY7C344 has fixed internal delays, allowing the user to determine the worst case timing delays for any design. For complete timing information the MAX+PLUS software provides a timing simulator.

Design Recommendations

Operation of the devices described herein with conditions above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability. The CY7C344 contains circuitry to protect device pins from high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND (V_{IN} or V_{OUT}) V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected together directly at the device. Power supply decoupling capacitors of at least 0.2 μF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled.

Timing Considerations

Unless otherwise stated, propagation delays do not include expanders. When using expanders add the maximum expander delay t_{EXP} to the overall delay.

When calculating synchronous frequencies, use t_{S_1} if all inputs are on the input pins. t_{S_2} should be used if data is applied at an I/O pin. If t_{S_2} is greater than t_{CO_1}, $1/t_{S_2}$ becomes the limiting frequency in the data path mode unless $1/(t_{WH} + t_{WL})$ is less than $1/t_{S_2}$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{S_1}. Determine which of $1/(t_{WH} + t_{WL})$, $1/t_{CO_1}$, or $1/(t_{EXP} + t_{S_1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the synchronous configuration.

When calculating external asynchronous frequencies, use t_{AS_1} if all inputs are on dedicated input pins. If any data is applied to an I/O pin, t_{AS_2} must be used as the required set up time. If $(t_{AS_2} + t_{AH})$ is greater than t_{ACO_1}, $1/(t_{AS_2} + t_{AH})$ becomes the limiting frequency in the data path mode unless $1/(t_{AWH} + t_{AWL})$ is less than $1/(t_{AS_2} + t_{AH})$.

When expander logic is used in the data path, add the appropriate maximum expander delay, t_{EXP} to t_{AS_1}. Determine which of $1/(t_{AWH} + t_{AWL})$, $1/t_{ACO_1}$, or $1/(t_{EXP} + t_{AS_1})$ is the lowest frequency. The lowest of these frequencies is the maximum data path frequency for the asynchronous configuration.

Timing Considerations (Continued)

The parameter t_{OH} indicates the system compatibility of this device when driving other synchronous logic with positive input hold times, which is controlled by the same synchronous clock. If t_{OH} is greater than the minimum required input hold time of the subsequent synchronous logic, then the devices are guaranteed to function properly with a common synchronous clock under worst-case environmental and supply voltage conditions.

The parameter t_{AOH} indicates the system compatibility of this device when driving subsequent registered logic with a positive hold time and using the same clock as the CY7C344.

In general, if t_{AOH} is greater than the minimum required input hold time of the subsequent logic (synchronous or asynchronous) then the devices are guaranteed to function properly under worst-case environmental and supply voltage conditions, provided the clock signal source is the same. This also applies if expander logic is used in the clock signal path of the driving device, but not for the driven device. This is due to the expander logic in the second device's clock signal path adding an additional delay (t_{EXP}) causing the output data from the preceding device to change prior to the arrival of the clock signal at the following device's register.

External Synchronous Switching Characteristics[5] Over Operating Range

Parameters	Description		CY7C344-20		CY7C344-25		CY7C344-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}	Dedicated Input to Combinatorial Output Delay[6]	Com'l		20		25			ns
		Mil				25		35	
t_{PD2}	I/O Input to Combinatorial Output Delay[7]	Com'l		20		25			ns
		Mil				25		35	
t_{PD3}	Dedicated Input to Combinatorial Output Delay with Expander Delay[8]	Com'l		30		40			ns
		Mil				40		60	
t_{PD4}	I/O Input to Combinatorial Output Delay with Expander Delay[9]	Com'l		30		40			ns
		Mil				40		60	
t_{EA}	Input to Output Enable Delay	Com'l		20		25			ns
		Mil				25		35	
t_{ER}	Input to Output Disable Delay	Com'l		20		25			ns
		Mil				25		35	
t_{CO1}	Synchronous Clock Input to Output Delay	Com'l		12		15			ns
		Mil				15		23	
t_{CO2}	Synchronous Clock to Local Feedback to Combinatorial Output[10]	Com'l		22		30			ns
		Mil				30		46	
t_S	Dedicated Input or Feedback Setup Time to Synchronous Clock Input	Com'l	12		15				ns
		Mil			15		21		
t_H	Input Hold Time from Synchronous Clock Input[5]	Com'l	1		2.5				ns
		Mil			2.5		2.5		
t_{WH}	Synchronous Clock Input High Time	Com'l	7		8				ns
		Mil			8		10		
t_{WL}	Synchronous Clock Input Low Time	Com'l	7		8				ns
		Mil			8		10		
t_{RW}	Asynchronous Clear Width	Com'l	23		28				ns
		Mil			28		33		
t_{RR}	Asynchronous Clear Recovery Time	Com'l	20		25				ns
		Mil			25		35		
t_{RO}	Asynchronous Clear to Registered Output Delay	Com'l		23		28			ns
		Mil				28		33	
t_{PW}	Asynchronous Preset Width	Com'l	23		28				ns
		Mil			28		33		
t_{PR}	Asynchronous Preset Recovery Time	Com'l		23		28			ns
		Mil				28		38	

External Synchronous Switching Characteristics[5] Over Operating Range (Continued)

Parameters	Description		CY7C344-20 Min.	CY7C344-20 Max.	CY7C344-25 Min.	CY7C344-25 Max.	CY7C344-35 Min.	CY7C344-35 Max.	Units
t_{PO}	Asynchronous Preset to Registered Output Delay	Com'l		23		28			ns
		Mil				28		33	
t_{CF}	Synchronous Clock to Local Feedback Input[11]	Com'l		4		7			ns
		Mil				7		13	
t_P	External Synchronous Clock Period ($t_{CO_1} + t_S$)	Com'l	24		30				ns
		Mil			30		44		
f_{MAX_1}	External Maximum Frequency ($1/(t_{CO_1} + t_S)$)[12]	Com'l	41.6		33.3				MHz
		Mil			33.3		22.7		
f_{MAX_2}	Maximum Frequency with Internal Only Feedback ($1/(t_{CF} + t_S)$)[13]	Com'l	62.5		45.4				MHz
		Mil			45.4		29.4		
f_{MAX_3}	Data Path Maximum Frequency, least of $1/(t_{WL} + t_{WH})$, $(1/(t_{S_1} + t_H))$ or $(1/t_{CO_1})$[14]	Com'l	71.4		57.1				MHz
		Mil			57.1		42.5		
f_{MAX_4}	Maximum Register Toggle Frequency $1/(t_{WH} + t_{WL})$[15]	Com'l	71.4		62.5				MHz
		Mil			62.5		50.0		
t_{OH}	Output Data Stable Time from Synchronous Clock Input[16]	Com'l	3		3				ns
		Mil			3		3		

Notes:

6. This parameter is the delay from an input signal applied to a dedicated input pin to a combinatorial output on any output pin. This delay assumes no expander terms are used to form the logic function.
7. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output. This delay assumes no expander terms are used to form the logic function.
8. This parameter is the delay associated with an input signal applied to a dedicated input pin to combinatorial output on any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
9. This parameter is the delay associated with an input signal applied to an I/O macrocell pin to any output pin. This delay assumes expander terms are used to form the logic function and includes the worst-case expander logic delay for one pass through the expander logic. This parameter is tested periodically by sampling production material.
10. This specification is a measure of the delay from synchronous register clock input to internal feedback of the registered output signal to a combinatorial output for which the registered output signal is used as an input. This parameter assumes that no expanders are used in the logic of the combinatorial output and the register is synchronously clocked. This parameter is tested periodically by sampling production material.
11. This specification is a measure of the delay associated with the internal register feedback path. This delay plus the register setup time, t_S, is the minimum internal period for an internal state machine configuration. This parameter is tested periodically by sampling production material.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external only feedback can operate.
13. This specification indicates the guaranteed maximum frequency at which a state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as it is less than $1/t_{CO_1}$. This specification assumes no expander logic is used. This parameter is tested periodically by sampling production material.
14. This frequency indicates the maximum frequency at which the device may operate in data path mode (dedicated input pin to output pin). This assumes that no expander logic is used.
15. This specification indicates the guaranteed maximum frequency in synchronous mode, at which an individual output or buried register can be cycled by a clock signal applied to either a dedicated input pin or an I/O pin.
16. This parameter indicates the minimum time after a synchronous register clock input that the previous register output data is maintained on the output pin.

External Asynchronous Switching Characteristics[5] Over Operating Range

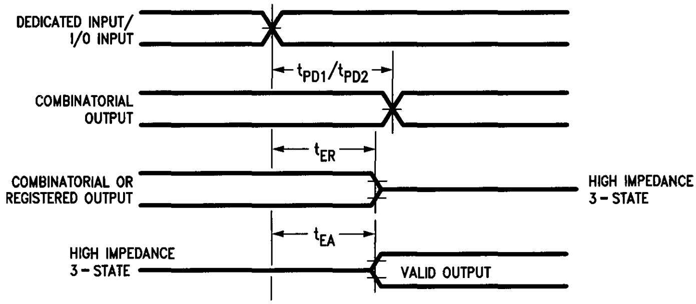
Parameters	Description		CY7C344-20 Min.	CY7C344-20 Max.	CY7C344-25 Min.	CY7C344-25 Max.	CY7C344-35 Min.	CY7C344-35 Max.	Units
t_{ACO_1}	Asynchronous Clock Input to Output Delay	Com'l		20		25			ns
		Mil				25		35	
t_{ACO_2}	Asynchronous Clock Input to Local Feedback to Combinatorial Output[17]	Com'l		38		46			ns
		Mil				46		62	
t_{AS}	Dedicated Input or Feedback Setup Time to Asynchronous Clock Input	Com'l	9		12				ns
		Mil			12		15		
t_{AH}	Input Hold Time from Asynchronous Clock Input	Com'l	9		12				ns
		Mil			12		17.5		
t_{AWH}	Asynchronous Clock Input High Time	Com'l	15		20				ns
		Mil			20		30		
t_{AWL}	Asynchronous Clock Input Low Time	Com'l	15		20				ns
		Mil			20		30		
t_{ACF}	Asynchronous Clock to Local Feedback Input[18]	Com'l		18		21			ns
		Mil				21		27	
t_{AP}	External Asynchronous Clock Period ($t_{ACO_1} + t_{AS}$) or ($t_{AWH} + t_{AWL}$)	Com'l	30		40				ns
		Mil			40		60		
f_{MAXA_1}	External Maximum Frequency in Asynchronous Mode ($1/t_{AP}$)[19]	Com'l	33.3		25.0				MHz
		Mil			25.0		16.6		
f_{MAXA_2}	Maximum Internal Asynchronous Frequency $1/(t_{ACF} + t_{AS})$[22]	Com'l	33.3		25.0				MHz
		Mil			25.0		16.6		
f_{MAXA_3}	Data Path Maximum Frequency in Asynchronous Mode[21]	Com'l	33.3		25.0				MHz
		Mil			25.0		16.6		
f_{MAXA_4}	Maximum Asynchronous Register Toggle Frequency $1/(t_{AWH} + t_{AWL})$[20]	Com'l	33.3		25.0				MHz
		Mil			25.0		16.6		
t_{AOH}	Output Data Stable Time from Asynchronous Clock Input[23]	Com'l	15		15				ns
		Mil			15		15		

Notes:

17. This specification is a measure of the delay from an asynchronous register clock input to internal feedback of the registered output signal to a combinatorial output for which the registered output signal is used as an input. Assumes no expanders are used in logic of combinatorial output or the asynchronous clock input. This parameter is tested periodically by sampling production material.
18. This specification is a measure of the delay associated with the internal register feedback path for an asynchronously clocked register. This delay plus the asynchronous register setup time, t_{AS}, is the minimum internal period for an asynchronously clocked state machine configuration. This delay assumes no expander logic in the asynchronous clock path. This parameter is tested periodically by sampling production material.
19. This parameter indicates the guaranteed maximum frequency at which an asynchronously clocked state machine configuration with external feedback can operate. It is assumed that no expander logic is employed in the clock signal path or data input path.
20. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode by a clock signal applied to either a dedicated input or an I/O pin.
21. This specification indicates the guaranteed maximum frequency at which an individual output or buried register can be cycled in asynchronously clocked mode. If this frequency is less than $1/t_{ACO_1}$ or $1/(t_{AH} + t_{AS})$. It also indicates the maximum frequency at which the device may operate in the asynchronously clocked data path mode. Assumes no expander logic is used.
22. This specification indicates the guaranteed maximum frequency at which an asynchronously clocked state machine with internal only feedback can operate. If register output states must also control external points, this frequency can still be observed as long as this frequency is less than $1/t_{ACO_1}$. This specification assumes no expander logic is utilized. This parameter is tested periodically by sampling production material.
23. This parameter indicates the minimum time that the previous register output data is maintained on the output pin after an asynchronous register clock input to an external dedicated input or I/O pin.

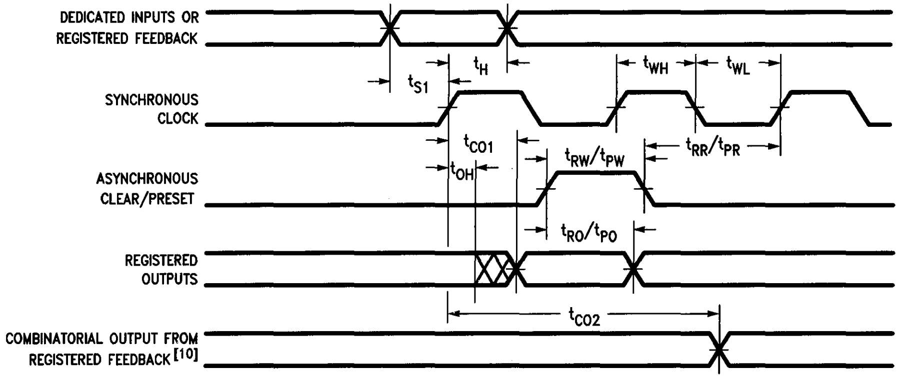
Switching Waveforms

External Combinatorial



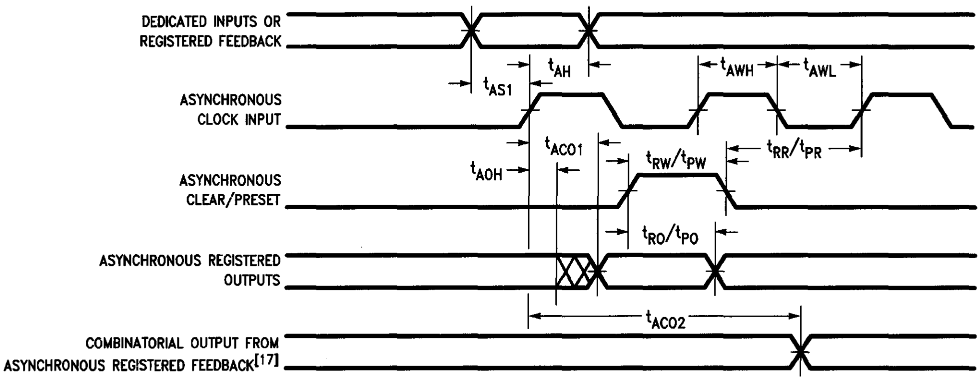
0184-8

External Synchronous



0184-9

External Asynchronous



0184-10

Internal Switching Characteristics[22] Over Operating Range

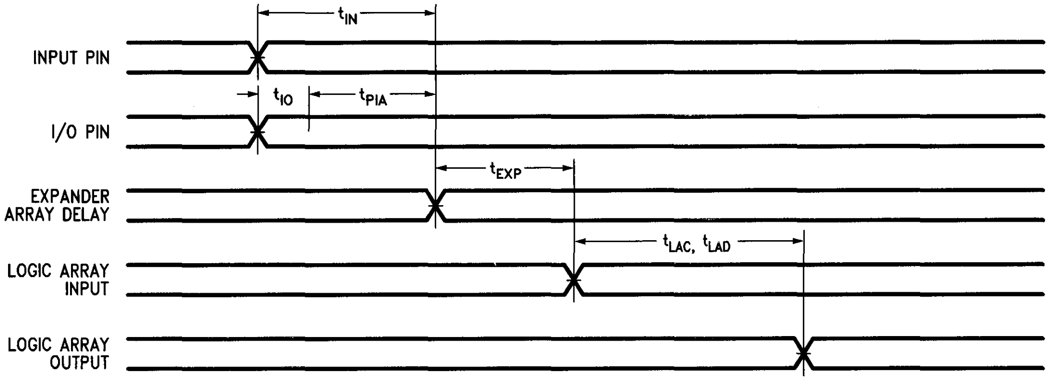
Parameters	Description		CY7C344-20		CY7C344-25		CY7C344-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{IN}	Dedicated Input Pad and Buffer Delay	Com'l		5		7			ns
		Mil				7		11	
t_{IO}	I/O Input Pad and Buffer Delay	Com'l		5		7			ns
		Mil				7		11	
t_{EXP}	Expander Array Delay	Com'l		10		15			ns
		Mil				15		23	
t_{LAD}	Logic Array Data Delay	Com'l		9		10			ns
		Mil				10		12	
t_{LAC}	Logic Array Control Delay	Com'l		7		7			ns
		Mil				7		7	
t_{OD}	Output Buffer and Pad Delay[24]	Com'l		5		5			ns
		Mil				5		5	
t_{ZX}	Output Buffer Enable Delay[25]	Com'l		8		11			ns
		Mil				11		17	
t_{XZ}	Output Buffer Disable Delay[26]	Com'l		8		11			ns
		Mil				11		17	
t_{RSU}	Register Setup Time Relative to Clock Signal at Register	Com'l	5		8				ns
		Mil			8		14		
t_{RH}	Register Hold Time Relative to Clock Signal at Register	Com'l	9		12				ns
		Mil			12		18		
t_{LATCH}	Flow Through Latch Delay	Com'l		1		3			ns
		Mil				3		7	
t_{RD}	Register Delay	Com'l		1		1			ns
		Mil				1		1	
t_{COMB}	Transparent Mode Delay[27]	Com'l		1		3			ns
		Mil				3		7	
t_{CH}	Clock High Time	Com'l	7		8				ns
		Mil			8		9		
t_{CL}	Clock Low Time	Com'l	7		8				ns
		Mil			8		9		
t_{IC}	Asynchronous Clock Logic Delay	Com'l		8		10			ns
		Mil				10		12	
t_{ICS}	Synchronous Clock Delay	Com'l		2		3			ns
		Mil				3		5	
t_{FD}	Feedback Delay	Com'l		1		1			ns
		Mil				1		1	
t_{PRE}	Asynchronous Register Preset Time	Com'l		6		9			ns
		Mil				9		15	
t_{CLR}	Asynchronous Register Clear Time	Com'l		6		9			ns
		Mil				9		15	
t_{PCW}	Asynchronous Preset and Clear Pulse Width	Com'l	6		7				ns
		Mil			7		9		
t_{PCR}	Asynchronous Preset and Clear Recovery Time	Com'l	6		7				ns
		Mil			7		9		

Notes:

24. t_{OD} is specified with $C_L = 35$ pF.
25. t_{ZX} is specified with $C_L = 35$ pF. Sample tested only for an output change of 500 mV.
26. t_{XZ} is specified with $C_L = 5$ pF.
27. This specification guarantees the maximum combinatorial delay associated with the macrocell register bypass when the macrocell is configured for combinatorial operation.

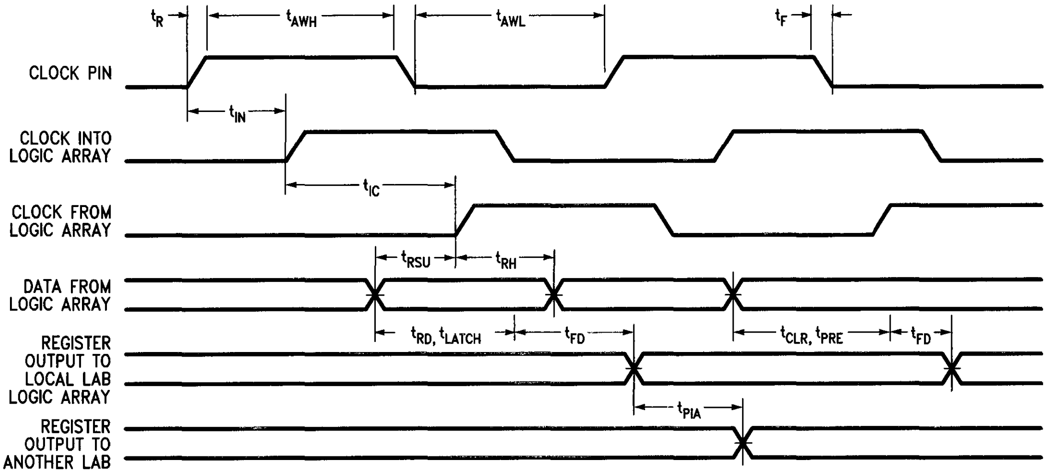
Switching Waveforms

Internal Combinatorial



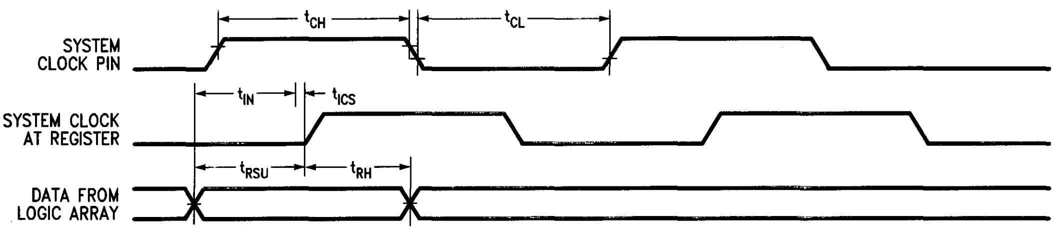
0184–11

Internal Asynchronous



0184–12

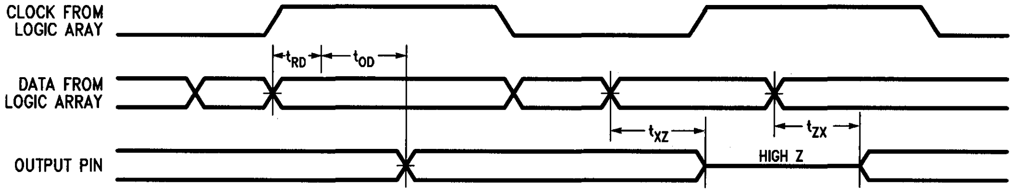
Internal Synchronous (Input Path)



0184–13

Switching Waveforms (Continued)

Internal Synchronous (Output Path)



0184–14

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C344-20PC	P21	Commercial
	CY7C344-20DC	D22	
	CY7C344-20WC	W22	
	CY7C344-20HC	H64	
	CY7C344-20JC	J64	
25	CY7C344-25PC	P21	Commercial
	CY7C344-25DC	D22	
	CY7C344-25WC	W22	
	CY7C344-25HC	H64	
	CY7C344-25JC	J64	
	CY7C344-25HMB	H64	Military
	CY7C344-25WMB	W22	
35	CY7C344-35HMB	H64	Military
	CY7C344-35WMB	W22	

Document #: 38-00127

CYPRESS SEMICONDUCTOR

Ultra High Speed State Machine EPLD

Features

- **High speed: 125 MHz conditional state control sequence generation**
  - **Multiple, concurrent processes**
  - **Multiway branch or join**
  - **Full input field decode**
- **32 synchronous macrocells**
- **Skew-controlled, OR output array**
  - **Outputs are sum of states like PLA**
  - **3 ns skew**
- **Metastable hardened input registers**
  - **10 year MTBF metastable**
  - **Configurable as 0, 1 or 2 stages**
  - **Clock enables on all input registers**
- **8 to 12 inputs, 10 to 14 outputs, 1 clock**
- **Programmable clock doubler and conditioner**
  - **'Squares up' input clock**
- **Security fuse**
- **Space saving 28 pin slim-line DIP package; also available in 28 pin PLCC**
- **Low power "L" versions**
  - **150 mA max at 125 MHz**
- **UV-erasable and reprogrammable**
- **Programming and operation 100% testable**

Product Characteristics

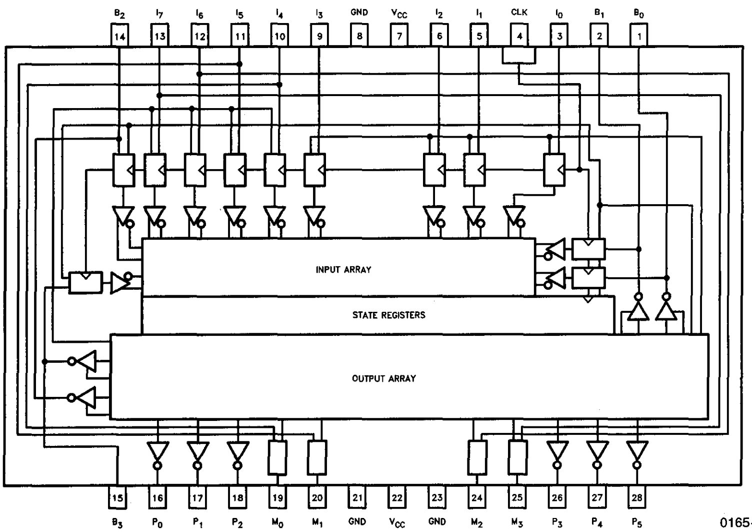
The CY7C361 is a CMOS erasable, programmable logic device (EPLD) with very high speed sequencing and arbitration capabilities.

Applications include: cache and I/O subsystem control for high speed microprocessor based systems, control of high speed numeric processors, and control of asynchronous systems including dataflow organizations.

An onboard clock doubler and conditioning circuit allows the device to operate at 125 MHz based on a 62.5 MHz input reference. The same circuit guards against asymmetric clock waveforms and thus allows for the use of a clock with an imperfect duty cycle. The CY7C361 has two arrays which serve in function similar to the arrays in a PLA except that the registers are placed between the two arrays and the long feedback path of the PLA is eliminated.

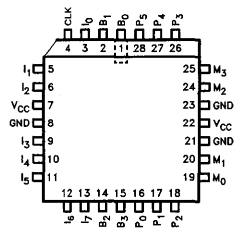
4

Block Diagram



0165-1

LCC, PLCC and HLCC Pinout



0165-21

Selection Guide

Generic Part Number	ICC mA at fMAX				fMAX MHz		tIS ns		tCO ns	
	Com	Com "L"	Mil	Mil "L"	Com	Mil	Com	Mil	Com	Mil
CY7C361-125	200	150			125.0		2		15	
CY7C361-100	200	150	200	150	100.0	100.0	3	3	19	19
CY7C361-83		150		150	83.3	83.3	5	5	23	23
CY7C361-66		150		150	66.6	66.6	5	5	25	25

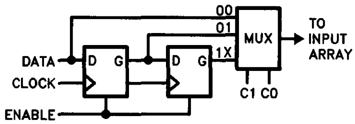
Product Characteristics (Continued)

In the CY7C361, the state information is contained in 32 macrocells sandwiched between the input and output arrays. The current state information is fed back in time to keep up with the 125 MHz operating frequency.

The output array performs an OR function over the state macrocell outputs. The signals from the output array are connected to 14 outputs; in addition they are connected to 3 groups of input macrocells to act as clock enables.

Input Macrocells

The CY7C361 has 12 input macrocells. Each macrocell can be configured to have 0, 1 or 2 registers in the path of the input data. In the configuration where there is no input register, the setup time requirement is largest. In the single register configuration, the setup time is less than half. The double register configuration is used for asynchronous inputs.



0165-3

Figure 1. Input Macrocell

Input Register Enables

The input macrocells are divided into 3 groups, each of which has a register clock enable signal coming from the output array. The purpose of the enable signal is to allow the inputs to be sampled at times controlled by the state of the device.

There is one enable signal per group of input macrocells. The assignment of enable signal node numbers to input macrocell groups is as follows:

Input Nodes	Enable Node
3, 5, 6, 9	29
10,11,12,13	30
1, 2, 14, 15	31

When the enable node is true, data is clocked into the registers of the input macrocells on the rising edge of the internal global clock.

Metastable Immunity

A high level of metastable immunity is afforded in the double register configuration. The CY7C361 input registers are of fast CMOS and resolve inputs in a minimal amount of time. With all inputs switching at the maximum frequency, one metastable event capable of violating the setup time window of the second input register occurs every 10 years. The probability of failure for the configured state machine is much lower than this calculation suggests, because there are more registers in the device and thus more decision time is allowed. No state machine failures due to metastable phenomena will be observed if the maximum frequency and double register operating mode are used.

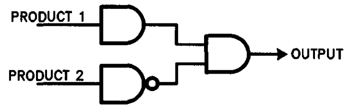
The CY7C361 is thus a superior device for constructing state machines requiring arbitration.

Input Array

The input array has 41 condition decoders: one global reset decoder, 8 local reset decoders, and 32 macrocell decoders. The array has 44 true/complement inputs or 88 inputs in total; for speed reasons, the feedback signals are folded.

Folding or partitioning of the feedback part of the array reduces the number of inputs per decoder to 56. Because of the way the feedback signals are used, this array reduction has minimal impact on utility.

The CY7C361 condition decoder is shown in *Figure 2.* In a conventional PLA or PAL device, only PRODUCT 1 would be present in the first array and the output and feedback would be encoded by a second programmable or fixed OR array. The speed of state machines made from these conventional devices is limited mainly by the feedback path.

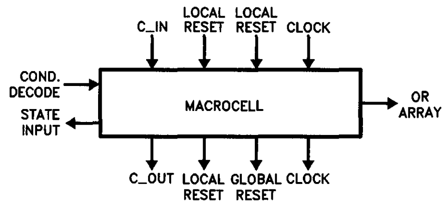


0165-4

Figure 2. Condition Decoder

The condition decoder of the CY7C361 forms a product of a product and a sum over the input field. Since there is immediate feedback information in the input field, multiway fork and join operations can be performed using this type of condition decoder. State transitions can be made in half the time because there is no "state encoding" delay.

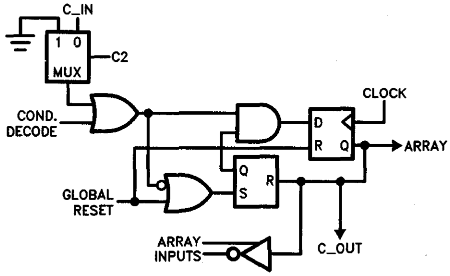
State Machine Macrocells



0165-5

Figure 3. CY7C361 Macrocell

The CY7C361 has 32 state macrocells. The state macrocells each have a single condition decode and share a common clock and global reset condition. For each 4 macrocell group there is a local reset condition.



C1,C0 = 0,1: START

0165-6

Figure 4. Start Configuration

Product Characteristics (Continued)

There are 3 macrocell configurations, named START, TERMINATE and TOGGLE. The purpose of the START configuration is to create a "token" based on a condition decode. The purpose of the TERMINATE configuration is to capture a token and maintain it until a particular condition is decoded, then terminate the token. The TOGGLE configuration is used to make counters.

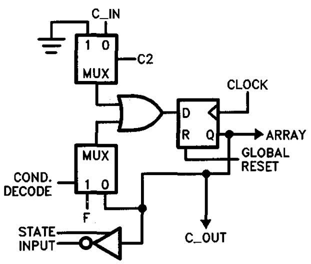
The start configuration creates a token at the leading edge of the condition decode or C__IN. The token is represented by a true output on the macrocell register going to the output array and back as feedback to the input array. The CY7C361 consists of multiple machines or processes running concurrently, each with zero, one or more tokens active at a given time. As the output field is independent, the programmed pattern in the two arrays is one to one translatable to microcode. The microcode is concurrent in operation.

In addition to the main register going to the array, there is an R-S latch in the feedback path. The purpose of the R-S latch is to convert the input condition to a pulse.

In operation, the start macrocell starts from a reset condition (array input = FALSE). When a condition decode "fires" or a token carries in (C__IN), the register output (Q going to array) goes true for exactly one cycle. The OR of the condition decode and the C__IN signal must go FALSE before the start configuration can "fire" again.

Configuration bit C2 is used in all state macrocells to select C__IN to be active (C2 = 0) or inactive (C2 = 1).

For the topmost macrocell (N32), the C2 bit is used to specify a reset option. If the bit is '0', then for the cycle immediately following a reset, the C__IN for this macrocell will be true. At all other times, or if the C2 bit is '1', the C__IN signal will remain false. Note that this option facilitates efficient startup of state machines.



C0,C1 = 1,0: TERMINATE

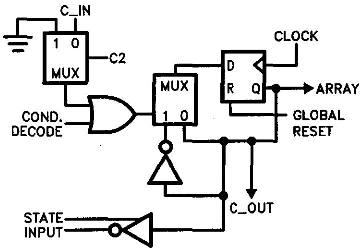
0165-7

Figure 5. Terminate Configuration

Figure 5 shows the terminate configuration which is used to maintain state tokens until a condition occurs.

In operation, the terminate configuration "captures" a token via C—IN and the OR gate. The condition decode is normally false or 0 so the token circulates and the register stays set. When the condition decode "fires", the register resets.

The third configuration, TOGGLE, is for counting and signalling. If the condition decode or the C__IN signal is true, then the register will toggle. The TOGGLE configuration is intended to make counters and state machines with simple control requirements.



C0,C1 = 11: TOGGLE

0165-8

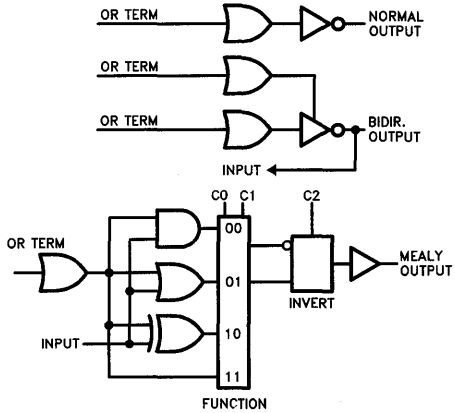
Figure 6. Toggle Configuration

There is one local reset signal for each group of 4 macrocells. The local reset condition decoders will only work with TOGGLE configurations.

The Output Section

There are 3 types of outputs: normal, bidirectional and Mealy. All 3 types can function as normal outputs, but two types—the bidirectional type and the Mealy type—can be used for other purposes. The bidirectional type can be used as an input and the Mealy type can be used as a fast combinational output.

The different types of output structures are shown in *Figure 7.* Note that the only output type that has configuration information to be programmed is the Mealy type.



0165-9

Figure 7. Output Types

A normal output signal from the device is a boolean sum of a subset of the macrocell outputs. The subset selection is programmed into the output array. The number of state machines in the device, and the output mappings of each are determined by the user. The architecture is thus "horizontally divisible" and offers advantages in coding efficiency and event response time over the non-divisible architectures found in most PLA and sequencer types.

A normal output pin is low asserted. The output gate performs an OR function over the flip-flop outputs of the state macrocells. The OR function includes only the outputs which are programmably connected to the OR line in the output array. When none of the connected state macrocell flip-flops are in the true or set condition, the output is high.

4

Product Characteristics (Continued)

If any connected macrocell flip-flop is asserted (or true) then the OR gate function is true and the output pin is low.

Forcing a false condition is easily accomplished by not connecting any state macrocells to the OR line. To force a true condition, line 33 (labelled V_{CC}) is included in the output array. Any OR line connected to line 33 will be permanently true which will cause a normal output to be low.

The bidirectional outputs are I/O pins which may be used as either inputs or outputs. Under state machine control, these pins may be tristated and used as inputs or outputs depending on how the OE term is programmed.

Each bidirectional output has an OE or output enable control and an associated input path to the first array. The OE control is an OR term from the output array which enables the output when the OR function is true. Thus, an OE which has its OR term connected to line 33 will turn the output on permanently.

The Mealy outputs are designed to implement the fastest possible path between an input to the device and an output. Functions are available which combine the OR term and an input signal. These functions, XOR, AND, and OR, with true or negated assertion levels, are useful for data strobes and semaphore operations where signalling occurs depending on the state, but independent of a signal transition.

The AND and OR functions can be used to gate data strobe signals by the state. The XOR function can be used to implement 2 cycle signalling, which is used in self-timed systems to minimize signalling delays. If these functions are not needed, then the Mealy outputs can be configured as normal outputs.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (DIP Pins 7 or 22 to Pins 8, 21 or 23) ... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Voltage Applied to Outputs During Programming ....0.0V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

DC Programming Voltage 13.0V

Output Current into Outputs (Low) ....8 mA

UV Exposure ....7258 Wsec/cm²

Static Discharge Voltage .... >2001V (per MIL-STD-883, Method 3015.2)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +75°C	5V ±10%
Military	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -4.0$ mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 8.0$ mA		0.4	V
V_{IH}	Input HIGH Level	Guaranteed HIGH Input, All Inputs[1]		2.2		V
V_{IL}	Input LOW Level	Guaranteed LOW Input, All Inputs[1]			0.8	V
I_{IX}	Input Leakage Current	$V_{SS} < V_{IN} < V_{CC}$, V_{CC} = Max.		−10	10	μA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} < V_{OUT} < V_{CC}$		−40	40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[2]		−30	−110	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open, Operating at f = f_{MAX}	Commercial "L"		150	mA
			Military "L"			
			Commercial		200	mA
			Military			

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

AC Test Loads and Waveforms

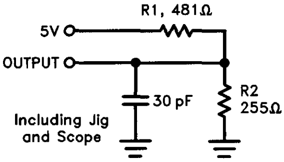


Figure 8a

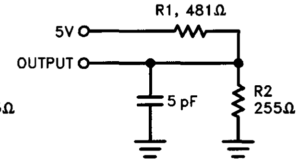
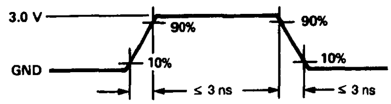


Figure 8b

0165–13

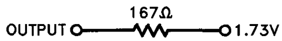
Input Pulses



0165–14

Figure 9

Equivalent to: THÉVENIN EQUIVALENT



0165–15

Switching Characteristics[7]

Parameters	Description	Commercial								Military						Units
		-125		-100		-83		-66		-100		-83		-66		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD1}[13]	Input to Mealy Output Delay	2	9	2	11	2	12	2	15	2	11	2	13	2	15	ns
t_{PD2}[14]	Input to Mealy Output Delay	2	8	2	10	2	11	2	14	2	10	2	12	2	14	ns
t_{CO1}[3, 13]	Clock to Output Delay	5	15	5	19	5	23	5	25	5	19	5	23	5	25	ns
t_{CO2}[3, 14]	Clock to Output Delay	5	14	5	18	5	22	5	24	5	18	5	22	5	24	ns
t_{CM1}[3, 13]	Clock to Mealy Output Delay	5	17	5	20	5	25	5	28	5	21	5	25	5	28	ns
t_{CM2}[3, 14]	Clock to Mealy Output Delay	5	16	5	19	5	24	5	27	5	20	5	24	5	27	ns
t_{IS}[3]	Input Register Input Set Up Time	2		3		5		5		3		5		5		ns
t_{IH}[3]	Input Register Input Hold Time	3		4		5		5		4		5		5		ns
t_S[3, 4]	State Register Input Set Up Time	7		9		12		14		9		12		14		ns
t_H[3, 4]	State Register Input Hold Time	0		0		0		0		0		0		0		ns
t_{WH}[6]	Input Clock Pulse Width HIGH	6		7		9		11		7		9		11		ns
t_{WL}[6]	Input Clock Pulse Width LOW	6		7		9		11		7		9		11		ns
t_{SO1}[3, 11]	Output Skew		4		5		6		6		5		6		6	ns
t_{SO2}[3, 12]	Output Skew		3		4		5		5		4		5		5	ns
t_{SM1}[3, 15]	Mealy Output Skew		4		5		6		6		5		6		6	ns
t_{SM2}[3, 16]	Mealy Output Skew		3		4		5		5		4		5		5	ns
f_{MAX}[5]	Output Maximum Frequency	125.0		100.0		83.3		66.6		100.0		83.3		66.6		MHz
t_{CER}[3, 7]	Clock to Output Disable Delay		16		20		22		25		20		22		25	ns
t_{CEA}[3, 8, 9]	Clock to Output Enable Delay		16		20		22		25		20		22		25	ns

4

Notes:

3. Minimum clock pulse width 8 ns Commercial, 10 ns Military for measurement. Periodically sampled.
4. Input register bypassed.
5. Input clock frequency is ½ f_{MAX} when clock doubler is used.
6. The clock input is tested to accommodate a 60/40 duty cycle waveform at the maximum frequency.
7. Output reference point on AC measurements is 1.5V, except as noted in *Figure 12*:

   $t_{CER(-)}$ negative going is measured at V_{OH} −0.5V.

   $t_{CER(+)}$ positive going is measured at V_{OL} + 0.5V.
8. R1 is disconnected for $t_{CEA(+)}$ positive going (open circuited). (See *Figures 8a* and *8b*).
9. R2 is disconnected for $t_{CEA(-)}$ negative going (open circuited). (See *Figures 8a* and *8b*).
10. *Figure 8a* test load is used for all parameters except t_{CEA} and t_{CER}. *Figure 8b* test load is used for t_{CEA} and t_{CER}.
11. This parameter specifies the maximum allowable t_{CO} clock to output delay difference, or skew, between any two outputs triggered by the same clock edge with all other device outputs changing state within the same clock cycle.
12. This parameter specifies the maximum allowable t_{CO} clock to output delay difference, or skew, between any two outputs triggered by the same clock edge with only the two device outputs changing state within the same clock cycle.
13. This specification is guaranteed for the worst case programmed pattern for which all device outputs are changing state on a given access or clock cycle.
14. This specification is guaranteed for two or fewer outputs changing state in a given access or clock cycle.
15. This parameter specifies the maximum allowable t_{PD} difference between any two mealy outputs triggered by the same or simultaneous input signals with all other device outputs changing state within the same access or clock cycle.
16. This parameter specifies the maximum allowable t_{PD} difference between any two mealy outputs triggered by the same or simultaneous input signals with only the two device outputs changing state within the given access cycle.

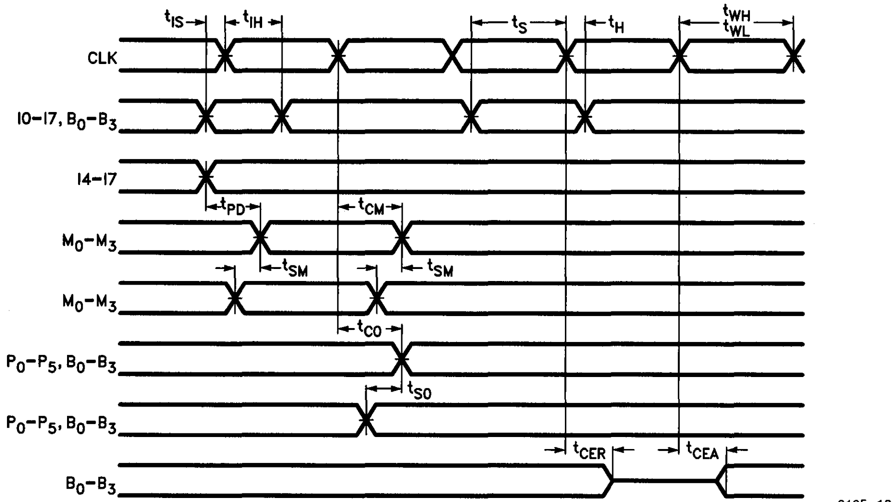
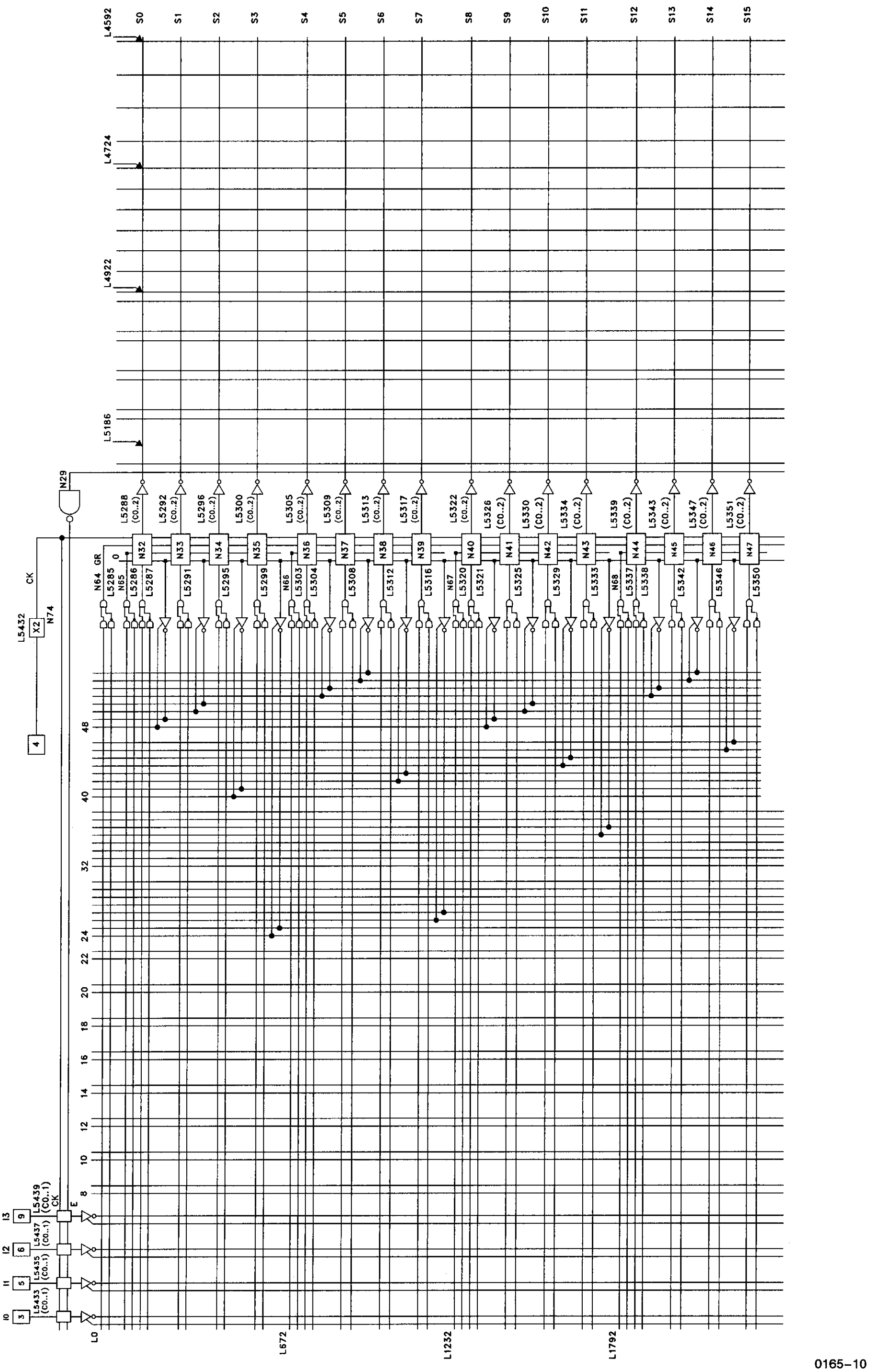
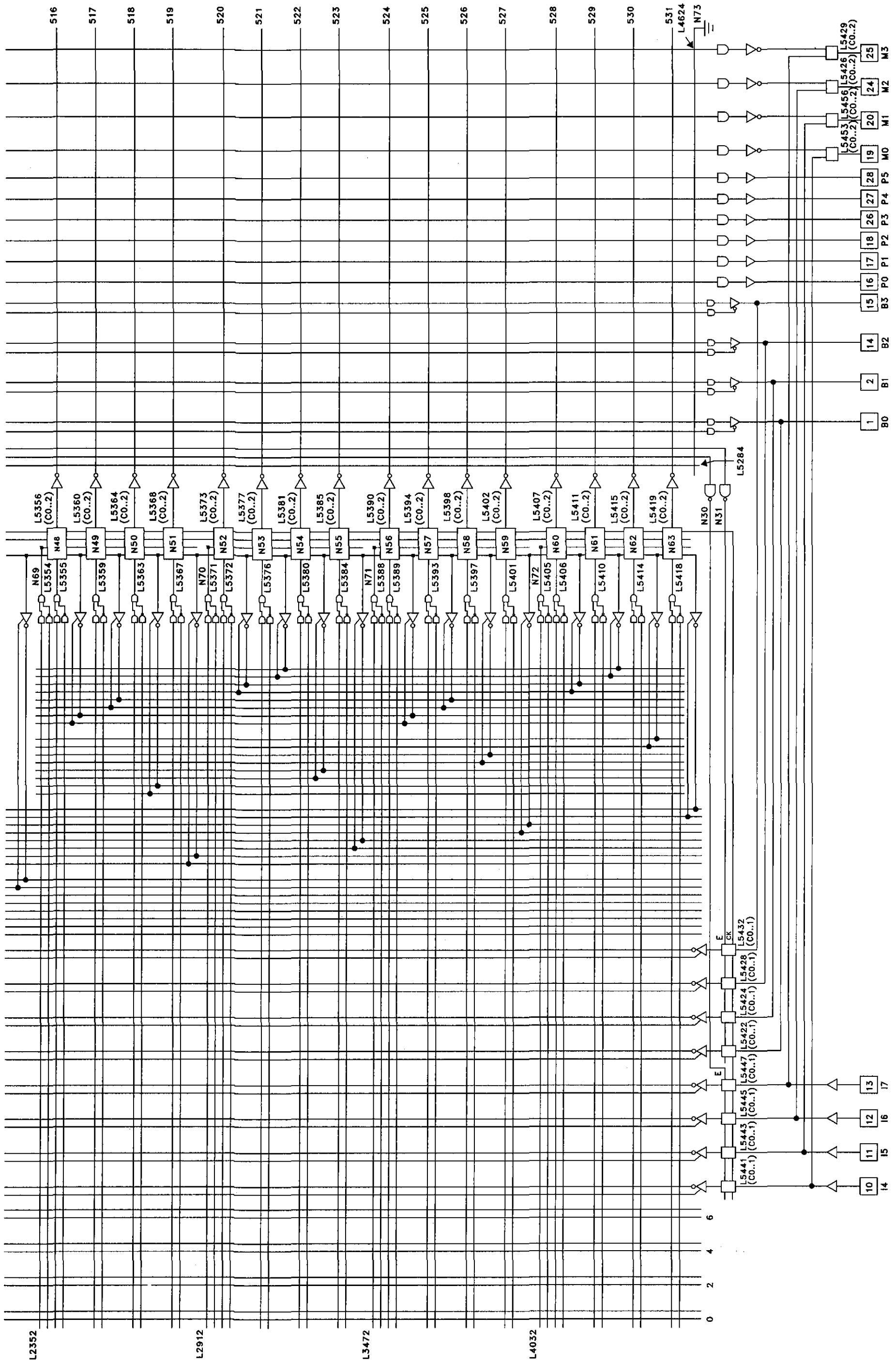


Figure 10. AC Timing Waveforms



0165–10

Figure 11a. CY7C361 Block Diagram (Upper Half)



0165-11

Figure 11b. CY7C361 Block Diagram (Lower Half)

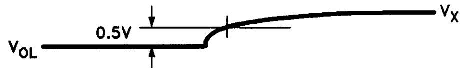
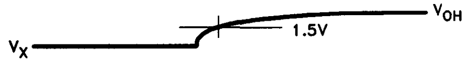
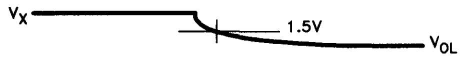
Parameters	V_x	Output Waveform—Measurement Level
$t_{CER}(-)$	0.0V	 0165-22
$t_{CER}(+)$	2.6V	 0165-23
$t_{CEA}(+)$	0.0V	 0165-24
$t_{CEA}(-)$	2.6V	 0165-25

Figure 12. Test Waveforms

4

Ordering Information

I_{CC} mA	f_{MAX} MHz	Ordering Code	Package Type	Operating Range
200	125.0	CY7C361-125PC	P21	Commercial
		CY7C361-125WC	W22	
		CY7C361-125JC	J64	
		CY7C361-125HC	H64	
150	125.0	CY7C361L-125PC	P21	Commercial
		CY7C361L-125WC	W22	
		CY7C361L-125JC	J64	
		CY7C361L-125HC	H64	
200	100.0	CY7C361-100PC	P21	Commercial
		CY7C361-100WC	W22	
		CY7C361-100JC	J64	
		CY7C361-100HC	H64	
150	100.0	CY7C361L-100PC	P21	Commercial
		CY7C361L-100WC	W22	
		CY7C361L-100JC	J64	
		CY7C361L-100HC	H64	
200	100.0	CY7C361-100WMB	W22	Military
		CY7C361-100DMB	D22	
		CY7C361-100QMB	Q64	
		CY7C361-100LMB	L64	
		CY7C361-100HMB	H64	
150	100.0	CY7C361L-100WMB	W22	Military
		CY7C361L-100DMB	D22	
		CY7C361L-100QMB	Q64	
		CY7C361L-100LMB	L64	
		CY7C361L-100HMB	H64	
150	83.3	CY7C361L-83PC	P21	Commercial
		CY7C361L-83WC	W22	
		CY7C361L-83JC	J64	
		CY7C361L-83HC	H64	
150	83.3	CY7C361L-83WMB	W22	Military
		CY7C361L-83DMB	D22	
		CY7C361L-83QMB	Q64	
		CY7C361L-83LMB	L64	
		CY7C361L-83HMB	H64	
150	66.6	CY7C361L-66PC	P21	Commercial
		CY7C361L-66WC	W22	
		CY7C361L-66JC	J64	
		CY7C361L-66HC	H64	
150	66.6	CY7C361L-66WMB	W22	Military
		CY7C361L-66DMB	D22	
		CY7C361L-66QMB	Q64	
		CY7C361L-66LMB	L64	
		CY7C361L-6HMB	H64	

Document #: 38-00106-A

PLD Programming Information

Introduction

PLDs or Programmable Logic Devices provide an attractive alternative to logic implemented with discrete devices. Because the primary requirements for this logic has been to provide high performance and increased functional density, in the past all programmable logic functions have been implemented in a bipolar technology. Bipolar technology uses a fuse for the programming mechanism. The fuses are intact when the product is delivered to the user, and may be programmed once, then read and used indefinitely. The fuses are literally blown using a high current supplied by a programming system. Programming or blowing a fuse is a one time event; once blown, the fuse is forever open. Therefore, a fuse cannot be tested to see that it will blow or program properly before it is delivered to the user. This difficulty in testing fuses for programming results in less than 100% programming yield in the field. The failures can be placed into three categories.

A certain percentage of the product simply fails to program. These devices are easily identified, and may be returned for replacement. A small percentage of the product will program and verify correctly, but fail to function properly as a logic element. This can happen because, without programming each location, the connection between the programmed cell and the logic it is to control cannot be verified. Some programmers can test for this condition through the use of a set of test vectors for each unique code or part. Additional material will be lost, however, even if a structured set of test vectors is used due to the device functioning too slowly. This failure is much more subtle and can only be found by 100% AC testing of the programmed device, or worse yet by troubleshooting an assembled board or system.

Cypress PLDs use an EPROM programming mechanism. This technology has been available since the early 1970's, however, as with most MOS technologies, the emphasis has been on density, not performance. CMOS at Cypress is as fast as or faster than Bipolar and, coupled with EPROM programming, offers a viable alternative to bipolar programmable logic from a performance point of view. In addition, CMOS EPROM technology offers other overwhelming advantages. EPROM cells are programmed by injecting charge on an electrically isolated gate which causes the transistor to be permanently turned off. This mechanism may be reversed by irradiating the cell with ultraviolet light. This feature totally changes the testing philosophy and provides a new feature for the user. All programmable cells may now be tested by the manufacturer prior to delivery to the customer. This provides an easy methodology to certify programming, functionality, and performance. With built in test arrays, functionality and performance may be tested even if the device is packaged in a non-windowed package. Devices packaged in a windowed package may be programmed and erased indefinitely, providing the designer a tool for the development of his logic without throwing away devices that are programmed incorrectly as the design proceeds.

Programmable Technology

EPROM Process Technology

EPROM technology employs a floating or isolated gate between the normal control gate and the source/drain region of a transistor. This gate may be charged with electrons during the programming operation, permanently turning off the transistor. The state of the floating gate, charged or uncharged, is permanent because the gate is isolated in an extremely pure oxide. The charge may be removed if the device is irradiated with ultraviolet energy in the form of light. This ultraviolet light allows the electrons on the gate to recombine and discharge the gate. This process is repeatable and therefore can be used during the processing of the device, repeatedly if necessary, to assure programming function and performance.

Two Transistor Cells

In order to provide an EPROM cell that is as fast as the fuse technology employed in bipolar processes, Cypress uses a two transistor EPROM cell. One transistor is optimized for reliable programming, and one transistor is optimized for high speed. The floating gates are connected such that charge injected on the floating gate of the programming transistor is conducted to the read transistor biasing it off.

Programming Algorithm

Byte Addressing and Programming

All Cypress Programmable Logic Devices are addressed and programmed on BYTE or EXTENDED BYTE basis where an EXTENDED BYTE is a field that is as wide as the output path of the device. Each device or family of devices has a unique address map which is available in the product data sheet. Each BYTE or EXTENDED BYTE is written into the addressed location from the pins that serve as the output pins in normal operation. To program a cell, a "1" or HIGH is placed on the input pin and a "0" or LOW is placed on pins corresponding to cells that are not to be programmed. Data is also read from these pins in parallel for verification after programming. A "1" or HIGH during program verify operation indicates an unprogrammed cell, while a "0" or LOW indicates that the cell accessed has been programmed.

Blank Check

Before programming, all Programmable Logic Devices may be checked in a conventional manner to determine that they have not been previously programmed. This is accomplished in a program verify mode of operation by reading the contents of the array. During this operation, a "1" or HIGH output indicates that the addressed cell is unprogrammed, while a "0" or LOW indicates a programmed cell.

Programming The Data Array

Programming is accomplished by applying a supervoltage to one pin of the device causing it to enter the programming mode of operation. This also provides the programming voltage for the cells to be programmed. In this mode of operation, the address lines of the device are used to address each location to be programmed, and the data is presented on the pins normally used for reading the contents of the device. Each device has a READ/WRITE pin in the programming mode. This signal causes a write operation when switched to a supervoltage, and a read operation when switched to a logic "0" or LOW. In the logic HIGH state "1" the device is in a program inhibit condition and the output pins are in a high impedance state. During a WRITE operation, the data on the output pins is written into the addressed array location. In a READ operation the contents of the addressed location are present on the output pins and may be verified. Programming therefore is accomplished by placing data on the output pins, and writing it into the addressed location. Verification of data is accomplished by examining the information on the output pins during a READ operation.

The timing for actual programming is supplied in the unique programming specification for each device.

Phantom Operating Modes

All Cypress Programmable Logic Devices contain a PHANTOM ARRAY for post assembly testing. This array is accessed, programmed and operated in a special PHANTOM mode of operation. In this mode, the normal array is disconnected from control of the logic, and in its place the PHANTOM ARRAY is connected. In normal operation the PHANTOM ARRAY is disconnected and control is only via the normal array. This special feature allows every device to be tested for both functionality and performance after packaging and, if desired, by the user before programming and use. The PHANTOM modes are entered through the use of supervoltages and are unique for each device or family of devices. See specific data sheets for details.

Special Features

Cypress Programmable Logic devices, depending on the device, have several special features. For example the security mechanism defeats the verify operation and therefore secures the contents of the device against unauthorized tampering or access. In advanced devices such as the PAL C 22V10, PLD C 20G10, and the CY7C330 the MACROCELLs are programmable through the use of the architecture bits. This allows the user to more effectively tailor the device architecture to his unique system requirements. These features are also programmed through the use of EPROM cells. Specific programming is detailed in the device data sheet.

Programming Support

Programming support for Cypress CMOS Programmable Logic Devices is available from a number of programmer manufacturers, some of which are listed as follows. The hardware module version number listed is the earliest version qualified by Cypress. Any subsequent version is also qualified unless otherwise specifically noted.

Data I/O Corporation
10525 Willows Rd. N.E.
P.O. Box 97046
Redmond, WA
98073-9746
(206) 881-6444

Data I/O 29B LOGICPAK VO4				Adapters: PT	Adapters: Generic
Cypress Part Number	Generic Part Number	Family Code and Pinout		303A-009 Revision	303A-011A/B Revision
PALC16R8	16R8	28	24	V03	V01
PALC16R6	16R6	28	24	V03	V01
PALC16R4	16R4	28	24	V03	V01
PALC16L8	16L8	28	17	V03	V01
PALC22V10	22V10	28	28	V04	V01
PLDC20G10	20G10	28	56	V04	V01
PLDC20G10	20R4	28	65	V04	V02
PLDC20G10	20R6	28	66	V04	V02
PLDC20G10	20R8	28	27	V04	V02
PLDC20G10	20L8	28	26	V04	V01
PLDC20G10	20L10	28	6	V04	V01
PLDC20G10	20L2	28	5	V04	V02
PLDC20G10	18L4	28	4	V04	V01
PLDC20G10	16L6	28	3	V04	V01
PLDC20G10	14L8	28	2	V04	V01
PLDC20G10	12L10	28	1	V04	V01
CY7C330	7C330	28	1A	V06	V01

Data I/O Model 60A, 60H				
Cypress Part Number	Generic Part Number	Family Code and Pinout		Revision
PALC16R8	16R8	28	24	V05
PALC16R6	16R6	28	24	V05
PALC16R4	16R4	28	24	V05
PALC16L8	16L8	28	17	V05
PALC22V10	22V10	28	28	V08
PLDC20G10	20G10	28	56	V08

Data I/O Unisite			
Cypress Part Number	Generic Part Number	Family Code and Pinout	Revision
PALC16R8	16R8	Menu Driven	2.0
PALC16R6	16R6		2.0
PALC16R4	16R4		2.0
PALC16L8	16L8		2.0
PALC22V10	22V10		2.0
PLDC20G10	20G10		2.0
CY7C331	7C331		2.71
CY10E301	16P8		2.5
CY100E301	16P8		2.5
CY10E302	16P4		2.5
CY100E302	16P4		2.5

Stag Microsystems
1600 Wyatt Dr.
Santa Clara, CA 95054
(408) 988-1118
STAG ZL32 Rev. 30A03

STAG PPZ Zm2200 Rev. 18 ZL32 Rev. 30A03		
Cypress Part Number	**Generic Part Number**	**Family Code and Pinout**
PALC16R8	16R8	Menu Driven
PALC16R6	16R6	
PALC16R4	16R4	
PALC16L8	16L8	
PALC22V10	22V10	

Cypress Semiconductor Inc.
3901 North First Street
San Jose, CA 95134
(408) 943-2600

Cypress CY3000 QuickPro Rev. PLD 2.8		
Cypress Part Number	**Generic Part Number**	**Family Code and Pinout**
PALC16R8	16R8	Menu Driven
PALC16R6	16R6	
PALC16R4	16R4	
PALC16L8	16L8	
PALC22V10	22V10	
PALC22V10B	22V10	
PLDC20G10(B)	20G10	
PLDC20G10(B)	20R4	
PLDC20G10(B)	20R6	
PLDC20G10(B)	20R8	
PLDC20G10(B)	20L8	
PLDC20G10(B)	20L10	
PLDC20G10(B)	20L2	
PLDC20G10(B)	18L4	
PLDC20G10(B)	16L6	
PLDC20G10(B)	14L8	
PLDC20G10(B)	12L10	
PLDC20RA10	20RA10	
CY7C330	7C330	
CY7C331	7C331	
CY7C332	7C332	
CY10E301	16P8	
CY100E301	16P8	
CY10E302	16P4	
CY100E302	16P4	

Digelec Corporation
1602 Lawrence Ave.
Suite 113
Ocean, NJ 07712
(201) 493-2420

DIGELEC 803 FAM-52 Rev. A-6.0			
Cypress Part Number	**Generic Part Number**	**Family Code and Pinout**	**Adapter Rev. A-3**
PALC16R8	16R8	Menu Driven	DA-53
PALC16R6	16R6		DA-53
PALC16R4	16R4		DA-53
PALC16L8	16L8		DA-53
PALC22V10	22V10		DA-53

Adams MacDonald Enterprises
800 Airport Rd.
Monterey, CA 93940
(408) 373-3607

SMS Sprint Rev. 3.2i		
Cypress Part Number	**Generic Part Number**	**Family Code and Pinout**
PALC16R8	16R8	Menu Driven
PALC16R6	16R6	
PALC16R4	16R4	
PALC16L8	16L8	
PALC22V10	22V10	
PALC22V10B	22V10	
PLDC20G10(B)	20G10	
PLDC20G10(B)	20R4	
PLDC20G10(B)	20R6	
PLDC20G10(B)	20R8	
PLDC20G10(B)	20L8	
PLDC20G10(B)	20L10	
PLDC20G10(B)	20L2	
PLDC20G10(B)	18L4	
PLDC20G10(B)	16L6	
PLDC20G10(B)	14L8	
PLDC20G10(B)	12L10	
PLDC20RA10	20RA10	
CY7C330	7C330	
CY7C331	7C331	
CY7C332	7C332	

Logical Devices Inc.
1321 N.W. 65th Place
Ft. Lauderdale, FL 33309
(305) 974-0975

Logical Devices ALLPRO Rev. V1.4		
Cypress Part Number	**Generic Part Number**	**Family Code and Pinout**
PALC16R8	16R8	Menu Driven
PALC16R6	16R6	
PALC16R4	16R4	
PALC16L8	16L8	
PALC22V10	22V10	

Kontron Electronics
1230 Charleston Road
Mountain View, CA
94039-7230
(415) 965-7020

Kontron EPP 80 UPM-P		
Cypress Part Number	**Generic Part Number**	**Family Code and Pinout**
PALC16R8	16R8	Menu Driven
PALC16R6	16R6	
PALC16R4	16R4	
PALC16L8	16L8	
PALC22V10	22V10	

Third Party Development Software	Supported Devices:
ABEL™ Data I/O Corporation 10525 Willows Rd. N.E. P.O. Box 97046 Redmond, WA 98073-9746 (206) 881-6444	PALC16R8 PALC16R6 PALC16R4 PALC16L8 PALC22V10 PLDC20G10 CY7C330
CUPL™ Assisted Technology 1290 Parkmoor Ave. San Jose, CA 95126 (800) 523-5207 (800) 628-8748 CA	PALC16R8 PALC16R6 PALC16R4 PALC16L8 PALC22V10 CY7C330
LOG/iC™ ISDATA GmbH Haid-und-Neu-Strasse 7 D-7500 Karlsruhe 1 West Germany (0721) 69 30 92	PALC16R8 PALC16R6 PALC16R4 PALC16L8 PALC22V10 CY7C330 CY7C331

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CUPL™ is a trademark of Assisted Technology.
ISDATA® is a registered trademark of ISDATA GmbH.
LOG/iC™ is a trademark of ISDATA GmbH.

Section Contents

FIFOs

64 x 4 FIFO Serial Memory

Features

- **1.2/2 MHz data rate**
- **Fully TTL compatible**
- **Independent asynchronous inputs and outputs**
- **Direct replacement for PMOS 3341**
- **Expandable in word length and width**
- **CMOS for optimum speed/power**
- **Capable of withstanding greater than 2000V electrostatic discharge**

Functional Description

The 3341 is a 64-word x 4-bit First-In First-Out (FIFO) Serial Memory. The inputs and outputs are completely independent (no common clocks) making the 3341 ideal for asynchronous buffer applications.

Control signals are provided for both vertical and horizontal expansion.

The 3341 is manufactured using Cypress CMOS technology and is available in both ceramic and plastic packages.

Data Input

The four bits of data on the D_0 through D_3 inputs are entered into the first location when both Input Ready (IR) and Shift In (SI) are HIGH. This causes IR to go LOW but data will stay locked in the first bit location until both IR and SI are LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus, data will stack up at the end of the device while empty locations will "bubble" to the front. t_{BT} defines the time required for the first data to travel from the input to the output of a previously empty device, or for the first empty space to travel from the output to the input of a previously full device.

Data Output

When data has been transferred into the last cell, Output Ready (OR) goes HIGH, indicating the presence of valid data at the output pins Q_0 through Q_3. The transfer of data is initiated when both the Output Ready output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

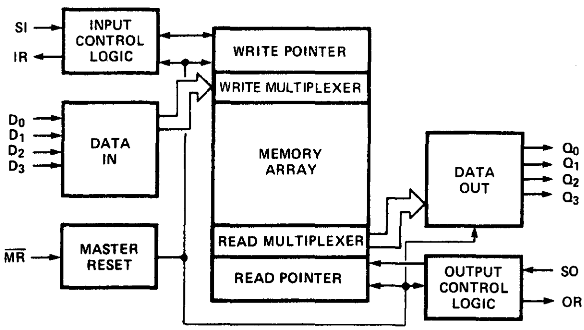
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{BT}) or completely empty (Output Ready stays LOW for at least t_{BT}).

Reset

When Master Reset ($\overline{MR}$) goes LOW, the control logic is cleared, and the data outputs enter a LOW state. When $\overline{MR}$ returns HIGH, Output Ready (OR) stays LOW, and Input Ready (IR) goes HIGH if Shift In (SI) was LOW.

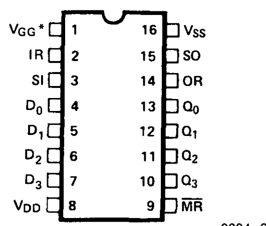
5

Logic Block Diagram



0004-1

Pin Configuration



0004-2

*Internally not connected

Selection Guide

		3341	3341-2
Maximum Operating Frequency		1.2 MHz	2.0 MHz
Maximum Operating Current (mA)	Commercial	45	45
	Military	60	60

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential
(Pin 16 to Pin 8)..................... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883 Method 3015)

Latchup Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}*
Commercial	0°C to +70°C	5V ±10%	GND	NC
Military[3]	−55°C to +125°C	5V ±10%	GND	NC

*Internally Not Connected.

Electrical Characteristics Over the Operating Range[4]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{SS} = Min., I_{OH} = −0.3 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{SS} = Min., I_{OL} = 1.6 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{SS}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	$V_{DD} \leq V_I \leq V_{SS}$		−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{SS} = Max., V_{OUT} = V_{DD}			−90	mA
I_{DD}	Power Supply Current	V_{SS} = Max., I_{OUT} = 0 mA	Commercial		45	mA
			Military		60	
I_{GG}	V_{GG} Current				0	mA

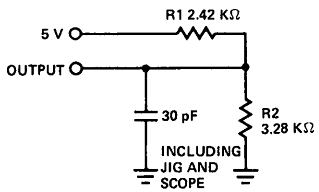
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	7	pF
C_{OUT}	Output Capacitance	V_{SS} = 5.0V	10	

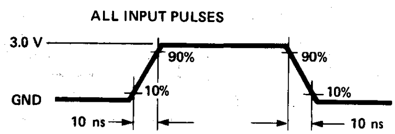
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms



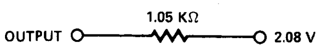
0004-3



0004-5

Equivalent to:

THÉVENIN EQUIVALENT



0004-4

Switching Characteristics Over the Operating Range[4, 5]

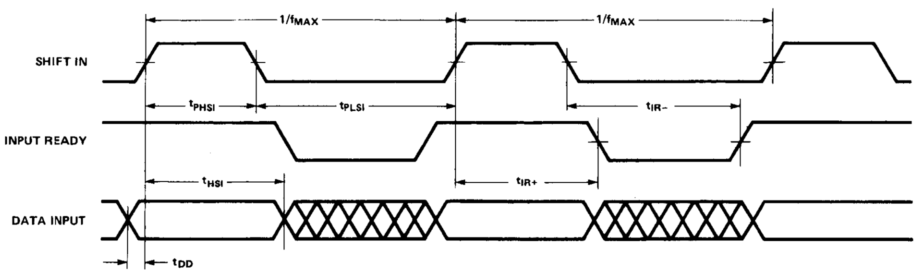
Parameters	Description	Test Conditions	3341		3341-2		Units
			Min.	Max.	Min.	Max.	
f_{MAX}	Operating Frequency	Note 6		1.2		2	MHz
t_{PHSI}	SI HIGH Time		80		80		ns
t_{PLSI}	SI LOW Time		80		80		ns
t_{DD}	Data Setup to SI		0		0		ns
t_{HSI}	Data Hold from SI		200		100		ns
t_{IR+}	Delay, SI HIGH to IR LOW		20	350	20	160	ns
t_{IR-}	Delay, SI LOW to IR HIGH		20	450	20	200	ns
t_{PHSO}	SO HIGH Time		80		80		ns
t_{PLSO}	SO LOW Time		80		80		ns
t_{OR+}	Delay, SO HIGH to OR LOW		20	370	20	160	ns
t_{OR-}	Delay, SO LOW to OR HIGH		20	450	20	200	ns
t_{DA}	Data Setup to OR HIGH		0		0		ns
t_{DH}	Data Hold from OR LOW		75		20		ns
t_{BT}	Bubble through Time			1000		500	ns
t_{MRW}	$\overline{MR}$ Pulse Width		400		200		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		30		30		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			400		200	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			400		200	ns

Notes:

5. Test conditions assume signal transitions of 10 ns or less. Timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
6. $1/f_{MAX} > t_{PHSI} + t_{IR-}$, $1/f_{MAX} > t_{PHSO} + t_{OR-}$.

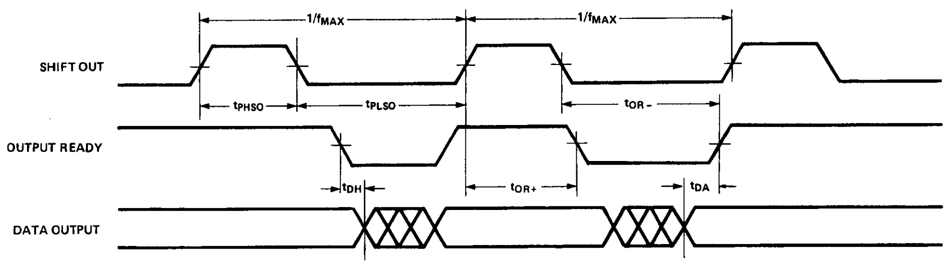
Switching Waveforms

Data In Timing Diagram



0004-6

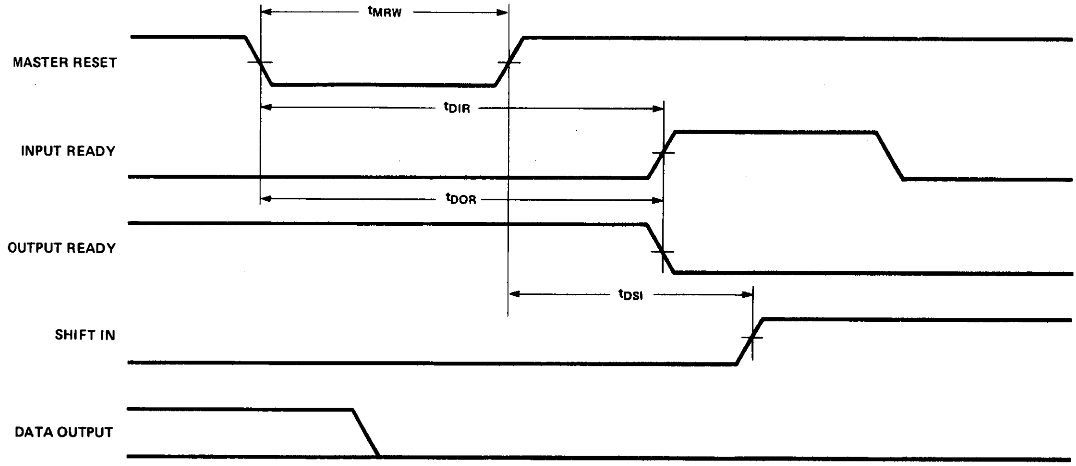
Data Out Timing Diagram



0004-7

Switching Waveforms (Continued)

Master Reset Timing Diagram



0004–8

Ordering Information

Ordering Code (1.2 MHz)	Package Type	Operating Range
CY3341PC CY3341DC	P1 D2	Commercial
CY3341DMB	D2	Military

Ordering Code (2 MHz)	Package Type	Operating Range
CY3341-2PC CY3341-2DC	P1 D2	Commercial
CY3341-2DMB	D2	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{DD}	1,2,3

Switching Characteristics

Parameters	Subgroups
f_{MAX}	7,8,9,10,11
t_{PHSI}	7,8,9,10,11
t_{PLSI}	7,8,9,10,11
t_{DD}	7,8,9,10,11
t_{HSI}	7,8,9,10,11
t_{IR+}	7,8,9,10,11
t_{IR-}	7,8,9,10,11
t_{PHSO}	7,8,9,10,11
t_{PLSO}	7,8,9,10,11
t_{OR+}	7,8,9,10,11
t_{OR-}	7,8,9,10,11
t_{DA}	7,8,9,10,11
t_{DH}	7,8,9,10,11
t_{BT}	7,8,9,10,11
t_{MRW}	7,8,9,10,11
t_{DSI}	7,8,9,10,11
t_{DOR}	7,8,9,10,11
t_{DIR}	7,8,9,10,11

Document #: 38-00011-B

CY7C401/CY7C403
CY7C402/CY7C404

CYPRESS SEMICONDUCTOR

Cascadeable 64 x 4 FIFO and 64 x 5 FIFO

Features

- 64 x 4 (CY7C401 and CY7C403) 64 x 5 (CY7C402 and CY7C404) High speed first-in first-out memory (FIFO)
- Processed with high-speed CMOS for optimum speed/power
- 25 MHz data rates
- 50 ns bubble-through time—25 MHz
- Expandable in word width and/or length
- 5 volt power supply ±10% tolerance both commercial and military
- Independent asynchronous inputs and outputs
- TTL compatible interface
- Output enable function available on CY7C403 and CY7C404
- Capable of withstanding greater than 2001V electrostatic discharge
- Pin compatible with MMI 67401A/67402A

Functional Description

The CY7C401 and CY7C403 are asynchronous first-in first-out memories (FIFOs) organized as 64 four bit words. The CY7C402 and CY7C404 are similar FIFOs organized as 64 five bit words. Both the CY7C403 and CY7C404 have an Output Enable (OE) function.

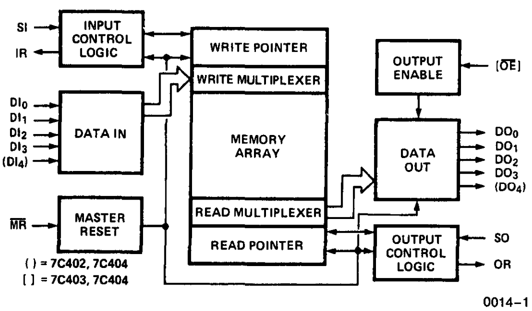
The devices accept 4/5 bit words at the data input (DI_0-DI_n) under the control of the Shift In (SI) input. The stored words stack up at the output (DO_0-DO_n) in the order they were entered. A read command on the Shift Out (SO) input causes the next to last word to move to the output and all data shifts down once in the stack. The Input Ready (IR) signal acts as a flag to indicate when the input is ready to accept new data (HIGH), to indicate when the FIFO is full (LOW), and to provide a signal for cascading. The Output Ready (OR) signal is a flag to indicate the output contains valid data (HIGH), to indicate the FIFO is empty (LOW), and to provide a signal for cascading.

Parallel expansion for wider words is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

Serial expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready (IR) pin of the receiving device is connected to the Shift Out (SO) pin of the sending device, and the Output Ready (OR) pin of the sending device is connected to the Shift In (SI) pin of the receiving device.

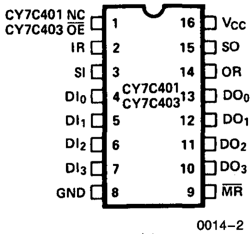
Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The 25 MHz operation makes these FIFOs ideal for high speed communication and controller applications.

Logic Block Diagram

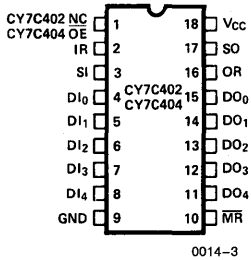


0014-1

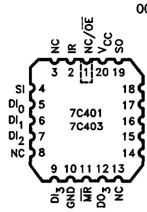
Pin Configurations



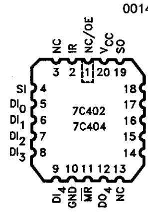
0014-2



0014-3



0014-16



0014-17

Selection Guide

		7C401/2-5	7C40X-10	7C40X-15	7C40X-25
Maximum Shift Rate (MHz)		5	10	15	25
Maximum Operating Current (mA)	Commercial	75	75	75	75
	Military	—	90	90	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V
(per MIL-STD-883 Method 3015)

Latch-up Current......................... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)[4]

Parameters	Description	Test Conditions		7C40X-10, 15, 25		Units
				Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	6.0	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
V_{CD}[1]	Input Diode Clamp Voltage[1]					
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5V Output Disabled (CY7C403 and CY7C404)		−50	+50	μA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND			−90	mA
I_{CC}	Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		75	mA
			Military		90	mA

Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:

1. The CMOS process does not provide a clamp diode. However, the FIFO is insensitive to −3V dc input levels and −5V undershoot pulses of less than 10 ns (measured at 50% point).
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. Tested initially and after any design or process changes that may affect these parameters.

5

AC Test Load and Waveform

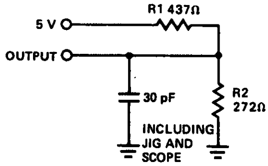


Figure 1a

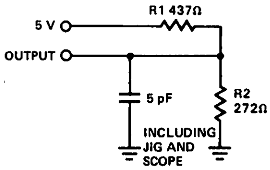
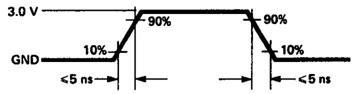


Figure 1b

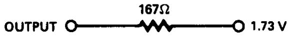
0014-4

ALL INPUT PULSES



0014-5

Equivalent to: THÉVENIN EQUIVALENT



0014-6

Switching Characteristics Over the Operating Range[4, 6]

Parameters	Description	Test Conditions	7C401-5 7C402-5		7C40X-10		7C40X-15		7C40X-25 [12]		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 7		5		10		15		25	MHz
t_{PHSI}	SI HIGH Time		20		20		20		11		ns
t_{PLSI}	SI LOW Time		45		30		25		20		ns
t_{SSI}	Data Setup to SI	Note 8	0		0		0		0		ns
t_{HSI}	Data Hold from SI	Note 8	60		40		30		20		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			75		40		35		21/22	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			75		45		40		28/30	ns
t_{PHSO}	SO HIGH Time		20		20		20		11		ns
t_{PLSO}	SO LOW Time		45		25		25		20		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			75		40		35		19/21	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			80		55		40		34/37	ns
t_{SOR}	Data Setup to OR HIGH		0		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		5		5		5		5		ns
t_{BT}	Bubble through Time			200	10	95	10	65	10	50/60	ns
t_{SIR}	Data Setup to IR	Note 9	5		5		5		5		ns
t_{HIR}	Data Hold from IR	Note 9	30		30		30		20		ns
t_{PIR}	Input Ready Pulse HIGH		20		20		20		15		ns
t_{POR}	Output Ready Pulse HIGH		20		20		20		15		ns
t_{PMR}	MR Pulse Width		40		30		25		25		ns
t_{DSI}	MR HIGH to SI HIGH		40		35		25		10		ns
t_{DOR}	MR LOW to OR LOW			85		40		35		35	ns
t_{DIR}	MR LOW to IR HIGH			85		40		35		35	ns
t_{LZMR}	MR LOW to Output LOW	Note 10		50		40		35		25	ns
t_{OOE}	Output Valid from OE LOW			—		35		30		20	ns
t_{HZOE}	Output HIGH-Z from OE HIGH	Note 11		—		30		25		15	ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1a*.
7. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} + t_{DHOR}$
8. t_{SSI} and t_{HSI} apply when memory is not full.
9. t_{SIR} and t_{HIR} apply when memory is full, SI is high and minimum bubble through (t_{BT}) conditions exist.
10. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.
11. HIGH-Z transitions are referenced to the steady-state V_{OH} −500 mV and V_{OL} +500 mV levels on the output. t_{HZOE} is tested with 5 pF load capacitance as in *Figure 1b*.
12. Commercial/Military

Operational Description

CONCEPT

Unlike traditional FIFOs these devices are designed using a dual port memory, read and write pointer, and control logic. The read and write pointers are incremented by the Shift Out (SO) and Shift In (SI) respectively. The availability of an empty space to shift in data is indicated by the Input Ready (IR) signal, while the presence of data at the output is indicated by the Output Ready (OR) signal. The conventional concept of bubble through is absent. Instead, the delay for input data to appear at the output is the time required to move a pointer and propagate an Output Ready (OR) signal. The $\overline{\text{Output Enable}}$ ($\overline{\text{OE}}$) signal provides the capability to OR tie multiple FIFOs together on a common bus.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset (MR) signal. This causes the FIFO to enter an empty condition signified by the Output Ready (OR) signal being LOW at the same time the Input Ready (IR) signal is HIGH. In this condition, the data outputs DO_0-DO_n) will be in a LOW state.

SHIFTING DATA IN

Data is shifted in on the rising edge of the Shift In (SI) signal. This loads input data into the first word location of the FIFO. On the falling edge of the Shift In (SI) signal, the write pointer is moved to the next word position and the Input Ready (IR) signal goes HIGH indicating the readiness to accept new data. If the FIFO is full, the Input Ready (IR) will remain LOW until a word of data is shifted out.

SHIFTING DATA OUT

Data is shifted out of the FIFO on the falling edge of the Shift Out (SO) signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the Output Ready (OR) signal will go HIGH. If data is not present, the Output Ready (OR) signal will stay LOW indicating the FIFO is empty. Upon the rising edge of Shift Out (SO), the Output Ready (OR) signal goes LOW. The data outputs of the FIFO should be sampled with edge sensitive type D flip-flop (or equivalent), using the SO signal as the clock input to the flip-flop.

BUBBLE THROUGH

Two bubble through conditions exist. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the Output Ready (OR) flag goes HIGH indicating valid data at the output.

The second bubble through condition occurs when the device is full. Shifting data out creates an empty location which propagates to the input. After a delay, the Input Ready (IR) flag goes HIGH. If the Shift In (SI) signal is HIGH at this time, data on the input will be shifted in.

APPLICATION OF THE 7C403-25/7C404-25 AT 25 MHz

Application of the CY7C403 or CY7C404 Cypress CMOS FIFO's requires attention to characteristics not easily specified in a Datasheet, but necessary for reliable operation under all conditions.

When an empty FIFO is filled with initial information, at maximum "shift in" SI frequency, followed by immediate shifting out of the data also at maximum "shift out" SO frequency, the designer must be aware of a window of time which follows the initial rising edge of the "output Ready" OR signal during which the SO signal is not recoginized. This condition exists only at high speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full frequency operation, but rather delays the full 25 MHz operation until after the window has passed.

There are several implementation techniques to manage the window so that all SO signals are recognized:

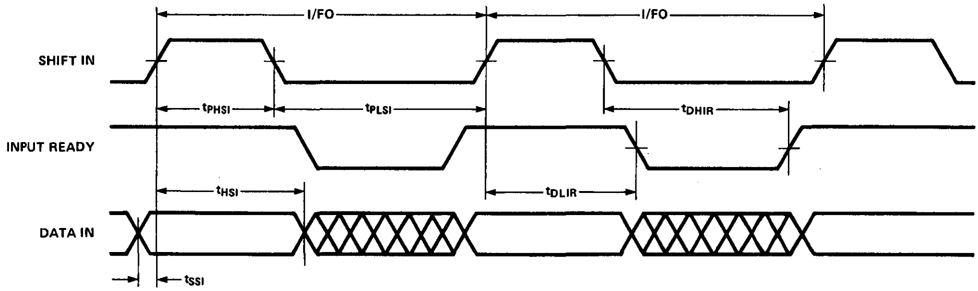
1. The first involves delaying SO operation such that it does not occur in the critical window. This can be accomplished by causing a fixed delay of 40 ns "initiated by the SI signal only when the FIFO is empty" to inhibit or gate the SO activity. This however requires that the SO operation at least temporarily be synchronized with the input SI operation. In synchronous applications this may well be possible and a valid solution.
2. Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is greater than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Cypress FIFOs do not have this limitation, any system designed in this manner will not encounter the window condition described above.
3. The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO 40 ns from the rising edge of the initial OR "output ready" signal. This however involves the requirement that this only occurs on the first occurance of data being loaded into the FIFO from an empty condition and therefore requires the knowledge of "input ready" IR and SI conditions as well as SO.
4. Handshaking with the OR signal can be a third method of avoiding the window in question. With this technique the rising edge of SO, or the fact that the SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken low again, advancing the internal pointer to the next data, until the OR signal goes LOW. This assures that the SO pulse that is initiated in the window will be automatically extended sufficient time to be recognized.
5. There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the SO signal is most appropriate because data is guaranteed to be stable prior to and after the SO leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

Any of the above solutions will provide a solution for correct operation of a Cypress FIFO at 25 MHz. The specific implementation is left to the designer and dependent on the specific application needs.

5

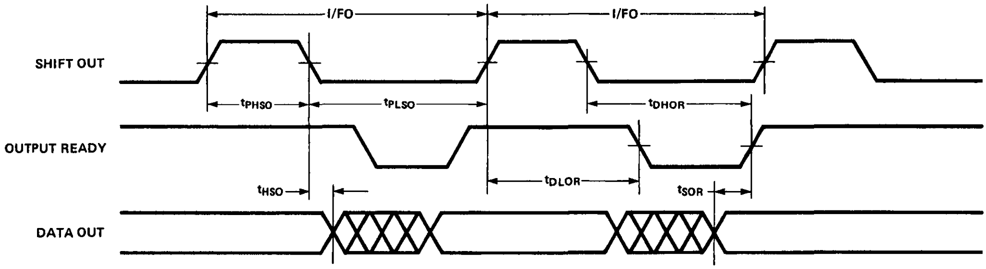
Switching Waveforms

Data In Timing Diagram



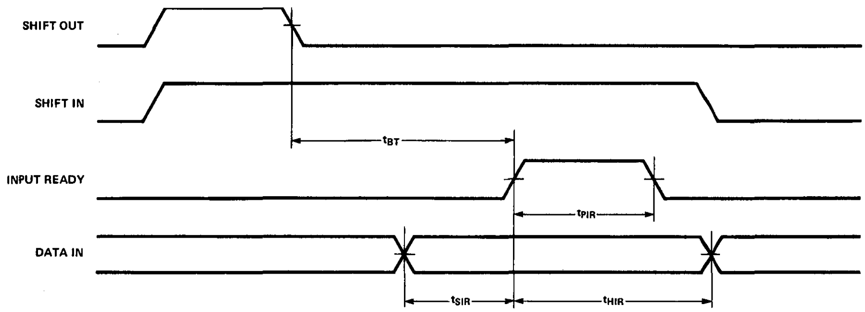
0014–7

Data Out Timing Diagram



0014–8

Bubble Through, Data Out To Data In Diagram

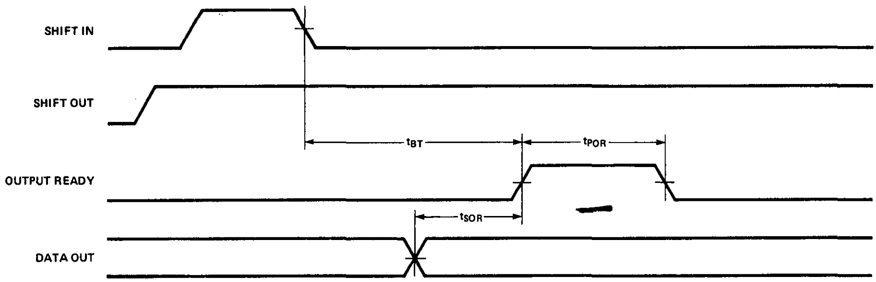


0014–9

Note:
Interfacing to the FIFO—
Please refer to the Interfacing to the FIFO applications brief in the Applications Section at the back of this data book.

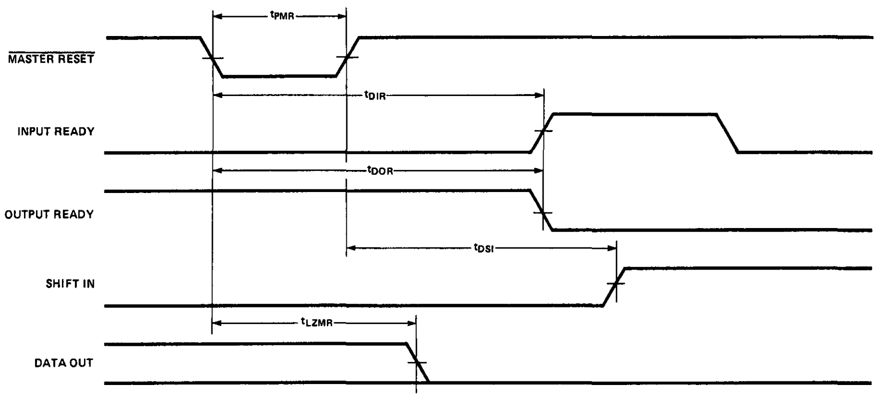
Switching Waveforms (Continued)

Bubble Through, Data In To Data Out Diagram



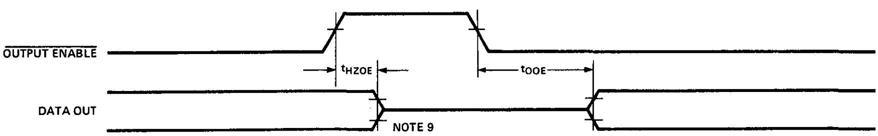
0014–10

Master Reset Timing Diagram



0014–11

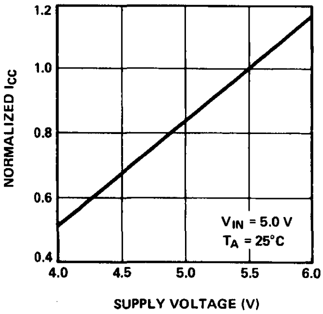
Output Enable Timing Diagram



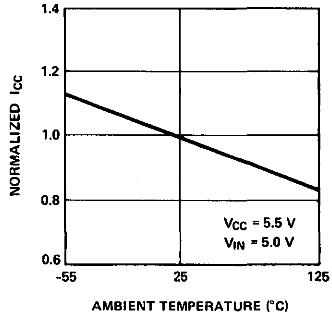
0014–12

Typical DC and AC Characteristics

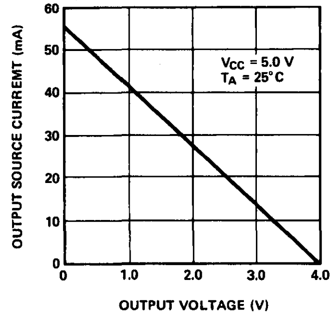
NORMALIZED SUPPLY CURRENT
vs. SUPPLY VOLTAGE



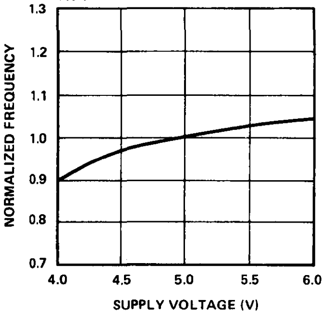
NORMALIZED SUPPLY CURRENT
vs. AMBIENT TEMPERATURE



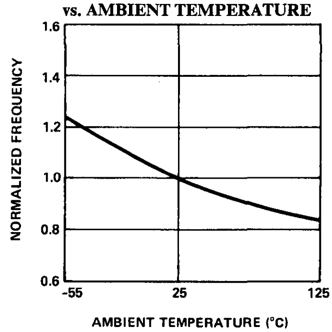
OUTPUT SOURCE CURRENT
vs. OUTPUT VOLTAGE



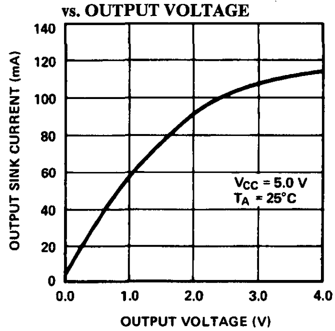
NORMALIZED FREQUENCY
vs. SUPPLY VOLTAGE



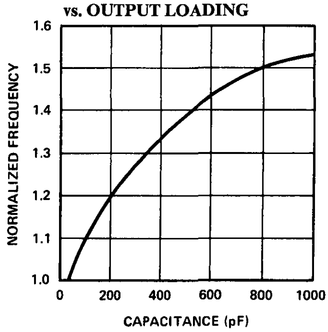
NORMALIZED FREQUENCY
vs. AMBIENT TEMPERATURE



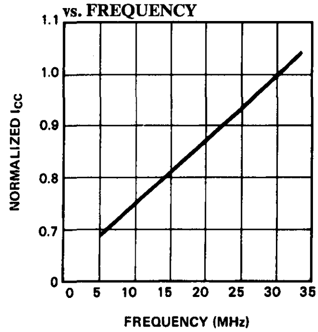
OUTPUT SINK CURRENT
vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE
vs. OUTPUT LOADING



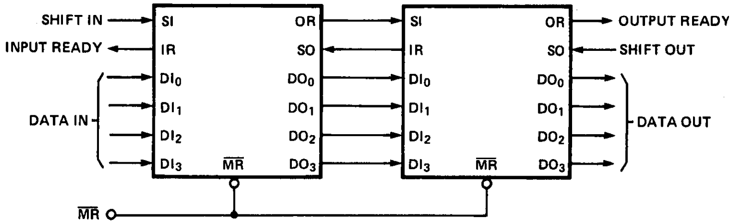
NORMALIZED I_{CC}
vs. FREQUENCY



0014-13

FIFO Expansion

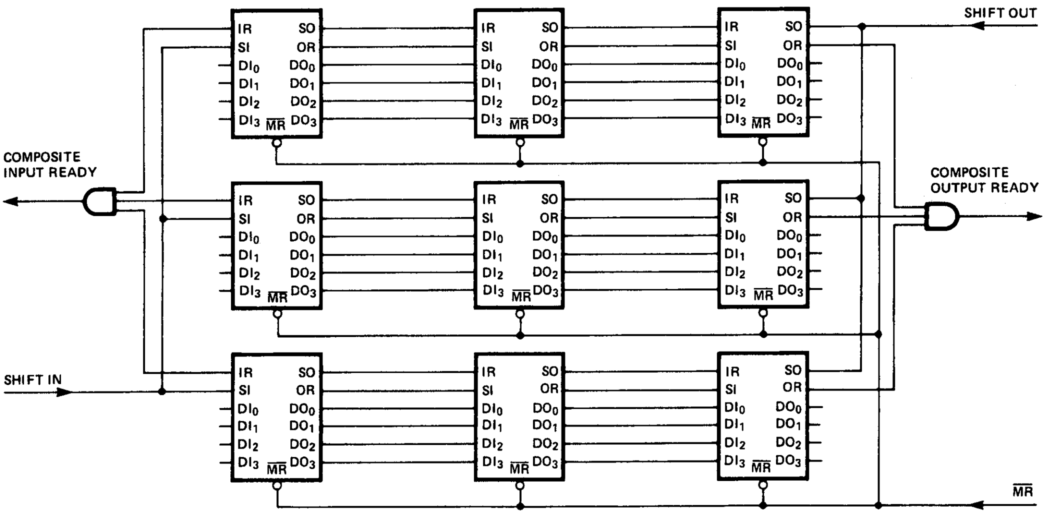
128 x 4 Application



0014–14

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

192 x 12 Application



0014–15

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the variation of delays of the FIFOs.

User Notes:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All Cypress FIFOs will cascade with other Cypress FIFOs. However, they may not cascade with pin-compatible FIFO's from other manufacturers.

5

Ordering Information

Ordering Code (25 MHz)	Package Type	Operating Range
CY7C401-25PC	P1	Com.
CY7C402-25PC	P3	
CY7C403-25PC	P1	
CY7C404-25PC	P3	
CY7C401-25DC	D2	
CY7C402-25DC	D4	
CY7C403-25DC	D2	
CY7C404-25DC	D4	
CY7C401-25LC	L61	
CY7C402-25LC	L61	
CY7C403-25LC	L61	
CY7C404-25LC	L61	
CY7C401-25DMB	D2	Mil.
CY7C402-25DMB	D4	
CY7C403-25DMB	D2	
CY7C404-25DMB	D4	
CY7C401-25LMB	L61	
CY7C402-25LMB	L61	
CY7C403-25LMB	L61	
CY7C404-25LMB	L61	

Ordering Code (15 MHz)	Package Type	Operating Range
CY7C401-15PC	P1	Com.
CY7C402-15PC	P3	
CY7C403-15PC	P1	
CY7C404-15PC	P3	
CY7C401-15DC	D2	
CY7C402-15DC	D4	
CY7C403-15DC	D2	
CY7C404-15DC	D4	
CY7C401-15LC	L61	
CY7C402-15LC	L61	
CY7C403-15LC	L61	
CY7C404-15LC	L61	
CY7C401-15DMB	D2	Mil.
CY7C402-15DMB	D4	
CY7C403-15DMB	D2	
CY7C404-15DMB	D4	
CY7C401-15LMB	L61	
CY7C402-15LMB	L61	
CY7C403-15LMB	L61	
CY7C404-15LMB	L61	

Ordering Code (10 MHz)	Package Type	Operating Range
CY7C401-10PC	P1	Com.
CY7C402-10PC	P3	
CY7C403-10PC	P1	
CY7C404-10PC	P3	
CY7C401-10DC	D2	
CY7C402-10DC	D4	
CY7C403-10DC	D2	
CY7C404-10DC	D4	
CY7C401-10LC	L61	
CY7C402-10LC	L61	
CY7C403-10LC	L61	
CY7C404-10LC	L61	
CY7C401-10DMB	D2	Mil.
CY7C402-10DMB	D4	
CY7C403-10DMB	D2	
CY7C404-10DMB	D4	
CY7C401-10LMB	L61	
CY7C402-10LMB	L61	
CY7C403-10LMB	L61	
CY7C404-10LMB	L61	

Ordering Code (5 MHz)	Package Type	Operating Range
CY7C401-5PC	P1	Com.
CY7C402-5PC	P3	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{OS}	1,2,3
I_{CC}	1,2,3

5

Switching Characteristics

Parameters	Subgroups
f_O	7,8,9,10,11
t_{PHSI}	7,8,9,10,11
t_{PLSI}	7,8,9,10,11
t_{SSI}	7,8,9,10,11
t_{HSI}	7,8,9,10,11
t_{DLIR}	7,8,9,10,11
t_{DHIR}	7,8,9,10,11
t_{PHSO}	7,8,9,10,11
t_{PLSO}	7,8,9,10,11
t_{DLOR}	7,8,9,10,11
t_{DHOR}	7,8,9,10,11
t_{SOR}	7,8,9,10,11
t_{HSO}	7,8,9,10,11
t_{BT}	7,8,9,10,11
t_{SIR}	7,8,9,10,11
t_{HIR}	7,8,9,10,11
t_{PIR}	7,8,9,10,11
t_{POR}	7,8,9,10,11
t_{PMR}	7,8,9,10,11
t_{DSI}	7,8,9,10,11
t_{DOR}	7,8,9,10,11
t_{DIR}	7,8,9,10,11
t_{LZMR}	7,8,9,10,11

Parameters	Subgroups
t_{OOE}	7,8,9,10,11
t_{HZOE}	7,8,9,10,11

Document #: 38-00040-D

CYPRESS SEMICONDUCTOR

Cascadeable 64 x 8 FIFO
Cascadeable 64 x 9 FIFO

Features

- **64 x 8 and 64 x 9 first-in first-out (FIFO) buffer memory**
- **35 MHz shift-in and shift-out rates**
- **Almost Full/Almost Empty and Half Full flags**
- **Dual port RAM architecture**
- **Fast, 50 ns, bubblethrough**
- **Independent asynchronous inputs and outputs**
- **Output Enable (CY7C408A)**
- **Expandable in word width and FIFO depth**
- **5V ±10% supply**
- **TTL compatible**
- **Capable of withstanding greater than 2000V electrostatic discharge voltage**
- **300 mil, 28-pin DIP**

Functional Description

The CY7C408A and CY7C409A are 64-word deep by 8- or 9-bit wide first-in first-out (FIFO) buffer memories. In addition to the industry standard handshaking signals, Almost Full/Almost Empty (AFE) and Half Full (HF) flags are provided. AFE is HIGH when the FIFO is almost full or almost empty, otherwise AFE is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW.

The CY7C408A has an Output Enable (OE) function.

The memory accepts 8- or 9-bit parallel words at its inputs (DI_0-DI_8) under the control of the Shift-In (SI) input when the Input-Ready (IR) control signal is HIGH. The data is output, in the same order as it was stored, on the DO_0-DO_8 output pins under the control of the Shift-Out (SO) input when the Output-Ready (OR) control signal is HIGH. If the FIFO is full (IR LOW), pulses at the SI input are ignored: if the FIFO is empty (OR LOW), pulses at the SO input are ignored.

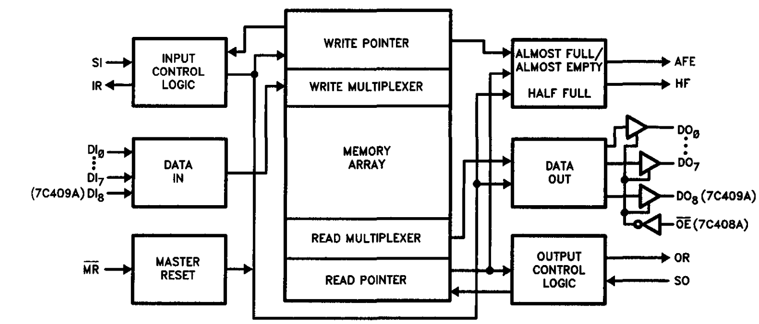
The IR and OR signals are also used to connect the FIFO's in parallel to make a wider word, or in series to make a deeper buffer, or both.

Parallel expansion for wider words is implemented by logically ANDing the IR and OR outputs (respectively) of the individual FIFOs together *(Figure 7)*. The AND operation insures that all of the FIFOs are either ready to accept more data (IR HIGH) or are ready to output data (OR HIGH) and thus compensate for variations in propagation delay times between devices.

Serial expansion (cascading) for deeper buffer memories is accomplished by connecting the data outputs of the FIFO closest to the data source (upstream device) to the data inputs of the following (downstream) FIFO *(Figure 6)*. In addition, to insure proper operation, the SO signal of the upstream FIFO must be connected to the IR output of the downstream FIFO and the SI signal of the downstream FIFO must be connected to the OR output of the upstream FIFO. In this serial expansion configuration, the IR and OR signals are used to pass data through the FIFOs.

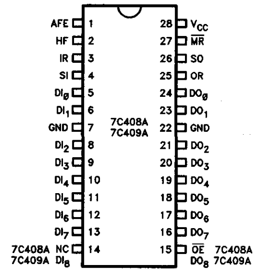
Reading and writing operations are completely asynchronous, allowing the FIFO to be used as a buffer between two digital machines of widely differing operating frequencies. The high shift-in and shift-out rates of these FIFOs, and their high throughput rate due to the fast bubblethrough time, which is due to their dual port RAM architecture, make them ideal for high speed communications and controllers.

Logic Block Diagram

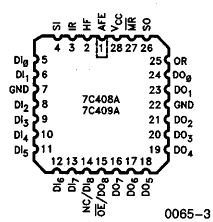


0065-1

Pin Configurations



0065-2



0065-3

Flag Definitions

HF	AFE	Words Stored
L	H	0–8
L	L	9–31
H	L	32–55
H	H	56–64

Selection Guide

		7C408A-15 7C409A-15	7C408A-25 7C409A-25	7C408A-35 7C409A-35
Maximum Shift Rate (MHz)		15	25	35
Maximum Operating Current (mA)[2]	Commercial	115	125	135
	Military	140	150	N/A

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State (7C408A) .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage .... > 2001V (per MIL-STD-883 Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[4]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range (Unless Otherwise Noted)[5]

Parameters	Description	Test Conditions		CY7C408A CY7C409A Min.	CY7C408A CY7C409A Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−90	mA
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$	Commercial		100	mA
			Military		125	mA
I_{CC}	Power Supply Current	$I_{CC} = I_{CCQ} + 1\ \text{mA/MHz} \times (f_{SI} + f_{SO})/2$				

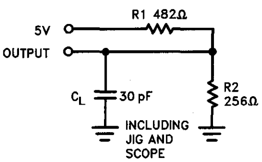
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:

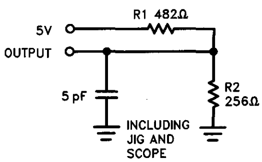
1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. $I_{CC} = I_{CCQ} + 1\ \text{mA/MHz} \times (f_{SI} + f_{SO})/2$
3. Tested initially and after any design or process changes that may affect these parameters.
4. T_A is the "instant on" case temperature.
5. See the last page of this specification for Group A subgroup testing information.

AC Test Load and Waveforms



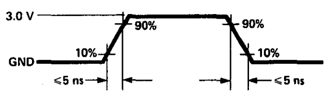
0065-4

Figure 1a



0065-21

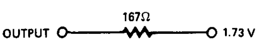
Figure 1b



0065-5

Figure 2. All Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



0065-6

Switching Characteristics Over the Operating Range[5, 6]

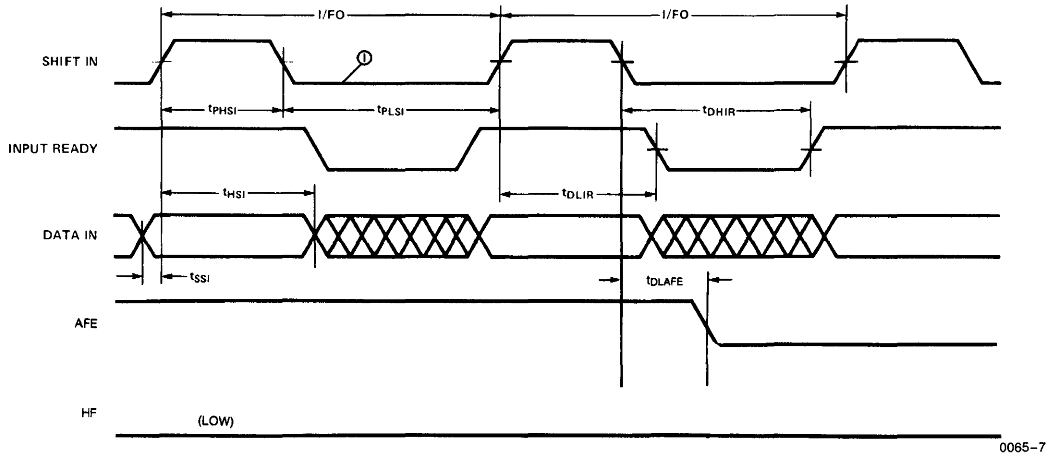
Parameters	Description	Test Conditions	CY7C408A-15 CY7C409A-15		CY7C408A-25 CY7C409A-25		CY7C408A-35 CY7C409A-35		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
f_O	Operating Frequency	Note 7		15		25		35	MHz
t_{PHSI}	SI HIGH Time	Note 7	23		11		9		ns
t_{PLSI}	SI LOW Time	Note 7	25		24		17		ns
t_{SSI}	Data Setup to SI	Note 8	0		0		0		ns
t_{HSI}	Data Hold from SI	Note 8	30		20		12		ns
t_{DLIR}	Delay, SI HIGH to IR LOW			35		21		15	ns
t_{DHIR}	Delay, SI LOW to IR HIGH			40		23		16	ns
t_{PHSO}	SO HIGH Time	Note 7	23		11		9		ns
t_{PLSO}	SO LOW Time	Note 7	25		24		17		ns
t_{DLOR}	Delay, SO HIGH to OR LOW			35		21		15	ns
t_{DHOR}	Delay, SO LOW to OR HIGH			40		23		16	ns
t_{SOR}	Data Setup to OR HIGH		0		0		0		ns
t_{HSO}	Data Hold from SO LOW		0		0		0		ns
t_{BT}	Fallthrough, Bubbleback Time		10	65	10	60	10	50	ns
t_{SIR}	Data Setup to IR	Note 9	5		5		5		ns
t_{HIR}	Data Hold from IR	Note 9	30		20		20		ns
t_{PIR}	Input Ready Pulse HIGH	Note 10	6		6		6		ns
t_{POR}	Output Ready Pulse HIGH	Note 11	6		6		6		ns
t_{DLZOE}	OE LOW to LOW Z (7C408)	Note 12		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (7C408)	Note 12		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH			65		55		45	ns
t_{DLHF}	SO LOW to HF LOW			65		55		45	ns
t_{DLAFE}	SO or SI LOW to AFE LOW			65		55		45	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH			65		55		45	ns
t_{PMR}	$\overline{MR}$ Pulse Width		55		45		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		10		10		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			55		45		35	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			55		45		35	ns
t_{LZMR}	$\overline{MR}$ LOW to Output LOW	Note 13		55		45		35	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH			55		45		35	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW			55		45		35	ns
t_{OD}	SO LOW to Next Data Out Valid			28		20		16	ns

Notes:

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1*.
7. $1/f_O \geq (t_{PHSI} + t_{PLSI})$, $1/f_O \geq (t_{PHSO} + t_{PLSO})$.
8. t_{SSI} and t_{HSI} apply when memory is not full.
9. t_{SIR} and t_{HIR} apply when memory is full, SI is HIGH and minimum bubblethrough (t_{BT}) conditions exist.
10. At any given operating condition $t_{PIR} \geq$ (t_{PHSO} required).
11. At any given operating condition $t_{POR} \geq$ (t_{PHSI} required).
12. t_{DHZOE} and t_{DLZOE} are specified with $C_L = 5$ pF as in *Figure 1b.* t_{DHZOE} transition is measured ± 500 mV from steady state voltage. t_{DLZOE} transition is measured ± 100 mV from steady state voltage. These parameters are guaranteed and not 100% tested.
13. All data outputs will be at LOW level after reset goes HIGH until data is entered into the FIFO.

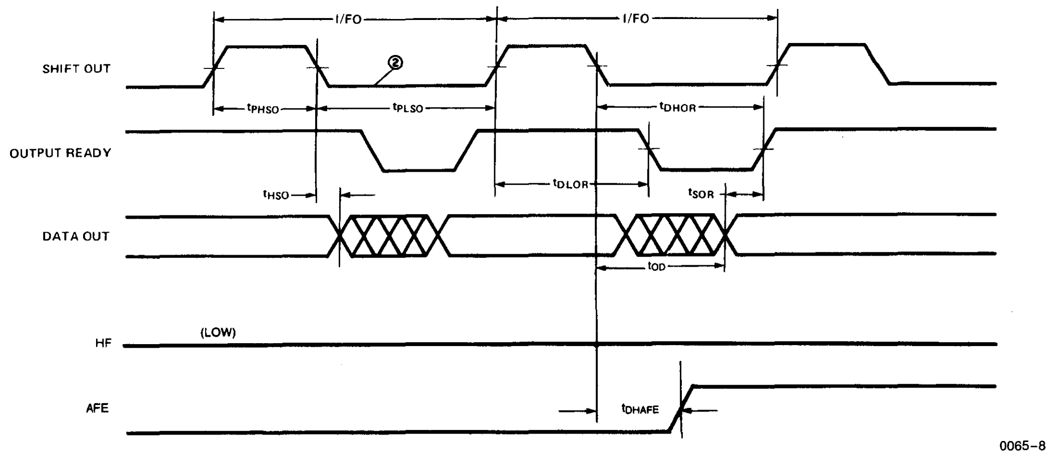
Switching Waveforms

Data In Timing Diagram



① FIFO Contains 8 Words

Data Out Timing Diagram

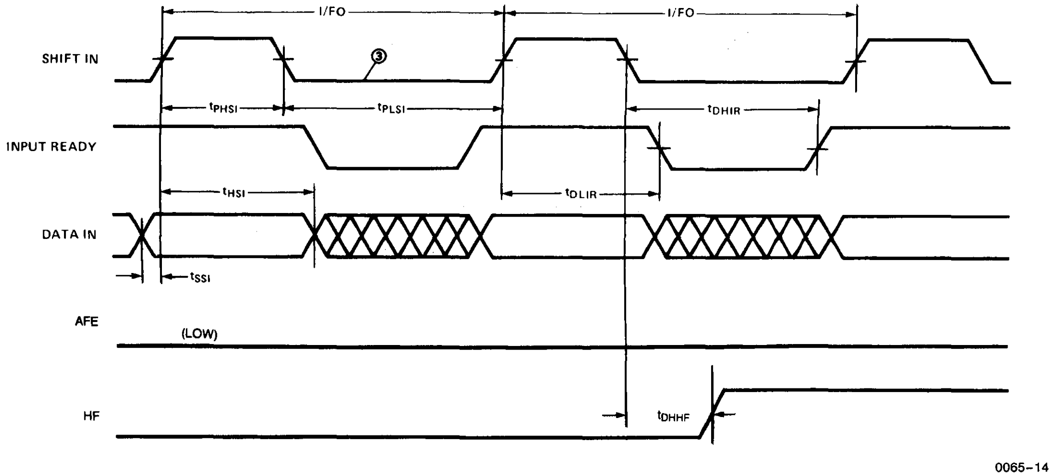


② FIFO Contains 9 Words

5

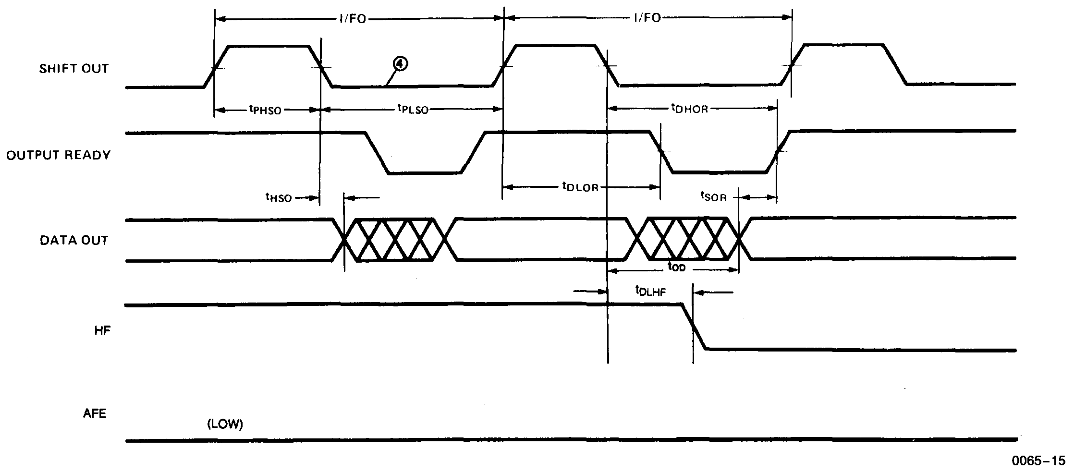
Switching Waveforms (Continued)

Data In Timing Diagram



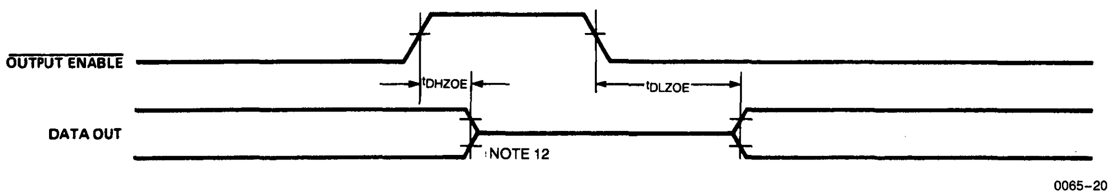
③ FIFO Contains 31 Words

Data Out Timing Diagram



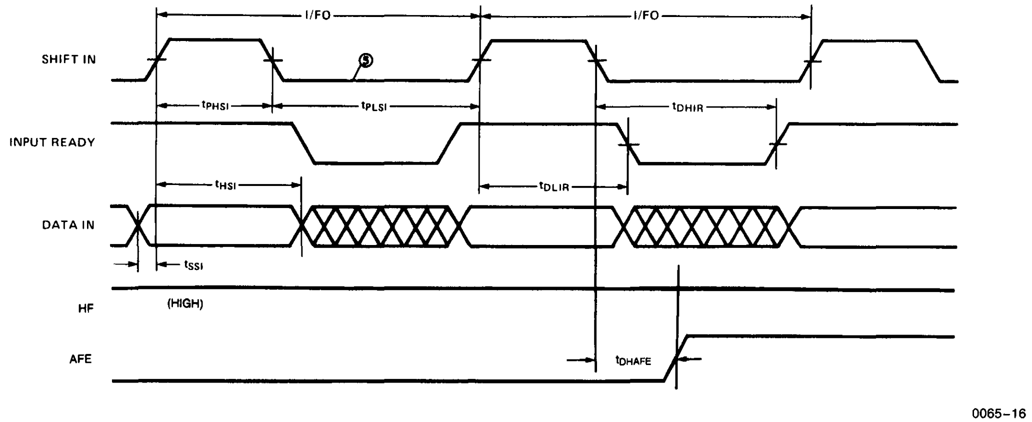
④ FIFO Contains 32 Words

Output Enable (CY7C408A only)



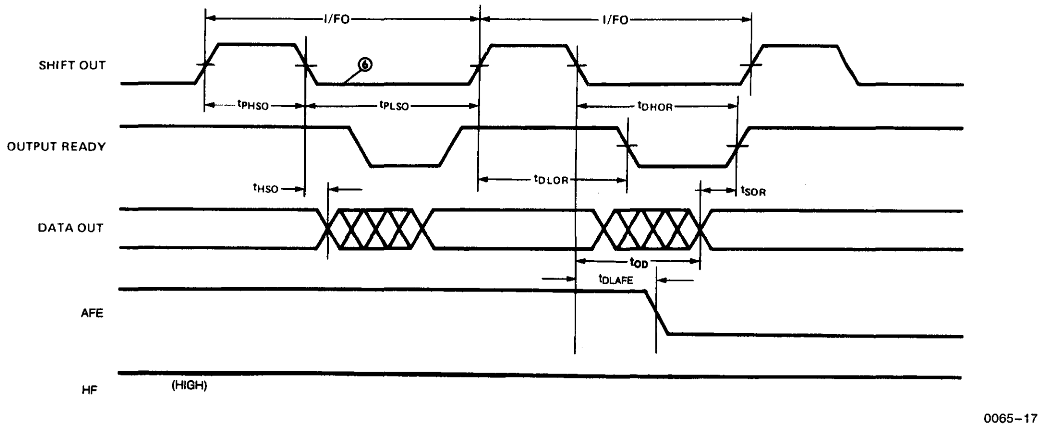
Switching Waveforms (Continued)

Data In Timing Diagram



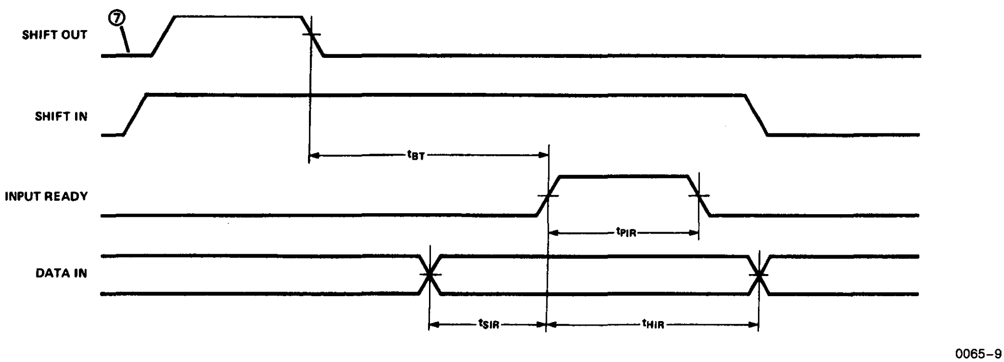
⑤ FIFO Contains 55 Words

Data Out Timing Diagram



⑥ FIFO Contains 56 Words

Bubbleback, Data Out to Data In Diagram

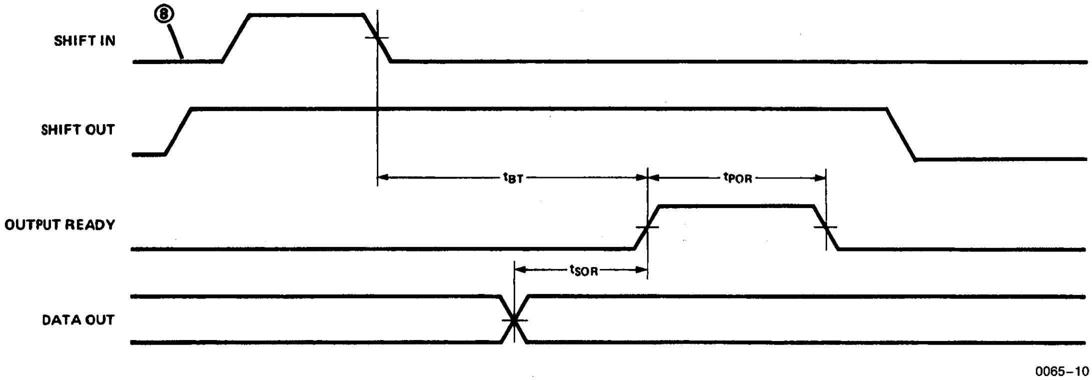


⑦ FIFO Contains 64 Words

5

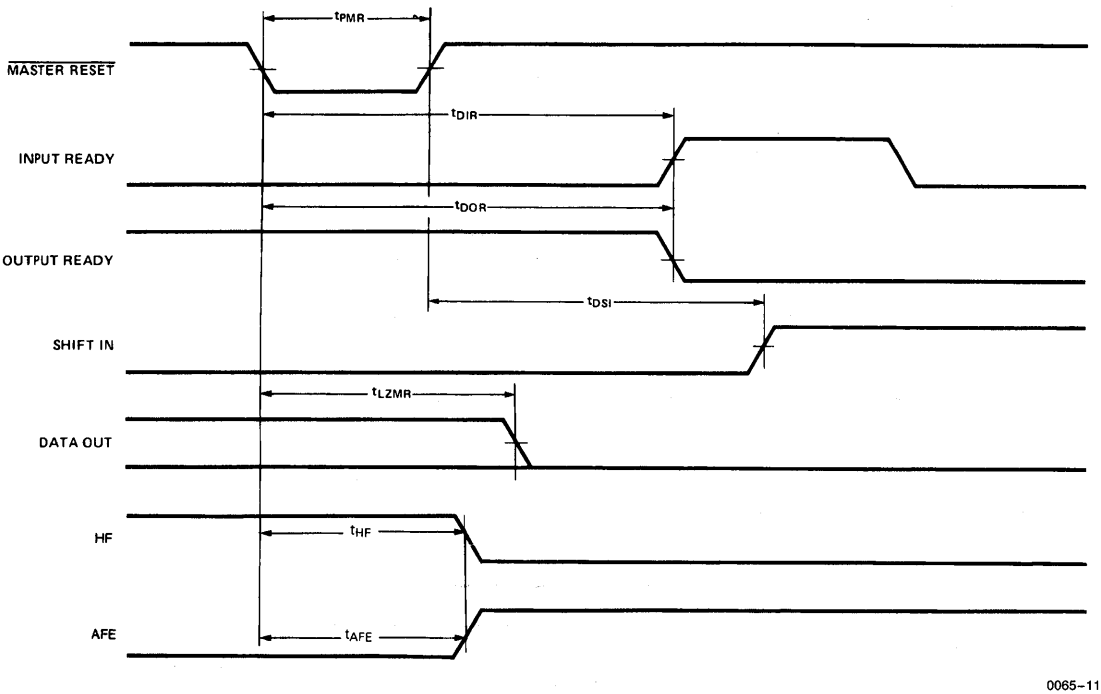
Switching Waveforms (Continued)

Fallthrough, Data In to Data Out Diagram

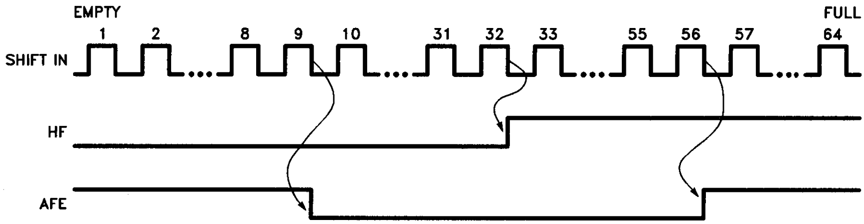


⑧ FIFO Is Empty

Master Reset Timing Diagram



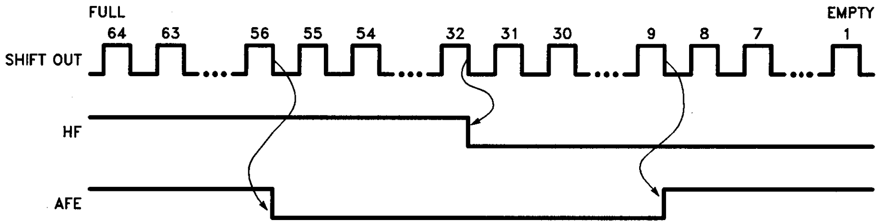
Shifting Words In



0065-18

Figure 3

Shifting Words Out



0065-19

Figure 4

Architecture of the CY7C408A and CY7C409A

The CY7C408A and CY7C409A FIFOs consist of an array of 64 words of 8- or 9-bits each (which are implemented using a dual port RAM cell), a write pointer, a read pointer and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the Almost Full/Almost Empty (AFE) and the Half Full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard CY7C401/402/403/404 FIFOs.

Dual Port RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Fallthrough and Bubbleback

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the Fallthrough time.

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the Bubbleback time.

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fallthrough time when it is empty (or near empty) and by the bubbleback time when it is full (or near full).

The conventional definitions of fallthrough and bubbleback do not apply to the CY7C408A and CY7C409A FIFOs because the data is not physically propagated through the memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

Resetting the FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (DO_0–DO_8) will be LOW. The AFE flag will be HIGH and the HF flag will be LOW.

Shifting Data Into the FIFO

The availability of an empty location is indicated by the HIGH state of the Input Ready (IR) signal. When IR is HIGH a LOW to HIGH transition on the Shift-In (SI) pin will clock the data on the DI_0–DI_8 inputs into the FIFO. Data propagates through the device at the falling edge of SI.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH to LOW transition of the SI signal initiates the LOW to HIGH transition of the IR signal if the FIFO is not full. If the FIFO is full, IR will remain LOW.

Shifting Data Out of the FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the Output Ready (OR) signal. After the FIFO is reset all data outputs (DO_0-DO_8) will be in the LOW state. As long as the FIFO remains empty the OR signal will be LOW and all Shift Out (SO) pulses applied to it will be ignored. After data is shifted into the FIFO the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate a SO pulse. The data outputs of the FIFO should be sampled with edge sensitive type D flip-flops (or equivalent), using the SO signal as the clock input to the flip-flop.

Interfacing to the FIFO Application Brief

See the application brief in the back of this databook for information regarding interfacing to the FIFO under asynchronous operating conditions.

AFE and HF Flags

Two flags, Almost Full/Almost Empty (AFE) and Half Full (HF), describe how many words are stored in the FIFO. AFE is HIGH when there are eight or less, or 56 or more, words stored in the FIFO. Otherwise the AFE flag is LOW. HF is HIGH when there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO (*Figures 3* and *4*).

Due to the asynchronous nature of the SI and SO signals, it is possible to encounter specific timing relationships which may cause short pulses on the AFE and HF flags. These pulses are entirely due to the dynamic relationship of the SI and SO signals. The flags, however, will always settle to their correct state after the appropriate delay (t_{DHAFE}, t_{DLAFE}, t_{DHHF} or t_{DLHF}). Therefore, use of level-sensitive rather than edge-sensitive flag detection devices is recommended to avoid false flag encoding.

Cascading the 7C408/9A-35 Above 25 MHz

If cascaded FIFOs are to be operated with an external clock rate greater than 25 MHz, the interface IR signal must be inverted before being fed back to the interface SO pin *(Figure 5)*. Two things should be noted when this configuration is implemented.

First, the capacity of N cascaded FIFOs is decreased from $N \times 64$ to $(N \times 63) + 1$.

Secondly, the frequency at the cascade interface is less than the 35 MHz rate at which the external clocks may operate. Therefore, the first device has its data Shifted-In faster than it is Shifted-Out and eventually this device becomes momentarily full. When this occurs, the maximum sustainable external clock frequency changes from 35 MHz to the cascade interface frequency.[14]

When data packets[15] are transmitted, this phenomenon does not occur unless more than three FIFOs are depth cascaded. For example, if two FIFOs are cascaded, a packet of 127 ($= 2 \times 63 + 1$) words may be shifted-in at up to 35 MHz and then the entire packet may be shifted-out at up to 35 MHz.

If data is to be shifted-out simultaneously with the data being shifted-in, the concept of "virtual capacity" is introduced. Virtual capacity is simply how large a packet of data can be shifted-in at a fixed frequency, e.g., 35 MHz, simultaneously with data being shifted-out at any given frequency. *Figure 8* is a graph of packet size[16] vs. shift-out frequency (f_{SOx}) for two different values of Shift-In frequency (f_{SIx}) when two FIFOs are cascaded.

The exact complement of this occurs if the FIFOs initially contain data and a high Shift-Out frequency is to be maintained, i.e., a 35 MHz f_{SOx} can be sustained when reading data packets from devices cascaded two or three deep. If data is shifted-in simultaneously, *Figure 8* applies with f_{SIx} and f_{SOx} interchanged.

Notes:

14. Because the data throughput in the cascade interface is dependent on the inverter delay, it is recommended that the fastest available inverter be used.
15. Transmission of data packets assumes that up to the maximum cumulative capacity of the FIFOs is Shifted-In without simultaneous Shift-Out clocks occurring. The complement of this holds when data is Shifted-Out as a packet.
16. These are typical packet sizes using an inverter whose delay is 4 ns.
17. Only devices with the same speed grade are specified to cascade together.

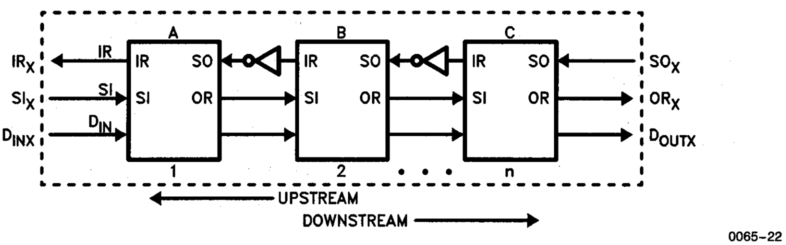


Figure 5. Cascaded Configuration Above 25 MHz

FIFO Expansion

128 x 9 Configuration

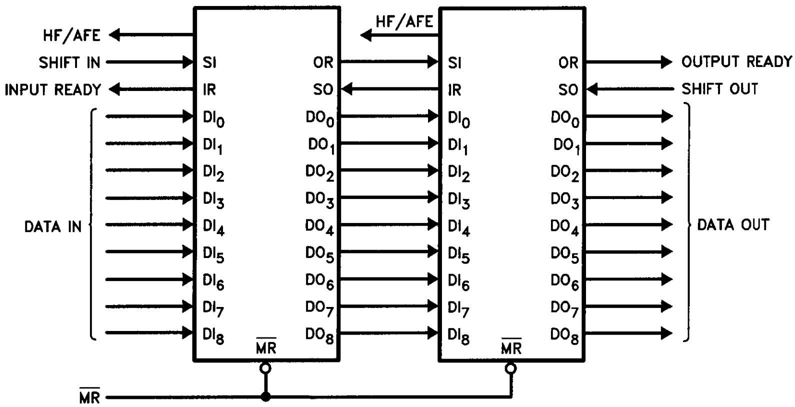


Figure 6. Cascaded Configuration at or below 25 MHz

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

User Notes referencing *Figures 6* and *7*:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{POR}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW.

FIFO Expansion (Continued)

192 x 27 Configuration

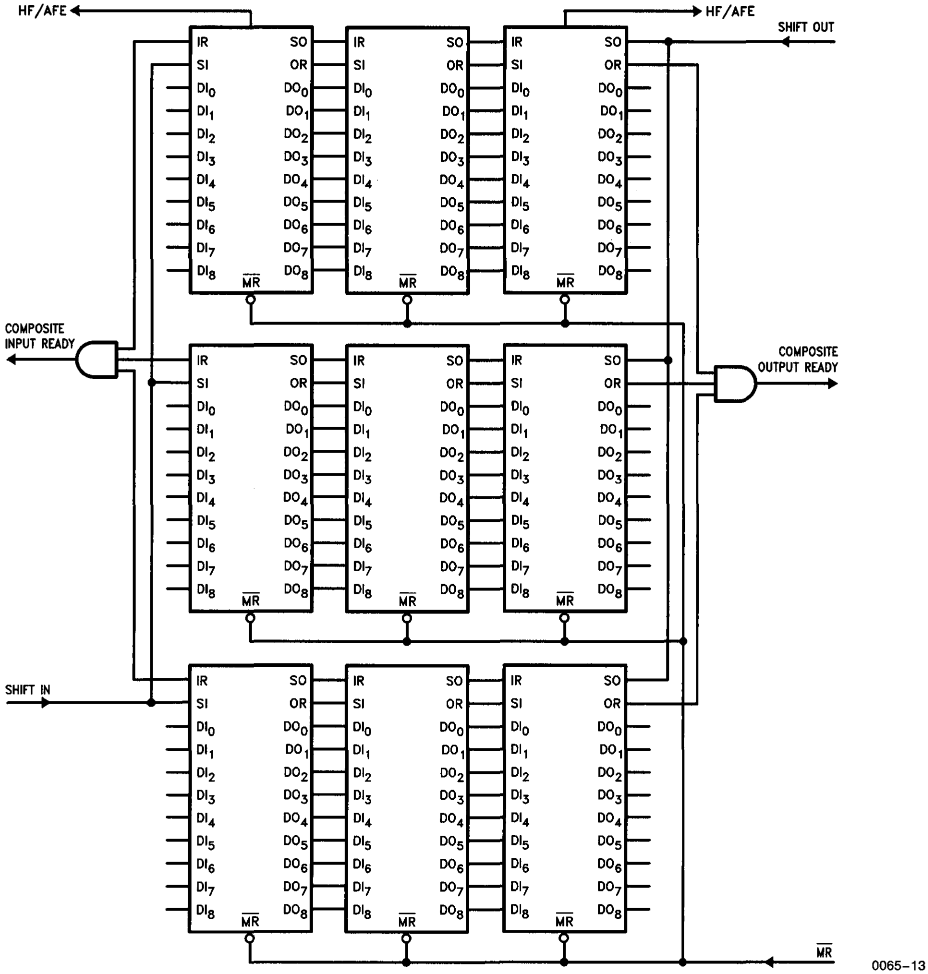


Figure 7. Depth and Width Expansion

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the variation of delays of the FIFOs.

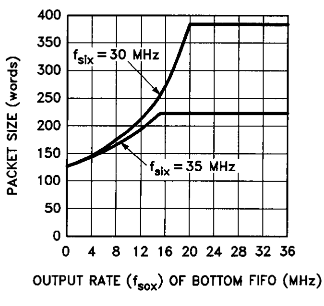
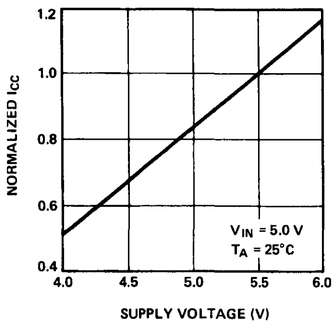


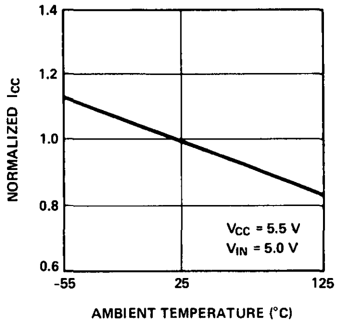
Figure 8. Virtual Capacity vs. Output Rate for Two FIFOs Cascaded Using an Inverter

Typical DC and AC Characteristics

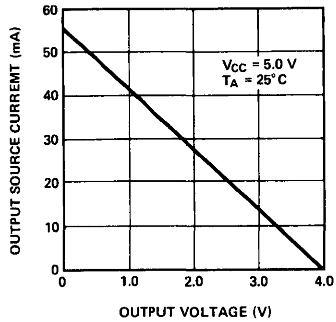
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



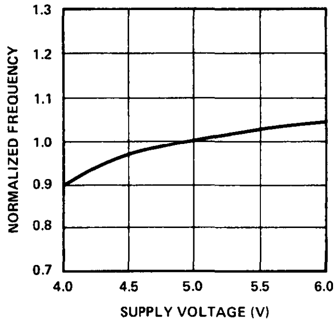
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



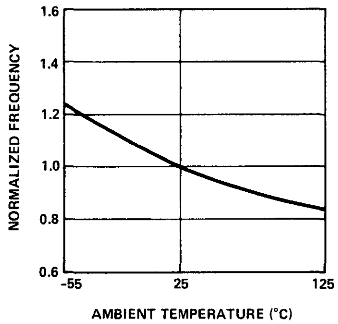
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



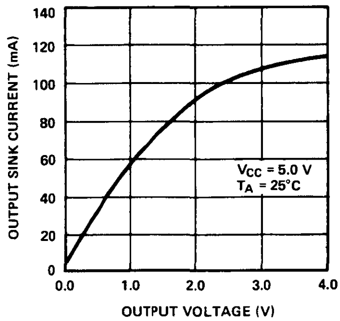
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



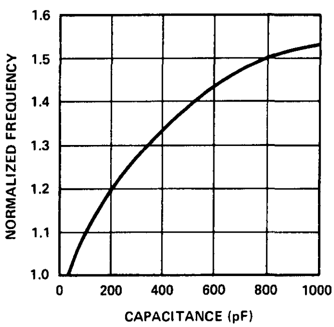
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



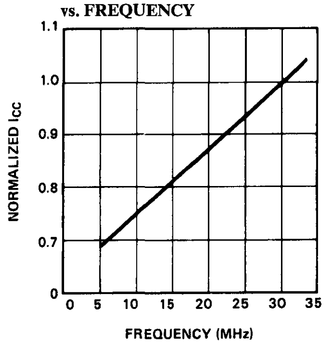
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL FREQUENCY CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0065-23

Ordering Information

Frequency (MHz)	Ordering Code	Package Type	Operating Range
35	CY7C408A-35PC	P21	Commercial
	CY7C408A-35DC	D22	
	CY7C408A-35LC	L64	
	CY7C408A-35VC	V21	
25	CY7C408A-25PC	P21	Commercial
	CY7C408A-25DC	D22	
	CY7C408A-25LC	L64	
	CY7C408A-25VC	V21	
	CY7C408A-25DMB	D22	Military
	CY7C408A-25LMB	L64	
	CY7C408A-25KMB	K74	
15	CY7C408A-15PC	P21	Commercial
	CY7C408A-15DC	D22	
	CY7C408A-15LC	L64	
	CY7C408A-15VC	V21	
	CY7C408A-15DMB	D22	Military
	CY7C408A-15LMB	L64	
	CY7C408A-15KMB	K74	

Frequency (MHz)	Ordering Code	Package Type	Operating Range
35	CY7C409A-35PC	P21	Commercial
	CY7C409A-35DC	D22	
	CY7C409A-35LC	L64	
	CY7C409A-35VC	V21	
25	CY7C409A-25PC	P21	Commercial
	CY7C409A-25DC	D22	
	CY7C409A-25LC	L64	
	CY7C409A-25VC	V21	
	CY7C409A-25DMB	D22	Military
	CY7C409A-25LMB	L64	
	CY7C409A-25KMB	K74	
15	CY7C409A-15PC	P21	Commercial
	CY7C409A-15DC	D22	
	CY7C409A-15LC	L64	
	CY7C409A-15VC	V21	
	CY7C409A-15DMB	D22	Military
	CY7C409A-15LMB	L64	
	CY7C409A-15KMB	K74	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OS}	1,2,3
I_{CCQ}	1,2,3

Switching Characteristics

Parameters	Subgroups
f_O	7,8,9,10,11
t_{PHSI}	7,8,9,10,11
t_{PLSI}	7,8,9,10,11
t_{SSI}	7,8,9,10,11
t_{HSI}	7,8,9,10,11
t_{DLIR}	7,8,9,10,11
t_{DHIR}	7,8,9,10,11
t_{PHSO}	7,8,9,10,11
t_{PLSO}	7,8,9,10,11
t_{DLOR}	7,8,9,10,11
t_{DHOR}	7,8,9,10,11
t_{SOR}	7,8,9,10,11
t_{HSO}	7,8,9,10,11
t_{BT}	7,8,9,10,11
t_{SIR}	7,8,9,10,11
t_{HIR}	7,8,9,10,11
t_{PIR}	7,8,9,10,11
t_{POR}	7,8,9,10,11
t_{SIIR}	7,8,9,10,11
t_{SOOR}	7,8,9,10,11
t_{DLZOE}	7,8,9,10,11
t_{DHZOE}	7,8,9,10,11
t_{DHHF}	7,8,9,10,11
t_{DLHF}	7,8,9,10,11

Parameters	Subgroups
t_{DLAFE}	7,8,9,10,11
t_{DHAFE}	7,8,9,10,11
t_B	7,8,9,10,11
t_{OD}	7,8,9,10,11
t_{PMR}	7,8,9,10,11
t_{DSI}	7,8,9,10,11
t_{DOR}	7,8,9,10,11
t_{DIR}	7,8,9,10,11
t_{LZMR}	7,8,9,10,11
t_{AFE}	7,8,9,10,11
t_{HF}	7,8,9,10,11

Document #: 38-00059-E

CY7C420, CY7C421, CY7C424
CY7C425, CY7C428, CY7C429

CYPRESS SEMICONDUCTOR

Cascadeable 512 x 9 FIFO
Cascadeable 1024 x 9 FIFO
Cascadeable 2048 x 9 FIFO

Features

- **512 x 9, 1024 x 9, 2048 x 9 FIFO buffer memory**
- **Dual port RAM cell**
- **Asynchronous read/write**
- **High speed 33.3 MHz read/write independent of depth/width**
- **Low operating power**
  I_{CC} (max.) = 142 mA commercial
  I_{CC} (max.) = 147 mA military
- **Half full flag in standalone**
- **Empty and full flags**
- **Retransmit in standalone**
- **Expandable in width and depth**
- **Parallel Cascade minimizes bubblethrough**
- **5V ±10% supply**
- **300 mil DIP packaging**
- **300 mil SOJ packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functional equivalent to IDT7201, IDT7202 and IDT7203**

Functional Description

The (CY7C420, CY7C421,) (CY7C424, CY7C425,) and (CY7C428, CY7C429) are, respectively, 512, 1024 and 2048 words by 9-bit wide first-in first-out (FIFO) memories offered in 600 mil wide and 300 mil wide packages, respectively. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

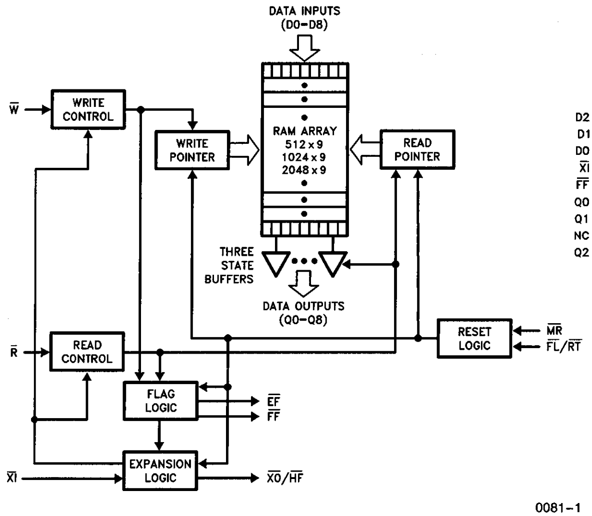
The read and write operations may be asynchronous; each can occur at a rate of 33.3 MHz. The write operation occurs when the Write ($\overline{W}$) signal is LOW. Read occurs when Read ($\overline{R}$) goes LOW. The 9 data outputs go to the high impedance state when $\overline{R}$ is HIGH.

A Half-Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration this pin provides the expansion out ($\overline{XO}$) information which is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations a LOW on the Retransmit ($\overline{RT}$) input causes the FIFO's to retransmit the data. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data.

The CY7C420, CY7C421, CY7C424, CY7C425, CY7C428 and CY7C429 are fabricated using an advanced 0.8 micron N-well CMOS technology. Input ESD protection is greater than 2000V and latchup is prevented by careful layout, guard rings and a substrate bias generator.

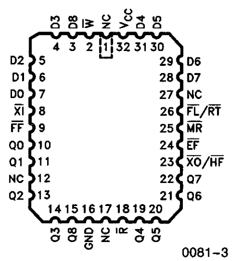
Logic Block Diagram



0081–1

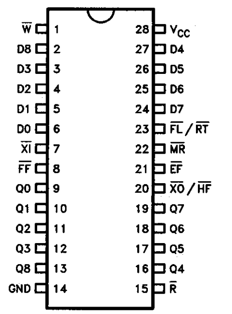
Pin Configurations

PLCC/LCC
Top View



0081–3

DIP
Top View



0081–2

Selection Guide

		7C420-20, 7C421-20 7C424-20, 7C425-20 7C428-20, 7C429-20	7C420-25, 7C421-25 7C424-25, 7C425-25 7C428-25, 7C429-25	7C420-30, 7C421-30 7C424-30, 7C425-30 7C428-30, 7C429-30	7C420-40, 7C421-40 7C424-40, 7C425-40 7C428-40, 7C429-40	7C420-65, 7C421-65 7C424-65, 7C425-65 7C428-65, 7C429-65
Frequency (MHz)		33.3	28.5	25	20	12.5
Access Time (ns)		20	25	30	40	65
Maximum Operating Current (mA)	Commercial	142	132	125	115	100
	Military		147	140	130	115

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015)

Latch-up Current........................ >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[4]

Parameter	Description	Test Conditions		CY7C420-20 CY7C421-20 CY7C424-20 CY7C425-20 CY7C428-20 CY7C429-20 Min.	Max.	CY7C420-25 CY7C421-25 CY7C424-25 CY7C425-25 CY7C428-25 CY7C429-25 Min.	Max.	CY7C420-30 CY7C421-30 CY7C424-30 CY7C425-30 CY7C428-30 CY7C429-30 Min.	Max.	CY7C420-40 CY7C421-40 CY7C424-40 CY7C425-40 CY7C428-40 CY7C429-40 Min.	Max.	CY7C420-65 CY7C421-65 CY7C424-65 CY7C425-65 CY7C428-65 CY7C429-65 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2 mA		2.4		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		COM'L	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
			MIL/IND					2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	COM'L[5]		142		132		125		115		100	mA
			MIL[6]/IND				147		140		130		115	mA
I_{SB_1}	Standby Current	All Inputs = V_{IH} Min.	COM'L		30		25		25		25		25	mA
			MIL/IND				30		30		30		30	mA
I_{SB_2}	Power Down Current	All Inputs V_{CC} −0.2V	COM'L		25		20		20		20		20	mA
			MIL/IND				25		25		25		25	mA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−90		−90		−90		−90		−90	mA

Shaded area contains preliminary information.

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:

1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. I_{CC} (commercial) = 100 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
6. I_{CC} (military) = 115 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.

AC Test Load and Waveform

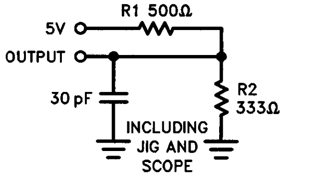


Figure 1a

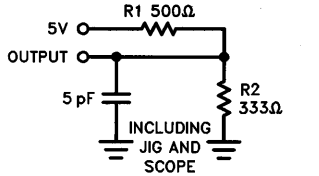


Figure 1b

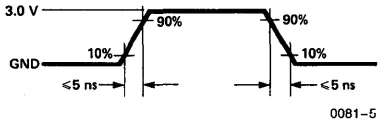
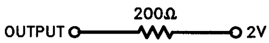


Figure 2. All Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[1, 4]

Parameter	Description	7C420-20, 7C421-20 7C424-20, 7C425-20 7C428-20, 7C429-20		7C420-25, 7C421-25 7C424-25, 7C425-25 7C428-25, 7C429-25		7C420-30, 7C421-30 7C424-30, 7C425-30 7C428-30, 7C429-30		7C420-40, 7C421-40 7C424-40, 7C425-40 7C428-40, 7C429-40		7C420-65, 7C421-65 7C424-65, 7C425-65 7C428-65, 7C429-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	30		35		40		50		80		ns
t_{A}	Access Time		20		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		10		15		ns
t_{PR}	Read Pulse Width	20		25		30		40		65		ns
t_{LZR}[3]	Read LOW to Low Z	3		3		3		3		3		ns
t_{DVR}[2, 3]	Read HIGH to Data Valid	3		3		3		3		3		ns
t_{HZR}[2, 3]	Read HIGH to High Z		15		18		20		25		30	ns
t_{WC}	Write Cycle Time	30		35		40		50		80		ns
t_{PW}	Write Pulse Width	20		25		30		40		65		ns
t_{HWZ}[3]	Write HIGH to Low Z	10		10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		10		15		ns
t_{SD}	Data Set-Up Time	12		15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	30		35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	20		25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	20		25		30		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	20		25		30		40		65		ns
t_{RTC}	Retransmit Cycle Time	30		35		40		50		80		ns
t_{PRT}	Retransmit Pulse Width	20		25		30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		30		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		30		35		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		30		35		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		25		25		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		25		25		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		25		25		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		25		25		30		35		60	ns

Shaded area contains preliminary information.

Switching Characteristics Over the Operating Range[1, 4] (Continued)

Parameter	Description	7C420-20, 7C421-20 7C424-20, 7C425-20 7C428-20, 7C429-20		7C420-25, 7C421-25 7C424-25, 7C425-25 7C428-25, 7C429-25		7C420-30, 7C421-30 7C424-30, 7C425-30 7C428-30, 7C429-30		7C420-40, 7C421-40 7C424-40, 7C425-40 7C428-40, 7C429-40		7C420-65, 7C421-65 7C424-65, 7C425-65 7C428-65, 7C429-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WHF}	Write LOW to $\overline{HF}$ LOW		30		35		40		50		80	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		30		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		20		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{EF}$ HIGH	20		25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		20		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{FF}$ HIGH	20		25		30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		20		25		30		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		20		25		30		40		65	ns

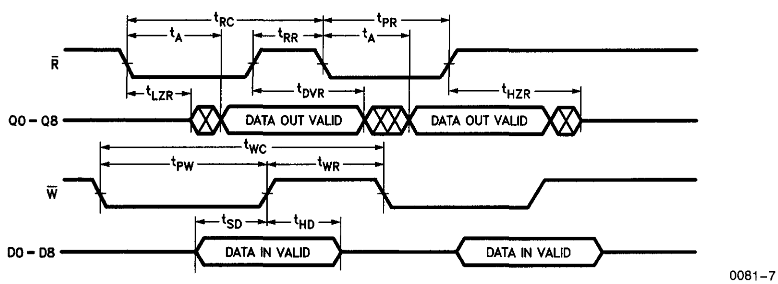
Shaded area contains preliminary information.

Notes:
1. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1a,* unless otherwise specified.
2. t_{HZR} and t_{DVR} use capacitance loading as in *Figure 1b.*
3. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ±100 mV from the steady state.
4. See the last page of this specification for Group A subgroup testing information.

5

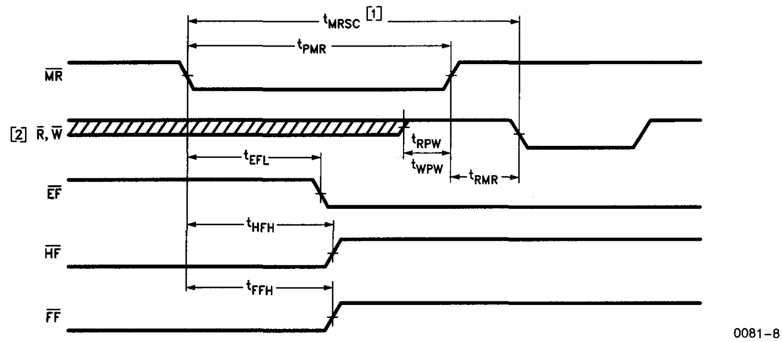
Switching Waveforms

Asynchronous Read and Write Timing Diagram



0081-7

Master Reset Timing Diagram

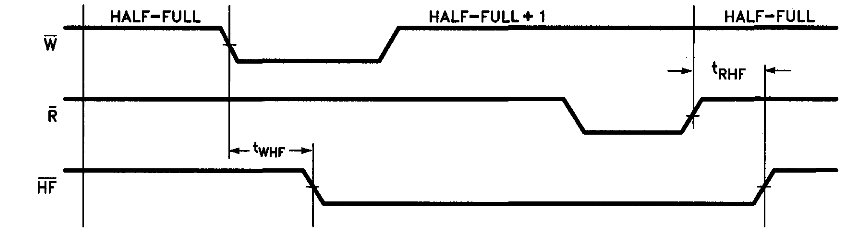


0081-8

Notes:
1. $t_{MRSC} = t_{PMR} + t_{RMR}$.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{MR}$.

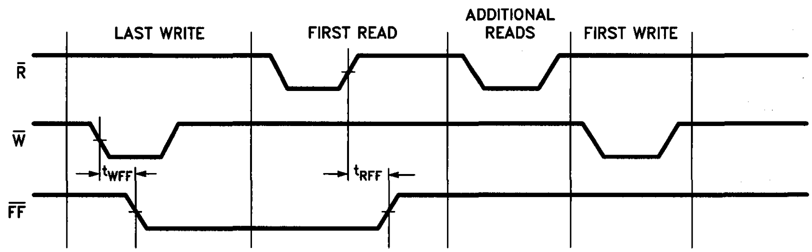
Switching Waveforms (Continued)

Half-Full Flag Timing Diagram



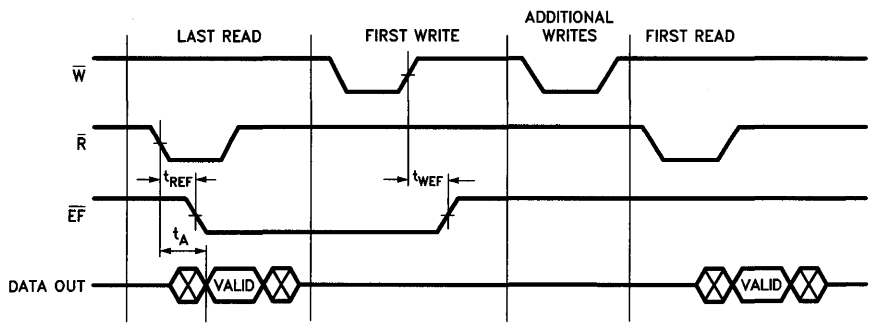
0081-9

Last WRITE to First READ Full Flag Timing Diagram



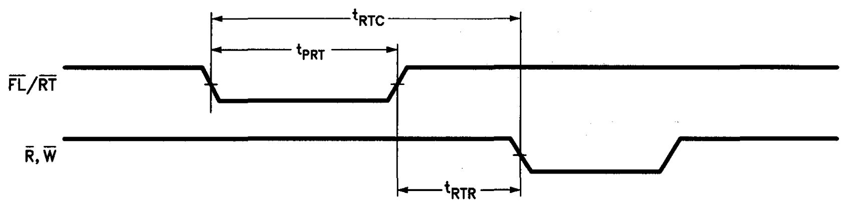
0081-10

Last READ to First WRITE Empty Flag Timing Diagram



0081-11

Retransmit Timing Diagram



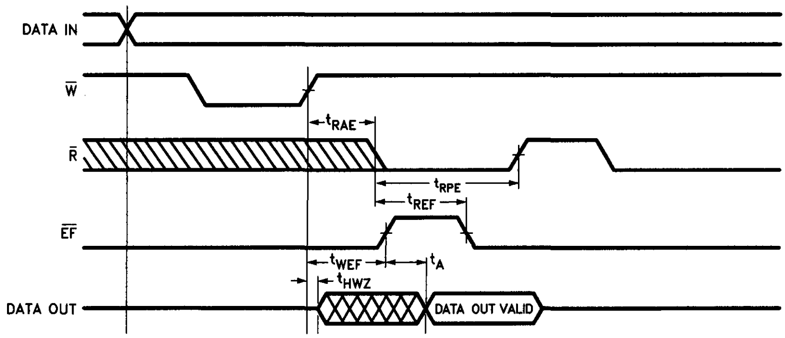
0081-12

Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

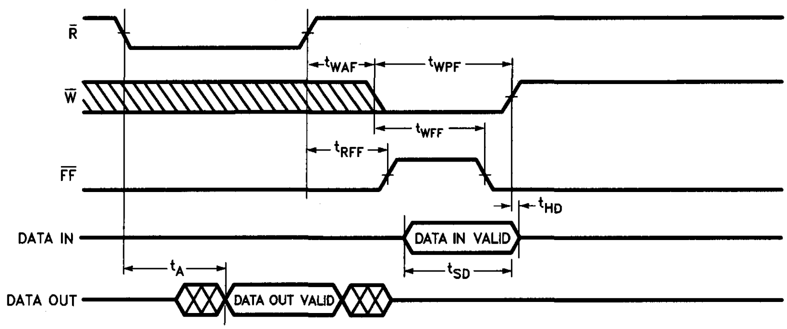
Switching Waveforms (Continued)

Empty Flag and Read Bubble-Through Mode Timing Diagram



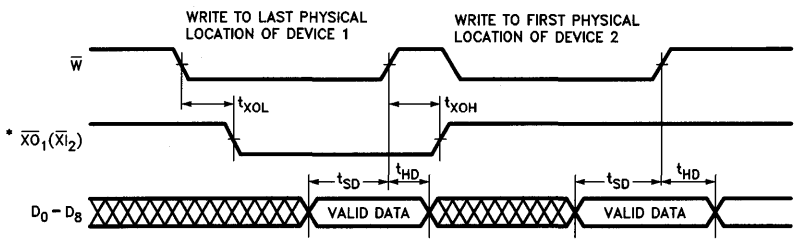
0081-13

Full Flag and Write Bubble-Through Mode Timing Diagram

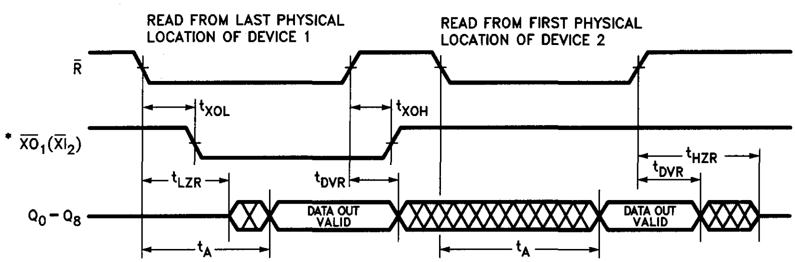


0081-14

Expansion Timing Diagrams



0081-15



0081-16

*Expansion Out of Device 1 ($\overline{XO}_1$) is connected to Expansion In of Device 2 ($\overline{XI}_2$).

Architecture

The CY7C420/421/424/425/428/429 FIFOs consist of an array of 512/1024/2048 words of 9-bits each (implemented by an array of dual port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$) and Full, Half Full, and Empty flags.

Dual Port RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half-Full ($\overline{HF}$) and Full flag ($\overline{FF}$) resetting to HIGH. Read ($\overline{R}$) and Write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle.

Writing Data to the FIFO

The availability of an empty location is indicated by the HIGH state of the Full flag ($\overline{FF}$). A falling edge of Write ($\overline{W}$) initiates a write cycle. Data appearing at the inputs (D0–D8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The Empty flag ($\overline{EF}$) LOW to HIGH transition occurs t_{WEF} after the first LOW to HIGH transition on the write clock of an empty FIFO. The Half-Full flag ($\overline{HF}$) will go LOW on the falling edge of the write clock following the occurrence of half full. $\overline{HF}$ will remain LOW while less than one half of the total memory of this device is available for writing. The LOW to HIGH transition of the $\overline{HF}$ flag occurs on the rising edge of Read ($\overline{R}$). $\overline{HF}$ is available in Single Device Mode only. The Full flag ($\overline{FF}$) goes low on the falling edge of $\overline{W}$ during the cycle in which the last available location in the FIFO is written, prohibiting overflow. $\overline{FF}$ goes HIGH t_{RFF} after the completion of a valid read of a full FIFO.

Reading Data from the FIFO

The falling edge of Read ($\overline{R}$) initiates a read cycle if the Empty flag ($\overline{EF}$) is not LOW. Data outputs (Q0–Q8) are in a high impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is in the Depth Expansion Mode but is not the active device.

The falling edge of $\overline{R}$ during the last read cycle before the empty condition triggers a HIGH to LOW transition of $\overline{EF}$, prohibiting any further read operations until t_{WEF} after a valid write.

Retransmit

The Retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be interrogated by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the Single Device Mode only. The Retransmit feature is intended for use when 512/1024/2048 (corresponding to device depth) or less writes have occurred since the previous $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. The write pointer is unaffected. $\overline{R}$ and $\overline{W}$ must both be HIGH during a retransmit cycle. Full, Half Full and Empty flags are governed by the relative locations of the Read and Write pointers and will be updated by a retransmit operation.

After a retransmit cycle, previously read data may be reaccessed using $\overline{R}$ to initiate standard read cycles beginning with the first physical location.

Single Device/Width Expansion Modes

Single Device and Width Expansion Modes are entered by grounding $\overline{XI}$. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFOs can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Depth Expansion Mode *(Figure 3)*

Depth Expansion Mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the Depth Expansion Mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in Depth Expansion Mode.

Architecture (Continued)

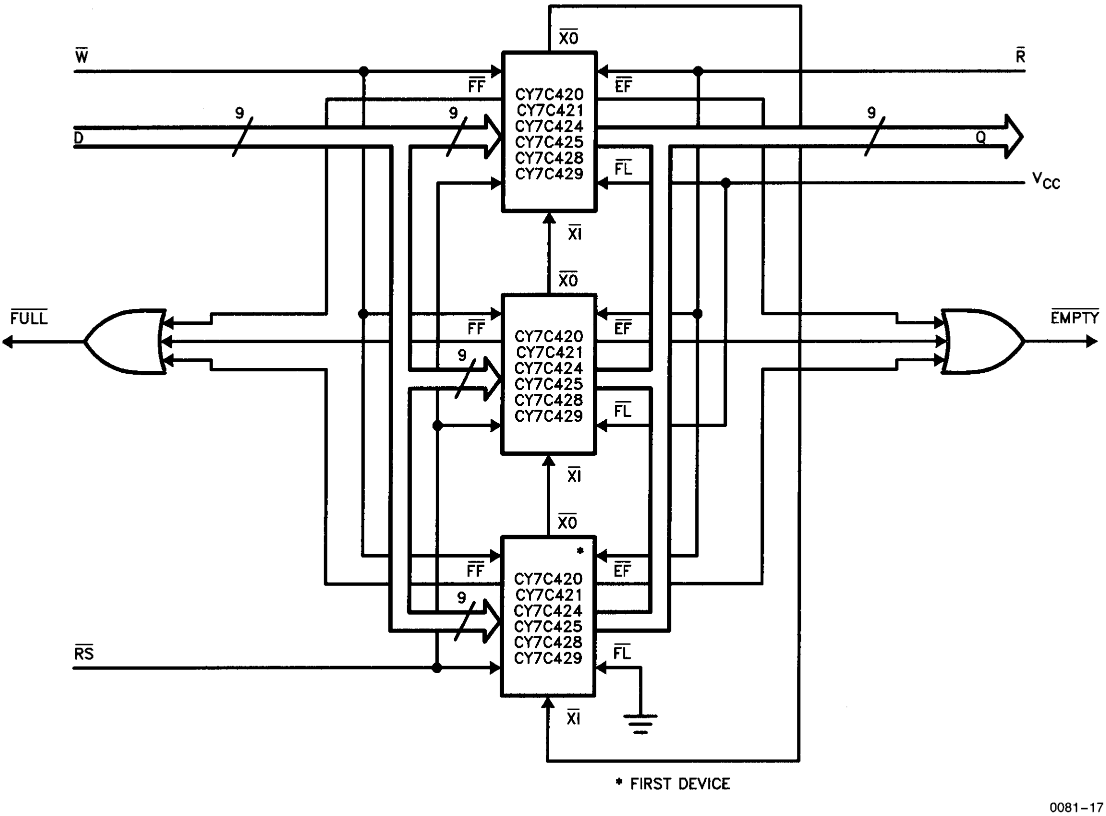
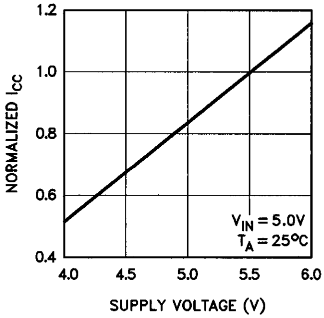


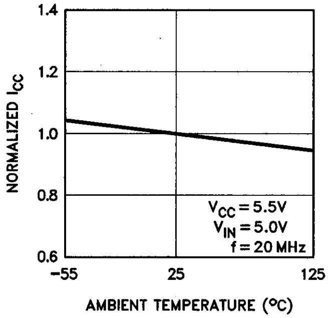
Figure 3. Depth Expansion

Typical DC and AC Characteristics

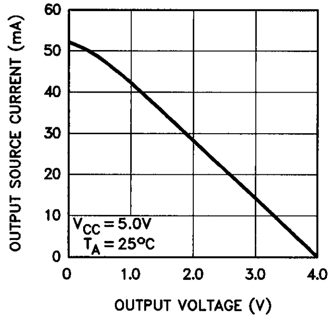
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



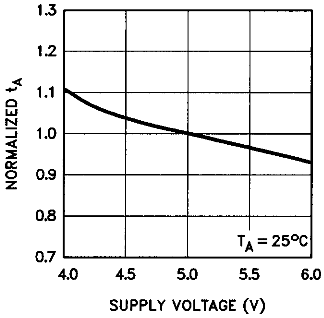
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



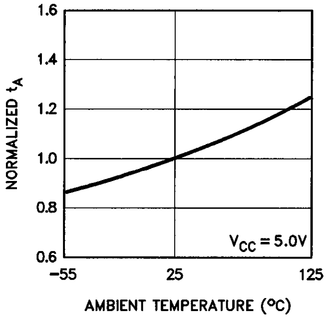
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



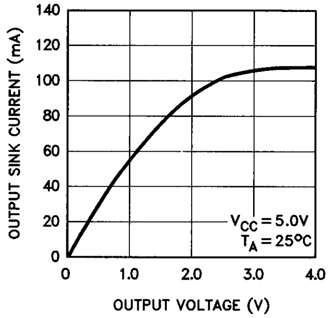
NORMALIZED t_A vs. SUPPLY VOLTAGE



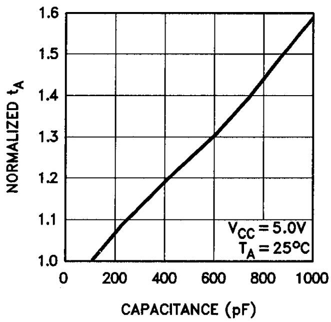
NORMALIZED t_A vs. AMBIENT TEMPERATURE



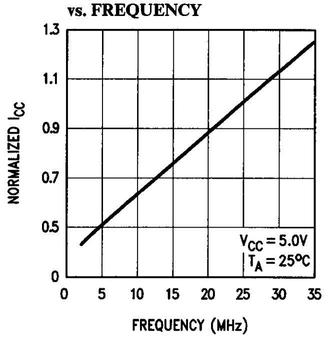
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



TYPICAL t_A CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0081–19

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C420-20PC	P15	Commercial
	CY7C420-20DC	D16	
25	CY7C420-25PC	P15	Commercial
	CY7C420-25DC	D16	
	CY7C420-25PI	P15	Industrial
	CY7C420-25DMB	D16	Military
30	CY7C420-30PC	P15	Commercial
	CY7C420-30DC	D16	
	CY7C420-30PI	P15	Industrial
	CY7C420-30DMB	D16	Military
40	CY7C420-40PC	P15	Commercial
	CY7C420-40DC	D16	
	CY7C420-40PI	P15	Industrial
	CY7C420-40DMB	D16	Military
65	CY7C420-65PC	P15	Commercial
	CY7C420-65DC	D16	
	CY7C420-65PI	P15	Industrial
	CY7C420-65DMB	D16	Military

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C421-20PC	P21	Commercial
	CY7C421-20JC	J65	
	CY7C421-20VC	V21	
	CY7C421-20DC	D22	
	CY7C421-20LC	L55	
25	CY7C421-25PC	P21	Commercial
	CY7C421-25JC	J65	
	CY7C421-25VC	V21	
	CY7C421-25DC	D22	
	CY7C421-25LC	L55	
	CY7C421-25PI	P21	Industrial
	CY7C421-25JI	J65	
	CY7C421-25DMB	D22	Military
	CY7C421-25LMB	L55	
	CY7C421-25KMB	K74	
30	CY7C421-30PC	P21	Commercial
	CY7C421-30JC	J65	
	CY7C421-30VC	V21	
	CY7C421-30DC	D22	
	CY7C421-30LC	L55	
	CY7C421-30PI	P21	Industrial
	CY7C421-30JI	J65	
	CY7C421-30DMB	D22	Military
	CY7C421-30LMB	L55	
	CY7C421-30KMB	K74	
40	CY7C421-40PC	P21	Commercial
	CY7C421-40JC	J65	
	CY7C421-40VC	V21	
	CY7C421-40DC	D22	
	CY7C421-40LC	L55	
	CY7C421-40PI	P21	Industrial
	CY7C421-40JI	J65	
	CY7C421-40DMB	D22	Military
	CY7C421-40LMB	L55	
	CY7C421-40KMB	K74	
65	CY7C421-65PC	P21	Commercial
	CY7C421-65JC	J65	
	CY7C421-65VC	V21	
	CY7C421-65DC	D22	
	CY7C421-65LC	L55	
	CY7C421-65PI	P21	Industrial
	CY7C421-65JI	J65	
	CY7C421-65DMB	D22	Military
	CY7C421-65LMB	L55	
	CY7C421-65KMB	K74	

Ordering Information (Continued)

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C424-20PC	P15	Commercial
	CY7C424-20DC	D16	
25	CY7C424-25PC	P15	Commercial
	CY7C424-25DC	D16	
	CY7C424-25PI	P15	Industrial
	CY7C424-25DMB	D16	Military
30	CY7C424-30PC	P15	Commercial
	CY7C424-30DC	D16	
	CY7C424-30PI	P15	Industrial
	CY7C424-30DMB	D16	Military
40	CY7C424-40PC	P15	Commercial
	CY7C424-40DC	D16	
	CY7C424-40PI	P15	Industrial
	CY7C424-40DMB	D16	Military
65	CY7C424-65PC	P15	Commercial
	CY7C424-65DC	D16	
	CY7C424-65PI	P15	Industrial
	CY7C424-65DMB	D16	Military

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C425-20PC	P21	Commercial
	CY7C425-20JC	J65	
	CY7C425-20DC	D22	
	CY7C425-20LC	L55	
	CY7C425-20VC	V21	
25	CY7C425-25PC	P21	Commercial
	CY7C425-25JC	J65	
	CY7C425-25DC	D22	
	CY7C425-25LC	L55	
	CY7C425-25VC	V21	
	CY7C425-25PI	P21	Industrial
	CY7C425-25JI	J65	
	CY7C425-25DMB	D22	Military
	CY7C425-25LMB	L55	
	CY7C425-25KMB	K74	
30	CY7C425-30PC	P21	Commercial
	CY7C425-30JC	J65	
	CY7C425-30DC	D22	
	CY7C425-30LC	L55	
	CY7C425-30VC	V21	
	CY7C425-30PI	P21	Industrial
	CY7C425-30JI	J65	
	CY7C425-30DMB	D22	Military
	CY7C425-30LMB	L55	
	CY7C425-30KMB	K74	
40	CY7C425-40PC	P21	Commercial
	CY7C425-40JC	J65	
	CY7C425-40DC	D22	
	CY7C425-40LC	L55	
	CY7C425-40VC	V21	
	CY7C425-40PI	P21	Industrial
	CY7C425-40JI	J65	
	CY7C425-40DMB	D22	Military
	CY7C425-40LMB	L55	
	CY7C425-40KMB	K74	
65	CY7C425-65PC	P21	Commercial
	CY7C425-65JC	J65	
	CY7C425-65DC	D22	
	CY7C425-65LC	L55	
	CY7C425-65VC	V21	
	CY7C425-65PI	P21	Industrial
	CY7C425-65JI	J65	
	CY7C425-65DMB	D22	Military
	CY7C425-65LMB	L55	
	CY7C425-65KMB	K74	

Ordering Information (Continued)

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C428-20PC	P15	Commercial
	CY7C428-20DC	D16	
25	CY7C428-25PC	P15	Commercial
	CY7C428-25DC	D16	
	CY7C428-25PI	P15	Industrial
	CY7C428-25DMB	D16	Military
30	CY7C428-30PC	P15	Commercial
	CY7C428-30DC	D16	
	CY7C428-30PI	P15	Industrial
	CY7C428-30DMB	D16	Military
40	CY7C428-40PC	P15	Commercial
	CY7C428-40DC	D16	
	CY7C428-40PI	P15	Industrial
	CY7C428-40DMB	D16	Military
65	CY7C428-65PC	P15	Commercial
	CY7C428-65DC	D16	
	CY7C428-65PI	P15	Industrial
	CY7C428-65DMB	D16	Military

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY7C429-20PC	P21	Commercial
	CY7C429-20JC	J65	
	CY7C429-20DC	D22	
	CY7C429-20LC	L55	
	CY7C429-20VC	V21	
25	CY7C429-25PC	P21	Commercial
	CY7C429-25JC	J65	
	CY7C429-25DC	D22	
	CY7C429-25LC	L55	
	CY7C429-25VC	V21	
	CY7C429-25PI	P21	Industrial
	CY7C429-25JI	J65	
	CY7C429-25DMB	D22	Military
	CY7C429-25LMB	L55	
	CY7C429-25KMB	K74	
30	CY7C429-30PC	P21	Commercial
	CY7C429-30JC	J65	
	CY7C429-30DC	D22	
	CY7C429-30LC	L55	
	CY7C429-30VC	V21	
	CY7C429-30PI	P21	Industrial
	CY7C429-30JI	J65	
	CY7C429-30DMB	D22	Military
	CY7C429-30LMB	L55	
	CY7C429-30KMB	K74	
40	CY7C429-40PC	P21	Commercial
	CY7C429-40JC	J65	
	CY7C429-40DC	D22	
	CY7C429-40LC	L55	
	CY7C429-40VC	V21	
	CY7C429-40PI	P21	Industrial
	CY7C429-40JI	J65	
	CY7C429-40DMB	D22	Military
	CY7C429-40LMB	L55	
	CY7C429-40KMB	K74	
65	CY7C429-65PC	P21	Commercial
	CY7C429-65JC	J65	
	CY7C429-65DC	D22	
	CY7C429-65LC	L55	
	CY7C429-65VC	V21	
	CY7C429-65PI	P21	Industrial
	CY7C429-65JI	J65	
	CY7C429-65DMB	D22	Military
	CY7C429-65LMB	L55	
	CY7C429-65KMB	K74	

5

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{CC}	1,2,3
I_{SB1}	1,2,3
I_{SB2}	1,2,3
I_{OS}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9,10,11
t_{A}	9,10,11
t_{RR}	9,10,11
t_{PR}	9,10,11
t_{LZR}	9,10,11
t_{DVR}	9,10,11
t_{HZR}	9,10,11
t_{WC}	9,10,11
t_{PW}	9,10,11
t_{HWZ}	9,10,11
t_{WR}	9,10,11
t_{SD}	9,10,11
t_{HD}	9,10,11
t_{MRSC}	9,10,11
t_{PMR}	9,10,11
t_{RMR}	9,10,11
t_{RPW}	9,10,11
t_{WPW}	9,10,11
t_{RTC}	9,10,11
t_{PRT}	9,10,11
t_{RTR}	9,10,11
t_{EFL}	9,10,11
t_{HFH}	9,10,11
t_{FFH}	9,10,11

Parameters	Subgroups
t_{REF}	9,10,11
t_{RFF}	9,10,11
t_{WEF}	9,10,11
t_{WFF}	9,10,11
t_{WHF}	9,10,11
t_{RHF}	9,10,11
t_{RAE}	9,10,11
t_{RPE}	9,10,11
t_{WAF}	9,10,11
t_{WPF}	9,10,11
t_{XOL}	9,10,11
t_{XOH}	9,10,11

Document #: 38-00079-F

CYPRESS SEMICONDUCTOR

PRELIMINARY

CY7C432 CY7C433

Cascadeable 4096 x 9 FIFO

Features

- **4096 x 9 FIFO buffer memory**
- **Dual port RAM cell**
- **Asynchronous read/write**
- **High speed 28.5 MHz read/write independent of depth/width**
- **25 ns access time**
- **Low operating power**
  I_{CC} (max.) = 142 mA commercial
  I_{CC} (max.) = 160 mA military
- **Half full flag in standalone**
- **Empty and full flags**
- **Retransmit in standalone**
- **Expandable in width and depth**
- **Parallel Cascade minimizes bubblethrough**
- **5V ±10% supply**
- **300 mil DIP packaging**
- **300 mil SOJ packaging**
- **TTL compatible**
- **Three-state outputs**
- **Pin compatible and functional equivalent to IDT7204**

Functional Description

The CY7C432 and CY7C433 are 4096 words by 9-bit wide first-in first-out (FIFO) memories offered in 600 mil wide and 300 mil wide packages, respectively. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 28.5 MHz. The write operation occurs when the Write ($\overline{\text{W}}$) signal is LOW. Read occurs when Read ($\overline{\text{R}}$) goes LOW. The 9 data outputs go to the high impedance state when $\overline{\text{R}}$ is HIGH.

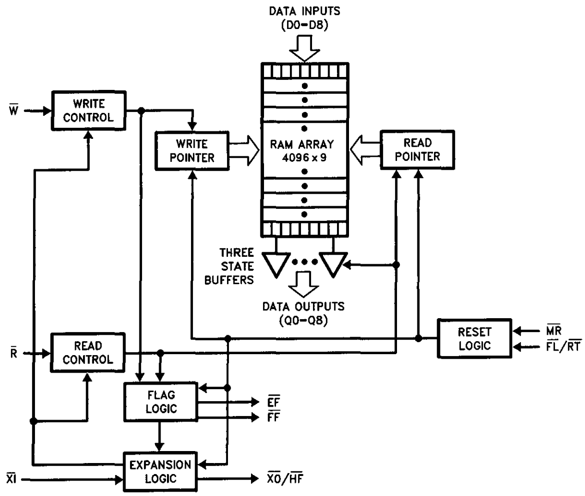
A Half-Full ($\overline{\text{HF}}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration this pin provides the expansion out ($\overline{\text{XO}}$) information which is used to tell the next FIFO that it will be activated.

In the standalone and width expansion configurations a LOW on the Retransmit ($\overline{\text{RT}}$) input causes the FIFO's to retransmit the data. Read Enable ($\overline{\text{R}}$) and Write Enable ($\overline{\text{W}}$) must both be HIGH during a retransmit cycle, and then $\overline{\text{R}}$ is used to access the data.

The CY7C432 and CY7C433 are fabricated using an advanced 0.8 micron N-well CMOS technology. Input ESD protection is greater than 2000V and latchup is prevented by careful layout, guard rings and a substrate bias generator.

5

Logic Block Diagram



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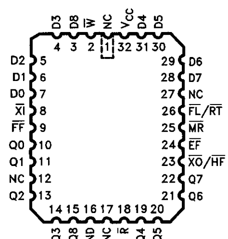
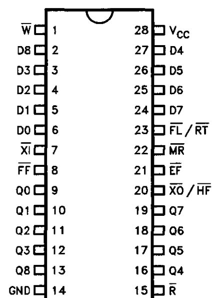
Pin Configurations

PLCC/LCC Top View



0169-2

DIP Top View



0169-3

Selection Guide

		7C432-25 7C433-25	7C432-30 7C433-30	7C432-40 7C433-40	7C432-65 7C433-65
Frequency (MHz)		28.5	25	20	12.5
Access Time (ns)		25	30	40	65
Maximum Operating Current (mA)	Commercial	142	135	125	110
	Military		160	145	130

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015)

Latch-up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[4]

Parameters	Description	Test Conditions		7C432-25 7C433-25 Min.	Max.	7C432-30 7C433-30 Min.	Max.	7C432-40 7C433-40 Min.	Max.	7C432-65 7C433-65 Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}[7]	Input HIGH Voltage		Commercial	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
			Military/Ind			2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial[5]		142		135		125		110	mA
			Military[6]/Ind				160		145		130	mA
I_{SB1}	Standby Current	All Inputs = V_{IH} Min.	Commercial		25		25		25		25	mA
			Military/Ind				30		30		30	mA
I_{SB2}	Power Down Current	All Inputs V_{CC} −0.2V	Commercial		20		20		20		20	mA
			Military/Ind				25		25		25	mA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND			−90		−90		−90		−90	mA

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:

1. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. I_{CC} (commercial) = 110 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
6. I_{CC} (military) = 130 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
7. $\overline{XI}$ must use CMOS levels with V_{IH} ≥ 3.5V.

AC Test Load and Waveform

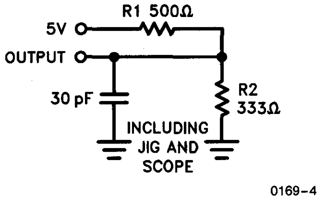


Figure 1a

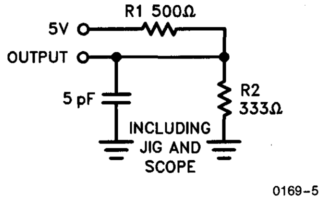


Figure 1b

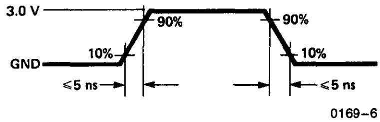
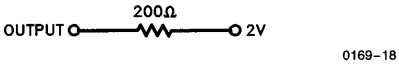


Figure 2. All Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[1, 4]

Parameter	Description	7C432-25 7C433-25		7C432-30 7C433-30		7C432-40 7C433-40		7C432-65 7C433-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	35		40		50		80		ns
t_{A}	Access Time		25		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		10		15		ns
t_{PR}	Read Pulse Width	25		30		40		65		ns
t_{LZR}[3]	Read LOW to Low Z	3		3		3		3		ns
t_{DVR}[2, 3]	Read HIGH to Data Valid	3		3		3		3		ns
t_{HZR}[2, 3]	Read HIGH to High Z		18		20		25		30	ns
t_{WC}	Write Cycle Time	35		40		50		80		ns
t_{PW}	Write Pulse Width	25		30		40		65		ns
t_{HWZ}[3]	Write HIGH to Low Z	10		10		10		10		ns
t_{WR}	Write Recovery Time	10		10		10		15		ns
t_{SD}	Data Set-Up Time	15		18		20		30		ns
t_{HD}	Data Hold Time	0		0		0		10		ns
t_{MRSC}	$\overline{MR}$ Cycle Time	35		40		50		80		ns
t_{PMR}	$\overline{MR}$ Pulse Width	25		30		40		65		ns
t_{RMR}	$\overline{MR}$ Recovery Time	10		10		10		15		ns
t_{RPW}	Read HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{WPW}	Write HIGH to $\overline{MR}$ HIGH	25		30		40		65		ns
t_{RTC}	Retransmit Cycle Time	35		40		50		80		ns
t_{PRT}	Retransmit Pulse Width	25		30		40		65		ns
t_{RTR}	Retransmit Recovery Time	10		10		10		15		ns
t_{EFL}	$\overline{MR}$ to $\overline{EF}$ LOW		35		40		50		80	ns
t_{HFH}	$\overline{MR}$ to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{FFH}	$\overline{MR}$ to $\overline{FF}$ HIGH		35		40		50		80	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW		25		30		35		60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH		25		30		35		60	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH		25		30		35		60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW		25		30		35		60	ns

5

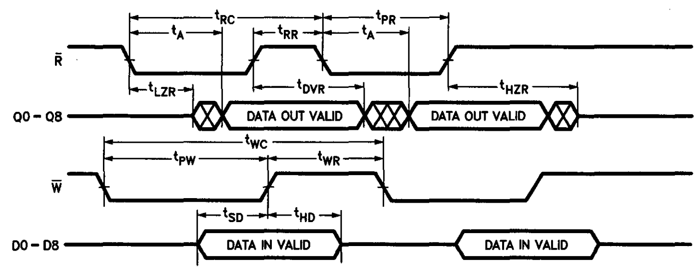
Switching Characteristics Over the Operating Range[1, 4] (Continued)

Parameter	Description	7C432-25 7C433-25		7C432-30 7C433-30		7C432-40 7C433-40		7C432-65 7C433-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{WHF}	Write LOW to $\overline{HF}$ LOW		35		40		50		80	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH		35		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		25		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{EF}$ HIGH	25		30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		25		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{FF}$ HIGH	25		30		40		65		ns
t_{XOL}	Expansion Out LOW Delay from Clock		25		30		40		65	ns
t_{XOH}	Expansion Out HIGH Delay from Clock		25		30		40		65	ns

Notes:
1. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1a,* unless otherwise specified.
2. t_{HZR} and t_{DVR} use capacitance loading as in *Figure 1b.*
3. t_{HZR} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} transition is measured at the 1.5V level. t_{HWZ} and t_{LZR} transition is measured at ± 100 mV from the steady state.
4. See the last page of this specification for Group A subgroup testing information.

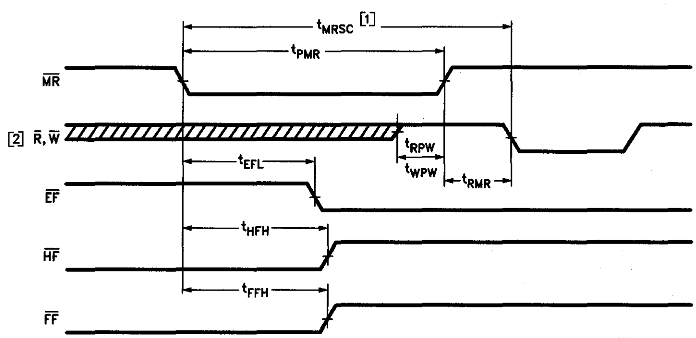
Switching Waveforms

Asynchronous Read and Write Timing Diagram



0169-7

Master Reset Timing Diagram

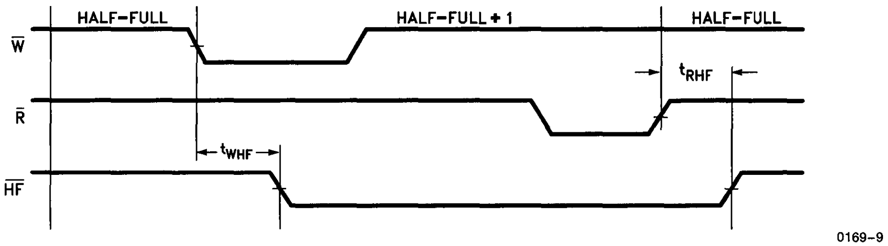


0169-8

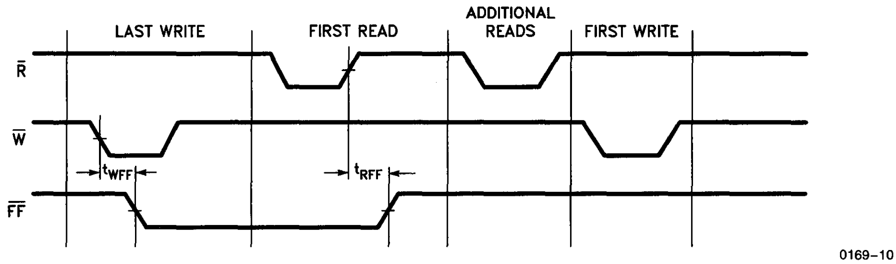
Notes:
1. $t_{MRSC} = t_{PMR} + t_{RMR}$.
2. $\overline{W}$ and $\overline{R} \geq V_{IH}$ for at least t_{WPW} or t_{RPR} before the rising edge of $\overline{MR}$.

Switching Waveforms (Continued)

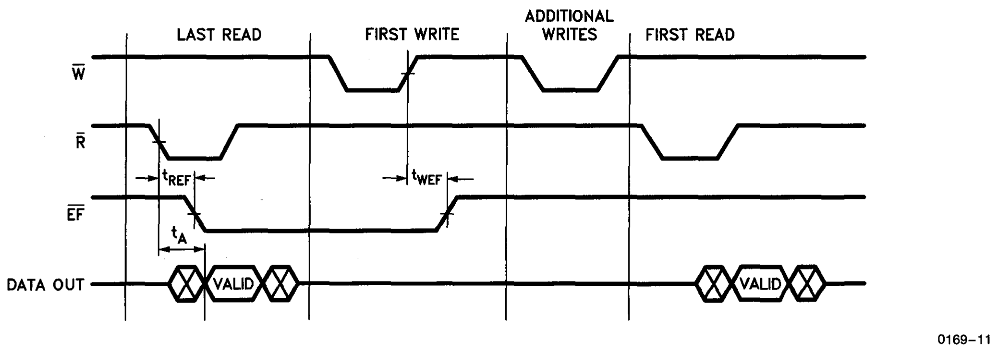
Half-Full Flag Timing Diagram



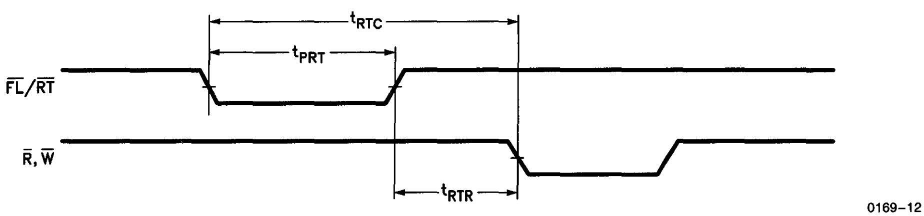
Last WRITE to First READ Full Flag Timing Diagram



Last READ to First WRITE Empty Flag Timing Diagram



Retransmit Timing Diagram



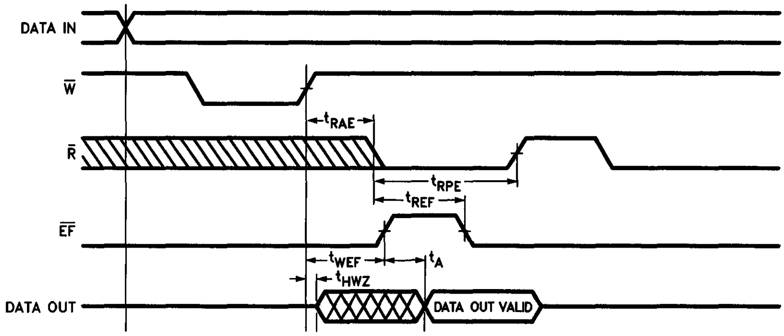
Notes:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

5

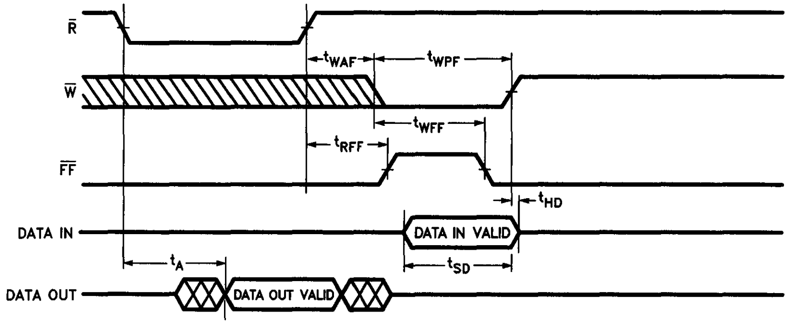
Switching Waveforms (Continued)

Empty Flag and Read Bubble-Through Mode Timing Diagram



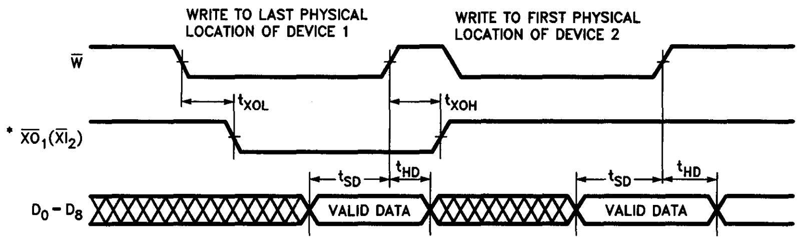
0169–13

Full Flag and Write Bubble-Through Mode Timing Diagram

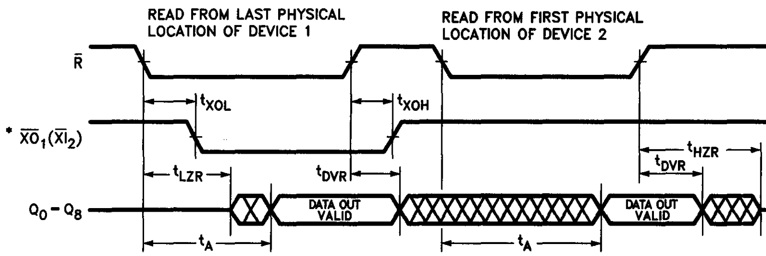


0169–14

Expansion Timing Diagrams



0169–15



0169–16

*Expansion Out of Device 1 ($\overline{XO}_1$) is connected to Expansion In of Device 2 ($\overline{XI}_2$).

Architecture

The CY7C432/33 FIFOs consist of an array of 4096 words of 9-bits each (implemented by an array of dual port RAM cells), a read pointer, a write pointer, control signals ($\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{XO}$, $\overline{FL}$, $\overline{RT}$, $\overline{MR}$) and Full, Half Full, and Empty flags.

Dual Port RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional register array architecture.

Resetting the FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half-Full ($\overline{HF}$) and Full flag ($\overline{FF}$) resetting to HIGH. Read ($\overline{R}$) and Write ($\overline{W}$) must be HIGH t_{RPW}/t_{WPW} before and t_{RMR} after the rising edge of $\overline{MR}$ for a valid reset cycle.

Writing Data to the FIFO

The availability of an empty location is indicated by the HIGH state of the Full flag ($\overline{FF}$). A falling edge of Write ($\overline{W}$) initiates a write cycle. Data appearing at the inputs (D0–D8) t_{SD} before and t_{HD} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The Empty flag ($\overline{EF}$) LOW to HIGH transition occurs t_{WEF} after the first LOW to HIGH transition on the write clock of an empty FIFO. The Half-Full flag ($\overline{HF}$) will go LOW on the falling edge of the write clock following the occurrence of half full. $\overline{HF}$ will remain LOW while less than one half of the total memory of this device is available for writing. The LOW to HIGH transition of the $\overline{HF}$ flag occurs on the rising edge of Read ($\overline{R}$). $\overline{HF}$ is available in Single Device Mode only. The Full flag ($\overline{FF}$) goes low on the falling edge of $\overline{W}$ during the cycle in which the last available location in the FIFO is written, prohibiting overflow. $\overline{FF}$ goes HIGH t_{RFF} after the completion of a valid read of a full FIFO.

Reading Data from the FIFO

The falling edge of Read ($\overline{R}$) initiates a read cycle if the Empty flag ($\overline{EF}$) is not LOW. Data outputs (Q0–Q8) are in a high impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is in the Depth Expansion Mode but is not the active device.

The falling edge of $\overline{R}$ during the last read cycle before the empty condition triggers a HIGH to LOW transition of $\overline{EF}$, prohibiting any further read operations until t_{WEF} after a valid write.

Retransmit

The Retransmit feature is beneficial when transferring packets of data. It enables the receipt of data to be interrogated by the receiver and retransmitted if necessary.

The Retransmit ($\overline{RT}$) input is active in the Single Device Mode only. The Retransmit feature is intended for use when 4096 or less writes have occurred since the previous $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. The write pointer is unaffected. $\overline{R}$ and $\overline{W}$ must both be HIGH during a retransmit cycle. Full, Half Full and Empty flags are governed by the relative locations of the Read and Write pointers and will be updated by a retransmit operation.

After a retransmit cycle, previously read data may be reaccessed using $\overline{R}$ to initiate standard read cycles beginning with the first physical location.

Single Device/Width Expansion Modes

Single Device and Width Expansion Modes are entered by connecting $\overline{XI}$ to ground prior to an $\overline{MR}$ cycle. During these modes the $\overline{HF}$ and $\overline{RT}$ features are available. FIFOs can be expanded in width to provide word widths greater than 9 in increments of 9. During Width Expansion Mode all control line inputs are common to all devices and flag outputs from any device can be monitored.

Depth Expansion Mode *(Figure 3)*

Depth Expansion Mode is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the Depth Expansion Mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and is pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one is enabled for write at any given time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by OR-ing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by OR-ing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in Depth Expansion Mode.

Architecture (Continued)

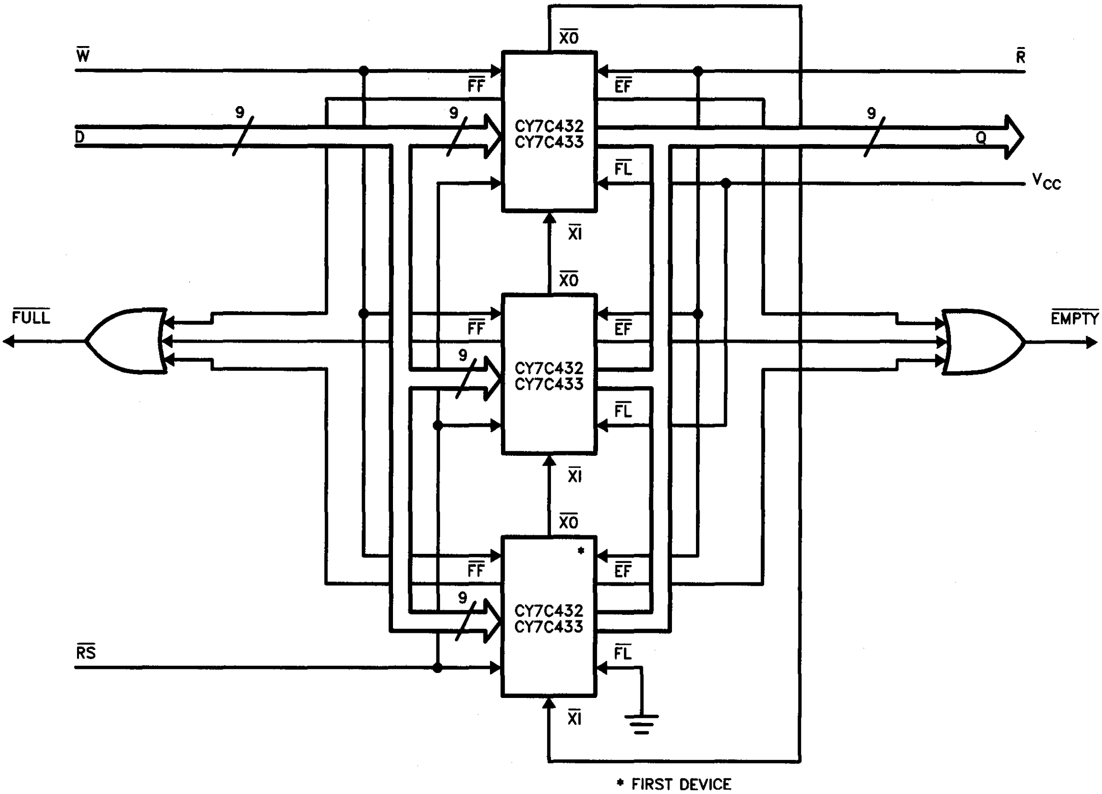


Figure 3. Depth Expansion

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C432-25PC	P15	Commercial
	CY7C432-25DC	D16	
	CY7C432-25PI	P15	Industrial
30	CY7C432-30PC	P15	Commercial
	CY7C432-30DC	D16	
	CY7C432-30PI	P15	Industrial
	CY7C432-30DMB	D16	Military
40	CY7C432-40PC	P15	Commercial
	CY7C432-40DC	D16	
	CY7C432-40PI	P15	Industrial
	CY7C432-40DMB	D16	Military
65	CY7C432-65PC	P15	Commercial
	CY7C432-65DC	D16	
	CY7C432-65PI	P15	Industrial
	CY7C432-65DMB	D16	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C433-25PC	P21	Commercial
	CY7C433-25VC	V21	
	CY7C433-25DC	D22	
	CY7C433-25LC	L55	
	CY7C433-25JC	J65	
	CY7C433-25PI	P21	Industrial
	CY7C433-25JI	J65	
30	CY7C433-30PC	P21	Commercial
	CY7C433-30VC	V21	
	CY7C433-30DC	D22	
	CY7C433-30LC	L55	
	CY7C433-30JC	J65	
	CY7C433-30PI	P21	Industrial
	CY7C433-30JI	J65	
	CY7C433-30DMB	D22	Military
	CY7C433-30LMB	L55	
	CY7C433-30KMB	K74	
40	CY7C433-40PC	P21	Commercial
	CY7C433-40VC	V21	
	CY7C433-40DC	D22	
	CY7C433-40LC	L55	
	CY7C433-40JC	J65	
	CY7C433-40PI	P21	Industrial
	CY7C433-40JI	J65	
	CY7C433-40DMB	D22	Military
	CY7C433-40LMB	L55	
	CY7C433-40KMB	K74	
65	CY7C433-65PC	P21	Commercial
	CY7C433-65VC	V21	
	CY7C433-65DC	D22	
	CY7C433-65LC	L55	
	CY7C433-65JC	J65	
	CY7C433-65PI	P21	Industrial
	CY7C433-65JI	J65	
	CY7C433-65DMB	D22	Military
	CY7C433-65LMB	L55	
	CY7C433-65KMB	K74	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{CC}	1,2,3
I_{SB1}	1,2,3
I_{SB2}	1,2,3
I_{OS}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9,10,11
t_{A}	9,10,11
t_{RR}	9,10,11
t_{PR}	9,10,11
t_{LZR}	9,10,11
t_{DVR}	9,10,11
t_{HZR}	9,10,11
t_{WC}	9,10,11
t_{PW}	9,10,11
t_{HWZ}	9,10,11
t_{WR}	9,10,11
t_{SD}	9,10,11
t_{HD}	9,10,11
t_{MRSC}	9,10,11
t_{PMR}	9,10,11
t_{RMR}	9,10,11
t_{RPW}	9,10,11
t_{WPW}	9,10,11
t_{RTC}	9,10,11
t_{PRT}	9,10,11
t_{RTR}	9,10,11
t_{EFL}	9,10,11
t_{HFH}	9,10,11
t_{FFH}	9,10,11

Parameters	Subgroups
t_{REF}	9,10,11
t_{RFF}	9,10,11
t_{WEF}	9,10,11
t_{WFF}	9,10,11
t_{WHF}	9,10,11
t_{RHF}	9,10,11
t_{RAE}	9,10,11
t_{RPE}	9,10,11
t_{WAF}	9,10,11
t_{WPF}	9,10,11
t_{XOL}	9,10,11
t_{XOH}	9,10,11

Document #: 38-00109

CYPRESS SEMICONDUCTOR

Bidirectional 2048 x 9 FIFO

Features

- **2048 x 9 FIFO buffer memory**
- **Bidirectional operation**
- **High-speed 25-MHz asynchronous reads and writes**
- **Simple control interface**
- **Registered and transparent bypass modes**
- **Flags indicate empty, full and half full conditions**
- **5V ±10% supply**
- **Available in 300-mil DIP, PLCC, LCC, and SOJ packages**
- **TTL compatible**

Functional Description

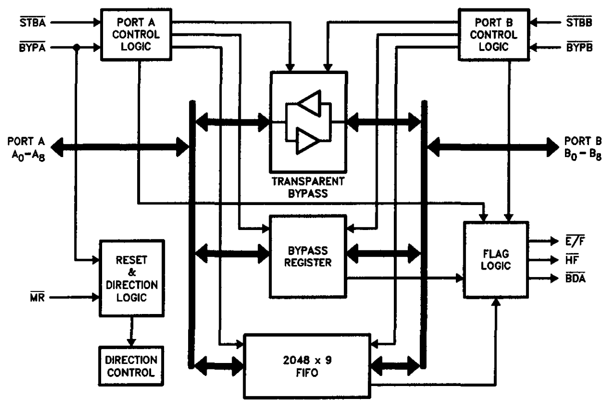
The CY7C439 is a 2048 x 9 FIFO memory capable of bidirectional operation. As the term first-in first-out (FIFO) implies, data becomes available to the output port in the same order that it was presented to the input port. There are two pins that indicate the amount of data contained within the FIFO block—$\overline{E/F}$ (empty/full) and $\overline{HF}$ (half full). These pins can be decoded to determine one of four states. Two 9-bit data ports are provided. The direction selected for the FIFO determines the input and output ports. The FIFO direction can be programmed by the user at any time through the use of the reset pin ($\overline{MR}$) and the bypass/direction pin ($\overline{BYPA}$). There are no control or status registers on the CY7C439, making the part simple to use while meeting the needs of the majority of bidirectional FIFO applications.

FIFO read and write operations may occur simultaneously, and each can occur at up to 25 MHz. The port designated as the write port drives its strobe pin ($\overline{STBX}$, X = A or B) LOW to initiate the write operation. The port designated as the read port drives its strobe pin LOW to initiate the read operation. Output port pins go to a high-impedance state when the associated strobe pin is HIGH. All normal FIFO operations require the bypass control pin ($\overline{BYPX}$, X = A or B) to remain HIGH.

In addition to the FIFO, two other data paths are provided on the CY7C439; registered bypass and transparent bypass. Registered bypass can be considered as a single-word FIFO in the reverse direction to the main FIFO. The bypass register provides a means of sending a 9-bit status or control word to the FIFO-write port. The bypass

5

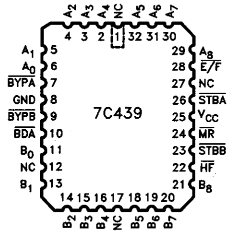
Logic Block Diagram



0178–1

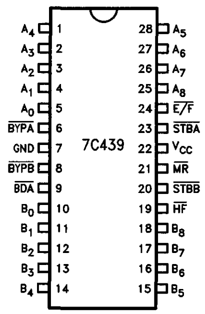
Pin Configurations

PLCC/LCC Top View



0178–2

DIP Top View



0178–3

Selection Guide

		7C439-30	7C439-40	7C439-65
Frequency (MHz)		25	20	12.5
Access Time (ns)		30	40	65
Maximum Operating Current (mA)	Commercial	145	130	115
	Military	—	165	145

Functional Description (Continued)

data available pin ($\overline{BDA}$) indicates whether the bypass register is full or empty. The direction of the bypass register is always opposite to that of the main FIFO.

The port designated to write to the bypass register drives its bypass control pin ($\overline{BYPX}$) LOW. The other port detects the presence of data by monitoring $\overline{BDA}$, and reads the data by driving its bypass control pin ($\overline{BYPX}$) LOW. Registered bypass operations require that the associated FIFO strobe pin ($\overline{STBX}$) remains HIGH. Registered bypass operations do not affect data residing in the FIFO, or FIFO operations at the other port.

Transparent bypass provides a means of transferring a single word (9 bits) of data immediately in either direction. This feature allows the device to act as a simple 9-bit bidirectional buffer. This is useful for allowing the controlling circuitry to access a dumb peripheral for control/programming information.

For transparent bypass, the port wishing to send immediate data to the other side side drives both its bypass and its strobe pins LOW simultaneously. This causes the buffered data to be driven out of the other port. On-chip circuitry detects conflicting use of the control pins and causes both data ports to enter a high-impedance state until the conflict is resolved.

The CY7C439 is fabricated using an advanced 0.8μ N-well CMOS technology. Input ESD protection is greater than 2000V, and latch-up is prevented by reliable layout techniques, guard rings, and a substrate bias generator.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Power Dissipation 1.0W

Output Current, into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Pin Definitions

Signal Name	I/O	Description
$A_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPA}$ and $\overline{STBA}$
$B_{(8-0)}$	I/O	Data Port Associated with $\overline{BYPB}$ and $\overline{STBB}$
$\overline{BYPA}$	I	Registered Bypass Mode Select for A Side
$\overline{BYPB}$	I	Registered Bypass Mode Select for B Side
$\overline{BDA}$	O	Bypass Data Available Flag
$\overline{STBA}$	I	Data Strobe for A Side
$\overline{STBB}$	I	Data Strobe for B Side
$\overline{E/F}$	O	Encoded Empty/Full Flag
$\overline{HF}$	O	Half Full Flag
$\overline{MR}$	I	Master Reset

Electrical Characteristics Over Operating Range[2]

Parameters	Description	Test Conditions		7C439-30 Min.	7C439-30 Max.	7C439-40 Min.	7C439-40 Max.	7C439-65 Min.	7C439-65 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage		Commercial	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
			Military	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	−3.0	0.8	−3.0	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	$\overline{STBX}$ ≥ V_{IH}, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial[5]		145		130		115	mA
			Military[6]				165		145	mA
I_{SB_1}	Standby Current	All Inputs = V_{IH} Min.	Commercial		40		40		40	mA
			Military		45		45			mA
I_{SB_2}	Power Down Current	All Inputs V_{CC} −0.2V	Commercial		20		20		20	mA
			Military				25		25	mA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−90		−90		−90	mA

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{CC} = 4.5V	7	

Notes:
1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.
5. I_{CC} (commercial) = 100 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.
6. I_{CC} (military) = 115 mA + [($\bar{f}$ − 12.5) * 2 mA/MHz] for $\bar{f}$ ≥ 12.5 MHz
   where $\bar{f}$ = the larger of the write or read operating frequency.

AC Test Load and Waveform

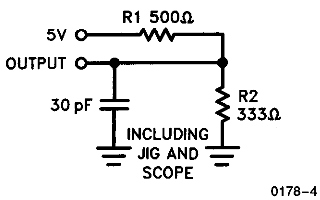


Figure 1a

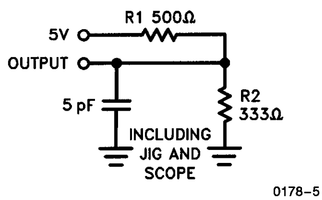


Figure 1b

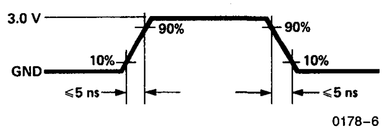
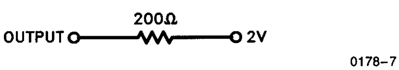


Figure 2. All Input Pulses

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[7, 10]

Parameter	Description	7C439-30		7C439-40		7C439-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	40		50		80		ns
t_{A}	Access Time		30		40		65	ns
t_{RR}	Read Recovery Time	10		10		15		ns
t_{PR}	Read Pulse Width	30		40		65		ns
t_{LZR}[8, 9]	Read LOW to Low Z	3		3		3		ns
t_{DVR}[8, 9]	Read HIGH to Data Valid	3		3		3		ns
t_{HZR}[8, 9]	Read HIGH to High Z		20		25		30	ns
t_{WC}	Write Cycle Time	40		50		80		ns
t_{PW}	Write Pulse Width	30		40		65		ns
t_{HWZ}[8, 9]	Write HIGH to Low Z	10		10		10		ns
t_{WR}	Write Recovery Time	10		10		15		ns
t_{SD}	Data Set-Up Time	18		20		30		ns
t_{HD}	Data Hold Time	0		0		10		ns
t_{MRSC}	$\overline{\text{MR}}$ Cycle Time	40		50		80		ns
t_{PMR}	$\overline{\text{MR}}$ Pulse Width	30		40		65		ns
t_{RMR}	$\overline{\text{MR}}$ Recovery Time	10		10		15		ns
t_{RPS}	$\overline{\text{STBX}}$ HIGH to $\overline{\text{MR}}$ HIGH	30		40		65		ns
t_{RPBS}	$\overline{\text{BYPA}}$ to $\overline{\text{MR}}$ HIGH	10		15		20		ns
t_{RPBH}	$\overline{\text{BYPA}}$ Hold after $\overline{\text{MR}}$ HIGH	0		0		0		ns
t_{BDH}	$\overline{\text{MR}}$ LOW to $\overline{\text{BDA}}$ HIGH		40		50		80	ns
t_{BSR}	$\overline{\text{STBX}}$ HIGH to $\overline{\text{BYPX}}$ LOW	10		10		15		ns
t_{EFL}	$\overline{\text{MR}}$ to $\overline{\text{E/F}}$ LOW		40		50		80	ns
t_{HFH}	$\overline{\text{MR}}$ to $\overline{\text{HF}}$ HIGH		40		50		80	ns
t_{BRS}	$\overline{\text{BYPX}}$ HIGH to $\overline{\text{STBX}}$ LOW	10		10		15		ns
t_{REF}	$\overline{\text{STBX}}$ LOW to $\overline{\text{E/F}}$ LOW (Read)		30		35		60	ns
t_{RFF}	$\overline{\text{STBX}}$ HIGH to $\overline{\text{E/F}}$ HIGH (Read)		30		35		60	ns
t_{WEF}	$\overline{\text{STBX}}$ HIGH to $\overline{\text{E/F}}$ HIGH (Write)		30		35		60	ns
t_{WFF}	$\overline{\text{STBX}}$ LOW to $\overline{\text{E/F}}$ LOW (Write)		30		35		60	ns

Switching Characteristics Over the Operating Range[7, 10] (Continued)

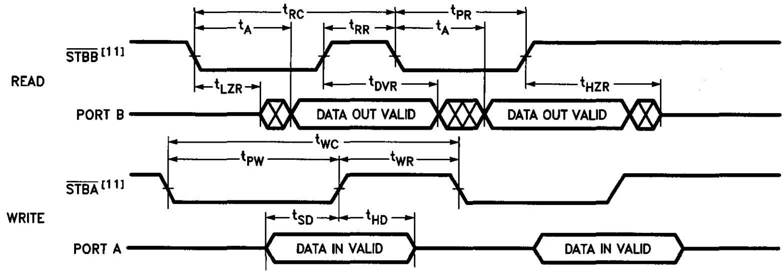
Parameter	Description	7C439-30		7C439-40		7C439-65		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{BDA}	$\overline{\text{BYPX}}$ HIGH to $\overline{\text{BDA}}$ LOW (Write)		30		35		60	ns
t_{BDB}	$\overline{\text{BYPX}}$ HIGH to $\overline{\text{BDA}}$ HIGH (Read)		30		35		60	ns
t_{BA}	$\overline{\text{BYPX}}$ LOW to Data Valid (Read)		30		40		60	ns
t_{BHZ}[8, 9]	$\overline{\text{BYPX}}$ HIGH to High Z (Read)		20		25		30	ns
t_{TSB}	$\overline{\text{STBX}}$ HIGH to $\overline{\text{BYPX}}$ LOW Set-Up	10		10		15		ns
t_{TBS}	$\overline{\text{STBX}}$ LOW after $\overline{\text{BYPX}}$ LOW	0	5	0	10	0	15	ns
t_{TSN}	$\overline{\text{STBX}}$ HIGH Recovery Time	10		10		15		ns
t_{TSD}[8, 9]	$\overline{\text{STBX}}$ HIGH to Data High Z		20		25		30	ns
t_{TBN}	$\overline{\text{BYPX}}$ HIGH Recovery Time	10		10		15		ns
t_{TBD}[8, 9]	$\overline{\text{BYPX}}$ HIGH to Data High Z		20		25		30	ns
t_{TPD}	$\overline{\text{STBX}}$ LOW to Data Valid		25		35		50	ns
t_{DL}	Transparent Propagation Delay		20		25		30	ns
t_{ESD}[8, 9]	$\overline{\text{STBX}}$ LOW to High Z		20		25		30	ns
t_{EBD}[8, 9]	$\overline{\text{BYPX}}$ LOW to High Z		20		25		30	ns
t_{EDS}	$\overline{\text{STBX}}$ HIGH to Low Z		20		25		30	ns
t_{EDB}	$\overline{\text{BYPX}}$ HIGH to Low Z		20		25		30	ns
t_{BPW}	$\overline{\text{BYPX}}$ Pulse Width (Trans.)	30		40		65		ns
t_{TSP}	$\overline{\text{STBX}}$ Pulse Width (Trans.)	25		30		50		ns
t_{BLZ}[8, 9]	$\overline{\text{BYPX}}$ LOW to Low Z (Read)	5		10		15		ns
t_{BDV}[8, 9]	$\overline{\text{BYPX}}$ HIGH to Data Invalid (Read)	3		3		3		ns
t_{WHF}	$\overline{\text{STBX}}$ LOW to $\overline{\text{HF}}$ LOW (Write)		40		50		80	ns
t_{RHF}	$\overline{\text{STBX}}$ HIGH to $\overline{\text{HF}}$ HIGH (Read)		40		50		80	ns
t_{RAE}	Effective Read from Write HIGH		30		35		60	ns
t_{RPE}	Effective Read Pulse Width after $\overline{\text{EF}}$ HIGH	30		40		65		ns
t_{WAF}	Effective Write from Read HIGH		30		35		60	ns
t_{WPF}	Effective Write Pulse Width after $\overline{\text{FF}}$ HIGH	30		40		65		ns
t_{BSU}	Bypass Data Set-Up Time	18		20		30		ns
t_{BHL}	Bypass Data Hold Time	0		0		10		ns

Notes:

7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance, as in *Figure 1a*, unless otherwise specified.
8. t_{DVR}, t_{BDV}, t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, t_{TSD}, t_{LZR}, t_{HWZ}, and t_{BLZ} use capacitance loading as in *Figure 1b*.
9. t_{HZR}, t_{TBD}, t_{BHZ}, t_{EBD}, t_{ESD}, and t_{TSD} transition is measured at +500 mV from V_{OL} and −500 mV from V_{OH}. t_{DVR} and t_{BDV} transition is measured at the 1.5V level. t_{LZR}, t_{HWZ} and t_{BLZ} transition is measured at ± 100 mV from the steady state.
10. See the last page of this specification for Group A subgroup testing information.
11. Direction selected Port A to Port B.

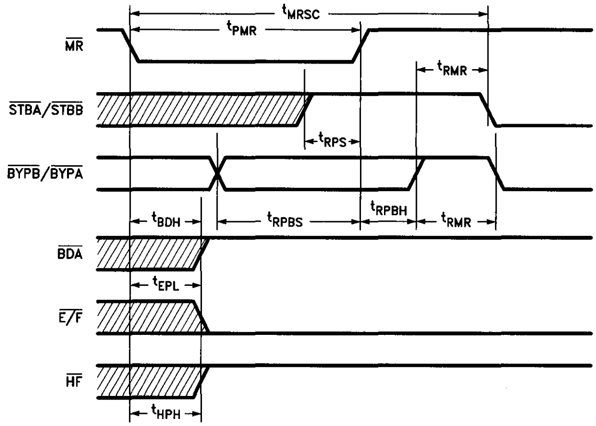
Switching Waveforms

Asynchronous Read and Write Timing Diagram



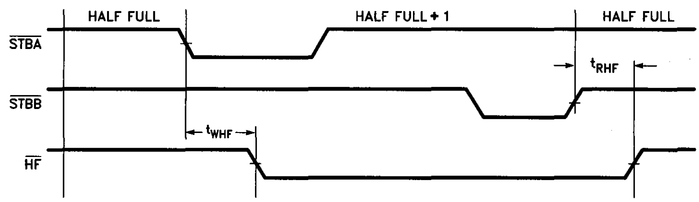
0178-8

Master Reset Timing Diagram



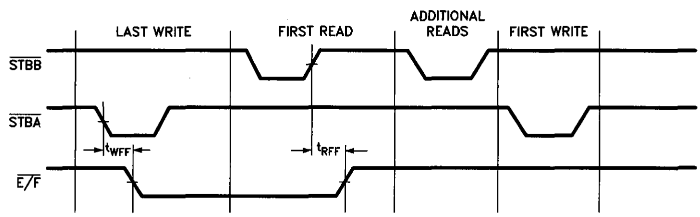
0178-9

Half Full Flag Timing Diagram[12]



0178-10

Last WRITE to First READ Empty/Full Flag Timing Diagram[12]



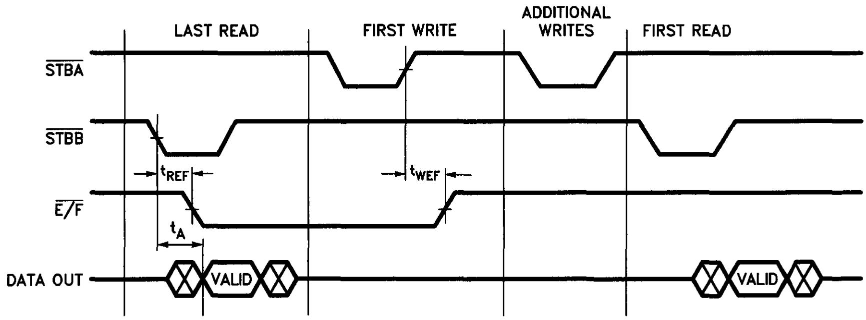
0178-11

Note:

12. Direction selected as A to B.

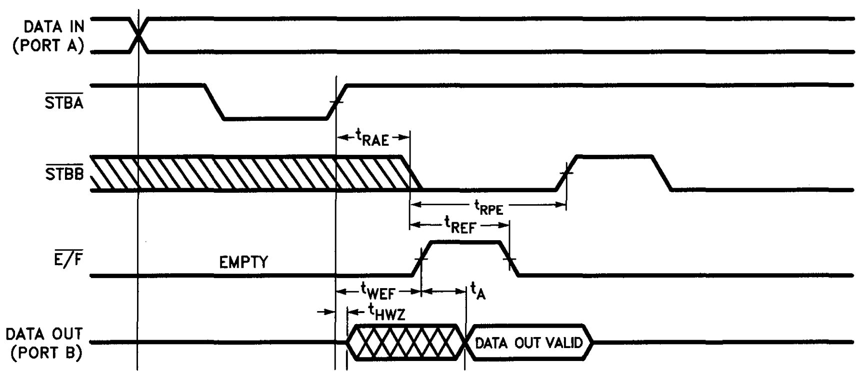
Switching Waveforms (Continued)

Last READ to First WRITE Empty/Full Flag Timing Diagram[12]



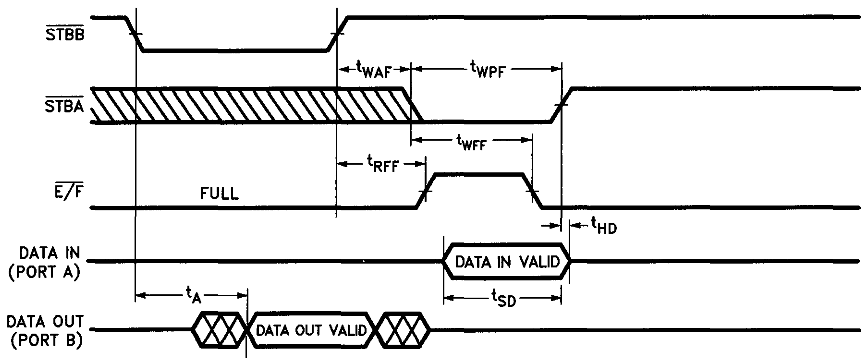
0178-12

Empty/Full Flag and Read Bubble-Through Mode Timing Diagram[12]



0178-13

Empty/Full Flag and Write Bubble-Through Mode Timing Diagram[12]

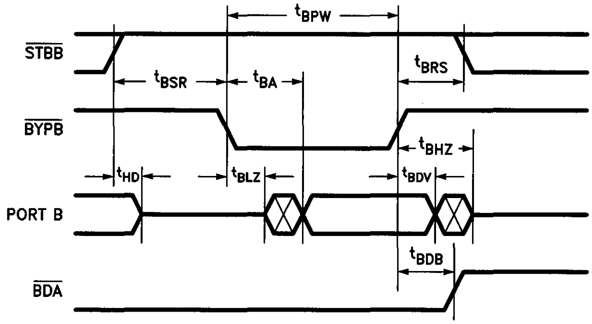


0178-14

Note:
12. Direction selected as A to B.

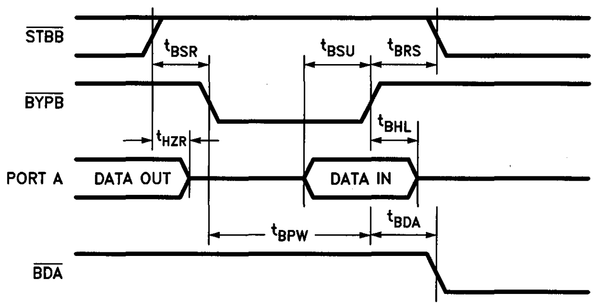
Switching Waveforms (Continued)

Registered Bypass Read Timing Diagram[13]



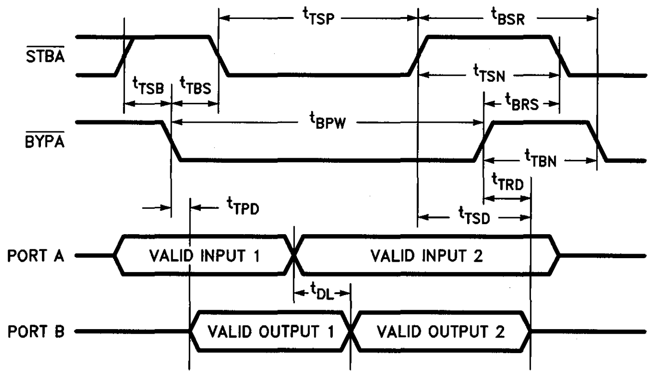
0178–15

Registered Bypass Write Timing Diagram[14]



0178–16

Transparent Bypass Timing Diagram[15]



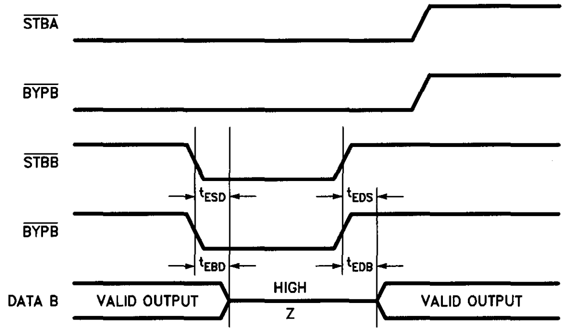
0178–17

Notes:

13. PORT B selected to read bypass register (FIFO direction PORT B to PORT A).
14. PORT A selected to write bypass register (FIFO direction PORT B to PORT A).
15. Diagram shows transparent bypass initiated by PORT A. Times are identical if initiated by PORT B.

Switching Waveforms (Continued)

Exception Condition Timing Diagram[15]



0178–18

Note:

15. Diagram shows transparent bypass initiated by PORT A. Times are identical if initiated by PORT B.

Architecture

The CY7C439 consists of a 2048 x 9-bit dual-ported RAM array, a read pointer, a write pointer, data switching circuitry, buffers, a bypass register, control signals ($\overline{STBA}$, $\overline{STBB}$, $\overline{BYPA}$, $\overline{BYPB}$, $\overline{MR}$), and flags ($\overline{E/F}$, $\overline{HF}$, $\overline{BDA}$).

Operation at Power-On

Automatic power-on reset is provided; the FIFO is cleared, $\overline{BDA}$ and $\overline{HF}$ go HIGH, $\overline{E/F}$ goes LOW, FIFO direction is port A to port B. At power-on the user can initialize the device by choosing the direction of FIFO operation *(Table 1)*, and pulsing $\overline{MR}$ LOW. There is a minimum low period for $\overline{MR}$, but no maximum time. The state of $\overline{BYPA}$ is latched internally by the rising edge of $\overline{MR}$ and used to determine the direction of subsequent data operations.

Resetting the FIFO

During the time $\overline{MR}$ is low, the FIFO tristates the data ports, sets $\overline{BDA}$ and $\overline{HF}$ HIGH, $\overline{E/F}$ LOW, and ignores the state of $\overline{BYPA/B}$ and $\overline{STBA/B}$. The bypass registers are initialized to zero. During this time the user is expected to set the direction of the FIFO by driving $\overline{BYPA}$ HIGH or LOW, and $\overline{BYPB}$, $\overline{STBA}$, and $\overline{STBB}$ HIGH. Following the rising edge of $\overline{MR}$ the FIFO memory is cleared. If $\overline{BYPA}$ is LOW (selecting direction B > A), the FIFO will then remain in a reset condition until the user terminates the reset operation by driving $\overline{BYPA}$ HIGH. If $\overline{BYPA}$ is HIGH (selecting direction A > B), the reset condition terminates after the rising edge of $\overline{MR}$. The entire reset phase can be accomplished in one cycle time of t_{RC}.

FIFO Operation

The operation of the FIFO requires only one control pin per port ($\overline{STBX}$). The user determines the direction of the FIFO data flow by initiating an $\overline{MR}$ cycle (see *Table 1*), which clears the FIFO and bypass register, and sets the data path and control signal multiplexers. The bypass register is configured in the opposite direction to the FIFO data flow. The FIFO direction can be reversed at any time by initiating another $\overline{MR}$ cycle. Data is written into the FIFO on the rising edge of the input, $\overline{STBX}$, and read from the FIFO by a low level at the output, $\overline{STBX}$. The two ports are asynchronous and independent. If the user attempts to read the FIFO when it is empty, no action takes place (the read pointer is not incremented) until the other port writes to the FIFO. Then a "bubble-through" read takes place, in which the read strobe is generated internally and the data becomes available at the read port shortly thereafter, if the read strobe ($\overline{STBX}$) is still LOW. Similarly, for an attempted write operation when the FIFO is full, no internal operation takes place until the other port performs a read operation, at which time the "bubble-through" write is performed, if the write strobe ($\overline{STBX}$) is still LOW.

Registered Bypass Operation

The registered bypass feature provides a means of transferring one 9-bit word of data in the opposite direction to normal data flow without affecting either the FIFO contents, or the FIFO write operations at the other port. The bypass register is configured during reset to provide a data path in the opposite direction to that of the FIFO (see *Table 1*). For example, if port A is writing data to the FIFO (hence port B is reading data from the FIFO) then $\overline{BYPB}$ is used to write to the bypass register at port B, and $\overline{BYPA}$ is used to read a single word from the bypass register at port A. The bypass data available flag ($\overline{BDA}$) is generated to notify port A that bypass data is available. $\overline{BDA}$ goes true on the trailing edge of the $\overline{BYPX}$ write operation, and false upon the trailing edge of the $\overline{BYPX}$ read operation.

Data is written on the rising edge of $\overline{BYPX}$ into the bypass register for later retrieval by the other port, irrespective of the state of $\overline{BDA}$. The bypass register is read by a low level at $\overline{BYPX}$, irrespective of the state of $\overline{BDA}$.

Transparent Bypass Operation

The transparent bypass feature provides a means of sending immediate data "around" the FIFO in either direction. The FIFO contents are not affected by the use of transparent bypass, but the control signals for transparent bypass are shared with those of the normal FIFO operation. Hence there are limitations on the use of transparent

Architecture (Continued)

bypass to ensure that data integrity and ease-of-use are preserved. The port wishing to send immediate data must ensure that the other port will not attempt a FIFO read or write during the transparent bypass cycle. If this is not possible, registered bypass or external circuitry should be used.

Transparent bypass mode is initiated by bringing both $\overline{BYPA}$ and $\overline{STBA}$ LOW together. Care should be taken to observe the following constraints on the timing relationships. Since $\overline{STBA}$ is used for normal FIFO operations, it must follow $\overline{BYPA}$ falling edge by t_{TBS} to prevent erroneous FIFO read or write operations. Since $\overline{BYPA}$ is used alone to initiate registered bypass read and write, it is internally delayed before initiating registered bypass. If $\overline{STBA}$ falls during this time, delay registered bypass is averted, and transparent bypass is initiated. Identical arguments apply to $\overline{BYPB}$ and $\overline{STBB}$.

If a transparent bypass sequence is successfully accomplished, data presented to the initiating port (port A in the above discussion) will be buffered to the other (port B) after t_{DL}. Either port can initiate a transparent bypass operation at any time, but if the control signals ($\overline{STBA/B}$, $\overline{BYPA/B}$) are in conflict (exception condition), internal circuitry will switch both ports to high impedance until the conflict is resolved.

Flag Operation

There are two flags, empty/full ($\overline{E/F}$) and half full ($\overline{HF}$), which are used to decode four FIFO states (see *Table 3*). The states are empty, 1–1024 locations full, 1025–2047 locations full, and full. Note that two conditions cause the $\overline{E/F}$ pin to go low, empty and full, hence both flag pins must be used to resolve the two conditions.

Table 1. FIFO Direction Select Truth Table

$\overline{MR}$	$\overline{BYPA}$	$\overline{BYPB}$	$\overline{STBA}$	$\overline{STBB}$	Action
1	X	X	X	X	Normal Operation
↑	1	1	1	1	FIFO Direction A to B, Registered Bypass Direction B to A
↑	0	1	1	1	FIFO Direction B to A, Registered Bypass Direction A to B
0	X	X	X	X	Internal Reset

X = Don't Care ↑ = Rising Edge

Table 2. Bypass Operation Truth Table

Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYPB}$	Action
A>B	⊔	1	⊔	1	Normal FIFO Operations, Write at A, Read at B
A>B	1	⊔	⊔	1	Normal FIFO Read at B, Bypass Register Read at A
A>B	⊔	1	1	⊔	Normal FIFO Write at A, Bypass Register Write at B
B>A	⊔	1	⊔	1	Normal FIFO Operations, Write at B, Read at A
B>A	1	⊔	⊔	1	Normal FIFO Write at B, Bypass Register Write at A
B>A	⊔	1	1	⊔	Normal FIFO Read at A, Bypass Register Read at B
X	0	0	1	1	No FIFO Operations, Transparent Data A to B
X	1	1	0	0	No FIFO Operations, Transparent Data B to A

Exception Conditions: Operation Not Defined

Direction	$\overline{STBA}$	$\overline{BYPA}$	$\overline{STBB}$	$\overline{BYPB}$	Action
X	0	1	0	0	Data Buses High Impedance
X	1	0	0	0	Data Buses High Impedance
X	0	0	0	0	Data Buses High Impedance
X	0	0	1	0	Data Buses High Impedance
X	0	0	0	1	Data Buses High Impedance

X = Either Direction ⊔ = Low Pulse

Table 3. Flag Truth Table

$\overline{E/F}$	$\overline{HF}$	State
0	1	Empty
1	1	1–1024 Locations Full
1	0	1025–2047 Locations Full
0	0	Full

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C439-30PC	P21	Commercial
	CY7C439-30JC	J65	
	CY7C439-30VC	V21	
	CY7C439-30DC	D22	
	CY7C439-30LC	L55	
40	CY7C439-40PC	P21	Commercial
	CY7C439-40JC	J65	
	CY7C439-40VC	V21	
	CY7C439-40DC	D22	
	CY7C439-40LC	L55	
	CY7C439-40DMB	D22	Military
	CY7C439-40LMB	L55	
	CY7C439-40KMB	K74	
65	CY7C439-65PC	P21	Commercial
	CY7C439-65JC	J65	
	CY7C439-65VC	V21	
	CY7C439-65DC	D22	
	CY7C439-65LC	L55	
	CY7C439-65DMB	D22	Military
	CY7C439-65LMB	L55	
	CY7C439-65KMB	K74	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{CC}	1,2,3
I_{SB1}	1,2,3
I_{SB2}	1,2,3
I_{OS}	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{RC}	9,10,11
t_{A}	9,10,11
t_{RR}	9,10,11
t_{PR}	9,10,11
t_{LZR}	9,10,11
t_{DVR}	9,10,11
t_{HZR}	9,10,11
t_{WC}	9,10,11
t_{PW}	9,10,11
t_{HWZ}	9,10,11
t_{WR}	9,10,11
t_{SD}	9,10,11
t_{HD}	9,10,11
t_{MRSC}	9,10,11
t_{PMR}	9,10,11
t_{RMR}	9,10,11
t_{RPS}	9,10,11
t_{RPBS}	9,10,11
t_{RPBH}	9,10,11
t_{BDH}	9,10,11
t_{BSR}	9,10,11
t_{EFL}	9,10,11
t_{HFH}	9,10,11
t_{BRS}	9,10,11

Parameters	Subgroups
t_{REF}	9,10,11
t_{RFF}	9,10,11
t_{WEF}	9,10,11
t_{WFF}	9,10,11
t_{WHF}	9,10,11
t_{RHF}	9,10,11
t_{RAE}	9,10,11
t_{RPE}	9,10,11
t_{WAF}	9,10,11
t_{WPF}	9,10,11
t_{BSU}	9,10,11
t_{BHL}	9,10,11
t_{BDA}	9,10,11
t_{BDB}	9,10,11
t_{BA}	9,10,11
t_{BHZ}	9,10,11
t_{TSB}	9,10,11
t_{TBS}	9,10,11
t_{TSN}	9,10,11
t_{TSD}	9,10,11
t_{TBN}	9,10,11
t_{TBD}	9,10,11
t_{TPD}	9,10,11
t_{DL}	9,10,11

Parameters	Subgroups
t_{ESD}	9,10,11
t_{EBD}	9,10,11
t_{EDS}	9,10,11
t_{EDB}	9,10,11
t_{BPW}	9,10,11
t_{TSP}	9,10,11
t_{BLZ}	9,10,11
t_{BDV}	9,10,11

Document #: 38-00126

ADVANCED INFORMATION

CY7C441
CY7C442

CYPRESS SEMICONDUCTOR

Synchronous 512 x 9 FIFO
Synchronous 2K x 9 FIFO

Features

- **512 x 9 (CY7C441) and 2K x 9 (CY7C442) FIFO buffer memory**
- **Ultra-high-speed 70 MHz operation**
- **Supports free-running 50% (±10%) duty cycle clock inputs**
- **Empty, almost empty, and almost full status flags**
- **Width-expandable**
- **Fully asynchronous and simultaneous read and write operation**
- **Rising-edge triggered clock inputs**
- **Independent read and write enable pins**
- **Registered data inputs and outputs**
- **Available in 300-mil 28-pin DIP, PLCC, LCC, and SOJ packages**
- **Center power and ground pins for reduced noise**
- **Dual-port RAM cell**
- **Proprietary 0.8μ CMOS technology**
- **TTL compatible**

Functional Description

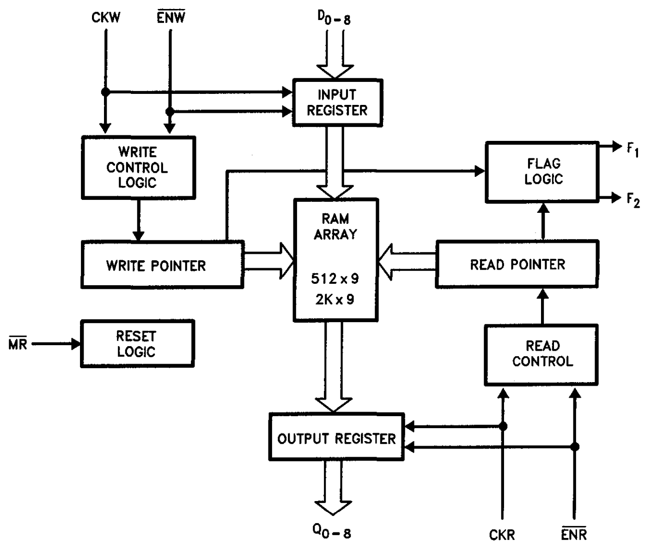
The CY7C441 and CY7C442 are ultra-high-speed low-power first-in first-out (FIFO) memories with registered (synchronous) interfaces and status flags. The CY7C441 has a 512 x 9-bit memory array, while the CY7C442 has a 2048 x 9-bit wide array. These devices provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces and communications buffering.

Both FIFOs have 9-bit input and output ports. The input port is controlled by a free-running 50% (±10%) duty-cycle clock (CKW) and a write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is low, data is written into the synchronous FIFO on the rising edge of CKW. The output port is controlled in a similar manner by a free-running read clock (CKR) and the read enable pin ($\overline{ENR}$). The read (CKR) and write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write operations. Clock frequencies up to 70 MHz are acceptable.

The synchronous FIFOs have two fixed status flags, F1 and F2, which indicate empty, almost empty, and almost full states. The empty and almost empty status is updated exclusively by RCK while almost full is updated exclusively by WCK. This architecture guarantees that the flags maintain their status for a minimum of one clock cycle.

5

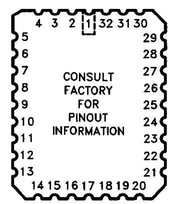
Logic Block Diagram



0176-1

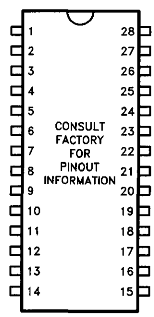
Pin Configurations

PLCC/LCC
Top View



0176-2

DIP
Top View



0176-3

CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7C443 CY7C444

Cascadeable Synchronous FIFO 512 x 9, 2K x 9

Features

- **512 x 9 (CY7C443) and 2K x 9 (CY7C444) FIFO buffer memory**
- **Ultra-high-speed 70 MHz operation**
- **Supports free-running 50% (±10%) duty cycle clock inputs**
- **Programmable parity generate/check**
- **Empty/full and half full status flags**
- **Programmable almost empty/full status flags**
- **Depth and width expandable**
- **Fully asynchronous and simultaneous read and write operation**
- **Rising-edge triggered clock inputs**
- **Independent read and write enable pins**
- **Retransmit function**
- **Registered data inputs and outputs**
- **Three-state outputs (with output enable)**
- **Available in 300-mil 32-pin DIP, PLCC, LCC, and SOJ packages**
- **Center power and ground pins for reduced noise**
- **Dual-port RAM cell**
- **Proprietary 0.8μ CMOS technology**
- **TTL compatible**

Functional Description

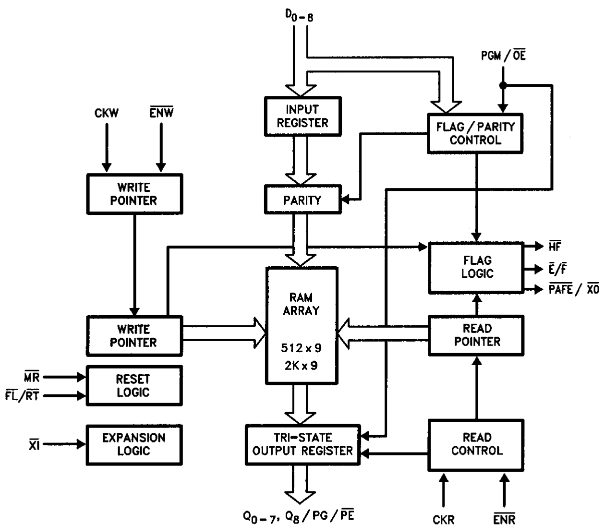
The CY7C443 and CY7C444 are ultra-high-speed low-power first-in first-out (FIFO) memories with registered (synchronous) interfaces, programmable status flags, and parity generate/check features. The CY7C443 has a 512 x 9-bit memory array, while the CY7C444 has a 2048 x 9-bit wide array. These devices provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces and communications buffering.

Both FIFOs have 9-bit input and output ports. The input port is controlled by a free-running 50% (±10%) duty-cycle clock (CKW) and the write enable pin ($\overline{ENW}$). When $\overline{ENW}$ is low, data is written into the synchronous FIFO on the rising edge of CKW. The output port is controlled in a similar manner by a free-running read clock (CKR) and the read enable pin ($\overline{ENR}$). The read (CKR) and the write (CKW) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write operations. Clock frequencies up to 70 MHz are acceptable.

The synchronous FIFOs have three status flags, $\overline{E/F}$, $\overline{PAFE}$, and $\overline{HF}$, which indicate empty, almost empty, half full, almost full, and full conditions. The empty and almost empty status is updated exclusively by RCK while the full, almost full, and half full conditions are updated exclusively by WCK. This architecture guarantees that the flags maintain their status for a minimum of one clock cycle. The programmable almost full/empty flag ($\overline{PAFE}$) and the retransmit function are available in width expansion and single device mode only.

Parity generate/check and the programmable flags are configured by loading a register during the master reset cycle. The $\overline{XI}$ and $\overline{XO}$ pins provide FIFO depth expansion using a daisy-chain technique.

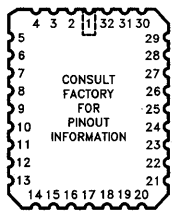
Logic Block Diagram



0177-1

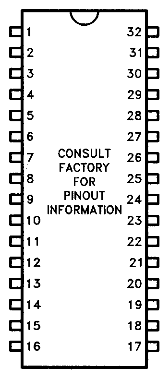
Pin Configurations

PLCC/LCC Top View



0177-2

DIP Top View



0177-3

CYPRESS SEMICONDUCTOR

Cascadeable 8K x 9 FIFO

Features

- 8K x 9 FIFO buffer memory
- Asynchronous read/write
- High-speed 20-MHz read/write
- Pin-compatible with 7C42X series of monolithic FIFOs
- Low operating power
  - I_{CC} (max.) = 350 mA
- 600-mil DIP package
- Empty, full flags
- Small PCB footprint
  - 0.84 sq. in.
- Expandable in depth and width

Functional Description

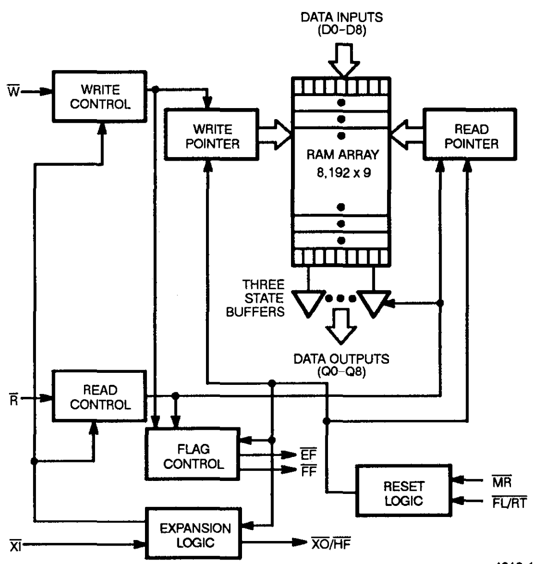
The CYM4210 is a first-in first-out (FIFO) memory module that is 8,192 words by 9 bits wide. It is offered in a 600-mil-wide DIP package. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 20 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The 9 data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

In the depth expansion configuration the ($\overline{XO}$) pin provides the expansion out information that is used to tell the next FIFO that it will be activated.

5

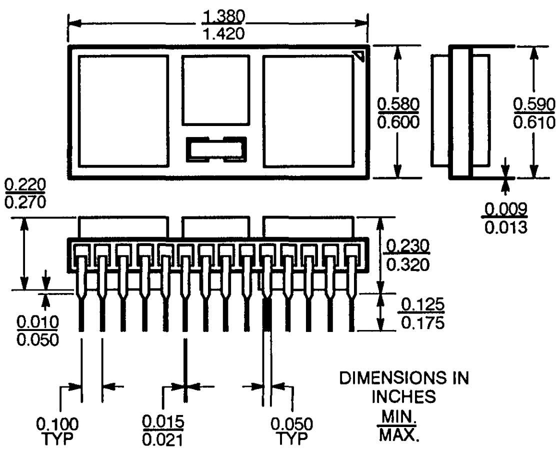
Logic Block Diagram



4210-1

Package Diagram

28-Pin DIP Module



4210-2

Document #: 38-M-00032

CYPRESS SEMICONDUCTOR

Cascadeable 16K x 9 FIFO

Features

- **16K x 9 FIFO buffer memory**
- **Asynchronous read/write**
- **High-speed 20-MHz read/write**
- **Pin-compatible with 7C42X series of monolithic FIFOs**
- **Low operating power**
  - **I_{CC} (max.) = 400 mA**
- **600-mil DIP package**
- **Empty and full flags**
- **Small PCB footprint**
  - **0.84 sq. in.**
- **Expandable in depth and width**

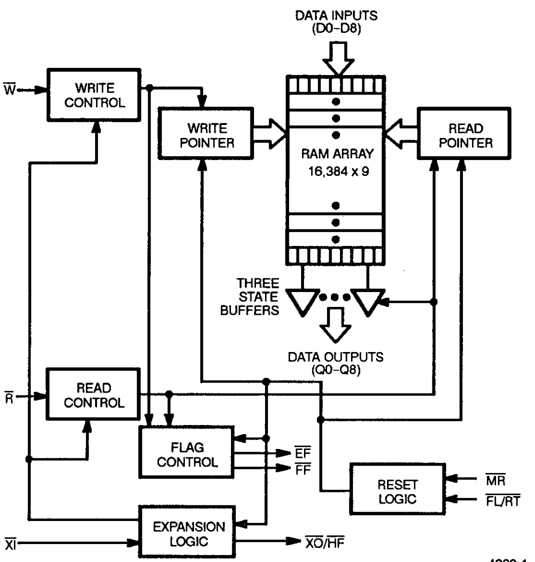
Functional Description

The CYM4220 is a first-in first-out (FIFO) memory module that is 16,384 words by 9 bits wide. It is offered in a 600-mil-wide DIP package. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 20 MHz. The write operation occurs when the Write ($\overline{W}$) signal is LOW. Read occurs when Read ($\overline{R}$) goes LOW. The 9 data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half-Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration the ($\overline{XO}$) pin provides the expansion out information which is used to tell the next FIFO that it will be activated.

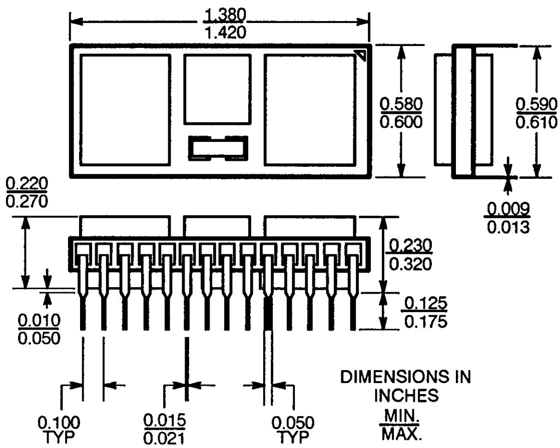
Logic Block Diagram



4220-1

Package Diagram

28-Pin DIP Module



4220-2

Document #: 38–M–00033

Section Contents

LOGIC

CMOS Four-Bit Slice

Features

- **Pin compatible and functional equivalent to AMD AM2901C**
- **Low power**
- **V_{CC} margin**
  - **— 5V ±10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **Eight function ALU**
  Performs eight operations on two 4-bit operands
- **Expandable**
  Infinitely expandable in 4-bit increments
- **Four status flags**
  Carry, overflow, negative, zero
- **ESD protection**
  Capable of withstanding greater than 2000V static discharge voltage

Functional Description

The CY2901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY2901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY2901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

The operation performed is determined by nine input control lines (I_0 to I_8) that are usually inputs from an instruction register.

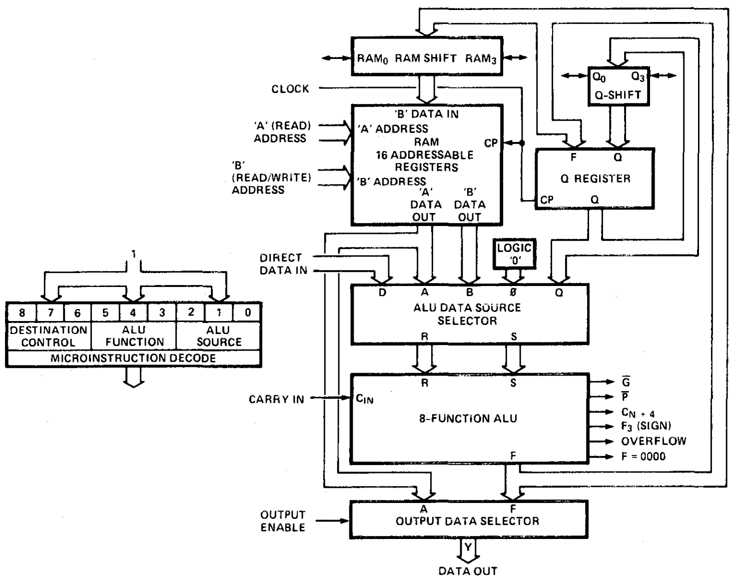
The CY2901 is expandable in 4-bit increments, has three-state data outputs as well as flag outputs, and can use either a full-look ahead carry or a ripple carry.

The CY2901 is a pin compatible, functional equivalent, improved performance replacement for the AM2901.

The CY2901 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection over 2000V and achieves superior performance at a low power dissipation.

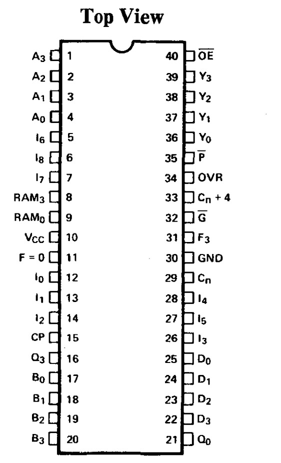
6

Logic Block Diagram



0007-1

Pin Configuration



0007-2

Selection Guide

See last page for ordering information.

Read Modify-Write Cycle (Min.) in ns	Operating I_{CC} (Max.) in mA	Operating Range	Part Number
31	140	Commercial	CY2901C
32	180	Military	CY2901C

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30)................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State..................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015)

Latchup Current (Outputs)................. >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Note:

1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
A_0–A_3	I	These 4 address lines select one of the registers in the stack and output its contents on the (internal) A port.
B_0–B_3	I	These 4 address lines select one of the registers in the stack and output is contents on the (internal) B port. This can also be the destination address when data is written back into the register file.
I_0–I_8	I	These 9 instruction lines select the ALU data sources ($I_{0,1,2}$), the operation to be performed ($I_{3,4,5}$) and what data is to be written into either the Q register or the register file ($I_{6,7,8}$).
D_0–D_3	I	These are 4 data input lines that may be selected by the $I_{0,1,2}$ lines as inputs to the ALU.
Y_0–Y_3	O	These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the $I_{6,7,8}$ lines.
$\overline{OE}$	I	Output Enable. This is an active LOW input that controls the Y_0–Y_3 outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high impedance state.
CP	I	Clock Input. The LOW level of the clock writes data to the 16 x 4 RAM. The HIGH level of the clock writes data from the RAM to the A-port and B-port latches. The operation of the Q register is similar. Data is entered into the master latch on the LOW level of the clock and transferred from master to slave when the clock is HIGH.
Q_3 RAM_3	I/O	These two lines are bidirectional and are controlled by the $I_{6,7,8}$ inputs. Electrically they are three-state output drivers connected to the TTL compatible CMOS inputs.
Q_3 RAM_3 (Cont.)	I/O	**Outputs:** When the destination code on lines $I_{6,7,8}$ indicates a shift left (UP) operation the three-state outputs are enabled and the MSB of the Q register is output on the Q_3 pin and the MSB of the ALU output (F_3) is output on the RAM 3 pin. **Inputs:** When the destination code indicates a shift right (DOWN) the pins are the data inputs to the MSB of the Q register and the MSB of the RAM.
Q_0 RAM_0	I/O	These two lines are bidirectional and function in a manner similar to the Q_3 and RAM_3 lines, except that they are the LSB of the Q register and RAM.
C_n	I	The carry-in to the internal ALU.
C_{n+4}	O	The carry-out from the internal ALU.
$\overline{G}, \overline{P}$	O	The carry generate and the carry propagate outputs of the ALU, which may be used to perform a carry look-ahead operation over the 4 bits of the ALU.
OVR	O	Overflow. This signal is logically the exclusive-OR of the carry-in and the carry-out of the MSB of the ALU. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine. It is valid only for the sign bit and assumes two's complement coding for negative numbers.
F = 0	O	Open collector output that goes HIGH if the data on the ALU outputs ($F_{0,1,2,3}$) are all LOW. It indicates that the result of an ALU operation is zero (positive logic).
F_3	O	The most significant bit of the ALU output.

Electrical Characteristics Over Commercial and Military Operating Range[3]

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

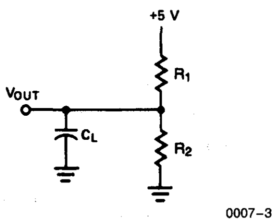
Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = −3.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 20 mA Commercial I_{OL} = 16 mA Military			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max. V_{IN} = V_{CC}			10	μA
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = GND			−10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min. V_{OH} = 2.4V		−3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min. V_{OL} = 0.4V	Commercial	20		mA
			Military	16		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max. V_{OUT} = GND to V_{CC}		−40	+40	μA μA
I_{SC}	Output Short Circuit Current[1]	V_{CC} = Max. V_{OUT} = 0V		−30	−85	mA
I_{CC}	Supply Current	V_{CC} = Max.	Commercial		140	mA
			Military		180	mA

Capacitance[2]

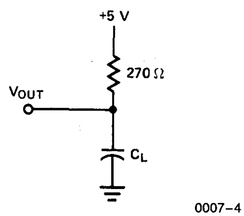
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:
1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Tested initially and after any design or process changes that may affect these parameters.
3. See the last page of this specification for Group A subgroup testing information.

Output Loads used for AC Performance Characteristics



All outputs except open drain



Open drain (F = 0)

Notes:
1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.
3. Loads shown above are for commercial (20 mA) I_{OL} specifications only.

	Commercial	Military
R_1	203Ω	252Ω
R_2	148Ω	174Ω

6

CY2901C Guaranteed Commercial Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See previous page for loading circuit information.

This data applies to parts with the following numbers:
CY2901CPC   CY2901CDC   CY2901CLC

Cycle Time and Clock Characteristics

CY2901-	C
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	31 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	15 ns
Minimum Clock Period	31 ns

For faster performance see CY7C901-23 specification.

Combinational Propagation Delays. C_L = 50 pF

To Output / From Input	Y	F_3	$C_n + 4$	$\overline{G}, \overline{P}$	F = 0	OVR	RAM_0 RAM_3	Q_0 Q_3
A, B Address	40	40	40	37	40	40	40	—
D	30	30	30	30	38	30	30	—
C_n	22	22	20	—	25	22	25	—
I_{012}	35	35	35	37	37	35	35	—
I_{345}	35	35	35	35	38	35	35	—
I_{678}	25	—	—	—	—	—	26	26
A Bypass ALU (I = 2XX)	35	—	—	—	—	—	—	—
Clock ↑	35	35	35	35	35	35	35	28

Set-up and Hold Times Relative to Clock (CP) Input

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	15	1 (Note 3)	30, 15 + t_{PWL} (Note 4)	1
B Destination Address	15	← Do Not Change	→	1
D	—	—	25	0
C_n	—	—	20	0
I_{012}	—	—	30	0
I_{345}	—	—	30	0
I_{678}	10	← Do Not Change	→	0
$RAM_{0,3}, Q_{0,3}$	—	—	12	0

Output Enable/Disable Times

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY2901C	$\overline{OE}$	Y	23	23

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

CY2901C Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" of this data sheet for loading circuit information.

This data applies to parts with the following numbers:

CY2901CDMB

Cycle Time and Clock Characteristics[5]

CY2901-	C
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	32 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	15 ns
Minimum Clock Period	32 ns

For faster performance see CY7C901-27 specification.

Combinational Propagation Delays C_L = 50 pF[5]

To Output / From Input	Y	F_3	$C_n + 4$	$\overline{G}, \overline{P}$	F = 0	OVR	RAM_0 RAM_3	Q_0 Q_3
A, B Address	48	48	48	44	48	48	48	—
D	37	37	37	34	40	37	37	—
C_n	25	25	21	—	28	25	28	—
I_{012}	40	40	40	44	44	40	40	—
I_{345}	40	40	40	40	40	40	40	—
I_{678}	29	—	—	—	—	—	29	29
A Bypass ALU (I = 2XX)	40	—	—	—	—	—	—	—
Clock	40	40	40	40	40	40	40	33

Set-up and Hold Times Relative to Clock (CP) Input[5]

Input	Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	15	2 (Note 3)	30, 15 + t_{PWL} (Note 4)	2
B Destination Address	15	← Do Not Change	→	2
D	—	—	25	0
C_n	—	—	20	0
I_{012}	—	—	30	0
I_{345}	—	—	30	0
I_{678}	10	← Do Not Change	→	0
$RAM_{0, 3}, Q_{0, 3}$	—	—	12	0

Output Enable/Disable Times[5]

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY2901C	$\overline{OE}$	Y	25	25

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.
5. See the last page of this specification for Group A subgroup testing information.

Ordering Information

Read Modify-Write Cycle (ns)	Ordering Code	Package Type	Operating Range
31	CY2901CPC	P17	Commercial
31	CY2901CDC	D18	Commercial
32	CY2901CDMB	D18	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IH}	1,2,3
I_{IL}	1,2,3
I_{OH}	1,2,3
I_{OL}	1,2,3
I_{OZ}	1,2,3
I_{SC}	1,2,3
I_{CC}	1,2,3

Cycle Time and Clock Characteristics

Parameters	Subgroups
Minimum Clock LOW Time	7,8,9,10,11
Minimum Clock HIGH Time	7,8,9,10,11

Combinational Propagation Delays

Parameters	Subgroups
From A, B Address to Y	7,8,9,10,11
From A, B Address to F3	7,8,9,10,11
From A, B Address to $C_n + 4$	7,8,9,10,11
From A, B Address to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From A, B Address to F = 0	7,8,9,10,11
From A, B Address to OVR	7,8,9,10,11
From A, B Address to $RAM_{0, 3}$	7,8,9,10,11
From D to Y	7,8,9,10,11
From D to F_3	7,8,9,10,11
From D to $C_n + 4$	7,8,9,10,11
From D to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From D to F = 0	7,8,9,10,11
From D to OVR	7,8,9,10,11
From D to $RAM_{0, 3}$	7,8,9,10,11

Combinational Propagation Delays (Continued)

Parameters	Subgroups
From C_n to Y	7,8,9,10,11
From C_n to F3	7,8,9,10,11
From C_n to $C_n + 4$	7,8,9,10,11
From C_n to F = 0	7,8,9,10,11
From C_n to OVR	7,8,9,10,11
From C_n to $RAM_{0, 3}$	7,8,9,10,11
From I_{012} to Y	7,8,9,10,11
From I_{012} to F_3	7,8,9,10,11
From I_{012} to $C_n + 4$	7,8,9,10,11
From I_{012} to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From I_{012} to F = 0	7,8,9,10,11
From I_{012} to OVR	7,8,9,10,11
From I_{012} to $RAM_{0, 3}$	7,8,9,10,11
From I_{345} to Y	7,8,9,10,11
From I_{345} to F_3	7,8,9,10,11
From I_{345} to $C_n + 4$	7,8,9,10,11
From I_{345} to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From I_{345} to F = 0	7,8,9,10,11
From I_{345} to OVR	7,8,9,10,11
From I_{345} to $RAM_{0, 3}$	7,8,9,10,11
From I_{678} to Y	7,8,9,10,11
From I_{678} to $RAM_{0, 3}$	7,8,9,10,11
From I_{678} to $Q_{0, 3}$	7,8,9,10,11
From A Bypass ALU to Y (I = 2XX)	7,8,9,10,11
From Clock $\uparrow$ to Y	7,8,9,10,11
From Clock $\uparrow$ to F_3	7,8,9,10,11
From Clock $\uparrow$ to $C_n + 4$	7,8,9,10,11
From Clock $\uparrow$ to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From Clock $\uparrow$ to F = 0	7,8,9,10,11
From Clock $\uparrow$ to OVR	7,8,9,10,11
From Clock $\uparrow$ to $RAM_{0, 3}$	7,8,9,10,11
From Clock $\uparrow$ to $Q_{0, 3}$	7,8,9,10,11

Set-up and Hold Times Relative to Clock (CP) Input

Parameters	Subgroups
A, B Source Address Set-up Time Before H → L	7,8,9,10,11
A, B Source Address Hold Time After H → L	7,8,9,10,11
A, B Source Address Set-up Time Before L → H	7,8,9,10,11
A, B Source Address Hold Time After L → H	7,8,9,10,11
B Destination Address Set-up Time Before H → L	7,8,9,10,11
B Destination Address Hold Time After H → L	7,8,9,10,11
B Destination Address Set-up Time Before L → H	7,8,9,10,11
B Destination Address Hold Time After L → H	7,8,9,10,11
D Set-up Time Before L → H	7,8,9,10,11

Parameters	Subgroups
D Hold Time After L → H	7,8,9,10,11
C_n Set-up Time Before L → H	7,8,9,10,11
C_n Hold Time After L → H	7,8,9,10,11
I_{012} Set-up Time Before L → H	7,8,9,10,11
I_{012} Hold Time After L → H	7,8,9,10,11
I_{345} Set-up Time Before L → H	7,8,9,10,11
I_{345} Hold Time After L → H	7,8,9,10,11
I_{678} Set-up Time Before H → L	7,8,9,10,11
I_{678} Hold Time After H → L	7,8,9,10,11
I_{678} Set-up Time Before L → H	7,8,9,10,11
I_{678} Hold Time After L → H	7,8,9,10,11
RAM_0, RAM_3, Q_0, Q_3 Set-up Time Before L → H	7,8,9,10,11
RAM_0, RAM_3, Q_0, Q_3 Hold Time After L → H	7,8,9,10,11

Document #: 38-00008-B

CY2909A
CY2911A

CYPRESS SEMICONDUCTOR

CMOS Micro Program Sequencers

Features

- **Fast**
  - **CY2909A/11A has a 40 ns (min.) clock to output cycle time; commercial**
  - **CY2909/11 has a 40 ns (min.) clock to output cycle time; military**
- **Low power**
  - **I_{CC} (max.) = 70 mA commercial**
  - **I_{CC} (max.) = 90 mA military**
- **V_{CC} margin**
  - **5V ±10%**
  - **All parameters guaranteed over commercial and military operating temperature range**
- **Expandable**
  Infinitely expandable in 4-bit increments
- **ESD protection**
  Capable of withstanding greater than 2000V static discharge voltage
- **Pin compatible and functional equivalent to AMD AM2909A/AM2911A**

Description

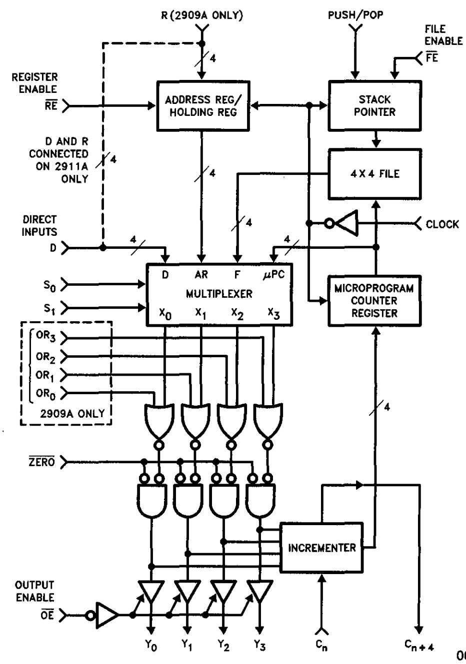
The CY2909A and CY2911A are high-speed, four-bit wide address sequencers intended for controlling the sequence of execution of microinstructions contained in microprogram memory. They may be connected in parallel to expand the address width in 4 bit increments. Both devices are implemented in high performance CMOS for optimum speed and power.

The CY2909A can select an address from any of four sources. They are: 1) a set of four external direct inputs (D_i); 2) external data stored in an internal register (R_i); 3) a four word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs (Y_i) can be OR'ed with an external input for conditional skip or branch instructions. A $\overline{\text{ZERO}}$ input line forces the outputs to all zeros. The outputs are three state, controlled by the Output Enable ($\overline{\text{OE}}$) input.

The CY2911A is an identical circuit to the CY2909A, except the four OR inputs are removed and the D and R inputs are tied together. The CY2911A is available in a 20-pin, 300-mil package. The CY2909 is available in a 28-pin, 600-mil package.

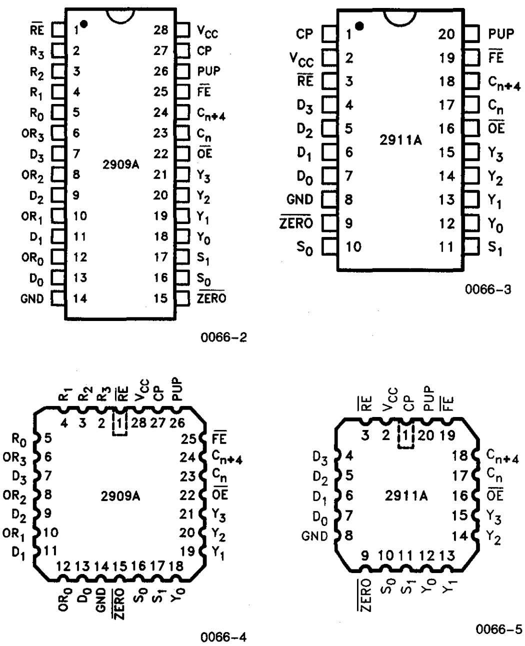
6

Logic Block Diagram



0066–1

Pin Configurations



0066–2

0066–3

0066–4

0066–5

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current, into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V (per MIL-STD-883 Method 3015)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[4]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.6 mA (Comm.)		2.4		V
		V_{CC} = Min., I_{OH} = −1.0 mA (Mil.)		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input High Voltage			2.0	V_{CC}	V
V_{IL}	Input Low Voltage			−2.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−20	+20	μA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max.	V_{OUT} = GND	−30	−85	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		70	mA
			Military		90	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms

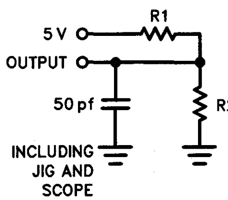
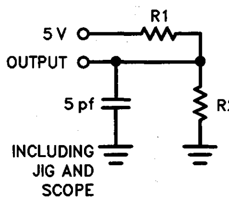


Figure 1a



0066–6

Figure 1b

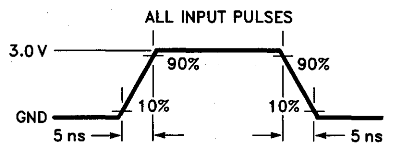


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Figure 2

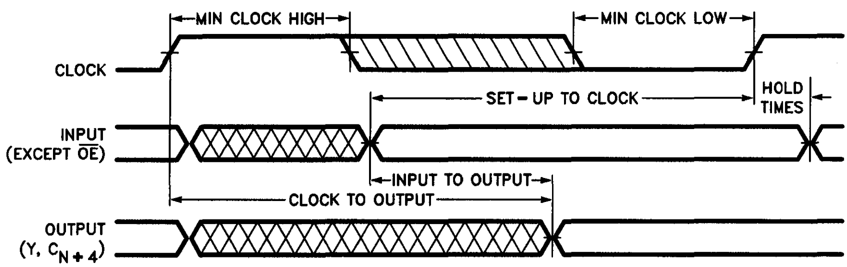
	Commercial	Military
R_1	254Ω	258Ω
R_2	187Ω	216Ω

Switching Characteristics Over Operating Range[4]

	2909A 2911A		2909A 2911A		Units
	Commercial		Military		
Minimum Clock Low Time	20		20		ns
Minimum Clock High Time	20		20		ns
MAXIMUM COMBINATIONAL PROPAGATION DELAYS					
From Input To:	Y	$C_N + 4$	Y	$C_N + 4$	ns
D_i	17	22	20	25	ns
S_0, S_1	29	34	29	34	ns
OR_i CY2909A	17	22	20	25	ns
C_N	—	14	—	16	ns
$\overline{ZERO}$	29	34	30	35	ns
$\overline{OE}$ Low to Output	25	—	25	—	ns
$\overline{OE}$ High to High Z[5]	25	—	25	—	ns
Clock High, S_0, S_1 = LH	39	44	45	50	ns
Clock High, S_0, S_1 = LL	39	44	45	50	ns
Clock High, S_0, S_1 = HL	44	49	53	58	ns
MINIMUM SET-UP AND HOLD TIMES (All Times Relative to Clock LOW to HIGH Transition)					
From Input	**Set-up**	**Hold**	**Set-up**	**Hold**	
$\overline{RE}$	19	4	19	5	ns
R_i [6]	10	4	12	5	ns
Push/Pop	25	4	27	5	ns
FE	25	4	27	5	ns
C_N	18	4	18	5	ns
D_i	25	0	25	0	ns
OR_i (CY2909A)	25	0	25	0	ns
S_0, S_1	25	0	29	0	ns
$\overline{ZERO}$	25	0	29	0	ns

Notes:
5. Output Loading as in *Figure 1b.*
6. R_i and D_i are internally connected on the CY2911A. Use R_i set-up and hold times for D_i inputs.

Switching Waveforms



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6

Ordering Information

Ordering Code	Package Type	Operating Range
CY2909APC	P15	Commercial
CY2909ADC	D16	
CY2909ALC	L64	
CY2909ADMB	D16	Military
CY2909ALMB	L64	

Ordering Code	Package Type	Operating Range
CY2911APC	P5	Commercial
CY2911ADC	D6	
CY2911ALC	L61	
CY2911ADMB	D6	Military
CY2911ALMB	L61	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{OS}	1,2,3
I_{CC}	1,2,3

Switching Characteristics

Parameters	Subgroups
Minimum Clock Low Time	7,8,9,10,11
Minimum Clock High Time	7,8,9,10,11
MAXIMUM COMBINATIONAL PROPAGATION DELAYS	
D_i to Y	7,8,9,10,11
D_i to C_{N+4}	7,8,9,10,11
S_0, S_1 to Y	7,8,9,10,11
S_0, S_1 to C_{N+4}	7,8,9,10,11
OR_i (CY2909A) to Y	7,8,9,10,11
OR_i (CY2909A) to C_{N+4}	7,8,9,10,11
C_N to C_{N+4}	7,8,9,10,11
$\overline{ZERO}$ to C_{N+4}	7,8,9,10,11
Clock High, S_0, S_1 = LH to Y	7,8,9,10,11
Clock High, S_0, S_1 = LH to C_{N+4}	7,8,9,10,11
Clock High, S_0, S_1 = LL to Y	7,8,9,10,11
Clock High, S_0, S_1 = LL to C_{N+4}	7,8,9,10,11
Clock High, S_0, S_1 = HL to Y	7,8,9,10,11
Clock High, S_0, S_1 = HL to C_{N+4}	7,8,9,10,11

Parameters	Subgroups
MINIMUM SET-UP AND HOLD TIMES	
$\overline{RE}$ Set-up Time	7,8,9,10,11
$\overline{RE}$ Hold Time	7,8,9,10,11
Push/Pop Set-up Time	7,8,9,10,11
Push/Pop Hold Time	7,8,9,10,11
FE Set-up Time	7,8,9,10,11
FE Hold Time	7,8,9,10,11
C_N Set-up Time	7,8,9,10,11
C_N Hold Time	7,8,9,10,11
D_i Set-up Time	7,8,9,10,11
D_i Hold Time	7,8,9,10,11
OR_i (CY2909A) Set-up Time	7,8,9,10,11
OR_i (CY2909A) Hold Time	7,8,9,10,11
S_0, S_1 Set-up Time	7,8,9,10,11
S_0, S_1 Hold Time	7,8,9,10,11
$\overline{ZERO}$ Set-up Time	7,8,9,10,11
$\overline{ZERO}$ Hold Time	7,8,9,10,11

Document #: 38-00009-B

CY2910A

CMOS Microprogram Controller

Features

- **Fast**
  - **— CY2910AC has a 50 ns (min.) clock cycle; commercial**
  - **— CY2910AM has a 51 ns (min.) clock cycle; military**
- **Low power**
  - **— I_{CC} (max.) = 170 mA**
- **V_{CC} Margin 5V ±10% commercial and military**
- **Sixteen powerful microinstructions**
- **Three output enable controls for three-way branch**
- **Twelve-bit address word**
- **Four sources for addresses: microprogram counter (MPC), branch address bus, 9-word stack, internal holding register**
- **Internal 9-word by 12-bit stack The internal stack can be used for subroutine return address or data storage**
- **12-bit Internal loop counter**
- **ESD protection Capable of withstanding over 2000 volts static discharge voltage**
- **Pin compatible and functional equivalent to Am2910A**

Functional Description

The CY2910A is a stand-alone micro-program controller that selects, stores, retrieves, manipulates and tests addresses that control the sequence of execution of instructions stored in an external memory. All addresses are 12-bit binary values that designate an absolute memory location.

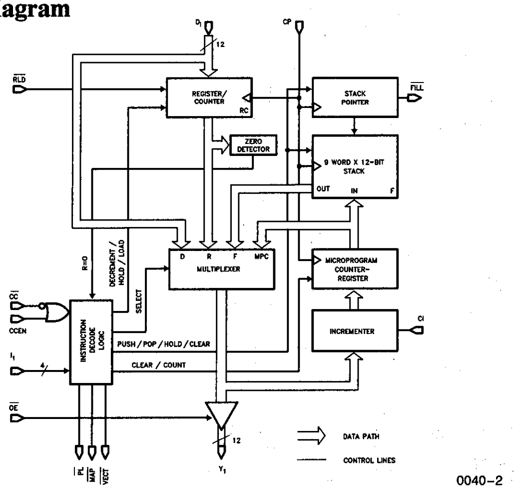
The CY2910A, as illustrated in the block diagram, consists of a 9-word by 12-bit LIFO (Last-In-First-Out) stack and SP (Stack Pointer), a 12-bit RC (Register/Counter), a 12-bit MPC (Microprogram Counter) and incrementer, a 12-bit wide by 4-input multiplexer and the required data manipulation and control logic.

The operation performed is determined by four input instruction lines (I0–I3) that in turn select the (internal) source of the next micro-instruction to be fetched. This address is output on the Y0–Y11 pins. Two additional inputs ($\overline{CC}$ and $\overline{CCEN}$) are provided that are examined during certain instructions and enable the user to make the execution of the instruction either unconditional or dependent upon an external test.

The CY2910A is a pin compatible, functional equivalent, improved performance replacement for the Am2910A.

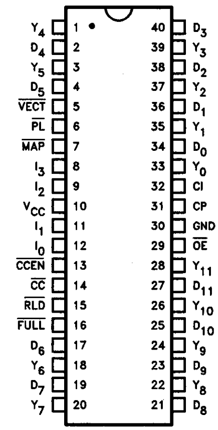
The CY2910A is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection of over 2000 volts and achieves superior performance and low power dissipation.

Logic Block Diagram



0040-2

Pin Configuration



0040-3

Top View

Selection Guide

Clock Cycle (Min.) in ns	Stack Depth	Operating Range	Part Number
50	9 words	Commercial	CY2910AC
51	9 words	Military	CY2910AM

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30)..................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) ....30 mA

Static Discharge Voltage ....>2001V (Per MIL-STD-883 Method 3015)

Latchup Current (Outputs)..................>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Commercial and Military Operating Range[4]

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameter	Description	Test Condition	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −1.6 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.5	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC}	V
V_{IL}	Input LOW Voltage		−3.0	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		10	μA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		−10	μA
I_{OH}	Output HIGH Current	V_{CC} = Min., V_{IH} = 2.4V	−1.6		mA
I_{OL}	Output LOW Current	V_{CC} = Min., V_{OL} = 0.5V	8		mA
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND/V_{CC}	 −40	+40	μA μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V		−85	mA
I_{CC}	Supply Current	V_{CC} = Max.		170	mA

Capacitance[2]

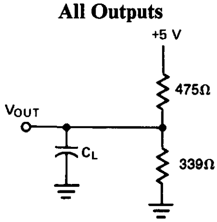
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not exceed one second.
2. Tested initially and after any design or process changes that may affect these parameters.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.

Output Load for AC Performance Characteristics

All Outputs

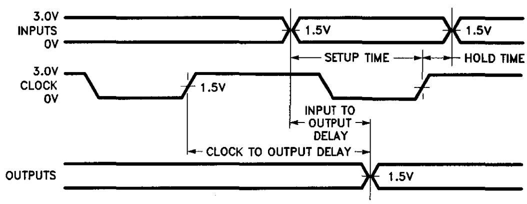


Notes: 0040-4

C_L = 50 pF includes scope probe, writing and stray capacitance.

C_L = 5 pF for output disable tests.

Switching Waveforms



0040-5

Guaranteed AC Performance Characteristics

The tables below specify the guaranteed AC performance of the CY2910A over the commercial (0°C to + 70°C) and the military (− 55°C to + 125°C) temperature ranges with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels.

The inputs switch between 0V and 3V with signal transition rates of 1 Volt per nanosecond. All outputs have maximum DC current loads.

Clock Requirements[1, 4]

	Commercial	Military
Minimum Clock LOW	20	25
Minimum Clock HIGH	20	25
Minimum Clock Period I = 14	50	51
Minimum Clock Period I = 8, 9, 15 (Note 2)	50	50

Combinational Propagation Delays. C_L = 50 pF[4]

To Output	Commercial			Military		
From Input	**Y**	**$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$**	**$\overline{FULL}$**	**Y**	**$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$**	**$\overline{FULL}$**
D0–D11	20	—	—	25	—	—
I0–I3	35	30	—	40	35	—
$\overline{CC}$	30	—	—	36	—	—
$\overline{CCEN}$	30	—	—	36	—	—
CP I = 8, 9, 15 (Note 2)	40	—	31	—	—	35
CP All Other I	40	—	31	46	—	35
$\overline{OE}$ (Note 3)	25 27	—	—	25 30	—	—

Minimum Set-up and Hold Times Relative to clock LOW to HIGH Transition. C_L = 50 pF[4]

	Commercial		Military	
Input	**Set-up**	**Hold**	**Set-up**	**Hold**
DI → RC	16	0	16	0
DI → MPC	30	0	30	0
I0–I3	35	0	38	0
$\overline{CC}$	24	0	35	0
$\overline{CCEN}$	24	0	35	0
CI	18	0	18	0
$\overline{RLD}$	19	0	20	0

Notes:

1. A dash indicates that a propagation delay path or set-up time does not exist.
2. These instructions are dependent upon the register/counter. Use the shorter delay times if the previous instruction either does not change the register/counter or could only decrement it. Use the longer delay if the instruction prior to the clock was 4 or 12 or if $\overline{RLD}$ was LOW.
3. The enable/disable times are measured to a 0.5 Volt change on the output voltage level with C_L = 5 pF.
4. See the last page of this specification for Group A subgroup testing information.

Table of Instructions

I_3–I_0	MNEMONIC	NAME	REG/CNTR CONTENTS	RESULT: FAIL $\overline{CCEN}$ = L and $\overline{CC}$ = H: Y	FAIL: STACK	PASS $\overline{CCEN}$ = H or $\overline{CC}$ = L: Y	PASS: STACK	REG/CNTR	ENABLE
0	JZ	Jump Zero	X	0	Clear	0	Clear	Hold	PL
1	CJS	Cond JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	Jump Map	X	D	Hold	D	Hold	Hold	Map
3	CJP	Cond Jump PL	X	PC	Hold	D	Hold	Hold	PL
4	PUSH	Push/Cond LD CNTR	X	PC	Push	PC	Push	(Note 1)	PL
5	JSRP	Cond JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	Cond Jump Vector	X	PC	Hold	D	Hold	Hold	Vect
7	JRP	Cond Jump R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	Repeat Loop, CNTR ≠ 0	≠0	F	Hold	F	Hold	Dec	PL
			=0	PC	POP	PC	Pop	Hold	PL
9	RPCT	Repeat PL, CNTR ≠ 0	≠0	D	Hold	D	Hold	Dec	PL
			=0	PC	Hold	PC	Hold	Hold	PL
10	CRTN	Cond RTN	X	PC	Hold	F	Pop	Hold	PL
11	CJPP	Cond Jump PL & Pop	X	PC	Hold	D	Pop	Hold	PL
12	LDCT	LD Cntr & Continue	X	PC	Hold	PC	Hold	Load	PL
13	LOOP	Test End Loop	X	F	Hold	PC	Pop	Hold	PL
14	CONT	Continue	X	PC	Hold	PC	Hold	Hold	PL
15	TWB	Three-Way Branch	≠0	F	Hold	PC	Pop	Dec	PL
			=0	D	Pop	PC	Pop	Hold	PL

Notes:
1. If $\overline{CCEN}$ = L and $\overline{CC}$ = H, hold; else load.

H = HIGH L = LOW X = Don't Care

6

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
50	CY2910ADC	D18	Commercial
	CY2910AJC	J67	
	CY2910ALC	L67	
	CY2910APC	P17	
51	CY2910ADMB	D18	Military
	CY2910ALMB	L67	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IH}	1,2,3
I_{IL}	1,2,3
I_{OH}	1,2,3
I_{OL}	1,2,3
I_{OZ}	1,2,3
I_{SC}	1,2,3
I_{CC}	1,2,3

Clock Requirements

Parameters	Subgroups
Minimum Clock LOW	7,8,9,10,11

Combinational Propagation Delays

Parameters	Subgroups
From D0–D11 to Y	7,8,9,10,11
From I0–I3 to Y	7,8,9,10,11
From I0–I3 to $\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	7,8,9,10,11
From $\overline{CC}$ to Y	7,8,9,10,11
From $\overline{CCEN}$ to Y	7,8,9,10,11
From CP (I = 8, 9, 15) to $\overline{FULL}$	7,8,9,10,11
From CP (All Other I) to Y	7,8,9,10,11
From CP (All Other I) to $\overline{FULL}$	7,8,9,10,11

Document #: 38-00010-B

Minimum Set-up and Hold Times

Parameters	Subgroups
DI → RC Set-up Time	7,8,9,10,11
DI → RC Hold Time	7,8,9,10,11
DI → MPC Set-up Time	7,8,9,10,11
DI → MPC Hold Time	7,8,9,10,11
I0–I3 Set-up Time	7,8,9,10,11
I0–I3 Hold Time	7,8,9,10,11
$\overline{CC}$ Set-up Time	7,8,9,10,11
$\overline{CC}$ Hold Time	7,8,9,10,11
$\overline{CCEN}$ Set-up Time	7,8,9,10,11
$\overline{CCEN}$ Hold Time	7,8,9,10,11
CI Set-up Time	7,8,9,10,11
CI Hold Time	7,8,9,10,11
$\overline{RLD}$ Set-up Time	7,8,9,10,11
$\overline{RLD}$ Hold Time	7,8,9,10,11

16 x 16 Multiplier Accumulator

Features

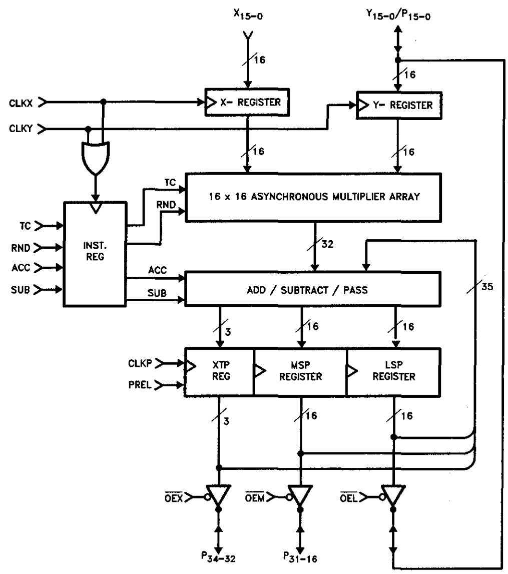
- **Fast**
  - **CY7C510-45 has a 45 ns (max.) clock cycle (commercial)**
  - **CY7C510-55 has a 55 ns (max.) clock cycle (military)**
- **Low Power**
  - **I_{CC} (max. at 10 MHz) = 100 mA (commercial)**
  - **I_{CC} (max. at 10 MHz) = 110 mA (military)**
- **V_{CC} Margin**
  - **5V ± 10%**
  - **All parameters guaranteed over commercial and military operating temperature range**
- **16 × 16 bit parallel multiplication with accumulation to 35-bit result**
- **Two's complement or unsigned magnitude operation**
- **ESD Protection**
  - **Capable of withstanding greater than 2000V static discharge voltage**
- **Pin compatible and functionally equivalent to Am29510 and TMC2110**

Functional Description

The CY7C510 is a high-speed 16 × 16 parallel multiplier accumulator which operates at 45 ns clocked multiply accumulate (MAC) time (22 MHz multiply accumulate rate). The operands may be specified as either two's complement or unsigned magnitude 16-bit numbers. The accumulator functions include loading the accumulator with the current product, adding or subtracting the accumulator contents and the current product, or preloading the accumulator from the external world.

All inputs (data and instructions) and outputs are registered. These independently clocked registers are positive edge triggered D-type flip-flops. The 35-bit accumulator/output register is divided into a 3-bit extended product (XTP), a 16-bit most significant product (MSP), and a 16-bit least significant product (LSP). The XTP and MSP have dedicated ports for three-state output; the LSP is multiplexed with the Y-input. The 35-bit accumulator/output register may be preloaded through the bidirectional output ports.

Logic Block Diagram



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Selection Guide

		7C510-45	7C510-55	7C510-65	7C510-75
Maximum Multiply-Accumulate Time (ns)	Commercial	45	55	65	75
	Military		55	65	75

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Ambient Temperature Under Bias .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

DC Voltage Applied to Outputs ..... −0.5V to V_{CC} Max.

Output Current, into Outputs (low)............. 10 mA

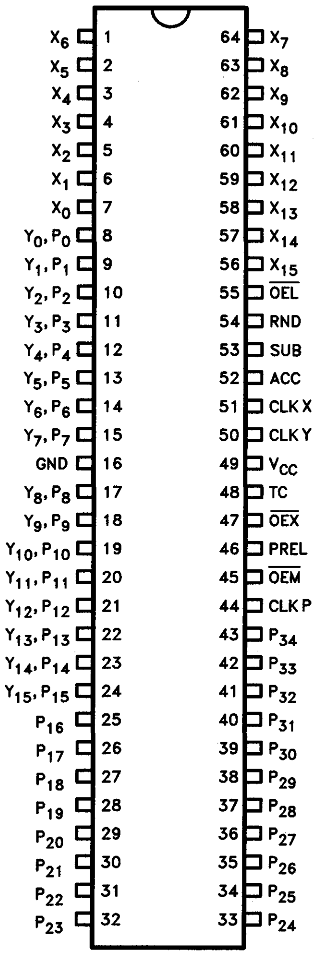
Static Discharge Voltage .... >2001V
(per MIL-STD-883 Method 3015)

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55° to +125°C	5V ±10%

Note:
1. T_A is the "instant on" case temperature.

Pin Configurations



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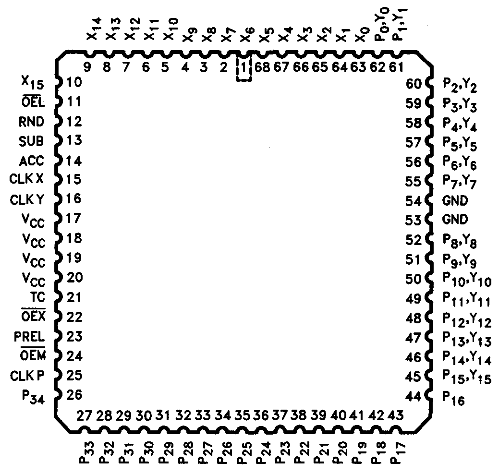
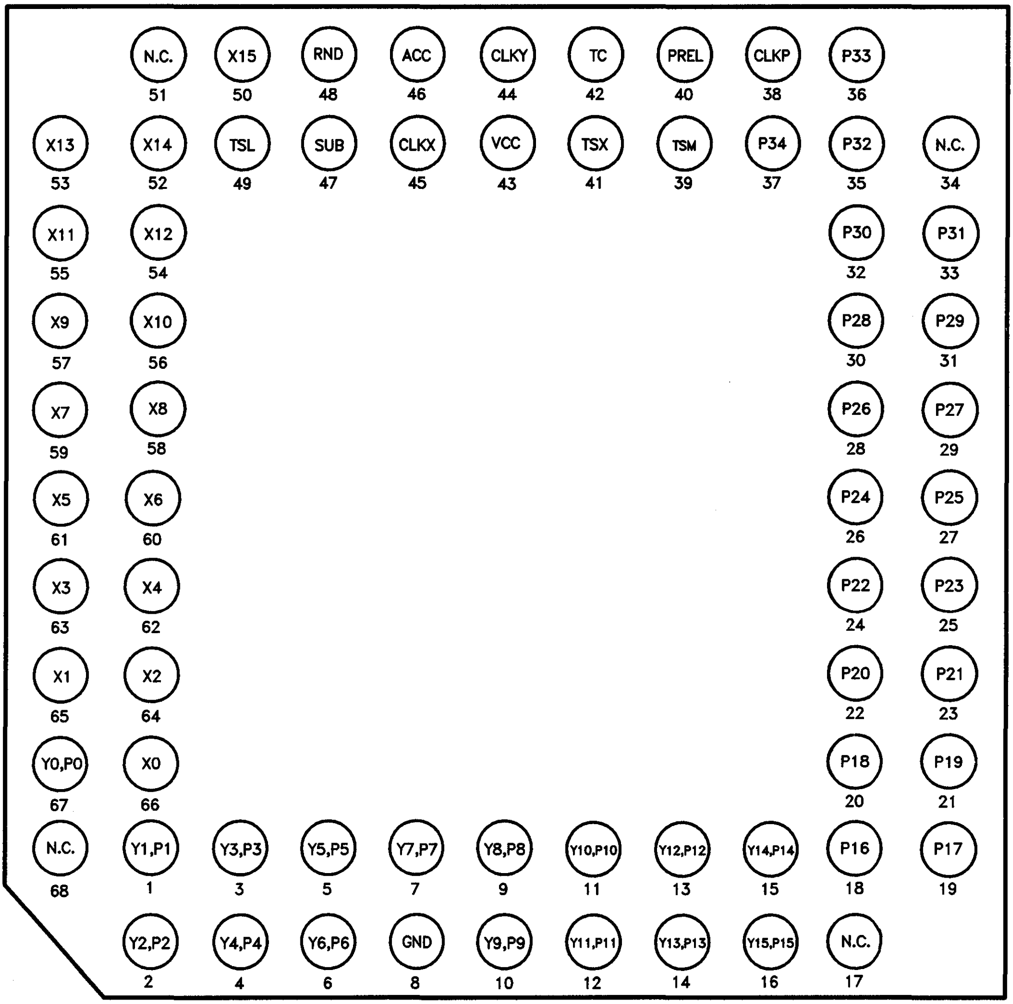


0057-3

Pin Configurations (Continued)

Pin Configuration for 68-Pin Grid Array



0057-13

6

Pin Definitions

Signal Name	I/O	Description
X_{15-0}	I	X-Input Data. This 16-bit number may be interpreted as two's complement or unsigned magnitude.
Y_{15-0} (P_{15-0})	I/O	Y-Input Data/LSP Output Data. When this port is used to input a Y value, the 16-bit number may be interpreted as two's complement or unsigned magnitude. This bidirectional port is multiplexed with the LSP output (P_{15-0}), and can also be used to preload the LSP register.
P_{34-32}	I/O	Extended Product (XTP) Output Data. This port is bidirectional. The extended product emerges through this port. The XTP register may also be preloaded through this port.
P_{31-16}	I/O	MSP Output Data. This port is bidirectional. The most significant product emerges through this port. The MSP register may also be preloaded through this port.
P_{15-0}	I/O	LSP Output Data. This port is bidirectional. The least significant product emerges through this port. The LSP register may also be preloaded through this port.
CLKX	I	X-Register Clock. X-Input Data are latched into the X-register at the rising edge of CLKX.
CLKY	I	Y-Register Clock. Y-Input Data are latched into the Y-register at the rising edge of CLKY.
CLKP	I	Product Register Clock. XTP, MSP, and LSP are latched into their respective registers at the rising edge of CLKP. If preload is selected, these registers are loaded with the preload data at the output pins via the bidirectional ports. If preload is not selected, these registers are loaded with the current accumulated product.
$\overline{\text{OEX}}$	I	Output Enable Extended. When LOW, the extended product bidirectional port is enabled for output. When HIGH, the outputs drivers are disabled (high impedance) and the XTP port may be used for preloading. See Preload Function Table.
$\overline{\text{OEM}}$	I	Output Enable Most. When LOW, the MSP bidirectional port is enabled for output. When HIGH, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See Preload Function Table.

Signal Name	I/O	Description
$\overline{\text{OEL}}$	I	Output Enable Least. When LOW, the LSP bidirectional port is enabled for output. When HIGH, the output drivers are disabled (high impedance) and the MSP port may be used for preloading. See Preload Function Table.
PREL	I	Preload. When HIGH, the three bidirectional ports may be used to preload data into the accumulator register at the rising edge of CLKP. The three-state controls ($\overline{\text{OEX}}$, $\overline{\text{OEM}}$, $\overline{\text{OEL}}$) must be HIGH to preload data. When LOW, the accumulated product is loaded into the accumulator/output register at the rising edge of CLKP. The output drivers must be enabled ($\overline{\text{OEX}}$, $\overline{\text{OEM}}$, $\overline{\text{OEL}}$ must be LOW) for the accumulated product to be output. Ordinarily, PREL, $\overline{\text{OEX}}$, $\overline{\text{OEM}}$, and $\overline{\text{OEL}}$ are tied together. See accumulator function table.
TC	I	Two's Complement Control. When HIGH, the 7C510 is in two's complement mode, where the input and output data are interpreted as two's complement numbers. The device is in unsigned magnitude mode when TC is LOW. This control is loaded into the instruction register at the rising edge of CLKX + CLKY.
RND	I	Round Control. When HIGH, rounding is enabled and a "1" is added to the MSB of the LSB (P_{15}). When LOW, the product is unchanged. This control is loaded into the instruction register at the rising edge of CLKX + CLKY.
ACC	I	Accumulate Control. When HIGH, the accumulator/output register contents are added to or subtracted from the current product (XY) and this result is stored back into the accumulator/output register. When LOW, the product is loaded into the accumulator register, overwriting the current contents. This control is loaded into the instruction register at the rising edge of CLKX + CLKY. See accumulator function table.
SUB	I	Subtract Control. When both ACC and SUB are HIGH, the accumulator register contents are subtracted from the current product XY and this result is written back into the accumulator register. When ACC is HIGH and SUB is LOW, the accumulator register contents and current product are summed, then written back to the accumulator register. This control is loaded into the instruction register at the rising edge of CLKX + CLKY. See accumulator function table.

Functional Description

The CY7C510 is a high-speed 16 × 16-bit multiplier accumulator (MAC). It comprises a 16-bit parallel multiplier followed by a 35-bit accumulator. All inputs (data and instructions) and outputs are registered. The 7C510 is divided into four sections: the input section, the 16 × 16 asynchronous multiplier array, the accumulator, and the output/preload section.

The input section has two 16-bit operand input registers for the X and Y operands, clocked by the rising edge of CLKX and CLKY, respectively. The four-bit instruction register (TC, RND, ACC, SUB) is clocked by the rising edge of the logical OR of CLKX, CLKY.

The 16 × 16 asynchronous multiplier array produces the 32-bit product of the input operands. Either two's complement or unsigned magnitude operation is selected, based on control TC. If rounding is selected, (RND = 1), a "1" is added to the MSB of the LSP (position P_{15}). The 32-bit product is zero-filled or sign-extended as appropriate and passed as a 35-bit number to the accumulator section.

The accumulator function is controlled by ACC, SUB, and PREL. Four functions may be selected: the accumulator may be loaded with the current product; the product may be added to the accumulator contents; the accumulator contents may be subtracted from the current product; or the accumulator may be preloaded from the bidirectional ports.

The output/preload section contains the accumulator/output register and the bidirectional ports. This section is controlled by the signals PREL, $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$. When PREL is HIGH, the output buffers are in high impedance state. When the controls $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ are also high, data present at the output pins will be preloaded into the appropriate accumulator register at the rising edge of CLKP. When PREL is LOW, the signals $\overline{OEX}$, $\overline{OEM}$, and $\overline{OEL}$ are enable controls for their respective three-state output ports.

Preload Function Table

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	Output Register		
				XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	PL
1	0	1	0	Z	PL	Z
1	0	1	1	Z	PL	PL
1	1	0	0	PL	Z	Z
1	1	0	1	PL	Z	PL
1	1	1	0	PL	PL	Z
1	1	1	1	PL	PL	PL

Z = Output buffers at High impedance (disabled.)
Q = Output buffers at Low impedance. Contents of output register available through output ports.
PL = Output disabled. Preload data supplied to the output pins will be loaded into the output register at the rising edge of CLKP.

Accumulator Function Table

PREL	ACC	SUB	P	OPERATION
L	L	X	Q	Load
L	H	L	Q	Add
L	H	H	Q	Subtract
H	X	X	PL	Preload

CY7C510
Input Formats

Fractional Two's Complement Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

Integer Two's Complement Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(Sign)															

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
(Sign)															

Unsigned Fractional Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Unsigned Integer Input

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

CY7C510
Output Formats

Two's Complement Fractional Output

XTP

34	33	32
-2^{4}	2^{3}	2^{2}
(Sign)		

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

Two's Complement Integer Output

XTP

34	33	32
-2^{34}	2^{33}	2^{32}
(Sign)		

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Output

XTP

34	33	32
2^{2}	2^{1}	2^{0}

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer Output

XTP

34	33	32
2^{34}	2^{33}	2^{32}

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Electrical Characteristics Over Operating Range[4]

Parameters	Description		Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = Min., I_{OH} = −0.4 mA		2.4		V
V_{OL}	Output LOW Voltage		V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input HIGH Voltage				2.0		V
V_{IL}	Input LOW Voltage					0.8	V
I_{OH}	Output HIGH Current		V_{CC} = Min., V_{OH} = 2.4V		−0.4		mA
I_{OL}	Output LOW Current		V_{CC} = Min., V_{OL} = 0.4V		4.0		mA
I_{IX}	Input Leakage Current		GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_I	Input Current, Max. Input Voltage		V_{CC} = Max., V_{IN} = 7.0V			10	mA
I_{OS}[1]	Output Short Circuit Current		V_{CC} = Max., V_{OUT} = 0.5V		−3	−30	mA
I_{OZL}	Output OFF (Hi-Z) Current		V_{CC} = Max., $\overline{OE}$ = 2.0V			−25	μA
I_{OZH}	Output OFF (Hi-Z) Current		V_{CC} = Max., $\overline{OE}$ = 2.0V		25		μA
I_{CC} (Q1)[2]	Supply Current (Quiescent)		V_{CC} = Max., V_{IN} = [GND to V_{IL}] or [V_{IH} to V_{CC}]			30	mA
I_{CC} (Q2)[2]	Supply Current (Quiescent)		V_{CC} = Max $V_{CC} \geq V_{IN} \geq$ 3.85V 0.4V ≥ V_{IN} ≥ GND	Commercial		20	mA
				Military		25	
I_{CC} (Max.)[2]	Supply Current	Commercial	V_{CC} = Max., f_{CLK} = 10 MHz			100	mA
		Military				110	

Capacitance[3]

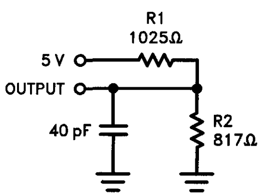
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	

Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. For I_{CC} measurements, the outputs are three-stated. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given clock frequency, use 30 mA + I_{CC} (A.C.), where I_{CC} (A.C.) = (7 mA/MHz) × Clock Frequency for the Commercial temperature range. I_{CC} (A.C.) = (8 mA/MHz) × Clock Frequency for Military temperature range.
3. Tested initially and after any design or process changes that may affect these parameters.
4. See the last page of this specification for Group A subgroup testing information.

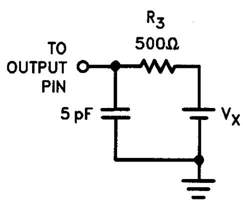
Output Loads Used for A.C. Performance Characteristics

Normal Load (Load 1)



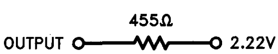
0057-4

Three-State Delay Load (Load 2)



0057-5

Equivalent to: THÉVENIN EQUIVALENT

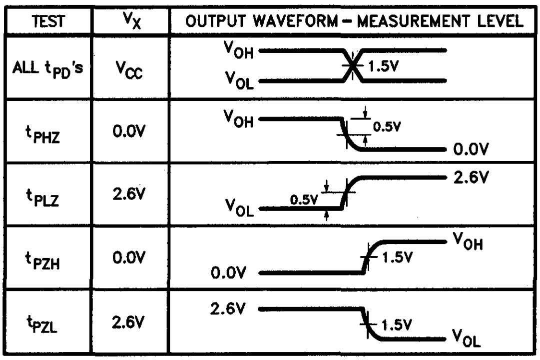


0057-6

Switching Characteristics Over Operating Range[3]

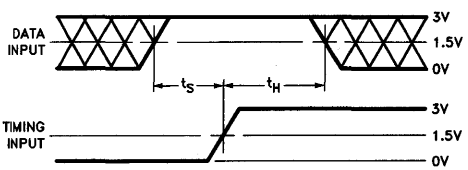
Parameters	Description		7C510-45		7C510-55		7C510-65		7C510-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply Accumulate Time			45		55		65		75	ns
t_S	Setup Time		20		20		25		25		ns
t_H	Hold Time		3		3		3		3		ns
t_{PW}	Clock Pulse Width		25		25		30		30		ns
t_{PDP}	Output Clock to P			30		30		35		35	ns
t_{PDY}	Output Clock to Y			30		30		35		35	ns
t_{PHZ}	$\overline{OEX}$, $\overline{OEM}$ to P; $\overline{OEL}$ to Y (Disable Time)	HIGH to Z		25		25		30		30	ns
t_{PLZ}		LOW to Z		25		25		30		30	ns
t_{PZH}	$\overline{OEX}$, $\overline{OEM}$ to P; $\overline{OEL}$ to Y (Enable Time)	Z to HIGH		30		30		35		35	ns
t_{PZL}		Z to LOW		30		30		35		35	ns
t_{HCL}	Relative Hold Time		0		0		0				ns

Test Waveforms



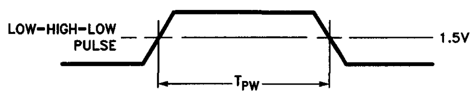
0057-7

Setup and Hold Time



0057-8

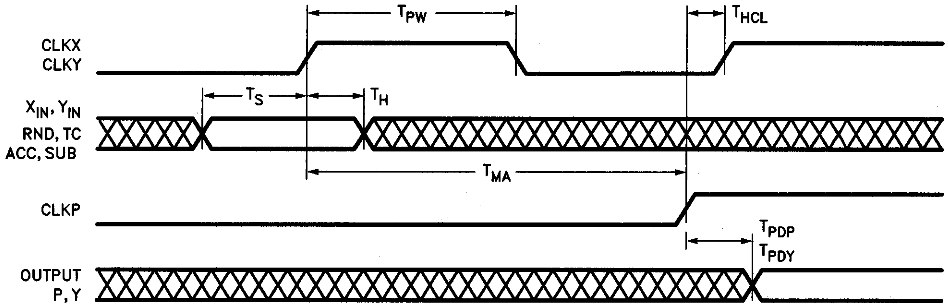
Pulse Width



0057-9

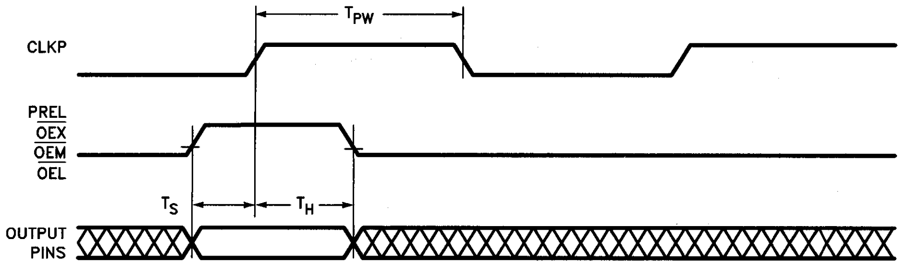
Notes:
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.
3. See the last page of this specification for Group A subgroup testing information.

CY7C510 Timing Diagram



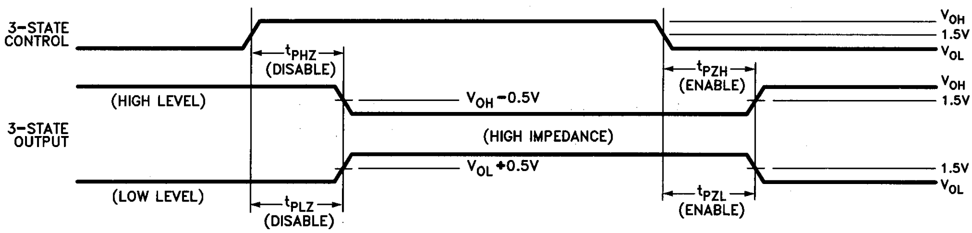
0057-10

Preload Timing Diagram



0057-11

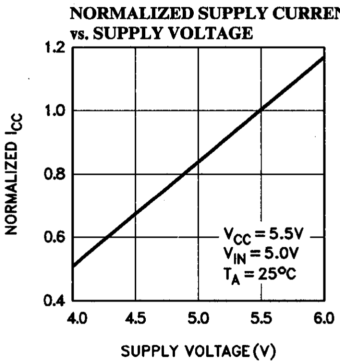
Three-State Timing Diagram

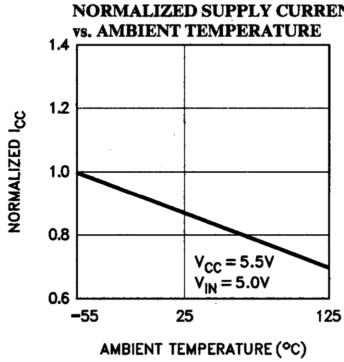


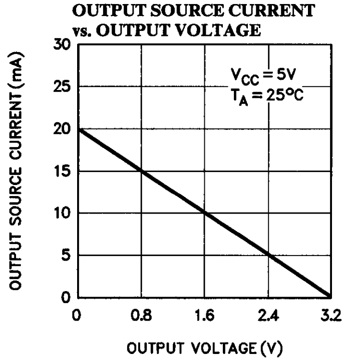
0057-12

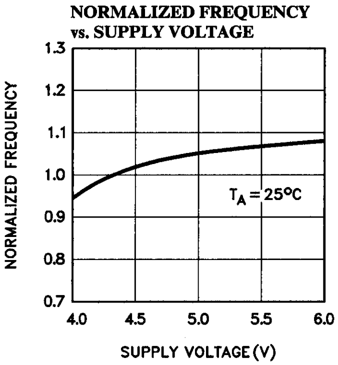
6

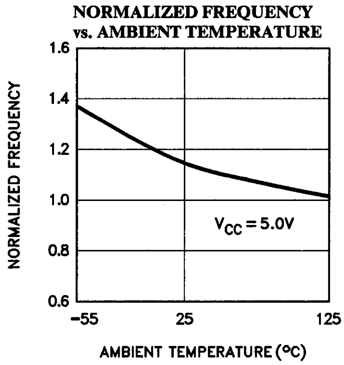
Typical AC and DC Characteristics

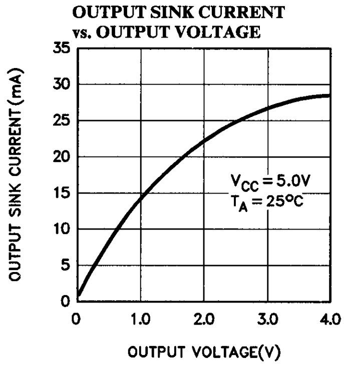


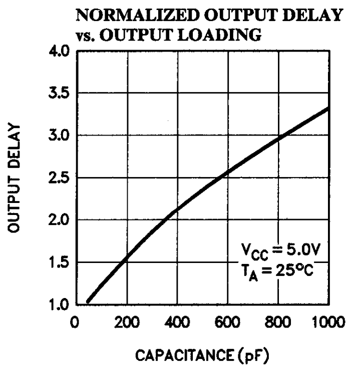


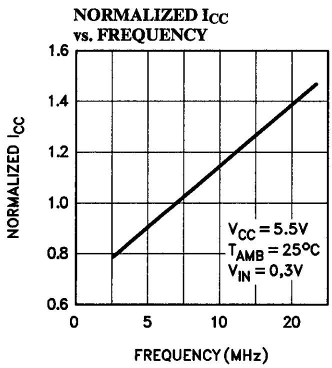












0057–14

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
45	CY7C510-45 PC	P29	Commercial
	CY7C510-45 LC	L81	
	CY7C510-45 JC	J81	
	CY7C510-45 DC	D30	
	CY7C510-45 GC	G68	
55	CY7C510-55 PC	P29	Commercial
	CY7C510-55 LC	L81	
	CY7C510-55 JC	J81	
	CY7C510-55 DC	D30	
	CY7C510-55 GC	G68	
	CY7C510-55 LMB	L81	Military
	CY7C510-55 DMB	D30	
	CY7C510-55 GMB	G68	
65	CY7C510-65 PC	P29	Commercial
	CY7C510-65 LC	L81	
	CY7C510-65 JC	J81	
	CY7C510-65 DC	D30	
	CY7C510-65 GC	G68	
	CY7C510-65 LMB	L81	Military
	CY7C510-65 DMB	D30	
	CY7C510-65 GMB	G68	
75	CY7C510-75 PC	P29	Commercial
	CY7C510-75 LC	L81	
	CY7C510-75 JC	J81	
	CY7C510-75 DC	D30	
	CY7C510-75 GC	G68	
	CY7C510-75 LMB	L81	Military
	CY7C510-75 DMB	D30	
	CY7C510-75 GMB	G68	

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{OH}	1,2,3
I_{OL}	1,2,3
I_{IX}	1,2,3
I_I	1,2,3
I_{OS}	1,2,3
I_{OZL}	1,2,3
I_{OZH}	1,2,3

Parameters	Subgroups
I_{CC} (Q1)	1,2,3
I_{CC} (Q2)	1,2,3
I_{CC} (Max.)	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{MA}	7,8,9,10,11
t_S	7,8,9,10,11
t_H	7,8,9,10,11
t_{PW}	7,8,9,10,11
t_{PDP}	7,8,9,10,11
t_{PDY}	7,8,9,10,11
t_{PHZ}	7,8,9,10,11
t_{PLZ}	7,8,9,10,11
t_{PZH}	7,8,9,10,11
t_{PZL}	7,8,9,10,11
t_{HCL}	7,8,9,10,11

Document #: 38-00014-B

CY7C516
CY7C517

16 x 16 Multipliers

Features

- **Fast**
  - **— 38 ns clock cycle (commercial)**
  - **— 42 ns clock cycle (military)**
- **Low Power**
  - **— I_{CC} (max. at 10 MHz) = 100 mA (commercial)**
  - **— I_{CC} (max. at 10 MHz) = 110 mA (military)**
- **V_{CC} Margin**
  - **— 5V ±10%**
  - **— All parameters guaranteed over commercial and military operating temperature range**
- **16 x 16 bit parallel multiplication with full precision 32-bit product output**
- **Two's complement, unsigned magnitude, or mixed mode multiplication**
- **CY7C516 pin compatible and functionally equivalent to Am29516, MPY016K, MPY016H**
- **CY7C517 pin compatible and functionally equivalent to Am29517**

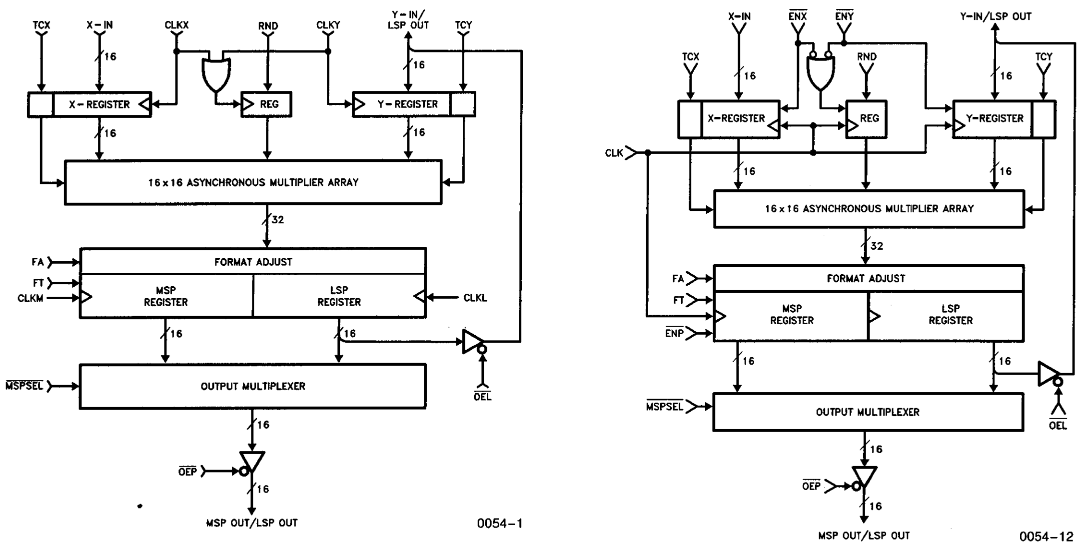
Functional Description

The CY7C516/517 are high-speed 16 x 16 parallel multipliers which operate at 38 ns clocked multiply times (26 MHz multiplication rate). The two input operands may be independently specified as either two's complement or unsigned magnitude numbers. Controls are provided for rounding and format adjustment of the full precision 32-bit product.

On the 7C516, individually clocked input and output registers are provided to maximize throughput and to simplify bus interfacing. On the 7C517, a single clock (CLK) is provided, along with three register enables. This facilitates the use of the 7C517 in microprogrammed systems. The input and output registers are positive edge triggered D-type flip-flops. The output register may be made transparent for asynchronous output.

Logic Block Diagrams

CY7C516 CY7C517



Selection Guide

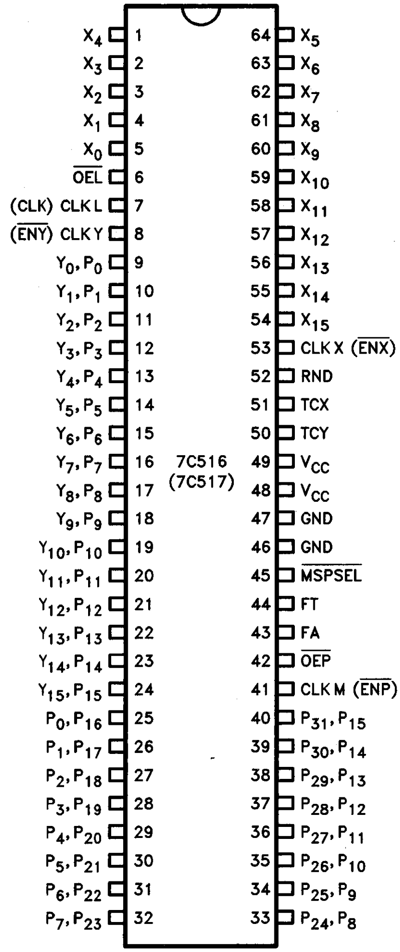
		7C516-38 7C517-38	7C516-42 7C517-42	7C516-45 7C517-45	7C516-55 7C517-55	7C516-75 7C517-75
Maximum Multiply Time (ns) Clocked/Unclocked	Commercial	38/58		45/65	55/75	75/100
	Military		42/65		55/75	75/100

Functional Description (Continued)

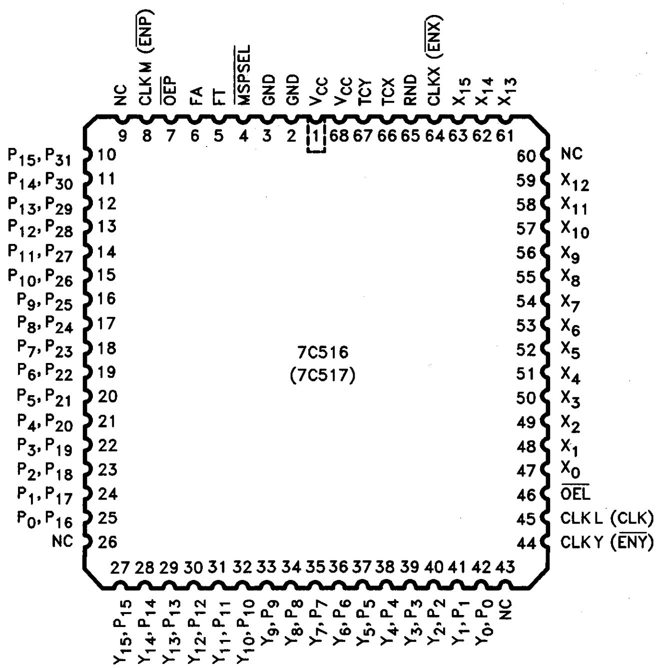
Two output modes may be selected by using the output multiplexer control, $\overline{\text{MSPSEL}}$. Holding $\overline{\text{MSPSEL}}$ LOW causes the most significant product (MSP) to be available at the dedicated output port. The LSP is simultaneously available at the bidirectional port shared with the Y-inputs.

The other mode of output involves toggling of the $\overline{\text{MSPSEL}}$ control, allowing both the MSP and LSP to be available for output through the dedicated 16-bit output port.

Pin Configurations



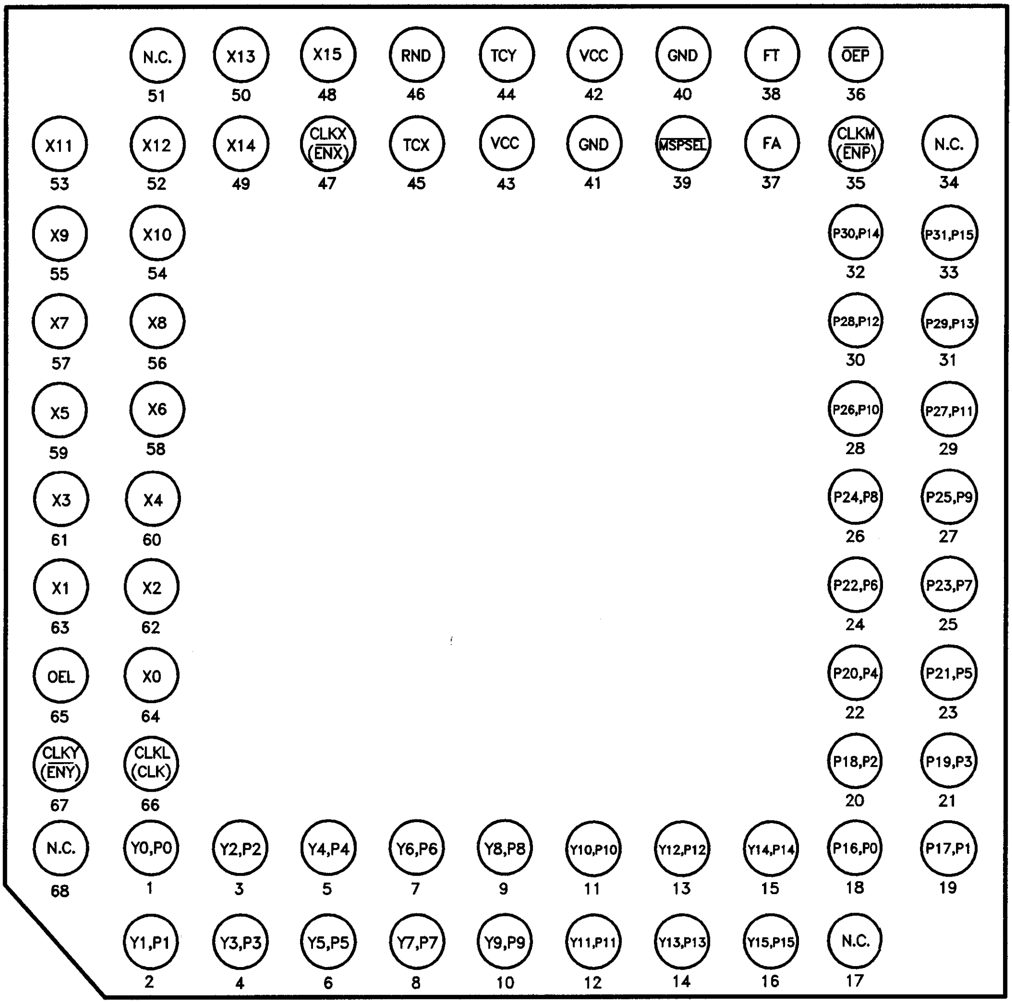
0054–2



0054–3

Pin Configurations (Continued)

Pin Configuration for 68-Pin Grid Array



0054–16

6

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Ambient Temperature Under Bias .... $-55°C$ to $+125°C$

Supply Voltage to Ground Potential .... $-0.5V$ to $+7.0V$

DC Input Voltage .... $-0.5V$ to $+7.0V$

DC Voltage Applied to Outputs ..... $-0.5V$ to V_{CC} Max.

Output Current, into Outputs (low).............. 10 mA

Static Discharge Voltage .... > 1000V
(per MIL-STD-883 Method 3015)

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

Note:
1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
X_{15-0}	I	**X-Input Data.** This 16-bit number may be interpreted as two's complement or unsigned magnitude.
Y_{15-0} (P_{15-0})	I/O	**Y-Input/LSP Output Data.** This 16-bit number may be interpreted as two's complement or unsigned magnitude. The Y-input port may be multiplexed with the LSP output (P_{15-0}).
P_{31-16} (P_{15-0})	O	**Output Data.** This 16-bit port may carry either the MSP (P_{31-16}) or the LSP (P_{15-0}).
FT	I	The MSP and LSP registers are made transparent (asynchronous operation) if FT is HIGH.
FA	I	**Format Adjust Control.** If FA is HIGH, a full 32-bit product is output. If FA is LOW, a left-shifted product is output, with the sign bit replicated in the LSP. FA must be HIGH for two's complement integer, unsigned magnitude, and mixed mode multiplication.
$\overline{\text{MSPSEL}}$	I	**Output Multiplexer Control.** When $\overline{\text{MSPSEL}}$ is LOW, the MSP is available for output at the MSP output port, and the LSP is available at the Y-input/LSP output port. When $\overline{\text{MSPSEL}}$ is HIGH, the LSP is available at both ports (above) and the MSP is not available.
RND	I	**Round Control.** When RND is HIGH, a one is added to the MSB of the LSP. This position is dependent on the FA control; FA = HIGH means RND adds to the 2^{-15} bit (P_{15}), FA = LOW means RND adds to the 2^{-16} bit (P_{14}).
TCX	I	**Two's Complement Control X.** X-input data are interpreted as two's complement when TCX is HIGH. TCX LOW means the data are interpreted as unsigned magnitude.

Signal Name	I/O	Description
TCY	I	**Two's Complement Control Y.** Y-Input data are interpeted as two's complement when TCY is HIGH. TCY LOW means the data are interpreted as unsigned magnitude.
$\overline{\text{OEP}}$	I	**P_{31-16}/P_{15-0} Output Port Three-State Control.** When $\overline{\text{OEP}}$ is LOW, the output port is enabled; when $\overline{\text{OEP}}$ is HIGH, the drivers are in a high impedance state.
$\overline{\text{OEL}}$	I	**Y-in/P_{15-0} Port Three State Control.** When $\overline{\text{OEL}}$ is LOW, the timeshared port is enabled for LSP output. When $\overline{\text{OEL}}$ is HIGH, the output drivers are in a high impedance state. This is required for Y-input.
CY7C516 Only		
CLKX	I	**X-Register Clock.** X-input data and TCX are latched in at the rising edge of CLKX.
CLKY	I	**Y-Register Clock.** Y-input data and TCY are latched in at the rising edge of CLKY.
CLKM	I	**MSP Register Clock.** The most significant product (MSP) is latched in at the MSP Register at the rising edge of CLKM.
CLKL	I	**LSP Register Clock.** The least significant product (LSP) is latched in at the LSP Register at the rising edge of CLKL.
CY7C517 Only		
CLK	I	**Clock.** All enabled registers latch in their data at the rising edge of CLK.
$\overline{\text{ENX}}$	I	**X-Register Enable.** When $\overline{\text{ENX}}$ is LOW, the X-Register is enabled. X-input data and TCX will be latched in at the rising edge of CLK when the register is enabled. When $\overline{\text{ENX}}$ is HIGH, the X-Register is in hold mode.
$\overline{\text{ENY}}$	I	**X-Register Enable.** $\overline{\text{ENY}}$ enables the Y-Register. (See $\overline{\text{ENX}}$.)
$\overline{\text{ENP}}$	I	**Product Register Enable.** $\overline{\text{ENP}}$ enables the product register. Both the MSP and LSP Sections are enabled by $\overline{\text{ENP}}$. (See $\overline{\text{ENX}}$.)

Input Formats (All Devices)

Fractional Two's Complement Input Format

TCX, TCY = 1

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0} (Sign)	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0} (Sign)	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Integer Two's Complement Input Format

TCX, TCY = 1

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15} (Sign)	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15} (Sign)	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Input Format

TCX, TCY = 0

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

Unsigned Integer Input Format

TCX, TCY = 0

X_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Y_{IN}

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Output Formats (All Devices)

Fractional Two's Complement (Shifted)* Format

FA = 0

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
(Sign)															

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}
(Sign)															

Fractional Two's Complement Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}
(Sign)															

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}

Integer Two's Complement Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
-2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
(Sign)															

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Unsigned Fractional Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}	2^{-32}

Unsigned Integer Output

FA = 1

MSP

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}

LSP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

*In this format an overflow occurs in the attempted multiplication of the two's complement number 1.000 . . . (−1) with itself, yielding a product of 1.000 . . . or −1.

Electrical Characteristics Over Operating Range[4]

Parameters	Description		Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = Min., I_{OH} = −0.4 mA	2.4		V
V_{OL}	Output LOW Voltage		V_{CC} = Min., I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage			2.0		V
V_{IL}	Input LOW Voltage				0.8	V
I_{OH}	Output HIGH Current		V_{CC} = Min., V_{OH} = 2.4V	−0.4		mA
I_{OL}	Output LOW Current		V_{CC} = Min., V_{OL} = 0.4V	4.0		mA
I_{IX}	Input Leakage Current		$V_{SS} \leq V_{IN} \leq V_{CC}$, V_{CC} = Max.	−10	10	μA
I_{OS}[1]	Output Short Circuit Current		V_{CC} = Max., V_{OUT} = 0V	−3	−30	mA
I_{OZL}	Output OFF (Hi-Z) Current		V_{CC} = Max., $\overline{OE}$ = 2.0V		−25	μA
I_{OZH}	Output OFF (Hi-Z) Current		V_{CC} = Max., $\overline{OE}$ = 2.0V	25		μA
I_{CC} (Q_1)[2]	Supply Current (Quiescent)	Commercial (-38)	GND $\leq V_{IN} \leq V_{IL}$ or $V_{IH} \leq V_{IN} \leq V_{CC}$; $\overline{OE}$ = HIGH		40	mA
		Military (-42)			45	
		All Others			30	
I_{CC} (Q_2)[2]	Supply Current (Quiescent)	Commercial	GND $\leq V_{IN} \leq$ 0.4V or 3.85V $\leq V_{IN} \leq V_{CC}$; $\overline{OE}$ = HIGH		20	mA
		Military			25	
I_{CC} (Max.)[2]	Supply Current	Commercial	V_{CC} = Max., f_{CLK} = 10 MHz; $\overline{OE}$ = HIGH		100	mA
		Military			110	

6

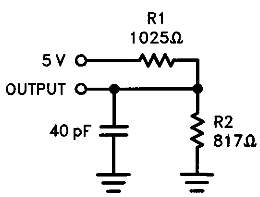
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	

Notes:
1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given clock frequency, use 30 mA + I_{CC} (A.C.), where I_{CC} (A.C.) = (7 mA/MHz) × Clock Frequency for the Commercial temperature range. I_{CC} (A.C.) = (8 mA/MHz) × Clock Frequency for the Military temperature range.
3. Tested initally and after any design or process changes that may affect these parameters.
4. See the last page of this specification for Group A subgroup testing information.

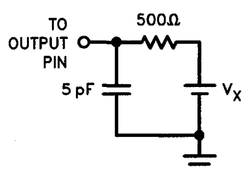
Output Loads Used for A.C. Performance Characteristics

Normal Load (Load 1)



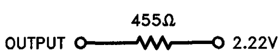
0054-4

Three-State Delay Load (Load 2)



0054-5

Equivalent to: THÉVENIN EQUIVALENT



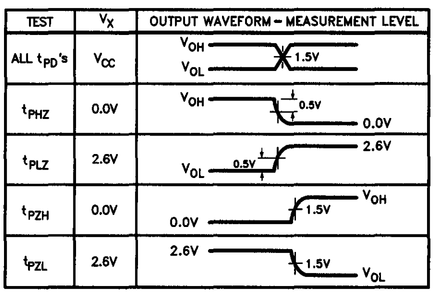
0054-6

Switching Characteristics Over Operating Range[2]

Parameters	Description	Test Conditions	7C516-38 7C517-38 Min.	Max.	7C516-42 7C517-42 Min.	Max.	7C516-45 7C517-45 Min.	Max.	7C516-55 7C517-55 Min.	Max.	7C516-75 7C517-75 Min.	Max.	Units
t_{MUC}	Unclocked Multiply Time	Load 1		58		65		65		75		100	ns
t_{MC}	Clocked Multiply Time	Load 1		38		42		45		55		75	ns
t_S	X_i, Y_i, RND, TCX, TCY Set-up Time	Load 1	7		8		20		20		25		ns
t_H	X_i, Y_i, RND, TCX, TCY Hold Time	Load 1	3		3		3		3		3		ns
t_{SE}	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Set-up Time (7C517 Only)	Load 1	10		15		20		20		25		ns
t_{HE}	$\overline{ENX}$, $\overline{ENY}$, $\overline{ENP}$ Hold Time (7C517 Only)	Load 1	3		3		3		3		3		ns
t_{PWH}, t_{PWL}	Clock Pulse Width (HIGH and LOW)	Load 1	10		10		20		25		30		ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out	Load 1		18		21		25		25		30	ns
t_{PDP}	Output Clock to P	Load 1		25		30		30		30		35	ns
t_{PDY}	Output Clock to Y	Load 1		25		30		30		30		35	ns
t_{PHZ}	$\overline{OEP}$ Disable Time, HIGH to Z	Load 2		15		17		25		25		30	ns
t_{PLZ}	$\overline{OEP}$ Disable Time, LOW to Z	Load 2		15		17		25		25		30	ns
t_{PZH}	$\overline{OEP}$ Enable Time, Z to HIGH	Load 2		23		25		30		30		35	ns
t_{PZL}	$\overline{OEP}$ Enable Time, Z to LOW	Load 2		23		25		30		30		35	ns
t_{PHZ}	$\overline{OEL}$ Disable Time, HIGH to Z	Load 2		15		17		25		25		30	ns
t_{PLZ}	$\overline{OEL}$ Disable Time, LOW to Z	Load 2		15		17		25		25		30	ns
t_{PZH}	$\overline{OEL}$ Enable Time, Z to HIGH	Load 2		23		25		30		30		35	ns
t_{PZL}	$\overline{OEL}$ Enable Time, Z to LOW	Load 2		23		25		30		30		35	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML[1]	Load 1	0		0		0		0		0		ns

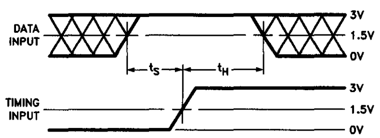
Notes:
1. To ensure that the correct product is entered in the output registers, new data may not be entered into the input registers before the output registers have been clocked.
2. See the last page of this specification for Group A subgroup testing information.

Test Waveforms (All Devices)



0054-7

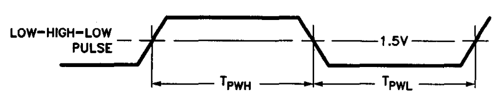
Setup and Hold Time (All Devices)



0054-8

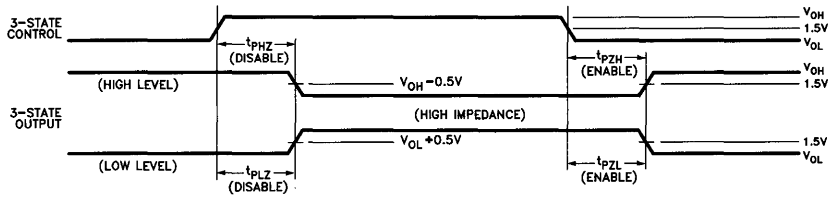
Notes:
1. Diagram shown for HIGH data only. Output transition may be opposite sense.
2. Cross hatched area is don't care condition.

Pulse Width (All Devices)



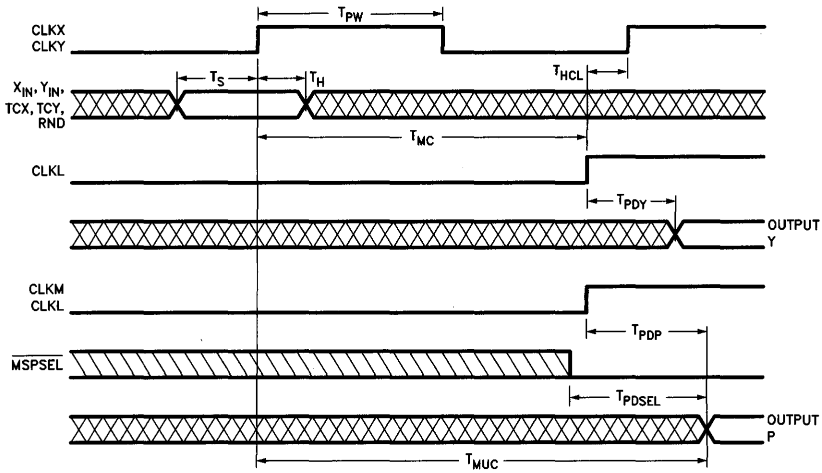
0054-9

Three-State Timing Diagram



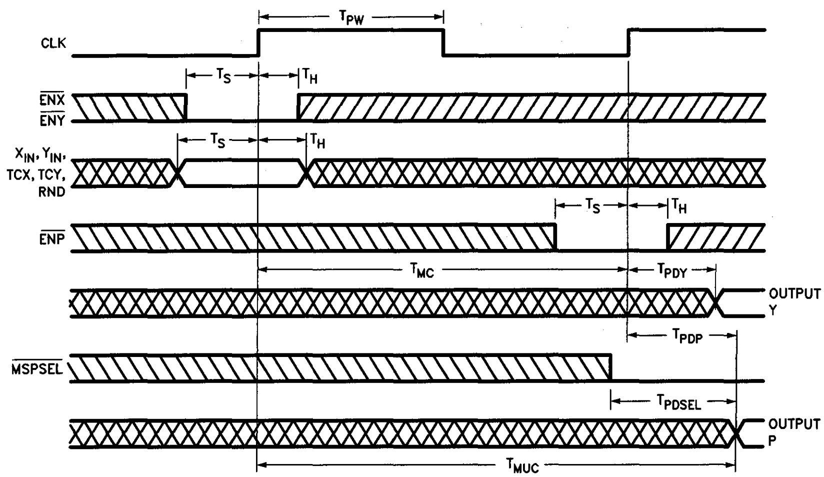
0054-10

Timing Diagram 7C516



0054-11

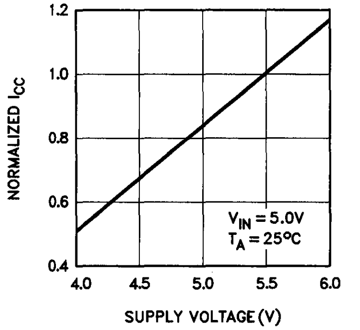
Timing Diagram 7C517



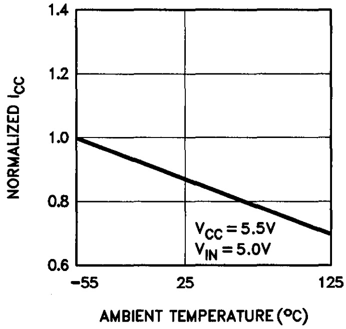
0054-15

Typical DC and AC Characteristics

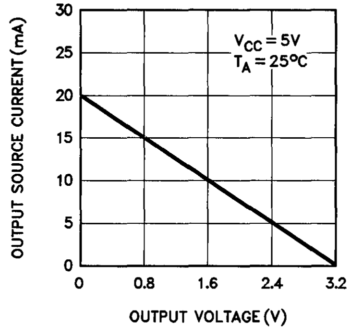
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



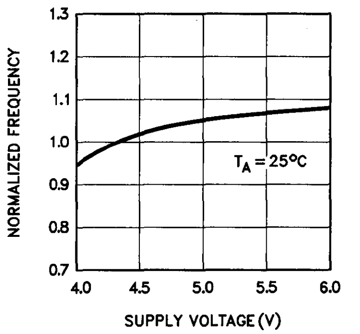
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



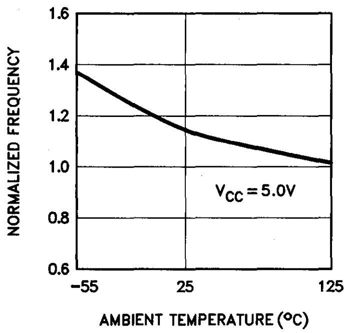
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



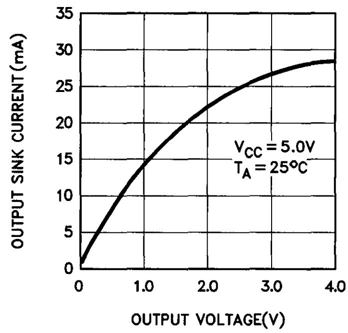
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



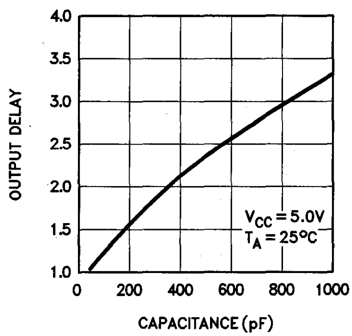
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



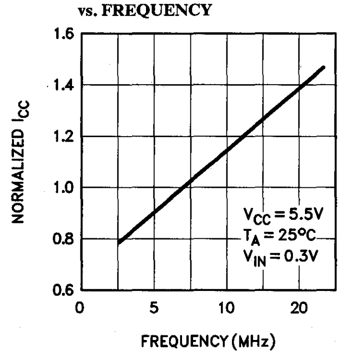
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED CURRENT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0054–17

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
38	CY7C516-38PC CY7C517-38PC	P29	Commercial
	CY7C516-38LC CY7C517-38LC	L81	
	CY7C516-38JC CY7C517-38JC	J81	
	CY7C516-38DC CY7C517-38DC	D30	
	CY7C516-38GC CY7C517-38GC	G68	
42	CY7C516-42LMB CY7C517-42LMB	L81	Military
	CY7C516-42DMB CY7C517-42DMB	D30	
	CY7C516-42GMB CY7C517-42GMB	G68	
45	CY7C516-45PC CY7C517-45PC	P29	Commercial
	CY7C516-45LC CY7C517-45LC	L81	
	CY7C516-45JC CY7C517-45JC	J81	
	CY7C516-45DC CY7C517-45DC	D30	
	CY7C516-45GC CY7C517-45GC	G68	

Speed (ns)	Ordering Code	Package Type	Operating Range
55	CY7C516-55PC CY7C517-55PC	P29	Commercial
	CY7C516-55LC CY7C517-55LC	L81	
	CY7C516-55JC CY7C517-55JC	J81	
	CY7C516-55DC CY7C517-55DC	D30	
	CY7C516-55GC CY7C517-55GC	G68	
	CY7C516-55LMB CY7C517-55LMB	L81	Military
	CY7C516-55DMB CY7C517-55DMB	D30	
	CY7C516-55GMB CY7C517-55GMB	G68	
75	CY7C516-75PC CY7C517-75PC	P29	Commercial
	CY7C516-75LC CY7C517-75LC	L81	
	CY7C516-75JC CY7C517-75JC	J81	
	CY7C516-75DC CY7C517-75DC	D30	
	CY7C516-75GC CY7C517-75GC	G68	
	CY7C516-75LMB CY7C517-75LMB	L81	Military
	CY7C516-75DMB CY7C517-75DMB	D30	
	CY7C516-75GMB CY7C517-75GMB	G68	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL}	1,2,3
I_{OH}	1,2,3
I_{OL}	1,2,3
I_{IX}	1,2,3
I_{OS}	1,2,3
I_{OZL}	1,2,3
I_{OZH}	1,2,3
I_{CC} (Q_1)	1,2,3

Parameters	Subgroups
I_{CC} (Q_2)	1,2,3
I_{CC} (Max.)	1,2,3

Switching Characteristics

Parameters	Subgroups
t_{MUC}	7,8,9,10,11
t_{MC}	7,8,9,10,11
t_S	7,8,9,10,11
t_H	7,8,9,10,11
t_{SE}	7,8,9,10,11
t_{HE}	7,8,9,10,11
t_{PWH}, t_{PWL}	7,8,9,10,11
t_{PDSEL}	7,8,9,10,11
t_{PDP}	7,8,9,10,11
t_{PDY}	7,8,9,10,11
t_{PHZ}	7,8,9,10,11
t_{PLZ}	7,8,9,10,11
t_{PZH}	7,8,9,10,11
t_{PZL}	7,8,9,10,11
t_{PHZ}	7,8,9,10,11
t_{PLZ}	7,8,9,10,11
t_{PZH}	7,8,9,10,11
t_{PZL}	7,8,9,10,11
t_{HCL}	7,8,9,10,11

Document #: 38-00018-C

CY7C901

CMOS Four-Bit Slice

Features

- **Fast**
  CY7C901-23 has a 23 ns Read Modify-Write Cycle; Commercial 25% Faster than "C" Spec 2901
  CY7C901-27 has a 27 ns Read Modify-Write Cycle; Military 15% Faster than "C" Spec 2901
- **Low Power**
  70 mA (commercial)
  90 mA (military)
- **V_{CC} 5V ±10%**
  Commercial and military
- **Eight Function ALU**
- **Infinitely expandable in 4-bit increments**
- **Four Status Flags: Carry, overflow, negative, zero**
- **Capable of withstanding greater than 2000V static discharge voltage**
- **Pin Compatible and Functional Equivalent to Am2901B, C**

Functional Description

The CY7C901 is a high-speed, expandable, 4-bit wide ALU that can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C901 is basic but yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C901, as illustrated in the block diagram, consists of a 16-word by 4-bit dual-port RAM register file, a 4-bit ALU and the required data manipulation and control logic.

The operation performed is determined by nine input control lines (I_0 to I_8) that are usually inputs from a microinstruction register.

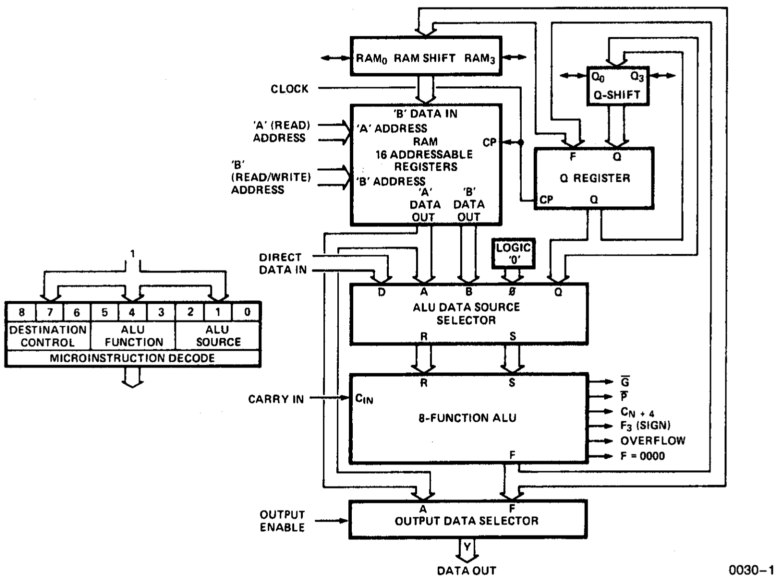
The CY7C901 is expandable in 4-bit increments, has three-state data outputs as well as flag output, and can use either a full look ahead carry or a ripple carry.

The CY7C901 is a pin compatible, functional equivalent, improved performance replacement for the Am2901.

The CY7C901 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection over 2000V and achieves superior performance with low power dissipation.

6

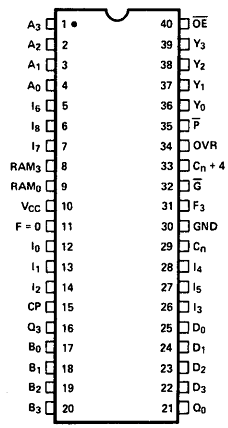
Logic Block Diagram



0030-1

Pin Configuration

Top View



0030-2

Selection Guide

See last page for ordering information.

Read Modify-Write Cycle (Min.) in ns	Operating I_{CC} (Max.) in mA	Operating Range	Part Number
23	80	Commercial	CY7C901-23
27	90	Military	CY7C901-27
31	70	Commercial	CY7C901-31
32	90	Military	CY7C901-32

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30).................... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015)

Latchup Current (Outputs).................. >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[1]	−55°C to +125°C	5V ± 10%

Note:

1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
A_0–A_3	I	These 4 address lines select one of the registers in the stack and output its contents on the (internal) A port.
B_0–B_3	I	These 4 address lines select one of the registers in the stack and output is contents on the (internal) B port. This can also be the destination address when data is written back into the register file.
I_0–I_8	I	These 9 instruction lines select the ALU data sources ($I_{0, 1, 2}$), the operation to be performed ($I_{3, 4, 5}$) and what data is to be written into either the Q register or the register file ($I_{6, 7, 8}$).
D_0–D_3	I	These are 4 data input lines that may be selected by the $I_{0, 1, 2}$ lines as inputs to the ALU.
Y_0–Y_3	O	These are three-state data output lines that, when enabled, output either the output of the ALU or the data in the A latches, as determined by the code on the $I_{6, 7, 8}$ lines.
$\overline{OE}$	I	Output Enable. This is an active LOW input that controls the Y_0–Y_3 outputs. When this signal is LOW the Y outputs are enabled and when it is HIGH they are in the high impedance state.
CP	I	Clock Input. The LOW level of the clock write data to the 16 x 4 RAM. The HIGH level of the clock writes data from the RAM to the A-port and B-port latches. The operation of the Q register is similar. Data is entered into the master latch on the LOW level of the clock and transferred from master to slave when the clock is HIGH.
Q_3 RAM_3	I/O	These two lines are bidirectional and are controlled by the $I_{6, 7, 8}$ inputs. Electrically they are three-state output drivers connected to the TTL compatible CMOS inputs.

Signal Name	I/O	Description
Q_3 RAM_3 (Cont.)	I/O	**Outputs:** When the destination code on lines $I_{6, 7, 8}$ indicates a shift left (UP) operation the three-state outputs are enabled and the MSB of the Q register is output on the Q_3 pin and the MSB of the ALU output (F_3) is output on the RAM 3 pin. **Inputs:** When the destination code indicates a shift right (DOWN) the pins are the data inputs to the MSB of the Q register and the MSB of the RAM.
Q_0 RAM_0	I/O	These two lines are bidirectional and function in a manner similar to the Q_3 and RAM_3 lines, except that they are the LSB of the Q register and RAM.
C_n	I	The carry-in to the internal ALU.
C_{n+4}	O	The carry-out from the internal ALU.
$\overline{G}$, $\overline{P}$	O	The carry generate and the carry propagate outputs of the ALU, which may be used to perform a carry look-ahead operation over the 4-bits of the ALU.
OVR	O	Overflow. This signal is logically the exclusive-OR of the carry-in and the carry-out of the MSB of the ALU. This pin indicates that the result of the ALU operation has exceeded the capacity of the machine. It is valid only for the sign bit and assumes two's complement coding for negative numbers.
F = 0	O	Open drain output that goes HIGH if the data on the ALU outputs ($F_{0, 1, 2, 3}$) are all LOW. It indicates that the result of an ALU operation is zero (positive logic).
F_3	O	The most significant bit of the ALU output.

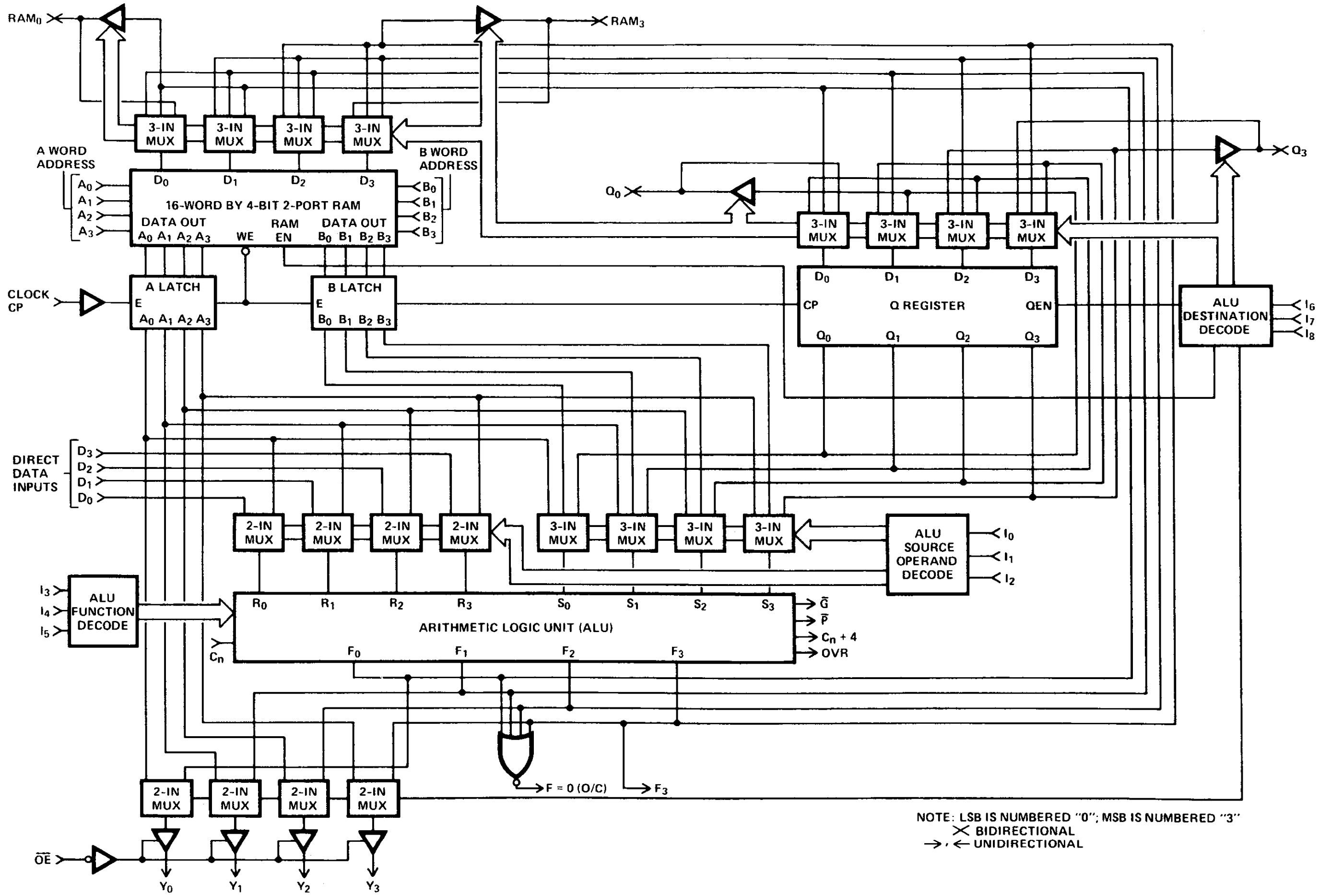


Figure 1. CY7C901 Block Diagram

Functional Tables

Mnemonic	Micro Code				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Figure 2. ALU Source Operand Control

Mnemonic	Micro Code				ALU Function	Symbol
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	$R + S$
SUBR	L	L	H	1	S Minus R	$S - R$
SUBS	L	H	L	2	R Minus S	$R - S$
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \veebar S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Figure 3. ALU Function Control

Mnemonic	Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	None	None	$F \rightarrow Q$	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	$F \rightarrow B$	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	$F \rightarrow B$	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	$F/2 \rightarrow B$	DOWN	$Q/2 \rightarrow Q$	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	$F/2 \rightarrow B$	X	None	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	$2F \rightarrow B$	UP	$2Q \rightarrow Q$	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	$2F \rightarrow B$	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
A = Register Addressed by A inputs.
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control

	I_{210} Octal	0	1	2	3	4	5	6	7
Octal I_{543}	ALU Source / ALU Function	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	$C_n = L$	$A+Q$	$A+B$	Q	B	A	$D+A$	$D+Q$	D
	R plus S								
	$C_n = H$	$A+Q+1$	$A+B+1$	$Q+1$	$B+1$	$A+1$	$D+A+1$	$D+Q+1$	$D+1$
1	$C_n = L$	$Q-A-1$	$B-A-1$	$Q-1$	$B-1$	$A-1$	$A-D-1$	$Q-D-1$	$-D-1$
	S minus R								
	$C_n = H$	$Q-A$	$B-A$	Q	B	A	$A-D$	$Q-D$	$-D$
2	$C_n = L$	$A-Q-1$	$A-B-1$	$-Q-1$	$-B-1$	$-A-1$	$D-A-1$	$D-Q-1$	$D-1$
	R minus S								
	$C_n = H$	$A-Q$	$A-B$	$-Q$	$-B$	$-A$	$D-A$	$D-Q$	D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

$+$ = Plus; $-$ = Minus; $\vee$ = OR; $\wedge$ = AND; $\veebar$ = EX-OR

Figure 5. Source Operand and ALU Function Matrix

Description of Architecture

General Description

A block diagram of the CY7C901 is shown in *Figure 1.* The circuit is a 4-bit slice consisting of a register file (16 x 4 dual port RAM), the ALU, the Q register and the necessary control logic. It is expandable in 4-bit increments.

RAM

The RAM is addressed by two 4-bit address fields (A_0-A_3, B_0-B_3) that cause the data to appear at the A or B (internal) ports. If the A and B addresses are the same, the data at the A and B ports will be identical.

New data is written into the RAM location specified by the B address when the RAM write enable (RAM EN) is active and the clock input is LOW. Each of the four RAM inputs is driven by a 3-input multiplexer that allows the outputs of the ALU ($F_{0, 1, 2, 3,}$) to be shifted one bit position to the left, the right, or not to be shifted. The other inputs to the multiplexer are from the RAM_3 and RAM_0 I/O pins.

For a shift left (up) operation, the RAM_3 output buffer is enabled and the RAM_0 multiplexer input is enabled. For a shift right (down) operation the RAM_0 output buffer is enabled and the RAM_3 multiplexer input is enabled.

The data to be written into the RAM is applied to the D inputs of the CY7C901 and is passed (unchanged) through the ALU to the RAM location addressed by the B word address.

The outputs of the RAM A and B ports drive separate 4-bit latches that are enabled (follow the RAM data) when the clock is HIGH. The outputs of the A latches go to three multiplexers whose outputs drive the two inputs to the ALU ($R_{0, 1, 2, 3}$) and ($S_{0, 1, 2, 3}$) and the ($Y_{0, 1, 2, 3}$) chip outputs.

ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on two 4-bit input words, R and S. The R inputs are driven from four 2-input multiplexers whose inputs are from either the (RAM) A-port or the external data (D) inputs. The S inputs are driven from four 3-input multiplexers whose inputs are from the A-port, the B-port, or the Q register. Both multiplexers are controlled by the $I_{0, 1, 2}$ inputs as shown in *Figure 2.* This configuration of multiplexers on the ALU R and S inputs enables the user to select eight pairs of combinations of A, B, D, Q and "0" (unselected) inputs as 4-bits operands to the ALU. The logical and arithmetic operations performed by the ALU upon the data present at its R and S inputs are tabulated in *Figure 3.* The ALU has a carry-in (C_n) input, carry-propagate ($\overline{P}$) output, carry-generate ($\overline{G}$) output, carry-out ($C_n + 4$) and overflow (OVR) pins to enable the user to (1) speed up arithmetic operations by implementing carry look-ahead logic and (2) determine if an arithmetic overflow has occurred.

The ALU data outputs ($F_{0, 1, 2, 3}$) are routed to the RAM, the Q register inputs and the Y outputs under control of the $I_{6, 7, 8}$ control signal inputs as shown in *Figure 4.* In addition, the MSB of the ALU is output as F3 so that the user can examine the sign bit without enabling the three-state outputs. The F = 0 output, used for zero detection, is HIGH when all bits of the F output are LOW. It is an open-drain output which may be wire OR'ed across multiple 7C901 processor slices.

Q Register

The Q register functions as an accumulator or temporary storage register. Physically it is a 4-bit register implemented with master-slave latches. The inputs to the Q register are driven by the outputs from four 3-input multiplexers under control of the $I_{6, 7, 8}$ inputs. The Q_0 and Q_3 I/O pins function in a manner similar to the RAM_0 and RAM_3 pins. The other inputs to the multiplexer enable the contents of the Q register to be shifted up or down, or the outputs of the ALU to be entered into the master latches. Data is entered into the master latches when the clock is LOW and transferred from master to slave (output) when the clock changes from LOW to HIGH.

ALU Source Operand and ALU Functions

The ALU source operands and ALU function matrix is summarized in *Figure 5* and separated by logic operation or arithmetic operation in *Figures 6* and *7*, respectively. The $I_{0, 1, 2}$ lines select eight pairs of source operands and the $I_{3, 4, 5}$ lines select the operation to be performed. The carry-in (C_n) signal affects the arithmetic result and the internal flags; not the logical operations.

Conventional Addition and Pass-Increment/Decrement

When the carry-in is HIGH and either a conventional addition or a PASS operation is performed, one (1) is added to the result. If the DECREMENT operation is performed when the carry-in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry-in is HIGH, it nullifies the DECREMENT operation so that the result is equivalent to the PASS operation.

Octal I_{543}, I_{210}	Group	Function
4 0 4 1 4 5 4 6	AND	$A \wedge Q$ $A \wedge B$ $D \wedge A$ $D \wedge Q$
3 0 3 1 3 5 3 6	OR	$A \vee Q$ $A \vee B$ $D \vee A$ $D \vee Q$
6 0 6 1 6 5 6 6	EX-OR	$A \forall Q$ $A \forall B$ $D \forall A$ $D \forall Q$
7 0 7 1 7 5 7 6	EX-NOR	$\overline{A \forall Q}$ $\overline{A \forall B}$ $\overline{D \forall A}$ $\overline{D \forall Q}$
7 2 7 3 7 4 7 7	INVERT	$\overline{Q}$ $\overline{B}$ $\overline{A}$ $\overline{D}$
6 2 6 3 6 4 6 7	PASS	Q B A D
3 2 3 3 3 4 3 7	PASS	Q B A D
4 2 4 3 4 4 4 7	"ZERO"	0 0 0 0
5 0 5 1 5 5 5 6	MASK	$\overline{A} \wedge Q$ $\overline{A} \wedge B$ $\overline{D} \wedge A$ $\overline{D} \wedge Q$

Figure 6. ALU Logic Mode Functions

Subtraction

Recall that in two's complement integer coding −1 is equal to all ones and that in one's complement integer coding zero is equal to all ones. To convert a positive integer to its two's complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e., TWC = ONC + 1. In *Figure 7* the symbol −Q represents the two's complement of Q so that the one's complement of Q is then −Q −1.

Octal I_{543}, I_{210}	$C_n = 0$ (Low)		$C_n = 1$ (High)	
	Group	Function	Group	Function
0 0 0 1 0 5 0 6	ADD	A+Q A+B D+A D+Q	ADD plus one	A+Q+1 A+B+1 D+A+1 D+Q+1
0 2 0 3 0 4 0 7	PASS	Q B A D	Increment	Q+1 B+1 A+1 D+1
1 2 1 3 1 4 2 7	Decrement	Q−1 B−1 A−1 D−1	PASS	Q B A D
2 2 2 3 2 4 1 7	1's Comp.	−Q−1 −B−1 −A−1 −D−1	2's Comp. (Negate)	−Q −B −A −D
1 0 1 1 1 5 1 6 2 0 2 1 2 5 2 6	Subtract (1's Comp.)	Q−A−1 B−A−1 A−D−1 Q−D−1 A−Q−1 A−B−1 D−A−1 D−Q−1	Subtract (2's Comp.)	Q−A B−A A−D Q−D A−Q A−B D−A D−Q

Figure 7. ALU Arithmetic Mode Functions

Logic Functions for $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the CY7C901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to *Figure 2.*

Definitions (+ = OR)

$P_0 = R_0 + S_0$	$G_0 = R_0S_0$
$P_1 = R_1 + S_1$	$G_1 = R_1S_1$
$P_2 = R_2 + S_2$	$G_2 = R_2S_2$
$P_3 = R_3 + S_3$	$G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_N+4	OVR
0	R+S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0}$	C_4	$C_3 \veebar C_4$
1	S−R	← Same as R+S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R−S	← Same as R+S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0}+C_n$	$\overline{P_3P_2P_1P_0}+C_n$
4	R ∧ S	LOW	$\overline{G_3+G_2+G_1+G_0}$	$G_3+G_2+G_1+G_0+C_n$	$G_3+G_2+G_1+G_0+C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ⊻ S	← Same as $\overline{R \veebar S}$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \veebar S}$	$G_3+G_2+G_1+G_0$	$G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1P_0$	$\overline{G_3+P_3G_2+P_3P_2G_1 + P_3P_2P_1P_0(G_0+\overline{C}_n)}$	See note

Notes:

$[P_2 + G_2P_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \veebar [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$

+ = OR

Figure 8

6

Electrical Characteristics Over Commercial and Military Operating Range[3]

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = −3.4 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 20 mA Commercial I_{OL} = 16 mA Military			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$ V_{CC} = Max.		−10	10	µA
I_{OH}	Output HIGH Current	V_{CC} = Min. V_{OH} = 2.4V		−3.4		mA
I_{OL}	Output LOW Current	V_{CC} = Min. V_{OL} = 0.4V	Commercial	20		mA
			Military	16		
I_{OZ}	Output Leakage Current	V_{CC} = Max. V_{OUT} = V_{SS} to V_{CC}		−40	+40	µA µA
I_{SC}	Output Short Circuit Current[1]	V_{CC} = Max. V_{OUT} = 0V			−85	mA
I_{CC}	Supply Current	V_{CC} = Max.	Commercial -31		70	mA
			Commercial -23		80	
			Military -27, -32		90	
I_{CC_1}	Supply Current	$V_{IH} \geq V_{CC}$ − 1.2V, 10 MHz $V_{IL} \leq$ 0.4V	Commercial		26.5	mA
			Military		31	

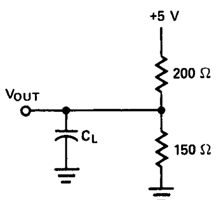
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f= 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

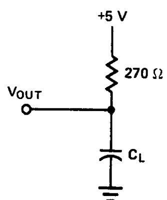
1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Tested initially and after any design or process changes that may affect these parameters.
3. See the last page of this specification for Group A subgroup testing information.

Output Loads used for AC Performance Characteristics



0030-4

All outputs except open drain



0030-5

Open drain (F = 0)

Notes:

1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.
3. Loads shown above are for commercial (20 mA) I_{OL} spec only.

CY7C901-23 Commercial and CY7C901-27 Military AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) and Military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" for loading circuit information.

This data applies to parts with the following numbers:

CY7C901-23PC	CY7C901-23DC	CY7C901-23LC
CY7C901-23JC	CY7C901-27DMB	CY7C901-27LMB

Cycle Time and Clock Characteristics[5]

CY7C901	-23	-27
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	23 ns	27 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	43 MHz	37 MHz
Minimum Clock LOW Time	13 ns	15 ns
Minimum Clock HIGH Time	10 ns	12 ns
Minimum Clock Period	23 ns	27 ns

Combinational Propagation Delays. $C_L = 50$ pF[5]

To Output / From Input	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3	
CY7C901	23	27	23	27	23	27	23	27	23	27	23	27	23	27	23	27
A, B Address	30	33	30	33	30	33	28	33	30	33	30	33	30	33	—	—
Data	21	24	20	23	20	23	20	21	24	25	21	24	22	25	—	—
C_n	17	18	16	17	14	14	—	—	18	19	16	17	18	19	—	—
I_{012}	26	28	25	27	24	26	24	28	25	29	24	27	25	27	—	—
I_{345}	26	27	24	27	24	26	24	26	26	27	24	26	26	27	—	—
I_{678}	16	18	—	—	—	—	—	—	—	—	—	—	21	21	21	21
A Bypass ALU (I = 2XX)	24	26	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock ⌠	24	27	23	26	23	26	23	25	24	27	24	26	24	27	19	20

Set-up and Hold Times Relative to Clock (CP) Input[5]

CP:

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H	
CY7C901	23	27	23	27	23	27	23	27
A, B Source Address	10	12	0 (Note 3)		21, 10 + t_{PWL} (Note 4)		0	
B Destination Address	10	12	← Do Not Change →				0	
Data	—	—	—		16		0	
C_n	—	—	—		13		0	
I_{012}	—	—	—		19		0	
I_{345}	—	—	—		19		0	
I_{678}	7	9	← Do Not Change →				0	
$RAM_{0,3}, Q_{0,3}$	—	—	—		9		0	

Output Enable/Disable Times[5]

Output disable tests performed with $C_L = 5$ pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C901-23	$\overline{OE}$	Y	14	16
CY7C901-27	$\overline{OE}$	Y	16	18

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.
5. See the last page of this specification for Group A subgroup testing information.

CY7C901-31 Commercial and CY7C901-32 Military AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) and Military (−55°C to + 125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See "Electrical Characteristics" for loading circuit information.

Cycle Time and Clock Characteristics[5]

CY7C901-	-31	-32
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	31 ns	32 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	32 MHz	31 MHz
Minimum Clock LOW Time	16 ns	17 ns
Minimum Clock HIGH Time	15 ns	15 ns
Minimum Clock Period	31 ns	32 ns

For faster performance see CY7C901-23 specification on page 9.

This data applies to parts with the following numbers:

CY7C901-31PC CY7C901-31DC CY7C901-31LC CY7C901-31JC CY7C901-32DMB CY7C901-32LMB

Combinational Propagation Delays. C_L = 50 pF[5]

To Output	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3	
From Input	-31	-32	-31	-32	-31	-32	-31	-32	-31	-32	-31	-32	-31	-32	-31	-32
A, B Address	40	48	40	48	40	48	37	44	40	48	40	48	40	48	—	—
D	30	37	30	37	30	37	30	34	38	40	30	37	30	37	—	—
C_n	22	25	22	25	20	21	—	—	25	28	22	25	25	28	—	—
I_{012}	35	40	35	40	35	40	37	44	37	44	35	40	35	40	—	—
I_{345}	35	40	35	40	35	40	35	40	38	40	35	40	35	40	—	—
I_{678}	25	29	—	—	—	—	—	—	—	—	—	—	26	29	26	29
A Bypass ALU (I = 2XX)	35	40	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock ↑	35	40	35	40	35	40	35	40	35	40	35	40	35	40	28	33

Set-up and Hold Times Relative to Clock (CP) Input[5]

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	15	0 (Note 3)	30, 15 + t_{PWL} (Note 4)	0
B Destination Address	15	← Do Not Change	→	0
D	—	—	25	0
C_n	—	—	20	0
I_{012}	—	—	30	0
I_{345}	—	—	30	0
I_{678}	10	← Do Not Change	→	0
$RAM_{0,3}, Q_{0,3}$	—	—	12	0

Output Enable/Disable Times[5]

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

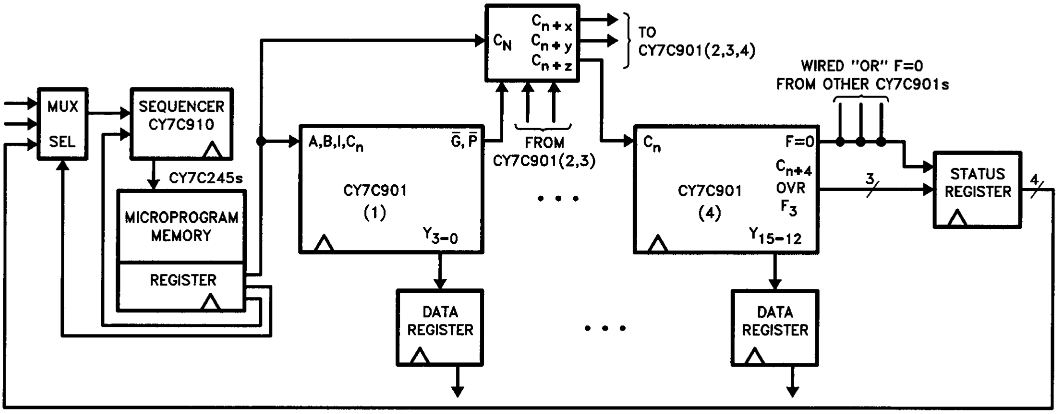
Device	Input	Output	Enable	Disable
CY7C901-31	$\overline{OE}$	Y	23	23
CY7C901-32	$\overline{OE}$	Y	25	25

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.
5. See the last page of this specification for Group A subgroup testing information.

Minimum Cycle Time Calculations for 16-Bit Systems

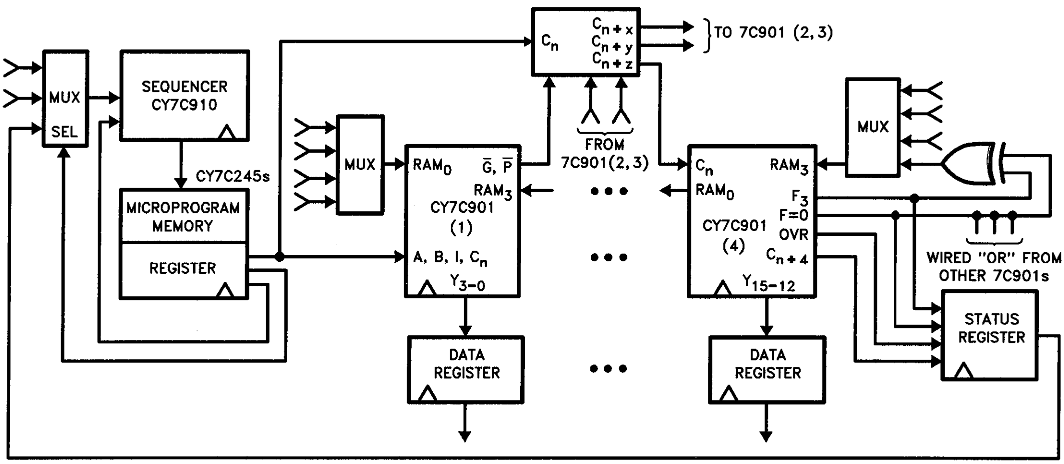
Speed used in calculations for parts other than CY7C901 are representative for MSI parts.



Pipelined System, Add without Simultaneous Shift

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to $\overline{G}$, $\overline{P}$	28	MUX	Select to Output	12
Carry Logic	$\overline{G}_0$, $\overline{P}_0$ to $C_n + z$	9	CY7C910	CC to Output	22
CY7C901	C_n to Worst Case	18	CY7C245	Access Time	20
Register	Setup	4			
		71 ns			66 ns

Minimum Clock Period = 71 ns



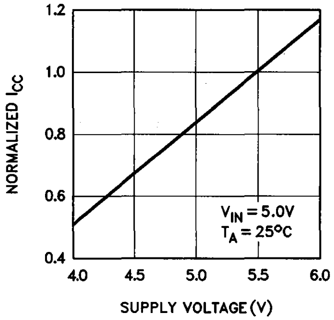
Pipelined System, Simultaneous Add and Shift Down (RIGHT)

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to $\overline{G}$, $\overline{P}$	28	MUX	Select to Output	12
Carry Logic	$\overline{G}_0$, $\overline{P}_0$ to $C_n + z$	9	CY7C910	CC to Output	22
CY7C901	C_n to Worst Case	18	CY7C245	Access Time	20
XOR and MUX	Prop. Delay, Select to Output	20			66 ns
CY7C901	RAM_3 Setup	9			
		96 ns			

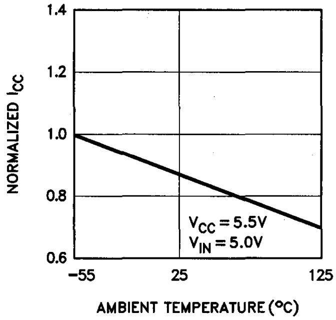
Minimum Clock Period = 96 ns

Typical DC and AC Characteristics

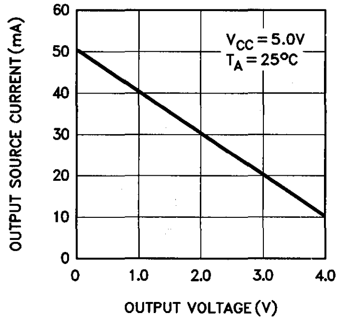
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



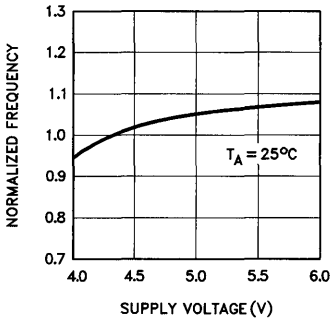
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



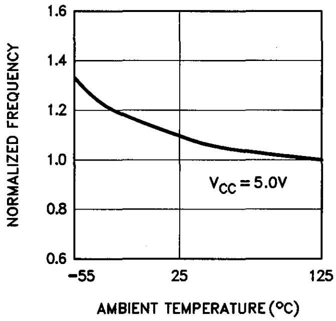
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



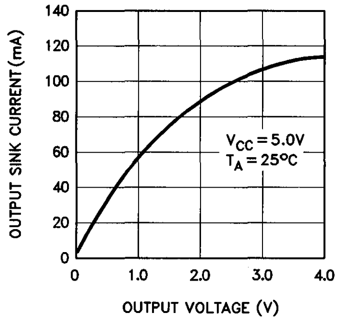
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



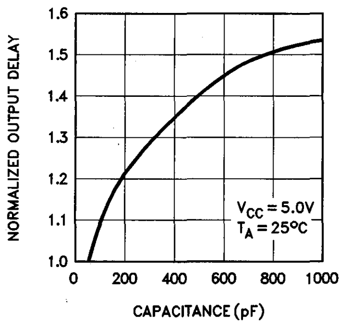
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



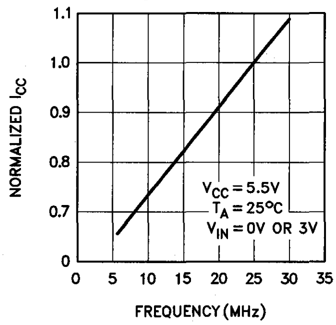
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



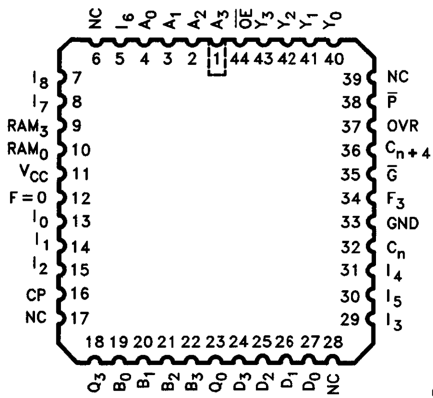
0030–10

Ordering Information

Read Modify-Write Cycle (ns)	Ordering Code	Package Type	Operating Range
23	CY7C901-23PC	P17	Commercial
	CY7C901-23DC	D18	Commercial
	CY7C901-23JC	J67	Commercial
	CY7C901-23LC	L67	Commercial
27	CY7C901-27DMB	D18	Military
	CY7C901-27LMB	L67	Military
31	CY7C901-31PC	P17	Commercial
	CY7C901-31DC	D18	Commercial
	CY7C901-31JC	J67	Commercial
	CY7C901-31LC	L67	Commercial
32	CY7C901-32DMB	D18	Military
	CY7C901-32LMB	L67	Military

Pin Configuration

Top View



0030-9

6

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{SC}	1,2,3
I_{CC}	1,2,3
I_{CC1}	1,2,3

Cycle Time and Clock Characteristics

Parameters	Subgroups
Minimum Clock LOW Time	7,8,9,10,11
Minimum Clock HIGH Time	7,8,9,10,11

Combinational Propagation Delays

Parameters	Subgroups
From A, B Address to Y	7,8,9,10,11
From A, B Address to F_3	7,8,9,10,11
From A, B Address to C_{n+4}	7,8,9,10,11
From A, B Address to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From A, B Address to F=0	7,8,9,10,11
From A, B Address to OVR	7,8,9,10,11
From A, B Address to $RAM_{0,3}$	7,8,9,10,11
From D to Y	7,8,9,10,11
From D to F_3	7,8,9,10,11
From D to C_{n+4}	7,8,9,10,11
From D to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From D to F = 0	7,8,9,10,11
From D to OVR	7,8,9,10,11
From D to $RAM_{0,3}$	7,8,9,10,11
From C_n to Y	7,8,9,10,11
From C_n to F_3	7,8,9,10,11

Combinational Propagation Delays (Continued)

Parameters	Subgroups
From C_n to C_{n+4}	7,8,9,10,11
From C_n to F = 0	7,8,9,10,11
From C_n to OVR	7,8,9,10,11
From C_n to $RAM_{0,3}$	7,8,9,10,11
From I_{012} to Y	7,8,9,10,11
From I_{012} to F_3	7,8,9,10,11
From I_{012} to C_{n+4}	7,8,9,10,11
From I_{012} to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From I_{012} to F=0	7,8,9,10,11
From I_{012} to OVR	7,8,9,10,11
From I_{012} to $RAM_{0,3}$	7,8,9,10,11
From I_{345} to Y	7,8,9,10,11
From I_{345} to F_3	7,8,9,10,11
From I_{345} to C_{n+4}	7,8,9,10,11
From I_{345} to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From I_{345} to F=0	7,8,9,10,11
From I_{345} to OVR	7,8,9,10,11
From I_{345} to $RAM_{0,3}$	7,8,9,10,11
From I_{678} to Y	7,8,9,10,11
From I_{678} to $RAM_{0,3}$	7,8,9,10,11
From I_{678} to $Q_{0,3}$	7,8,9,10,11
From A Bypass ALU to Y (I = 2XX)	7,8,9,10,11
From Clock $\uparrow$ to Y	7,8,9,10,11
From Clock $\uparrow$ to F_3	7,8,9,10,11
From Clock $\uparrow$ to C_{n+4}	7,8,9,10,11
From Clock $\uparrow$ to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From Clock $\uparrow$ to F=0	7,8,9,10,11
From Clock $\uparrow$ to OVR	7,8,9,10,11
From Clock $\uparrow$ to $RAM_{0,3}$	7,8,9,10,11
From Clock $\uparrow$ to $Q_{0,3}$	7,8,9,10,11

Set-up and Hold Times Relative to Clock (CP) Input

Parameters	Subgroups
A, B Source Address Set-up Time Before H → L	7,8,9,10,11
A, B Source Address Hold Time After H → L	7,8,9,10,11
A, B Source Address Set-up Time Before L → H	7,8,9,10,11
A, B Source Address Hold Time After L → H	7,8,9,10,11
B Destination Address Set-up Time Before H → L	7,8,9,10,11
B Destination Address Hold Time After H → L	7,8,9,10,11
B Destination Address Set-up Time Before L → H	7,8,9,10,11
B Destination Address Hold Time After L → H	7,8,9,10,11
D Set-up Time Before L → H	7,8,9,10,11

Parameters	Subgroups
D Hold Time After L → H	7,8,9,10,11
C_n Set-up Time Before L → H	7,8,9,10,11
C_n Hold Time After L → H	7,8,9,10,11
I_{012} Set-up Time Before L → H	7,8,9,10,11
I_{012} Hold Time After L → H	7,8,9,10,11
I_{345} Set-up Time Before L → H	7,8,9,10,11
I_{345} Hold Time After L → H	7,8,9,10,11
I_{678} Set-up Time Before H → L	7,8,9,10,11
I_{678} Hold Time After H → L	7,8,9,10,11
I_{678} Set-up Time Before L → H	7,8,9,10,11
I_{678} Hold Time After L → H	7,8,9,10,11
RAM_0, RAM_3, Q_0, Q_3 Set-up Time Before L → H	7,8,9,10,11
RAM_0, RAM_3, Q_0, Q_3 Hold Time After L → H	7,8,9,10,11

Document #: 38-00021-B

6

CY7C909
CY7C911

CYPRESS SEMICONDUCTOR

CMOS Micro Program Sequencers

Features

- Fast
  - CY7C909/11 has a 30 ns (min.) clock to output cycle time; commercial and military
- Low Power
  - I_{CC} (max.) = 55 mA; commercial and military
- V_{CC} margin
  - 5 V ± 10%
  - All parameters guaranteed over commercial and military operating temperature range
- Expandable
  Infinitely expandable in 4-bit increments
- Capable of withstanding greater than 2000V static discharge voltage
- Pin compatible and functional equivalent to 2909A/2911A

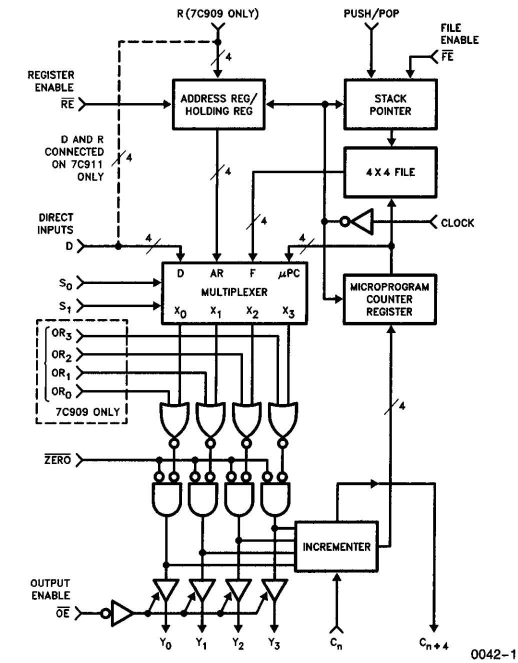
Description

The CY7C909 and CY7C911 are high-speed, four-bit wide address sequencers intended for controlling the sequence of execution of microinstructions contained in microprogram memory. They may be connected in parallel to expand the address width in 4 bit increments. Both devices are implemented in high performance CMOS for optimum speed and power.

The CY7C909 can select an address from any of four sources. They are: 1) a set of four external direct inputs (D_i); 2) external data stored in an internal register (R_i); 3) a four word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs (Y_i) can be OR'ed with an external input for conditional skip or branch instructions. A $\overline{\text{ZERO}}$ input line forces the outputs to all zeros. The outputs are three state, controlled by the Output Enable ($\overline{\text{OE}}$) input.

The CY7C911 is an identical circuit to the CY7C909, except the four OR inputs are removed and the D and R inputs are tied together. The CY7C911 is available in a 20-pin, 300-mil package.

Logic Block Diagram



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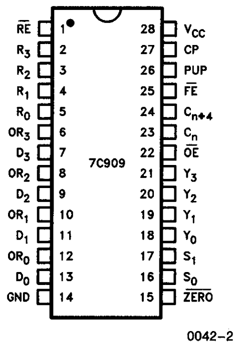
Pin Configurations



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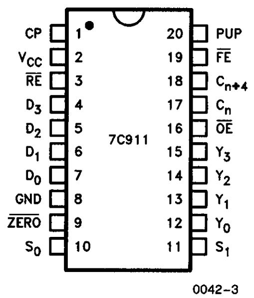
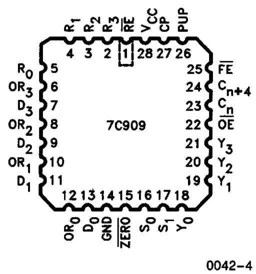
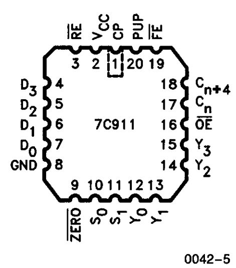


0042-3



0042-4



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . −65°C to +150°C

Ambient Temperature with
Power Applied . . . . −55°C to +125°C

Supply Voltage to Ground Potential . . . . −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State. . . . . −0.5V to +7.0V

DC Input Voltage . . . . −3.0V to +7.0V

Output Current, into Outputs (Low) . . . . 30 mA

Static Discharge Voltage . . . . >2001V
(per MIL-STD-883 Method 3015)

Latch-Up Current . . . . >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Operating Range[4]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −2.6 mA (Comm.)		2.4		V
		V_{CC} = Min., I_{OH} = −1.0 mA (Mil.)		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16.0 mA			0.4	V
V_{IH}	Input High Voltage			2.0	V_{CC}	V
V_{IL}	Input Low Voltage			−2.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−20	+20	μA
I_{OS}	Output Short[1] Circuit Current	V_{CC} = Max.	V_{OUT} = GND	−30	−85	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max. I_{OUT} = 0 mA	Commercial		55	mA
			Military		55	
I_{CC1}	V_{CC} Operating Supply Current	V_{CC} = Max. V_{IH} ≥ 3.0V, V_{IL} ≤ 0.4V	Commercial		35	mA
			Military		35	

Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested initially and after any design or process changes that may affect these parameters.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.

AC Test Loads and Waveforms

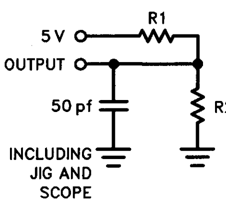


Figure 1a

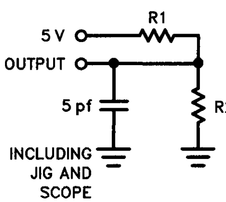


Figure 1b

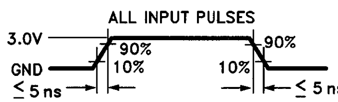


Figure 2

	Commercial	Military
R_1	254Ω	258Ω
R_2	187Ω	216Ω

6

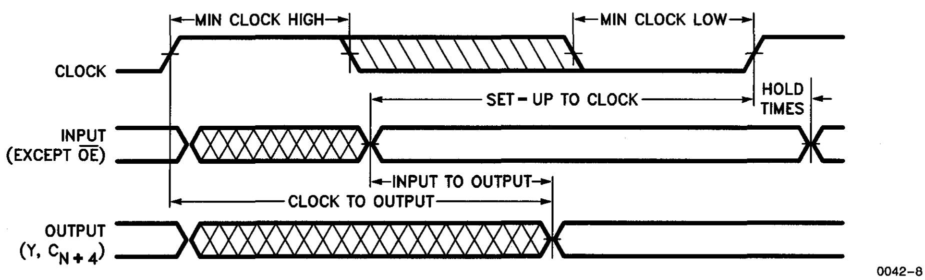
Switching Characteristics Over Operating Range[4, 5]

	7C909-30 7C911-30		7C909-30 7C911-30		7C909-40 7C911-40		7C909-40 7C911-40		Units
	Commercial		Military		Commercial		Military		
Minimum Clock Low Time	15		15		20		20		ns
Minimum Clock High Time	15		15		20		20		ns
MAXIMUM COMBINATIONAL PROPAGATION DELAYS									
From Input To:	Y	C_{N+4}	Y	C_{N+4}	Y	C_{N+4}	Y	C_{N+4}	ns
D_i	17	18	18	19	17	22	20	25	ns
S_0, S_1	18	18	20	20	29	34	29	34	ns
OR_i (7C909)	16	16	17	17	17	22	20	25	ns
C_N	—	13	—	15	—	14	—	16	ns
$\overline{ZERO}$	18	18	20	20	29	34	30	35	ns
$\overline{OE}$ Low to Output	16	—	18	—	25	—	25	—	ns
$\overline{OE}$ HIGH to HIGH Z[5]	16	—	18	—	25	—	25	—	ns
Clock HIGH, S_1, S_0 = LH	20	20	22	22	39	44	45	50	ns
Clock HIGH, S_1, S_0 = LL	20	20	22	22	39	44	45	50	ns
Clock HIGH, S_1, S_0 = HL	20	20	22	22	44	49	53	58	ns
MINIMUM SET-UP AND HOLD TIMES (All Times Relative to Clock LOW to HIGH Transition)									
From Input	**Set-up**	**Hold**	**Set-up**	**Hold**	**Set-up**	**Hold**	**Set-up**	**Hold**	
$\overline{RE}$	11	0	12	0	19	0	19	0	ns
R_i [6]	10	0	11	0	10	0	12	0	ns
Push/Pop	12	0	13	0	25	0	27	0	ns
FE	12	0	13	0	25	0	27	0	ns
C_N	10	0	11	0	18	0	18	0	ns
D_i	14	0	16	0	25	0	25	0	ns
OR_i (7C909)	12	0	14	0	25	0	25	0	ns
S_0, S_1	14	0	16	0	25	0	29	0	ns
$\overline{ZERO}$	12	0	13	0	25	0	29	0	ns

Notes:

5. Output Loading as in *Figure 1b.*
6. R_i and D_i are internally connected on the CY7C911. Use R_i set-up and hold times when D_i inputs are used to load register.
7. System clock cycle time (Clock Low Time and Clock High Time) cannot be less than maximum propagation delay.

Switching Waveforms



0042–8

Functional Description

The tables below define the control logic of the 7C909/911. Table 1 contains the Multiplexer Control Logic which selects the address source to appear on the outputs.

Table 1. Address Source Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS
0	L	L	Microprogram Counter (μPC)
1	L	H	Address/Holding Register (AR)
2	H	L	Push-Pop stack (STK)
3	H	H	Direct inputs (D_i)

Control of the Push/Pop Stack is contained in Table 2. $\overline{\text{FILE ENABLE}}$ ($\overline{\text{FE}}$) enables stack operations, while Push/Pop (PUP) controls the stack.

Table 2. Synchronous Stack Control

$\overline{\text{FE}}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Push current PC into stack increment stack pointer
L	L	pop stack, decrement stack pointer

Table 3 illustrates the Output Control Logic of the 7C909/911. The $\overline{\text{ZERO}}$ control forces the outputs to zero. The OR inputs are OR'ed with the output of the multiplexer.

Table 3. Output Control

OR_i	$\overline{\text{ZERO}}$	$\overline{\text{OE}}$	Y_i
X	X	H	High Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Table 4 defines the effect of S_0, S_1, $\overline{\text{FE}}$ and PUP control signals on the 7C909. It illustrates the Address Source on the outputs and the contents of the Internal Registers for every combination of these signals. The Internal Register contents are illustrated before and after the Clock LOW to HIGH edge.

Table 4

CYCLE	S_1, S_0, $\overline{\text{FE}}$, PUP	μ PC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N + 1	0 0 0 0 —	J J + 1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J —	Pop Stack	End Loop
N N + 1	0 0 0 1 —	J J + 1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J —	Push μPC	Set-up Loop
N N + 1	0 0 1 X —	J J + 1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J —	Continue	Continue
N N + 1	0 1 0 0 —	J K + 1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K —	Use AR for Address; Pop Stack	End Loop
N N + 1	0 1 0 1 —	J K + 1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K —	Jump to Address in AR; Push μPC	JSR AR
N N + 1	0 1 1 X —	J K + 1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K —	Jump to Address in AR	JMP AR
N N + 1	1 0 0 0 —	J Ra + 1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra —	Jump to Address in STK0; Pop Stack	RTS
N N + 1	1 0 0 1 —	J Ra + 1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra —	Jump to Address in STK0; Push μPC	
N N + 1	1 0 1 X —	J Ra + 1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra —	Jump to Address in STK0	Stack Ref (Loop)
N N + 1	1 1 0 0 —	J D + 1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D —	Jump to Address on D; Pop Stack	End Loop
N N + 1	1 1 0 1 —	J D + 1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D —	Jump to Address on D; Push μPC	JSR D
N N + 1	1 1 1 X —	J D + 1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D —	Jump to Address on D	JMP D

J = Contents of Microprogram Counter
K = Contents of Address Register
R_a, R_b, R_c, R_d = Contents in Stack

6

Functional Description (Continued)

Two examples of Subroutine Execution appear below. *Figure 3* illustrates a single subroutine while *Figure 4* illustrates two nested subroutines.

The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the 7C909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to sub-routine at A". At the time T_2, this instruction is in the μWR, and the 7C909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J + 3 is pushed onto the stack. The return instruction is executed at T_5. *Figure 4* is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J-1	-
T_0	J	-
T_1	J+1	-
T_2	J+2	JSR A
T_6	J+3	-
T_7	J+4	-
	-	-
	-	-
	-	-
	-	-
	-	-
T_3	A	I(A)
T_4	A+1	-
T_5	A+2	RTS
	-	-
	-	-
	-	-
	-	-
	-	-
	-	-

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	-	-	-	J+3	J+3	J+3	-	-		
	STK1	-	-	-	-	-	-	-	-		
	STK2	-	-	-	-	-	-	-	-		
	STK3	-	-	-	-	-	-	-	-		
Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)		

0042–9

Figure 3. Subroutine Execution.

C_n = HIGH

CONTROL MEMORY

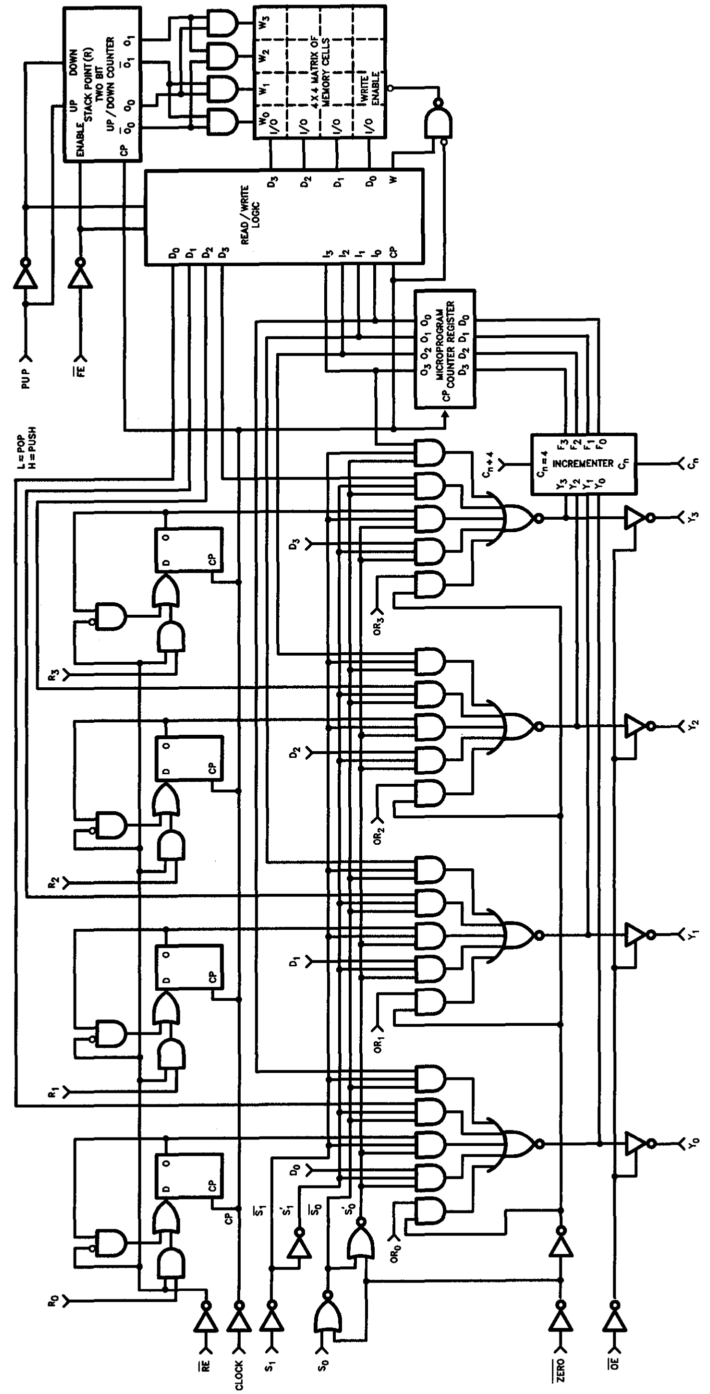
Execute Cycle	Microprogram Address	Microprogram Sequencer Instruction
	J-1	-
T_0	J	-
T_1	J+1	-
T_2	J+2	JSR A
T_9	J+3	-
	-	-
	-	-
	-	-
T_3	A	-
T_4	A+1	-
T_5	A+2	JSR B
T_7	A+3	-
T_8	A+4	RTS
	-	-
	-	-
	-	-
	-	-
T_6	B	RTS
	-	-
	-	-

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock Signals											
Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	-	-	-	J+3	J+3	J+3	A+3	J+3	J+3	-
	STK1	-	-	-	-	-	-	J+3	-	-	-
	STK2	-	-	-	-	-	-	-	-	-	-
	STK3	-	-	-	-	-	-	-	-	-	-
Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)

0042–10

Figure 4. Two Nested Subroutines. Routine B is Only One Instruction.

C_n = HIGH



0042-11

Note:
R_i and D_i connected together and OR_i Inputs removed on CY7C911

Figure 5. Microprogram Sequencer Block Diagram

Functional Description (Continued)

Architecture

The CY7C909 and CY7C911 are CMOS microprogram sequencers for use in high speed processor applications. They are cascadable in 4-bit increments. Two devices can address 256 words of microprogram, three can address up to 4K words, and so on. The architecture of the CY7C909/911 is illustrated in the logic diagram in *Figure 5*. The various blocks are described below.

Multiplexer

The Multiplexer is controlled by the S_0 and S_1 inputs to select the address source. It selects either the Direct Inputs (D_i), the Address Register (AR), the Microprogram Counter (μPC), or the stack (SP) as the source of the next microinstruction address.

Direct Inputs

The Direct Inputs (D_i) allow addresses from an external source to be output on the Y outputs. On the CY7C911, the direct inputs are also the inputs to the Address Register.

Address Register

The Address Register (AR) consists of four D-type, edge-triggered flip-flops which are controlled by the $\overline{\text{Register Enable}}$ ($\overline{\text{RE}}$) input. When $\overline{\text{Register Enable}}$ is LOW, new data is entered into the register on the LOW to HIGH clock transition.

Microprogram Counter

The Microprogram Counter (μPC) is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has a Carry-in (C_N) input and a Carry-out (C_{N+4}) output to facilitate cascading. The Carry-in input controls the microprogram counter. When Carry-in is HIGH the incrementer counts sequentially. The counter register is loaded with the current Y output plus one ($Y + 1 -> \mu PC$) on the next clock cycle. When Carry-in is LOW the incrementer does not count. The microprogram counter register is loaded with the same Y output ($Y -> \mu PC$) on the next clock cycle.

Stack

The Stack consists of a 4 x 4 memory array and a built-in Stack Pointer (SP) which always points to the last word written. The Stack is used to store return addresses when executing microsubroutines.

The Stack Pointer is an up/down counter controlled by $\overline{\text{File Enable}}$ ($\overline{\text{FE}}$) and Push/Pop (PUP) inputs. The $\overline{\text{File Enable}}$ input allows stack operations only when it is LOW. The Push/Pop input controls the stack pointer position.

The PUSH operation is initiated at the beginning of a microsubroutine. Push/Pop is set HIGH while $\overline{\text{File Enable}}$ is kept LOW. The stack pointer is incremented and the memory array is written with the microinstruction address following the subroutine jump that initiated the push.

The POP operation is initiated at the end of a microsubroutine to obtain the return address. Both Push/Pop and $\overline{\text{File Enable}}$ are set LOW. The return address is already available to the multiplexer. The stack pointer is decremented on the next LOW to HIGH clock transition, effectively removing old information from the top of the stack. The stack is configured so that data will roll-over if more than four POPs are performed, thus preventing data from being lost.

The contents of the memory position pointed to by the Stack Pointer is always available to the multiplexer. Stack reference operations can thus be performed without a push or a pop. Since the stack is four words deep, up to four microsubroutines can be nested.

The $\overline{\text{ZERO}}$ input resets the four Y outputs to a binary zero state. The OR inputs (7C909 only) are connected to the Y outputs such that any output can be set to a logical one.

The $\overline{\text{Output Enable}}$ ($\overline{\text{OE}}$) input controls the Y outputs. A HIGH on $\overline{\text{Output Enable}}$ sets the outputs into a high impedance state.

Definition of Terms

Name	Description
INPUTS	
S_1, S_0	Multiplexer Control Lines, for Access Source Selection
$\overline{\text{FE}}$	$\overline{\text{File Enable}}$, Enables Stack Operation, Active LOW
PUP	Push/Pop, Selects Stack Operation
$\overline{\text{RE}}$	$\overline{\text{Register Enable}}$, Enables Address Register Active LOW
$\overline{\text{ZERO}}$	Forces Output to Logical Zero
$\overline{\text{OE}}$	$\overline{\text{Output Enable}}$, Controls Three-State Outputs Active LOW
OR_i	Logic OR Input to each Address Output Line (7C909 only)
C_n	Carry-In, Controls Microprogram Counter
R_i	Inputs to the Internal Address Register
D_i	Direct Inputs to the Multiplexer
CP	Clock Input

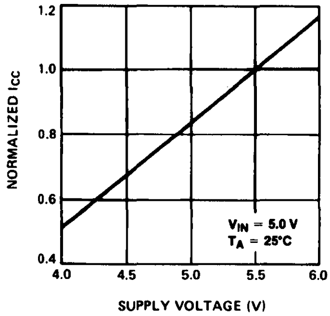
Definition of Terms (Continued)

Name	Description
OUTPUTS	
Y_i	Address Outputs
C_{N+4}	Carry-Out from Incrementer
INTERNAL SIGNALS	
μPC	Contents of the Microprogram Counter
AR	Contents of the Address Register
STK0- STK3	Contents of the Push/Pop Stack
SP	Contents of the Stack Pointer
EXTERNAL SIGNALS	
A	Address to the Counter Memory
I(A)	Instruction in Control Memory at Address A
μWR	Contents of the Microword Register at the Output of the Control Memory
T_N	Time Period (Cycle) n

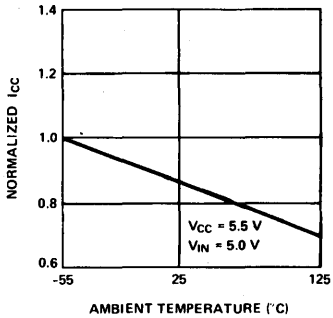
6

Typical DC and AC Characteristics

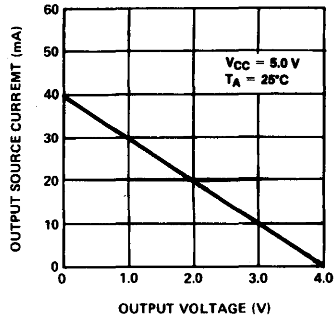
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



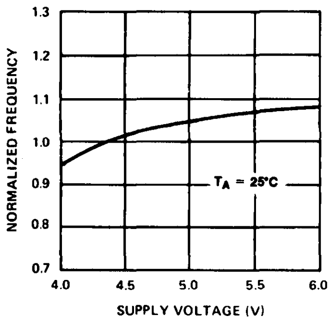
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



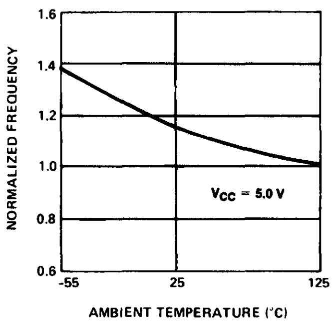
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



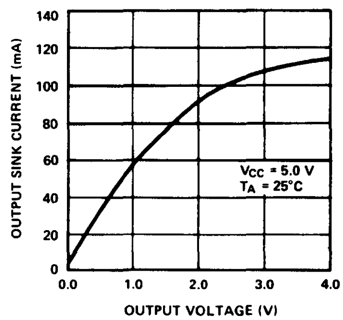
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



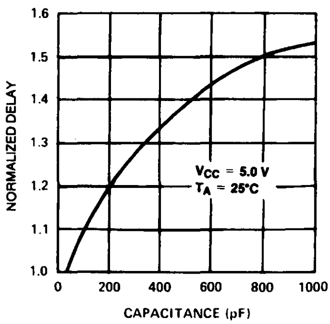
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



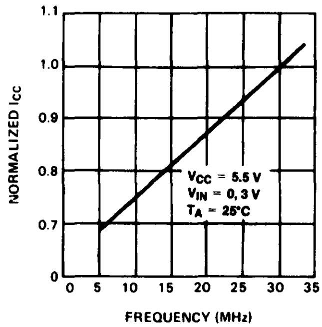
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0042–12

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
30	CY7C909-30PC	P15	Commercial
40	CY7C909-40PC	P15	Commercial
30	CY7C909-30JC	J64	Commercial
40	CY7C909-40JC	J64	Commercial
30	CY7C909-30DC	D16	Commercial
40	CY7C909-40DC	D16	Commercial
40	CY7C909-40LC	L64	Commercial
30	CY7C909-30DMB	D16	Military
40	CY7C909-40DMB	D16	Military
40	CY7C909-40LMB	L64	Military

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
30	CY7C911-30PC	P5	Commercial
40	CY7C911-40PC	P5	Commercial
30	CY7C911-30JC	J61	Commercial
40	CY7C911-40JC	J61	Commercial
30	CY7C911-30DC	D6	Commercial
40	CY7C911-40DC	D6	Commercial
40	CY7C911-40LC	L61	Commercial
30	CY7C911-30DMB	D6	Military
40	CY7C911-40DMB	D6	Military
40	CY7C911-40LMB	L61	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{OS}	1,2,3
I_{CC}	1,2,3
I_{CC1}	1,2,3

Switching Characteristics

Parameters	Subgroups
Minimum Clock Low Time	7,8,9,10,11
Minimum Clock High Time	7,8,9,10,11
MAXIMUM COMBINATIONAL PROPAGATION DELAYS	
D_i to Y	7,8,9,10,11
D_i to C_{N+4}	7,8,9,10,11
S_0, S_1 to Y	7,8,9,10,11
S_0, S_1 to C_{N+4}	7,8,9,10,11
OR_i (7C909) to Y	7,8,9,10,11
OR_i (7C909) to C_{N+4}	7,8,9,10,11
C_N to C_{N+4}	7,8,9,10,11
$\overline{ZERO}$ to C_{N+4}	7,8,9,10,11
Clock High, S_0, S_1 = LH to Y	7,8,9,10,11
Clock High, S_0, S_1 = LH to C_{N+4}	7,8,9,10,11
Clock High, S_0, S_1 = LL to Y	7,8,9,10,11
Clock High, S_0, S_1 = LL to C_{N+4}	7,8,9,10,11
Clock High, S_0, S_1 = HL to Y	7,8,9,10,11
Clock High, S_0, S_1 = HL to C_{N+4}	7,8,9,10,11

Parameters	Subgroups
MINIMUM SET-UP AND HOLD TIMES	
$\overline{RE}$ Set-up Time	7,8,9,10,11
$\overline{RE}$ Hold Time	7,8,9,10,11
Push/Pop Set-up Time	7,8,9,10,11
Push/Pop Hold Time	7,8,9,10,11
FE Set-up Time	7,8,9,10,11
FE Hold Time	7,8,9,10,11
C_N Set-up Time	7,8,9,10,11
C_N Hold Time	7,8,9,10,11
D_i Set-up Time	7,8,9,10,11
D_i Hold Time	7,8,9,10,11
OR_i (7C909) Set-up Time	7,8,9,10,11
OR_i (7C909) Hold Time	7,8,9,10,11
S_0, S_1 Set-up Time	7,8,9,10,11
S_0, S_1 Hold Time	7,8,9,10,11
$\overline{ZERO}$ Set-up Time	7,8,9,10,11
$\overline{ZERO}$ Hold Time	7,8,9,10,11

Document #: 38-00015-B

CYPRESS SEMICONDUCTOR

CY7C910

CMOS Microprogram Controller

Features

- Fast
  - CY7C910-40 has a 40 ns (min.) clock cycle; commercial
  - CY7C910-46 has a 46 ns (min.) clock cycle; military
- Low power
  - I_{CC} (max.) = 70 mA
- V_{CC} margin 5V ±10% commercial and military
- Sixteen powerful microinstructions
- Three output enable controls for three-way branch
- Twelve-bit address word
- Four sources for addresses: microprogram counter (MPC), stack, branch address bus, internal holding register
- 12-bit internal loop counter
- Internal 17-word by 12-bit stack The internal stack can be used for subroutine return address or data storage
- ESD protection Capable of withstanding over 2000V static discharge voltage
- Pin compatible and functional equivalent to AM2910A

Functional Description

The CY7C910 is a stand-alone microprogram controller that selects, stores, retrieves, manipulates and tests addresses that control the sequence of execution of instructions stored in an external memory. All addresses are 12-bit binary values that designate an absolute memory location.

The CY7C910, as illustrated in the block diagram, consists of a 17-word by 12-bit LIFO (Last-In-First-Out) stack and SP (Stack Pointer), a 12-bit RC (Register/Counter), a 12-bit MPC (Microprogram Counter) and incrementer, a 12-bit wide by 4-input multiplexer and the required data manipulation and control logic.

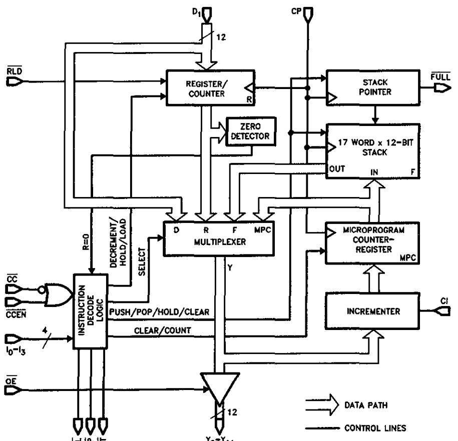
The operation performed is determined by four input instruction lines (I0–I3) that in turn select the (internal) source of the next micro-instruction to be fetched. This address is output on the Y0–Y11 pins. Two additional inputs ($\overline{CC}$ and $\overline{CCEN}$) are provided that are examined during certain instructions and enable the user to make the execution of the instruction either unconditional or dependent upon an external test.

The CY7C910 is a pin compatible, functional equivalent, improved performance replacement for the AM2910A.

The CY7C910 is fabricated using an advanced 1.2 micron CMOS process that eliminates latchup, results in ESD protection of over 2000 volts and achieves superior performance and low power dissipation.

6

Logic Block Diagram



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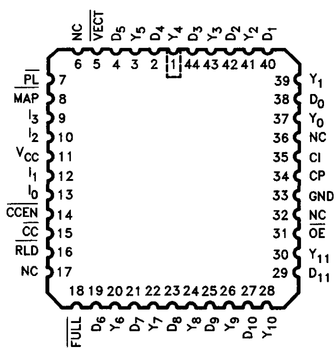
Pin Configurations



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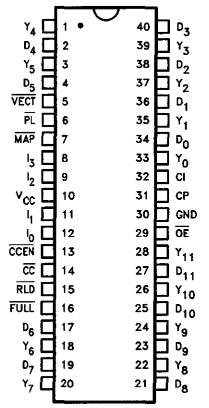

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Top View

Selection Guide

Clock Cycle (Min.) in ns	Stack Depth	Operating Range	Part Number
40	17 words	Commercial	CY7C910-40
46	17 words	Military	CY7C910-46
50	17 words	Commercial	CY7C910-50
51	17 words	Military	CY7C910-51
93	17 words	Commercial	CY7C910-93
99	17 words	Military	CY7C910-99

Pin Definitions

Signal Name	I/O	Description
D0–D11	I	Direct inputs to the RC (Register/Counter) and multiplexer. D0 is LSB and D11 is MSB.
$\overline{\text{RLD}}$	I	Register load. Control input to RC that, when LOW, loads data on the D0–D11 pins into RC on the LOW to HIGH clock (CP) transition.
I0–I3	I	Instruction inputs that select one of sixteen instructions to be performed by the CY7C910.
$\overline{\text{CC}}$	I	Control input that, when LOW, signifies that a test has passed.
$\overline{\text{CCEN}}$	I	Enable for $\overline{\text{CC}}$ input. When HIGH $\overline{\text{CC}}$ is ignored and a pass is forced. When LOW the state of $\overline{\text{CC}}$ is examined.
CP	I	Clock input. All internal states are changed on the LOW to HIGH clock transitions.

Signal Name	I/O	Description
CI	I	Carry input to the LSB of the incrementer for the MPC.
$\overline{\text{OE}}$	I	Control for Y0–Y11 outputs. LOW to enable; High to disable.
Y0–Y11	O	Address output to microprogram memory. Y0 is LSB and Y11 is MSB.
$\overline{\text{FULL}}$	O	When LOW indicates the stack is full.
$\overline{\text{PL}}$	O	When LOW selects the pipeline register as the direct input (D0–D11) source.
$\overline{\text{MAP}}$	O	When LOW selects the Mapping PROM (or PLA) as the direct input source.
$\overline{\text{VECT}}$	O	When LOW selects the Interrupt Vector as the direct input source.

Architecture of the CY7C910

Introduction

The CY7C910 is a high performance CMOS microprogram controller that produces a sequence of 12-bit addresses that control the execution of a microprogram. The addresses are selected from one of four sources, depending upon the (internal) instruction being executed (I0–I3), and other external inputs. The sources are (1) the (external) D0–D11 inputs, (2) the RC, (3) the stack and (4) the MPC. Twelve bit lines from each of these four sources are the inputs to a multiplexer, as shown in *Figure 1,* whose outputs are applied to the inputs of the Y0–Y11 three-state output drivers.

External Inputs: D0–D11

The external inputs are used as the source for destination addresses for the jump or branch type of instructions. These are shown as Ds in the two columns in the Table of Instructions. A second use of these inputs is to load the RC.

Register Counter: RC

The RC is implemented as 12 D-type, edge-triggered flip-flops that are synchronously clocked on the LOW to HIGH transition of the clock, CP. The data on the D inputs is synchronously loaded into the RC when the load control input, RLD, is LOW. The output of the RC is available to the multiplexer as its R input and is output on the Y outputs during certain instructions, as shown by R in the Table of Instructions.

The RC is operated as a 12-bit down counter and its contents decremented and tested if zero during instructions 8, 9 and 15. This enables micro-instructions to be repeated up to 4096 times. The RC is arranged such that if it is loaded with a number, N, the sequence will be executed exactly N + 1 times.

The Stack and Stack Pointer: SP

The 17-word by 12-bit stack is used to provide return addresses from micro-subroutines or from loops. Intergal to it is a SP, which points to (addresses) the last word written. This permits reference to the data on the top of the stack without having to perform a POP operation.

The SP operates as an up/down counter that is incremented when a PUSH operation (instructions 1, 4 or 5) is performed or decremented when a POP operation (instructions 8, 10, 11, 13 or 15) is performed. The PUSH operation writes the return address on the stack and the POP operation effectively removes it. The actual operation occurs on the LOW to HIGH clock transition following the instruction.

The stack is initialized by executing instruction zero (JUMP TO LOCATION 0 or RESET). Every time a "jump to subroutine" instruction (1, 5) or a loop instruction (4) is executed, the return address is PUSHed onto the stack; and every time a "return from subroutine (or loop)" instruction is executed, the return address is POPed off the stack.

When one subroutine calls another or a loop occurs within a loop (or a combination), which is called nesting, the Logical depth of the stack increases. The physical stack depth is 17 words. When this depth occurs, the $\overline{\text{FULL}}$ signal goes LOW on the next LOW to HIGH clock transition. Any further PUSH operations on a full stack will cause the data at that location to be over-written, but will not increment the SP. Similarily, performing a POP operation on a empty stack will not decrement the SP and may result in non-meaningful data being available at the Y outputs.

The Microprocessor Counter: MPC

The MPC consists of a 12-bit incrementer followed by a 12-bit register. The register usually holds the address of the instruction being fetched. When sequential instructions are fetched, the carry input (CI) to the incrementer is HIGH and one is added to the Y outputs of the multiplexer, which is loaded into the MPC on the next LOW to HIGH clock transition. When the CI input is LOW, the Y outputs of the multiplexer are loaded directly into the MPC, so that the same instruction is fetched and executed.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 10 to Pin 30) .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[3]	−55°C to +125°C	5V ±10%

Electrical Characteristics Over Commercial and Military Operating Range, V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V[4]

Parameter	Description		Test Condition	Min.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = Min. I_{OH} = −1.6 mA	2.4		V
V_{OL}	Output LOW Voltage		V_{CC} = Min. I_{OL} = 12 mA		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IH}	Input HIGH Current		V_{CC} = Max. V_{IN} = V_{CC}		10	μA
I_{IL}	Input LOW Current		V_{CC} = Max. V_{IN} = V_{SS}		−10	μA
I_{OH}	Output HIGH Current		V_{CC} = Min. V_{IH} = 2.4V	−1.6		mA
I_{OL}	Output LOW Current		V_{CC} = Min. V_{OL} = 0.4V	12		mA
I_{OZ}	Output Leakage Current		V_{CC} = Max. V_{OUT} = V_{SS}/V_{CC}	−40	+40	μA μA
I_{SC}	Output Short Circuit Current		V_{CC} = Max. V_{OUT} = 0V		−85	mA
I_{CC}	Supply Current	Commercial	V_{CC} = Max.		70	mA
		Military			90	
I_{CC1}	Supply Current	Commercial	$V_{IH} \geq 3.85V$, $V_{IL} \leq 0.4V$		35	mA
		Military			50	

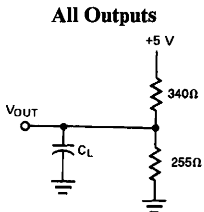
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	8	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

1. Not more than one output should be tested at a time. Duration of the short circuit should not exceed one second.
2. Tested initially and after any design or process changes that may affect these parameters.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.

Output Load used for AC Performance Characteristics

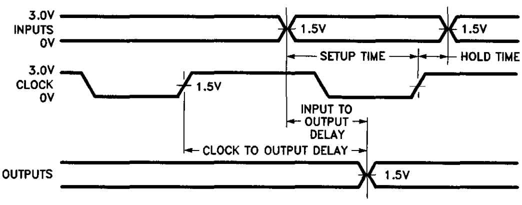


0041-4

Notes:

1. C_L = 50 pF includes scope probe, writing and stray capacitance.
2. C_L = 5 pF for output disable tests.

Switching Waveforms



0041-5

Guaranteed AC Performance Characteristics

The tables below specify the guaranteed AC performance of the CY7C910 over the commercial (0°C to +70°C) and the military (−55°C to +125°C) temperature ranges with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels.

The inputs switch between 0V and 3V with signal transition rates of 1 Volt per nanosecond. All outputs have maximum DC current loads.

Clock Requirements[1, 3]

	Commercial			Military		
CY7C910-	40	50	93	46	51	99
Minimum Clock LOW	20	20	50	23	25	58
Minimum Clock HIGH	20	20	35	23	25	42
Minimum Clock Period I = 14	40	50	93	46	51	100
Minimum Clock Period I = 8, 9, 15	40	50	113	46	51	114

Combinatorial Propagation Delays. C_L = 50 pF[3]

	Commercial									Military								
From Input	Y			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$			$\overline{FULL}$			Y			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$			$\overline{FULL}$		
CY7C910-	40	50	93	40	50	93	40	50	93	46	51	99	46	51	99	46	51	99
D0–D11	17	20	20	—	—	—	—	—	—	21	25	25	—	—	—	—	—	—
I0–I3	25	35	50	20	30	51	—	—	—	30	40	54	25	35	58	—	—	—
$\overline{CC}$	22	30	30	—	—	—	—	—	—	27	36	35	—	—	—	—	—	—
$\overline{CCEN}$	22	30	30	—	—	—	—	—	—	27	36	37	—	—	—	—	—	—
CP I = 8, 9, 15 (Note 2)	30	40	75	—	—	—	25	31	60	35	46	77	—	—	—	30	35	67
CP All Other I	30	40	55	—	—	—	25	31	60	35	46	61	—	—	—	30	35	67
$\overline{OE}$	21	25	35	—	—	—	—	—	—	22	25	40	—	—	—	—	—	—
(Note 2)	21	27	30	—	—	—	—	—	—	22	30	30	—	—	—	—	—	—

Minimum Set-Up and Hold Times Relative to clock LOW to HIGH Transition. C_L = 50 pF[3]

	Commercial						Military					
Input	Set-Up			Hold			Set-Up			Hold		
CY7C910-	40	50	93	40	50	93	46	51	99	46	51	99
DI → RC	13	16	24	0	0	0	13	16	28	0	0	0
DI → MPC	20	30	58	0	0	0	20	30	62	0	0	0
I0–I3	25	35	75	0	0	0	27	38	81	0	0	0
$\overline{CC}$	20	24	63	0	0	0	25	35	65	0	0	0
$\overline{CCEN}$	20	24	63	0	0	0	25	35	63	0	0	0
CI	15	18	46	0	0	0	15	18	58	0	0	0
$\overline{RLD}$	15	19	36	0	0	0	15	20	42	0	0	0

Notes:
1. A dash indicates that a propagation delay path or set-up time does not exist.
2. The enable/disable times are measured to a 0.5 Volt change on the output voltage level with C_L = 5 pF.
3. See the last page of this specification for Group A subgroup testing information.

Table of Instructions

I_3–I_0	Mnemonic	Name	Reg/Cntr Contents	Result: Fail $\overline{CCEN}$ = L and $\overline{CC}$ = H		Result: Pass $\overline{CCEN}$ = H or $\overline{CC}$ = L		Result: Reg/Cntr	Result: Enable
				Y	Stack	Y	Stack		
0	JZ	Jump Zero	X	0	Clear	0	Clear	Hold	PL
1	CJS	Cond JSB PL	X	PC	Hold	D	Push	Hold	PL
2	JMAP	Jump Map	X	D	Hold	D	Hold	Hold	Map
3	CJP	Cond Jump PL	X	PC	Hold	D	Hold	Hold	PL
4	PUSH	Push/Cond LD CNTR	X	PC	Push	PC	Push	(Note 1)	PL
5	JSRP	Cond JSB R/PL	X	R	Push	D	Push	Hold	PL
6	CJV	Cond Jump Vector	X	PC	Hold	D	Hold	Hold	Vect
7	JRP	Cond Jump R/PL	X	R	Hold	D	Hold	Hold	PL
8	RFCT	Repeat Loop, CNTR ≠ 0	≠0	F	Hold	F	Hold	Dec	PL
			=0	PC	POP	PC	Pop	Hold	PL
9	RPCT	Repeat PL, CNTR ≠ 0	≠0	D	Hold	D	Hold	Dec	PL
			=0	PC	Hold	PC	Hold	Hold	PL
10	CRTN	Cond RTN	X	PC	Hold	F	Pop	Hold	PL
11	CJPP	Cond Jump PL & Pop	X	PC	Hold	D	Pop	Hold	PL
12	LDCT	LD Cntr & Continue	X	PC	Hold	PC	Hold	Load	PL
13	LOOP	Test End Loop	X	F	Hold	PC	Pop	Hold	PL
14	CONT	Continue	X	PC	Hold	PC	Hold	Hold	PL
15	TWB	Three-Way Branch	≠0	F	Hold	PC	Pop	Dec	PL
			=0	D	Pop	PC	Pop	Hold	PL

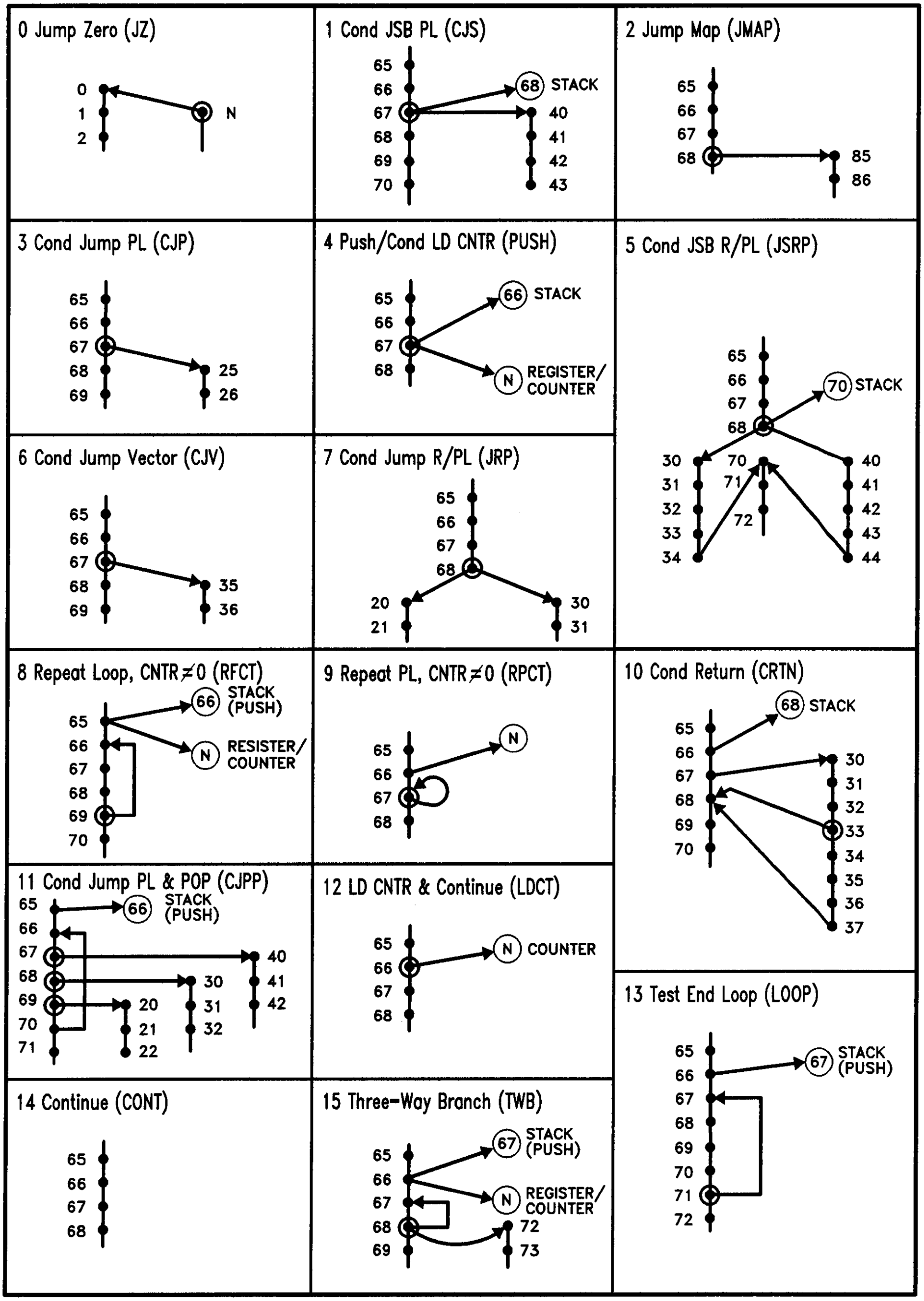
Notes:

1. If $\overline{CCEN}$ = L and $\overline{CC}$ = H, hold; else load.

H = HIGH L = LOW X = Don't Care

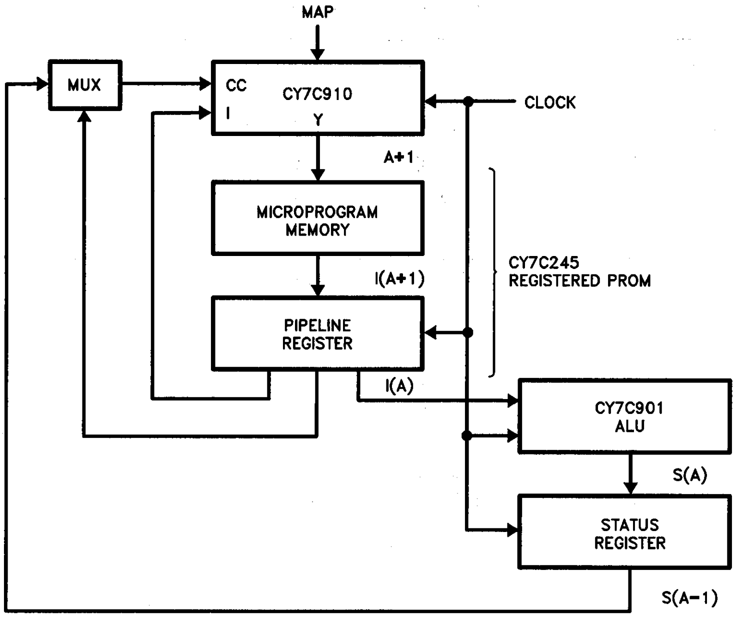
CY7C910 CMOS Microprogram Controller

CY7C910 Flow Diagrams

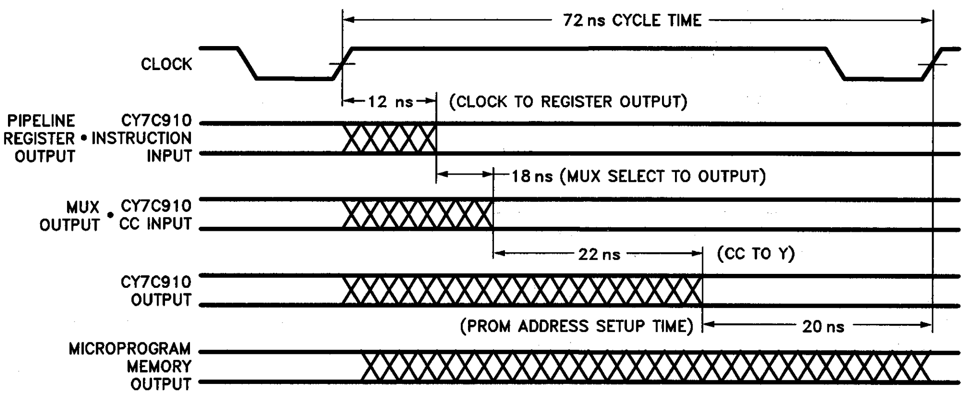


0041–9

One Level Pipeline Based Architecture (Recommended)



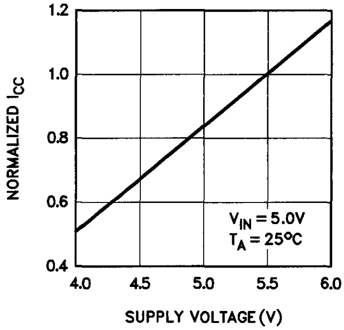
0041-6



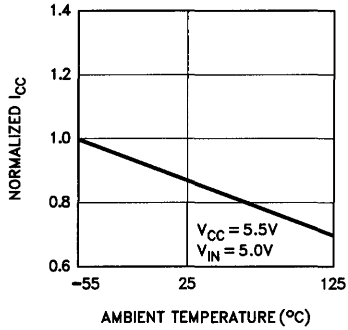
0041-7

Typical DC and AC Characteristics

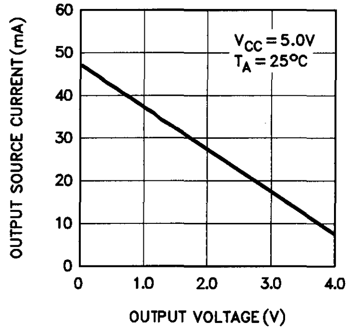
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



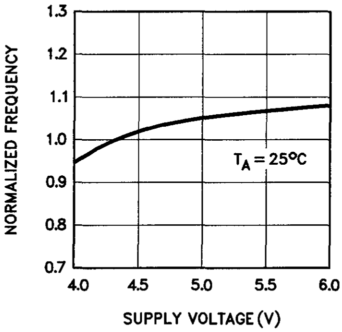
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



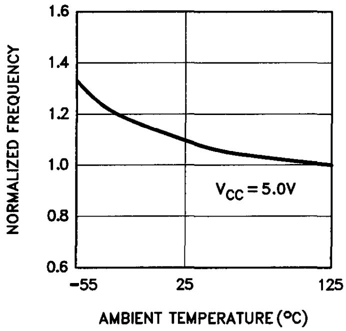
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



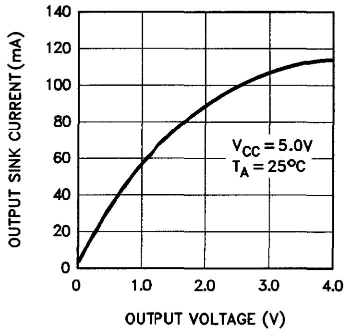
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



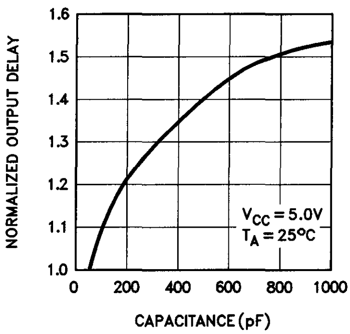
NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



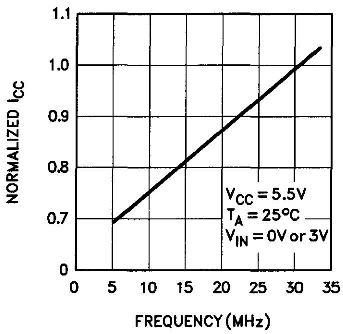
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0041–10

6

Ordering Information

Clock Cycle (ns)	Ordering Code	Package Type	Operating Range
40	CY7C910-40PC	P17	Commercial
	CY7C910-40DC	D18	
	CY7C910-40JC	J67	
	CY7C910-40LC	L67	
46	CY7C910-46DMB	D18	Military
	CY7C910-46LMB	L67	
50	CY7C910-50PC	P17	Commercial
	CY7C910-50DC	D18	
	CY7C910-50JC	J67	
	CY7C910-50LC	L67	
51	CY7C910-51DMB	D18	Military
	CY7C910-51LMB	L67	
93	CY7C910-93PC	P17	Commercial
	CY7C910-93DC	D18	
	CY7C910-93JC	J67	
	CY7C910-93LC	L67	
99	CY7C910-99DMB	D18	Military
	CY7C910-99LMB	L67	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IH}	1,2,3
I_{IL}	1,2,3
I_{OH}	1,2,3
I_{OL}	1,2,3
I_{OZ}	1,2,3
I_{SC}	1,2,3
I_{CC}	1,2,3
I_{CC1}	1,2,3

Clock Requirements

Parameters	Subgroups
Minimum Clock LOW	7,8,9,10,11

Combinational Propagation Delays

Parameters	Subgroups
From D0–D11 to Y	7,8,9,10,11
From I0–I3 to Y	7,8,9,10,11
From I0–I3 to $\overline{\text{PL}}$, $\overline{\text{VECT}}$, $\overline{\text{MAP}}$	7,8,9,10,11
From $\overline{\text{CC}}$ to Y	7,8,9,10,11
From $\overline{\text{CCEN}}$ to Y	7,8,9,10,11
From CP (I = 8,9,15) to $\overline{\text{FULL}}$	7,8,9,10,11
From CP (All Other I) to Y	7,8,9,10,11
From CP (All Other I) to $\overline{\text{FULL}}$	7,8,9,10,11

Document #: 38-00016-B

Minimum Set-up and Hold Times

Parameters	Subgroups
DI → RC Set-up Time	7,8,9,10,11
DI → RC Hold Time	7,8,9,10,11
DI → MPC Set-up Time	7,8,9,10,11
DI → MPC Hold Time	7,8,9,10,11
I0–I3 Set-up Time	7,8,9,10,11
I0–I3 Hold Time	7,8,9,10,11
$\overline{\text{CC}}$ Set-up Time	7,8,9,10,11
$\overline{\text{CC}}$ Hold Time	7,8,9,10,11
$\overline{\text{CCEN}}$ Set-up Time	7,8,9,10,11
$\overline{\text{CCEN}}$ Hold Time	7,8,9,10,11
CI Set-up Time	7,8,9,10,11
CI Hold Time	7,8,9,10,11
$\overline{\text{RLD}}$ Set-up Time	7,8,9,10,11
$\overline{\text{RLD}}$ Hold Time	7,8,9,10,11

CY7C9101

CMOS Sixteen-Bit Slice

CYPRESS SEMICONDUCTOR

Features

- **Fast**
  - **CY7C9101-30 has a 30 ns (max.) clock cycle (commercial)**
  - **CY7C9101-35 has a 35 ns (max.) clock cycle (military)**
- **Low Power**
  - **I_{CC} (max. at 10 MHz) = 60 mA (commercial)**
  - **I_{CC} (max. at 10 MHz) = 85 mA (military)**
- **V_{CC} Margin**
  - **5V ±10%**
- **All parameters guaranteed over commercial and military operating temperature range**
- **Replaces four 2901's with carry look-ahead logic**
- **Eight Function ALU**
  - **Performs three arithmetic and five logical operations on two 16-bit operands**
- **Expandable**
  - **Infinitely expandable in 16-bit increments**
- **Four Status Flags**
  - **Carry, overflow, negative, zero**
- **ESD Protection**
  - **Capable of withstanding greater than 2000V static discharge voltage**
- **Pin compatible and functionally equivalent to AM29C101**

Functional Description

The CY7C9101 is a high-speed, expandable, 16-bit wide ALU slice which can be used to implement the arithmetic section of a CPU, peripheral controller, or programmable controller. The instruction set of the CY7C9101 is basic, yet so versatile that it can emulate the ALU of almost any digital computer.

The CY7C9101, as shown in the block diagram, consists of a 16-word by 16-bit dual-port RAM register file, a 16-bit ALU, and the necessary data manipulation and control logic.

The function performed is determined by the nine-bit instruction word (I_8 to I_0) which is usually input via a microinstruction register.

The CY7C9101 is expandable in 16-bit increments, has three-state data outputs as well as flag outputs, and can implement either a full look-ahead carry or a ripple carry.

The CY7C9101 is a pin compatible, functional equivalent of the Am29C101 with improved performance. The 7C9101 replaces four 2901's and includes on-chip carry look-ahead logic.

Fabricated in an advanced 1.2 micron CMOS process, the 7C9101 eliminates latchup, has ESD protection greater than 2000V, and achieves superior performance with low power dissipation.

Logic Block Diagram

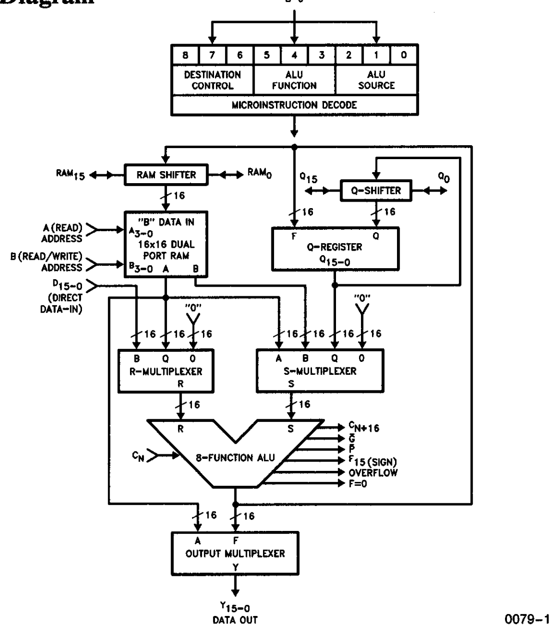
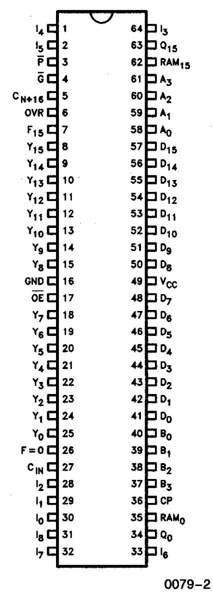


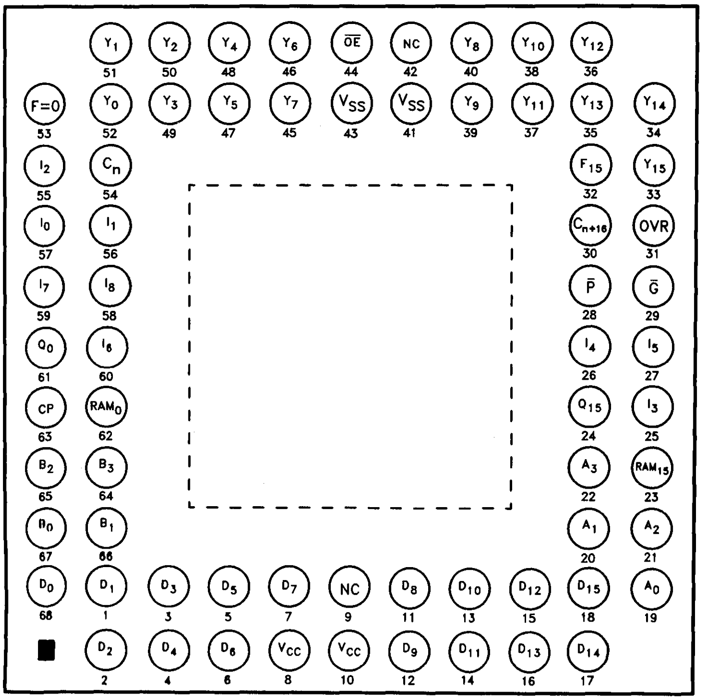
Figure 1

Pin Configuration

Top View



Top View

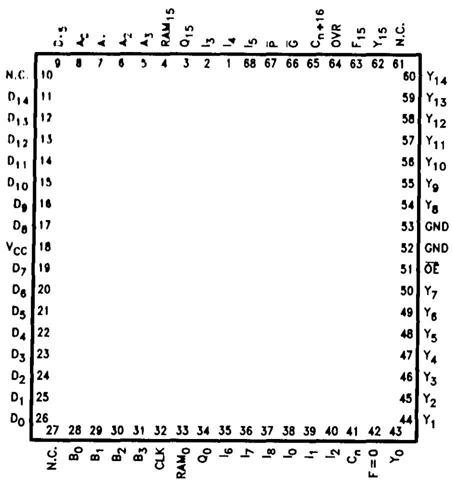


0079-11

CY7C9101 Pinout for 68PGA

NC = No Connect

Top View



0079-3

CY7C9101 Pinout for LCC/PLCC

NC = No Connect

Selection Guide

		7C91 7C91
Minimum Clock Cycle (ns)	Commercial	30
	Military	35
Maximum Operating Current at 10 MHz (mA)	Commercial	60
	Military	85

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 30 mA

Static Discharge Voltage ....
(Per MIL-STD-883 Method 30.

Latchup Current (Outputs).....

Operating Range

Range	Ambient Temperature
Commercial	0°C to +70°C
Military[1]	−55°C to +125°C

Note:
1. T_A is the "instant on" case temperature.

Pin Definitions

Signal Name	I/O	Description
A_{3-0}	I	**RAM Address A.** This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) A-port.
B_{3-0}	I	**RAM Address B.** This 4-bit address word selects one of the 16 registers in the register file for output on the (internal) B-port. When data is written back to the register file, this is the destination address.
I_{8-0}	I	**Instruction Word.** This nine-bit word is decoded to determine the ALU data sources ($I_{0,1,2}$), the ALU operation ($I_{3,4,5}$), and the data to be written to the Q-register or register file ($I_{6,7,8}$).
D_{15-0}	I	**Direct Data Input.** This 16-bit data word may be selected by the $I_{0,1,2}$ lines as an input to the ALU.
Y_{15-0}	I	**Data Output.** These are three-state data output lines which, when enabled, output either the ALU result or the data in the A latch, as determined by the code on $I_{6,7,8}$.
$\overline{OE}$	I	**Output Enable.** This is an active LOW input which controls the Y_{15-0} outputs. A HIGH level on this signal places the output drivers at the high impedance state.
CP	I	**Clock.** The LOW level of CP is used to write data to the RAM register file. A HIGH level of CP writes data from the dual port RAM to the A and B latches. The operation of the Q register is similar; data is entered into the master latch on the LOW level of CP and transferred from master to slave during CP = HIGH.
Q_{15}, RAM_{15}	I/O	These two lines are bidirectional and are controlled by $I_{6,7,8}$. They are three-state output drivers connected to the TTL compatible CMOS inputs.

Signal Name	I/O	Description
Q_{15}, RAM_{15} (Cont.)	I/O	**Output Mode:** When the destination $I_{6,7,8}$ indicates a left shift (UP) oper three-state outputs are enabled and t the Q register is output on the Q_{15} pi likewise, the MSB of the ALU outpu output on the RAM 15 pin. **Input Mode:** When the destination co a right shift (DOWN), the pins are th inputs to the MSB of the Q register an RAM, respectively.
Q_0, RAM_0	I/O	These two lines are bidirectional and f similarly to the Q_{15} and RAM_{15} lines. and RAM_0 lines are the LSB of the Q and the RAM.
C_n	I	**Carry In.** The carry in to the internal A
C_{n+16}	O	**Carry Out.** The carry out from the inte
$\overline{G}$, $\overline{P}$	O	**Carry Generate, Carry Propagate.** Out the ALU which may be used to perforn look-ahead operation over the 16-bits o ALU.
OVR	O	**Overflow.** This signal is the logical exch of the carry-in and carry-out of the MSI ALU. This indicates when the result of t operation exceeded the capacity of the m two's complement number range. It is va for the sign bit.
F = 0	O	**Zero Detect.** Open drain output which g HIGH when the data on outputs (F_{15-0}) LOW. It indicates that the result of an A operation is zero (positive logic assumed)
F_{15}	O	**Sign.** The MSB of the ALU output.

Functional Tables

Table 1. ALU Source Operand Control

Mnemonic	Micro Code				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

Table 2. ALU Function Control

Mnemonic	Micro Code				ALU Function	Symbol
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	$R + S$
SUBR	L	L	H	1	S Minus R	$S - R$
SUBS	L	H	L	2	R Minus S	$R - S$
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \veebar S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Table 3. ALU Destination Control

Mnemonic	Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	None	None	$F \rightarrow Q$	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	$F \rightarrow B$	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	$F \rightarrow B$	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	$F/2 \rightarrow B$	DOWN	$Q/2 \rightarrow Q$	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	$F/2 \rightarrow B$	X	None	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	$2F \rightarrow B$	UP	$2Q \rightarrow Q$	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	$2F \rightarrow B$	X	None	F	IN_0	F_{15}	X	Q_{15}

X = Don't care. Electrically, the input shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
A = Register Addressed by A inputs.
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Table 4. Source Operand and ALU Function Matrix

	I_{210} Octal	0	1	2	3	4	5	6	7
Octal I_{543}	ALU Source / ALU Function	A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	$C_n = L$	$A+Q$	$A+B$	Q	B	A	$D+A$	$D+Q$	D
	R plus S								
	$C_n = H$	$A+Q+1$	$A+B+1$	$Q+1$	$B+1$	$A+1$	$D+A+1$	$D+Q+1$	$D+1$
1	$C_n = L$	$Q-A-1$	$B-A-1$	$Q-1$	$B-1$	$A-1$	$A-D-1$	$Q-D-1$	$-D-1$
	S minus R								
	$C_n = H$	$Q-A$	$B-A$	Q	B	A	$A-D$	$Q-D$	$-D$
2	$C_n = L$	$A-Q-1$	$A-B-1$	$-Q-1$	$-B-1$	$-A-1$	$D-A-1$	$D-Q-1$	$D-1$
	R minus S								
	$C_n = H$	$A-Q$	$A-B$	$-Q$	$-B$	$-A$	$D-A$	$D-Q$	D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

$+$ = Plus; $-$ = Minus; $\vee$ = OR; $\wedge$ = AND; $\veebar$ = EX-OR

Description of Architecture

General Description

The 7C9101 block diagram is shown in Figure 1. Detailed block diagrams show the operation of specific sections as described below. The device is a 16-bit slice consisting of a register file (16-word by 16-bit dual port RAM), the ALU, the Q-register and the necessary control logic. It is expandable in 16-bit increments.

Register File

The dual port RAM is addressed by two 4-bit address fields (A_{3-0} and B_{3-0}) which cause the data to simultaneously appear at the A or B (internal) ports. Both the A and B addresses may be identical; in this case, the same data will appear at both the A and B ports.

Data to be written to RAM is applied to the D inputs of the 7C9101 and is passed (unchanged) through the ALU to the RAM location specified by the B-address word. New data is written into the RAM by specifying a B address while RAM write enable (RAM EN) is active and the clock input is LOW. RAM EN is an internal signal decoded from the signals $I_{6,7,8}$. As shown below, each of the 16 RAM inputs is driven by a three-input multiplexer that allows the ALU output (F_{15-0}) to be shifted one bit position to the left, right, or not shifted. The RAM_{15} and RAM_0 I/O pins are also inputs to the 16-bit, 3-input multiplexer.

During the left shift (upshift) operation, the RAM_{15} output buffer and RAM_0 input multiplexer are enabled. For the down shift (right) operation, the RAM_0 output buffer and the RAM_{15} input multiplexer are enabled.

The A and B outputs of the RAM drive separate 16-bit latches that are enabled (track the RAM data) when the clock is HIGH. The outputs of the A latch go to three multiplexers which feed the two ALU inputs (R_{15-0} and S_{15-0}) and the chip output (Y_{15-0}). The B latch outputs are directed to the multiplexer which feeds the S input to the ALU.

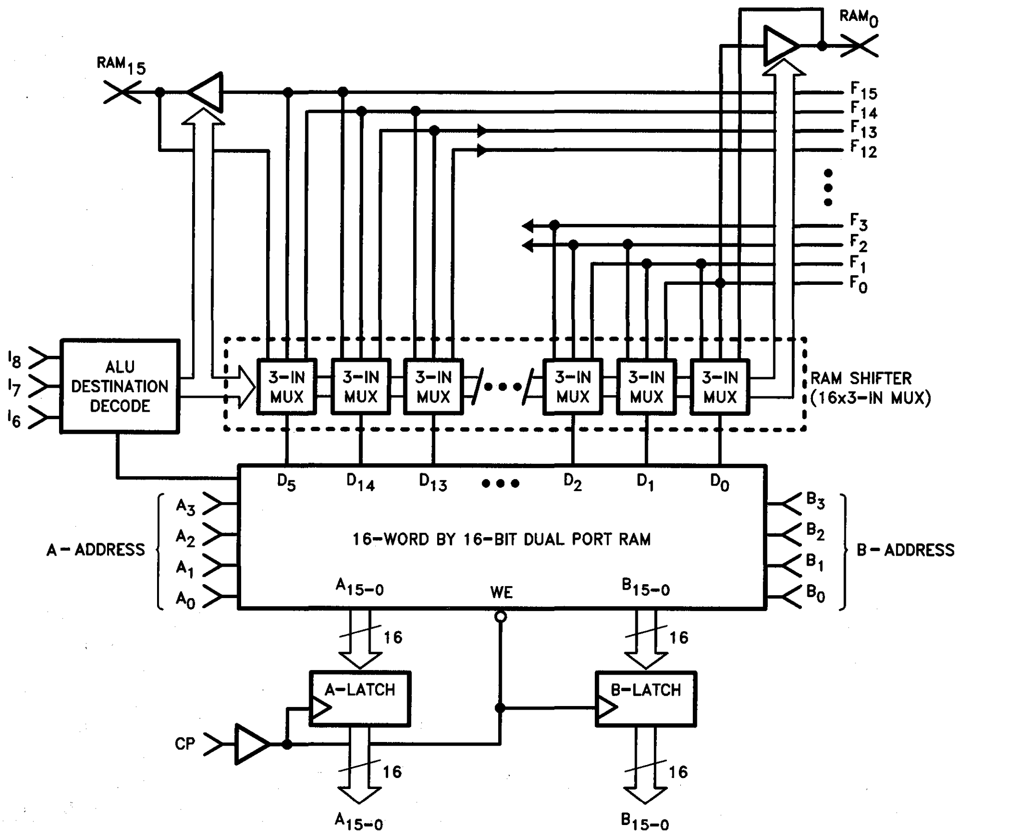
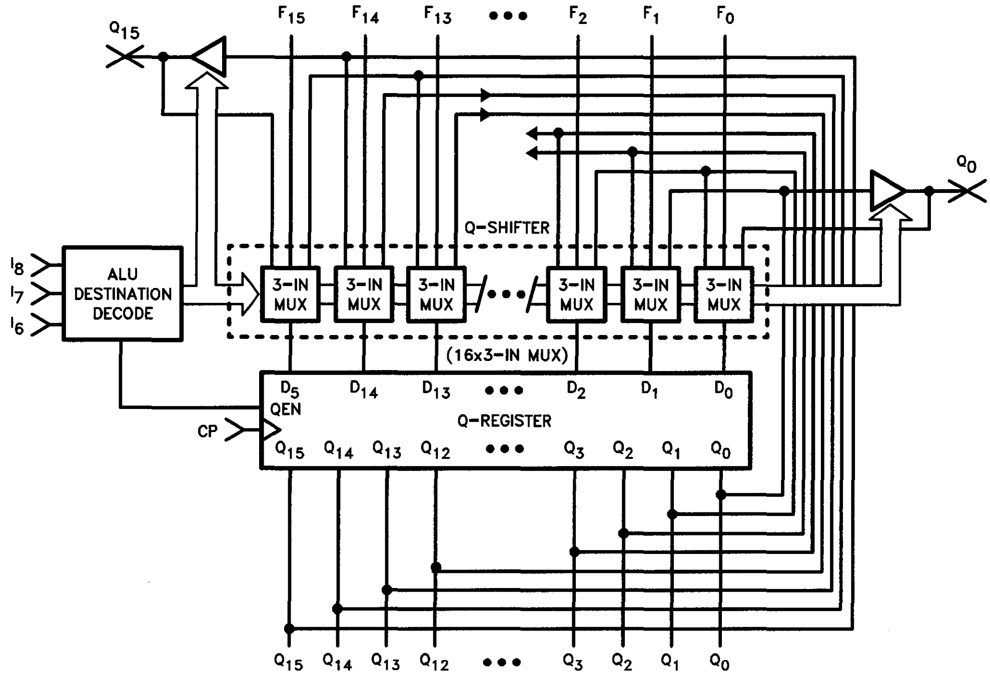


Figure 2. Register File

Description of Architecture (Continued)

Q-Register

The Q-register is mainly intended for use as a separate working register for multiplication and division routines. It may also function as an accumulator or temporary storage register. Sixteen master-slave latches are used to implement the Q-register. As shown below, the Q-register inputs are driven by the outputs of the Q-shifter (sixteen 3-input multiplexers, under the control of $I_{6, 7, 8}$). The function of the Q-register input multiplexers is to allow the ALU output (F_{15-0}) to be either shifted left, right, or directly entered into the master latches. The Q_{15} and Q_0 pins (I/O) function similarly to the RAM_{15} and RAM_0 pins described earlier. Data is entered into the master latches when the clock is LOW and transferred to the slave (output) at the clock LOW to HIGH transition.



0079-5

Figure 3. Q-Register

6

Description of Architecture (Continued)

ALU (Arithmetic Logic Unit)

The ALU can perform three arithmetic and five logical operations on the two 16-bit input operands, R and S. The R-input multiplexer selects between data from the RAM A-port and data at the external data input, D_{15-0}. The S-input multiplexer selects between data from the RAM A-port, the RAM B-port, and the Q-register. The R and S multiplexers are controlled by the $I_{0,1,2}$ inputs as shown in Table 1. The R and S input multiplexers each have an "inhibit capability," offering a state where no data is passed. This is equivalent to a source operand consisting of all zeroes. The R and S ALU source multiplexers are configured to allow eight pairs of combinations of A, B, D, Q, and "0" to be selected as ALU input operands.

The ALU functions, which are controlled by $I_{3,4,5}$, are shown in Table 2. Carry lookahead logic is resident on the 7C9101, using the ALU inputs carry in (C_n) and the ALU outputs carry propagate ($\overline{P}$), carry generate ($\overline{G}$), carry out (C_{n+16}), and overflow to implement carry lookahead arithmetic and determine if arithmetic overflow has occurred. Note that the carry in (C_n) signal affects the arithmetic result and internal flags; it has no effect on the logical operations.

Control signals $I_{6,7,8}$ route the ALU data output (F_{15-0}) to the RAM, the Q-register inputs, and the Y-outputs as shown in Table 3. The ALU result MSB (F_{15}) is output so the user may examine the sign bit without needing to enable the three-state outputs. The F = 0 output, used for zero detection, is HIGH when all bits of the F output are LOW. It is an open drain output which may be wire OR'ed across multiple 7C9101 processor slices.

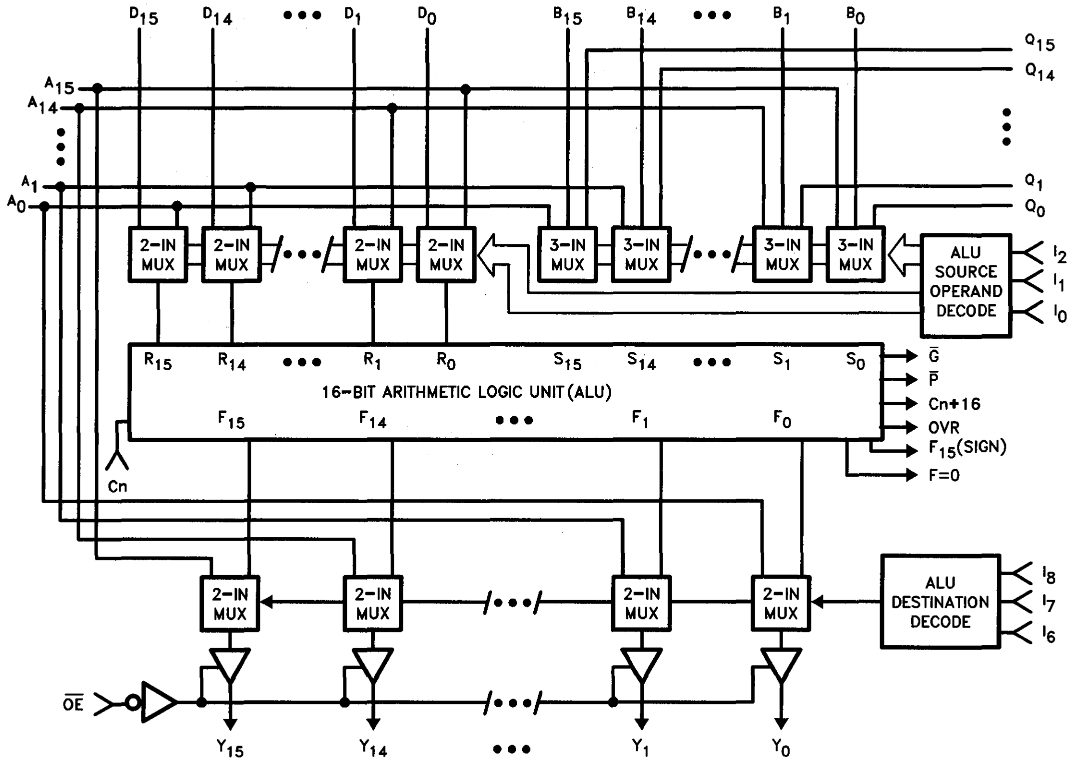


Figure 4. ALU

Description of Architecture (Continued)

Table 5. ALU Logic Mode Functions

Octal I_{543}, I_{210}	Group	Function
4 0 4 1 4 5 4 6	AND	$A \wedge Q$ $A \wedge B$ $D \wedge A$ $D \wedge Q$
3 0 3 1 3 5 3 6	OR	$A \vee Q$ $A \vee B$ $D \vee A$ $D \vee Q$
6 0 6 1 6 5 6 6	EX-OR	$A \veebar Q$ $A \veebar B$ $D \veebar A$ $D \veebar Q$
7 0 7 1 7 5 7 6	EX-NOR	$\overline{A \veebar Q}$ $\overline{A \veebar B}$ $\overline{D \veebar A}$ $\overline{D \veebar Q}$
7 2 7 3 7 4 7 7	INVERT	$\overline{Q}$ $\overline{B}$ $\overline{A}$ $\overline{D}$
6 2 6 3 6 4 6 7	PASS	Q B A D
3 2 3 3 3 4 3 7	PASS	Q B A D
4 2 4 3 4 4 4 7	"ZERO"	0 0 0 0
5 0 5 1 5 5 5 6	MASK	$\overline{A} \wedge Q$ $\overline{A} \wedge B$ $\overline{D} \wedge A$ $\overline{D} \wedge Q$

Table 6. ALU Arithmetic Mode Functions

Octal I_{543}, I_{210}	$C_n = 0$ (Low)		$C_n = 1$ (High)	
	Group	Function	Group	Function
0 0 0 1 0 5 0 6	ADD	A+Q A+B D+A D+Q	ADD plus one	A+Q+1 A+B+1 D+A+1 D+Q+1
0 2 0 3 0 4 0 7	PASS	Q B A D	Increment	Q+1 B+1 A+1 D+1
1 2 1 3 1 4 2 7	Decrement	Q−1 B−1 A−1 D−1	PASS	Q B A D
2 2 2 3 2 4 1 7	1's Comp.	−Q−1 −B−1 −A−1 −D−1	2's Comp. (Negate)	−Q −B −A −D
1 0 1 1 1 5 1 6 2 0 2 1 2 5 2 6	Subtract (1's Comp.)	Q−A−1 B−A−1 A−D−1 Q−D−1 A−Q−1 A−B−1 D−A−1 D−Q−1	Subtract (2's Comp.)	Q−A B−A A−D Q−D A−Q A−B D−A D−Q

Conventional Addition and Pass-Increment/Decrement

When the carry-in is HIGH and either a conventional addition or a PASS operation is performed, one (1) is added to the result. If the DECREMENT operation is performed when the carry-in is LOW, the value of the operand is reduced by one. However, when the same operation is performed when the carry-in is HIGH, it nullifies the DECREMENT operation so that the result is equivalent to the PASS operation. In logical operations, the carry-in (C_n) will not affect the ALU output.

Subtraction

Recall that in two's complement integer coding −1 is equal to all ones and that in one's complement integer coding zero is equal to all ones. To convert a positive integer to its two's complement (negative) equivalent, invert (complement) the number and add 1 to it; i.e., TWC = ONC + 1. In Table 6 the symbol −Q represents the two's complement of Q so that the one's complement of Q is then −Q −1.

Electrical Characteristics Over Commercial and Military Operating Range[4]

V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

Parameters	Description		Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = Min. $I_{OH} = -3.4$ mA	2.4		V
V_{OL}	Output LOW Voltage		V_{CC} = Min. I_{OL} = 16 mA		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			−3.0	0.8	V
I_{IX}	Input Leakage Current		$V_{SS} \leq V_{IN} \leq V_{CC}$ V_{CC} = Max.	−10	10	μA
I_{OH}	Output HIGH Current		V_{CC} = Min. V_{OH} = 2.4V	−3.4		mA
I_{OL}	Output LOW Current		V_{CC} = Min. V_{OL} = 0.4V	16		mA
I_{OZ}	Output Leakage Current		V_{CC} = Max. $V_{OUT} = V_{SS}$ to V_{CC}	 −40	+40	μA μA
I_{SC}	Output Short Circuit Current[1]		V_{CC} = Max. V_{OUT} = 0V		−85	mA
$I_{CC}(Q_1)$[2]	Supply Current (Quiescent)	Commercial	$V_{SS} \leq V_{IN} \leq V_{IL}$ or $V_{IH} \leq V_{IN} \leq V_{CC}$; $\overline{OE}$ = HIGH		30	mA
		Military			35	
$I_{CC}(Q_2)$[2]	Supply Current (Quiescent)	Commercial	$V_{SS} \leq V_{IN} \leq 0.4V$ or $3.85V \leq V_{IN} \leq V_{CC}$; $\overline{OE}$ = HIGH		25	mA
		Military			30	
$I_{CC}(Max.)$[2]	Supply Current	Commercial	V_{CC} = Max., f_{CLK} = 10 MHz; $\overline{OE}$ = HIGH		60	mA
		Military			85	

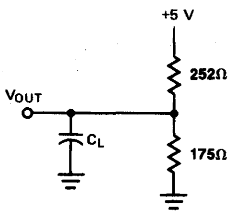
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

Notes:

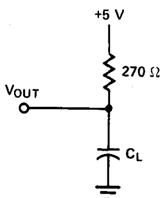
1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. Two quiescent figures are given for different input voltage ranges. To calculate I_{CC} at any given frequency, use $I_{CC}(Q_1) + I_{CC}(A.C.)$ where $I_{CC}(Q_1)$ is shown above and $I_{CC}(A.C.)$ = (3 mA/MHz) × Clock Frequency for the Commercial temperature range. $I_{CC}(A.C.)$ = (5 mA/MHz) × Clock Frequency for Military temperature range.
3. Tested initially and after any design or process changes that may affect these parameters.
4. See the last page of this specification for Group A subgroup testing information.

Output Loads used for AC Performance Characteristics



0079-9

All Outputs except Open Drain



0079-10

Open Drain (F = 0)

Notes:

1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.

Table 7. Logic Functions for CARRY and OVERFLOW Conditions

I_{543}	Function	$\overline{P}$	$\overline{G}$	$C_n + 16$	OVR
0	R + S	$\overline{P_0 - P_{15}}$	$\overline{G_{15} + P_{15}G_{14} + P_{15}P_{14}G_{13} + \ldots + P_{1-15}G_0}$	C_{16}	$C_{16} \veebar C_{15}$
1	S − R	←	Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions		→
2	R − S	←	Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions		→
3	R ∨ S	HIGH	HIGH	LOW	LOW
4	R ∧ S				
5	$\overline{R}$ ∧ S				
6	R ⊻ S				
7	$\overline{R \veebar S}$				

Definitions: + = OR

$P_{0-15} = P_{15}\,P_{14}\,P_{13}\,P_{12}\,P_{11}\,P_{10}\,P_9\,P_8\,P_7\,P_6\,P_5\,P_4\,P_3\,P_2\,P_1\,P_0$
$P_0 = R_0 + S_0$
$P_1 = R_1 + S_2$
$P_2 = R_2 + S_2$
$P_3 = R_3 + S_3$, etc.

$G_{0-15} = G_{15}\,G_{14}\,G_{13}\,G_{12}\,G_{11}\,G_{10}\,G_9\,G_8\,G_7\,G_6\,G_5\,G_4\,G_3\,G_2\,G_1\,G_0$
$G_0 = R_0\,S_0$
$G_1 = R_1\,S_1$
$G_2 = R_2\,S_2$
$G_3 = R_3\,S_3$, etc.
$C_{16} = G_{15} + P_{15}\,G_{14} + P_{15}\,P_{14}\,G_{13} + \ldots + P_{0-15}\,C_n$
$C_{15} = G_{14} + P_{14}\,G_{13} + P_{14}\,P_{13}\,G_{12} + \ldots + P_{0-14}\,C_n$

CY7C9101-30 and CY7C9101-40 Guaranteed Commercial Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Commercial (0°C to 70°C) and Military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See also loading circuit information.

This data applies to parts with the following numbers:

CY7C9101-30PC CY7C9101-30DC CY7C9101-30LC CY7C9101-30JC CY7C9101-30GC
CY7C9101-40PC CY7C9101-40DC CY7C9101-40LC CY7C9101-40JC CY7C9101-40GC

Cycle Time and Clock Characteristics

CY7C9101-	30	40
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	30 ns	40 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	33 MHz	25 MHz
Minimum Clock LOW Time	20 ns	25 ns
Minimum Clock HIGH Time	10 ns	15 ns
Minimum Clock Period	30 ns	40 ns

Combinational Propagation Delays. C_L = 50 pF

To Output / From Input	Y		F_{15}		$C_n + 16$		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_{15}		Q_0 Q_{15}	
CY7C9101-	30	40	30	40	30	40	30	40	30	40	30	40	30	40	30	40
A, B Address	37	47	36	47	35	44	32	41	35	46	32	42	32	40	—	—
D	29	34	28	34	25	32	25	30	29	36	21	26	27	33	—	—
C_n	22	27	22	27	20	25	—	—	22	26	22	26	24	30	—	—
$I_{0, 1, 2}$	32	40	32	40	30	38	28	36	34	42	26	32	27	35	—	—
$I_{3, 4, 5}$	34	43	33	42	33	42	27	35	34	40	32	42	29	38	—	—
$I_{6, 7, 8}$	19	22	—	—	—	—	—	—	—	—	—	—	22	26	22	26
A Bypass ALU (I = 2XX)	25	30	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock ⟋	31	40	30	39	30	38	27	34	28	37	27	34	27	35	20	23

Set-Up and Hold Times Relative to Clock (CP) Input[1]

Input	CP: Set-Up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H	
CY7C9101-	**30**	**40**	**30**	**40**	**30**	**40**	**30**	**40**
A, B Source Address	10	15	3[3]	3[3]	30[4]	40[4]	0	0
B Destination Address	10	15	←	Do Not Change[2]		→	0	0
D	—	—	—	—	22	28	0	0
C_n	—	—	—	—	16	22	0	0
$I_{0, 1, 2}$	—	—	—	—	26	35	0	0
$I_{3, 4, 5}$	—	—	—	—	29	37	0	0
$I_{6, 7, 8}$	10	12	←	Do Not Change[2]		→	0	0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	—	—	11	14	0	0

Output Enable/Disable Times

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C9101-30	$\overline{OE}$	Y	18	16
CY7C9101-40	$\overline{OE}$	Y	22	19

Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

CY7C9101-35 and CY7C9101-45 Guaranteed Military Range AC Performance Characteristics

The tables below specify the guaranteed AC performance of these devices over the Military (−55°C to +125°C) operating temperature range with V_{CC} varying from 4.5V to 5.5V. All times are in nanoseconds and are measured between the 1.5V signal levels. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads. See also loading circuit information.

This data applies to parts with the following numbers:

CY7C9101-35DMB CY7C9101-35LMB CY7C9101-35GMB
CY7C9101-45DMB CY7C9101-45LMB CY7C9101-45GMB

Cycle Time and Clock Characteristics[5]

CY7C9101-	35	45
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle).	35 ns	45 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	28 MHz	22 MHz
Minimum Clock LOW Time	23 ns	28 ns
Minimum Clock HIGH Time	12 ns	17 ns
Minimum Clock Period	35 ns	45 ns

Combinational Propagation Delays C_L = 50 pF[5]

To Output / From Input	Y		F_{15}		$C_n + 16$		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_{15}		Q_0 Q_{15}	
CY7C9101-	35	45	35	45	35	45	35	45	35	45	35	45	35	45	35	45
A, B Address	41	52	40	51	38	48	37	45	40	48	36	46	36	43	—	—
D	31	37	31	36	29	36	28	32	33	40	23	32	30	35	—	—
C_n	25	30	24	29	23	27	—	—	24	29	23	27	26	31	—	—
$I_{0, 1, 2}$	36	44	35	43	33	41	31	38	38	46	29	38	30	38	—	—
$I_{3, 4, 5}$	38	48	37	47	37	46	31	38	38	45	36	45	33	41	—	—
$I_{6, 7, 8}$	21	24	—	—	—	—	—	—	—	—	—	—	24	28	24	28
A Bypass ALU (I = 2XX)	28	33	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Clock ↗	35	44	34	43	34	42	30	37	34	40	28	38	30	37	21	25

Set-Up and Hold Times Relative to Clock (CP) Input[1, 5]

Input	CP: Set-Up Time Before H → L		Hold Time After H → L		Set-Up Time Before L → H		Hold Time After L → H	
CY7C9101-	35	45	35	45	35	45	35	45
A, B Source Address	12	17	3[3]	3[3]	35[4]	45[4]	0	0
B Destination Address	12	17	←	Do Not Change[2]		→	1	1
D	—	—	—	—	25	30	0	0
C_n	—	—	—	—	19	24	0	0
$I_{0, 1, 2}$	—	—	—	—	30	37	0	0
$I_{3, 4, 5}$	—	—	—	—	33	40	0	0
$I_{6,7,8}$	12	16	←	Do Not Change[2]		→	0	0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	—	—	13	15	1	1

Output Enable/Disable Times[5]

Output disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage level.

Device	Input	Output	Enable	Disable
CY7C9101-35	$\overline{OE}$	Y	20	17
CY7C9101-45	$\overline{OE}$	Y	23	20

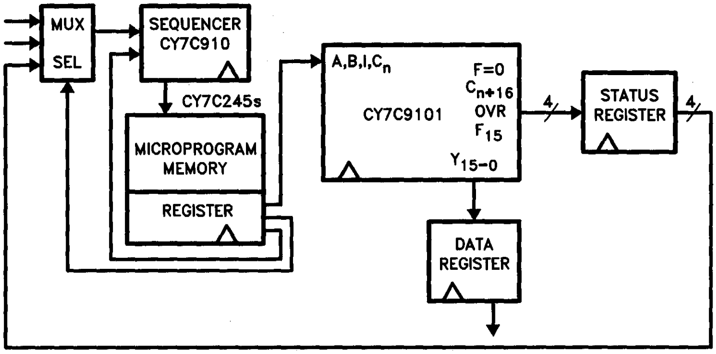
Notes:

1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.
5. See the last page of this specification for Group A subgroup testing information.

Applications

Minimum Cycle Time Calculations for 16-Bit Systems

Speeds used in calculations for parts other than CY7C9101 and CY7C910 are representative for available MSI parts.

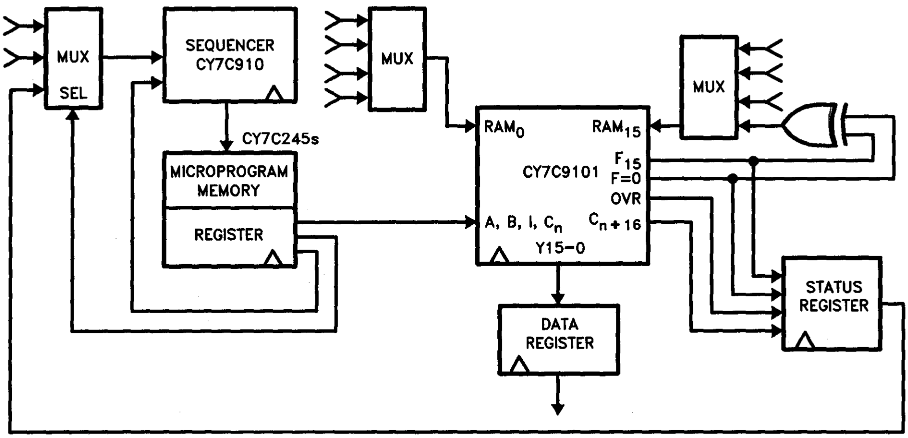


0079-15

Pipelined System, Add without Simultaneous Shift

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C901	A, B to Y, C_{n+16}, OVR	37	MUX	Select to Output	12
Register	Setup	4	CY7C910	CC to Output	22
		53 ns	CY7C245	Access Time	20
					66 ns

Minimum Clock Period = 66 ns



0079-13

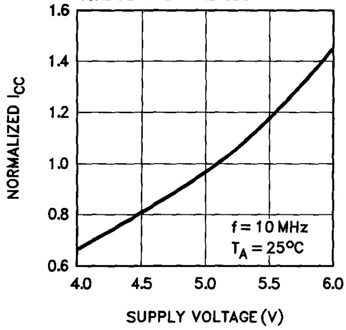
Pipelined System, Simultaneous Add and Shift Down (RIGHT)

	Data Loop			Control Loop	
CY7C245	Clock to Output	12	CY7C245	Clock to Output	12
CY7C9101	A, B to Y, C_{n+16}, OVR	37	MUX	Select to Output	12
XOR and MUX	Prop. Delay, Select to Output	20	CY7C910	CC to Output	22
CY7C9101	RAM_{15} Setup	11	CY7C245	Access Time	20
		80 ns			66 ns

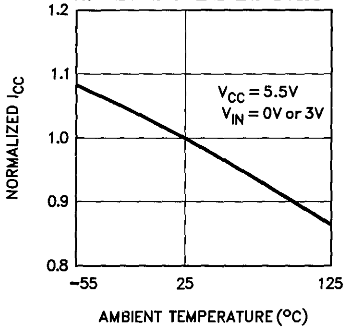
Minimum Clock Period = 80 ns

Typical DC and AC Characteristics

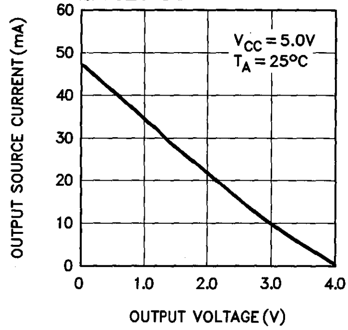
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



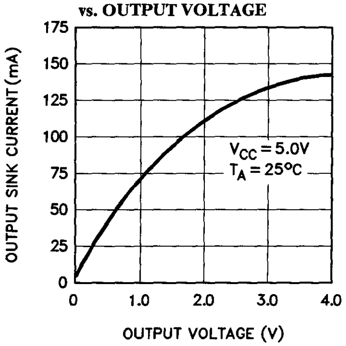
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



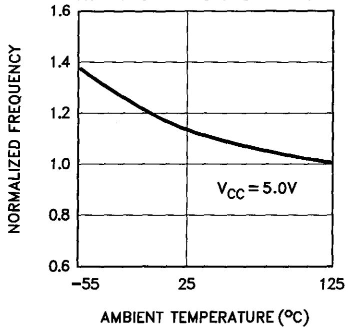
OUTPUT SOURCE CURRENT vs. VOLTAGE



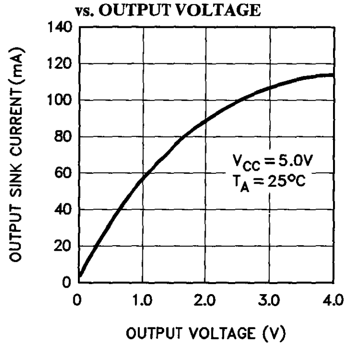
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



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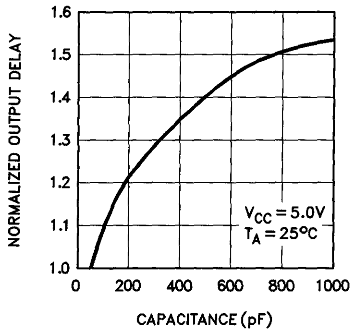
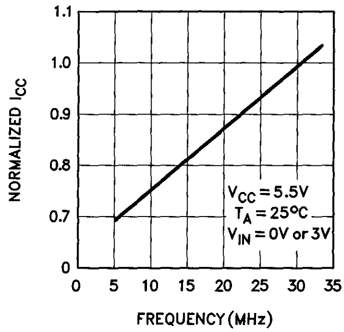
TYPICAL OUTPUT DELAY CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0079–14

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
30	CY7C9101-30 PC	P29	Commercial
	CY7C9101-30 LC	L81	
	CY7C9101-30 JC	J81	
	CY7C9101-30 DC	D30	
	CY7C9101-30 GC	G68	
40	CY7C9101-40 PC	P29	
	CY7C9101-40 LC	L81	
	CY7C9101-40 JC	J81	
	CY7C9101-40 DC	D30	
	CY7C9101-40 GC	G68	
35	CY7C9101-35 LMB	L81	Military
	CY7C9101-35 DMB	D30	
	CY7C9101-35 GMB	G68	
45	CY7C9101-45 LMB	L81	
	CY7C9101-45 DMB	D30	
	CY7C9101-45 GMB	G68	

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{SC}	1,2,3
I_{CC} (Q1)	1,2,3
I_{CC} (Q2)	1,2,3
I_{CC} (Max.)	1,2,3

Combinational Propagation Delays

Parameters	Subgroups
From A, B Address to Y	7,8,9,10,11
From A, B Address to F_{15}	7,8,9,10,11
From A, B Address to C_{n+16}	7,8,9,10,11
From A, B Address to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From A, B Address to F = 0	7,8,9.10,11
From A, B Address to OVR	7,8,9,10,11
From A, B Address to $RAM_{0, 15}$	7,8,9,10,11
From D to Y	7,8,9,10,11
From D to F_{15}	7,8,9,10,11
From D to C_{n+16}	7,8,9,10,11
From D to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From D to F = 0	7,8,9,10,11
From D to OVR	7,8,9,10,11
From D to $RAM_{0, 15}$	7,8,9,10,11
From C_n to Y	7,8,9,10,11
From C_n to F_{15}	7,8,9,10,11
From C_n to C_{n+16}	7,8,9,10,11

Combinational Propagation Delays (Continued)

Parameters	Subgroups
From C_n to F = 0	7,8,9,10,11
From C_n to OVR	7,8,9,10,11
From C_n to $RAM_{0, 15}$	7,8,9,10,11
From I_{012} to Y	7,8,9,10,11
From I_{012} to F_{15}	7,8,9,10,11
From I_{012} to C_{n+16}	7,8,9,10,11
From I_{012} to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From I_{012} to F = 0	7,8,9,10,11
From I_{012} to OVR	7,8,9,10,11
From I_{012} to $RAM_{0, 15}$	7,8,9,10,11
From I_{345} to Y	7,8,9,10,11
From I_{345} to F_{15}	7,8,9,10,11
From I_{345} to C_{n+16}	7,8,9,10,11
From I_{345} to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From I_{345} to F = 0	7,8,9,10,11
From I_{345} to OVR	7,8,9,10,11
From I_{345} to $RAM_{0, 15}$	7,8,9,10,11
From I_{678} to Y	7,8,9,10,11
From I_{678} to $RAM_{0, 15}$	7,8,9,10,11
From I_{678} to $Q_{0, 15}$	7,8,9,10,11
From A Bypass ALU to Y (I = 2XX)	7,8,9,10,11
From Clock $\uparrow$ to Y	7,8,9,10,11
From Clock $\uparrow$ to F_{15}	7,8,9,10,11
From Clock $\uparrow$ to C_{n+16}	7,8,9,10,11
From Clock $\uparrow$ to $\overline{G}$, $\overline{P}$	7,8,9,10,11
From Clock $\uparrow$ to F = 0	7,8,9,10,11
From Clock $\uparrow$ to OVR	7,8,9,10,11
From Clock $\uparrow$ to $RAM_{0, 15}$	7,8,9,10,11
From Clock $\uparrow$ to $Q_{0, 15}$	7,8,9,10,11

Set-up and Hold Times Relative to Clock (CP) Input

Parameters	Subgroups
A, B Source Address Set-up Time Before H → L	7,8,9,10,11
A, B Source Address Hold Time After H → L	7,8,9,10,11
A, B Source Address Set-up Time Before L → H	7,8,9,10,11
A, B Source Address Hold Time After L → H	7,8,9,10,11
B Destination Address Set-upTime Before H → L	7,8,9,10,11
B Destination Address Hold Time After H → L	7,8,9,10,11
B Destination Address Set-upTime Before L → H	7,8,9,10,11
B Destination Address Hold Time After L → H	7,8,9,10,11
D Set-up Time Before L → H	7,8,9,10,11

Parameters	Subgroups
D Hold Time After L → H	7,8,9,10,11
C_n Set-up Time Before L → H	7,8,9,10,11
C_n Hold Time After L → H	7,8,9,10,11
I_{012} Set-up Time Before L → H	7,8,9,10,11
I_{012} Hold Time After L → H	7,8,9,10,11
I_{345} Set-up Time Before L → H	7,8,9,10,11
I_{345} Hold Time After L → H	7,8,9,10,11
I_{678} Set-up Time Before H → L	7,8,9,10,11
I_{678} Hold Time After H → L	7,8,9,10,11
I_{678} Set-up Time Before L → H	7,8,9,10,11
I_{678} Hold Time After L → H	7,8,9,10,11
RAM_0, RAM_{15}, Q_0, Q_{15} Set-up Time Before L → H	7,8,9,10,11
RAM_0, RAM_{15}, Q_0, Q_{15} Hold Time After L → H	7,8,9,10,11

Document #: 38-00017-B

CYPRESS SEMICONDUCTOR

CMOS 16-Bit Microprogrammed ALU

Features

- Fast
  - 35 ns worst case propagation delay, I to Y
- Low power CMOS
  - I_{CC} (max. at 10 MHz) = 145 mA (commercial)
  - I_{CC} (max. static) = 68 mA (commercial)
- V_{CC} margin
  - 5V ±10%
  - All parameters guaranteed over commercial and military operating temperature range
- Instruction set and architecture optimized for high speed controller applications
- CY7C9117 separate I/O
  - One and two operand arithmetic and logical operations
  - Bit manipulation, field insertion/extraction instructions
  - Eleven types of instructions
- Immediate instruction capability
- 16-bit barrel shifter capability
- 32-word x 16-bit register file
- 8-bit status register
  - Four ALU status bits
  - Link bit and three user definable status bits
- ESD protection
  - Capable of withstanding greater than 2001V static discharge voltage
- Pin compatible and functionally equivalent to 29116, 29116A, 29C116, 29117, 29117A, 29C117

Functional Description

The CY7C9115, CY7C9116 and CY7C9117 are high speed 16-bit microprogrammed Arithmetic and Logic Units, (ALU).

The architecture and instruction set of the devices are optimized for peripheral controller applications such as disk controllers, graphics controllers, communications controllers, and modems.

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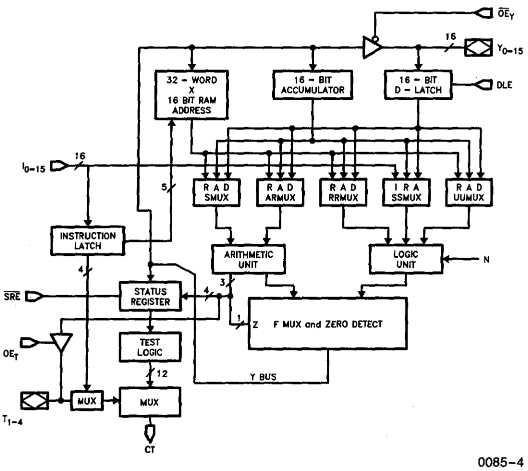
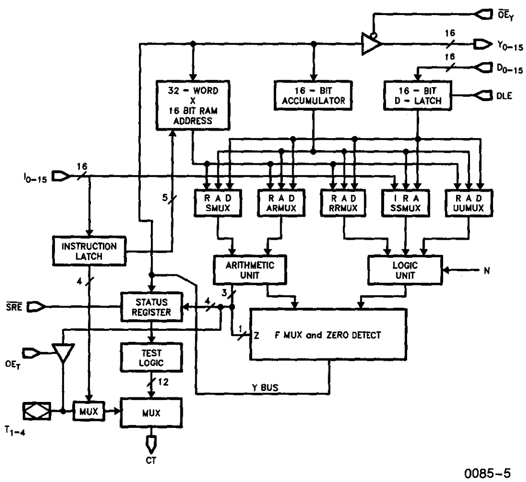


0085-4

Figure 1. CY7C9115, CY7C9116 Block Diagram



0085-5

Figure 2. CY7C9117 Block Diagram

Selection Guide

		7C9115-35 7C9116-35 7C9117-35	7C9115-40, 45 7C9116-40, 45 7C9117-40, 45	7C9115-65 7C9116-65 7C9117-65	7C9115-79 7C9116-79 7C9117-79
Worst Case I-Y Propagation Delay (ns)	Commercial	35	45	65	
	Military		40	65	79
Maximum Operating Current @ 10 MHz (mA)	Commercial	145	145	145	
	Military		166	166	166

Functional Description (Continued)

When used with the CY7C517 multiplier, the CY7C9115, CY7C9116 and CY7C9117 also support microprogrammed processor applications.

The CY7C9115, CY7C9116 and CY7C9117 are shown in the block diagram, consists of a 32-word by 16-bit single-port RAM register file, a 16-bit arithmetic unit and logic unit, an instruction latch and decoder, a data latch, an accumulator register, a 16-bit barrel shifter, a priority encoder, a status register, a condition code generator and multiplexer, and three-state output buffers.

The instruction set of the CY7C9115, CY7C9116 and CY7C9117 can be divided into eleven instruction types: single-operand, two-operand, single-bit shifts, rotate and merge, rotate and compare, rotate by n-bits, bit oriented instructions, prioritize, Cyclic Redundancy Check (CRC), status, and NO-OP. Instruction execution occurs in a single clock cycle except for Immediate Instructions, which require two clock cycles to execute.

The CY7C9116 and CY7C9117 are pin compatible, functional equivalent of the industry standard 29116, 29116A, 29C116, 29117, 29117A, 29C117 with improved performance.

Fabricated in an advanced 1.2 micron, two-level metal CMOS process, the CY7C9115, CY7C9116 and CY7C9117 eliminates latchup, has ESD protection greater than 2001V, and achieves superior performance with low power dissipation.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State...................... −0.5V to +7.0V

DC Input Voltage .... −3.0V to +7.0V

Output Current into Outputs (Low) .... 30 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015)

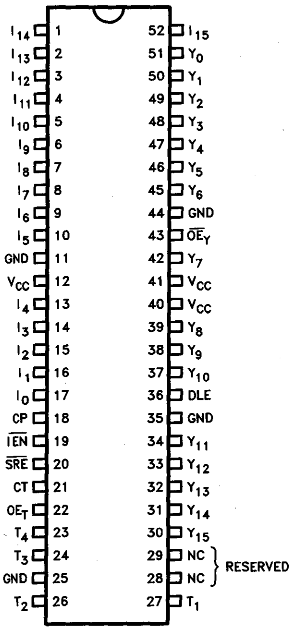
Latchup Current (Outputs).................. >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Military[1]	−55°C to +125°C	5V ±10%

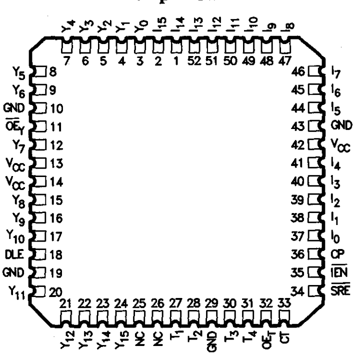
Note:
1. T_A is the "instant on" case temperature.

Pin Configurations CY7C9115, CY7C9116



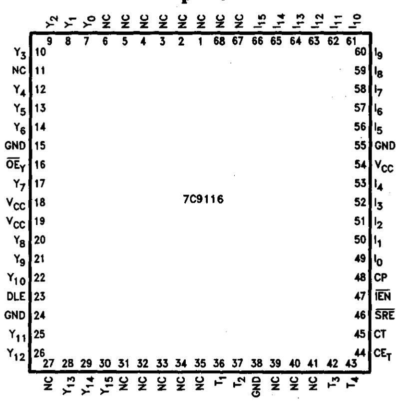
0085-2

7C9116 DIP



0085-3

7C9115 PLCC
7C9116 LCC



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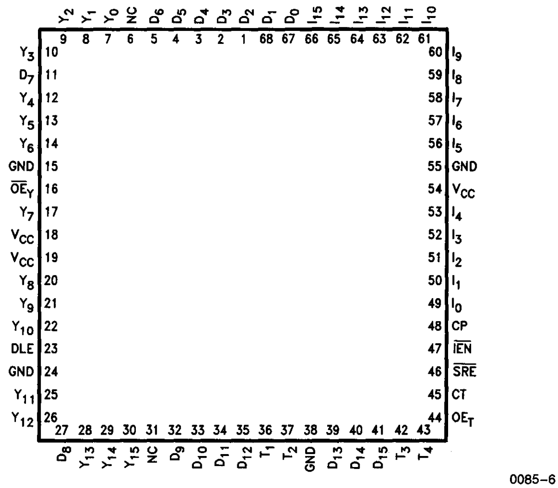
PLCC

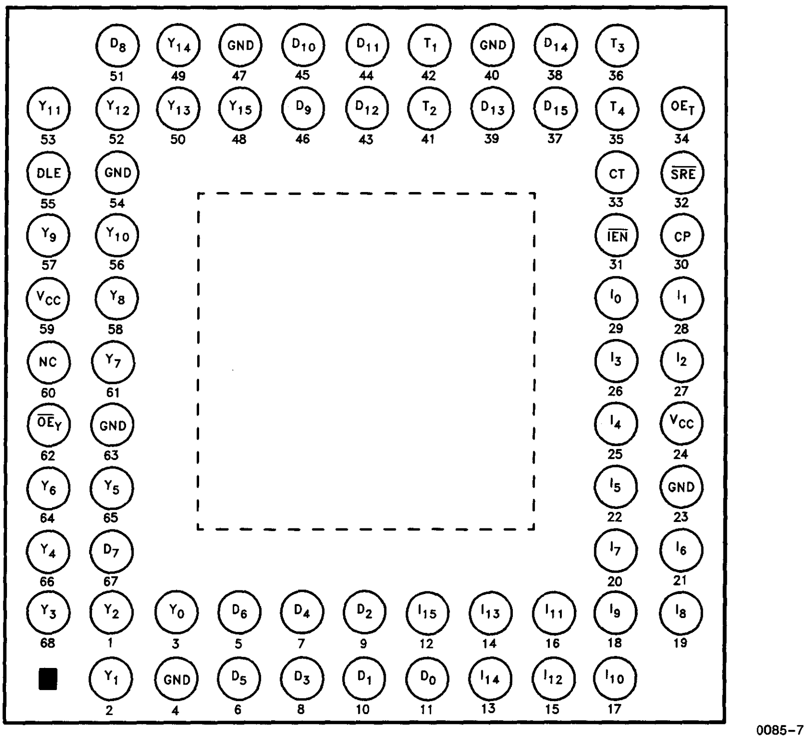
Pin Configurations CY7C9117

Top View



LCC/PLCC
NC = No Connect

Top View



CY7C9117 Pin for 68 PGA
NC = No Connect

Description of Architecture

The CY7C9115, CY7C9116 and CY7C9117 are 16-bit microprogrammed arithmetic and logic units comprised of the following sections (see block diagram):

- 32 Word x 16-Bit Register File
- Data Latch
- Instruction Latch and Decoder
- Accumulator
- Logic Unit with a 16-bit Barrel Shift Capability
- Arithmetic Unit
- Priority Encoder
- Condition Code Generator and Multiplexer
- Status Register
- Output Buffers

32-Word x 16-Bit Register File

The 32-word x 16-bit register file is a single port RAM with a 16-bit latch at the output. The latch is transparent while CP is HIGH and latched when CP is LOW. If $\overline{\text{IEN}}$ is LOW and the current instruction specifies the RAM at its destination, data is written into the RAM while CP is LOW. Word instructions write into all 16-bits of the RAM word addressed; byte instructions write into only the lower eight bits.

Use of an external multiplexer on five of the instruction inputs makes it possible to select separate read and write addresses for the same NON-IMMEDIATE instruction. Immediate Instructions do not allow this two-address operation for the 7C9115 and 7C9116. The 7C9117 does support two-address Immediate Instructions.

Data Latch

The data latch holds the 16-bit input to the CY7C9115, CY7C9116 and CY7C9117 from the Y (bidirectional) bus for the 7C9115 and 7C9116 and the data bus for the 7C9117. When DLE is HIGH, the latch is transparent, it is latched when DLE is LOW.

Instruction Latch and Decoder

The 16-bit instruction latch is always transparent, except when Immediate Instructions are executed. The Instruction Decoder decodes the instruction inputs into the internal signals which control the CY7C9115, CY7C9116 and CY7C9117. All instructions other than Immediate Instructions execute in a single clock cycle.

Execution of Immediate Instructions takes two clock cycles. During the first clock cycle, the Instruction Decoder identifies the instruction as an Immediate Instruction and the Instruction Latch captures the instruction at the instruction inputs. For Immediate Instructions, the data at the instruction inputs during the second clock cycle is used as one of the operands for the Immediate Instruction specified during the first clock cycle. Upon completion of the Immediate Instruction (the end of the second clock cycle), the Instruction Latch again becomes transparent.

Accumulator

The accumulator is a 16-bit edge triggered register. If the $\overline{\text{IEN}}$ is LOW and the current instruction specifies the accumulator as its destination, the accumulator accepts Y input data at the clock LOW to HIGH transition. Word instructions write into all 16 bits of the accumulator, byte instructions write into the lower eight bits.

16-Bit Barrel Shifter

The barrel shifter can rotate data input to it from either the register file, the accumulator, or the data latch from 0 to 15 bit positions. In word mode, the barrel shifter rotates a 16-bit word; in byte mode, it only affects the lower eight bits. The barrel shifter is used as one of the ALU inputs.

Arithmetic and Logic Unit

The CY7C9115, CY7C9116 and the CY7C9117 have an arithmetic unit and a logic unit. The arithmetic unit is capable of operating on one or two operands while the logic unit is capable of operating on one, two or three operands. The two units in parallel are able to execute the one and two operand instructions such as pass, complement, two's complement, add, subtract, AND, OR, EXOR, NAND, NOR, and EXNOR. Three operand instructions include rotate/merge and rotate/masked compare. There are three data types supported by the CY7C9115, CY7C9116 and CY7C9117; bit, byte, and 16-bit word.

All arithmetic and logic unit operations can be performed in either word or byte mode, with byte instructions performed only on the lower eight bits.

Three status output are generated by the arithmetic unit: carry (C), negative (N), and overflow (OVR). A zero flag (Z) detects a zero condition, though this flag is not generated by the arithmetic unit or the logic unit. These flags are generated in either word or byte mode, as appropriate.

The arithmetic unit uses full carry look-ahead across all 16 bits during arithmetic operations. The carry input to the arithmetic unit comes from the carry multiplexer, which can select either zero, one, or a stored carry bit (QC) from the status register. Multiprecision arithmetic uses QC as the carry input.

Priority Encoder

The priority encoder generates a binary-weighted code based on the location of the highest order ONE in its input word or byte. The operand to be prioritized may be AND-ed with a mask to eliminate certain bits from the priority encoding. This masking is performed by the logic unit.

In word mode, the output is a binary one if bit 15 is the first (unmasked) HIGH encountered, a binary two if bit 14 is the first HIGH and so on. If bit 0 is the only HIGH, the output of the priority encoder is binary 16. If no bits are HIGH, a binary zero is output.

In byte mode, only bits 7 through 0 are examined. Bit 7 HIGH produces a binary one, bit 6 a binary two, and so on. If bit 0 is the only HIGH, a binary eight is output; if no bits are HIGH, a binary zero is output.

Condition Code Generator and Multiplexer

The twelve condition code test signals are generated in this section. The multiplexer selects one of these twelve and places it at the CT output. The multiplexer is addressed by either using the Test Instruction or by using the bidirec-

Description of Architecture (Continued)

tional T bus as an input. The test instruction specifies the test condition to be placed at the CT output, but it does not allow an ALU operation at the same time. Using the T bus as input, the CY7C9115, CY7C9116 and CY7C9117 may simultaneously test and execute an instruction. The test instruction lines (I_{4-0}) take precedence over T_{4-1} for testing status.

Status Register

The 8-bit status word is held by the status register. The status register is updated at the end of all instructions except NO-OP, Save Status, and Test Status, provided the status register enable ($\overline{SRE}$) and instruction enable ($\overline{IEN}$) are both LOW. The status register is inhibited from changing if either $\overline{SRE}$ or $\overline{IEN}$ are HIGH.

The lower four status bits are the ALU status: OVR (overflow), N (negative), C (carry), and Z (zero). The upper four bits are a link bit and three user-defined status bits (Flag1, Flag2, Flag3).

As stated above, when $\overline{IEN}$ and $\overline{SRE}$ are LOW, the status register is updated at the end of all instructions other than NO-OP, Save Status, and Test Status. The lower four status bits are updated under the above conditions, with the additional exception of when $\overline{IEN}$ and $\overline{SRE}$ are LOW and the Status Set/Reset instruction is performed on the upper four bits. When $\overline{IEN}$ and $\overline{SRE}$ are LOW, the upper four status bits are only changed during their corresponding Status Set/Reset instructions and during Status Load instructions in word mode. The Link-Status bit is also updated after every shift instruction.

The status register can be loaded via the internal Y bus; it can also be selected as a source for the internal Y bus. Loading the status register in word mode updates all eight bits of the status register. In byte mode, only the lower four bits are updated.

Using the status register as a source in the word mode loads all eight bits into the lower byte of the destination; the upper byte is zero-filled. In byte mode, the status register loads the lower byte of the destination; however the upper byte is unchanged. Interrupt and subroutine processing is facilitated by this store/load combination, which allows saving and restoring the status register. The lower four bits of the status register can be read directly by outputting them to the T_{4-1} outputs. These outputs are enabled when OE_T is HIGH.

Output Buffers

Two sets of bidirectional buses exist on the CY7C9115 and CY7C9116. The bidirectional Y bus (16 bits) is controlled by $\overline{OE}_Y$. The three state outputs are enabled when $\overline{OE}_Y$ is LOW, they are at high impedance when $\overline{OE}_Y$ is HIGH. This will allow data to be input to the data latch from the external world. The second bidirectional bus is the four-bit T bus. These three state buffers are enabled by a HIGH on OE_T, which will output the internal ALU status bits (OVR, N, C, Z). If OE_T is LOW, the T outputs are at high impedance, and a test condition can be input on the T bus to determine the CT output.

The 7C9117 has separate Y bus output and Data Input buses. All other pins are functionally equivalent to the 7C9115 and 7C9116.

Pin Definitions

Signal Name	I/O	Description
Y_{15-0}	I/O	**Data Input/Output.** These bidirectional lines are used to directly load the 16-bit data latch when $\overline{OE}_Y$ is HIGH. When $\overline{OE}_Y$ is LOW, the arithmetic unit or the logic unit output data is output on Y_{15-0}.
I_{15-0}	I	**Instruction Word.** This 16-bit word selects the functions performed by the 7C9116. These lines are also used to input data when executing Immediate Instructions.
T_{4-1}	I/O	**Status Input/Output.** These bidirectional pins are used to output the lower four status bits (OV_R, N, C, and Z) when OE_T is HIGH. When OE_T is LOW, these lines are used as inputs to generate the conditional test (CT) output.
CT	O	**Conditional Test.** One of twelve condition code signals is selected by the condition code multiplexer to be placed on the CT output. CT = HIGH for a pass condition; CT = LOW for a fail condition.
DLE	I	**Data Latch Enable.** The 16-bit data latch is transparent when DLE is HIGH and latched when DLE is LOW.
$\overline{IEN}$	I	**Instruction Enable.** The following occurs with $\overline{IEN}$ LOW: Data may be written into the RAM when the clock is LOW, the Accumulator can accept data during the clock LOW to HIGH transition, and the Status Register can be updated when $\overline{SRE}$ is LOW. If $\overline{IEN}$ is HIGH, CT is disabled as a function of the instruction inputs. $\overline{IEN}$ should be LOW during the first half of the first cycle of Immediate Instructions.
$\overline{SRE}$	I	**Status Register Enable.** The Status Register is updated at the end of all instructions except NO-OP, Save Status, and Test Status when $\overline{SRE}$ and $\overline{IEN}$ are both LOW. The Status Register is inhibited from changing when either $\overline{SRE}$ or $\overline{IEN}$ are HIGH.
$\overline{OE}_Y$	I	**Y Output Enable.** This controls the 16-bit Y_{15-0} I/O port. When $\overline{OE}_Y$ is LOW, the Y-outputs are enabled, when $\overline{OE}_Y$ is HIGH, the Y outputs are disabled (high impedance).
OE_T	I	**T Output Enable.** The four bit T outputs are enabled when OE_T is HIGH: they are disabled (high impedance) when OE_T is LOW.
CP	I	**Clock Pulse.** The RAM output latch is transparent when CP is HIGH; the RAM output is latched when CP goes LOW. If $\overline{IEN}$ is LOW and the current instruction specifies the RAM as the destination, then data is written into the RAM while CP is LOW. If $\overline{IEN}$ is LOW, the Accumulator and Status Register will accept data at the clock LOW to HIGH transition. The instruction latch becomes transparent upon exiting an Immediate Instruction during a LOW to HIGH clock transition.
D_{15-0}	I	These input lines are used to directly load the data latch.
Y_{15-0}	I/O	These output lines are used to present the arithmetic unit or the logic unit output when $\overline{OE}_Y$ is LOW. (CY7C9117 Y_{15-0} and output only)

6

Instruction Set

The instruction set of the CY7C9115, CY7C9116 and CY7C9117 is optimized for peripheral controller applications. It features: Bit Set, Bit Reset, Bit Test, Rotate and Merge, Rotate and Compare, and Cyclic-Redundancy-Check (CRC) generation, in addition to standard Single- or Two-Operand logical and arithmetic instructions. A single clock cycle will execute all but the Immediate Instructions which take 2 clock cycles.

The CY7C9115, CY7C9116 and CY7C9117 can operate in three different data modes: bit, byte and word (16 bits). The LSB of the word is used for Byte Mode. Also in Byte Mode when the status register is specified as the destination, only the LSH (OVR, N, C, Z) of the register is updated. Save Status and Test Status instructions do not change the status register. During Test Status instructions the Y-bus (or D-bus for the CY7C9117) is undefined; the result is in the CT output.

The eleven instruction types outlined below are described in detail on the following pages.

Single-Operand	Rotate and Compare
Two-Operand	Prioritize
Single Bit Shift	CRC
Rotate and Merge	Status
Bit-Oriented	No-Op
Rotate by n Bits	

Table 1. Operand Source-Destination Combinations

Instruction Type	Operand Combinations (Note 1)		
	Source (R/S)		Destination
Single Operand SOR SONR	RAM (Note 2) ACC D D(OE) D(SE) I O		RAM ACC Y Bus Status ACC and Status
	Source (R)	Source (S)	Destination
Two Operand TOR1 TOR2 TONR	RAM RAM D D ACC D	ACC I RAM ACC I I	RAM ACC Y Bus Status ACC and Status
	Source (U)		Destination
Single Bit Shift SHFTR SHFTNR	RAM ACC ACC D D D		RAM ACC Y Bus RAM ACC Y Bus
	Source (U)		Destination
Rotate n Bits ROTR1 ROTR2 ROTNR	RAM ACC D		RAM ACC Y Bus
	Source (R/S)		Destination
Bit Oriented BOR1 BOR2 BONR	RAM ACC D		RAM ACC Y Bus
	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
Rotate and Merge ROTM ROTC	D D D D ACC RAM	I RAM I ACC I I	ACC ACC RAM RAM RAM ACC

Instruction Type	Operand Combinations (Note 1)		
	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)
Rotate and Compare CDAI CDRI CDRA CRAI	D D D RAM	I I ACC I	ACC RAM RAM ACC
	Source (R)	Mask (S)	Destination
Prioritize (Note 3) PRT1 PRT2 PRTNR	RAM ACC D	RAM ACC I O	RAM ACC Y Bus
	Data In	Destination	Polynominal
Cyclic Redundancy Check CRCF CRCR	QLINK	RAM	ACC
No Operation NOOP	—		
	Bits Affected		
Set Reset Status SETST RSTST SVSTR SVSTNR TEST	OVR, N, C, Z LINK Flag1 Flag2 Flag3		
	Source		Destination
Store Status	Status		RAM ACC Y Bus
	Source (R)	Source (S)	Destination
Status Load	D ACC D	ACC I I	Status Status and ACC
	Test Condition (CT)		
Test Status	$(N \oplus OVR) + Z$ $N \oplus OVR$ Z OVR Low C		$Z + \overline{C}$ N LINK Flag1 Flag2 Flag3

Notes:
1. If there is no division between the R/S operand or SOURCE and DESTINATION, the two are a given pair. If a division exists, any combination is possible.
2. RAM cannot be used as source when both ACC and STATUS are designated as a DESTINATION.
3. OPERAND and MASK must be different sources.

Instruction Set (Continued)

$\overline{OE}_Y$ is assumed LOW for all cases, allowing ALU outputs on the Y- or D-bus.

Instructions are individually distinguished by using OP-CODES and 2 assigned quadrant bits. Four quadrants, 0 to 3, have been assigned to each instruction type in order to ease groupings of instructions and addressing modes.

Single Operand Instructions

Each Single Operand Instruction contains four designators:

1. Mode (Byte or Word)
2. Opcode
3. Source
4. Address or Destination

These designators are divided into two basic categories, those which use RAM addresses and those that do not.

The instruction formats shown below are unique for each category. In both cases the desired operation, controlled by the instruction inputs, is performed on the source with the result either placed on the Y-bus or stored in the destination or both. The functions of Extending Sign Bit (D(SE)) and Binary Zero (D(OE)) over 16 bits in the Word Mode are available for cases where 8-bit to 16-bit conversion is necessary. The functions performed using Single Operand instructions update the LSB of the Status Register (OVR, N, C, Z) but do not effect the MSB (FLAG1, FLAG2, FLAG3, LINK). Single Operation instructions are limited when both the ACC and Status Register are the destination, the source cannot be RAM.

Single Operand Field Definitions

	15	14–13	12–9	8–5	4–0
SOR	B/W	Quadrant	Opcode	SRC-Dest	RAM Address

	15	14–13	12–9	8–5	4–0
SONR	B/W	Quadrant	Opcode	SRC	Destination

Single Operand Instruction Set

Instruction[1] (15)	B/W[2] (14)	Quad[3] (13)	Opcode (12–9)	R/S[4] (8–5)	Dest[4]	RAM Address/Destination (4–0)
SOR	0 = B 1 = W	10	1100 MOVE SRC → Dest 1101 COMP $\overline{SRC}$ → Dest 1110 INC SRC + 1 → Dest 1111 NEG $\overline{SRC}$ + 1 → Dest	0000 SORA RAM 0010 SORY RAM 0011 SORS RAM 0100 SOAR ACC 0110 SODR D 0111 SOIR I 1000 SOZR O 1001 SOZER D(OE) 1010 SOSER D(SE) 1011 SORR RAM	ACC Y Bus Status RAM RAM RAM RAM RAM RAM RAM	00000 R00 RAM Reg 00 . . . . 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**Opcode**	**R/S[4]**		**Destination**
SONR	0 = B 1 = W	11	1100 MOVE SRC → Dest 1101 COMP $\overline{SRC}$ → Dest 1110 INC SRC + 1 → Dest 1111 NEG $\overline{SRC}$ + 1 → Dest	0100 SOA ACC 0110 SOD D 0111 SOI I 1000 SOZ O 1001 SOZE D(OE) 1010 SOSE D(SE)		00000 NRY Y Bus 00001 NRA ACC 00100 NRS Status[5] 00101 NRAS ACC, Status[5]

Notes:

1. Instruction mnemonic.
2. B = Byte Mode, W = Word Mode.
3. Quadrant subdivides instuctions into categories.
4. R = Source; S = Source; Dest = Destination.
5. Status is destination,
   Status i ← Yi i = 0 to 3 (byte mode)
   i = 0 to 7 (word mode)

Y Bus and Status

Instruction	Opcode	Description	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SOR SONR	COMP	$\overline{SCR}$ → Dest	1 = W 0 = B	Y → $\overline{SRC}$	NC	NC	NC	NC	0	U	0	U
	INC	SCR + 1 → Dest		Y → SRC + 1	NC	NC	NC	NC	U	U	U	U
	MOVE	SCR → Dest		Y → SRC	NC	NC	NC	NC	0	U	0	U
	NEG	$\overline{SCR}$ + 1 → Dest		Y → SRC + 1	NC	NC	NC	NC	U	U	U	U

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Instruction Set (Continued)

Each Two Operand Instruction is constructed of 5 fields:

1. Mode (Byte or Word)
2. Opcode
3. R Source
4. S Source
5. Address or Destination

These instructions are further divided into those using RAM addresses and those that do not. The first type uses two formats which differ only by quadrant designator.

Functions are performed on the specified R and S sources and results are stored in the specified destination and/or placed on the Y-bus. Arithmetic functions update the least significant nibble of the Status Register (OVR, N, C, Z) while logical functions affect only the N and Z bits. Execution of logical functions clear the OVR and C bits of the Status Register.

Two Operand Field Definitions

	15	14 13	12 9	8 5	4 0
TOR1	B/W	Quadrant	SRC-SRC, Dest	Opcode	RAM Address
TOR2	B/W	Quadrant	SRC-SRC, Dest	Opcode	RAM Address
TONR	B/W	Quadrant	SRC-SRC, Dest	Opcode	Destination

Two Operand Instruction Set

Instruction	B/W	Quad			R[1]	S[1]	Dest[1]	Opcode			RAM Address		
	0 = B	00	0000	TORAA	RAM	ACC	ACC	0000	SUBR	S minus R	00000	R00	RAM Reg 00
	1 = W		0010	TORIA	RAM	I	ACC	0001	SUBRC[2]	S minus R	..	..	....
			0011	TODRA	D	RAM	ACC			with carry	11111	R31	RAM Reg 31
			1000	TORAY	RAM	ACC	Y Bus	0010	SUBS	R minus S			
			1010	TORIY	RAM	I	Y Bus	0011	SUBSC[2]	R minus S			
			1011	TODRY	D	RAM	Y Bus			with carry			
			1100	TORAR	RAM	ACC	RAM	0100	ADD	R plus S			
TOR1			1110	TORIR	RAM	I	RAM	0101	ADDC	R plus S			
			1111	TODRR	D	RAM	RAM			with carry			
								0110	AND	$R \bullet S$			
								0111	NAND	$\overline{R \bullet S}$			
								1000	EXOR	$R \oplus S$			
								1001	NOR	$\overline{R + S}$			
								1010	OR	$R + S$			
								1011	EXNOR	$\overline{R \oplus S}$			
Instruction	**B/W**	**Quad**			**R[1]**	**S[1]**	**Dest[1]**	**Opcode**			**RAM Address**		
	0 = B	10	0001	TODAR	D	ACC	RAM	0000	SUBR	S minus R	00000	R00	RAM Reg 00
	1 = W		0010	TOAIR	ACC	I	RAM	0001	SUBRC[2]	S minus R	..	..	....
			0101	TODIR	D	I	RAM			with carry	11111	R31	RAM Reg 31
								0010	SUBS	R minus S			
								0011	SUBSC[2]	R minus S			
										with carry			
								0100	ADD	R plus S			
TOR2								0101	ADDC	R plus S			
										with carry			
								0110	AND	$R \bullet S$			
								0111	NAND	$\overline{R \bullet S}$			
								1000	EXOR	$R \oplus S$			
								1001	NOR	$\overline{R + S}$			
								1010	OR	$R + S$			
								1011	EXNOR	$\overline{R \oplus S}$			

Notes:

1. R = Source
   S = Source
   Dest = Destination
2. For subtraction the carry is interpreted as $\overline{\text{borrow}}$.

Instruction Set (Continued)

Two Operand Instruction Set

Instruction	B/W	Quad			R[1]	S[1]	Opcode			Destination		
	0 = B	11	0001	TODA	D	ACC	0000	SUBR	S minus R	00000	NRY	Y Bus
	1 = W		0010	TOAI	ACC	I	0001	SUBRC	S minus R with carry	00001	NRA	ACC
			0101	TODI	D	I				00100	NRS	Status[2]
							0010	SUBS	R minus S	00101	NRAS	ACC, Status[2]
TONR							0011	SUBSC	R minus S with carry			
							0100	ADD	R plus S			
							0101	ADDC	R plus S with carry			
							0110	AND	$R \bullet S$			
							0111	NAND	$\overline{R \bullet S}$			
							1000	EXOR	$R \oplus S$			
							1001	NOR	$\overline{R + S}$			
							1010	OR	$R + S$			
							1011	EXNOR	$\overline{R \oplus S}$			

Notes:
1. R = Source
   S = Source
2. Status is destination,
   Status i ← Yi, i = 0 to 3 (byte mode)
   i = 0 to 7 (word mode)
3. For subtraction the carry is inverted.

Y Bus and Status Contents

Instruction	Opcode	Description	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
TOR1 TOR2 TONR	ADD	R plus S	0 = B	$Y \leftarrow R + S$	NC	NC	NC	NC	U	U	U	U
	ADDC	R plus S with carry	1 = W	$Y \leftarrow R + S + QC$	NC	NC	NC	NC	U	U	U	U
	AND	$R \bullet S$		$Y \leftarrow R_i$ AND S_i	NC	NC	NC	NC	0	U	0	U
	EXOR	$R \oplus S$		$Y_i \leftarrow R_i$ EXOR S_i	NC	NC	NC	NC	0	U	0	U
	EXNOR	$\overline{R \oplus S}$		$Y_i \leftarrow R_i$ EXNOR S_i	NC	NC	NC	NC	0	0	0	U
	NAND	$\overline{R \bullet S}$		$Y_i \leftarrow R_i$ NAND S_i	NC	NC	NC	NC	0	U	0	U
	NOR	$\overline{R + S}$		$Y_i \leftarrow R_i$ NOR S_i	NC	NC	NC	NC	0	U	0	U
	OR	$R + S$		$Y_i \leftarrow R_i$ OR S_i	NC	NC	NC	NC	0	U	0	U
	SUBR	S minus R		$Y \leftarrow S + \overline{R} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBRC	S minus R with carry		$Y \leftarrow S + \overline{R} + QC$	NC	NC	NC	NC	U	U	U	U
	SUBS	R minus S		$Y \leftarrow R + \overline{S} + 1$	NC	NC	NC	NC	U	U	U	U
	SUBSC	R minus S with carry		$Y \leftarrow R + \overline{S} + QC$	NC	NC	NC	NC	U	U	U	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Single Bit Shift Instructions

Single Bit Shift Instructions are constructed of four fields:
1. Mode (Byte or Word)
2. Direction (up or down) and shift linkage
3. Source
4. Destination

These instructions are further divided into those using RAM addresses and those that do not. The shift linkage indicator indicates what is to be loaded into the vacant bit.

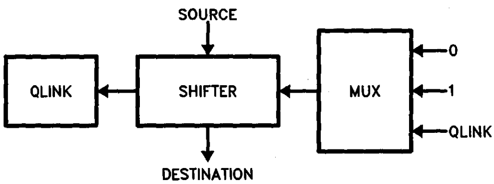
During a shift up the LSB may be loaded with a zero, one or with the link status bit (QLINK), while the MSB is shifted into the QLINK bit. During a shift down, the MSB is loaded with a zero, one, the Status Carry bit (QC), the Exclusive-Or of the Negative-Status bit and the Overflow-Status bit (QN ⊕ QOVR), or the Link-Status bit. The Status Register's N and Z bits are updated, while the OVR and C bits are reset. Shift down with QN ⊕ QOVR can be used in Two's Complement Multiplication.

Single Bit Shift Instructions (Continued)

Single Bit Shift Field Definitions

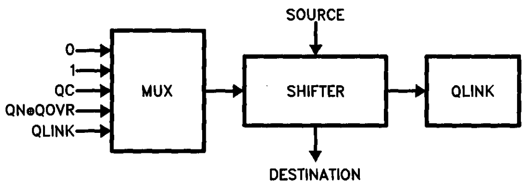
	15	14 — 13	12 — 9	8 — 5	4 — 0
SHFTR	B/W	Quadrant	SRC-Dest	Opcode	RAM Address
SHFTNR	B/W	Quadrant	Source	Opcode	Destination

Shift Up Function



0085-8

Shift Down Function



0085-9

Single Bit Shift Instruction Set

Instruction	B/W	Quad	U[1]	Dest[1]	Opcode	RAM Address/Destination
SHFTR	0 = B 1 = W	10	0110 SHRR RAM 0111 SHDR D	RAM RAM	0000 SHUPZ Up 0 0001 SHUP1 Up 1 0010 SHUPL Up QLINK 0100 SHDNZ Down 0 0101 SHDN1 Down 1 0110 SHDNL Down QLINK 0111 SHDNC Down QC 1000 SHDNOV Down QN ⊕ QOVR	00000 R00 RAM Reg 00 . . . . 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**U[1]**		**Opcode**	**Destination**
SHFTNR	0 = B 1 = W	11	0110 SHA ACC 0111 SHD D		0000 SHUPZ Up 0 0001 SHUP1 Up 1 0010 SHUPL Up QLINK 0100 SHDNZ Down 0 0101 SHDN1 Down 1 0110 SHDNL Down QLINK 0111 SHDNC Down QC 1000 SHDNOV Down QN ⊕ QOVR	00000 NRY Y-Bus 00001 NRA ACC

Note:
1. U = Source
   Dest = Destination

Y Bus and Status

Instruction	Opcode	Description	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
SHR SHNR	SHUPZ SHUP1 SHUPL	Up 0 Up 1 Up QLINK	1 = W	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 15; $Y_0 \leftarrow$ Shift Input	NC	NC	NC	SRC_{15}*	0	SRC_{14}	0	U
			0 = B	$Y_i \leftarrow SRC_{i-1}$, i = 1 to 7; $Y_0 \leftarrow$ Shift Input; $Y_8 \leftarrow SRC_7$, $Y_i \leftarrow SRC_{i-9}$ for i = 9 to 15	NC	NC	NC	SRC_7*	0	SRC_6	0	U
	SHDNZ SHDN1 SHDNL SHDNC SHCNOV	Down 0 Down 1 Down QLINK Down QC Down QN ⊕ QOVR	1 = W	$Y_i \leftarrow SRC_{i+1}$, i = 0 to14; $Y_{15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U
			0 = B	$Y_i \leftarrow SRC_{i+1}$, i = 0 to 6; $Y_i \leftarrow SRC_{i-7}$, i = 8 to 14; $Y_{7,15} \leftarrow$ Shift Input	NC	NC	NC	SRC_0*	0	Shift Input	0	U

*Shifted output is loaded into the QLINK.
SRC = Source   0 = Reset
U = Update   1 = Set
NC = No Change   i = 0 to 15 when not specified

Instruction Set (Continued)

Bit-Oriented Instructions

Bit-Oriented Instructions are constructed from four fields:

1. Mode (Byte or Word)
2. Operation
3. Source or Destination
4. Bit position operated on (0 = LSB)

These instructions are further divided into those using RAM addresses and those that do not. The specified function operates on the given source and the result is stored in the specified destination and/or on the Y-bus.

Set Bit n: Forces the nth bit to ONE without affecting other bit positions.

Reset Bit n: Forces the nth bit to ZERO without affecting other bit positions.

Test Bit n: Sets the Z status bit to the state of bit n.

$\overline{\textbf{Load } 2^n}$: Loads ZERO in bit position n and sets all other bits.

Load 2^n: Loads ONE in bit position n and clears all other bits.

Increment 2^n: Adds 2^n to the operand.

Decrement 2^n: Subtracts 2^n from the operand.

Load, Set, Reset and Test instructions update N and Z status bits while forcing OVR and C bits to ZERO. Arithmetic operations affect the entire lower nibble of the Status Register (OVR, C, N, and Z).

Bit Oriented Field Definitions

	15	14 13	12 9	8 5	4 0
BOR1	B/W	Quadrant	N	Opcode	RAM Address
BOR2	B/W	Quadrant	N	Opcode	RAM Address
BONR	B/W	Quadrant	N	1100	Opcode

Bit Oriented Instruction Set

Instruction	B/W	Quadrant	n	Opcode	RAM Address
BOR1	0 = B 1 = W	11	0 to 15	1101 SETNR Set RAM, bit n 1110 RSTNR Reset RAM, bit n 1111 TSTNR Test RAM, bit n	00000 R00 RAM Reg 00 . . . . 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quadrant**	**n**	**Opcode**	**RAM Address**
BOR2	0 = B 1 = W	10	0 to 15	1100 LD2NR $2^n \rightarrow$ RAM 1101 LDC2NR $\overline{2^n} \rightarrow$ RAM 1110 A2NR RAM plus $2^n \rightarrow$ RAM 1111 S2NR RAM minus $2^n \rightarrow$ RAM	00000 R00 RAM Reg 00 . . . . 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quadrant**	**n**	**Opcode**	**Opcode**
BONR	0 = B 1 = W	11	0 to 15	1100	00000 TSTNA Test ACC, bit n 00001 RSTNA Reset ACC, bit n 00010 SETNA Set ACC, bit n 00100 A2NA ACC plus $2^n \rightarrow$ ACC 00101 S2NA ACC minus $2^n \rightarrow$ ACC 00110 LD2NA $2^n \rightarrow$ ACC 00111 LDC2NA $\overline{2^n} \rightarrow$ ACC 10000 TSTND Test D, bit n 10001 RSTND Reset D, bit n 10010 SETND Set D, bit n 10100 A2NDY D plus $2^n \rightarrow$ Y Bus 10101 S2NDY D minus $2^n \rightarrow$ Y Bus 10110 LS2NY $2^n \rightarrow$ Y Bus 10111 LDC2NY $\overline{2^n} \rightarrow$ Y Bus

Instruction Set (Continued)

Rotate By n Bits Instructions

The Rotate by n Bits Instructions contain four indicators: byte or word mode, source, destination and the number of places the source is to be rotated. They are further subdivided into two types. The first type uses RAM as a source and/or a destination and the second type does not use RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in the table. Under the control of instruction inputs, the n indicator specifies the number of bit positions the source is to be rotated up (0 to 15), and the result is either stored in the specified destination or placed on the Y bus or both. An example of this instruction is given in Figure 5. In the Word mode, all 16-bits are rotated up; while in the Byte mode, only the lower 8-bits (0–7) are rotated up. In the Word Mode, a rotate up by n bits is equivalent to a rotate down by (16-n) bits. Similarly, in the Byte mode a rotate up by n bits is equivalent to a rotate down by (8-n) bits. The N and Z bits of the Status Register are affected and OVR and C bits are forced to ZERO.

Rotate By n Bits Field Definitions

	15	14 13	12 9	8 5	4 0
ROTR1	B/W	Quadrant	n	SRC-Dest	RAM Address
ROTR2	B/W	Quadrant	n	SRC-Dest	RAM Address
ROTNR	B/W	Quadrant	n	1100	SRC-Dest

Rotate by n Example

EXAMPLE: n = 4, Word Mode

Source	0001	0011	0111	1111
Destination	0011	0111	1111	0001

EXAMPLE: n = 4, Byte Mode

Source	0001	0011	0111	1111
Destination	0001	0011	1111	0111

Rotate By n Bits Instruction Set

Instruction	B/W	Quadrant	n			U[1]	Dest[1]	RAM Address		
ROTR1	0 = B 1 = W	00	0 to 15	1100 1110 1111	RTRA RTRY RTRR	RAM RAM RAM	ACC Y Bus RAM	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quadrant**	**n**			**U[1]**	**Dest[1]**	**RAM Address**		
ROTR2	0 = B 1 = W	01	0 to 15	0000 0001	RTAR RTDR	ACC D	RAM RAM	00000 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quadrant**	**n**						**U[1]**	**Dest[1]**
ROTNR	0 = B 1 = W	11	0 to 15	1100				11000 11001 11100 11101	RTDY RTDA RTAY RTAA	D Y Bus D ACC ACC Y Bus ACC ACC

Note:
1. U = Source
Dest = Destination

Y Bus and Status

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTR1 ROTR2 ROTNR		1 = W	$Y_i \leftarrow SRC_{(i-n)mod16}$	NC	NC	NC	NC	0	SRC_{15-n}	0	U
		0 = B	$Y_i \leftarrow SRC_{i+8} = SRC_{(i-n)mod8}$ for i = 0 to 7	NC	NC	NC	NC	0	SRC_{6-n}	0	U

SRC = Source
U = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Instruction Set (Continued)

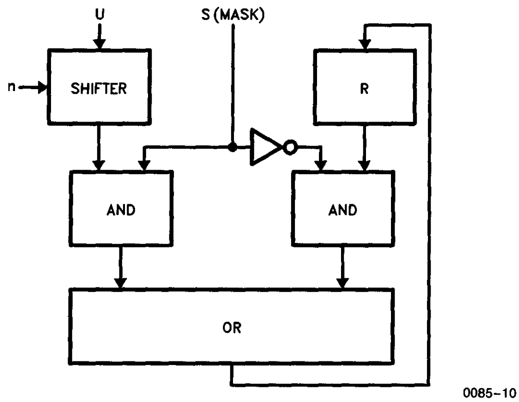
Rotate and Merge Instructions

Each Rotate and Merge instruction consists of five fields:

1. Mode (Byte or Word)
2. Rotated Source (U)
3. Non-Rotated Source (R)
4. Mask Location (S)
5. Number of bits Rotated (n)

The shift register rotates source U up n places. ANDing with the mask causes any bit i to be passed from the rotated source that corresponds to a set bit in mask position i. The R input is not shifted, but is masked by the compliment of mask S, so that a ZERO in mask bit i will pass bit i of R. The ORed result is stored in register R. Rotate and Merge operations update the N and Z status bits, while clearing the OVR and C bits.

Rotate and Merge Function



Rotate and Merge Field Definitions

	15	14–13	12–9	8–5	4–0
ROTM	B/W	Quadrant	n	U,R,S	RAM Address

EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	1010	1010	1010	1010
Mask (S)	0000	1111	0000	1111
Destination	1010	0101	1010	0011

Rotate and Merge Instruction Set

Instruction	B/W	Quadrant	n			U[1]	R/Dest[1]	S[1]	RAM Address		
ROTM	0 = B 1 = W	01	0 to 15	0111	MDAI	D	ACC	I	00000	R00	RAM Reg 00
				1000	MDAR	D	ACC	RAM	. .	. .	. . . .
				1001	MDRI	D	RAM	I	11111	R31	RAM Reg 31
				1010	MDRA	D	RAM	ACC			
				1100	MARI	ACC	RAM	I			
				1110	MRAI	RAM	ACC	I			

Note:
1. U = Rotated Source
   R/Dest = Non-Rotated Source/Destination
   S = Mask

Y Bus and Status

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTM		1 = W	$Y_i \leftarrow (\text{Non Rot Op})_i * \overline{(\text{mask})}_i + (\text{Rot Op})_{(i-n)\bmod 16} * (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i * \overline{(\text{mask})}_i + (\text{Rot Op})_{(i-n)\bmod 8} * (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set

Instruction Set (Continued)

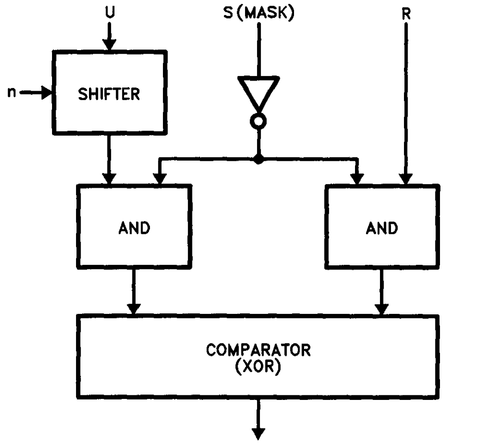
Rotate and Compare Instructions

The five fields of the Rotate and Compare instructions are:

1. Mode (Byte or Word)
2. Rotated Source (U)
3. Non-Rotated Source (R)
4. Mask (S)
5. Number of bits Rotated (n)

Input U is rotated n bits, ANDed with the inversion of S and compared with the input R ANDed with the inversion of S. Thus, a zero in the mask S will allow that bit of both inputs to be compared. The Z bit of the Status Register is set if the comparison passes, and reset if it does not. OVR and C bits are reset in the Status Register.

Rotate and Compare Function



0085–11

Rotate and Compare Field Definitions

	15 14	13 12	9 8	5 4	0
ROTC	B/W	Quadrant	n	U,R,S	RAM Address

EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	0001	0101	1111	0000
Mask (S)	0001	0101	1111	1111
Z (Status) = 1				

Rotate and Compare Instruction Set

Instruction	B/W	Quad	n			U[1]	R[1]	S[1]	RAM Address		
ROTC	0 = B 1 = W	01	0 to 15	0010 0011 0100 0101	CDAI CDRI CDRA CRAI	D D D RAM	ACC RAM RAM ACC	I I ACC I	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31

Note:
1. U = Rotated Source
   R = Non-Rotated Source
   S = Mask

Y Bus and Status

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
ROTC		1 = W	$Y_i \leftarrow (\text{Non Rot Op})_i * \overline{(\text{mask})}_i \oplus (\text{Rot Op})_{(i-n) \bmod 16} * (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U
		0 = B	$Y_i \leftarrow (\text{Non Rot Op})_i * \overline{(\text{mask})}_i \oplus (\text{Rot Op})_{(i-n) \bmod 8} * (\text{mask})_i$	NC	NC	NC	NC	0	U	0	U

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Instruction Set (Continued)

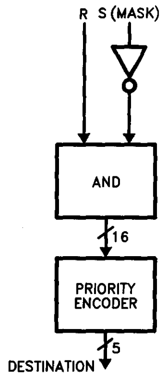
Prioritize Instruction

The four fields of the Prioritize instruction are:

1. Mode (Byte or Word)
2. Mask Source (S)
3. Operand Source (R)
4. Destination

The inverted mask, S is ANDed with R. A "one" in S prohibits that bit from participating in the priority encoding. From the 16-bit input, the priority encoder outputs a 5-bit binary weighted code indicating the bit-position of the highest priority active bit. If there are no active bits, the output is zero. See Figure for operation in both word and byte mode. Using Prioritize updates the N and Z bits of the Status Register, and forces C and OVR to zero. This instruction is limited in that the operand and the mask must be different sources.

Prioritize Function



0085-12

Prioritize Instruction Field Definitions

15	14 13	12 9	8 5	4 0
B/W	Quad	Destination	Source (R)	RAM Address/ Mask (S)
B/W	Quad	Mask (S)	Destination	RAM Address/ Source (R)
B/W	Quad	Mask (S)	Source (R)	RAM Address/ Destination
B/W	Quad	Mask (S)	Source (R)	Destination

Word Mode: Highest Priority Bit Active	Word Mode: Encoder Output	Byte Mode: Highest Priority Bit Active	Byte Mode: Encoder Output
None	0	None	0
15	1	7	1
14	2	6	2
*	*	*	*
*	*	*	*
1	15	1	7
0	16	0	8

*Bits 8 through 15 not available.

Prioritize Instruction

Instruction	B/W	Quad	Destination	Source (R)	RAM Address/Mask (S)
PRT1	0 = B 1 = W	10	1000 PRIA ACC 1010 PR1Y Y Bus 1011 PR1R RAM	0111 RPT1A ACC 1001 PR1D D	00000 R00 RAM Reg 00 . . . . 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**	**Destination**	**RAM Address/Source (R)**
PRT2	0 = B 1 = W	10	1000 PRA ACC 1010 PRZ O 1011 PRI I	0000 PR2A ACC 0010 PR2Y Y Bus	00000 R00 RAM Reg 00 . . . . 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**	**Source (R)**	**RAM Address/Destination**
PRT3	0 = B 1 = W	10	1000 PRA ACC 1010 PRZ O 1011 PRI I	0011 PR3R RAM 0100 PR3A ACC 0110 PR3D D	00000 R00 RAM Reg 00 . . . . 11111 R31 RAM Reg 31
Instruction	**B/W**	**Quad**	**Mask (S)**	**Source (R)**	**Destination**
PRTNR	0 = B 1 = W	11	1000 PRA ACC 1010 PRZ O 1011 PRI I	0100 PRTA ACC 0110 PRTD D	00000 NRY Y Bus 00001 NRA ACC

Instruction Set (Continued)

Y Bus and Status—Prioritize Instruction

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
PRT1 PRT2		1 = W	$Y_i \leftarrow$ CODE ($SCR_n * \overline{mask_n}$); $Y_m \leftarrow$ 0; i = 0 to 4 and n = 0 to 15 m = 5 to 15	NC	NC	NC	NC	0	U	0	U
PRT3 PRTNR		0 = B	$Y_i \leftarrow$ CODE ($SCR_n * \overline{mask_n}$); $Y_m \leftarrow$ 0; i = 0 to 3 and n = 0 to 7 m = 4 to 15	NC	NC	NC	NC	0	U	0	U

*QLINK is loaded with the shifted out bit from the checksum register.

SRC = Source　　0 = Reset
U = Update　　1 = Set
NC = No Change　　i = 0 to 15 when not specified

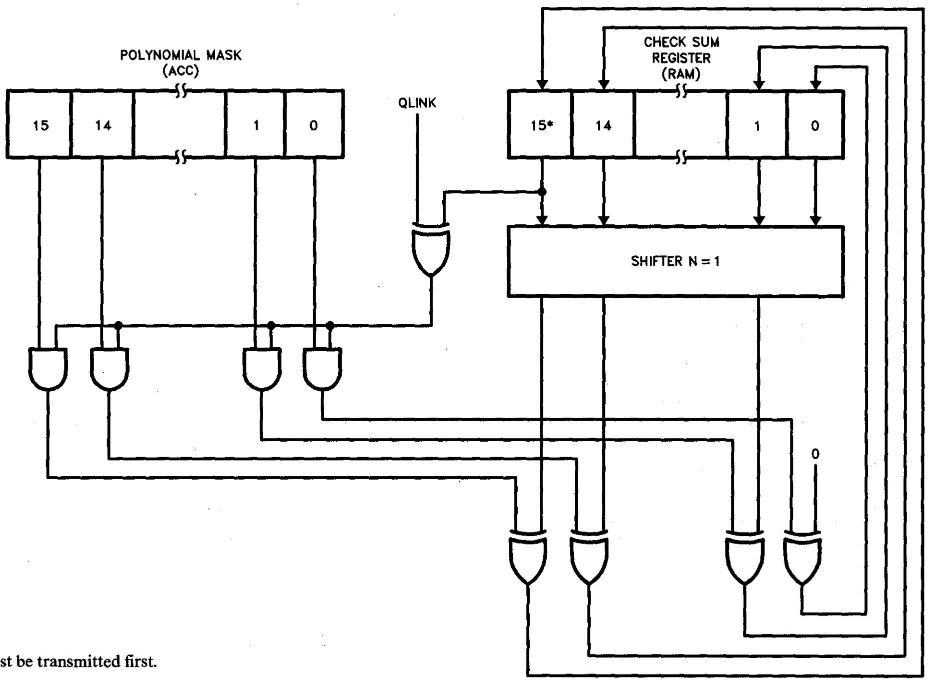
CRC Instruction

The single designator for this instruction is the address of the RAM location that is used as the check sum register. Two CRC instructions, CRC Forward and CRC Reverse, are available. These instructions give the procedure for determining the check bits in a CRC calculation. Since the CRC standards do not specify which data bit is transmitted first, the MSB or the LSB, both Forward and Reverse options are available to the user. The process for generating the check bits for the CRC Forward and Reverse operations are illustrated in the figures below. The ACC is used as a polynomial mask while the RAM contains the partial sum and eventually the final check sum. The serial input comes from the QLINK bit of the Status Register. Status Register bits OVR and C are forced to zero while LINK, N and Z bits are updated.

Cyclic-Redundancy-Check Definitions

	15	14 13	12 9	8 5	4 0
CRCF	1	Quadrant	0110	0011	RAM Address
CRCR	1	Quadrant	0110	1001	RAM Address

CRC Forward Function

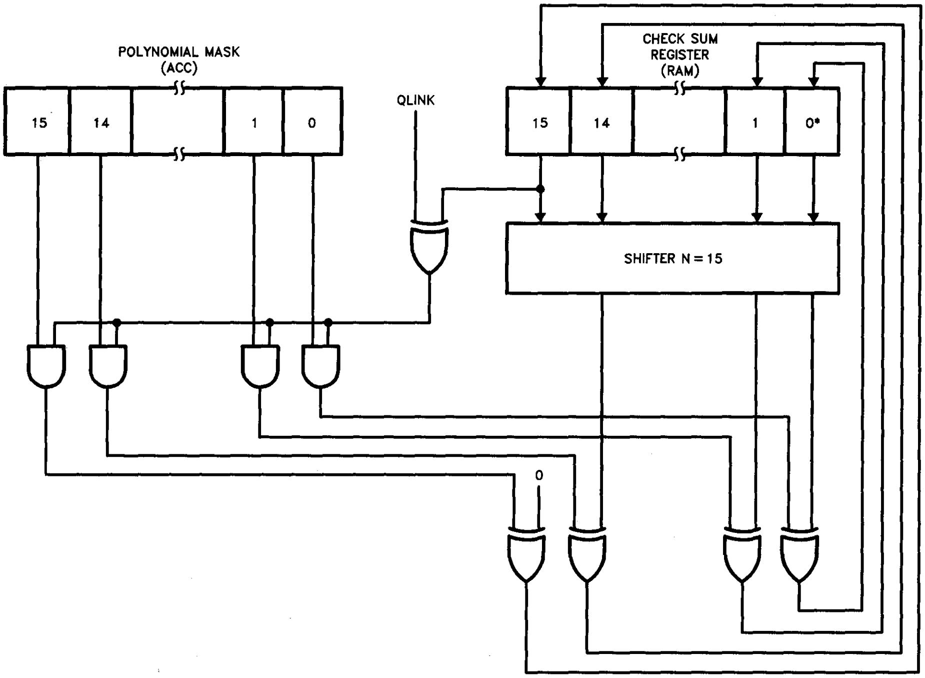


*This bit must be transmitted first.

0085–1?

Instruction Set (Continued)

CRC Reverse Function



0085-14

*This bit must be transmitted first.

Cyclic Redundancy Check Instruction Set

Instruction	B/W	Quad			RAM Address		
CRCF	1	10	0110	0011	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quad**			**RAM Address**		
CRCR	1	10	0110	1001	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31

Y Bus and Status

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
CRCF		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_{15}) * ACC_i]$ $\oplus RAM_{i-1}$ for $i = 15$ to 1 $Y_0 \leftarrow [(QLINK \oplus RAM_{15}) * ACC_0] \oplus 0$	NC	NC	NC	RAM_{15}*	0	U	0	U
CRCR		1 = W	$Y_i \leftarrow [(QLINK \oplus RAM_0) * ACC_i]$ $\oplus RAM_{i+1}$ for $i = 14$ to 0 $Y_{15} \leftarrow [(QLINK \oplus RAM_0) * ACC_{15}] \oplus 0$	NC	NC	NC	RAM_0*	0	U	0	U

*QLINK is loaded with the shifted out bit from the checksum register.

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

6

Instruction Set (Continued)

Status Instructions

7	6	5	4	3	2	1	0
Flag3	Flag2	Flag1	Link	OVR	N	C	Z

Set Status: Specifies which bits in the Status Register are to be set.

Reset Status: Specifies which bits in the Status Register are to be cleared.

Store Status: Indicates byte or word and the destination into which the processor status is saved. The register is always stored in the low byte of the destination. The high byte is unchanged for RAM storage and is loaded with zeroes for ACC storage.

Load Status: Imbedded in the Single- and Two-Operand Instructions.

Test Status: Instructions specify which of the 12 possible test conditions are to be placed on the conditional test output. In addition to the 8 status bits, four logical functions may be selected: N ⊕ OVR, (N ⊕ OVR) + Z, Z + $\overline{C}$, and LOW. These functions are useful in testing two's complement and unsigned number arithmetic operations.

The status register may also be tested via the T bus as shown below. The instruction lines I_1 thru I_4 have bus priority for testing the status register on the CT output.

T_4 I_4	T_3 I_3	T_2 I_2	T_1 I_1	CT
0	0	0	0	(N ⊕ OVR) + Z
0	0	0	1	N ⊕ OVR
0	0	1	0	Z
0	0	1	1	OVR
0	1	0	0	LOW
0	1	0	1	C
0	1	1	0	Z + $\overline{C}$
0	1	1	1	N
1	0	0	0	LINK
1	0	0	1	Flag1
1	0	1	0	Flag2
1	0	1	1	Flag3

Status

	15	14–13	12–9	8–5	4–0
SETST	0	Quad	1011	1010	Opcode
RSTST	0	Quad	1010	1010	Opcode
SVSTR	B/W	Quad	0111	1010	RAM Address/ Dest
SVSTNR	B/W	Quad	0111	1010	Destination

Status Instruction Set

Instruction	B/W	Quad			Opcode		
SETST	0	11	1011	1010	00011 00101 00110 01001 01010	SONCZ SL SF1 SF2 SF3	Set OVR, N, C, Z Set LINK Set Flag1 Set Flag2 Set Flag3
Instruction	**B/W**	**Quad**			**Opcode**		
RSTST	0	11	1010	1010	00011 00101 00110 01001 01010	RONCZ RL RF1 RF2 RF3	Reset OVR, N, C, Z Reset LINK Reset Flag1 Reset Flag2 Reset Flag3
Instruction	**B/W**	**Quad**			**RAM Address/Destination**		
SVSTR	0 = B 1 = W	10	0111	1010	00000 . . 11111	R00 . . R31	RAM Reg 00 . . . . RAM Reg 31
Instruction	**B/W**	**Quad**			**Destination**		
SVSTNR	0 = B 1 = W	11	0111	1010	00000 00001	NRY NRA	Y Bus ACC
Instruction	**B/W**	**Quad**			**Opcode (CT)**		
Test	0	11	1001	1010	00000 00010 00100 00110 01000 01010 01100 01110 10000 10010 10100 10110	TNOZ TNO TZ TOVR TLOW TC TZC TN TL TF1 TF2 TF3	Test (N⊕OVR) + Z Test N⊕OVR Test Z Test OVR Test LOW Test C Test Z + $\overline{C}$ Test N Test LINK Test Flag1 Test Flag2 Test Flag3

Note: $\overline{IEN}$ * test status instruction has priority over T_{1-4} instruction.

Instruction Set (Continued)

Y Bus and Status

Instruction	Opcode	Description	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
RSTST	RONCZ	Reset OVR, N, C, Z	0 = B	$Y_i \leftarrow$ 0 for i = 0 to 15	NC	NC	NC	NC	0	0	0	0
	RL	Reset LINK			NC	NC	NC	0	NC	NC	NC	NC
	RF1	Reset Flag1			NC	NC	0	NC	NC	NC	NC	NC
	RF2	Reset Flag2			NC	0	NC	NC	NC	NC	NC	NC
	RF3	Reset Flag3			0	NC	NC	NC	NC	NC	NC	NC
SETST	SONCZ	Set OVR, N, C, Z	0 = B	$Y_i \leftarrow$ 1 for i = 0 to 15	NC	NC	NC	NC	1	1	1	1
	SL	Set LINK			NC	NC	NC	1	NC	NC	NC	NC
	SF1	Set Flag1			NC	NC	1	NC	NC	NC	NC	NC
	SF2	Set Flag2			NC	1	NC	NC	NC	NC	NC	NC
	SF3	Set Flag3			1	NC	NC	NC	NC	NC	NC	NC
SVSTR SVSTNR		Save Status*	0 = B 1 = W	$Y_i \leftarrow$ Status for $i \leftarrow$ 0 to 7; $Y_i \leftarrow$ 0 for i = 8 to 15	NC	NC	NC	NC	NC	NC	NC	NC
Test	TNOZ	Test (N⊕OVR) + Z	0 = B	**	NC	NC	NC	NC	NC	NC	NC	NC
	TNO	Test (N⊕OVR)			NC	NC	NC	NC	NC	NC	NC	NC
	TZ	Test Z			NC	NC	NC	NC	NC	NC	NC	NC
	TOVR	Test OVR			NC	NC	NC	NC	NC	NC	NC	NC
	TLOW	Test LOW			NC	NC	NC	NC	NC	NC	NC	NC
	TC	Test C			NC	NC	NC	NC	NC	NC	NC	NC
	TZC	Test Z + $\overline{C}$			NC	NC	NC	NC	NC	NC	NC	NC
	TN	Test N			NC	NC	NC	NC	NC	NC	NC	NC
	TL	Test LINK			NC	NC	NC	NC	NC	NC	NC	NC
	TF1	Test Flag1			NC	NC	NC	NC	NC	NC	NC	NC
	TF2	Test Flag2			NC	NC	NC	NC	NC	NC	NC	NC
	TF3	Test Flag3			NC	NC	NC	NC	NC	NC	NC	NC

U = Update
NC = No Change
) = Reset
l = Set
. = 0 to 15 when not specified

*In byte mode only the lower byte from the Y bus is loaded into the RAM or ACC and in word mode all 16-bits from the Y bus are loaded into the RAM or ACC.
**Y-Bus is Undefined.

No-Op Instruction

The No-Op Instruction does not affect any internal registers; the Status Register, RAM register and AC register are left unchanged. The 16-bit opcode is fixed.

No Operation Field Definition

	15	14 13	12 9	8 5	4 0
No-Op	0	11	1000	1010	00000

No-Op Instruction

Instruction	B/W	Quad			
No-Op	0	11	1000	1010	0000

Y Bus and Status

Instruction	Opcode	B/W	Y-Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	Z
No-Op		0 = B	*	NC	NC	NC	NC	NC	NC	NC	NC

Y-Bus is undefined.
RC = Source
J = Update
JC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

Electrical Characteristics Over Commercial and Military Operating Range V_{CC} Min. = 4.5V, V_{CC} Max. = 5.5V

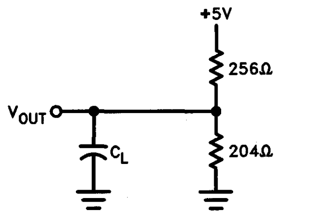
Parameters	Description		Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage		V_{CC} = Min. I_{OH} = −1.6 mA	2.4		V
V_{OL}	Output LOW Voltage		V_{CC} = Min. I_{OL} = 16 mA		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IX}	Input Leakage Current		$V_{SS} \leq V_{IN} \leq V_{CC}$ V_{CC} = Max.	−10	+10	μA
I_{OZ}	Output Leakage Current		V_{CC} = Max. $V_{OUT} = V_{SS}$ to V_{CC}		+10	μA
				−10		μA
I_{SC}	Output Short Circuit Current[1]		V_{CC} = Max. V_{OUT} = 0V		−85	mA
$I_{CC}(Q1)$[2]	Supply Current (Quiescent)	Commercial	$V_{SS} \leq V_{IN} \leq V_{IL}$ or $V_{IH} \leq V_{IN} \leq V_{CC}$; $\overline{OE}_Y$ = HIGH		126	mA
		Military			145	
$I_{CC}(Q2)$	Supply Current (Static)	Commercial	$V_{IN} = V_{CC}$ or GND V_{CC} = Max. I_{OPER} = 0 μA		68	mA
		Military			78	mA
$I_{CC}(Max.)$[2]	Supply Current	Commercial	V_{CC} = Max., f_{CLK} = 10 MHz $\overline{OE}_Y$ = HIGH		145	mA
		Military			166	

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	5	pF
C_{OUT}	Output Capacitance		7	

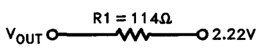
Notes:
1. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.
2. To calculate I_{CC} at any given frequency, use $I_{CC}(Q_1) + I_{CC}(A.C.)$ where $I_{CC}(Q_1)$ is shown above and $I_{CC}(A.C.)$ = 1.9 mA/MHz × Clock Frequency for the Commercial temperature range. $I_{CC}(A.C.)$ = 2.1 mA/MHz × Clock Frequency for Military temperature range.
3. Tested on a sample basis.

Output Loads Used for AC Performance Characteristics



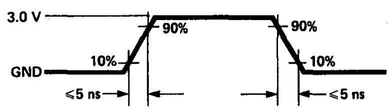
0085-15

All Outputs



0085-16

All Input Pulses



0085-17

Notes:
1. C_L = 50 pF includes scope probe, wiring and stray capacitance.
2. C_L = 5 pF for output disable tests.

Commercial Switching Characteristics

Guaranteed Commercial Range A.C. Performance Characteristics

(T_A = 0°C to +70°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF)

Combinational Propagation Delays (ns)

To Output / From Input	Y_{0-15}			T_{1-4}			CT		
CY7C9116 CY7C9117	35	45	65	35	45	65	35	45	65
I_{0-4} (ADDR)	35	45	65	35	52	73			
I_{0-15} (DATA)	35	45	65	35	52	73			
I_{0-15} (INST)	35	45	65	35	52	73	20	29	30
DLE*	20	32	55	30	32	55			
T_{1-4}							15	25	27
CP	30	32	60	30	32	66	25	25	37
Y_{0-15}	20	32	53	30	32	53			
$\overline{IEN}$							15	25	25

*DLE is guaranteed by other tests.

Enable/Disable Times (ns) (C_L = 5 pF, Disable Only)

From Input	To Output	Enable						Disable					
		T_{PZH}			T_{PZL}			T_{PHZ}			T_{PLZ}		
		35	45	65	35	45	65	35	45	65	35	45	65
$\overline{OE}_Y$	Y_0-Y_{15}	18	20	22	18	20	22	18	20	22	18	20	22
OE_T	T_1-T_4	15	20	22	15	20	22	15	20	22	15	20	22

Clock and Pulse Requirements (ns)

Input	Minimum Low Time			Minimum High Time		
	35	45	65	35	45	65
CP	15	15	20	15	15	15
DLE				15	15	15
$\overline{IEN}$	15	15	20			

Set-up and Hold Times (ns)

[5]	Input	With Respect To	High to Low Transition						Low to High Transition						Comments
			Set-up			Hold			Set-up			Hold			
CY7C9116 and CY7C9117			35	45	65	35	45	65	35	45	65	35	45	65	
1	I_{0-4} (RAM Addr)	CP	12	13	13	0	0	0							Single Addr (Source)
2	I_{0-4} (RAM Addr)	CP & $\overline{\text{IEN}}$	5	5	5	← Do Not Change →						0	2	0	Two Addr (Destination)
3	I_{0-15} (Data)	CP							40	43	60	0	0	0	
4	I_{0-4} (RAM Addr)[2]	$\overline{\text{IEN}}$	15[1]	18[1]	24[1]	4[1]	5[1]	10[1]							Two Addr (Immediate)
5	I_{0-15} (Instr)[3]	CP	15[1]	18[1]	24[1]	4[1]	5[1]	10[1]	40	43	60	0	0	0	
6	$\overline{\text{IEN}}$[2]	CP										8	8	8	Two Addr (Immediate)
7	$\overline{\text{IEN}}$ HIGH	CP	5	5	5							0	1	2	Disable
8	$\overline{\text{IEN}}$ LOW	CP							10	10	10	0	1	1	Enable
9	$\overline{\text{IEN}}$ LOW	CP	5	5	5	1	1	0							Note 1
10	$\overline{\text{SRE}}$	CP							12	12	12	0	2	0	
11	Y[4]	CP							32	32	42	0	0	0	
12	Y[4]	DLE	6	6	6	5	5	5							
13	DLE	CP							20	25	43	0	0	0	

Notes:
1. Timing for immediate instruction for first cycle.
2. CY7C9117 only.
3. CY7C9115 and CY7C9116 only.
4. Y = D for CY7C9117.
5. t_{SX} and t_{HK} referenced on the waveforms are looked up on this table by x = line number on the left. Ex: t_{SI} = 13 ns for −53 ns devices.

Military Switching Characteristics

Guaranteed Military Range A.C. Performance Characteristics

(T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50 pF)

Combinational Propagation Delays (ns)

To Output / From Input	Y_{0-15}			T_{1-4}			CT		
CY7C9116 CY7C9117	40	65	79	40	65	79	40	65	79
I_{0-4} (ADDR)	40	65	79	40	65	79			
I_{0-15} (DATA)	40	65	79	40	65	79			
I_{0-15} (INST)	40	65	79	40	65	79	22	26	29
DLE*	20	52	62	30	52	62			
T_{1-4}							15	26	29
CP	30	57	67	35	65	75	33	33	39
Y_{0-15}	20	52	60	30	52	60			
$\overline{\text{IEN}}$							20	26	29

*DLE is guaranteed by other tests.

Military Switching Characteristics (Continued)

Enable/Disable Times (ns) (C_L = 5 pF, Disable Only)

From Input	To Output	Enable						Disable					
		T_{PZH}			T_{PZL}			T_{PHZ}			T_{PLZ}		
		40	65	79	40	65	79	40	65	79	40	65	79
$\overline{OE}_Y$	Y_0–Y_{15}	18	22	25	18	22	25	18	18	25	18	18	25
$\overline{OE}_T$	T_1–T_4	18	18	20	18	18	20	15	15	20	15	15	20

Clock and Pulse Requirements (ns)

Input	Minimum Low Time			Minimum High Time		
	40	65	79	40	65	79
CP	15	20	25	15	15	15
DLE				15	15	15
$\overline{IEN}$	15	15	15			

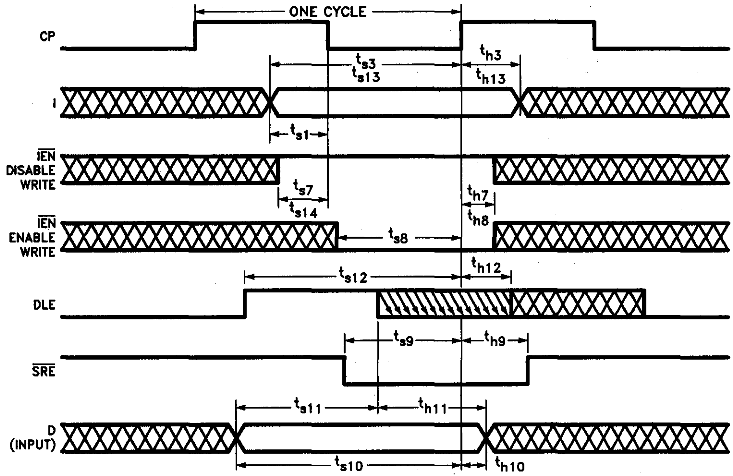
Set-up and Hold Times (ns)

[5]	Input	With Respect To	High to Low Transition						Low to High Transition						Comments
			Set-up			Hold			Set-up			Hold			
CY7C9116 and CY7C9117			40	65	79	40	65	79	40	65	79	40	65	79	
1	I_{0-4} (RAM Addr)	CP	12	12	12	0	1	1							Single Addr (Source)
2	I_{0-4} (RAM Addr)	CP & $\overline{IEN}$	5	7	7	← Do Not Change →						0	0	0	Two Addr (Destination)
3	I_{0-15} (Data)	CP							43	56	65	0	0	0	
4	I_{0-4} (RAM Addr)[2]	$\overline{IEN}$	15[1]	25	27[1]	5[1]	12	12[1]							Two Addr (Immediate)
5	I_{0-15} (Instr)[3]	CP	15[1]	25	27[1]	5[1]	12	12[1]	45	56	65	0	2	2	
6	$\overline{IEN}$[2]	CP										8	8	8	Two Addr (Immediate)
7	$\overline{IEN}$ HIGH	CP	5	5	5							0	2	2	Disable
8	$\overline{IEN}$ LOW	CP							10	10	12	0	3	3	Enable
9	$\overline{IEN}$ LOW	CP	7	7	7	0	3	3							Note 1
10	$\overline{SRE}$	CP							10	10	12	0	1	1	
11	Y[4]	CP							39	45	53	0	0	0	
12	Y[4]	DLE	7	7	7	3	3	3							
13	DLE	CP							20	46	54	0	0	0	

Notes:
1. Timing for immediate instruction for first cycle.
2. CY7C9117 only.
3. CY7C9115 and CY7C9116 only.
4. Y = D for CY7C9117.
5. t_{SX} and t_{HX} referenced on the waveforms are looked up on this table by x = line number on the left. Ex: t_{SI} = 24 ns for — 79 ns devices.

Switching Waveforms

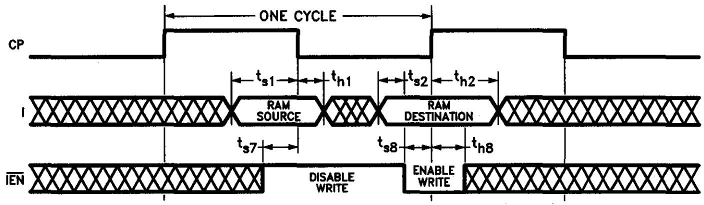
Single Address Access Timing



If t_{h11} is satisfied, t_{h10} need not be satisfied

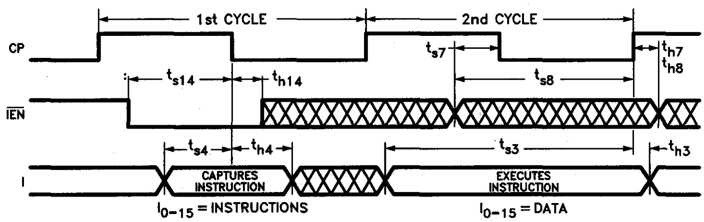
0085–18

Double Address Access Timing



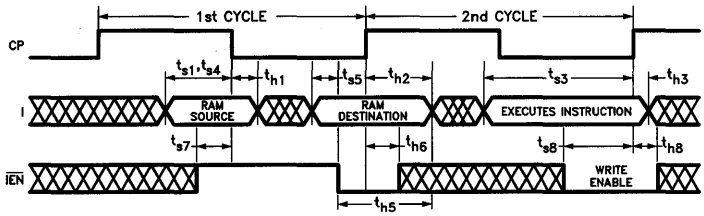
0085–19

One-Address Immediate Instruction Cycle Timing



0085–20

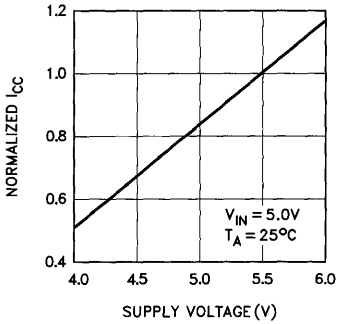
Two-Address Immediate Instruction Timing (7C9117 Only)



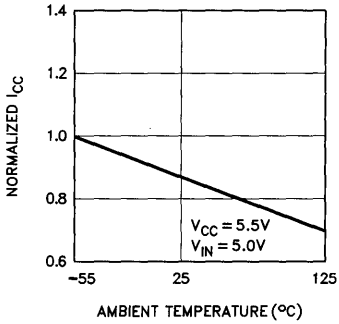
0085–21

Typical DC and AC Characteristics

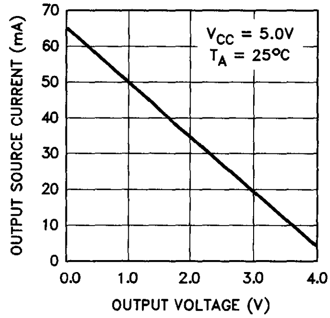
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



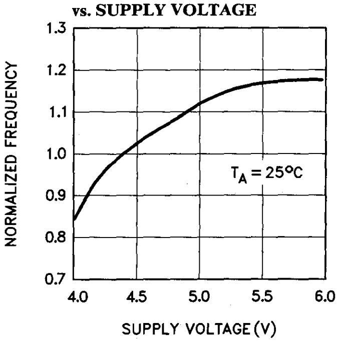
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



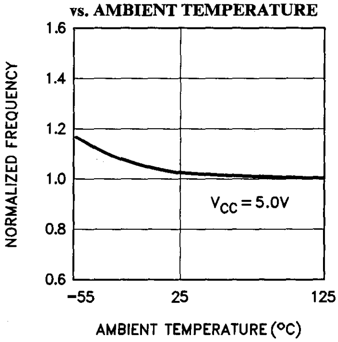
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



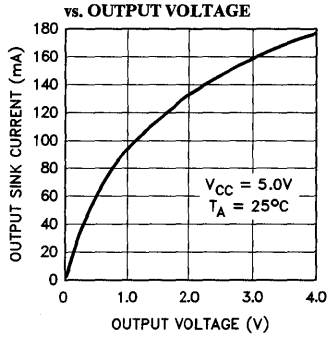
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



NORMALIZED FREQUENCY vs. AMBIENT TEMPERATURE

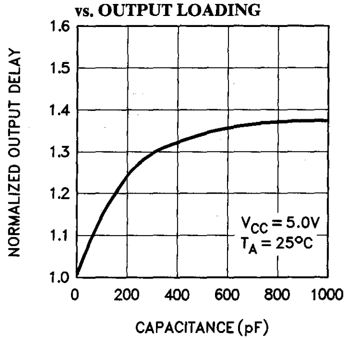


OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

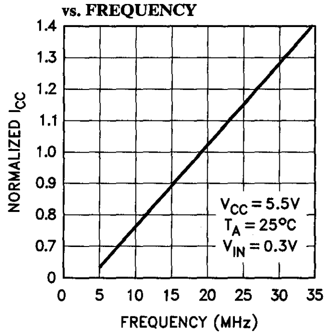


6

NORMALIZED OUTPUT DELAY vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. FREQUENCY



0085–23

Set-up and Hold Times (Cross Ref. Table)

[1]	High to Low Transition		Low to High Transition	
	Set-up	Hold	Set-up	Hold
1	t_{S1}	t_{h1}		
2	t_{S2}			t_{h2}
3			t_{S3}	t_{h3}
4	t_{S5}	t_{h5}		
5	t_{S4}	t_{h4}	t_{S13}	t_{h13}
6				t_{h6}
7	t_{S7}			t_{h7}
8			t_{S8}	t_{h8}
9	t_{S14}	t_{h14}		
10			t_{S9}	t_{h9}
11			t_{S10}	t_{h10}
12	t_{S11}	t_{h11}		
13			t_{S12}	t_{h12}

Note:
1. Refer to Set-up and Hold times shown on pages 22 & 23.

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C9115-35JC	J69	Commercial
45	CY7C9115-45JC	J69	
65	CY7C9115-65JC	J69	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C9116-35LC	L69	Commercial
	CY7C9116-35JC	J81	
	CY7C9116-35DC	D28	
45	CY7C9116-45LC	L69	
	CY7C9116-45JC	J81	
	CY7C9116-45DC	D28	
65	CY7C9116-65LC	L69	
	CY7C9116-65JC	J81	
	CY7C9116-65DC	D28	
40	CY7C9116-40LMB	L69	Military
	CY7C9116-40DMB	D28	
65	CY7C9116-65LMB	L69	
	CY7C9116-65DMB	D28	
79	CY7C9116-79LMB	L69	
	CY7C9116-79DMB	D28	

Speed (ns)	Ordering Code	Package Type	Operating Range
35	CY7C9117-35GC	G68	Commercial
	CY7C9117-35JC	J81	
	CY7C9117-35LC	L81	
45	CY7C9117-45GC	G68	
	CY7C9117-45JC	J81	
	CY7C9117-45LC	L81	
65	CY7C9117-65GC	G68	
	CY7C9117-65JC	J81	
	CY7C9117-65LC	L81	
40	CY7C9117-40GMB	G68	Military
	CY7C9117-40LMB	L81	
65	CY7C9117-65GMB	G68	
	CY7C9117-65LMB	L81	
79	CY7C9117-79GMB	G68	
	CY7C9117-79LMB	L81	

Military Specifications
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1,2,3
V_{OL}	1,2,3
V_{IH}	1,2,3
V_{IL} Max.	1,2,3
I_{IX}	1,2,3
I_{OZ}	1,2,3
I_{SC}	1,2,3
I_{CC}(Q1)	1,2,3
I_{CC}(Max)	1,2,3

Switching Characteristics

Parameters	Subgroups
I_{0-4}(Addr)	7,8,9,10,11
I_{0-15}(Data)	7,8,9,10,11
I_{0-15}(Instr)	7,8,9,10,11
DLE	7,8,9,10,11
t_{1-4}	7,8,9,10,11
CP	7,8,9,10,11
Y_{0-15}	7,8,9,10,11
$\overline{IEN}$	7,8,9,10,11
$\overline{OE}_Y$	7,8,9,10,11
OE_T	7,8,9,10,11
CP	7,8,9,10,11

Document #: 38-00057-C

Section Contents

RISC

CYPRESS SEMICONDUCTOR

Introduction to RISC

Introduction

This section provides an overview of the basic concepts and advantages of RISC computer architectures in general and a brief summary of the specific features of the RISC computer implemented in Cypress's CY7C600 family.

Scalable Processor Architecture

The Cypress CY7C600 family implements a RISC architecture called SPARC™. SPARC stands for Scalable Processor ARChitecture. It is applicable to large high-performance machines as well as small machines. The term "scalable" refers to the size of the smallest lines on a chip. As lines become smaller, chips get faster. However, some chip designs do not shrink well (they do not scale properly) because the architecture is too complicated. Because of its simplicity, the CY7C600 scales well. Consequently, CY7C600 systems will become faster as better semiconductor techniques are perfected. SPARC is an open computer architecture. We believe that the intelligent and aggressive nature of the SPARC design will make it an industry standard. The design specification is published, and other vendors are also producing SPARC microprocessors.

What is RISC?

RISC, an acronym for Reduced Instruction Set Computer, is a style of computer architecture emphasizing simplicity and efficiency. RISC designs begin with a necessary and sufficient instruction set. Typically, a few simple operations account for almost all computations. RISC machines are about two to five times faster than machines with traditional complex instruction set architectures. Also, RISC machine's simpler designs are easier to implement, resulting in shorter design cycles.

RISC architectures are a response to the evolution from assembly language to high-level languages. Assembly language programs occasionally employ elaborate machine instructions, whereas high-level language compilers rarely do. For example, most C compilers use only about 30% of the available instructions on CISC machines. Studies show that approximately 80% of a typical program's computations require only about 20% of a processor's instruction set.

RISC is to hardware what the UNIX® operating system is to software. The UNIX system proves that operating systems can be both simple and useful. Hardware studies lead to the same conclusion. As advances in semiconductor technology reduce the cost of processing and memory, overly complex instruction sets become a performance liability. The designers of RISC machines strive for hardware simplicity, with close cooperation between machine architecture and compiler design. At each step, computer architects must ask: to what extent does a feature improve or degrade performance and is it worth the cost of implementation? Each additional feature, no matter how useful it is in an isolated instance, makes all other perform more slowly by its mere presence.

The goal of RISC architecture is to maximize the effective speed of a design by performing infrequent functions in software, including hardware-only features that yield a net performance gain. Performance gains are measured by conducting detailed studies of large high-level language programs. RISC improves performance by providing the building blocks from which high-level functions can be synthesized without the overhead of general but complex instructions.

RISC Architecture

The following characteristics are typical of RISC architectures, including the CY7C600 design:

- **Single-cycle execution.** Most instructions are executed in a single machine cycle.
- **Hardwired control with no microcode.** Microcode add a level of complexity and raises the number of cycles per instruction.
- **Load/store, register-to-register design.** All computational instructions involve registers. Memory accesses are made with only load and store instructions.
- **Simple fixed-format instructions with few addressing modes.** All instructions are one word long (typically 32 bits) and have few addressing modes.
- **Pipelining.** The instruction set design allows for the processing of several instructions at the same time.
- **High-performance memory.** RISC machines have at least 32 general-purpose registers (the 7C600 has 136) and large cache memories.
- **Migration of functions to software.** Only those features that measurably improve performance are implemented in hardware. Programs contain sequences of simple instructions for executing complex functions rather than the complex instructions themselves.
- **Simple, efficient instruction pipeline visible to compilers.** For example, branches take effect after execution of the following instruction, permitting a fetch of the next instruction during execution of the current instruction.

The real keys to enhanced performance are single-cycle execution and keeping the cycle time as short as possible. Many characteristics of RISC architectures, such as load/store and register-to-register design, facilitate single-cycle execution. Simple fixed-format instructions, in the other hand, permit shorter cycles by reducing decoding time.

Note that some of these features, particularly pipelining and high-performance memories, have been used in super-computer designs for many years. The difference is that in RISC architectures these ideas are integrated into a processor with a simple instruction set and no microcode.

Moving functionality from run time to compile time also enhances performance. Functions calculated at compile time do not require further calculating each time the program runs. Furthermore, optimizing compilers can rearrange pipelined instruction sequences and arrange register-to-register operations to reuse computational results.

A new set of simplified design criteria has emerged:

- Instructions should be simple unless there is a good reason for complexity. To be worthwhile, a new instruction that increases cycle time by 10% must reduce the total number of cycles executed by at least 10%..
- Microcode is generally no faster than sequences of hardwired instructions. Moving software into microcode does not make it better, it just makes it harder to modify.
- Fixed-format instructions and pipelined execution are more important than program size. As memory gets cheaper and faster, the space/time tradeoff resolves in favor of time. Reducing space no longer decreases time.
- Compiler technology should use simple instructions to generate more complex instructions. Instead of substituting a complicated microcoded instruction for several simple instructions, which compilers did in the 1970s, optimizing compilers can form sequences of simple, fast instructions out of complex high-level code. Operands can be kept in registers to increase speed even further.

RISC's Speed Advantage

Using any given benchmark, the performance (P) of a particular computer is inversely proportional to the product of the benchmark's instruction count (I), the average number of clock cycles per instruction (C), and the inverse of the clock speed (S). Assuming that a RISC machine runs at the same clock speed as a corresponding traditional machine, S is identical. The number of clock cycles per instruction (C), is around 1.3 to 1.7 for RISC machines, and between 4 and 10 for traditional machines. This makes the instruction execution rate of RISC machines about 3 to 6 times faster than traditional machines. But because traditional machines have more powerful instructions, RISC machines must execute more instructions for the same program, typically about 10% to 30% more. Since RISC machines execute 10% to 30% more instructions 3 to 6 times faster, they are about 2 to 5 times faster than traditional machines for executing typical large programs.

$$P = \frac{1}{I \times C \times \frac{1}{S}}$$

Compiled programs on RISC machines are somewhat larger than compiled programs on traditional machines because several simple instructions replace one complex instruction resulting in decreased code density. All SPARC instructions are 32 bits wide, whereas some instructions on traditional machines are narrower. But the number of instructions actually executed may not be as great as the increased program size would indicate. A windowed register file, for example, often simplifies call/return sequences so that context switches become less expensive.

CY7C600 Architecture

The SPARC CPU is composed of a CY7C601 Integer Unit (IU) that performs basic processing, and a CY7C602 Floating-Point Unit (FPU) that performs floating-point calculations. The CY7C602 is a SPARC-compatible floating-point unit. CY7C600-based computers typically have a Memory Management Unit (MMU), a large virtual-address cache for instructions and data, and are organized around a 32-bit data and instruction bus.

The integer and floating-point units operate concurrently. The FPU performs floating-point calculations with a set number of floating-arithmetic units. The CY7C600 architecture also specifies an interface for the connection of an additional coprocessor.

Instruction Categories

The CY7C600 architecture has about 50 integer instructions. CY7C600 instructions fall into seven basic categories:

- **Load and store instructions** (the only way to access memory). These instructions use two registers or a register and a constant to calculate the memory address involved. Half-word accesses must be aligned on 2-byte boundaries, word accesses on 4-byte boundaries, and double-word accesses on 8-byte boundaries. These alignment restrictions greatly speed up memory access.
- **Arithmetic/logical/shift instructions.** These instructions compute a result that is a function of two source operands and then place the result in a register. They perform arithmetic, logical, or shift operations.
- **Floating-point and coprocessor instructions.** These include floating-point calculations, operations on floating-point registers, and instructions involving the optional coprocessor. Floating-point operations execute concurrently with IU instructions and with other floating-point operations when necessary. This concurrency is transparent to the programmer.
- **Control transfer instructions.** These include jumps, calls, traps, and branches. Control transfers are usually delayed until after execution of the next instruction so that the pipeline is not emptied every time a control transfer occurs. Thus compilers can be optimized for delayed branching.
- **Read/write control register instructions.** These include instructions to read and write the contents of various control registers. Generally the source or destination is implied by the instructions.
- **Artificial intelligence instructions.** These include the tagged arithmetic instructions Tagged Add and Tagged Subtract. Tagged instructions are useful for implementing artificial intelligence languages such as LISP, because tags can automatically indicate to software interpreters the data type of arithmetic operands.
- **Multiprocessing instructions.** These include two instructions for implementing semaphores in memory: Atomic Load/Store Unsigned Byte, which loads a byte from memory and then sets the location to all 1s, and SWAP, which exchanges the contents of a register and memory location. Both of these instructions are "atomic" or ininterruptible.

Register Windows

A unique feature contributing to the high performance of the CY7C600 design is its overlapping register windows. Results left in registers by a calling routine automatically become available operands for the called routine, reducing the need for load and store instructions to main memory.

According to the architectural specification, there may be anywhere between 2 and 32 register windows, each window having 24 working registers, plus 8 global registers. The first implementation has 8 register windows with 24 registers each (but count only 16 since 8 overlap), plus 8 global registers, for a total of 136 registers. Recent research suggests that register windows and tagged arithmetic, found in CY7C600 systems, but not in other commercial RISC machines, are sufficient to provide excellent performance for expert system development requiring AI languages such as LISP and Smalltalk.

Traps and Interrupts

The CY7C600 design supports a full set of traps and interrupts. They are handled by a table that supports 128 hardware and 128 software traps. Even though floating-point instructions can execute concurrently with integer instructions, floating-point traps are precise because the FPU supplies (from the table) the address of the instructions that failed.

Protection

Some CY7C600 instructions are privileged and can only be executed while the processor is in supervisor mode. This instruction execution protection ensures that user programs cannot accidentally alter the state of the machine with respect to its peripherals.

The CY7C600 design also provides memory protection, which is essential for smooth multitasking operation. Memory protection makes it impossible for user programs to corrupt the system, other user programs, or themselves.

Open Architecture

Advantages of Open Architecture

The CY7C600 design is the first open RISC architecture, and one of the few open CPU architectures. Standard products are more beneficial than proprietary ones because standards allow users to acquire that most cost-effective hardware and software in a competitive multivendor marketplace. Integrated circuits come from several competing semiconductor vendors, while software is supplied by systems vendors. This advantage is lost when users are limited by a processor with proprietary hardware and software.

RISC architectures, and the CY7C600 design in particular, are easy to implement because they are relatively simple. Since they have short design cycles, RISC machines can absorb new technologies almost immediately, unlike more complicated computer architectures.

CY7C600 systems were designed to support:

- The C programming language and the UNIX operating system
- Numerical applications (using FORTRAN)
- Artificial intelligence and expert system applications using AI languages such as LISP and Prolog

Supporting C is relatively easy; most modern hardware architectures are able to do so. The one essential feature is byte addressability. However, numerical applications require fast floating-point operations and artificial intelligence applications require large address spaces and interchangeability of data types.

The floating-point processor, with pipelined floating-point operation capabilities, achieves the high performance needed for numerical applications.

For artificial intelligence and expert system applications, CY7C600 systems offer tagged instructions and word alignment. Because languages such as LISP and Prolog are often interpreted, word alignment makes it easier for interpreters to manipulate and interchange integers and different types of pointers. In the tagged instructions, the two low-order bits of an operand specify the type of operand. If an operand is an integer, most of the time it is added to (or subtracted from) a register. If an operand is a pointer, most of the time a memory reference is involved. Language interpreters can leave operands in the appropriate registers, greatly improving the performance of exploratory programming environments.

The CY7C600 architecture does not dictate a memory management unit (MMU), although a high-performance unit has been specified for the SPARC architecture. The same processor will be used in different types of machines. For example, a single-user machine with embedded applications does not need an MMU. By contrast, a multitasking machine used for timesharing, such as a traditional UNIX workstation, needs a paging MMU. Furthermore, a multiprocessor such as a vector machine or hypercube requires specialized memory management facilities. The CY7C600 architecture can be implemented with a different MMU configuration for each of these purposes, without affecting user software.

CY7C600 Machines and Other RISC Machines

The CY7C600 design has more similarities to Berkeley's RISC-II architecture than to any other RISC architecture. Like the RISC-II architecture, it uses register windows in order to reduce the number of load/store instructions. The CY7C600 architecture allows 32 register windows, but the initial implementation has 8 windows. The tagged instructions are derived from SOAR, the "Smalltalk On A RISC" processor developed at Berkeley after implementing RISC-II.

CY7C600 systems are designed for optimal floating-point performance and support single-, double-, and extended-precision operands and operations, as specified by the ANIS/IEEE 754 floating-point standard. High floating-point performance results from concurrency of the IU and FPU. The integer unit loads and stores floating-point operands, while the floating-point unit performs calculations. If an error (such as a floating-point exception) occurs, the floating-point unit specifies precisely where the trap took place; execution is expediently resumed at the discretion of the integer unit. Furthermore, the floating-point unit has an internal instruction queue; it can operate while the integer unit is processing unrelated functions.

CY7C600 systems deliver very high levels of performance. The flexibility of the architecture makes future systems capable of delivering performance many times greater than the performance of the initial implementation. Moreover, the openness of the architecture makes it possible to absorb technological advances almost as soon as they occur.

CY7C600 Product Family

Since the CY7C600 has been designed to offer a complete solution fo the implementation of high-performance computers and controllers, the family consists of several members including an Integer Unit, a Floating-Point Controller, a Floating-Point Processor, a Cache Controller and Memory Management Unit, and a Cache Data RAM.

The SPARC processor family consists of a CY7C601 Integer Unit to perform all non-floating-point operations and a CY7C608 Floating-Point Controller (FPC), which interfaces to a CY7C609 Floating-Point Processor to perform floating-point arithmetic concurrent with the IU. Support is also provided for a second generic coprocessor interface. The IU communicates with external memory via a 32-bit address bus and a 32-bit data/instruction bus. In typical data-processing applications, the IU and FPU are combined with a high-performance CY7C604 Cache Controller and Memory Management Unit and a cache memory implemented with CY7C157 Cache RAMs. In many dedicated controller applications the IU can function by itself with high-speed local memory only.

CY7C601 Integer Unit

The IU is the basic processing engine that executes all of the instruction set except for floating-point operations. The CY7C601 IU contains a large 136 x 32 triple-port register file, which is divided into 8 windows. Each window contains 24 working registers and has access to the same 8 global registers. A current window pointer (CWP) filed in the Processor State Register keeps track of which window is currently active. The CWP is decremented when the processor calls a subroutine and is incremented when the processor returns.

The registers in each window are divided into ins, outs, and locals, Each window shares its ins and outs with adjacent windows. The outs of the previous window are the ins of the current window, and the outs of the current window are the ins of the next window. The globals are equally available to all windows and the locals are unique to each window. The windows are joined together in a circular stack where the outs of the last window are the ins of the first window.

The IU supports a multitasking operating system by providing user and supervisor modes. Some instructions are privileged and can only be executed while the processor is in supervisor mode. Changing from user to supervisor mode requires taking a hardware interrupt or executing a trap instruction.

The IU supports both asynchronous traps (interrupts) and synchronous traps (error conditions and trap instructions). Traps transfer control to an offset within a table. The base address of the table is specified by a Trap Base Register and the offset is a function of the trap type. Traps are taken before the current instruction causes any changes visible to the programmer and can therefore be considered to occur between instructions.

CY7C602 Floating-Point Unit

The CY7C602 FPU provides high-performance, IEEE STD-754-1985-compatible single- and double-precision floating-point calculations for 7C600 systems and is designed to operate concurrently with the CY7C601. All address and control signals for memory accesses by the CY7C602 are supplied by the CY7C601. Floating-point instructions are addressed by the CY7C601, and are simultaneously latched from the data bus by both the CY7C601 and CY7C602. Floating-point instructions are concurrently decoded by the CY7C601 and the CY7C602, but do not begin execution in the CY7C602 until after the instruction is enabled by a signal from the CY7C601. Pending and currently executing FP instructions are placed in an on-chip queue while the IU continues to execute non-floating-point instructions.

The CY7C602 has a 32 x 32-bit data register file for floating-point operations. The contents of these registers are transferred to and from external memory under control of the CY7C601 using floating-point load/store instructions. Addresses and control signals for data accesses during a floating-point load or store are supplied by the CY7C601, while the CY7C602 supplies or receives data. Although the CY7C602 operates concurrently with the CY7C601, a program containing floating-point computations generates results as if the instructions were being executed sequentially.

CY7C604 Cache Controller and Memory Management Unit

The CY7C604 Cache Controller and Memory Management Unit (CMU) provides hardware support for a demand-paged virtual memory environment for the CY7C601 processor. The CY7C604 conforms to the standard SPARC architecture definition for memory management. Page size is fixed at 4 kilobytes. The CMU translates 32-bit virtual addresses from the processor into 36-bit physical addresses and provides both write-through and buffered copy-back cache policies. The on-chip context register allows support of up to 4096 contexts.

High-speed address look-up is provided by an on-chip translation lookaside buffer (TLB). Each entry contains the virtual to physical mapping of a 4-kbyte page. If a virtual address match is detected in one of the TLB entries, the physical address translation contained in that entry will be delivered to the outputs of the CMU. If the virtual address from the processor has no corresponding entry in the CMU, the CMU will automatically perform address translation for the virtual address using on-chip hardware to access a main memory resident three-level page table. Each "matched" TLB entry is checked for protection violation automatically and violations are reported to the Integer Unit as memory exceptions.

The CMU also provides storage for 2048 cache address tags for a 64-kbyte cache with a 32-byte line size. The tag entries can be directly written or read by the processor. In normal operation, eleven low-order bits, 15–5, of the virtual address from the processor are used to select one of the tag entries in the CY7C604 and its 16-bit contents are compared on chip with the 16 high-order processor address bits to determine if the cache contains the required data or instruction. This cache hit/miss comparison is then qualified by various built-in protection checks and the result is output. Pipelined accesses are supported via on-chip registers that capture both address and data from the processor.

The CY7C604 also contains the logic required in a system to implement the byte and half-word write capabilities provided in the SPARC instruction set. Cache tag update is also simplified by an automatic page update on miss feature, which eliminates the need for processor accesses during tag update.

CY7C605 Cache Controller and Memory Management Unit for Multiprocessor Systems

The CY7C605 Cache Controller and Memory Management Unit is an extension of the CY7C604 for use in multiprocessor systems. The CY7C605 provides the same SPARC reference MMU as the CY7C604, but adds an enhanced cache controller that incorporates bus snooping and cache coherency protocol required to maintain a multiprocessor cache. The CY7C605 provides a dual-cache tag memory, which allows the CY7C605 to perform bus snooping while it simultaneously supports cache accesses by the CY7C601. The CY7C605 cache coherency protocol is based on the IEEE Futurebus, which has been recognized as a superior protocol for maintaining cache consistency without degrading processor performance.

The CY7C605 supports direct data intervention, which is the capability of a CY7C605-based cache to directly supply modified data to another requesting cache without first requiring main memory in order to supply modified data to another cache. In addition to direct data intervention, the CY7C605 also supports memory reflection. Memory reflection allows a memory system to automatically update itself during a direct data intervention operation. This feature allows a multiprocessing system to update both a requesting cache and main memory in a single bus operation. The CY7C605 is designed to be pin-compatible with the CY7C604. This feature allows a system to be upgraded from uniprocessor to multiprocessor by modifying the operating system and replacing the CY7C604 with the CY7C605.

CY7C157 Cache Data RAM

The CY7C157 16K x 16 static RAMs are designed to interface easily to and provide maximum performance for the CY7C600 processor. The RAM has registered address inputs and latched data inputs and outputs as well as a self-timed write pulse that greatly simplifies the design of cache memories for the CY7C601 Integer Unit. The device has a single clock that controls loading of the address register, data input latches, data output latches, pipeline control latch, and chip enable register. The chip enable is clocked into a register and pipelined through a control register to condition the output enable. This pipelined design allows a cache that works as an extension of the internal instruction pipeline of the CY7C601 Integer Unit, thereby maximizing performance. The write enable is edge-activated and self-timed, thereby eliminating the need for the user to generate accurate write pulses in external logic. A separate asynchronous output enable is provided to disable outputs during a write or to allow other devices access to the bus.

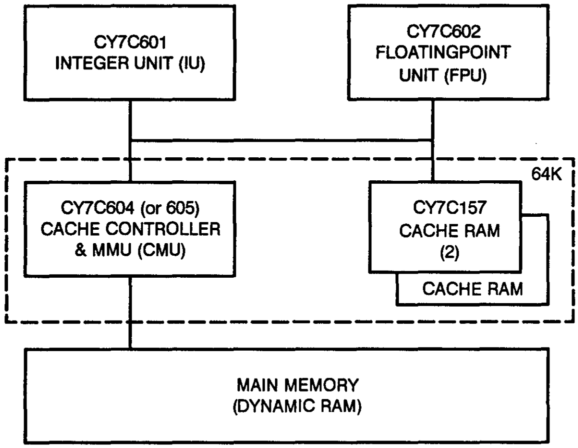


Figure 1. Full System Block Diagram

32-Bit RISC Processor

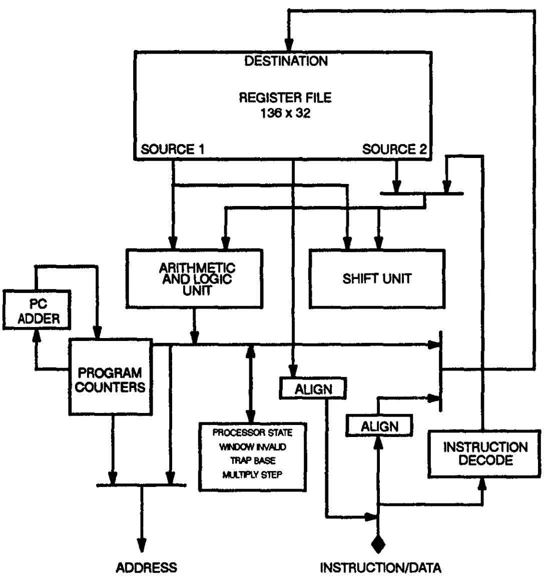
Features

- **Reduced Instruction Set Computer (RISC) Architecture**
  - **Simple format instructions**
  - **Most instructions execute in a single cycle**
- **Very high performance**
  - **25-, 33-, and 40-MHz clock speeds yield 18, 24, and 29 MIPS sustained throughput respectively**
  - **Very fast interrupt response**
  - **Four-stage pipeline**
- **Large windowed register file**
  - **136 general-purpose 32-bit registers**
  - **Registers can be used as eight windows of 24 registers each for low procedure overhead**
  - **Registers can also be used as register banks for fast context switching**
- **Multiprocessing support**
- **Large virtual address space**
  - **32-bit virtual address bus**
  - **8-bit address space identifier bus**
- **Hardware pipeline interlocks**
- **Multitasking support**
  - **User/supervisor modes**
  - **Privileged instructions**
- **Artificial intelligence support**
- **High-performance coprocessor interface for user-defined coprocessor**
- **FPU interface allows concurrent execution of floating-point instructions**
- **0.8-micron CMOS technology**
- **207 pin grid array package or 208 quad flat package**

Overview

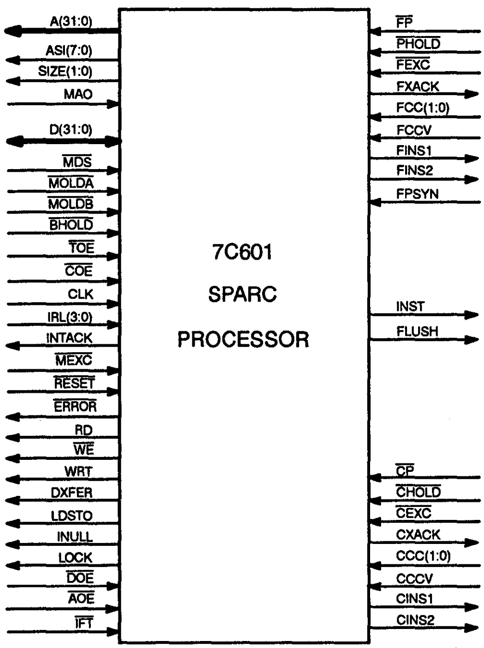
The CY7C601 integer unit is a high-speed CMOS implementation of the SPARC 32-bit RISC processor. The RISC architecture makes possible the creation of a processor that can execute instructions at a rate of one instruction per processor clock. The CY7C601 supports a tightly coupled floating-point interface and coprocessor interface that allows concurrent execution of floating-point, coprocessor, and integer instructions.

Logic Block Diagram



C601-1

Pin Configuration



C601-2

Selection Guide

		7C601-40	7C601-33	7C601-25
Maximum Operating Current (mA)	Commercial	650	600	600
	Military			600

Overview (continued)

The CY7C601 SPARC processor provides the following features:

Simple instruction format. All instructions are 32-bits wide and aligned on 32-bit boundaries in memory. The three basic instruction formats feature uniform placement of opcode and address fields.

Register intensive architecture. Most instructions operate on either two registers or one register and a constant, and place the result in a third register. Only load and store instructions access off-chip memory.

Large windowed register file. The processor has 136 on-chip 32-bit registers configured as eight overlapping sets of 24 registers each and eight global registers. This scheme allows compilers to cache local values across subroutine calls and provides a register based parameter passing mechanism.

Delayed control transfer. The processor always fetches the next instruction after a control transfer, and either executes it or annuls it depending on the state of a bit in the control transfer instruction. This feature allows compilers to rearrange code to place a useful instruction after a delayed control transfer and thereby take better advantage of the processor pipeline.

Concurrent floating-point. Floating-point instructions can execute concurrently with each other and with non-floating-point instructions.

Fast interrupt response. Interrupt inputs are sampled on every clock cycle and can be acknowledged in one to three cycles. The first instruction of an interrupt service routine can be executed within 6 to 8 cycles of receiving the interrupt request.

The 7C600 Family

The SPARC processor family consists of a CY7C601 integer unit to perform all non-floating-point operations and a CY7C602 Floating-Point Unit (FPU) to perform floating-point arithmetic concurrent with the CY7C601. Support is also provided for a second generic coprocessor interface. The CY7C601 communicates with external memory via a 32-bit address bus and a 32-bit data/instruction bus. In typical data processing applications, the CY7C601 and CY7C602 are combined with a high-performance CY7C604 memory management unit and cache controller and a cache memory implemented with CY7C157 16-kbyte x 16 cache RAMS. In many dedicated controller applications the CY7C601 can function by itself with only high speed local memory.

Coprocessor Interface

The CY7C601 is the basic processing engine which executes all of the instruction set except for floating-point operations. The CY7C601 and CY7C602 operate concurrently. The CY7C602 recognizes floating-point instructions and places them in a queue while the CY7C601 continues to execute non-floating-point instructions. If the CY7C602 encounters an instruction which will not fit in its queue, the CY7C602 holds the CY7C601 until the instruction can be stored. The CY7C602 contains its own set of registers on which it operates. The contents of these registers are transferred to and from external memory under control of the CY7C601 via floating-point load/store instructions. Processor interlock hardware hides floating-point concurrency from the compiler or assembly language programmer. A program containing floating-point computations generates the same results as if instructions were executed sequentially.

Registers

The CY7C601 contains a large 136 x 32 triple-port register file which is divided into 8 windows, each with 24 working registers and each having access to the same 8 global registers. A Current Window Pointer (CWP) field in the processor state register keeps track of which window is currently active. The CWP is decremented when the processor calls a subroutine and is incremented when the processor returns. The registers in each window are divided into ins, outs, and locals. The eight global registers are shared by all windows and appear as registers 0–7 in each window. Registers 8–15 serve as outs, registers 16–23 as locals, and 24–31 serve as ins. Each window shares its ins and outs with adjacent windows. The outs of the previous window are the ins of the current window, and the outs of the current window are the ins of the next window. The globals are equally available to all windows and the locals are unique to each window. The windows are joined together in a circular stack where the outs of window 7 are the ins of window 0.

Multitasking Support

The CY7C601 supports a multitasking operating system by providing user and supervisor modes. Some instructions are privileged and can only be executed while the processor is in supervisor mode. Changing from user to supervisor mode requires taking a hardware interrupt or executing a trap instruction.

Interrupts and Traps

The CY7C601 supports both asynchronous traps (interrupts) and synchronous traps (error conditions and trap instructions). Traps transfer control to an offset within a table. The base address of the table is specified by a trap base register and the offset is a function of the trap type. Traps are taken before the current instruction causes any changes visible to the programmer and can therefore be considered to occur between instructions.

Instruction Set Summary

Instructions fall into five basic categories as follows:

1. Load and store instructions. Load and store are the only instructions which access external memory. They use two CY7C601 registers or one CY7C601 register and a signed immediate value to generate the memory address. The instruction destination field specifies either an CY7C601 register, a CY7C602 register, or a coprocessor register as the destination for a load or source for a store. Integer load and store instructions support 8-, 16-, 32-, and 64-bit transfers while floating-point and coprocessor instructions support 32- and 64-bit accesses.

2. Arithmetic/logical/shift. These instructions compute a result that is a function of two source operands and write the result into a destination register or discard it. They perform arithmetic, tagged arithmetic, logical, and shift operations. An instruction SETHI, useful in creating 32-bit constants in two instructions, writes a 22-bit constant into the high order bits of a register and zeroes the remaining bits. The contents of any register can be shifted left or right any number of bits in one clock cycle as specified by a register or the instruction itself. The tagged instructions are useful in artificial intelligence applications.

3. Control transfer. Control transfer instructions include jumps, calls, traps and branches. Control transfer is usually delayed so that the instruction immediately following the control transfer (called the delay instruction) is executed before control is transferred to the target location. The delay instruction is always fetched, however, a bit in the control transfer instruction can cause the delay instruction to be nullified if the branch is not taken. This flexibility increases the likelihood that a useful instruction can be placed after the control transfer thereby filling an otherwise unused hole in the processors pipeline. Branch and call instructions use program counter relative displacements. A jump and link instruction uses a register indirect displacement computing its target address as either the sum of two registers or the sum of a register and a 13-bit signed immediate value. The branch instruction provides a displacement plus or minus 8 megabytes, and the call instructions 30-bit displacement allows transfer to almost any address.

4. Read/write control registers. The processor provides special instructions to read and write the contents of the various control registers within the machine. These registers include the multiply step register, processor state register, window invalid mask register, and trap base register.

5. Floating-point/coprocessor instructions. These instructions include all floating-point conversion and arithmetic operations as well as future coprocessor instructions. These instructions involve operations only on the contents of the register file internal to the CY7C602 or coprocessor.

The instruction set of the processor is summarized in *Table 1.*

Registers

The following sections provide an overview of the 7C601 registers. The CY7C601 has two types of registers; working registers (r registers), and control registers. The r registers provide storage for processes, and the control registers keep track of and control the state of the CY7C601.

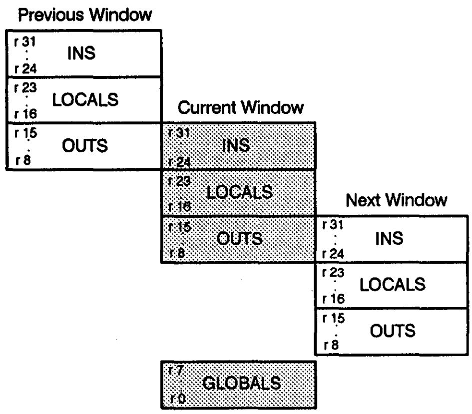


Figure 1. Register Windows

r Registers. The r registers (*Figure 1*) consist of eight 32-bit global registers, and 8 windows, each having twenty-four 32-bit registers. Each two adjacent windows are overlapped in eight registers. This results in a total of 136 32-bit general purpose registers on the chip.

CY7C601 Control Registers. The CY7C601 control registers contain various addresses and pointers used by the system to control its internal state. They include the Program Counters (PC and nPC), the Processor State Register (PSR), the Window Invalid Mask register (WIM), the Trap Base Register (TBR), and the Y register. The following paragraphs briefly describe each:

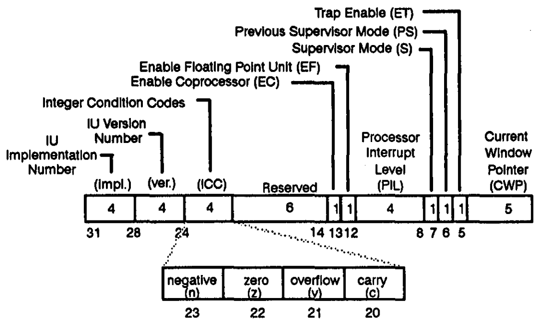


Figure 2. Processor State Register

Processor Status Register (PSR). The processor status register contains fields that describe and control the state of the CY7C601.

IU Implementation and IU Version Numbers (IMPL field, PSR<31:28>; VER field, PSR<27:24>). These are read-only fields in the PSR. The version number and the implementation number are each set to "0001".

Table 1. Instruction Set Summary

	Inputs	Operation		Cycles
Load and Store Instructions	LDSB(LDSBA*)	Load Signed Byte	(from Alternate Space)	2
	LDSH(LDSHA*)	Load Signed Halfword	(from Alternate Space)	2
	LDUB(LDUBA*)	Load Unsigned Byte	(from Alternate Space)	2
	LDUH(LDUHA*)	Load Unsigned Halfword	(from Alternate Space)	2
	LD(LDA*)	Load Word	(from Alternate Space)	2
	LDD(LDDA*)	Load Doubleword	(from Alternate Space)	3
	LDF	Load Floating Point		2
	LDDF	Load Double Floating Point		3
	LDFSR	Load Floating Point State Register		2
	LDC	Load Coprocessor		2
	LDDC	Load Double Coprocessor		3
	LDCSR	Load Coprocessor State Register		2
	STB(STBA*)	Store Byte	(into Alternate Space)	3
	STH(STHA*)	Store Halfword	(into Alternate Space)	3
	ST(STA*)	Store Word	(into Alternate Space)	3
	STD(STDA*)	Store Doubleword	(into Alternate Space)	4
	STF	Store Floating Point		3
	STDF	Store Double Floating Point		4
	STFSR	Store Floating Point State Register		3
	STDFQ*	Store Double Floating Point Queue		4
	STC	Store Coprocessor		3
	STDC	Store Double Coprocessor		4
	STCSR	Store Coprocessor State Register		3
	STDCO*	Store Double Coprocessor Queue		4
	LDSTUB(LDSTUBA*)	Atomic Load/Store Unsigned Byte	(in Alternate Space)	4
	SWAP(SWAPA*)	Swap r Register with Memory	(in Alternate Space)	4
Arithmetic/Logical/Shift	ADD(ADDcc)	Add	(modify icc)	1
	ADDX(ADDXcc)	Add with Carry	(modify icc)	1
	TADDcc(TADDccTV)	Tagged Add and modify icc	(and Trap on overflow)	1
	SUB(SUBcc)	Subtract	(modify icc)	1
	SUBX(SUBXcc)	Subtract with Carry	(modify icc)	1
	TSUBcc(TSUBccTV)	Tagged Subtract and modify icc	(and Trap on overflow)	1
	MULScc	Multiply Step and modify icc		1
	AND(ANDcc)	And	(and modify icc)	1
	ANDN(ANDNcc)	And Not	(and modify icc)	1
	OR(ORcc)	Inclusive Or	(and modify icc)	1
	ORN(ORNcc)	Inclusive Or Not	(and modify icc)	1
	XOR(XORcc)	Exclusive Or	(and modify icc)	1
	XNOR(XNORcc)	Exclusive Nor	(and modify icc)	1
	SLL	Shift Left Logical		1
	SRL	Shift Right Logical		1
	SRA	Shift Right Arithmetic		1
	SETHI	Set High 22 Bits of r Register		1
	SAVE	Save Caller's window		1
	RESTORE	Restore Caller's window		1
Control Transfer	Bicc	Branch on Integer Condition Codes		1**
	FBicc	Branch on Floating Point Condition Codes		1**
	CBccc	Branch on Coprocessor Condition Codes		1**
	CALL	Call		1**
	JMPL	Jump and Link		2**
	RETT	Return from Trap		2**
	Ticc	Trap on Integer Condition Codes		1 (4 if Taken)

7

Table 1. Instruction Set Summary (continued)

	Inputs	Operation	Cycles
Read/Write Control Registers	RDY RDPSR RDWIM RDTBR	Read Y Register Read Processor State Register Read Window Invalid Mask Read Trap Base Register	1 1 1 1
	WRY WRPSR* WRWIM* WRTBR*	Write Y Register Write Processor State Register Write Window Invalid Mask Write Trap Base Register	1 1 1 1
	UNIMP	Unimplemented Instruction	1
	IFLUSH	Instruction Cache Flush	1
FP (CP) Ops	FPop CPop	Floating Point Unit Operations Coprocessor Operations	1 to Launch 1 to Launch

* Privileged instruction.

** Assuming delay slot is filled with useful instruction.

Integer Condition Codes (PSR<23:20>). The integer condition codes consist of four flags: negative, zero, overflow, and carry. These flags are set by the conditions occurring during integer logic and arithmetic operations.

Enable Coprocessor (EC bit, PSR<13>). This bit is used to enable the coprocessor. If a coprocessor operation (CPop) is encountered and the EC bit is cleared (i.e., coprocessor disabled), a coprocessor disabled trap is generated.

Enable Floating Point Unit (EF bit, PSR<12>). This bit is used to enable the floating point unit. If a floating point operation (FPop) is encountered and the EF bit is cleared (i.e., FPU disabled), a floating point disabled trap is generated.

Processor Interrupt Level (PIL field, PSR<11:8>). This four bit field sets the CY7C601 interrupt level. The CY7C601 will only acknowledge interrupts greater than the level indicated by the PIL field. Bit 11 is the MSB; bit 8 is the LSB.

Supervisor Mode (S bit, PSR<7>). S = 1 indicates that the CY7C601 is in supervisor mode. Supervisor mode can only be entered by a software or hardware trap.

Previous Supervisor Mode (PS bit, PSR<6>). This bit indicates the state of the supervisor bit before the most recent trap.

Trap Enable (ET bit, PSR<5>). This bit enables or disables the CY7C611 traps. This bit is automatically set to 0 (traps disabled) upon entering a trap. When ET = 0, all asynchronous traps are ignored. If a synchronous trap occurs when ET = 0, the CY7C601 enters error mode.

Current Window Pointer (CWP field, PSR<4:0>). The r registers are addressed by the Current Window Pointer (CWP), a field of the Processor Status Register (PSR), which points to the 24 active local registers. It is incremented by a RESTORE instruction and decremented by a SAVE instruction. Note that the globals are always accessible regardless of the CWP. In the overlapping configuration each window shares its ins and outs with adjacent windows. The outs from a previous window (CWP + 1) are the ins of the current window, and the outs from the current window are the ins for the next window (CWP -1). In both the windowed and register bank configurations globals are equally available and the locals are unique to each window.

Program Counters (PC and nPC). The Program Counter (PC) holds the address of the instruction being executed, and the next Program Counter (nPC) holds the address of the next instruction to be executed.

Trap Base Register (TBR). The trap base register contains the base address of the trap table and a field that provides a pointer into the trap table.

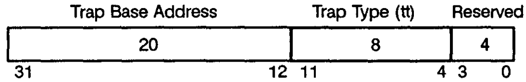


Figure 3. Trap Base Register

Window Invalid Mask Register (WIM). The window invalid mask register determines which windows are valid and which window accesses cause window_overflow and window_underflow traps.

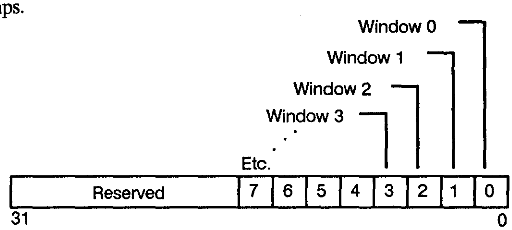


Figure 4. Window Invalid Mask

Y register. The Y register is used to hold the partial product during execution of the multiply-step instruction (MULSCC).

Pin Description

The integer unit's external signals fall into three categories: 1) memory subsystem interface signals, 2) floating-point unit/coprocessor interface signals, and 3) miscellaneous I/O signals. These are described in the following sections. Paragraphs after the tables describe each signal. Signals that are active LOW are marked with an overcomer; all others are active HIGH. For example, $\overline{\text{WE}}$ is active LOW, while RD is active HIGH.

Memory Subsystem Interface Signals

A[31:0]. These 32 bits are the addresses of instructions or data and they are sent out "unlatched" by the integer unit. Assertion of the MAO signal during a cache miss will force the integer unit to put the previous (missed) address on the address bus. A[31:0] pins are tristated if the AOE or TOE signal is deasserted.

ASI[7:0]. These 8 bits are the address space identifier for an instruction or data access to the memory. ASI[7:0] are sent out "unlatched" by the integer unit. The value on these pins during any given cycle is the address space identifier corresponding to the memory address on the A[31:0] pins at that cycle. Assertion of the MAO signal during a cache miss will force the integer unit to put the previous address space identifier on the ASI[7:0] pins. ASI[7:0] pins are tristated if the AOE or TOE signal is deasserted. Normally, the encoding of the ASI bits is as shown in *Table 2*. The remaining codes are software generated.

Table 2. ASI Bit Assignment

Address Space Identifier (ASI)	Address Space
00001000	User Instruction
00001010	User Data
00001001	Supervisor Instruction
00001011	Supervisor Data

D[31:0]. D[31:0] is the bi-directional data bus to and from the integer unit. The data bus is driven by the integer unit during the execution of integer store instructions and the store cycle of atomic load/store instructions. Similarly, the data bus is driven by the floating point unit only during the execution of floating-point store instructions. The store data is sent out unlatched and must be latched externally before it is used. Once latched, store data is valid during the second data cycle of a store single access, the second and third data cycle of a store double access, and the third data cycle of an atomic load store access. The alignment for load and store instructions is done inside the processor. A double word is aligned on an 8-byte boundary, a word is aligned on a 4-byte boundary, and a half word is aligned on a 2-byte boundary. D(31) corresponds to the most significant bit of the least significant byte of the 32-bit word. If a double word, word, or half word load or store instruction generates an improperly aligned address, a memory address not aligned trap will occur. Instructions and operands are always expected to be fetched from a 32-bit wide memory.

SIZE[1:0]. These two bits specify the data size associated with a data or instruction fetch. Size bits are sent out "unlatched" by the integer unit. The value on these pins at any given cycle is the data size corresponding to the memory address on the A[31:0] pins at that cycle. SIZE[1:0] remains valid on the bus during all data cycles of loads, stores, load_doubles, store_doubles and atomic load stores. Since all instructions are 32-bits long, SIZE[1:0] is set to "10" during all instruction fetch cycles. Encoding of the SIZE[1:0] bits is shown in *Table 3*.

Table 3. Size Bit Assignment

Size 1	Size 0	Data Transfer Type
0	0	Byte
0	1	Halfword
1	0	Word
1	1	Word (Load/Store Double)

MHOLDA and MHOLDB. The processor pipeline will be frozen while MHOLDA or MHOLDB is asserted and the CY7C601 outputs will revert to and maintain the value they had at the rising edge of the clock in the cycle before MHOLDA or MHOLDB was asserted. MHOLDA/B is used to freeze the clock to both the integer and floating point units during a cache miss (for systems with cache) or when a slow memory is accessed. This signal must be presented to the processor chip at the beginning of each processor clock cycle and be stable during the high time of the processor clock. Either MHOLDA or MHOLDB can be used for stopping the processor during a cache miss or memory exception. MHOLDB has the same definition as MHOLDA. The processor hardware uses the logical "OR" of all hold signals (i.e., MHOLDA, MHOLDB and BHOLD) to generate a final hold signal for freezing the processor pipeline. All HOLD signals are latched (transparent latch) in the CY7C601 before they are used.

BHOLD. BHOLD is asserted by the I/O controller when an external bus master requests the data bus. Assertion of this signal will freeze the processor pipeline. External logic should guarantee that after deassertion of BHOLD, the data at all inputs to the chip is the same as what it was before BHOLD was asserted. This signal must be presented to the processor chip at the beginning of each processor clock cycle and be stable during the high time of the processor clock since the CY7C601 processes the BHOLD input through a transparent latch before it is used. BHOLD should be used only for bus access requests by an external device since the MDS and MEXC signals are not recognized while this input is active. BHOLD should not be deasserted while LOCK is asserted.

MDS. Assertion of this signal will enable the clock input to the on-chip instruction register (during an instruction fetch) or to the load result register (during a data fetch). In a system with cache, MDS is used to signal the processor when the missed data (cache miss) is ready on the bus. In a system with slow memories, MDS is used to signal the processor when the read data is available on the bus. MDS must be asserted only while the processor is frozen by either the MHOLDA or MHOLDB input signals. The CY7C601 samples the MDS signal via an on-chip transparent latch before it is used. The MDS signal is also used for strobing memory exceptions. In other words, MDS should be asserted whenever MEXC is asserted (see MEXC definition).

MEXC. This signal is asserted by the memory (or cache) controller to initiate an instruction (or data) exception trap. MEXC is latched in the processor at the rising edge of CLK and is used in the following cycle. If MEXC is asserted during an instruction fetch cycle an instruction access exception is generated, and if MEXC is asserted during a data fetch cycle, a data access exception trap is generated. The MEXC signal is used during (MHOLD) in conjunction with the MDS signal to indicate to the CY7C601 that the memory system was unable to supply valid instruction or data. If MDS is applied without MEXC, the CY7C601 accepts the contents of the data bus as valid information but when MDS is applied with MEXC an exception trap is generated and the contents of the data bus is ignored by the CY7C601. (i.e., MHOLD and MDS must be low when MEXC is asserted). MEXC must be deasserted in the same clock cycle in which MHOLD is released.

MAO. This signal is used during a MHOLD by the integer unit to select between the current memory access parameters and the previous (missed) memory parameters (i.e., the value of those parameters at the second rising edge of CLK before MHOLD was applied). A logic high value at this pin during a cache miss will cause the integer unit to put A[31:0], ASI[7:0], SIZE[1:0], RD, WE, WRT, LDSTO, LOCK, and DXFER values corresponding to the missed memory address on the bus. Normally, MAO should be kept at a "low" level, selecting the access parameters for the current access. MAO should not be used during store cycle misses because the WE output would be lost.

AOE. deassertion of this signal will three-state all output drivers associated with A[31:0] and ASI[7:0] outputs. AOE is connected directly to the output drivers of the address and ASI signals and must be asserted during normal operations. This signal should be deasserted only when the bus is granted to another bus master (i.e., when either BHOLD, MHOLDA or MHOLDB is asserted).

DOE. deassertion of this signal will three-state all output drivers of the data D[31:0] bus. DOE is connected directly to the data bus output drivers and must be asserted during normal operations. This signal should be deasserted only when the bus is granted to another bus master (i.e., when either BHOLD, MHOLDA or MHOLDB is asserted).

COE. deassertion of this signal will three-state all output drivers associated with SIZE[1:0], RD, WE, WRT, LOCK, LDSTO and DXFER outputs. COE is connected directly to the output drivers and must be asserted during normal operations. This signal should be deasserted only when the bus is granted to another bus master (i.e., when either BHOLD, MHOLDA, or MHOLDB is asserted).

RD. This signal specifies whether the current memory access is a read or write operation. It is sent out "unlatched" by the integer unit and must be latched externally before it is used. RD is set to "0" only during data cycles of store instructions including the store cycles of atomic load store instructions. This signal when used in conjunction with SIZE[1:0], ASI[7:0], and LDSTO, can be used to check access rights of bus transactions. In addition, the RD signal may be used to turn off the output drivers of data RAMs during a store operation. For atomic load store instructions the RD signal is "1" during the first data cycle (read cycle) and "0" during the second and third data cycles (write cycle).

WE. This signal is asserted by the integer unit during the second data cycle of store single instructions, the second and third data cycles of store double instructions, and the third data cycle of atomic load/store instructions. The WE signal is sent out "unlatched" and must be latched externally before it is used. The WE signal may be externally qualified by HOLD signals (i.e., MHOLDA and MHOLDB) to avoid writing into the memory during memory exceptions.

WRT. This signal is asserted (set to "1") by the processor during the first data cycle of single or double integer store instructions, the first data cycle of single or double floating-point store instructions, and the second data cycle of atomic load/store instructions. WRT is sent out "unlatched" and must be latched externally before it is used.

LDSTO. This signal is asserted by the integer unit during the data cycles of atomic load store operations. LDSTO is sent out "unlatched" by the integer unit and must be latched externally before it is used.

LOCK. This signal is set to "1" when the processor needs the bus for multiple cycle transactions such as atomic load/store, double loads and double stores. LOCK signal is sent "unlatched" and should be latched externally before it is used. The bus may not be granted to another bus master as long as LOCK signal is asserted (i.e., BHOLD should not be asserted in the following processor clock cycle when LOCK = 1).

DXFER. This signal is asserted by the processor at the beginning of all bus data transfer cycles. DXFER is "unlatched" and DXFER = 1 indicates a data cycle.

INULL. Assertion of INULL indicates that the current memory access (whose address is held in an external latch) is to be nullified by the processor. INULL is intended to be used to disable cache misses (in systems with cache) and to disable memory exception generation for the current memory access (i.e., MDS and MEXC should not be asserted for a memory access when INULL = 1). INULL is a latched output and is active during the same cycle as the address which it nullifies. INULL is asserted under the following conditions: During the second cycle of a store instruction, or whenever the CY7C601 address is invalid due to an external or internal exception. If a floating-point unit or coprocessor unit is present in the system, INULL should be ORed with the FNULL and CNULL signals from these units.

IFT. The state of this pin determines the behavior of the IFLUSH instruction. If IFT = 1, then IFLUSH executes like a NOP with no side effects. If IFT = 0, then IFLUSH causes an unimplemented instruction trap.

Floating-Point/Coprocessor Interface Signals

FP. This signal indicates whether or not a floating-point unit exists in the system. The FP signal is normally pulled up to VDD by a resistor. It is grounded when the FPU chip is present. The integer unit generates a floating-point disable trap if FP = 1 during the execution of a floating-point instruction, FBfcc instruction or floating-point load, and store instructions.

CP. This signal indicates whether or not a coprocessor exists in the system. The CP signal is normally pulled up to VDD by a resistor. It is grounded when the coprocessor chip is present. The integer unit generates a coprocessor disable trap if CP = 1 during the execution of a coprocessor instruction, CBccc instruction or coprocessor load and store instructions.

FCC[1:0]. These bits are taken as the current condition code bits of the FPU. They are considered valid if FCCV = 1. During the execution of the FBfcc instruction, the processor uses these bits to determine whether the branch should be taken or not. FCC[1:0] are latched by the processor before they are used.

CCC[1:0]. These bits are taken as the current condition code bits of the coprocessor. They are considered valid if CCCV = 1. During the execution of the CBccc instruction, the processor uses these bits to determine whether the branch should be taken or not. CCC[1:0] are latched by the processor before they are used.

FCCV. This signal should be asserted only when the FCC[1:0] bits are valid. The floating-point unit deasserts FCCV if pending floating-point compare instructions exist in the floating-point queue. FCCV is reasserted when the compare instruction is completed and the floating-point condition codes FCC[1:0] are valid. The integer unit will enter a wait state if FCCV is deasserted (i.e., FCCV = "0"). The FCCV signal is latched (transparent latch) in the CY7C601 before it is used.

CCCV. This signal should be asserted only when the CCC[1:0] bits are valid. The coprocessor deasserts CCCV if pending coprocessor compare instructions exist in the coprocessor queue. CCCV is reasserted when the compare instruction is completed and the coprocessor condition codes CCC[1:0] are valid. The integer unit will enter a wait state if CCCV is deasserted (i.e., CCCV = "0"). The CCCV signal is latched (transparent latch) in the CY7C601 before it is used.

FHOLD. This signal is asserted by the floating-point unit if a situation arises in which the FPU cannot continue execution. The floating-point unit checks all dependencies in the decode stage of the instruction and asserts FHOLD (if necessary) in the next cycle. This signal is used by the integer unit to freeze the instruction pipeline in the same cycle. The FPU must eventually deassert $\overline{\text{FHOLD}}$ in order to unfreeze the integer unit's pipeline. The $\overline{\text{FHOLD}}$ signal is latched (transparent latch) in the CY7C601 before it is used.

$\overline{\text{CHOLD}}$. This signal is asserted by the coprocessor if a situation arises in which the coprocessor cannot continue execution. The coprocessor checks all dependencies in the decode stage of the instruction and asserts $\overline{\text{CHOLD}}$ (if necessary) in the next cycle. This signal is used by the integer unit to freeze the instruction pipeline in the same cycle. The coprocessor must eventually deassert $\overline{\text{CHOLD}}$ in order to unfreeze the integer unit's pipeline. The $\overline{\text{CHOLD}}$ signal is latched (transparent latch) in the CY7C601 before it is used.

$\overline{\text{FEXC}}$. Assertion of this signal indicates that a floating-point exception has occurred. $\overline{\text{FEXC}}$ must remain asserted until the integer unit takes the trap and acknowledges the FPU via FXACK signal. Floating-point exceptions are taken only during the execution of floating-point instructions, FBfcc instruction and floating-point load, and store instructions. $\overline{\text{FEXC}}$ is latched in the integer unit before it is used. The FPU should deassert $\overline{\text{FHOLD}}$ if it detects an exception while $\overline{\text{FHOLD}}$ is asserted. In this case $\overline{\text{FEXC}}$ should be asserted a cycle before $\overline{\text{FHOLD}}$ is deasserted.

$\overline{\text{CEXC}}$. Assertion of this signal indicates that a coprocessor exception has occurred. This signal must remain asserted until the integer unit takes the trap and acknowledges the coprocessor via CXACK signal. Coprocessor exceptions are taken only during the execution of coprocessor instructions, CBccc instruction and coprocessor load and store instructions. $\overline{\text{CEXC}}$ is latched in the integer unit before it is used. The coprocessor should deassert $\overline{\text{CHOLD}}$ if it detects an exception while $\overline{\text{CHOLD}}$ is asserted. In this case $\overline{\text{CEXC}}$ should be asserted a cycle before $\overline{\text{CHOLD}}$ is deasserted.

INST. This signal is asserted by the integer unit whenever a new instruction is being fetched. It is used by the FPU or coprocessor to latch the instruction on the D[31:0] bus into the FPU or coprocessor instruction buffer. The FPU (or coprocessor) needs two instruction buffers (D1 and D2) to save the last two fetched instructions. When INST is asserted a new instruction enters into the D1 buffer and the old instruction in D1 enters into the D2 buffer.

FLUSH. This signal is asserted by the integer unit and is used by the FPU or coprocessor to flush the instructions in its instruction registers. This may happen when a trap is taken by the integer unit. Instructions that have entered into the floating-point (or coprocessor) queue may continue their execution if FLUSH is raised as a result of a trap or exception other than floating-point (or coprocessor) exceptions.

FINS1. This signal is asserted by the integer unit during the decode stage of an FPU instruction if the instruction is in the D1 buffer of the FPU chip. The FPU uses this signal to latch the instruction in D1 buffer into its Execute stage instruction register.

FINS2. This signal is asserted by the integer unit during the decode stage of an FPU instruction if the instruction is in the D2 buffer of the FPU chip. The FPU uses this signal to latch the instruction in D2 buffer into its execute stage instruction register.

CINS1. This signal is asserted by the integer unit during the decode stage of a coprocessor instruction if the instruction is in the D1 buffer of the coprocessor chip. The coprocessor uses this signal to latch the instruction in D1 buffer into its execute stage instruction register.

CINS2. This signal is asserted by the integer unit during the decode stage of a coprocessor instruction if the instruction is in the D2 buffer of the coprocessor chip. The coprocessor uses this signal to latch the instruction in D2 buffer into its execute stage instruction register.

FXACK. This signal is asserted by the integer unit in order to acknowledge to the FPU that the current $\overline{\text{FEXC}}$ trap is taken. The FPU must deassert $\overline{\text{FEXC}}$ after it receives an asserted level of FXACK signal so that the next floating-point instruction does not cause a "repeated" floating-point exception trap.

CXACK. This signal is asserted by the integer unit in order to acknowledge to the coprocessor that the current $\overline{\text{CEXC}}$ trap is taken. The coprocessor must deassert $\overline{\text{CEXC}}$ after it receives an asserted level of CXACK signal so that the next coprocessor instruction does not cause a "repeated" coprocessor exception trap.

Miscellaneous I/O Signals

IRL[3:0]. The data on these pins defines the external interrupt level. IRL[3:0] = 0000 indicates that no external interrupts are pending. The integer unit uses two on-chip synchronizing latches to sample these signals on the rising edge of CLK. A given interrupt level must remain valid for at least two consecutive cycles to be recognized by the integer unit. IRL[3:0] = 1111 signifies an non-maskable interrupt. All other interrupt levels are maskable by the PIL field of the Processor State Register (PSR). External interrupts should be latched and prioritized by the external logic before they are passed to the integer unit. The external interrupt latches should keep the interrupts pending until they are taken (and acknowledged) by the integer unit. External interrupts can be acknowledged by software or by the Interrupt Acknowledge (INTACK) output.

INTACK. This signal is asserted by the integer unit when an external interrupt is taken.

$\overline{\text{RESET}}$. Assertion of this pin will reset the integer unit. The $\overline{\text{RESET}}$ signal must be asserted for a minimum of eight processor clock cycles. After a reset, the integer unit will start fetching from address 0. The $\overline{\text{RESET}}$ signal is latched by the integer unit before it is used.

$\overline{\text{ERROR}}$. This signal is asserted by the integer unit when a trap is encountered while traps are disabled via the ET bit in the PSR. In this situation the integer unit saves the PC and nPC registers, sets the tt value in the TBR, enters into an error state, asserts the $\overline{\text{ERROR}}$ signal and then halts. The only way to restart the processor trapped in the error state, is to trigger a reset by asserting the $\overline{\text{RESET}}$ signal.

$\overline{\text{TOE}}$. This signal is used to force all output drivers of the processor chip into a high-impedance state. It is used to isolate the chip from the rest of the system for debugging purposes.

FPSYN. This pin is a mode pin which is used to allow execution of additional instructions in future designs. It should be normally kept deasserted (FPSYN = 0) to disable the execution of these instructions.

CLK. CLK is a 50% duty-cycle clock used for clocking the CY7C601's pipeline registers. It is HIGH during the first half of the processor cycle, and LOW during the second half. The rising edge of CLK defines the beginning of each pipeline stage in the CY7C601 chip.

CYPRESS SEMICONDUCTOR

Floating-Point Unit

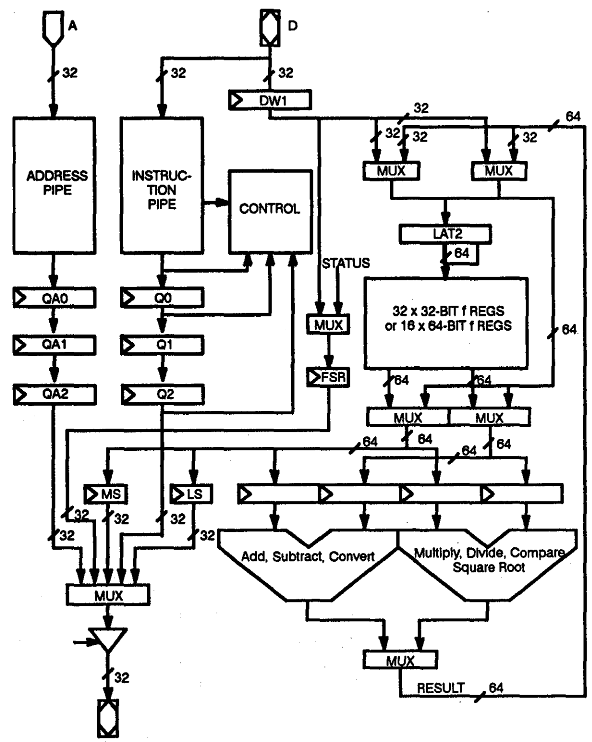
Features

- Direct interface to CY7C601 integer unit
- Direct interface to CY7C157 cache RAM
- Full compliance with ANSI/IEEE-754 standard for binary floating-point arithmetic
- Supports single and double precision floating-point operations
- 6.15 MFLOPs peak double-precision performance at 40 MHz
- SPARC-compatible interface allows concurrent execution of integer and floating-point instructions
- Hardware interlocks synchronize integer unit and floating-point unit operations
- 64-bit multiplier and divide/square root unit
- 64-bit ALU
- 16 64-bit registers or 32 32-bit registers in a three-port floating-point register file with an independent load/store port.
- 144-pin PGA package
- Available in speeds of 25, 33, and 40 MHz

Description

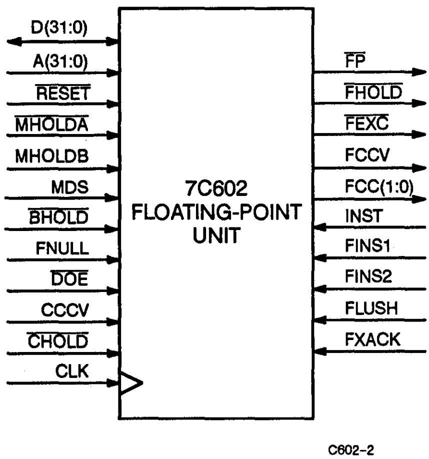
The CY7C602 is a high-speed SPARC®-compatible floating-point unit for use with the CY7C601 integer unit. The CY7C602 floating-point unit allows floating-point instructions to execute concurrently with CY7C601 integer unit instructions. The CY7C602 interfaces directly to the CY7C601 integer unit without glue logic. The CY7C602 provides a peak 6.15 MFLOPS of double-precision performance at 40 MHz.

Logic Block Diagram



C602-1

Pin Configuration



C602-2

Selection Guide

		7C602-40	7C602-33	7C602-25
Maximum Supply Current (mA)	Commercial	450	400	350

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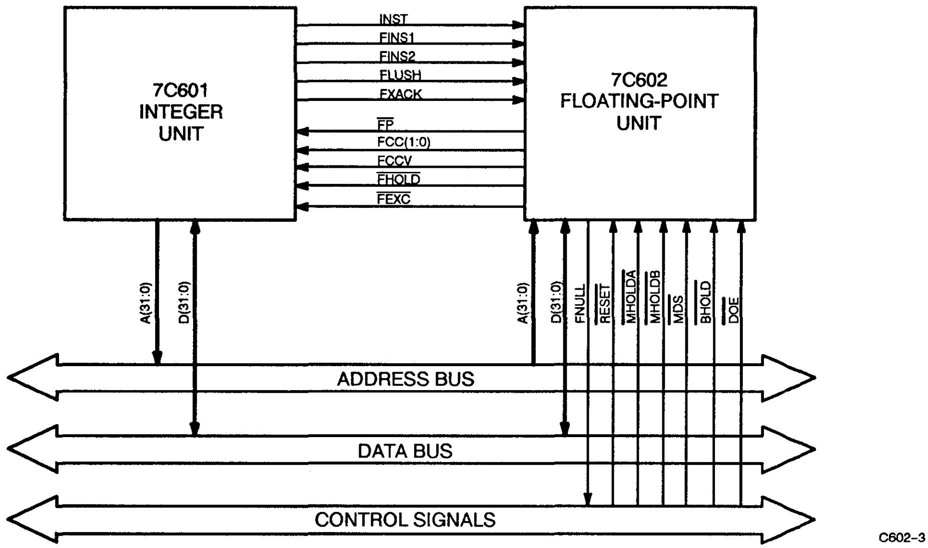


Figure 1. CY7C601 - CY7C602 Hardware Interface

Functional Description

The CY7C602 floating-point unit is a high-performance, single-chip implementation of the SPARC reference floating-point unit. The CY7C602 FPU directly interfaces with the CY7C601 integer unit, providing concurrent floating-point and integer instruction execution. The Cypress 7C600 chip-set, comprised of the CY7C601 integer unit, CY7C602 floating-point unit, CY7C604 cache controller and memory management unit, and two CY7C157 cache RAMs, constitutes a high-performance CPU requiring no interface logic. The Cypress 7C600 chip-set is available in speeds up to 40 MHz, providing a sustained 29 MIPS of integer unit performance and over 6 MFLOPS of double-precision floating-point performance.

The CY7C602 supports single and double precision floating-point operation. Double precision floating-point is efficiently executed in the CY7C602 using a 64-bit internal datapath. The floating-point datapath circuitry contains a 64-bit multiplier, a 64-bit ALU, and a 64-bit divide/square-root unit. The CY7C602 provides thirty-two 32-bit floating-point registers, which can be concatenated for use as 64-bit registers. The CY7C602 complies with the ANSI/IEEE-754 floating-point standard.

The CY7C602 supports the execution of SPARC floating-point instructions. These instructions are separated into two groups: floating-point load/store and floating-point operate instructions (FPops). Floating-point load/store instructions are used to transfer data to and from the data registers (f registers). FP load/store instructions also allow the CY7C601 integer unit to read and write the floating-point status register (FSR) and to read the front entry of the floating-point queue. Floating-point operate instructions (FPops) include basic numeric operations (add, subtract, multiply, and divide), conversions between data types, register to register moves, and floating-point number comparison. FPops operate only on data in the floating-point registers. Floating-point branch instructions are executed by the IU on the basis of FP condition codes, and are not executed by the FPU.

The SPARC floating-point/integer unit interface provides concurrent execution of integer and floating-point instructions. The CY7C601 integer unit fetches all instructions for both itself and the CY7C602 FPU, providing all addressing and control signals. The CY7C602 floating-point unit latches all integer and floating-point instructions in parallel with the CY7C601. When the CY7C601 decodes a floating-point instruction, it signals the CY7C602 with the FINS1 or FINS2 signal. This starts the execution of the floating-point instruction by the CY7C602.

7

CY7C602 Registers

The CY7C602 has three types of user-accessible registers: the f registers, the FP queue, and the floating-point status register (FSR). The f registers are the CY7C602 data registers. The FSR is the CY7C602 status and operating mode register. The FP queue contains the CY7C602 instructions that have started execution and are awaiting completion. The following section describes these registers in detail.

f Registers

The CY7C602 provides 32 registers for floating-point operations, referred to as f registers. These registers are 32 bits in length, which can be concatenated to support 64-bit double words.

Integer and single precision data requires a single 32-bit f register. Double precision data requires 64 bits of storage and occupies an even-odd pair of adjacent f registers. Extended precision data requires 128 bits of storage and occupies a group of four consecutive f registers, always starting with register f0, f4, f8, f12, f20, f24, or f28.

The CY7C602 forces register addressing to match the data type specified by the floating-point instruction. This ensures data alignment in the f register file for double and extended precision data. *Figure 2* illustrates how the CY7C602 uses the five register address bits in a floating-point instruction for the different types of data. Single data word transfers (integer, single-precision floating-point) can be stored in any register. Consequently, all five bits of the register address specified in the floating-point instruction are valid. Double precision data must reside in an even-odd pair of adjacent registers. By ignoring the LSB of the register address for a FPop requiring a register pair, the CY7C602 ensures data alignment. In a similar manner, the two LSBs of the register address are ignored in a SPARC FPU that supports extended precision data.

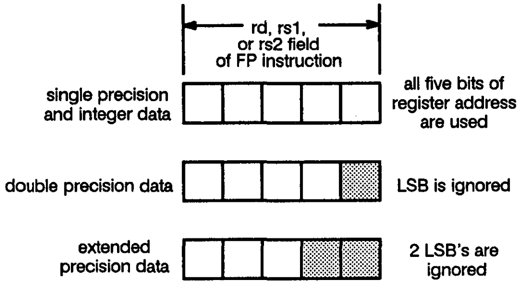


Figure 2. f Register Addressing

FP Queue

The CY7C602 maintains a floating-point queue of instructions that have started execution, but have yet to complete execution. The FP queue is used to accommodate the multiple clock nature of floating-point instructions. It also allows the CY7C602 to optimize execution through the use of data forwarding. Data forwarding allows FPop results to be used by a subsequent FPop before the results have been stored in its destination register. This saves one clock of execution time for each instruction that uses this feature.

The other purpose of the FP queue is to support the handling of FP exceptions. When the CY7C602 encounters an exception case, it enters pending exception mode and waits for the next FP instruction to be executed. When the CY7C601 decodes a FP instruction following the exception, it asserts the FINS1 or FINS2 signal. The CY7C602 then enters exception mode and asserts $\overline{\text{FEXC}}$ to signal a floating-point exception. When the CY7C602 enters the exception mode, floating-point execution halts until the FP queue is emptied. This allows the CY7C601 to store the floating-point instructions under execution when the exception case occurred. Emptying the FP queue frees the CY7C602 for use by the trap handler without losing the pre-exception state of the CY7C602. After the trap handler finishes execution, the CY7C601 re-fetches the FPop instructions previously stored in the FP queue, thus bringing the CY7C602 back to its previous state.

The FP queue contains the 32-bit address and 32-bit FPop instruction of up to three instructions under execution. Only FPop instructions are queued. The top entry of the FP queue is accessible by executing the store double floating-point queue (STDFQ) instruction. A load FP queue instruction does not exist, as the FP queue must be re-initialized by launching the queued instructions.

Floating-Point Status Register (FSR)

The following paragraphs describe the bit fields of the Floating-Point Status Register (FSR). *Figure 3* illustrates the bit assignments for the FSR. Refer to *Table 1* (following page) for bit assignments for the FSR fields.

RD *FSR(31:30).* Rounding Direction: These two bits define the rounding direction used by the CY7C602 during an FP arithmetic operation.

RP *FSR(29:28).* Rounding Precision: These two bits define the rounding precision to which extended results are rounded. This is in accordance with the ANSI/IEEE STD-745-1985.

TEM *FSR(27:23).* Trap Enable Mask: These five bits enable traps caused by FPops. These bits are ANDed (1 = enable, 0 = disable) with the bits of the CEXC (current exception field) to determine which traps will force a floating-point exception to the CY7C601. All trap enable fields correspond to the similarly named bit in the CEXC field (see below). The TEM field only affects which bits in the CEXC field will cause the $\overline{\text{FEXC}}$ signal to be asserted. ALL trap types, regardless of the state of the TEM field, are reported in the AEXC and CEXC fields.

NS *FSR(22).* Non-Standard Floating Point: This bit enables non-standard floating-point operations in the CY7C602.

version *FSR(19:17).* The version number is used to identify the SPARC floating-point processor type. This field is set to 011 (3H) for the CY7C602, and is read-only.

FTT *FSR(16:14).* Floating-point Trap Type: This field identifies the floating-point trap type of the current FP exception. This field can be read and written, and must be cleared by software.

QNE *FSR(13).* Queue Not Empty: This bit signals whether the FP queue is empty. (0 = empty, 1 = not empty)

FCC *FSR(11:10).* Floating-point Condition Codes: These two bits report the FP condition codes (see *Table 1* below).

AEXC *FSR(9:5).* Accumulated EXCeptions: This field reports the accumulated FP exceptions. All exception cases, masked or unmasked, are ORed with the contents of the AEXC and accumulated as status. All accumulated fields have the same definition as the corresponding field for CEXC (see below). This field can be read and written, and must be cleared by software (see *Table 1* below).

CEXC *FSR(4:0).* Current EXCeptions: This field reports the current FP exceptions. This field is automatically cleared upon the execution of the next floating-point instruction. CEXC status is not lost upon assertion of a floating-point exception, since instructions following a valid exception are not executed by the CY7C602. The following defines the five CEXC bits:

nvc = 1 indicates invalid operation exception. This is defined as an operation using an improper operand value. An example of this is 0/0, ∞, or −∞.

ofc = 1 indicates overflow exception. The rounded result would be larger in magnitude than the largest normalized number in the specified format.

ufc = 1 indicates underflow exception. The rounded result is inexact, and would be smaller in magnitude than the smallest normalized number in the indicated format.

dzc = 1 indicates division-by-zero, X/0, where X is subnormal or normalized. Note that 0/0 does not set the dzc bit.

nxc = 1 indicates inexact exception. The rounded result differs from the infinitely precise correct result.

R *FSR21, 20, and 12.* Reserved - always set to 0.

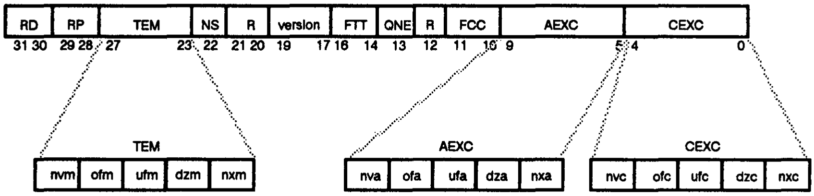


Figure 3. Floating-Point Status Register

Table 1. Floating-Point Status Register Summary

Field	Values	FSR bits	Description	Loadable by LDFSR
RD	0 - Round to nearest (tie-even) 1 - Round to 0 2 - Round to $+\infty$ 3 - Round to $-\infty$	31:30	Rounding Direction	yes
RP	0 - Extended precision 1 - Single precision 2 - Double precision 3 - Reserved	29:28	Extended Rounding Precision	yes
TEM	0 - Disable trap 1 - Enable trap NVM OFM UFM DZM NXM	27:23 27 26 25 24 23	Trap Enable Mask invalid operation trap mask overflow trap mask underflow trap mask divide by zero trap mask inexact trap mask	yes
NS	0 - Disable 1 - Enable	22	Non-standard Floating-point	yes
version	0 - 7	19:17	FPU version number	no
FIT	0 - None 1 - IEEE Exception 2 - Unfinished FPop 3 - Unimplemented FPop 4 - Sequence Error 5 - 7 Reserved	16:14	Floating-point trap type	no
QNE	0 - queue empty	13	Queue Not Empty	no
FCC	0 - = 1 - < 2 - > 3 - Unordered	11:10	Floating-point Condition Codes	yes
AEXC	 NVA OFA UFA DXA NXA	9:5 9 8 7 6 5	Accrued Exception Bits accrued invalid exception accrued overflow exception accrued underflow exception accrued divide by zero exception accrued inexact exception	yes
CEXC	 NVC OFC UFC DZC NXC	4:0 4 3 2 1 0	Current Exception Bits current invalid exception current overflow exception current underflow exception current divide by zero exception current inexact exception	yes
r	Always set to 0	21, 20, 12	reserved bits	no

7

CY7C602 Pin Definitions

Integer Unit Interface Signals:

FP *active-low output.* Floating-point Present: This signal indicates to the CY7C601 that a FPU is present in the system. In the absence of a FPU, this signal is pulled up to VCC by a resistor. This is a static signal; it always asserts a low output. The CY7C601 generates a floating-point disable trap if FP is not asserted during the execution of a floating-point instruction.

FCC(1:0) *output.* Floating-point Condition Codes: The FCC(1:0) bits indicate the current condition code of the FPU, and are valid only if FCCV is asserted. FBfcc instructions use the value of these bits during the execute cycle if they are valid. If the FCC bits are not valid, then FCCV is released, which halts the CY7C601 until the FCC bits become valid.

FCC1	FCC0	Condition
0	0	equal
0	1	Op1 < Op2
1	0	Op1 > Op2
1	1	Unordered

Table 2. FCC(1:0) Condition Codes

FCCV *output.* Floating-point Condition Codes Valid: The CY7C602 asserts the FCCV signal when the FCC represent a valid condition. The FCCV signal is deasserted when a pending floating-point compare instruction exists in the floating-point queue. FCCV is reasserted when the compare instruction is completed and FCC bits are valid.

FHOLD *output.* Floating-point HOLD: The FHOLD signal is asserted by the CY7C602 if it cannot continue execution due to a resource or operand dependency. The CY7C602 checks for all dependencies in the decode stage, and if necessary, asserts FHOLD in the next cycle. The FHOLD signal is used by the CY7C601 to freeze its pipeline in the same cycle. The CY7C602 must eventually deassert FHOLD to release the CY7C601 pipeline.

FEXC *output.* Floating-point EXCeption: The FEXC is asserted if a floating-point exception has occurred. It remains asserted until the CY7C601 acknowledges that it has taken a trap by asserting FXACK. Floating-point exceptions are taken only during the execution of a floating-point instruction. The CY7C602 releases FEXC when it receives FXACK.

FXACK *input.* Floating-point eXception ACKnowledge: The FXACK signal is asserted by the CY7C601 to acknowledge to the CY7C602 that the current FP trap is taken.

INST *input.* INSTruction fetch: The INST signal is asserted by the CY7C601 whenever a new instruction is being fetched. It is used by the CY7C602 to latch the instruction on the D(31:0) bus into the FPU instruction buffer. The CY7C602 has two instruction buffers (D1 and D2) to save the last two fetched instructions. When INST is asserted, the new instruction enters the D1 buffer and the old instruction in D1 enters the D2 buffer.

FINS1 *input.* Floating-point INStruction in buffer 1: The FINS1 signal is asserted by the CY7C601 during the decode stage of a FPU instruction if the instruction is stored in the D1 buffer of the CY7C602. The CY7C602 uses this signal to launch the instruction in the D1 buffer into its execute stage instruction register.

FINS2 *input.* Floating-point INStruction in buffer 2: The FINS2 signal is asserted by the CY7C601 during the decode stage of a FPU instruction if the instruction is stored in the D2 buffer of the CY7C602. The CY7C602 uses this signal to launch the instruction in the D2 buffer into its execute stage instruction register.

FLUSH *input.* Floating-point instruction fLUSH: The FLUSH signal is asserted by the CY7C601 to signal to the CY7C602 to flush the instructions in its instruction registers. This may happen when a trap is taken by the CY7C601. The CY7C601 will restart the flushed instructions after returning from the trap. FLUSH has no effect on instructions in the floating-point queue. In addition to freezing the FPU pipeline, the CY7C602 uses FLUSH to shut off D bus drivers during store. To ensure correct operation of the CY7C602, FLUSH must not change state more than once during a clock cycle.

Coprocessor Interface Signals:

CHOLD *input.* Coprocessor HOLD: The CHOLD signal is asserted by the coprocessor if it cannot continue execution. The coprocessor must check all dependencies in the decode stage of the instruction and assert the CHOLD signal, if necessary, in the next cycle. The coprocessor must eventually deassert this signal to unfreeze the CY7C601 and CY7C602 pipelines. The CHOLD signal is latched with a transparent latch in the CY7C602 before it is used.

CCCV *input.* Coprocessor Condition Codes Valid: The coprocessor asserts the CCCV signal when the CCC(1:0) represent a valid condition. The CCCV signal is deasserted when a pending floating-point compare instruction exists in the coprocessor queue. CCCV is reasserted when the compare instruction is completed and CCC bits are valid. The CY7C602 will enter a wait state if CCCV is deasserted. The CCCV signal is latched with a transparent latch in the CY7C602 before it is used.

System/Memory Interface Signals:

A(31:0) *input.* Address bus (31:0): The address bus for the CY7C602 is an input-only bus. The CY7C601 supplies all addresses for instruction and data fetches for the CY7C602. The CY7C602 captures addresses of floating-point instructions from the A(31:0) bus into the DDA register. When INST is asserted by the CY7C601, the contents of the DDA is transferred to the DA1 register.

D(31:0) *input/output.* Data bus (31:0): The D(31:0) bus is driven by the FPU only during the execution of floating-point store instructions. The store data is sent out unlatched and must be latched externally before it is used. Once latched, store data is valid during the second data cycle of a store single access and on the second and third data cycle of a store double access. The data alignment for load and store instructions is done inside the FPU. A double word is aligned on an eight-byte boundary. A single word is aligned on a four-byte boundary.

DOE *input.* Data Output Enable: The DOE signal is connected directly to the data output drivers and must be asserted during normal operation. deassertion of this signal tri-states all output drivers on the data bus. This signal should be deasserted only when the bus is granted to another bus master, i.e, when either BHOLD, MHOLDA, or MHOLDB is asserted.

MHOLDA, MHOLDB *input.* Memory HOLD: Asserting MHOLDA or MHOLDB freezes the CY7C602 pipeline. Either MHOLDA or MHOLDB is used to freeze the FPU (and the IU) pipelines during a cache miss (for systems with cache) or when slow memory is accessed.

BHOLD *input.* Bus HOLD: This signal is asserted by the system's I/O controller when an external bus master requests the data bus. Assertion of this signal will freeze the FPU pipeline. External logic should guarantee that after deassertion of BHOLD, the state of all inputs to the chip is the same as before BHOLD was asserted.

MDS *input.* Memory Data Strobe: The MDS signal is used to load data into the FPU when the internal FPU pipeline is frozen by assertion of MHOLDA, MHOLDB, or BHOLD.

FNULL *output.* Fpu NULLify cycle: This signal signals to the memory system when the CY7C602 is holding the instruction pipeline of the system. This hold would occur when FHOLD or FCCV is asserted. This signal is used by the memory system in the same fashion as the integer unit's INULL signal. The system needs this signal because the IU's INULL does not take into account holds requested by the FPU.

RESET *input.* RESET: Asserting the RESET signal resets the pipeline and sets the writable fields of the floating-point status register (FSR) to zero. The RESET signal must remain asserted for a minimum of eight cycles. After a reset, the IU will start fetching from address 0.

CLK *input.* CLocK: The CLK signal is used for clocking the FPU's pipeline registers. It is high during the first half of the processor cycle and low during the second half. The rising edge of CLK defines the beginning of each pipeline stage in the FPU.

CYPRESS SEMICONDUCTOR

Cache Controller and Memory Management Unit

Features

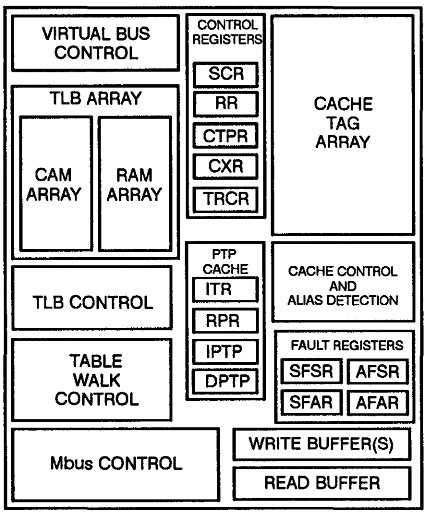
- Fully conforms to the SPARC® Reference Memory Management Unit (MMU) Architecture
- Support for virtual memory
- Supports context switching
  - 4096 contexts for TLB entries
  - 4096 contexts for cache tag
- On-chip Translation Lookaside Buffer (TLB)
  - 64 fully associative entries
  - Multi-level TLB flush
  - TLB probe support
  - Lockable entries
  - Random TLB replacement
  - Supports multi-level address mapping (4-kbyte, 256-kbyte, 16-Mbyte, and 4-Gbyte).
- Page-level memory access protection
  - Read/Write/Execute
  - User/supervisor modes
- Hardware table walk
- Large address space support
  - 32-bit virtual address
  - 36-bit physical address
- 2048 cache tag entries
- 32-byte cache line size
- Address and data latches for virtual bus
- Lockable cache
- Write-through and copy-back cache polices
- 32-byte read line buffer
- 32-byte copy-back write line buffer
- 32-byte write-through buffer
- Conforms to SPARC Reference Mbus Level 1 specification
- Aliasing detection
- Byte write generation
- 0.8-micron CMOS technology
- 2.2 watts typical power dissipation at 33 MHz

Description

The CY7C604 consists of a cache controller with on-chip cache tag and a memory management unit. It is a high-speed CMOS implementation of the SPARC reference memory management architecture, combined with a cache tag and cache memory controller. The CY7C604 directly connects to the CY7C601 integer unit microprocessor and CY7C157 cache data RAM without any external circuitry.

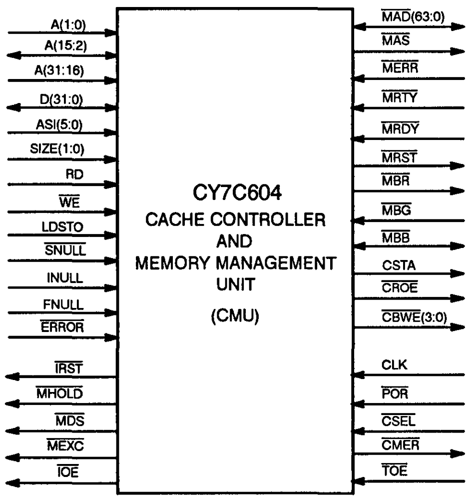
When combined with two CY7C157 16-kbyte by 16 cache RAMs, the CY7C604 forms a complete, no wait-state, 64-kbyte direct mapped virtual cache. The cache size can be scaled up to 256-kbyte and the number of TLB entries increased to 256 with the use of additional CY7C604s and CY7C157s.

Logic Block Diagram



C602-1

Pin Configuration



C602-2

Selection Guide

		7C604-40	7C604-33	7C604-25
Maximum Supply Current (mA)	Commercial	650	600	600
	Military			650

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Functional Description

The CY7C604 (CMU) is a combined Memory Management Unit (MMU) and cache controller with on-chip cache tag memory. The CY7C604 is designed as part of a system solution for high-performance computing using the Cypress SPARC chip set. This chip set consists of the CY7C601 integer unit, the CY7C602 floating-point unit, the CY7C604 CMU, and two CY7C157 cache RAMs. The Cypress SPARC chip set comprises a five chip, high-performance CPU requiring no additional glue logic. As part of this chip set, the CY7C604 provides support for large addressing spaces with virtual to physical address translation. In addition to an MMU, the CY7C604 provides 2048 cache tag entries and logic to control a 64-kbyte virtual cache. The CY7C604 is a high-performance, high-ingetration solution to virtual memory and cache support for the CY7C600 family.

The CY7C604 is designed to be used in conjunction with the CY7C157 cache RAM. Two 16-kbyte x 16-bit CY7C157s and one CY7C604 constitute a 64-kbyte cache. The combination of a CY7C604 and two CY7C157s may be cascaded to provide up to 256 kbytes of cache.

The MMU portion of the CY7C604 provides translation from a 32-bit virtual address range (4 gigabytes) to a 36-bit physical address (64 gigabytes), as provided in the SPARC reference MMU specification. Virtual address translation is further extended with the use of a context register, which is used to identify up to 4096 contexts or tasks. The cache tag entries and TLB entries contain context numbers to identify tasks or processes. This minimizes unnecessary cache tag and TLB entry replacement during task switching.

The MMU features a 64-entry Translation Lookaside Buffer (TLB). The TLB acts as a cache for address mapping entries used by the MMU to map a virtual address to a physical address. These mapping entries, referred to as page table entries or PTEs, allow one of four levels of address mapping. A PTE can be defined as the address mapping for a single 4-kbyte page, a 256-kbyte region, a 16-Mbyte region, or a 4-Gbyte region. The TLB entries are lockable, allowing important TLB entries to be excluded from replacement. The use of multiple CY7C604s in a system allows the number of TLB entries to increase from 64 up to a maximum of 256.

The MMU performs its address translation task by comparing a virtual address supplied by the CY7C601 (integer unit) to the address tags in the TLB entries. If the virtual address and the value of the context register match a TLB entry, a TLB "hit" occurs. When this occurs, the physical address stored in the TLB is used to translate the virtual address to a physical address. The access type (read/write of data or instruction) and privilege level (user/supervisor) are checked during translation. If a TLB hit occurs but access level protection is violated, the MMU signals an exception and the operation ends.

If the virtual address or context does not match any valid TLB entry, a TLB "miss" occurs. This causes a table walk to be performed by the MMU. The table walk is a search performed by the MMU through the address translation tables stored in main memory. The MMU searches through several levels of tables for the PTE corresponding to the virtual address. Upon finding the PTE, the MMU translates the address and selects a TLB entry for replacement, where it then stores the PTE.

The 64-kbyte virtual cache is organized into 2048 lines of 32 bytes each. The term "virtual cache" refers to the direct addressing of the cache by the integer unit (CY7C601) with the virtual address bus. Virtual address bits (VA(15:5)) select the cache line, and virtual address bits (VA(4:2)) select the 32-bit word of the cache line, as illustrated in *Figure 1.* The CY7C604 provides access control for the cache by checking the context and virtual address against the cache tags. If the virtual address, access level, and context match the cache tag for the cache line addressed, a cache hit occurs and the access is enabled. If the virtual address or context do not match the cache tag for the cache line, a cache miss occurs and the cache controller accesses main memory for the required data.

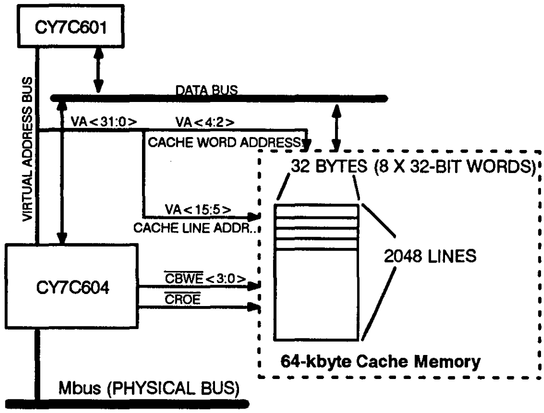


Figure 1. Virtual 64-kbyte Cache

The CY7C604 provides cache locking, which prevents the data stored in the cache from being replaced. The entire cache is locked by setting the Cache Lock bit (CL) in the System Control Register (SCR).

The cache controller supports two modes of caching: write-through with no write allocate and copy-back with write allocate. Write-through mode is a simpler style of cache management that causes write accesses to the cache to be written through to main memory upon each write access. The advantage of this method is that the cache always remains coherent with main memory. Its disadvantage is that each write to the cache is echoed to main memory, which increases traffic on the system bus. Another disadvantage to write-through is that the processor is delayed by the time required to arbitrate the system bus and write the data to main memory. However, in the case of the CY7C604, this disadvantage is largely offset by the inclusion of write buffers. The write buffers can store up to four double-word accesses, allowing the CY7C601 to continue execution while data is written to main memory.

Copy-back cache mode causes write accesses to be written to the cache only. This causes the cache line to become modified. Modified cache lines are automatically written back to main memory only when the cache line is no longer needed. Copy-back mode provides substantial system performance improvements over write-through due to decreased traffic on the system bus.

A 32-byte write buffer and a 32-byte read buffer are provided in the CY7C604 to fully buffer the transfer of a cache line. This feature allows the CY7C604 to simultaneously read a cache line from main memory as it is flushing a modified cache line from the cache. This feature is also used in write-through cache mode for write accesses to main memory. The write buffer avoids stalling the CY7C601 on writes to main memory by storing the write data until the physical bus becomes available. The write buffer writes the data to memory as a background task.

The CY7C604 supports the SPARC Mbus standard bus interface. The Mbus is a peer level, high-speed, 64-bit, multiplexed address and data bus which supports a full peer level protocol (i.e., multiple bus masters). The Mbus transfers data in either burst or non-burst mode, depending upon size. Data transactions larger than eight bytes (one doubleword) are transferred in burst mode, which consists of an address phase followed by four data phases (32-bytes total). Non-burst transactions consist of an address phase followed by one data phase, and are used for data transactions less than eight bytes. Bus mastership is granted and controlled by an external bus arbiter. The bus arbiter sets bus priorities, and grants access to a bus master.

Memory Management Unit

The MMU provides virtual to physical address translation with the use of an on-chip Translation Lookaside Buffer (TLB). The translation lookaside buffer is in reality a full Address Translation Cache (ATC) for address translation entries stored from tables in main memory. These entries, referred to as page table entries or PTEs, contain the mapping information used by the MMU to translate the virtual addresses. Addresses presented to the MMU for translation are compared against the set of PTEs stored in the TLB. All entries in the TLB are simultaneously accessed through the use of advanced Content Addressable Memory (CAM) technology. If a match for the virtual address and context is found in a valid TLB entry and the access protection is not violated, a TLB hit occurs and the address is translated. A virtual address and context that matches a valid TLB entry but violates the memory access protections will cause the CY7C604 to generate a memory exception to the CY7C601. If the TLB entries do not match the address and context, or the TLB entry is invalid, then a TLB miss occurs. The MMU responds to the TLB miss by initiating a table walk to find the correct PTE stored in main memory for the virtual address.

The MMU uses a tree-structured table walk algorithm to find page table entries not found in the TLB. The table walk is a search through a series of tables in main memory for the PTE corresponding to a virtual address. The table walk uses a series of four tables. These tables are: the context table, the level 1 table, the level 2 table, and the level 3 table. The table walk uses the context pointer register as a base register and the context number as an offset to point to an entry in the context table. At any address, the MMU finds either a PTE, which terminates its search, or a page table pointer (PTP). A PTP is a pointer used in conjunction with a field in the virtual address to select an entry in the next level of tables. The table walk continues searching through levels of tables as long as PTPs are found pointing to the next table. The table walk terminates when a PTE is found, or an exception is generated if a PTE is not found after accessing the level 3 table. An exception is also generated if the table walk finds an invalid or reserved entry in the page tables.

Upon finding the PTE, the CY7C604 stores it in an available TLB entry and translates the corresponding virtual address. The table walk processing is implemented in the CY7C604 hardware. It is self-initiated, and is transparent to the user.

Cache Controller

The cache controller provides cache memory access control for a 64-kbyte direct mapped virtual cache. The cache controller is designed to use two CY7C157 cache RAMs for the cache memory. These cache RAMs are 16-kbyte x 16 SRAMs with on-chip address and data latches and timing control. The CY7C601 cache can be expanded to a maximum of 256 kbytes by adding additional groups of one CY7C604 and two CY7C157s. Using multiple CY7C604s to expand the cache is referred to as a multichip configuration for the CY7C604, and is described in the CY7C604 Multichip Configuration section in the SPARC RISC User's Manual.

The cache is organized as 2048 cache lines of 32 bytes each. The CY7C604 has 2048 cache tag entries on-chip, one tag entry for each cache line. Addressing for the virtual cache is provided directly from the virtual address bus. The virtual address field (VA(15:5)) selects one of the 2048 lines of the cache. This address field also selects one of the corresponding cache tag entries in the CY7C604. A cache hit occurs when the upper sixteen bits of the virtual address and the context register match with the virtual address and context stored in the selected cache tag entry. The lowest five bits of the virtual address bus (VA(4:0)) select one of the 32 bytes in the cache line. Cache data replacement is always performed by replacing cache lines.

The cache is designed to provide data with every read access asserted on the virtual bus, regardless of the cache controller. The CY7C604 controls cache read access by halting the CY7C601 if a cache hit is not detected by the cache controller. The cache controller then reads the new cache line from main memory, and supplies the correct data to the CY7C601. After the correct data is latched into the CY7C601 by strobing the $\overline{\text{MDS}}$ signal, the CY7C601 is released and execution proceeds normally.

Writes to the cache are controlled by the CY7C604, which decodes the lowest two bits of the virtual address, the SIZE(1:0) signal, and checks for a cache hit to enable the correct cache byte write enable signals. If a cache write hit occurs, the CY7C604 decodes the correct $\overline{\text{CBWE}}$ signals for the write access, and outputs these to the CY7C157 cache RAM write enables. If the cache mode is set to write-through (see Cache Modes), the write data is also written to main memory. If a write cache miss occurs for write-through cache mode, the data is written to main memory and the cache is not updated. If the write cache miss occurs during copy-back cache mode (see Cache Modes), the cache line is fetched from main memory. If the cache line stored in the cache when the write cache miss occurred has been modified, the old cache line is written to main memory before the cache line is replaced by the new data. After the cache line has been replaced, the write access is enabled by the CY7C604.

Cache Tag

The CY7C604 features 2048 direct-mapped cache tag entries. The on-chip cache tag and the TLB are accessed simultaneously. Each entry in the cache consists of 16 bits of virtual address (VA(31:16)), a 12-bit context number (CXN(11:0)), one valid bit (V) and one modified bit (M). The valid bit (V) is set or cleared to indicate the validity of the cache tag entry. The modified bit (M) of a cache tag entry is set during copy-back mode after a write access to the cache line. This indicates that the cache line has been modified. The modified bit has no meaning for write-through cache mode. The cache line select field (VA(15:5)) is used to select a cache line entry and its corresponding cache tag entry. The address field (VA(31:16)) and context register are compared against the virtual address and the context fields of the selected cache tag entry. If a match occurs, then a cache hit is generated. If a match is not found, then a cache miss is generated. To complete an access successfully, both the cache tag and the TLB must be hit with appropriate access level permission. On Power-On Reset ($\overline{\text{POR}}$), all cache tag entries are invalidated (all V bits are cleared).

A supervisor bit (S) is included in the cache tag entry. For cache tag entries which are accessible by the supervisor only (access level field 6 or 7), the S bit is set. During a cache tag look up, if the access is supervisor mode and the the S bit is set, the context number comparison is ignored and the context match is forced. This operation is similar to a TLB look up with access level field set to either 6 or 7.

Cache Modes

The virtual cache can be programmed for either write-through with no write allocate or copy-back with write allocate. The two cache modes differ in how they treat cache write accesses. Write-through cache mode causes write hits to the cache to be written to both cache and main memory. Write-through write cache misses will only update main memory and invalidate the cache tag, but will not modify the cache.

A write access in copy-back mode will modify the cache only. The writing of the modified cache line to main memory is deferred until the cache line is no longer required. Copy-back cache mode has the advantage of reducing traffic on the system bus. Bus traffic is reduced since all updates to memory are deferred and are performed subsequently only as absolutely required. In addition, all such data transfers are made utilizing the more efficient burst mode.

CY7C604 Registers

All values in all control registers are read/write (with the exception of the implementation and version fields of the SCR). Control registers are accessible by use of the alternate space load or store instructions with ASI = 4.

Programmer's Note: To ensure software compatibility with future versions of the CY7C604, reserved fields in a register should be written as zeros and masked out when read.

System Control Register (SCR)

The system control register, as shown in *Figure 2*, defines the operation modes for the cache controller and MMU. The following describes the functions of the bit fields in the SCR.

CE. *Cache-enable bit* (SCR(8)) indicates whether the virtual cache is enabled or not. This bit is set to 1 to enable the cache controller.

CL. *Cache-lock bit* (SCR(9)) indicates whether the entire cache is locked or not. This bit is set to 1 to lock the cache.

CM. *Cache-mode bit* (SCR(10)) indicates whether the cache is operating under write-through no write allocate policy or copy-back write allocate policy. This bit is set to 1 to enable copy-back cache mode. Setting this bit to 0 will enable write-through cache mode.

C. *Cacheable bit* (SCR(13)) indicates whether the access is cacheable or not when the MMU is disabled. This bit is set to 1 if accesses on the physical bus (with the MMU disabled) are to be considered cacheable.

BM. *Boot-mode bit* (SCR(14)) indicates the system is in boot mode. This bit is set to 1 to indicate boot mode and is automatically set upon power-on reset.

MCA(1:0). *Multichip address field* (SCR(23:22)) provides the address field in multichip configuration. For more information, refer to the CY7C604 Multichip Configuration section in the SPARC RISC User's Manual.

MCM(1:0). *Multichip mask field* (SCR(21:20)) provides a masking facility to mask certain multichip address (MCA) bits in order to provide a facility to build systems with a different number of CY7C604s (from 1 to 4).

MV. *Multichip configuration valid bit* (SCR(19)) indicates that the MCA and MCM fields are valid.

NF. *No-fault bit* (SCR(1)) prevents supervisor data accesses from signaling data faults to the CY7C601. When the NF bit is set, exception-generating logic (in both the TLB and the table walk) does not indicate supervisor data faults to the CY7C601 (via $\overline{\text{MEXC}}$), but status and address information is recorded in the SFSR and SFAR registers as in normal data access operations. When the NF bit is not set, the CY7C604 reports the supervisor data exceptions.

ME. *MMU-enable bit* (SCR(0)) indicates whether the MMU is enabled or not. This bit is set to 1 to enable the MMU.

7

The implementation number (SCR(31:28)) and the version number (SCR(27:24)) fields are hardwired; they are read only fields and writes to those fields are ignored.

Implementation number field: 0001
Version number field: 0000

On power-on reset, all writeable control bits except the BM bit are cleared. This sets the CY7C604 into the following state: cache disabled (CE = 0), cache unlocked (CL = 0), write-through mode (CM = 0), non-cacheable (C = 0), boot-mode enabled (BM = 1), multichip disabled (MV = 0), no fault disabled (NF = 0), and MMU disabled (ME = 0).

IMPL	VER	MCA	MCM	MV	RS V	BM	C	RSV	CM	CL	CE	RSV	NF	ME
31 28	27 24	23 22	21 20	19	18 15	14	13	12 11	10	9	8	7 2	1	0

IMPL = Specific Implementation of the MMU
VER = Version of Specific Implementation (typically mask revision)
MCA (0:1) = Multichip Address
MCM (0:1) = Multichip Mask
MV = Multichip Valid
BM = Boot Mode
C = Cacheable (when MMU disabled)
CM = Cache Mode
CL = Cache Lock
CE = Cache Enable
NF = No Fault
ME = MMU Enable
RSV = Reserved

Figure 2. System Control Register (SCR)

Context Table Pointer Register (CTPR)

The context table pointer points to the context table in physical memory. The table is indexed by the contents of the context register. The context table pointer appears on bits 35 through 14 of the Mbus (MAD(35:14)) during the first fetch of TLB miss processing. Once the root pointer is cached in the PTPC (page table pointer cache), no fetching of the root pointer is required until the context is changed (see *Figure 3).*

CTP	RSV
31 … 10	9 … 0

CTP = Context Table Pointer
RSV = Reserved

Figure 3. Context Table Pointer Register

Context Register (CXR)

The context register defines a virtual address space associated with the current process. The CXR is a twelve bit register that supports 4096 contexts. This register is used to define the current context for the CY7C604. Nearly all CY7C604 operations are dependent upon matching the value of this register to a cache tag entry or TLB entry.

RSV	CXN
31 … 12	11 … 0

CXN = Context Number
RSV = Reserved

Figure 4. Context Register

Reset Register (RR)

The RR register contains information regarding whether Watch Dog Reset (WDR), Software Internal Reset (SIR) or Software External Reset (SER) occurred. This is a read/write register, and setting the software internal reset bit (SIR) or the software external reset (SER) causes the corresponding reset. On power-on reset, the WDR, SIR, and SER bits in the RR will be cleared. Reading the RR will also clear these bits.

RSV	WDR	SIR	SER
31 … 3	2	1	0

RSV = Reserved
WDR = Watchdog Reset
SIR = Software Internal Reset
SER = Software External Reset

Figure 5. Reset Register

Root Pointer Register (RPR)

The RPR is the context level table Page Table Pointer (PTP) and is cached in the page table pointer cache.

RP	RSV	V
31 … 6	5 … 1	0

RP = Root Pointer
RSV = Reserved
V = Valid

Figure 6. Root Pointer Register

On power-on reset, the V bit is cleared. When the current context is changed by writing to the Context Pointer Register (CXR), the V bit of the RPR is cleared. The V bit is also cleared when the CTPR register is written.

Instruction access PTP (IPTP)

The IPTP is the instruction access level 2 table Page Table Pointer (PTP) and is part of the page table pointer cache. On power-on reset, the V bit is cleared.

IPTP	RSV	V
31 … 4	3 … 1	0

IPTP = Instruction Access PTP
RSV = Reserved
V = Valid

Figure 7. Instruction Access PTP Register

Data access PTP (DPTP)

The DPTP is the data access level 2 table Page Table Pointer (PTP) and is a register in the page table pointer cache. On power-on reset, the V bit is cleared.

DPTP	RSV	v
31 … 4	3 … 1	0

DPTP = Data Access PTP
RSV = Reserved
V = Valid

Figure 8. Data Access PTP Register

Index Tag Register (ITR)

The ITR contains the tag (index1 and index2) fields of the IPTP and DPTP entries.

ITAG	RSV	DTAG	RSV
31 … 18	17 16	15 … 2	1 0

RSV = Reserved
ITAG = Instruction Access PTP Tag
DTAG = Data Access PTP Tag

Figure 9. Index Tag Register

TLB Replacement Control Register (TRCR)

The TRCR contains the Replacement Counter (RC) and Initial Replacement Counter (IRC) fields as shown in *Figure 10.* These fields are used in order to support random replacement and to support locking capabilities of the TLB. On power-on reset, both the RC and IRC fields are initialized to zero.

RSV	RC	RSV	IRC
31–14	13–8	7–6	5–0

RSV = Reserved
RC = Replacement Counter
IRC = Initial Replacement Counter

Figure 10. TLB Replacement Control Register

Synchronous Fault Status Register (SFSR)

The synchronous fault status register, illustrated in *Figure 11*, contains fault-associated information for synchronous faults. Synchronous faults are faults that occur during an integer unit access of memory. Synchronous faults include almost all possible faults for the CY7C604. This type of fault is synchronous to the operations of the CY7C601. For the CY7C604, this fault type covers all cases except those caused by delayed writes of data stored in the write buffers. These faults are asynchronous to the operation of the CY7C601, and are named asynchronous faults.

An example of a synchronous fault is a privilege violation fault caused by attempting an unauthorized memory access. Upon encountering a synchronous fault, the CY7C604 asserts the $\overline{\text{MEXC}}$ signal, along with $\overline{\text{MHOLD}}$ and $\overline{\text{MDS}}$. Synchronous faults are the only exception type that assert the $\overline{\text{MEXC}}$ signal.

The CBT bit indicates that a translation error occurred during a table walk for the flush of a modified cache line of a copy-back mode cache miss. The SFAR will contain the address of the missed cache access, not the modified cache line address causing the translation error. When this type of error occurs, the cache tag remains valid, and the cache line remains modified.

The Uncorrectable Error (UE), Timeout Error (TO), and Bus Error bits (BE) report error status as encoded in the $\overline{\text{MERR}}$, $\overline{\text{MRTY}}$, and $\overline{\text{MRDY}}$ signals. (Refer to the section on Mbus for further information.) The level bits (L) describe the level in a table walk process at which the fault occurred (if applicable).

RSV	CBT	UC	TO	BE	L	AT	FT	FAV	OW
31–14	13	12	11	10	9–8	7–5	4–2	1	0

RSV = Reserved
UC = Uncorrectable Error
TO = Time Out Error
BE = Bus Error
CBT = Copy-back Translation Error
L = Level
AT = Access Type
FT = Fault Type
FV = Fault Address Valid
OW = Over Write

Figure 11. Synchronous Fault Status Register

The access type bits (AT(2:0)) describes the access type that caused the fault. This field specifies user/supervisor access and whether the access is load or store of data or instruction. The Fault-Type bits (FT) describe the fault type. The fault address valid bit is set when the address in the Synchronous Fault Address Register (SFAR) is a valid fault address. The Over-Write bit (OW) is set in the case of a double fault where the fault status stored in the SFSR does not correspond with the fault first trapped on by the CY7C601.

Synchronous Fault Address Register (SFAR)

The synchronous fault address register contains the faulted virtual address.

SFA
31–0

SFA = Synchronous Fault Address

Figure 12. Synchronous Falut Address Registers

Asynchronous Fault Status Register (AFSR)

Asynchronous faults are those faults caused by a delayed memory access initiated by the CY7C604. This type of error can only be caused by a delayed write to main memory initiated by the write buffer. Asynchronous faults cause the $\overline{\text{CMER}}$ signal to be asserted, which can be used as an interrupt to the CY7C601.

The UC, TO, and BE bits are identical to those in the SFSR. They are set by the information encoded into the $\overline{\text{MERR}}$, $\overline{\text{MRTY}}$, and $\overline{\text{MRDY}}$ signals of the Mbus. The asynchronous fault address bits provide the upper four bits of the physical address not captured in the Asynchronous Fault Address Register (AFAR), which is a thirty-two bit register.

RSV	UC	TO	BE	RSV	AFA(35:32)	RSV	AFO
31–13	12	11	10	9–8	7–4	3–1	0

RSV = Reserved
UC = Uncorrectable Error
TO = Time Out Error
BE = Bus Error
AFA = Asynchronous Fault Address
AFO = Asynchronous Fault Occurred

Figure 13. Asynchronous Falut Status Register

The Asynchronous Fault Occurred bit (AFO) is set when an asynchronous fault is encountered. Once the Asynchronous Fault Occurred (AFO) bit is set, no further asynchronous faults are recorded until the AFO bit is cleared, which is accomplished by reading the asynchronous fault address register (see *Figure 13).* On power-on reset, the UC, TO, BE, and AFO bits in the AFSR will be cleared. Reading the AFSR will also clear these bits.

Asynchronous Fault Address Register (AFAR)

The AFAR contains bits 31 - 0 of the physical address for a asynchronous faults (bus errors). Asynchronous faults can occur during delayed write accesses or during background cache line flush operations in copy-back mode (see *Figure 14).* The address in the AFAR is concatenated with the four AFA bits in the AFSR to define the entire 36-bit physical address.

AFA
31–0

AFA = Asynchronous Fault Address

Figure 14. Asynchronous Fault Address Register

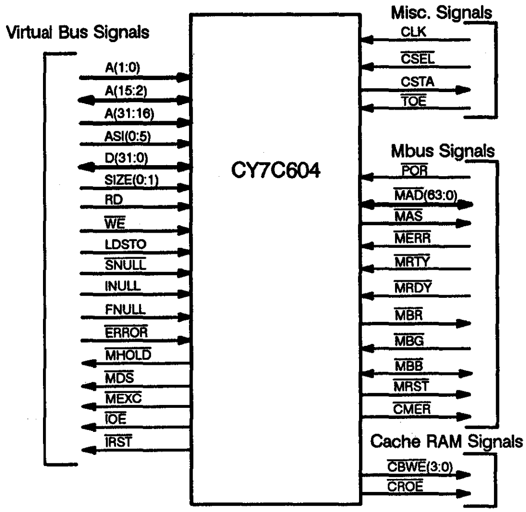


Figure 15. CY7C604 Pin Configuration

Pin Definitions

The functional pinout is shown in *Figure 15*. Note that all three-state output signals are driven to their inactive state before they are released to three-state.

Virtual Bus Signals

Signal Name	I/O	Description
A(31:16)	I	Virtual Address bus. A(31:16) are input signals during normal read/write accesses and are latched into the CY7C604 on the rising edge of clock.
A(15:2)	I/O	Virtual Address bus. Three-state input/output signals. A(15:2) are input signals during normal read/write accesses and are latched into the CY7C604 on the rising edge of the clock. They are output signals during cache line loads into the cache RAM and modified cache-line reads from the cache RAM.
A(1:0)	I	Virtual Address bus. A(1:0) are input signals during normal read/write accesses and are latched on the rising edge of clock.
ASI(5:0)	I	Address Space Identifiers. The ASI bits are used to: 1. Identify various types of accesses (user/supervisor, instruction/data) 2. Access CY7C604 registers 3. Initiate MMU flush/probe operation 4. Identify cache flush operations 5. Recognize diagnostic operations 6. Recognize pass physical address space

Virtual Bus Signals (continued)

Signal Name	I/O	Description
D(31:0)	I/O	Virtual Data bus. Three-state input/output signals. D(31:0) are input signals during CY7C601 normal write accesses, modified cache-line reads from the cache RAM, CY7C604 register writes or CY7C604 diagnostic accesses. They are output signals during cache line loads into cache RAM, CY7C604 register reads or CY7C604 diagnostic accesses.
$\overline{\text{ERROR}}$	I	Error (active low) signal from the CY7C601. When this signal is asserted, it indicates the CY7C601 has halted due to entering the error state. The CY7C604 reads this signal and initiates a watchdog reset.
FNULL	I	Floating point unit NULLification cycle (active high). When FNULL is active, the current access will be ignored.
INULL	I	Integer unit NULLification cycle (active high). When INULL is active, the current access will be ignored.
$\overline{\text{IOE}}$	O	Integer unit Output Enable (active low). This signal is continually driven high or low. This signal is connected to the $\overline{\text{AOE}}$ and $\overline{\text{DOE}}$ inputs of the CY7C601. When asserted, the $\overline{\text{IOE}}$ will place the address (A(31:0)), address space identifiers (ASI(7:0)), and data (D(31:0)) drivers of the CY7C601 in a three-state condition.
$\overline{\text{IRST}}$	O	Integer unit Reset (active low) is asserted to reset integer unit. This signal is continually driven high or low.
LDSTO	I	Load Store Atomic operation indicator (active high). Asserted by the CY7C601 during atomic load store cycles and is sampled by the CY7C604 on the rising edge of the clock.
$\overline{\text{MDS}}$	O	Memory Data Strobe (active low) is asserted for one clock to strobe data into the CY7C601 during a cache miss. $\overline{\text{MHOLD}}$ must be low when $\overline{\text{MDS}}$ is asserted. It is driven off of the falling edge of the clock. This is a three-state output.
$\overline{\text{MEXC}}$	O	Memory Exception (active low) is asserted for one clock whenever a privilege or protection violation is detected. $\overline{\text{MHOLD}}$ and $\overline{\text{MDS}}$ must be low when $\overline{\text{MEXC}}$ is asserted. This is a three-state output.
$\overline{\text{MHOLD}}$	O	Memory Hold (active low) is asserted by the CY7C604 whenever it requires additional time to complete the current access such as during cache miss etc. It is driven off of the falling edge of the clock.

Virtual Bus Signals (continued)

Signal Name	I/O	Description
RD	I	Read cycle indicator (active high). Asserted by the CY7C601 during read cycles and is sampled by the CY7C604 on the rising edge of the clock. This signal is also used to generate cache output enable ($\overline{\text{CROE}}$).
SIZE(1:0)	I	SIZE of access indicator. Specifies the data width of the CY7C601 access and is sampled by the CY7C604 at the rising edge of the clock.
SNULL	I	System NULLification cycle (active high). When $\overline{\text{SNULL}}$ is active, the current access will be ignored.
$\overline{\text{WE}}$	I	Write Enable to indicate write cycle (active low). Asserted by the CY7C601 during write cycles and is sampled by the CY7C604 on the rising edge of the clock. This signal is also used to generate cache byte write enables ($\overline{\text{CBWE}}$(3:0)).

Mbus Signals

Signal Name	I/O	Description
$\overline{\text{CMER}}$	O	CMU Error (active low). This signal is asserted if any bus error has occurred during writes to main memory. A system can use this signal to cause an interrupt. This signal has the same timing specifications as the Mbus control signals and asserted for one clock. This signal is constantly driven.
MAD (63:0)	I/O	Mbus Address and Data (three-stated bus). During the address phase of a transaction MAD(35:0) contains the physical address PA(35:0). The remaining signals MAD(63:36) during the address phase of the transaction contains the transaction associated information as shown below: MAD(39:36) — Transaction Type 0 H — Mbus write 1 H — Mbus read 2-F H — Reserved MAD(42:40) — Transaction Size 0 — Byte (8 bits) 1 — Halfword (16 bits) 2 — Word (32 bits) 3 — Doubleword (64bits) 4 — 16 Bytes* 5 — 32 Bytes 6 — 64 Bytes* 7 — 128 Bytes* * Not supported by the CY7C604. MAD(43) (MC) Mbus Cacheable (active high). Indicates the current Mbus transaction is cacheable.

Mbus Signals (continued)

Signal Name	I/O	Description
		MAD(45) (MBL) Mbus Boot Mode/Local indicator. MBL is high during the address phase of boot mode transactions. The instruction fetch and data accesses to the Mbus while the MMU is disabled in boot mode are considered BOOT MODE transactions. The data transactions on the Mbus required for Load/Store Alternate instructions with ASI = 1 are considered LOCAL transactions. MAD(63:46) Reserved during address phase (Driven high). During the data phase of the transaction the MAD(63:0) lines contain the 64 bits of data being transferred.
$\overline{\text{MAS}}$	O	Mbus Address Strobe (active low). Asserted by the bus master during the first cycle of every bus transaction to indicate the address phase of that transaction. This is a three-state output.
$\overline{\text{MBB}}$	I/O	Mbus Bus Busy (active low). Asserted by the current Mbus master during an entire transaction and, if required, during both the read and write transactions of indivisible accesses. The potential bus master devices sample $\overline{\text{MBB}}$ in order to obtain bus mastership as soon as the current master releases the bus. This is a three-state output.
$\overline{\text{MBG}}$	I	Mbus Bus Grant (active low). Asserted by external arbiter when the Mbus is granted to a master. This signal is continually driven.
$\overline{\text{MBR}}$	O	Mbus Bus Request (active low). Asserted by potential Mbus master devices to acquire bus mastership. This signal is continually driven.
$\overline{\text{MERR}}$	I	Mbus Error (active low). Asserted or deasserted by an Mbus slave during every data phase of a transaction. This signal is to be three-stated when released.
$\overline{\text{MRDY}}$	I	Mbus Ready (active low). Asserted or deasserted by an Mbus slave during every data phase of a transaction. This signal is to be three-stated when released.
$\overline{\text{MRST}}$	O	Mbus Reset (active low). Asserted for 1024 clock cycles by only one source on the Mbus to initialize all devices on the Mbus. This signal is continually driven.
$\overline{\text{MRTY}}$	I	Mbus Retry (active low). Asserted or deasserted by an Mbus slave during every data phase of a transaction. This signal is to be three-stated when released.

7

Mbus Signals (continued)

Signal Name	I/O	Description
		MERR MRDY MRTY Action H H H Nothing H H L Relinquish and Retry* H L H Data Strobe H L L Reserved L H H Bus Error L H L Time Out L L H Uncorrectable Error L L L Retry* * See section on Physical Bus (Mbus)
POR	I	Power-On Reset (active low). The POR initializes all on-chip logic to a known state, invalidates all the TLB entries, and all cache tag entries. It must be asserted for a minimum of 8 clocks. It also causes the CY7C604 to assert IRST to reset the CY7C601.

Cache RAM Signals

Signal Name	I/O	Description
CBWE (3:0)	O	Cache Byte Write Enables (active low). During normal write operations, certain byte enable signals are asserted depending upon the size and A(1:0) inputs. During a cache line load all four byte enable signals are asserted. These signals can also be driven by using a store alternate instruction with ASI = F H. This feature is supported for diagnostic purposes. This output is continually driven (not three-stated). CBWE0 controls the most significant byte (MSB) and CBWE3 controls the least significant byte (LSB).
CROE	O	Cache RAM Output Enable (active low). Asserted during normal read operations with ASI = 8, 9, A, B and during modified cache line read operations. This signal is also asserted during cache data read operations with ASI = F for diagnostic purposes. This signal is continually driven.

Miscellaneous Signals

Signal Name	I/O	Description
CLK	I	System Clock. This is the same clock used by the 7C601 integer unit.
CSEL	I	Chip Select (active low). In multi-CMU systems, CSEL on each CY7C604 is connected to different address lines (any one from A(31:16)) to initialize the multichip configuration. In single-CMU systems, CSEL should be connected to ground in order to permanently enable the CY7C604. In multi-CMU systems, CSEL should be connected to ground or VCC through a resistor during Power-On Reset. This is required in order to enable only one boot mode CMU.
CSTA	O	Cache Status. This pin provides the status of cache. In write-through, the CSTA indicates whether the write transaction on the Mbus has cache hit or not. For read transaction on the Mbus in either write-through or copy-back mode, the CSTA indicates whether it is replacing a valid cache line entry or not. This signal has the same timing specifications as the Mbus signals such as MC and has meaning only in the address phase of Mbus transactions. This signal is continually driven high or low.

CACHE MODE	CSTA	CONDITION
Write-through	1	read and valid cache line replacement
	0	read and invalid cache line replacement
	1	write and cache hit
	0	write and cache miss
Copy-back	1	read and valid cache line replacement
	0	read and invalid cache line replacement
	undef.	write

Signal Name	I/O	Description
TOE	I	Test Output Enable (active low). This signal is used (when high) to three-state all output drivers of the CY7C604. TOE SHOULD BE TIED LOW DURING NORMAL OPERATION. It is used to isolate the CY7C604 from the rest of the system for debugging purposes.

CYPRESS SEMICONDUCTOR

CY7C605 Cache Controller and Memory Management Unit

Features

- Multiprocessing support
- Pin-compatible with CY7C604
- Cache coherency protocol modeled after IEEE Futurebus
- Separate virtual and physical cache tag memories
  - Each cache tag memory holds 2048 cache entries
  - Allows concurrent bus snooping without stalling processor
- Large address space support
  - 32-bit virtual address
  - 36-bit physical address
- 32-byte cache line size
- Byte write generation
- Write-through and copy-back cache policies
- 32-byte read line buffer
- 32-byte copy-back write line buffer
- 32-byte write-through buffer
- Fully conforms to SPARC Reference Mbus Level-2 specification
- Fully conforms to the SPARC reference Memory Management Unit (MMU) architecture
- On-chip Translation Lookaside Buffer (TLB)
  - 64 fully associative entries
  - Multi-level TLB flush
  - TLB probe support
  - Lockable entries
  - Random TLB replacement
  - Supports multi-level address mapping (4-kbyte, 256-kbyte, 16-Mbyte, and 4-Gbyte).
- Supports context switching
  - 4096 contexts for TLB entries
  - 4096 contexts for cache tag
- Page-level memory access protection
  - Read/Write/Execute
  - User/Supervisor modes
- Hardware table walk
- 0.8-micron CMOS technology

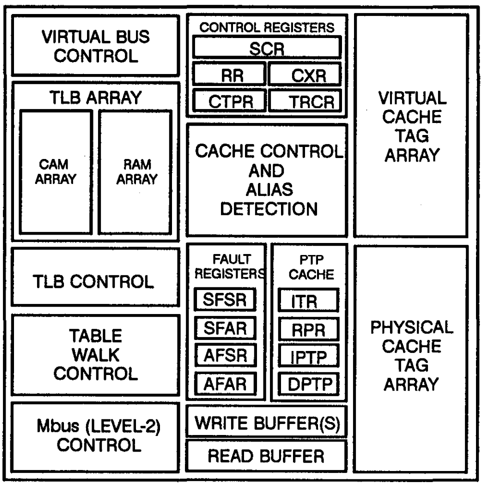
Description

The CY7C605 is a combined cache controller and memory management unit optimized for multiprocessing systems. It is a high-speed CMOS implementation of the SPARC® reference memory management architecture, combined with a cache memory controller and on-chip virtual and physical cache tag memories. The CY7C605 supports the SPARC reference Mbus level-2 protocol for multiprocessing systems.

The CY7C605 is a functional superset of the CY7C604, and is pin-compatible to the CY7C604. The CY7C605 directly connects to the CY7C601 integer unit microprocessor and CY7C157 cache data RAM without any external circuitry. When combined with two CY7C157 16-kbyte x 16 cache RAMs, the CY7C605 forms a complete, no wait-state, 64-kbyte direct mapped virtual cache system.

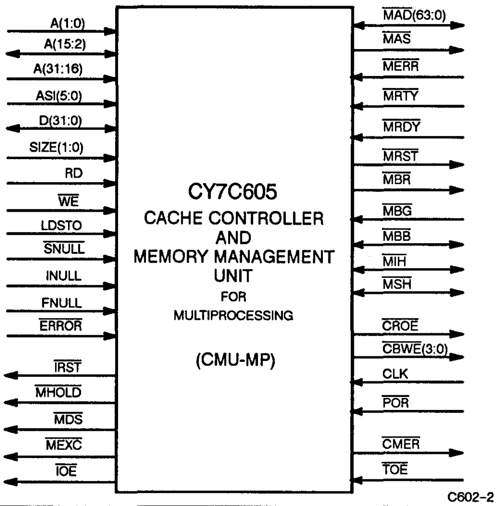
7

Logic Block Diagram



C602–1

Pin Configuration



C602–2

Selection Guide

		7C605-40	7C605-33	7C605-25
Maximum Supply Current (mA)	Commercial	650	600	600
	Military			650

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Functional Description

The CY7C605 represents the evolution of the Cypress CY7C600 family into the realm of multiprocessing. The CY7C605 is a combined memory management unit (MMU) and cache controller with on-chip cache tag memory. A superset of the CY7C604, the CY7C605 is designed to support the requirements of multiprocessing systems. The CY7C605 provides two separate cache tag memories as compared to the single cache tag memory used on the CY7C604. The second cache tag memory allows concurrent bus snooping without stalling the CY7C601. This allows the CY7C605 to maintain cache coherency with other cache systems without degrading CPU performance. The CY7C605 supports the Mbus cache coherency protocol, which is modeled after the acclaimed IEEE Futurebus. The CY7C605 is pin-compatible with the CY7C604. This allows a CY7C604-based CPU to be used in a multiprocessor system by substituting the CY7C605.

The CY7C605 is designed as part of a system solution for high-performance multiprocessor computing using the Cypress SPARC chip set. This chip set consists of the CY7C601 integer unit, the CY7C602 floating-point unit, the CY7C605 CMU, and two CY7C157 cache RAMs. The Cypress SPARC chip set comprises a five chip, high-performance CPU requiring no additional glue logic. As part of this chip set, the CY7C605 provides support for large addressing spaces with virtual to physical address translation, and provides control for a 64-kbyte virtual cache. As part of a multiprocessor system, the CY7C605 automatically maintains cache coherency with other multiprocessor CPUs sharing a common memory system.

The MMU portion of the CY7C605 provides translation from a 32-bit virtual address range (4 gigabytes) to a 36-bit physical address (64 gigabytes), as provided in the SPARC reference MMU specification. Virtual address translation is further extended with the use of a context register, which is used to identify up to 4096 contexts or tasks. The cache tag entries and TLB entries contain context numbers to identify tasks or processes. This minimizes unnecessary cache tag and TLB entry replacement during task switching.

The MMU features a 64-entry Translation Lookaside Buffer (TLB). The TLB acts as a cache for address mapping entries used by the MMU to map a virtual address to a physical address. These mapping entries, referred to as page table entries or PTEs, allow one of four levels of address mapping. A PTE can be defined as the address mapping for a single 4-kbyte page, a 256-kbyte region, a 16-Mbyte region, or a 4-Gbyte region. The TLB entries are lockable, allowing important TLB entries to be excluded from replacement.

The MMU performs its address translation task by comparing a virtual address supplied by the CY7C601 (integer unit) to the address tags in the TLB entries. If the virtual address and the value of the context register match a valid TLB entry, a TLB "hit" occurs. When this occurs, the physical address stored in the TLB is used to translate the virtual address to a physical address. The access type (read/write of data or instruction) and privilege level (user/supervisor) are checked during translation. If a TLB hit occurs but access level protection is violated, the MMU signals an exception and the operation ends.

If the virtual address or context does not match any valid TLB entry, a TLB "miss" occurs. This causes a table walk to be performed by the MMU. The table walk is a search performed by the MMU through the address translation tables stored in main memory. The MMU searches through several levels of tables for the PTE corresponding to the virtual address. Upon finding the PTE, the MMU translates the address and selects a TLB entry for replacement, where it then stores the PTE.

The 64-kbyte virtual cache is organized into 2048 lines of 32 bytes each. The term "virtual cache" refers to the direct addressing of the cache by the integer unit (CY7C601) with the virtual address bus. Virtual address bits (VA(15:5)) select the cache line, and virtual address bits (VA(4:2)) select the 32-bit word of the cache line, as illustrated in *Figure 1*. The cache line selected by (VA(15:5)) is associated with a cache tag entry for that cache line. The CY7C605 provides access control for the cache by checking the context and virtual address against the cache tag for the selected cache line. If the virtual address, access level, and context match the validated cache tag for the cache line addressed, a cache hit occurs and the access is enabled. If the virtual address or context do not match the cache tag, or if the cache tag entry has been invalidated, a cache miss occurs and the cache controller accesses main memory for the required data.

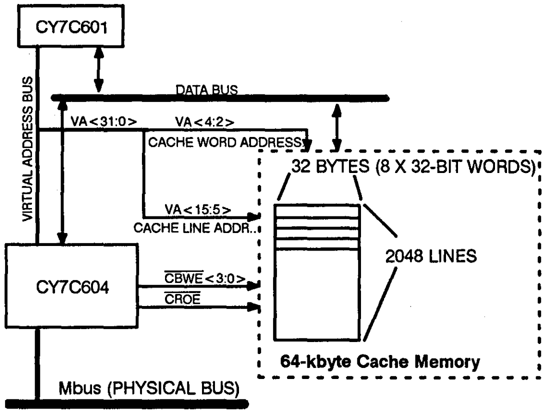


Figure 1. Virtual 64-kbyte Cache

The cache controller supports two modes of caching: write-through with no write allocate and copy-back with write allocate. The difference between the two caching modes is in how they handle write accesses to the cache. Write-through mode causes write accesses to the cache to be written through to both cache and main memory upon each write access. Copy-back cache mode causes write accesses to be written to the cache only, which causes the caches lines to become modified with respect to main memory. Modified cache lines are automatically written back to main memory only when the cache line is no longer needed.

Write-through has the disadvantage that each write to the cache increases traffic on the system bus. This disadvantage becomes of increasing importance as multiple processors contend for memory bus bandwidth. Write-through also has the disadvantage that the processor is delayed by the time required to arbitrate the system bus and write the data to main memory. However, in the case of the CY7C605, this disadvantage is largely offset by the inclusion of write buffers. The write buffers can store up to four double-word accesses, allowing the CY7C601 to continue execution while data is written to main memory.

Copy-back caching has long been recognized as providing higher system performance than write-through. Blocks of write accesses (typically occurring in context switching or data intensive operations) cause a write-through cache system to stall the processor even with the inclusion of write buffers. This is a problem inherent with write-through that is avoided by copy-back caching mode. However, copy-back caching in multiprocessing systems introduces the issue of data consistency. Since copy-back holds modified data until the processor no longer requires the data, main memory becomes inconsistent with the contents of the cache.

Cache coherency protocols have been established to deal with the data consistency problem, but many cache designs have avoided copy-back caching due to the complexity of implementing the protocol. The CY7C605 solves the problems of supporting cache consistency protocols and provides the multiprocessor designer with the performance of a true copy-back cache system The CY7C605 supports a cache coherency protocol modeled after the IEEE Futurebus, which has been acclaimed in the industry as a superior cache protocol. To support this protocol, the CY7C605 utilizes a dual cache tag memory to allow concurrent bus snooping. This enables the CY7C605 to monitor all bus activity without stalling the processor. The CY7C605 uses the bus activity information to maintain cache coherency, which it does automatically as a concurrent task without interfering with the cache operations for the processor. Therefore, the CY7C605 provides a multiprocessing system a maximum performance copy-back cache without the problems of supporting a cache coherency protocol.

A 32-byte write buffer and a 32-byte read buffer are provided in the CY7C605 to fully buffer the transfer of a cache line. This feature is used in copy-back cache mode to allow the CY7C605 to simultaneously read a cache line from main memory as it is flushing a modified cache line from the cache. This feature is also used in write-through cache mode for write accesses to main memory. The write buffer avoids stalling the CY7C601 on writes to main memory by storing the write data until the physical bus becomes available. The write buffer then writes the data to memory as a background task.

The CY7C605 supports the SPARC Mbus standard bus interface. The Mbus is a peer level, high-speed, 64-bit, multiplexed address and data bus which supports a full peer level protocol (i.e., multiple bus masters). The Mbus transfers data in transaction sizes from 1 to 128 bytes. These data transfers are performed in either burst or non-burst mode, depending upon size. Data transactions larger than eight bytes (one doubleword) are transferred in burst mode, which consists of an address phase followed by multiple data phases. Non-burst transactions consist of an address phase followed by one data phase, and are used for data transactions less than eight bytes. Bus mastership is granted and controlled by an external bus arbiter. The bus arbiter sets bus priorities, and grants access to a bus master.

Mbus is divided into two levels of implementation: level-1 and level-2. Level-1, implemented on the CY7C604, is the uniprocessor version of Mbus. Level-1 is a subset of level-2, which is the multiprocessor version of Mbus. The CY7C605 supports level-2 Mbus. Level-2 Mbus includes the IEEE Futurebus cache coherency protocol, which has been recognized in the industry as a superior method of supporting multiprocessing systems.

The level-2 Mbus supports direct data intervention, which allows a cache system with the up-to-date version of a cache line to directly supply the data to another cache system without having to first update main memory. Direct data intervention provides a significant performance improvement over systems which do not support this feature. In addition, the CY7C605 provides support for memory systems with reflective memory controllers. A memory system with reflective memory control can recognize a cache to cache data transaction and automatically update itself without delaying the system. Secondary cache controllers are also supported by the CY7C605, which provide a performance advantage over systems directly using main memory.

Memory Management Unit

The MMU provides virtual to physical address translation with the use of an on-chip Translation Lookaside Buffer (TLB). The translation lookaside buffer is in reality a full Address Translation Cache (ATC) for address translation entries stored from tables in main memory. These entries, referred to as page table entries or PTEs, contain the mapping information used by the MMU to translate the virtual addresses. Addresses presented to the MMU for translation are compared against the set of PTEs stored in the TLB. All entries in the TLB are simultaneously accessed through the use of advanced Content Addressable Memory (CAM) technology. If a match for the virtual address and context is found in a valid TLB entry and the access protection is not violated, a TLB hit occurs and the address is translated. A virtual address and context that matches a valid TLB entry but violates the memory access protections will cause the CY7C605 to generate a memory exception to the CY7C601. If the TLB entries do not match the address and context, or the TLB entry is invalid, then a TLB miss occurs. The MMU responds to the TLB miss by initiating a table walk to find the correct PTE stored in main memory for the virtual address.

7

The MMU uses a tree-structured table walk algorithm to find page table entries not found in the TLB. The table walk is a search through a series of tables in main memory for the PTE corresponding to a virtual address. The table walk uses a series of four tables. These tables are: the context table, the level 1 table, the level 2 table, and the level 3 table. The table walk uses the context pointer register as a base register and the context number as a offset to point to an entry in the context table. At any address, the MMU finds either a PTE, which terminates its search, or a page table pointer (PTP). A PTP is a pointer used in conjunction with a field in the virtual address to select an entry in the next level of tables. The table walk continues searching through levels of tables as long as PTPs are found pointing to the next table. The table walk terminates when a PTE is found, or an exception is generated if a PTE is not found after accessing the level 3 table. An exception is also generated if the table walk finds an invalid or reserved entry in the page tables.

Upon finding the PTE, the CY7C605 stores it in an available TLB entry and translates the corresponding virtual address. The tablewalk processing is implemented in the CY7C605 hardware. It is self-initiated, and is transparent to the user.

Cache Controller

The cache controller provides cache memory access control for a 64-kbyte direct mapped virtual cache. The cache controller performs this task by comparing memory accesses against the address and status entries in a cache tag memory. The CY7C605 provides two separate cache tag memories for access comparison. Cache memory accesses from the processor are compared against the Processor Virtual cache TAG (PVTAG) memory. Bus snooping operations are compared against the Mbus Physical cache TAG (MPTAG) memory. The use of two cache tag memories allows the cache controller to service processor cache accesses concurrently with bus snooping cache tag accesses. This feature of the CY7C605 provides significant performance improvements over cache systems sharing a single cache tag memory between the processor cache access and the bus snooping operations. Single cache tag systems typically must stall the processor when a bus snooping operation is required, causing serious performance degradation.

The cache controller is designed to use two CY7C157 cache RAMs for the cache memory. These cache RAMs are 16-kbyte x 16 SRAMs with on-chip address and data latches and timing control. Two CY7C157s and one CY7C605 comprise an entire 64-kbyte cache system with physical bus interface and read and write buffers.

The cache is organized as 2048 cache lines of 32 bytes each. The CY7C605 has 2048 cache tag entries in both the PVTAG and MPTAG, one entry in each cache tag memory per cache line. Addressing for the virtual cache is provided directly from the virtual address bus. The virtual address field (VA(15:5)) selects one of the 2048 lines of the cache. This address field also selects the cache tag entry in the PVTAG dedicated to the selected cache line. A cache hit occurs when the upper sixteen bits of the virtual address and the context register match with the virtual address and context stored in the selected cache tag entry in PVTAG. The lowest five bits of the virtual address bus (VA(4:0)) select one of the 32 bytes in the cache line. Cache data replacement is always performed by replacing cache lines.

The cache is designed to provide data with every read access asserted on the virtual bus, regardless of the cache controller. The CY7C605 controls cache read access by halting the CY7C601 if a cache hit is not detected by the cache controller. The cache controller then reads the new cache line from main memory, and supplies the correct data to the CY7C601. After the correct data is latched into the CY7C601 by strobing the $\overline{\text{MDS}}$ signal, the CY7C601 is released and execution proceeds normally.

Writes to the cache are controlled by the CY7C605, which decodes the lowest two bits of the virtual address, the SIZE(1:0) signal, and checks for a cache hit to enable the correct cache byte write enable signals. If a cache write hit occurs, the CY7C605 decodes the correct $\overline{\text{CBWE}}$ signals for the write access, and outputs these to the CY7C157 cache RAM write enables. If the cache mode is set to write-through (see Cache Modes), the write data is also written to main memory. If a write cache miss occurs for write-through cache mode, the data is written to main memory and the cache is not updated. If the write cache miss occurs during copy-back cache mode (see Cache Modes), the cache line is fetched from main memory. If the cache line stored in the cache when the write cache miss occurred has been modified, the old cache line is written to main memory before the cache line is replaced by the new data. After the cache line has been replaced, the write access is enabled by the CY7C605.

Cache Tag

The CY7C605 features two separate cache tag arrays: the processor virtual cache tag memory (PVTAG) and the Mbus physical cache tag memory (MPTAG). Cache controllers using only one cache tag array must delay the processor when bus snooping requires access to the cache tags. The inclusion of two independent cache tag memories allows the CY7C605 to support processor accesses to cache while simultaneously performing bus snooping on the Mbus.

Cache Modes

The cache can be programmed for either write-through with no write allocate or copy-back with write allocate. The two cache modes differ in how they treat cache write accesses. Write-through cache mode causes write hits to the cache to be written to both cache and main memory. Write-through write cache misses will only update main memory and invalidate the cache tag, but will not modify the cache.

A write access in copy-back mode will modify the cache only. The writing of the modified cache line to main memory is deferred until the cache line is no longer required. Copy-back cache mode has the advantage of reducing traffic on the system bus. Bus traffic is reduced since all updates to memory are deferred and are subsequently performed only as absolutely required. In addition, all such data transfers are made utilizing the more efficient burst mode. The following describes the two cache modes in detail.

Write-through mode with no Write Allocate

For write-through cache mode, write access cache hits cause both the cache and main memory to be updated simultaneously. A write access cache miss causes only main memory to be updated (no write allocate). The selected cache line is invalidated for a write access cache miss. Write-through caching mode normally requires a processor to delay during a write miss while the data is written to main memory. The CY7C605 provides write buffers to prevent this delay in most cases. The write buffers store the write access and write the data to main memory as a background task.

During read access cache hits, the cached data is read out and supplied to the CY7C601. In the case of a read access cache miss, a cache line is fetched from main memory to load into the cache and the required data is supplied to the CY7C601.

Copy-back mode with Write Allocate

When the cache is configured for copy-back mode, only the cache is updated on write access cache hits (i.e., main memory is not updated). The modified bit of the cache tag for the cache line is set on a copy-back write access (write hit or after a write miss is corrected). During write access cache misses, if the selected cache line is clean (not modified), a cache line is fetched from main memory to load into the cache and only the cache is updated. If the selected cache line is modified, the selected cache line is flushed out to update main memory. The CY7C605 simultaneously fetches the new cache line from main memory and stores it into the read buffer as it flushes the modified cache line from the cache and stores it into its write buffer. After the modified cache line has been flushed, the CY7C605 writes the modified cache line out of its write buffer into main memory while the new cache line is stored into the cache memory from the read buffer.

During read access cache hits, the cached data is read out and supplied to the CY7C601. During read access cache misses, if the selected cache line is clean (not modified), a cache line is fetched from main memory to load into the cache. If the selected cache line is modified, the selected cache line is flushed out to the CY7C605 write buffer, and a new cache line is fetched from main memory and stored into the read buffer. The new cache line is then stored in the cache from the read buffer, while the modified cache line stored in the write buffer is written out to main memory.

Multiprocessing Support

The CY7C605 is specifically designed to support multiprocessing systems. The CY7C605 accomplishes this by providing features necessary to maintain cache coherency with a second-level memory system (typically main memory or a secondary cache) and other caching systems on the shared bus.

The CY7C605 supports two modes of caching: write-through and copy-back. Write-through caching mode modifies main memory with each write access to the cache. This avoids the issue of lack of coherency between the individual cache systems and main memory, but greatly increases memory bus traffic. The effect of this increased bus traffic is a degrading of the performance of a multiprocessor system as the processing nodes compete for memory bus bandwidth. This problem is greatly reduced when copy-back caching mode is used.

Copy-back mode holds all changes to a cache line until the line is flushed from the cache. This minimizes bus traffic to only those transactions necessary to maintain the cache. However, by allowing the cache line to be modified without updating main memory, a problem arises when other processing nodes require an up-to-date copy of that memory location. The problem of modified cache lines is solved by the enforcement of a cache coherency protocol.

The CY7C605 implements a cache coherency protocol specified by the SPARC reference standard Mbus level-2 interface. This protocol is modeled after that used by the IEEE Futurebus. In this protocol, each cache line is described by one of five states: Invalid (I), Exclusive Clean (EC), Exclusive Modified (EM), Shared Clean (SC), and Shared Modified (SM). The following describes these five cache states:

Invalid (I): Cache line is not valid.

Exclusive Clean (EC): Only this cache module has a valid copy of this cache line, other than the next level of memory (main memory or secondary cache). No other cache module on the same level of memory has a valid copy of this cache line.

Exclusive Modified (EM): Only this cache module has a valid copy of this cache line. This cache module is the OWNER of the cache line, and has the responsibility to update the next level of memory (main memory or secondary cache) and also to supply data if any other cache references this memory location.

Shared Clean (SC): The same cache line may exist in more than one cache module. The next level of memory may or may not contain a valid copy of this cache line, depending upon whether this cache line has been modified in any other cache.

Shared Modified (SM): The same cache line may exist in more than one cache module, but this cache module is the OWNER of the cache line. The next level of memory does not have a valid copy of this cache line, and this cache module has the responsibility to update the next level of memory and to supply any other cache that may reference this same memory location.

These five states are described by three state bits (Valid (V), Shared (SH), and Modified(M)) in each MPTAG cache tag entry. The PVTAG cache tag entries corresponding to the same cache lines can be in one of two states: Valid (V) and Invalid (I).

Under write-through cache mode, only the valid and invalid states apply to either the MPTAG or PVTAG cache tag entries. The shared and modified bits in the MPTAG are ignored by the CY7C605 when in write-through mode.

CY7C605 Registers

All values in all control registers are read/write (with the exception of the implementation and version fields of the SCR). Control registers are accessible by use of the alternate space load or store instructions with ASI = 4.

System Control Register (SCR)

The system control register, as shown in *Figure 2*, defines the operation modes for the cache controller and MMU. The following describes the functions of the bit fields in the SCR.

IMPL, VER—The implementation number (SCR(31:28)) and the version number (SCR(27:24)) fields are hardwired; they are read only fields and writes to those fields are ignored.

Implementation number field: 0001
Version number field: 1111

MID(3:0)—*Module Identification number* (SCR(18:15)) identifies the processor module during transactions on the Mbus. This four-bit module identification number is embedded in the Mbus address phase of all Mbus transactions initiated by the CY7C605.

BM—*Boot-mode bit* (SCR(14)) indicates the system is in boot mode. This bit is set to 1 to indicate boot mode. This bit is automatically set upon power-on reset.

C—*Cacheable bit* (SCR(13)) indicates whether the access is cacheable or not when the MMU is disabled. This bit is set to 1 if accesses on the physical bus (with the MMU disabled) are to be considered cacheable.

MR—*Memory Reflection* (SCR(11)) indicates whether the main memory system on the Mbus supports memory reflection. MR affects the status of the MTAG cache tag bits.

CM—*Cache-mode bit* (SCR(10)) indicates whether the cache is operating under write-through no write allocate policy or copy-back write allocate policy. This bit is set to 1 to enable copy-back cache mode. Setting this bit to 0 will enable write-through cache mode.

IMPL	VER	RSV	MID(3:0)	BM	C	RSV	MR	CM	RSV	CE	RSV	NF	ME
31 28	27 24	23 19	18 15	14	13	12	11	10	9	8	7 2	1	0

IMPL = Specific Implementation of the MMU
VER = Version of Specific Implementation (typically mask revision)
MID(3:0) = Module Identifier (3:0)
BM = Boot Mode
C = Cacheable (when MMU disabled)
MR = Memory Reflection
CM = Cache Mode
CE = Cache Enable
NF = No Fault
ME = MMU Enable
RSV = Reserved

Figure 2. System Control Register (SCR)

CE—*Cache-enable bit* (SCR(8)) indicates whether the virtual cache is enabled or not. This bit is set to 1 to enable the cache controller.

NF—*No-fault bit* (SCR(1)) prevents supervisor data accesses from signaling data faults to the CY7C601. When the NF bit is set, exception-generating logic (in both the TLB and the table walk) does not indicate supervisor data faults to the CY7C601 (via $\overline{\text{MEXC}}$), but status and address information is recorded in the SFSR and SFAR registers as in normal data access operations. When the NF bit is not set, the CY7C605 reports the supervisor data exceptions.

ME—*MMU-enable bit* (SCR(0)) indicates whether the MMU is enabled or not. This bit is set to 1 to enable the MMU.

On power-on reset, all writeable control bits except the BM bit are cleared. This sets the CY7C605 into the following state: cache disabled (CE = 0), write-through mode (CM = 0), non-cacheable (C = 0), boot-mode enabled (BM = 1), no fault disabled (NF = 0), and MMU disabled (ME = 0).

Context Table Pointer Register (CTPR)

The context table pointer points to the context table in physical memory. The table is indexed by the contents of the context register. The context table pointer appears on bits 35 through 14 of the Mbus (MAD(35:14)) during the first fetch of TLB miss processing. Once the root pointer is cached in the PTPC (page table pointer cache), no fetching of the root pointer is required until the context is changed (see *Figure 3).*

CTP	RSV
31 — 10	9 — 0

CTP = Context Table Pointer
RSV = Reserved

Figure 3. Context Table Pointer Register

Context Register (CXR)

The context register defines a virtual address space associated with the current process. The CXR is a twelve-bit register that supports 4096 contexts. This register is used to define the current context for the CY7C605. Nearly all CY7C605 operations are dependent upon matching the value of this register to a cache tag entry or TLB entry.

RSV	CXN
31 — 12	11 — 0

CXN = Context Number
RSV = Reserved

Figure 4. Context Register

Reset Register (RR)

The RR register contains information regarding whether Watch Dog Reset (WDR), Software Internal Reset (SIR) or Software External Reset (SER) occurred. This is a read/write register, and setting the Software Internal Reset bit (SIR) or the Software External Reset (SER) causes the corresponding reset. On power-on reset, the WDR, SIR, and SER bits in the RR will be cleared. Reading the RR will also clear these bits.

RSV	WDR	SIR	SER
31 — 3	2	1	0

RSV = Reserved
WDR = Watchdog Reset
SIR = Software Internal Reset
SER = Software External Reset

Figure 5. Reset Register

Root Pointer Register (RPR)

The RPR is the context level table Page Table Pointer (PTP) and is cached in the page table pointer cache.

RP	RSV	V
31 — 6	5 — 1	0

RP = Root Pointer
RSV = Reserved
V = Valid

Figure 6. Root Pointer Register

On power-on reset, the V bit is cleared. When the current context is changed by writing to the Context Pointer Register (CXR), the V bit of the RPR is cleared. The V bit is also cleared when the CTPR register is written.

Instruction access PTP (IPTP)

The IPTP is the instruction access level 2 table Page Table Pointer (PTP) and is part of the page table pointer cache. On power-on reset, the V bit is cleared.

IPTP	RSV	V
31 — 4	3 — 1	0

IPTP = Instruction Access PTP
RSV = Reserved
V = Valid

Figure 7. Instruction Access PTP Register

Data access PTP (DPTP)

The DPTP is the data access level 2 table Page Table Pointer (PTP) and is a register in the page table pointer cache. On power-on reset, the V bit is cleared.

DPTP	RSV	V
31 — 4	3 — 1	0

DPTP = Data Access PTP
RSV = Reserved
V = Valid

Figure 8. Data Access PTP Register

Index Tag Register (ITR)

The ITR contains the tag (index1 and index2) fields of the IPTP and DPTP entries.

ITAG	RSV	DTAG	RSV
31 18	17 16	15 2	1 0

RSV = Reserved
ITAG = Instruction Access PTP Tag
DTAG = Data Access PTP Tag

Figure 9. Index Tag Register

TLB Replacement Control Register (TRCR)

The TRCR contains the Replacement Counter (RC) and Initial Replacement Counter (IRC) fields as shown in *Figure 10.* These fields are used in order to support random replacement and to support locking capabilities of the TLB. On power-on reset, both the RC and IRC fields are initialized to zero.

RSV	RC	RSV	IRC
31 14	13 8	7 6	5 0

RSV = Reserved
RC = Replacement Counter
IRC = Initial Replacement Counter

Figure 10. TLB Replacement Control Register

Synchronous Fault Status Register (SFSR)

The synchronous fault status register, illustrated in *Figure 11,* contains fault-associated information for synchronous faults. Synchronous faults are faults that occur during an integer unit access of memory. Synchronous faults include almost all possible faults for the CY7C605. This type of fault is synchronous to the operations of the CY7C601. For the CY7C605, this fault type covers all cases except those caused by delayed writes of data stored in the write buffers. These faults are asynchronous to the operation of the CY7C601, and are named asynchronous faults.

An example of a synchronous fault is a privilege violation fault caused by attempting an unauthorized memory access. Upon encountering a synchronous fault, the CY7C605 asserts the $\overline{MEXC}$ signal, along with $\overline{MHOLD}$ and $\overline{MDS}$. Synchronous faults are the only exception type that assert the $\overline{MEXC}$ signal.

The uncorrectable error (UE), timeout error (TO), and bus error bits (BE) report error status as encoded in the $\overline{MERR}$, $\overline{MRTY}$, and $\overline{MRDY}$ signals. (Refer to the section on Mbus for further information.) The level bits (L) describe the level in a table walk process at which the fault occurred (if applicable).

RSV	UC	TO	BE	L	AT	FT	FAV	OW
31 13	12	11	10	9 8	7 5	4 2	1	0

RSV = Reserved
UC = Uncorrectable Error
TO = Time Out Error
BE = Bus Error
L = Level
AT = Access Type
FT = Fault Type
FV = Fault Address Valid
OW = Over Write

Figure 11. Synchronous Fault Status Register

The access type bits (AT(2:0)) describes the access type that caused the fault. This field specifies user/supervisor access and whether the access is load or store of data or instruction. The fault address valid bit is set when the address in the Synchronous Fault Address Register (SFAR) is a valid fault address. The Over-Write bit (OW) is set in the case of a double fault where the fault status stored in the SFSR does not correspond with the fault first trapped on by the CY7C601.

Synchronous Fault Address Register (SFAR)

The synchronous fault address register contains the faulted virtual address.

SFA
31 0

SFA = Synchronous Fault Address

Figure 12. Synchronous Fault Address Register

Asynchronous Fault Status Register (AFSR)

Asynchronous faults are those faults caused by a delayed memory access initiated by the CY7C605. This type of error can only be caused by a delayed write to main memory initiated by the write buffer. Asynchronous faults cause the $\overline{CMER}$ signal to be asserted, which can be used as an interrupt to the CY7C601.

The UC, TO, and BE bits are identical to those in the SFSR. They are set by the information encoded into the $\overline{MERR}$, $\overline{MRTY}$, and $\overline{MRDY}$ signals of the Mbus. The asynchronous fault address bits provide the upper four bits of the physical address not captured in the Asynchronous Fault Address Register (AFAR), which is a thirty-two bit register.

RSV	UC	TO	BE	RSV	AFA(35:32)	RSV	AFO
31 13	12	11	10	9 8	7 4	3 1	0

RSV = Reserved
UC = Uncorrectable Error
TO = Time Out Error
BE = Bus Error
AFA = Asynchronous Fault Address
AFO = Asynchronous Fault Occurred

Figure 13. Asynchronous Fault Status Register

The Asynchronous Fault Occurred bit (AFO) is set when an asynchronous fault is encountered. Once the Asynchronous Fault Occurred (AFO) bit is set, no further asynchronous faults are recorded until the AFO bit is cleared, which is accomplished by reading the asynchronous fault address register (see *Figure 13).* On power-on reset, the UC, TO, BE, and AFO bits in the AFSR will be cleared. Reading the AFSR will also clear these bits.

Asynchronous Fault Address Register (AFAR)

The AFAR contains bits 31 - 0 of the physical address for a asynchronous faults (bus errors). Asynchronous faults can occur during delayed write accesses or during background cache line flush operations in copy-back mode (see *Figure 14).* The address in the AFAR is concatenated with the four AFA bits in the AFSR to define the entire 36-bit physical address.

AFA
31 0

AFA = Asynchronous Fault Address

Figure 14. Asynchronous Fault Address Register

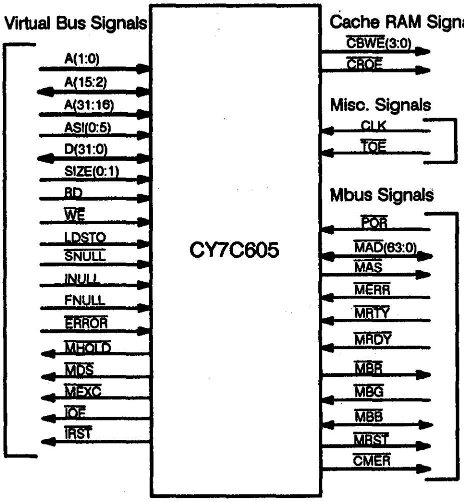


Figure 15. CY7C605 Pin Configuration

Pin Definitions

The functional pinout is shown in *Figure 15.* Note that all three-state output signals are driven to their inactive state before they are released to three-state.

Virtual Bus Signals

Signal Name	I/O	Description
A(31:16)	I	Virtual Address bus. A(31:16) are input signals during normal read/write accesses and are latched into the CY7C605 on the rising edge of clock.
A(15:2)	I/O	Virtual Address bus. Three-state input/output signals. A(15:2) are input signals during normal read/write accesses and are latched into the CY7C605 on the rising edge of the clock. They are output signals during cache line loads into the cache RAM and modified cache-line reads from the cache RAM.
A(1:0)	I	Virtual Address bus. A(1:0) are input signals during normal read/write accesses and are latched on the rising edge of clock.

Virtual Bus Signals (continued)

Signal Name	I/O	Description
ASI(5:0)	I	Address Space Identifiers. The ASI bits are used to: 1. Identify various types of accesses (user/supervisor, instruction/data) 2. Access CY7C605 registers 3. Initiate MMU flush/probe operation 4. Identify cache flush operations 5. Recognize diagnostic operations 6. Recognize pass physical address space
D(31:0)	I/O	Virtual Data bus. Three-state input/output signals. D(31:0) are input signals during CY7C601 normal write accesses, modified cache-line reads from the cache RAM, CY7C605 register writes, or CY7C605 diagnostic accesses. They are output signals during cache line loads into cache RAM, CY7C605 register reads, or CY7C605 diagnostic accesses.
$\overline{\text{ERROR}}$	I	Error (active low) signal from the CY7C601. When this signal is asserted, it indicates the CY7C601 has halted due to entering the error state. The CY7C605 reads this signal and initiates a watchdog reset.
FNULL	I	Floating point unit NULLification cycle (active high). When FNULL is active, the current access will be ignored.
INULL	I	Integer unit NULLification cycle (active high). When INULL is active, the current access will be ignored.
$\overline{\text{IOE}}$	O	Integer unit Output Enable (active low). This signal is continually driven high or low. This signal is connected to the $\overline{\text{AOE}}$ and $\overline{\text{DOE}}$ inputs of the CY7C601. When asserted, the $\overline{\text{IOE}}$ will place the address (A(31:0)), address space identifiers (ASI(7:0)), and data (D(31:0)) drivers of the CY7C601 in a three-state condition.
$\overline{\text{IRST}}$	O	Integer unit Reset (active low) is asserted to reset integer unit. This signal is continually driven high or low.
LDSTO	I	Load Store Atomic operation indicator (active high). Asserted by the CY7C601 during atomic load store cycles and is sampled by the CY7C605 on the rising edge of the clock.

Virtual Bus Signals

Signal Name	I/O	Description
$\overline{MDS}$	O	Memory Data Strobe (active low) is asserted for one clock to strobe data into the CY7C601 during a cache miss. $\overline{MHOLD}$ must be low when $\overline{MDS}$ is asserted. It is driven off of the falling edge of the clock. This is a three-state output.
$\overline{MEXC}$	O	Memory Exception (active low) is asserted for one clock whenever a privilege or protection violation is detected. $\overline{MHOLD}$ and $\overline{MDS}$ must be low when $\overline{MEXC}$ is asserted. This is a three-state output.
$\overline{MHOLD}$	O	Memory Hold (active low) is asserted by the CY7C605 whenever it requires additional time to complete the current access such as during cache miss etc. It is driven off of the falling edge of the clock.
RD	I	Read cycle indicator (active high). Asserted by the CY7C601 during read cycles and is sampled by the CY7C605 on the rising edge of the clock. This signal is also used to generate cache output enable ($\overline{CROE}$).
SIZE(1:0)	I	SIZE of access indicator. Specifies the data width of the CY7C601 access and is sampled by the CY7C605 at the rising edge of the clock.
SNULL	I	System NULLification cycle (active high). When $\overline{SNULL}$ is active, the current access will be ignored.
$\overline{WE}$	I	Write Enable to indicate write cycle (active low). Asserted by the CY7C601 during write cycles and is sampled by the CY7C605 on the rising edge of the clock. This signal is also used to generate cache byte write enables ($\overline{CBWE}$(3:0)).

Mbus Signals

Signal Name	I/O	Description
$\overline{CMER}$	O	CMU Error (active low). This open-drain signal is asserted if any bus error has occurred during writes to main memory. A system can use this signal to cause an interrupt. This signal has the same timing specifications as the Mbus control signals.
MAD (63:0)	I/O	Mbus Address and Data (three-stated bus). During the address phase of a transaction MAD(35:0) contains the physical address PA(35:0). The remaining signals MAD(63:36) during the address phase of the transaction contains the transaction associated information as shown below:

Mbus Signals (continued)

Signal Name	I/O	Description
		MAD(39:36) Transaction Type: 0 H Mbus write; 1 H Mbus read; 2 H Coherent invalidate; 3 H Coherent read; 4 H Coherent write and invalidate; 5 H Coherent read and invalidate; 6 - F H Reserved
		MAD(42:40) Transaction Size: 0 Byte (8 bits); 1 Halfword (16 bits); 2 Word (32 bits); 3 Doubleword (64bits); 4 16 Bytes*; 5 32 Bytes; 6 64 Bytes*; 7 128 Bytes* * Not supported by the CY7C605.
		MAD(43) (MC) Mbus Cacheable (active high). Indicates the current Mbus transaction is cacheable.
		MAD(45) (MBL) Mbus Boot Mode/Local indicator. MBL is high during the address phase of boot mode transactions. The instruction fetch and data accesses to the Mbus while the MMU is disabled in boot mode are considered BOOT MODE transactions. The data transactions on the Mbus required for load/store alternate instructions with ASI = 1 are considered LOCAL transactions.
		MAD(63:46) Reserved during address phase (driven high).
		During the data phase of the transaction the MAD(63:0) lines contain the 64 bits of data being transferred.
$\overline{MAS}$	I/O	Mbus Address Strobe (active low). Asserted by the bus master during the first cycle of every bus transaction to indicate the address phase of that transaction. This signal is bidirectional on the CY7C605.
$\overline{MBB}$	I/O	Mbus Bus Busy (active low) asserted by the current Mbus master during an entire transaction and, if required, during both the read and write transactions of indivisible accesses. The potential bus master devices sample $\overline{MBB}$ in order to obtain bus mastership as soon as the current master releases the bus. This is a three-state output.

Mbus Signals (continued)

Signal Name	I/O	Description
$\overline{\text{MBG}}$	I	Mbus Bus Grant (active low). Asserted by external arbiter when the Mbus is granted to a master. This signal is continually driven.
$\overline{\text{MBR}}$	O	Mbus Bus Request (active low). Asserted by potential Mbus master devices to acquire bus mastership. This signal is continually driven.
$\overline{\text{MERR}}$	I	Mbus Error (active low). Asserted or de-asserted by an Mbus slave during every data phase of a transaction. This signal is to be three-stated when released.
$\overline{\text{MIH}}$	I/O	Memory INhibit (active low). Asserted by the CY7C605 for Mbus transactions where the cache owns the data that has been requested on the Mbus. This signal is monitored during bus snooping by the CY7C605.
$\overline{\text{MRDY}}$	I/O	Mbus Ready (active low). Asserted or de-asserted by an Mbus slave during every data phase of a transaction. This signal is asserted by the CY7C605 during direct data intervention operations This signal is to be three-stated when released.
$\overline{\text{MRST}}$	O	Mbus Reset (active low). Asserted for 1024 clock cycles by only one source on the Mbus to initialize all devices on the Mbus. This signal is continually driven.
$\overline{\text{MRTY}}$	I	Mbus Retry (active low). Asserted or de-asserted by an Mbus slave during every data phase of a transaction. This signal is to be three-stated when released.

$\overline{\text{MERR}}$	$\overline{\text{MRDY}}$	$\overline{\text{MRTY}}$	Action
H	H	H	Nothing
H	H	L	Relinquish and Retry*
H	L	H	Data Strobe
H	L	L	Reserved
L	H	H	Bus Error
L	H	L	Time Out
L	L	H	Uncorrectable Error
L	L	L	Retry*

* See section on Physical Bus (Mbus)

Signal Name	I/O	Description
$\overline{\text{MSH}}$	I/O	Memory SHared (active low). Asserted by the CY7C605 after detecting a data request on the Mbus for which the CY7C605 has a copy. This signal is monitored by the CY7C605 during bus snooping.
$\overline{\text{POR}}$	I	Power-On Reset (active low). The $\overline{\text{POR}}$ initializes all on-chip logic to a known state, invalidates all the TLB entries, and all cache tag entries. It must be asserted for a minimum of 8 clocks. It also causes the CY7C605 to assert $\overline{\text{IRST}}$ to reset the CY7C601.

Cache RAM Signals

Signal Name	I/O	Description
$\overline{\text{CBWE}}$ (3:0)	O	Cache Byte Write Enables (active low). During normal write operations, certain byte enable signals are asserted depending upon the size and A(1:0) inputs. During a cache line load all four byte enable signals are asserted. These signals can also be driven by using a store alternate instruction with ASI = F H. This feature is supported for diagnostic purposes. This output is continually driven (not three-stated). $\overline{\text{CBWE0}}$ controls the most significant byte (MSB) and $\overline{\text{CBWE3}}$ controls the least significant byte (LSB).
$\overline{\text{CROE}}$	O	Cache RAM Output Enable (active low). Asserted during normal read operations with ASI = 8, 9, A, B and during modified cache line read operations. This signal is also asserted during cache data read operations with ASI = F for diagnostic purposes. This signal is continually driven.

Miscellaneous Signals

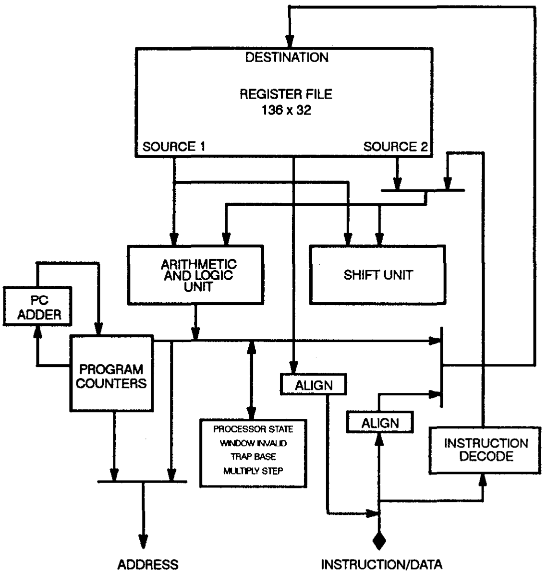
Signal Name	I/O	Description
CLK	I	System Clock. This is the same clock used by the 7C601 integer unit.
$\overline{\text{TOE}}$	I	Test Output Enable (active low). This signal is used (when high) to three-state all output drivers of the CY7C605. $\overline{\text{TOE}}$ SHOULD BE TIED LOW DURING NORMAL OPERATION. It is used to isolate the CY7C605 from the rest of the system for debugging purposes.

32-Bit RISC Controller

Features

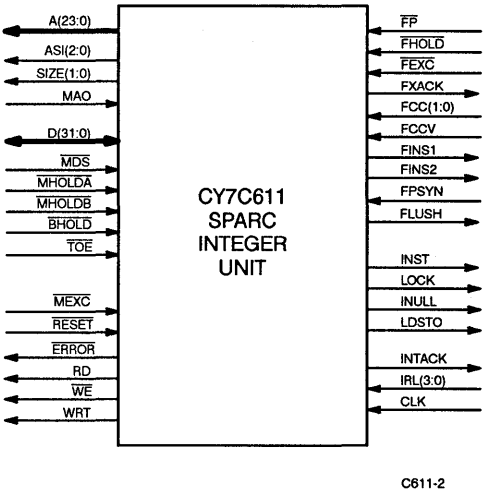
- **SPARC® processor optimized for embedded control applications**
- **Reduced Instruction Set Computer (RISC) architecture**
  - **Simple format instructions**
  - **Most instructions execute in a single cycle**
- **Very high performance**
  - **40-ns instruction cycle with 4-stage pipeline**
  - **18 sustained MIPS at 25 MHz**
  - **240-ns worst-case interrupt response**
- **136 32-bit registers**
  - **Eight overlapping windows of 24 registers each**
  - **Dividing registers into seperate register banks allows fast context switching**
  - **8 global registers**
- **Hardware pipeline interlocks**
- **16 prioritized interrupts levels**
- **Large address space**
  - **24-bit address space**
  - **3-bit address space indentifier**
- **Multitasking support**
  - **User/supervisor modes**
  - **Privileged instructions**
- **Artificial intelligence support**
- **Multiprocessing support**
- **High-performance floating-point processor interface**
  - **Concurrent execution of floating-point instructions**
- **0.8-micron 2-layer metal CMOS technology**
- **160-pin quad flat package**
- **Power**
  - **3 watts maximum**

Logic Block Diagram



C611-1

Pin Configuration



C611-2

Selection Guide

		CY7C611-25
Maximum Operating Current (mA)	Commercial	600

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Overview

The CY7C611 controller is a high-speed CMOS implementation of the SPARC 32-bit RISC architecture processor optimized for embedded control applications. RISC architecture makes possible the creation of a processor which can execute instructions at a rate of one instruction per processor clock. The CY7C611 supports a tightly-coupled floating-point coprocessor capable of executing at a rate of 4-5 MFLOPS. The CY7C611 SPARC controller provides the following features:

Simple instruction format. All instructions are 32 bits wide and aligned on 32-bit boundaries in memory. Three basic instruction formats feature uniform placement of opcode and address fields.

Register intensive architecture. Most instructions operate on either two registers or one register and a constant, and place the result in a third register. Only load and store instructions access off-chip memory.

Large windowed register file. The processor has 136 on-chip 32-bit general purpose registers. Eight of these are global registers. The remaining 128 registers can be configured as four separate non-overlapping register banks or as eight overlapping sets of 24 registers each. The first configuration allows for extremely fast context switch times and the second provides for very low overhead procedure calls. The actual configuration and use of the registers is determined by the user's application.

Delayed control transfer. The processor always fetches the next instruction after a control transfer, and either executes it or annuls it depending on the state of a bit in the control transfer instruction. This feature allows compilers to rearrange code to place a useful instruction after a delayed control transfer and thereby take better advantage of the processor pipeline.

Concurrent floating point. Floating-point instructions can execute concurrently with each other and with non-floating-point instructions.

Fast interrupt response. Interrupt inputs are sampled on every clock cycle and can be acknowledged in one to three cycles. The first instruction of an interrupt service routine can be executed within six to eight cycles of receiving the interrupt request.

The 7C600 Family

The SPARC processor family consists of the CY7C601 and CY7C611 integer units and the CY7C602 floatingp-oint unit. The CY7C601 and CY7C611 integer units are a high-speed implementation of the SPARC architecture, and are binary compatible with all SPARC processors. The CY7C602 is a high-performance floating-point unit that allows floating-point instructions to execute concurrently with the CY7C601 or the CY7C611.

The CY7C611 is designed for embedded control and application specific systems. The CY7C611 communicates with external memory via a 24-bit address bus and a 32-bit data/instruction bus. In many dedicated controller applications, the CY7C611 can function by itself with high-speed local memory. The CY7C611 retains the signals supplied on the CY7C601 for discrete implementations of cache systems. The CY7C157 cache RAM can be used with the CY7C611 to provide a zero wait-state memory system with no glue logic. The CY7C289 registered PROM (available 1st quarter 1990) provides a zero wait-state PROM memory for most accesses and requires no glue logic for interfacing to the CY7C611.

Floating-Point Coprocessor Interface

The CY7C611 is the basic processing engine which executes all of the instruction set except for floating-point operations. The CY7C602 and CY7C611 operate concurrently. The CY7C602 recognizes floating-point instructions and places them in a queue while the CY7C611 continues to execute non-floating point instructions. If the CY7C602 encounters an instruction which will not fit in its queue, the CY7C602 holds the CY7C611 until the instruction can be stored. The CY7C602 contains its own set of registers on which it operates. The contents of these registers are transferred to and from external memory under control of the CY7C611 via floating-point load/store instructions. Processor interlock hardware hides floating-point concurrency from the compiler or assembly language programmer. A program containing floating-point computations generates the same results as if instructions were executed sequentially.

Multitasking Support

The CY7C611 supports a multitasking operating system by providing user and supervisor modes. Some instructions are privileged and can only be executed while the processor is in supervisor mode. Changing from user to supervisor mode requires taking a hardware interrupt or executing a trap instruction.

Interrupts and Traps

The CY7C611 supports both asynchronous traps (interrupts) and synchronous traps (error conditions and trap instructions). The occurrence of a trap causes the CY7C611 to fetch the beginning address of the trap routine from a trap table. The base address of the trap table is specified by a trap base register and the offset is a function of the trap type. After fetching the trap routine address, program control jumps to the trap routine. Traps are taken before the current instruction is executed and can therefore be considered to occur between instructions.

Registers

The following sections provide an overview of the CY7C611 registers. The CY7C611 has two types of registers; working registers (r registers), and control registers. The r registers provide storage for processes, and the control registers keep track of and control the state of the CY7C611.

Special r Registers. The utilization of four r registers is partially fixed by the instruction set. Global register r[0] is dummy register; it returns the value "0" when it is used as a source register, and it is not modified when used as a destination register. This feature makes the most common value easily available and eliminates the need for a clear register instruction. Another r register fixed by the instruction set is r[15]. Upon executing a CALL instruction, the address of the CALL instruction is written into r[15]. Upon entering a trap routine, registers r[17] and r[18] contain the PC and nPC.

r Register Addressing. r registers r8 through r31 are addressed internally using the register number and current window pointer (CWP) field of the processor status register (PSR; see next section). The CWP is essentially an index field for r register addressing, and acts as a pointer to a group of 24 registers. *Figure 1* illustrates r register addressing using the CWP. Incrementing or decrementing the CWP changes the register offset by 16, thereby causing the register addressing to overlap by eight registers. This allows r24

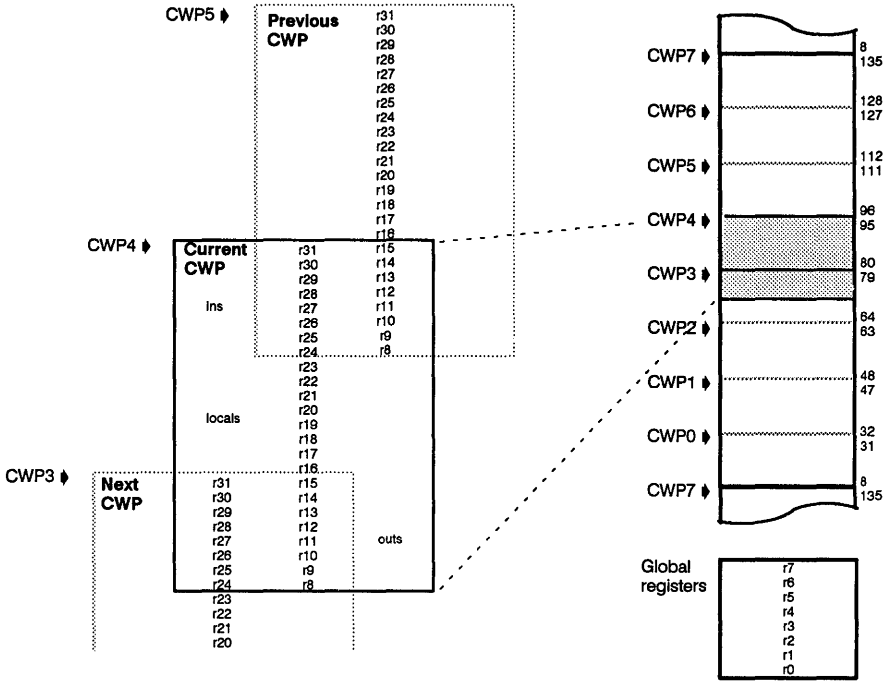


Figure 1. CWP register addressing

through r31 of the current window to act as r8 through r15 of the next window. Registers r0 through r7 do not use the CWP to address them, therefore they are global in nature.

The Window Invalid Mask register (WIM) is used to disallow selected CWP values. Each bit of the least significant byte of the WIM register corresponds to a register window or CWP value. Incrementing or decrementing the CWP to a window invalidated by the WIM register causes the CY7C611 to cause a window underflow or window overflow trap. This is used in a register window environment to set the boundaries for software. The WIM register can also be used to set boundaries for register banks in a bank switching environment.

CY7C611 Control Registers. The CY7C611's control registers contain various addresses and pointers used by the system to control its internal state. They include the Program Counters (PC and nPC), the Processor State Register (PSR), the Window Invalid Mask register (WIM), the Trap Base Register (TBR), and the Y register. The following paragraphs briefly describe each:

Processor Status Register (PSR). The processor status register contains fields that describe and control the state of the CY7C611. *Figure 2* illustrates the bit assignments for the PSR.

IU Implementation and IU Version Numbers. These are read-only fields in the PSR. The version number is set to "0001" and the implementation number is set to binary "0011".

Integer Condition Codes. The integer condition codes consist of four flags: negative, zero, overflow, and carry. These flags are set by the conditions occurring during integer logic and arithmetic operations.

Enable Floating-Point Unit (EF bit). This bit is used to enable the floating-point unit. If a floating-point operation (FPop) is encountered and the EF bit is cleared (i.e., FPU disabled), a floating-point disabled trap is generated.

Processor Interrupt Level (PIL). This four bit field sets the CY7C611 interrupt level. The CY7C611 will only acknowledge interrupts greater than the level indicated by the PIL field. Bit 11 is the MSB; bit 8 is the LSB.

Supervisor Mode (S). S = 1 indicates that the CY7C611 is in supervisor mode. Supervisor mode can only be entered by a software or hardware trap.

Previous Supervisor Mode (PS). This bit indicates the state of the supervisor bit before the most recent trap.

Trap Enable (ET). This bit enables or disables the CY7C611 traps. This bit is automatically set to 0 (traps disabled) upon entering a trap. When ET = 0, all asynchronous traps are ignored. If a synchronous trap occurs when ET = 0, the CY7C611 enters error mode.

Current Window Pointer (CWP). The r registers are addressed by the Current Window Pointer (CWP), a field of the Processor Status Register (PSR) that points to the 24 active local registers. It is incremented by a RESTORE instruction and decremented by a SAVE instruction. Note that the globals are always accessible regardless of the CWP. In the overlapping configuration each window shares its ins and outs with adjacent windows. The outs from a previous window (CWP + 1) are the ins of the current window, and the outs from the current window are the ins for the next window (CWP -1). In both the windowed and register bank configurations globals are equally available and the locals are unique to each window.

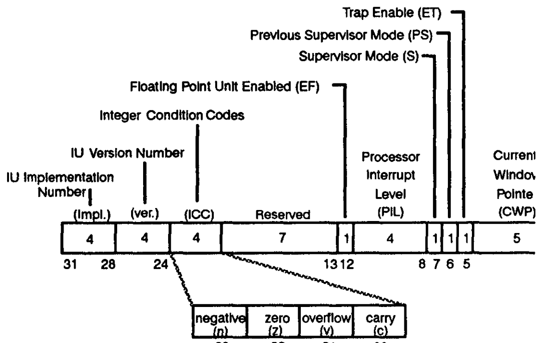


Figure 2. Processor State Register

Program Counters (PC and nPC). The Program Counter (PC) holds the address of the instruction being executed, and the Next Program Counter (nPC) holds the address of the next instruction to be executed.

Trap Base Register (TBR). The trap base register contains the base address of the trap table and a field that provides a pointer into the trap table.

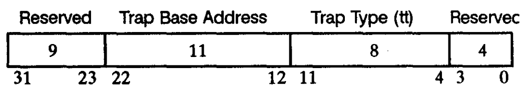


Figure 3. Trap Base Register

Window Invalid Mask Register (WIM). The window invalid mask register determines which windows are valid and which window accesses cause window_overflow and window_underflow traps.

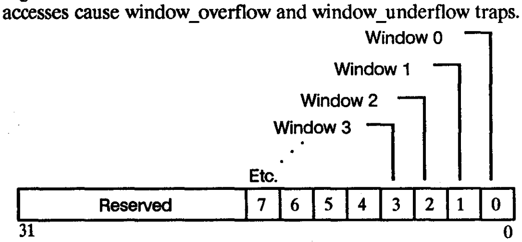


Figure 4. Window Invalid Mask

Y register. The Y register is used to hold the partial product during execution of the multiply-step instruction (MULSCC).

Pin Description

The integer unit's external signals fall into three categories:

1. memory subsystem interface signals,
2. floating-point unit interface signals, and
3. miscellaneous I/O signals.

These are described in the following sections. Paragraphs after the tables describe each signal. Signals that are active LOW are marked with an overbar; all others are active HIGH. For example, $\overline{\text{WE}}$ is active LOW, while RD is active HIGH.

Memory Subsystem Interface Signals

The memory interface signals consist of 27 bit of address (24 bits of address and a three-bit address space identifier), 32 bits of bidirectional data lines, and two bits to identify the size (byte, halfword, word, or double word) of data bus transactions.

A[23:0]—These 24 bits are the addresses of instructions or data and they are sent out "unlatched" by the CY7C611. Assertion of the MAO signal during a cache miss will force the integer unit to put the previous (missed) address on the address bus. A[23:0] pins are tristated if the $\overline{\text{TOE}}$ signal is deasserted.

ASI[2:0]—These three bits are the address space identifier for an instruction or data access to the memory. ASI[2:0] are sent out "unlatched" by the integer unit. The value on these pins during any given cycle is the address space identifier corresponding to the memory address on the A[23:0] pins at that cycle. Assertion of the MAO signal during a cache miss will force the integer unit to put the previous address space identifier on the ASI[2:0] pins. ASI[2:0] pins are tri-stated if the $\overline{\text{TOE}}$ signal is deasserted. Normally, the encoding of the ASI bits is as shown in *Table 1.* The remaining codes are software generated.

Address Space Identifier (ASI)	Address Space
000	User Instruction
010	User Data
001	Supervisor Instruction
011	Supervisor Data

Table 1. ASI Bit Assignment

D[31:0]—D[31:0] is the bidirectional data bus to and from the integer unit. The data bus is driven by the integer unit during the execution of integer store instructions and the store cycle of atomic load/store instructions. Similarly, the data bus is driven by the floating-point unit only during the execution of floating-point store instructions. The store data is sent out unlatched and must be latched externally before it is used. Once latched, store data is valid during the second data cycle of a store single access, the second and third data cycle of a store double access, and the third data cycle of an atomic load store access. The alignment for load and store instructions is done inside the processor. A double word is aligned on an eight-byte boundary, a word is aligned on a four-byte boundary, and a half word is aligned on a two-byte boundary. D(31) corresponds to the most significant bit of the least significant byte of the 32-bit word. If a double-word, word, or half-word load or store instruction generates an improperly aligned address, a memory address not aligned trap will occur. Instructions and operands are always expected to be fetched from a 32-bit wide memory.

SIZE[1:0]. These two bits specify the data size associated with a data or instruction fetch. Size bits are sent out "unlatched" by the CY7C611. The value on these pins at any given cycle is the data size corresponding to the memory address on the A[23:0] pins in that cycle. SIZE[1:0] remains valid on the bus during all data cycles of loads, stores, load_doubles, store_doubles and atomic load stores. Since all instructions are 32-bits long, SIZE[1:0] is set to "10" during all instruction fetch cycles. Encoding of the SIZE[1:0] bits is shown in *Table 2.*

SIZE1	SIZE0	Data Transfer Type
0	0	Byte
0	1	Halfword
1	0	Word
1	1	Word (Load/Store Double)

Table 2. Size Bit Assignment

$\overline{\text{MHOLDA}}$ or $\overline{\text{MHOLDB}}$. The processor pipeline will be frozen while $\overline{\text{MHOLDA}}$ is asserted and the CY7C611 outputs will revert to and maintain the value they had at the rising edge of the clock in the cycle before $\overline{\text{MHOLDA}}$ was asserted. $\overline{\text{MHOLDA}}$ is used to freeze the clock to both the Integer and floating-point units during a cache miss (for systems with cache) or when a slow memory is accessed. This signal must be presented to the processor chip at the beginning of each processor clock cycle and be stable during the high time of the processor clock. Either $\overline{\text{MHOLDA}}$ or $\overline{\text{MHOLDB}}$ can be used for stopping the processor during a cache miss or memory exception. $\overline{\text{MHOLDB}}$ has the same definition as $\overline{\text{MHOLDA}}$. The processor hardware uses the logical "OR" of all hold signals (i.e., $\overline{\text{MHOLDA}}$, $\overline{\text{MHOLDB}}$, and $\overline{\text{BHOLD}}$) to generate a final hold signal for freezing the processor pipeline. All HOLD signals are latched (transparent latch) in the CY7C611 before they are used.

$\overline{\text{BHOLD}}$. $\overline{\text{BHOLD}}$ is asserted by the I/O controller when an external bus master requests the data bus. Assertion of this signal will freeze the processor pipeline. External logic should guarantee that after deassertion of $\overline{\text{BHOLD}}$, the data at all inputs to the chip is the same as what it was before $\overline{\text{BHOLD}}$ was asserted. This signal must be presented to the processor chip at the beginning of each processor clock cycle and be stable during the high time of the processor clock since the CY7C611 processes the $\overline{\text{BHOLD}}$ input through a transparent latch before it is used. $\overline{\text{BHOLD}}$ should be used only for bus access requests by an external device since the $\overline{\text{MDS}}$ and $\overline{\text{MEXC}}$ signals are not recognized while this input is active. $\overline{\text{BHOLD}}$ should not be deasserted while LOCK is asserted.

$\overline{\text{MDS}}$. Assertion of this signal will enable the clock input to the on-chip instruction register (during an instruction fetch) or to the load result register (during a data fetch). In a system with cache, $\overline{\text{MDS}}$ is used to signal the processor when the missed data (cache miss) is ready on the bus. In a system with slow memories, $\overline{\text{MDS}}$ is used to signal the processor when the read data is available on the bus. $\overline{\text{MDS}}$ must be asserted only while the processor is frozen by either the $\overline{\text{MHOLDA}}$ or $\overline{\text{MHOLDB}}$ input signals. The CY7C611 samples the $\overline{\text{MDS}}$ signal via an on-chip transparent latch before it is used. The $\overline{\text{MDS}}$ signal is also used for strobing memory exceptions. In other words, $\overline{\text{MDS}}$ should be asserted whenever $\overline{\text{MEXC}}$ is asserted (see $\overline{\text{MEXC}}$ definition).

$\overline{\text{MEXC}}$. This signal is asserted by the memory (or cache) controller to initiate an instruction (or data) exception trap. $\overline{\text{MEXC}}$ is latched in the processor at the rising edge of CLK and is used in the following cycle. If $\overline{\text{MEXC}}$ is asserted during an instruction fetch cycle, an instruction access exception is generated, and if $\overline{\text{MEXC}}$ is asserted during a data fetch cycle, a data access exception trap is generated. The $\overline{\text{MEXC}}$ signal is used during ($\overline{\text{MHOLD}}$) in conjunction with the $\overline{\text{MDS}}$ signal to indicate to the CY7C611 that the memory system was unable to supply valid instruction or data. If $\overline{\text{MDS}}$ is applied without $\overline{\text{MEXC}}$, the CY7C611 accepts the contents of the data bus as valid information, but when $\overline{\text{MDS}}$ is applied with $\overline{\text{MEXC}}$ an exception trap is generated and the contents of the data bus is ignored by the CY7C611. (In other words, $\overline{\text{MHOLD}}$ and $\overline{\text{MDS}}$ must be low when $\overline{\text{MEXC}}$ is asserted.) $\overline{\text{MEXC}}$ must be deasserted in the same clock cycle in which $\overline{\text{MHOLD}}$ is released.

MAO. This signal is used during a MHOLD by the integer unit to select between the current memory access parameters and the previous (missed) memory parameters (i.e. the value of those parameters at the second rising edge of CLK before MHOLD was applied). A logic high value at this pin during a cache miss will cause the integer unit to put A[23:0], ASI[2:0], SIZE[1:0], RD, $\overline{\text{WE}}$, WRT, LDSTO, and LOCK values corresponding to the missed memory address on the bus. Normally, MAO should be kept at a "low" level, selecting the access parameters for the current access. MAO should not be used during store cycle misses because the $\overline{\text{WE}}$ output would be lost.

RD. This signal specifies whether the current memory access is a read or write operation. It is sent out "unlatched" by the integer unit and must be latched externally before it is used. RD is set to "0" only during data cycles of store instructions including the store cycles of atomic load store instructions. This signal, when used in conjunction with SIZE[1:0] and LDSTO, can be used to check access rights of bus transactions. In addition, the RD signal may be used to turn off the output drivers of data RAMs during a store operation. For atomic load store instructions the RD signal is "1" during the first data cycle (read cycle), and "0" during the second and third data cycles (write cycle).

$\overline{\text{WE}}$. This signal is asserted by the integer unit during the second data cycle of store single instructions, the second and third data cycles of store double instructions, and the the third data cycle of atomic load/store instructions. The $\overline{\text{WE}}$ signal is sent out "unlatched" and must be latched externally before it is used. The $\overline{\text{WE}}$ signal may be externally qualified by HOLD signals (i.e., $\overline{\text{MHOLDA}}$ and $\overline{\text{MHOLDB}}$) to avoid writing into the memory during memory exceptions.

WRT. This signal is asserted (set to "1") by the processor during the first data cycle of single or double integer store instructions, the first data cycle of single or double floating-point store instructions, and the second data cycle of atomic load/store instructions. WRT is sent out "unlatched" and must be latched externally before it is used.

LDSTO. This signal is asserted by the integer unit during the data cycles of atomic load store operations. LDSTO is sent out "unlatched" by the integer unit and must be latched externally before it is used.

LOCK. This signal is set to "1" when the processor needs the bus for multiple cycle transactions such as atomic load/store, double loads and double stores. The LOCK signal is sent "unlatched" and should be latched externally before it is used. The bus may not be granted to another bus master as long as the LOCK signal is

7

asserted (i.e., $\overline{BHOLD}$ should not be asserted in the following processor clock cycle when LOCK = 1).

INULL. Assertion of INULL indicates that the current memory access (whose address is held in an external latch) is to be nullified by the processor. INULL is intended to be used to disable cache misses (in systems with cache) and to disable memory exception generation for the current memory access (i.e., $\overline{MDS}$ and $\overline{MEXC}$ should not be asserted for a memory access when INULL = 1). INULL is a latched output and is active during the same cycle as the address which it nullifies. INULL is asserted under the following conditions: During the second cycle of a store instruction, or whenever the CY7C611 address is invalid due to an external or internal exception. If a floating-point unit or coprocessor unit is present in the system INULL should be ORed with the FNULL and CNULL signals from these units.

Floating-Point Interface Signals

The floating-point/coprocessor unit interface is a dedicated group of connections between the CY7C611 and the CY7C602. Note that no external circuits are required between the CY7C611 and the CY7C602; all traces should connect directly. The interface consists of the following signals:

$\overline{FP}$. This signal indicates whether or not a floating-point unit exists in the system. The $\overline{FP}$ signal is normally pulled up to VDD by a resistor. It is grounded when the CY7C602 chip is present. The integer unit generates a floating-point disable trap if $\overline{FP}$ = 1 during the execution of a floating-point instruction, FBfcc instruction or floating-point load and store instructions.

FCC[1:0]. These bits are taken as the current condition code bits of the CY7C602. They are considered valid if FCCV = 1. During the execution of the FBfcc instruction, the processor uses these bits to determine whether the branch should be taken or not. FCC[1:0] are latched by the processor before they are used.

FCCV. This signal should be asserted only when the FCC[1:0] bits are valid. The floating-point unit deasserts FCCV if pending floating-point compare instructions exist in the floating-point queue. FCCV is reasserted when the compare instruction is completed and the floating-point condition codes FCC[1:0] are valid. The integer unit will enter a wait state if FCCV is deasserted (i.e., FCCV = "0"). The FCCV signal is latched (transparent latch) in the CY7C611 before it is used.

$\overline{FHOLD}$. This signal is asserted by the floating-point unit if a situation arises in which the CY7C602 cannot continue execution. The floating-point unit checks all dependencies in the Decode stage of the instruction and asserts $\overline{FHOLD}$ (if necessary) in the next cycle. This signal is used by the integer unit to freeze the instruction pipeline in the same cycle. The CY7C602 must eventually deassert $\overline{FHOLD}$ in order to unfreeze the integer unit's pipeline. The $\overline{FHOLD}$ signal is latched (transparent latch) in the CY7C611 before it is used.

$\overline{FEXC}$. Assertion of this signal indicates that a floating-point exception has occurred. $\overline{FEXC}$ must remain asserted until the integer unit takes the trap and acknowledges the CY7C602 via FXACK signal. Floating-point exceptions are taken only during the execution of floating-point instructions, FBfcc instruction and floating-point load and store instructions. $\overline{FEXC}$ is latched in the integer unit before it is used. The CY7C602 should deassert $\overline{FHOLD}$ if it detects an exception while $\overline{FHOLD}$ is asserted. In this case $\overline{FEXC}$ should be asserted a cycle before $\overline{FHOLD}$ is deasserted.

INST. This signal is asserted by the integer unit whenever a new instruction is being fetched. It is used by the CY7C602 to latch the instruction on the D[31:0] bus into the CY7C602 instruction buffer. The CY7C602 needs two instruction buffers (D1 and D2) to save the last two fetched instructions. When INST is asserted a new instruction enters into the D1 buffer and the old instruction in D1 enters into the D2 buffer.

FLUSH. This signal is asserted by the integer unit and is used by the CY7C602 to flush the instructions in its instruction registers. This may happen when a trap is taken by the integer unit. Instructions that have entered into the floating-point queue may continue their execution if FLUSH is raised as a result of a trap or exception other than floating-point exceptions.

FINS1. This signal is asserted by the integer init during the decode stage of a CY7C602 instruction if the instruction is in the D1 buffer of the CY7C602 chip. The CY7C602 uses this signal to latch the instruction in D1 buffer into its execute stage instruction register.

FINS2—This signal is asserted by the integer unit during the decode stage of a CY7C602 instruction if the instruction is in the D2 buffer of the CY7C602 chip. The CY7C602 uses this signal to latch the instruction in D2 buffer into its execute stage instruction register.

FXACK—This signal is asserted by the integer unit in order to acknowledge to the CY7C602 that the current $\overline{FEXC}$ trap is taken. The CY7C602 must deassert $\overline{FEXC}$ after it receives an asserted level of FXACK signal so that the next floating-point instruction does not cause a "repeated" floating-point exception trap.

Miscellaneous I/O Signals

These signals are used by the CY7C611 to control external events or to receive input from external events. This interface consists of the following signals:

IRL[3:0]. The data on these pins defines the external interrupt level. IRL[3:0] = 0000 indicates that no external interrupts are pending. The integer unit uses two on-chip synchronizing latches to sample these signals on the rising edge of CLK. A given interrupt level must remain valid for at least two consecutive cycles to be recognized by the integer unit. IRL[3:0] = 1111 signifies an non-maskable interrupt. All other interrupt levels are maskable by the PIL field of the Processor State Register (PSR). External interrupts should be latched and prioritized by the external logic before they are passed to the integer unit. The external interrupt latches should keep the interrupts pending until they are taken (and acknowledged) by the integer unit. External interrupts can be acknowledged by software or by the Interrupt Acknowledge (INTACK) output.

INTACK—This signal is asserted by the integer unit when an external interrupt is taken.

$\overline{RESET}$—Assertion of this pin will reset the integer unit. The $\overline{RESET}$ signal must be asserted for a minimum of eight processor clock cycles. After a reset, the integer unit will start fetching from address 0. The $\overline{RESET}$ signal is latched by the integer unit before it is used.

$\overline{ERROR}$—This signal is asserted by the integer unit when a trap is encountered while traps are disabled via the ET bit in the PSR. In this situation the integer unit saves the PC and nPC registers, sets the tt value in the TBR, enters into an error state, asserts the

$\overline{\text{ERROR}}$ signal and then halts. The only way to restart the processor trapped in the error state, is to trigger a reset by asserting the $\overline{\text{RESET}}$ signal.

$\overline{\text{TOE}}$—This signal is used to force all output drivers of the processor chip into a high-impedance state. It is used to isolate the chip from the rest of the system for debugging purposes. THIS PIN SHOULD BE TIED LOW FOR NORMAL OPERATION.

FPSYN—This pin is a mode pin which is used to allow execution of additional instructions in future designs. It should be normally kept deasserted (FPSYN = 0) to disable the execution of these instructions.

CLK—CLK is a 50% duty-cycle clock used for clocking the CY7C611's pipeline registers. It is HIGH during the first half of the processor cycle, and LOW during the second half. The rising edge of CLK defines the beginning of each pipeline stage in the CY7C611 chip.

Section Contents

Modules **Page Number**

CYPRESS SEMICONDUCTOR

Custom Module Capabilities

Cypress's Multichip Products group is a leading supplier of custom memory and/or logic modules. This turnkey capability provides designers with a fast, low-risk solution for when they require the ultimate in system performance and density. Detailed information on our standard modules can be found in the static RAM and Module sections of this book.

Custom Capabilities

Cypress's Multichip Products Division is currently supporting custom modules with the following technical requirements:

Substrate Type:	Ceramic, Epoxy Laminate
Comp. Packaging:	LCC, SOJ, SOIC, PLCC
Pin Configuration:	DIP, VDIP (DSIP), ZIP, SIP, QUIP, PGA
Data Word Width:	Up to 144 Bits
Pin Count:	Up to 200 Pins
Access Time:	10 ns and up

As 1990 progresses, we will be introducing new technology which will extend each of these capabilities.

Multichip modules are typically SRAM based. However, other types of components can be used in addition to or instead of SRAMs—Logic, PLDs, EPROM, gate arrays, microprocessors, etc.

Advantages of Custom Modules

Custom modules provide the memory system designer with the ultimate in flexibility and performance. For example, when using a custom module it is very straightforward to implement unusual memory word widths—a capability that becomes critical in high-speed applications such as digital signal processing and RISC-based systems.

Custom modules are built using fully-tested components, and are rigorously tested before they are shipped. This testing redundancy saves time and effort during system testing and provides an added degree of reliability.

Performance and Density Improvements

Far greater memory densities can be achieved with the use of modules than with even the most advanced surface mount technologies. This density can be attained for several reasons:

- **Orientation.** Module substrates can be oriented vertically, with devices mounted on both sides
- **Routing Efficiency.** Due to compact module size, more efficient routing techniques can be used. These include tighter line spacing, blind and buried vias, and selective manual routing.
- **Pin Reduction.** The reduced number of device pins, which results from the use of modules, allows the memory system itself to be routed more efficiently.
- **Ceramic Substrates.** Ceramic is the highest density interconnect medium for surface-mount packages. Thus, modules provide large density improvements while satisfying hermeticity requirements, if desired.

Module usage also improves memory system performance. These performance advantages include the following

- Crosstalk characteristics are substantially improved.
- Number of pins is minimized.
- Ceramic may be used to improve thermal characteristics.

Custom Module Flow

Multichip's focus is on providing turnkey memory modules. *Figure 1* illustrates the tasks performed during the development of the module.

Module development commences with the generation of a detailed Objective Specification. The module is designed to this specification, and once in production it will be guaranteed to perform as indicated in the Objective Spec.

Components are selected while the specification is being generated. In many cases, the spec is designed such that multiple sources of components can be utilized. Once the spec is complete and the components are selected, a schematic for the module is generated. The netlist from the schematic is used to drive the circuit simulator.

During simulation, several types of analyses are performed. A functional simulation is used to ensure that the module's logic is designed properly. Timing simulation is run to verify that the module will function when subjected to the worst case timing delays of the components. Finally, thermal analysis may be performed to determine the thermal characteristics of the module.

Custom Module Flow (continued)

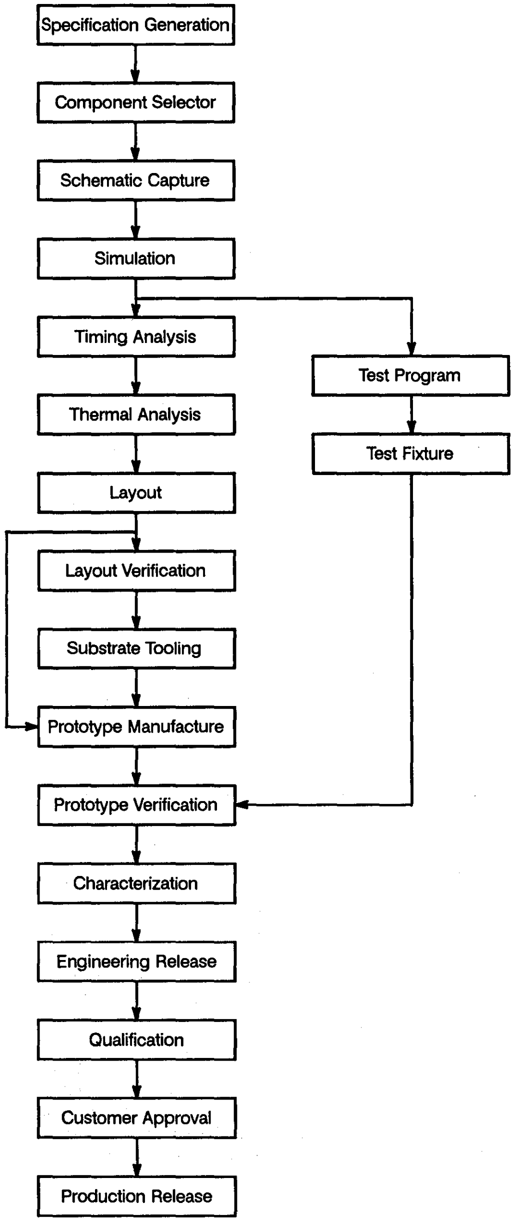


Figure 1. Custom Module Flow

The layout of the module is also netlist driven. An autorouter may or may not be used, depending on the complexity and density of the module. Design rule checks are run to ensure that the layout does not violate any electrical or mechanical design rules. Finally, the layout output is used to generate the module substrate.

The layout output is also used to drive the pick and place equipment. This ensures consistency between design and manufacturing. While the module prototypes are being assembled, the test program is generated and the test fixture is constructed. Test program generation is largely automated, using as inputs the simulation outputs and pre-defined test program subroutines for common configurations.

Once prototypes have been generated, the standard release procedure is initiated. This procedure includes steps such as bench testing, module characterization and qualification, and fine tuning of the test program. Following customer approval of the module, it is released to production.

Future Technologies

Cypress is committed to providing the most advance custom module capability in the industry. This commitment includes more than simply modularizing the most advanced Cypress memory products. As part of our commitment to redefining the leading edge in module technology, we are pioneering the use of several advanced technologies:

- ECL and BiCMOS products of Cypress's Aspen Semiconductor subsidiary
- Advanced packaging techniques such as Tape Automated Bonding (TAB).
- Advanced module package formats, such as ZIP packaging and sub-one hundred mil pin spacing.
- Application of design automation techniques to module products.

Quoting Information

In order to prepare a quotation or proposal, we need as much as possible of the following information:

- Circuit schematic
- Functional description
- Mechanical dimensions required
- Speed and power requirements
- Prototype and production deadlines
- Production quantity estimates
- An engineering contact to answer questions

Once the above information is received, a budgetary quotation will typically be provided within one to two weeks.

This is a partial data sheet. For complete data sheet, see Section 2, Static RAMs.

CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1220**

64K x 4 SRAM Module

Features

- **Very high speed 256K SRAM module**
  - **Access time of 10 nsec.**
- **300-mil-wide hermetic DIP package**
- **Low active power**
  - **1.8W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **On-chip decode for speed and density**
- **JEDEC pinout—compatible with 7C194 monolithic SRAMs**
- **Small PCB footprint**
  - **0.36 sq. in.**

Functional Description

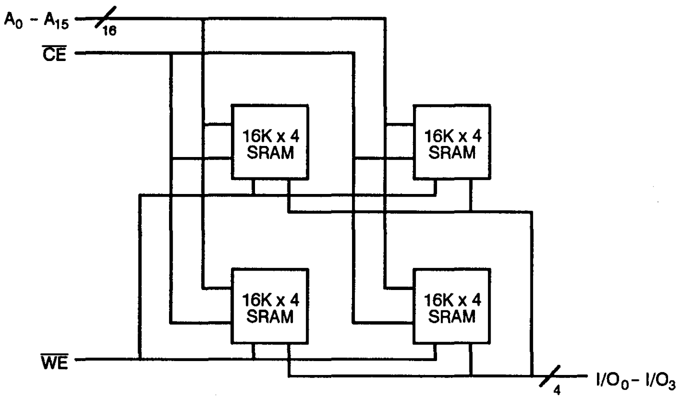
The CYM1220 is an extremely high performance 256-kilobit static RAM module organized as 65,536 words by 4 bits. This module is constructed using four 16K x 4 static RAMs in LCC packages mounted on a 300-mil-wide ceramic substrate. Extremely high speed and density are achieved by using BiCMOS SRAMs containing internal address decoding logic.

Writing to the module is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I/O_0 through I/O_3) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{15}) will appear on the four output pins (I/O_0 through I/O_3).

The data output pins remain in a high-impedance state unless the module is selected and write enable ($\overline{WE}$) is HIGH.

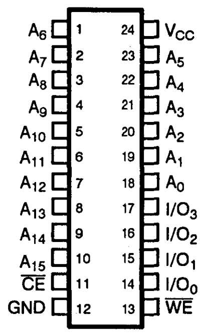
Logic Block Diagram



1220-1

Pin Configuration

DIP
Top View



1220-2

Selection Guide

		1220HD-10	1220HD-12	1220HD-15	1220HD-20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	325	325	325	
	Military		375	375	375
Maximum Standby Current (mA)	Commercial	200	200	200	
	Military		250	250	250

This is a partial data sheet. For complete data sheet, see Section 2, Static RAMs.

CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1240**

256K X 4 SRAM Module

Features

- High-density 1-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 25 ns
- Low active power
  - 2.6W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of 0.3 in.
- Small PCB footprint
  - 0.56 sq. in.

Functional Description

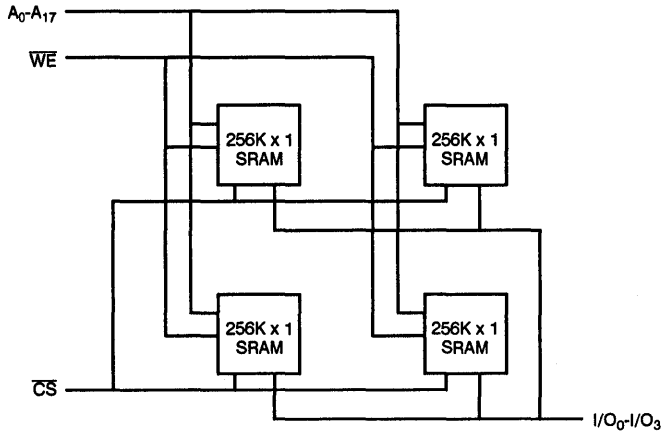
The CYM1240 is a very high performance 1-megabit static RAM module organized as 256K words by 4 bits. This module is constructed using four 256K x 1 static RAMs in LCC packages mounted on a ceramic substrate with pins. It is socket-compatible with monolithic 256K x 4 SRAMs.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 - I/O_3) of the device is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) low while ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{17}) will appear on the appropriate data input/output pins (I/O_0 - I/O_3).

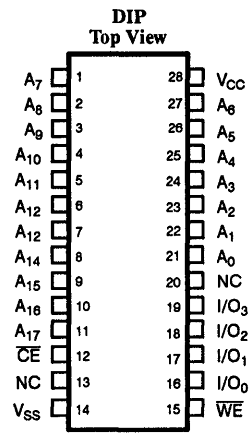
The data input/output pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or when write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



1240-1

Pin Configuration



1240-2

Selection Guide

		1240HD-25	1240HD-35	1240HD-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	480	480	480
	Military	480	480	480
Maximum Standby Current (mA)	Commercial	160	160	160
	Military	160	160	160

PRELIMINARY **CYM1400**

32K x 8 SRAM Module

Features

- **Very high speed 256K SRAM module**
  - **Access time of 10 nsec.**
- **300-mil-wide hermetic DIP package**
- **Low active power**
  - **2.1W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **On-chip decode for speed and density**
- **JEDEC pinout—compatible with 7C199 monolithic SRAMs**
- **Small PCB footprint**
  - **0.42 sq. in.**

Functional Description

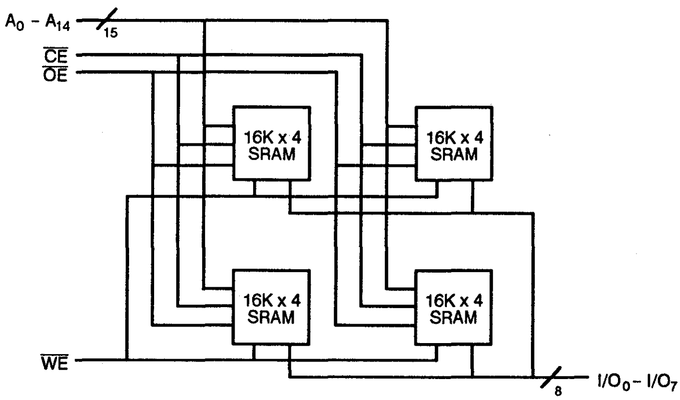
The CYM1400 is an extremely high performance 256-kilobit static RAM module organized as 32,768 words by 8 bits. This module is constructed using four 16K x 4 static RAMs in LCC packages mounted on a 300-mil-wide ceramic substrate. Extremely high speed and density are achieved by using BiCMOS SRAMs containing internal address decoding logic.

Writing to the module is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{14}) will appear on the eight output pins (I/O_0 through I/O_7).

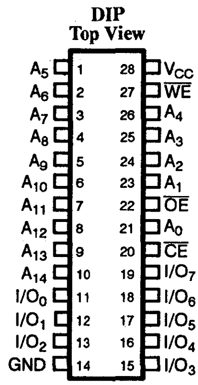
The data output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1400-1

Pin Configuration



1400-2

8

Selection Guide

		1400HD-10	1400HD-12	1400HD-15	1400HD-20
Maximum Access Time (ns)		10	12	15	20
Maximum Operating Current (mA)	Commercial	375	375	375	
	Military		425	425	425
Maximum Standby Current (mA)	Commercial	200	200	200	
	Military		250	250	250

This is a partial data sheet. For complete data sheet, see Section 2, Static RAMs.

CYPRESS SEMICONDUCTOR

CYM1420

128K x 8 Static RAM Module

Features

- High-density 1-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 30 ns
- 32-pin, 0.6-in.-wide DIP package
- JEDEC-compatible pinout
- Low active power
  - 1.2W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Commercial and military temperature ranges

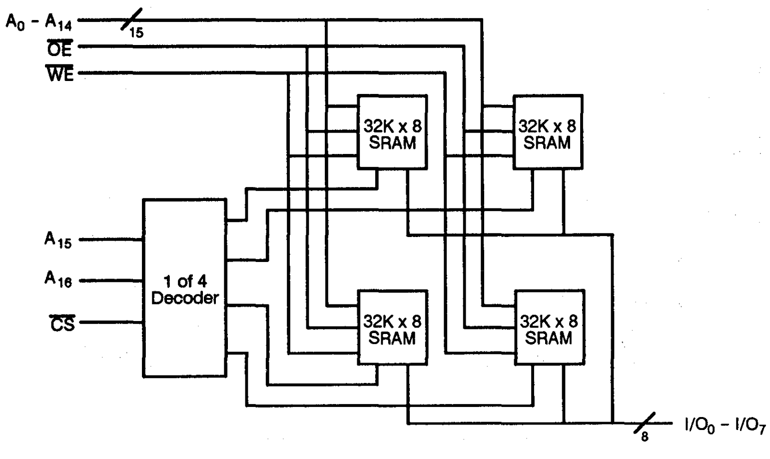
Functional Description

The CYM1420 is a very high performance 1-megabit static RAM module organized as 128K words by 8 bits. The module is constructed using four 32K x 8 static RAMs in leadless chip carriers mounted onto a double-sided multilayer ceramic substrate. A decoder is used to interpret the higher-order addresses A_{15} and A_{16} and to select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$), and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

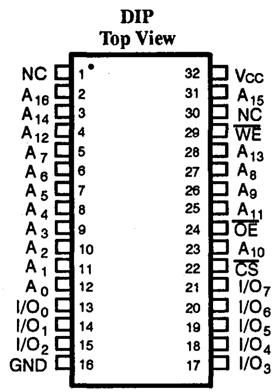
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1420-1

Pin Configuration



1420-2

Selection Guide

		1420HD-30	1420HD-35	1420HD-45	1420HD-55
Maximum Access Time (ns)		30	35	45	55
Maximum Operating Current (mA)	Commercial	210	210	210	210
	Military			210	210
Maximum Standby Current (mA)	Commercial	140	140	140	140
	Military			140	140

This is a partial data sheet. For complete data sheet, see Section 2, Static RAMs.

CYPRESS SEMICONDUCTOR

CYM1421

128K x 8 Static RAM Module

Features

- High-density 1-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 70 ns
- 32-pin, 0.6-in.-wide DIP package
- JEDEC-compatible pinout
- Low active power
  - 660 mW (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- 2V data retention (L version)

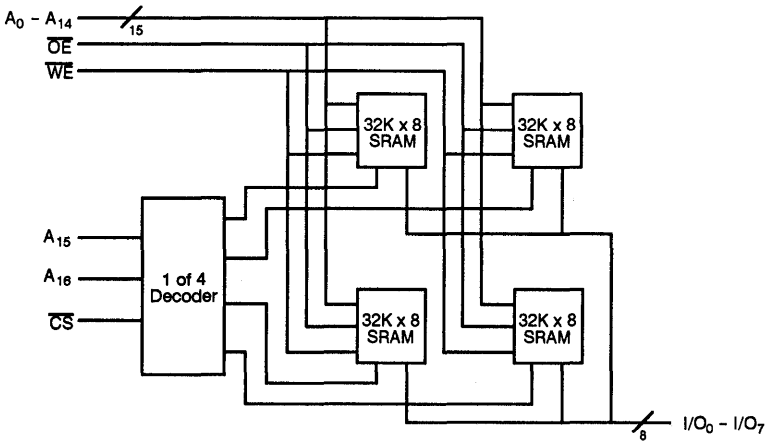
Functional Description

The CYM1421 is a high-performance 1-megabit static RAM module organized as 128K words by 8 bits. The module is constructed using four 32K x 8 static RAMs in leadless chip carriers mounted onto a double sided multilayer ceramic substrate. A decoder is used to interpret the higher-order addresses A_{15} and A_{16} and select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$), and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

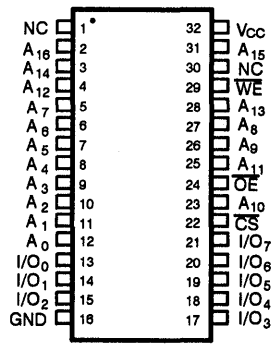
Logic Block Diagram



1421-1

Pin Configuration

DIP
Top View



1421-2

8

Selection Guide

		1421HD-70	1421HD-85
Maximum Access Time (ns)		70	85
Maximum Operating Current (mA)	Commercial	120	120
Maximum Standby Current (mA)	Commercial	70	70

CYPRESS SEMICONDUCTOR

128K x 8 Static RAM Module

Features

- High-density 1-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 30 ns
- Low active power
  - 1.1W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of 0.65 in.
- Small PCB footprint
  - 0.8 sq. in.

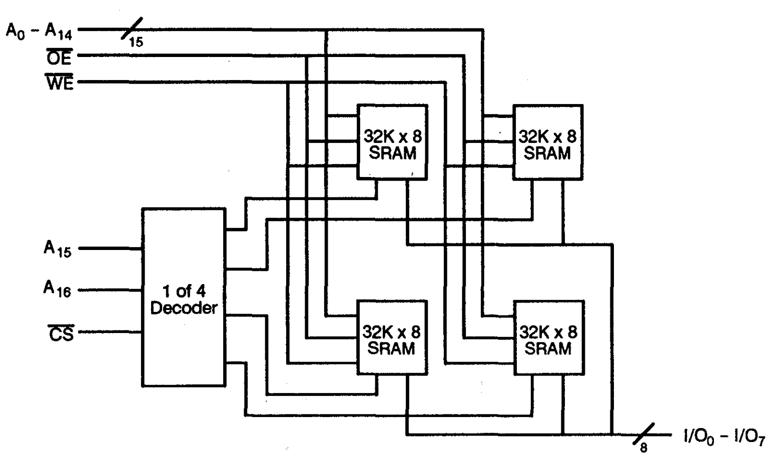
Functional Description

The CYM1422 is a high-performance 1-megabit static RAM module organized as 128K words by 8 bits. This module is constructed using four 32K x 8 static RAMs in SOICs mounted onto a single sided multilayer epoxy laminate board with pins. A decoder is used to interpret the higher-order address A_{15} and A_{16} and select one of the four RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the eight data input/output pins.

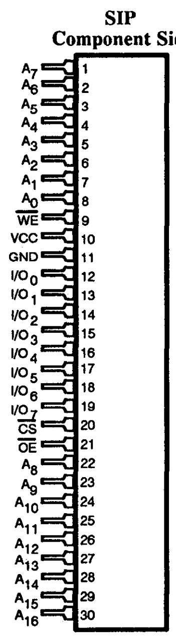
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1422-1

Pin Configuration



1422-2

Selection Guide

	1422PS-30	1422PS-35	1422PS-45	1422PS-55
Maximum Access Time (ns)	30	35	45	55
Maximum Operating Current (mA)	200	200	200	200
Maximum Standby Current (mA)	140	140	140	140

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –10°C to +90°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1422PS		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		–0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–15	+15	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	–15	+15	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS} \leq V_{IL}$		200	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}; $\overline{CS} \geq V_{IH}$ Min. Duty Cycle = 100%		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}; $\overline{CS} \geq V_{CC}$ – 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq$ 0.3V		80	mA

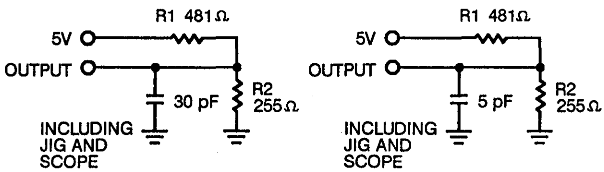
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		35	pF

Notes:

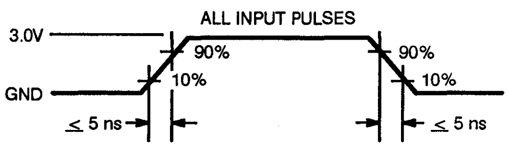
1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms



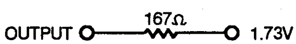
(a) (b)

1422-3



1422-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

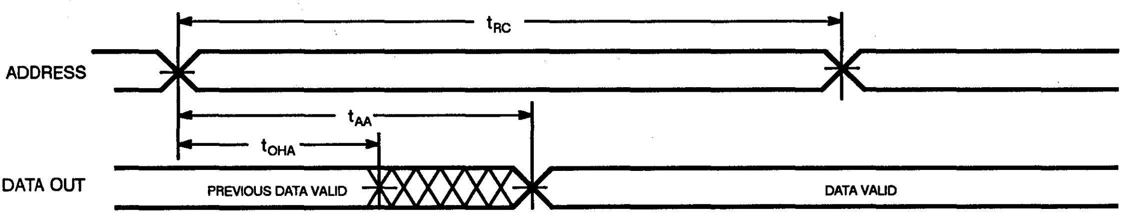
Parameters	Description	1422PS-30		1422PS-35		1422PS-45		1422PS-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	30		35		45		55		ns
t_{AA}	Address to Data Valid		30		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		30		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		20		20		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		15		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		30		35		45		55	ns
WRITE CYCLE [7]										
t_{WC}	Write Cycle Time	30		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	25		30		40		45		ns
t_{AW}	Address Set-Up to Write End	25		30		40		45		ns
t_{HA}	Address Hold from Write End	5		5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		25		35		35		ns
t_{SD}	Data Set-Up to Write End	15		20		20		20		ns
t_{HD}	Data Hold from Write End	3		3		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	15	0	20	0	25	0	25	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms [11]

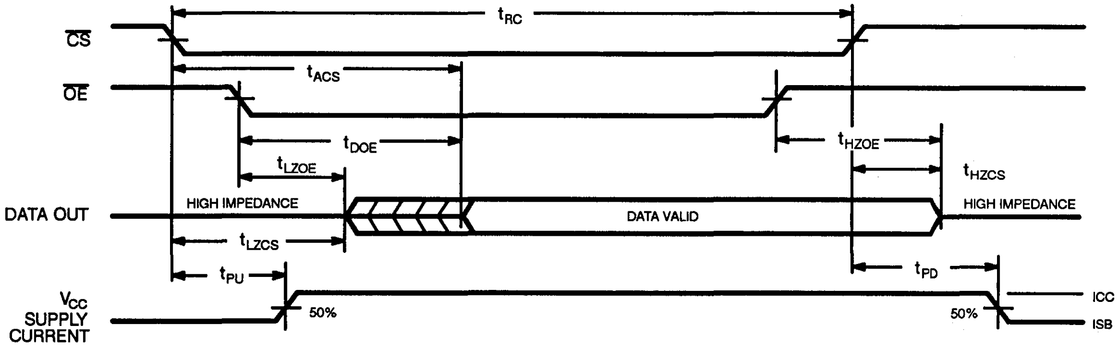
Read Cycle No. 1 [8, 9]



1422-5

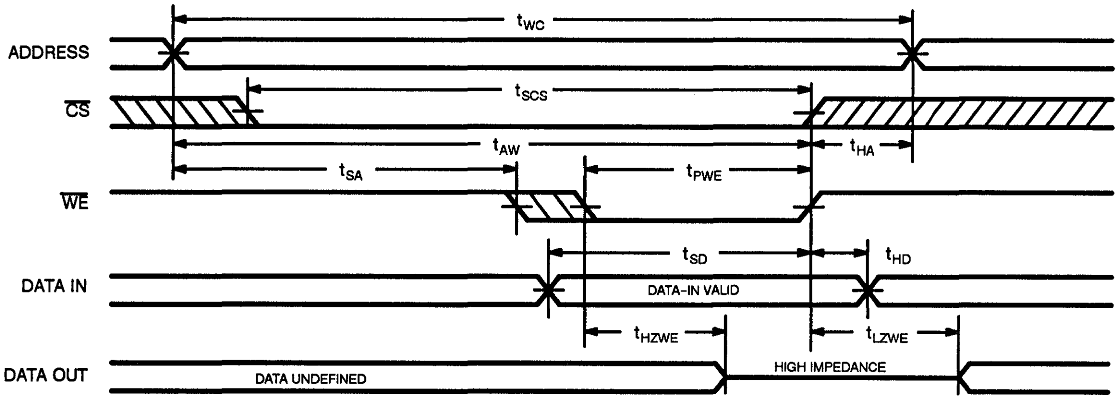
Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



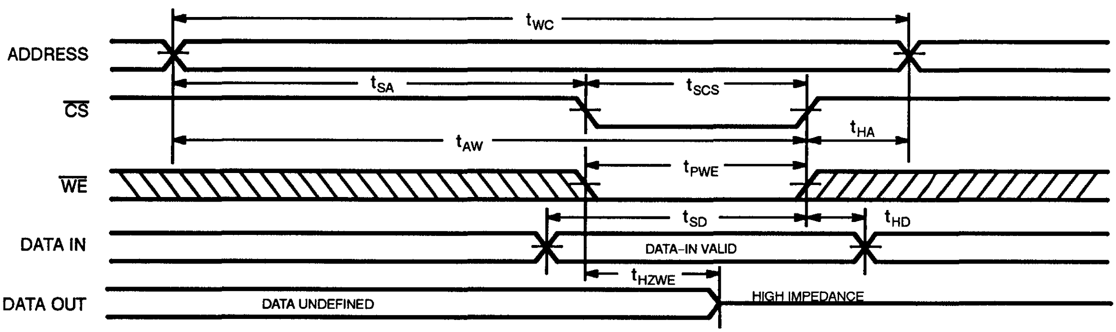
1422-6

Write Cycle No. 1 (WE Controlled)[7]



1422-7

Write Cycle No. 2 (CS Controlled)[7, 12]



1422-8

8

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
30	M1422PS-30C	PS03	Commercial
35	M1422PS-35C	PS03	Commercial
45	M1422PS-45C	PS03	Commercial
55	M1422PS-55C	PS03	Commercial

Document #: 38-M-00003-A

This is a partial data sheet. For complete data sheet, see Section 2, Static RAMs.

CYPRESS SEMICONDUCTOR

CYM1423

128K x 8 Static RAM Module

Features

- High-density 1-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 45 ns
- 32-pin, 0.6-inch-wide DIP package
- JEDEC-compatible pinout
- Low active power
  - 1.2W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Commercial temperature range
- Small PCB footprint
  - 1.1 sq. in.

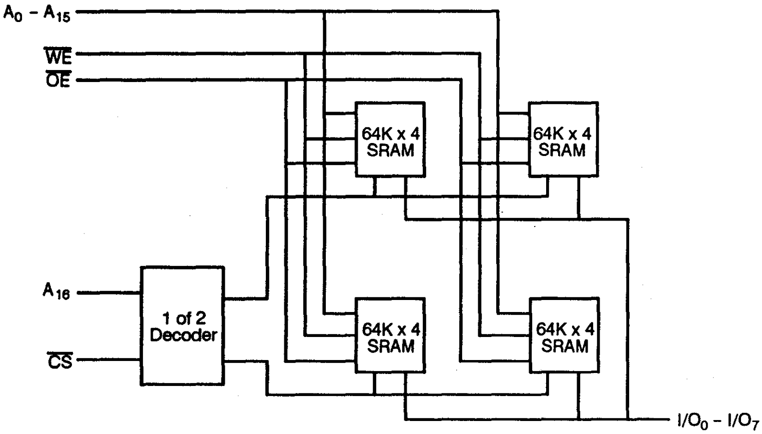
Functional Description

The CYM1423 is a high-performance 1-megabit static RAM module organized as 128K words by 8 bits. This module is constructed using four 64K x 4 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins. A decoder is used to interpret the higher-order address and select two of the four RAMs.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{16}). Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{16}) will appear on the eight input/output pins (I/O_0 through I/O_7).

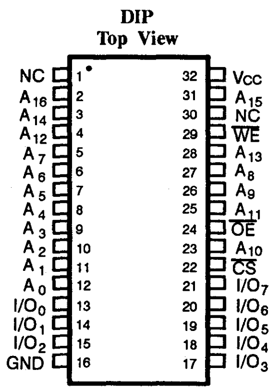
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1423-1

Pin Configuration



1423-2

Selection Guide

	1423PD-45	1423PD-55	1423PD-70
Maximum Access Time (ns)	45	55	70
Maximum Operating Current (mA)	210	210	210
Maximum Standby Current (mA)	80	80	80

8

256K x 8 SRAM Module

Features

- **High-density 2-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 25 ns**
- **Low active power**
  - **— 5.3W (max.)**
- **SMD technology**
- **Separate Data I/O**
- **60-pin ZIP package**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .5 in.**
- **Small PCB footprint**
  - **— 1.17 sq. in.**

Functional Description

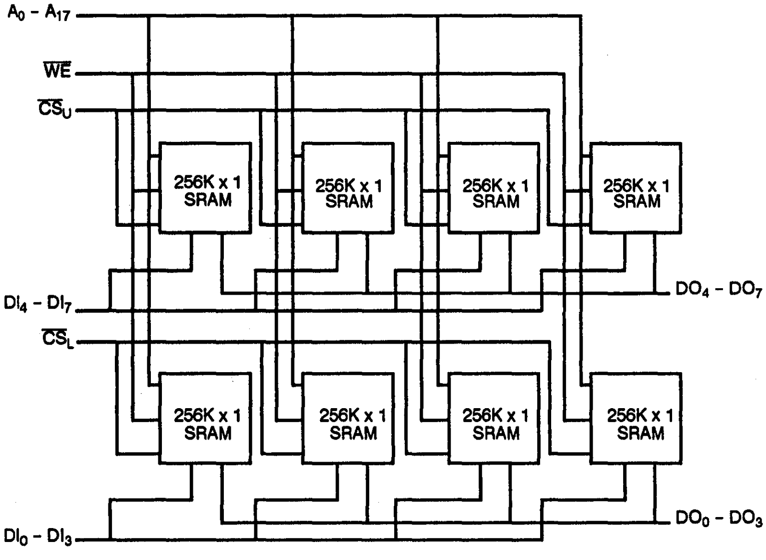
The CYM1441 is a very high performance 2-megabit static RAM module organized as 256K words by 8 bits. This module is constructed using eight 256K x 1 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins. Two chip selects ($\overline{CS}_L$ and $\overline{CS}_U$) are used to independently enable the upper and lower 4 bits of the data word.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input pins (DI_0 through DI_7) of the device is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) low, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{17}) will appear on the appropriate data output pins (DO_0 through DO_7).

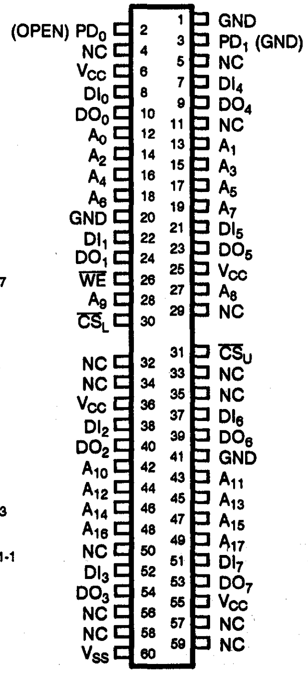
The data output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1441-1

Pin Configuration



1441-2

Selection Guide

	1441PZ-25	1441PZ-35	1441PZ-45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	960	960	960
Maximum Standby Current (mA)	320	320	320

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −10°C to +85°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1624PV		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−80	80	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−50	50	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		960	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		160	mA

8

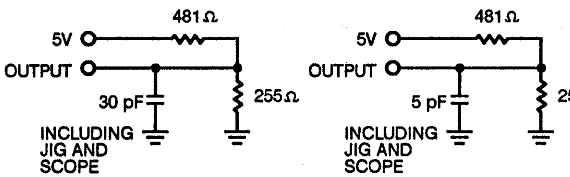
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	70	pF
C_{OUT}	Output Capacitance		25	pF

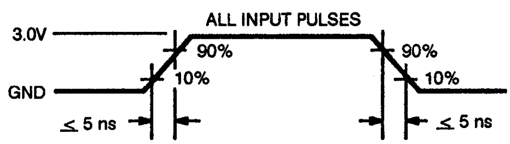
Notes:

1. $V_{IL(MIN)}$ = −3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



(a) (b) 1441-3



1441-4

Switching Characteristics Over Operating Range [3]

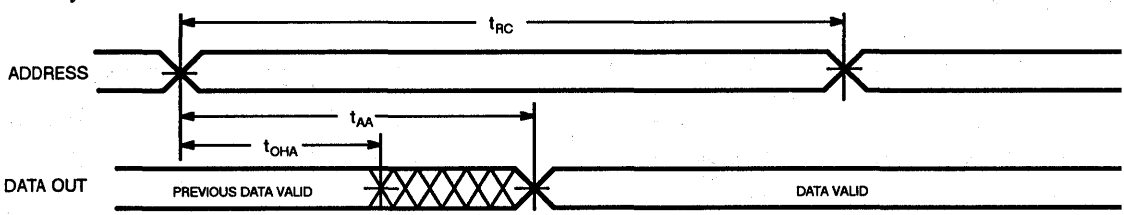
Parameters	Description	1441PZ-25		1441PZ-35		1441PZ-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]		15		25		30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		35		ns
t_{AW}	Address Set-Up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up from Write Start	0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [4]	0	15	0	20	0	25	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{CS}$ transition low.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

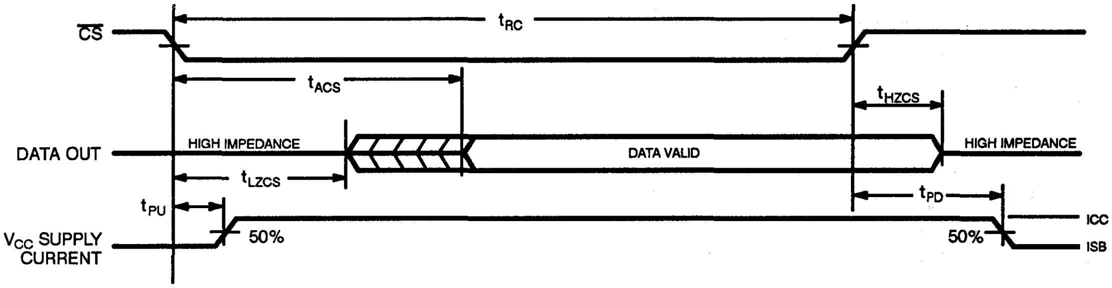
Read Cycle No. 1[6, 7]



1441-

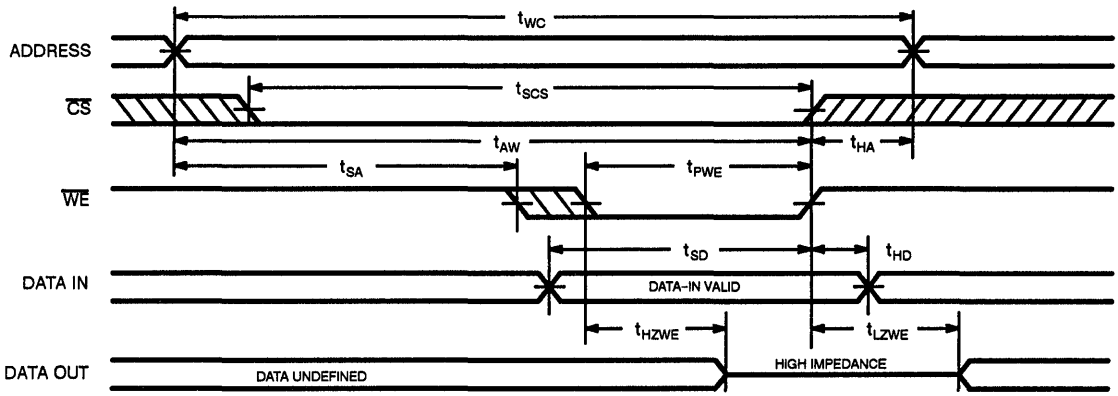
Switching Waveforms (continued)

Read Cycle No. 2[6, 8]



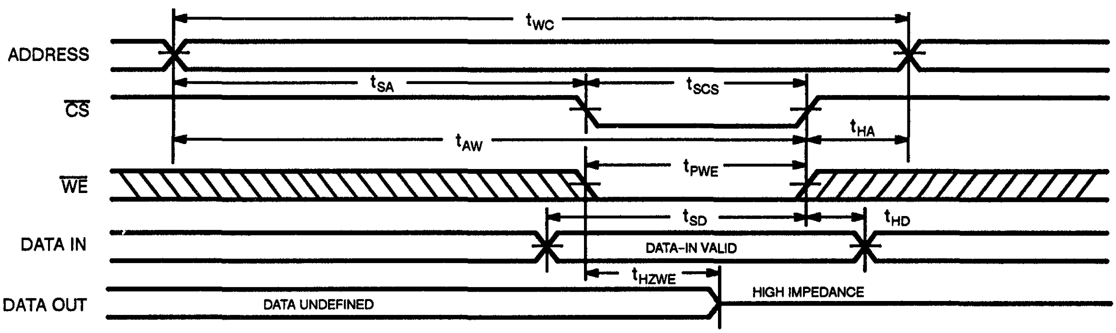
1441-6

Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



1441-7

Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



1441-8

8

Truth Table

CS	WE	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read Word
L	L	Data In	Write Word
L	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1441PZ-25C	PZ04	Commercial
35	CYM1441PZ-35C	PZ04	Commercial
45	CYM1441PZ-45C	PZ04	Commercial

Document #: 38-M-00020

512K x 8 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 35 ns**
- **Low active power**
  - **— 3.4W (max.)**
- **Double-sided SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile version (PF)**
  - **— Max. height of .345 in.**
- **Small footprint SIP version (PS)**
  - **— PCB layout area of 1.2 sq. in.**

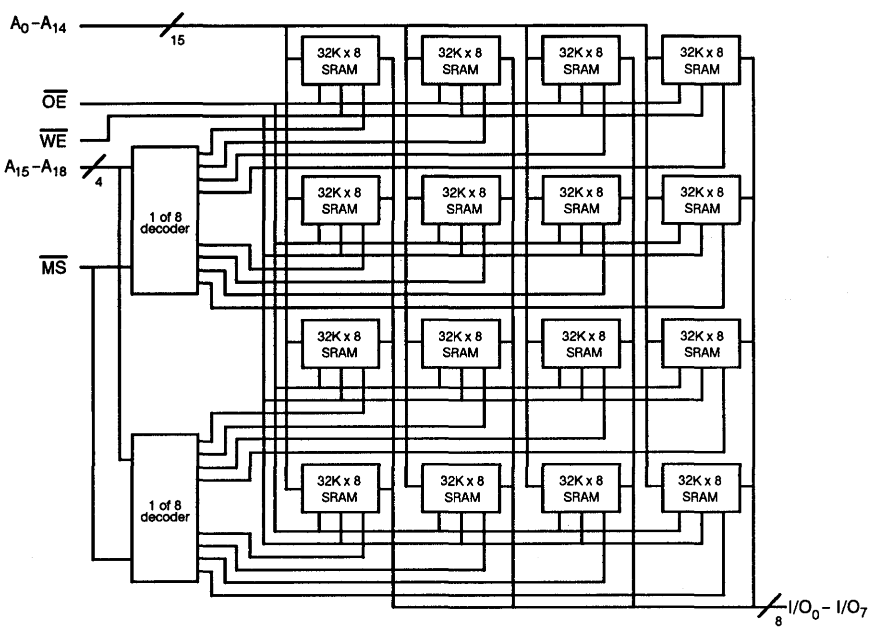
Functional Description

The CYM1460 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed from sixteen 32K x 8 SRAMs in plastic surface mount packages on an epoxy laminate board with pins. Two choices of pins are available for vertical (PS) or horizontal (PF) through-hole mounting. On-board decoding selects one of the sixteen SRAMs from the high-order address lines, keeping the remaining fifteen devices in standby mode for minimum power consumption.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{MS}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{MS}$ and $\overline{OE}$, active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

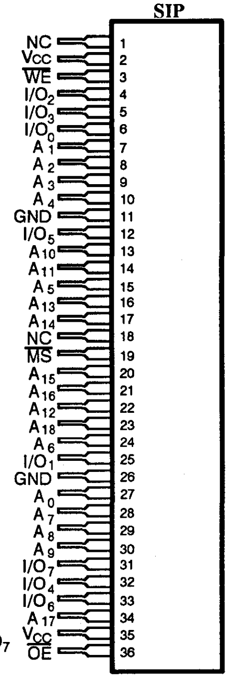
Logic Block Diagram



1460-1

Pin Configuration

SIP



1460-2

Selection Guide

	1460PS-35 1460PF-35	1460PS-45 1460PF-45	1460PS-55 1460PF-55	1460PS-70 1460PF-70
Maximum Access Time (ns)	35	45	55	70
Maximum Operating Current (mA)	625	625	625	625
Maximum Standby Current (mA)	560	560	560	560

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied .... 0°C to +70°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1460		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		–0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–20	+20	μA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$ Output Disabled	–20	+20	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., MS $\leq V_{IL}$ I_{OUT} = 0 mA		625	mA
I_{SB1}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS} \geq V_{IH}$, Min. Duty Cycle = 100%		560	mA
I_{SB2}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V		320	mA

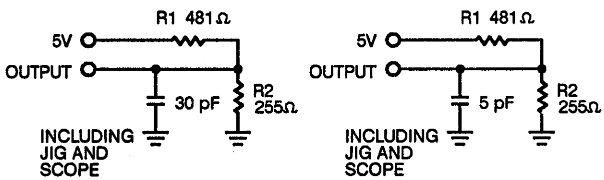
Capacitance[1]

Parameters	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	120	pF
C_{OUT}	Output Capacitance		180	pF

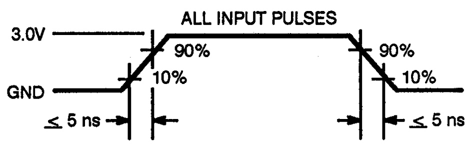
Notes:

1. Tested on a sample basis.

AC Test Loads and Waveforms

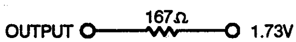


(a) (b) 1460-3



1460-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [2]

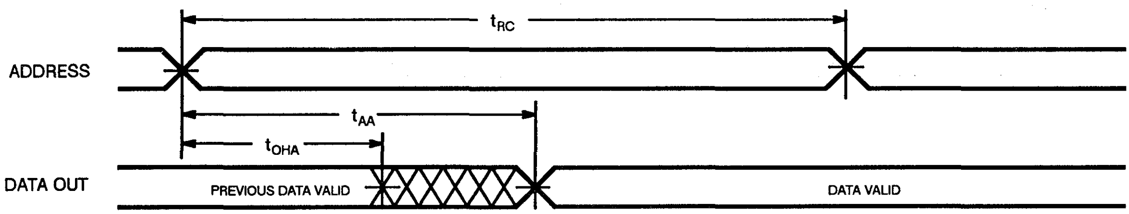
Parameters	Description	1460PS-35 1460PF-35 Min.	1460PS-35 1460PF-35 Max.	1460PS-45 1460PF-45 Min.	1460PS-45 1460PF-45 Max.	1460PS-55 1460PF-55 Min.	1460PS-55 1460PF-55 Max.	1460PS-70 1460PF-70 Min.	1460PS-70 1460PF-70 Max.	Units
READ CYCLE										
t_{RC}	Read Cycle Time	35		45		55		70		ns
t_{AA}	Address to Data Valid		35		45		55		70	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{AMS}	$\overline{MS}$ LOW to Data Valid		35		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[3]		15		25		25		30	ns
t_{LZMS}	$\overline{MS}$ LOW to Low Z[4]	5		5		5		5		ns
t_{HZMS}	$\overline{MS}$ HIGH to High Z[3, 4]		15		20		25		35	ns
WRITE CYCLE [5]										
t_{WC}	Write Cycle Time	35		45		55		70		ns
t_{SMS}	$\overline{MS}$ LOW to Write End	30		40		50		60		ns
t_{AW}	Address Set-Up to Write End	30		40		50		60		ns
t_{HA}	Address Hold from Write End	2		5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	25		30		40		55		ns
t_{SD}	Data Set-Up to Write End	15		20		25		30		ns
t_{HD}	Data Hold from Write End	2		2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[3]		15		20		25		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		3		ns

Notes:

2. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
3. t_{HZOE}, t_{HZMS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
4. At any given temperature and voltage condition, t_{HZMS} is less than t_{LZMS} for any given device. These parameters are guaranteed and not 100% tested.
5. The internal write time of the memory is defined by the overlap of $\overline{MS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected. $\overline{OE}$, $\overline{MS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{MS}$ transition low.
9. Data I/O is HIGH impedance if $\overline{OE}$ = V_{IH}.
10. If $\overline{MS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

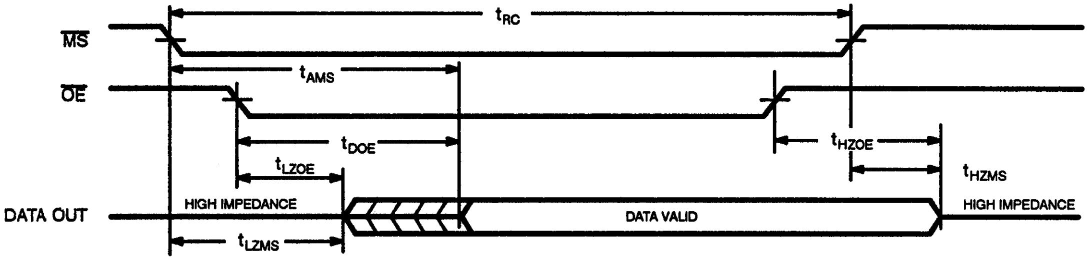
Read Cycle No. 1[7, 8]



1460-5

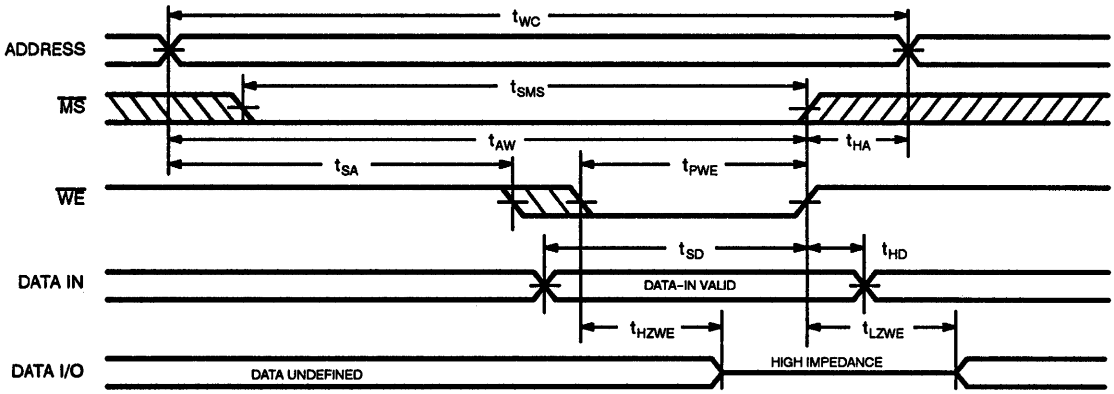
Switching Waveforms (continued)

Read Cycle No. 2 [6, 8]



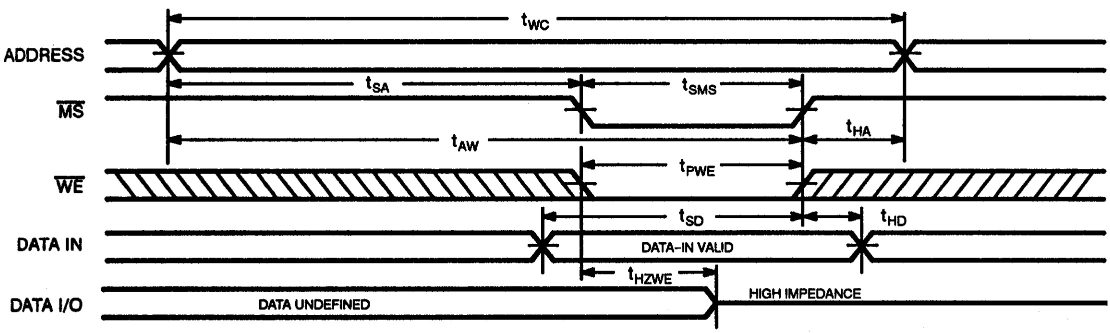
1460-6

Write Cycle No. 1 ($\overline{WE}$ Controlled) [5, 9]



1460-7

Write Cycle No. 2 ($\overline{MS}$ Controlled) [5, 9, 10]



1460-8

Truth Table

$\overline{MS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Document #: 38-M-00004-A

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
35	CYM1460PS-35C	PS05	Commercial
	CYM1460PF-35C	PF03	
45	CYM1460PS-45C	PS05	Commercial
	CYM1460PF-45C	PF03	
55	CYM1460PS-55C	PS05	Commercial
	CYM1460PF-55C	PF03	
70	CYM1460PS-70C	PS05	Commercial
	CYM1460PF-70C	PF03	

8

CYPRESS SEMICONDUCTOR

CYM1461

512K x 8 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 70 ns**
- **Low active power**
  - **— 825 mW (max.)**
- **Double-sided SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile version (PF)**
  - **— Max. height of .315 in.**
- **Small footprint SIP version (PS)**
  - **— PCB layout area of 1.5 sq. in.**
- **2V data retention (L version)**

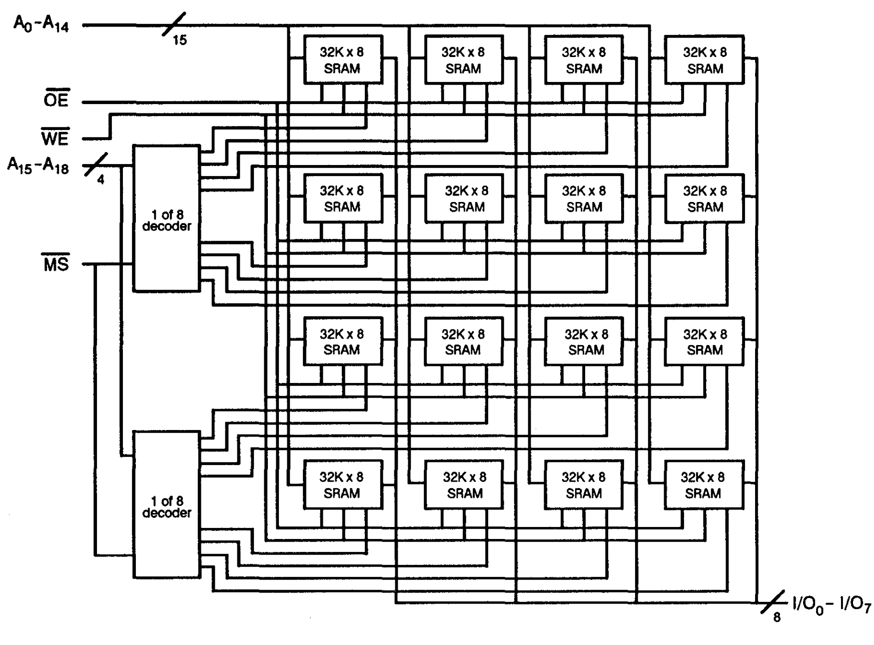
Functional Description

The CYM1461 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed from sixteen 32K x 8 SRAMs in plastic surface mount packages on an epoxy laminate board with pins. Two choices of pins are available for vertical (PS) or horizontal (PF) through-hole mounting. On-board decoding selects one of the sixteen SRAMs from the high-order address lines keeping the remaining fifteen devices in standby mode for minimum power consumption.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{MS}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins is written into the memory location specified on the address pins. Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{MS}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the content of the location addressed by the information on the address pins is present on the eight data input/output pins.

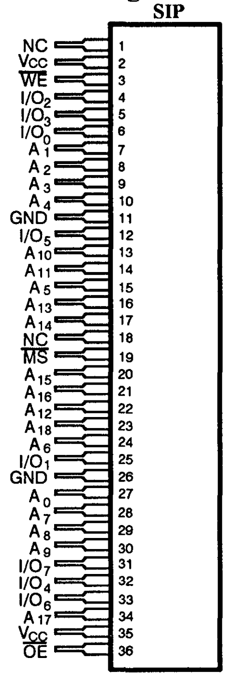
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1461-1

Pin Configuration



1461-2

Selection Guide

	1461PS-70 1461PF-70	1461PS-85 1461PF-85	1461PS-100 1461PF-100
Maximum Access Time (ns)	70	85	100
Maximum Operating Current (mA)	150	150	150
Maximum Standby Current (mA)	50	50	50

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... 0°C to +70°C

Supply Voltage to Ground Potential .... –0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State .... –0.3V to +7.0V

DC Input Voltage .... –0.3V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1461		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–20	+20	µA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$ Output Disabled	–20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., $\overline{MS} \leq V_{IL}$ I_{OUT} = 0 mA		150	mA
I_{SB1}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS} \geq V_{IH}$, Min. Duty Cycle = 100%		50	mA
I_{SB2}	Automatic $\overline{MS}$ Power-Down Current	Max. V_{CC}, $\overline{MS} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V		32	mA

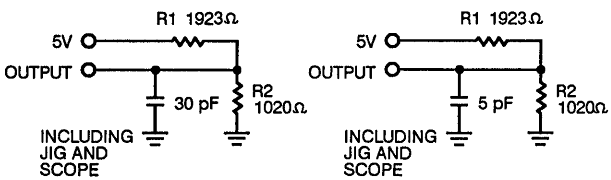
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	100	pF
C_{OUT}	Output Capacitance		100	pF

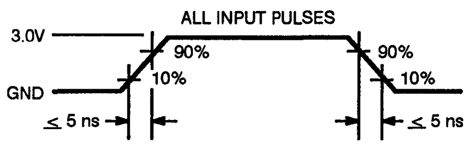
Notes:

1. Tested on a sample basis.

AC Test Loads and Waveforms

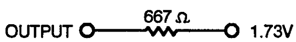


(a) (b) 1461-3



1461-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [3]

Parameters	Description	1461PS-70 1461PF-70		1461PS-85 1461PF-85		1461PS-100 1461PF-100		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	70		85		100		ns
t_{AA}	Address to Data Valid		70		85		100	ns
t_{OHA}	Data Hold from Address Change	20		20		20		ns
t_{AMS}	$\overline{MS}$ LOW to Data Valid		70		85		100	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		40		50		55	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[4]		35		35		40	ns
t_{LZMS}	$\overline{MS}$ LOW to Low Z[5]	5		5		5		ns
t_{HZMS}	$\overline{MS}$ HIGH to High Z[4, 5]		35		35		40	ns
WRITE CYCLE [6]								
t_{WC}	Write Cycle Time	70		85		100		ns
t_{SMS}	$\overline{MS}$ LOW to Write End	70		80		85		ns
t_{AW}	Address Set-Up to Write End	70		80		85		ns
t_{HA}	Address Hold from Write End	5		5		5		ns
t_{SA}	Address Set-Up to Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	60		65		65		ns
t_{SD}	Data Set-Up to Write End	35		40		45		ns
t_{HD}	Data Hold from Write End	5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]		30		35		40	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	5		5		5		ns

Notes:

2. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
3. t_{HZOE}, t_{HZMS}, and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
4. At any given temperature and voltage condition, t_{HZMS} is less than t_{LZMS} for any given device. These parameters are guaranteed and not 100% tested.
5. The internal write time of the memory is defined by the overlap of $\overline{MS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected. $\overline{OE}$, $\overline{MS} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{MS}$ transition low.
9. Data I/O is HIGH impedance if $\overline{OE} = V_{IH}$.

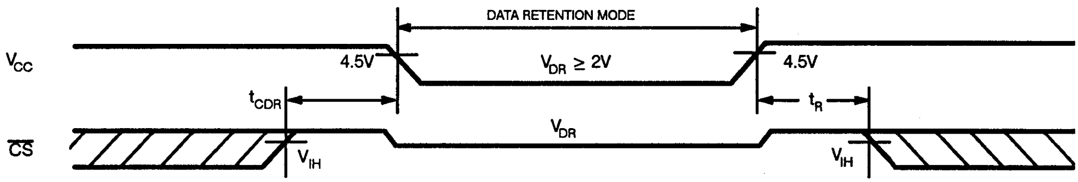
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1461		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			300	mA
t_{CDR} [6]	Chip Deselect to Data Retention Time		0		ns
t_R [6]	Operation Recovery Time		t_{RC} [7]		ns

Notes:

10. t_{RC} = Read Cycle Time.
11. If $\overline{MS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
12. Guaranteed, not tested.

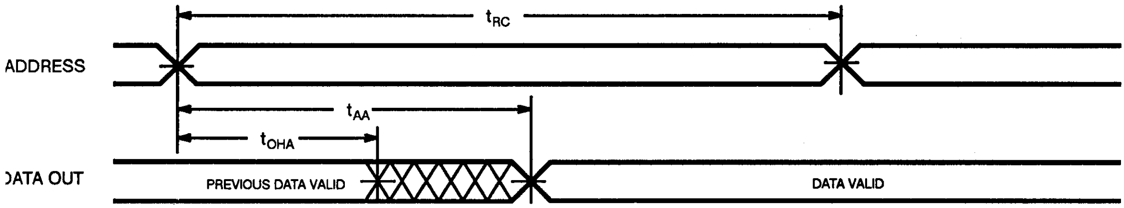
Data Retention Waveform



1461-5

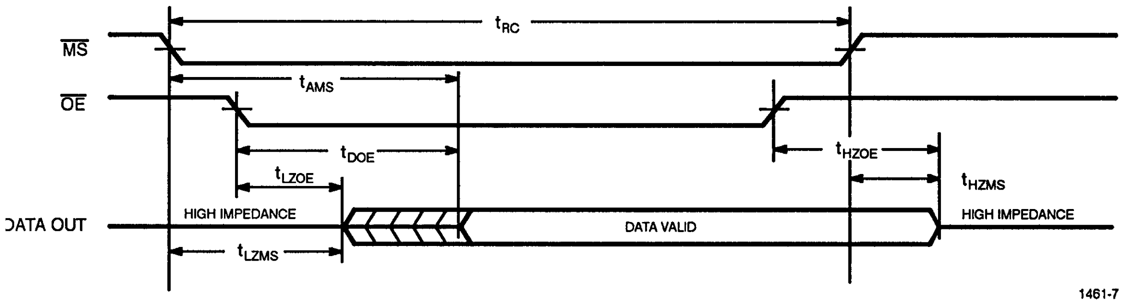
Switching Waveforms

Read Cycle No. 1[8, 9]



1461-6

Read Cycle No. 2 [9, 10, 11]

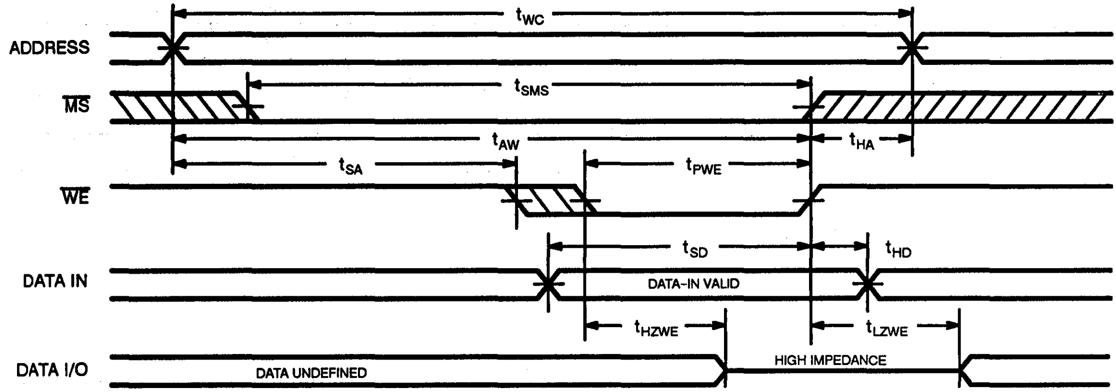


1461-7

8

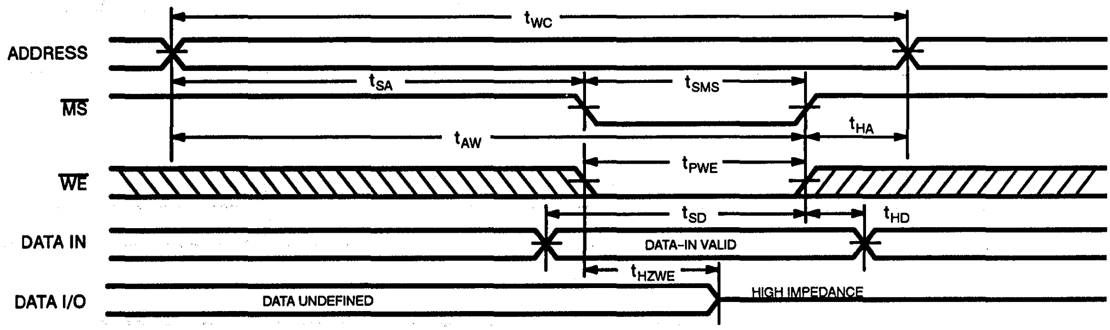
Switching Waveforms (continued)

Write Cycle No. 2[9, 10]



1461-8

Write Cycle No. 2 ($\overline{MS}$ Controlled)[11, 12]



1461-9

Truth Table

$\overline{MS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Document #: 38-M-00005-A

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
70	CYM1461PS-70C	PS01	Commercial
	CYM1461LPS-70C		
	CYM1461PF-70C	PF01	
	CYM1461LPF-70C		
85	CYM1461PS-85C	PS01	Commercial
	CYM1461LPS-85C		
	CYM1461PF-85C	PF01	
	CYM1461LPF-85C		
100	CYM1461PS-100C	PS01	Commercial
	CYM1461LPS-100C		
	CYM1461PF-100C	PF01	
	CYM1461LPF-100C		

8

This is a partial data sheet. For complete data sheet, see Section 2, Static RAMs.

CYPRESS SEMICONDUCTOR

PRELIMINARY **CYM1464**

512K x 8 SRAM Module

Features

- High-density 4-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 45 ns
- Low active power
  - 1.65W (max.)
- JEDEC-compatible pinout
- 32-pin, 0.6-inch-wide DIP package
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of .34 in.
- Small PCB footprint
  - 0.98 sq. in.

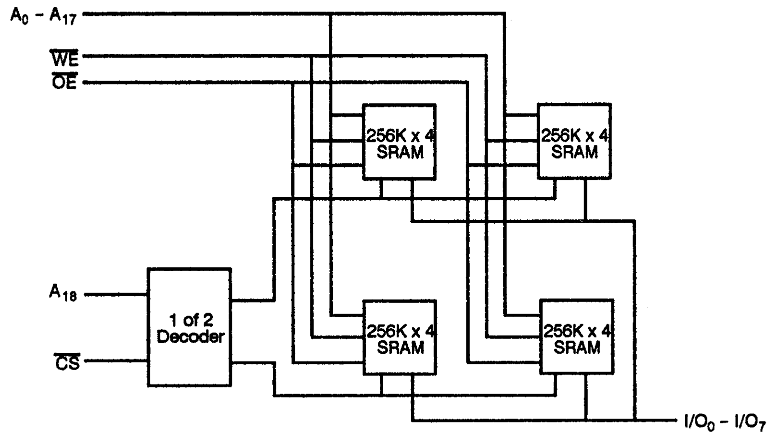
Functional Description

The CYM1464 is a high-performance 4-megabit static RAM module organized as 512K words by 8 bits. This module is constructed using four 256K x 4 static RAMs in SOJ packages mounted on an epoxy laminate substrate with pins. A decoder is used to interpret the higher-order address (A_{18}) and to select two of the four RAMs.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the eight input/output pins (I/O_0 through I/O_7) of the device is written into the memory location specified on the address pins (A_0 through A_{18}). Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{18}) will appear on the eight appropriate data input/output pins (I/O_0 through I/O_7).

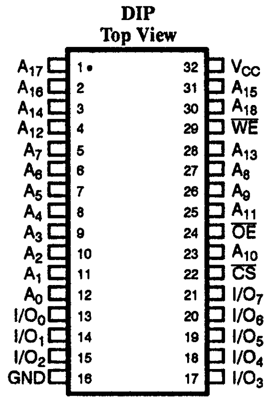
The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

Logic Block Diagram



1464-1

Pin Configuration



1464-2

Selection Guide

	1464PD-45	1464PD-55	1464PD-70
Maximum Access Time (ns)	45	55	70
Maximum Operating Current (mA)	300	300	300
Maximum Standby Current (mA)	240	240	240

CYPRESS SEMICONDUCTOR

CYM1540

256K x 9 Buffered SRAM Module with Separate I/O

Features

- **High-density 2-megabit SRAM module with parity**
- **High-speed CMOS SRAMs**
  - **Access time of 30 ns**
- **Buffered address and control inputs**
- **Low active power**
  - **6.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .52 in.**
- **Small PCB footprint**
  - **1.6 sq. in.**

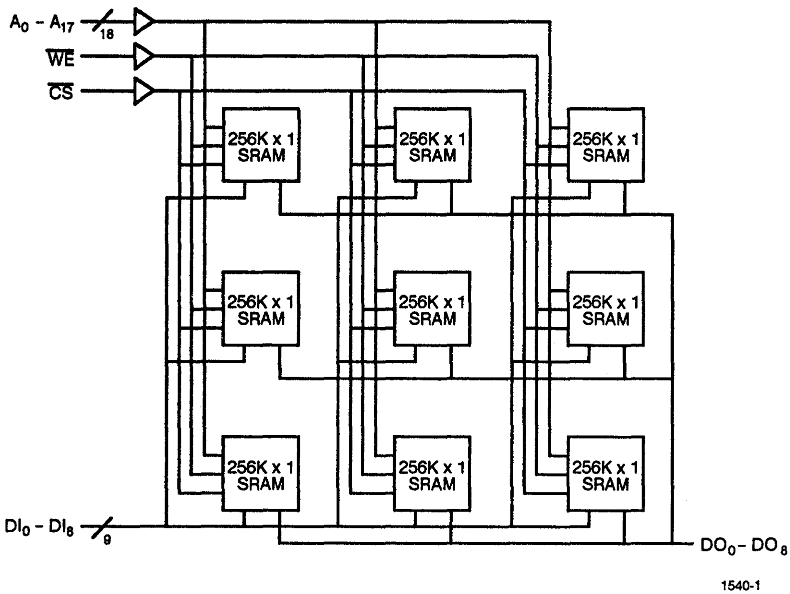
Functional Description

The CYM1540 is a very high performance 2-megabit static RAM module organized as 256K words by 9 bits. This module is constructed using nine 256K x 1 static RAMs in SOJ packages mounted on an epoxy laminate board with pins. Input buffers are provided on the address and control lines to reduce input capacitance and loading.

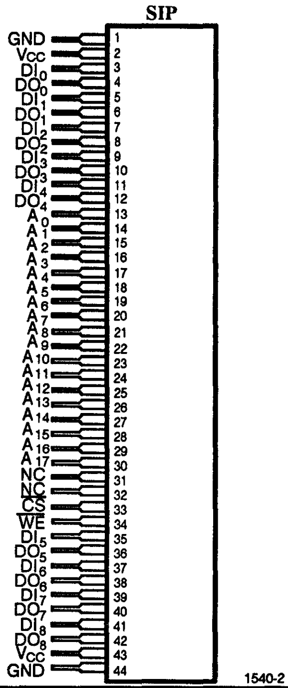
Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the data input pins (DI_0 through DI_8) of the device is written into the memory location specified on the address pins (A_0 through A_{17}). Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{17}) will appear on the appropriate data output pins (DO_0 through DO_8). The data output pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or when write enable ($\overline{WE}$) is LOW.

8

Logic Block Diagram



Pin Configuration



Selection Guide

	1540PF-30 1540PS-30	1540PF-35 1540PS-35	1540PF-45 1540PS-45
Maximum Access Time (ns)	30	35	45
Maximum Operating Current (mA)	1125	1125	1125
Maximum Standby Current (mA)	350	350	350

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −45°C to + 125°C

Ambient Temperature with Power Applied .... −10°C to +85°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1540PS		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IHA}	Input HIGH Voltage $A_0 - A_{17}$, $\overline{CS}$, $\overline{WE}$		2.0	6.0	V
V_{IHD}	Input HIGH Voltage $DI_0 - DI_8$		2.2	6.0	V
V_{ILA}	Input LOW Voltage $A_0 - A_{17}$, $\overline{CS}$, $\overline{WE}$			0.8	V
V_{ILD}	Input LOW Voltage $DI_0 - DI_8$		−0.5	0.8	V
V_{IK}	Input Clamp Level $A_0 - A_{17}$, $\overline{CS}$, $\overline{WE}$	V_{CC} = Min., I_{IN} = −18 mA		−1.2	V
I_{IL}	Input Load Current	GND $\leq V_I \leq V_{CC}$	−10	+10	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	−10	+10	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		1125	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [1]	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		350	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [1]	V_{CC} = Max., $\overline{CS} \geq V_{CC}$ − 0.2V, $V_{IN} \geq V_{CC}$ − 0.2V or $V_{IN} \leq$ 0.2V		230	mA

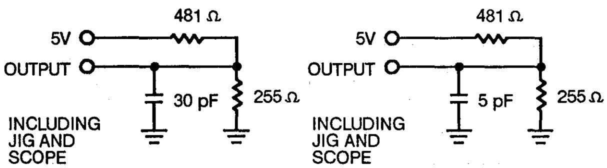
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		15	pF

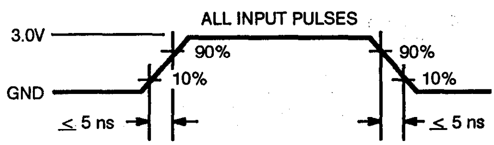
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms



(a) (b) 1540-3



1540-4

Switching Characteristics Over the Operating Range [3]

Parameters	Description	1540PF-30 1540PS-30		1540PF-35 1540PS-35		1540PF-45 1540PS-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	30		35		45		ns
t_{AA}	Address to Data Valid		30		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		30		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [4]	3	20	3	20	3	25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	3		3		3		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		30		35		45	ns
WRITE CYCLE [5]								
t_{WC}	Write Cycle Time	30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		35		ns
t_{AW}	Address Set-Up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	4		4		5		ns
t_{SA}	Address Set-Up from Write Start	5		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-Up to Write End	20		25		35		ns
t_{HD}	Data Hold from Write End	5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [4]	3	20	3	25	3	30	ns

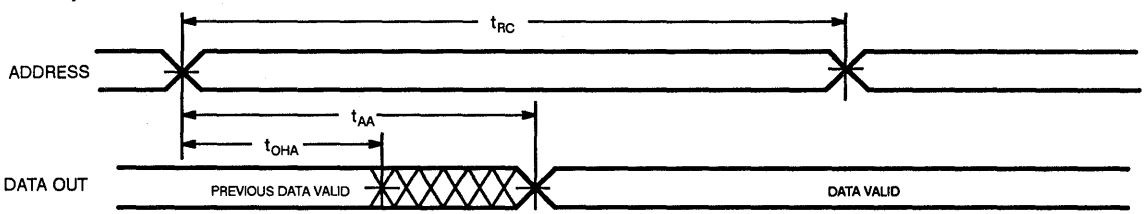
Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{CS}$ transition low.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

8

Switching Waveforms

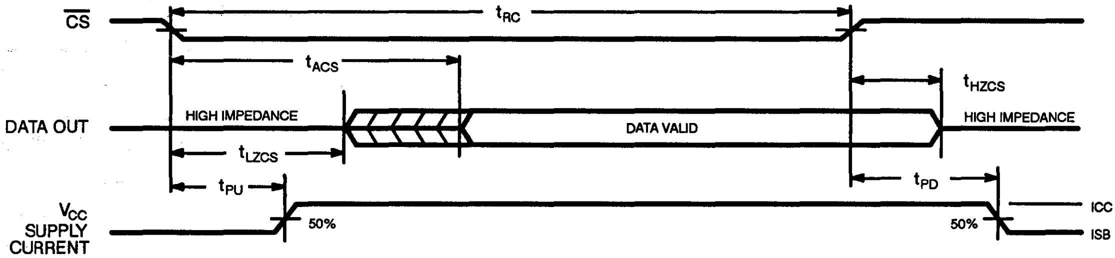
Read Cycle No. 1 [6, 7]



1540-5

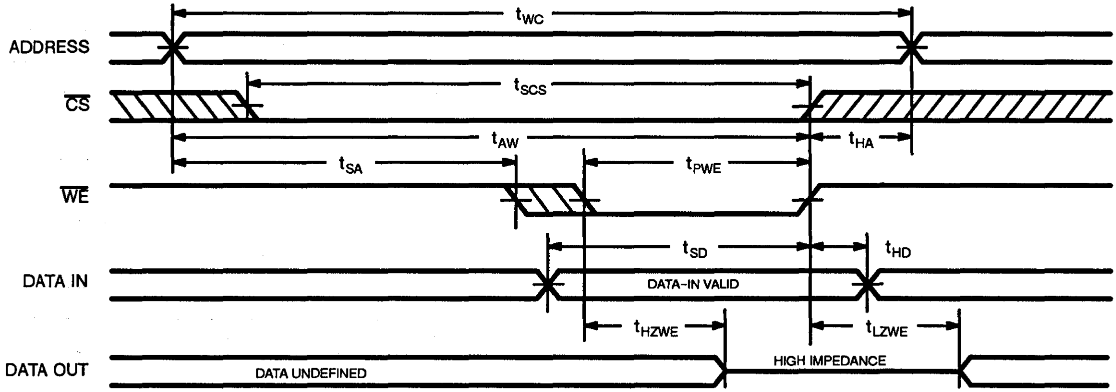
Switching Waveforms (continued)

Read Cycle No. 2[6, 8]



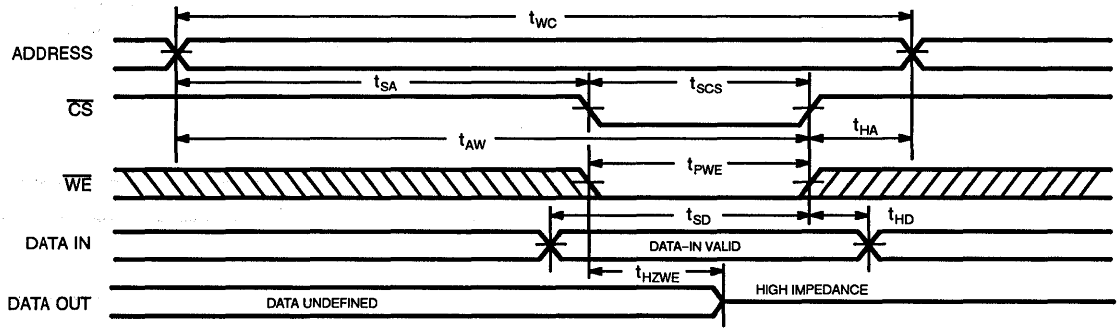
1540-6

Write Cycle No. 1 (WE Controlled)[5]



1540-7

Write Cycle No. 2 (CS Controlled)[5, 9]



1540-8

Truth Table

$\overline{CS}$	$\overline{WE}$	Data In	Data Out	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	X	Data Out_{0-8}	Read
L	L	Data In_{0-8}	High Z	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
30	CYM1540PF-30C	PF02	Commercial
	CYM1540PS-30C	PS04	
35	CYM1540PF-35C	PF02	Commercial
	CYM1540PS-35C	PS04	
45	CYM1540PF-45C	PF02	Commercial
	CYM1540PS-45C	PS04	

8

This is a partial data sheet. For complete data sheet, see Section 2, Static RAMs.

CYPRESS SEMICONDUCTOR

CYM1610

16K x 16 Static RAM Module

Features

- High-density 256-kbit SRAM module
- High-speed CMOS SRAMs
  - Access time of 12 ns
- Low active power
  - 3W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of .215 in.
- Small PCB footprint
  - 1.2 sq. in.
- JEDEC-defined pinout
- Independent byte select
- 2V data retention (L version)

Functional Description

The CYM1610 is a high-performance 256-kbit static RAM module organized as 16K words by 16 bits. This module is constructed from four 16K x 4 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins.

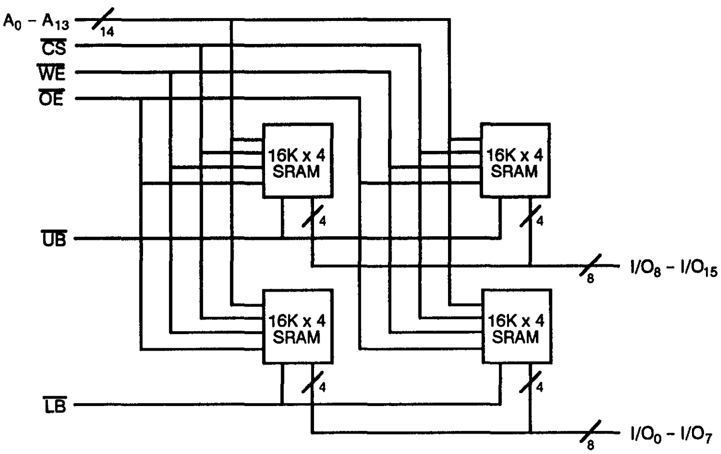
Selecting the device is achieved by a chip select input pin as well as two byte select pins ($\overline{UB}$, $\overline{LB}$) for independently selecting upper or lower byte for read or write operations.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and write enable ($\overline{WE}$) inputs are LOW. Data on the input/output pins of the selected byte ($I/O_8 - I/O_{15}$, $I/O_0 - I/O_7$) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

The input/output pins remain in a high-impedance state when chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

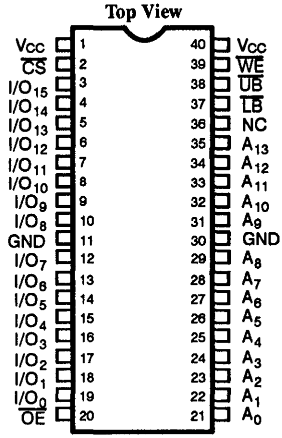
Logic Block Diagram



1610-1

Pin Configuration

DIP
Top View



1610-2

Selection Guide

		1610HD-12	1610HD-15	1610HD-20	1610HD-25	1610HD-35	1610HD-45	1610HD-50
Maximum Access Time (ns)		12	15	20	25	35	45	50
Maximum Operating Current (mA)	Com'l	550	550	330	330	330	330	330
	Mil		550	550	360	330	330	330
Maximum Standby Current (mA)	Com'l	250	250	60	60	60	60	60
	Mil		250	250	60	60	60	60

Shaded area contains preliminary information.

CYM1611

CYPRESS SEMICONDUCTOR

16K x 16 Static RAM Module

Features

- **High-density 256-kbit SRAM module**
- **High speed**
  - **Access time of 12 ns**
- **16-bit-wide organization**
- **Low active power**
  - **1.8W (max.) at 25 ns**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of 0.5 in.**
- **Small PCB footprint**
  - **0.4 sq. in.**
- **2V data retention (L version)**

Functional Description

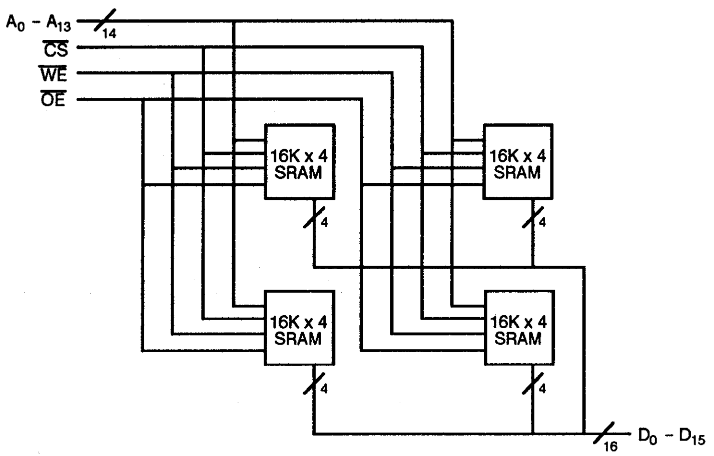
The CYM1611 is a very high performance 256-kbit static RAM module organized as 16K words by 16 bits. The module is constructed from four 16K x 4 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. A vertical DIP format minimizes board space (footprint = 0.4 sq. in.) while still keeping a maximum height of 0.5 in.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (D_0 through D_{15}) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the sixteen data input/output pins.

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

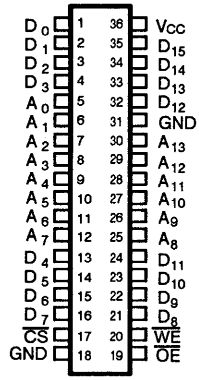
Logic Block Diagram



1611-1

Pin Configuration

VDIP
Top View



1611-2

Selection Guide

		1611HV-12	1611HV-15	1611HV-20	1611HV-25	1611HV-30	1611HV-35	1611HV-45
Maximum Access Time (ns)		12	15	20	25	30	35	45
Maximum Operating Current (mA)	Commercial	550	550	330	330	330	330	330
	Military		550	550	330	330	330	330
Maximum Standby Current (mA)	Commercial	250	250	80	80	80	80	80
	Military		250	250	80	80	80	80

Shaded area contains preliminary information.

8

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... -65°C to +150°C

Ambient Temperature with Power Applied .... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... -0.5V to +7.0V

DC Input Voltage .... -0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	-55°C to +125°C	5V ± 10%

Electrical Characteistics Over the Operating Range

Parameters	Description	Test Conditions	CYM1611HV-12 CYM1611HV-15 CYM1611HV-20M		CYM1611HV-20C CYM1611HV-25 CYM1611HV-30 CYM1611HV-35 CYM1611HV-45		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	-20	+20	-20	+20	µA
I_{OZ}	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output Disabled	-20	+20	-20	+20	µA
I_{OS}	Output Short Circuit Current [1]	V_{CC} = Max., V_{OUT} = GND		-350		-350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		550		330	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}; $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		250		80	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	Max. V_{CC}; $\overline{CS} \geq V_{CC}$ - 0.3V, $V_{IN} \geq V_{CC}$ - 0.3V or $V_{IN} \leq$ 0.3V				80	mA

Shaded area contains preliminary information.

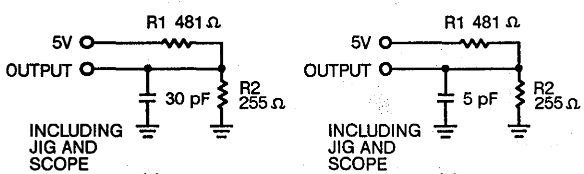
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	40	pF
C_{OUT}	Output Capacitance		15	pF

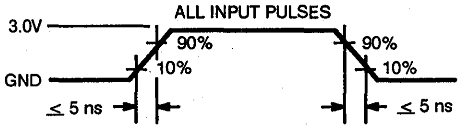
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. Tested on a sample basis.

AC Test Loads and Waveforms

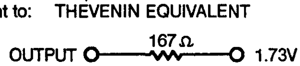


(a) (b) 1611-3



1611-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [2]

Parameters	Description	CYM1611HV-12		CYM1611HV-15		CYM1611HV-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		2		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [4]		8		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [5]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [4, 5]		8		8		8	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE [6]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Set-Up to Write End	10		12		15		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [4]	3		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0	7	0	7	0	7	ns

Shaded area contains preliminary information.

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZOE}, t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected. $\overline{OE}$, $\overline{CS}$ = V_{IL}.
9. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
10. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

8

Switching Characteristics Over the Operating Range (continued) [2]

Parameters	Description	1611HV-25		1611HV-30		1611HV-35		1611HV-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_{AA}	Address to Data Valid		25		30		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[4]		10		15		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[5]	5		10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4, 5]		10		15		15		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		30		35		45	ns
WRITE CYCLE [6]										
t_{WC}	Write Cycle Time	20		25		25		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	13		20		20		25		ns
t_{HD}	Data Hold from Write End	2		2		2		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	7	0	12	0	12	0	15	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		5		5		5		ns

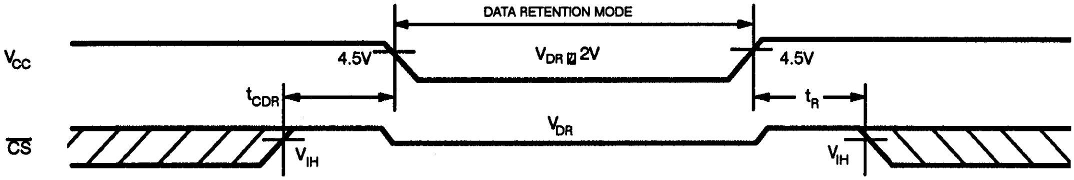
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1611		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention of Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			4	mA
t_{CDR}	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		t_{RC} [11]		ns
I_{LI}	Input Leakage Current			5	µA

Note:

11. t_{RC} = Read Cycle Time.

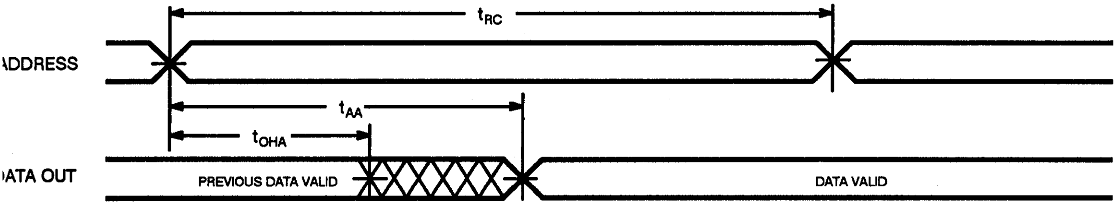
Data Retention Waveform



1611-5

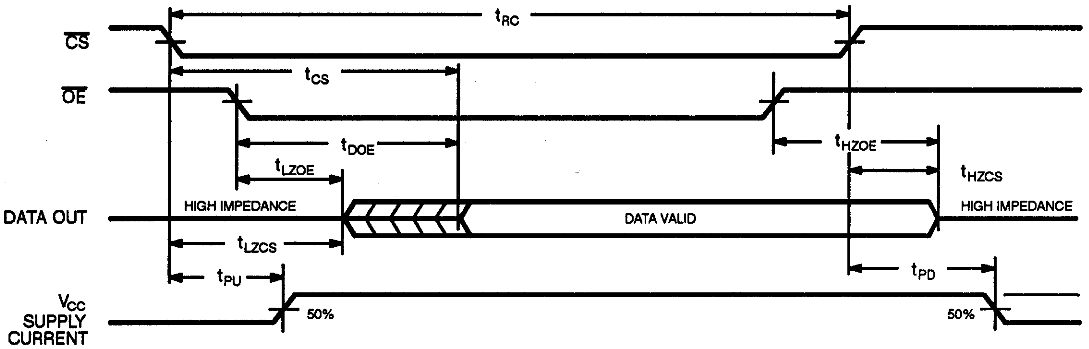
Switching Waveforms

Read Cycle No. 1[7, 8]



1611-6

Read Cycle No. 2[7, 9]

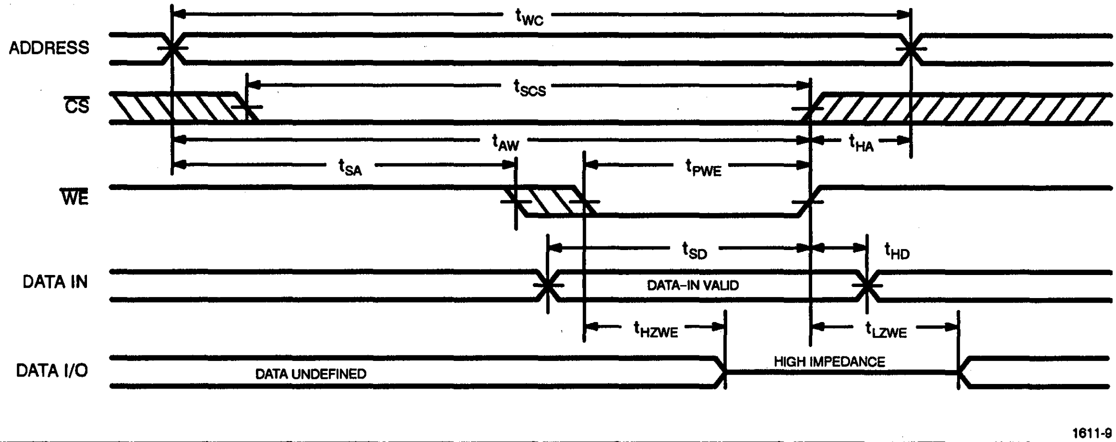


1611-7

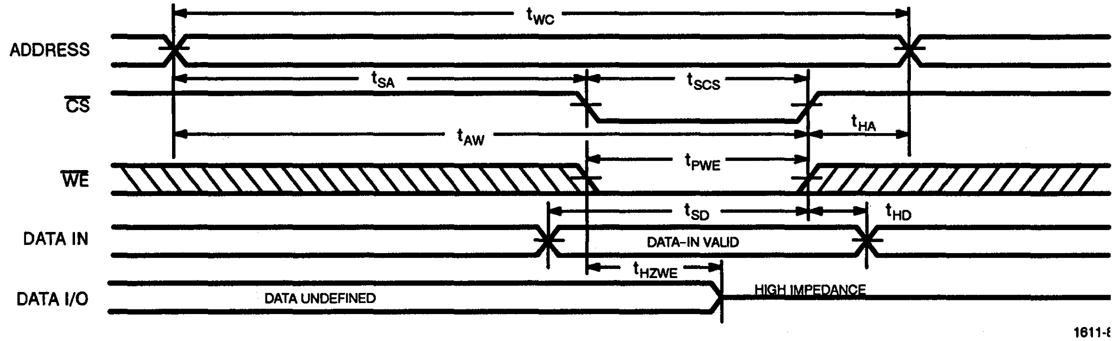
8

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled) [6, 10]



Write Cycle No. 2 ($\overline{CS}$ Controlled) [6, 10, 12]



Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
12	CYM1611HV-12C	HV01	Commercial
15	CYM1611HV-15C	HV01	Commercial
	CYM1611HV-15M	HV01	Military
20	CYM1611HV-20C	HV01	Commercial
	CYM1611LHV-20C	HV01	
	CYM1611HV-20M	HV01	Military
25	CYM1611HV-25C	HV01	Commercial
	CYM1611LHV-25C	HV01	
	CYM1611HV-25M	HV01	Military
	CYM1611LHV-25M	HV01	
30	CYM1611HV-30C	HV01	Commercial
	CYM1611LHV-30C	HV01	
	CYM1611HV-30M	HV01	Military
	CYM1611LHV-30M	HV01	
35	CYM1611HV-35C	HV01	Commercial
	CYM1611LHV-35C	HV01	
	CYM1611HV-35M	HV01	Military
	CYM1611LHV-35M	HV01	
45	CYM1611HV-45C	HV01	Commercial
	CYM1611LHV-45C	HV01	
	CYM1611HV-45M	HV01	Military
	CYM1611LHV-45M	HV01	

Shaded area contains preliminary information.

Document #: 38-M-00007-A

CYPRESS SEMICONDUCTOR

CYM1620

64K x 16 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 30 ns**
- **40-pin, 0.6-inch-wide DIP package**
- **JEDEC-compatible pinout**
- **Low active power**
  - **— 1.9W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Commercial and military temperature ranges**

Functional Description

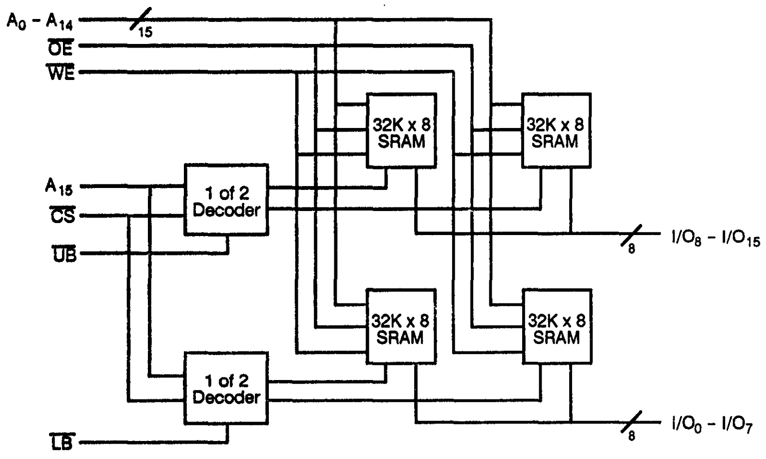
The CYM1620 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 32K x 8 static RAMs in leadless chip carriers mounted onto a double-sided multilayer ceramic substrate. A decoder is used to interpret the higher-order address A_{15} and select one of the two pairs of RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins of the selected byte (I/O_8 - I/O_{15}, I/O_0 - I/O_7) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

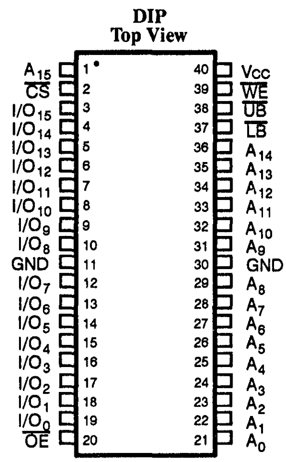
The input/output pins remain in a high-impedance state when chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



1620-1

Pin Configuration



1620-2

Selection Guide

		1620HD-30	1620HD-35	1620HD-45	1620HD-55
Maximum Access Time (ns)		30	35	45	55
Maximum Operating Current (mA)	Commercial	340	340	340	340
	Military			340	340
Maximum Standby Current (mA)	Commercial	140	140	140	140
	Military			140	140

CYPRESS SEMICONDUCTOR

64K x 16 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 20 ns**
- **Customer configurable**
  - **x4, x8, x16**
- **Low active power**
  - **6.8W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .270 in.**
- **Small PCB footprint**
  - **2 sq. in.**
- **2V data retention (L version)**

Functional Description

The CYM1621 is a high-performance 1-megabit static RAM module organized as 64K words by 16 bits. This module is constructed from sixteen 64K x 1 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. Four separate $\overline{CS}$ pins are used to control each 4-bit nibble of the 16-bit word. This feature permits the user to configure this module as either 256K x 4, 128K x 8 or 64K x 16 organization through external decoding and appropriate pairing of the outputs.

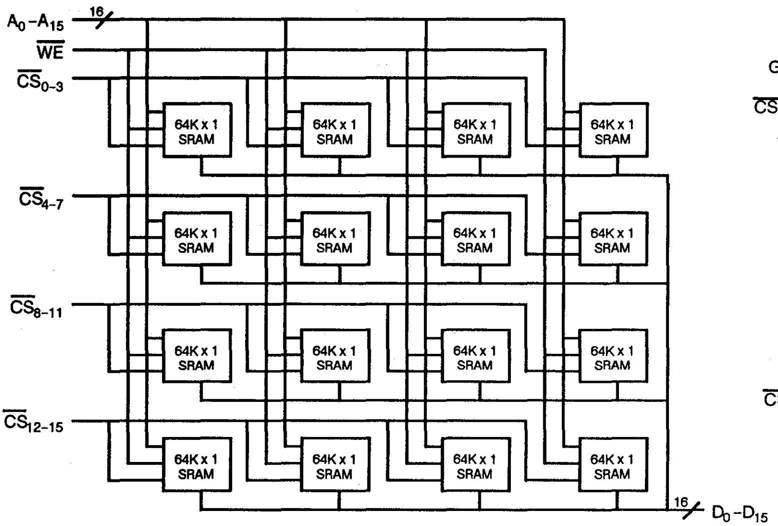
Writing to the device is accomplished when the chip select ($\overline{CS}_{xx}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the data lines (D_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip select ($\overline{CS}_{xx}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data lines (D_X).

The data output is in the high-impedance state when chip enable ($\overline{CS}_{xx}$) is HIGH or write enable ($\overline{WE}$) is LOW.

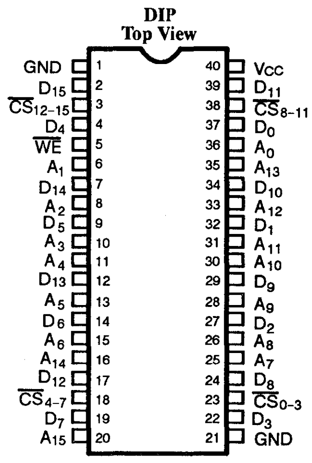
Power is consumed in each 4-bit nibble only when the appropriate $\overline{CS}$ is enabled, thus reducing power in the x4 or x8 mode.

Logic Block Diagram



1621-1

Pin Configuration



1621-2

8

Selection Guide

		1621HD-20	1621HD-25	1621HD-30	1621HD-35	1621HD-45
Maximum Access Time (ns)		20	25	30	35	45
Maximum Operating Current (mA)	Commercial	1250	1250	1250	1250	1250
	Military		1250	1250	1250	1250
Maximum Standby Current (mA)	Commercial	320	320	320	320	320
	Military		320	320	320	320

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... -65°C to +150°C

Ambient Temperature with Power Applied .... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... -0.5V to +7.0V

DC Input Voltage .... -0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military[4]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1621HD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		-0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	-20	+20	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	-20	+20	µA
I_{OS}	Output Short Circuit Current[1]	V_{CC} = Max., V_{OUT} = GND		-350	mA
I_{CCx16}	V_{CC} Operating Supply Current by 16 mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_{xx} \leq V_{IL}$		1250	mA
I_{CCx8}	V_{CC} Operating Supply Current by 8 mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_{xx} \leq V_{IL}$		850	mA
I_{CCx4}	V_{CC} Operating Supply Current by 4 mode	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}_{xx} \leq V_{IL}$		650	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}_{xx} \geq V_{IH}$, Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}_{xx} \geq V_{CC}$ - 0.3V, $V_{IN} \geq V_{CC}$ - 0.3V or $V_{IN} \leq$ 0.3V		320	mA

Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	130	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested initially and after any design or process changes that may affect these parameters.
4. T_A is the "instant on" case temperature.

Switching Characteristics Over the Operating Range [5]

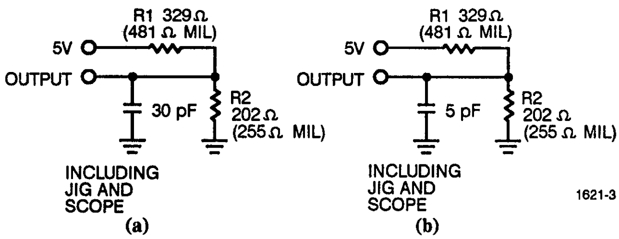
Parameters	Description	1621HD-20		1621HD-25		1621HD-30		1621HD-35		1621HD-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	20		25		30		35		45		ns
t_{AA}	Address to Data Valid		20		25		30		35		45	ns
t_{OHA}	Output Hold from Address Change	5		5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		25		30		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[7]	5		5		5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6, 7]		10		20		25		30		30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		20		25		30		35		35	ns
WRITE CYCLE [8]												
t_{WC}	Write Cycle Time	20		25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	15		22		25		30		40		ns
t_{AW}	Address Set-Up to Write End	15		22		25		30		40		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	2		2		3		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	16		20		20		25		30		ns
t_{SD}	Data Set-Up to Write End	10		15		20		20		25		ns
t_{HD}	Data Hold from Write End	2		3		5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	5		5		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]	0	20	0	20	0	25	0	25	0	25	ns

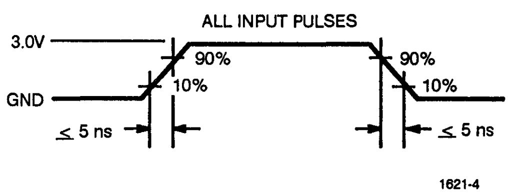
Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS} = V_{IL}$.
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

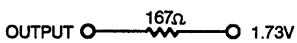
8

AC Test Loads and Waveforms

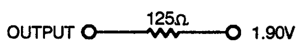




Equivalent to: THÉVENIN EQUIVALENT



Military



Commercial

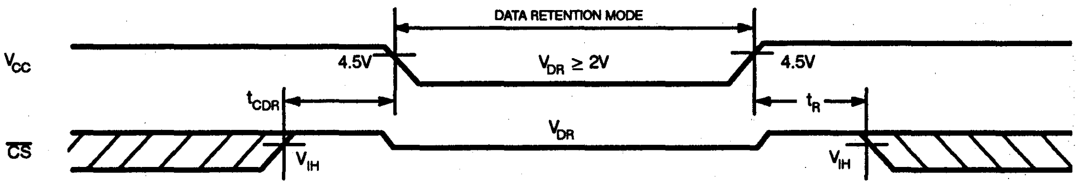
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1621 Min.	CYM1621 Max.	Units
V_{DR}	V_{CC} for Retention of Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			16	mA
t_{CDR}	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		t_{RC} [12]		ns
I_{LI}	Input Leakage Current			10	μA

Notes:

12. t_{RC} = Read Cycle Time.

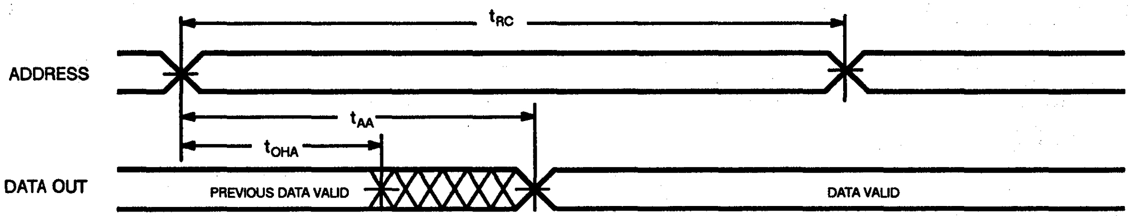
Data Retention Waveform



1621-5

Switching Waveforms [10]

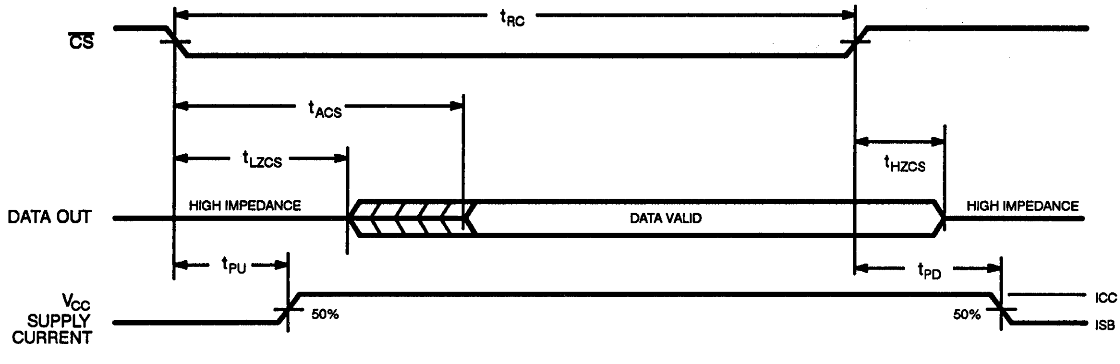
Read Cycle No. 1[9, 10]



1621-6

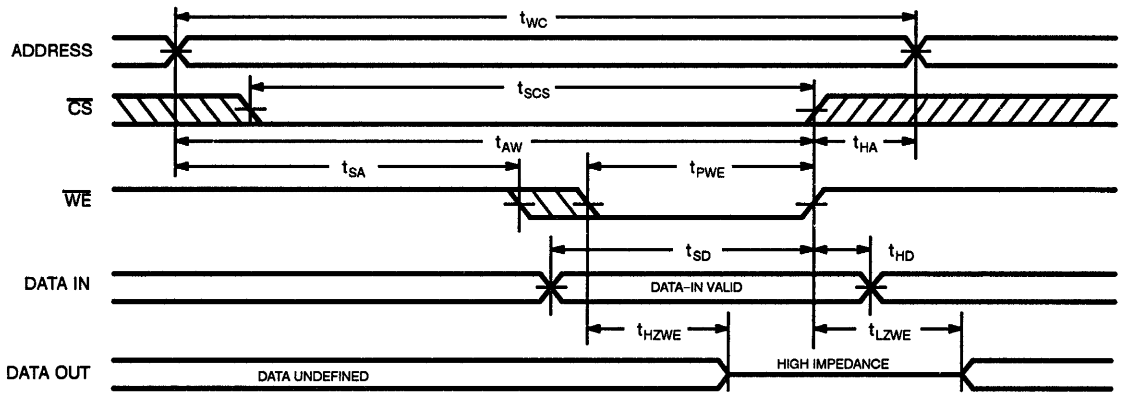
Switching Waveforms (continued)

Read Cycle No. 2 [9, 10]



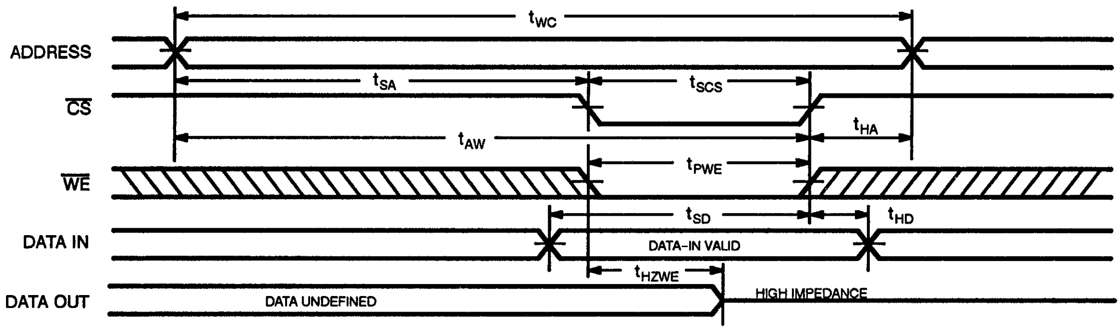
1621-7

Write Cycle No. 1 ($\overline{WE}$ Controlled) [8]



1621-8

Write Cycle No. 2 ($\overline{CS}$ Controlled) [8, 11]



1621-9

Truth Table

$\overline{CS}_{xx}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
20	CYM1621HD-20C	HD02	Commercial
	CYM1621LHD-20C	HD02	
25	CYM1621HD-25C	HD02	Commercial
	CYM1621LHD-25C	HD02	
	CYM1621HD-25MB	HD02	Military
	CYM1621LHD-25MB	HD02	
30	CYM1621HD-30C	HD02	Commercial
	CYM1621LHD-30C	HD02	
	CYM1621HD-30MB	HD02	Military
	CYM1621LHD-30MB	HD02	
35	CYM1621HD-35C	HD02	Commercial
	CYM1621LHD-35C	HD02	
	CYM1621HD-35MB	HD02	Military
	CYM1621LHD-35MB	HD02	
45	CYM1621HD-45C	HD02	Commercial
	CYM1621LHD-45C	HD02	
	CYM1621HD-45MB	HD02	Military
	CYM1621LHD-45MB	HD02	

Document #: 38-M-00009-A

CYPRESS SEMICONDUCTOR

64K x 16 SRAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 25 ns**
- **Low active power**
  - **— 2.2W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Pinout-compatible with CYM1611 and CYM1624**
- **Low profile**
  - **— Max. height of .50 in.**
- **Small PCB footprint**
  - **— 0.5 sq. in.**

Functional Description

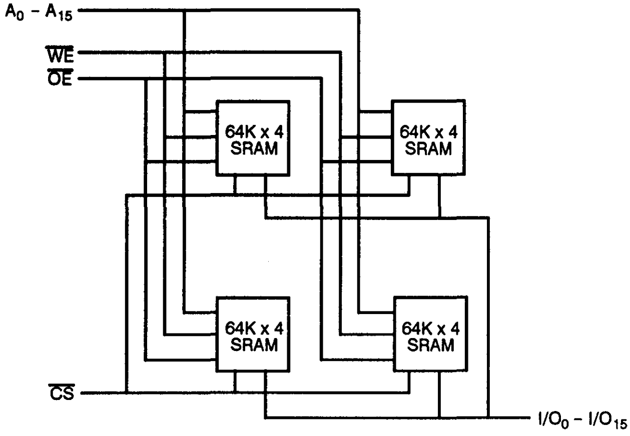
The CYM1622 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. This module is constructed using four 64K x 4 static RAMs in LCC packages mounted on a ceramic substrate with pins. The pinout of this module is compatible with two other Cypress modules (CYM1611 and CYM1624) to maximize system flexibility.

Writing to the module is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (I/O_0 through I/O_{15}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable $\overline{OE}$) low, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{15}) will appear on the appropriate data input/output pins (I/O_0 through I/O_{15}).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

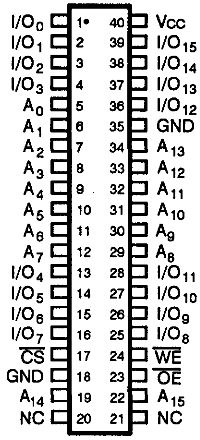
Logic Block Diagram



1622-1

Pin Configuration

Plastic VDIP
Top View



1622-2

8

Selection Guide

	1622HV-25	1622HV-35	1622HV-45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	400	400	400
Maximum Standby Current (mA)	140	140	140

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −10°C to +80°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1624PV		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]		−0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	−20	+20	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		400	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		140	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		80	mA

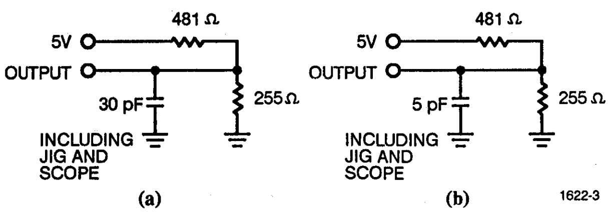
Capacitance[3]

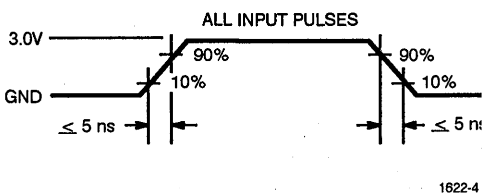
Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

1. $V_{IL(MIN)}$ = −3.0V for pulse widths less than 20 ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range [3]

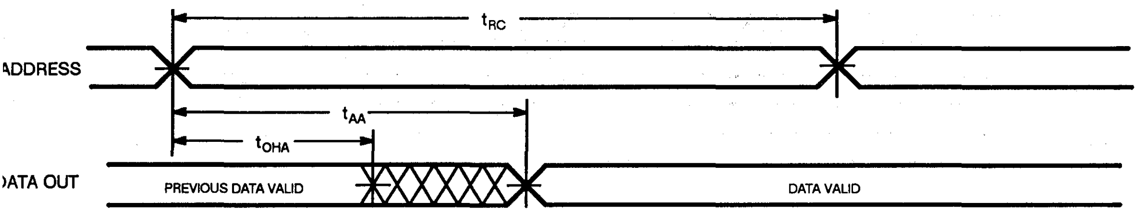
Parameters	Description	1622HV-25 Min.	1622HV-25 Max.	1622HV-35 Min.	1622HV-35 Max.	1622HV-45 Min.	1622HV-45 Max.	Units
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid	25		35		45		ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid	25		35		45		ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]		15		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0	25	0	35	0	45	ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		40		ns
t_{AW}	Address Set-Up to Write End	20		30		40		ns
t_{HA}	Address Hold from Write End	3		3		3		ns
t_{SA}	Address Set-Up from Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [4]	0	15	0	15	0	20	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS}$ = V_{IL}.
8. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms

Read Cycle No. 1 [6, 7]

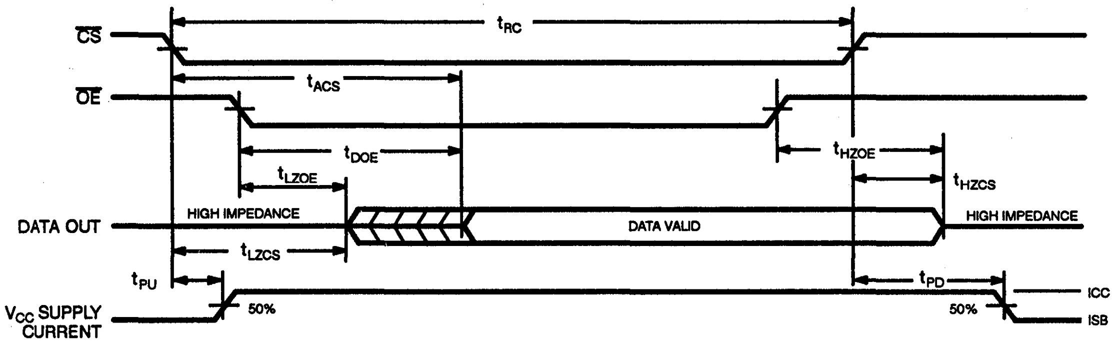


1622-5

8

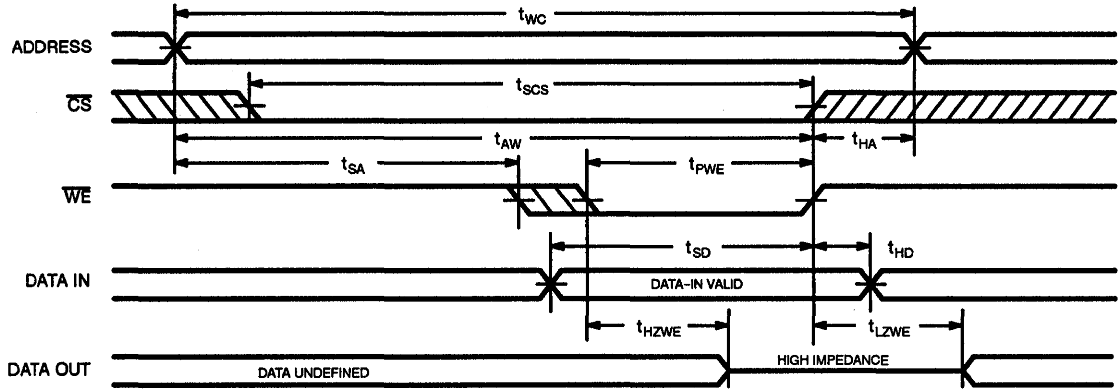
Switching Waveforms (continued)

Read Cycle No. 2 [6, 8]



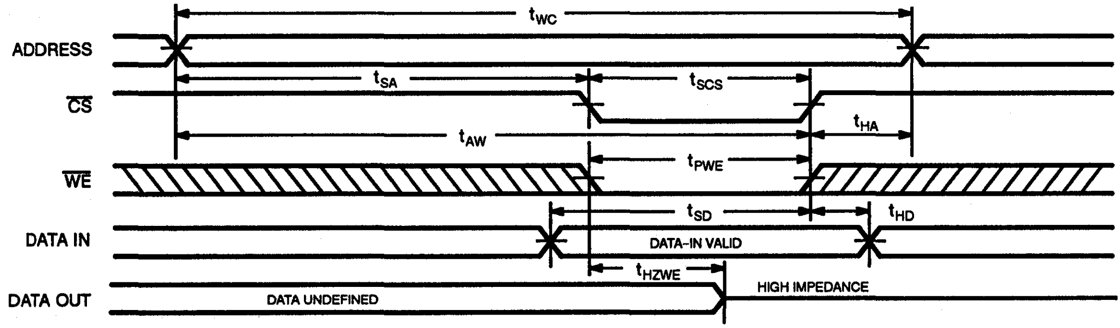
1622-6

Write Cycle No. 1 (WE Controlled) [5]



1622-7

Write Cycle No. 2 (CS Controlled) [5, 9]



1622-8

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1622HV-25C	HV03	Commercial
35	CYM1622HV-35C	HV03	Commercial
45	CYM1622HV-45C	HV03	Commercial

Document #: 38–00010

8

CYPRESS SEMICONDUCTOR

CYM1623

64K x 16 Static RAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 70 ns**
- **40-pin, 0.6-in.-wide DIP package**
- **JEDEC-compatible pin-out**
- **Low active power**
  - **— 1.3W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **2V data retention (L version)**

Functional Description

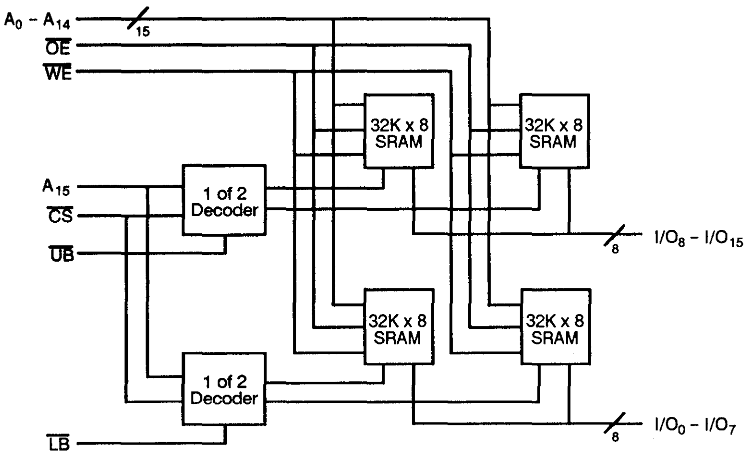
The CYM1623 is a high-performance 1-megabit static RAM module organized as 64K words by 16 bits. The module is constructed using four 32K x 8 static RAMs in leadless chip carriers mounted onto a double-sided multilayer ceramic substrate. A decoder is used to interpret the higher-order address A_{15} and to select one of the two pairs of RAMs.

Writing to the memory module is accomplished when the chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins of the selected byte ($I/O_8 - I/O_{15}$, $I/O_0 - I/O_7$) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) and output enable ($\overline{OE}$) LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the appropriate data input/output pins.

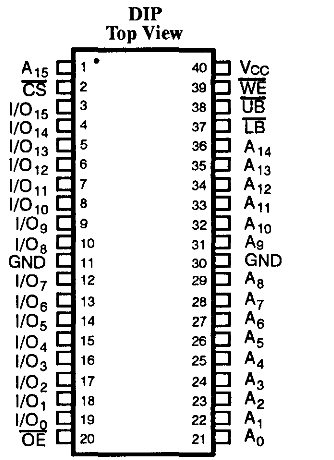
The input/output pins remain in a high-impedance state when chip select ($\overline{CS}$), byte select ($\overline{UB}$, $\overline{LB}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



1623-9

Pin Configuration



1623-10

Selection Guide

		1623HD-70	1623HD-85	1623HD-100
Maximum Access Time (ns)		70	85	100
Maximum Operating Current (mA)	Commercial	240	240	240
Maximum Standby Current (mA)	Commercial	70	70	70

CYPRESS SEMICONDUCTOR

CYM1624

64K x 16 SRAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **2.75W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Pin layout compatible with CYM1611 and CYM1622**
- **Low profile**
  - **Max. height of .54 in.**
- **Small PCB footprint**
  - **0.7 sq. in.**

Functional Description

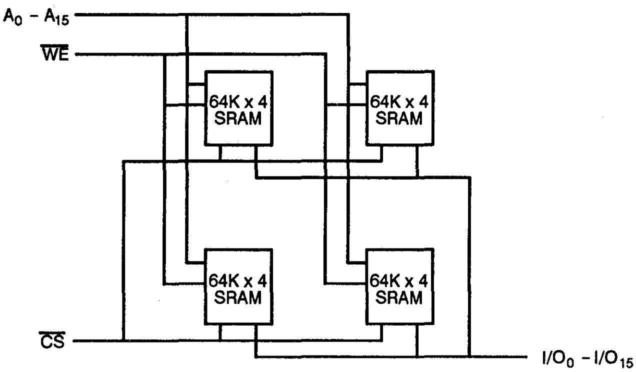
The CYM1624 is a very high performance 1-megabit static RAM module organized as 64K words by 16 bits. This module is constructed using four 64K x 4 static RAMs in SOJ packages mounted on an epoxy laminate board with pins. The pinout of this module is compatible with two other Cypress modules (CYM1611 and CYM1622) to maximize system flexibility.

Writing to the module is accomplished when the chip select ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the sixteen input/output pins (I/O_0 through I/O_{15}) of the device is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{15}) will appear on the appropriate data input/output pins (I/O_0 through I/O_{15}).

The data input/output pins remain in a high-impedance state when chip select ($\overline{CS}$) is HIGH or when write enable ($\overline{WE}$) is LOW.

Logic Block Diagram



1624-1

Pin Configuration

Plastic VDIP

Signal	Pin	Pin	Signal
I/O_0	1	40	V_{CC}
I/O_1	2	39	I/O_{15}
I/O_2	3	38	I/O_{14}
I/O_3	4	37	I/O_{13}
A_0	5	36	I/O_{12}
A_1	6	35	GND
A_2	7	34	A_{13}
A_3	8	33	A_{12}
A_4	9	32	A_{11}
A_5	10	31	A_{10}
A_6	11	30	A_9
A_7	12	29	A_8
I/O_4	13	28	I/O_{11}
I/O_5	14	27	I/O_{10}
I/O_6	15	26	I/O_9
I/O_7	16	25	I/O_8
$\overline{CS}$	17	24	$\overline{WE}$
GND	18	23	NC
A_{14}	19	22	A_{15}
NC	20	21	NC

1624-2

8

Selection Guide

	1624PV-25	1624PV-35	1624PV-45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	500	500	500
Maximum Standby Current (mA)	160	160	160

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −45°C to +125°C

Ambient Temperature with Power Applied .... −10°C to +85°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1624PV Min.	CYM1624PV Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]		−0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	−20	+20	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	−20	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS} \leq V_{IL}$		500	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{IH}$, Min. Duty Cycle = 100%		160	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current	V_{CC} = Max., $\overline{CS} \geq V_{CC}$ − 0.2V, $V_{IN} \geq V_{CC}$ − 0.2V or $V_{IN} \leq$ 0.2V		80	mA

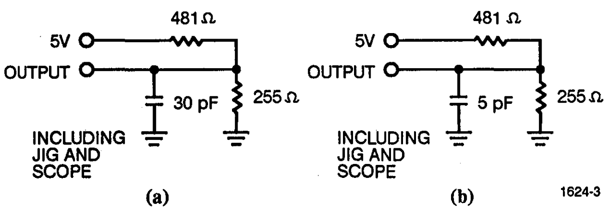
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		15	pF

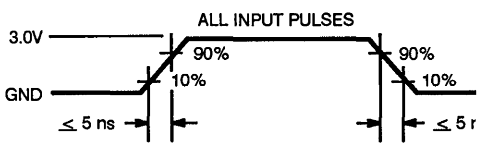
Notes:

1. $V_{IL(MIN)}$ = −3.0V for pulse widths less than 20ns.
2. Tested on a sample basis.

AC Test Loads and Waveforms



1624-3



1624-

Switching Characteristics Over the Operating Range [3]

Parameters	Description	1624PV-25		1624PV-35		1624PV-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[4]		15		25		30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		35		ns
t_{AW}	Address Set-Up to Write End	20		30		35		ns
t_{HA}	Address Hold from Write End	3		5		5		ns
t_{SA}	Address Set-Up from Write Start	2		3		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		35		ns
t_{SD}	Data Set-Up to Write End	15		20		20		ns
t_{HD}	Data Hold from Write End	3		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		2		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[4]	0	15	0	15	0	15	ns

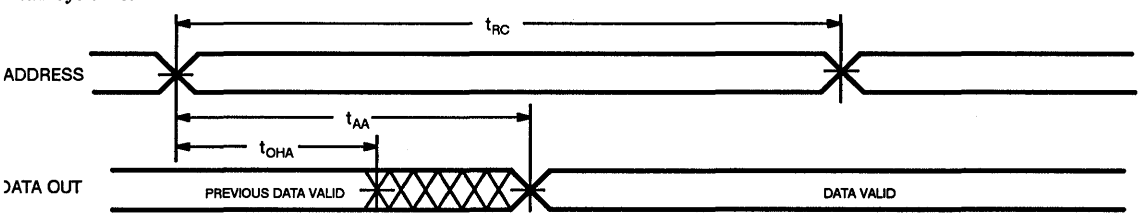
Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
5. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
6. $\overline{WE}$ is HIGH for read cycle.
7. Device is continuously selected, $\overline{CS} = V_{IL}$.
8. Address valid prior to or coincident with $\overline{CS}$ transition low.
9. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

8

Switching Waveforms

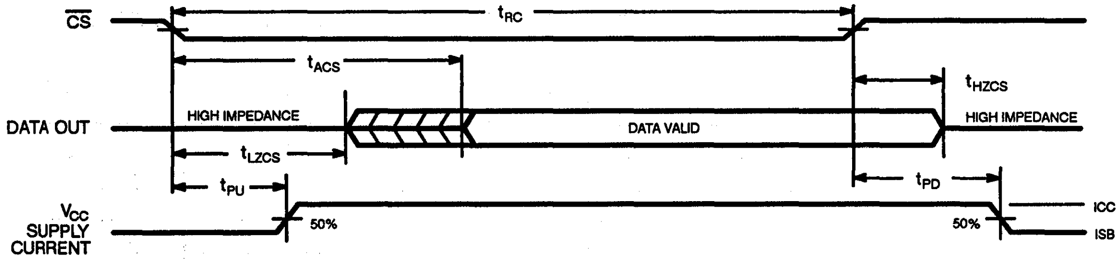
Read Cycle No. 1[6, 7]



1624-5

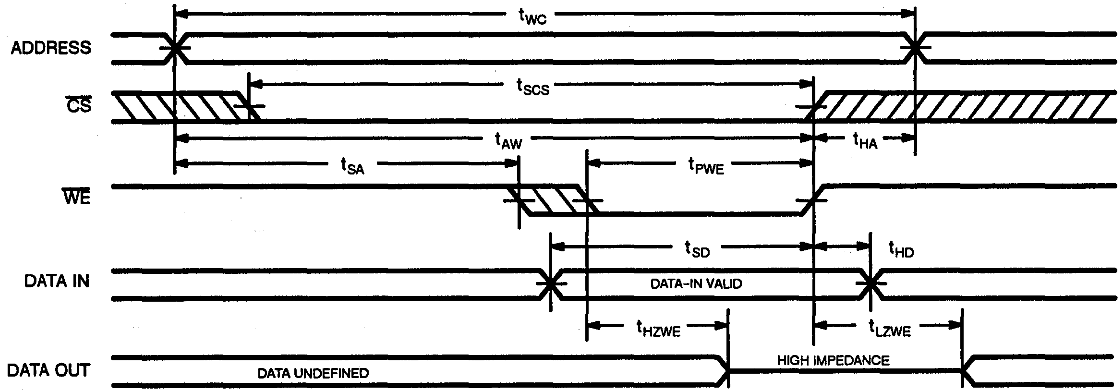
Switching Waveforms (continued)

Read Cycle No. 2[6, 8]



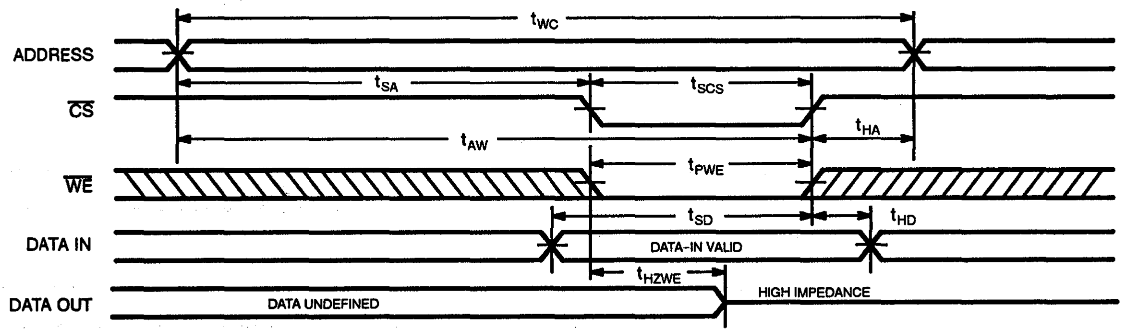
1624-6

Write Cycle No. 1 ($\overline{WE}$ Controlled)[5]



1624-7

Write Cycle No. 2 ($\overline{CS}$ Controlled)[5, 9]



1624-8

Truth Table

$\overline{CS}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1624PV-25C	PV01	Commercial
35	CYM1624PV-35C	PV01	Commercial
45	CYM1624PV-45C	PV01	Commercial

Document #: 38-M-00028

8

CYM1641

CYPRESS SEMICONDUCTOR

256K x 16 Static RAM Module

Features

- **High-density 4-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Customer configurable**
  - **x4, x8, x16**
- **Low active power**
  - **10W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .300 in.**
- **Small PCB footprint**
  - **2.2 sq. in.**

Functional Description

The CYM1641 is a high-performance 4-megabit static RAM module organized as 256K words by 16 bits. This module is constructed from sixteen 256K x 1 SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. Four separate $\overline{CS}$ pins are used to control each 4-bit nibble of the 16-bit word. This feature permits the user to configure this module as either 1M x 4, 512K x 8 or 256K x 16 organization through external decoding and appropriate pairing of the outputs.

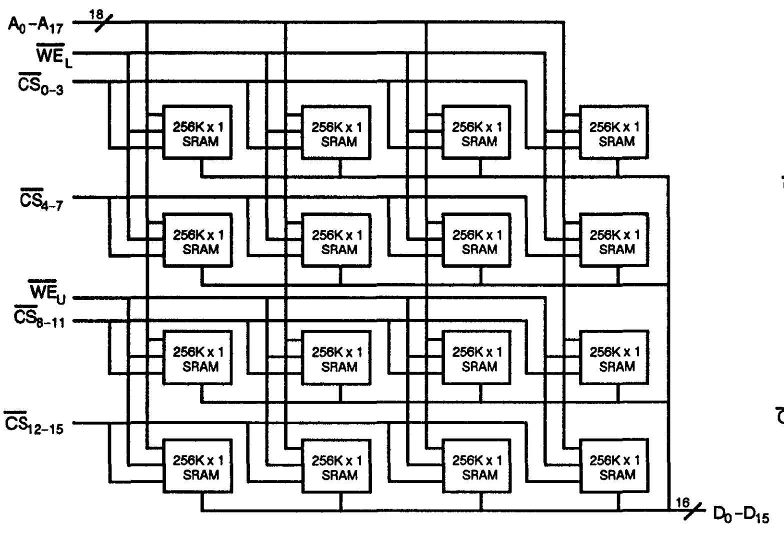
Writing to the device is accomplished when the chip select ($\overline{CS}_{XX}$) and write enable ($\overline{WE}_{U,L}$) inputs are both LOW. Data on the data lines (D_X) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip select ($\overline{CS}_{XX}$) LOW, while write enable ($\overline{WE}_{U,L}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data lines (D_X).

The data output is in the high-impedance state when chip enable ($\overline{CS}_{XX}$) is HIGH or write enable ($\overline{WE}_{U,L}$) is LOW.

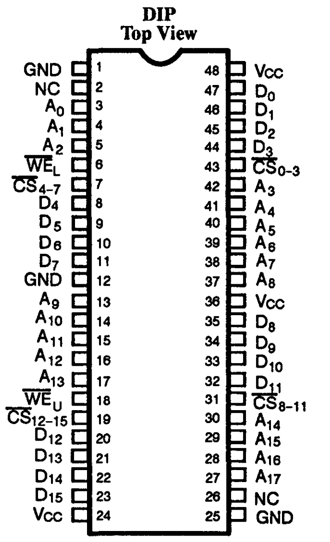
Power is consumed in each 4-bit nibble only when the appropriate $\overline{CS}$ is enabled, thus reducing power in the x4 or x8 mode.

Logic Block Diagram



1641-1

Pin Configuration



1641-2

Selection Guide

		1641HD-25	1641HD-35	1641HD-45	1641HD-55
Maximum Access Time (ns)		25	35	45	55
Maximum Operating Current (mA)	Commercial	1800	1800	1800	1800
	Military		1800	1800	1800
Maximum Standby Current (mA)	Commercial	560	560	560	560
	Military		560	560	560

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... -65°C to +150°C

Ambient Temperature with
Power Applied .... -55°C to +125°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs
in High Z State .... -0.5V to +7.0V

DC Input Voltage .... -0.5V to 7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military [4]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions		CYM1641HD		Units
				Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8.0 mA Military I_{OL} = 12.0 mA Commercial		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			-0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$		-80	+80	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		-10	+10	μA
I_{CCx16}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_{xx} \leq V_{IL}$			1800	mA
I_{CCx8}	V_{CC} Operating Supply Current by 8 Mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_{xx} \leq V_{IL}$			950	mA
I_{CCx4}	V_{CC} Operating Supply Current by 4 Mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_{xx} \leq V_{IL}$			720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [1]	Max. V_{CC}, $\overline{CS}_{xx} \geq V_{IH}$ Min. Duty Cycle = 100%			560	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [1]	Max. V_{CC}, $\overline{CS}_{xx} \geq V_{CC}$- 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V			320	mA

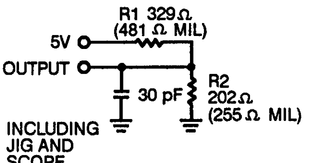
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance ($A_0 - A_{17}$, $\overline{CS}$, $\overline{WE}$)	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	150	pF
C_{INB}	Input Capacitance ($D_0 - D_{15}$)		30	pF
C_{OUT}	Output Capacitance		30	pF

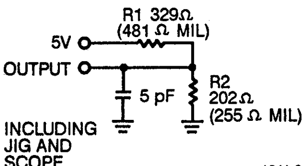
Notes:

1. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested initially and after any design or process changes that may affect these parameters.
3. T_A is the "instant on" case temperature.

AC Test Loads and Waveforms

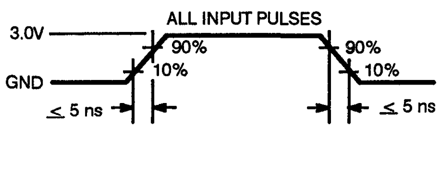


(a)



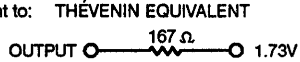
(b)

1641-3



1641-4

Equivalent to: THÉVENIN EQUIVALENT



Military

Commercial

Switching Characteristics Over the Operating Range [5]

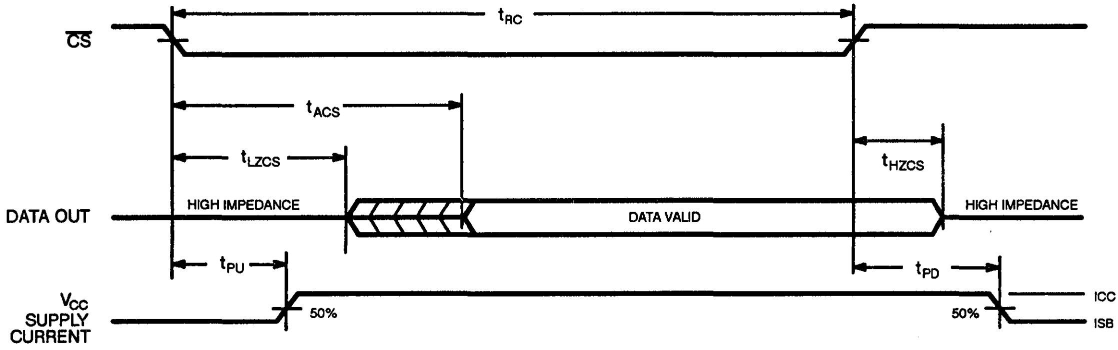
Parameters	Description	1641HD-25		1641HD-35		1641HD-45		1641HD-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6, 7]		15		20		25		25	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45		55	ns
WRITE CYCLE [8]										
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		40		40		ns
t_{AW}	Address Set-Up to Write End	20		30		40		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		30		ns
t_{SD}	Data Set-Up to Write End	15		17		20		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]	0	20	0	25	0	25	0	25	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS} = V_{IL}$.
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

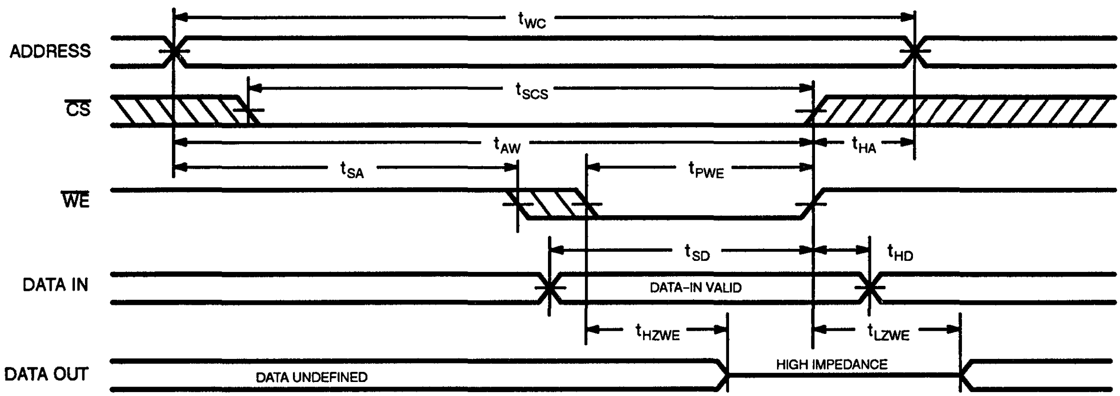
Switching Waveforms

Read Cycle[9, 10]



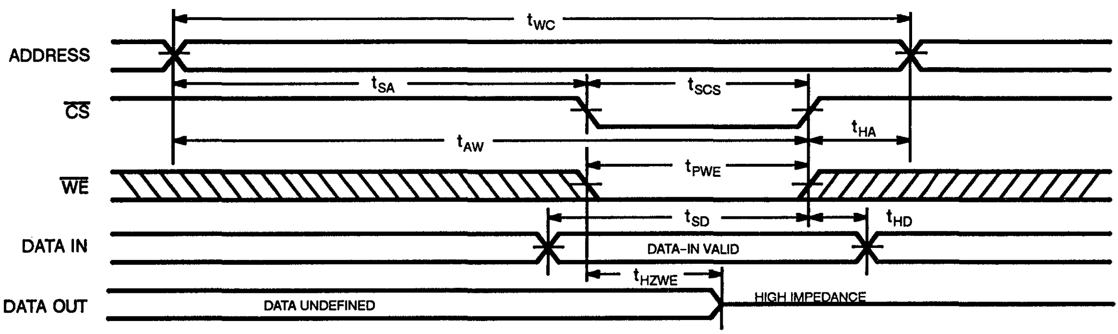
1641-5

Write Cycle No. 1 (WE Controlled)[8]



1641-6

Write Cycle No. 2 (CS Controlled)[8, 11]



1641-7

Truth Table

$\overline{CS}_{xx}$	$\overline{WE}_n$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1641HD-25C	HD05	Commercial
35	CYM1641HD-35C	HD05	Commercial
	CYM1641HD-35MB	HD05	Military
45	CYM1641HD-45C	HD05	Commercial
	CYM1641HD-45MB	HD05	Military
55	CYM1641HD-55C	HD05	Commercial
	CYM1641HD-55MB	HD05	Military

Document #: 38-M-00013-A

CYPRESS SEMICONDUCTOR

32K x 24 SRAM Module

Features

- High-density 768-kbit SRAM module
- High-speed CMOS SRAMs
  - Access time of 25 ns
- 56-pin, 0.5-inch-high ZIP package
- Low active power
  - 1.8W (max.)
- SMD technology
- TTL-compatible inputs and outputs
- Commercial temperature range
- Small PCB footprint
  - 0.66 sq. in.

Functional Description

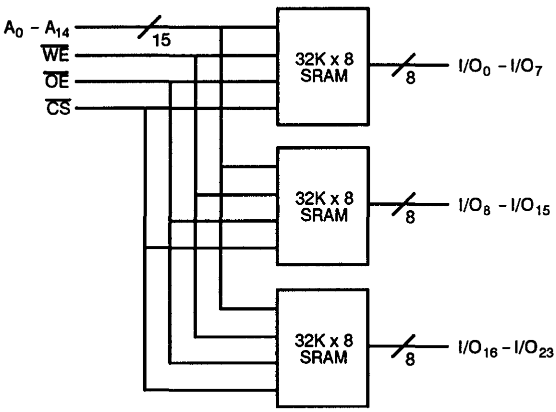
The CYM1720 is a high-performance 768-kbit static RAM module organized as 32K words by 24 bits. This module is constructed using three 32K x 8 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins.

Writing to the module is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_0 through I/O_{23}) of the device is written into the memory location specified on the address pins (A_0 through A_{14}).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains inactive or HIGH. Under these conditions, the contents of the memory location specified on the address pins (A_0 through A_{14}) will appear on the input/output pins (I/O_0 through I/O_{23}).

The input/output pins remain in a high-impedance state unless the module is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH.

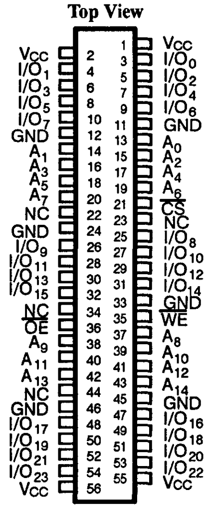
Logic Block Diagram



1720-1

Pin Configuration

ZIP
Top View



1720-2

8

Selection Guide

	1720PZ-25	1720PZ-30	1720PZ-35
Maximum Access Time (ns)	25	30	35
Maximum Operating Current (mA)	330	330	330
Maximum Standby Current (mA)	60	60	60

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −55°C to +125°C

Ambient Temperature with Power Applied .... 0°C to +70°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1720PZ		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		330	mA
I_{SB1}	Automatic $\overline{CS}$[1] Power Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		60	mA
I_{SB2}	Automatic $\overline{CS}$[1] Power Down Current	V_{CC} = Max., $\overline{CS}$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V		60	mA

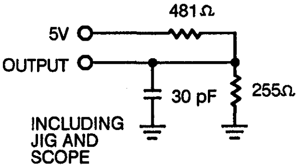
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	35	pF
C_{OUT}	Output Capacitance		25	pF

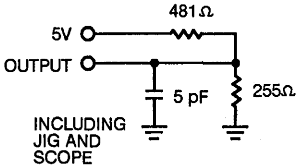
Notes:

1. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms

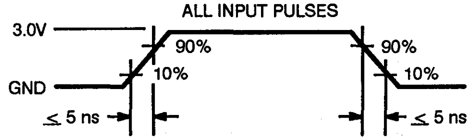


(a)



(b)

1720-3



1720-4

Switching Characteristics Over the Operating Range [3]

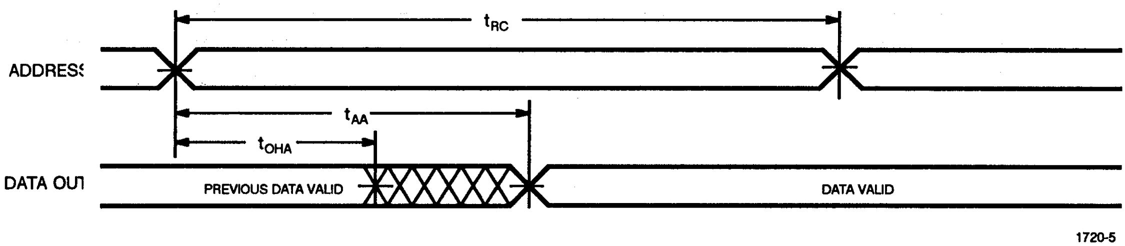
Parameters	Description	1720PZ-25		1720PZ-30		1720PZ-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		30		35		ns
t_{AA}	Address to Data Valid		25		30		35	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		12		15		20	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		10		15		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [5]	5		5		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [4, 5]		10		15		15	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		25		30	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		30		35		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		ns
t_{AW}	Address Set-Up to Write End	22		25		30		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up from Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		23		25		ns
t_{SD}	Data Set-Up to Write End	13		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [4]	0	10	0	10	0	15	ns

Notes:

3. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
4. t_{HZOE}, t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
6. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
7. $\overline{WE}$ is HIGH for read cycle.
8. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
9. Address valid prior to or coincident with $\overline{CS}$ transition low.
10. Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

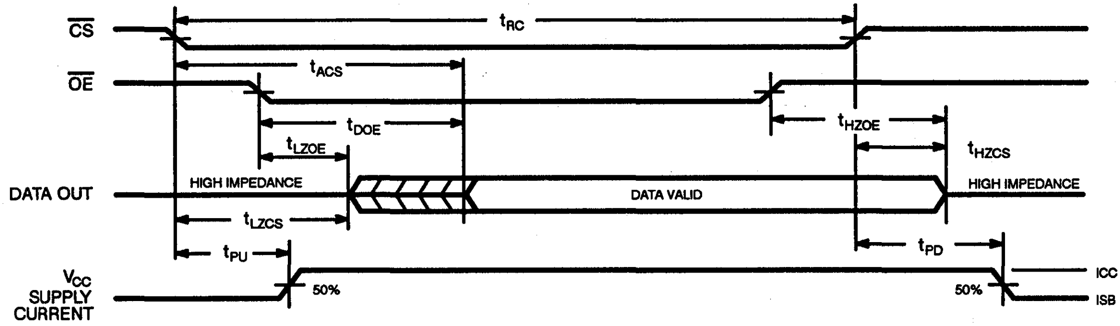
Switching Waveforms

Read Cycle No. 1 [7, 8]



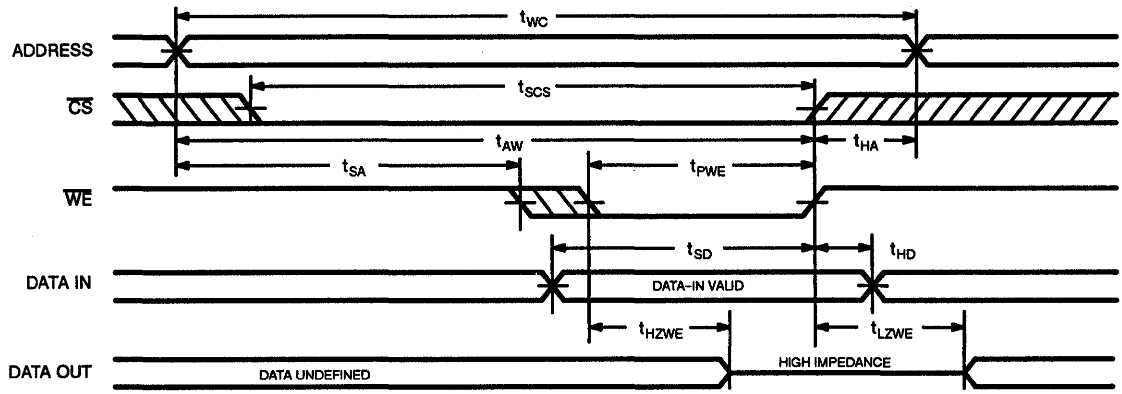
Switching Waveforms (continued)

Read Cycle No. 2[7, 9]



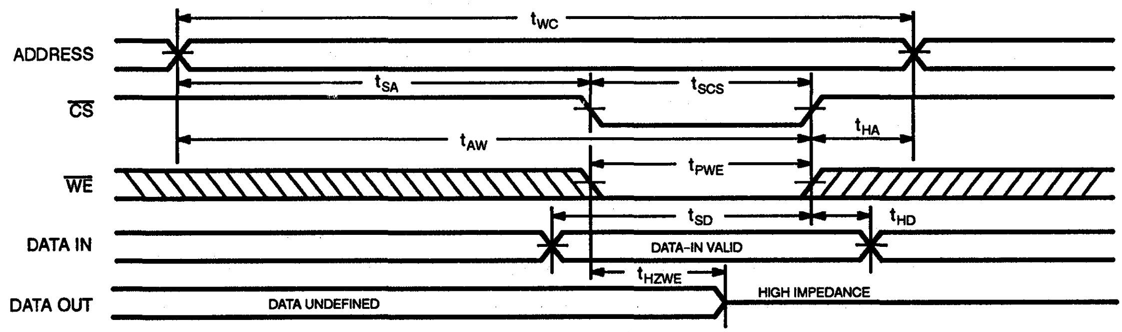
1720-6

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)[6, 10]



1720-7

Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled)[6, 10, 11]



1720-8

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1720PZ-25C	PZ05	Commercial
30	CYM1720PZ-30C	PZ05	Commercial
35	CYM1720PZ-35C	PZ05	Commercial

Document #: 38-M-00021

CYPRESS SEMICONDUCTOR

CYM1821

16K x 32 Static RAM Module

Features

- **High-density 512-kbit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 12 ns**
- **Low active power - 4W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **Max. height of .50 in.**
- **Small PCB footprint**
  - **1.0 sq. in.**
- **JEDEC-compatible pinout**
- **2V data retention (L version)**

Functional Description

The CYM1821 is a high-performance 512-kbit static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 SRAM SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$ and $\overline{CS}_4$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

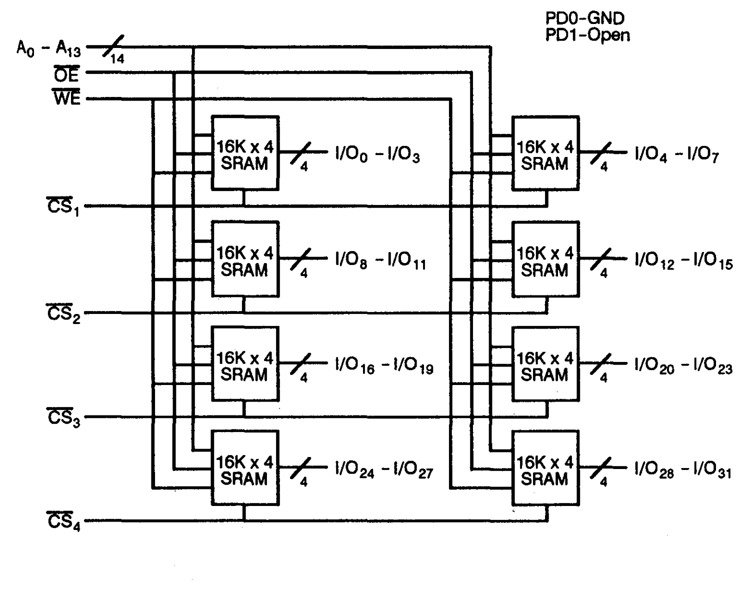
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS}_N$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_N$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

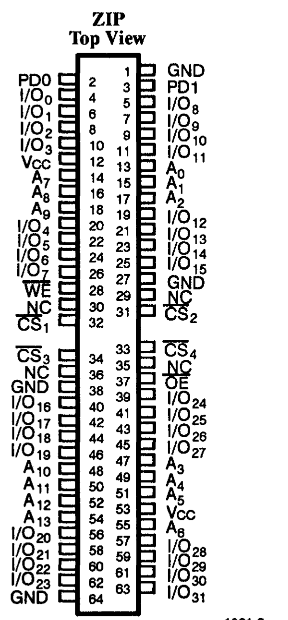
Two pins (PD0 and PD1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

Logic Block Diagram



1821-1

Pin Configuration



1821-2

Selection Guide

	1821PZ-12	1821PZ-15	1821PZ-20	1821PZ-25	1821PZ-35	1821PZ-45
Maximum Access Time (ns)	12	15	20	25	35	45
Maximum Operating Current (mA)	960	960	720	720	720	720
Maximum Standby Current (mA)	450	450	160	160	160	160

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... 0°C to +70°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Static Discharge Voltage .... >2001V (Per MIL-STD-883 Method 3015.2)

Latch-Up Current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	1821PZ-12 1821PZ-15		1821PZ-20 1821PZ-25 1821PZ-35 1821PZ-45		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}	−20	+20	−20	+20	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−20	+20	−20	+20	μA
I_{OS}	Output Short Circuit Current [1]	V_{CC} = Max., V_{OUT} = GND		−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_N$ ≤ V_{IL}		960		720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}; $\overline{CS}_N$ ≥ V_{IH} Min. Duty Cycle = 100%		450		160	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}; $\overline{CS}_N$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V				160	mA

Shaded area contains preliminary information.

Capacitance[3]

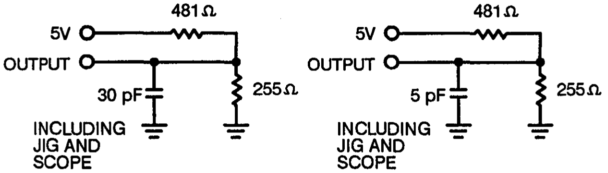
Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance (ADDR, OE, WE)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	70	pF
C_{INB}	Input Capacitance (CS_N)		35	pF
C_{OUT}	Output Capacitance		20	pF

Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

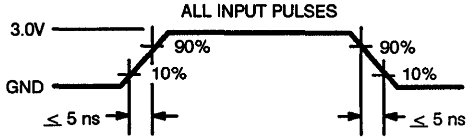
8

AC Test Loads and Waveforms



(a) (b)

1821-3



1821-4

Equivalent to: THÉVENIN EQUIVALENT

Switching Characteristics Over the Operating Range[4]

Parameters	Description	1821PZ-12		1821PZ-15		1821PZ-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		2		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		10	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		8		8		8	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE [7]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Set-Up to Write End	10		12		15		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		10		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	7	0	7	0	7	ns

Shaded area contains preliminary information.

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. $\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$ and $\overline{CS}_4$ are represented by $\overline{CS}$ in the Switching Characteristics and Waveforms.

Switching Characteristics Over the Operating Range (continued) [4]

Parameters	Description	1821PZ-25		1821PZ-35		1821PZ-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	5		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		10		15		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45	ns
WRITE CYCLE [7]								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		35		ns
t_{AW}	Address Set-Up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	13		15		20		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	3		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	7	0	10	0	15	ns

8

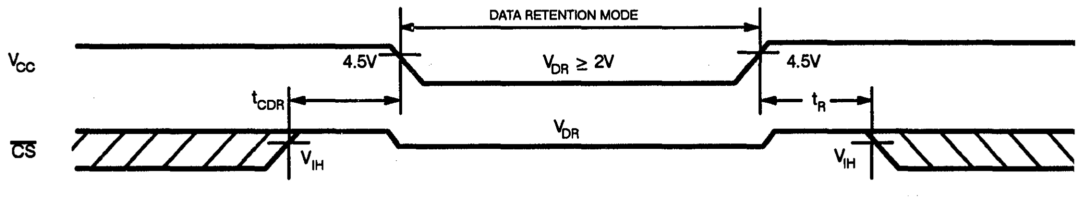
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1821		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			8	mA
t_{CDR} [13]	Chip Deselect to Data Retention Time		0		ns
t_R [13]	Operation Recovery Time		t_{RC} [12]		ns
I_{LI} [13]	Input Leakage Current			10	μA

Notes:

12. t_{RC} = Read Cycle Time.
13. Guaranteed, not tested.
14. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

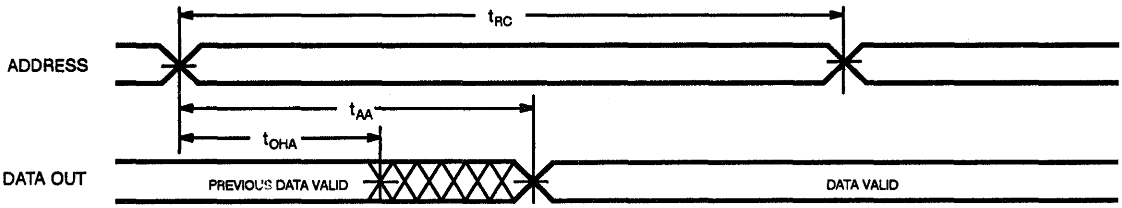
Data Retention Waveform



1821-5

Switching Waveforms [11]

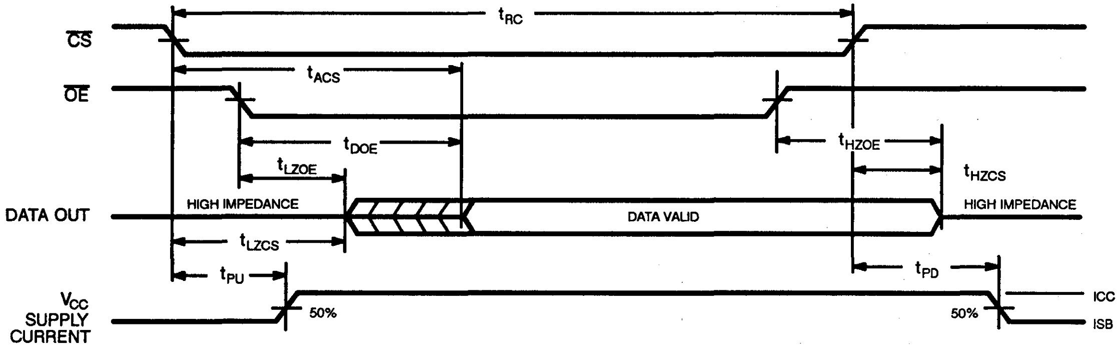
Read Cycle No. 1[8, 9]



1821-6

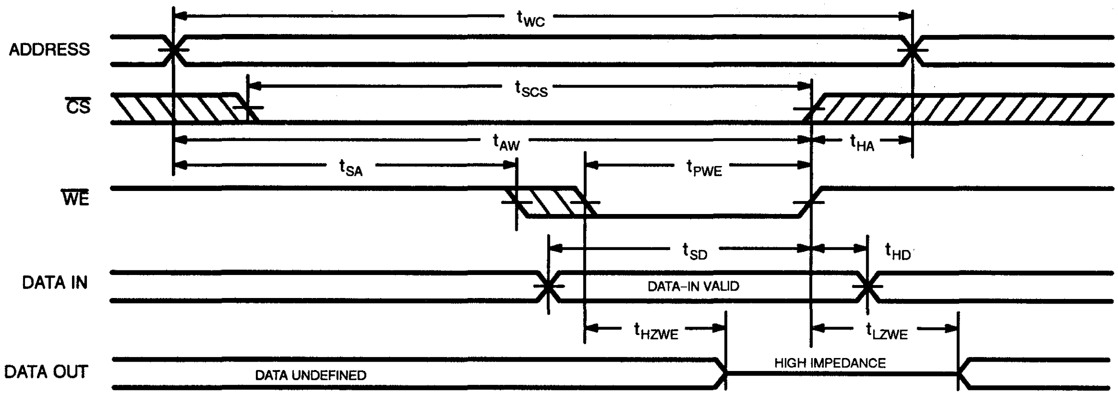
Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



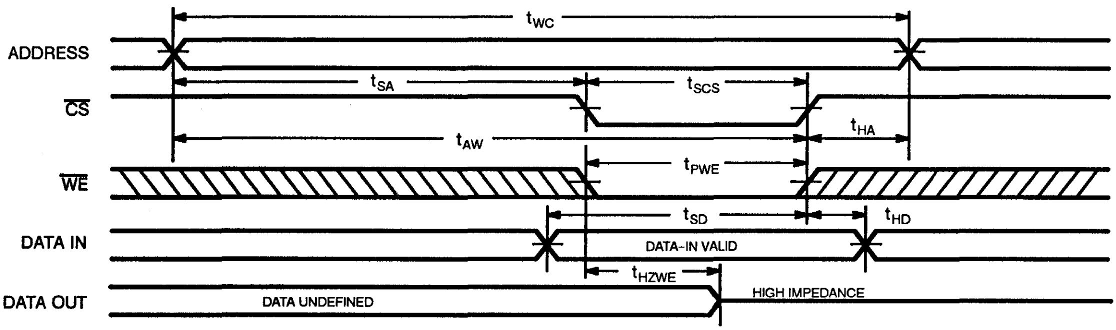
1821-7

Write Cycle No. 1 (WE Controlled)[7]



1821-8

Write Cycle No. 2 (CS Controlled)[7, 14]



1821-9

Truth Table

$\overline{CS_N}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
12	CYM1821PZ-12C	PZ01	Commercial
15	CYM1821PZ-15C	PZ01	Commercial
20	CYM1821PZ-20C	PZ01	Commercial
	CYM1821LPZ-20C	PZ01	
25	CYM1821PZ-25C	PZ01	Commercial
	CYM1821LPZ-25C	PZ01	
35	CYM1821PZ-35C	PZ01	Commercial
	CYM1821LPZ-35C	PZ01	
45	CYM1821PZ-45C	PZ01	Commercial
	CYM1821LPZ-45C	PZ01	

Shaded area contains preliminary information.

Document #: 38-M-00015-A

16K x 32 Static RAM Module with Separate I/O

Features

- **High-density 512K-bit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 12 ns**
- **Low active power**
  - **— 5.3W (max.)**
- **Hermetic SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .52 in.**
- **Small PCB footprint**
  - **— 1.0 sq. in.**
- **2V data retention (L version)**

Functional Description

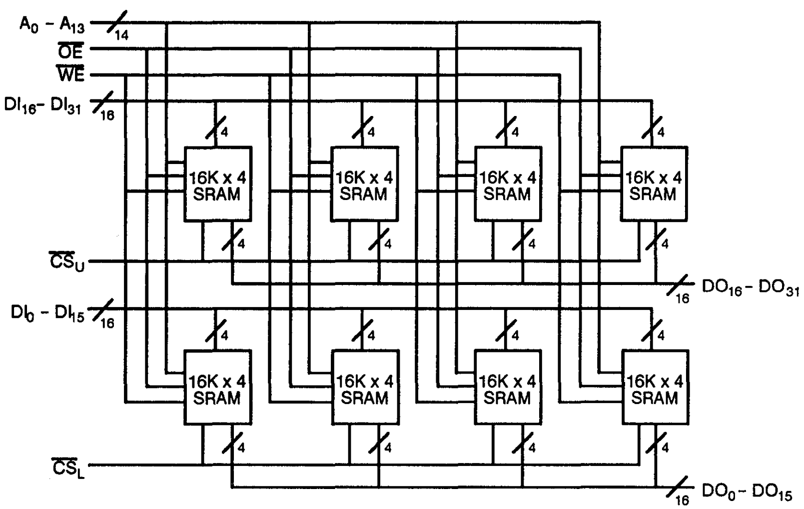
The CYM1822 is a high-performance 512-kbit static RAM module organized as 16K words by 32 bits. This module is constructed from eight 16K x 4 separate I/O SRAMs in leadless chip carriers mounted on a ceramic substrate with pins. Two chip selects ($\overline{CS}_U$ and $\overline{CS}_L$) are used to independently enable the upper and lower 16-bit data words.

Writing to the device is accomplished when the chip selects ($\overline{CS}_U$ and/or $\overline{CS}_L$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input pins (DI_X) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip selects ($\overline{CS}_U$ and/or $\overline{CS}_L$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data output pins (DO_X).

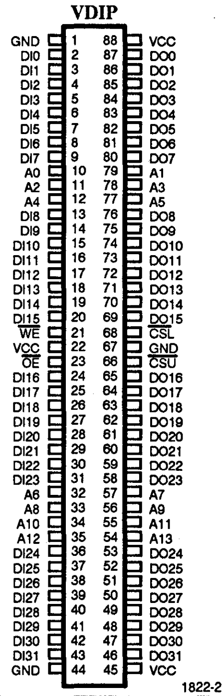
The output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, the appropriate chip selects are HIGH, or $\overline{OE}$ is HIGH.

Logic Block Diagram



1822-1

Pin Configuration



1822-2

Selection Guide

		1822HV-12	1822HV-15	1822HV-20	1822HV-25	1822HV-30	1822HV-35	1822HV-45
Maximum Access Time (ns)		12	15	20	25	30	35	45
Maximum Operating Current (mA)	Commercial	960	960	720	720	720	720	720
	Military		960	960	720	720	720	720
Maximum Standby Current (mA)	Commercial	450	450	160	160	160	160	160
	Military		450	450	160	160	160	160

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	1822HV-12 1822HV-15 1822HV-20M		1822HV-20C 1822HV-25 1822HV-35 1822HV-45 1822HV-50		Units
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–20	+20	–20	+20	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	–20	+20	–20	+20	μA
I_{OS}	Output Short Circuit Current [1]	V_{CC} = Max., V_{OUT} = GND		–350		–350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_L$, $\overline{CS}_U \leq V_{IL}$		960		720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}; $\overline{CS}_U$, $\overline{CS}_L \geq V_{IH}$ Min. Duty Cycle = 100%		450		160	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}; $\overline{CS}_U$, $\overline{CS}_L \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V		—		160	mA

Shaded area contains preliminary information.

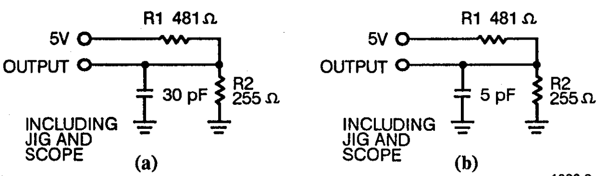
Capacitance [3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	80	pF
C_{OUT}	Output Capacitance		15	pF
C_{INDATA}	Input Capacitance		15	pF

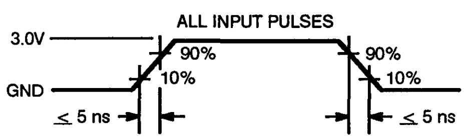
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the CE input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

Ac Test Loads and Waveforms

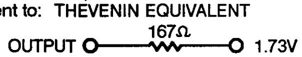


1822-3



1822-3

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

Parameters	Description	1822HV-12		1822HV-15		1822HV-20		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	2		2		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		10		15	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	2		2		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		8		8		8	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	3		3		5		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		8		8		8	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		12		15		20	ns
WRITE CYCLE [7]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Set-Up to Write End	10		12		15		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		13		ns
t_{HD}	Data Hold from Write End	2		2		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	7	0	7	0	7	ns

Shaded area contains preliminary information.

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

8

Switching Characteristics Over the Operating Range (continued) [4]

Parameters	Description	1822HV-25		1822HV-30		1822HV-35		1822HV-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_{AA}	Address to Data Valid		25		30		35		45	ns
t_{OHA}	Data Hold from Address Change	5		5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		20		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	5		10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5, 6]		10		15		15		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35		45	ns
WRITE CYCLE [7]										
t_{WC}	Write Cycle Time	25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	13		20		20		25		ns
t_{HD}	Data Hold from Write End	3		3		3		3		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		5		5		5		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5, 6]	0	7	0	12	0	12	0	15	ns

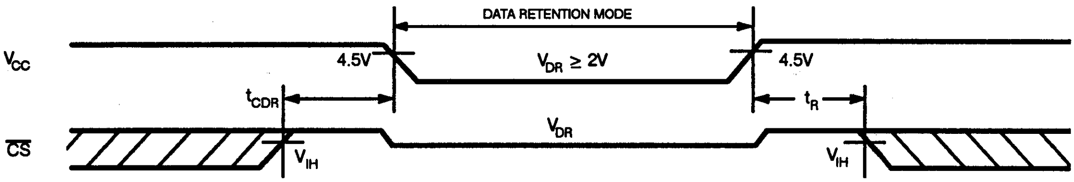
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1822		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			8	mA
t_{CDR} [8]	Chip Deselect to Data Retention Time		0		ns
t_R [8]	Operation Recovery Time		t_{RC} [9]		ns
I_{LI} [8]	Input Leakage Current			10	μA

Notes:

8. Guaranteed, not tested.
9. t_{RC} = Read Cycle Time.
10. Both $\overline{CS}_L$ and $\overline{CS}_U$ are represented by $\overline{CS}$ in the Switching Characteristics and Waveforms.
11. $\overline{WE}$ is HIGH for read cycle.
12. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
13. Address valid prior to or coincident with $\overline{CS}$ transition low.
14. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

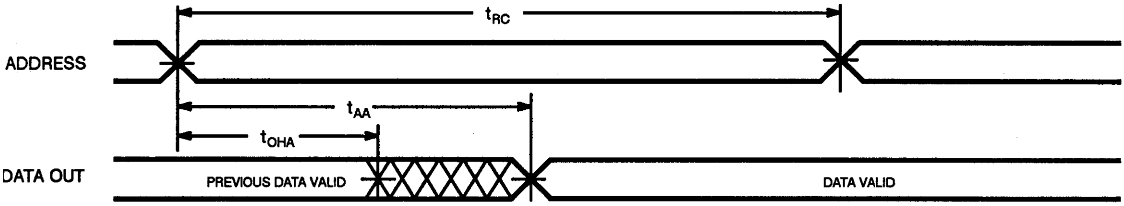
Data Retention Waveform



1822-5

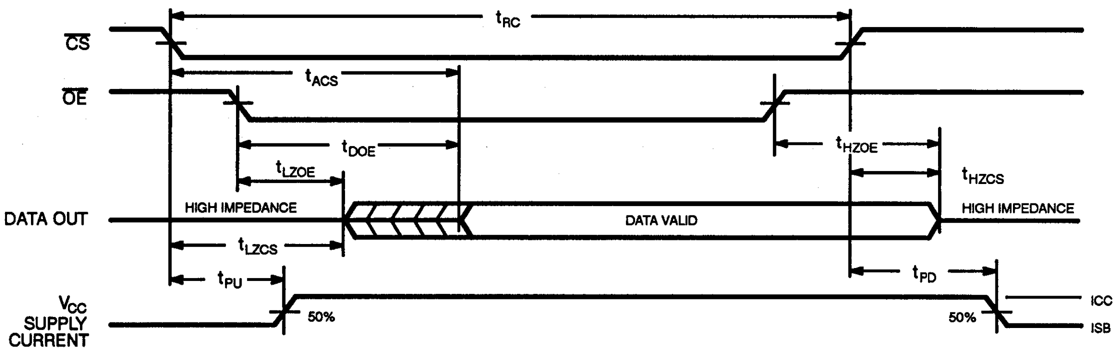
Switching Waveforms [10]

Read Cycle No. 1 [11, 12]



1822-6

Read Cycle No. 2 [11, 13]

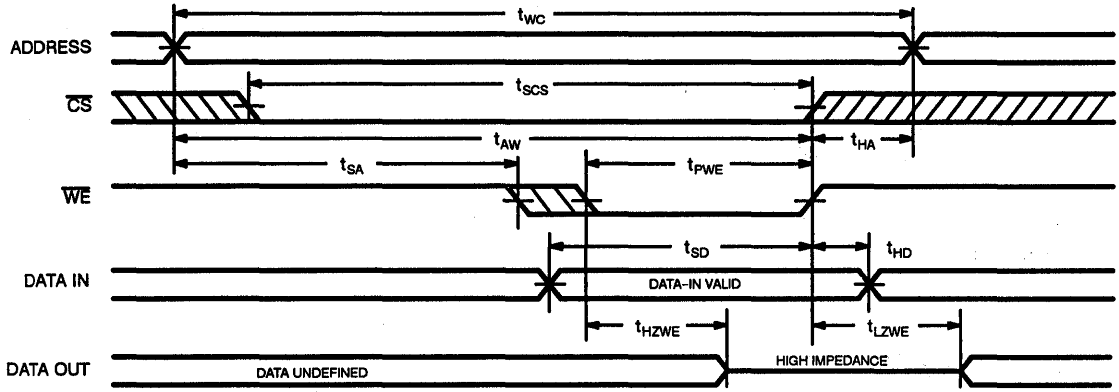


1822-7

8

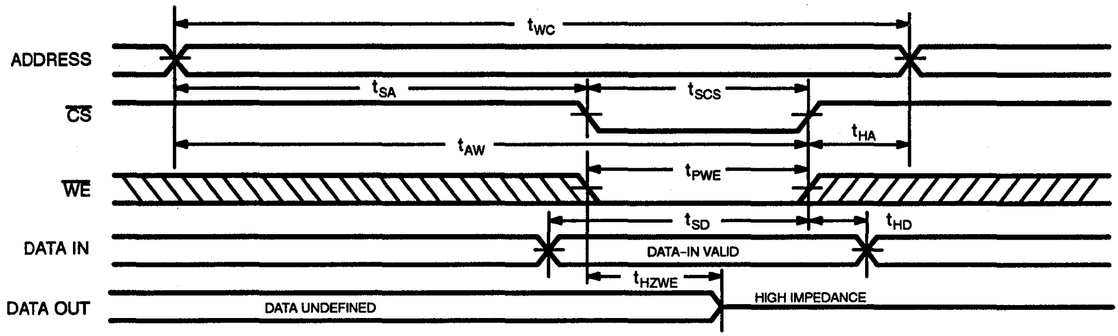
Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled) [7]



1822-9

Write Cycle No. 2 (CS Controlled) [7, 14]



1822-8

Truth Table

$\overline{CS_U}$	$\overline{CS_L}$	$\overline{OE}$	$\overline{WE}$	Input/Outputs	Mode
H	H	X	X	High Z	Deselect/Power-Down
L	L	L	H	Data Out $_{0-31}$	Read
H	L	L	H	Data Out $_{0-15}$	Read Lower Word
L	H	L	H	Data Out $_{16-31}$	Read Upper Word
L	L	X	L	Data In $_{0-31}$	Write
H	L	X	L	Data In $_{0-15}$	Write Lower Word
L	H	X	L	Data In $_{16-31}$	Write Upper Word
L	L	H	H	High Z	Deselect
H	L	H	H	High Z	Deselect
L	H	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
12	CYM1822HV-12C	HV02	Commercial
15	CYM1822HV-15C	HV02	Commercial
	CYM1822HV-15MB	HV02	Military
20	CYM1822HV-20C	HV02	Commercial
	CYM1822LHV-20C	HV02	
	CYM1822HV-20MB	HV02	Military
25	CYM1822HV-25C	HV02	Commercial
	CYM1822LHV-25C	HV02	
	CYM1822HV-25MB	HV02	Military
	CYM1822LHV-25MB	HV02	
30	CYM1822HV-30C	HV02	Commercial
	CYM1822LHV-30C	HV02	
	CYM1822HV-30MB	HV02	Military
	CYM1822LHV-30MB	HV02	
35	CYM1822HV-35C	HV02	Commercial
	CYM1822LHV-35C	HV02	
	CYM1822HV-35MB	HV02	Military
	CYM1822LHV-35MB	HV02	
45	CYM1822HV-45C	HV02	Commercial
	CYM1822LHV-45C	HV02	
	CYM1822HV-45MB	HV02	Military
	CYM1822LHV-45MB	HV02	

Shaded area contains preliminary information.

Document #: 38-M-00016-A

8

CYPRESS SEMICONDUCTOR

CYM1830

64K x 32 Static RAM Module

Features

- High-density 2-megabit SRAM module
- High-speed CMOS SRAMs
  - Access time of 25 ns
- Independent byte and word controls
- Low active power
  - 4.8W (max.)
- Hermetic SMD technology
- TTL-compatible inputs and outputs
- Low profile
  - Max. height of .270 in.
- Small PCB footprint
  - 1.8 sq. in.

Functional Description

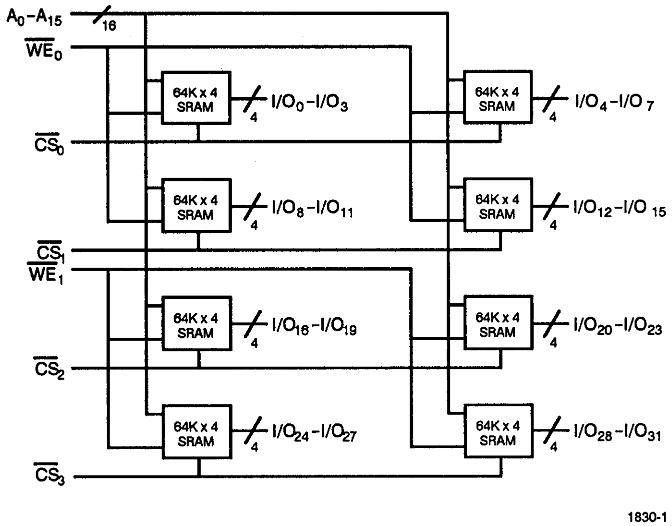
The CYM1830 is a high-performance 2-megabit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in LCC packages mounted on a ceramic substrate with pins. Four chip selects ($\overline{CS_0}$, $\overline{CS_1}$, $\overline{CS_2}$ and $\overline{CS_3}$) are used to independently enable the four bytes. Two write enables ($\overline{WE_0}$ and $\overline{WE_1}$) are used to independently write to either upper or lower 16-bit word of RAM. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects and write enables.

Writing to each byte is accomplished when the appropriate chip select ($\overline{CS_X}$) and write enable ($\overline{WE_X}$) inputs are both LOW. Data on the input/output pins ($\overline{I/O_X}$) is written into the memory location specified on the address pins (A_0 through A_{15}).

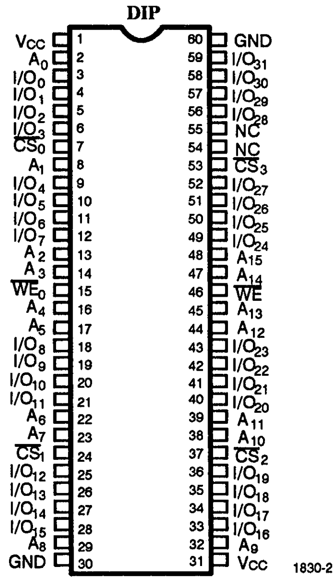
Reading the device is accomplished by taking the chip selects ($\overline{CS_X}$) LOW, while write enables($\overline{WE_X}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins ($\overline{I/O_X}$).

The Data input/output pins stay in the high-impedance state when write enables ($\overline{WE_X}$) are LOW, or the appropriate chip selects are HIGH.

Logic Block Diagram



Pin Configuration



Selection Guide

		1830HD-25	1830HD-30	1830HD-35	1830HD-45	1830HD-55
Maximum Access Time (ns)		25	30	35	45	55
Maximum Operating Current (mA)	Commercial	880	880	880	880	880
	Military			880	880	880
Maximum Standby Current (mA)	Commercial	320	320	320	320	320
	Military			320	320	320

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –55°C to +125°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military [4]	–55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1830HD		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		–0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–20	+20	μA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	–10	+10	μA
I_{OS}	Output Short Circuit Current [1]	V_{CC} = Max., V_{OUT} = GND		–350	mA
I_{CC}	V_{CC} Operating Supply Current by 16 Mode	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_X \leq V_{IL}$		880	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}_X \geq V_{IH}$ Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}, $\overline{CS}_X \geq V_{CC}$ – 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V or $V_{IN} \leq$ 0.3V		160	mA

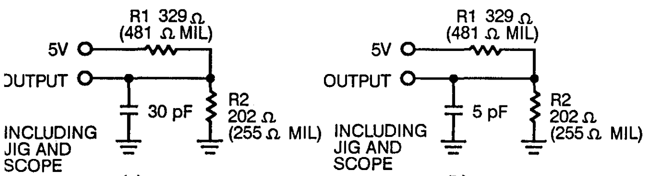
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance, Address Pins	T_A = 25°C, f = 1 MHz V_{CC} = 5.0V	90	pF
C_{INB}	Input Capacitance, I/O Pins		30	pF
C_{OUT}	Output Capacitance		30	pF

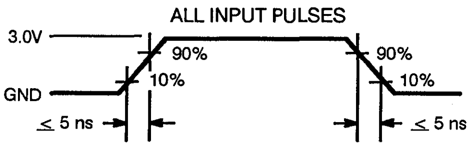
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested initially and after any design or process changes that may affect these parameters.
4. T_A is the "instant on" case temperature.

AC Test Loads and Waveforms

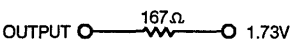


(a) (b)

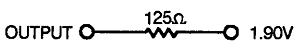


1830-3 1830-4

Equivalent to: THÉVENIN EQUIVALENT



Military



Commercial

8

Switching Characteristics Over the Operating Range [5]

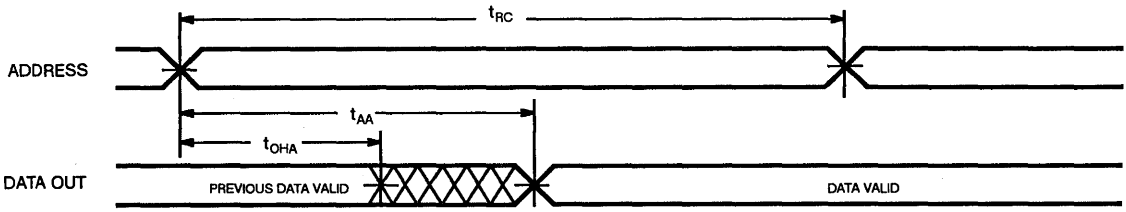
Parameters	Description	1830HD-25		1830HD-30		1830HD-35		1830HD-45		1830HD-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	25		30		35		45		55		ns
t_{AA}	Address to Data Valid		25		30		35		45		55	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[7]	3		3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[6, 7]		15		15		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35		45		55	ns
WRITE CYCLE [8]												
t_{WC}	Write Cycle Time	25		30		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		40		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		40		ns
t_{SD}	Data Set-Up to Write End	15		20		20		25		25		ns
t_{HD}	Data Hold from Write End	2		2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	1		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]	0	15	0	20	0	20	0	20	0	20	ns

Notes:

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS} = V_{IL}$.
11. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms [10]

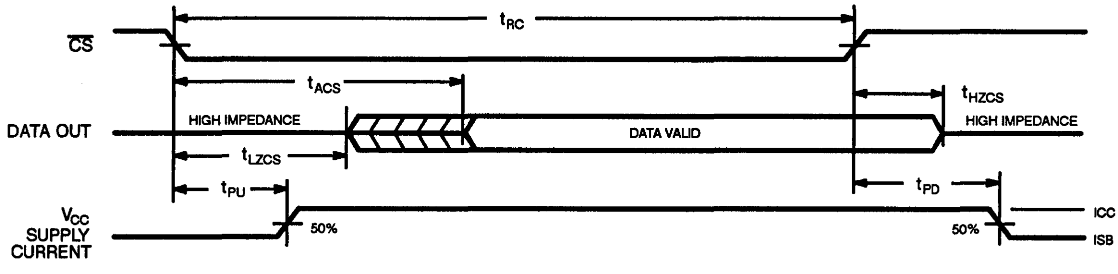
Read Cycle No. 1[9, 10]



1830-5

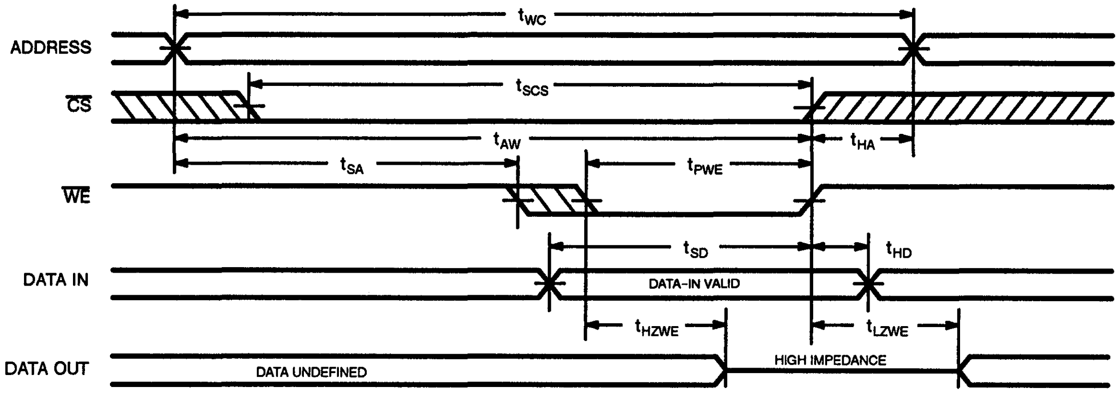
Switching Waveforms (continued)

Read Cycle No. 2[9, 10]



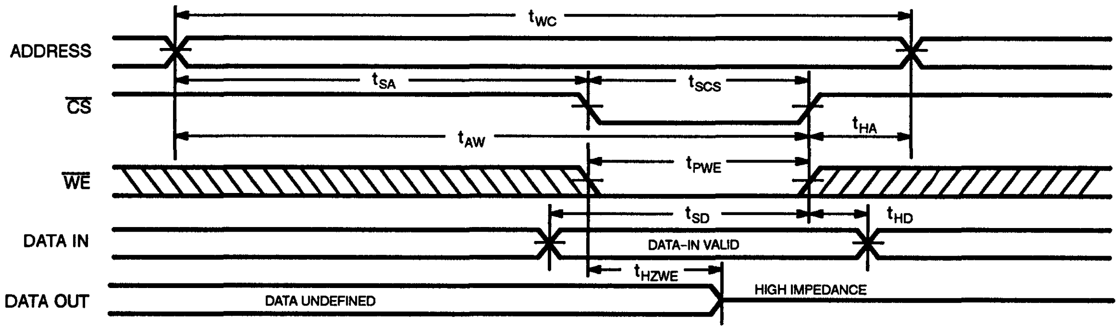
1830-6

Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]



1830-7

Write Cycle No. 2 ($\overline{CS}$ Controlled)[8, 12]



1830-8

8

Truth Table

$\overline{CS}_X$	$\overline{WE}_X$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	M1830HD-25C	HD06	Commercial
30	M1830HD-30C	HD06	Commercial
35	M1830HD-35C	HD06	Commercial
	M1830HD-35MB	HD06	Military
45	M1830HD-45C	HD06	Commercial
	M1830HD-45MB	HD06	Military
55	M1830HD-55C	HD06	Commercial
	M1830HD-55MB	HD06	Military

Document #: 38-M-00017-A

CYM1831

CYPRESS SEMICONDUCTOR

64K x 32 Static RAM Module

Features

- **High-density 2-Mbit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 25 ns**
- **Low active power**
  - **— 4W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .50 in.**
- **Small PCB footprint**
  - **— 1.2 sq. in.**
- **JEDEC-compatible pinout**

Functional Description

The CYM1831 is a high-performance 2-Mbit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$ and $\overline{CS_4}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

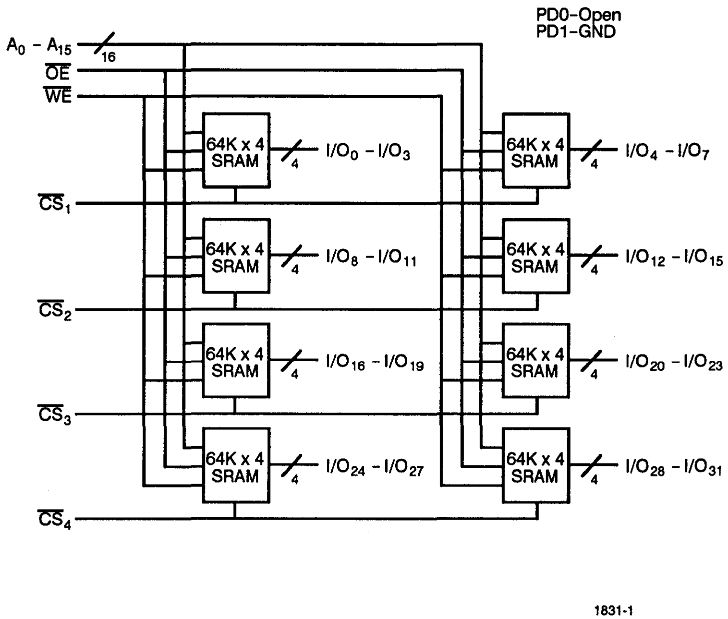
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS_N}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects ($\overline{CS_N}$) LOW and output enable ($\overline{OE}$) low, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

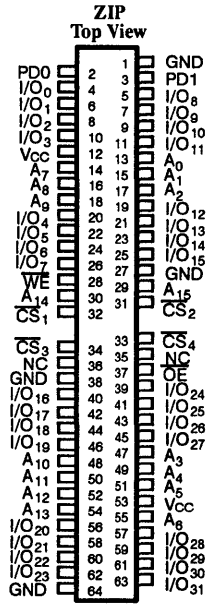
Two pins (PD0 and PD1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

Logic Block Diagram



1831-1

Pin Configuration



1831-2

Selection Guide

	1831PM-25 1831PZ-25	1831PM-30 1831PZ-30	1831PM-35 1831PZ-35	1831PM-45 1831PZ-45
Maximum Access Time (ns)	25	30	35	45
Maximum Operating Current (mA)	720	720	720	720
Maximum Standby Current (mA)	160	160	160	160

8

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... 0°C to +70°C

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1831PZ		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		–0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	–20	+20	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	–20	+20	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_N \leq V_{IL}$		720	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}; $\overline{CS}_N \geq V_{IH}$ Min. Duty Cycle = 100%		320	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[1]	Max. V_{CC}, $\overline{CS}_N \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V		160	mA

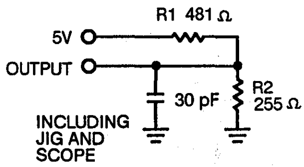
Capacitance[2]

Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance (A_0 – A_{16}, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	80	pF
C_{INB}	Input Capacitance (I/O_0 – I/O_{31})		15	pF
C_{OUT}	Output Capacitance		15	pF

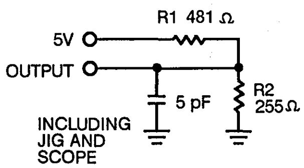
Notes:

1. A pull-up resistor to V_{CC} on the CS input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
2. Tested on a sample basis.

AC Test Loads and Waveforms

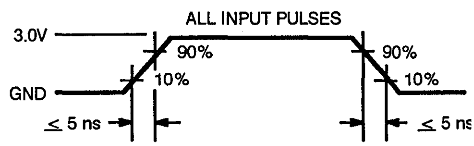


(a)



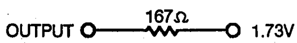
(b)

1831-3



1831-4

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

Parameters	Description	1831PM-25 1831PZ-25		1831PM-30 1831PZ-30		1831PM-35 1831PZ-35		1831PM-45 1831PZ-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_{AA}	Address to Data Valid		25		30		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		30		35		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		20		30	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		15		20		20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	3		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]		13		15		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		30		35		45	ns
WRITE CYCLE [7]										
t_{WC}	Write Cycle Time	25		30		35		45		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		30		40		ns
t_{AW}	Address Set-Up to Write End	20		25		30		40		ns
t_{HA}	Address Hold from Write End	2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		25		25		30		ns
t_{SD}	Data Set-Up to Write End	15		15		20		20		ns
t_{HD}	Data Hold from Write End	2		2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	13	0	15	0	20	0	20	ns

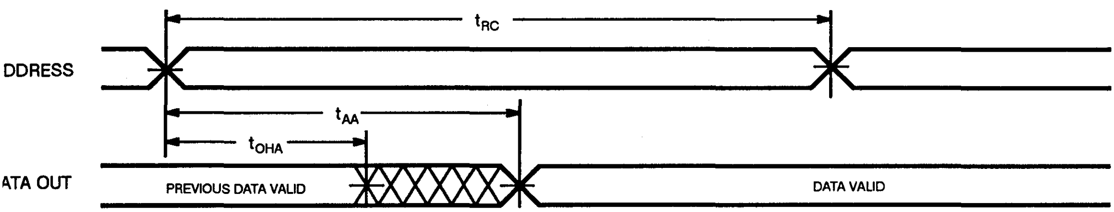
8

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. $\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$ and $\overline{CS_4}$ are represented by $\overline{CS}$ in the switching Characteristics and Waveforms.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms [11]

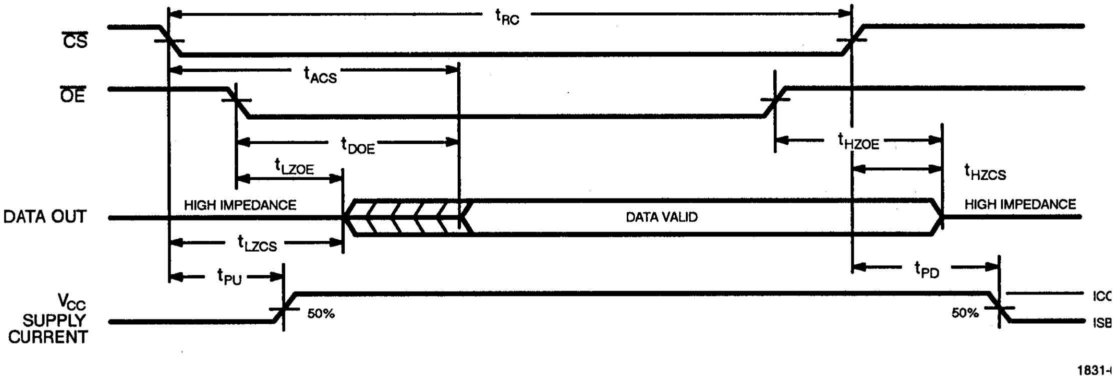
Read Cycle No. 1 [8, 9]



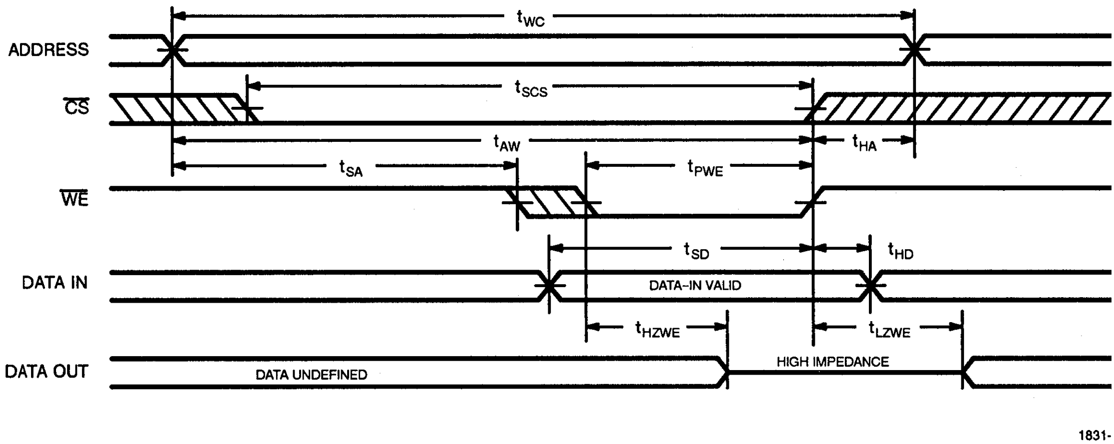
1831-5

Switching Waveforms (continued)

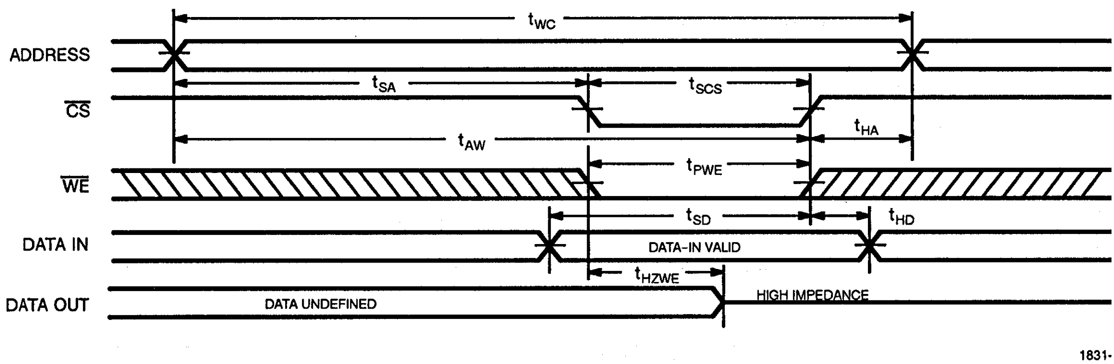
Read Cycle No. 2[8, 10]



Write Cycle No. 1 (WE Controlled)[7]



Write Cycle No. 2 (CS Controlled)[7, 12]



Truth Table

$\overline{CS_N}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1831PM-25C	PM01	Commercial
	CYM1831PZ-25C	PZ01	
30	CYM1831PM-30C	PM01	Commercial
	CYM1831PZ-30C	PZ01	
35	CYM1831PM-35C	PM01	Commercial
	CYM1831PZ-35C	PZ01	
45	CYM1831PM-45C	PM01	Commercial
	CYM1831PZ-45C	PZ01	

Document #: 38-M-00018-A

8

CYPRESS SEMICONDUCTOR

CYM1832

64K x 32 Static RAM Module

Features

- **High-density 2-Mbit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 25 ns**
- **Low active power**
  - **— 5.4W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .50 in.**
- **Small PCB footprint**
  - **— 1.0 sq. in.**

Functional Description

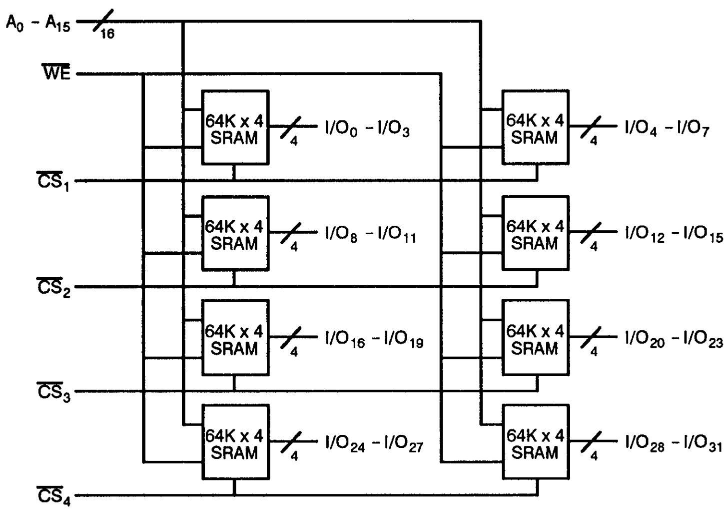
The CYM1832 is a high-performance 2-Mbit static RAM module organized as 64K words by 32 bits. This module is constructed from eight 64K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$, and $\overline{CS_4}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS_N}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_X) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip selects ($\overline{CS_N}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_X).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

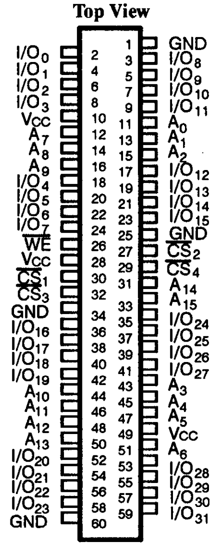
Logic Block Diagram



1832-1

Pin Configuration

ZIP
Top View



1832-2

Selection Guide

	1832PZ-25	1832PZ-35	1832PZ-45	1832PZ-55
Maximum Access Time (ns)	25	35	45	55
Maximum Operating Current (mA)	980	980	980	980
Maximum Standby Current (mA)	240	240	240	240

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −45°C to +125°C

Ambient Temperature with Power Applied .... −10°C to +85°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1832PZ		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage [1]		−0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	−20	+20	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	−100	+100	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_N \leq V_{IL}$		980	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}; $\overline{CS}_N \geq V_{IH}$ Min. Duty Cycle = 100%		240	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current [2]	Max. V_{CC}; $\overline{CS}_N \geq V_{CC}$ − 0.2V, $V_{IN} \geq V_{CC}$ − 0.2V or $V_{IN} \leq$ 0.2V		120	mA

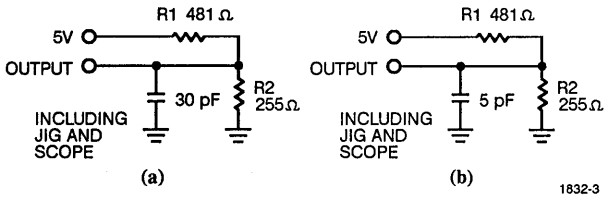
Capacitance[3]

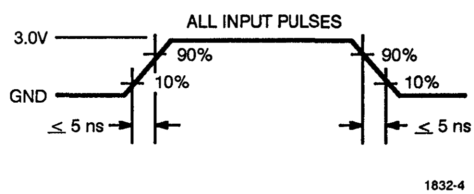
Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance (A_X, $\overline{WE}$)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	60	pF
C_{INB}	Input Capacitance ($\overline{CS}$)		25	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

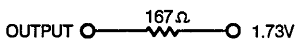
1. $V_{IL(MIN)}$ = −3.0V for pulse widths less than 20ns.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range [4]

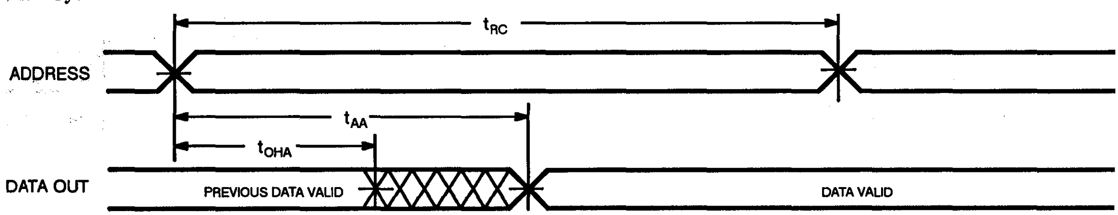
Parameters	Description	1832PZ-25C Min.	1832PZ-25C Max.	1832PZ-35 Min.	1832PZ-35 Max.	1832PZ-45 Min.	1832PZ-45 Max.	1832PZ-55 Min.	1832PZ-55 Max.	Units
READ CYCLE										
t_{RC}	Read Cycle Time	25		35		45		55		ns
t_{AA}	Address to Data Valid		25		35		45		55	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		25		35		45		55	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z [6]	2		3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z [5, 6]	0	15	0	25	0	30	0	30	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		25		35		45		55	ns
WRITE CYCLE [7]										
t_{WC}	Write Cycle Time	25		35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		30		40		45		ns
t_{AW}	Address Set-Up to Write End	20		30		35		45		ns
t_{HA}	Address Hold from Write End	2		2		5		5		ns
t_{SA}	Address Set-Up to Write Start	2		3		5		5		ns
t_{PWE}	$\overline{WE}$ Pulse Width	20		30		35		45		ns
t_{SD}	Data Set-Up to Write End	15		20		25		35		ns
t_{HD}	Data Hold from Write End	3		5		5		5		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [6]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [5, 6]	0	15	0	15	0	20	0	30	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. $\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$ and $\overline{CS}_4$ are represented by $\overline{CS}$ in the Switching Characteristics and Waveforms.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms [11]

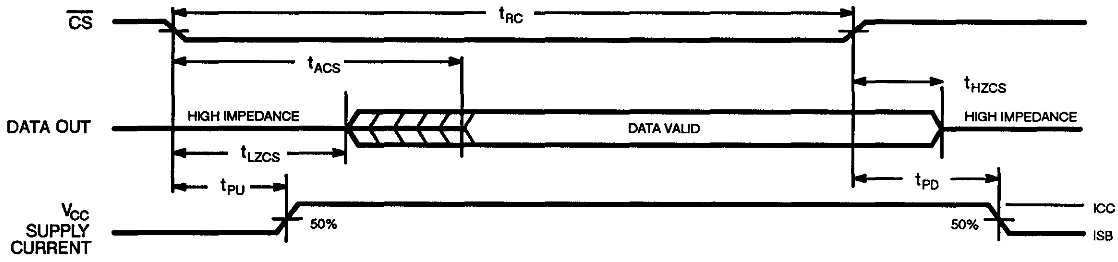
Read Cycle No. 1 [8, 9]



1832-

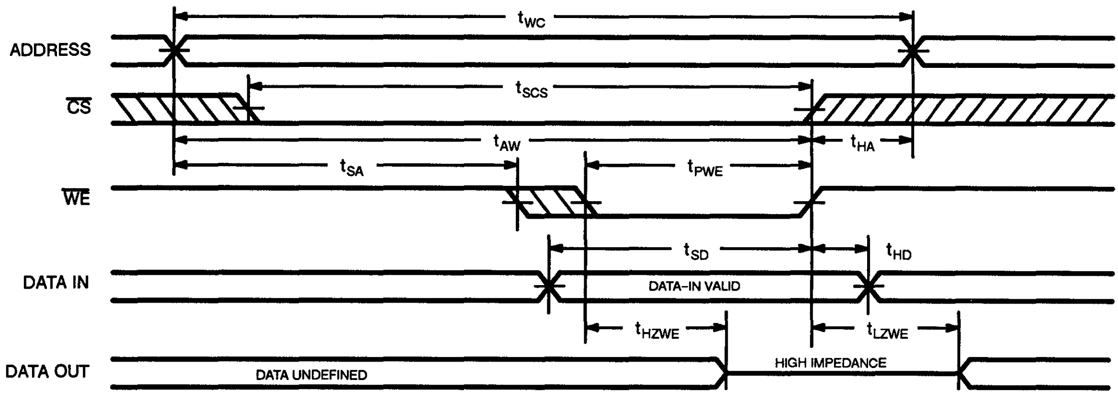
Switching Waveforms (continued)

Read Cycle No. 2[8, 10]



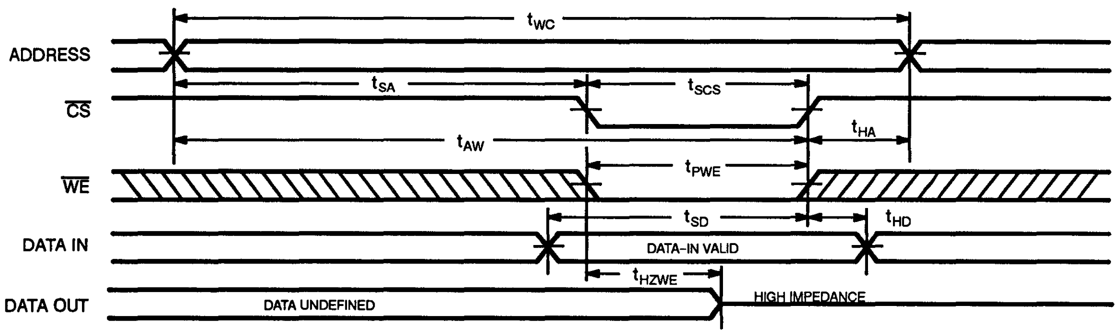
1832-6

Write Cycle No. 1 (WE Controlled)[7]



1832-7

Write Cycle No. 2 (CS Controlled)[7, 12]



1832-8

8

Truth Table

$\overline{CS_N}$	$\overline{WE}$	Input/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1832PZ-25C	PZ02	Commercial
35	CYM1832PZ-35C	PZ02	Commercial
45	CYM1832PZ-45C	PZ02	Commercial
55	CYM1832PZ-55C	PZ02	Commercial

Document #: 38-M-00019-A

256K x 32 Static RAM Module

Features

- **High-density 8-Mbit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 35 ns**
- **Low active power**
  - **— 5.3W (max.)**
- **SMD technology**
- **TTL-compatible inputs and outputs**
- **Low profile**
  - **— Max. height of .58 in.**
- **Small PCB footprint**
  - **— 1.3 sq. in.**
- **JEDEC-compatible pinout**

Functional Description

The CYM1841 is a high-performance 8-Mbit static RAM module organized as 256K words by 32 bits. This module is constructed from eight 256K x 4 SRAMs in SOJ packages mounted on an epoxy laminate board with pins. Four chip selects ($\overline{CS_1}$, $\overline{CS_2}$, $\overline{CS_3}$, $\overline{CS_4}$) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

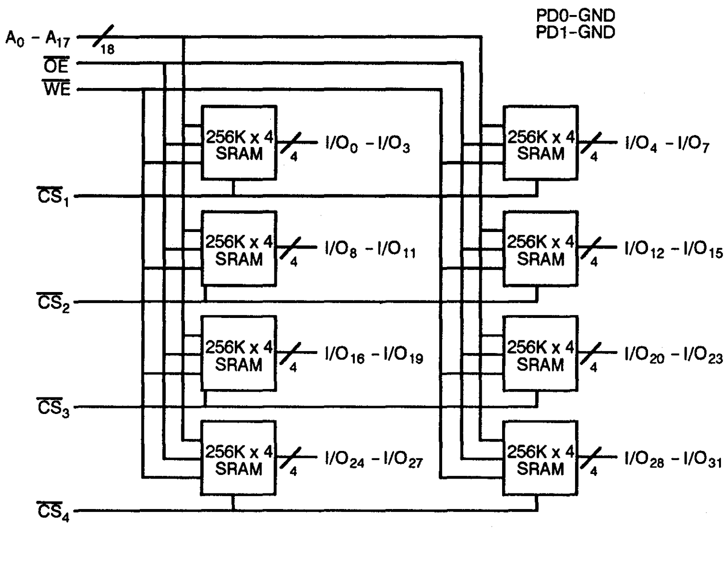
Writing to each byte is accomplished when the appropriate chip selects ($\overline{CS_N}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the input/output pins (I/O_x) is written into the memory location specified on the address pins (A_0 through A_{17}).

Reading the device is accomplished by taking the chip selects ($\overline{CS_N}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the data input/output pins (I/O_x).

The data input/output pins stay in the high-impedance state when write enable ($\overline{WE}$) is LOW, or the appropriate chip selects are HIGH.

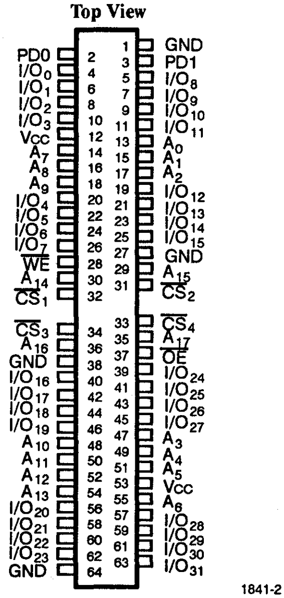
Two pins (PD0 and PD1) are used to identify module memory density in applications where alternate versions of the JEDEC standard modules can be interchanged.

Logic Block Diagram



1841-1

Pin Configuration



1841-2

Selection Guide

	1841PM-35 1841PZ-35	1841PM-45 1841PZ-45	1841PM-55 1841PZ-55
Maximum Access Time (ns)	35	45	55
Maximum Operating Current (mA)	960	960	960
Maximum Standby Current (mA)	480	480	480

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... -55°C to +125°C

Ambient Temperature with Power Applied .... 0°C to +70°C

Supply Voltage to Ground Potential .... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... -0.5V to +7.0V

DC Input Voltage .... -0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1841PZ		Units
			Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = -4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage		-0.5	0.8	V
I_{IX}	Input Load Current	GND $\leq V_I \leq V_{CC}$	-16	+16	mA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled	-10	+10	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA $\overline{CS}_N \leq V_{IL}$		960	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}; $\overline{CS}_N \geq V_{IH}$ Min. Duty Cycle = 100%		480	mA
I_{SB2}	Automatic $\overline{CS}$ Power-Down Current[2]	Max. V_{CC}; $\overline{CS}_N \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V		16	mA

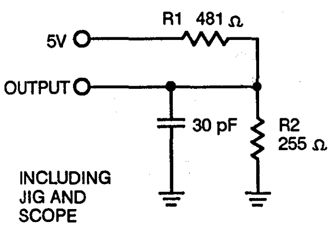
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	70	pF
C_{OUT}	Output Capacitance		20	pF

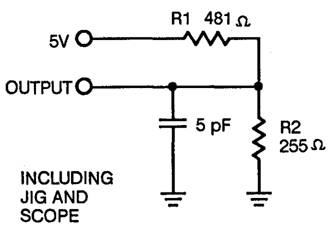
Notes:

1. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

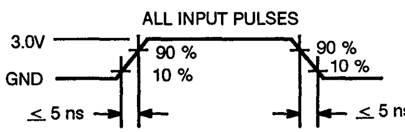


(a)



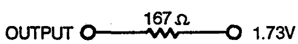
(b)

1841-3



1841

Equivalent to: THÉVENIN EQUIVALENT



Switching Characteristics Over the Operating Range[4]

Parameters	Description	1841PM-35 1841PZ-35		1841PM-45 1841PZ-45		1841PM-55 1841PZ-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address to Data Valid		35		45		55	ns
t_{OHA}	Data Hold from Address Change	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		35		45		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		30		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z		15		15		15	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	10		10		10		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5,6]		20		20		20	ns
t_{PU}	$\overline{CS}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CS}$ HIGH to Power-Down		35		45		55	ns
WRITE CYCLE[7]								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	30		40		50		ns
t_{AW}	Address Set-Up to Write End	30		40		50		ns
t_{HA}	Address Hold from Write End	2		2		2		ns
t_{SA}	Address Set-Up to Write Start	2		2		2		ns
t_{PWE}	$\overline{WE}$ Pulse Width	30		35		45		ns
t_{SD}	Data Set-Up to Write End	20		25		35		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[5,6]	0	10	0	15	0	15	ns

Notes:

4. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$ and $\overline{OE} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. $\overline{CS}_1, \overline{CS}_2, \overline{CS}_3, \overline{CS}_4$ are represented by $\overline{CS}$ in the Switching Characteristics and Waveforms.
12. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

8

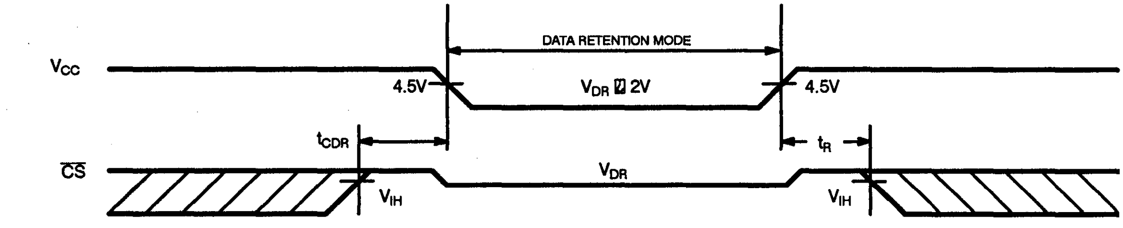
Data Retention Characteristics (L Version Only)

Parameter	Description	Test Conditions	CYM1841		Units
			Min.	Max.	
V_{DR}	V_{CC} for Retention Data	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0		V
I_{CCDR}	Data Retention Current			800	mA
t_{CDR}[14]	Chip Deselect to Data Retention Time		0		ns
t_R[14]	Operation Recovery Time		5		ms

Notes:

13. t_{RC} = Read Cycle Time.
14. Guaranteed, not tested.

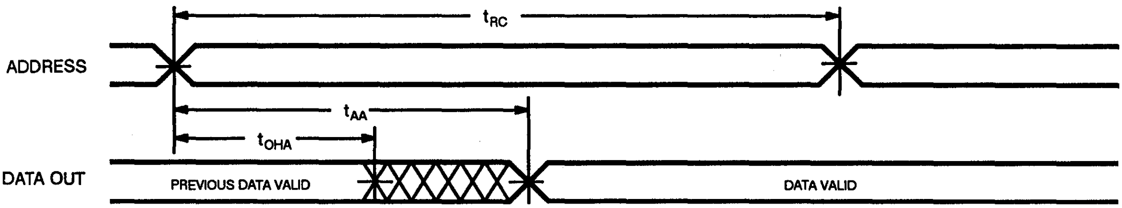
Data Retention Waveform



1841-5

Switching Waveforms [11]

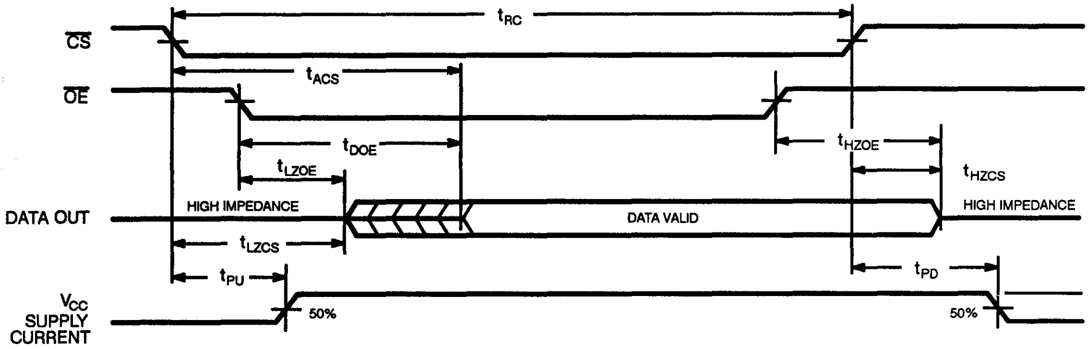
Read Cycle No. 1[8, 9]



1841-6

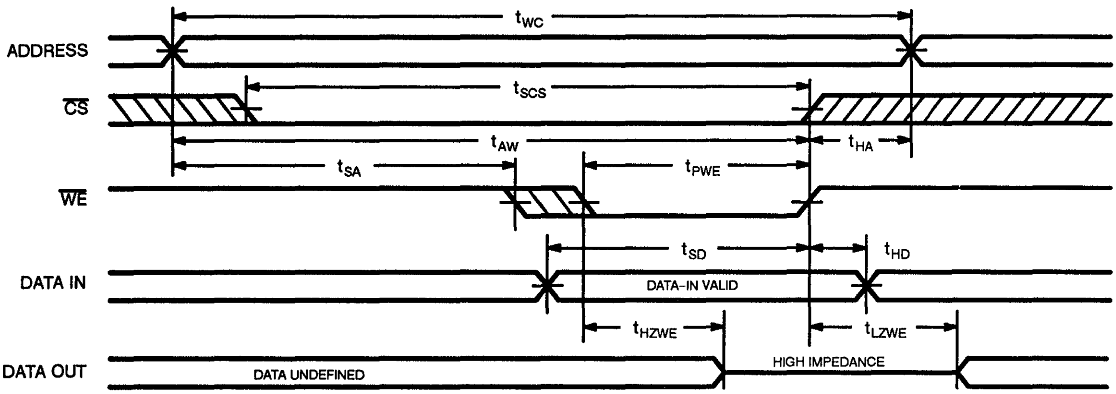
Switching Waveforms (continued)

Read Cycle No. 2[8,10]



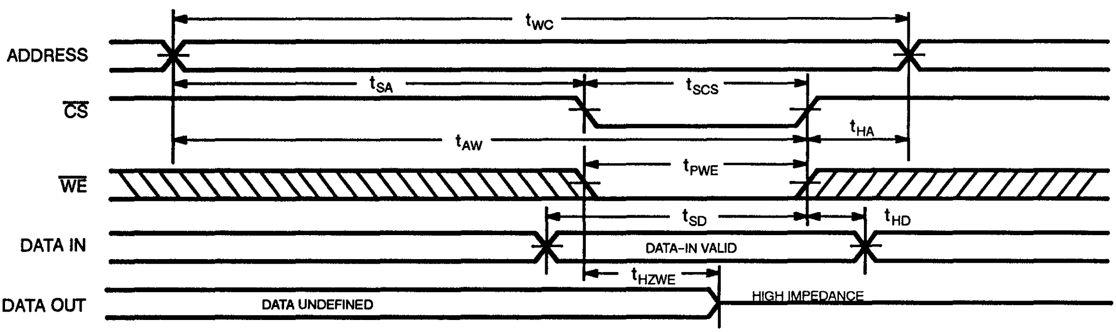
1841-7

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



1841-8

Write Cycle No. 2 ($\overline{CS}$ Controlled)[7, 12]



1841-9

8

Truth Table

$\overline{CS_N}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
35	CYM1841PM-35C	PM02	Commercial
	CYM1841LPM-35C	PM02	
	CYM1841PZ-35C	PZ03	
	CYM1841LPZ-35C	PZ03	
45	CYM1841PM-45C	PM02	Commercial
	CYM1841LPM-45C	PM02	
	CYM1841PZ-45C	PZ03	
	CYM1841LPZ-45C	PZ03	
55	CYM1841PM-55C	PM02	Commercial
	CYM1841LPM-55C	PM02	
	CYM1841PZ-55C	PZ03	
	CYM1841LPZ-55C	PZ03	

Document #: 38-M-00031

CYPRESS SEMICONDUCTOR

16K x 68 SRAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **— Access time of 25 ns**
- **Low active power**
  - **— 10.4W (max.)**
- **SMD technology**
- **Registered address inputs**
- **Four completely independent memory banks**
- **Small PCB footprint**
  - **— 1.9 sq. in.**

Functional Description

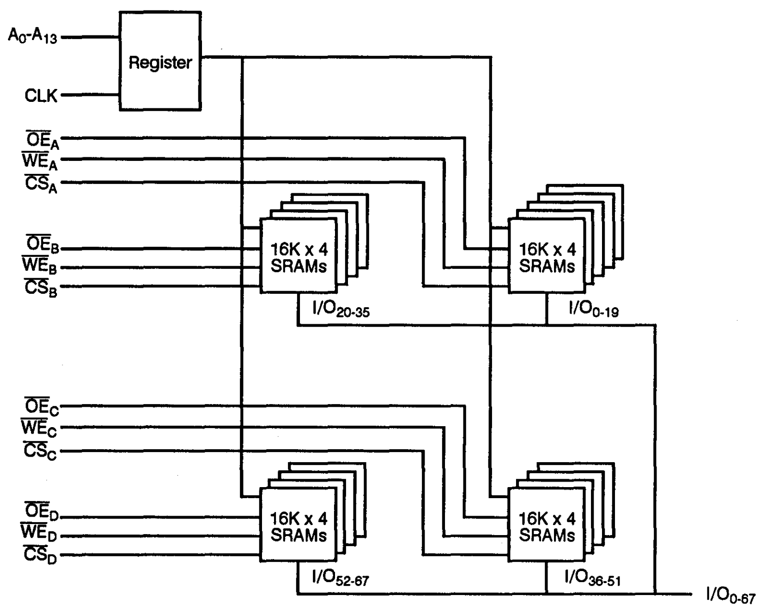
The CYM1910 is a very high performance 1-megabit static RAM module organized as 16K words by 68 bits. This module is constructed using seventeen 16K x 4 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins. The memory is organized as three banks of 16K x 16 and one of 16K x 20, each of which has its own chip select, write enable, and output enable signals.

Writing to the module is accomplished when the appropriate chip select ($\overline{CS}_x$) and write enable ($\overline{WE}_x$) inputs are both LOW. Data on the appropriate input/output pins (I/O_{nn}) of the device is written into the memory location specified by the content of the address register. The address register is loaded on the rising edge of the clock signal (CLK).

Reading the device is accomplished by taking chip select ($\overline{CS}_x$) and output enable ($\overline{OE}_x$) low while $\overline{WE}_x$ remains inactive or HIGH. Under these conditions, the contents of the memory location specified by the contents of the address register will appear on the appropriate data input/output pins (I/O_{nn}).

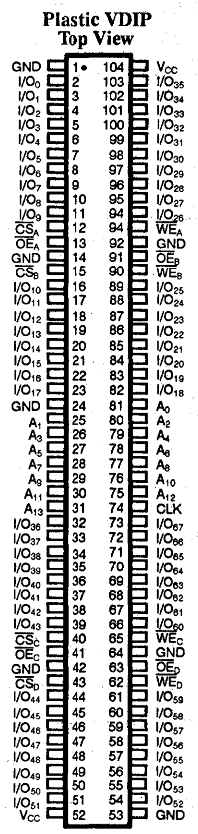
The data input/output pins remain in a high-impedance state when chip select ($\overline{CS}_x$) or output enable ($\overline{OE}_x$) is HIGH, or when write enable ($\overline{WE}_x$) is LOW.

Logic Block Diagram



1910-1

Pin Configuration



1910-2

8

Selection Guide

	1910PV-25	1910PV-35	1910PV-45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	1900	1900	1900
Maximum Standby Current (mA)	650	650	650

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −45°C to +125°C

Ambient Temperature with Power Applied .... −10°C to +85°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1910PV Min.	CYM1910PV Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	V
I_{IXA}	Input Load Current $\overline{OE}$, $\overline{WE}$, $\overline{CS}$	GND ≤ V_I ≤ V_{CC}	−15	+15	μA
I_{IXB}	Input Load Current A_0 - A_{13}, CLK	GND ≤ V_I ≤ V_{CC}	−1.2	+.040	mA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−15	+15	μA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		1900	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		650	mA

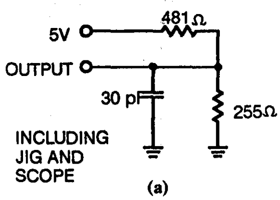
Capacitance[3]

Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance (A_0 - A_{13}, CLK)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	20	pF
C_{INB}	Input Capacitance ($\overline{OE}$, $\overline{WE}$, $\overline{CS}$)		35	pF
C_{OUT}	Output Capacitance		15	pF

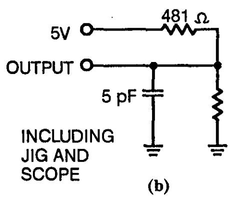
Notes:

1. $V_{IL(MIN)}$ = −3.0V for pulse widths less than 20 ns.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms

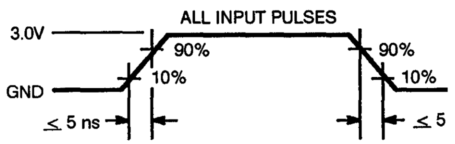


(a)



(b)

1910-3



191

Switching Characteristics Over the Operating Range[4]

Parameters	Description	1910PV-25		1910PV-35		1910PV-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time CLK Cycle Time	25		35		45		ns
t_{CA}	CLK to Data Valid Access Time		25		35		45	ns
t_{SAC}	Address Set-Up to CLK Rising Edge	3		4		4		ns
t_{HAC}	Address Hold from CLK Rising Edge	2		2		2		ns
t_{OHC}	Data Hold from CLK Rising Edge	5		5		5		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		30		40	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]	0	10	0	15	0	20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5,6]		10		15		20	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SAC}	Address Set-Up to CLK Rising Edge	3		4		4		ns
t_{HAC}	Address Hold from CLK Rising Edge	2		2		2		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		35		ns
t_{CW}	CLK Rising Edge Set-Up to Write End	25		30		40		ns
t_{HC}	CLK Rising Edge Hold from Write End	0		0		0		ns
t_{SC}	CLK Rising Edge Set-Up to Write Start	10		10		10		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		10		15		20	ns

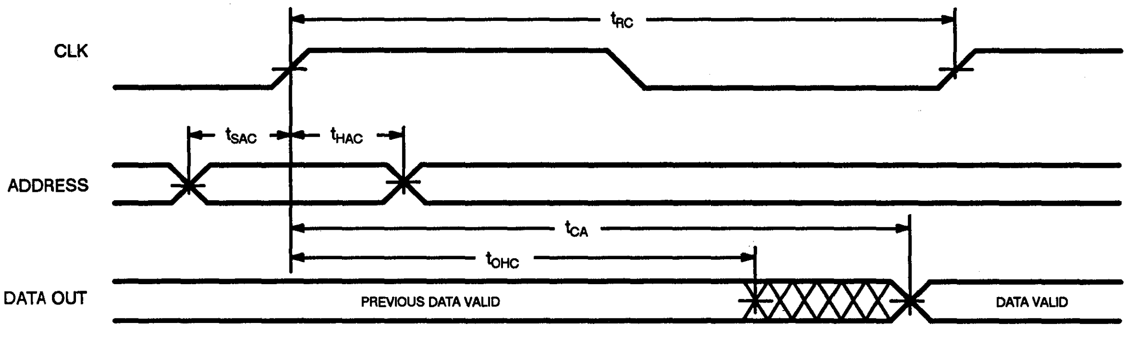
Notes:

4. Test Conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZOE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

8

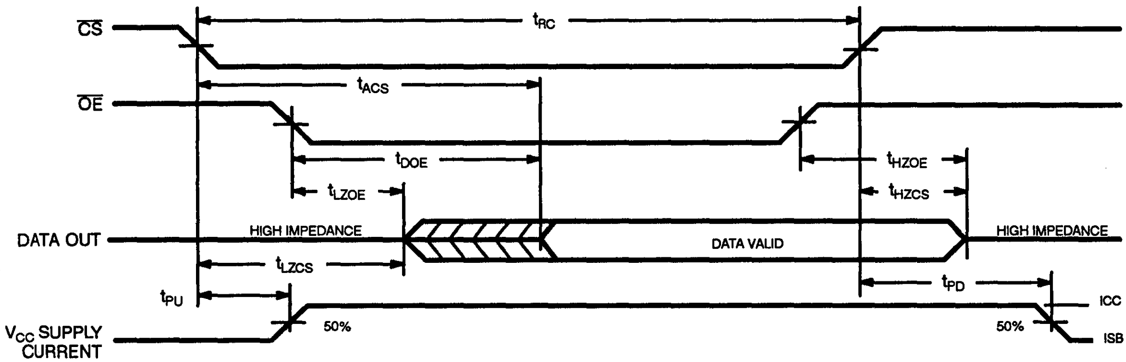
Switching Waveforms

Read Cycle No. 1[8,9]



1910-5

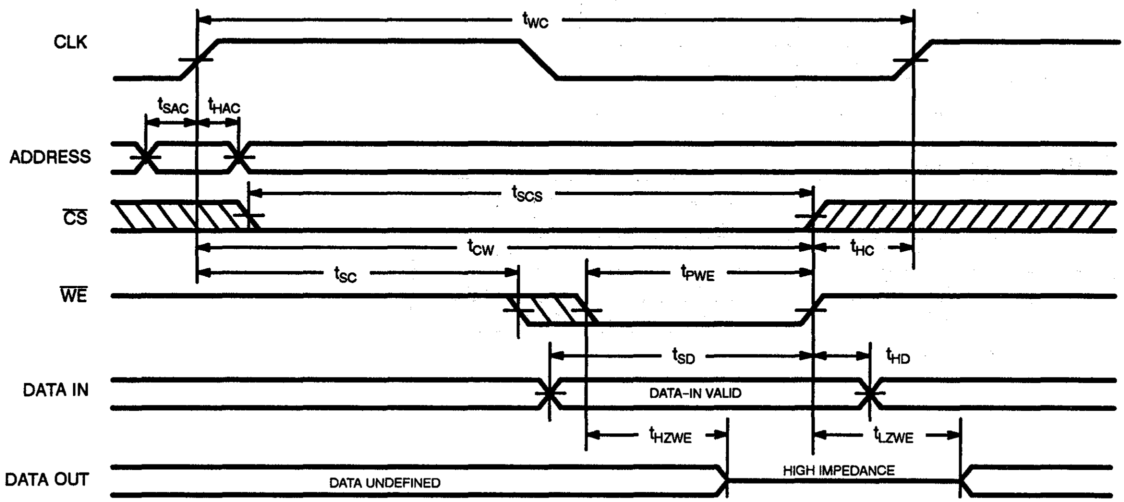
Read Cycle No. 2[8,10]



1910-6

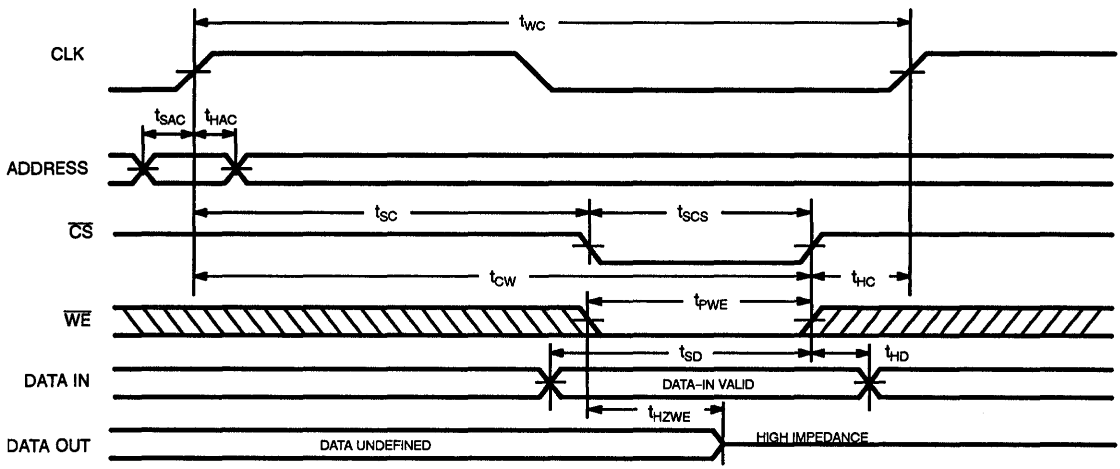
Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled)[7]



1910-7

Write Cycle No. 2 ($\overline{CS}$ Controlled[7, 11]



1910-8

8

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1910PV-25C	PV02	Commercial
35	CYM1910PV-35C	PV02	Commercial
45	CYM1910PV-45C	PV02	Commercial

Document #: 38-M-00023-A

CYPRESS SEMICONDUCTOR

16K x 68 SRAM Module

Features

- **High-density 1-megabit SRAM module**
- **High-speed CMOS SRAMs**
  - **Access time of 25 ns**
- **Low active power**
  - **10.4W (max.)**
- **SMD technology**
- **Latched address inputs**
- **Four completely independent memory banks**
- **Small PCB footprint**
  - **1.9 sq. in.**

Functional Description

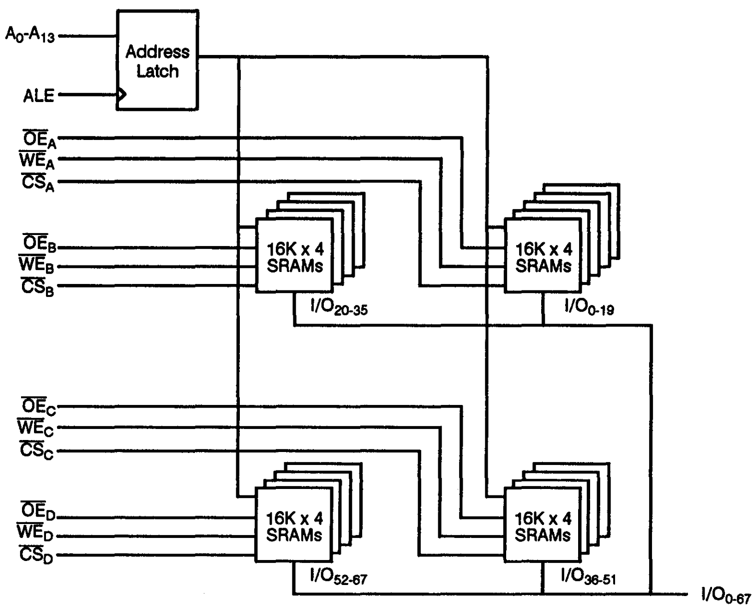
The CYM1911 is a very high performance 1-megabit static RAM module organized as 16K words by 68 bits. This module is constructed using seventeen 16K x 4 static RAMs in SOJ packages mounted onto an epoxy laminate board with pins. The memory is organized as three banks of 16K x 16 and one of 16K x 20, each of which has its own chip select, write enable, and output enable signals.

Writing to the module is accomplished when the appropriate chip select ($\overline{CS}_X$) and write enable ($\overline{WE}_X$) inputs are both LOW. If Latch Enable (ALE) is HIGH, data on the appropriate input/output pins (I/O_{nn}) of the device is written into the memory location specified on the address pins (A_0 through A_{13}). If ALE is LOW, data is written into the address specified by the contents of the address latch. The value in this latch is updated on the falling edge of ALE.

Reading the device is accomplished by taking chip select ($\overline{CS}_X$) and output enable ($\overline{OE}_X$) LOW while $\overline{WE}_X$ remains inactive or HIGH. If Latch Enable (ALE) is HIGH, the contents of the memory location specified on the address pins (A_0 through A_{13}) will appear on the appropriate data input/output pins (I/O_{nn}). If ALE is LOW, the contents of the memory location specified by the value in the address latch will appear on I/O_{nn}.

The data input/output pins remain in a high-impedance state when chip select ($\overline{CS}_X$) or output enable ($\overline{OE}_X$) is HIGH, or when write enable ($\overline{WE}_X$) is LOW.

Logic Block Diagram



1911-1

Pin Configuration

Plastic VDIP

Signal	Pin	Pin	Signal
GND	1	104	V_{CC}
I/O_0	2	103	I/O_{35}
I/O_1	3	102	I/O_{34}
I/O_2	4	101	I/O_{33}
I/O_3	5	100	I/O_{32}
I/O_4	6	99	I/O_{31}
I/O_5	7	98	I/O_{30}
I/O_6	8	97	I/O_{29}
I/O_7	9	96	I/O_{28}
I/O_8	10	95	I/O_{27}
I/O_9	11	94	I/O_{26}
$\overline{CS}_A$	12	94	$\overline{WE}_A$
$\overline{OE}_A$	13	92	GND
GND	14	91	$\overline{OE}_B$
$\overline{CS}_B$	15	90	$\overline{WE}_B$
I/O_{10}	16	89	I/O_{25}
I/O_{11}	17	88	I/O_{24}
I/O_{12}	18	87	I/O_{23}
I/O_{13}	19	86	I/O_{22}
I/O_{14}	20	85	I/O_{21}
I/O_{15}	21	84	I/O_{20}
I/O_{16}	22	83	I/O_{19}
I/O_{17}	23	82	I/O_{18}
GND	24	81	A_0
A_1	25	80	A_2
A_3	26	79	A_4
A_5	27	78	A_6
A_7	28	77	A_8
A_9	29	76	A_{10}
A_{11}	30	75	A_{12}
A_{13}	31	74	ALE
I/O_{36}	32	73	I/O_{67}
I/O_{37}	33	72	I/O_{66}
I/O_{38}	34	71	I/O_{65}
I/O_{39}	35	70	I/O_{64}
I/O_{40}	36	69	I/O_{63}
I/O_{41}	37	68	I/O_{62}
I/O_{42}	38	67	I/O_{61}
I/O_{43}	39	66	I/O_{60}
$\overline{CS}_C$	40	65	$\overline{WE}_C$
$\overline{OE}_C$	41	64	GND
GND	42	63	$\overline{OE}_D$
$\overline{CS}_D$	43	62	$\overline{WE}_D$
I/O_{44}	44	61	I/O_{59}
I/O_{45}	45	60	I/O_{58}
I/O_{46}	46	59	I/O_{57}
I/O_{47}	47	58	I/O_{56}
I/O_{48}	48	57	I/O_{55}
I/O_{49}	49	56	I/O_{54}
I/O_{50}	50	55	I/O_{53}
I/O_{51}	51	54	I/O_{52}
V_{CC}	52	53	GND

1911-2

8

Selection Guide

	1911PV-25	1911PV-35	1911PV-45
Maximum Access Time (ns)	25	35	45
Maximum Operating Current (mA)	1900	1900	1900
Maximum Standby Current (mA)	650	650	650

Maximum Ratings

(Above which the useful life may be impaired)

Storage Temperature .... −45°C to +125°C

Ambient Temperature with Power Applied .... −10°C to +85°C

Supply Voltage to Ground Potential .... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State .... −0.5V to +7.0V

DC Input Voltage .... −0.5V to +7.0V

Output Current into Outputs (Low) .... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameters	Description	Test Conditions	CYM1911PV Min.	CYM1911PV Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]		−0.5	0.8	V
I_{IXA}	Input Load Current $\overline{OE}$, $\overline{WE}$, $\overline{CS}$	GND ≤ V_I ≤ V_{CC}	−15	+15	µA
I_{IXB}	Input Load Current A_0 - A_{13}, ALE	GND ≤ V_I ≤ V_{CC}	−1.2	+.040	mA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	−15	+15	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, $\overline{CS}$ ≤ V_{IL}		1900	mA
I_{SB1}	Automatic $\overline{CS}$ Power-Down Current[2]	V_{CC} = Max., $\overline{CS}$ ≥ V_{IH}, Min. Duty Cycle = 100%		650	mA

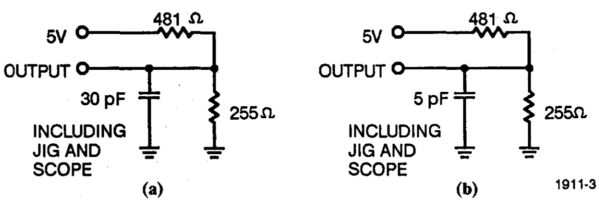
Capacitance[3]

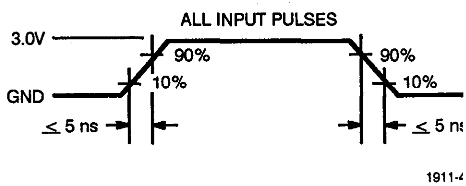
Parameters	Description	Test Conditions	Max.	Units
C_{INA}	Input Capacitance (A_0 - A_{13}, ALE)	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	20	pF
C_{INB}	Input Capacitance ($\overline{OE}$, $\overline{WE}$, $\overline{CS}$)		35	pF
C_{OUT}	Output Capacitance		15	pF

Notes:

1. $V_{IL(MIN)}$ = −3.0V for pulse widths less than 20 ns.
2. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested on a sample basis.

AC Test Loads and Waveforms





Switching Characteristics Over the Operating Range[4]

Parameters	Description	1911PV-25		1911PV-35		1911PV-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time ALE Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{LA}	ALE to Data Valid Access Time	25		35		45		ns
t_{SAL}	Address Set-Up to ALE Falling Edge	3		4		4		ns
t_{HAL}	Address Hold from ALE Falling Edge	2		2		2		ns
t_{OHL}	Data Hold from ALE Falling Edge	3		3		3		ns
t_{ACS}	$\overline{CS}$ LOW to Data Valid		20		30		40	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		15		20		25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[5]	0	10	0	15	0	20	ns
t_{LZCS}	$\overline{CS}$ LOW to Low Z[6]	3		3		3		ns
t_{HZCS}	$\overline{CS}$ HIGH to High Z[5,6]		10		15		20	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	25		35		45		ns
t_{SAL}	Address Set-Up to ALE Falling Edge	3		4		4		ns
t_{HAL}	Address Hold from ALE Falling Edge	2		2		2		ns
t_{SCS}	$\overline{CS}$ LOW to Write End	20		25		35		ns
t_{LW}	ALE Falling Edge Set-Up to Write End	25		30		40		ns
t_{HL}	ALE Falling Edge Hold From Write End	0		0		0		ns
t_{SL}	ALE Falling Edge Set-Up to Write Start	10		10		10		ns
t_{PWE}	$\overline{WE}$ Pulse Width	15		20		25		ns
t_{SD}	Data Set-Up to Write End	15		20		25		ns
t_{HD}	Data Hold from Write End	2		2		2		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z		10		10		20	ns

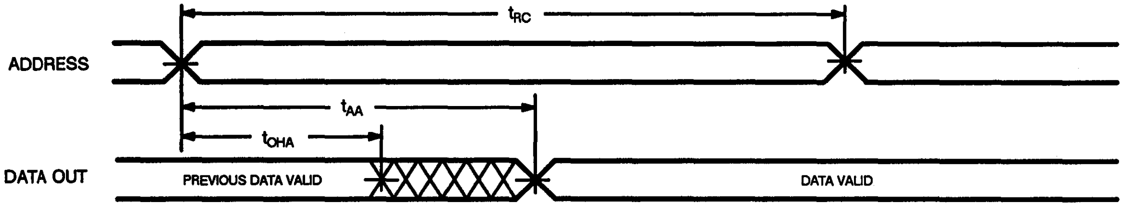
Notes:

4. Test Conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. t_{HZCS} and t_{HZOE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
6. At any given temperature and voltage condition, t_{HZCS} is less than t_{LZCS} for any given device. These parameters are guaranteed and not 100% tested.
7. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

8

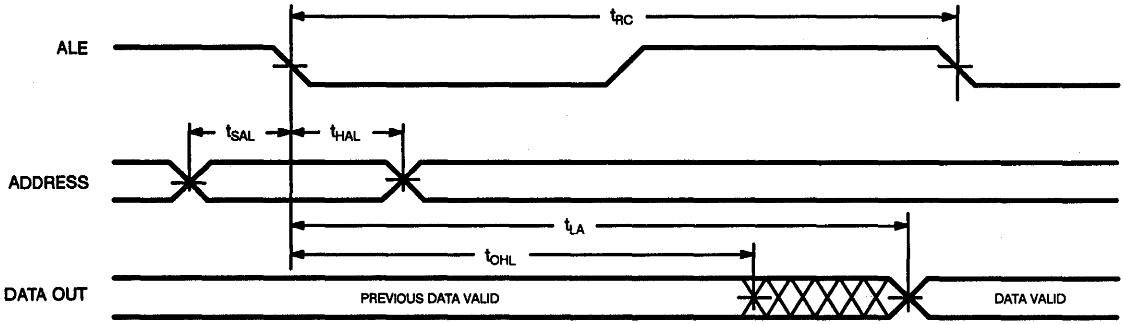
Switching Waveforms

Read Cycle No. 1a (Buffered Address Mode)[8,9]



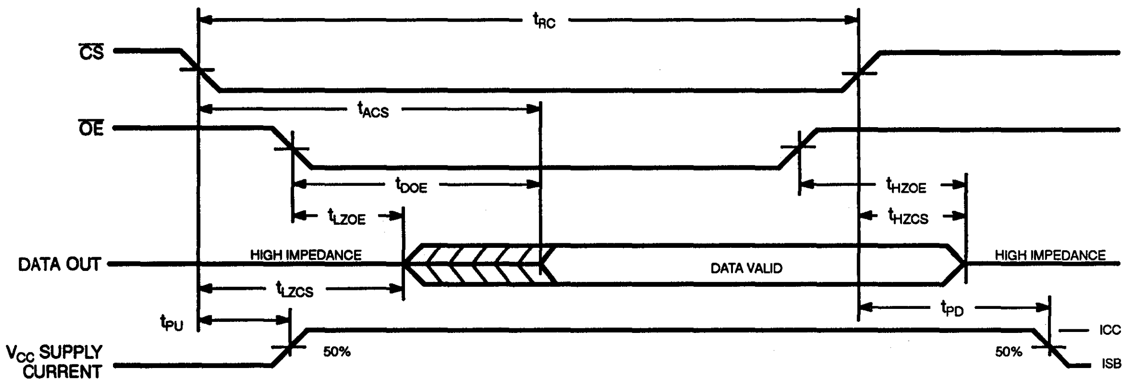
1911-5

Read Cycle No. 1b (Latched Address Mode)[8,9]



1911-6

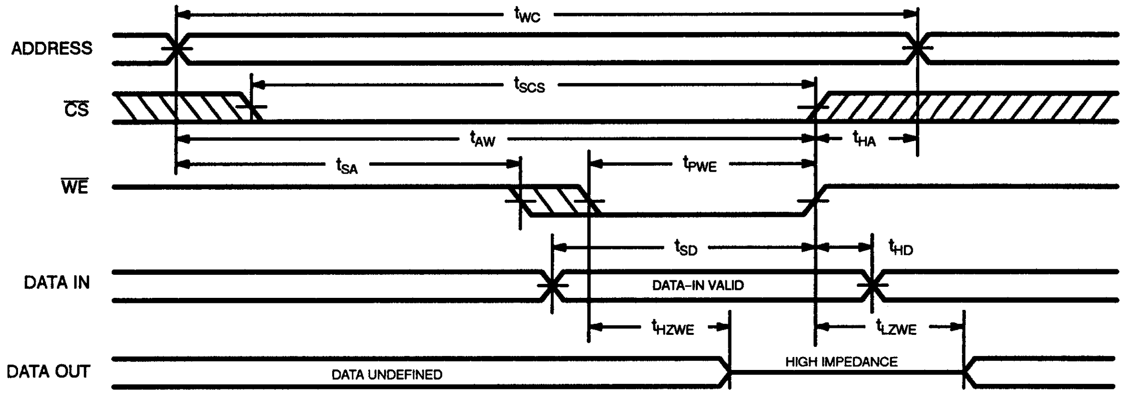
Read Cycle No. 2[8,10]



1911-7

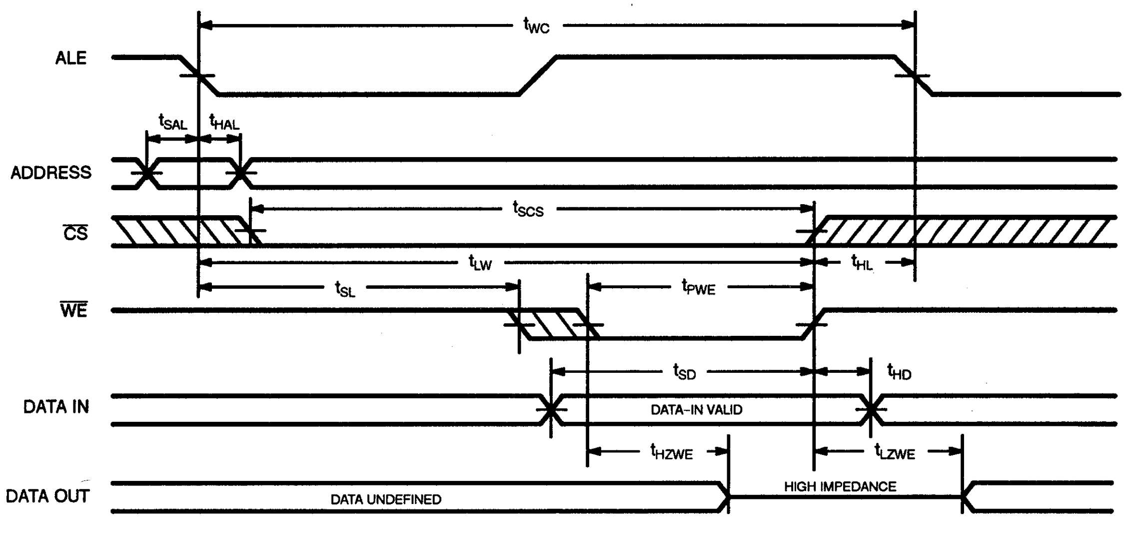
Switching Waveforms (continued)

Write Cycle No. 1a ($\overline{WE}$ Controlled, Buffered Address Mode)[7]



1911-8

Write Cycle No. 1b ($\overline{WE}$ Controlled, Latched Address Mode)[7]

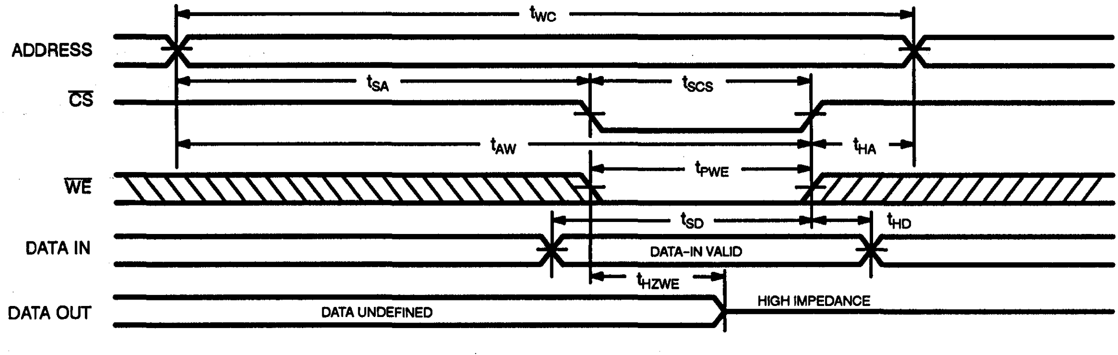


1911-9

8

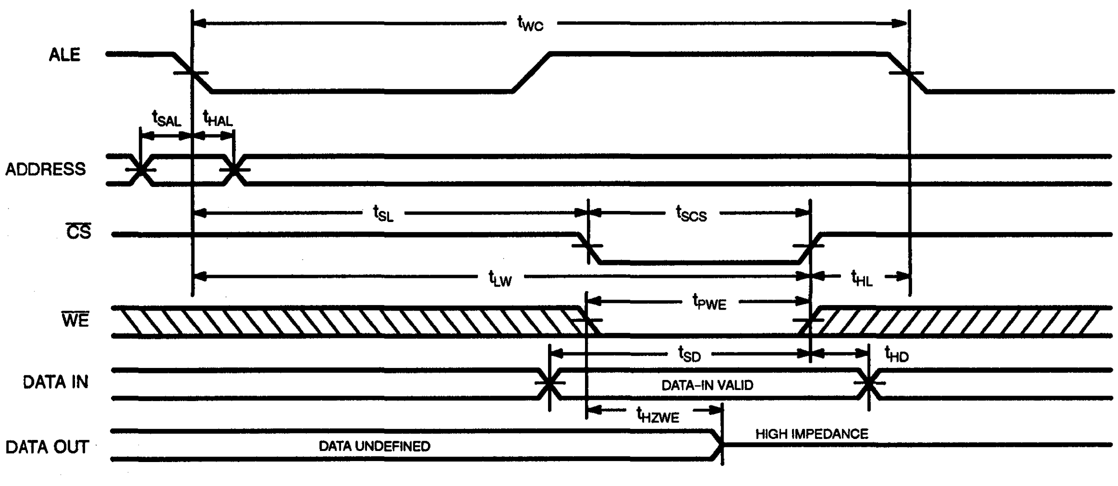
Switching Waveforms (continued)

Write Cycle No. 2a ($\overline{CS}$ Controlled, Buffered Address Mode)[7, 11]



1911-10

Write Cycle No. 2b ($\overline{CS}$ Controlled, Latched Address Mode)[7, 11]



1911-11

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read Word
L	L	X	Data In	Write Word
L	H	H	High Z	Deselect

Ordering Information

Speed	Ordering Code	Package Type	Operating Range
25	CYM1911PV-25C	PV02	Commercial
35	CYM1911PV-35C	PV02	Commercial
45	CYM1911PV-45C	PV02	Commercial

Document #: 38-M-00024-A

8

CYPRESS SEMICONDUCTOR

Cascadeable 8K x 9 FIFO

Features

- **8K x 9 FIFO buffer memory**
- **Asynchronous read/write**
- **High-speed 20-MHz read/write**
- **Pin-compatible with 7C42X series of monolithic FIFOs**
- **Low operating power**
  - **I_{CC} (max.) = 350 mA**
- **600-mil DIP package**
- **Empty, full flags**
- **Small PCB footprint**
  - **0.84 sq. in.**
- **Expandable in depth and width**

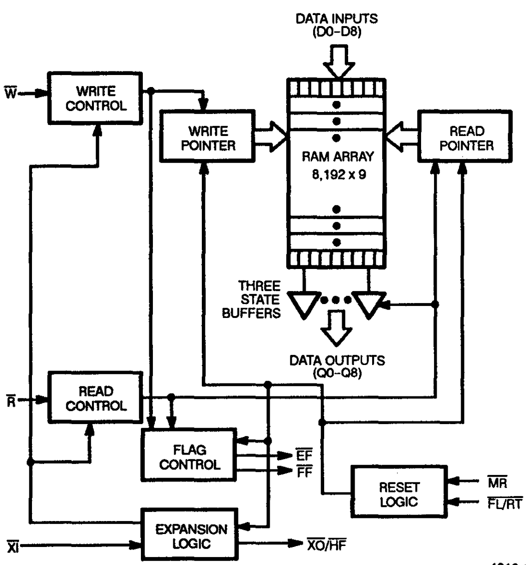
Functional Description

The CYM4210 is a first-in first-out (FIFO) memory module that is 8,192 words by 9 bits wide. It is offered in a 600-mil-wide DIP package. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 20 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The 9 data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

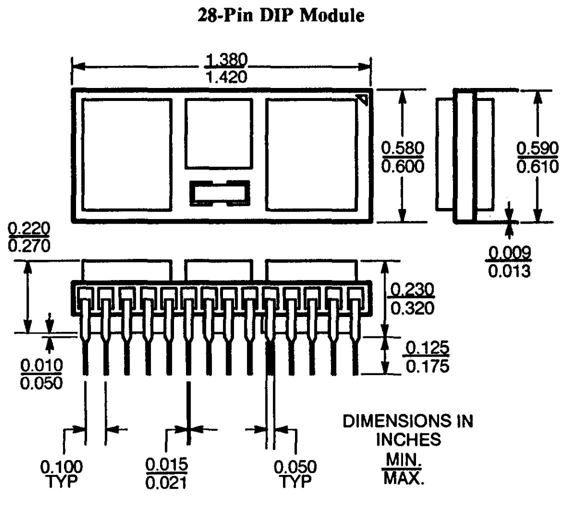
In the depth expansion configuration the ($\overline{XO}$) pin provides the expansion out information that is used to tell the next FIFO that it will be activated.

Logic Block Diagram



4210-1

Package Diagram



4210-2

Document #: 38-M-00032

CYPRESS SEMICONDUCTOR

Cascadeable 16K x 9 FIFO

Features

- **16K x 9 FIFO buffer memory**
- **Asynchronous read/write**
- **High-speed 20-MHz read/write**
- **Pin-compatible with 7C42X series of monolithic FIFOs**
- **Low operating power**
  - **— I_{CC} (max.) = 400 mA**
- **600-mil DIP package**
- **Empty and full flags**
- **Small PCB footprint**
  - **— 0.84 sq. in.**
- **Expandable in depth and width**

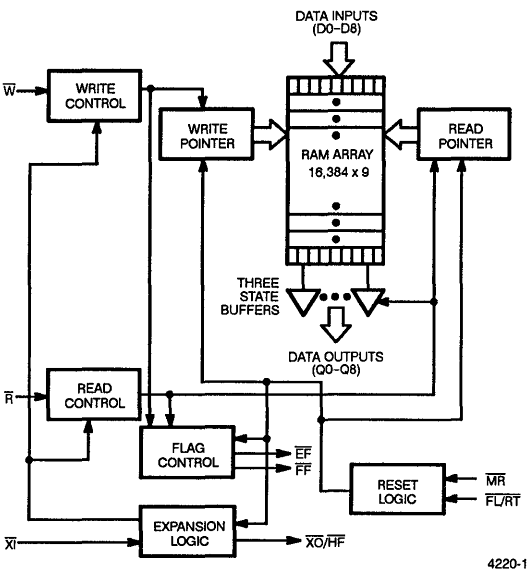
Functional Description

The CYM4220 is a first-in first-out (FIFO) memory module that is 16,384 words by 9 bits wide. It is offered in a 600-mil-wide DIP package. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and Empty flags are provided to prevent over-run and under-run. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel, thus eliminating the serial addition of propagation delays so that throughput is not reduced. Data is steered in a similar manner.

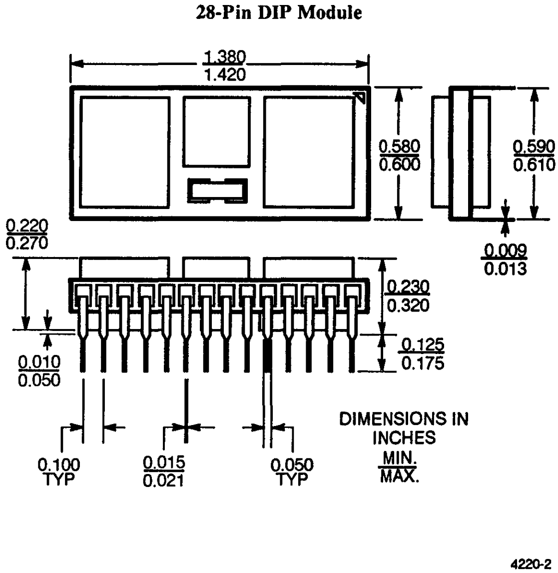
The read and write operations may be asynchronous; each can occur at a rate of 20 MHz. The write operation occurs when the Write ($\overline{W}$) signal is LOW. Read occurs when Read ($\overline{R}$) goes LOW. The 9 data outputs go to the high-impedance state when $\overline{R}$ is HIGH.

A Half-Full ($\overline{HF}$) output flag is provided that is valid in the standalone and width expansion configurations. In the depth expansion configuration the ($\overline{XO}$) pin provides the expansion out information which is used to tell the next FIFO that it will be activated.

Logic Block Diagram



Package Diagram



8

Document #: 38-M-00033

Section Contents

ECL

CYPRESS SEMICONDUCTOR

Combinatorial ECL 16P8 Programmable Logic Device

Features

- **Standard 16P8 pinout and architecture**
  - **16 inputs, 8 outputs**
  - **User-programmable output polarity**
- **Ultra high speed/standard power**
  - **t_{PD} = 3.5 ns (max.)**
  - **I_{EE} = 240 mA (max.)**
- **Low power version**
  - **t_{PD} = 6 ns (max.)**
  - **I_{EE} = 170 mA (max.)**
- **Both 10KH and 100K compatible I/O versions available**
- **Enhanced test features**
  - **Additional test input terms**
  - **Additional test product terms**
- **Security fuse**

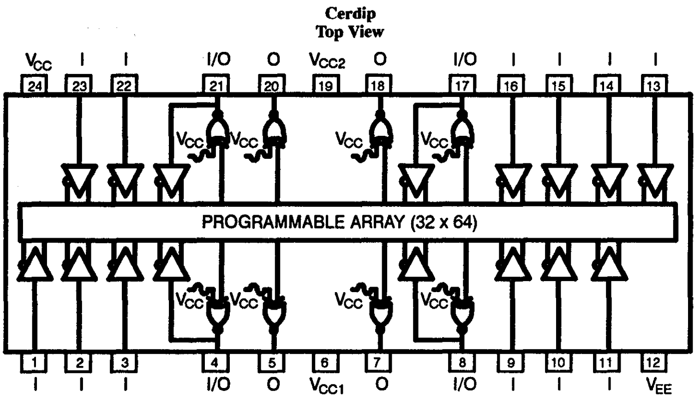
Functional Description

Cypress Semiconductor's PLD family offers the user the highest level of performance in ECL Programmable Logic Devices. These PLDs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor, using Aspen's advanced STAR™ Bipolar process incorporating proven Ti-W fuses.

The CY10E301 is 10KH-compatible and the CY100E301 is 100K-compatible. These PLDs implement the familiar sum-of-products logic functions by selectively programming cell elements to configure the AND gates by disconnecting either the true or complement input term. If all inputs are disconnected from an AND gate, then a logical true will exist at the output of this AND gate. An output polarity fuse is also provided to allow an active LOW to occur if this fuse is blown. A security feature provides the user protection for the implementation of proprietary logic. When invoked by blowing the security fuse, the contents of the array cannot be accessed in the verify mode.

The CY10E301 and CY100E301 can be programmed using Cypress's QuickPro or other industry-standard programming equipment. Programming support information can be obtained from local Cypress sales offices.

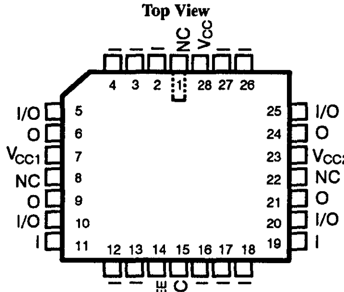
Logic Block Diagram



C301-1

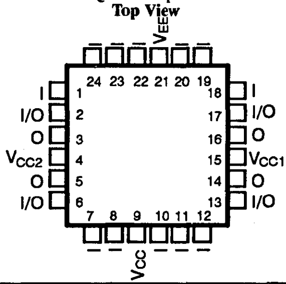
Pin Configurations

PLCC/CLCC
Top View



C301-2

Quad Cerpack
Top View



C301-3

Selection Guide

		10E301-3.5 100E301-3.5	10E301-4 100E301-4	10E301-5	10E301L-6 100E301L-6
Maximum Input to Output Propagation Delay (ns)		3.5	4	5	6
I_{EE} (mA)	Commercial	-240	-240		-170
	Military			-240	

Shaded area contains preliminary information.
STAR is a trademark of Aspen Semiconductor.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied [1] .... –55°C to +125°C

Supply Voltage V_{EE} to V_{CC} .... –7.0 V to +0.5V

Input Voltage .... V_{EE} to +0.5V

Output Current.................................. –50 mA

Operating Range Referenced to V_{CC} at Ground

Range	I/O	Temperature	V_{EE}
Commercial (Standard, "L")	10KH	0°C to +75°C Ambient	–5.2V ± 5%
Commercial (Standard, "L")	100K	0°C to +85°C Ambient	–4.5V ± 0.3V
Military	10KH	–55°C to +125°C Case	–5.2V ± 5%

Electrical Characteristics Over Operating Range [2]

Parameters	Description	Test Conditions	Temperature [1]	10E301 Min.	10E301 Max.	100E301 Min.	100E301 Max.	Units
V_{OH}	Output HIGH Voltage	10KH, R_L = 50 Ω to -2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_C = –55°C	–1140	–920			mV
			T_A = 0°C	–1020	–840			mV
			T_A = +25°C	–980	–810			mV
			T_A = +75°C	–920	–735			mV
			T_C = +125°C	–900	–700			mV
		100K, R_L = 50 Ω to -2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to +85°C			–1025	–880	mV
V_{OL}	Output LOW Voltage	10KH, R_L = 50 Ω to -2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_C = –55°C	–1950	–1650			mV
			T_A = 0°C	–1950	–1630			mV
			T_A = +25°C	–1950	–1630			mV
			T_A = +75°C	–1950	–1600			mV
			T_C = +125°C	–1950	–1590			mV
		100K, R_L = 50 Ω to -2V V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to +85°C			–1810	–1620	mV
V_{IH}	Input HIGH Voltage	10KH	T_C = –55°C	–1270	–920			mV
			T_A = 0°C	–1170	–840			mV
			T_A = +25°C	–1130	–810			mV
			T_A = +75°C	–1070	–735			mV
			T_C = +125°C	–1050	–700			mV
		100K	T_A = 0°C to +85°C			–1165	–880	mV
V_{IL}	Input LOW Voltage	10KH	T_C = –55°C	–1950	–1520			mV
			T_A = 0°C	–1950	–1480			mV
			T_A = +25°C	–1950	–1480			mV
			T_A = +75°C	–1950	–1450			mV
			T_C = +125°C	–1950	–1440			mV
		100K	T_A = 0°C to +85°C			–1810	–1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220		220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min. (Except I/O pins)		0.5		0.5		µA
I_{EE}	Supply Current (All inputs and outputs open)	Commercial "L" (Low Power)			–170		–170	mA
		Commercial (Standard Power)			–240		–240	mA
		Military			–240			mA

Notes:
1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
2. See AC Test Loads and Waveforms for test conditions.

Capacitance[3]

Parameters	Description	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance		4	8	pF
C_{OUT}	Output Capacitance		6	10	pF

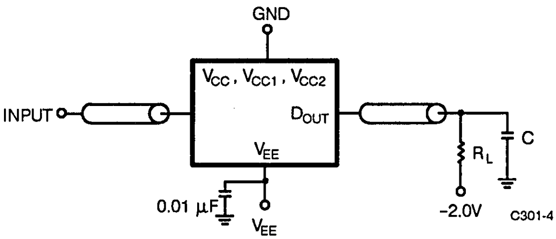
Note:
3. Tested initially and after any design or process changes that may affect these parameters.

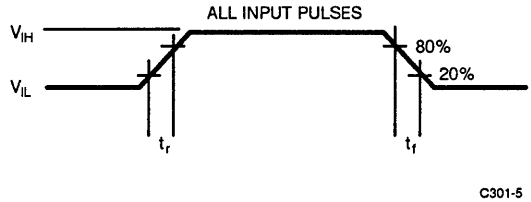
Switching Characteristics Over Operating Range[2]

Parameters	Description	10E301-3.5 100E301-3.5		10E301-4 100E301-4		10E301-5		10E301L-6 100E301L-6		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay		3.5		4.0		5.0		6.0	ns
t_r	Output Rise Time	0.35	1.5	0.35	1.5	0..35	1.5	0.35	1.5	ns
t_f	Output Fall Time	0.35	1.5	0.35	1.5	0.35	1.5	0.35	1.5	ns

Shaded areas contain preliminary information.

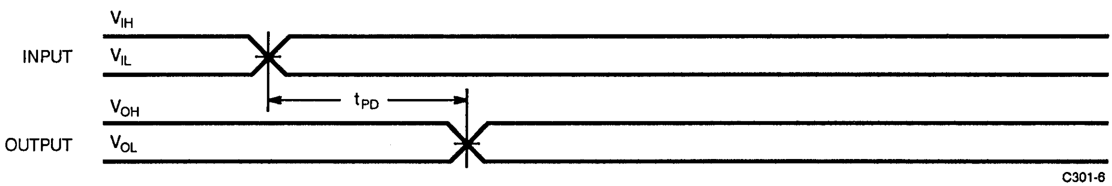
AC Test Loads and Waveforms [4, 5, 6, 7, 8, 9]





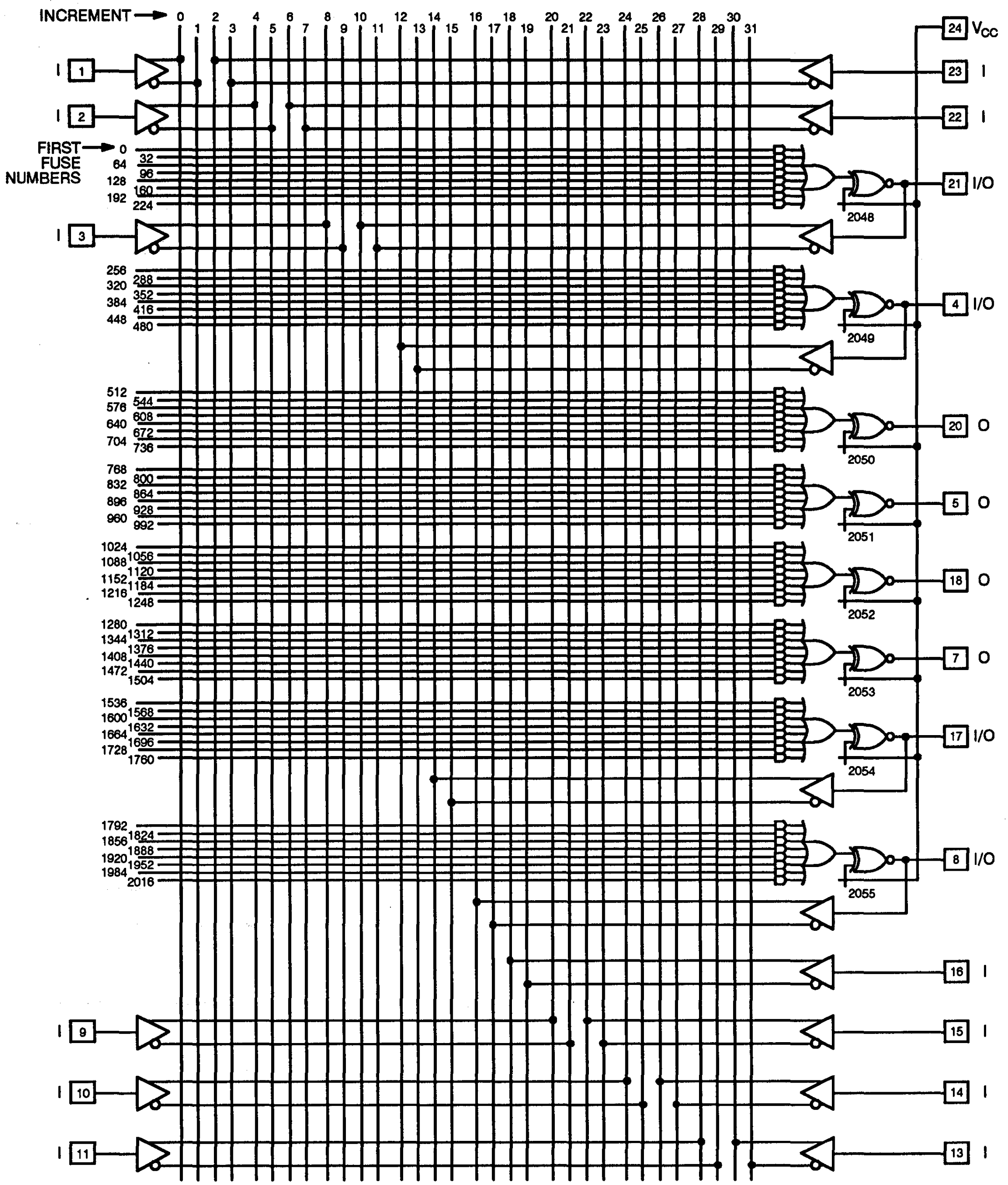
Notes:
4. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10KH version.
5. V_{IL} = −1.7V, V_{IH} = −0.9V on 100K version.
6. R^L = 50Ω, C < 5 pF (includes fixture and stray capacitance).
7. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
8. t_r = t_f = 0.7 ns.
9. All timing measurements are made from the 50% point of all waveforms.

Switching Waveforms



9

Functional Logic Diagram (DIP Pinout)



JEDEC fuse number = first fuse number + increment

Ordering Information

I/O	t_{PD} (ns)	I_{EE} (mA)	Ordering Code	Package Type	Operating Range
10KH	3.5	240	CY10E301-3.5DC	D14	Commercial
			CY10E301-3.5KC	K63	
			CY10E301-3.5YC	Y64	
	4	240	CY10E301-4DC	D14	Commercial
			CY10E301-4KC	K63	
			CY10E301-4YC	Y64	
	5	240	CY10E301-5DMB	D14	Military
			CY10E301-5YMB	Y64	
	6	170	CY10E301L-6PC	P13A	Commercial
			CY10E301L-6JC	J64	
100K	3.5	240	CY100E301-3.5DC	D14	Commercial
			CY100E301-3.5KC	K63	
			CY100E301-3.5YC	Y64	
	4	240	CY100E301-4DC	D14	Commercial
			CY100E301-4KC	K63	
			CY100E301-4YC	Y64	
	6	170	CY100E301L-6PC	P13A	Commercial
			CY100E301L-6JC	J64	

Shaded areas contain preliminary information.
Document #: 38-A-00011A

CY10E302
CY100E302

Combinatorial ECL 16P4 Programmable Logic Device

CYPRESS SEMICONDUCTOR

Features

- **Standard 16P4 pinout and architecture**
  - **16 inputs, 4 outputs**
  - **User-programmable output polarity**
- **Ultra high speed/standard power**
  - **t_{PD} = 3 ns (max.)**
  - **I_{EE} = 220 mA (max.)**
- **Low-power version**
  - **t_{PD} = 4 ns (max.)**
  - **I_{EE} = 170 mA (max.)**
- **Both 10KH and 100K compatible I/O versions available**
- **Enhanced test features**
  - **Additional test input terms**
  - **Additional test product terms**
- **Security fuse**

Functional Description

Cypress Semiconductor's PLD family offers the user the highest level of performance in ECL Programmable Logic Devices. These PLDs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor, using an advanced process incorporating proven Ti-W fuses.

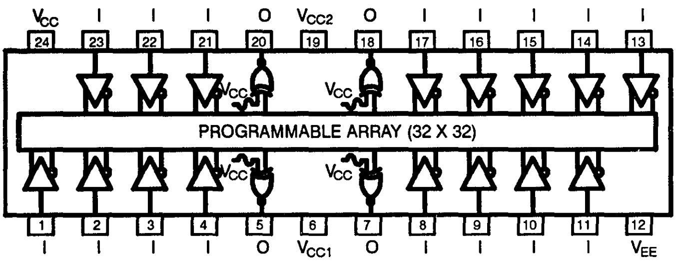
The CY10E302 is 10KH-compatible and the CY100E302 is 100K-compatible. These PLDs implement the familiar sum-of-products logic functions by selectively programming cell elements to configure the AND gates by disconnecting either the true or complement input term. If all inputs are disconnected from an AND gate, then a logical true will exist at the output of this AND gate. An output polarity fuse is also provided to allow an active LOW to occur if this fuse is blown.

A security feature provides the user protection for the implementation of proprietary logic. When invoked by blowing the security fuse, the contents of the array cannot be accessed in the verify mode.

The CY10E302 and CY100E302 can be programmed using Cypress's QuickPro or other industry-standard programming equipment. Programming support information can be obtained from local Cypress Semiconductor sales offices.

Logic Block Diagram

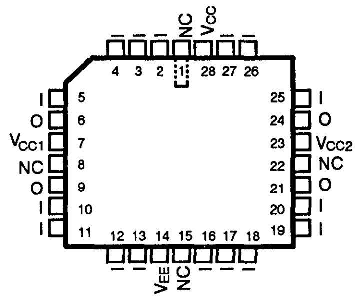
Cerdip
Top View



C302-1

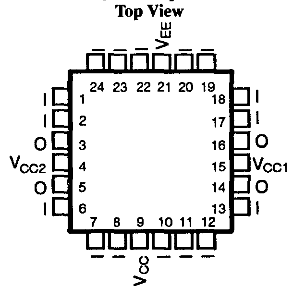
Pin Configurations

PLCC/CLCC
Top View



C302-2

Quad Cerpack
Top View



C302-3

Selection Guide

		10E302-3 100E302-3	10E302-4 100E302-4	10E302-4	10E302L-4 100E302L-4
Maximum Input to Output Propagation Delay (ns)		3	4	4	4
I_{EE} (mA)	Commercial	–220	–220		–170
	Military			–220	

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied [1] .... –55°C to +125°C

Supply Voltage V_{EE} to V_{CC} .... –7.0 V to +0.5V

Input Voltage .... V_{EE} to +0.5V

Output Current.................................. –50 mA

Operating Range Referenced to V_{CC} at Ground

Range	I/O	Temperature	V_{EE}
Commercial (Standard, "L")	10KH	0°C to +75°C Ambient	–5.2V + 5%
Commercial (Standard, "L")	100K	0°C to +85°C Ambient	–4.5V + 0.3V
Military	10KH	–55°C to+125°C Case	–5.2V + 5%

Electrical Characteristics Over the Operating Range [2]

Parameters	Description	Test Conditions	Temperature [1]	10E302 Min.	10E302 Max.	100E302 Min.	100E302 Max.	Units
V_{OH}	Output HIGH Voltage	10KH, R_L = 50 Ω to –2V, V_{IN} = V_{IH} Min. or V_{IL} Max.	T_C = –55°C	–1140	–920			mV
			T_A = 0°C	–1020	–840			mV
			T_A = +25°C	–980	–810			mV
			T_A = +75°C	–920	–735			mV
			T_C = +125°C	–900	–700			mV
		100K, R_L = 50 Ω to –2V, V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to 85°C			–1025	–880	mV
V_{OL}	Output LOW Voltage	10KH, R_L = 50 Ω to –2V, V_{IN} = V_{IH} Min. or V_{IL} Max.	T_C = –55°C	–1950	–1650			mV
			T_A = 0°C	–1950	–1630			mV
			T_A = +25°C	–1950	–1630			mV
			T_A = +75°C	–1950	–1600			mV
			T_C = +125°C	–1950	–1590			mV
		100K, R_L = 50 Ω to –2V, V_{IN} = V_{IH} Min. or V_{IL} Max.	T_A = 0°C to 85°C			–1810	–1620	mV
V_{IH}	Input HIGH Voltage	10KH	T_C = –55°C	–1270	–920			mV
			T_A = 0°C	–1170	–840			mV
			T_A = +25°C	–1130	–810			mV
			T_A = +75°C	–1070	–735			mV
			T_C = +125°C	–1050	–700			mV
		100K	T_A = 0°C to 85°C			–1165	–880	mV
V_{IL}	Input LOW Voltage	10KH	T_C = –55°C	–1950	–1520			mV
			T_A = 0°C	–1950	–1480			mV
			T_A = +25°C	–1950	–1480			mV
			T_A = +75°C	–1950	–1450			mV
			T_C = +125°C	–1950	–1440			mV
		100K	T_A = 0°C to 85°C			–1810	–1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220		220	mA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.		0.5		0.5		mA
I_{EE}	Supply Current (All inputs and outputs open)	Commercial "L" (Low Power)			–170		–170	mA
		Commercial (Standard Power)			–220		–220	mA
		Military			–220			mA

Notes:
1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
2. See AC Test Loads and Waveforms for test conditions.

9

Capacitance[3]

Parameters	Description	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance		4	8	pF
C_{OUT}	Output Capacitance		6	10	pF

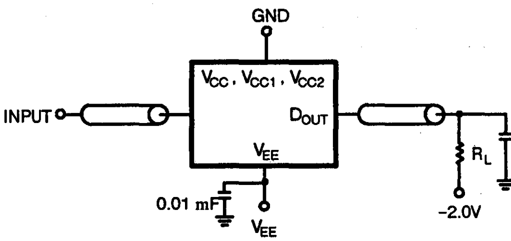
Note:

3. Tested initially and after any design or process changes that may affect these parameters.

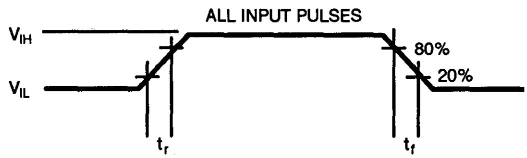
Switching Characteristics Over the Operating Range [2]

Parameters	Description	10E302-3 100E302-3		10E302-4 100E302-4		10E302L-4 100E302L-4		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay		3.0		4.0		4.0	ns
t_r	Output Rise Time	0.35	1.5	0.35	1.5	0.35	1.5	ns
t_f	Output Fall Time	0.35	1.5	0.35	1.5	0.35	1.5	ns

AC Test Loads and Waveforms [4, 5, 6, 7, 8, 9]



C302-4

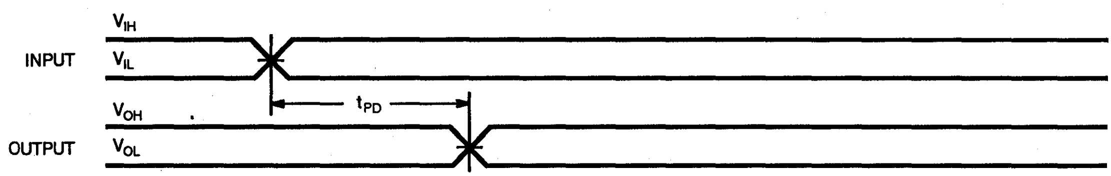


C302-5

Notes:

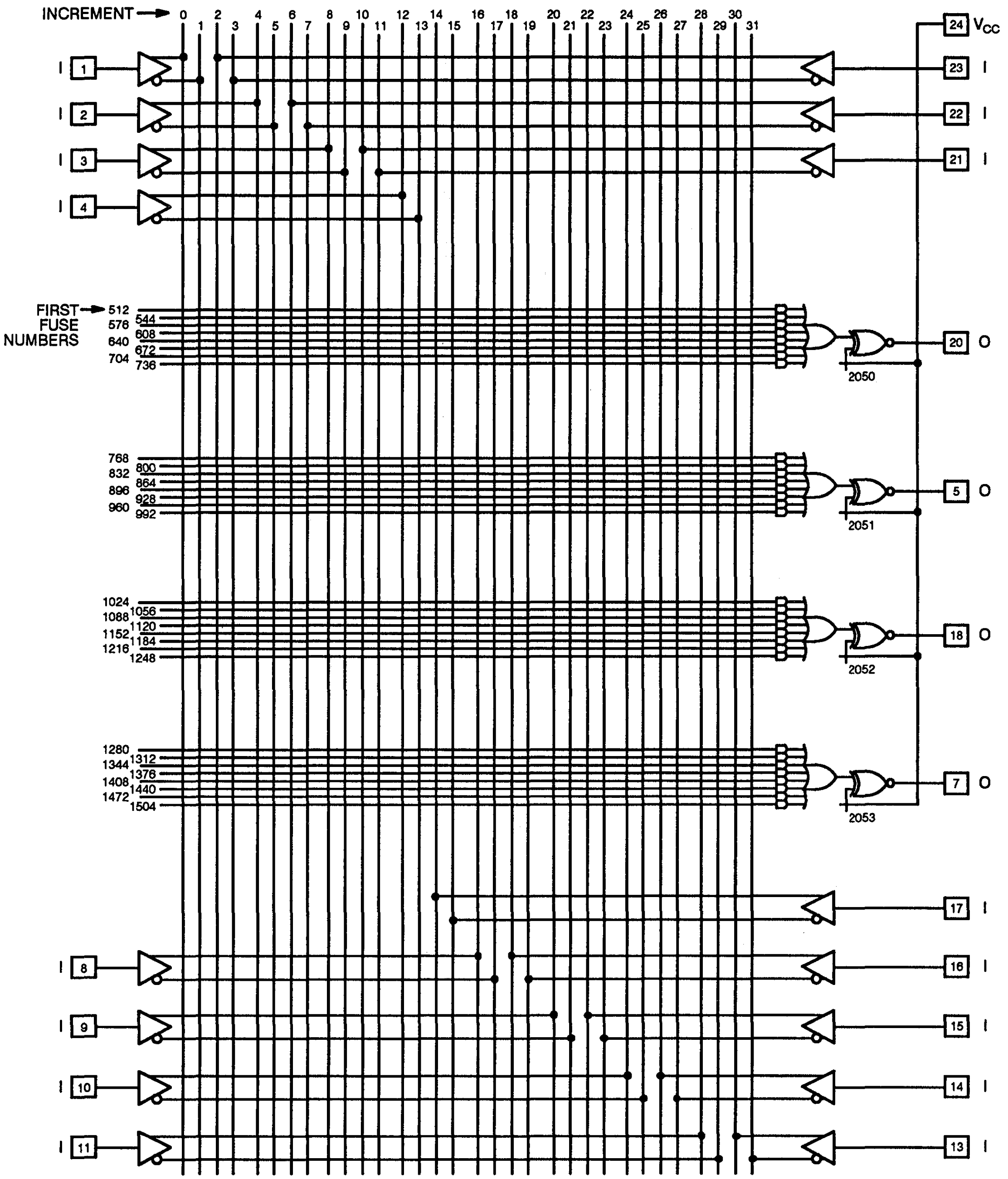
4. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10KH version.
5. V_{IL} = −1.7V, V_{IH} = −0.9V on 100K version.
6. R_L = 50 W, C < 5 pF (includes fixture and stray capacitance).
7. All coaxial cables should be 50 W with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
8. $t_r = t_f = 0.7$ ns.
9. All timing measurements are made from the 50% point of all waveforms.

Switching Waveforms



C302-6

Functional Logic Diagram (DIP Pinout)



C302-7

JEDEC fuse number = first fuse number + increment

Ordering Information

I/O	t_{PD} (ns)	I_{EE} (mA)	Ordering Code	Package Type	Operating Range
10KH	3	220	CY10E302-3DC	D14	Commercial
			CY10E302-3KC	K63	
			CY10E302-3YC	Y64	
	4	220	CY10E302-4DC	D14	Commercial
			CY10E302-4KC	K63	
			CY10E302-4YC	Y64	
	4	220	CY10E302-4DMB	D14	Military
			CY10E302-4YMB	Y64	
	4	170	CY10E302L-4PC	P13A	Commercial
			CY10E302L-4JC	J64	
100K	3	220	CY100E302-3DC	D14	Commercial
			CY100E302-3KC	K63	
			CY100E302-3YC	Y64	
	4	220	CY100E302-4DC	D14	Commercial
			CY100E302-4KC	K63	
			CY100E302-4YC	Y64	
	4	170	CY100E302L-4PC	P13A	Commercial
			CY100E302L-4JC	J64	

Document #: 38-A-00012A

CY10E422
CY100E422

CYPRESS SEMICONDUCTOR

256 x 4 ECL Static RAM

Features

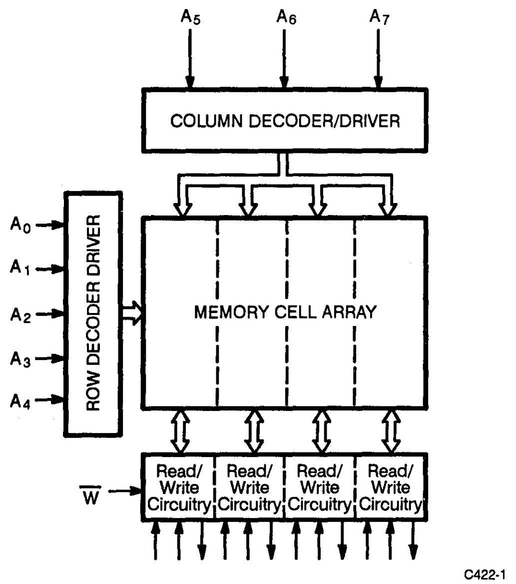
- 256 x 4-bit organization
- Ultra high speed/standard power
  - t_{AA} = 3 ns, t_{ABS} = 2 ns
  - I_{EE} = 220 mA
- Low-power version
  - t_{AA} = 5 ns
  - I_{EE} = 150 mA
- Both 10KH/10K and 100K compatible I/O versions
- 10K/10KH Military version
- On-chip voltage compensation for improved noise margin
- Open emitter output for ease of memory expansion
- Industry-standard pinout

Functional Description

The Cypress CY10E422 and CY100E422 are 256 x 4 ECL RAMs designed for scratch pad, control, and buffer storage applications. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Both parts are fully decoded random access memories organized as 256 words by 4 bits. The CY10E422 is 10KH-/10K-compatible and is available in a Military version. The CY100E422 is 100K-compatible.

The four independent active LOW block select ($\overline{B}$) inputs control memory selection and allow for memory expansion and reconfiguration. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{B}_X$ LOW, the corresponding data at D_X is written into the addressed location. To read, $\overline{W}$ is held HIGH, while $\overline{B}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand or reconfigure the memory.

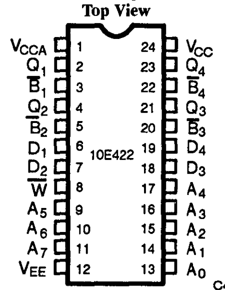
Logic Block Diagram



C422-1

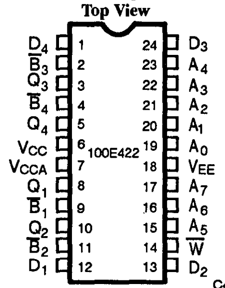
Pin Configurations (cont. p6)

Cerdip
Top View



C422-2

Cerdip
Top View



C422-3

9

Selection Guide

		10E422-3 100E422-3	10E422-5 100E422-5	10E422-7 100E422-7
Maximum Access Time (ns)		3	5	7
I_{EE} Max. (mA)	Commercial	220	220	
	"L" (Low Power)		150	150
	Military (10KH/10K only)		150	150

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature .... -65°C to +150°C

Ambient Temperature with Power Applied .... -55°C to +125°C

Supply Voltage V_{EE} to V_{CC} .... -7.0 to +0.5V

Input Voltage .... V_{EE} to +0.5V

Output Current .... -50 mA

Operating Range Referenced to V_{CC}

Range	I/O	Ambient Temperature	V_{EE}
Commercial (Standard, "L")	10KH/10K	0°C to 75°C	-5.2V ± 5%
Commercial (Standard, "L")	100K	0°C to 85°C	-4.5V ± 0.3V
Military ("L")	10KH/10K	-55°C to +125°C Case	-5.2V ± 5%

Electrical Characteristics

Parameters	Description	Test Conditions	Temperature [1]	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	10E[2] R_L = 50 Ω to -2V, V_{EE} = -5.2V, V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = -55°C	-1140	-900	mV
			T_A = 0°C	-1000	-840	mV
			T_A = +25°C	-960	-810	mV
			T_A = +75°C	-900	-735	mV
			T_C = +125°C	-880	-700	mV
		100K R_L = 50 Ω to -2V, V_{EE} = -4.5V, V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	-1025	-880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50 Ω to -2V, V_{EE} = -5.2V, V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = -55°C	-1920	-1670	mV
			T_A = 0°C	-1870	-1665	mV
			T_A = +25°C	-1850	-1650	mV
			T_A = +75°C	-1830	-1625	mV
			T_C = +125°C	-1830	-1610	mV
		100K R_L = 50 Ω to -2V, V_{EE} = -4.5V, V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	-1810	-1620	mV
V_{IH}	Input HIGH Voltage	10E V_{EE} = -5.2V	T_C = -55°C	-1260	-900	mV
			T_A = 0°C	-1170	-840	mV
			T_A = +25°C	-1130	-810	mV
			T_A = +75°C	-1070	-720	mV
			T_C = +125°C	-1030	-700	mV
		100K V_{EE} = -4.5V	T_A = 0°C to 85°C	-1165	-880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = -5.2V	T_C = -55°C	-1950	-1540	mV
			T_A = 0°C	-1950	-1480	mV
			T_A = +25°C	-1950	-1475	mV
			T_A = +75°C	-1950	-1450	mV
			T_C = +125°C	-1950	-1450	mV
		100K V_{EE} = -4.5V	T_A = 0°C to 85°C	-1810	-1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{B}$ inputs	0.5	170	µA
			All other inputs	-50		µA
I_{EE}	Supply Current (All inputs and outputs open)	Commercial/Military "L" (Low Power)		-150		mA
		Commercial (Standard)		-220		mA

Notes:

1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as cas temperature.
2. 10E specifications support both 10K and 10KH compatibility.

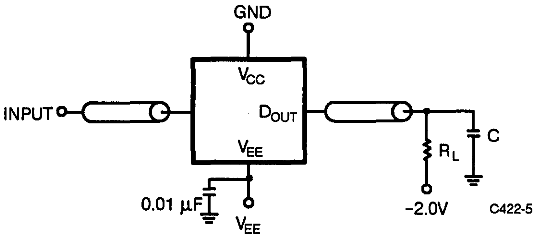
Capacitance[3]

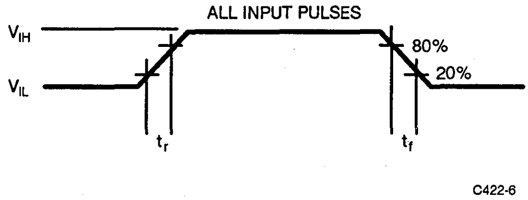
Parameters	Description	Min.	Typ.	Max.[4]	Units
C_{IN}	Input Capacitance		4	5	pF
C_{OUT}	Output Capacitance		5	6	pF

Notes:

3. Tested initially and after any design or process changes that may affect these parameters.
4. For all packages except Cerdip (D40), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.

AC Test Loads and Waveforms [5, 6, 7, 8, 9, 10]





Notes:

5. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10E version.
6. V_{IL} = -1.7V, V_{IH} = -0.9V on 100K version.
7. R_L = 50Ω, C < 5 pF (3 ns grade) or < 30 pF (5, 7 ns grade) (includes fixture and stray capacitance).
8. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
9. $t_r = t_f$ = 0.7 ns.
10. All timing measurements are made from the 50% point of all waveforms.

9

Switching Characteristics Over the Commercial Operating Range

Parameters	Description	10E422-3 100E422-3		10E422-5 100E422-5		10E422-7 100E422-7		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{ABS}	Block Select to Output delay		2.5	0.5	3.0	0.5	4.0	ns
t_{RBS}	Block Select Recovery		2.5	0.5	3.0	0.5	4.0	ns
t_{AA}	Address Access Time		3.0	1.2	5.0	1.2	7.0	ns
t_W	Write Pulse Width	3.0		3.5		5.0		ns
t_{WSD}	Data Set-Up to Write	0		0.5		1.0		ns
t_{WHD}	Data Hold to Write	1.0		1.0		1.0		ns
t_{WSA}	Address Set-Up/Write	1.0		0.5		1.0		ns
t_{WHA}	Address Hold/Write	1.0		1.0		1.0		ns
t_{WSBS}	Block Select Set-Up/Write	0		0.5		1.0		ns
t_{WHBS}	Block Select Hold/Write	1.0		1.0		1.0		ns
t_{WS}	Write Disable		2.5	0.3	3.5	0.3	4.0	ns
t_{WR}	Write Recovery		3.5	0.5	3.5	0.5	8.0	ns
t_r	Output Rise Time	0.35	1.5	0.35	2.5	1.0	2.5	ns
t_f	Output Fall Time	0.35	1.5	0.35	2.5	1.0	2.5	ns

Shaded area contains preliminary information.

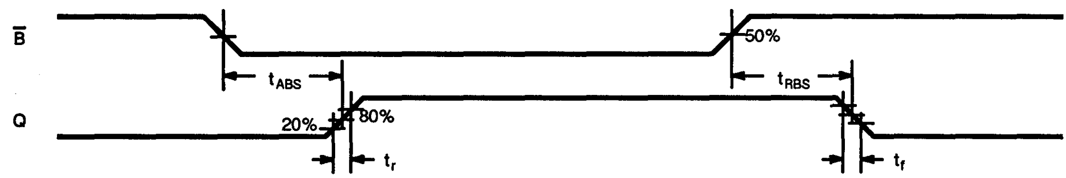
Switching Characteristics Over the Military Operating Range

Parameters	Description	10E422-5		10E422-7		Units
		Min.	Max.	Min.	Max.	
t_{ABS}	Block Select to Output delay	0.5	4.0	0.5	4.0	ns
t_{RBS}	Block Select Recovery	0.5	4.0	0.5	4.0	ns
t_{AA}	Address Access Time	1.2	5.0	1.2	7.0	ns
t_W	Write Pulse Width	5.0		5.0		ns
t_{WSD}	Data Set-Up to Write	0.0		1.0		ns
t_{WHD}	Data Hold to Write	1.0		1.0		ns
t_{WSA}	Address Set-Up/Write	1.0		1.0		ns
t_{WHA}	Address Hold/Write	1.0		1.0		ns
t_{WSBS}	Block Select Set-Up/Write	0.0		1.0		ns
t_{WHBS}	Block Select Hold/Write	1.0		1.0		ns
t_{WS}	Write Disable	0.3	4.0	0.3	4.0	ns
t_{WR}	Write Recovery	0.5	5.0	0.5	8.0	ns
t_r	Output Rise Time	1.0	2.5	1.0	2.5	ns
t_f	Output Fall Time	1.0	2.5	1.0	2.5	ns

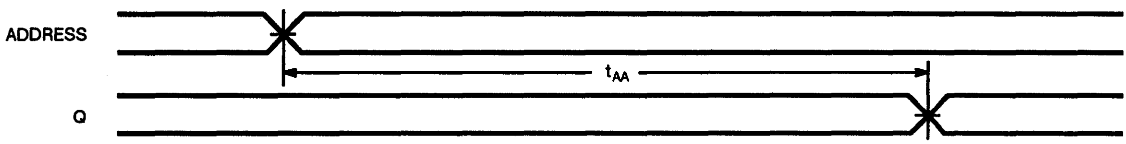
Shaded area contains preliminary information.

Switching Waveforms

Read Mode

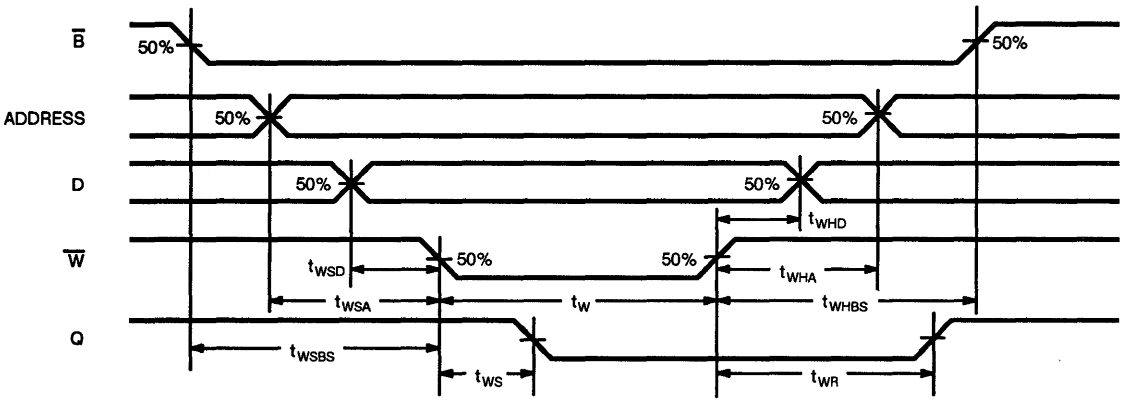


C422-7



C422-8

Write Mode

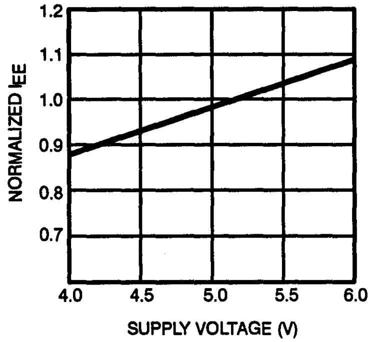


C422-9

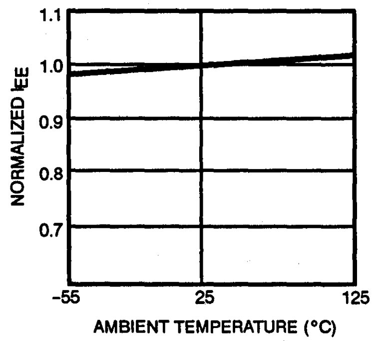
9

Typical DC and AC Characteristics (10E422/10E422L/100E422/100E422L)

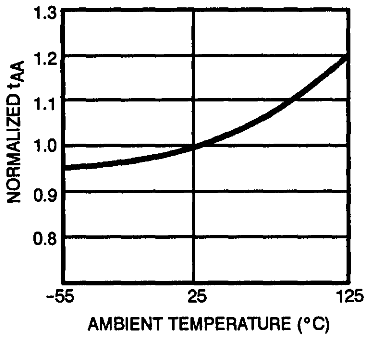
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



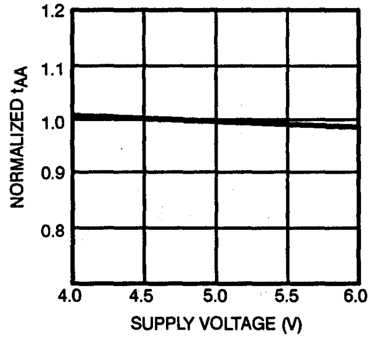
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



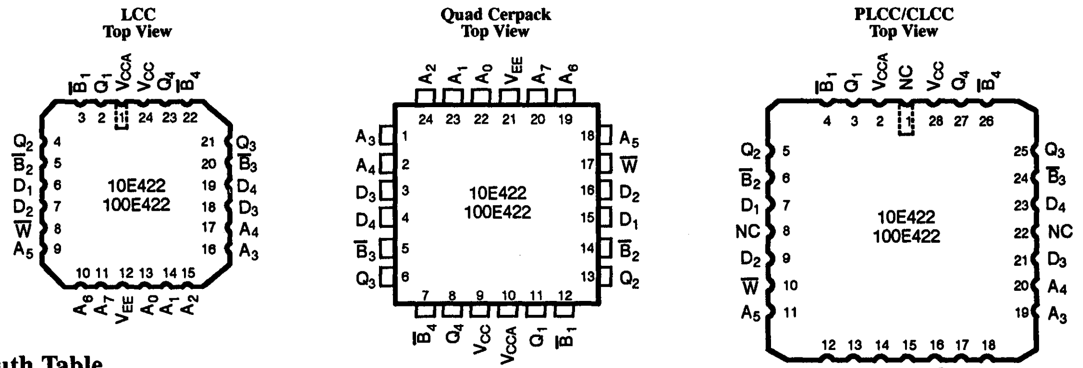
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



Pin Configurations



Truth Table

Inputs			Outputs	
$\overline{B}_x$	$\overline{W}$	D_x	Q_x	Mode
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	Out	Read

Ordering Information

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Type	Operating Range
10E[11]	220	3	CY10E422-3LC	L63	Commercial
			CY10E422-3KC	K63	
			CY10E422-5YC	Y64	
		5	CY10E422-5YC	Y64	
			CY10E422-5LC	L63	
			CY10E422-5DC	D40	
			CY10E422-5KC	K63	
	150	5	CY10E422L-5LC	L63	Commercial
			CY10E422L-5DC	D40	
			CY10E422L-5KC	K63	
			CY10E422L-5JC	J64	
			CY10E422L-5DMB	D40	Military
			CY10E422L-5KMB	K63	
			CY10E422L-5YMB	Y64	
		7	CY10E422L-7JC	J64	Commercial
			CY10E422L-7KC	K63	
			CY10E422L-7LC	L63	
			CY10E422L-7DC	D40	
			CY10E422L-7DMB	D40	Military
			CY10E422L-7KMB	K63	
			CY10E422L-7YMB	Y64	
100K	220	3	CY100E422-3LC	L63	Commercial
			CY100E422-3KC	K63	
			CY100E422-3YC	Y64	
		5	CY100E422-5YC	Y64	
			CY100E422-5LC	L63	
			CY100E422-5DC	D40	
			CY100E422-5KC	K63	
	150	5	CY100E422L-5LC	L63	Commercial
			CY100E422L-5DC	D40	
			CY100E422L-5KC	K63	
			CY100E422L-5JC	J64	
		7	CY100E422L-7JC	J64	
			CY100E422L-7KC	K63	
			CY100E422L-7LC	L63	
			CY100E422L-7DC	D40	

Notes:

11. 10E specifications support both 10K and 10KH compatibility.

Shaded area contains preliminary information.

Document #: 38-A-00002A

CY10E474
CY100E474

CYPRESS SEMICONDUCTOR

1024 x 4 ECL Static RAM

Features

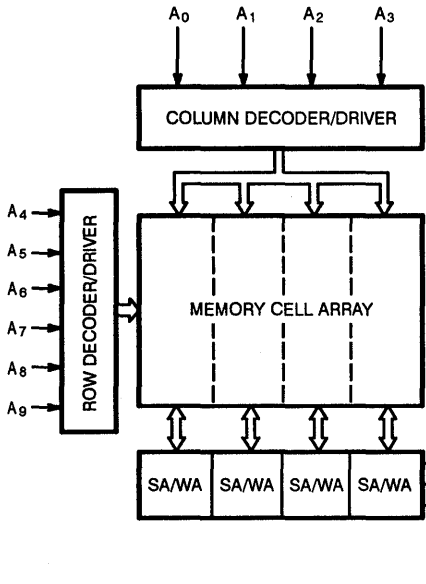
- **1024 x 4-bit organization**
- **Ultra high speed/standard power**
  - **— t_{AA} = 3 ns, t_{ACS} = 2 ns**
  - **— I_{EE} = 275 mA**
- **Low-power version**
  - **— t_{AA} = 5 ns**
  - **— I_{EE} = 190 mA**
- **Both 10KH/10K and 100K compatible I/O versions**
- **10K/10KH Military version**
- **On-chip voltage compensation for improved noise margin**
- **Open emitter output for ease of memory expansion**
- **Industry-standard pinout**

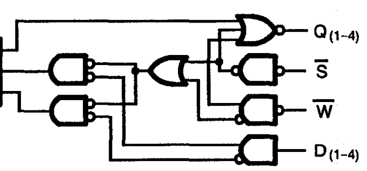
Functional Description

The Cypress CY10E474 and CY100E474 are 1K x 4 ECL RAMs designed for scratch pad, control, and buffer storage applications. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Both parts are fully decoded random access memories organized as 1024 words by 4 bits. The CY10E474 is 10KH-/10K-compatible and is available in a Military version. The CY100E474 is 100K-compatible.

The active LOW chip select ($\overline{S}$) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ LOW, the data at $D_{(1-4)}$ is written into the addressed location. To read, $\overline{W}$ is held HIGH, while $\overline{S}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory.

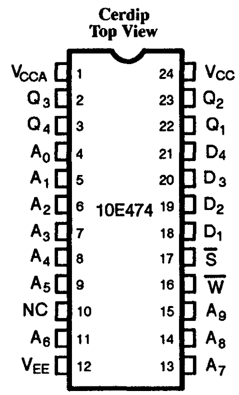
Logic Block Diagram



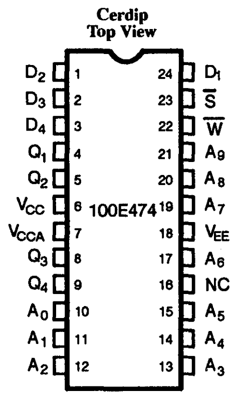


C474-1

Pin Configurations



C474-2



C474-3

Selection Guide

		10E474-3 100E474-3	10E474-5 100E474-5	10E474-7 100E474-7
Maximum Access Time (ns)		3	5	7
I_{EE} Max. (mA)	Commercial	275	275	
	"L"		190	190
	Military (10K/10KH only)		190	190

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature .... -65°C to +150°C

Ambient Temperature with Power Applied .... -55°C to +125°C

Supply Voltage V_{EE} to V_{CC} .... -7.0 to +0.5V

Input Voltage .... V_{EE} to +0.5V

Output Current .... -50 mA

Operating Range Referenced to V_{CC}

Range	I/O	Ambient Temperature	V_{EE}
Commercial (Standard, "L")	10KH/10K	0°C to 75°C	-5.2V ± 5%
Commercial (Standard, "L")	100K	0°C to 85°C	-4.5V ± 0.3V
Military ("L")	10KH/10K	-55°C to +125°C Case	-5.2V ± 5%

Electrical Characteristics

Parameters	Description	Test Conditions	Temperature [1]	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	10E[2] R_L = 50 Ω to -2V V_{EE}= -5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = -55°C	-1140	-900	mV
			T_A = 0°C	-1000	-840	mV
			T_A = +25°C	-960	-810	mV
			T_A = +75°C	-900	-735	mV
			T_C = +125°C	-880	-700	mV
		100K R_L = 50 Ω to -2V V_{EE} = -4.5V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	-1025	-880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50 Ω to -2V V_{EE}= -5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_C = -55°C	-1920	-1670	mV
			T_A = 0°C	-1870	-1665	mV
			T_A = +25°C	-1850	-1650	mV
			T_A = +75°C	-1830	-1625	mV
			T_C = +125°C	-1830	-1610	mV
		100K R_L = 50 Ω to -2V V_{EE} = -4.5V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	-1810	-1620	mV
V_{IH}	Input HIGH Voltage	10E V_{EE} = -5.2V	T_C = -55°C	-1260	-900	mV
			T_A = 0°C	-1170	-840	mV
			T_A = +25°C	-1130	-810	mV
			T_A = +75°C	-1070	-720	mV
			T_C = +125°C	-1030	-700	mV
		100K V_{EE} = -4.5V	T_A = 0°C to 85°C	-1165	-880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = -5.2V	T_C = -55°C	-1950	-1540	mV
			T_A = 0°C	-1950	-1480	mV
			T_A = +25°C	-1950	-1475	mV
			T_A = +75°C	-1950	-1450	mV
			T_C = +125°C	-1950	-1450	mV
		100K V_{EE} = -4.5V	T_A = 0°C to 85°C	-1810	-1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{S}$ inputs	0.5	170	µA
			All other inputs	-50		µA
I_{EE}	Supply Current (All inputs and outputs open)	Commercial/Military Standard "L" (Low Power)		-190		mA
		Commercial (Standard)		-275		mA

Notes:

1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
2. 10E specifications support both 10K and 10KH compatibility.

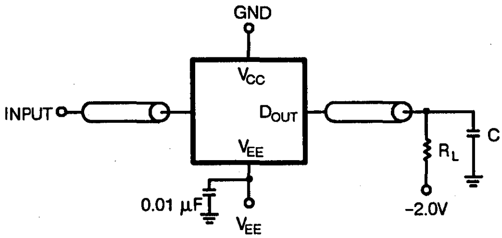
Capacitance[3]

Parameters	Description	Typ.	Max.[4]	Units
C_{IN}	Input Pin Capacitance	4	5	pF
C_{OUT}	Output Pin Capacitance	5	6	pF

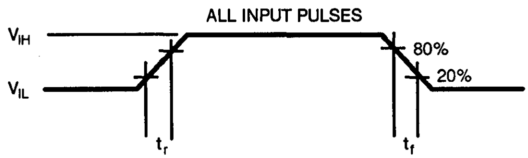
Notes:

3. Tested initially and after any design or process changes that may affect these parameters.
4. For all packages except Cerdip (D40) which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.

AC Test Loads and Waveforms [5, 6, 7, 8, 9, 10]



C474-4



C474-5

Notes:

5. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10E version.
6. V_{IL} = -1.7V, V_{IH} = -0.9V on 100K version.
7. R_L = 50Ω, C < 5 pF (3 ns grade) or < 30 pF (5, 7 ns grade) (includes fixture and stray capacitance).
8. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
9. t_r = t_f = 0.7 ns.
10. All timing measurements are made from the 50% point of all waveforms.

Switching Characteristics Over the Commercial Operating Range

Parameters	Description	10E474-3 100E474-3 Min.	10E474-3 100E474-3 Max.	10E474-5 100E474-5 Min.	10E474-5 100E474-5 Max.	10E474-7 100E474-7 Min.	10E474-7 100E474-7 Max.	Units
t_{AC}	Input to Output delay		2.5	0.5	3.0	0.5	5.0	ns
t_{RC}	Chip Select Recovery		2.5	0.5	3.0	0.5	5.0	ns
t_{AA}	Address Access Time		3.0	1.2	5.0	1.2	7.0	ns
t_{WW}	Write Pulse Width	3.0		5.0		5.0		ns
t_{SD}	Data Set-Up to Write	0		0.0		0.0		ns
t_{HD}	Data Hold to Write	1.0		0.0		1.0		ns
t_{SA}	Address Set-Up/Write	1.0		0.0		1.0		ns
t_{HA}	Address Hold/Write	1.0		0.0		1.0		ns
t_{SC}	Chip Select Set-Up/Write	0		0.0		0.0		ns
t_{HC}	Chip Select Hold/Write	1.0		0.0		1.0		ns
t_{WS}	Write Disable		2.5	0.3	3.0	0.3	6.5	ns
t_{WR}	Write Recovery		3.5	0.5	5.0	0.5	7.0	ns
t_r	Output Rise Time	0.35	1.5	0.35	2.5	1.0	2.5	ns
t_f	Output Fall Time	0.35	1.5	0.35	2.5	1.0	2.5	ns

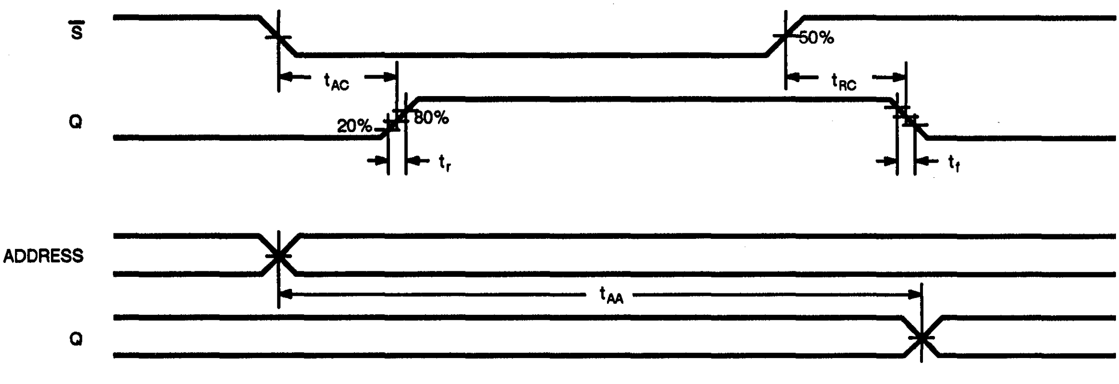
Shaded area contains preliminary information.

Switching Characteristics Over the Military Operating Range

Parameters	Description	10E474-5 Min.	10E474-5 Max.	10E474-7 Min.	10E474-7 Max.	Units
t_{AC}	Input to Output delay	0.5	4.0	0.5	5.0	ns
t_{RC}	Chip Select Recovery	0.5	4.0	0.5	5.0	ns
t_{AA}	Address Access Time	1.2	5.0	1.2	7.0	ns
t_{WW}	Write Pulse Width	5.0		5.0		ns
t_{SD}	Data Set-Up to Write	0.0		0.0		ns
t_{HD}	Data Hold to Write	1.0		1.0		ns
t_{SA}	Address Set-Up/Write	1.0		1.0		ns
t_{HA}	Address Hold/Write	1.0		1.0		ns
t_{SC}	Chip Select Set-Up/Write	0.0		0.0		ns
t_{HC}	Chip Select Hold/Write	1.0		1.0		ns
t_{WS}	Write Disable	0.3	4.0	0.3	6.5	ns
t_{WR}	Write Recovery	0.5	5.0	0.5	7.0	ns
t_r	Output Rise Time	1.0	2.5	1.0	2.5	ns
t_f	Output Fall Time	1.0	2.5	1.0	2.5	ns

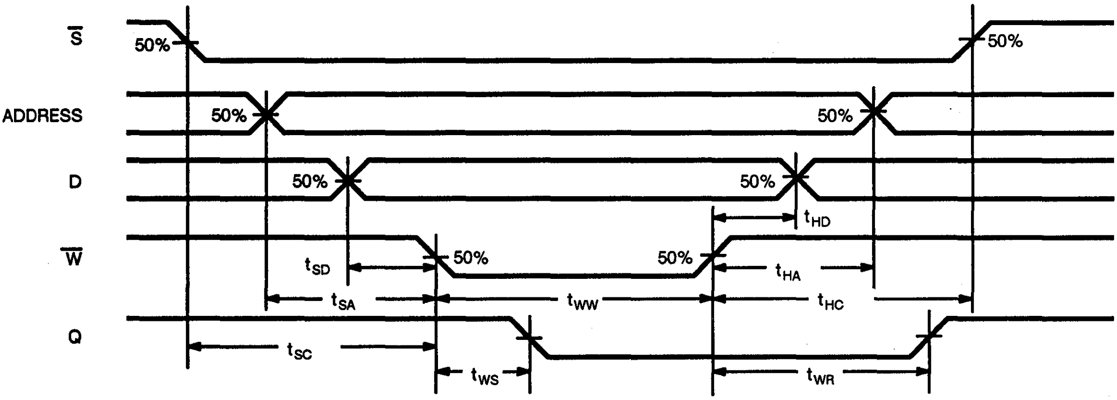
Switching Waveforms

Read Mode



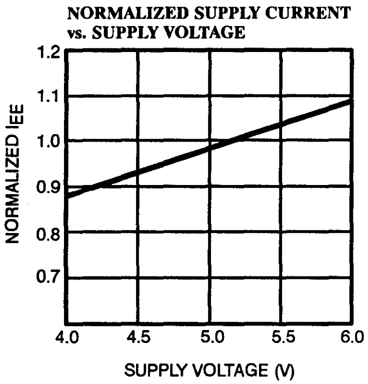
C474-6

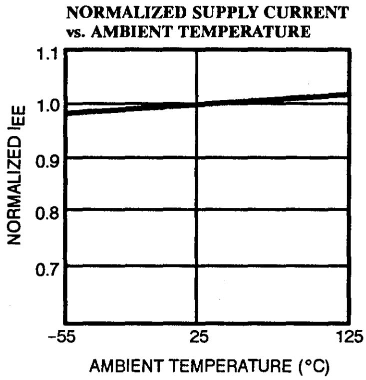
Write Mode

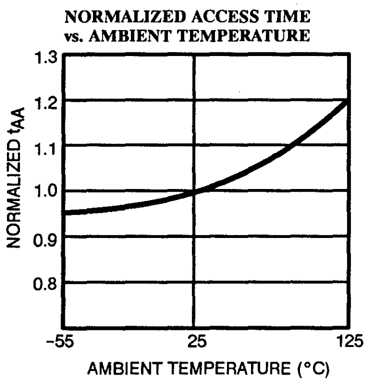


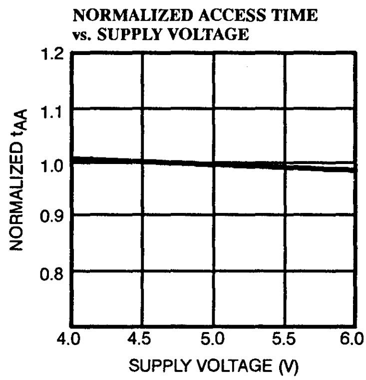
C474-7

Typical DC and AC Characteristics (10E474/10E474L/100E474/100E474L)



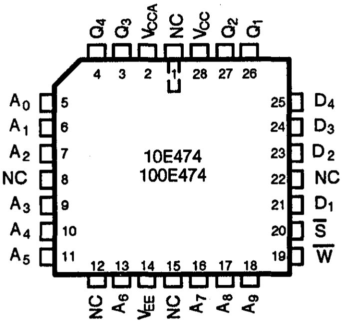




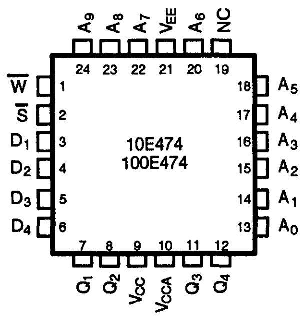


Pin Configurations

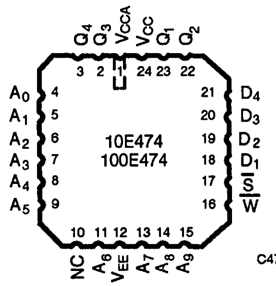
PLCC/CLCC
Top View



Quad Cerpack
Top View



LCC
Top View



C474-8

Truth Table

Input			Output	Mode
$\overline{S}$	$\overline{W}$	D	Q	
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Ordering Information

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Type	Operating Range
100K	275	3	CY100E474-3LC	L63	Commercial
			CY100E474-3YC	Y64	
			CY100E474-3KC	K63	
		5	CY100E474-5LC	L63	
			CY100E474-5DC	D40	
			CY100E474-5YC	Y64	
			CY100E474-5KC	K63	
	190	5	CY100E474L-5LC	L63	Commercial
			CY100E474L-5DC	D40	
			CY100E474L-5JC	J64	
			CY100E474L-5KC	K63	
		7	CY100E474L-7LC	L63	
			CY100E474L-7DC	D40	
			CY100E474L-7JC	J64	
			CY100E474L-7KC	K63	
10E[11]	275	3	CY10E474-3LC	L63	Commercial
			CY10E474-3YC	Y64	
			CY10E474-3KC	K63	
		5	CY10E474-5LC	L63	
			CY10E474-5DC	D40	
			CY10E474-5YC	Y64	
			CY10E474-5KC	K63	
	190	5	CY10E474L-5LC	L63	Commercial
			CY10E474L-5DC	D40	
			CY10E474L-5JC	J64	
			CY10E474L-5KC	K63	
			CY10E474L-5DMB	D40	Military
			CY10E474L-5KMB	K63	
			CY10E474L-5YMB	Y64	
		7	CY10E474L-7LC	L63	Commercial
			CY10E474L-7DC	D40	
			CY10E474L-7JC	J64	
			CY10E474L-7KC	K63	
			CY10E474L-7DMB	D40	Military
			CY10E474L-7KMB	K63	
			CY10E474L-7YMB	Y64	

Notes:

11. 10E specifications support both 10K and 10KH compatibility.

Shaded area contains preliminary information.

Document #: 38-A-00004B

CYPRESS SEMICONDUCTOR

CY1E484
CY10E484
CY100E484

4096 x 4 ECL Static RAM

Features

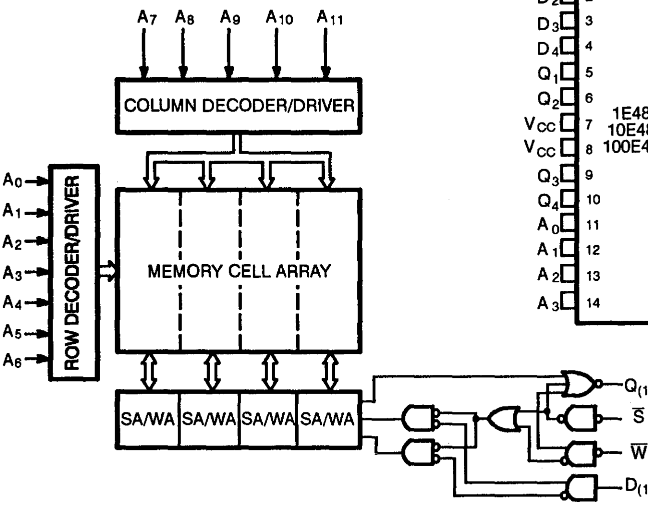
- **4096 x 4 bits organization**
- **Ultra high speed/standard power**
  - **— tAA = 7 ns**
  - **— IEE = TBD mA**
- **Low-power version**
  - **— tAA = 7, 10 ns**
  - **— IEE = 180 mA**
- **Both 10KH/10K and 100K compatible I/O versions**
- **On-chip voltage compensation for improved noise margin**
- **Open emitter output for ease of memory expansion**
- **Industry standard A version pinout**

Functional Description

The Cypress CY1E484, CY10E484 and CY100E484 are 4K x 4 ECL RAMs designed for scratch pad, control and buffer storage applications. These parts are fully decoded random access memories organized and 4096 words by 4 bits. The CY10E484 is 10KH-/10K-compatible. The CY100E484 is 100K-compatible, and the CY1E484 is 100K-compatible with a -5.2V supply.

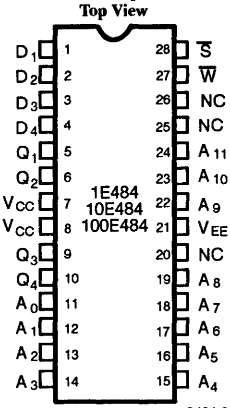
The active LOW chip select ($\overline{S}$) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With ($\overline{W}$) and ($\overline{S}$) LOW, the data at $D_{(1-4)}$ is written into the addressed location. To read, ($\overline{W}$) is held HIGH, while ($\overline{S}$) is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory. The devices are packaged in 28-pin Cerdips, PLCCs and rectangular Cerpacks in the high-performance center power-ground version pin configurations.

Logic Block Diagram

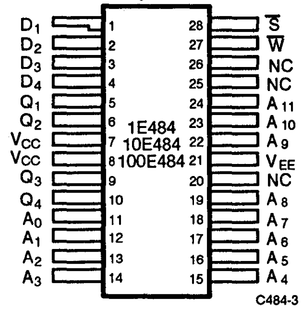


Pin Configurations

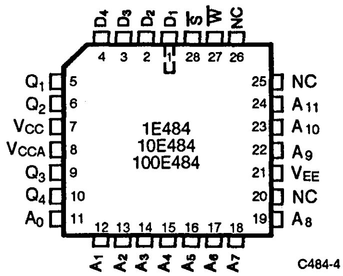
Cerdip
Top View



Rectangular Cerpak
Top View



PLCC
Top View



Selection Guide

			1E484-7 10E484-7 100E484-7	1E484-10 10E484-10 100E484-10
Maximum Access Time (ns)			7	10
I_{EE} Max. (mA)	Commercial		TBD	
	L		180	180

CY1E494
CY10E494
PRELIMINARY **CY100E494**

CYPRESS SEMICONDUCTOR

16,384 x 4 ECL Static RAM

Features

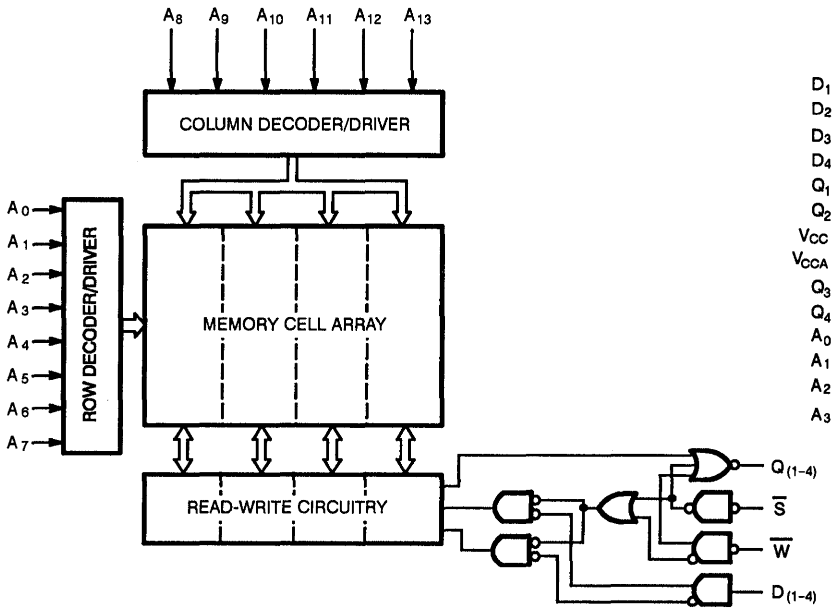
- **16,384 x 4 bits organization**
- **Ultra high speed/standard power**
  - **t_{AA} = 7 ns**
  - **I_{EE} = 180 mA**
- **Low-power version**
  - **t_{AA} = 12 ns**
  - **I_{EE} = 135 mA**
- **Both 10KH/10K and 100K compatible I/O versions as well as 100K with 10K supplies**
- **On-chip voltage compensation for improved noise margin**
- **Open emitter output for ease of memory expansion**
- **Industry standard pinout**

Functional Description

The Cypress CY1E494, CY10E494 and CY100E494 are 16K x 4 ECL RAMs designed for scratch pad, control, and buffer storage applications. These RAMs are developed by Aspen Semiconductor Corporation, a subsidiary of Cypress Semiconductor. Both parts are fully decoded random access memories organized as 16,384 words by 4 bits. The CY10E494 is 10KH-/10K-compatible. The CY100E494 is 100K-compatible, and the CY1E494 has 100K-compatible levels with a -5.2V supply voltage.

The active LOW chip select ($\overline{S}$) input controls memory selection and allows for memory expansion. The read and write operations are controlled by the state of the active LOW write enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ LOW, the data at $D_{(1-4)}$ is written into the addressed location. To read $\overline{W}$ is held HIGH, while $\overline{S}$ is held LOW. Open emitter outputs allow for wired-OR connection to expand the memory.

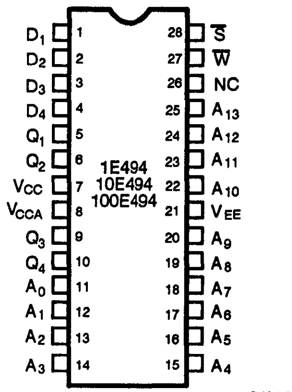
Logic Block Diagram



C494-1

Pin Configuration

Cerdip
Top View



C494-2

Selection Guide

		1E494-7 10E494-7	1E494-10 10E494-10	10E494-12 100E494-12
Maximum Access Time (ns)		7	10	12
Max, I_{EE} (mA)	Commercial	180	180	
	L			135

Maximum Ratings

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested.)

Storage Temperature .... −65°C to +150°C

Ambient Temperature with Power Applied .... −55°C to +125°C

Supply Voltage V_{EE} to V_{CC} .... −7.0 to +0.5V

Input Voltage .... V_{EE} to +0.5V

Output Current.................................. −50 mA

Operating Range Referenced to V_{CC}

Range	I/O	Ambient Temperature	V_{EE}
Commercial (Standard, “L”)	10KH/10K	0°C to 75°C	−5.2V ± 5%
Commercial (Standard, “L”)	100K 1E	0°C to 85°C 0°C to 75°C	−4.5V ± 0.3V −5.2V ± 5%

Electrical Characteristics

Parameters	Description	Test Conditions	Temperature [1]	Min.	Max.	Units
V_{OH}	Output HIGH Voltage	10E[2] R_L = 50 Ω to −2V V_{EE} = −5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	−1000	−840	mV
			T_A = +25°C	−960	−810	mV
			T_A = +75°C	−900	−735	mV
		100E R_L = 50 Ω to −2V V_{EE} = −4.5V, 1E[3] V_{EE} = −5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1025	−880	mV
V_{OL}	Output LOW Voltage	10E R_L = 50 Ω to −2V V_{EE} = −5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C	−1870	−1665	mV
			T_A = +25°C	−1850	−1650	mV
			T_A = +75°C	−1830	−1625	mV
		100E R_L = 50 Ω to −2V V_{EE} = −4.5V, 1E[3] V_{EE} = −5.2V V_{IN} = V_{IH} Max. or V_{IL} Min.	T_A = 0°C to 85°C	−1810	−1620	mV
V_{IH}	Input HIGH Voltage	10E V_{EE} = −5.2V	T_A = 0°C	−1170	−840	mV
			T_A = +25°C	−1130	−810	mV
			T_A = +75°C	−1070	−720	mV
		100E V_{EE} = −4.5V 1E[3] V_{EE} = −5.2V	T_A = 0°C to 85°C	−1165	−880	mV
V_{IL}	Input LOW Voltage	10E V_{EE} = −5.2V	T_A = 0°C	−1950	−1480	mV
			T_A = +25°C	−1950	−1475	mV
			T_A = +75°C	−1950	−1450	mV
		100E V_{EE} = −4.5V 1E[3] V_{EE} = −5.2V	T_A = 0°C to 85°C	−1810	−1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IH} Max.			220	µA
I_{IL}	Input LOW Current	V_{IN} = V_{IL} Min.	$\overline{S}$	0.5	170	µA
			All others	−50		
I_{EE}	Supply Current (All inputs and outputs open)	Commercial L (Low Power)			−135	mA
		Commercial Standard			−180	mA

Notes:

1. Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute.
2. 10E specifications support both 10K and 10KH compatibility.
3. 1E specifications support 100K compatibility with V_{EE}= −5.2V, T_A = 0°C to 75°C.

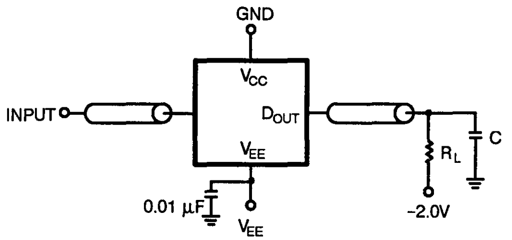
Capacitance[3]

Parameters	Description	Typ.	Max.[4]	Units
C_{IN}	Input Pin Capacitance	3	6	pF
C_{OUT}	Output Pin Capacitance	5	7	pF

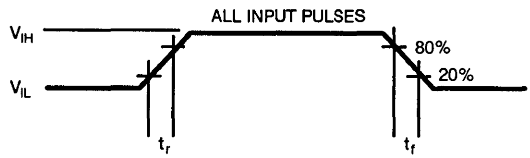
Notes:

3. Tested initially and after any design or process changes that may affect these parameters.
4. For all packages except Cerdip (D42), which has maximums of C_{IN} = 8 pF, C_{OUT} = 9 pF.

AC Test Loads and Waveforms [5, 6, 7, 8, 9, 10]



C494-3



C494-4

Notes:

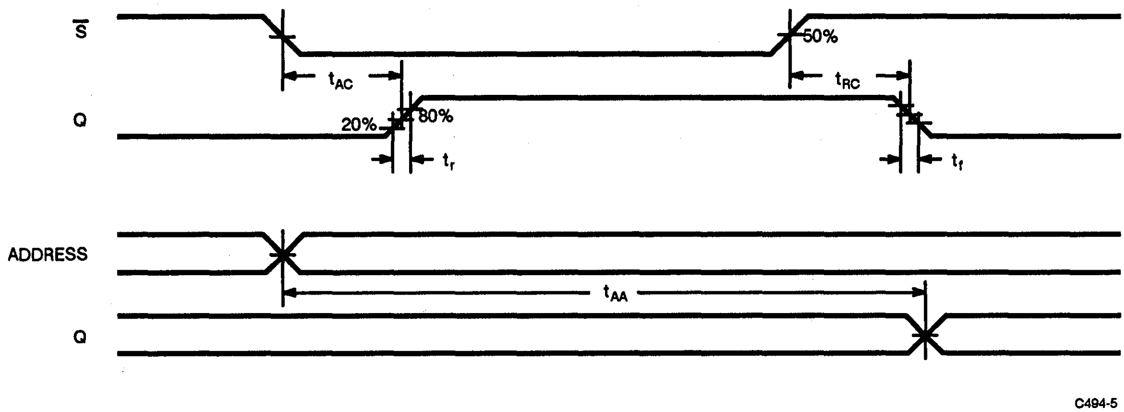
5. V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10E version.
6. V_{IL} = –1.7V, V_{IH} = –0.9V on 100K version.
7. R_L = 50Ω, C < 5 pF (7 ns grade) or < 30 pF (10, 12 ns grade) (includes fixture and stray capacitance).
8. All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be "nulled" out of the measurement.
9. t_r = t_f = 0.7 ns.
10. All timing measurements are made from the 50% point of all waveforms.

Switching Characteristics Over the Operating Range

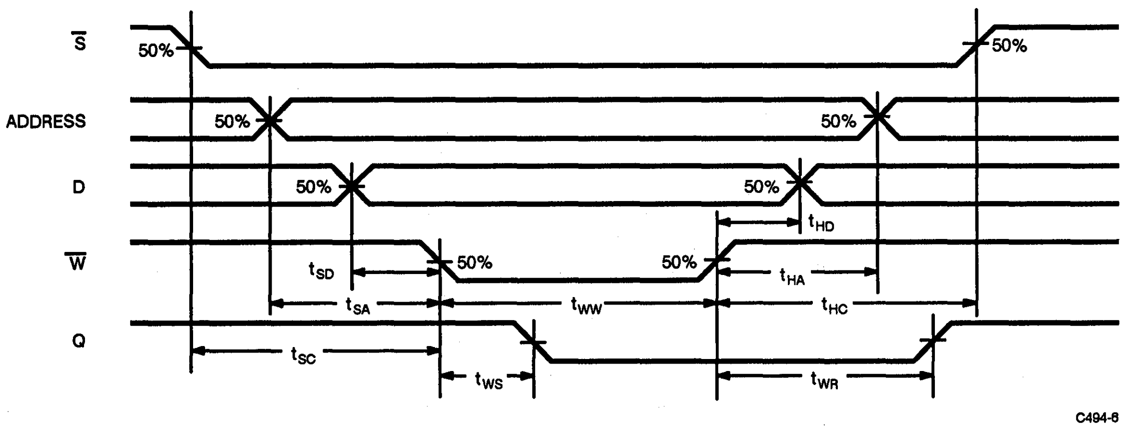
Parameters	Description	1E494-7 10E494-7		1E494-10 10E494-10		10E494-12 100E494-12		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AC}	Input to Output delay		5.0		5.0		5.0	ns
t_{RC}	Chip Select Recovery		5.0		5.0		5.0	ns
t_{AA}	Address Access Time		7.0		10.0		12.0	ns
t_{WW}	Write Pulse Width	5.0		6.0		8.0		ns
t_{SD}	Data Set-Up to Write	1.0		2.0		2.0		ns
t_{HD}	Data Hold to Write	1.0		2.0		2.0		ns
t_{SA}	Address Set-Up/Write	1.0		2.0		2.0		ns
t_{HA}	Address Hold/Write	1.0		2.0		2.0		ns
t_{SC}	Chip Select Set-Up/Write	1.0		2.0		2.0		ns
t_{HC}	Chip Select Hold/Write	1.0		2.0		2.0		ns
t_{WS}	Write Disable		5.0		5.0		5.0	ns
t_{WR}	Write Recovery		8.0		12.0		14.0	ns
t_r	Output Rise Time	0.35	1.5	0.35	2.5	0.75	2.5	ns
t_f	Output Fall Time	0.35	1.5	0.35	2.5	0.75	2.5	ns

Switching Waveforms

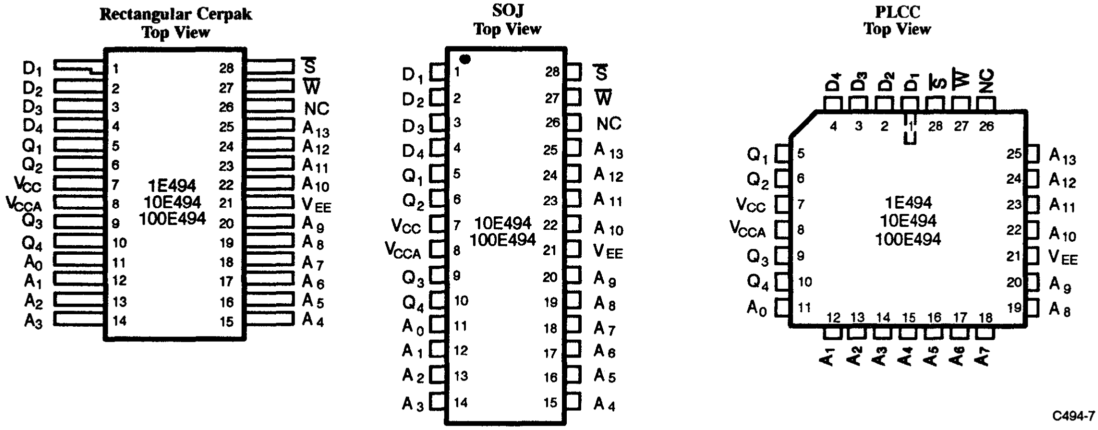
Read Mode



Write Mode



Pin Configurations



Truth Table

Input			Output	Mode
$\overline{S}$	$\overline{W}$	D	Q	
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

9

Ordering Information

I/O	I_{EE} (mA)	t_{AA} (ns)	Ordering Code	Package Type	Operating Range
1E	180	7	CY1E494–7JC	J64	Commercial
			CY1E494–7KC	K74	
			CY1E494–7DC	D42	
		10	CY1E494–10JC	J64	
			CY1E494–10KC	K74	
			CY1E494–10DC	D42	
10K	180	7	CY10E494–7JC	J64	Commercial
			CY10E494–7KC	K74	
			CY10E494–7DC	D42	
		10	CY10E494–10JC	J64	
			CY10E494–10KC	K74	
			CY10E494–10DC	D42	
	135	12	CY10E494L–12JC	J64	Commercial
			CY10E494L–12KC	K74	
			CY10E494L–12VC	V21	
			CY10E494L–12DC	D42	
100K	135	12	CY100E494L–12JC	J64	Commercial
			CY100E494L–12KC	K74	
			CY100E494L–12VC	V21	
			CY100E494L–12DC	D42	

Document #: 38–A–00009A

Section Contents

Military Information

Page Number

CYPRESS SEMICONDUCTOR

Military Overview

Features

Success in any endeavor requires a high level of dedication to the task. Cypress Semiconductor has demonstrated its dedication through its corporate commitment to support the military marketplace. This commitment starts with product design. All products are designed on our state-of-the-art CMOS, BiCMOS, and Bipolar processes, and they must meet the full - 55 to + 125 degrees Celsius operational criteria for military use. The commitment continues with the 1986 DESC certification of our automated U.S. facility in San Jose, California. The commitment shows in our dedication to meet and exceed the stringent quality and reliability requirements of MIL-STD-883 and MIL-M-38510. It shows in Cypress's participation in each of the military processing programs: MIL-STD-883C compliant, SMD (Standardized Military Drawing) and JAN. Finally, our commitment shows in our leadership position in special packages for military use.

Product Design

Every Cypress product is designed to meet or exceed the full temperature and functional requirements of military product. This means that Cypress builds military product as a matter of course, rather than as an accidental benefit of favorable test yield. Designs are being carried out on our industry-leading 0.8 micron CMOS, BiCMOS, and Bipolar processes. Cypress is able to offer a family of products that are industry leaders in density, low operating and standby current, and high speed. In addition, our technology results in products with very small manufacturable die sizes that will fit into the LCCs and flatpacks so often used in military programs.

DESC-Certified Facility

On May 8, 1986, the Cypress facility at 3901 North First Street in San Jose, California was certified by DESC for the production of JAN Class B CMOS Microcircuits. This certification not only allows Cypress to qualify product for JAN use, but also assures our customers that our San Jose Facility has the necessary documentation and procedures to manufacture product to the most stringent of quality and reliability requirements. Our wafer fabrication facilities are Class 10 (San Jose) and Class 1 (Round Rock, TX) manufacturing environments and our assembly facility is also a clean room. In addition, our highly automated assembly facility is located entirely in the U.S.A. and is capable of handling virtually any hermetic package configuration.

Data Sheet Documentation

Every Cypress final data sheet is a corporate document with a revision history. The document number and revision appears on each final data sheet. Cypress maintains a listing of all data sheet documentation and a copy is available to customers upon request. This gives a customer the ability to verify the current status of any data sheet and it also gives that customer the ability to obtain updated specifications as required.

Every final data sheet also contains detailed Group A subgroup testing information. Each of the specified parameters that are tested at Group A are listed in a table at the end of each final data sheet, with a notation as to which specific Group A test subgroups apply.

Assembly Traceability Code™

Cypress Semiconductor marks an assembly traceability code on every military package that is large enough to contain the code. The ATC automatically provides traceability for that product to the individual wafer lot. This unique code provides Cypress with the ability to determine which operators and equipment were used in the manufacture of that product from start to finish.

Quality and Reliability

MIL-STD-883 and MIL-M-38510 spell out the toughest of quality and reliability standards for military products. Cypress products meet all of these requirements and more. Our in-house quality and reliability programs are being updated regularly with tighter and tighter objectives. Please refer to the chapter on Quality, Reliability, and Process Flows for further details.

Military Product Offerings

Cypress offers three different levels of processing for military product.

First, all Cypress products are available with processing in full compliance with MIL-STD-883, Revision C.

Second, selected products are available to the SMD (Standardized Military Drawing) program administered by DESC. These products are not only fully MIL-STD-883C compliant but they are also screened to the electrical requirements of the applicable military drawing.

Third, selected products are available as JAN devices. These products are processed in full accordance with MIL-M-38510 and they are screened to the electrical requirements of the applicable JAN slash sheet.

Product Packaging

All packages for military product are hermetic. A look at the package appendix in the back of this data book will give the reader an appreciation of the variety of packages offered. Included are CERDIPs, windowed CERDIPs, leadless chip carriers (LCCs), leadless chip carriers with windows for reprogrammable products, CERPAK, windowed CERPAK, quad CERPAK, windowed quad CERPAK, bottom-brazed flatpacks, and pin grid arrays. As indicated above, all of these packages are assembled in the U.S. in our highly automated San Jose plant.

Summary

Cypress Semiconductor is committed to the support of the military marketplace. Our commitment is demonstrated by our product designs, our DESC-certified facility, our documentation and traceability, our quality and reliability programs, our support of all levels of military processing and by our leadership in special packaging.

Static RAMs

Size	Organization	Pins (DIP)	Part Number	JAN/SMD Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	883 Availability
64	16x4—Inverting	16	CY7C189		t_{AA} = 25	70@25	Now
64	16x4—Non-Inverting	16	CY7C190	5962-89694	t_{AA} = 25	70@25	Now
64	16x4—Inverting	16	CY27S03/A		t_{AA} = 25, 35	100@35	Now
64	16x4—Non-Inverting	16	CY27S07/A		t_{AA} = 25, 35	100@25	Now
64	16x4—Inverting/Low Power	16	CY27LS03		t_{AA} = 65	38@65	Now
1K	256x4—10K/10KH ECL	24	CY10E422L		t_{AA} = 5, 7	150@5/7	Now
1K	256x4	22	CY7C122	5962-88594	t_{AA} = 25, 35	90@25	Now
1K	256x4	24S	CY7C123		t_{AA} = 10, 12, 15	150@15	Now
1K	256x4	22	CY9122/91L22	5962-88594	t_{AA} = 35, 45	90@45	Now
1K	256x4	22	CY93422A/93L422A		t_{AA} = 45, 55, 60, 75	90@55	Now
4K	4Kx1—CS Power Down	18	CY7C147	M38510/289	t_{AA} = 35, 45	110/10@35	Now
4K	4Kx1—CS Power Down	18	CY2147	M38510/289	t_{AA} = 45, 55	140/25@45	Now
4K	4Kx1—CS Power Down	18	CY7C147	5962-88587	t_{AA} = 35, 45	110/10@35	Now
4K	4Kx1—CS Power Down	18	CY2147	5962-88587	t_{AA} = 45, 55	140/25@45	Now
4K	1Kx4—10K/10KH ECL	24	CY10E474L		t_{AA} = 5, 7	190@5/7	Now
4K	1Kx4—CS Power Down	18	CY7C148	M38510/289	t_{AA} = 35, 45	110/10@35	Now
4K	1Kx4—CS Power Down	18	CY2148	M38510/289	t_{AA} = 45, 55	140/25@45	Now
4K	1Kx4	18	CY7C149		t_{AA} = 35, 45	110@35	Now
4K	1Kx4	18	CY2149		t_{AA} = 45, 55	140@45	Now
4K	1Kx4—Separate I/O	24S	CY7C150	5962-88588	t_{AA} = 12, 15, 25, 35	100@15	Now
8K	1Kx8—Dual Port	48	CY7C130/31	5962-86875	t_{AA} = 35, 45, 55	120/40@45	Now
8K	1Kx8—Dual Port Slave	48	CY7C140/41	5962-86875	t_{AA} = 35, 45, 55	120/40@45	Now
16K	2Kx8—CS Power Down	24S	CY7C128A	5962-89690	t_{AA} = 20, 25	125@20	Now
16K	2Kx8—CS Power Down	24	CY6116A/7A	5962-89690	t_{AA} = 20, 25	125@20	Now
16K	2Kx8—CS Power Down	24S	CY7C128	84036	t_{AA} = 45, 55	100/20@55	Now
16K	2Kx8—CS Power Down	24S	CY7C128A	84036	t_{AA} = 20, 25, 35	125/40@25	Now
16K	2Kx8—CS Power Down	24	CY6116/7	84036	t_{AA} = 45, 55	130/20@45	Now
16K	16Kx1—CS Power Down	20	CY7C167	84132	t_{AA} = 35, 45	50/20@45	Now
16K	16Kx1—CS Power Down	20	CY7C167A	84132	t_{AA} = 20, 25, 35	70/20@25	Now
16K	4Kx4—CS Power Down	20	CY7C168	5962-86705	t_{AA} = 35, 45	70/20@45	Now
16K	4Kx4—CS Power Down	20	CY7C168A	5962-86705	t_{AA} = 20, 25, 35	100/20@25	Now
16K	4Kx4	20	CY7C169		t_{AA} = 40	70@40	Now
16K	4Kx4	20	CY7C169A		t_{AA} = 20, 25, 35	100/20@35	Now
16K	4Kx4—Output Enable	22S	CY7C170		t_{AA} = 45	120@45	Now
16K	4Kx4—Output Enable	22S	CY7C170A		t_{AA} = 20, 25, 35	120@25	Now
16K	4Kx4—Separate I/O, T-write	24S	CY7C171		t_{AA} = 45	70@45	Now
16K	4Kx4—Separate I/O	24S	CY7C172		t_{AA} = 45	70@45	Now
16K	4Kx4—Separate I/O	24S	CY7C171A/2A		t_{AA} = 20, 25, 35	100/20@25	Now
16K	2Kx8—Dual Port	48	CY7C132/36		t_{AA} = 35, 45, 55	170/65@35	Now
16K	2Kx8—Dual Port Slave	48	CY7C142/46		t_{AA} = 35, 45, 55	120/40@45	Now
64K	8Kx8—CS Power Down	28S	CY7C185A	5962-89691	t_{AA} = 20, 25	125@20	Now
64K	8Kx8—CS Power Down	28S	CY7C185A	5962-85525	t_{AA} = 35, 45, 55	100/20/1@45	Now
64K	8Kx8—CS Power Down	28S	CY7B185		t_{AA} = 15	145/50@15	Now
64K	8Kx8—CS Power Down	28	CY7C186A	5962-89691	t_{AA} = 20, 25	125@20	Now
64K	8Kx8—CS Power Down	28	CY7C186A	5962-85525	t_{AA} = 35, 45, 55	100/20/1@45	Now
64K	8Kx8—CS Power Down	28	CY7B186		t_{AA} = 15	145/50@15	Now
64K	16Kx4—CS Power Down	22S	CY7C164A	5962-89692	t_{AA} = 20, 25	90@20	Now
64K	16Kx4—CS Power Down	22S	CY7C164A	5962-86859	t_{AA} = 35, 45	70/20/1@35	Now
64K	16Kx4—CS Power Down	22S	CY7B164		t_{AA} = 15	135/50@15	Now
64K	16Kx4—CS Power Down	22S	CY7C166A	5962-89892	t_{AA} = 20, 25	90@20	Now
64K	16Kx4—Output Enable	24S	CY7C166A	5962-86859	t_{AA} = 35, 45	70/20/1@35	Now
64K	16Kx4—Output Enable	24S	CY7B166		t_{AA} = 15	135/50@15	Now
64K	16Kx4—Separate I/O, T-write	28S	CY7C161A		t_{AA} = 20, 25, 35, 45	70/20/1@35	Now
64K	16Kx4—Separate I/O	28S	CY7C162A	5962-89712	t_{AA} = 20, 25, 35, 45	70/20/1@35	Now
64K	16Kx4—Separate I/O	28S	CY7B161/2		t_{AA} = 15	135/50@15	2Q90
64K	64Kx1—CS Power Down	22S	CY7C187A	5962-86015	t_{AA} = 20, 25, 35, 45	70/20/1@35	Now
256K	16Kx16—Cache RAM	44	CY7C157		t_{AA} = 24, 33	300@24	Now
256K	32Kx8—CS Power Down	28	CY7C198	5962-88662	t_{AA} = 35, 45, 55	160/20@35	Now
256K	32Kx8—CS Power Down	28S	CY7C199	5962-88662	t_{AA} = 35, 45, 55	160/20@35	Now
256K	64Kx4—CS Power Down	24S	CY7C194	5962-88681	t_{AA} = 35, 45	130/20@35	Now
256K	64Kx4—CS PD + OE/CE2	28S	CY7C196		t_{AA} = 35, 45	130/20@35	Now
256K	64Kx4—Separate I/O, T-write	28S	CY7C191		t_{AA} = 35, 45	130/20@35	Now

Static RAMs (continued)

Size	Organization	Pins (DIP)	Part Number	JAN/SMD Number	Speed (ns)	$I_{CC}/I_{SB}/I_{CCDR}$ (mA@ns)	883 Availability
256K	64Kx4 – Separate I/O	28S	CY7C192		t_{AA} = 35, 45	130/20@35	Now
256K	256Kx1 – CS Power Down	24S	CY7C197	5962-88725	t_{AA} = 35, 45	110/20@35	Now

PROMs

Size	Organization	Pins	Part Number	JAN/SMD Number[1]	Speed (ns)	I_{CC}/I_{SB} (mA@ns)	883 Availability
4K	512x8 – Registered	24S	CY7C225	5962-88518(O)	$t_{SA/CO}$ = 30/15, 35/20, 40/25	120@30/15	Now
8K	1Kx8 – Registered	24S	CY7C235	5962-88636(O)	$t_{SA/CO}$ = 30/15, 40/20	120@30/15	Now
8K	1Kx8	24S	CY7C281	5962-87651(O)	t_{AA} = 45	120@45	Now
8K	1Kx8	24	CY7C282	5962-87651(O)	t_{AA} = 45	120@45	Now
16K	2Kx8 – Registered	24S	CY7C245	5962-87529(W)	$t_{SA/CO}$ = 35/15, 45/25	120@35/15	Now
16K	2Kx8 – Registered	24S	CY7C245A	5962-89815(W)	t_{SA} = 25/15, 35/20	120@25/15	Now
16K	2Kx8 – Registered	24S	CY7C245A	5962-88735(O)	$t_{SA/CO}$ = 25/15, 35/20	120@25/15	Now
16K	2Kx8	24S	CY7C291	5962-87650(W)	t_{AA} = 35, 50	120@35	Now
16K	2Kx8	24S	CY7C291A	5962-88734(O)	t_{AA} = 25, 30, 35, 50	120@30	Now
16K	2Kx8 – CS Power Down	24S	CY7C293A	5962-88680(W)	t_{AA} = 25, 30, 35, 50	120/30@35	Now
16K	2Kx8	24	CY7C292		t_{AA} = 50	120@50	Now
16K	2Kx8	24	CY7C292A	5962-88734(O)	t_{AA} = 25, 30, 35, 50	120@30	Now
64K	8Kx8 – CS Power Down	24S	CY7C261	5962-87515(W)	t_{AA} = 45, 55	120/30@45	Now
64K	8Kx8	24S	CY7C263		t_{AA} = 45, 55	120@45	Now
64K	8Kx8	24	CY7C264		t_{AA} = 45, 55	120@45	Now
64K	8Kx8 – Registered	28S	CY7C265		$t_{SA/CO}$ = 50/25, 60/25	120@50/25	Now
64K	8Kx8 – EPROM Pinout	28	CY7C266		t_{AA} = 55	90	Now
64K	8Kx8 – Registered/Diagnostic	28S	CY7C269		$t_{SA/CO}$ = 50/25, 60/25	100@60/25	Now
64K	8Kx8 – Registered/Diagnostic	32	CY7C268		$t_{SA/CO}$ = 50/25, 60/25	100@60/25	Now
128K	16Kx8 – CS Power Down	28S	CY7C251	5962-89537(W)	t_{AA} = 55, 65	120/35@55	Now
128K	16Kx8	28	CY7C254	5962-89538(W)	t_{AA} = 55, 65	120@55	Now
256K	32Kx8 – CS Power Down	28S	CY7C271		t_{AA} = 45, 55	130/40@55	Now
256K	32Kx8 – EPROM Pinout	28	CY7C274		t_{AA} = 45, 55	130/40@55	Now
256K	32Kx8 – Registered	28S	CY7C277		$t_{SA/CO}$ = 40/20, 50/25	130/40@55	Now
256K	32Kx8 – Latched	28S	CY7C279		t_{AA} = 45, 55	130/40@55	Now
512K	64Kx8 – Fast Column Access	28S	CY7C285		t_{AA}/FCA = 65/25	200@65	2Q90
512K	64Kx8 – EPROM Pinout	28	CY7C286		t_{AA} = 70	150@70	2Q90
512K	64Kx8 – Registered	28S	CY7C287		$t_{SA/CO}$ = 65/20	150@65	2Q90
512K	64Kx8 – FCA/Reg or Latched	32S	CY7C289		t_{AA}/FCA = 65/25	200@65	2Q90

PLDs

	Organization	Pins	Part Number	JAN/SMD Number[1]	Speed (ns/MHz)	I_{CC} (mA@ns/MHz)	883 Availability
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88678(W)	t_{PD} = 20, 30, 40	70@20	Now
PALC20	16L8, 16R8, 16R6, 16R4	20	PALC16XX	5962-88713(O)	t_{PD} = 20, 30, 40	70@20	Now
PLD20	18G8 – Generic	20	PLDC18G8		$t_{PD/S/CO}$ = 15/15/20	110	2Q90
PLDC24	22V10 – Macrocell	24S	PALC22V10	5962-87539(W)	$t_{PD/S/CO}$ = 20/17/15	100@25	Now
PLDC24	22V10 – Macrocell	24S	PALC22V10	5962-88670(O)	$t_{PD/S/CO}$ = 20/17/15	100@25	Now
PLDC24	22V10 – Macrocell	24S	PALC22V10	M38510/507	$t_{PD/S/CO}$ = 25/18/15	120@25	2Q90
PLDC24	20G10 – Generic	24S	PLDC20G10	5962-88637(O)	$t_{PD/S/CO}$ = 20/17/15	80@30	Now
PLDC24	20RA10 – Asynchronous	24S	PLD20RA10		$t_{PD/SU/CO}$ = 25/15/25	100@25	Now
ECL	16P8 – 10KH ECL	24S	CY10E301		t_{PD} = 5	-240@5	Now
ECL	16P4 – 10KH ECL	24S	CY10E302		t_{PD} = 4	-220@4	Now
PLDC28	7C330 – State Machine	28S	CY7C330	5962-89546(W)	50, 40, 28 MHz	180@40MHz	Now
PLDC28	7C331 – Asynchronous	28S	CY7C331	5962-89855(O)	$t_{PD/S/CO}$ = 30/25/30	200@20MHz	Now
PLDC28	7C332 – Combinatorial	28S	CY7C332		$t_{ICO/IS/IH}$ = 25/5/7	200@24MHz	Now
MAX28	7C344 – 32 Macrocell	28S	CY7C344		$t_{PD/S/CO}$ = 25/15/15	TBD	3Q90
MAX40	7C343 – 64 Macrocell	40/44	CY7C343		$t_{PD/S/CO}$ = 35/25/20	TBD	4Q90
MAX40	7C345 – 128 Macrocell	40/44	CY7C345		$t_{PD/S/CO}$ = 35/25/20	TBD	3Q90
MAX68	7C342 – 128 Macrocell	68	CY7C342		$t_{PD/S/CO}$ = 35/25/20	TBD	3Q90
PLDC28	7C361 – State Machine	28S	CY7C361		100, 83, 50 MHz	150@100MHz	3Q90

FIFOs

Organization	Pins	Part Number	JAN/SMD Number	Speed	I_{CC}/I_{SB} (mA @ ns/MHz)	883 Availability
64x4—Cascadeable	16	CY3341		1.2, 2 MHz	60 @ 2.0 MHz	Now
64x4—Cascadeable	16	CY7C401		10, 15, 25 MHz	90 @ 15 MHz	Now
64x4—Cascadeable/OE	16	CY7C403	5962-89523	10, 15, 25 MHz	90 @ 25 MHz	Now
64x5—Cascadeable	18	CY7C402		10, 15, 25 MHz	90 @ 15 MHz	Now
64x5—Cascadeable/OE	18	CY7C404	5962-86846	10, 15, 25 MHz	90 @ 25 MHz	Now
64x8—Cascadeable/OE	28S	CY7C408A	5962-89664	15, 25 MHz	120 @ 25 MHz	Now
64x9—Cascadeable	28S	CY7C409A	5962-89661	15, 25 MHz	120 @ 25 MHz	Now
512x9—Cascadeable	28	CY7C420	5962-89863	t_A = 30, 40, 65 ns	120/20 @ 30	Now
512x9—Cascadeable	28S	CY7C421	5962-89863	t_A = 30, 40, 65 ns	120/20 @ 30	Now
1Kx9—Cascadeable	28	CY7C424		t_A = 30, 40, 65 ns	120/20 @ 30	Now
1Kx9—Cascadeable	28S	CY7C425		t_A = 30, 40, 65 ns	120/20 @ 30	Now
2Kx9—Cascadeable	28	CY7C428	5962-88669	t_A = 30, 40, 65 ns	120/20 @ 30	Now
2Kx9—Cascadeable	28S	CY7C429	5962-88669	t_A = 30, 40, 65 ns	120/20 @ 30	Now
2Kx9—Bidirectional	28S	CY7C439		t_A = 40, 65 ns	120/20 @ 40	2Q90
4Kx9—Cascadeable	28	CY7C432		t_A = 30, 40, 65 ns	160/20 @ 30	Now
2Kx9—Cascadeable	28S	CY7C433		t_A = 30, 40, 65 ns	160/20 @ 30	Now

Logic

Organization	Pins	Part Number	JAN/SMD Number	Speed (ns)	I_{CC} (mA @ ns)	883 Availability
2901—4-Bit Slice	40	CY7C901	5962-88535	t_{CLK} = 27, 32	90 @ 27	Now
2901—4-Bit Slice	40	CY2901C	5962-88535	C	180 @ 32	Now
4x2901—16-Bit Slice	64	CY7C9101	5962-89517	t_{CLK} = 35, 45	85 @ 35	Now
2909—Sequencer	28	CY7C909		t_{CLK} = 30, 40	55 @ 30	Now
2911—Sequencer	20	CY7C911		t_{CLK} = 30, 40	55 @ 30	Now
2909—Sequencer	28	CY2909A		A	90 @ 40	Now
2911—Sequencer	20	CY2911A		A	90 @ 40	Now
2910—Controller (17-Word Stack)	40	CY7C910	5962-87708	t_{CLK} = 46, 51, 99	90 @ 46	Now
2910—Controller (9-Word Stack)	40	CY2910A	5962-87708	A	170 @ 51	Now
16-Bit Microprogrammed ALU	52	CY7C9116	5962-88612	40, 65, 79	166 @ 10 MHz	Now
16-Bit Microprogrammed ALU	68	CY7C9117		40, 65, 79	166 @ 10 MHz	Now
16x16 Multiplier	64	CY7C516	5962-86873	t_{MC} = 42, 55, 75	110 @ 10 MHz	Now
16x16 Multiplier	64	CY7C517	5962-87686	t_{MC} = 42, 55, 75	110 @ 10 MHz	Now
16x16 Multiplier/Accumulator	64	CY7C510	5962-88733	t_{MC} = 55, 65, 75	110 @ 10 MHz	Now

RISC

	Description	Pins	Part Number	Speed (ns)	I_{CC} (mA @ MHz)	883 Availability
IU	SPARC 32-Bit Integer Unit	207	CY7C601	t_{CYC} = 33, 25 MHz	TBD	Now
FPU	Floating-Point Unit	144	CY7C602	t_{CYC} = 33, 25 MHz	TBD	2H90
CMU	Cache-Controlled Memory Management Unit	244	CY7C604	t_{CYC} = 33, 25 MHz	TBD	1H90
CMU-MP	Cache Controller and Multiprocessing Memory Management Unit	244	CY7C605	t_{CYC} = 33, 25 MHz	TBD	2H90
CRAM	SPARC Cache RAM	52	CY7C157	t_{AA} = 33, 24	TBD	2H90

Modules

Size	Organization	Pins	Part Number	Packages	Speed (ns)	I_{CC} (mA@ns)	883 Availability
256K	64Kx4 SRAM (JEDEC)	24	CYM1220	HD08	t_{AA} = 12, 15, 20	375@12	Now
256K	32Kx8 SRAM (JEDEC)	28	CYM1400	HD09	t_{AA} = 12, 15, 20	425@12	Now
256K	16Kx16 SRAM (JEDEC)	40	CYM1610	HD01	t_{AA} = 15, 20, 25, 35, 45, 50	550@15; 330@25	Now
256K	16Kx16 SRAM	36	CYM1611	HV01	t_{AA} = 15, 20, 25, 30, 35, 45	550@15; 330@25	Now
512K	16Kx32 SRAM	88	CYM1822	HV02	t_{AA} = 15, 20, 25, 30, 35, 45	960@15; 720@25	Now
1M	256Kx4 SRAM (JEDEC)	28	CYM1240	HD07	t_{AA} = 35, 45	480@35	Now
1M	128Kx8 SRAM (JEDEC)	32	CYM1420	HD04	t_{AA} = 45, 55	210@45	Now
1M	64Kx16 SRAM (JEDEC)	40	CYM1620	HD03	t_{AA} = 45, 55	340@45	Now
1M	64Kx16 SRAM	40	CYM1621	HD02	t_{AA} = 25, 30, 35, 45	1250@25	Now
1M	64Kx16 SRAM	40	CYM1622	HV03	t_{AA} = 25, 35, 45	400@25	Now
2M	64Kx32 SRAM	60	CYM1830	HD06	t_{AA} = 35, 45, 55	880@35	Now
4M	256Kx16 SRAM	48	CYM1641	HD05	t_{AA} = 35, 45, 55	1800@35	Now

Notes:

The Cypress facility at 3901 North First Street in San Jose, CA is DESC-certified for JAN class B production.

All of the above products are available with processing to MIL-STD-883C at a minimum. Many of these products are also available either to SMDs (Standardized Military Drawings) or to JAN slash sheets.

The speed and power specifications listed above cover the full military temperature range. All power supplies are V_{CC} = 5V ± 10%.

Modules are available with MIL-STD-883C components. These modules are assembled and screened to the proposed JEDEC military processing standard for modules.

1. (W) = Windowed Package
   (O) = Opaque Package
   HD = Hermetic DIP Module

2. 100K ECL devices are available only to extended temperature range.

22S stands for 22-pin 300-mil DIP.
24S stands for 24-pin 300-mil DIP.
28S stands for 28-pin 300-mil DIP.

Cypress Semiconductor fully supports the DESC standardized Military Drawing Program for devices that are compliant to the Class B requirements of MIL-STD-883.

Listed below are the SMDs for which Cypress is an approved source of supply. Please contact your local Cypress representative for the latest SMD update.

DESC SMD (Standardized Military Drawing) Approvals[1]

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
84036 09JX	CY6116-45DMB	24.6 DIP	D12	2K x 8 SRAM
84036 09KX	CY7C128-45KMB	24 CP	K73	2K x 8 SRAM
84036 09LX	CY7C128-45DMB	24.3 DIP	D14	2K x 8 SRAM
84036 09XX	CY6117-45LMB	32 R LCC	L55	2K x 8 SRAM
84036 09YX	CY7C128-45LMB	24 R LCC	L53	2K x 8 SRAM
84036 093X	CY6116-45LMB	28 S LCC	L64	2K x 8 SRAM
84036 11JX	CY6116-55DMB	24.6 DIP	D12	2K x 8 SRAM
84036 11KX	CY7C128-55KMB	24 CP	K73	2K x 8 SRAM
84036 11LX	CY7C128-55DMB	24.3 DIP	D14	2K x 8 SRAM
84036 11XX	CY6117-55LMB	32 R LCC	L55	2K x 8 SRAM
84036 11YX	CY7C128-55LMB	24 R LCC	D14	2K x 8 SRAM
84036 113X	CY6116-55LMB	28 S LCC	L64	2K x 8 SRAM
84036 14JX	CY6116A-35DMB	24.6 DIP	D12	2K x 8 SRAM
84036 14KX	CY7C128A-35KMB	24 CP	K73	2K x 8 SRAM
84036 14LX	CY7C128A-35DMB	24.3 DIP	D14	2K x 8 SRAM
84036 14XX	CY6117A-35LMB	32 R LCC	L55	2K x 8 SRAM
84036 14YX	CY7C128A-35LMB	24 R LCC	L53	2K x 8 SRAM
84036 143X	CY6116A-35LMB	28 S LCC	L64	2K x 8 SRAM
84132 02RX	CY7C167-45DMB	20.3 DIP	D6	16K x 1 SRAM
84132 02SX	CY7C167-45KMB	20 CP	K71	16K x 1 SRAM
84132 02YX	CY7C167-45LMB	20 R LCC	L51	16K x 1 SRAM
84132 05RX	CY7C167-35DMB	20.3 DIP	D6	16K x 1 SRAM
84132 05SX	CY7C167-35KMB	20 CP	K71	16K x 1 SRAM
84132 05YX	CY7C167-35LMB	20 R LCC	L51	16K x 1 SRAM
5962-85525 05TX	CY7C185A-55KMB	28 CP	K74	8K x 8 SRAM
5962-85525 05UX	CY7C185A-55LMB	28 R TLCC	L54	8K x 8 SRAM
5962-85525 05XX	CY7C186A-55DMB	28.6 DIP	D16	8K x 8 SRAM
5962-85525 05ZX	CY7C185A-55DMB	28.3 DIP	D22	8K x 8 SRAM
5962-85525 06TX	CY7C185A-45KMB	28 CP	K74	8K x 8 SRAM
5962-85525 06UX	CY7C185A-45LMB	28 R TLCC	L54	8K x 8 SRAM
5962-85525 06XX	CY7C186A-45DMB	28.6 DIP	D16	8K x 8 SRAM
5962-85525 06ZX	CY7C185A-45DMB	28.3 DIP	D22	8K x 8 SRAM
5962-85525 07TX	CY7C185A-35KMB	28 CP	K74	8K x 8 SRAM
5962-85525 07UX	CY7C185A-35LMB	28 R TLCC	L54	8K x 8 SRAM
5962-85525 07XX	CY7C186A-35DMB	28.6 DIP	D16	8K x 8 SRAM
5962-85525 07ZX	CY7C185A-35DMB	28.3 DIP	D22	8K x 8 SRAM
5962-86015 01YX	CY7C187A-35DMB	22.3 DIP	D10	64K x 1 SRAM
5962-86015 01ZX	CY7C187A-35LMB	22 R LCC	L52	64K x 1 SRAM
5962-86015 02YX	CY7C187AL-35DMB	22.3 DIP	D10	64K x 1 SRAM
5962-86015 02ZX	CY7C187AL-35LMB	22 R LCC	L52	64K x 1 SRAM
5962-86015 03YX	CY7C187A-45DMB	22.3 DIP	D10	64K x 1 SRAM
5962-86015 03ZX	CY7C187A-45LMB	22 R LCC	L52	64K x 1 SRAM
5962-86015 04YX	CY7C187AL-45DMB	22.3 DIP	D10	64K x 1 SRAM
5962-86015 04ZX	CY7C187AL-45LMB	22 R LCC	L52	64K x 1 SRAM
5962-86705 12RX	CY7C168-35DMB	20.3 DIP	D6	4K x 4 SRAM
5962-86705 12XX	CY7C168-35LMB	20 R LCC	L51	4K x 4 SRAM
5962-86846 01VX	CY7C404-10DMB	18.3 DIP	D4	64 x 5 FIFO
5962-86846 012X	CY7C404-10LMB	20 S LCC	L61	64 x 5 FIFO
5962-86846 01XX	CY7C404-10KMB	18 CP	K70	64 x 5 FIFO
5962-86846 02VX	CY7C404-15DMB	18.3 DIP	D4	64 x 5 FIFO
5962-86846 022X	CY7C404-15LMB	20 S LCC	L61	64 x 5 FIFO
5962-86846 02XX	CY7C404-15KMB	18 CP	K70	64 x 5 FIFO
5962-86846 03VX	CY7C404-25DMB	18.3 DIP	D4	64 x 5 FIFO
5962-86846 032X	CY7C404-25LMB	20 S LCC	L61	64 x 5 FIFO

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962-86846 03XX	CY7C404-25KMB	18 CP	K70	64 x 5 FIFO
5962-86859 15KX	CY7C166AL-45KMB	24 CP	K73	16K x 4 SRAM W/OE
5962-86859 15LX	CY7C166AL-45DMB	24.3 DIP	D14	16K x 4 SRAM W/OE
5962-86859 15UX	CY7C166AL-45LMB	28 R LCC	L54	16K x 4 SRAM W/OE
5962-86859 15XX	CY7C166AL-45LMB	28 R TLCC	L54	16K x 4 SRAM W/OE
5962-86859 16KX	CY7C166A-45KMB	24 CP	K73	16K x 4 SRAM W/OE
5962-86859 16LX	CY7C166A-45DMB	24.3 DIP	D14	16K x 4 SRAM W/OE
5962-86859 16UX	CY7C166A-45LMB	28 R LCC	L54	16K x 4 SRAM W/OE
5962-86859 16XX	CY7C166A-45LMB	28 R TLCC	L54	16K x 4 SRAM W/OE
5962-86859 17KX	CY7C166AL-35KMB	24 CP	K73	16K x 4 SRAM W/OE
5962-86859 17LX	CY7C166AL-35DMB	24.3 DIP	D14	16K x 4 SRAM W/OE
5962-86859 17UX	CY7C166AL-35LMB	28 R LCC	L54	16K x 4 SRAM W/OE
5962-86859 17XX	CY7C166AL-35LMB	28 R TLCC	L54	16K x 4 SRAM W/OE
5962-86859 18KX	CY7C166A-35KMB	24 CP	K73	16K x 4 SRAM W/OE
5962-86859 18LX	CY7C166A-35DMB	24.3 DIP	D14	16K x 4 SRAM W/OE
5962-86859 18UX	CY7C166A-35LMB	28 R LCC	L54	16K x 4 SRAM W/OE
5962-86859 18XX	CY7C166A-35LMB	28 R TLCC	L54	16K x 4 SRAM W/OE
5962-86859 21KX	CY7C164AL-45KMB	24 CP	K73	16K x 4 SRAM
5962-86859 21YX	CY7C164AL-45DMB	22.3 DIP	D10	16K x 4 SRAM
5962-86859 21ZX	CY7C164AL-45LMB	22 R LCC	L52	16K x 4 SRAM
5962-86859 22KX	CY7C164A-45KMB	24 CP	K73	16K x 4 SRAM
5962-86859 22YX	CY7C164A-45DMB	22.3 DIP	D10	16K x 4 SRAM
5962-86859 22ZX	CY7C164A-45LMB	22 R LCC	L52	16K x 4 SRAM
5962-86859 23KX	CY7C164AL-35KMB	24 CP	K73	16K x 4 SRAM
5962-86859 23YX	CY7C164AL-35DMB	22.3 DIP	D10	16K x 4 SRAM
5962-86859 23ZX	CY7C164AL-35LMB	22 R LCC	L52	16K x 4 SRAM
5962-86859 24KX	CY7C164A-35KMB	24 CP	K73	16K x 4 SRAM
5962-86859 24YX	CY7C164A-35DMB	22.3 DIP	D10	16K x 4 SRAM
5962-86859 24ZX	CY7C164A-35LMB	22 R LCC	L52	16K x 4 SRAM
5962-86873 01XX	CY7C516-42DMB	64 DIP	D30	16 x 16 Multiplier
5962-86873 01YX	CY7C516-42LMB	68 S LCC	L81	16 x 16 Multiplier
5962-86873 01ZX	CY7C516-42GMB	68 PGA	G68	16 x 16 Multiplier
5962-86873 01UX	CY7C516-42FMB	64 Q FP	F90	16 x 16 Multiplier
5962-86873 02XX	CY7C516-55DMB	64 DIP	D30	16 x 16 Multiplier
5962-86873 02YX	CY7C516-55LMB	68 S LCC	L81	16 x 16 Multiplier
5962-86873 02ZX	CY7C516-55GMB	68 PGA	G68	16 x 16 Multiplier
5962-86873 02UX	CY7C516-55FMB	64 Q FP	F90	16 x 16 Multiplier
5962-86873 03XX	CY7C516-75DMB	64 DIP	D30	16 x 16 Multiplier
5962-86873 03YX	CY7C516-75LMB	68 S LCC	L81	16 x 16 Multiplier
5962-86873 03ZX	CY7C516-75GMB	68 PGA	G68	16 x 16 Multiplier
5962-86873 03UX	CY7C516-75FMB	64 Q FP	F90	16 x 16 Multiplier
5962-86875 03XX	CY7C130-55DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 03YX	CY7C130-55LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962-86875 03ZX	CY7C131-55LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 04XX	CY7C130-45DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 04YX	CY7C130-45LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962-86875 04ZX	CY7C131-45LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 11XX	CY7C140-55DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 11YX	CY7C140-55LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962-86875 11ZX	CY7C141-55LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 12XX	CY7C140-45DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 12YX	CY7C140-45LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962-86875 12ZX	CY7C141-45LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 17XX	CY7C130-35DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 17YX	CY7C130-35LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962-86875 17ZX	CY7C131-35LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-86875 18XX	CY7C140-35DMB	48.6 DIP	D26	1K x 8 Dual-Port SRAM
5962-86875 18YX	CY7C140-35LMB	48 LCC	L68	1K x 8 Dual-Port SRAM
5962-86875 18ZX	CY7C141-35LMB	52 LCC	L69	1K x 8 Dual-Port SRAM
5962-87515 05KX	CY7C261-45TMB	24 CP	T73	8K X 8 UV EPROM

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962-87515 05LX	CY7C261-45WMB	24.3 DIP	W14	8K X 8 UV EPROM
5962-87515 053X	CY7C261-45QMB	28 S LCC	Q64	8K X 8 UV EPROM
5962-87515 06KX	CY7C261-55TMB	24 CP	T73	8K X 8 UV EPROM
5962-87515 06LX	CY7C261-55WMB	24.3 DIP	W14	8K X 8 UV EPROM
5962-87515 063X	CY7C261-55QMB	28 S LCC	Q64	8K X 8 UV EPROM
5962-87529 01KX	CY7C245-45TMB	24 CP	T73	2K x 8 Registered UV PROM
5962-87529 01LX	CY7C245-45WMB	24.3 DIP	W14	2K x 8 Registered UV PROM
5962-87529 013X	CY7C245-45QMB	28 S LCC	Q64	2K x 8 Registered UV PROM
5962-87529 02KX	CY7C245-35TMB	24 CP	T73	2K x 8 Registered UV PROM
5962-87529 02LX	CY7C245-35WMB	24.3 DIP	W14	2K x 8 Registered UV PROM
5962-87529 023X	CY7C245-35QMB	28 S LCC	Q64	2K x 8 Registered UV PROM
5962-87539 01KX	PALC22V10-25TMB	24 CP	T73	24-Pin CMOS UV E PLD
5962-87539 01LX	PALC22V10-25WMB	24.3 DIP	W14	24-Pin CMOS UV E PLD
5962-87539 013X	PALC22V10-25QMB	28 S LCC	Q64	24-Pin CMOS UV E PLD
5962-87539 02KX	PALC22V10-30TMB	24 CP	T73	24-Pin CMOS UV E PLD
5962-87539 02LX	PALC22V10-30WMB	24.3 DIP	W14	24-Pin CMOS UV E PLD
5962-87539 023X	PALC22V10-30QMB	28 S LCC	Q64	24-Pin CMOS UV E PLD
5962-87539 03KX	PALC22V10-40TMB	24 CP	T73	24-Pin CMOS UV E PLD
5962-87539 03LX	PALC22V10-40WMB	24.3 DIP	W14	24-Pin CMOS UV E PLD
5962-87539 033X	PALC22V10-40QMB	28 S LCC	Q64	24-Pin CMOS UV E PLD
5962-87650 01KX	CY7C291-50TMB	24 CP	T73	2K x 8 UV EPROM
5962-87650 01LX	CY7C291-50WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962-87650 013X	CY7C291-50QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962-87650 03KX	CY7C291-35TMB	24 CP	T73	2K x 8 UV EPROM
5962-87650 03LX	CY7C291-35WMB	24.3 DIP	W14	2K x 8 UV EPROM
5962-87650 033X	CY7C291-35QMB	28 S LCC	Q64	2K x 8 UV EPROM
5962-87651 01JX	CY7C282-45DMB	24.6 DIP	D12	1K x 8 PROM
5962-87651 01KX	CY7C281-45KMB	24 CP	K73	1K x 8 PROM
5962-87651 01LX	CY7C281-45DMB	24.3 DIP	D14	1K x 8 PROM
5962-87651 013X	CY7C281-45LMB	28 S LCC	L64	1K x 8 PROM
5962-87686 01XX	CY7C517-42DMB	64 DIP	D30	16 x 16 Multiplier
5962-87686 01YX	CY7C517-42LMB	68 S LCC	L81	16 x 16 Multiplier
5962-87686 01ZX	CY7C517-42GMB	68 PGA	G68	16 x 16 Multiplier
5962-87686 01UX	CY7C517-42FMB	64 Q FP	F90	16 x 16 Multiplier
5962-87686 02XX	CY7C517-55DMB	64 DIP	D30	16 x 16 Multiplier
5962-87686 02YX	CY7C517-55LMB	68 S LCC	L81	16 x 16 Multiplier
5962-87686 02ZX	CY7C517-55GMB	68 PGA	G68	16 x 16 Multiplier
5962-87686 02UX	CY7C517-55FMB	64 Q FP	F90	16 x 16 Multiplier
5962-87686 03XX	CY7C517-75DMB	64 DIP	D30	16 x 16 Multiplier
5962-87686 03YX	CY7C517-75LMB	68 S LCC	L81	16 x 16 Multiplier
5962-87686 03ZX	CY7C517-75GMB	68 PGA	G68	16 x 16 Multiplier
5962-87686 03UX	CY7C517-75FMB	64 Q FP	F90	16 x 16 Multiplier
5962-87708 01QX	CY2910ADMB	40.6 DIP	D18	Microprogram Controller
5962-87708 01UX	CY2910ALMB	44 LCC	L67	Microprogram Controller
5962-87708 04QX	CY7C910-51DMB	40.6 DIP	D18	Microprogram Controller
5962-87708 04UX	CY7C910-51LMB	44 LCC	L67	Microprogram Controller
5962-87708 05QX	CY7C910-46DMB	40.6 DIP	D18	Microprogram Controller
5962-87708 05UX	CY7C910-46LMB	44 LCC	L67	Microprogram Controller
5962-88518 01LX	CY7C225-30DMB	24.3 DIP	D14	512 x 8 Registered PROM
5962-88518 013X	CY7C225-30LMB	28 S LCC	L64	512 x 8 Registered PROM
5962-88518 02LX	CY7C225-35DMB	24.3 DIP	D14	512 x 8 Registered PROM
5962-88518 023X	CY7C225-35LMB	28 S LCC	L64	512 x 8 Registered PROM
5962-88518 03LX	CY7C225-40DMB	24.3 DIP	D14	512 x 8 Registered PROM
5962-88518 033X	CY7C225-40LMB	28 S LCC	L64	512 x 8 Registered PROM
5962-88535 01QX	CY7C901-32DMB	40.6 DIP	D18	4-Bit Slice
5962-88535 01XX	CY7C901-32LMB	44 LCC	L67	4-Bit Slice
5962-88535 01YX	CY7C901-32FMB	42 FP	F76	4-Bit Slice
5962-88535 02QX	CY7C901-27DMB	40.6 DIP	D18	4-Bit Slice
5962-88535 02XX	CY7C901-27LMB	44 LCC	L67	4-Bit Slice

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962-88535 02YX	CY7C901-27FMB	42 FP	F76	4-Bit Slice
5962-88587 01VX	CY7C147-45DMB	18.3 DIP	D4	4K x 1 SRAM
5962-88587 01XX	CY7C147-45KMB	18 CP	K70	4K x 1 SRAM
5962-88587 01YX	CY7C147-45LMB	18 R LCC	L50	4K x 1 SRAM
5962-88587 02VX	CY7C147-35DMB	18.3 DIP	D4	4K x 1 SRAM
5962-88587 02XX	CY7C147-35KMB	18 CP	K70	4K x 1 SRAM
5962-88587 02YX	CY7C147-35LMB	18 R LCC	L50	4K x 1 SRAM
5962-88588 01KX	CY7C150-35KMB	24 CP	K73	1K x 4 SRAM with Reset
5962-88588 01LX	CY7C150-35DMB	24.3 DIP	D14	1K x 4 SRAM with Reset
5962-88588 01XX	CY7C150-35LMB	28 R LCC	L54	1K x 4 SRAM with Reset
5962-88588 02KX	CY7C150-25KMB	24 CP	K73	1K x 4 SRAM with Reset
5962-88588 02LX	CY7C150-25DMB	24.3 DIP	D14	1K x 4 SRAM with Reset
5962-88588 02XX	CY7C150-25LMB	28 R LCC	L54	1K x 4 SRAM with Reset
5962-88588 03KX	CY7C150-15KMB	24 CP	K73	1K x 4 SRAM with Reset
5962-88588 03LX	CY7C150-15DMB	24.3 DIP	D14	1K x 4 SRAM with Reset
5962-88588 03XX	CY7C150-15LMB	28 R LCC	L54	1K x 4 SRAM with Reset
5962-88594 02WX	CY7C122-35DMB	22.4 DIP	D8	256 x 4 SRAM
5962-88594 02KX	CY7C122-35KMB	24 CP	K73	256 x 4 SRAM
5962-88594 03WX	CY7C122-25DMB	22.4 DIP	D8	256 x 4 SRAM
5962-88594 03KX	CY7C122-25KMB	24 CP	K73	256 x 4 SRAM
5962-88612 01XX	CY7C9116-99DMB	52.8 DIP	D28	16-Bit Microprogrammed ALU
5962-88612 01YX	CY7C9116-99FMB	64 FP	F90	16-Bit Microprogrammed ALU
5962-88612 01UX	CY7C9116-99LMB	52 S LCC	L69	16-Bit Microprogrammed ALU
5962-88612 02XX	CY7C9116-75DMB	52.8 DIP	D28	16-Bit Microprogrammed ALU
5962-88612 02YX	CY7C9116-75FMB	64 FP	F90	16-Bit Microprogrammed ALU
5962-88612 02UX	CY7C9116-75LMB	52 S LCC	L69	16-Bit Microprogrammed ALU
5962-88612 03XX	CY7C9116-65DMB	52.8 DIP	D28	16-Bit Microprogrammed ALU
5962-88612 03YX	CY7C9116-65FMB	64 FP	F90	16-Bit Microprogrammed ALU
5962-88612 03UX	CY7C9116-65LMB	52 S LCC	L69	16-Bit Microprogrammed ALU
5962-88612 04XX	CY7C9116-40DMB	52.8 DIP	D28	16-Bit Microprogrammed ALU
5962-88612 04YX	CY7C9116-40FMB	64 FP	F90	16-Bit Microprogrammed ALU
5962-88612 04UX	CY7C9116-40LMB	52 S LCC	L69	16-Bit Microprogrammed ALU
5962-88636 01KX	CY7C235-40KMB	24 CP	K73	1K x 8 Registered PROM
5962-88636 01LX	CY7C235-40DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962-88636 013X	CY7C235-40LMB	28 S LCC	L64	1K x 8 Registered PROM
5962-88636 02KX	CY7C235-30KMB	24 CP	K73	1K x 8 Registered PROM
5962-88636 02LX	CY7C235-30DMB	24.3 DIP	D14	1K x 8 Registered PROM
5962-88636 023X	CY7C235-30LMB	28 S LCC	L64	1K x 8 Registered PROM
5962-88637 01KX	PLDC20G10-40KMB	24 CP	K73	Generic CMOS PLD
5962-88637 01LX	PLDC20G10-40DMB	24.3 DIP	D14	Generic CMOS PLD
5962-88637 013X	PLDC20G10-40LMB	28 S LCC	L64	Generic CMOS PLD
5962-88637 02KX	PLDC20G10-30KMB	24 CP	K73	Generic CMOS PLD
5962-88637 02LX	PLDC20G10-30DMB	24.3 DIP	D14	Generic CMOS PLD
5962-88637 023X	PLDC20G10-30LMB	28 S LCC	L64	Generic CMOS PLD
5962-88662 03UX	CY7C199-55LMB	28 R LCC	L54	32K x 8 SRAM
5962-88662 03XX	CY7C198-55DMB	28.6 DIP	D16	32K x 8 SRAM
5962-88662 03YX	CY7C198-55LMB	32 R LCC	L55	32K x 8 SRAM
5962-88662 04UX	CY7C199-45LMB	28 R LCC	L54	32K x 8 SRAM
5962-88662 04XX	CY7C198-45DMB	28.6 DIP	D16	32K x 8 SRAM
5962-88662 04YX	CY7C198-45LMB	32 R LCC	L55	32K x 8 SRAM
5962-88669 02UX	CY7C429-65KMB	28 CP	K74	2K x 9 FIFO
5962-88669 02XX	CY7C428-65DMB	28.6 DIP	D16	2K x 9 FIFO
5962-88669 02YX	CY7C429-65DMB	28.3 DIP	D22	2K x 9 FIFO
5962-88669 02ZX	CY7C429-65LMB	32 R LCC	L55	2K x 9 FIFO
5962-88669 04UX	CY7C429-40KMB	28 CP	K74	2K x 9 FIFO
5962-88669 04XX	CY7C428-40DMB	28.6 DIP	D16	2K x 9 FIFO
5962-88669 04YX	CY7C429-40DMB	28.3 DIP	D22	2K x 9 FIFO
5962-88669 04ZX	CY7C429-40LMB	32 R LCC	L55	2K x 9 FIFO
5962-88669 05UX	CY7C429-30KMB	28 CP	K74	2K x 9 FIFO

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962-88669 05XX	CY7C428-30DMB	28.6 DIP	D16	2K x 9 FIFO
5962-88669 05YX	CY7C429-30DMB	28.3 DIP	D22	2K x 9 FIFO
5962-88669 05ZX	CY7C429-30LMB	32 R LCC	L55	2K x 9 FIFO
5962-88670 01KX	PALC22V10-25KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 01LX	PALC22V10-25DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 013X	PALC22V10-25LMB	28 S LCC	L64	24-Pin CMOS PLD
5962-88670 02KX	PALC22V10-30KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 02LX	PALC22V10-30DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 023X	PALC22V10-30LMB	28 S LCC	L64	24-Pin CMOS PLD
5962-88670 03KX	PALC22V10-40KMB	24 CP	K73	24-Pin CMOS PLD
5962-88670 03LX	PALC22V10-40DMB	24.3 DIP	D14	24-Pin CMOS PLD
5962-88670 033X	PALC22V10-40LMB	28 S LCC	L64	24-Pin CMOS PLD
5962-88678 01RX	PALC16L8-40WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 01XX	PALC16L8-40QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 02RX	PALC16R8-40WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 02XX	PALC16R8-40QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 03RX	PALC16R6-40WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 03XX	PALC16R6-40QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 04RX	PALC16R4-40WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 04XX	PALC16R4-40QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 05RX	PALC16L8-30WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 05XX	PALC16L8-30QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 06RX	PALC16R8-30WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 06XX	PALC16R8-30QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 07RX	PALC16R6-30WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 07XX	PALC16R6-30QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 08RX	PALC16R4-30WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 08XX	PALC16R4-30QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 09RX	PALC16L8-20WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 09XX	PALC16L8-20QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 10RX	PALC16R8-20WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 10XX	PALC16R8-20QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 11RX	PALC16R6-20WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 11XX	PALC16R6-20QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88678 12RX	PALC16R4-20WMB	20.3 DIP	W6	20-Pin CMOS UV E PLD
5962-88678 12XX	PALC16R4-20QMB	20 S LCC	Q61	20-Pin CMOS UV E PLD
5962-88681 01LX	CY7C194-35DMB	24.3 DIP	D14	64K x 4 SRAM
5962-88681 01XX	CY7C194-35LMB	28 R LCC	L54	64K x 4 SRAM
5962-88681 02LX	CY7C194-45DMB	24.3 DIP	D14	64K x 4 SRAM
5962-88681 02XX	CY7C194-45LMB	28 R LCC	L54	64K x 4 SRAM
5962-88713 01RX	PALC16L8-40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 01SX	PALC16L8-40KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 01XX	PALC16L8-40LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 02RX	PALC16R8-40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 02SX	PALC16R8-40KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 02XX	PALC16R8-40LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 03RX	PALC16R6-40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 03SX	PALC16R6-40KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 03XX	PALC16R6-40LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 04RX	PALC16R4-40DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 04SX	PALC16R4-40KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 04XX	PALC16R4-40LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 05RX	PALC16L8-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 05SX	PALC16L8-30KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 05XX	PALC16L8-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 06RX	PALC16R8-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 06SX	PALC16R8-30KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 06XX	PALC16R8-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 07RX	PALC16R6-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 07SX	PALC16R6-30KMB	20 CP	K71	20-Pin CMOS PLD

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3]		Product Description
		Description	Type	
5962-88713 07XX	PALC16R6-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 08RX	PALC16R4-30DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 08SX	PALC16R4-30KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 08XX	PALC16R4-30LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 09RX	PALC16L8-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 09SX	PALC16L8-20KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 09XX	PALC16L8-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 10RX	PALC16R8-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 10SX	PALC16R8-20KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 10XX	PALC16R8-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 11RX	PALC16R6-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 11SX	PALC16R6-20KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 11XX	PALC16R6-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88713 12RX	PALC16R4-20DMB	20.3 DIP	D6	20-Pin CMOS PLD
5962-88713 12SX	PALC16R4-20KMB	20 CP	K71	20-Pin CMOS PLD
5962-88713 12XX	PALC16R4-20LMB	20 S LCC	L61	20-Pin CMOS PLD
5962-88725 01LX	CY7C197-35DMB	24.3 DIP	D14	256K x 1 SRAM
5962-88725 01XX	CY7C197-35LMB	28 R LCC	L54	256K x 1 SRAM
5962-88725 02LX	CY7C197-45DMB	24.3 DIP	D14	256K x 1 SRAM
5962-88725 02XX	CY7C197-45LMB	28 R LCC	L54	256K x 1 SRAM
5962-88733 01XX	CY7C510-55DMB	64 DIP	D30	16 x 16 MAC
5962-88733 01YX	CY7C510-55LMB	68 S LCC	L81	16 x 16 MAC
5962-88733 01ZX	CY7C510-55GMB	68 PGA	G68	16 x 16 MAC
5962-88733 02XX	CY7C510-65DMB	64 DIP	D30	16 x 16 MAC
5962-88733 02YX	CY7C510-65LMB	68 S LCC	L81	16 x 16 MAC
5962-88733 02ZX	CY7C510-65GMB	68 PGA	G68	16 x 16 MAC
5962-88733 03XX	CY7C510-75DMB	64 DIP	D30	16 x 16 MAC
5962-88733 03YX	CY7C510-75LMB	68 S LCC	L81	16 x 16 MAC
5962-88733 03ZX	CY7C510-75GMB	68 PGA	G68	16 x 16 MAC
5962-88734 02JX	CY7C292A-45DMB	24.6 DIP	D12	2K x 8 EPROM
5962-88734 02KX	CY7C291A-45KMB	24 CP	K73	2K x 8 EPROM
5962-88734 02LX	CY7C291A-45DMB	24.3 DIP	D14	2K x 8 EPROM
5962-88734 023X	CY7C291A-45LMB	28 S LCC	L64	2K x 8 EPROM
5962-88734 03JX	CY7C292A-35DMB	24.6 DIP	D12	2K x 8 EPROM
5962-88734 03KX	CY7C291A-35KMB	24 CP	K73	2K x 8 EPROM
5962-88734 03LX	CY7C291A-35DMB	24.3 DIP	D14	2K x 8 EPROM
5962-88734 033X	CY7C291A-35LMB	28 S LCC	L64	2K x 8 EPROM
5962-88734 04JX	CY7C292A-25DMB	24.6 DIP	D12	2K x 8 EPROM
5962-88734 04KX	CY7C291A-25KMB	24 CP	K73	2K x 8 EPROM
5962-88734 04LX	CY7C291A-25DMB	24.3 DIP	D14	2K x 8 EPROM
5962-88734 043X	CY7C291A-25LMB	28 S LCC	L64	2K x 8 EPROM
5962-88735 01KX	CY7C245-45KMB	24 CP	K73	2K x 8 Registered PROM
5962-88735 01LX	CY7C245-45DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962-88735 013X	CY7C245-45LMB	28 S LCC	L64	2K x 8 Registered PROM
5962-88735 02KX	CY7C245-35KMB	24 CP	K73	2K x 8 Registered PROM
5962-88735 02LX	CY7C245-35DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962-88735 023X	CY7C245-35LMB	28 S LCC	L64	2K x 8 Registered PROM
5962-88735 03KX	CY7C245A-35KMB	24 CP	K73	2K x 8 Registered PROM
5962-88735 03LX	CY7C245A-35DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962-88735 033X	CY7C245A-35LMB	28 S LCC	L64	2K x 8 Registered PROM
5962-88735 04KX	CY7C245A-25KMB	24 CP	K73	2K x 8 Registered PROM
5962-88735 04LX	CY7C245A-25DMB	24.3 DIP	D14	2K x 8 Registered PROM
5962-88735 043X	CY7C245A-25LMB	28 S LCC	L64	2K x 8 Registered PROM
5962-89517 01XX	CY7C9101-45DMB	64 DIP	D30	16-Bit Slice
5962-89517 01YX	CY7C9101-45LMB	68 S LCC	L81	16-Bit Slice
5962-89517 01ZX	CY7C9101-45GMB	68 PGA	G68	16-Bit Slice
5962-89517 01UX	CY7C9101-45FMB	64 Q FP	F90	16-Bit Slice
5962-89517 02XX	CY7C9101-35DMB	64 DIP	D30	16-Bit Slice
5962-89517 02YX	CY7C9101-35LMB	68 S LCC	L81	16-Bit Slice
5962-89517 02ZX	CY7C9101-35GMB	68 PGA	G68	16-Bit Slice

DESC SMD (Standardized Military Drawing) Approvals[1] (continued)

SMD Number	Cypress[2] Part Number	Package[3] Description	Package[3] Type	Product Description
5962-89517 02UX	CY7C9101-35FMB	64 Q FP	F90	16-Bit Slice
5962-89537 01UX	CY7C251-65QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962-89537 01YX	CY7C251-65WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962-89537 01ZX	CY7C251-65TMB	28 CP	T74	16K x 8 UV EPROM
5962-89537 02UX	CY7C251-55QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962-89537 02YX	CY7C251-55WMB	28.3 DIP	W22	16K x 8 UV EPROM
5962-89537 02ZX	CY7C251-55TMB	28 CP	T74	16K x 8 UV EPROM
5962-89538 01UX	CY7C254-65QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962-89538 01XX	CY7C254-65WMB	28.6 DIP	W16	16K x 8 UV EPROM
5962-89538 01ZX	CY7C254-65TMB	28 CP	T74	16K x 8 UV EPROM
5962-89538 02UX	CY7C254-55QMB	32 R LCC	Q55	16K x 8 UV EPROM
5962-89538 02XX	CY7C254-55WMB	28.6 DIP	W16	16K x 8 UV EPROM
5962-89538 02ZX	CY7C254-55TMB	28 CP	T74	16K x 8 UV EPROM
5962-89546 01XX	CY7C330-28WMB	28.3 DIP	W22	PLD State Machine
5962-89546 01YX	CY7C330-28TMB	28 CP	T74	PLD State Machine
5962-89546 013X	CY7C330-28QMB	28 S LCC	Q64	PLD State Machine
5962-89546 02XX	CY7C330-40WMB	28.3 DIP	W22	PLD State Machine
5962-89546 02YX	CY7C330-40TMB	28 CP	T74	PLD State Machine
5962-89546 023X	CY7C330-40QMB	28 S LCC	Q64	PLD State Machine
5962-89546 03XX	CY7C330-50WMB	28.3 DIP	W22	PLD State Machine
5962-89546 03YX	CY7C330-50TMB	28 CP	T74	PLD State Machine
5962-89546 033X	CY7C330-50QMB	28 S LCC	Q64	PLD State Machine
5962-89661 01XX	CY7C409A-15DMB	28.3 DIP	D22	64 x 9 FIFO
5962-89661 01YX	CY7C409A-15KMB	28 CP	K74	64 x 9 FIFO
5962-89661 013X	CY7C409A-15LMB	28 S LCC	L64	64 x 9 FIFO
5962-89661 02XX	CY7C409A-25DMB	28.3 DIP	D22	64 x 9 FIFO
5962-89661 02YX	CY7C409A-25KMB	28 CP	K74	64 x 9 FIFO
5962-89661 023X	CY7C409A-25LMB	28 S LCC	L64	64 x 9 FIFO
5962-89664 01XX	CY7C408A-15DMB	28.3 DIP	D22	64 x 8 FIFO
5962-89664 01YX	CY7C408A-15KMB	28 CP	K74	64 x 8 FIFO
5962-89664 013X	CY7C408A-15LMB	28 S LCC	L64	64 x 8 FIFO
5962-89664 02XX	CY7C408A-25DMB	28.3 DIP	D22	64 x 8 FIFO
5962-89664 02YX	CY7C408A-25KMB	28 CP	K74	64 x 8 FIFO
5962-89664 023X	CY7C408A-25LMB	28 S LCC	L64	64 x 8 FIFO
5962-89690 01JX	CY6116A-25DMB	24.6 DIP	D12	2K x 8 SRAM
5962-89690 01KX	CY7C128A-25KMB	24 CP	K73	2K x 8 SRAM
5962-89690 01LX	CY7C128A-25DMB	24.3 DIP	D14	2K x 8 SRAM
5962-89690 01XX	CY6117A-25LMB	32 R LCC	L55	2K x 8 SRAM
5962-89690 01YX	CY7C128A-25LMB	24 R LCC	L53	2K x 8 SRAM
5962-89690 013X	CY6116A-25LMB	28 S LCC	L64	2K x 8 SRAM
5962-89690 02JX	CY6116A-20DMB	24.6 DIP	D12	2K x 8 SRAM
5962-89690 02KX	CY7C128A-20KMB	24 CP	K73	2K x 8 SRAM
5962-89690 02LX	CY7C128A-20DMB	24.3 DIP	D14	2K x 8 SRAM
5962-89690 02XX	CY6117A-20LMB	32 R LCC	L55	2K x 8 SRAM
5962-89690 02YX	CY7C128A-20LMB	24 R LCC	L53	2K x 8 SRAM
5962-89690 023X	CY6116A-20LMB	28 S LCC	L64	2K x 8 SRAM
5962-89694 01EX	CY7C190-25DMB	16.3 DIP	D2	16K x 4 SRAM
5962-89694 01FX	CY7C190-25KMB	16 CP	K69	16K x 4 SRAM
5962-89694 01XX	CY7C190-25LMB	20 S LCC	L61	16K x 4 SRAM

Notes:

1. SMD approvals are continually being updated. Contact your local Cypress representative for the latest update.
2. Use the SMD part number as the ordering code.
3. Package: 24.3 DIP = 24-pin 0.300" DIP;
   24.6 DIP = 24-pin 0.600" DIP
   28 R LCC = 28 terminal rectangular LCC;
   S = Square LCC; TLCC = Thin LCC
   24 CP = 24-pin ceramic flatpack (Configuration 1);
   FP = brazed flatpack
   PGA = Pin Grid Array

SMD Ordering Information

5962–8XXXX 01 L X

- LEAD FINISH
  - A = Solder Dip
  - B = Tin Plate
  - C = Gold
  - X = Don't Care (The letter "X" will not be marked on the device, but will be replaced with the actual lead finish designation.)
- PACKAGE TYPE (Not a complete list)
  - V = 18-pin 0.300 DIP
  - R = 20-pin 0.300 DIP
  - S = 20-pin Cerpack
  - W = 22-pin 0.400 DIP
  - L = 24-pin 0.300 DIP
  - J = 24-pin 0.600 DIP
  - Q = 40-pin 0.600 DIP
  - K = 24-pin Cerpack
  - 2 = 20-pin SQ LCC
  - 3 = 28-pin SQ LCC

  X, Y, Z, U, T, N = Non-dedicated package designations and will vary per drawing.
- DEVICE TYPE
- DRAWING NUMBER
- DRAWING PREFIX
  5962 = Federal Stock Code (FSC) for microcircuits. Pre-1985 drawings do not have this prefix.

10

Section Contents

BridgeMOS **Page Number**

CYPRESS SEMICONDUCTOR

BridgeMOS

Features

- **May be driven by CMOS or TTL**
- **Drives fully loaded TTL**
  - **Inputs switch at 1.5V**
- **Can drive CMOS to full input levels**
  - **V_{OL} = 0.2V at I_{OL} = 20 μA**
  - **V_{OH} = 0.9 V_{CC} at I_{OH} = –20 μA**
- **SRAM, PROM, LOGIC**
- **2.0V (V_{CC}) data retention on all devices**

Overview

The BridgeMOS® product line from Cypress Semiconductor provides an electrical bridge between CMOS and TTL or TTL and CMOS devices. BridgeMOS devices may be driven by either TTL or CMOS devices and in turn can drive either fully loaded TTL or CMOS to full input levels. As a result, any combination of TTL and/or CMOS may be interfaced to Cypress BridgeMOS products.

All devices in the BridgeMOS product line are specified at a 2.0V (V_{CC}) standby mode of operation. This allows the device to be powered at 2.0 volts and maintain the integrity of the data in any volatile storage element.

The output drivers in the 7CXXX Cypress products are designed for TTL signals and pull-up to 2.4 volts. For BridgeMOS, Cypress has designed an output driver that boosts the output voltage sufficiently to drive the inputs of a device to greater than 3.85 volts, thus guaranteeing that the input converter will draw minimum power. The output drivers source 20 microamps at their rated BridgeMOS levels. They will also source and drive normal TTL loads. Therefore, they are capable of driving other non-BridgeMOS loads and normal TTL loads at the same time.

Although the TTL to CMOS input converters power down as described above, they switch at TTL levels and all timing is referenced to 1.5 volts. The device will operate at normal TTL levels with no AC performance degradation.

CY8C150 Selection Guide

		8C150-15	8C150-25	8C150-35
Maximum Access Time (ns)	Commercial	15	25	35
	Military		25	35
Maximum Operating Current (mA)	Commercial	100	100	100
	Military		125	125

CY8C245 Selection Guide

		8C245-35	8C245-45
Maximum Access Time (ns)		35	50
Maximum Operating Current (mA)	Commerical	45	45
	Military	80	80

CY8C291 Selection Guide

		8C291-35	8C291-50
Maximum Access Time (ns)		35	50
Maximum Operating Current (mA)	Commerical	45	45
	Military	80	80

CY8C901 Selection Guide

Read Modify-Write Cycle (min.) in ns	Operating ICC (max.) in mA	Operating Range	Part Number
31	26.5	Commercial	8C901-31
32	31.0	Military	8C901-32

CY8C909/8C911 Selection Guide

	8C909-30 8C911-30	8C909-40 8C911-40
Minimum Clock to Output Cycle Time (ns)	30	40
Maximum Operating Current (mA)	15	15

Section Contents

Design and Programming Tools

Page Number

CYPRESS SEMICONDUCTOR

CY3000

QuickPro®

Features

- **Combined PROM, PLD, and EPROM programmer**
- **Programs Cypress CMOS PLDs and PROMs**
- **Reads bipolar PLDs and PROMs**
- **Easy-to-use, menu-driven software**
- **New device updates via floppy disk**
- **IBM-PC® plug-in card format, external ZIP-DIP socket**
- **Compatible with the IBM PC family of computers and plug compatibles**
- **Programs 24- and 28-pin NMOS and CMOS EPROMs**
- **One long slot and 256 kbytes of memory required**
- **Designed for present and future NMOS and CMOS devices**
- **Optional LCC, PLCC, SOIC socket adapters**

Description

QuickPro is a development tool for present and future CMOS PROM and PLD devices, and is used within the IBM PC and compatible environment. Older generation bipolar PLDs and PROMs required special current and programming voltages that were difficult to generate within the IBM PC.

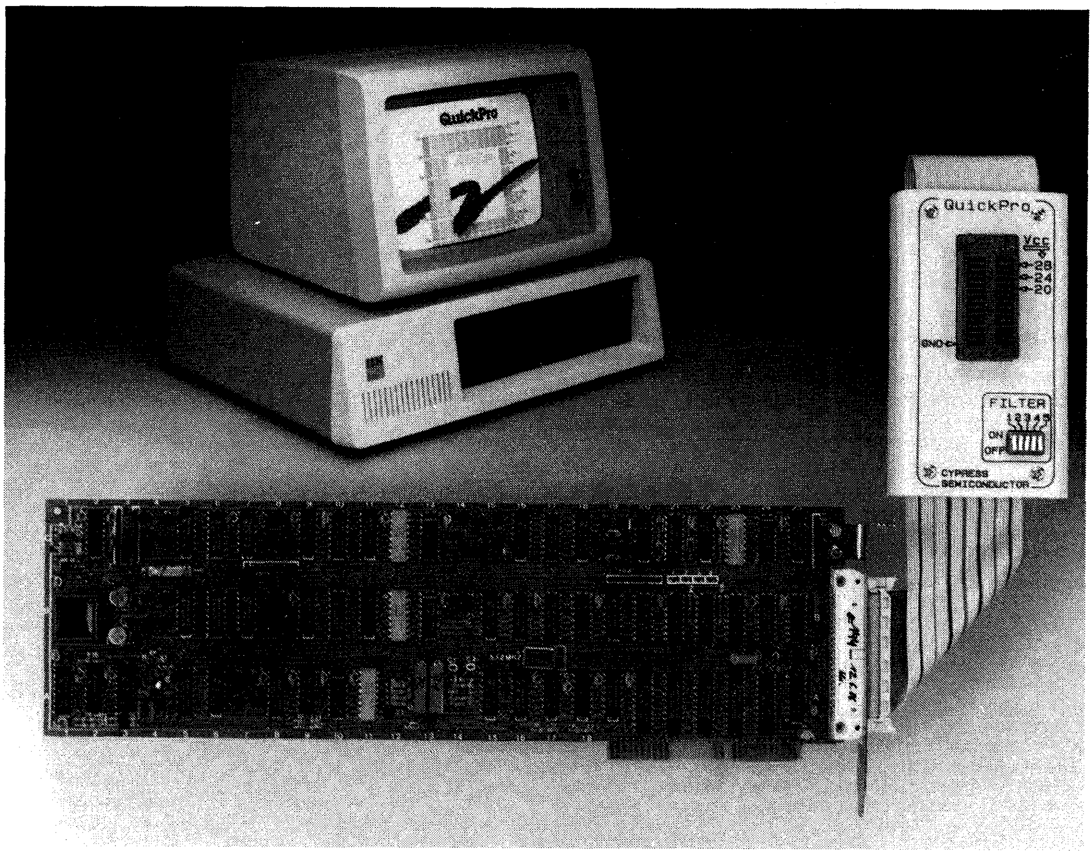
QuickPro is designed for new generations of CMOS PLDs and PROMs that obsolete the older technology and use a programming technique, which is more compatible with low cost programming methods.

QuickPro can also program standard NMOS and CMOS EPROMs in packages up to 28 pins. And QuickPro is fast; intelligent programming is used to reduce programming time to a minimum.

QuickPro is future oriented. Each I/O pin is fully programmable, allowing the parameters and timing of each device to be handled via software. As new devices become available, they will be supported by QuickPro. Updates are managed by a simple exchange of floppy disks.

QuickPro includes a comprehensive set of commands to make programming PLDs and PROMs as easy as possible.

For PLDs, QuickPro uses the JEDEC standard data format, so present and future logic design tools such as ABEL™, CUPL™, and PALASM™ can be used. Because the QuickPro add-in card plugs into your PC backplane and is driven directly by the PC software, it avoids serial download problems from a PC to a standalone programmer. For PROMs, QuickPro reads Intellec 86™, Motorola S, TEK,



12

Description (continued)

and space format files. QuickPro also reads and writes PROM PC-DOS binary files for use with assemblers and compilers. QuickPro is low cost, so each workstation can have one, eliminating the inconvenience of sharing one expensive programmer. All actions are menu-driven, with complete explanations provided on-screen, in clear text. There is no need to loop up manufacturer's codes in a table.

QuickPro Commands

Program device	Write disk file
Select device type	Verify device
Edit memory	Blank check device
Display memory	Program security fuse
Change PROM memory location	Fill memory
Read device	Convert PLD type
Test PLD device	Summary display
Read disk file	

Technical Information

Size

IBM-PC standard full length card. Selectable port addresses 300-31F, 320-33F, 340-35F, 360-37F hex.

Power

+5V	1.0 amp
+12V	1.0 amp (peak) 0.4 amp average
- 12V	0.05 amp

Socket Pod

This is the external socket for connection to the device to be programmed or read. It provides a 28-pin 300/600-mil socket for compatibility with a wide range of devices. Other adapters for leadless packages are also available. Five filter switches are located on the pod for bypass capacitors according to manufacturers' published programming specifications.

Memory

256 kbytes of total memory is sufficient to operate QuickPro.

Devices Supported

Cypress CMOS PROMs:
CY7C225, CY7C235, CY7C245, CY7C245A, CY7C251, CY7C254, CY7C261, CY7C263, CY7C264, CY7C268, CY7C269, CY7C271, CY7C274, CY7C277, CY7C279, CY7C281, CY7C282, CY7C291, CY7C291A, CY7C292, CY7C292A, CY7C293A

Cypress CMOS PLDs:
PALC16L8, PALC16R4, PALC16R6, PALC1648, PALC22V10, PLDC20G10, PLDC20RA10, CY7C330, CY7C331, CY7C332

QuickPro can read 20- and 24-pin Bipolar PLDs for conversion to Cypress PLDs.

EPROMs: (NMOS and CMOS)
2716, 2732, 2732A, 2764, 2764A, 27128, 27256, 27512

Ordering Information

CY3000	QuickPro System ($995.00) contains:
CY3001	QuickPro Board
CY3002	QuickPro Pod
CY3003	QuickPro System Disk QuickPro Manual

Optional QuickPro Package Adaptors Include:

CY3004A (CY3006A) 28-lead square (P)LCC:
PALC22V10, CG20G10

CY3004B (CY3006B) 28-lead square (P)LCC:
7C225, 7C235, 7C245, 7C261, 7C263, 7C264, 7C281, 7C282, 7C291, 7C292

CY3005 (CY3007) 20-lead square (P)LCC:
16L8, 16R4, 16R6, 16R8

CY3008 (CY3009) 28-lead square (P)LCC:
7C269, 7C271, 7C330, 7C331, 7C332

CY3010 (CY3011) 28-lead square (P)LCC:
PLDC20G10

CY3012 (CY3013) 32-lead rectangular (P)LCC:
7C268

CY3014 28-pin SOIC:
7C225, 7C235, 7C245, 7C251, 7C254, 7C261, 7C263, 7C264, 7C269, 7C271, 7C281, 7C282, 7C291, 7C292

CY3015 32-pin DIP:
7C268

CY3017 (CY3018) 32-lead square (P)LCC:
7C251, 7C254

CY3101
PLD ToolKit

CYPRESS SEMICONDUCTOR

Features

- Logic assembler, Reverse assembler
- Concise easy-to-use syntax
- JEDEC read/write capability
- Integrated waveform logic simulator
- Mouse-driven simulation editor
- Mouse, keyboard, command line interface
- CGA, EGA, VGA, Hercules support
- Supports all Cypress PLDs

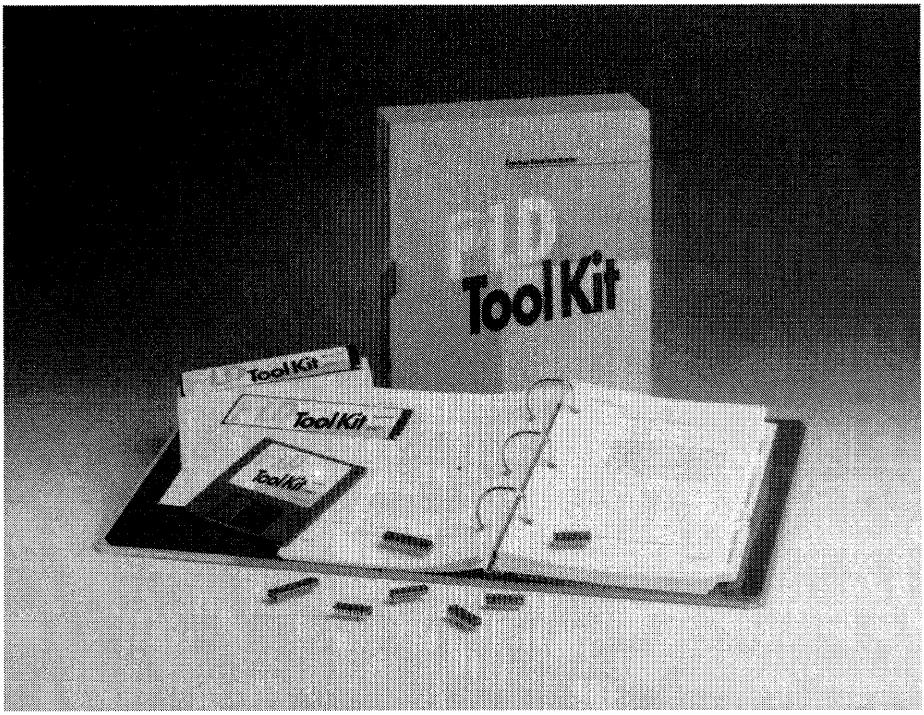
Description

The Cypress PLD ToolKit is a sophisticated programmable logic design tool that supports the Cypress family of programmable logic products. The ToolKit includes the ability to assemble a logic source file, interactively perform logic simulation on the result, and write a standard JEDEC output file for programming the PLD. In addition, JEDEC files may be read, simulated, and reverse assembled, creating source files that may be modified and reassembled.

The PLD ToolKit runs on any standard IBM PC®, AT®, 386 or compatible personal computer with a CGA, EGA, VGA, or Hercules display. The ToolKit features mouse, keyboard, or command line interface, and supports Logitech™ and Microsoft® mouse compatibility. Command line control is provided for assembly from a source file to JEDEC file or disassembly of a JEDEC file to a source file.

The language contains syntax that allows the management of programmable logic device macrocells in all possible configurations, as well as default conditions that provide concise source files. In addition, there are language constructs called connectives that provide expressions for connecting any product term to a macrocell.

The ToolKit simulator features waveform entry, multiple views and multi-segment simulation. The simulator provides the capability to specify initial design conditions, and "view nodes" may be created and used to probe internal nodes in the device.



12

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PLD ToolKit Command Menus

Command Menu

Assemble	Invokes Assembles
Disassemble	Invokes Disassembler
Write JEDEC	Writes JEDEC Output File
Read JEDEC	Reads JEDEC File into PLD ToolKit
Simulate	Invokes Simulator
Options	Selects Option Menu
Information	Selects System Information Menu
Clear	Resets ToolKit

Information

Release Number	Information about the PLD ToolKit for registration purposes
Release Date	
Serial Number	
Free Memory	
Screen Size	
Number of Colors	

Options

Simulation Colors	Selects Simulation Colors Menu
Menu Colors	Selects Menu Color Menu
JEDEC Brief/Annotate	Toggles JEDEC Annotated or Brief Listing
G Fuse (JEDEC Security): ON/OFF	Toggles Security Fuse
Working Directory Path ( )	Sets Path to Working Directory

Simulation Colors

Background	Allows the selection of colors for the Simulator Display
Input Trace	
Output Trace	
Name of Pin or Node	
Pin or Node Background	
Trace Selected	
Selected Trace Background	

Memory

512 kbytes of total memory is required to operate the PLD ToolKit.

Devices Supported

PALC16R8, PALC16R6, PALC16R4, PALC16L8, PALC22V10, PLDC20G10, CY7C330, CY7C331, CY7C332, CY7C361, CY10E301, CY100E301, CY10E302, CY100E302

Ordering Information

CY3101 Cypress PLD ToolKit Level 1 contains:

Two 5 ¼" Floppy Disks
One 3 ½" Floppy Disk
One Manual
One Registration Card

CYPRESS SEMICONDUCTOR

CY3200

PLDS-MAX+PLUS® Design System

Features

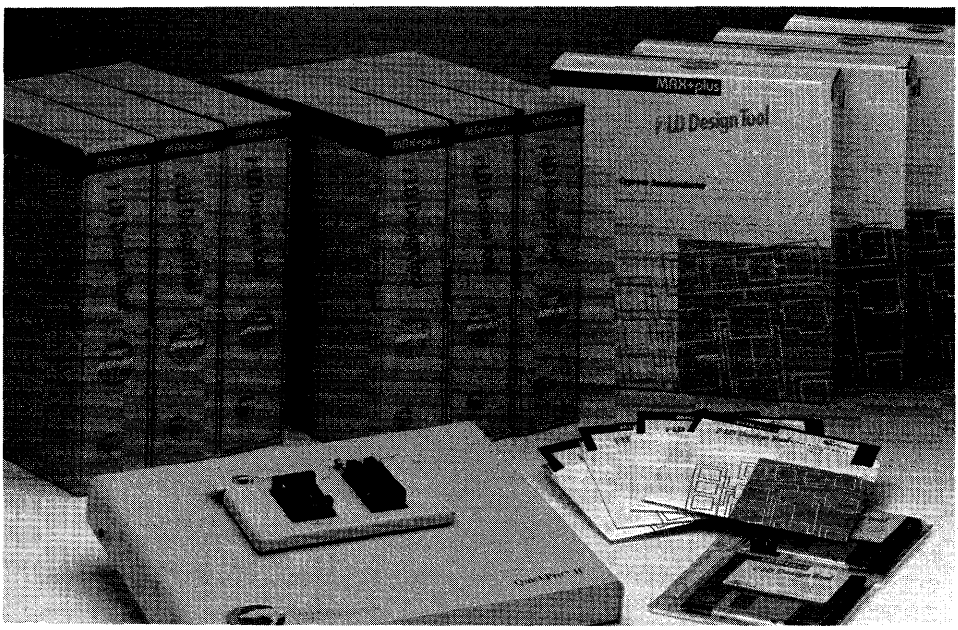
- **Fully integrated development and programming system for Multiple Array MatriX (MAX®) family of EPLDs**
- **Offers multiple modes of design entry including State Machine, Boolean Equations, and schematic capture via a Hierarchical Graphic Editor**
- **Hierarchical Graphic Editor features include:**
  - **Multiple-level schematics**
  - **User-definable macrofunctions**
  - **Library of 7400 Series TTL and special-purpose macrofunctions optimized for MAX architecture**
  - **Delay path predictor**
- **Logic Synthesis and minimization ensures quick and optimal design implementation**
- **Automatic Error Location**
- **Interractive timing simulation**
- **Graphical Waveform Editor for creating simulation stimulus and viewing simulation results**
- **Runs on IBM PC/AT®, PS/2® or compatible machines**
- **Includes the QP2-MAX® programmer for device programming**

Description

The PLDS-MAX+PLUS Development System is a complete hardware and software design environment for realizing applications in the Cypress CY7C340 family of EPLDs. It includes design entry, timing simulation, placement and routing on the target device (compiling), and device programming via the QP2-MAX programmer (MAX+PLUS version of QuickPro II® PLD programmer). Hosted on an IBM PC/AT, PS/2, or compatible machine, PLDS-MAX+PLUS gives designers all the tools they need to quickly and efficiently realize complex logic applications on Cypress MAX devices.

The MAX+PLUS software compiles designs for MAX EPLDs in a matter of minutes. Designs may be entered using any combination of a number of different design entry methods. MAX+PLUS supports hierarchical graphic entry (schematics), Boolean Equations, State Machine, and Truth Table entry methods. The Graphic Editor features include tag and drag editing, multiple windows, multiple levels of zoom and a menu-driven command structure. The Graphic Editor provides a comprehensive library of 7400 TTL logic macros, and also allows you to create your own logic macros through the use of its multiple hierarchy levels and symbol editing features. Boolean Equation, State Machine, and Truth Table entry methods may be used separately or in conjunction with the graphics entry method.

In addition to having multiple design entry methods, MAX+PLUS includes a sophisticated compiler to map logical design descriptions to MAX logical resources, place



12

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QP2-MAX and QuickPro II are trademarks of Cypress Semiconductor Corporation.

designs within physical MAX EPLDs and rout the necessary interconnect. The compiler uses advanced logic synthesis and minimization techniques in conjunction with knowledge-based fitting rules to optimally accomplish this. A programming file is created by the compiler, which can then be used by the software to program a MAX EPLD using the QP2-MAX programming hardware.

Logic simulations may be performed using a powerful event-driven timing simulator within PLDS-MAX+PLUS. This simulator interactively displays timing results in a Graphical Waveform Editor display, as well as hard-copy tabular and waveform output. The Graphical Waveform Editor allows the entry and modifications of simulator input stimulus waveforms and logical operations on pairs of waveforms. A comparison between two simulations can be performed in the Waveform Editor, and the difference between the simulations are highlighted.

Unlike most design environments, PLDS-MAX+PLUS is fully integrated with a central database used by all portions of the design process. This enables the software to provide such features as Automatic Error Location and Delay Prediction. If a design contains an error, PLDS-MAX+PLUS not only flags the error, but takes the user to the actual location of the error in the original schematic. Propagation delays of critical circuit paths may be determined in the Graphical Editor using the Delay Predictor. By simply tagging start and end nodes with the cursor, the shortest and longest timing delay is calculated.

Design Entry

PLDS-MAX+PLUS supports a variety of design entry methods. Boolean Equation entry is available for entering simple combinatorial logic and register functions. High-level language entry is also provided with State Machine and Truth Table entry methods. To provide a more classic design entry tool for larger logic circuits, a powerful Graphical Editor allows design entry through schematics.

Graphic Editor

The hierarchical design methodology supported by the Graphical Editor allows designers to work in either a top-down or a bottom-up fashion. Using the top-down method, designers start with system-level block diagrams, defining symbols for each block, and then work their way down into each block with detailed schematics. Likewise, in a bottom-up approach, designers create, simulate, and debug small blocks of logic, creating symbols for each, and then tie them all together with an upper-level system schematic.

The Graphic Editor is mouse-driven and uses pull-down menus or single keystrokes to enter commands. The display utilizes multiple windows to provide the user with a maximum amount of information. One window displays the local schematic view, another the total global circuit view, another contains the hierarchy display showing where you are currently viewing, and still other windows provide control, graphic options, and message information.

Included with the Graphic Editor is a library of popular 7400 TTL SSI/MSI macrofunctions and a collection of special macrofunctions that optimally utilize the resources available on the MAX architecture. Designers may use these macrofunctions to create their design by simply placing the library's symbols on their schematics and wiring them up, or they may create their own macrofunctions by first creating the logic schematic (or Boolean Equations or State Machine descriptions) for it and then creating a symbol using the Symbol Editor. This symbol can also be created by the software automatically. These new macrofunctions may

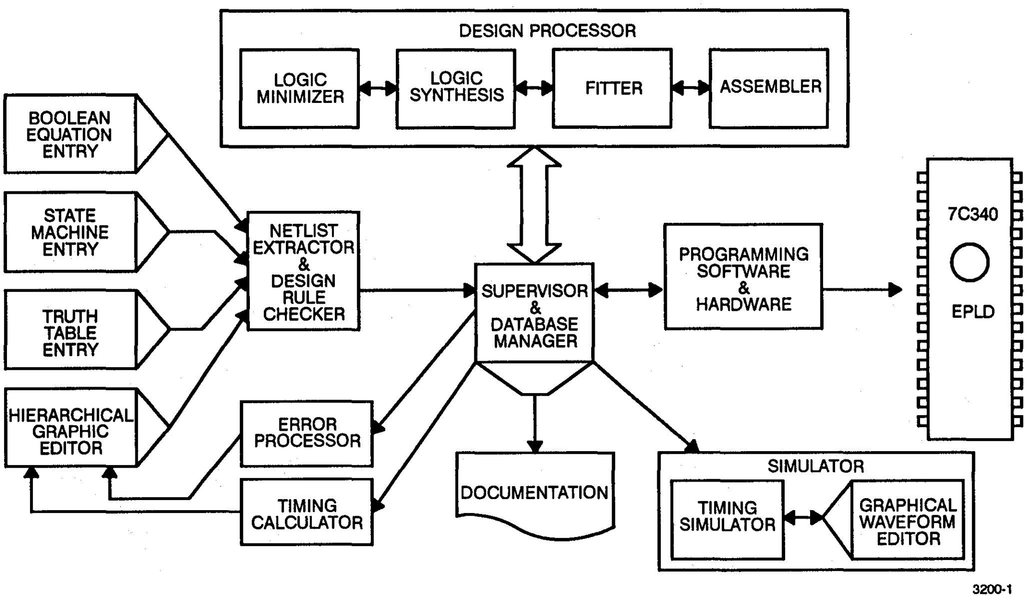


Figure 1. PLDS-MAX+PLUS Block Diagram

then be used multiple times in the current design, or saved and used in other designs.

Creating and editing schematics within the Graphical Editor environment is accomplished using advanced graphics features. Tag and drag editing is used to move individual symbols, or entire areas may be identified and moved. Lines stay connected with true orthogonal rubberbanding. This means that symbols and areas can be moved and yet the connection wires retain clean 90-degree angles as they move to maintain the connectivity of the schematic. Hardcopy of a completed design may be produced on an Epson FX compatible printer or HP plotter.

An additional feature of the hierarchical Graphic Editor is the Delay Predictor. This tool gives the designer instant feedback on propagation delays between nodes in the design. By placing probes on the starting and the ending nodes, the minimum and maximum delays are calculated for the path between the nodes and these values are displayed. This is a valuable tool for design debugging and documentation.

Design Processing

After a design has been entered, the PLDS-MAX+PLUS Compiler is invoked. This program performs several tasks on the design database under control of a variety of options. First a netlist is extracted from the hierarchical design. During the extraction process, design rules are checked for any errors, and if errors are found, the error processor leads the designer directly to the schematic location where the error occurred. Once the design compiles error-free, the extracted netlist is placed in the design database. If the design has been compiled previously, and only a portion of the design has been changed, an incremental compile may be chosen, and only the changed parts of the design will be re-extracted, decreasing the compile time.

Next, the Logic Synthesizer module operates on the design database. This program translates and optimizes the user-defined logic for the MAX architecture and resources. In this process, the logic is first minimized with any unused logic in the design being automatically removed. Using knowledge-based synthesis rules, the program then factors and maps the logic in a manner that ensures the most efficient use of silicon resources.

After Logic Synthesis, the Fitter program is invoked, which uses heuristic rules to optimally place the synthesised design within the chosen Cypress MAX device. It assigns the logical design elements to the physical MAX macros and expansion product terms. Next, it routes the interconnect signals to realize the design. If a MAX device with a Programmable Interconnect Array is used, then the software automatically makes optimal use of this resource to achieve complete signal routing. Upon completion, the fitter issues a report showing exactly how the design was realized in the device, as well as any unused resources. This information can then be used to determine if any additional logic might fit in the EPLD chosen.

The final two operations performed by the Design Processor software are to extract a simulator netlist file for use with the Timing Simulator, and create a Programmer Object File (POF). The POF file is used with the QP2-MAX programming hardware to program the desired part.

Design Simulation

Debugging and verification of a completed design can be accomplished with the PLDS-MAX+PLUS timing simulator. This program is an interactive, event-driven simulator that emulates the true timing and functional characteristics of the compiled design. Input stimulus can be created using a straightforward vector format, or the Graphical Waveform Editor can be used to enter them graphically. Simulation results can also be viewed either in tabular form or with the Waveform Editor.

The Simulator operates on the netlist extracted by the Design Processor, and performs timing simulation with 1/10 nanosecond resolution. During simulation, the program will check for a variety of timing relationships and warn the user when violations occur. These timing relationships include flip-flop set-up or hold time violations, minimum pulse width violations and minimum oscillation period violations as defined by the designer. The designer can also set break-point conditions for the simulator.

The Waveform Editor may be used in conjunction with the timing simulator to edit input stimulus files and to view simulation results. It provides multiple zoom levels for viewing and the ability to define busses. Logical operators may also be performed on pairs of waveforms to highlight particular relationships. Input waveforms are created using the mouse and familiar text editing commands.

Device Programming

The PLDS-MAX+PLUS includes both the software and hardware necessary to program, verify and read Cypress MAX devices. The QP2-MAX programmer provides the basic hardware capability, while specific device adapters are used with each particular device. Adapters for the CY7C344 (DIP and PLCC) and the CY7C342 (PLCC) are included with the PLDS-MAX+PLUS. Additional adapters for support of other MAX devices and packages can be purchased separately.

System Requirements

Minimum System Configuration

IBM PS/2 model 50 or higher, PC/AT or compatible computer.

PC-DOS version 3.1 or higher.

640 kbytes RAM.

EGA, VGA or Hercules monochrome display.

20-MB hard disk drive.

1.2-MB 5¼" or 1.44-MB 3½" floppy disk drive.

3-button serial port mouse.

Recommended System Configuration

IBM PS/2 model 70 or higher, or Compaq 386 20-Mhz computer.

PC-DOS version 3.3.

640 kbytes of RAM plus 1 MB of expanded memory with LIM 3.2-compatible EMS driver.

VGA graphics display.

20-MB hard disk drive.

1.2-MB 5¼" or 1.44-MB 3½" floppy disk drive.

3-button serial port mouse.

Ordering Information

CY3200	PLDS-MAX + PLUS System including:	
	CY3201	MAX + PLUS software, manuals and key.
	CY3202	QP2-MAX PLD programmer with CY3342 & CY3344 adapters.

Device Adapters

CY3342	Adapter for CY7C342 in PLCC packages.
CY3344	Adapter for CY7C344 in DIP and PLCC packages.
CY3342R	Adapter for CY7C342 in PGA packages.
CY33435	Adapter for CY7C343 and CY7C345 in DIP and PLCC packages.

CYPRESS SEMICONDUCTOR

CY3300

QuickPro II®

Features

- **Combined PROM, PLD, and EPROM Programmer**
- **Programs all Cypress CMOS & ECL PLDs and PROMs**
- **Easy-to-use, menu-driven software**
- **New device and feature updates via floppy disk and adapters**
- **Plugs into standard IBM PC® parallel port—no need to use up a bus slot**
- **Compatible with IBM PC/AT®, PS/2®, and compatible computers**
- **Programs 20-, 24-, 28-, 32-, 40-, 44-, and 68-pin Cypress PLDs and PROMs via device adapters**
- **Modular design with adapter bus for future device support and future feature enhancements**
- **Comprehensive self-test and automatic calibration software**
- **Supports Vmargin verification for a higher degree of device reliability**

Description

QuickPro II is Cypress's second-generation QuickPro PLD and PROM device programmer. It incorporates new architectural features that enable it to handle all current and future devices through a 96-pin universal bus connector. The QuickPro II hardware can be installed on any IBM PC/AT- or PS/2-compatible computer by simply plugging into a standard parallel port. The software communicates with the QuickPro II electronics via this parallel port and utilizes intelligent programming algorithms to minimize device programming time.

The QuickPro II architecture and feature set were dictated by the needs of Cypress's new-generation PLDs and PROMs. Many of these devices offer very high performance and complexity with large numbers of pins. To meet these needs, the QuickPro II utilizes flexible pin electronics, a universal adapter bus and a carefully engineered system design that minimizes electrical noise. Pin electronics are located as close as possible to the device being programmed. In addition to the V_{PP} and V_{CC} voltage sources needed to program parts, the QuickPro II incorporates a Vmargin voltage source for measuring the relative programming margins to which a device has been programmed and a Vref voltage source for doing on-board self-testing and calibration.

For PLDs, QuickPro II uses the JEDEC standard data format, so present and future design tools such as PLD ToolKit®, ABEL®, CUPL®, and PALASM® can be used. QuickPro II reads Intellec 86®, Motorola S, TEK and space format files. It also reads and writes PROM PC DOS binary files for use with assemblers and compilers. QuickPro II is a low-cost, full-feature programming/verification system with a flexible and extendible architecture. The user interface software is menu-driven with complete on-screen explanations.

Technical Information

Size

The QuickPro II base unit is approximately 10 1/2" x 8 1/2" x 1". Individual device family adapters vary in size from 5" x 3" to 6" x 6". The parallel port cable and AC power adapter cable are both approximately 6′ in length.

Power

AC Power Adapter: 17 VAC @ 500 mA

Device Adapters

Device adapters are external modules with various pin and socket configurations. Each adapter plugs into the QuickPro II bus connector and maps the pins of particular devices and packages to the pin electronics resources available at the connector. Each adapter has at least one LED that indicates when power is being applied to the socket. In addition to these device adapters, package adapters are also used to accommodate the various package options available for PLDs and PROMs.

Memory

640K of total memory is necessary to operate the QuickPro II software.

Devices Supported

QuickPro II hardware and software supports the programming and verification of all Cypress and Aspen PLDs and PROMs.

Ordering Information

CY3300 QuickPro II system including:

- CY3301 QuickPro II base unit
- CY3302 QuickPro II parallel port cable
- CY3303 QuickPro II AC power adapter
- CY3304 QuickPro II software (disk & manual)

CY3202 QP2-MAX version of QuickPro II for PLDS-MAX + PLUS design tool. Includes CY3342 and CY3344 adapters.

Device Adapters

CY3320	Adapter for all Cypress 20-, 24-, 28-, and 32-pin devices excluding the MAX parts. Contains 20-, 24, and 28- pin DIP sockets (package adapters required for 32-pin devices).
CY3342	Adapter for the CY7C342—PLCC
CY3342R	Adapter for the CY7C342—PGA
CY3344	Adapter for the CY7C344—PLCC & DIP
CY33435	Adapter for the CY7C343 and CY7C345—PLCC & DIP

Package Adapters

Package adapters are used with the CY3320 generic device programming adapter on the QuickPro II in order to accommodate Cypress's wide variety of device packaging options. The package adapters used with devices having 28 native pins on the QuickPro II are the same as those used on the original QuickPro®. The number of native pins that a device has refers to the number of actual signal, power and ground pins used—excluding any N/C (No Connects) in a particular package. All devices are programmed in the CY3320 adapter's DIP socket having the same number of pins as the native pins on the device. Thus, for example, a 22V10 is programmed in the 24-pin DIP socket, regardless of whether it is in a DIP package or a PLCC package, even though the PLCC package has 28 pins (4 are N/Cs). A package adapter between the 28-pin PLCC and the 24-pin DIP sockets is used to accomplish this. The following list summarizes the package adapters used with the CY3320 adapter on the QuickPro II.

Devices with 20 native pins

CY3360A	20-pin LCC – Package codes L61 and Q61 – All devices
CY3360B	20-pin PLCC – Package code J61 – All devices
CY3360C	20-pin SOJ – Package code V5 – All devices
CY3360D	20-pin Cerpack – Package code K71

Devices with 24 native pins

CY3361A	28-pin LCC (22V10, CG7C323, CG7C324)
CY3361B	28-pin LCC (7C325, 7C235, 7C245, 7C261/3/4, 7C281/2, 7C291/2, 7C245, 7C291A/2A/3A)
CY3361C	28-pin LCC (20G10)
CY3361D	28-pin LCC (20RA10)
CY3361E	28-pin PLCC and HLCC (22V10, CG7C323, CG7C324)
CY3361F	28-pin PLCC and HLCC (20G10, 20RA10)
CY3361G	24-pin Cerpack – Package codes K73, T73 – All devices
CY3361H	24-pin SOIC – Package code S13 – All devices

Devices with 28 native pins

CY3008	28-pin LCC – Package codes L64 and Q64 – All devices
CY3009	28-pin PLCC and HLCC – Package codes J64 and H64 – All devices
CY3022	28-pin SOJ – Package code V21 – All devices
CY3020	28-pin Cerpack – Package codes K74, T74 – All devices
CY3017	32-pin rectangular LCC (7C251/4)
CY3012	32-pin rectangular LCC (7C266, 7C271/4, 7C279)
CY3024	32-pin rectangular LCC (7C277)

Document #: 38-00129

Section Contents

Quality and Reliability **Page Number**

CYPRESS SEMICONDUCTOR

Quality, Reliability, and Process Flows

Corporate Views on Quality and Reliability

Cypress believes in product excellence. Excellence can only be defined by how the users perceive both our product quality and reliability. If you, the user, are not satisfied with every device that is shipped, then product excellence has not been achieved.

Product excellence does not occur by following the industry norms. It begins by being better than one's competitors, with better designs, processes, controls and materials. Therefore, product quality and reliability are built into every Cypress product from the start.

Some of the techniques used to insure product excellence are the following:

- Product Reliability starts at the initial design inception. It is built into every product design from the very start.
- Product Quality is built into every step of the manufacturing process through stringent inspections of incoming materials and conformance checks after critical process steps.
- Stringent inspections and reliability conformance checks are done on finished product to insure the finished product quality requirements are met.
- Field data test results are encouraged and tracked so that accelerated testing can be correlated to actual use experiences.

Product Assurance Documents

Cypress Semiconductor uses MIL-STD-883C and MIL-M-38510H as baseline documents to determine our Test Methods, Procedures and General Specifications for semiconductors.

Customers using our Commercial and Industrial grade product receive the benefit of a military patterned process flow at no additional charge.

Product Testing Categories

Five different testing categories are offered by Cypress:

1. Commercial operating range product: 0°C to +70°C.
2. Industrial operating range product: -40°C to +85°C.
3. Military Grade product processed to MIL-STD-883C; Military operating range: -55°C to +125°C.
4. SMD (Standardized Military Drawing) approved product: Military operating range: -55°C to + 125°C, electrically tested per the applicable Military Drawing.
5. JAN qualified product; Military operating range: -55°C to +125°C, electrically tested per MIL-M-38510 slash sheet requirements.

Category 1, 2, and 3 are available on all products offered by Cypress Semiconductor. Category 4 and 5 are offered on a more limited basis, dependent upon the specific part type in question.

Commercial Product Assurance Categories

Commercial grade devices are offered with two different classes of product assurance. Every device shipped, as a minimum, meets the processing and screening requirements of level 1.

Level 1: For commercial or industrial systems where the demand for quality and reliability is high, but where field service and device replacement can be reasonably accomplished.

Level 2: For enhanced reliability applications and commercial or industrial systems where maintenance is difficult and/or expensive and reliability is paramount.

Devices are upgraded from Level 1 to Level 2 by additional testing and a burn-in to MIL-STD-883, Method 1015.

Tables 1 and *2* list the 100% screening and quality conformance testing performed by Cypress Semiconductor in order to meet requirements of these programs.

Military Product Assurance Categories

Cypress' Military Grade components and SMD products are processed per MIL-STD-883C using methods 5004 and 5005 to define our screening and quality conformance procedures. The processing performed by Cypress results in a product that meets the class B screening requirements as called out by these methods. Every device shipped, as a minimum, meets these requirements.

JAN, SMD and Military Grade devices supplied by Cypress are processed for applications where maintenance is difficult or expensive and reliability is paramount. *Tables 3* through *Table 7* list the screening and quality conformance testing that is performed in order to meet the processing requirements required by MIL-STD-883C and MIL-M-38510.

Table 1. Cypress Commercial and Industrial Product Screening Flows—Components

Screen	MIL-STD-883 Method	Product Temperature Ranges Commercial 0°C to +70°C; Industrial -40°C to +85°C			
		Level 1		Level 2	
		Plastic	Hermetic	Plastic	Hermetic
Visual/Mechanical					
• Internal Visual	2010	0.4% AQL	100%	0.4% AQL	100%
• Hermeticity					
– Fine Leak	1014, Cond A or B (sample)	Does Not Apply	LTPD = 5	Does Not Apply	LTPD = 5
– Gross Leak	1014, Cond C	Does Not Apply	100%	Does Not Apply	100%
Burn-in					
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Burn-in	Per Cypress Specification	Does Not Apply	Does Not Apply	100%[1]	100%[1]
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	Does Not Apply	100%	100%
• Percent Defective Allowable (PDA)		Does Not Apply	Does Not Apply	5% (max)[2]	5% (max)[2]
Final Electrical	Per Device Specification				
• Static (DC), Functional, and Switching (AC) Tests	1. At 25°C and Power Supplies Extremes	Not Performed	Not Performed	100%[1]	100%[1]
	2. At Hot Temperature and Power Supply Extremes	100%	100%	100%	100%
Cypress Quality Lot Acceptance					
• External Visual	2009	[3]	[3]	[3]	[3]
• Final Electrical Conformance	Cypress Method 17-00064	[3]	[3]	[3]	[3]

Table 2. Cypress Commercial and Industrial Product Screening Flows—Modules

Screen	MIL-STD-883 Method	Product Temperature Ranges Commercial 0°C to +70°C; Industrial -40°C to +85°C	
		Level 1	Level 2
Burn-in			
• Pre-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Burn-in	1015	Does Not Apply	100%
• Post-Burn-in Electrical	Per Device Specification	Does Not Apply	100%
• Percent Defective Allowable (PDA)		Does Not Apply	15%
Final Electrical	Per Device Specification		
• Static (DC), Functional, and Switching (AC) Tests	1) At 25°C and Power Supply Extremes	Not Performed	100%
	2) At Hot Temperature and Power Supply Extremes	100%	100%
Cypress Quality Lot Acceptance			
• External Visual	2009	Per Cypress Module Specification	Per Cypress Module Specification
• Final Electrical Conformance	Cypress Method 17-00064	[3]	[3]

Notes:
1. Burn-in is performed as a standard for 12 hours at 150°C.
2. Electrical Test is performed after burn-in. Results of this are used to determine PDA percentage.
3. Lot acceptance testing is performed on every lot to guarantee 200 PPM average outgoing quality.

Table 3. Cypress JAN/SMD/Military Grade Product Screening Flows for Class B

Screen	Screening Per Method 5004 of MIL-STD-883	Product Temperature Ranges –55°C to +125°C		
		JAN	SMD/Military Grade Product	Military Grade Module
Visual/Mechanical				
• Internal Visual	Method 2010, Cond B	100%	100%	N/A
• Temperature Cycling	Method 1010, Cond C, (10 cycles)	100%	100%	Optional
• Constant Acceleration	Method 2001, Cond E (Min), Y1 Orientation Only	100%	100%	N/A
• Hermeticity:				
— Fine Leak	Method 1014, Cond A or B	100%	100%	N/A
— Gross Leak	Method 1014, Cond C	100%	100%	N/A
Burn-in				
• Pre-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%	100%
• Burn-in Test	Method 1015, Cond D, 160 Hrs at 125°C Min or 80 Hrs at 150°C	100%	100%	100% (48 Hours at 125°C)
• Post-Burn-in Electrical Parameters	Per Applicable Device Specification	100%	100%	100%
• Percent Defective Allowable (PDA)	Maximum PDA, for All Lots	5%	5%	10%
Final Electrical Tests				
• Static Tests	Method 5005 Subgroups 1, 2 and 3	100% Test to Slash Sheet	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Functional Tests	Method 5005 Subgroups 7, 8A and 8B	100% Test to Slash Sheet	100% Test to Applicable Device Specification	100% Test to Applicable Specification
• Switching	Method 5005 Subgroups 9, 10 and 11	100% Test to Slash Sheet	100% Test to Applicable Device Specification	100% Test to Applicable Specification
Quality Conformance Tests				
• Group A[4]	Method 5005, See	Sample	Sample	Sample
• Group B	Table 4–7 for	Sample	Sample	Sample
• Group C[5]	details	Sample	Sample	Sample
• Group D[5]		Sample	Sample	Sample
External Visual	Method 2009	100%	100%	100%

Notes:

4. Group A subgroups tested for SMD/Military Grade products are 1, 2, 3, 7, 8A, 8B, 9, 10, 11, or per JAN Slash Sheet.
5. Group C and D end-point electrical tests for SMD/Military Grade products are performed to Group A subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11, or per JAN Slash Sheet.

Table 4. Group A Test Descriptions

Subgroup	Description	Sample Size/Accept No.	
		Components	Modules[6]
1	Static Tests at 25°C	116/0	77/1
2	Static Tests at Maximum Rated Operating Temperature	116/0	55/1
3	Static Tests at Minimum Rated Operating Temperature	116/0	55/1
4	Dynamic Tests at 25°C	116/0	77/1
5	Dynamic Tests at Maximum Rated Operating Temperature	116/0	55/1
6	Dynamic Tests at Minimum Rated Operating Temperature	116/0	55/1
7	Functional Tests at 25°C	116/0	77/1
8A	Functional Tests at Maximum Temperature	116/0	55/1
8B	Functional Tests at Minimum Temperature	116/0	55/1
9	Switching Tests at 25°C	116/0	77/1
10	Switching Tests at Maximum Temperature	116/0	55/1
11	Switching Tests at Minimum Temperature	116/0	55/1

Cypress uses an LTPD sampling plan that was developed by the Military to assure product quality. Testing is performed to the subgroups found to be appropriate for the particular device type. All Military Grade component products have a Group A sample test performed on each inspection lot per MIL-STD-883 and the applicable device specification..

Table 5. Group B Quality Tests

Subgroup	Description	Quantity/Accept # or LTPD	
		Components	Modules[6]
2	Resistance to Solvents, Method 2015	4/0	4/0
3	Solderability, Method 2003	10	10/0
5	Bond Strength, Method 2011	15	NA

Notes:

6. Military Grade Modules are processed to proposed JEDEC standard flows for MIL-STD-883 compliant modules.

Group B testing is performed for each inspection lot. An inspection lot is defined as a group of material of the same device type, package type and lead finish built within a six week seal period and submitted to Group B testing at the same time.

Table 6. Group C Quality Tests

Subgroup	Description	LTPD	
		Components	Modules[6]
1	Steady State Life Test, End Point Electricals, Method 1005	5	15/2

Group C tests for JAN product are performed on one device type from one inspection for lot representing each technology. Sample tests are performed per MIL-M-38510 from each three month production of devices, which is based upon the die fabrication date code.

Group C tests for SMD and Military Grade products are performed on one device type from one inspection lot representing each technology. Sample tests are performed per MIL-STD-883 from each four calendar quarters production of devices, which is based upon the die fabrication date code.

End-point electrical tests and parameters are performed per the applicable device specification.

Table 7. Group D Quality Tests (Package Related)

Subgroup	Description	Quantity/Accept # or LTPD	
		Components	Modules[6]
1	Physical Dimensions, Method 2016	15	15/2
2	Lead Integrity, Seal: Fine & Gross Leak, Method 2004 & 1014	15	15/2
3	Thermal Shock, Temp Cycling, Moisture Resistance, Seal: Fine & Gross Leak, Visual Examination, End-Point, Electricals, Methods 1011, 1010, 1004 & 1014	15	15/2
4	Mechanical Shock, Vibration - Variable Frequency, Constant Acceleration, Seal: Fine & Gross Leak, Visual Examination, End-Point Electricals, Methods 2002, 2007, 2001 & 1014	15	15/2

Table 7. Group D Quality Tests (Package Related) (continued)

Sub-group	Description	Quantity/Accept # or LTPD	
		Components	Modules[7]
5	Salt Atmosphere, Seal: Fine & Gross Leak, Visual Examination, Methods 1009 & 1014	15 (0)	15/2
6	Internal Water-Vapor Content; 5000 ppm maximum @ 100°C. Method 1018	3(0) or 5(1)	N/A
7	Adhesion of Lead Finish,[8] Method 2025	15(0)	15/2
8	Lid Torque, Method 2024[9]	5(0)	N/A

Notes:
7. Does not apply to leadless chip carriers.
8. Based on the number of leads.
9. Applies only to packages with glass seals.

Group D tests for JAN product are performed per MIL-M-38510 on each package type from each six months of production, based on the lot inspection identification (or date) codes.

Group D tests for SMD and Military Grade products are performed per MIL-STD-883 on each package type from each 52 weeks of production, based on the lot inspection identification (or date) codes.

End-point electrical tests and parameters are performed per the applicable device specification.

Product Screening Summary

Commercial and Industrial Product

- Screened to either Level 1 or Level 2 product assurance flows
- Hermetic and Molded packages available
- Incoming Mechanical and Electrical performance guaranteed:
  - 0.02% AQL Electrical Sample test performed on every lot prior to shipment
  - 0.65% AQL External Visual Sample inspection
- Electrically tested to Cypress data sheet

Ordering Information

Product Assurance Grade: Level 1

- Order Standard Cypress part number
- Parts marked the same as ordered part number
  Ex: CY7C122-15PC, PALC22V10-25PI

Product Assurance Grade: Level 2

- Burn-in performed on all devices to Cypress detailed circuit specification
- Add "B" Suffix to Cypress standard part number when ordering to designate Burn-in option
- Parts marked the same as ordered part number
  Ex: CY7C122-15PCB, PALC22V10-25PIB

Military Grade Product

- SMD and Military Grade components are manufactured in compliance with paragraph 1.2.1 of MIL-STD-883. Compliant products are identified by an 'MB' suffix on the part number (CY7C122-25DMB) and the letter "C"
- JAN devices are manufactured in accordance with MIL-M-38510
- Military grade devices electrically tested to:
  - Cypress data sheet specifications

    OR
  - SMD devices electrically tested to military drawing specifications

    OR
  - JAN devices electrically tested to slash sheet specifications
- All devices supplied in Hermetic packages
- Quality conformance inspection: Method 5005, Groups A, B, C, and D performed as part of the standard process flow
- Burn-in performed on all devices
  - Cypress detailed circuit specification for non-Jan devices

    OR
  - Slash sheet requirements for JAN products
- Static functional and switching tests performed at 25°C as well as temperature and power supply extremes on 100% of the product in every lot
- JAN product manufactured in a DESC certified facility

Ordering Information

JAN Product:

- Order per military document
- Marked per military document
  Ex: JM38510/28901BVA

SMD Product:

- Order per military document
- Marked per military document
  Ex: 5962-8867001LA

Military Grade Product:

- Order per Cypress standard military part number
- Marked the same as ordered part number
  Ex: CY7C122-25DMB

Military Modules

- Military Temperature Grade Modules are designated with an 'M' suffix only. These modules are screened to standard combined flows and tested at both military temperature extremes.
- MIL-STD-883 Equivalent Modules are processed to proposed JEDEC standard flows for MIL-STD-883 compliant modules. All MIL-STD-883 equivalent modules are assembled with fully-compliant MIL-STD-883 components.

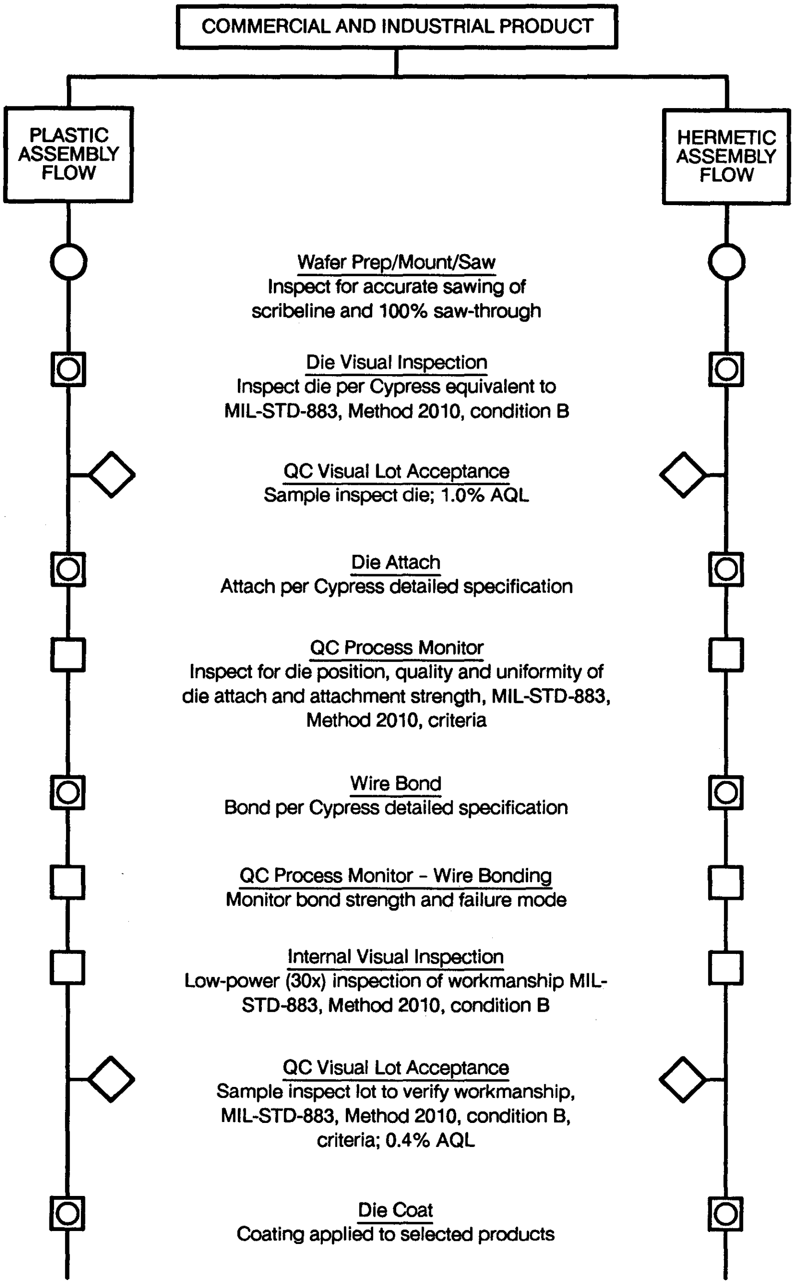
Product Quality Assurance Flow—Components

Area	PROCESS	Process Details
QC	INCOMING MATERIALS INSPECTION	All incoming materials are inspected to documented procedures covering the handling, inspection, storage, and release of raw materials used in the manufacture of Cypress products. Materials inspected are: wafers, masks, leadframes, ceramic packages and/or piece parts, molding compounds, gases, chemicals, etc.
FAB	DIFFUSION/ION IMPLANTATION	Sheet resistance, implant dose, species and CV characteristics are measured for all critical implants on every product run. Test wafers may be used to collect this data instead of actual production wafers. If this is done, they are processed with the standard product prior to collecting specific data. This assures accurate correlation between the actual product and the wafers used to monitor implantation.
FAB	OXIDATION	Sample wafers and sample sites are inspected on each run from various positions of the furnace load to inspect for oxide thickness. Automated equipment is used to monitor pinhole counts for various oxidations in the process. In addition, an appearance inspection is performed by the opeartor to further monitor the oxidation process.
FAB	PHOTOLITHOGRAPHY /ETCHING	Appearance of resist is checked by the operator after the spin operation. Also, after the film is developed, both dimensions and appearance are checked by the operator on a sample of wafers and locations upon each wafer. Final CDs and alignment are also sample inspected on several wafers and sites on each wafer on every product run.
FAB	METALIZATION	Film thickness is monitored on every run. Step coverage cross-sections are performed on a periodic basis to insure coverage.
FAB	PASSIVATION	An outgoing visual inspection is performed on 100% of the wafers in a lot to inspect for scratches, particles, bubbles, etc. Film thickness is verified on a sample of wafers and locations within each given wafer on each run. Pinholes are monitored on a sample basis weekly.
FAB	QC VISUAL OF WAFERS	
FAB	E-TEST	Electrical test is performed for final process electrical characteristics on every wafer.
FAB	QC MONITOR OF E-TEST DATA	Weekly review of all data trends; running averages, minimums, maximums, etc. are reviewed with the process control manager.
TEST	WAFER PROBE/SORT	Verify functionality, electrical characteristics, stress test devices.
TEST	QC CHECK PROBING AND ELECTRICAL TEST RESULTS	Pass/fail lot based on yield and correct probe placement.

TO ASSEMBLY AND TEST

(continued)

Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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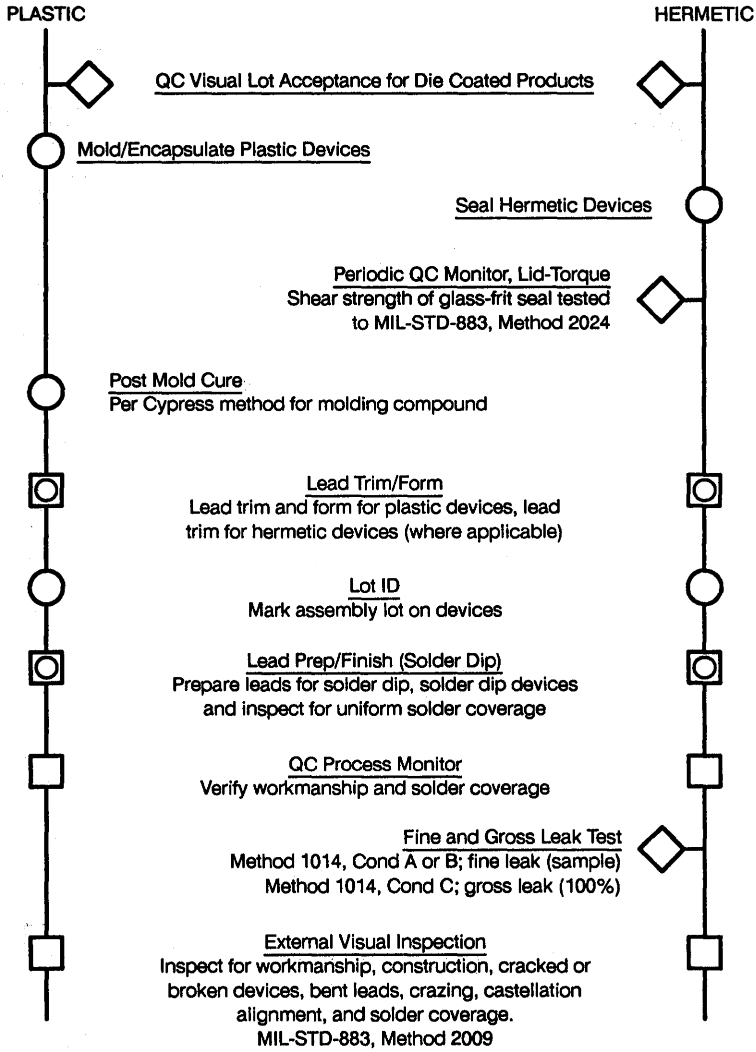
Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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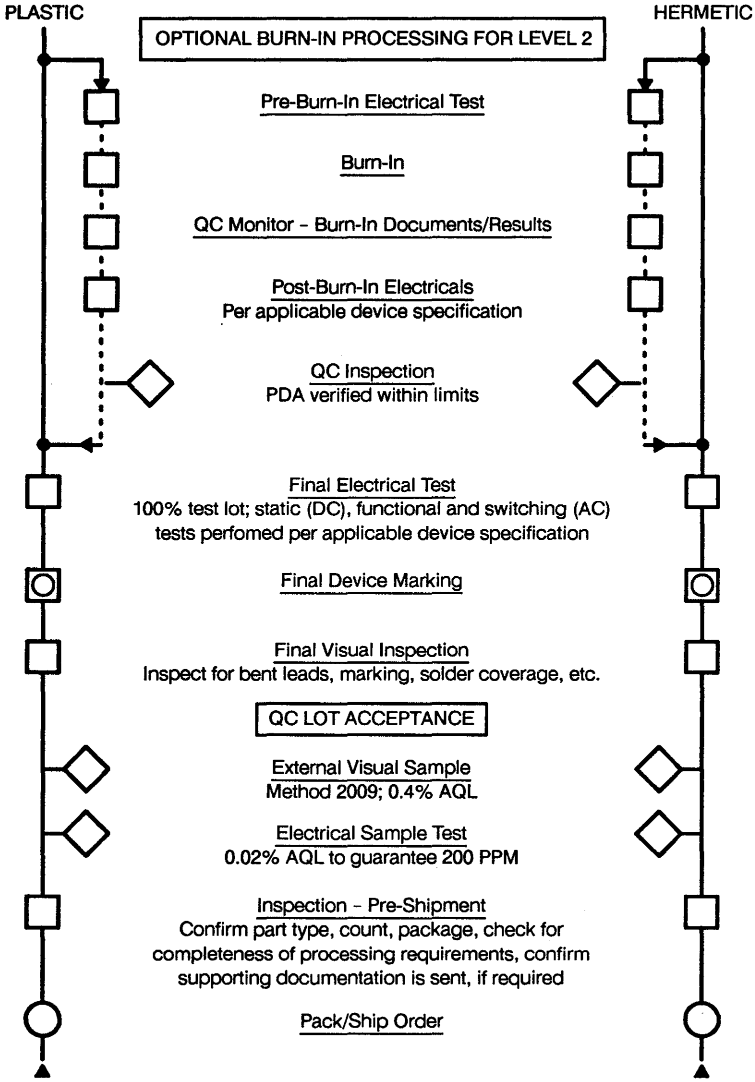
Product Quality Assurance Flow—Components (continued)
Commercial and Industrial Product



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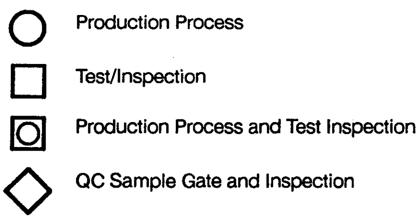
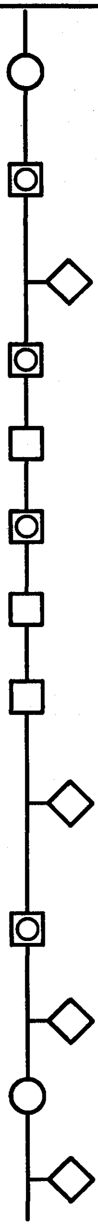


Product Quality Assurance Flow—Components
Military Components

MILITARY ASSEMBLY FLOW



Wafer Prep/Mount/Saw
Inspect for accurate sawing of scribeline and 100% saw-through

Die Visual Inspection
Inspect die per MIL-STD-883, Method 2010, condition B

QC Visual Lot Acceptance
Sample inspect die; 1.0% AQL

Die Attach
Attach per Cypress detailed specification

Die Adherence Monitor
MIL-STD-883, Method 2019 or Method 2027

Wire Bond
Bond per Cypress detailed specification

Bond Pull Monitor
MIL-STD-883, Method 2011

Internal Visual Inspection
Low-power and high-power inspection per
MIL-STD-883, Method 2010, condition B

QC Visual Lot Acceptance
Sample inspect lot per MIL-STD-883,
Method 2010, condition B, 0.4% AQL

Die Coat
Coating applied to selected products

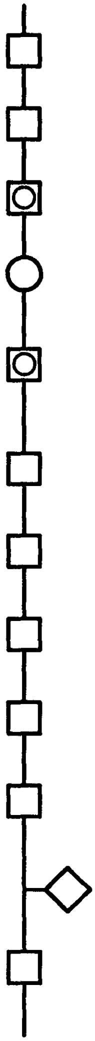
QC Visual Lot Acceptance for Die Coated Products

Seal

Periodic QC Monitor, Lid-Torque
Shear strength of glass

(continued)

Product Quality Assurance Flow—Components (continued)
Military Components



Temperature Cycle
Method 1010, Cond C, 10 cycles

Constant Acceleration
Method 2001, Cond E, Y1 Orientation

Lead Trim
Lead trim when applicable

Lot ID
Mark assembly lot on devices

Lead Finish
Solder dip or matte tin plate applicable devices and inspect

QC Process Monitor
Verify workmanship and lead finish coverage

External Visual Inspection
Method 2009

Pre-Burn-In Electrical Test
Method 5004, per applicable device specification

Burn-In
Method 1015, condition D

Post-Burn-In Electricals
Method 5004, per applicable device specification

PDA Calculation
Method 5004, 5%

Final Electrical Test
Method 5004; Static, functional and switching tests per applicable device specification

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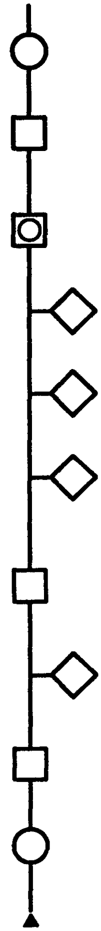
Product Quality Assurance Flow—Components (continued)
Military Components



Lead Finish - Solder Dip
Solder dip applicable devices

Fine and Gross Leak Test
Method 1014, condition A or B, fine leak; condition C, gross leak

Final Device Marking
MIL-STD-883 or applicable device specification

Group B
Method 5005

Group A
Method 5005, per applicable device specification

Group C and D
Method 5005, in accordance with 1.2.1 of MIL-STD-883; JAN devices in accordance with MIL-M-38510

External Visual
Method 2009, 100% inspection

External Visual Sample
Method 2009, 0.4% AQL

Plant Clearance

Pack/Ship Order

Key

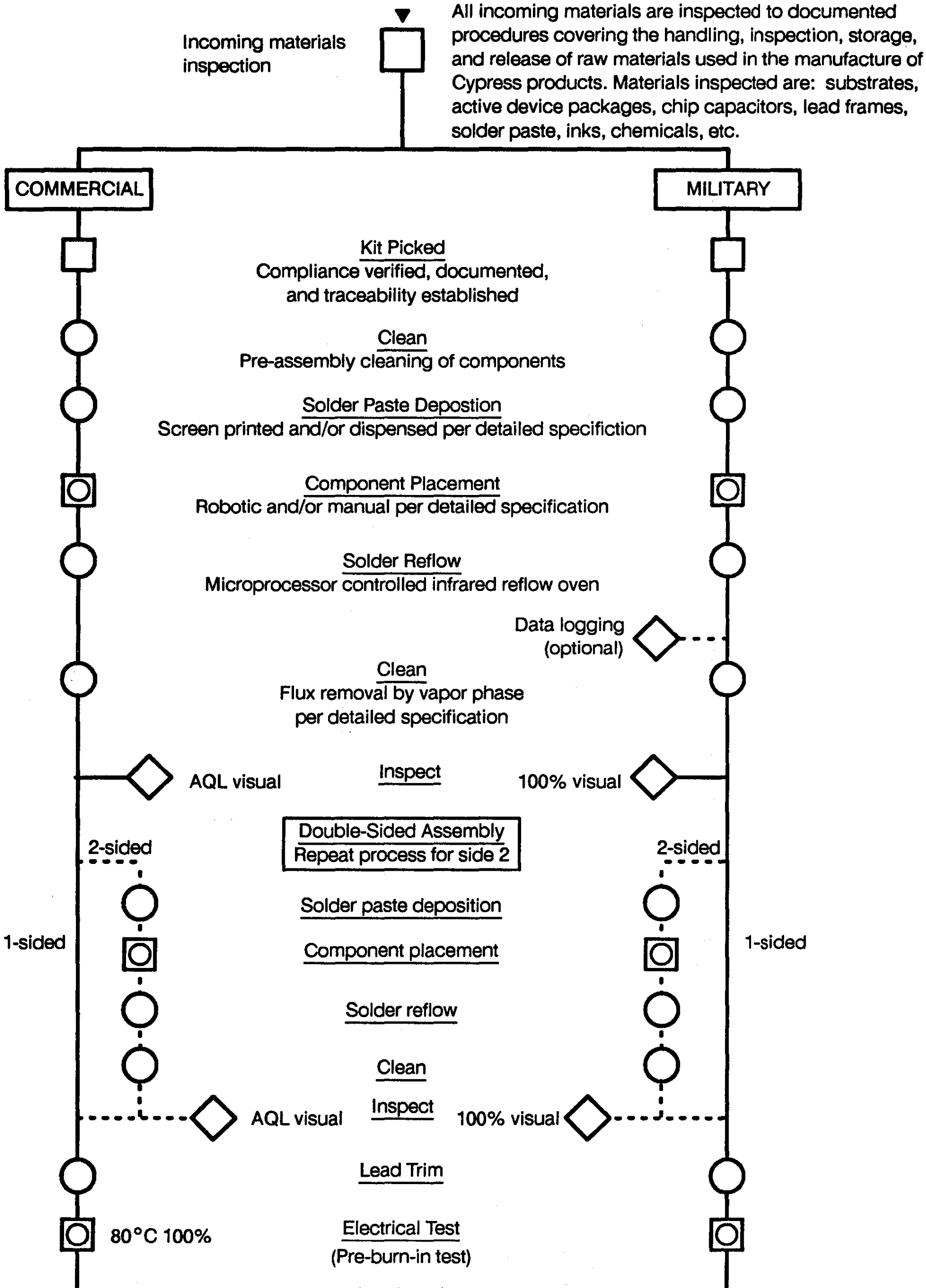
Production Process

Test/Inspection

Production Process and Test Inspection

QC Sample Gate and Inspection

Product Quality Assurance Flow—Modules



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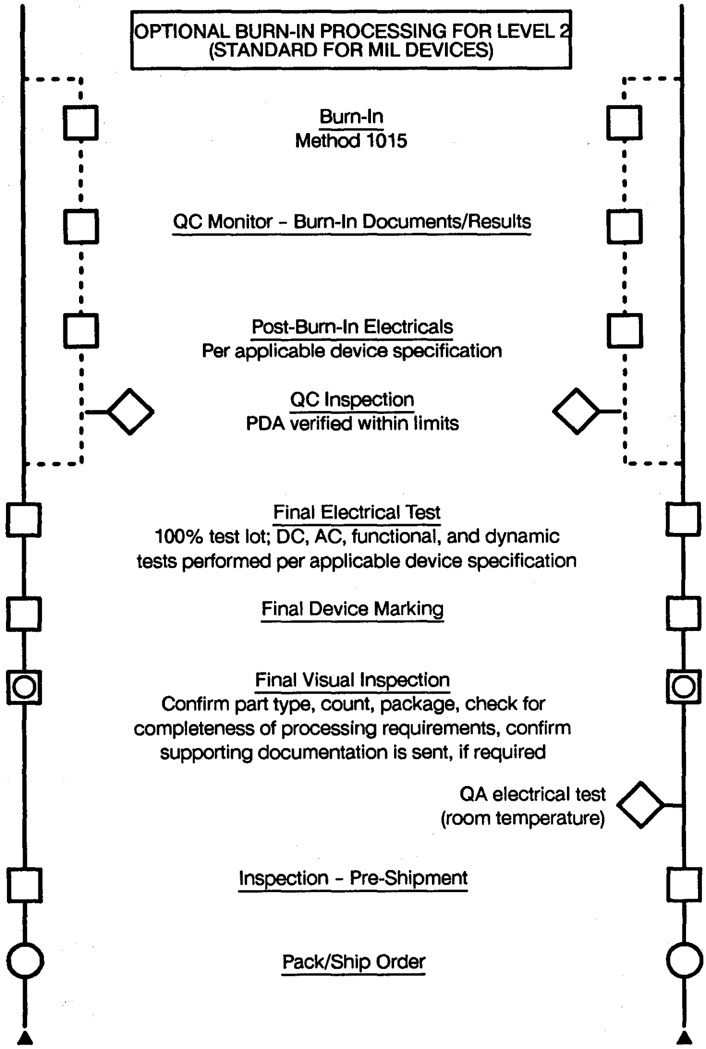
Product Quality Assurance Flow—Modules (continued)



Key

- Production Process
- Test/Inspection
- Production Process and Test Inspection
- QC Sample gate and inspection

Reliability Monitor Program

The Reliability Monitor Program is a documented Cypress procedure that is described in Cypress specification #25-00008, which is available to Cypress customers upon request. This specification describes a procedure that provides for periodic reliability monitors to insure that all Cypress products comply with established goals for reliability improvement and to minimize reliability risks for Cypress customers. The Reliability Monitor Program is designed to monitor key products within each generic process family. This procedure requires that detailed failure analysis be performed on all test rejects and the corrective actions be taken as indicated by the analysis. A summary of the Reliability Monitor Program test and sampling plan is shown below.

Reliability Monitor Program Sampling Plan

Test Description	Duration	Sample Size	Frequency[10]
Early Failure Rate (EFR)			
150°C HTOL	12 Hours	195/116[11]	Weekly
125°C HTOL	80 Hours	195/116[10]	Bi-Weekly
Latent Failure Rate (LFR)			
150°C HTOL	2000 Hours	195/116[10]	Monthly
125°C HTOL	3000 Hours	195/116[10]	Monthly
High Temperature Steady State Life (HTSSL)			
150°C HTOL	168 Hours	116	Weekly
150°C HTOL (1 lot/quarter extended)	1000 Hours	116	Quarterly
Plastic Package Data Retention (DRET) PROM/PLD 165°C Bake	1000 Hours	45	Weekly
Hermetic Package Data Retention (DRET) PROM/PLD 250°C Bake	1000 Hours	45	Bi-Weekly
Pressure Cooker (PCT) 121°C/100% R. H.	288 Hours	45	Weekly
High-Acceleration Saturation (HAST) Biased 121°C/85% R. H.	200 Hours	45	Monthly
Temperature Cycle (T/C)			
- 65°C to + 150°C	100 Cycles	45	Weekly
- 65°C to + 150°C (1 lot/quarter extended)	1000 Cycles	45	Quarterly

Notes:

10. Maximum period between samples is listed. More frequent sampling may occur.
11. 116 units for PROM/PLD.

13

Tape and Reel Specifications

Description

Surface-mounted devices are packaged in embossed tape and wound onto reels for shipment in compliance with Electronics Industries Association Standard EIA-481 Rev. A.

Specifications

Cover Tape

- The cover tape may not extend past the edge of the carrier tapes
- The cover tape shall not cover any part of any sprocket hole.
- The seal of the cover tape to the carrier tape is uniform, with the seal extending over 100% of the length of each pocket, on each side.
- The force to peel back the cover tape from the carrier tape shall be: 20 gms minimal, 70 gms nominal, 100 gms maximal, at a pull-back speed of 300 ± 10 mm/min.

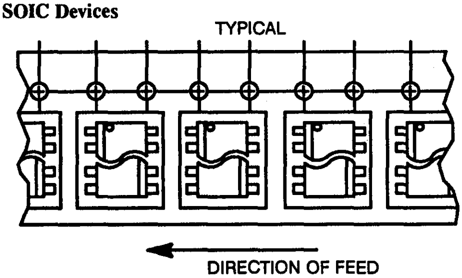
Loading the Reel

Empty pockets between the first and last filled pockets on the tape are permitted within the following requirements:

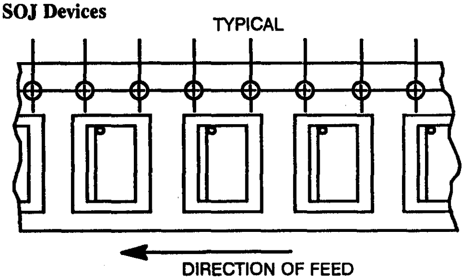
- No two consecutive pockets may be left empty
- No more than a total of ten (10) empty pockets may be on a reel

The surface-mount devices are placed in the carrier tape with the leads down, as shown in *Figure 1.*

SOIC Devices



SOJ Devices



PLCC and LCC Devices

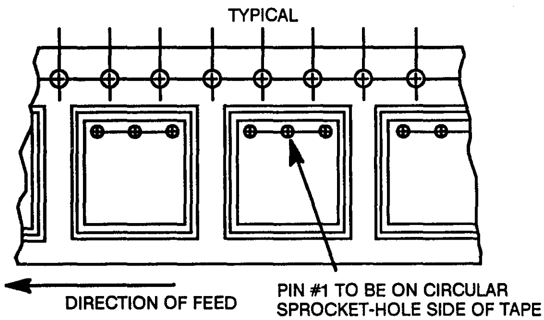


Figure 1. Part Orientation in Carrier Tape

Leaders and Trailers

The carrier tape and the cover tape may not be spliced. Both tapes must be one single uninterrupted piece from end to end.

Both ends of the tape must have empty pockets meeting the following minimum requirements:

- Trailer end (inside hub of reel) is 300 mm minimum
- Leader end (outside of reel) is 500 mm min., 560 mm max.
- Unfilled leader and trailer pockets are sealed
- Leaders and trailers are taped to tape and hub respectively using masking tape

Packaging

- Full reels contain a standard number of units (refer to *Table 1*)
- Reels may contain up to 3 inspection lots.
- Each reel is packed in an anti-static bag and then in its own individual box.
- Labels are placed on each reel as shown in *Figure 2*. The information on the label consists of a minimum of the following information, which complies with EIA 556, "Shipping and Receiving Transaction Bar Code Label Standard":
  - Barcoded Information:
    Customer PO number
    Quantity
    Date code
  - Human Readable Only:
    Package count (number of reels per order)
    Description
    "Cypress-San Jose"
    Cypress p/n
    Cypress CS number (if applicable)
    Customer p/n
- Each box will contain an identical label plus an ESD warning label.

Ordering Information

CY7Cxxx-yyzzz

xxx = part type

yy = speed

zzz = package, temperature, and options

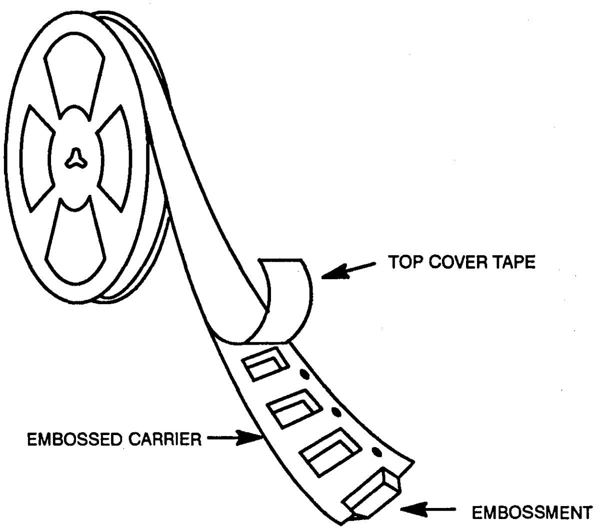
SCT = soic, commercial temperature range
SIT = soic, inductrial temperature range
SCR = soic, commercial temperature plus burn-in
SIR = soic, industrial temperature plus burn-in
VCT = soj, commercial temperature range
VIT = soj, industrial temperature range
VCR = soj, commercial temperature plus burn-in
VIR = soj, industrial temperature plus burn-in
JCT = plcc, commercial temperature range
JIT = plcc, industrial temperature range
JCR = plcc, commercial temperature range plus burn-in
JIR = plcc, industrial temperature range plus burn-in

Notes:

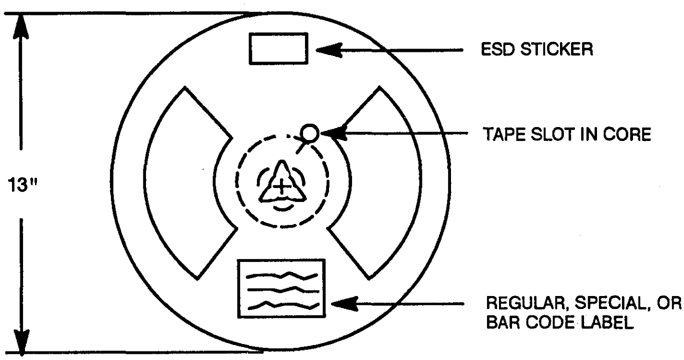
1. The T or R suffix will not be marked on the device. Units will be marked the same as parts in a tube.
2. Order releases must be in full-reel multiples as listed in *Table 1.*

Table 1. Parts Per Reel and Tape Specifications

Package Type	Terminals	Carrier Width (mm)	Pocket Pitch	Parts Per Meter	Parts Per Full Reel
PLCC	18	24	3	83.3	750
	20	16	3	83.3	750
	28(S)	24	4	62.5	500
	44	32	6	41.6	400
	52	32	6	41.6	400
	68	44	8	31.2	350
	84	44	8	31.2	350
SOIC	20	24	3	83.3	1,000
	24	24	3	83.3	1,000
	28	24	3	83.3	1,000
SOJ	20	24	3	83.3	1,000
	24	24	3	83.3	1,000
	28	24	3	83.3	1,000
PQFP	84	32	8	31.2	500
	100	44	9	27.7	400
	132	44	9	27.7	350
	164	56	11	22.7	200
	196	56	11	22.7	200



Tape and Reel Shipping Medium



Label Placement

Figure 2. Shipping Medium and Label Placement

Section Contents

Packages **Page Number**

CYPRESS SEMICONDUCTOR

Thermal Management and Component Reliability

One of the key variables determining the long-term reliability of an integrated circuit is the junction temperature of the device during operation. Long-term reliability of the semiconductor chip degrades proportionally with increasing temperatures following an exponential function described by the Arrhenius equation of the kinetics of chemical reactions. The slope of the logarithmic plots is given by the activation energy of the failure mechanisms causing thermally activated wear out of the device (see *Figure 1.*).

Typical activation energies for commonly observed failure mechanisms in CMOS devices are shown in *Table 1.*

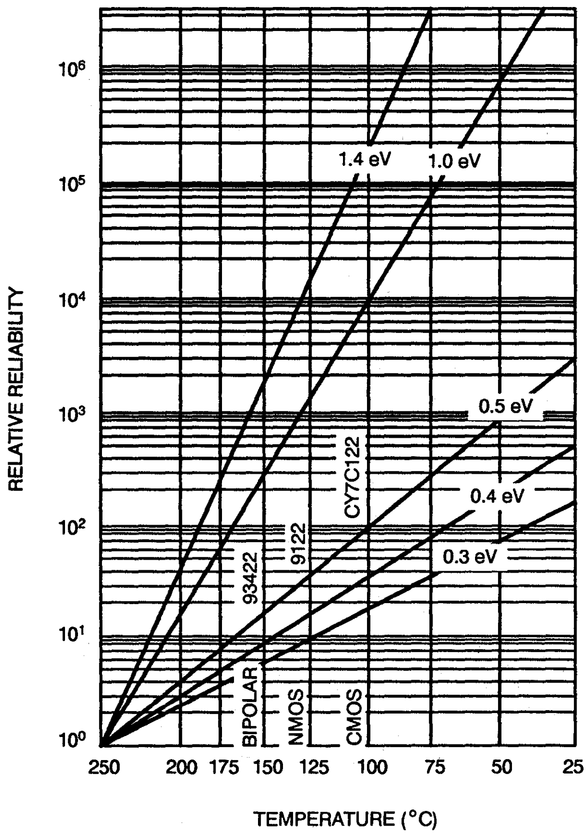


Figure 1. Arrhenius plot, which assumes a failure rate proportional to EXP ($-E_A/kT$) where E_A is the activation energy for the particular failure mechanism

14

Table 1. Failure Mechanisms and Activation Energies in CMOS Devices

Failure Mode	Approximate Activation Energy (EQ)
Oxide Defects	0.3 eV
Silicon Defects	0.3 eV
Electromigration	0.6 eV
Contact Metallurgy	0.9 eV
Surface Charge	0.5—1.0 eV
Slow Trapping	1.0 eV
Plastic Chemistry	1.0 eV
Polarization	1.0 eV
Microcracks	1.3 eV
Contamination	1.4 eV

To reduce thermally activated reliability failures, Cypress Semiconductor has optimized both their low-power generating 1.2μ CMOS device fabrication process and their high heat dissipation packaging capabilities. *Table 2* demostrates this optimized thermal performance by comparing bipolar, NMOS and Cypress high-speed 1K SRAM CMOS devices in their respective plastic packaging environments under standard operating conditions

Table 2. Thermal Performance of Fast 1K SRAMs in Plastic Packages

Technology	Bipolar	NMOS	Cypress CMOS
Device Number	93422	9122	7C122
Speed (ns)	30	25	25
I_{CC} (mA)	150	110	60
V_{CC} (V)	5.0	5.0	5.0
P_{MAX} (mW)	750	550	300
Package RTH (JA) (°C/W)	120	120	70
Junction Temperature (°C) at Data Sheet P_{MAX}[1]	160	136	91

Notes:
1. $T_{ambient} = 70°C$

During its normal operation, the Cypress 7C122 device experiences a 91°C junction temperature, whereas competitive devices in their respective packaging environments see a 45°C and 69°C higher junction temperature. In terms of relative reliability life expectancy, assuming a 1.0 eV activation energy failure mechanisms, this translates into an improvement in excess of two orders of magnitude (100x) over the bipolar 93422 device and more than one order of magnitude (30x) over the NMOS 9122 device.

Thermal Performance Data of Cypress Component Packages

The thermal performance of a semiconductor device in its package is determined by many factors, including package design and construction, packaging materials, chip size, chip thickness, chip attachment process and materials, package size, etc.

Thermal Resistance (θ_{JA}, θ_{JC})

For a packaged semiconductor device, heat generated near the juction of the powered chip causes the juction temperature to rise above the ambient temperature. The total thermal resistance is defined as

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

and θ_{JA} physically represents the temperature differential between the die junction and the surrounding ambient at a power dissipation of 1 watt.

The junction temperature is given by the equation

$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

$$\theta_{JC} = \frac{T_J - T_C}{P} \quad \text{and} \quad \theta_{CA} = \frac{T_C - T_A}{P}$$

T_A = Ambient temperature at which the device is operated; Most common standard temperature of operation equals 70°C

T_J = Junction temperature of the IC chip

T_C = Temperature of the case (package)

P = Power at which the device operates

θ_{JC} = Junction-to-case thermal resistance

θ_{JA} = Junction-to-ambient thermal resistance

θ_{CA} = Case-to-ambient thermal resistance

The junction-to-ambient environment is a still-air environment where the device is inserted into a low-cost standard device socket and mounted on a standard .062" G10 PC board. For juction-to-case measurements, the same assembly is immersed into a constant temperature liquid reservoir approaching infinite heat sinking for the heat dissipated from the package surface.

The thermal resistance values of Cypress standard packages are graphically illustrated in *Figures* 2 through 5. Each envelope represents a spread of typical Cypress integrated circuit chip sizes (upper boundary = 5000 Mils^2, lower boundary = 30,000 Mils^2) in their thermally optimized packaging environment.

All thermal characteristics are measured using the TSP (Temperature Sensitive Parameter) test method described in MIL STD 883C, Method 1012.1. A thermal silicon test chip, containing a 25Ω diffused resistor to heat the chip and a calibrated TSP diode to measure the junction temperature, is used for all characterizations.

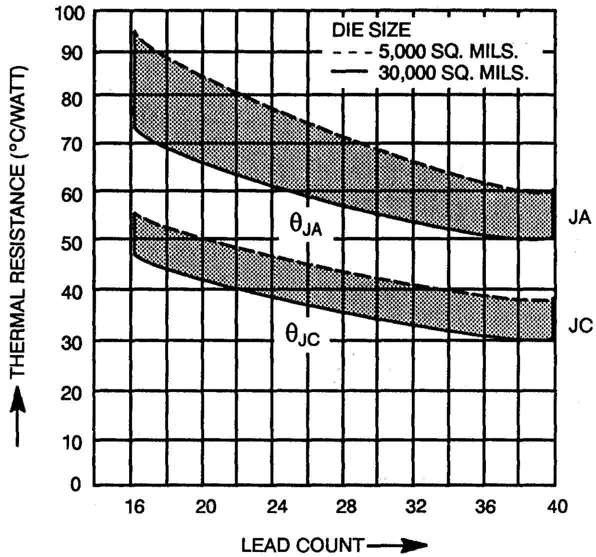


Figure 2. Thermal Resistance of Cypress Plastic DIP Packages

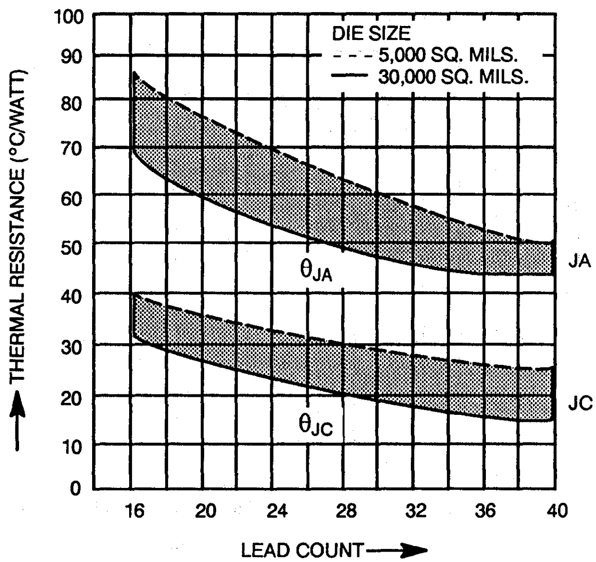


Figure 3. Thermal Resistance of Cypress Cerdip Packages

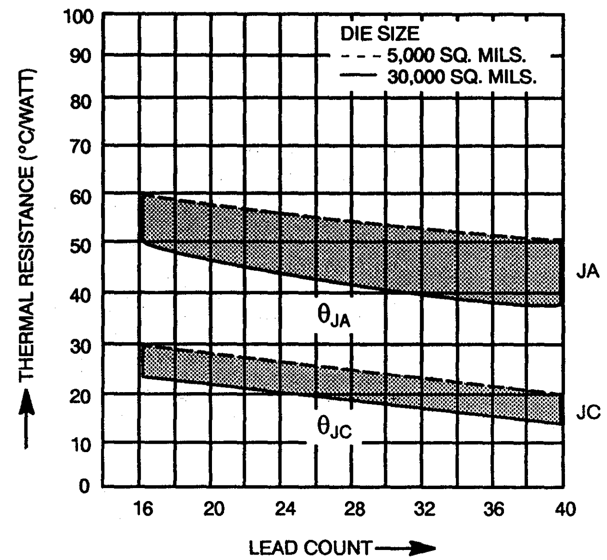


Figure 4. Thermal Resistance of Cypress Hermetic Chip Carriers (HLCC)

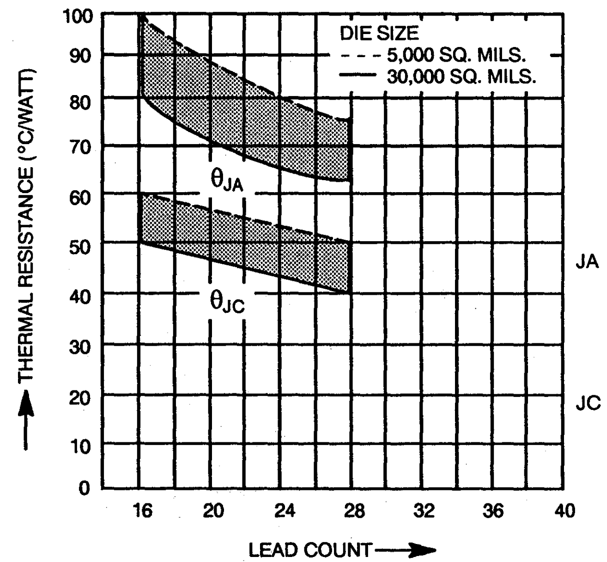


Figure 5. Thermal Resistance of Cypress SOICs

Packaging Materials

Cypress Plastic Packages incorporate:

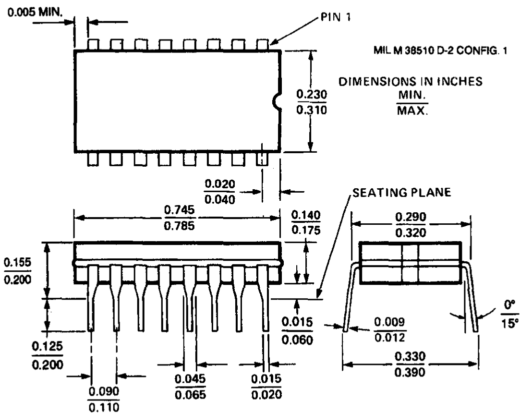
- High thermal conductivity copper lead frame
- Molding compound with high thermal conductivity
- Silver-filled conductive epoxy as die attach material
- Gold bond wires

Cypress Cerdip Packages incorporate:

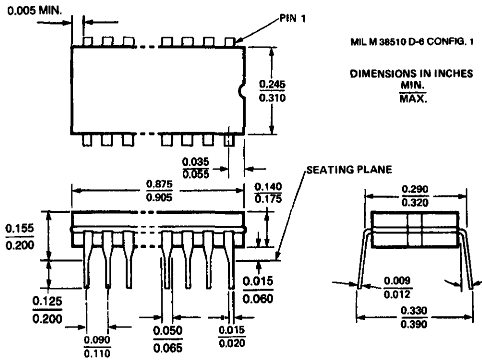
- High conductivity alumina substrates
- Silver-filled glass as die attach material
- Alloy 42 lead frame
- Aluminum bond wires

Package Diagrams

16 Lead (300 MIL) Cerdip D2

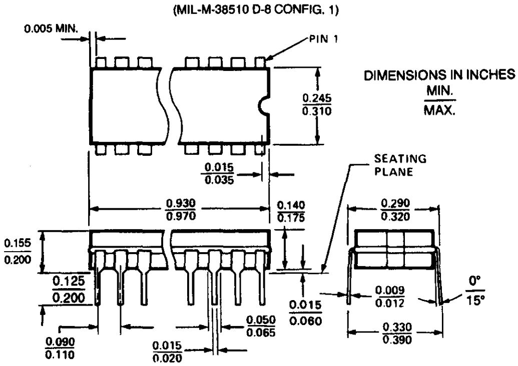


18 Lead (300 MIL) Cerdip D4



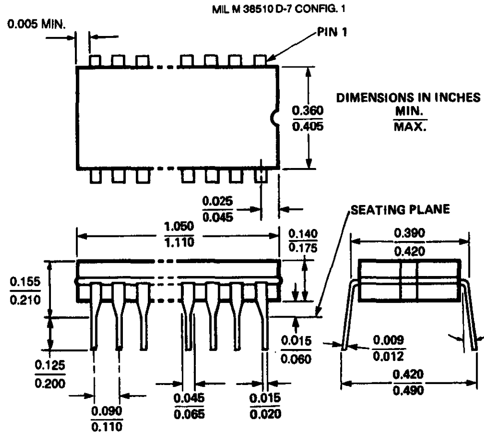
20 Lead (300 MIL) Cerdip D6

(MIL-M-38510 D-8 CONFIG. 1)

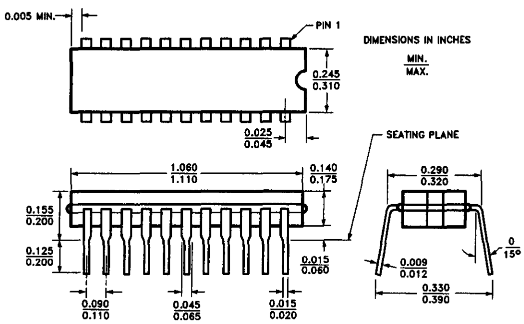


22 Lead (400 MIL) Cerdip D8

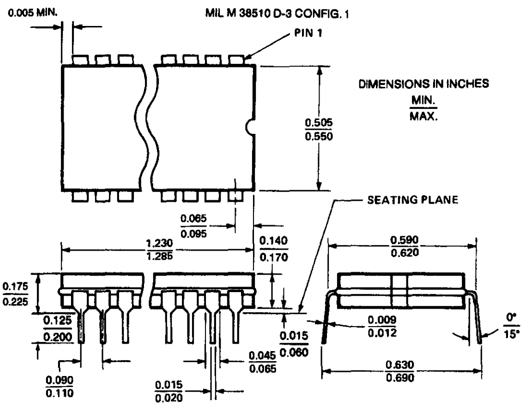
MIL M 38510 D-7 CONFIG. 1



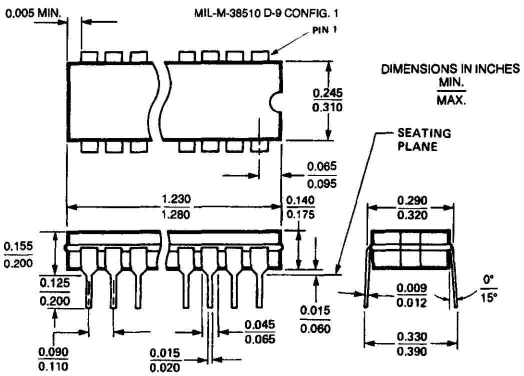
22 Lead (300 MIL) Cerdip D10



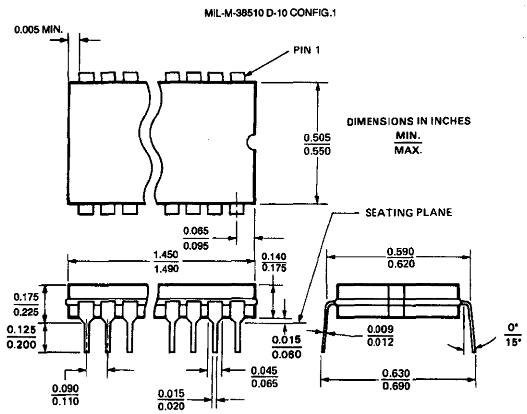
24 Lead (600 MIL) Cerdip D12



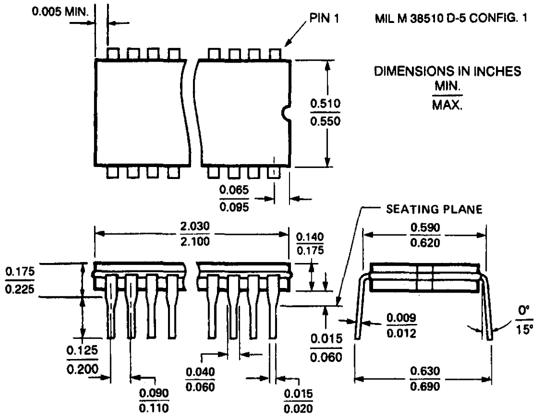
24 Lead (300 MIL) Cerdip D14



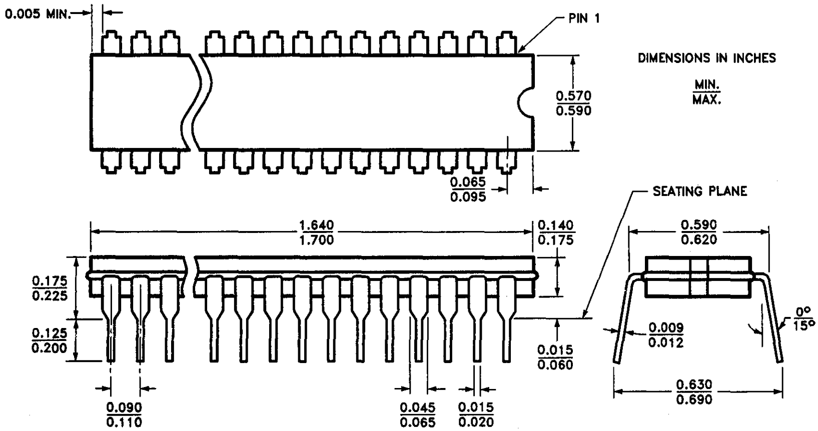
28 Lead (600 MIL) Cerdip D16



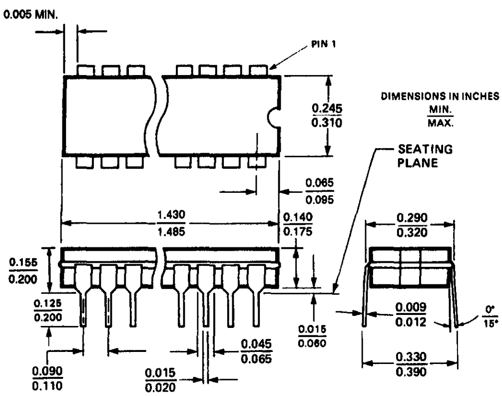
40 Lead (600 MIL) Cerdip D18



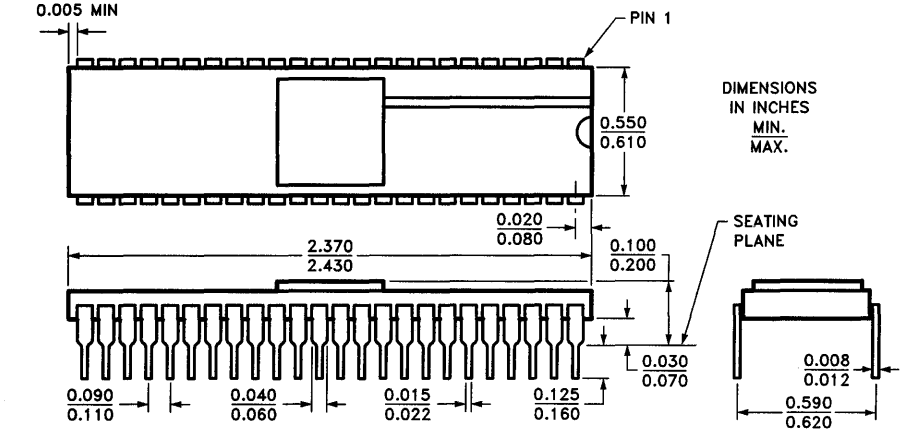
32 Lead (600 MIL) Cerdip D20



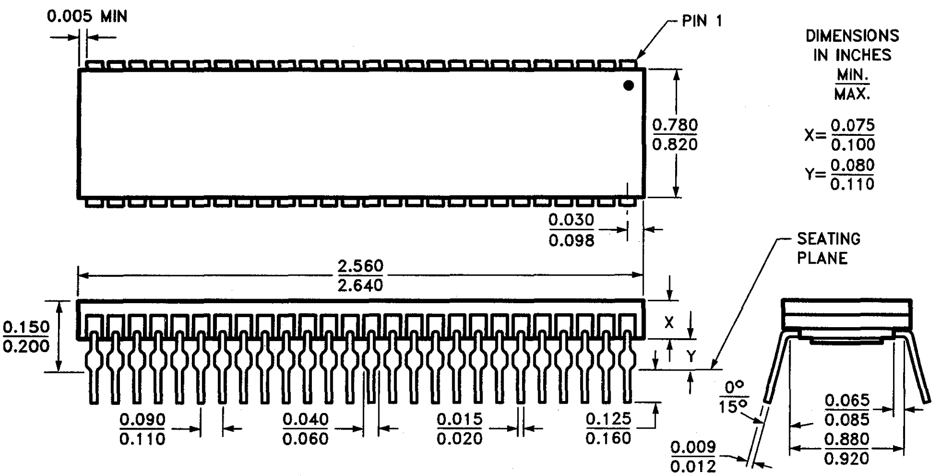
28 Lead (300 MIL) Cerdip D22



48 Lead (600 MIL) Sidebraze DIP D26

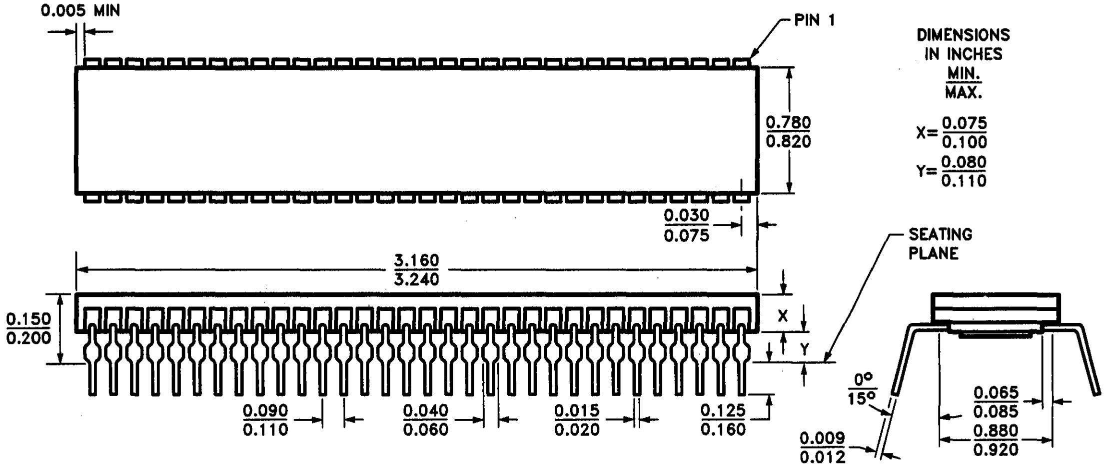


52 Lead (900 MIL) Bottombraze DIP D28

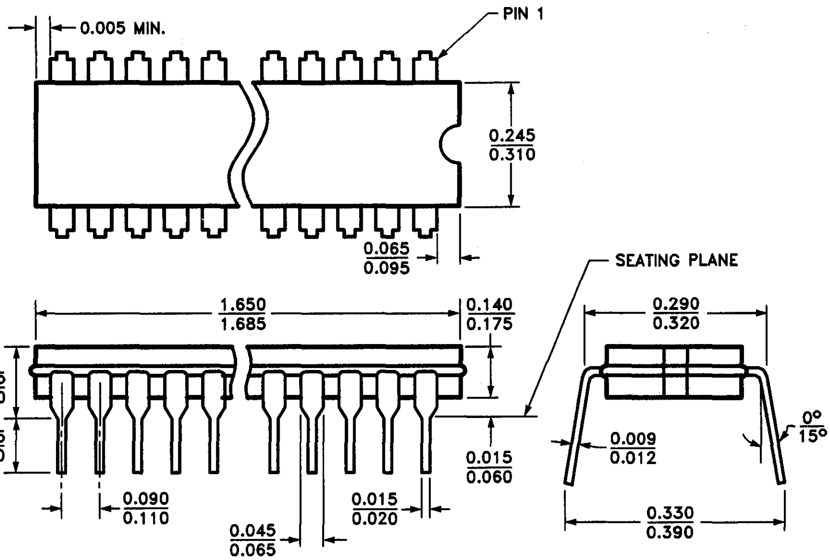


14

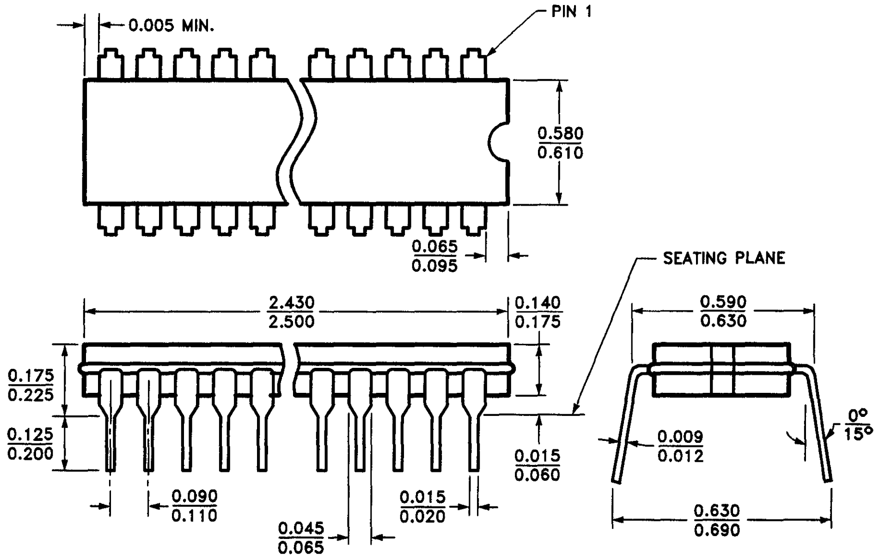
64 Lead (900 MIL) Bottombraze DIP D30



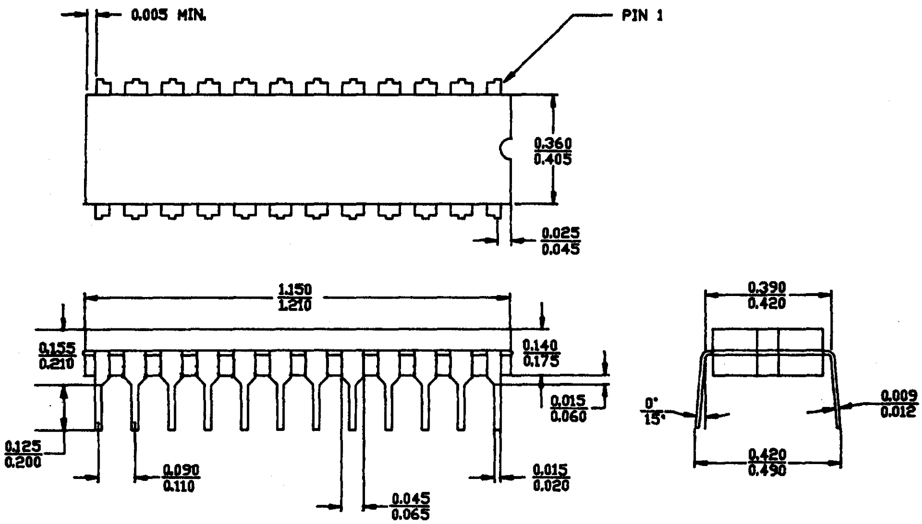
32 Lead (300 MIL) Cerdip D32



48 Lead (600 MIL) Cerdip D34

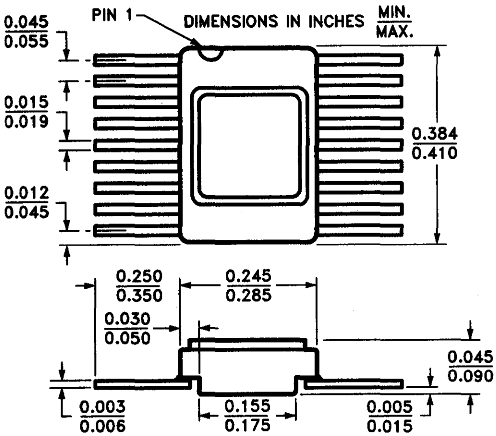


24 Lead (400 MIL) Cerdip D40

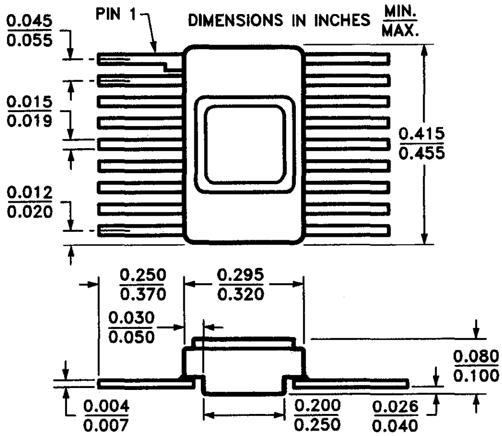


16 Lead Rectangular Flatpack F69

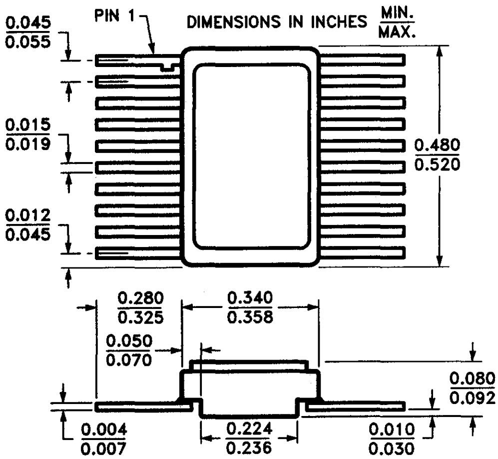
(MIL-M-38510 F-5 CONFIG 2)



18 Lead Rectangular Flatpack F70

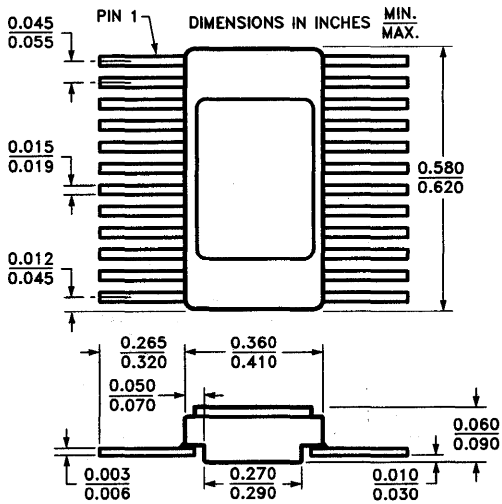


20 Lead Rectangular Flatpack F71

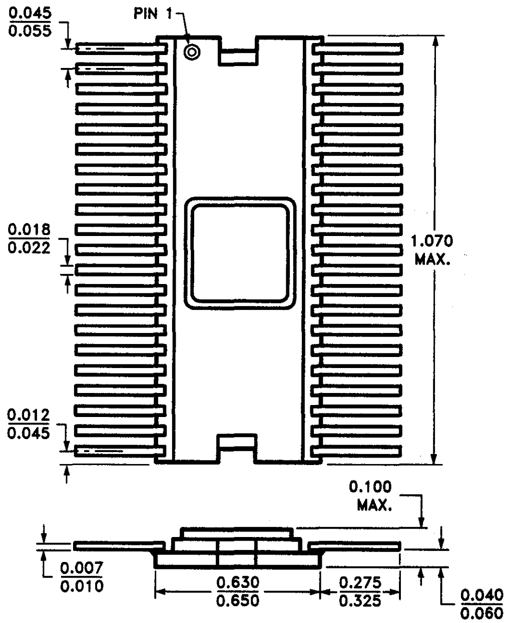


24 Lead Rectangular Flatpack F73

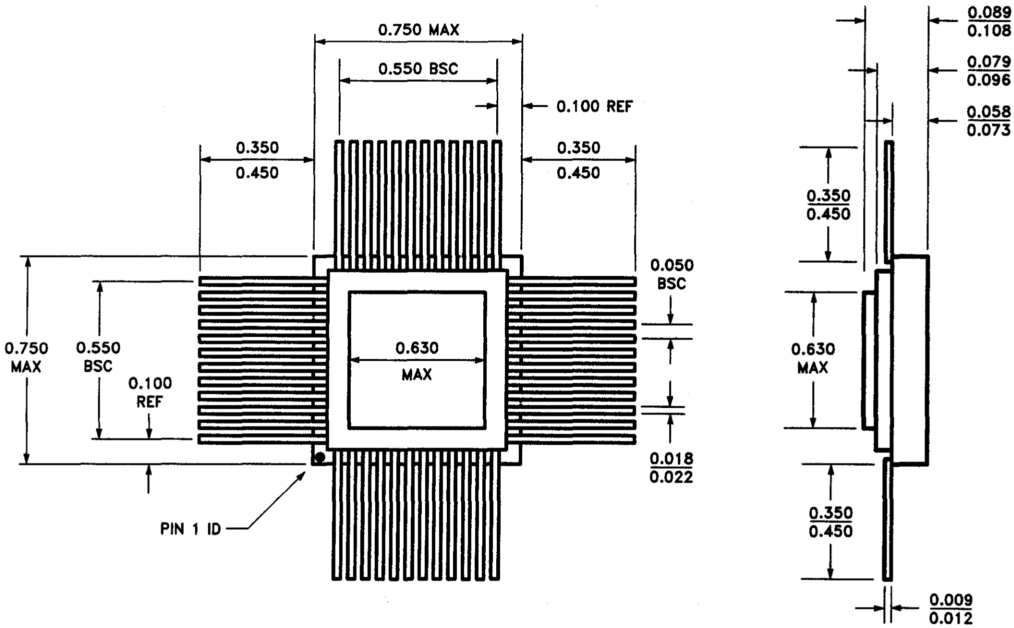
(MIL-M-38510 F-6 CONFIG 2)



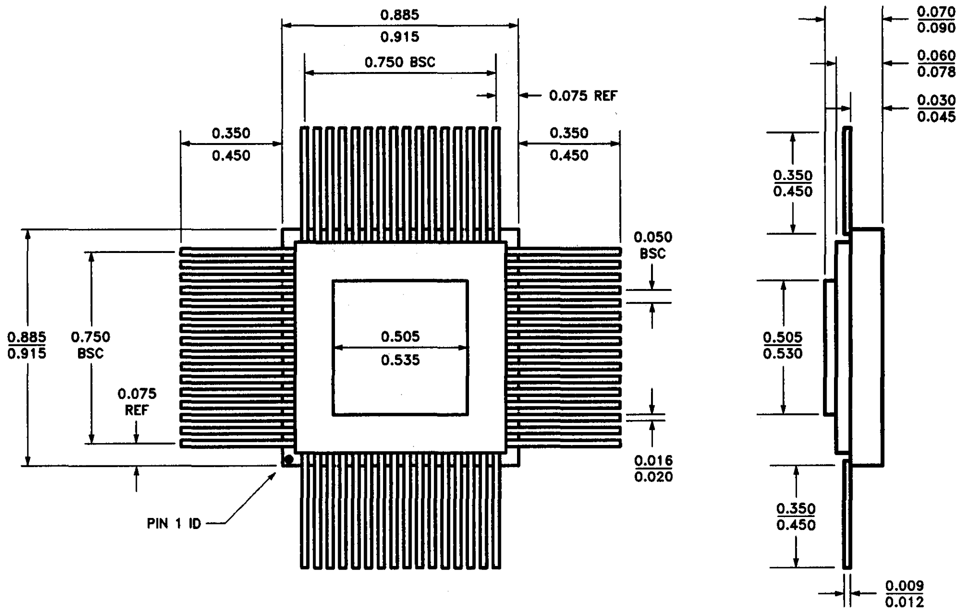
42 Lead Rectangular Flatpack F76



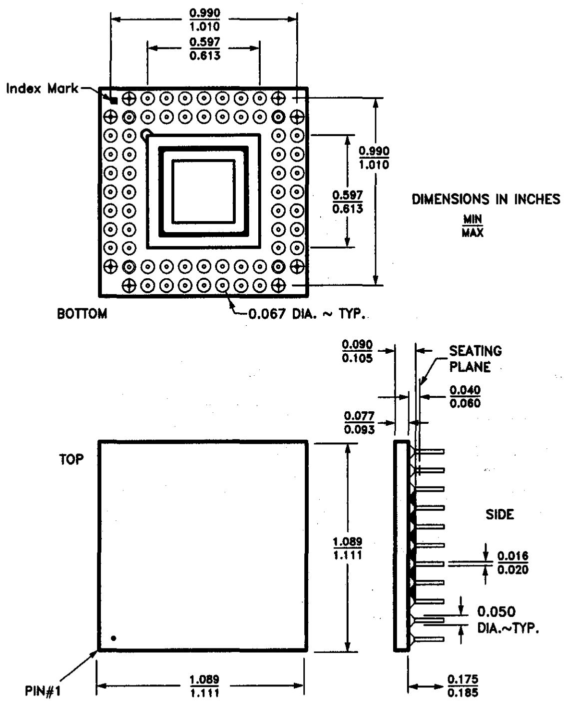
48 Lead Quad Flatpack F78
(Preliminary)



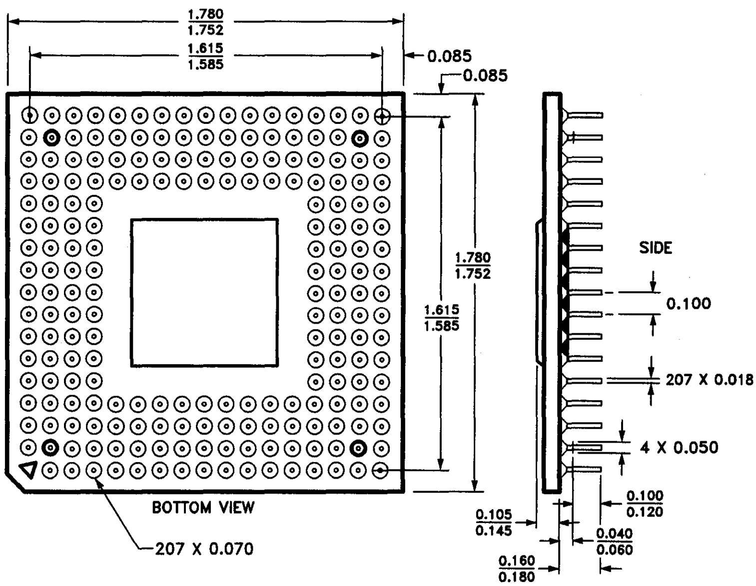
64 Lead Quad Flatpack F90
(Preliminary)



68 Pin Grid Array Package G68



207 Pin Grid Array G207



299 Pin Grid Array G299
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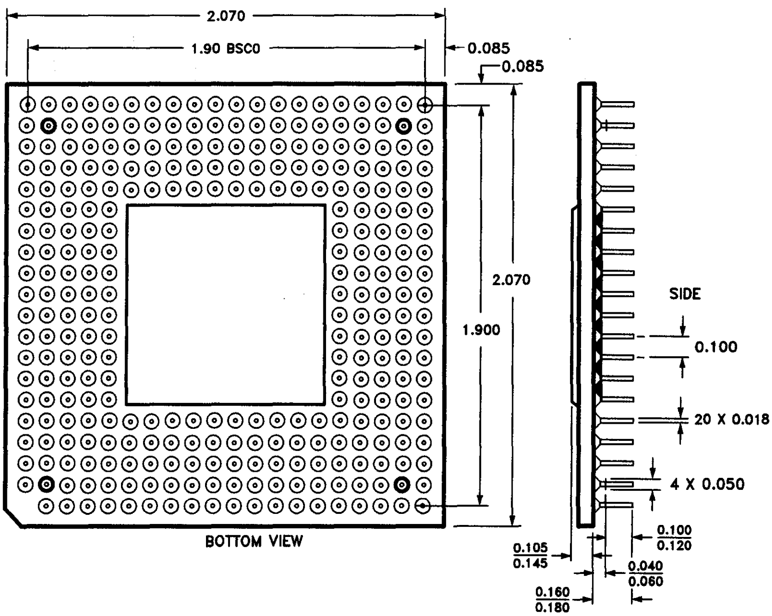
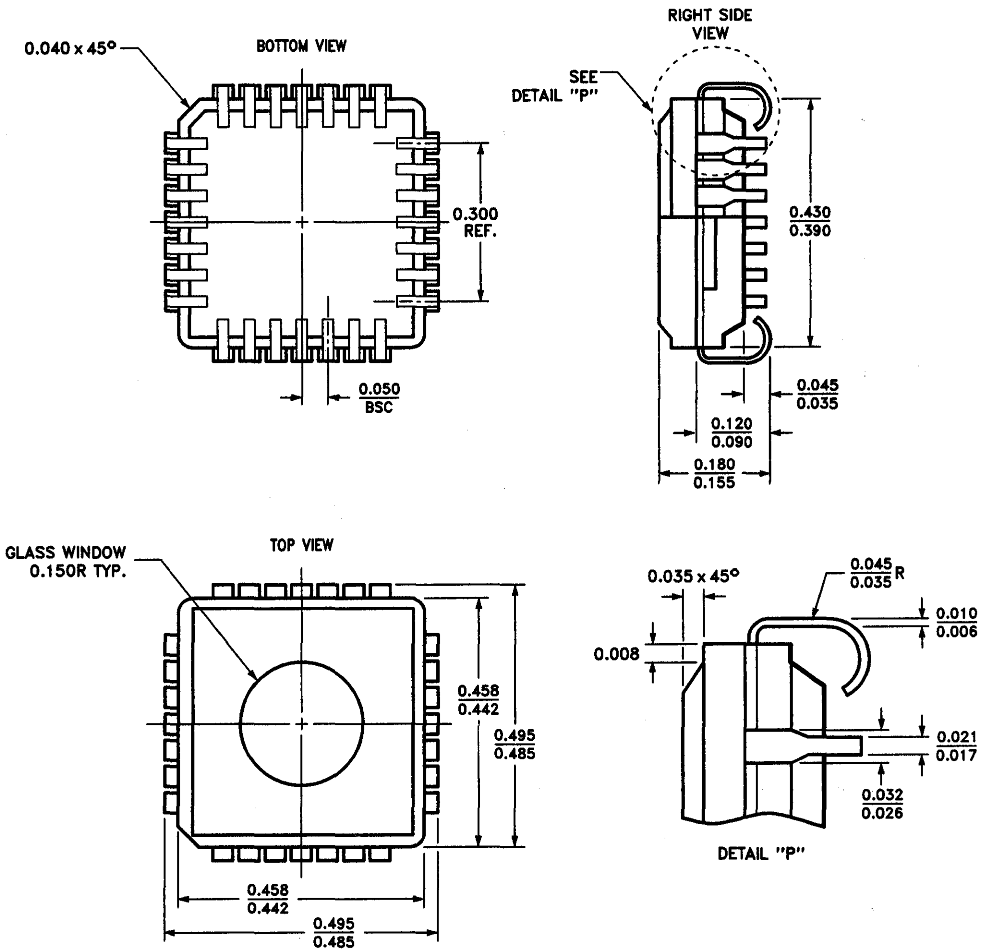
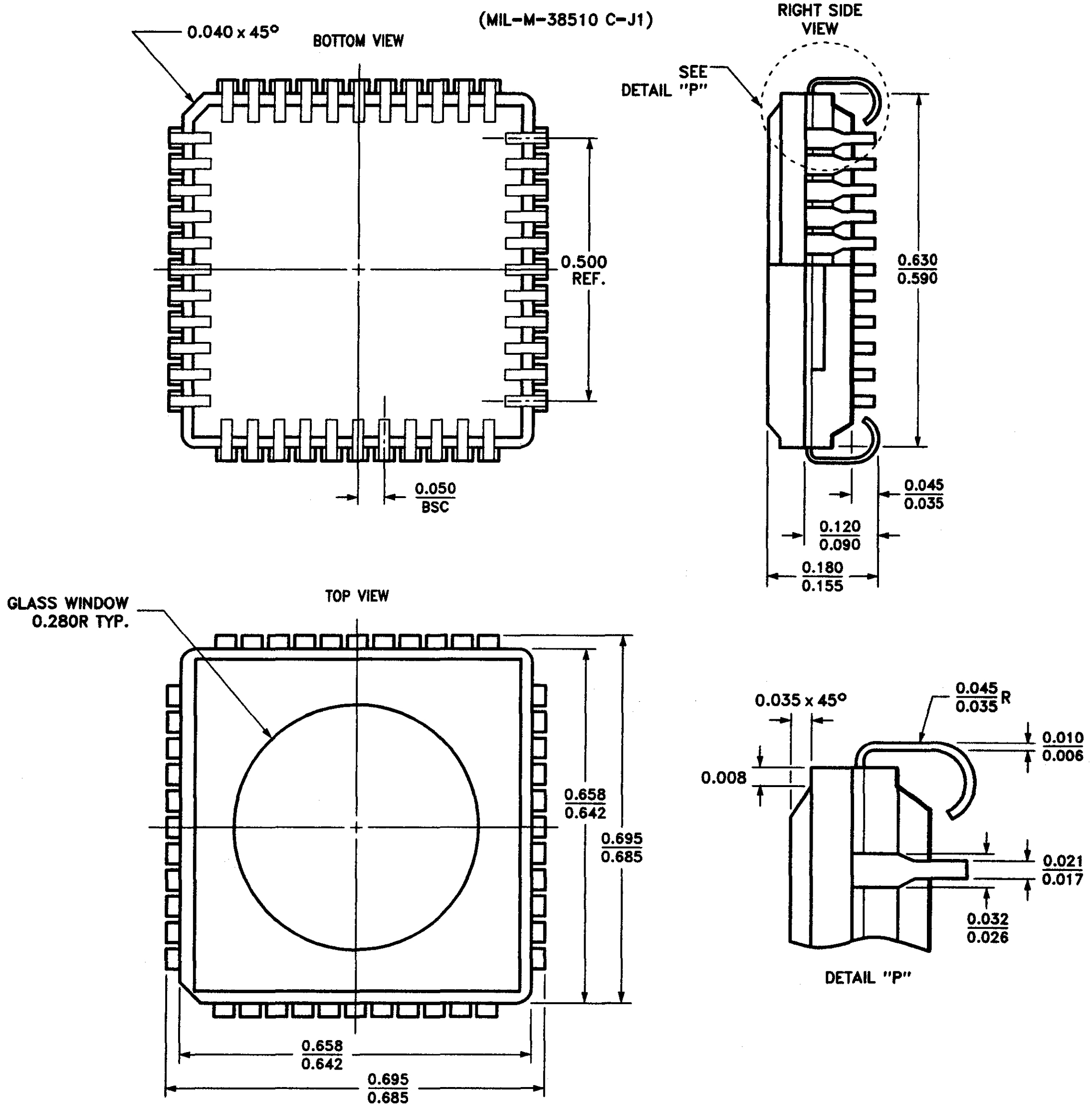


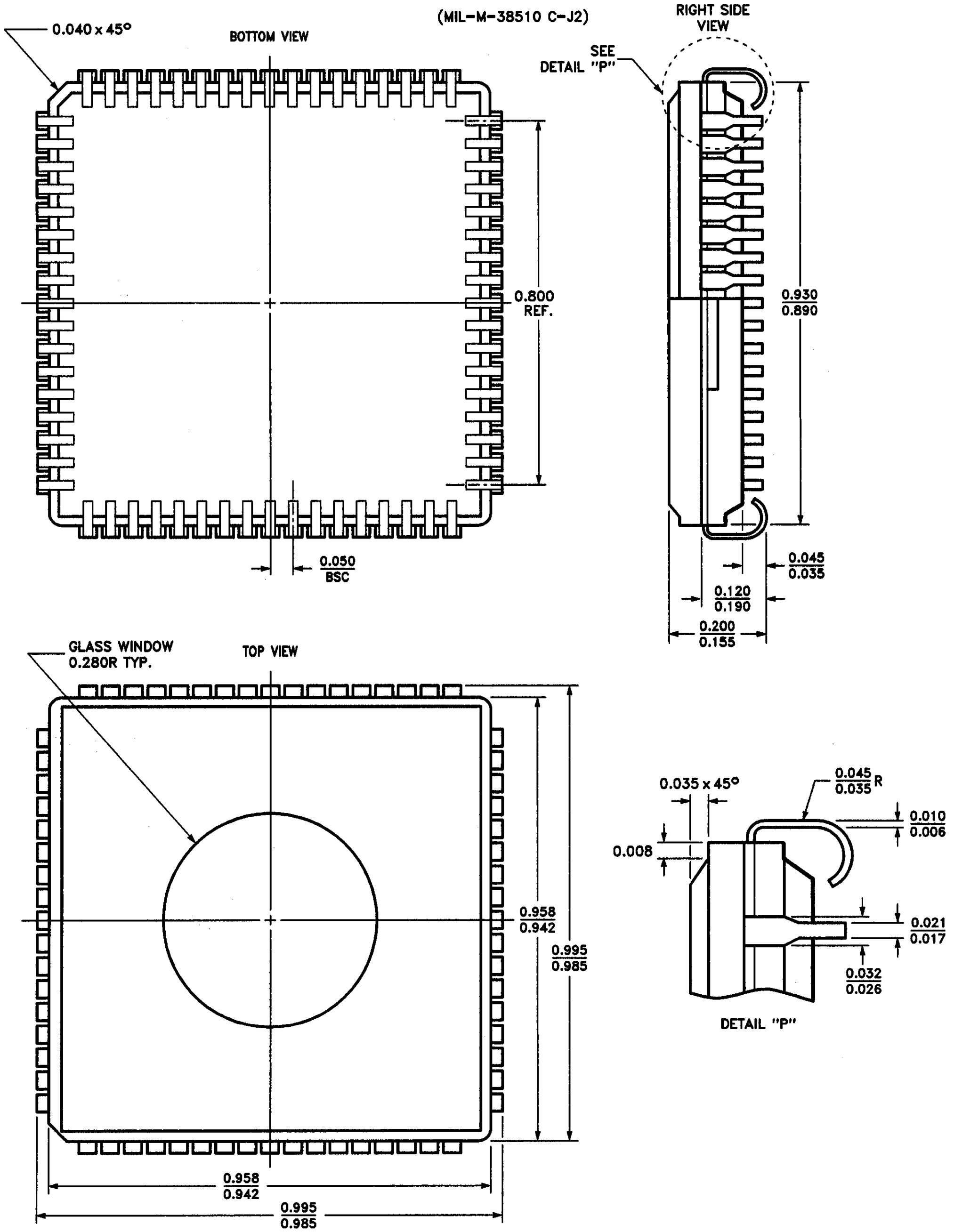
28 Pin Windowed Leaded Chip Carrier H64



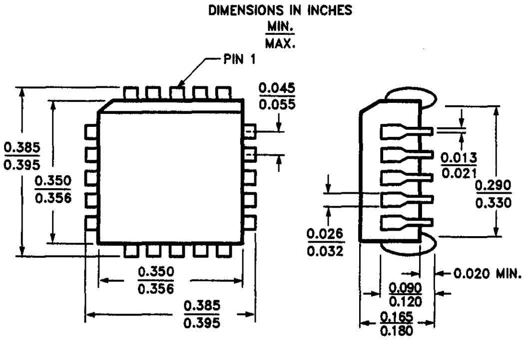
44 Pin Windowed Leaded Chip Carrier H67



68 Pin Windowed Leaded Chip Carrier H81



20 Lead Plastic Leadless Chip Carrier J61



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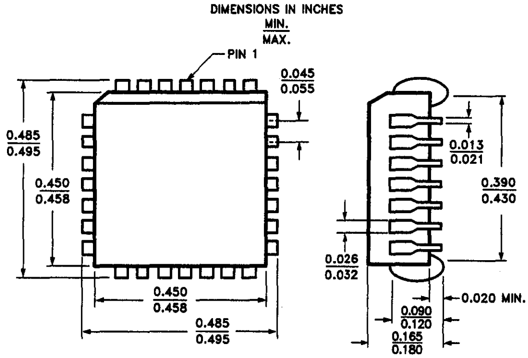
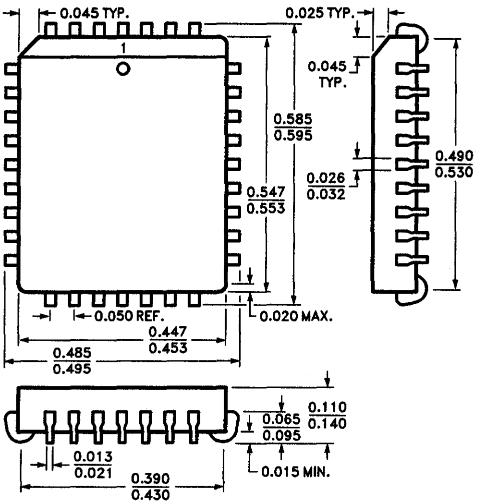
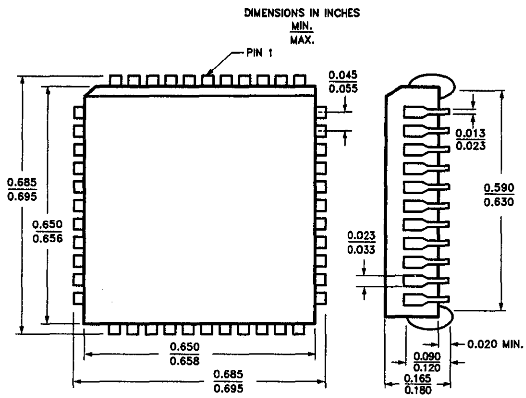


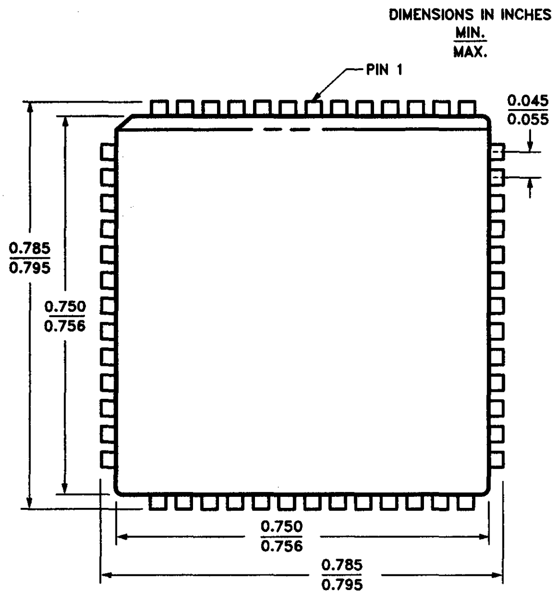
32 Lead Plastic Leadless Chip Carrier J65

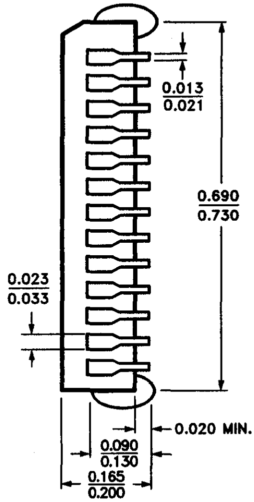


44 Lead Plastic Leadless Chip Carrier J67

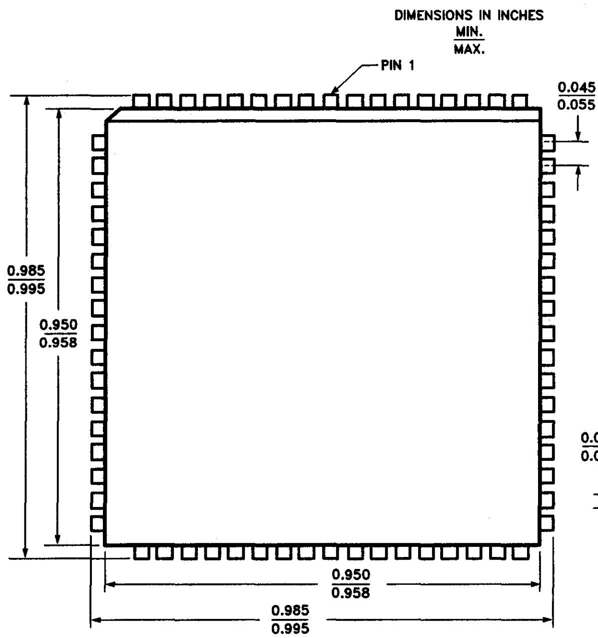


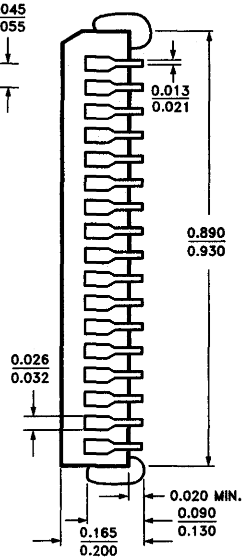
52 Lead Plastic Leadless Chip Carrier J69





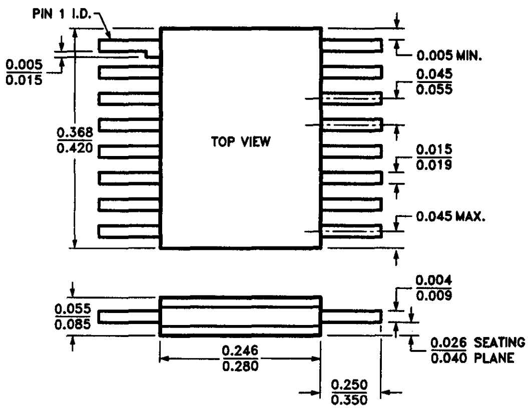
68 Lead Plastic Leadless Chip Carrier J81





16 Lead Rectangular Cerpack K69

(MIL-M-38510 F-5 CONFIG 1)



18 Lead Rectangular Cerpack K70

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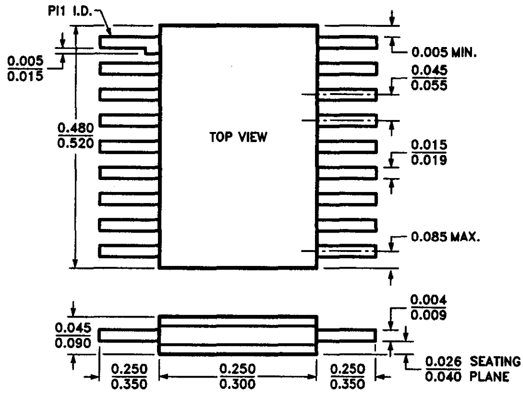
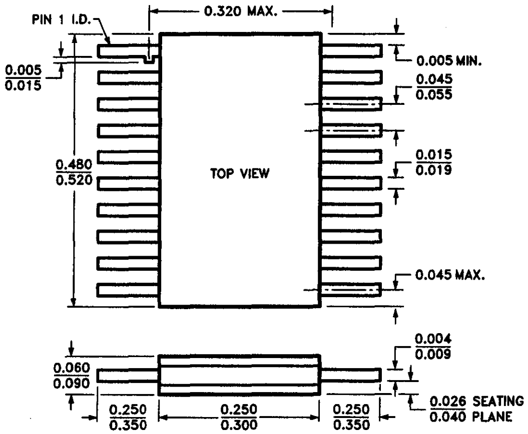


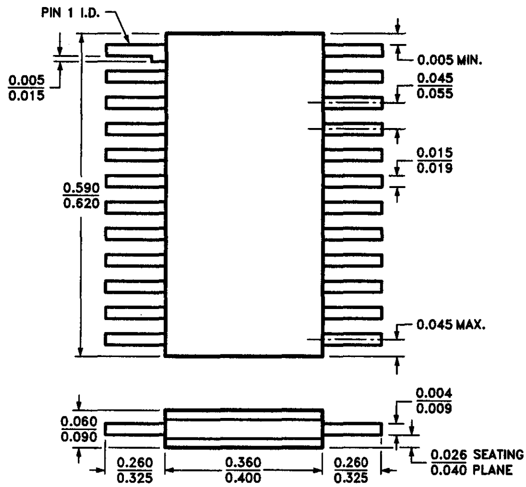
20 Lead Rectangular Cerpack K71

(MIL-M-38510 F-9 CONFIG 1)

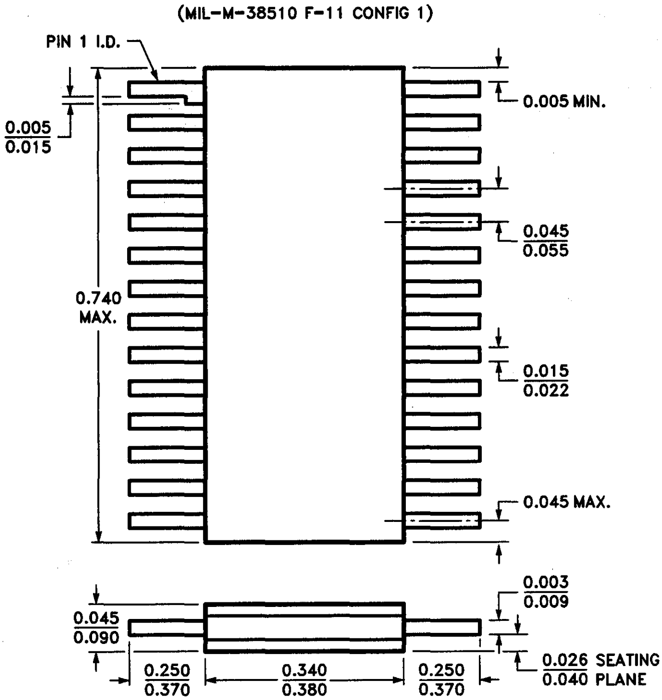


24 Lead Rectangular Cerpack K73

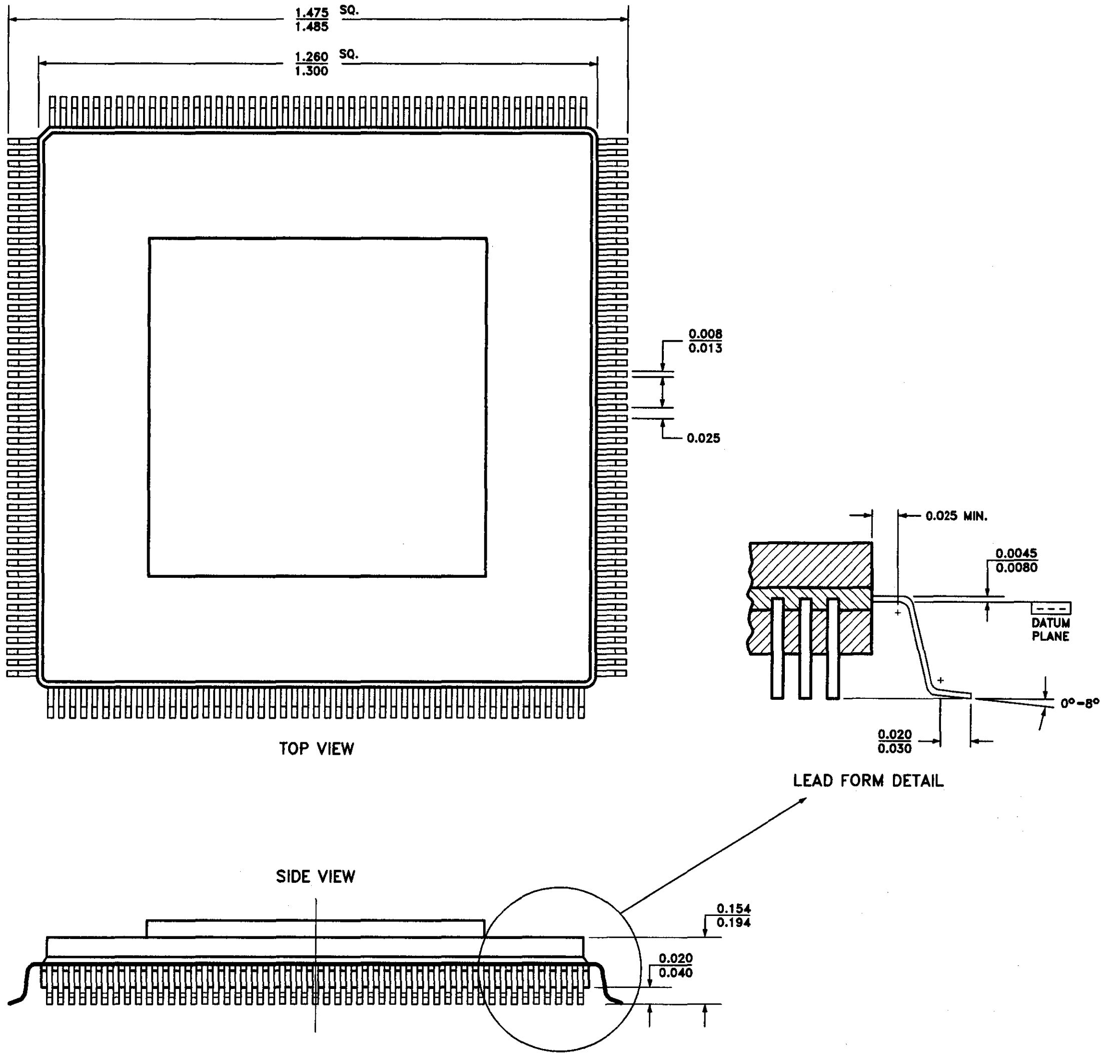
(MIL-M-38510 F-6 CONFIG 1)



28 Lead Rectangular Cerpack K74

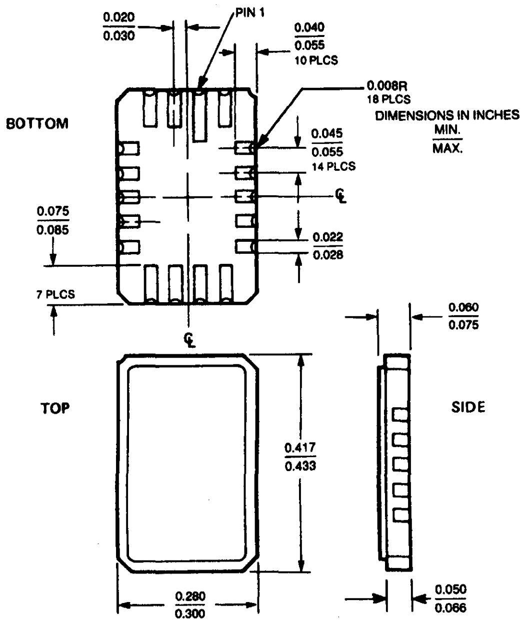


196 Lead Quad Flatpack Package K196



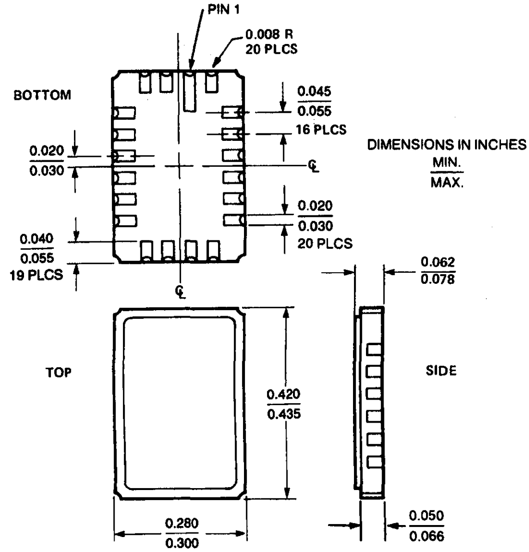
18 Pin Rectangular Leadless Chip Carrier L50

(MIL-M-38510 C-10A)

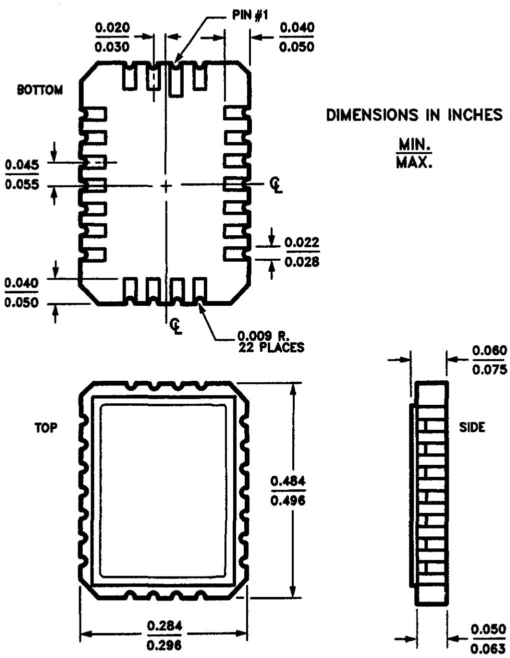


20 Pin Rectangular Leadless Chip Carrier L51

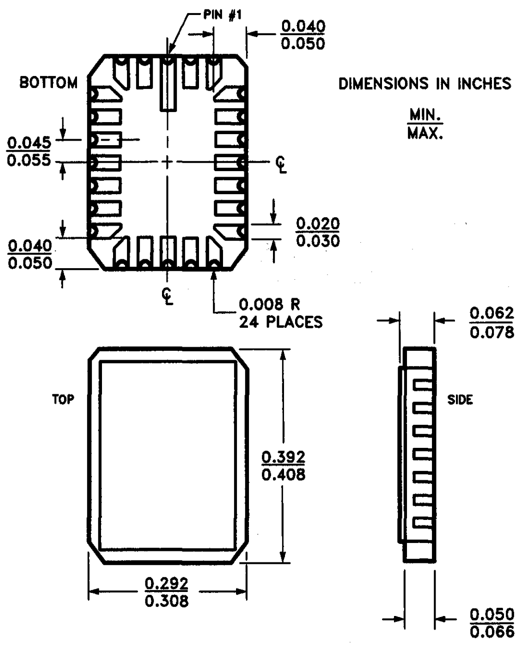
(MIL-M-38510 C-13)



22 Pin Rectangular Leadless Chip Carrier L52

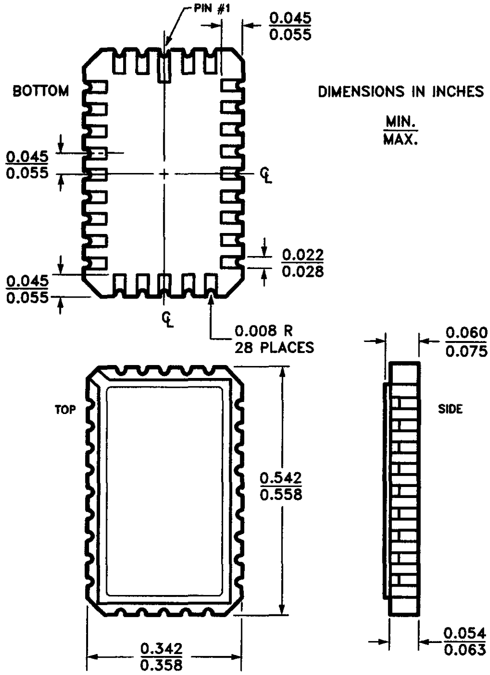


24 Pin Rectangular Leadless Chip Carrier L53



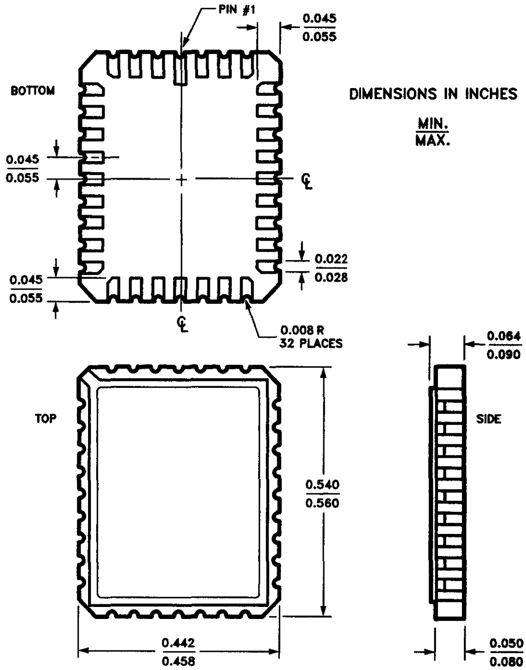
28 Pin Rectangular Leadless Chip Carrier L54

(MIL-M-38510 C-11A)



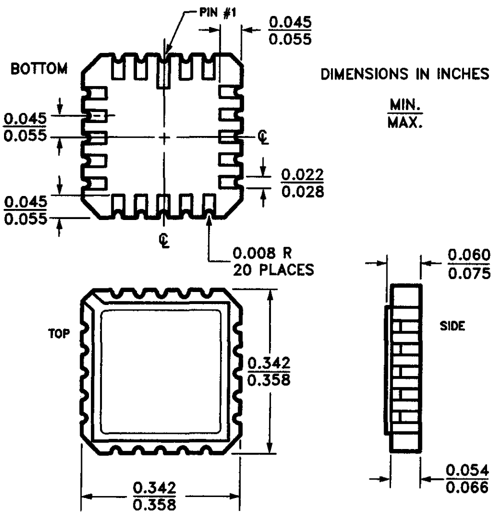
32 Pin Rectangular Leadless Chip Carrier L55

(MIL-M-38510 C-12)

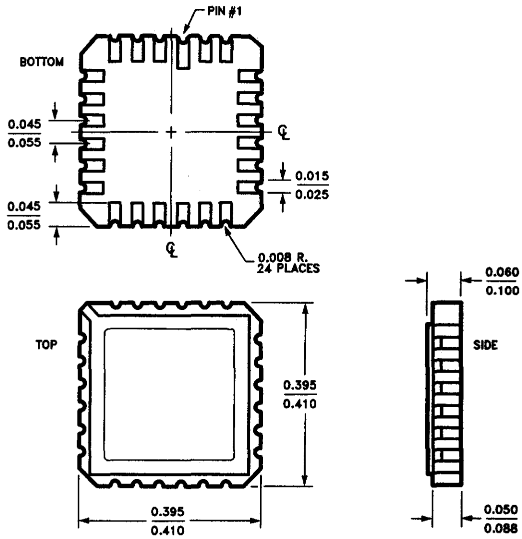


20 Pin Square Leadless Chip Carrier L61

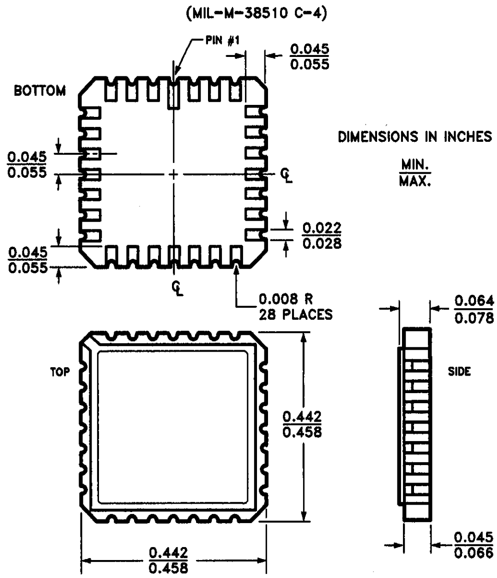
(MIL-M-38510 C-2A)



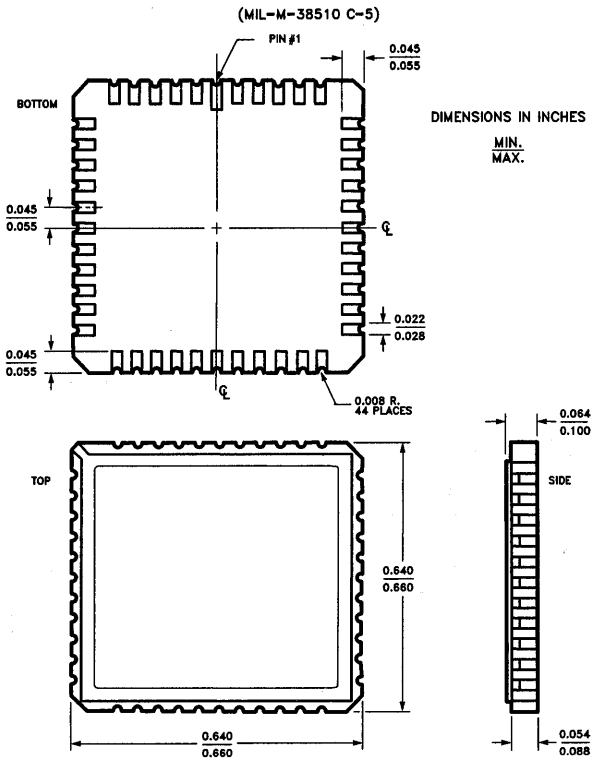
24 Pin Square Leadless Chip Carrier L63



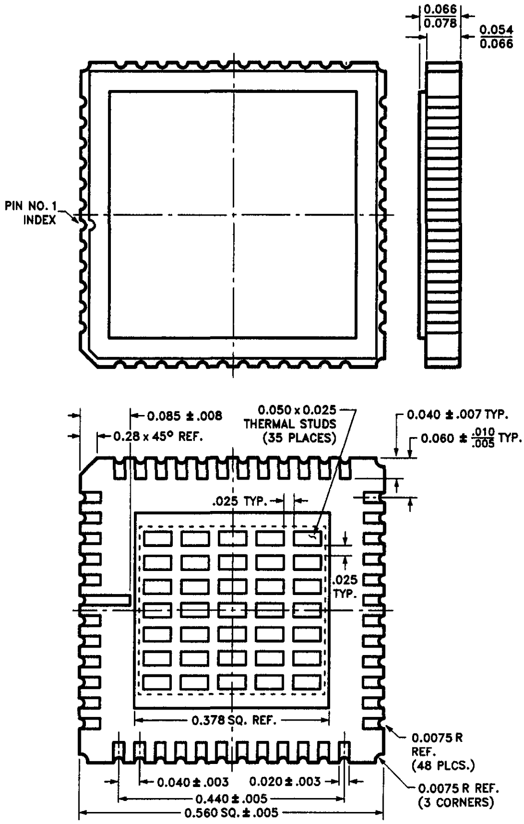
28 Pin Square Leadless Chip Carrier L64



44 Pin Square Leadless Chip Carrier L67

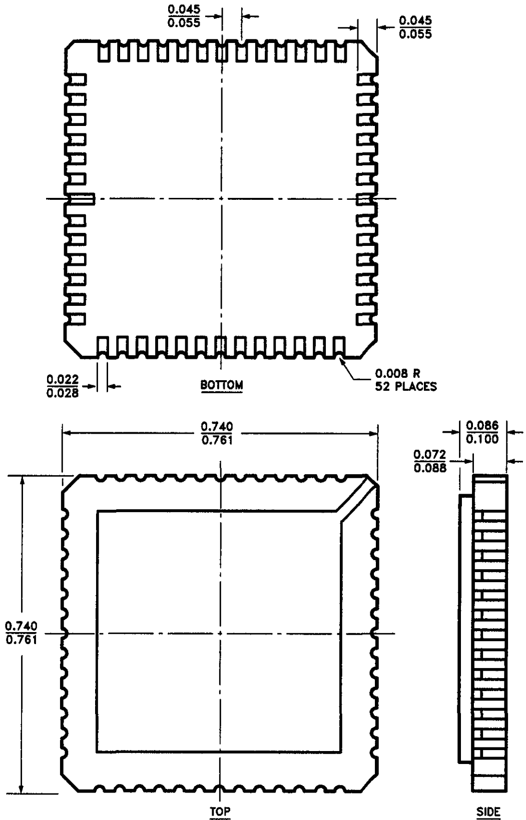


48 Pin Square Leadless Chip Carrier L68

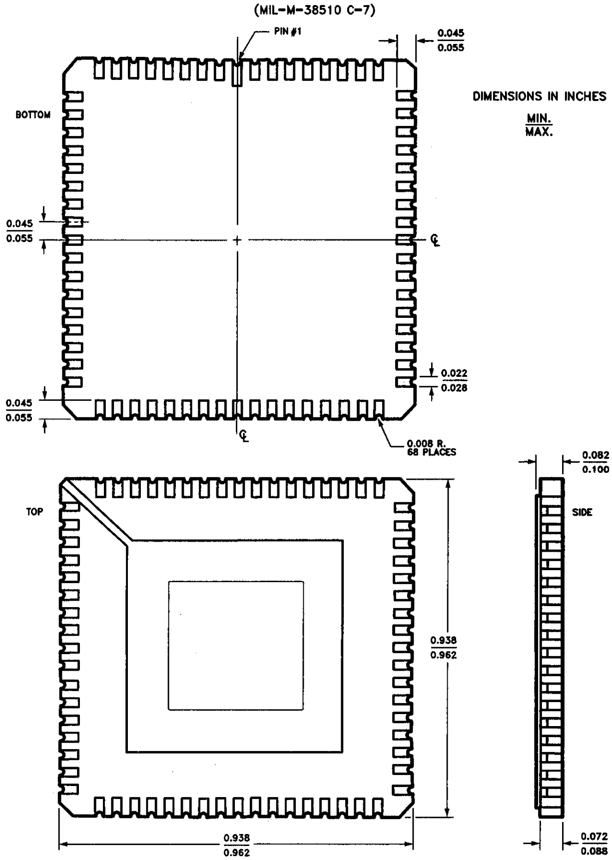


Note:
Thermal studs not used on DESC approved SMD products. If other products ordered cannot have thermal studs, contact your local sales office for special arrangements.

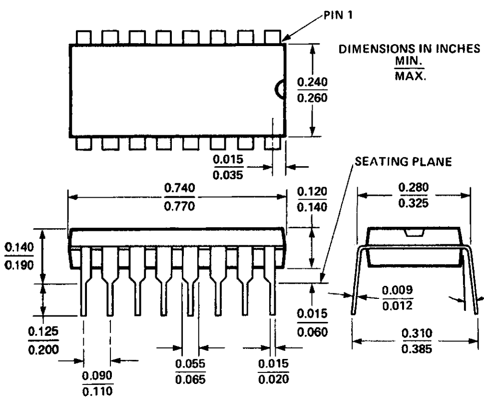
52 Pin Square Leadless Chip Carrier L69



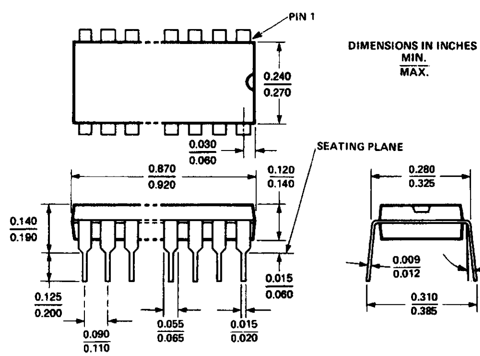
68 Pin Square Leadless Chip Carrier L81



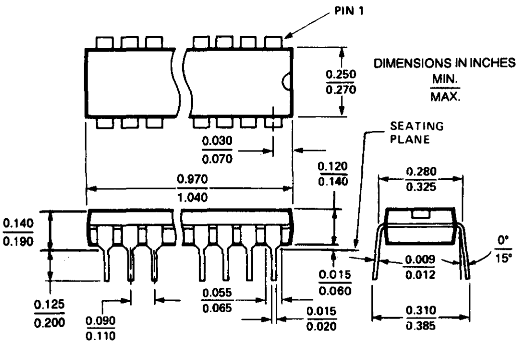
16 Lead (300 MIL) Molded DIP P1



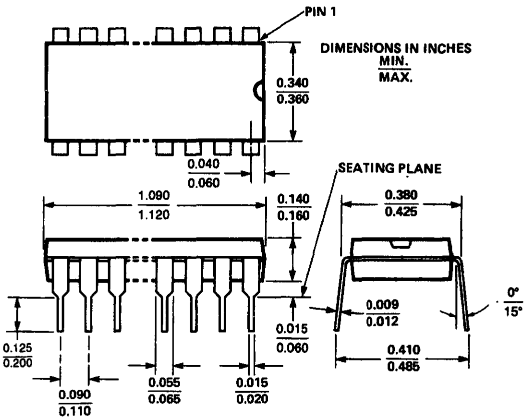
18 Lead (300 MIL) Molded DIP P3



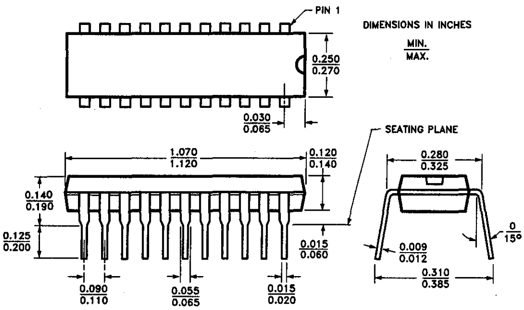
20 Lead (300 MIL) Molded DIP P5



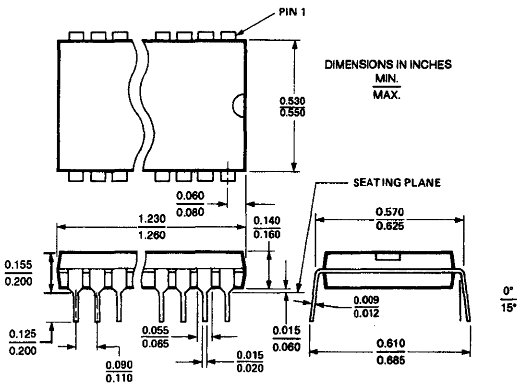
22 Lead (400 MIL) Molded DIP P7



22 Lead (300 MIL) Molded DIP P9

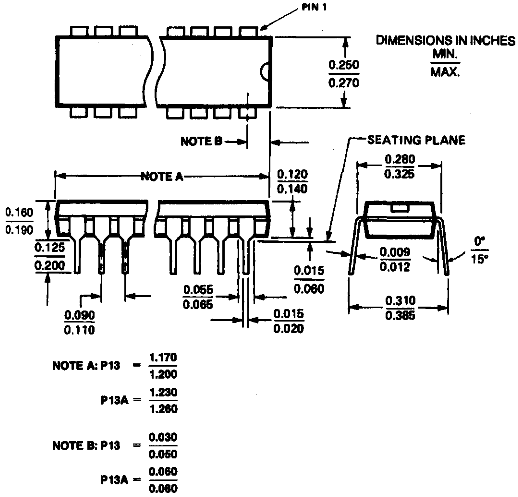


24 Lead (600 MIL) Molded DIP P11

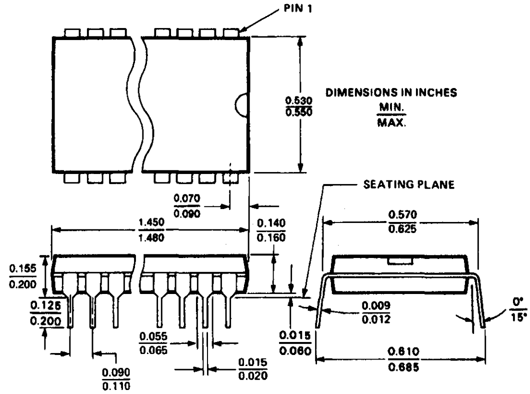


14

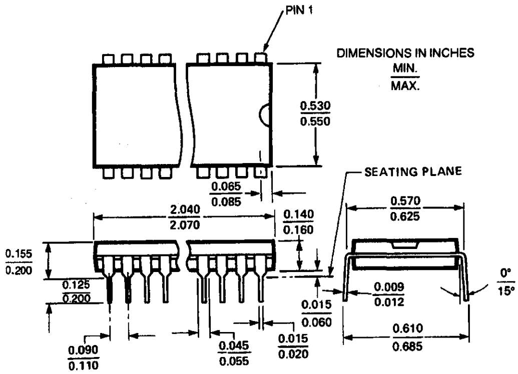
24 Lead (300 MIL) Molded DIP P13/P13A



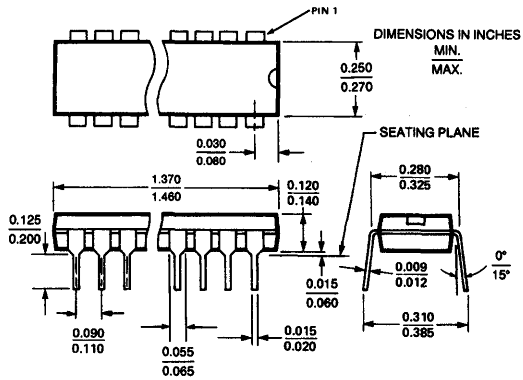
28 Lead (600 MIL) Molded DIP P15



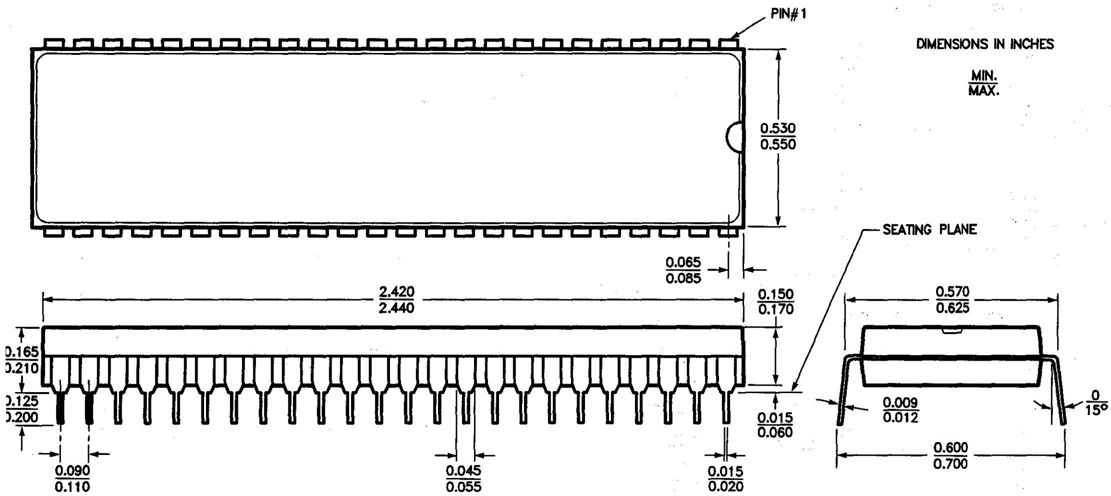
40 Lead (600 MIL) Molded DIP P17



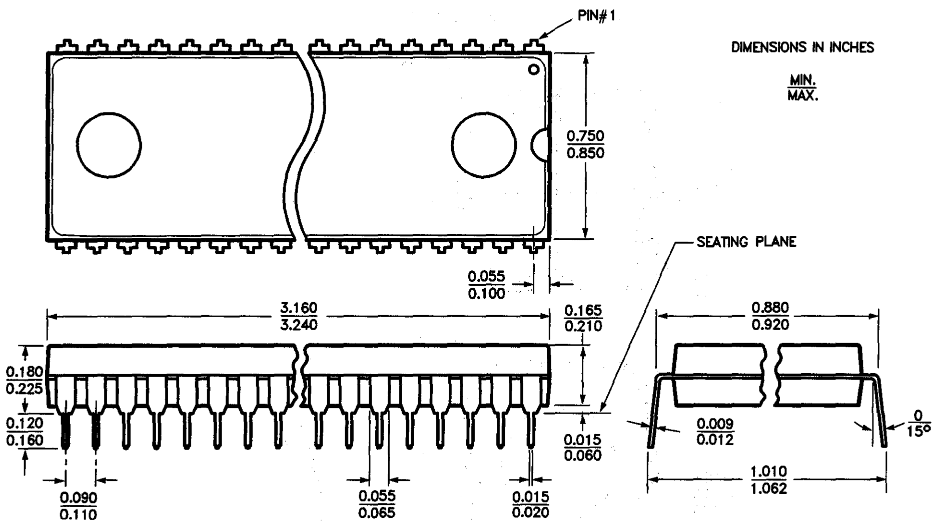
28 Lead (300 MIL) Molded DIP P21



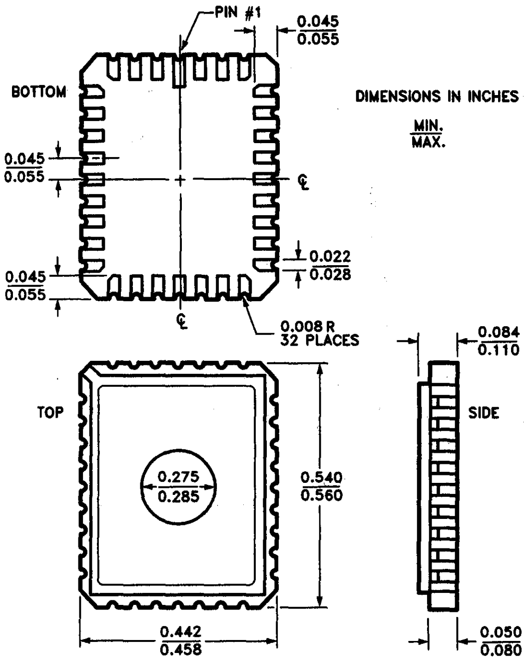
48 Lead (600 MIL) Molded DIP P25



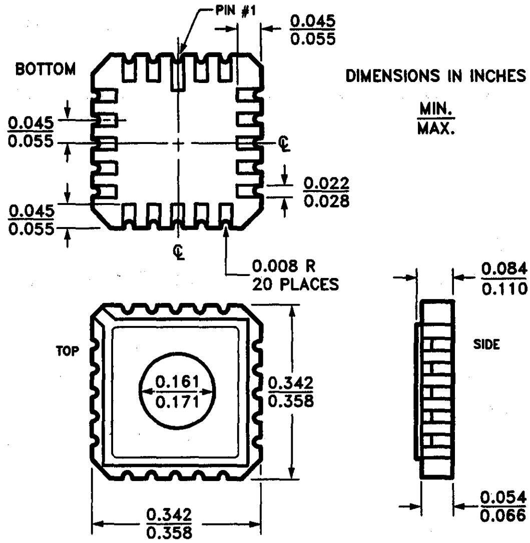
64 Lead (900 MIL) Molded DIP P29



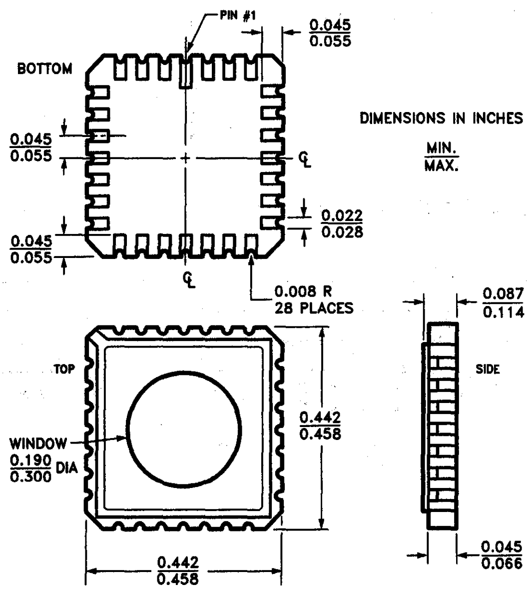
32 Pin Windowed Rectangular Leadless Chip Carrier Q55



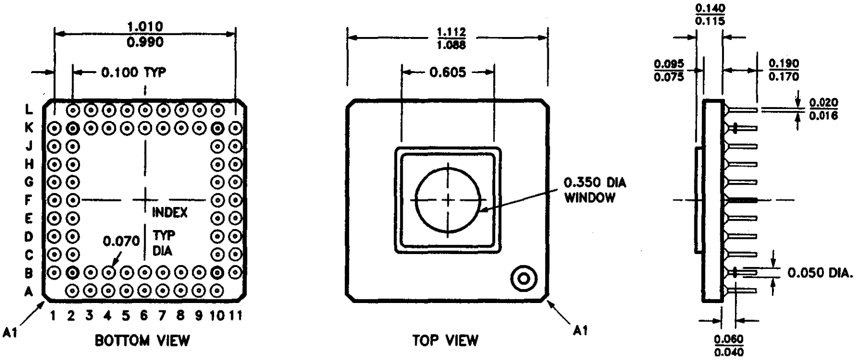
20 Pin Windowed Square Leadless Chip Carrier Q61



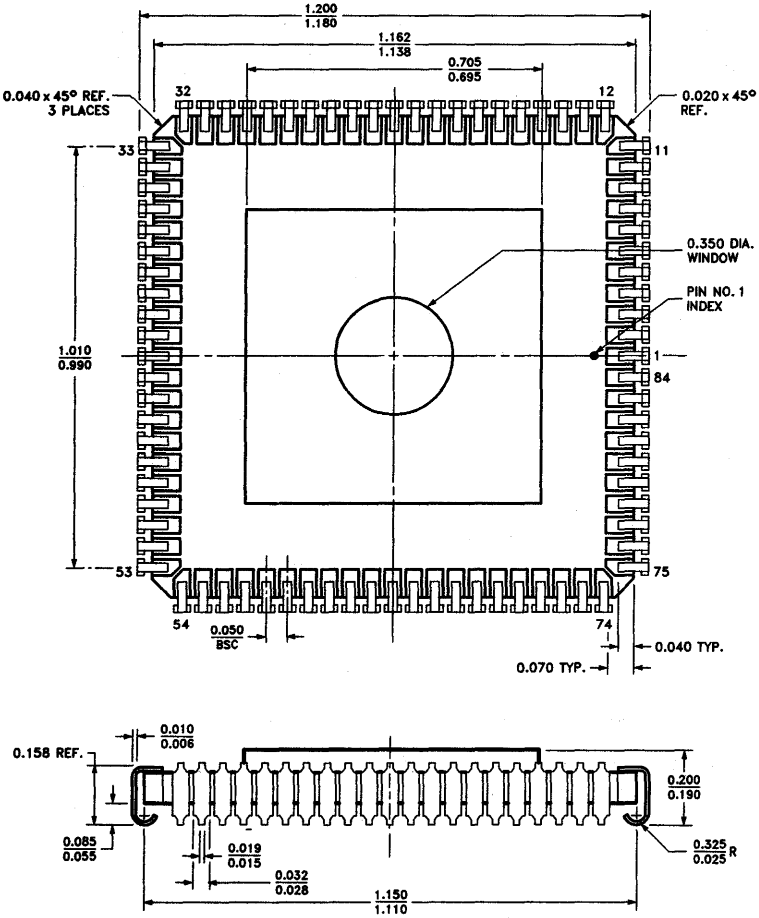
28 Pin Windowed Leadless Chip Carrier Q64



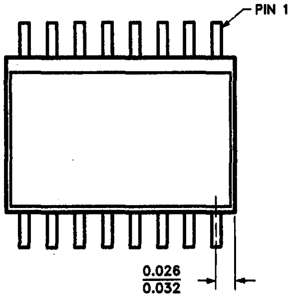
68 Pin Windowed PGA Ceramic R68



84 Pin J-Leaded Ceramic Chip Carrier R84



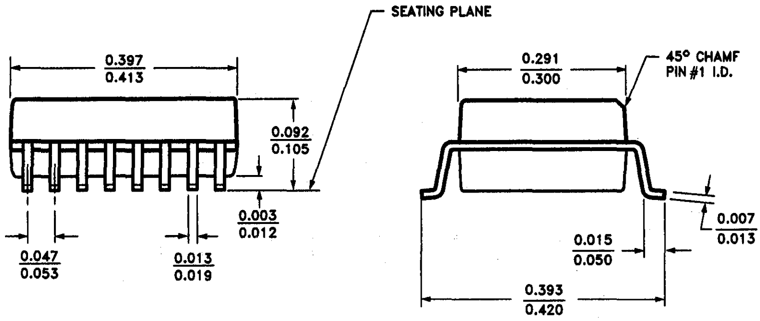
16 Lead Molded SOIC S1



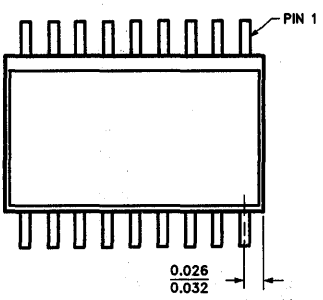
DIMENSIONS IN INCHES

MIN.
MAX.

LEAD COPLANIARITY 0.004 MAX.



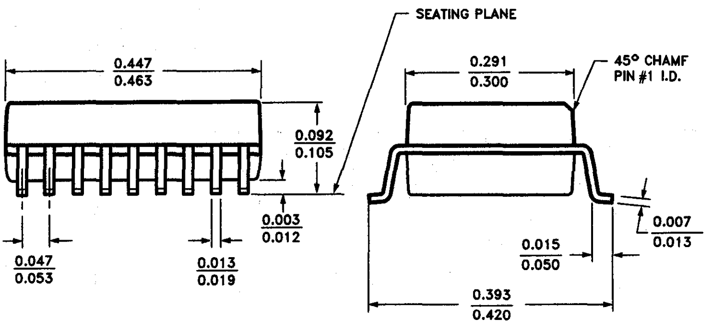
18 Lead Molded SOIC S3



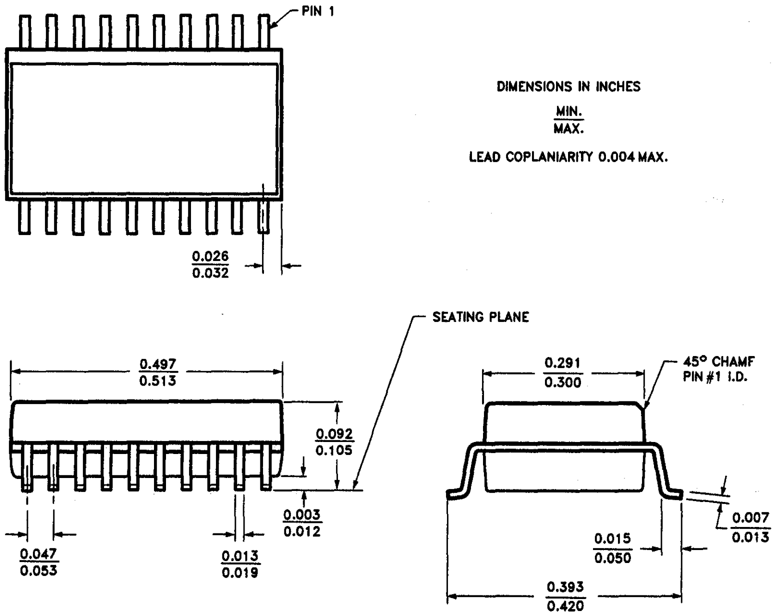
DIMENSIONS IN INCHES

MIN.
MAX.

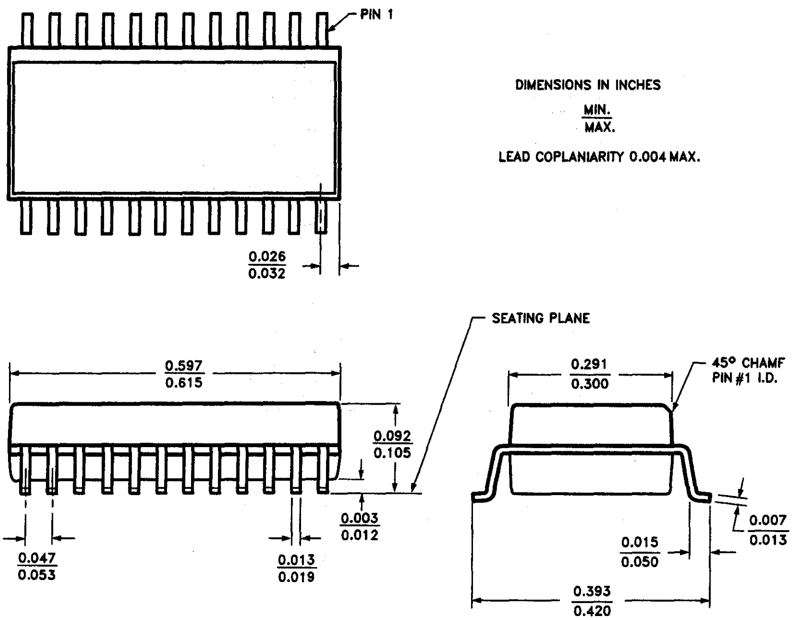
LEAD COPLANIARITY 0.004 MAX.



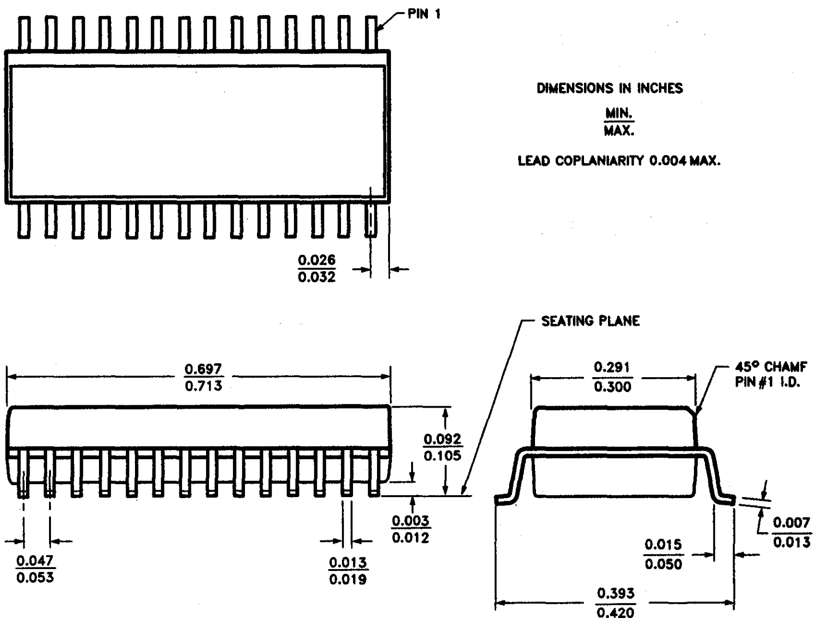
20 Lead Molded SOIC S5



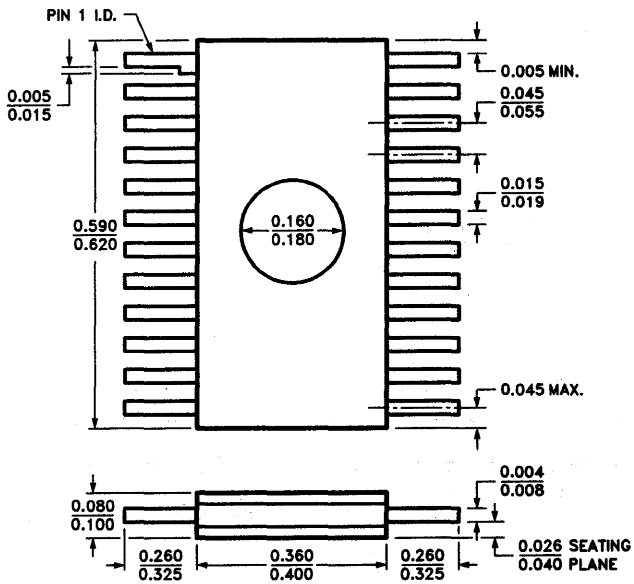
24 Lead Molded SOIC S13



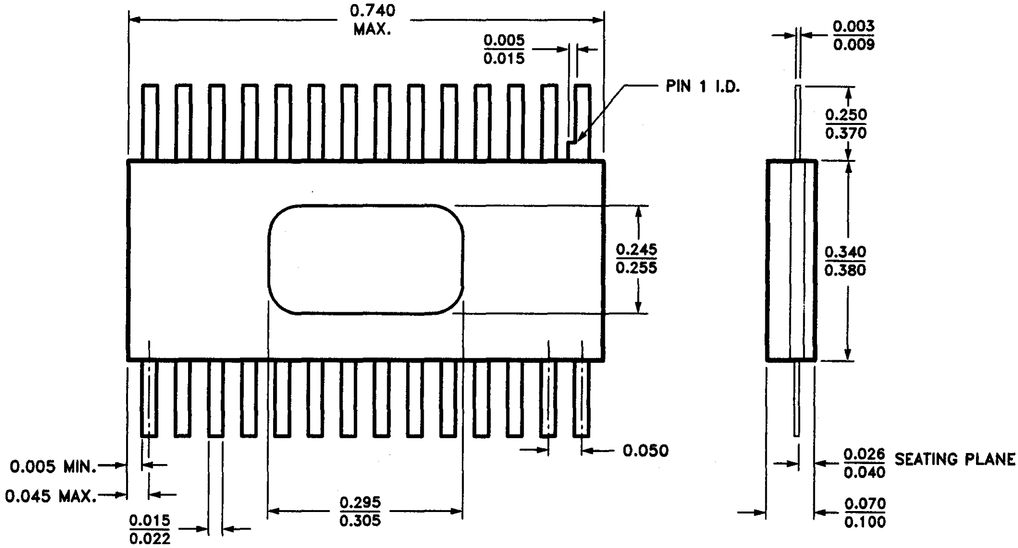
28 Lead Molded SOIC S21



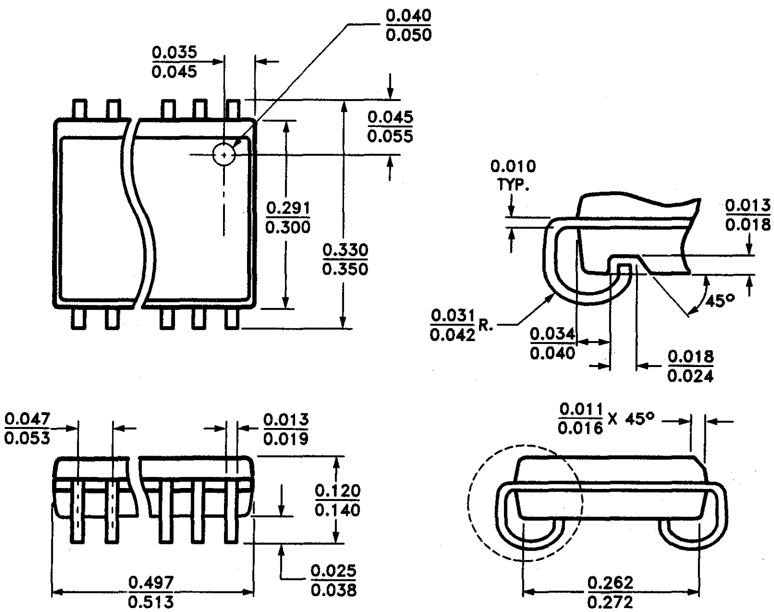
24 Lead Windowed Cerpack T73



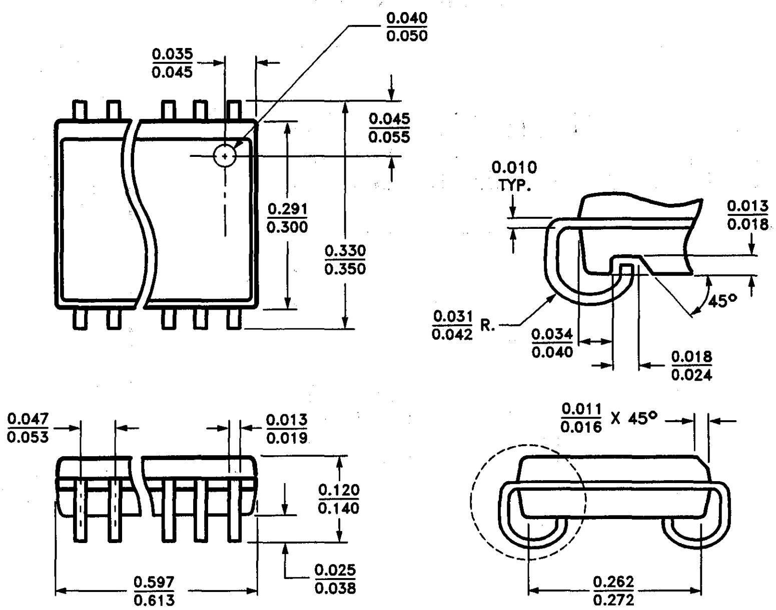
28 Lead Windowed Cerpack T74



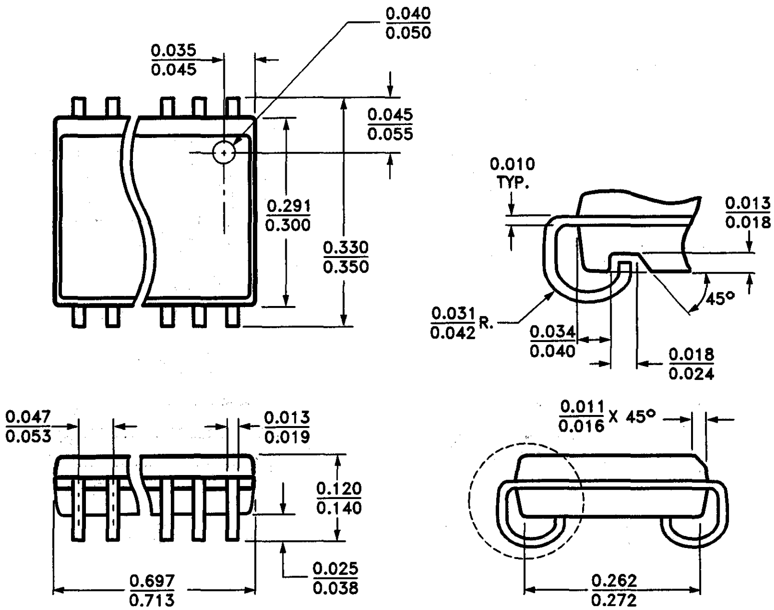
20 Lead Molded SOJ V5



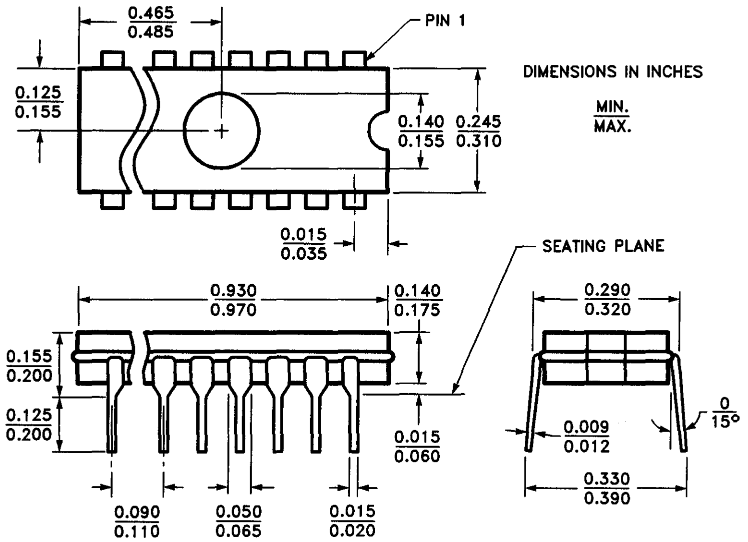
24 Lead Molded SOJ V13



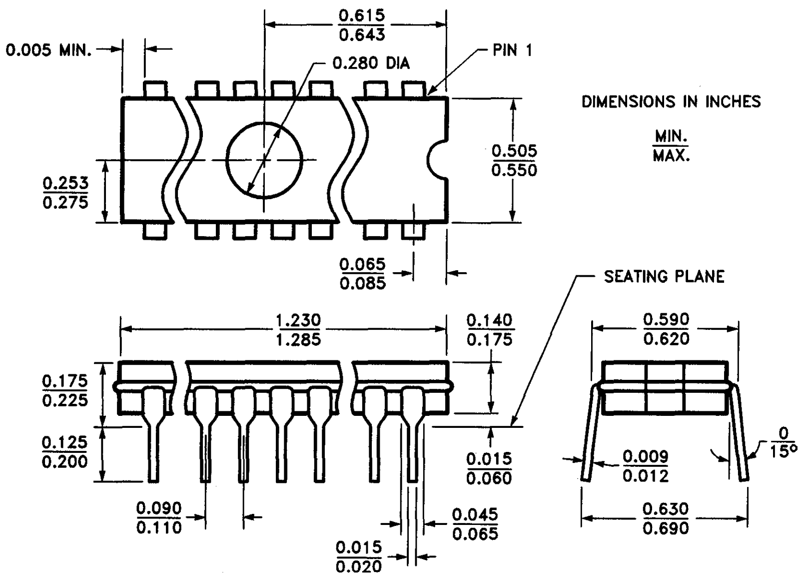
28 Lead Molded SOJ V21



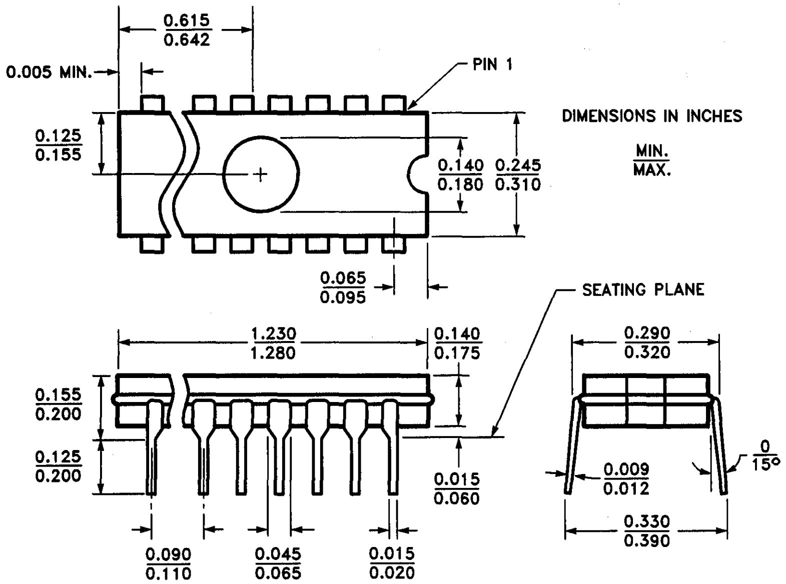
20 Lead (300 MIL) Windowed Cerdip W6



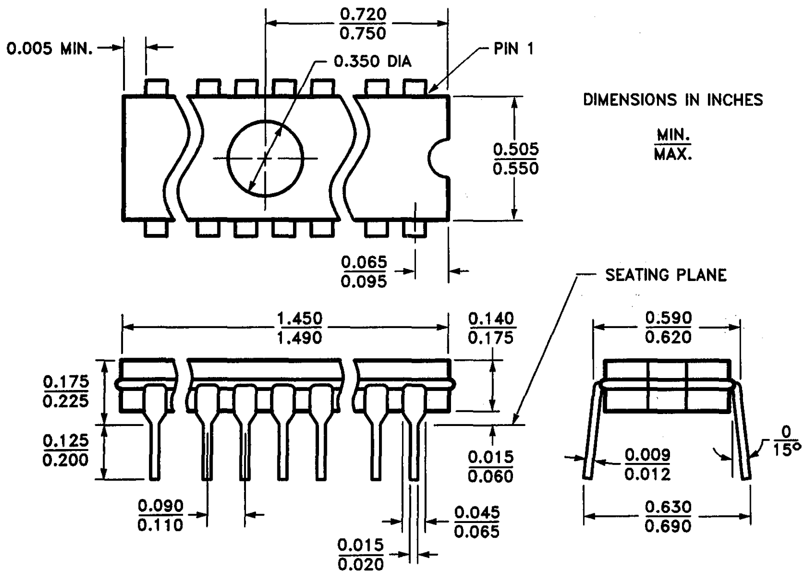
24 Lead (600 MIL) Windowed Cerdip W12



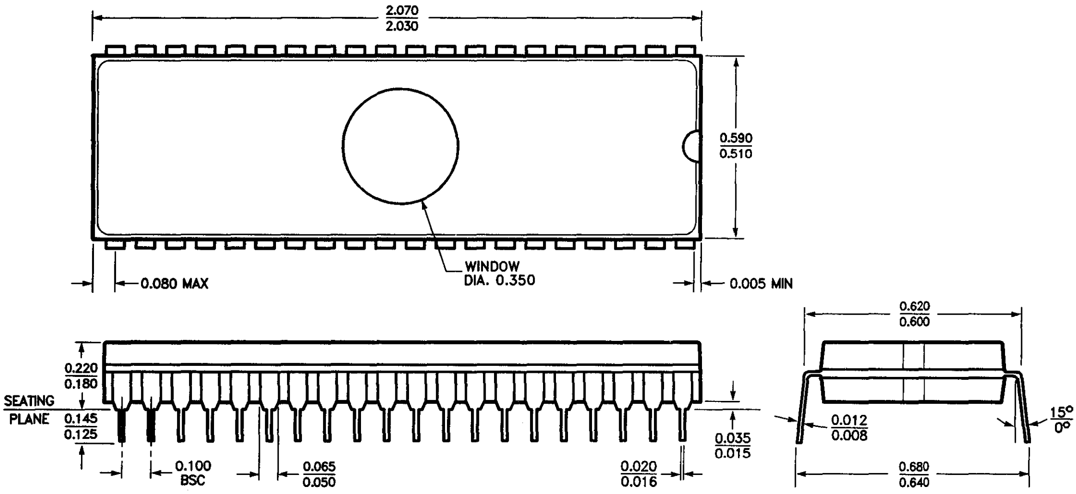
24 Lead (300 MIL) Windowed Cerdip W14



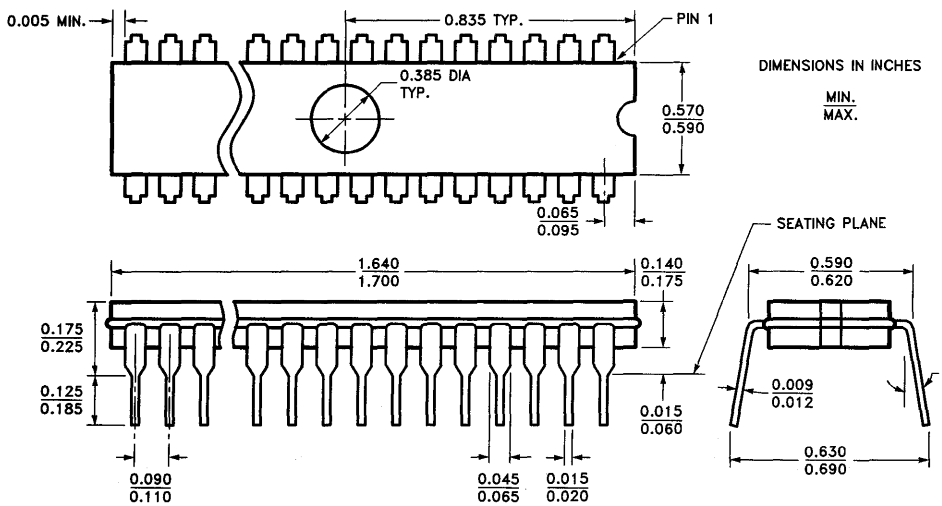
28 Lead (600 MIL) Windowed Cerdip W16



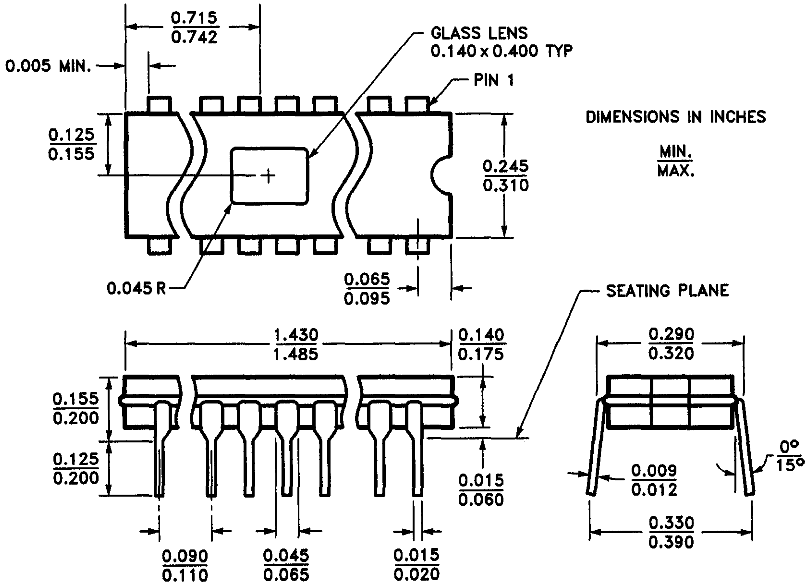
40 Lead (600 MIL) Windowed Cerdip W18



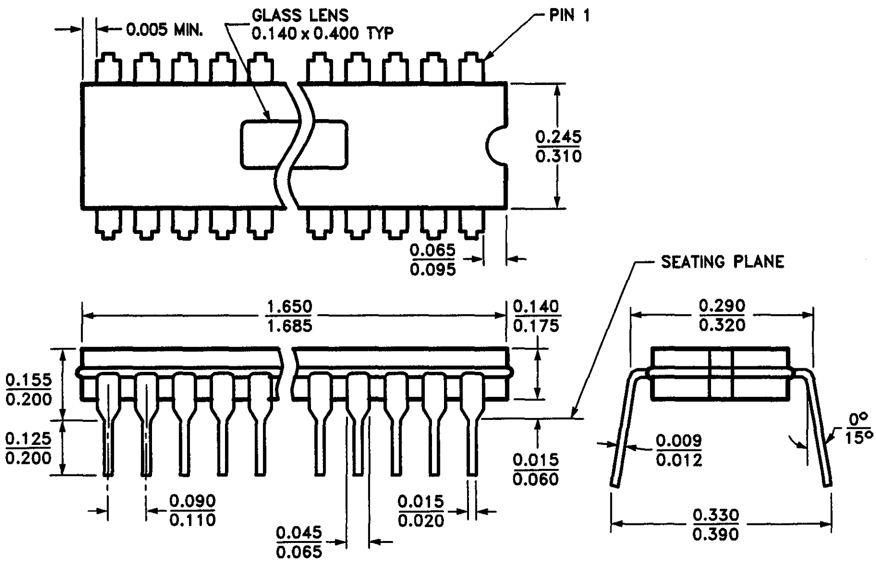
32 Lead (600 MIL) Windowed Cerdip W20



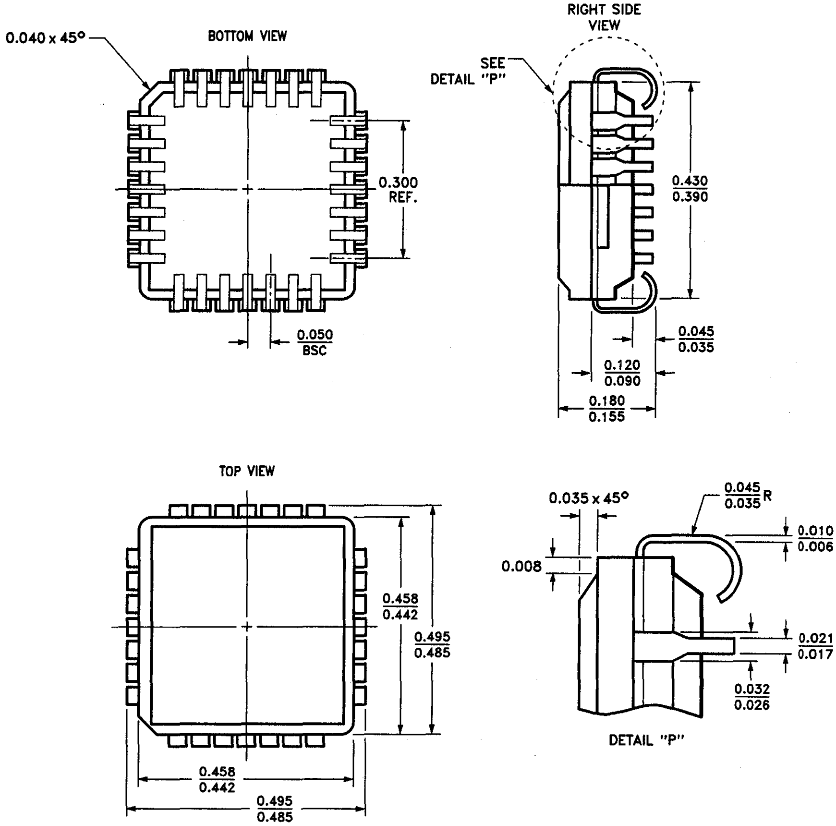
28 Lead (300 MIL) Windowed Cerdip W22



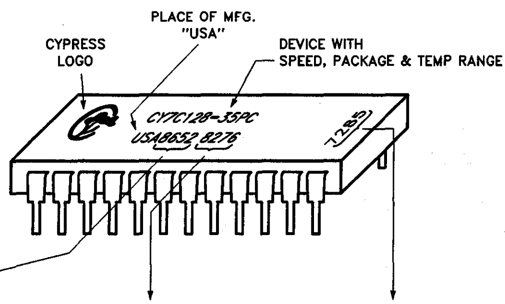
32 Lead (300 MIL) Windowed Cerdip W32



28 Pin Ceramic Leaded Chip Carrier Y64



Typical Marking for DIP Packages (P and D Type)



DATE CODE:

XXYY
XX = YEAR
YY = WORK WEEK
WEEK PARTS WERE MARKED (FOR PLASTIC)
WEEK PARTS WERE SEALED (FOR HERMETIC)

SHIP CODE:

IDENTIFIES SPECIFIC SHIPMENT LOTS TO CUSTOMERS.

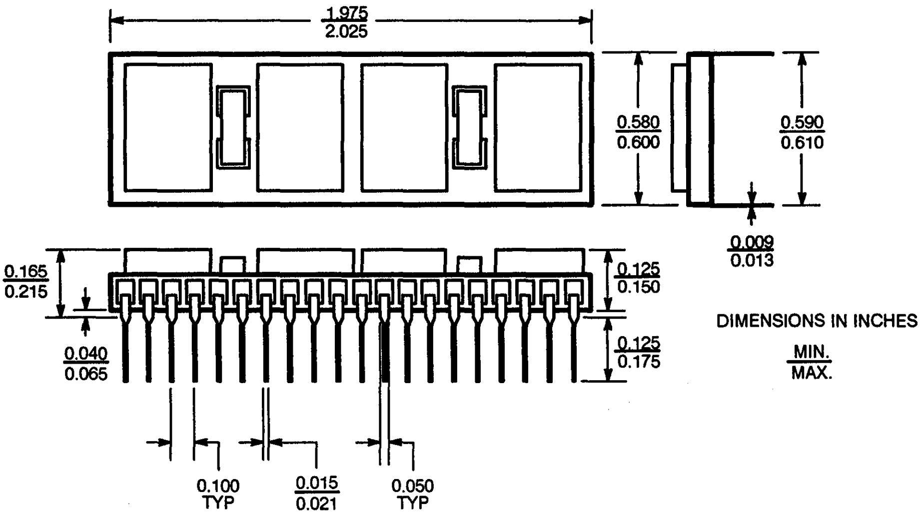
ASSEMBLY CODE:

IDENTIFIES THE SPECIFIC ASSEMBLY LOT THE PRODUCT CAME FROM.

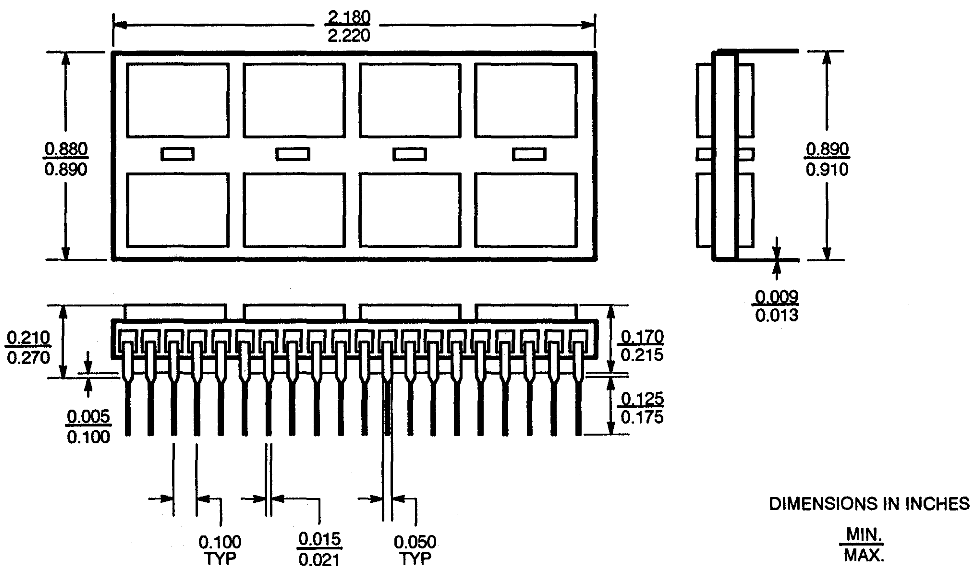
0047-1

Package Diagrams for Modules

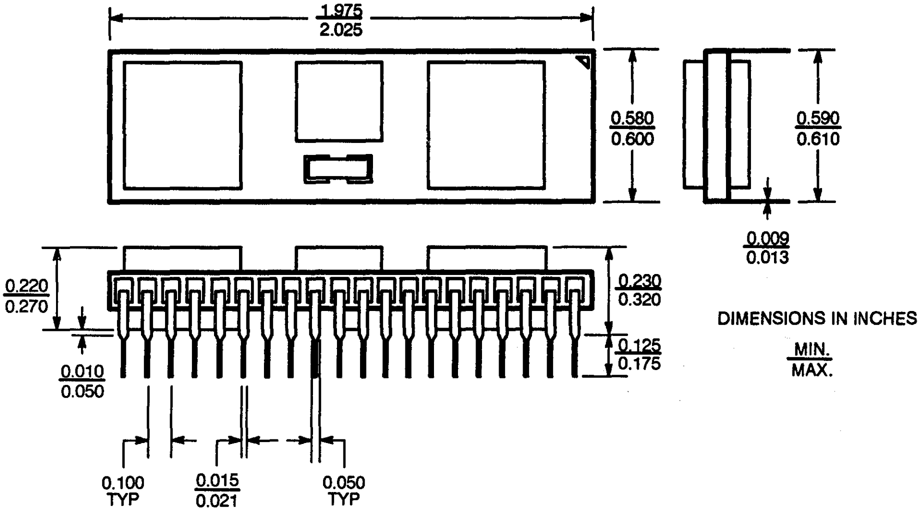
40-Pin DIP Module HD01



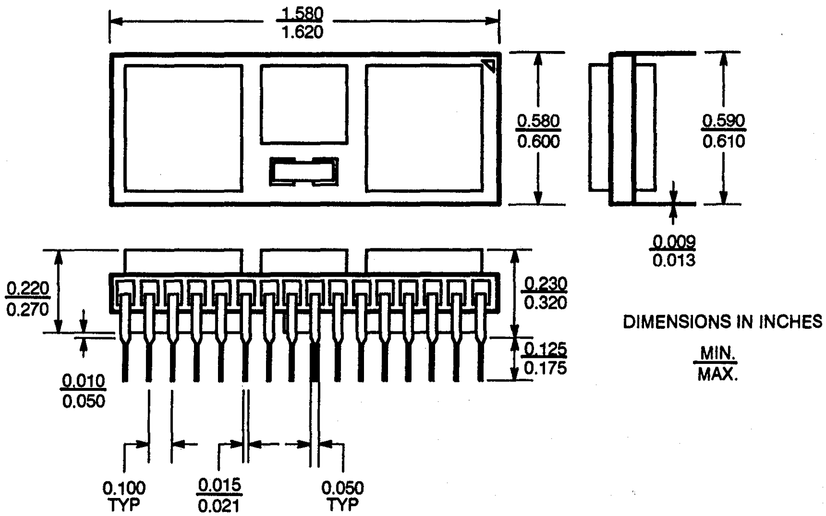
40-Pin Ceramic DIP Module HD02



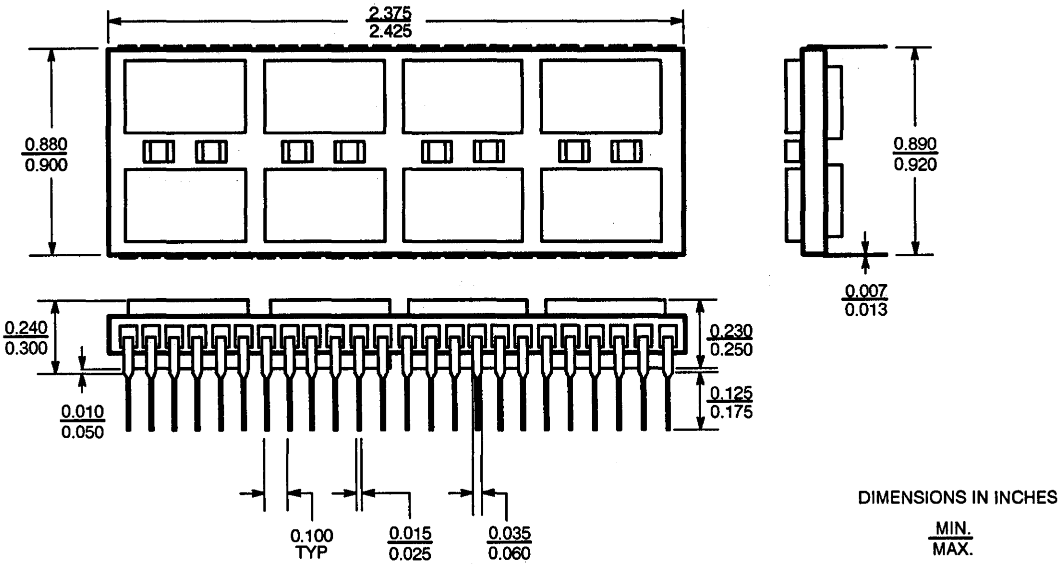
40-Pin DIP Module HD03



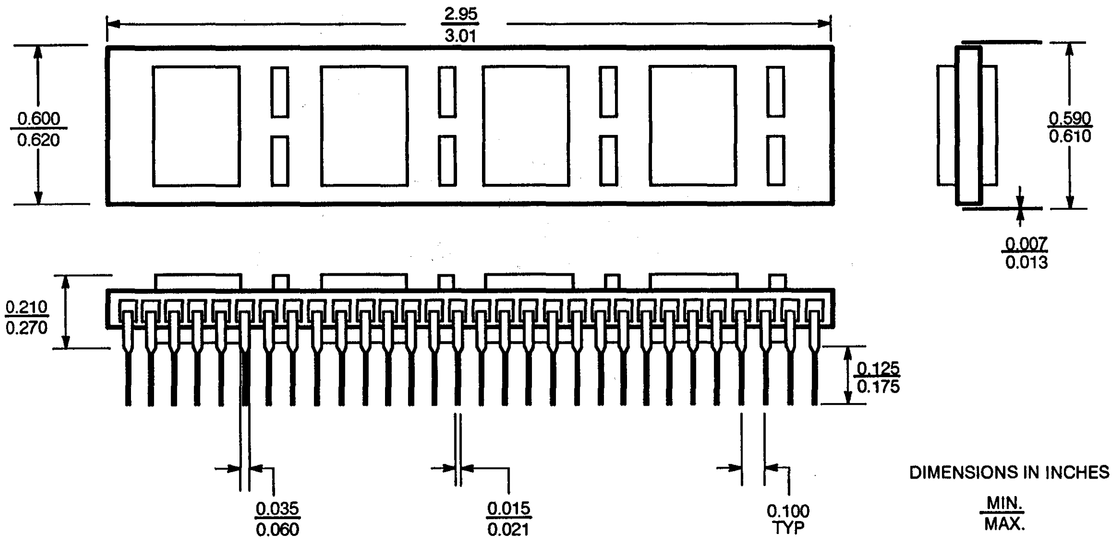
32-Pin DIP Module HD04



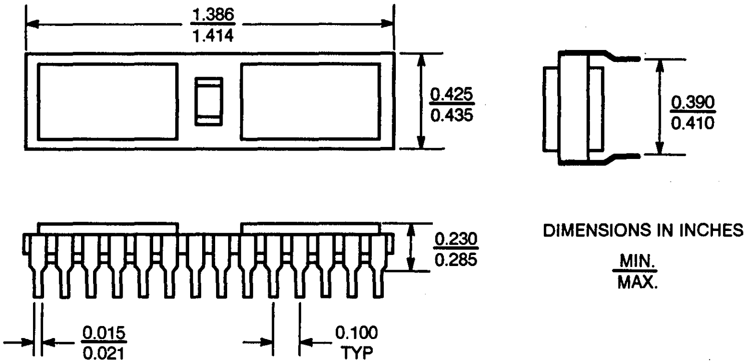
48-Pin Ceramic DIP Module HD05



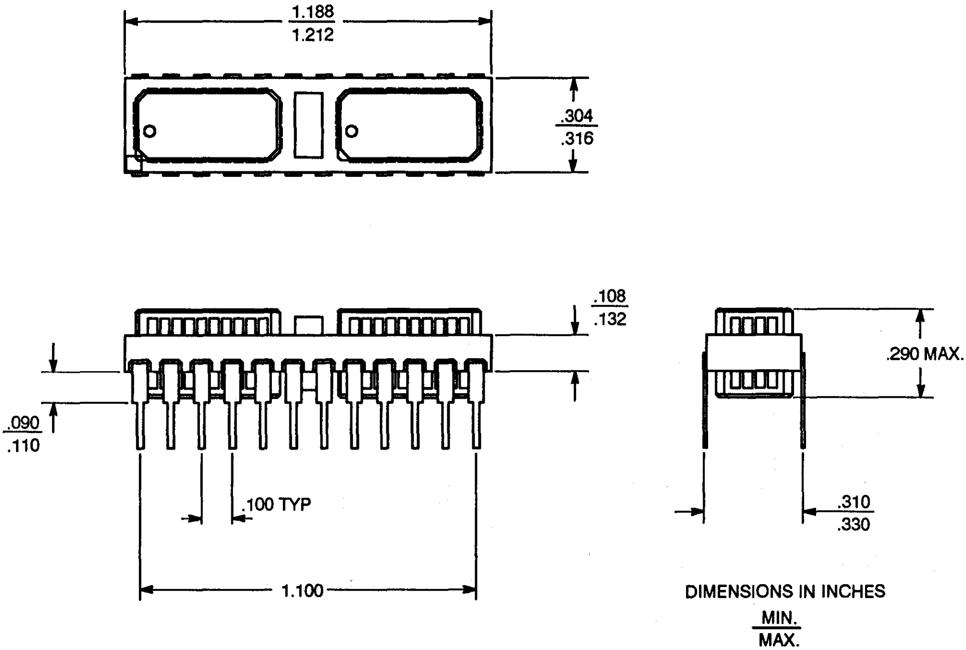
60-Pin Ceramic DIP Module HD06



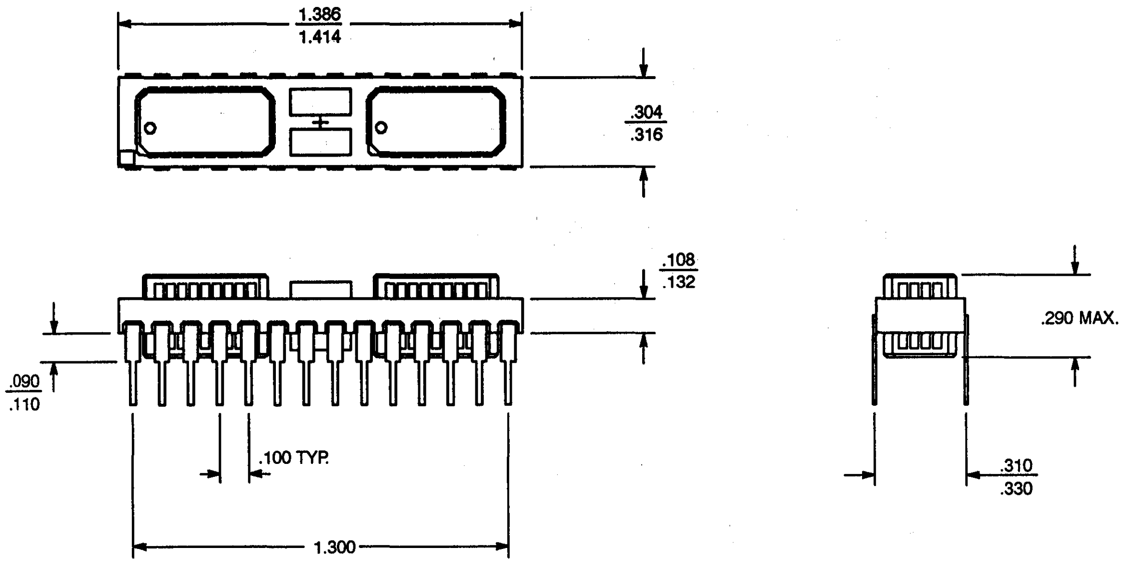
28-Pin DIP Module HD07



24-Pin DIP Module HD08

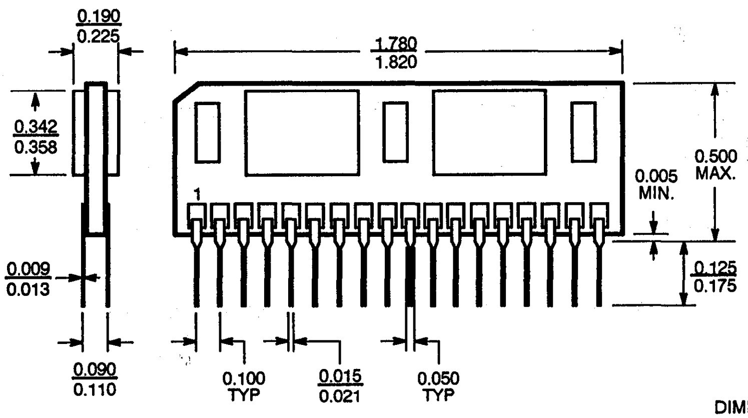


28-Pin DIP Module HD09



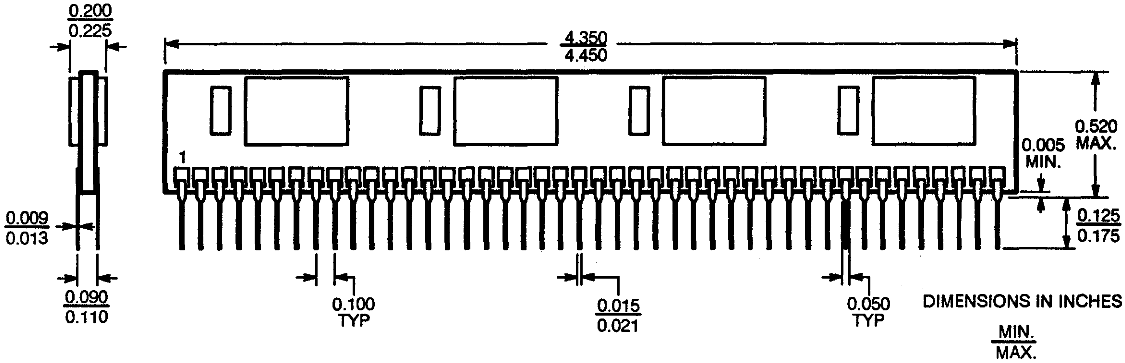
DIMENSIONS IN INCHES
MIN.
MAX.

36-Pin Vertical DIP Module HV01

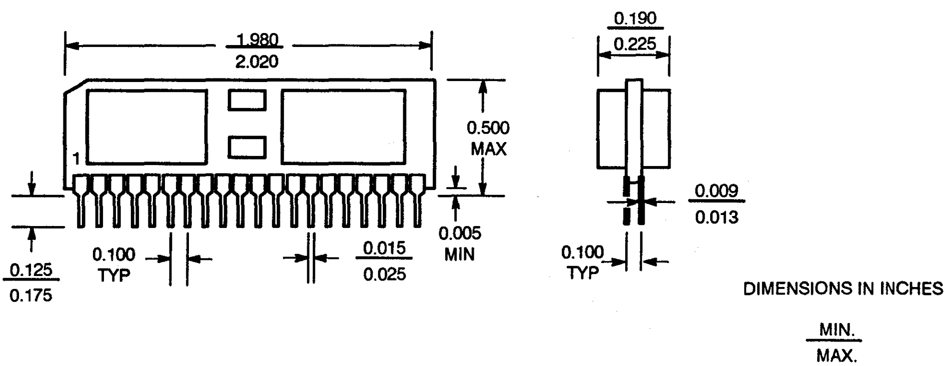


DIMENSIONS IN INCHES
MIN.
MAX.

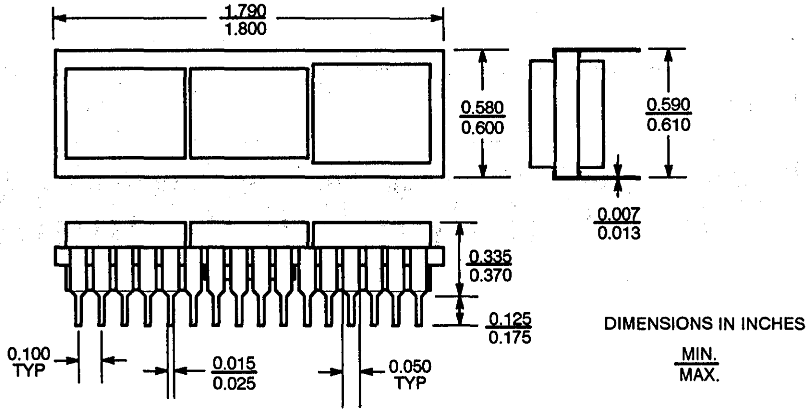
88-Pin Vertical DIP Module HV02



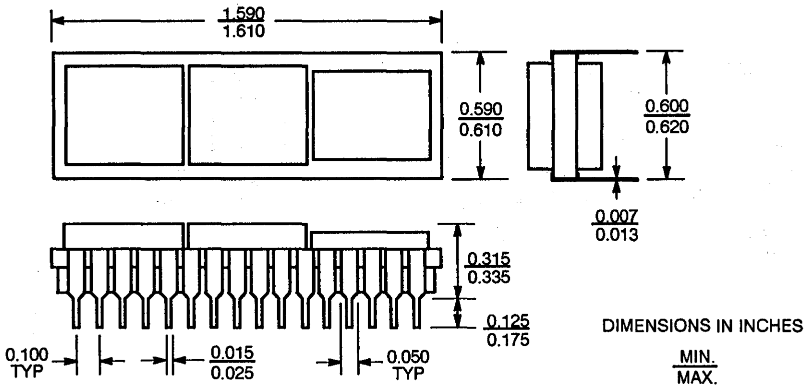
40-Pin VDIP Module HV03



32-Pin DIP Module PD01

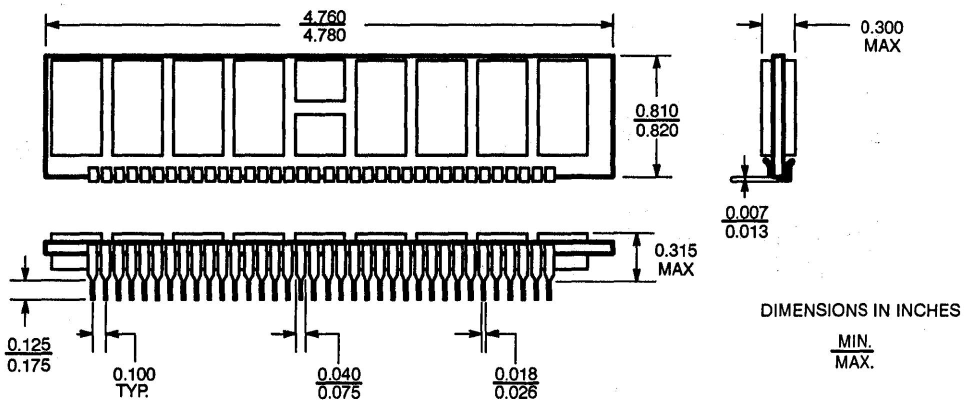


32-Pin DIP Module PD02

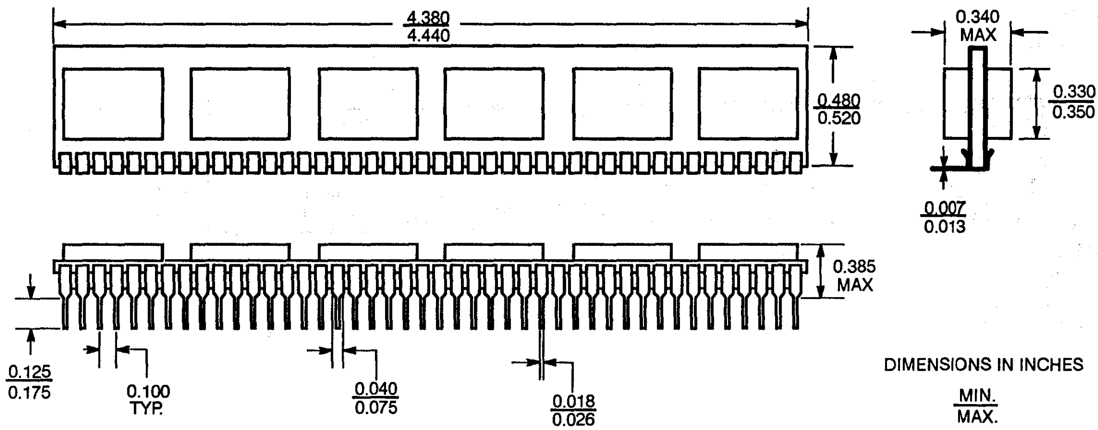


36-Pin Flat SIP Module PF01

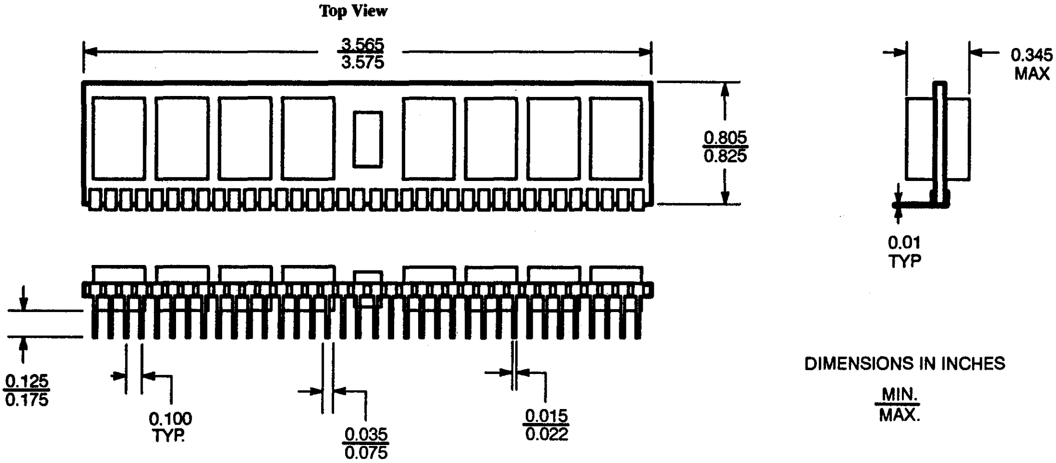
Top View



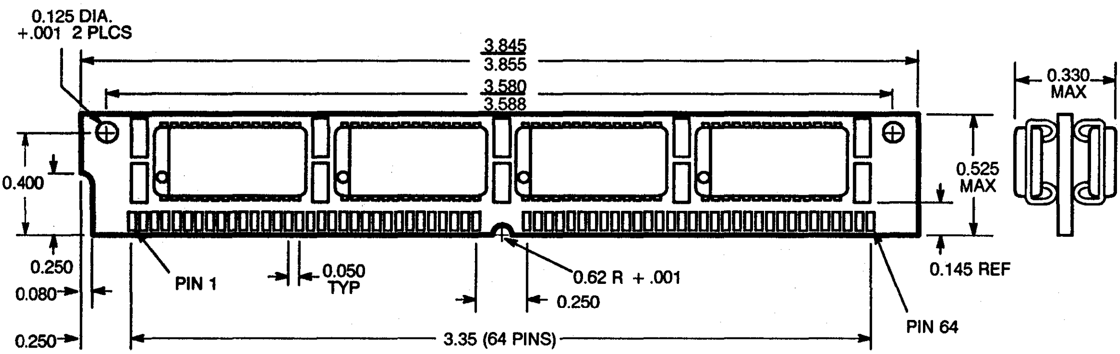
44-Pin Flat SIP Module PF02



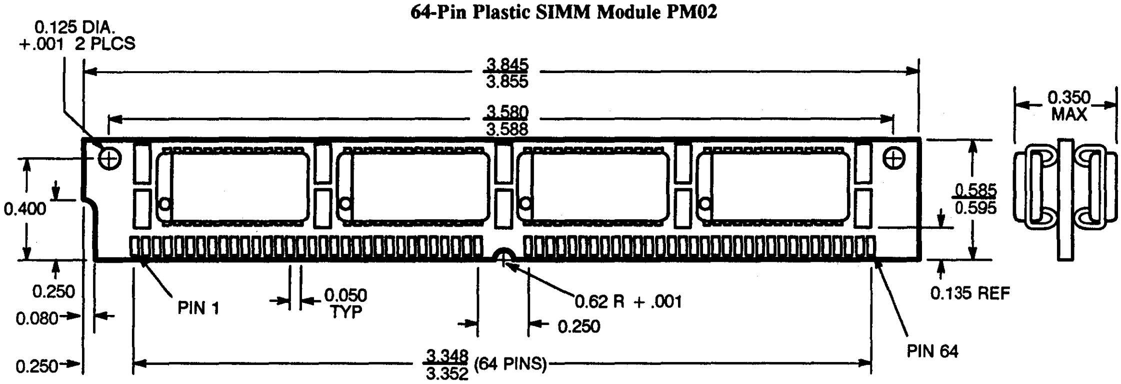
36-Pin Flat SIP Module PF03



64-Pin Plastic SIMM Module PM01

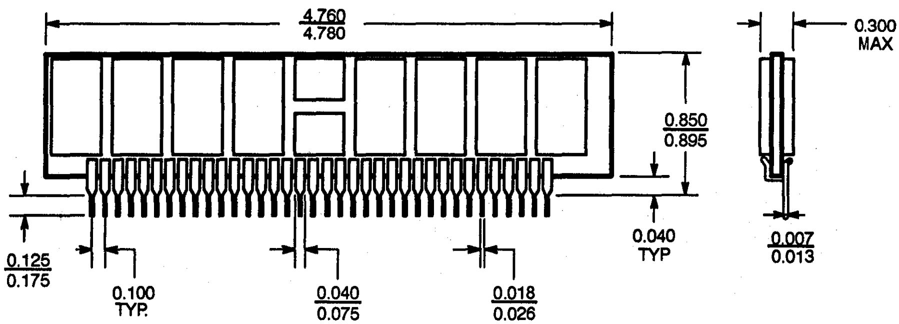


64-Pin Plastic SIMM Module PM02

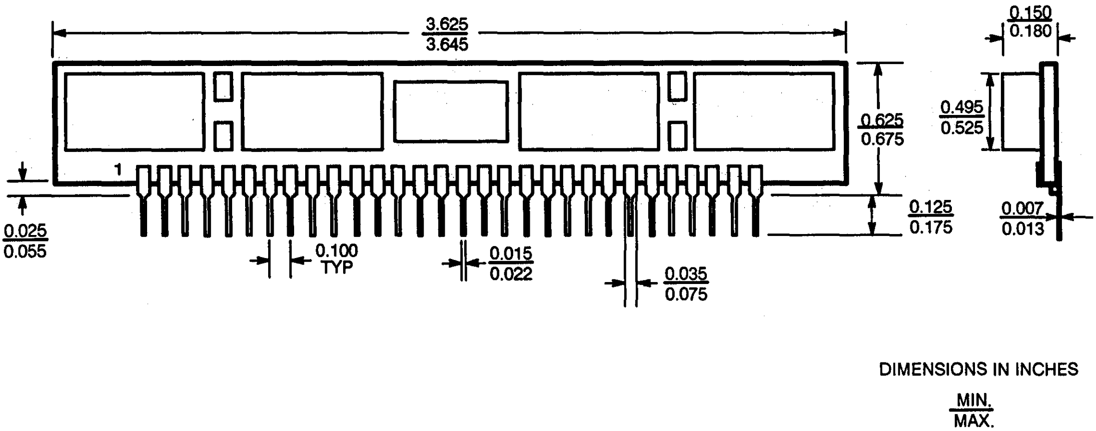


36-Pin SIP Module PS01

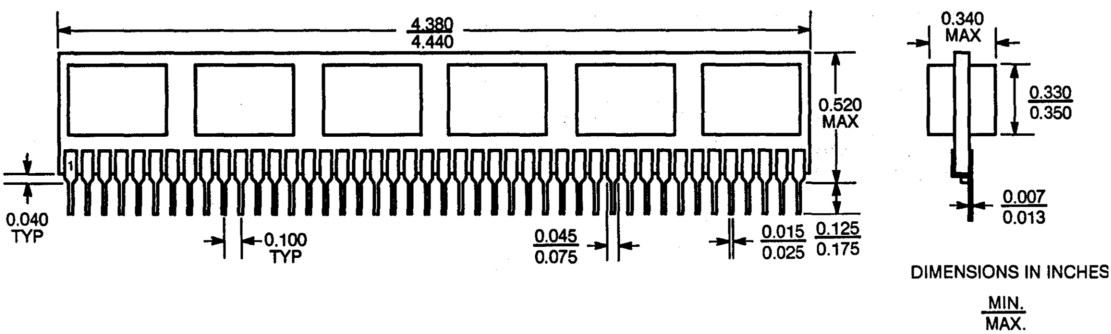
Top View



30-Pin Plastic SIP PS03

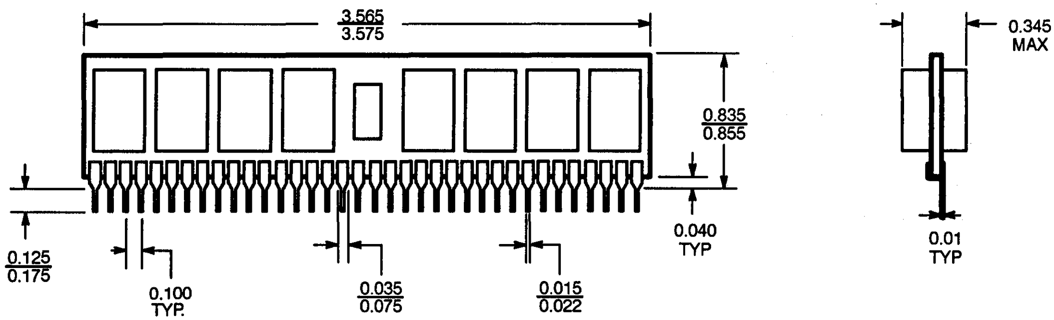


44-Pin Plastic SIP Module PS04

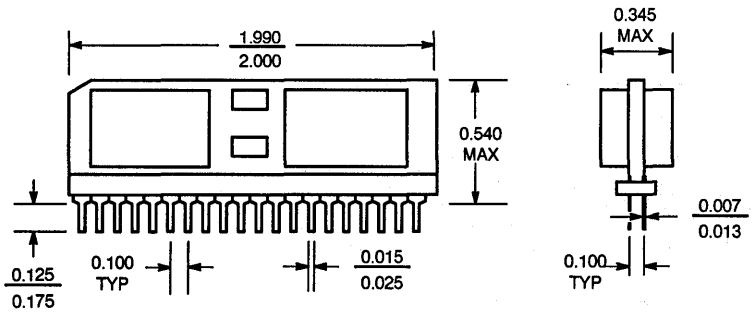


36-Pin SIP Module PS05

Top View



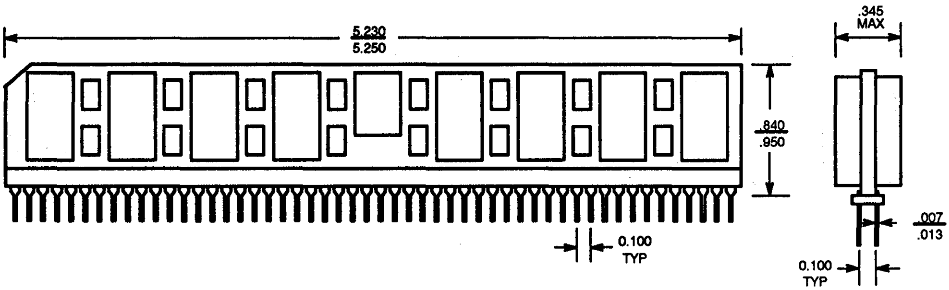
40-Pin VDIP Module PV01



DIMENSIONS IN INCHES

MIN.
MAX.

104-Pin VDIP Module PV02

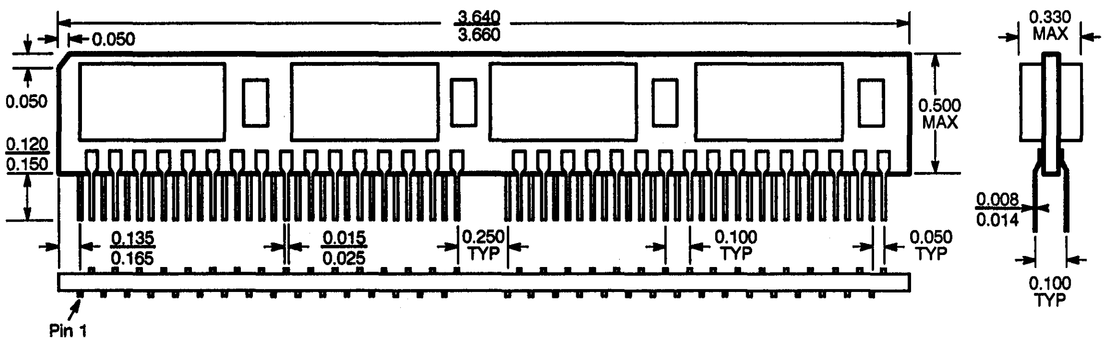


DIMENSIONS IN INCHES

MIN.
MAX.

64-Pin Plastic ZIP Module PZ01

Bottom View

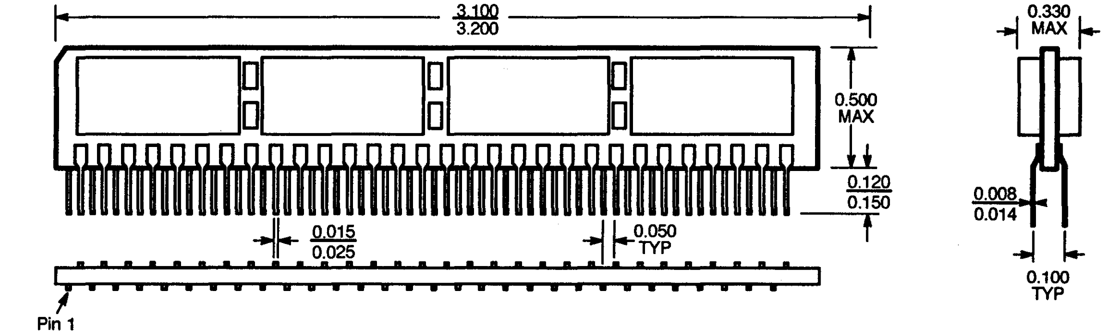


DIMENSIONS IN INCHES

MIN.
MAX.

60-Pin Plastic ZIP Module PZ02

Bottom View

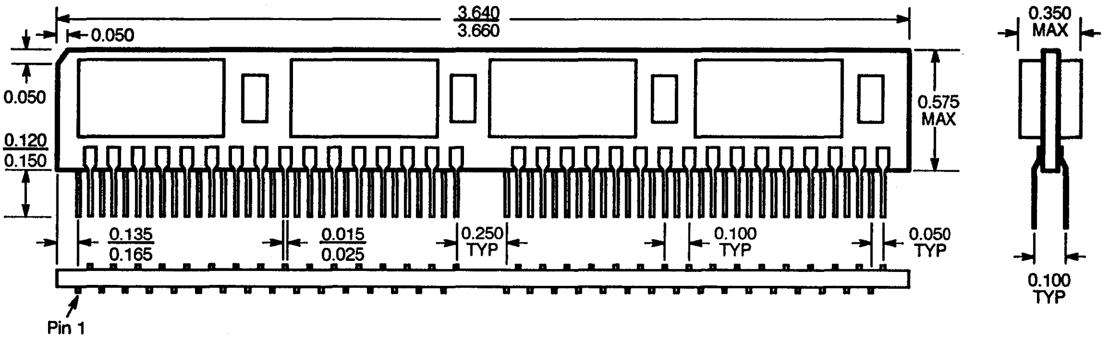


DIMENSIONS IN INCHES

MIN.
MAX.

64-Pin Plastic ZIP Module PZ03

Bottom View

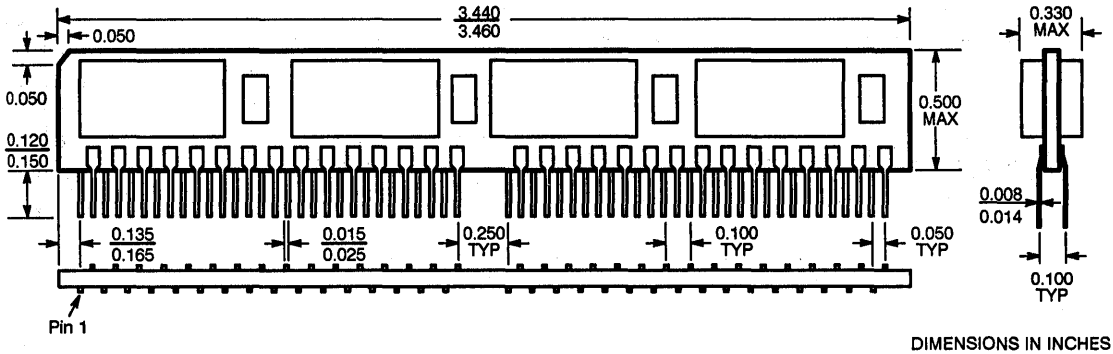


DIMENSIONS IN INCHES

MIN.
MAX.

60-Pin ZIP Module PZ04

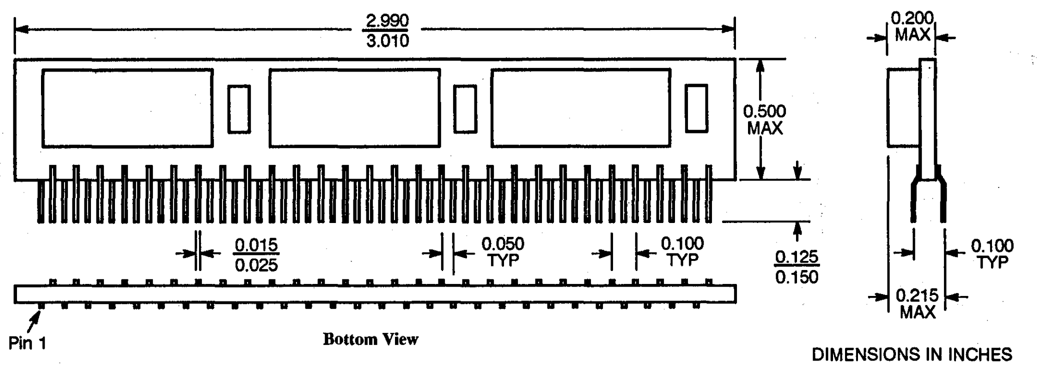
Bottom View



DIMENSIONS IN INCHES

MIN.
MAX.

56-Pin ZIP Module PZ05



DIMENSIONS IN INCHES

MIN.
MAX.

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