FAIRCHILD SEMICONDUCTOR

9500 Series • High Speed Logic

easy ECL

MAY 1971

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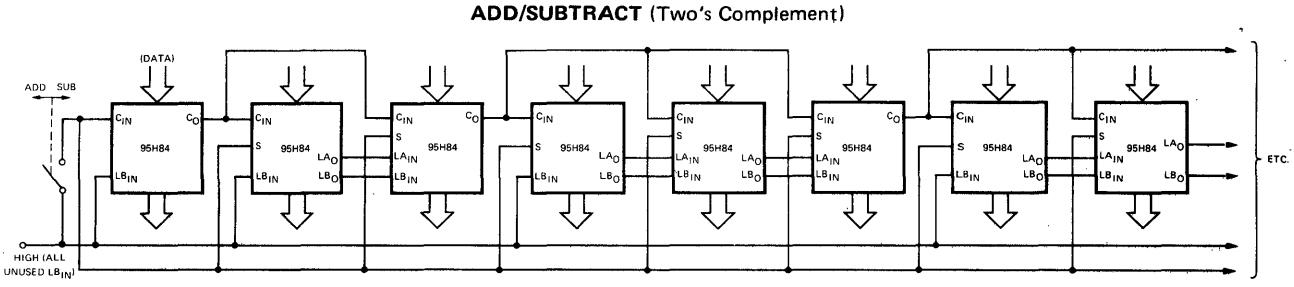
ADD/SUBTRACT (Two's Complement)



37	9505	Fig. 8: One input of unused OR gate must be HIGH.
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FAIRCHILD
SEMICONDUCTOR

FAIRCHILD 9500 EASY ECL FAMILY

SSI		MSI								
Gates	Flip Flops	Decoders	Multiplexers	Registers	Latches	Operators	Counters	Memory	Interface	
95L22 Dual 95L23 Triple 95L24 Quad										LOW POWER
9502 Dual 9503 Triple 9504 Quad 9505 OR/And 9507 Quad And	9528 Dual D	9538 1 of 8	9579 Quad 2 9580 Trip 2 9581 8 Input		9534 4 Bit	9578 Ex-Or/ Comp-arator		95410 256 Bit Ram	9582 Receiver/ Amplifier 9595 Converter	STANDARD
95H02 Dual 95H03 Triple 95H04 Quad	95H28 Dual D 95H29 J-K			95H39 Multi-port 95H00 4 Bit		95H55 5-Bit Comp-arator 95H42 Carry 95H41 4 Bit ALU 95H84 2 Bit Adder	95H10 Decimal 95H16 Binary 95H90 Prescaler	95400 64 Bit Ram 95401 16 Bit Ram		HIGH SPEED

FAIRCHILD 9500 EASY ECL

ECL offers both maximum speed performance and optimum logic flexibility in the design of high speed systems. Circuit features such as Wired-OR, complementary outputs and series gating permit the implementation of many digital functions with lower package count and therefore lower component cost, with similar system power dissipation, than with high speed TTL.

9500 ECL incorporates unique design features, including temperature compensation and on chip terminating resistors to eliminate many of the application problems (low noise margin and instability) associated with earlier forms of ECL. In addition the basic gate characteristics have been chosen to allow the use of more relaxed wiring rules and therefore lower cost interconnection methods than any logic family in the same speed range.

By taking advantage of Fairchild's experience in designing high speed custom circuits the 9500 user will have at his disposal one of the best planned circuit families available. The intermixing of high speed and very high speed ECL technologies, and basic gates with complex MSI functions in a single logic family allows a designer to optimise a system to his particular cost-performance goal.

The 9500 product range has been planned around the requirements of the three basic application areas for high speed circuits.

Computers — Basic Gates in 2.5 ns and 1.5 ns ranges, complex gate functions, dual D flip-flops, latches scratchpad memories, decoders, registers, adders.

Communications — Prescalers, mixers, broad band amplifiers, oscillators, multiplexers, decoders.

Instrumentation — High speed flip-flops for 100 MHz and 250 MHz applications, multiplexers, demultiplexers, line receivers.

This dynamic logic family will continue to expand as technology and applications demand. All additions to the 9500 range will be compatible with the present devices, permitting upgrading of existing designs to take advantage of economic and performance improvements as they become available.

SYSTEMS ADVANTAGES OF ECL

In addition to the maximum possible operating speeds, ECL also offers many advantages over other logic forms for the design of digital systems.

ADVANTAGES	FEATURE
• Transmission line compatible • Can be fully terminated • Minimum line reflections • Low transient noise susceptibility • High fan in/fan out possible across speed range	HIGH INPUT/LOW OUTPUT IMPEDANCE
• No additional inversion delay • Two logic decisions per gate delay • Up to 30% lower system package count	COMPLEMENTARY OUTPUTS/WIRE-OR CAPABILITY
• Low crosstalk • Simpler wiring rules for same system speed	HIGHER NOISE MARGIN RELATIVE TO LOGIC SWING. LOWER EDGE SPEED RELATIVE TO DELAY
• Low internal noise generation • Constant power dissipation across frequency range	CONSTANT SUPPLY CURRENT DRAIN
• Circuitry oriented to design of very high speed, medium power MSI functions	SERIES GATING, EMITTER AND COLLECTOR DOTTING,ETC.

9500 TEMPERATURE COMPENSATED ECL –

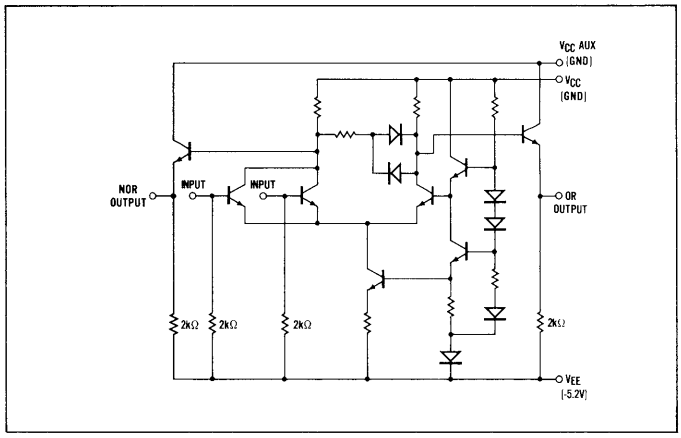
Significant applications characteristics of 9500 are:

- **Temperature Compensation**
  Logic levels remain constant across range 0°C to 75°C. Maintains maximum system noise immunity and eliminates saturation problems.
- **Packaging**
  Hermetic 16 pin Dual In-Line Package
- **Internal Pull Down Resistors**
  Point to point wiring up to 8" on single sided boards permitted by internal 2 k ohm resistors and choice of edge rates. These resistors also eliminate oscillation problems and allow unused inputs to be left open.
- **Low Crosstalk And Noise Generation**
  Insured by provision of split V_{CC} lines and location of supply pins.
- **50 Ohm Line Drive Capability**
  Output transistors designed to drive a 50 ohm terminated line and a fanout of 10 loads simultaneously.
- **Single Power Supply**
  9500 elements are specified for use with a single power supply.
- **MSI Flexibility**
  The 9500 product range has been designed to take maximum advantage of MSI performance in logic flexibility, economy and speed-power optimisation. Basic building blocks are aimed at computing, communications and instrumentation applications.
- **Cost Effectiveness**
  Low cost processing, together with above features insure simple applications rules and lowest cost hardware and components for high speed systems.

9500 ECL FAMILY CHARACTERISTICS

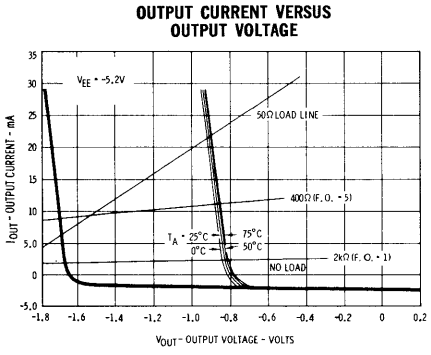
The 9500 circuit uses the same basic configuration as conventional ECL with the addition of temperature compensated internal reference and current source networks. These maintain the logic ZERO state insensitive to temperature variations. Logic ONE is clamped to ZERO by the collector cross-coupling diode network.

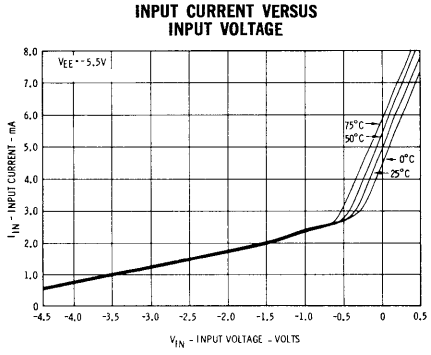
The temperature compensation networks require only minimal additional chip area for the gate functions. On MSI and complex gate elements the additional area is insignificant as compensation is only applied to the output nodes.



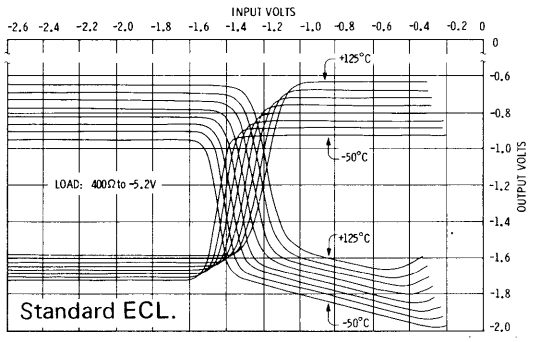
With –5.2 volt V_{EE} logic ONE is typically V_{OH} = –850 mV and logic ZERO V_{OL} = –1700 mV. These levels will interface directly with other ECL families, and with DTL and TTL using simple discrete and monolithic interface circuits. 9500 elements can also be operated from a positive supply if desired. (See Fairchild Application Brief 157).

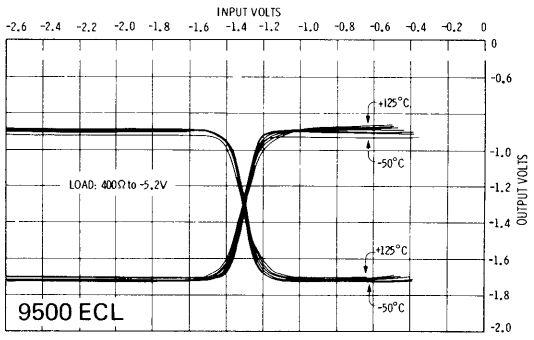
9500 Input-Output Characteristics





Conventional ECL vs. 9500 Transfer Characteristics





PRODUCT ANNOUNCEMENT SCHEDULE

AVAILABLE NOW IN QUANTITY

9502	Dual 4-Input OR/NOR Gate
9503	Triple 2-Input OR/NOR Gate
9504	Quad 2-Input NOR Gate
9505	Quad OR-AND Gate
9528	"Dual D" Flip Flop
9538	3 Line/8 Line Decoder
9581	8-Input Multiplexer
9582	Multifunction Receiver/ Amplifier
95H90	High Speed VHF Prescaler
9595	Level Converter

AVAILABLE 3RD QUARTER 1971

9507	Quad-AND-NAND Gate
95H02	High Speed 9502 (Dual 4-Input OR/NOR Gate)
95H03	High Speed 9503 (Triple 2-Input OR/NOR Gate)
95H04	High Speed 9504 (Quad 2-Input NOR Gate)
*95H22	High ohm option of the High Speed Dual 4-Input Gate
95L22	Low Power Dual Gate
*95H23	High ohm option of the High Speed Triple 2-Input Gate
95L23	Low Power Triple Gate
*95H24	High ohm option of the High Speed Quad 2-Input Gate
95L24	Low Power Quad Gate
95H29	High Speed J-K Flip Flop
*95H30	High ohm option of the High Speed J-K Flip Flop
9534	Quad Latch
95400	High Speed 64 Bit Scratch Pad
9578	Quad Exclusive-Or Gate/4-Bit Comparator
9579	Quad 2-Input Multiplexer
9580	Triple 2-Input Multiplexer
95H84	High Speed 2-Bit Adder/Subtractor

AVAILABLE 4TH QUARTER 1971

95H00	High Speed 4-Bit Universal Register
95H10	High Speed Synchronous Decade Counter
95H16	High Speed Synchronous Binary Counter
*95H26	High ohm option of the High Speed Dual D Flip Flop
95H28	High Speed Dual D Flip Flop
95H39	High Speed Multiport Register
95H41	High Speed 4-Bit ALU
95H42	High Speed Carry Lookahead
95H55	High Speed 5-Bit Comparator

*Special Order

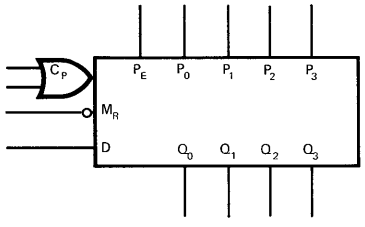
PRODUCT SUMMARY

95H00 FOUR BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION The 95H00 is a four bit Parallel/Serial In, Parallel/Serial Out Universal shift register. High speed ECL technology permits storage, shifting, counting and serial code conversion in excess of 150 MHz.

Features include assertion outputs on each state, overriding asynchronous master reset, serial and parallel D type inputs and a gated clock. Availability of all these features on one chip significantly improves the reliability, performance, and power consumption of high speed systems.

- HIGH SPEED . . . 150 MHz SHIFT FREQUENCY
- D TYPE INPUT IN SERIAL AND PARALLEL
- GATED CLOCK INPUT
- ASYNCHRONOUS MASTER RESET
- 50 Ω DRIVE ON Q3 OUTPUT
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER



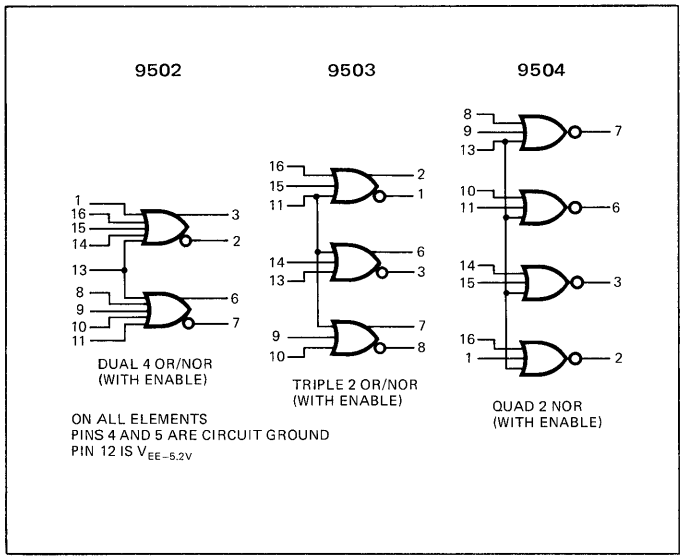
P_N = PARALLEL IN
P_E = PARALLEL ENABLE
Q_N = PARALLEL OUT, 10 LOADS
Q_3 = SERIAL 0 t, 50 Ω + 10 LOADS
C_P = CLOCK IN, SHIFTS ON POS. EDGE
M_R = ASYNCHRONOUS MASTER RESET
D = DATA INPUT, SERIAL

9502·9503·9504 BASIC GATES

DESCRIPTION The 9502, 9503 and 9504 are temperature compensated OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve high speed. The elements are intended for the design of high speed central processors, terminals, instrumentation and digital communications systems.

Input and output 2K Ω pulldown resistors eliminate the necessity for external termination of lines up to 6-8 inches and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk.

- HIGH SPEED . . . 2.3 ns PER GATE
- SEPARATE V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN RESISTORS
- COMMON ENABLE INPUTS
- LOW CROSSTALK AND NOISE GENERATION
- WIRE-OR CAPABILITY
- 50 Ω LINE DRIVING CAPABILITY
- COMPLEMENTARY OR/NOR OUTPUTS (9502, 9503)
- SINGLE –5.2V POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE



DUAL 4 OR/NOR (WITH ENABLE)

TRIPLE 2 OR/NOR (WITH ENABLE)

QUAD 2 NOR (WITH ENABLE)

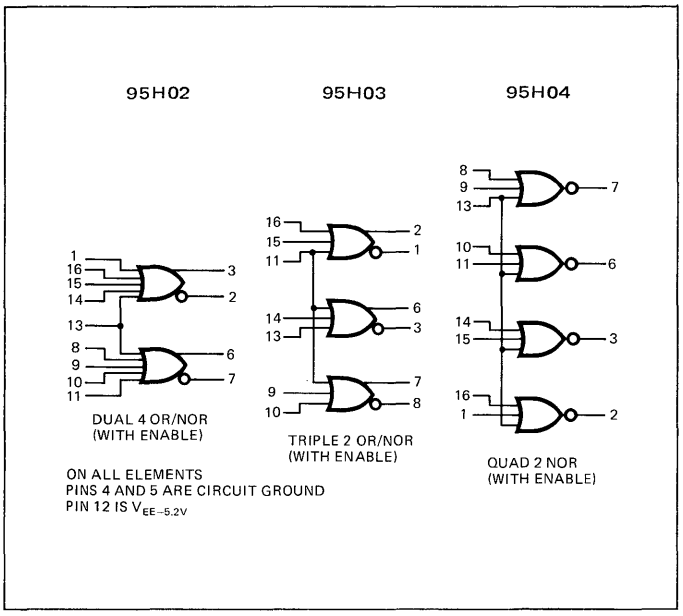
ON ALL ELEMENTS
PINS 4 AND 5 ARE CIRCUIT GROUND
PIN 12 IS $V_{EE-5.2V}$

95H02·95H03·95H04 CLOCK DRIVER/ HIGH SPEED GATES

DESCRIPTION The 95H02, H03 and H04 are temperature compensated OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve a very high speed. The elements are intended for use where higher logic speeds and faster edges than standard 9500 gates are required, as in clock and flip-flop driving.

These gates will improve available speed performance of 9528 flip-flops and 9534 latches in counting and register application.

- **HIGH SPEED . . . 1.6 ns PER GATE**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **COMMON ENABLE INPUTS**
- **LOW CROSSTALK AND NOISE GENERATION**
- **WIRE-OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **COMPLEMENTARY OR/NOR OUTPUTS (95H02, H03)**
- **SINGLE –5.2V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**



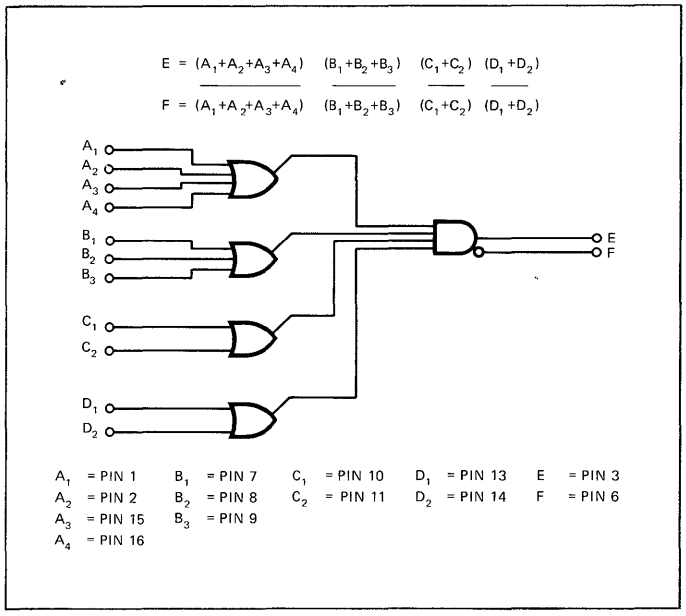
9505 4 WIDE OR-AND GATE

DESCRIPTION The 9505 is a temperature compensated OR-AND gate that achieves in slightly over one basic gate delay the AND of four different OR'ed functions.

The NOR outputs of the four OR gates are OR'ed to derive the OR-NOR function.

This element is useful in the design of Arithmetic Logic Units for construction of adders, subtracters, multipliers etc. Just two 9505's will implement a full carry adder function.

- **HIGH SPEED . . . 2.7 ns OR-AND, 2.5 ns NOR-OR**
- **SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATED**
- **INTERNAL 2K PULL DOWN RESISTORS**
- **COMPLEX LOGIC FUNCTION REDUCES PACKAGE COUNT**
- **WIRE OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **SINGLE –5.2V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

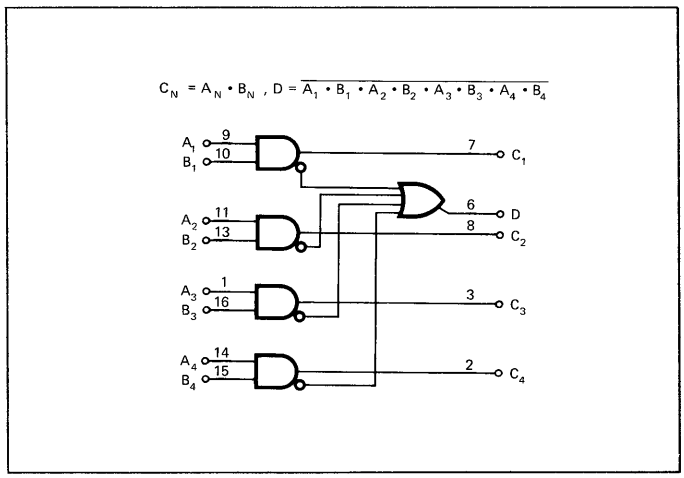


9507
QUAD AND/NAND

DESCRIPTION The 9507 is a Temperature Compensated Quad ECμL AND gate using series gating and collector and emitter dotting to achieve the logical functions within approximately one gate delay.

The uses are for any logical AND or 8 input NAND function with higher speed than similar logic implemented with standard gates. This element is designed to increase speed and reduce package count in high performance processors and controllers.

- HIGH SPEED . . . 2.6 ns PER GATE
- 8 INPUT LOGIC NAND IN ONE GATE DELAY
- SEPARATE NON-STANDARD ECL LOGIC FUNCTIONS –4 DUAL AND GATES
- HIGHER SYSTEM RELIABILITY AND LOWER COST BY ELIMINATING COMPLEX WIRING OF OR/NOR GATES
- SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN RESISTORS
- LOW CROSSTALK AND NOISE GENERATION
- WIRE OR CAPABILITY
- 50 Ω LINE DRIVING CAPABILITY
- SINGLE –5.2V POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP

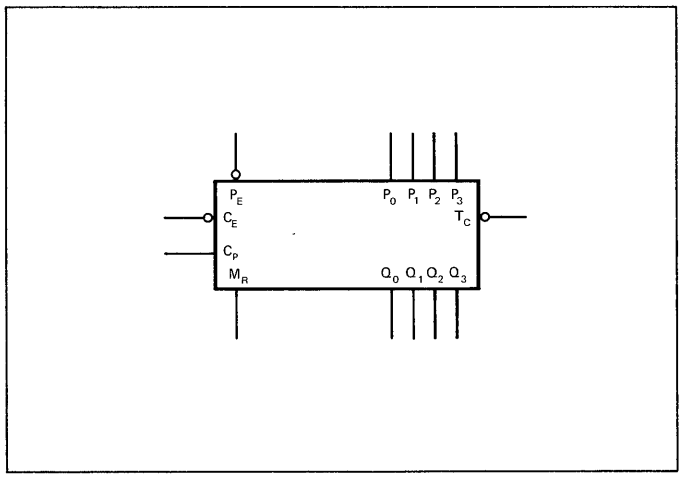


95H10 MSI BCD
DECADE COUNTER

DESCRIPTION The 95H10 is a high speed synchronously presettable 8421 BCD decade counter. It is a synchronously presettable, multifunction MSI building block useful for a large number of counting, digital integration, and conversion applications. Up to 9 decades can be cascaded with no speed degradation using the standard 9500 gates. With 95H00 gates a multidecade synchronous load counter to over 150 MHz can be built. Typical counter frequency is over 180 MHz or easy frequency increase to over 250 MHz with the 95H29 JK Flip Flop.

Features include assertion inputs and outputs on each of the 4 master slave counting flip flop. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter. When the parallel load feature is not needed, the CE input may be used as a clock gate regardless of clock input level. Availability of all these features on one chip significantly improves the reliability, performance and power consumption of high speed systems.

- HIGH SPEED COUNT . . . 180 MHz TYPICAL COUNT FREQUENCY
- HIGH SPEED SYNCHRONOUSLY LOAD . . . OVER 150 MHz SYNCHRONOUS LOAD FREQUENCY
- INTERNAL COUNT ENABLE
- EXPANDABLE TO OVER 250 MHz WITH THE 95H29
- ASYNCHRONOUS MASTER RESET
- 50 Ω OR FANOUT OF 10 ON EACH OUTPUT
- WIRE OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN FOR DIRECT LOW COST WIRING
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT AND POWER

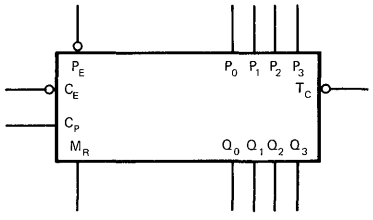


95H16 MSI 4-BIT BINARY COUNTER

DESCRIPTION The 95H16 is a high speed synchronously presettable 4-Bit Binary counter. It is a synchronously presettable, multifunction MSI building block useful for a large number of counting, digital, integration, and conversion applications. Up to 9 devices can be cascaded with no speed degradation using the standard 9500 gates. With 95H00 gates a multidecade synchronous load counter to over 150 MHz can be built. Typical count frequency is over 180 MHz or easy frequency increase to over 250 MHz with the 95H29 JK Flip Flop.

Features include assertion inputs and outputs on each of the 4 master slave counting flip flop. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter. When the parallel load feature is not needed, the CE input may be used as a clock gate regardless of clock input level. Availability of all these features on one chip significantly improves the reliability, performance and power consumption of high speed systems.

- HIGH SPEED COUNT . . . 180 MHz TYPICAL COUNT FREQUENCY
- HIGH SPEED SYNCHRONOUSLY LOAD . . . OVER 150 MHz SYNCHRONOUS LOAD FREQUENCY
- INTERNAL COUNT ENABLE
- EXPANDABLE TO OVER 250 MHz WITH THE 95H29
- ASYNCHRONOUS MASTER RESET
- 50 Ω OR FANOUT OF 10 ON EACH OUTPUT
- WIRE OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN FOR DIRECT LOW COST WIRING
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT AND POWER

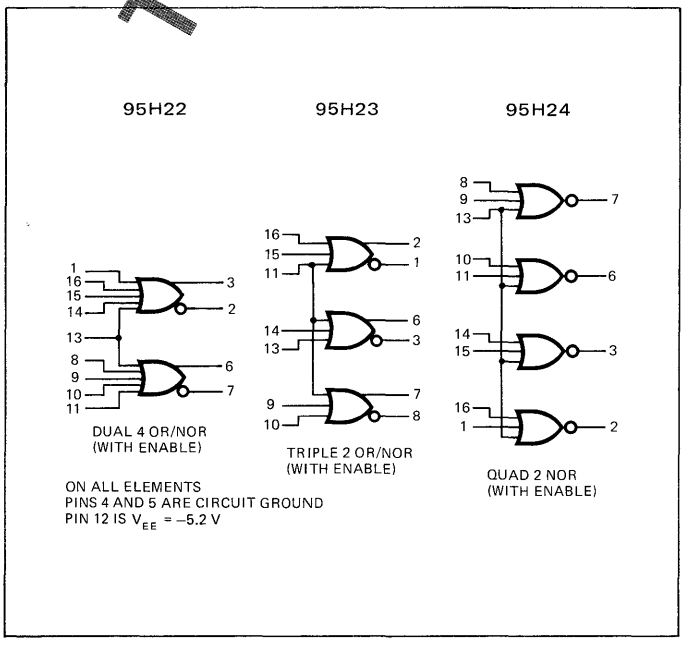


95H22·95H23·95H24 CLOCK DRIVER/ HIGH SPEED GATES

DESCRIPTION The 95H22, H23 and H24 are temperature compensated OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve a very high speed. The elements are intended for use where higher logic speeds and faster edges than standard 9500 gates are required, as in clock and flip-flop driving.

These gates will improve available speed performance of 9528 flip-flops and 9534 latches in counting and register application.

- HIGH SPEED . . . 1.6 ns PER GATE
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL 50 KΩ RESISTORS FOR GREATER FANOUT
- COMMON ENABLE INPUTS
- LOW CROSSTALK AND NOISE GENERATION
- WIRE-OR CAPABILITY
- 50 Ω LINE DRIVING CAPABILITY
- COMPLEMENTARY OR/NOR OUTPUTS (95H22, H23)
- SINGLE –5.2V POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE

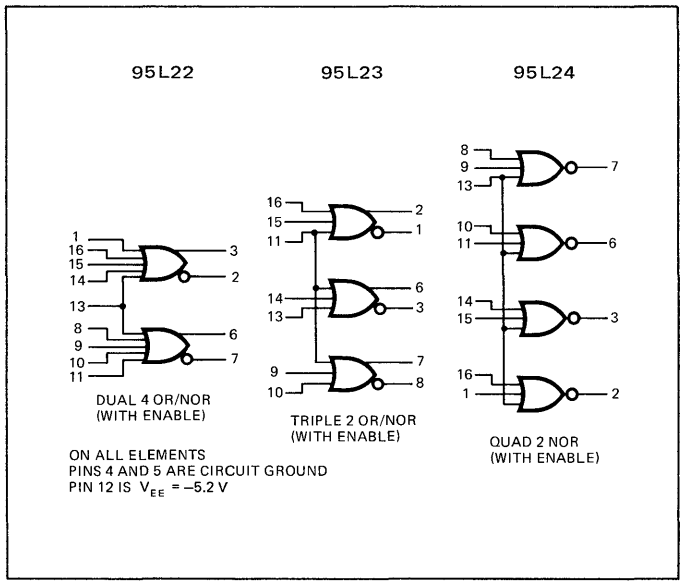


95L22·95L23·95L24
LOW POWER GATES

DESCRIPTION The 95L22, L23, and L24 are temperature compensated ECμL OR/NOR Gates employing a non-saturating current switch, emitter follower configuration to achieve high speed. These elements are intended for use where power is to be minimized. External pull-down resistors are needed for all outputs. For longer lines series termination may be used to further reduce system power.

These gates will improve available power performance of ECL systems where speed degrading due to fanout and loading can be tolerated.

- **LOW POWER . . . 20 MW PER GATE**
- **HIGH SPEED . . . 2.0 ns INTO 50 OHMS**
- **TEMPERATURE COMPENSATION**
- **INTERNAL 50 K Ω RESISTORS ON INPUTS**
- **COMMON ENABLE INPUTS**
- **50 Ω LINE DRIVE CAPABILITY**
- **WIRE-OR CAPABILITY**
- **PIN COMPATIBLE WITH OTHER 9500 GATES**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**



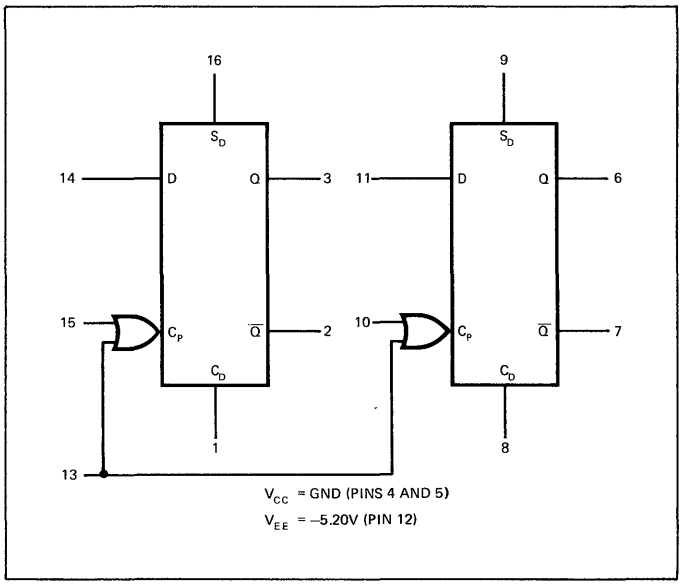
95H26
VERY HIGH SPEED
DUAL D FLIP-FLOP

DESCRIPTION The 95H26 is a high speed, temperature compensated ECμL dual D (data) flip-flop compatible with all other members of the 9500 series of ECμL circuits. The device is versatile and permits easy implementation of high speed counters, registers, and control circuits.

FUNCTIONAL DESCRIPTION Each D Flip-Flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when low speed edges are encountered in the system.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The ORed clock permits the use of one input as a clock pulse input and the other as an active low enable.

- **260 MHz OPERATION**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL 50 K Ω RESISTORS FOR GREATER FANOUT**
- **MASTER-SLAVE CIRCUIT**
- **SEPARATE DIRECT SET AND CLEAR INPUTS**
- **BOTH COMMON AND SEPARATE CLOCK INPUTS**
- **WIRED-OR CAPABILITY ON OUTPUTS**
- **50 Ω LINE DRIVING CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**



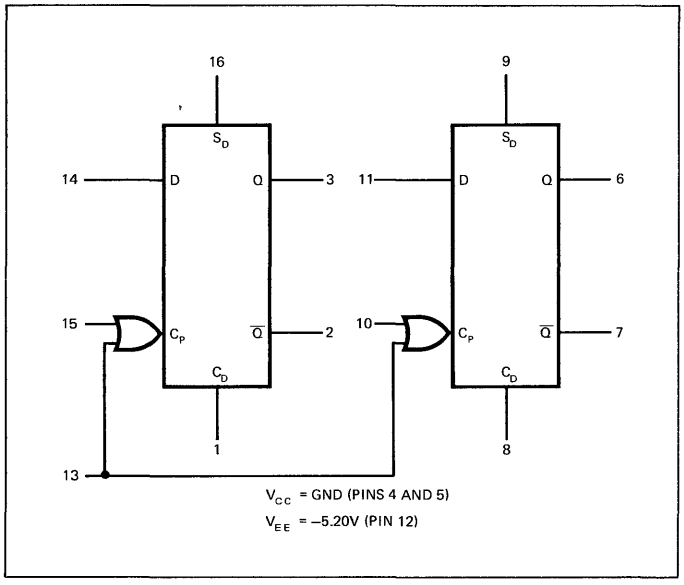
9528 HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION The 9528 is a high speed, temperature compensated ECμL dual D (data) flip-flop compatible with all other members of the 9500 series of ECμL circuits. The device is versatile and permits easy implementation of high speed counters, registers, and control circuits.

FUNCTIONAL DESCRIPTION Each D Flip-Flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when low speed edges are encountered in the system.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The ORed clock permits the use of one input as a clock pulse input and the other as an active low enable.

- 160 MHz OPERATION
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN RESISTORS
- MASTER-SLAVE CIRCUIT
- SEPARATE DIRECT SET AND CLEAR INPUTS
- BOTH COMMON AND SEPARATE CLOCK INPUTS
- WIRED-OR CAPABILITY ON OUTPUTS
- 50 Ω LINE DRIVING CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE



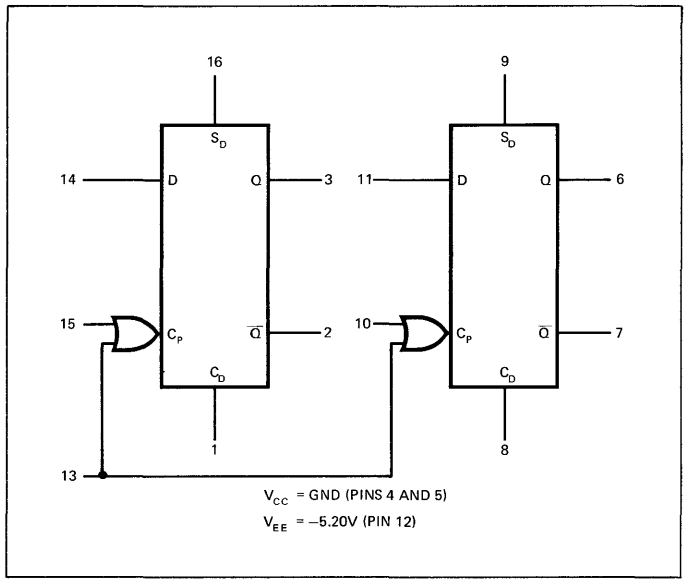
95H28 VERY HIGH SPEED DUAL D FLIP-FLOP

DESCRIPTION The 95H28 is a high speed, temperature compensated ECμL dual D (data) flip-flop compatible with all other members of the 9500 series of ECμL circuits. The device is versatile and permits easy implementation of high speed counters, registers, and control circuits.

FUNCTIONAL DESCRIPTION Each D Flip-Flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when low speed edges are encountered in the system.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The ORed clock permits the use of one input as a clock pulse input and the other as an active low enable.

- 260 MHz OPERATION
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN RESISTORS
- MASTER-SLAVE CIRCUIT
- SEPARATE DIRECT SET AND CLEAR INPUTS
- BOTH COMMON AND SEPARATE CLOCK INPUTS
- WIRED-OR CAPABILITY ON OUTPUTS
- 50 Ω LINE DRIVING CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE

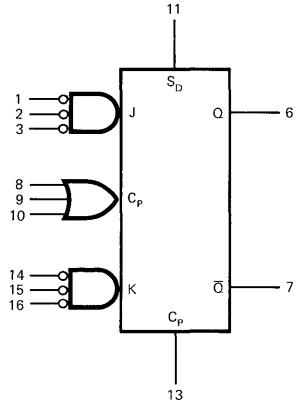


95H29 VERY HIGH SPEED $\overline{J}$-$\overline{K}$ FLIP-FLOP

DESCRIPTION The 95H29 is a Hi-Speed edge-triggered $\overline{J}$ $\overline{K}$ Master-Slave flip-flop with both direct set and clear inputs. The $\overline{J}$, $\overline{K}$ and Clock functions are the active low AND of three inputs. With these inputs this device may be used effectively in counters, registers and other applications where data must be stored or shifted at a high rate.

In addition the full frequency range may be used effectively as a prescaler and controlled divider for frequencies up to 250 MHz.

- 250 MHz OPERATION
- ASYNCHRONOUS DIRECT SET AND CLEAR
- MASTER-SLAVE CIRCUIT
- NON-ONES CATCHING
- SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS
- $\overline{J}$ AND $\overline{K}$ INPUTS
- INTERNAL PULLDOWN RESISTORS
- WIRED-OR CAPABILITY ON OUTPUTS
- 50 Ω LINE DRIVING CAPABILITY
- TEMPERATURE COMPENSATION
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP



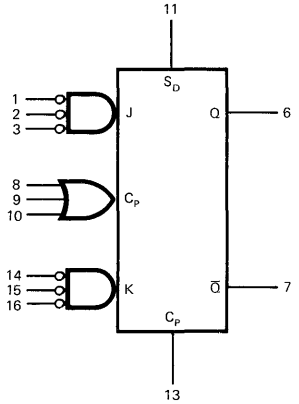
PIN 4 & 5 = V_{CC}
PIN 12 = V_{EE} (–5.2)

95H30 VERY HIGH SPEED $\overline{J}$-$\overline{K}$ FLIP-FLOP

DESCRIPTION The 95H30 is a Hi-Speed edge-triggered $\overline{J}$ $\overline{K}$ Master-Slave flip-flop with both direct set and clear inputs. The $\overline{J}$, $\overline{K}$ and Clock functions are the active low AND of three inputs. With these inputs this device may be used effectively in counters, registers and other applications where data must be stored or shifted at a high rate.

In addition the full frequency range may be used effectively as a prescaler and controlled divider for frequencies up to 250 MHz.

- 250 MHz OPERATION
- ASYNCHRONOUS DIRECT SET AND CLEAR
- MASTER-SLAVE CIRCUIT
- NON-ONES CATCHING
- SEPARATE CURRENT SWITCH & EMITTER FOLLOWER V_{CC} PINS
- $\overline{J}$ AND $\overline{K}$ INPUTS
- INTERNAL 50K Ω INPUT RESISTORS FOR GREATER FANOUT
- WIRED-OR CAPABILITY ON OUTPUTS
- 50 Ω LINE DRIVING CAPABILITY
- TEMPERATURE COMPENSATION
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP



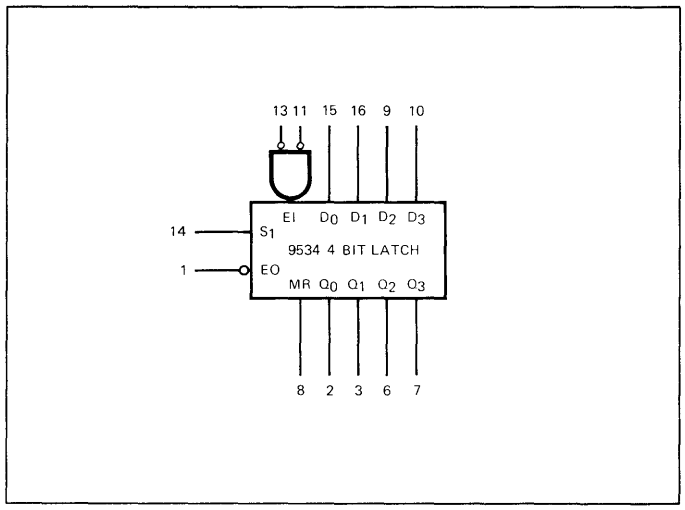
PIN 4 & 5 = V_{CC}
PIN 12 = V_{EE} (–5.2)

9534 QUAD LATCH WITH INPUT AND OUTPUT ENABLES

DESCRIPTION The 9534 quad D latch will store four bits of information simultaneously. Two Input enable inputs and a common output enable allow maximum logic flexibility. A common Select input selects 'D' type or 'Set' type of operation. A common reset clears the device so that the 1's catching feature may be used when desired.

This element is designed as a storage buffer for high speed registers in arithmetic logic units and parallel-serial conversion in communication systems.

- HIGH SPEED . . . 4.3 ns TYPICAL DATA DELAYS 'S
- COMMON LATCH ENABLE
- COMMON MASTER RESET
- COMMON SELECT FOR 'D' OR 'SET'
- COMPLEX MULTIGATE CHIP REDUCES PACKAGE COUNT
- EASILY EXPANDED TO LARGE HIGH SPEED MEMORY
- WIRED-OR CAPABILITY
- SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP



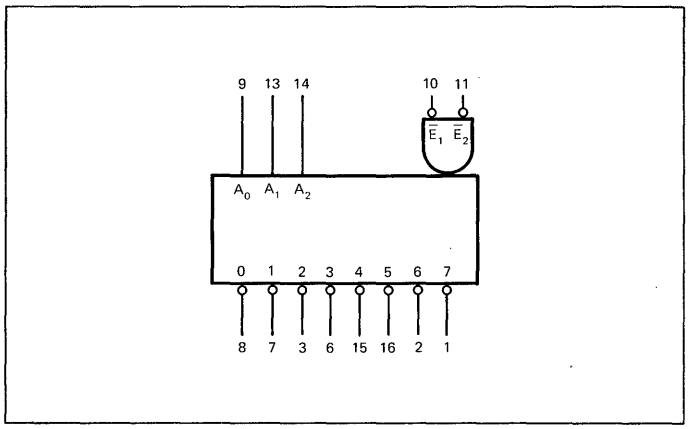
9538 OCTAL DECODE-3 LINE/8 LINE

DESCRIPTION The 9538 decoder accepts three binary address inputs and under control of the enables activate one of the eight active low outputs. Both enables must be low for any output to go low.

The ECL 9538 may be used as a demultiplexer by connecting a data source to one of the enable inputs. The other enable input will function as a data enable line while inputs A_0, A_1, and A_2 select the desired data output line (0 through 7).

The 9538 is particularly useful in memory expansion and register or peripheral selection applications.

- HIGH SPEED . . . 4 ns FROM ADDRESS TO OUTPUT
- USEABLE FOR DEMULTIPLEXING – 2 ENABLE INPUTS
- OUTPUTS ACTIVE LOW FOR ENABLING WITH OTHER MEMBERS OF THE 9500 FAMILY
- NO INVERSION FROM ENABLE TO SELECTED OUTPUT
- WIRED-OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER

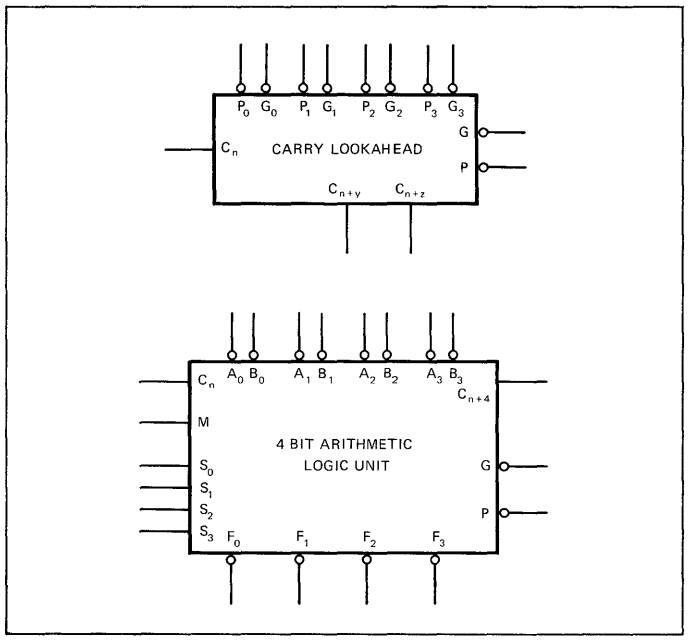


95H41 MSI 4 BIT ALU 95H42 MSI CARRY LOOKAHEAD UNIT

DESCRIPTION The 95H41 is a 4 Bit High Speed Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes being the most important. This ALU is ideally suited for mini-computers, data processors, peripheral systems, and instrument systems. The functions found in the successful TTL 9341/54181 have been used to define this ECL/MSI. Although not as fast as the 95H84 2 Bit Adder/Subtractor the multiple functions permit reduced package count for the multiple function applications.

Features include: All 16 operations of two variables – Exclusive OR, Comparator, AND, NAND, OR, NOR, plus ten other logic operations. The experience gained from use of the TTL equivalent can be directly applied to this high speed ECL MSI. The 95H42 is the Carry Lookahead Generator.

- HIGH SPEED . . . TYPICAL 4 BIT ADD OF 5 ns
- COMPLEX MULTIFUNCTION CHIP REDUCES PACKAGE AND POWER REQUIREMENTS
- 50 Ω OR FANOUT OF 10 ON EACH OUTPUT
- WIRE-OR CAPABILITY
- SEPARATE CURRENT SWITCH, EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN FOR DIRECT LOW COST WIRING
- SINGLE –5.2 VOLT SUPPLY
- HERMETIC CERAMIC 24 PIN DIP

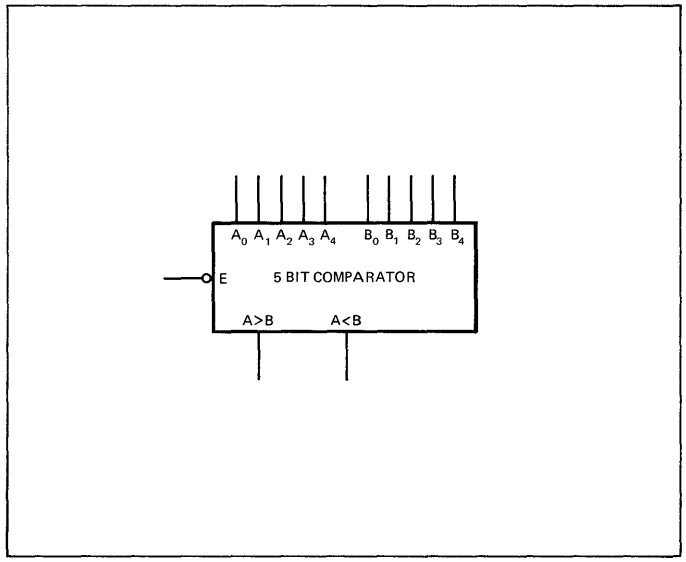


95H55 MSI 5 BIT COMPARATOR WITH ENABLE

DESCRIPTION The 95H55 is a high speed expandable 5 Bit Comparator which provides comparisons between two 5 bit words and gives two outputs, "Less Than" and "Greater Than". "Equal To" can be obtained by ORing the "Less Than" and "Greater Than" outputs. A high level on the Enable function forces both outputs low.

Features include easy expansion to larger word comparisons and very high speed operation. Experience gained in use of the TTL 9324 can be directly applied to the 95H55.

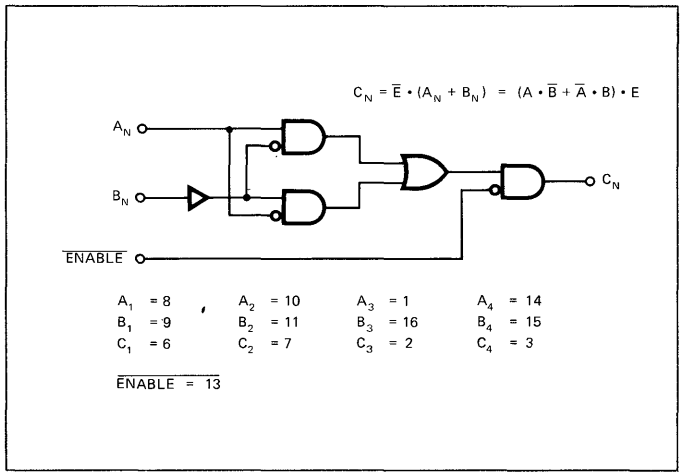
- HIGH SPEED . . . 1.0 ns INTERNAL GATE DELAYS
- "GREATER THAN" AND "LESS THAN" IN ONE DEVICE
- OUTPUT ENABLE INPUT IS ACTIVE LOW FOR EASE OF USE WITH OTHER MEMBERS OF THE 9500 FAMILY
- WIRE-OR CAPABILITY
- 50 Ω OR FANOUT OF 10 ON EACH OUTPUT
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATED
- INTERNAL PULLDOWN RESISTORS FOR DIRECT LOW COST WIRING
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP



9578 QUAD EXCLUSIVE - OR WITH ENABLE, 4 BIT COMPARATOR

DESCRIPTION The 9578 provides four exclusive OR gates in one package using internal gating to achieve the logic function within approximately one gate delay. An additional enable gate is included so that all outputs may be held low if desired. With four of these devices a 16 bit compare function may be built with one gate delay. This element is useful in many applications such as data comparison, parity generation and checking, frequency mixing, decision and code conversion, etc.

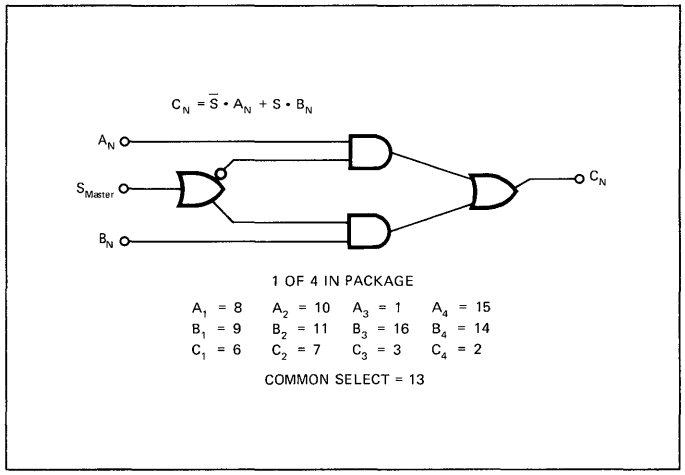
- HIGH SPEED . . . 3.0 ns FOR EX-OR
- COMMON ENABLE
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULLDOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER



9579 QUAD 2 INPUT MULTIPLEXER WITH COMMON SELECT

DESCRIPTION The 9579 is a Temperature Compensated logic equivalent of a 4 pole – 2 position switch. It will select logically one of two groups of 4 data sources with a common select line. This high speed switch operates within about one 9500 gate delay and provides a significant increase in reliability and power savings by delivering this function in one 16 pin package.

- HI-SPEED . . . 3.0 ns FROM SELECT TO OUTPUT
- COMMON SELECT
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER



9580 TRIPLE 2 INPUT MULTIPLEXER WITH COMMON ENABLE

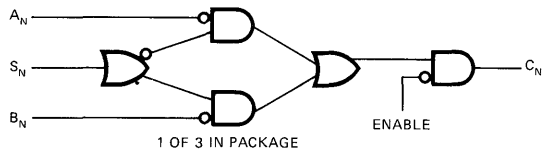
DESCRIPTION The 9580 multiplexer is the logic equivalent of 3 single pole, two position switches.

By the use of the separate select lines the 9580 may be interconnected as a 4 input multiplexer.

The output Enable function allows ease of expansion into more complex elements by use of the wired OR feature. For example with the additional use of a standard gate two 9580's will expand into a triple 4 input multiplexer, useful in register and peripheral applications.

- HIGH SPEED . . . 3.0 ns FROM SELECT TO OUTPUT
- SEPARATE SELECTS
- COMMON ENABLE
- INTERCONNECTS TO 4 INPUT MULTIPLEXER
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVER CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER

$C_N = \overline{E} \cdot (\overline{S}_N \cdot \overline{A}_N + S_N \cdot \overline{B}_N)$



1 OF 3 IN PACKAGE

$A_1 = 7$ $A_2 = 1$ $A_3 = 14$
$B_1 = 8$ $B_2 = 16$ $B_3 = 13$
$S_1 = 9$ $S_2 = 15$ $S_3 = 11$
$C_1 = 6$ $C_2 = 3$ $C_3 = 2$
COMMON ENABLE = PIN 10

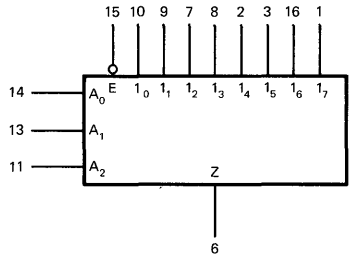
9581 1 OF 8 MULTIPLEXER

DESCRIPTION The 9581 eight input multiplexer is fundamentally a high speed semiconductor implementation of a single-pole eight-position switch. Three address lines select one out of the eight data inputs and feed this input to the output (Z). An active low enable forces the output LOW if held HIGH.

The 9581 provides the ability to select from or sequence eight data sources. It may therefore be used as a parallel to serial converter by sequentially advancing through the input address combinations.

The device may also be used as a universal logic element capable of generating any function of four variables by proper manipulation of the inputs. The wire-ORable outputs and the input enable permit easy expansion of several 9581's to form multiplexers with more than eight inputs.

- HIGH SPEED . . . 3.2 ns DATA
- ACTIVE LOW ENABLE – INTERFACES WITH OTHER MEMBERS OF THE LINE
- PARALLEL TO SERIAL CONVERTER
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER

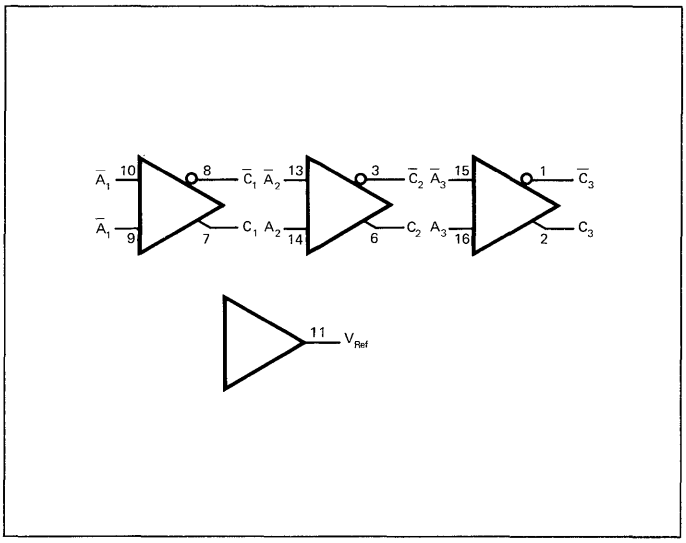


V_{CC} = GND (PINS 4 & 5)
V_{EE} = –5.2 V (PIN 12)

9582 MULTI-FUNCTION LINE RECEIVER/ AMPLIFIER

DESCRIPTION The 9582 is 3 differential input amplifiers. Both the true and complement outputs are temperature compensated to be compatible with other ECL 9500 products. With appropriate connection of the base pins the device will function as a differential line receiver; Schmitt trigger; high speed comparator; broad band video, IF. or R.F. amplifier; or oscillator. V_{ref} is made available to allow use of this device as a high input impedance buffer gate.

- DIFFERENTIAL INPUT
- TRUE AND COMPLEMENT OUTPUT
- HIGH INPUT IMPEDANCE
- HIGH SPEED . . . 3.0 ns
- OUTPUTS PRE-LOADED WITH 2K
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- 50 Ω LINE DRIVER CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP

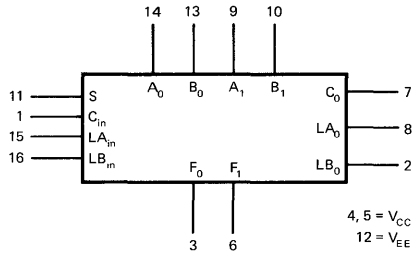


95H84 2 BIT ADDER/SUBTRACTOR

DESCRIPTION Performs addition and subtraction on two bits with full internal carry look ahead expandable between units. No additional carry look ahead unit is required. Can be implemented to add or subtract 2 64 bit words within 20 nsec at a power comparable to a TTL adder with carry look ahead units.

An arithmetic logic unit using 95H84 for adders, 9528 and 34 for registers and a scratchpad memory of 9538 and 95H40 could effectively process 32 bit words at a 40 MHz clock rate using a multiphase clocking scheme.

- HIGH SPEED . . . 1.5 ns INTERNAL GATE DELAYS
- ADDS AND SUBTRACTS WITH ONE DEVICE
- INTERNAL CARRY LOOKAHEAD
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS – ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER



ACTIVE HIGH BLOCK DIAGRAM

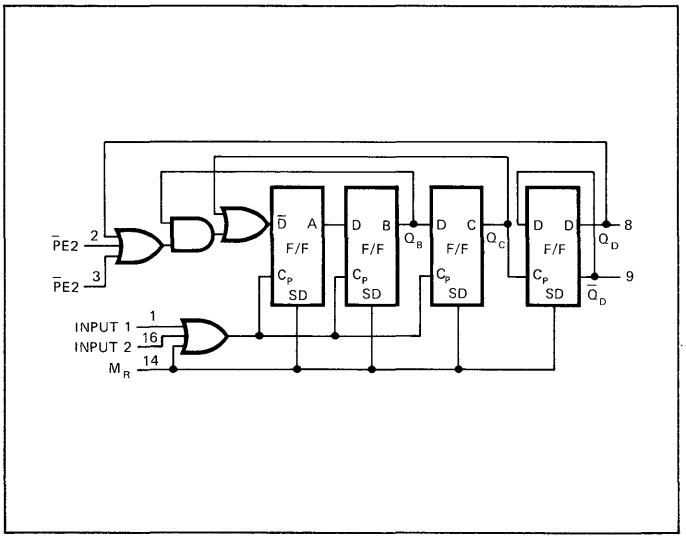
A_0, B_0, A_1, B_1	- OPERAND INPUTS
F_0, F_1	- FUNCTION OUTPUTS
S	- SUBTRACT SELECT LINE
C_{in}, C_0	- CARRY IN AND OUT
LA_n, LB_{in}	- CARRY LOOKAHEAD INPUTS FROM PREVIOUS UNIT
LA_0, LB_0	- CARRY LOOKAHEAD OUTPUTS TO FOLLOWING UNIT

95H90 VHF PRESCALER ÷ 10/11

DESCRIPTION The 95H90 prescaler is a high speed ECL MSI designed specifically for the communication and instrumentation manufacturer. In its simplest use it will divide any clock frequency up to 250 MHz, by 10. By using the 9590 with other control logic a divide by 10/11 logic control element allows a divide by "N" counter to be constructed with a max frequency over 250 MHz.

By keeping all the high speed logic manipulation "on chip", a dramatic decrease in power and increase in reliability and wire-ability are made available at much lower cost than a comparable SSI function.

- HIGH SPEED . . . 300 MHz
- ÷10/11 ENABLE
- HIGH SPEED RESET
- WIRED OR CAPABILITY
- SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS ELIMINATE NOISE COUPLING
- TEMPERATURE COMPENSATION
- INTERNAL PULL DOWN
- 50 Ω LINE DRIVE CAPABILITY
- SINGLE –5.2 VOLT POWER SUPPLY
- HERMETIC CERAMIC 16 PIN DIP
- COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER

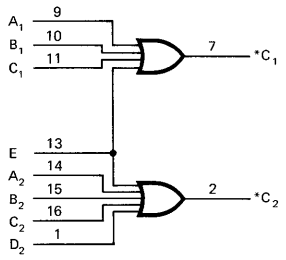


9595 DUAL ECL/TTL CONVERTER

DESCRIPTION The 9595 is a high speed logic converter for use in systems using both the high speed of ECL and the many available functions of TTL. The 9595 requires the –5.2 volt V_{EE} supply of ECμL and the +5 volt V_{CC} of TTL. The TTL fanout of 4 may be expanded by adding more pulldown current at the TTL output pin.

By allowing the logic converter to function as a logic gate the normally wasted time of logic conversion may be used in the logic implementation with the through delay generally less than that found in TTL circuits.

- HIGH SPEED . . . 6 ns
- FAN OUT 10
- NO INVERSION THROUGH CONVERTER
- ECL INPUT TEMPERATURE COMPENSATED
- INTERNAL PULL DOWNS
- HERMETIC CERAMIC 16 PIN DIP
- FUNCTIONS AS DUAL 2 INPUT GATE
- MULTIPLE LOGIC GATE CAPABILITY



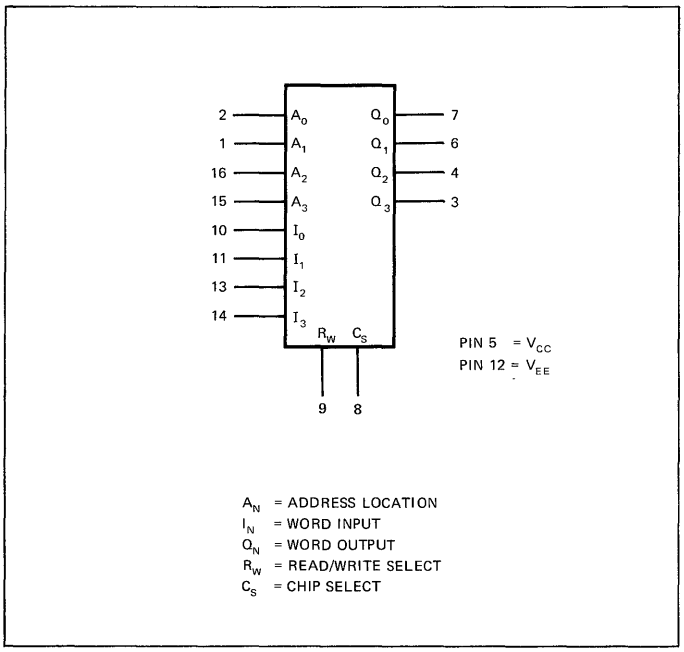
* = CCSL, UP TO 4 LOADS, UP TO 10 WITH EXTERNAL R TO V_{EE}

95400 64 BIT MEMORY

DESCRIPTION The 95400 is a very high speed 64 bit memory organized 16 words by 4 bits. Internal decoding is employed with the 16 words selected through four address lines. A chip select input, read/write control line, and OR-tieable outputs are also provided.

The 16x4 organization was chosen as optimum for small high speed scratchpad applications. For word capacities in excess of 16, the 9538 decoder will permit expansion with very little decrease in overall speed.

- **HIGH SPEED . . . 12 ns ACCESS TIME**
- **LARGE CAPACITY – 64 BITS**
- **OPTIMIZED FOR SMALL WORDS – 16 x 4**
- **HIGH SPEED CHIP ENABLE FOR EASE OF EXPANSION**
- **WIRED-OR CAPABILITY**
- **TEMPERATURE COMPENSATION**
- **ALL INPUTS AND OUTPUTS OPEN FOR EASE OF EXPANSION**
- **50 Ω LINE DRIVE CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**
- **COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER**



95401 16 BIT SCRATCHPAD MEMORY

DESCRIPTION This element is a 16 bit monolithic integrated memory element designed for use in very high speed scratchpad memory applications. The element consists of 16 nonsaturating bistable storage cells arranged in an addressable four-by-four matrix.

The logic diagram below indicates the X and Y address lines, sense zero and sense one, S_0, S_1 and write zero and write one. W_0, W_1, pin locations.

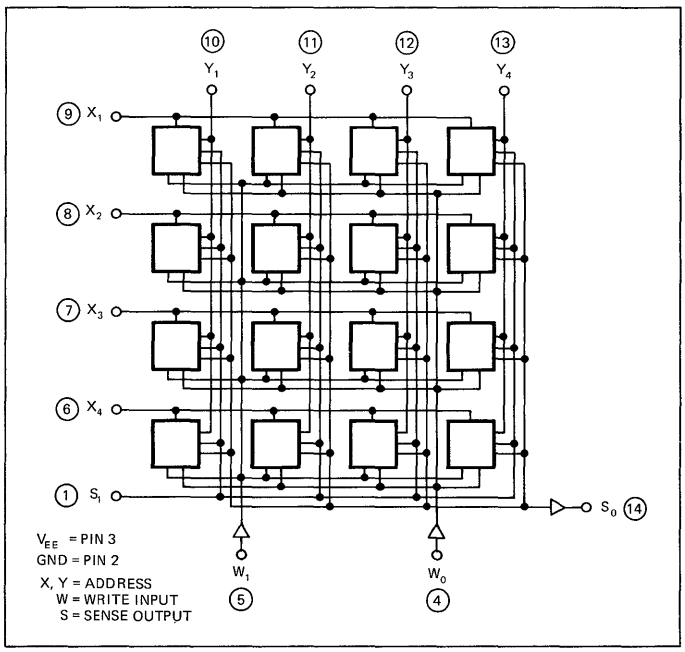
All outputs are normal logic "0" for ease of expansion to larger word sizes.

A desired bit location is selected by raising the coincident X–Y address lines to a logic "1" (typically –0.8 volts) and holding the nonselected address lines at logic "0" (typically –1.6 volts). The data, and its complement stored at the addressed location are read at the sense output terminals. If a "1" is stored, terminal S_1 will be at logical "1", if "0" is stored, terminal S_0 will be at "1".

Writing a logical "1" is accomplished by raising W_1 to "1" and addressing the appropriate location, as for sensing. A logic "0" is stored by applying "1" to terminal W_0.

This element is available in the hermetically sealed, 14 lead ceramic Dual-In-line Package, suitable for operation over the temperature range 0°C to 75°C. This device is second sourced by RCA as the CD2155D.

- **HIGH SPEED – ACCESS TIME <6 ns, READ/WRITE CYCLE TIME <18 ns**
- **OUTPUT WIRE – OR FACILITY FOR WORD EXPANSION**
- **NON-DESTRUCTIVE READ-OUT**
- **TRUE AND COMPLEMENTARY OUTPUTS PROVIDED**
- **50 Ω LINE DRIVE CAPABILITY**
- **ECL COMPATIBLE – LOGIC "1" TYPICALLY –0.8V**
  – LOGIC "0" TYPICALLY –1.6V
- **SINGLE POWER SUPPLY (–5.0V/–5.2V)**
- **POWER DISSIPATION TYPICALLY 300 mW**



DATA SHEETS

9502 • 9503 • 9504

HIGH SPEED GATES

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The 9502, 9503 and 9504 are temperature compensated ECμL OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve high speed. The elements are intended for the design of high speed central processors, terminals, instrumentation and digital communications systems.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range. Input and output 2 kΩ pulldown resistors eliminate the necessity for external termination of lines up to 6-8 inches and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The devices are packaged in the hermetic CERAMIC, 16 pin Dual In-Line Package and specified for operation over the temperature range 0°C to 75°C.

- **HIGH SPEED . . . 2.3 ns PER GATE**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS — ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **COMMON ENABLE INPUTS**
- **LOW CROSSTALK AND NOISE GENERATION**
- **WIRE-OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **COMPLEMENTARY OR/NOR OUTPUTS (9502, 9503)**
- **SINGLE —5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

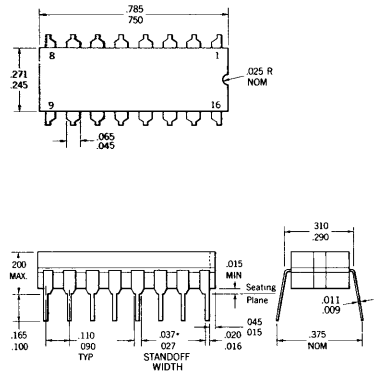
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

ORDER INFORMATION

Specify U6B9502XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range for 9502 gate. Substitute 9503 or 9504 for other elements.

PHYSICAL DIMENSIONS
16 LEAD DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
The .027/.037 dimensions does not apply to the corner leads

FUNCTIONAL DESCRIPTION

The 9500 Series Temperature Compensated ECμL Gates are based on the current switch-emitter follower (CSEF), or emitter coupled (ECμL), configuration of Figure 1. Additional circuit complexity compared with conventional ECμL is incorporated to improve system operating characteristics. This includes temperature compensation networks to insure that logic levels and thresholds, set by the on chip bias driver, are essentially independent of temperature. On chip output emitter follower and input pulldown 2 k ohm resistors reduce external components normally required for short line termination and unused logic inputs. A current source in the tail of the differential amplifier equalizes ONE and ZERO level noise margins by removing the NOR side saturation knee, and also improves saturation temperature dependency.

Defining logic "ONE" as $V_{OH} = -895$ mV (typ) and logic "ZERO" as $V_{OL} = -1710$ mV (typ), the elements perform the logical NOR and OR functions. The opposite definition specifies NAND/AND operation. All parameters specified in the characteristics are defined by the algebraic maximum and minimum limits.

Gate pin configurations are indicated in Fig. 2. An input enable line common to all gates in each package is provided for additional logical flexibility.

Fig. 1 — CIRCUIT SCHEMATIC

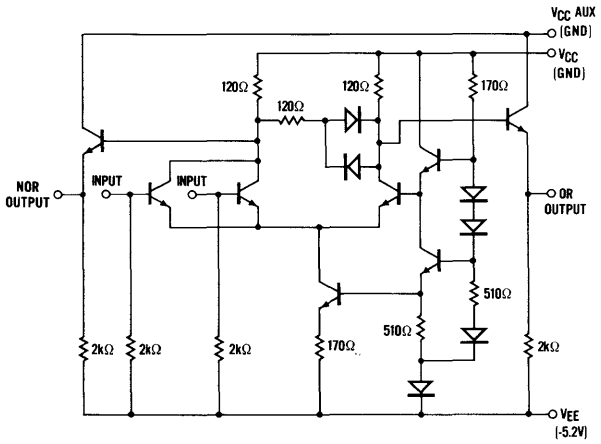
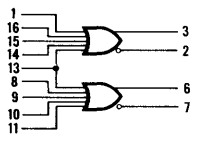


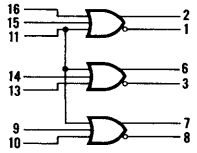
Fig. 2 — LOGIC DIAGRAM AND PIN CONNECTION

9502



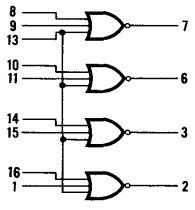
Dual 4 OR/NOR
(with enable)

9503



Triple 2 OR/NOR
(with enable)

9504



Quad 2 NOR
(with enable)

On all elements
Pins 4 and 5
are circuit
ground, V_{CC}
Pin 12 is
V_{EE}, −5.2 V

D.C. ELECTRICAL CHARACTERISTICS (Industrial Temperature Range 0°C to +75°C, V_{CC} = Gnd, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
$I_{IN}(1)$	Input Current at V_{IH}											
	Standard Gate		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = −900 mV to each input sequentially
	Enable Lines											
	9502		4.60	6.30		4.50	6.20		4.30	6.00	mA	
	9503		6.90	9.45		6.75	9.30		6.45	9.00	mA	
	9504		9.20	12.60		9.00	12.40		8.60	12.00	mA	
$I_{IN}(0)$	Input Current at V_{IL}											
	Standard Gate		1.80	2.40		1.75	2.35		1.65	2.25	mA	V_{IL} = −1700 mV to each input sequentially
	Enable Lines											
	9502		3.60	4.80		3.50	4.70		3.30	4.50	mA	
	9503		5.40	7.20		5.25	7.05		4.95	6.75	mA	
	9504		7.20	9.60		7.00	9.40		6.60	9.00	mA	
I_{PD}	Power Supply Current											
	9502	25	33	43	29	35	44	30	37	48	mA	All inputs
	9503	35	46	59	40	48	60	40	51	65	mA	open
	9504	40	52	67	45	54	68	41	57	74	mA	
ΔI_{IN}	Input Saturation Test									50	μA	See Fig. 4 $\Delta I_{IN} = I_B - I_A$ $I_A = I_{IN}$ @ V_{IN} = 800 mV $I_B = I_{IN}$ @ V_{IN} = 750 mV

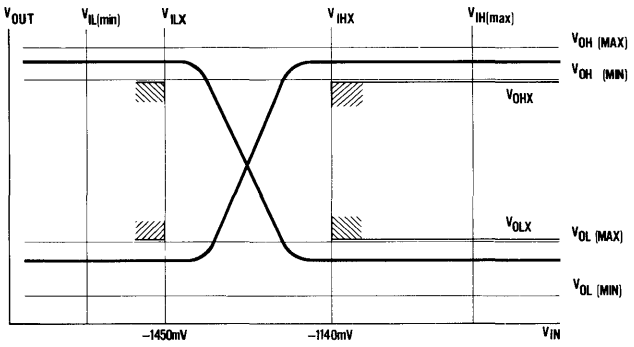
A.C. ELECTRICAL CHARACTERISTICS (Industrial Temperature Range 0°C to +75°C)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
t_{pd}	Propagation Delay											
	t_{pd--}		2.3			2.3	3.5		2.5		ns	See Fig. 5
	t_{pd++}		2.2			2.2	3.5		2.4		ns	R_L = 50 Ω to −2.0 V
	t_{pd-+}		2.4			2.4	3.5		2.6		ns	C_L <5.0 pF
	t_{pd+-}		2.5			2.5	3.2		2.7		ns	$t_r = t_f$ = 2.5 ns
t_r	Rise Time	1.5		4.5	1.5	3.0	4.5	1.5		4.5	ns	See Fig. 5 R_L = 50 Ω to −2.0 V C_L <5.0 pF
t_f	Fall Time	1.5		4.5	1.5	3.0	4.5	1.5		4.5	ns	See Fig. 5 R_L = 50 Ω to −2.0 V C_L <5.0 pF
I_T	Transient Input Current											
	Standard Gate					2.5	3.5				mA	See Fig. 6 on Page 5
	Enable Lines											
	9502					3.4	4.5				mA	
	9503					4.7	5.7				mA	
	9504					5.0	6.0				mA	
t_{pd}	Propagation Delay											
	t_{pd--}		2.6			2.6	3.5		2.8		ns	See Fig. 5
	t_{pd++}		2.5			2.5	3.5		2.7		ns	R_L = 50 Ω to −2.0 V
	t_{pd-+}		2.7			2.7	3.5		2.9		ns	C_L = 15 pF ±5%
	t_{pd+-}		2.8			2.8	3.5		3.0		ns	$t_r = t_f$ = 2.5 ns

D.C. ELECTRICAL CHARACTERISTICS (Industrial Temperature Range 0°C to +75°C, V_{CC} = Gnd, V_{EE} = −5.2 V)

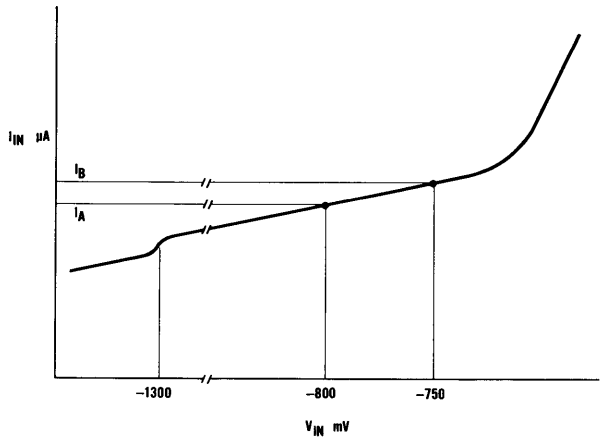
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C TYP.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage											V_{IL} = −1700 mV
	F.O. = 1 gate	−900	−850	−800	−900	−850	−800	−890	−840	−790	mV	for NOR gate
	F.O. = 5 gates	−940	−890	−840	−940	−890	−840	−940	−890	−840	mV	V_{IH} = −900 mV
	50 Ω to −2.0 V	−975	−925	−875	−975	−925	−875	−975	−925	−875	mV	for OR gate
V_{OL}	Output Low Voltage											V_{IL} = −1700 mV
	F.O. = 1 gate	−1745	−1670	−1595	−1745	−1670	−1595	−1745	−1670	−1595	mV	for OR gate
	F.O. = 5 gates	−1785	−1710	−1635	−1785	−1710	−1635	−1785	−1710	−1635	mV	V_{IH} = −900 mV
	50 Ω to −2.0 V	−1775	−1700	−1625	−1775	−1700	−1625	−1775	−1700	−1625	mV	for NOR gate
V_{OHX}	Output High Voltage at V_{IN} (threshold)											See Fig. 3 / V_{ILX} = −1450 mV for NOR gate / V_{IHX} = −1140 mV for OR gate — To each input sequentially (other inputs open)
	F.O. = 1 gate	−910			−910			−900			mV	
	F.O. = 5 gates	−950			−950			−950			mV	
	50 Ω to −2.0 V	−985			−985			−985			mV	
V_{OLX}	Output Low Voltage at V_{IN} (threshold)											See Fig. 3 / V_{ILX} = −1450 mV for OR gate / V_{IHX} = −1140 mV for NOR gate — To each input sequentially (other inputs open)
	F.O. = 1 gate			−1585			−1585			−1585	mV	
	F.O. = 5 gates			−1625			−1625			−1625	mV	
	50 Ω to −2.0 V			−1615			−1615			−1615	mV	

Fig. 3 — NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

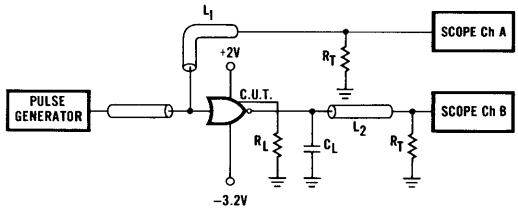
Fig. 4 — INPUT SATURATION TEST

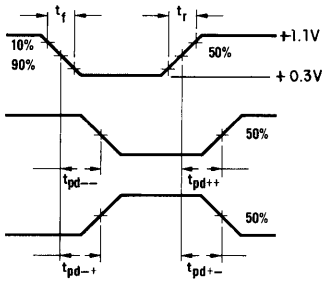


This test insures that the input transistor is not in saturation at $V_{IN} = 750$ mV. This represents a worst case condition with the driving gate at V_{OH} (min) = 750 mV (ie. for $T_A = 75°C$ this is equivalent to driving gate into FO = 1 with its power supply at −5%).

Saturation is defined as no increase in collector current for 20% increase in base drive current I_R. The effect is to increase t_{pd}.

Fig. 5 — SWITCHING TIME TEST CIRCUIT AND WAVEFORM



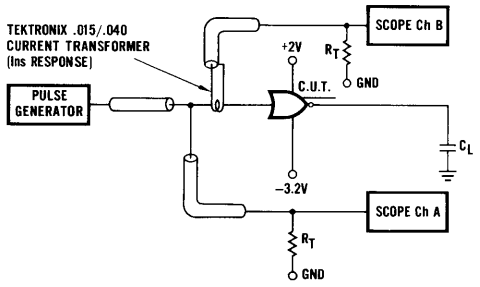


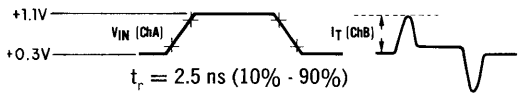
$t_r = t_f = 2.5$ ns (10% - 90%) Jig setup with no circuit under test

$V_{CC} = V_{CC}$ (AUX) = +2.0 V

$V_{EE} = -3.2$ V

Fig. 6 — TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS





This test provides a measure of the average value of C_{IN}; also current mismatch in the line.

$V_{CC} = V_{CC}$ (AUX) = +2.0 V

$V_{EE} = -3.2$ V

L_1 and L_2 = equal length 50 Ω impedance lines

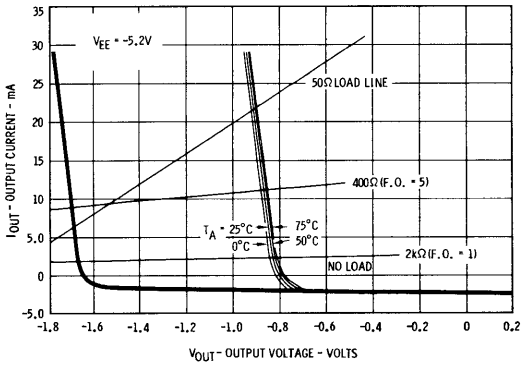
$R_L = R_T = 50$ Ω Termination of Scope

C_L = Jig and Stray Capacitance < 5.0 pF

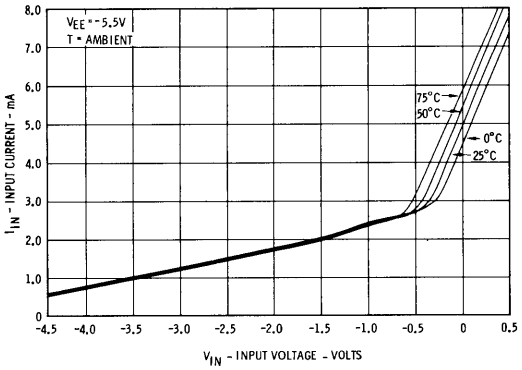
Logic levels for Figs. 5 and 6 are nominal values at 50 Ω fanout determined by indicated power supplies. These values chosen to permit use of scope 50 Ω termination to ground.

Decoupling 0.1 μF from GND to V_{EE}.

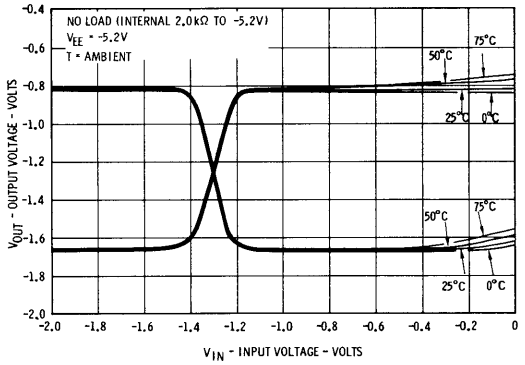
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



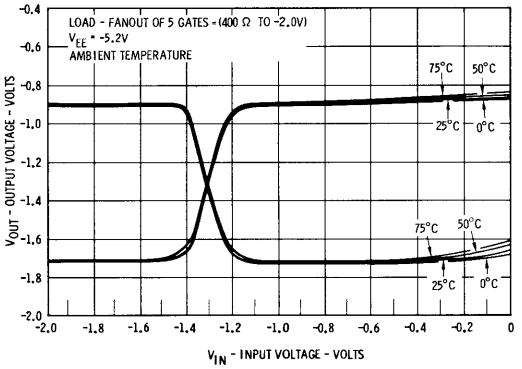
INPUT CURRENT VERSUS INPUT VOLTAGE



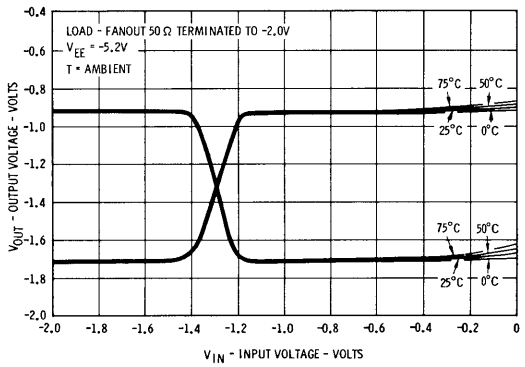
TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



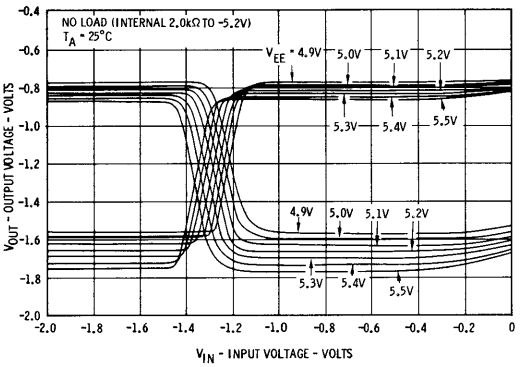
TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



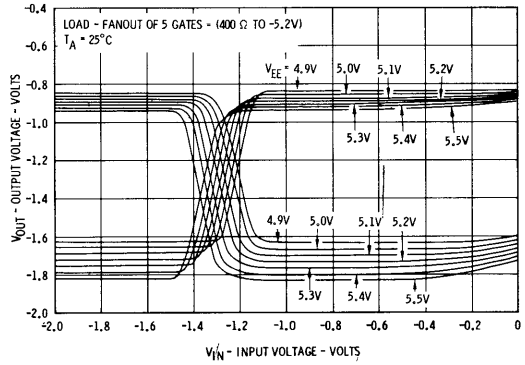
TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



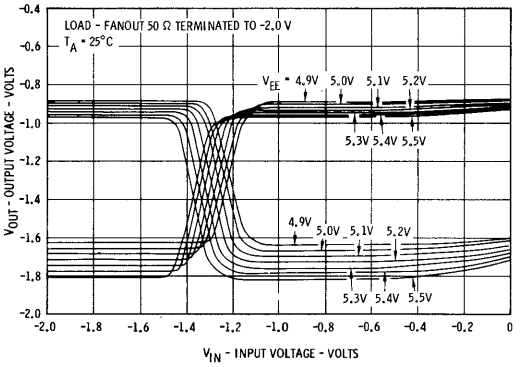
TRANSFER CHARACTERISTICS VERSUS POWER SUPPLY VARIATION



TRANSFER CHARACTERISTICS VERSUS POWER SUPPLY VARIATION

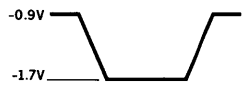


TRANSFER CHARACTERISTICS VERSUS POWER SUPPLY VARIATION

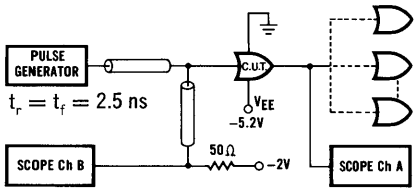


TYPICAL PROPAGATION DELAY VERSUS FAN OUT

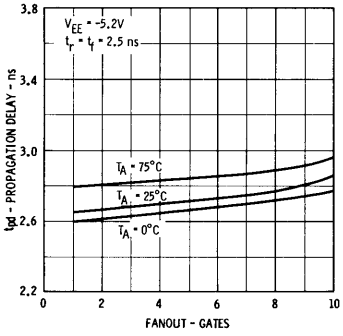
INPUT WAVEFORM



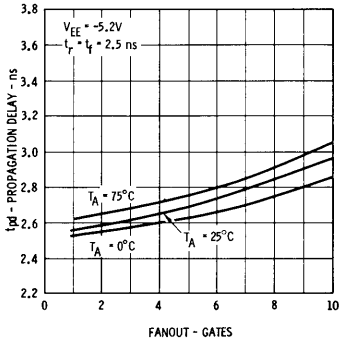
$t_r = t_f = 2.5$ ns (10% - 90%)



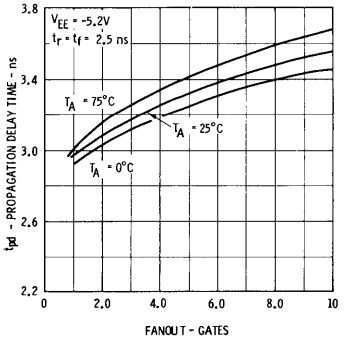
TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd++} (OR output)



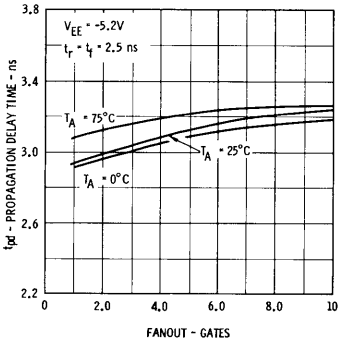
TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd--} (OR output)



TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd+-} (NOR output)



TYPICAL PROPAGATION DELAY VERSUS FANOUT t_{pd-+} (NOR output)

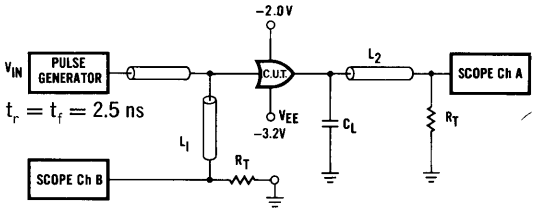


TYPICAL PROPAGATION DELAY VERSUS CAPACITIVE LOAD (in a 50 ohm system)

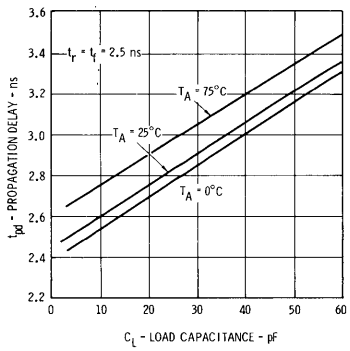
INPUT WAVEFORM

$t_r = t_f = 2.5$ ns (10% - 90%)

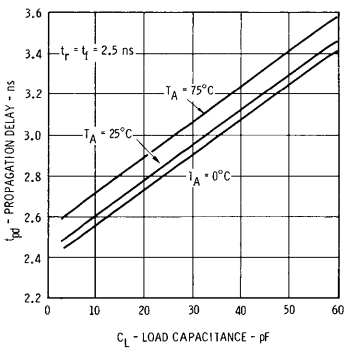
$V_{CC} = V_{CC}(AUX) = +2.0$ V
$V_{EE} = -3.2$ V
$R_T = 50\ \Omega$ Termination of scope
L_1 & L_2 = Equal length 50 Ω impedance lines



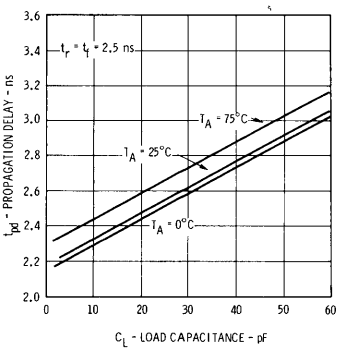
TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd+-} (NOR output)



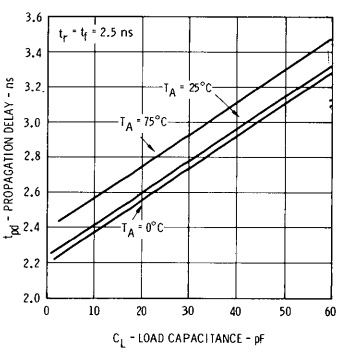
TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd-+} (NOR output)



TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd++} (OR output)

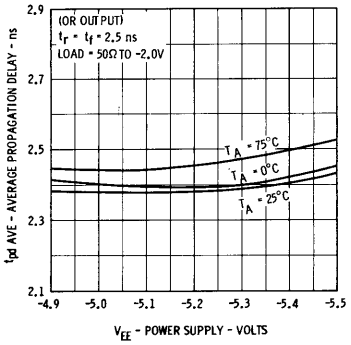


TYPICAL PROPAGATION DELAY VERSUS LOAD CAPACITANCE t_{pd--} (OR output)

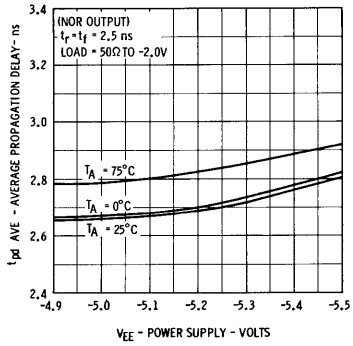


TYPICAL AVERAGE PROPAGATION DELAY VERSUS POWER SUPPLY

TYPICAL AVERAGE PROPAGATION DELAY VERSUS POWER SUPPLY



TYPICAL AVERAGE PROPAGATION DELAY VERSUS POWER SUPPLY



$$t_{pd\ ave} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

APPLICATIONS NOTES

INTERCONNECTION RECOMMENDATIONS

All high speed ECμL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECμL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a −2 volt supply: $R = \frac{Z_O}{1 - NZ_O/2000}$ where Z_O is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6\,R$ connected to ground and $R_2 = 2.6\,R$ connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

The 9500 series ECμL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

95H02 • 95H03 • 95H04

VERY HIGH SPEED GATES

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 95H02, 95H03 and 95H04 are temperature compensated ECL OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve high speed. The elements are intended for the design of high speed central processors, terminals, instrumentation and digital communications systems.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range. Input and output 2 kΩ pulldown resistors eliminate the necessity for external termination of lines up to 6-8 inches and unused logic inputs. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The devices are packaged in the hermetic CERAMIC, 16 pin Dual In-Line Package and specified for operation over the temperature range 0°C to 75°C.

- **PIN IDENTICAL TO LOWER SPEED GATES (9502 • 9503 • 9504)**
- **VERY HIGH SPEED . . . 1.7 ns PER GATE**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **COMMON ENABLE INPUTS**
- **LOW CROSSTALK AND NOISE GENERATION**
- **WIRED–OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **COMPLEMENTARY OR/NOR OUTPUTS (9502, 9503)**
- **SINGLE –5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

ORDER INFORMATION – Specify U6B95H02XX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range for 95H02 gate. Substitute 95H03 or 95H04 for other elements.

CIRCUIT SCHEMATIC

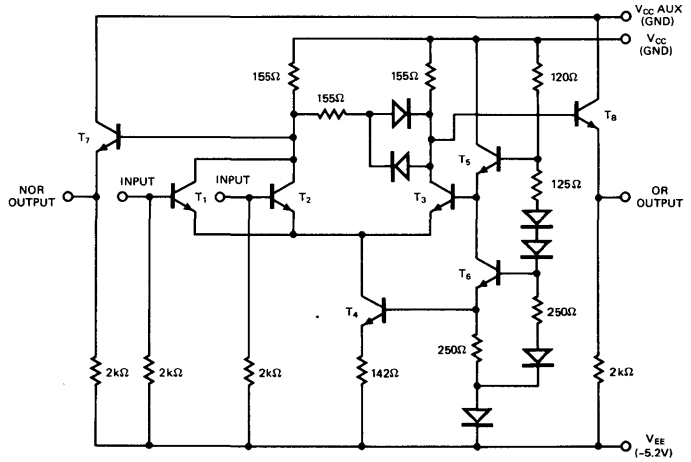
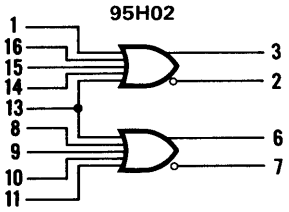


Fig. 1

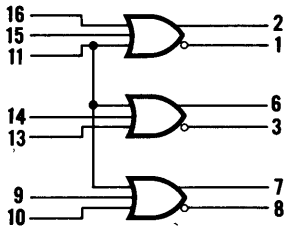
LOGIC DIAGRAM AND PIN CONNECTION

95H02



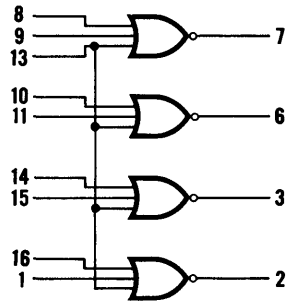
Dual 4 OR/NOR
(with enable)

95H03



Triple 2 OR/NOR
(with enable)

95H04



Quad 2 NOR
(with enable)

On all elements Pins 4 and 5 are circuit ground, V_{CC}.
Pin 12 is V_{EE}, –5.2 V

Fig. 2

FUNCTIONAL DESCRIPTION — The 9500 Series Temperature Compensated ECL Gates are based on the current switch-emitter follower (CSEF), or emitter coupled (ECL), configuration of Figure 1. Additional circuit complexity compared with conventional ECL is incorporated to improve system operating characteristics. This includes temperature compensation networks to insure that logic levels and thresholds, set by the on chip bias driver, are essentially independent of temperature. On chip output emitter follower and input pulldown 2 k ohm resistors reduce external components normally required for short line termination and unused logic inputs. A current source in the tail of the differential amplifier equalizes ONE and ZERO level noise margins by removing the NOR side saturation knee, and also improves saturation temperature dependency.

Defining logic "ONE" as V_{OH} = –900 mV (typ) and logic "ZERO" as V_{OL} = –1700 mV (typ), the elements perform the logical NOR and OR functions. The opposite definition specifies NAND/AND operation. All parameters specified in the characteristics are defined by the algebraic maximum and minimum limits.

Gate pin configurations are indicated in Fig. 2. An input enable line common to all gates in each package is provided for additional logical flexibility.

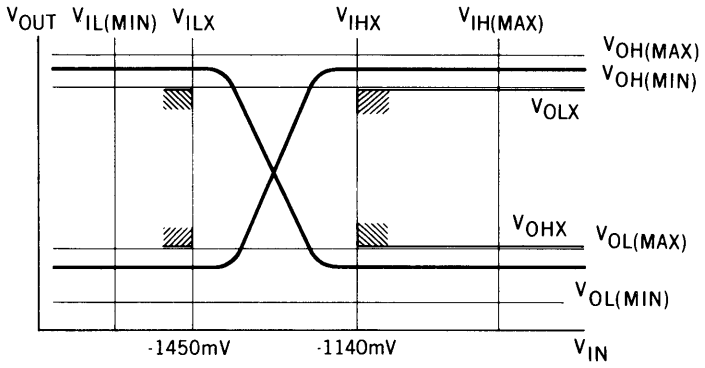
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	–6 Volts
Supply Voltage V_{EE} (Pulsed)	–8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

D.C. ELECTRICAL CHARACTERISTICS (Operating Temperature Range: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = –5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS		CONDITIONS
V_{OH}	Output Voltage High		–860 –910 –950		mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	$V_{IN} = V_{IL}$ = –1700 mV for NOR Gate $V_{IN} = V_{IH}$ = –900 mV for OR Gate
V_{OL}	Output Voltage Low		–1690 –1740 –1720		mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	$V_{IN} = V_{IH}$ = –900 mV for NOR Gate $V_{IN} = V_{IL}$ = –1700 mV for OR Gate
V_{OHX}	Output Voltage High at $V_{IN} = V_{IX}$ (Threshold)	–930 –970 –1010			mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	See Fig. 3 $V_{IN} = V_{ILX}$ = –1450 mV for NOR Gate $V_{IN} = V_{IHX}$ = –1140 mV for OR Gate
V_{OLX}	Output Voltage Low at $V_{IN} = V_{IX}$ (Threshold)			–1605 –1655 –1635	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	See Fig. 3 $V_{IN} = V_{ILX}$ = –1450 mV for OR Gate $V_{IN} = V_{IHX}$ = –1140 mV for NOR Gate
V_{IHX}	Guaranteed Input High Threshold Voltage	–1140			mV		Guaranteed Input High Threshold Voltage
V_{ILX}	Guaranteed Input Low Threshold Voltage			–1450	mV		Guaranteed Input Low Threshold Voltage
$V_{IN(H)}$	Input Current High		2.40	3.58	mA		V_{IN} = –900 mV to Common Enable Input
$V_{IN(H)}$	Input Current High		2.25	3.16	mA		V_{IN} = –900 mV to Other Inputs Sequentially
$V_{IN(L)}$	Input Current Low		1.75	2.46	mA		V_{IN} = –1700 mV to Each Input Sequentially
I_{PS}	Power Supply Current				mA		All Inputs & Outputs Open
	95H02	26	34	45			
	95H03	36	49	64			
	95H04	48	62	80			

NOISE MARGIN SPECIFICATION POINTS



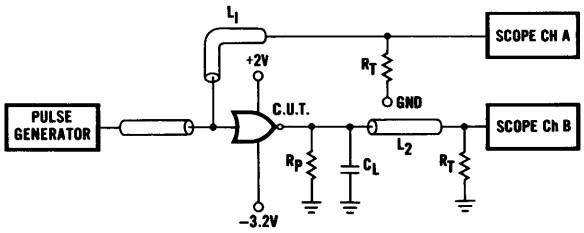
Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

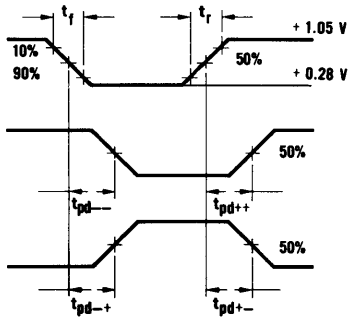
Fig. 3

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C)

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C TYP.	UNITS	CONDITIONS
	Propagation Delay							
t_{pd}	10% – 50%						ns	See Fig. 5
	t_{pd} – –	1.6	–	1.6	2.4	1.8		R_L = 50 Ω to –2 V
	t_{pd} + +	1.7	–	1.7	2.4	1.9		C_L <5 pF
	t_{pd} – +	1.6	–	1.6	2.4	1.8		$t_r = t_f$ = 2.2 ns (10 – 90%)
	t_{pd} + –	1.8	–	1.8	2.4	2.0		
t_f	Fall Time 10% – 90%	2.2	1.4	2.2	3.0	2.2	ns	
t_r	Rise Time 10% – 90%	2.2	1.4	2.2	3.0	2.2		

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





$t_r = t_f$ = 2.4 ns (10% - 90%)

Jig setup with no circuit under test.

$V_{CC} = V_{CC(AUX)}$ = +2.0 V

V_{EE} = –3.2 V

L_1 and L_2 = equal length 50 Ω impedance lines

$R_L = R_T$ = 50 Ω Termination of Scope

C_L = Jig and Stray Capacitance <5.0 pF

Logic levels for Fig. 5 is nominal values at 50 Ω fanout determined by indicated power supplies. These values chosen to permit use of scope 50 Ω termination to ground.

Decoupling 0.1 μF from GND to V_{EE}.

Fig. 4

APPLICATION

INTERCONNECTION RECOMMENDATIONS – All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

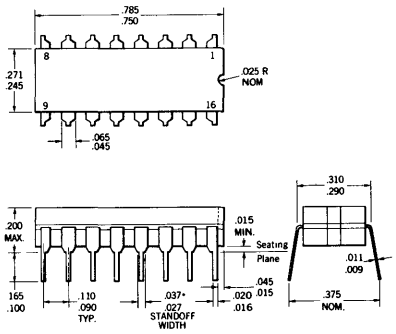
Microstrip interconnections may be terminated by a resistor to a −2 volt supply. Alternately, a 2 resistor divider network may be used with R_1 = 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY – The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

PHYSICAL DIMENSIONS
16 LEAD SSI DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
*The .037/.027 dimensions does not apply to the corner leads

9505

FOUR WIDE-OR AND/NAND (NOR-OR) GATE

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The ECL 9505 is a temperature compensated OR-AND gate that achieves in slightly over one basic gate delay, the AND of four different ORed functions.

The NOR outputs of the four OR gates are ORed to derive the OR-NAND (NOR-OR) function.

This element is useful in the design of Arithmetic Logic Units for construction of adders, multipliers, comparitors, etc. Just two 9505's will implement a full carry adder function.

FEATURES:

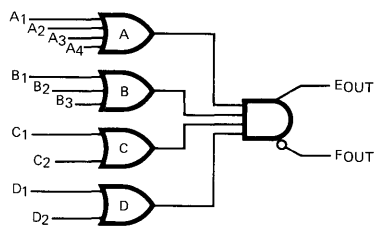
- **HIGH SPEED . . . 2.7 ns OR-AND, 2.5 ns OR-NAND**
- **COMPLEX LOGIC FUNCTION REDUCES PACKAGE COUNT**
- **WIRE OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **INTERNAL 2 k PULL DOWN RESISTORS**
- **TEMPERATURE COMPENSATED**
- **SEPARATE V_{CC} PINS - ELIMINATE NOISE COUPLING**

PIN NAMES

A_N = 4 Inputs to OR Gate A
B_N = 3 Inputs to OR Gate B
C_N = 2 Inputs to OR Gate C
D_N = 2 Inputs to OR Gate D
E_{OUT} = AND Output of Gates A, B, C and D
F_{OUT} = NAND Output of Gates A, B, C and D

ORDER INFORMATION — Specify U6B9505XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0° C to 75° C temperature range.

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)

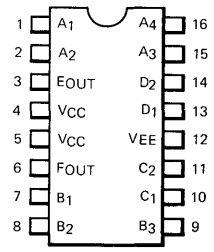
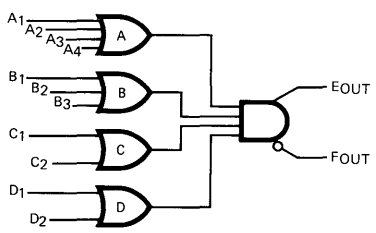


Fig. 2.

LOGIC DIAGRAM



$E = A_N \cdot B_N \cdot C_N \cdot D_N$
$F = A_N \cdot B_N \cdot C_N \cdot D_N$

Where:

$A_N = A_1 + A_2 + A_3 + A_4$,
$B_N = B_1 + B_2 + B_3$
$C_N = C_1 + C_2$
$D_N = D_1 + D_2$

Fig. 3.

FUNCTIONAL DESCRIPTION – The 9505 OR-AND gate combines two of the most often used functions in logic into one package to obtain maximum utilization of power and pin connections with minimum logic delay.

The AND of four OR gates is obtained by connecting the four collectors of the OR gates together with one collector load resistor and one emitter follower output device. High speed and temperature compensated output levels are maintained by a special controlled clamp at the collectors. This prevents saturation and loss of noise immunity as different logic conditions are encountered.

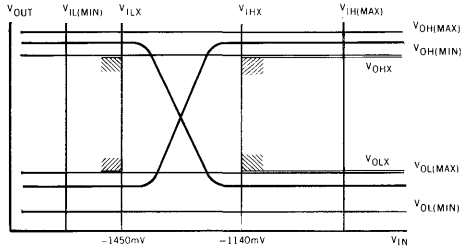
The NAND (NOR-OR) function is obtained by connecting the four NOR output emitter followers together at the output. In this way maximum speed is maintained with optimum use of package pins. This output is temperature compensated by an additional pulldown transistor on each NOR gate collector.

Selection of this input configuration of the four OR-NOR gates gives maximum utilization of available pins and meets almost all of the system requirements for this type of logic block.

DC ELECTRICAL CHARACTERISTICS (Operating Temperature: $T_A = 0°C$ to $75°C$, V_{CC} = GND, $V_{EE} = -5.2$ V

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
V_{OH}	Output Voltage High	–920	–850	–770	mV	F.O. = 1 Gate	$V_{IN} = V_{IH} = -900$ mV
		–960	–885	–790	mV	F.O. = 5 Gates	
		–995	–905	–805	mV	$R_L = 50\ \Omega$ to –2.0 V	
$V_{OL(OR\text{-}AND)}$	Output Voltage Low	–2055	–1750	–1595	mV	F.O. = 1 Gate	$V_{IN} = V_{IL} = -1700$ mV
		–2055	–1760	–1630	mV	F.O. = 5 Gates	
		–2055	–1755	–1625	mV	$R_L = 50\ \Omega$ to –2.0 V	
$V_{OL(OR\text{-}NAND)}$	Output Voltage Low	–1805	–1750	–1595	mV	F.O. = 1 Gate	$V_{IN} = V_{IH} = -900$ mV
		–1825	–1760	–1630	mV	F.O. = 5 Gates	
		–1815	–1755	–1625	mV	$R_L = 50\ \Omega$ to –2.0 V	
V_{OHX}	Output Voltage HIgh	–1005			mV	$R_L = 50\ \Omega$ to –2.0 V	$V_{IN} = V_{IHX} = -1140$ V for OR-AND $V_{IN} = V_{ILX} = -1450$ V for OR-NAND
V_{OLX}	Output Voltage Low			–1615	mV	$R_L = 50\ \Omega$ to –2.0 V	$V_{IN} = V_{ILX} = -1450$ V for OR-AND $V_{IN} = V_{IHX} = -1140$ V for OR-NAND
V_{IHX}	Input High Threshold Voltage	–1140			mV	Guaranteed Input High Voltage	
V_{ILX}	Input Low Threshold Voltage			–1450	mV	Guaranteed Input Low Voltage	
$I_{IN(1)}$	Input Current at V_{IH}			3.15	mA	$V_{IH} = -900$ mV to Each Input Sequentially	
$I_{IN(0)}$	Input Current at V_{IL}			2.40	mA	$V_{IL} = -1700$ mV to Each Input Sequentially	
I_{PS}	Power Supply Current	43	61	81	mA	All Inputs Open	

Fig. 4. NOISE MARGIN SPECIFICATION POINTS

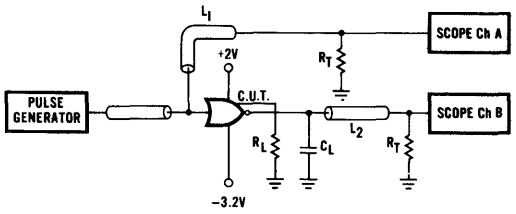


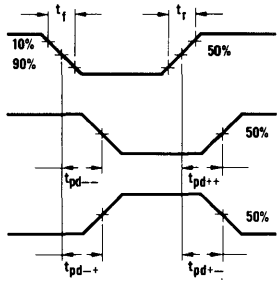
Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

AC ELECTRICAL CHARACTERISTICS (Operating Temperature: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS
		0°C	25°C			75°C				
		TYP	MIN	TYP	MAX	MIN	TYP	MAX		
	Propagation Delay									
	t_{pd++}	2.8		2.8	3.7		2.8		ns	R_L = 50 Ω to −2.0 V
t_{pd}	t_{pd--}	2.5		2.5	3.3		2.5		ns	C_L = 5.0 pF
	t_{pd+-}	2.4		2.4	3.2		2.4		ns	$t_r = t_f$ = 2.5 ns
	t_{pd-+}	2.4		2.4	3.2		2.4		ns	See Fig. 5
I_T	Transient Input Current			2.0	3.5				mA	See Fig. 6

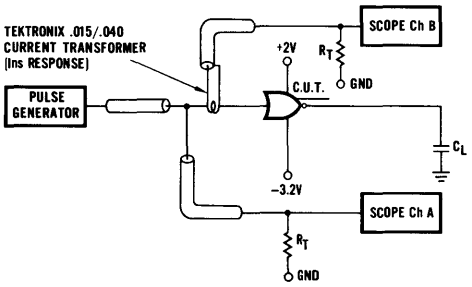
Fig. 5. SWITCHING TIME TEST CIRCUIT AND WAVEFORM

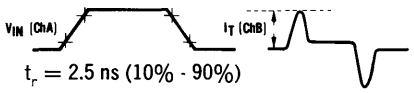




L_1 and L_2 = equal length 50 Ω impedance lines
$R_L = R_T$ = 50 Ω Termination of Scope
C_L = Jig and Stray Capacitance < 5.0 pF
$t_r = t_f$ = 2.5 ns (10% - 90%) Jig setup with no circuit under test
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

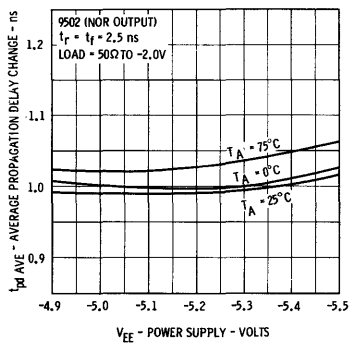
Fig. 6. TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS





This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = −3.2 V

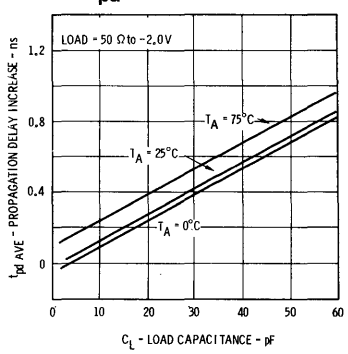
TYPICAL AVERAGE PROPAGATION DELAY CHANGE VERSUS POWER SUPPLY



$$t_{pd\ AVE} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

Reference:
AC Electrical Characteristic

TYPICAL PROPAGATION DELAY INCREASE VERSUS LOAD CAPACITANCE t_{pd} AVE (OR output)



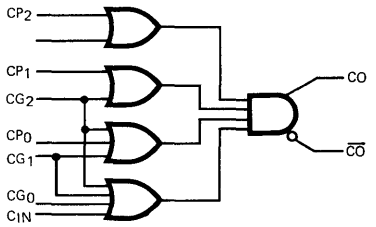


Fig. 7. **LOGIC EQUATIONS** – The 9505 is useful in implementing a large variety of logic equations with minimum propagation delay. As an example the equation for carry lookahead is:

$CO = CG_2+CG_1 \cdot CP_2+CG_0 \cdot CP_1 \cdot CP_2+C_{IN} \cdot CP_0 \cdot CP_1 \cdot CP_2$

An equivalent form of this equation is:

$\overline{CO} = \overline{CP}_2+\overline{CG}_2 \cdot \overline{CP}_1+\overline{CG}_1 \cdot \overline{CG}_2 \cdot \overline{CP}_0+\overline{CG}_0 \cdot \overline{CG}_1 \cdot \overline{CG}_2 \cdot \overline{C_{IN}}$

By DeMorgan's theorem this may be written as:

$CO = CP_2 \cdot (CG_2+CP_1)\,(CG_1+CG_2+CP_0)\,(CG_0+CG_1+CG_2+C_{IN})$

Fig. 8. **ADDER** – Two 9505's may be used to build a fast full adder.

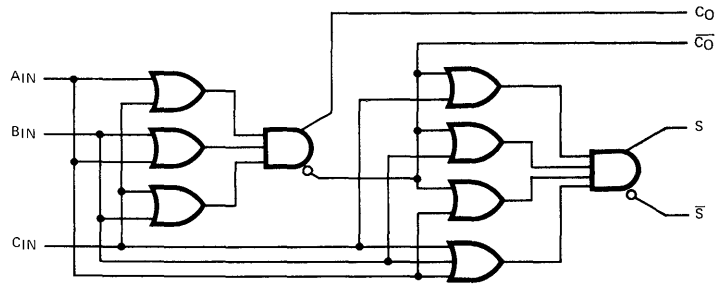


Fig. 9. **COMPARE CIRCUIT** – 9505's may be used to generate a compare circuit capable of handling two bit per 9505.

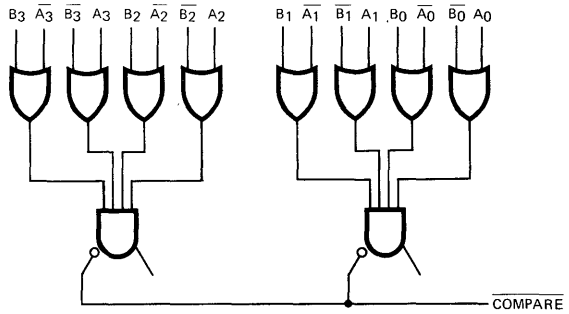
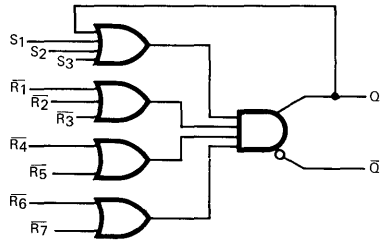
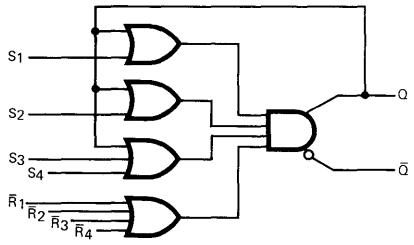


Fig. 10. **LATCHES** – A 9505 may be used to store one bit of information by connecting it as a latch. Many configurations of set and reset inputs are possible.

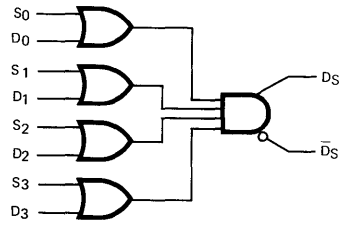


$S = S_1 + S_2 + S_3$ $\quad \overline{R} = (\overline{R}_1 + \overline{R}_2 + \overline{R}_3)(\overline{R}_4 + \overline{R}_5)(\overline{R}_6 + \overline{R}_7)$ $\quad R = R_1 \cdot R_2 \cdot R_3 + R_4 \cdot R_5 + R_6 \cdot R_7$



$S = S_1 \cdot S_2 \cdot (S_3 + S_4)$ $\quad \overline{R} = (\overline{R}_1 + \overline{R}_2 + \overline{R}_3 + \overline{R}_4)$ $\quad R = R_1 \cdot R_2 \cdot R_3 \cdot R_4$

Fig. 11. **MILTIPLEXERS** – A 9505 may be used as a 4 input multiplexer. A logic "0" on the selected S_N will allow D_N to be selected. All other S_N must be a "1".



INTERCONNECTION RECOMMENDATIONS

All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a −2 volt supply. Alternately, a 2 resistor divider network may be used with $R_1 = 1.6$ R connected to ground and $R_2 = 2.6$ R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

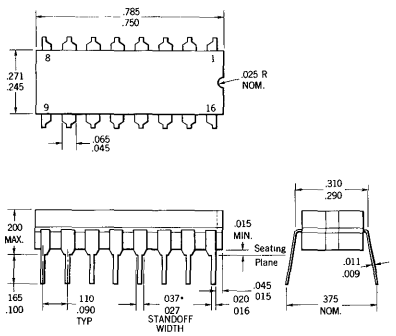
The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 Ω coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 Ω coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65° C to +150° C
Junction Temperature	+150° C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

PACKAGE INFORMATION

6B–16 LEAD SSI DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
* The .037/.027 dimensions does not apply to the corner leads

95L22 • 95L23 • 95L24

LOW POWER HIGH SPEED GATES

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 95L22, 95L23 and 95L24 are low power temperature compensated ECL OR/NOR Gates employing a nonsaturating current switch, emitter follower configuration to achieve high speed. The elements are intended for the design of high speed central processors, terminals, instrumentation and digital communications systems.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margin and speed remain relatively constant over a wide temperature range. High input impedance and open outputs allow effective usage of terminated line technology and large wired-OR ties. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The devices are packaged in the hermetic CERAMIC, 16 pin Dual In-Line Package and specified for operation over the temperature range 0°C to 75°C.

- **VERY HIGH SPEED . . . 2.0 ns PER GATE**
- **LOW POWER DISSIPATION OF 20 mW/GATE (TYP.)**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL HI–Z INPUT PULLDOWN RESISTORS**
- **COMMON ENABLE INPUTS**
- **LOW CROSSTALK AND NOISE GENERATION**
- **EXTENSIVE WIRED–OR CAPABILITY**
- **50 Ω LINE DRIVING CAPABILITY**
- **COMPLEMENTARY OR/NOR OUTPUTS (95L22, 95L23)**
- **SINGLE –5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

ORDER INFORMATION – Specify U6B95L22XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range for 95L22 gate. Substitute 95L23 or 95L24 for other elements.

CIRCUIT SCHEMATIC

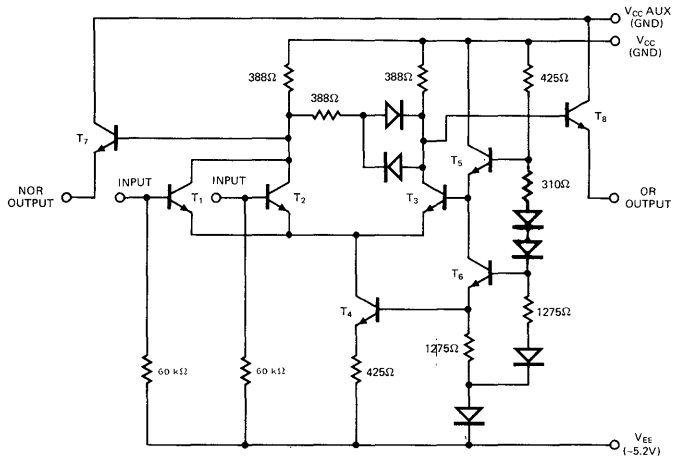
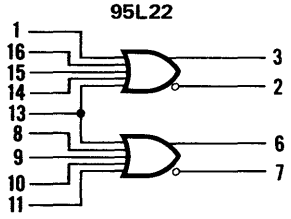


Fig. 1

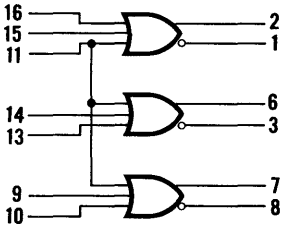
LOGIC DIAGRAM AND PIN CONNECTION

95L22



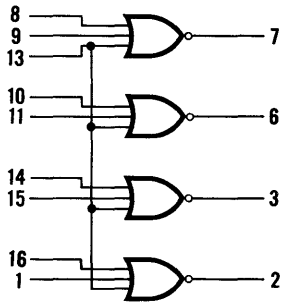
Dual 4 OR/NOR
(with enable)

95L23



Triple 2 OR/NOR
(with enable)

95L24



Quad 2 NOR
(with enable)

On all elements Pins 4 and 5 are circuit ground, V_{CC}. Pin 12 is V_{EE}, –5.2 V

Fig. 2

FUNCTIONAL DESCRIPTION – The 9500 Series Temperature Compensated ECL Gates are based on the current switch-emitter follower (CSEF), or emitter coupled (ECL), configuration of Figure 1. Additional circuit complexity compared with conventional ECL is incorporated to improve system operating characteristics. This includes temperature compensation networks to insure that logic levels and thresholds, set by the on chip bias driver, are essentially independent of temperature. A current source in the tail of the differential amplifier equalizes ONE and ZERO level noise margins by removing the NOR side saturation knee, and also improves saturation temperature dependency.

Defining logic "ONE" as V_{OH} = –960 mV (typ) and logic "ZERO" as V_{OL} = –1720 mV (typ), the elements perform the logical NOR and OR functions. The opposite definition specifies NAND/AND operation. All parameters specified in the characteristics are defined by the algebraic maximum and minimum limits.

Gate pin configurations are indicated in Fig. 2. An input enable line common to all gates in each package is provided for additional logical flexibility.

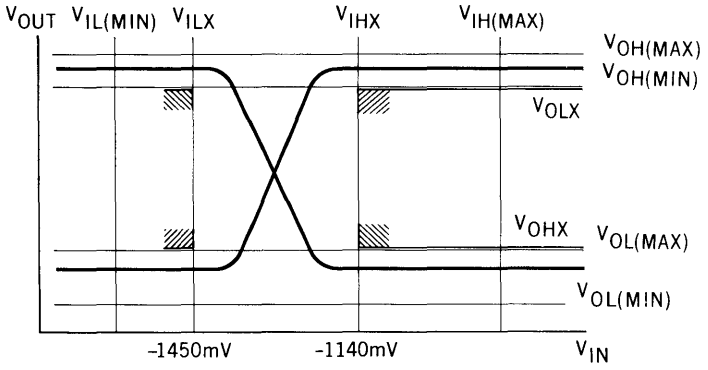
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	–65° C to +150° C
Junction Temperature	+150° C
Supply Voltage V_{EE} (Continuous)	–6 Volts
Supply Voltage V_{EE} (Pulsed)	–8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

D.C. ELECTRICAL CHARACTERISTICS (Operating Temperature Range: T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = –5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
V_{OH}	Output Voltage High		–960		mV	50 Ω to –2.0 V	$V_{IN} = V_{IL}$ = –1700 mV for NOR Gate $V_{IN} = V_{IH}$ = –900 mV for OR Gate
V_{OL}	Output Voltage Low		–1720		mV	50 Ω to –2.0 V	$V_{IN} = V_{IL}$ = –1700 mV for OR Gate $V_{IN} = V_{IH}$ = –900 mV for NOR Gate
V_{OHX}	Output Voltage High at $V_{IN} = V_{IX}$ (Threshold)	–1040			mV	50 Ω to –2.0 V	See Fig. 3 $V_{IN} = V_{ILX}$ = –1450 mV for NOR Gate $V_{IN} = V_{IHX}$ = –1140 mV for OR Gate
V_{OLX}	Output Voltage Low at $V_{IN} = V_{IX}$ (Threshold)			–1615	mV	50 Ω to –2.0 V	See Fig. 3 $V_{IN} = V_{ILX}$ = –1450 mV for OR Gate $V_{IN} = V_{IHX}$ = –1140 mV for NOR Gate
V_{IHX}	Guaranteed Input High Threshold Voltage	–1140			mV		Guaranteed Input High Threshold Voltage
V_{ILX}	Guaranteed Input Low Threshold Voltage			–1450	mV		Guaranteed Input Low Threshold Voltage
$V_{IN(H)}$	Input Current High		0.14	0.30	mA		V_{IN} = –900 mV to Common Enable Input
$V_{IN(H)}$	Input Current High		0.06	0.20	mA		V_{IN} = –900 mV to Other Inputs Sequentially
$V_{IN(L)}$	Input Current Low		.035	.125	mA		V_{IN} = –1700 mV to Each Input Sequentially
I_{PS}	Power Supply Current				mA		V_{EE} = –5.2 V, V_{CC} = GND All Inputs and Outputs Open
	95L22	7.0	10.5	15			
	95L23	9.0	13	18			
	95L24	11	16	22			

NOISE MARGIN SPECIFICATION POINTS



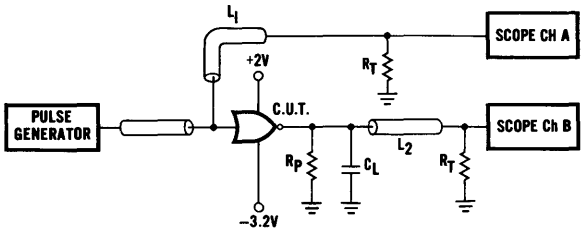
Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

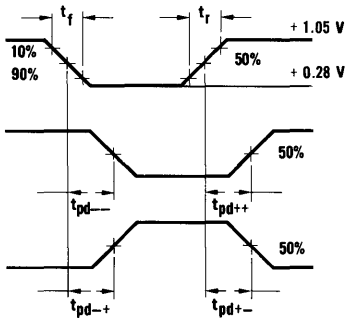
Fig. 3

AC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C)

SYMBOL	CHARACTERISTICS	LIMITS 0°C TYP.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C TYP.	UNITS	CONDITIONS
t_{pd}	Propagation Delay							
	10% – 50%						ns	See Fig. 4
	t_{pd} – –	2.0		2.0	3.0	2.2		P_L = 50 Ω to –2 V
	t_{pd} + +	2.0		2.0	3.0	2.2		C_L <5 pF
	t_{pd} – +	2.0		2.0	3.0	2.2		$t_r = t_f$ = 2.2 ns (10 – 90%)
	t_{pd} + –	2.0		2.0	3.0	2.2		
t_f	Fall Time 10% – 90%	3.0		3.0	4.5	3.0	ns	
t_r	Rise Time 10% – 90%	3.0		3.0	4.5	3.0		

SWITCHING TIME TEST CIRCUIT AND WAVEFORM





L_1 and L_2 = equal length 50 Ω impedance lines

$R_L = R_T$ = 50 Ω Termination of Scope C

C_L = Jig and Stray Capacitance <5.0 pF

$t_r = t_f$ = 2.2 ns (10% - 90%)

Jig setup with no circuit under test.

$V_{CC} = V_{CC(AUX)}$ = +2.0 V

V_{EE} = –3.2 V

Logic levels for Fig. 5 is nominal values at 50 Ω fanout determined by indicated power supplies. These values chosen to permit use of scope 50 Ω termination to ground.

Decoupling 0.1 μF from GND to V_{EE}.

Fig. 4

APPLICATION

INTERCONNECTION RECOMMENDATIONS – All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

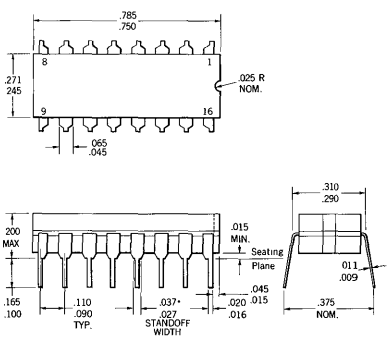
Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. Microstrip interconnections may be terminated by a resistor to a −2 volt supply. Alternately, a 2 resistor divider network may be used with R_1 = 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

The high impedance 95L00 devices may be wired using series type termination, but must have additional 510Ω resistors from each output to V_{EE} or terminate through the appropriate value resistor −2.00 volts. The high impedance inputs allow high fanouts, and slight (<3 ns) and open outputs allow wire-ORing to greater than 30 with degradation. Care must be taken to avoid glitches in the threshold region of the waveform occuring at certain combinations of line length and series resistor value.

A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY – The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

PHYSICAL DIMENSIONS
16 LEAD SSI DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
* The .037/.027 dimensions does not apply to the corner leads

9528

HIGH SPEED DUAL D FLIP-FLOP

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The 9528 is a high speed, temperature compensated ECμL dual D (data) flip-flop compatible with all other members of the 9500 series of ECμL circuits. The device is versatile and permits easy implementation of high speed counters, registers, and control circuits.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margins and speed remain relatively constant over a wide temperature range. Input and output two kilohm pulldown resistors eliminate the necessity for external termination of lines up to six or eight inches and permit unused inputs to be left open. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The device is packaged in the hermetic ceramic 16 pin dual in-line package and specified for operation over the temperature range 0°C to +75°C.

- **160 MHz OPERATION**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS — ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **MASTER-SLAVE CIRCUIT**
- **SEPARATE DIRECT SET AND CLEAR INPUTS**
- **BOTH COMMON AND SEPARATE CLOCK INPUTS**
- **WIRED-OR CAPABILITY ON OUTPUTS**
- **50 Ω LINE DRIVING CAPABILITY**
- **SINGLE —5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

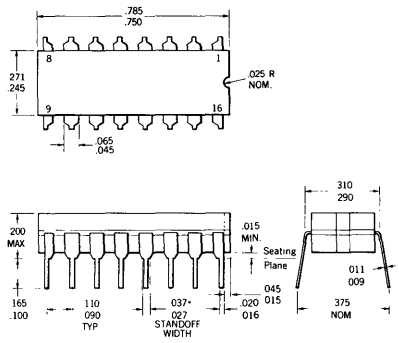
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6.0 Volts
Supply Voltage V_{EE} (Pulsed)	−8.0 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

ORDER INFORMATION

Specify U6B9528XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range for 9528 flip-flop.

PHYSICAL DIMENSIONS

16 Lead Dual In-Line



NOTES:

All dimensions in inches

Leads are intended for insertion in hole rows on .300" centers

They are purposely shipped with "positive" misalignment to facilitate insertion

Board-drilling dimensions should equal your practice for.0 20 inch diameter lead

Leads are tin plated kovar

Package weight is 2.0 grams

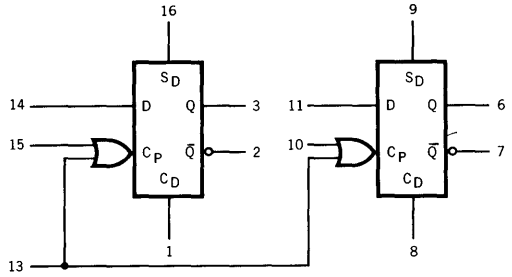
The .027/.037 dimensions does not apply to the corner leads

FUNCTIONAL DESCRIPTION — The 9528 Dual D (data) Flip-Flop uses the non-saturating, current switch-emitter follower circuit configuration to achieve high speed. In addition series gating and other current mode design techniques are incorporated to implement the circuits with minimum propagation delays and minimum power dissipation.

Each D Flip-Flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state making it insensitive to the D input and connects the slave to the master causing the new information to be reflected on the outputs. The following clock transition from HIGH to LOW again locks the slave and permits information to flow into the master. Logic races are avoided by offsetting the master and slave thresholds to avoid simultaneous switching when low speed edges are encountered in the system.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The outputs will only switch following a LOW to HIGH transition of the ORed clock (unless the direct set or clear inputs are activated). The ORed clock permits the use of one input as a clock pulse input and the other as an active low enable. If one clock input is held HIGH, clock pulses on the other input will not be seen by the flip-flop. To maintain synchronous operation, however, the clock input used as an enable should only be changed while the clock is HIGH.

Fig. 1 — LOGIC DIAGRAM



V_{CC} = GND (Pins 4 & 5)
V_{EE} = −5.20 V (Pin 12)

TRUTH TABLE

SYNCHRONOUS OPERATION

D TABLE	
D_n	$Q_n + 1$*
L	L
H	H
*S_D - C_D = Low	

ASYNCHRONOUS OPERATION

S_D - C_D TABLE			
C_D	S_D	Q	$\bar{Q}$
L	L	See D Table	See D Table
L	H	H	L
H	L	L	H
H	H	Not Allowed	

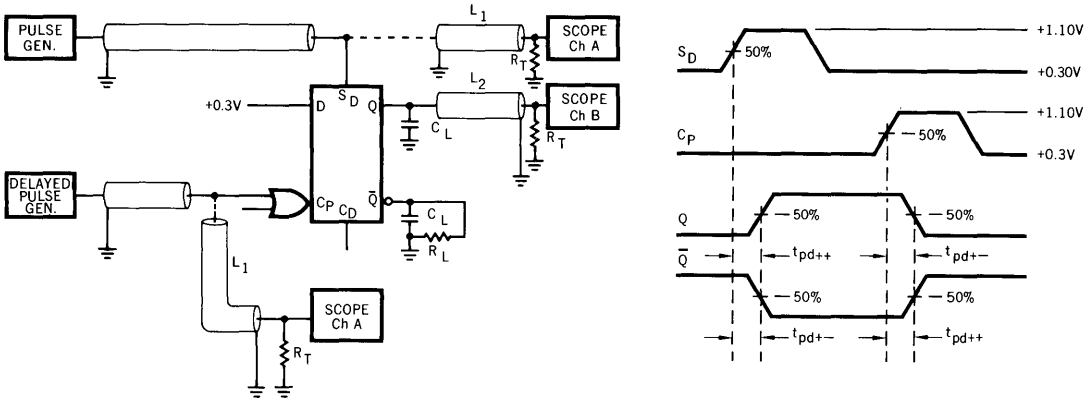
D.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{OH}	Output High Voltage	−905	−850	−795	−905	−850	−795	−895	−840	−785	mV	FO = 1 Gate
		−945	−890	−835	−945	−890	−835	−945	−890	−835	mV	FO = 5 Gates
		−980	−925	−870	−980	−925	−870	−980	−925	−870	mV	R_L = 50 Ω to −2.0 V
V_{OL}	Output Low Voltage	−1755	−1670	−1585	−1755	−1670	−1585	−1755	−1670	−1585	mV	FO = 1 Gate
		−1795	−1710	−1625	−1795	−1710	−1625	−1795	−1710	−1625	mV	FO = 5 Gates
		−1785	−1700	−1615	−1785	−1700	−1615	−1785	−1700	−1615	mV	R_L = 50 Ω to −2.0 V
V_{IHX}	Input High Threshold Voltage	−1140			−1140			−1140			mV	Guaranteed Input High
V_{ILX}	Input Low Threshold Voltage			−1450			−1450			−1450	mV	Guaranteed Input Low
$I_{IN(1)}$	Input Current at V_{IH}		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = 900 mV to each
	Common Clock Input		4.60	6.30		4.50	6.20		4.30	6.00		input sequentially
$I_{IN(0)}$	Input Current at V_{IL}		1.80	2.40		1.75	2.35		1.65	2.25	mA	V_{IL} = 1700 mV to each
	Common Clock Input		3.60	4.80		3.50	4.70		3.30	4.50		input sequentially
I_{PS}	Power Supply Current	46	62	84	51	64	85	52	66	90	mA	All inputs open

A.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C)

SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
I_T	Transient Input Current					2.5	3.5				mA	See Fig. 5
	Common Clock					3.5	4.5				mA	
t_{pd}	Clock Input											V_{CC} = 2.0 V
	t_{pd++}		3.6			3.6	4.8		3.6		ns	V_{EE} = −3.2 V
	t_{pd+-}		3.6			3.6	4.8		3.6		ns	See Fig. 2 & 3
	S_D & C_D Input											R_L = 50 Ω to Gnd
	t_{pd++}		3.6			3.6	4.8		3.6		ns	C_L < 5 pF
	t_{pd+-}		3.6			3.6	4.8		3.6		ns	$t_r = t_f$ = 2.5 ns
	Toggle Rate				110	160					MHz	See Fig. 4

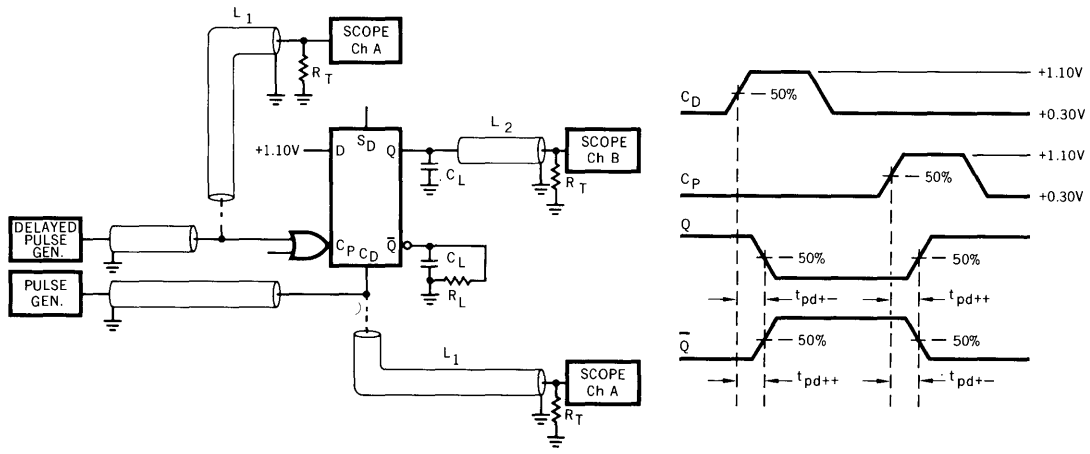
SWITCHING TIME TEST CIRCUITS AND WAVEFORMS



CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = Jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal $t_r = t_f$ = 2.5 ns (10% - 90%)
with no circuit under test

Fig. 2 — S_D ASYNCHRONOUS INPUT SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

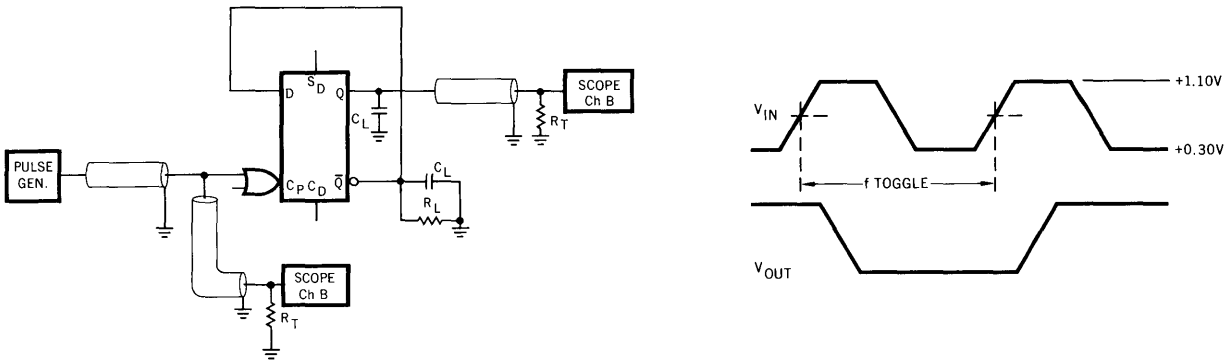


CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = Jig and stray capacitance < 5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal $t_r = t_f$ = 2.5 ns (10% - 90%)
with no circuit under test

Fig. 3 — C_D ASYNCHRONOUS INPUT SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

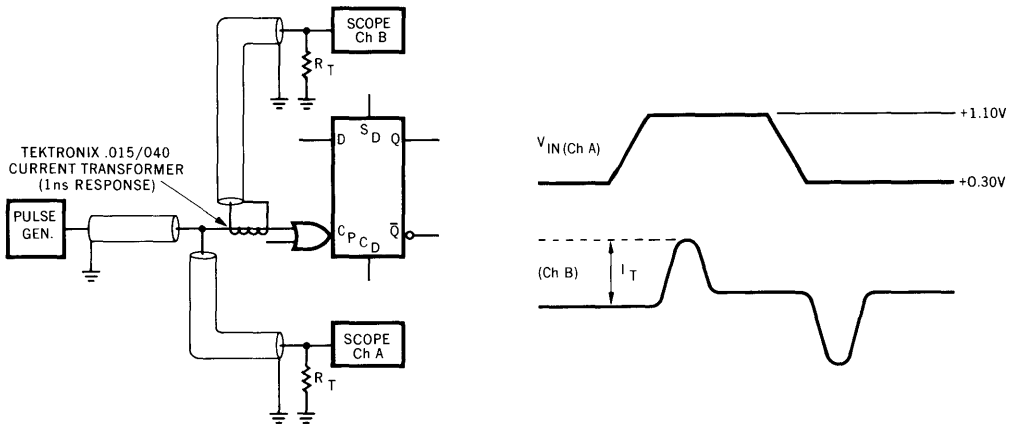
SWITCHING TIME TEST CIRCUITS AND WAVEFORMS (continued)



CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = Jig and stray capacitance < 5 pF
Pulse Gen. — EH 122 or equivalent

Fig. 4 — TOGGLE RATE TEST CIRCUIT AND WAVEFORMS



This test provides a measure of the average value of C_{IN}.

CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_T = 50 Ω (Scope input impedance)
Input signal $t_r = t_f$ = 2.5 ns (10% - 90%) with no circuit under test

Fig. 5 — TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS

9534

RESETTABLE QUAD "D" LATCH WITH I/O ENABLE

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The ECL 9534 quad D latch will store four bits of information simultaneously. Two common enable inputs and a common output enable allow maximum logic flexibility. A common Select input selects 'D' type or 'Set' type of operation. A common reset clears the device so that the 1's catching feature may be used when desired.

This element is designed as a storage buffer for high speed registers in arithmetic logic units and a data buffer in communication systems.

- **HIGH SPEED . . . 4.3 ns TYPICAL DATA DELAYS**
- **COMMON LATCH ENABLE**
- **COMMON MASTER RESET**
- **COMMON SELECT FOR 'D' OR 'SET'**
- **COMPLEX MULTIGATE CHIP REDUCES PACKAGE COUNT**
- **EASILY EXPANDED TO LARGE HIGH SPEED MEMORY**
- **WIRED OR CAPABILITY**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS – ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN**
- **50 Ω LINE DRIVE CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**

PIN NAMES

D_N	Data Inputs
Q_N	Data Output
S_1	Select, Data or 1's Catching
MR	Master Reset
$\overline{EO}$	Output Enable
$\overline{EI}$	Input Enable

ORDER INFORMATION – Specify U6B9534XXX for 16 pin Dual In-Line Package where XXX is 59X for 0°C to +75°C Temperature Range.

LOGIC SYMBOL

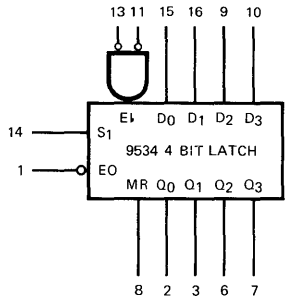


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

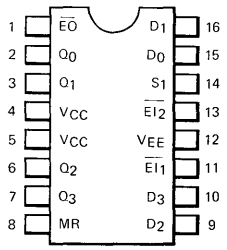


Fig. 2

LOGIC DIAGRAM (4 Each)

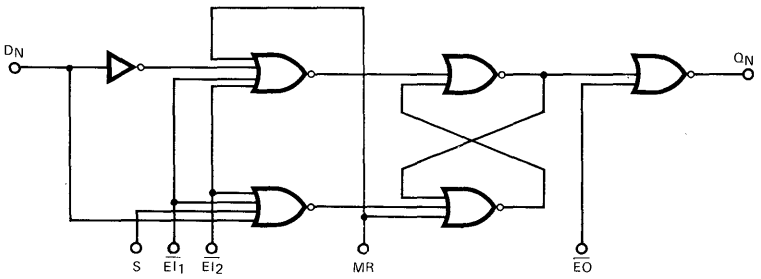


Fig. 3

FUNCTIONAL DESCRIPTION – Data can be entered into the latch whenever both input enable inputs ($\overline{EI}$) are low.

If either of the input enables ($\overline{EI}$) goes high the data present in the latch at that time is held and is no longer affected by the data input.

Data may be read out of the latches whenever the output enable ($\overline{E0}$) is low.

If the output enable goes high then the outputs are forced low, but the data is undisturbed. This function allows many 9534 latches to be wire ORed together and read out when selected. Information may be fed into the latch and stored while the outputs are held low.

If the S_1 input is raised the 9534 becomes a quad set-reset latch with separate sets (D_N) and a common reset (MR). In this mode (S_1 = high) if both input enables ($\overline{EI}$) are low the latches are ones catching. Again if either input enable ($\overline{EI}$) goes high the data present in the latch is held and is no longer affected by the data input.

If at any time the master rest (MR) goes high all latches are forced to "0". If the output enable goes high, only the outputs will be forced to "0". The data remains undisturbed.

D.C. ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (T_A = 0°C to 75°C, V_{EE} = –5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage	–905 –945 –980	–850 –890 –925	–785 –835 –870	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	V_{IN} = –0.900 V (D operation)
V_{OL}	Output Low Voltage	–1755 –1795 –1785	–1670 –1710 –1700	–1585 –1625 –1615	mV	FO = 1 Gate FO = 5 Gates 50Ω to –2.0 V	V_{IN} = –1.700 V (D operation)
V_{OHC}	Output High Corner Point (See Fig. 4)	–915 –955 –990			mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	$V_{IN} = V_{IHX}$ (D Input) $V_{IN} = V_{ILX}$ (EO Input)
V_{OLC}	Output Low Corner Point (See Fig. 4)			–1575 –1615 –1605	mV	FO = 1 Gate FO = 5 Gates 50 Ω to –2.0 V	$V_{IN} = V_{ILX}$ (D Input) $V_{IN} = V_{IHX}$ (EO Input)
V_{IHX}	Input High Level	–1140			mV	Guaranteed Input High Threshold Voltage	
V_{ILX}	Input Low Level			–1450	mV	Guaranteed Input Low Threshold Voltage	
$I_{IN(H)}$	Input Current at V_{IH}		2.25	3.15	mA	V_{IN} = –900 mV to Each Input Sequentially	
$I_{IN(L)}$	Input Current at V_{IL}		1.75	2.40	mA	V_{IN} = –1700 mV to Each Input Sequentially	
I_{PS}	Power Supply Current		80		mA	V_{EE} = –5.2 V, All Inputs Open	

NOISE MARGIN SPECIFICATION POINTS

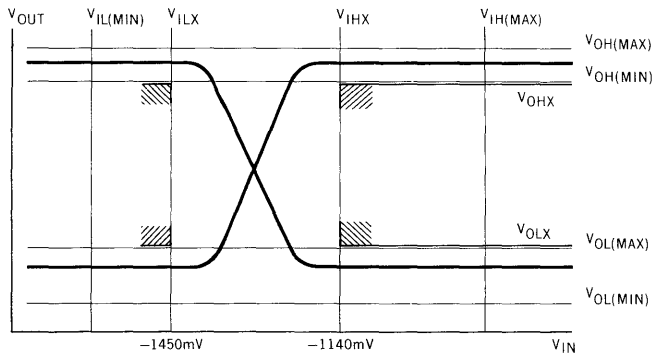


Fig. 4

Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

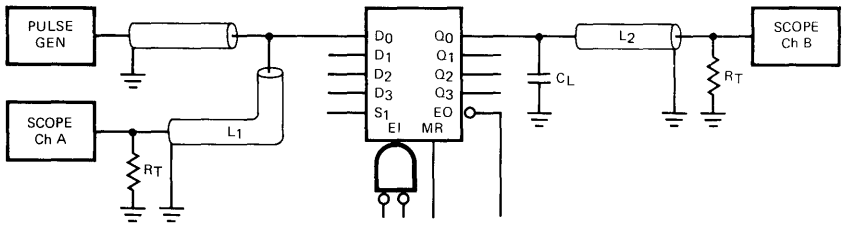
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	–6 Volts
Supply Voltage V_{EE} (Pulsed)	–8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

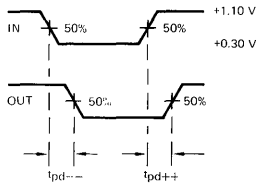
A.C. ELECTRICAL CHARACTERISTICS (V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN	0°C TYP	0°C MAX	25°C MIN	25°C TYP	25°C MAX	75°C MIN	75°C TYP	75°C MAX	UNITS	CONDITIONS
	Propagation Delay											
	DATA INPUT											
	t_{pd--}		4.3			4.3			4.6		ns	See Fig. 5
	t_{pd++}		4.3			4.3			4.6		ns	
	OUTPUT ENABLE											
	t_{pd-+}		3.4			3.4			3.6		ns	See Fig. 6
	t_{pd++}		3.4			3.4			3.6		ns	
t_{pd}	MR INPUT											
	t_{pd-+}		5.6			5.6			6.0		ns	See Fig. 7
	t_{pd+-}		5.6			5.6			6.0		ns	
	EI INPUT											
	t_{pd-+}		5.6			5.6			6.0		ns	See Fig. 8
	SELECT INPUT											
	t_{pd-+}		5.6			5.6			6.0		ns	See Fig. 9
	Transient Input Current					2.5	3.5				mA	
I_T	Master Reset					5.0	6.0				mA	See Fig. 10
	Output Enable					3.5	4.5				mA	

SWITCHING TIME CIRCUITS AND WAVEFORMS

DATA TO OUTPUT

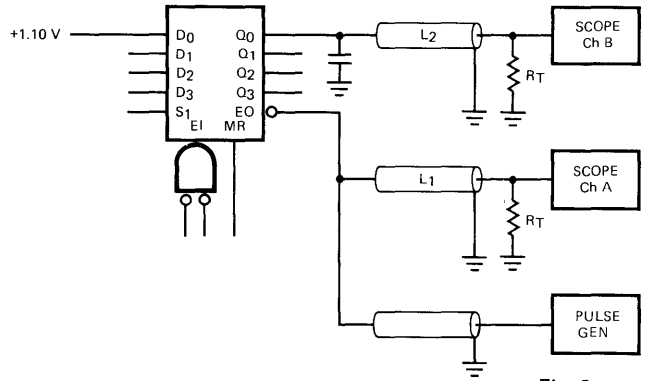


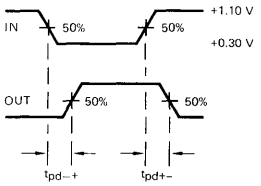


CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = −3.2 V
- R_L = 50 Ω = R_T (Scope input impedance)
- C_L = jig and stray capacitance < 5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

Fig. 5

OUTPUT ENABLE TO OUTPUT





CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = −3.2 V
- R_L = 50 Ω = R_T (Scope input impedance)
- C_L = jig and stray capacitance < 5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

Fig. 6

SWITCHING TIME CIRCUITS AND WAVEFORMS (Cont'd)

M.R. TO OUTPUT

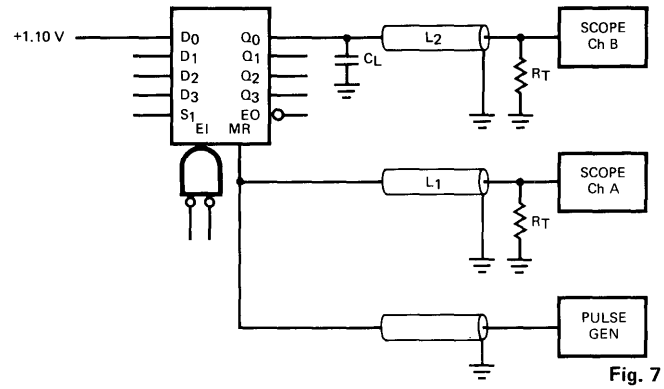
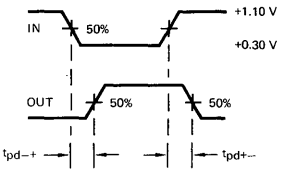


Fig. 7



CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = −3.2 V
- R_L = 50 Ω = R_T (Scope input impedance)
- C_L = jig and stray capacitance <5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

INPUT ENABLE TO OUTPUT

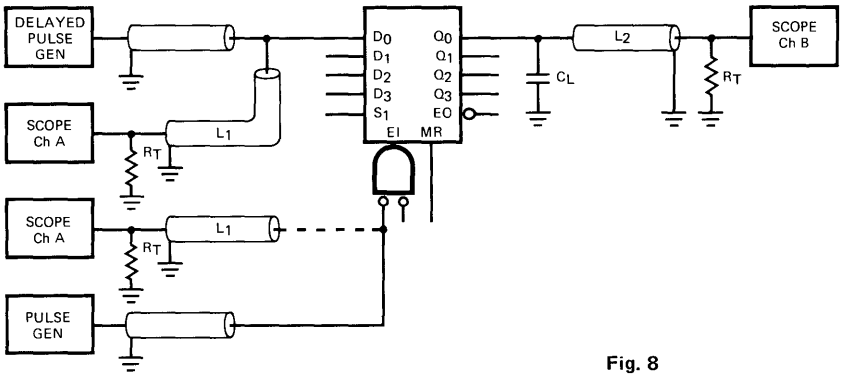
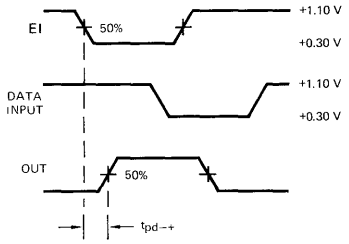


Fig. 8



CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = −3.2 V
- R_L = 50 Ω = R_T (Scope input impedance)
- C_L = jig and stray capacitance <5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

SELECT TO OUTPUT

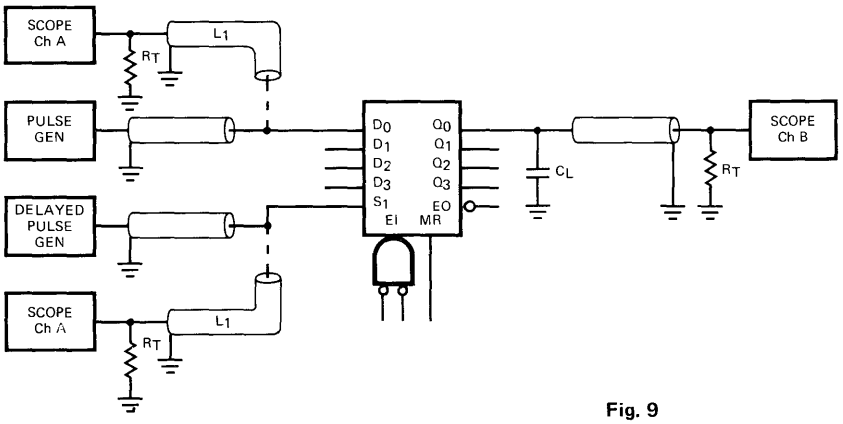
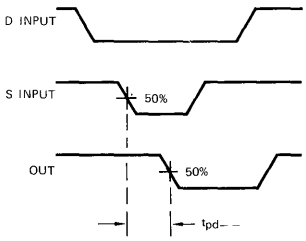


Fig. 9



CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = −3.2 V
- R_L = 50 Ω = R_T (Scope input impedance)
- C_L = jig and stray capacitance <5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

TRANSIENT INPUT CURRENT

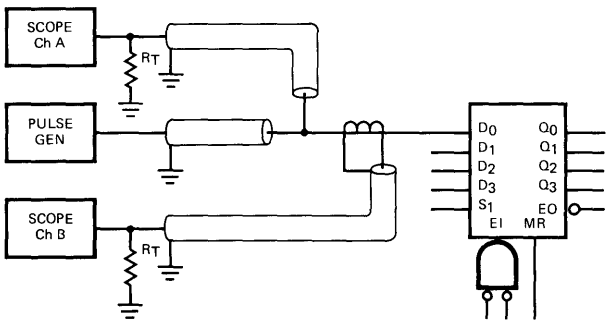
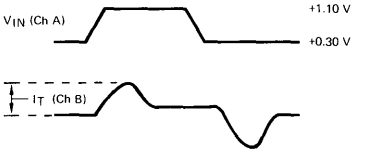


Fig. 10



This test provides a measure of the average value of C_{IN}

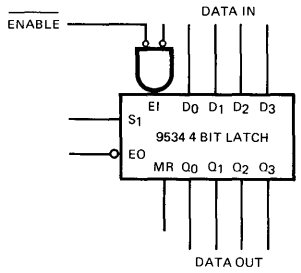
CONDITIONS
- V_{CC} = +2.0 V
- V_{EE} = −3.2 V
- R_T = 50 Ω (Scope input impedance)
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

APPLICATIONS – The 9534 quad latch is designed for all register applications encountered in high speed digital systems.

The 9534 has two modes of operation: as a 4-bit "D" type latch (Figure 11) or as a 4-bit Set-Reset type latch (Figure 12). The S (set) input determines which of these two modes the device operates in: S = "LOW" for "D" operation, S = "HIGH" for "S–R" operation.

An output enable (EO) is provided in addition to the input enables (EI). This permits both multiplexing of outputs (Figure 13) and demultiplexing of inputs (Figure 14). The Multiport Register in Figure 15 makes use of these features.

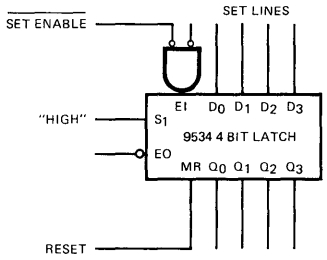
4 BIT STORAGE LATCH



The figure illustrates the use of the 9534 as a D type storage latch. Data is stored in the latch when the enable line is high.

Fig. 11

QUAD SET-RESET LATCH



This figure illustrates the use of the 9534 as a quad set-reset latch. If while the enable is low, a "HIGH" appears at an input (D_N) the latch sets, and stays set even if the input returns to a "LOW". A "HIGH" on the master reset removes all "HIGH's" from the latch.

Fig. 12

REGISTER MULTIPLEXING

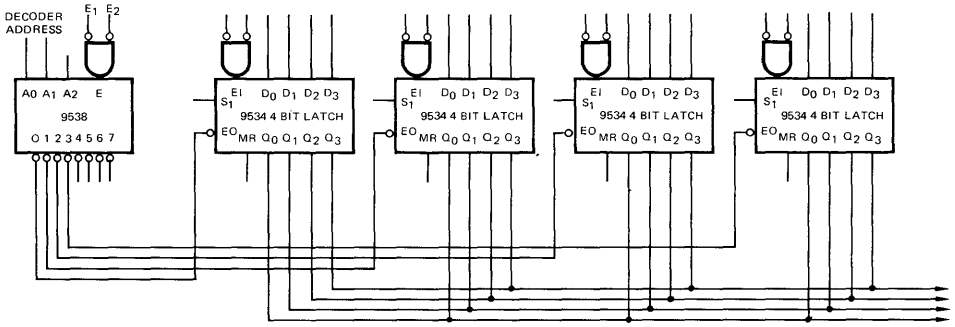


Fig. 13

REGISTER DEMULTIPLEXING

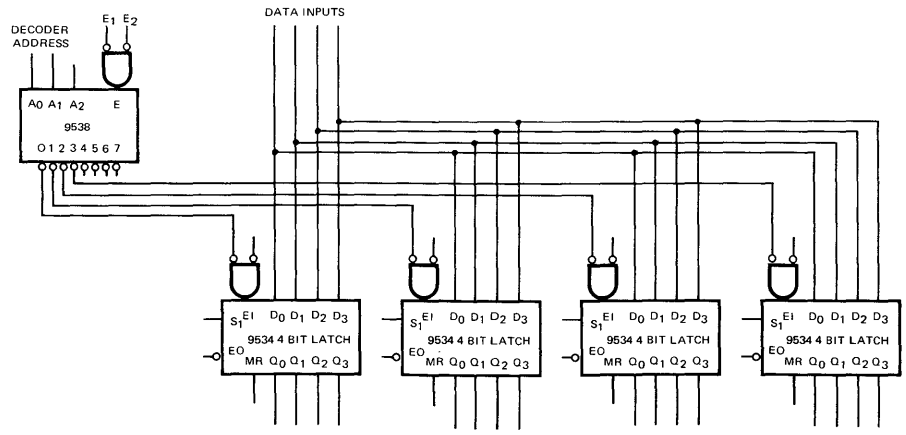
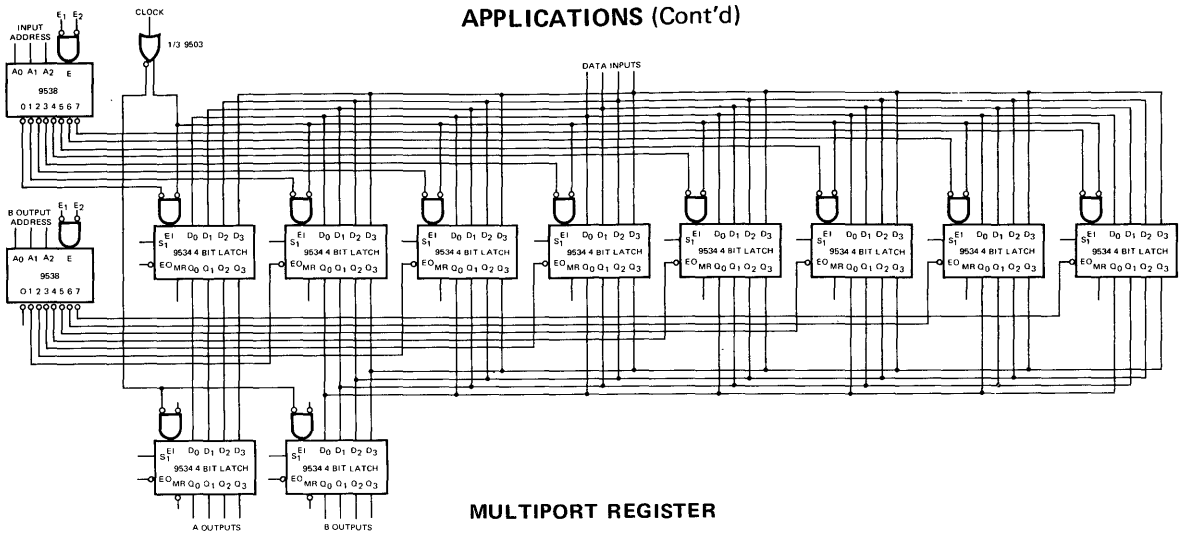


Fig. 14

APPLICATIONS (Cont'd)



MULTIPORT REGISTER

9534's may be used to form a multiport register for use in conjunction with an arithmetic unit. It is usually desirable for a multiport register to have two data outputs to simultaneously provide the two operands, A and B, and a data input for accepting the result of the operation. One of many possible variations is shown above.

The register uses eight master latches and two slave latches to provide dual-rank master-slave operation with the outputs changing following the "LOW" to "HIGH" transition of the clock. This fits nicely into a fully synchronous system where the address inputs come from sources also changing on the rising clock edge. The master-slave operation eliminates race conditions otherwise present when writing into and reading from the same location.

The multiport register shown allows the input (the result of the operation) to be read into any one of the eight locations. The A data output always comes from location 000 while the B data output may come from any of the other seven locations as selected by the 9538 decoder.

The system may easily be expanded to handle longer word lengths and a greater number of words by the addition of more 9534's and 9538's as well as 9581 multiplexers for additional output multiplexing. **Fig. 15**

INTERCONNECTION RECOMMENDATIONS

All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a −2 volt supply. Alternately, a 2 resistor divider network may be used with R_1 = 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

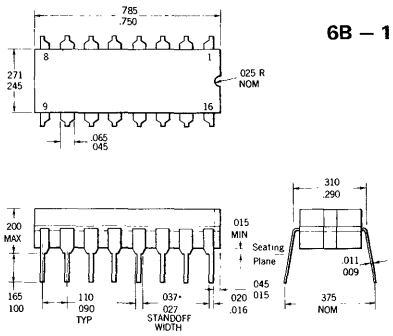
A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 Ω coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 Ω coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential

PHYSICAL DIMENSIONS

6B – 16 LEAD SSI DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

9538

ONE OF EIGHT DECODER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 9538 is a high speed temperature compensated ECμL one of eight decoder compatible with all other members of the 9500 series of ECμL circuits. It provides in one package the ability to activate any one of eight lines by the binary address of three input lines. In addition this device may be used as a demultiplexer by connecting data to the enable inputs.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margins and speed remain relatively constant over a wide temperature range. Input and output two kilohm pulldown resistors eliminate the necessity for external termination of lines up to six to eight inches and permit unused inputs to be left open. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The device is packaged in the hermetic ceramic 16 pin dual in-line package and specified for operation over the temperature range 0°C to + 75°C.

- **HIGH SPEED 4.0 ns FROM SELECT INPUT TO OUTPUT LINE**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS–ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **ENABLE INPUTS**
- **WIRED-OR CAPABILITY ON OUTPUT**
- **50 Ω LINE DRIVING CAPABILITY**
- **SINGLE -5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

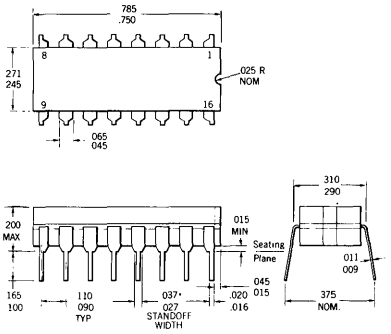
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	-65°C to + 150°C
Junction Temperature	+ 150°C
Supply Voltage V_{EE} (Continuous)	-6 Volts
Supply Voltage V_{EE} (Pulsed)	-8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

ORDER INFORMATION

Specify U6B9538XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to + 75°C temperature range.

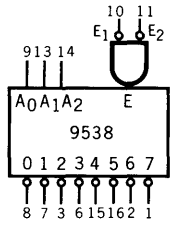
PHYSICAL DIMENSIONS
16 LEAD DUAL IN-LINE



Notes:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
The .037/.027 dimensions does not apply to the corner leads.

Fig. 1

LOGIC SYMBOL



V_{CC} = GND (Pins 4 & 5)
V_{EE} = Pin 12

Fig. 2

FUNCTIONAL DESCRIPTION

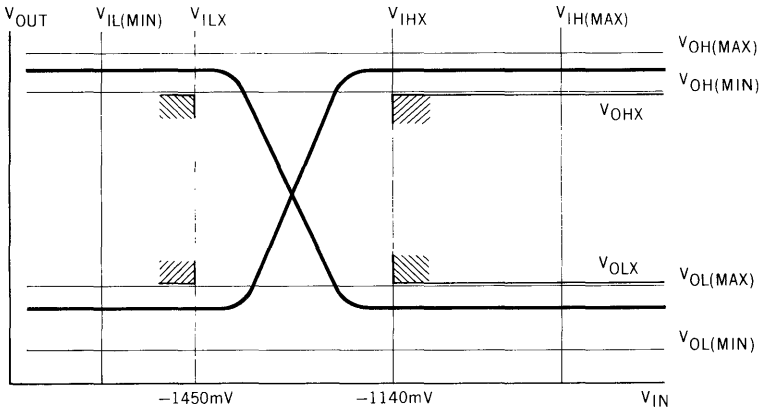
The 9538 decoder accepts three binary address inputs and under control of the enables, activates one of the eight active LOW outputs. Both of the active LOW enable input lines must be LOW to enable the outputs. In other words, if either of the enable inputs is HIGH all eight outputs remain HIGH. A truth table for the decoder is given in Figure 2.

The 9538 decoder may be used as a demultiplexer by connecting a data source to one of the enable inputs. The other enable input will function as a data enable line while inputs A_0, A_1 and A_2 determine which of the eight output lines the data is fed to. The data will not be inverted through the demultiplexer since both the input and the outputs are active low. The delay through the demultiplexer from either enable input to an output is only two gate delays.

TRUTH TABLE

INPUTS					OUTPUTS							
A_0	A_1	A_2	E_1	E_2	0	1	2	3	4	5	6	7
L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	L
X	X	X	H	L	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H

Fig. 3—NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

D.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to + 75°C, V_{CC} = Gnd, V_{EE} = -5.2 V)

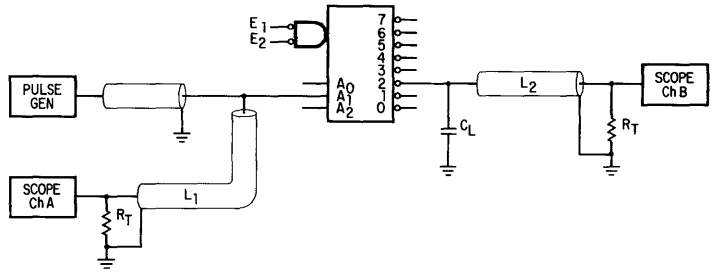
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C TYP.	0°C MAX.	+ 25°C MIN.	+ 25°C TYP.	+ 25°C MAX.	+ 75°C MIN.	+ 75°C TYP.	+ 75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	-915	-850	-785	-915	-850	-785	-905	-840	-775	mV	FO = 1 Gate
		-955	-880	-805	-955	-880	-805	-955	-880	-805	mV	FO = 5 Gates
		-990	-915	-840	-990	-915	-840	-990	-915	-840	mV	R_L = 50 Ω to -2.0 V
V_{OL}	Output Low Voltage	-1755	-1670	-1585	-1755	-1670	-1585	-1755	-1670	-1585	mV	FO = 1 Gate
		-1795	-1710	-1625	-1795	-1710	-1625	-1795	-1710	-1625	mV	FO = 5 Gates
		-1785	-1700	-1615	-1785	-1700	-1615	-1785	-1700	-1615	mV	R_L = 50 Ω to -2.0 V
V_{OHX}	Output High Voltage at V_{IN} (Threshold) V_{IHX} or V_{ILX} Applied to each. Select Line Sequentially.	-925			-925			-915			mV	FO = 1 Gate
		-965			-965			-965			mV	FO = 5 Gates
		-1000			-1000			-1000			mV	R_L = 50 Ω to -2.0 V See Fig. 3
V_{OLX}	Output Low Voltage at V_{IN} (Threshold) V_{IHX} or V_{ILX} Applied to each. Select Line Sequentially.			-1575			-1575			-1575	mV	FO = 1 Gate
				-1615			-1615			-1615	mV	FO = 5 Gates
				-1605			-1605			-1605	mV	R_L = 50 Ω to -2.0 V See Fig. 3
$I_{IN(1)}$	Input Current at V_{IH}		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = -900 mV to each Input Sequentially
$I_{IN(0)}$	Input Current at V_{IL}		1.80	2.40		1.75	2.35		1.65	2.25	mV	V_{IL} = -1700 mV to each Input Sequentially
I_{PS}	Power Supply Current		50		42	53	71		57		mA	All Inputs Open

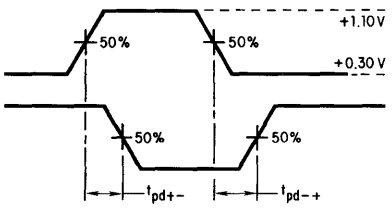
A.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to + 75°C)

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C TYP.	75°C MAX.	UNIT	CONDITIONS
t_{pd}	Propagation Delay									See Fig. 4 & 5
	Select Lines									R_L = 50 Ω to
	A_1	3.0		3.0	4.0		3.0		ns	Gnd
	A_0 & A_2	4.0		4.0	5.3		4.0		ns	$C_L \leq$ 5.0 pF
	Enable Lines	5.0		5.0	6.7		5.0		ns	$t_r = t_f$ = 2.5 ns
I_T	Transient Input Current			2.5	3.5				mA	See Fig. 6

SWITCHING TIME CIRCUITS AND WAVEFORMS

Fig. 4—SELECT LINES TO OUTPUT

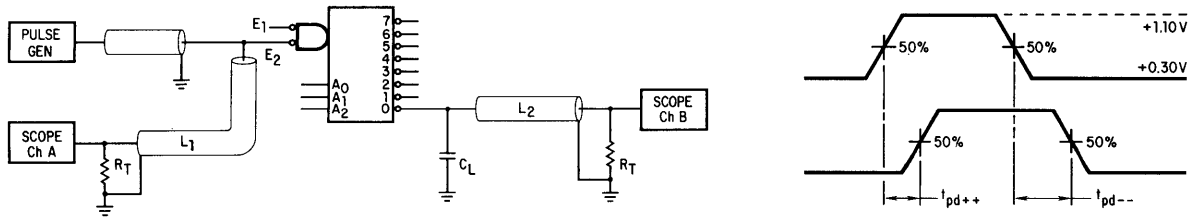




CONDITIONS
- V_{CC} = + 2.0 V
- V_{EE} = -3.2 V
- R_L = 50 Ω = R_T (Scope input impedance)
- C_L = jig and stray capacitance < 5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal $t_r = t_f$ = 2.5 ns (10% - 90%)
- With no circuit under test

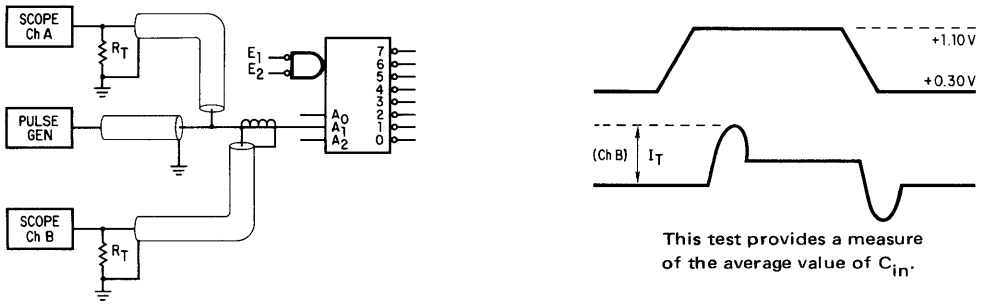
SWITCHING TIME CIRCUITS AND WAVEFORMS (CONT'D)

Fig. 5—ENABLE LINE TO OUTPUT



CONDITIONS
- V_{CC} = + 2.0 V
- V_{EE} = -3.2V
- R_L = 50 Ω = R_r (Scope input impedance)
- C_L = jig and stray capacitance < 5 pF
- L_1 = L_2 equal 50 Ω impedance lines
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

Fig. 6—TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS



This test provides a measure of the average value of C_{in}.

CONDITIONS
- V_{CC} = + 2.0 V
- V_{EE} = -3.2 V
- R_r = 50 Ω (Scope input impedance)
- Input signal t_r = t_f = 2.5 ns (10% - 90%)
- With no circuit under test

9581

EIGHT INPUT MULTIPLEXER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The 9581 is a high speed, temperature compensated ECμL eight input multiplexer compatible with all other members of the 9500 series of ECμL circuits. It provides in one package the ability to select one bit of data from up to eight sources. In addition, the 9581 can be used as a universal function generator to generate any logic function of four variables.

All 9500 series elements incorporate a unique temperature compensation network. This insures that significant parameters such as logic levels, noise margins and speed remain relatively constant over a wide temperature range. Input and output two kilohm pulldown resistors eliminate the necessity for external termination of lines up to six to eight inches and permit unused inputs to be left open. Package pin locations are chosen to reduce internal noise generation and crosstalk.

The device is packaged in the hermetic ceramic 16 pin dual in-line package and specified for operation over the temperature range 0°C to +75°C.

- **HIGH SPEED . . . 3.0 ns FROM DATA INPUT TO OUTPUT**
- **SEPARATE CURRENT SWITCH AND EMITTER FOLLOWER V_{CC} PINS — ELIMINATES NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULLDOWN RESISTORS**
- **ENABLE INPUTS**
- **WIRED-OR CAPABILITY ON OUTPUT**
- **50 Ω LINE DRIVING CAPABILITY**
- **SINGLE —5.2 V POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DUAL IN-LINE PACKAGE**

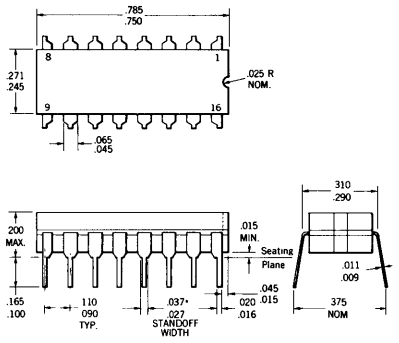
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

ORDER INFORMATION

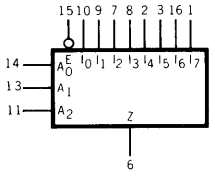
Specify U6B9581XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range.

PHYSICAL DIMENSIONS
16 LEAD DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
The .037/.027 dimensions does not apply to the corner leads

LOGIC SYMBOL



V_{CC} = GND (Pins 4 & 5)
V_{EE} = −5.2 V (Pin 12)

Fig. 1

FUNCTIONAL DESCRIPTION

The 9581 eight input multiplexer uses the non-saturating, current switch-emitter follower circuit configuration to achieve high speed. In addition series gating and other current mode design techniques are incorporated to implement the circuits with minimum propagation delays and minimum power dissipation. Data encounters only one gate delay from one of the eight inputs to the output.

The 9581 is fundamentally a high speed semiconductor implementation of a single-pole eight-position switch. Three address lines select one out of the eight data inputs and feed this input to the output (Z). An active low enable forces the output LOW if held HIGH. The logic function provided at the output is:

$$Z = E\bullet(I_0\bullet\overline{A_0}\bullet\overline{A_1}\bullet\overline{A_2} + I_1\bullet A_0\bullet\overline{A_1}\bullet\overline{A_2} + I_2\bullet\overline{A_0}\bullet A_1\bullet\overline{A_2} + I_3\bullet A_0\bullet A_1\bullet\overline{A_2} + I_4\bullet\overline{A_0}\bullet\overline{A_1}\bullet A_2 + I_5\bullet A_0\bullet\overline{A_1}\bullet A_2 + I_6\bullet\overline{A_0}\bullet A_1\bullet A_2 + I_7\bullet A_0\bullet A_1\bullet A_2).$$

(Since the enable is an active low input, the E in the equation implies pin 15 must be LOW to activate Z).

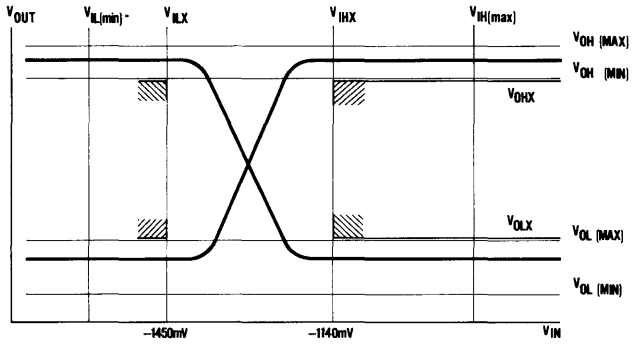
The 9581 provides the ability to select from or sequence eight data sources. It may therefore be used as a parallel to serial converter by sequentially advancing through the input address combinations.

The device may also be used as a universal logic element capable of generating any function of four variables by proper manipulation of the inputs. The wire-ORable outputs and the input enable permit easy expansion of several 9581's to form multiplexers with more than eight inputs.

Fig. 2 — TRUTH TABLE

INPUTS											OUTPUT
A_0	A_1	A_2	$\overline{E}$	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
H	L	L	L	X	L	X	X	X	X	X	X	L
H	L	L	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
H	H	L	L	X	X	X	L	X	X	X	X	L
H	H	L	L	X	X	X	H	X	X	X	X	H
L	L	H	L	X	X	X	X	L	X	X	X	L
L	L	H	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	L

Fig. 3 — NOISE MARGIN SPECIFICATION POINTS (DATA LINES)



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

D.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = Gnd, V_{EE} = −5.2 V)

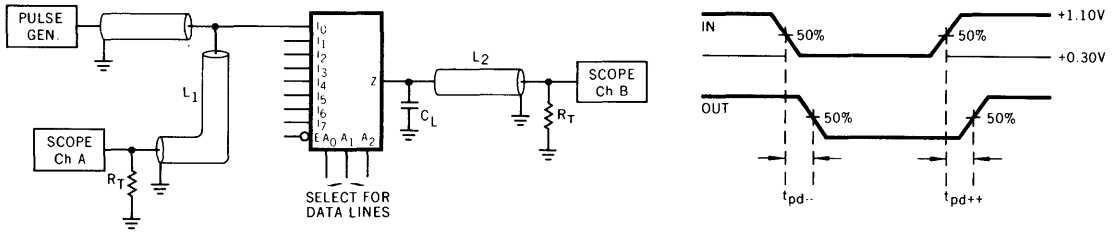
SYMBOL	CHARACTERISTIC	LIMITS									UNITS	CONDITIONS
		0°C			+25°C			+75°C				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
V_{OH}	Output High Voltage	−905	−850	−795	−905	−850	−795	−895	−840	−785	mV	FO = 1 Gate
		−945	−890	−835	−945	−890	−835	−945	−890	−835	mV	FO = 5 Gates
		−980	−925	−870	−980	−925	−870	−980	−925	−870	mV	R_L = 50 Ω to −2.0 V
V_{OL}	Output Low Voltage	−1755	−1670	−1585	−1755	−1670	−1585	−1755	−1670	−1585	mV	FO = 1 Gate
		−1795	−1710	−1625	−1795	−1710	−1625	−1795	−1710	−1625	mV	FO = 5 Gates
		−1785	−1700	−1615	−1785	−1700	−1615	−1785	−1700	−1615	mV	R_L = 50 Ω to −2.0 V
V_{OHX}	Data Lines Output High Voltage at V_{in} = −1140 mV	−915			−915			−905			mV	FO = 1 Gate
		−955			−955			−955			mV	FO = 5 Gates
		−990			−990			−990			mV	R_L = 50 Ω to −2.0 V See Fig. 3
V_{OLX}	Data Lines Output Low Voltage at V_{in} = −1450 mV			−1575			−1575			−1575	mV	FO = 1 Gate
				−1615			−1615			−1615	mV	FO = 5 Gates
				−1605			−1605			−1605	mV	R_L = 50 Ω to −2.0 V See Fig. 3
V_{IHX}	Select Lines Input High Threshold Voltage	−1140			−1140			−1140			mV	Guaranteed Input High Voltage
V_{ILX}	Select Lines Input Low Voltage			−1450			−1450			−1450	mV	Guaranteed Input Low Voltage
$I_{IN(1)}$	Input Current at V_{IH}		2.30	3.15		2.25	3.10		2.15	3.00	mA	V_{IH} = −900 mV to each Input Sequentially
$I_{IN(0)}$	Input Current at V_{IL}		1.80	2.40		1.75	2.35		1.65	2.25	mA	V_{IL} = −1700 mV to each Input Sequentially
I_{PS}	Power Supply Current		48		40	50	67		55		mA	All Inputs Open

A.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C)

SYMBOL	CHARACTERISTIC	LIMITS							UNIT	CONDITIONS
		0°C	25°C			75°C				
		TYP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{pd}	Propagation Delay									See Fig. 4, 5 & 6
	Data Lines	3.2		3.2	4.3		3.2		ns	R_L = 50 Ω to Gnd
	Select Lines	5.5		5.5	7.5		5.5		ns	C_L < 5.0 pF
	Enable Lines	3.5		3.5	4.8		3.5		ns	$t_r = t_f$ = 2.5 ns
I_T	Transient Input Current			2.5	3.5				mA	See Fig. 7

SWITCHING TIME CIRCUITS AND WAVEFORMS

Fig. 4 — DATA LINES TO OUTPUT

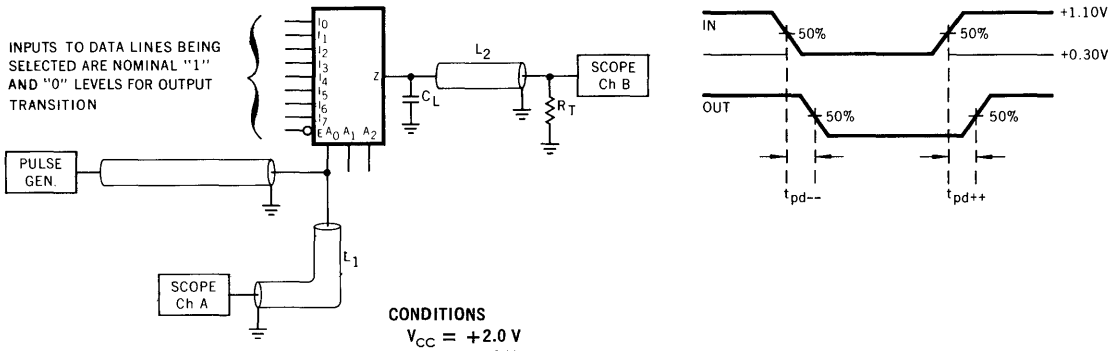


CONDITIONS

V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance <5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal $t_r = t_f$ = 2.5 ns (10% - 90%)
With no circuit under test

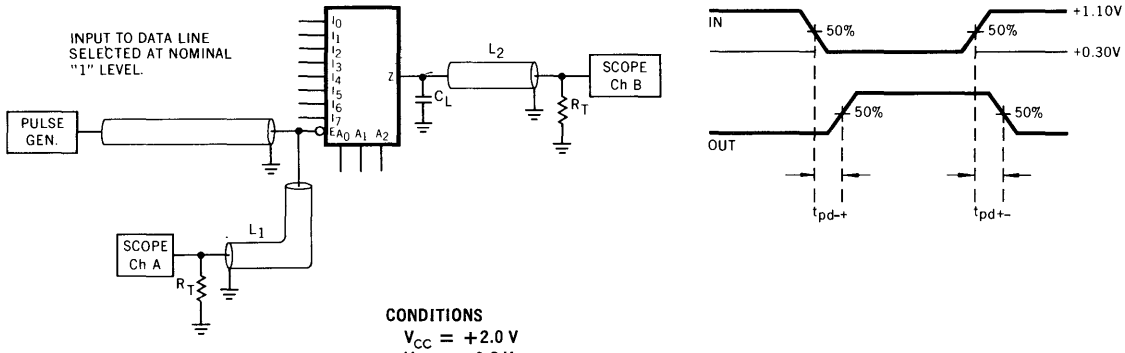
SWITCHING TIME CIRCUITS AND WAVEFORMS (CONT'D)

Fig. 5 — SELECT LINES TO OUTPUT



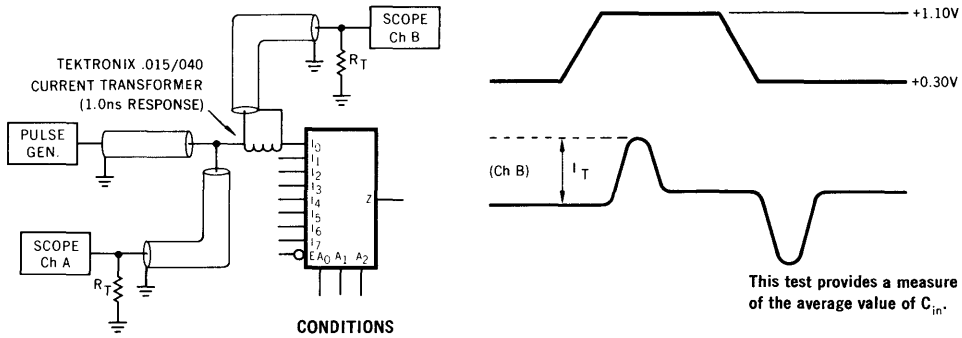
CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance <5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

Fig. 6 — ENABLE TO OUTPUT



CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_L = 50 Ω = R_T (Scope input impedance)
C_L = jig and stray capacitance <5 pF
L_1 = L_2 equal 50 Ω impedance lines
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

Fig. 7 — TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS



This test provides a measure of the average value of C_{in}.

CONDITIONS
V_{CC} = +2.0 V
V_{EE} = −3.2 V
R_T = 50 Ω (Scope input impedance)
Input signal t_r = t_f = 2.5 ns (10% - 90%)
With no circuit under test

9582

MULTI-FUNCTION LINE RECEIVER/AMPLIFIER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION – The 9582 is 3 differential input amplifiers. Both the true and compliment outputs are temperature compensated to be compatible with other ECL 9500 products. With appropriate connection of the base pins the device will function as a differential line receiver; Schmitt trigger; high speed comparator; broad band video, I.F. or R.F. amplifier; or oscillator. V_{ref} is made available to allow use of this device as a high input impedance buffer gate.

FEATURES:

- **DIFFERENTIAL INPUT**
- **TRUE AND COMPLIMENT OUTPUT**
- **HIGH INPUT IMPEDANCE**
- **HIGH SPEED – 2.5 ns**
- **REFERENCE VOLTAGE AVAILABLE FOR GATE OR LINEAR OPERATION**
- **PACKAGE GAIN OVER 50 dB FOR LINE RECEIVER, VIDEO OR RF APPLICATION.**

PIN NAMES

A_N = Positive (Non-Inverting) Input of Amplifier N
$\overline{A}_N$ = Negative (Inverting) Input of Amplifier N
Q_N = True (Non-Inverting) Output of Amplifier N
$\overline{Q}_N$ = Compliment (Inverting) Output of Amplifier N
V_R = Reference Voltage

ORDER INFORMATION – Specify U6B9582XXX for 16 pin Dual In-Line Package, where XXX is 59X for the 0°C to 75°C temperature range.

LOGIC SYMBOL

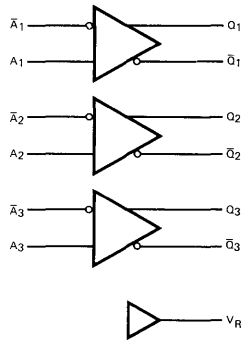


Fig. 1

CONNECTION DIAGRAM
DIP (TOP VIEW)

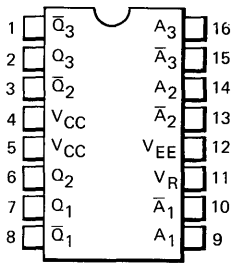
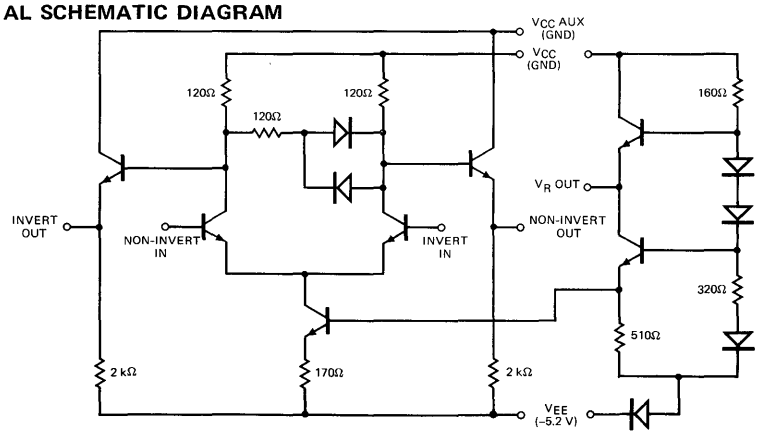


Fig. 2

PARTIAL SCHEMATIC DIAGRAM



For maximum Bandwidth, an additional R_L to V_{EE} of 220 ohms on each output will permit a bandwidth of >80 MHz at 3 dB.

Unused inputs must be grounded.

Fig. 3

FUNCTIONAL DESCRIPTION – The 9582 consists of three differential amplifiers with emitter-follower outputs and a bias (V_R) driver. This device is designed to be used as a line receiver in applications requiring a medium gain, high band-width limiting differential amplifier.

The ECL 9582 Triple line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 4. Any 9500 gate with differential outputs may be used to drive the twisted pair line. The line is terminated in its characteristic impedance (around 125 ohms). A voltage divider is formed between the high-level gate output, the terminating resistor, and the pull-down resistor on the low-level gate output. The equivalent DC circuit is shown in Figure 5. The voltage swing across the terminating resistor (R_T) is typically 260 mV. Any input voltage swing in excess of 160 mV ensure the output levels due to the voltage gain of the 9582. The output of the line receiver is similar to a standard ECL 9500 gate. For worst-case pull-down resistors in the driving gate (2.0k ohms ±20%) and a V_{OH} min, the differential drop across an R_T of 100 ohms is ±185 mV.

Very long lines may be used with excellent results. The only restriction on line length (other than common mode noise) is series line resistance. The nominal voltage drop across R_T is actually shared with the series resistance of the twisted pair line. The resistance of No. 22 AWG wire averages about .016 ohms per foot, while No. 24 AWG wire averages about .026 ohms per foot. For very long lines, an additional voltage drop across R_T is easily obtained by paralleling additional pull-down resistors with those internal to the driver gate. For example, by paralleling a 2.0k ohm resistor with each output, the voltage drop across R_T is effectively doubled.

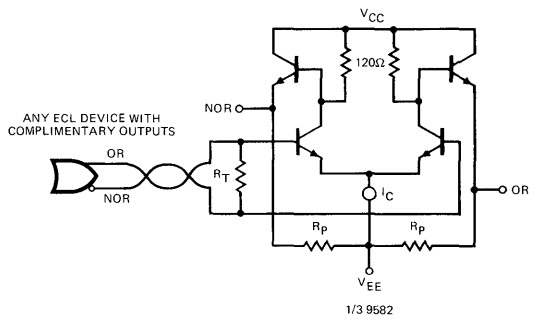
Extensive data have shown that a positive transient of 1.0 V or a negative, transient of 1.5 V may be introduced on the twisted pair line (i.e., between driver and receiver system grounds) before noise can propagate through another ECL device tied to the line receiver output. This method of data transmission is useful at frequencies to 100 MHz.

A twisted pair transmission line is recommended for clock distribution in high-speed systems since distribution skew time may be balanced out by adjusting line lengths. Propagation delay times are approximately 1.0 ns per eight inches of line.

In system design it is often convenient to organize information transfer with a data bus or "party-line" approach. In this application, one of many sources may "talk" to the common data line and multiple receivers may "listen". Figure 6 illustrates such a data bus utilizing ECL 9500 gates as drivers and ECL 9582 as line receivers. Note that the line is unbalanced, but this will in turn allow all drivers to be ORed together. Bandwidth of data distribution is excellent. The technique may be used to 100 MHz over the entire industrial temperature range. Noise immunity is also good due to the low impedance methods of transmission and the common mode rejection of the line receiver. The following results were obtained during an evaluation of the data bus shown in Figure 6 under the following conditions:

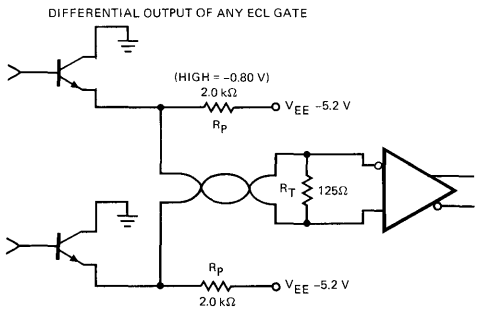
Number of driver gates: 10
Number of receivers: 10
Line length: 10 feet
Maximum operating frequency: 100 MHz
Total terminating resistance: 60 ohms, i.e., 120Ω at each end.
Differential power supply voltage from transmitter gate to receiver gate: ±5.0%

The Triple line receiver can also be used in many linear applications. The minimum differential voltage gain is 6 volt/volt, with a 3.0 dB bandwidth of typically 70 MHz for each differential amplifier. The device makes an excellent FM limiter with minimal phase shift. By employing feedback, both selective band-pass amplifiers and notch frequency rejection amplifiers may be built.



$100\Omega < R_T < 150\Omega$
Driver worst-case R_E = 2.2 kΩ @ R_T = 100Ω
Differential gain = 7.0 V/V
Common mode rejection > 60 dB
Common mode voltage rejection range
(voltages between driver and receiver groundes) = +1.5 V
-1.0 V

Fig. 4 TWISTED PAIR LINE RECEIVER



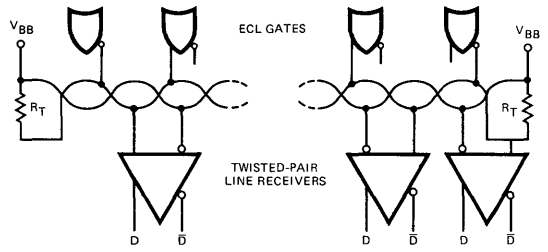
V_R = VOLTAGE DROP ACROSS R_T (TERMINATING RESISTOR)

$$V_R = \frac{(5.2\text{ V} - 0.80\text{ V})\,(R_T)}{2\text{ k}\Omega + R_T}$$

$$= \frac{(4.40)\,(125)}{2125}$$

$$= 260\text{ mV}$$

Fig. 5 LINE RECEIVER DC EQUIVALENT CIRCUIT



System Design Criteria

1. A minimum of two emitter pull-down resistors is recommended in the driver gates.
2. R_T should be Z_{out} of the twisted pair line: 100 to 125 ohms
3. Either OR or NOR outputs may drive the line.
4. All driver gates are ORed together.
5. The line receiver output is Data or $\overline{Data}$ depending upon the input and output configurations.
6. V_{BB} should be able to source 6.0 mA or sink 7.0 mA total current. This is accomplished by the addition of a 500Ω resistor from V_R (Pin 11) to V_{EE}.

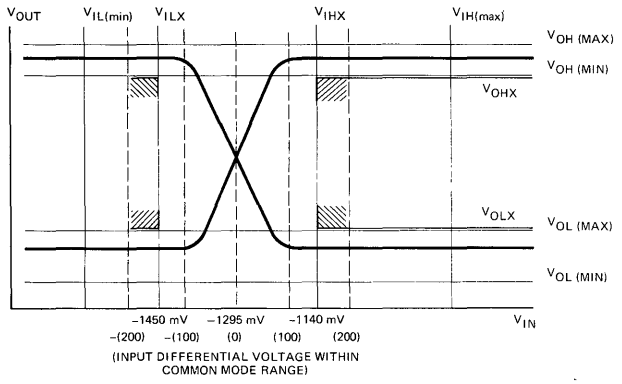
Fig. 6 DATA BUS DRIVING WITH ECL 9500

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	−6 Volts
Supply Voltage V_{EE} (Pulsed)	−8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

DC ELECTRICAL CHARACTERISTICS (Operating Temperature Range 0°C to 75°C, V_{CC} = GND, V_{EE} = −5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS (Measured with $\overline{Inputs}$: $\overline{A}_1, \overline{A}_2, \overline{A}_3$; connected to V_R)	
V_{OH}	Output Voltage High	−900	−850	−800	mV	F.O. = 1 Gate	V_{IL} = −1700 mV for NOR Gate
		−940	−890	−840	mV	F.O. = 5 Gates	V_{IH} = −900 mV for OR Gate
		−975	−925	−875	mV	50Ω to −2.0 V	
V_{OL}	Output Voltage Low	−1745	−1670	−1595	mV	F.O. = 1 Gate	V_{IL} = −1700 mV for OR Gate
		−1785	−1710	−1635	mV	F.O. = 5 Gates	V_{IH} = −900 mV for NOR Gate
		−1775	−1700	−1625	mV	50Ω to −2.0 V	
V_{OHX}	Ouptut Voltage High at V_{IN} (threshold)	−910			mV	F.O. = 1 Gate	V_{ILX} = −1450 mV for NOR Gate } To Each Input Sequentially
		−950			mV	F.O. = 5 Gates	V_{IHX} = −1140 mV for OR Gate } To Each Input Sequentially
		−985			mV	50Ω to −2.0 V	See Fig. 7
V_{OLX}	'Ouptut Voltage Low at V_{IN} (threshold)			−1585	mV	F.O. = 1 Gate	V_{ILX} = −1450 mV for OR Gate } To Each Input Sequentially
				−1625	mV	F.O. = 5 Gates	V_{IHX} = −1140 mV for NOR Gate } To Each Input Sequentially
				−1615	mV	50Ω to −2.0 V	See Fig. 7
I_{PS}	Power Supply Current	35	48	65	mA	All Inputs Open Except A_1, A_2, A_3 to V_R	



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Fig. 7 NOISE MARGIN SPECIFICATION POINTS

FOR LINEAR APPLICATIONS OF THE 9582

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, V_{CC} = GND, $V_{EE} = -5.2$ V)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain		6.0	7.0		V/V
Bandwidth	Open output		70		MHz
Risetime	$R_S = 50\Omega$		2.5		ns
Propagation Delay	$R_S = 50\Omega$		2.4		ns
Input Resistance			1.3		kΩ
Input Capacitance				5.0	pF
Input Offset Current			7.0		μA
Input Bias Current			40		μA
Input Offset Voltage			5.0		mV
Input Voltage Range	Around V_R	±1.3			V
Common Mode Rejection Ratio	$V_{cm} = \pm 1$ V, $f \leq 100$ kHz Around V_R	60			dB
Supply Voltage Rejection Ratio	$\Delta V_S = \pm 0.5$ V	60			dB
Output Common Mode Voltage			-1.3		V
Output Voltage Swing		0.8			Vpp
Output Sink Current		1.3	2.0		mA
Output Source Current				40	mA
Output Resistance			10	20	Ω

DEFINITION OF TERMS

DIFFERENTIAL VOLTAGE GAIN – The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

BANDWIDTH – The frequency at which the differential gain is 3 dB below its low frequency value.

RISE TIME – The time required for an output voltage step to change from 10% to 90% of its final value.

PROPAGATION DELAY – The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

INPUT RESISTANCE – The resistance seen looking into either input terminal with the other grounded.

INPUT OFFSET CURRENT – The difference between the currents into the two input terminals.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO – The ratio of a change in input common mode voltage to the resulting change in output offset voltage referred to the input.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of a change in supply voltage to the resulting change in output offset voltage referred to the input.

OUTPUT COMMON MODE VOLTAGE – The average of the voltages at the two output terminals.

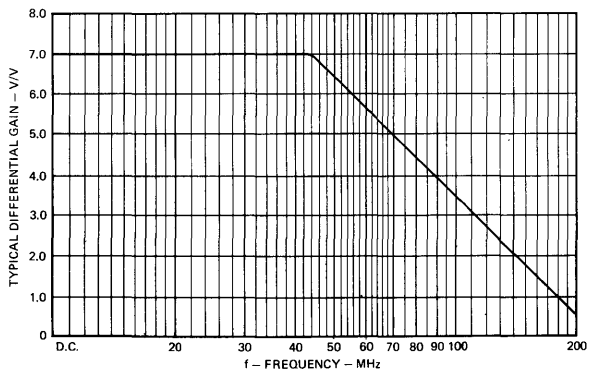
OUTPUT VOLTAGE SWING – The peak-to-peak output swing that can be obtained without clipping. This includes the unbalance caused by output offset voltage.

OUTPUT SINK CURRENT – The peak negative current available at either output of the amplifier.

OUTPUT SOURCE CURRENT – Peak positive current available at either output of the amplifier.

OUTPUT RESISTANCE – The resistance seen looking into either output terminal.

9582 LINE RECEIVER TYPICAL DIFFERENTIAL GAIN VERSUS FREQUENCY



A.C. ELECTRICAL CHARACTERISTICS (Temperature Range 0° C to +75° C, V_{CC} = GND, V_{EE} = –5.2 V)

SYMBOL	CHARACTERISTIC	LIMITS 0° C MIN.	0° C TYP.	0° C MAX.	+25° C MIN.	+25° C TYP.	+25° C MAX.	+75° C MIN.	+75° C TYP.	+75° C MAX.	UNITS	CONDITIONS
t_{pd}	Propagation Delay											
	t_{pd--}		2.3			2.3	3.5		2.5		ns	See Fig. 10
			2.2			2.2	3.5		2.4		ns	R_L = 50Ω to –2.0 V
			2.4			2.4	3.5		2.6		ns	C_L <5.0 pF
			2.5			2.5	3.2		2.7		ns	$t_r = t_f$ = 2.5 ns
t_r	Rise Time		3.0		1.5	3.0	4.5		3.0		ns	
t_f	Fall Time		3.0		1.5	3.0	4.5		3.0		ns	
I_T	Transient Input Current Standard Gate					2.5	3.5				mA	See Fig. 11

Fig. 8
TYPICAL AVERAGE PROPAGATION DELAY CHANGE VERSUS POWER SUPPLY

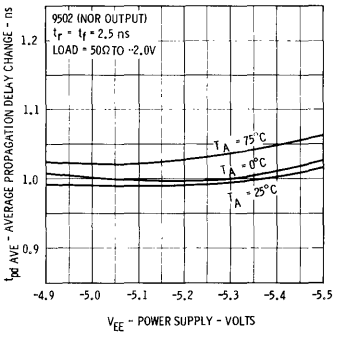
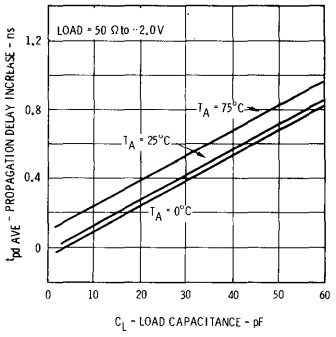
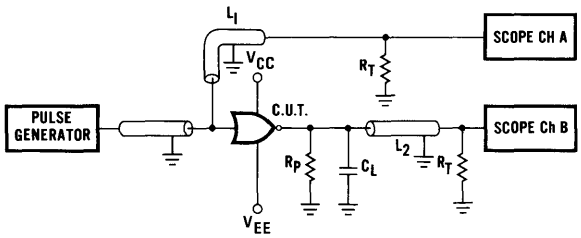


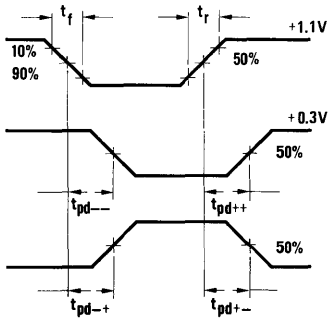
Fig. 9
TYPICAL PROPAGATION DELAY INCREASE VERSUS LOAD CAPACITANCE $t_{pd\ AVE}$ (OR OUTPUT)



$$t_{pd\ ave} = \frac{t_{pd\ rising} + t_{pd\ falling}}{2}$$

REFERENCE: A.C. ELECTRICAL CHARACTERISTICS



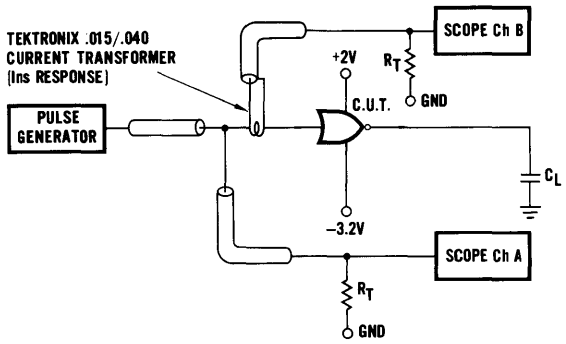


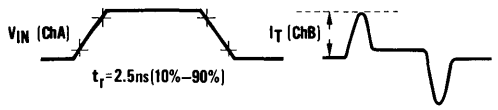
L_1 and L_2 = equal length 50Ω impedance lines
$R_L = R_T$ = 50Ω Termination of Scope
C_L = Jig and Stray Capacitance <5.0 pF

$t_r = t_f$ = 2.5 ns (10% – 90%) Jig setup with no circuit under test
$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = –3.2 V

Fig. 10 SWITCHING TIME TEST CIRCUIT AND WAVEFORM

SWITCHING CHARACTERISTICS (Cont'd)





This test provides a measure of the average value of C_{IN}; also current mismatch in the line.

$V_{CC} = V_{CC}$ (AUX) = +2.0 V
V_{EE} = –3.2 V
R_T = 50Ω (Scope input impedance)
Input signal $t_r = t_f$ = 2.5 ns (10% – 90%)
With no circuit under test

Fig. 11 TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS

INTERCONNECTION RECOMMENDATIONS

All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a –2 volt supply:

Alternately, a 2 resistor divider network may be used with R_1 = 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

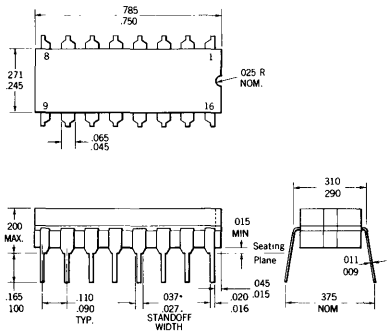
A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

PACKAGE INFORMATION

6B – 16 LEAD DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
*The .037/.027 dimensions does not apply to the corner leads

95H90

VERY HIGH SPEED ÷ 10 / 11 PRESCALER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The ECL 95H90 prescaler is a high speed ECL MSI device designed specifically for the communication and instrumentation manufacturer. In its simplest use it will divide any clock frequency up to 320 MHz, by 10. By using the 95H90, with other control logic a divide by "N" counter can be constructed.

By keeping all the high speed logic manipulation "on chip," a dramatic decrease in power and increase in reliability and wire-ability are made available at much lower cost than a comparable SSI function.

FEATURES

- **HIGH SPEED . . . 320 MHz (TYP.)**
- **÷10/11 ENABLE**
- **HIGH SPEED RESET**
- **SEPARATE CURRENT SWITCH EMITTER FOLLOWER V_{CC} PINS — ELIMINATE NOISE COUPLING**
- **TEMPERATURE COMPENSATION**
- **INTERNAL PULL DOWN**
- **50 Ω LINE DRIVE CAPABILITY**
- **SINGLE –5.2 VOLT POWER SUPPLY**
- **HERMETIC CERAMIC 16 PIN DIP**
- **COMPLEX MULTI-GATE CHIP REDUCES PACKAGE COUNT & POWER**
- **LOW CLOCK FEED-THROUGH OF ONLY 70 mV (TYP.)**
- **SMALL SIGNAL INPUT IMPEDANCE POSITIVE REAL FOR ALL FREQUENCIES**

PIN NAMES

$\overline{CP}_1$, $\overline{CP}_2$	Dual "OR" Clock Inputs (Active High)
$\overline{PE}_1$, $\overline{PE}_2$	Prescale by 11 (eleven) "AND" Enable Inputs (Active Low)
MS	Asynchronous Master Set (Active High)
Q_4	Assertion Output
$\overline{Q}_4$	Negative Output

ORDER INFORMATION

Specify U6B95H90XXX for 16 pin Dual In-Line package where XXX is 59X for the 0°C to +75°C and 56X for the –20°C to 100°C temperature range.

LOGIC SYMBOL

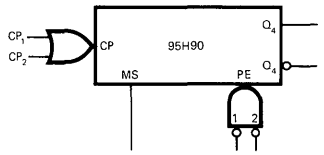


Fig. 1

CONNECTION DIAGRAM DIP (TOP VIEW)

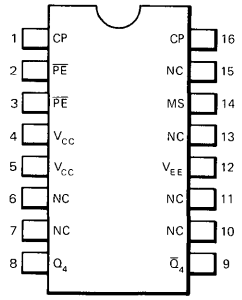


Fig. 2

LOGIC DIAGRAM

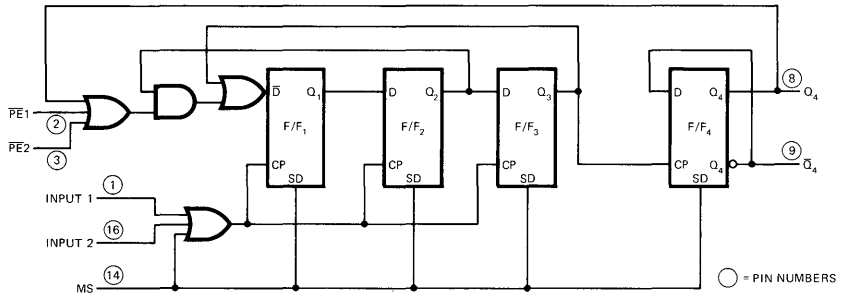


Fig. 3

COUNT SEQUENCE

Q_1	Q_2	Q_3	Q_4
H	H	H	H
L	H	H	H
L	L	H	H
L	L	L	H
H	L	L	H
H	H	L	H
L	H	H	L
L	L	H	L
L	L	L	L
H	L	L	L
H	H	L	L

NOTE: "HHHH" is set state and additional state for ÷11 mode.

FUNCTIONAL DESCRIPTION

The Device acts as a controllable (divide by 10/divide by 11) prescaler, accepting clock pulses of up to 320 MHz. Output Q_4 is low for 5 incoming clock pulses and high for the subsequent 5 or 6 incoming clock pulses, the decision between the two modes is made by the state of the two active low PE inputs. If both $\overline{PE}_1$ and $\overline{PE}_2$ are low 5.4 ns before the rising edge of Q_4, then Q_4 will stay high for 6 incoming clock pulses (divided by 11), if either $\overline{PE}_1$ or $\overline{PE}_2$ is high before the rising edge of Q_4, the output will stay high for 5 clock pulses (divided by 10).

The two input "OR" clock inputs can be used to combine two independent clock sources or one input can act as a clock enable (active low).

A master set is provided to initialize the prescaler. This input, when activated, overrides the clock and forces the prescaler into the HHHH state with Q_4 forced high and $\overline{Q}_4$ forced low. The prescaler will divide by 11 the first count cycle after being master set.

NOTE:
When using the 95H90 simply as a modulo 10 prescaler, the $\overline{Q}$ output may be connected to a $\overline{PE}$ input.

95H90 MODE SELECTION TABLE

$\overline{PE}_1$	$\overline{PE}_2$	PRESCALER MODULO
		Divide By
L	L	11
L	H	10
H	L	10
H	H	10

D. C. ELECTRICAL CHARACTERISTICS (Operating Temperature Range: $T_A = 0^oC$ to 75^oC) (V_{CC} = GND, $V_{EE} = -5.2V$)

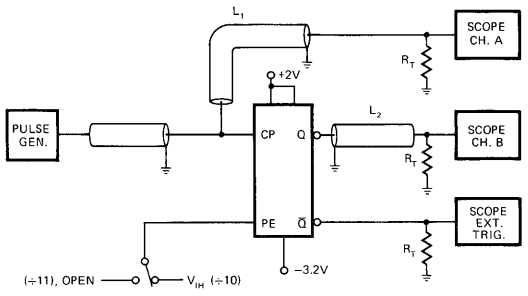
SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
V_{OH}	Output Voltage High		−860 −910 −950		mV	FO= 1 Gate FO= 5 Gates R_L = 50 Ω to −2.0V	$V_{IN} = V_{IL}$ (−1700mV) or V_{IH} = (−900mV) as per Count Sequence
V_{OL}	Output Voltage Low		−1690 −1740 −1720		mV	FO= 1 Gate FO= 5 Gates R_L = 50 Ω to −2.0V	$V_{IN} = V_{IL}$ (−1700mV) or V_{IH} = (−900mV) as per Count Sequence
V_{OHC}	Output Voltage High at $V_{IN} = V_{IX}$ (threshold)	−930 −970 −1010			mV	FO= 1 Gate FO= 5 Gates R_L = 50 Ω to −2.0V	$V_{IN} = V_{ILX}$ or V_{IHX} as per Count Sequence
V_{OLC}	Output Voltage Low at $V_{IN} = V_{IX}$ (threshold)			−1605 −1655 −1635	mV		$V_{IN} = V_{ILX}$ or V_{IHX} as per Count Sequence
V_{IHX}	Input High Threshold Voltage	−1140			mV		Guaranteed Input High Threshold Voltage
V_{ILX}	Input Low Threshold Voltage			−1450	mV		Guaranteed Input Low Threshold Voltage
$I_{IN(H)}$	Input Current High		2.40	3.65	mA		V_{IN} = −900mV to MS Input (Pin 14)
$I_{IN(H)}$	Input Current High		2.25	3.15	mA		V_{IN} = −900mV to other Inputs Sequentially
$I_{IN(L)}$	Input Current Low		1.75	2.40	mA		V_{IN} = −1700 mV to Each Input Sequentially
I_{PS}	Power Supply Current	66	90	119	mA		All Inputs Open

A.C. ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = GND, V_{EE} = –5.2V)

SYMBOL	CHARACTERISTIC	LIMITS 0°C TYP.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C TYP.	75°C MAX.	UNITS	CONDITIONS
t_{pd}	Propagation Delay(50%-50%)									Output
	CP to Q_4, t_{pd++}	4.9		5.1	6.8		5.5		ns	R_L = 50Ω to –2.0V
	CP to Q_4, t_{pd--}	4.9		5.1	6.8		5.5		ns	C_L = 5.0pF
	MS to Q_4, t_{pd++}	5.3		5.7	7.6		6.5		ns	Input
	$\overline{PE}$ to Q_4, t_{pd++}(Note 1)	5.2		5.4			5.8		ns	$t_r = t_f$ = 2.2±0.1 ns (10%-90%)
t_r	Output Rise Time (10%-90%)	2.4	1.2	2.4	3.6		2.4		ns	
t_f	Output Fall Time (10%-90%)	2.4	1.2	2.4	3.6		2.4		ns	
t_{ri}=t_{fi}	Clock Input Transition Time	30			25			25	ns	Input t_r, t_f for correct operation
f_{max}	Maximum Clock Frequency	320	220	320			270		MHz	Sine Wave of 800mVpp about –1300mV

Note 1: See Functional Description and Top of Page 5

Fig. 4. SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



CONDITIONS

V_{CC} = +2.0 V

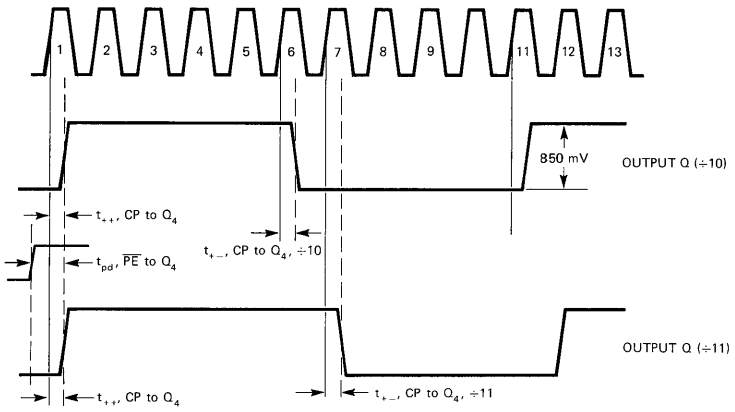
V_{EE} = –3.2 V

R_L = 50Ω = R_T (Scope input impedance)

C_L = Jig and stray capacitance <5 pF

L_1 = L_2 equal 50Ω impedance lines

Input signal t_r = t_f = 2.5 ns (10% - 90%)
with no circuit under test



CLOCK PULSE CONDITIONS

V_{IH} = +1050 mV

V_{IL} = +280 mV

t_r = t_f = 2.2 ± 0.1 ns (10% - 90%)

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} (Continuous)	–6 Volts
Supply Voltage V_{EE} (Pulsed)	–8 Volts
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

APPLICATIONS

Prescaler —In its simplest application, as a divide-by-ten prescaler, the 95H90 extends the frequency range of TTL frequency counters and phase locked systems to over 300 MHz (Figure 5). For this and other RF applications the input bias should be set close to the clock threshold ($R_2 \approx 3 \cdot R_1$). This improves AC-sensitivity but it also increases noise sensitivity. A preamplifier is often a better way to improve sensitivity (Figure 6), especially in frequency counters. Care should be taken to avoid overdriving the prescaler input which would saturate the input transistor and seriously degrade the frequency resolution. Excessive input voltages might also damage the device.

Fig. 5. Divide by ten RF prescaler

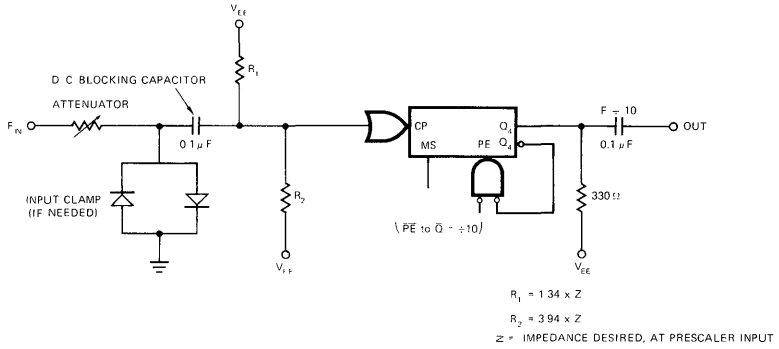
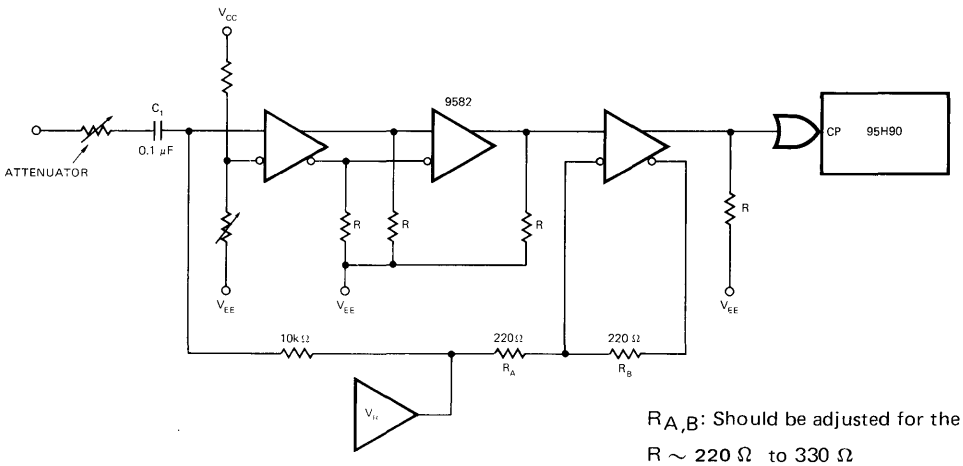


Fig. 6. Prescaler with RF preamplifier



$R_{A,B}$: Should be adjusted for the desired Hysteresis

R ~ 220 Ω to 330 Ω

Programmable Divider for Frequency Synthesizers — An integral part of most frequency synthesizers is a programmable divider. In a conventional design these become bulky, expensive and power consuming when implemented for frequencies above the TTL range. The 95H90 is especially designed for a technique called "pulse swallowing" which allows a simple high speed ECL divider (the 95H90) to be controlled by a relatively slow TTL-MSI presettable counter. This technique offers the advantage of prescaling (only the simple prescaler operates at the high input frequency) but it does not sacrifice resolution. The only drawback (usually not a limitation) is that there is a clearly defined minimum divide ratio below which the system does not function.

Pulse swallowing uses three functional blocks: (Figure 7)

(1) A variable modulo prescaler, controllable between modulo K and K+1 (typically 10/11, 20/21 or 100/101),

(2) A swallow counter which controls the prescaler, and

(3) A programmable counter.

The swallow counter determines the number of times that the prescaler divides by K+1, effectively swallowing one additional input pulse for each output pulse to the programmable counter. As an example, consider a divider (K = 10) that is programmed by decade switches. Inverting nine's complement decade switches are required, since the switch must ground the counter input in order to insert a zero. At the beginning of a divide cycle the swallow counter and the program counter are loaded with the nine's complement of the desired ratio and the count from there to their respective terminal states. If a ratio of 83 is desired, the swallow counter is preset to 6 and the program counter to 9991. The programmable counter will produce a terminal count output after 8 pulses from the prescaler, but since the swallow counter was preset to 6, the prescaler will have divided by 11 three times, by 10 the other five times. As a result, the output pulse will occur after 83 input pulses.

The prescaler modulo (K) is chosen to bring the prescaler output frequency into the range of TTL. Higher modulo (20/21, 100/101) prescalers can be implemented by additional flip-flops and counters.

An important speed parameter to be considered is the delay in the 10/11 prescaler control path. The delay through the ECL/TTL interfaces, the TTL logic, and back through the TTL/ECL interface must be less than $10/f_{in} - t_{pd}$ from Q_4 to PE.

APPLICATIONS (Cont'd)

Fig. 7. PULSE SWALLOWING PROGRAMMABLE DIVIDER

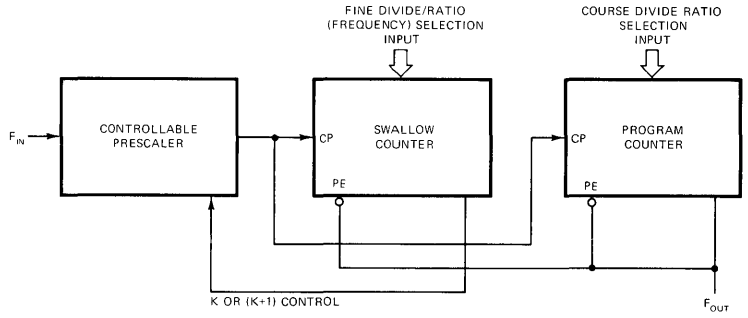
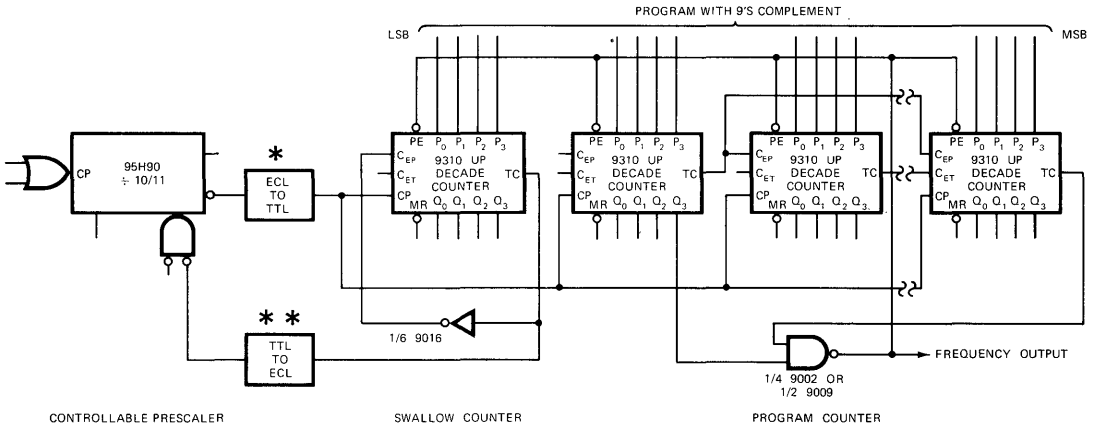
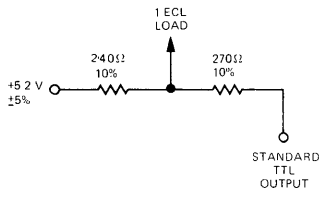


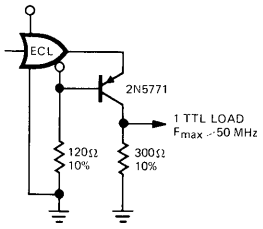
Fig. 8. HIGH SPEED PROGRAMMABLE DIVIDER (UTILIZING 10/11 PRESCALER)



***TTL to ECL, Common Power Supply.**



****ECL to TTL, Common Power Supply.**



INTERCONNECTION RECOMMENDATIONS

All high speed ECL circuits demand that special precautions be taken for optimum system performance. A ground plane must be provided for a good, low impedance, ground current return path and to transform interconnections into microstrip transmission lines. The voltage supply line should be well decoupled with small ceramic capacitors throughout each card between V_{EE} and the ground plane and by including at least one larger tantalum capacitor per card.

Typical microstrip lines have a characteristic impedance between 50 and 150 ohms with the lower being more desirable in ECL systems. For local interconnects the internal 2 kΩ resistors provide adequate termination but for optimum performance lines longer than 6 or 8 inches in length should be terminated in their characteristic impedance.

Lines up to 12 inches may be left unterminated if a degraded waveform can be tolerated with the resultant decrease in speed and increase in ringing.

Microstrip interconnections may be terminated by a resistor to a −2 volt supply: $R = \frac{Z_O}{1 - NZ_O/2000}$ where Z_O is the characteristic impedance of the line and N is the number of loads. Alternately, a 2 resistor divider network may be used with R_1 and 1.6 R connected to ground and R_2 = 2.6 R connected to V_{EE}.

Series terminating resistors decrease noise immunity and slow rise and fall times, but can still be used if these effects are tolerable. In addition, care must be taken to avoid glitches in the threshold region of the waveform occurring at certain combinations of line length and series resistor value.

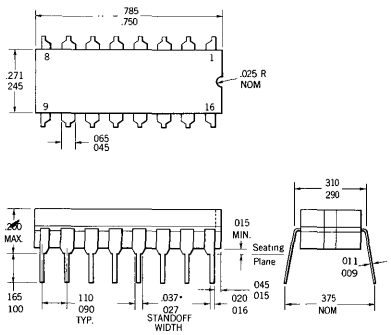
A single terminated wire running over a ground screen can be used for backpanel interconnections up to 4 or 5 inches in length, but terminated coaxial cables or terminated twisted pairs of wire are required for longer interconnections.

LINE DRIVING CAPABILITY

The 9500 series ECL circuits are capable of driving fairly long lines if the previous recommendations are followed. 50 ohm coaxial cables 10 feet in length or longer and properly terminated may be driven with almost no degradation in the waveform. The normal delay due to the finite speed of the signal traveling down the cable will be encountered in addition to a slight decrease in signal swing. This decrease caused by the attenuation of the cable (about 40 mV for 10 feet of 50 ohm coax) will lower the noise immunity of the receiving circuit by the same amount. Care must be exercised to ensure the ground potentials at the driving and receiving ends of a line are equal and no differential noise is present.

PACKAGE INFORMATION

6B — 16 LEAD SSI DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads

9595

DUAL HIGH SPEED ECL TO TTL CONVERTER

FAIRCHILD TEMPERATURE COMPENSATED ECL

GENERAL DESCRIPTION — The ECL 9595 is a high speed logic converter for use in systems using both the high speed of ECL and the many available functions of TTL. The 9595 requires the −5.2 volt V_{EE} supply of ECL and the +5 volt V_{CC} of TTL. The TTL fanout may be expanded by adding more pulldown current at the TTL output pin.

By allowing the logic converter to function as a logic gate the normally wasted time of logic conversion may be used in the logic implementation with the through delay generally less than that found in TTL circuits.

FEATURES:

- **HIGH SPEED . . . 6.0 ns**
- **FAN OUT 10 TTL LOADS WITH EXTERNAL PULL DOWN RESISTOR**
- **NO INVERSION THROUGH CONVERTER**
- **ECL INPUT TEMPERATURE COMPENSATED**
- **INTERNAL PULL DOWNS**
- **HERMETIC CERAMIC 16 PIN DIP**
- **FUNCTIONS AS DUAL 4 INPUT GATE**
- **TWO SEPARATE V_{CC} PINS ELIMINATE NOISE COUPLING**

ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

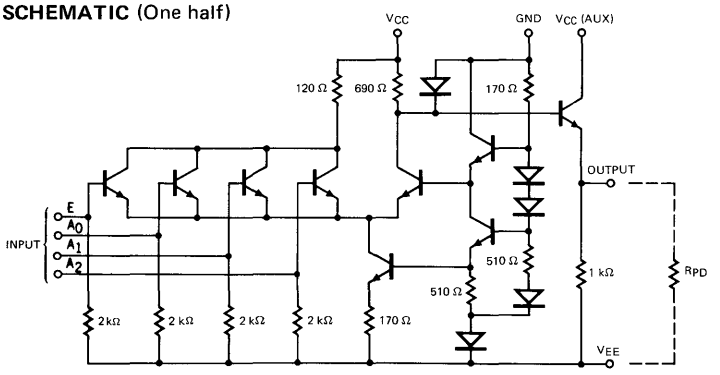
Storage Temperature	−65°C to +150°C
Junction Temperature	+150°C
Supply Voltage V_{EE} Continuous (Pulsed)	−6 Volts (−8 Volts)
Supply Voltage V_{CC} Continuous (Pulsed)	+6 Volts (+8 Volts)
Input Voltage	GND to V_{EE} (max)
Output Current	40 mA

PIN NAMES

A_N = OR Inputs to A Gate
Q_A = TTL Output of A Gate
B_N = OR Inputs to B Gate
Q_B = TTL Output of B Gate
E = Common Enable Input to A and B Gates

ORDER INFORMATION — Specify U6B9595XXX for 16 pin Dual In-Line Package where XXX is 59X for the 0°C to +75°C temperature range.

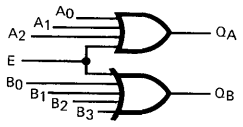
CIRCUIT SCHEMATIC (One half)



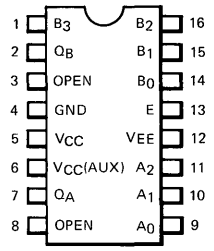
External Pull Down Resistor (R_{PD}) to V_{EE}:
(Recommended for best speed and noise immunity)

$3 \leqslant$ Fan Out $\leqslant 10$
$R_{PD} = 360\ \Omega$

LOGIC SYMBOL

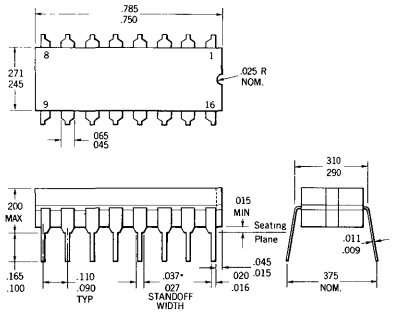


CONNECTION DIAGRAM
DIP (TOP VIEW)



PACKAGE INFORMATION

6B–16 LEAD SSI DUAL IN-LINE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams
* The .037/.027 dimensions does not apply to the corner leads

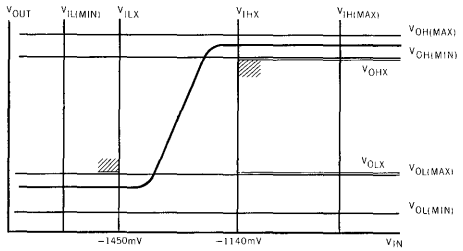
DC ELECTRICAL CHARACTERISTICS (Operating Temperature: T_A = 0°C to 75°C, V_{CC} = V_{CC} (AUX) = +5.0 V ±5%, V_{EE} = –5.2 V ±5%.

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
V_{OH}	Output Voltage High	2.40	3.90		V	R_{PD} = 360 Ω to V_{EE}, See Fig. 5 V_{IN} = –1140 mV (V_{IHX}) or More Positive (for V_{OH})
V_{OL}	Ouput Voltage Low	–2.0	–1.5	0.4	V	F.O. = 1 (I_S = 1.6 mA), No External R_{PD}, See Fig. 5 V_{IN} = –1450 mV (V_{ILX}) or More Negative (for V_{OL})
$I_{IN(H)}$	Input Current High		2.25	3.10	mA	V_{IH} = –900 mV
$I_{IN(L)}$	Input Current Low		1.75	2.35	mA	V_{IL} = –1700 mV
I_{PS}	Power Supply Current	28	37	44	mA	All Inputs Open

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = V_{CC} (AUX) = +5.0 V, V_{EE} = –5.2 V)

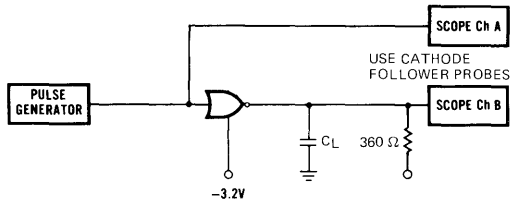
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{pd}	Propagation Delay		6.0	8.0	ns	See Fig. 6
t_r	Rise Time	3.0	6.0	8.0	ns	C_L < 5.0 pF
t_f	Fall Time	3.0	6.0	8.0	ns	t_r = t_f = 2.5 ns (10%–90%)
I_T	Transient Input Current		2.0	3.5	mA	See Fig. 7
	Enable Line	2.8	2.8	5.7	mA	

Fig. 5 — NOISE MARGIN SPECIFICATION POINTS



Corner points indicated on the transfer characteristics represent the worst case points (thresholds) at which the device will start to switch. The values V_{ILX} and V_{IHX} define the maximum width of the transition region.

Fig. 6. SWITCHING TIME TEST CIRCUIT AND WAVEFORM



t_r = t_f = 2.5 ns (10% - 90%)
Jig setup with no circuit under test
V_{CC} = V_{CC} (AUX) = +5.0 V
V_{EE} = –5.2 V
C_L = Jig and Stray Capacitance <5.0 pF

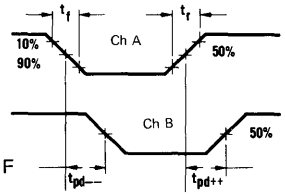
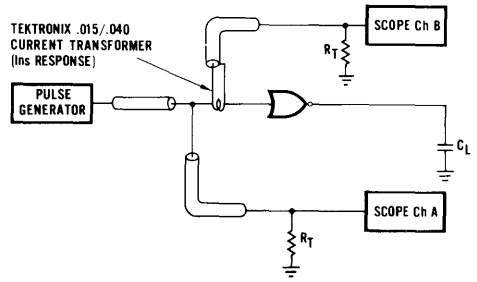
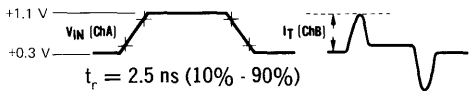


Fig. 7. TRANSIENT INPUT CURRENT TEST CIRCUIT AND WAVEFORMS





This test provides a measure of the average value of C_{IN}; also current mismatch in the line.
V_{CC} = V_{CC} (AUX) = +5.0 V
V_{EE} = –5.2 V
R_T = 50 Ω Termination of Scope
C_L = Jig and Stray Capacitance <5.0 pF

DESIGN INFORMATION

9500 SYSTEM APPLICATION AND WIRING RULES

INTRODUCTION

High speed is essential in many real-time data processing and communications systems. In addition, the cost of information processing on large digital computers is inversely proportional to the square root of the machine's speed. These system requirements have prompted the design of the Fairchild 9500 Temperature Compensated ECL family. This series offers standard gate propagation delays of 2 to 3 ns, high-speed gates with propagation delays of 1 to 2 ns and internal MSI gates with typical delays of 1.5 ns.

To achieve speeds faster than 3 ns, the use of nonsaturating circuitry is essential. This is attained with ECL by maintaining a narrow logic swing. Keeping transistors out of saturation eliminates the long turn-off delay caused by excess stored charge. This, together with ECL logic advantages such as wired-OR and complementary outputs, permits system speeds four to ten times faster than conventional or Schottky TTL.

The penalties that must be paid for high speed are generally more restrictive wiring rules regardless of logic family, ECL or TTL. The necessity of terminating connecting lines and considering capacitive loading effects on high fan-out, short lines has been minimized in the design of the 9500 ECL family. Power per package has been optimized in a trade-off of gate-power and ease of wiring. The advantages of ECL are in the implementation and use of MSI. ECL's greater logic flexibility also means fewer gates per function for most systems. This implies that if an ECL and TTL logic family is each used in an efficient manner to process a given amount of data, the power requirements of the ECL system would be lower than those of the TTL system.

THE 9500 SERIES

9500 Series ECL elements have been designed with unique temperature compensation circuitry and other features aimed at extending the advantages of high speed to a wide range of low cost applications. This is achieved by simplifying the application and usage rules traditionally associated with ECL.

At gate propagation delays faster than 4 ns, package interconnections begin to look like transmission lines. Unless these conditions are handled correctly, reflections or crosstalk can cause unreliable system operations. This is common to all high speed logic forms including TTL.

9500 elements have been designed for use on standard two-sided printed circuit boards. Higher performance can be achieved with a ground plane or with multilayer boards which convert printed wiring into a controlled impedance system of high speed transmission lines. ECL input and output impedances are compatible with optimum transmission line requirements.

9500 BASIC GATE OPERATION

In the basic ECL gating circuit shown in Figure 1, T4 acts as a constant current source while T5 establishes a reference voltage for T3. Current must flow through T1, T2 or T3. If both inputs are LOW, T1 and T2 are OFF and current flows through T3 and R2 bringing the voltage on the collector of T3 negative, but not low enough to saturate the transistor. This negative voltage is reflected on the OR output as a LOW by transistor T8, an emitter follower. Little current flows through R1, forcing the NOR output HIGH. If either input is HIGH, most of the current flows through R1 instead of R2, forcing the NOR output LOW and the OR output HIGH. 2-kilohm resistors are included on the inputs and outputs to provide pulldown and to permit short interconnections without external resistors. These resistors also permit unused inputs and outputs to be left unconnected with no degradation in performance. These 2-kilohm resistors have been replaced with 50-kilohm resistors on the 95L22, L23 and L24 gates. This allows high fan-out and series terminations. The rest of the circuitry is used to generate the reference voltage and to provide temperature compensation for both the reference and output voltages. Separate V_{CC} (ground) pins are provided for the input circuitry reducing noise problems when driving unbalanced loads.

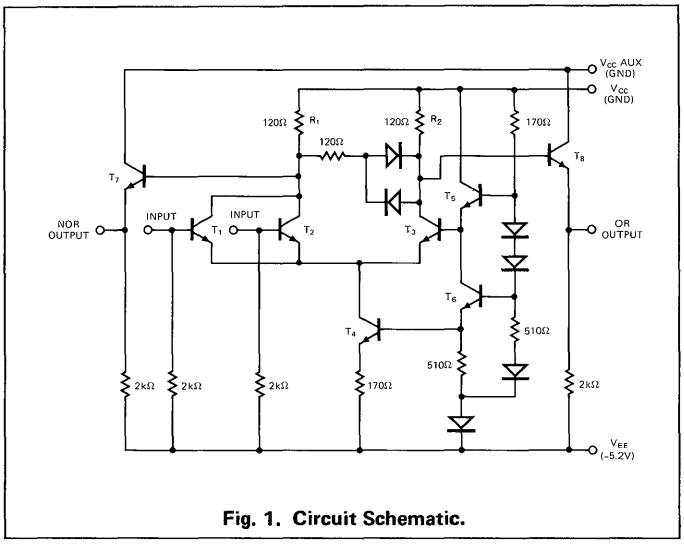


Fig. 1. Circuit Schematic.

9500 series circuits employ a unique temperature compensation network making the output HIGH and LOW levels and the input threshold level almost insensitive to temperature. This is extremely significant in maintaining full system noise immunity over all operating temperatures. In addition, interfacing circuits with different power dissipation, and thus different operating temperatures, does not decrease the noise immunity. A detailed description of the compensation action is provided in Fairchild Application Note APP-206.

The 9500 Series flip-flops and MSI elements use the same basic gating circuit with temperature compensation, but in addition make use of series gating and other ECL design techniques to achieve the required logical functions with minimum propagation delays and minimum power dissipation. All input and output levels for these devides are identical to the gate input and output levels.

All 9500 series outputs are buffered, using an emitter follower to make all outputs wire-ORable. The isolation provided by these output buffers makes it impossible to affect the state of a flip-flop or latch. Backlatching is therefore impossible.

Device Descriptions

Logic configurations, pin connections and loading for the basic elements in the 9500 series ECL family are shown in Figure 3. Positive logic is assumed.

ONE (HIGH) = –0.900 V., ZERO (LOW) = –1.700 V. All active LOW inputs and outputs are indicated by a small circle.

Gates

The simplest building block in the ECL family is the NOR gate. Nine are available in three gate configurations: the dual 4-input gates, the triple 2-input gates and the quad 2-input gates. The OR output from each gate is available on the dual and triple units. For each of the dual, triple and quad gate configuration three types of gates are available:

Basic 2.4-ns 9500 gates –	9502 dual, 9503 triple, 9504 quad
Basic 1.6-ns 95H00 gates –	95H02 dual, 95H03 triple, 95H04 quad
High input impedance, high-speed lower power gates –	95L22 dual, 95L23 triple, 95L24 quad

In addition, each device is equipped with a common enable input controlling all the gates in the package. If the enable line is held HIGH, all NOR outputs are forced LOW and all OR outputs HIGH. Alternatively, the NOR gates may be viewed as AND gates with active LOW inputs, as indicated in Figure 2.

Fig. 2. Logically Equivalent Representations of OR/NOR Gates.

Selecting Gate Types

Standard 9500 gates should be used whenever possible because: 1. they have the lowest cost, and 2. they allow use of the easiest wiring.

High-speed gates should be used in areas of a system where speed is critical, such as register switching and clock driving.

The high input impedance low power gates should be used whenever maximum fan-out (>10) or wire-OR is needed. These gates also permit power savings and special wiring by allowing series terminations to be used.

Low power gates should also be used whenever overall system power is critical. The main disadvantage of these gates is their fan-out sensitivity and the need for external resistors for every output. These gates are similar to the internal gates found in the MSI elements.

Standard devices will satisfy most system requirements with only a small percentage of high-speed and high input impedance gates being needed.

All MSI elements are supplied with internal low-power gates and internal 2 k ohm pulldown resistors so that circuits can be wired directly without additional components and still maintain reasonable package power levels.

Two additional gate building blocks can be used to reduce package count and delay. These are the 9505 OR-AND and the 9507 quad AND gates. A specific advantage of the 9505 is the high-speed ANDing of four OR gates by collector dotting and wire ORing. The 9507 quad AND uses series gating to attain the positive logical AND and achieves an 8-input NAND function by dotting the complement outputs.

9595 ECL to TTL Interface

Another special gate found in the 9500 family is the 9595 ECL to TTL interface element. This device is logically organized as two OR gates, one 3-input and one 4-input. Like the basic gates, the 9595 has a common enable input. With an ECL logic "l" this enable input forces the outputs to a TTL logic "l". With the additional gate inputs and the 6 ns typical conversion delay, a hybrid system of ECL and TTL (or ECL and TTL-level MOS) can be constructed utilizing the optimum speeds and advantages of each.

The 9595 can also be used as a computer interface element. In this case both outputs should be connected together to give a maximum drive of 80 mA with both gates driven in parallel through the enable input.

Line Receiver: 9582

The 9582 consists of three differential input amplifiers. Both the true and complement outputs are temperature compensated to be compatible with other ECL 9500 products. With appropriate connection of the base pins the device will function as a differential line receiver, Schmitt trigger, high-speed comparator, broad-band video, IF or RF amplifiers, or as an oscillator. V_{ref} is made available to allow use of this device as a high input impedance buffer gate.

Dual D Flip-Flop: 9528 (160 MHz), 95H28 (260 MHz),

The dual D flip-flops will function in high speed counting, shifting or data storage applications. Each flip-flop is provided with asynchronous set direct and clear direct inputs as well as both assertion and negation outputs. Each flip-flop consists of both a master and a slave. While the clock is LOW the slave is held steady, but the information on the D (data) input is permitted to enter the master. The next clock transition from LOW to HIGH locks the master in its present state, making it insensitive to the D input, and connects the slave to the master, causing the new information to be reflected on the outputs. The following clock transition from HIGH to LOW again locks the slave and permits new information to flow into the master.

The internal clock is the OR of two clock inputs, one common to both flip-flops. The outputs will only switch following a LOW to HIGH transition of the ORed clock (unless either the set direct or clear direct input is activated). The ORed clock permits the use of one input as a clock pulse input and the other as an active LOW enable. If one clock input (the enable line) is held HIGH, clock pulses on the other input will not be seen by the flip-flop. To maintain synchronous operation however, this enable should only be changed while the clock is HIGH.

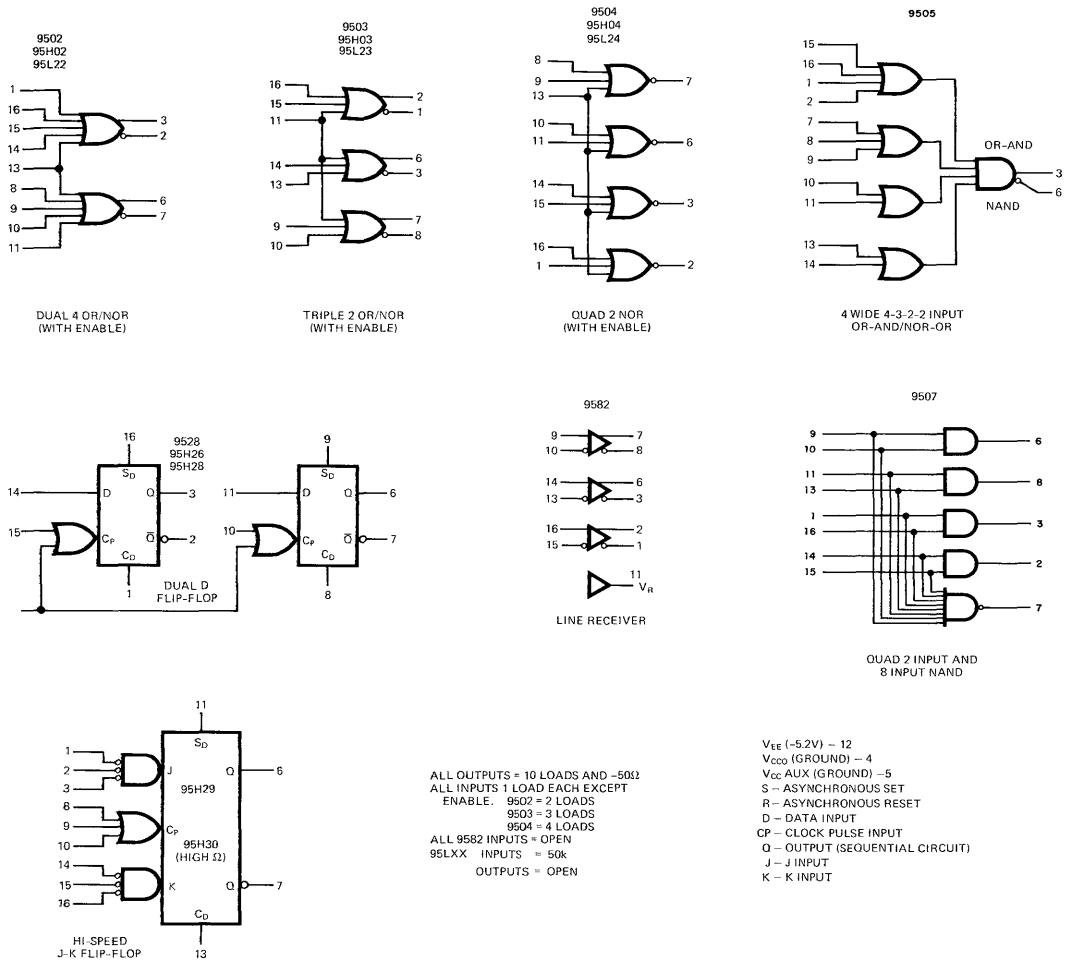


Fig. 3. 9500 Series Basic ECL Circuits.

$\overline{J}$-$\overline{K}$ Flip-Flops – 95H29 (260MHz),

The 95H29 is a high-speed, edge-triggered $\overline{J}$-$\overline{K}$ master-slave flip-flop with both direct set and clear inputs. The $\overline{J}$-$\overline{K}$ and Clock functions are the active low AND of three inputs. With these inputs this device can be used effectively in counters, registers and other applications where data must be stored or shifted at a high rate. In addition, the full frequency range can be used effectively as a prescaler and controlled divider for frequencies up to 260 MHz.

Loading

The input and output loading for the 9500 series ECL circuits is given in Figure 3. As indicated, outputs are capable of delivering the DC currents required by a fairly large number of inputs, but a degradation in the AC performance must be expected if many loads are driven from one output.

For optimum performance, limiting the fan-outs to fewer than those specified as maximum is desirable. The number of loads an output can satisfactorily drive depends on the length of interconnecting lines, the impedance of the lines, terminations used and the required performance. The information given on the data sheets will permit the designer to determine a more stringent set of fan-outs applicable to his specific interconnection configurations and performance requirements.

Each output that is wire-ORed together can be considered as one additional input load. So, if three outputs are wire-ORed together, the fan-out should be decreased by two. For high impedance devices only AC fan-out need be considered. With the high capacity output found in the standard high speed 9500 ECL driving the high input impedance, lower power gates, the maximum AC fan-out with slight speed degredation will be about 10 load units. For the high speed low power devices, six standard gate AC and DC loads and one 50 ohm, shunt-terminated line will be the maximum for full speed performance. With series termination schemes this fan-out may be increased to a maximum of 16, or 4 per series load.

APPLICATION

OR/NOR Gate Flexibility

In addition to offering high speed, 9500 series ECL gates add a new freedom to logic design. Wire-ORing outputs is permitted, and both the OR function and the NOR function may be implemented directly. Tying gate outputs together results in a true wired-OR function, i.e., if either output is a ONE, the function is ONE. This is different from the so-called wired-OR function achieved by tying DTL gate outputs together; really a wired-AND function.

Of the 16 possible functions of two variables, A and B, six are trivial: 1, 0, A, $\overline{A}$, B and $\overline{B}$. Simple implementations of the other 10 are shown in Figure 4. They may all be implemented with no more than two gate delays. If both assertion and negation inputs are available, any of these 10 functions may be implemented with only one gate delay. Only a single gate package is required to implement any of the function.

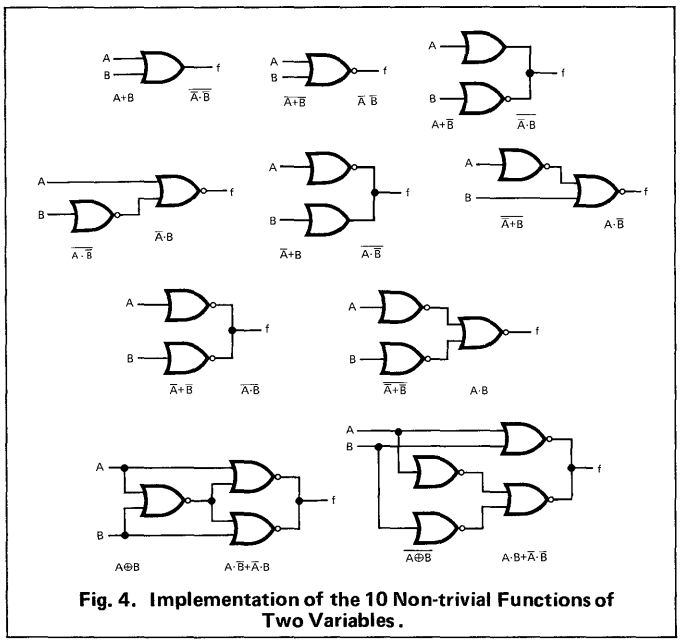


Fig. 4. Implementation of the 10 Non-trivial Functions of Two Variables.

9500 series ECL gates are provided with common enable inputs. The enable input may be used as an additional data input if one particular variable is required as an input to each gate, or if a variable is required as an input to some of the gates in the package and is redundant as an input to the others. The enable input is used in this way in some of the examples in the following section. This section gives examples of functions implemented using SSI elements, complex gates, and MSI elements. The MSI elements make ECL sub-nanosecond speeds usable with ordinary wiring rules.

High Speed Adder Using SSI

ECL gates permit the implementation of very high speed adders. Ripple adders require the least circuitry, but are too slow for longer word lengths to be included in a high-speed ECL system. The most commonly used technique for increasing the speed of an adder is the use of carry generate (CG) and carry propagate (CP) signals.

These two signals are generated by each adder stage and are only a function of the operands and not of the incoming carry. A carry lookahead unit accepts these signals from a number of adder stages and generates the carries directly.

A single adder stage is shown in Figure 5A, and a carry lookahead unit for four stages is shown in Figure 5B. Figure 5C shows the units interconnected to form a 4-bit adder. The carry generate (CG) and carry propagate (CP) signals are generated in one gate delay. The carries in two more gate delays and the sum outputs follow one additional gate delay later. This results in four gate delays for an addition. The number of delays in the adder from the A and B inputs to the S output (three delays) can be reduced, but the total addition time would not be shortened. The Boolean equations for the adder and carry lookahead are shown in Table 1.

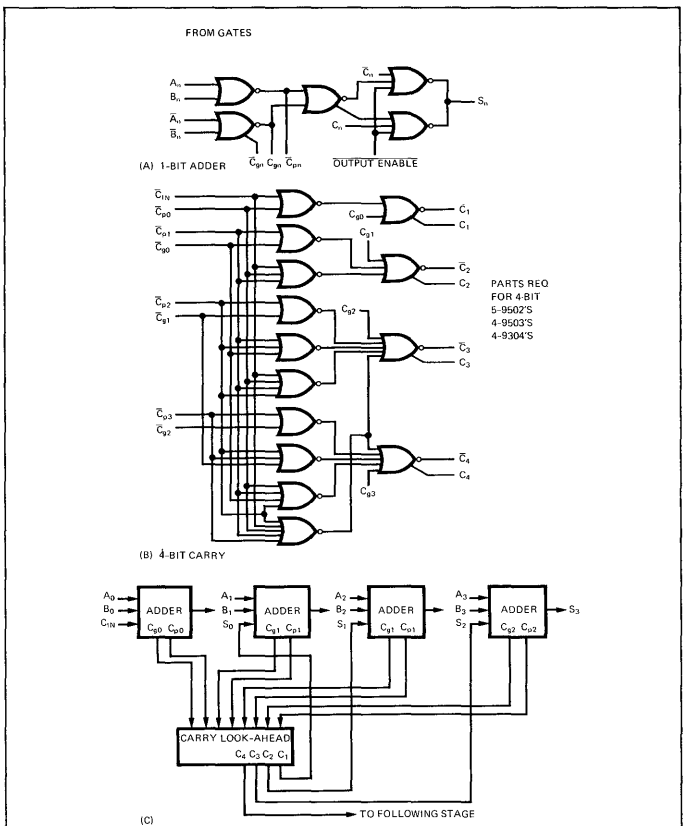


Fig. 5.

$$C_p = A + B$$

$$C_G = A \cdot B = \overline{\overline{A} + \overline{B}}$$

$$S = (A \cdot B + \overline{A} \cdot \overline{B}) \cdot C + (A \cdot \overline{B} + \overline{A} \cdot B) \cdot \overline{C}$$

$$= \overline{[(\overline{A} + \overline{B}) + (A + B) + C]} + \overline{[(\overline{A} + B) + (\overline{A} + \overline{B}) + C]}$$

$$C_1 = C_{g0} + C_{in} \cdot C_{p0} = C_{g0} + \overline{(\overline{C_{in}} + \overline{C_{p0}})}$$

$$C_2 = C_{g1} + C_{g0} \cdot C_{p1} + C_{in} \cdot C_{p0} \cdot C_{p1}$$

$$C_3 = C_{g2} + C_{g1} \cdot C_{p2} + C_{g0} \cdot C_{p1} \cdot C_{p2} + C_{in} \cdot C_{p0} \cdot C_{p1} \cdot C_{p2}$$

$$C_4 = C_{g3} + C_{g2} \cdot C_{p3} + C_{g1} \cdot C_{p2} \cdot C_{p3} + C_{g0} \cdot C_{p1} \cdot C_{p2} \cdot C_{p3} + C_{in} \cdot C_{p0} \cdot C_{p1} \cdot C_{p2} \cdot C_{p3}$$

Etc.

The implementation is straightforward. The *enable* lines on two 9502 gates are used to expand the gates to 5-input gates. C_{P2} is required as an input to both gates anyway. The extra input to the gate generating C_3 is redundant, but again allows the enable to function as a fifth input to the other gate in the package.

An adder for a longer word length may be constructed by rippling between 4-bit sections and adding two gate delays for each additional 4-bit section. But adding a second level of carry lookahead would result in a faster adder. This requires generating an additional carry generate and carry propagate output from each 4-bit section and running these into an identical carry lookahead unit.

The ripple adder should be given a closer look before it is discarded. Figure 6 shows a 4-bit ripple adder where the carry propagates through each section in only one gate delay. Every other stage accepts an active LOW carry input and generates an active HIGH carry directly — while each of the remaining stages generates an active LOW carry from an active high carry input. Both the active low and active high carry are still needed to generate the sum, but more gate delays may be used to do this. The ripple adder shown will add two 4-bit numbers in five gate delays, only one delay more than required by the carry lookahead adder.

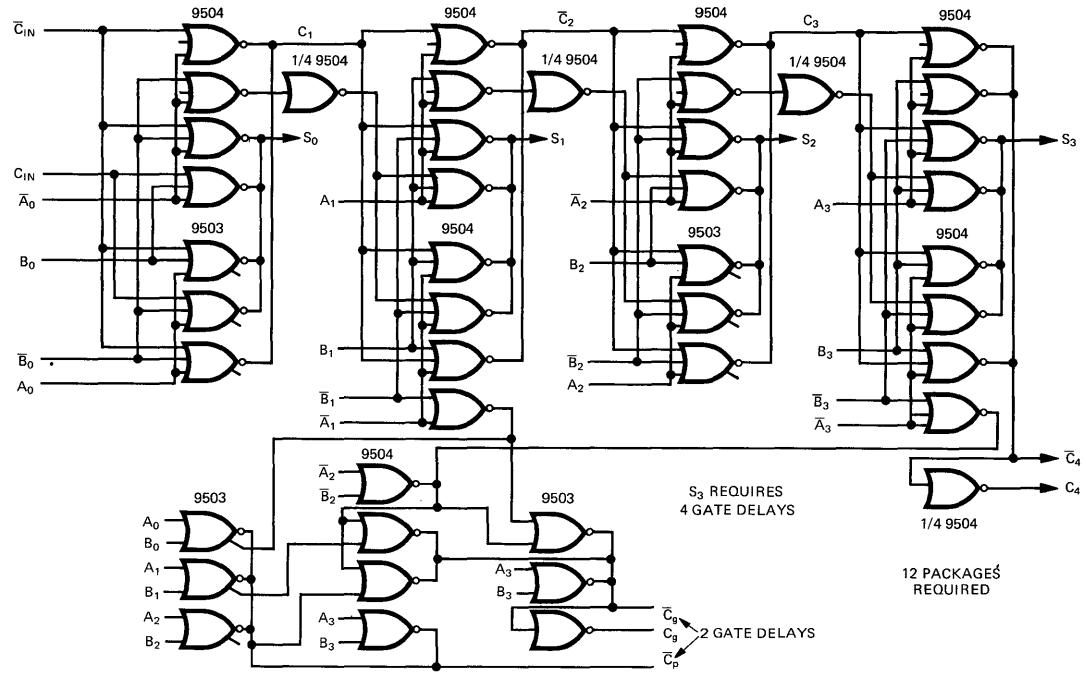
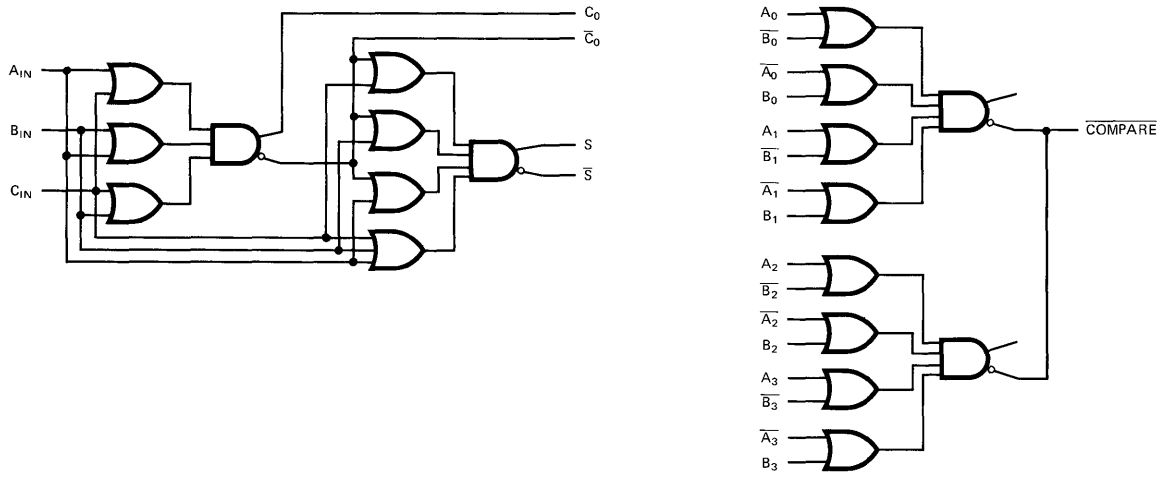


Fig. 6. 4-Bit Ripple Adder with Carry Generate and Carry Propagate Output.



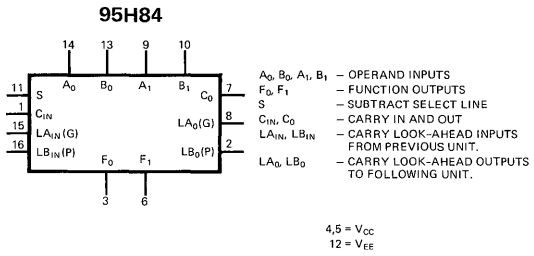
ADDER (a) **COMPARATOR (b)**

Fig. 7.

Carry lookahead may now be used between 4-bit sections. The required carry generate and carry propagate signals are generated by the circuit in Figure 6 in two gate delays. Four of these ripple adders used in conjunction with the lookahead unit in Figure 5B will add two 16-bit numbers in nine gate delays.

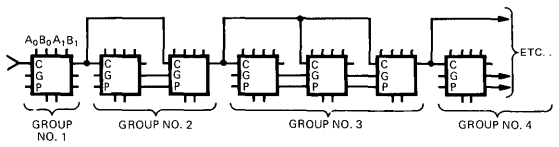
9505 Adder-Comparator

Another adder that can be implemented with two packages uses a pair of 9505s (Figure 7a). This device is recommended whenever one needs to add only 2 or 3 bits together. The 9505 also can be used to construct comparators (Figure 7b).



Add/Subtract

ACTIVE HIGH BLOCK DIAGRAM



GROUP	NUMBER OF BITS	TOTAL NUMBER OF GATE DELAYS	ADD/SUB SPEED AT 2.0 ns PER GATE (TYPICAL)
1	1–2	2	4
2	3–6	5	10
3	7–12	6	12
4	13–20	7	14
5	21–30	8	16
6	31–42	9	18
7	43–56	10	20
8	57–72	11	22

FOR 8 BITS THE CONFIGURATION BELOW ALLOWS A TYPICAL ADD TIME OF 10 ns
ADD ONLY

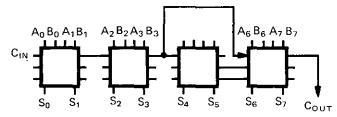


Fig. 8. 95H84 MSI 2-Bit Adder

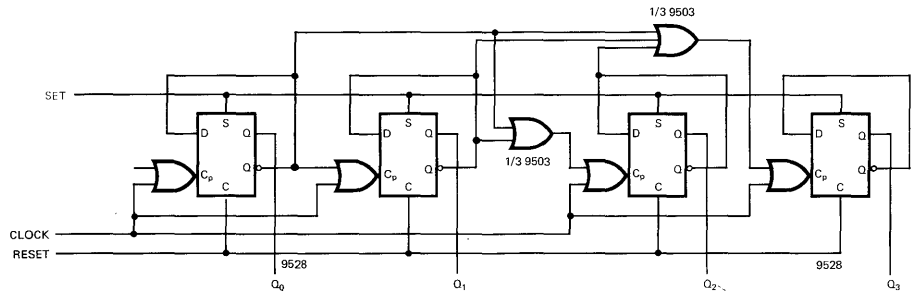


Fig. 9. Synchronous Binary Counter.

95H84 2-Bit Adder-Subtractor

For adding 2-bit words the 95H84 will provide the highest speed combined with minimum package count. As shown in Figure 8, the 95H84 performs both addition and subtraction on two bits with full internal carry lookahead, expandable between units. No additional carry lookahead unit is required. It can be implemented to add or subtract two 64-bit words within 22 ns at a power comparable to a TTL adder with carry lookahead units.

Counters

High-speed counters can be implemented easily with 9528 dual D flip-flops. Figure 9 shows a fully synchronous binary counter. Toggle flip-flops are formed by connecting the D input of each flip-flop to the $\overline{Q}$ output. The first flip-flop must toggle on every clock pulse. By using the two ORed clock inputs as a clock input and an active LOW enable, the second flip-flop is made to toggle on rising clock edges only if the first flip-flop is a ONE ($\overline{Q}$ LOW). Similarly, the third flip-flop only toggles if both $\overline{Q_0}$ and $\overline{Q_1}$ are LOW, etc.

While most high-speed applications require a synchronous counter, a ripple counter will function as well in certain applications and can be implemented with fewer external gates and less clock loading. Figure 10 shows such a counter. The "divide-by-64" (Terminal count) output is as fast as if decoded from a synchronous 64 counter. Only two transitions are of interest: from 011111 (least significant bit) to 111111 (most significant bit) and from this state to 000000. These transitions depend on the first (least significant) bit, and the more significant flip-flops have more than enough time to settle.

The D flip-flop is well suited for use in shift counters. The resulting count sequence is not binary, naturally, but this is of no consequence in many applications.

A shift counter of length 2^n-1 (n = number of stages) is easy to implement as shown in Figure 11. For n = 6 the counter will pass through 63 states by toggling the first flip-flop whenever the last flip-flop is ZERO (Q_5 LOW). The other flip-flops function as normal D flip-flops. As can be seen by examining the count sequence in Figure 11, the one missing state is the persistent 111111 state. A gate is used to reset the first flip-flop if the counter should accidentally enter this state. The reset line, as shown, sets the counter to the 100000 state and thus 000000 becomes the terminal state. This choice is arbitrary.

The feedback used for this shift counter will function properly for the following values of n (numbers of stages) less than 25: n = 2, 3, 4, 6, 7, 15 and 22. Other values require a different feedback arrangement.

The counter may be made to count by 64 (2^n) by modifying the feedback to include the 111111 state as shown in Figure 12.

Figure 13 shows a combination of the synchronous binary and shift counters. Each pair of flip-flops is connected as a count-by-4 shift counter and is permitted to count when all less significant pairs are in the 01 state. The resulting count sequence also is shown.

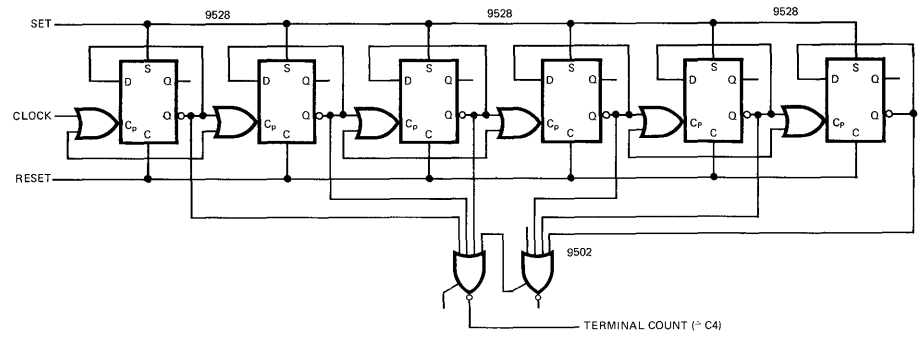
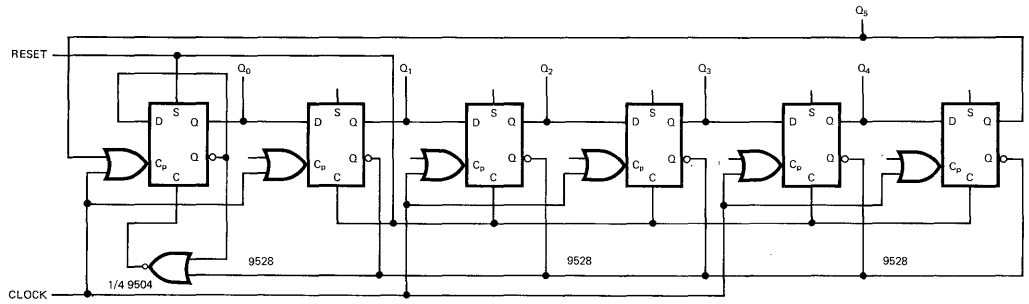


Fig. 10. Divide-by-64 Ripple Counter. (As fast as synchronous counter.)



COUNT SEQUENCE

1 0 0 0 0 0	1 1 0 1 0 0	1 0 1 0 1 1
0 1 0 0 0 0	0 1 1 0 1 0	1 1 0 1 0 1
1 0 1 0 0 0	1 0 1 1 0 1	1 1 1 0 1 0
0 1 0 1 0 0	1 1 0 1 1 0	0 1 1 1 0 1
1 0 1 0 1 0	0 1 1 0 1 1	0 0 1 1 1 0
0 1 0 1 0 1	0 0 1 1 0 1	1 0 0 1 1 1
0 0 1 0 1 0	0 0 0 1 1 0	1 1 0 0 1 1
1 0 0 1 0 1	1 0 0 0 1 1	1 1 1 0 0 1
1 1 0 0 1 0	1 1 0 0 0 1	1 1 1 1 0 0
0 1 1 0 0 1	1 1 1 0 0 0	0 1 1 1 1 0
0 0 1 1 0 0	0 1 1 1 0 0	1 0 1 1 1 1
1 0 0 1 1 0	1 0 1 1 1 0	1 1 0 1 1 1
0 1 0 0 1 1	0 1 0 1 1 1	1 1 1 0 1 1
0 0 1 0 0 1	0 0 1 0 1 1	1 1 1 1 0 1
0 0 0 1 0 0	0 0 0 1 0 1	1 1 1 1 1 0
1 0 0 0 1 0	0 0 0 0 1 0	0 1 1 1 1 1
0 1 0 0 0 1	1 0 0 0 0 1	0 0 1 1 1 1
0 0 1 0 0 0	1 1 0 0 0 0	0 0 0 1 1 1
1 0 0 1 0 0	0 1 1 0 0 0	0 0 0 0 1 1
0 1 0 0 1 0	1 0 1 1 0 0	0 0 0 0 0 1
1 0 1 0 0 1	0 1 0 1 1 0	0 0 0 0 0 0
		1 0 0 0 0 0

Fig. 11. Synchronous 63-Shift Counter.

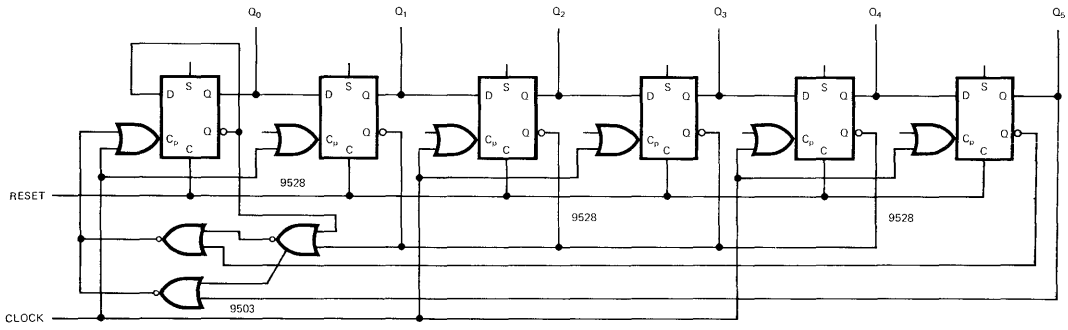


Fig. 12. Synchronous 64-Shift Counter.

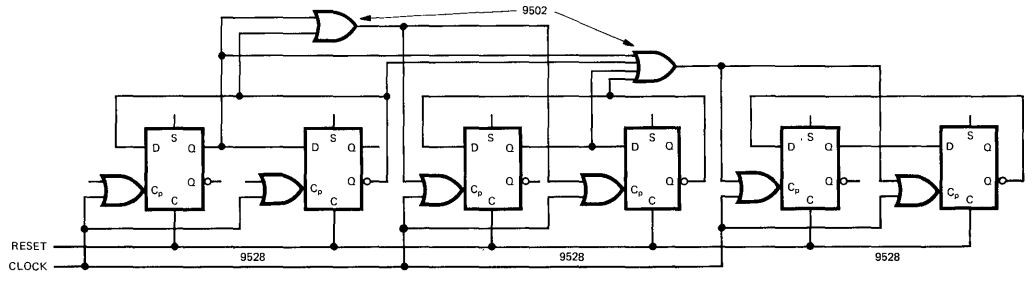
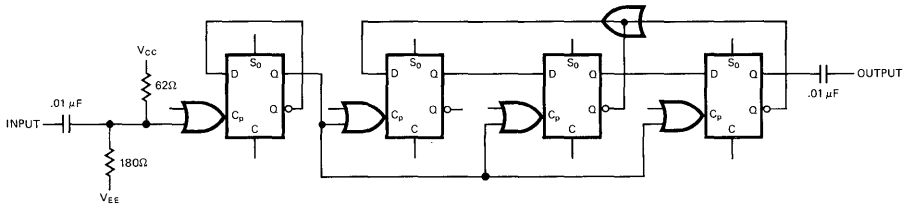


Fig. 13. Synchronous 64-Counter.



High-Speed Prescalers: 9528/95H28

High-Speed Prescalers: 9528/95H28

This easy-to-implement prescaler, Figure 14, has many applications in digital instruments and communications. By using only two integrated circuits the operating range of 10 to 30-MHz counters may be extended well into the VHF range. The prescaler also can be incorporated in digital phase-lock loop systems in communications equipment. The integrated circuits used to build the prescaler shown are 9528/95H28 dual D, temperature-compensated flip-flops.

The circuit will accept AC input voltages from 0.15V RMS to 0.5V RMS. If a greater input range is desired, either an attenuator or preamplifier can be inserted before the 9528's.

The logic configuration of this prescaler is straightforward. It consists of a divide-by-two toggle stage clocking a divide-by-five shift counter. The advantages of this configuration are: an output duty cycle of 60/40 (good for driving slower speed TTL logic), a single flip-flop on the input to reduce the loading of the driving circuitry if desired, and no lockup states.

High-Speed Prescaler: 95H90

The ECL 95H90 prescaler, Figure 15, is a high-speed ECL/MSI element designed specifically for the communication and instrumentation manufacturer. In its simplest use it will divide any clock frequency up to 250 MHz by 10. By using the 95H90 with other control logic a divide by 10/11 logic control element allows a divide by "N" counter to be constructed with a maximum frequency above 250 MHz. Typically maximum clock frequency for the 95H90 is 340 MHz.

By keeping all the high speed logic manipulation "on chip," a dramatic decrease in power and increase in reliability and wireability are made available at much lower cost than that of a comparable SSI function.

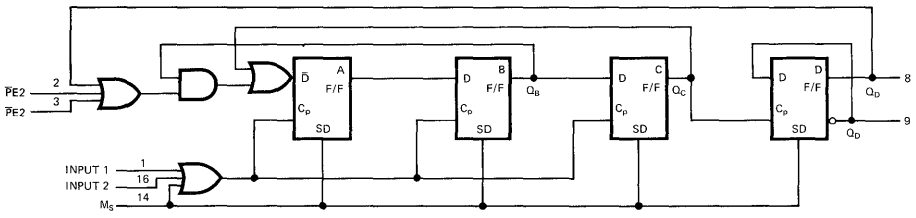


Fig. 15. 95H90 Logic Diagram.

Multiplexers/Decoders

The 9500 ECL product line includes many devices that can be used as multiplexers and demultiplexers or decoders. A simple 2-input multiplexer can be implemented using two (or more) 9504 gates. (Figure 16).

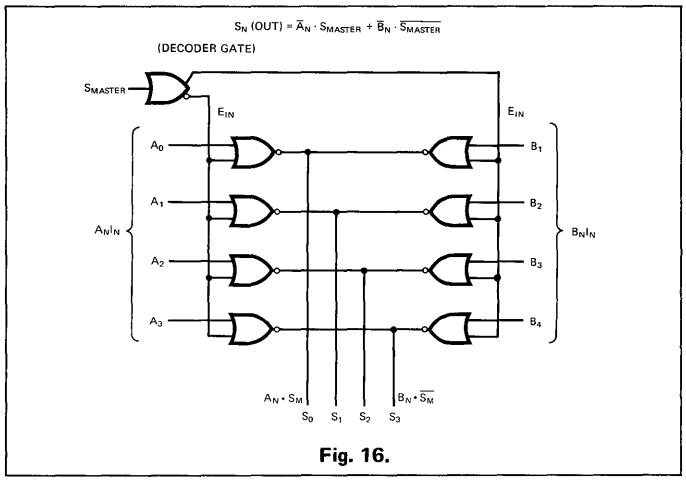


Fig. 16.

This type of multiplexer can be expanded to either of two 16-bit words with more decoders (i.e., 3-input, 4-input, etc.) or more NOR gates.

The MSI equivalent of this logic function is found in the 9579 quad 2-input multiplexer (Figure 17). The advantage of the 9579 over the SSI equivalent is lower power and higher speed, as well as fewer connections.

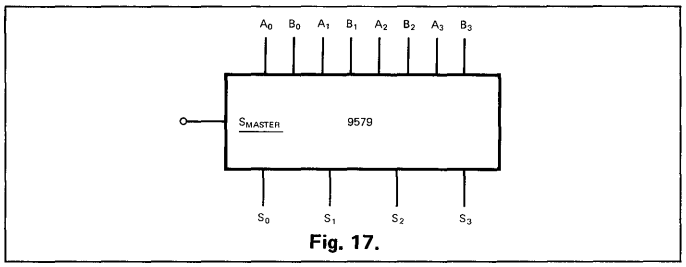


Fig. 17.

A special triple 2-input multiplexer, the 9580 combines several features. These are: 1. separate select on each output, 2. common enable on all outputs, disabling low for OR tying, and 3. inversion through the multiplexer. By using the wired-OR on the inverted outputs, a logical NAND may be obtained. Figure 18 illustrates this with gates in place of multiplexers.

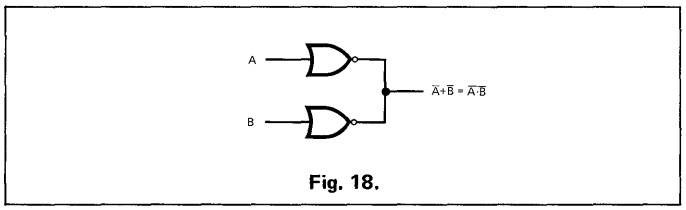
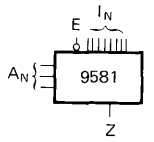


Fig. 18.

8-Input Multiplexer: 9581

The 9581 multiplexer is fundamentally a high-speed semiconductor implementation of a single-pole eight-position switch. Three address lines select one of the eight data inputs and feed this input to output (Z). An active LOW enable input forces the output LOW if held HIGH. Data encounters only one gate delay from one of the eight data inputs to the output. A truth table for the device is given in Figure 19.

The multiplexer also can be used as a universal logic block capable of generating any function of four variables. To generate an arbitrary function of A, B, C and D; three of the variables (A, B and C for example) should be connected to the address input lines A_0, A_1 and A_2. The desired function is achieved by wiring each of the eight data inputs to either a LOW (open input), a HIGH (-.89 volts), the fourth variable (D), or the negation of the fourth variable ($\overline{D}$).

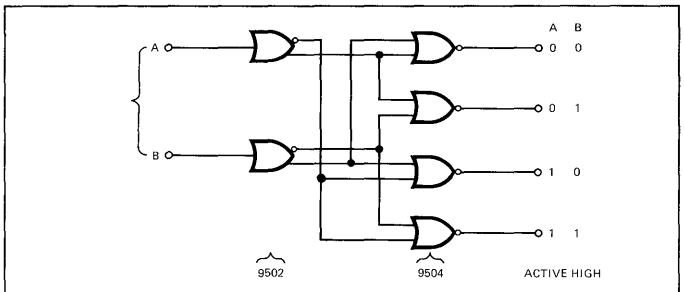


INPUTS												OUTPUT
A_0	A_1	A_2	E	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
H	L	L	L	X	L	X	X	X	X	X	X	L
H	L	L	L	X	H	X	X	X	X	X	X	H
L	H	L	L	X	X	L	X	X	X	X	X	L
L	H	L	L	X	X	H	X	X	X	X	X	H
H	H	L	L	X	X	X	L	X	X	X	X	L
H	H	L	L	X	X	X	H	X	X	X	X	H
L	L	H	L	X	X	X	X	L	X	X	X	L
L	L	H	L	X	X	X	X	H	X	X	X	H
H	L	H	L	X	X	X	X	X	L	X	X	L
H	L	H	L	X	X	X	X	X	H	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	L	X	X	X	X	X	X	H	X	H
H	H	H	L	X	X	X	X	X	X	X	L	L
H	H	H	L	X	X	X	X	X	X	X	H	H
X	X	X	H	X	X	X	X	X	X	X	X	L

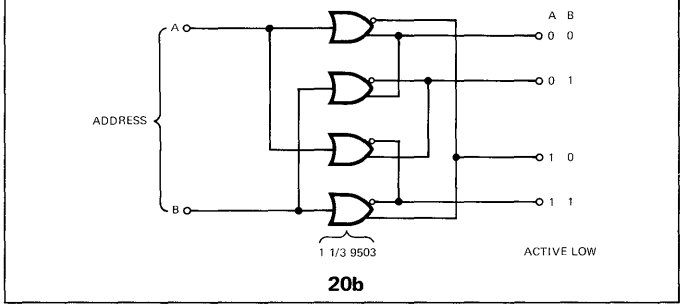
Fig. 19. 9581 Truth Table

Decoding: Using the 9503 and 9504 Gates

For decoding or demultiplexing, the true and complement outputs and the wire-OR features can be used to make a decoder in one gate delay. For example Figure 20a is a 2 to 4-line, active low decoder. If added delay can be tolerated, then the 2 to 4-line, active high decoder of Figure 20b can be used. In 20b the 9504 enable will force all inputs low for OR tying or serve as the "data in" line for demultiplexing.



20a

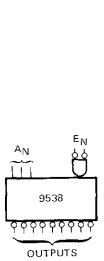


20b

3-Line, 8-Line Decoder: 9538

The 9538 decoder accepts three binary address inputs, and under control of the enables, activates one of the eight active LOW outputs. Both of the active LOW enable input lines must be LOW to enable the outputs. In other words, if either of the enable inputs is HIGH, all eight outputs remain HIGH. A truth table for the decoder is given in Figure 21.

The 9538 decoder can be used as a demultiplexer by connecting a data source to one of the enable inputs. The other enable input will function as a data enable line, while inputs A_0, A_1 and A_2 determine which of the eight output lines the data is fed to. The data will not be inverted through the demultiplexer since both the input and the outputs are active low. The delay through the demultiplexer from either enable input to an output is only two gate delays.



9538 AND TRUTH TABLE

INPUTS					OUTPUTS							
A_0	A_1	A_2	E_1	E_2	0	1	2	3	4	5	6	7
L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	L
X	X	X	H	L	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H

Fig. 21

Exclusive OR, Parity Checking

Using standard OR gates: If both assertion and negation inputs are available, an exclusive-OR may be implemented in only one gate delay, Figure 4.

This function is made available in the 9578 Quad Exclusive-OR gate, Figure 22. An additional feature of this product is the output enable.

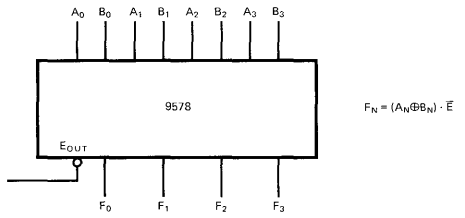


Fig. 22.

With this device a 4-bit comparator is made by OR-tying the four outputs. This output will be low only if $A_N \equiv B_N$, otherwise it is high.

An addressable comparator may be constructed using two or more 9578's and a decoder gate. Figure 23.

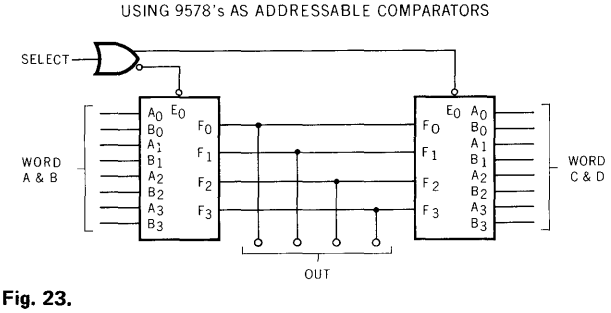


Fig. 23.

For parity checking, several 9578's may be connected together to yield a fast logic block (Figure 24).

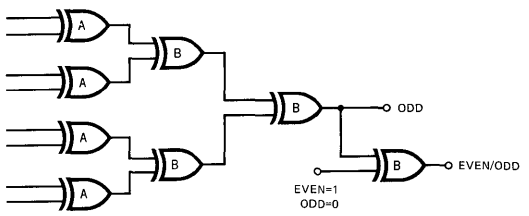


Fig. 24. Parity Checker - 2 9578's

The 9578 will function as an RF Mixer for $F_1 + F_2$ to over 150 MHz. In this application an RF spectrum analyzer will display a text book wave form.

WIRING RULES

General

It is possible to use 9500 in a variety of board constructions ranging from the simple PC or wired board without ground plane to the relatively complex multilayer PC board with ground plane on which all of the connections are terminated transmission lines. 9500 speeds and circuit features have been chosen so that most system manufacturers will find that the system design approach which gives them optimum cost/performance will lie somewhere between these two extremes, where both unterminated and terminated microstrip lines can be used over ground planes. 95H00 speeds are up to 50% faster and must use more restrictive wiring rules. For this reason, double-sided boards with ground planes are recommended for this high-speed logic.

I. Double-Sided PC Or Wired Board *Without Ground Plane*

Although a board with a ground plane gives the most reliable performance, it is possible to operate simple systems on a single board without a ground plane according to the following rules:

(1) Use PC or wired board with maximum size of 3 x 4 inches.

(2) Keep interconnects less than 8 inches total line length. Greater lengths may be used for some applications where increased ringing is tolerable.

(3) Use a common ground line of equal length or shorter than the common data line between interconnecting devices.

(4) Bypass each device at the package. The two V_{CC} pins (4 and 5) are joined together to ground via a 0.02 μF capacitor to V_{EE} (pin 12) at -5.2 V.

(5) Since interconnects must be very short for operation without a ground plane, the radial form interconnection shown in Figure 26a will be most practical.

(6) Minimize interconnections between two or more boards and use a controlled impedance line such as RG-174 50-ohm coax or twisted pair (see Figure 26 for terminations) if any length greater than 8 inches is

encountered. For larger systems of several boards, it is advisable to use ground plane construction.

(7) For distribution of high frequency (such as clock pulses), terminated 50-ohm coax or twisted pair can be used, secured to the board with adhesive or cable ties.

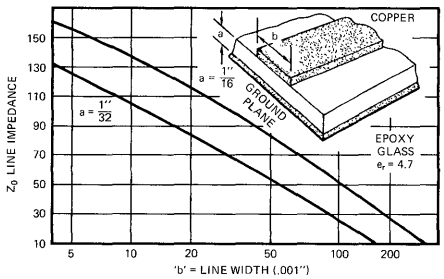


Fig. 25. Characteristic Impedance for Microstrip.

II. Double-Sided PC (Wired) Board *with ⩾60% Ground Plane*

Relatively large systems of 100 or more packages can operate reliably using boards on which a ground plane is plated on one side. With a ground plane present, the conductors on the opposite surface of the board appear electrically as microstrip transmission lines with a specific characteristic impedance Z_0 (typically 85–150 ohms). See Figure 25. Ideally, for minimum reflections, both source resistance R_S and load resistance R_L should each equal Z_0. However, this is not always practical or necessary in a real system where interconnections between source and load are often short enough so that the circuit rise times are longer than the interconnecting line delays. Any reflections are masked in the rising edge of the input waveform and do not seriously affect logic operation. It is on this basis that 9500 rise times of 2.5 to 3.0 ns and on-chip pulldown resistors allow reliable operation with unterminated lines on PC boards of 6 to 8-inch sides. Here interconnections are generally less than 9500 rise times. The following rules will help establish optimum performance for ground plane microstrip unterminated or terminated connections:

Printed circuit interconnections become microstrip transmission lines when backed up by a ground plane. Thus, the standard equations describing transmission line behavior apply. This means a characteristic impedance can be associated with a line, and reflections will occur unless the line is terminated in this impedance. Typical microstrip transmission lines have a characteristic impedance between 50 and 150 ohms. It can be calculated by the following equation developed by H. R. Kaupp ("Characteristics of Microstrip Transmission Lines," IEEE transactions on Electronic Computers, Vol. EC-16, No. 2, April 1967, pp. 185-193):

$$Z_0 = \frac{87}{\sqrt{E_r + 1.41}} \times \ln \frac{5.98\,h}{0.8w + t}$$

where Z_0 = Characteristic Impedance
E_r = Dielectric Constant (4.7 for epoxy-glass)
(4.5 for phenolic-glass)
w = Width of line
t = Thickness of line
h = Thickness of dielectric

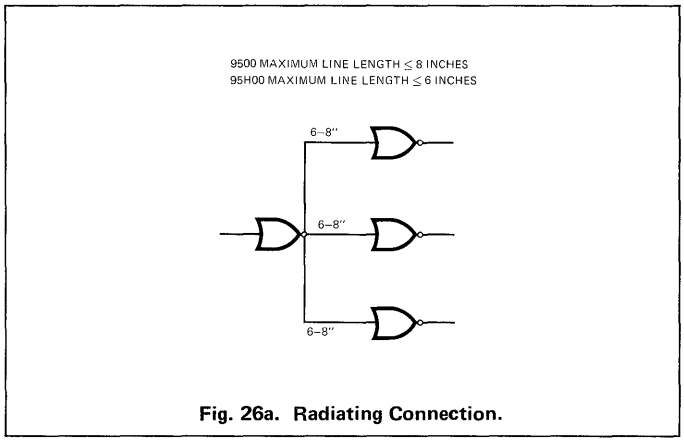


Fig. 26a. Radiating Connection.

This type of connection is preferable for unterminated lines and should be kept short (1-2 inches) for minimum inductive effects. For terminated inputs the maximum fan-out current must not be exceeded.

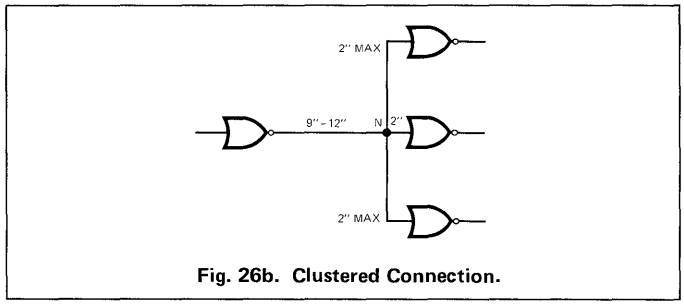


Fig. 26b. Clustered Connection.

This type of connection can be used with or without terminated lines. For terminated lines it is preferable to keep the lines from node N to each input equal in length, very short and terminated at N. Distributed connections should be used if the lines from node N to input exceed one inch.

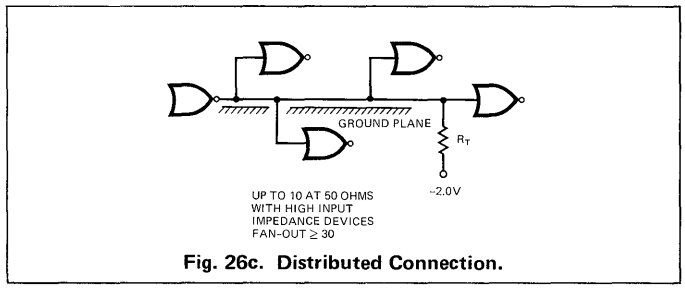


Fig. 26c. Distributed Connection.

This type of connection is preferred for long terminated lines such as clock runs. Termination should be made at the last input. For unterminated connections, the input nearest the source will be slowest in operation because of multiple reflections from the other loads. This is especially true when line length approaches the 8-inch limit of unterminated connections.

(1) Unterminated Load Distribution

In general, any connection arrangements can be used within the maximum unterminated D.C. fan-out of 20, providing all connections are no more than eight inches from source to load and the propagation delay is within the rise times of 9500. The shorter the interconnections, the less the probability of undesirable effects such as ringing and crosstalk. For 95H00, unterminated connections must be less than 5 inches from the source.

It may be possible to use up to 12 inches on unterminated line (8 inches with 95H00) with clustered loads with no undesirable effects. Wire ORing can always be carried out providing sources are less than 2 inches apart. Otherwise, logic timing must be considered. Each OR input appears as one logic load to the other outputs. *If critical timing paths are encountered, the simple single resistor terminated to -5.2 V (the technique shown in Figure 27a) will provide optimum speed.* The value of this resistor should be selected to load the outputs with a total D.C. current of 30 mA. Other resistors on gate inputs and outputs must be considered to prevent exceeding the 40 mA maximum current rating.

(2) Terminated Load Distribution

For distribution of high-speed signals such as clock pulses, where minimum delays are required or where intolerable reflections are incurred in interconnections that are more than 8 inches (5 inches with 95H00), it is desirable to terminate the microstrip line in its equivalent impedance. *Figure 27b* shows the various forms of interconnection that can be used on terminated lines with more than one input. The Data Buss interconnection method should be used for more complicated arrangements where more than one data source is present and large areas of data distribution are required. (Figure 29.)

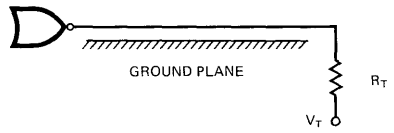
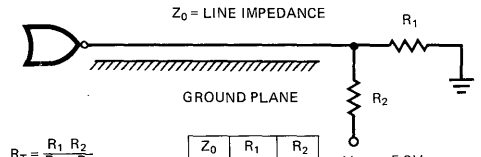


Fig. 27a. Single-Resistor Termination.

This enables the use of a single resistor terminated to -2V. For some applications for up to a fan-out of 5, a single resistor to V_{EE} may be used. The maximum fan-out current should not be exceeded for the later termination. In this case, a typical application would be in terminating a distributed load clock run of 6 to 12 inches.



Z_0	R_1	R_2
50	80	130
75	120	195
100	160	260
R	1.6R	2.6R

Fig. 27b. Two-Resistor Termination.

This avoids bringing -2V onto the board. *NOTE* that as fan-out increases beyond 4 at the end of line, as in *Figure 27b,* the paralleling of the internal 2-kilohm pulldown resistor at each input required that R_2 be increased to maintain correct termination. For example, FO = 6, Zo = 100, then R_1 = 160, R_2 = 1.17 kilohms.

System fan-outs of more than 4 at the end of a terminated line are uncommon. If a higher number of clustered loads at the end of a terminated line is desired, the lowest line impedance (m 50) should be used and the correct R_2 calculated.

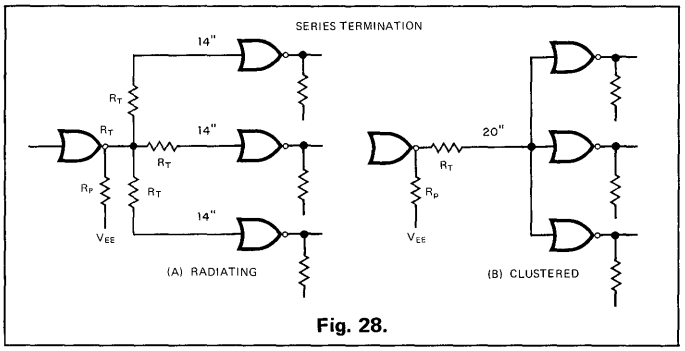


Fig. 28.

(3) Series Termination

Series termination can be used with the high input impedance 95L00 devices whenever lines longer than 8 inches are needed and it is undesirable to terminate the load ends of each line. The technique shown in Figure 28a allows radiating type connections up to 14 inches on each leg. In Figure 28b connections over 20 inches can be used. In this case, a reflection will occur from the gate load but will be absorbed by the series termination resistor at the source.*

A good rule for calculating the value of the series terminating resistor (R_T) is to subtract 5 ohms from the loaded transmission line impedance. For example, a 75-ohm line, minus 5 ohms, yields a series termination resistor value of 70 ohms. A standard value resistor (68 ohms) would be close enough. For a 50-ohm line, a 43-ohm standard resistor is a good choice.

The value of the pulldown resistor (R_P) should be a minimum of 150 ohms, but can be optimized around other values, depending upon the desired speed, power or fan-out. Driving a 50-ohm transmission line (series terminated with 40 ohms) with an 0.85-volt logic swing requires a surge current capacity of 8.8 mA. This requirement is met with an R_P of 500 ohms to V_{EE}.

Better speeds can be obtained when driving three 50-ohm, series-terminated lines with an R_P of 1/2 to 1/3 the 510-ohm value. But the additional decrease in fall time speed may present more problems, such as ringing.

Generally, the series termination speed will be slower than the shunt. This is caused by degradation of the rise and fall times with the series resistor and the capacitive load. But series termination allows the use of radiating type lines to drive several locations on back panels, as opposed to shunt type terminations which would require additional gate outputs. For certain types of connections this additional wiring advantage offsets the slower speed.

***NOTE:** This technique should not be used to drive low input impedance 9500 or 95H00 devices. The additional pulldown current of the 2-kilohm input resistor will lower the noise margin by 100 to 300 mV, which is totally unacceptable.

(4) Data Buss Termination (Wired OR)

This kind of interconnection is usually required when data must be distributed over a large area to a number of loads. These loads may stem from two or more sources

that are located in different parts of the system, such as between boards. Care should be taken in logic timing to ensure that sources are not activated simultaneously. Since a system malfunction results when any load receives both source data outputs at odd time intervals, due to line delays, the following precautions must be taken:

(a) ORed connections may always be made within 2 inches of each other. For any greater distance, differences in logic timing must be considered but may be placed anywhere on the line. Each OR output is effectively one gate load. When using high input impedance 95L00 devices, wire ORing greater than 30 is possible with slight speed degradation (1.5-3.0).

(b) If the distance between any of the sources and either end of the line is greater than 8 inches (5 inches with 95H00), the line must be terminated at the more distant end. If both ends are at least 8 inches from any source, both ends must be terminated as shown in Figure 29. For this double termination, the interconnecting line impedance should be as high as is practical (e.g., 100 to 150 ohms), since each source will be driving into an equivalent load of half the line impedance. If a 50-ohm line has a double termination, it is possible to provide increased drive by paralleling two adjacent gates in a single package. Because of current hogging conditions between sources, however, maximum fan-out should be limited to 30 standard gates for single terminations or to 15 for double 50-ohm (i.e., 25-ohm) terminations. Generally, the high input impedance devices should be used for double termination schemes.

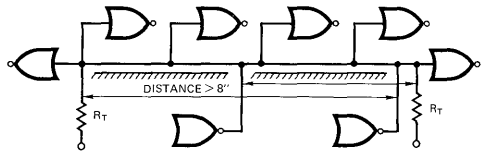


Fig. 29. Data Buss Termination.

If both ends are at least 8 inches from any source, the line requires double termination for best performance.

(5) Decoupling

A minimum of one small (0.01 μF) ceramic capacitor should be used for every five to ten packages, and at least one large (2-20 μF) tantalum capacitor per board should be used between V_{EE} and ground (V_{CC}). Capacitors should be used liberally around the highest frequency components, such as flip-flops. When using boards with large areas of ground and power planes, then the 0.01 μF ceramic capacitor can be reduced in value or eliminated.

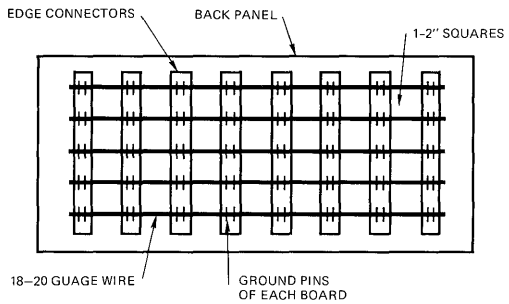


Fig. 30. Backpanel Ground Screen.

(6) Back Panel Wiring (Figure 30)

A ground screen can be constructed on the back panel of the system that interconnects with the board ground planes. This will provide an adequate screen for any data line passing over it between boards. The terminated line arrangements should be used as described above in the paragraph on terminated load distribution.

(7) Line Driving

The two basic modes most commonly used for line driving are differential and single-ended. The differential mode is generally superior to the single-ended mode in terms of noise immunity. Both coaxial cable and twisted pair can be used in these modes, with coax providing superior performance at greater expense.

(a) Coaxial Cable

For differential driving, Figure 31a shows a method of termination which must use coax of 75 ohms or higher with 9500 circuits to avoid exceeding the maximum current ratings. Differential drive through 2 coax lines will yield the highest possible speed with maximum noise rejection. In this mode each coax is terminated in its characteristic impedance to -2V, as if it were used in the single-ended mode.

The single-ended mode is shown in Figure 31b. It can use 50 or 75 ohms with appropriate termination. Over 10 feet of 50-ohm or 75-ohm cable may be driven without serious attenuation.

(b) Twisted Pair

Figures 31c and 31d show differential and single-ended modes respectively for twisted pair cable. Up to about 20 feet can be driven without serious attenuation.

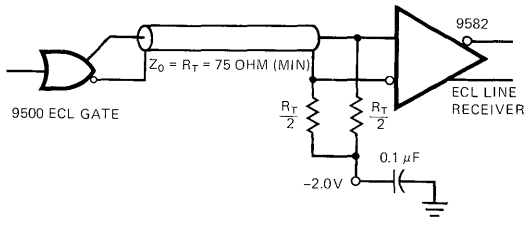


Fig. 31a. Differential Transmission Coax.

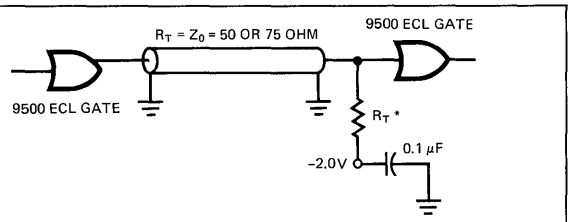


Fig. 31b. Single-Ended Transmission Coax.

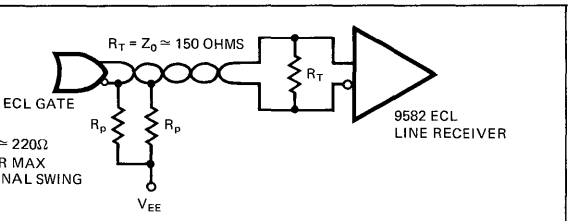


Fig. 31c. Differential Transmission Twisted Pair.

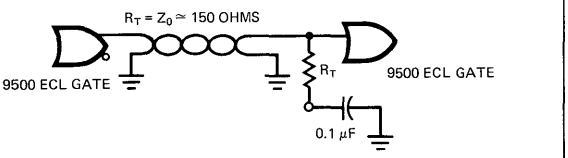


Fig. 31d. Single Ended Transmission Twisted Pair.

NOISE CONSIDERATIONS

Noise is classified under two categories of unwanted signals:
(a) Externally generated noise
(b) Internally generated noise

I. External Noise

This is due to external influences in the system such as motors, fluorescent lighting or power lines. External noise can best be attenuated by standard means of good cabinet design and power line filtering. A full description of this kind of noise is beyond the scope of this discussion. The design of 9500 ECL maintains a constant noise margin sufficient to prevent false logic levels caused by external noise. The percent noise margin of 9500 is at least as good as that of standard TTL logic, and the low impedance lines associated with ECL are generally immune to RF noise.

II. Internal Noise

Internal noise is attributable to the operation of the system itself. For convenience these types of noise are classified as follows:

(1) Reflections and Ringing
(2) Crosstalk
(3) Power Distribution

By allocating connector pins spaced above ground and connected both internally to the board ground plane and externally to the cross wires, an effective ground screen is formed. Data wires passing directly over the screen form transmission lines (Zo $\simeq$ 150 ohms) and can be treated as such. Values of Zo can vary ±50% or more. If excessive, ringing and reflections can be limited by ferrite beads slipped over data wires near the connector pins.

(1) Reflections and Ringing

The conditions which cause reflections or ringing can best be shown by this example:

Line Delay Greater Than Half Rise Time
$T_D > 0.5\ t_r$ (Figure 32a).

This diagram shows the unterminated line conditions under which large reflections can occur. If the design rules for terminated lines are followed, however, extreme amplitudes of greater than 20% logic swing should seldom be encountered. For the majority of such interconnections, the amplitude will be 5% or less, even for a relatively poor termination. Generally, the undershoot of a reflected wave front is a greater problem than overshoot, since undershoot causes temporary reduction in noise immunity as the waveform excursion approaches the logic threshold. A 20% reflection represents a 50% loss of noise immunity for a time as long as the undershoot exists. Overshoot has to be considerable (25% or more) to risk driving the load circuit input transistors into saturation. Therefore, it is not a problem if reasonably good terminations are achieved.

Line Delay = Half Rise Time
$T_D = 0.5\ t_r$ (Figure 32b)

For this condition, in which the electrical delay length of the line approaches that of the circuit rise time, the reflections get closer together and are generally referred to as ringing, since this is how they appear on an oscilloscope. Ringing may be a problem when stretching the unterminated design rule line length to a maximum of 8 inches or more. What constitutes tolerable undershoot or overshoot will be different for various systems. Generally the 20% of logic swing rule of thumb applies.

Line Delay Less Than Half Rise Time
$T_D < .5 t_r$ (Figure 32c)

For this condition, the line appears to be capacitive, rise times are slightly slower and ringing is minimal. Thus, unterminated wiring rules apply, and few noise problems are encountered. The internal pulldown resistors ensure adequate fall times. For lines between 4 and 8 inches, *in cases where speed and timing are critical*, a single resistor to V_{EE} will insure maximum frequency of operation. Maximum output current must not be exceeded (Figure 27a).

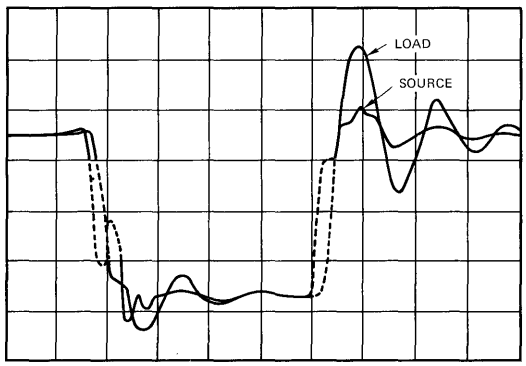


Fig. 32a. Line reflections at $T_D > .5\ t_r$, unterminated line, four gates clustered at 12 inches from source, 10ns/0.2V/cm.

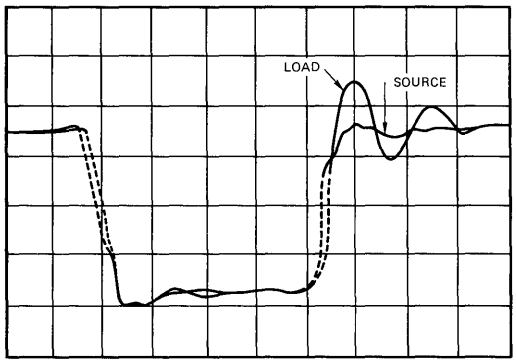
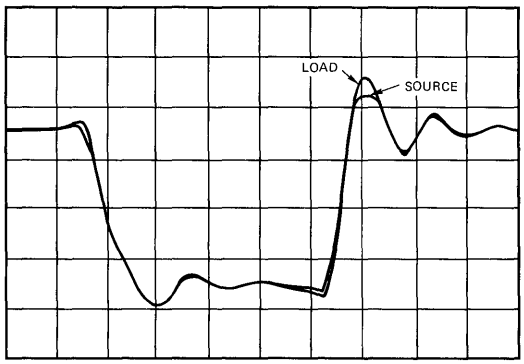


Fig. 32b. Line ringing at $T_D = 0.5\ t_r$, unterminated, four gates clustered at 8 inches from source, 10ns/0.2V/cm.



***T_D = Propagation Delay of Line, t_r = Pulse Rise Time.**

Fig. 32c. Line Ringing at $T_D < .5\ t_r$, unterminated, three gates radiating on 2-inch stubs, 5ns/0.2V/cm.

(2) Crosstalk

Crosstalk is the unwanted coupling of one signal path to another by mutual capacitance or inductance. Because of the high frequencies involved, the following nominal amount of care in board layout should be observed:

Keep adjacent data paths no less than one board thickness or one line thickness apart, whichever is greater.

Do not allow more than 2 to 6 inches of parallel runs when adjacent data paths are this close.

Generally, the inherent good noise immunity and low impedance of 9500 will minimize crosstalk. Separate V_{CC} ground pins for emitter follower and current switches of each 9500 circuit reduce on-chip crosstalk to a negligible level. A large area of ground plane ensures low crosstalk.

(3) Power Distribution

The following rules should be adopted for safe performance.

(a) Voltage drops on V_{EE} lines between gates should be minimized by using maximum conductor area for current to be carried, or by ring connection around the board.

(b) Connections to ground or ground plane must be as short as possible.

(c) Since 9500 logic levels are a function of supply voltages, supply variations are best kept to ±5%, which is normal for most industrial systems. A significant improvement in system noise immunity can be gained with 9500, especially under worst-case conditions, if power supply variations are kept to ±2% or less. This is because levels are directly controlled by the supply voltages.

(d) Use decoupling capacitors as stated in the wiring rules.

9500 SYSTEM THERMAL CONSIDERATIONS

When 9500 ECL is operated in still air or in unknown air movement, the permissible range of ambient temperature operation is 0°C to 75°C with ±5% power supplies. With ±2% power supplies and a minimum of 500 linear feet per minute airflow, 9500 ECL meets all DC specs from 0°C to +125°C. Above 100°C with ⩾ 500 linear feet per minute airflow, AC performance (T_{PD}) must be derated by 33%.

SPECIAL CLOCK CIRCUITS

General

Crystal oscillators and monostable multivibrators are two types of special circuits often encountered in high-speed digital systems. To use a digital gate as an oscillator, it must be biased into its linear operating region and have a high input impedance (> 2 kΩ). The 9582 line receiver satisfies these conditions.

Fundamental Crystal Oscillator (Figure 33a)

The fundamental crystal oscillator requires no tank circuit. The 9582 serves simply as an amplifier, with the crystal in the series mode functioning as a bandpass filter. C_A is the fine frequency adjustment, but if small variations of frequency are not needed, it can be replaced with a short circuit.

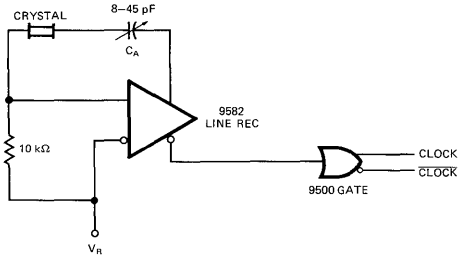


Fig. 33a. Fundamental Crystal Oscillator (1-20 MHz).

Overtone Crystal Oscillator (Figure 33b)

The overtone crystal oscillator employs an adjustable resonant tank circuit which insures operation at the desired crystal overtone.

C_1 and L_1 form the tank circuit, which has a resonant frequency adjustable from 30 MHz to 100 MHz with the values specified.

Overtone operation is accomplished by adjusting the tank circuit frequency to or near the desired frequency. The tank appears to be a shunt to all frequencies except those near resonance. Operation in this manner insures that the oscillator will always start at the correct overtone. C_A is the fine frequency tuning.

With both fundamental and overtone oscillators the gate serves the dual purpose of buffer and wave-shaper. The output of the first 9582, which is approximately a sine wave, is fed into the gate which shapes it into a square wave with rise and fall times of approximately 2.5 ns.

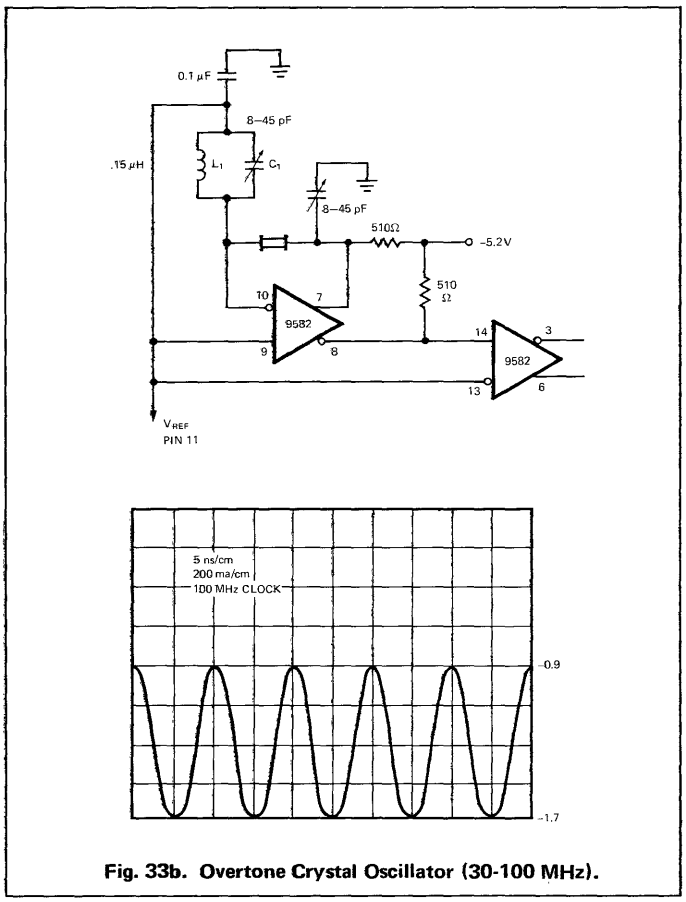


Fig. 33b. Overtone Crystal Oscillator (30-100 MHz).

Clock Restorer/Monostable

The circuit in Figure 34 can be used to restore clock pulses to standard rise and fall times and pulse width. This circuit also can be used to convert a change in logic level from "0" to "1" to a pulse with a well-defined width.

An advantage of this monostable is that the output pulse width is determined solely by delay D. Circuit operation can best be described by following the numbers and events on the circuit.

When the input goes positive (1) the complement output (2) becomes negative. Since the true output (3) had been LOW, the output of the delay line (4) is also LOW. With both inputs into gate 2 LOW, the complement output (5) goes HIGH, removing the control from the input. The input now can assume any state with no effect on the output pulse. The outputs of gate 2 will stay in this state until the logic "1" from the true output of gate 1 (3) arrives at the input of gate 2 (4). At this time gate 2 outputs will change state and control will be restored to the input (1). If the input is still up, it must return to logic "0" for at least "D" ns before the cycle can start again. Should it be at logic "0", at least "D" ns must elapse before it can be recycled.

The delay device used can range from a length of terminated coax or standard delay line to several gates in series. One gate, using its true output, can be used for a minimum pulse width. Caution should be exercised when using this minimal pulse, since it will not have a flat top. It will appear as 1/2 of a sine wave, with its width slightly greater than its rise/fall time.

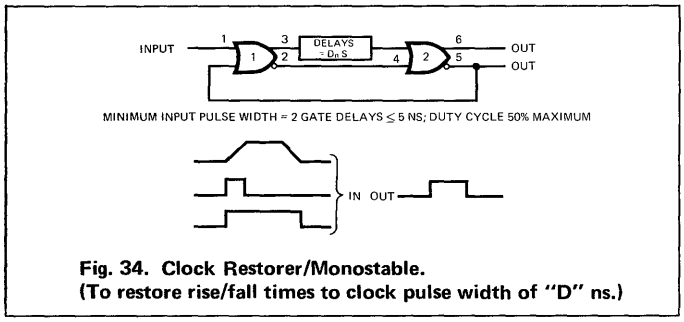


Fig. 34. Clock Restorer/Monostable.
(To restore rise/fall times to clock pulse width of "D" ns.)

LOGIC CONVERSION

General

The 9500 family can be interconnected with other ECL families with little difficulty. Because of superior output level control, and internal pulldown resistors, 9500 can be directly connected to MECL II, III without external components or terminating resistors. Conversion circuits are included for TTL and DTL levels. Generally a fan-out of one is recommended when converting from one circuit family to another. Also, lines into and out of the converter circuits should be short. When interfacing, some circuits will need a reference voltage centered on the 9500 logic swing. This may be derived from any standard 9500 gate simply by returning the complement output to its input with a line of less than 1 ns delay, as shown in Figure 35.

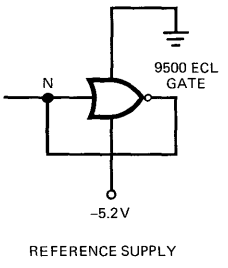


Fig. 35.

Interface Between Motorola MECL II, III 10K, and 9500

Wire directly without any external resistors. Limit fan-out between families to one.

Interface Between Texas Instruments ECL 2500 and 9500

V_{CC} must be common for both circuits. Two separate V_{EE}s are required. Wire directly without any external resistors. Use 9500 gate for TI 2500 reference voltage as shown in Figure 35. Fan-out may be four or more between 9500 and 2500 when operated in this manner.

ECL/TTL INTERFACE

Mixing 9500 series ECL and TTL logic families offers the design engineer a new level of freedom and opens the entire VHF frequency spectrum to the advantages of digital measurement, control and logic operation.

The chief advantages of emitter coupled logic are high speed, flexibility, design versatility and transmission line compatibility. But application and interfacing cost problems have traditionally discouraged the use of ECL in many areas, particularly in low-cost, less sophisticated systems. Using 9500 temperature-compensated ECL with new ECL/TTL interface devices and several new methods of interfacing with all TTL circuits promises to extend the advantages of ECL to many low-cost systems designs.

The interfacing method that may be most practical for smaller systems involves using a common supply of +5 to +5.2 volts. Care must be exercised with both logic families when using this technique to assure proper bypassing of the power supply to prevent any coupling of noise between circuit families. If only a few 9500 ECL packages are designed into a predominantly TTL system, the safest method is to use a 0.01-μF miniature ceramic capacitor across each 9500 device. This value capacitor has the highest Q, or bypassing efficiency. When larger systems are operated on a common supply, separate power busses to each logic family will help prevent problems. Otherwise, good high frequency bypassing techniques usually will be sufficient.

9500 devices are delivered with either high resistance (>20 kilohm) or low resistance (2 kilohm) pulldown resistors at their inputs. The low input resistance ECL devices (basic 9500 series) are generally easier to use. This is because these resistors can replace the costly external pulldown or termination resistors normally required and can improve stability by keeping the input impedance positive real, which eliminates oscillation. When using these Fairchild 9500 devices with short lines (less than 8 inches) no additional external components are needed.

All circuits described will operate with ± 5% ECL and ± 10% TTL power variations, except those with ECL and TTL on a common supply. In those cases a ± 5% supply will assure proper performance.

TTL to ECL

The easiest conversion is from TTL to ECL, and is best done with resistors. An ECL gate should be used as a buffer if high fanout is required. Resistors always will suffice because the amount of signal attenuation is compatible with the required DC offset. Additional factors to be considered are converter circuit delay and drive requirements. Figures 36a and 36b both assume an unloaded TTL gate as the standard TTL source.

The input capacitance of an ECL gate is about 5 pF. With the 2 to 4-ns transition times, this gives a peak input current of 1 to 3 mA. The resistor divider, when calculated to load the driving gate with about 5 mA, will have a delay of only 2 to 3 ns. Since this usually is faster than the TTL rise times, it is normally considered adequate.

If power is to be minimized and extra delay can be tolerated, the current through the converter circuit may be reduced. However, it is important to remember the internal 2-kilohm resistor between the ECL input and V_{EE} when using this type of circuit.

ECL to TTL

When interfacing between high voltage-swing logic such as TTL and low voltage-swing logic such as ECL, the more difficult conversion is from ECL to TTL. This requires a voltage amplifier to build up the 0.8-volt logic swing to a minimum of 2.5 volts. The circuits shown in Figures 36c and 36d or a 9595 may be used to interface from ECL to TTL.

The higher-speed converters usually have the lowest fanout —only one or two TTL gates. This fanout can be increased simply by adding a TTL buffer gate to the output of the converter. Another option, if the ultimate speed is required, is to use additional logic converters.

Fig. 36a.
TTL to ECL,
Separate Power Supplies.

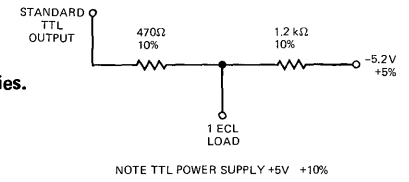


Fig. 36b.
TTL to ECL,
Common Power Supply.

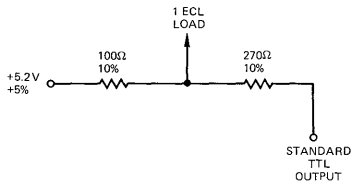


Fig. 36c.
ECL to TTL,
Common Power Supply.

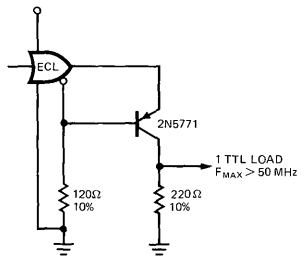
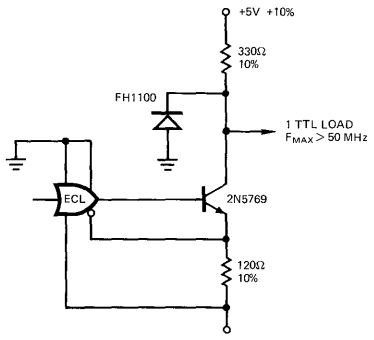


Fig. 36d.
ECL to TTL,
Separate Power Supplies.
Discrete Circuit or
Use 9595 for Dual



CONCLUSION

Very high speed systems can be designed by using 9500 series ECL circuits. The temperature-compensated inputs and outputs and the good noise immunity of 9500 series systems provide reliable operation over a large temperature range. Speed is enhanced by the high speed of the basic gate, the low number of gate delays encountered in MSI circuits and by the relatively few and short interconnections required. The logic flexibility of ECL circuits and the availability of MSI functions permit systems to be implemented with a minimum number of packages, which in turn minimizes the required interconnections.

TEMPERATURE COMPENSATED ECL

THEORETICAL DESIGN

In the past, standard ECL circuits have caused problems in characterization at different temperature levels as well as system noise immunity loss due to temperature gradients. These problems were due to use of the low output impedance emitter follower which enabled the heavy load driving required in system applications. Standard ECL circuit logic levels and threshold are a function of temperature. The logic "1" level is a direct function of high current density V_{BE}. The logic "0" level and threshold are set by the resistors chosen with the bias voltage tracking at one half the logic "1" and logic "0" level temperature deltas.

The primary consideration in this paper is a new circuit shown in Figure 1 which offers temperature invarient levels and internal threshold. The primary advantages of this circuit are an increase in system noise margins due to the loss of temperature gradient effects, an increase in producibility due to the elimination of V_{BE} drifts due to process and hence a tighter control of logic level voltage spreads. The differences with respect to a normal ECL current sourced gate are the addition of two diodes in the bias driver and a network connected between the output device base nodes.

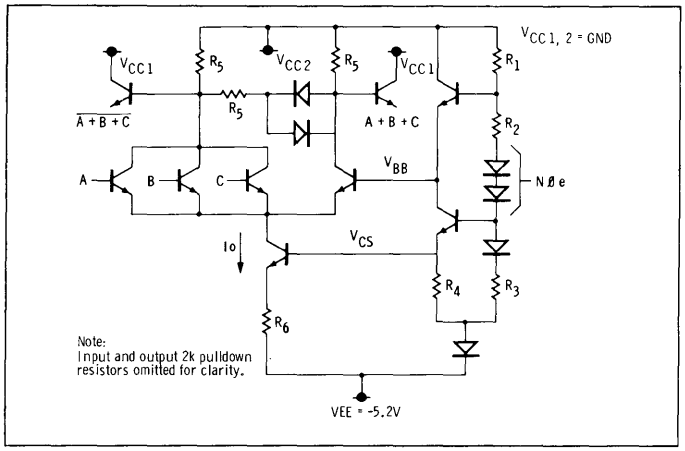


Fig. 1.

Threshold Level V_{BB}

Analysis of the new bias driver network shows that the V_{BB} level (threshold) can be expressed by the following equation.

$$V_{BB} = -\Phi e - \frac{R_1}{R_1+R_2+R_3}\left[|V_{EE}| - (N+2)\,\Phi e\right] \quad (1)$$

$$= -\Phi e\left[1 - \frac{(N+2)\,R_1}{R_1+R_2+R_3}\right] - \frac{R_1\ |V_{EE}|}{R_1+R_2+R_3} \quad (2)$$

N = number of diodes in bias chain at junction of R_2 and R_3

This implies that for V_{BB} to be temperature invarient all the terms involving Φ e (emitter-base forward voltage) must be removed. The result will be dependent solely on V_{EE}, resistor ratio and second order temperature effects.

$$\therefore\ 1 - \frac{(N+2)\,R_1}{R_1+R_2+R_3} = 0 \quad (3)$$

$$N+2 = \frac{R_1+R_2+R_3}{R_1} \quad (4)$$

$$\therefore\ V_{BB} = -\frac{|V_{EE}|}{N+2} \quad (5)$$

Analysis of the output voltages in terms of current source, current I_o results in the following equations, regardless of the input state, for V_H (logic high level) and V_L (logic low level).

Logic Low Level V_L

$$\frac{V_L+\Phi e}{R_5} + \frac{V_L+2\Phi e}{2R_5} = -I_o \quad (6)$$

$$\frac{3}{2}\frac{V_L}{R_5} + \frac{2\Phi e}{R_5} = -I_o \quad (7)$$

$$V_L = -(I_o + \frac{2\Phi e}{R_5})\ \frac{2R_5}{3} \quad (8)$$

$$V_L = -\frac{2R_5 I_o}{3} - \frac{4\Phi e}{3} \quad (9)$$

Logic High Level V_H

$$V_H = \frac{R_5}{2R_5}\left[V_L + 2\Phi e\right] - \Phi e \quad (10)$$

$$= \frac{V_L}{2} + \Phi e - \Phi e \quad (11)$$

$$= \frac{V_L}{2} \quad (12)$$

This implies that if V_H is temperature independent, then V_L must necessarily also be temperature independent. This is critical as the choice of network yielding temperature compensation must work with a single switching current source.

$$\text{Now } I_o = \left[\frac{R_3}{R_1 + R_2 + R_3}\left[|V_{EE}| - (2+N)\Phi e + 2\Phi e - 2\Phi e\right]\right]\frac{1}{R_6} \quad (13)$$

$$= \frac{R_3(|V_{EE}| - (2+N)\Phi e)}{R_6(R_1 + R_2 + R_3)} \quad (14)$$

$$V_L = \frac{-4\Phi e}{3} - \frac{2R_5R_3(|V_{EE}| - (2+N)\Phi e)}{3(R_6)(R_1 + R_2 + R_3)} \quad (15)$$

$$= -\Phi e\left[\frac{4}{3} - \frac{2(N+2)R_5R_3}{3(R_1+R_2+R_3)R_6}\right] - \frac{2R_5R_3|V_{EE}|}{3R_6(R_1+R_2+R_3)} \quad (16)$$

If V_L is to be solely a function of V_{EE} then the terms in Φ must be made equal to zero.

$$\therefore \frac{2R_5R_3}{3(R_1 + R_2 + R_3)R_6} = \frac{4}{3(2+N)} \quad (17)$$

$$\therefore V_L = \frac{-4|V_{EE}|}{3(2+N)} \quad (18)$$

$$\therefore V_H = \frac{V_L}{2} = \frac{-2|V_{EE}|}{3(2+N)} \quad (19)$$

As a result, with selected power supply voltage and operating levels, it is possible to adjust the number of diode drops (N in equations) to yield the required levels. ECL circuits have in general used the −5.2 volt power supply because of market acceptability and the fact that this power supply approaches the minimum which will allow two levels of vertical gating. In addition, V_H for most logic families has been in the −850 mV region for high speed circuits.

$$\therefore -.85 = -\frac{2}{3}\frac{(5.2)}{2+N} \quad (20)$$

$$\therefore (2+N) = \frac{5.2}{.85} \times \frac{2}{3} = \frac{10.4}{2.55} \approx 4 \quad (21)$$

The family of circuits developed by Fairchild uses a total of four diodes in the bias driver to obtain a fully compensated circuit set. The voltage dependence for the logic levels and threshold is shown below.

$$V_H = -\frac{|V_{EE}|}{6} \quad (22)$$

$$V_L = -\frac{|V_{EE}|}{3} \quad (23)$$

$$V_{BB} = -\frac{|V_{EE}|}{4} \quad (24)$$

A comparison of transfer characteristics between temperature compensated and incompensated ECL gates is shown in Figures 2 and 3. An indication of the control of the levels and threshold is given by the transfer characteristic (V_{IN} vs V_{OUT}).

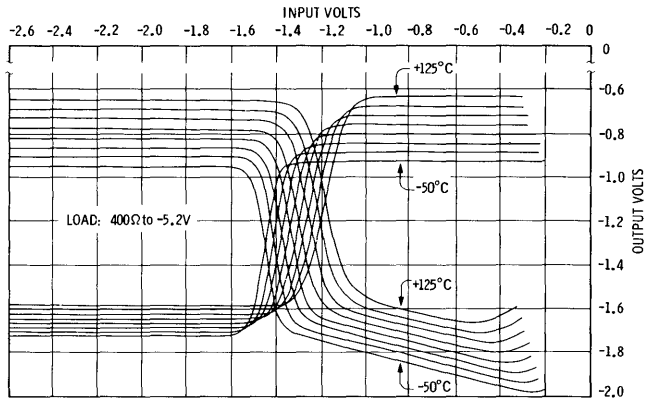


Fig. 2. Transfer characteristics of uncompensated ECL (shown for temperature range −50°C to +125°C in increments of 25°C).

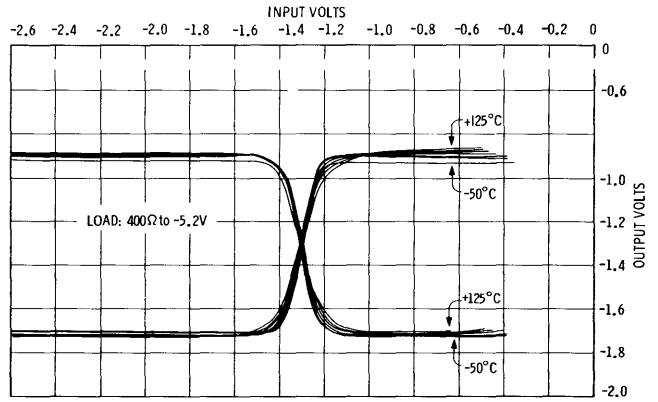


Fig. 3. Transfer characteristics of 9500 temperature compensated ECμL (shown for temperature range −50°C to +125°C in increments of 25°C).

COLD TEMPERATURE OPERATION

It should be noted that at cold temperatures the compensating cross connect network composed of two diodes and a resistor has insufficient forward bias to guarantee current flow. When this occurs, it can be shown that the levels change as a function of temperature and track at the normal V_{BE} rate towards the threshold.

$$V_H = -\Phi e \quad (25)$$

$$V_L = -\Phi e - R_5 I_o \quad (26)$$

$$= -\Phi e \frac{R_5R_3\left[|V_{EE}| - (2+N)\Phi e\right]}{R_6(R_1 + R_2 + R_3)} \quad (27)$$

It has previously been shown (page 2 equation 17) that for the compensation to work, the following equations are true.

$$\frac{R_5R_3}{R_6(R_1 + R_2 + R_3)} = \frac{2}{2+N} \quad N = 2 \text{ (two diodes)} \quad (28)$$

$$\therefore V_L = -\Phi e - 1/2\left[|V_{EE}| - 4\Phi e\right] \quad (29)$$

$$= -\frac{|V_{EE}|}{2} + \Phi e \quad (30)$$

The important consideration now is whether the loss of noise immunity is equal on the logic "1" and logic "0" levels and whether the threshold of the new levels is still $V_{BB} = V_{EE}/4$.

An examination of the new V_H and V_L equations indicates the high level will decrease at the diode temperature tracking

rate and the low level will increase at the diode tracking rate. In addition, if we define $V_{BB} = (V_H + V_L)/2$, then

$$V_{BB} = -\frac{\left[\frac{|V_{EE}|}{2} + \Phi e - \Phi e\right]}{2} \quad (31)$$

$$= -\frac{|V_{EE}|}{4} \quad (32)$$

This guarantees both the normal operating range and the sub zero centigrade region have the same V_{BB} which implies noise immunity will be defined solely by the driving gate's temperature (i. e. fixed if above 0°C ambient decreasing from the fixed value for $T_A < 0°C$). It also guarantees that the input signal will always be centered with respect to V_{BB} resulting in the same gate delays over the entire temperature range (−50°C to 75°C). The loss of signal swing at −50°C is insufficient to increase the unit delays due to the high overdrive situation normally existing in ECL circuits.

SATURATION PERFORMANCE

Another serious consideration for any ECL derived circuit is the performance limiting parameters at high temperature. The most significant parameter here is saturation because saturation at light levels affects the circuit speed by causing storage. Upon gross saturation, the logic levels are adversely affected. Figures 2 and 3 should be reviewed at this time and it will be noted the temperature compensated circuit shows slight level shift due to saturation on both the logic "1" and logic "0" levels. This is caused by the interaction between the low level and the high level due to the diode-resistor cross connect network.

Figure 4 shows both circuits with the indicated voltage movement of both the voltage and temperature. For the sake of comparison, it will be assumed the two circuits are equivalent at one junction temperature (i. e. 25°C T_j). This implies that the logic swings, processing (i. e. V_{BE}'s), and forward bias on the base collector junction would be equal at this temperature. The requirement of equal base-collector bias is reasonable even though the internal collector voltages would be different nominally. The 9500 series gate would have a lower V_H under these conditions, but V_L is also lower by the same amount so for equal signal swings the collector-base junctions would be equally biased.

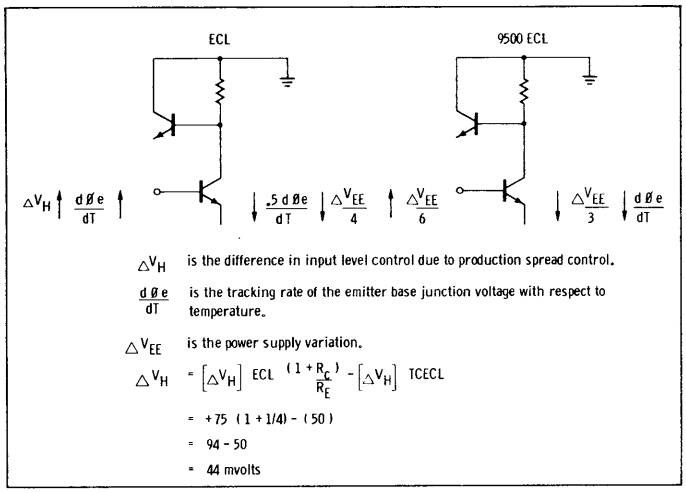


Fig. 4.

If we assume equal power supply control tolerance and worst case movements as shown to accentuate saturation, we could derive an equation relating the 9500 gate temperature increase (T_2) to the ECL gate temperature increase (T_1) in terms of V_{EE}.

$$V_{BC}(T_1) = V_{BC}(T_2) + K_2(T_2 - T_1) \quad (33)$$

$$V_{BC}(T_1) + K_2(T_1) = V_{BC}(T_2) + K_2(T_2) = V_{BCO} \quad (34)$$

where V_{BCO} defines the forward bias which results in a loss of speed due to storage at a fixed temperature (i. e. 25°C T_j). If we let V_{BCN} be the 25°C T_j normal forward bias, then

$$V_{BCN} + \Delta V_{BC}(T_1) + K_2(T_1) = V_{CBN} + \Delta V_{BC}(T_2) + K_2\ T_2 \quad (35)$$

$$\therefore \left[\Delta V_H + 1.5 K_1 T_1 + \frac{\Delta V_{EE}}{4}\right] + K_2(T_1) = K_1(T_2) + \frac{\Delta V_{EE}}{2} + K_2(T_2) \quad (36)$$

$$\Delta V_H + (1.5 K_1 + K_2)(T_1) = (K_1 + K_2)(T_2) + \frac{\Delta V_{EE}}{4} \quad (37)$$

$$(T_2) = \frac{(\Delta V_H - \Delta V_{EE}|4)}{K_1 + K_2} + \frac{(1.5 K_1 + K_2)(T_1)}{K_1 + K_2} \quad (38)$$

For most devices $K_1 \approx 1.5$ mV/°C, $K_2 \approx 2.2$ mV/°C

$$(T_2) = \frac{(\Delta V_H - \Delta V_{EE}|4)}{3.7} + 1.20(T_1) \quad (39)$$

Figure 5 shows the composite curves increase in junction temperature until saturation is reached vs. power supply tolerance for varying saturation temperature rise-of a standard ECL circuit. This type of worst case, considering levels due to production spread, V_{EE} and temperature, usually yields devices that saturate at 75 to 100°C T_j for standard ECL. If we assume a typical 85°C and ± 5% power supplies, it can be seen that this region of operation lies within the area where the temperature compensated 9500 gate would be superior.

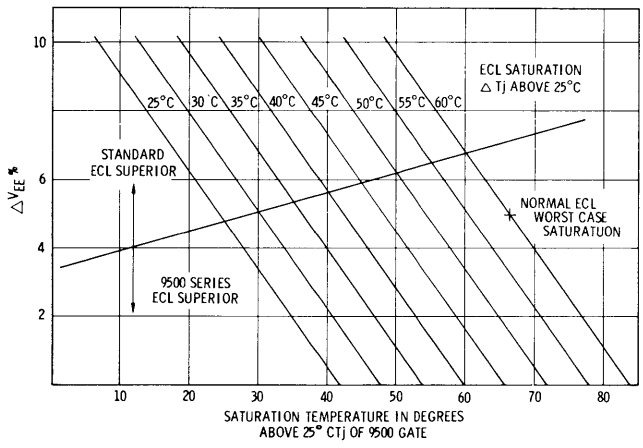


Fig. 5. Saturation comparison of 9500ECμL gates and standard ECL.

Figure 5 also shows that the system designer now has the ability to control his device performance with power supply regulation. 10% − 20% improvements in the saturation temperature at the junction could be obtained by using a 9500 gate and controlling the power supplies to ± 2% regulation or better. The alternate approach with a standard ECL device would be to incorporate a stud-mounted package or other heat sink

design to minimize the junction temperature rise above ambient. System fabricators have increasingly found this latter solution to be cumbersome and expensive when compared to power supply regulation.

It should be noted that no mention of an additional forward bias due to an OR tied output driving the gate was made in this analysis. The addition of this worst case would cause a performance reduction in both gates.

By computing the effect on the ECL gate, the new maximum junction temperature could be computed and the equivalent 9500 gate saturation junction temperature could be located on Figure 5. This is possible due to the analysis looking at ΔT_j from a 25°C T_j where all things were equal. The new V_H resulting from the OR tie would increment the inputs equally on each gate because of the equal output impedance. This additional variable reduces the upper temperature limit for saturation on both products.

SYSTEM NOISE IMMUNITY

System noise immunity is also a function of production spread in levels and threshold, power supply tolerance and system temperature gradients if the levels have a temperature dependence. Unlike the saturation problem which occurs worst case when both gates are hot (driver and receiver), noise immunity is worst for a normal ECL gate when the system temperature gradient between driver and receiver is maximum.

ECL Gate

$$V_H = -\Phi e \ (\pm 75\ mV) \tag{40}$$

$$V_{BB} = -\Phi e - \frac{1}{8}(|V_{EE}| - 2\Phi e)\ (\pm 50\ mV) \tag{41}$$

$$V_L = -\Phi e - \frac{1}{4}(|V_{EE}| - 2\Phi e)\ (\pm 100\ mV) \tag{42}$$

The important thing to notice here is that the logic "1" level has no V_{EE} dependence as the bias driver and V_L do. V_{BB} is centered nominally, but it can be shown that the worst case noise immunity on the logic "0" level is lower than on the logic "1" level. If we define noise immunity as the separation of V_{BB} and V_H or V_L under worst case conditions, equations for the noise immunities can be written. This assumes equal threshold widths for both products, not an unreasonable assumption given the same device geometries and process.

$$V_{N1} = \frac{3}{4}\Phi e(hot) - \Phi e(cold) + \frac{|V_{EE}|(1-n)}{8} - \Delta V_{BB} - \Delta V_H \tag{43}$$

$$V_{N0} = \frac{1}{2}\Phi e(hot) - \frac{3}{4}\Phi e(cold) + \frac{|V_{EE}|(1-3n)}{8} - \Delta V_L - \Delta V_{BB} \tag{44}$$

Assuming a 60°C temperature gradient with a 25°C T_j at cold temperatures, V_{EE} = −5.2 volts ± 5% ΔV_{BB} = ± 50mV, ΔV_H ± 75mV, and ΔV_L ± 100 mV, we could obtain some worst case noise immunities

for Φe = 0.85 volts and K_1 = 1.5 mV/°C

$$V_{N1} = -280 + 617 - 50 - 75 = 212\ mV \tag{45}$$

$$V_{N0} = -257 - 100 - 50 + 552 = 145\ mV \tag{46}$$

Threshold width for an ECL type gate at high current densities is typically 240 mV from unity gain to unity gain point. It would seem that only 20 − 30 mV of practical noise immunity is left on the "0" level and an OR tie still hasn't been considered. An additional problem with this circuit is that logic signals can be skewed because the temperature gradient can cause speed degradation in a large temperature gradient system.

9500 Gate

$$V_H = -|V_{EE}| \tag{47}$$

$$V_{BB} = -\frac{|V_{EE}|}{4} \quad \text{−5.2 volt logic supply} \tag{48}$$

$$V_L = -\frac{|V_{EE}|}{3} \tag{49}$$

$$\therefore V_{N0} = \frac{|V_{EE}|}{12}(1 - 7n) - \Delta V_L - \Delta V_{BB} \tag{50}$$

$$V_{N1} = |V_{EE}|(1 - 5n) - \Delta V_{BB} - \Delta V_H \tag{51}$$

Again using ± 5% power supplies and the production spreads of the compensated gate (ΔV_L = ± 75 mV, ΔV_{BB} = ± 40 mV and ΔV_H = ± 50 mV), some noise margins can be calculated.

$$V_{N1} = \frac{5200}{12}(.75) - 40 - 50 \tag{52}$$

$$= 325 - 90$$

$$= 235\ mV$$

$$V_{N0} = \frac{5200}{12}(.65) - 75 - 40 \tag{53}$$

$$= 282 - 115$$

$$= 167\ mV$$

In both cases the noise immunity is better by 20 mV worst case and additional noise immunity could be obtained with tighter power supply control for the compensated 9500 gate. A standard ECL gate with ΔT_j = 60°C and ΔV_{EE} = ± 2% would have V_{N1} = 231 mV and V_{N0} = 204 mV; the 9500 gate would have V_{N0} = 257 mV and V_{N1} = 300 mV. The equalization of both logic "1" level and logic "0" level noise immunity would require the threshold to be offset 30 mV above the mean of the two nominal levels to obtain optimum performance for both circuits. The effects of OR ties have not been considered in this analysis but a large tie on the driven input does adversely effect both the saturation and the logic "0" level noise immunity.

This comparison illustrates that in systems applications requiring ± 5% power supplies and a 60°C ΔT_j because of package power level difference and system thermal hot spots, the temperature compensated gate is superior in available noise immunity. In addition, it is possible to increase this margin of extra noise immunity by tighter power supply control rather than by thermal equalization as required with standard ECL. The power supply tolerance and ΔT_j are representative of the ECL user's requirements and indeed the large computer houses frequently have better than ± 5% power supply control. If anything, in a system using MSI elements and gates, the ΔT_j would probably be larger than 60°C unless a custom design was made forcing package power levels to be the same. The superior performance of the 9500 gate is then accomplished by shifting the control from thermal to electronic with a resultant increase in saturation junction temperature which also allows higher operating junction temperatures.

APPLICATIONS OF THE 9538

INTRODUCTION

The ECL/MSI 9538 is a 1-out-of-8 ultra high speed decoder designed for use in high performance digital equipment. This device is compatible with all other 9500 ECL elements and offers the same high speed systems design advantages. These include temperature compensation to maintain noise margin across the full operating range, input-output circuits designed to insure freedom from oscillation, and wiring rules to permit the use of low-cost board layout and interconnection techniques (Ref. 1 and 2). The 9538 has applications in memory expansion, register and peripheral selection, serial to parallel conversion in excess of 100 MHz and general high speed decoding functions.

DESCRIPTION

The logic diagram with pin locations for the 9538 decoder is shown in Figure 1. The 9538 accepts three binary address inputs and, under control of the enable lines, activates one of eight active-level LOW outputs. The A_0 terminal of the decoder is considered the least significant so that an input configuration such as $A_0 = 1$, $A_1 = 0$, $A_2 = 0$ would select Output 1 to be LOW. Both of the active-level LOW enable inputs must be low to enable the outputs. If either of the enable inputs is HIGH, all eight outputs remain HIGH. A truth table for the decoder is given in Figure 2.

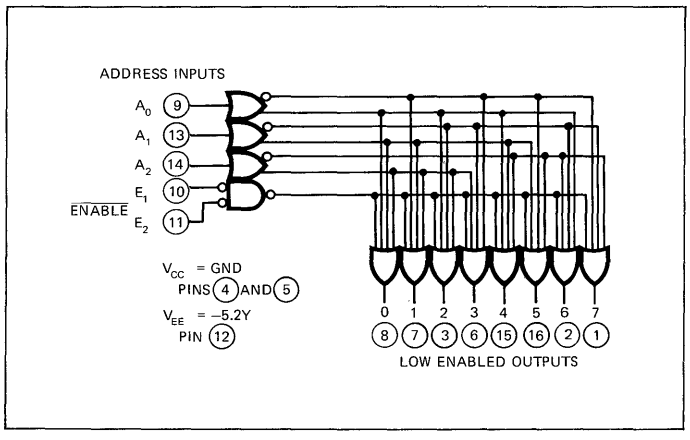


Fig. I. 9538 Logic Diagram

INPUTS					OUTPUTS							
A_0	A_1	A_2	E_1	E_2	0	1	2	3	4	5	6	7
L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H
H	H	L	L	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	L	H	H	H	H	H	L	H	H
L	H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	L	H	H	H	H	H	H	H	L
X	X	X	H	L	H	H	H	H	H	H	H	H
X	X	X	L	H	H	H	H	H	H	H	H	H
X	X	X	H	H	H	H	H	H	H	H	H	H

Fig. 2. 9538 Truth Table

Three levels of series gating are used to implement the 9538 thus providing very high speed — typically 3.5 ns select to output delay, for medium power dissipation — typically 275 mW with a −5.2 volt power supply. All inputs and outputs are terminated in 2kohm resistors. These resistors provide pull-down currents required for extra inputs and outputs OR-tied to the line, insure a positive real Zin over all frequencies, and eliminate the need for external resistors for termination of short lines or on unused inputs. All device outputs are designed to permit driving a 50 ohm coaxial line and a fan-out of 10 unit loads simultaneously, when desired.

APPLICATIONS

The 9538 is an extremely versatile functional building block. The high speed and relatively simple wiring rules make it suitable for use in a wide range of low cost, high speed systems. General applications of MSI decoders are described in other Fairchild publications (Ref. 3 and 4). Some of the more significant uses in high performance systems are summarized on the following pages.

The 9500 family is recommended for use with V_{CC} = ground and V_{EE} = −5.2 volts. However, if suitable decoupling precautions are taken, these devices can be operated in a TTL

system with conventional positive supply rail in association with suitable interface circuits (Ref. 5).

DEMULTIPLEXING

The 9538 decoder may be used as a demultiplexer by connecting a data source to one of the enable inputs. The other enable input will function as a data enable line while inputs A_0, A_1 and A_2 determine which of the eight output lines the data is fed to. The data will not be inverted through the demultiplexer since both the input and outputs are active low.

In the example of Figure 3, with inputs and enable addressed as indicated, the data signal from the source will appear uninverted at output #2.

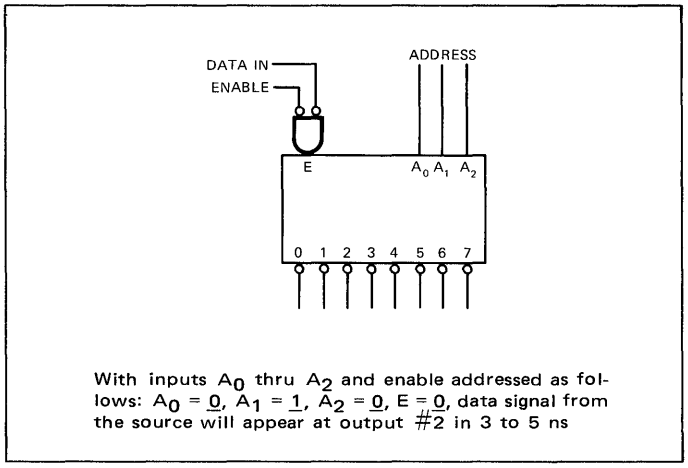


Fig. 3. 9538 as Demultiplexer

Many applications are possible using this principle. Figure 4 shows the decoder serving as a clock demultiplexer. The clock, under control of the address, switches to the appropriate register, counter or memory. For correct operation the clock signal need only be framed by the address inputs with the address set up prior to applying the clock. Up to ten 9500 ECL input loads can be driven by one decoder output.

Utilization of the demultiplexing capability of the 9538 in a serial-parallel conversion application is shown in Figure 5. This configuration also employs the 9581 MSI 8-input multiplexer and 9528 dual-D 150 MHz flip-flop for extremely high speed digital data transmission.

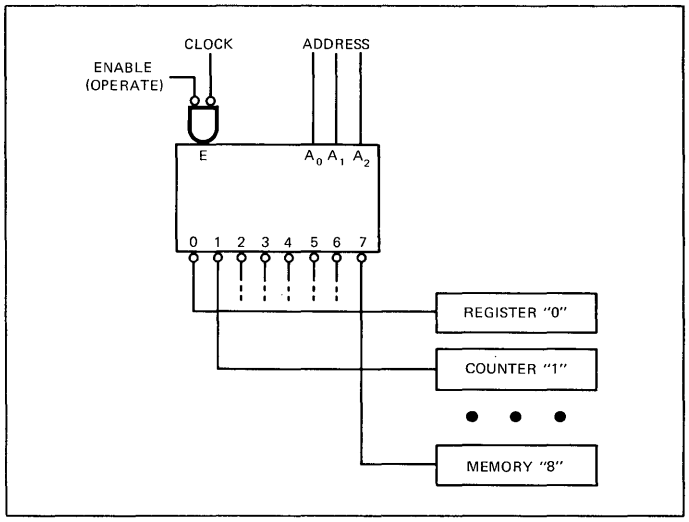


Fig. 4. Clock Demultiplexer

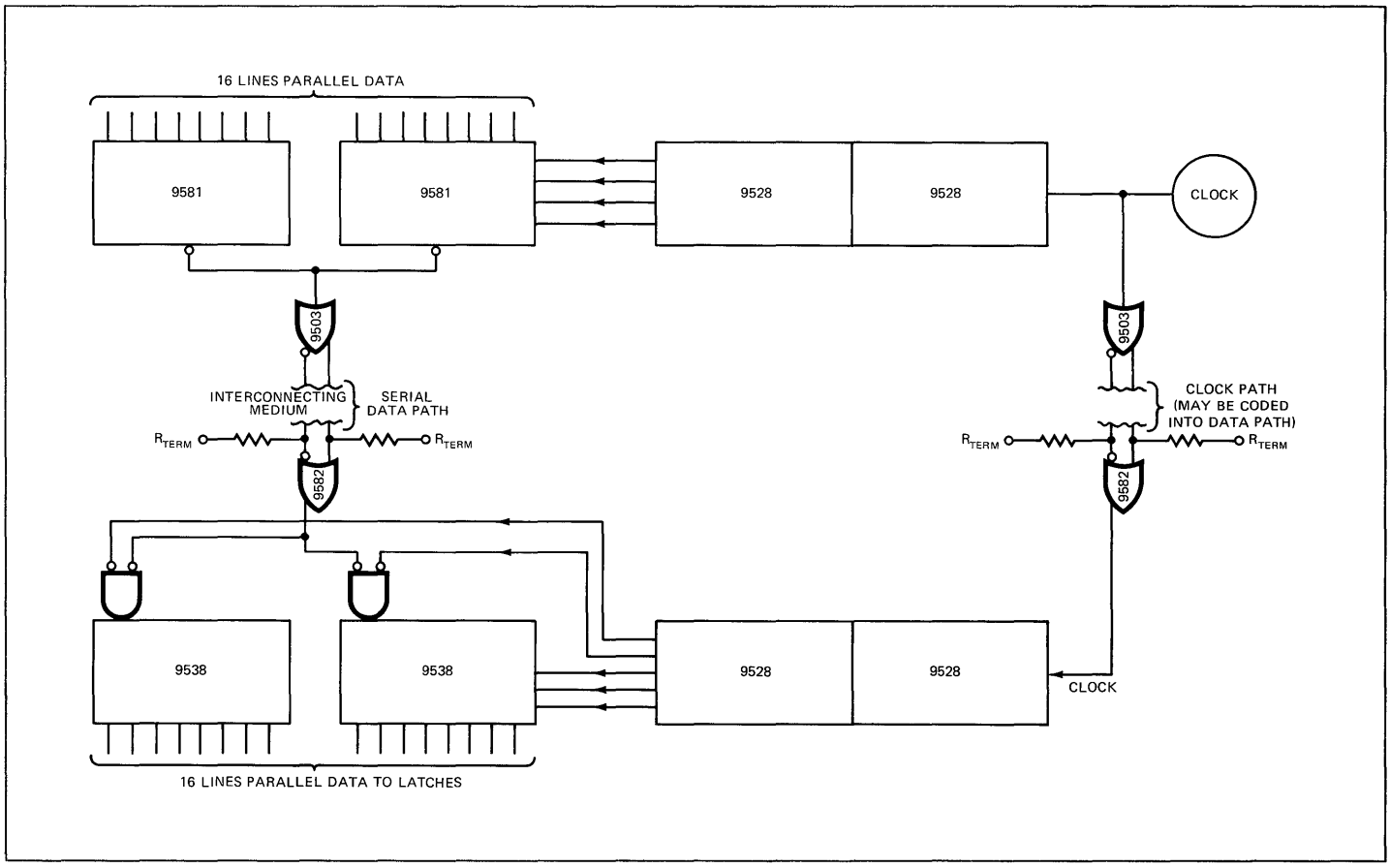
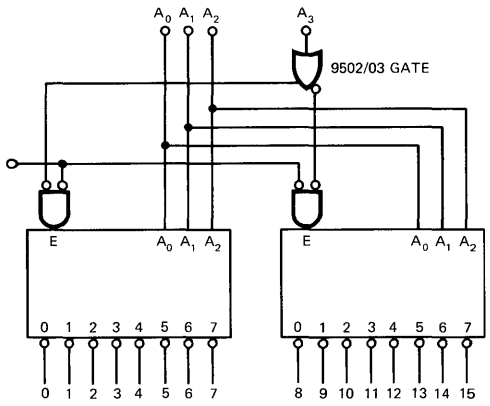


Fig. 5. Serial to Parallel — Parallel to Serial Conversion



	OUTPUT SELECTION				
	BCD CODE				
DECIMAL DIGIT	8421	5421	EXCESS 3	EXCESS 3 GRAY	2421
0	0	0	3	2	0
1	1	1	4	6	1
2	2	2	5	7	2
3	3	3	6	5	3
4	4	4	7	4	4
5	5	8	8	12	11
6	6	9	9	13	12
7	7	10	10	15	13
8	8	11	11	14	14
9	9	12	12	10	15

Fig. 6. Decode Any 4-bit Code

Here 16 channels of data are converted to serial form at a 5-MHz clock rate for transmission at an 80-megabit rate along a single line. The data is converted back to 16-channel parallel form (at the same rate) at the other end of the line. Advantages of temperature compensated ECL over conventional ECL in this application are that any drift in device threshold or output level can result in "glitches" in the decode circuitry. Since these may be interpreted as errors, either the speed or the number of channels must be reduced. With 9500 ECL these variables are eliminated or reduced so that maximum capability is preserved.

CODE DECODING

The enable inputs permit use of two 9538 decoders to decode any four-bit weighted or unweighted code by selecting the appropriate outputs in the required sequence. Figure 6 shows the connection diagram and decode table for this application. The other enable inputs allow enabling of the function. Complete decode operation is completed in 6 – 8 ns.

For decoding of 8421 code in only 3 to 5 ns Figure 7 indicates a lower cost approach using one 9503 Triple 2-input OR/NOR gate package in place of the second 9538 element. The disadvantage of this scheme is the lack of an enable control for the whole function.

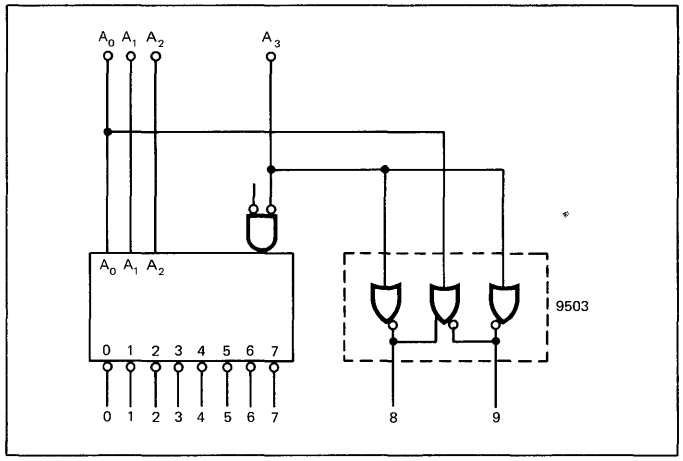


Fig. 7. Higher Speed Decode for 8421 Only

MEMORY DECODING

A major application for the 9538 is in address decoding of high speed memory systems.

The enable inputs allow the use of several 9538 decoders together to decode words of greater than four bits as illustrated in Figure 8. Here four packages are used to select 1 out of 32

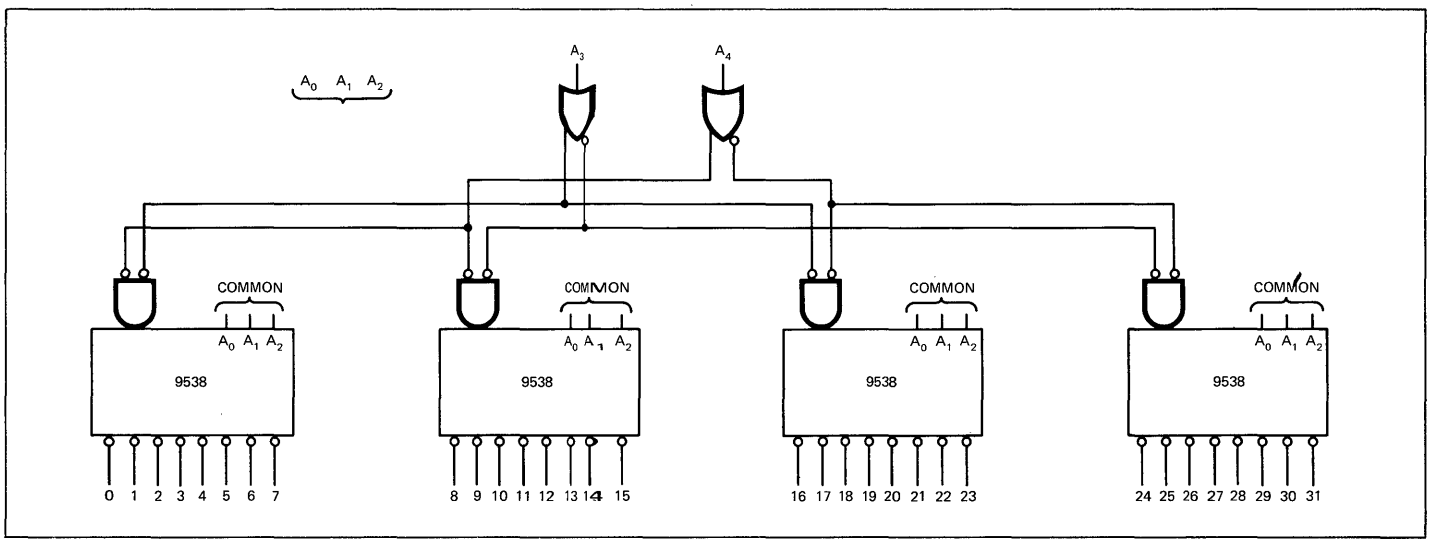


Fig. 8. 1-Out-of-32 Decoder

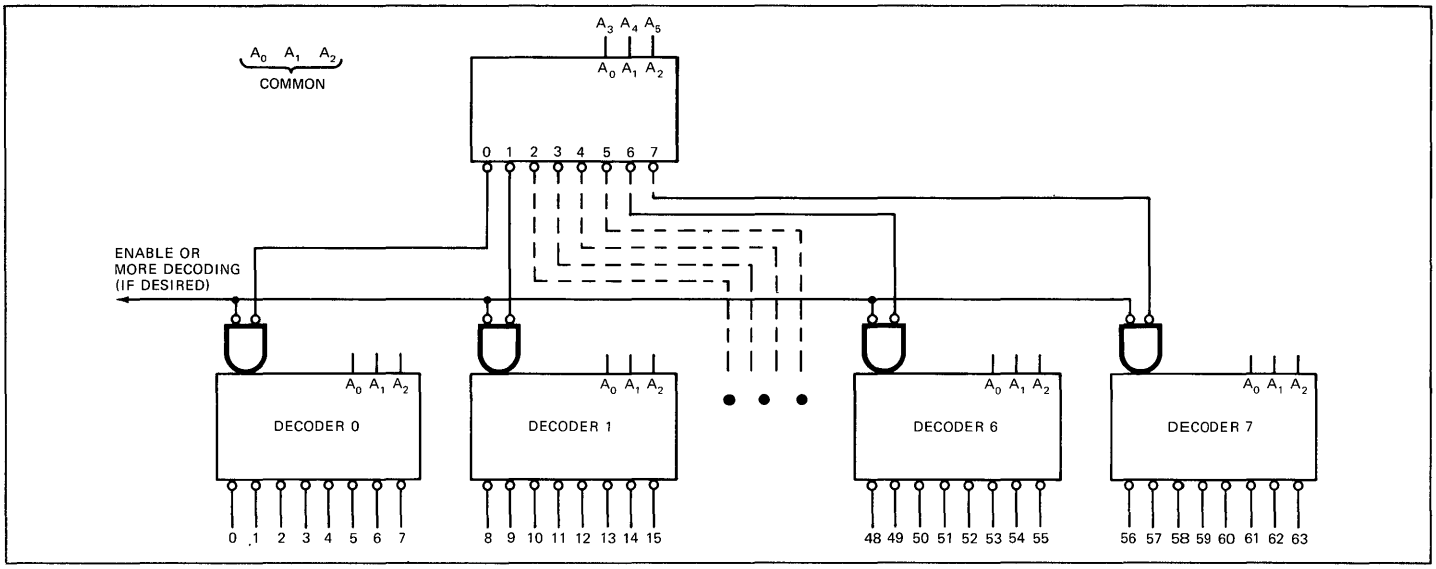


Fig. 9. 1-Out-of-64 Decoder

outputs in 6 – 8 ns from application of the address at inputs A_0 through A_4. This technique may be extended to a six-bit address by using the low output of the 9538 to select one decoder from a group of decoders. Figure 9 shows a 1-of-64 decoding scheme with select propagation delay of 7 to 10 ns. The remaining enable input may be used for overall control or wider decoding if desired.

The low propagation delay of the 9538 makes it particularly useful for high performance ECL semiconductor memory

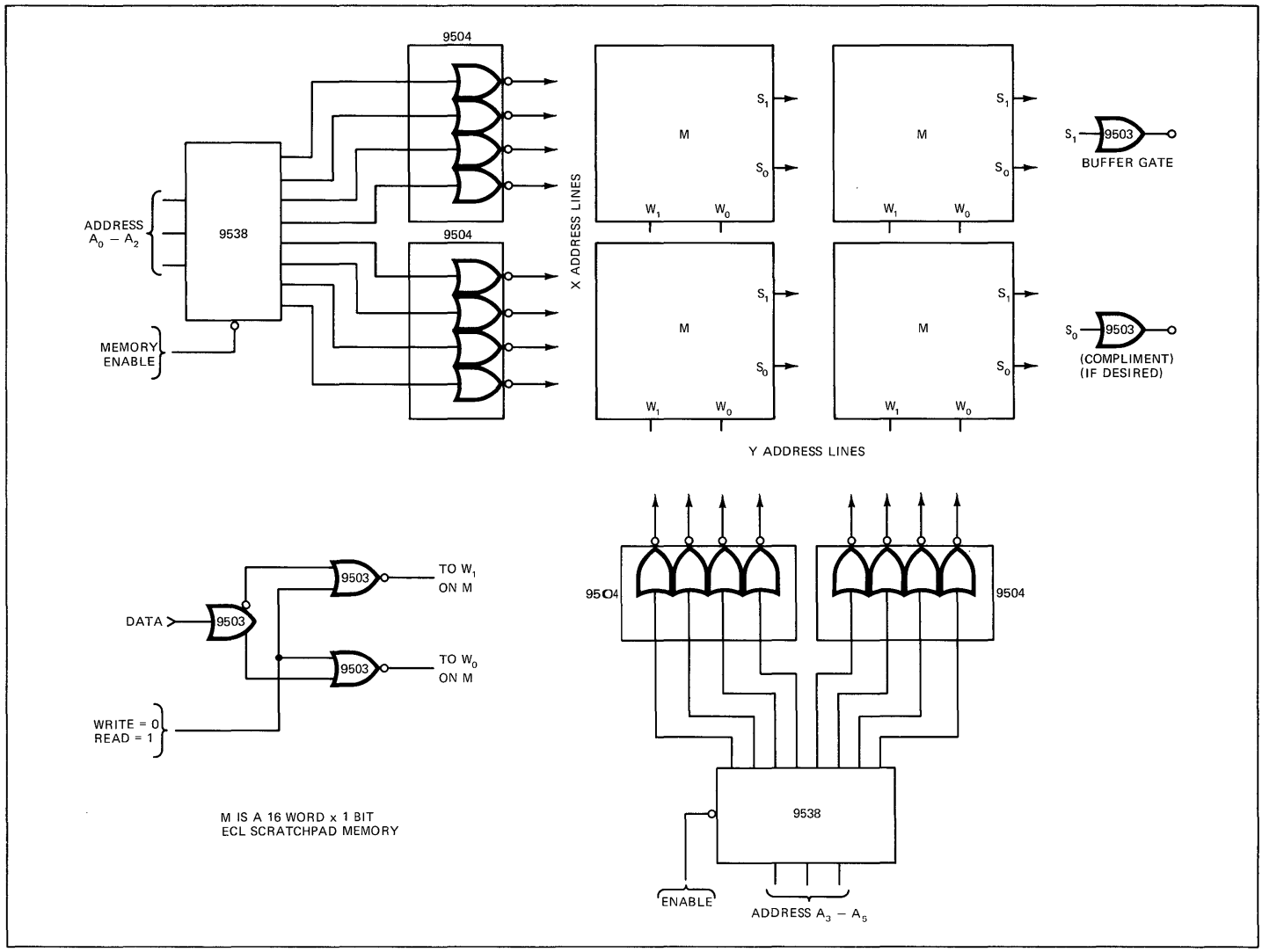


Fig. 10a. Decoding of 64 Word by 1-Bit Memory Array

configurations. Figure 10a shows the 9538 selecting a particular location in a 64-word by 1-bit memory plane constructed from four 16-word by 1-bit ECL scratchpad cells with a linear 4 x 4 x — y select. Each 9538 is connected to two 9504 Quad NOR (with common enable) gates serving as inverter and driver for the X and Y address lines of the memory elements. Wiring and sensing data is achieved with the 9503 Triple OR/NOR gates. Figure 10b shows a 64-word by 6-bit memory based on six of the stacks of Figure 8a. Using a 16-bit ECL scratchpad element with 5 — 6 ns access, the access time of the 64-word by 6-bit system would be typically 12 ns.

This same principle is extended to larger word sizes in Figure 11. Here each clock on the memory plane consists of one stack similar to Figure 10a. The capacity of this configuration is therefore 4K words by 1 bit, with a 20 ns typical access time. Each output of decoders addressed by A_0 through A_2 and A_6 through A_8 fans-out to eight 9504 gate inputs. No termination is required unless interconnecting lines exceed 8 inches. Decoders addressed by A_3 through A_5 and A_9 through A_{11} are connected to the common enable gate input on each

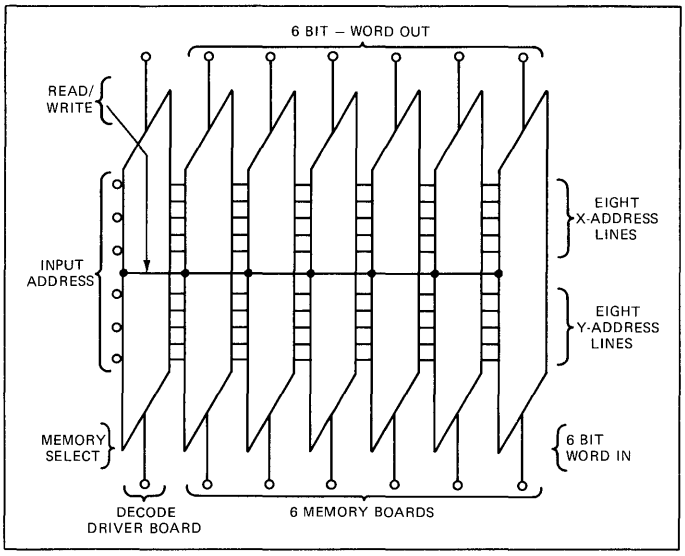


Fig. 10b. 64-Word by 6-Bit High Speed Scratchpad Using Basic Cell of Fig. 10a

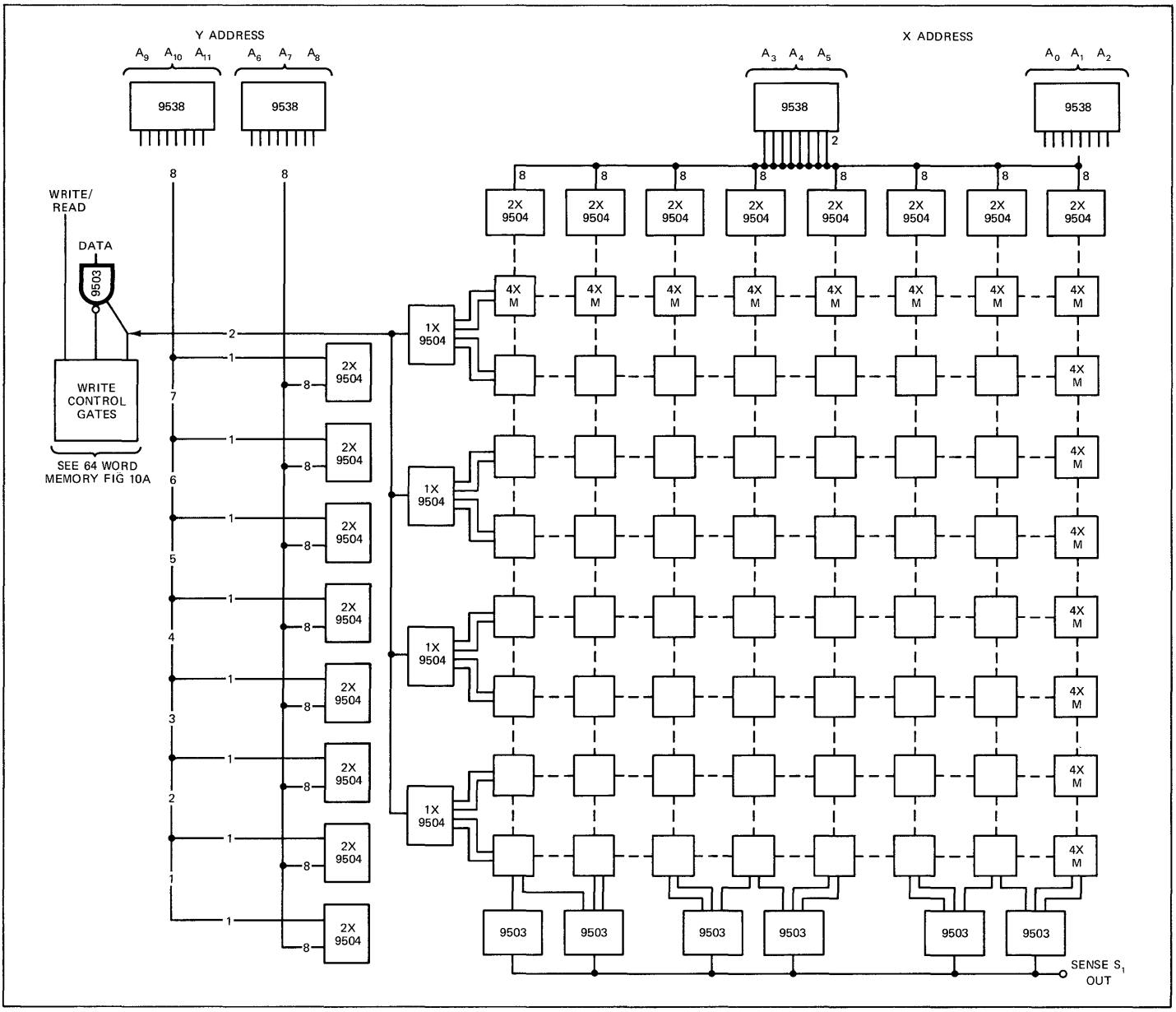
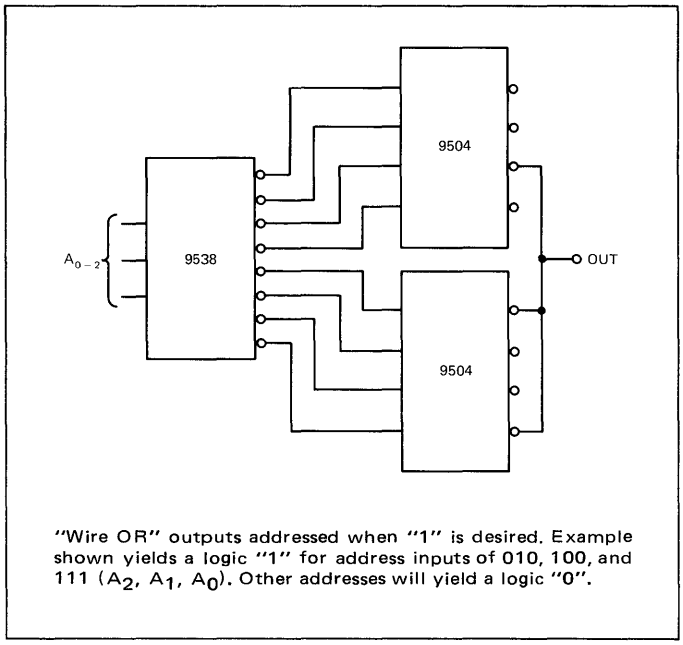


Fig. 11. 4K-Word X 1-Bit Memory

of two 9504 drivers. No external termination is required unless line length exceeds 12 inches in this case, as the enable input presents a heavier load. The 9504 driver outputs fan out to sixteen memory address inputs. 9504 gates are employed on the Read/Write control columns and for sensing sixteen memory outputs are tied to each 9503 gate input.

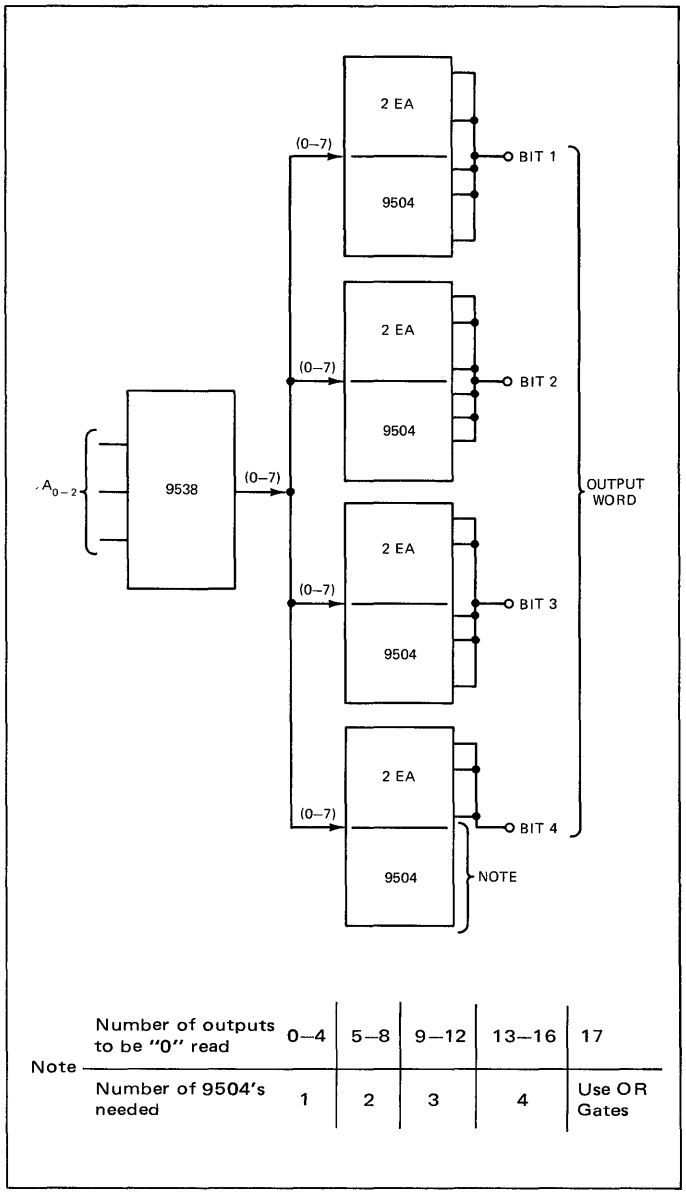
FUNCTION GENERATOR

The 9538 may also be used to construct a Read Only Memory or Function (minterm) Generator. By driving two 9504 Quad inverters from each output bit a simple 8-word x 1-bit function generator is achieved, Figure 12. This can be used for any control or display function where very high speed is required. Typical propagation delay of a ROM/Function Generator of 8 words by "N" bits will be less than 8 ns. A method of expanding the 8-bit ROM (Figure 12) to a 32-bit ROM (8 words x 4 bits) is shown in Figure 13.



"Wire OR" outputs addressed when "1" is desired. Example shown yields a logic "1" for address inputs of 010, 100, and 111 (A_2, A_1, A_0). Other addresses will yield a logic "0".

Fig. 12. 8 X 1 ROM/Function Generator



Note

Number of outputs to be "0" read	0–4	5–8	9–12	13–16	17
Number of 9504's needed	1	2	3	4	Use OR Gates

Fig. 13.

By use of the expansion schemes shown in Figures 8 and 9 a 32 or 64-word ROM is obtained with read times of only 3 ns more than the decode time.

The 9581 multiplexer may also be used for this function. The difference being that an 8 x "N" ROM would use either "N" 9581's or 1 9538 and "N" 9504's. The latter is the most economical, while the former uses fewer packages.

SUMMARY

This Application Brief has described the operation and major features of the 9538 1-out-of-8 ECL/MSI decoder. The device is particularly useful for memory address selection and provides functional building block capability for the 9500 Temperature Compensated ECL family.

The availability of ECL/MSI functions significantly reduces the cost of high performance systems implementation as it concentrates many operations on chip, thus eliminating many interconnections with associated delays and termination requirements.

REFERENCES

1. Fairchild Applications Brief #App. 157 – "9500 System Applications and Wiring Rules"
2. Fairchild Technical Paper #TP59 – "Temperature Compensated ECL"
3. Fairchild Application Bulletin #App 160 – "Applications of 9301 Decoder"
4. Fairchild Application Note #App 170 – "Applications of the 9311 Decoder"
5. Fairchild Applications Brief #App 179 – "Discrete ECL/TTL Interface Circuits"

FAIRCHILD SEMICONDUCTOR

9500 SERIES
TEMPERATURE COMPENSATED ECL

9500 Product Listing

*95H00	4-Bit Universal Register
9502	Dual-4-Input OR/NOR Gate (2.4 ns)
95H02	High Speed 9502 (1.6 ns)
9503	Triple 2-Input OR/NOR Gate (2.4 ns)
95H03	High Speed 9503 (1.6 ns)
9504	Quad 2-Input NOR Gate (2.4 ns)
95H04	High Speed 9504 (1.6 ns)
9505	Quad OR-AND Gate
9507	Quad AND-NAND Gate
*95H10	Synchronous Decade Counter
*95H16	Synchronous Binary Counter
95L22	Low Power (20 mW, 2 ns)
95L23	Low Power (20 mW, 2 ns)
95L24	Low Power (20 mW, 2 ns)
*9528	160 MHz "Dual D" Flip-Flop
95H28	220 MHz 9528
95H29	210 MHz J-K Flip-Flop
9534	Quad Latch
9538	3 Line/8 Line Decoder
*95H39	8-Bit Multiport Memory
*95H41	4-Bit ALU
*95H42	Look Ahead Unit for 95H41
*95H55	5-Bit Comparator
9578	Quad Exclusive-OR Gate/4-Bit Comparator
9579	Quad 2-Input Multiplexer
9580	Triple 2-Input Multiplexer
9581	8-Input Multiplexer
9582	Multifunction Receiver/Schmitt Trigger
95H84	2-Bit Adder/Subtractor
95H90	250 MHz Prescaler (divide by 10/11)
9595	ECL–TTL Converter
*95400	64-Bit RAM - 16x4
95401	16-Bit RAM - 16x1
*95410	256-Bit RAM - 256x1

* In Development

9500 "EASY ECL"

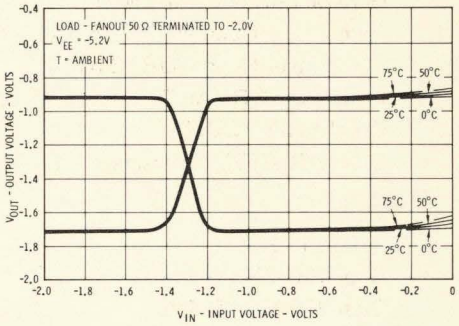
The Fairchild 9500 Temperature Compensated ECL family is designed for low power, low cost, high performance digital systems:

- Mainframe Computers
- High Speed Peripherals
- Minicomputers
- Instrumentation
- Test Systems
- Digital Communications

The provision of temperature stable logic levels insures up to four times higher noise immunity, across the operating temperature range than with conventional ECL. This permits the use of simple direct wiring interconnections. Thus board design requirements no more costly or difficult to apply than those necessary for high speed TTL may be employed. System performance, on the other hand, may be improved by a factor of two to five times.

9500 offers a versatile line of SSI devices with functions optimized for low power, high speed and general purpose, low cost applications. However the major emphasis is on MSI functions. This insures low cost, together with both high speed and low power by eliminating the majority of external wiring delays and power consuming terminations incurred by an SSI design.

TRANSFER CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



9500 FEATURES

- **Low Power High Speed**
  Low power SSI gates and high complexity MSI insure system power dissipation, including terminations, below 20 mW per gate.
- **Temperature Compensation**
  Logic levels remain constant across range 0°C to 75°C. Maintains maximum system noise immunity and eliminates saturation problems.
- **Packaging**
  Hermetic 16 pin Dual In-Line Package
- **Internal Pull Down Resistors**
  Point to point wiring up to 8" on single sided boards permitted by internal 2 kΩ resistors.
- **Low Crosstalk and Noise Generation**
  Insured by provision of split V_{CC} lines and location of supply pins.

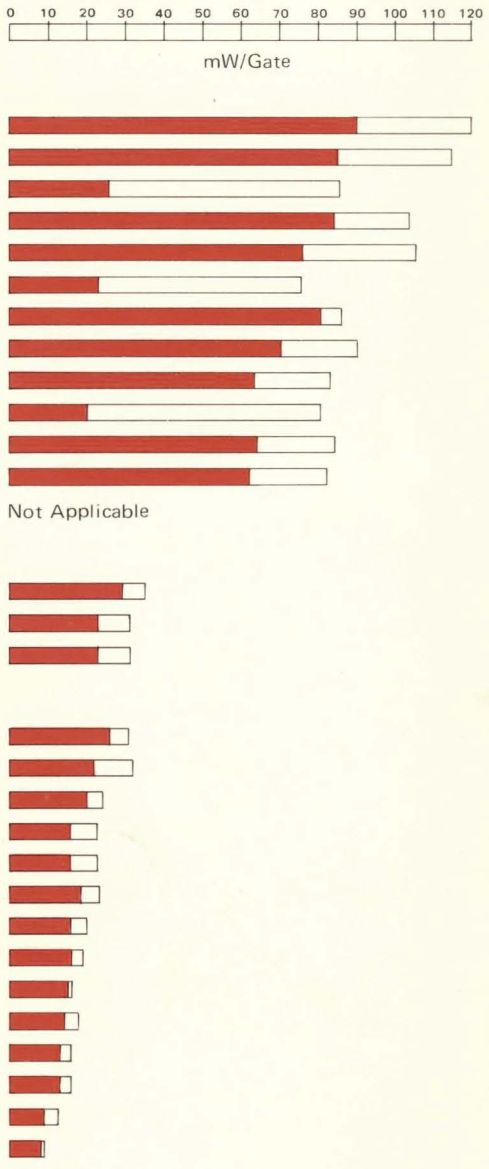
OCTOBER 1971

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA 94040, (415) 962-5011, TWX 910-379-6435

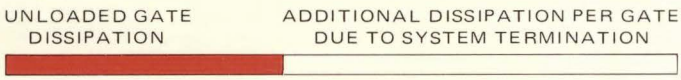
- **50 Ω Line Drive Capability**
  Output transistors designed to drive a 50 Ω terminated line and a fanout of 10 loads simultaneously.
- **Single Power Supply**
  9500 elements are specified for use with a single power supply.
- **MSI Flexibility**
  The 9500 product range has been designed to take maximum advantage of MSI devices to insure highest speed at low power.

ECL – MSI INSURES LOWEST POWER, HIGH PERFORMANCE SYSTEMS

DEVICE	DESCRIPTION	GATES/ FUNCTION (1)
SSI – GATES		
9502	General Purpose Dual OR–NOR (2.4 ns)	2
95H02	High Speed Dual OR–NOR (1.6 ns)	2
95L22	Low Power Dual OR–NOR (2 ns)	2
9503	General Purpose Triple OR–NOR	3
95H03	High Speed Triple OR–NOR	3
95L23	Low Power Triple OR–NOR (2 ns)	3
9582	Triple Line Receiver/Amplifier	3
9504	General Purpose Quad NOR	4
95H04	High Speed Quad NOR (1.6 ns)	4
95L24	Low Power Quad NOR (2 ns)	4
9505	Four Wide OR–AND	5
9507	Quad AND–NAND	5
9595	Dual ECL–TTL Converters	2
SSI – FLIP-FLOPS		
95H29	210 MHz J–K	9
9528	Dual 160 MHz D-Type	12
95H28	Dual 220 MHz D-Type	12
MSI – ELEMENTS		
9538	1 of 8 Decoder	12
9581	8 Input Multiplexer	12
9580	Triple 2 Input Multiplexer	13
9578	Quad EX/OR Comparator	16
9579	Quad 2 Input Multiplexer	16
95H42	Carry Look Ahead Unit	18
9534	Quad Latch	24
95H84	Adder/Subtractor	29
95H90	250 MHz Prescaler	29
95H00	4 Bit Shift Register	38
95H10	Decimal Counter	40
95H16	Binary Counter	40
95H41	4 Bit A.L.U.	75
95H39	8 Bit Multiport Register	76



Note (1). On-chip ECL gates, not discrete TTL equivalents.



KEY

The chart above compares the unloaded and system loaded power dissipations of 9500 ECL functions. The increase in power is due to dissipation in the output stage and either 2 kΩ on-chip or 50 Ω external termination resistors. Note that 20 mW SSI gates increase to 80 mW in a 50 Ω shunt termination system.

In an MSI function the additional power is only incurred at the output gate and is amortized over many internal gates. Thus in a system built largely with MSI, the system power per gate remains close to the unloaded power. Lowest power systems are therefore achieved with maximum use of MSI.

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