

# MB85346A-60/-70/-80

## CMOS 1 M x 36 Fast Page Mode DRAM Module

### CMOS 1,024,576 x 36 Bit Fast Page Mode DRAM Module

The Fujitsu MB85346A is a fully decoded, CMOS dynamic random access memory (DRAM) module consisting of eight MB814400A devices and four MB81C1000A devices. The MB85346A is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85346A are the same as the MB814400A which features fast page mode operation. For ease of memory expansion, the MB85346A is offered in a 72-pad Single In-line Memory Module package (SIMM).

#### PRODUCT LINE & FEATURES

| Parameter                 | MB85346A-60                                     | MB85346A-70        | MB85346A-80        |
|---------------------------|---|--------------------|--------------------|
| RAS Access Time           | 60ns  | 70ns               | 80ns               |
| Random Cycle Time         | max.<br>110ns min.                              | max.<br>125ns min. | max.<br>140ns min. |
| Address Access Time       | 30ns  | 35ns               | 40ns               |
| CAS Access Time           | max.<br>15ns                                    | max.<br>20ns       | max.<br>20ns       |
| Fast Page Mode Cycle Time | max.<br>40ns min.                               | max.<br>45ns min.  | max.<br>45ns min.  |
| Power Dissipation         | 6468mW max.                                     | 5896mW max.        | 5324mW max.        |
| • Operating mode          | 132mW max. (TTL level) / 66mW max. (CMOS level) |                    |                    |
| • Standby mode            |   |                    |                    |

- Organization : 1,024,576 words x 36 bits
- Memory : MB814400A, 8 pcs  
MB81C1000A, 4 pcs
- Decoupling Capacitor : 0.22  $\mu$ F, 12 pcs
- Package and Ordering Information:  
72-pad SIMM, order as  
MB85346A-xxPJPBK  
(PJPBK = Gold Pad) or  
MB85346A-xxPJPB  
(PJPB = Solder Pad)

#### ABSOLUTE MAXIMUM RATINGS (See NOTE.)

| Parameter                    | Symbol | Value        | Unit |
|------------------------------|--------|--------------|------|
| Supply Voltage               | VCC    | -1.0 to +7.0 | V    |
| Input Voltage                | VIN    | -1.0 to +7.0 | V    |
| Output Voltage               | VOUT   | -1.0 to +7.0 | V    |
| Short Circuit Output Current | IOUT   | 50           | mA   |
| Power Dissipation            | PD     | 12.0         | W    |
| Storage Temperature          | TSTG   | -55 to +125  | °C   |

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**PRELIMINARY**

See page 6  
**MSS-72P-P11**

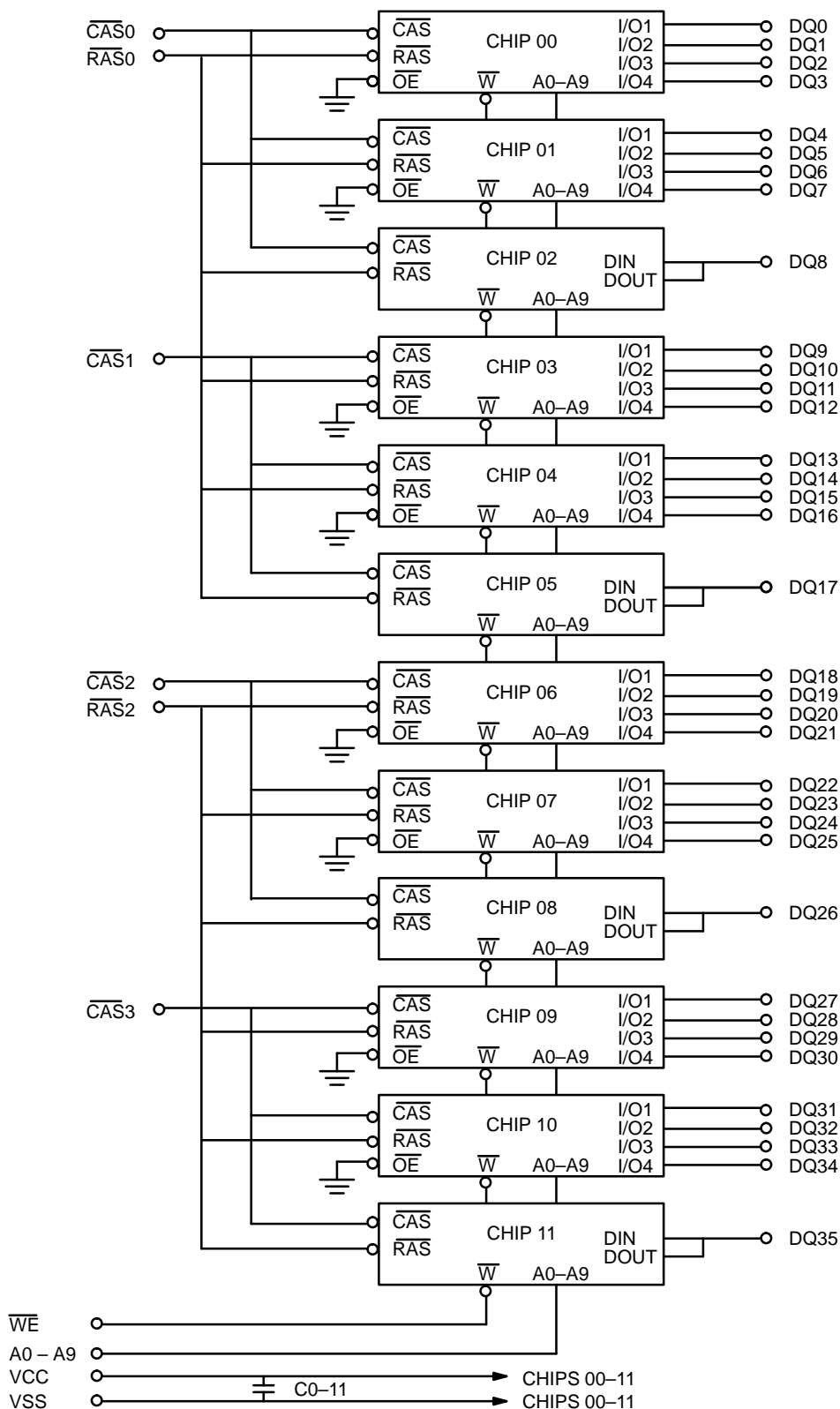
See page 7  
**MSS-72P-P23**

|      |    |    |      |
|------|----|----|------|
| DQ0  | 2  | 1  | VSS  |
| DQ1  | 4  | 3  | DQ18 |
| DQ2  | 6  | 5  | DQ19 |
| DQ3  | 8  | 7  | DQ20 |
| VCC  | 10 | 9  | DQ21 |
| A0   | 12 | 11 | NC   |
| A2   | 14 | 13 | A1   |
| A4   | 16 | 15 | A3   |
| A6   | 18 | 17 | A5   |
| DQ4  | 20 | 19 | NC   |
| DQ5  | 22 | 21 | DQ22 |
| DQ6  | 24 | 23 | DQ23 |
| DQ7  | 26 | 25 | DQ24 |
| A7   | 28 | 27 | DQ25 |
| VCC  | 30 | 29 | NC   |
| A9   | 32 | 31 | A8   |
| RAS2 | 34 | 33 | NC   |
| DQ8  | 36 | 35 | DQ26 |
| DQ35 | 38 | 37 | DQ17 |
| CAS0 | 40 | 39 | VSS  |
| CAS3 | 42 | 41 | CAS2 |
| RAS0 | 44 | 43 | CAS1 |
| NC   | 46 | 45 | NC   |
| NC   | 48 | 47 | WE   |
| DQ27 | 50 | 49 | DQ9  |
| DQ28 | 52 | 51 | DQ10 |
| DQ29 | 54 | 53 | DQ11 |
| DQ30 | 56 | 55 | DQ12 |
| DQ31 | 58 | 57 | DQ13 |
| DQ32 | 60 | 59 | VCC  |
| DQ33 | 62 | 61 | DQ14 |
| DQ34 | 64 | 63 | DQ15 |
| NC   | 66 | 65 | DQ16 |
| PD2  | 68 | 67 | PD1  |
| PD4  | 70 | 69 | PD3  |
| VSS  | 72 | 71 | NC   |

| Pin # | Symbol | -60 | -70 | -80 |
|-------|--------|-----|-----|-----|
| 67    | PD1    | Vss | Vss | Vss |
| 68    | PD2    | Vss | Vss | Vss |
| 69    | PD3    | NC  | Vss | NC  |
| 70    | PD4    | NC  | NC  | Vss |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

# FUNCTIONAL BLOCK DIAGRAM



## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

| Parameter   | Notes       | Symbol | Conditions  | Values |     |      | Unit |
|---|-------------|--------|---|--------|-----|------|------|
|   |             |        |   | Min    | Typ | Max  |      |
| Output High Voltage                                       |             | VOH    | IOH = -5mA  | 2.4    | —   | —    | V    |
| Output Low Voltage  |             | VOL    | IOL = 4.2mA   | —      | —   | 0.4  | V    |
| Input Leakage Current                                     | RAS         | II(L)  | 0V ≤ VIN ≤ 5.5V;<br>4.5V ≤ VCC ≤ 5.5V;<br>VSS=0V; all other pins<br>not under test = 0V | -40    | —   | 40   | μA   |
|   | CAS         |        |   | -30    | —   | 30   |      |
|   | ADD, WE     |        |   | -80    | —   | 80   |      |
| Output Leakage Current                                    |             | IO(L)  | 0V ≤ VOUT ≤ 5.5V;<br>Data out disabled  | -20    | —   | 20   | μA   |
| Operating Current<br>(Average power<br>supply current) 1  | MB85346A-60 | ICC1   | RAS & CAS cycling;<br>tRC = min.  | —      | —   | 1176 | mA   |
|   | MB85346A-70 |        |   |        |     | 1072 |      |
|   | MB85346A-80 |        |   |        |     | 968  |      |
| Standby Current<br>(Power supply<br>current)              | TTL Level   | ICC2   | RAS = CAS = VIH   | —      | —   | 24   | mA   |
|   | CMOS Level  |        | RAS = CAS ≥ VCC-0.2V  |        |     | 12   |      |
| Refresh Current #1<br>(Average power<br>supply current) 1 | MB85346A-60 | ICC3   | CAS = VIH;<br>RAS = cycling;<br>tRC = min.  | —      | —   | 1176 | mA   |
|   | MB85346A-70 |        |   |        |     | 1072 |      |
|   | MB85346A-80 |        |   |        |     | 968  |      |
| Fast Page Mode<br>Current 1                               | MB85346A-60 | ICC4   | RAS = VIL;<br>CAS = cycling;<br>tPC = min.  | —      | —   | 684  | mA   |
|   | MB85346A-70 |        |   |        |     | 624  |      |
|   | MB85346A-80 |        |   |        |     | 584  |      |
| Refresh Current #2<br>(Average power<br>supply current) 1 | MB85346A-60 | ICC5   | RAS = cycling;<br>CAS-before-RAS<br>tRC = min.  | —      | —   | 1016 | mA   |
|   | MB85346A-70 |        |   |        |     | 912  |      |
|   | MB85346A-80 |        |   |        |     | 808  |      |

**Note:** 1. ICC depends on the output load conditions and cycle rate; The specified values are obtained with the output open.  
ICC depends on the number of address change as RAS = VIL and CAS = VIH, VIL > -0.5V.  
ICC1, ICC3 and ICC5 are specified at one time of address change during RAS = VIL and CAS = VIH.  
ICC4 is specified at one time of address change during one Page cycle.

## CAPACITANCE (TA = 25°C, f = 1MHz)

| Parameter  | Symbol | Value |     | Unit |
|--|--------|-------|-----|------|
|  |        | Typ   | Max |      |
| Input Capacitance, A0 to A9                        | CIN1   | —     | 77  | pF   |
| Input Capacitance, RAS0 and RAS2                   | CIN2   | —     | 40  | pF   |
| Input Capacitance, CAS0 to CAS3                    | CIN3   | —     | 27  | pF   |
| Input Capacitance, WE                              | CIN4   | —     | 68  | pF   |
| I/O Capacitance, (DQ0-7, DQ9-16, DQ18-25, DQ27-34) | CDQ1   | —     | 10  | pF   |
| I/O Capacitance, (DQ8, DQ17, DQ26, DQ35)           | CDQ2   | —     | 14  | pF   |

## AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

| No. | Parameter  | Notes | Symbol | MB85346A-60 |        | MB85346A-70 |        | MB85346A-80 |        | Unit |
|-----|--|-------|--------|-------------|--------|-------------|--------|-------------|--------|------|
|     |  |       |        | Min         | Max    | Min         | Max    | Min         | Max    |      |
| 1   | Time Between Refresh   | 17    | tREF   | —           | 16.4   | —           | 16.4   | —           | 16.4   | ms   |
| 2   | Random Read/Write Cycle Time   |       | tRC    | 110         | —      | 125         | —      | 140         | —      | ns   |
| 3   | Access Time from $\overline{\text{RAS}}$   | 4, 7  | tRAC   | —           | 60     | —           | 70     | —           | 80     | ns   |
| 4   | Access Time from $\overline{\text{CAS}}$   | 5, 7  | tCAC   | —           | 15     | —           | 20     | —           | 20     | ns   |
| 5   | Column Address Access Time   | 6, 7  | tAA    | —           | 30     | —           | 35     | —           | 40     | ns   |
| 6   | Output Hold Time   |       | tOH    | 0           | —      | 0           | —      | 0           | —      | ns   |
| 7   | Output Buffer Turn on Delay Time   |       | tON    | 0           | —      | 0           | —      | 0           | —      | ns   |
| 8   | Output Buffer Turn off Delay Time  | 8     | tOFF   | —           | 15     | —           | 15     | —           | 20     | ns   |
| 9   | Transition Time  |       | tT     | 2           | 50     | 2           | 50     | 2           | 50     | ns   |
| 10  | $\overline{\text{RAS}}$ Precharge Time   |       | tRP    | 40          | —      | 45          | —      | 50          | —      | ns   |
| 11  | $\overline{\text{RAS}}$ Pulse Width  |       | tRAS   | 60          | 100000 | 70          | 100000 | 80          | 100000 | ns   |
| 12  | $\overline{\text{RAS}}$ Hold Time  |       | tRSH   | 15          | —      | 20          | —      | 20          | —      | ns   |
| 13  | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time                                    |       | tCRP   | 5           | —      | 5           | —      | 5           | —      | ns   |
| 14  | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time  | 9, 10 | tRCD   | 20          | 45     | 20          | 50     | 20          | 60     | ns   |
| 15  | $\overline{\text{CAS}}$ Pulse Width  |       | tCAS   | 15          | —      | 20          | —      | 20          | —      | ns   |
| 16  | $\overline{\text{CAS}}$ Hold Time  |       | tCSH   | 60          | —      | 70          | —      | 80          | —      | ns   |
| 17  | $\overline{\text{CAS}}$ Precharge Time<br>(C-B-R Refresh)  | 15    | tCPN   | 10          | —      | 10          | —      | 10          | —      | ns   |
| 18  | Row Address Setup Time   |       | tASR   | 0           | —      | 0           | —      | 0           | —      | ns   |
| 19  | Row Address Hold Time  |       | tRAH   | 10          | —      | 10          | —      | 10          | —      | ns   |
| 20  | Column Address Setup Time  |       | tASC   | 0           | —      | 0           | —      | 0           | —      | ns   |
| 21  | Column Address Hold Time   |       | tCAH   | 12          | —      | 12          | —      | 15          | —      | ns   |
| 22  | $\overline{\text{RAS}}$ to Column Address Delay Time   | 11    | tRAD   | 15          | 30     | 15          | 35     | 15          | 40     | ns   |
| 23  | Column Address to $\overline{\text{RAS}}$ Lead Time  |       | tRAL   | 30          | —      | 35          | —      | 40          | —      | ns   |
| 24  | Column Address to $\overline{\text{CAS}}$ Lead Time  |       | tCAL   | 30          | —      | 35          | —      | 40          | —      | ns   |
| 25  | Read Command Setup Time  |       | tRCS   | 0           | —      | 0           | —      | 0           | —      | ns   |
| 26  | Read Command Hold Time<br>Referenced to $\overline{\text{RAS}}$                                      | 12    | tRRH   | 0           | —      | 0           | —      | 0           | —      | ns   |
| 27  | Read Command Hold Time<br>Referenced to $\overline{\text{CAS}}$                                      | 12    | tRCH   | 0           | —      | 0           | —      | 0           | —      | ns   |
| 28  | Write Command Setup Time   | 13    | tWCS   | 0           | —      | 0           | —      | 0           | —      | ns   |
| 29  | Write Command Hold Time  |       | tWCH   | 10          | —      | 10          | —      | 12          | —      | ns   |
| 30  | $\overline{\text{WE}}$ Pulse Width   |       | tWP    | 10          | —      | 10          | —      | 12          | —      | ns   |
| 31  | Write Command to $\overline{\text{RAS}}$ Lead Time   |       | tRWL   | 15          | —      | 20          | —      | 20          | —      | ns   |
| 32  | Write Command to $\overline{\text{CAS}}$ Lead Time   |       | tCWL   | 15          | —      | 18          | —      | 20          | —      | ns   |
| 33  | DIN Setup Time   |       | tDS    | 0           | —      | 0           | —      | 0           | —      | ns   |
| 34  | DIN Hold Time  |       | tDH    | 10          | —      | 10          | —      | 12          | —      | ns   |
| 35  | $\overline{\text{RAS}}$ Precharge Time to $\overline{\text{CAS}}$ Active<br>Time Low (Refresh Cycle) |       | tRPC   | 0           | —      | 0           | —      | 0           | —      | ns   |

## AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

| No. | Parameter                            | Notes | Symbol | MB85346A-60 |        | MB85346A-70 |        | MB85346A-80 |        | Unit |
|-----|--------------------------------------|-------|--------|-------------|--------|-------------|--------|-------------|--------|------|
|     |                                      |       |        | Min         | Max    | Min         | Max    | Min         | Max    |      |
| 36  | CAS Setup Time (C-B-R Refresh)       |       | tCSR   | 0           | —      | 0           | —      | 0           | —      | ns   |
| 37  | CAS Hold Time (C-B-R refresh)        |       | tCHR   | 10          | —      | 10          | —      | 12          | —      | ns   |
| 38  | WE Set Up Time from RAS              | 16    | tWSR   | 0           | —      | 0           | —      | 0           | —      | ns   |
| 39  | WE Hold Time from RAS                | 16    | tWHR   | 10          | —      | 10          | —      | 10          | —      | ns   |
| 40  | DIN to CAS Delay Time                |       | tDZC   | 0           | —      | 0           | —      | 0           | —      | ns   |
| 41  | Fast Page Mode RAS Pulse Width       |       | tRASP  | —           | 100000 | —           | 100000 | —           | 100000 | ns   |
| 42  | Fast Page Mode Read/Write Cycle Time |       | tPC    | 40          | —      | 45          | —      | 45          | —      | ns   |
| 43  | Access Time from CAS Precharge       | 7, 14 | tCPA   | —           | 35     | —           | 40     | —           | 40     | ns   |
| 44  | Fast Page Mode CAS Precharge Time    |       | tCP    | 10          | —      | 10          | —      | 10          | —      | ns   |
| 45  | RAS Hold Time from CAS Precharge     |       | tRHCP  | 35          | —      | 40          | —      | 40          | —      | ns   |

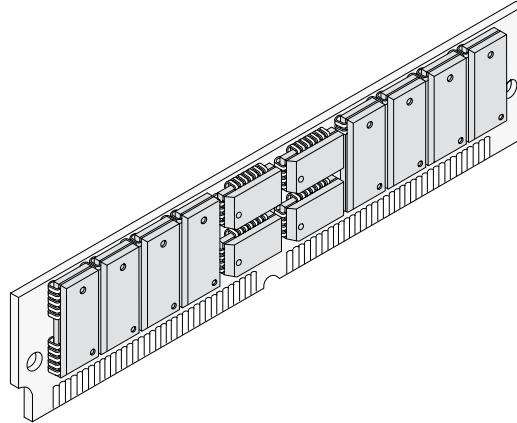
### Notes:

1. An Initial pause ( $\overline{\text{RAS}} = \overline{\text{CAS}} = \text{VIH}$ ) of 200 $\mu\text{s}$  is required after power-up followed by any eight  $\overline{\text{RAS}}$ —only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight  $\overline{\text{CAS}}$ —before— $\overline{\text{RAS}}$  initialization cycles are required instead of eight  $\overline{\text{RAS}}$  cycles.
2. AC characteristics assume  $t_T = 5\text{ns}$ .
3.  $\text{VIH}$  (min) and  $\text{VIL}$  (max) are reference levels for measuring the timing of input signals. Also, transition times are measured between  $\text{VIH}$  (min) and  $\text{VIL}$  (max).
4. Assumes that  $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ ,  $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$ . If  $t_{\text{RCD}}$  is greater than the maximum recommended value shown in this table,  $t_{\text{RAC}}$  will be increased by the amount that  $t_{\text{RCD}}$  exceeds the value shown.
5. If  $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ ,  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$ , and  $t_{\text{ASC}} \geq t_{\text{AA}} - t_{\text{CAC}} - t_T$ , access time is  $t_{\text{CAC}}$ .
6. If  $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$  and  $t_{\text{ASC}} \leq t_{\text{AA}} - t_{\text{CAC}} - t_T$ , access time is  $t_{\text{AA}}$ .
7. Measured with a load equivalent to two TTL loads and 100 pF.
8.  $t_{\text{OFF}}$  is specified that output buffer change to high impedance state.
9. Operation within the  $t_{\text{RCD}}(\text{max})$  limit ensures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RCD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RCD}}$  is greater than the specified  $t_{\text{RCD}}(\text{max})$  limit, access time is controlled exclusively by  $t_{\text{CAC}}$  or  $t_{\text{AA}}$ .
10.  $t_{\text{RCD}}(\text{min}) = t_{\text{RAH}}(\text{min}) + 2t_T + t_{\text{ASC}}(\text{min})$ .
11. Operation within the  $t_{\text{RAD}}(\text{max})$  limit ensures that  $t_{\text{RAC}}(\text{max})$  can be met.  $t_{\text{RAD}}(\text{max})$  is specified as a reference point only; if  $t_{\text{RAD}}$  is greater than the specified  $t_{\text{RAD}}(\text{max})$  limit, access time is controlled exclusively by  $t_{\text{CAC}}$  or  $t_{\text{AA}}$ .
12. Either  $t_{\text{RRH}}$  or  $t_{\text{RCH}}$  must be satisfied for a read cycle.
13. If  $t_{\text{WCS}} > t_{\text{WCS}}(\text{min})$ , the data output pin will remain in the high-Z state through the entire cycle.
14.  $t_{\text{CPA}}$  is access time from the selection of a new column address (caused by changing  $\overline{\text{CAS}}$  from "L" to "H"). Therefore, if  $t_{\text{CP}}$  become long,  $t_{\text{CPA}}$  also become longer than  $t_{\text{CPA}}(\text{max})$ .
15. Assumes that  $\overline{\text{CAS}}$ —before— $\overline{\text{RAS}}$  refresh.
16. Assumes that test mode function for non-parity bit.
17.  $t_{\text{REF}}$  is for distributed refresh (1024 refresh cycles / 16.4 ms). For burst refresh,  $t_{\text{REF}} = 8.2\text{ms}$  (1024 refresh cycles / 8.2 ms).

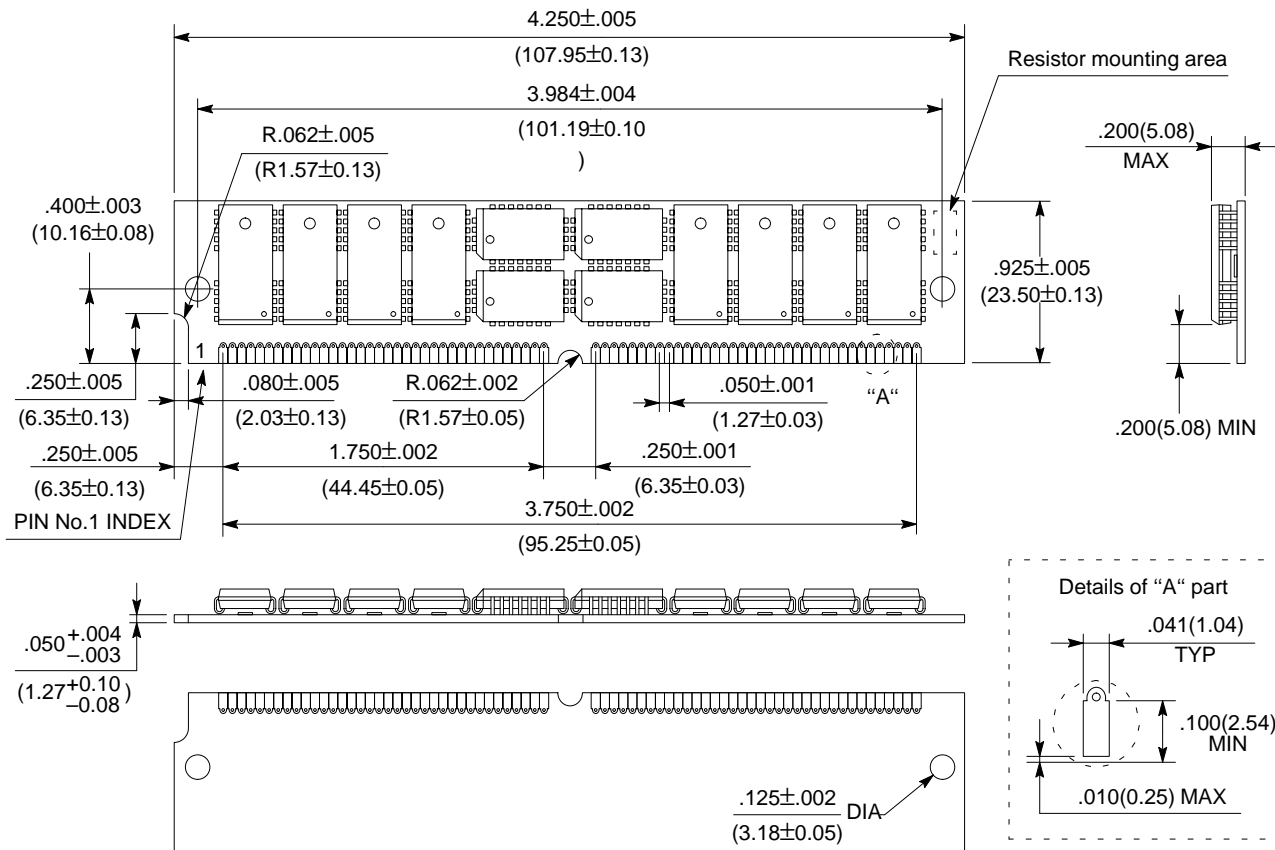
\*Source: See MB814400A Data Sheet for details on the electricals.

# PACKAGE DIMENSIONS

(Suffix: PJPBK)



## 72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE (CASE No.: MSS-72P-P11)



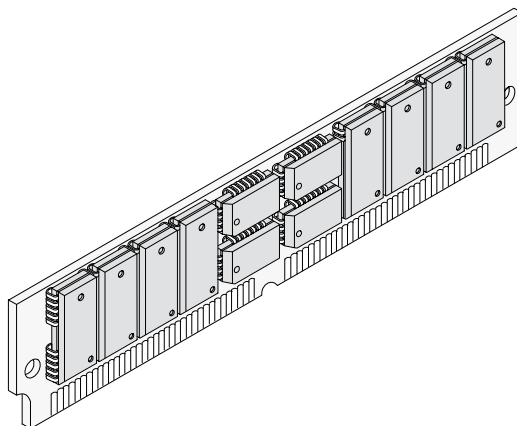
\*Resistor thickness is .040(1.00)max. from board surface.

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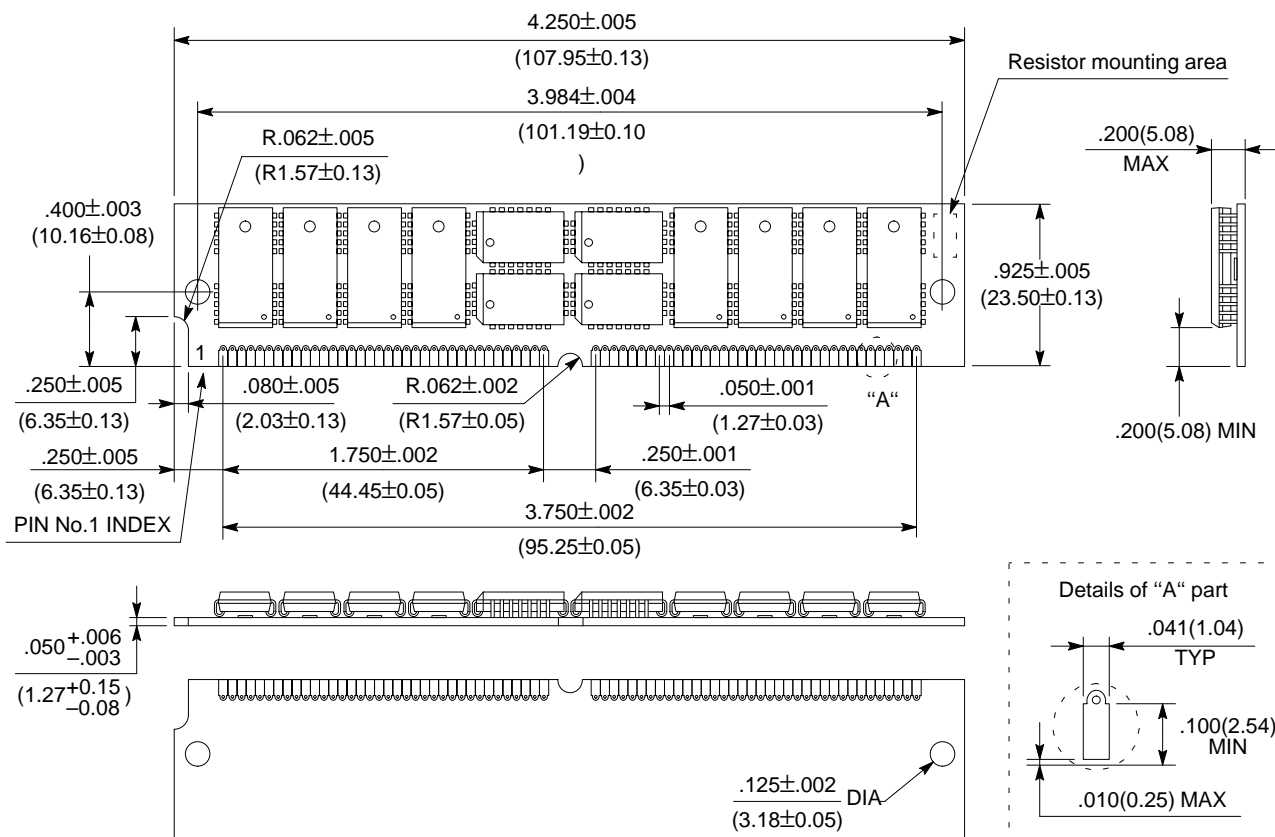
Dimensions in  
inches (millimeters)

# PACKAGE DIMENSIONS

(Suffix: PJPB)



## 72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE (CASE No.: MSS-72P-P23)



\*Resistor thickness is .040(1.00)max. from board surface.

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Dimensions in  
inches (millimeters)

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