

## MB8116800A-60/-70

### CMOS 2M X 8BIT FAST PAGE MODE DYNAMIC RAM

#### CMOS 2,097,152 x 8BIT Fast Page Mode Dynamic RAM

The Fujitsu MB8116800A is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 8-bit increments. The MB8116800A features a "fast page" mode of operation whereby high-speed random access of up to 512-bits of data within the same row can be selected. The MB8116800A DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB8116800A is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB8116800A is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB8116800A are not critical and all inputs are TTL compatible.

#### PRODUCT LINE & FEATURES

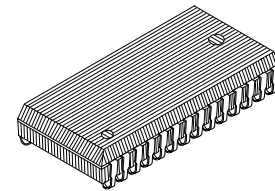
Parameter		MB8116800A -60	MB8116800A -70
RAS Access Time		60ns max.	70ns max.
Random Cycle Time		110ns min.	130ns min.
Address Access Time		30ns max.	35ns max.
CAS Access Time		15ns max.	17ns max.
Fast Page Mode Cycle Time		40ns min.	45ns min.
Low Power Dissipation	Operating current	495mW max.	440mW max.
	Standby current	11mW max. (TTL level) / 5.5mW max. (CMOS level)	

- 2,097,152 words × 8 bit organization
- Silicon gate, CMOS, Advanced Capacitor Cell
- All input and output are TTL compatible
- 4096 refresh cycles every 65.6ms
- Self refresh function
- Early write or  $\overline{OE}$  controlled write capability
- RAS only, CAS-before-RAS, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

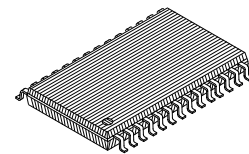
#### ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to +7.0	V
Voltage of $V_{CC}$ supply relative to $V_{SS}$	$V_{CC}$	-0.5 to +7.0	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Operating Temperature	$T_{OPE}$	0 to 70	°C
Storage Temperature	$T_{STG}$	-55 to +125	°C

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Plastic SOJ Package  
(LCC-28P-M07)



Plastic TSOP Packages  
(FPT-28P-M14)

#### Package and Ordering Information

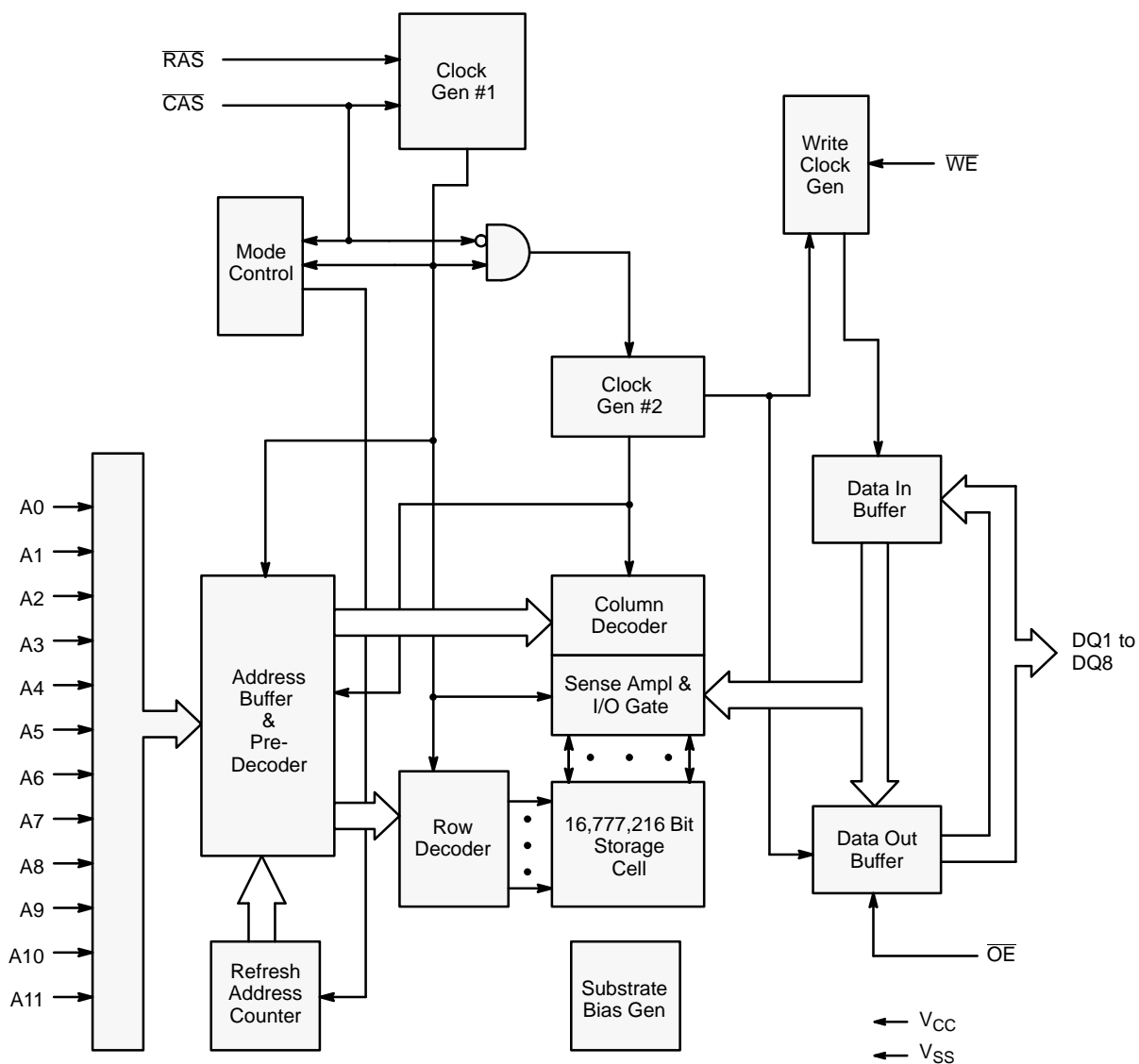
- 28-pin plastic (400mil) SOJ,  
order as MB8116800A-XXPJ
- 28-pin plastic (400mil) TSOP-II  
with normal bend leads,  
order as MB8116800A-XXPFTN

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Edition 2.0

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**MB8116800A-70**

**Fig. 1 – MB8116800A DYNAMIC RAM – BLOCK DIAGRAM**

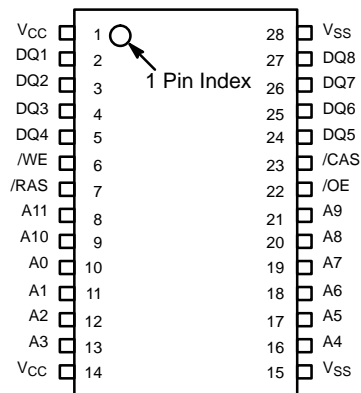


## CAPACITANCE ( $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

Parameter	Symbol	Max	Unit
Input Capacitance, A0 to A11	$C_{IN1}$	5	pF
Input Capacitance, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	$C_{IN2}$	5	pF
Input/Output Capacitance, DQ1 to DQ8	$C_{DQ}$	7	pF

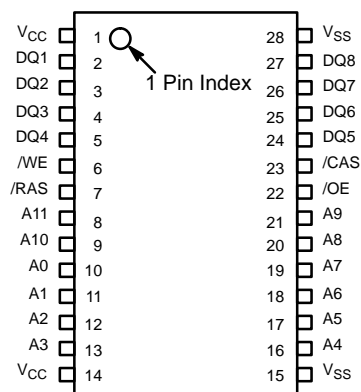
## PIN ASSIGNMENTS AND DESCRIPTIONS

28-Pin SOJ  
(TOP VIEW)



Designator	Function
A0 to A11	Address inputs row : A0 to A11 column : A0 to A8 refresh : A0 to A11
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
DQ1 to DQ8	Data Input/Output
$V_{\text{CC}}$	+5.0 volt power supply
$V_{\text{SS}}$	Circuit ground

28-Pin TSOP  
(TOP VIEW)



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## RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp.
Supply Voltage	1	$V_{CC}$	4.5	5.0	5.5	V	0°C to +70°C
		$V_{SS}$	0	0	0		
Input High Voltage, all inputs	1	$V_{IH}$	2.4	—	6.5	V	
Input High Voltage, all inputs/outputs*	1	$V_{IL}$	–0.3	—	0.8	V	

\* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20ns are acceptable.

## FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty-one input bits are required to decode any eight of 16,777,216 cell addresses in the memory matrix. Since only twelve address bits (A0 to A11) are available, the row and column inputs are separately strobed by  $\overline{RAS}$  and  $\overline{CAS}$  as shown in Figure 1. First, twelve row address bits are input on pins A0–through–A11 and latched with the row address strobe ( $\overline{RAS}$ ) then, nine column address bits are input and latched with the column address strobe ( $\overline{CAS}$ ). Both row and column addresses must be stable on or before the falling edge of  $\overline{RAS}$  and  $\overline{CAS}$ , respectively. The address latches are of the flow-through type; thus, address information appearing after  $t_{RAH}(\text{min}) + t_f$  is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of  $\overline{WE}$ . When  $\overline{WE}$  is active Low, a write cycle is initiated; when  $\overline{WE}$  is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an  $\overline{OE}$  (delayed) write cycle, and a read-modify-write cycle. The falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data (DQ1–DQ8) is strobed by  $\overline{CAS}$  and the setup/hold times are referenced to  $\overline{CAS}$  because  $\overline{WE}$  goes Low before  $\overline{CAS}$ . In a delayed write or a read-modify-write cycle,  $\overline{WE}$  goes Low after  $\overline{CAS}$ ; thus, input data is strobed by  $\overline{WE}$  and all setup/hold times are referenced to the write-enable signal.

### DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- $t_{RAC}$  : from the falling edge of  $\overline{RAS}$  when  $t_{RCD}(\text{max})$  is satisfied.
- $t_{CAC}$  : from the falling edge of  $\overline{CAS}$  when  $t_{RCD}$  is greater than  $t_{RCD}(\text{max})$ .
- $t_{AA}$  : from column address input when  $t_{RAD}$  is greater than  $t_{RAD}(\text{max})$ .
- $t_{OEA}$  : from the falling edge of  $\overline{OE}$  when  $\overline{OE}$  is brought Low after  $t_{RAC}$ ,  $t_{CAC}$ , or  $t_{AA}$ .

The data remains valid until either  $\overline{CAS}$  or  $\overline{OE}$  returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

### FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions,  $\overline{RAS}$  is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 512 x 8-bits can be accessed and, when multiple MB8116800As are used,  $\overline{CAS}$  is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Notes 3

Parameter	Notes	Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Output high voltage		$V_{OH}$	$I_{OH} = -5.0\text{mA}$	2.4	—	—	V
Output low voltage		$V_{OL}$	$I_{OL} = +4.2\text{mA}$	—	—	0.4	
Input leakage current (any input)		$I_{I(L)}$	$0\text{V} \leq V_{IN} \leq V_{CC}$ ; $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ ; $V_{SS} = 0\text{V}$ ; All other pins under test = 0V	-10	—	10	$\mu\text{A}$
Output leakage current		$I_{DQ(L)}$	$0\text{V} \leq V_{OUT} \leq V_{CC}$ ; Data out disabled	-10	—	10	
Operating current (Average power supply current) <span style="border: 1px solid black; padding: 0 2px;">2</span>	MB8116800A-60	$I_{CC1}$	RAS & CAS cycling; $t_{RC} = \text{min}$	—	—	90	mA
	MB8116800A-70					80	
Standby current (Power supply current)	TTL level	$I_{CC2}$	$RAS = CAS = V_{IH}$	—	—	2.0	mA
	CMOS level		$RAS = CAS \geq V_{CC} - 0.2\text{V}$			1.0	
Refresh current #1 (Average power supply current) <span style="border: 1px solid black; padding: 0 2px;">2</span>	MB8116800A-60	$I_{CC3}$	$CAS = V_{IH}$ , RAS cycling; $t_{RC} = \text{min}$	—	—	90	mA
	MB8116800A-70					80	
Fast Page Mode Current <span style="border: 1px solid black; padding: 0 2px;">2</span>	MB8116800A-60	$I_{CC4}$	$RAS = V_{IL}$ , CAS cycling; $t_{PC} = \text{min}$	—	—	80	mA
	MB8116800A-70					70	
Refresh current #2 (Average power supply current) <span style="border: 1px solid black; padding: 0 2px;">2</span>	MB8116800A-60	$I_{CC5}$	RAS cycling; CAS-before-RAS; $t_{RC} = \text{min}$	—	—	80	mA
	MB8116800A-70					70	
Refresh current #3 (Average power sup- ply current)	MB8116800A-60	$I_{CC9}$	RAS = VIL, CAS = VIL Self refresh ; $t_{RASS} = \text{min.}$	—	—	1000	$\mu\text{A}$
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## AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3,4,5

No.	Parameter	Notes	Symbol	MB8116800A-60		MB8116800A-70		Unit
				Min	Max	Min	Max	
1	Time Between Refresh		$t_{REF}$	—	65.6	—	65.6	ms
2	Random Read/Write Cycle Time		$t_{RC}$	110	—	130	—	ns
3	Read-Modify-Write Cycle Time		$t_{RWC}$	150	—	174	—	ns
4	Access Time from $\overline{RAS}$	6,9	$t_{RAC}$	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	7,9	$t_{CAC}$	—	15	—	17	ns
6	Column Address Access Time	8,9	$t_{AA}$	—	30	—	35	ns
7	Output Hold Time		$t_{OH}$	3	—	3	—	ns
8	Output Buffer Turn On Delay Time		$t_{ON}$	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	10	$t_{OFF}$	—	15	—	17	ns
10	Transition Time		$t_T$	3	50	3	50	ns
11	$\overline{RAS}$ Precharge Time		$t_{RP}$	40	—	50	—	ns
12	$\overline{RAS}$ Pulse Width		$t_{RAS}$	60	100000	70	100000	ns
13	$\overline{RAS}$ Hold Time		$t_{RSH}$	15	—	17	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		$t_{CRP}$	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	$t_{RCD}$	20	45	20	53	ns
16	$\overline{CAS}$ Pulse Width		$t_{CAS}$	15	—	17	—	ns
17	$\overline{CAS}$ Hold Time		$t_{CSH}$	60	—	70	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	19	$t_{CPN}$	10	—	10	—	ns
19	Row Address Set Up Time		$t_{ASR}$	0	—	0	—	ns
20	Row Address Hold Time		$t_{RAH}$	10	—	10	—	ns
21	Column Address Set Up Time		$t_{ASC}$	0	—	0	—	ns
22	Column Address Hold Time		$t_{CAH}$	15	—	15	—	ns
23	Column Address Hold Time from $\overline{RAS}$		$t_{AR}$	35	—	35	—	ns
24	$\overline{RAS}$ to Column Address Delay Time	13	$t_{RAD}$	15	30	15	35	ns
25	Column Address to $\overline{RAS}$ Lead Time		$t_{RAL}$	30	—	35	—	ns
26	Column Address to $\overline{CAS}$ Lead Time		$t_{CAL}$	30	—	35	—	ns
27	Read Command Set Up Time		$t_{RCS}$	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{RAS}$	14	$t_{RRH}$	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{CAS}$	14	$t_{RCH}$	0	—	0	—	ns
30	Write Command Set Up Time	15	$t_{WCS}$	0	—	0	—	ns
31	Write Command Hold Time		$t_{WCH}$	15	—	15	—	ns
32	Write Hold Time from $\overline{RAS}$		$t_{WCR}$	35	—	35	—	ns
33	$\overline{WE}$ Pulse Width		$t_{WP}$	15	—	15	—	ns
34	Write Command to $\overline{RAS}$ Lead Time		$t_{RWL}$	15	—	17	—	ns
35	Write Command to $\overline{CAS}$ Lead Time		$t_{CWL}$	15	—	17	—	ns

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## AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3,4,5

No.	Parameter	Notes	Symbol	MB8116800A-60		MB8116800A-70		Unit
				Min	Max	Min	Max	
36	DIN Set Up Time		$t_{DS}$	0	—	0	—	ns
37	DIN Hold Time		$t_{DH}$	15	—	15	—	ns
38	Data Hold Time from $\overline{RAS}$		$t_{DHR}$	35	—	35	—	ns
39	RAS to WE Delay Time	20	$t_{RWD}$	80	—	92	—	ns
40	CAS to WE Delay Time	20	$t_{CWD}$	35	—	39	—	ns
41	Column Address to WE Delay Time	20	$t_{AWD}$	50	—	57	—	ns
42	RAS Precharge Time to CAS Active Time (Refresh cycles)		$t_{RPC}$	5	—	5	—	ns
43	CAS Set Up Time for CAS-before-RAS Refresh		$t_{CSR}$	0	—	0	—	ns
44	CAS Hold Time for CAS-before-RAS Refresh		$t_{CHR}$	10	—	12	—	ns
45	Access Time from OE	9	$t_{OEA}$	—	15	—	17	ns
46	Output Buffer Turn Off Delay from OE	10	$t_{OEZ}$	—	15	—	17	ns
47	OE to RAS Lead Time for Valid Data		$t_{OEL}$	10	—	10	—	ns
48	OE Hold Time Referenced to WE	16	$t_{OEH}$	5	—	5	—	ns
49	OE to Data In Delay Time		$t_{OED}$	15	—	17	—	ns
50	CAS to Data In Delay Time		$t_{CDD}$	15	—	17	—	ns
51	DIN to CAS Delay Time	17	$t_{DZC}$	0	—	0	—	ns
52	DIN to OE Delay Time	17	$t_{DZO}$	0	—	0	—	ns
60	Fast Page Mode RAS Pulse width		$t_{RASP}$	—	100000	—	100000	ns
61	Fast Page Mode Read/Write Cycle Time		$t_{PC}$	40	—	45	—	ns
62	Fast Page Mode Read-Modify-Write Cycle Time		$t_{PRWC}$	80	—	89	—	ns
63	Access Time from CAS Precharge	9,18	$t_{CPA}$	—	35	—	40	ns
64	Fast Page Mode CAS Precharge Time		$t_{CP}$	10	—	10	—	ns
65	Fast Page Mode RAS Hold Time from CAS Precharge		$t_{RHCP}$	35	—	40	—	ns
66	Fast Page Mode CAS Precharge to WE Delay Time		$t_{CPWD}$	55	—	62	—	ns

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### Notes:

1. Referenced to  $V_{SS}$ .
2.  $I_{CC}$  depends on the output load conditions and cycle rates;  
The

specified values are obtained with the output open.  $I_{CC}$   
depends on the number of address change as  $\overline{RAS} = V_{IL}$ ,  
 $\overline{CAS} = V_{IH}$  and  $V_{IL} > -0.3V$ .  
 $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC5}$  are specified at one time of address  
change

3. An initial pause ( $\overline{RAS} = \overline{CAS} = V_{IH}$ ) of 200 $\mu s$  is required after  
power-up followed by any eight RAS-only cycles before  
proper device operation is achieved. In case of using internal  
refresh counter, a minimum of eight  $\overline{CAS}$ -before-RAS initiali-  
zation cycles instead of 8  $\overline{RAS}$  cycles are required.
4. AC characteristics assume  $t_T = 5ns$ .
5.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring tim-  
ing of input signals. Also transition times are measured be-  
tween  $V_{IH}$  (min) and  $V_{IL}$  (max).
6. Assumes that  $t_{RCD} \leq t_{RCD}(max)$ ,  $t_{RAD} \leq t_{RAD}(max)$ . If  $t_{RCD}$  is  
greater than the maximum recommended value shown in this  
table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds  
the value shown. Refer to Fig.2 and 3.
7. If  $t_{RCD} \geq t_{RCD}(max)$ ,  $t_{RAD} \geq t_{RAD}(max)$ , and  $t_{ASC} \geq t_{AA}$   
 $-t_{CAC}-t_T$ , access time is  $t_{CAC}$ .
8. If  $t_{RAD} \geq t_{RAD}(max)$  and  $t_{ASC} \leq t_{AA} -t_{CAC}-t_T$ , access time is  
 $t_{AA}$ .
9. Measured with a load equivalent to two TTL loads and 100pF.
10.  $t_{OFF}$  and  $t_{OEZ}$  is specified that output buffer change to high  
impedance state.
11. Operation within the  $t_{RCD}(max)$  limit ensures that  $t_{RAC}(max)$   
can be met.  $t_{RCD}(max)$  is specified as a reference point only; if

$t_{RCD}$   
is greater than the specified  $t_{RCD}(max)$  limit, access time  
is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .

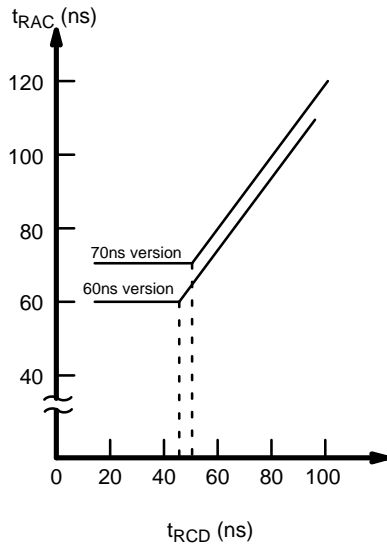
12.  $t_{RCD}(min) = t_{RAH}(min) + 2t_T + t_{ASC}(min)$ .
13. Operation within the  $t_{RAD}(max)$  limit ensures that  $t_{RAC}(max)$   
can be met.  $t_{RAD}(max)$  is specified as a reference point only; if  
 $t_{RAD}$  is greater than the specified  $t_{RAD}(max)$  limit, access time  
is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
14. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
15.  $t_{WCS}$  is specified as a reference point only. If  $t_{WCS} \geq t_{WCS}$   
(min)  
the data output pin will remain High-Z state through entire  
cycle.
16. Assumes that  $t_{WCS} < t_{WCS}(min)$ .
17. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
18.  $t_{CPA}$  is access time from the selection of a new column address  
(that

is caused by changing  $\overline{CAS}$  from "L" to "H"). Therefore, if  
 $t_{CP}$  is long,  $t_{CPA}$  is longer than  $t_{CPA}(max)$ .

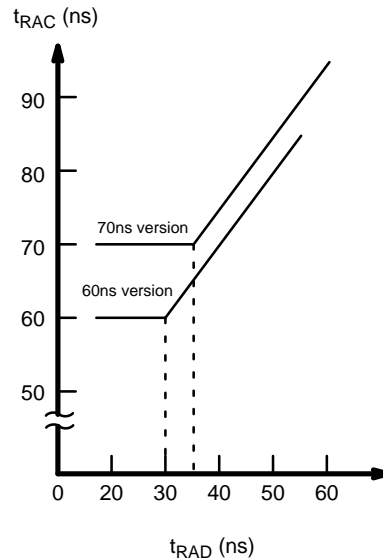
19. Assumes that  $\overline{CAS}$ -before- $\overline{RAS}$  refresh.
20.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$  and  $t_{AWD}$  are not restrictive operating  
parameters. They are included in the data sheet as an  
electrical characteristic only. If  $t_{WCS} > t_{WCS}(min)$ , the cycle is  
an early write cycle and  $D_{OUT}$  pin will maintain high impedance  
state through-out the entire cycle. If  $t_{CWD} > t_{CWD}(min)$ ,  $t_{RWD} >$   
 $t_{RWD}(min)$ , and  $t_{AWD} > t_{AWD}(min)$ , the cycle is a  
read-modify-write cycle and data from the selected cell will  
appear at the  $D_{OUT}$  pin. If neither of the above conditions is  
satisfied, the cycle is a delayed write cycle and invalid data will  
appear the  $D_{OUT}$  pin, and write operation can be executed by  
satisfying  $t_{RWL}$ ,  $t_{CWL}$ , and  $t_{RAL}$  specifications.



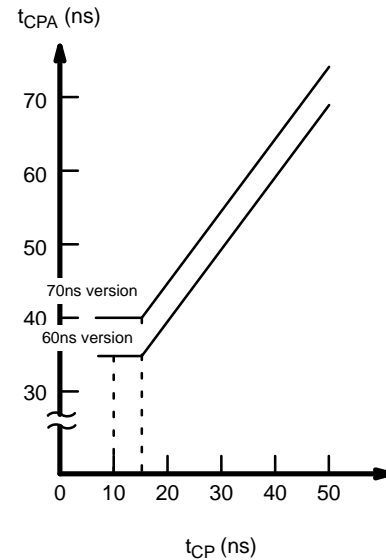
**Fig. 2 –  $t_{RAC}$  vs.  $t_{RCD}$**



**Fig. 3 –  $t_{RAC}$  vs.  $t_{RAD}$**



**Fig. 4 –  $t_{CPA}$  vs.  $t_{CP}$**



## FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input				Address		Input Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output		
Standby	H	H	X	X	–	–	–	High-Z	–	
Read Cycle	L	L	H	L	Valid	Valid	–	Valid	Yes*	$t_{RCS} \geq t_{RCS}(\text{min})$
Write Cycle (Early Write)	L	L	L	X	Valid	Valid	Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}(\text{min})$
Read-Modify-Write Cycle	L	L	H→L	L→H	Valid	Valid	Valid	Valid	Yes*	
$\overline{RAS}$ -only Refresh Cycle	L	H	X	X	Valid	–	–	High-Z	Yes*	
$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Cycle	L	L	X	X	–	–	–	High-Z	Yes*	$t_{CSR} \geq t_{CSR}(\text{min})$
Hidden Refresh Cycle	H→L	L	H→X	L	–	–	–	Valid	Yes*	Previous data is kept

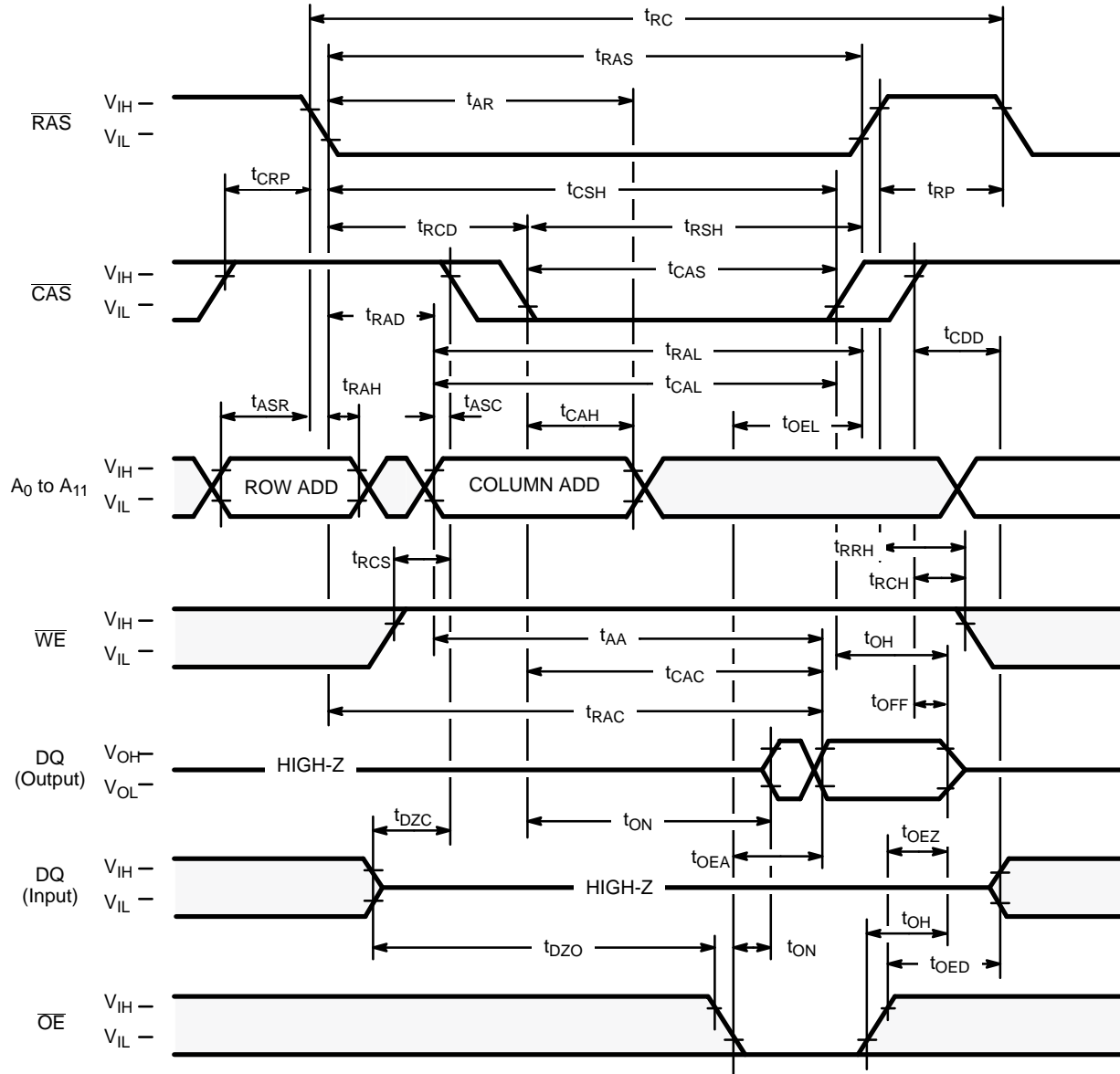
X; "H" or "L"

\*; It is impossible in Fast Page Mode.

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**Fig. 5 – READ CYCLE**



"H" or "L"

**DESCRIPTION**

To implement a read operation, a valid address is latched in by the  $\overline{RAS}$  and  $\overline{CAS}$  address strobes and with  $\overline{WE}$  set to a High level and  $\overline{OE}$  set to a low level, the output is valid once the memory access time has elapsed. The access time is determined by  $\overline{RAS}(t_{RAC})$ ,  $\overline{CAS}(t_{CAC})$ ,  $\overline{OE}(t_{OEA})$  or column addresses ( $t_{AA}$ ) under the following conditions:

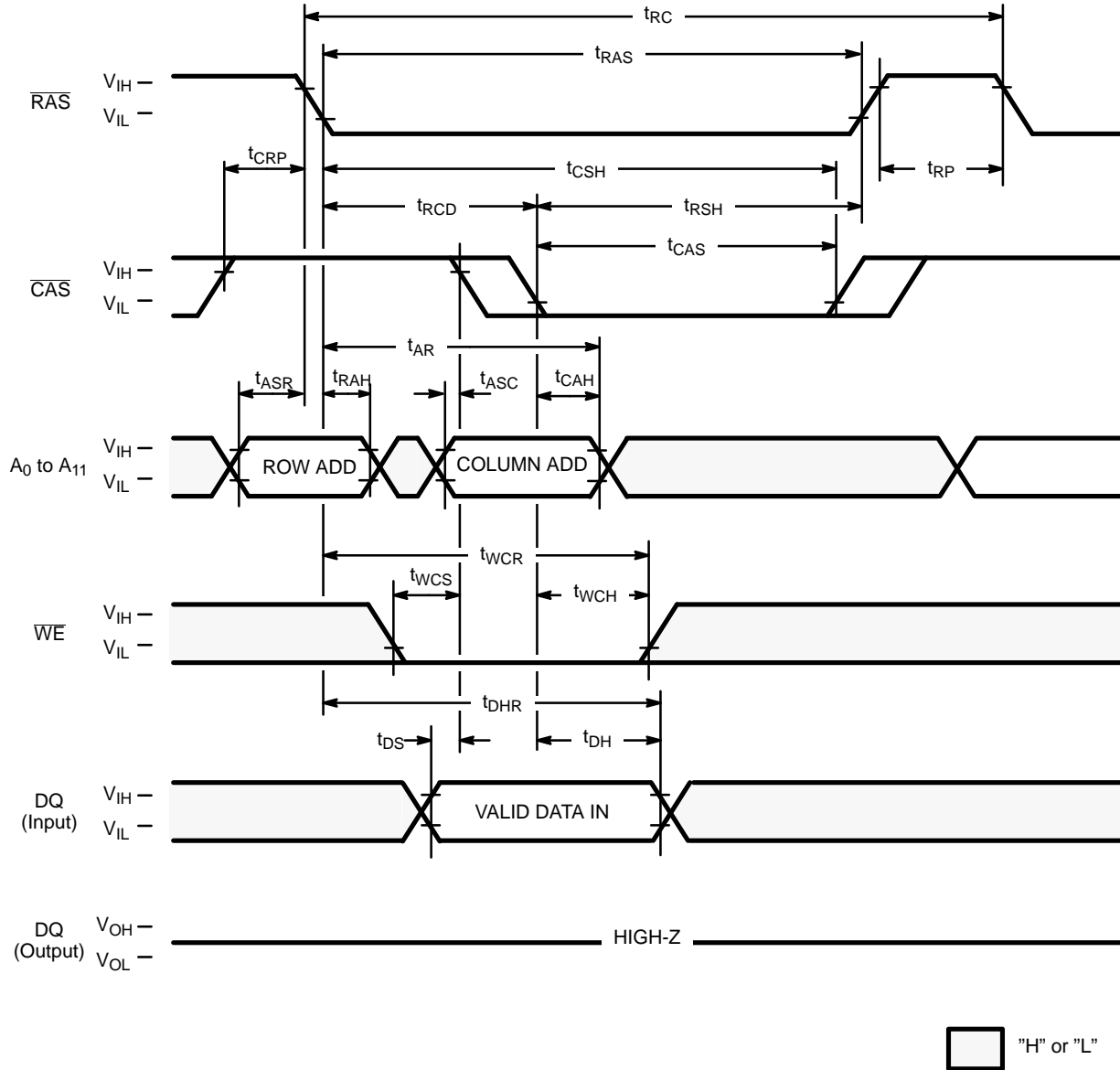
If  $t_{RCD} > t_{RCD}(\max)$ , access time =  $t_{CAC}$ .

If  $t_{RAD} > t_{RAD}(\max)$ , access time =  $t_{AA}$ .

If  $\overline{OE}$  is brought Low after  $t_{RAC}$ ,  $t_{CAC}$ , or  $t_{AA}$  (whichever occurs later), access time =  $t_{OEA}$ .

However, if either  $\overline{CAS}$  or  $\overline{OE}$  goes High, the output returns to a high-impedance state after  $t_{OH}$  is satisfied.

**Fig. 6 – EARLY WRITE CYCLE ( $\overline{OE}$  = "H" or "L")**



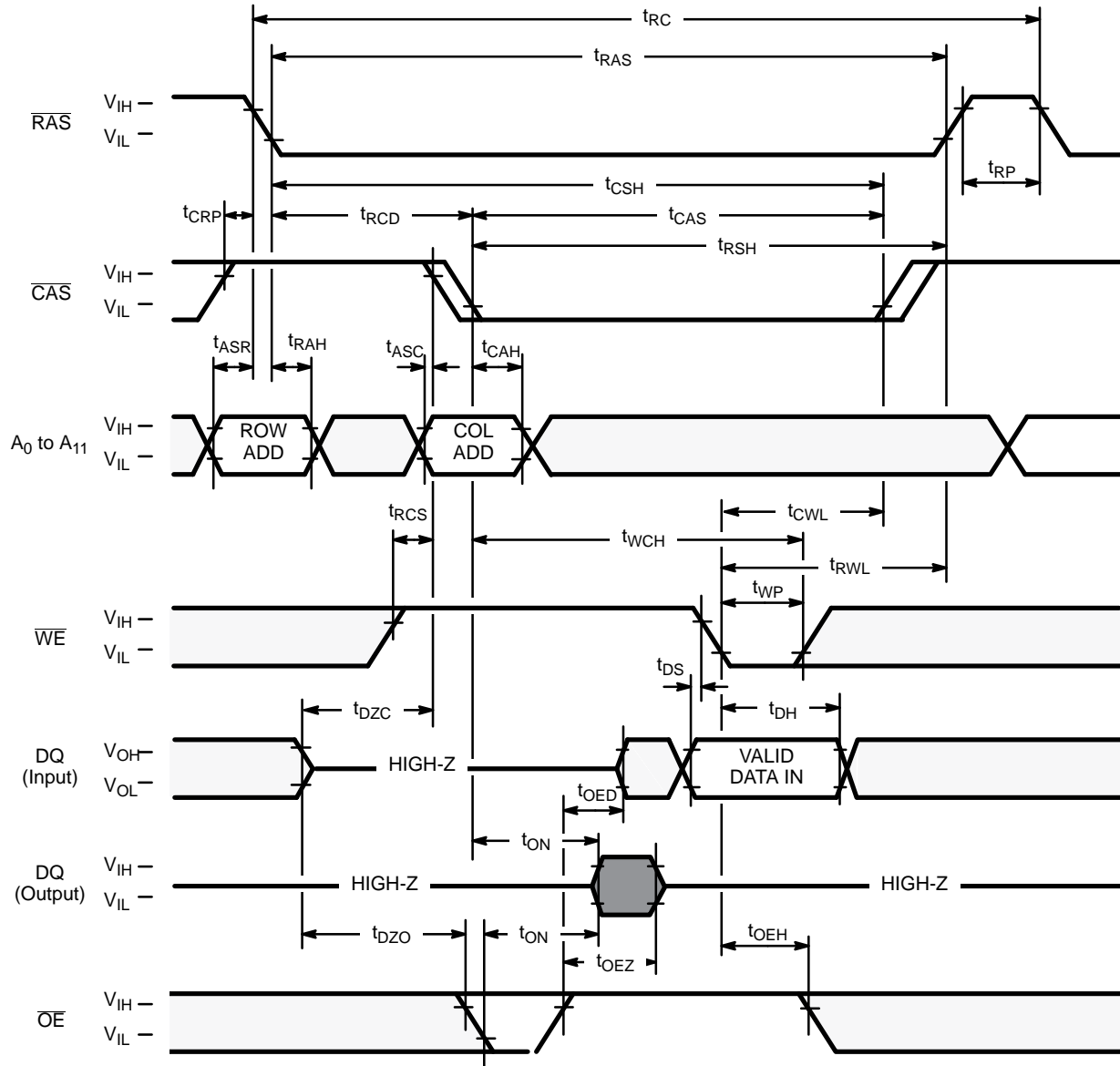
### DESCRIPTION

A write cycle is similar to a read cycle except  $\overline{WE}$  is set to a Low state and  $\overline{OE}$  is an "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, delayed write, or read-modify-write. During all write cycles, timing parameters  $t_{RWL}$ ,  $t_{CWL}$  and  $t_{RAL}$  must be satisfied. In the early write cycle shown above  $t_{WCS}$  satisfied, data on the DQ pin is latched with the falling edge of  $\overline{CAS}$  and written into memory.

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**Fig. 7 – DELAYED WRITE CYCLE**

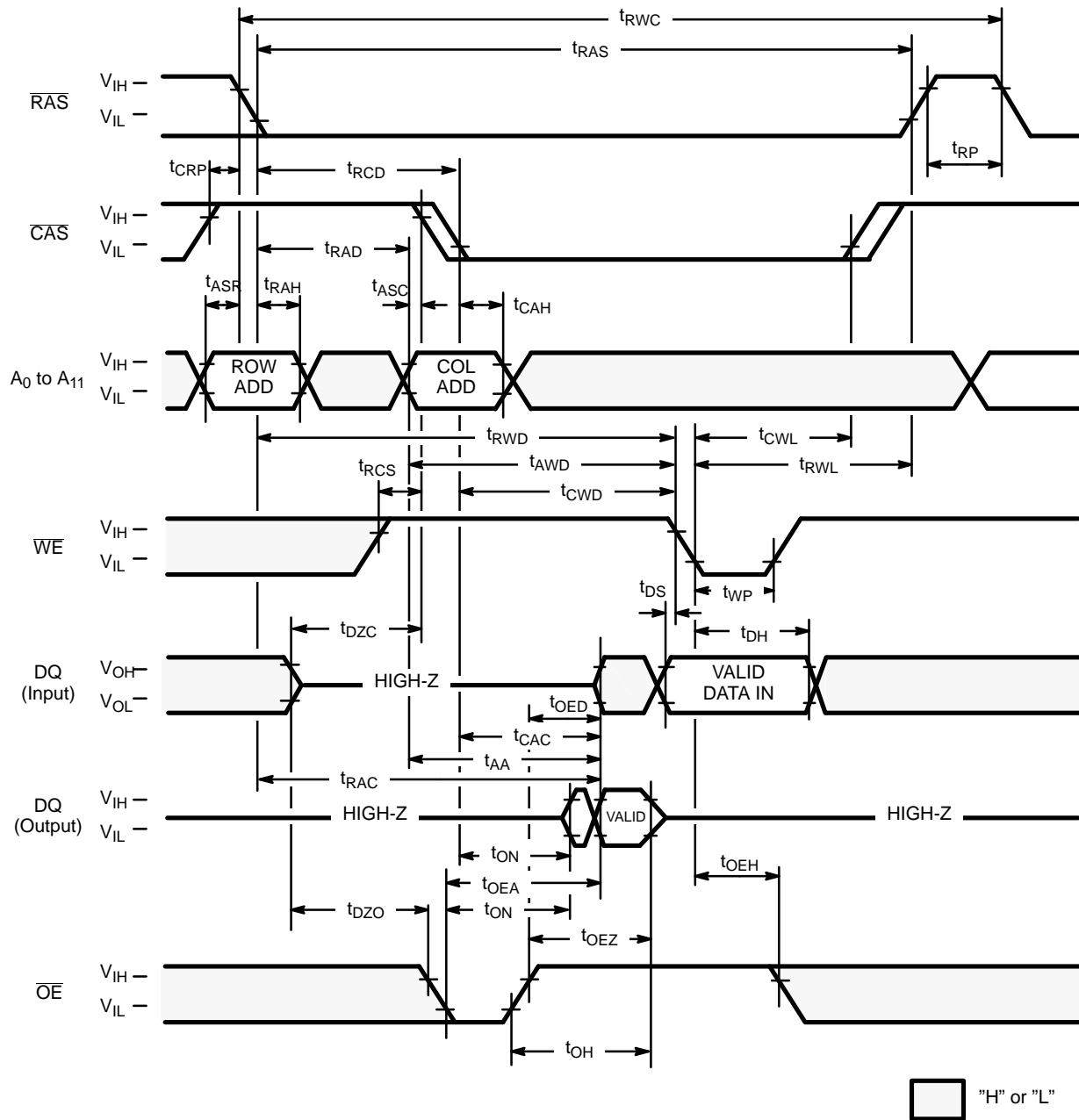


"H" or "L"  
 Invalid Data

**DESCRIPTION**

In the Delayed write cycle,  $t_{\text{WCS}}$  is not satisfied; thus, the data on the DQ pins is latched with the falling edge of  $\overline{\text{WE}}$  and written into memory. The Output Enable ( $\overline{\text{OE}}$ ) signal must be changed from Low to High before  $\overline{\text{WE}}$  goes Low ( $t_{\text{OED}} + t_{\text{DS}}$ ).

**Fig. 8 – READ-MODIFY-WRITE-CYCLE**



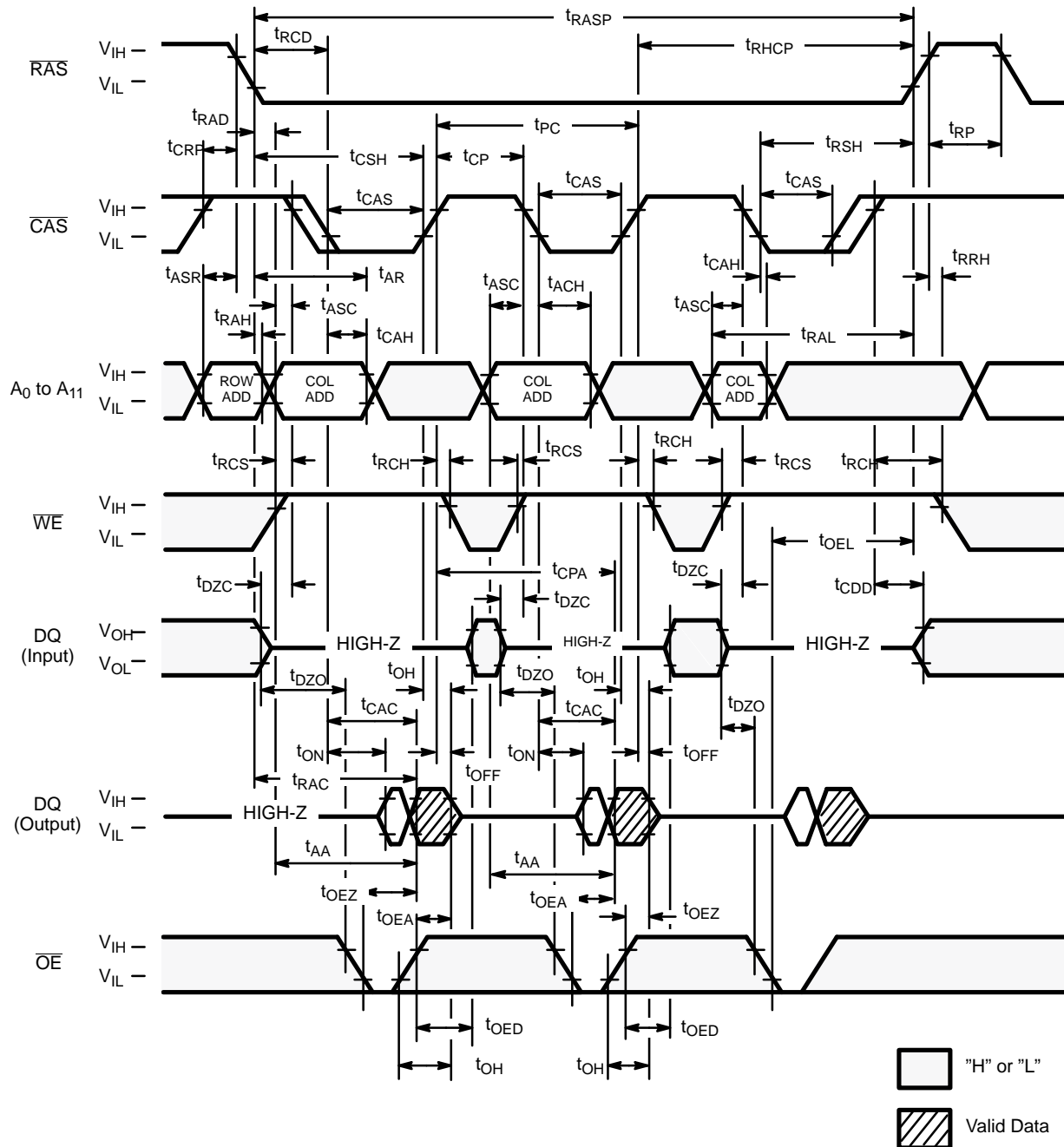
**DESCRIPTION**

The read-modify-write cycle is executed by changing  $\overline{WE}$  from High to Low after the data appears on the DQ pins. In the read-modify-write cycle,  $\overline{OE}$  must be changed from Low to High after the memory access time.

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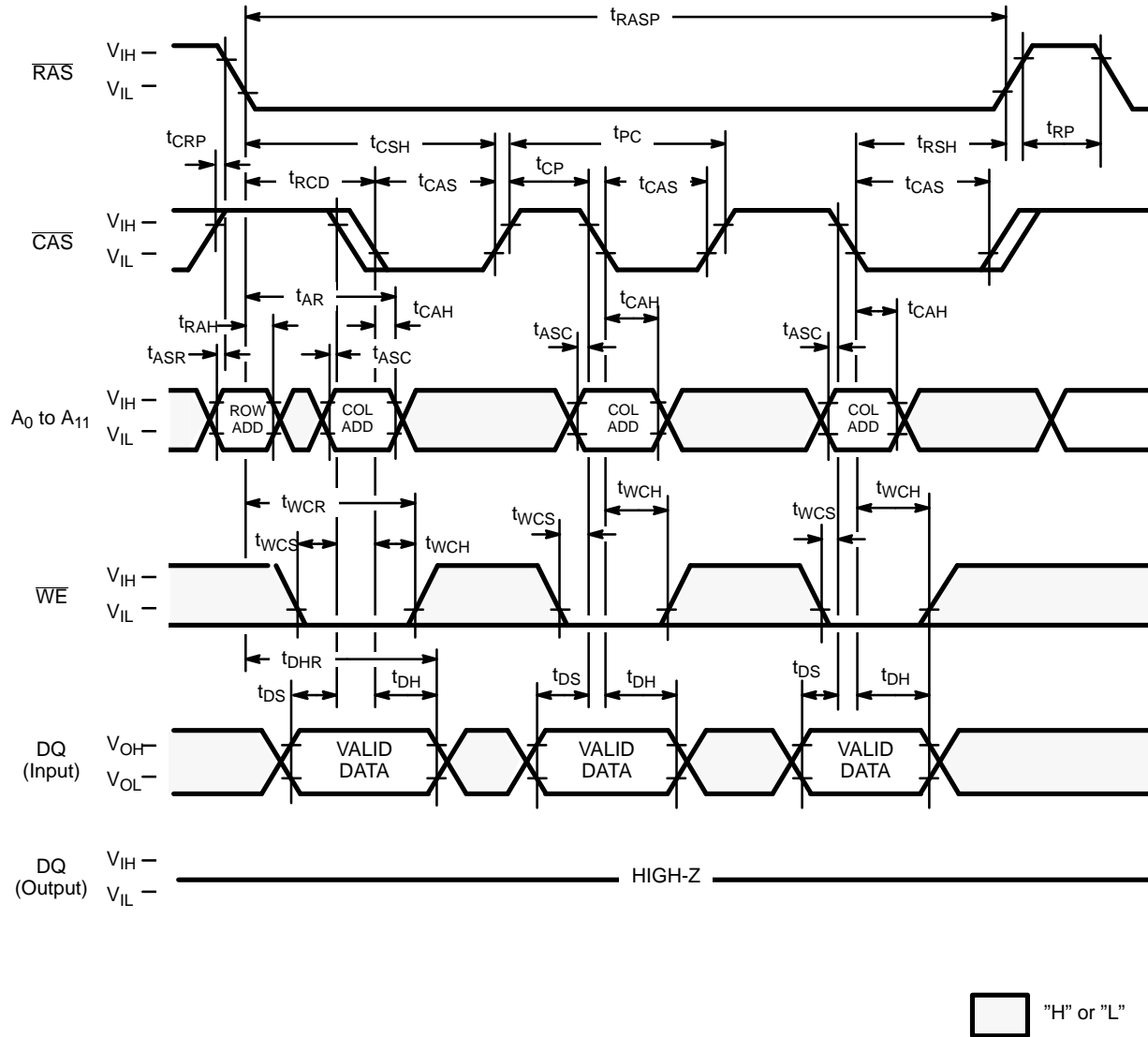
**Fig. 9 – FAST PAGE MODE READ CYCLE**



**DESCRIPTION**

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining  $\overline{RAS}$  at a Low level and  $\overline{WE}$  at a High level during all successive memory cycles in which the row address is latched. The address time is determined by  $t_{CAC}$ ,  $t_{AA}$ ,  $t_{CPA}$ , or  $t_{OEA}$ , whichever one is the latest in occurring.

**Fig. 10 – FAST PAGE MODE EARLY WRITE CYCLE ( $\overline{OE}$  = "H" or "L")**



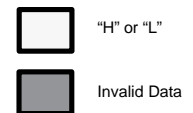
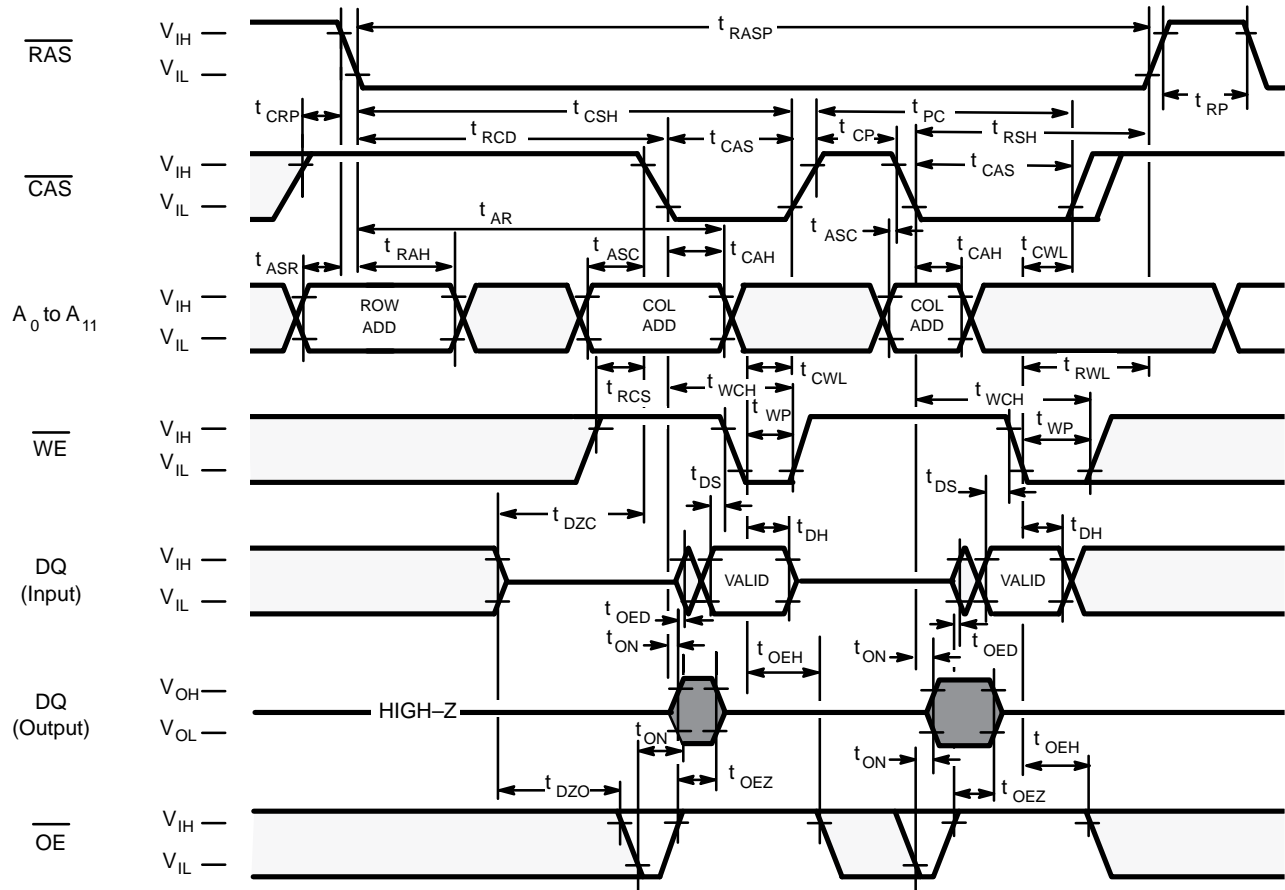
## DESCRIPTION

The fast page mode early write cycle is executed in the same manner as the fast page mode read cycle except the states of  $\overline{WE}$  and  $\overline{OE}$  are reversed. Data appearing on the  $DQ$  pins is latched on the falling edge of  $\overline{CAS}$  and written into memory. During the fast page mode early write cycle, including the delayed ( $\overline{OE}$ ) write and read-modify-write cycles,  $t_{CWL}$  must be satisfied.

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**Fig. 11 – FAST PAGE MODE DELAYED WRITE CYCLE**

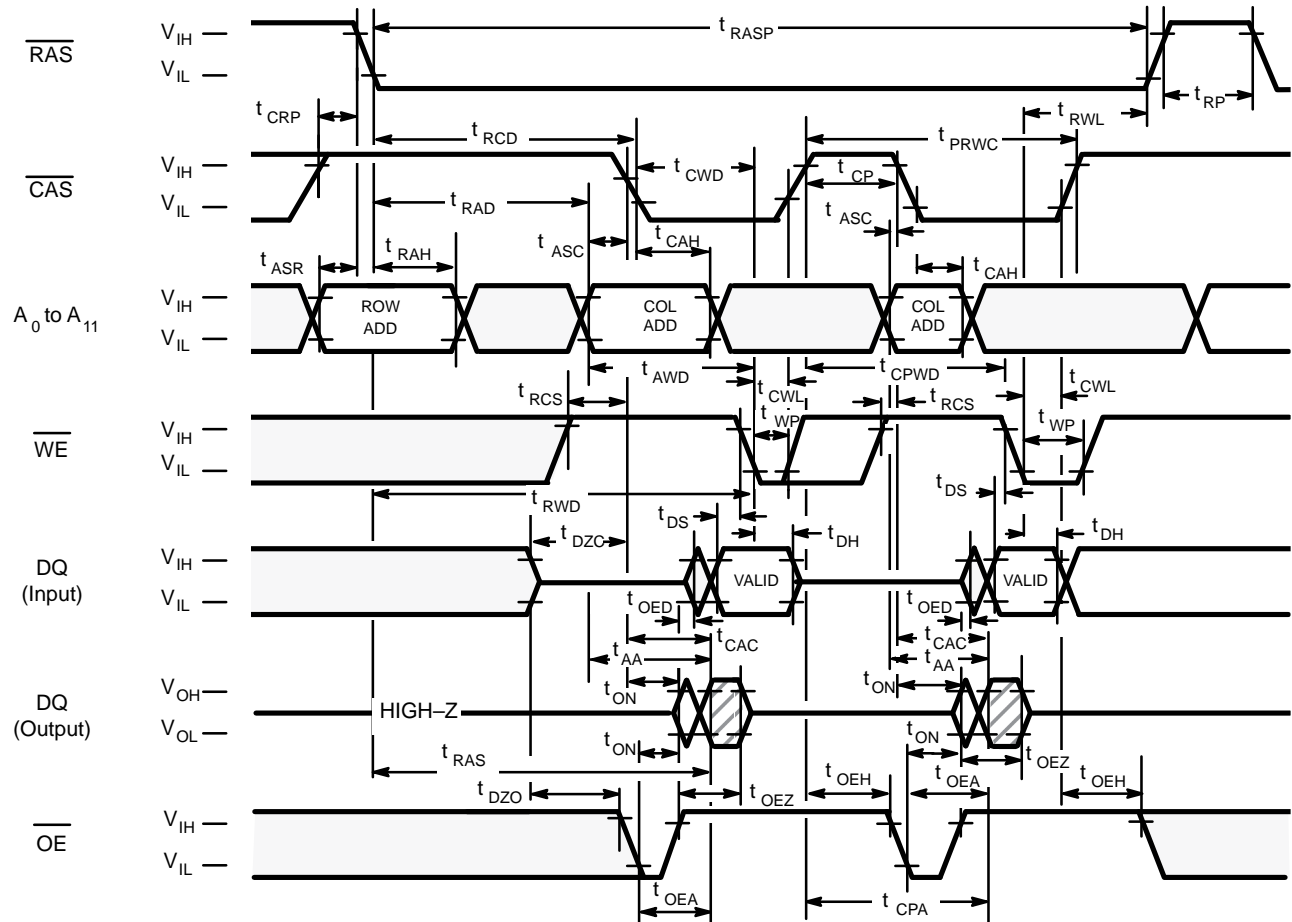


**DESCRIPTION**

The fast page mode delayed write cycle is executed in the same manner as the fast page mode early write cycle except for the states of  $\overline{WE}$  and  $\overline{OE}$ . Input data on the DQ pins are latched on the falling edge of  $\overline{WE}$  and written into memory. In the fast page mode delayed write cycle,  $\overline{OE}$  must be changed from Low to High before  $\overline{WE}$  goes Low ( $t_{OED} + t_r + t_{DS}$ ).



**Fig. 12 Fast Page Mode Read Modify Write Cycle**

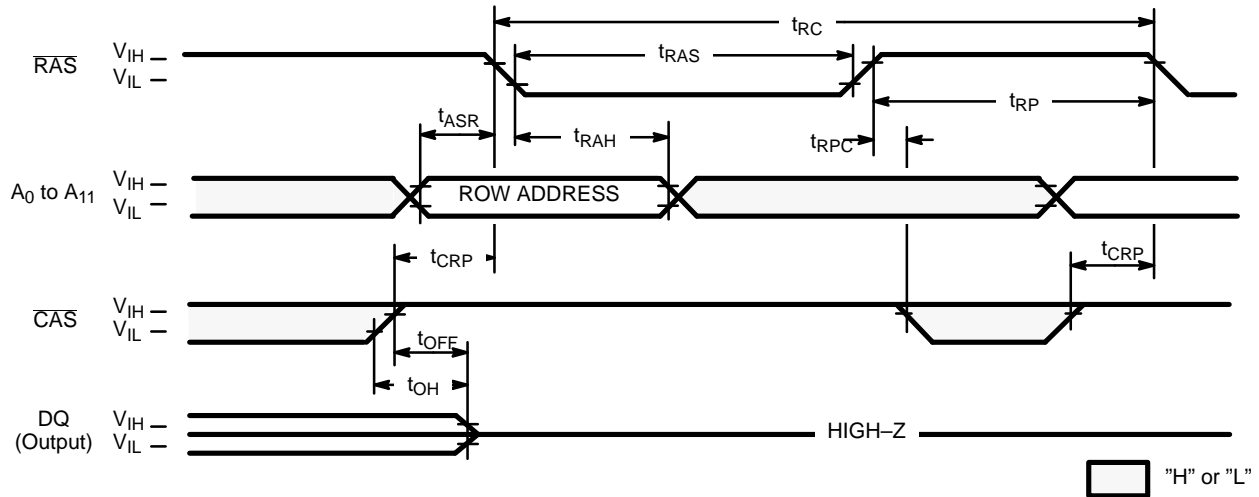


## DESCRIPTION

During the fast page mode of operation, the read-modify-write cycle can be executed by switching  $\overline{WE}$  from High to Low after input data appears at the DQ pins during a normal cycle.

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**Fig. 13 – RAS-ONLY REFRESH ( $\overline{WE} = \overline{OE} = \text{"H" or "L"}$ )**

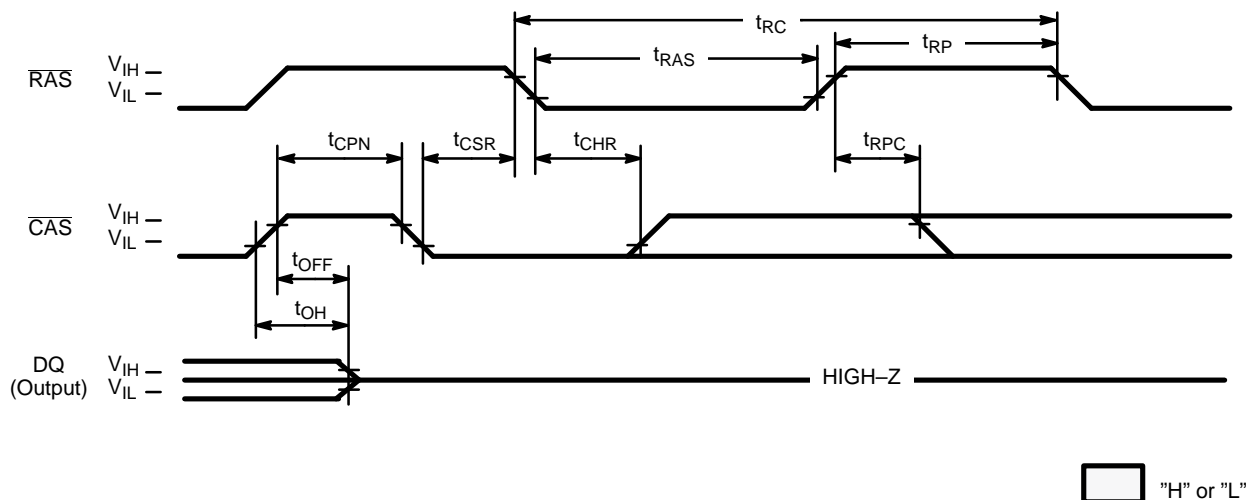


#### DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 4096 row addresses every 65.6-milliseconds. Three refresh modes are available: RAS-only refresh,  $\overline{CAS}$ -before-RAS refresh, and hidden refresh.

$\overline{RAS}$ -only refresh is performed by keeping  $\overline{RAS}$  Low and  $\overline{CAS}$  High throughout the cycle; the row address to be refreshed is latched on the falling edge of  $\overline{RAS}$ . During  $\overline{RAS}$ -only refresh,  $D_{OUT}$  pins are kept in a high-impedance state.

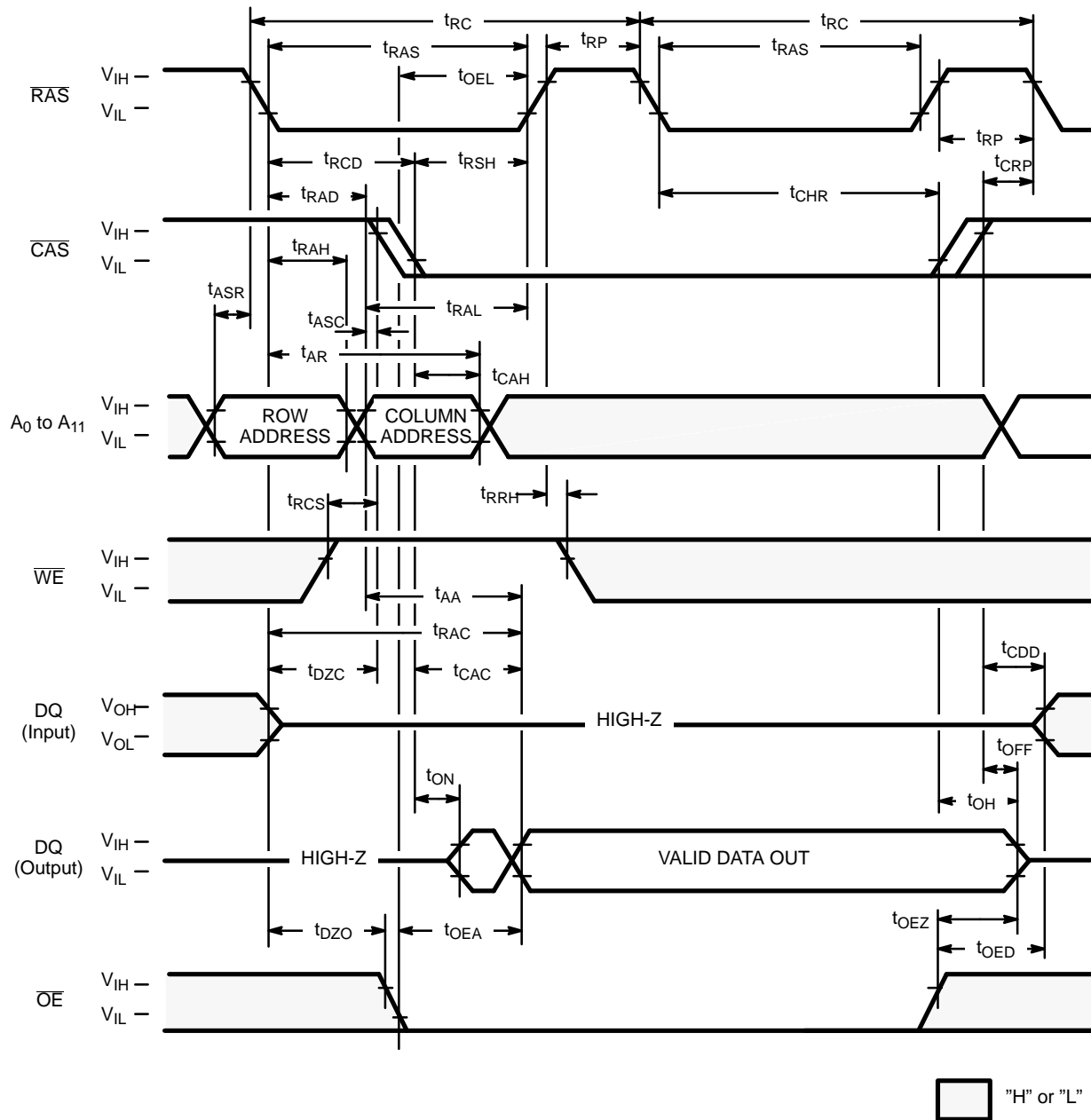
**Fig. 14 –  $\overline{CAS}$ -BEFORE- $\overline{RAS}$  REFRESH (ADDRESSES =  $\overline{WE} = \overline{OE} = \text{"H" or "L"}$ )**



#### DESCRIPTION

$\overline{CAS}$ -before- $\overline{RAS}$  refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{CAS}$  is held Low for the specified setup time ( $t_{CSR}$ ) before  $\overline{RAS}$  goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next  $\overline{CAS}$ -before- $\overline{RAS}$  refresh operation.

**Fig. 15 – HIDDEN REFRESH CYCLE**



### DESCRIPTION

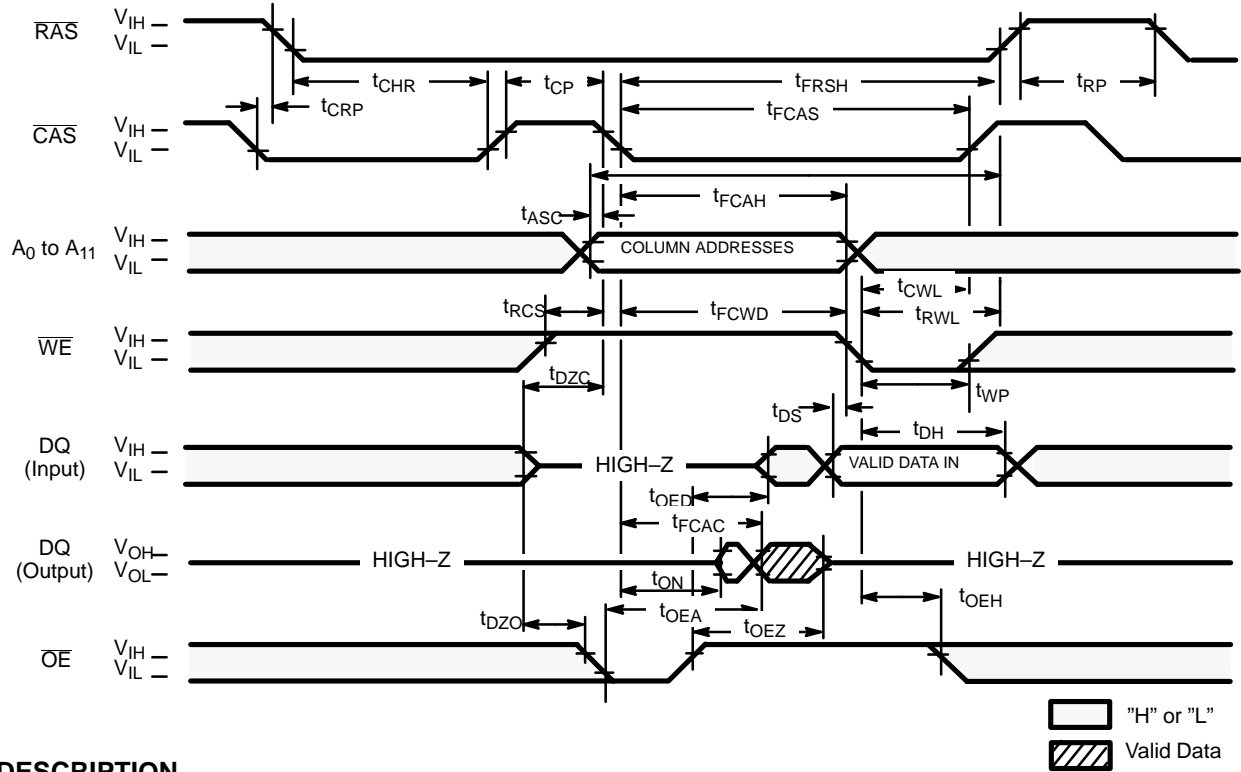
A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of  $\overline{CAS}$  and cycling RAS. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have  $\overline{CAS}$ -before- $\overline{RAS}$  refresh capability.

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**Fig. 16 –  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH COUNTER TEST CYCLE**



## DESCRIPTION

A special timing sequence using the  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test cycle provides a convenient method to verify the function of  $\text{CAS}$ -before- $\text{RAS}$  refresh circuitry. If, a  $\text{CAS}$ -before- $\text{RAS}$  refresh cycle  $\text{CAS}$  makes a transition from High to Low while  $\text{RAS}$  is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A0 through A11 are defined by the on-chip refresh counter.

Column Address: Bits A0 through A8 are defined by latching levels on A0–A8 at the second falling edge of  $\overline{\text{CAS}}$ .

The  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Counter Test procedure is as follows;

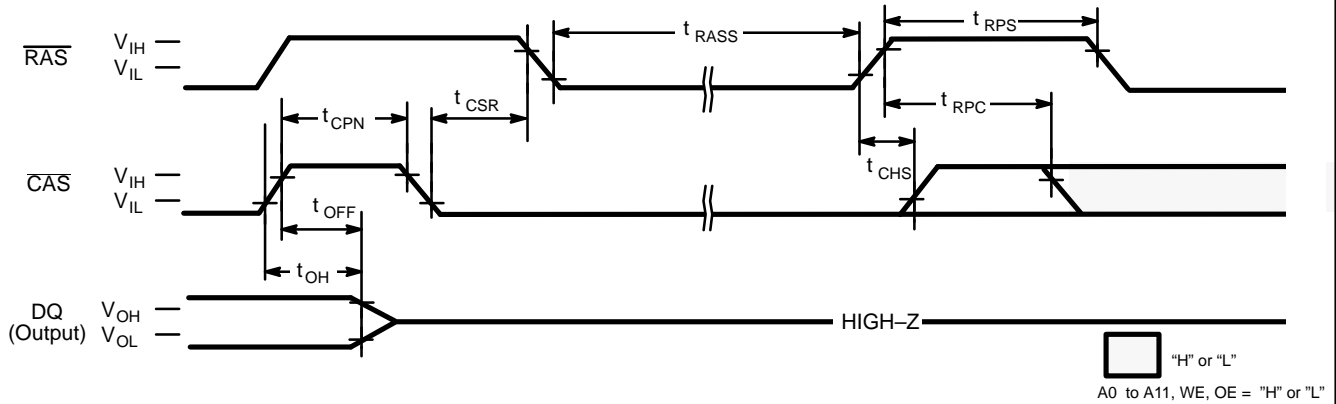
- 1) Initialize the internal refresh address counter by using 8  $\overline{\text{RAS}}$  only refresh cycles.
- 2) Use the same column address throughout the test.
- 3) Write "0" to all 4096 row addresses at the same column address by using normal write cycles.
- 4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test (read-modify-write cycles). Repeat this procedure 4096 times with addresses generated by the internal refresh address counter.
- 5) Read and check data written in procedure 4) by using normal read cycle for all 4096 memory locations.
- 6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB8116800A-60		MB8116800A-70		Unit
			Min	Max	Min	Max	
90	Access Time from $\overline{\text{CAS}}$	$t_{\text{FCAC}}$	—	50	—	55	ns
91	Column Address Hold Time	$t_{\text{FCAH}}$	35	—	35	—	ns
92	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{FCWD}}$	70	—	77	—	ns
93	$\overline{\text{CAS}}$ Pulse width	$t_{\text{FCAS}}$	90	—	99	—	ns
94	$\overline{\text{RAS}}$ Hold Time	$t_{\text{FRSH}}$	90	—	99	—	ns

Note: Assumes that  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test cycle only.

**Fig. 17 – SELF REFRESH CYCLE (A0–A11 =  $\overline{WE}$  =  $\overline{OE}$  = "H" or "L")**



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB8116800A-60		MB8116800A-70		Unit
			Min	Max	Min	Max	
100	$\overline{RAS}$ Pulse Width	$t_{RASS}$	100	—	100	—	$\mu s$
101	$\overline{RAS}$ Precharge Time	$t_{RPS}$	110	—	125	—	ns
102	$\overline{CAS}$ Hold Time	$t_{CHS}$	–50	—	–50	—	ns

Note . Assumes self refresh cycle only

### DESCRIPTION

The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter and timing generator. If  $\overline{CAS}$  goes to "L" before  $\overline{RAS}$  goes to "L" (CBR) and the condition of  $\overline{CAS}$  "L" and  $\overline{RAS}$  "L" is kept for term of  $t_{RASS}$  (more than 100 $\mu s$ ), the device can enter the self refresh cycle. Following that, refresh operation is automatically executed at fixed intervals using internal refresh address counter during " $\overline{RAS}$ =L" and " $\overline{CAS}$ =L".

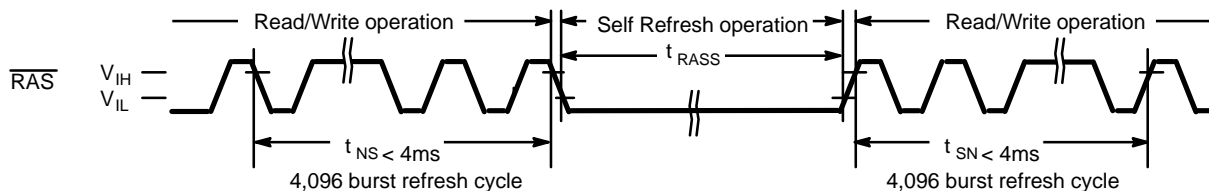
Exit from self refresh cycle is performed by toggling  $\overline{RAS}$  and  $\overline{CAS}$  to "H" with specified  $t_{CHS}$  min.. In this time,  $\overline{RAS}$  must be kept "H" with specified  $t_{RPS}$  min..

Using self refresh mode, data can be retained without external  $\overline{CAS}$  signal during system is in standby.

Restriction for Self Refresh operation ;

For self refresh operation, the notice below must be considered.

- 1) In the case that distributed CBR refresh are operated between read/write cycles  
Self refresh cycles can be executed without special rule if 4,096 cycles of distributed CBR refresh are executed within  $t_{REF}$  max..
- 2) In the case that burst CBR refresh or distributed/burst /RAS only refresh are operated between read/write cycles  
4,096 times of burst CBR refresh or 4,096 times of burst /RAS only refresh must be executed before and after Self refresh cycles.



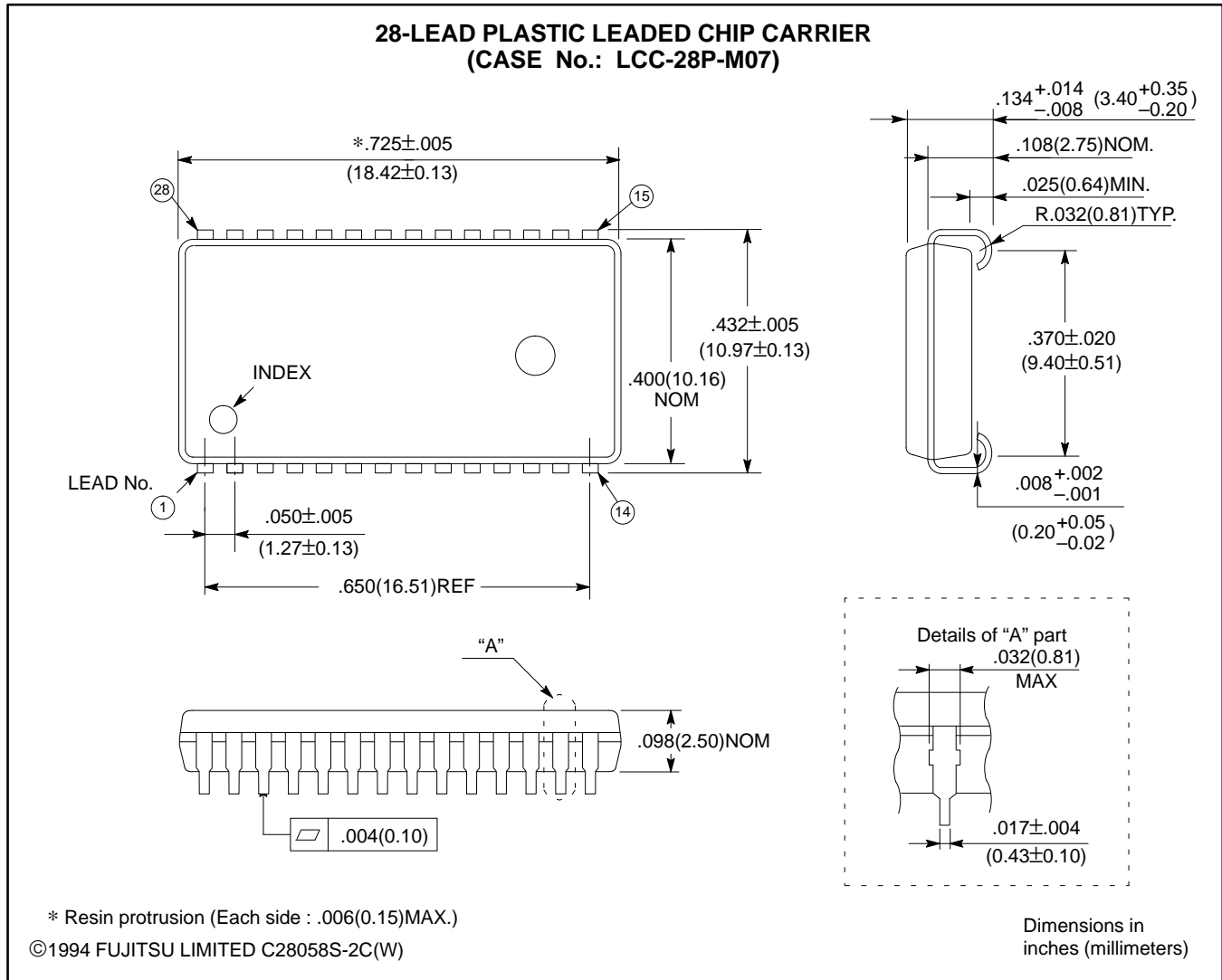
\* read/write operation can be performed non refresh time within  $t_{NS}$  or  $t_{SN}$

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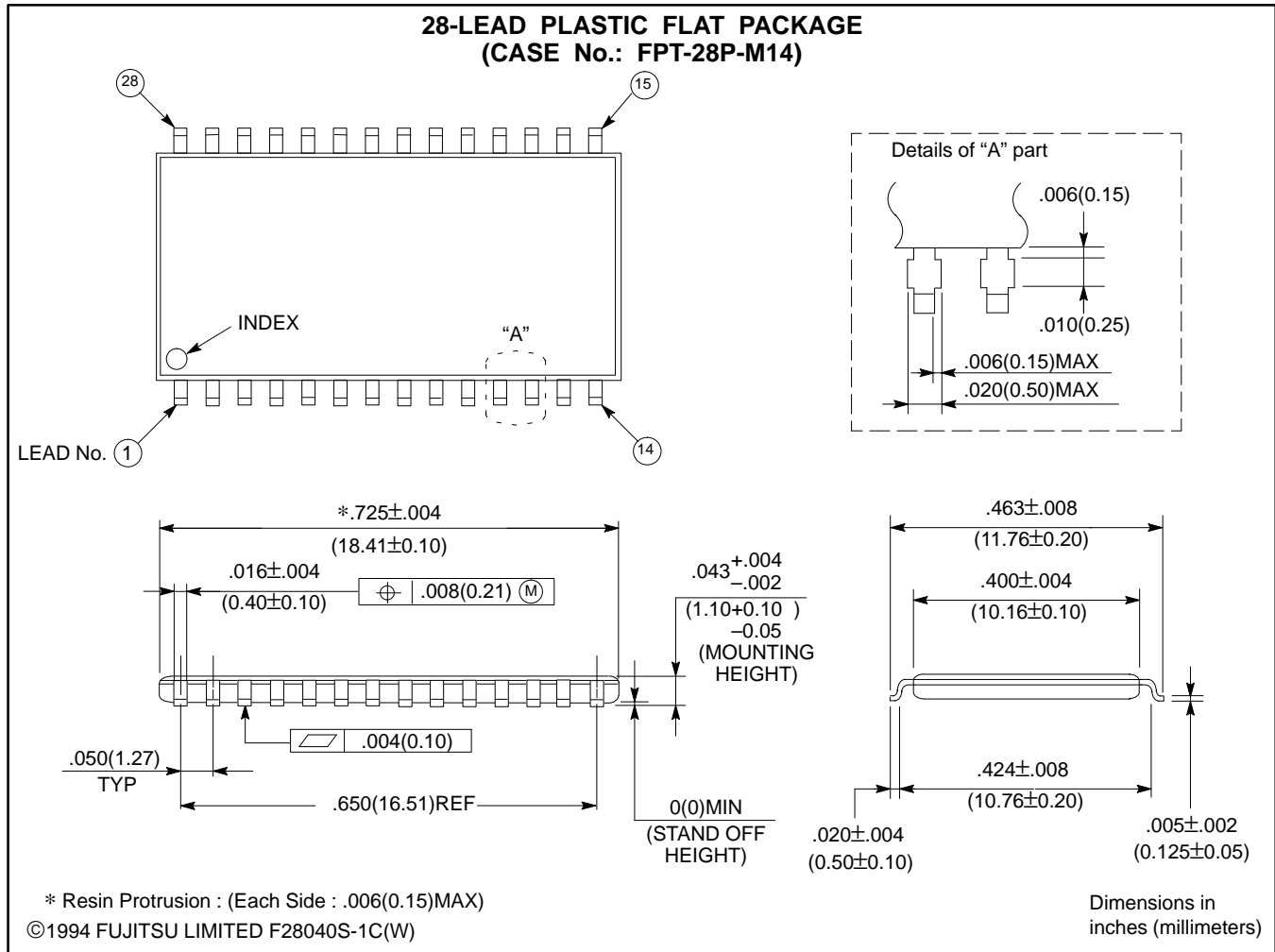
## PACKAGE DIMENSIONS

(Suffix: -PJ)



## PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN)



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