

# MB1518

## Serial Input PLL Frequency Synthesizer With On-Chip 2.5GHz Prescaler

The Fujitsu MB1518 with an on chip 2.5 GHz dual modulus prescaler is a serial input PLL (Phase Locked Loop) frequency synthesizer with pulse swallow function. It is well suited for BS tuner, CATV system applications.

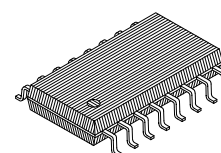
It operates supply voltage of 5.0V typ. and dissipates 16mA typ. of current realized through the use of Fujitsu's unique U-ESBIC Bi-CMOS technology.

- Power supply voltage:  $V_{CC} = 4.5$  to  $5.5V$
- High operating frequency:  $f_{in} = 2.5GHz$  ( $P_{in} = -4dBm$ )
- 2.5GHz dual modulus prescaler:  $P = 512/528$
- Low power supply current:  $I_{CC} = 16mA$  typ.
- Programmable reference divider :  $R = 512$
- Programmable divider consisting of:  
Binary 5-bit swallow counter ( $A = 0$  to  $31$ )  
Binary 9-bit programmable counter ( $N = 32$  to  $511$ )
- Wide operating temperature:  $T_a = -40$  to  $+85^{\circ}C$
- Plastic 16-pin flat package (Suffix: -PF)

### ABSOLUTE MAXIMUM RATINGS (see NOTE)

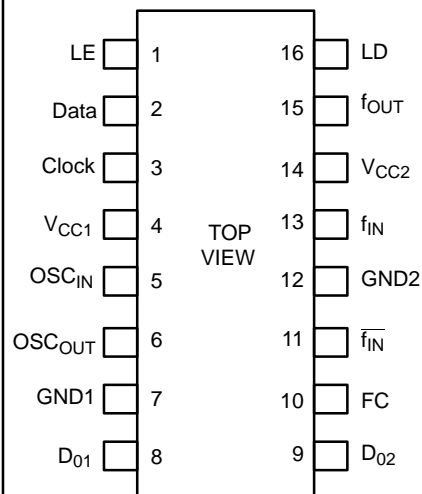
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	$-0.5$ to $7.0$	V
Output Voltage	$V_O$	$0.5$ to $V_{CC} + 0.5$	V
Output Current	$I_O$	$\pm 10$	mA
Storage Temperature	$T_{STG}$	$-55$ to $+125$	$^{\circ}C$

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



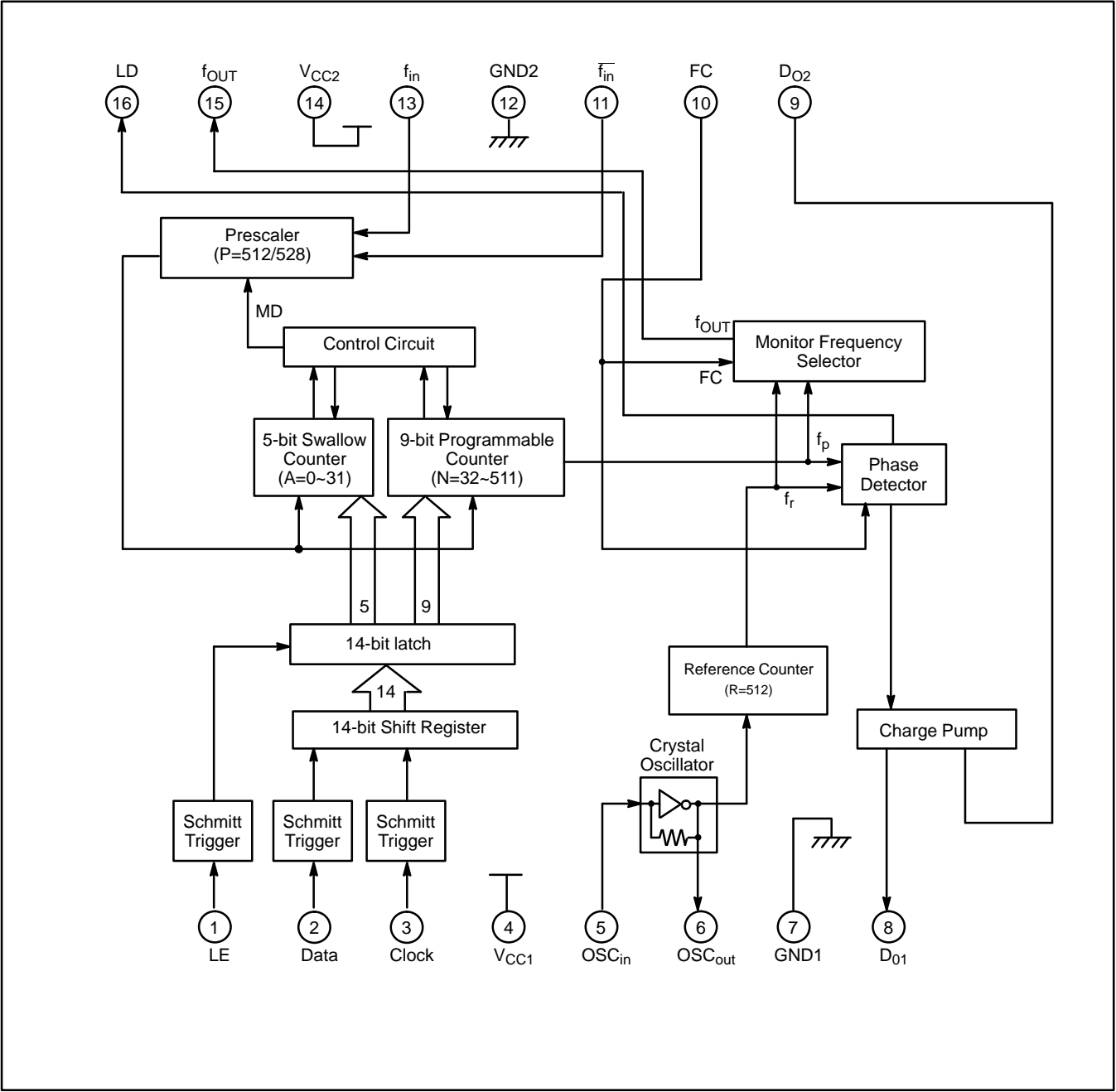
**PLASTIC PACKAGE**  
**FPT-16P-M06**

### PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



## PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions						
1	LE	I	Load enable input pin. This pin involves a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch.						
2	Data	I	Serial data of binary code input pin. This pin involves a schmitt trigger circuit.						
3	Clock	I	Clock input pin of the 14–bit shift register. This pin involves a schmitt trigger circuit. On rising edge of the clock shifts one bit of the data into the shift register.						
4	V <sub>CC1</sub>	–	PLL power supply voltage input pin.						
5 6	OSC <sub>IN</sub> OSC <sub>OUT</sub>	I O	Oscillator input pin. Oscillator output pin. A crystal is connected between OSC <sub>IN</sub> pin and OSC <sub>OUT</sub> pin.						
7	GND1	–	PLL ground pin.						
8 9	D <sub>O1</sub> D <sub>O2</sub>	O O	Charge pump output pins. Phase characteristics can be reversed depending upon FC pin input level.						
10	FC	I	Phase select input pin of the phase detector. This pin involves an internal pull up resistor. When this pin is low, characteristics of the charge pump and phase detector can be reversed. This input also selects f <sub>OUT</sub> pin output level, either fr or fp. Please see on page 6.						
11	$\overline{f}_{in}$	I	Complementary input pin of f <sub>in</sub> . Please connect to GND through a capacitor.						
12	GND2	–	Prescaler ground pin.						
13	f <sub>in</sub>	I	Prescaler input pin, This signal is input with AC coupled.						
14	V <sub>CC2</sub>	–	Prescaler power supply voltage input pin.						
15	f <sub>OUT</sub>	O	Monitor pin of the phase detector input. f <sub>OUT</sub> pin outputs either of the programmable reference divider output frequency fr or programmable divider output frequency fp depending upon the FC pin input level. <table><tr><td>FC pin</td><td>f<sub>out</sub> output signal</td></tr><tr><td>H</td><td>fr</td></tr><tr><td>L</td><td>fp</td></tr></table>	FC pin	f <sub>out</sub> output signal	H	fr	L	fp
FC pin	f <sub>out</sub> output signal								
H	fr								
L	fp								
16	LD	O	Phase detector output pin. Normally this pin outputs high. While the phase difference between fr and fp exists, this pin outputs low.						

# FUNCTIONAL DESCRIPTIONS

## DIVIDE RATIO SETTING

Divide ratio can be set using the following equation:

$$f_{VCO} = \{(P \times N) + (16 \times A)\} \times f_{OSC} \div R$$

$f_{VCO}$ : Output frequency of an external voltage controlled oscillator (VCO)

P: Preset divide ratio of an internal dual modulus prescaler (512)

N: Preset divide ratio of binary 9-bit programmable counter (32 to 511)

A: Preset divide ratio of binary 5-bit swallow counter (0 to 31)

$f_{OSC}$ : Reference oscillator frequency

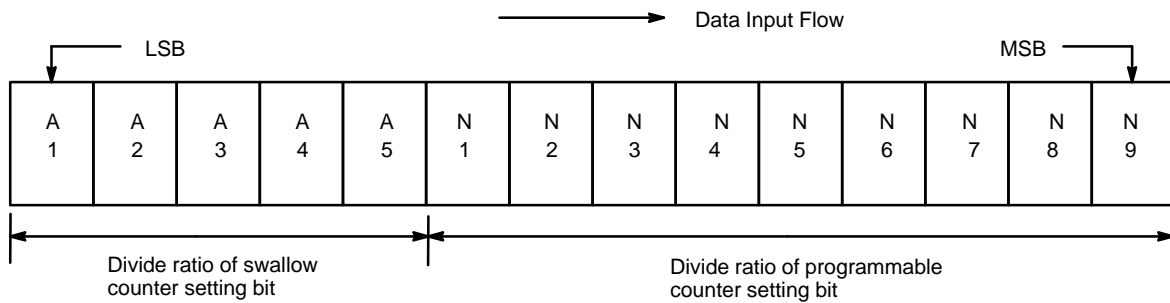
R: Preset divide ratio of reference counter (512)

## SERIAL DATA INPUT

On rising edge of the clock shifts one bit of the data into the shift register.

When the load enable is high, the data stored in the shift register is transferred to the latch.

14 bit of serial data format is shown below.



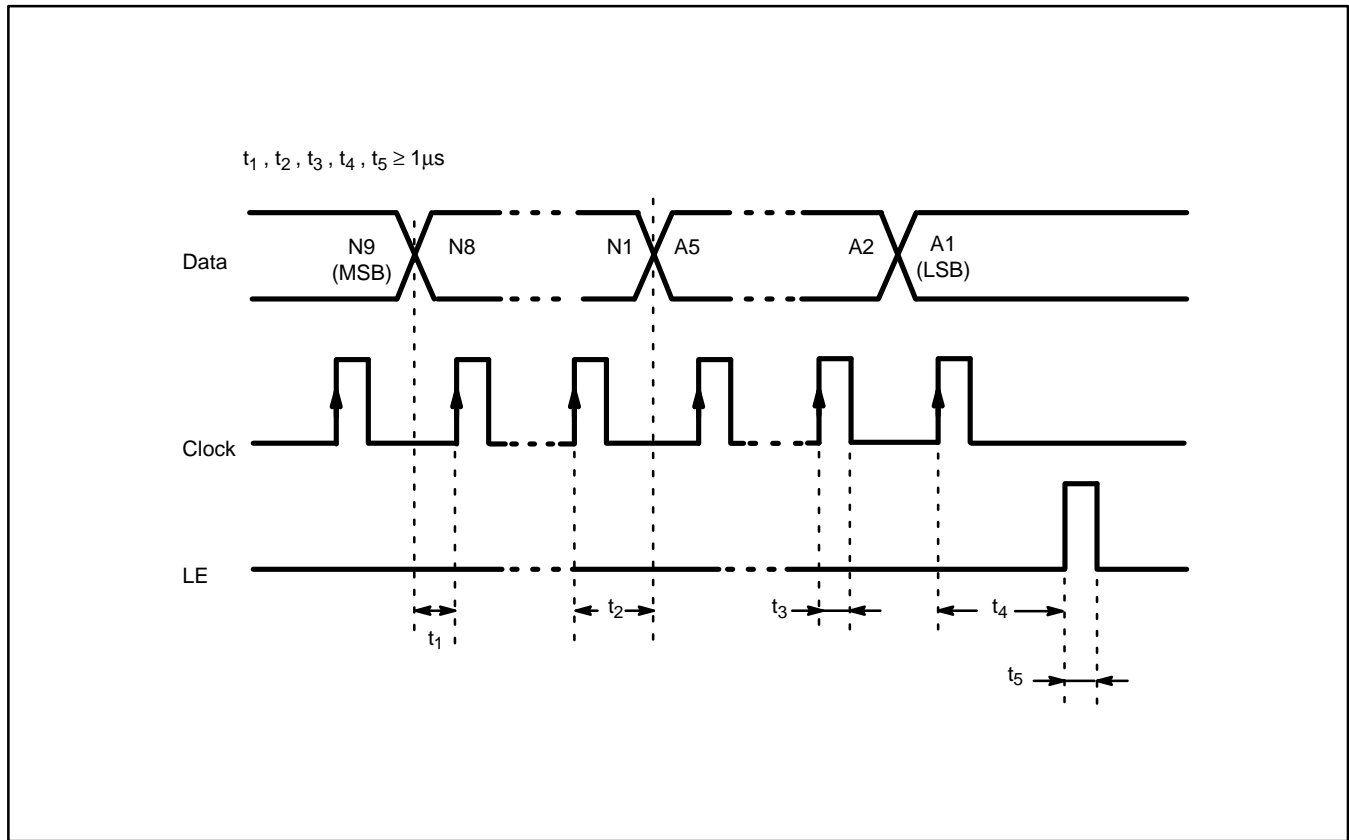
5-bit swallow counter divide ratio (A1 to A5)

Divide ratio A	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
:	:	:	:	:	:
31	1	1	1	1	1

9-bit programmable counter divide ratio (N1 to N9)

Divide ratio	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
32	0	0	0	1	0	0	0	0	0
33	0	0	0	1	0	0	0	0	1
34	0	0	0	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:	:
511	1	1	1	1	1	1	1	1	1

## SERIAL DATA INPUT TIMING



**Note:** On rising edge of the clock shifts one bit of the data into the shift register.  
When LE is high, the data stored the shift register is transferred into the latch.

PHASE DETECTOR CHARACTERISTICS

FC pin selects the phase of the phase detector. Phase characteristics (chage pump output) can be reversed depending upon the FC pin input level. Monitor pin (fout) output level is selected by the FC pin input level as well.

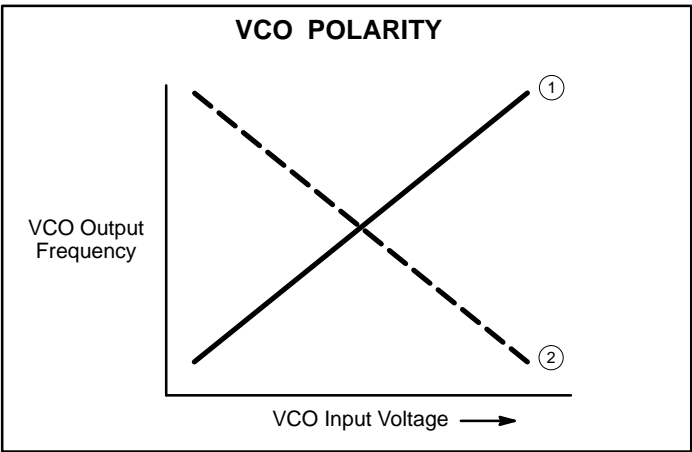
	FC = H (or open)		FC = L	
	D <sub>01</sub> , D <sub>02</sub>	f <sub>out</sub>	D <sub>01</sub> , D <sub>02</sub>	f <sub>out</sub>
fr > fp	H	Outputs programmable reference divider output frequency fr.	L	Outputs programmable divider output frequency fp.
fr = fp	Z		Z	
fr < fp	L		H	

Note:

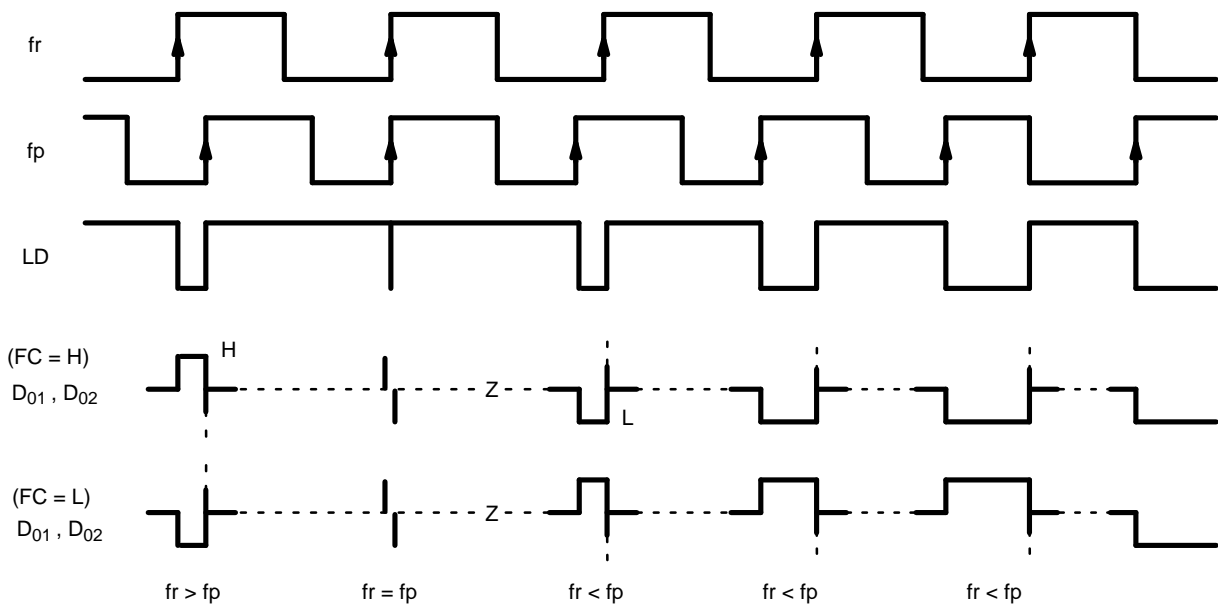
Z: High-impedance

Depending upon the VCO polarity, FC pin should be set accordingly.

When VCO polarity is like 1,  
FC should be set high or open.  
When VCO polarity is like 2,  
FC should be set low.



PHASE DETECTOR WAVEFORM



Note: Phase difference detection range :  $-2\pi$  to  $+2\pi$

Spike shape depends on the charge pump characteristics.  
The spike is output to diminish the dead band.

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Input Voltage	V <sub>I</sub>	GND	–	V <sub>CC</sub>	V
Operating Temperature	T <sub>a</sub>	–40	–	+85	°C

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

## ELECTRICAL CHARACTERISTICS

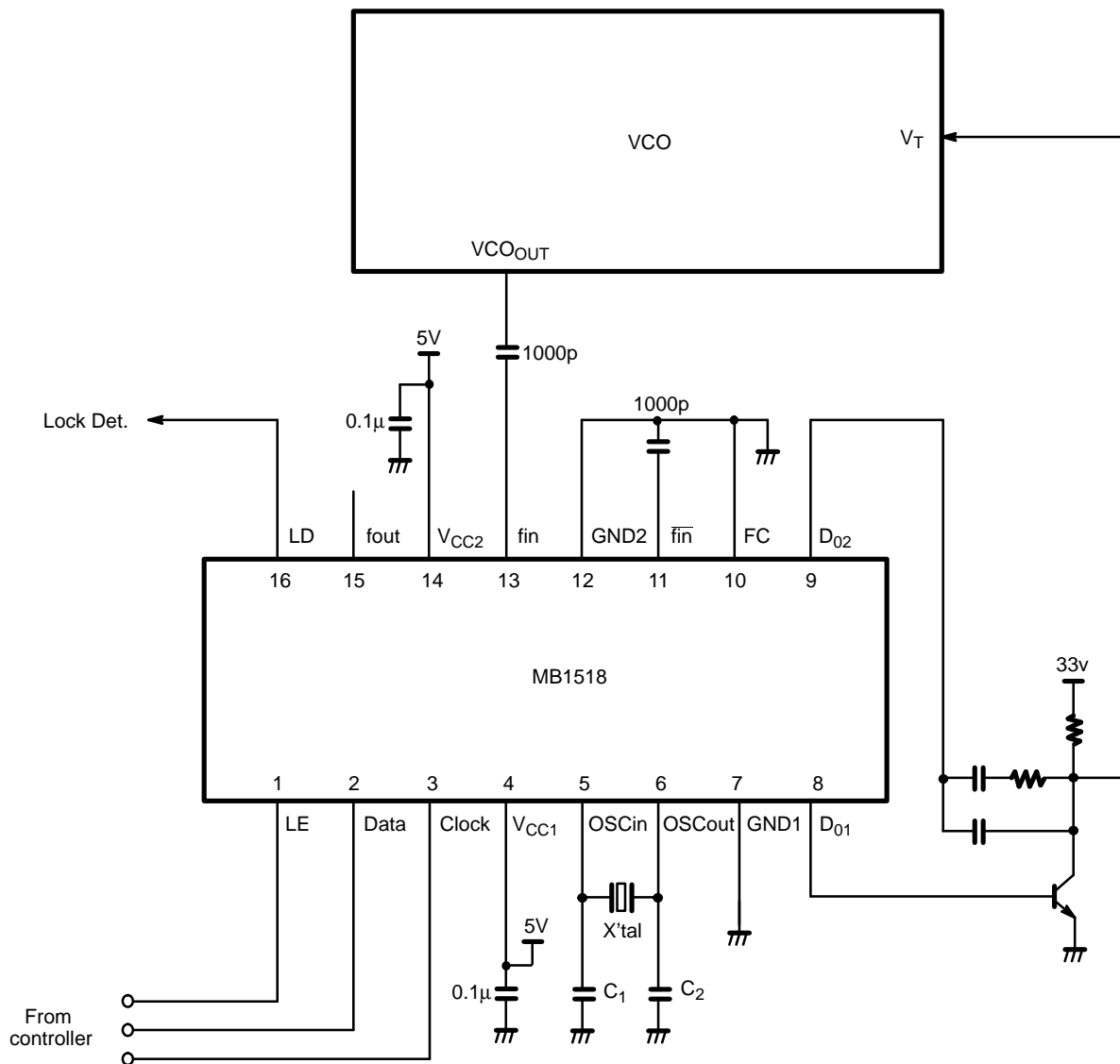
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		I <sub>CC</sub>	Note1	–	16.0	–	mA
Operating Frequency	f <sub>in</sub>	f <sub>in</sub>	Note2	10	–	2500	MHz
	OSC <sub>IN</sub>	f <sub>OSC</sub>	–	–	4	10	
Input Sensitivity	f <sub>in</sub>	P <sub>fin</sub>	2300 to 2500MHz	–4	–	6	dBm
			1900 to 2300MHz	–7	–	6	
			10 to 1900MHz	–10	–	6	
	OSC <sub>IN</sub>	V <sub>OSC</sub>	–	0.5	–	–	V <sub>PP</sub>
High–level Input Voltage	Except f <sub>in</sub> and OSC <sub>IN</sub>	V <sub>IH</sub>	–	V <sub>CC</sub> ×0.7+0.4	–	–	V
Low-level Input Voltage		V <sub>IL</sub>	–	–	–	V <sub>CC</sub> ×0.3–0.4	
High–level Input Current	Data, Clock, LE	I <sub>IH</sub>	–	–	1.0	–	μA
Low-level Input Current		I <sub>IL</sub>	–	–	–1.0	–	
	FC	I <sub>ILFC</sub>	–	–	–60	–	
Input Current	OSC <sub>IN</sub>	I <sub>IOSC</sub>	–	–	±50	–	
High–level Output Voltage	Except D <sub>O</sub>	V <sub>OH</sub>	V <sub>CC</sub> = 5.0V	4.4	–	–	V
Low-level Output Voltage		V <sub>OL</sub>	–	–	–	0.4	
High–impedance Cutoff Current	D <sub>01</sub> ,D <sub>02</sub>	I <sub>OFF</sub>	–	–	–	1.1	μA
High-level Output Current	Except D <sub>O</sub>	I <sub>OH</sub>	–	–1.0	–	–	mA
Low-level Output Current		I <sub>OL</sub>	–	1.0	–	–	

**Note1:**  $f_{in}=2.5GHz$ ,  $OSC_{IN}=4.0MHz$ ,  $V_{CC}=5.0V$ . Input pins are grounded and output pins are open.

**Note2:** AC coupling. Minimum operating frequency is measured with a capacitor 1000pF.

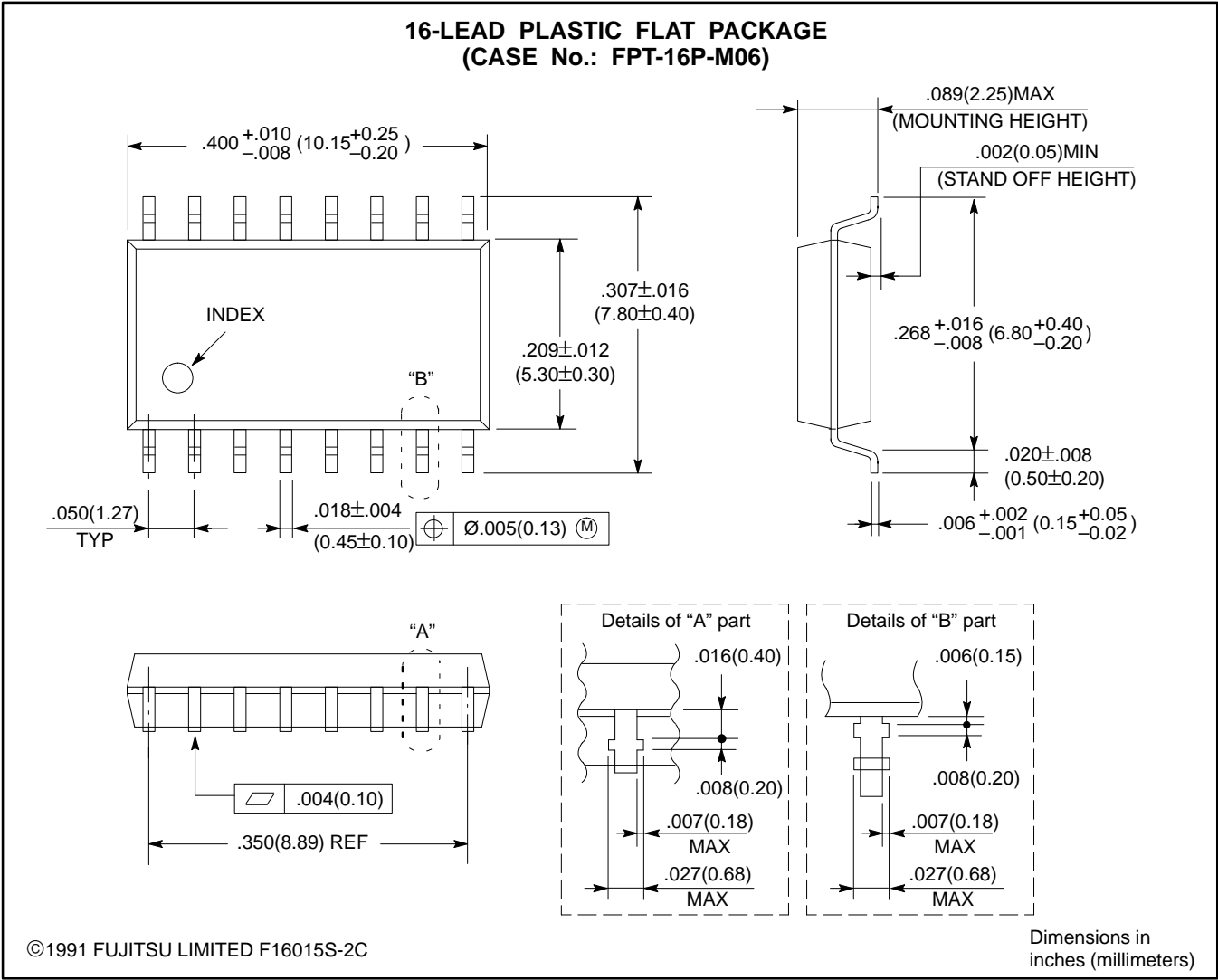


# MB1518 APPLICATION CIRCUIT



C<sub>1</sub>, C<sub>2</sub> : depends on the crystal oscillator.  
 FC : with internal pull up resistor.

PACKAGE DIMENSIONS



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Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete Information sufficient for construction purposes is not necessarily given.

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# FUJITSU LIMITED

For further information please contact:

## **Japan**

FUJITSU LIMITED  
Electronic Devices  
International Operations Department  
KAWASAKI PLANT, 1015 Kamikodanaka,  
Nakahara-ku, Kawasaki-shi,  
Kanagawa 211, Japan  
Tel: (044) 754-3753  
FAX: (044) 754-3332

## **North and South America**

FUJITSU MICROELECTRONICS, INC.  
Semiconductor Division  
3545 North First Street  
San Jose, CA 95134-1804, USA  
Tel: (408) 922-9000  
FAX: (408) 432-9044/9045

## **Europe**

FUJITSU MIKROELEKTRONIK GmbH  
Am Siebenstein 6-10,  
63303 Dreieich-Buchschlag,  
Germany  
Tel: (06103) 690-0  
FAX: (06103) 690-122

## **Asia Pacific**

FUJITSU MICROELECTRONICS ASIA PTE LIMITED  
No.51 Bras Basah Road,  
Plaza By The Park,  
#06-04 to #06-07  
Singapore 0718  
Tel: 336-1600  
FAX: 336-1609