Data Manual

Prescaler and Phase Lock Loop

1988

Prescaler and Phase Lock Loop

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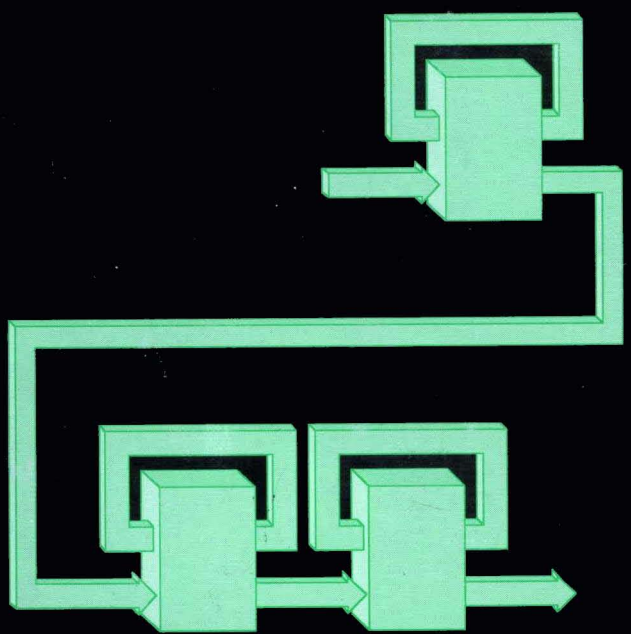
Data Manual



FUJITSU

Prescaler/Phase Lock Loop

1988 Data Manual

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Printed in the U.S.A.

Edition 1.0

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Section 1

Prescalers

FUJITSU

HIGH FREQUENCY PRESCALER

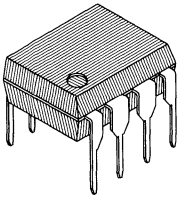
MB 467

November 1986
Edition 1.0

HIGH FREQUENCY PRESCALER

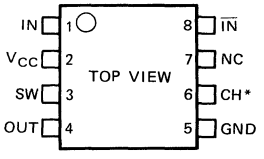
The Fujitsu MB 467 is a high frequency prescaler, which is used in Phase Locked Loop (PLL) frequency synthesizer and divides the input frequency by 10 or 20. The output is an open collector output to drive TTL or CMOS logic circuit.

- High Speed, Low Power Operation
  200 MHz at 30 mW typ.
- Low Level Input Voltage: $V_{IN} \geqq 150$ mVp-p
- Wide Operation Temperature
  $-30°C$ to $+85°C$ at $V_{CC} = +5$ V ± 10%
- Interface
  Input: Capacitor coupling due to internal biased input
  Output: Open collector output
- Plastic 8-pin Standard Dual-In-Line Package



PLASTIC PACKAGE
DIP-08P-M01

PIN ASSIGNMENT



Note: * It should be open.

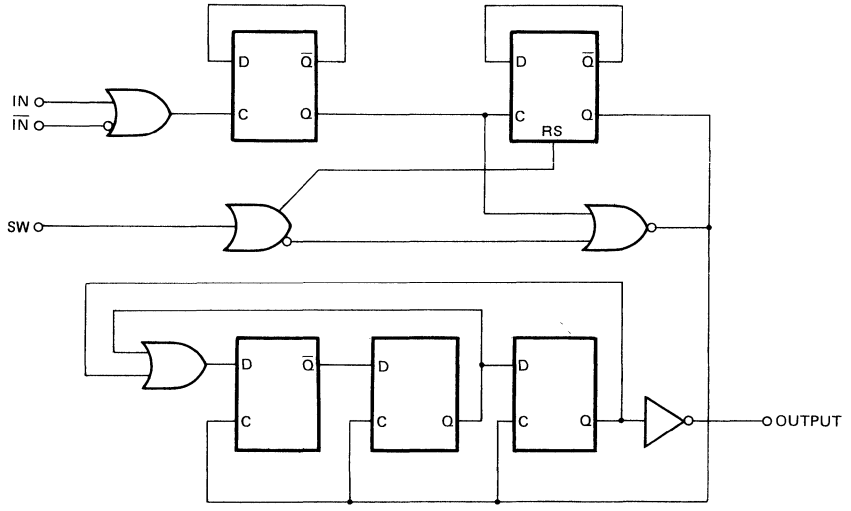
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC}	V
Output Current	I_O	5	mA
Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



SW	Divide Ratio
H	1/10
L	1/20
Open	1/20

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	CH	Check Input For Outgoing Test. It should be open.
7	NC	Non Connection
8	IN	Complementary Input

RECOMMENDED OPERATING CONDITIONS

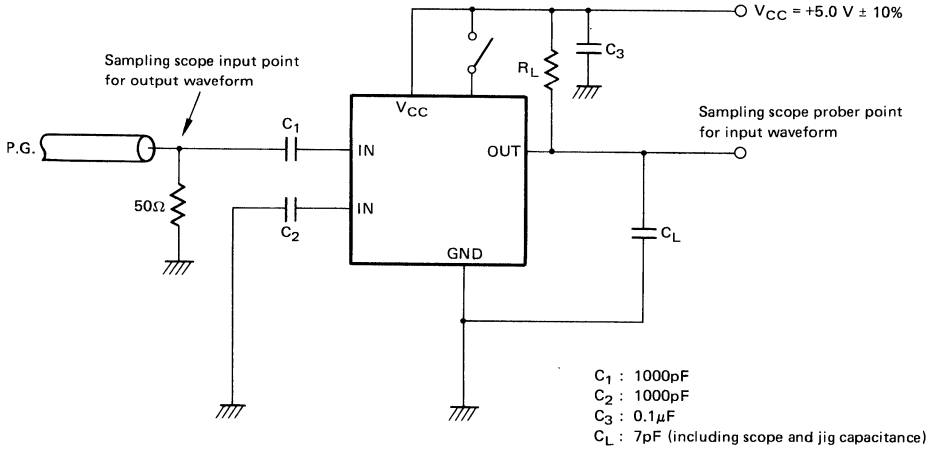
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ambient Temperature	T_A	−30		+85	°C
Load Capacitance	C_L			7	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

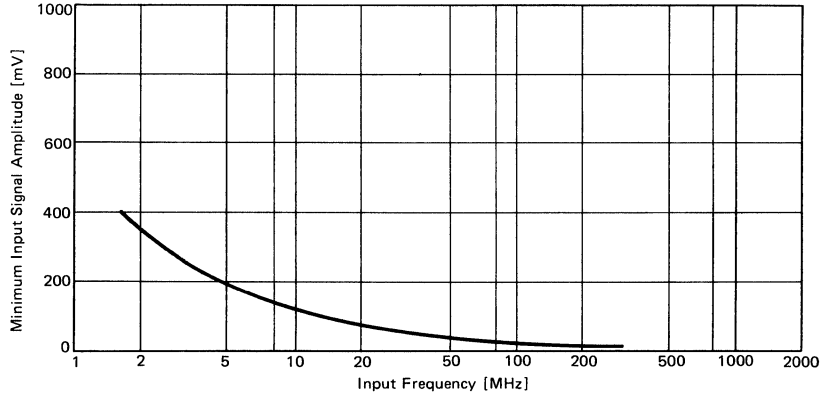
Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}	V_{CC} = 5.0 V, T_A = 25°C		6	10	mA
Output High Voltage	V_{OH}	With 2 kΩ pull-up resistor to V_{CC}	4.0			V
Output Low Voltage	V_{OL}	With 2 kΩ pull-up resistor to V_{CC}			0.4	V
Input Frequency	f_{IN}	V_{IN}: 150 mVp-p sine wave	10		200	MHz
Input Signal Amplitude for IN	V_{IN}		150		2000	mVp-p

TEST CIRICUIT



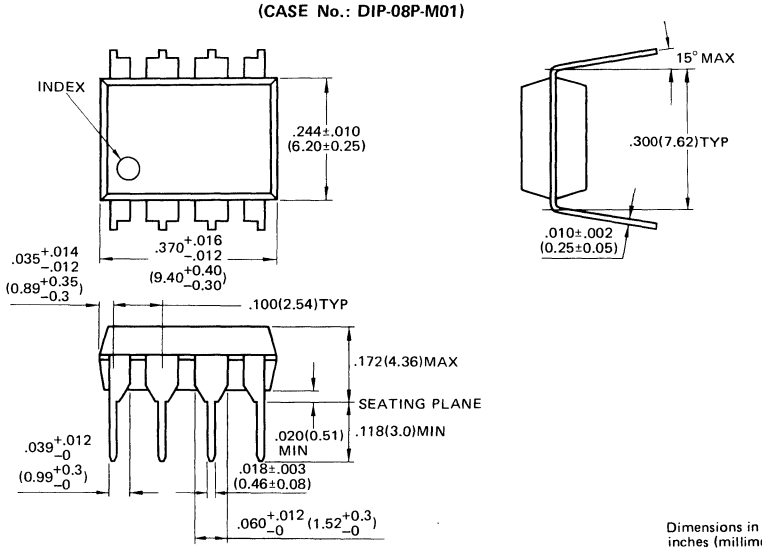
TYPICAL CHARACTERISTICS CURVES

INPUT SIGNAL AMPLITUDE vs INPUT FREQUENCY



PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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 Printed in Japan 0V2236-86YC

FUJITSU

TWO MODULUS PRESCALERS

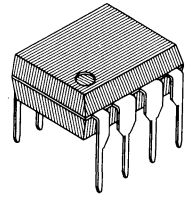
MB 501
MB 501L
MB 503
MB 504
MB 504L

November 1987
Edition 4.0

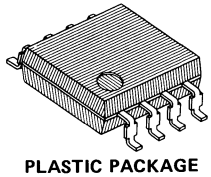
TWO MODULUS PRESCALER

The Fujitsu MB 501/503/504 are two modulus prescalers, which are used in Phase Locked Loop (PLL) frequency synthesizer and will divide the input frequency by the modulus of 64/65 or 128/129, 16/17 or 32/33, and 32/33 or 64/65 respectively. MB 501L/MB 504L is the low-power version of MB 501/MB 504; it will perform exactly the same function as MB 501/MB 504 but with much lower power dissipation.

The outputs are 1.6 V peak to peak on ECL level.



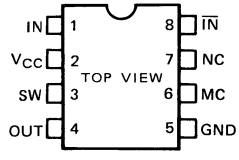
PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

- High Speed, Low Power Operation
  - 1.0 GHz at 150 mW typ. (MB 501)
  - 1.1 GHz at 50 mW typ. (MB 501L)
  - 200 MHz at 40 mW typ. (MB 503)
  - 520 MHz at 50 mW typ. (MB 504)
  - 520 MHz at 25 mW typ. (MB 504L)
- Pulse Swallow Function
- Wide Operation Temperature -40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.6 V_{P-P}
- Complete PLL synthesizer circuit with the Fujitsu MB 87001A, PLL synthesizer system block IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

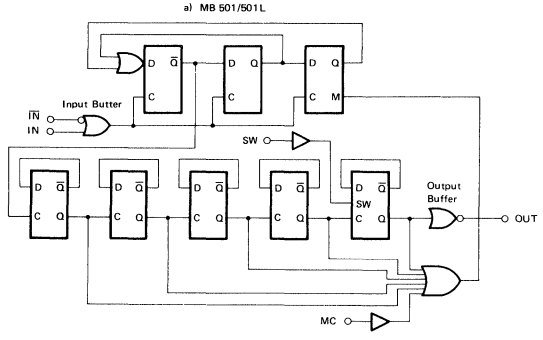
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Ambient Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAMS

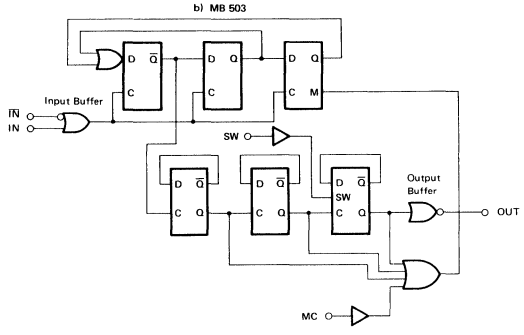
a) MB 501/501L



	SW	MC	Divide Ratio
MB 501/ MB 501L	H	H	1/64
	H	L	1/65
	L	H	1/128
	L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC},
L = GND to 0.8 V

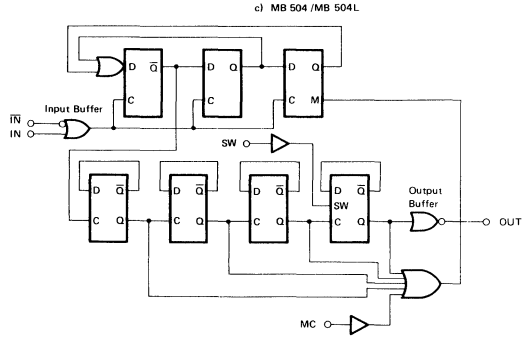
b) MB 503



	SW	MC	Divide Ratio
MB 503	H	H	1/16
	H	L	1/17
	L	H	1/32
	L	L	1/33

Note: SW : H = V_{CC}, L = open
MC : H = 2.0 V to V_{CC},
L = GND to 0.8 V

c) MB 504 /MB 504L



	SW	MC	Divide Ratio
MB 504/ MB 504L	H	H	1/32
	H	L	1/33
	L	H	1/64
	L	L	1/65

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC},
L = GND to 0.8 V

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
Input Signal Amplitude for IN	MB 501	V_{IN}	0.4		2	V_{P-P}
	MB 501L		0.4		2	V_{P-P}
	MB 503		0.15		2	V_{P-P}
	MB 504		0.15		2	V_{P-P}
	MB 504L		0.15		2	V_{P-P}
High Level Input Voltage for MC		V_{IH}	2.0			V
Low Level Input Voltage for MC		V_{IL}			0.8	V
Output Current		I_O		1.2		mA
Ambient Temperature		T_A	-40		+85	°C
Load Capacitance		C_L			12	pF

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input Selecting divide ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

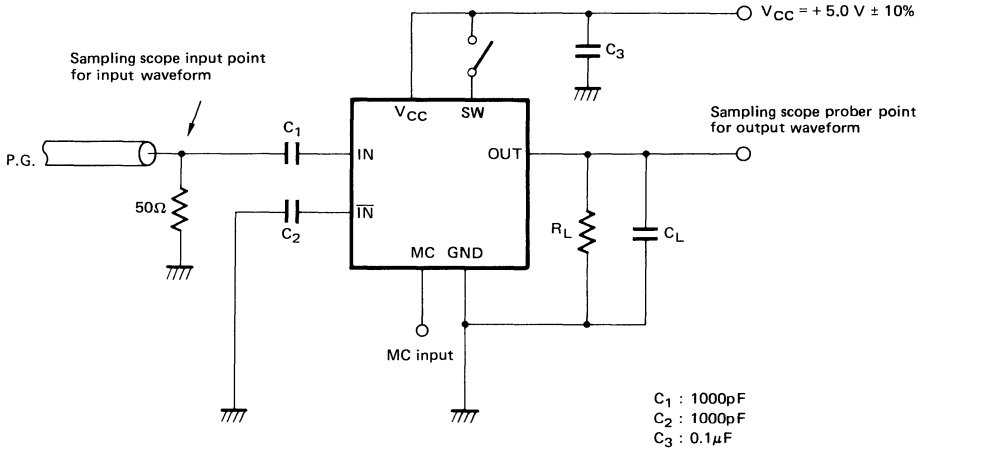
ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max.	
Power Supply Current	MB 501	I_{CC}	I/O pins are open		30	42*	mA
	MB 501L				10	14*	mA
	MB 503				8	12*	mA
	MB 504				10	14*	mA
	MB 504L				5	7*	mA
Output Amplitude		V_O		1.0	1.6		V_{P-P}
Input Frequency	MB 501	f_{IN}	with input coupling capacitor 1000pF	10		1000	MHz
	MB 501L			10		1100	MHz
	MB 503			10		200	MHz
	MB 504			10		520	MHz
	MB 504L			10		520	MHz
High Level Input Current for MC Input		I_{IH}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input		I_{IL}	V_{IL} = 0.8V	-0.2			mA
Modulus Set-up Time MC to OUT	MB 501	t_{SET}			16	26	ns
	MB 501L				16	26	ns
	MB 503				38	46	ns
	MB 504				20	30	ns
	MB 504L				18	28	

Note: * V_{CC} = 5V, T_A = 25°C

Fig. 2 – TEST CIRCUIT



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TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs INPUT FREQUENCY

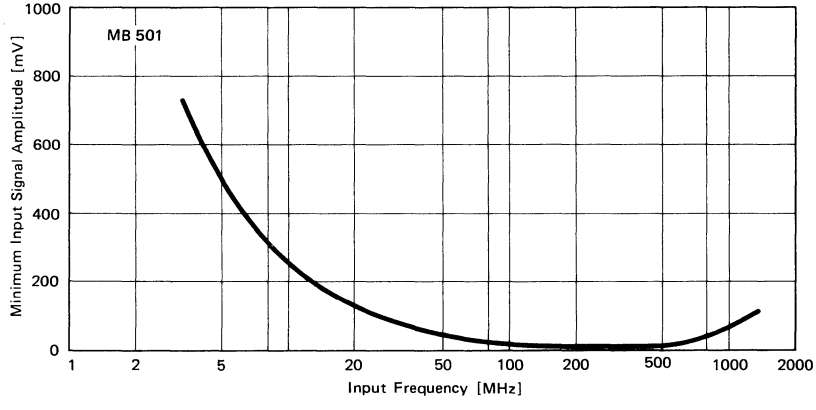

Fig. 4 – INPUT SIGNAL AMPLITUDE vs INPUT FREQUENCY

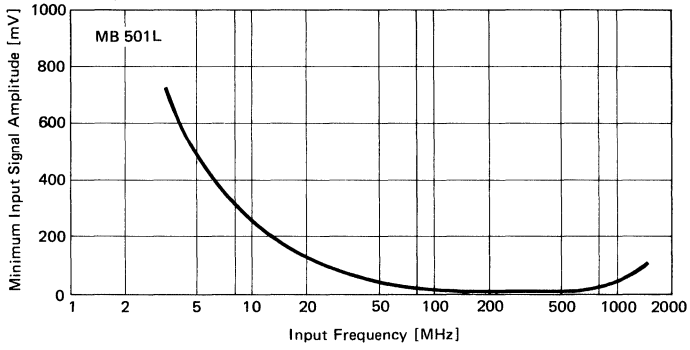

Fig. 5 – INPUT SIGNAL AMPLITUDE vs INPUT FREQUENCY

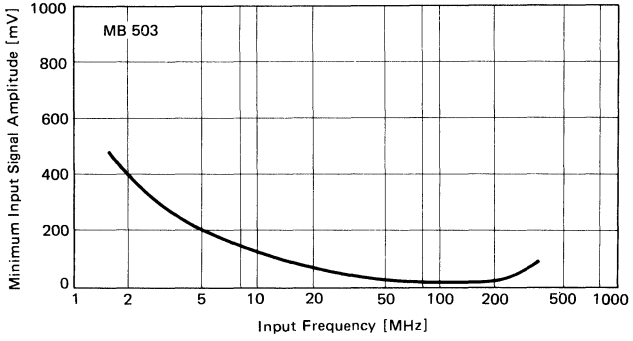

Fig. 6 – INPUT SIGNAL AMPLITUDE vs INPUT FREQUENCY

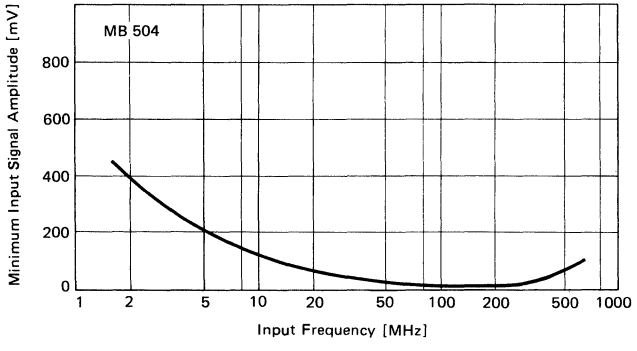

Fig. 7 — INPUT SIGNAL AMPLITUDE vs INPUT FREQUENCY

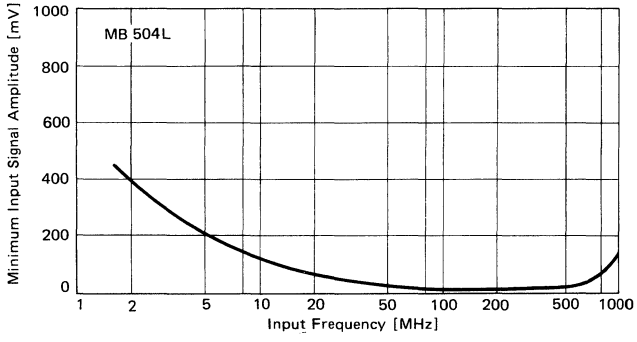

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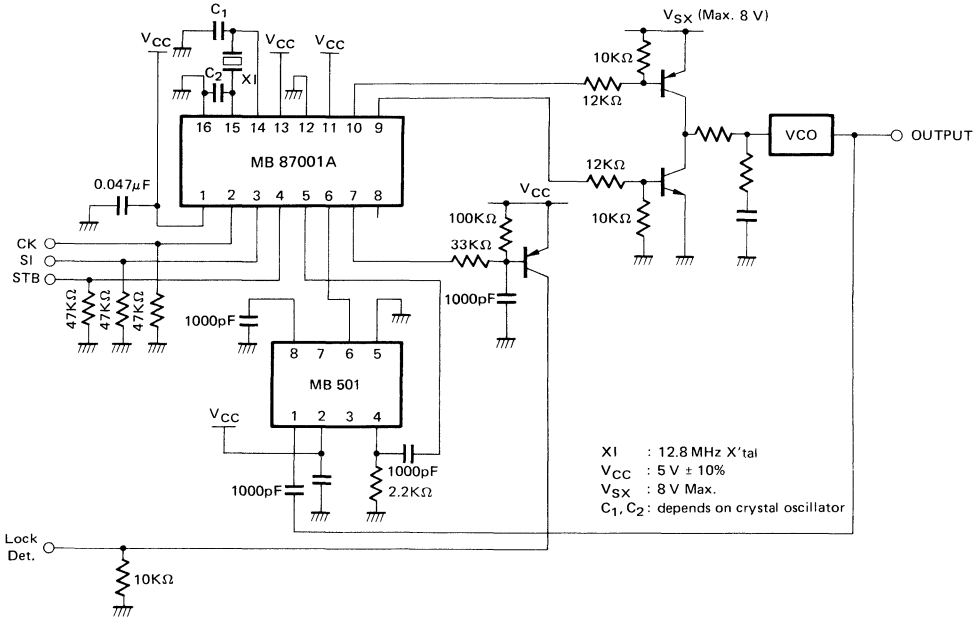
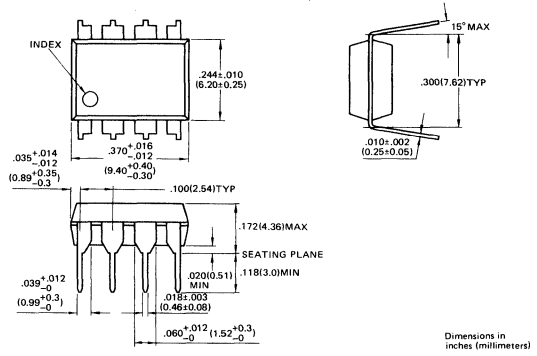
Fig. 8 — TYPICAL APPLICATION EXAMPLE



An example of application of MB501/501L/503/504/504L with PLL Synthesizer System Block IC MB 87001A

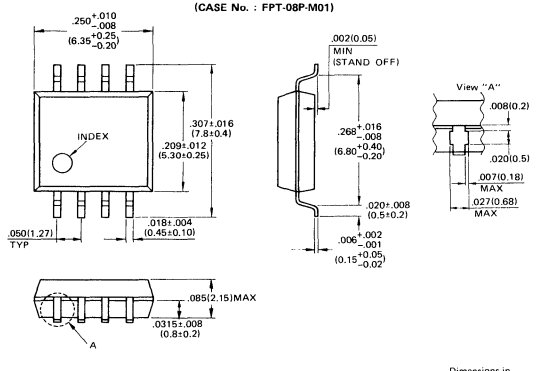
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches (millimeters)

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Printed in Japan 0V2158-87YC4

FUJITSU

LOW VOLTAGE/LOW POWER TWO MODULUS PRESCALERS

MB 501LV MB 504LV

September 1986
Edition 1.0

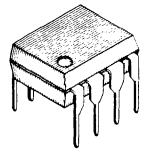
LOW VOLTAGE/LOW POWER TWO MODULUS PRESCALER

The Fujitsu MB 510LV/504LV are low power and low voltage versions of MB 510/504 two modulus prescalers, which are used in Phase Locked Loop (PLL) frequency symthesizer and will divide the input frequency by the modulus of 64/65 or 128/129, and 32/33 or 64/65 respectively.
The outputs are 1.1 V peak to peak on ECL level.

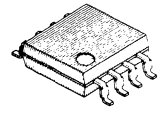
- Wide Low Voltage Operation 3.0 V typ., +2.7 to 4.5 V
- High Speed, Low Power Operation (V_{IN} = 0.4 V_{p-p})

  1.1 GHz at 36 mW typ. (MB 501LV)

  520 MHz at 18 mW typ. (MB 504V)
- Pulse Swallow Function
- Wide Operation Temperature -40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.1 V_{p-p}
- Complete PLL synthesizer circuit with the Fujitsu MB 87001A, PLL synthesizer system block IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package

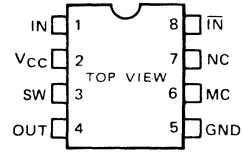


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temp.	T_{STG}	-55 to +125	°C

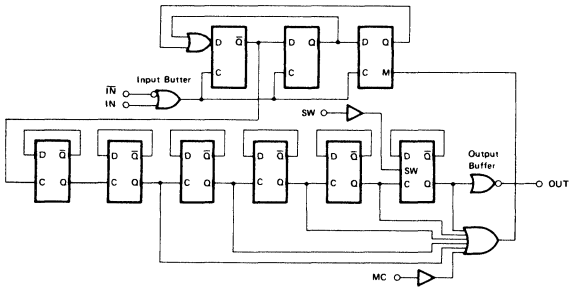
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Note: † Preliminary

Fig. 1 – BLOCK DIAGRAMS

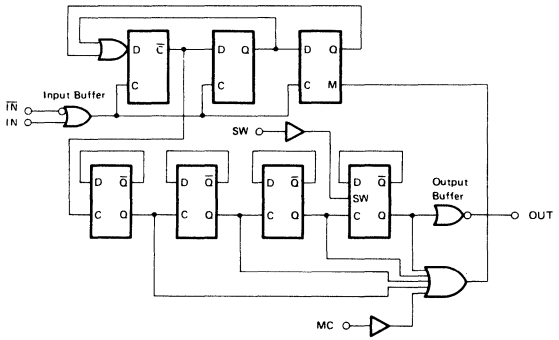
a) MB 501LV



SW	MC	Divide Ratio
H	H	1/64
H	L	1/65
L	H	1/128
L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = V_{IHM} to V_{CC},
L = GND to 0.8V
$V_{IHM} = \frac{1}{2}V_{CC} + 0.3V$

b) MB 504LV



SW	MC	Divide Ratio
H	H	1/32
H	L	1/33
L	H	1/64
L	L	1/65

Note: SW: H = V_{CC}, L = open
MC: H = V_{IHM} to V_{CC},
L = GND to 0.8V
$V_{IHM} = \frac{1}{2}V_{CC} + 0.3V$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	2.7	3.0	4.5	V
Input Signal Amplitude for IN	V_{IN}	0.4		1.2	$V_{p\text{-}p}$
High Level Input Voltage for MC	V_{IH}	V_{IHM}			V
Low Level Input Voltage for MC	V_{IL}			0.8	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			12	pF

Note: $V_{IHM} = \frac{1}{2} V_{CC} + 0.3$ V

1

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input Selecting divde ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	IN	Complementary Input

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Power Supply Current	MB 501LV	I_{CC}			12		mA
	MB 504LV				6		mA
Output Amplitude		V_O		0.8	1.1		$V_{p\text{-}p}$
Input Frequency	MB 501LV	f_{IN}	with input coupling capacitor 1000 pF	10		1100	MHz
	MB 504LV			10		520	MHz
High Level Input Current for MC Input		I_{IH}	V_{IH} = 2.0 V			0.4	mA
Low Level Input Current for MC Input		I_{IL}	V_{IL} = 0.8 V	-0.2			mA
Modulus Set-up Time MC to OUT	MB 501LV	t_{SET}			16	26	ns
	MB 504LV				18	28	ns

Fig. 2 – TEST CIRCUIT

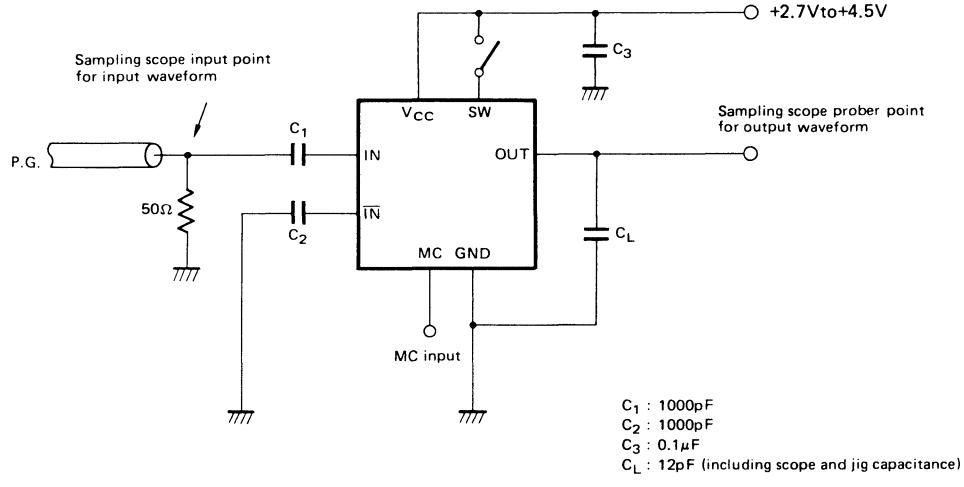
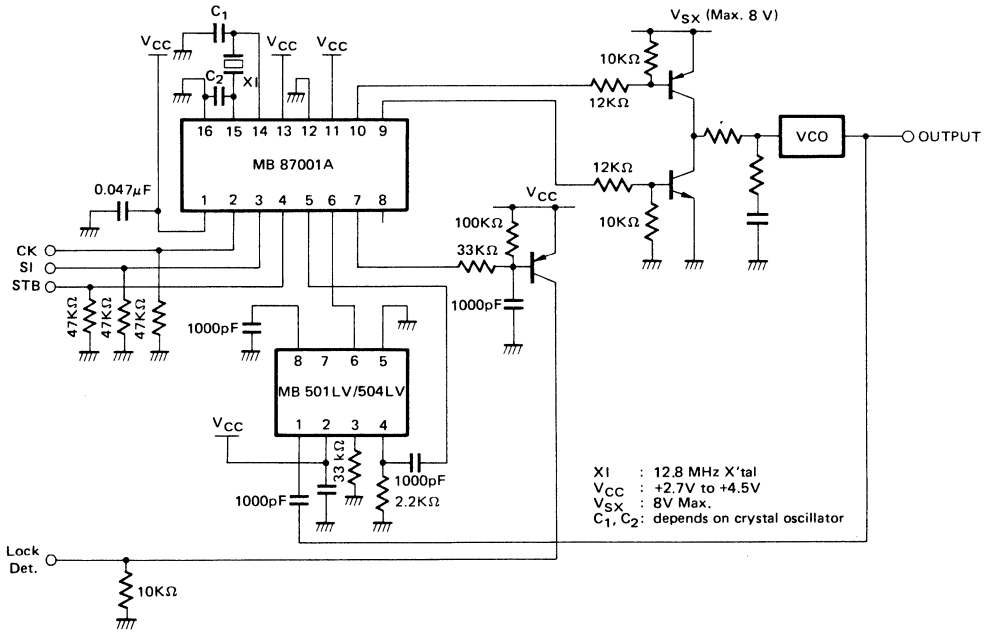


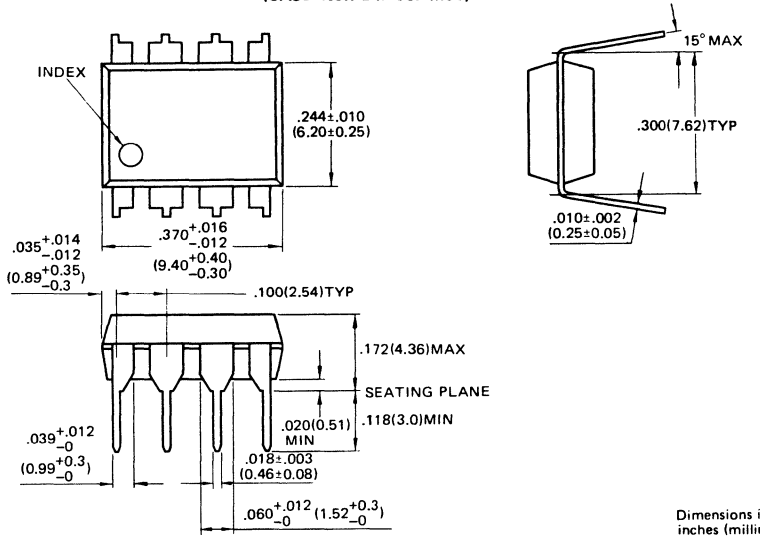
Fig. 3 – TYPICAL APPLICATION EXAMPLE



An example of application of MB 501LV/MB 504LV with PLL Synthesizer System Block IC MB 87001

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)

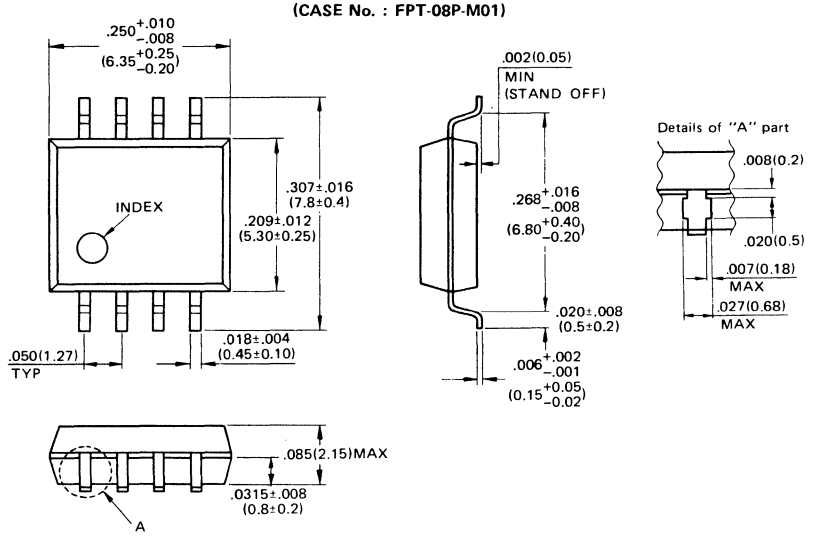


Dimensions in inches (millimeters)

1

PACKAGE DIMENSIONS

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches (millimeters)

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FUJITSU

SUPER LOW POWER TWO MODULUS PRESCALER

MB501SL

December 1987
Edition 1.0

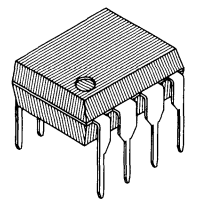
SUPER LOW POWER TWO MODULUS PRESCALER

The Fujitsu MB501SL is a super low power version of MB501 two modulus prescaler which are used in Phase Locked Loop (PLL) frequency synthesizer and divides the input frequency by the modulus of 64/65 or 128/129, respectively. The MB501SL achieves extremely small stray capacitance of internal element, realized through the use of Fujitsu Advanced Process Technology. As the results, high speed operation is achieved with low power supply current of 5 mA typ., about a half current value of MB501L.

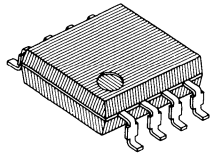
- High Speed: fmax = 1.1 GHz max. (V_{IN} = 0.4 Vp-p)
- Pulse Swallow Function: 64/65, 128/129
- Low Power Supply Current: 5.0 mA typ.
- Stable Output Amplitude: V_O = 1.6 Vp-p typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer system block IC
- Plastic 8-pin Dual-In-Line Package (Suffix: –P)

  Plastic 8-pin Mini Flat Package (Suffix: –PF)
- Built-in a Terminal Resistor

  Stable output amplitude is obtained up to output load capacitance of 8 pF.

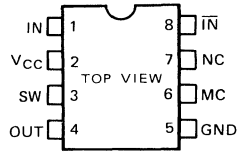


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



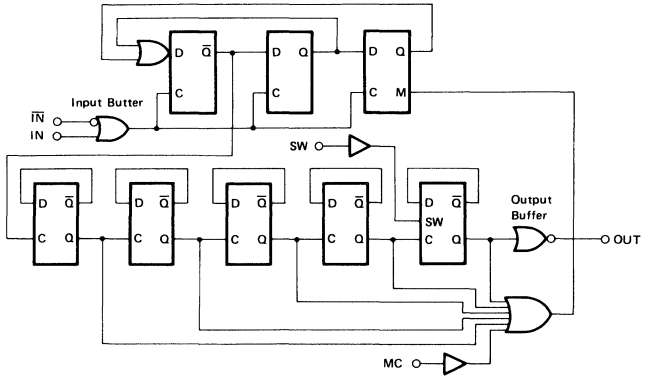
ABSOLUTE MAXIMUM RATINS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB501SL BLOCK DIAGRAM



	SW	MC	Divide Ratio
MB 501SL	H	H	1/64
	H	L	1/65
	L	H	1/128
	L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC},
L = GND to 0.8 V

PIN DESCRIPTION

Pin Number	Symbol	Description
1	IN	Input
2	V_{CC}	Power Supply, +5V
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

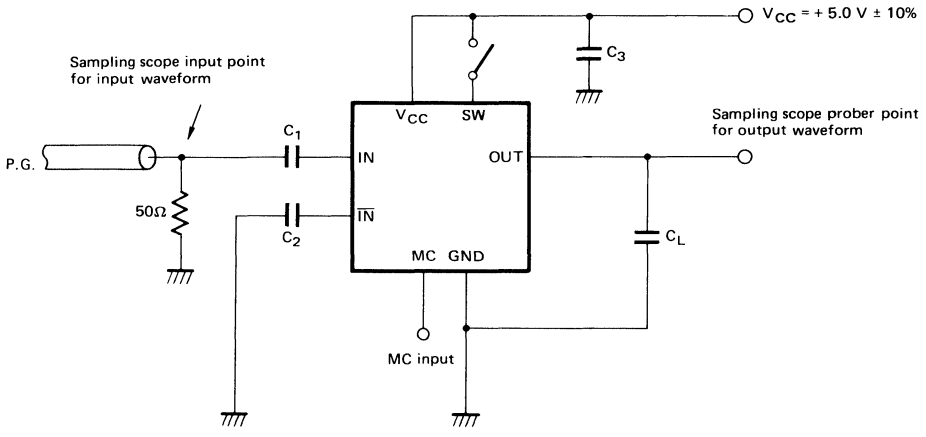
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	-40	–	+85	°C
Load Capacitance	CL	–	–	8	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

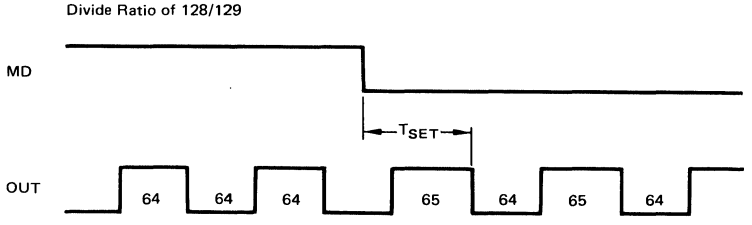
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}		–	5.0	7.0	mA
Output Amplitude	V_O	Built-in a Terminal Resistor. Load capacitance = 8pF	1.0	1.6	–	Vp-p
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	10	–	1100	MHz
Input Signal Amplitude	V_{IN}	–	0.4	–	2.0	Vp-p
High Level Input Voltage for MC	V_{IH}	–	2.0	–	–	V
Low Level Input Voltage for MC	V_{IL}	–	–	–	0.8	V
High Level Input Current for MC	I_{IH}	V_{IH} = 2.0V, V_{IL} = 0.8V	–	–	0.4	mA
Low Level Input Current for MC	I_{IL}		-0.2	–	–	mA
Modulus Set-up Time MC to Output	t_{SET}	–	–	16	26	ns

Fig. 2 – TEST CIRCUIT



C_1 : 1000pF
C_2 : 1000pF
C_3 : 0.1μF
C_L : 8 pF (including scope and jig capacitance)

TWO MODULUS OPERATING TIMING CHART



Notes:
When divide ratio of 129 is selected, positive pulse has increased by one to 65.

Set up time = 16 ns typ
The time between MD signal is input and divide ratio of prescaler is changed.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

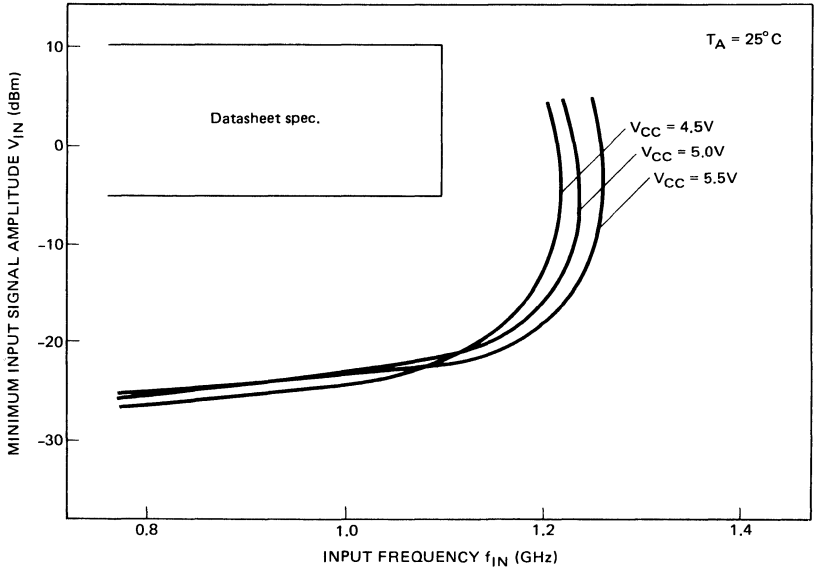


Fig. 4 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

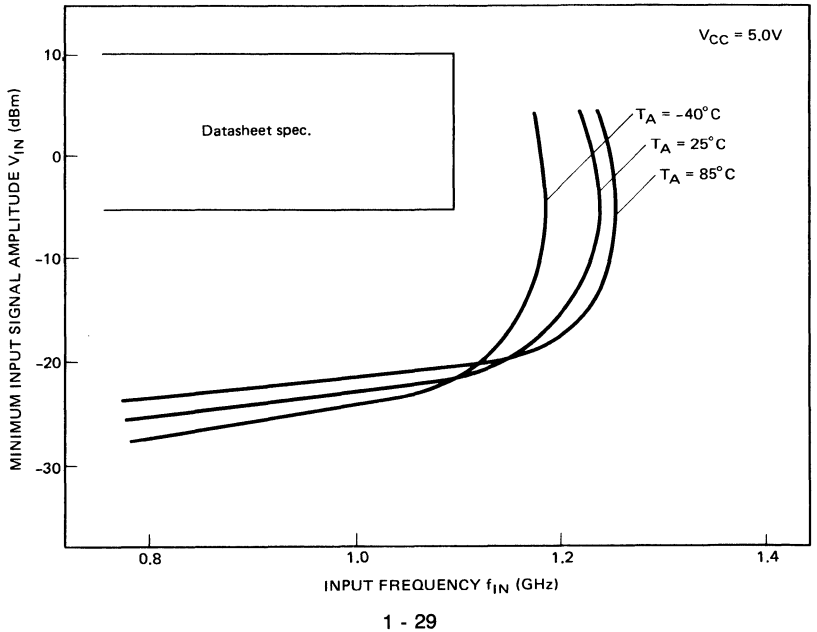


Fig. 5 – POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE

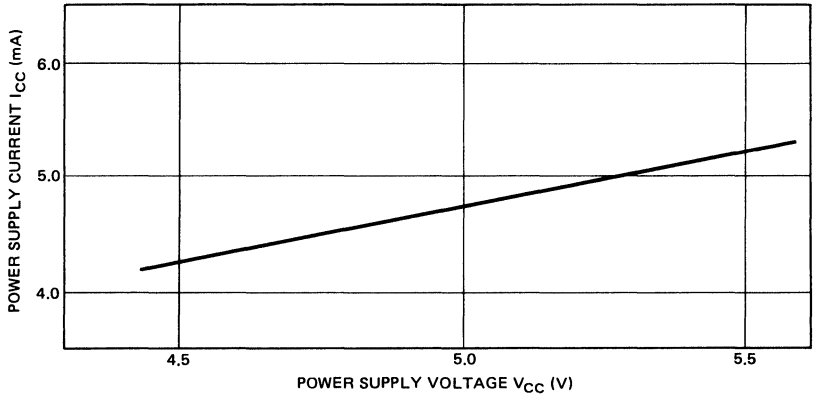


Fig. 6 – POWER SUPPLY CURRENT vs. TEMPERATURE

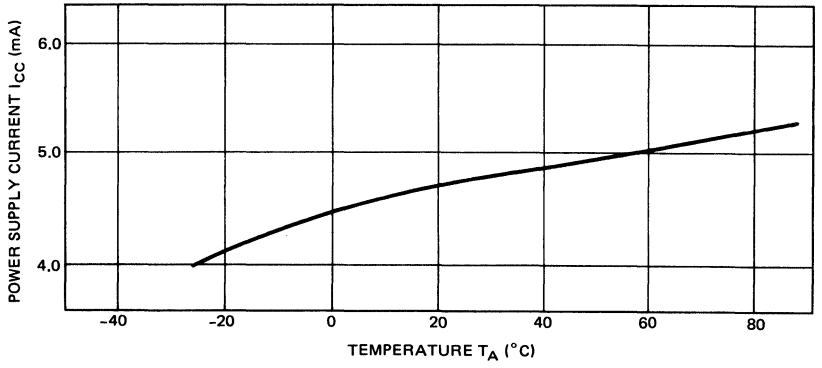
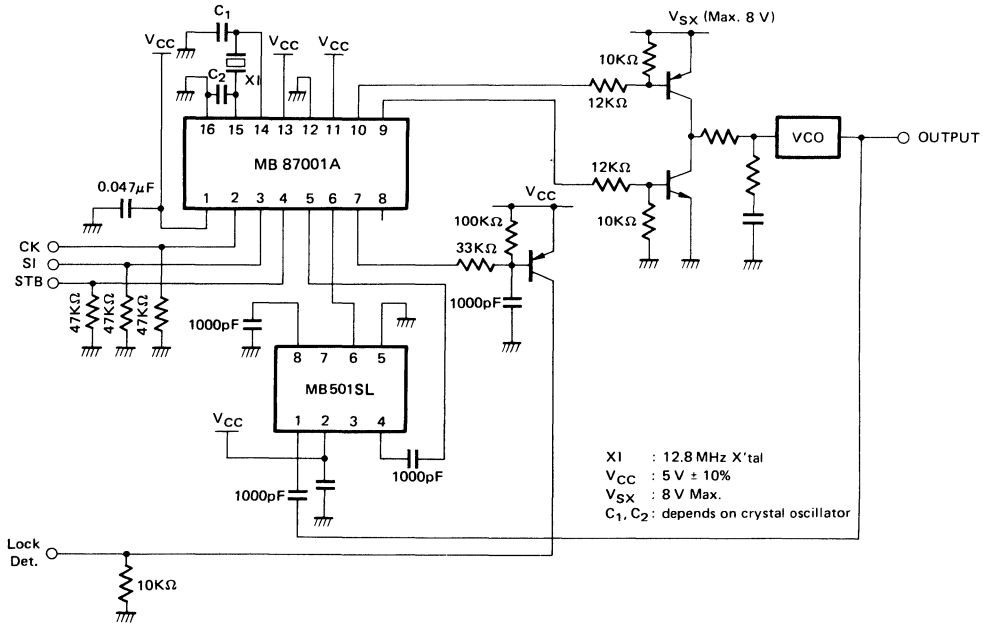


Fig. 7 – TYPICAL APPLICATION EXAMPLE

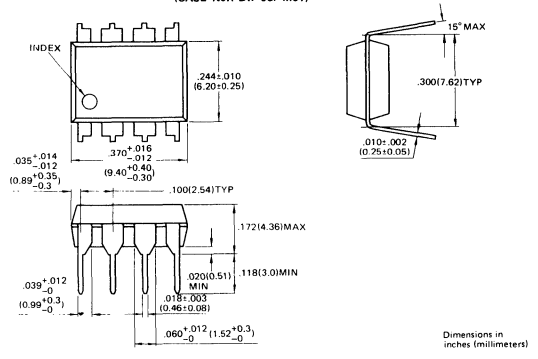


1

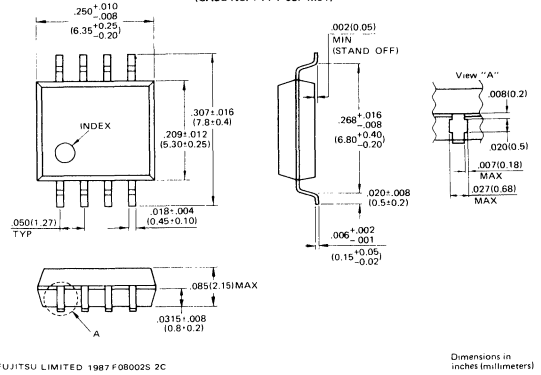
PACKAGE DIMENSIONS

(Suffix: -P) (Suffix: -PF)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



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Printed in USA 0V2306-87ZC1

FUJITSU

ULTRA HIGH FREQUENCY PRESCALER

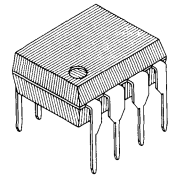
MB 505-16

September 1986
Edition 2.0

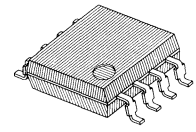
ULTRA HIGH FREQUENCY PRESCALER

The Fujitsu MB 505 is a high frequency prescaler, which is used in Phase Locked Loop (PLL) frequency synthesizer and will divide the input frequency by the modulus of 128 or 256. The outputs are 1.6 V peak to peak on ECL level.
Its ultra high frequency operation provides wide application range, such as Direct Broadcasting Satellite System, CATV system, UHF Transceiver, etc.

- High Speed, Low Power Operation
  MB 505-16: 1.6 GHz at 45 mW typ.
- Wide Operation Temperature -40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.6 V_{P-P}
- Complete PLL synthesizer circuit with the Fujitsu MB 87006A, PLL synthesizer system block IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package

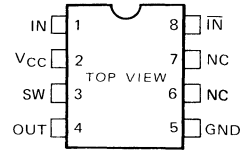


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



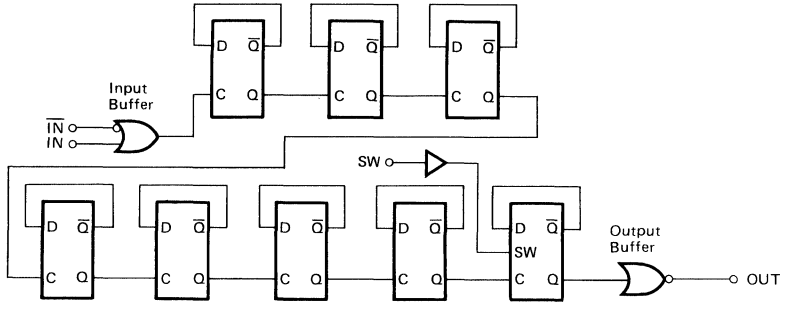
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Ambient Temp.	T_A	-40 to +85	°C
Storage Temp.	T_{STG}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 505 BLOCK DIAGRAM



SW	Divide Ratio
H	1/128
L	1/256

Note: SW: H = V_{CC}, L = open

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	Power Supply Voltage
3	SW	Divide Ratio Control Input Selecting divide ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	NC	Non Connection
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Signal Amplitude for IN	V_{IN}	0.15		1.2	V_{P-P}
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS

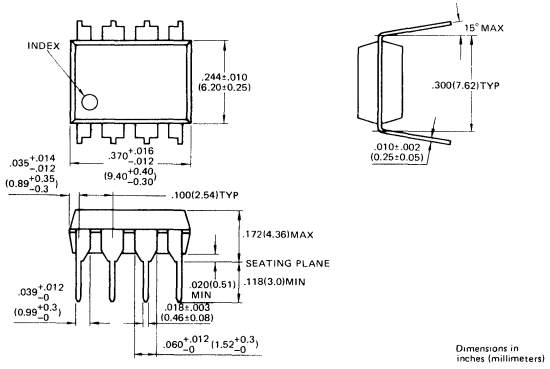
(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}			9		mA
Output Amplitude	V_O		1.0	1.6		V_{p-p}
Input Frequency	f_{IN}	with input coupling capacitor 1000 pF	100		1600	MHz
Input Voltage	V_{IN}	f_{IN} = 100 MHz to 1.6 GHz	0.15		1.2	V_{p-p}

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)

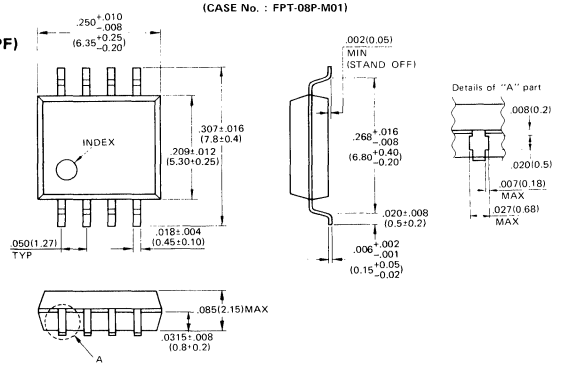
(Suffix: P)



Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)

(Suffix: PF)



Dimensions in inches (millimeters)

Marking Format

MB 505-16, 8-pin Plastic DIP

MB 505-16, 8-lead Plastic Flat Package

xxxx. Date Code
xxx: Control Code

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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FUJITSU

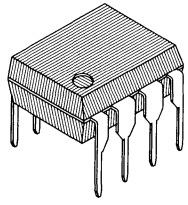
ULTRA HIGH FREQUENCY PRESCALER

MB 506

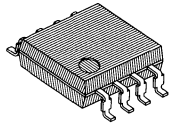
May 1986
Edition 1.0

ULTRA HIGH FREQUENCY PRESCALER

The Fujitsu MB 506 is a high frequency prescaler, which is used in Phase Locked Loop (PPL) frequency synthesizer and will divide the input frequency by the modulus of 64, 128, or 256. The outputs are 1.6 V peak to peak on ECL level.
Its ultra high frequency operation provides wide application range, such as Direct Broadcasting Satellite System, CATV system, UHF Transceiver, etc.



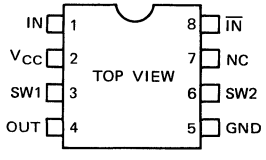
PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
PFT-08P-M01

- High Speed, Low Power Operation
  2.4 GHz at 90 mW typ.
- Wide Operation Temperature $-40°C$ to $+85°C$
- Stable Output Amplitude $V_{OUT} = 1.6\ V_{P-P}$
- Complete PLL synthesizer circuit with the Fujitsu MB 87006A, PLL synthesizer system block IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package

PIN ASSIGNMENT



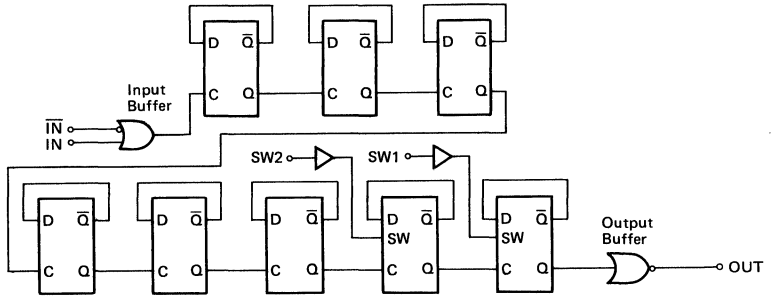
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temp.	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 506 BLOCK DIAGRAM



SW1	SW2	Divide Ratio
H	H	1/64
L	H	1/128
H	L	1/128
L	L	1/256

Note: H = V_{CC}, L = open

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	Power Supply Voltage
3	SW1	Divide Ratio Control Input Selecting divide ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	SW2	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

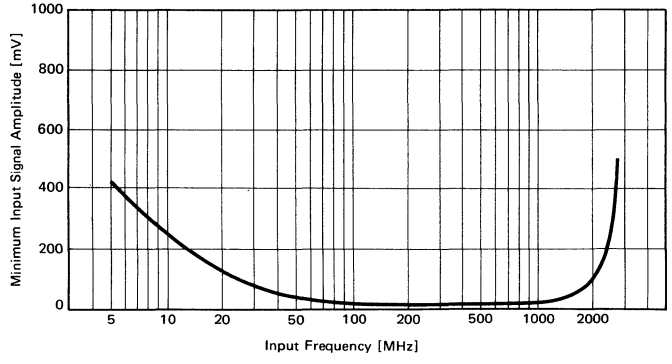
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Signal Amplitude for IN	V_{IN}	0.1		1.2	V_{P-P}
Output Current	I_O		2		mA
Ambient Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

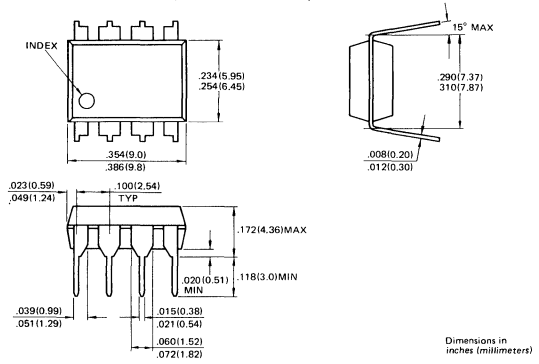
Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Power Supply Current	I_{CC}				18		mA
Output Amplitude	V_O			1.0	1.6		V_{P-P}
Input Frequency	f_{IN}	with input coupling capacitor 1000 pF	T_A = -40°C to 85°C	100		2200	MHz
			T_A = -40°C to 60°C	100		2400	
Input Voltage	V_{IN}	f_{IN} = 100 MHz to 1.3 GHz		0.1		1.2	V_{P-P}
		f_{IN} = 1.3 MHz to 2.4 GHz		0.4			

Fig. 2 – INPUT SIGNAL AMPLITUDE vs INPUT FREQUENCY



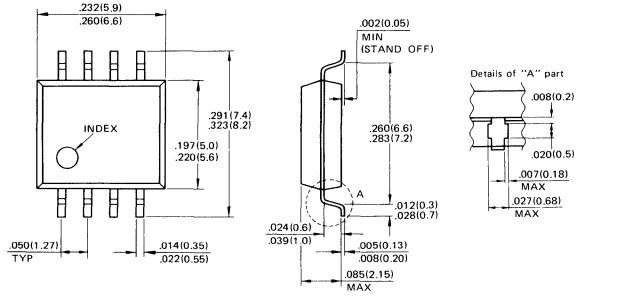
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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FUJITSU

1.6 GHz TWO MODULUS PRESCALERS

MB 507

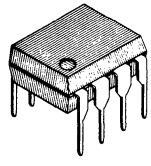
August 1986
Edition 1.0

1.6 GHz TWO MODULUS PRESCALER

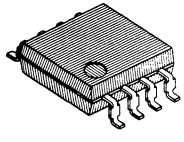
The Fujitsu MB 507 is a 1.6 GHz two modulus prescalers, which are used in Phase Locked Loop (PLL) frequency synthesizer and will divide the input frequency modulus of 128/129 or 256/357.
The outputs are 1.6 V peak to peak on ECL level.

- High Speed, Low Power Operation
  1.6 GHz at 90mW typ.
- Pulse Swallow Function
- Wide Operation Temperature -40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.6 V_{P-P}
- Complete PLL synthesizer circuit with the Fujitsu MB 87001A, PLL synthesizer system block IC
- Plastic 8-pin standard Dual-In-Line Package or space saving Flat Package

PRELIMINARY

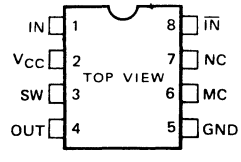


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



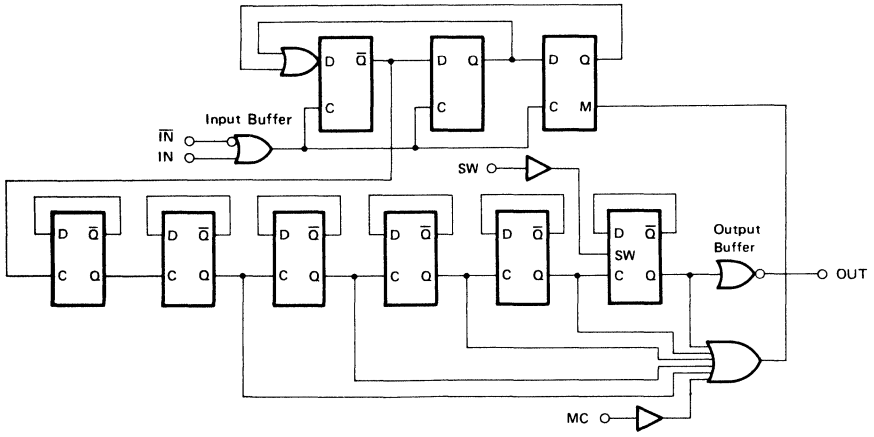
ABSOLUTE MAXIMUM RATINGS*

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Ambient Temp.	T_A	-40 to +85	°C
Storage Temp.	T_{STG}	-55 to +150	°C

Note:* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM



	SW	MC	Divide Ratio
MB 507	H	H	1/128
	H	L	1/129
	L	H	1/256
	L	L	1/257

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC}, L = GND to 0.8 V

RECOMMENDED OPERATING CONDITIONS*

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Signal Amplitude for IN	V_{IN}	0.4		2	V_{P-P}
High Level Input Voltage for MC	V_{IH}	2.0			V
Low Level Input Voltage for MC	V_{IL}			0.8	V
Output Current	I_O		2		mA
Ambient Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			12	pF

1

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input Selecting Divide Ratio (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	IN	Complementary Input

ELECTORICAL CHARACTERISTICS*

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}			18		mA
Output Amplitude	V_O		1.0	1.6		V_{P-P}
Input Frequency	f_{IN}	with input coupling capacitor 1000pF	100		1600	MHz
High Level Input Current for MC Input	I_{IH}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC Input	I_{IL}	V_{IL} = 0.8V	-0.2			mA
Modulus Set-up Time MC to OUT in 1.6GHz Operation	t_{SET}			18	28	ns

Fig. 2 – TEST CIRCUIT

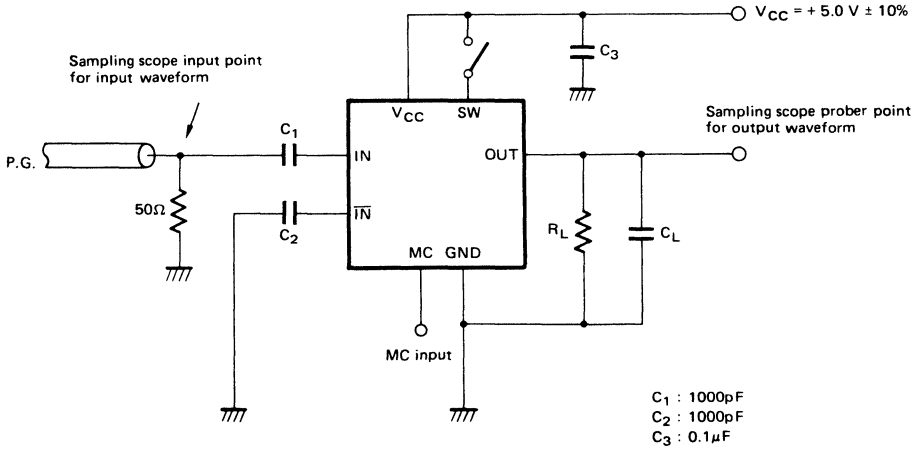
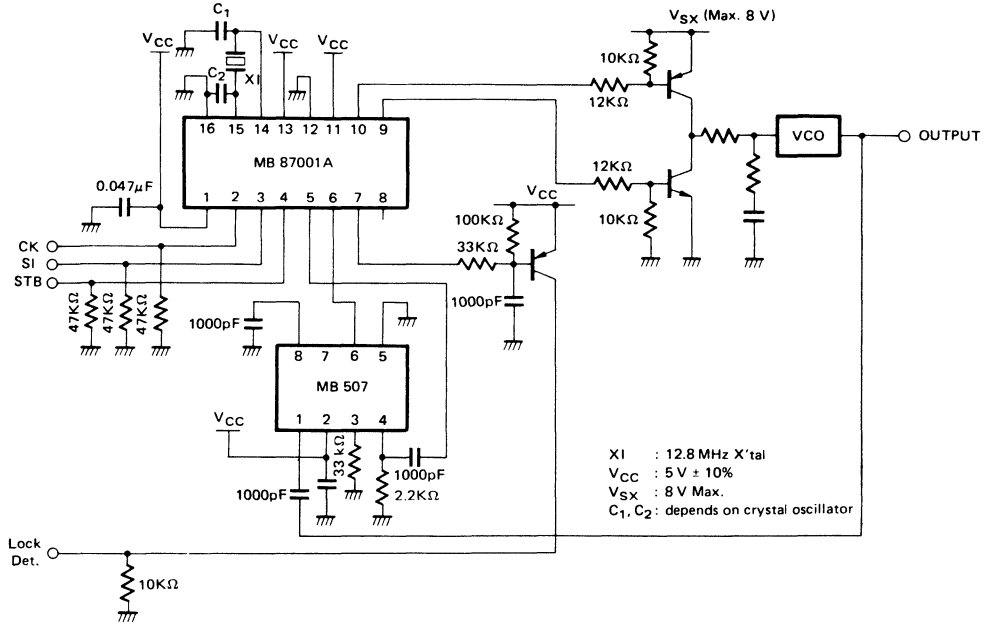


Fig. 3 – TYPICAL APPLICATION EXAMPLE

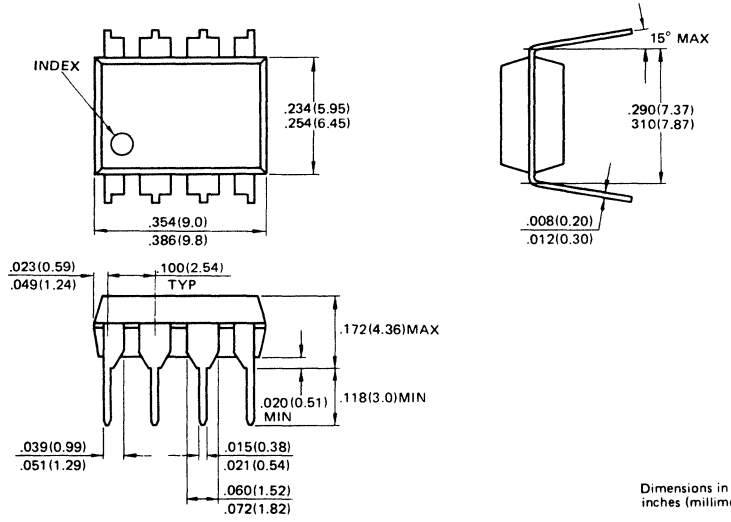


1

PACKAGE DIMENSIONS

(Suffix: P)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)

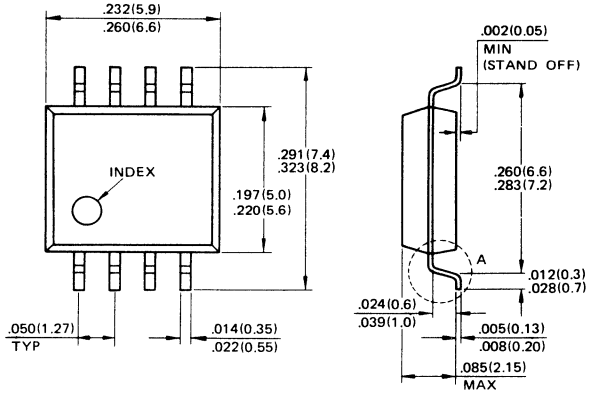


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches
(millimeters)

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FUJITSU

2.3 GHz TWO MODULUS PRESCALERS

MB508

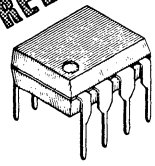
November 1987
Edition 1.0

2.3 GHz TWO MODULUS PRESCALERS

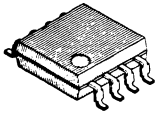
PRELIMINARY

The Fujitsu MB508 is a 2.3 GHz two modulus prescalers, which are used in Phase Locked Loop (PLL) frequency synthesizer and divides the input frequency modulus of 128/130, 256/258 or 512/514. The output is 1.6 V peak to peak ECL level. Its ultra high frequency operation provides wide application, such as Direct Broadcasting Satellite System, CATV system, UHF Transceiver, etc.

- High Speed : f = 2.3 GHz max. (V_{IN} = 0.4 Vp-p)
- Input Signal Amplitude : V_{IN}= 100 mVp-p (f_{IN} =~ 1.8GHz)
- Pulse Swallow Function : 128/130, 256/258, 512/514
- Power Dissipation : 120 mW typ.
- Wide Operation Temperature : -40 °C to +85 °C
- Stable Output Amplitude : V_{OUT} = 1.6 Vp-p typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer system block IC
- Plastic 8-pin standard Dual-In-Line Package or Mini Flat Package



PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

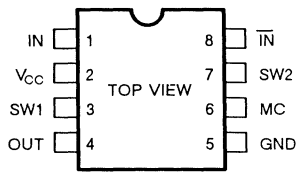
1

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C

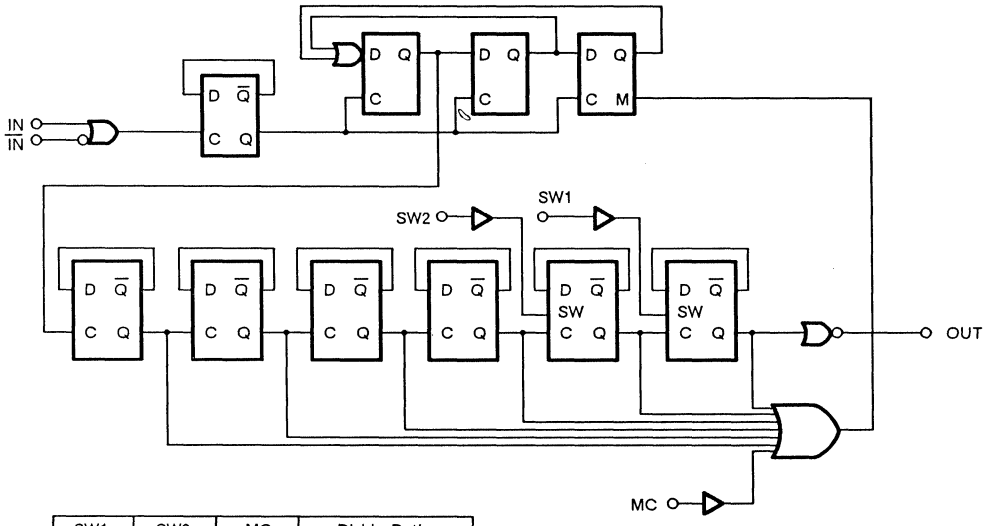
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB508 BLOCK DIAGRAM



SW1	SW2	MC	Divide Ratio
H	H	H	1/128
H	H	L	1/130
H	L	H	1/256
L	H	H	1/256
H	L	L	1/258
L	H	L	1/258
L	L	H	1/512
L	L	L	1/514

Note: SW: H=Vcc, L=open
MC: H=2.0V to Vcc, L=GND to 0.8V

PIN DESCRIPTIONS

Pin Number	Symbol	Descriptions
1	IN	Input
2	Vcc	Power Supply, +5V
3	SW1	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	SW2	Divide Ratio Control Input (See Divide Ratio Table)
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Operating Temperature	T_A	-40		+85	°C
Load Capacitance	C_L			12	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}			24		mA
Output Amplitude	V_O		1.0	1.6		Vp-p
Input Frequency	f_{IN}	with inupt coupling capacitor 1000pF	100		2300	MHz
Input Signal Amplitude	V_{INA}	f_{IN} = 1800MHz to 2300MHz	0.4		1.2	Vp-p
	V_{INB}	f_{IN} = 100MHz to 1800MHz	0.1		2.0	Vp-p
High Level Input Voltage for MC	V_{IH}		2.0			V
Low Level Input Voltage for MC	V_{IL}				0.8	V
High level Input Current for MC	I_{IH}	V_{IH} = 2.0V, V_{IL} =0.8V			0.4	mA
Low Level Input Current for MC	I_{IL}		-0.2			mA
Modulus Set-up Time MC to Output at 2.3 GHz Operation	t_{SET}			18	28	ns

FUJITSU

Fig. 2 – TEST CIRCUIT

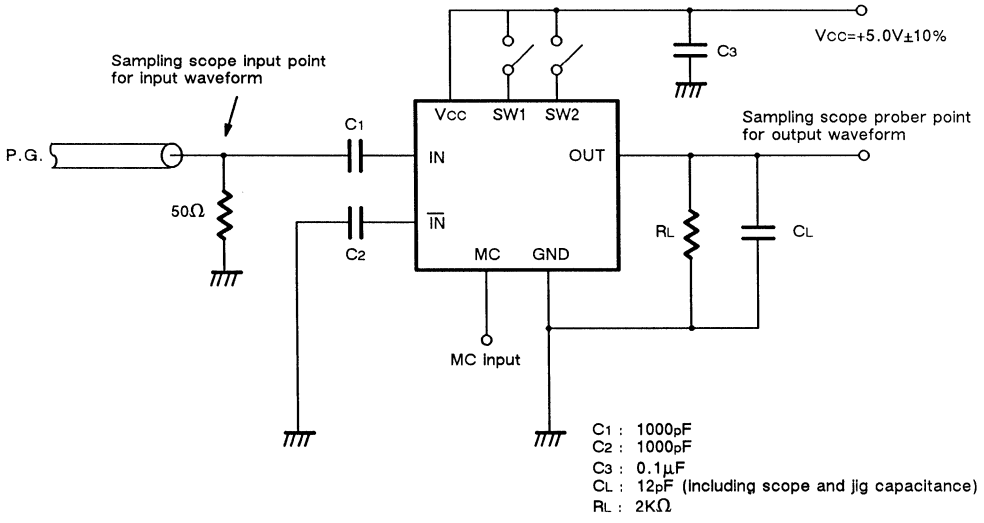


Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

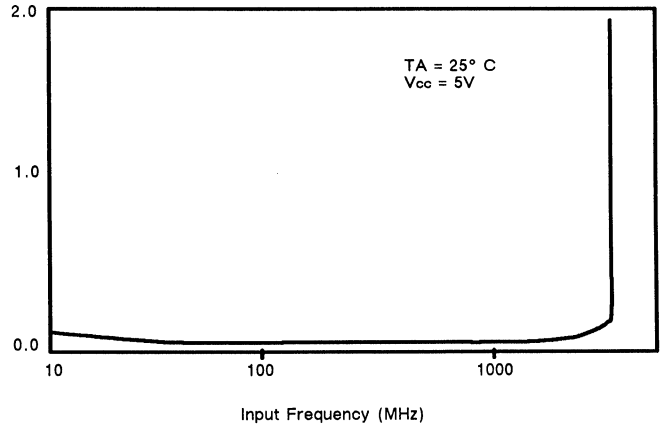
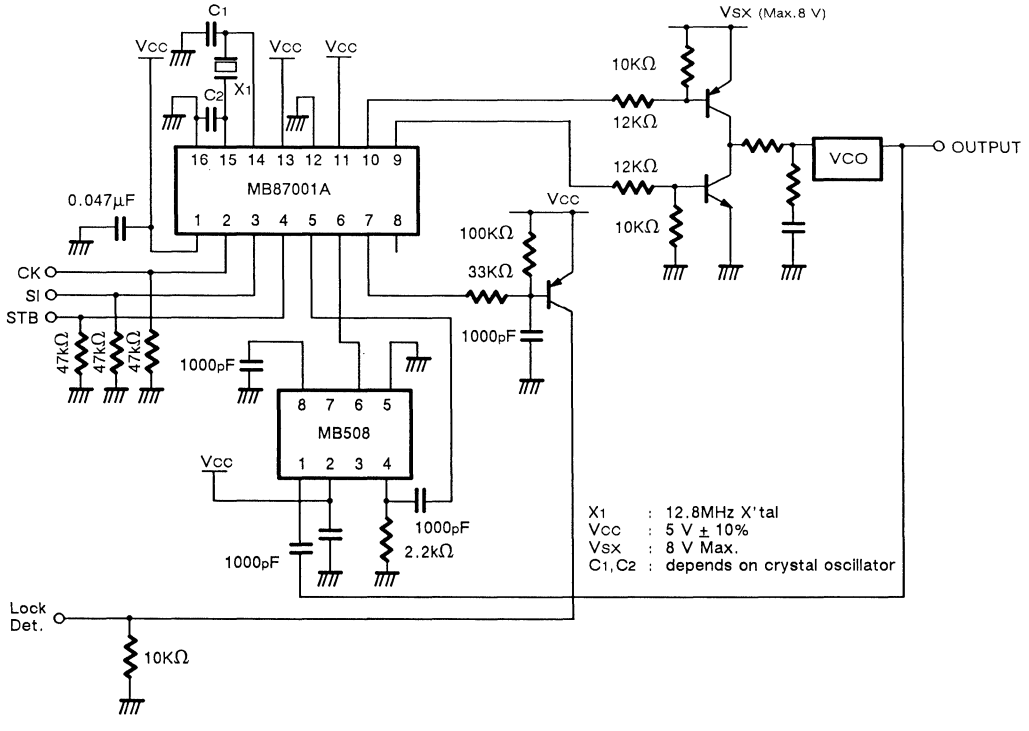


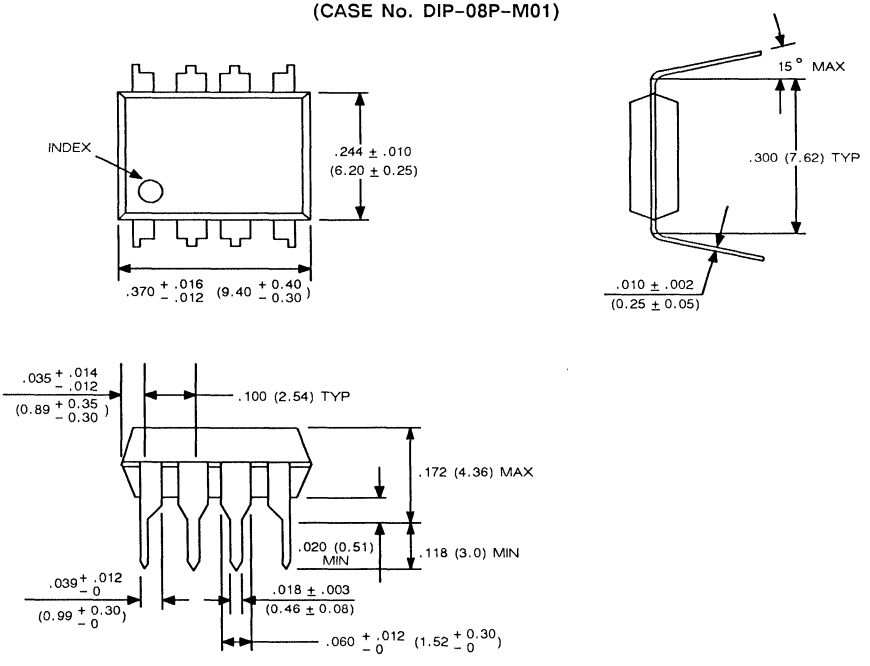
Fig. 4 – TYPICAL APPLICATION EXAMPLE



PACKAGE DIMENSIONS

(Suffix: P)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No. DIP-08P-M01)



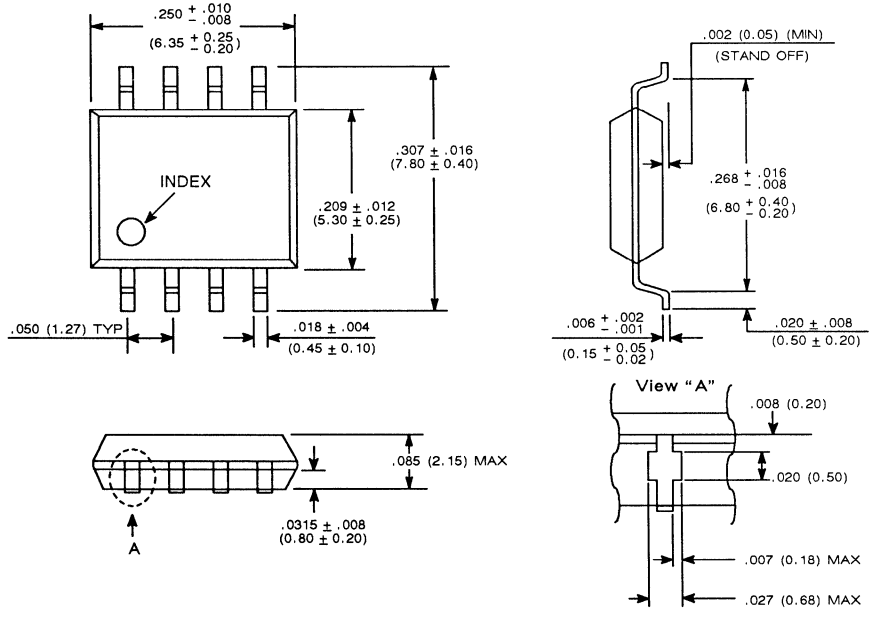
Dimensions in
inches (millimeters)

D08006S-2C

PACKAGE DIMENSIONS (Continued)

(Suffix: PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. FPT-08P-M01)



Dimensions in
inches (millimeters)

F08002S-2C

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FUJITSU

TWO MODULUS PRESCALER WITH STAND-BY MODE

MB509

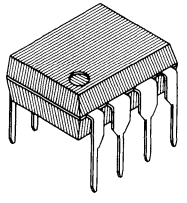
January 1988
Edition 1.0

TWO MODULUS PRESCALER WITH STAND-BY MODE

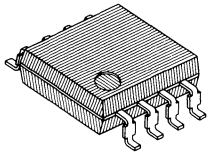
The Fujitsu MB509 is a low power two modulus prescaler which enables pulse swallow function. The MB509 is used in Phase Locked Loop (PLL) frequency synthesizer and divides the input frequency by the modulus of 64/65 or 128/129, respectively.

Power consumption is 58 mW typ. at power supply voltage of 5.0V. The MB509 is equipped with the stand by mode which cuts off the power supply current I_{CC} under PLL phase lock condition. (I_{CC} =180 μA under current cut condition)

- High Speed: fmax = 1.1 GHz max. (V_{IN} = 0.4 Vp-p)
- Pulse Swallow Function: 64/65, 128/129
- Power Supply Consumption: 58 mW typ.
- Stand-by Current: 180 μA typ.
- Stable Output Amplitude: V_O = 1.6 Vp-p typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer system block IC
- Plastic 8-pin Dual-In-Line Package (Suffix: –P)
  Plastic 8-pin Mini Flat Package (Suffix: –PF)
- Built-in a Terminal Resistor
  Stable output amplitude is obtained up to output load capacitance of 8 pF.

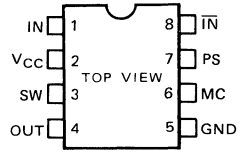


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



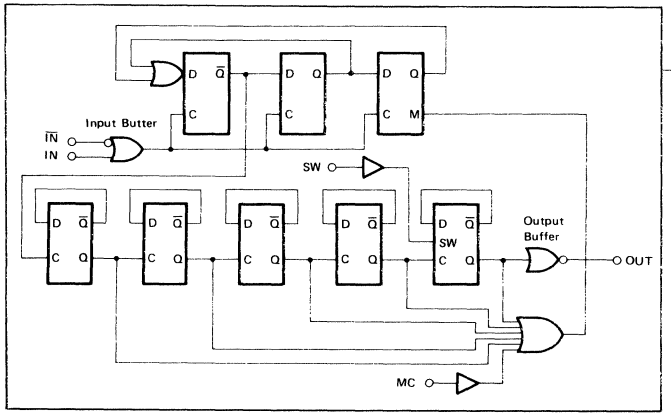
ABSOLUTE MAXIMUM RATINS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB509 BLOCK DIAGRAM



PS	SW	MC	Divide Ratio
H	H	H	1/64
H	H	L	1/65
H	L	H	1/128
H	L	L	1/129
L	–	–	Stand-by mode

Note: SW: H = V_{CC}, L = open
MC: H = 3.0V to V_{CC},
L = GND to 0.8V
PS: H = 2.0V to V_{CC},
L = GND to 0.4V

PIN DESCRIPTION

Pin Number	Symbol	Description
1	IN	Input
2	V_{CC}	Power Supply, +5V
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	PS	Stand-by Control Input (See Divide Ratio Table)
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

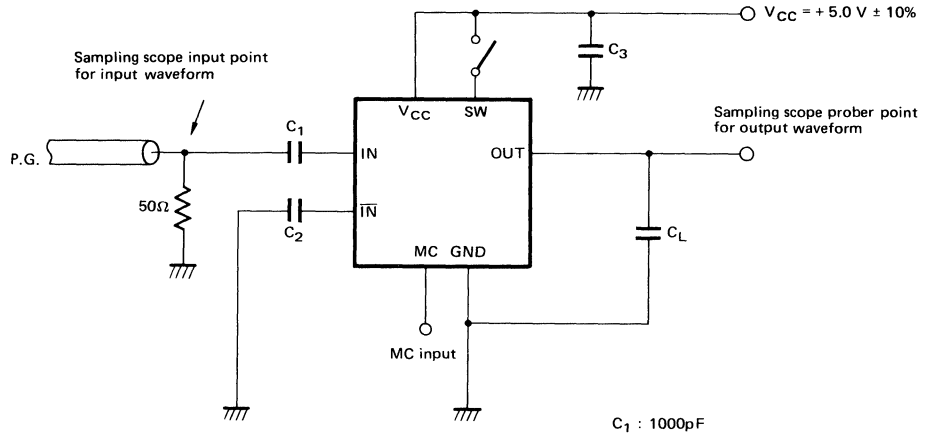
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	-40	–	+85	°C
Load Capacitance	CL	–	–	8	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}		–	11.6	–	mA
	I_{PS}	Stand-by mode	–	180	–	μA
Output Amplitude	V_O	Built-in a Terminal Resitor. Load capacitance = 8pF	1.0	1.6	–	Vp-p
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	10	–	1100	MHz
Input Siganl Amplitude	V_{IN}	–	0.4	–	2.0	Vp-p
High Level Input Voltage for MC	V_{IH}	–	3.0	–	–	V
Low Level Input Voltage for MC	V_{IL}	–	–	–	0.8	V
High Level Input Voltage for PS	V_{IH}	–	2.0	–	–	V
Low Level Input Voltage for PS	V_{IL}	–	–	–	0.4	V
High Level Input Current for MC	I_{IH}	V_{IH} = 3.0V, V_{IL} = 0.8V	–	–	0.4	mA
Low Level Input Current for MC	I_{IL}		-0.2	–	–	mA
Modulus Set-up Time MC to Output	t_{SET}	–	–	16	26	ns

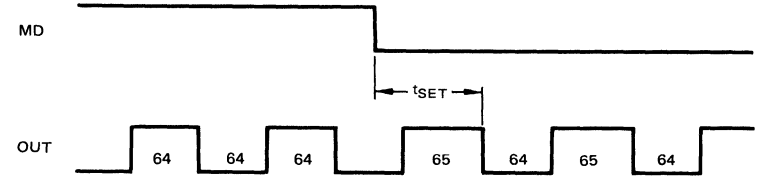
Fig. 2 – TEST CIRCUIT



C_1 : 1000pF
C_2 : 1000pF
C_3 : 0.1μF
C_L : 8 pF (including scope and jig capacitance)
PS pin is open.

TWO MODULUS OPERATING TIMING CHART

Example. Divide Ratio of 128/129



Notes:
When divide ratio of 129 is selected, positive pulse is added by one to 65.

The typical set up time is 16 ns from the MD signal input to the timing of change of prescaler divide ratio.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

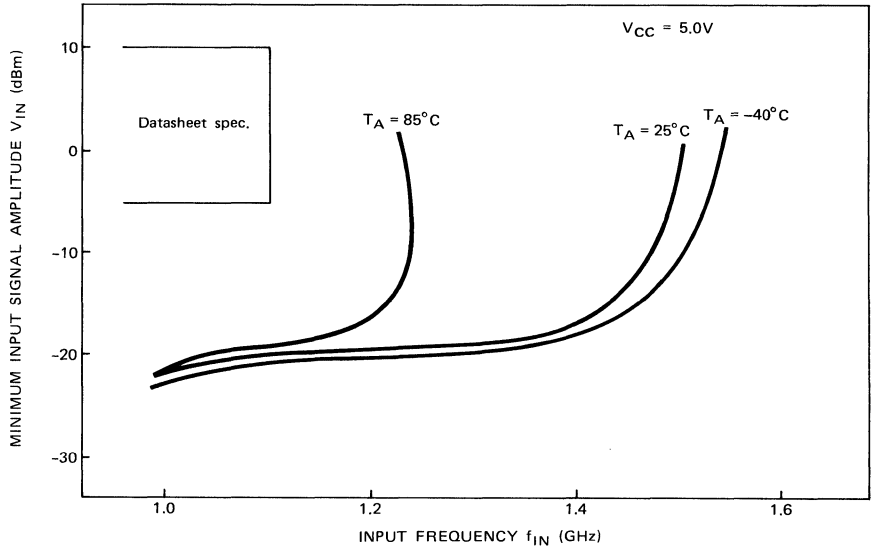
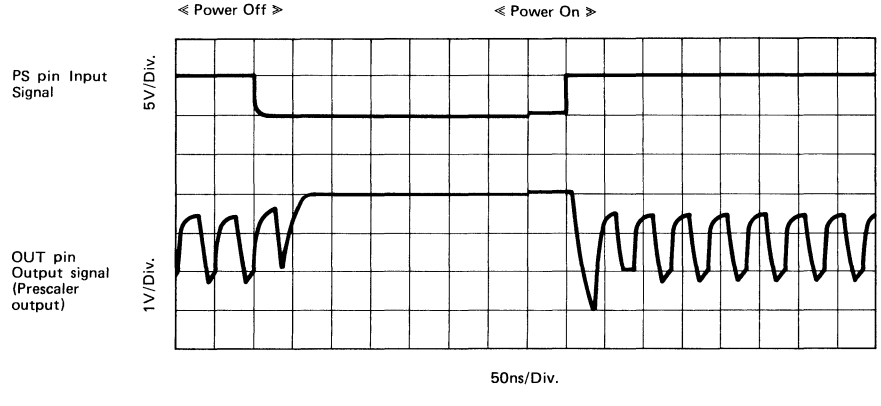


Fig. 4 – WAVEFORM OF STAND BY MODE

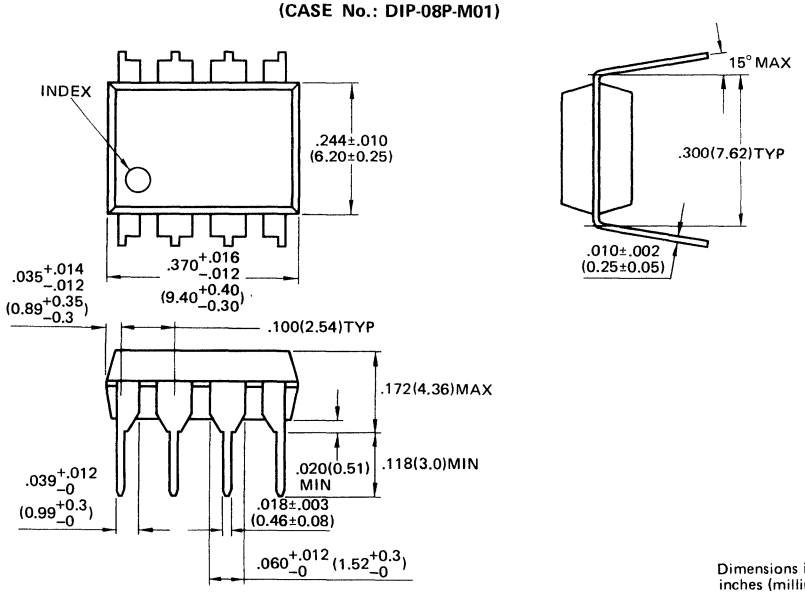


Note: About 50 ns of set up time is required for both power on/off.

PACKAGE DIMENSIONS

(Suffix: -P)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)

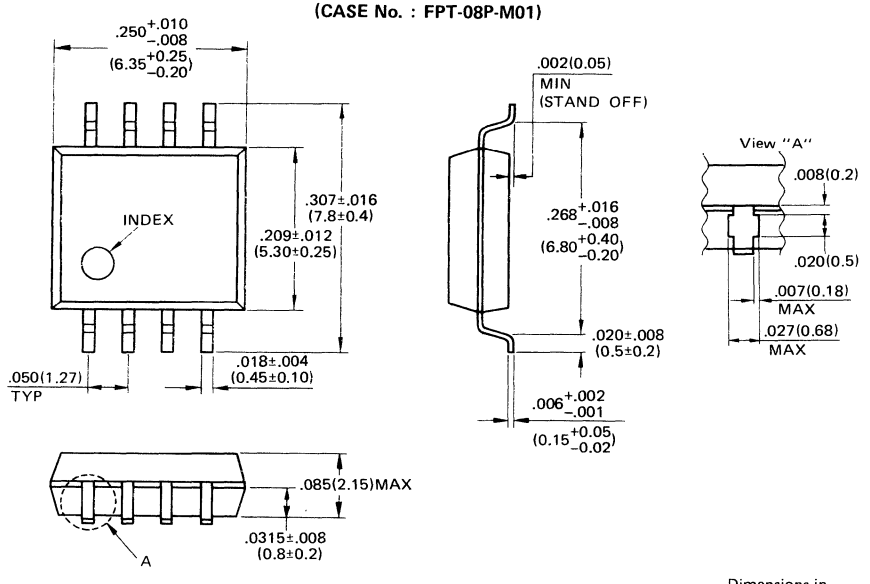


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Cont'd)

(Suffix: -PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in
inches (millimeters)

FUJITSU

MB509

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FUJITSU

2.7 GHz TWO MODULUS PRESCALER

MB510

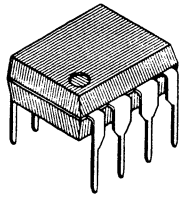
TS587-A882
February 1988

2.7 GHz TOW MODULUS PRESCALER

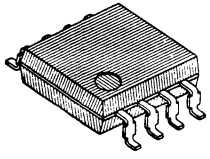
The Fujitsu MB510 is a ultra high speed two modulus prescaler which enables pulse swallow function. The MB510 is used in Phase Locked Loop (PLL) frequency synthesizer and divides the input frequency by the modulus of 128/144 or 256/272, respectively

The MB510 achieves extremely small stray capacitance of internal element, realized through the use of Fujitsu Advanced Process Technology. As the results, ultra high speed is achieved with low power supply current of 10 mA typ.

- High Speed: fmax = 2.7 GHz max. (V_{IN} = 0.4 Vp-p)
- Pulse Swallow Function: 128/144, 256/272
- Low Supply Current : 10 mA typ.
- Stable Output Amplitude: V_O = 1.6 Vp-p typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer system block IC
- Plastic 8-pin Dual-In-Line Package (Suffix: –P)
  Plastic 8-pin Mini Flat Package (Suffix: –PF)
- Built-in a Terminal Resistor
  Stable output amplitude is obtained up to output load capacitance of 8 pF.

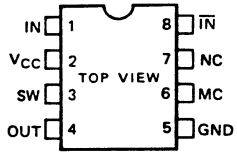


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



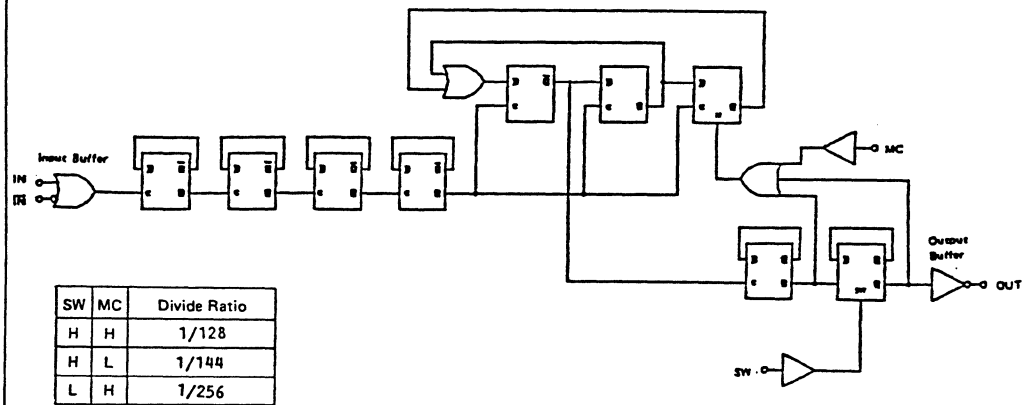
ABSOLUTE MAXIMUM RATINS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	I_O	10	mA
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB510 BLOCK DIAGRAM



SW	MC	Divide Ratio
H	H	1/128
H	L	1/144
L	H	1/256
L	L	1/272

Note: SW: H = V_{CC}, L = open
MC: H = 2.0V to V_{CC},
L = GND to 0.8V

PIN DESCRIPTION

Pin Number	Symbol	Description
1	IN	Input
2	V_{CC}	Power Supply, +5V
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

RECOMMENDED OPERATING CONDITIONS

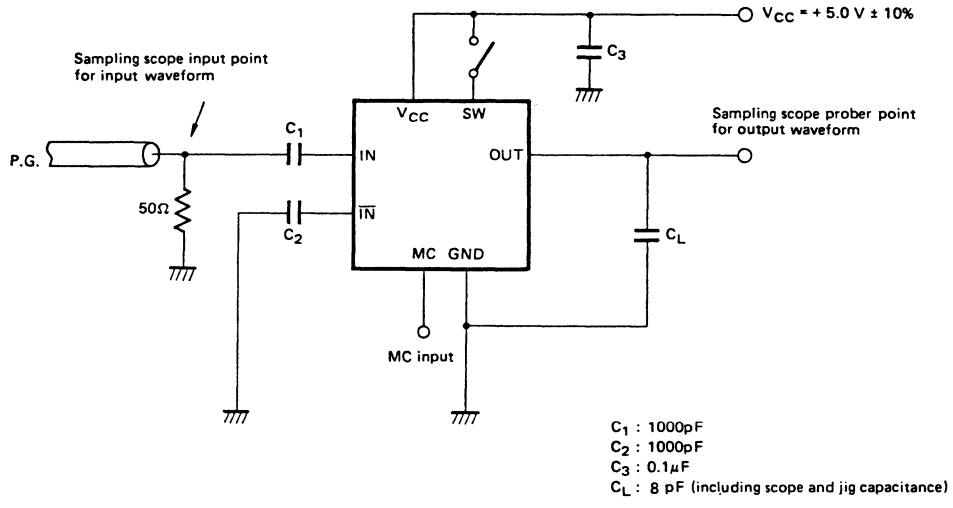
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating Temperature	T_A	-40	–	+85	°C
Load Capacitance	CL	–	–	8	pF

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

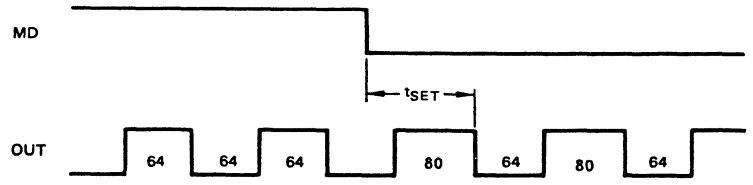
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}		–	10.0	15.0	mA
Output Amplitude	V_O	Built-in a Terminal Resitor. Load capacitance = 8pF	1.0	1.6	–	Vp-p
Input Frequency	f_{IN}	With input coupling capacitor 1000pF	10	–	2700	MHz
Input Siganl Amplitude	V_{IN}	fin = 2200 to 2700 MHz	0.4	–	1.2	Vp-p
Input Siganl Amplitude	V_{IN}	fin = 10 to 2200 MHz	0.2	–	1.2	Vp-p
High Level Input Voltage for MC	V_{IH}	–	3.0	–	–	V
Low Level Input Voltage for MC	V_{IL}	–	–	–	0.8	V
High Level Input Current for MC	I_{IH}	V_{IH} = 2.0V, V_{IL} = 0.8V	–	–	0.4	mA
Low Level Input Current for MC	I_{IL}		-0.2	–	–	mA
Modulus Set-up Time MC to Output	t_{SET}	–	–	16	26	ns

Fig. 2 – TEST CIRCUIT



TWO MODULUS OPERATING TIMING CHART

Example. Divide Ratio of 128/144



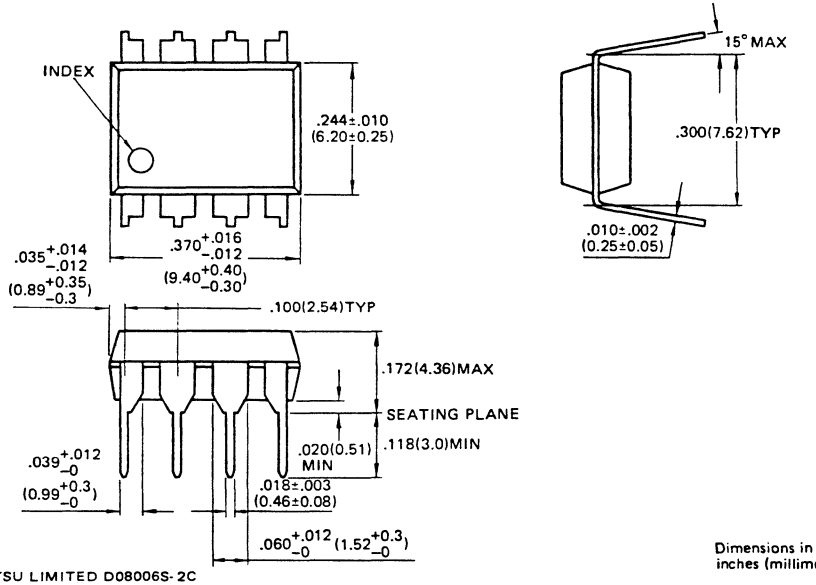
Notes:
When divide ratio of 144 is selected, positive pulse is added by 16 to 80

The typical set up time is 16 ns from the MD signal input to the timing of change of prescaler divide ratio.

PACKAGE DIMENSIONS

(Suffix: P)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



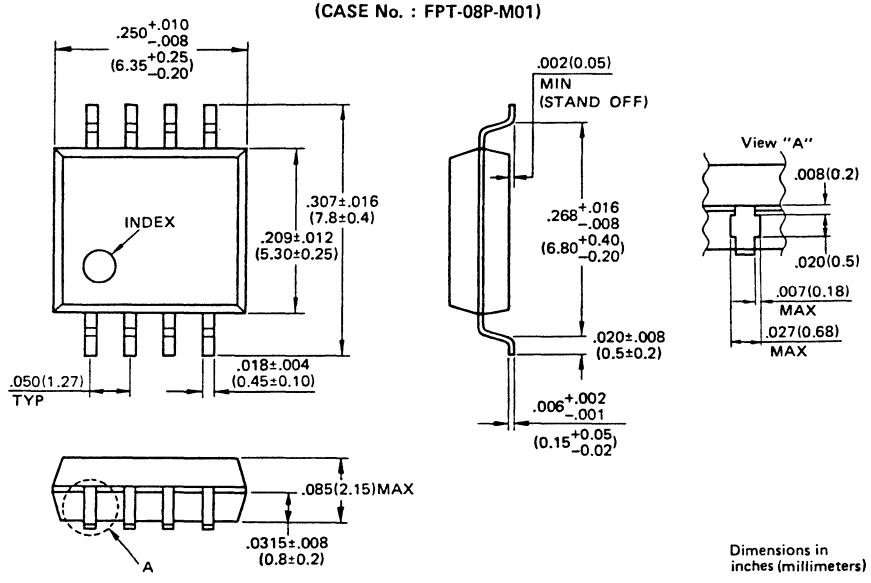
Dimensions in inches (millimeters)

1

PACKAGE DIMENSIONS

(Suffix: PF)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches (millimeters)

Section 2

Phase Lock Loops (PLL)

FUJITSU

CMOS PLL FREQUENCY SYNTHESIZER SYSTEM BLOCK

MB87001A

July 1987
Edition 3.0

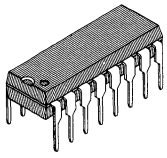
CMOS SERIAL INPUT Phase-Locked-Loop (PLL) FREQUENCY SYNTHESIZER SYSTEM BLOCK

The Fujitsu MB 87001A is designed for the PLL Frequency Synthesizer with the MB 501 Dual Modulus Prescaler. The MB 87001A contains a Crystal Oscillator Circuit, a Digital Controlled Reference Frequency Divider, a Phase Detector, a Charge Pump, 17-bit Shift Register, 17-bit Latch, Binary 7-bit Swallow Counter, Binary 10-bit Programmable Counter, and control circuit for the prescaler.

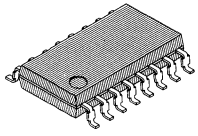
- Power Supply Voltage: 2.7 to 5.5V
- Wide Operation Temperature Range: –40 to +85°C
- Inverter for oscillator
- 17-bit Programmable Divider with Input Buffer Amplifier
- Binary 7-bit Swallow Counter plus Binary 10-bit Programmable Counter
- 11-bit Programmable Reference Divider with control circuit
- 8 divided factors for reference frequency selected by external input S_1 thru S_3
  8, 16, 64, 128, 256, 512, 1024, 2048
- Divided factor for Programmable Dividers is input as serial data bit
- 2 types of Phase Detector Output
  Bult-in Charge Pump Output
  Output for External Charge Pump
- Easy to make up PLL system with Dual Modulous Prescaler ICs MB 50X
- 16-pin Standard Dual-in-line Package (DIP) and 16-pin Flat Package.
- Pulse Swallow Function

  $f_{VCO} = [(N \times M) + A] \times f_r$

  f_{VCO} : VCO (Voltage Controlled Oscillator) Output Frequency
  N : Preset Divided Factor of Binary 10-bit Programmable Counter (16 through 1023) : N should be greater than A.
  M : Preset Modulus Factor of external two modulus prescaler (64 in 64/65 mode, 128 in 128/129 mode)
  A : Preset Divided Factor of Binary Swallow Counter (0 through 127)
  f_r : Output Frequency of Reference Frequency Divider



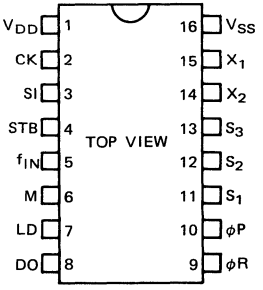
PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

2

PIN ASSIGNMENT



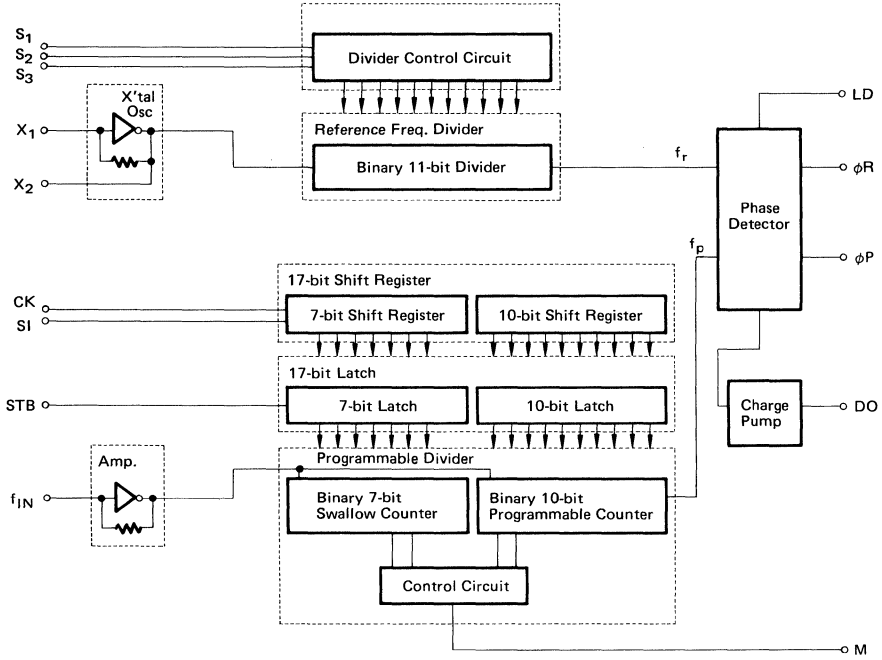
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	GND–0.5 to GND+7.0	V
Input Voltage	V_I	GND–0.5 to V_{DD}+0.5	V
Output Voltage	V_O	GND–0.5 to V_{DD}+0.5	V
Output Current	I_O	±10	mA
Open-drain Output	V_{OOP}	GND–0.5 to V_{DD}+3.0	V
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–65 to +150	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 87001A BLOCK DIAGRAM



PIN NAME TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	–	V_{DD}	9	O	ϕR
2	I	CK	10	O	ϕP
3	I	SI	11	I	S_1
4	I	STB	12	I	S_2
5	I	f_{in}	13	I	S_3
6	O	M	14	O	X_2
7	O	LD	15	I	X_1
8	O	DO	16	–	V_{SS}

PIN DESCRIPTION

Pin No.	Symbol	Function
1	V_{DD}	Power Supply Voltage
2	CK	Clock signal input for 17-bit Shift Register. Serial input is valid at the rising edge of CK.
3	SI	Serial Data Input for 17-bit Shift Register. See SERIAL DATA INPUT FOR PROGRAMMABLE DIVIDER.
4	STB	Strobe signal input for transfer the data of 17-bit Shift Register to 17-bit Latch. The operation is executed when STB is at High level.
5	f_{IN}	Input for Binary 7-bit Swallow Counter and Binary 10-bit Programmable Counter. This input involves bias circuit and amplifier. The connection with Dual Modulus Prescaler should be AC connection.
6	M	Control output for Dual Modulus Prescaler. The connection with the prescaler should be DC connection. Pulse Swallow Function: MB 501: M = High : Preset Module Factor 64 or 128 M = Low : Preset Module Factor 65 or 129
7	LD	Output of Phase Comparator; It is at High level when f_r and f_p are coherent, and then the loop is locked. Otherwise it outputs pulse signal.
8	DO	Three-stage Charge Pump Output; The mode of DO is changed by the combination of Reference Freq. Divider output frequency f_r and Programmable Divider output frequency f_p as listed below: $f_r > f_p$: Drive Mode (DO = High) $f_r = f_p$: High-Impedance Mode $f_r < f_p$: Sink Mode (DO = Low)
9 10	ϕR ϕP	Outputs for external charge pump. Note that ϕP is an N-ch open-drain output. ϕR ϕP $f_r > f_p$: Low : Low $f_r = f_p$: Low : High-Impedance $f_r < f_p$: High : High-Impedance
11 12 13	S_1 S_2 S_3	Control Inputs for Reference Frequency Divider. The combination of these inputs provides divided factor to Reference Frequency Divider. Divided Factor 8 16 64 128 256 512 1024 2048 S_1 0 1 0 1 0 1 0 1 S_2 0 0 1 1 0 0 1 1 S_3 0 0 0 0 1 1 1 1
14	X_2	Pin for Crystal Oscillator; Output pin of the inverting amplifier. This pin should be open when an external oscillator is used.
15	X_1	Pin for Crystal Oscillator; Input pin of the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupling when an external oscillator is used, but for large amplitude signals (standard CMOS levels), DC coupling may also be used.
16	V_{SS}	Ground

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage (V_{SS} = 0V)	V_{DD}	2.7 to 5.5	V
Input Voltage	V_I	GND to V_{DD}	V
Operating Ambient Temperature	T_A	−40 to +85	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V, T_A = −40 to +85°C)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	All inputs except f_{IN} and X_1	V_{IH}	3.5	–	–	V
Low-level Input Voltage	All inputs except f_{IN} and X_1	V_{IL}	–	–	1.5	V
Input Sensitivity of f_{IN}	Sine wave AC coupling	V_{fpp}	1.0	–	–	Vp-p
Input Sensitivity of X_1	Sine wave AC coupling	V_{sin}	1.5	–	–	Vp-p
High-level Input Current	All inputs except f_{IN} and X_1 $V_I = V_{DD}$	I_{IH}	–	1.0	–	μA
Low-level Input Current	All inputs except f_{IN} and X_1 V_I = GND	I_{IL}	–	-1.0	–	μA
Input Current of f_{IN}	V_I = GND to V_{DD}	I_{fIN}	–	±50	–	μA
Input Current of X_1	V_I = GND to V_{DD}	I_{X1}	–	±50	–	μA
High-level Output Voltage	All outputs except φP and X_2 I_{OH} = 0μA	V_{OH}	4.95	–	–	V
Low-level Output Voltage	All outputs except φP and X_2 I_{OL} = 0μA	V_{OL}	–	–	0.05	V
Low-level Output Voltage of φP	I_{OL} = 2mA	V_{OLP}	–	–	1.0	V
High-level Output Voltage of X_2	I_{OH} = 0μA	V_{OHX}	4.50	–	–	V
Low-level Output Voltage of X_2	I_{OL} = 0μA	V_{OLX}	–	–	0.50	V
High-level Output Current	All outputs except φP and X_2 V_{OH} = 4.0V	I_{OH}	-1.0	–	–	mA
Low-level Output Current	All outputs except φP and X_2 V_{OL} = 0.8V	I_{OL}	1.0	–	–	mA
N-ch. Open Drain Cut-off Current	φP only $V_O = V_{DD}$ + 3.0V	I_{OFF}	–	1.0	–	μA
Power Supply Current	See Note *	I_{DD}	–	3.0	–	mA
Maximum Operation Frequency	Divider Unit: Ref. Freq. Divider	f_{maxd}	15	25		MHz
Maximum Operation Frequency	Prog. Counter 7/10 bit Counter	f_{maxp}	13	25		MHz

Note *: f_{IN} = 5.0 MHz using 12.8 MHz X'tal. All inputs except f_{IN} are connected with GND. All outputs are open.

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.0V, T_A = −40 to +85°C)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	All inputs except f_{IN} and X_1	V_{IH}	2.1	–	–	V
Low-level Input Voltage	All inputs except f_{IN} and X_1	V_{IL}	–	–	0.9	V
Input Sensitivity of f_{IN}	Sine wave AC coupling	V_{fpp}	0.8	–	–	Vp-p
Input Sensitivity of X_1	Sine wave AC coupling	V_{sin}	1.0	–	–	Vp-p
High-level Input Current	All inputs except f_{IN} and X_1 $V_I = V_{DD}$	I_{IH}	–	1.0	–	μA
Low-level Input Current	All inputs except f_{IN} and X_1 V_I = GND	I_{IL}	–	-1.0	–	μA
Input Current of f_{IN}	V_I = GND to V_{DD}	I_{fIN}	–	±30	–	μA
Input Current of X_1	V_I = GND to V_{DD}	I_{X1}	–	±30	–	μA
High-level Output Voltage	All outputs except ϕP and X_2 $I_{OH} = 0\mu A$	V_{OH}	2.95	–	–	V
Low-level Output Voltage	All outputs except ϕP and X_2 $I_{OL} = 0\mu A$	V_{OL}	–	–	0.05	V
Low-level Output Voltage of ϕP	I_{OL} = 0.8mA	V_{OLP}	–	–	0.8	V
High-level Output Voltage of X_2	$I_{OH} = 0\mu A$	V_{OHX}	2.5	–	–	V
Low-level Output Voltage of X_2	$I_{OL} = 0\mu A$	V_{OLX}	–	–	0.50	V
High-level Output Current	All outputs except ϕP and X_2 V_{OH} = 2.0V	I_{OH}	-0.5	–	–	mA
Low-level Output Current	All outputs except ϕP and X_2 V_{OL} = 0.8V	I_{OL}	0.5	–	–	mA
N-ch. Open Drain Cut-off Current	ϕP only $V_O = V_{DD}$ + 3.0V	I_{OFF}	–	1.0	–	μA
Power Supply Current	See Note *	I_{DD}	–	2.0	–	mA
Maximum Operation Frequency	Divider Unit: Ref. Freq. Divider	f_{maxd}	13	20		MHz
Maximum Operation Frequency	Prog. Counter 7/10 bit Counter	f_{maxp}	10	20		MHz

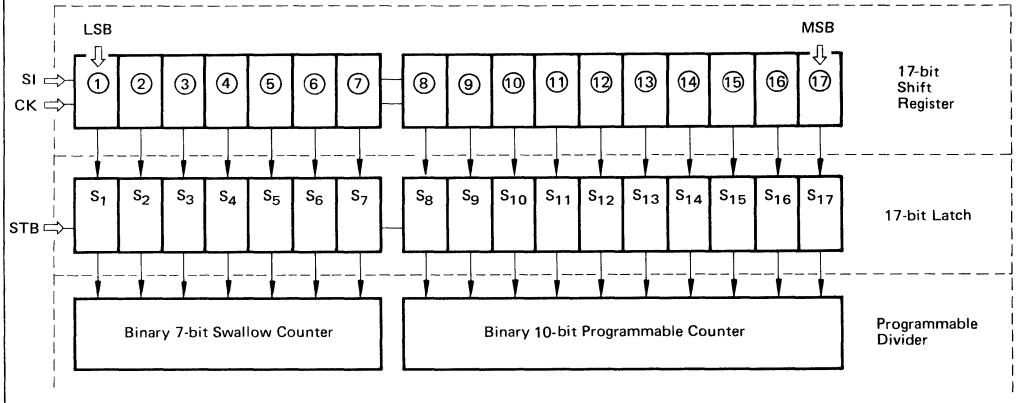
Note *: f_{IN} = 5.0 MHz using 12.8 MHz X'tal. All inputs except f_{IN} are connected with GND. All outputs are open.

2

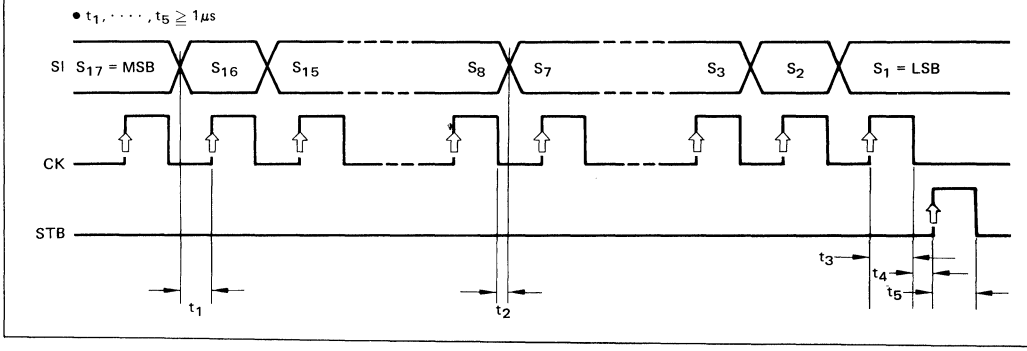
SERIAL DATA INPUT FOR PROGRAMMABLE DIVIDER

The Divided factor of the programmable divder is provided by the 17-bit latch. The data of the latch is transferred from the 17-bit shift register at the rising edge of strobe signal STB. The shift register has a serial input with clock input. A divided factor is input from MSB as illustrated in TIMING CHART.

Fig. 2 – Block Diagram of Programmable Divider



Timing Chart



Binary 7-bit Swallow Counter Data Input

Digit No. / Divided Factor	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
3	0	0	0	0	0	1	1
4	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.

Note:

- Divided Factor: 0 thru 127
- Depending the external prescaler's Divided Factor Swap, SW, the input data should be as follow:
  MB 501:
  - SW = "H": Bit 7 of the shift register should be "0."
  - SW = "L": Bit 7 is "0" or "1."

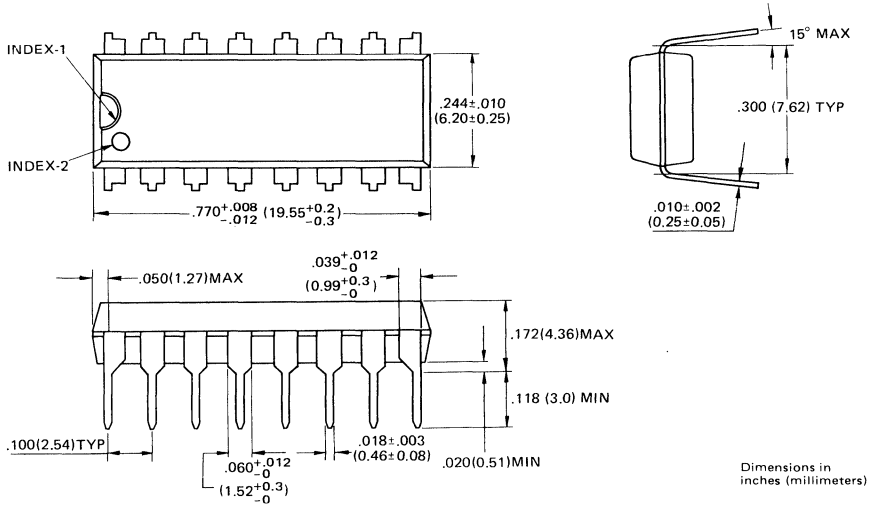
Binary 10-bit Programmable Data Input

Digit No. / Divided Factor	17	16	15	14	13	12	11	10	9	8
16	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	1	0	0	0	1
18	0	0	0	0	0	1	0	0	1	0
19	0	0	0	0	0	1	0	0	1	1
20	0	0	0	0	0	1	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.

Note: Divided factor less than 16 is prohibited.

PACKAGE DIMENSIONS

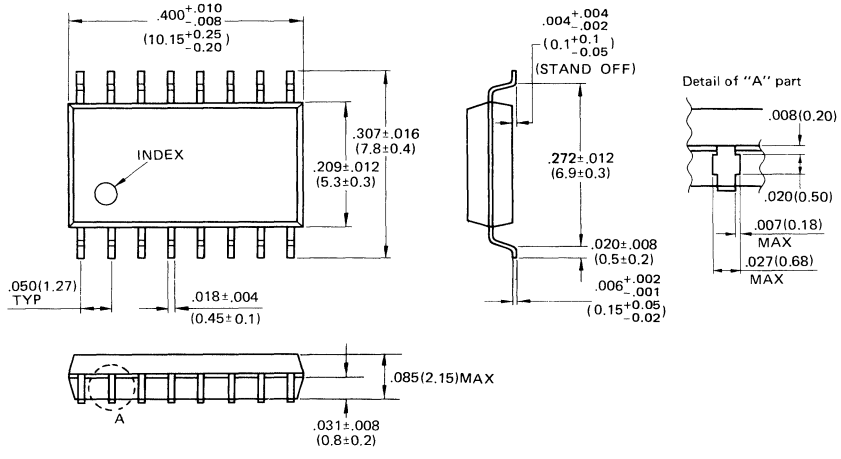
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
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CMOS PLL FREQUENCY SYNTHESIZER SYSTEM BLOCK

MB 87006A

November 1986
Edition 3.0

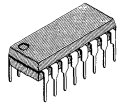
CMOS SERIAL INPUT Phase-Locked-Loop (PLL) FREQUENCY SYNTHESIZER SYSTEM BLOCK

The Fujitsu MB 87006A is designed for the PLL frequency synthesizer with the MB 501 Dual Modulus Prescaler. The MB 87006A contains a crystal oscillater circuit, a digital controlled referenced frequency divider, a phase detector, a charge pump, 17-bit shift register, 17-bit latch binary 7-bit swallow counter, binary 10-bit Programmable Counter, and control circuit for the prescaler.

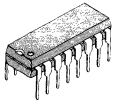
- Single Power Supply Voltage
- Wide Operation Temperature Range
- Inverter for oscillater
- 17-bit Programmable Divider with Input Buffer Amplifier
  Binary 7-bit Swallow Counter plus Binary 10-bit Programmable Counter
- 14-bit Programmable Reference Divider with Input Buffer Amplifier
  Binary 14-bit Programmable Reference Counter
- Divided factor for Programmable Dividers is input as serial data with a control bit
- 2 types of Phase Detector output
  Built-in Charge Pump output
  Output for External Charge Pump
- Easy to make up PLL system with Dual Modulous Prescaler IC MB 501, which works upto 1 GHz.
- 16-pin Standard Dual-in-line package (DIP)
- Pulse Swallow Function

$f_{VCO} = \{(N \times M) + A\} \times f_R \div R$

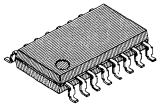
f_{VCO} : VCO (Voltage Controlled Oscillator) Output Frequency
N : Preset Divided Factor of Binary 10-bit Programmable Counter (16 through 1023) : N should be greater than A.
M : Preset Modulus Factor of external two modulus prescaler (64 in 64/65 mode, 128 in 128/129 mode)
A : Preset Divided Factor of Binary Swallow Counter (0 through 127)
f_R : Output Frequency of Reference Frequency Divider
R : Preset Divided Factor of Binary 14-bit Programmable Reference Divider (8 thru 16383)



PLASTIC PACKAGE
DIP-16P-M02

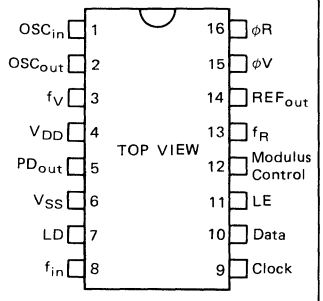


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

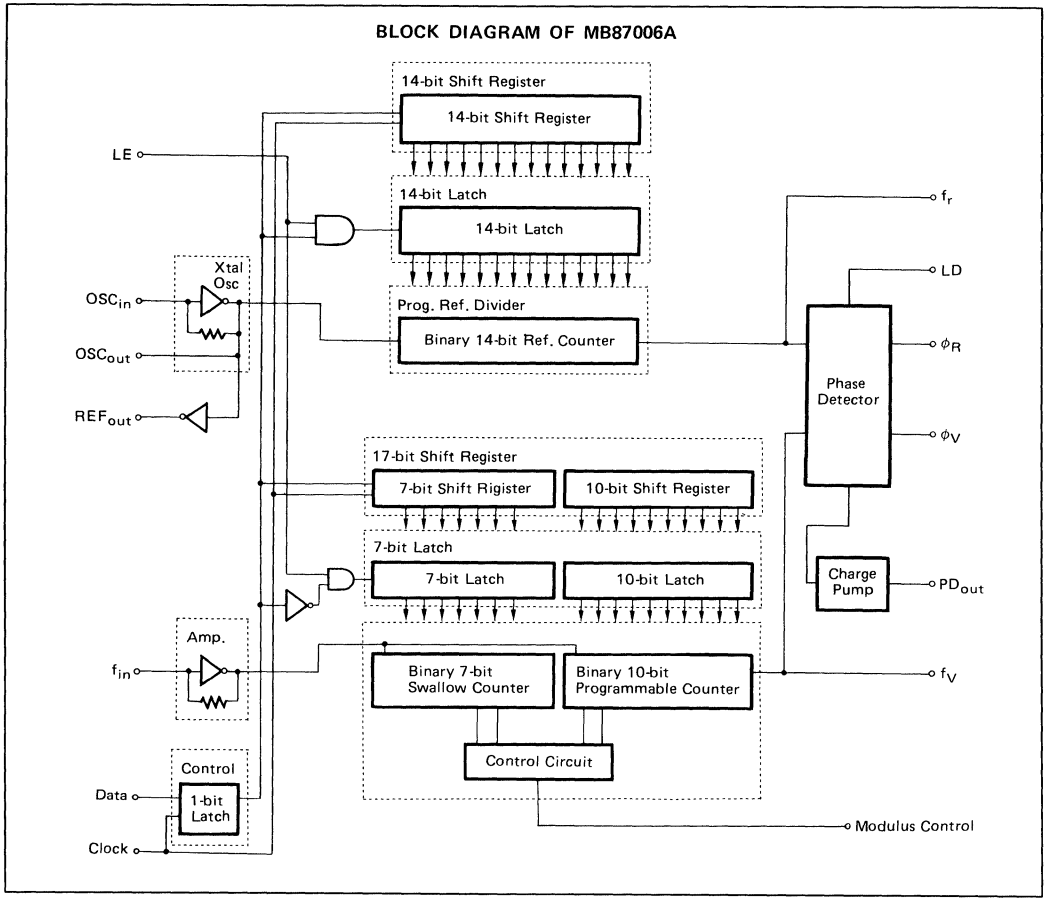
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	GND-0.5 to GND+7.0	V
Input Voltage	V_I	GND-0.5 to V_{DD}+0.5	V
Output Voltage	V_O	GND-0.5 to V_{DD}+0.5	V
Output Current	I_O	±10	mA
Operating Ambient Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

BLOCK DIAGRAM OF MB87006A



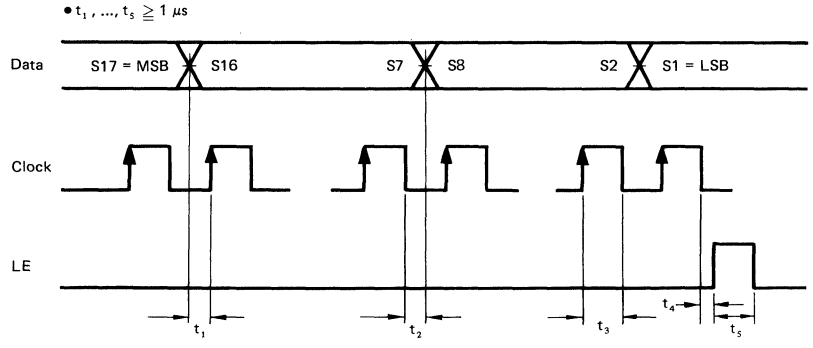
PIN NAME TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	I	OSC_{in}	9	I	Clock
2	O	OSC_{out}	10	I	Data
3	O	f_V	11	I	LE
4	–	V_{DD}	12	O	Modulus Control
5	O	PD_{out}	13	O	f_R
6	–	V_{SS}	14	O	REF_{out}
7	O	LD	15	O	ϕV
8	I	f_{in}	16	O	ϕR

PIN DESCRIPTION

Pin No.	Symbol	Function
1	OSC_{in}	Pin for Crystal Resonator; Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupling when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also used.
2	OSC_{out}	Pin for Crystal Resonator; Output of the inverting amplifier. This pin should be connected to open when an external oscillator is used.
3	f_V	Monitor output of the phase comparator input; as well as monitoring the output of the programmable divider
4	V_{DD}	Power Supply Voltage
5	PD_{out}	Three-state Charge Pump Output; The mode of PD_{OUT} is changed by the combination of Reference Divider output frequency f_R and Programmable Divider output frequency f_V as listed below:
		$f_R > f_V$: Drive Mode (PD_{OUT} = High) $f_R = f_V$: High-Impedance Mode $f_R < f_V$: Sink Mode (PD_{OUT} = Low)
6	V_{SS}	Ground
7	LD	Output of Phase Comparator; It is at High level when f_R and f_V are coherent, and then the loop is locked. Otherwise it outputs pulse signal.
8	f_{in}	Input for Binary 7-bit Swallow Counter and Binary 10-bit Programmable Counter from VCO; The connection with Dual Modulus Prescaler should be AC connection. This input involves bias circuit and amplifier.
9	Clock	Clock signal input for 17-bit Shift Register and 14-bit Shift Register; Each rising edge of the clock makes one bit of the data shift into the shift register which specified by the last bit of the data (control bit).
10	Data	Serial data input with pull-up register for 17-bit Programmable Divider and 14-bit Programmable Reference Divider; This data is the divided factor of the divider, which is provided from the corresponded shift register. The last bit of the data is the control bit which specified destination shift register. The data is transferred to 14-bit Shift Register when the bit is at high level, and to 17-bit Shift Register when at low level.
11	LE	Load Enable Input; Data input is enabled when it is High.
12	Modulus Control	Control output for Dual Modulus Prescaler. The connection should be DC connection. Pulse Swallow Function: MB501: M = High : Module Factor 64 or 128 M = Low : Module Factor 65 or 129
13	f_R	Monitor output of the phase comparator input; as well as monitoring the output of the reference divider.
14	REF_{out}	Monitor output of the reference frequency; its output can be used as system clock for microprocessor, or reference oscillator for another PLL frequency synthesizer.
15 16	ϕ_V ϕ_R	Outputs for external charge pump. ϕ_R ϕ_V $f_R > f_V$: Low High $f_R = f_V$: High High $f_R < f_V$: High Low

Notes on Serial Data Input Timing



Note 1: Clock: Input of 17-bit Shift Register; Data is obtained at the edge of Clock.
Data: Serial Data Input of 17-bit Shift Register; External data is input from this terminal.
LE: Strobe Signal Input. The contents of 17-bit Shift Register or 14-bit Shift Register are transferred to 17-bit Latch or 14-bit Latch when it is at high-level. The value of the contents is the divided ratio of the programmable divider.

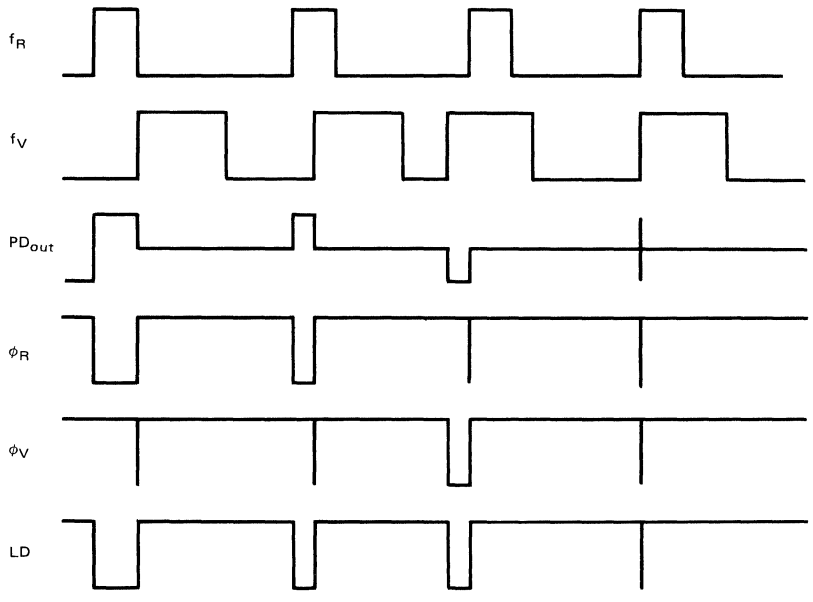
RECOMMENDED OPERTING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage (V_{SS} = OV)	V_{DD}	3.0 to 6.0	V
Input Voltage	V_I	GND to V_{DD}	V
Operating Ambient Temperature	T_A	-40 to +85	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V, T_A = -40 thru +85°)

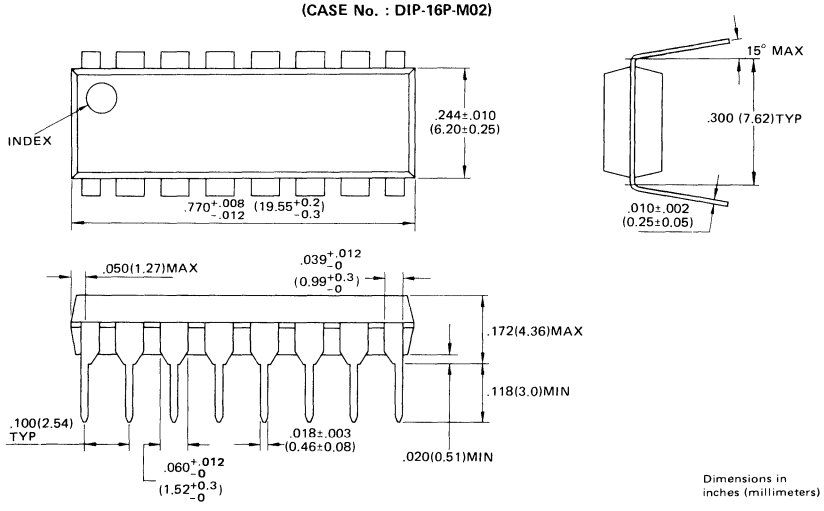
Parameter	Condition	Symbol	Min	Typ	Max	Unit
High-level Input Voltage except f_{in} and OSC_{in}		V_{IH}	V_{DD}x0.7			V
Low-level Input Voltage except f_{in} and OSC_{in}		V_{IL}			V_{DD}x0.3	V
Input Sensitivity (f_{in})	Amplitude in AC coupling, sine wave	V_{fpp}	0.5			V_{p-p}
Input Sensitivity (OSC_{in})	sine wave	V_{sin}	0.5			V_{p-p}
High-level Input Current except f_{in} and OSC_{in}	$V_I = V_{DD}$	I_{IH}		1.0		μA
Low-level Input Current except f_{in} and OSC_{in}	V_I = GND	I_{IL}		-1.0		μA
Input Current (f_{in})	V_I = GND thru V_{DD}	I_{fin}		±50		μA
Input Current (OSC_{in})	V_I = GND thru V_{DD}	I_{DSC}		±50		μA
Input Current (LE)	V_I = GND	I_{LE}		-60		μA
High-level Output Voltage except OSC_{OUT}	I_{OH} = 0μA	V_{OH}	4.95			V
Low-level Output Voltage except OSC_{OUT}	I_{OL} = 0μA	V_{OL}			0.05	V
High-level Output Current except OSC_{OUT} and Modulus Control	V_{OH} = 4.6V	I_{OH}	-1.0			mA
Low-level Output Current except OSC_{OUT} and Modulus Control	V_{OL} = 0.4V	I_{OL}	1.0			mA
High-level Output Current (Modulus Control)	V_{OH} = 4.6V	I_{OHM}	-1.5			mA
Low-level Output Current (Modulus Control)	V_{OL} = 0.4V	I_{OLM}	3.0			mA
Supply Current	f_{in} = 8.0 MHz, 11.5 MHz X'tal used between OSC_{in} and OSC_{OUT}, Inputs are at GND except f_{in} Outputs are open.	I_{DD}		3.5		mA
Max. Operation Freq. Reference Counter	V_{DD} = 5.0V	f_{maxd}	10	25		MHz
Max. Operation Freq. of Binary 7-bit Swallow Counter and Binary 10-bit Programmable Counter	V_{DD} = 5.0V	f_{maxp}	17	25		MHz

PHASE DETECTOR OUTPUT WAVEFORMS



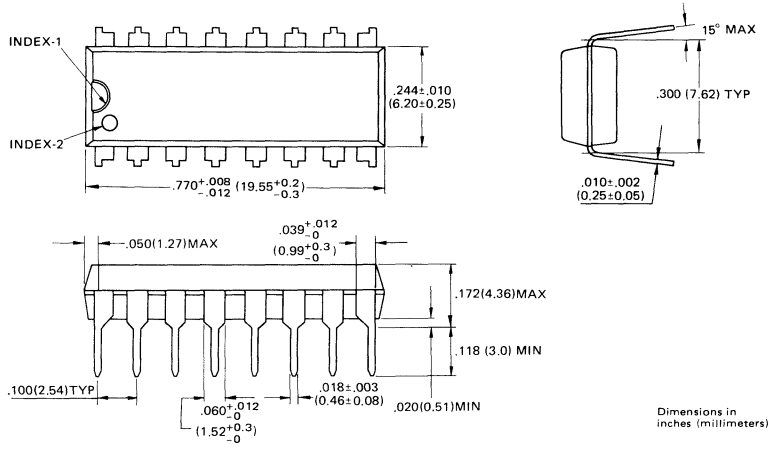
PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M02)



Dimensions in inches (millimeters)

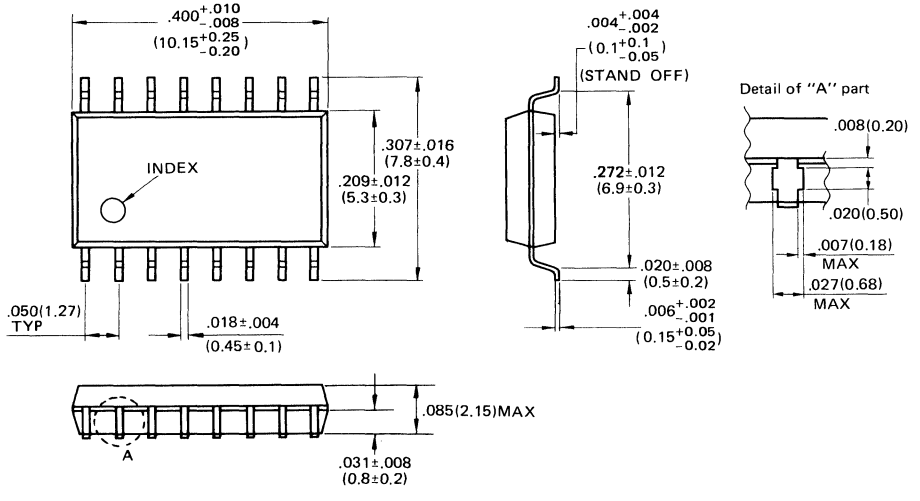
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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 Printed in Japan 0V2233-86YC3

FUJITSU

CMOS PLL FREQUENCY SYNTHESIZER

MB 87014

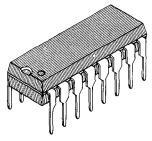
April 1987
Edition 2.0

CMOS SERIAL INPUT PLL Frequency Synthesizer

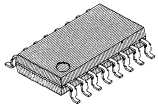
The Fujitsu MB 87014 is a single-chip PLL frequency synthesizer including an on-chip 180 MHz two-modulus prescaler.

MB 87014 contains a two-modulus prescaler, a crystal oscillation circuit, a digital controlled reference frequency divider, a phase detector, charge pumps, a 16-bit shift register, a 16-bit latch, a binary 6-bit swallow counter, a control register and a binary 10-bit programmable counter.

- On-chip 180 MHz two modulus prescaler
- 16-bit Programmable Divider
  (Binary 6-bit Swallow Counter plus Binary 10-bit Programmable Counter)
- 16-bit Programmable Reference Frequency Divider with Input Buffer Amplifier
- Divide factor for Programmable Dividers is input as serial data with a countrol bit
- 3 types of Phase Detector Outputs
  Built-in Charge Pump Output for Active Low Pass Filter
  Built-in Charge Pump Output for Passive Low Pass Filter
  Output for External Charge Pump
- Single Power Supply Voltage: +5 V
- Wide Operating Temperature Range: -30°C to +60°C
- 16-pin Standard Dual In-Line Package (DIP) and 16-pin Flat Package
- Pulse Swallow Function:
  $f_{VCO} = [(N_F \times M) + A] \times f_{XIN} \div N_R$
  f_{VCO} : VCO (Voltage Controlled Oscillator) Output Frequency
  N_F : Preset Divided Factor of Binary 10-bit Programmable Counter (5 through 1023) : N_F should be greater than A.
  M : Preset Modulus Factor of two-modulus prescaler (64/65)
  A : Preset Divided Factor of Binary 6-bit Swallow Counter (0 through 63)
  f_{XIN} : Output Frequency of an external oscillator
  N_R : Preset Divided Factor of Binary 16-bit Programmable Reference Frequency Divider (5 through 65535)

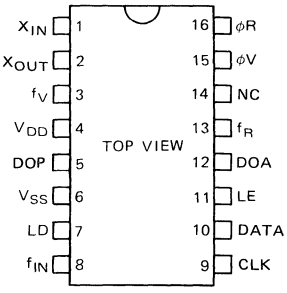


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



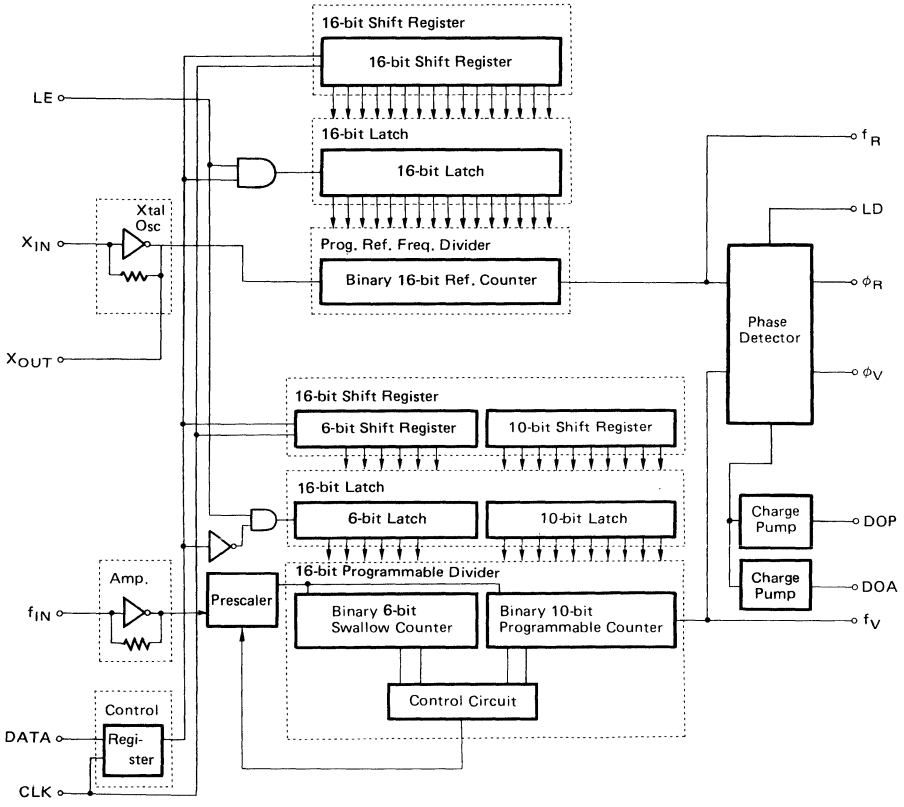
ABSOLUTE MAXIMUM RATINGS (V_{SS} = GND)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS}-0.3 to V_{SS}+6.0	V
Input Voltage	V_{IN}	V_{SS}-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	V_{SS}-0.3 to V_{DD}+0.3	V
Output Current	I_{OUT}	±10	mA
Operating Ambient Temperature	T_A	-30 to +80	°C
Storage Temperature	T_{STG}	-40 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 87014 BLOCK DIAGRAM



PIN NAME TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	I	X_{IN}	9	I	CLK
2	O	X_{OUT}	10	I	DATA
3	O	f_V	11	I	LE
4	–	V_{DD}	12	O	DOA
5	O	DOP	13	O	f_R
6	–	V_{SS}	14	–	NC
7	O	LD	15	O	ϕV
8	I	f_{IN}	16	O	ϕR

PIN DESCRIPTIONS

Pin No.	Symbol	Function
1	X_{IN}	Pin for Crystal Resonator; Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupling when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also used.
2	X_{OUT}	Pin for Crystal Resonator; Output of the inverting amplifier. This pin should be open when an external oscillator is used.
3	f_V	Monitor output of the phase comparator input; as well as monitoring the output of the programmable divider.
4	V_{DD}	Power Supply Voltage
5	DOP	Three-state Charge Pump Output; The mode of DOP is changed by the combination of the reference frequency divider output frequency f_R and the programmable divider output frequency f_V as listed below: $f_R > f_V$: Drive Mode (DOP = High) $f_R = f_V$: High-Impedance Mode $f_R < f_V$: Sink Mode (DOP = Low)
6	V_{SS}	Ground
7	LD	Output of Phase Comparator; LD is High when f_R and f_V are coherent, that is, the loop is locked. When the loop is not locked, a pulse signal is present at LD.
8	f_{IN}	Input for the Two-Modulus Prescaler from VCO; The connection with VCO should be AC connection. This input involves bias circuit and amplifier.
9	CLK	Clock signal input for the 16-bit Shift Register and the Control Register; Each rising edge of the clock makes one bit of the data shift into the shift register.
10	DATA	Serial data input with pull-up register for the programmable divider and the programmable reference frequency divider; This data is the divided factor of the divider, which is provided by the corresponded shift register. The last bit of the data is the control bit which specified destination shift register. The data is transferred to the 16-bit Shift Register when the bit is at high level, and to the 6/10 bit Shift Register when at low level.
11	LE	Load Enable Input; The contents of 6/10-bit Shift Register or 16-bit Shift Register are transferred to 6/10-bit latch or 16-bit Latch when it is at high level.
12	DOA	Three-state Charge Pump Output; The mode of DOA is changed by the combination of reference frequency divider output frequency f_R and the programmable divider output frequency f_V as listed below: $f_R > f_V$: Sink Mode (DOA = Low) $f_R = f_V$: High-Impedance Mode $f_R < f_V$: Drive Mode (DOA = High)
13	f_R	Monitor output of the phase comparator input; as well as monitoring the output of the reference frequency divider.
14	NC	Non connection.
15 16	ϕ_V ϕ_R	Outputs for external charge pump. ϕ_R ϕ_V $f_R > f_V$: Low High $f_R = f_V$: High High $f_R < f_V$: High Low

2

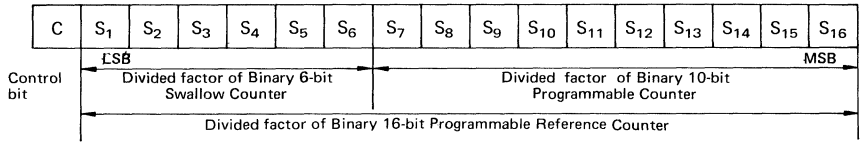
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage (V_{SS} = 0V)	V_{DD}	4.0 to 5.5	V
Input Voltage	V_{IN}	GND to V_{DD}	V
Operating Ambient Temperature	T_A	-30 to 60	°C

ELECTRICAL CHARACTERISTICS (V_{SS} = GND, V_{DD} = 5.0 V, T_A = -30°C to +60°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
High-level Input Voltage except f_{IN} and X_{IN}		V_{IH}	3.5			V
Low-level Input Voltage except f_{IN} and X_{IN}		V_{IL}			1.5	V
Input Sensitivity (f_{IN})	Amplitude in AC coupling, sine wave	V_{fpp}	1.0			$V_{p\text{-}p}$
Input Sensitivity (X_{IN})	Amplitude in AC coupling, sine wave	V_{sin}	1.0			$V_{p\text{-}p}$
High-level Input Current except f_{IN} and X_{IN}	$V_I = V_{DD}$	I_{IH}		1.0		μA
Low-level Input Current except f_{IN} and X_{IN}	$V_I = V_{SS}$	I_{IL}		-1.0		μA
Input Current (f_{IN})	$V_I = V_{SS}$ thru V_{DD}	I_{fIN}		±50		μA
Input Current (X_{IN})	$V_I = V_{SS}$ thru V_{DD}	I_{XIN}		±50		μA
High-level Output Voltage except X_{OUT}	I_{OH} = 0 μA	V_{OH}	4.95			V
Low-level Output Voltage except X_{OUT}	I_{OL} = 0 μA	V_{OL}			0.05	V
HIgh-level Output Current except X_{OUT}	V_{OH} = 4.6 V	I_{OH}	-1.0			mA
Low-level Output Current except X_{OUT}	V_{OL} = 0.4 V	I_{OL}	1.0			mA
Supply Current	f_{IN} = 180 MHz, 22 MHz X'tal used between X_{IN} and X_{OUT}, Inputs are at V_{SS} except f_{IN} Outputs are open.	I_{DD}		8.0		mA
Max. Operation Freq. for f_{IN}, Two-Modulus Prescaler	V_{DD} = 5.0 V	f_{maxps}	180	250		MHz
Max. Operation Freq. for X_{IN}, Binary 16-bit Reference Freq. Counter, Binary 6-bit Swallow Counter and Binary 10-bit Programmable Counter	V_{DD} = 4.0 V V_{DD} = 5.0 V	f_{maxc}	15 22	22 25		MHz

Fig. 2 – MB 87014 INPUT DATA FORMAT



Binary 6-bit Swallow Counter Data Input

Divided factor	Digit No.					
	6	5	4	3	2	1
0	0	0	0	0	0	0
1	0	0	0	0	0	1
.	.	.	.	.	.	.

Note: Divided factor: 0 to 63

Binary 10-bit Programmable Data Input

Divided factor	Digit No.									
	16	15	14	13	12	11	10	9	8	7
5	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.

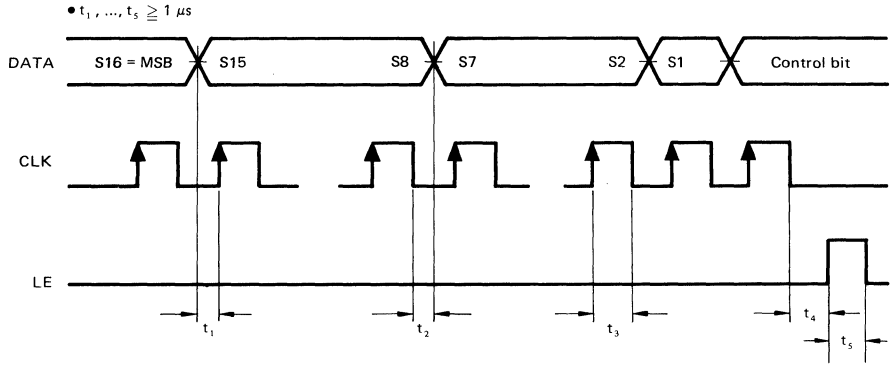
Note: Divided factor less than 4 is prohibited.
Divided factor: 5 to 1023

Binary 16-bit Counter Programmable Reference Data Input

Divided factor	Digit No.															
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
5	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.

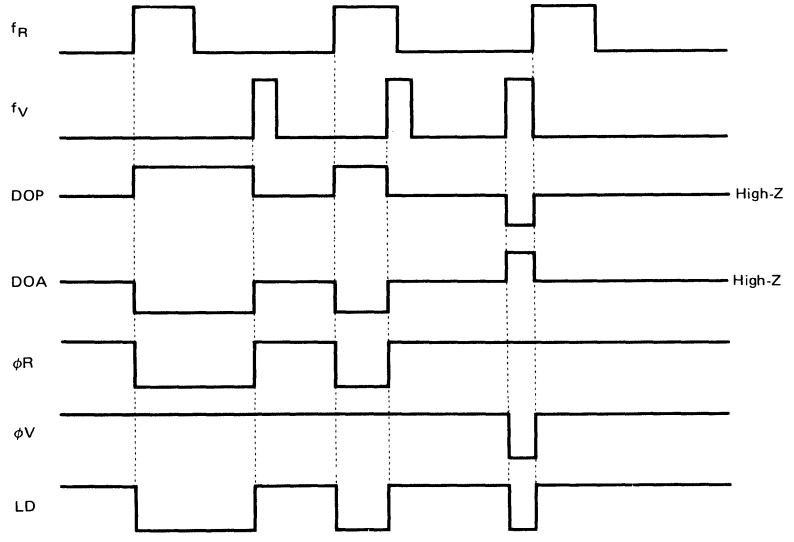
Note: Divided factor less than 4 is prohibited.
Divided factor: 5 to 65535

Fig. 3 – SERIAL DATE INPUT TIMING



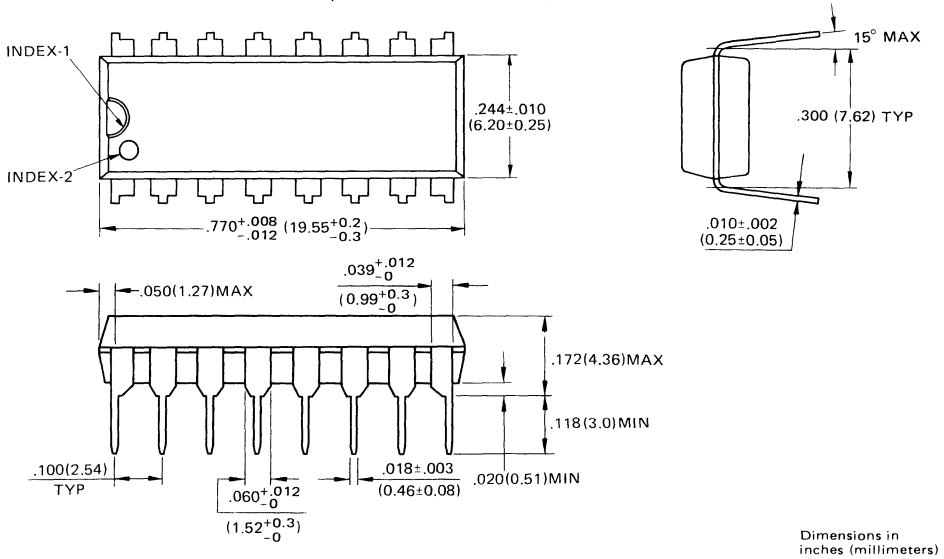
Note 1: CLK: Input of 16-bit Shift Register and the Control Register; Data is obtained at the edge of Clock.
DATA: Serial Data Input of 16-bit Shift Register and the Control Register; Serial data is input from this terminal.
LE: Load Enable Input. The contents of 6/10-bit Shift Register or 16-bit Shift Register are transferred to 6/10-bit Latch or 16-bit Latch when it is at high-level. The value of the contents is the divided ratio of the programmable divider.

Fig. 4 – PHASE DETECTOR OUTPUT WAVEFORM



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)

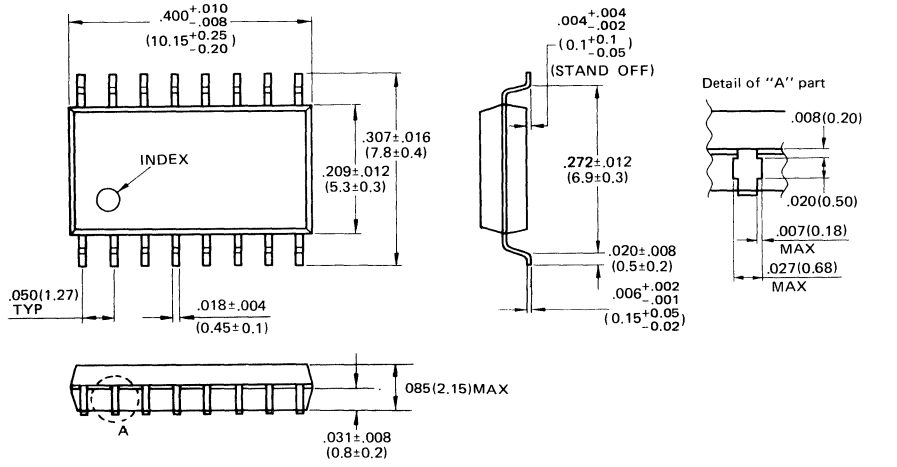


Dimensions in
inches (millimeters)

2

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

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FUJITSU

CMOS PLL FREQUENCY SYNTHESIZER SYSTEM BLOCK

MB87073

October 1987
Edition 1.0

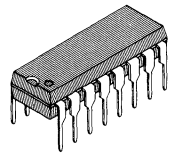
CMOS SERIAL INPUT Phase-Locked-Loop (PLL) FREQUENCY SYNTHESIZER SYSTEM BLOCK

The Fujitsu MB87073 is designed for the PLL Frequency Synthesizer with the MB501 Dual Modulus Prescaler. The MB87073 contains a Crystal Oscillator Circuit, a Digital Controlled Reference Frequency Divider, a Phase Detector, a Charge Pump, 18-bit Shift Register, 18-bit Latch, Binary 7-bit Swallow Counter, Binary 11-bit Programmable Counter, and control circuit for the prescaler.

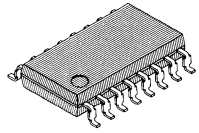
- Power Supply Voltage: 2.7 to 5.5V
- Wide Operation Temperature Range: −40 to +85°C
- Inverter for oscillator
- 18-bit Programmable Divider with Input Buffer Amplifier
  Binary 7-bit Swallow Counter plus Binary 11-bit Programmable Counter
- 11-bit Programmable Reference Divider with control circuit
- 8 divided factors for reference frequency selected by external input S_1 thru S_3
  8, 16, 64, 128, 256, 512, 1024, 2048
- Divided factor for Programmable Dividers is input as serial data bit
- 2 types of Phase Detector Output
  Built-in Charge Pump Output
  Output for External Charge Pump
- Easy to make up PLL system with Dual Modulous Prescaler ICs MB 50X
- 16-pin Standard Dual-in-line Package (DIP) and 16-pin Flat Package.
- Pulse Swallow Function

$f_{VCO} = [(N \times M) + A] \times f_r$

f_{VCO} : VCO (Voltage Controlled Oscillator) Output Frequency
N : Preset Divided Factor of Binary 11-bit Programmable Counter (16 through 2047) : N should be greater than A.
M : Preset Modulus Factor of external two modulus prescaler (64 in 64/65 mode, 128 in 128/129 mode)
A : Preset Divided Factor of Binary Swallow Counter (0 through 127)
f_r : Output Frequency of Reference Frequency Divider



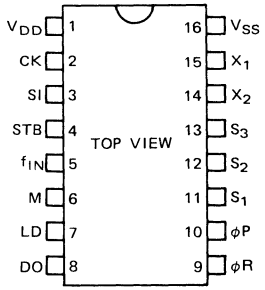
PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

2

PIN ASSIGNMENT



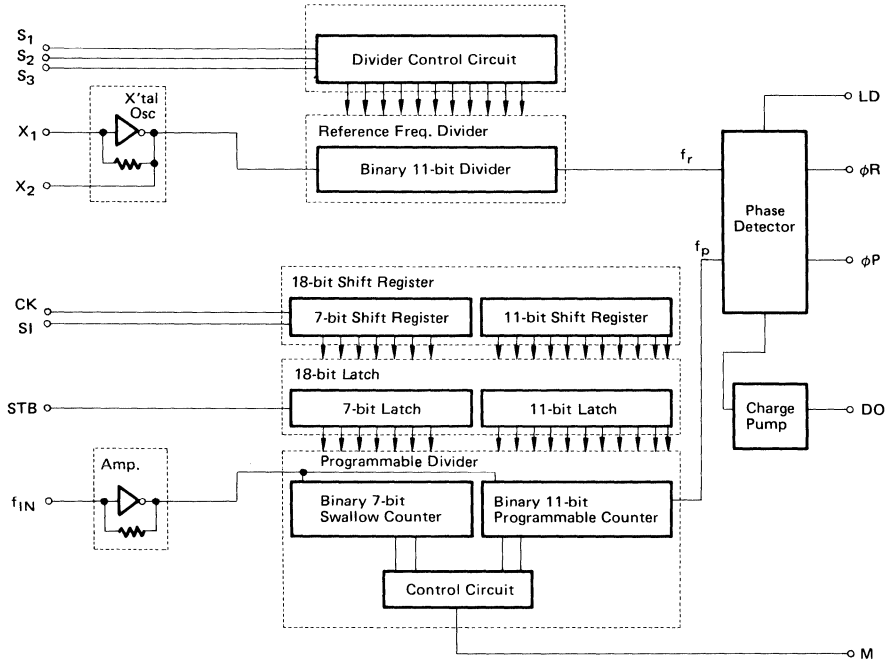
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	GND−0.5 to GND+7.0	V
Input Voltage	V_I	GND−0.5 to V_{DD}+0.5	V
Output Voltage	V_O	GND−0.5 to V_{DD}+0.5	V
Output Current	I_O	±10	mA
Open-drain Output	V_{OOP}	GND−0.5 to V_{DD}+3.0	V
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{STG}	−65 to +150	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB87073 BLOCK DIAGRAM



PIN NAME TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	–	V_{DD}	9	O	φR
2	I	CK	10	O	φP
3	I	SI	11	I	S_1
4	I	STB	12	I	S_2
5	I	f_{in}	13	I	S_3
6	O	M	14	O	X_2
7	O	LD	15	I	X_1
8	O	DO	16	–	V_{SS}

PIN DESCRIPTION

Pin No.	Symbol	Function
1	V_{DD}	Power Supply Voltage
2	CK	Clock signal input for 18-bit Shift Register. Serial input is valid at the rising edge of CK.
3	SI	Serial Data Input for 18-bit Shift Register. See SERIAL DATA INPUT FOR PROGRAMMABLE DIVIDER.
4	STB	Strobe signal input for transfer the data of 18-bit Shift Register to 18-bit Latch. The operation is executed when STB is at High level.
5	f_{IN}	Input for Binary 7-bit Swallow Counter and Binary 11-bit Programmable Counter. This input involves bias circuit and amplifier. The connection with Dual Modulus Prescaler should be AC connection.
6	M	Control output for Dual Modulus Prescaler. The connection with the prescaler should be DC connection. Pulse Swallow Function: MB 501: M = High : Preset Module Factor 64 or 128 M = Low : Preset Module Factor 65 or 129
7	LD	Output of Phase Comparator; It is at High level when f_r and f_p are coherent, and then the loop is locked. Otherwise it outputs pulse signal.
8	DO	Three-state Charge Pump Output; The mode of DO is changed by the combination of Reference Freq. Divider output frequency f_r and Programmable Divider output frequency f_p as listed below: $f_r > f_p$: Drive Mode (DO = High) $f_r = f_p$: High-Impedance Mode $f_r < f_p$: Sink Mode (DO = Low)
9 10	ϕR ϕP	Outputs for external charge pump. Note that ϕP is an N-ch open-drain output. ϕR ϕP $f_r > f_p$: Low : Low $f_r = f_p$: Low : High-Impedance $f_r < f_p$: High : High-Impedance
11 12 13	S_1 S_2 S_3	Control Inputs for Reference Frequency Divider. The combination of these inputs provides divided factor to Reference Frequency Divider. Divided Factor 8 16 64 128 256 512 1024 2048 S_1 0 1 0 1 0 1 0 1 S_2 0 0 1 1 0 0 1 1 S_3 0 0 0 0 1 1 1 1
14	X_2	Pin for Crystal Oscillator; Output pin of the inverting amplifier. This pin should be open when an external oscillator is used.
15	X_1	Pin for Crystal Oscillator; Input pin of the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupling when an external oscillator is used, but for large amplitude signals (standard CMOS levels), DC coupling may also be used.
16	V_{SS}	Ground

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage (V_{SS} = 0V)	V_{DD}	2.7 to 5.5	V
Input Voltage	V_I	GND to V_{DD}	V
Operating Ambient Temperature	T_A	−40 to +85	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V, T_A = −40 to +85°C)

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	All inputs except f_{IN} and X_1	V_{IH}	3.5	–	–	V
Low-level Input Voltage	All inputs except f_{IN} and X_1	V_{IL}	–	–	1.5	V
Input Sensitivity of f_{IN}	Sine wave AC coupling	V_{fpp}	1.0	–	–	Vp-p
Input Sensitivity of X_1	Sine wave AC coupling	V_{sin}	1.5	–	–	Vp-p
High-level Input Current	All inputs except f_{IN} and X_1 $V_I = V_{DD}$	I_{IH}	–	1.0	–	μA
Low-level Input Current	All inputs except f_{IN} and X_1 V_I = GND	I_{IL}	–	-1.0	–	μA
Input Current of f_{IN}	V_I = GND to V_{DD}	I_{fIN}	–	±50	–	μA
Input Current of X_1	V_I = GND to V_{DD}	I_{X1}	–	±50	–	μA
High-level Output Voltage	All outputs except ϕP and X_2 I_{OH} = 0μA	V_{OH}	4.95	–	–	V
Low-level Output Voltage	All outputs except ϕP and X_2 I_{OL} = 0μA	V_{OL}	–	–	0.05	V
Low-level Output Voltage of ϕP	I_{OL} = 2mA	V_{OLP}	–	–	1.0	V
High-level Output Voltage of X_2	I_{OH} = 0μA	V_{OHX}	4.50	–	–	V
Low-level Output Voltage of X_2	I_{OL} = 0μA	V_{OLX}	–	–	0.50	V
High-level Output Current	All outputs except ϕP and X_2 V_{OH} = 4.0V	I_{OH}	-1.0	–	–	mA
Low-level Output Current	All outputs except ϕP and X_2 V_{OL} = 0.8V	I_{OL}	1.0	–	–	mA
N-ch. Open Drain Cut-off Current	ϕP only $V_O = V_{DD}$ + 3.0V	I_{OFF}	–	1.0	–	μA
Power Supply Current	See Note *	I_{DD}	–	3.0	–	mA
Maximum Operation Frequency	Divider Unit: Ref. Freq. Divider	f_{maxd}	15	25		MHz
Maximum Operation Frequency	Prog. Counter 7/11 bit Counter	f_{maxp}	13	25		MHz

Note *: f_{IN} = 5.0 MHz using 12.8 MHz X'tal. All inputs except f_{IN} are connected with GND. All outputs are open.

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.0V, T_A = −40 to +85°C)

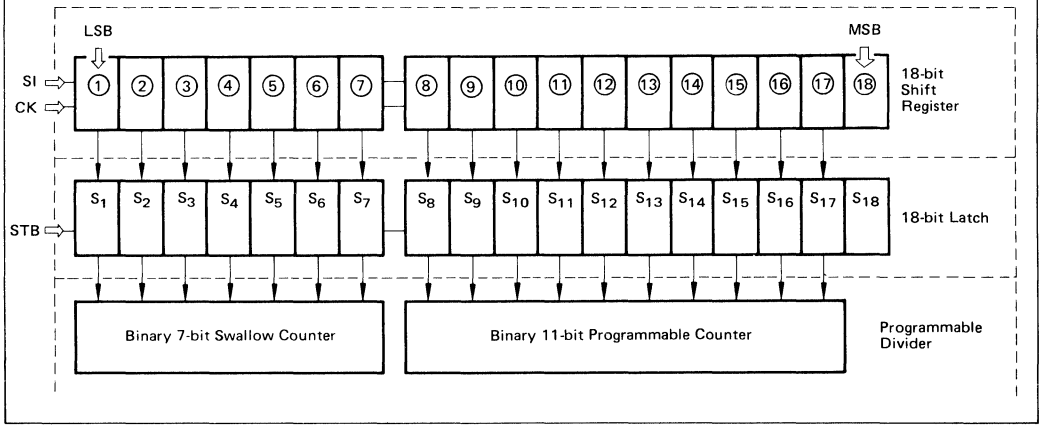
Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	All inputs except f_{IN} and X_1	V_{IH}	2.1	–	–	V
Low-level Input Voltage	All inputs except f_{IN} and X_1	V_{IL}	–	–	0.9	V
Input Sensitivity of f_{IN}	Sine wave AC coupling	V_{fpp}	0.8	–	–	Vp-p
Input Sensitivity of X_1	Sine wave AC coupling	V_{sin}	1.0	–	–	Vp-p
High-level Input Current	All inputs except f_{IN} and X_1 $V_I = V_{DD}$	I_{IH}	–	1.0	–	μA
Low-level Input Current	All inputs except f_{IN} and X_1 V_I = GND	I_{IL}	–	-1.0	–	μA
Input Current of f_{IN}	V_I = GND to V_{DD}	I_{fIN}	–	±30	–	μA
Input Current of X_1	V_I = GND to V_{DD}	I_{X1}	–	±30	–	μA
High-level Output Voltage	All outputs except ϕP and X_2 I_{OH} = 0μA	V_{OH}	2.95	–	–	V
Low-level Output Voltage	All outputs except ϕP and X_2 I_{OL} = 0μA	V_{OL}	–	–	0.05	V
Low-level Output Voltage of ϕP	I_{OL} = 0.8mA	V_{OLP}	–	–	0.8	V
High-level Output Voltage of X_2	I_{OH} = 0μA	V_{OHX}	2.5	–	–	V
Low-level Output Voltage of X_2	I_{OL} = 0μA	V_{OLX}	–	–	0.50	V
High-level Output Current	All outputs except ϕP and X_2 V_{OH} = 2.0V	I_{OH}	-0.5	–	–	mA
Low-level Output Current	All outputs except ϕP and X_2 V_{OL} = 0.8V	I_{OL}	0.5	–	–	mA
N-ch. Open Drain Cut-off Current	ϕP only $V_O = V_{DD}$ + 3.0V	I_{OFF}	–	1.0	–	μA
Power Supply Current	See Note *	I_{DD}	–	2.0	–	mA
Maximum Operation Frequency	Divider Unit: Ref. Freq. Divider	f_{maxd}	13	20		MHz
Maximum Operation Frequency	Prog. Counter 7/11 bit Counter	f_{maxp}	10	20		MHz

Note *: f_{IN} = 5.0 MHz using 12.8 MHz X'tal. All inputs except f_{IN} are connected with GND. All outputs are open.

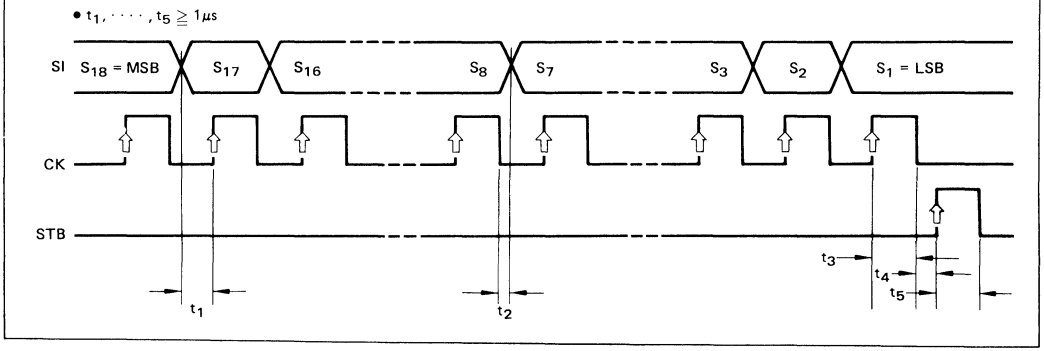
SERIAL DATA INPUT FOR PROGRAMMABLE DIVIDER

The Divided factor of the programmable divder is provided by the 18-bit latch. The data of the latch is transferred from the 18-bit shift register at the rising edge of strobe signal STB. The shift register has a serial input with clock input. A divided factor is input from MSB as illustrated in TIMING CHART.

Fig. 2 — Block Diagram of Programmable Divider



Timing Chart



Binary 7-bit Swallow Counter Data Input

Digit No. / Divided Factor	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
2	0	0	0	0	0	1	0
3	0	0	0	0	0	1	1
4	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.

Note:

- Divided Factor: 0 thru 127
- Depending the external prescaler's Divided Factor Swap, SW, the input data should be as follow:
  MB 501:
  - SW = "H": Bit 7 of the shift register should be "0."
  - SW = "L": Bit 7 is "0" or "1."

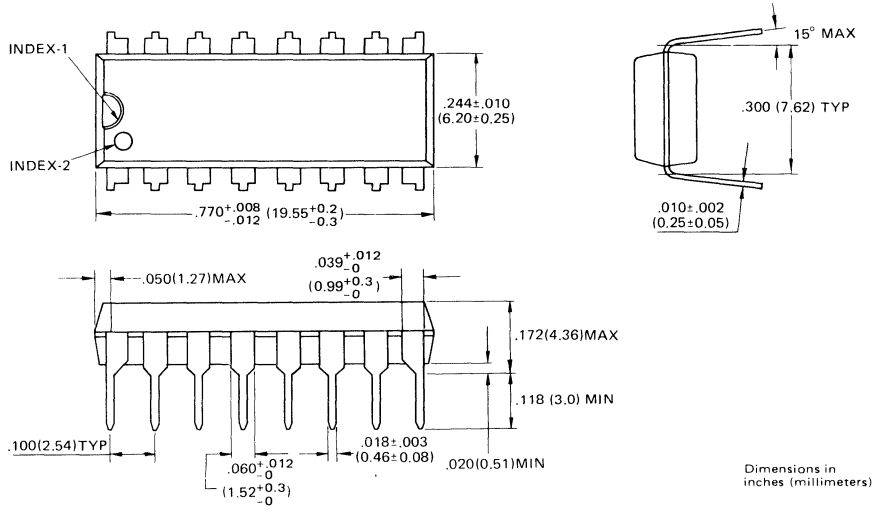
Binary 11-bit Programmable Data Input

Digit No. / Divided Factor	18	17	16	15	14	13	12	11	10	9	8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
18	0	0	0	0	0	0	1	0	0	1	0
19	0	0	0	0	0	0	1	0	0	1	1
20	0	0	0	0	0	0	1	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.

Note: Divided factor less than 16 is prohibited.
Divided factor: 16 thru 2047

PACKAGE DIMENSIONS

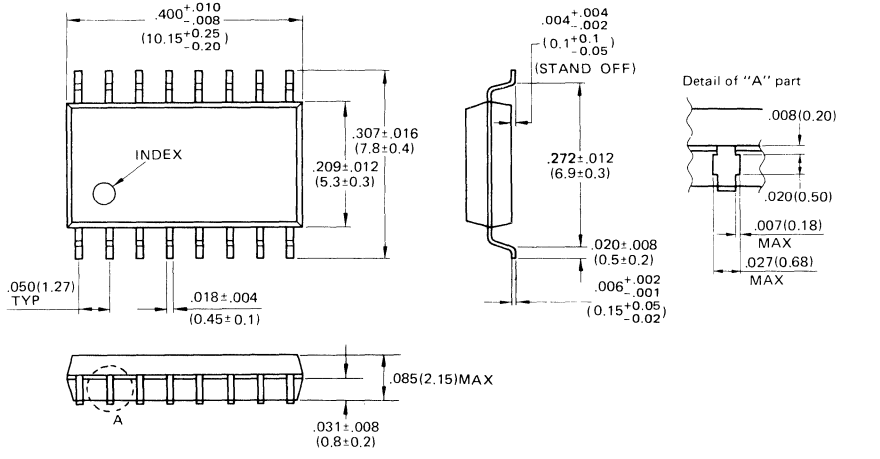
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

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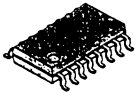
FUJITSU

TS588-A883
March 1988

INTERMITTENT OPERATING CMOS SERIAL INPUT Phase-Locked-Loop (PLL) FREQUENCY SYNTHESIZER

The Fujitsu MB87076 is a intermittent operating serial input PLL frequency synthesizer fabricated Advanced CMOS Technology.
The MB87076 contains inverter for Oscillator, 14-bit Shift Register, 18-bit Shift Register, 1-bit Control Register, 14-bit Latch, 18-bit Latch, Programmable Divider (Binary 11-bit Programmable Counter and Binary 7-bit Swallow Counter), Programmable Reference Divider (Binary 14-bit Programmable Reference Counter), Phase Detector, Charge Pump, Control Generator for External Two Modulus Prescaler and Intermittent Operating Controller.
The MB87076 has a selection of either operation mode or power down mode depending on PS input signal level.
Whenever device starts operation, fr and fv are forced to phase synchronizm condition.

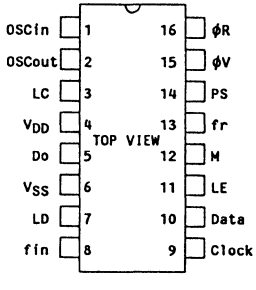
PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

- Single Power Supply Voltage
- Wide Operation Temperature Range : T_A = -40 to 85 °C
- On-chip Inverter for Oscillator
- Programmable Reference Divider with Input Amplifier
  Programmable Divider with Input Amplifier
- 2 Types of Phase Detector Output
  On-chip Charge Pump Output
  Output for External Charge Pump
- 16-pin Standard Dual-in-line Package (Suffix:-P)
  16-pin Standard Flat Package (Suffix:-PF)
- Pulse Swallow Function
  $f_{VCO} = \{ (N \times M) + A \} \times fOSC \div R$
  f_{VCO} : VCO (Voltage Controlled Oscillator) Output Frequency
  N : Preset Divide Factor of Binary 11-bit Programmable Counter (16 to 2047)
  M : Preset Modulus Factor of External Two Modulus Prescaler (64 in 64/65 mode, 128 in 128/129 mode)
  A : Preset Divide Factor of Binary 7-bit Swallow Counter (0 to 127)
  fOSC : Output Frequecny of an External Oscillator
  R : Preset Divide Factor of Binary 14-bit Programmable Reference Counter (8 to 16383)

PIN ASSIGNMENT



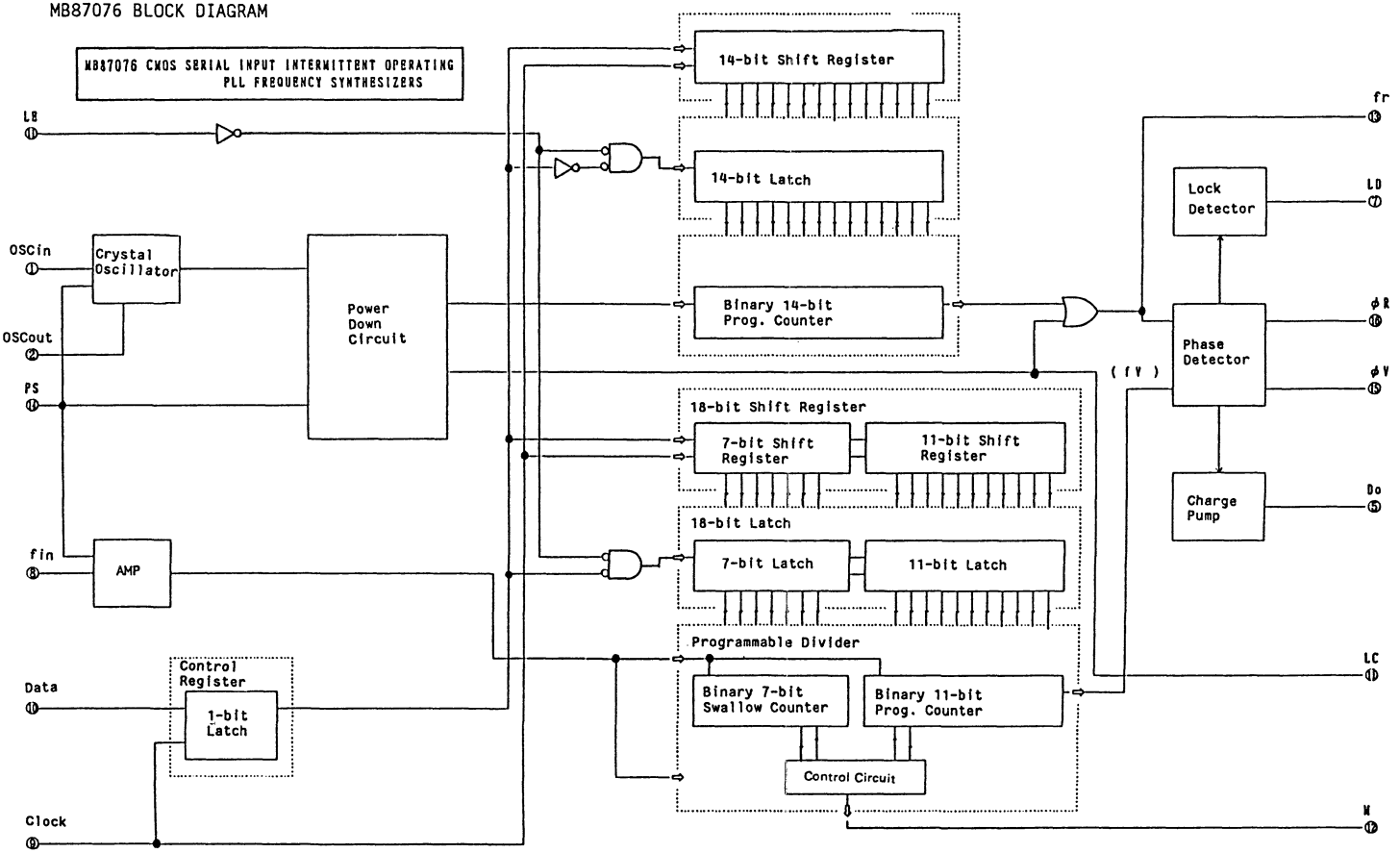
ABSOLUTE MAXIMUM RATING (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS}-0.5 to V_{SS}+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.5 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	V_{SS}-0.5 to V_{DD}+0.3	V
Output Current	I_{OUT}	± 10	mA
Open Drain Output	V_{OP}	V_{SS}-0.5 to V_{DD}+3.0	V
Operating Temperature	T_A	-40 to +85	°C
Storate Temperature	T_{STG}	-40 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB87076 BLOCK DIAGRAM



PIN NAME TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	IN	OSCin	16	OUT	ΦR
2	OUT	OSCout	15	OUT	ΦV
3	OUT	LC	14	IN	PS
4	___	V_{DD}	13	OUT	fr
5	OUT	Do	12	OUT	M
6	___	V_{SS}	11	IN	LE
7	OUT	LD	10	IN	Data
8	IN	fin	9	IN	Clock

PIN DESCRIPTION

Pin No.	Symbol	Description
1	OSCin	Pin for Crystal Oscillator; Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupling when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also used.
2	OSCout	Pin for Crystal Oscillator; Output of the inverting amplifier. This pin should be connected to ground when an external oscillator is used.
3	LC	Output pin for Loop Control Signal; It is at high level, when operation mode is selected. It is at low level, when power down mode is selected.
4	V_{DD}	Power Supply Voltage
5	Do	Three-state Charge Pump Output; The mode of Do is changed by the combination of Programmable Reference Divider output frequency fr and Programmable Divider output frequency fv as listed below: fr > fv : Drive Mode (Do = H level) fr = fv : High-Impedance Mode (Do = Z level) fr < fv : Sink Mode (Do = L level)
6	V_{SS}	Ground

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Description
7	LD	Output of Phase Comparator; It is at Low level when fr and fv are coherent, and then the loop is locked. Otherwise it outputs high level.
8	fin	Input for Binary 7-bit Swallow Counter and Binaray 10-bit Programmable Counter from VCO; This input involves bias circuit and amplifier. The connection with Dual Modulus Prescaler should be AC connection.
9	Clock	Clock signal input for 18-bit Shift Register and 14-bit Shift Register; Each rising edge of the clock makes one bit of the data shift into the shift registers.
10	Data	Serial data input for Shift Registers. This data is the divide ratio of the divider, which is provided from the corresponded shift register. The last bit of the data is the control bit which specified destination of shift register. The data is transferred to 14-bit Shift Register when the bit is at high level, and to 18-bit Shift Register when at low level.
11	LE	Load Enable Input; When this pin is at high level, the data latches from Shift Register is transferred to Programmable Reference Divider or Programmable Divider depending on the control bit data.
12	M	Control output for external Dual Modulus Prescraler. The connection should be DC connection. Pulse Swallow Function : MB501: M = High : Preset Module Factor 64 or 128 M = Low : Preset Module Factor 65 or 129
13	fr	Monitor output of the phase comparator input; as well as monitoring the output of the reference divider.
14	PS	Power down control input; When this pin is at High level, operation mode is selected. When this pin is at Low level, power down mode is selected.
15 16	ϕV ϕR	Output for external charge pump.

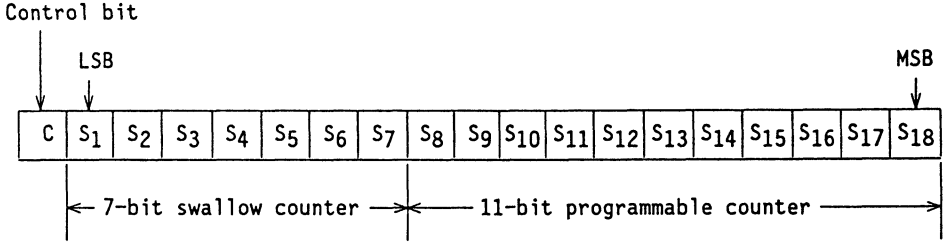
	ϕR	ϕV
fr > fv :	Low	Low
fr = fv :	Low	High-impedance
fr < fv :	High	High-impedance

FUNCTIONAL DESCRIPTIONS

Serial Data input for Programmable Divider

Binary serial data is input to Data pin. Each rising edge of clock makes one bit of the data shift into the shift registers and control register. Input data consists of 18-bit data and 1-bit of control bit data. In this case, control bit is set at low level. S_1 to S_7 selectes the divide ratio of 7-bit swallow counter and S_8 to S_{18} selects the divide ratio of 11 bit programmable counter.

The data format is shown below.



7-bit Swallow Counter Data Input

Divide factor	Digit No.						
	S_7	S_6	S_5	S_4	S_3	S_2	S_1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.

Note: Divide factor : 0 to 127

11-bit Programmable Divider Data Input

Divide factor	Digit No.										
	S_{18}	S_{17}	S_{16}	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.

Note: Divide factor less than 16 is prohibited.
Divide factor : 16 to 2047

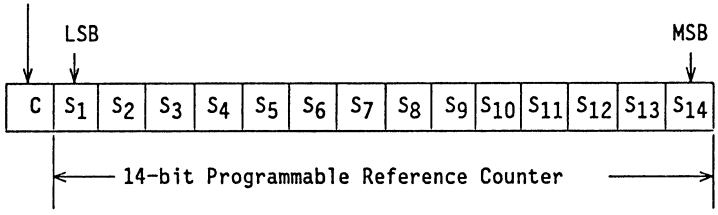
FUNCTIONAL DESCRIPTIONS (Continued)

Serial Data input for Programmable Reference Divider

Binary serial data is input to Data pin. Each rising edge of clock makes one bit of the data shift into the shift registers and control register. Input data consists of 14-bit data and 1-bit of control bit data. In this case, control bit is set at high level.

The data format is shown below.

Control bit

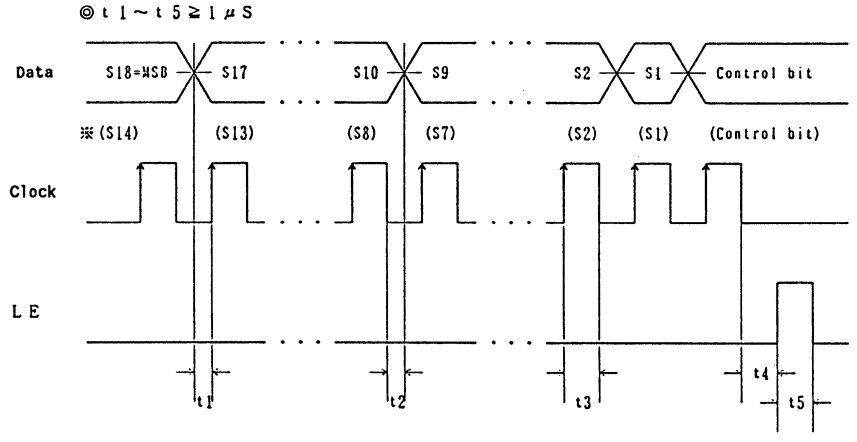


14-bit Programmable Divider Data Input

Divide factor	Digit No.													
	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8	S_7	S_6	S_5	S_4	S_3	S_2	S_1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.

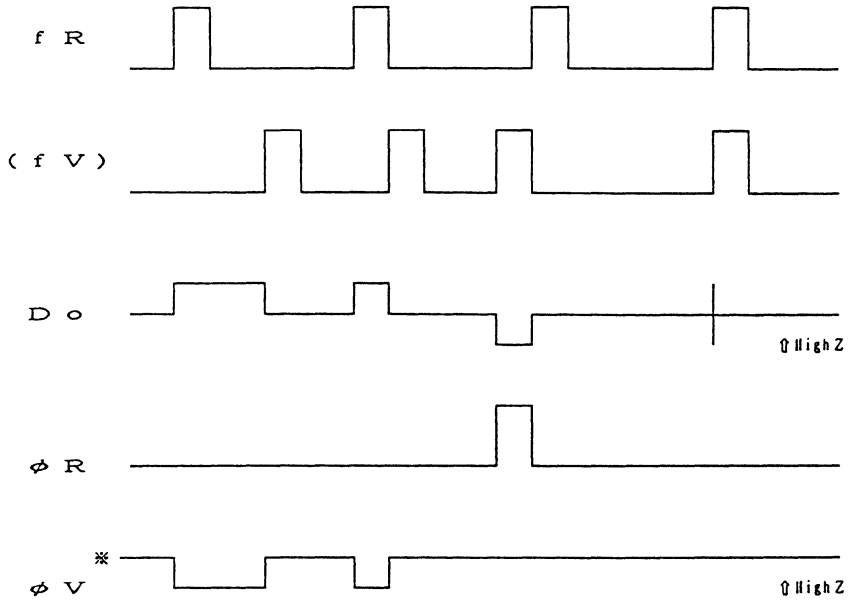
Note: Divide factor less than 8 is prohibited.
Divide factor : 8 to 16383

Fig.2 - SERIAL DATA INPUT TIMING

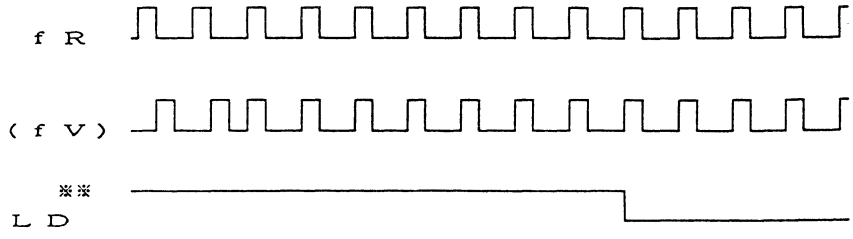


Note : * Input data of programmable reference divider

Fig.3 - PHASE DETECTOR WAVEFORM



※ φV : N-channel open drain output



※※ LD is set at High level when fr≠fv. (Unlock condition)
LD is set at Low level when fr=fv. (Lock condition)

INTERMITTENT OPERATIONAL DESCRIPTIONS

The MB87076 has Intermittent operation function which selects operation mode or power down mode depending on PS input signal level.
When PS is set at low level, power down mode is selected. During power down mode, internal dividers stop operation. Thus, very low power supply consumption is achieved and LC is set at Low level.

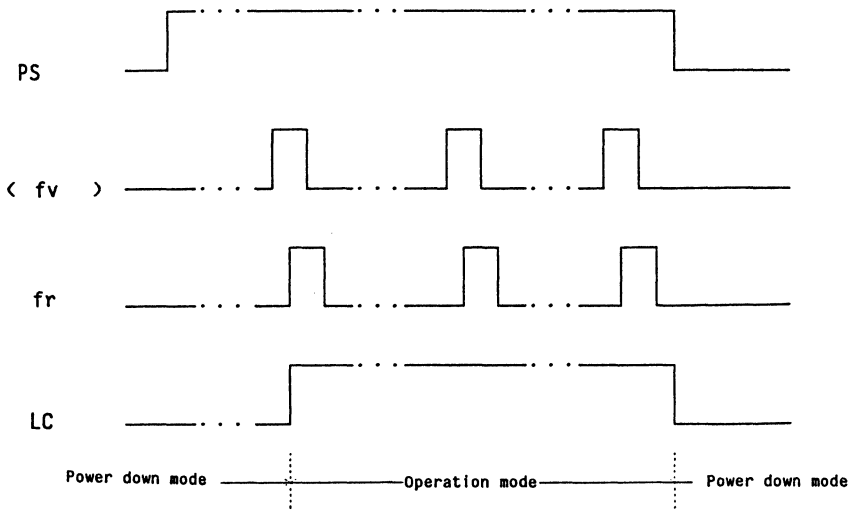
Then the PS level becomes High level with the frequency of VCO as nearly the same as that under the condition of phase lock.

When PS is set at High level, the following sequence steps are taken.

1) Programmable divider starts operation
2) fv is output with some dealy
3) Programmable reference divider starts operation when it receives fv.
4) fr is output
5) LC is forced to set at High level (Normal operation mode is selected)

As the fr outputs immediately after the fv outputs, and goes into the phase detector, the phase lock condition can be obtained just after the first clock.
When PS is set at Low level again, internal dividers stop operation.
Then internal condition turnes to be reset.

Fig.4 - INTERMITTENT OPERATION MODE



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	2.7	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	-40		+85	°C

ELECTRICAL CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 5.0 V, T_A= -40 to 85 °C)

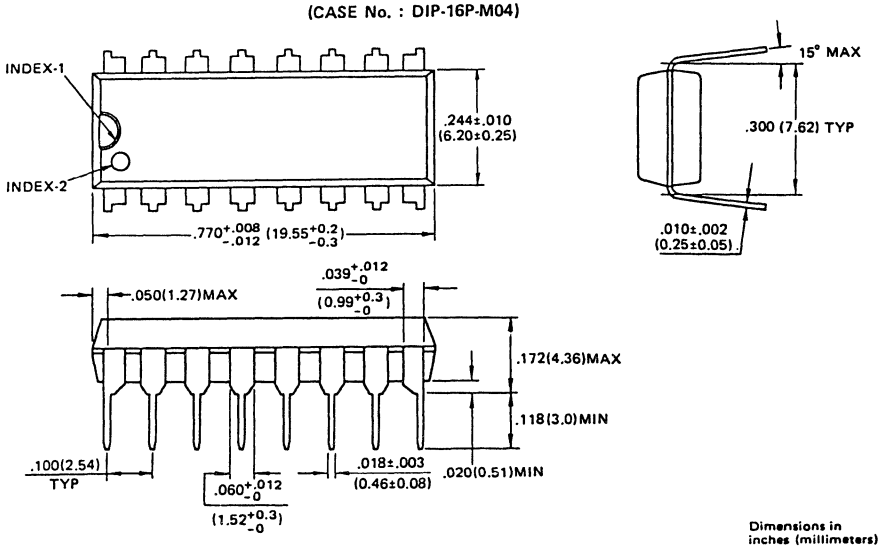
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Input Voltage except fin and OSCin	V_{IH}		3.5			V
Low-level Input Voltage except fin and OSCin	V_{IL}				1.5	V
Input Sensitivity (fin)	V_{fpp}	Amplitude in AC coupling,sine wave	0.8			V_{p-p}
Input Sensitivity (OSCin)	V_{sin}		1.0			V_{p-p}
High-level Input Current except fin and OSCin	I_{IH}	$V_{IN}=V_{DD}$			1.0	µA
Low-level Input Current except fin and OSCin	I_{IL}	$V_{IN}=V_{SS}$			-1.0	µA
Input Current (fin)	I_{fIN}	$V_{IN}=V_{SS}$ to V_{DD}		±50		µA
Input Current (OSCin)	I_{XIN}	$V_{IN}=V_{SS}$ to V_{DD}		±50		µA
High-level Output Voltage except ϕV and OSCout	V_{OH}	I_{OH}=0µA	4.95			V
Low-level Output Voltage except ϕV and OSCout	V_{OL}	I_{OL}=0µA			0.05	V
Low-level Output Voltage (ΦV)	V_{OLV}	I_{OL}=1mA			0.50	V
High-level Output Voltage (OSCout)	V_{OHX}	I_{OH}=0µA	4.50			V
Low-level Output Voltage (OSCout)	V_{OLX}	I_{OL}=0µA			0.50	V
High-level Output Current except ϕV and OSCout	I_{OH}	V_{OH}=4.0V	-1.0			mA
Low-level Output Current except ϕV and OSCout	I_{OL}	V_{OL}=0.8V	1.0			mA
N-ch open drain Cut Off Current	I_{OZ}	$V_O=V_{DD}$+3.0V		1.0		µA
* Power Supply Current	I_{DDOP}	Operation mode		3.0		mA
	I_{DDPS}	Power down mode			100	µA
Max. Operation Freq. of Programmable Reference Counter	f_{maxd}		15	25		MHz
Max. Operation Freq. of Programmable Counter	f_{maxp}		10	25		MHz

Note:

fin=8.0MHz, 11.5MHz Crystal is connected between OSCin and OSCout. PS is set at high level, the other inputs are set at low level. Output are open.

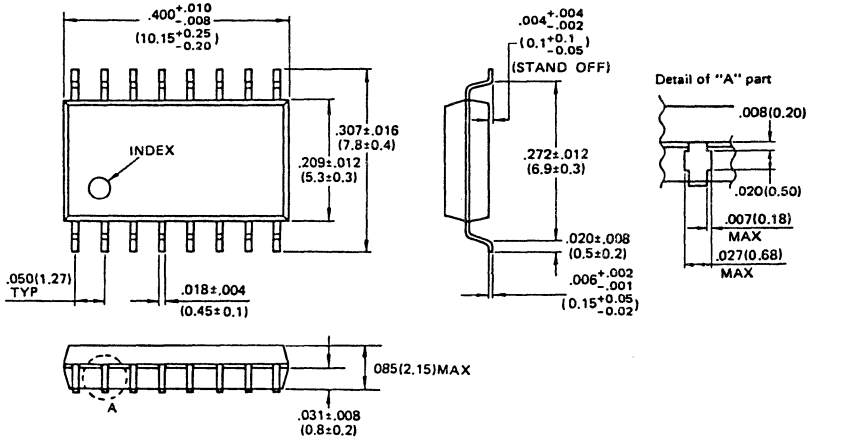
PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in
inches (millimeters)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

FUJITSU

CMOS SERIAL INPUT Phase-Locked-Loop (PLL) FREQUENCY SYNTHESIZER

TS583-A87Z
December 1987

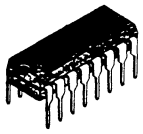
The Fujitsu MB87086 is a serial input PLL frequency synthesizer IC fabricated by Advanced CMOS Technology.

The MB87086 contains inverter for Oscillator, Binary 16-bit Programmable Reference Divider, Binary 10-bit Programmable Divider, Phase Detector, Charge pump, 16-bit Shift Register, 10-bit Shift Register, Control Register, 16-bit Latch and 10-bit Latch.
The MB87086 can make up PLL synthesizer which works up to fin of 130 MHz typ.

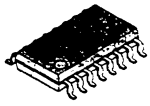
- Single Power Supply Voltage
- Wide Operation Temperature Range : -30 to 60 °C
- On-chip Inverter for Oscillator
- Serial Data Input for programmable reference divider and programmable divider is input as serial data
- 3 Types of Phase Detector Outputs
  - On-chip Charge Pump Output for Active LPF
  - On-chip Charge Pump Output for Passive LPF
  - Output for External Charge Pump
- 16-pin Standard Dual-in-line Package (Suffix:-p)
  16-pin Standard Flat Package (Suffix:-PF)
- The divide factor is selected by the following equation

$f_{VCO} = N \times (OSC \div R)$

f_{VCO} : VCO (Voltage Controlled Oscillator) output frequency
N : Preset divide factor of binary 10-bit programmable counter (5 to 1023)
OSC : Reference Frequency
R : Preset divide factor of binary 16-bit programmable reference counter (5 to 65535)

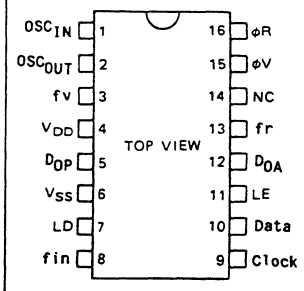


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



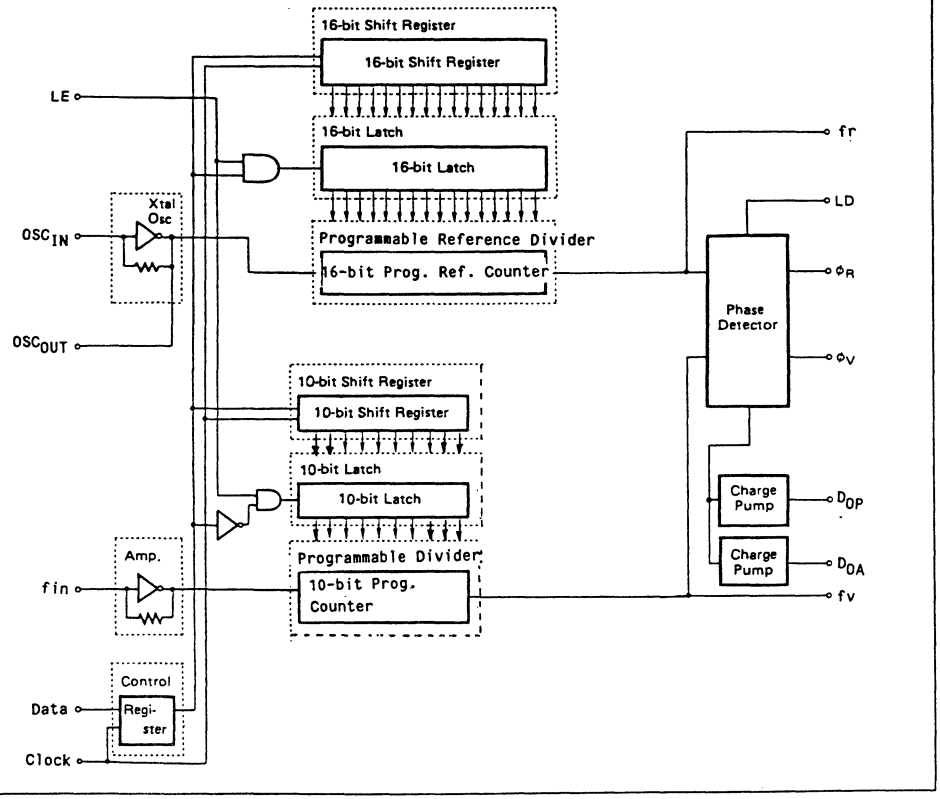
ABSOLUTE MAXIMUM RATING (See NOTE) (V_{SS}=0V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	V_{SS}-0.3 to V_{SS}+7.0	V
Input Voltage	V_{IN}	V_{SS}-0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}	V_{SS}-0.3 to V_{DD}+0.3	V
Output Current	I_{OUT}	± 10	mA
Operating Ambient Temperature	T_A	-30 to +80	°C
Storage Temperature	T_{STG}	-40 to +125	°C
Power Dissipation	P_D	300	mW

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB87086 BLOCK DIAGRAM



PIN NAME TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	I	OSC_{IN}	9	I	Clock
2	O	OSC_{OUT}	10	I	Data
3	O	fv	11	I	LE
4	–	V_{DD}	12	O	D_{OA}
5	O	D_{OP}	13	O	fr
6	–	V_{SS}	14	–	NC
7	O	LD	15	O	φV
8	I	fin	16	O	φR

PIN DESCRIPTION

Pin No.	Symbol	Description
1	OSCin	Pin for Crystal Oscillator; Input to the inverting amplifier that forms part of the oscillator. This pin receives the oscillator signal as AC coupling when an external oscillator is used, but for large amplitude signals (standard CMOS levels) DC coupling may also be used.
2	OSCout	Pin for Crystal Oscillator; Output of the inverting amplifier. This pin should be connected to open when an external oscillator is used.
3	fv	Monitor output of the phase comparator input; as well as monitoring the output of the programmable divider
4	V_{DD}	Power Supply Voltage
5	Dop	Three-state Charge Pump Output; The mode of Dop is changed by the combination of Programmable Reference Divider output frequency fr and Programmable Divider output frequency fv as listed below: fr > fv : Drive Mode (Dop = High) fr = fv : High-Impedance Mode fr < fv : Sink Mode (Dop = Low)
6	V_{SS}	Ground
7	LD	Output of Phase Comparator; It is at High level when fr and fv are coherent, and then the loop is locked. Otherwise it outputs pulse signal.
8	fin	Input for Programmable Divider from VCO; This input has a feed back resistor.
9	Clock	Clock signal input for 16-bit Shift Register and 10-bit Shift Register; Each rising edge of the clock makes one bit of the data shift into the shift registers.
10	Data	Serial data input for Shift Registers. This data is the divide factor of the divider, which is provided from the corresponded shift register. The last bit of the data is the control bit which specified destination of shift register. The data is transferred to 16-bit Shift Register when the bit is at high level, and to 10-bit Shift Register when at low level by instruction of LE signal.
11	LE	Load Enable Input; When this pin is at high level, the data latches from Shift Register is transferred to Programmable Reference Divider or Programmable Divider.

PIN DESCRIPTIONS (Continued)

Pin No.	Symbol	Descriptions
12	D_{OA}	Three state Charge Pump Output; The mode of D_{OA} is changed by the combination of Programmable Reference Divider output frequency fr and Programmable Divider output frequency fv as listed below. fr > fv : Sink Mode (D_{OA} = Low) fr = fv : High-Impedance Mode fr < fv : Drive Mode (D_{OA} = High)
13	fr	Monitor output of the phase comparator input; as well as monitoring output of Programmable Reference Divider.
14	NC	Non connection.
15 16	ϕV ϕR	Outputs for external charge pump. ϕV ϕR fr > fv : High-level Low-level fr = fv : High-level High-level fr < fv : Low-level High-level

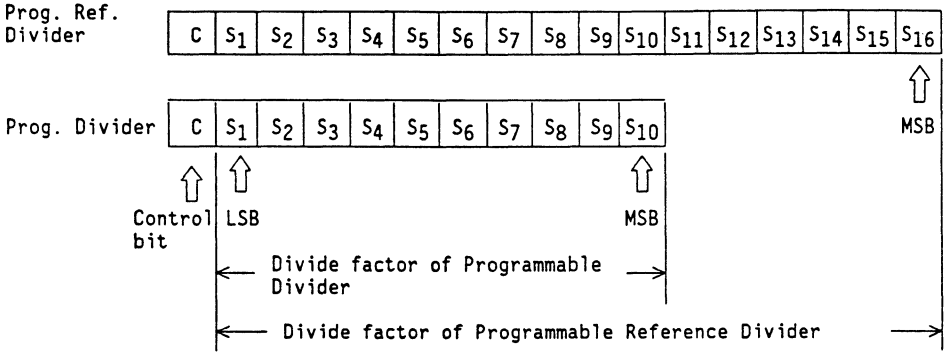
FUNCTIONAL DESCRIPTIONS

Serial Data input for Programmable Divider

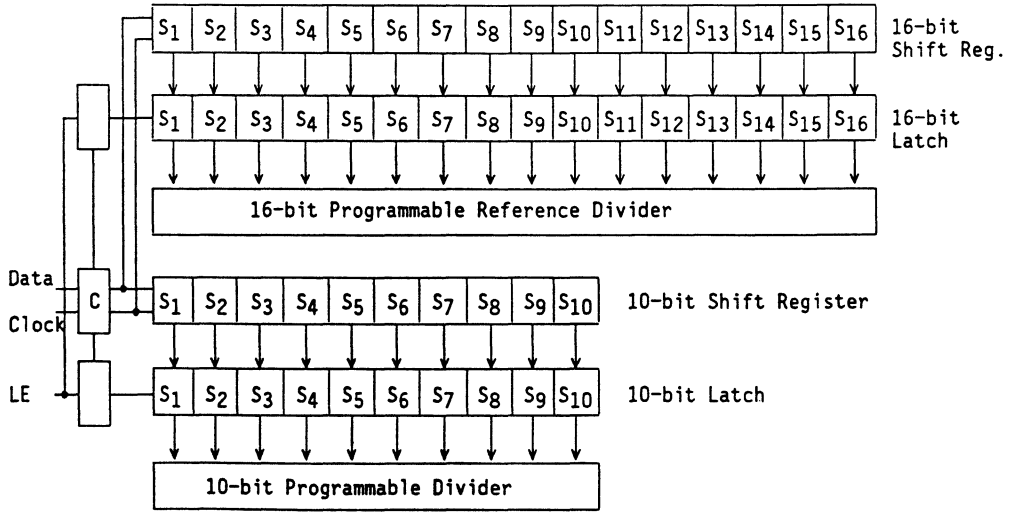
Binary serial data is input to Data pin. Each rising edge of clock makes one bit of the data shift into the shift registers and control register. Input data consists of 16-bit or 10-bit data and 1-bit of control bit data.

16-bit data selects the divide factor of Programmable Reference Divider
10-bit data selects the divide factor of Programmable Divider

The last bit of the data is stored in Control Register which specified destination of shift register.
When this bit is at high level, 16-bit Latch is selected. When this is at low level, 10-bit Latch is selected.
The data format is shown below.



When LE is at high level and Control bit is at high level, the data latches from 16-bit shift register are transferred to 16-bit Programmable Counter. When LE is at high level and Control bit is at low level, the data latches from 10-bit shift register are transferred to 10-bit Programmable Counter.



Binary 10-bit Programmable Divider Data Input

Divide factor	Digit No.									
	10	9	8	7	6	5	4	3	2	1
5	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.

Note: Divide factor less than 5 is prohibited.
Divide factor : 5 to 1023

Binary 16-bit Programmable Reference Divider Data Input

Divide factor	Digit No.															
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
5	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.

Note: Divide factor less than 5 is prohibited.
Divide factor : 5 to 65535

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V
Input Voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating Temperature	T_A	-30		+60	°C

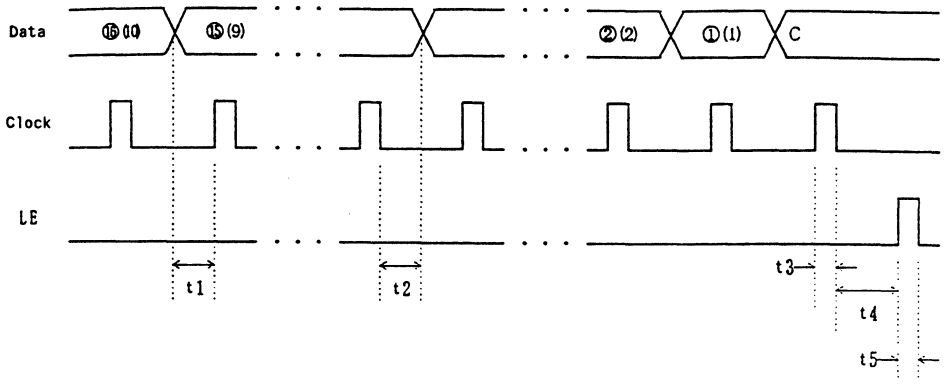
ELECTRICAL CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 5 V, T_A= -30 to 60 °C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Input Voltage except fin and OSCin	V_{IH}		3.5	-	-	V
Low-level Input Voltage except fin and OSCin	V_{IL}		-		1.5	V
Input Sensitivity (fin)	V_{fpp}	Amplitude in AC coupling,sine wave	1.0	-	-	V_{p-p}
Input Sensitivity (OSCin)	V_{sin}		0.5	-	-	V_{p-p}
High-level Input Current except fin and OSCin	I_{IH}	V_{IN}=5.0V	-	1.0	-	µA
Low-level Input Current except fin and OSCin	I_{IL}	V_{IN}=0.0V	-	-1.0	-	µA
Input Current (fin)	I_{fIN}	V_{IN}=V_{SS} to V_{DD}	-	±50	-	µA
Input Current (OSCin)	I_{XIN}	V_{IN}=V_{SS} to V_{DD}	-	±50	-	µA
High-level Output Voltage except OSCout	V_{OH}	I_{OH}=0µA	4.95	-	-	V
Low-level Output Voltage except OSCout	V_{OL}	I_{OL}=0µA	-	-	0.05	V
High-level Output Current except OSCout	I_{OH}	V_{OH}=4.6V	-1.0	-	-	mA
Low-level Output Current except OSCout	I_{OL}	V_{OL}=0.4V	1.0	-	-	mA
Power Supply Current	I_{DD}	V_{DD}=5V fin=100 MHz, 22 MHz X'tal used between OSCin and OSCout. Inputs are at GND except fin. Outputs are open.	-	8.0	-	mA
Max. Operation Freq. of Binary 16-bit Prog. Ref. Counter	f_{max}	V_{DD}=5.0V	95	130	-	MHz
Max. Operation Freq. of Binary 10-bit Prog. Counter	f_{max}	V_{DD}=5.0V	40	60	-	MHz

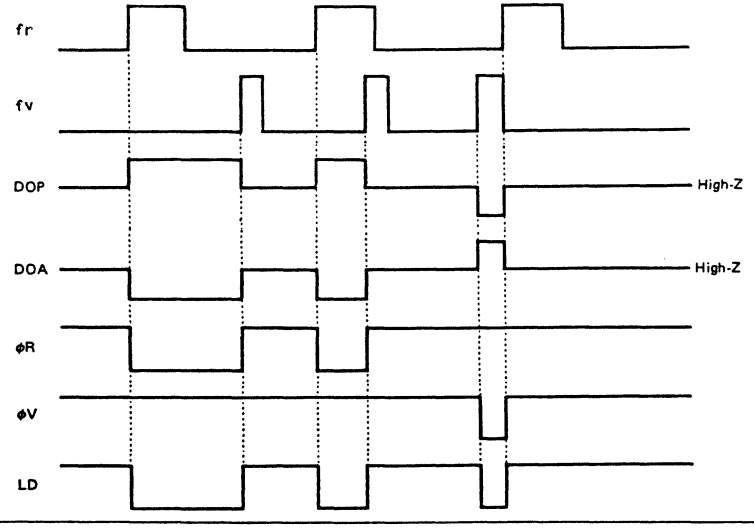
SERIAL DATA INPUT TIMING

$t_n \geq 1.0\ [\mu S]$



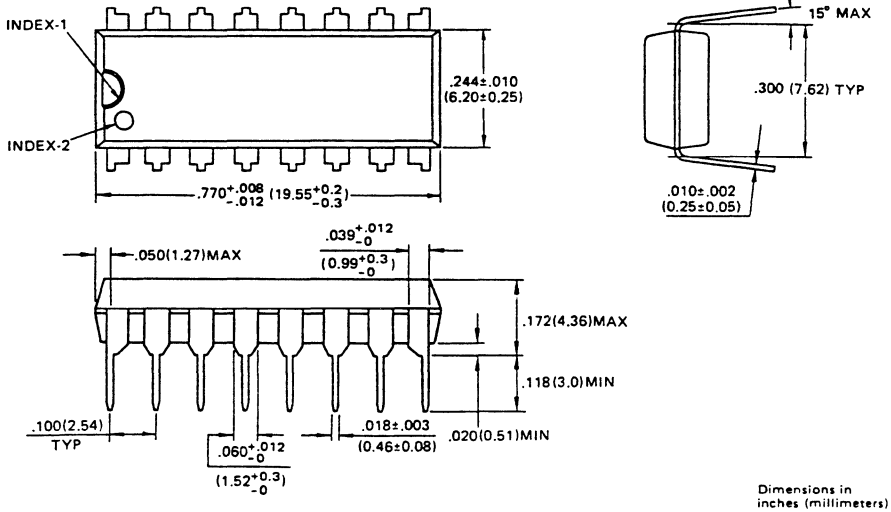
Note: Programmable Reference Divider Input (N)
Programmable Divider Input (N)

PHASE DETECTOR OUTPUT WAVEFORM



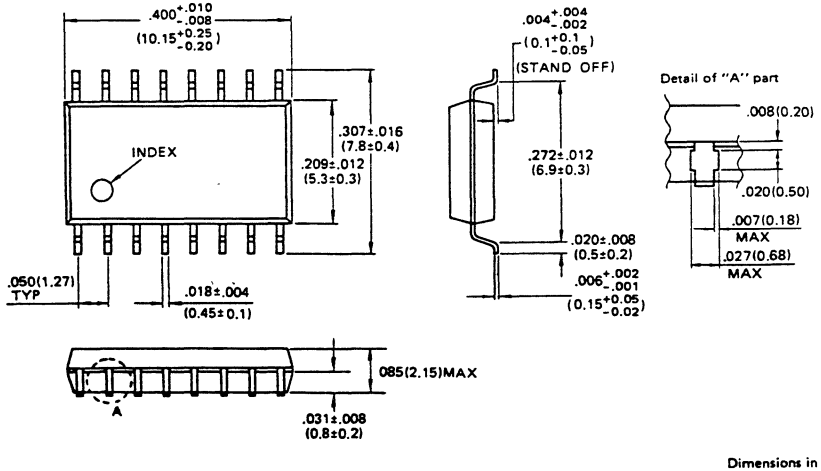
PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in inches (millimeters)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



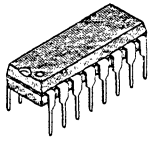
Dimensions in inches (millimeters)

Section 3

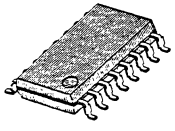
Super PLLs

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1 GHz PRESCALERS

The Fujitsu MB1501, utilizing BI-CMOS technology, is a single chip serial input PLL synthesizer which enables pulse-swallow function.
The MB1501 consists of 1.1 GHz two modulus prescaler which has the selection of either 64 divide ratio or 128, control signal generator, 16-bit shift register, 15-bit latch, 14-bit programmable referecne counter, 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, binary 7-bit swallow counter and binary 11-bit programmable counter.
It can function at low voltage, 3V typ, with low power consumption 45mW at 1.1GHz.



PLASTIC PACKAGE
DIP-16P-M04



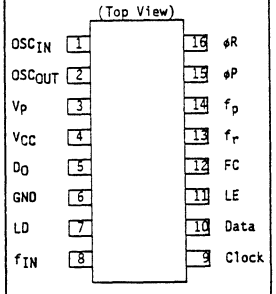
PLASTIC PACKAGE
FPT-16P-M02

- High operating frequency : f_{INMAX}=1.1 GHz (V_{INMIN}=0.20 Vp-p)
- Low power supply voltage : 2.7 V to 5.5 V (3.0 V typ)
- Low power consumption : 45 mW (3.0V , 1.1 GHz operation)
- Serial input 18-bit programmable divider
  - Binary 7-bit swallow counter
  - Binary 11-bit programmable counter
- Serial input 15-bit programmable reference divider
  - Binary 14-bit programmable reference counter
  - 1-bit switch counter (set divide ratio of prescaler)
- 2 types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature : -40°C to +85°C
- 16-pin Plastic DIP Package (Suffix:-P)
  16-pin Plastic mini-flat Package (Suffix:-PF)
- Pulse Swallow Function

$f_{VCO} = \{ (P \times N) + A \} \times f_{OSC} \div R$

- f_{VCO} : VCO (Voltage Controlled Oscillator) Output Frequency
- N : Preset Divide ratio of Binary 11-bit Programmalbe Counter (16 to 2047)
- A : Preset Divide ratio of Binary 7-bit Swallow Counter (0≤A≤127, A<N)
- f_{OSC} : Reference Oscillation Frequency
- R : Preset Divide ratio of Binary 14-bit Programmable Reference Counter (8 to 16383)
- P : Preset Divide ratio of Prescaler (64 or 128)

PIN ASSIGNMENT



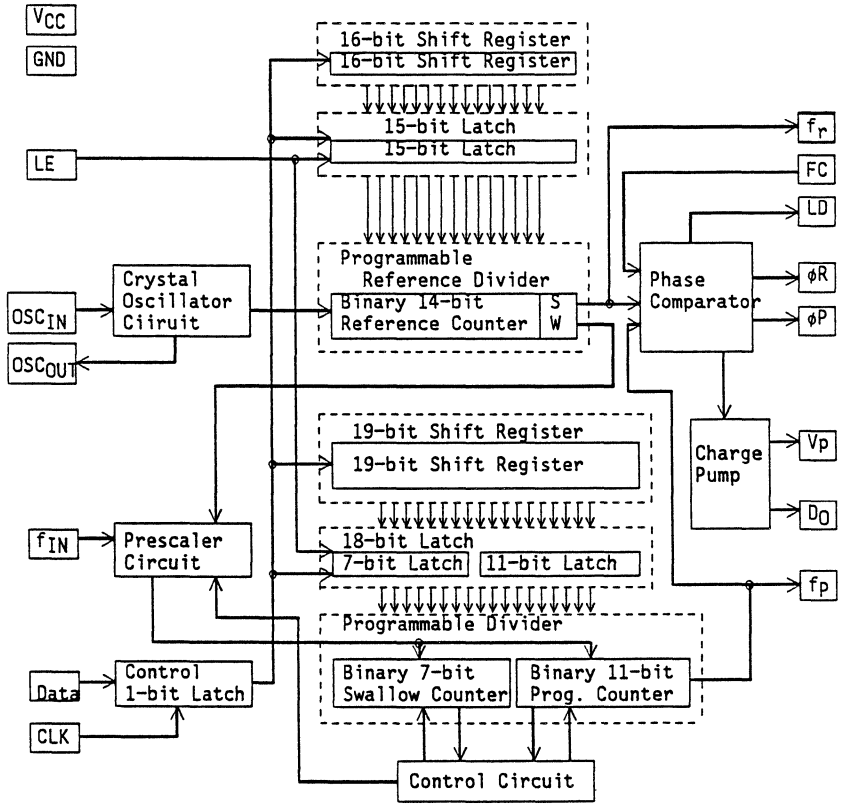
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	-0.5 to V_{CC}+0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB1501 BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin name	Descriptions
1	OSC_{IN}	Oscillator input
2	OSC_{OUT}	Oscillator output A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	Power supply for charge pump
4	V_{CC}	Power supply voltage
5	D_O	Charge pump output The characteristics are reversed depending on FC input.
6	GND	Ground
7	LD	Phase comparator output Normally, this output level is high level. While the phase of fr and fp is exists, the output becomes low level.
8	f_{IN}	Prescaler input The connection with VCO should be AC connection.
9	Clock	Clock input for 19-bit shift register and 16-bit shift register. Each rising edge of the clock shifts one bit of data into the shift registers.
10	Data	Serial data input The last bit of the data is control bit which specified destination of shift registers. When this bit is high level and LE is high level, data is transferred to 15-bit latch. When this bit is low level and LE is high level, data is transferred to 18-bit latch.
11	LE	Load enable input (with pull up resistor) When LE is high level, data stored in the shift register is transferred to latch.
12	FC	Phase select input of phase comparator (with pull resistor) When FC is low level, charge pump and phase detector characteristics becomes reverse.
13	fr	Monitor pin of phase comparator input It is equivalent to reference divider output.
14	fp	Monitor pin of phase comparator input It is equivalent to programmable divider output.
15	ϕP	Outputs for external charge pump
16	ϕR	The characteristics are reversed according to FC input.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data input consists of 3 inputs, data input (pin 10), clock input (pin 9) and load enable input (pin 11). 15-bit programmable reference divider and 18-bit programmable divider are controlled respectively.
Serial data is input to Data pin. The data is stored in the shift registers at the rising edge of clock.
When road enable is high level (or open), data stored in shift register is transferred to 15-bit latch or 18-bit latch depending on the control bit level.

Control data "H" Data is transferred into 15-bit latch.
Control data "L" Data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.

LSB MSB

CN	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW

← Divide ratio of reference counter (Binary 14-bit) →

SW : This bit selects divide ratio of Prescaler
SW = H 64
SW = L 128

R1 to R14 : Divide ratio of reference counter (8 to 16383)
CN : Control bit = H

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown below.

LSB MSB

CN	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

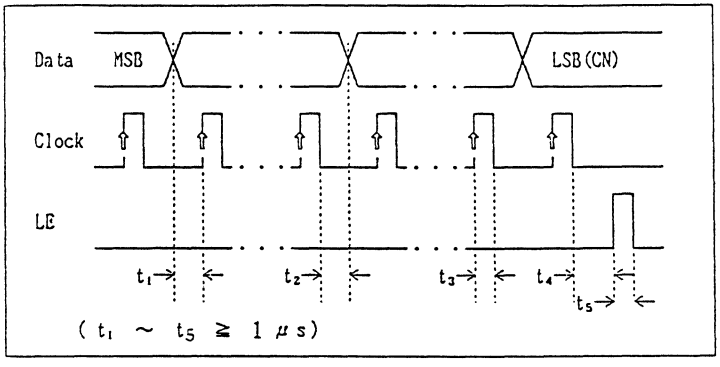
← Divide ratio of swallow counter (Binary 7-bit) →

← Divide ratio of programmable counter (Binary 11-bit) →

N1 to N11 : Divide ratio of programmable counter (16 to 2047)
A1 to A7 : Divide ratio of swallow counter (0 to 127)
CN : Control bit = L
Data is input from MSB data.

FUNCTIONAL DESCRIPTIONS (Continued)

SERIAL DATA INPUT TIMING



At the rising edge of clock one bit of data is shifted into the shift registers.

PHASE CHARACTERISTICS

FC pin (pin 12) is provided to change phase of phase comparator.
Characteristics of internal charge pump output (D_O), Phase detector outputs (ΦR, ϕP) are reversed depending on FC input data.
Outputs are shown below.

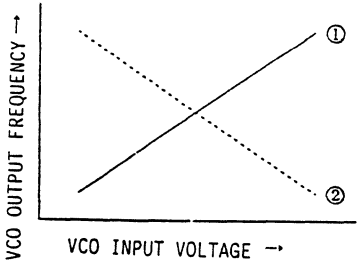
	FC = H (or open)			FC = L		
	DO	ϕR	ϕP	DO	ϕR	ϕP
fr > fp	H	L	L	L	H	Z
fr < fp	L	H	Z	H	L	L
fr = fp	Z	L	Z	Z	L	Z

Note: Z (High Impedance)

When synthesizer system is designed, FC pin is set according to VCO characteristics.

VCO characteristics is 1,
FC is set High or open.

VCO characteristics is 2,
FC is set Low.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltate	V_{CC}	2.7	3.0	5.5	V
	Vp	V_{CC}		8.0	V
Input voltage	V_{IN}	GND		V_{CC}	V
Operating Temperature	T_A	-40		+85	°C

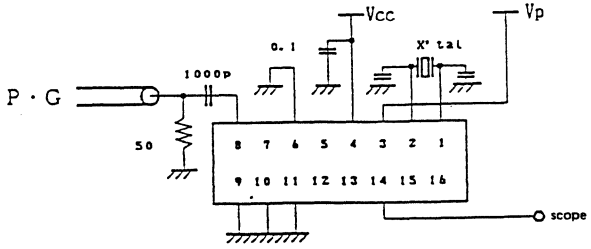
ELECTRICAL CHARACTERISTICS

(V_{CC}=2.7 to 5.5 V, T_A = -40 to +85 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply current *1	I_{CC}		15		mA
Operating frequency (f_{IN})	f_{IN}	10 *2		1100	MHz
Operating frequency (OSC_{IN})	f_{OSC}		12	20	MHz
Input sensitivity (f_{IN}) *3	V_{fIN1}	0.2		1.2	Vp-p
	V_{fIN2}	0.4		1.2	Vp-p
Input sensitivity (OSC_{IN})	V_{OSC}	0.5			Vp-p
High-level input voltage except f_{IN} and OSC_{IN}	V_{IH}	V_{CC}x0.7			V
Low-level input voltage except f_{IN} and OSC_{IN}	V_{IL}			V_{CC}x0.3	V
High-level input current (Data, CLK)	I_{IH}		1.0		µA
Low-level input current (Data, CLK)	I_{IL}		-1.0		µA
Input current (OSC_{IN})	I_{OSC}		±50		µA
Input current (LE/FC)	I_{LE}		-60		µA
High-level output voltage except OSC_{OUT}	V_{OH}	2.4			V
Low-level output voltage except OSC_{OUT}	V_{OL}			0.4	V
High-level output current	I_{OH}	-1.0			mA
Low-level output current	I_{OL}	1.0			mA

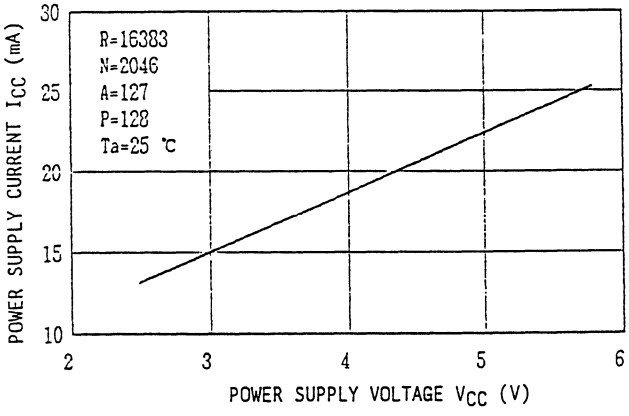
*1 f_{IN} = 1.1GHz, 12MHz X'tal used between OSC_{IN} and OSC_{OUT}, V_{CC}=3V.
Inputs are at GND excpet f_{IN} and outputs are open.
*2 Input coupling capacitance = 1000 pF
*3 V_{fIN1} : V_{CC} = 2.7 to 4.0 V
V_{fIN2} : V_{CC} = 4.0 to 5.5 V

TEST CIRCUIT

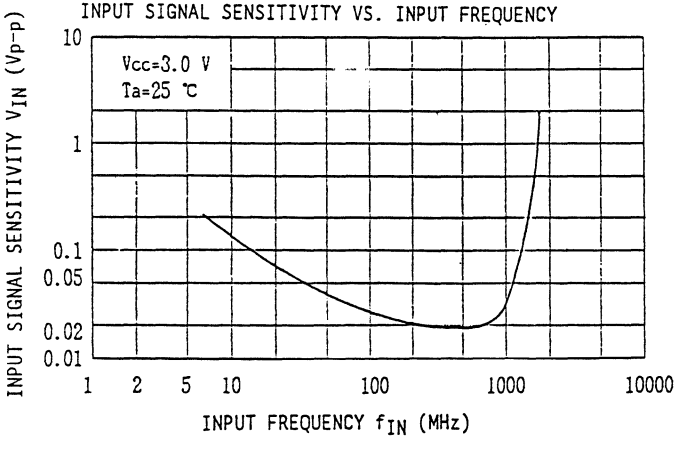


TYPICAL CHARACTERISTICS CURVES

POWER SUPPLY CURRENT VS. POWER SUPPLY VOLTAGE

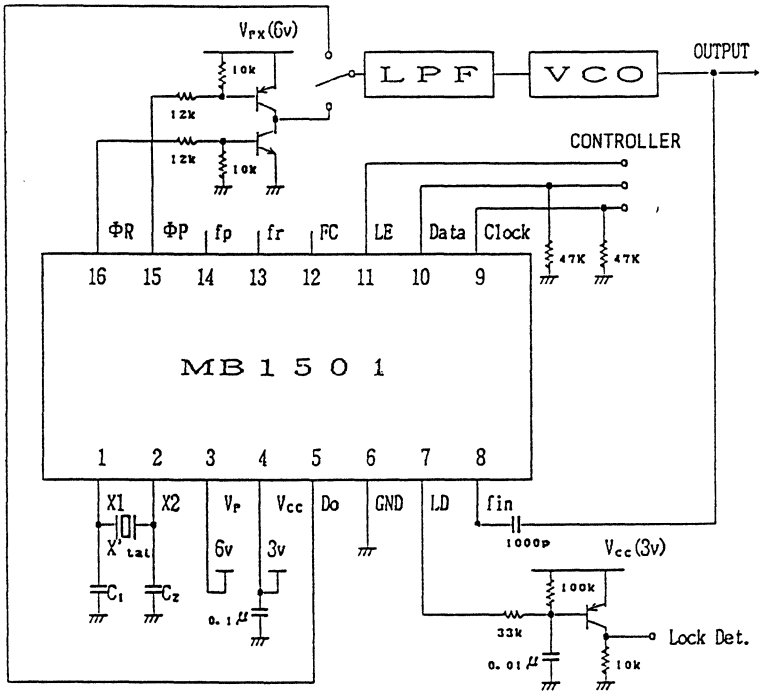


INPUT SIGNAL SENSITIVITY VS. INPUT FREQUENCY



3

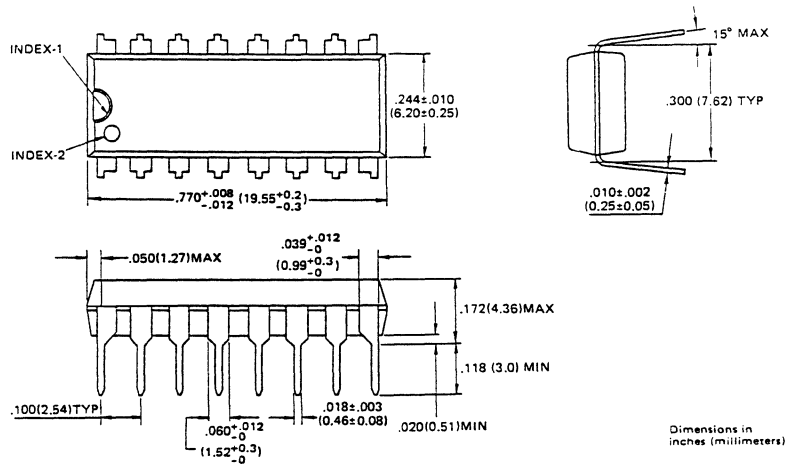
TYPICAL APPLICATION EXAMPLE



V_P, V_{PX} : 8 V max.
C_1, C_2 : Depends on crystal oscillator
LE, FC : With pull up resistor
ϕP : Open drain output

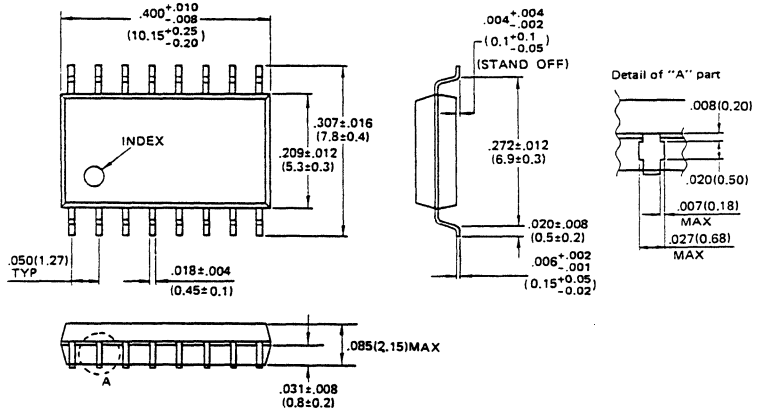
PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in inches (millimeters)

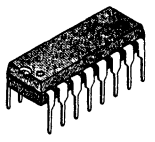
16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



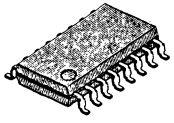
Dimensions in inches (millimeters)

SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 520MHz PRESCALERS

The Fujitsu MB1504, utilizing BI-CMOS technology, is a single chip serial input PLL synthesizer which enables pulse-swallow function.
The MB1504 consists of 520 MHz two modulus prescaler which has the selection of either 32 divide ratio or 64, control signal generator, 16-bit shift register, 15-bit latch, 14-bit programmable referecne counter, 1-bit switch counter, phase comparator with phase conversion function, charge pump, crystal oscillator, 19-bit shift register, 18-bit latch, binary 7-bit swallow counter and binary 11-bit programmable counter.
It can function at low voltage, 3V typ, with low power consumption 30mW at 520MHz.



PLASTIC PACKAGE
DIP-16P-M04



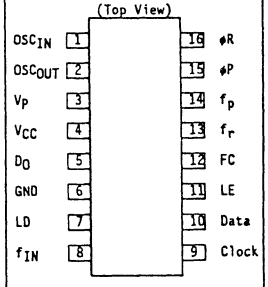
PLASTIC PACKAGE
FPT-16P-M02

- High operating frequency : f_{INMAX}=520MHz (V_{INMIN}=0.20Vp-p)
- Low power supply voltage : 2.7V to 5.5V (3.0V typ)
- Low power consumption : 30mW (3.0V, 520MHz operation)
- Serial input 18-bit programmable divider
  - Binary 7-bit swallow counter
  - Binary 11-bit programmable counter
- Serial input 15-bit programmable reference divider
  - Binary 14-bit programmable reference counter
  - 1-bit switch counter (set divide ratio of prescaler)
- 2 types of phase detector output
  - On-chip charge pump (Bipolar type)
  - Output for external charge pump
- Wide operating temperature : -40°C to +85°C
- 16-pin Plastic DIP Package (Suffix:-P)
  16-pin Plastic mini-flat Package (Suffix:-PF)
- Pulse Swallow Function

  $f_{VCO} = \{ (P \times N) + A \} \times f_{OSC} \div R$

  f_{VCO} : VCO (Voltage Controlled Oscillator) Output Frequency
  N : Preset Divide ratio of Binary 11-bit Programmalbe Counter (16 to 2047)
  A : Preset Divide ratio of Binary 7-bit Swallow Counter ($0 \leq A \leq 127$, $A < N$)
  f_{OSC} : Reference Oscillation Frequency
  R : Preset Divide ratio of Binary 14-bit Programmable Reference Counter (8 to 16383)
  P : Preset Divide ratio of Prescaler (32 or 64)

PIN ASSIGNMENT



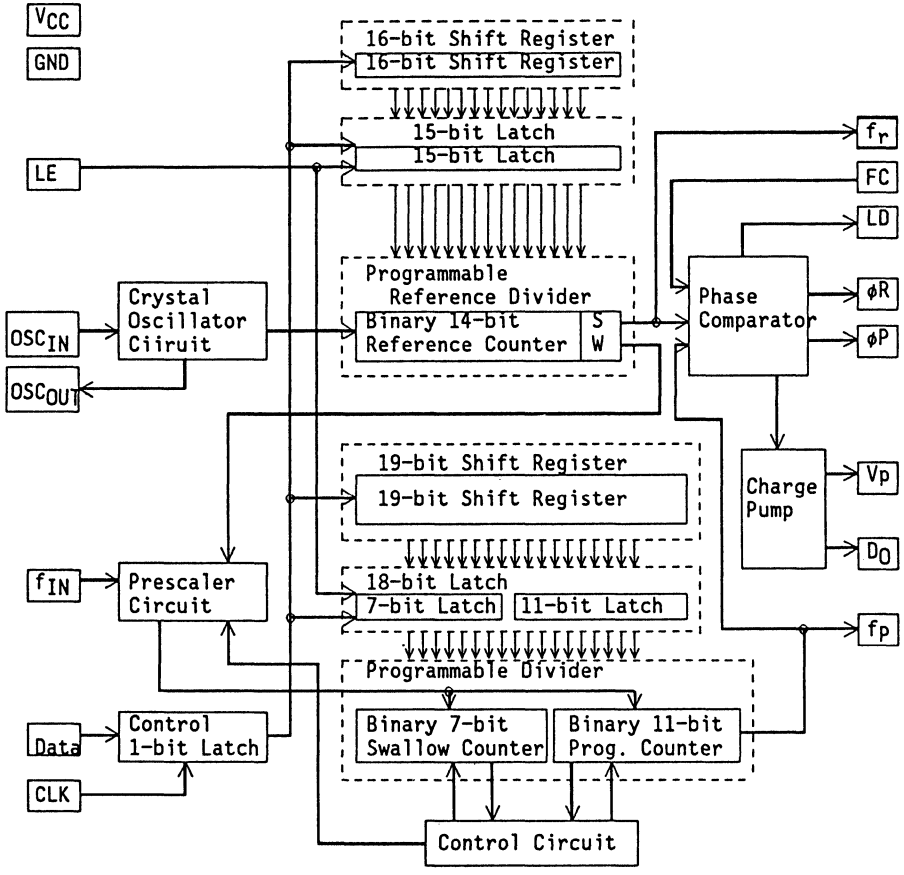
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
	V_P	V_{CC} to 10.0	V
Output Voltage	V_{OUT}	-0.5 to V_{CC}+0.5	V
Output Current	I_{OUT}	±10	mA
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 - MB1504 BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin name	Descriptions
1	OSC_{IN}	Oscillator input
2	OSC_{OUT}	Oscillator output A crystal is placed between OSC_{IN} and OSC_{OUT}.
3	V_P	Power supply for charge pump
4	V_{CC}	Power supply voltage
5	D_O	Charge pump output The characteristics are reversed depending on FC input.
6	GND	Ground
7	LD	Phase comparator output Normally, this output level is high level. While the phase of fr and fp is exists, the output becomes low level.
8	f_{IN}	Prescaler input The connection with VCO should be AC connection.
9	Clock	Clock input for 19-bit shift register and 16-bit shift register. Each rising edge of the clock shifts one bit of data into the shift registers.
10	Data	Serial data input The last bit of the data is control bit which specified destination of shift registers. When this bit is high level and LE is high level, data is transferred to 15-bit latch. When this bit is low level and LE is high level, data is transferred to 18-bit latch.
11	LE	Load enable input (with pull up resistor) When LE is high level, data stored in the shift register is transferred to latch.
12	FC	Phase select input of phase comparator (with pull resistor) When FC is low level, charge pump and phase detector characteristics becomes reverse.
13	fr	Monitor pin of phase comparator input It is equivalent to reference divider output.
14	fp	Monitor pin of phase comparator input It is equivalent to programmable divider output.
15	ϕP	Outputs for external charge pump
16	ϕR	The characteristics are reversed according to FC input.

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

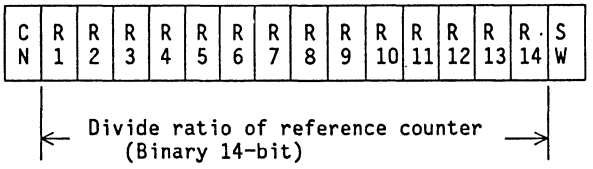
Serial data input consists of 3 inputs, data input (pin 10), clock input (pin 9) and load enable input (pin 11). 15-bit programmable reference divider and 18-bit programmable divider are controlled respectively.
Serial data is input to Data pin. The data is stored in the shift registers at the rising edge of clock.
When road enable is high level (or open), data stored in shift register is transferred to 15-bit latch or 18-bit latch depending on the control bit level.

Control data "H" Data is transferred into 15-bit latch.
Control data "L" Data is transferred into 18-bit latch.

PROGRAMMABLE REFERENCE DIVIDER

Reference divider consists of 16-bit shift register, 15-bit latch and 14-bit reference counter. Serial 16-bit data format is shown below.

LSB MSB



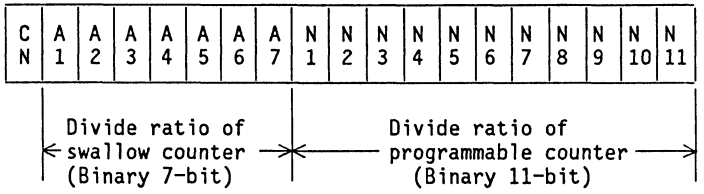
SW : This bit selects divide ratio of Prescaler.
SW = H 32
SW = L 64

R1 to R14 : Divide ratio of reference counter (8 to 16383)
CN : Control bit = H

PROGRAMMABLE DIVIDER

Programmable divider consists of 19-bit shift register, 18-bit latch, 7-bit swallow counter and 11-bit programmable counter. Serial 19-bit data format is shown below.

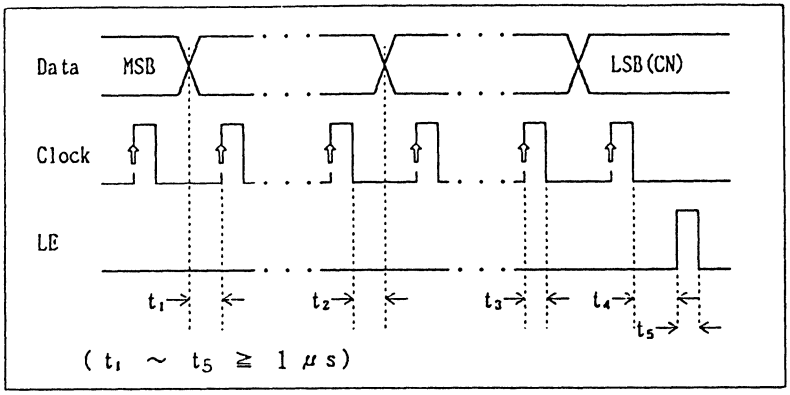
LSB MSB



N1 to N11 : Divide ratio of programmable counter (16 to 2047)
A1 to A7 : Divide ratio of swallow counter (0 to 127)
CN : Control bit = L
Data is input from MSB data.

FUNCTIONAL DESCRIPTIONS (Continued)

SERIAL DATA INPUT TIMING



At the rising edge of clock one bit of data is shifted into the shift registers.

PHASE CHARACTERISTICS

FC pin (pin 12) is provided to change phase of phase comparator.
Characteristics of internal charge pump output (D_O), Phase detector outputs (ΦR, ϕP) are reversed depending on FC input data.
Outputs are shown below.

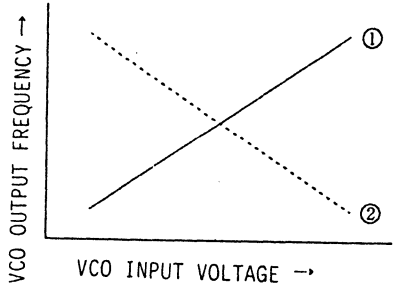
	FC = H (or open)			FC = L		
	DO	ϕR	ϕP	DO	ϕR	ϕP
fr > fp	H	L	L	L	H	Z
fr < fp	L	H	Z	H	L	L
fr = fp	Z	L	Z	Z	L	Z

Note: Z (High Impedance)

When designing the synthesizer system, FC pin is set according to VCO characteristics.

VCO characteristics is 1,
FC is set High or open.

VCO characteristics is 2,
FC is set Low.



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltate	V_{CC}	2.7	3.0	5.5	V
	V_P	V_{CC}		8.0	V
Input voltage	V_{IN}	GND		V_{CC}	V
Operating Temperature	T_A	-40		+85	°C

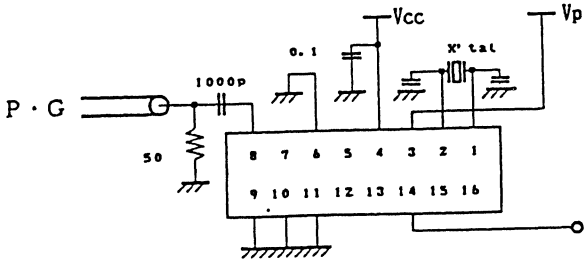
ELECTRICAL CHARACTERISTICS

(V_{CC}=2.7 to 5.5 V, T_A = -40 to +85 °C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply current *1	I_{CC}		10		mA
Operating frequency (f_{IN})	f_{IN}	10 *2		520	MHz
Operating frequency (OSC_{IN})	f_{OSC}		12	20	MHz
Input sensitivity (f_{IN}) *3	V_{fIN1}	0.2		1.2	Vp-p
	V_{fIN2}	0.4		1.2	Vp-p
Input sensitivity (OSC_{IN})	V_{OSC}	0.5			Vp-p
High-level input voltage except f_{IN} and OSC_{IN}	V_{IH}	V_{CC}x0.7			V
Low-level input voltage except f_{IN} and OSC_{IN}	V_{IL}			V_{CC}x0.3	V
High-level input current (Data, CLK)	I_{IH}		1.0		µA
Low-level input current (Data, CLK)	I_{IL}		-1.0		µA
Input current (OSC_{IN})	I_{OSC}		±50		µA
Input current (LE/FC)	I_{LE}		-60		µA
High-level output voltage except OSC_{OUT}	V_{OH}	2.4			V
Low-level output voltage except OSC_{OUT}	V_{OL}			0.4	V
High-level output current	I_{OH}	-1.0			mA
Low-level output current	I_{OL}	1.0			mA

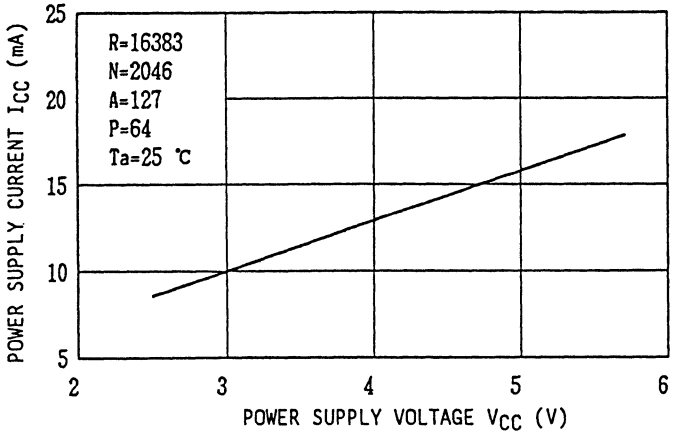
*1 f_{IN} = 520MHz, 12MHz X'tal used between OSC_{IN} and OSC_{OUT}, V_{CC}=3V.
Inputs are at GND excpet f_{IN} and outputs are open.
*2 Input coupling capacitance = 1000 pF
*3 V_{fIN1} : V_{CC} = 2.7 to 4.0 V
V_{fIN2} : V_{CC} = 4.0 to 5.5 V

TEST CIRCUIT

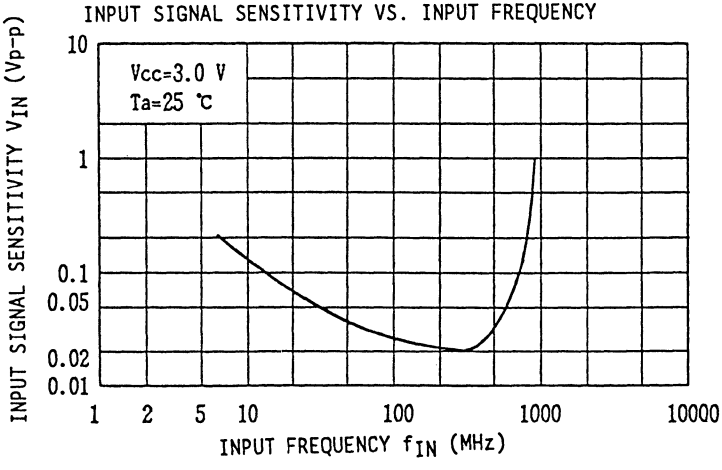


TYPICAL CHARACTERISTICS CURVES

POWER SUPPLY CURRENT VS. POWER SUPPLY VOLTAGE

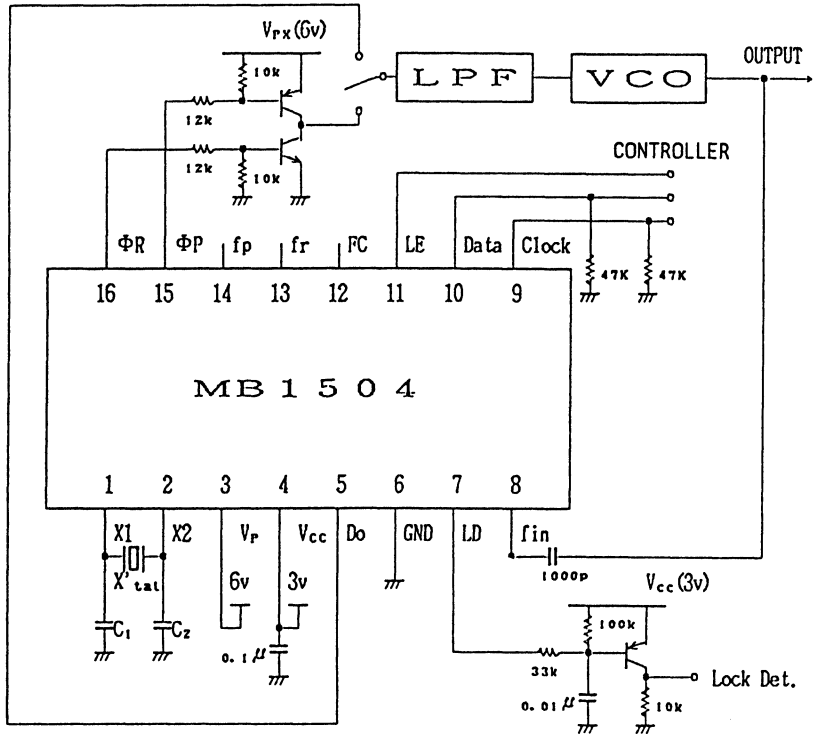


INPUT SIGNAL SENSITIVITY VS. INPUT FREQUENCY



3

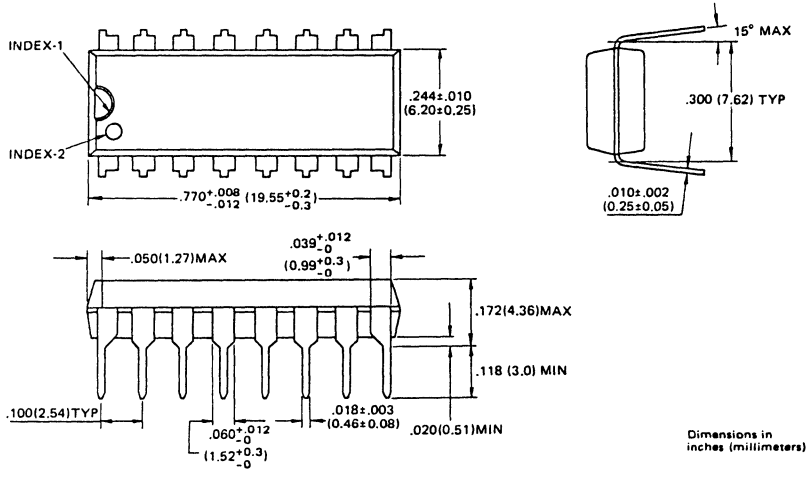
TYPICAL APPLICATION EXAMPLE



V_P, V_{PX} : 8 V max.
C_1, C_2 : Depends on crystal oscillator
LE, FC : With pull up resistor
ϕP : Open drain output

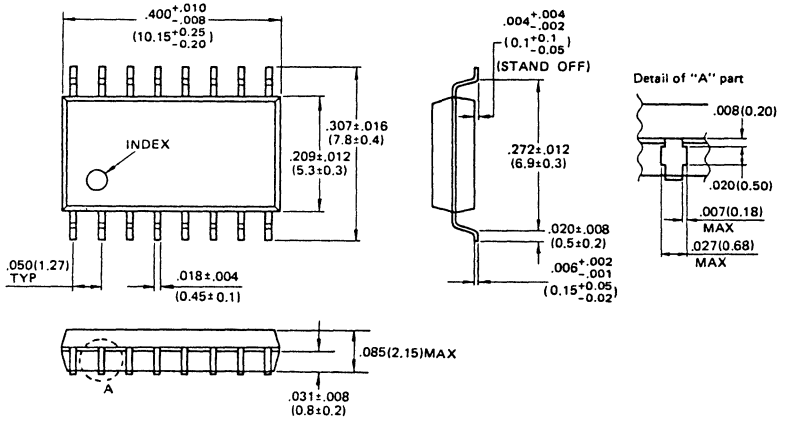
PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in inches (millimeters)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in inches (millimeters)

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