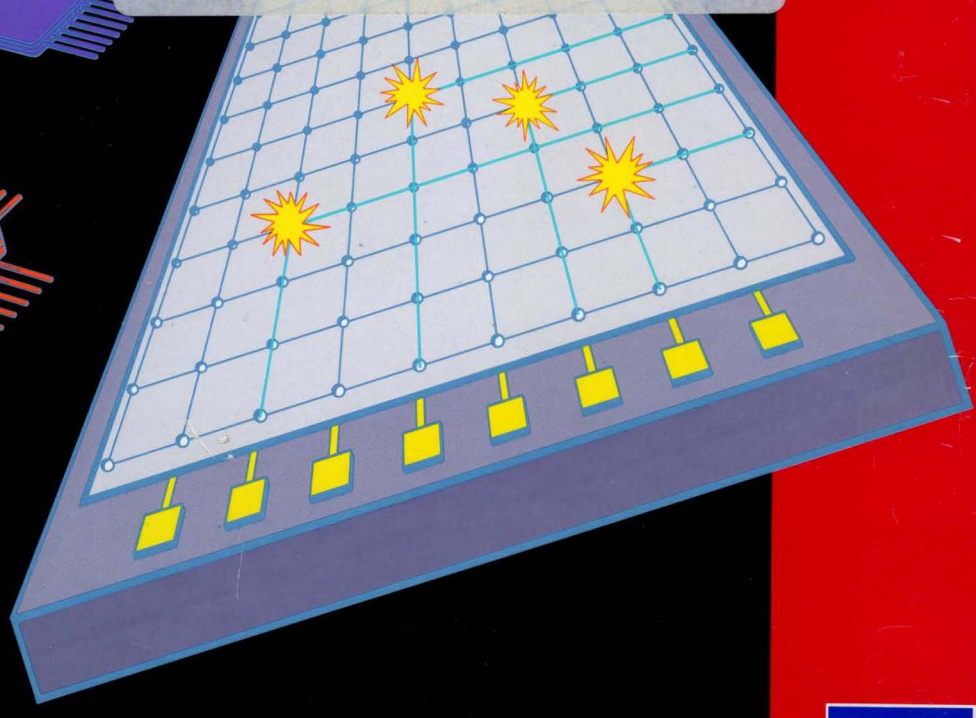
Bipolar Memory Products

1989
Data
Book



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Bipolar Memory Products

1989 Data Book

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Overview

Fujitsu's Bipolar Memory Products

Introduction

Fujitsu manufactures a wide range of integrated circuits that includes linear products, microprocessors, telecommunications circuits, ASICs, high-speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and both static and dynamic memories.

The Bipolar memory product line offers devices for use in a wide range of applications. These memories are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

ECL RAMs

FMI currently offers fast ECL I/O RAMs ranging in density from 1K to 256K. The pure ECL RAMs are available in the following organizations: 512 x 4 to 16K x 4 and 4K x 1 to 64K x 1. Fujitsu has the fastest pure ECL RAMs available, with speeds as fast as 3 ns, 5 ns, and 7 ns for other 4K, 16K, and 64K densities respectively.

BiCMOS RAMs

Fujitsu offers BiCMOS ECL I/O RAMs in both 64K and 256K densities. The 64K devices are pin compatible with the pure ECL devices and are also offered in 16K x 4 and 64K x 1 organizations. The 256K BiCMOS ECL I/O RAMs have both the x1 and x4 organizations and have a T_{aa} of 15 ns maximum.

Programmable ROMs

Fujitsu's complete line of low-power EPROMs are compatible with the industry standards. The EPROM product line offers BiCMOS technology and high-density, high-reliablility parts.

Section 1

ECL RAMs

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1-39	MBM100422A-5 MBM100422A-7	5 7	1024 bits (256w x 4b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
1-47	MBM10470A-7	7	4096 bits (4096w x 1b)	18-pin Ceramic DIP 18-pin Ceramic FPT 18-pad Ceramic LCC
1-57	MBM10470A-10 MBM10470A-15 MBM10470A-20	10 15 20	4096 bits (4096w x 1b)	18-pin Ceramic DIP 18-pin Ceramic FPT 18-pad Ceramic LCC
1-67	MBM100470A-7	7	4096 bits (4096w x 1b)	18-pin Ceramic DIP 18-pin Ceramic FPT 18-pad Ceramic LCC
1-77	MBM100470A-10 MBM100470A-15	10 15	4096 bits (4096w x 1b)	18-pin Ceramic DIP 18-pin Ceramic FPT 18-pad Ceramic LCC
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1-93	MBM100474A-3	3	4096 bits (1024w x 4b)	24-pin Ceramic DIP 24-pin Ceramic FPT
1-101	MBM10474A-5 MBM10474A-7	5 7	4096 bits (1024w x 4b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
1-111	MBM10474A-10 MBM10474A-15	10 15	4096 bits (1024w x 4b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
1-121	MBM100474A-5 MBM100474A-7	5 7	4096 bits (1024w x 4b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
1-131	MBM100474A-10 MBM100474A-15	10 15	4096 bits (1024w x 4b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
1-141	MBM10480-15 MBM10480-25	15 25	16384 bits (16384w x 1b)	20-pin Ceramic DIP 20-pin Ceramic FPT 20-pad Ceramic LCC
1-153	MBM10480A-8	8	16384 bits (16384w x 1b)	20-pin Ceramic DIP 20-pin Ceramic FPT 20-pad Ceramic LCC
1-163	MBM10480A-10	10	16384 bits (16384w x 1b)	20-pin Ceramic DIP 20-pin Ceramic FP 20-pad Ceramic LCC

ECL RAMs
(Continued)

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
1-173	MBM100480-15 MBM100480-25	15 25	16384 bits (16384w x 1b)	20-pin Ceramic DIP 20-pin Ceramic FPT 20-pad Ceramic LCC
1-185	MBM100480A-8	8	16384 bits (16384w x 1b)	20-pin Ceramic DIP 20-pin Ceramic FPT 20-pad Ceramic LCC
1-195	MBM100480A-10	10	16384 bits (16384w x 1b)	20-pin Ceramic DIP 20-pin Ceramic FPT 20-pad Ceramic LCC
1-205	MBM10484-15	15	16384 bits (4096w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT
1-213	MBM10A484-5	5	16384 bits (4096w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT
1-219	MBM10484A-8	8	16384 bits (4096w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT 28-pad Ceramic LCC
1-229	MBM10484A-10	10	16384 bits (4096w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT 28-pad Ceramic LCC
1-241	MBM100484-15	15	16384 bits (4096w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT
1-249	MBM100484A-8	8	16384 bits (4096w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT 28-pad Ceramic LCC
1-259	MBM100484A-10	10	16384 bits (4096w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT 28-pad Ceramic LCC
1-271	MBM100A484-5	5	16384 bits (4096w x 4b)	28-pin Ceramic FPT 28-pin Ceramic DIP
1-277	MBM10490-15 MBM10490-25	15 25	65536 bits (65536w x 1b)	22-pin Ceramic DIP 22-pin Ceramic FPT
1-285	MBM100490-15 MBM100490-25	15 25	65536 bits (65536w x 1b)	22-pin Ceramic DIP 22-pin Ceramic FPT
1-293	MBM10494-7	7	65536 bits (16384w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT
1-299	MBM93419	45	576 bits (64w x 9b)	28-pin Ceramic DIP

Introduction to Emitter-Coupled Logic

Emitter Coupled Logic (ECL) refers to a type of circuit in which the signal is coupled from the emitter of the transistor(s) of one stage, to the base(s) of the next stage. This interconnection pattern differs from normal bipolar practice in that the collectors of the transistors are used to couple the signal from one stage to the next. The ECL arrangement is necessary because, unlike normal bipolar circuitry, ECL transistors are, ideally, never saturated, or turned fully on. In actual practice, however, there may be instances where saturation does occur.

The benefit of ECL circuit non-saturated operation is speed.The ECL transistor can turn on and off much faster than a transistor operating in a saturated mode. All other things being equal, ECL memories are five to ten times as fast as the nearest competitor, CMOS. This gap is narrowing, however, as some of the faster CMOS memories have reached the 35- to 25-ns range. This is beginning to encroach on ECL territory, which ranges at present from 25 ns for some of the slower ECL devices to 3 ns for the fastest, state-of-the-art integrated circuits.

10K Versus 100K—What is the Difference

ECL logic and memories come in the following two basic family groups: 10K and 100K. These can usually be differentiated by the use of the numbers 10 or 100 in the part number (e.g., MBM10480 and MBM100480). In most cases, the 10K part and the 100K part are the same die with the 100K modification being a mask option.

Because ECL transistors usually are not saturated, the voltage level of the transistor is a function of more than just the drive level of the base. When a transistor is driven into saturation, enough drive is applied to the base of the transistor to turn it fully on. At this point, the collector and emitter of the transistor are at the supply voltage level or Vcc. In a non-saturated transistor, the collector is at Vcc, but the emitter is at some voltage below that level.

For example, imagine the transistor as a valve in a water pipe. The base drive is represented by the force on the valve handle. When the handle is turned fully clockwise, the water pressure on one side of the closed valve is high and the pressure on the other side of the valve is zero. As the valve handle is turned counter-clockwise, the water pressure on the controlled side of the valve starts to increase. When the valve is turned fully counter-clockwise, the water flow is essentially unrestricted, therefore, the pressure measures the same on one side of the valve as it does on the other.

A transistor works in a similar manner. As the base drive (or force on the valve handle) increases, the voltage across the collector-emitter (the water flow) also increases until the point is reached where the resistance to current flow cannot be reduced further. At this point, the transistor is said to be saturated (fully on). In the saturated state, the stability of the current being conducted by the transistor is largely unaffected by such factors as temperature and power supply regulation.

In ECL design, however, the opposite is true. Because the transistor is never saturated, the emitter voltage is a function of the base drive. The relationship between the base drive and the output level of the transistor is dependent upon both power supply and temperature. This means that for a given drive voltage, the output of the transistor can vary over a voltage and temperature range. In 10K ECL parts, voltage is specified over temperature. The specified temperatures are usually given as 0 degrees C, 25 degrees C, and 75 degrees C.100K ECL parts temperature is not specified over voltage because ECL integrated circuits have built-in voltage/temperature compensation.

The major difference between the 10K and the 100K products is that the 100K parts have temperature compensation components on board the integrated circuit as well as voltage regulation. This makes the 100K ECL much more stable over extremes of temperature and voltage.

ECL Soft Error

Generally, aside from the non-saturated transistor's susceptibility to voltage and temperature variations, there are no inherent disadvantages to ECL circuitry. However, as ECL devices have become larger and more dense, a problem has come to light that was not previously associated with ECL.

This problem, called soft error, is caused by the memory cell's state being altered by the intrusion of an alpha particle. Unfortunately this phenomenon, caused by increasingly smaller cell geometries, is aggravated by the non-saturated mode of the cell's transistors. To overcome this problem, many ECL manufacturers are changing to a cell structure that contains one or more saturated transistors. While this may seem a contradictory move, it must be remembered that only one of two transistors per cell are affected. The actual cell pair itself is not saturated. Any speed lost due to the saturation of the added transistor pull-ups will be regained by further reductions in actual cell size due to design improvements. The important consideration is the reduction, or in some cases, the virtual elimination of soft errors.

PNP Load Cell Design: A Design Strategy to Eliminate Soft Errors

With access times in the five nanosecond range, present Emitter Coupled Logic (ECL) Static Random Access Memories (RAMs) are the fastest computer memories available. Their circuitry is designed primarily for speed.

ECL Memory in Computers

ECL memories are usually used in large processing systems where the lightning fast speeds of individual integrated circuits (ICs) make up for the complex circuitry that these machines contain. The complexity of mainframe computers make it desirable for designers to save power and board space by using very dense memories. A single large memory chip can do the same job as many smaller ones, at a fraction of the power dissipation and with only one package. Therefore, the desire to squeeze as much ECL memory as possible into one single package is the driving force in ECL memory design today.

In order to meet the market requirements for larger ECL RAM ICs, it has become necessary to reduce the physical size of the on-chip components to levels thought impossible a few years ago. As the size of the individual memory cells shrinks to smaller dimensions, a problem formerly associated with the much slower MOS designs has started to plague ECLs. This problem is alpha-induced soft error.

Hard and Soft Errors

In IC memories, an error can either be hard or soft. A hard error is one which is device-related, that is, an error caused by a fault in the chip itself. Hard errors are usually repeatable and are generally corrected by replacement of the faulty IC. A soft error is caused by an outside source, usually random, which cannot be repeated easily in a test. Sources of soft errors in memories are usually either disturbances on the power lines, sometimes called glitches, or alpha particles. Power glitches can be controlled by power supply design or by adding special filters to the computer's AC line. However, alpha particle-induced soft errors cannot be so easily eliminated.

The Alpha Particle

Alpha particles continuously bombard the earth from outer space. Our atmosphere filters most of the alpha particles out, but a few still manage to make it to the earth's surface. These particles have very little mass and, under most circumstances, have little or no effect on human technical endeavor. However, in the case of modern high-density IC technology, alpha particles can create real problems.

In ECL memories, the cell is usually made up of two transistors, which in older technologies were large enough that an alpha particle passing through didn't cause any problems. But as the cells have gotten smaller, so have the transistors that comprise the cell. Therefore, an alpha particle passing through one of the new, small cells has more than enough energy to cause change. A one becomes a zero and a zero becomes a one, thereby creating inaccuracies.

An alpha particle penetrating a standard ECL memory cell creates a temporary conductive path along its trajectory through the cell. This conductive path bleeds away the charge that is keeping the on transistor in that state. When the on transistor starts to turn off, the memory cell flips and produces an error, resulting in bad data.

To illustrate the point, imagine that your company's payroll service has a large mainframe that uses ECL memories to handle payrolls. One soft error could change someone's paycheck by a factor of ten! To avoid this, most computers using ECL memory in sensitive locations use a hardware fix called error correction. Error correction works, but it is at best a treatment for the symptom rather than a cure for the disease. Error correction works by using a redundant bit of data that can take the place of any data that has been lost or altered by a soft failure. While this technique can be successfully applied to ECL system design, it is often not desirable to do so because the resultant increase in complexity and decrease in speed makes error correction impractical. By not using this approach to soft error correction, the mainframe computer designers have placed the burden of eliminating or controlling alpha-induced soft errors squarely on the shoulders of the ECL memory manufacturer.

Solving the Alpha Particle Error Problem

The problem of alpha particle soft error increases with each newer and larger ECL memory. ECL producers have tried to solve the problem in several ways. In the past, the most practical approach has been to shield the memory area of the die with some material through which alpha particles could not pass, such as polyamide. The major problem with this approach is that many of the most successful alpha shield materials are also low level alpha sources. This means that when an alpha particle is stopped by the shield material, the energy is sometimes transferred to that material on a sub-atomic level and can knock an electron loose. The accelerated electron then penetrates the die. This doesn't happen very often and generally alpha shields do a fairly good job of reducing alpha-induced soft error to acceptable levels.

The Best Solution

The best method for controlling alpha particle circuit disruption is to change the cell design. Fujitsu Microelectronics, Inc. has done just that. The PNP pull-up cell design developed by Fujitsu allows for further reduce overall cell size with an accompanying increase in the cell's transistor stability.

An ECL memory cell contains two NPN transistors connected so that when one is turned on, the other is turned off. The cell's memory state, (that is, whether it contains a logic one or a logic zero), is determined by which transistor in the cell is on and which one is off. This arrangement of transistors is called a monostable multivibrator, or a flip-flop. One of the major characteristics of flip-flop is that the state of one transistor cannot be altered without changing the state of the other transistor. So, if the on transistor is turned off, then the off transistor will automatically turn on.

How The Classic ECL Memory Cell (NPN) Works

As explained above, the traditional ECL memory cell is constructed from a pair of NPN transistors connected together as a monostable multivibrator called a Parallel Diode Cell (Figure 1-1). The two transistors in the cell are connected so that they are pulled up to the word line via a pair of resistors in parallel with a pair of Schottky diodes. This diode pull-up configuration is the classic ECL memory cell design and, until recently, was the basis of almost all ECL static RAMs.

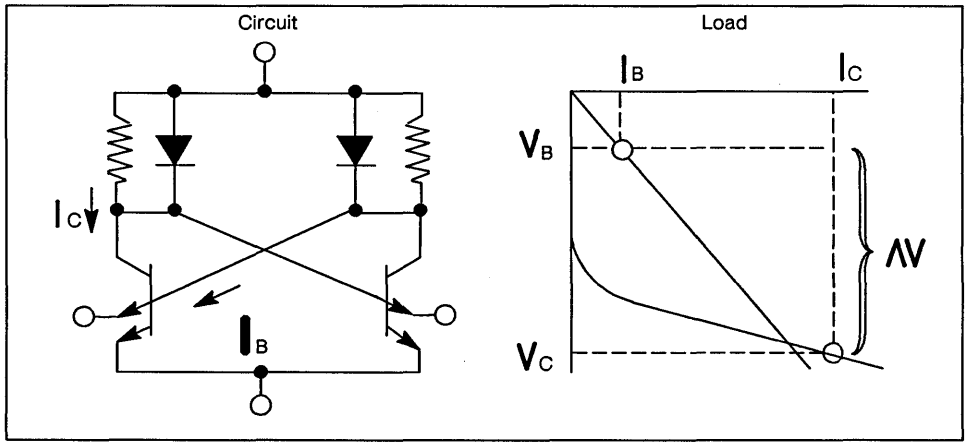

Figure 1-1. Parallel Diode Cell

This design has the advantage of being fast because the two multivibrator transistors are biased so that when they are turned on, neither are in a saturated state. Being non-saturated, they are able to turn on and off very quickly. As long as the cell is designed with relatively large geometries, this traditional architecture is problem-free. Problems do occur however, when the geometries are shrunk to make larger and larger ECL organizations.

As cell geometries get smaller, the individual cell transistors become more susceptible to soft error because the other on transistor in the cell is held high by its base capacitance charge. Since the base areas of these devices have now become much smaller than they once were, they hold a very small charge (on the order of approximately 75000 electrons). This charge is easily dispersed, and an alpha particle has enough energy to do so. The voltage drop at the load resistor in the standby mode

$$(\Delta V = iC \times RL)$$

is limited by the forward voltage applied to the Schottky diode. Therefore, there is a chance that due to alpha particle penetration, the charge on the on transistor

(Q = C x ΔV)

could become as small as the charge on the off transistor, causing the cell to flip.

How the New PNP Load Cell Works

In an effort to solve this problem and to supply very fast, virtually error-free ECL memories to its customers, Fujitsu has developed a new design that is a radical departure from the classic diode pull-up cell. This new design is called the PNP load cell because it replaces the diode-resistor pull-up with a PNP load cell (Figure 1-2). The PNP load cell places a PNP transistor between the collector of the cell transistor and the pull-up's emitter is also tied to the word line.

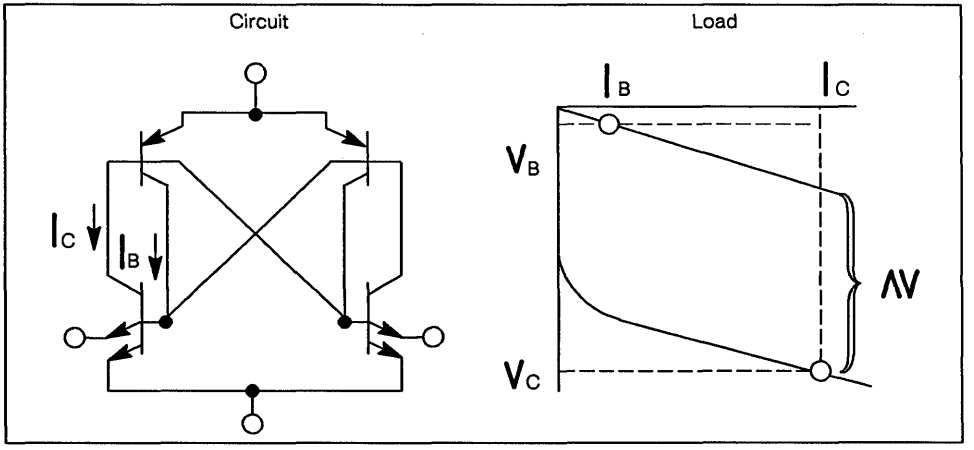

Figure 1-2. PNP Load Cell

The result of this design change is a decrease in noise and an increase in alpha particle immunity. The increased protection from soft error is due to the difference between the dynamic characteristics of the Schottky diode in the standard pull-up configuration and the PNP transistor in the PNP load cell.

Since the voltage drop across the PNP transistor is greater than across the Schottky diode, the /\V for the new design is twice the /\V of the diode cell. The internal capacitance for the two designs is about equal, the base-collector capacitance is about equal, but the base-emitter capacitance is much greater for the PNP cell design because both transistors are saturated. Since the cell noise immunity, or "Q" is the product of the base-emitter capacitance and theΔV of the design, the PNP load cell enjoys a large increase in noise and alpha particle immunity over the diode-resistor design (on the order of a ten to the fifth or a ten to the sixth improvement).

Fujitsu's new design has made it almost impossible for the transistors in a memory cell to be changed by an alpha particle because the size of the charge that holds the on transistor in that state has been increased. If an alpha particle cannot bleed away enough charge to flip the cell, then soft errors cannot occur.

Are There Tradeoffs

The new PNP cell design uses saturated, active components to achieve the high noise immunity that ordinarily would cause a loss of speed. However, in the case of the Fujitsu ECL family, the performance of the ECL Static RAMs has been retained and, in some organizations, improved. Fujitsu has reconciled these two diametrically opposed concepts of high noise immunity and high performance by recovering lost speed through the reduction of propagation delays on the chip itself via improved design rules.

Fujitsu's Improved Design—IOP II and ESPER

Fujitsu uses Isolation by Oxide and Polysilicon (IOP) in its ECL memory designs. The original IOP design has a V-groove isolation channel between cells. The width across the top of the groove was a function of the depth to which the groove had to be etched (see Figure 1-3).

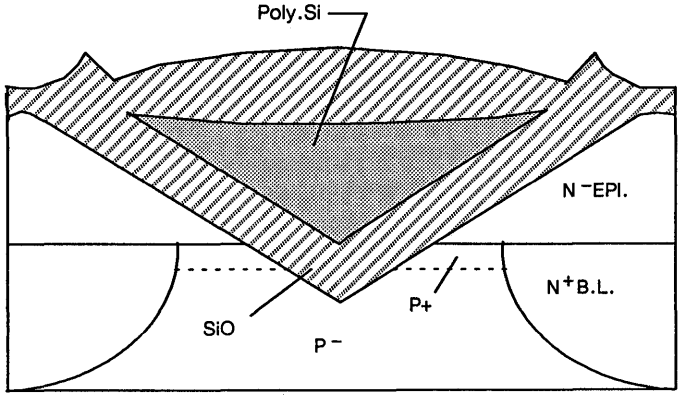

Figure 1-3. Original IOP Design

PNP Load Cell Design (Continued)

The new PNP pull-up cell design features a U-shaped isolation channel instead of a V-shaped one. The IOP II design is shown in Figure 1-4. When a U-shape is used, both the width and the depth of the channel can be carefully controlled. The resultant groove is about one-half the width of the old V-groove. This allows for a reduction in overall die size and a shortening of both row and column lines, while allowing decoders and other peripheral circuitry to be located closer to the cell area. This new set of design rules will be used for all future Fujitsu ECL memory designs.

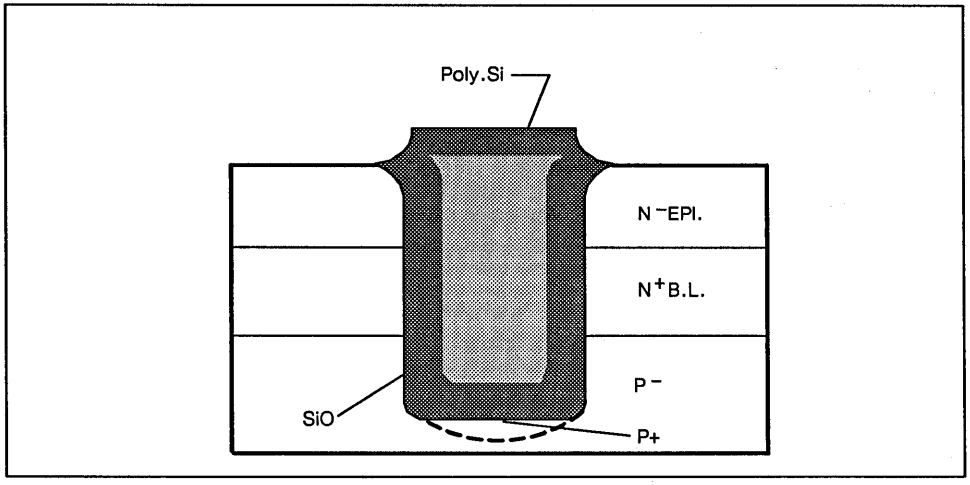

Figure 1-4. IOP II Design

Fujitsu has now developed an improved, second generation PNP load cell design known as ESPER that offers high soft error immunity, smaller die size, lower power dissipation and performance uncompromised by the presence of saturated components in the cell.

Summary

In summary, an ECL memory design that nearly eliminates alpha particle-induced soft error is invaluable to designers of large, fast, mainframe computers, processors, testers, and other systems in which errors cannot be tolerated. The PNP pull-up design of Fujitsu's ECL Static RAMs, when coupled with new technologies such as IOP II and ESPER, achieves this goal with little or no overall loss of ECL performance.

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How to Design Efficient ECL Systems: A Collection of Do's and Don'ts for Designing with Fujitsu's ECL Devices.

by Nusra Lodhi

Fujitsu Microelectronics, Inc.

Publication Number OV0048-877F1

INTRODUCTION

ECL (Emitter Coupled Logic) devices are considered by most computer designers to be the highest performance devices available. However, these devices are not used in many system designs where they could be the most appropriate choice. This restriction stems from the fact that most system designers, even experienced ones, are usually uncomfortable with switching from designing with TTL compatible parts to ECL parts. The purpose of this document is to acquaint both experienced and inexperienced designers with the ECL technology and recommended steps for implementing an ECL design. This document covers different aspects of ECL system design. In order to understand the basic rules for designing with ECL, it is worthwhile to have a brief discussion of what ECL is and how the basic gates are designed.

ECL: WHAT IS IT?

ECL (Emitter-Coupled-Logic) is one form of current mode logic. The basic current switch for Fujitsu's ECL RAM is shown in Figure 1.

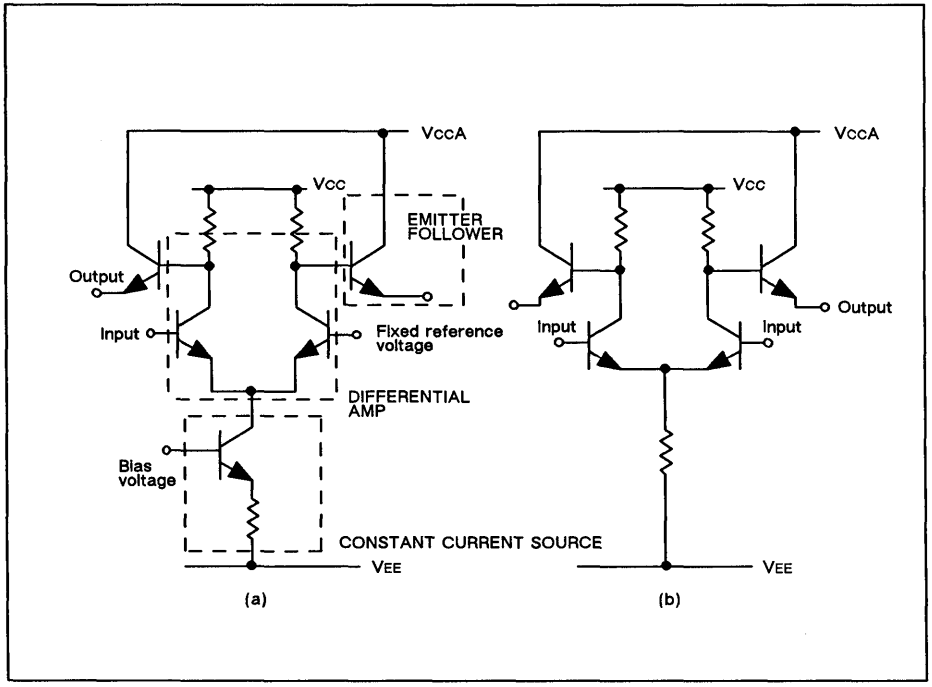


Figure 1. Basic Current Switch for ECL RAM

At the base of this switch there is a constant current source or resistor. (The current source is programmable for ECL gate arrays). The collectors are also connected to resistors.

The inputs can be driven in two different ways. In the first technique, a differential input is used on both the bases of the transistors forming a current switch. Whereas in the second method, an input voltage is applied to one transistor base while a fixed reference voltage is applied to the other transistor base. The latter technique is very common because it has twice the input voltage swing compared to the previous case. Emitter-follower outputs are connected to the collectors to provide high driving capability. With an insight into the basic ECL gate, let us now discuss the nature of the inputs and outputs in a standard ECL RAM.

ECL Inputs

Fujitsu's ECL RAMs have a pulldown resistor on the Chip select input, tied internally to VEE. This input is an assertive LOW signal when left open. Hence, if the input is left floating, the pulldown resistor ensures that the device is held in an active state. On the other hand, the write enable, the address inputs, and the data input pins do not have a pulldown resistor connected internally to VEE. Thus, these pins should never be left floating, because the input level may change due to leakage current. Therefore, it is recommended that the specified level on these inputs be maintained.

Wire-ORing the ECL Outputs

Like the preceding input pins, the output pins do not have pulldown resistors. Hence, wired-OR connections are possible and ECL gate arrays support this feature. However, propagation delays will increase because of greater capacitive loading. Propagation delays increase about 30psec for each output load increase of 1pF. As the output capacitance for the current ECL RAMs is 6pF max, the propagation delay caused by one wired-OR connection is about 180psec. Compared to address access time, the delay is negligible. Fujitsu guarantees the AC characteristics for an output load of 30pF; thus, five 5 wired-OR connections can be used without causing noticeable propagation delays. For ECL gate arrays, Fujitsu recommends using cutoff mode output buffers to wire–OR ECL outputs in order to minimize reflections.

In using the wire–ORed capability, the designer must be aware that the output transistor is never completely at cutoff so, in the high–impedance state, current leakage is possible. If a large number of drivers are combined in a wired-ORed arrangement, the sum of their leakage currents can pull the output voltage out of the logic 0 state. Hence with every additional driver wired to an output, a slight loss in noise margin is incurred. (Reference 1). Before discussing noise margins and their effects, differences between 100K and 10K families must be pinpointed.

Difference Between 10K and 100K

Basic differences between these two families are circuit stability and performance with variations in supply voltage and ambient temperature. 100K ECL parts are both temperature-compensated and voltage compensated; 10K parts are only voltage compensated.

ECL is a current mode logic, that is, it relies on voltage changes to generate changes in current. ECL has only a 1V logic swing with appropriately small noise margins. Before further discussions, an explanation of noise margins is in order.

NOISE MARGIN

Noise margin is a DC voltage specification which measures the immunity of a circuit to adverse operating conditions. This is defined as the difference between the worst-case input logic level (VIH min or VIL max) and the worst-case output (VOH min or VOL max) for the corresponding input logic level. Guaranteed noise margins (NM) for 10K at 25 degree C are:

Logic 1 NM = VOH min - VIH min
= -.960-(-1.105)
= 145mV

Logic 0 NM = VIL max - VOL max
= -1.475-(-1.650)
= 175mV

For 100K it is as follows:

Logic 1 NM = 1.025-(-1.165)=140mV
Logic 0 NM = 1.475-(-1.620)=145mV

For system design, worst case conditions are always considered. If so, the 145mV noise margin becomes the design limit. In system design, the user is concerned with the noise margin when devices at different temperatures and different power supply voltages interface with each other. This is because, the logic level thresholds of ECL parts drift with temperature. Hence, unless the ECL family being used is temperature compensated, a hot driver may not be able to send data to a cold receiver due to threshold differences. This is the result of noise margin impairment due to the ambient temperature differential existing between the receiver and the transmitter circuit. When several hundreds, or thousands of ECL circuits are present in the same cabinet, it becomes difficult to provide sufficient cooling so that all of these circuits are essentially at the same temperature. The bottom line shows it is really worthwhile to use the 100K family with built-in temperature compensation.

Without voltage compensation, output thresholds and switching parameters vary from part to part, thereby decreasing noise margins. Also, power dissipation is the product of the constant current source and the supply voltage VEE; uncompensated ECL circuits will experience rapid power dissipation changes as VEE varies.

High and Low Level for ECL RAM Inputs

A high level for 100K is -880mV to -1025mV. In order to preset the inputs to a high level, they should not be tied directly to the ground which is the higher of the two voltage planes available on the board. If the input is tied directly to ground it will drive the input transistors into saturation, which will drastically slow down the gate's switching time in response to changing signal levels at the inputs which are not tied high. Hence, Fujitsu recommends the following circuit for presetting the inputs (both 10K and 100K) to a high and a low level. The value of the output termination depends upon various factors which will be discussed later in the section on terminating techniques.

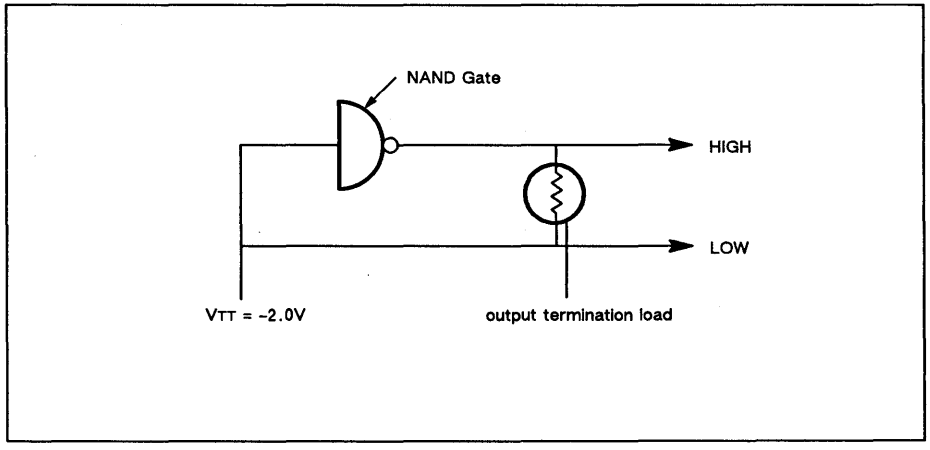


Figure 2. Presetting the Inputs to a High or Low Level

Switching Multiple Inputs and Outputs

The base current flowing through the ECL inputs is very small. Hence, when multiple inputs are switched simultaneously it does not cause any specific problem. However, in case of switching multiple outputs certain precautions should be taken.

This is because output current changes drastically when switching from high to low or from low to high (for 50 ohms termination resistor and termination voltage = -2.0 V, I_{OH} = 22mA and I_{OL} = 5mA). Thus, when multiple outputs (4-bit wide and 8-bit wide devices) are switched simultaneously, current spikes may occur at the V_{CCO} terminal. This in turn induces voltage spikes on V_{CC} (ground) and decreases input and output noise immunity.

Before going into precautions for spikes on the ground lines, a look at the power supply lines on Fujitsu's ECL devices will be beneficial. All ECL devices have a V_{EE} supply line (a negative power supply, -4.5V for 100K and -5.2V for 10K devices) and a V_{CC} ground line. In some ECL RAMs, i.e '422, '474, '484 etc., there are two V_{CC} pins. As shown in Figure 3, V_{CCO} supplies the output drivers while V_{CC} supplies the remaining circuits.

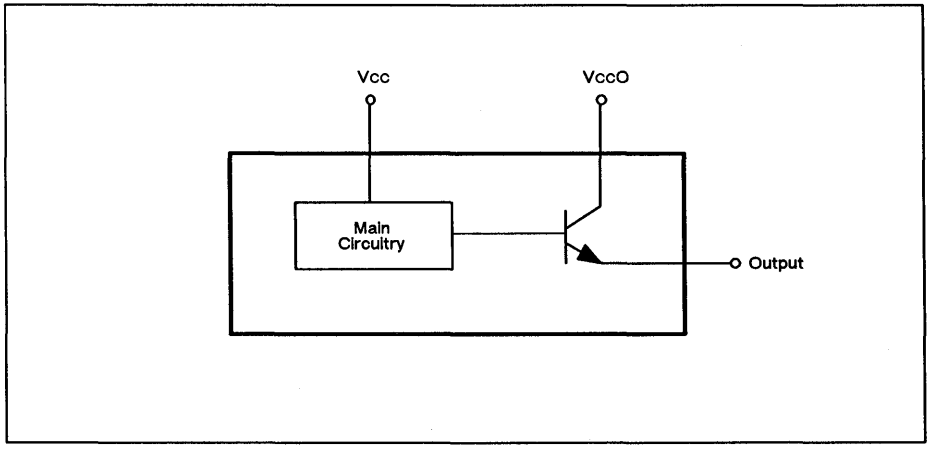


Figure 3. V_{CC} and V_{CCO}

Due to the separation of V_{CC} and V_{CCO}, changes in load currents while the outputs are switching do not cause glitches on the power supply ground bus which is connected to the V_{CC}. This can, however, cause ringing on the outputs.

The ringing can be eliminated by internal connection of V_{CC} and V_{CCO} pins but it may cause spikes on the power supply ground lines when multiple outputs are switching. This is due to the current noise caused by the switching of multiple outputs. These spikes will produce glitches on the output waveforms. Glitches may also be observed when the impedance of the V_{CC} pin is too large.

To prevent ringing on the outputs and glitches on the V_{CC} and V_{CCO} lines, Fujitsu recommends that the V_{CC} and V_{CCO} pins be connected to the nearest place outside

the package. A thick cable for VCC on the printed circuit board is also recommended to reduce the VCC impedance as much as possible.

Preceding discussions were focused on ECL gates and the 10K/100K families of parts. The remainder of this Applications Note is devoted to system design details when switching from TTL to ECL.

EFFECT OF RISE AND FALL TIME

As devices operate faster and faster, rise and fall times become shorter and shorter. For TTL, the voltage swings are typically 2 to 3 volts, while ECL voltage swings are 750 to 1000 millivolt. These TTL swings are harder to deal with than the ECL swings when rise and fall times are only a few nanoseconds. Crosstalk current I which flows between signal paths through a coupling capacitor C is proportional to dV.

$$I = CdV/dt$$

I = cross talk current
C = coupling capacitor
dt = given rise/fall time
dV = logic swing

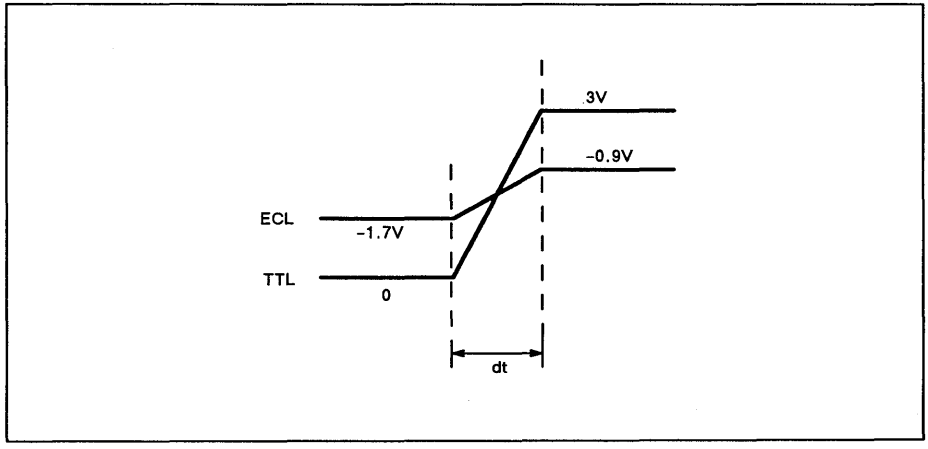


Figure 4. Voltage Swings for ECL and TTL Signals

For a given set of rise and fall times, the crosstalk for TTL is more than ECL because dV for TTL is greater.

Another difficulty is that at very high-speeds it becomes hard for circuit designers to develop satisfactory output buffers to drive realistic signal line impedances with full TTL voltage swings (Reference 1).

TERMINATING TECHNIQUES FOR THE ECL DEVICES

Any signal path on a circuit board may be considered as a form of transmission line. If the line propagation delay is short with respect to the rise time of the signal, any reflections are masked out during rise time and are not seen as overshoot or ringing (Reference 2). Thus when the edge speed increases with faster forms of logic, the line lengths should be shorter in order to retain signal integrity.

When high-speed signals are transmitted over long lines, terminations should be used to minimize reflections and line distortion. These reflections cause ringing on the signal line, which, if severe, will effect system noise immunity. The reflections appear as undershoot and overshoot as shown in Figure 5.

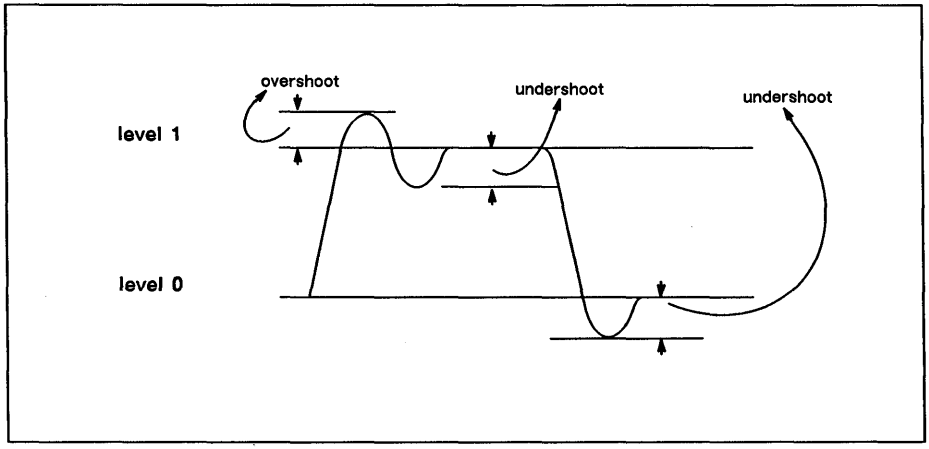


Figure 5. Definition of Overshoot and Undershoot

For best system performance the designer should consider using termination resistors when the two-way propagation time of the line is greater then the rise time of the signal on the line.

In ECL systems, every output must be terminated in the characteristic impedance of the signal interconnection which is being driven. However, these terminations depend on the physical parameters of the circuit boards. Realistic values are 50 to

75 ohms for multilayer etched boards, 100 ohms for multiwire boards(R), and 100 to 120 ohms for wirewrap boards (Reference 1). Standard, prepackaged termination resistors are available with values of 50 ohms, 68 ohms, 75 ohms, and 100 ohms.

Basically, there are two methods of termination viz: parallel termination and series termination. Respectively, these two methods are required for impedance matching and damping.

Parallel Termination

Parallel termination lines are used for the fastest circuit performance.There are two methods of parallel termination. In the first method, the termination resistor can be connected to a termination supply voltage VTT of -2.0V as shown in Figure 6. The value of the termination resistor Rp should match the transmission line impedance Zo. If there is an appreciable mismatch, line reflections will be present with an increase in both noise and propagation delay. In parallel terminated lines, the line termination supplies the output pulldown. Consequently, no pulldown resistor is required at the output of the driving gate.

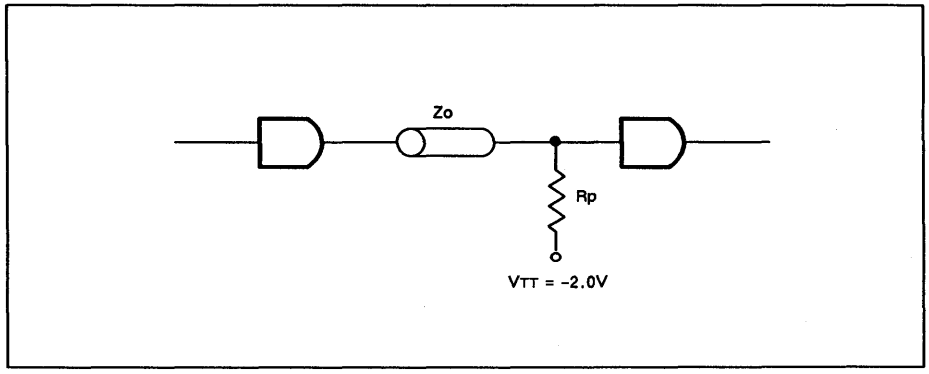
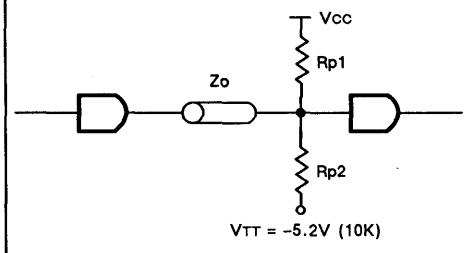


Figure 6. Parallel Termination Using Separate Termination Voltage Plane VTT.

However, equivalent Zo may decrease when the loads are distributed over the transmission line. Hence, the designer should consider each case separately. The recommended value of Rp is 50, 75, 100 or 150 ohms depending on the estimated value of Zo. (The values of Zo can be calculated for various transmission lines as shown in Ch 3 of Reference 2). For large systems where total power is a consideration, the lines are normally terminated with a -2.0V DC supply. When

power consumption is a major concern, this is the most efficient manner of terminating ECL circuits. The drawback, of course, is the requirement of an additional power supply voltage.

In the second method, a pair of resistors is connected in series between ground (VCC) and VEE, providing a Thevinens equivalent resistance and voltage. In this case VTT = VEE = -5.2V (10K) as shown in Figure 7.



Zo (Ω)	Rp1 (Ω)	Rp2 (Ω)
50	81	130
70	113	182
75	121	195
80	130	208
90	146	234
100	162	260
120	194	312
150	243	390

Figure 7. Parallel Termination Using Thevinens Equivalent

Rp1 and Rp2 are selected so that they satisfy the following equation:

$$1/Zo = 1/Rp1 + 1/Rp2$$

Hence

$$Rp1 = 1.625\ Zo$$
$$Rp2 = 2.6\ Zo$$

for

$$VTT = -5.2V\ (10K)$$

In contrast to the first method, this technique requires about 11 times more power per termination (because the drop across the termination resistance is not as large) and uses twice as many components per termination. The advantage, however, is the non- requirement of a special power supply or a separate voltage plane per circuit board.

Series Termination

Overshoot and ringing on longer lines may be controlled by using series damping or series terminating techniques. Series damping is accomplished by inserting a small

resistor Rs in series with the output of the gate as shown in Figure 8. In this case, the value of Rp is such that it can drive 5 — 15mA of current. As for VTT, -2.0V is not compulsory, hence -5.2V(10K) can be used. It is mandatory that Rs be equal to Zo. Signal transmitted from (A) is reflected at (B). But due to the presence of Rs (Rs=Zo), this signal is not seen at (B). The advantage of this method is that the power does not increase as much as in the parallel termination method even when multiple lines are connected to (A). (**Note:** This advantage is not effective if the load is distributed on the signal lines.)

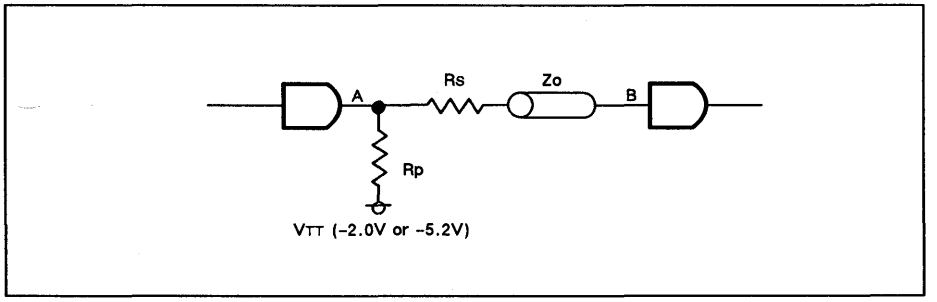


Figure 8. Series Termination

For efficient ECL system design, it is important to know not only the termination techniques but also power supply considerations (tolerances and decoupling), as well as the board layout techniques.

Power Supply Voltage Tolerances

Power supply voltage tolerances must be equal to or better than ±5% for 10K ECL parts. 100K ECL parts are designed to operate over the range of -4.2 to -5.7 volts, which includes the 10K voltage range and also includes the 100K range of -4.5 volts ±7%.

Power Supply Decoupling

Power supply decoupling is required at the point of board entry and at every ECL device. In order to block low frequency noise from entering the board, a tantalum electrolytic capacitor of 22 microfarads or more is placed across the main power supply terminals. On the other hand to block high frequency noise, Rf grade ceramic disk capacitors of 0.1 microfarads are placed across the main power pins

of each device (Reference 1). It is recommended that a 0.1 microfarad capacitor be placed at the end of each row of packages for additional decoupling. If the ground plane is not good, then a 0.1 microfarad bypass capacitor should be used for every two packages.

For good design, the power supply ground line noise should be limited to less than 50mV peak-to-peak. Also maintain VEE power supply voltage with less than 10mV difference among all logic cards to which the signals must interconnect (Reference 2).

For dealing with very high frequency noise, boards are available which have internal power supply voltage planes separated from each other by a few mils thickness of mylar, to provide distributed capacitor for the whole board.

SOME THOUGHTS ON CIRCUIT BOARDS AND LAYOUT

Standard double-sided circuit boards with good ground distribution may be used. A low impedance ground is necessary because any noise which is present on the ground lines are coupled into the signal lines. Any voltage drop across the ground impedance will increase noise response of the ECL circuits (Reference 2).

In the past, most of the ECL work has been done with multilayer, custom-designed etched PC boards. If proper care is used in designing, then Multiwire(R)* boards and /wirewrap boards can also be used. Several vendors offer wirewrap boards which are specifically designed for ECL work.

One thing is worth mentioning about the ground and voltage planes on these boards and that is, to ensure clean signals, at least 50% or more of the board area should be occupied by ground and voltage planes (Reference 1). These voltage planes present a low impedance return path to the ECL circuits and so act as electromagnetic shields for the signal lines.

For high-speed systems, signal lines should be kept as short as possible to minimize ringing and overshoot. Ringing and overshoot are due to the intrinsic inductance and capacitance of the line itself and can be reduced by shortening the lines. In so doing, propagation delays are minimized and critical timing parameters are easier to achieve. Also for ECL circuits, the ringing on the logic level 1 is critical as it subtracts from noise immunity.

Fanout Limitations for ECL Outputs

When laying out a circuit board an important consideration is device fanout. Fanout is the number of inputs which can be driven by a single output. This is

greater in the ECL world than in the TTL world. For gold-doped TTL, a fanout of 10 is assumed. In case of ECL, if one looks at the ratio of external output currents to input currents in ECL specifications, the fanout is about 100, so there are no fanout limitations. Although there are other disadvantages, each additional input which is connected to a given output adds more capacitance. This in turn will cause switching time delays as well as decrease in the output transmission line impedance which causes reflections. In case of MBM10480-15, this delay is about 30psec/1pF.

Note: Multiwire is a registered trademark of Multiwire Corp.

Also, input capacitance of an ECL RAM varies depending on the package type and the pin location. For the MBM10480, typical input capacitance is as follows:

	PACKAGE CENTER	PACKAGE CORNER
DIP	3.5pF	4.8pF
FPT	3.0pF	3.8pF

For other ECL RAMs, these values can be requested from Fujitsu. In addition to fanout limitations for the ECL outputs, another factor that should be considered while working with ECL devices is the voltage swings and the slew rate.

EDGE RATES FOR THE ECL FAMILIES

In ECL circuits, the output logic swing is typically 900mV. Rise and fall times are defined as the transition time between 20% and 80% reference points as shown in Figure 9. The difference of the voltage level between 20% point and 80% point is about 540mV (900mV x 60%). The voltage slew rate is 0.54/tr or 0.54/tf (V/ns).

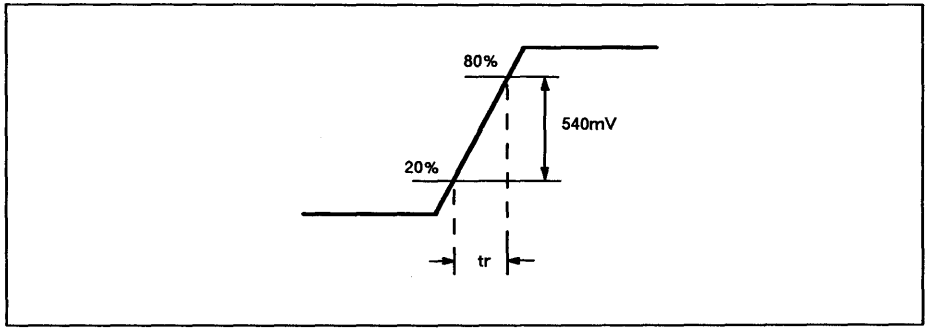


Figure 9. Rise Time

In most system designs, ECL, TTL, and CMOS devices are intermixed; thus, the designer should understand the "whats", "whys", and "hows", of interfacing these technologies.

INTERFACING TECHNIQUES

Intermixing of 10K and 100K ECL Families

ECL is used to obtain the required circuit speed and provide the circuit features necessary to optimize high-speed system design. All ECL of the same family interface directly with each other. As mentioned previously, the power supply range of 100K ECL includes the range of 10K parts. Hence, no basic physical problems are encountered when interfacing these two families. The real problem is when a 100K output is connected to a 10K input. At high temperatures, V_{OH} min of 100K approaches V_{IH} max of 10K. This results in a decrease in noise margin. However, this type of connection is allowed if the operating ambient temperature of all the ECL devices is under control. Another important fact is that when 100K is operated at -5.2V, V_{OH} is shifted to a low level by about 30mV. The devices can still function as indicated by the data sheet specification, although max/min limits of each parameter cannot be guaranteed.

Interfacing ECL RAMs with TTL

Circuits of the 10K ECL family normally operate with ground on V_{CC} and a negative supply 5.2V DC power supply on V_{EE}. The negative supply operation has a noise immunity advantage and is recommended for large systems. Circuits of the 100K ECL family normally operate on V_{CC} and -4.5V DC power applied to V_{EE}.

With the -5.2V power supply for 10K ECL, the high logic level is about -0.96V and the low logic level is about -1.65V. This provides a small voltage swing of 690mV. So for this reason, the 10K ECL and 100K ECL are not directly compatible with common slower-speed logic types such as TTL and MOS. Translators should be used when interfacing ECL with these devices.

The most common interface requirement for ECL is with TTL logic levels. This occurs when ECL system must interface with an existing TTL system or when both ECL and TTL are used in the same system design. The interface requirements between ECL and TTL depends on how circuits are being used.

The normal ECL/TTL interface occurs when ECL is powered with a -5.2V power supply (10K devices) or -4.5V power supply (100K devices) and TTL is powered

with a +5V power supply. The use of common ground and separate power supplies will isolate the TTL generated noise from ECL supply lines. At the outputs of the ECL devices translators are used to convert ECL level to TTL level.

On the other hand, for interfacing TTL to ECL devices, TTL to ECL translators are used. These devices usually have a propagation delay in the order of 1.6nsec. The devices from Fujitsu are shown in Table 1.

Table 1. TTL to ECL Translators

PART #	INPUT	OUTPUT	tPD (TYP)	NO. OF CKT PER PACKAGE	PACKAGE
MB766	ECL 10KH	TTL	5nsec at 75pF	8	DIP-20
MB767	TTL	ECL 10KH	1.6nsec	8	DIP-20

Usually the ECL to TTL translators have a propagation delay which is dependent on fanout loading. Thus, if more devices are being driven, tPD of these translators increase. For ECL gate arrays, on-chip translators are used; hence, intermixing of ECL with TTL can be easily accomplished.

Interfacing with TTL on a Common Power Supply

In many system designs, where only a small number of ECL devices are used, it is desirable to operate both ECL and TTL on a +5V DC power supply. ECL works well in this mode (pseudo-ECL) if care is taken to isolate the TTL generated noise from the ECL +5V supply line. Translators for interfacing TTL and ECL in this mode are built out of discrete components since integrated circuit translators do not operate on +5V. Typical discrete translators (ECL/TTL and TTL/ECL) are shown in Figure 10(a) and (b) (Reference 2). The ECL/TTL translator uses one PNP transistor for translation and the typical translation delay time is less than 10nsec when one high-speed TTL load is driven. The TTL/ECL translator consists of three resistors in series to attenuate TTL outputs to ECL requirements. The translation is very fast, normally under 1 nsec, depending on wiring delays and stray capacitance.

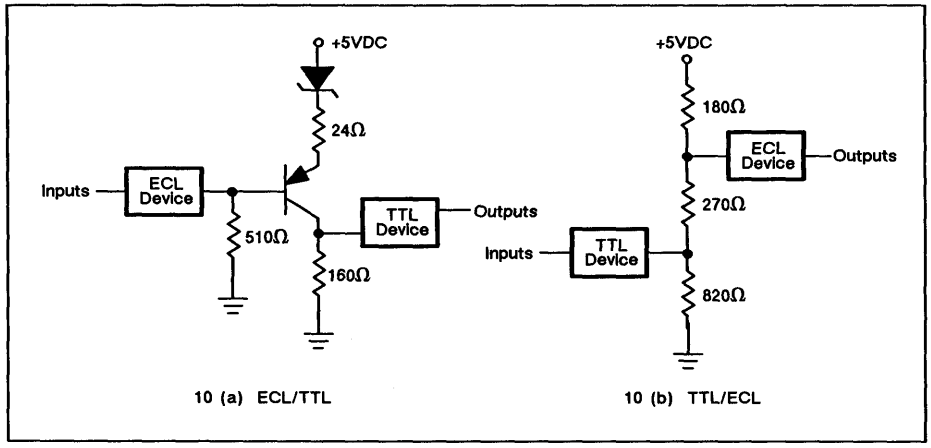


Figure 10. Discrete Translators

Interfacing ECL to CMOS

The ECL/MOS interface varies with the MOS power supply voltage. For P-channel MOS circuits operating between ground and a $-V_E$ voltage, a discretely built translator is used. Modern N-channel circuits are commonly TTL compatible, so CMOS at +5V operates with TTL logic levels. For such cases, TTL/ECL translators are used.

ECL devices offer an efficient solution to a high-performance system design as compared to TTL and CMOS with only one extra requirement for system cooling. The reason for this is that ECL devices consume more power than TTL. Thus, it is important for ECL system design to consider the thermal characteristics of the ECL devices and the different cooling techniques normally used.

Thermal Considerations for ECL Circuits

The electrical power dissipated in any integrated circuit forms a heat source in the package. This heat source increases the temperature of the circuit die relative to some reference point (normally 25 degree C ambient) in an amount which depends upon the net thermal resistance between the heat source and the reference point. Thermal resistance, theta, is the difference between the temperature of the junction and the temperature of the reference point, per unit power dissipation. Thermal

resistance is the primary figure of merit for power handling capability of any integrated circuit package. Thermal resistance from "junction to case", theta JC, and/or the thermal resistance from "junction to ambient ", theta JA, are the thermal parameters most often specified for integrated circuit packages. The junction temperature T_j for a given junction to ambient thermal resistance theta JA, power dissipation P_D, and ambient temperature T_A, is given by :

$$T_j = P_D \theta_{JA} + T_A \quad \text{---------- (i)}$$

If a heat sink is used and it has the thermal resistance θ_{SA} (sink to ambient) and the thermal resistance from junction to case, θ_{JC}, is given by :

$$T_j = P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A \quad \text{---------- (ii)}$$

where θ_{CS} = thermal resistance from integrated circuit (case) to heat sink.

The values of θ_{JC}, θ_{JA} for Fujitsu's ECL RAMs and different ECL gate arrays are available upon request.

Thermal resistance is not usually specified for digital ICs, though maximum power dissipation is generally defined. The maximum ambient temperature rating is the usual point-of-interest for users of digital integrated circuits. Regardless of the ambient temperature, the system designer using ECL should be aware of the device junction temperature. The lower the junction temperature of the device, the higher the reliability and consequently the life of the device. For every 10-degree rise in junction temperature, the MTBF (Mean Time Between Failure) decreases by a factor of 2.

Cooling Techniques

ECL products dissipate a lot of heat. The power dissipated in an integrated circuit is the heat source for thermal purposes. This power dissipation is somewhere in the vicinity of 1 Watt. This means to stay within the operating range of 0 to 75 degree C, designers have to pay special attention to heat dissipation in their systems.

The majority of ECL users provide some form of air flow cooling in medium and large size systems. Fujitsu specifies a constant air flow of more than 500 linear feet per minute across the package. As air passes over devices on a printed circuit board, it absorbs heat from each package. Thus, the ambient temperature of the air will increase as it flows from the inlet to the outlet. The heat gradient from the first package to the last package is a function of the package density, air flow rate, and the individual package dissipation.

The major means of heat transfer from the top of the die to the outside surface of the package is by conduction through the solids. Heat transfer through the bonding wire from die to lead frame is negligible. Once heat is transmitted to the package, transfer to ambient air depends upon the package mounting techniques and its environment. If the integrated circuit package is installed in, or attached to a heat sink, the heat transfer is mainly due by conduction to a heat sink, and then by convection and radiation from the heat sink to the ambient. Figure 11 shows the different type of heat sinks recommended by Fujitsu. The material used is Aluminum. The number of fins is dependent upon the theta JA of the device. If theta JA is large then more fins are required.

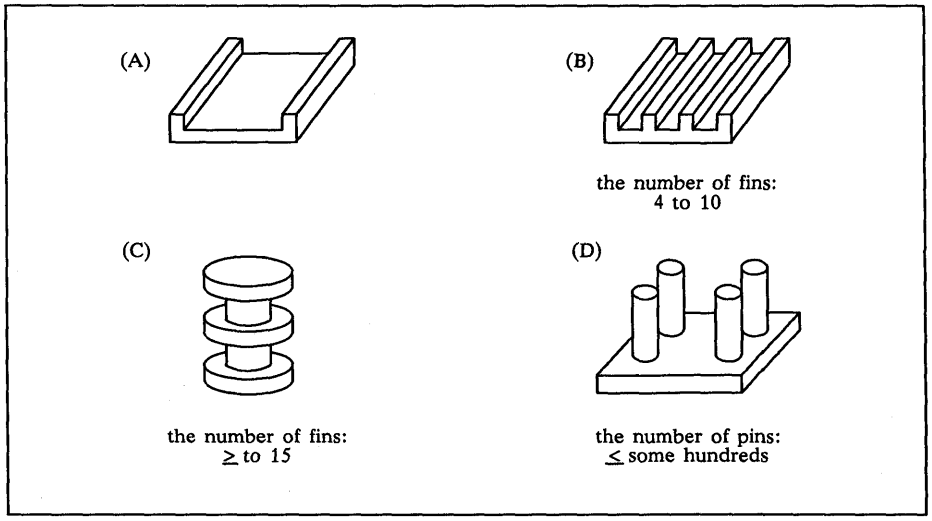


Figure 11. Recommended Heat Sinks

Besides air cooling together with heat sinks, some users use emergent cooling techniques when the system generates a lot of heat.

Liquid Coolants

As mentioned earlier, cooling is used to prevent excessive temperatures, since higher power together with reduced size often results in detrimentally high heat dissipation density.

A common technique used for cooling of high performance and high voltage electronic equipment use a dielectric liquid. This is used in many applications

where forced air cooling is not adequate. The liquid cooling techniques commonly used are divided into four categories.

1. Ebullient (Boiling) Cooling
2. Free (Natural) Convection

In both these techniques, the sealed package with electronic components is immersed in fluid.

3. Forced convection-Laminar flow
4. Forced convection turbulent flow

In these techniques, the coolant is circulated through or around the outside of the package.

The basic considerations in selecting a coolant for electronic system are :

1. Properties relating to heat transfer (density, thermal conductivity, specific heat, viscosity, etc).
2. Properties relating to handling (boiling point, freeze point, toxicity, etc.)
3. Properties relating to electrical characteristics (dielectric strength, dielectric constant, etc).
4. Properties relating to reliability (compatibility with components, thermal stability).
5. Cost.

The classes of liquids considered suitable as dielectric coolants are petroleum oil, diester synthetic oil, polyglycols, phosphate Esters, chlorinated hydrocarbon, Fluorocarbons (Flourinert (R) liquids) and Chloroflurocarbons, silicones and silicate esters. Most ECL users using liquid cooling techniques use Fluorinert (Reference 3). The Fluorinert(R) liquids provide effective heat transfer in free or forced convection. Cooling by boiling, using Flourinert liquids is even more effective. Because of their ability to remove heat so rapidly, especially in boiling, the Flourinert liquids keep component temperatures lower and thus reduce failure rates and increase reliability. Thus the components can be packaged closer together to maximize power densities and minimize equipment size.

FUJITSU'S ECL RAM FAMILY

Fujitsu offers an extensive line of different organizations and speeds of ECL SRAMs, both in 10K and 100K. The deepest configuration now available is the 64K x 1 at 15nsec and the fastest ECL RAM available is 5nsec at 4K and 1K depth. In addition to this, Fujitsu also offers a 16-bit wide ECL RAM which are 256 and 1024 words deep. In addition to the Buffer Address Array, the Color Display Palette and Self-Timed RAMs are offered as Application Specific memories.

ECL Gate Arrays

Fujitsu offers a wide variety of ECL gate arrays. The largest gate array available at present is about 4500 gates (ET4500). The basic gate in this series features typical propagation delay times of only 220 picoseconds unloaded and 500 picoseconds loaded (3mm wire loaded).

Finale

This paper has covered most of the questions which may arise in the system designer's mind, when planning to work with ECL system design instead of the usual TTL environment. For system designers, the ECL technology with efficient implementation brings a new dimension of expertise and problem-solving ability to an already advanced field. However, one common benefit will be encountered by both the experienced and inexperienced designer and, that is, a major gain in system speed over standard TTL designs.

References

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3. *Coolant Selection For Electronic Systems*, Leon A. Sigel, Westinghouse Electric Corporation, Aerospace Division, Baltimore, Maryland.

FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10422A-5
MBM 10422A-7

April 1986
Edition 3.0

1

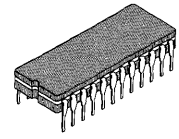
1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10422A is fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

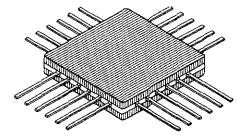
The MBM 10422A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10422A is specified over a temperature range of from 0° to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10 K-series ECL families.

- 256 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time: 5 ns max. (MBM 10422A-5)
  7 ns max. (MBM 10422A-7)
- Block select access time: 3 ns max. (MBM 10422A-5)
  4 ns max. (MBM 10422A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.7 mW/bit typ.
- DOPOS and IOP-II processing
- Pin compatible with the F10422



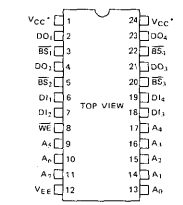
CERAMIC PACKAGE
DIP-24C-C05

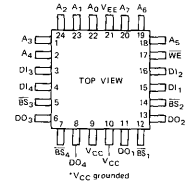


CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See Page 9

PIN ASSIGNMENT





LCC PAD CONFIGURATION: See Page 9

ABSOLUTE MAXIMUM RATINGS (See NOTE)

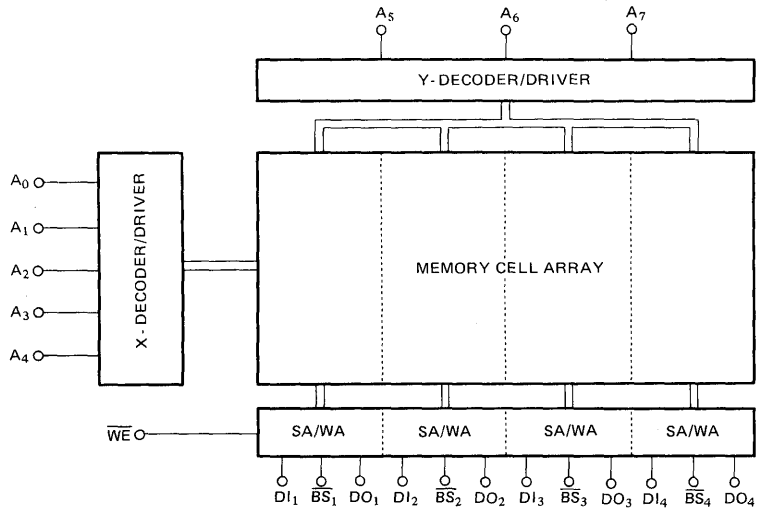
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A for DIP	−55 to +125	°C
	T_C for Flat Package and LCC	−55 to +125	
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 10422A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{BS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10422A is fully decoded 1024-bit read/write random access memory organized as 256 words by 4 bits. Memory cell selection is achieved by means of a 8-bit address designated $A_0 \sim A_7$. The active low Block Select ($\overline{BS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{BS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{BS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage		-5.46	-5.2	-4.94 V	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for flat package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{BS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	-200			mA	0°C to 75°C

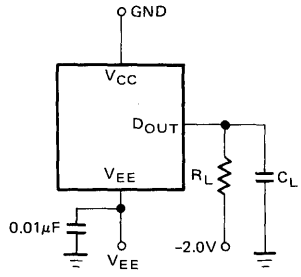
CAPACITANCE

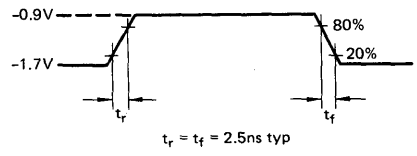
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		6	7	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ± 5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

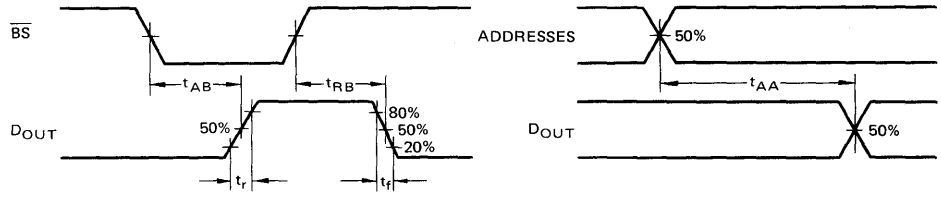
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10422A-5			MBM 10422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			5		5	7	ns
Block Select Access Time	t_{AB}			3		2.5	4	ns
Block Select Recovery Time	t_{RB}			3		2.5	4	ns

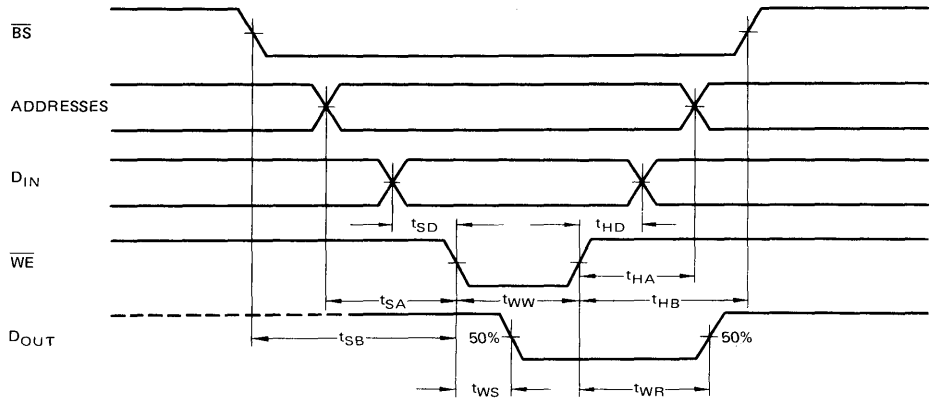
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10422A-5			MBM 10422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	3.5			5			ns
Write Disable Time	t_{WS}			3.5			4	ns
Write Recovery Time	t_{WR}			3.5			8	ns
Address Set Up Time	t_{SA}	0.5			1			ns
Block Select Set Up Time	t_{SB}	0.5			1			ns
Data Set Up Time	t_{SD}	0.5			1			ns
Address Hold Time	t_{HA}	1.0			1			ns
Block Select Hold Time	t_{HB}	1.0			1			ns
Data Hold Time	t_{HD}	1.0			1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

1

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

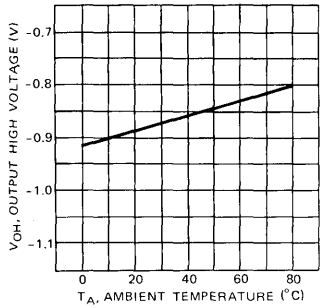


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

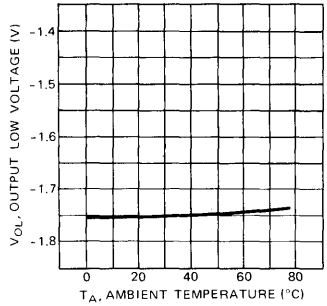


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

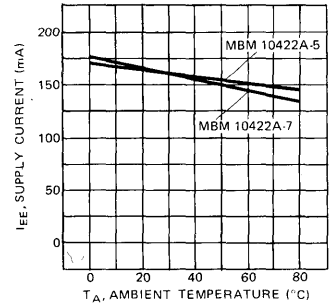


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

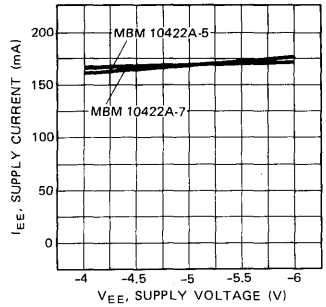


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

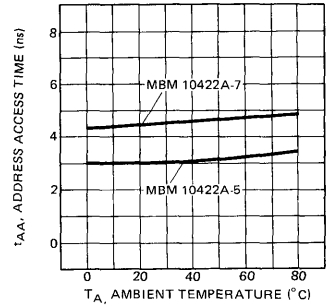


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

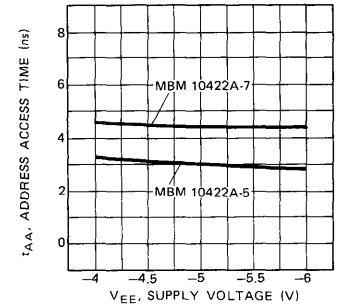


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

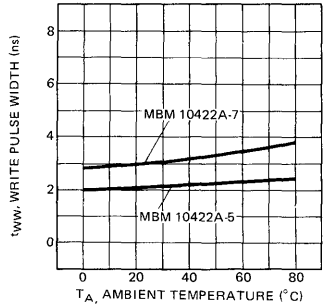
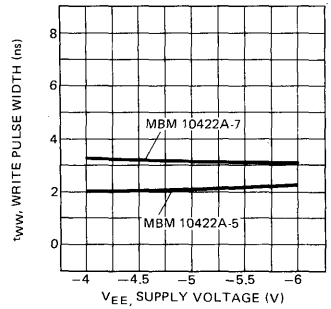


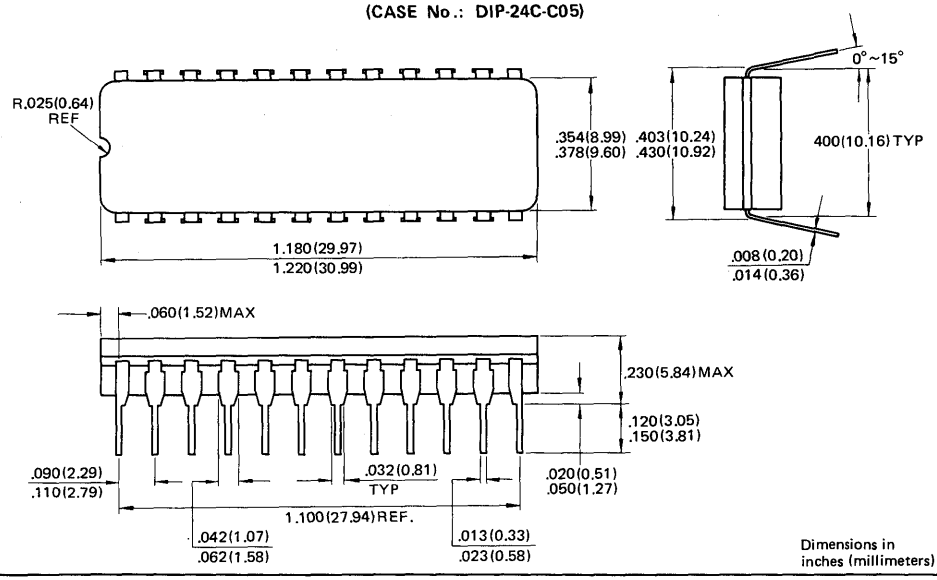
Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)

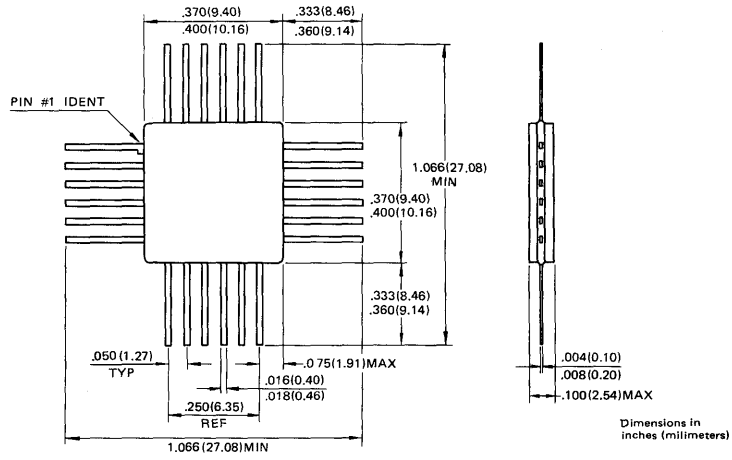
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



Dimensions in inches (millimeters)

CERAMIC FPT (: -ZF)

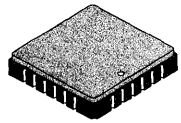
24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



Dimensions in inches (milimeters)

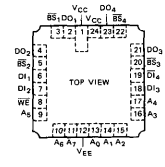
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

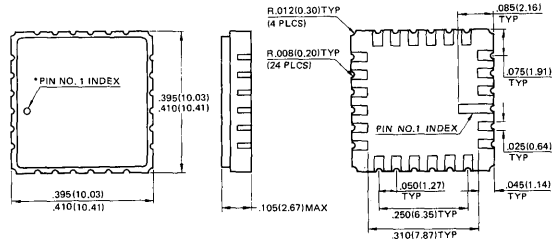


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100422A-5
MBM 100422A-7

April 1987
Edition 3.0

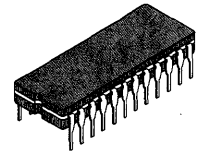
1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100422A is fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

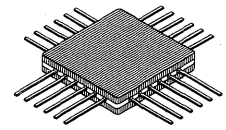
The MBM 100422A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 100422A is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 256 words x 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K-series ECL families
- Address access time: 5 ns max. (MBM 100422A-5)
  7 ns max. (MBM 100422A-7)
- Block select access time: 3 ns max. (MBM 100422A-5)
  4 ns max. (MBM 100422A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.7mW/bit
- DOPOS and IOP-II processing.
- Pin compatible with the F100422.



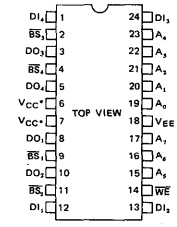
CERAMIC PACKAGE
DIP-24C-C05

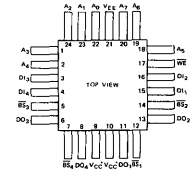


CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See Page 8

PIN ASSIGNMENT





*V_{CC} grounded

LCC PAD CONFIGURATION: See Page 8

ABSOLUTE MAXIMUM RATINGS (See NOTE)

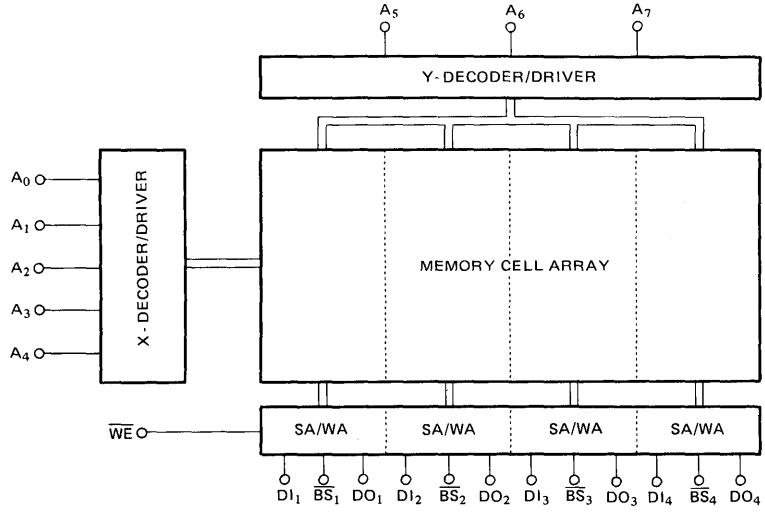
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A for DIP	−55 to +125	°C
	T_C for Flat Package and LCC		
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100422A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{BS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100422A is fully decoded 1024-bit read/write random access memory organized as 256 words by 4 bits. Memory cell selection is achieved by means of a 8-bit address designated A_0 through A_7. The active low Block Select ($\overline{BS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{BS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{BS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Value			Unit	Ambient Temperature for DIP Case Temperature for Flat Package and LCC
		Min	Typ	Max		
Supply Voltage	V	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V, T_A = 0°C to 85°C for DIP, Air flow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output High Voltage (V_{IN} = $V_{IH\,max}$ or $V_{IL\,min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\,max}$ or $V_{IL\,min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\,min}$ or $V_{IL\,max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\,min}$ or $V_{IL\,max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\,max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\,min}$)	I_{IL}	-50			μA
$\overline{BS}$ Input Low Current (V_{IN} = $V_{IL\,min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-200			mA

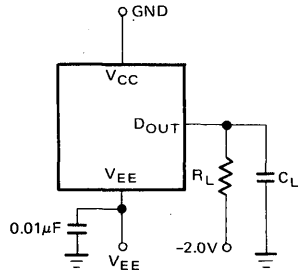
CAPACITANCE

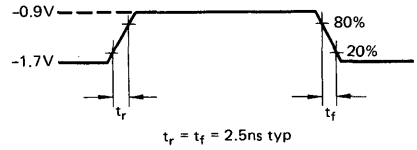
Parameter	Symbol	MBM 100422A-5			MBM 100422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Pin Capacitance	C_{IN}			6			5	pF
Output Pin Capacitance	C_{OUT}			7			8	pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V ± 5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Air flow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

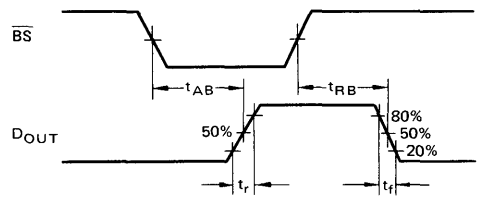
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

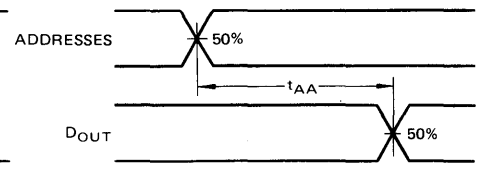
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100422A-5			MBM 100422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	1.5		5			7	ns
Block Select Access Time	t_{AB}	0.5		3			4	ns
Block Select Recovery Time	t_{RB}	0.5		3			4	ns

READ CYCLE TIMING DIAGRAMS

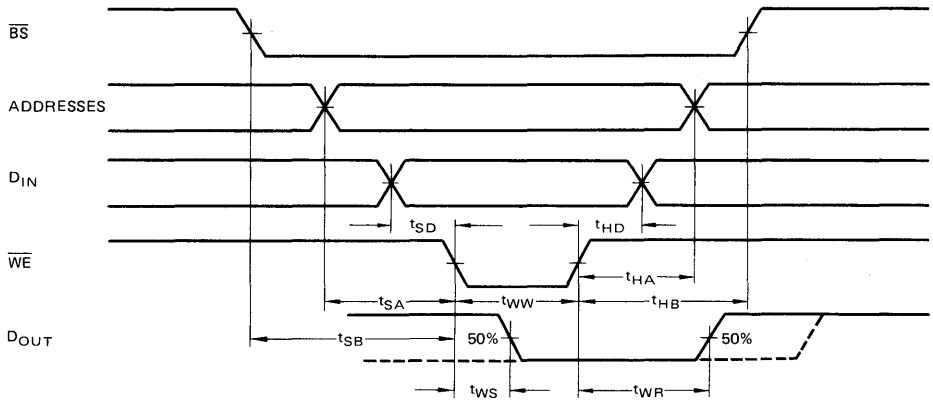




WRITE CYCLE

Parameter	Symbol	MBM 100422A-5			MBM 100422A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	3.5			5			ns
Write Disable Time	t_{WS}	0.5		3.5			4	ns
Write Recovery Time	t_{WR}	0.5		3.5			8	ns
Address Set Up Time	t_{SA}	0.5			1			ns
Block Select Set Up Time	t_{SB}	0.5			1			ns
Data Set Up Time	t_{SD}	0.5			1			ns
Address Hold Time	t_{HA}	1.0			1			ns
Block Select Hold Time	t_{HB}	1.0			1			ns
Data Hold Time	t_{HD}	1.0			1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

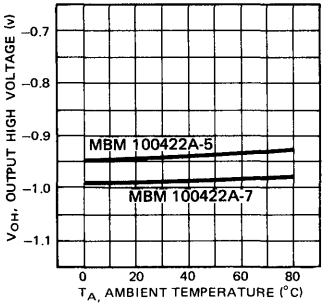


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

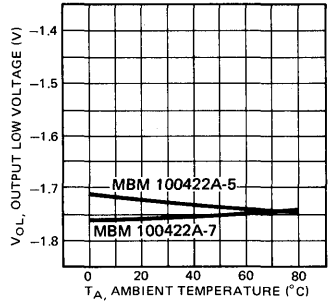


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

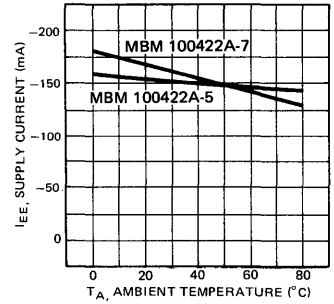


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

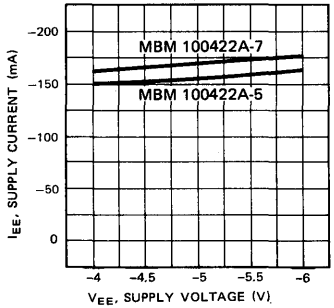


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

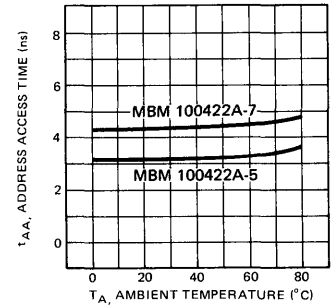


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

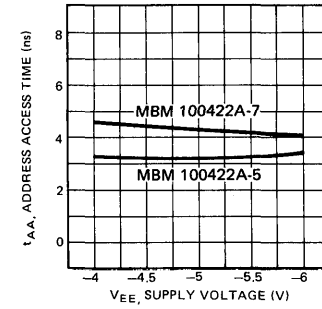


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

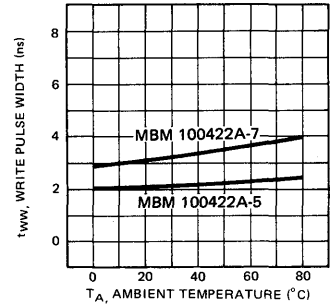
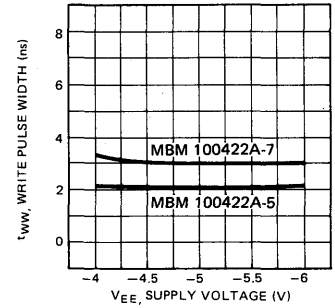


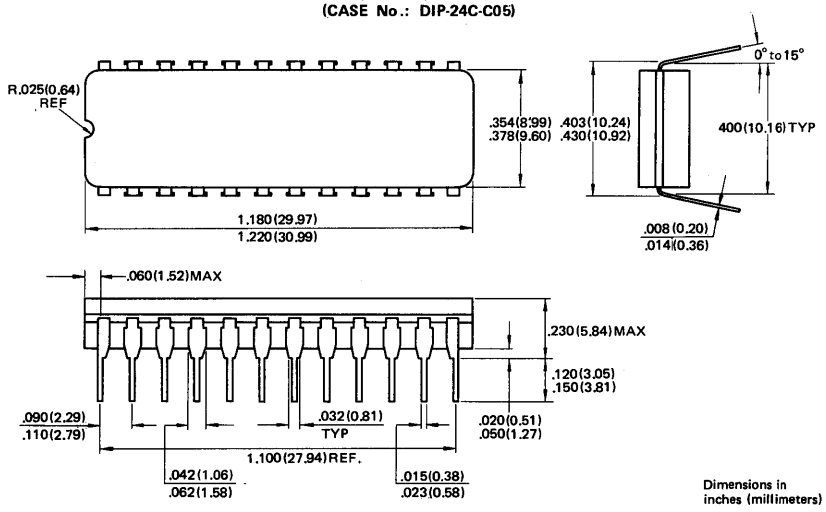
Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)

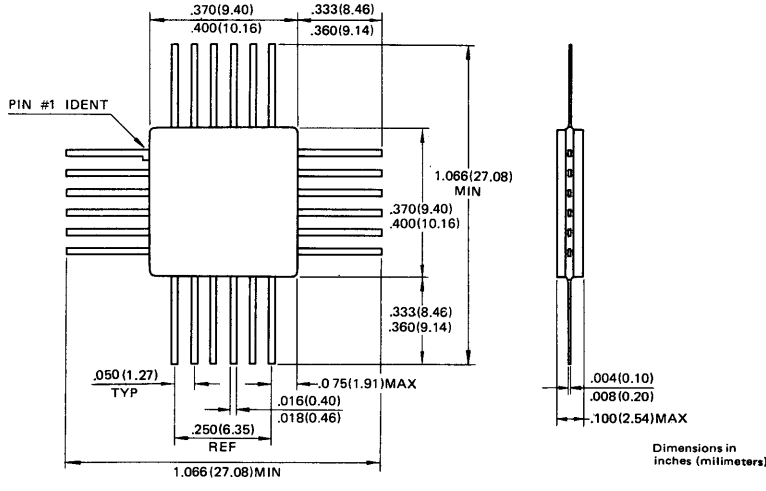
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



Dimensions in inches (millimeters)

CERAMIC FPT (: -ZF)

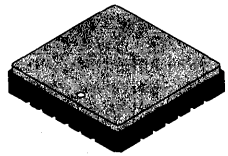
24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



Dimensions in inches (millimeters)

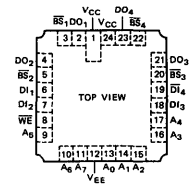
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

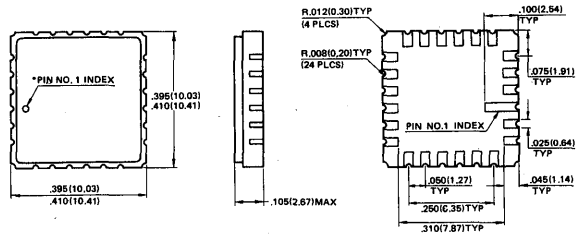


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10470A-7

August 1988
Edition 1.0

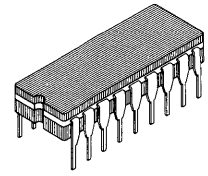
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10470A is a fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage compensation for improved noise margin.

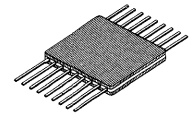
The MBM10470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10470A is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 18-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

- 4096 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time :7 ns max.
- Chip select access time :3.5 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation :0.22 mW/bit (typ.)
- DOPOS and IOP-II processing
- Pin compatible with the F10470



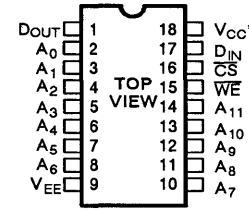
CERAMIC PACKAGE
DIP-18C-C01

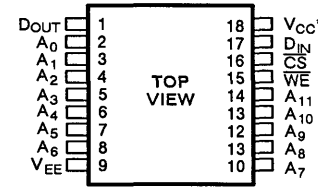


CERAMIC PACKAGE
FPT-18C-C01

LCC-18C-F01 See Page 10

PIN ASSIGNMENT





*V_{CC} grounded

LCC PAD CONFIGURATION: See Page 10

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

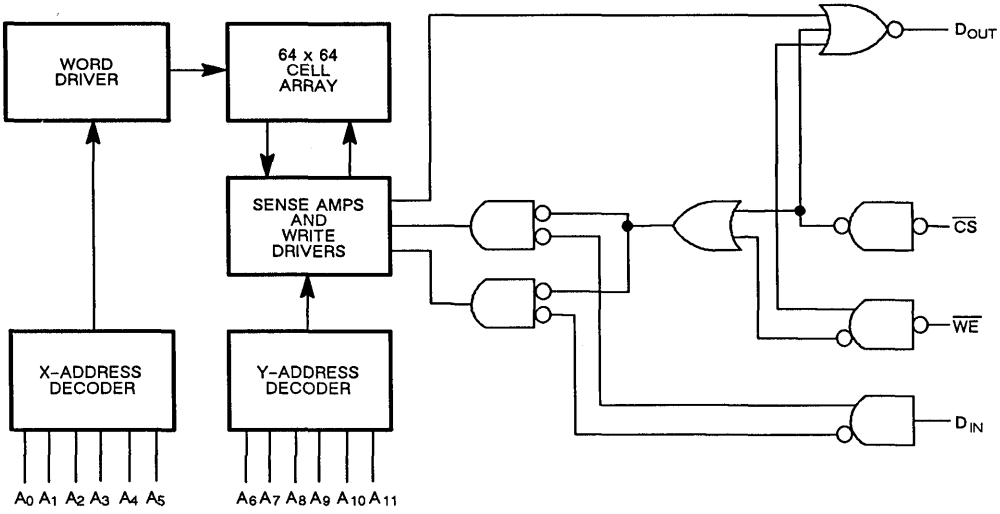
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

1

Fig. 1 — MBM10470A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10470A is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0 °C 25 °C 75 °C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0 °C 25 °C 75 °C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OHC}	-1020 -980 -920			mV	0 °C 25 °C 75 °C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OLC}			-1645 -1630 -1605	mV	0 °C 25 °C 75 °C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0 °C 25 °C 75 °C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0 °C 25 °C 75 °C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			-220	µA	0°C to 75°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	-200			mA	0°C to 75°C

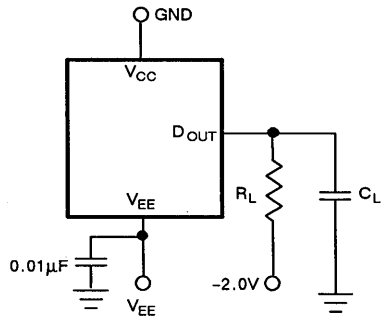
CAPACITANCE

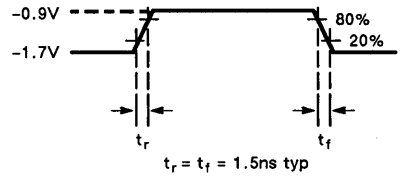
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V ±5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITION





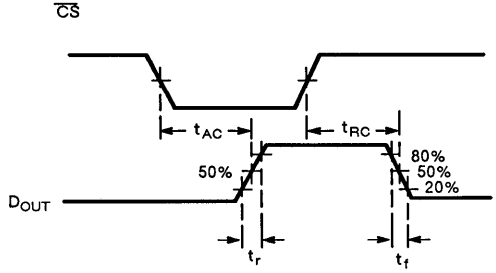
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

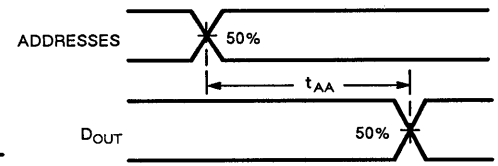
Note: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM10470A-7			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}			7	ns
Chip Select Access Time	t_{AC}			3.5	ns
Chip Select Recovery Time	t_{RC}			3.5	ns

READ CYCLE TIMING DIAGRAMS

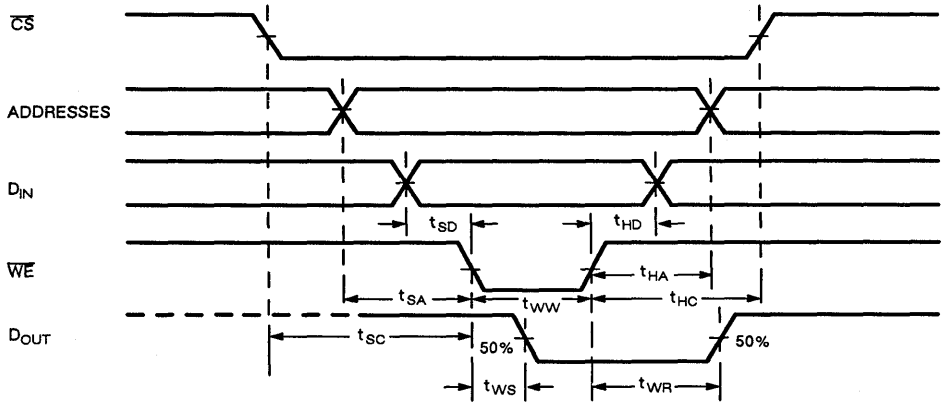




WRITE CYCLE

Parameter	Symbol	MBM10470A-7			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	7			ns
Write Disable Time	t_{WS}			3.5	ns
Write Recovery Time	t_{WR}			8	ns
Address Set Up Time	t_{SA}	1			ns
Chip Select Set Up Time	t_{SC}	0			ns
Data Set Up Time	t_{SD}	0			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	0			ns
Data Hold Time	t_{HD}	0			ns

WRITE CYCLE TIMING DIAGRAMS



RISE TIME and FALL TIME

Parameter	Symbol	MBM10470A-7			Unit
		Min	Typ	Max	
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

TYPICAL PERFORMANCE CHARACTERISTICS

FIG. 3 – OUTPUT HIGH VOLTAGE VS AMBIENT TEMPERATURE

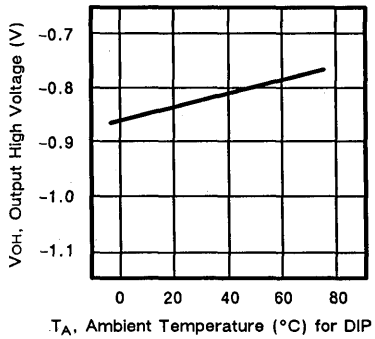


FIG. 4 – OUTPUT HIGH VOLTAGE VS SUPPLY VOLTAGE

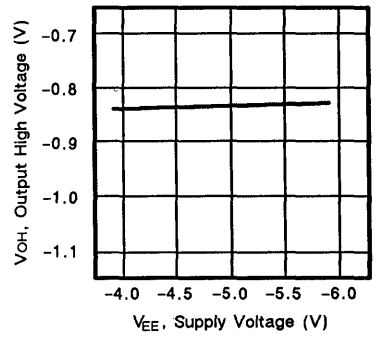


FIG. 5 – OUTPUT LOW VOLTAGE VS AMBIENT TEMPERATURE

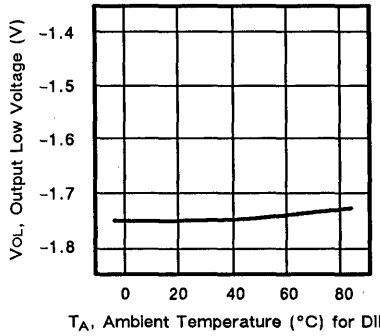


FIG. 6 – OUTPUT LOW VOLTAGE VS SUPPLY VOLTAGE

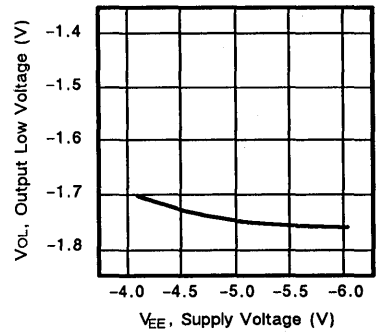
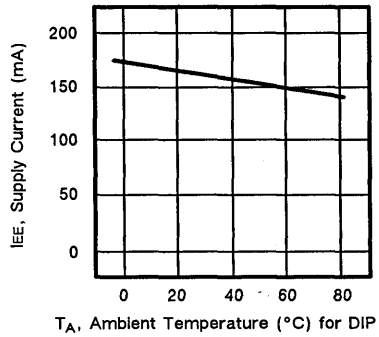


FIG. 7 – SUPPLY CURRENT VS AMBIENT TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

FIG. 8 – ADDRESS ACCESS TIME VS AMBIENT TEMPERATURE

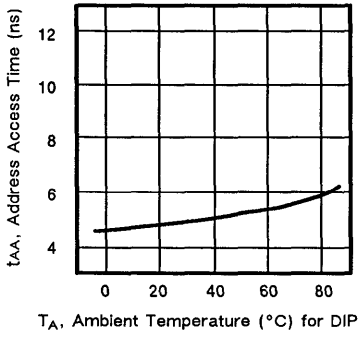


FIG. 9 – ADDRESS ACCESS TIME VS SUPPLY VOLTAGE

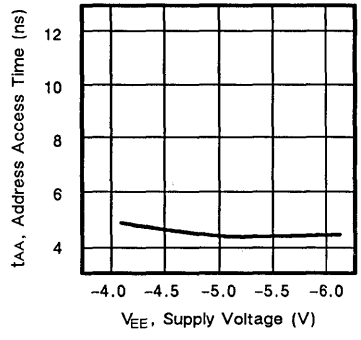


FIG. 10 – WRITE PULSE WIDTH VS AMBIENT TEMPERATURE

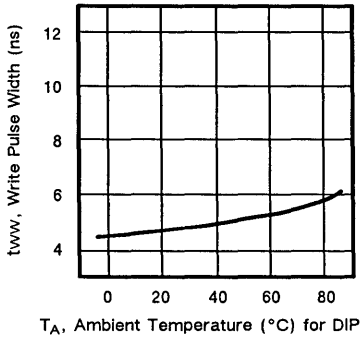
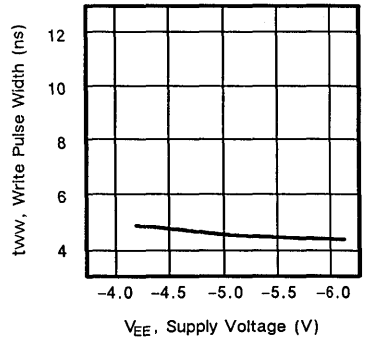
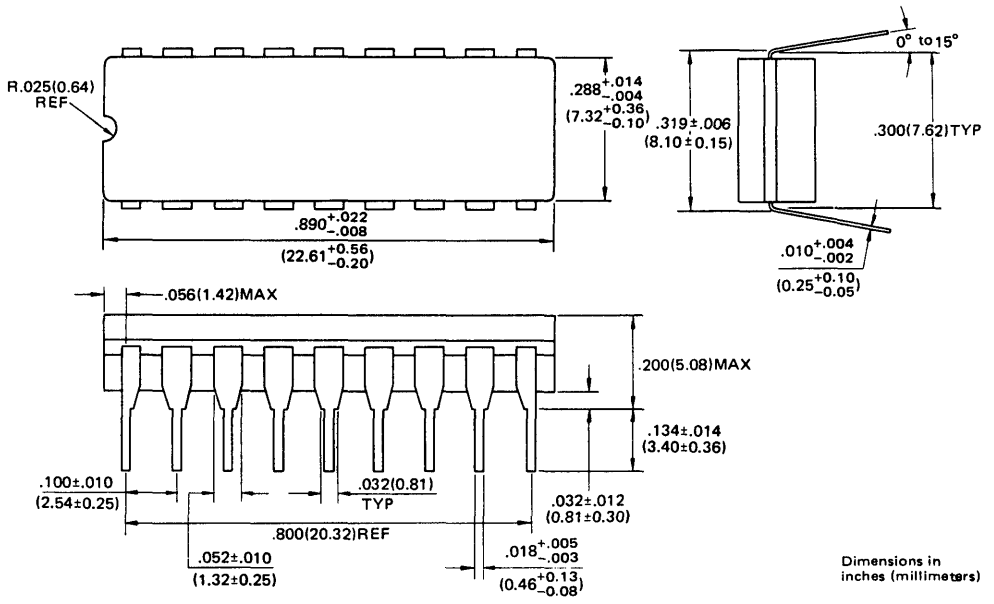


FIG. 11 – WRITE PULSE WIDTH VS SUPPLY VOLTAGE



PACKAGE DIMENSIONS

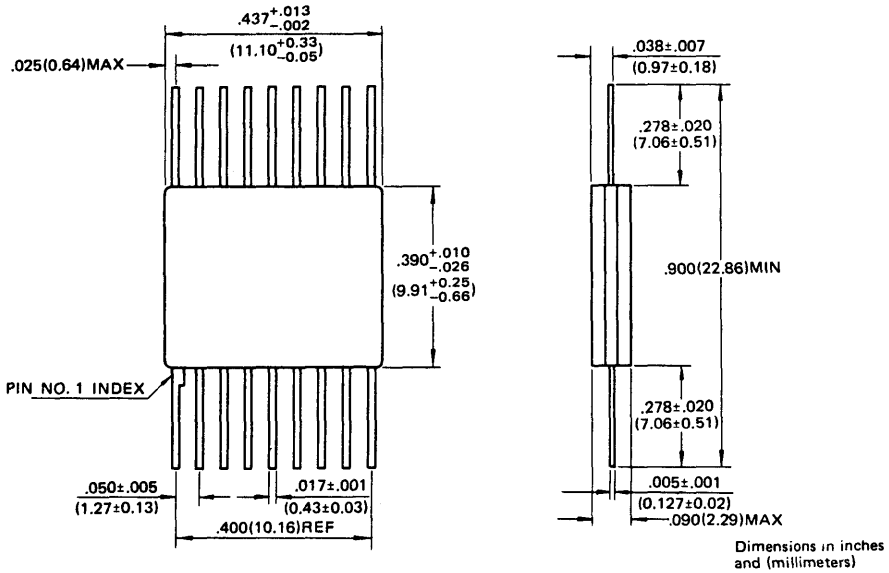
18-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18C-C01)



Dimensions in inches (millimeters)

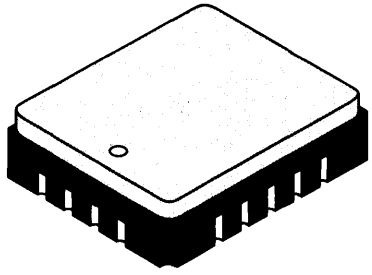
PACKAGE DIMENSIONS (continued)

18-LEAD CERAMIC (AXIAL) FLAT PACKAGE
(CASE No.: FPT-18C-C01)



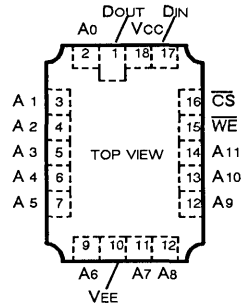
Dimensions in inches and (millimeters)

PACKAGE DIMENSIONS (continued)



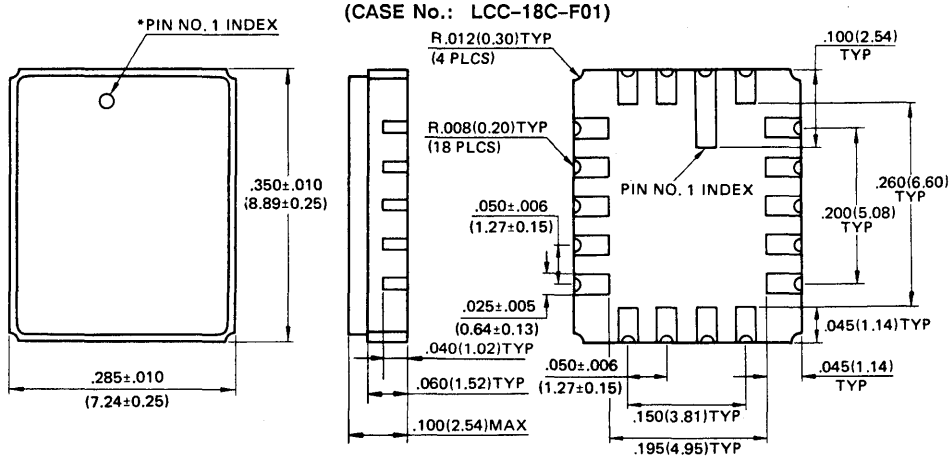
LCC-18C-F01

PAD CONFIGURATION



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER

(CASE No.: LCC-18C-F01)



*Shape of Pin 1 index: Subject to change without notice

Dimension in inches and (millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10470A-10
MBM 10470A-15
MBM 10470A-20

July 1984
Edition 2.0

1

4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10470A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage compensation for improved noise margin.

The MBM 10470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

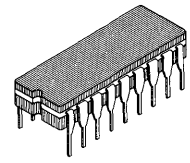
Operation for the MBM 10470A is specified over a temperature range of from 0° to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 18-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

- 4096 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time: 10 nsec. max. (MBM 10470A-10)
  15 nsec. max. (MBM 10470A-15)
  20 nsec. max. (MBM 10470A-20)
- Chip select access time: 6 nsec. max. (MBM 10470A-10)
  8 nsec. max. (MBM 10470A-15)
  15 nsec max. (MBM 10470A-20)
- Open emitter output for ease of memory expansion
- Low power dissipation: 0.22mW/bit
- DOPOS and IOP-II processing
- Pin compatible with the F10470

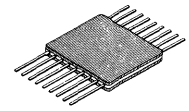
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.



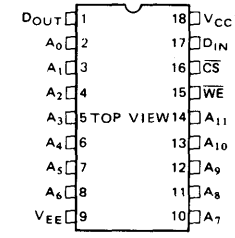
CERAMIC PACKAGE
DIP-18C-C01

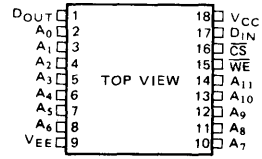


CERAMIC PACKAGE
FPT-18C-C01

LCC-18C-F01 : See Page 10

PIN ASSIGNMENT





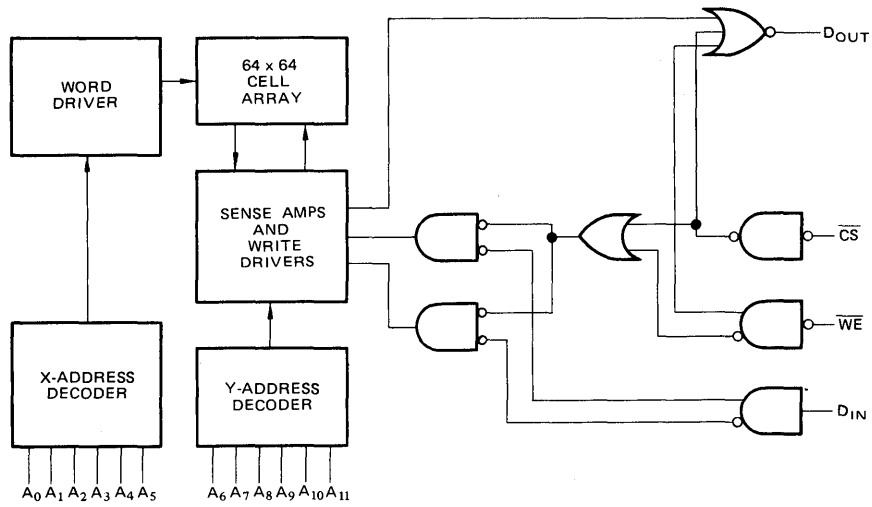
*V_{CC} grounded

LCC PAD CONFIGURATION : See Page 10

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 10470A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10470A is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 75°C for DIP, Airflow≧2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max}$)	I_{IH}			−220	μA	0°C to 75°C
Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	−200			mA	0°C to 75°C

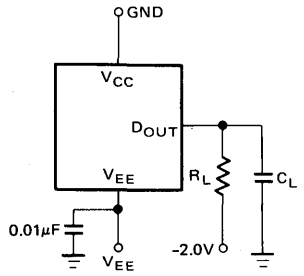
CAPACITANCE

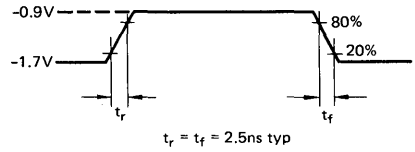
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V ± 5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

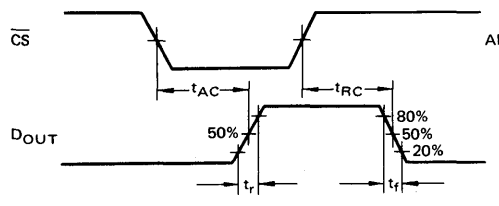
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

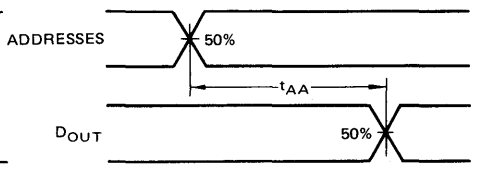
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10470A-10			MBM 10470A-15			MBM 10470A-20			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			10			15			20	ns
Chip Select Access Time	t_{AC}			6			8			15	ns
Chip Select Recovery Time	t_{RC}			6			8			15	ns

READ CYCLE TIMING DIAGRAMS

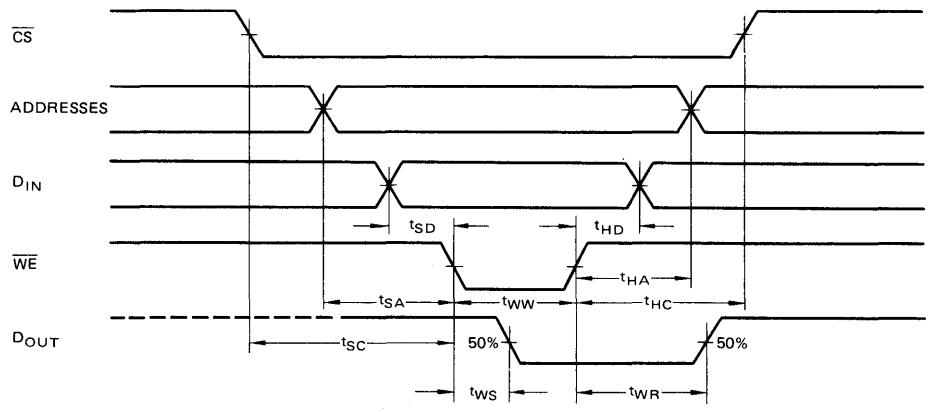




WRITE CYCLE

Parameter	Symbol	MBM 10470A-10			MBM 10470A-15			MBM 10470A-20			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	12			15			15			ns
Write Disable Time	t_{WS}			6			8			15	ns
Write Recovery Time	t_{WR}			10			10			15	ns
Address Set Up Time	t_{SA}	1			1			3			ns
Chip Select Set Up Time	t_{SC}	1			1			2			ns
Data Set Up Time	t_{SD}	1			1			2			ns
Address Hold Time	t_{HA}	2			2			2			ns
Chip Select Hold Time	t_{HC}	2			2			2			ns
Data Hold Time	t_{HD}	2			2			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	MBM 10470A-10			MBM 10470A-15			MBM 10470A-20			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Rise Time	t_r		1.5			1.5			1.5		ns
Output Fall Time	t_f		1.5			1.5			1.5		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

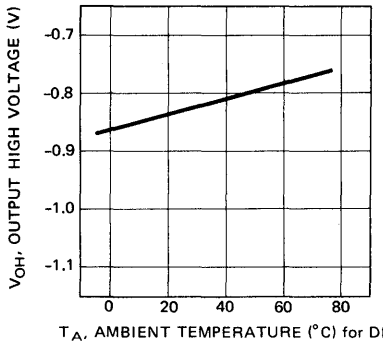


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

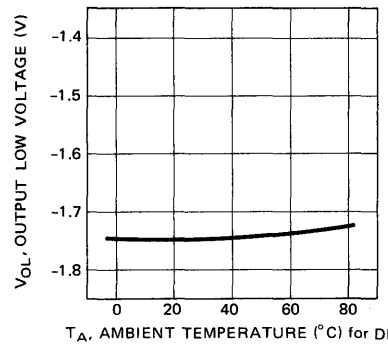


Fig. 5 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

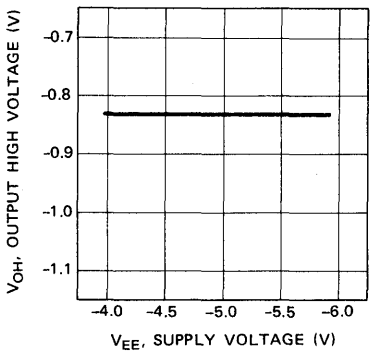


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

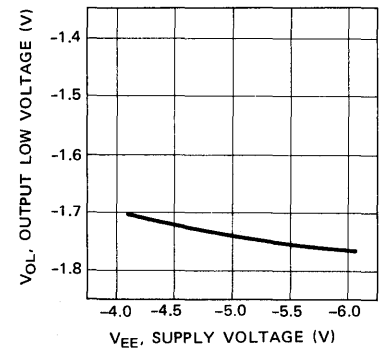


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

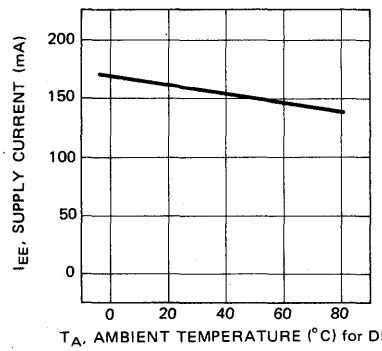


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

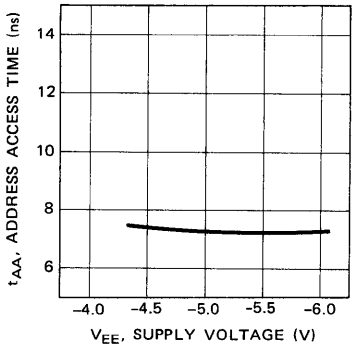


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

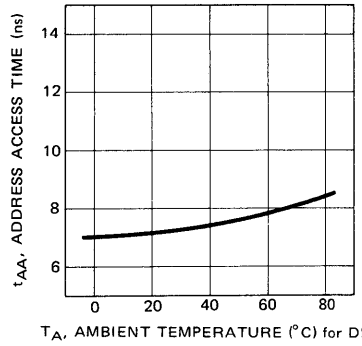


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

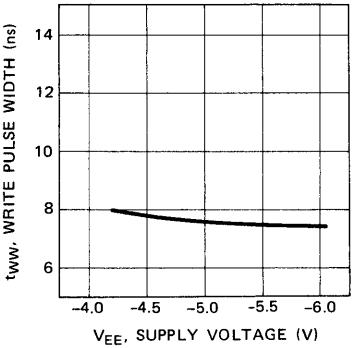
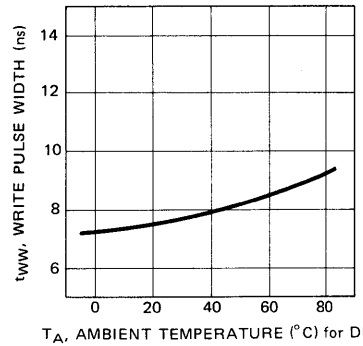


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



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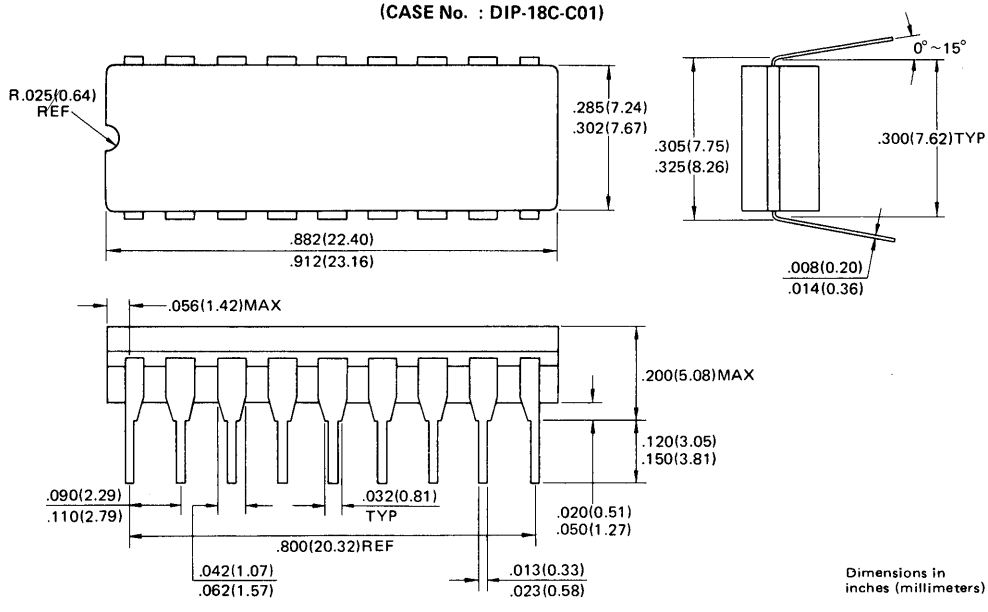
1

PACKAGE DIMENSIONS

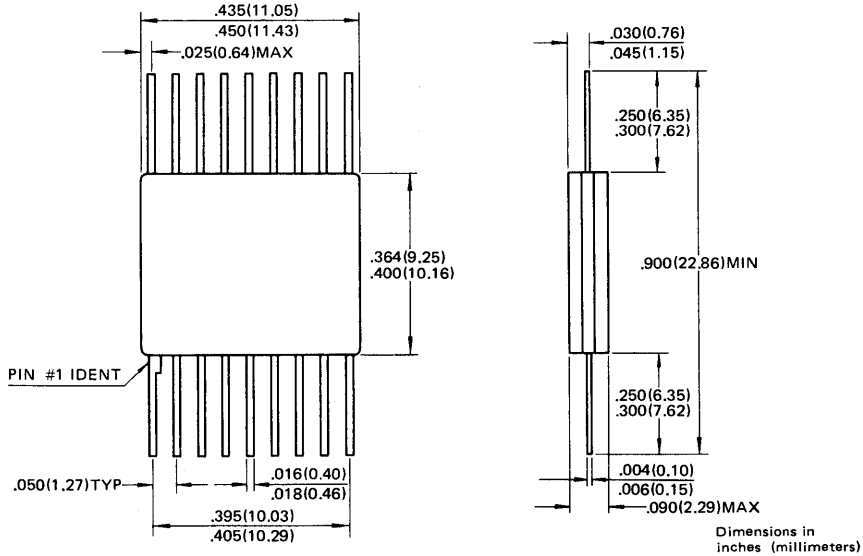
18-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-18C-C01)



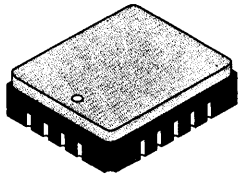
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

18-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No. : FPT-18C-C01)

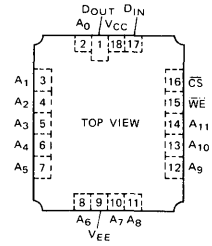


PACKAGE DIMENSIONS

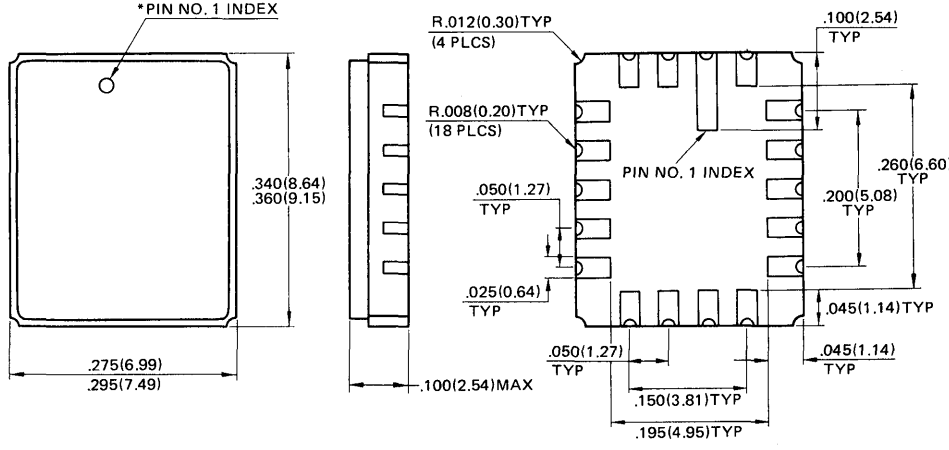


LCC-18C-F01

PAD ASSIGNMENT



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE NO.: LCC-18C-F01)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100470A-7

August 1988
Edition 1.0

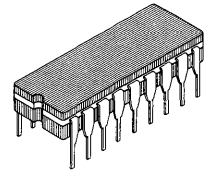
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100470A is a fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

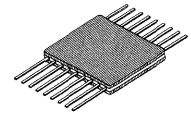
The MBM100470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100470A is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 18-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 4096 words x 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K-series ECL families
- Address access time :7 ns max.
- Chip select access time :3.5 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation :0.19 mW/bit (typ.)
- DOPOS and IOP-II processing
- Pin compatible with the F100470



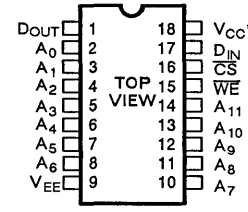
CERAMIC PACKAGE
DIP-18C-C01

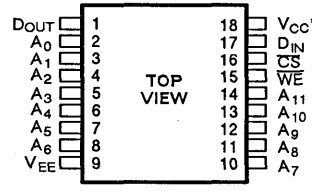


CERAMIC PACKAGE
FPT-18C-C01

LCC-18C-F01: See Page 10

PIN ASSIGNMENT





*V_{CC} grounded

LCC PAD CONFIGURATION: See Page 10

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

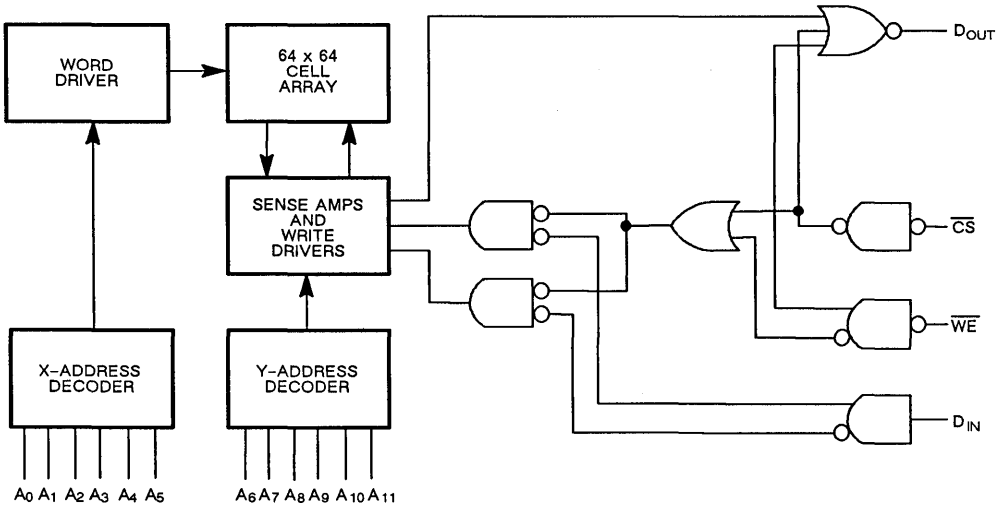
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

1

Fig. 1 — MBM100470A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100470A is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Oper emitter outputs are provided to allow for maximum flexibility ir output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	µA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-200			mA

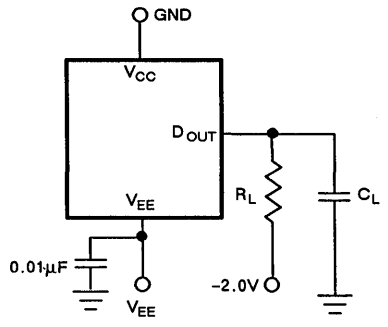
CAPACITANCE

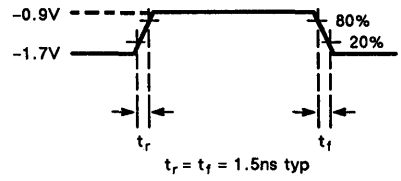
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −4.5V ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 1.5ns typ

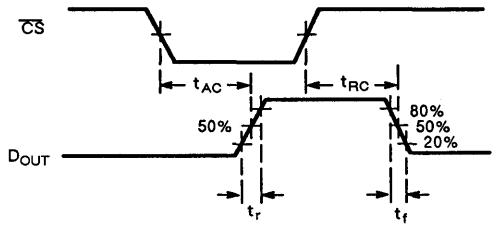
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

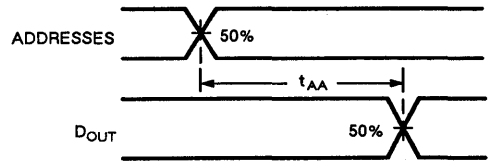
Note: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM100470A-7			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}			7	ns
Chip Select Access Time	t_{AC}			3.5	ns
Chip Select Recovery Time	t_{RC}			3.5	ns

READ CYCLE TIMING DIAGRAMS

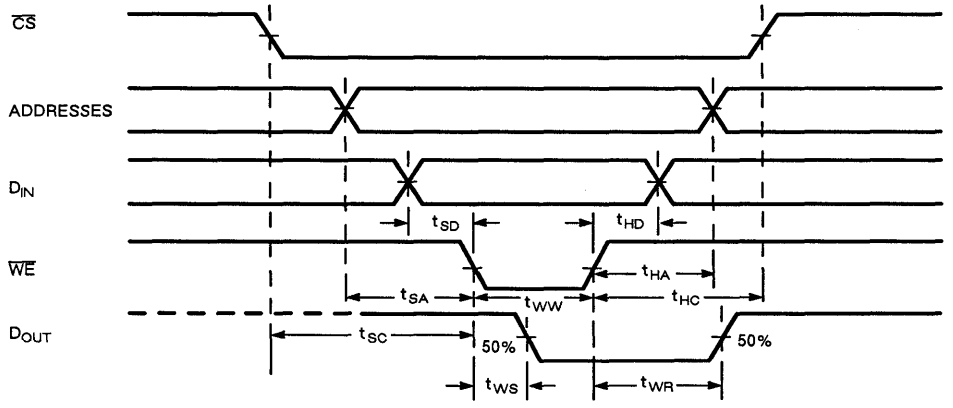




WRITE CYCLE

Parameter	Symbol	MBM100470A-7			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	7			ns
Write Disable Time	t_{WS}			3.5	ns
Write Recovery Time	t_{WR}			8	ns
Address Set Up Time	t_{SA}	1			ns
Chip Select Set Up Time	t_{SC}	0			ns
Data Set Up Time	t_{SD}	0			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	0			ns
Data Hold Time	t_{HD}	0			ns

WRITE CYCLE TIMING DIAGRAMS



RISE TIME and FALL TIME

Parameter	Symbol	MBM100470A-7			Unit
		Min	Typ	Max	
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

TYPICAL PERFORMANCE CHARACTERISTICS

FIG. 3 – OUTPUT HIGH VOLTAGE VS AMBIENT TEMPERATURE

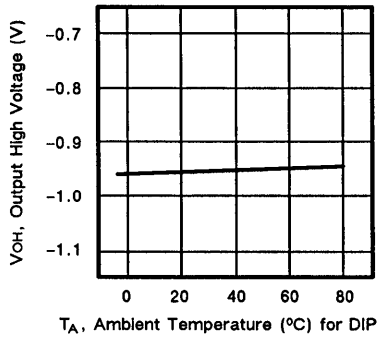


FIG. 4 – OUTPUT HIGH VOLTAGE VS SUPPLY VOLTAGE

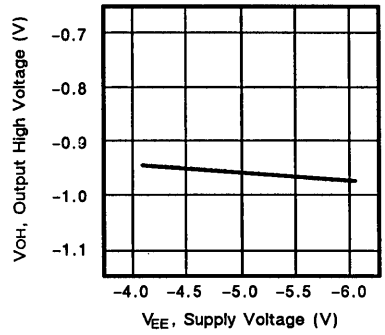


FIG. 5 – OUTPUT LOW VOLTAGE VS AMBIENT TEMPERATURE

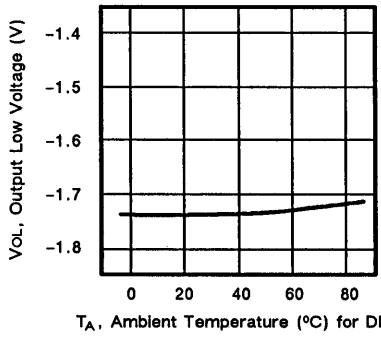


FIG. 6 – OUTPUT LOW VOLTAGE VS SUPPLY VOLTAGE

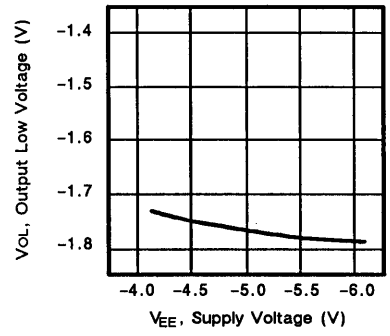
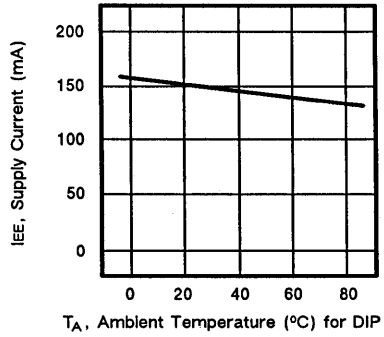


FIG. 7 – SUPPLY CURRENT VS AMBIENT TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS

FIG. 8 – ADDRESS ACCESS TIME VS AMBIENT TEMPERATURE

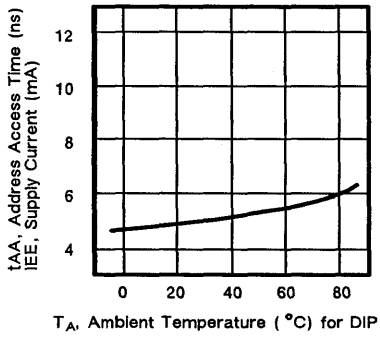


FIG. 9 – ADDRESS ACCESS TIME VS SUPPLY VOLTAGE

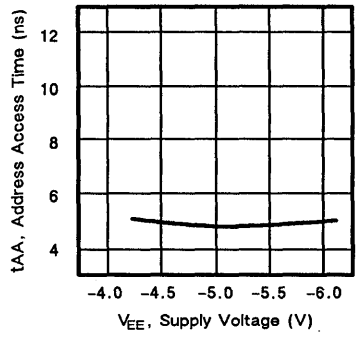


FIG. 10 – WRITE PULSE WIDTH VS AMBIENT TEMPERATURE

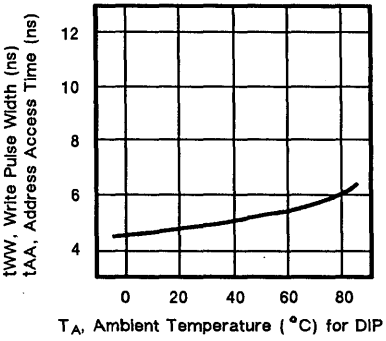
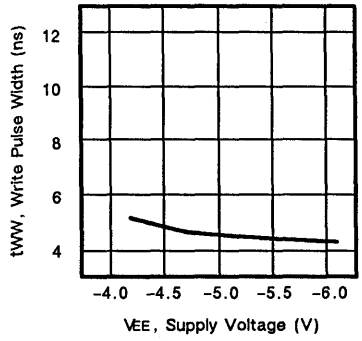
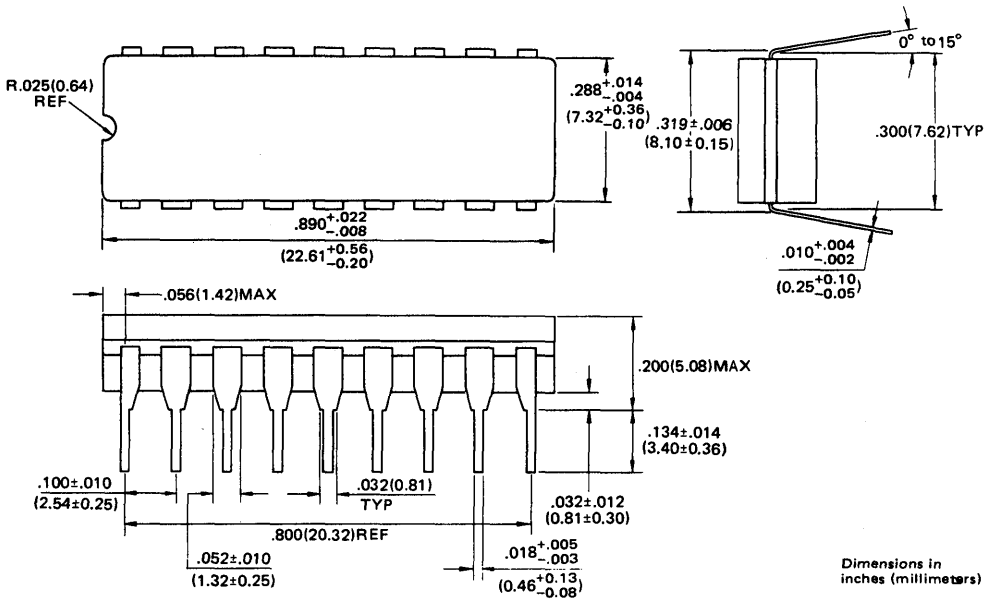


FIG. 11 – WRITE PULSE WIDTH VS SUPPLY VOLTAGE



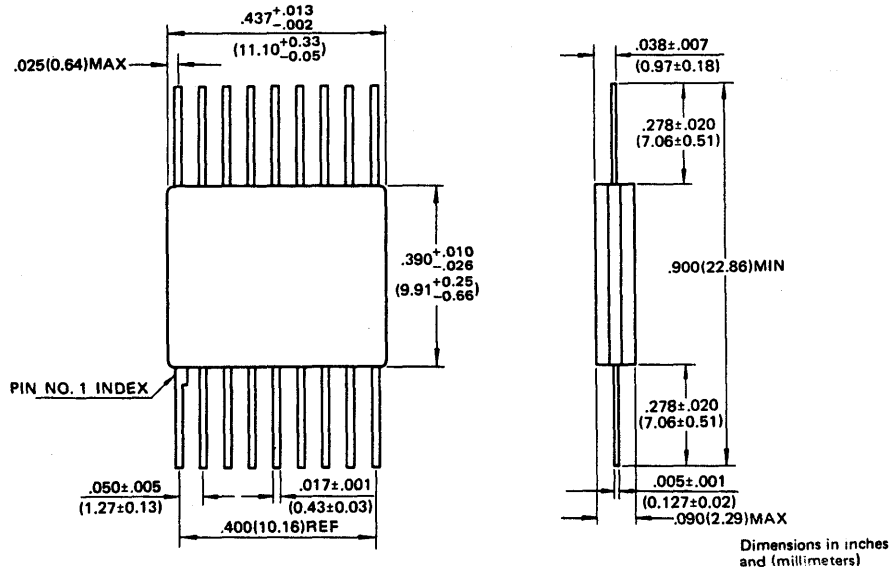
PACKAGE DIMENSIONS

18-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18C-C01)



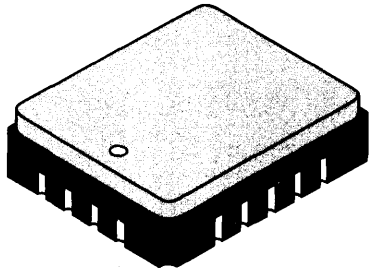
PACKAGE DIMENSIONS (continued)

18-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-18C-C01)



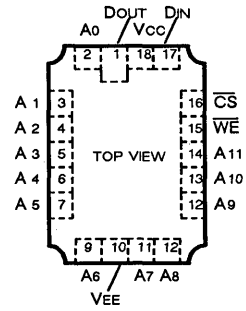
Dimensions in inches
and (millimeters)

PACKAGE DIMENSIONS (continued)

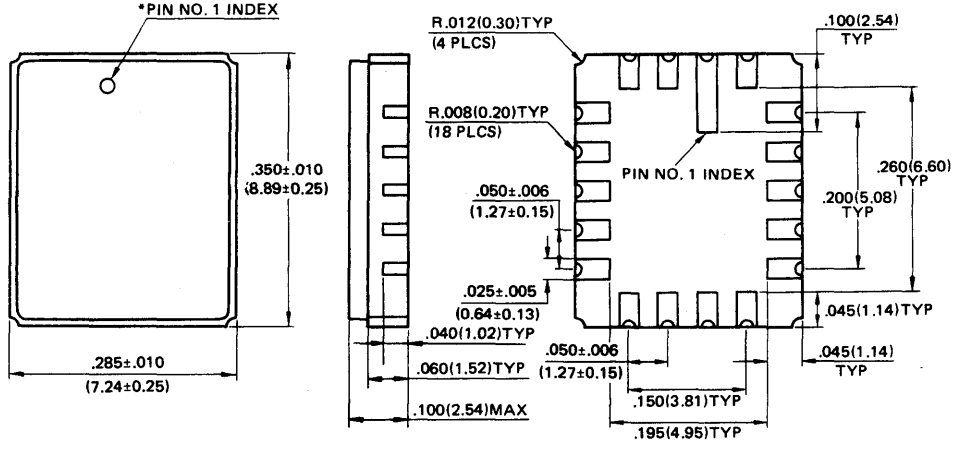


LCC-18C-F01

PAD CONFIGURATION



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F01)



*Shape of Pin 1 index: Subject to change without notice

Dimension in inches
and (millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100470A-10
MBM 100470A-15

July 1984
Edition 2.0

1

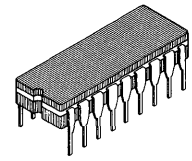
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100470A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

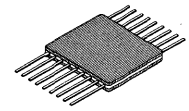
The MBM 100470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100470A is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 18-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 4096 words x 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin.
- Fully compatible with industry-standard 100K-series ECL families
- Address access time: 10 nsec.max. (MBM 100470A-10)
  15 nsec.max. (MBM 100470A-15)
- Chip select access time: 6 nsec.max. (MBM 100470A-10)
  8 nsec.max. (MBM 100470A-15)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.19mW/bit
- DOPOS and IOP-II processing
- Pin compatible with the F100470



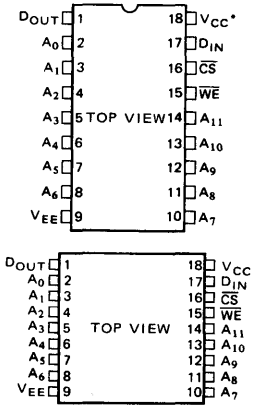
CERAMIC PACKAGE
DIP-18C-C01



CERAMIC PACKAGE
FPT-18C-C01

LCC-18C-F01 : See Page 10

PIN ASSIGNMENT



LCC PAD CONFIGURATION : See Page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

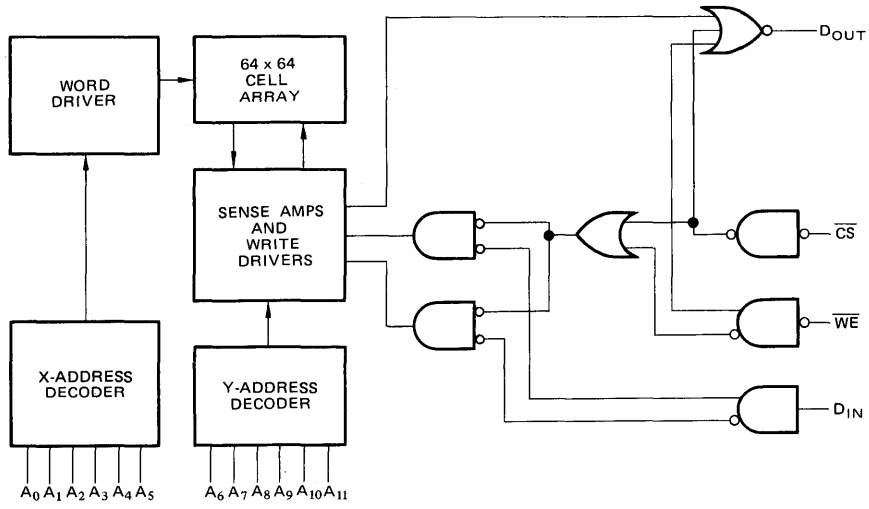
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100470A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100470A is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is proveded for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 85°C for DIP, airflow≧2.5m/s, T_C=0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-200			mA

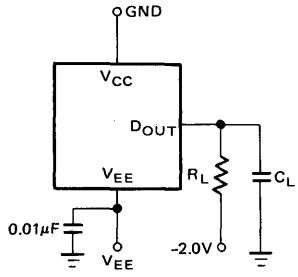
CAPACITANCE

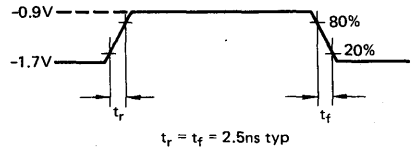
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V ± 5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧2.5m/s T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

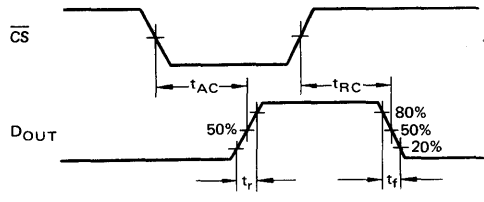
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

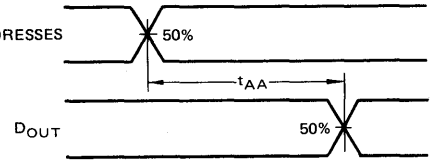
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100470A-10			MBM 100470A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			10			15	ns
Chip Select Access Time	t_{AC}			6			8	ns
Chip Select Recovery Time	t_{RC}			6			8	ns

READ CYCLE TIMING DIAGRAMS

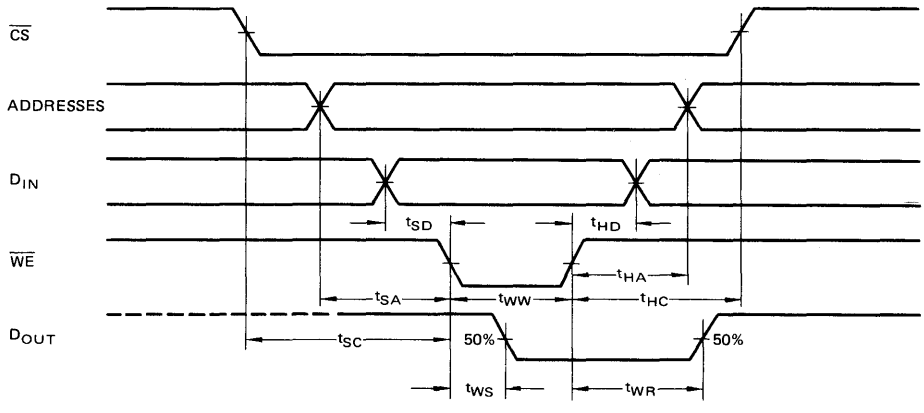




WRITE CYCLE

Parameter	Symbol	MBM 100470A-10			MBM 100470A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	12			15			ns
Write Disable Time	t_{WS}			6			8	ns
Write Recovery Time	t_{WR}			12			12	ns
Address Set Up Time	t_{SA}	1			1			ns
Chip Select Set Up Time	t_{SC}	1			1			ns
Data Set Up Time	t_{SD}	1			1			ns
Address Hold Time	t_{HA}	2			2			ns
Chip Select Hold Time	t_{HC}	2			2			ns
Data Hold Time	t_{HD}	2			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

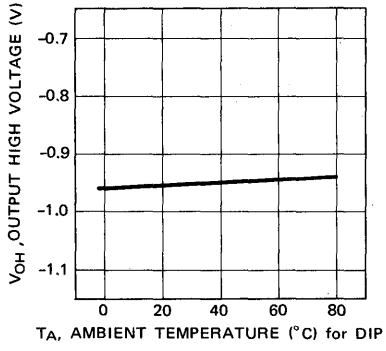


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

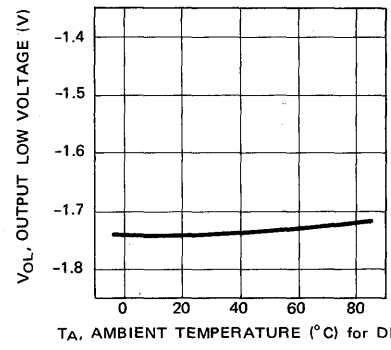


Fig. 5 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

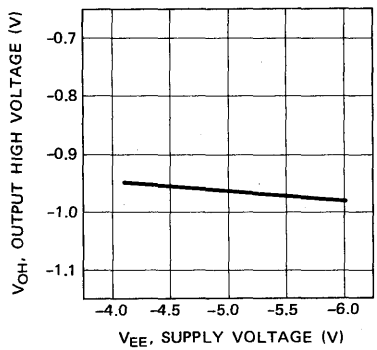


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

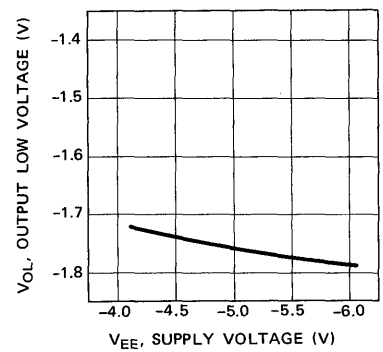


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

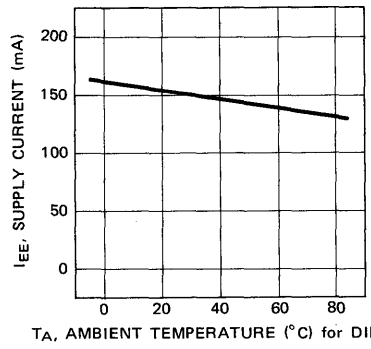


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

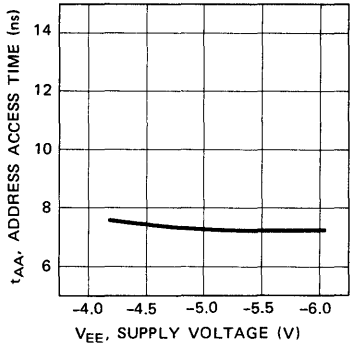


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

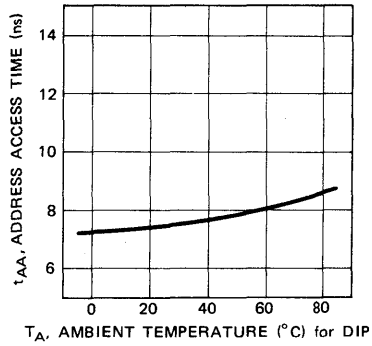


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

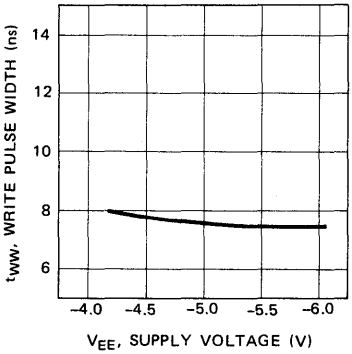
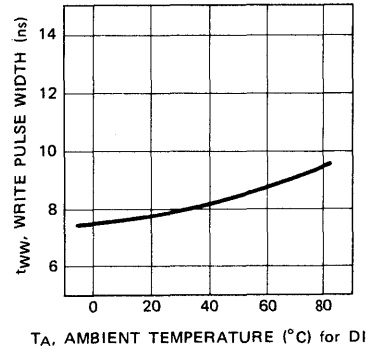


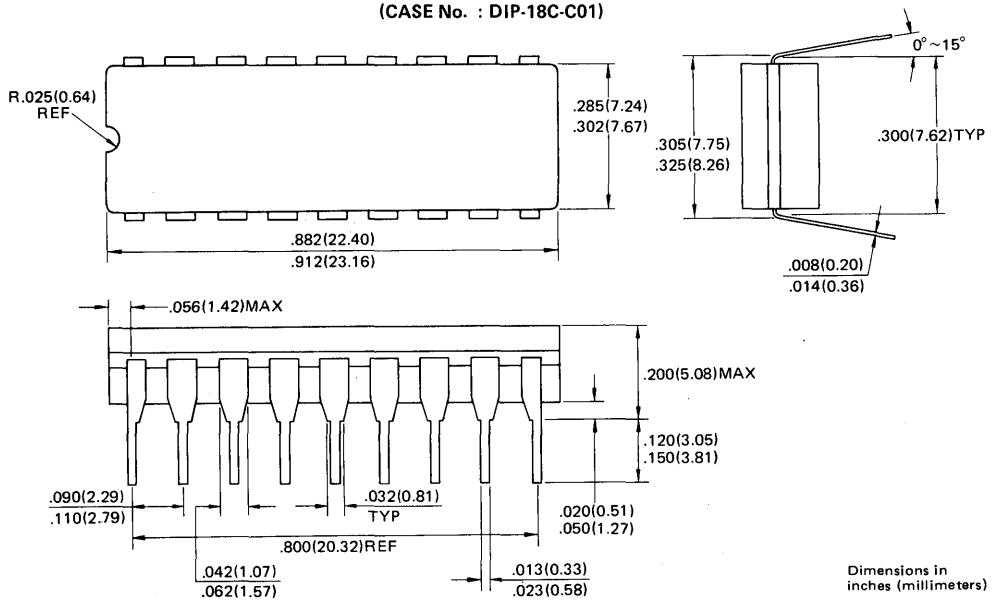
Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



1

PACKAGE DIMENSIONS

18-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-18C-C01)

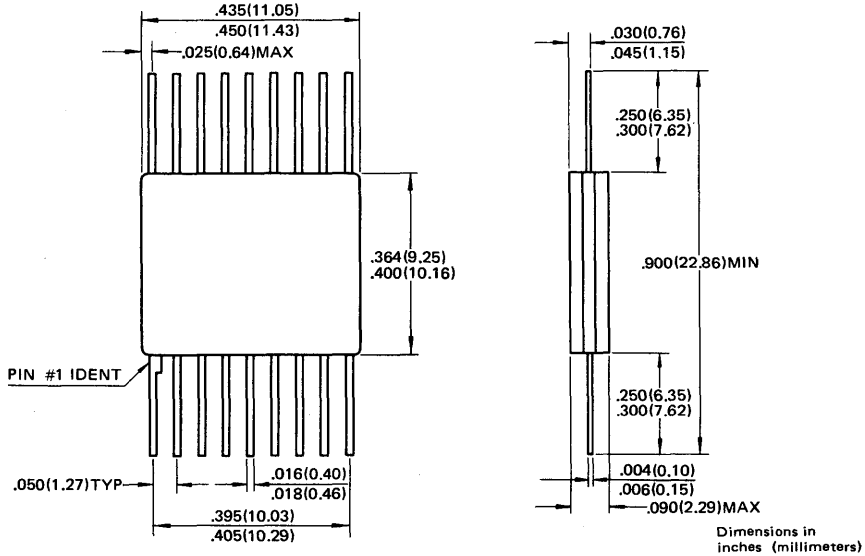


Dimensions in
inches (millimeters)

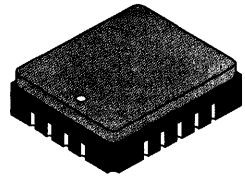
1

PACKAGE DIMENSIONS

18-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No. : FPT-18C-C01)

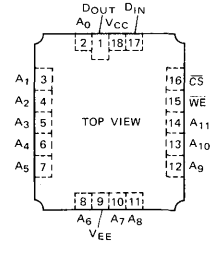


PACKAGE DIMENSIONS

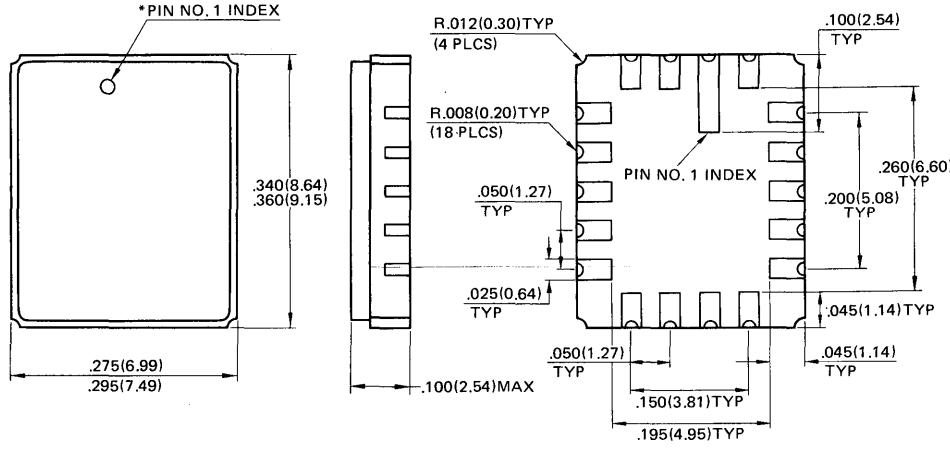


LCC-18C-F01

PAD ASSIGNMENT



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE NO.: LCC-18C-F01)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10A474-3

TARGET SPECIFICATION

TS315-A87Y
November 1987

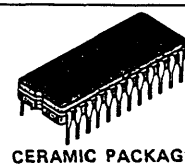
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10A474 is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. The device is organized as 1024 words by 4 bits, and it features on chip voltage compensation for improved noise margin.

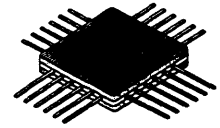
The MBM10A474 offers extremely small cell and chip size. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume productuion.

Operation for the MBM10A474 is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package). It also features 24-pin Ceramic DIP or Flat Package and is fully compatible with industry standard 10K-series ECL families.

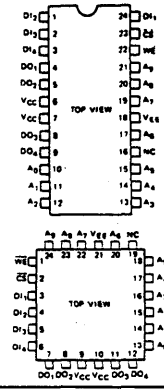
- 1024 words x 4 bit organization
- On-chip voltage compensation for improved noise margin.
- Fully compatible with industory standard 10K series ECL families
- Address access time: 3ns max
  Chip select access time: 2ns max
- Open emitter output for ease of memory expansion



CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02
PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	TA for DIP TC for FPT	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

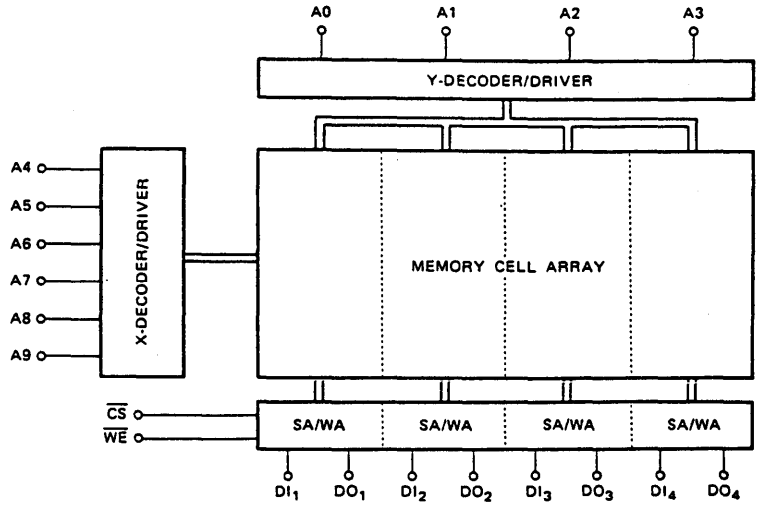
Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device dmage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TARGET SPECIFICATION

1

Fig.1 - MBM10A474 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10A474 is fully decoded 4096 bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designed A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection

TARGET SPECIFICATION

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flatpackage
Supply Voltage	V_{EE}	-5.46	-4.5	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC=0V, VEE=-5.2V, Output Load = 50Ω to -2.0V, TA = 0°C to 75°C, Airflow ≥ 2.5 m/s unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TA
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°Cto75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°Cto75°C
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA	0°Cto75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-300			mA	0°Cto75°C

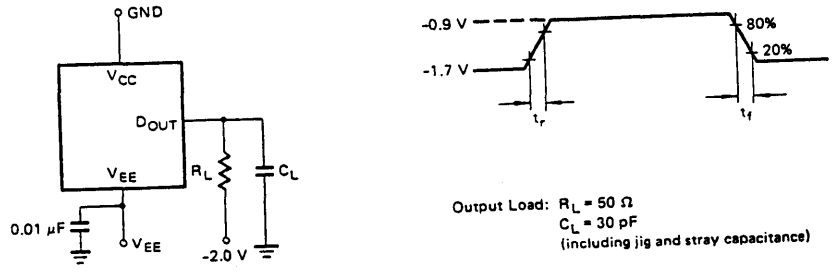
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capacitance	C_{OUT}		5	6	pF

AC CHARACTERISTICS

(VCC=0V, VEE=-5.2V±5%, Output Load=50Ω to -2.0V and 30pF to GND, TA = 0°C to 75°C for DIP, Airflow ≥ 2.5m/s, TC = 0°C to 75°C for Flatpackage, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



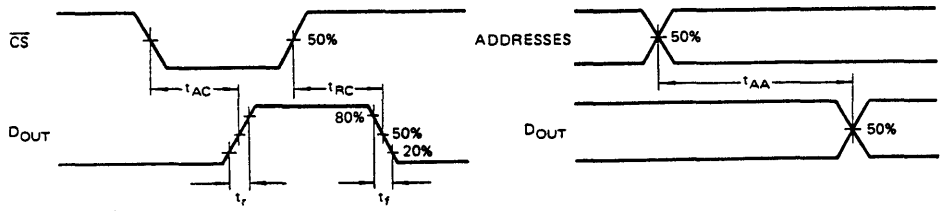
Output Load: R_L = 50 Ω
C_L = 30 pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			3	ns
Chip Select Access Time	t_{AC}			2	ns
Chip Select Recovery Time	t_{RC}			2	ns

READ CYCLE TIMING DIAGRAM

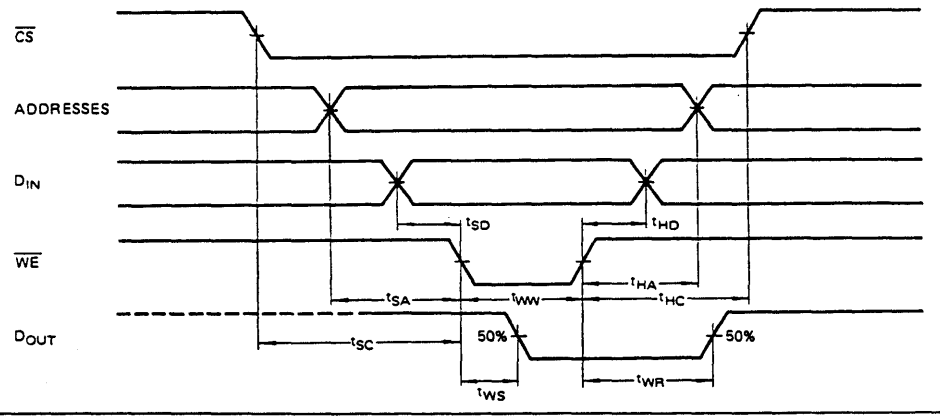


TARGET SPECIFICATION

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	TBD			ns
Write Disable Time	t_{WS}			TBD	ns
Write Recovery Time	t_{WR}			TBD	ns
Address Set Up Time	t_{SA}	1			ns
Chip Select Set Up Time	t_{SC}	0			ns
Data Set Up Time	t_{SD}	0			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

1

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100474A-3

TS316-A87Y
NOvember 1987

TARGET SPECIFICATION

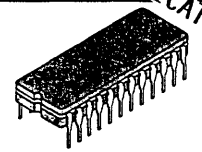
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. The device is organized as 1024 words by 4 bits, and it features on chip voltage / temperature compensation for improved noise margin.

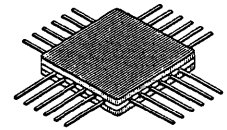
The MBM100474A offers extremely small cell and chip size. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume productuion.

Operation for the MBM100474A is specified over a temperature range of from 0°C to 85°C (T_A for DIP; T_C for Flat Package). It also features 24-pin Ceramic DIP or Flat Package and is fully compatible with industry standard 100K-series ECL families.

- 1024 words x 4 bit organization
- On-chip voltage/temperature compensation for improved noise margin.
- Fully compatible with industory standard 100K series ECL families
- Address access time: 3ns max
  Chip select access time: 2ns max
- Open emitter output for ease of memory expansion

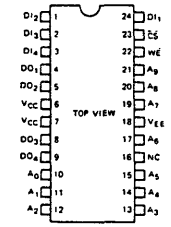


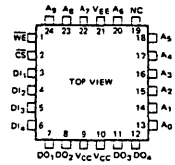
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	TA for DIP TC for FPT	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

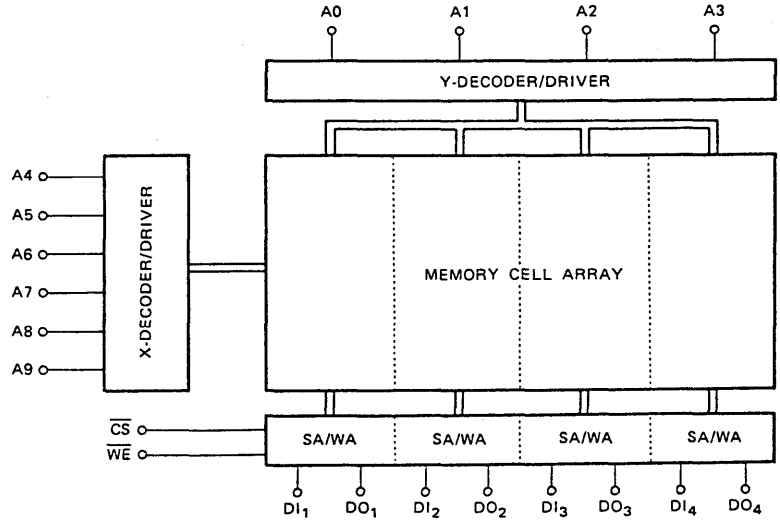
Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device dmage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TARGET SPECIFICATION

1

Fig.1 - MBM100474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100474A is fully decoded 4096 bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designed A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection

TARGET SPECIFICATION

1

GUARANTEED OPERATING CONDITIONS
(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flatpackage
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS
(VCC=0V, VEE=-4.5V, Output Load = 50Ω to -2.0V, TA = 0°C to 85°C for DIP, Airflow ≥ 2.5m/s, TC = 0°C to 85°C for Flatpackage, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810		-1620	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mA
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (VIN = VIH max)	I_{IH}			220	µA
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-300			mA

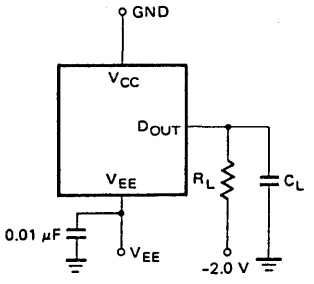
CAPACITANCE

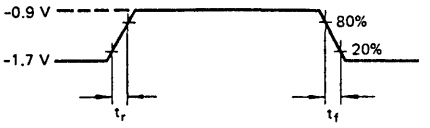
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capacitance	C_{OUT}		5	6	pF

AC CHARACTERISTICS

(VCC=0V, VEE=-4.5V±5%, Output Load=50Ω to -2.0V and 30pF to GND, TA = 0°C to 85°C for DIP, Airflow ≥ 2.5m/s, TC = 0°C to 85°C for Flatpackage, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





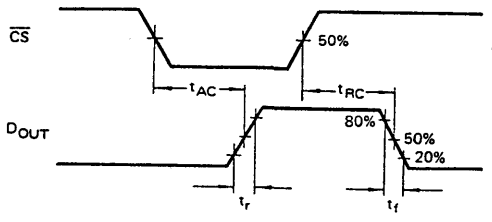
Output Load: R_L = 50 Ω
C_L = 30 pF
(including jig and stray capacitance)

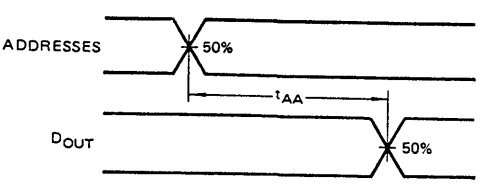
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			3	ns
Chip Select Access Time	t_{AC}			2	ns
Chip Select Recovery Time	t_{RC}			2	ns

READ CYCLE TIMING DIAGRAM





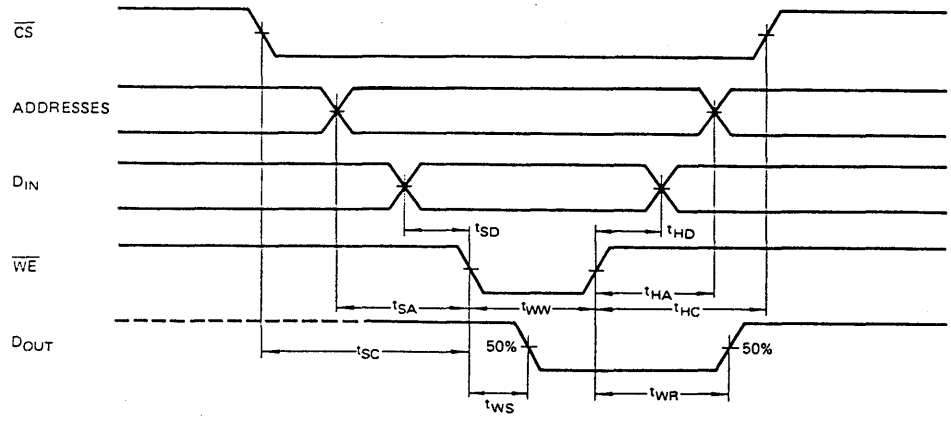
TARGET SPECIFICATION

1

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	TBD			ns
Write Disable Time	t_{WS}			TBD	ns
Write Recovery Time	t_{WR}			TBD	ns
Address Set Up Time	t_{SA}	1			ns
Chip Select Set Up Time	t_{SC}	0			ns
Data Set Up Time	t_{SD}	0			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



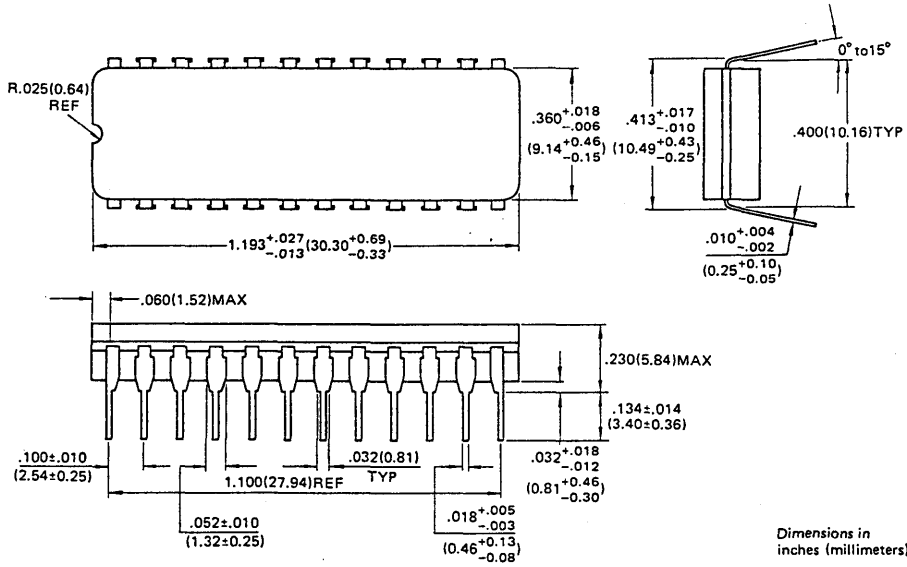
RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

TARGET SPECIFICATION

PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE NO.: DIP-24C-C05)

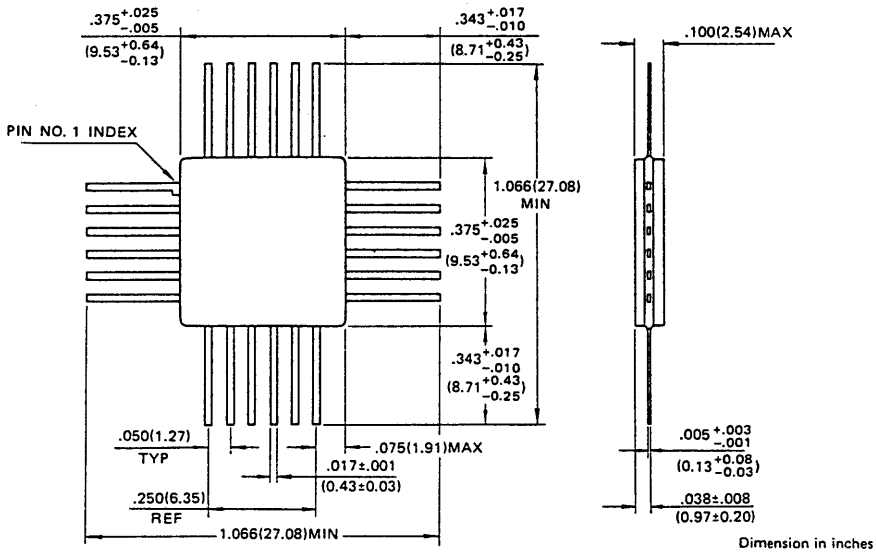


Dimensions in inches (millimeters)

TARGET SPECIFICATION

PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE NO.: FPT-24C-C02)



Dimension in inches
and (millimeters)

1

1

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10474A-5
MBM 10474A-7

June 1987
Edition 1.0

1

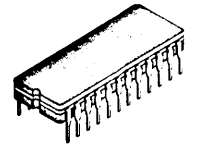
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

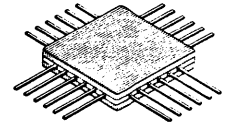
The MBM 10474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as U-Fox (U-groove isolation with thick field oxide) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10474A is specified over a temperature range of from 0° to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 5 ns max. (MBM 10474A-5)
  7 ns max. (MBM 10474A-7)
- Chip select access time: 3 ns max. (MBM 10474A-5)
  5 ns max. (MBM 10474A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.33 mW/bit typ. (MBM 10474A-5)
  0.24 mW/bit typ. (MBM 10474A-7)
- DOPOS and U-Fox processing
- Pin compatible with the F10474



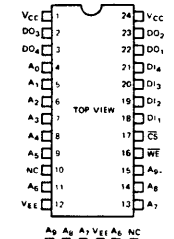
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See page 10

PIN ASSIGNMENT



V_{CC} grounded
LCC PAD CONFIGURATION : See page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

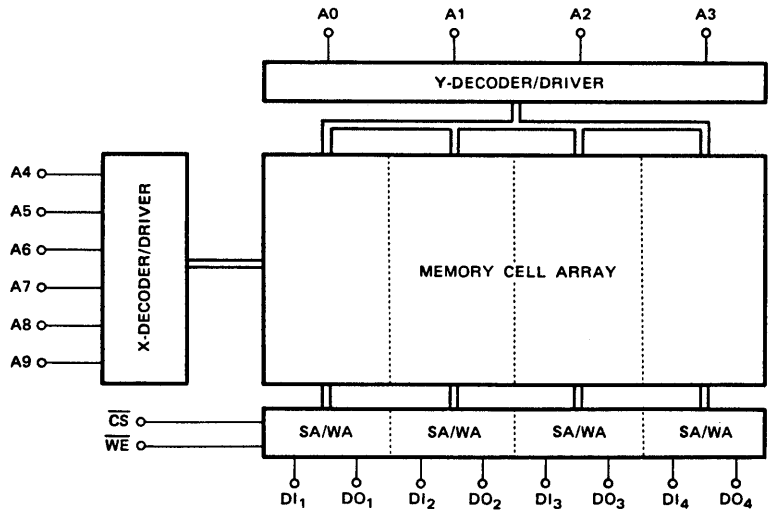
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 10474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10474A is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0° C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open) MBM 10474A-5	I_{EE}	-300			mA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open) MBM 10474A-7	I_{EE}	-220			mA	0°C to 75°C

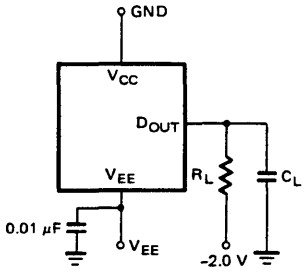
CAPACITANCE

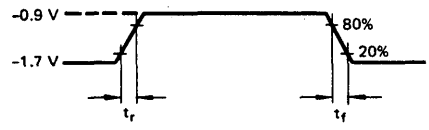
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capcitance	C_{OUT}		5	6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −5.2 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





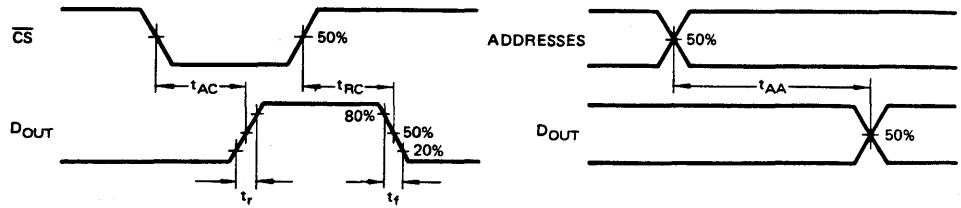
Output Load: R_L = 50 Ω
C_L = 30 pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10474A-5			MBM 10474A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	1.2		5	1.2		7	ns
Chip Select Access Time	t_{AC}	0.5		3	0.5		5	ns
Chip Select Recovery Time	t_{RC}	0.5		3	0.5		5	ns

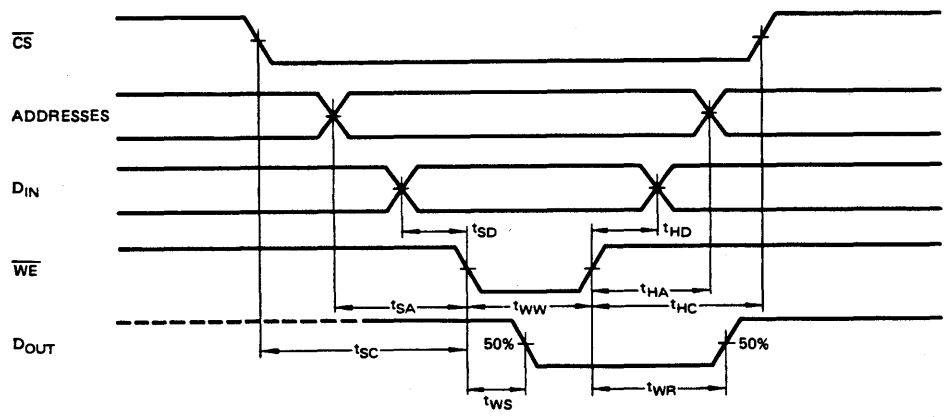
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10474A-5			MBM 10474A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	8			5			ns
Write Disable Time	t_{WS}	0.3		3	0.3		6.5	ns
Write Recovery Time	t_{WR}	0.5		7	0.5		8	ns
Address Set Up Time	t_{SA}	1			1			ns
Chip Select Set Up Time	t_{SC}	0			0			ns
Data Set Up Time	t_{SD}	0			0			ns
Address Hold Time	t_{HA}	1			1			ns
Chip Select Hold Time	t_{HC}	1			1			ns
Data Hold Time	t_{HD}	1			1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

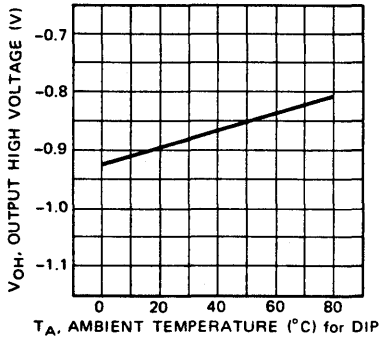


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

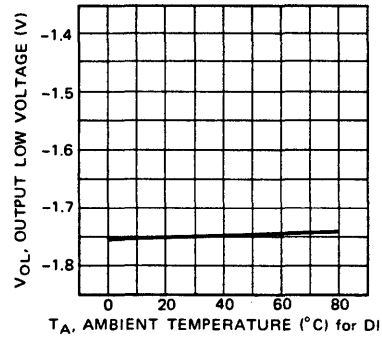


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

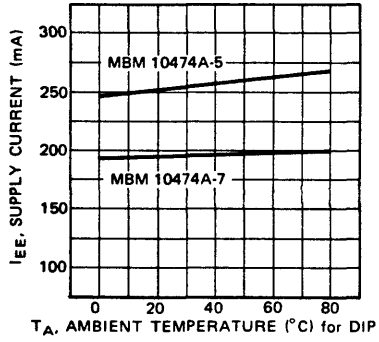


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

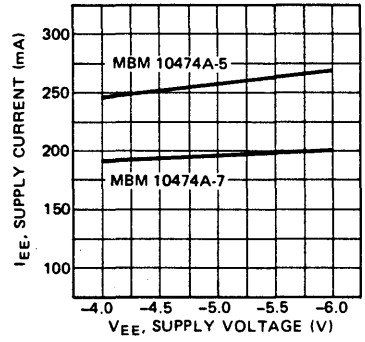


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

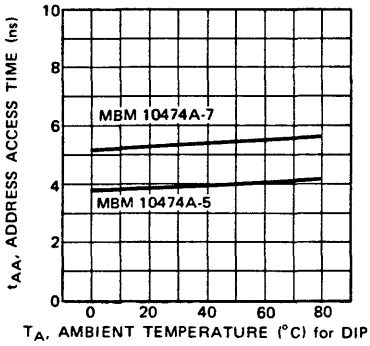


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

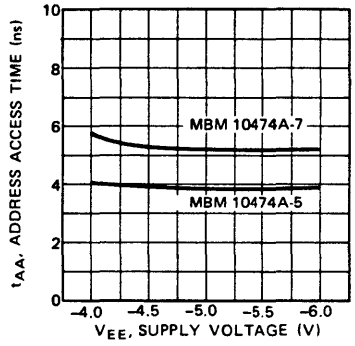


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

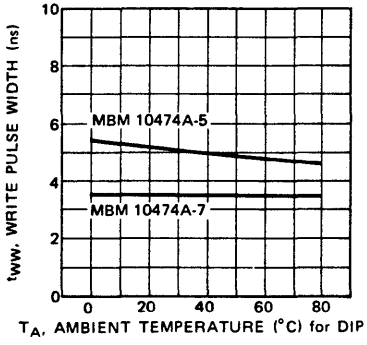
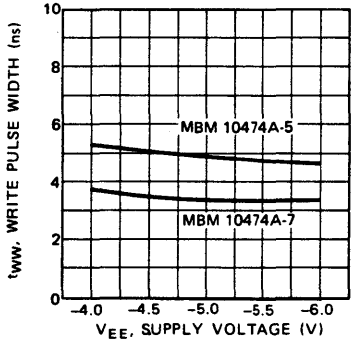
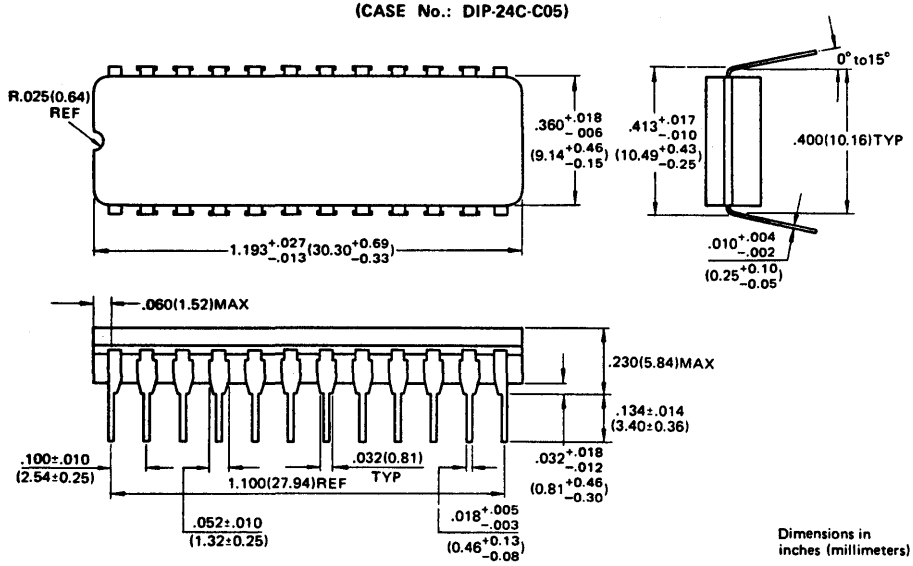


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



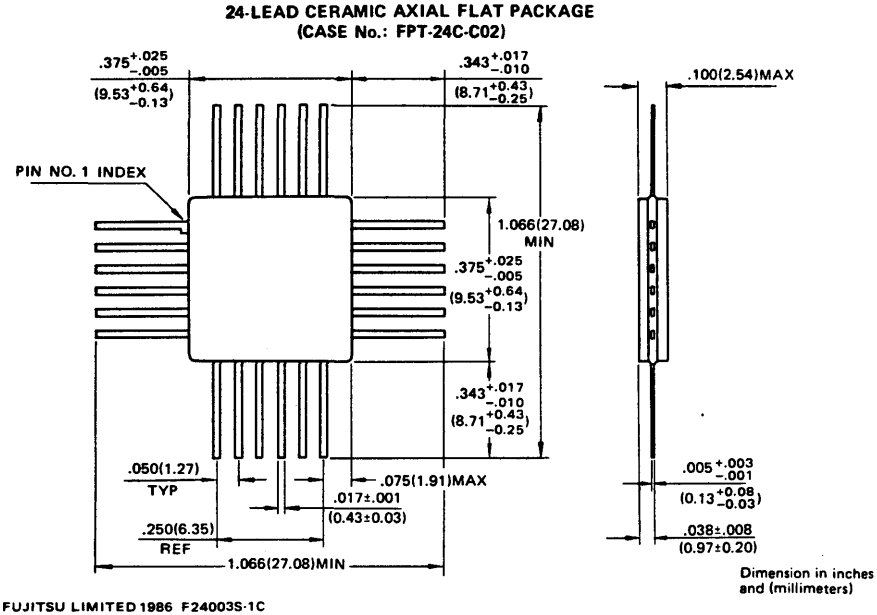
PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)

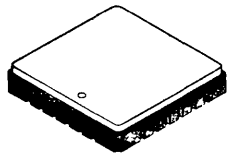


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

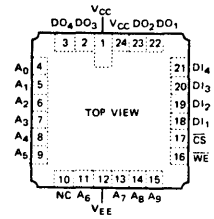


PACKAGE DIMENSIONS

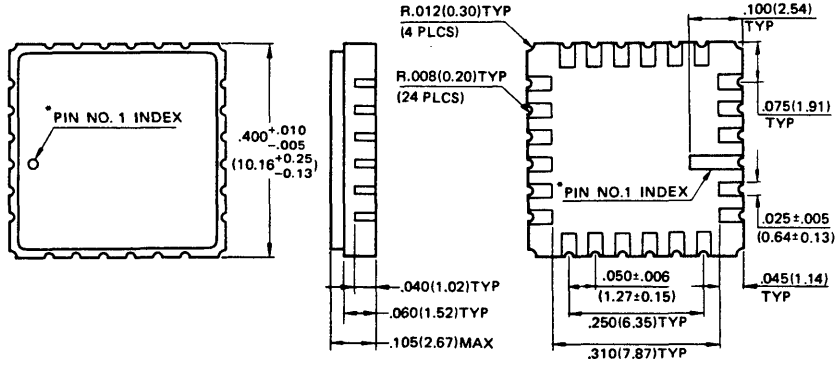


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10474A-10
MBM 10474A-15

August 1985
Edition 2.0

1

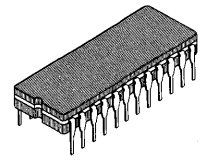
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

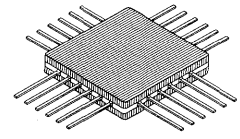
The MBM 10474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10474A is specified over a temperature range of from 0° to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 10 ns max. (MBM 10474A-10)
  15 ns max. (MBM 10474A-15)
- Chip select access time: 6 ns max. (MBM 10474A-10)
  8 ns max. (MBM 10474A-15)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.26 mW/bit typ. (MBM 10474A-10)
  0.20 mW/bit typ. (MBM 10474A-15)
- DOPOS and IOP-II processing
- Pin compatible with the F10474



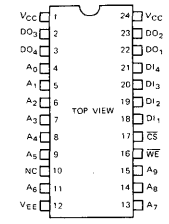
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See page 10

PIN ASSIGNMENT



V_{CC} grounded

LCC PAD CONFIGURATION : See page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

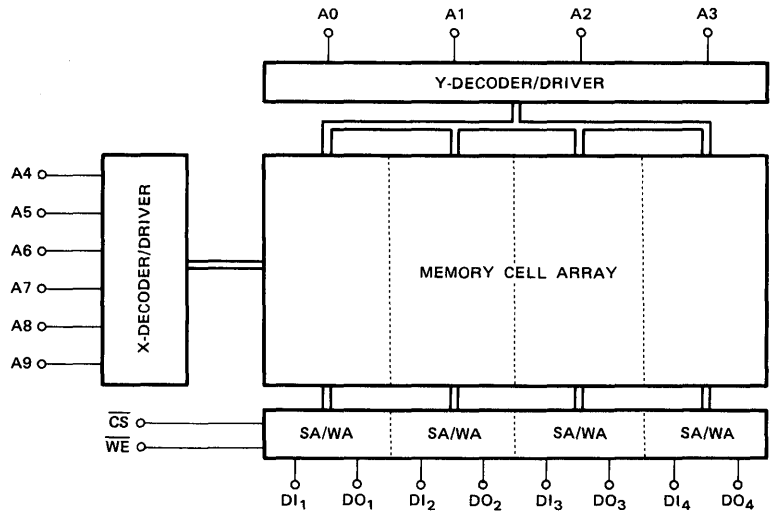
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 10474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10474A is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0° C to 75°C

1

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open) MBM 10474A-10	I_{EE}	-230			mA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open) MBM 10474A-15	I_{EE}	-200			mA	0°C to 75°C

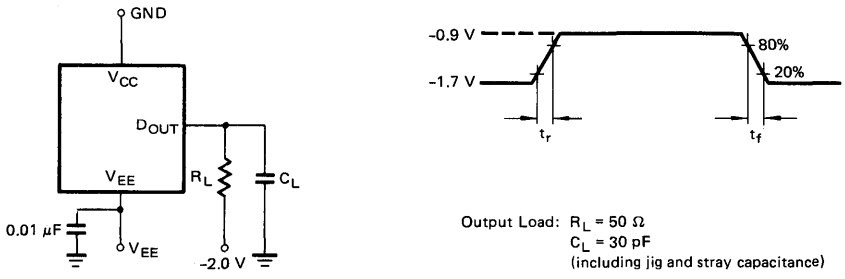
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capcitance	C_{OUT}		6	8	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −5.2 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS

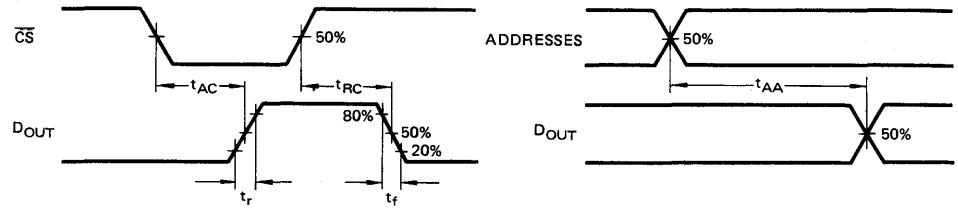


NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10474A-10			MBM 10474A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	2	7	10	3	10	15	ns
Chip Select Access Time	t_{AC}	1.5	3	6	2	4	8	ns
Chip Select Recovery Time	t_{RC}	1.5	3	6	2	4	8	ns

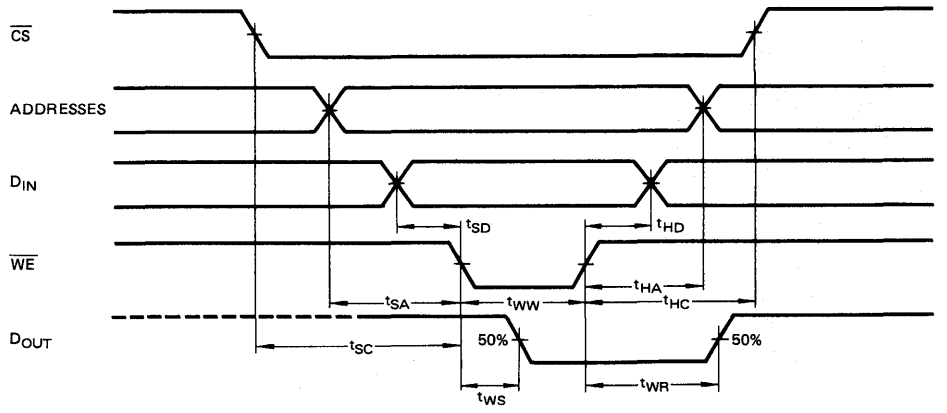
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10474A-10			MBM 10474A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	12			15			ns
Write Disable Time	t_{WS}			6			8	ns
Write Recovery Time	t_{WR}			10			15	ns
Address Set Up Time	t_{SA}	2			2			ns
Chip Select Set Up Time	t_{SC}	1			2			ns
Data Set Up Time	t_{SD}	1			2			ns
Address Hold Time	t_{HA}	1			3			ns
Chip Select Hold Time	t_{HC}	1			2			ns
Data Hold Time	t_{HD}	1			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	1		3.5	ns
Output Fall Time	t_f	1		3.5	ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

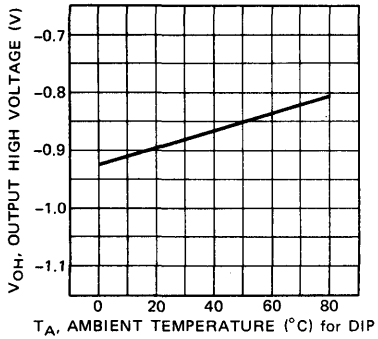


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

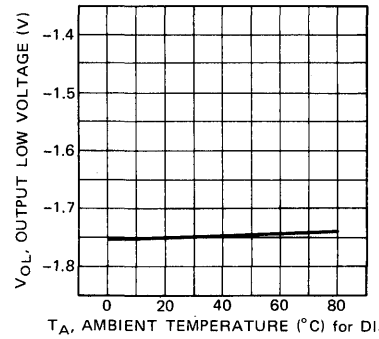


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

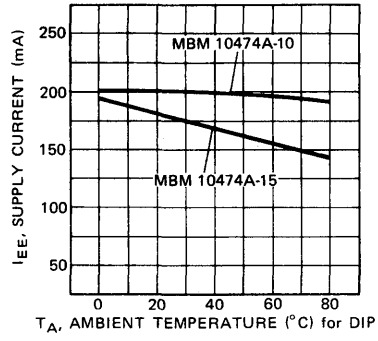


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

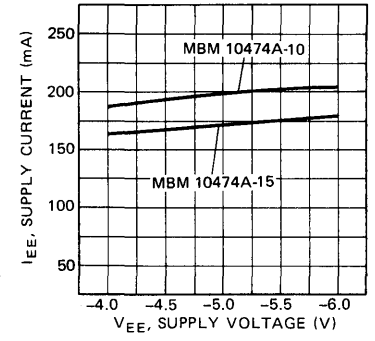


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

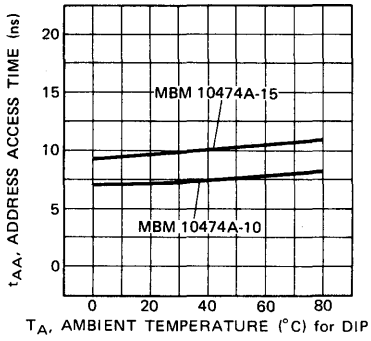


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

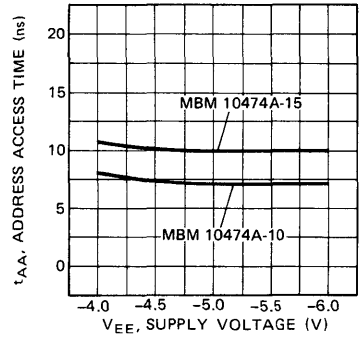


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

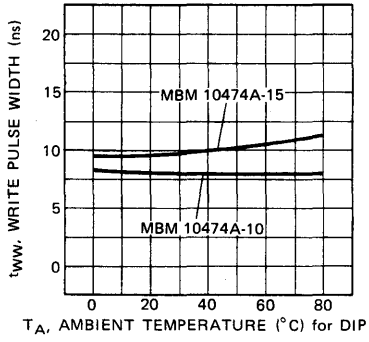
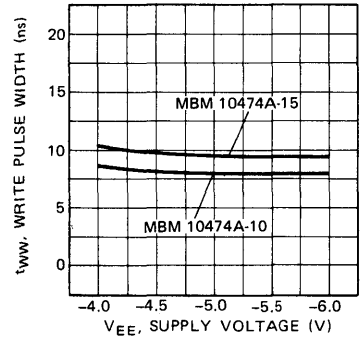


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



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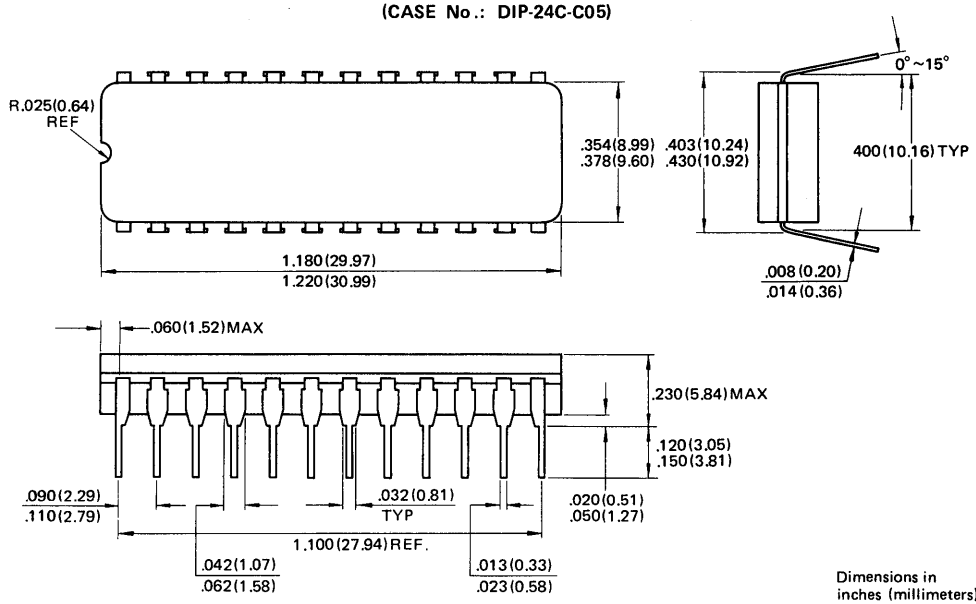
PACKAGE DIMENSIONS

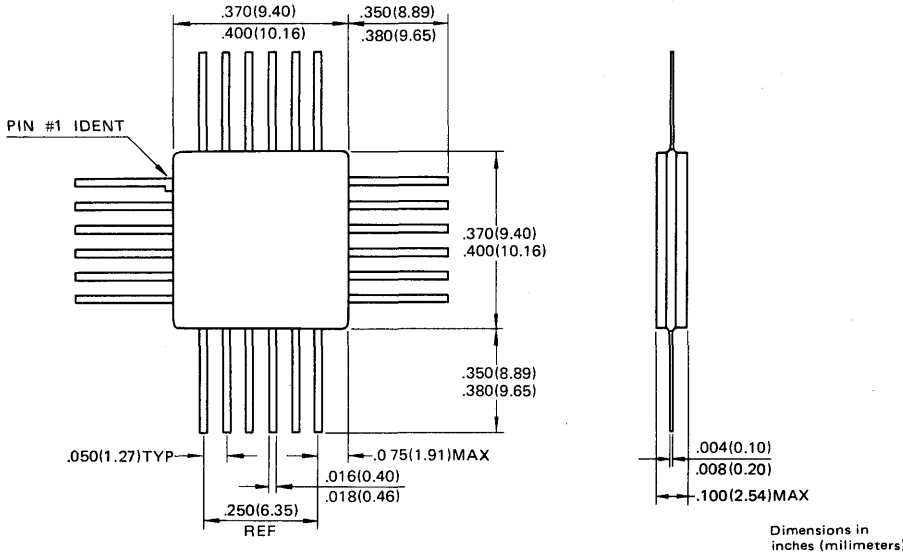
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



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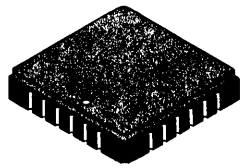
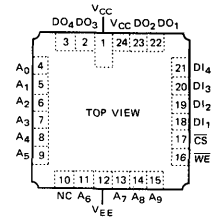
PACKAGE DIMENSIONS

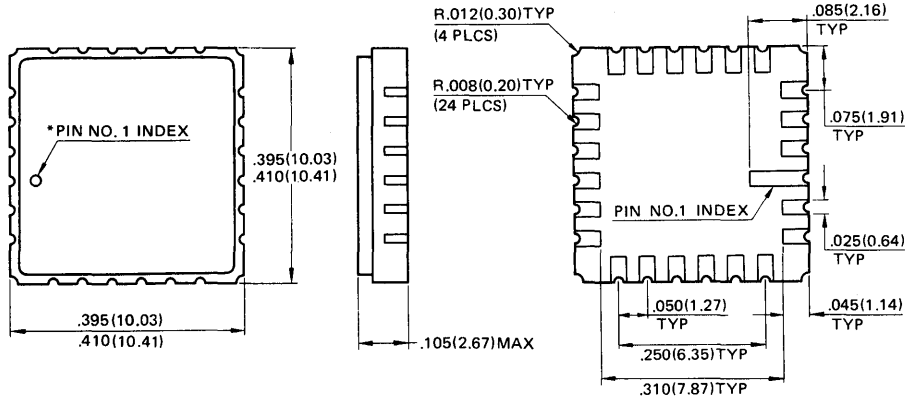


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100474A-5
MBM 100474A-7

June 1987
Edition 1.0

4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

The MBM 100474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as U-Fox (U-groove isolation with thick field oxide) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

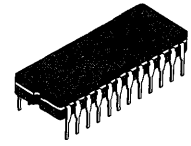
Operation for the MBM 100474A is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat package, or LCC. It is fully compatible with industry-standard 100 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 5 ns max. (MBM 100474A-5)
  7 ns max. (MBM 100474A-7)
- Chip select access time: 3 ns max. (MBM 100474A-5)
  5 ns max. (MBM 100474A-7)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.28 mW/bit typ. (MBM 100474A-5)
  0.20 mW/bit typ. (MBM 100474A-7)
- DOPOS and U-Fox processing
- Pin compatible with the F100474

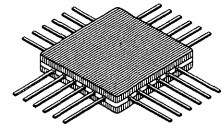
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.



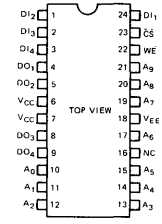
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See page 10

PIN ASSIGNMENT



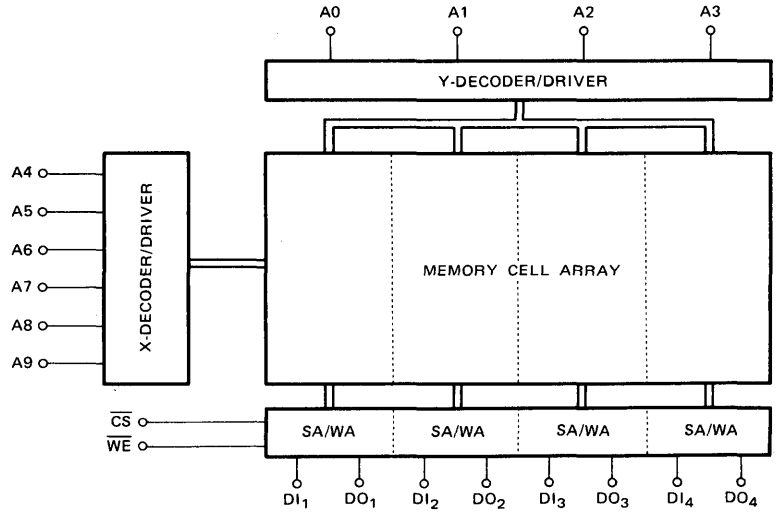
V_{CC} grounded

LCC PAD CONFIGURATION : See page 10

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100474A is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designed A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC.
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

1

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50Ω to -2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	-1810		-1620	mV
Output High Voltage ($V_{IN\ min}$ or $V_{IL\ max}$)		V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)		V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage for All Inputs)		V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)		I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power Supply Current (All inputs and Outputs Open)	MBM 100474A-5	I_{EE}	-300			mA
	MBM 100474A-7		-220			

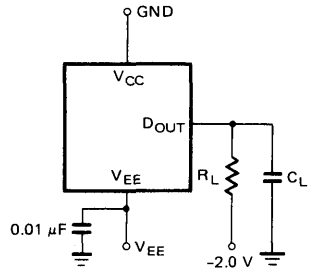
CAPACITANCE

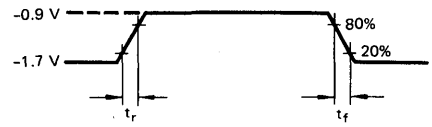
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capacitance	C_{OUT}		5	6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −4.5 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





$t_r = t_f$ = 2.5 ns typ

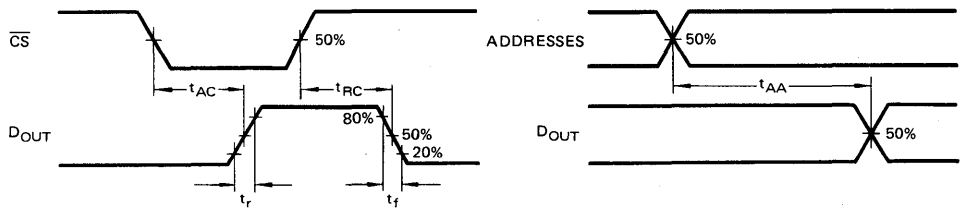
Output Load: R_L = 50 Ω
C_L = 30 pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100474A-5			MBM 100474A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	1.2		5	1.2		7	ns
Chip Select Access Time	t_{AC}	0.5		3	0.5		5	ns
Chip Select Recovery Time	t_{RC}	0.5		3	0.5		5	ns

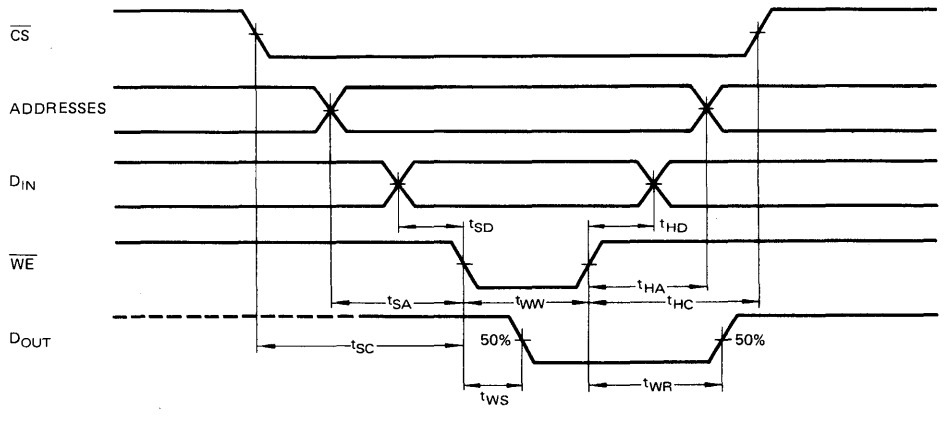
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 100474A-5			MBM 100474A-7			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	8			5			ns
Write Disable Time	t_{WS}	0.3		3	0.3		6.5	ns
Write Recovery Time	t_{WR}	0.5		7	0.5		8	ns
Address Set Up Time	t_{SA}	1			1			ns
Chip Select Set Up Time	t_{SC}	0			0			ns
Data Set Up Time	t_{SD}	0			0			ns
Address Hold Time	t_{HA}	1			1			ns
Chip Select Hold Time	t_{HC}	1			1			ns
Data Hold Time	t_{HD}	1			1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

1

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

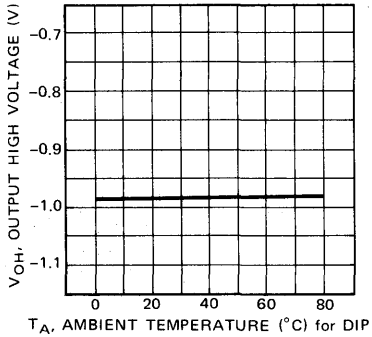


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

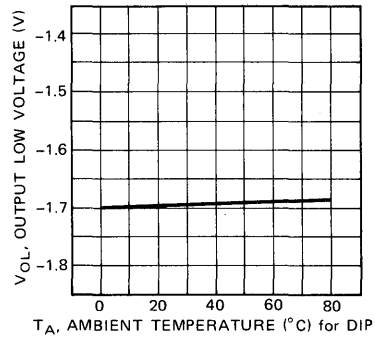


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

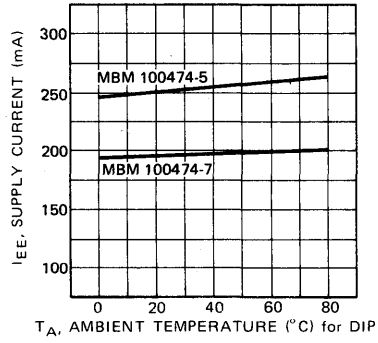


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

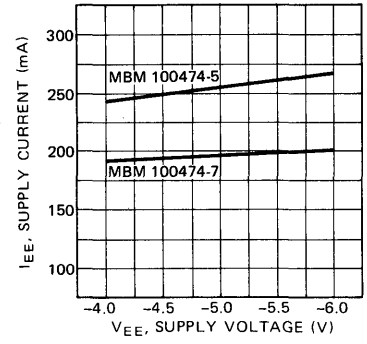


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

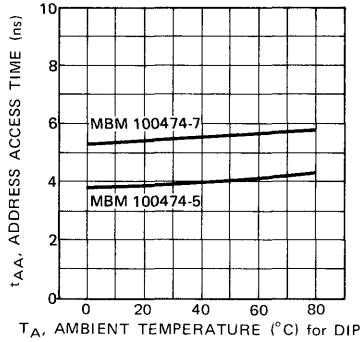


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

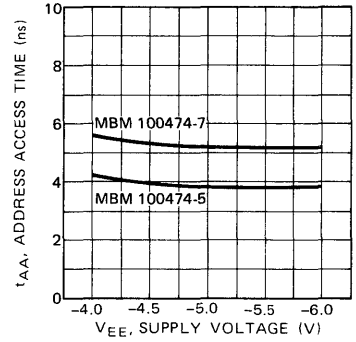


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

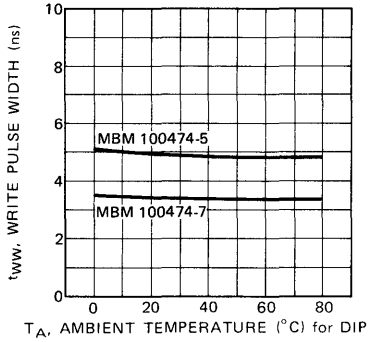
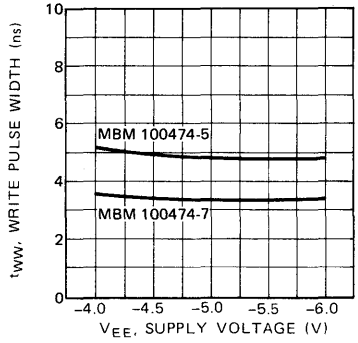


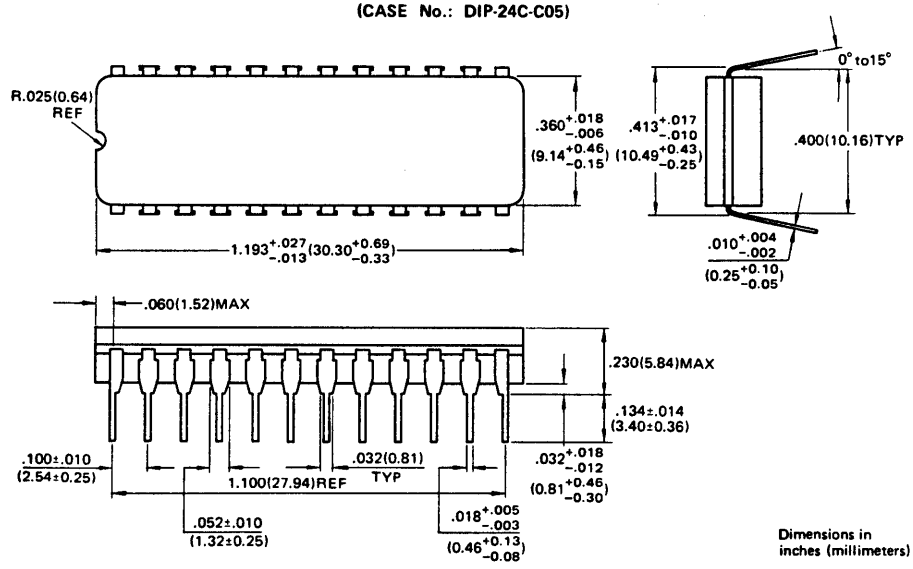
Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

(Suffix: -CZ)

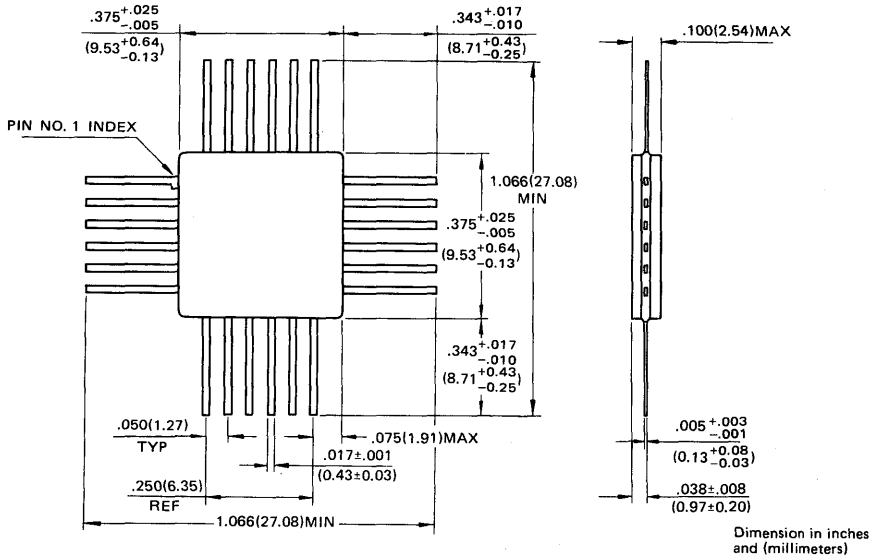
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



PACKAGE DIMENSIONS

(Suffix: -ZF)

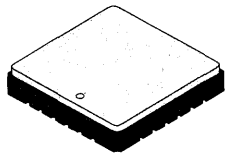
24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



Dimension in inches
and (millimeters)

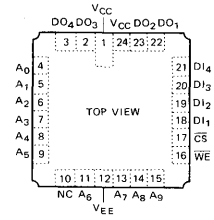
PACKAGE DIMENSIONS

(Suffix: -TV)

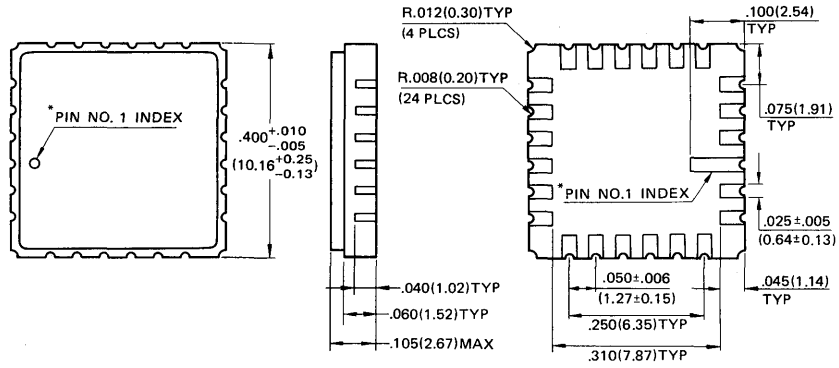


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

FUJITSU

ECL 4096-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100474A-10
MBM 100474A-15

August 1985
Edition 2.0

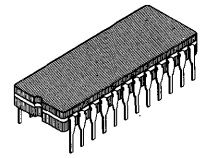
4096-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100474A is fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

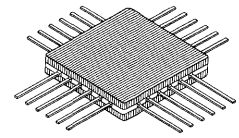
The MBM 100474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100474A is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin DIP, Flat package, or LCC. It is fully compatible with industry-standard 100 K-series ECL families.

- 1024 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 10 ns max. (MBM 100474A-10)
  15 ns max. (MBM 100474A-15)
- Chip select access time: 6 ns max. (MBM 100474A-10)
  8 ns max. (MBM 100474A-15)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.22 mW/bit typ. (MBM 100474A-10)
  0.20 mW/bit typ. (MBM 100474A-15)
- DOPOS and IOP-II processing
- Pin compatible with the F 100474



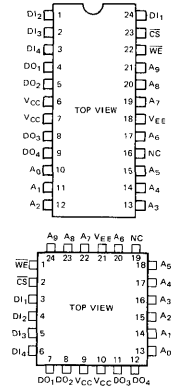
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See page 10

PIN ASSIGNMENT



V_{CC} grounded

LCC PAD CONFIGURATION : See page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

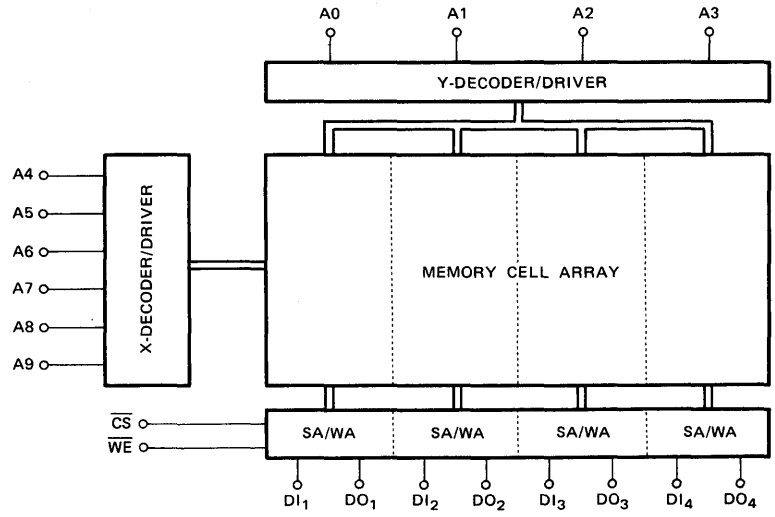
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100474A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100474A is fully decoded 4096-bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designed A_0 through A_9. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC.
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

1

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50Ω to -2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	-1810		-1620	mV
Output High Voltage ($V_{IN\ min}$ or $V_{IL\ max}$)		V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)		V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage for All Inputs)		V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)		I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power Supply Current (All inputs and Outputs Open)	MBM 100474A-10	I_{EE}	-230			mA
	MBM 100474A-15		-200			

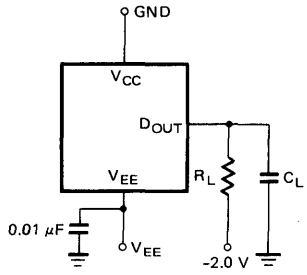
CAPACITANCE

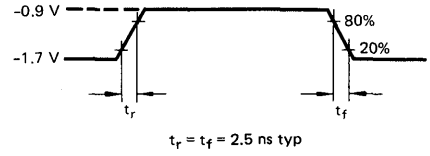
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	5	pF
Output Pin Capacitance	C_{OUT}		6	8	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −4.5 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





$t_r = t_f$ = 2.5 ns typ

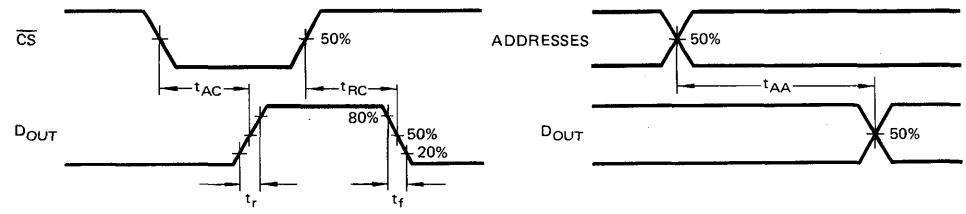
Output Load: R_L = 50 Ω
C_L = 30 pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100474A-10			MBM 100474A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}	2	7	10	3	10	15	ns
Chip Select Access Time	t_{AC}	1.5	3	6	2	4	8	ns
Chip Select Recovery Time	t_{RC}	1.5	3	6	2	4	8	ns

READ CYCLE TIMING DIAGRAMS

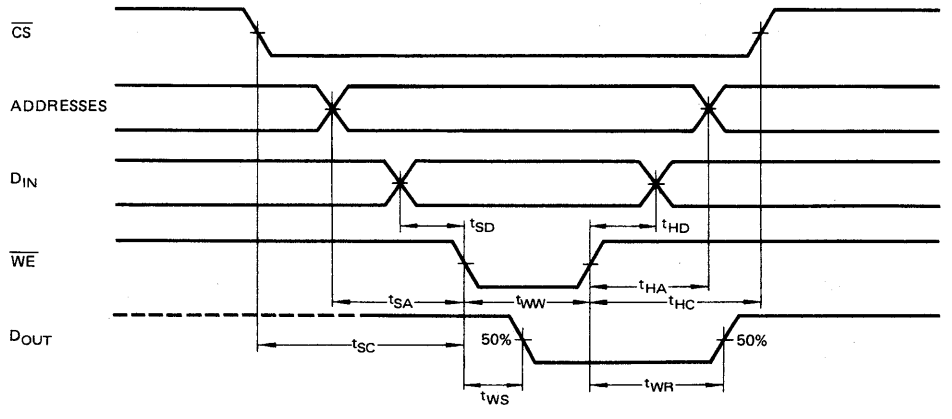


1

WRITE CYCLE

Parameter	Symbol	MBM 100474A-10			MBM 100474A-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	12			15			ns
Write Disable Time	t_{WS}			6			8	ns
Write Recovery Time	t_{WR}			10			15	ns
Address Set Up Time	t_{SA}	2			2			ns
Chip Select Set Up Time	t_{SC}	1			2			ns
Data Set Up Time	t_{SD}	1			2			ns
Address Hold Time	t_{HA}	1			3			ns
Chip Select Hold Time	t_{HC}	1			2			ns
Data Hold Time	t_{HD}	1			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	1		3.5	ns
Output Fall Time	t_f	1		3.5	ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

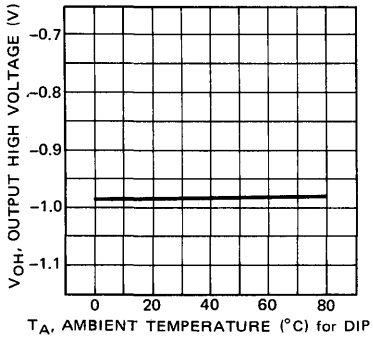


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

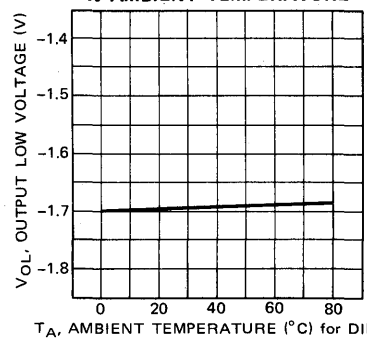


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

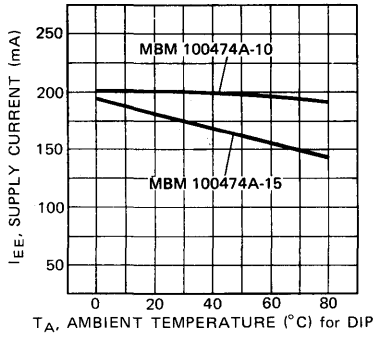


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

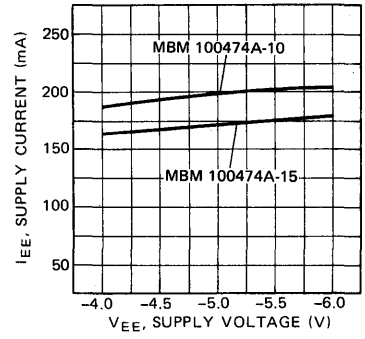


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

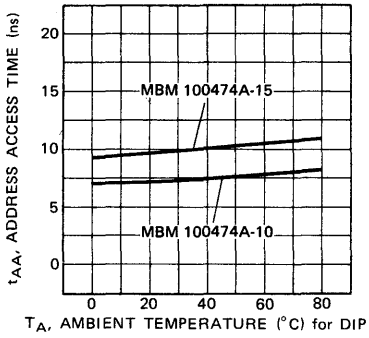


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

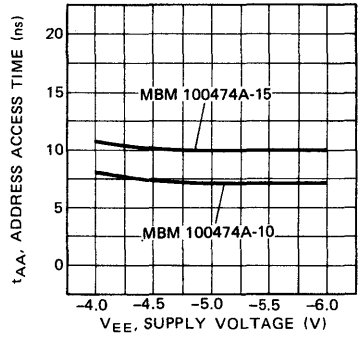


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

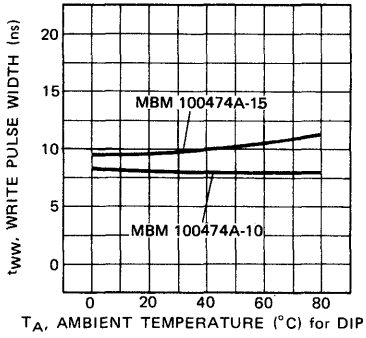
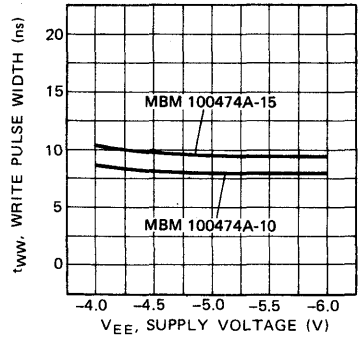


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

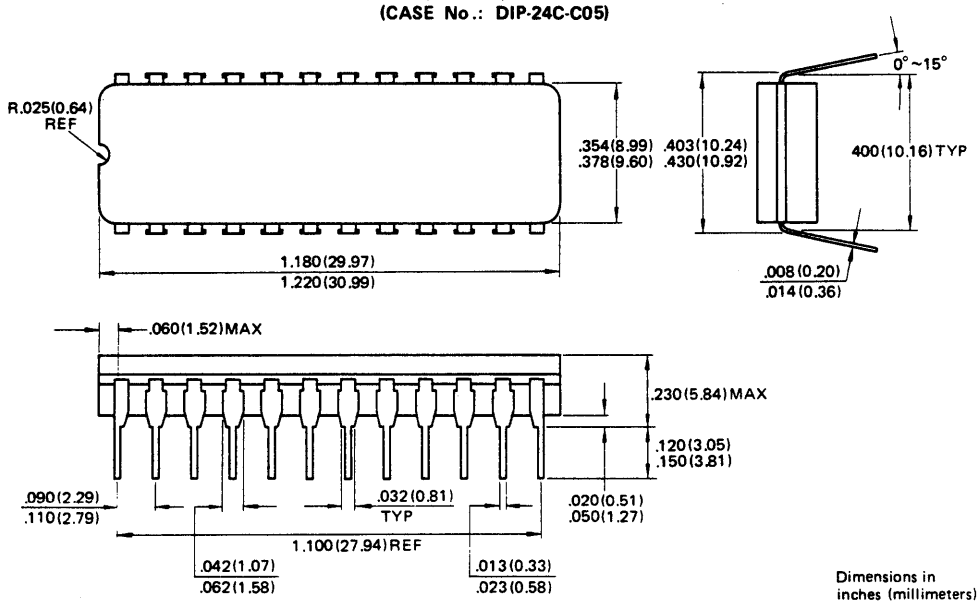


1

PACKAGE DIMENSIONS

(Suffix: -CZ)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)

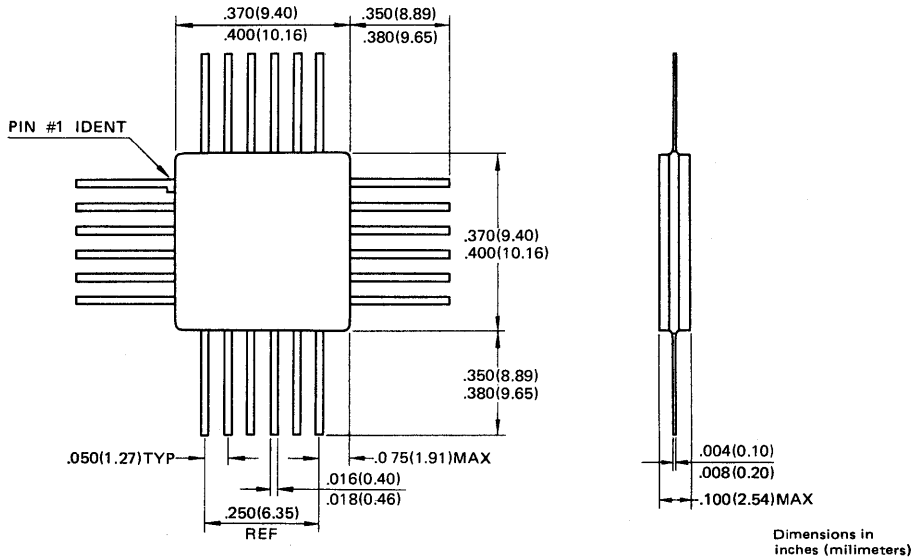


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

(Suffix: -ZF)

24-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-24C-C02)



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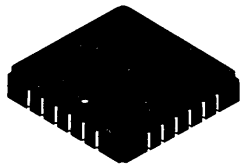
1

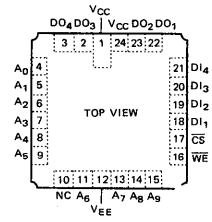
PACKAGE DIMENSIONS

(Suffix: -TV)

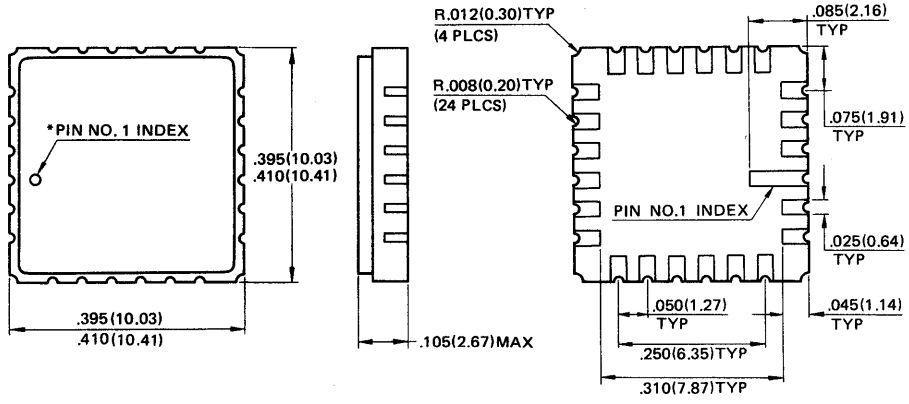


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

*Shape of Pin 1 index: Subject to change without notice

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 10480-15
MBM 10480-25

September 1984
Edition 3.0

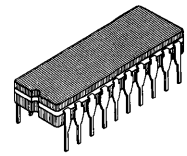
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10480 is fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

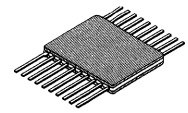
The MBM 10480 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 10480 is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

- 16384 words x 1 bit organization
- On-chip voltage compensation for improved noise margin.
- Fully compatible with industry-standard 10K-series ECL families
- Address access time : 15 ns max. (MBM 10480-15)
  : 25 ns max. (MBM 10480-25)
- Chip select access time : 8 ns max. (MBM 10480-15)
  : 10 ns max. (MBM 10480-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.05 mW/bit
- DOPOS and IOP-II
- Pin compatible with the F10480

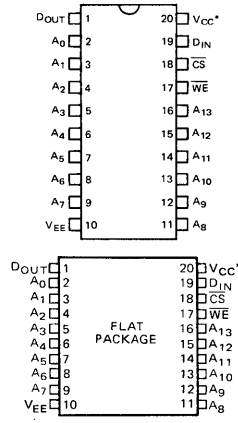


CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01
LCC-20C-F01: See Page 11

PIN ASSIGNMENT



*V_{CC} grounded

LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

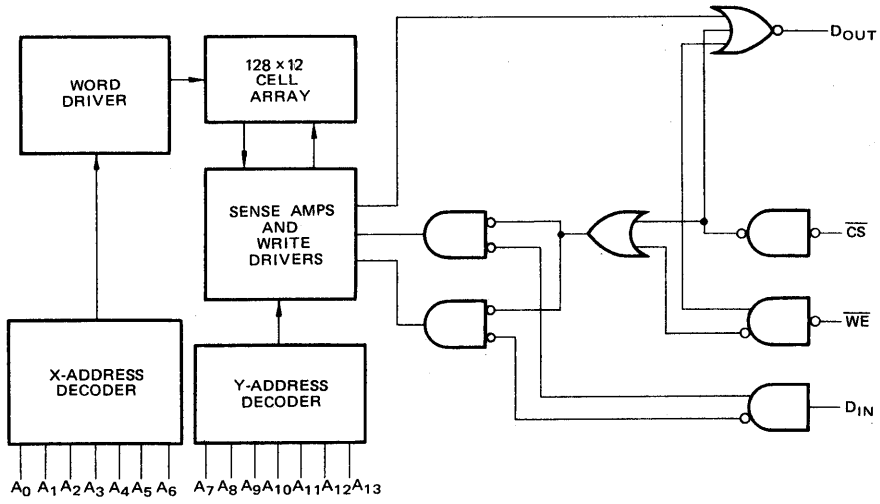
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 10480 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10480 is fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data in D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-or connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10480-15	I_{EE}	-220			mA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10480-25	I_{EE}	-200			mA	0°C to 75°C

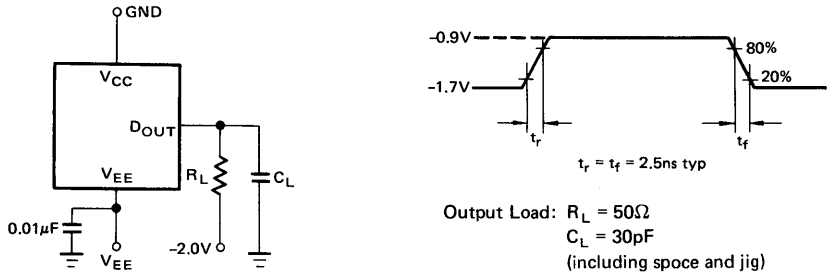
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		5		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC}=0V, V_{EE}=-5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A=0°C to 75°C for DIP, Airflow ≧ 2.5m/s, T_C=0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS



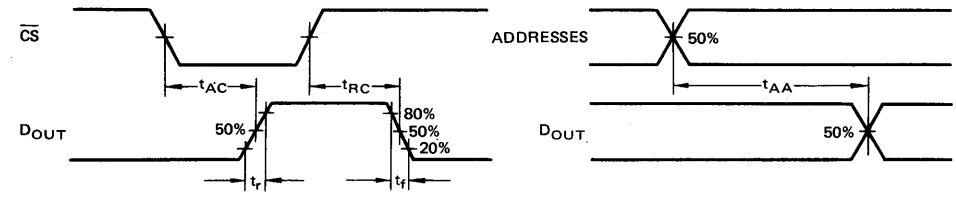
Output Load: R_L = 50Ω
C_L = 30pF
(including spoce and jig)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10480-15			MBM 10480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			15			25	ns
Chip Select Access Time	t_{AC}			8			10	ns
Chip Select Recovery Time	t_{RC}			8			10	ns

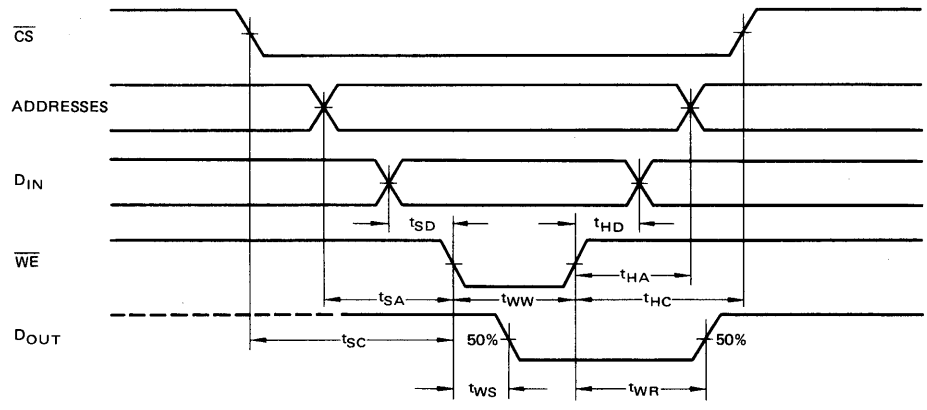
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 10480-15			MBM 10480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	15			25			ns
Write Disable Time	t_{WS}			8			10	ns
Write Recovery Time	t_{WR}			18			20	ns
Address Set Up Time	t_{SA}	2			5			ns
Chip Select Set Up Time	t_{SC}	2			5			ns
Data Set Up Time	t_{SD}	2			5			ns
Address Hold Time	t_{HA}	3			5			ns
Chip Select Hold Time	t_{HC}	3			5			ns
Data Hold Time	t_{HD}	3			5			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		3		ns
Output Fall Time	t_f		3		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

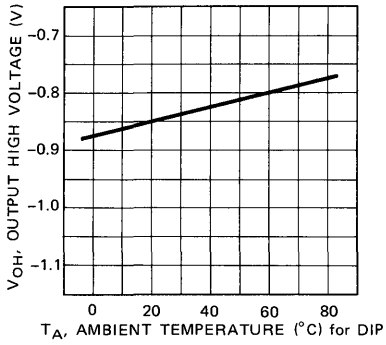


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

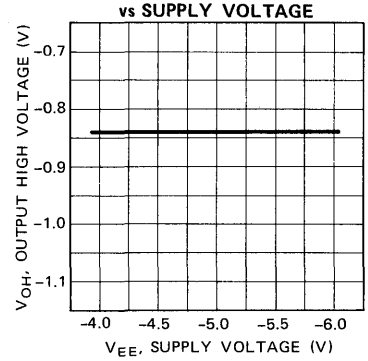


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

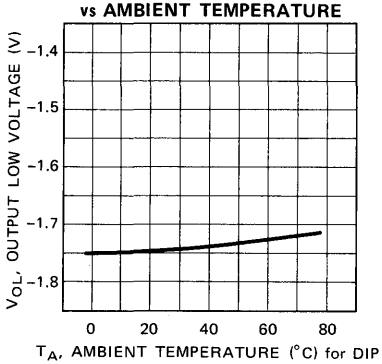


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

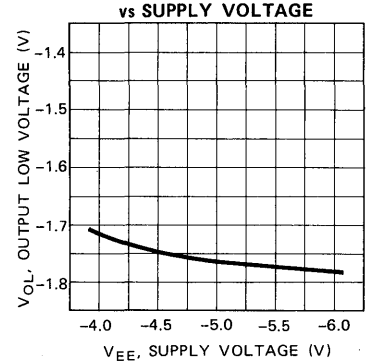


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

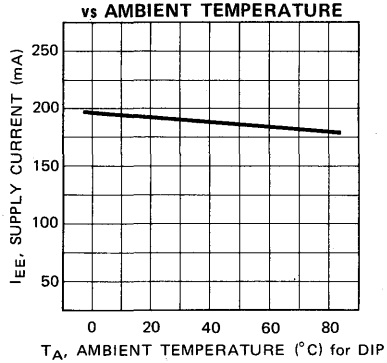


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

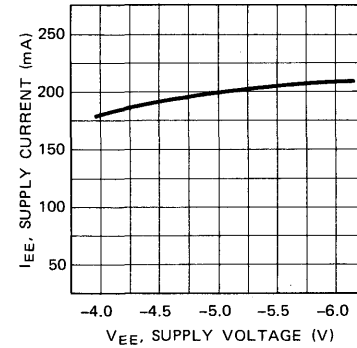


Fig.9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

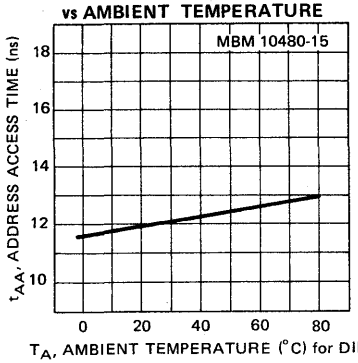


Fig. 10 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

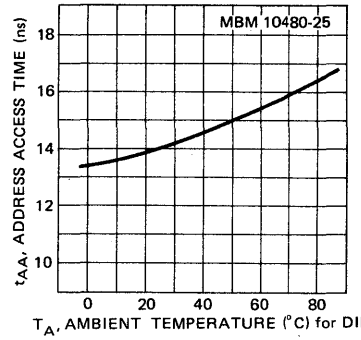


Fig.11 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

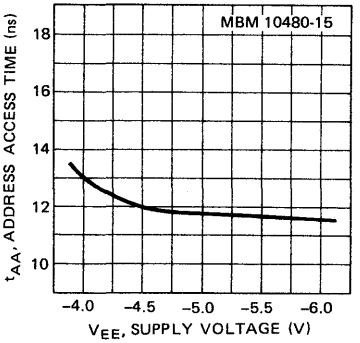


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

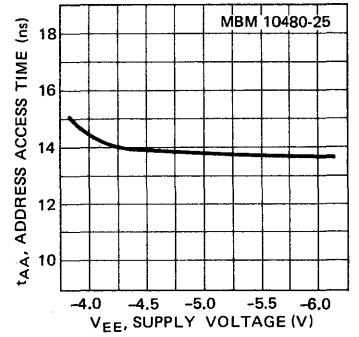


Fig.13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

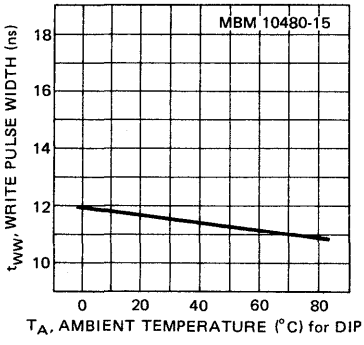
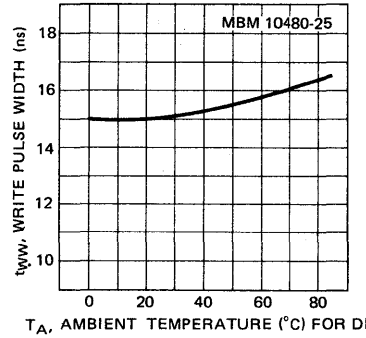


Fig. 14 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



1

Fig.15 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

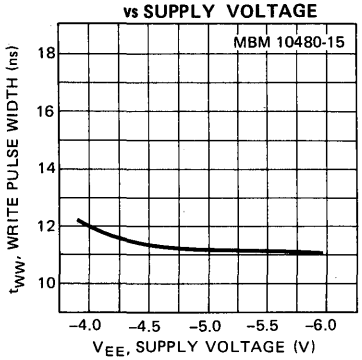
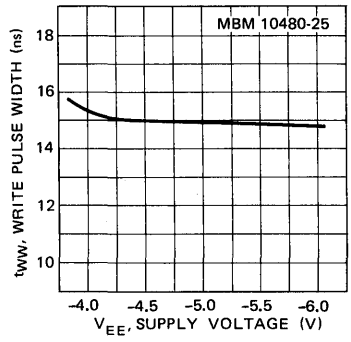
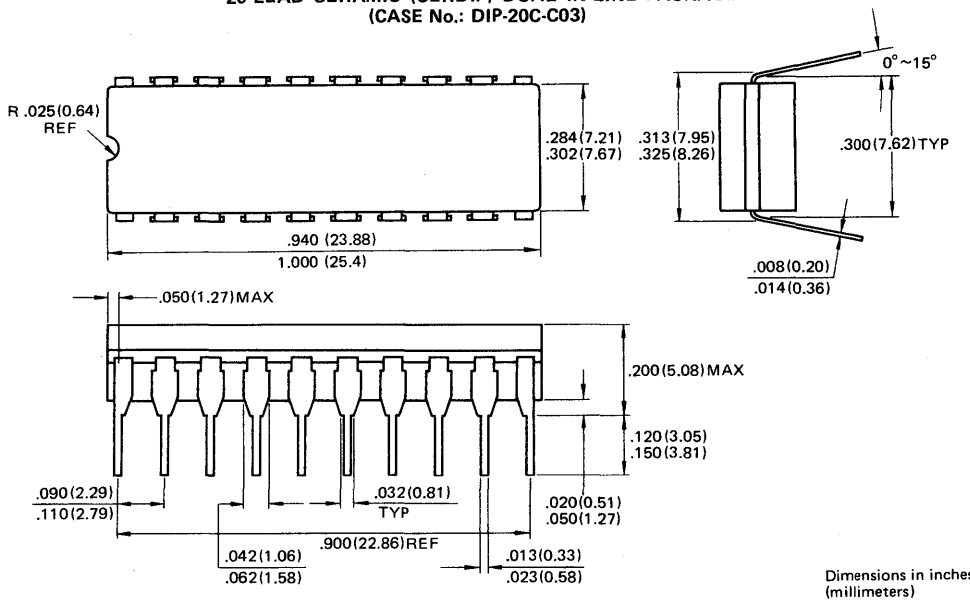


Fig. 16 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

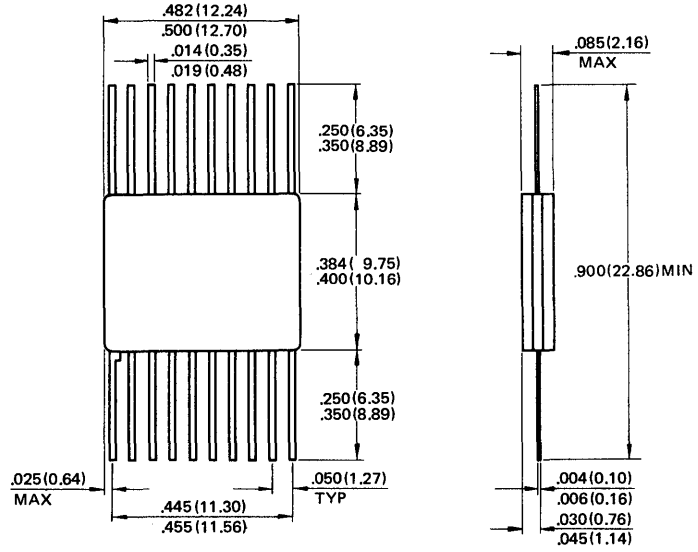


Dimensions in inches
(millimeters)

1

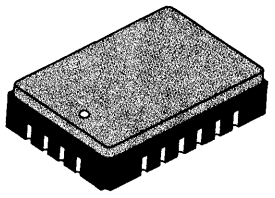
PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-20C-C01)



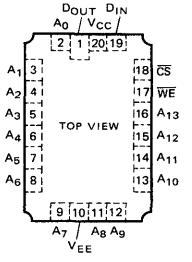
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

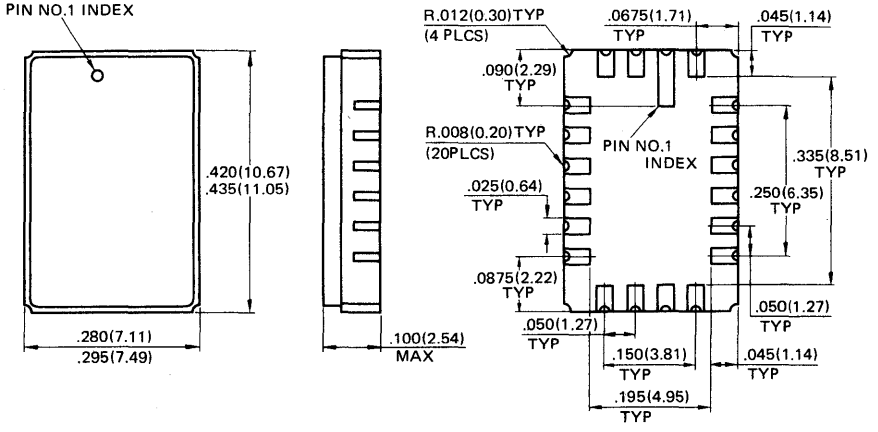


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



Dimension in
inches (millimeters)

1

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10480A-8

May 1988
Edition 1.0

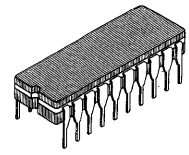
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10480A is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

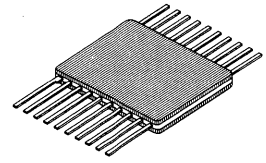
The MBM10480A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM10480A is specified over a temperature range of 0°C to 55°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

- 16384 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time: 8 ns max.
  Chip select access time: 4 ns max.
- Power dissipation: 0.07 mW/bit typ
- Open emitter output for ease of memory expansion
- DOPOS and IOP-II processing



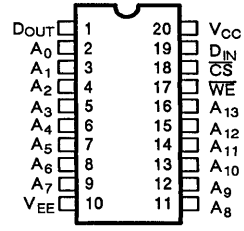
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01: See Page 10

PIN ASSIGNMENTS



LCC PAD CONFIGURATION: See Page 10

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

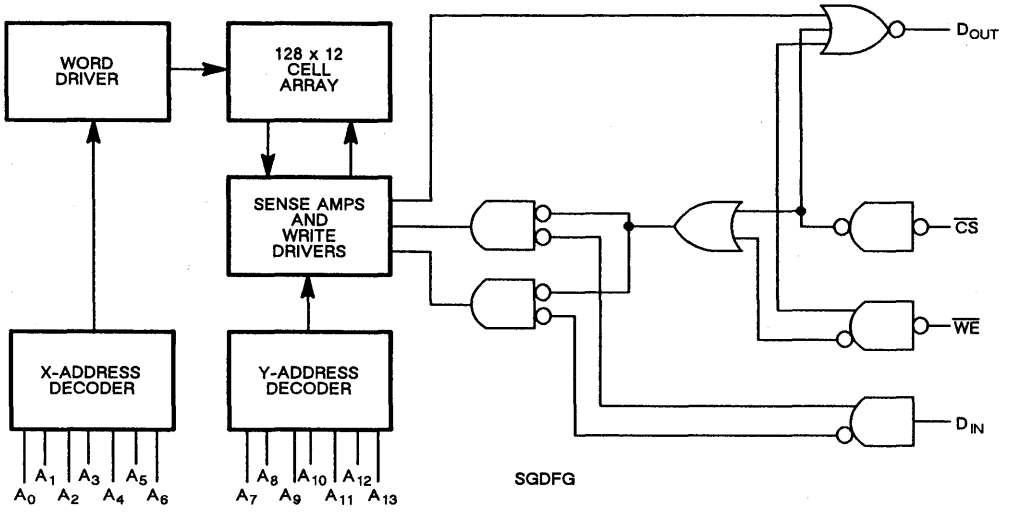
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

1

Fig. 1 — MBM10480A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10480A is a fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, TA = 0°C to 55°C for DIP, Airflow≥ 2.5 m/s, TC=0°C to 55°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -925	—	-840 -810 -760	mV	0°C 25°C 55°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830	—	-1665 -1650 -1625	mV	0°C 25°C 55°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -945	—	—	mV	0°C 25°C 55°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OLC}	—	—	-1645 -1630 -1605	mV	0°C 25°C 55°C
Input High voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1070	—	-840 -810 -760	mV	0°C 25°C 55°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1840	—	-1490 -1475 -1460	mV	0°C 25°C 55°C
Input High Current (VIN=VIH max)	I_{IH}	—	—	220	µA	0°C to 55°C
Input Low Current (VIN=VIL min)	I_{IL}	-50	—	90	µA	0°C to 55°C
CS Input Low Current (VIN=VIL min)	I_{IL}	0.5	—	170	µA	0°C to 55°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-260	—		mA	0°C to 55°C

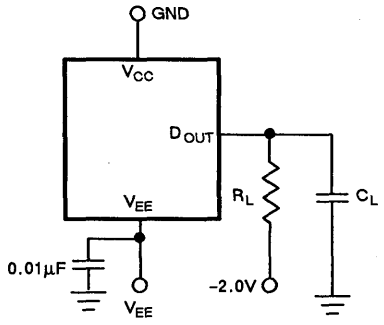
CAPACITANCE

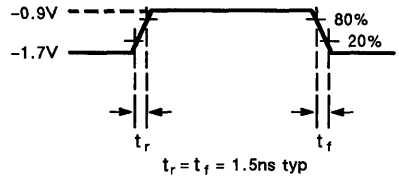
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

AC CHARACTERISTICS

(V_{CC} = 0V, VEE=-5.2V, Output Load=50Ω and 30pF and -2.0V, TA = 0°C to 55°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 55°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC Test Conditions



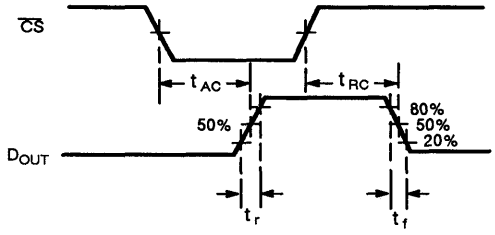


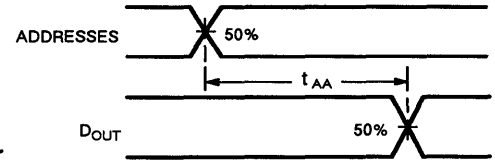
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

Note: All timing measurements referenced to 50% input levels.

Parameter	Symbol	MBM10480A-10			Unit
		Min	Typ	Max	
READ CYCLE					
Address Access Time	t_{AA}	2	—	8	ns
Chip Select Access Time	t_{AC}	1	—	4	ns
Chip Select Recovery Time	t_{RC}	1	—	4	ns

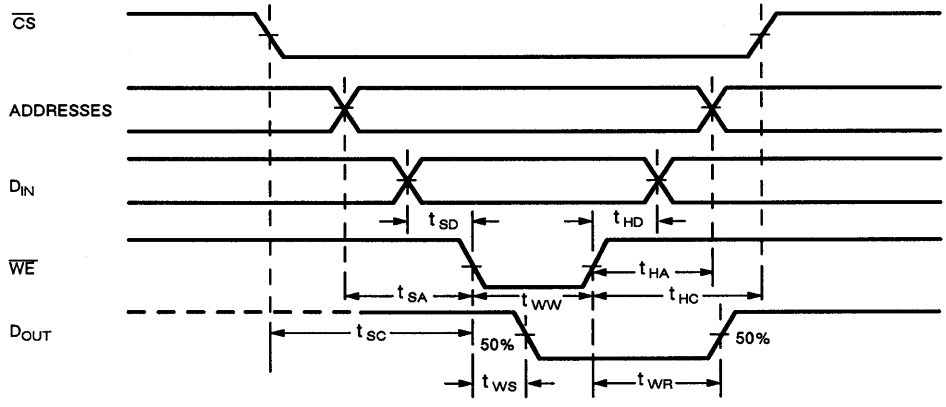
READ CYCLE TIMING DIAGRAMS





Parameter	Symbol	MBM10480A-10			Unit
		Min	Typ	Max	
WRITE CYCLE					
Write Pulse Width	t_{WW}	10	—	—	ns
Write Disable Time	t_{WS}	—	—	4	ns
Write Recovery Time	t_{WR}	—	—	11	ns
Address Set Up Time	t_{SA}	2	—	—	ns
Chip Select Set Up Time	t_{SC}	2	—	—	ns
Data Set Up Time	t_{SD}	2	—	—	ns
Address Hold Time	t_{HA}	1	—	—	ns
Chip Select Hold Time	t_{HC}	1	—	—	ns
Data Hold Time	t_{HD}	1	—	—	ns

WRITE CYCLE TIMING DIAGRAMS



Parameter	Symbol	Min	Typ	Max	Unit
RISE TIME and FALL TIME					
Output Rise Time	t_r	—	2	—	ns
Output Fall Time	t_f	—	2	—	ns

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 — OUTPIT HIGH VOLTAGE vs AMBIENT TEMPERATURE

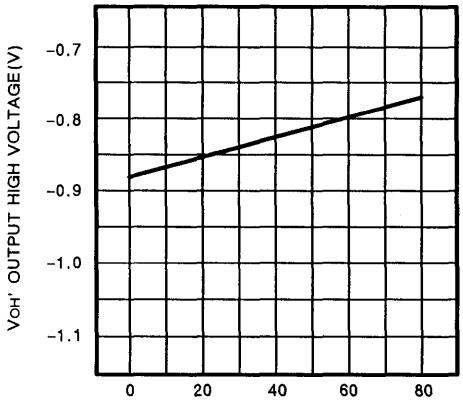


Fig. 4 — OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

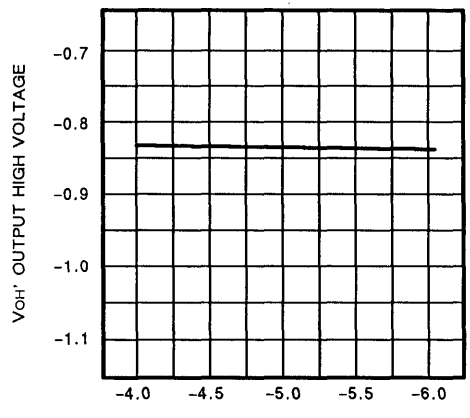


Fig. 5 — OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

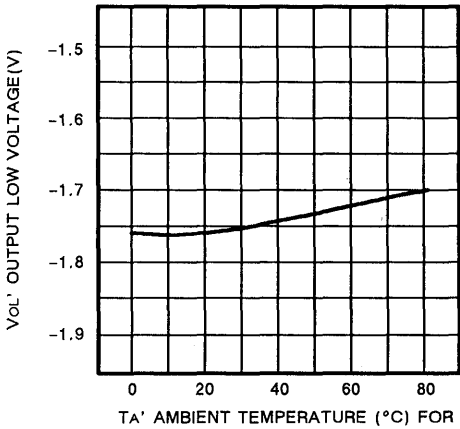
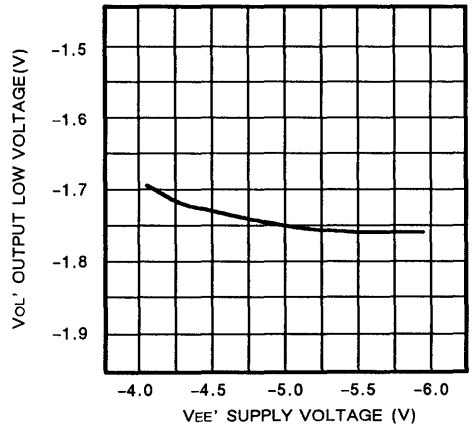


Fig. 6 — OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 7 — SUPPLY CURRENT vs AMBIENT TEMPERATURE

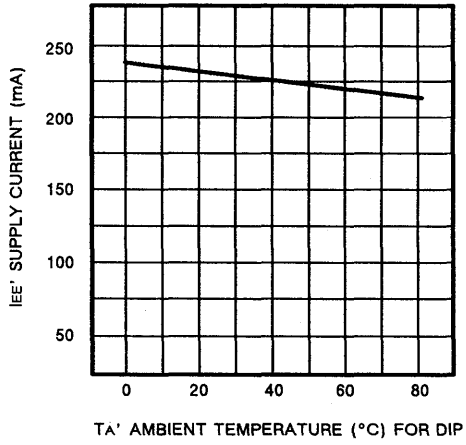


Fig. 8 — SUPPLY CURRENT vs SUPPLY VOLTAGE

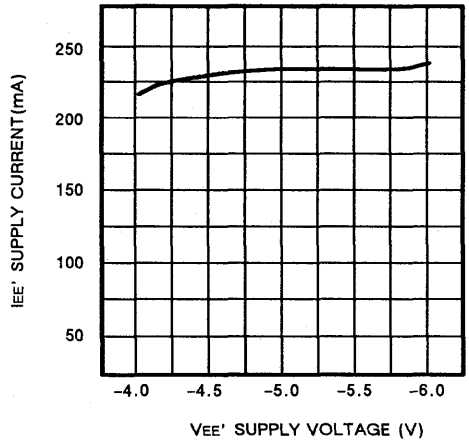


Fig. 9 — ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

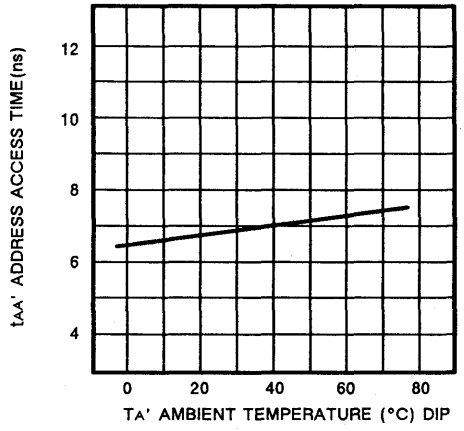
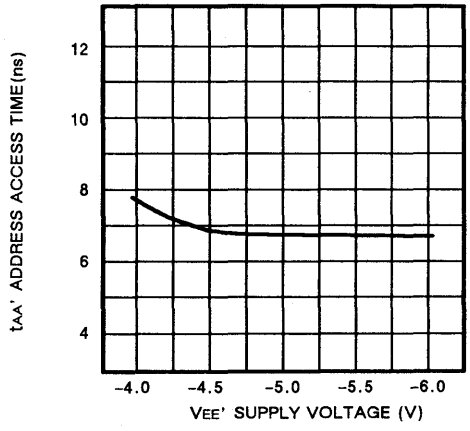


Fig. 10 — ADDRESS ACCESS TIME vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 11 — WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

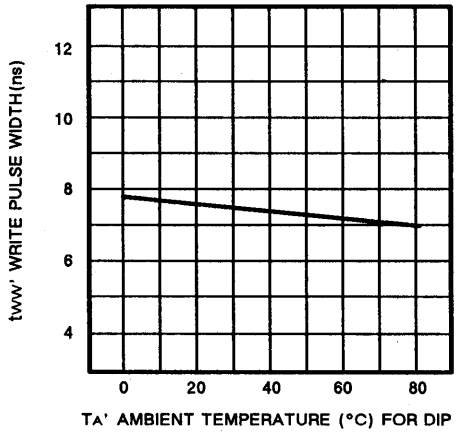
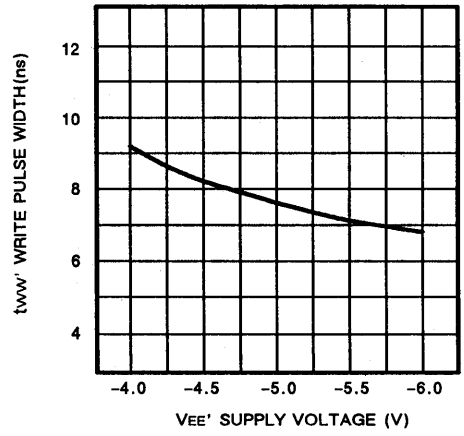
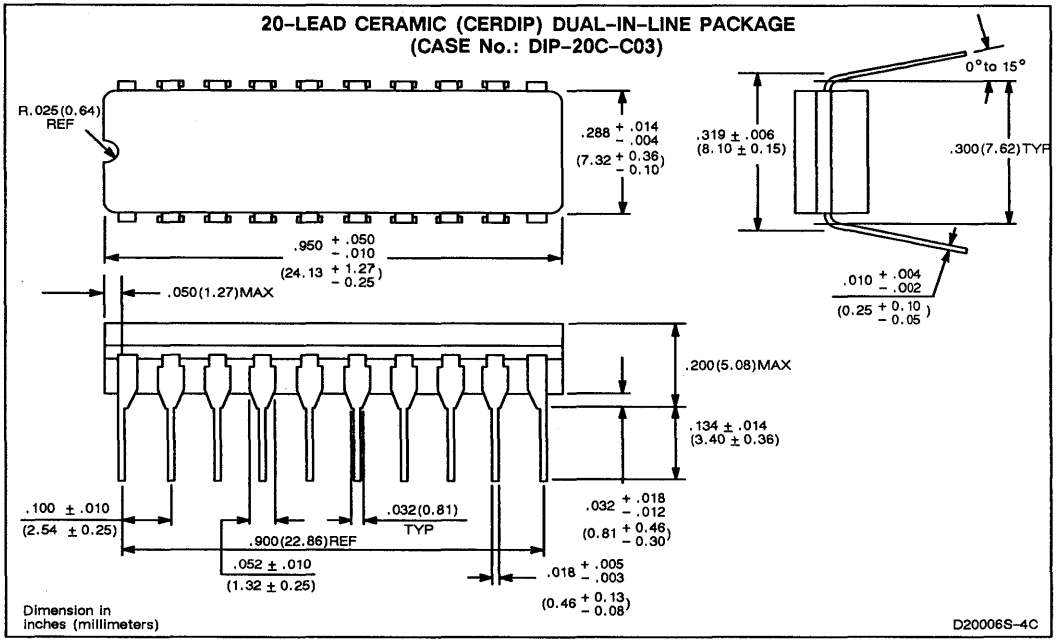


Fig. 12 — WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

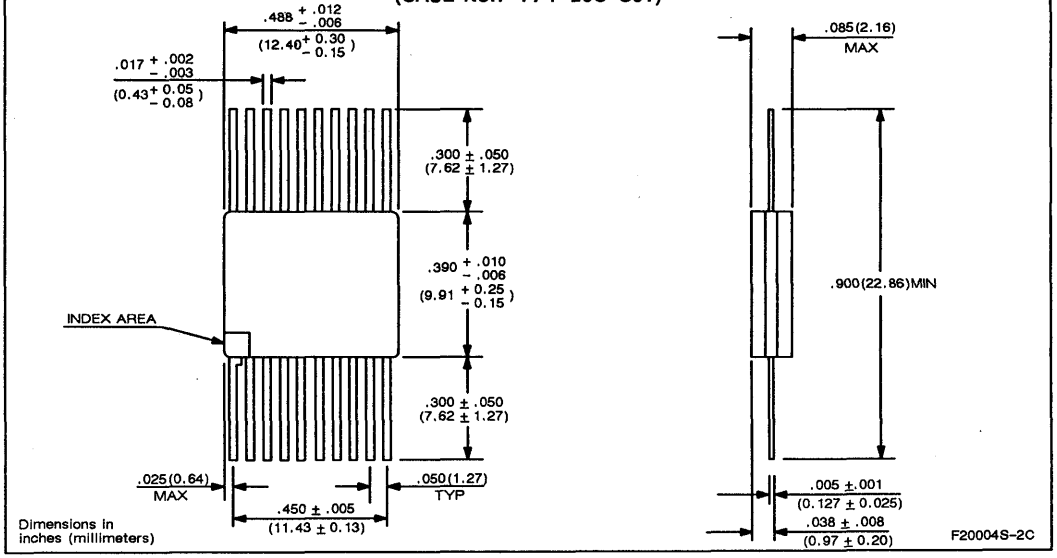
20-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimension in inches (millimeters)

D20006S-4C

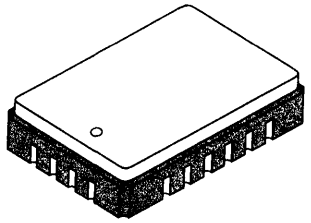
20-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-20C-C01)



Dimensions in inches (millimeters)

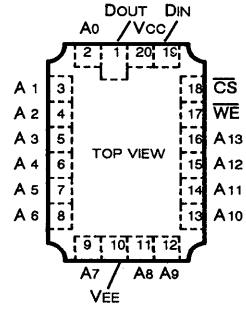
F20004S-2C

PACKAGE DIMENSIONS (Continued)

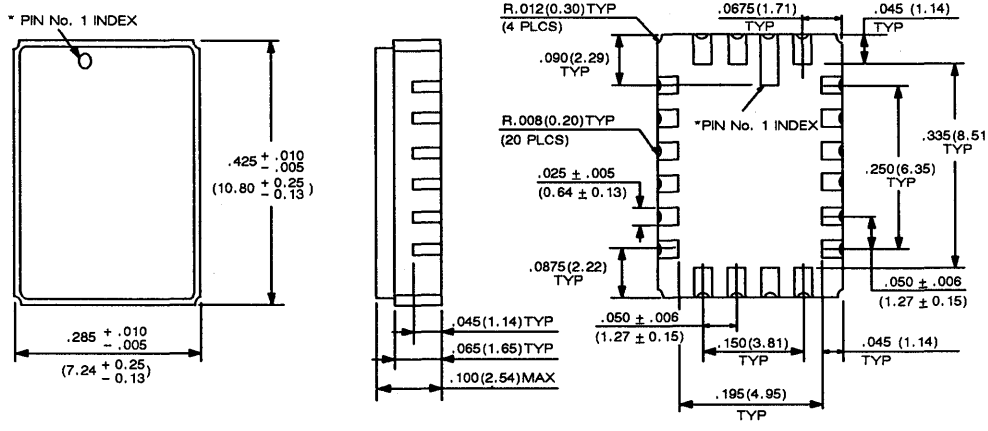


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIERS
(CASE No.: LCC-20C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

C20003S-1C

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10480A-10

May 1988
Edition 1.0

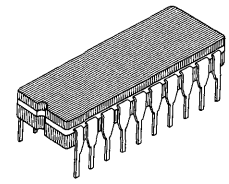
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10480A is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

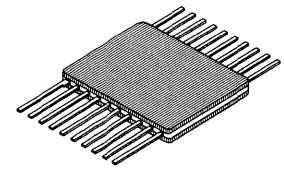
The MBM10480A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM10480A is specified over a temperature range of 0°C to 55°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 10K-series ECL families.

- 16384 words x 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10K-series ECL families
- Address access time: 10 ns max.
  Chip select access time: 4 ns max.
- Power dissipation: 0.07 mW/bit typ
- Open emitter output for ease of memory expansion
- DOPOS and IOP-II processing



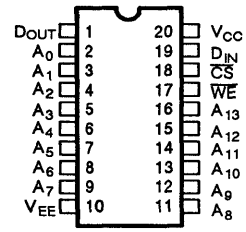
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01: See Page 10

PIN ASSIGNMENTS



LCC Pad Configuration: See Page 10

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

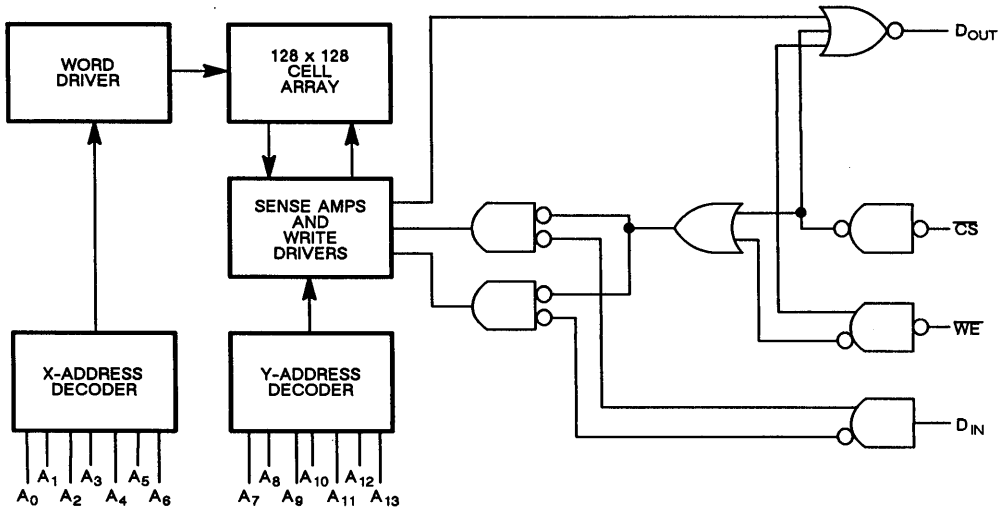
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

1

Fig. 1 — MBM10480A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

Notes:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10480A is a fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data in D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-or connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω and 30 pF to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage $V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage $V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage $V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage $V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Inout High Voltage (Guarenteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Inout Low Voltage (Guarenteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max}$)	I_{IH}			220	µA	0°C to 75°C
Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	-220			mV	0°C to 75°C

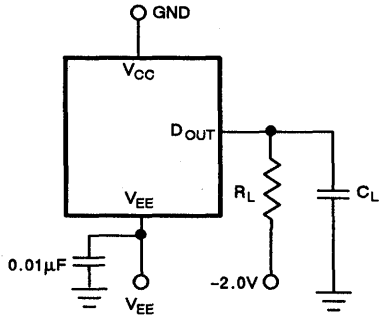
CAPACITANCE

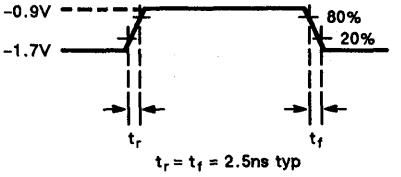
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC Test Conditions





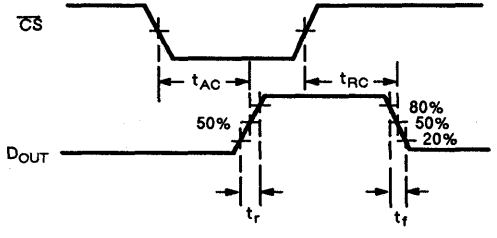
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

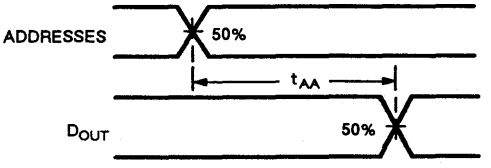
Note: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM10480A-10			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}	2		10	ns
Chip Select Access Time	t_{AC}	1		5	ns
Chip Select Recovery Time	t_{RC}	1		5	ns

READ CYCLE TIMING DIAGRAMS

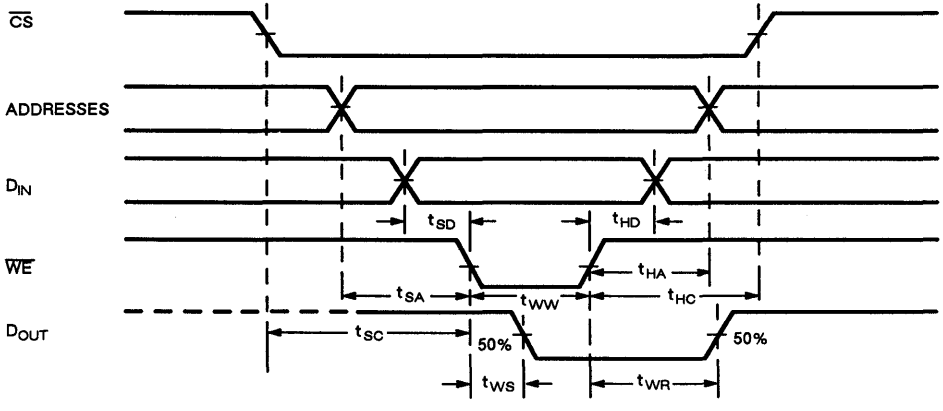




WRITE CYCLE

Parameter	Symbol	MBM10480A-10			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			5	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAMS



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2		ns
Output Fall Time	t_f		2		ns

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Output High Voltage vs Ambient Temperature

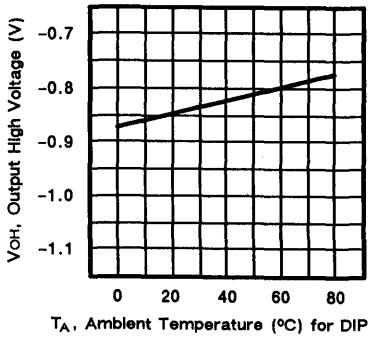


Fig. 4 – Output High Voltage vs Supply Voltage

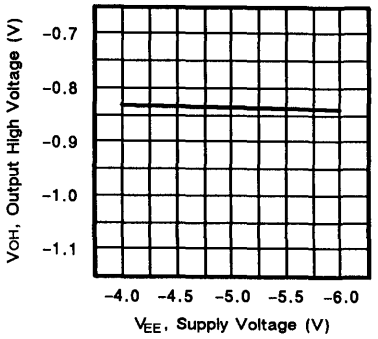


Fig. 5 – Output Low Voltage vs Ambient Temperature

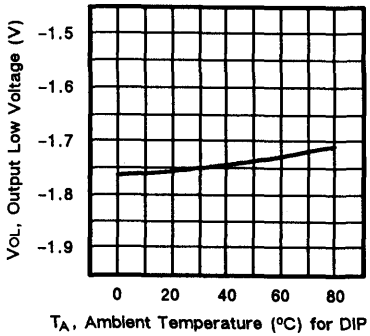


Fig. 6 – Output Low Voltage vs Supply Voltage

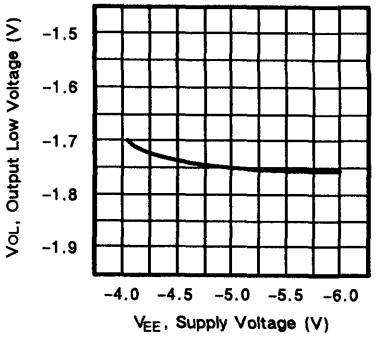


Fig. 7 – Supply Current vs Ambient Temperature

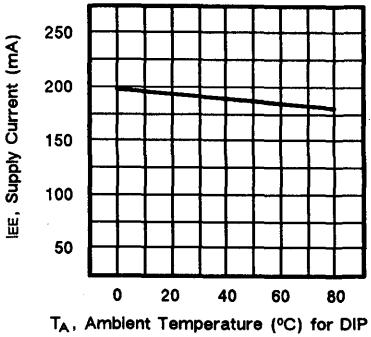
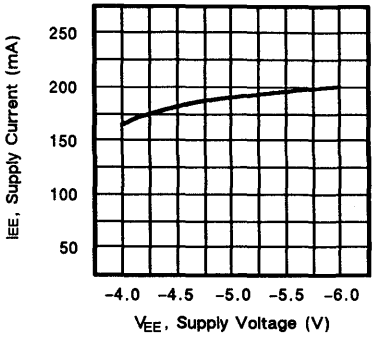


Fig. 8 – Supply Current vs Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 9 – Address Access Time vs Ambient Temperature

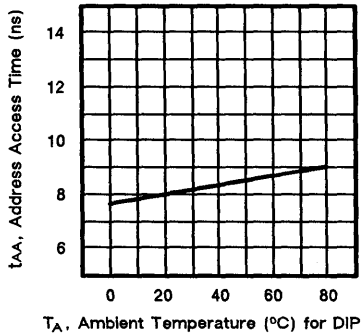


Fig. 10 – Address Access Time vs Supply Voltage

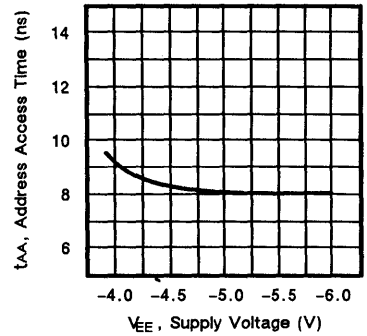


Fig. 11 – Write Pulse Width vs Ambient Temperature

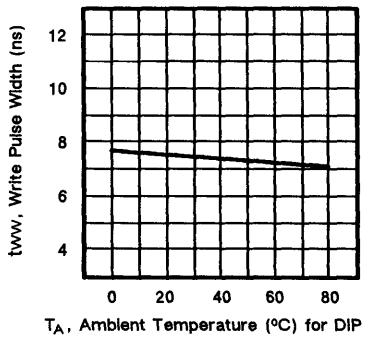
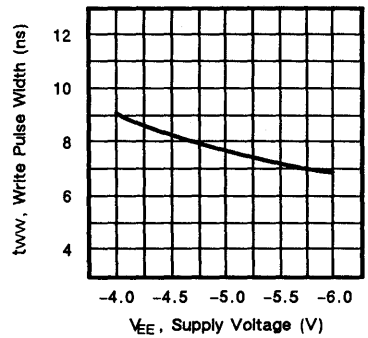


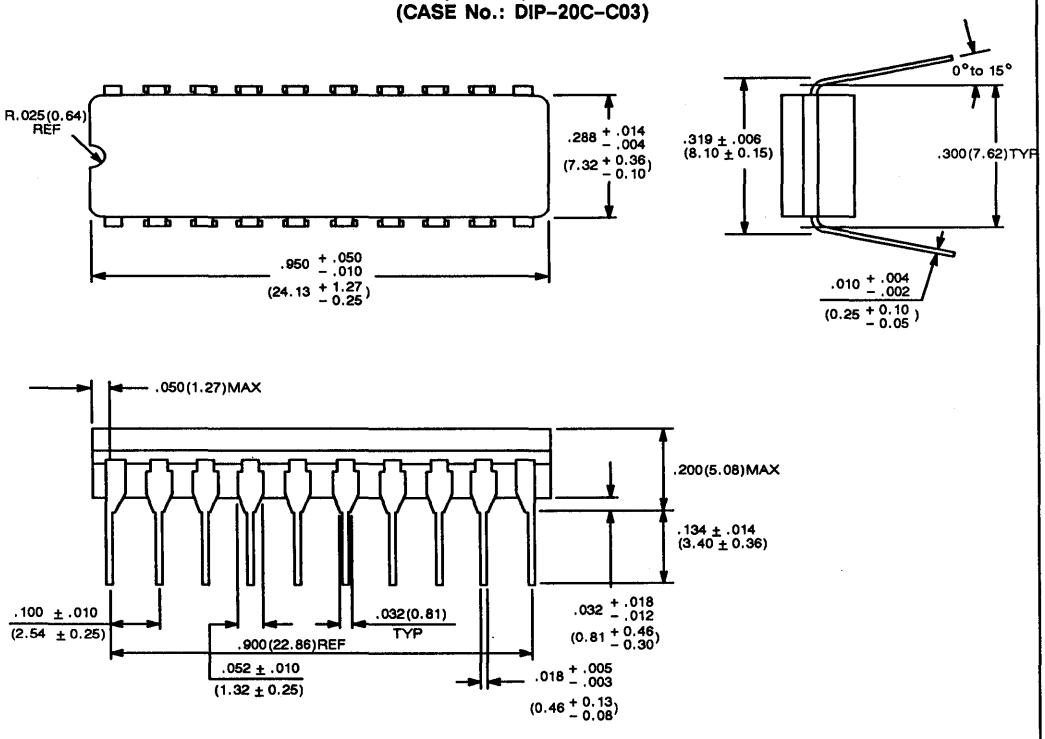
Fig. 12 – Write Pulse Width vs Supply Voltage



1

PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

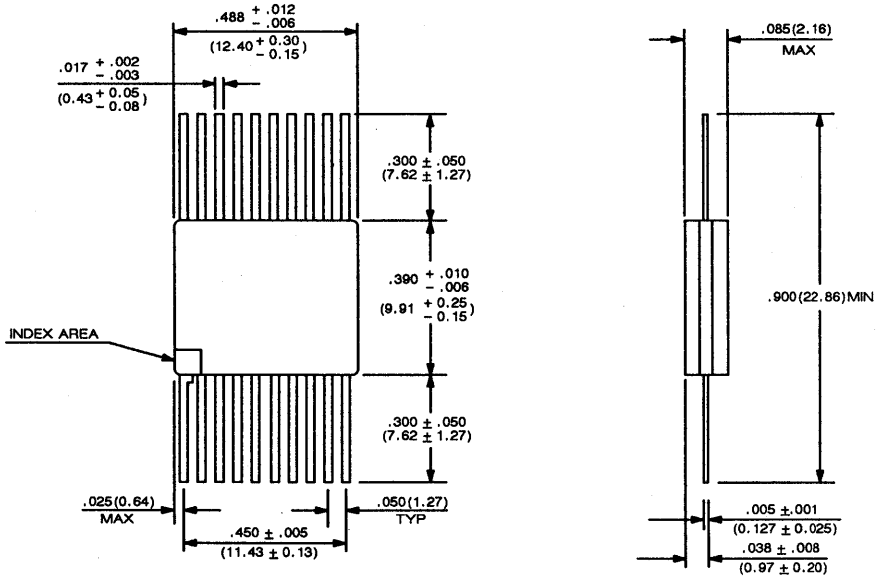


Dimension in inches (millimeters)

D20006S-4C

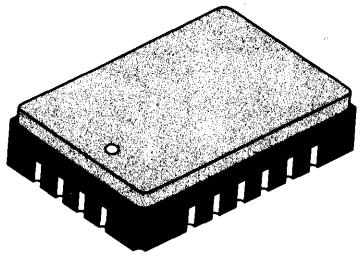
PACKAGE DIMENSIONS (continued)

20-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-20C-C01)



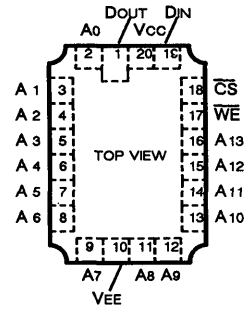
Dimensions in
inches (millimeters)

F20004S-2C

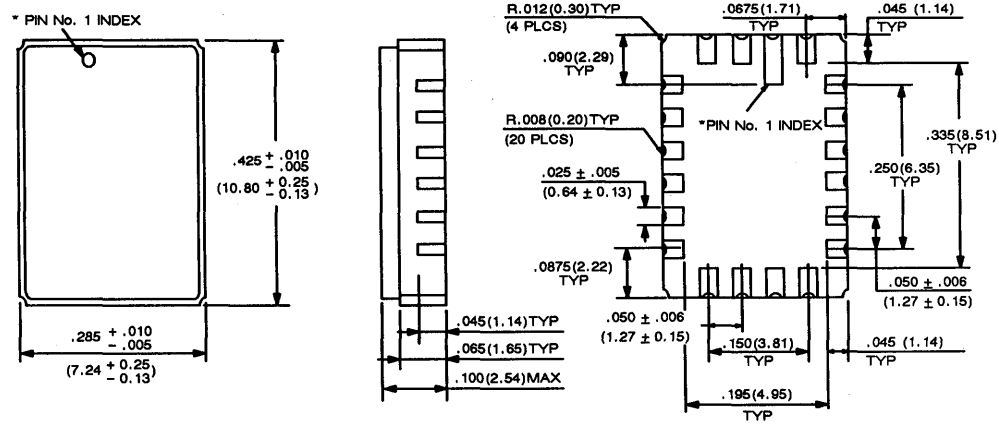


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

C20003S-1C

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 100480-15
MBM 100480-25

September 1984
Edition 3.0

1

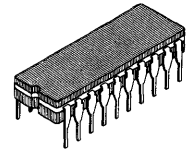
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100480 is fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

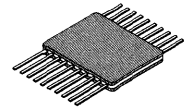
The MBM 100480 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100480 is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 16384 words x 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K-series ECL families
- Address access time : 15 ns max. (MBM 100480-15)
  : 25 ns max. (MBM 100480-25)
- Chip select access time : 8 ns max. (MBM 100480-15)
  : 10 ns max. (MBM 100480-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.04 mW/bit
- DOPOS and IOP-II
- Pin compatible with the F100480



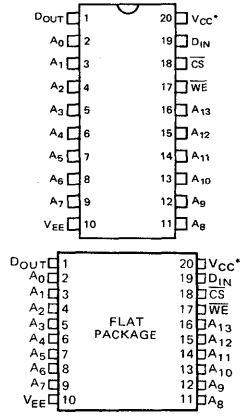
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01 : See Page 11

PIN ASSIGNMENT



*V_{CC} grounded

LCC PAD CONFIGURATION : See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

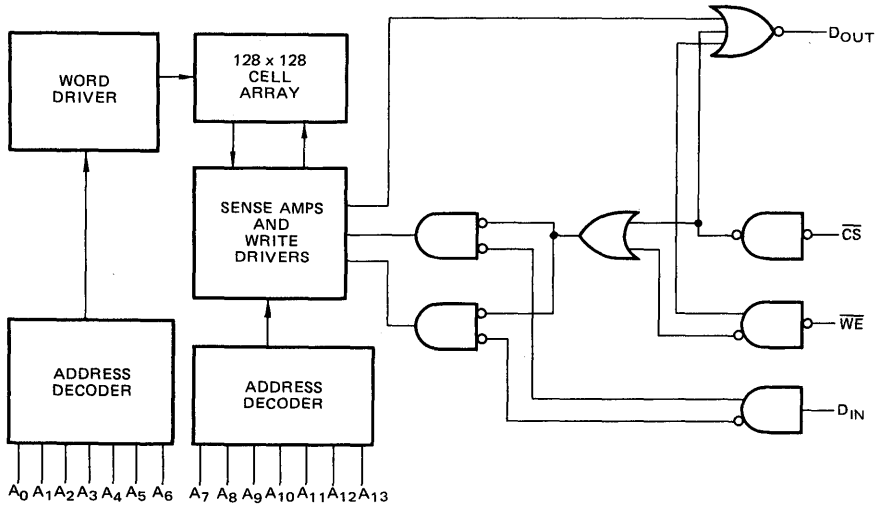
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	Tc for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

1

Fig. 1 – MBM 100480 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100480 is fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC}=0V, V_{EE}=-4.5V, Output Load = 50Ω and 30pF to -2.0V, T_A=0°C to 85°C for DIP, Airflow ≧ 2.5m/s, T_C=0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)		V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)		V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)		I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	MBM 100480-15	I_{EE}	-220			mA
	MBM 100480-25		-200			

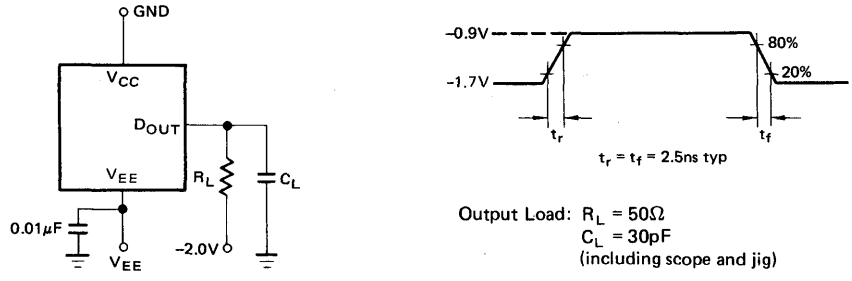
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		5		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC}=0V, V_{EE}=-4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_A=0°C to 85°C for DIP, Airflow ≧ 2.5m/s, T_C=0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS



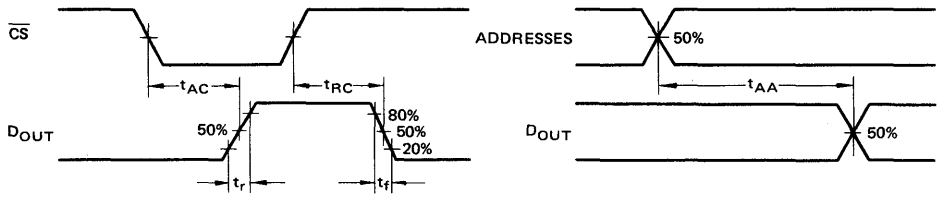
Output Load: R_L = 50Ω
C_L = 30pF
(including scope and jig)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 100480-15			MBM 100480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			15			25	ns
Chip Select Access Time	t_{AC}			8			10	ns
Chip Select Recovery Time	t_{RC}			8			10	ns

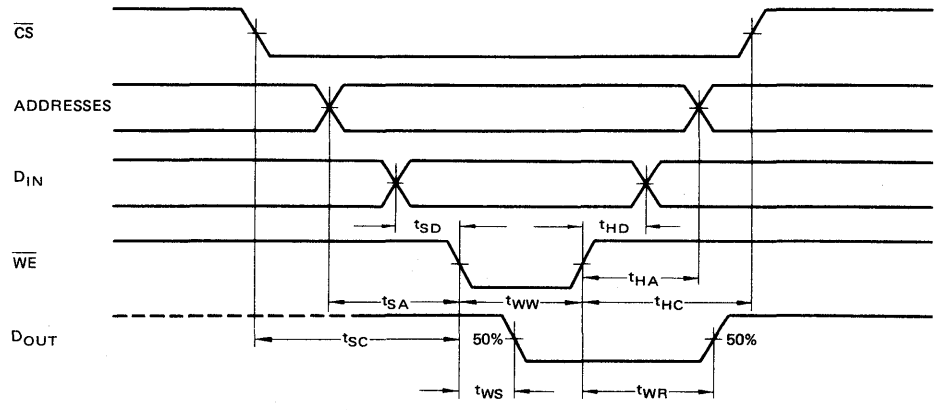
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	MBM 100480-15			MBM 100480-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	15			25			ns
Write Disable Time	t_{WS}			8			10	ns
Write Recovery Time	t_{WR}			18			20	ns
Address Set Up Time	t_{SA}	2			5			ns
Chip Select Set Up Time	t_{SC}	2			5			ns
Data Set Up Time	t_{SD}	2			5			ns
Address Hold Time	t_{HA}	3			5			ns
Chip Select Hold Time	t_{HC}	3			5			ns
Data Hold Time	t_{HD}	3			5			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		3		ns
Output Fall Time	t_f		3		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

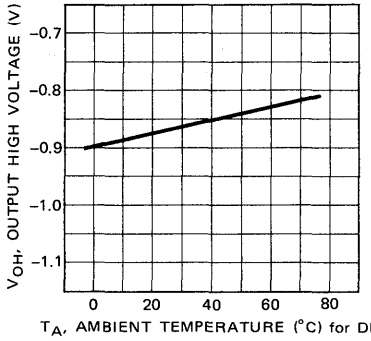


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

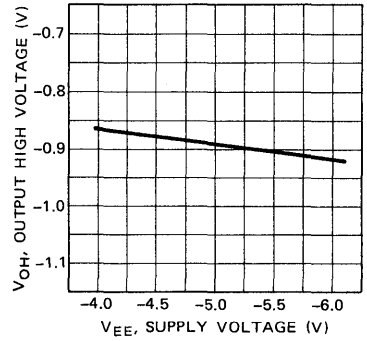


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

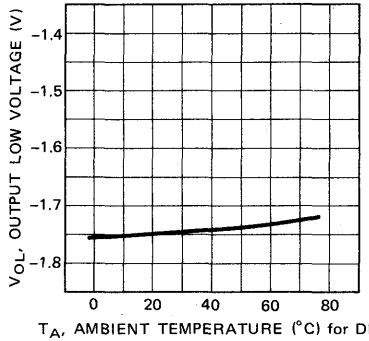


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

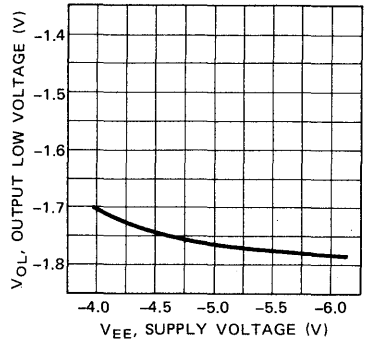


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

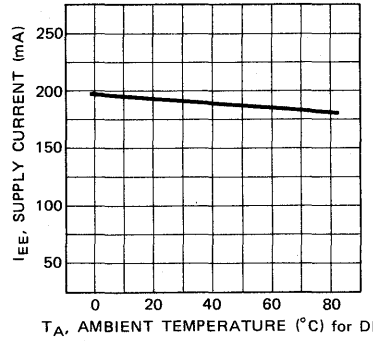
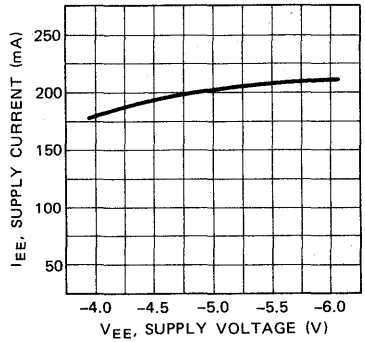


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE



1

Fig.9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

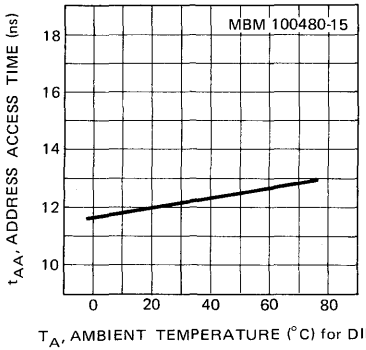


Fig.10 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

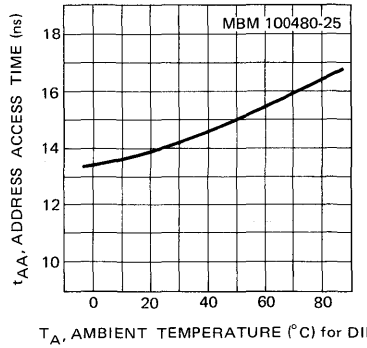


Fig.11 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

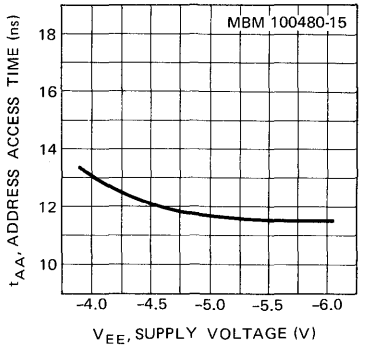


Fig.12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

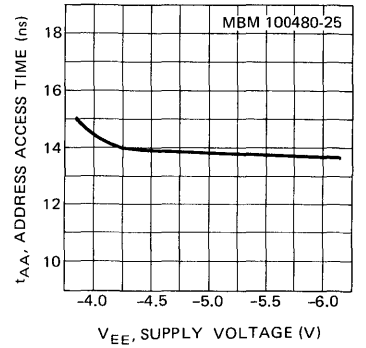


Fig.13 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

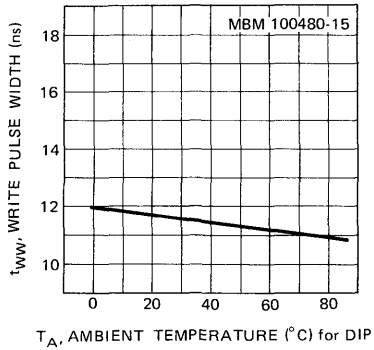
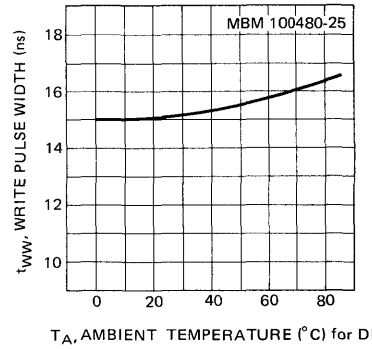


Fig.14 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE



1

Fig.15 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

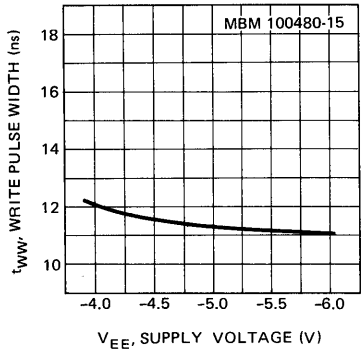
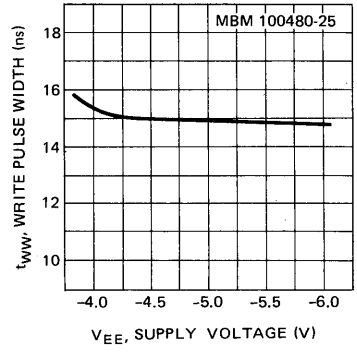
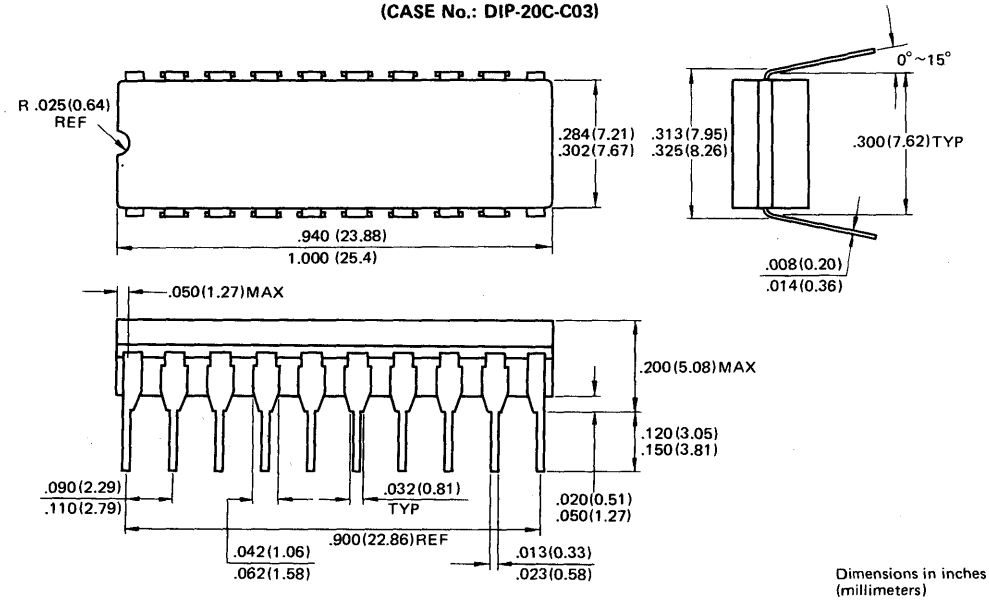


Fig.16 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

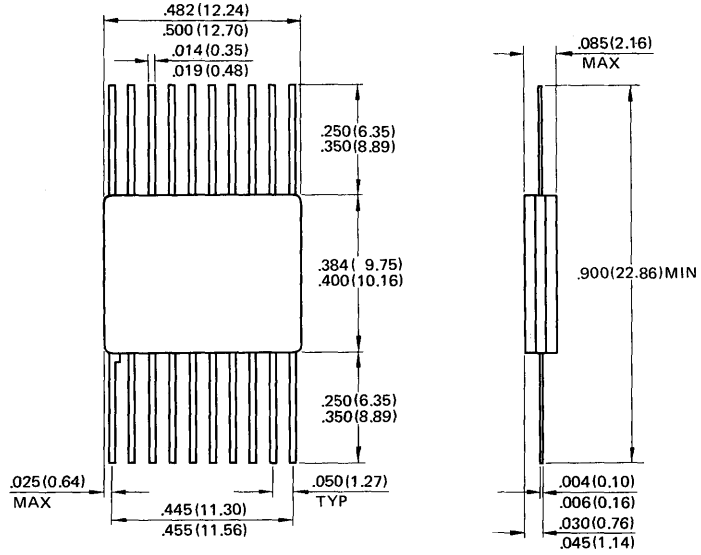


Dimensions in inches
(millimeters)

1

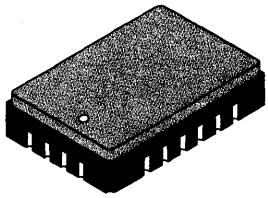
PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-20C-C01)



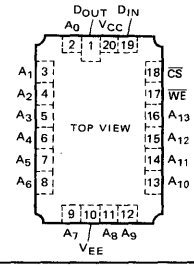
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

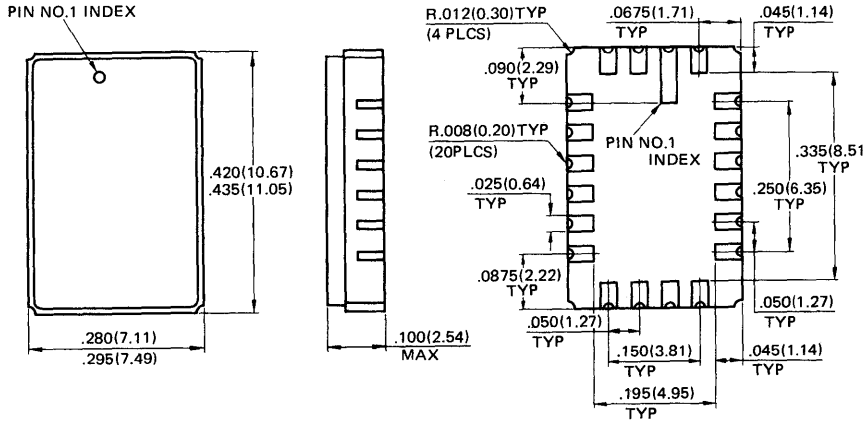


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



Dimension in
inches (millimeters)

1

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100480A-8

May 1988
Edition 1.0

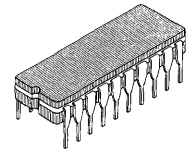
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100480A is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

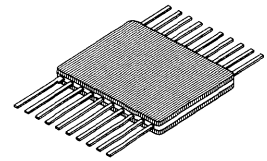
The MBM100480A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) Processing.

Operation for the MBM100480A is specified over a temperature range of from 0°C to 65°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 16384 words by 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K series ECL families
- Address access time: 8 ns max.
  Chip select access time: 4 ns max.
- Power dissipation: 0.06 mW/bit (typ.)
- Open emitter output for ease of memory expansion
- DOPOS and IOP-II processing



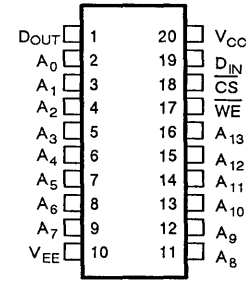
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01: See Page 10

PIN ASSIGNMENTS



LCC Pad Configuration: See Page 10

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

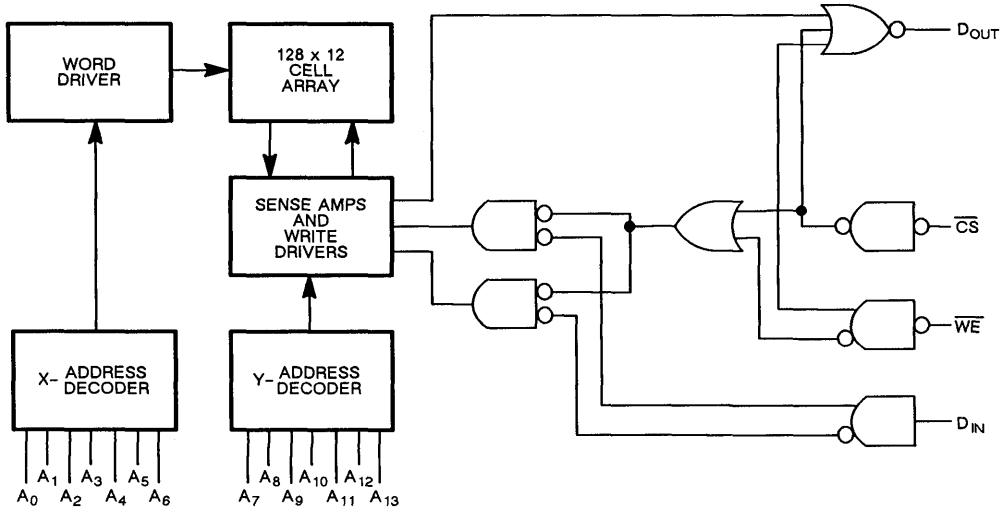
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to **Absolute Maximum Rating** conditions for extended periods may affect device reliability.

1

Fig. 1 — MBM100480A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100480A is fully decoded 16384 bit read/write random access memory organized as 16384 words by 1 bit. Memory cell selection is achieved by means of a 14-bit address designated A0 through A13. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 65°C

DC CHARACTERISTICS

(VCC=0V, VEE=-4.5V, Output Load=50Ω and 30pF to -2.0V, TA=0°C to 65°C for DIP, Airflow≥ 2.5m/s, TC=0°C to 5°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025	—	-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810	—	-1620	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035	—	—	mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}	—	—	-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165	—	-880	
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810	—	-1475	
Input High Current (VIN = VIH max)	I_{IH}	—	—	220	µA
Input Low Current (VIN = VIL min)	I_{IL}	—	—	90	µA
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5	—	170	µA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-260	—	—	mA

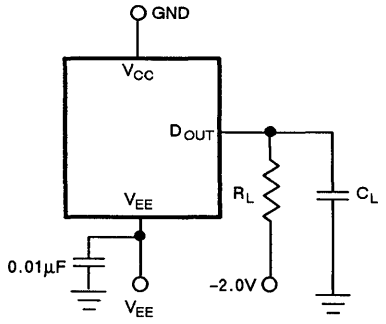
CAPACITANCE

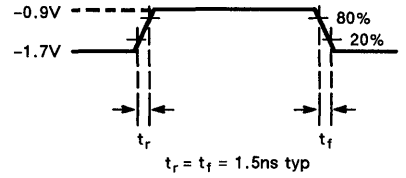
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	—	pF
Output Pin Capacitance	C_{OUT}	—	6	—	pF

AC CHARACTERISTICS

(VCC=0V, VEE=-4.5V ±5%, Output Load=50Ω to -2.0V and 30 pF to GND, TA=0°C to 65°C for DIP, Airflow ≧ 2.5m/s, TC=0°C to 65°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC Test Conditions





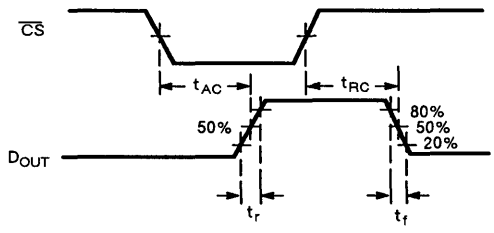
$t_r = t_f = 1.5ns$ typ

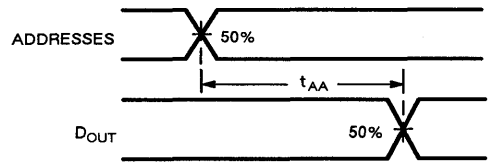
Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including spoce and jig)

Note: All timing measurements referenced to 50% input levels.

Parameter	Symbol	MBM100480A-8			Unit
		Min	Typ	Max	
READ CYCLE					
Address Access Time	t_{AA}	2	—	8	ns
Chip Select Access Time	t_{AC}	1	—	4	ns
Chip Select Recovery Time	t_{RC}	1	—	4	ns

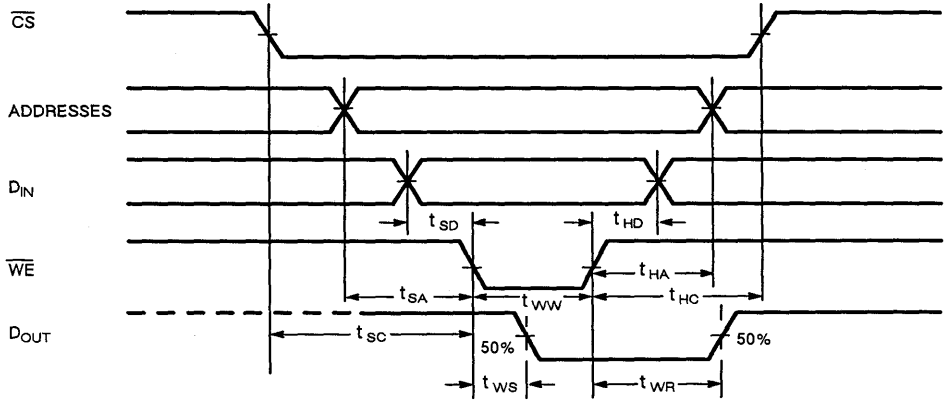
READ CYCLE TIMING DIAGRAMS





Parameter	Symbol	MBM100480A-8			Unit
		Min	Typ	Max	
WRITE CYCLE					
Write Pulse Width	t_{WW}	10	—		ns
Write Disable Time	t_{WS}	—	—	4	ns
Write Recovery Time	t_{WR}	—	—	11	ns
Address Set Up Time	t_{SA}	2	—	—	ns
Chip Select Set Up Time	t_{SC}	2	—	—	ns
Data Set Up Time	t_{SD}	2	—	—	ns
Address Hold Time	t_{HA}	1	—	—	ns
Chip Select Hold Time	t_{HC}	1	—	—	ns
Data Hold Time	t_{HD}	1	—	—	ns

WRITE CYCLE TIMING DIAGRAMS



Parameter	Symbol	Min	Typ	Max	Unit
RISE TIME and FALL TIME					
Output Rise Time	t_r	—	2	—	ns
Output Fall Time	t_f	—	2	—	ns

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 — OUTPIT HIGH VOLTAGE vs AMBIENT TEMPERATURE

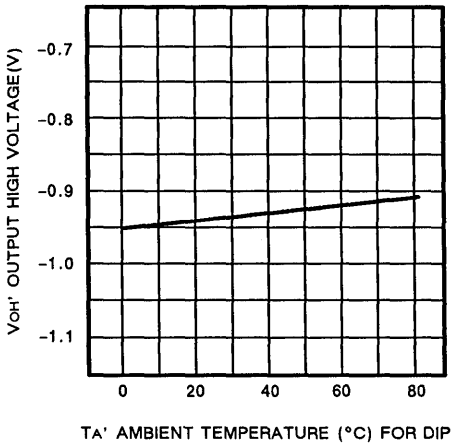


Fig. 4 — OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

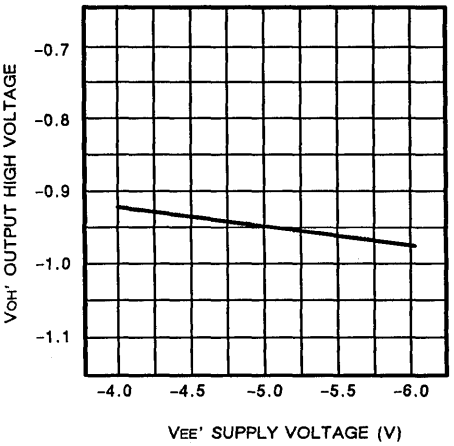


Fig. 5 — OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

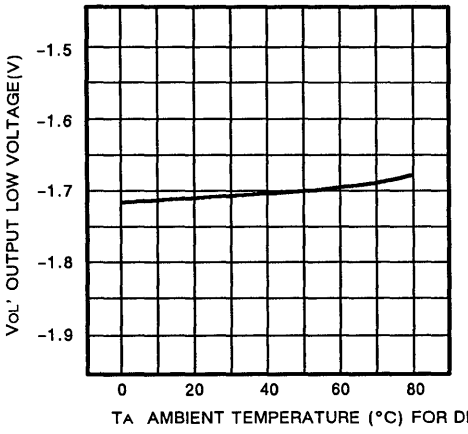
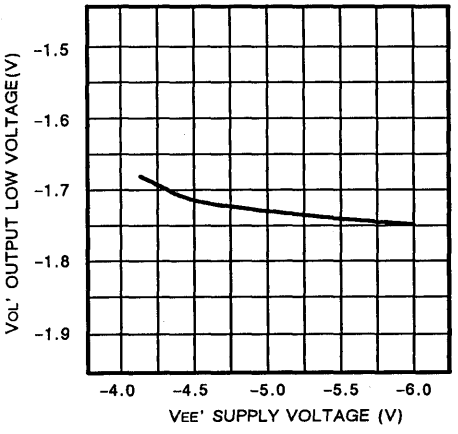


Fig. 6 — OUYPUT LOW VOLTAGE vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 7 — SUPPLY CURRENT vs AMBIENT TEMPERATURE

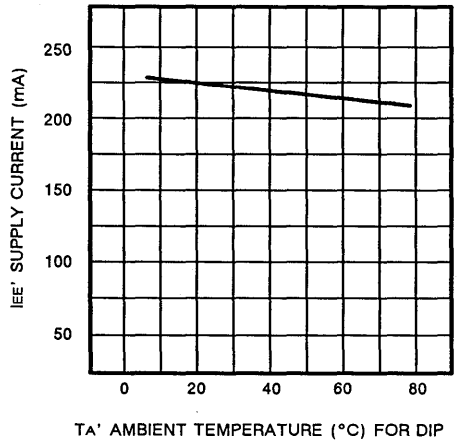


Fig. 8 — SUPPLY CURRENT vs SUPPLY VOLTAGE

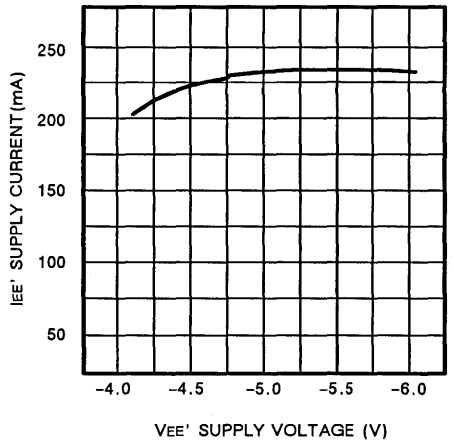


Fig. 9 — ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

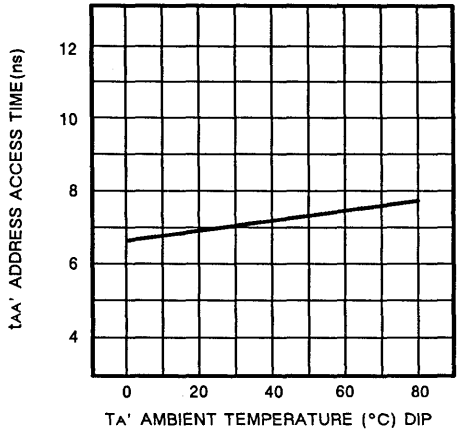
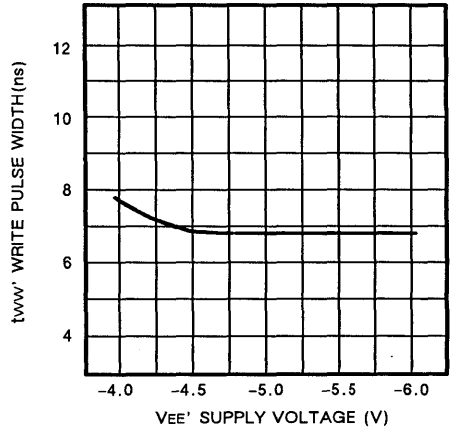


Fig. 10 — ADDESS ACCESS TIME vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 11 — WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

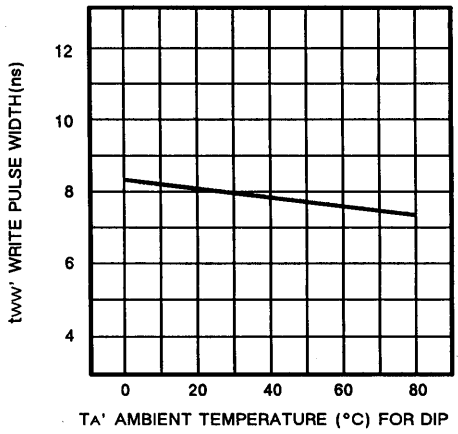
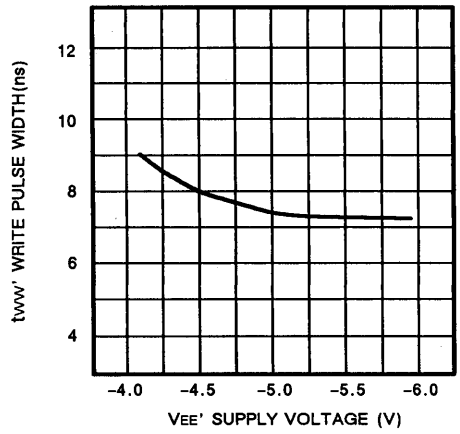
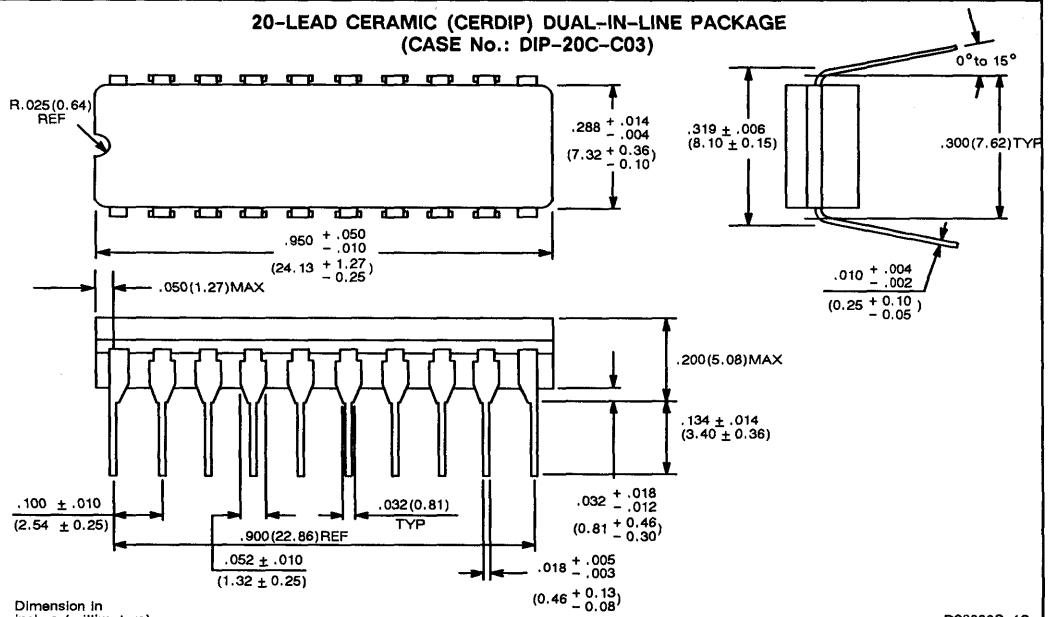


Fig. 12 — WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

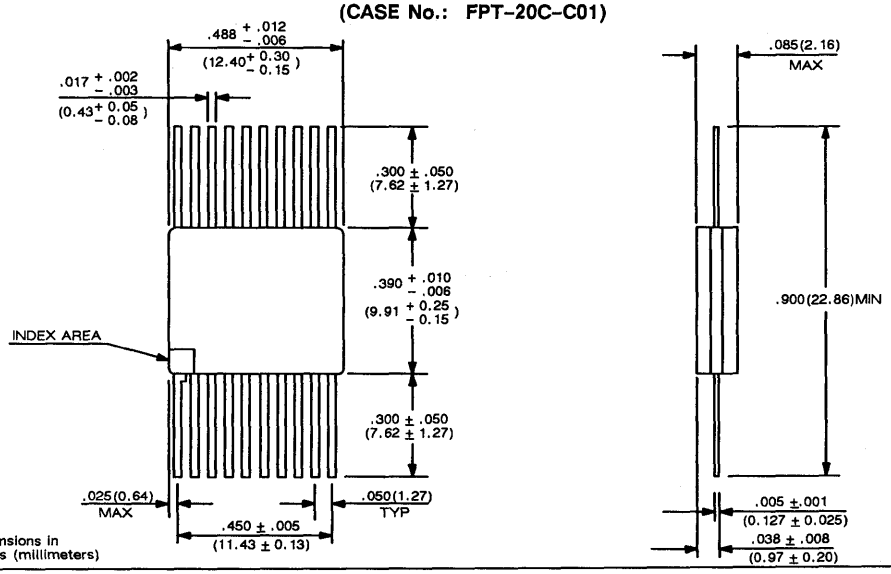
20-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimension in inches (millimeters)

D20006S-4C

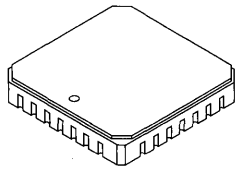
20-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-20C-C01)



Dimensions in inches (millimeters)

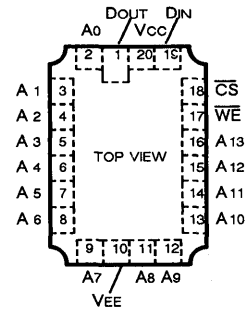
F20004S-2C

PACKAGE DIMENSIONS (Continued)

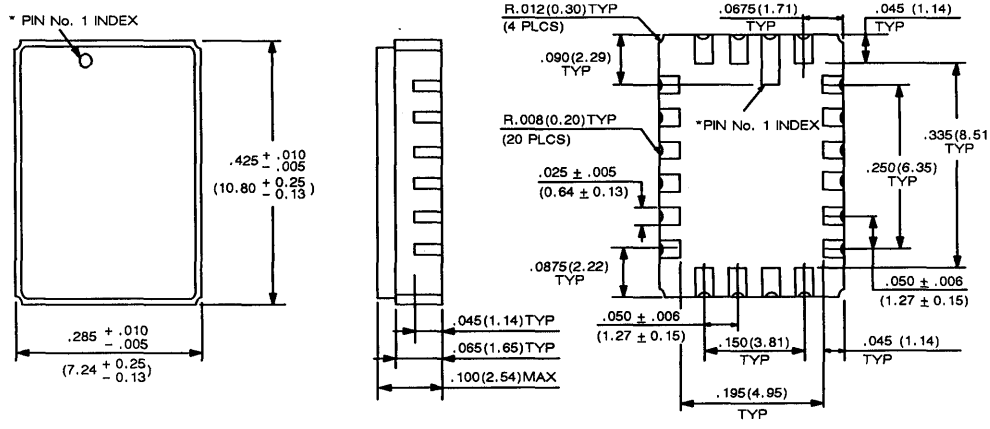


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

C20003S-1C

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100480A-10

May 1988
Edition 1.0

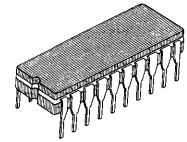
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100480A is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

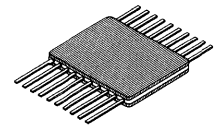
The MBM100480A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) Processing.

Operation for the MBM100480A is specified over a temperature range of from 0°C to 65°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, or LCC. It is fully compatible with industry-standard 100K-series ECL families.

- 16384 words by 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K series ECL families
- Address access time: 8 ns max.
  Chip select access time: 4 ns max.
- Power dissipation: 0.06 mW/bit (typ.)
- Open emitter output for ease of memory expansion
- DOPOS and IOP-II processing



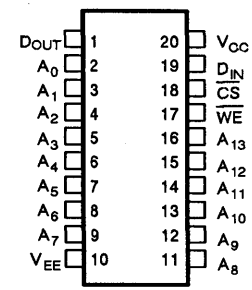
CERAMIC PACKAGE
DIP-20C-C03



CERAMIC PACKAGE
FPT-20C-C01

LCC-20C-F01: See Page 10

PIN ASSIGNMENTS



LCC Pad Configuration: See Page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

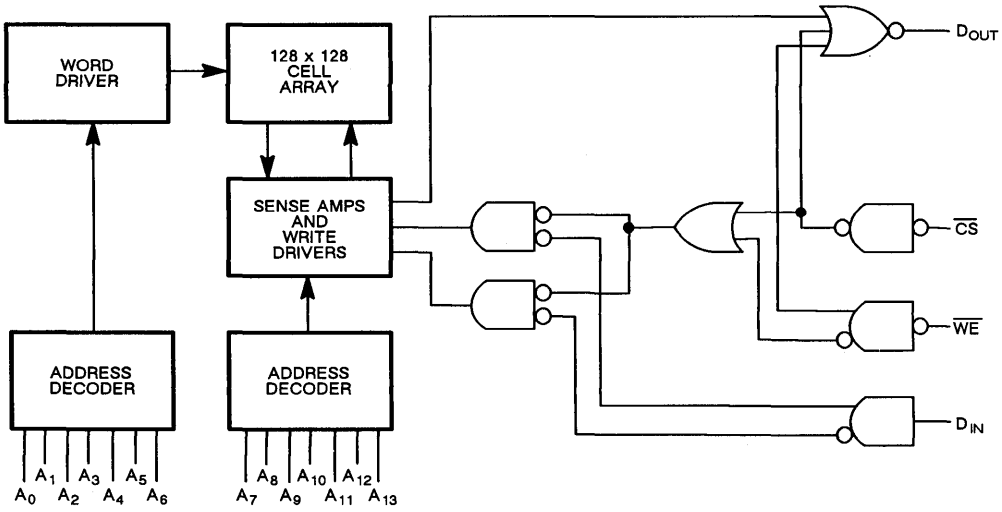
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to **Absolute Maximum Rating** conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

1

Fig. 1 — MBM100480A BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

Notes:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100480A is fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designated A_0 through A_{13}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then trasferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50 Ω and 30 pF to -2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	µA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-220			mA

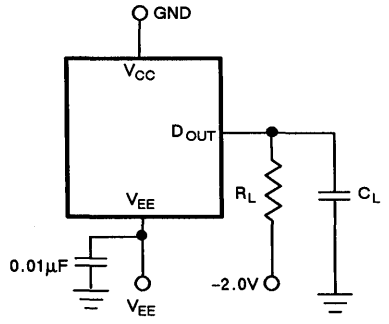
CAPACITANCE

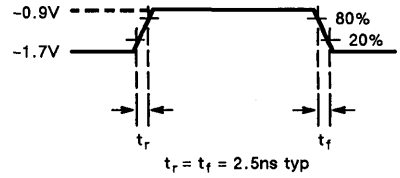
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −4.5 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC Test Conditions





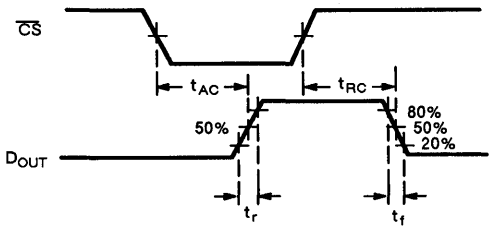
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

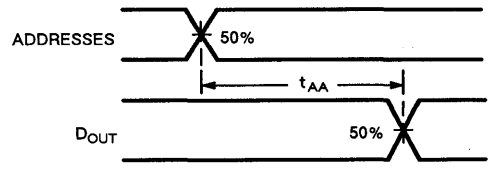
Note: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM100480A-10			Unit
		Min	Typ	Max	
Address Access Time	t_{AA}	2		10	ns
Chip Select Access Time	t_{AC}	1		5	ns
Chip Select Recovery Time	t_{RC}	1		5	ns

READ CYCLE TIMING DIAGRAMS

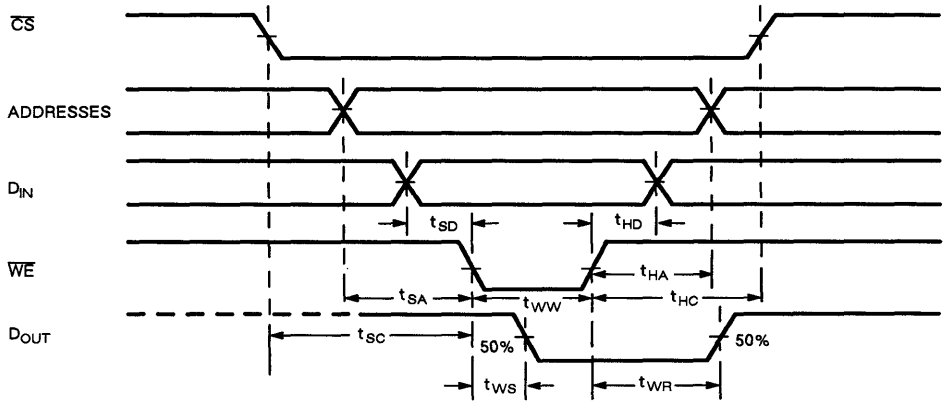




WRITE CYCLE

Parameter	Symbol	MBM100480A-10			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			5	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAMS



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2		ns
Output Fall Time	t_f		2		ns

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Output High Voltage vs Ambient Temperature

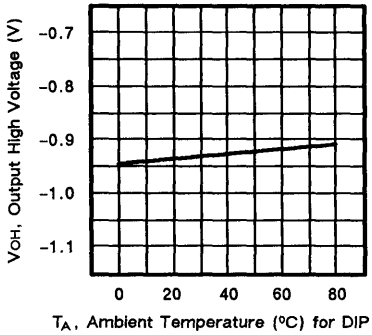


Fig. 4 – Output High Voltage vs Supply Voltage

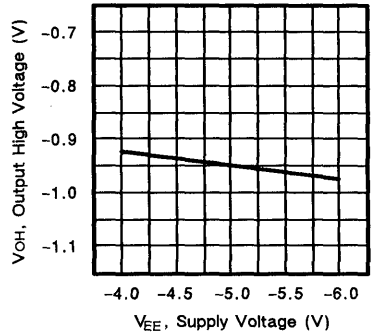


Fig. 5 – Output Low Voltage vs Ambient Temperature

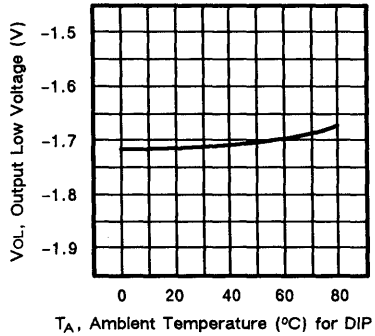


Fig. 6 – Output Low Voltage vs Supply Voltage

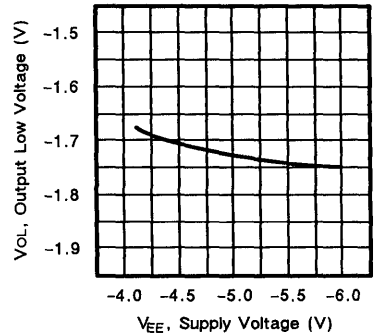


Fig. 7 – Supply Current vs Ambient Temperature

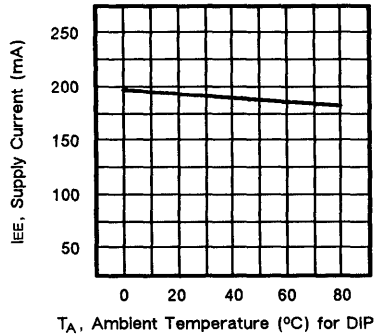
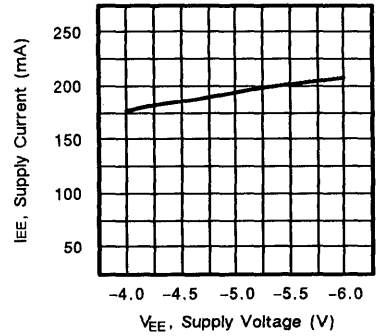


Fig. 8 – Supply Current vs Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 9 – Address Access Time vs Ambient Temperature

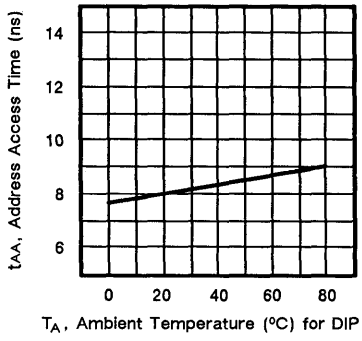


Fig. 10 – Address Access Time vs Supply Voltage

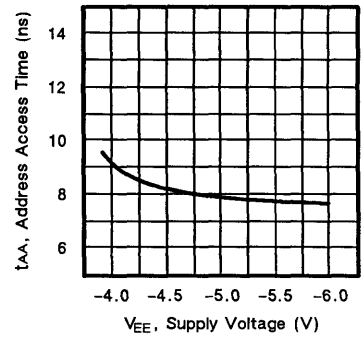


Fig. 11 – Write Pulse Width vs Ambient Temperature

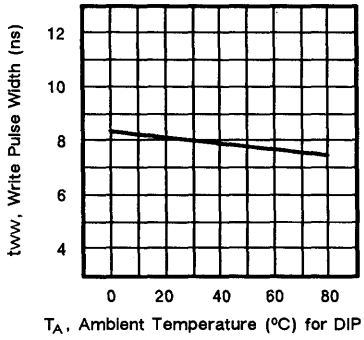
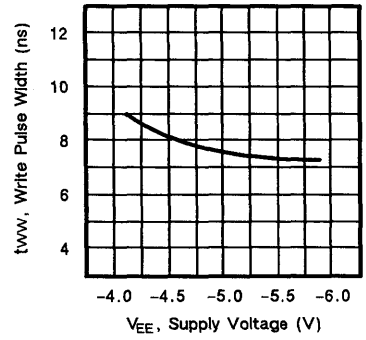
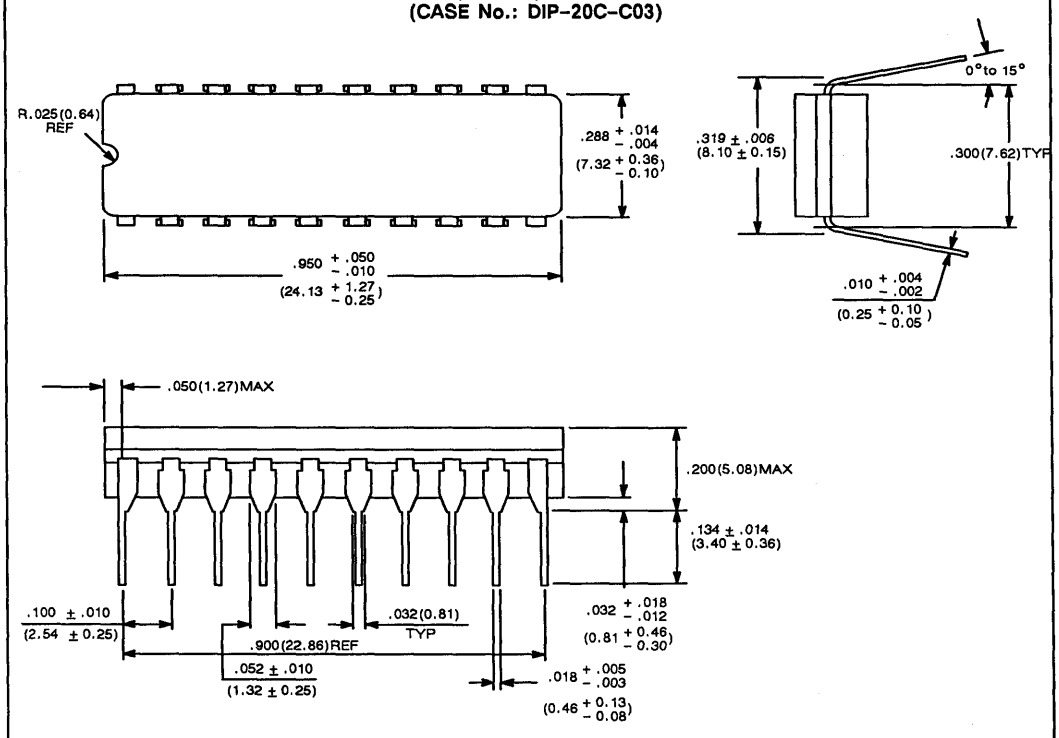


Fig. 12 – Write Pulse Width vs Supply Voltage



PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

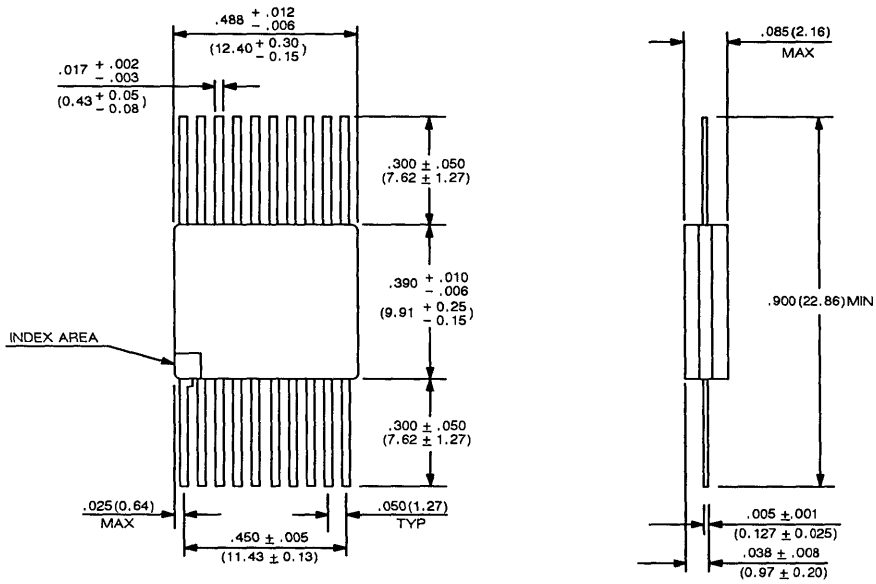


Dimension in inches (millimeters)

D20006S-4C

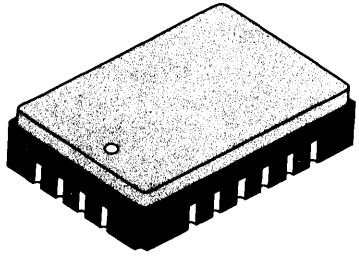
PACKAGE DIMENSIONS (continued)

20-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-20C-C01)



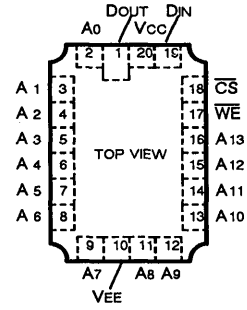
Dimensions in
inches (millimeters)

F20004S-2C

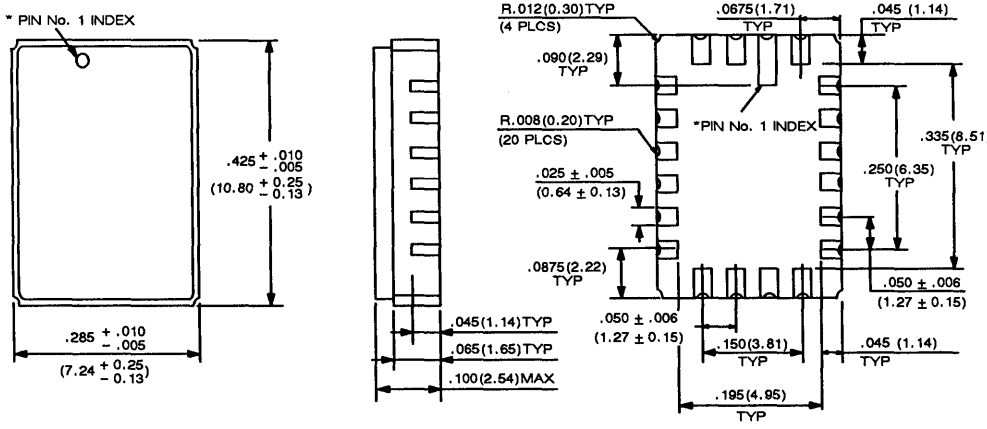


LCC-20C-F01

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F01)



*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimension in
inches (millimeters)

C20003S-1C

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10484-15

February 1988
Edition 2.0

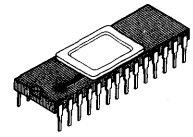
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10484 is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

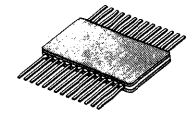
The MBM 10484 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10484 is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package). It also features 28-pin ceramic DIP or Flat package, and is fully compatible with industry-standard 10 K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 15 ns max.
- Chip select access time: 8 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.07 mW/bit typ.
- DOPOS and IOP-II processing

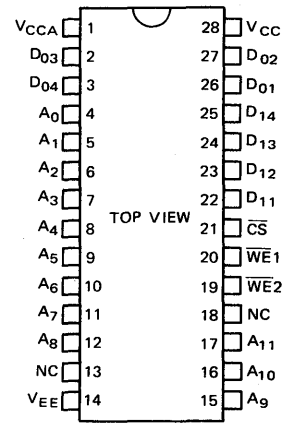


CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

PIN ASSIGNMENT



VCC grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

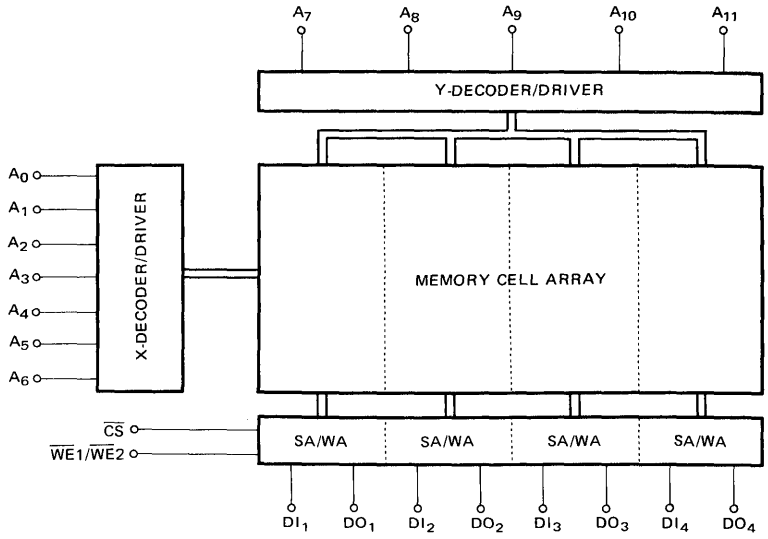
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 10484 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}1/\overline{WE}2$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE}1$ and $\overline{WE}2$ are low.
*H = Either $\overline{WE}1$ or $\overline{WE}2$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM 10484 is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}1/\overline{WE}2$) inputs With both $\overline{WE}1/\overline{WE}2$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE}1$ or $\overline{WE}2$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-240			mA	0°C to 75°C

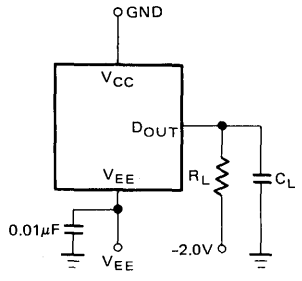
CAPACITANCE

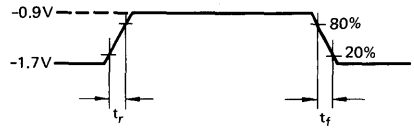
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = –5.2 V ±5%, Output Load = 50 Ω to –2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





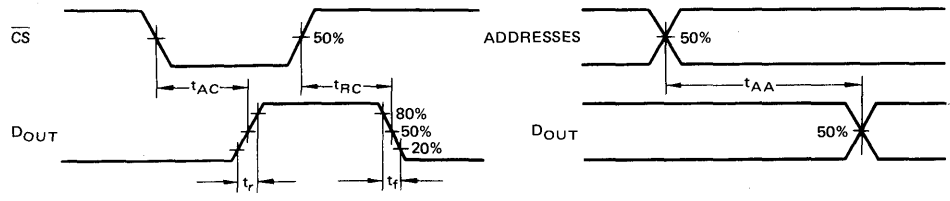
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15	ns
Chip Select Access Time	t_{AC}			8	ns
Chip Select Recovery Time	t_{RC}			8	ns

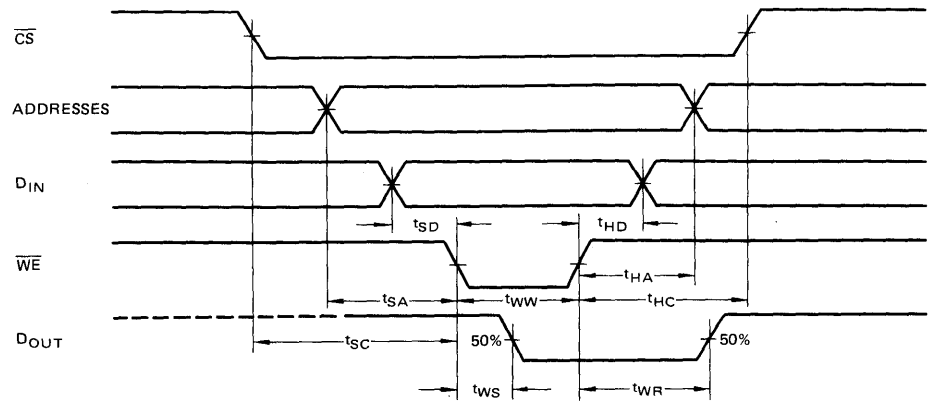
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	15			ns
Write Disable Time	t_{WS}			8	ns
Write Recovery Time	t_{WR}			17	ns
Address Set Up Time	t_{SA}	3			ns
Chip Select Set Up Time	t_{SC}	3			ns
Data Set Up Time	t_{SD}	3			ns
Address Hold Time	t_{HA}	2			ns
Chip Select Hold Time	t_{HC}	2			ns
Data Hold Time	t_{HD}	2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.5		ns
Output Fall Time	t_f		2.5		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

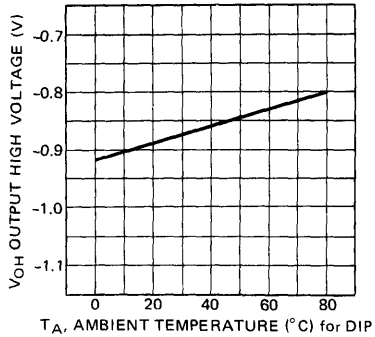


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

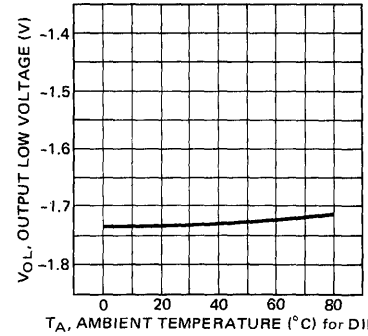


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

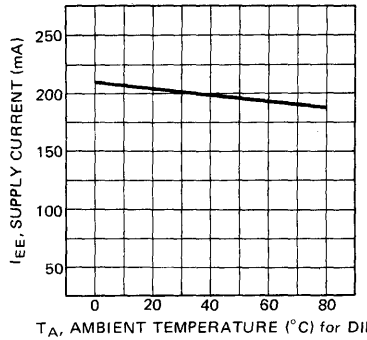


Fig. 6 – SUPPLY CURRENT vs SUPPLY VOLTAGE

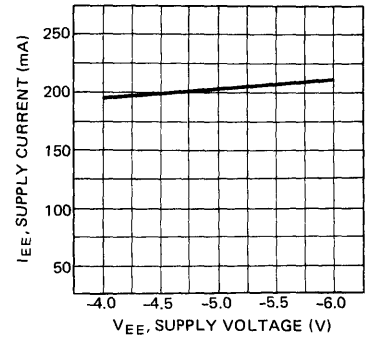


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

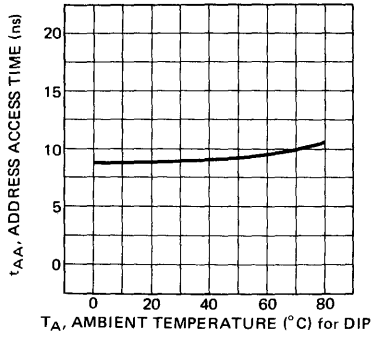


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

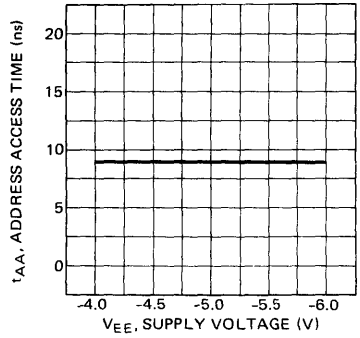


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

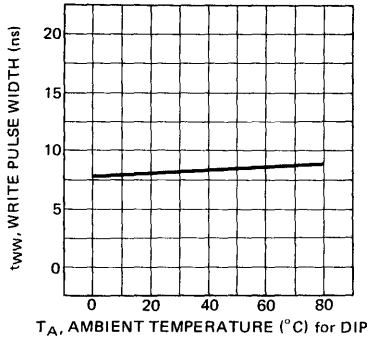
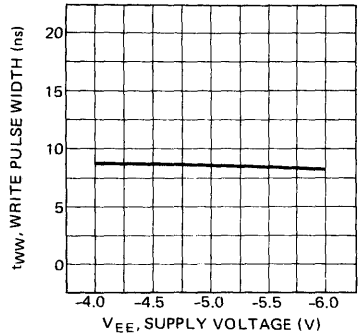
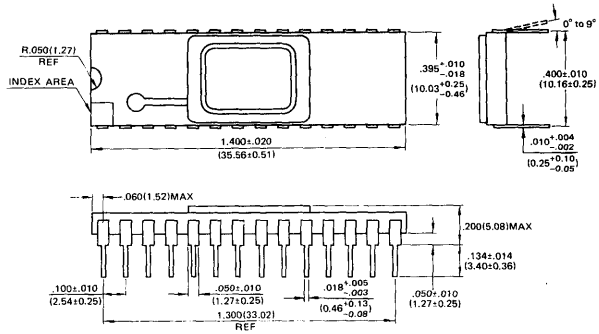


Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



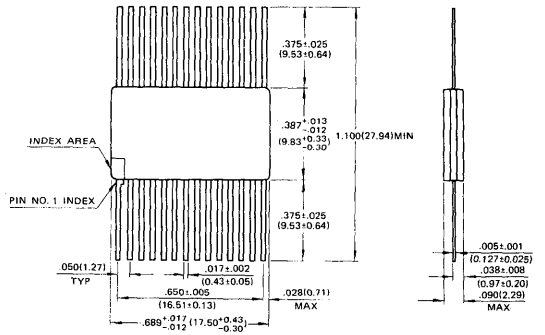
PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



Dimensions in
inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10A484-5

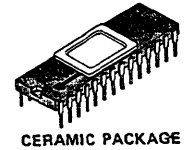
TS313-C886
June, 1988

16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10A484 is fully decoded 16384 bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. The device is organized as 4096 words by 4 bits, and it features on chip voltage compensation for improved noise margin.

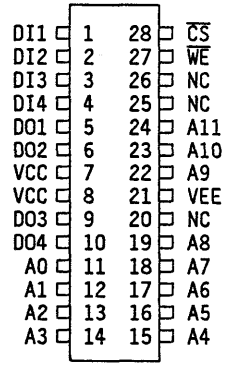
Operation for the MBM10A484 is specified over a temperature range of the Case Temperature (T_C) from 0°C to 75°C. It also features 28-pin Ceramic DIP or Flat Package and is fully compatible with industry standard 10K-series ECL families.

- 4096 words x 4 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standard 10K series ECL families
- Address access time: 5ns max
  Chip select access time: 3ns max
- Power dissipation: -300 mA min
- Open emitter output for ease of memory expansion



CERAMIC PACKAGE
DIP-28C-A06

CERAMIC PACKAGE
FPT-28C-C03



PIN ASSIGNMENTS

ABSOLUTE MAXIMUM RATINGS (See NOTE)

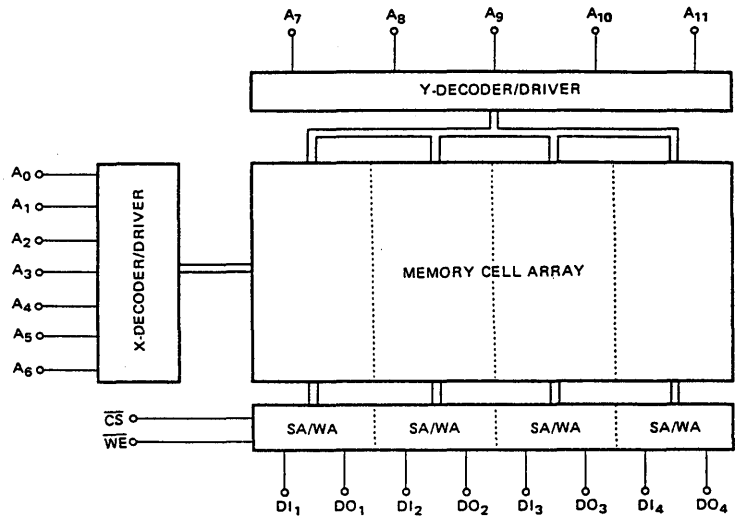
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -6.0	V
Input Voltage	V_{IN}	+0.5 to -2.0	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional ooperation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig.1 - MBM10A484 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10A484 is fully decoded 16384 bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designed A0 through A11. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{WE}$ input. With both $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS
(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (TC)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS
(VCC=0V, VEE=-5.2V, Output Load=50Ω to -2.0V, TC=0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°Cto75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°Cto75°C
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA	0°Cto75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-300			mA	0°Cto75°C

AC CHARACTERISTICS
(VCC=0V, VEE=-4.5V±5%, Output Load=50Ω to -2.0V, T_C=0°C to 85°C, unless otherwise noted.)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			5	ns
Chip Select Access Time	t_{AC}			3	ns
Chip Select Recovery Time	t_{RC}			3	ns

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	TBD			ns
Write Disable Time	t_{WS}			3	ns
Write Recovery Time	t_{WR}			TBD	ns
Address Set Up Time	t_{SA}	1			ns
Chip Select Set Up Time	t_{SC}	1			ns
Data Set Up Time	t_{SD}	1			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

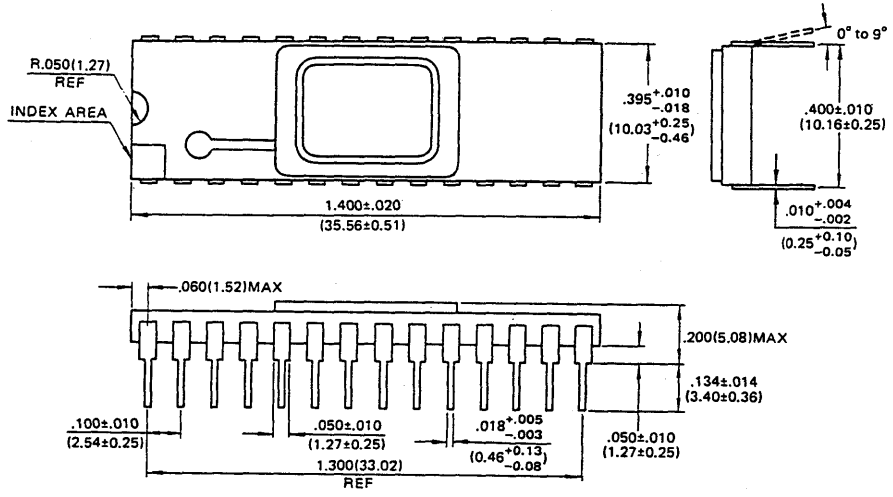
All timing measurement is referenced to 50% input and output levels.

RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

PACKAGE DIMENSIONS

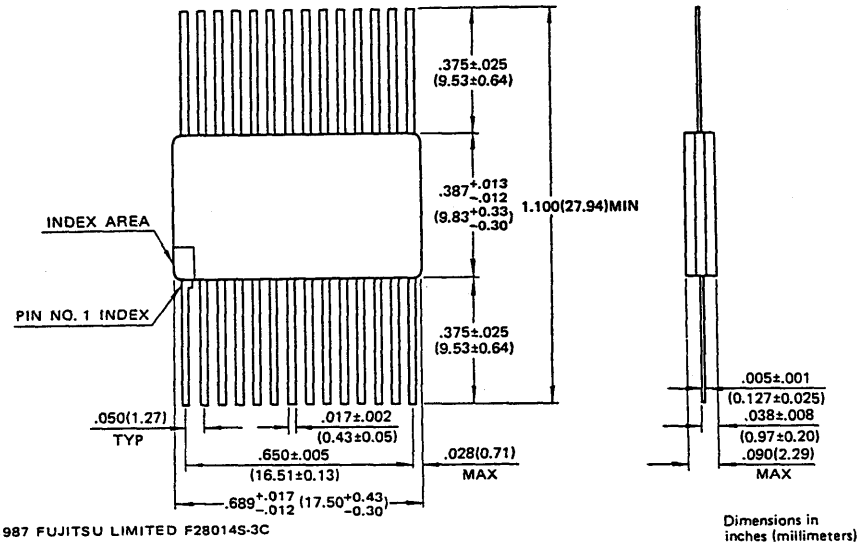
28-LEAD CERAMIC (METAL-SEAL) DUAL IN-LINE PACKAGE
(CASE NO.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE NO.: FPT-28C-C03)



Dimensions in inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10484A-8

August 1988
Edition 2.0

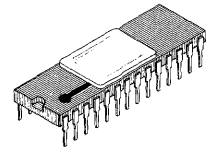
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

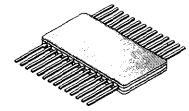
The MBM 10484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10484A is specified over a temperature range of from 0°C to 55°C (T_A for DIP T_C for Flat Package and LCC). It also features 28-pin ceramic DIP, Flat package, or LCC and is fully compatible with industry-standard 10K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 8 ns max.
- Chip select access time: 4 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.10 mW/bit typ.
- DOPOS and IOP-II processing



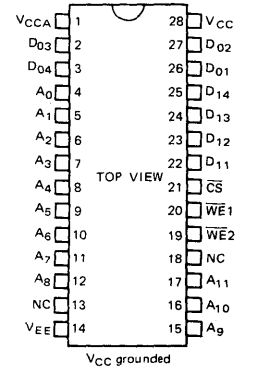
CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

LCC-28C-F02: See Page 10

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

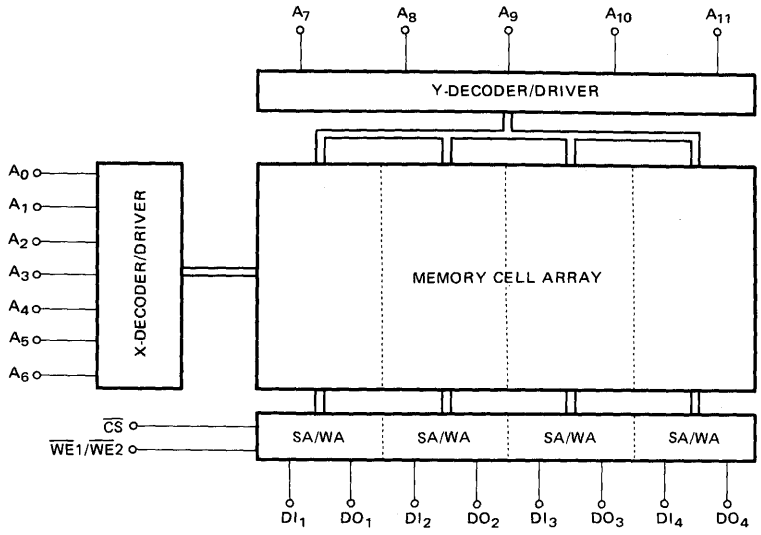
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 10484A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE1}/\overline{WE2}$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE1}$ and $\overline{WE2}$ are low.
*H = Either $\overline{WE1}$ or $\overline{WE2}$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM10484A is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE1}/\overline{WE2}$) inputs With both $\overline{WE1}/\overline{WE2}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE1}$ or $\overline{WE2}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 55°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 55°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 55°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 55°C
Output Low Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 55°C
Output High Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 55°C
Output Low Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 55°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 55°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 55°C
Input High Current ($V_{IN} = V_{IH\ max}$)	I_{IH}			220	μA	0°C to 55°C
Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 55°C
$\overline{CS}$ Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 55°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-330			mA	0°C to 55°C

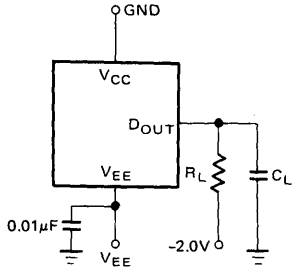
CAPACITANCE

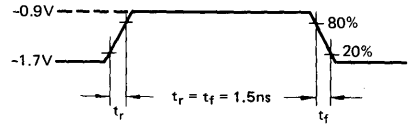
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}			4	pF
Output Pin Capacitance	C_{OUT}			6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 55°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 55°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





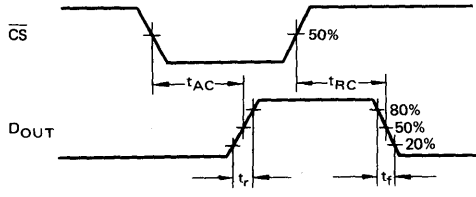
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

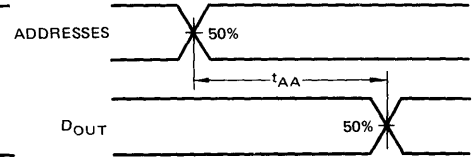
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			8	ns
Chip Select Access Time	t_{AC}			4	ns
Chip Select Recovery Time	t_{RC}			4	ns

READ CYCLE TIMING DIAGRAMS

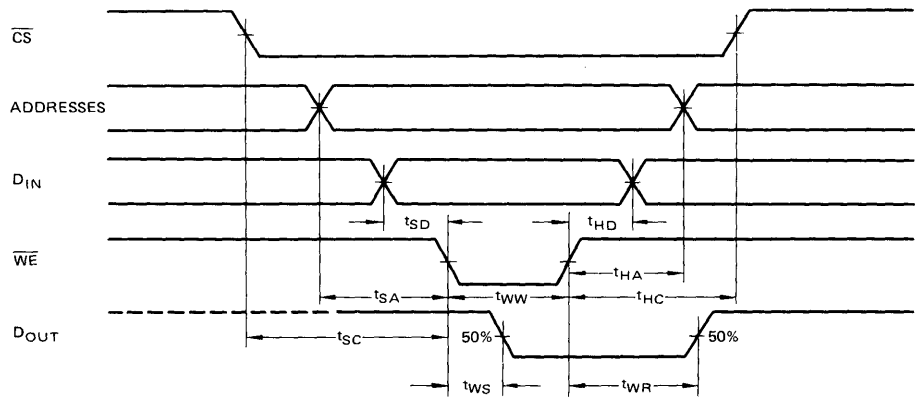




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			4	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

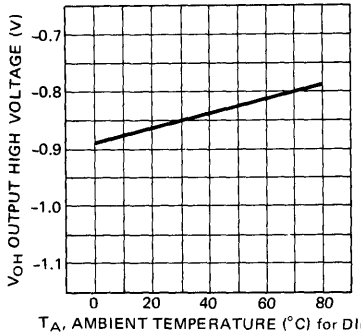


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

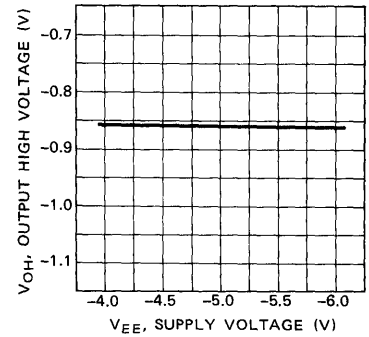


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

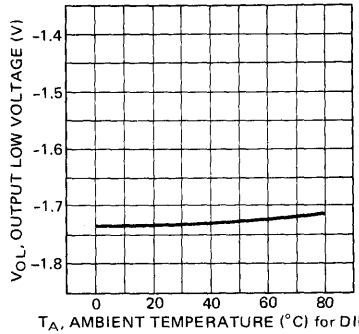


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

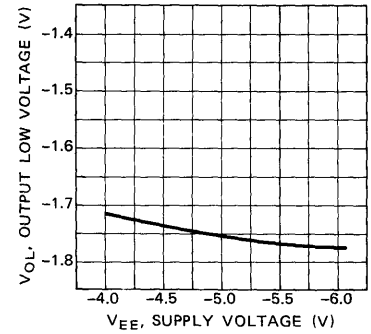


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

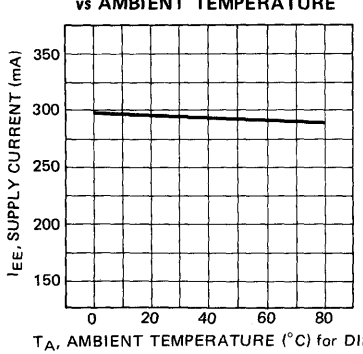


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

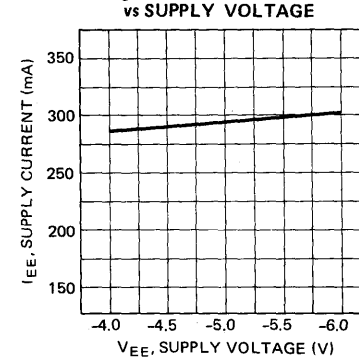


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

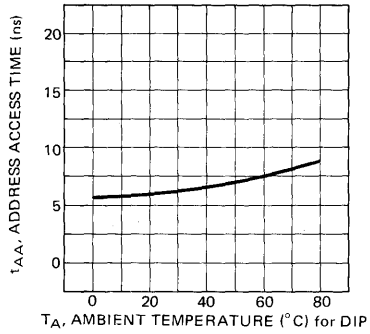


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

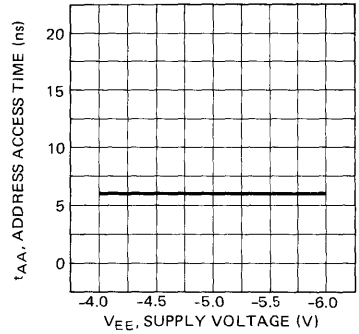


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

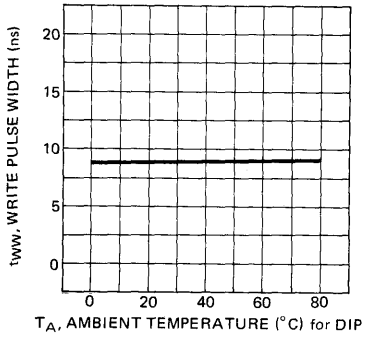
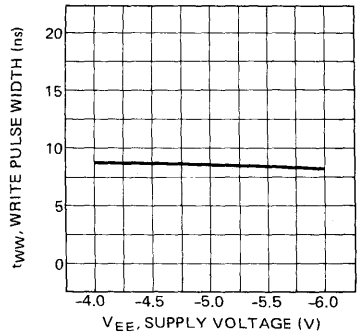
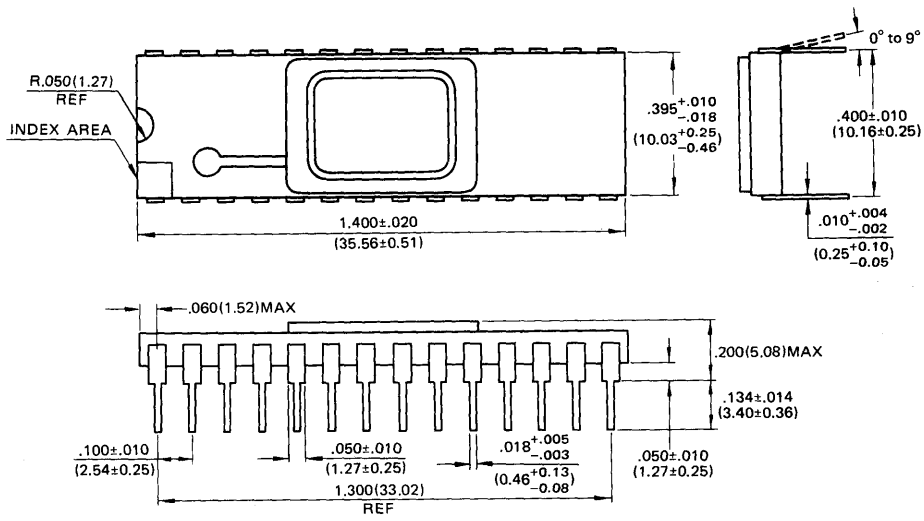


Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

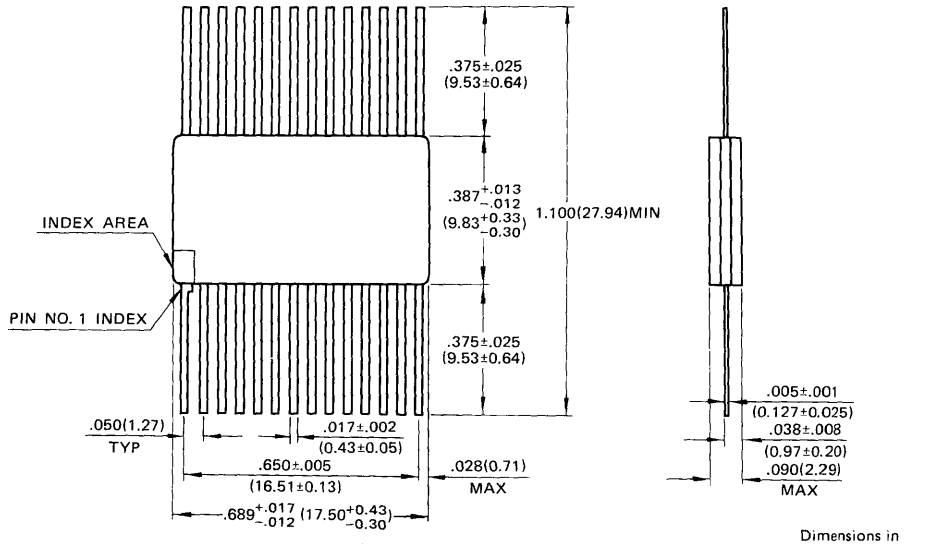
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

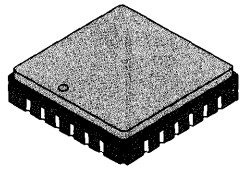
PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



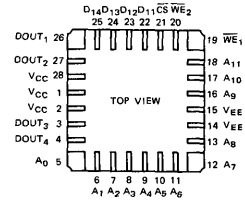
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

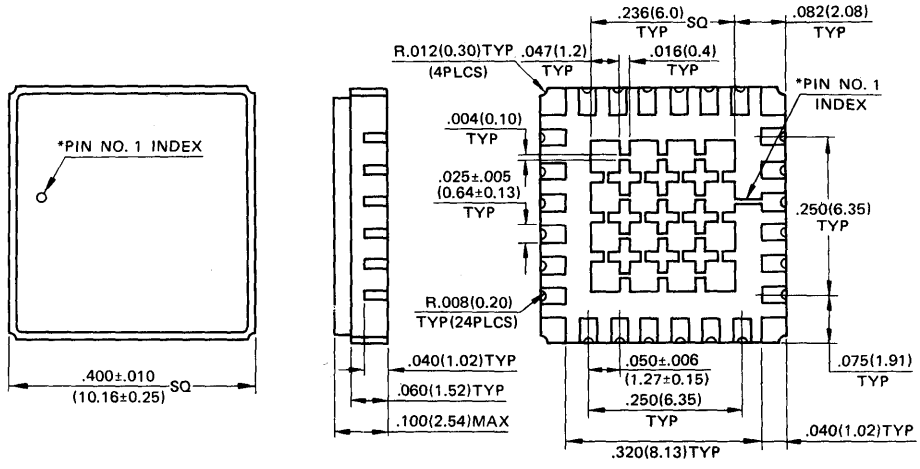


LCC-28C-F02

PAD CONFIGURATION



28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10484A-10

August 1988
Edition 2.0

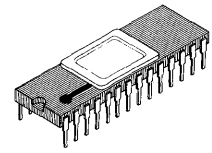
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

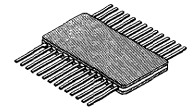
The MBM 10484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high hields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10484A is specified over a temperature range of from 0°C to 75°C (T_A for DIP T_C for Flat Package and LCC). It also features 28-pin ceramic DIP, Flat package, or LCC and is fully compatible with industry-standard 10K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry-standard 10 K-series ECL families
- Address access time: 10 ns max.
- Chip select access time: 5 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.07 mW/bit typ.
- DOPOS and IOP-II processing



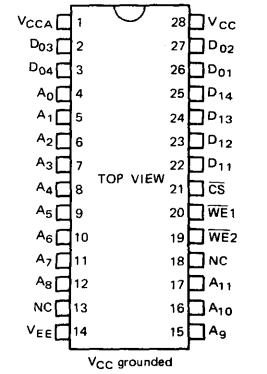
CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

LCC-28C-F01 : See Page 10
LCC-28C-F02 : See Page 11

PIN ASSIGNMENT



See Page 10
LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

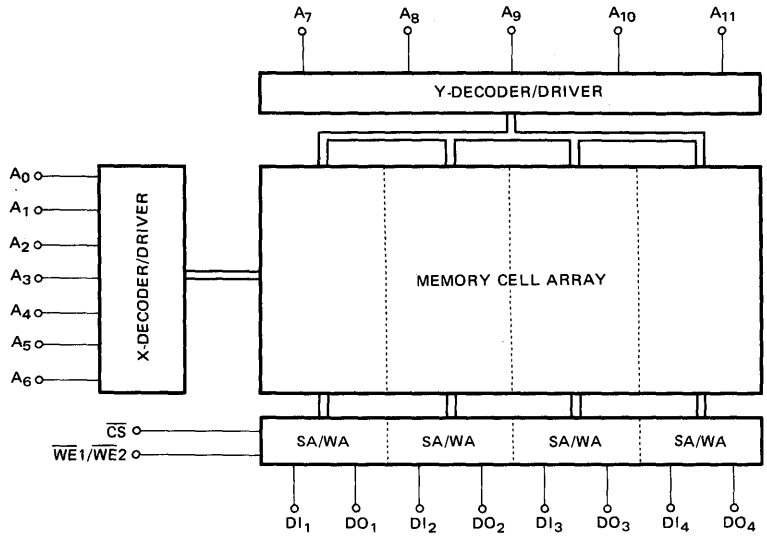
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 10484A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE1}/\overline{WE2}$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE1}$ and $\overline{WE2}$ are low.
*H = Either $\overline{WE1}$ or $\overline{WE2}$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM10484A is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE1}/\overline{WE2}$) inputs With both $\overline{WE1}/\overline{WE2}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE1}$ or $\overline{WE2}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-260			mA	0°C to 75°C

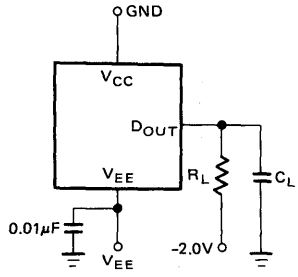
CAPACITANCE

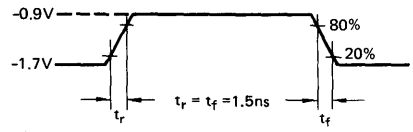
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}			4	pF
Output Pin Capacitance	C_{OUT}			6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V ±5%, Output Load = 50 Ω to -2.0 V and 30 pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





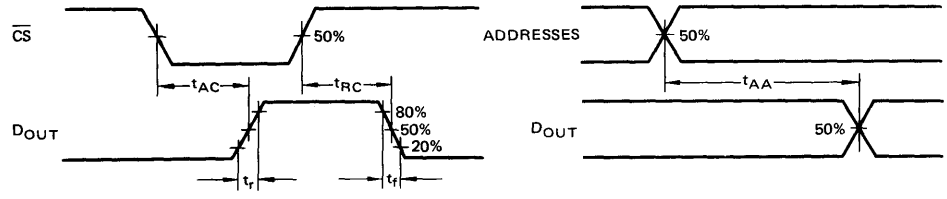
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	2		10	ns
Chip Select Access Time	t_{AC}	1		5	ns
Chip Select Recovery Time	t_{RC}	1		5	ns

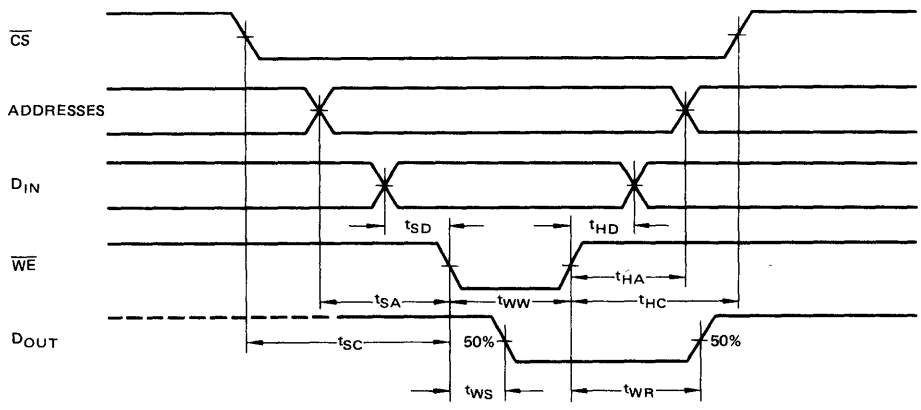
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			5	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

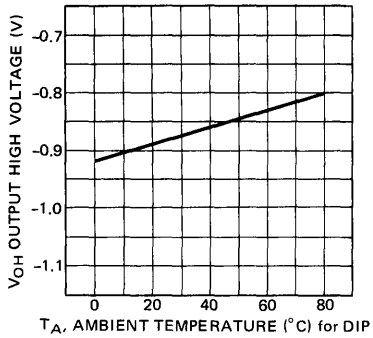


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

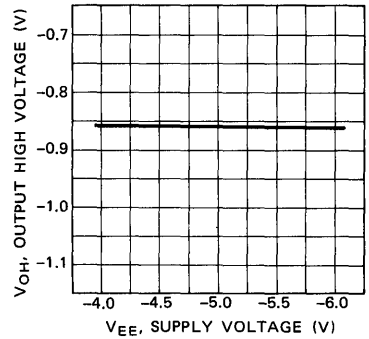


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

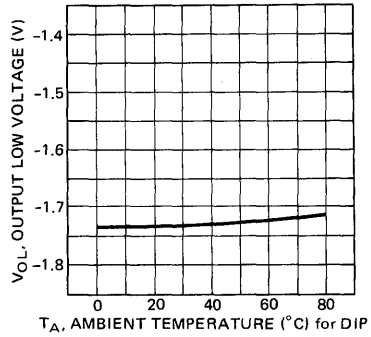


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

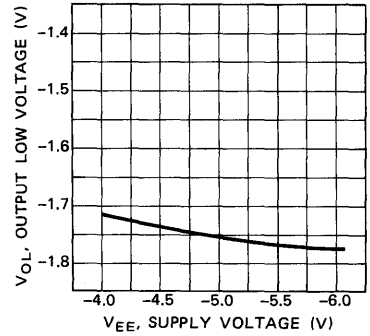


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

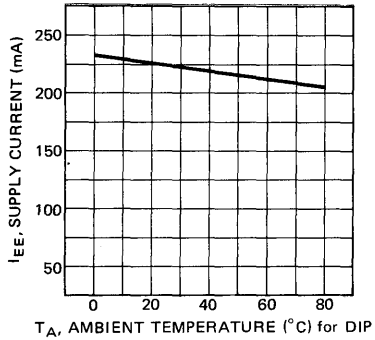


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

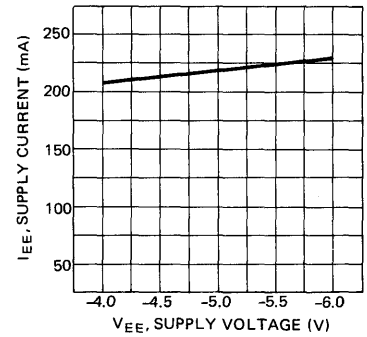


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

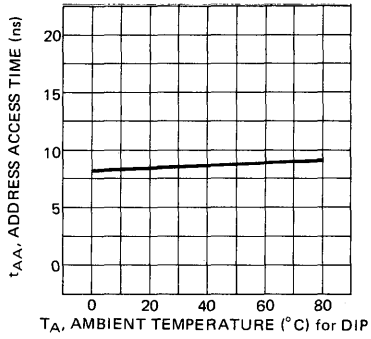


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

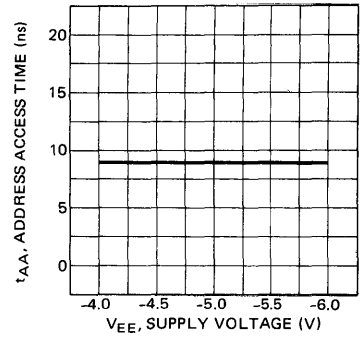


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

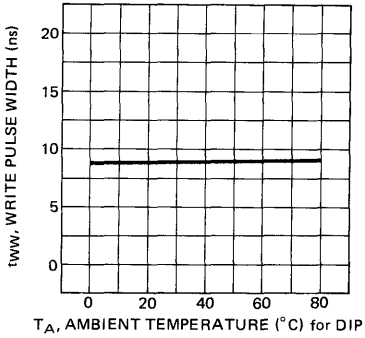
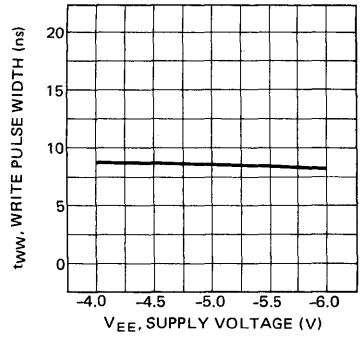


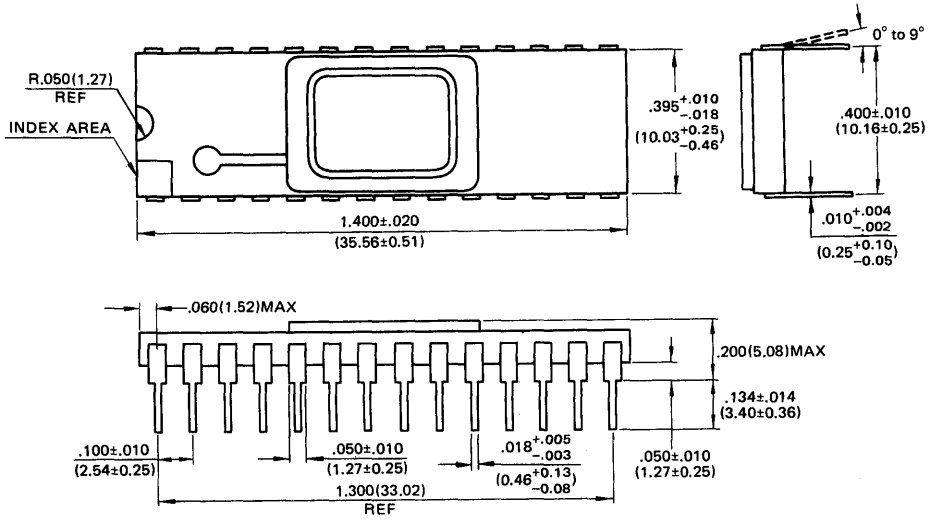
Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



1

PACKAGE DIMENSIONS

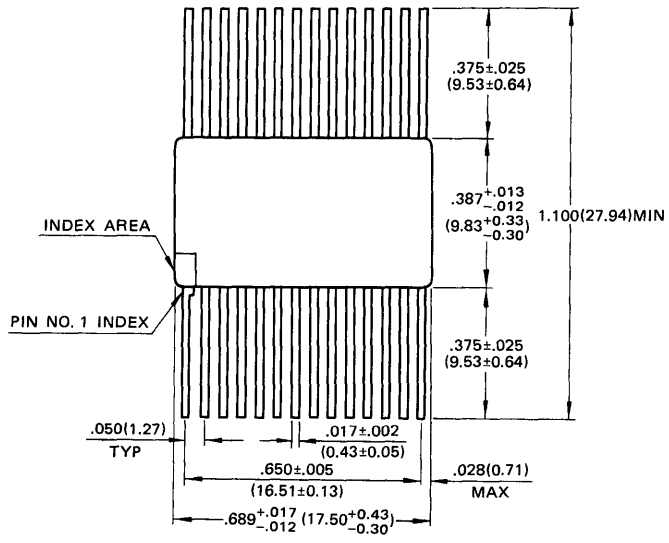
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

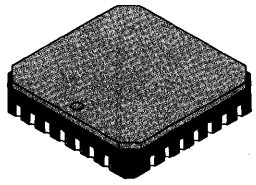
1

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



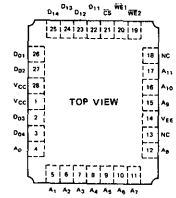
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

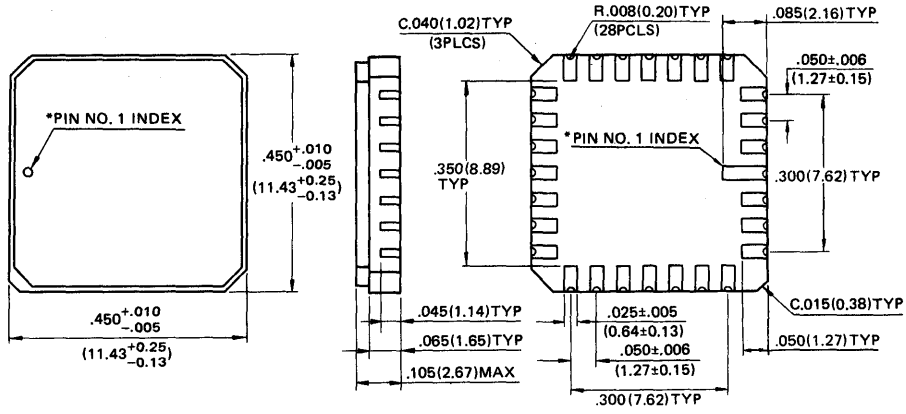


LCC-28C-F01

PAD CONFIGURATION

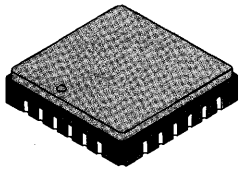


28-PAD CERAMIC (FRIT SEAL) LEADLE$S CHIP CARRIER
(CASE No.: LCC-28C-F01)



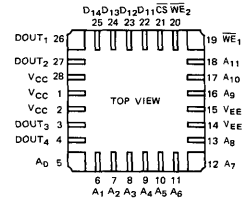
*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in
inches (millimeters)

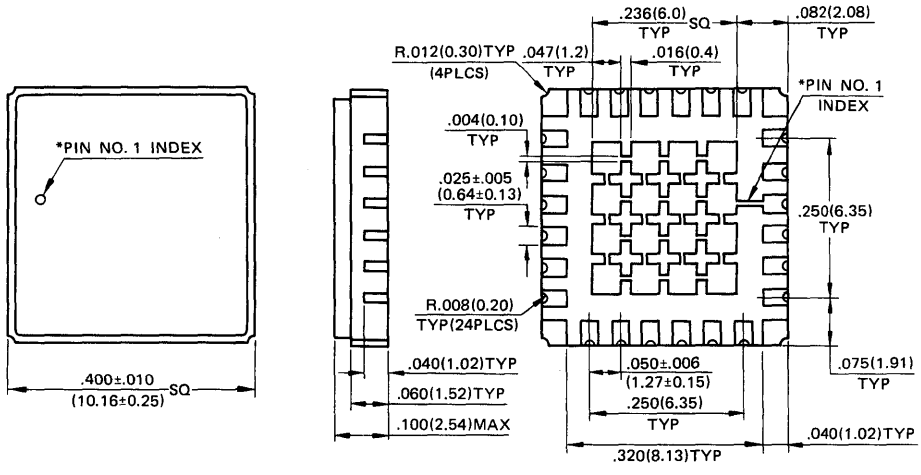


LCC-28C-F02

PAD CONFIGURATION



28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER (CASE No.: LCC-28C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100484-15

February 1988
Edition 2.0

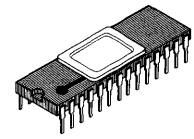
16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100484 is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

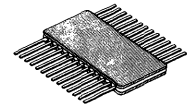
The MBM 100484 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100484 is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package). It also features 28-pin DIP or Flat package, and is fully compatible with industry-standard 100 K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 15 ns max.
- Chip select access time: 8 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation: 0.06 mW/bit typ.
- DOPOS and IOP-II processing

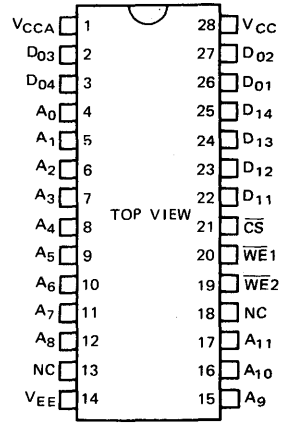


CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

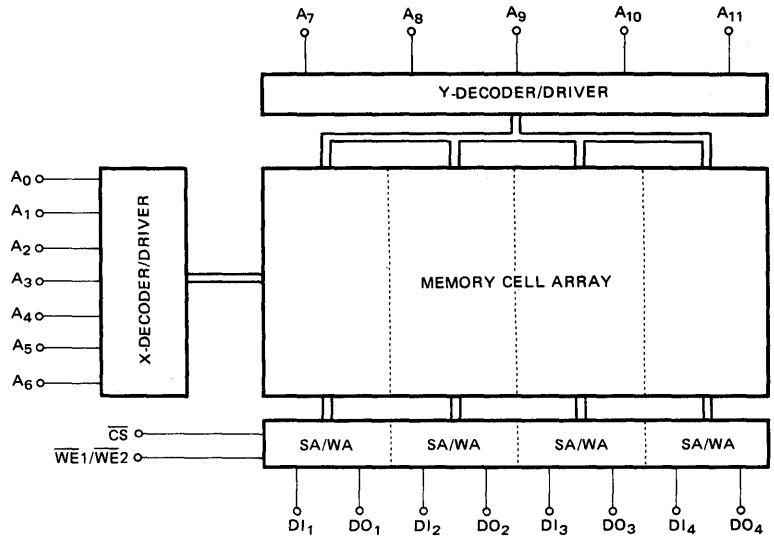
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 100484 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE1}/\overline{WE2}$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE1}$ and $\overline{WE2}$ are low.
*H = Either $\overline{WE1}$ or $\overline{WE2}$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM 100484 is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE1}/\overline{WE2}$) inputs. With both $\overline{WE1}/\overline{WE2}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE1}$ or $\overline{WE2}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-240			mA

CAPACITANCE

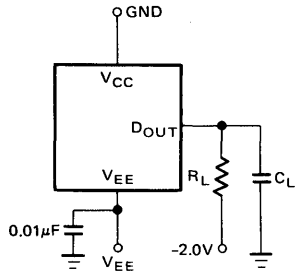
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

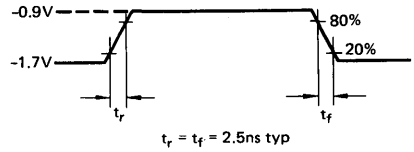
1

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −4.5 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

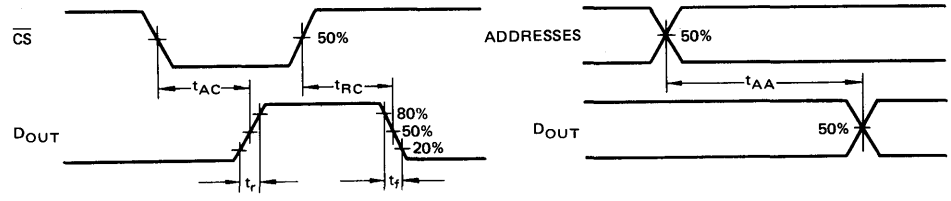
Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15	ns
Chip Select Access Time	t_{AC}			8	ns
Chip Select Recovery Time	t_{RC}			8	ns

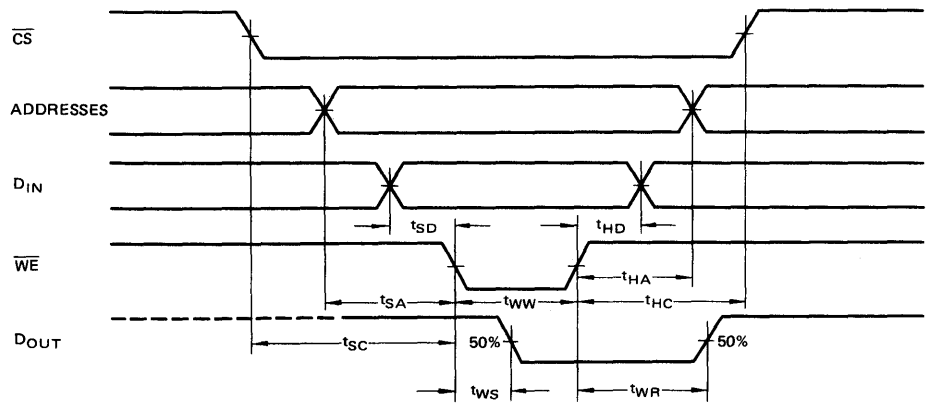
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	15			ns
Write Disable Time	t_{WS}			8	ns
Write Recovery Time	t_{WR}			17	ns
Address Set Up Time	t_{SA}	3			ns
Chip Select Set Up Time	t_{SC}	3			ns
Data Set Up Time	t_{SD}	3			ns
Address Hold Time	t_{HA}	2			ns
Chip Select Hold Time	t_{HC}	2			ns
Data Hold Time	t_{HD}	2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.5		ns
Output Fall Time	t_f		2.5		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

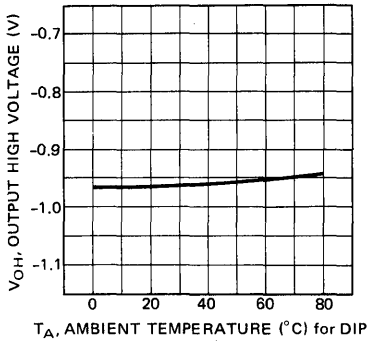


Fig. 4 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

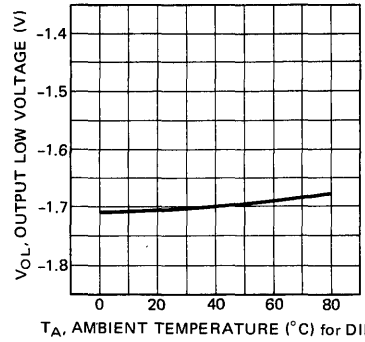


Fig. 5 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

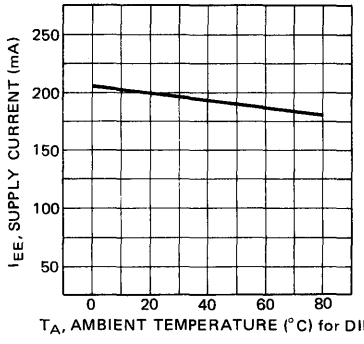


Fig. 6 – SUPPLY CURRENT vs. SUPPLY VOLTAGE

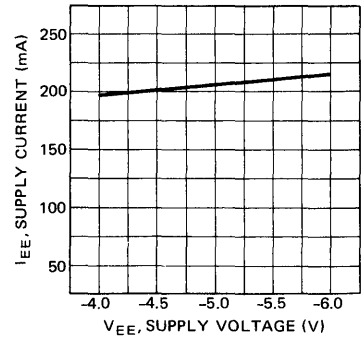


Fig. 7 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

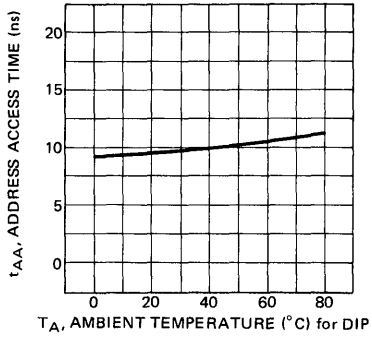


Fig. 8 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

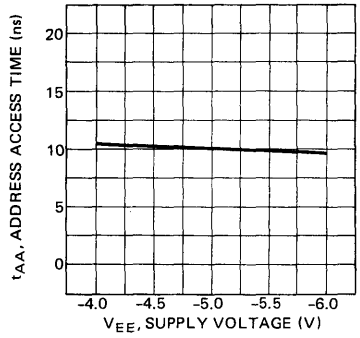


Fig. 9 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

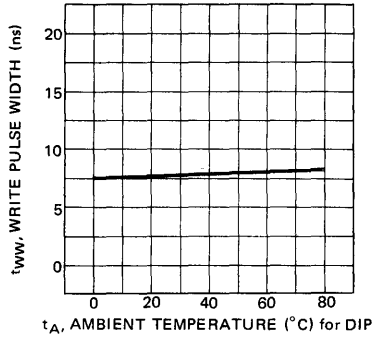
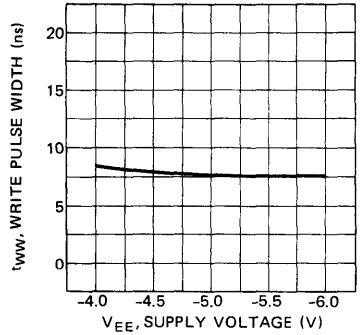
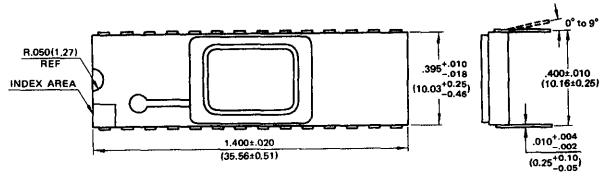


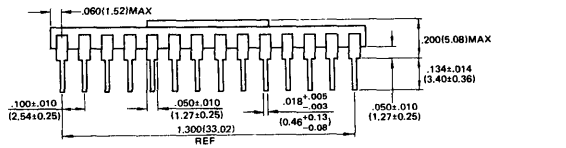
Fig. 10 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

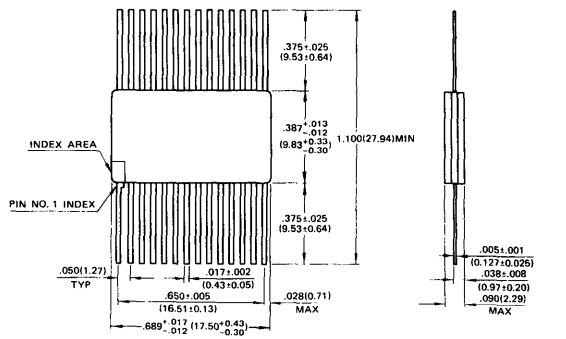
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)





Dimensions in
inches and (millimeters)

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



Dimensions in
inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100484A-8

August 1988
Edition 2.0

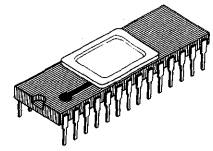
16384-BIT BIPPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

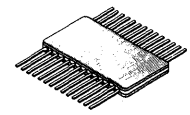
The MBM 100484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100484A is specified over a temperature range of from 0°C to 65°C (T_A for DIP, T_C for Flat Package and LCC). It also features 28-pin DIP or Flat package and LCC, and is fully compatible with industry-standard 100K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 8 ns max.
- Chip select access time: 4 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation: 0.091 mW/bit typ.
- DOPOS and IOP-II processing



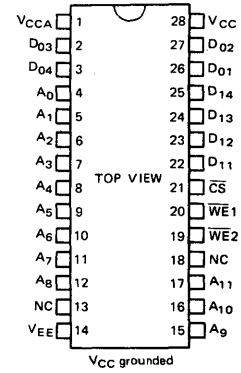
CERAMIC PACKAGE
DIP-28C-A06



CERAMIC PACKAGE
FPT-28C-C03

LCC-28C-F02: See Page 10

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

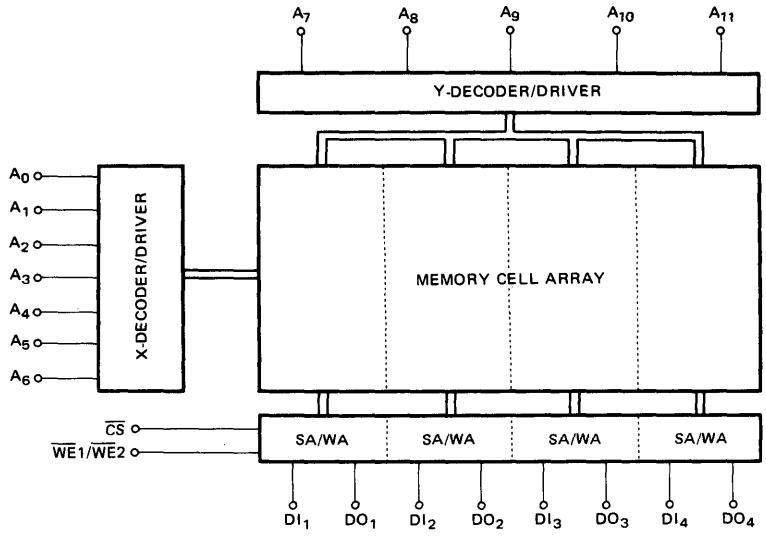
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 100484A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE1}/\overline{WE2}$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE1}$ and $\overline{WE2}$ are low.
*H = Either $\overline{WE1}$ or $\overline{WE2}$ is high.

H = High Voltage Level
L = Low Voltage Level
X = *Don't care*

FUNCTIONAL DESCRIPTION

The Fujits MBM 100484A is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE1}/\overline{WE2}$) inputs. With both $\overline{WE1}/\overline{WE2}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE1}$ or $\overline{WE2}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambinet Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 65°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 65°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 65°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-330			mA

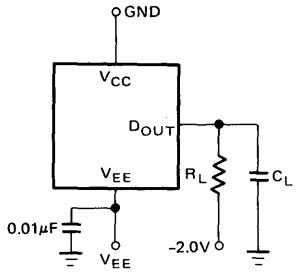
CAPACITANCE

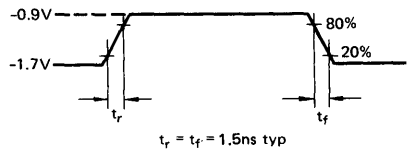
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}			4	pF
Output Pin Capacitance	C_{OUT}			6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −4.5 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 65°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 65°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f = 1.5$ns typ

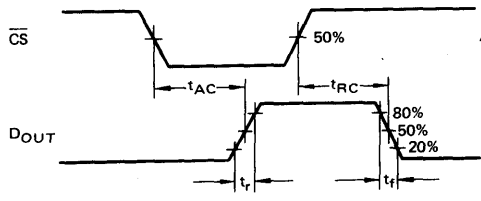
Output Load: $R_L = 50\Omega$
C_L = 30pF
(including jig and stray capacitance)

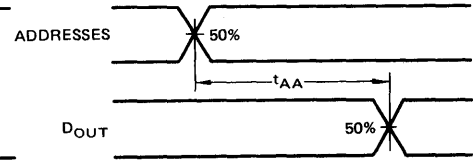
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			8	ns
Chip Select Access Time	t_{AC}			4	ns
Chip Select Recovery Time	t_{RC}			4	ns

READ CYCLE TIMING DIAGRAMS

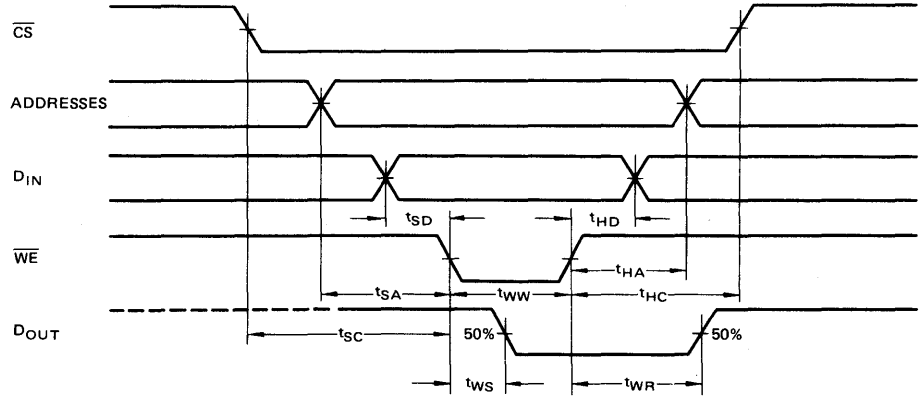




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			4	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

1

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

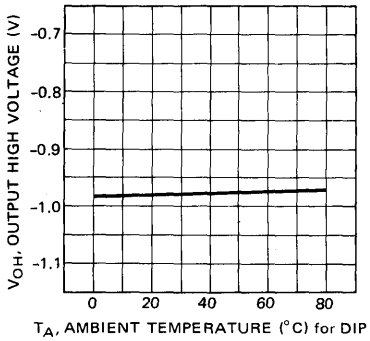


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

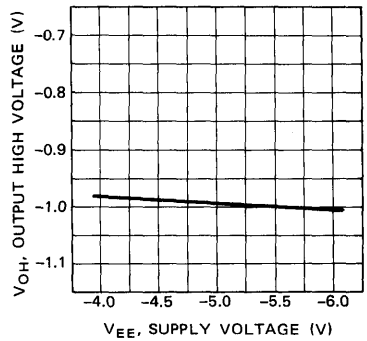


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

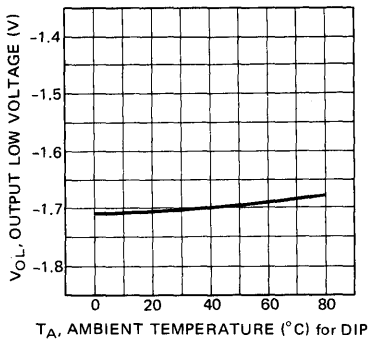


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

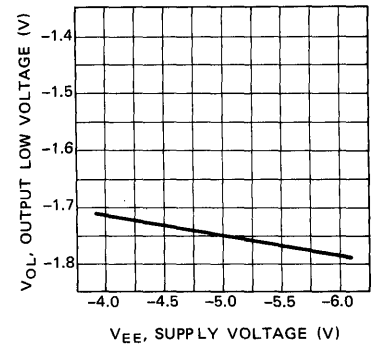


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

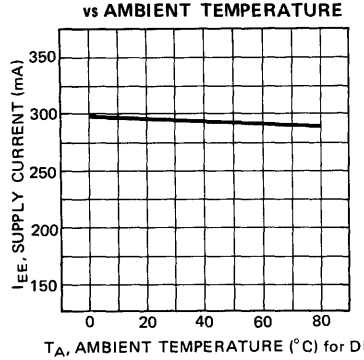


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

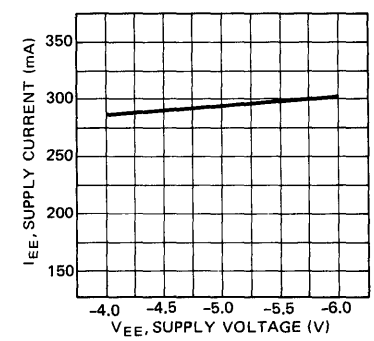


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

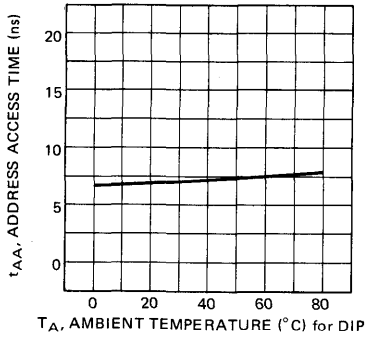


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

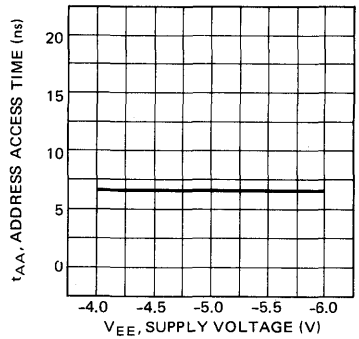


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

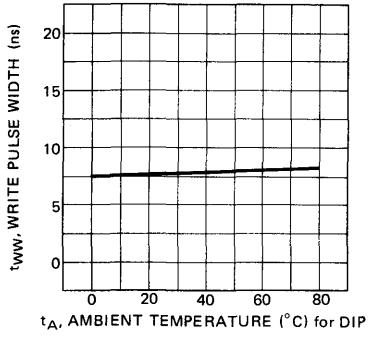
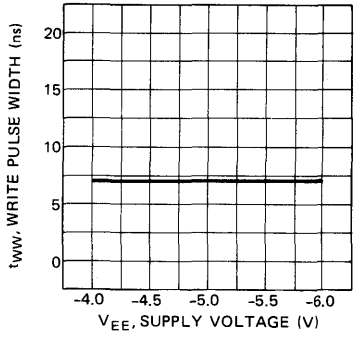
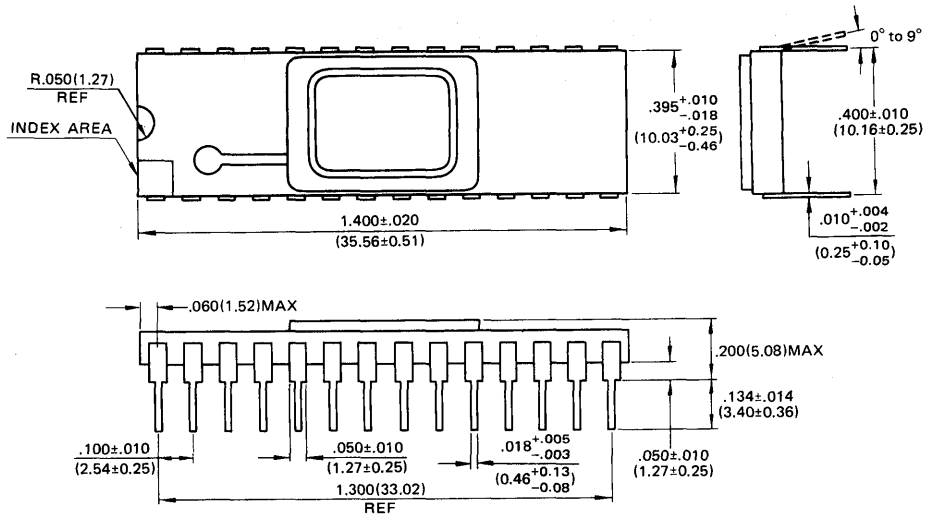


Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

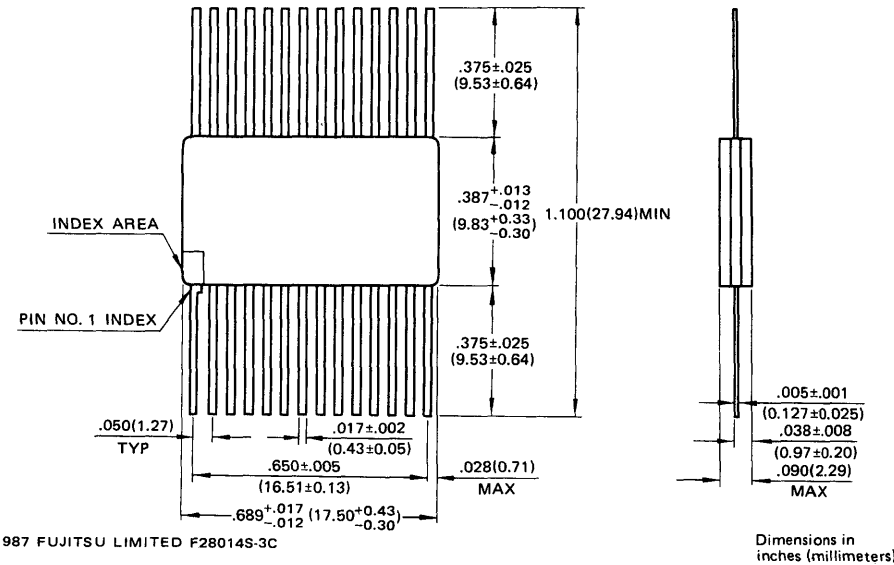
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

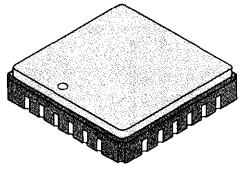
PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



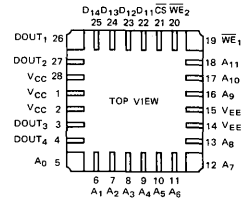
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

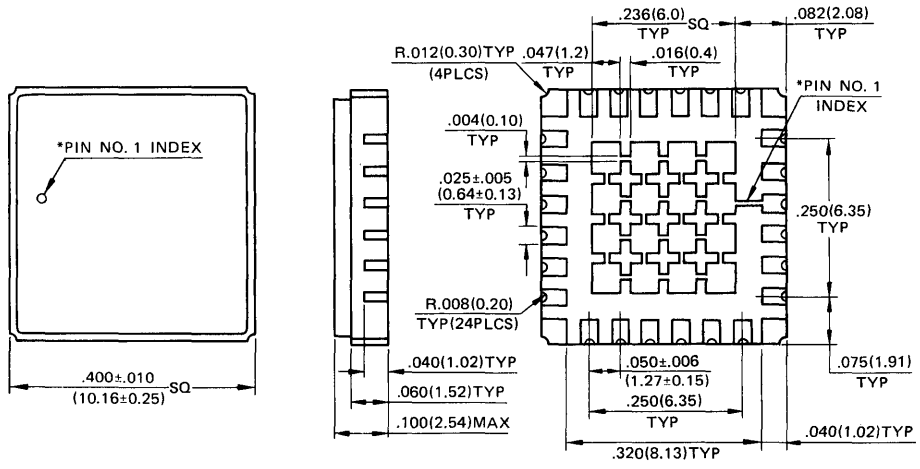


LCC-28C-F02

PAD CONFIGURATION



28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100484A-10

August 1988
Edition 2.0

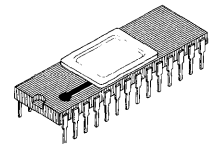
16384-BIT BIPPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100484A is fully decoded 16384-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by 4 bits, and it features on-chip voltage temperature compensation for improved noise margin.

The MBM 100484A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100484A is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 28-pin DIP or Flat package and LCC, and is fully compatible with industry-standard 100K-series ECL families.

- 4096 words x 4 bits organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industry-standard 100 K-series ECL families
- Address access time: 10 ns max.
- Chip select access time: 5 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation: 0.06 mW/bit typ.
- DOPOS and IOP-II processing

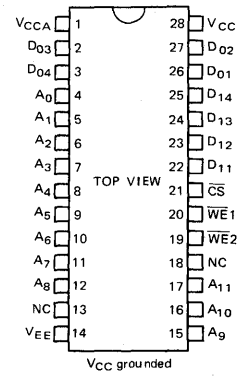


CERAMIC PACKAGE
DIP-28C-A06

CERAMIC PACKAGE
FPT-28C-C03

LCC-28C-F01 : See Page 10
LCC-28C-F02 : See Page 11

PIN ASSIGNMENT



See Page 10
LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

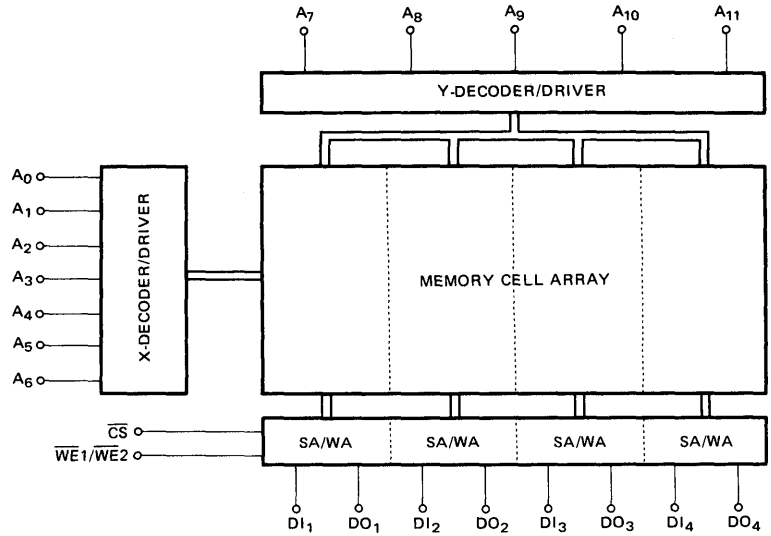
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 100484A BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE1}/\overline{WE2}$	D_{IN}		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	D_{OUT}	READ

*L = Both $\overline{WE1}$ and $\overline{WE2}$ are low.
*H = Either $\overline{WE1}$ or $\overline{WE2}$ is high.

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujits MBM 100484A is fully decoded 16384-bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12 bit address designed A_0 through A_{11}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE1}/\overline{WE2}$) inputs. With both $\overline{WE1}/\overline{WE2}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, either $\overline{WE1}$ or $\overline{WE2}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambinet Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -4.5 V, Output Load = 50 Ω to -2.0 V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_A = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	I_{EE}	-260			mA

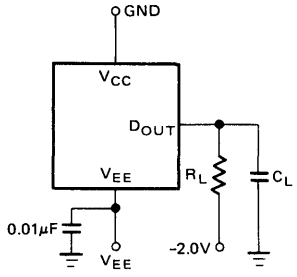
CAPACITANCE

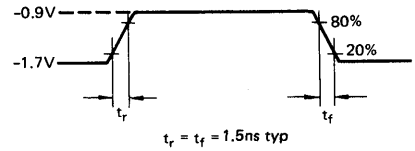
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}			4	pF
Output Pin Capacitance	C_{OUT}			6	pF

AC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = −4.5 V ±5%, Output Load = 50 Ω to −2.0 V and 30 pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Fig. 2 — AC TEST CONDITIONS





$t_r = t_f = 1.5ns$ typ

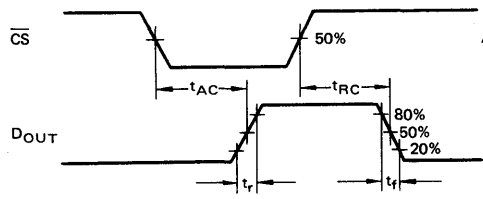
Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including jig and stray capacitance)

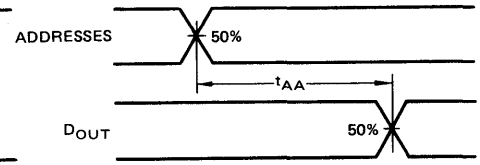
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	2		10	ns
Chip Select Access Time	t_{AC}	1		5	ns
Chip Select Recovery Time	t_{RC}	1		5	ns

READ CYCLE TIMING DIAGRAMS

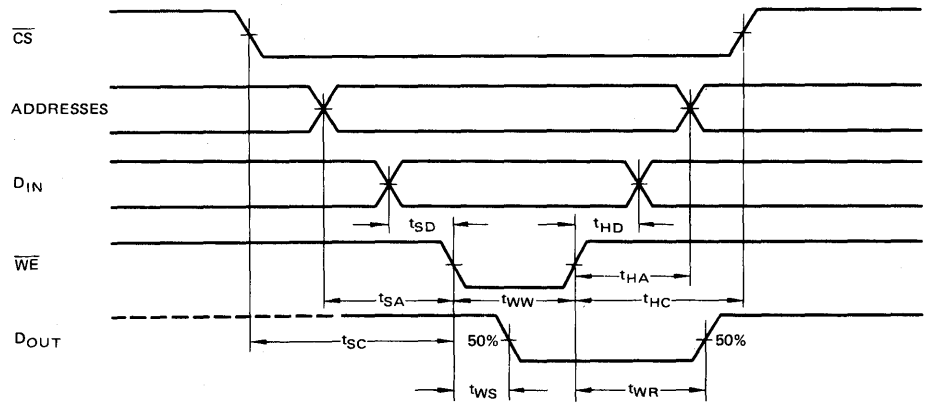




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10			ns
Write Disable Time	t_{WS}			5	ns
Write Recovery Time	t_{WR}			11	ns
Address Set Up Time	t_{SA}	2			ns
Chip Select Set Up Time	t_{SC}	2			ns
Data Set Up Time	t_{SD}	2			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

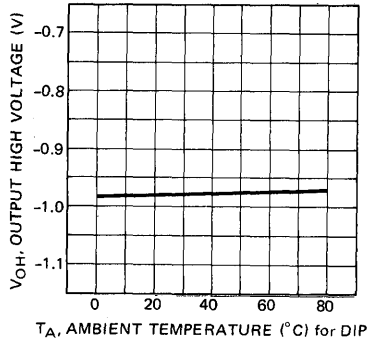


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

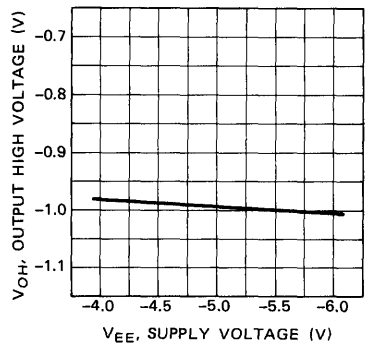


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

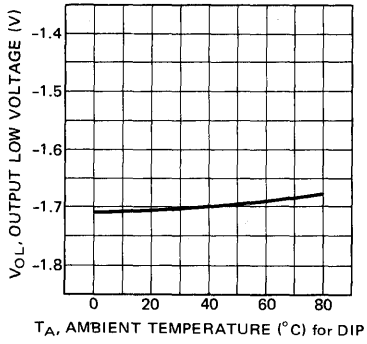


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

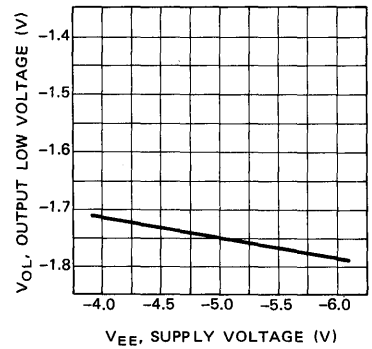


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

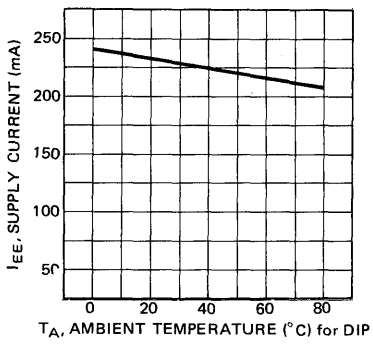


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

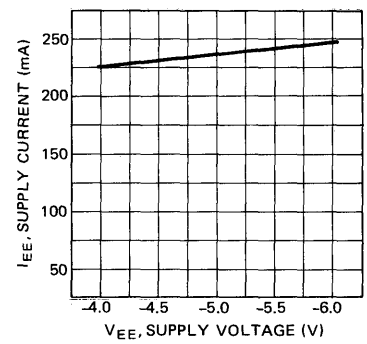


Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

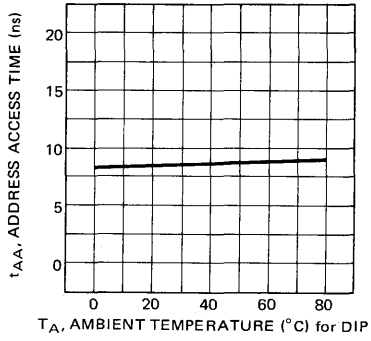


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

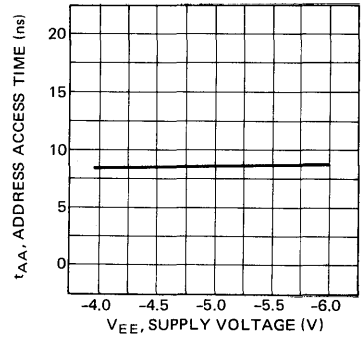


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

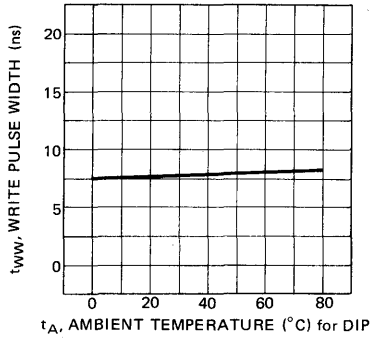
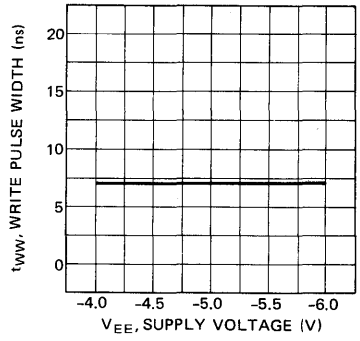


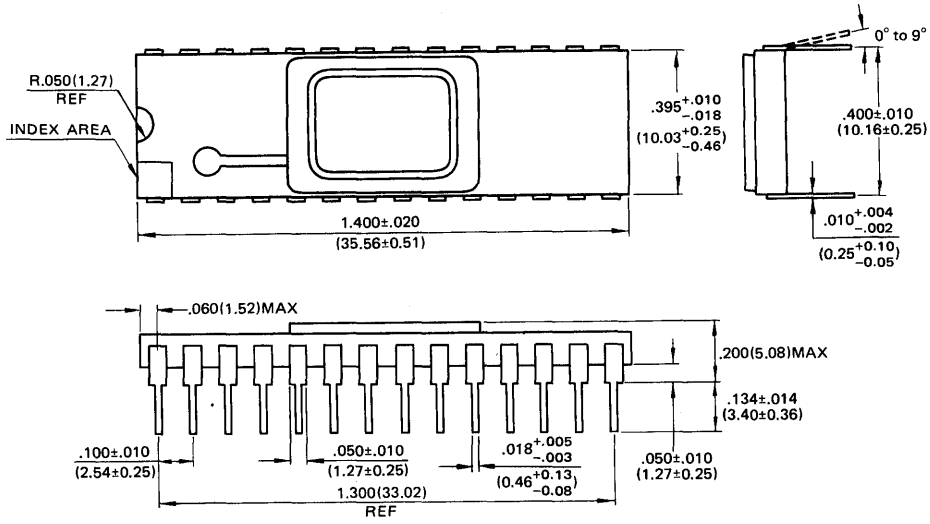
Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



1

PACKAGE DIMENSIONS

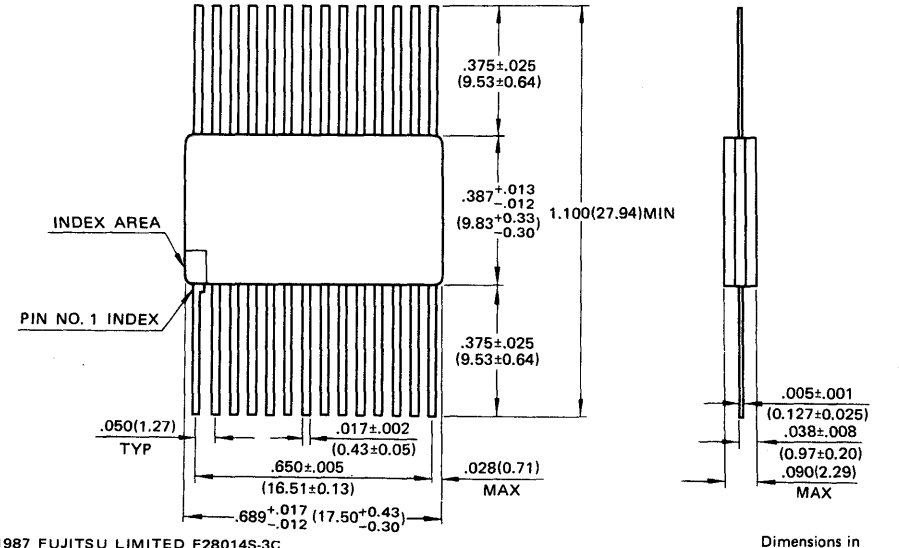
28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

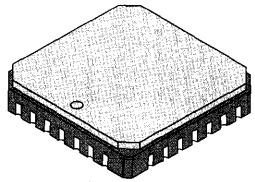
1

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE No.: FPT-28C-C03)



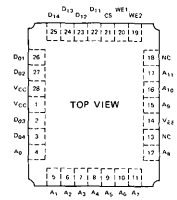
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

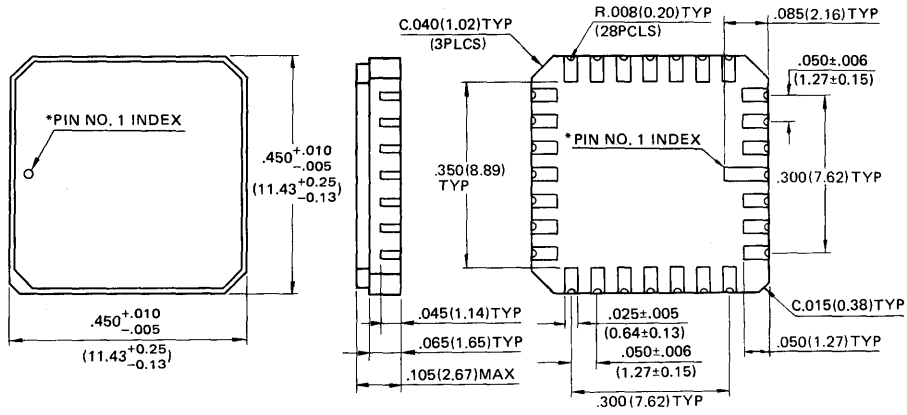


LCC-28C-F01

PAD CONFIGURATION

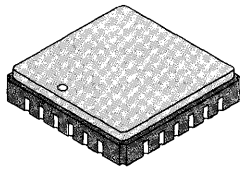


28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-F01)



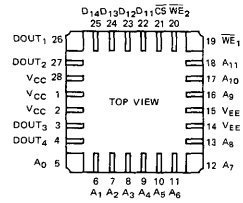
*Shape of PIN NO.1 INDEX: Subject to change without notice.

Dimensions in
inches (millimeters)

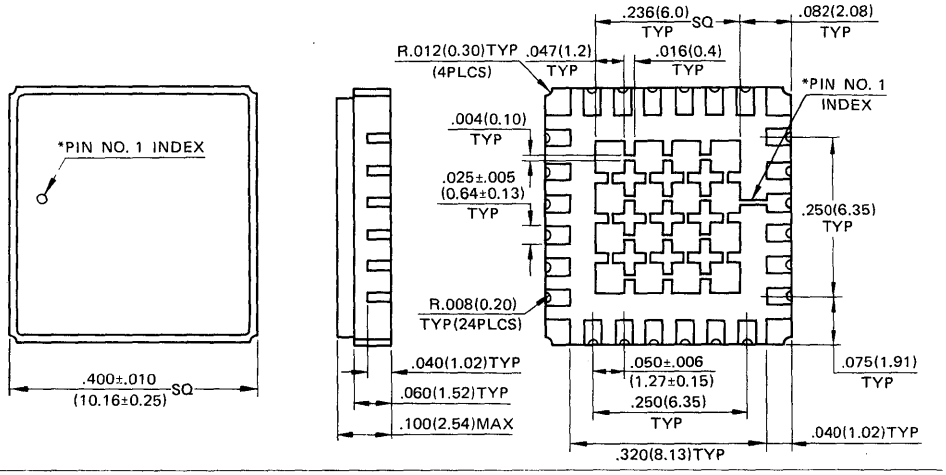


LCC-28C-F02

PAD CONFIGURATION



28-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

FUJITSU

ECL 16384-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100A484-5

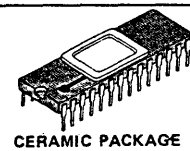
TS318-B886
June, 1988

16384-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100A484 is fully decoded 16384 bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. The device is organized as 4096 words by 4 bits, and it features on chip voltage temperature compensation for improved noise margin.

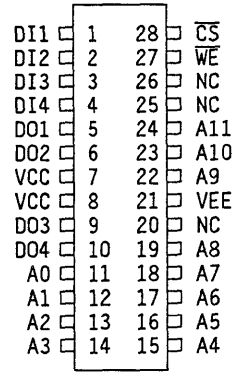
Operation for the MBM100A484 is specified over a temperature range of the Case Temperature (T_C) from 0°C to 85°C. It also features 28-pin Ceramic DIP or Flat Package and is fully compatible with industry standard 100K-series ECL families.

- 4096 words x 4 bit organization
- On-chip voltage temperature compensation for improved noise margin
- Fully compatible with industory standard 100K series ECL families
- Address access time: 5ns max
  Chip select access time: 3ns max
- Power dissipation: -300 mA min
- Open emitter output for ease of memory expansion



CERAMIC PACKAGE
DIP-28C-A06

CERAMIC PACKAGE
FPT-28C-C03



PIN ASSIGNMENTS

ABSOLUTE MAXIMUM RATINGS (See NOTE)

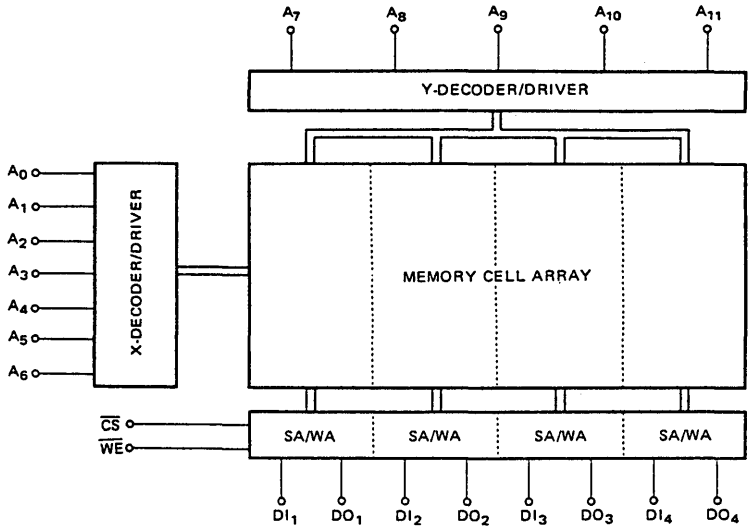
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -6.0	V
Input Voltage	V_{IN}	+0.5 to -2.0	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig.1 - MBM100A484 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100A484 is fully decoded 16384 bit read/write random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designed A0 through A11. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{WE}$ input. With both $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS
(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-4.73	-4.5	-4.27	V	0°C to 85°C

DC CHARACTERISTICS
(VCC=0V, VEE=-4.5V, Output Load=50Ω to -2.0V, TC=0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810		-1650	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (VIN = VIH max)	I_{IH}			220	µA
Input Low Current (VIN = VIL min)	I_{IL}	-50		90	µA
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-300			mA

AC CHARACTERISTICS

(VCC=0V, VEE=-4.5V±5%, Output Load=50Ω to -2.0V, T_C=0°C to 85°C, unless otherwise noted.)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			5	ns
Chip Select Access Time	t_{AC}			3	ns
Chip Select Recovery Time	t_{RC}			3	ns

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	TBD			ns
Write Disable Time	t_{WS}			3	ns
Write Recovery Time	t_{WR}			TBD	ns
Address Set Up Time	t_{SA}	1			ns
Chip Select Set Up Time	t_{SC}	1			ns
Data Set Up Time	t_{SD}	1			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

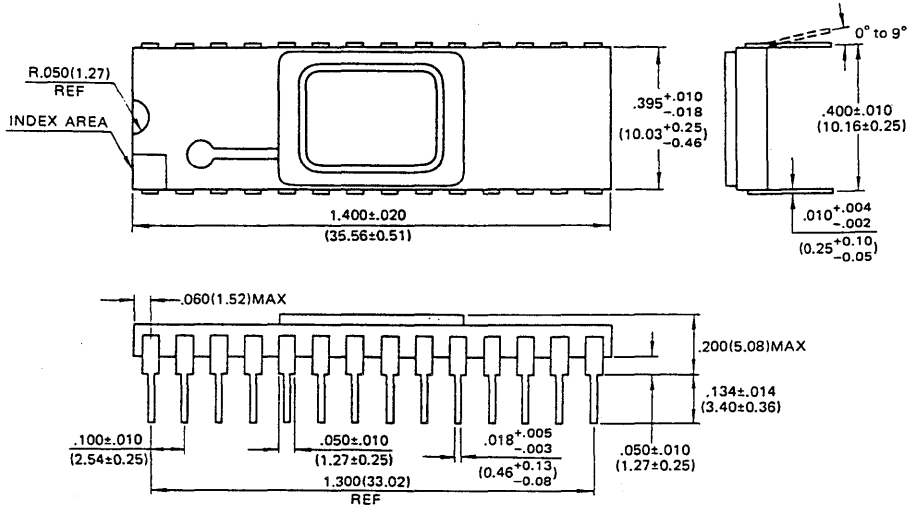
All timing measurement is referenced to 50% input and output levels.

RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

PACKAGE DIMENSIONS

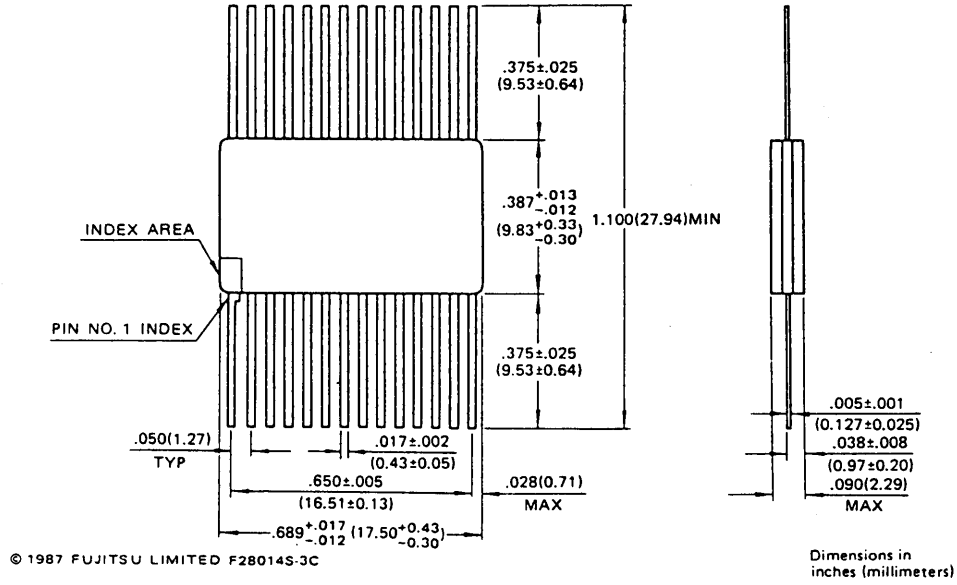
28-LEAD CERAMIC (METAL-SEAL) DUAL IN-LINE PACKAGE
(CASE NO.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE NO.: FPT-28C-C03)



FUJITSU

ECL 65536-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10490-15
MBM10490-25

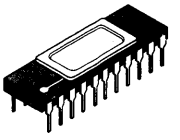
July 1987
Edition 3.0

65536-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

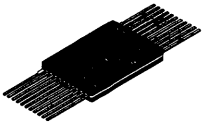
The Fujitsu MBM 10490 is fully decoded 65536-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by one bit, and it features on-chip voltage compensation for improved noise margin.

The MBM 10490 offers extremely small cell and chip size, realized through the use of Fujitsu's patented IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 10490 is specified over a temperature range of from 0°C to 75°C (T_C). It also features 22 pin Ceramic DIP or Flat Package. It is fully compatible with industry-standard 10K-series ECL familes.



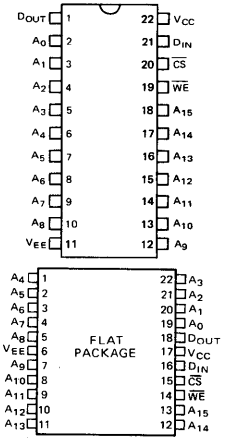
CERAMIC PACKAGE
DIP-22C-A02



CERAMIC PACKAGE
FPT-22C-C01

- 65536 words x 1 bit organization
- On-chip voltage compensation for improved noise margin.
- Fully compatible with industry-standard 10K-series ECL families.
- Address access time: : 15 ns max. (MBM 10490-15)
  25 ns max. (MBM 10490-25)
- Chip select access time : 10 ns max. (MBM 10490-15)
  15 ns max. (MBM 10490-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.017 mW/bit typ. (MBM 10490-15)
  0.012 mW/bit typ. (MBM 10490-25)
- IOP-II

PIN ASSIGNMENT



*V_{CC} grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

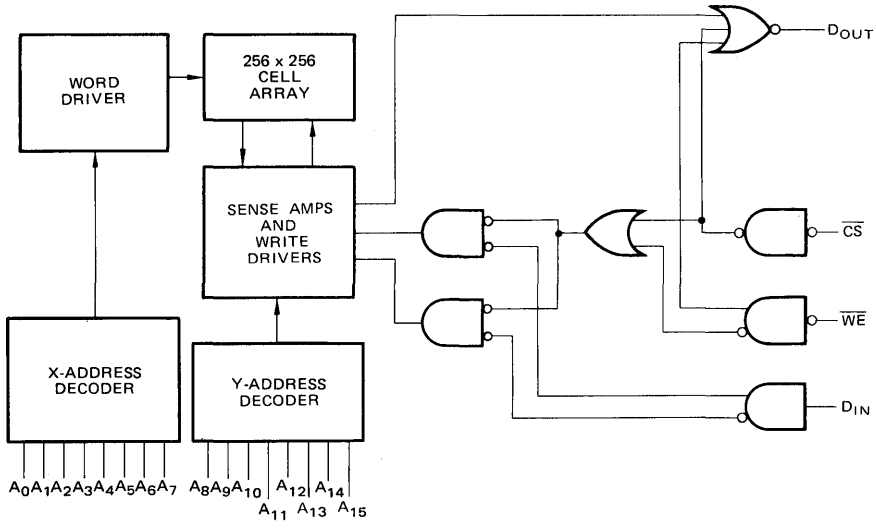
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature under Bias	T_C	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — MBM 10490 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10490 is fully decoded 65536 bit read/write random access memory organized as 65536 words by one bit. Memory cell selection is achieved by means of a 16 bit address designated A_0 through A_{15}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω and 30pF to -2.0V, T_C = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10490-15	I_{EE}	-300			mA	0°C to 75°C
Power Supply Current (All Inputs and Output Open) MBM 10490-25	I_{EE}	-200			mA	0°C to 75°C

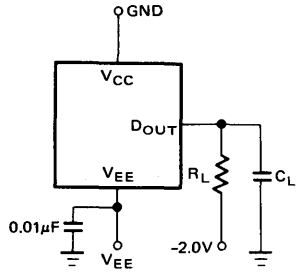
CAPACITANCE

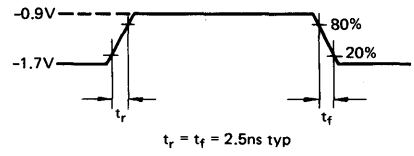
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		4	7	pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_C = 0°C to 85°C, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





$t_r = t_f$ = 2.5ns typ

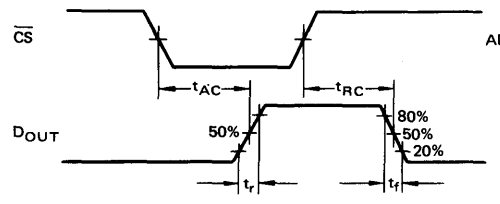
Output Load: R_L = 50Ω
C_L = 30pF
(including scope and jig)

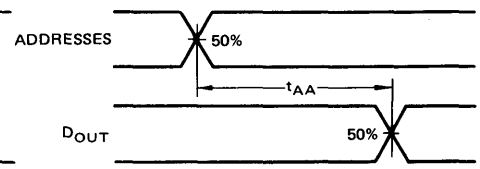
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10490-15			MBM 10490-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			15			25	ns
Chip Select Access Time	t_{AC}			10			15	ns
Chip Select Recovery Time	t_{RC}			10			15	ns

READ CYCLE TIMING DIAGRAMS

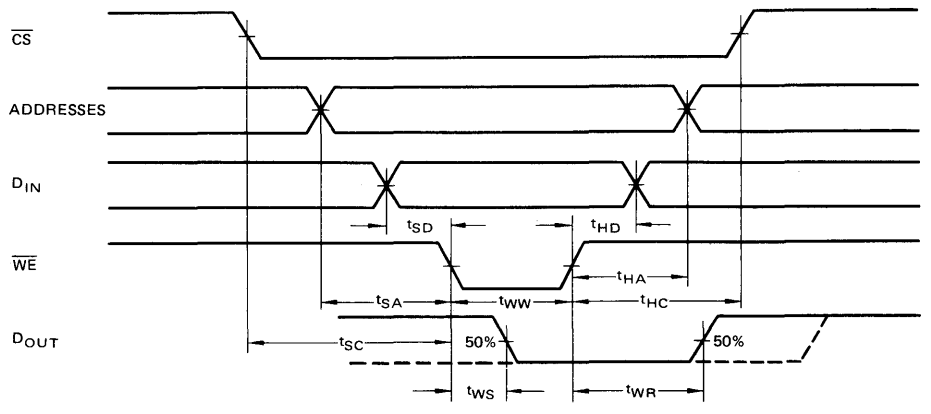




WRITE CYCLE

Parameter	Symbol	MBM 10490-15			MBM 10490-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	15			20			ns
Write Disable Time	t_{WS}			10			15	ns
Write Recovery Time	t_{WR}			15			25	ns
Address Set Up Time	t_{SA}	2			3			ns
Chip Select Set Up Time	t_{SC}	2			3			ns
Data Set Up Time	t_{SD}	2			3			ns
Address Hold Time	t_{HA}	2			2			ns
Chip Select Hold Time	t_{HC}	2			2			ns
Data Hold Time	t_{HD}	2			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2		ns
Output Fall Time	t_f		2		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

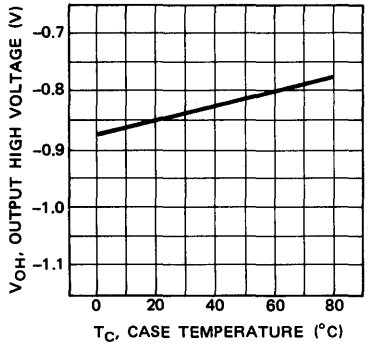


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

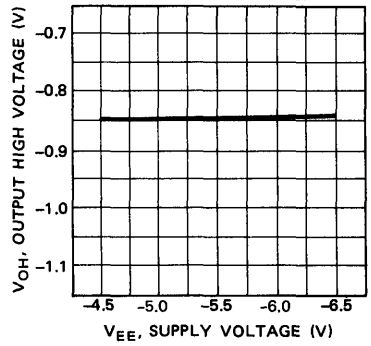


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

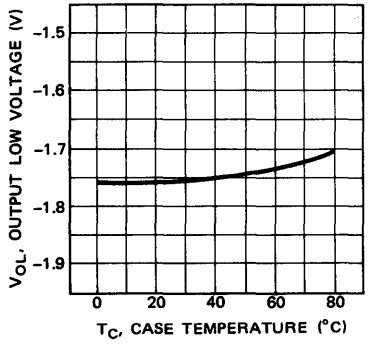


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

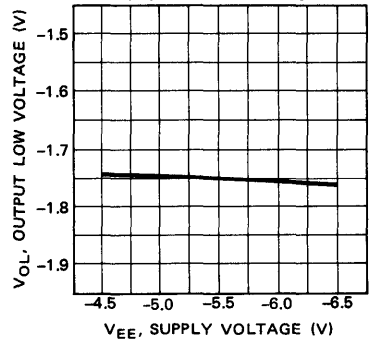


Fig. 7 – SUPPLY CURRENT vs CASE TEMPERATURE

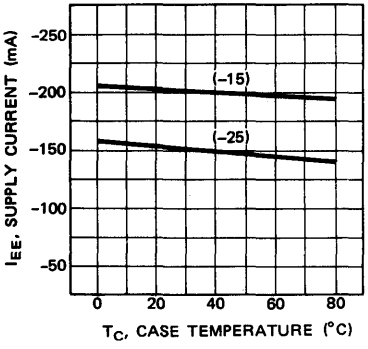


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

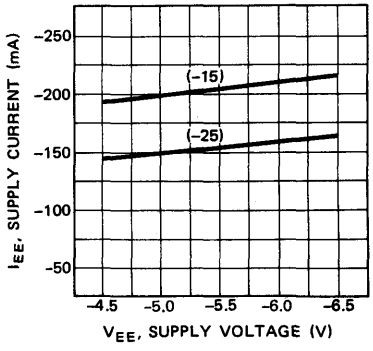


Fig. 9 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

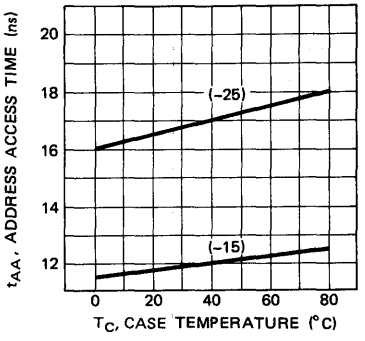


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

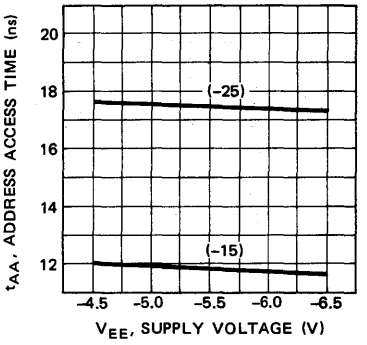


Fig. 11 – WRITE PULSE WIDTH vs CASE TEMPERATURE

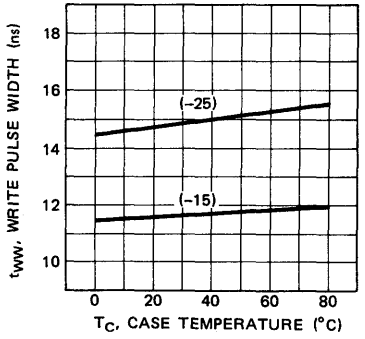
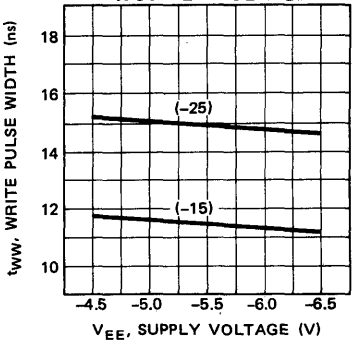


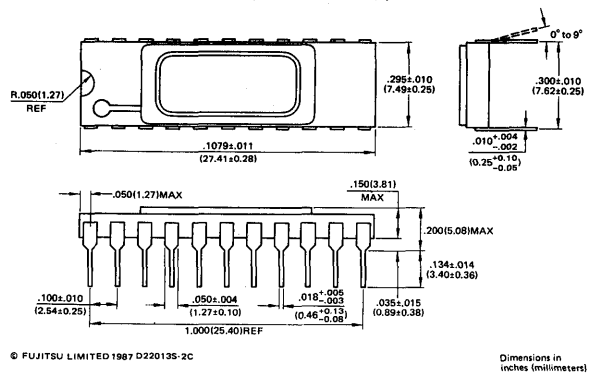
Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



1

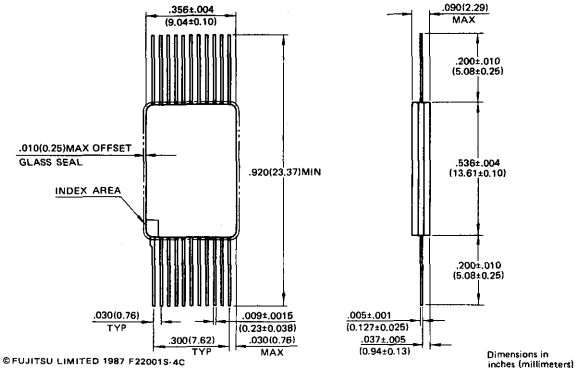
PACKAGE DIMENSIONS

22-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-22C-A02)



Dimensions in
inches (millimeters)

22-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-22C-C01)



Dimensions in
inches (millimeters)

FUJITSU

ECL 65536-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100490-15
MBM100490-25

July 1987
Edtion 1.0

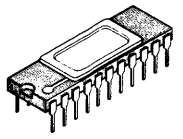
65536-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100490 is fully decoded 65536-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by one bit, and it features on-chip voltage temperature compensation for improved noise margin.

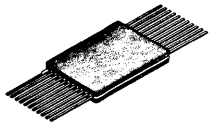
The MBM 100490 offers extremely small cell and chip size, realized through the use of Fujitsu's patened IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM 100490 is specified over a temperature range of from 0°C to 85°C (T_C). It also features 22 pin Ceremic DIP or Flat Package. It is fully compatible with industry-standard 100K-series ECL familes.

- 65536 words x 1 bit organization
- On-chip voltage temperature compensation for improved noise margin.
- Fully compatible with industry-standard 100K-series ECL families.
- Address access time: 15 ns max. (MBM 100490-15)
  25 ns max. (MBM 100490-25)
- Chip select access time: 10 ns max. (MBM 100490-15)
  15 ns max. (MBM 100490-25)
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.017 mW/bit typ. (MBM 100490-15)
  0.012 mW/bit typ. (MBM 100490-25)
- IOP-II

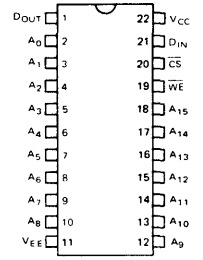


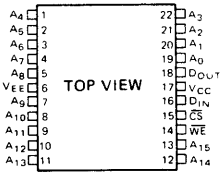
CERAMIC PACKAGE
DIP-22C-A02



CERAMIC PACKAGE
FPT-22C-C01

PIN ASSIGNMENT





*V_{CC} grounded

LCC PAD CONFIGURATION : SeePage 10

ABSOLUTE MAXIMUM RATINGS (See NOTE)

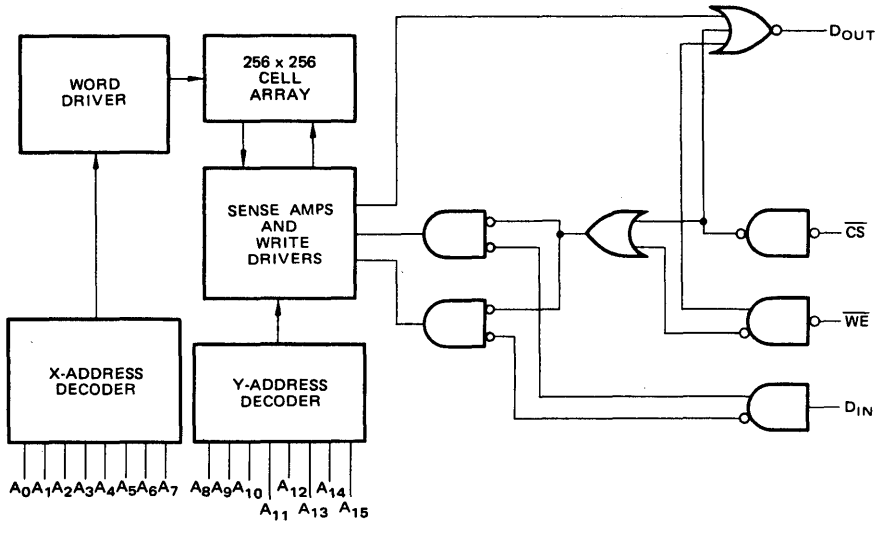
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MBM 100490 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 100490 is fully decoded 65536 bit read/write random access memory organized as 65536 words by one bit. Memory cell selection is achieved by means of a 16 bit address designated A_0 through A_{15}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature
Supply Voltage	V_{EE}	5.7	4.5	4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = –4.5V, Output Load = 50Ω and 30pF to –2.0V, T_C = 0°C to 85°C, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	–1025		–880	mV
Ouput Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	–1810		–1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OHC}	–1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			–1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)		V_{IH}	–1165		–880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)		V_{IL}	–1810		–1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)		I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	–50			μA
CS Input Low Current (V_{IN} = $V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Output Open)	MBM 100490-15	I_{EE}	–300			mA
	MBM 100490-25		–200			

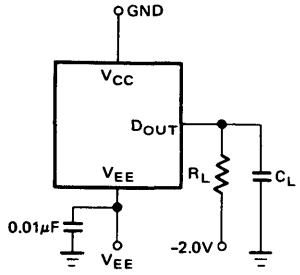
CAPACITANCE

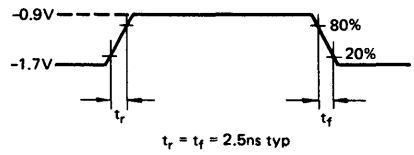
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		4	7	pF

AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, T_C = 0°C to 85°C, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





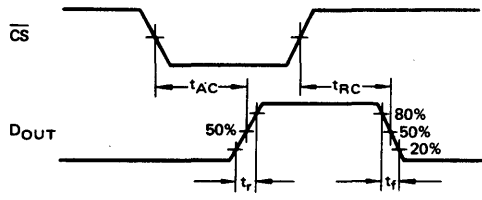
Output Load: R_L = 50Ω
C_L = 30pF
(including scope and jig)

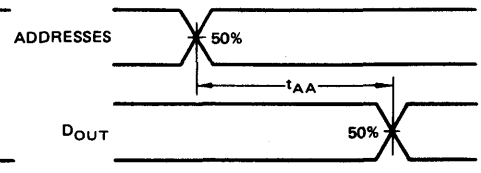
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM 10490-15			MBM 10490-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time	t_{AA}			15			25	ns
Chip Select Access Time	t_{AC}			10			15	ns
Chip Select Recovery Time	t_{RC}			10			15	ns

READ CYCLE TIMING DIAGRAMS

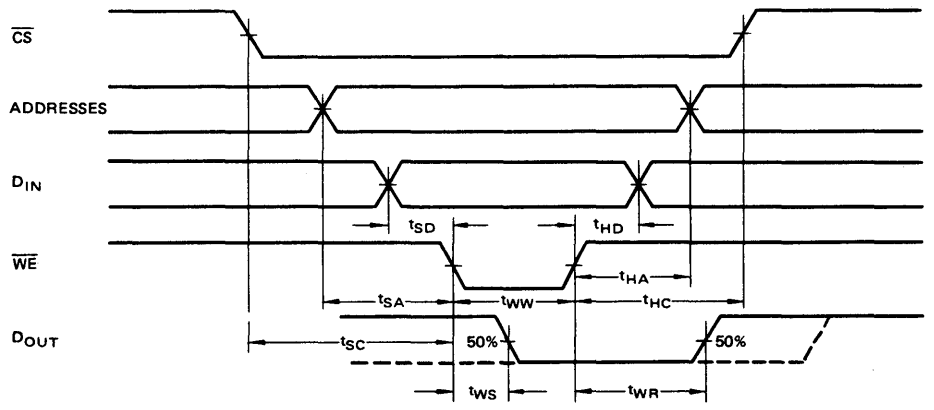




WRITE CYCLE

Parameter	Symbol	MBM 10490-15			MBM 10490-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Pulse Width	t_{WW}	15			20			ns
Write Disable Time	t_{WS}			10			15	ns
Write Recovery Time	t_{WR}			15			25	ns
Address Set Up Time	t_{SA}	2			3			ns
Chip Select Set Up Time	t_{SC}	2			3			ns
Data Set Up Time	t_{SD}	2			3			ns
Address Hold Time	t_{HA}	1			2			ns
Chip Select Hold Time	t_{HC}	1			2			ns
Data Hold Time	t_{HD}	1			2			ns

WRITE CYCLE TIMING DIAGRAM



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2		ns
Output Fall Time	t_f		2		ns

CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

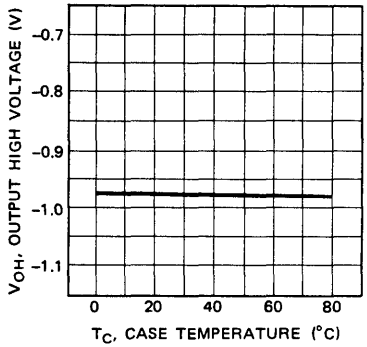


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

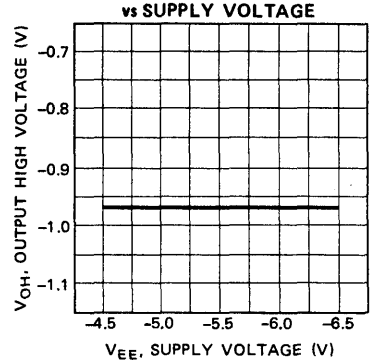


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

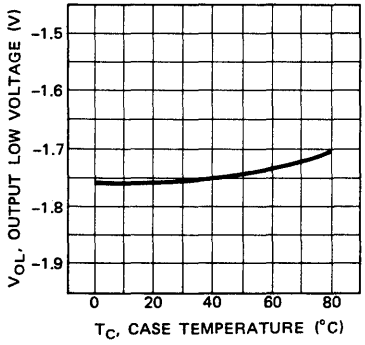


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

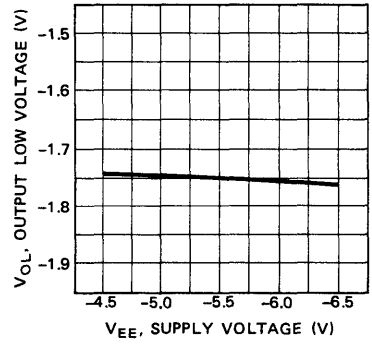


Fig. 7 – SUPPLY CURRENT vs CASE TEMPERATURE

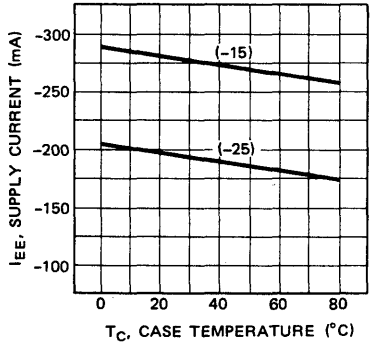


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

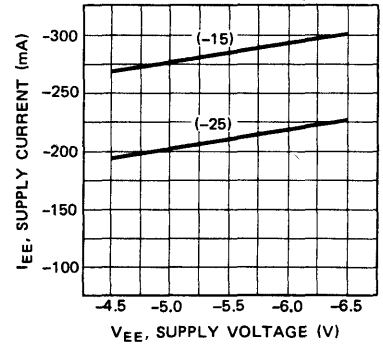


Fig. 9 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

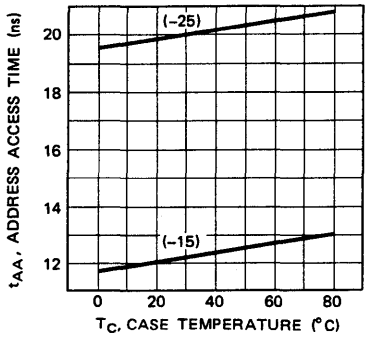


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

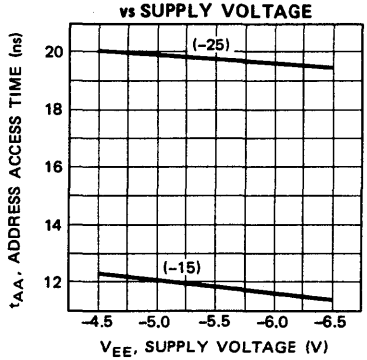


Fig. 11 – WRITE PULSE WIDTH vs CASE TEMPERATURE

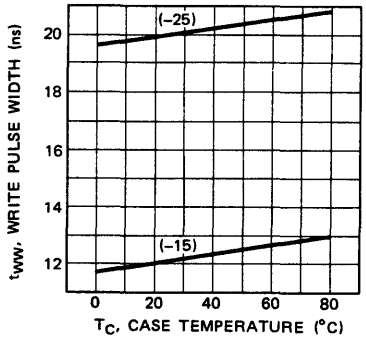
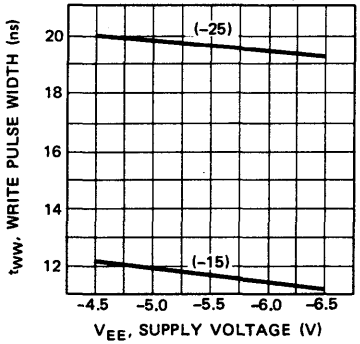


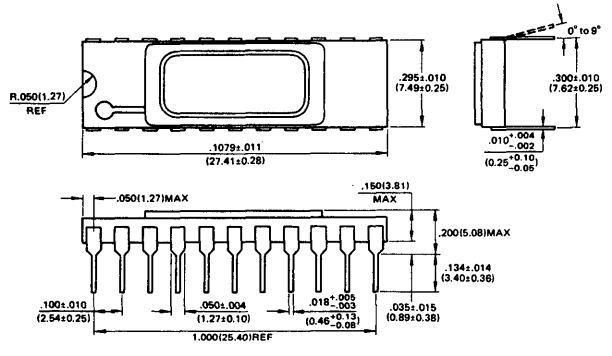
Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



1

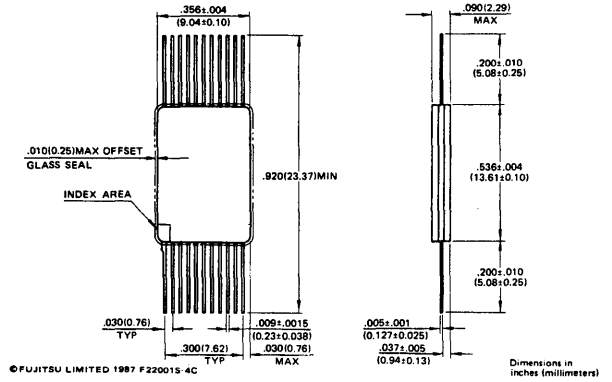
PACKAGE DIMENSIONS

22-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-22C-A02)



Dimensions in inches (millimeters)

22-LEAD CERAMIC AXIAL FLAT PACKAGE
(CASE No.: FPT-22C-C01)



Dimensions in inches (millimeters)

FUJITSU

ECL 65536-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10494-7

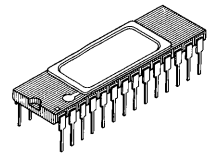
TS314-C886
June, 1988

65536-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10494 is fully decoded 65536 bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. The device is organized as 16384 words by 4 bits, and it features on chip voltage compensation for improved noise margin.

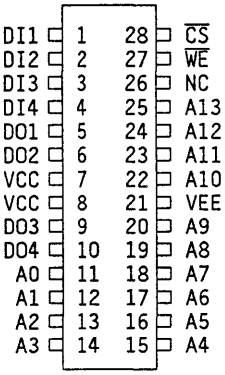
Operation for the MBM10494 is specified over a temparature range of the Case Temperature(T_C) from 0°C to 75°C. It also features 28-pin Ceramic DIP or Flat Package and is fully compatible with industry standard 10K-seriese ECL families.

- 16384 words x 4 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standard 10K series ECL families
- Address access time: 7ns max
  Chip select access time: 5ns max
- Power dissipation: -330 mA min
- Open emitter output for ease of memory expansion



CERAMIC PACKAGE
DIP-28C-A10

CERAMIC PACKAGE
FPT-28C-C03



PIN ASSIGNMENTS

ABSOLUTE MAXIMUM RATINGS (See NOTE)

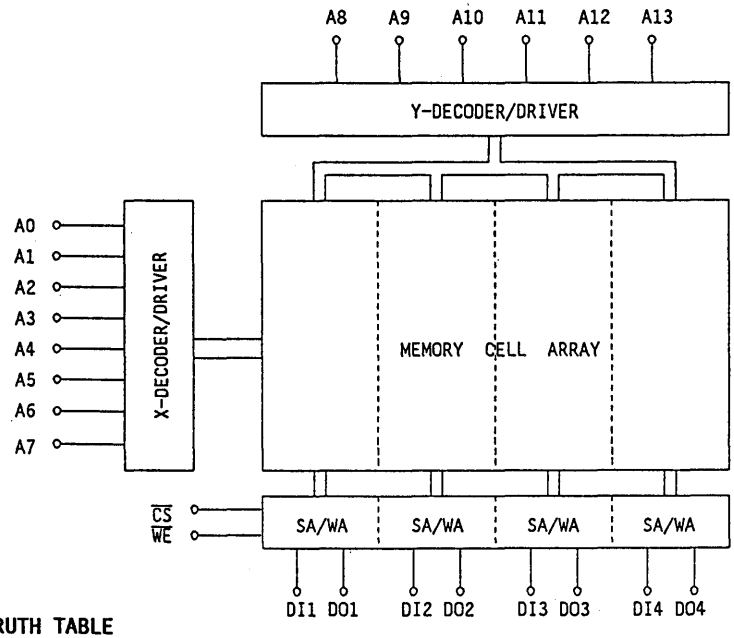
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -6.0	V
Input Voltage	V_{IN}	+0.5 to -2.0	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig.1 - MBM10494 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

L = Low voltage level
H = High voltage level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10494 is fully decoded 65536 bit read/write random access memory organized as 16384 words by 4 bits. Memory cell selection is achieved by means of a 14-bit address designed A0 through A13. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{WE}$ input. With both $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS
(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (TC)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS
(VCC=0V, VEE=-5.2V, Output Load=50Ω to -2.0V, TC=0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°Cto75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°Cto75°C
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA	0°Cto75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-330			mA	0°Cto75°C

AC CHARACTERISTICS

(VCC=0V, VEE=-4.5V±5%, Output Load=50Ω to -2.0V, T_C=0°C to 85°C, unless ptherwise noted.)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			7	ns
Chip Select Access Time	t_{AC}			5	ns
Chip Select Recovery Time	t_{RC}			5	ns

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	7			ns
Write Disable Time	t_{WS}			5	ns
Write Recovery Time	t_{WR}			8	ns
Address Set Up Time	t_{SA}	TBD			ns
Chip Select Set Up Time	t_{SC}	1			ns
Data Set Up Time	t_{SD}	1			ns
Address Hold Time	t_{HA}	1			ns
Chip Select Hold Time	t_{HC}	1			ns
Data Hold Time	t_{HD}	1			ns

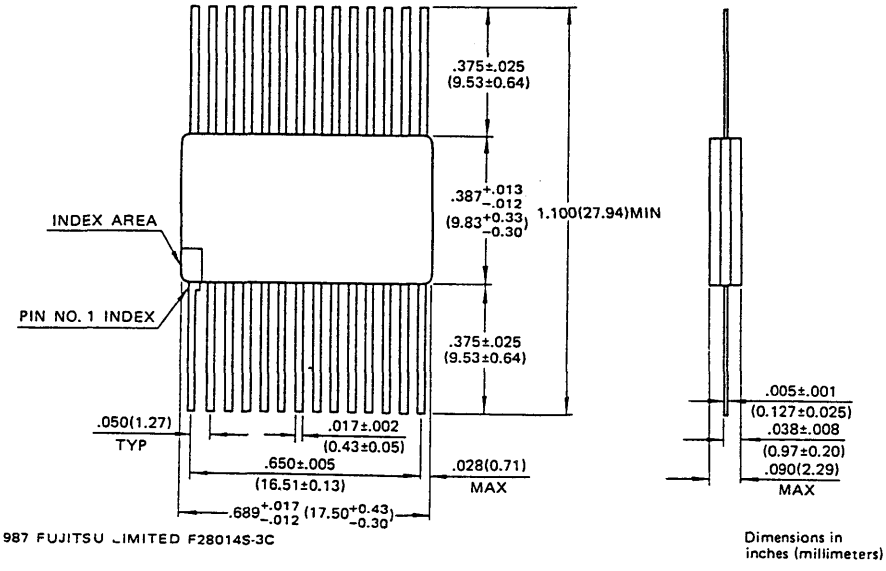
All timing measurement is referenced to 50% input and output levels.

RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE NO.: FPT-28C-C03)



Dimensions in
inches (millimeters)

1

FUJITSU

TTL 576-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM 93419

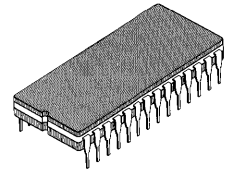
June 1983

1

64x9 BIT BIPOLAR TTL RANDOM ACCESS MEMORY

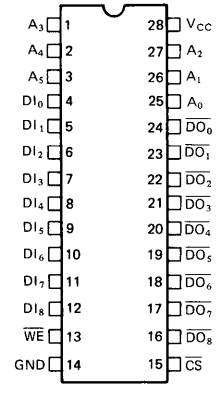
The Fujitsu MBM 93419 is a high speed TTL Read/Write Random Access Memory, organized as 64 words by 9 bits, and open collector outputs.
It is housed in 28-pin dual-in-line package, and plug-in replaceable with F93419.
It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and the number of required bits per word is relatively large. The ninth bit can provide parity for 8-bit words system.

- 64 Words x 9 Bits Organization
- +5V Single Power Supply
- TTL Inputs and Outputs
- Open Collector Outputs
- Address Access Time: 45ns Max.
- Chip Select Access Time: 40ns Max.
- Power Dissipation: 1.3mW/bit Typ.
- Compatible with F93419



CERAMIC PACKAGE
DIP-28C-C02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

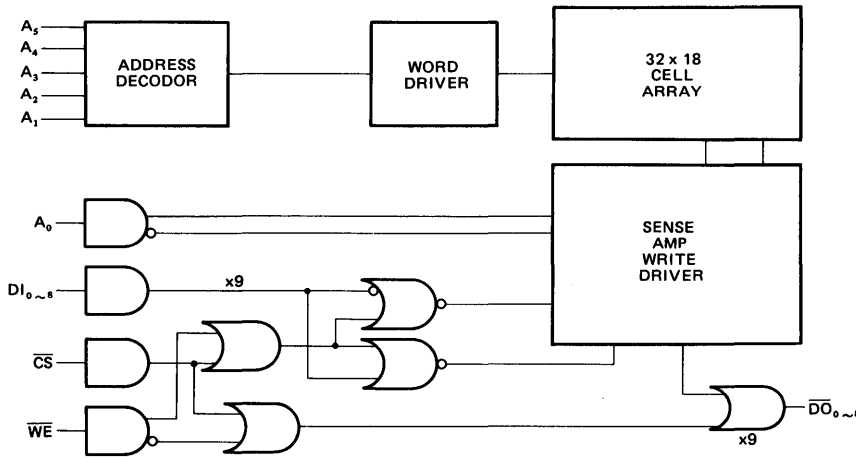
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage (DC)	V_{IN}	-0.5 to +5.5	V
Input Current (DC)	I_{IN}	-12.0 to +5.0	mA
Output Voltage (Output High)	V_{OUT}	-0.5 to +5.5	V
Output Current (DC, Output Low)	I_{OUT}	+20.0	mA
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — MBM 93419 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	DI		
H	X	X	H	DISABLED
L	L	H	H	WRITE "H"
L	L	L	H	WRITE "L"
L	H	X	$\overline{D_{OUT}}$ *	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE
*DATA OUTPUT IS THE COMPLEMENT OF DATA INPUT.

CAPACITANCE (T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 2.0V, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Pin Capacitance	C_{IN}	–	–	5.0	pF
Output Pin Capacitance	C_{OUT}	–	–	8.0	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C to +75°C
Input High Voltage	V_{IH}	2.1	–	–	V	
Input Low Voltage	V_{IL}	–	–	0.8	V	

1

DC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 75°C, Air Flow ≧ 2.5m/sec, After Warm-up ≧ 2min.)

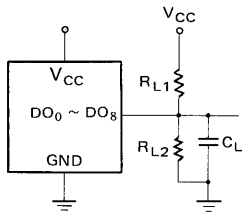
Parameter	Symbol	Min	Typ	Max	Unit
Output Low Voltage (V_{CC} = Min, I_{OL} = 12mA)	V_{OL}		0.4	0.5	V
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}		1.6		V
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}		1.5		V
Input Low Current (V_{CC} = Max, V_{IN} = 0.4V)	I_{IL}		-250	-400	μA
Input High Current (V_{CC} = Max, V_{IN} = 4.5V)	I_{IH1}		1.0	40	μA
Input High Current (V_{CC} = Max, V_{IN} = 5.25V)	I_{IH2}			1.0	mA
Output Leakage Current (V_{CC} = Max, V_{OUT} = 4.5V)	I_{CEX}		1.0	100	μA
Input Clamp Diode Voltage (V_{CC} = Max, I_{IN} = −10 mA)	V_{CD}		-1.0	-1.5	V
Power Supply Current (V_{CC} = Max, T_A = 25°C, All Input GND)	I_{CC}		160	200	mA

1

AC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 75°C, Air Flow ≧ 2.5m/sec, After Warm-up ≧ 2min.)

Fig. 2 — AC TEST CONDITIONS

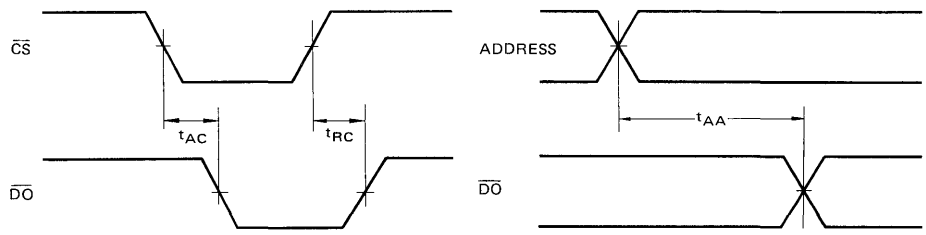


Input Pulse Voltage : $3.5V_{P-P}$
Input Pulse Rise and Fall Time : 10ns
Output Load : R_{L1} = 450Ω
: R_{L2} = 750Ω
: C_L = 30pF (Including Jig)
Timing Measurement Levels : Input = 1.5V
Output = 1.5V

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}		26	45	ns
Chip Select Access Time	t_{AC}		18	40	ns
Chip Select Recovery Time	t_{RC}		18	40	ns

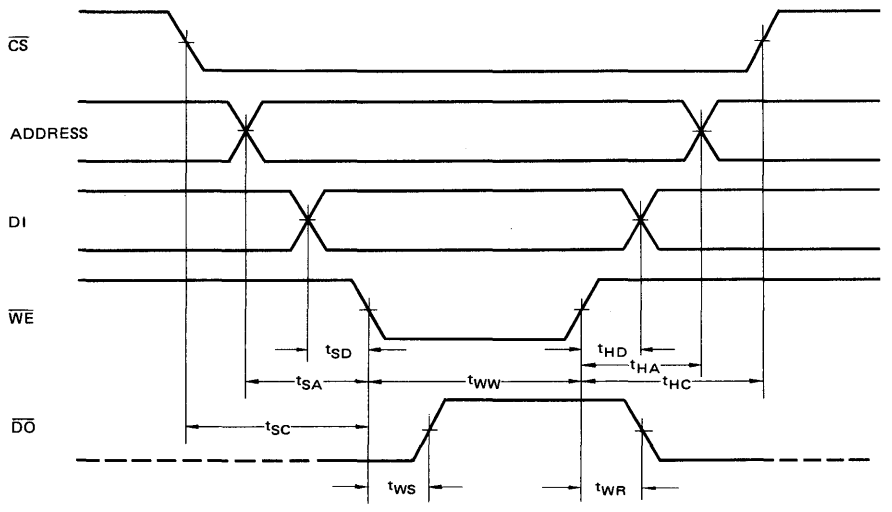
READ CYCLE TIMING DIAGRAMS



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	35	7		ns
Write Recovery Time	t_{WR}		20	45	ns
Write Delayed Time	t_{WS}		20	40	ns
Address Set Up Time	t_{SA}	5	0		ns
Chip Select Set Up Time	t_{SC}	5	0		ns
Data Set Up Time	t_{SD}	5	0		ns
Address Hold Time	t_{HA}	5	0		ns
Chip Select Hold Time	t_{HC}	5	0		ns
Data Hold Time	t_{HD}	5	0		ns

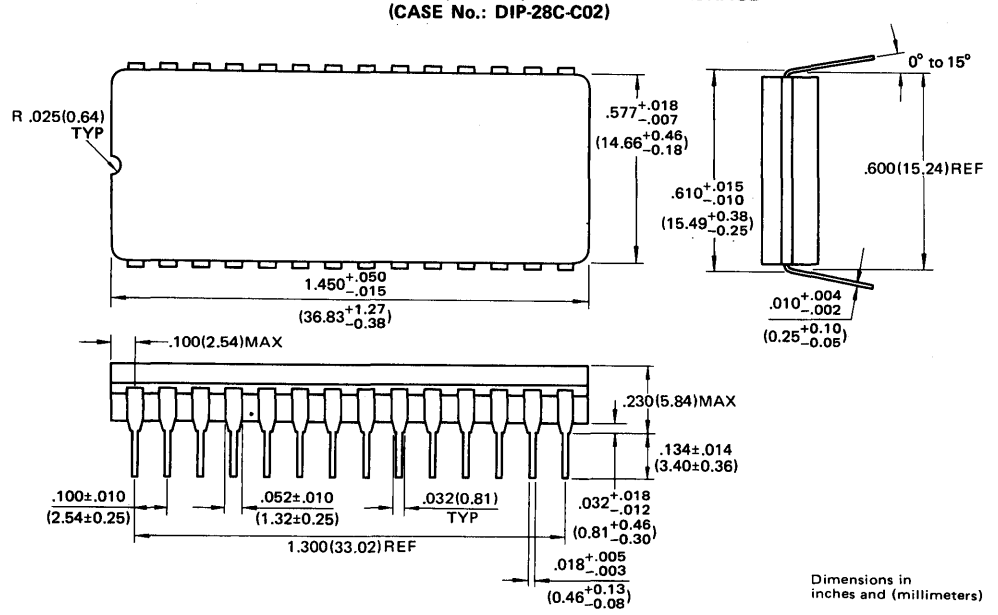
WRITE CYCLE TIMING DIAGRAM



1

PACKAGE DIMENSIONS

28-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C02)



Section 2

BiCMOS RAMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options
2-3	MBM10C490-15	15	65536 bits (65536w x 1b)	22-pin Ceramic DIP 22-pin Ceramic FPT
2-13	MBM100C490-15	15	65536 bits (65536w x 1b)	22-pin Ceramic DIP 22-pin Ceramic FPT 22-pad Ceramic LCC 24-pad Plastic LCC
2-21	MBM10C494-15	15	65536 bits (16384w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT 28-pad Ceramic LCC 28-pin Plastic FPT
2-29	MBM100C494-15	15	65536 bits (16384w x 4b)	28-pin Ceramic DIP 28-pin Ceramic FPT 28-pad Ceramic LCC
2-31	MBM10C500-15	15	262144 bits (262144w x 1b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
2-39	MBM101C500-15	15	262144 bits (262144w x 1b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
2-47	MBM100C500-15	15	262144 bits (262144w x 1b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
2-55	MBM100C504-15	15	262144 bits (65536w x 4b)	32-pin Ceramic DIP 28-pin Ceramic FPT

2

FUJITSU

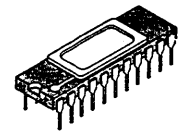
BICMOS 65536-BIT ECL RANDOM ACCESS MEMORY

MBM10C490-15

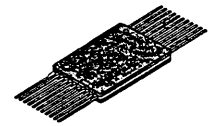
TS317-C886
June 1988 PRELIMINARY

65536-BIT BICMOS ECL RANDOM ACCESS MEMORY

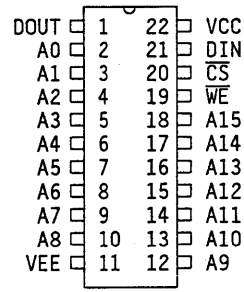
The Fujitsu MBM10C490 is fully decoded 65536 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by one bit, and it features on chip voltage compensation for improved noise margin.
Operation for the MBM10C490 is specified over an ambient temperature range of from 0°C to 75°C (TA). It is packaged in 22-pin ceramic DIP, flatpackage, or LCC and fully compatible with industory standard 10K series ECL families.



CERAMIC PACKAGE
DIP-22C-A02



CERAMIC PACKAGE
FPT-22C-C01



PIN ASSIGNMENTS
LCC-22C-A01 : See page 8
LCC-24P-M01 : See page 9

- 65536 words by 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standard 10K series ECL families
- Address access time: 15 ns max
  Chip select access time: 15 ns max
- Power dissipation: 450 mW typ
- Open emitter output for ease of memory expansion
- BICMOS Processing
- 22-pin ceramic DIP (Suffix: C)
  22-pin ceramic FPT (Suffix: ZF)
  22-pin ceramic LCC (Suffix: CV)
  24-pin plastic SOJ (Suffix: PJ)

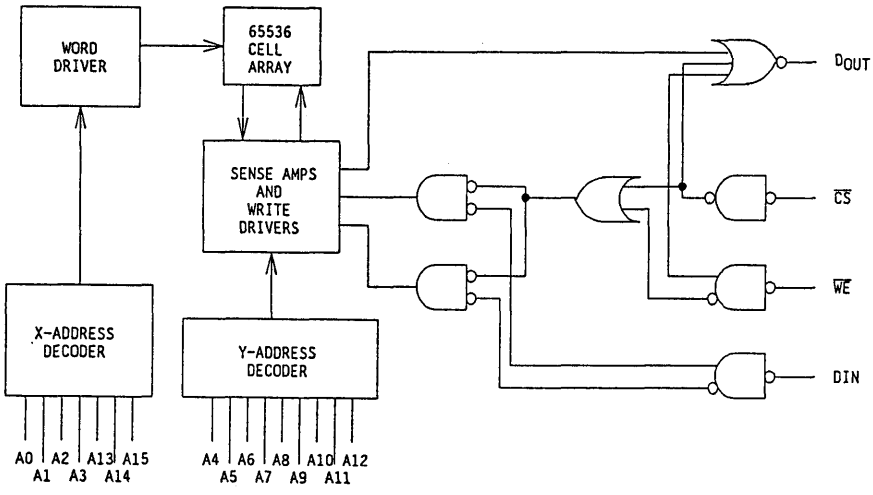
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig.1 - MBM10C490 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10C490 is fully decoded 65536 bit read/write random access memory organized as 65536 words by 1 bit. Memory cell selection is achieved by means of a 16-bit address designed A0 through A15. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient temperature(TA)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC=0V, VEE=-5.2V, Output Load = 50Ω to -2.0V, TA = 0°C to 75°C, Airflow ≥ 2.5 m/s unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TA
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°Cto75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA	0°Cto75°C
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA	0°Cto75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-140			mA	0°Cto75°C

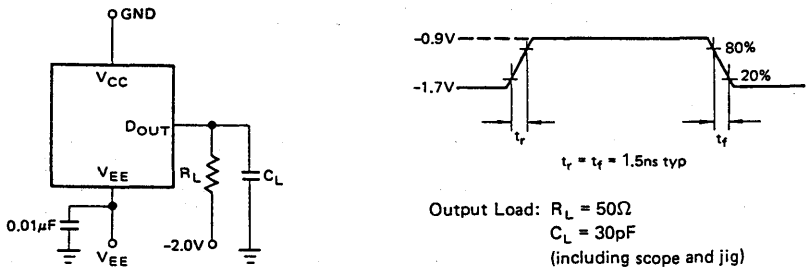
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		TBD		pF
Output Pin Capacitance	C_{OUT}		TBD		pF

AC CHARACTERISTICS

(VCC=0V, VEE=-5.2V±5%, Output Load=50Ω to -2.0V and 30pF to GND, TA = 0°C to 75°C, Airflow ≥ 2.5 m/s unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



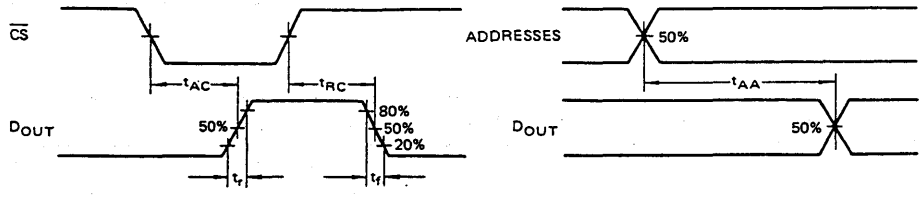
Output Load: R_L = 50Ω
C_L = 30pF
(including scope and jig)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15.0	ns
Chip Select Access Time	t_{AC}			15.0	ns
Chip Select Recovery Time	t_{RC}			15.0	ns

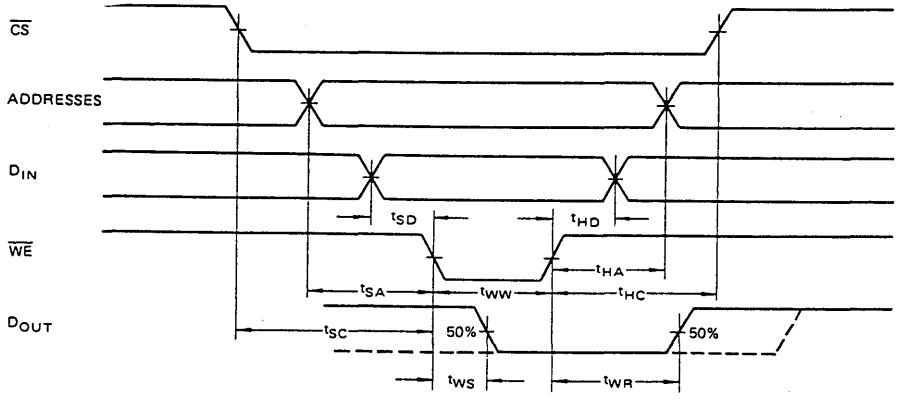
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}			10.0	ns
Write Recovery Time	t_{WR}			18.0	ns
Address Set Up Time	t_{SA}	2.0			ns
Chip Select Set Up Time	t_{SC}	2.0			ns
Data Set Up Time	t_{SD}	2.0			ns
Address Hold Time	t_{HA}	3.0			ns
Chip Select Hold Time	t_{HC}	3.0			ns
Data Hold Time	t_{HD}	3.0			ns

WRITE CYCLE TIMING DIAGRAM

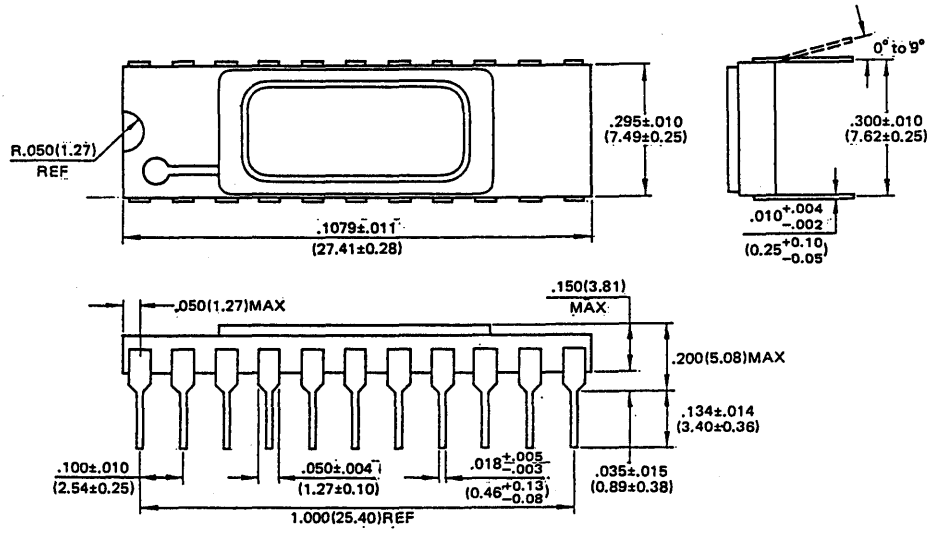


RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

PACKAGE DIMENSIONS

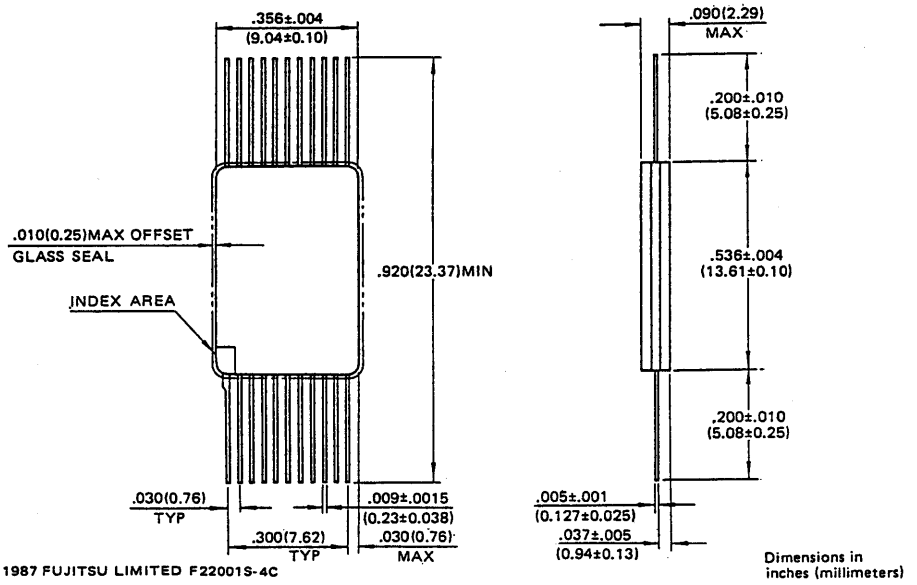
22-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE NO.: DIP-22C-A02)



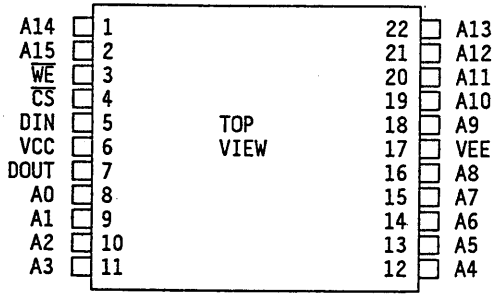
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

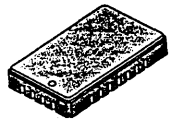
22-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE NO.: FPT-22C-C01)



FLAT PACKAGE PIN ASSIGNMENTS

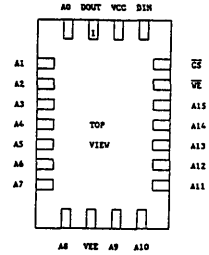


PACKAGE DIMENSIONS



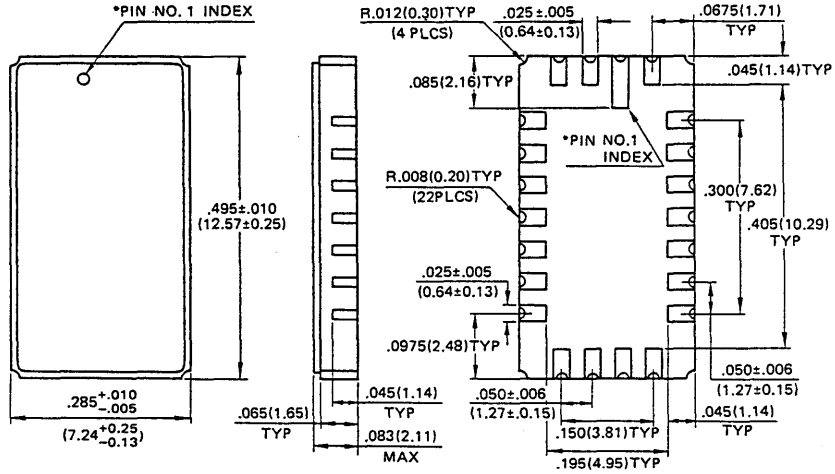
LCC-22C-A01

PAD CONFIGURLATION



2

22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIERS (CASE NO.: LCC-22C-A01)

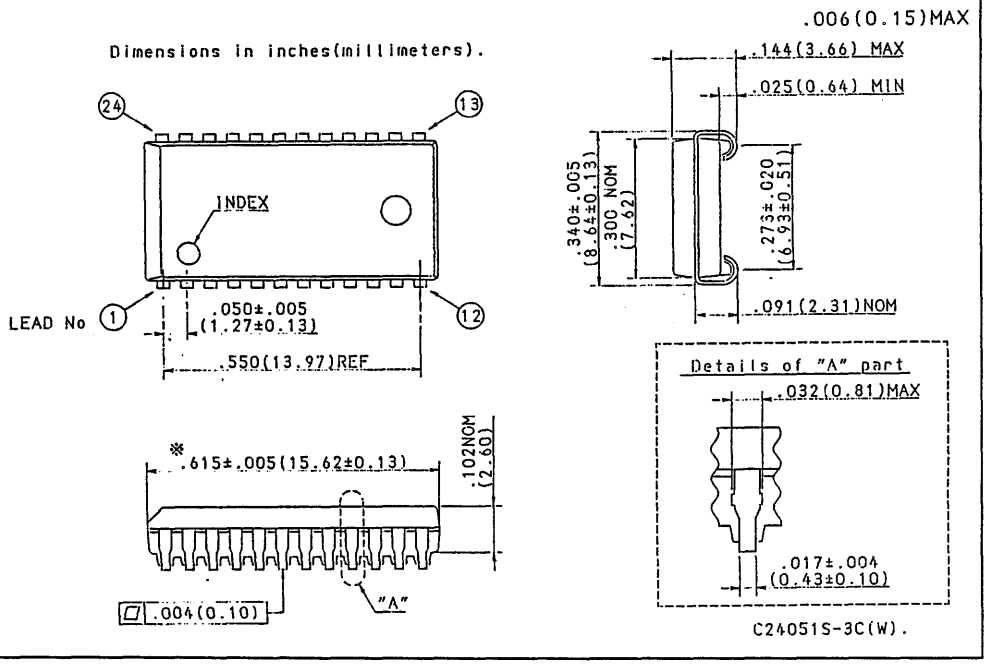


*Share of PIN NO. 1 INDEX: Subject to changed without notice.

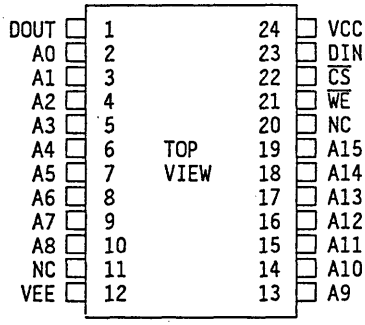
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

24-LEAD PLASTIC LEADED CHIP CARRIER
(CASE NO.: LCC-24P-M01)



SOJ PACKAGE PIN ASSIGNMENTS



FUJITSU

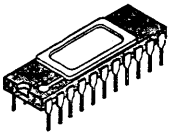
BICMOS 65536-BIT ECL RANDOM ACCESS MEMORY

MBM100C490-15

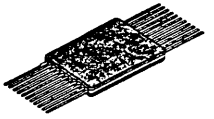
TS318-C886
June 1988 PRELIMINARY

65536-BIT BICMOS ECL RANDOM ACCESS MEMORY

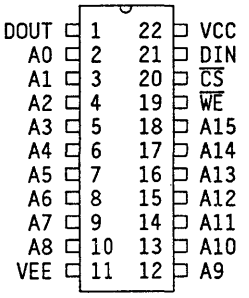
The Fujitsu MBM100C490 is fully decoded 65536 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by one bit, and it features on chip voltage compensation for improved noise margin.
Operation for the MBM100C490 is specified over as ambient temperature range of from 0°C to 85°C (TA). It is packaged in 22-pin ceramic DIP, flatpackage, or LCC and fully compatible with industory standard 100K series ECL families.



CERAMIC PACKAGE
DIP-22C-A02



CERAMIC PACKAGE
FPT-22C-C01



PIN ASSIGNMENT

LCC-22C-A01 : See page 8
LCC-24P-M01 : See page 9

- 65536 words by 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standard 100K series ECL families
- Address access time: 15 ns max
  Chip select access time: 15 ns max
- Power dissipation: 350 mW typ
- Open emitter output for ease of memory expansion
- BICMOS Processing
- 22-pin ceramic DIP (Suffix: C)
  22-pin ceramic FPT (Suffix: ZF)
  22-pin ceramic LCC (Suffix: CV)
  24-pin plastic SOJ (Suffix: PJ)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

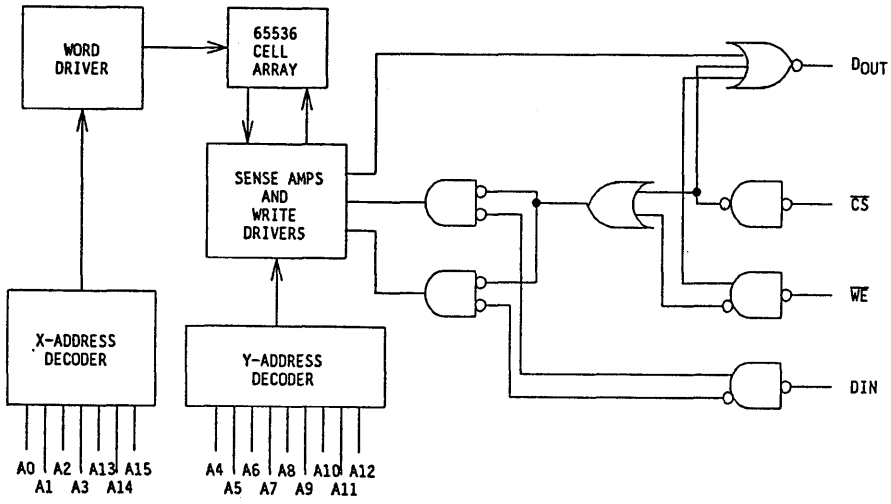
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig.1 - MBM100C490 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100C490 is fully decoded 65536 bit read/write random access memory organized as 65536 words by 1 bit. Memory cell selection is achieved by means of a 16-bit address designed A0 through A15. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS
(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient temperature(TA)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS
(VCC=0V, VEE=-4.5V, Output Load = 50Ω to -2.0V, TA = 0°C to 85°C , Airflow ≥ 2.5 m/s unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810		-1650	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (VIN = VIH max)	I_{IH}			220	µA
Input Low Current (VIN = VIL min)	I_{IL}	-50			µA
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-120			mA

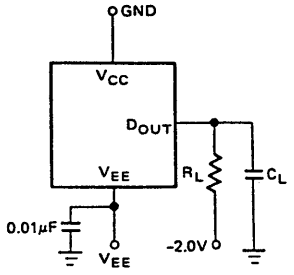
CAPACITANCE

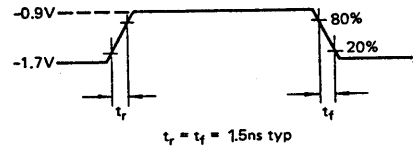
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		TBD		pF
Output Pin Capacitance	C_{OUT}		TBD		pF

AC CHARACTERISTICS

(VCC=0V, VEE=-4.5V±5%, Output Load=50Ω to -2.0V and 30pF to GND, TA = 0°C to 85°C, Airflow ≥ 2.5 m/s, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS





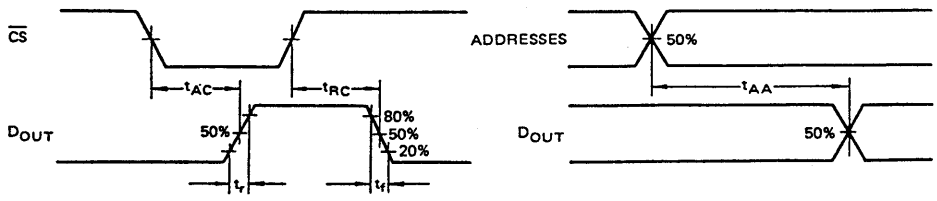
Output Load: R_L = 50Ω
C_L = 30pF
(including scope and jig)

NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15.0	ns
Chip Select Access Time	t_{AC}			15.0	ns
Chip Select Recovery Time	t_{RC}			15.0	ns

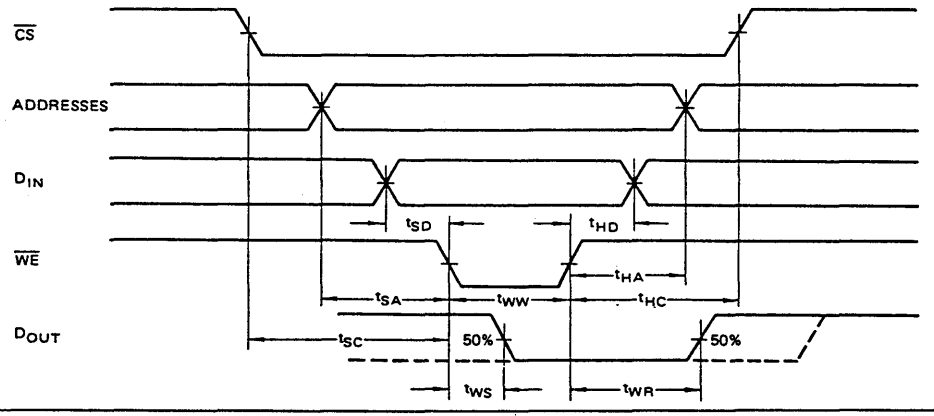
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}			10.0	ns
Write Recovery Time	t_{WR}			18.0	ns
Address Set Up Time	t_{SA}	2.0			ns
Chip Select Set Up Time	t_{SC}	2.0			ns
Data Set Up Time	t_{SD}	2.0			ns
Address Hold Time	t_{HA}	3.0			ns
Chip Select Hold Time	t_{HC}	3.0			ns
Data Hold Time	t_{HD}	3.0			ns

WRITE CYCLE TIMING DIAGRAM

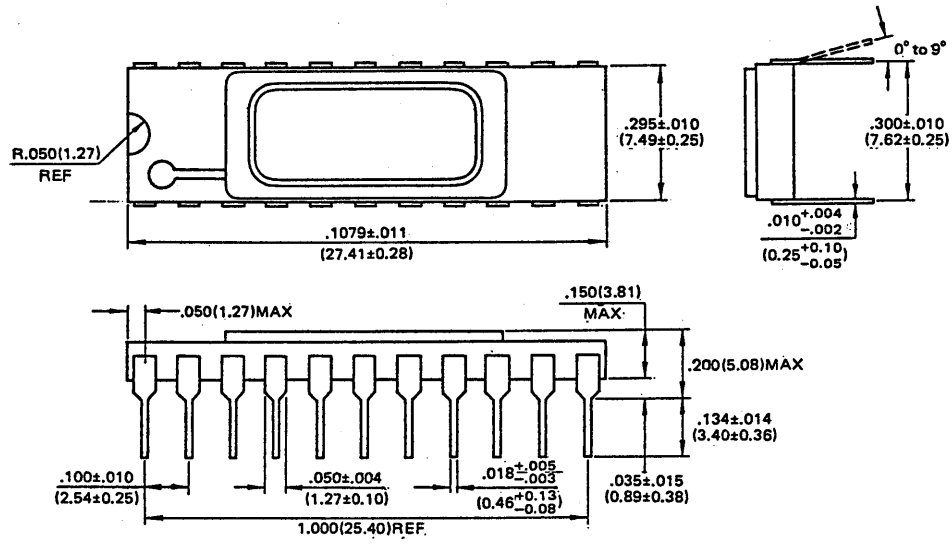


RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

PACKAGE DIMENSIONS

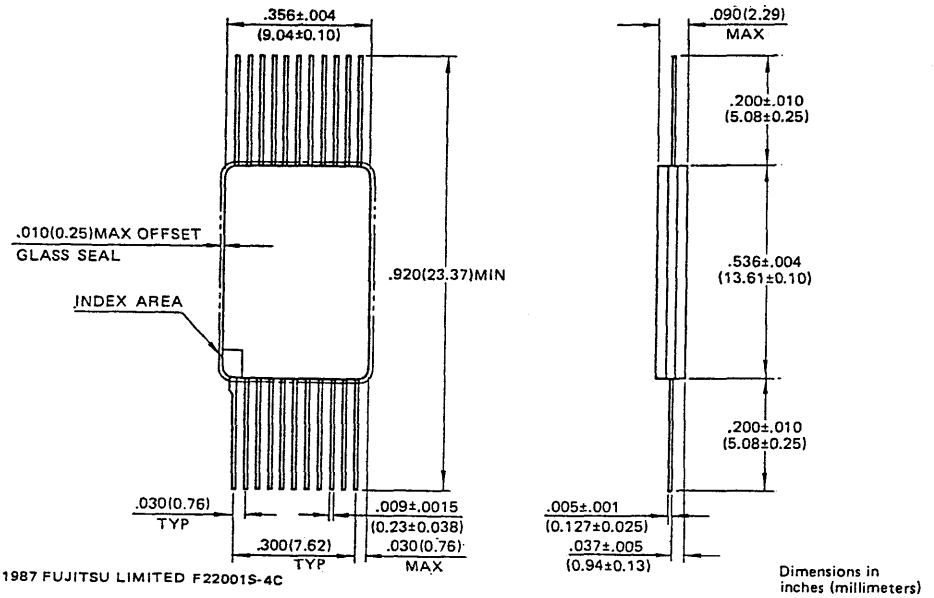
22-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE NO.: DIP-22C-A02)



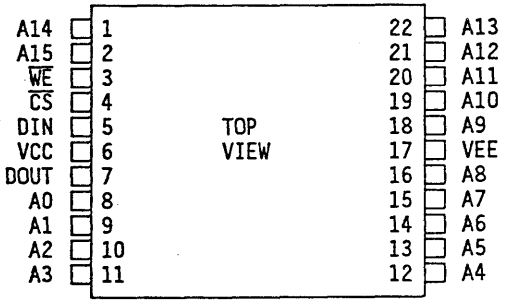
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

22-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE NO.: FPT-22C-C01)



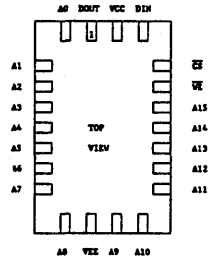
FLAT PACKAGE PIN ASSIGNMENTS



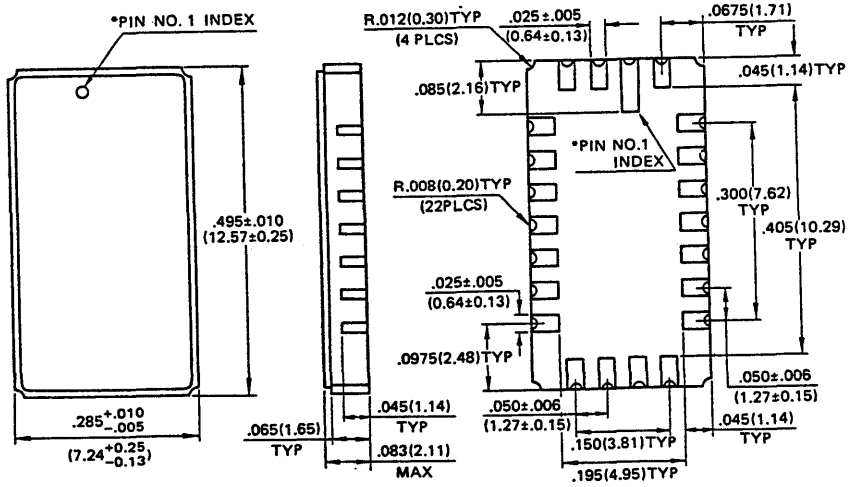
PACKAGE DIMENSIONS

LCC-22C-A01

PAD CONFIGURLATION



22-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIERS (CASE NO.: LCC-22C-A01)



*Share of PIN NO. 1 INDEX: Subject to changed without notice.

Dimensions in inches (millimeters)

FUJITSU

BICMOS 65536-BIT ECL RANDOM ACCESS MEMORY

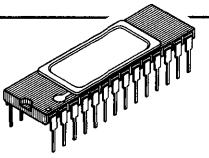
MBM10C494-15

TS311-C883
March 1988

PRELIMINARY

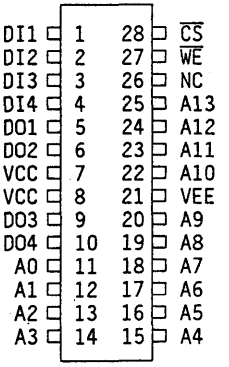
65536-BIT BICMOS ECL RANDOM ACCESS MEMORY

The Fujitsu MBM10C494 is fully decoded 65536 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by 4 bit, and it features on chip voltage compensation for improved noise margin.
Operation for the MBM10C494 is specified over an ambient temperature range of from 0°C to 75°C (TA). It is packaged in 28-pin ceramic DIP, flatpackage, LCC or plastic SOJ and fully compatible with industory standard 10K series ECL families.



CERAMIC PACKAGE
DIP-28C-A10

CERAMIC PACKAGE
FPT-28C-C03



PIN ASSIGNMENTS
LCC-28C-A02: See page 8
FPT-28P-M02: See page 9

- 16384 words x 4 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standard 10K series ECL families
- Address access time: 15ns max
  Chip select access time: 15ns max
- Power dissipation: 630 mW typ
- Open emitter output for ease of memory expansion
- BICMOS Processing
- 28-pin ceramic DIP (Suffix: C)
  28-pin ceramic FPT (Suffix: ZF)
  28-pin ceramic LCC (Suffix: CV)
  28-pin plastic SOJ (Suffix: PJ)

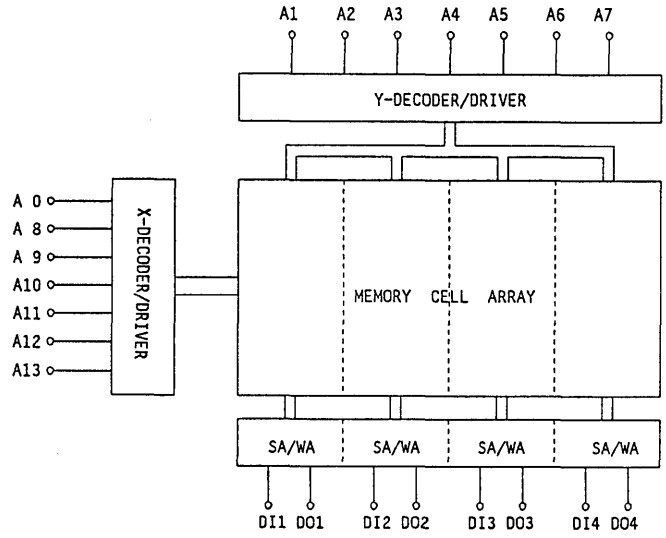
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig.1 - MBM10C494 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10C494 is fully decoded 65536 bit read/write random access memory organized as 16384 words by 4 bit. Memory cell selection is achieved by means of a 14-bit address designed A0 through A13. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient temperature(TA)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC=0V, VEE=-5.2V, Output Load = 50Ω to -2.0V, TA = 0°C to 75°C, Airflow ≥ 2.5 m/s unless other noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TA
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	I_{IH}			220	µA	0°Cto75°C
Input Low Current (VIN = VIL min)	I_{IL}	-50		90	µA	0°Cto75°C
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA	0°Cto75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-180			mA	0°Cto75°C

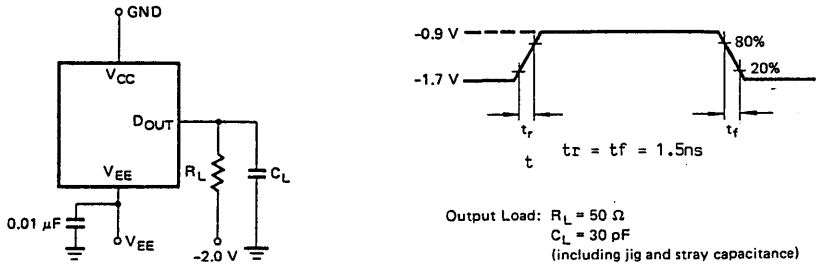
CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		TBD		pF
Output Pin Capacitance	C_{OUT}		TBD		pF

AC CHARACTERISTICS

(VCC=0V, VEE=-5.2V±5%, Output Load=50Ω to -2.0V and 30pF to GND, TA = 0°C to 75°C, Airflow ≥ 2.5 m/s unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS

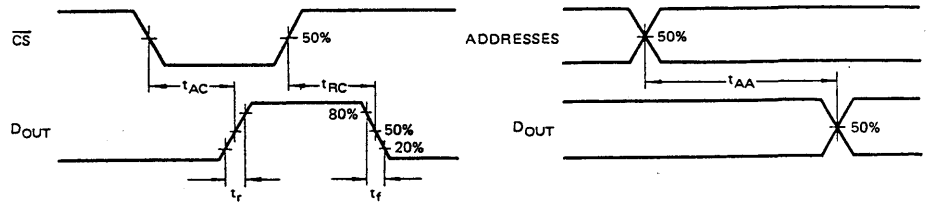


NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15.0	ns
Chip Select Access Time	t_{AC}			15.0	ns
Chip Select Recovery Time	t_{RC}			10.0	ns

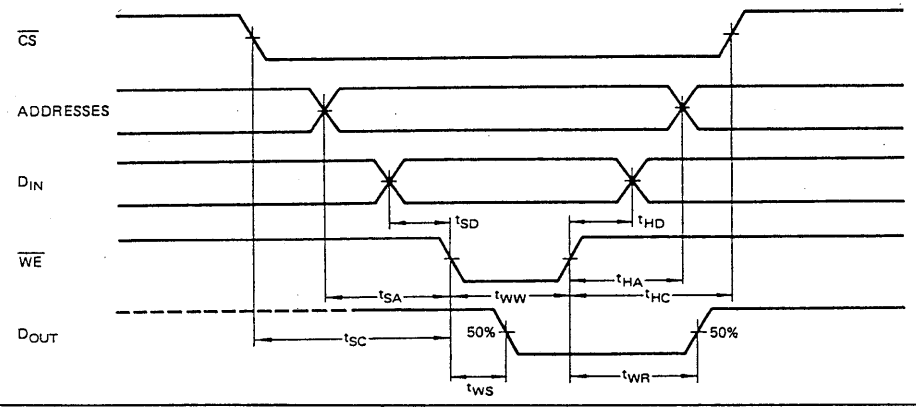
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}			10.0	ns
Write Recovery Time	t_{WR}			17.0	ns
Address Set Up Time	t_{SA}	3.0			ns
Chip Select Set Up Time	t_{SC}	3.0			ns
Data Set Up Time	t_{SD}	3.0			ns
Address Hold Time	t_{HA}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns

WRITE CYCLE TIMING DIAGRAM

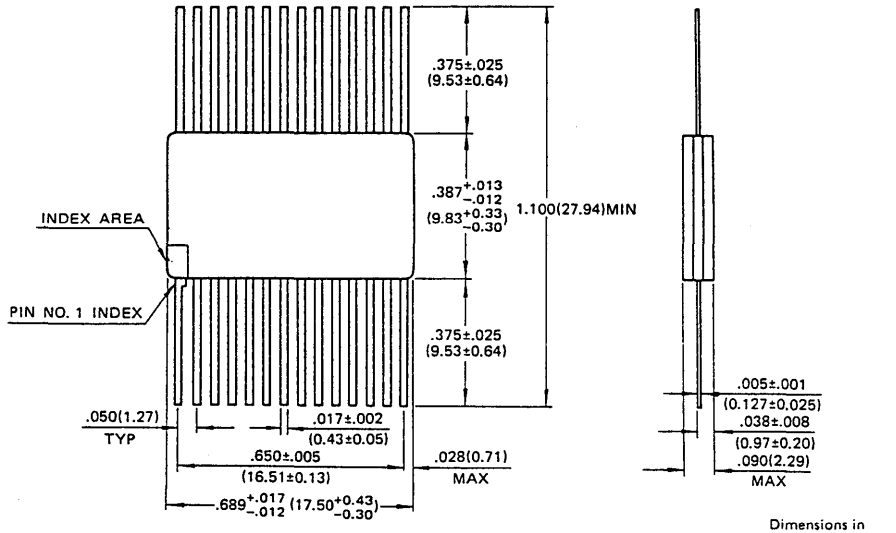


RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

PACKAGE DIMENSIONS

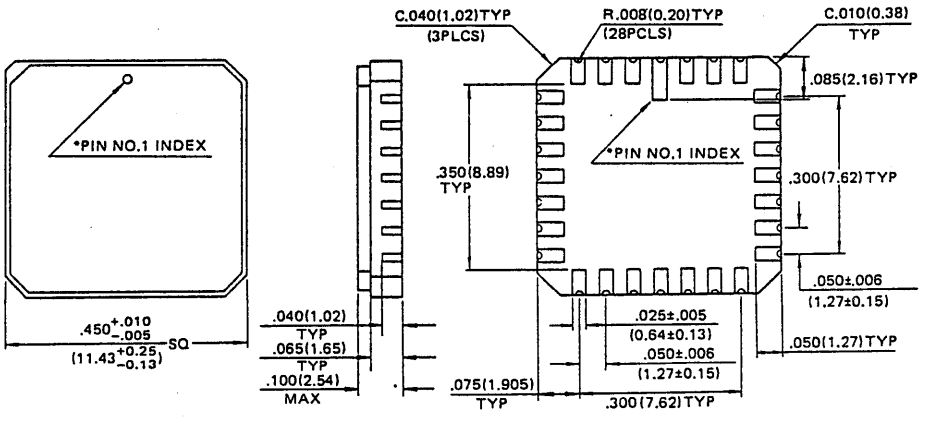
28-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE NO.: FPT-28C-C03)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

28-PAD CERAMIC (FRIT SEEL) LEEDLESS CHIP CARRIER
(CASE NO.: FPT-28C-A02)

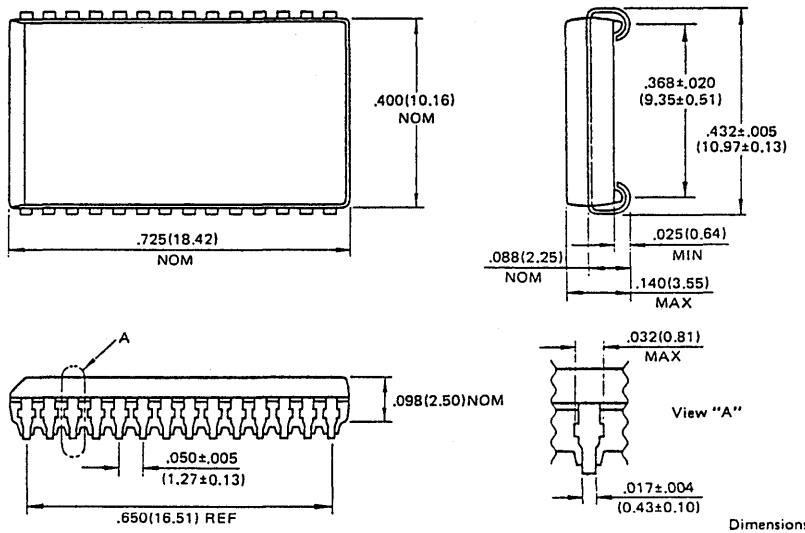


*Shape of Pin NO. 1 index : Subject to change without notice

Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE NO.: FPT-28P-M02)



Dimensions in inches (millimeters)

FUJITSU

BICMOS 65536-BIT ECL RANDOM ACCESS MEMORY

MBM100C494-15

November 1987
Edition 1.0

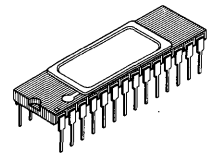
65536-BIT BICMOS ECL RANDOM ACCESS MEMORY

ADVANCE INFORMATION

The Fujitsu MBM100C494 is fully decoded 65536 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by 4 bit, and it features on chip voltage compensation for improved noise margin.

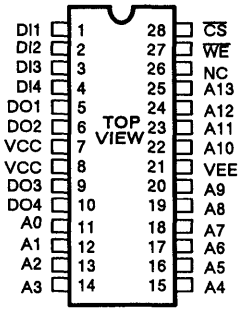
Operation for the MBM100C494 is specified over an ambient temperature range of from 0°C to 85°C (TA). It is packaged in 28-pin ceramic DIP, flatpackage, or LCC and fully compatible with industory standard 100K series ECL families.

- 16384 words x 4 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory-standard 100K series ECL families
- Address access time :15ns max.
  Chip select access time :15ns max.
- Power dissipation :590 mW typ
- Open emitter output for ease of memory expansion
- BICMOS Processing
- 28-pin ceramic DIP (Suffix: C)
  28-pin ceramic FPT (Suffix: ZF)
  28-pin ceramic LCC (Suffix: CV)



(DIP-28C-A10)

PIN ASSIGNMENT
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUJITSU

BICMOS 262144-BIT ECL RANDOM ACCESS MEMORY

MBM10C500-15

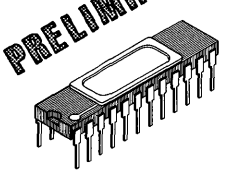
January 1988
Edition 1.0

262144-BIT BICMOS ECL RANDOM ACCESS MEMORY

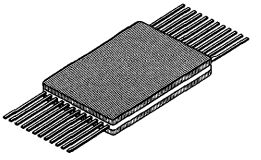
The Fujitsu MBM10C500 is fully decoded 262144 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 262144 words by one bit, and it features on chip voltage compensation for improved noise margin.
Operation for the MBM10C500 is specified over an ambient temperature range of from 0°C to 75°C (TA). It is packaged in 24-pin ceramic DIP, flatpackage, or LCC and fully compatible with industory standard 10K series ECL families.

- 262144 words by 1 bit organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standard 10K series ECL families
- Address access time: 15ns max
  Chip select access time: 15ns max
- Power dissipation: 650mW typ
- Open emitter output for ease of memory expansion
- BICMOS processing

PRELIMINARY



DIP-24C-A09

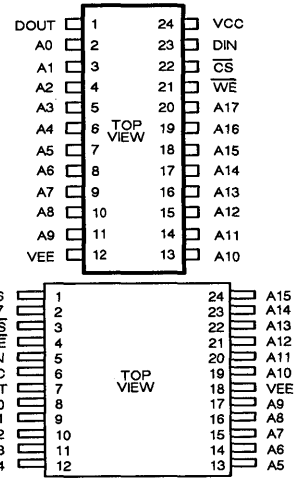


FPT-24C-C04

LCC-24C-A02, See page 7

2

PIN ASSIGNMENT



LCC PAD CONFIGURATION

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

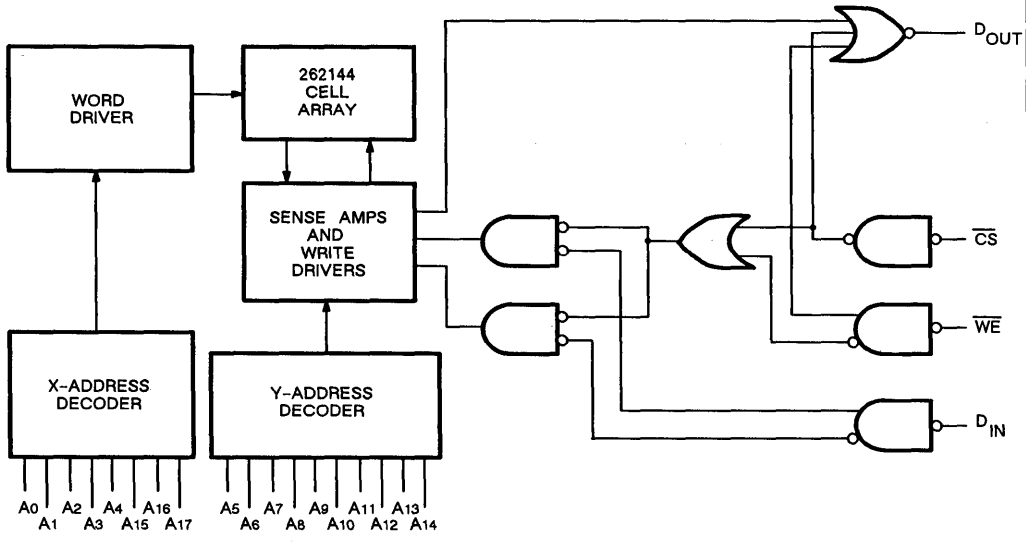
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
VEE Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 - MBM10C500 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{IN}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM10C500 is fully decoded 262144 bit read/write random access memory organized as 262144 words by 1 bit. Memory cell selection is achieved by means of a 18-bit addresses designed A_0 through A_{17}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature (TA)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC=0V, VEE=-5.2V, Output Load=50Ω to -2.0V, TA=0°C to 75°C, Airflow ≧ 2.5 m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TA
Output High Voltage (VIN = VIH max or VIL min)	VOH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	VOL	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	VOHC	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	VOLC			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	VIH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	VIL	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	IIH			220	μA	0°C to 75°C
Input Low Current (VIN = VIL min)	IIL	-50		90	μA	0°C to 75°C
CS Input Low Current (VIN = VIL min)	IIL	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Outputs Open)	IEE	-200			mA	0°C to 75°C

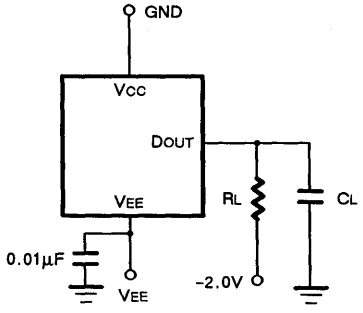
CAPACITANCE

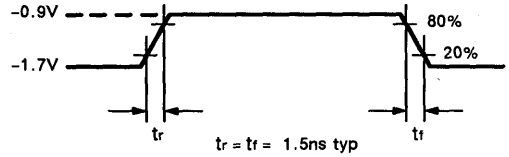
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	CIN		TBD		pF
Output Pin Capacitance	COUT		TBD		pF

AC CHARACTERISTICS

(VCC=0V, VEE=-5.2V± 5%, Output Load =50Ω to -2.0V and 30pF to GND, TA=0°C to 75°C, Airflow ≧ 2.5 m/s, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



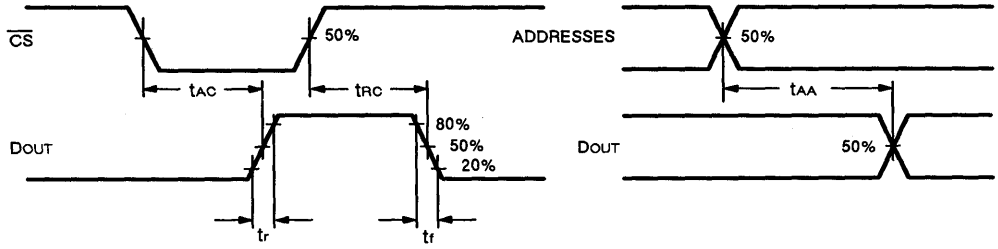


Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

Parameter	Symbol	Min	Typ	Max	Unit
READ CYCLE					
Address Access Time	t_{AA}			15.0	ns
Chip Select Access Time	t_{AC}			15.0	ns
Chip Select Recovery Time	t_{RC}			10.0	ns

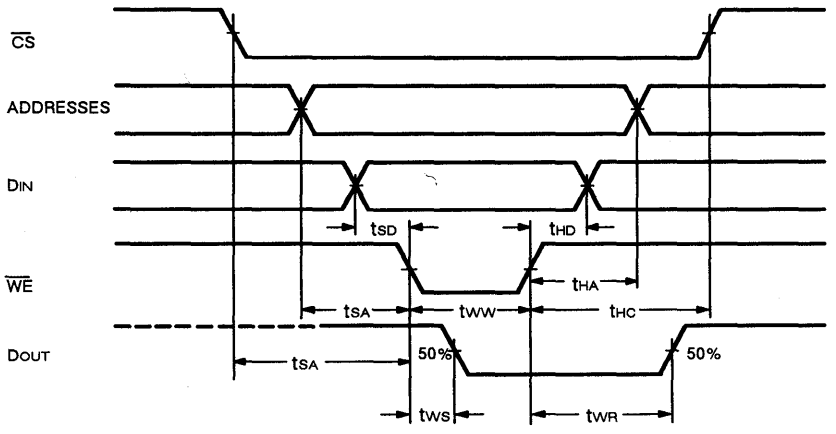
READ CYCLE TIMING DIAGRAM



Parameter	Symbol	Min	Typ	Max	Unit
WRITE CYCLE					
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}			10.0	ns
Write Recovery Time	t_{WR}			15.0	ns
Address Set Up Time	t_{SA}	3.0			ns
Chip Select Set Up Time	t_{SC}	3.0			ns
Data Set Up Time	t_{SD}	3.0			ns
Address Hold Time	t_{HA}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns

2

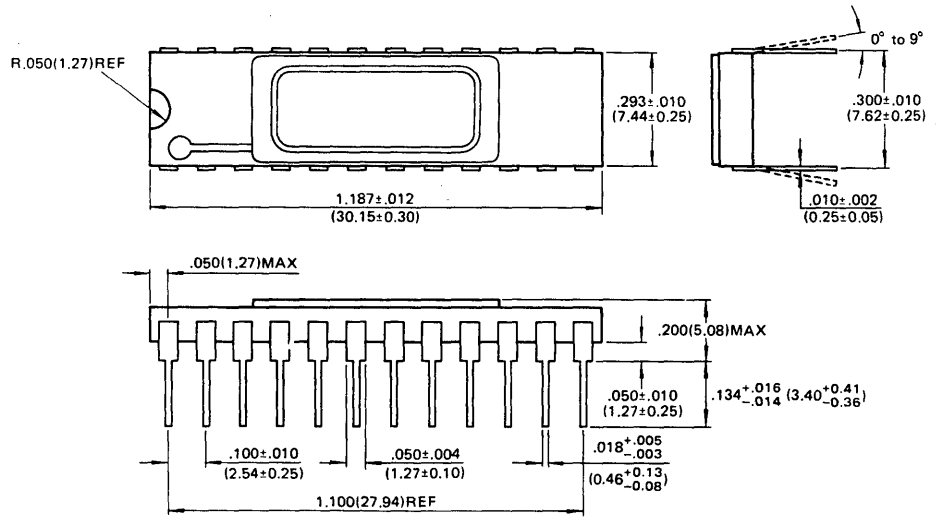
WRITE CYCLE TIMING DIAGRAM



Parameter	Symbol	Min	Typ	Max	Unit
RISE TIME and FALL TIME					
Output Rise Time	tr		TBD		ns
Output Fall Time	tf		TBD		ns

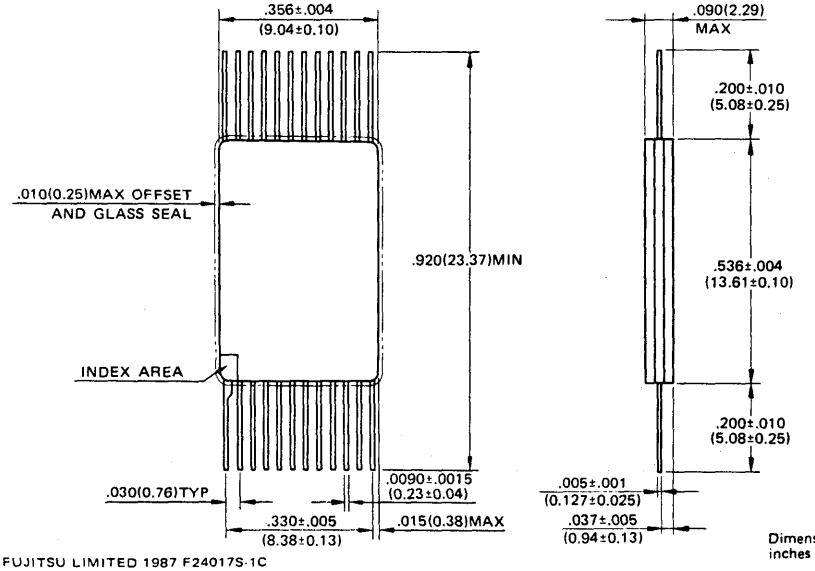
PACKAGE DIMENSIONS

24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE (CASE NO.: DIP-24C-A09)



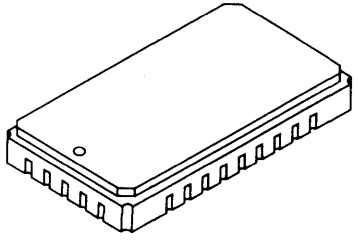
Dimensions in inches (millimeters)

24-LEAD CERAMIC (CERDIP) FLAT PACKAGE (CASE NO.: FPT-24C-C04)



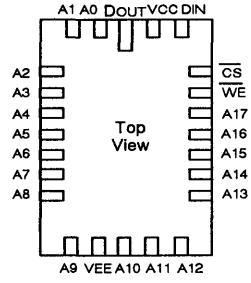
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

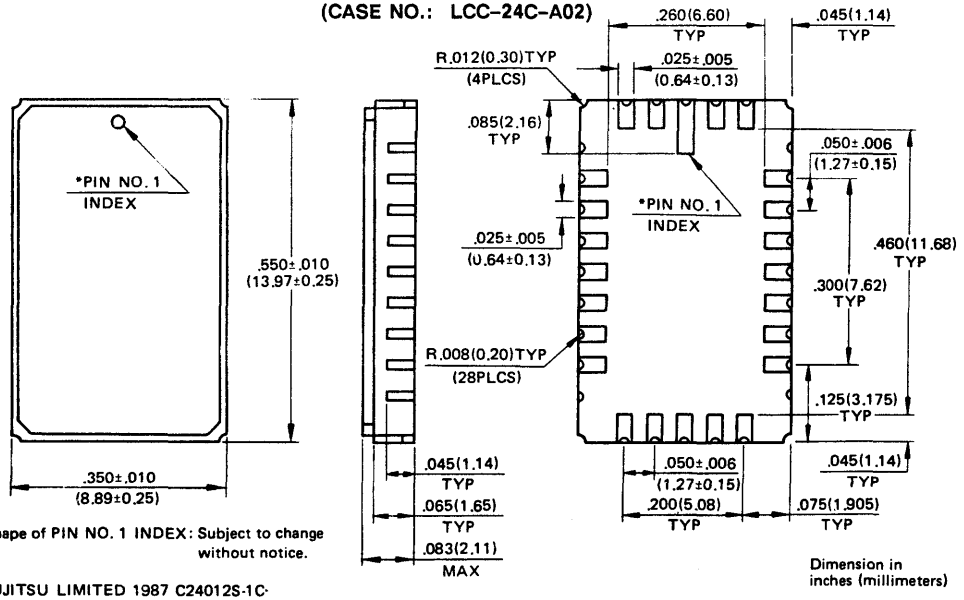


LCC-24C-A02

PAD CONFIGULATION



24-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE NO.: LCC-24C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in inches (millimeters)

FUJITSU

BICMOS 262144-BIT ECL RANDOM ACCESS MEMORY

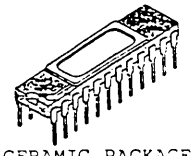
MBM101C500-15

TS319-D883
March 1988

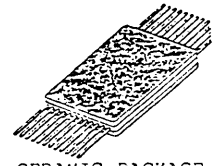
PRELIMINARY

262144-BIT BICMOS ECL RANDOM ACCESS MEMORY

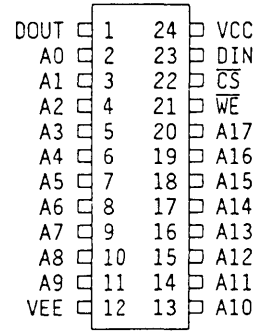
The Fujitsu MBM101C500 is fully decoded 262144 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 262144 words by one bit, and it features on chip voltage compensation for improved noise margin.
Operation for the MBM101C500 is specified over an ambient temperature range of from 0°C to 75°C (TA). It is packaged in 24-pin ceramic DIP, flatpackage, or LCC. It is compatible with industory standard 100K series ECL I/O levels with -5.2V supply voltage.



CERAMIC PACKAGE
DIP-24C-A09



CERAMIC PACKAGE
FPT-24C-C04



PIN ASSIGNMENTS
LCC-24C-A02 : See page 8

- 262144 words by 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Compatible with industory standard 100K series ECL I/O levels with -5.2V supply voltage
- Address access time: 15 ns max
  Chip select access time: 15 ns max
- Power dissipation: 650 mW typ

- Open emitter output for ease of memory expansion
- BICMOS Processing
- 24-pin ceramic DIP (Suffix: C)
  24-pin ceramic FPT (Suffix: ZF)
  24-pin ceramic LCC (Suffix: CV)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

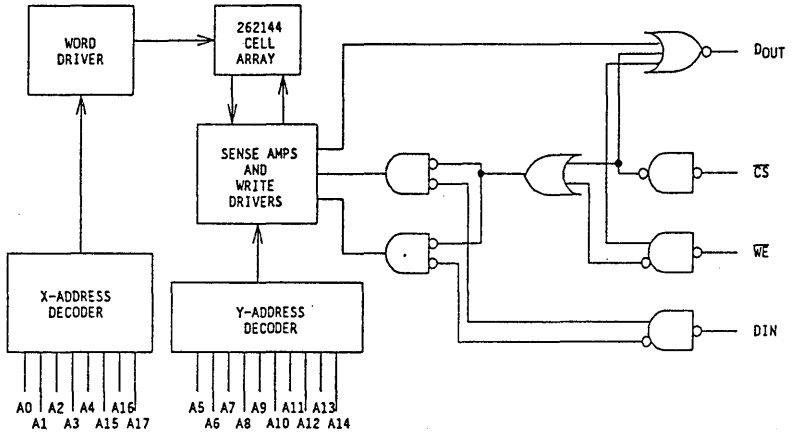
Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

2

Fig.1 - MBM101C500 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM101C500 is fully decoded 262144 bit read/write random access memory organized as 262144 words by 1 bit. Memory cell selection is achieve by means of a 18-bit address designed A0 through A17. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

PRELIMINARY

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient temperature(TA)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC=0V, VEE=-5.2V, Output Load = 50Ω to -2.0V, TA = 0°C to 75°C, Airflow ≥ 2.5 m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810		-1650	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1850		-1475	mV
Input High Current (VIN = VIH max)	I_{IH}			220	µA
Input Low Current (VIN = VIL min)	I_{IL}	-50		90	µA
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and Outputs Biased)	I_{EE}	-200			mA

CAPACITANCE

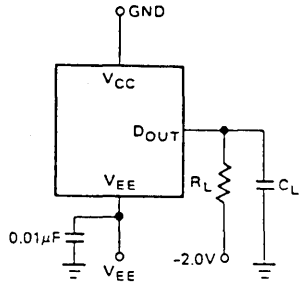
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		TBD		pF
Output Pin Capacitance	C_{OUT}		TBD		pF

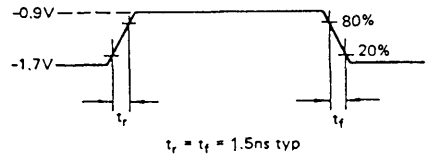
PRELIMINARY

AC CHARACTERISTICS

(VCC=0V, VEE=-5.2V±5%, Output Load=50Ω to -2.0V and 30pF to GND, TA = 0°C to 75°C, Airflow ≥ 2.5 m/s, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS





$t_r = t_f = 1.5ns$ typ

Output Load: $R_L = 50\Omega$
$C_L = 30pF$
(including scope and jig)

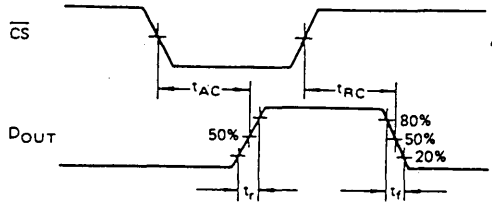
NOTE: All timing measurements referenced to 50% input levels.

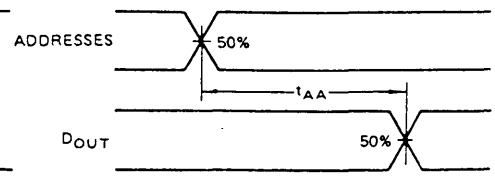
2

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15.0	ns
Chip Select Access Time	t_{AC}			15.0	ns
Chip Select Recovery Time	t_{RC}			10.0	ns

READ CYCLE TIMING DIAGRAM



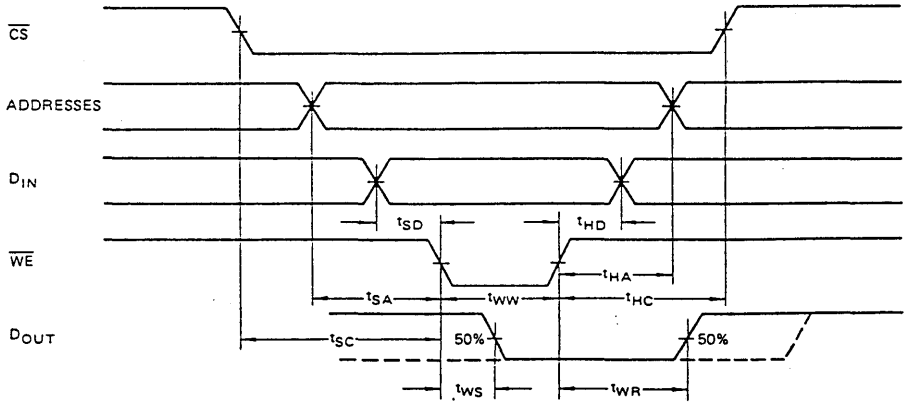


PRELIMINARY

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}			10.0	ns
Write Recovery Time	t_{WR}			15.0	ns
Address Set Up Time	t_{SA}	3.0			ns
Chip Select Set Up Time	t_{SC}	3.0			ns
Data Set Up Time	t_{SD}	3.0			ns
Address Hold Time	t_{HA}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns

WRITE CYCLE TIMING DIAGRAM



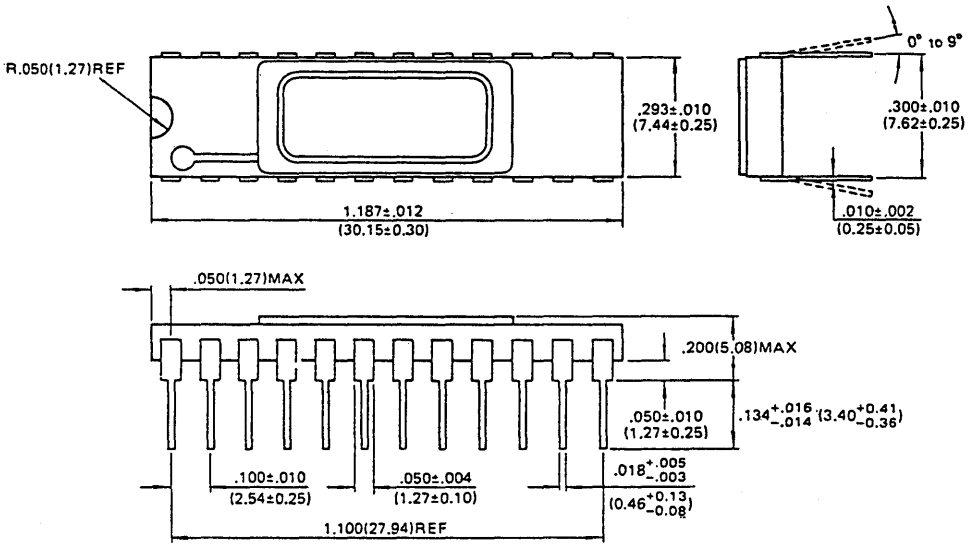
RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

PRELIMINARY

PACKAGE DIMENSIONS

24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE NO.: DIP-24C-A09)

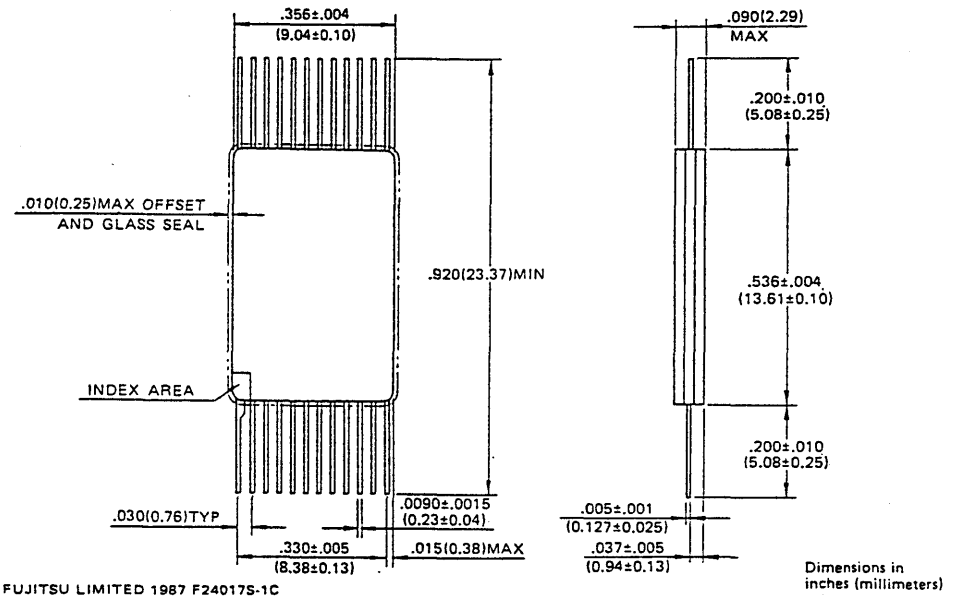


Dimensions in inches (millimeters)

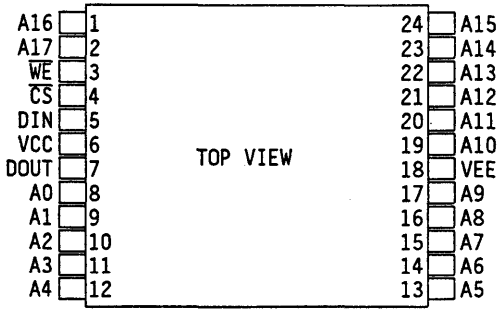
PRELIMINARY

PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) FLAT PACKAGE
(CASE NO.: FPT-24C-C04)

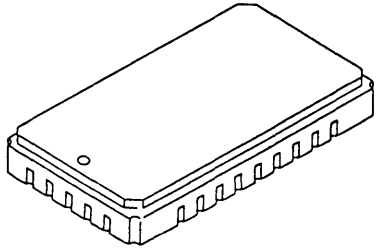


FLAT PACKAGE PIN ASSIGNMENTS



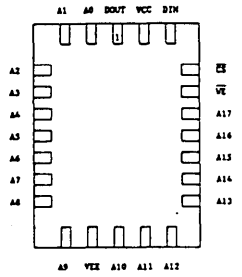
PRELIMINARY

PACKAGE DIMENSIONS



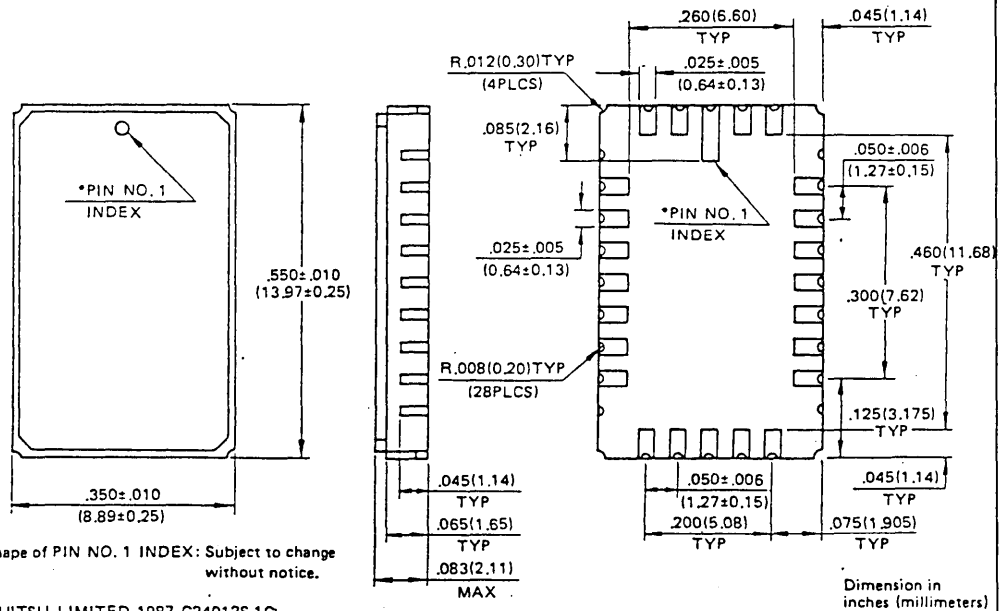
LCC-24C-A02

PAD CONFIGULATION



2

24-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIERS (CASE NO.: LCC-24C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in inches (millimeters)

FUJITSU

BICMOS 262144-BIT ECL RANDOM ACCESS MEMORY

MBM100C500-15

May 1988
Edition 1.0

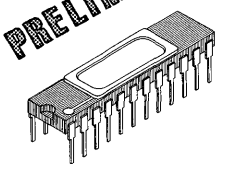
262144-BIT BICMOS ECL RANDOM ACCESS MEMORY

The Fujitsu MBM100C500 is fully decoded 262144 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 262144 words by one bit, and it features on chip voltage compensation for improved noise margin.

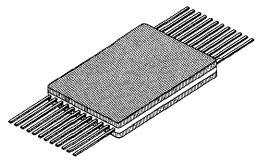
Operation for the MBM100C500 is specified over an ambient temperature range of from 0°C to 85°C (TA). It is packaged in 24-pin ceramic DIP, flatpackage, or LCC and fully compatible with industory standard 100K series ECL families.

- 262144 words by 1 bit organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standard 100K series ECL families
- Address access time: 15ns max
  Chip select access time: 15ns max
- Power dissipation: 550mW typ
- Open emitter output for ease of memory expansion
- BICMOS Processing

PRELIMINARY



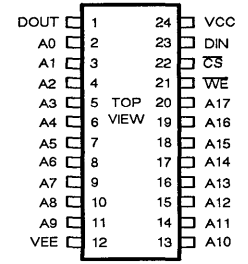
DIP-24C-A09

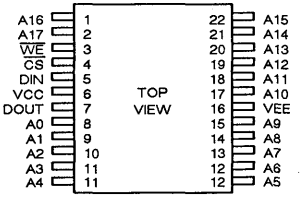


FPT-24C-C04

LCC-24C-A02: See page 7

PIN ASSIGNMENT





LCC Pad Configuration: See page 7

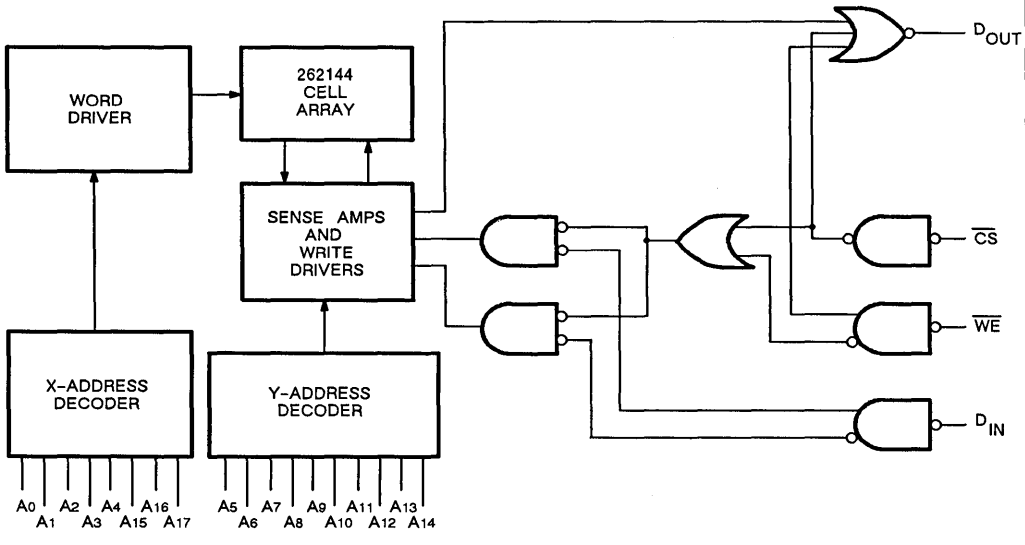
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
VEE Pin Potential to ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 - MBM100C500 BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	D_{IN}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100C500 is fully decoded 262144 bit read/write random access memory organized as 262144 words by 1 bit. Memory cell selection is achieved by means of a 18-bit address designed A_0 through A_{17}. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature (TA)
Supply Voltage	VEE	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(VCC=0V, VEE=-4.5V, Output Load=50Ω to -2.0V, TA = 0°C to 85°C, Airflow ≧2.5 m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN =VIH max or VIL min)	VOH	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	VOL	-1810		-1650	mV
Output High Voltage (VIN = VIH min or VIL max)	VOHC	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	VOLC			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for all Inputs)	VIH	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for all Inputs)	VIL	-1850		-1475	mV
Input High Current (VIN = VIH max)	IIH			220	µA
Input Low Current (VIN = VIL min)	IIL	-50		90	µA
$\overline{CS}$ Input Low Current (VIN=VIL min)	IIL	0.5		170	µA
Power Supply Current (All Inputs and Outputs Open)	IEE	-200			mA

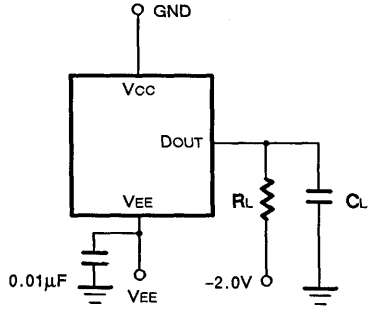
CAPACITANCE

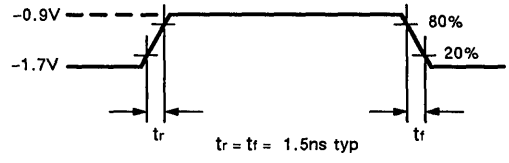
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	CIN		TBD		pF
Output Pin Capacitance	COUT		TBD		pF

AC CHARACTERISTICS

(VCC=0V, VEE=-4.5V±5%, Output Load=50Ω to -2.0V and 30pF to GND, TA=0°C to 85°C, Airflow ≧ 2.5m/s, unless otherwise noted.)

Fig. 2 - AC TEST CONDITIONS



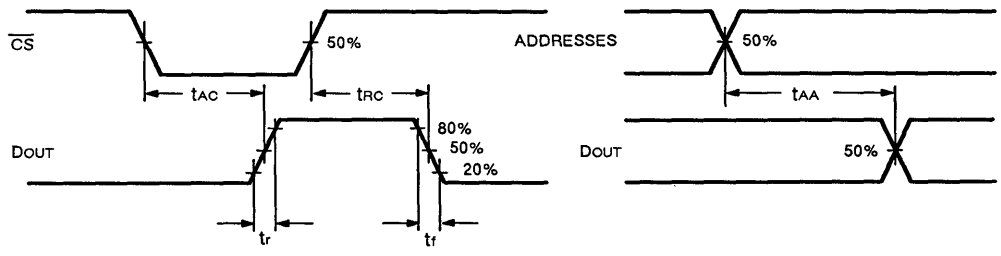


Output Load: RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

Parameter	Symbol	Min	Typ	Max	Unit
READ CYCLE					
Address Access Time	tAA			15.0	ns
Chip Select Access Time	tAC			15.0	ns
Chip Select Recovery Time	tRC			10.0	ns

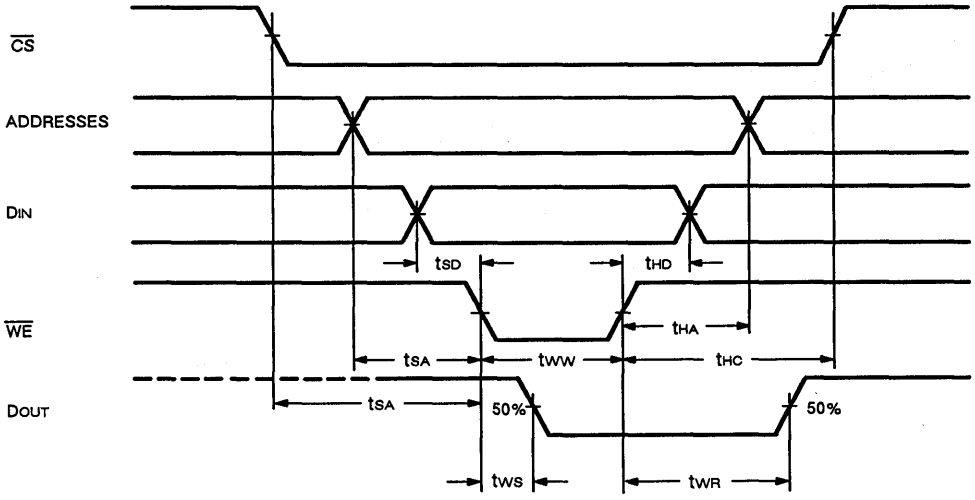
READ CYCLE TIMING DIAGRAM



Parameter	Symbol	Min	Typ	Max	Unit
WRITE CYCLE					
Write Pulse Width	tWW	10.0			ns
Write Disable Time	tWS			10.0	ns
Write Recovery Time	tWR			15.0	ns
Address Set Up Time	tSA	3.0			ns
Chip Select Set Up Time	tSC	3.0			ns
Data Set Up Time	tSD	3.0			ns
Address Hold Time	tHA	2.0			ns
Chip Select Hold Time	tHC	2.0			ns
Data Hold Time	tHD	2.0			ns

2

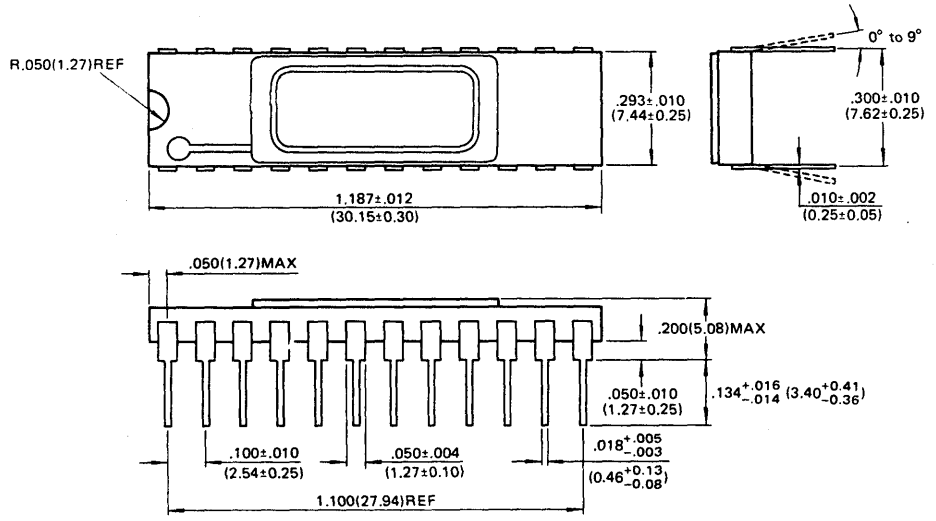
WRITE CYCLE TIMING DIAGRAM



Parameter	Symbol	Min	Typ	Max	Unit
RISE TIME and FALL TIME					
Output Rise Time	tr		TBD		ns
Output Fall Time	tf		TBD		ns

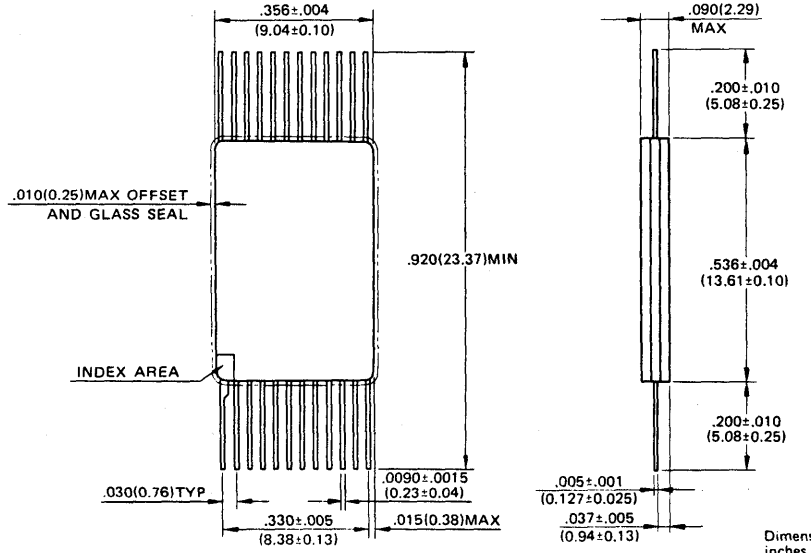
PACKAGE DIMENSIONS

24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE (CASE NO.: DIP-24C-A09)



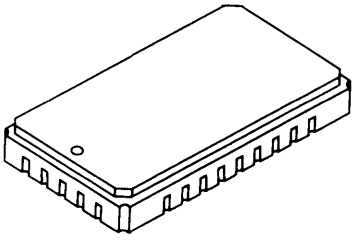
Dimensions in inches (millimeters)

24-LEAD CERAMIC (CERDIP) FLAT PACKAGE (CASE NO.: FPT-24C-C04)



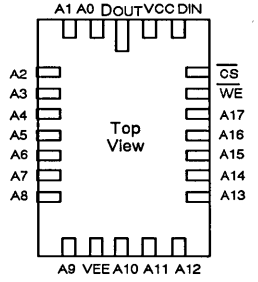
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)



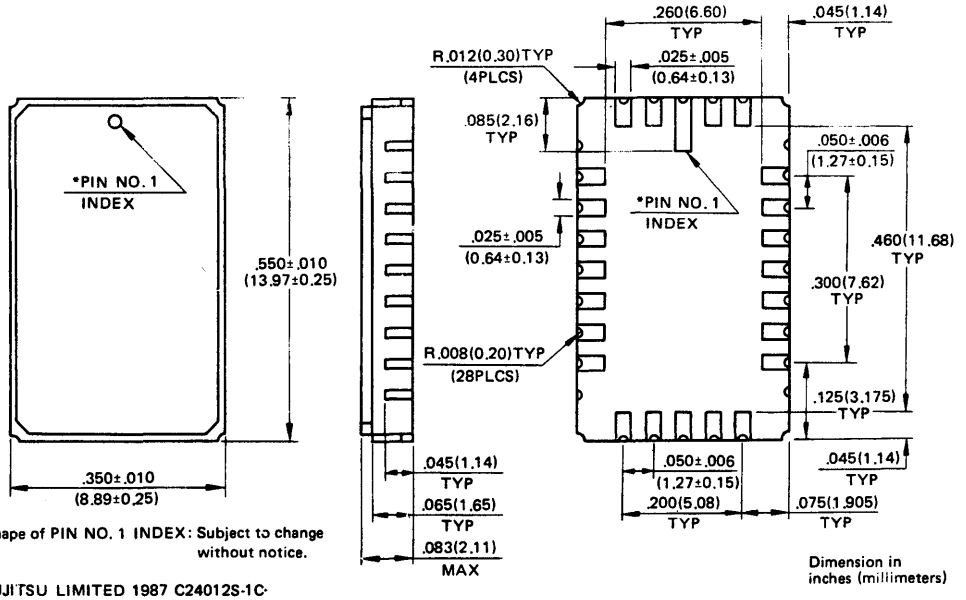
LCC-24C-A02

PAD CONFIGULATION



2

24-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIERS
(CASE NO.: LCC-24C-A02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimension in inches (millimeters)

FUJITSU

BICMOS 262144-BIT ECL RANDOM ACCESS MEMORY

MBM100C504-15

TS324-A888
August 1988

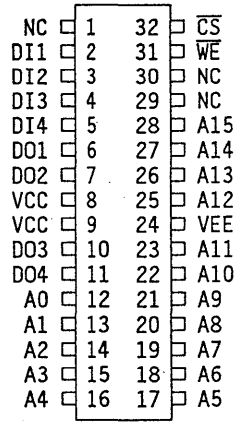
262144-BIT BICMOS ECL RANDOM ACCESS MEMORY

ADVANCE INFO.

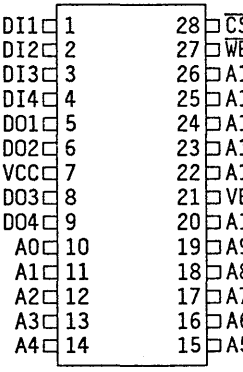
The Fujitsu MBM100C504 is fully decoded 262144 bit BICMOS ECL random access memory designed for main memory, control and buffer storage applications. This device is organized as 65536 words by 4 bit, and it features on chip voltage/temperature compensation for improved noise margin. Operation for the MBM100C504 is specified over a temperature range of from 0°C to 85°C (TA for DIP and TC for FPT). It is packaged in 32-pin ceramic DIP and 28-pin ceramic FPT and fully compatible with industory standard 100K series ECL families.

- 65536 words x 4 organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standard 100K series ECL families
- Address access time: 15ns max
  Chip select access time: 15ns max
- Power dissipation: -220mA min
- Open emitter output for ease of memory expansion
- BICMOS Processing
- Package: 32-pin ceramic DIP (Suffix: C)
  28-pin ceramic FPT (Suffix: ZF)

Pin Assignments for DIP



Pin Assignments for FPT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to VEE	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under Bias	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

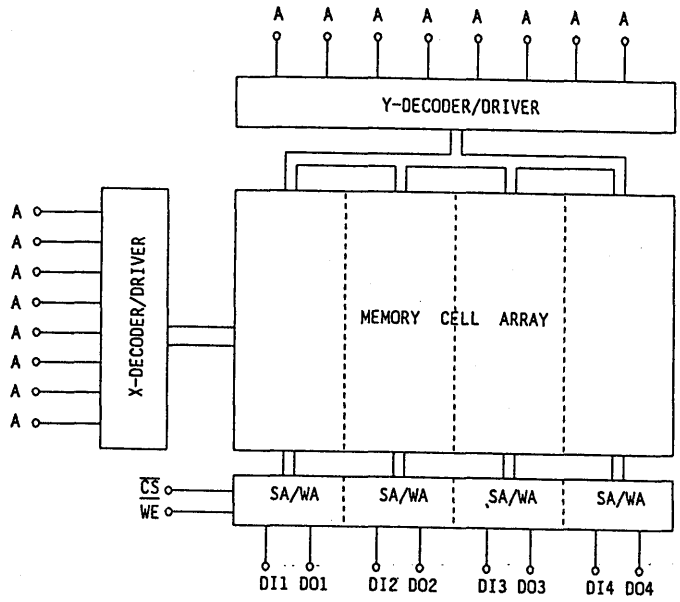
Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

NOTE: *Permanent device damage may occur of ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation* should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ADVANCE INFO.

2

Fig.1 - MBM100C504 BLOCK DIAGRAM



TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}		
H	X	X	L	Disabled
L	L	H	L	Write "H"
L	L	L	L	Write "L"
L	H	X	D_{OUT}	Read

Notes:
H = High Voltage Level
L = Low Voltage Level
X = Don't Care

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100C504 is fully decoded 262144 bit read/write random access memory organized as 65536 words by 4 bit. Memory cell selection is achieve by means of a 16-bit address designated A0 through A15. The active low Chip Select ($\overline{CS}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$ and $\overline{CS}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. Data at the addressed location is then transferred to DOUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

ADVANCE INFO

GUARANTEED OPERATING CONDITIONS
(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient temperature(TA)
Supply Voltage	V_{EE}	-4.725	-4.5	-4.275	V	0°C to 85°C

DC CHARACTERISTICS
(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TA = 0°C to 85°C for DIP, Airfloe ≥ 2.5m/s, TC = 0°C to 85°C for Flat Package, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (VIN = VIH max or VIL min)	V_{OH}	-1025		-880	mV
Output Low Voltage (VIN = VIH max or VIL min)	V_{OL}	-1810		-1620	mV
Output High Voltage (VIN = VIH min or VIL max)	V_{OHC}	-1035			mV
Output Low Voltage (VIN = VIH min or VIL max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (VIN = VIH max)	I_{IH}			220	µA
Input Low Current (VIN = VIL min)	I_{IL}	-50		90	µA
CS Input Low Current (VIN = VIL min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and Outputs Biased)	I_{EE}	-220			mA

CAPACITANCE

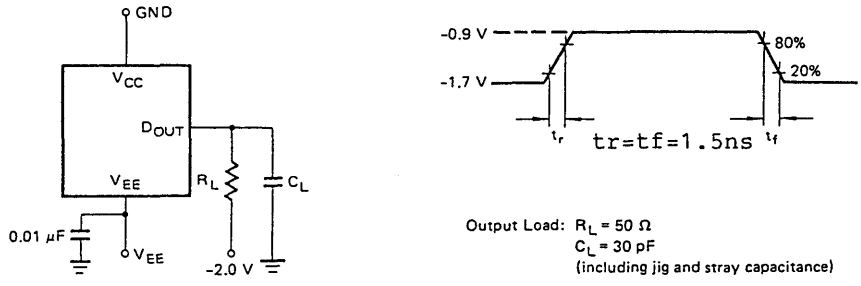
Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		TBD		pF
Output Pin Capacitance	C_{OUT}		TBD		pF

ADVANCE INFO

AC CHARACTERISTICS

(VCC=0V, VEE=-4.5V±5%, Output Load=50Ω to -2.0V and 30pF to GND, TA=0°C to 85°C for DIP, Airflow ≥ 2.5 m/s, TC=0°C to 85°C for Flat Package, unless otherwise noted.)

Fig. 2 – AC TEST CONDITIONS



Output Load: R_L = 50 Ω
C_L = 30 pF
(including jig and stray capacitance)

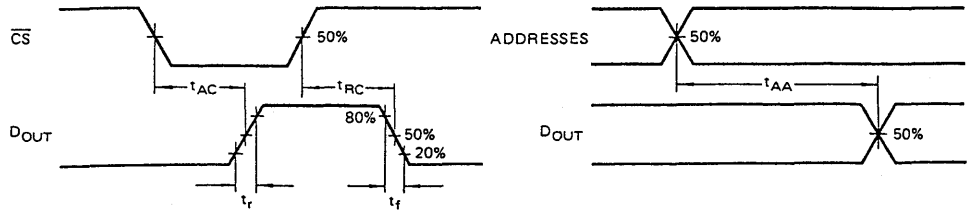
NOTE: All timing measurements referenced to 50% input levels.

2

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}			15.0	ns
Chip Select Access Time	t_{AC}			15.0	ns
Chip Select Recovery Time	t_{RC}			10.0	ns

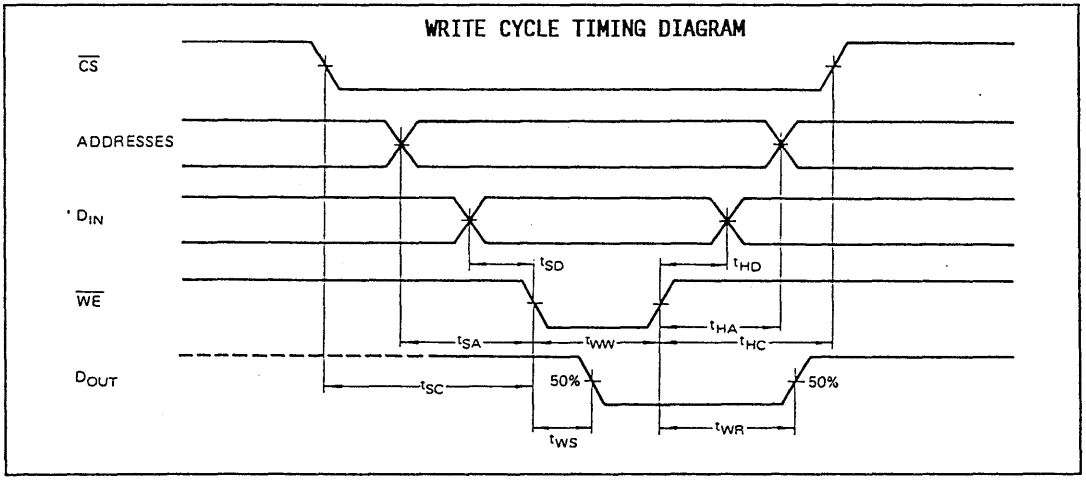
READ CYCLE TIMING DIAGRAM



ADVANCE INFO.

WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	10.0			ns
Write Disable Time	t_{WS}			10.0	ns
Write Recovery Time	t_{WR}			15.0	ns
Address Set Up Time	t_{SA}	3.0			ns
Chip Select Set Up Time	t_{SC}	3.0			ns
Data Set Up Time	t_{SD}	3.0			ns
Address Hold Time	t_{HA}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns



RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		TBD		ns
Output Fall Time	t_f		TBD		ns

Section 3

Application-Specific RAMs

Page	Device	Maximum Access Time (ns)	Capacity	Package Options
3-3	MBM10423LL-6	6	1024 bits (256w x 4b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
3-15	MBM100423LL-6	6	1024 bits (256w x 4b)	24-pin Ceramic DIP 24-pin Ceramic FPT 24-pad Ceramic LCC
3-27	MBM10476LL-9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3-39	MBM10476RR-9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3-49	MBM10476RL-9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3-59	MBM100476LL-9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3-71	MBM100476RR-9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3-81	MBM100476RL-9	9	4096 bits (1024w x 4b)	28-pin Ceramic DIP
3-91	MBM10486LL-13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3-103	MBM10486RR-13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3-105	MBM10486RL-13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3-107	MBM100486LL-13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3-119	MBM100486RR-13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3-121	MBM100486RL-13	13	16384 bits (4096w x 4b)	28-pin Ceramic DIP
3-123	MB7700H Series	5	4096 bits (256w x 16b)	60-pin Ceramic FPT

3

FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10423LL-6

October 1987
Edition 2.0

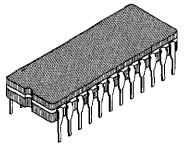
1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10423LL is fully decoded 1024-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4 bits with address input and output latches. Generally in the system, preceeding logic IC is needed for the synchronous entry of asynchronous address signal inputs of the RAM. MBM 10423LL contains internal latch circuits so that it can take synchronous address input and output timing, which contribute to higher system performance and save of power dissipation and board area. And it features on-chip voltage compensation for improved noise margin.

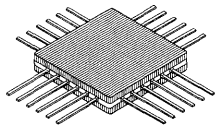
The MBM 10423LL offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 10423LL is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin Ceramic DIP, Flat Package, or LCC and is fully compatible with industry standard 10K-series ECL families.

- 256 words x 4 bits organization
- Address input and output latches which can be controlled separately
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry standard 10K-series ECL families
- Latch cycle time: 6 ns max.
- Address access time: 5 ns max.
- Block select access time: 3 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.84 mW/bit
- DOPOS and IOP-II



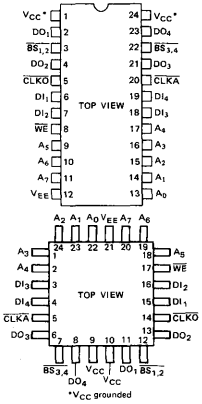
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See Page 11

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

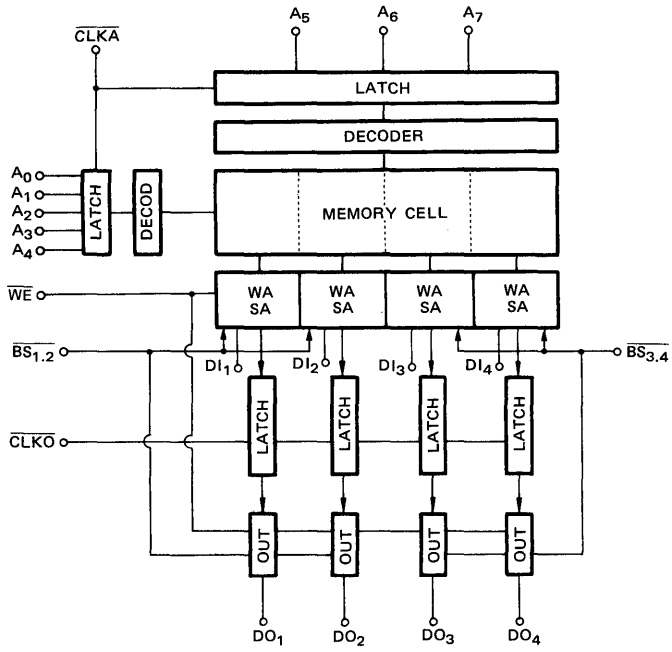
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A for DIP	−55 to +125	°C
	T_C for Flat Package and LCC	−55 to +125	
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MBM 10423LL BLOCK DIAGRAM



Symbol	Pin Name	Symbol	Pin Name
$A_0 \sim A_7$	Address Input	$\overline{CLKA}$	Address Latch Clock
$DI_1 \sim DI_4$	Data Input	$\overline{CLKO}$	Output Latch Clock
$DO_1 \sim DO_4$	Data Output	V_{EE}	Power Supply (-5.2V)
$\overline{WE}$	Write Enable	V_{CC}	Power Supply (0V)
$\overline{BS_{1.2}}, \overline{BS_{3.4}}$	Block Select		

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10423LL is fully decoded 1024 bit read/write random access memory organized as 256 words by 4 bits with address input and output latches which can be controlled separately by $\overline{CLKA}$ and $\overline{CLKO}$ pins. When clock is in high state, data is latched, while clock is held low, data goes through the latches like as conventional MBM 10422A. Memory cell selection is achieved by means of a 8-bit address designated A_0 through A_7. The active low Block Select inputs are provided for memory expansion. Two separate blocks are selected simultaneously by $\overline{BS_{1.2}}$ or $\overline{BS_{3.4}}$ pin. The read and write operation are controlled by the state of active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$, $\overline{BS_{1.2}}$ and/or $\overline{BS_{3.4}}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{BS_{1.2}}$ and/or $\overline{BS_{3.4}}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94 V	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for flat package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{BS}$ and $\overline{CLKA}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	-220			mA	0°C to 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		6	7	pF

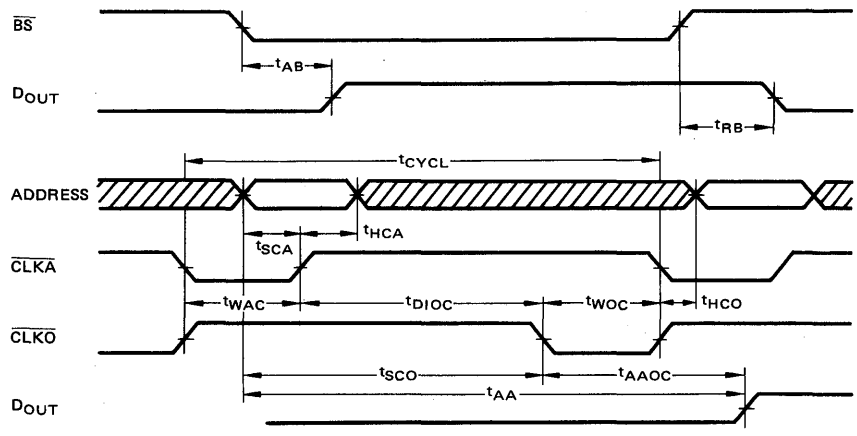
AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V ± 5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≥ 2.5m/s, T_C = 0°C to 75°C for Flatpackage and LCC, unless otherwise noted.)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	1.5		5.0	ns
Output Latch Access Time	t_{AAOC}	0.5		3.0	ns
Block Select Access Time	t_{AB}	0.5		3.0	ns
Block Select Recovery Time	t_{RB}	0.5		3.0	ns
Address Latch Clock Pulse Width	t_{WAC}	2.5			ns
Output Latch Clock Pulse Width	t_{WOC}	2.5			ns
Address Latch Clock Setup Time	t_{SCA}	1.5			ns
Address Latch Clock Hold Time	t_{HCA}	2.0			ns
Output Latch Clock Setup Time	t_{SCO}	2.5			ns
Output Latch Clock Hold Time	t_{HCO}	1.0			ns
Delay Time Between Input Clock and Output Clock	t_{DIOC}	1.0			ns
Latch Cycle Time	t_{CYCL}	6.0			ns

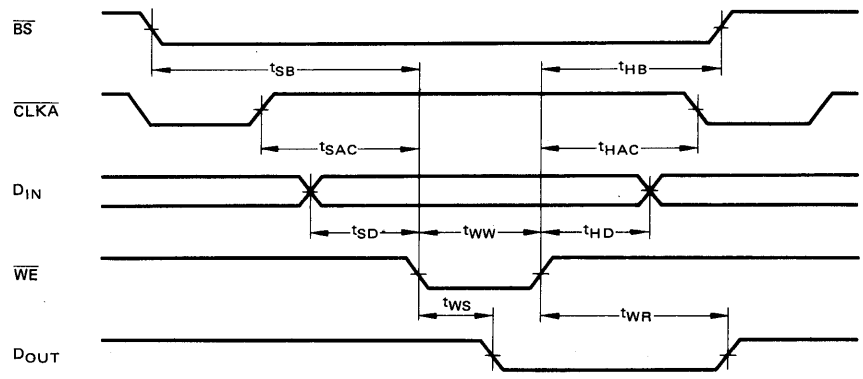
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	3.5			ns
Write Disable Time	t_{WS}	0.5		3.5	ns
Write Recovery Time	t_{WR}	0.5		3.5	ns
Write Clock Setup Time	t_{SAC}	−1.5			ns
Block Select Setup Time	t_{SB}	0.5			ns
Data Setup Time	t_{SD}	0.5			ns
Write Clock Hold Time	t_{HAC}	1.5			ns
Block Select Hold Time	t_{HB}	1.0			ns
Data Hold Time	t_{HD}	1.0			ns

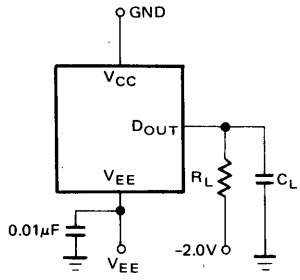
WRITE CYCLE TIMING DIAGRAM

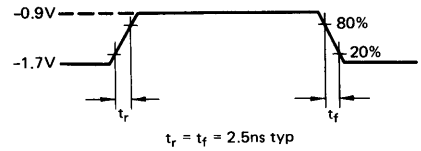


RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

Fig. 2 – AC TEST CONDITIONS





$t_r = t_f = 2.5$ns typ

Output Load: $R_L = 50\Omega$
$C_L = 30$pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

3

FUNCTIONAL TRUTH TABLE

$\overline{BS}$	$\overline{WE}$	DI	$\overline{CLKA}$	$\overline{CLKO}$	OUTPUT	MODE
H	X	X	X	X	L	DISABLED
L	L	L	L	L	L	THROUGH, WRITE "L"
L	L	H	L	L	L	THROUGH, WRITE "H"
L	H	X	L	L	DO	THROUGH, READ
L	L	L	H	X	L	LATCHED, WRITE "L"
L	L	H	H	X	L	LATCHED, WRITE "H"
L	H	X	H	L	DO^{-I}	LATCHED, READ
L	H	X	X	H	DO^{-O}	LATCHED, READ

L : Low Voltage Level
H : High Voltage Level
X : Don't care
DO^{-I} : Data Out at the Location Addressed Before $\overline{CLKA}$ Goes From "L" to "H"
DO^{-O} : Data Out at the Location Addressed Before $\overline{CLKO}$ Goes From "L" to "H"

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

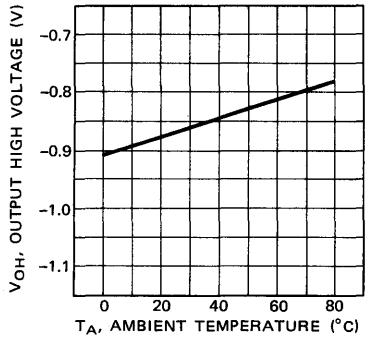


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

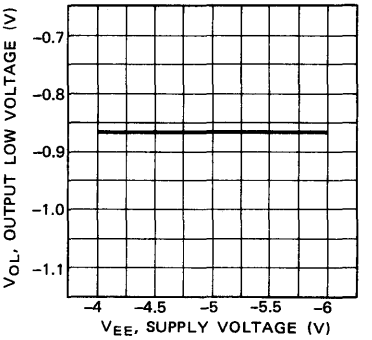


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

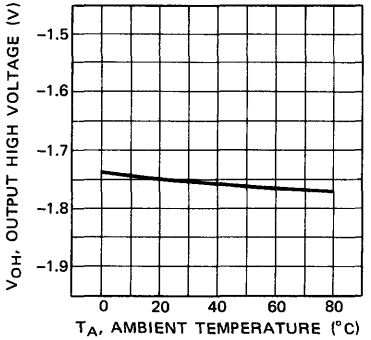


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

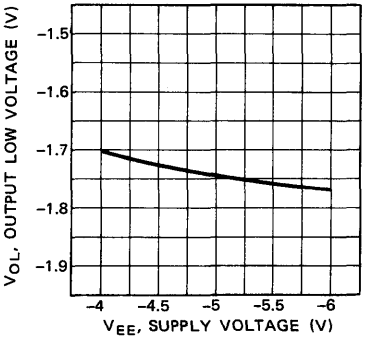


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

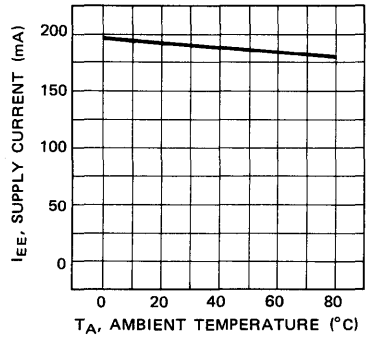
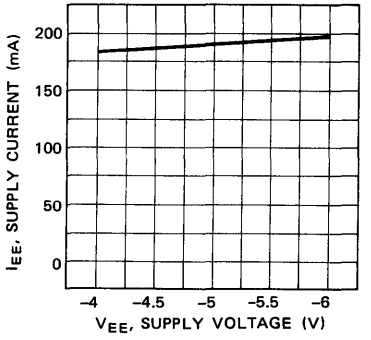


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE



3

Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

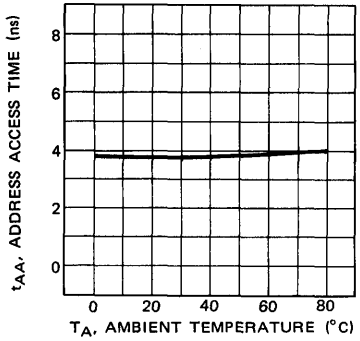


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

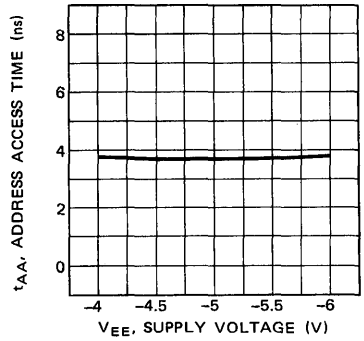


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

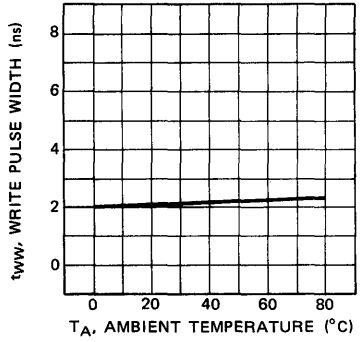
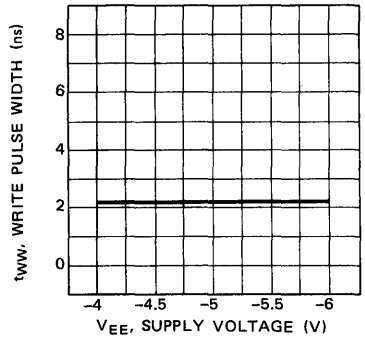


Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

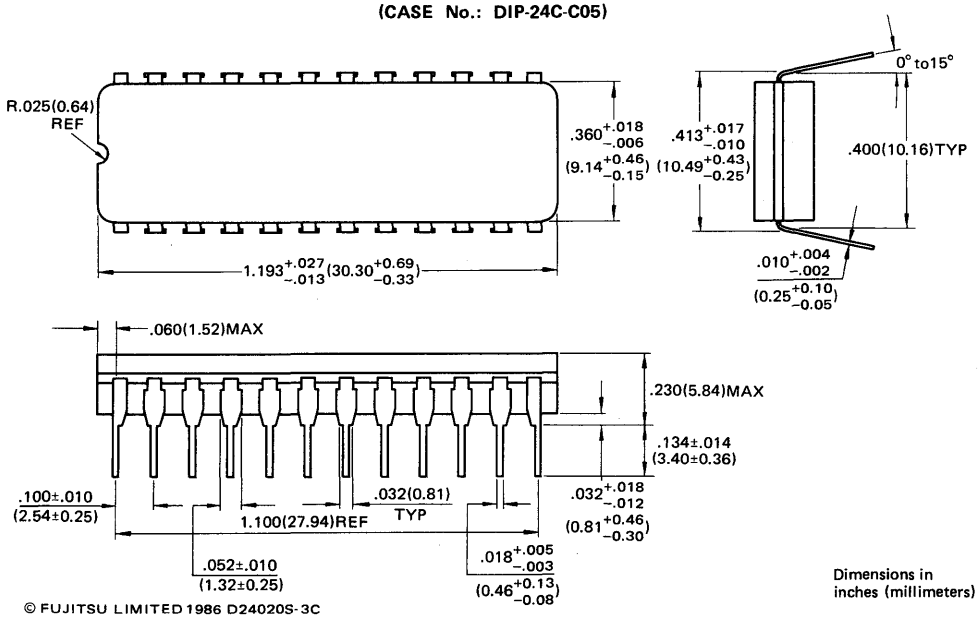


3

PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)

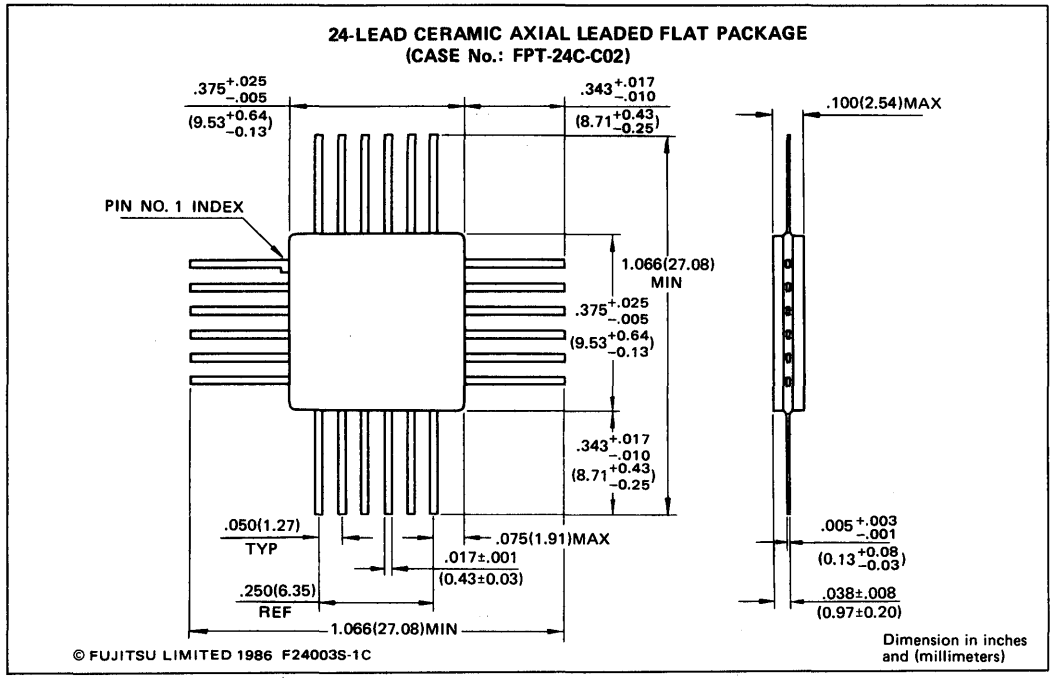


Dimensions in
inches (millimeters)

3

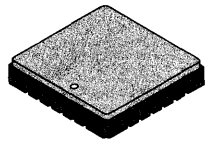
PACKAGE DIMENSIONS

CERAMIC FPT (: -ZF)



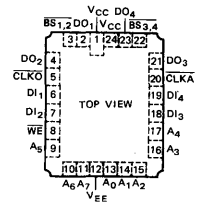
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

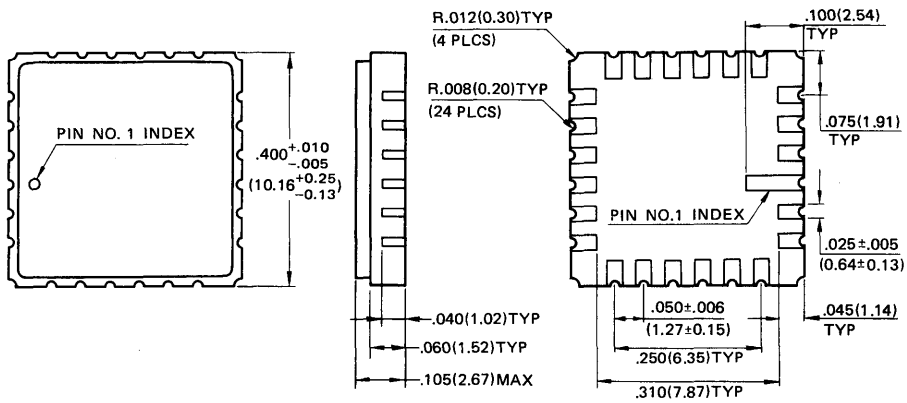


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

3

FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM100423LL-6

October 1987
Edition 2.0

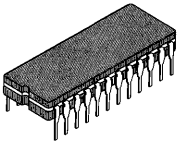
1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 100423LL is fully decoded 1024-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4 bits with address input and output latches. Generally in the system, preceeding logic IC is needed for the synchronous entry of asynchronous address signal inputs of the RAM. MBM 100423LL contains internal latch circuits so that it can take synchronous address input and output timing, which contribute to higher system performance and save of power dissipation and board area. And it features on-chip voltage/temperature compensation for improved noise margin.

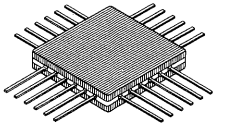
The MBM 100423LL offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 100423LL is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin Ceramic DIP, Flat Package, or LCC and is fully compatible with industry standard 100K-series ECL families.

- 256 words x 4 bits organization
- Address input and output latches which can be controlled separately
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry standard 100K-series ECL families
- Latch cycle time: 6 ns max.
- Address access time: 5 ns max.
- Block select access time: 3 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.73 mW/bit
- DOPOS and IOP-II



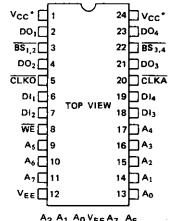
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: **See Page 11**

PIN ASSIGNMENT



LCC PAD CONFIGURATION: **See Page 11**

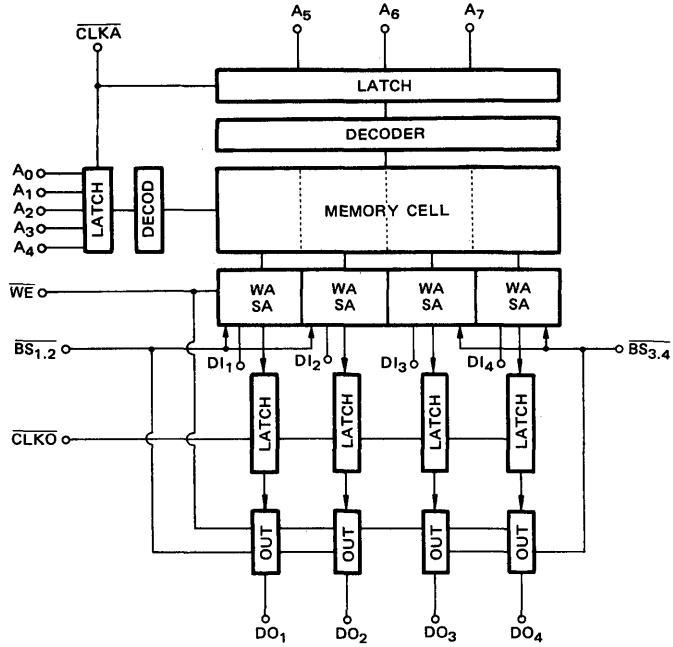
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MBM 100423LL BLOCK DIAGRAM



Symbol	Pin Name	Symbol	Pin Name
$A_0 \sim A_7$	Address Input	$\overline{CLKA}$	Address Latch Clock
$DI_1 \sim DI_4$	Data Input	$\overline{CLKO}$	Output Latch Clock
$DO_1 \sim DO_4$	Data Output	V_{EE}	Power Supply (–5.2V)
$\overline{WE}$	Write Enable	V_{CC}	Power Supply (0V)
$\overline{BS_{1.2}}, \overline{BS_{3.4}}$	Block Select		

FUNCTIONAL DESCRIPTION

The Fujitsu MBM100423LL is fully decoded 1024 bit read/write random access memory organized as 256 words by 4 bits with address input and output latches which can be controlled separately by $\overline{CLKA}$ and $\overline{CLKO}$ pins. When clock is in high state, data is latched, while clock is held low, data goes through the latches like as conventional MBM100422A. Memory cell selection is achieved by means of a 8-bit address designated A_0 through A_7. The active low Block Select inputs are provided for memory expansion. Two separate blocks are selected simultaneously by $\overline{BS_{1.2}}$ or $\overline{BS_{3.4}}$ pin. The read and write operation are controlled by the state of active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$, $\overline{BS_{1.2}}$ and/or $\overline{BS_{3.4}}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{BS_{1.2}}$ and/or $\overline{BS_{3.4}}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V, T_A = 0°C to 85°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 85°C for flat package and LCC, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA
$\overline{BS}$ and $\overline{CLKA}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	-220			mA

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		6	7	pF

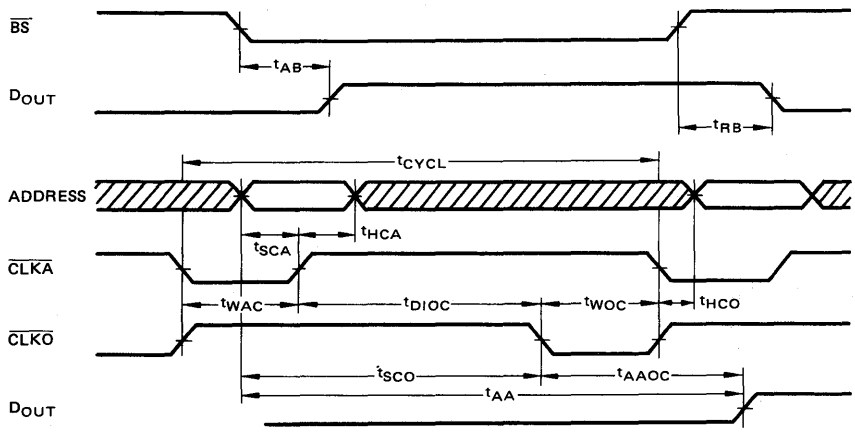
AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = –4.5V ± 5%, Output Load = 50Ω to –2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≥ 2.5m/s, T_C = 0°C to 85°C for Flatpackage and LCC, unless otherwise noted.)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	1.5		5.0	ns
Output Latch Access Time	t_{AAOC}	0.5		3.0	ns
Block Select Access Time	t_{AB}	0.5		3.0	ns
Block Select Recovery Time	t_{RB}	0.5		3.0	ns
Address Latch Clock Pulse Width	t_{WAC}	2.5			ns
Output Latch Clock Pulse Width	t_{WOC}	2.5			ns
Address Latch Clock Setup Time	t_{SCA}	1.5			ns
Address Latch Clock Hold Time	t_{HCA}	2.0			ns
Output Latch Clock Setup Time	t_{SCO}	2.5			ns
Output Latch Clock Hold Time	t_{HCO}	1.0			ns
Delay Time Between Input Clock and Output Clock	t_{DIOC}	1.0			ns
Latch Cycle Time	t_{CYCL}	6.0			ns

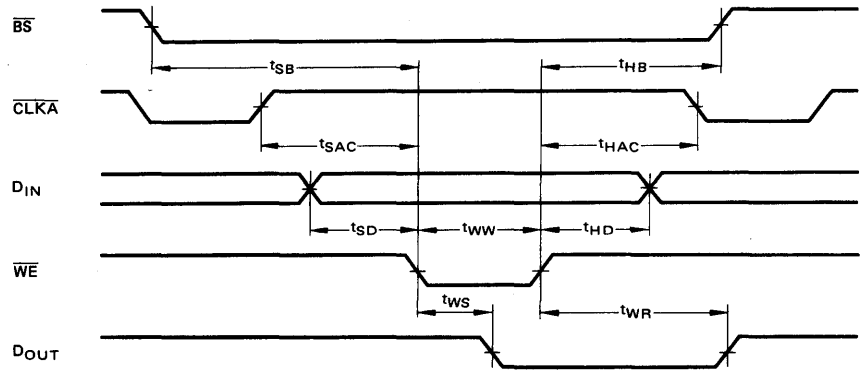
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	3.5			ns
Write Disable Time	t_{WS}	0.5		3.5	ns
Write Recovery Time	t_{WR}	0.5		3.5	ns
Write Clock Setup Time	t_{SAC}	−1.5			ns
Block Select Setup Time	t_{SB}	0.5			ns
Data Setup Time	t_{SD}	0.5			ns
Write Clock Hold Time	t_{HAC}	1.5			ns
Block Select Hold Time	t_{HB}	1.0			ns
Data Hold Time	t_{HD}	1.0			ns

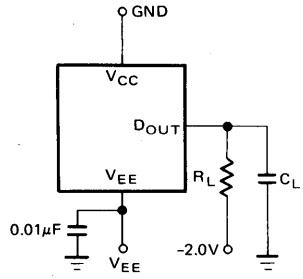
WRITE CYCLE TIMING DIAGRAM

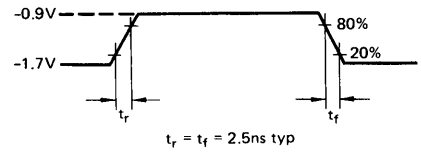


RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

Fig. 2 – AC TEST CONDITIONS





Output Load: R_L = 50Ω
C_L = 30pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

3

FUNCTIONAL TRUTH TABLE

$\overline{BS}$	$\overline{WE}$	DI	$\overline{CLKA}$	$\overline{CLKO}$	OUTPUT	MODE
H	X	X	X	X	L	DISABLED
L	L	L	L	L	L	THROUGH, WRITE "L"
L	L	H	L	L	L	THROUGH, WRITE "H"
L	H	X	L	L	DO	THROUGH, READ
L	L	L	H	X	L	LATCHED, WRITE "L"
L	L	H	H	X	L	LATCHED, WRITE "H"
L	H	X	H	L	DO^{-I}	LATCHED, READ
L	H	X	X	H	DO^{-O}	LATCHED, READ

L : Low Voltage Level
H : High Voltage Level
X : Don't care
DO^{-I} : Data Out at the Location Addressed Before $\overline{CLKA}$ Goes From "L" to "H"
DO^{-O} : Data Out at the Location Addressed Before $\overline{CLKO}$ Goes From "L" to "H"

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

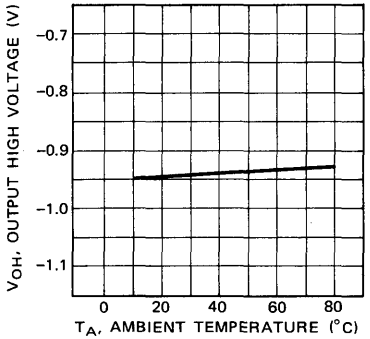


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

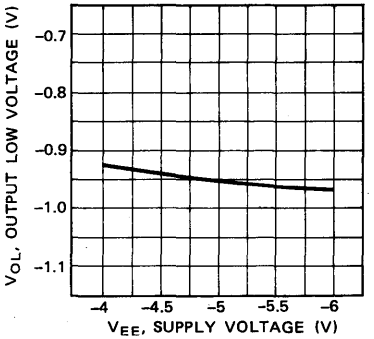


Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

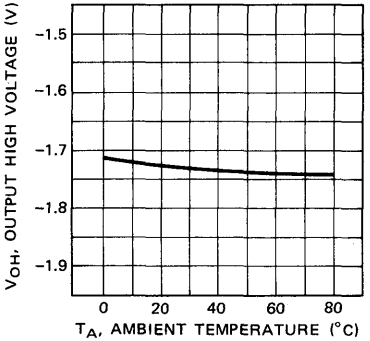


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

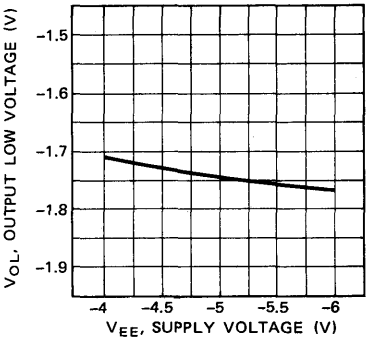


Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

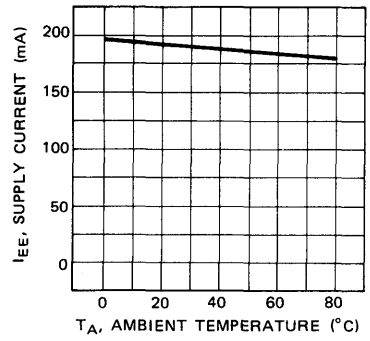
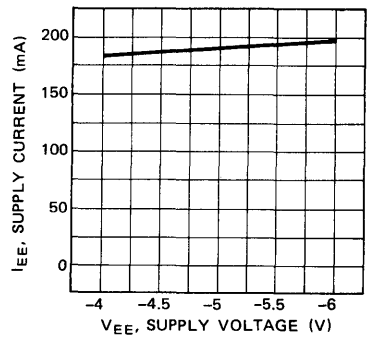


Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE



3

Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

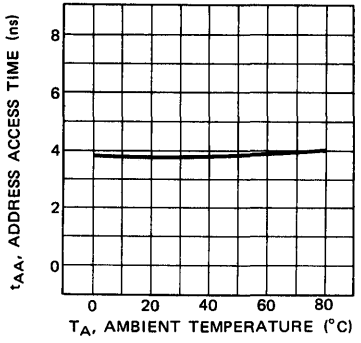


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

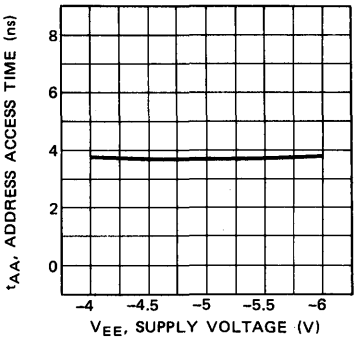


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

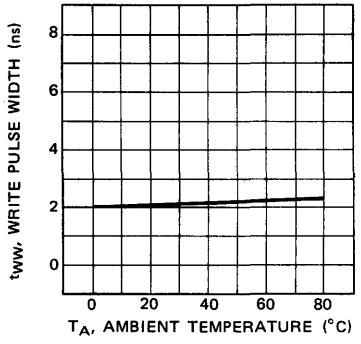
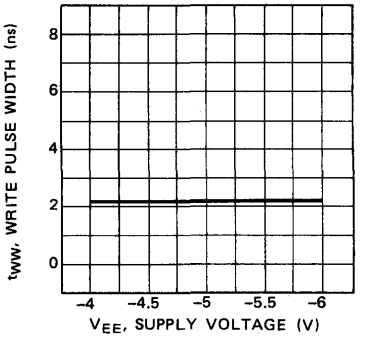


Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE

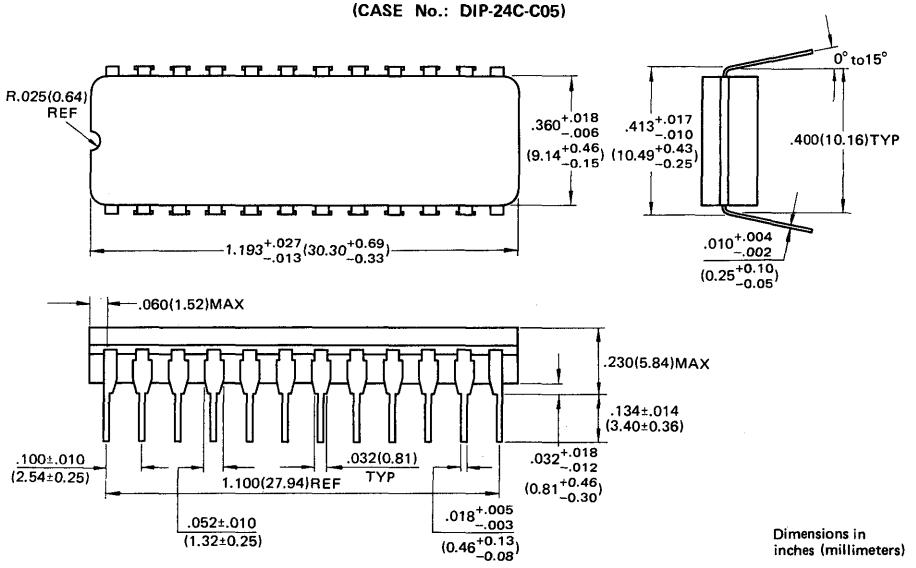


3

PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)

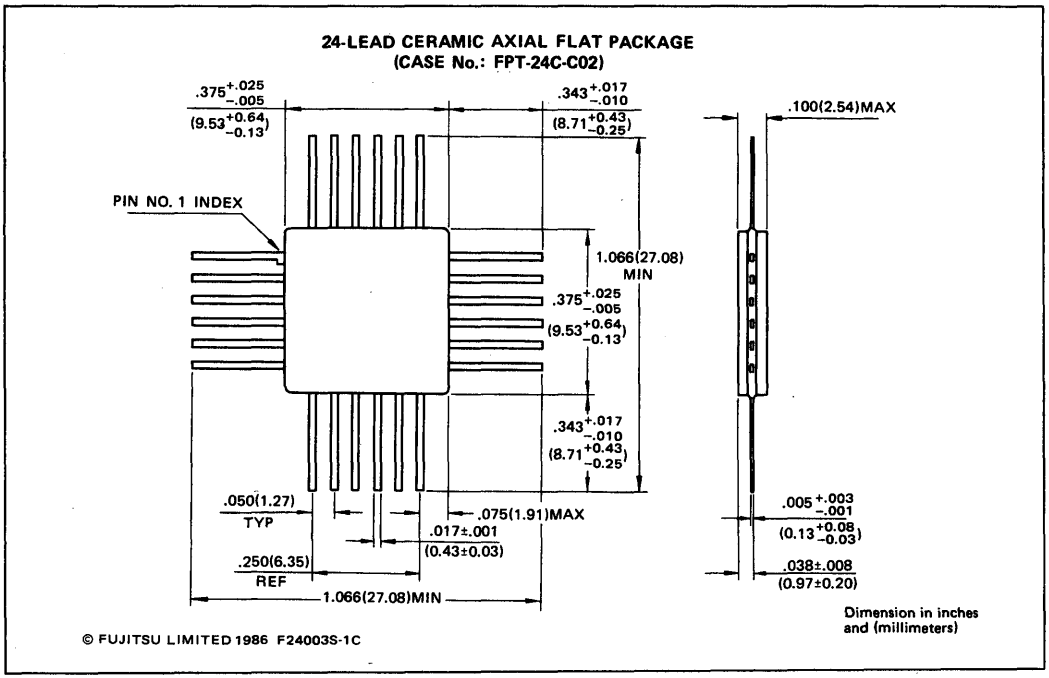


Dimensions in inches (millimeters)

3

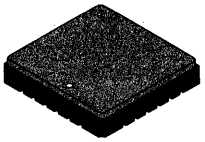
PACKAGE DIMENSIONS

CERAMIC FPT (: -ZF)



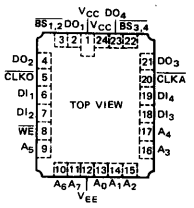
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

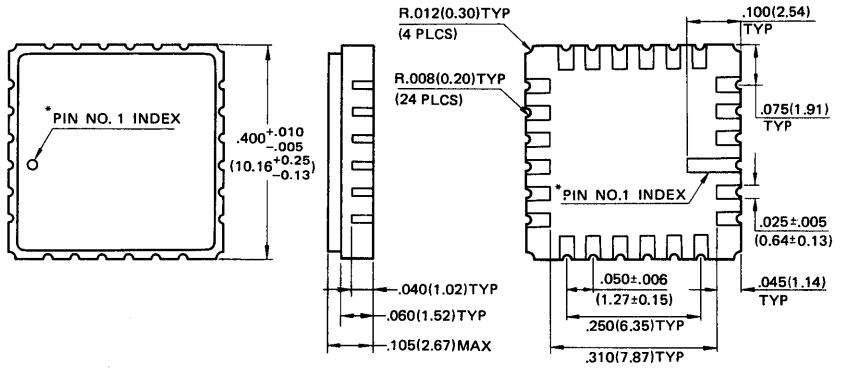


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

* Shape of PIN NO. 1 INDEX: Subject to change without notice.

3

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10476LL-9

4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

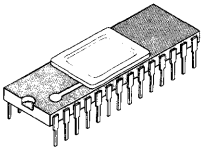
December, 1988
Edition 2.0

The Fujitsu MBM10476LL-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with latched inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded latch circuits allows to decrease the number of device on the board.

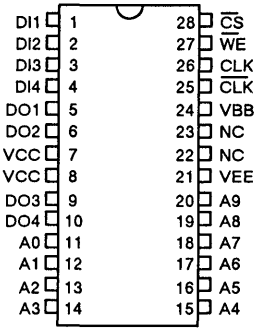
Operation for the MBM10476LL is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 9ns
  Address access time : 7ns
- Power dissipation : 1976mW max
- Open emitter output for ease of memory expansion
- D-type latches are used for input and output latches
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

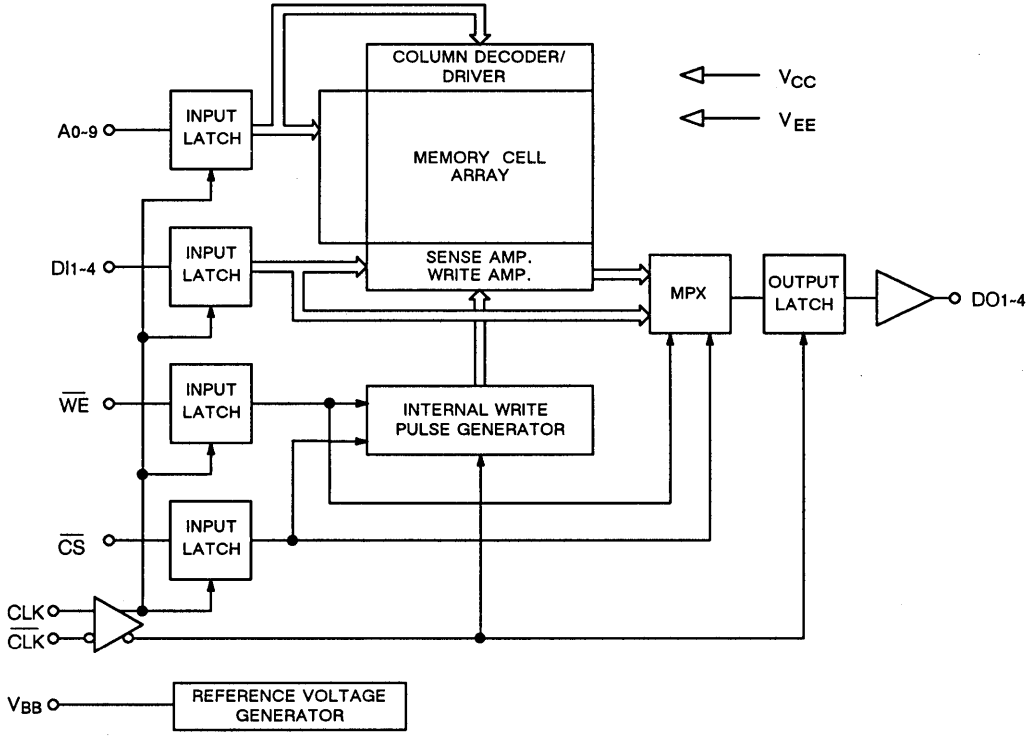
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	Tc	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM10476LL BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address inputs
DI1 thru DI4	Data inputs
DO1 thru DO4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
CLK, $\overline{CLK}$	Clock inputs
VBB	Reference voltage (-1.29V)
VEE	Supply voltage (-5.2V)
VCC	Supply voltage (0V)
NC	No connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -5.2V, Output Load = 50Ω to -2.0V, T_C = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL}min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-380			mA	0°C to 75°C
Reference Voltage	V_{BB}	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10476LL is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are level sensitive transparent latches controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input latches are transparent when CLK ($\overline{CLK}$) goes low (high), and close to hold the data when CLK($\overline{CLK}$) goes high (low) and on the other hand, output latches are transparent when CLK ($\overline{CLK}$) goes high (low) and data are held in the output latches when CLK ($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may fluctuate during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes high (low), inputs are latched, while previous read data goes through the output latches and appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), input latches are transparent, while output latches are closed and hold the data from the previous cycle.

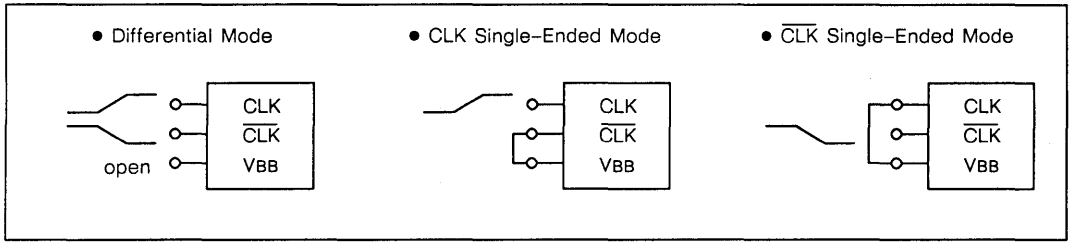
When setup time is wide enough, output data becomes valid in the short delay time (tDR) after the rising (falling) edge of CLK ($\overline{CLK}$). When setup time is short, output data appears on the outputs after the specified RAM access time (tA(ADD)) similar to the traditional RAM.

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and Address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully sef-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



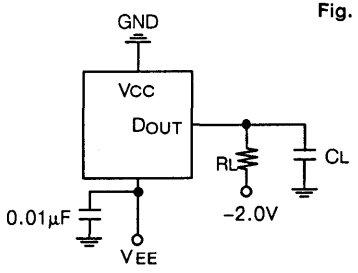
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

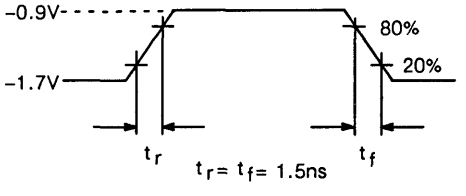
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	6.0			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0			ns
Cycle Time	t_{CYC}	9.0			ns
Address Access Time	$t_{A(ADD)}$			7.0 *1	ns
Data Access Time	$t_{A(DI)}$			4.0 *2	ns
Write Access Time	$t_{A(W)}$			4.0 *3	ns
Chip Select Access Time	$t_{A(CS)}$			4.0 *4	ns
Clock Access Time	$t_{A(CLK)}$			8.0 *5	ns
Output Delay Time	t_{DR}			3.0 *6	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at t_{SA} = 1.0ns
*2 Specified at t_{SD} = 1.0ns
*3 Specified at t_{SW} = 1.0ns
*4 Specified at t_{SC} = 1.0ns
*5 Specified at $t_{WL(CLK)}$ = 3.0ns
*6 Specified when $t_{WL(CLK)} > t_{A(CLK)\ max}$, $t_{SA} > t_{A(ADD)\ max}$, $t_{SC} > t_{A(CS)\ max}$, $t_{SD} > t_{A(DI)\ max}$, $t_{SW} > t_{A(W)\ max}$.

Fig. 2 - AC TEST CONDITIONS



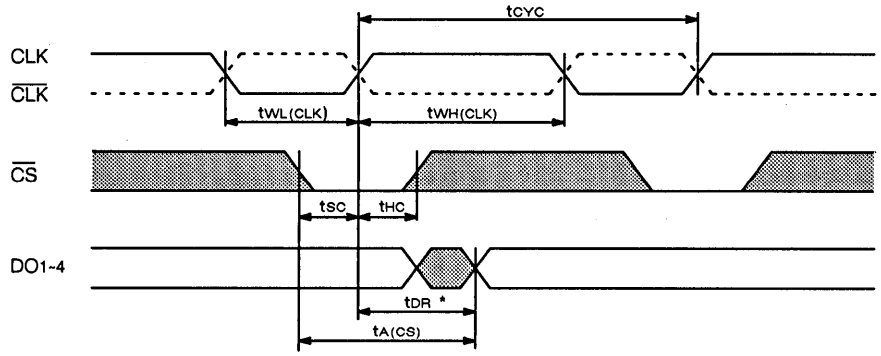
Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



Note : All timing measurements referenced to 50% input levels.

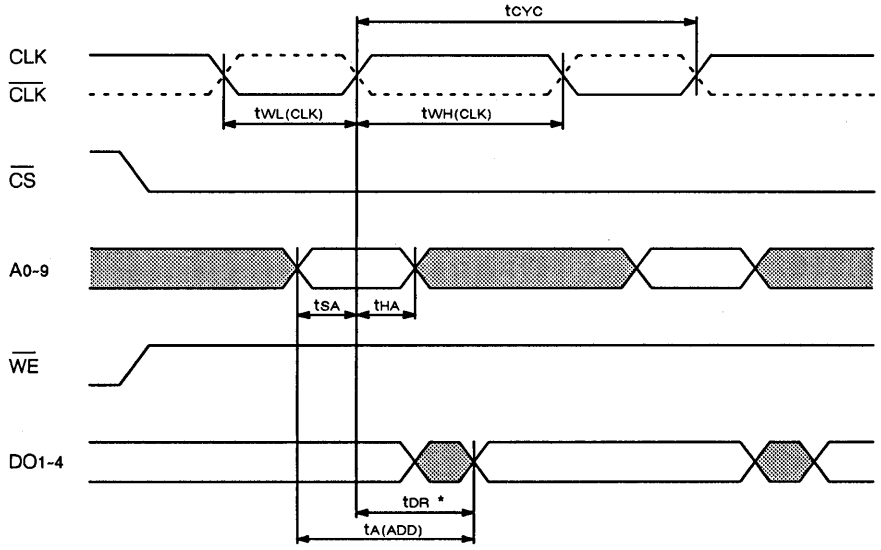
READ CYCLE TIMING DIAGRAMS

• CHIP SELECT ACCESS MODE



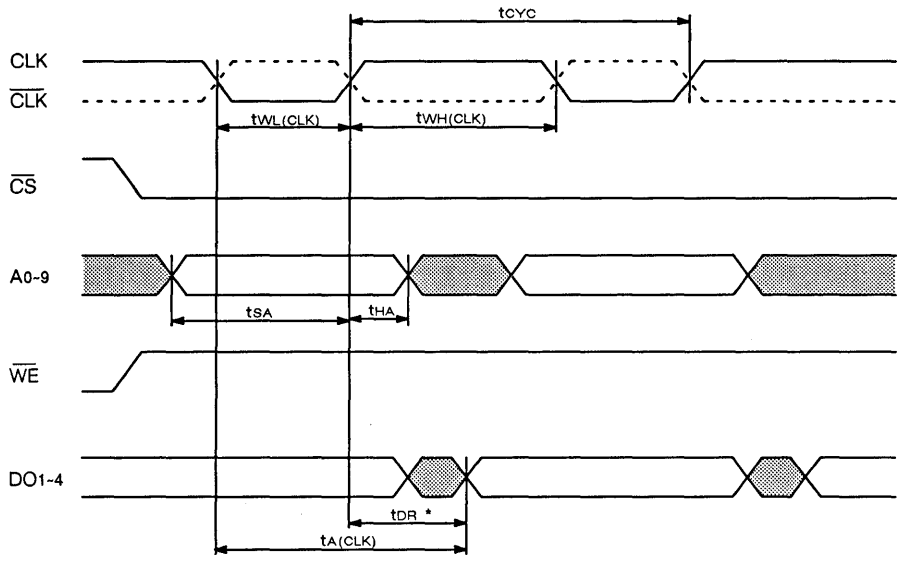
* Output is valid at tDR when tSC > tA(CS) max – tDR max.

• ADDRESS ACCESS MODE



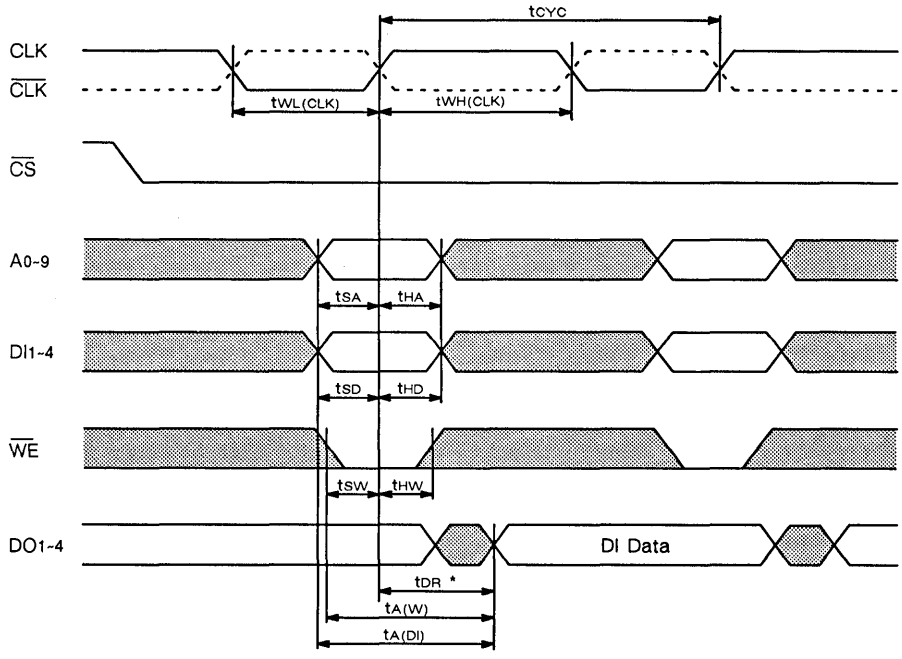
* Output is valid at tDR when tSA > tA(ADD) max – tDR max.

• CLOCK ACCESS MODE



* Output is valid at tDR when tWL(CLK) > tA(CLK) max – tDR max.

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at t_{DR} when $t_{SW} > t_{A(W)\ max} - t_{DR\ max}$ and $t_{SD} > t_{A(DI)\ max} - t_{DR\ max}$

Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

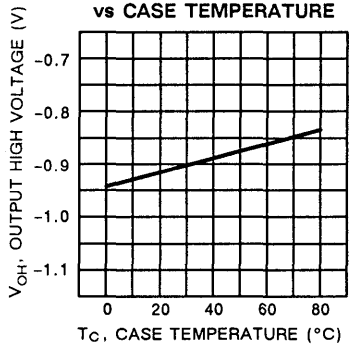


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

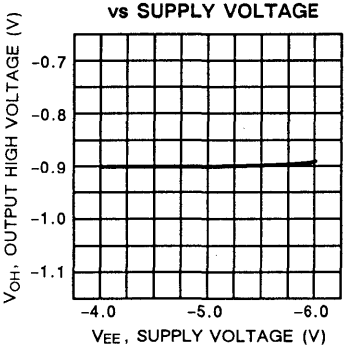


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

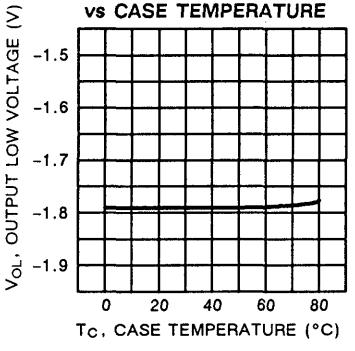


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

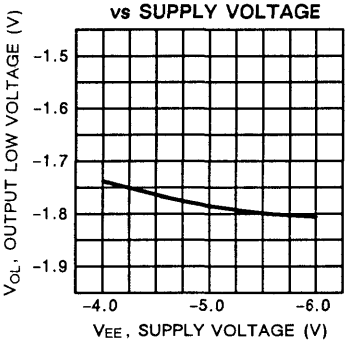


Fig. 7 – REFERENCE VOLTAGE vs CASE TEMPERATURE

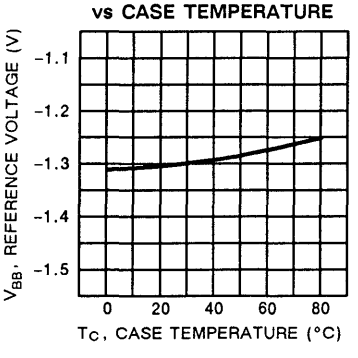
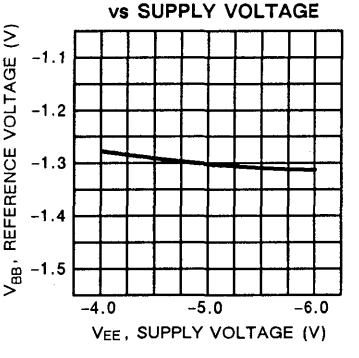


Fig. 8 – REFERENCE VOLTAGE vs SUPPLY VOLTAGE



3

3

Fig. 9 – SUPPLY CURRENT vs CASE TEMPERATURE

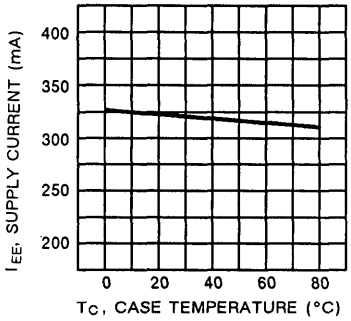


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

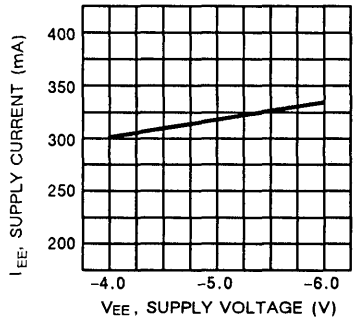


Fig. 11 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

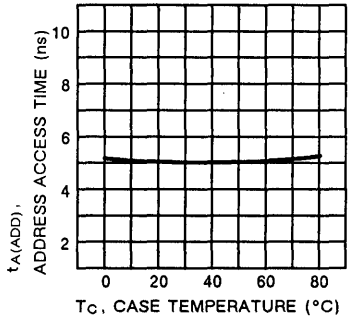


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

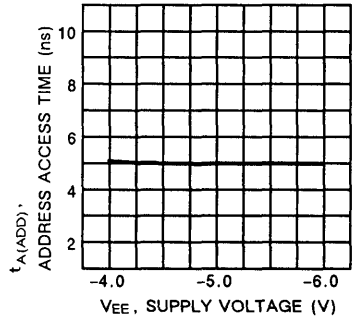


Fig. 13 – CLOCK ACCESS TIME vs CASE TEMPERATURE

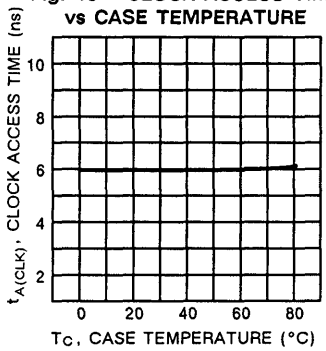


Fig. 14 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

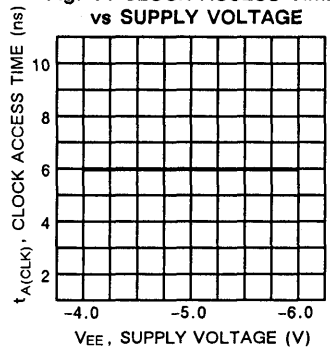


Fig. 15 – OUTPUT DELAY TIME vs CASE TEMPERATURE

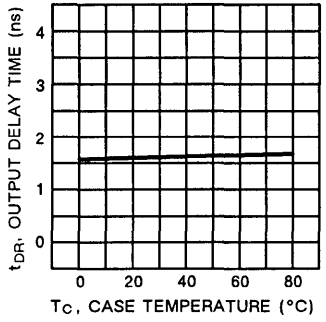


Fig. 16 – OUTPUT DELAY TIME vs SUPPLY VOLTAGE

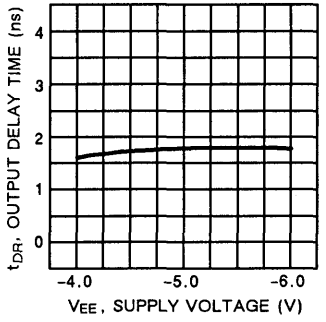


Fig. 17 – CLOCK PULSE WIDTH HIGH vs CASE TEMPERATURE

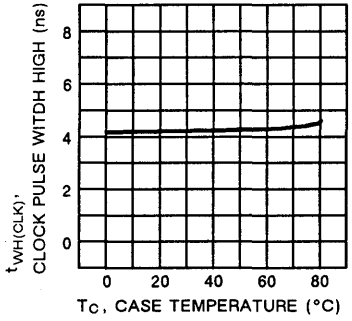
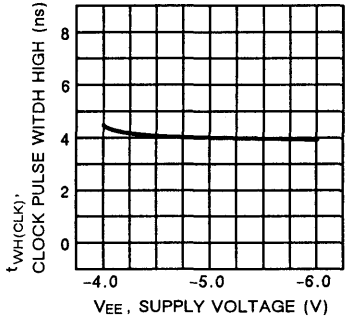


Fig. 18 – CLOCK PULSE WIDTH HIGH vs SUPPLY VOLTAGE



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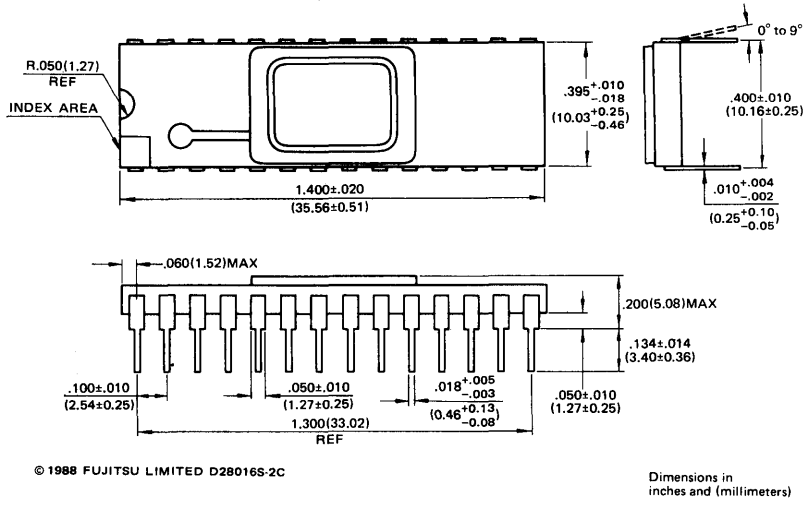
PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

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FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10476RR-9

December, 1988
Edition 1.0

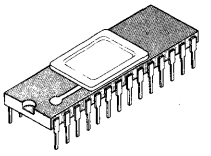
4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

The Fujitsu MBM10476RR-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with registered inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register circuits allows to decrease the number of device on the board.

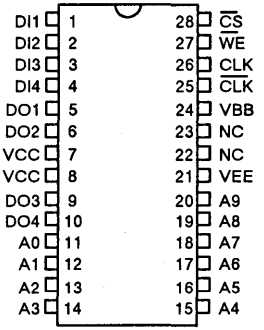
Operation for the MBM10476RR is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 9ns
  Output delay time : 3ns
- Power dissipation : 2080mW max
- Open emitter output for ease of memory expansion
- Edge triggered registers for inputs and outputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

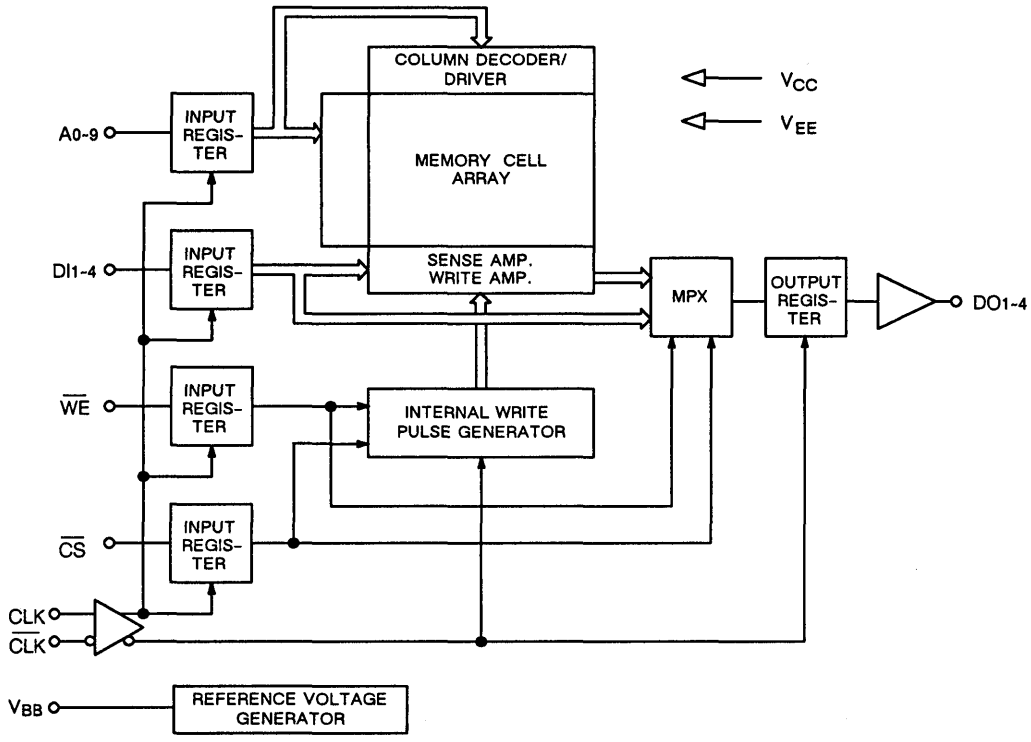
Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig.1 - MBM10476RR-9 BLOCK DIAGRAM



FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.29V)
VEE	Supply Voltage (-5.2V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TC
Output High Voltage (VIN = VIH max or VIL min)	VOH	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH max or VIL min)	VOL	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (VIN = VIH min or VIL max)	VOHC	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (VIN = VIH min or VIL max)	VOLC			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	VIH	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	VIL	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (VIN = VIH max)	IIH			220	µA	0°C to 75°C
Input Low Current (VIN = VIL min)	IIL	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (VIN = VIL min)	IIL	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	IEE	-400			mA	0°C to 75°C
Reference Voltage	VBB	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10476RR is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are edge triggered registered controlled by the clock input (CLK/$\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input and output registers are transparent when CLK ($\overline{CLK}$) goes high (low), and close to hold the data when CLK($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may not be stable during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes low (high), address data is held at output, while output data is kept valid during the same cycle. Thus, the output data becomes available at the next rising (falling) edge of CLK ($\overline{CLK}$).

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), inputs are transparent while previous read data appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the output by the CLK($\overline{CLK}$) rising (falling) edge of the next cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

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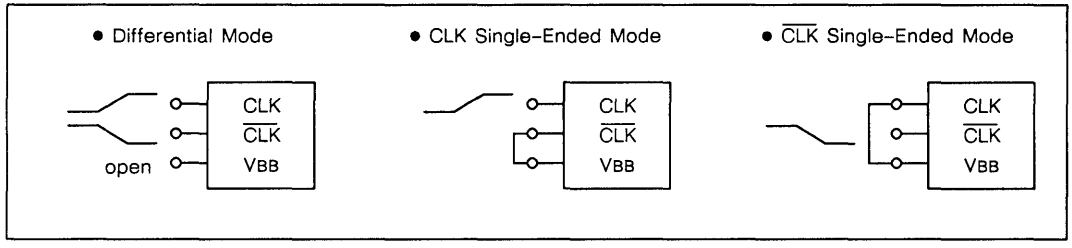
CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



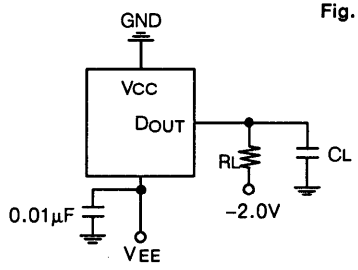
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

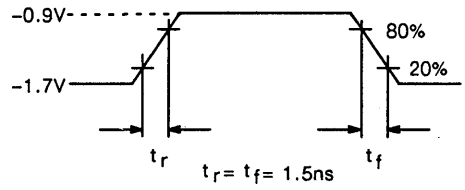
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	3.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0 *2			ns
Cycle Time	t_{CYC}	9.0			ns
Output Delay Time	t_{DR}			3.0	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) > 6.0ns
*2 Specified at tWH(CLK) > 6.0ns

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

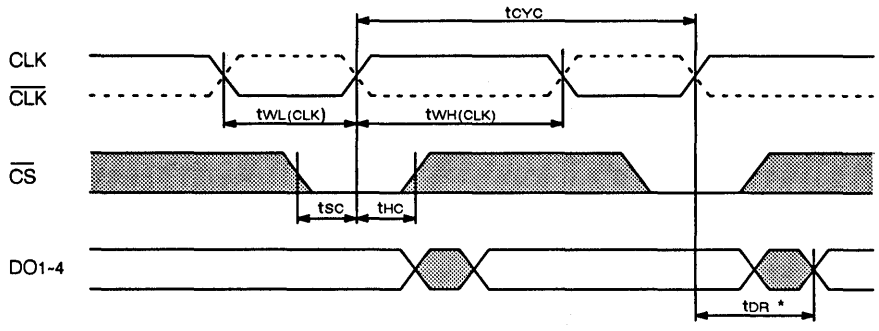


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

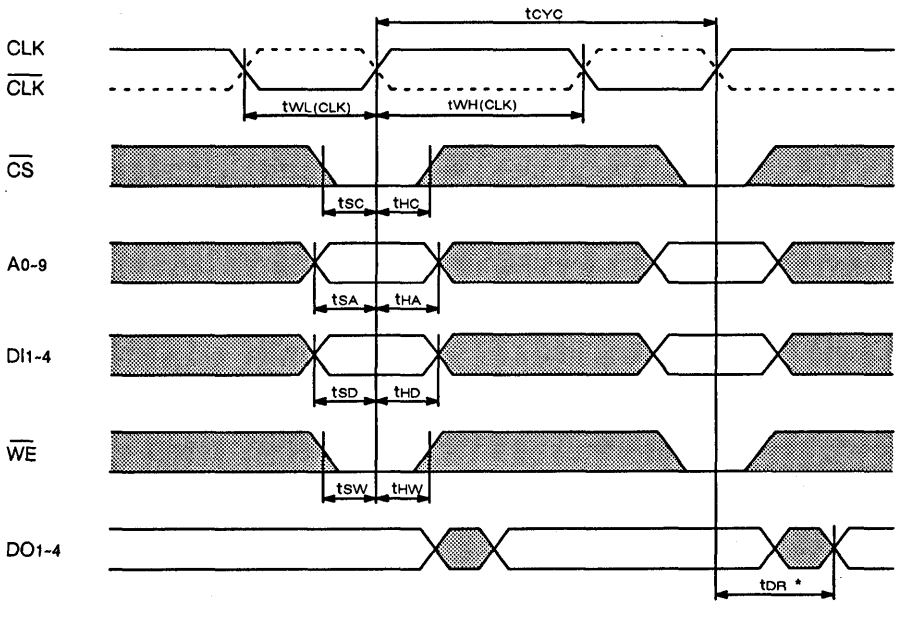
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

READ CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

WRTE CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 - OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

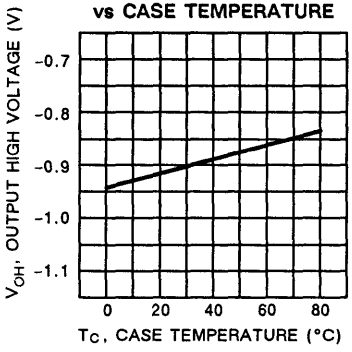


Fig. 4 - OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

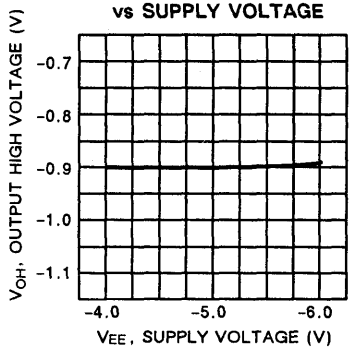


Fig. 5 - OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

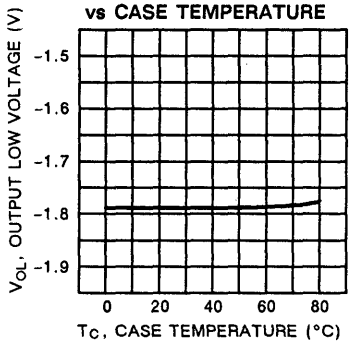


Fig. 6 - OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

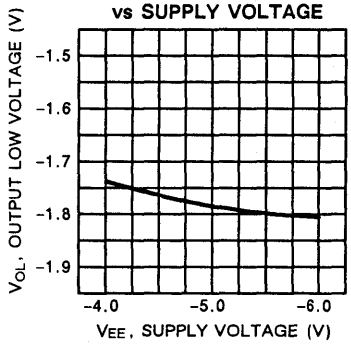


Fig. 7 - REFERENCE VOLTAGE vs CASE TEMPERATURE

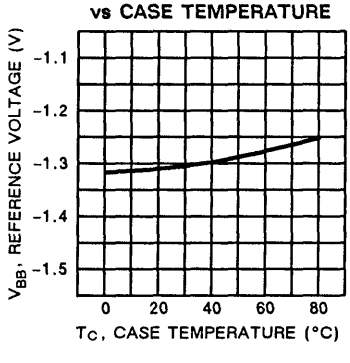


Fig. 8 - REFERENCE VOLTAGE vs SUPPLY VOLTAGE

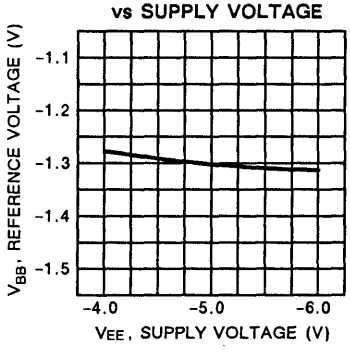


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Fig. 9 - SUPPLY CURRENT vs CASE TEMPERATURE

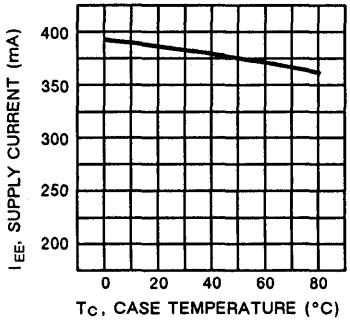


Fig. 10 - SUPPLY CURRENT vs SUPPLY VOLTAGE

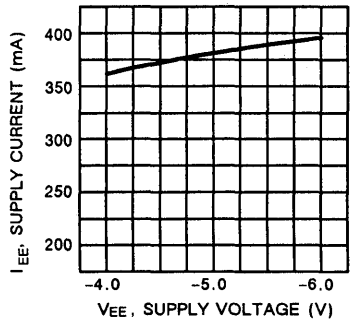


Fig. 11 - OUTPUT DELAY TIME vs CASE TEMPERATURE

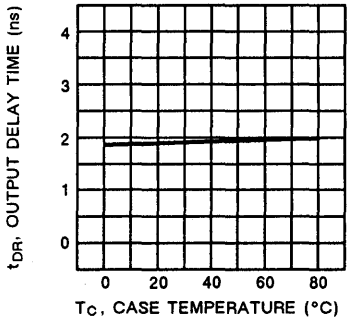
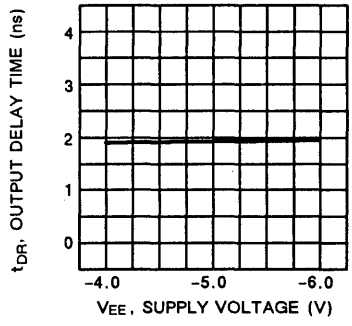
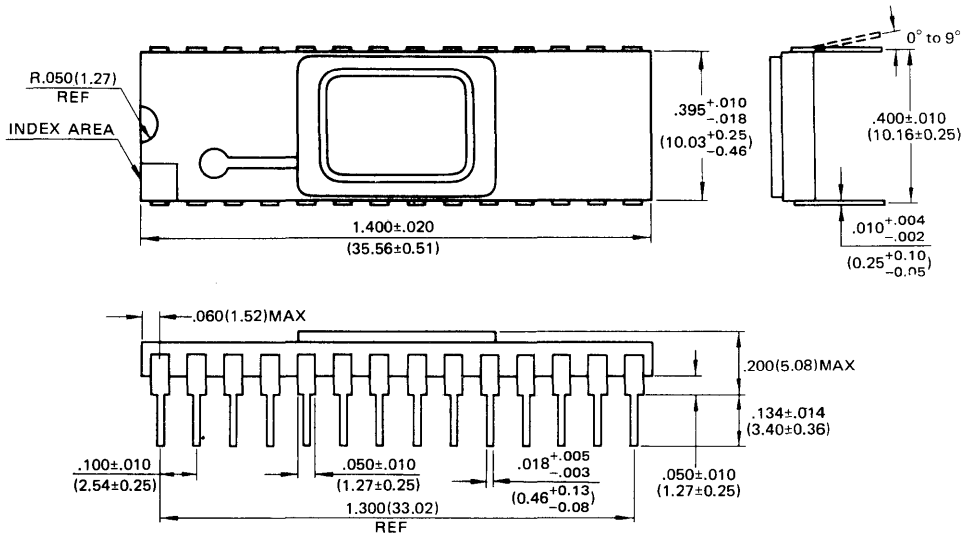


Fig. 12 - OUTPUT DELAY TIME vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10476RL-9

4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

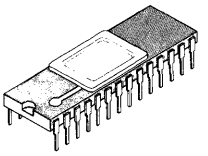
December, 1988
Edition 1.0

The Fujitsu MBM10476RL-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with registered inputs and latched outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register/latch circuits allows to decrease the number of device on the board.

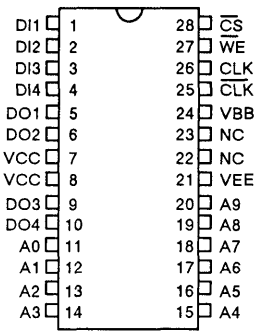
Operation for the MBM10476RL is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 9ns
  Output delay time : 3ns
- Power dissipation : 2080mW max
- Open emitter output for ease of memory expansion
- Level-sensitive D-type latch for outputs and edge triggered registers for inputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

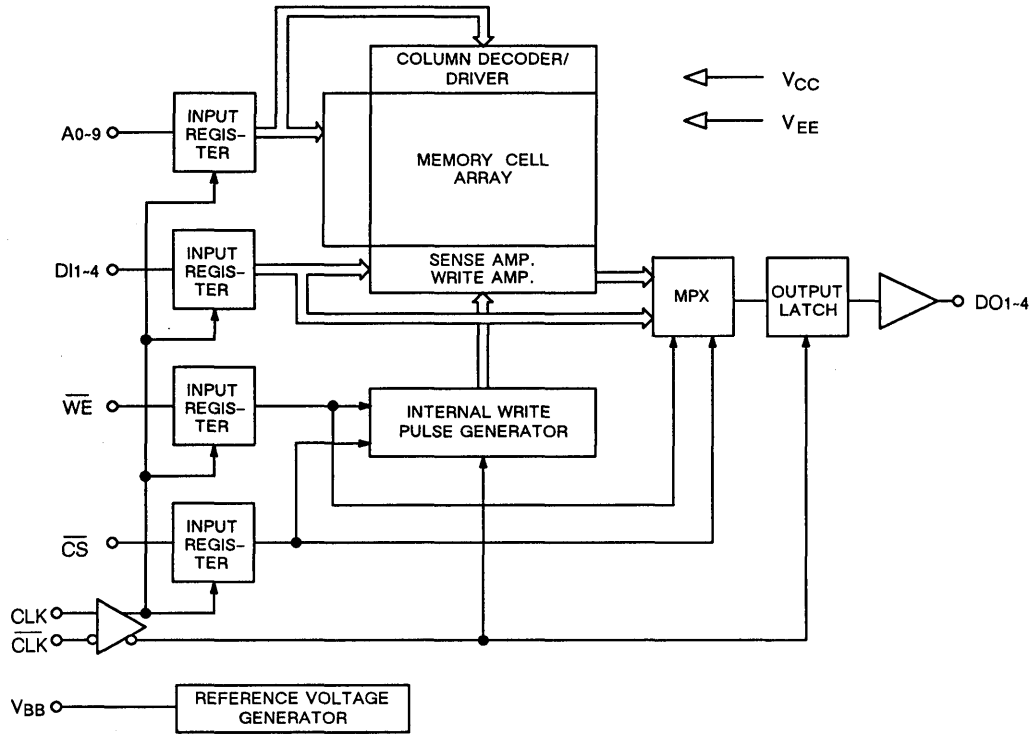
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM10476RL-9 BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.29V)
VEE	Supply Voltage (-5.2V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_C
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			mA	0°C to 75°C
Reference Voltage	V_{BB}	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10476RL is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) furnish edge triggered registers, whereas outputs (DOUT) have level sensitive transparent latches.

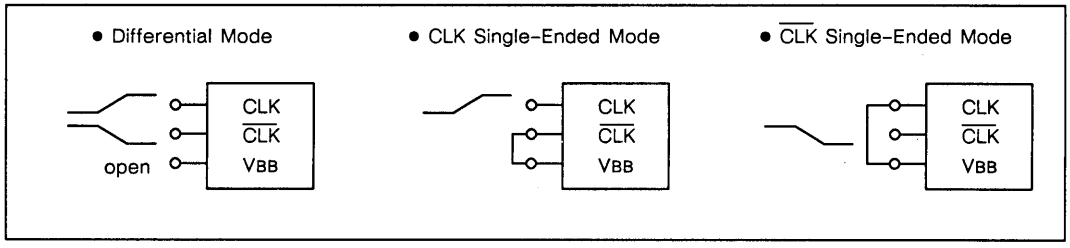
When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. All input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels are free to change for the rest of the cycle timeonce input data is held into the input register. Read out data becomes available during CLK low state in which output latches are transpatent. When CLK ($\overline{CLK}$) state is wide enough than the internal RAM access time, output data become valid in the short delay time (tDR) after the falling (rising)edge of CLK ($\overline{CLK}$).

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



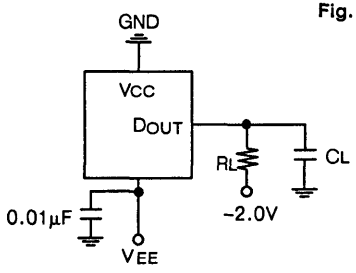
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

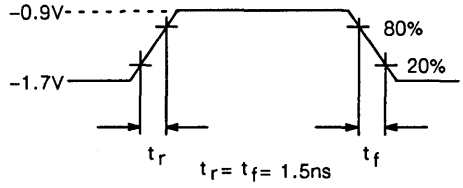
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	3.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0 *2			ns
Cycle Time	t_{CYC}	9.0			ns
Clock Access Time	$t_{A(CLK)}$			8.0 *3	ns
Output Delay Time	t_{DR}			3.0 *4	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) > 6.0ns
*2 Specified at tWH(CLK) > 6.0ns
*3 Specified at tWH(CLK) = 3.0ns
*4 Specified at tWH(CLK) > tA(CLK) max

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

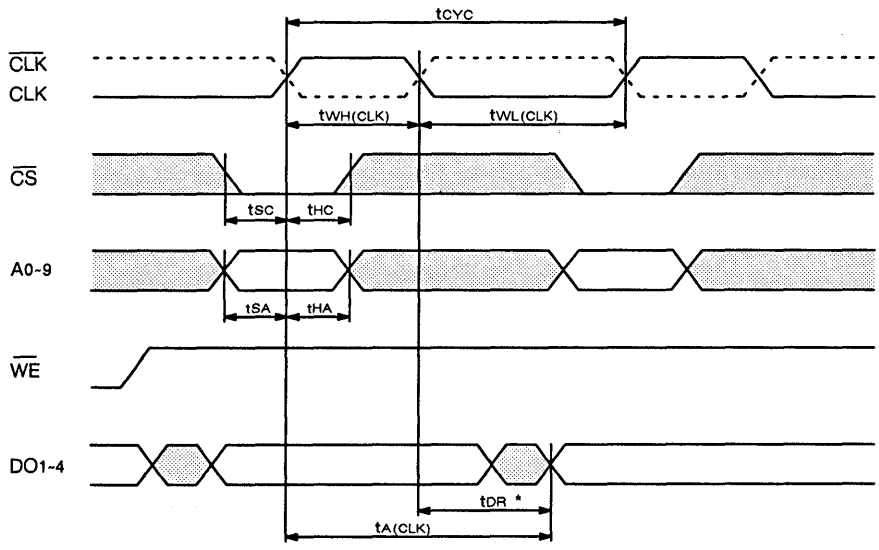


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

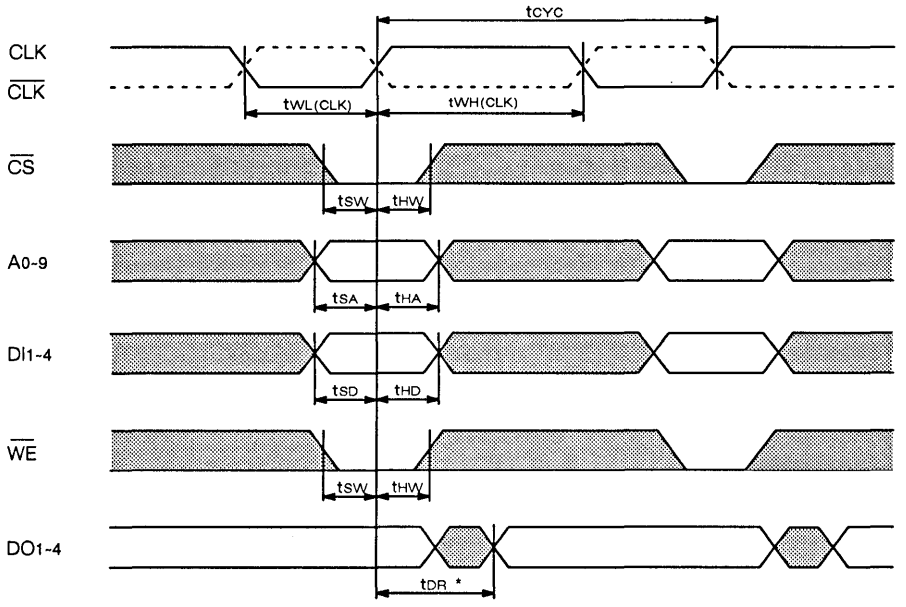
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

READ CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tWH(CLK) > tA(CLK) max − tDR max.

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tWH(CLK) > tA(CLK) max - tDR max.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 - OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

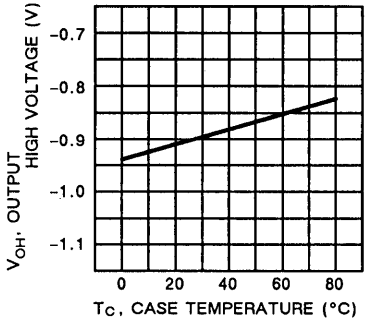


Fig. 4 - OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

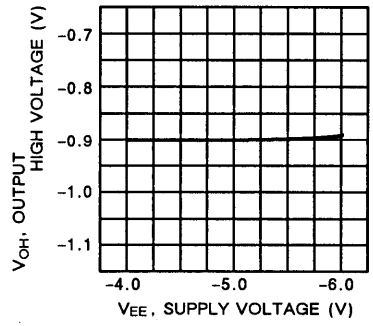


Fig. 5 - OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

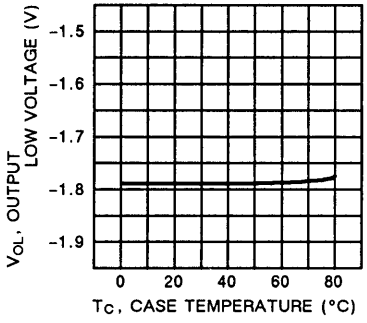


Fig. 6 - OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

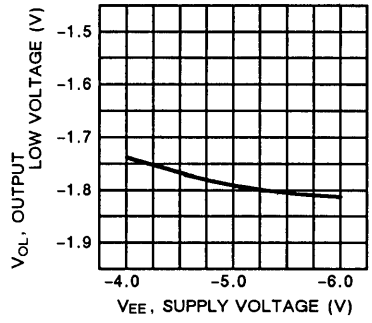


Fig. 7 - REFERENCE VOLTAGE vs CASE TEMPERATURE

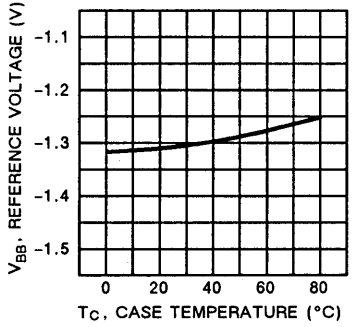


Fig. 8 - REFERENCE VOLTAGE vs SUPPLY VOLTAGE

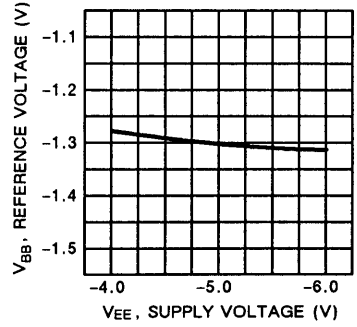


Fig. 9 - SUPPLY CURRENT vs CASE TEMPERATURE

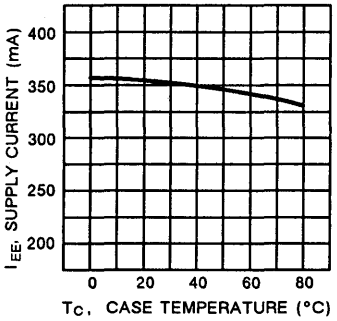


Fig. 10 - SUPPLY CURRENT vs SUPPLY VOLTAGE

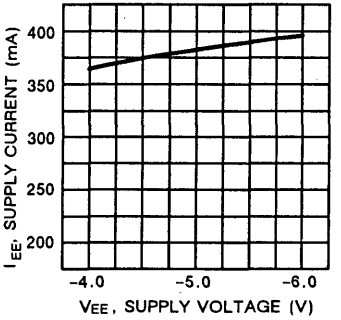


Fig. 11 - CLOCK ACCESS TIME vs CASE TEMPERATURE

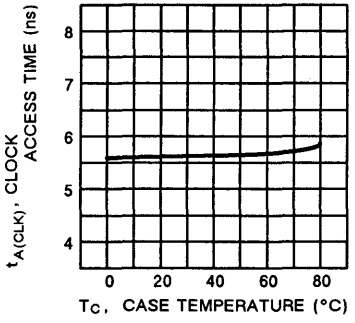


Fig. 12 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

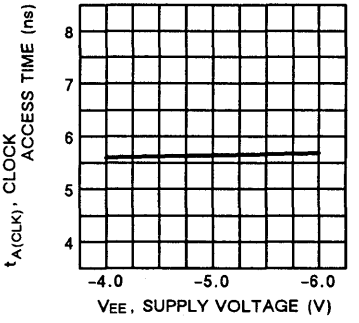


Fig. 13 - OUTPUT DELAY TIME vs CASE TEMPERATURE

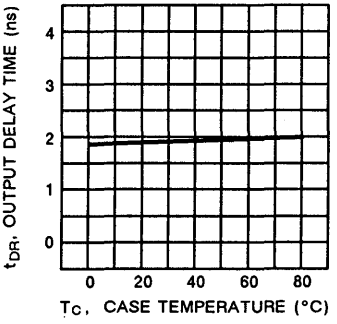
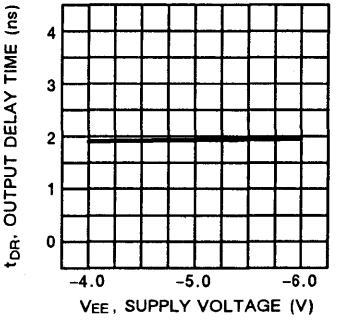


Fig. 14 - OUTPUT DELAY TIME vs SUPPLY VOLTAGE



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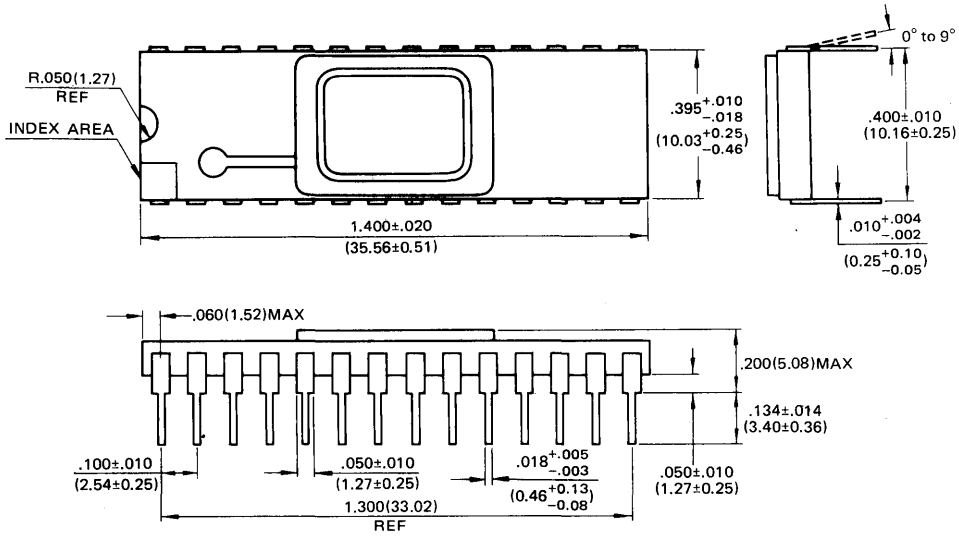
PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100476LL-9

December, 1988
Edition 2.0

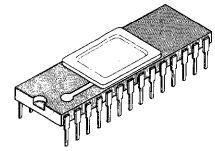
4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

The Fujitsu MBM100476LL-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with latched inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded latch circuits allows to decrease the number of device on the board.

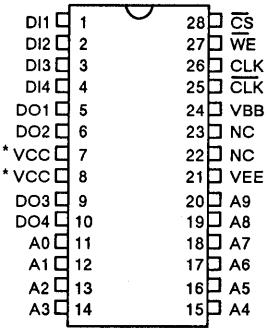
Operation for the MBM100476LL is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage/temperatuere compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 9ns
  Address access time : 7ns
- Power dissipation : 1710mW max
- Open emitter output for ease of memory expansion
- D-type latches are used for input and output latches
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

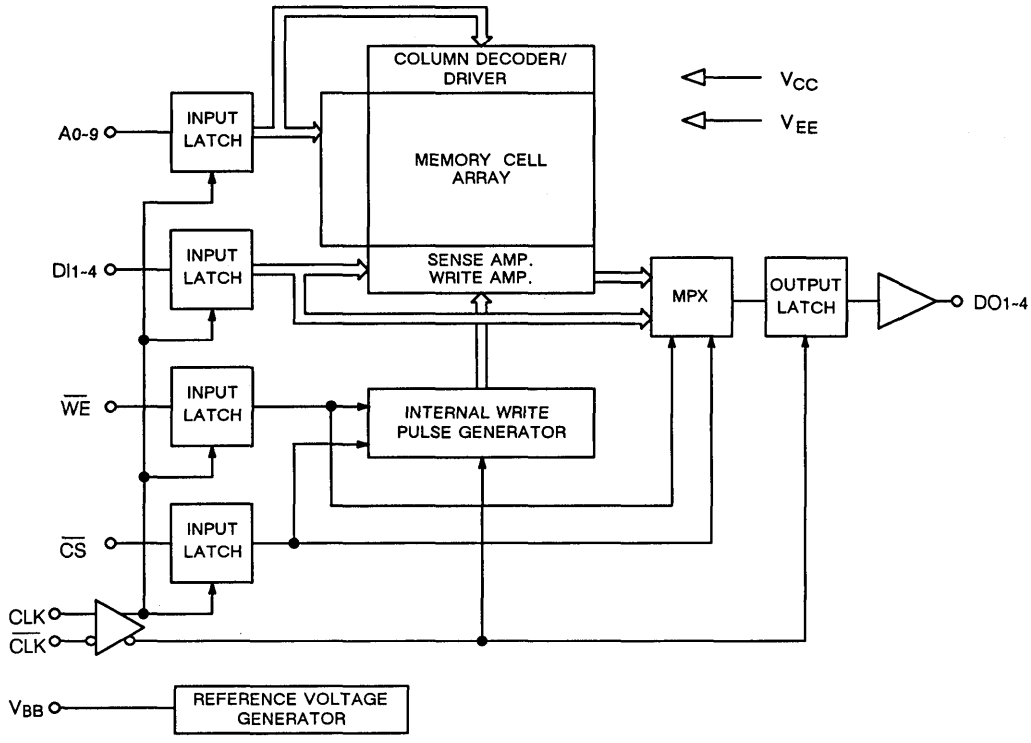
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM100476LL BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

 : Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
V_{BB}	Reference Voltage (-1.32V)
V_{EE}	Supply Voltage (-4.5V)
V_{CC}	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TC = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-380			mA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM100476LL is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are level sensitive transparent latches controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input latches are transparent when CLK ($\overline{CLK}$) goes low (high), and close to hold the data when CLK($\overline{CLK}$) goes high (low) and on the other hand, output latches are transparent when CLK ($\overline{CLK}$) goes high (low) and data are held in the output latches when CLK ($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may fluctuate during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes high (low), inputs are latched, while previous read data goes through the output latches and appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), input latches are transparent, while output latches are closed and hold the data from the previous cycle.

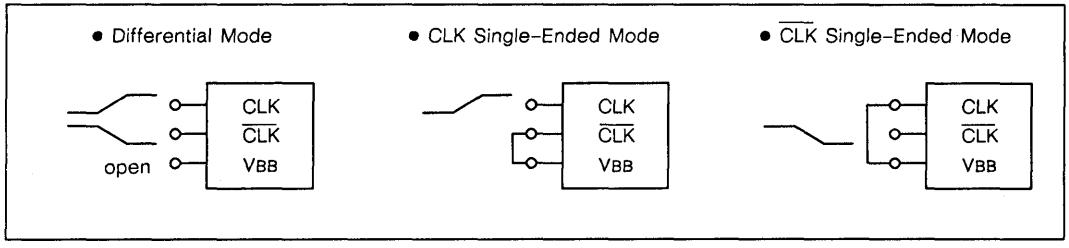
When setup time is wide enough, output data becomes valid in the short delay time (tDR) after the rising (falling) edge of CLK ($\overline{CLK}$). When setup time is short, output data appears on the outputs after the specified RAM access time (tA(ADD)) similar to the traditional RAM.

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and Address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully sef-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



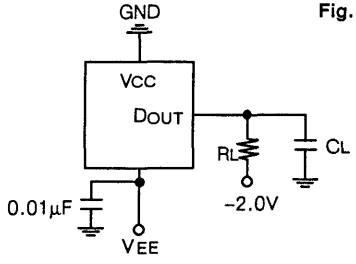
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

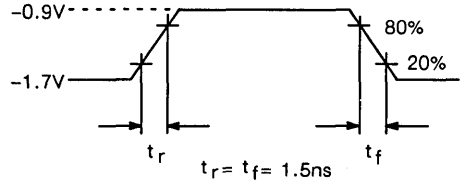
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	6.0			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0			ns
Cycle Time	t_{CYC}	9.0			ns
Address Access Time	$t_{A(ADD)}$			7.0 *1	ns
Data Access Time	$t_{A(DI)}$			4.0 *2	ns
Write Access Time	$t_{A(W)}$			4.0 *3	ns
Chip Select Access Time	$t_{A(CS)}$			4.0 *4	ns
Clock Access Time	$t_{A(CLK)}$			8.0 *5	ns
Output Delay Time	t_{DR}			3.0 *6	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at t_{SA} = 1.0ns
*2 Specified at t_{SD} = 1.0ns
*3 Specified at t_{SW} = 1.0ns
*4 Specified at t_{SC} = 1.0ns
*5 Specified at $t_{WL(CLK)}$ = 3.0ns
*6 Specified when $t_{WL(CLK)} > t_{A(CLK)}$ max, $t_{SA} > t_{A(ADD)}$ max, $t_{SC} > t_{A(CS)}$ max, $t_{SD} > t_{A(DI)}$ max, $t_{SW} > t_{A(W)}$ max.

Fig. 2 - AC TEST CONDITIONS



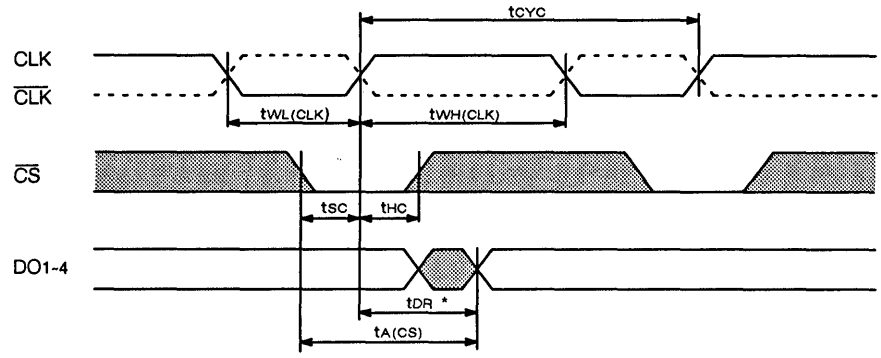
Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



Note : All timing measurements referenced to 50% input levels.

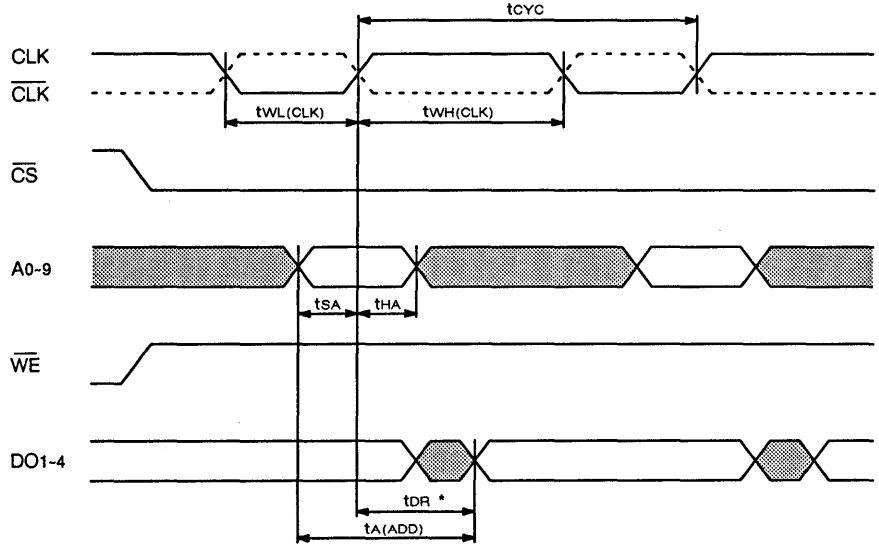
READ CYCLE TIMING DIAGRAMS

• CHIP SELECT ACCESS MODE



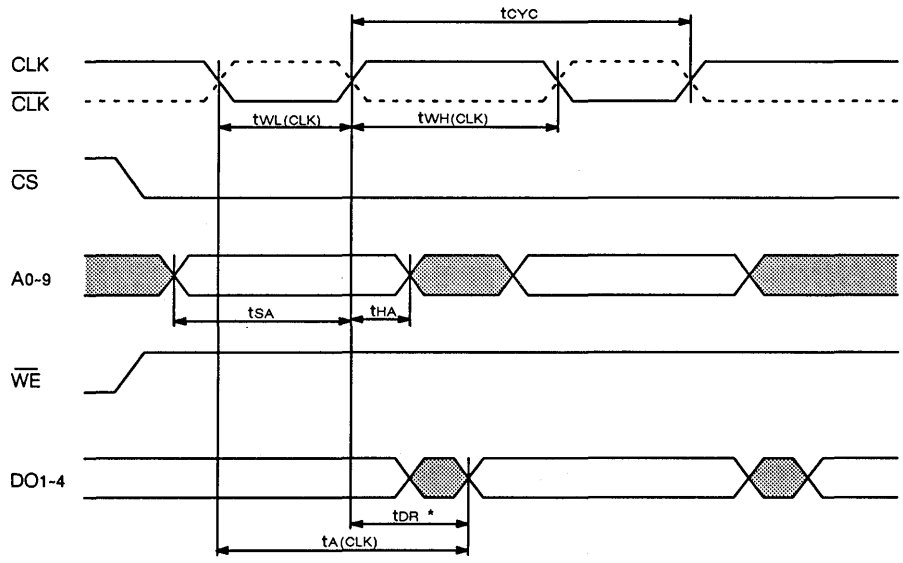
* Output is valid at tDR when tSC > tA(CS) max − tDR max.

• ADDRESS ACCESS MODE



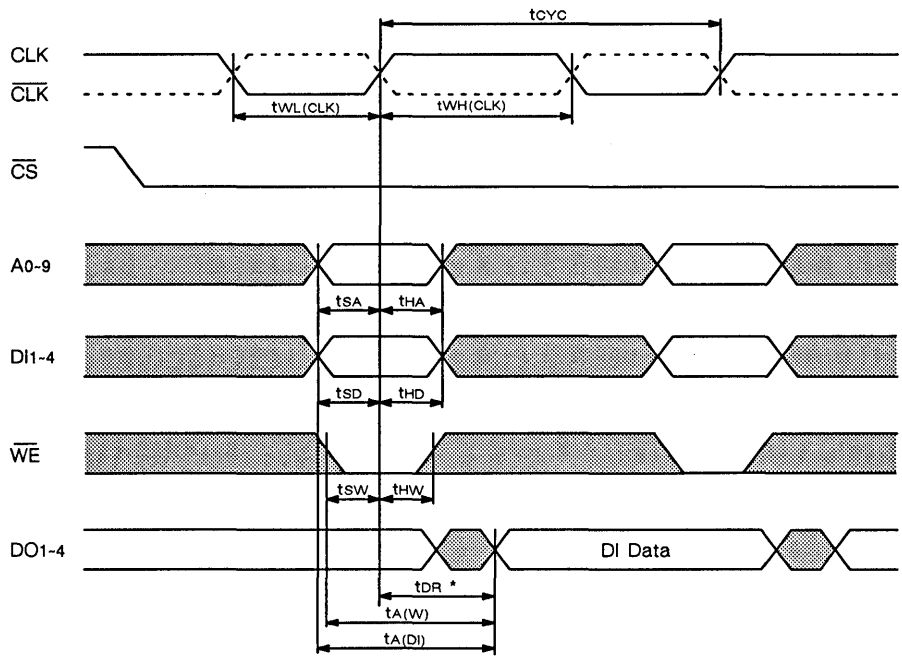
* Output is valid at tDR when tSA > tA(ADD) max − tDR max.

● CLOCK ACCESS MODE



* Output is valid at tDR when tWL(CLK) > tA(CLK) max − tDR max.

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tSW > tA(W) max − tDR max and tSD > tA(DI) max − tDR max

Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

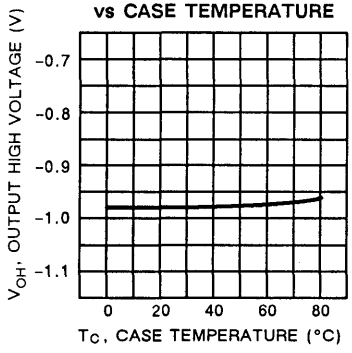


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

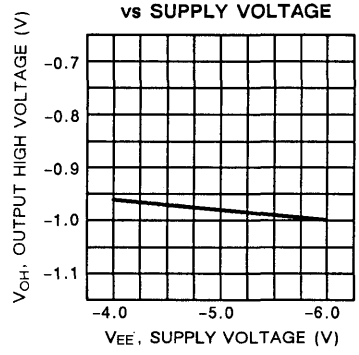


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

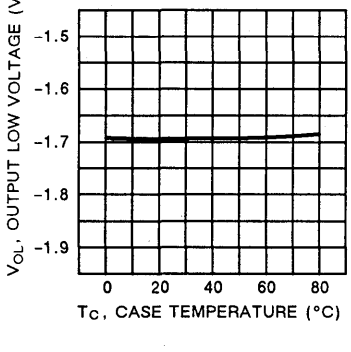


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

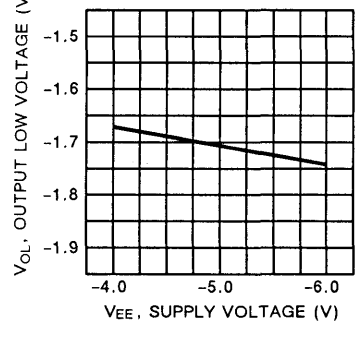


Fig. 7 – REFERENCE VOLTAGE vs CASE TEMPERATURE

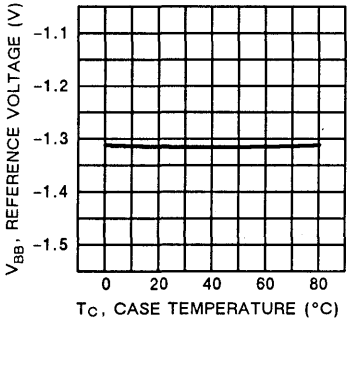
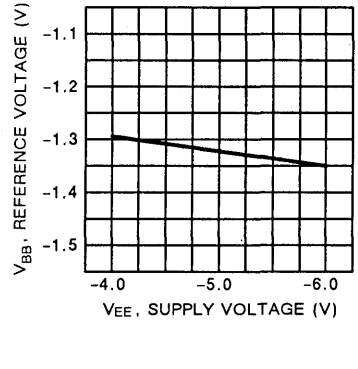


Fig. 8 – REFERENCE VOLTAGE vs SUPPLY VOLTAGE



3

Fig. 9 - SUPPLY CURRENT vs CASE TEMPERATURE

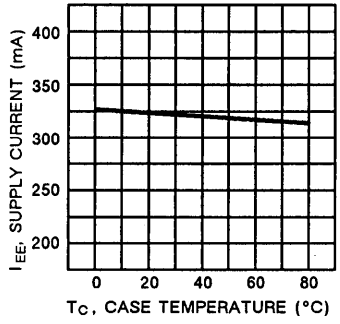


Fig. 10 - SUPPLY CURRENT vs SUPPLY VOLTAGE

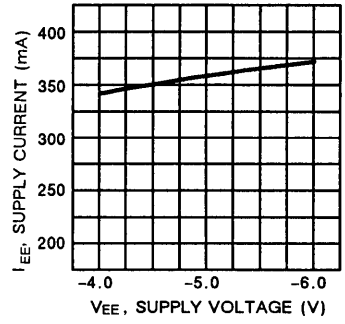


Fig. 11 - ADDRESS ACCESS TIME vs CASE TEMPERATURE

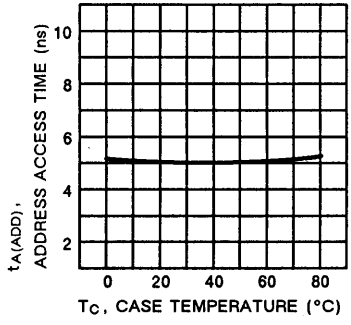


Fig. 12 - ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

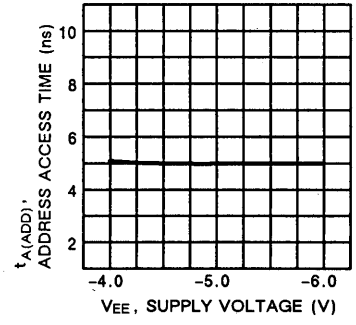


Fig. 13 - CLOCK ACCESS TIME vs CASE TEMPERATURE

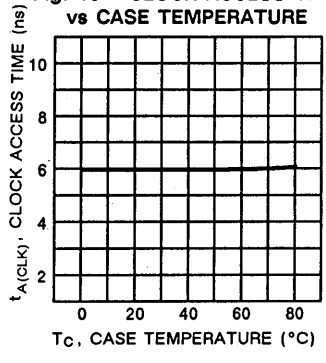


Fig. 14 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

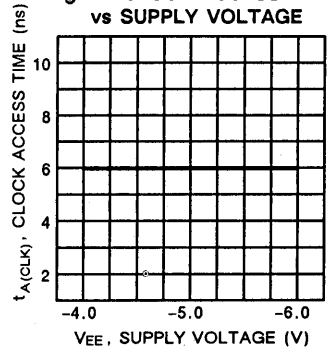


Fig. 15 – OUTPUT DELAY TIME vs CASE TEMPERATURE

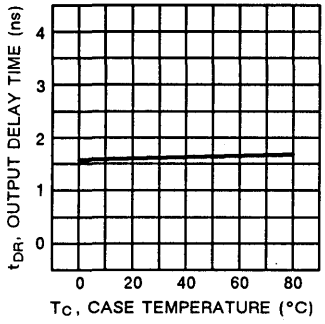


Fig. 16 – OUTPUT DELAY TIME vs SUPPLY VOLTAGE

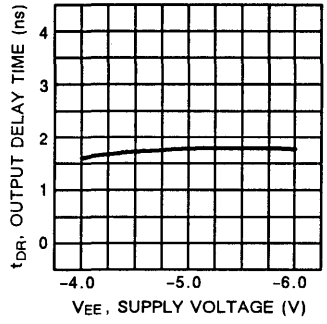


Fig. 17 – CLOCK PULSE WIDTH HIGH vs CASE TEMPERATURE

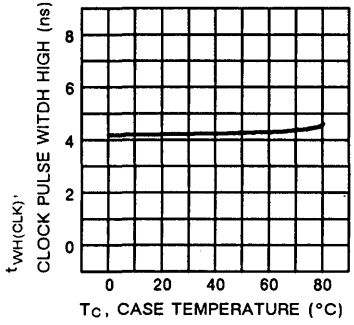
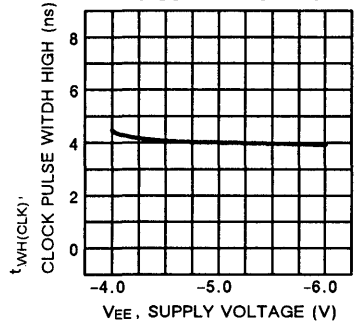


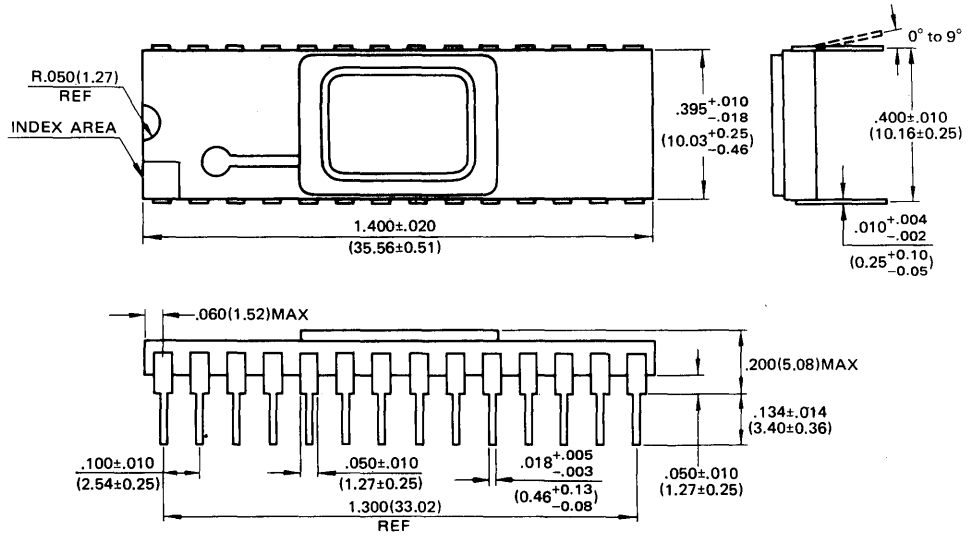
Fig. 18 – CLOCK PULSE WIDTH HIGH vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100476RR-9

December, 1988
Edition 1.0

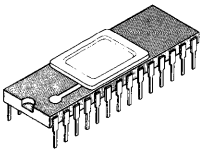
4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

The Fujitsu MBM100476RR-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with registered inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register circuits allows to decrease the number of device on the board.

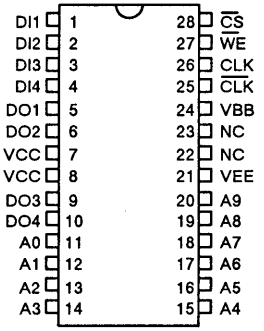
Operation for the MBM100476RR is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 9ns
  Output delay time : 3ns
- Power dissipation : 1800mW max
- Open emitter output for ease of memory expansion
- Edge triggered registers for inputs and outputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

ABSOLUTE MAXIMUM RATINGS (See NOTE)

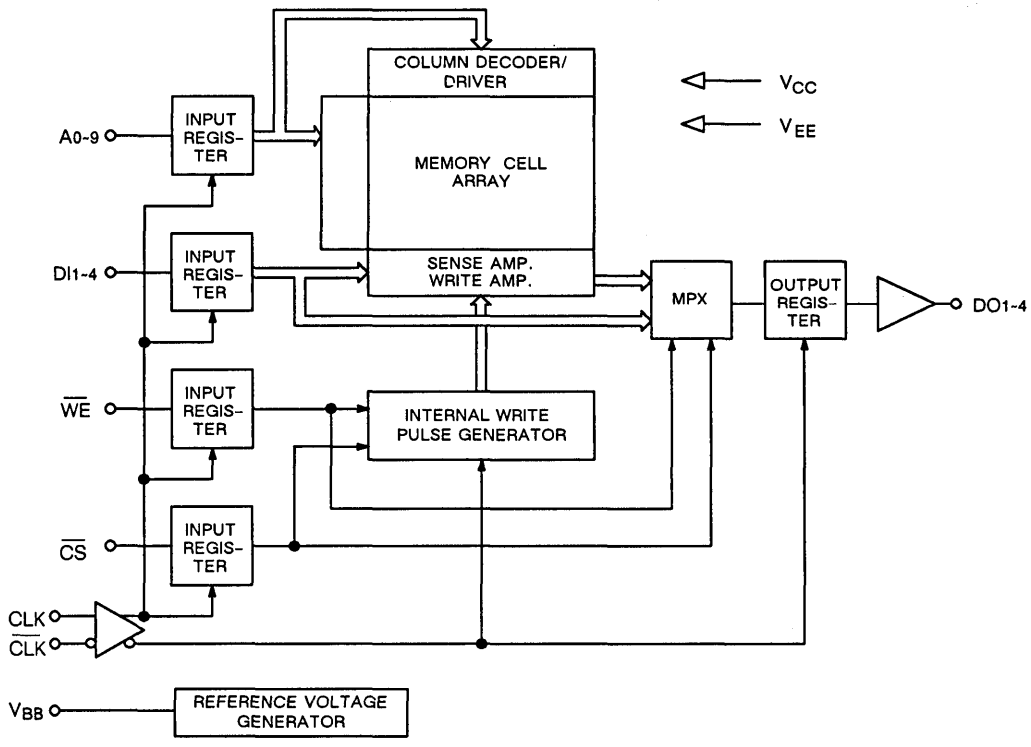
Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	Tc	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

3

Fig.1 - MBM100476RR-9 BLOCK DIAGRAM



FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.32V)
VEE	Supply Voltage (-4.5V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TC = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			mA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM100476RR is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are edge triggered registered controlled by the clock input (CLK/$\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input and output registers are transparent when CLK ($\overline{CLK}$) goes high (low), and close to hold the data when CLK($\overline{CLK}$) goes low (high).

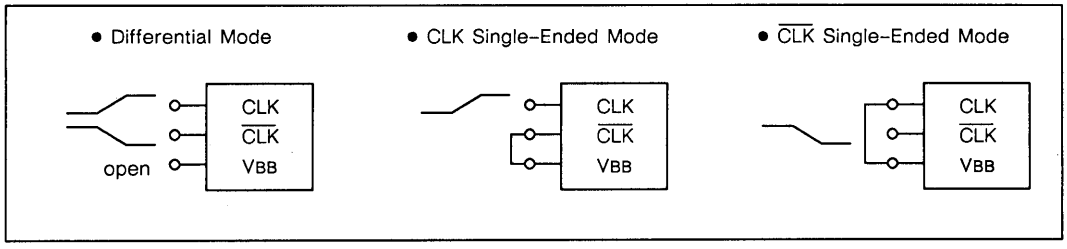
When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels may not be stable during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes low (high), address data is held at output, while output data is kept valid during the same cycle. Thus, the output data becomes available at the next rising (falling) edge of CLK ($\overline{CLK}$).

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), inputs are transparent while previous read data appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the output by the CLK($\overline{CLK}$) rising (falling) edge of the next cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



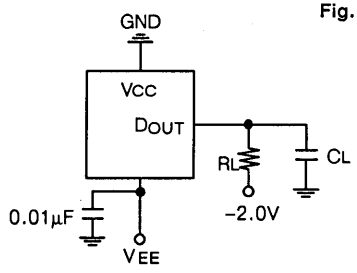
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

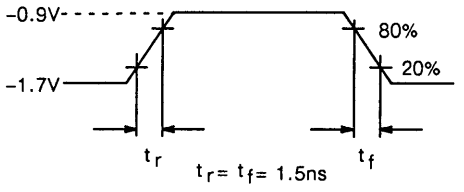
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	3.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0 *2			ns
Cycle Time	t_{CYC}	9.0			ns
Output Delay Time	t_{DR}			3.0	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) > 6.0ns
*2 Specified at tWH(CLK) > 6.0ns

Fig. 2 - AC TEST CONDITIONS



Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)

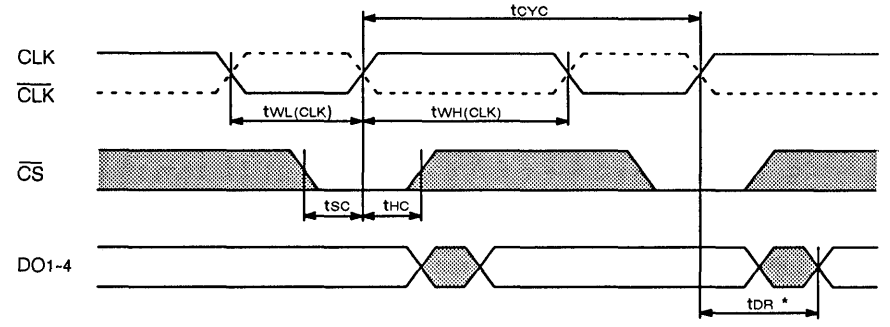


Note : All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

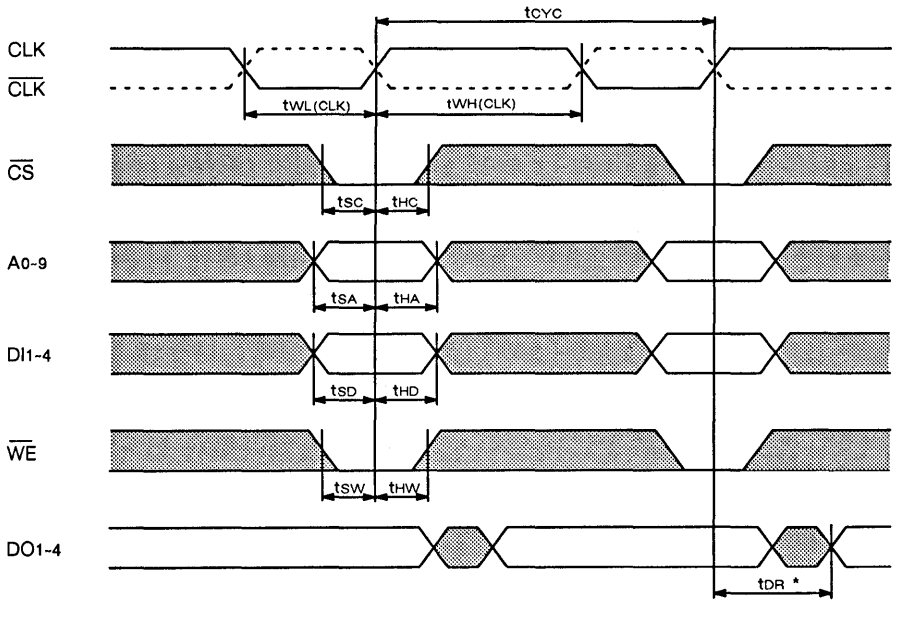
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

READ CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

WRTE CYCLE TIMING DIAGRAMS



* Output data appears in the next cycle.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

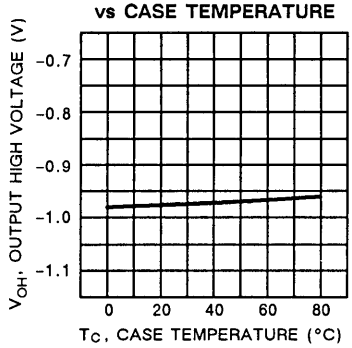


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

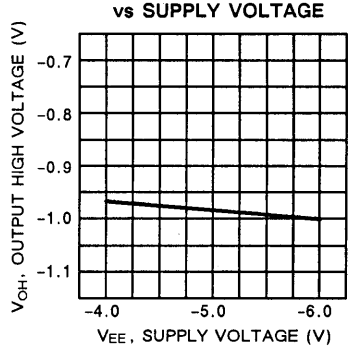


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

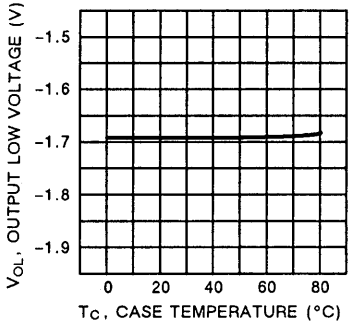


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

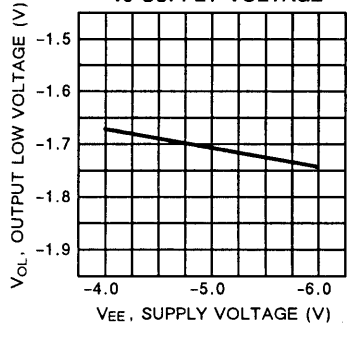


Fig. 7 – REFERENCE VOLTAGE vs CASE TEMPERATURE

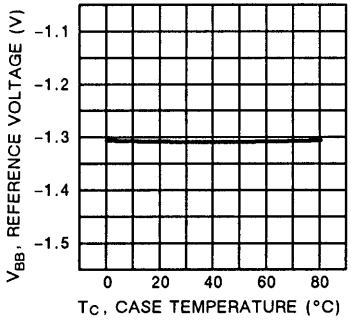


Fig. 8 – REFERENCE VOLTAGE vs SUPPLY VOLTAGE

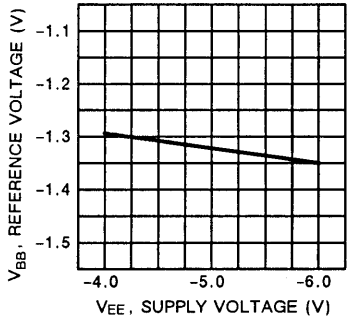


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Fig. 9 - SUPPLY CURRENT vs CASE TEMPERATURE

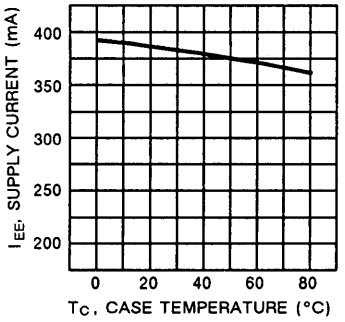


Fig. 10 - SUPPLY CURRENT vs SUPPLY VOLTAGE

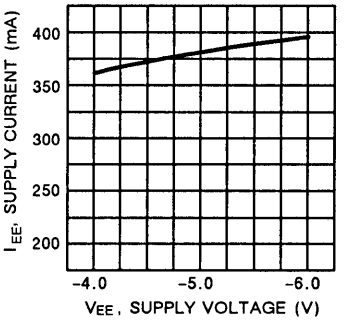


Fig. 11 - OUTPUT DELAY TIME vs CASE TEMPERATURE

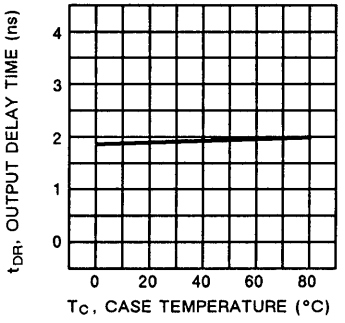
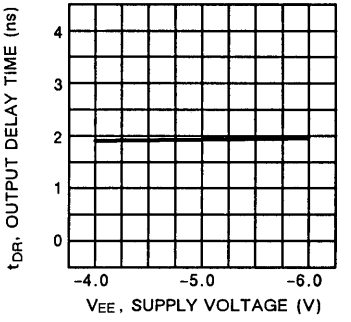


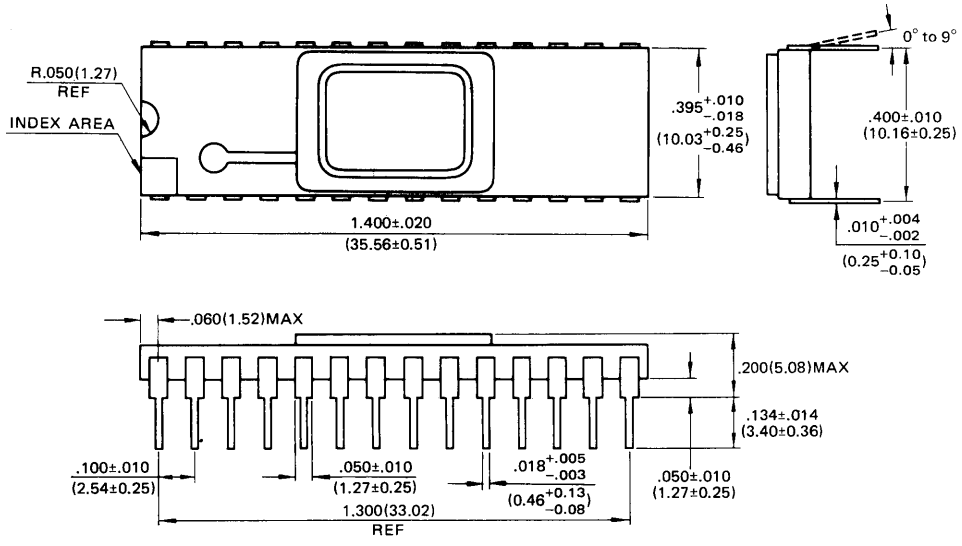
Fig. 12 - OUTPUT DELAY TIME vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

FUJITSU

ECL 4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100476RL-9

4096-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

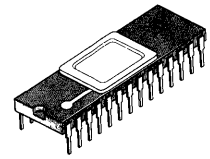
December, 1988
Edition 1.0

The Fujitsu MBM100476RL-9 is fully decoded 4096-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 1024 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with registered inputs and latched outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register/latch circuits allows to decrease the number of device on the board.

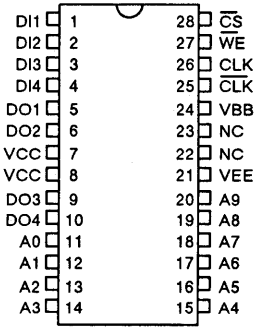
Operation for the MBM100476RL is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.

- 1024 words by 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 9ns
  Output delay time : 3ns
- Power dissipation : 1800MW max
- Open emitter output for ease of memory expansion
- Level-sensitive D-type latch for outputs and edge triggered registers for inputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and U-FOX processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

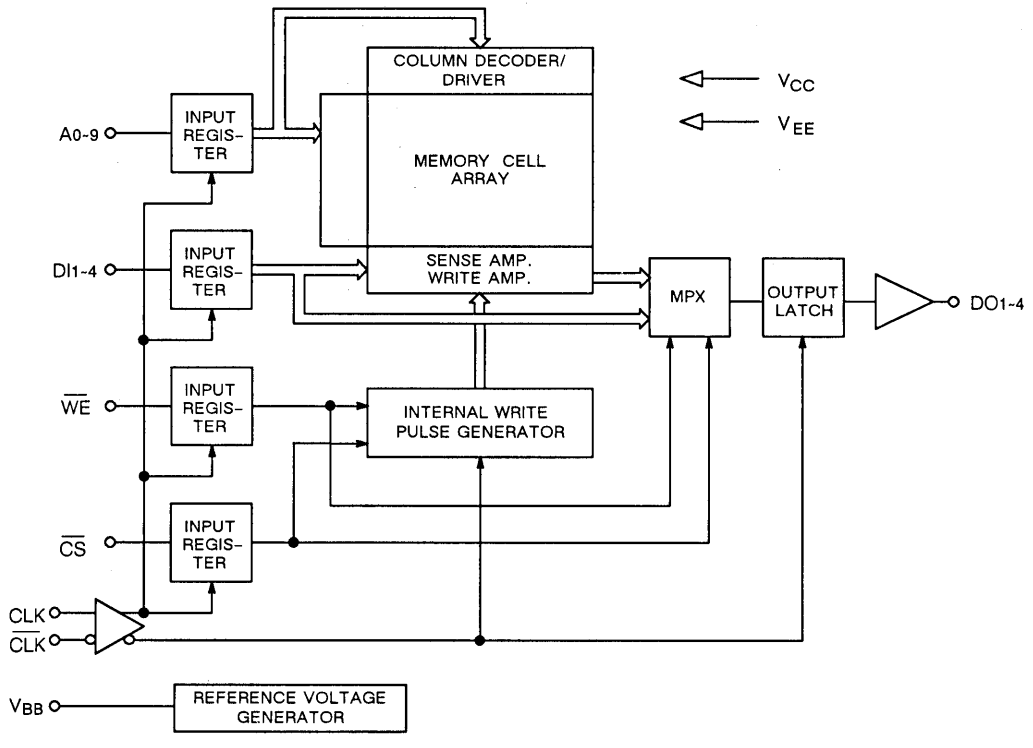
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM100476RL-9 BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A9	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.32V)
VEE	Supply Voltage (-4.5V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = -4.5V, Output Load = 50Ω to -2.0V, T_C = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-400			mA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM100476RL is fully decoded 4096-bit read/write self-timed random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designated A0 through A9. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) furnish edge triggered registers, whereas outputs (DOUT) have level sensitive transparent latches.

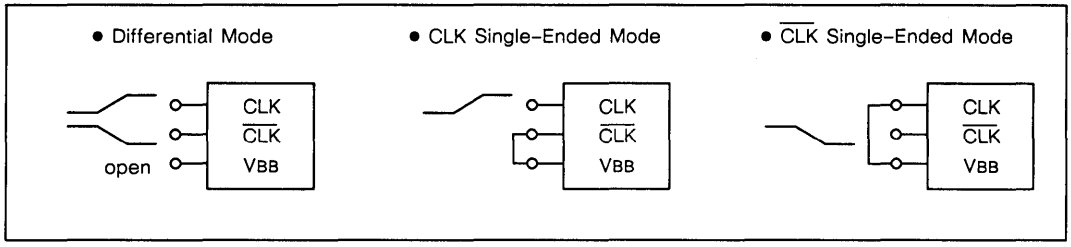
When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. All input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input levels are free to change for the rest of the cycle time once input data is held into the input register. Read out data becomes available during CLK low state in which output latches are transpatent. When CLK ($\overline{CLK}$) state is wide enough than the internal RAM access time, output data become valid in the short delay time (tDR) after the falling (rising)edge of CLK ($\overline{CLK}$).

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully self-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



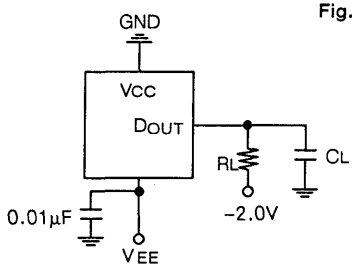
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V ±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

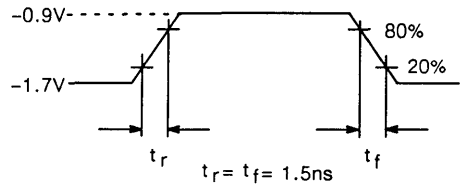
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	3.0 *1			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0 *2			ns
Cycle Time	t_{CYC}	9.0			ns
Clock Access Time	$t_{A(CLK)}$			8.0 *3	ns
Output Delay Time	t_{DR}			3.0 *4	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tWL(CLK) > 6.0ns
*2 Specified at tWH(CLK) > 6.0ns
*3 Specified at tWH(CLK) = 3.0ns
*4 Specified at tWH(CLK) > tA(CLK) max

Fig. 2 - AC TEST CONDITIONS



Output Lead : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



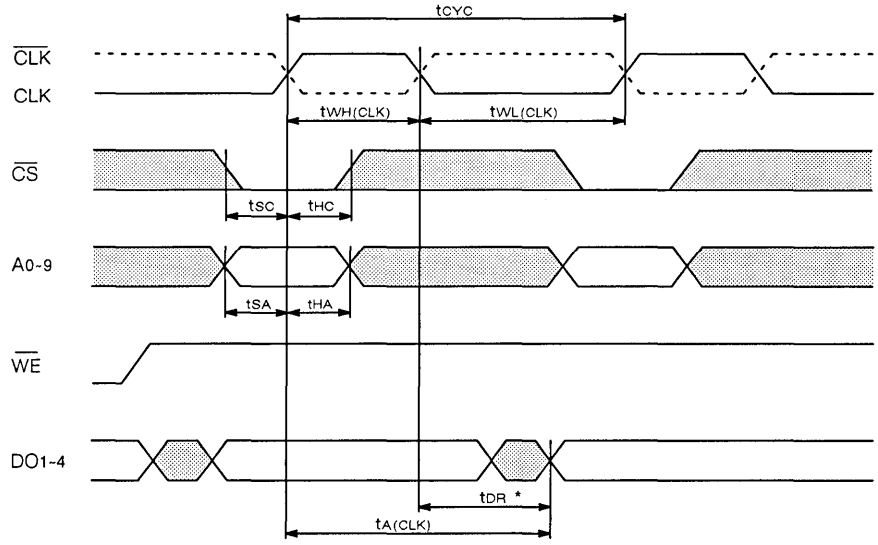
Note : All timing measurements referenced to 50% input levels.

3

Rise Time and Fall Time

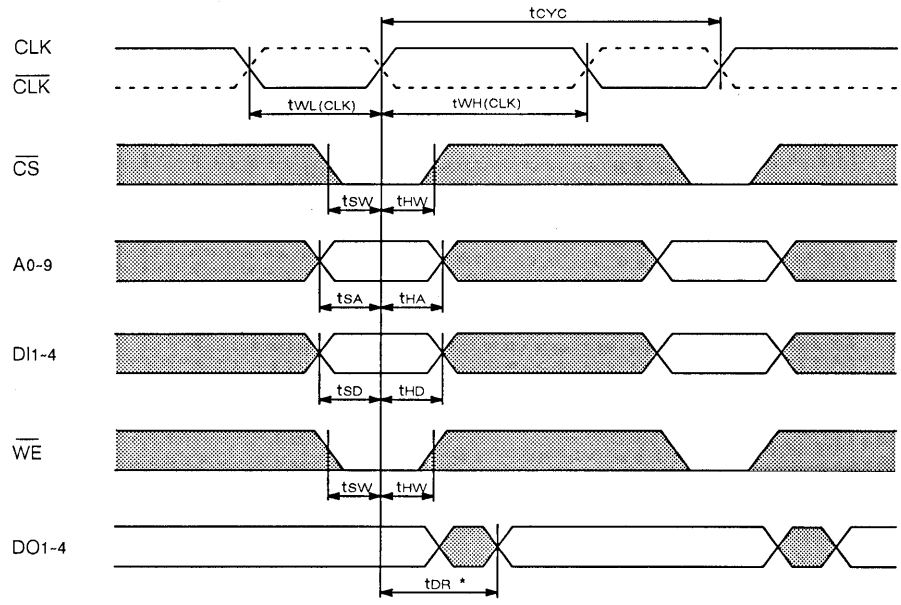
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

READ CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tWH(CLK) > tA(CLK) max − tDR max.

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tWH(CLK) > tA(CLK) max − tDR max.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

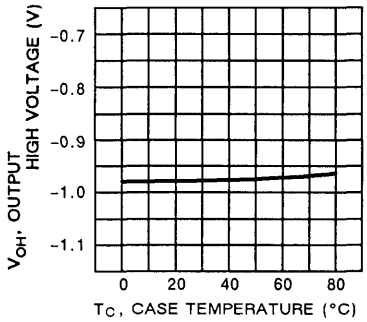


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

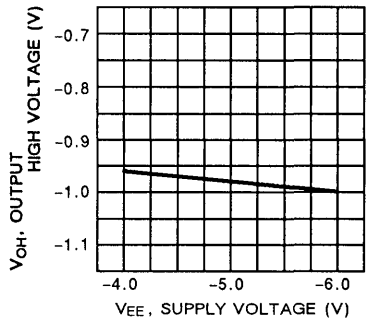


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

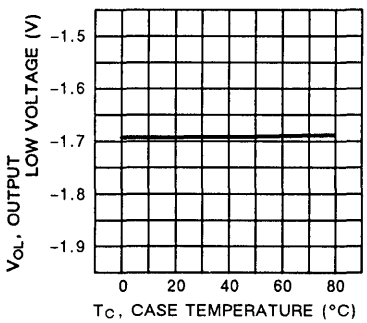


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

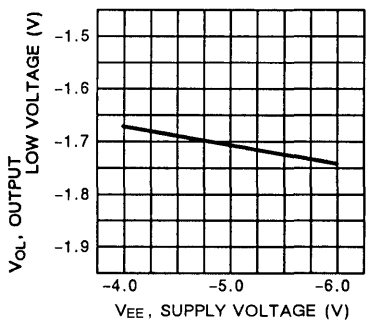


Fig. 7 – REFERENCE VOLTAGE vs CASE TEMPERATURE

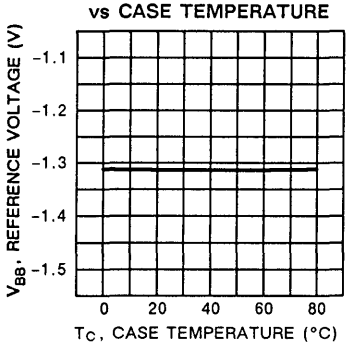


Fig. 8 – REFERENCE VOLTAGE vs SUPPLY VOLTAGE

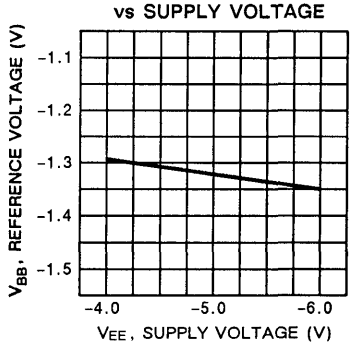


Fig. 9 - SUPPLY CURRENT vs CASE TEMPERATURE

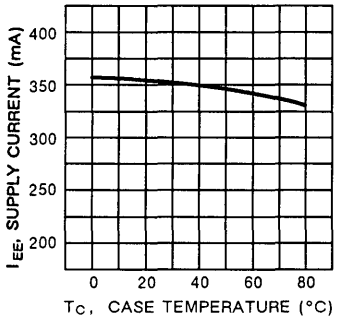


Fig. 10 - SUPPLY CURRENT vs SUPPLY VOLTAGE

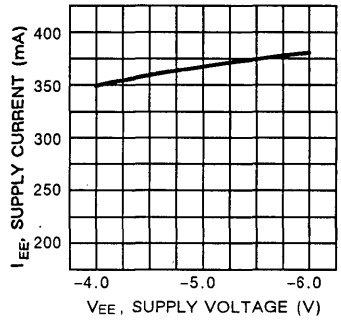


Fig. 11 - CLOCK ACCESS TIME vs CASE TEMPERATURE

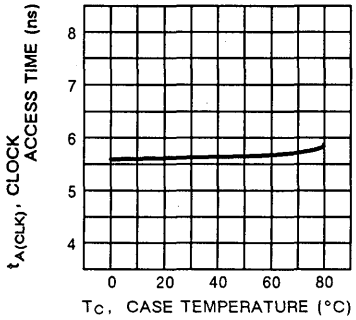


Fig. 12 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

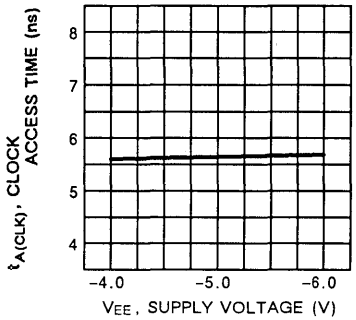


Fig. 13 - OUTPUT DELAY TIME vs CASE TEMPERATURE

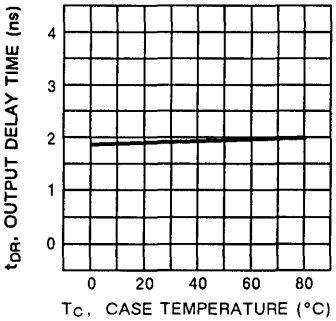
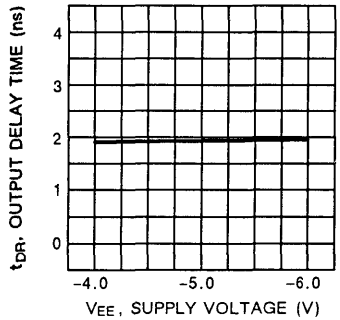


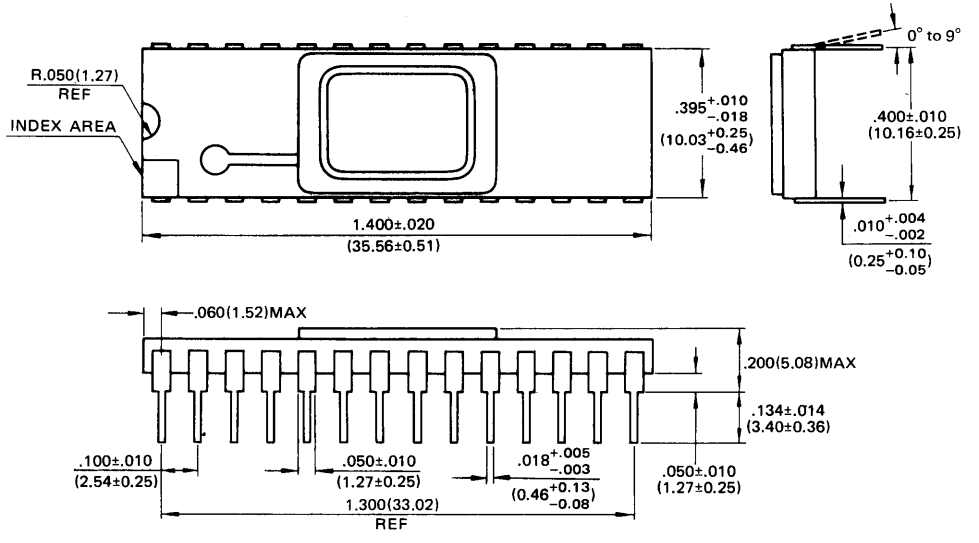
Fig. 14 - OUTPUT DELAY TIME vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

3

FUJITSU

ECL 16384 BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10486LL-13

16384-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

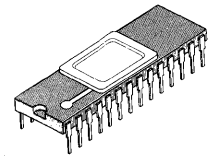
December, 1988
Edition 2.0

The Fujitsu MBM10486LL-13 is fully decoded 16384-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with latched inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded latch circuits allows to decrease the number of device on the board.

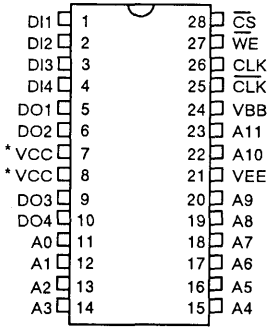
Operation for the MBM10486LL is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 4096 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 13ns
  Address access time : 10ns
- Power dissipation : 1976mW max
- Open emitter output for ease of memory expansion
- D-type latches are used for input and output latches
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and IOP-II processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

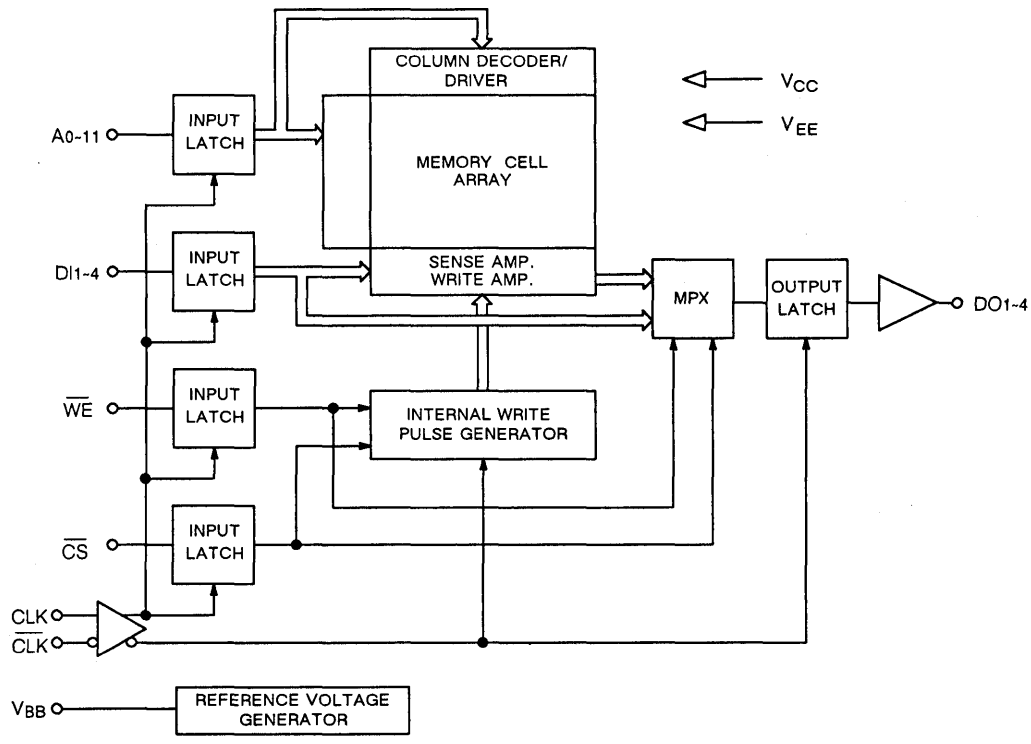
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM10486LL BLOCK DIAGRAM



FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A11	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.29V)
VEE	Supply Voltage (-5.2V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	V	0°C to 75°C

DC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V, Output Load = 50Ω to -2.0V, TC = 0°C to 75°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	TC
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA	0°C to 75°C
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA	0°C to 75°C
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA	0°C to 75°C
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-380			mA	0°C to 75°C
Reference Voltage	V_{BB}	-1405 -1390 -1365		-1230 -1190 -1130	mV	0°C 25°C 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10486LL is fully decoded 16384-bit read/write self-timed random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designated A0 through A11. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are level sensitive transparent latches controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input latches are transparent when CLK ($\overline{CLK}$) goes low (high), and close to hold the data when CLK($\overline{CLK}$) goes high (low) and on the other hand, output latches are transparent when CLK ($\overline{CLK}$) goes high (low) and data are held in the output latches when CLK ($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) *rising (falling) edge, read operation is specified.* Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (t_S) and the hold time (t_H) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input level may fluctuate during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes high (low), inputs are latched, while previous read data goes through the output latches and appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), input latches are transparent, while output latches are closed and hold the data from the previous cycle.

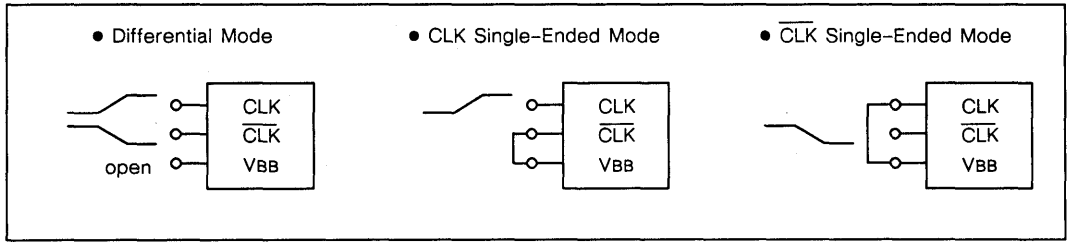
When setup time is wide enough, output data becomes valid in the short delay time (t_{DR}) after the rising (falling) edge of CLK ($\overline{CLK}$). When setup time is short, output data appears on the outputs after the specified RAM access time ($t_{A(ADD)}$) similar to the traditional RAM.

The write operation is initiated by the *rising (falling)* edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and Address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully sef-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (V_{BB}) pin. When CLK and $\overline{CLK}$ are used as differential inputs, V_{BB} pin is left open.



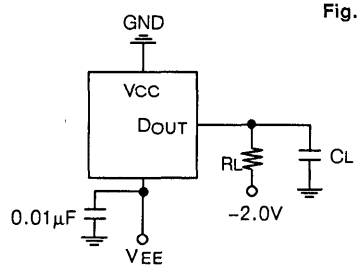
AC CHARACTERISTICS

(VCC = 0V, VEE = -5.2V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 75°C, unless otherwise noted.)

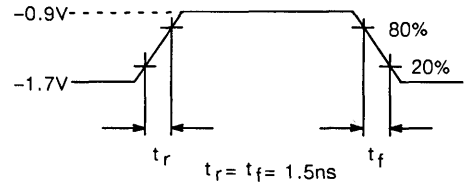
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	10.0			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0			ns
Cycle Time	t_{CYC}	13.0			ns
Address Access Time	$t_{A(ADD)}$			10.0 *1	ns
Data Access Time	$t_{A(DI)}$			5.0 *2	ns
Write Access Time	$t_{A(W)}$			5.0 *3	ns
Chip Select Access Time	$t_{A(CS)}$			5.0 *4	ns
Clock Access Time	$t_{A(CLK)}$			11.0 *5	ns
Output Delay Time	t_{DR}			4.0 *6	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at tSA = 1.0ns
*2 Specified at tSD = 1.0ns
*3 Specified at tSW = 1.0ns
*4 Specified at tSC = 1.0ns
*5 Specified at tWL(CLK) = 3.0ns
*6 Specified when $t_{WL(CLK)} > t_{A(CLK)\ max}$, $t_{SA} > t_{A(ADD)\ max}$, $t_{SC} > t_{A(CS)\ max}$, $t_{SD} > t_{A(DI)\ max}$, $t_{SW} > t_{A(W)\ max}$.

Fig. 2 - AC TEST CONDITIONS



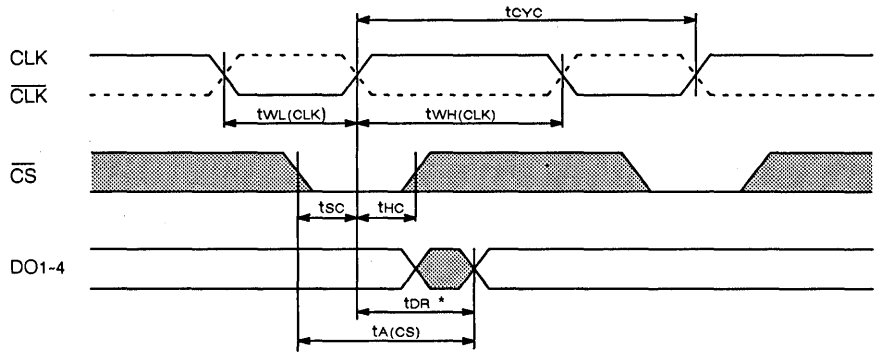
Output Load : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



Note : All timing measurements referenced to 50% input levels.

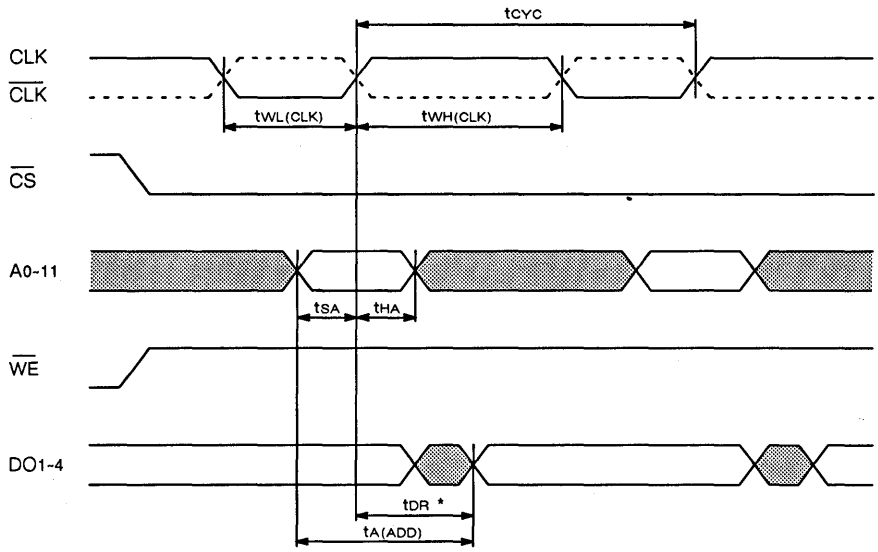
READ CYCLE TIMING DIAGRAMS

- CHIP SELECT ACCESS MODE



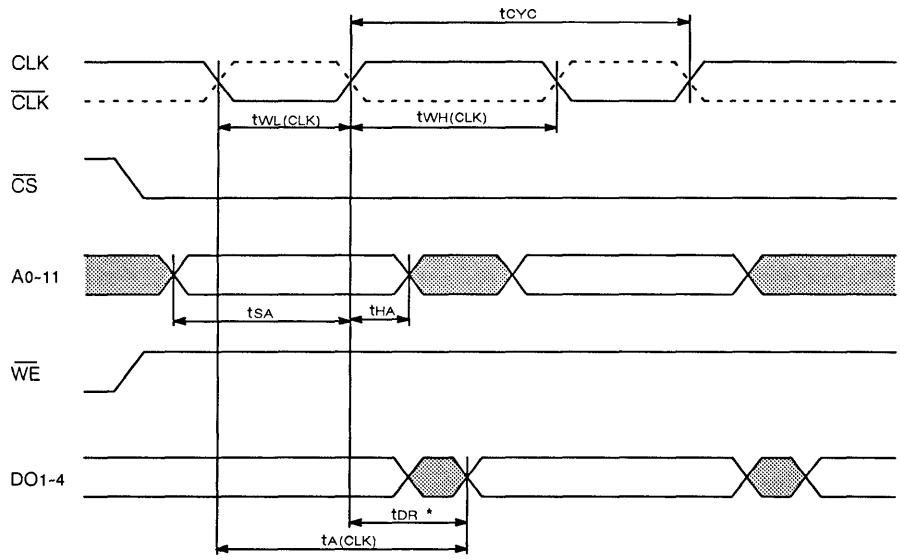
* Output is valid at t_{DR} when $t_{SC} > t_{A(CS)}$ max − t_{DR} max.

- ADDRESS ACCESS MODE



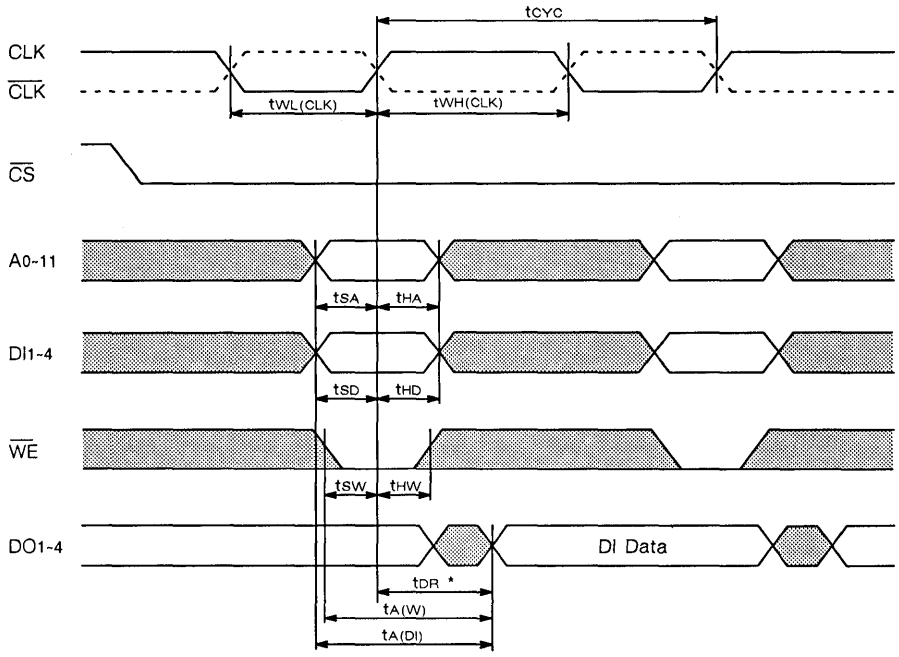
* Output is valid at t_{DR} when $t_{SA} > t_{A(ADD)}$ max − t_{DR} max.

• CLOCK ACCESS MODE



* Output is valid at t_{DR} when $t_{WL(CLK)} > t_{A(CLK)\ max} - t_{DR\ max}$

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at t_{DR} when $t_{SW} > t_{A(W)\ max} - t_{DR\ max}$ and $t_{SD} > t_{A(DI)\ max} - t_{DR\ max}$

Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 - OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

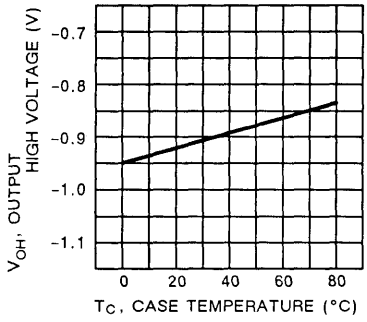


Fig. 4 - OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

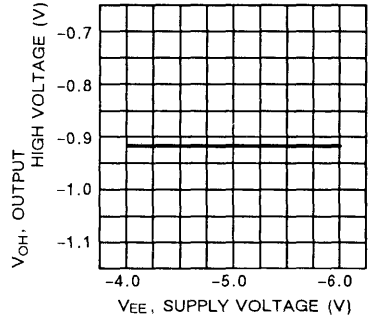


Fig. 5 - OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

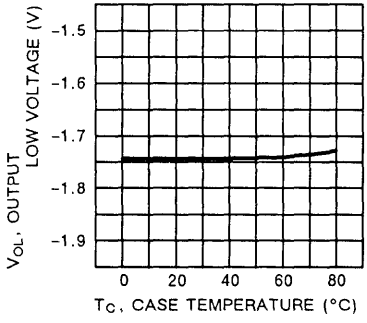


Fig. 6 - OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

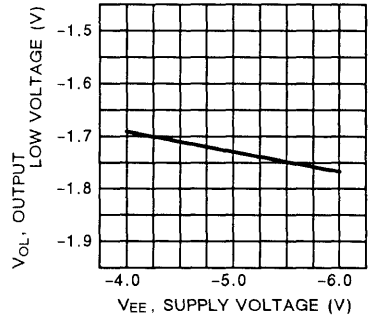


Fig. 7 - REFERENCE VOLTAGE vs CASE TEMPERATURE

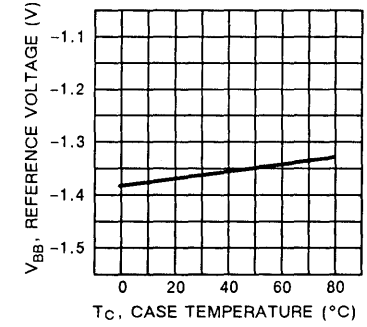
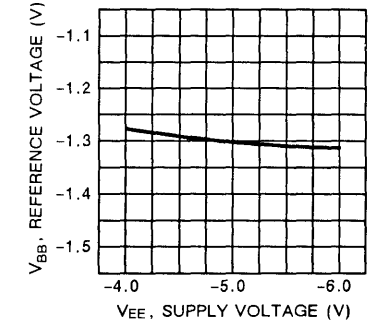


Fig. 8 - REFERENCE VOLTAGE vs SUPPLY VOLTAGE



3

Fig. 9 – SUPPLY CURRENT vs CASE TEMPERATURE

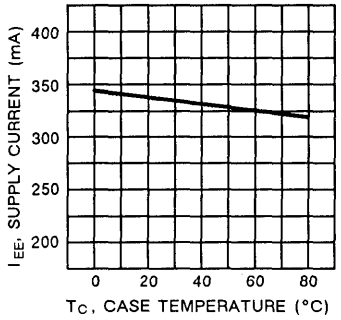
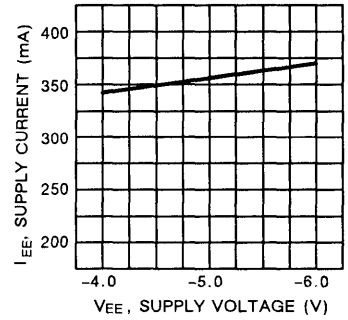


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE



3

Fig. 11 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

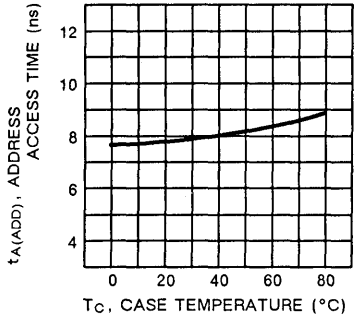


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

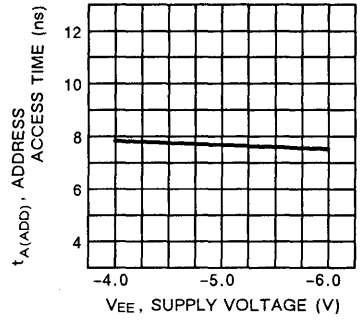


Fig. 13 – CLOCK ACCESS TIME vs CASE TEMPERATURE

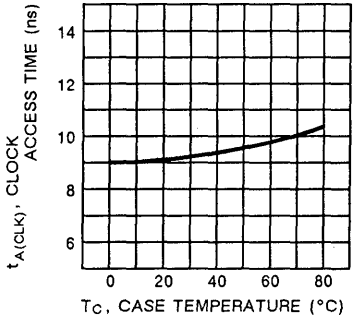


Fig. 14 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

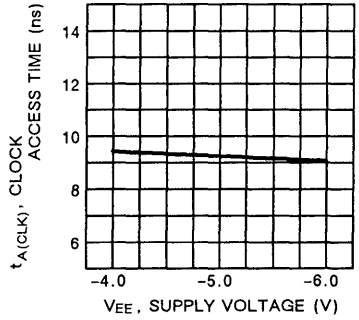


Fig. 15 – OUTPUT DELAY TIME vs CASE TEMPERATURE

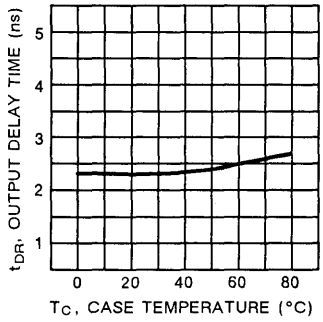


Fig. 16 – OUTPUT DELAY TIME vs SUPPLY VOLTAGE

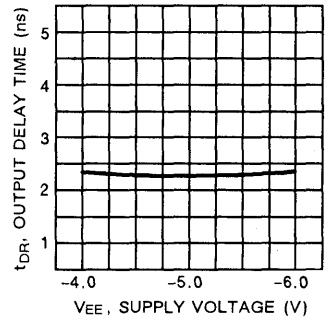


Fig. 17 – CLOCK PULSE WIDTH HIGH vs CASE TEMPERATURE

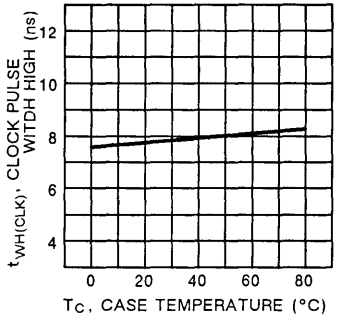
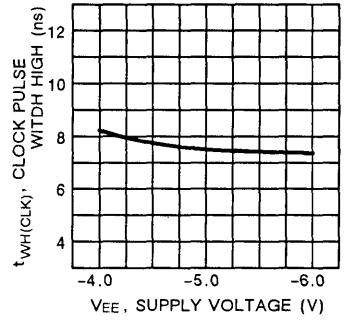


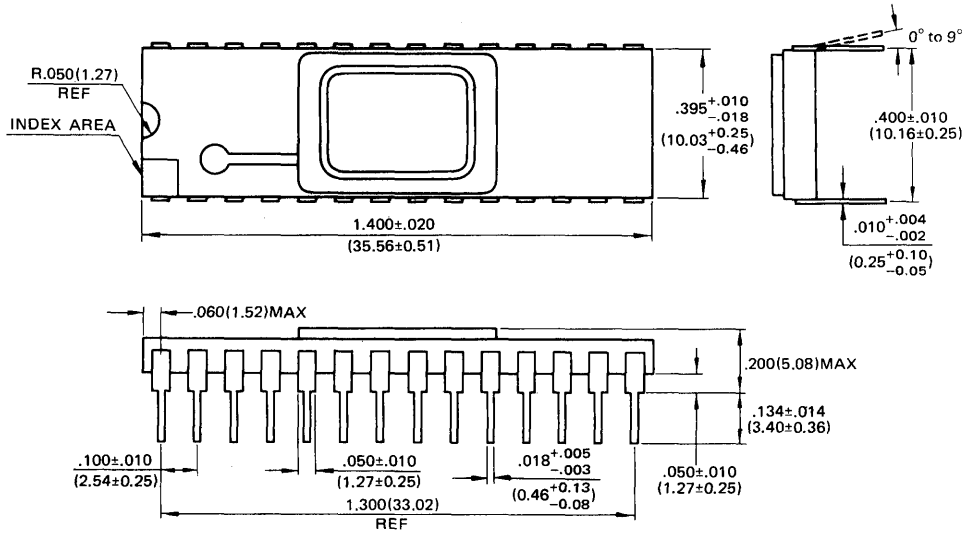
Fig. 18 – CLOCK PULSE WIDTH HIGH vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

FUJITSU

ECL 16384 BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10486RR-13

Nobember, 1988
Edition 1.0

16384-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

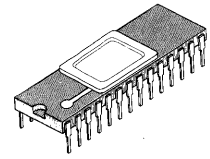
The Fujitsu MBM10486RR-13 is fully decoded 16384-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with registered inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register circuits allows to decrease the number of device on the board.

Operation for the MBM10486RR is specified over a case temperature range of from 0°C to 75°C (T_C). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 4096 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 13ns
  Output delay time : 3ns
- Power dissipation : 2080mW max
- Open emitter output for ease of memory expansion
- Edge triggered registers for inputs and outputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and IOP-II processing
- 28-pin ceramic side-brazed DIP (Suffix: C)

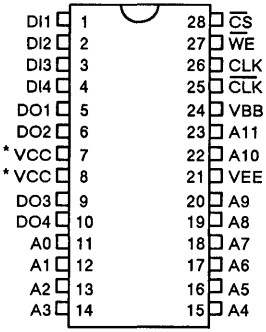
ADVANCE INFORMATION



CERAMIC PACKAGE
DIP-28C-A06

3

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} ground

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

FUJITSU

ECL 16384 BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM10486RL-13

November, 1988
Edition 1.0

ADVANCE INFORMATION

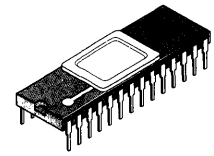
16384-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

The Fujitsu MBM10486RL-13 is fully decoded 16384-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The STRAM with registered inputs and latched outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register/latch circuits allows to decrease the number of device on the board.

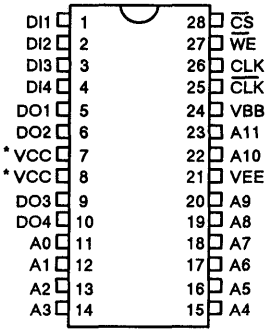
Operation for the MBM10486RL is specified over a case temperature range of from 0°C to 75°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 10K-series ECL families.

- 4096 words by 4 bits organization
- On-chip voltage compensation for improved noise margin
- Fully compatible with industory standrad 10K series ECL families
- Cycle time : 13ns
  Output delay time : 3ns
- Power dissipation : 2080mW max
- Open emitter output for ease of memory expansion
- Level-sensitive D-type latch for output and edge triggered registers for inputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and IOP-II processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} ground

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

FUJITSU

ECL 16384 BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100486LL-13

16384-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

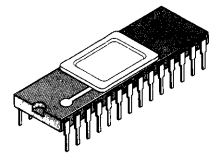
December, 1988
Edition 2.0

The Fujitsu MBM100486LL-13 is fully decoded 16384-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with latched inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded latch circuits allows to decrease the number of device on the board.

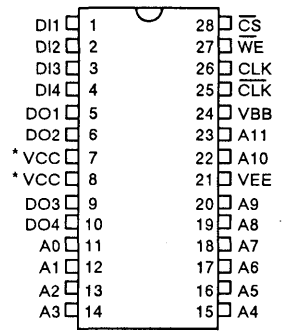
Operation for the MBM100486LL is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.

- 4096 words by 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 13ns
  Address access time : 10ns
- Power dissipation : 1710mW max
- Open emitter output for ease of memory expansion
- D-type latches are used for input and output latches
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and IOP-II processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} grounded

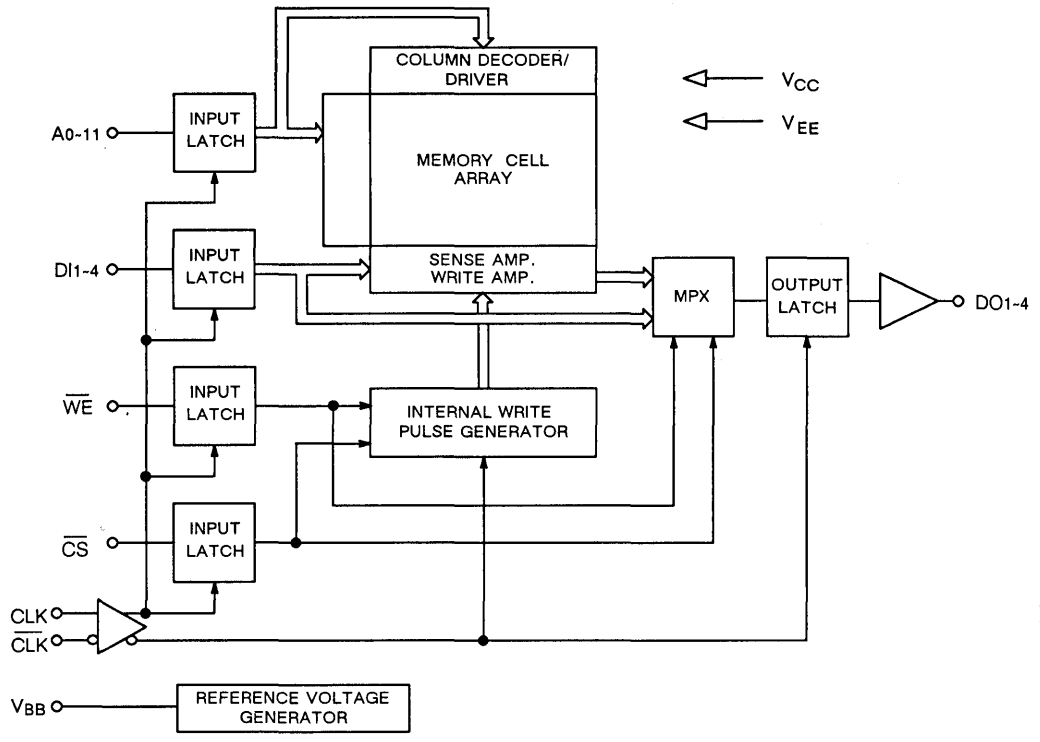
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	Tc	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

Fig.1 - MBM100486LL BLOCK DIAGRAM



3

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI	CLK/$\overline{CLK}$	Output	Mode
H	X	X		L	DISABLE
L	L	L		L	WRITE "L"
L	L	H		H	WRITE "H"
L	H	X		DOUT	READ

L : Low voltage level, H : High voltage level, X : Don't care

: Outputs are initiated by rising (falling) edge of CLK ($\overline{CLK}$).

PIN DESIGNATION

Symbol	Pin Name
A0 thru A11	Address Inputs
DI1 thru DI4	Data Inputs
DO1 thru DO4	Data Outputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
CLK, $\overline{CLK}$	Clock Inputs
VBB	Reference Voltage (-1.32V)
VEE	Supply Voltage (-4.5V)
VCC	Supply Voltage (0V)
NC	No Connection

GUARANTEED OPERATING CONDITIONS

(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit	Case Temperature (T_C)
Supply Voltage	V_{EE}	-5.7	-4.5	-4.2	V	0°C to 85°C

*Guaranteed Operating Conditions define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V, Output Load = 50Ω to -2.0V, TC = 0°C to 85°C, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output High Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OH}	-1025		-880	mV
Output Low Voltage (V_{IN} = V_{IH} max or V_{IL} min)	V_{OL}	-1810		-1620	mV
Output High Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OHC}	-1035			mV
Output Low Voltage (V_{IN} = V_{IH} min or V_{IL} max)	V_{OLC}			-1610	mV
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1165		-880	mV
Input low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1810		-1475	mV
Input High Current (V_{IN} = V_{IH} max)	I_{IH}			220	µA
Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	-50			µA
$\overline{CS}$ Input Low Current (V_{IN} = V_{IL} min)	I_{IL}	0.5		170	µA
Power Supply Current (All Inputs and All Outputs Open)	I_{EE}	-380			mA
Reference Voltage	V_{BB}	-1390		-1250	mV

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4		pF
Output Pin Capacitance	C_{OUT}		6		pF

FUNCTIONAL DESCRIPTIONS

The Fujitsu MBM10486LL is fully decoded 16384-bit read/write self-timed random access memory organized as 4096 words by 4 bits. Memory cell selection is achieved by means of a 12-bit address designated A0 through A11. All of the inputs, address (A), data-in (DIN), write enable ($\overline{WE}$), chip select ($\overline{CS}$) and outputs (DOUT) are level sensitive transparent latches controlled by the clock input (CLK/ $\overline{CLK}$). Inputs and outputs become active invertly with respect to the clock signal.

Input latches are transparent when CLK ($\overline{CLK}$) goes low (high), and close to hold the data when CLK($\overline{CLK}$) goes high (low) and on the other hand, output latches are transparent when CLK ($\overline{CLK}$) goes high (low) and data are held in the output latches when CLK ($\overline{CLK}$) goes low (high).

When $\overline{CS}$ is kept low and $\overline{WE}$ is kept high and address is valid on the CLK ($\overline{CLK}$) rising (falling) edge, read operation is specified. Input data such as $\overline{CS}$, $\overline{WE}$ and address should be valid during the setup time (tS) and the hold time (tH) with respect to the CLK ($\overline{CLK}$) rising (falling) edge. This means, input level may fluctuate during the time other than the required setup and hold times. When CLK ($\overline{CLK}$) goes high (low), inputs are latched, while previous read data goes through the output latches and appears on the outputs. On the other hand, when CLK ($\overline{CLK}$) goes low (high), input latches are transparent, while output latches are closed and hold the data from the previous cycle.

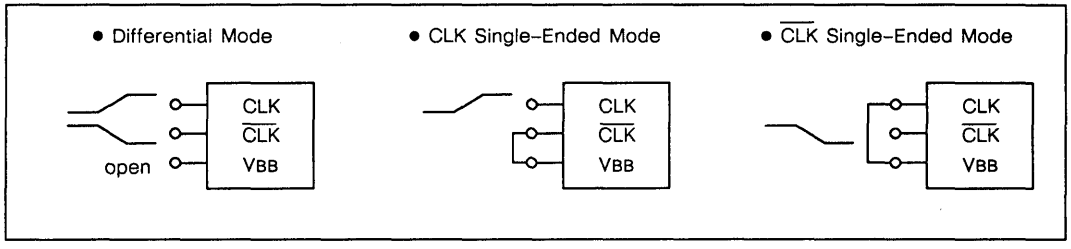
When setup time is wide enough, output data becomes valid in the short delay time (tDR) after the rising (falling) edge of CLK ($\overline{CLK}$). When setup time is short, output data appears on the outputs after the specified RAM access time (tA(ADD)) similar to the traditional RAM.

The write operation is initiated by the rising (falling) edge of CLK ($\overline{CLK}$). When $\overline{CS}$ and $\overline{WE}$ are kept low and Address and DIN are valid on the rising (falling) edge of CLK ($\overline{CLK}$), data is written into the addressed location during CLK high ($\overline{CLK}$ low) state. At the same time, data to be written appears on the outputs in the same cycle. Internal write pulse is generated in response to the CLK ($\overline{CLK}$) rising (falling) edge and fully sef-timed. Therefore, external control of write pulse width and care for $\overline{WE}$ timing with respect to other input signals are not necessary provided that setup time and hold time are met as specified.

3

CLOCK INPUT

Clock input modes are optional. CLK and $\overline{CLK}$ inputs can be used in a single ended manner by connecting CLK or $\overline{CLK}$ to the internal reference voltage (VBB) pin. When CLK and $\overline{CLK}$ are used as differential inputs, VBB pin is left open.



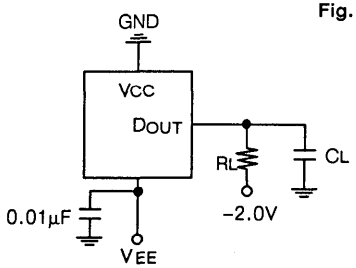
AC CHARACTERISTICS

(VCC = 0V, VEE = -4.5V±5%, Output Load = 50Ω to -2.0V and 30pF to GND, TC = 0°C to 85°C, unless otherwise noted.)

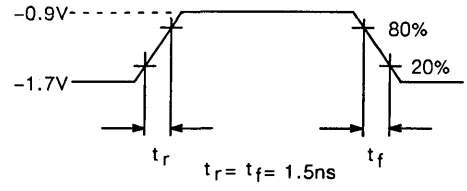
Parameter	Symbol	Min	Typ	Max	Unit
Clock Pulse Width High	$t_{WH(CLK)}$	10.0			ns
Clock Pulse Width Low	$t_{WL(CLK)}$	3.0			ns
Cycle Time	t_{CYC}	13.0			ns
Address Access Time	$t_{A(ADD)}$			10.0 *1	ns
Data Access Time	$t_{A(DI)}$			5.0 *2	ns
Write Access Time	$t_{A(W)}$			5.0 *3	ns
Chip Select Access Time	$t_{A(CS)}$			5.0 *4	ns
Clock Access Time	$t_{A(CLK)}$			11.0 *5	ns
Output Delay Time	t_{DR}			4.0 *6	ns
Address Setup Time	t_{SA}	1.0			ns
Data Setup Time	t_{SD}	1.0			ns
Write Setup Time	t_{SW}	1.0			ns
Chip Select Setup Time	t_{SC}	1.0			ns
Address Hold Time	t_{HA}	2.0			ns
Data Hold Time	t_{HD}	2.0			ns
Write Hold Time	t_{HW}	2.0			ns
Chip Select Hold Time	t_{HC}	2.0			ns

*1 Specified at t_{SA} = 1.0ns
*2 Specified at t_{SD} = 1.0ns
*3 Specified at t_{SW} = 1.0ns
*4 Specified at t_{SC} = 1.0ns
*5 Specified at $t_{WL(CLK)}$ = 3.0ns
*6 Specified when $t_{WL(CLK)} > t_{A(CLK)}$ max, $t_{SA} > t_{A(ADD)}$ max, $t_{SC} > t_{A(CS)}$ max, $t_{SD} > t_{A(DI)}$ max, $t_{SW} > t_{A(W)}$ max.

Fig. 2 - AC TEST CONDITIONS



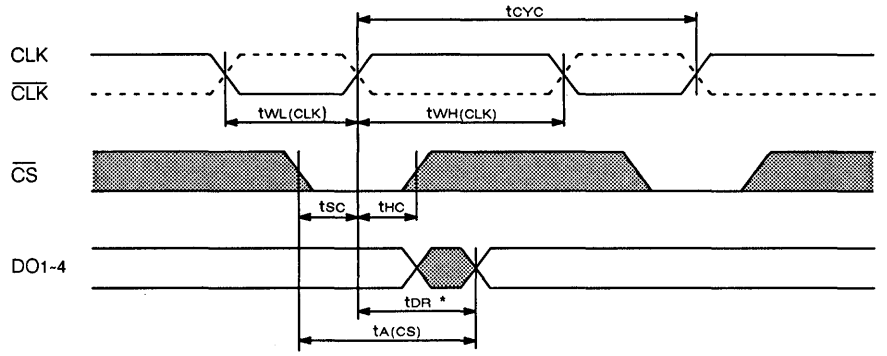
Output Lead : RL = 50Ω
CL = 30pF
(including jig and stray capacitance)



Note : All timing measurements referenced to 50% input levels.

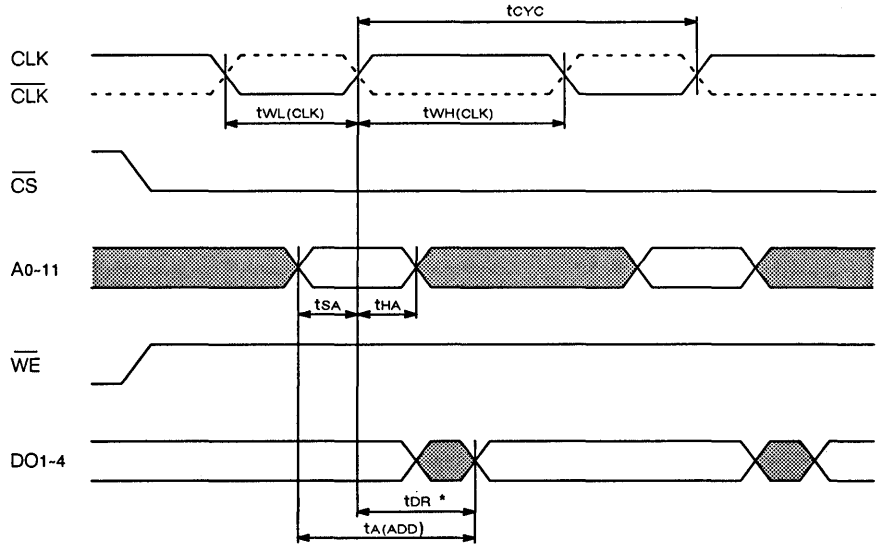
READ CYCLE TIMING DIAGRAMS

- CHIP SELECT ACCESS MODE



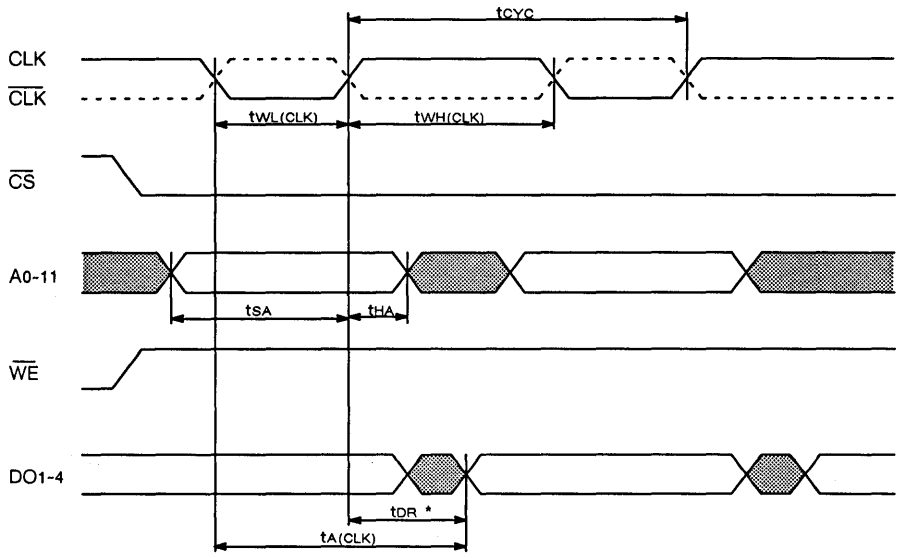
* Output is valid at t_{DR} when $t_{SC} > t_{A(CS)\ max} - t_{DR\ max}$.

- ADDRESS ACCESS MODE



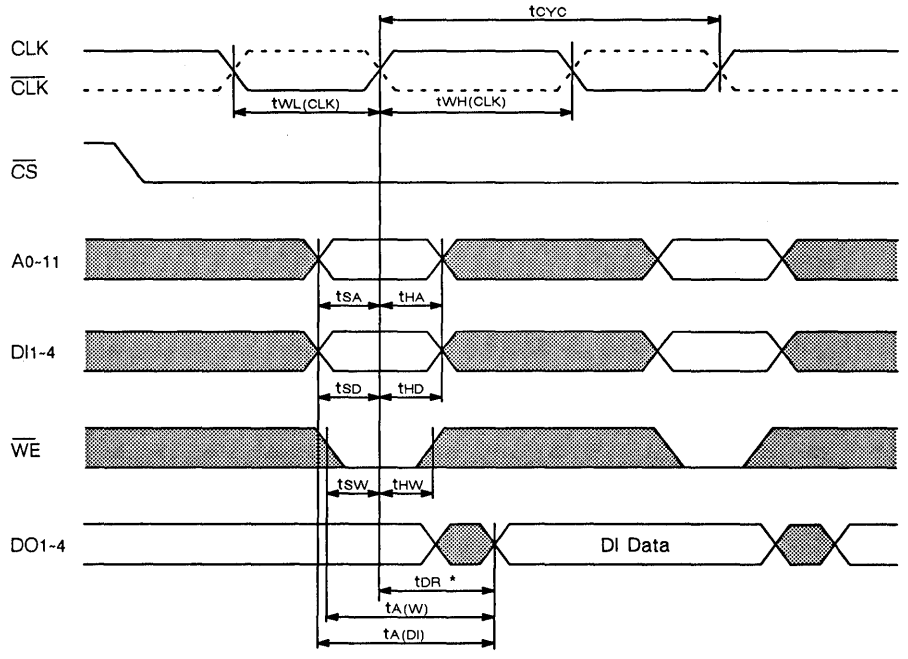
* Output is valid at t_{DR} when $t_{SA} > t_{A(ADD)\ max} - t_{DR\ max}$.

• CLOCK ACCESS MODE



* Output is valid at tDR when tWL(CLK) > tA(CLK) max − tDR max

WRTE CYCLE TIMING DIAGRAMS



* Output is valid at tDR when tSW > tA(W) max − tDR max and tSD > tA(DI) max − tDR max

Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		2.0		ns
Output Fall Time	t_f		2.0		ns

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs CASE TEMPERATURE

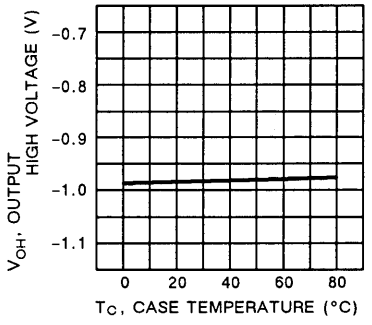


Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

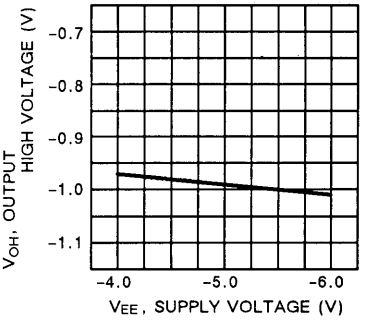


Fig. 5 – OUTPUT LOW VOLTAGE vs CASE TEMPERATURE

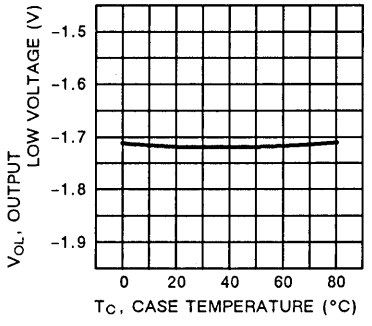


Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

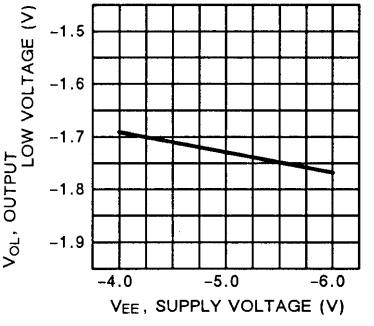


Fig. 7 – REFERENCE VOLTAGE vs CASE TEMPERATURE

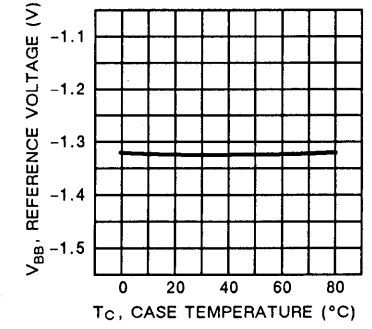
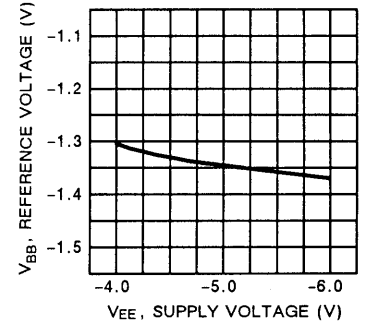


Fig. 8 – REFERENCE VOLTAGE vs SUPPLY VOLTAGE



3

3

Fig. 9 – SUPPLY CURRENT vs CASE TEMPERATURE

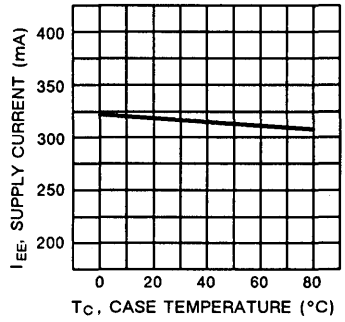


Fig. 10 – SUPPLY CURRENT vs SUPPLY VOLTAGE

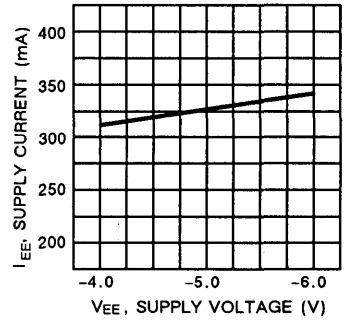


Fig. 11 – ADDRESS ACCESS TIME vs CASE TEMPERATURE

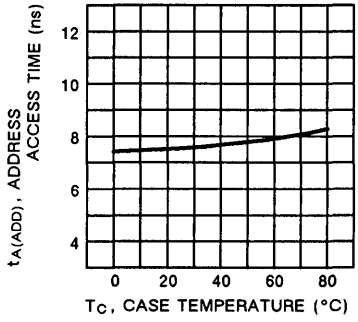


Fig. 12 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

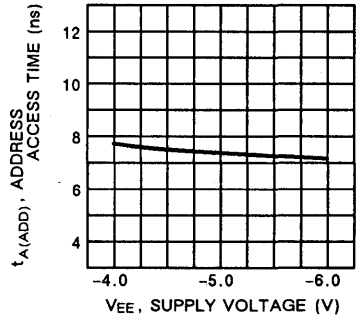


Fig. 13 – CLOCK ACCESS TIME vs CASE TEMPERATURE

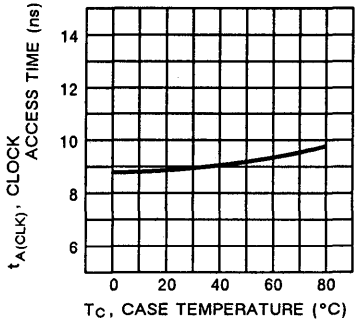


Fig. 14 CLOCK ACCESS TIME vs SUPPLY VOLTAGE

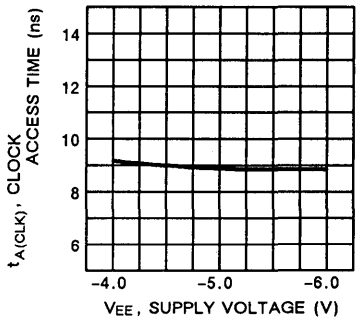


Fig. 15 - OUTPUT DELAY TIME vs CASE TEMPERATURE

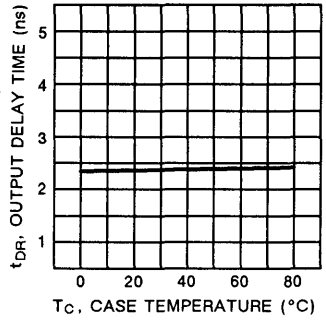


Fig. 16 - OUTPUT DELAY TIME vs SUPPLY VOLTAGE

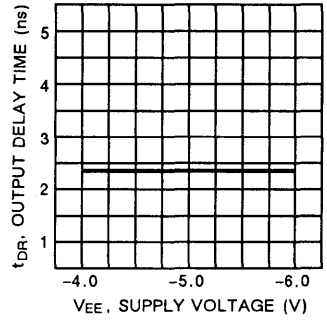


Fig. 17 - CLOCK PULSE WIDTH HIGH vs CASE TEMPERATURE

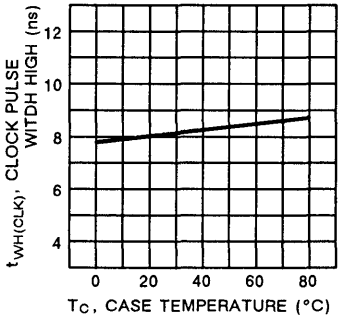
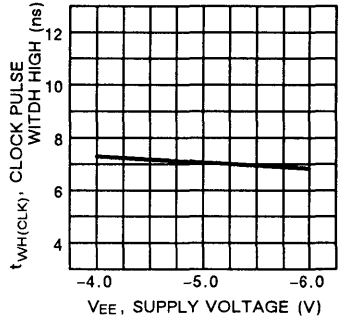


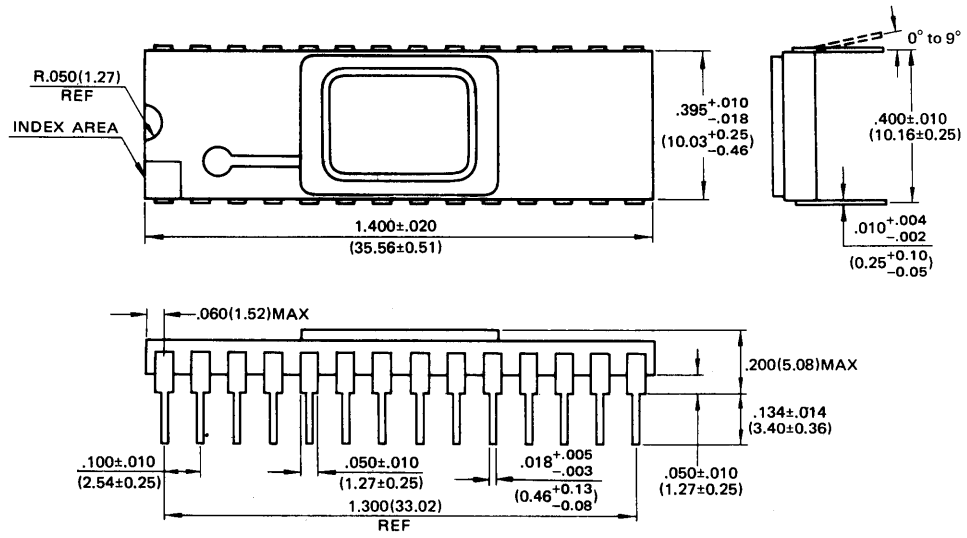
Fig. 18 - CLOCK PULSE WIDTH HIGH vs SUPPLY VOLTAGE



3

PACKAGE DIMENSIONS

28-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-A06)



Dimensions in
inches and (millimeters)

FUJITSU

ECL 16384 BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100486RR-13

Nobember, 1988
Edition 1.0

ADVANCE INFORMATION

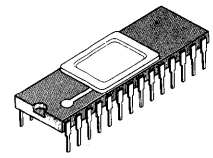
16384-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

The Fujitsu MBM100486RR-13 is fully decoded 16384-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with registered inputs and outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register circuits allows to decrease the number of device on the board.

Operation for the MBM100486RR is specified over a case temperature range of from 0°C to 85°C (T_C). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.

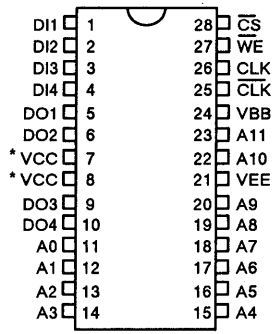
- 4096 words by 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 13ns
  Output delay time : 3ns
- Power dissipation : 1800mW max
- Open emitter output for ease of memory expansion
- Edge triggered registers for inputs and outputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and IOP-II processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

3

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} ground

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under bias	T_C	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

FUJITSU

ECL 16384 BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

MBM100486RL-13

Nobember, 1988
Edition 1.0

ADVANCE INFORMATION

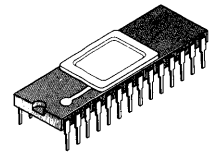
16384-BIT BIPOLAR SELF-TIMED RANDOM ACCESS MEMORY

The Fujitsu MBM100486RL-13 is fully decoded 16384-bit ECL self-timed read/write random access memory (STRAM). The device is organized as 4096 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The STRAM with registered inputs and latched outputs are fully synchronous to the external clock signal. Write operation is initiated by internal write pulse generator, which is driven by the clock signal given through the CLK ($\overline{CLK}$) pin and external control of write cycle timing is not necessary. Compared to the traditional RAM, STRAM drastically improves the system level cycle time because signal skews are not necessarily concerned. Also embedded register/latch circuits allows to decrease the number of device on the board.

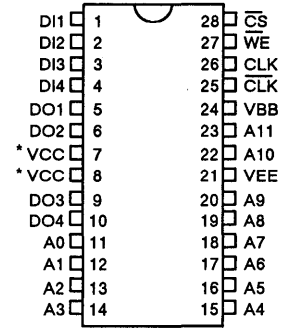
Operation for the MBM100486RL is specified over a case temperature range of from 0°C to 85°C (Tc). It is packaged in 28-pin ceramic side brazed DIP and fully compatible with industry standard 100K-series ECL families.

- 4096 words by 4 bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industory standrad 100K series ECL families
- Cycle time : 13ns
  Output delay time : 3ns
- Power dissipation : 1800mW max
- Open emitter output for ease of memory expansion
- Level-sensitive D-type latch for output and edge triggered registers for inputs
- Internal write pulse generator
- Optional clock inputs : single ended or differential
- DOPOS and IOP-II processing
- 28-pin ceramic side-brazed DIP (Suffix: C)



CERAMIC PACKAGE
DIP-28C-A06

PIN ASSIGNMENT
(TOP VIEW)



* V_{CC} ground

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature under bias	Tc	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Small geometry bipolar IC is occasionally susceptible to be damaged from static voltage or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this device.

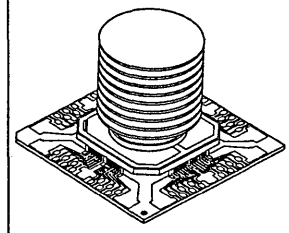
FUJITSU

MB7700H SERIES ECL BIPOLAR RANDAM ACCESS MEMORY

November 1988

The Fujitsu MB7700H series are ECL 4096-bit read/write randam access memories designed for applications of high-speed scratch pad, control and buffer storage. This device consists of 256 words x 4 bits memory array. By means of the metal options, several kinds of organization for various usages within a system are realized. (e.g. 256 words x 16 bits, 512 words x 8 bits and so on.)

The MB7700H series offers extremely small cell size realized through the use of IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time is achieved.



FPT-60C-A06

- 256 words x 16 bits organization (basic)
- On-chip voltage compensation for improved noise margin
- Fully compatible with 10K ECL families
- Address access time : 5 ns max.
  : 4 ns typ.
- Power dissipation : 6.0 W max.
  : 3.6 W typ.
- Open emitter output for ease of memory expansion
- 60 Pin FLAT package

PIN ASSIGNMENT

See page : 6 to 9

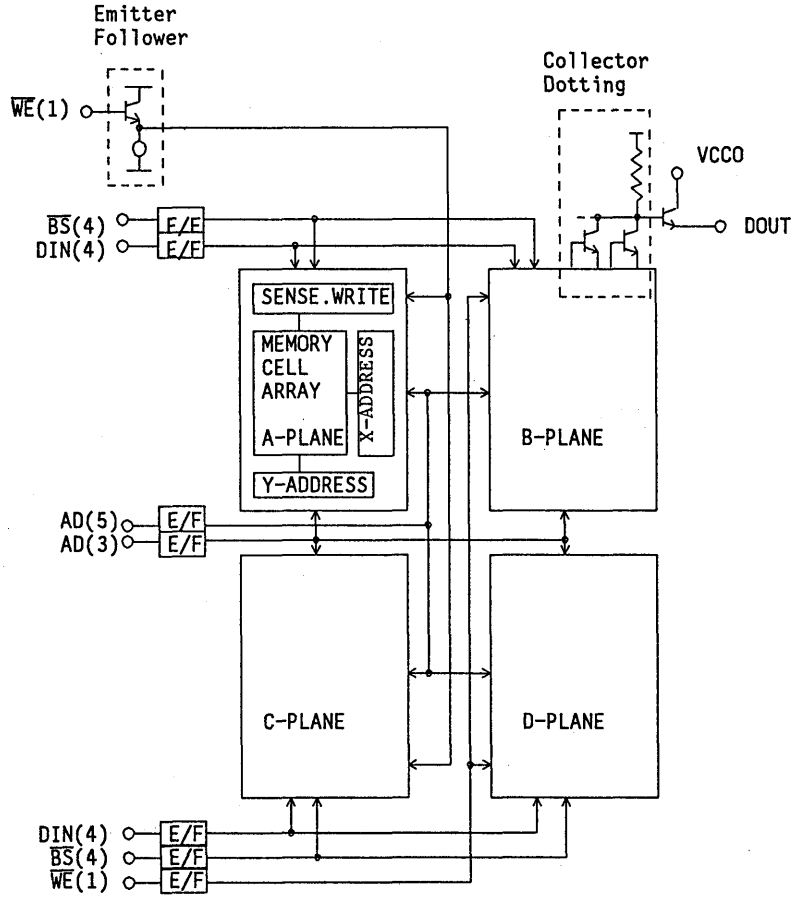
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
VEE1 Pin Potential to Ground Pin(VCC)	VEE1	+0.5 to -7.0	V
VEE2 Pin Potential to Ground Pin(VCC)	VEE2	+0.5 to -7.0	V
Input Voltage	VIN	+0.5 to VEE	V
Output Current (DC, Output High)	IOUT	-30	mA
Temperature under Bias	TA	-25 to 100	°C
Storage Temprature	TSTG	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

Fig.1 – MB7700H SERIES BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{BS}$	$\overline{WE}$	DIN		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	DOUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't care

GUARANTEED OPERATING CONDITIONS
(Referenced to VCC)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VEE1	-3.78	-3.60	-3.42	V
Supply Voltage	VEE2	-5.46	-5.20	-4.94	V
Operating Temprature	TA	0		55	°C

DC CHARACTERISTICS
MB7701H / MB7702H / MB7703H / MB7704H / MB7705H / MB7706H
VCC = VCCO = 0 V, VEE1 = -3.6 V, VEE2 = -5.2 V
Output Load = 50 Ohm to -2.0 V, Airflow ≥ 5m/s, unless otherwise noticed.

Parameter		Symbol	Min	Typ	Max	Unit	TA
Output High Voltage (VIN = VIH max or VIL min)		VOH	-1000 -960 -925		-840 -810 -755	mV	0°C 25°C 55°C
Output Low Voltage (VIN = VIH max or VIL min)		VOL	-1870 -1850 -1840		-1630 -1615 -1600	mV	0°C 25°C 55°C
Output High Voltage (VIN = VIH min or VIL max)		VOHC	-1020 -980 -945			mV	0°C 25°C 55°C
Output Low Voltage (VIN = VIH min or VIL max)		VOLC			-1610 -1595 -1580	mV	0°C 25°C 55°C
Input High Voltage		VIH	-1145 -1105 -1070		-840 -810 -755	mV	0°C 25°C 55°C
Input Low Voltage		VIL	-1870 -1850 -1840		-1490 -1475 -1460	mV	0°C 25°C 55°C
Input High Current (VIN = VIH max)	Address	IIH(A)			220	µA	0°Cto55°C
	Data In	IIH(DI)			220	µA	
	Write Enable	IIH(WE)			220	µA	
	Block Select	IIH(BS)			220	µA	
Input Low Current (VIN = VIL min)	Address	IIL(A)			170	µA	0°Cto55°C
	Data In	IIL(DI)			170	µA	
	Write Enable	IIL(WE)			170	µA	
	Block Select	IIL(BS)	0.5		170	µA	
Power Supply Current		IEE1	-480			mA	0°Cto55°C
Power Supply Current		IEE2	-800			mA	0°Cto55°C

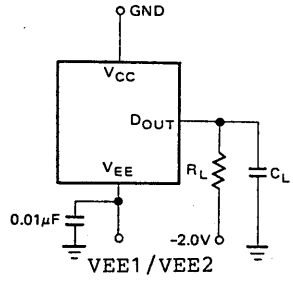
CAPACITANCE

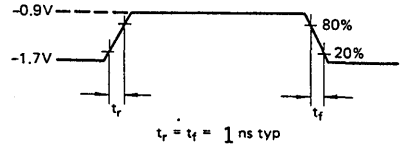
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	CIN			6.5	pF
Output Capacitance	COUT			8.0	pF

AC CHARACTERISTICS

(VCC=VCCO=0V, VEE1=−3.6V±5%, VEE2=−5.2V±5%, Output Load=50Ω to −2.0V and 10pF to GND, TC = 0°C to 55°C. Airflow ≥ 5m/s , unless otherwise noticed.)

Fig. 2 – AC TEST CONDITIONS





Output Load: R_L = 50Ω
C_L = 10pF
(including jig and stray capacitance)

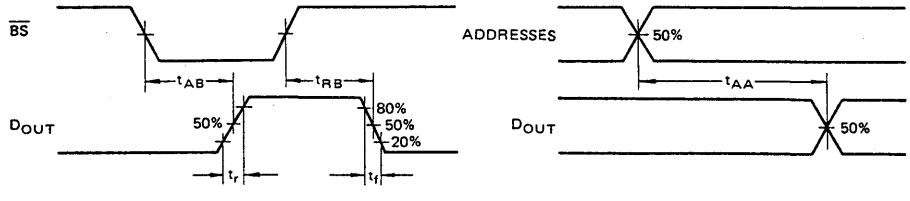
NOTE: All timing measurements referenced to 50% input levels.

3

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	tAA	1.5		5.0	ns
Block Select Access Time	tAB	0.5		3.0	ns
Block Select Recovery Time	tRB	0.5		3.0	ns

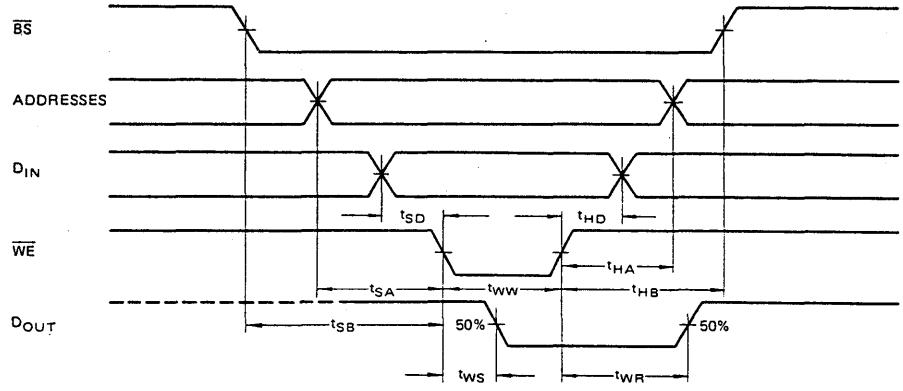
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pluse Width	tWW	3.5			ns
Address Set Up Time	tSA	1.5			ns
Block Select Set Up Time	tSB	1.5			ns
Data Set Up Time	tSD	0.5			ns
Address Hold Time	tHA	1.5			ns
Block Select Hold Time	tHB	1.5			ns
Data Hold Time	tHD	2.5			ns
Write Disable Time	tWS			4.0	ns
Write Recovery Time	tWR			4.0	ns

WRITE CYCLE TIMING DIAGRAM

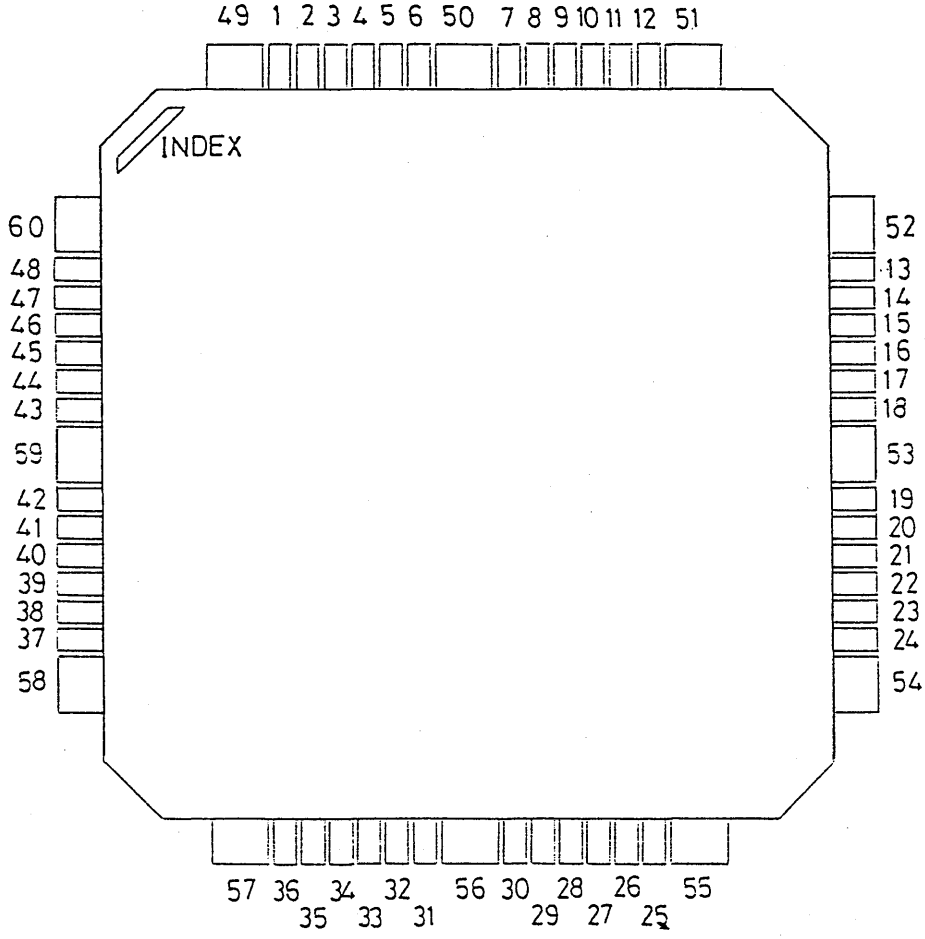


RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.0		ns
Output Fall Time	t_f		1.0		ns

PIN NUMBER ASSIGNMENT

TOP VIEW



PIN ASSIGNMENT

Part No. Pin No.	7701H	7702H	7703H	7704H	7705H	7706H
1	DO_{23}.a	DO_3.a	DO_3.a	DO_3.a	DO_3.a	DO_0.ac
2	DO_{01}.a	DO_2.a	DO_2.a	DO_2.a	DO_2.a	DO_1.ac
3	A_0	A_0	A_0	A_0.ab	A_0	A_0.ab
4	A_1	A_1	A_1	A_1.ab	A_1	A_1.ab
5	A_2	A_2	A_2	A_2.ab	A_2	A_2
6	A_3	A_3	A_3	A_3.ab	A_3	A_3
7	DO_{01}.b	DO_0.b	DO_0.b	DO_0.b	DO_0.b	DI_0.ab
8	DO_{23}.b	DO_1.b	DO_1.b	DO_1.b	DO_1.b	DI_1.ab
9	DI_0.b	DO_2.b	DO_2.b	DO_2.b	DO_2.b	DI_2.ab
10	DI_1.b	DO_3.b	DO_3.b	DO_3.b	DO_3.b	DI_3.ab
11	A_4	A_4	A_4	A_4.ab	A_4	A_4
12	A_5	A_5	A_5	A_5.ab	A_5	A_5
13	A_6	A_6	A_6	A_6.ab	A_6	A_6
14	A_7	A_7	A_7	A_7.ab	A_7	A_7
15	DI_2.b	DI_1.ab	DI_1.b	DI_1.ab	DI.b	----
16	DI_3.b	DI_0.ab	DI_0.b	DI_0.ab	$\overline{BS}_3$	$\overline{BS}_0$.ab
17	----	----	$\overline{BS}$.b	$\overline{BS}$.b	$\overline{BS}_2$	$\overline{BS}_1$.ab
18	$\overline{WE}$.b	$\overline{WE}$.bd	$\overline{WE}$.ab	$\overline{WE}$.ab	$\overline{WE}$.b	$\overline{WE}$.bd
19	$\overline{WE}$.d	$\overline{BS}$.cd	$\overline{BS}$.d	$\overline{BS}$.d	$\overline{WE}$.d	----
20	----	----	----	----	----	$\overline{BS}_3$.cd
21	$\overline{BS}_2$	DI_3.cd	DI_3.b	DI_3.cd	----	$\overline{BS}_2$.cd
22	$\overline{BS}_1$	DI_2.cd	DI_2.b	DI_2.cd	DI.d	----
23	----	DO_1.d	DO_1.d	DO_1.d	DO_1.d	DO_3.bd
24	----	DO_0.d	DO_0.d	DO_0.d	DO_0.d	DO_2.bd
25	DO_{23}.d	DO_3.d	DO_3.d	DO_3.d	DO_3.d	DO_0.bd
26	DO_{01}.d	DO_2.d	DO_2.d	DO_2.d	DO_2.d	DO_1.bd
27	DI_3.d	----	DI_1.d	A_0.cd	----	A_0.cd

Part No. Pin No.	7701H	7702H	7703H	7704H	7705H	7706H
28	$DI_{2.d}$	----	$DI_{0.d}$	$A_{1.cd}$	----	$A_{1.cd}$
29	$DI_{1.d}$	----	$DI_{2.d}$	$A_{2.cd}$	----	----
30	$DI_{0.d}$	----	$DI_{3.d}$	$A_{3.cd}$	----	----
31	$DO_{01.C}$	$DO_{0.c}$	$DO_{0.c}$	$DO_{0.c}$	$DO_{0.c}$	$DI_{0.cd}$
32	$DO_{23.c}$	$DO_{1.c}$	$DO_{1.c}$	$DO_{1.c}$	$DO_{1.c}$	$DI_{1.cd}$
33	$DI_{0.c}$	$DO_{2.c}$	$DO_{2.c}$	$DO_{2.c}$	$DO_{2.c}$	$DI_{2.cd}$
34	$DI_{1.c}$	$DO_{3.c}$	$DO_{3.c}$	$DO_{3.c}$	$DO_{3.c}$	$DI_{3.cd}$
35	----	----	$DI_{2.c}$	$A_{4.cd}$	----	----
36	----	----	$DI_{3.c}$	$A_{5.cd}$	----	----
37	$DI_{3.C}$	----	$DI_{1.c}$	$A_{6.cd}$	----	----
38	$DI_{2.c}$	----	$DI_{0.c}$	$A_{7.cd}$	----	----
39	$\overline{BS}_3$	$DI_{1.cd}$	$DI_{3.a}$	$DI_{1.cd}$	DI.c	----
40	$\overline{BS}_0$	$DI_{0.cd}$	$DI_{2.a}$	$DI_{0.cd}$	$\overline{BS}_0$	$\overline{BS}_{0.cd}$
41	----	----	$\overline{BS}_{.c}$	$\overline{BS}_{.c}$	$\overline{BS}_1$	$\overline{BS}_{1.cd}$
42	$\overline{WE}_{.c}$	$\overline{WE}_{.ac}$	$\overline{WE}_{.cd}$	$\overline{WE}_{.cd}$	$\overline{WE}_{.c}$	$\overline{WE}_{.ac}$
43	$\overline{WE}_{.a}$	$\overline{BS}_{.ab}$	$\overline{BS}_{.a}$	$\overline{BS}_{.a}$	$\overline{WE}_{.a}$	----
44	----	----	----	----	----	$\overline{BS}_{3.ab}$
45	$DI_{0.a}$	$DI_{3.ab}$	$DI_{0.a}$	$DI_{3.ab}$	----	$\overline{BS}_{2.ab}$
46	$DI_{1.a}$	$DI_{2.ab}$	$DI_{1.a}$	$DI_{2.ab}$	DI.a	----
47	$DI_{2.a}$	$DO_{1.a}$	$DO_{1.a}$	$DO_{1.a}$	$DO_{1.a}$	$DO_{3.ac}$
48	$DI_{3.a}$	$DO_{0.a}$	$DO_{0.a}$	$DO_{0.a}$	$DO_{0.a}$	$DO_{2.ac}$
49	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$	$VCC_{.a}$
50	VCCO	VCCO	VCCO	VCCO	VCCO	VCCO
51	VCC	VCC	VCC	VCC	VCC	VCC
52	VEE2	VEE2	VEE2	VEE2	VEE2	VEE2

Part No. Pin No.	7701H	7702H	7703H	7704H	7705H	7706H
53	VEE1	VEE1	VEE1	VEE1	VEE1	VEE1
54	VEE2	VEE2	VEE2	VEE2	VEE2	VEE2
55	VCC	VCC	VCC	VCC	VCC	VCC
56	VCCO	VCCO	VCCO	VCCO	VCCO	VCCO
57	VCC	VCC	VCC	VCC	VCC	VCC
58	VEE2	VEE2	VEE2	VEE2	VEE2	VEE2
59	VEE1	VEE1	VEE1	VEE1	VEE1	VEE1
60	VEE2	VEE2	VEE2	VEE2	VEE2	VEE2

VCC = VCCO = 0 V , VEE1 = -3.6 V , VEE2 = -5.2 V

NOTE) Pin name definition

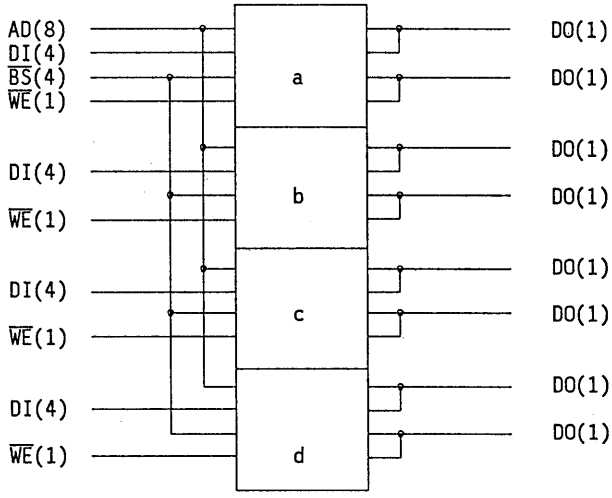
$DO_{1}.a$
- Plane location
- Terminal name of plane

$DO_{12}.a$
- DO_1, DO_2 dot (between terminals in a plane)

$DO_{1}.ab$
- Plane "a" , plane "b" dot (between planes)

---- Non connection

INTERNAL PLANE CONNECTION DIAGRAM FOR MB7701H

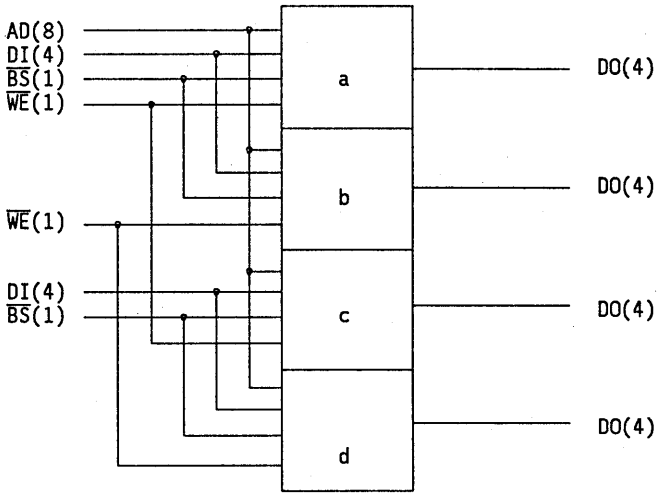


Note :

1) Values in ( ) show the number of external pins having the same pin name.

2) "a" , "b" , "c" and "d" in the boxes show four memory planes in a chip.

INTERNAL PLANE CONNECTION DIAGRAM FOR MB7702H

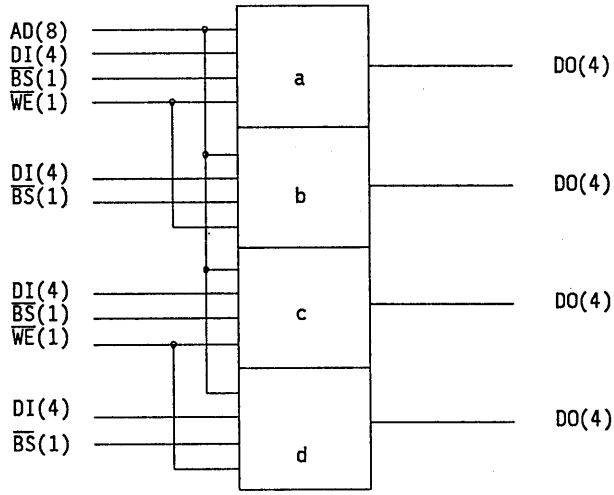


Note :

1) Values in ( ) show the number of external pins having the same pin name.

2) "a" , "b" , "c" and "d" in the boxes show four memory planes in a chip.

INTERNAL PLANE CONNECTION DIAGRAM FOR MB7703H

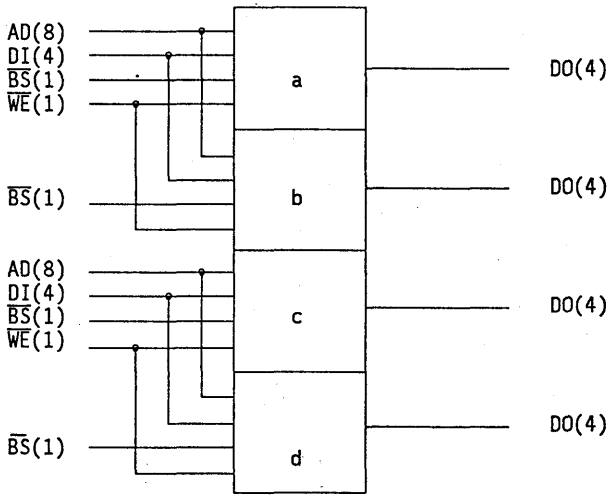


Note :

1) Values in ( ) show the number of external pins having the same pin name.

2) "a" , "b" , "c" and "d" in the boxes show four memory planes in a chip.

INTERNAL PLANE CONNECTION DIAGRAM FOR MB7704H

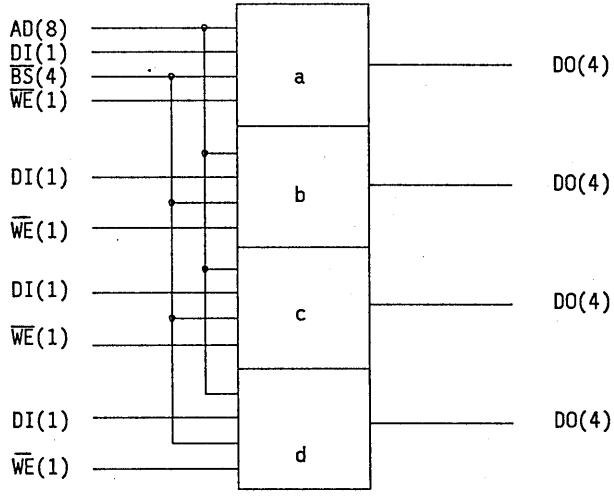


Note :

1) Values in ( ) show the number of external pins having the same pin name.

2) "a" , "b" , "c" and "d" in the boxes show four memory planes in a chip.

INTERNAL PLANE CONNECTION DIAGRAM FOR MB7705H

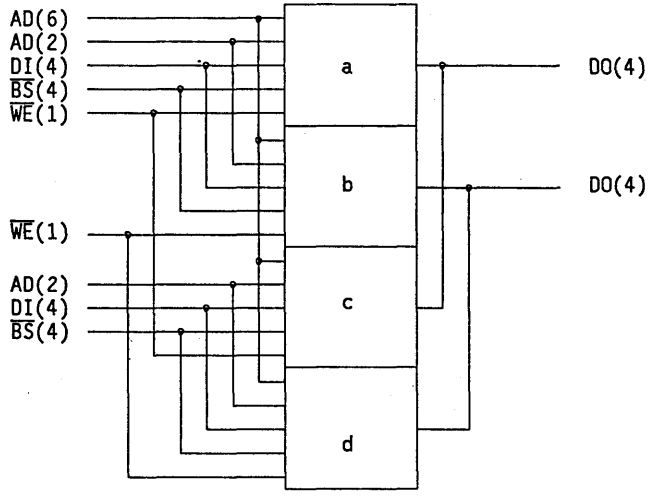


Note :

1) Values in ( ) show the number of external pins having the same pin name.

2) "a" , "b" , "c" and "d" in the boxes show four memory planes in a chip.

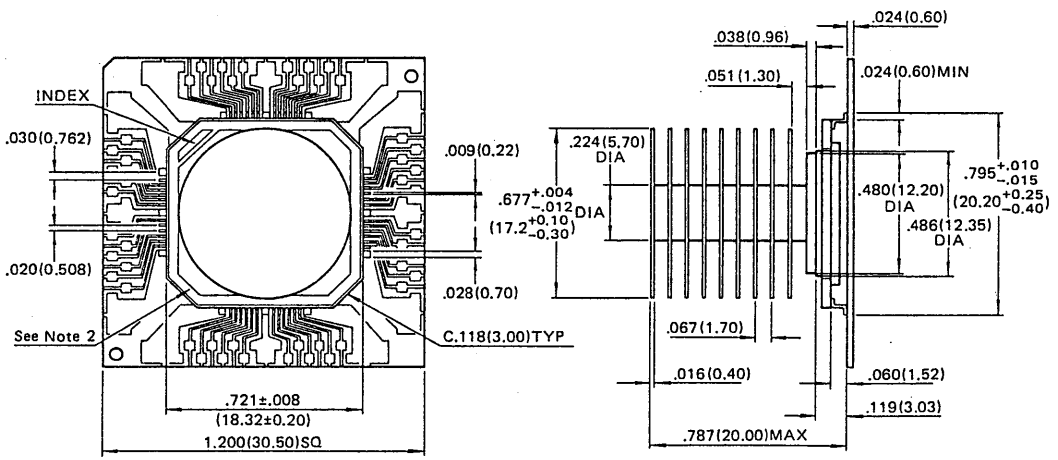
INTERNAL PLANE CONNECTION DIAGRAM FOR MB7706H



Note :
1) Values in ( ) show the number of external pins having the same pin name.

2) "a" , "b" , "c" and "d" in the boxes show four memory planes in a chip.

60-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(CASE NO.: FPT-60C-A01)



Notes:
1. Cooling fin center is within .020(0.50)
2. Bottom pattern of ceramic base is connected to V_{CC}.

Dimensions in inches (millimeters)

Section 4

Programmable ROMs

Page	Device	Maximum Access Time(ns)	Capacity	Package Options
4-47	MB7111E/H/L MB7112E/H/Y/L	35/25/50 35/25/20/50	256 bits (32w x 8b)	16-pin Ceramic DIP 16-pin Plastic DIP 16-pin Plastic FPT
4-67	MB7113E/L MB7114E/H/L	40/50 40/30/50	1024 bits (256w x 4b)	16-pin Ceramic DIP 16-pin Plastic DIP 16-pin Plastic FPT
4-87	MB7115E/H/L MB7116E/H/Y/L	45/35/60 45/35/30/60	2048 bits (512w x 4b)	16-pin Ceramic DIP 16-pin Plastic DIP 20-pad Ceramic LCC
4-103	MB7117E/H/L MB7118E/H/L	45/35/60 45/35/60	2048 bits (256w x 8b)	20-pin Ceramic DIP 20-pin Plastic DIP 20-pin Plastic FPT 20-pad Ceramic LCC
4-119	MB7121E/H/L MB7122E/H/Y/L	45/35/60 45/35/30/60	4096 bits (1024w x 4b)	18-pin Ceramic DIP 18-pin Plastic DIP 20-pad Ceramic LCC
4-135	MB7123E/H/L MB7124E/H/Y/L	45/35/60 45/35/30/60	4096 bits (512w x 8b)	20-pin Ceramic DIP 20-pin Plastic DIP 20-pin Plastic FPT 20-pad Ceramic LCC
4-151	MB7127E/H/L MB7128E/H/Y/L	55/45/70 55/45/35/70	8192 bits (2048w x 4b)	18-pin Ceramic DIP 18-pin Plastic DIP 18-pad Ceramic LCC
4-167	MB7131E/H/L/-SK MB7132E/H/Y/L/-SK	55/45/70 55/45/35/70	8192 bits (1024w x 8b)	24-pin Ceramic DIP 24-pin Ceramic SKDIP 24-pin Plastic DIP 24-pin Ceramic FPT 28-pad Ceramic LCC
4-183	MB7133E/H MB7134E/H/Y	55/45 55/45/35	16384 bits (4096w x 4b)	20-pin Ceramic DIP 28-pad Ceramic LCC

Programmable ROMs

(Continued)

Page	Device	Maximum Access Time(ns)	Capacity	Package Options
4-199	MB7137E/H/-SK	55/45	16384 bits	24-pin Ceramic SKDIP
	MB7138E/H/Y/-SK	55/45/35	(2048w x 8b)	24-pin Ceramic DIP
				24-pin Plastic DIP
				24-pin Ceramic FPT
				28-pad Ceramic LCC
4-215	MB7142E/H	65/55	32768 bits	24-pin Ceramic DIP
			(4096w x 8b)	24-pin Ceramic FPT
				28-pad Ceramic LCC
4-231	MB7144E/H	65/55	65536 bits	24-pin Ceramic DIP
			(8192w x 8b)	24-pin Ceramic FPT
				28-pad Ceramic LCC
4-247	MB7151E/H	55/45	16384 bits	20-pin Ceramic DIP
	MB7152E/H/Y	55/45/35	(4096w x 4b)	20-pin Plastic DIP
4-263	MB71A38-25	25	16384 bits	24-pin Ceramic DIP
	MB71A38-35	35	(2048w x 8b)	24-pin Plastic DIP
				24-pin Ceramic SKDIP
				24-pin Plastic SKDIP
4-277	MB71C44-35	35	65535 bits	24-pin Ceramic DIP
	MB71C44-45	45	(8192w x 8b)	24-pin Ceramic SKDIP
				24-pin Plastic DIP
				24-pin Plastic SKDIP
				24-pin Ceramic FPT
				28-pad Ceramic LCC
4-293	MB71C46-35	35	131072 bits	28-pin Ceramic DIP
	MB71C46-45	45	(16384w x 8b)	28-pin Plastic DIP
4-307	MB7226RA-20/-25/-25W	20/25/25	4096 bits	24-pin Ceramic DIP
	MB7226RA-20L/-25L/-25LW	20/25/25	(512w x 8b)	24-pin Ceramic FPT
	MB7226RS-20/-25/-25W	20/25/25		28-pad Ceramic LCC
4-323	MB7232RA-20/-25/-25W	20/25/25	8192 bits	24-pin Ceramic DIP
	MB7232RS-20/-25/-25W	20/25/25	(1024w x 8b)	24-pin Ceramic FPT
				28-pad Ceramic LCC
4-339	MB7238RA-20/-25/-25W	20/25/25	16384 bits	24-pin Ceramic DIP
	MB7238RS-20/-25/-25W	20/25/25	(2048w x 8b)	24-pin Ceramic FPT
				28-pad Ceramic LCC

FUJITSU

Registered PROMs
A Solution to High Speed
Digital Design

Application
Note

May 1988
Edition 1.0

Registered PROMs
A Solution to High Speed Digital Design

by Mohammad Shakaib Iqbal

Fujitsu Microelectronics, Inc.

Publication Number OV0155-885F1

ABSTRACT

Programmable read only memories are widely used in digital systems. The applications vary from its use as a logic implementor to its classic application as instruction storage for microprogram control store and software for microprocessor programs.

A family of registered PROMs offer new savings for system designers. The registered PROM class features on chip, "D" type output registers which are useful for pipelined microprogrammable systems as well as for state machine implementations. The microinstruction in the microprogram control which is held in wide instruction registers can now be incorporated into the PROM chip. This feature saves power, improves the system cycle time and economizes board space over the past method of utilizing an external register.

This document covers the use of registered PROMs in computer architecture and many other practical system's applications.

TABLE OF CONTENTS

INTRODUCTION

In digital system design, whether it is microprogrammable computer architecture, state machine implementation, or simply a logic implementation, combining different devices in one single chip offers considerable advantage in terms of board space savings and speed enhancement.

THE REGISTERED PROM FAMILY: A Discussion on Architectures

PROMs, Programmable Read Only Memory architectures are preferable over the read only memories, because they can be programmed at the design site. PROMs come in various organization i.e. different depths and word widths.

Fujitsu offers a wide variety of the standard PROMs (MB7143/44 being the deepest in 8k x 8 configuration with access time of t_{AA} = 55ns). The smaller PROMs have faster access times.

A registered PROM is a programmable read only memory with registers on the outputs. Fujitsu offers 3 organizations of registered PROMs which will be discussed in detail later.

The focal point of this paper is to view the advantages as offered by the family of registered PROMs from Fujitsu.

THE APPLICATION ADVANTAGES

In most PROM applications, the read data has to be stored temporarily in an output register before it is used. This structure is particularly useful in microprogramming and state machine designs. Figure 1 shows the block diagram of the 1k x 8 registered PROM. Due to the presence of registers on the data outputs, the data read from the previous cycle can be held on the outputs during a new address access on the inputs of the PROM i.e. the pipelined effect. The outputs of the registers change only on the rising edge of the clock. This results in the simplified system timings and faster microcycles which will be discussed later.

The incorporation of the two building blocks, namely the PROMs and the registers, results in tremendous advantages such as, 2 to 1 reduction in chip count, saving the board real estate, reduction in overall power consumption, as there is only one device instead of two, which was the case in the original implementation. Also, as the output registers are internal to the chip, hence the delay from PROM output to the register input is not significant, which results in smaller overall delay. A major advantage which is not transparent to the designer is that the rest of the digital design is insulated from glitches (outputs of PROM bounce up and down, while the address propagates through the PROM array).

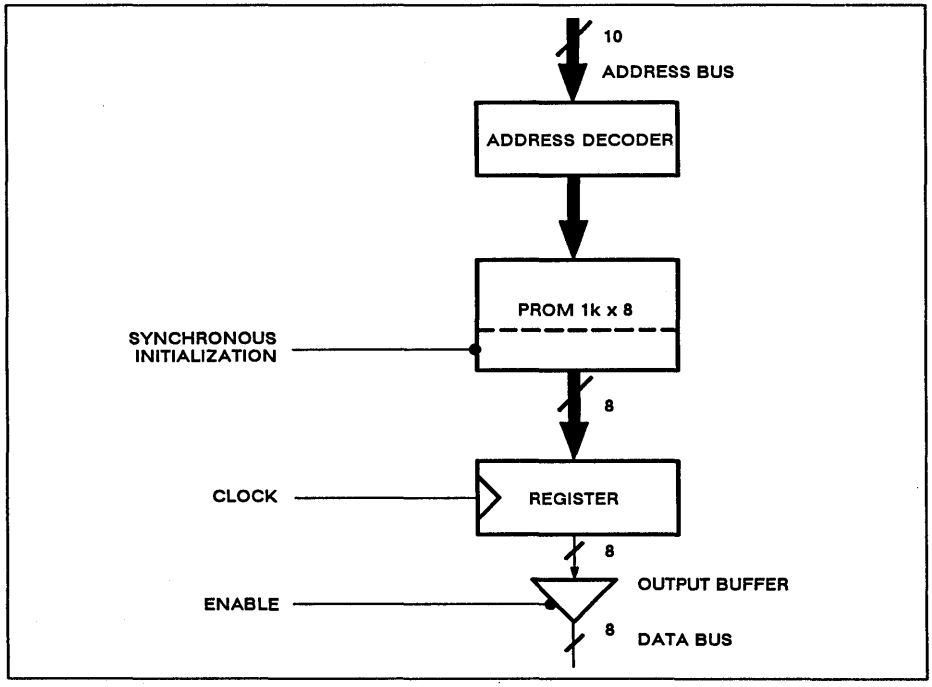


Figure 1. Typical Registered PROM Block Diagram

In microprogram control store without the use of an output register, there will be timing uncertainties for the rest of the system logic if the control word is not validated instantaneously.

THE FAMILY

Fujitsu offers six registered PROMS which are:

MB7226RA	512 x 8	asynchronous
MB7226RS	512 x 8	synchronous
MB7232RA	1k x 8	asynchronous
MB7232RS	1k x 8	synchronous
MB7238RA	2k x 8	asynchronous
MB7238RS	2k x 8	synchronous

These devices are available in industry standard 24 pin skinny dip (300 mil wide) packages as well as flat pack and LCC packages. The 4k x 8 will be announced in the future.

Objective specification provides a setup time from address to clock of 30ns and clock to output delay of 20ns.

The block diagrams of Fujitsu's 1k x 8 registered PROMs are shown in Figure 2.

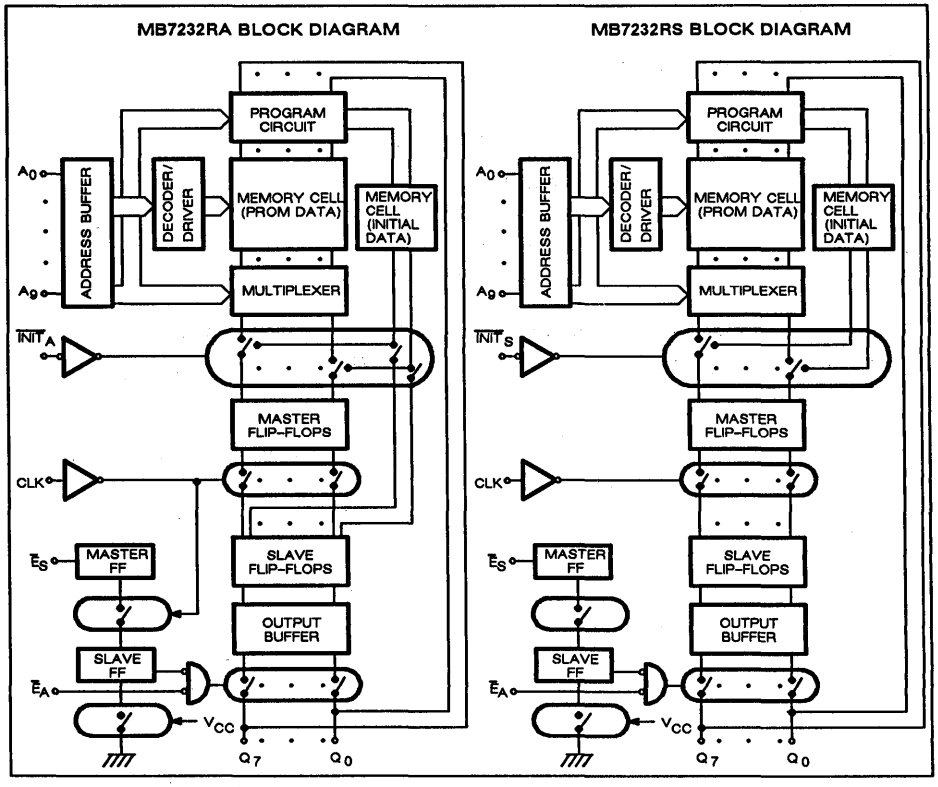


Figure 2. Block Diagrams of Fujitsu's 1k x 8 Registered PROMs

FEATURES:

Edge Triggered Registers

Data from the PROM is loaded into the output register (Q_7 – Q_0) on the rising edge of the clock. A register is made up of master-slave flip-flops. The data from PROM appears in the master register as soon as a new address is applied. At the next clock pulse, it is transferred to the slave register. (The chip enable should be low in order for the data to come out at the outputs (Q_7 – Q_0).) In short, the use of the register benefits the design with simplified and faster microcycles.

Synchronous and Asynchronous Enable

Fujitsu's registered PROMs are offered with both of these options. These PROMs come with two enable pins $\overline{E_A}$, the asynchronous enable and $\overline{E_S}$, the synchronous enable pin as shown in Figure 3. When $\overline{E_S}$ input = low, then pulling the $\overline{E_A}$ input low will enable the outputs immediately. Similarly, bringing $\overline{E_A}$ high immediately disables the outputs (Q_7 – Q_0). This enable option is useful for the cases when the outputs of the PROM are to be gated on the same type of bus. In such cases, the asynchronous enable ($\overline{E_A}$) option is used to allow direct control of the enable.

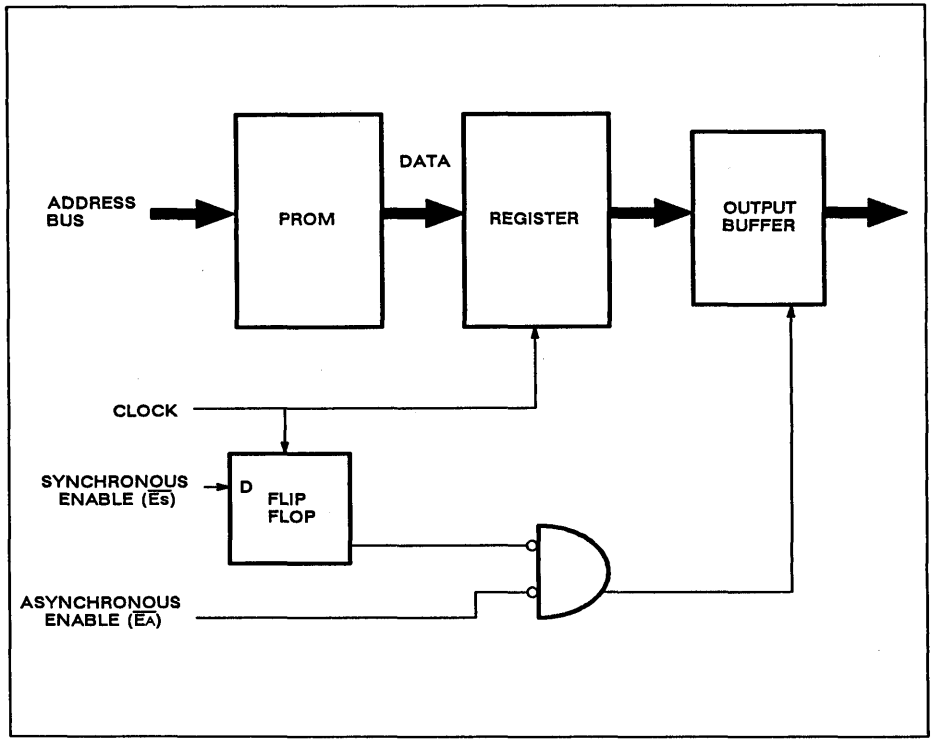


Figure 3. Synchronous & Asynchronous Enable

On the other hand, when it is desired to have a deeper PROM configuration, the synchronous enable ($\overline{ES}$) is used. In this case, the enable pin effectively becomes the most significant address bit, and hence, must be clocked in. Figure 4 shows the application of synchronous enable as the higher address bit.

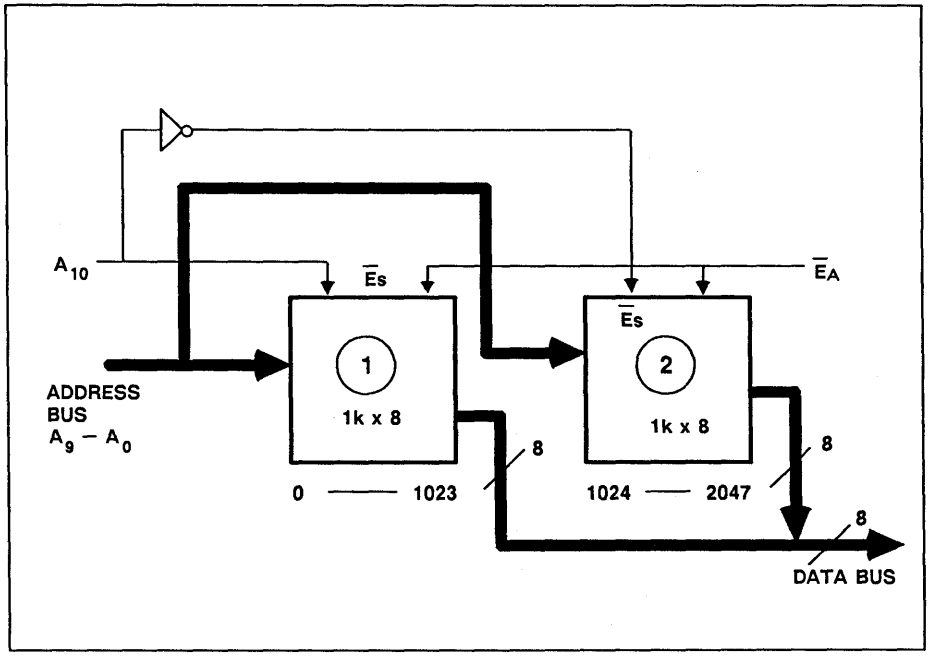


Figure 4. Application of Synchronous Enable ($\overline{ES}$) 2k x 8

NOTE: On the rising edge of the clock
$\overline{ES}$ = Low: Lower address are enable, i.e. 0 - 1023
$\overline{ES}$ = High: Higher addresses are enable, i.e. 1024 - 2047

Program Initialization

Available on:

MB7226RA/RS (512 x 8),
MB7232RA/RS (1k x 8) and
MB7238RA/RS (2k x 8).

The output of the register can be loaded by user-programmable initialization word. When INIT input is low, then the register is loaded with field programmable initial value. Each flip-flop in the output register may be individually programmed to either high state or low state.

In the MB7226RA, the INIT A = low is used to load both the master and the slave flip-flop immediately with the initial data, while for the MB7226RS, the initial data is loaded at the rising edge of the clock pulse.

This feature is a super set of preset and clear functions. Thus, programmable initialization can be used to generate any arbitrary microinstruction for system reset or interrupt. This feature is very useful in state machine applications to recover the initial state of the machine.

MAJOR APPLICATION AREAS

The following section will depict PROMs as memory element as well as a logic implementor in certain applications. The concept of microprogramming is discussed briefly here as the intent is to cover this topic in detail in a separate appnote, *Microprogrammed Architectures and Fujitsu's role in it.*

MEMORY DEVICE-CLASSIC APPLICATION (storage element)

Most of the digital systems prefer PROMs as an invaluable storage element. This is due to its advantages over the other options i.e. it is faster than EPROMs, and due to Bipolar technology, it does not require special handling (no ESD sensitivity, no sensitivity to radiation). They are also preferred over ROMs as they are portable i.e. programmable at user's site.

PROMs are used in data and control paths of a system to store constant data and firmware microprogram respectively. Both parts of a digital system can be viewed in Figure 5.

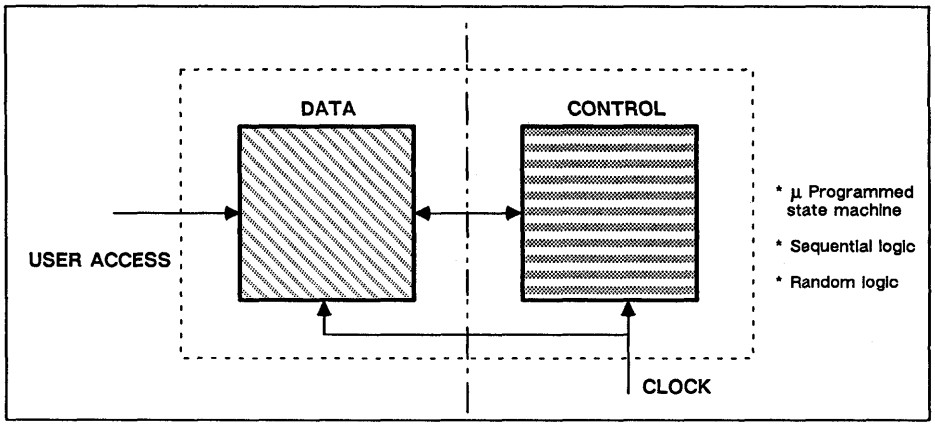


Figure 5. Typical Digital System Combination of Data and Control Parts

Data section is user accessible whereas the opposite is true for the control store. However, on currently available systems, control store is a combination of PROM and RAM, hence the privileged user can access and change the microcode.

In the data path area, PROMs are primarily used for applications like lookup tables. Data that is stored can be trigonometric functions; signal processing co-efficients, target identification, etc.

On the other hand, in control path applications, PROMs are mainly used for storing microprograms.

Microprogramming has become increasingly popular as a method of sequencing and control of states in a digital system. It provides a degree of flexibility which was not achievable in sophisticated processors and controllers. These Microprogrammed Controllers are most commonly used in computers, disk controllers, smart peripherals, video games, industrial control systems, etc.

As already stated, most memory applications of PROMs involve the PROM data being stored in a temporary register before it can be utilized. In all such applications, registered PROMs are preferable over other options. The following application examples utilizing registered PROMs as storing elements will further highlight this fact.

MICROPROGRAMMING AND MICROPROGRAM CONTROL STORE

In microprogammed systems, sequences of microinstructions stored in read only memory provide most of the system control. Each sequence has the basic steps to implement a particular system function. For example, if the system is a computer, then each sequence can execute a machine instruction. This is where PROM is used commonly. Many microprogram systems currently contain a writable portion of the control store which is implemented by random access memories, i.e. RAMs.

To have more insight in the registered PROM impact on microprogramming, let us first discuss what is the microprogram control store. A typical microprogrammable architecture is shown in Figure 6.

As already mentioned, each step of machine instruction fetch is controlled by micro instructions which are stored in the control store memory. In the simplistic form, when the machine instruction is fetched into the instruction register, a mapping function occurs which selects a control store address based upon the operation code of machine instruction. This address is the starting address of the microprogram in the control memory. With each machine cycle, a new micro instruction is fetched into the microinstruction register from the control store.

The address of the new microinstruction that has to be fetched depends upon three factors, namely, the address specified by the current microinstruction, the ALU status flags, and also the machine language instruction in the instruction register.

The microinstruction register (MIR) contains the state of the control unit generated signals. The logic block provides buffering or decoding of the control signals specified by the microinstruction in the MIR. A more detailed discussion on this will follow in a separate document as mentioned earlier.

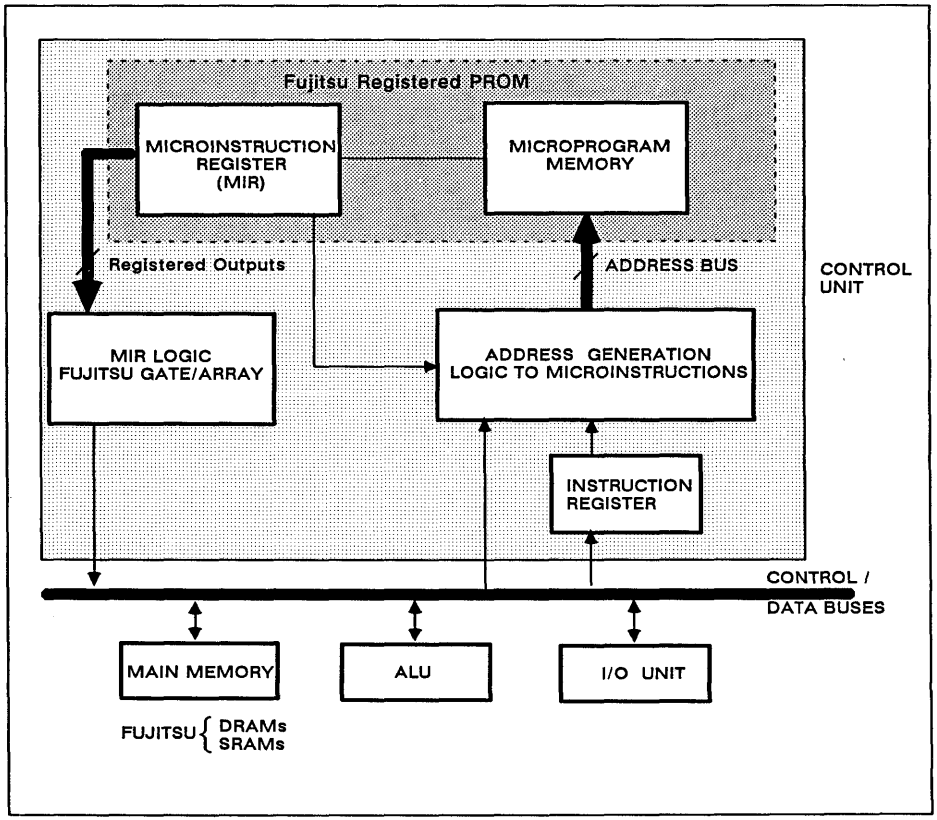


Figure 6. Typical Microprogrammable Architecture

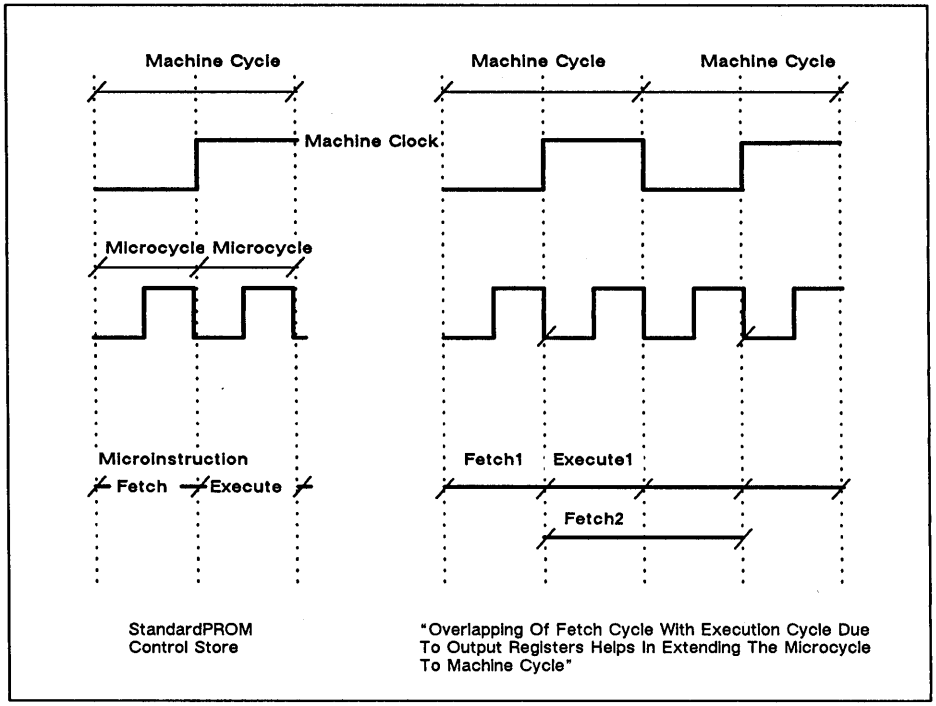


Figure 7. Overlapping of Fetch and Execution of Microinstruction Cycles

The same clock is used for the microinstruction address generator as well as the microinstruction register. The microinstruction register ensures that the bits change simultaneously after the clock pulse, and thus provide a pipelined effect, i.e. overlapping of fetch and execution of microinstruction cycles as shown in Figure 7. If the register is not used then the access to the control memory has to be completed in half of a machine cycle. For slow access speed of PROMs, the implementation requires longer machine cycles. Presence of register extends the fetch cycle to 1 machine cycle because of the separation of the control store outputs from the registered output. Using Fujitsu's Registered PROM devices helps not only in board space savings but also in achieving an enhanced performance over the standard PROM + Register implementation.

This can be extended to the implementation of pipelined CPU design with an onboard cache as shown in Figure 8.

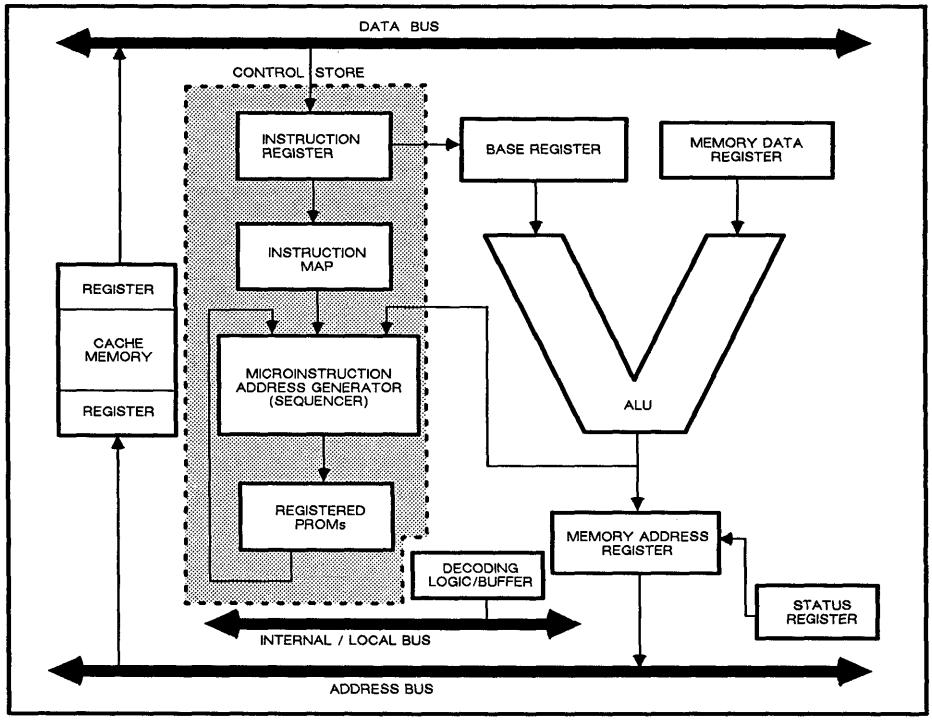


Figure 8. Block Diagram of a Complex Pipelined CPU Utilizing Registered PROMs

MICROCONTROLLER APPLICATION

Registered PROMs are also useful in implementing simple standalone microcontrollers which are powerful enough to control tape and disk drives, smart peripherals, etc.

A 2K word by 64-bit wide microcontroller can be constructed by using 16 MB7232RS devices. The Control logic can be implemented by using Fujitsu's Gate Array.

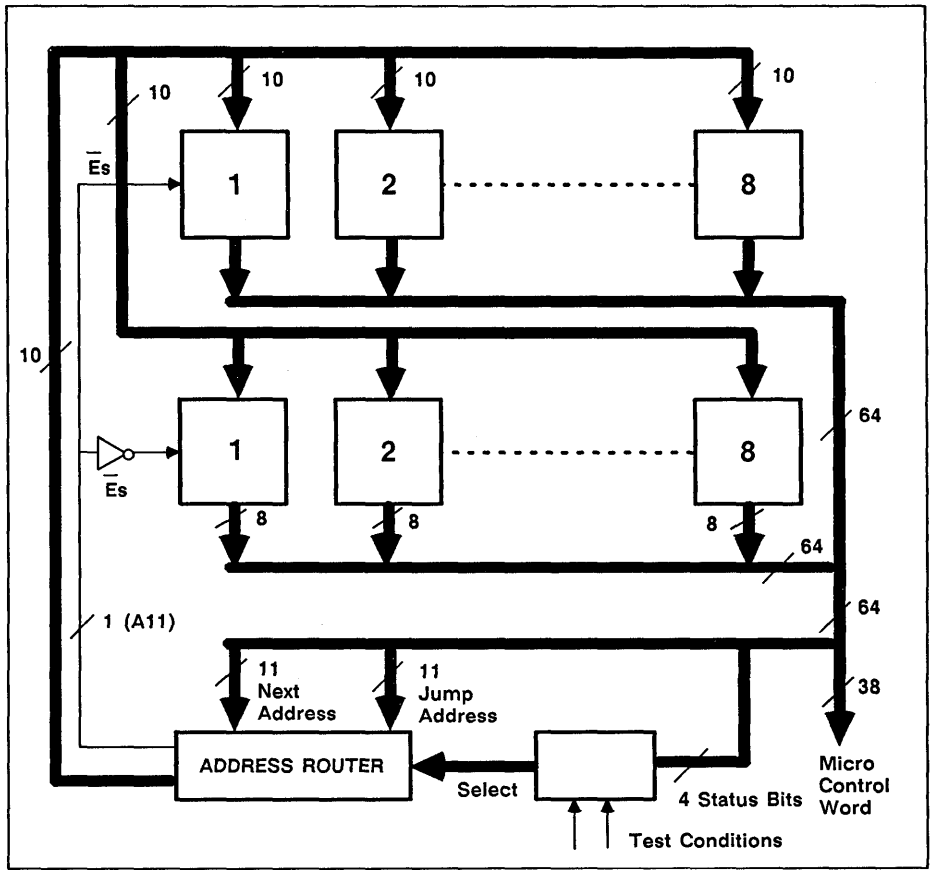


Figure 9. Typical Implementation of a Microcontroller

In this design registered PROMs are used to store the next address and the jump address. Note that still 2 inputs are left that are unused in these PROMs and can be used as control signals (3 x 8 – (11 + 11) = 2). Each PROM has 8 registered outputs which are sufficient to address 256 words of microprogram memory. As the MB72232RS is only 1K deep, hence two sets of 8 of these devices can be used to implement a 42-bit microcontroller. (Figure 9.)

The remaining 5 registered PROMs and the two unused bits can be employed to store 38-bit microcontrol word.

This word contains microcontrol signals which control various parts of the CPU and other external blocks such as main memory and I/O drivers. The 4 status bits select a status bit from the test conditions which will select jump or next address. This address is the address of the next microinstruction.

If this architecture is implemented using standard PROMs then the total cycle time to access 1 set of control signals (after the initial stage) will include:

$$t_{cycle} = t_{aa}(PROM) + t_{decision}$$

Where $t_{decision}$ is the time required to decode the test conditions with the status inputs to find out whether next address or jump address is required. The $t_{decision}$ can be decreased by performing the decision one cycle ahead. This can be done by using a registered PROM architecture. Besides the control path application, registered PROMs also find numerous applications in data path designs.

LOOKUP TABLE FOR IMAGE PROCESSING

One of the registered PROM applications in data path environment is to implement lookup tables, e.g. in image processing which involve restoration, enhancement and reproduction. A typical application is shown in Figure 10.

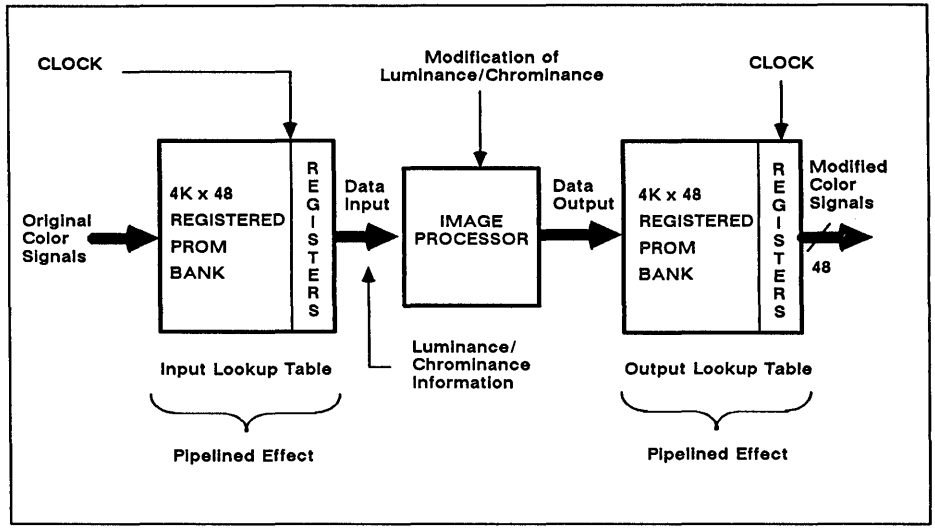


Figure 10. Lookup Table Application of Registered PROMs

In this application each image is transformed from one set of parameters to a second set. This is called homomorphic transformation. This transformation can be computed before hand and stored in a lookup table implemented by registered PROMs.

LOGIC IMPLEMENTATION BY USING REGISTERED PROMs

Any logic function can be expressed as a sum of product form or product sum form. The easiest way to implement a sum of product from is by an array of AND gates summed at an OR gate (see Figure 11). The number of inputs to the AND gates is dictated by the number of variables in the equation.

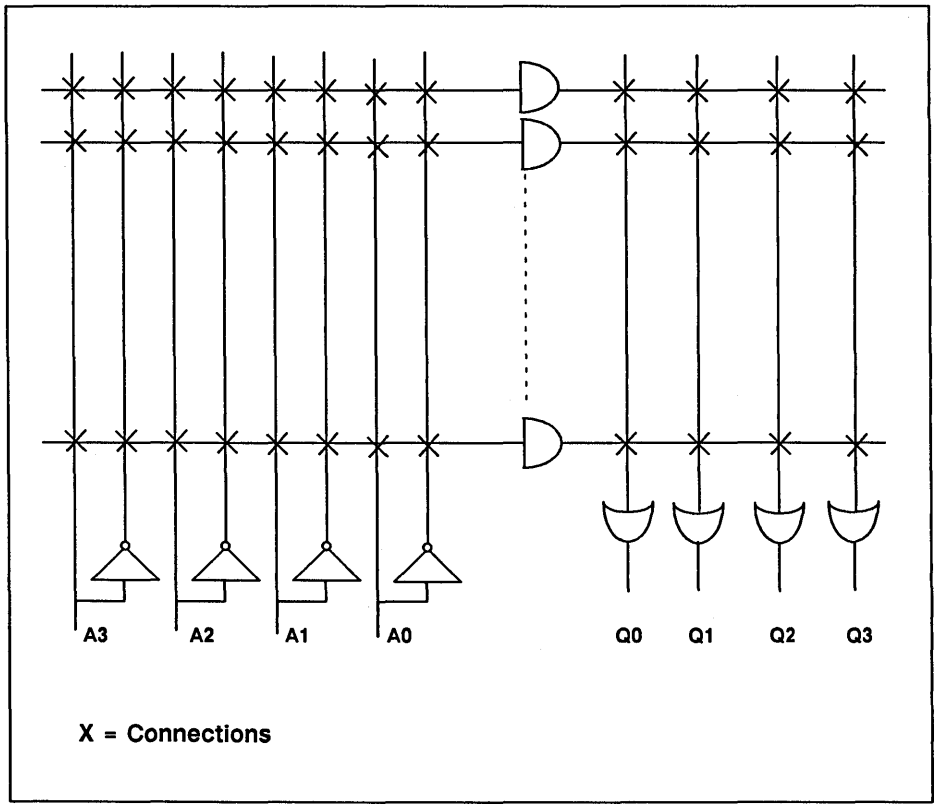


Figure 11. AND - OR Array

Each connection in Figure 11 can either be fixed or programmable. If all are programmable, it is known as Programmable Logic Array (PLA) with one disadvantage, i.e., complex programming software. Devices which have fixed OR gates and programmable AND gates are called Programmable Array Logic (PAL*). These devices are also not economical for applications requiring a large number of product terms, because of the requirement of large number of PAL devices.

In such cases, registered PROMs are used. PROMs have fixed AND arrays and programmable OR arrays, thus providing an abundance of product terms, i.e. = 2^n where "n" = number of inputs (each input has two states associated with it, thereby providing two product terms). Furthermore, when registered PROMs are used, the registers on outputs enhances overall system speed.

Besides being utilized in implementing control path logic, registered PROMs can also be used for data path logic implementation.

The following example shows an implementation of a complex function like Pseudo Number generation, using registered PROMs.

PSEUDO RANDOM NUMBER (PRN) GENERATOR

PRN sequences due to ease of their generation, enjoy a wide range of applications. Some of them are secure communication, radar ranging systems, encoding/decoding of information in signal processing, picture coding, waveform synchronization, etc. For secure communication, they are used for data encryption, while for data communication systems, they are used for error detection and correction.

PRN sequences can also be used as test vectors for circuit simulation. In radar range finding systems, PRN is used as signal modulators and as reference white noise in various DSP applications.

GENERATION OF PRN SEQUENCES

PRN sequences can be generated in many different ways. One of the most common implementations is by linear shift registers with feedback, as shown in Figure 12.

*MMI registered trademark

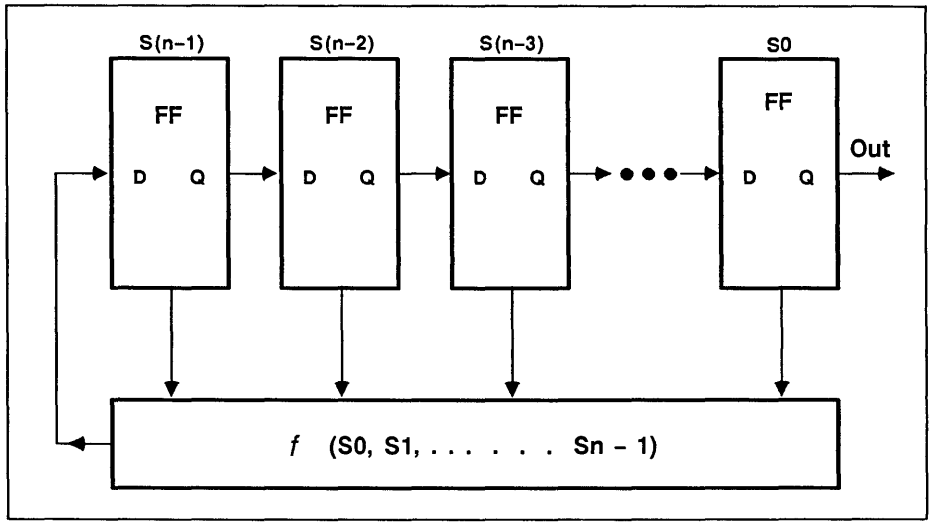


Figure 12. An "n" - Stage Shift Register With Feedback

4

Figure 12 depicts n-stages of linear shift register with some feedback function. For every clock cycle, all the information is shifted one position to the right with feedback term preventing the register from emptying.

Binary sequences with preassigned values can be obtained at the output by selecting a proper choice of stages in the shift register, the initial condition and the feedback function:

f (S0, S1, S2...S(n-1))

A linear shift register has the feedback function expressed as follows:

f (S0, S1, S2...S(n-1)) = Cn * S0 $\oplus$ Cn-1 * S1 $\oplus$ Cn-2...$\oplus$ C * S(n-1)

where C = Constant = either 0 or 1

$\oplus$ = addition modulo -2

An example of a 4-stage linear shift register is shown in Figure 12 for C1 = C2 = 0, C3 = C4 = 1. Feedback function is:

f (S0, S1, S2, S3) = C4 * S0 $\oplus$ C3 * S1 $\oplus$ C2 * S2 $\oplus$ C1 * S = S0 $\oplus$ S1

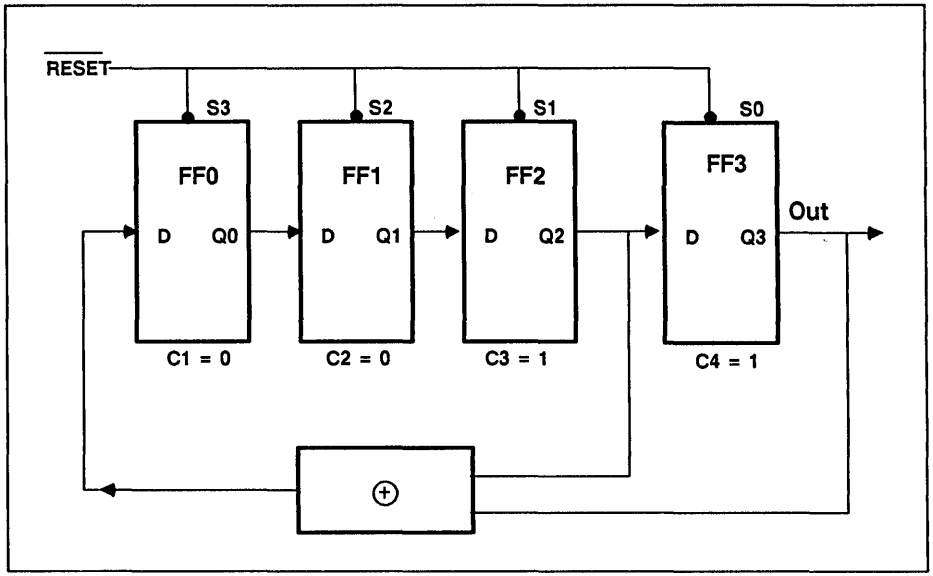


Figure 13. A Four-Stage Linear Shift Register With Feedback
f (SO, S1, S2, S3) = S1 ⊕ S0

Q0	Q1	Q2	Q3	
	STATES			
0	0	0	1	Initial State
1	0	0	0	
0	1	0	0	
0	0	1	0	
1	0	0	1	
1	1	0	0	
0	1	1	0	
1	0	1	1	
0	1	0	1	
1	0	1	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	
0	1	1	1	
0	0	1	1	
0	0	0	1	

OUT SEQUENCE 100010011010111 PERIOD = 15

The output sequence is periodic with a period "P" not exceeding 2^n. In the case of linear shift-register, the period is $P = 2^n - 1$. A sequence with a $P = 2^n - 1$ is called a maximum length sequence.

The four-stage linear shift register in Figure 13 generates the sequence 100010011010111 100010011010111...whose period is P = 15. In a maximum length sequence, all sets of n consecutive bits except all zeroes occur. Also, it is evident from Figure 13 that all states of 4-bit binary counter (except 0000) appear in random order.

The actual implementation of the PRN generator can be accomplished in various ways. The advantage of using registered PROMs for implementing PRN sequences is that it can be easily customized and also because it has a large number of product terms which are needed in the above design.

The PRN generator of Figure 13 can be implemented using registered PROMs as shown in Figure 14.

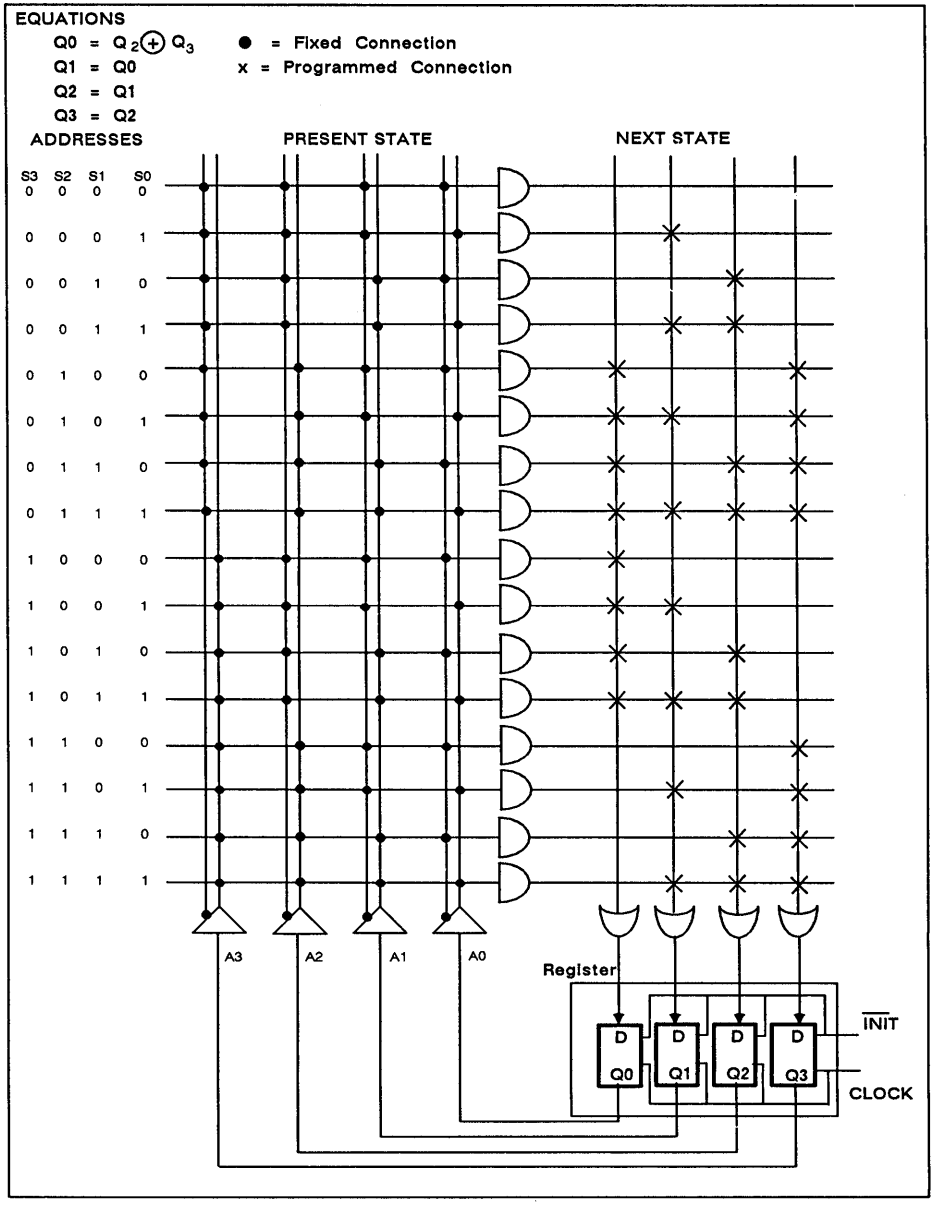


Figure 14. A Four-Stage PRN Generator Implemented With Registered PROMs

CONCLUSION

Summing up, registered PROMs from Fujitsu provide a high speed solution for computer architecture as well as for other digital system implementations. This leads to the conclusion that integration of registers in PROMs greatly enhances over all performance in the designs which utilize them.

REFERENCES

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2. *Complete Feedback Shift Register Design For Built-in Self-Test*, Wang, L. T. and E. J. McClusky, CRC Tech: Report Standford University, 1986
3. *Logic Implementation, A New Horizon For Bipolar PROMs* Nusra Lodhi, Fujitsu Microelectronics Incorporated, Application Note, May 1986
4. *Shift Register Sequences* Golomb, S. W., Holden-Day, Inc. 1967
5. *Digital Signal Processing*, Oppenhiem & Schafer, 1975, Addison Wesley, Inc. Chapter 10.

Bipolar PROM Cross Reference Guide (Max. Commercial Limits)

Fujitsu Part No.	Organi-zation	Out-put	Package Pins	Signetics	AMD	MMI	National	TI	Harris	Fairchild	Hitachi	Motorola	Raytheon	Intel
MB7111	32x8	OC	16	N82S23	AM27S18	6330	DM54S188 DM74S188	TBP18SA30	HM7602					
MB7112		TS	16	N82S123	AM27S19	6331	DM54S288 DM74S288	TBP18S030	HM7603			MCM27S19		
MB7113	256x4	OC	16	N82S126	AM27S20	6300	DM54S387 DM74S387	TBP24SA10	HM7610					
MB7114		TS	16	N82S129	AM27S21	6301	DM54S287 DM74S287	TBP24S10	HM7611					
MB7115	512x4	OC	16	N82S130	AM27S12	6305	DM54S570 DM74S570		HM7620					
MB7116		TS	16	N82S131	AM27S13	6306	DM54S571 DM74S571		HM7621			MCM7621		
MB7117	256x8	OC	20			5308 6308		TBP28LA22						
MB7118		TS	20			5309 6309	DM54S471 DM74S471	TBP28L22						
MB7121	1Kx4	OC	18		AN27S32	5352 6352	DM54S572 DM74S572	TBP24SA41	HM7642	93452	HN25044			
MB7122		TS	18	N82S137 S82S137	AM27S33	53S441 63S441	DM54S573 DM74S573	TBP24S41	HM7643	93453	HN25045	MCM7643		
MB7123	512x8	OC	20		AM27S28	5348 6348	DM54S473 DM74S473	TBP28SA42						
MB7124		TS	20	N82S147 S82S147	AM27S29	5349 6349	DM54S472 DM74S472	TBP28S42	HM7649				29623	
MB7128	2Kx4	TS	18	N82S185 S82S185	AM27S185	5389 6389	DM77S185 DM87S185	TBP24S81	HM7685			MCM7685	29651	
MB7132	1Kx8		24	N82S181 S82S181	AM27S181	5381 6381	DM77S281 DM87S281	TBP28S86	HM7681	93451	HN25089	MCM7681	29631	3628
MB7134	4Kx4		20	N82HS195 S82HS195	AM27541	53S1641 63S1641	DM77S195 DM87S195		HM76165			MCM76165		
MB7138	2Kx8		24	N82S191 S82S191	AM27S191	63S1681	DM77S191 DM87S191	TBP28S166A	HM76161	932511	HN25169	MCM76161	29681	3636
MB7142	4Kx8		24	N82S321 S82S321	AM27S43	63S3281	DM77S321 DM87S321		HM76321				29671	3632
MB7144	8Kx8		24	82HS641	AM27S49				HM76641					
MB7152	4Kx4		24	N82S195 S82S195	AM27S41	53S1641 63S1641	DM77S195 DM87S195		HM76165	93565		MCM76161		
MB7226RA	512x8		24		AM27S25	53RA481 63RA481	DM87SR25							
MB7232RA	1Kx8		24		AM27S35	53RA881 63RA881	DM87SR181					MCM27S35		

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Bipolar PROM Cross Reference Guide (Max. Commercial Limits)

FUJITSU P/N	TAA	ORG	OUT-PUT	PINS	FAIRCHILD P/N	TAA	CYPRESS P/N	TAA	WAFERSCALE P/N	TAA
MB7117E MB7117H	45ns 35ns	256 X 8	OC	20						
MB7118E MB7118H	45ns 35ns	256 X 8	3S	20						
MB7121E MB7121H	45ns 35ns	1K X 8	OC	18						
MB7122E MB7122H MB7122Y	45ns 35ns 30ns	1K X 4	3S	18						
MB7123E MB7123H	45ns 35ns	512 X 8	OC	20						
MB7124E MB7124H	45ns 35ns	512 X 8	3S	20						
MB7127E MB7127H	55ns 45ns	2K X 4	OC	18						
MB7128E MB7128H MB7128Y	55ns 45ns 35ns	2K X 4	3S	18						
MB7131E MB7131H	55ns 45ns	1K X 8	OC	24	93Z450 93Z450A	40ns 35ns				
MB7132E MB7132H MB7132Y	55ns 45ns 35ns	1K X 8	3S	24	93Z451 93Z451A	40ns 35ns	7C282-45 7C282-30	45ns 30ns		
MB7134E MB7134H MB7134Y	55ns 45ns 35ns	4K X 4	3S	20						

4

FUJITSU P/N	TAA	ORG	OUT-PUT	PINS	FAIRCHILD P/N	TAA	CYPRESS P/N	TAA	WAFERSCALE P/N	TAA
MB7138E MB7138H MB7138Y MB71A38-35 MB71A38-25	55ns 45ns 5ns 35ns 25ns	2K X 8	3S	24	93Z511	45ns	7C291/92-50 7C291/92-35 7C291A/92A-25	50ns 35ns 25ns	57C191/291-55 57C191/291-45 57C191B/291B-35	55ns 45ns 35ns
MB7141E MB7141H	65ns 55ns	4K X 8	OC	24						
MB7142E MB7142H	65ns 55ns	4K X 8	3S	24					57C43-70 57C43-55	70ns 55ns
MB7144E MB7144H MB71C44-45 MB71C44-35	65ns 55ns 45ns 35ns	8K X 8	3S	24	93Z565 93Z565A 93Z665-35 93Z667-35	55ns 45ns 35ns 35ns	7C263/64-45 7C263/64-35	45ns 35ns	57C49-70 57C49-55 57C49B-45 57C49B-35	70ns 55ns 45ns 35ns
MB7152E MB7152H MB7152Y	55ns 45ns 35ns	4K X 4	3S	20						
MB71C46-45 MB71C46-35	45ns 35ns	16K X 8	3S	28			7C254-55 7C254-45	55ns 45ns	57C51-70 57C51B-45 57C51B-40	70ns 45ns 40ns
MB7226RA-25 MB7226RA-20	25ns 20ns	512 X 8	3S	24			7C225-40 7C225-35	25ns 20ns		
MB7232RA-25 MB7232RA-20	25ns 20ns	1K X 8	3S	24			7C235-40 7C235-30	20ns 15ns		
MB7238RA-25 MB7238RA-20	25ns 20ns	2K X 8	3S	24			7C245-25 7C245A-20	25ns 20ns	57C45-35	15ns

10/28/88

Bipolar PROM Cross Reference Guide (Max. Commercial Limits)

FUJITSU P/N	TAA	ORG	OUT-PUT	PINS	SIGNETICS P/N	TAA	AMD P/N	TAA	MMI P/N	TAA	NATIONAL P/N	TAA	TI P/N	TAA
MB7152E MB7152H MB7152Y	55ns 45ns 35ns	4K X 4	3S	20	82HS195 82HS195A	45ns 35ns	27S41 27S41A	50ns 35ns	63S1641 63S1641A	50ns 35ns	87S195A 87S195B	45ns 35ns	34S162-45 34S162-35	45ns 35ns
MB71C46-45 MB71C46-35	45ns 35ns	16K X 8	3S	28	82HS1281	45ns	27S51 27S51A	55ns 35ns						
MB7226RA-25 MB7226RA-20	25ns 20ns	512 X 8	3S	24			27S25 27S25A	27ns 20ns	63RA481 63RA481A	20ns 15ns	87SR25 87SR25B	27ns 20ns		
MB7232RA-25 MB7232RA-20	25ns 20ns	1K X 8	3S	24	82HS187	20ns	27S35 27S35A	25ns 20ns			87SR183 87SR183B	25ns 20ns		
MB7232RS-25 MB7232RS-20	25ns 20ns	1K X 8	3S	24	82HS189	20ns	27S37 27S37A	25ns 20ns	63RS881 63RS881A	20ns 15ns	87SR181	20ns		
MB7238RA-25 MB7238RA-20	25ns 20ns	2K X 8	3S	24			27S45 27S45A	25ns 20ns	63RA1681 63RA1681A	25ns 15ns	87SR193	15ns	38R165-18 38R165-20	12ns 15ns
MB7238RS-25 MB7238RS-20	25ns 20ns	2K X 8	3S	24			27S47 27S47A	25ns 20ns	63RS1681 63RS1681A	20ns 15ns	87SR191	15ns		
MB7111E MB7111H	35ns 25ns	32 X 8	OC	16										
MB7112E MB7112H MB7112Y	35ns 25ns 20ns	32 X 8	3S	16										
MB7113E	40ns	256 X 4	OC	16										
MB7114E MB7114H	40ns 30ns	256 X 4	3S	16										
MB7115E MB7115H	45ns 35ns	512 X 4	OC	16										
MB7116E MB7116H MB7116Y	45ns 35ns 0ns	512 X 4	3S	16										

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Bipolar PROM Cross Reference Guide (Max. Commerical Limits)

FUJITSU P/N	TAA	ORG	OUT-PUT	PINS	SIGNETICS P/N	TAA	AMD P/N	TAA	MMI P/N	TAA	NATIONAL P/N	TAA	TI P/N	TAA
MB7111E MB7111H	35ns 25ns	32 X 8	OC	16	82S23 82S23A	50ns 25ns	27S18 27S18A	40ns 25ns	63S080	25ns	74S188 74S188A	35ns 25ns	18SA030 38SA030	40ns 25ns
MB7112E MB7112H MB7112Y	35ns 25ns 20ns	32 X 8	3S	16	82S123 82S123A	50ns 25ns	27S19 27S19A	40ns 25ns	63S081 63S081A	25ns 15ns	74S288 74S288A	35ns 25ns	18S030 38S030	40ns 25ns
MB7113E	40ns	256 X 4	OC	16	82S126 82S126A	50ns 30ns	27S20 27S20A	45ns 30ns	63S140	45ns	74S387 74S387A	50ns 30ns	24SA10	65ns
MB7114E MB7114H	40ns 30ns	256 X 4	3S	16	82S129 82S129A	50ns 27ns	27S21 27S21A	45ns 30ns	63S141 63S141A	45ns 30ns	74S287 74S287A	50ns 30ns	24S10	55ns
MB7115E MB7115H	45ns 35ns	512 X 4	OC	16	82S130 82S130A	50ns 33ns	27S12 27S12A	50ns 30ns	63S240	45ns	74S570 74S570A	55ns 45ns		
MB7116E MB7116H MB7116Y	45ns 35ns 30ns	512 X 4	3S	16	82S131 82S131A	50ns 30ns	27S13 27S13A	50ns 30ns	63S241 63S241A	45ns 35ns	74S571 74S571A 74S571B	55ns 45ns 35ns		
MB7117E MB7117H	45ns 35ns	256 X 8	OC	20					63S280	45ns			28LA22	70ns
MB7118E MB7118H	45ns 35ns	256 X 8	3S	20	82S135	45ns			63S281 63S281A	45ns 28ns	74LS471	60ns	28L22	70ns
MB7121E MB7121H	45ns 35ns	1K X 4	OC	18			27S32 27S32A	55ns 35ns	63S440	45ns	74S572 74S572A	60ns 45ns	24SA41	60ns
MB7122E MB7122H MB7122Y	45ns 35ns 30ns	1K X 4	3S	18	82S137 82S137A 82S137B	60ns 45ns 35ns	27S33 27S33A	55ns 35ns	63S441 63S441A	45ns 35ns	74S573 74S573A 74S573B	60ns 45ns 35ns	24S41	60ns
MB7123E MB7123H	45ns 35ns	512 X 8	OC	20			27S28 27S28A	55ns 35ns	63S480	45ns	74S473 74S473A	60ns 45ns	28SA42	65ns

FUJITSU P/N	TAA	ORG	OUT-PUT	PINS	SIGNETICS P/N	TAA	AMD P/N	TAA	MMI P/N	TAA	NATIONAL P/N	TAA	TI P/N	TAA
MB7124E MB7124H	45ns 35ns	512 X 8	3S	20	82S147 82S147A	60ns 45ns	27S29 27S29A	55ns 35ns	63S481 63S481A	45ns 30ns	74S472 74S472A 74S472B	60ns 45ns 35ns	28LS2 28S42	95ns 60ns
MB7127E MB7127H	55ns 45ns	2K X 4	OC	18			27S184 27S184A	50ns 35ns			87S184 87S184A	55ns 45ns	24SA81	70ns
MB7128E MB7128H MB7128Y	55ns 45ns 35ns	2K X 4	3S	18	82S185 82S185A 82S185B	100ns 50ns 45ns	27S185 27S185A	50ns 35ns	63S841 63S841A	50ns 35ns	87S185 87S185A 87S185B	55ns 45ns 35ns	24S81	70ns
MB7131E MB7131H	55ns 45ns	1K X 8	OC	24			27S180 27S180A	60ns 35ns			87S180	55ns	28SA86A	70ns
MB7132E MB7132H MB7132Y	55ns 45ns 35ns	1K X 8	3S	24	82S181 82S181A 82S181B 82S181C	70ns 55ns 45ns 35ns	27S181 27S181A	60ns 35ns	63S881 63S881A	45ns 30ns	87S181 87S181A	55ns 45ns	28S86A	65ns
MB7134E MB7134H MB7134Y	55ns 45ns 35ns	4K X 4	3S	20							87S195A 87S195B	45ns 35ns		
MB7138E MB7138H MB7138Y MB71A38-35 MB71A38-25	55ns 45ns 35ns 35ns 25ns	2K X 8	3S	24	82S191 82S191A 82S191C	80ns 55ns 35ns	27S191 27S191A	50ns 35ns	63S1681 63S1681A	50ns 35ns	87S191 87S191A 87S191B	65ns 45ns 35ns	28S166 38L165/66-45 38S165/66-35 38L165/66-35 38S165/66-25	75ns 45ns 35ns 35ns 25ns
MB7142E MB7142H	65ns 55ns	4K X 8	3S	24	82S321 82HS321 82HS321A	70ns 45ns 35ns	27S43 27S43A	55ns 40ns	63S3281 63S3281A	45ns 35ns	87S321	55ns		
MB7144E MB7144H MB71C44-45 MB71C44-35	65ns 55ns 45ns 35ns	8K X 8	3S	24	82HS641 82HS641A 82HS641B	55ns 45ns 35ns	27S49 27S49A 27C49	55ns 40ns 35ns						

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Commercial Temperature Range (0 °C to +75 °C)						
Device	Organization	Output	Access Time (ns)	Power Supply Volts	Power Supply Current	DIP pins
MB7111E	32 x 8	OC	35ns	+5V ± 5%	100mA	16-pin
H			25ns			
L			50ns		40mA	
MB7112E		TS	35ns		100mA	
H			25ns			
Y			20ns			
L			50ns		40mA	
MB7113E	256 x 4	OC	40ns		100mA	16-pin
H			30ns			
L			50ns		40mA	
MB7114E		TS	40ns		100mA	
H			30ns			
L			50ns		40mA	
MB7115E	512 x 4	OC	45ns		120mA	16-pin
H			35ns			
L			50ns		50mA	
MB7116E		TS	45ns		120mA	
H			35ns			
Y			25ns			
L			60ns		50mA	
MB7117E	256 x 8	OC	45ns		140mA	20-pin
H			35ns			
L			60ns		75mA	
MB7118E		TS	45ns		140mA	
H			35ns			
Y			25ns			
L			60ns		75mA	
MB7121E	1K x 4	OC	45ns		150mA	18-pin
H			35ns			
L			60ns		50mA	
MB7122E		TS	45ns		150mA	
H			35ns			
Y			25ns			
L			60ns		50mA	
MB7123E	512 x 8	OC	45ns		170mA	20-pin
H			35ns			
L			60ns		75mA	
MB7124E		TS	45ns		170mA	
H			35ns			
Y			25ns			
L			60ns		75mA	
MB7128E	2K x 4	TS	55ns		155mA	24-pin
H			45ns			
Y			35ns			
L			70ns		60mA	
MB7132E	1K x 8		55ns		175mA	24-pin
H			45ns			
Y			35ns			
L			70ns		60mA	
MB7134E	4K x 4		55ns		170mA	20-pin
H			45ns			
MB7138E	2K x 8		55ns		180mA	24-pin
H			45ns			
Y			35ns			
MB7142E	4K x 8		65ns		185mA	24-pin
H			55ns			

4

Temperature Ranges (Continued)

Commercial Temperature Range (0 °C to +75 °C)						
Device	Organization	Output	Access Time (ns)	Power Supply Volts	Power Supply Current	DIP pins
MB7144E H	8K x 8	TS	65ns 55ns	+5V ± 5%	190mA	24-pin
MB7152E H Y	4K x 4		55ns 45ns 35ns		170mA	20-pin
MB7226RA-25 -20 MB7226RS-25 -20	512 x 8		25ns 20ns 25ns 20ns		170mA	24-pin
MB7232RA-25 -20 MB7232RS-25 -20	1K x 8		25ns 20ns 25ns 20ns		185mA	
MB7238RA-25 -20 MB7238RS-25 -20	2K x 8		25ns 20ns 25ns 20ns			
MB71A38-35 -25	2K x 8		35ns 25ns		120mA	
MB71C44-45 -35	4K x 8		45ns 35ns		60mA	
MB71C46-45 -35	8K x 8		45ns 35ns			28-pin

Extended Temperature Range (-55 °C to +125 °C)						
Device	Organization	Output	Access Time (ns)	Power Supply Volts	Power Supply Current	DIP pins
MB7112E-W MB7112L-W	32 x 8	TS	35ns 60ns	+5V ±10%	100mA 40mA	16-pin
MB7114E-W MB7114L-W	256 x 4		40ns 60ns		100mA 40mA	
MB7116E-W MB7116L-W	512 x 4		45ns 70ns		120mA 50mA	
MB7118E-W MB7118L-W	256 x 8		45ns 70ns		140mA 75mA	20-pin
MB7122E-W MB7122L-W	1K x 4		45ns 70ns		150mA 50mA	18-pin
MB7124E-W MB7124L-W	512 x 8		45ns 70ns		170mA 75mA	20-pin
MB7128E-W MB7128L-W	2K x 4		55ns 80ns		155mA 60mA	24-pin
MB7132E-W MB7132L-W	1K x 8		55ns 80ns		175mA 60mA	18-pin
MB7134E-W	4K x 4		55ns		170mA	20-pin
MB7138E-W MB7142E-W MB7144E-W MB7152E-W	2K x 8 4K x 8 8K x 8 4K x 4		55ns 65ns 65ns 55ns		180mA 185mA 190mA 170mA	24-pin
MB7226RA-25-W MB7226RS-25-W	512 x 8		25ns		170mA	
MB7232RA-25-W MB7232RS-25-W	1K x 8		25ns		185mA	
MB7238RA-25-W MB7238RS-25-W	2K x 8		25ns		185mA	

FUJITSU PROM TECHNOLOGY

The Fujitsu MB71C00 series is the junction-shorting BICMOS PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate(Fig. 1).

Each memory cell is divided by passive isolations named U-FOX (U-groove isolation with thick Field OXide process).

The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

Fig. 1 - PROGRAMMED CELL (CROSS SECTION)

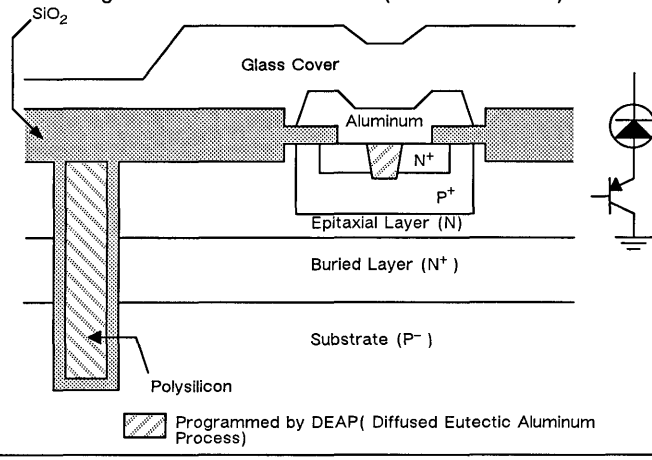
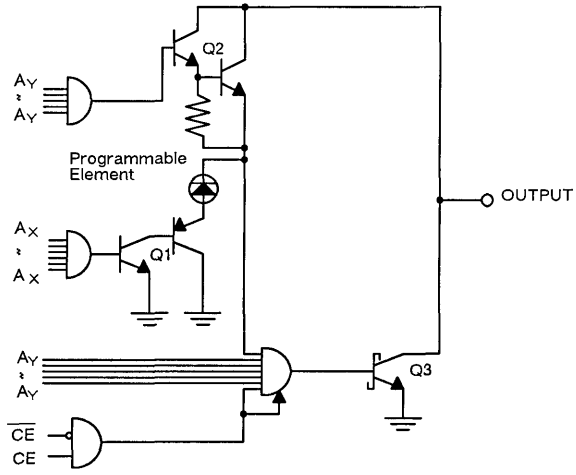


Fig. 2 - INTERNAL PROGRAMMING CIRCUIT



4

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (In electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

As shown in Fig. 2, transistors, Q1 and Q2, are turned on to select the desired bit for programming by using all address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q2 and memory cell into transistor Q1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified.

To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{CC}= 2.4V and V = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

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DC SPECIFICATIONS (TA = 25°C)

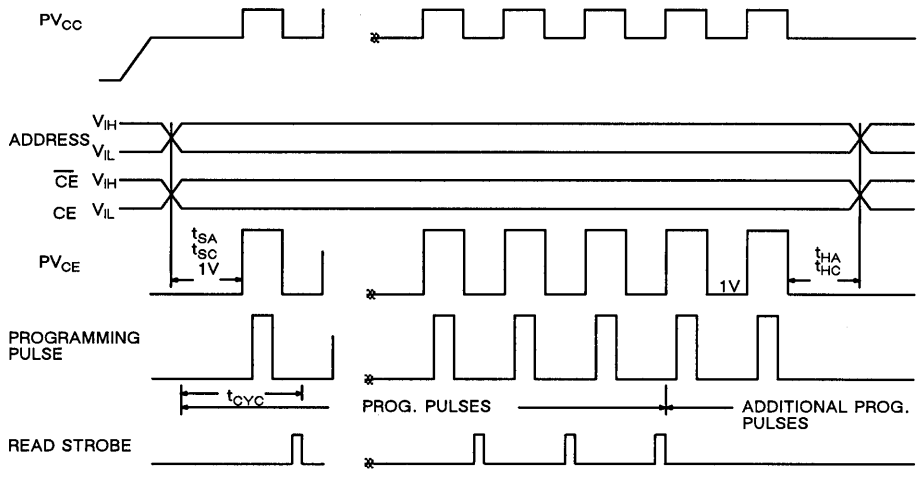
Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH}		2.0		5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	V
Programming Pulse Current	I_{PRG}		60		65	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS (T_A = 25°C)

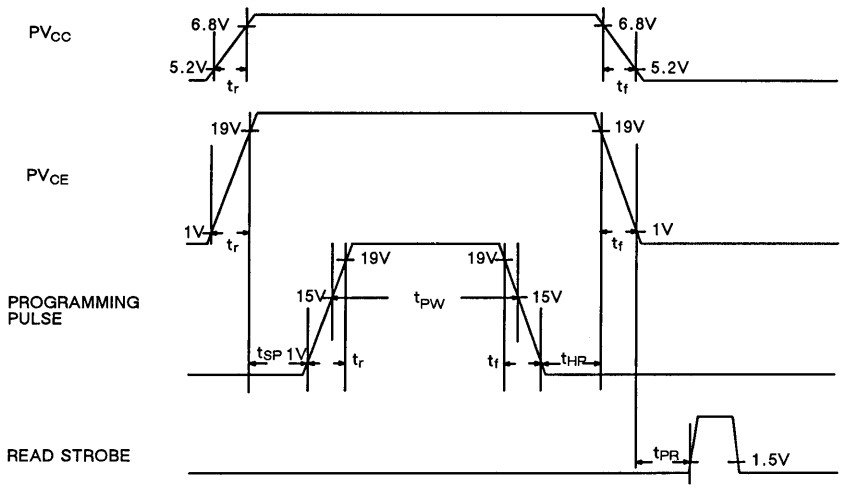
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	µs
Programming Pulse Width	t_{PW} (1)	10	11	12	µs
Programming Pulse Rise Time	t_r (2)	–	–	2	µs
PV_{CE} Pulse Rise Time	t_r (3)	–	–	2	µs
PV_{CC} Pulse Rise Time	t_r (4)	–	–	2	µs
Programming Pulse Fall Time	t_f (5)	–	–	2	µs
PV_{CE} Pulse Fall Time	t_f (6)	–	–	2	µs
PV_{CC} Pulse Fall Time	t_f (7)	–	–	2	µs
Address Input Set-up Time	t_{SA}	2	–	–	µs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	µs
PV_{CE} Set-up Time	t_{SP} (8)	4	–	–	µs
Address Input Hold Time	t_{HA}	2	–	–	µs
Chip Enable Input Hold Time	t_{HC}	2	–	–	µs
PV_{CE} Hold Time	t_{HP} (9)	2	–	–	µs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (10)	10	–	–	µs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	µs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Note: (1) Stipulated 400Ω load and 15V.
(2) From 1V to 19V (400Ω load).
(3) From 1V to 19V.
(4) From 5.2V to 6.8V.
(5) From 19V to 1V (400Ω load).
(6) From 19V to 1V.
(7) From 6.8V to 5.2V.
(8) From PV_{CE} pulse 19V to programming pulse 1V.
(9) From programming pulse 1V to PV_{CE}pulse 19V
(10) From PV_{CE} pulse 1V to read strobe.

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



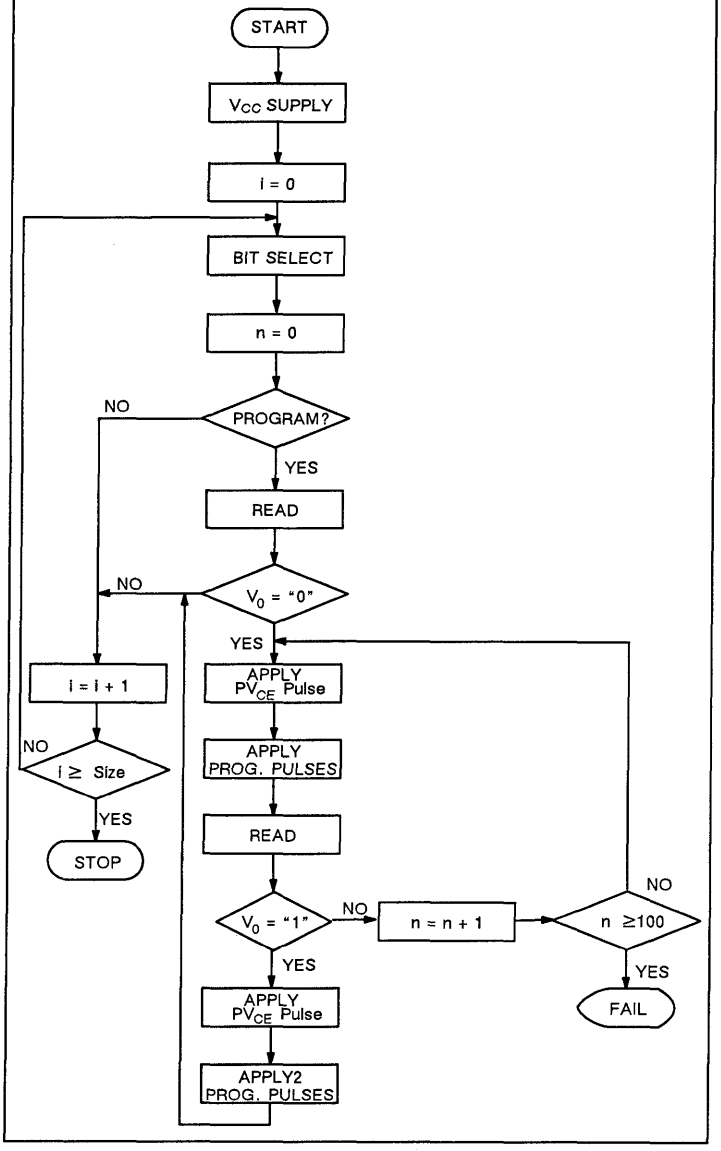
PROGRAMMING PROCEDURE

1. Apply power; V_{CC}= PV_{CC} ,GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 62.5mA and duration of t_{PW}(11μS) after a delay of t_{SP}(4μS).
6. Read the output V_O after a delay of t_{PR}(10μS).
   a) In the case of V_O = low, repeat steps "4","5" and "6" with cycle time of t_{CYC} (50μS)
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA}(2μS).

Note

1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C ± 2°C)

Fig. 3 - PROGRAMMING FLOW CHART



4

The DEAP Technique

Introduction

A PROM device is composed of a programmable memory cell array and peripheral circuitry for input, output, and programming. Fujitsu's memory cell consists of an emitter-base junction as the programmable element and a collector-base junction as the switching element. Programming is based on a technique referred to as DEAP, an acronym for Diffused Eutectic Aluminum Process.

Briefly described, the Fujitsu-designed DEAP programming technique utilizes an aluminum and a polysilicon layer sitting on top of an emitter–base diode. During programming, a reverse current sufficient to raise the temperature of the junction is applied to the emitter. When the temperature increases to a certain point, an aluminum-silicon eutectic is formed from the aluminum and polysilicon layers on top of the emitte-base junction. This eutectic is diffused from the surface of the emitter down through the emitter-base junction, thus shorting the junction out. Once the eutectic has shorted out the junction, power dissipation and temperature at the junction decrease rapidly. This phenomenon prevents further diffusion of the aluminum-silicon eutectic. Therefore, the collector-base junction is protected from damage. After the cell has cooled down, two additional programming pulses are applied to the cell to provide a highly reliable and uniform resistive short.

What Makes DEAP Better

Today, bipolar PROMs utilize two basic programming technologies. The first and most widely used is the fusible link. Several types of fuse materials are used to achieve this method of programming. The most common types of fuse materials are nichrome, titanium-tungsten and polysilicon. A second and more advantageous technology for programming bipolar PROMs, is the Fujitsu DEAP technique. A brief description of each technology is necessary to explain why DEAP is better.

Fusible link technology can be referred to as a "surface" technology. A fusible link normally sits on the surface of the silicon and occupies a considerable amount of silicon real estate. To make a small die and a highly dense device with fusible link technology requires a major effort in device masking during manufacturing.

When programming a fusible link, a section of the fuse is blown open just like a common electrical fuse. A closer look shows that the fuse material has been melted at the gap and splattered about. This fuse splattering causes fragments of fuse material to be scattered on the surface. This is not a "clean" operation. On some PROMs, the passivation layer could be ruptured exposing the die to possible contamination. On other PROMs, an opening is designed above the fuse gap in the passivation layer so the fuse is deliberately exposed. These openings or windows are potential reliability factors because moisture, salts or stray fuse material fragments can reach the die through these openings.

The DEAP Technique (Continued)

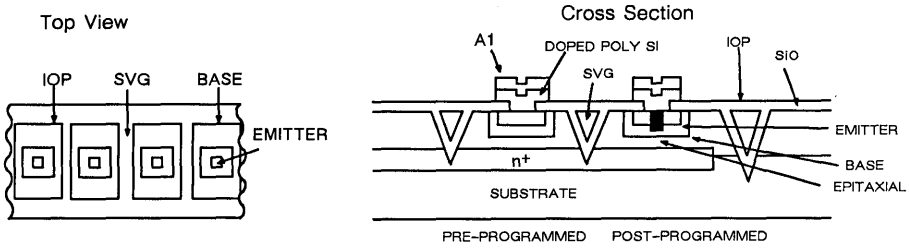
Generally after blowing a fusible link, the gap that has been created is very narrow. Because of the narrow width of the gap a very high electric field can exist across the gap. Because of this electric field, atoms can migrate across the gap and eventually partially reconnect the fuse of memory cells where programming has taken place. This action is referred to as "growback". Generally this problem becomes apparent under accelerated life testing or after many hours of operation.

The Fujitsu DEAP programming technique is not a "surface" technology but a "subsurface" technology. The programmable element is vertical not horizontal like a fusible link. There are several advantages to this type of approach. The memory cell can be designed much smaller with the same manufacturing tolerances resulting in smaller die sizes and faster access times. Since DEAP is a "subsurface" technology, there is no need for openings in the passivation layer and it cannot be ruptured. Therefore, there is no chance for the die to be exposed to contaminates. The DEAP technique exhibits no splatter fuse material whatsoever. The DEAP programming technique has no "growback" mechanism like a fusible link because the shorting mechanism is self limiting and extremely reliable.

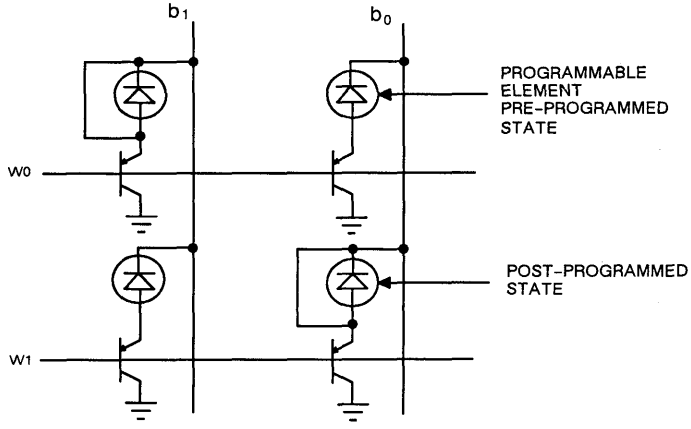
How Reliable is DEAP

In section 5, you'll see specific data on reliability. The DEAP technology with its fully passivated die and subsurface eutectic process means high reliability as well as fast access time and small die size.

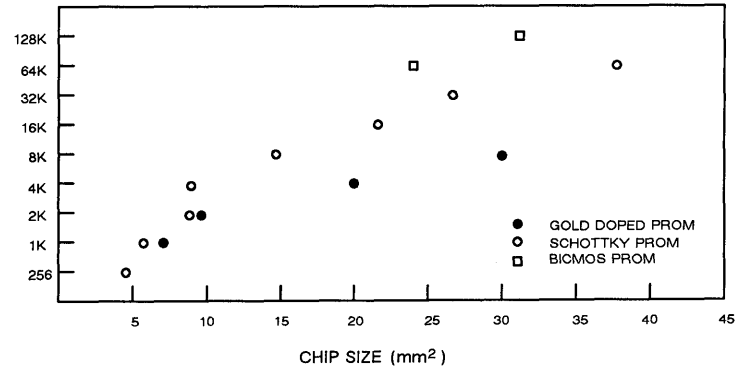
DEAP™ Cell Structure



Electrical Equivalent



PROM Cell Technologies



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FUJITSU

PROGRAMMABLE SCHOTTKY 256-BIT READ ONLY MEMORY

MB 7111E/H
MB 7112E/H/Y
MB 7111L
MB 7112L

March 1986
Edition 2.0

SCHOTTKY 256 BIT DEAP PROM (32 WORDS x 8 BITS)

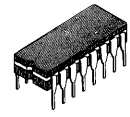
The Fujitsu MB 7111 and MB 7112 are high speed Schottky TTL electrically field programmable read only memories organized as 32 words by 8-bits. With uncommitted collector outputs provided on the MB 7111 and three-state outputs on the MB 7112 memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed SVG (Shallow V-Groove) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

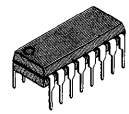
The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

- Single +5V supply voltage.
- Power supply current:
  100 mA max. (E/H/Y)
  40 mA max. (L)
- 32 words x 8 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time, 15 ns typ.
  Y: 20 ns max.
  H: 25 ns max.
  E: 35 ns max.
- Fast access time, 35 ns typ
  L: 50 ns max.
- TTL compatible inputs and outputs.
- Open collector outputs (MB 7111)
- 3-state outputs (MB 7112)
- One chip enable leads for simplified memory expansion.
- Standard 16 pin Ceramic (Cerdip) DIP (Suffix: -CZ)
  Standard 16 pin Plastic DIP (Suffix: -M)
  Standard 16 pin Plastic FPT (Suffix: -PF)
  Standard 20 pad Ceramic LCC (Suffix: -TV)
- JEDEC approned pin out

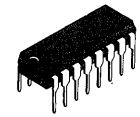


CERAMIC PACKAGE
DIP-16C-C02

PLASTIC PACKAGE
FPT-16P-M02



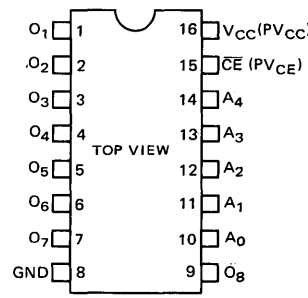
PLASTIC PACKAGE
DIP-16P-M02



PLASTIC PACKAGE
DIP-16P-M04

LCC-20C-F02: See Page 19

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 19

ABSOLUTE MAXIMUM RATINGS (See NOTE)

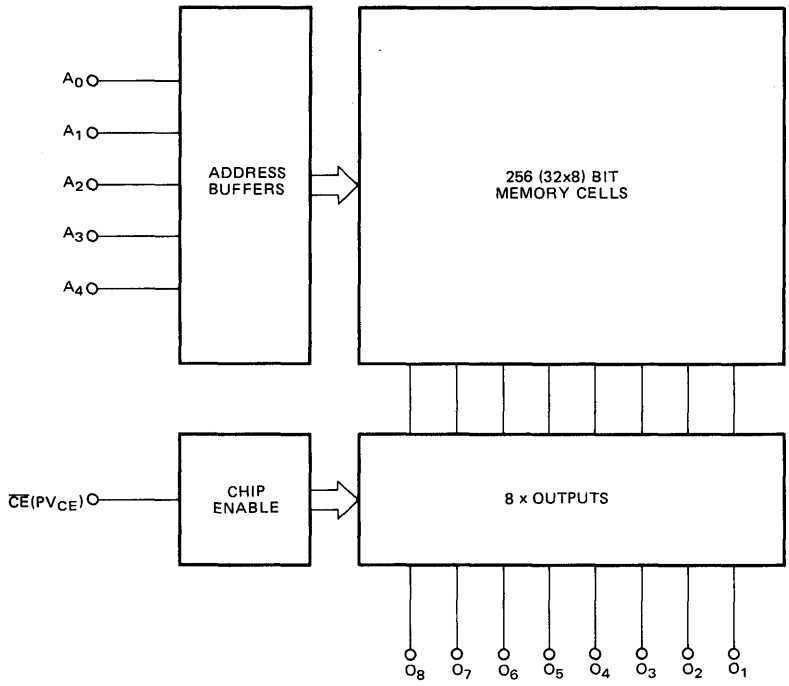
Parameter		Symbol	Rating	Unit
Power Supply Voltage		V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CC}	−0.5 to +7.5	V
Input Voltage		V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)		V_{IPRG}	22.5	V
Output Voltage (during programming)		V_{OPRG}	−0.5 to +22.5	V
Input Current		I_{IN}	−20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+150	mA
Storage Temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Output Voltage		V_{OUT}	−0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – MB 7111/7112 BLOCK DIAGRAM



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CAPACITANCE ($f = 1MHz$, $V_{CC} = +5V$, $V_{IN} = +2V$, $T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			12	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0		0.8	V
Input High Voltage	V_{IH}	2.0		5.5	V
Ambient Temperature	T_A	0		75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Low Current (V_{IL} = 0.45V)		I_F			-250	μA
Output Low Voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output Low Voltage (I_{OL} = 16mA)		V_{OL}			0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)	MB 7111	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4V, chip disabled)	MB 7112	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.45V, chip disabled)	MB 7112	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	E/H/Y	I_{CC}		70	100	mA
	L			25	40	
Output High Voltage (I_O = -2.4mA)	MB 7112	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB 7112	I_{OS}*	-15		-60	mA

NOTE: *Denotes guaranteed characteristics of the output high-level (ONE) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4 V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

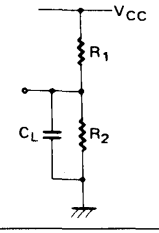
4

Fig. 2 – AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

LOAD CONDITION



	MB 7111/MB 7112		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

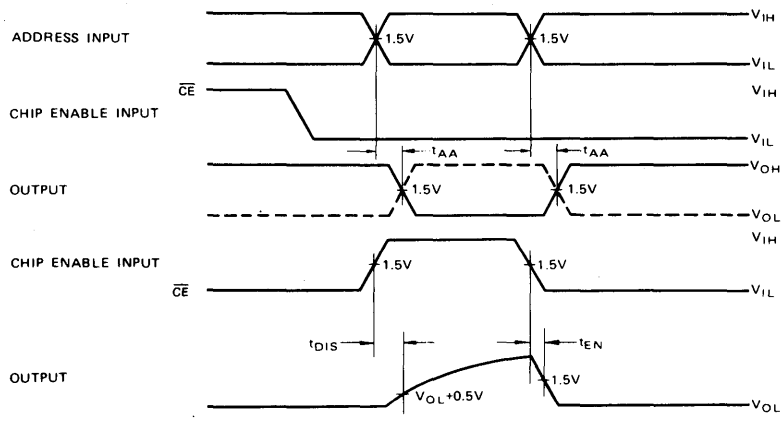
AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	E		H		Y		L		Unit
		Type	Max	Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	15	35	15	25	15	20	35	50	ns
Output Disable Time	t_{DIS}	15	25	15	20	15	20	20	30	ns
Output Enable Time	t_{EN}	10	20	10	20	10	15	20	30	ns

NOTE: Using Wired-OR outputs, this value is equivalent to the output enable time (t_{EN}) of the device.

OPERATION TIMING DIAGRAM



NOTE: Output disable time is the time taken for the output to reach a high inpedance state when chip enable goes high. Output enable time is the time taken for the output to become active when chip enable goes low. The high inpedance state is defined as a point on the output waveform, that is 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

OPEN-COLLECTOR OUTPUT

Open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7112 (3-state) compared to 0mA for the MB 7111 (open-collector).

THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

If two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously, with short circuit current from one enabled device flowing through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should ensure that this condition does not exist.

Fig. 3 – MB 7111/7112 INPUT

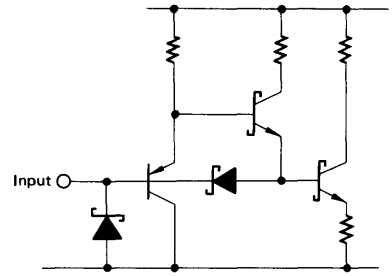


Fig. 4 – MB 7111L/7112L INPUT

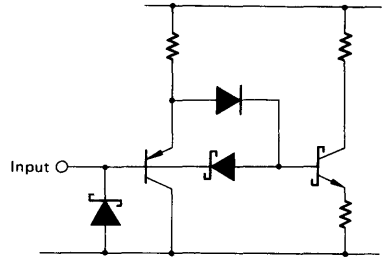
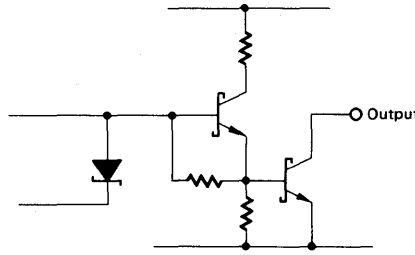


Fig. 5 – MB 7111 OUTPUT



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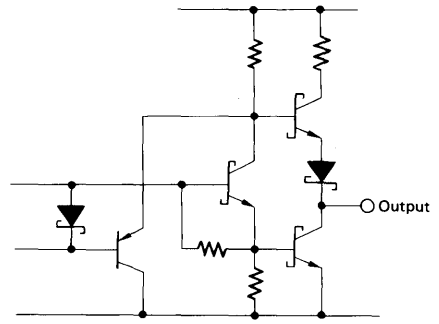
In the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the output circuit decreases the load on the Chip Enable circuit.

Fig. 6 – MB 7112 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 7 – I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

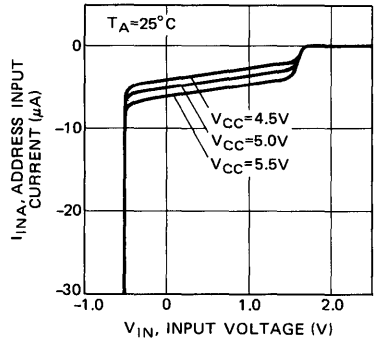

Fig. 8 – I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

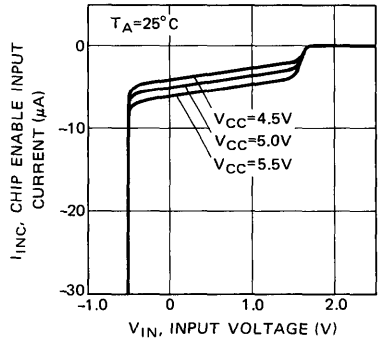

Fig. 9 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

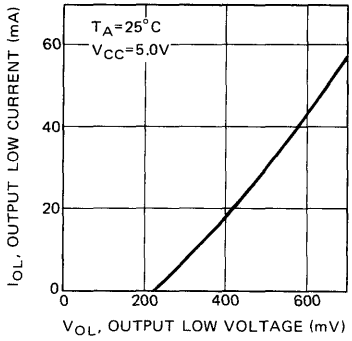

Fig. 10 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

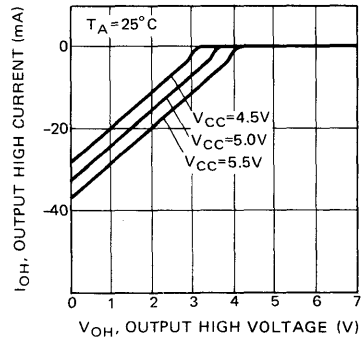

Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

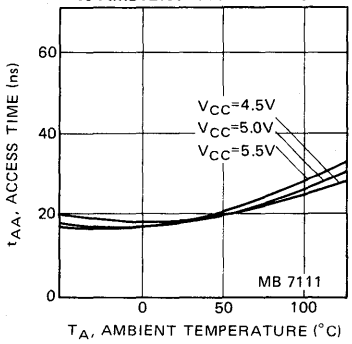

Fig. 12 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

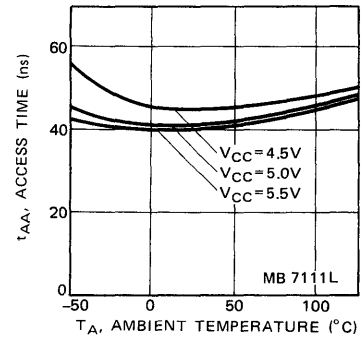

Fig. 13 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

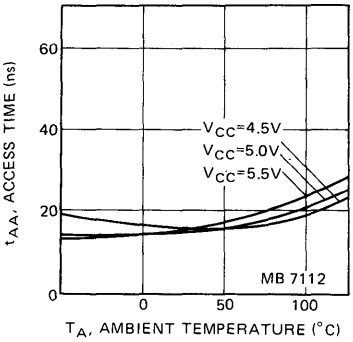

Fig. 14 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

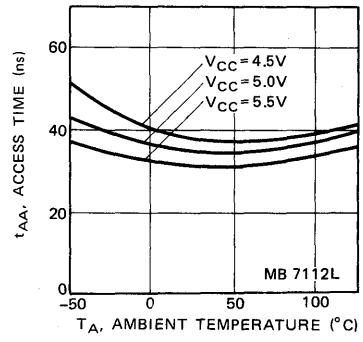

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Fig. 15 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

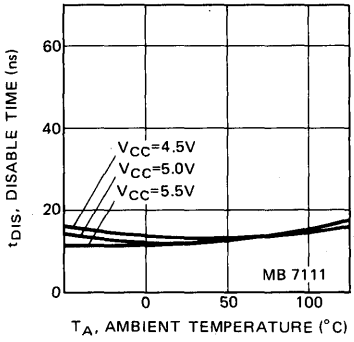

Fig. 16 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

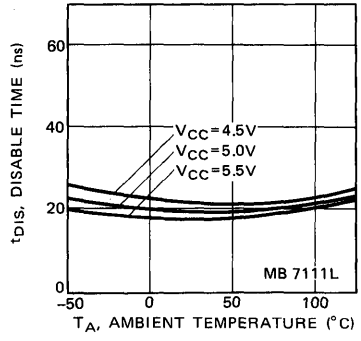

Fig. 17 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

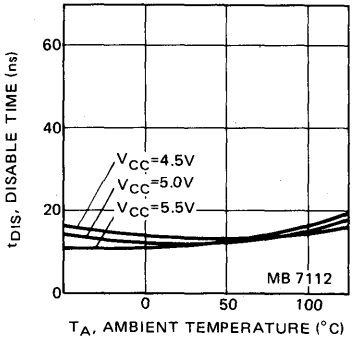

Fig. 18 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

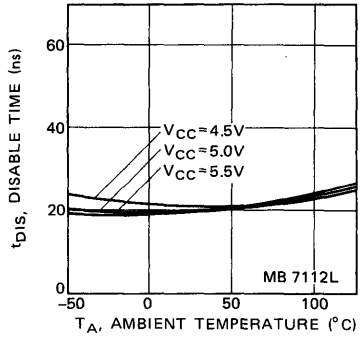

Fig. 19 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

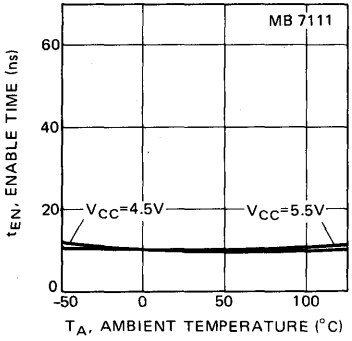

Fig. 20 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

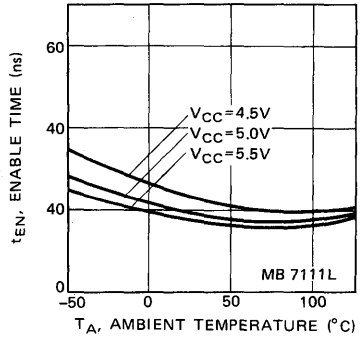

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Fig. 21 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

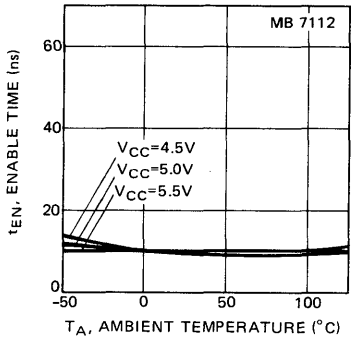


Fig. 22 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

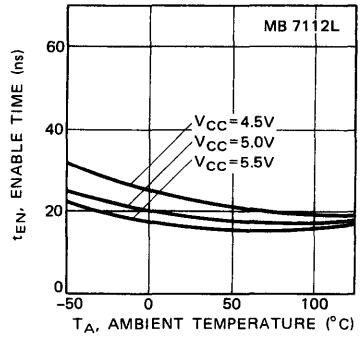


Fig. 23 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

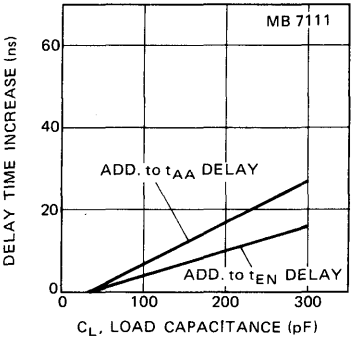


Fig. 24 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

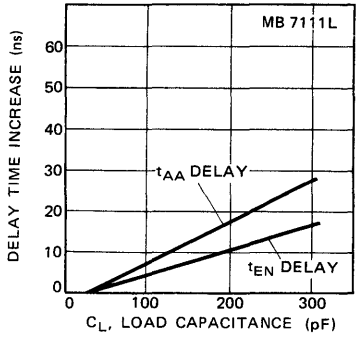


Fig. 25 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

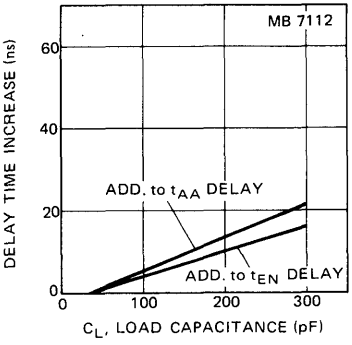
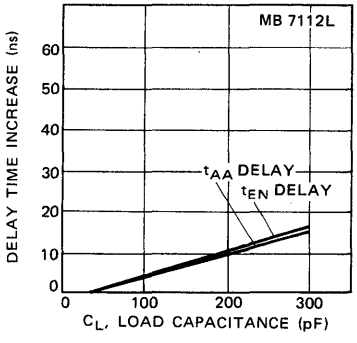


Fig. 26 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



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PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB 7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate (Fig. 27).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Groove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

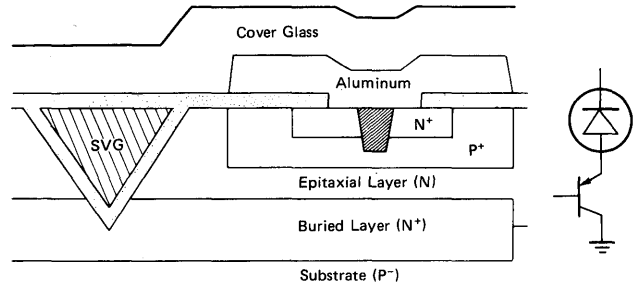
In programming, reverse current pulses are applied to the cathod of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

SPECIAL FACTORY TESTING

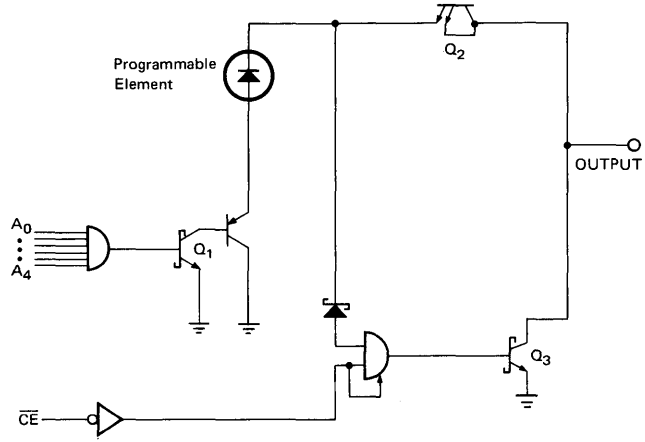
Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide en-

Fig. 27. PROGRAMMED CELL (CROSS SECTION)



Programmed by DEAP. (Diffused Eutectic Aluminum Process)

Fig. 28. INTERNAL PROGRAMMING CIRCUIT



hanced between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.
As shown in Fig. 28, transistor Q_1 is turned on to select the desired bit for programming by using five address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q_2 and memory cell into transistor Q_1. This programming current changes the programmable element to the conducting state. The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH}=2.4V and V_{CC}=7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A= 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	–	0.8	V
Input HIgh Voltage	V_{IH}		2.0	–	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	–	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	–	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

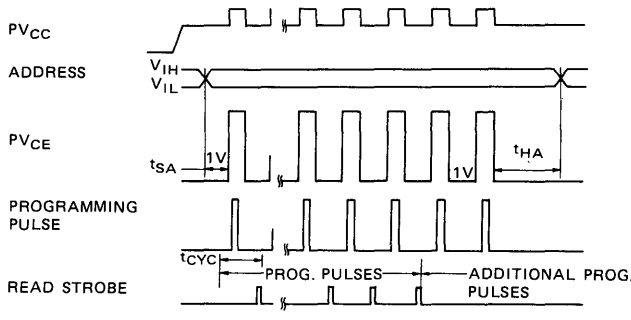
PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS ($T_A = 25°C$)

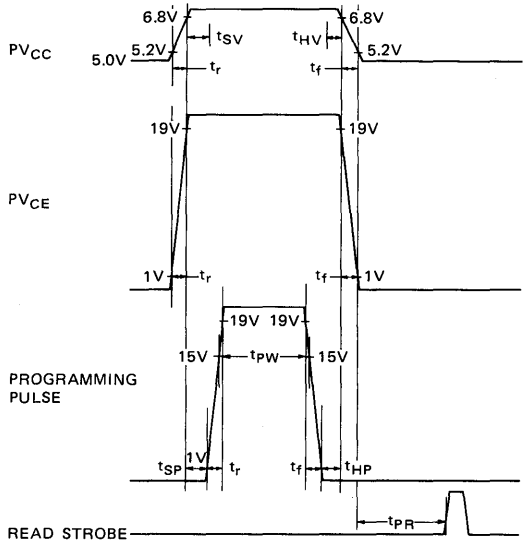
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW}(1)	10	11	12	μs
Programming Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r(3)	–	–	2	μs
Programming Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f(5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP}(6)	4	–	–	μs
PV_{CC} Pulse Set-up Time	t_{SV}	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
PV_{CE} Hold Time	t_{HP}(7)	2	–	–	μs
PV_{CC} Pulse Hold Time	t_{HV}	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(8)	10	–	–	μs
Programming Pulse Number	n	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

NOTE: (1) Stipulated 200Ω load and 15V
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



4

PROGRAMMING INFORMATION (continued)

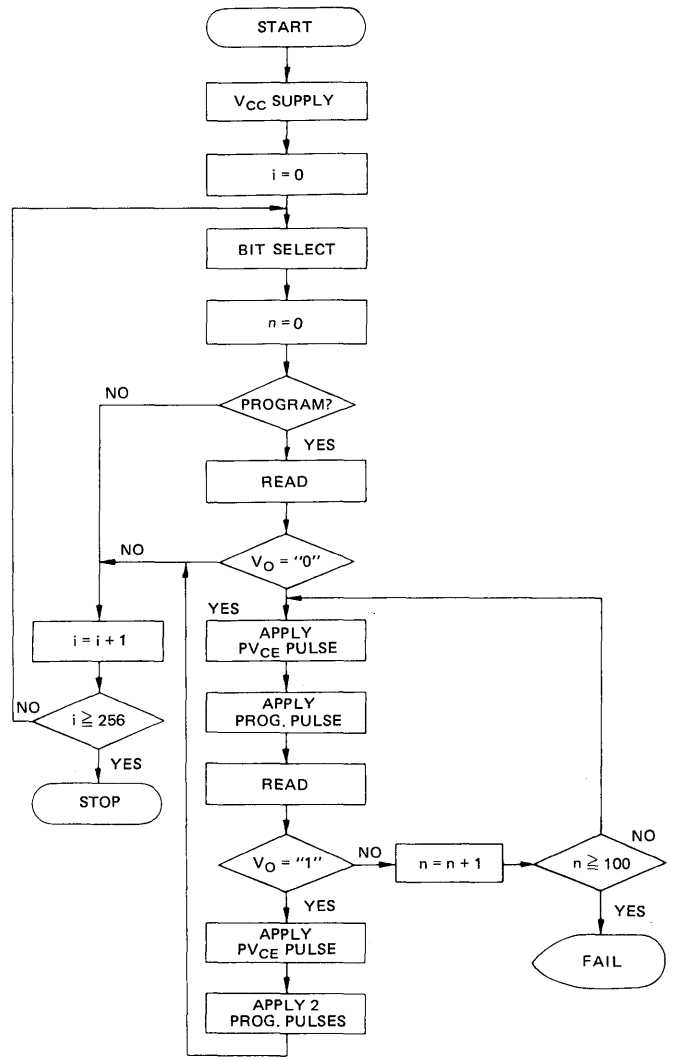
PROGRAMMING PROCEDURE

1. Apply power; $V_{CC} = PV_{CC}$, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (If V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125 mA and duration of t_{PW} (11 μs) after a delay of t_{SP} (4 μs).
6. Read the output V_O after a delay of t_{PR} (10 μs).
   a) If V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50 μs).
   b) If V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2 μs).

NOTE:

1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C ± 2°C)

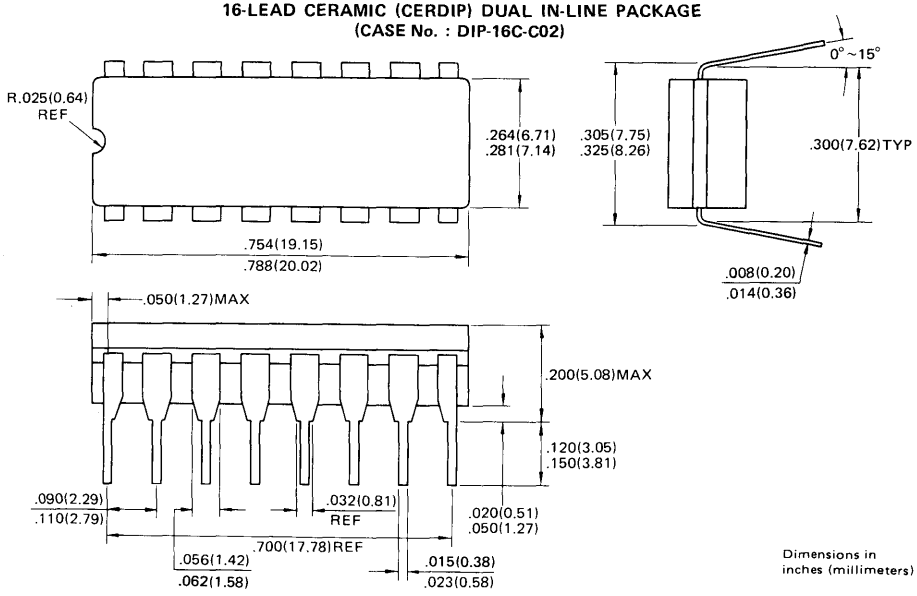
Fig. 29 — PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

Suffix (: -CZ)

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)



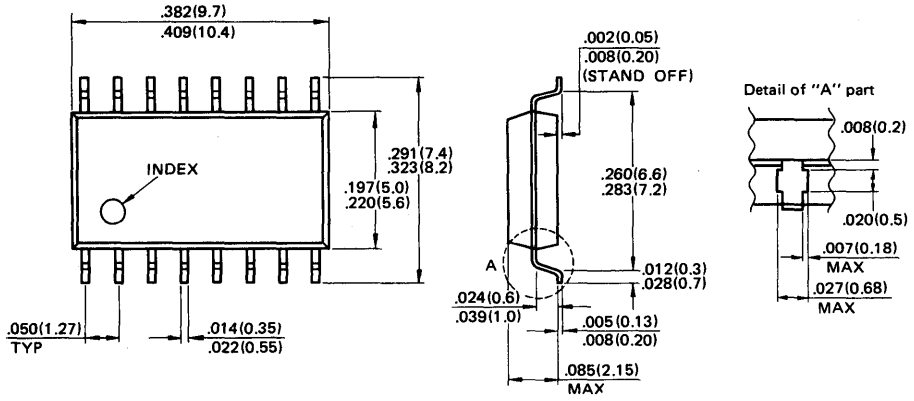
Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS

Suffix (: -M)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



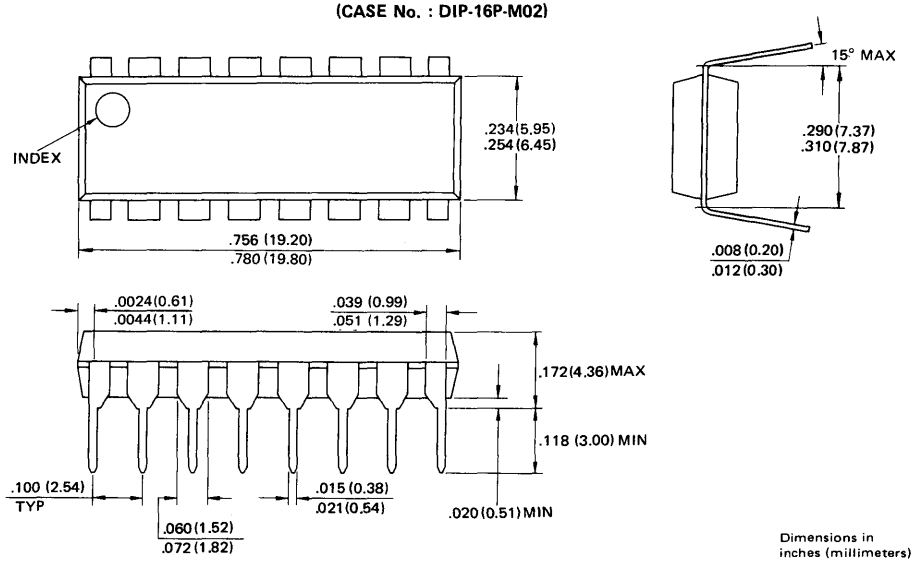
Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

Suffix (: -M)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M02)



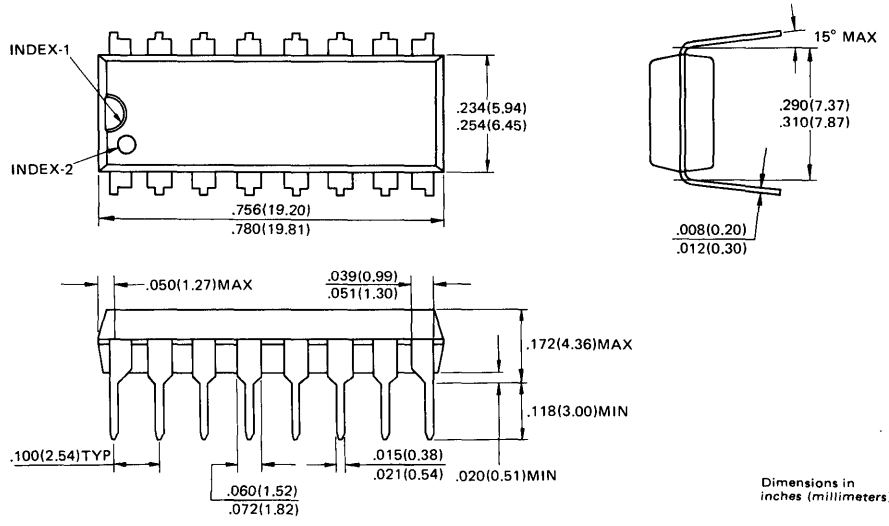
Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

Suffix (: -PF)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)

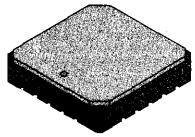


Dimensions in inches (millimeters)

4

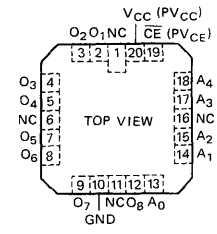
PACKAGE DIMENSIONS

Suffix (: -TV)

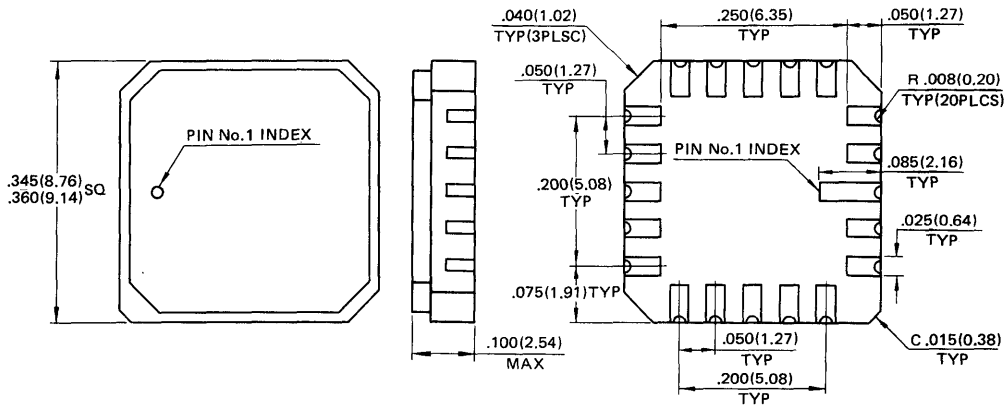


CERAMIC PACKAGE
LCC-20C-F02

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F02)



Dimension in inches
and (millimeters)

4

FUJITSU

PROGRAMMABLE SCHOTTKY 1024-BIT READ ONLY MEMORY

MB 7113E
MB 7114E/H
MB 7113L
MB 7114L

April 1986
Edition 3.0

SCHOTTKY 1024-BIT DEAP PROM (256 WORDS x 4 BITS)

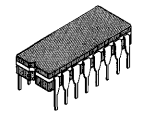
The Fujitsu MB 7113 and MB 7114 are high speed Schottky TTL electrically field programmable read only memories organized as 256 words by 4 bits. With uncommitted collector outputs provided on the MB 7113 and three-state outputs on the MB 7114, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

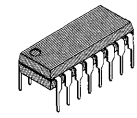
The sophisticated passive isolation termed SVG (Shallow V-Groove) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

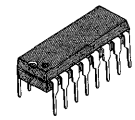
- Single +5V supply voltage.
- Power Supply Current:
  100 mA max. (E/H)
  40 mA max. (L)
- 256 words x 4 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time, 20ns typ.
  H: 30ns max.
  E: 40ns max.
- Fast access time, 35ns typ.
  L: 50ns max.
- TTL compatible inputs and outputs.
- Open collector outputs (MB 7113)
- 3-state outputs (MB 7114)
- Two chip enable leads for simplified memory expansion.
- Standard 16 pin Ceramic (Cerdip) DIP (Suffix: -CZ)
- Standard 16 pin Plastic DIP (Suffix: -P)
  Standard 16 pin Plastic FPT (Suffix: -PF)
  Standard 20 pad Ceramic LCC (Suffix: -TV)
- JEDEC approved



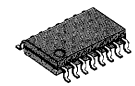
CERAMIC PACKAGE
DIP-16C-C02



PLASTIC PACKAGE
DIP-16P-M02



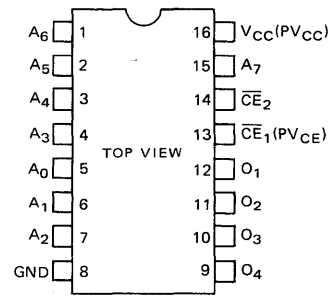
PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

LCC-20C-F02: See Page 18

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 18

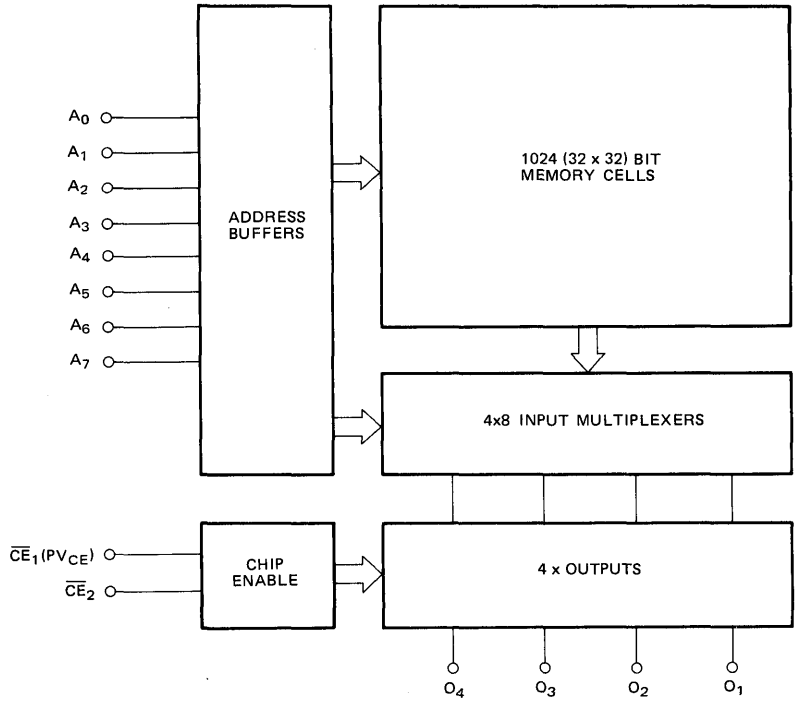
ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CC}	−0.5 to +7.5	V
Input Voltage		V_{IN}	−1.5 to +7.5	V
Input Voltage (during programming)		V_{IPRG}	22.5	V
Output Voltage (during programming)		V_{OPRG}	−0.5 to +22.5	V
Input Current		I_{IN}	−20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+150	mA
Storage Temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Output Voltage		V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 – MB 7113/7114 BLOCK DIAGRAM



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CAPACITANCE ($f = 1MHz$, $V_{CC} = +5V$, $V_{IN} = +2V$, $T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	12	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	5.5	V
Ambient Temperature	T_A	0	–	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	μA
Output Low Voltage (I_{OL} = 10mA)		V_{OL}			0.45	V
Output Low Voltage (I_{OL} = 16mA)		V_{OL}			0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)	MB 7113	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4V, chip disabled)	MB 7114	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.45V, chip disabled)	MB 7114	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	E/H	I_{CC}		60**	100	mA
	L			25	40	
Output High Voltage (I_O = -2.4mA)	MB 7114	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB 7114	I_{OS}*	-15		-60	mA

Note: * Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4 V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.
**This value denotes conditions at T_A = 25°C and V_{CC} = +5.0V.

4

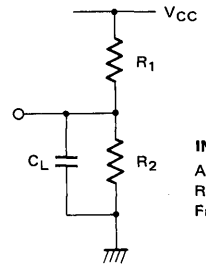


Fig. 2 – AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude . . . . . .0V to 3V
Rise and Fall Time . . . . . .5ns from 1V to 2V
Frequency 1MHz

	MB 7113/MB 7114		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

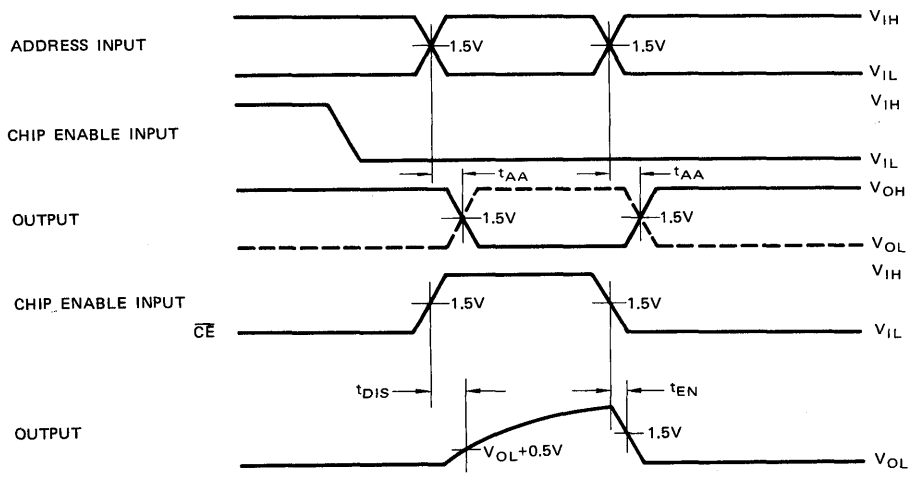
AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	MB 7114H		E		L		Unit
		Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	20	30	20	40	35	50	ns
Output Disable Time	t_{DIS}	15	25	15	25	25	40	ns
Output Enable Time	t_{EN}	15	25	15	25	25	40	ns

4

OPERATION TIMING DIAGRAM



Note: Output disable time is the time taken for the output to reach a high impedance state when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when the chip enables are taken enable. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7114 (3-state) compared to 0mA for the MB 7113 (open-collector)

THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists

Fig. 3 – MB 7113/7114 INPUT

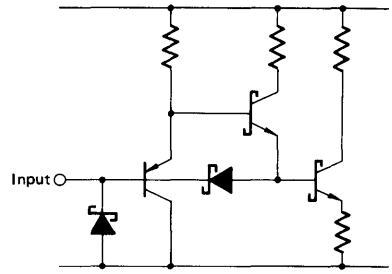


Fig. 4 – MB 7113L/7114L INPUT

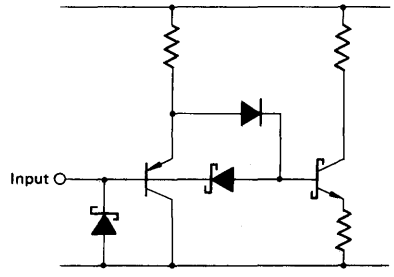
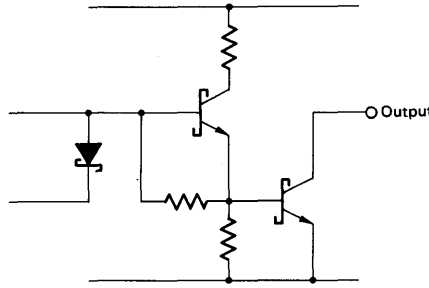


Fig. 5 – MB 7113 OUTPUT



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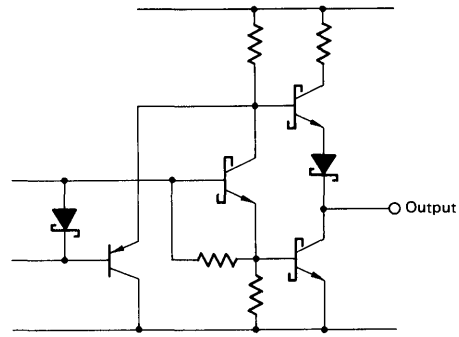
that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions in unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 6 – MB 7114 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 7 – I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

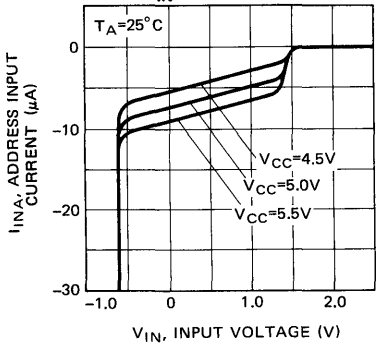

Fig. 8 – I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

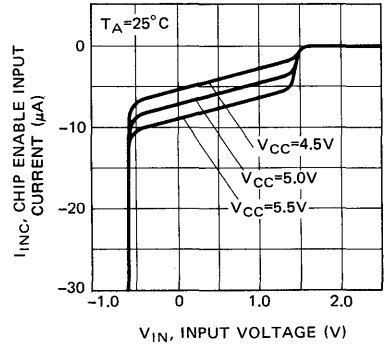

Fig. 9 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

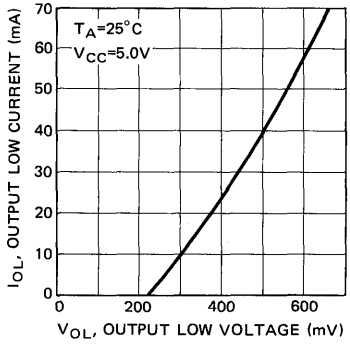

Fig. 10 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

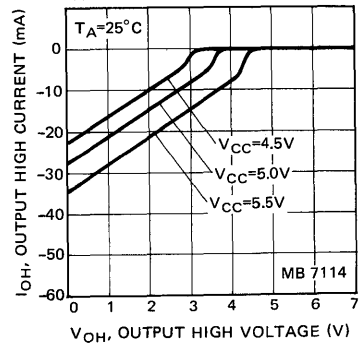

Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

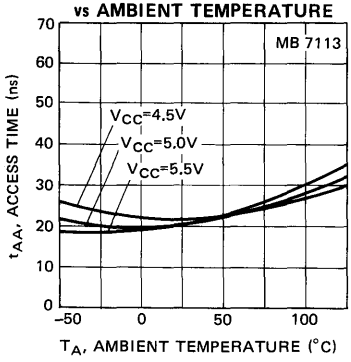

Fig. 12 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

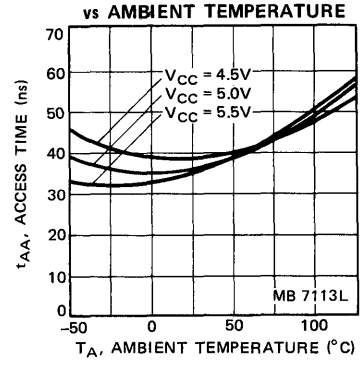

Fig. 13 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

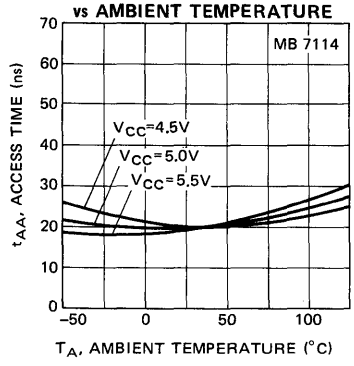

Fig. 14 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

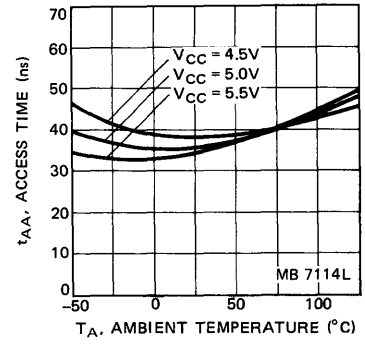

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Fig. 15 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

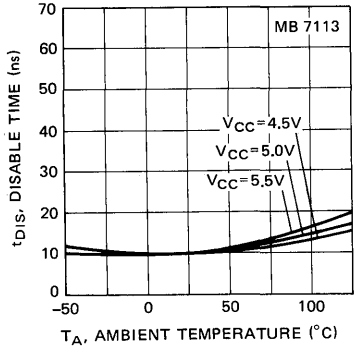

Fig. 16 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

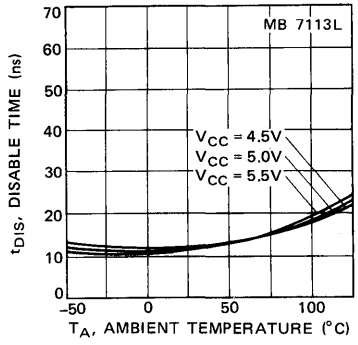

Fig. 17 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

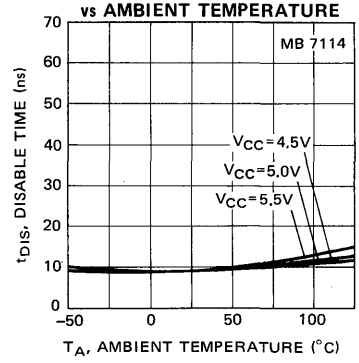

Fig. 18 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

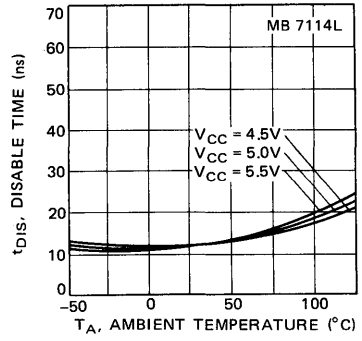

Fig. 19 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

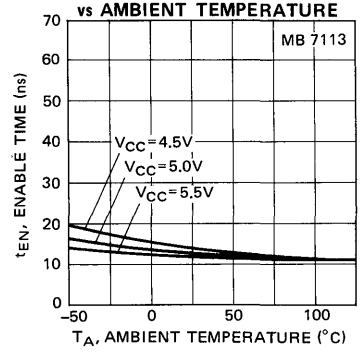

Fig. 20 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

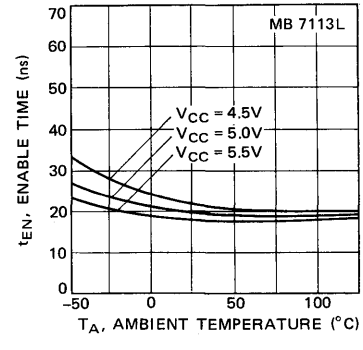

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Fig. 21 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

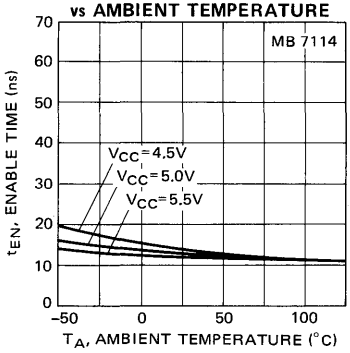


Fig. 22 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

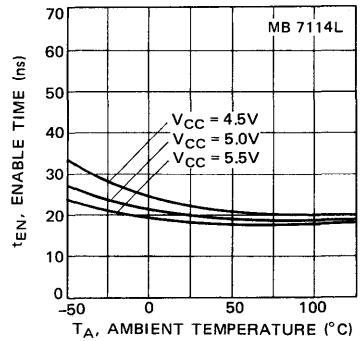


Fig. 23 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

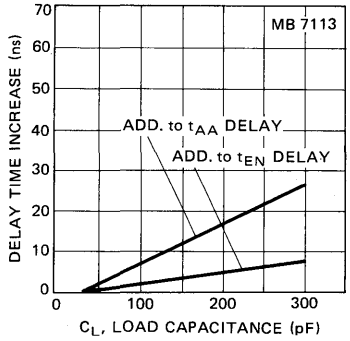


Fig. 24 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

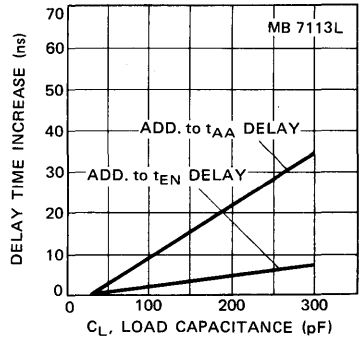


Fig. 25 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

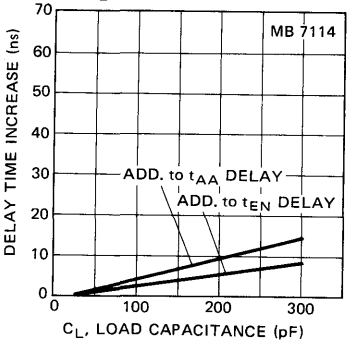
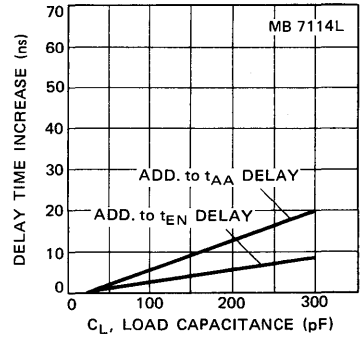


Fig. 26 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



4

PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB 7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate (Fig. 27).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Groove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

SPECIAL FACTORY TESTING

Extra rows and extra columns of test

Fig. 27 – PROGRAMMED CELL (CROSS SECTION)

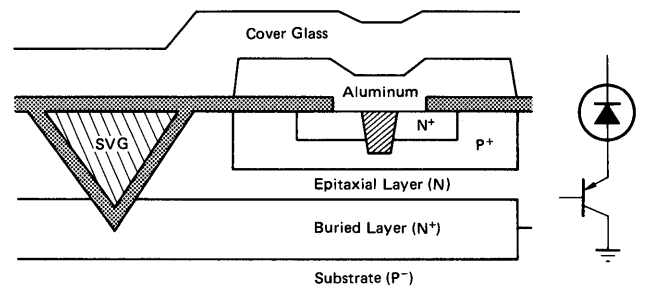
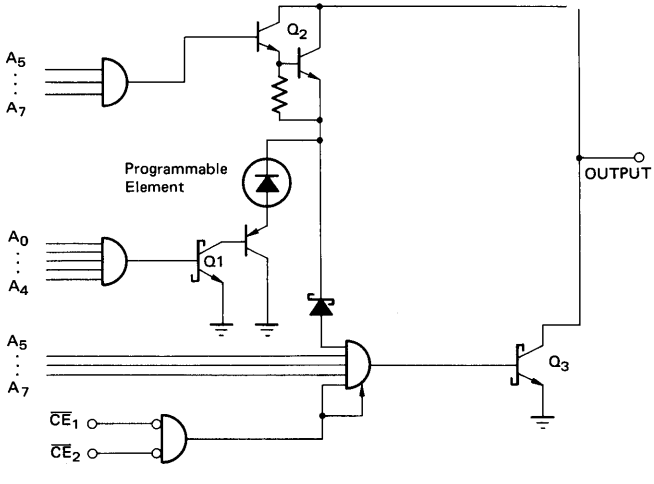


Fig. 28 – INTERNAL PROGRAMMING CIRCUIT



cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

"As shown in Fig. 28, transistors, Q_1 and Q_2, are turned on to select the desired bit for programming by using eight address inputs'. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q_2 and memory cell into transistor Q_1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking all chip enable inputs low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4 mA at V_{OH} = 2.4V and V_{CC} = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	–	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	–	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

PROGRAMMING INFORMATION (Cont'd)

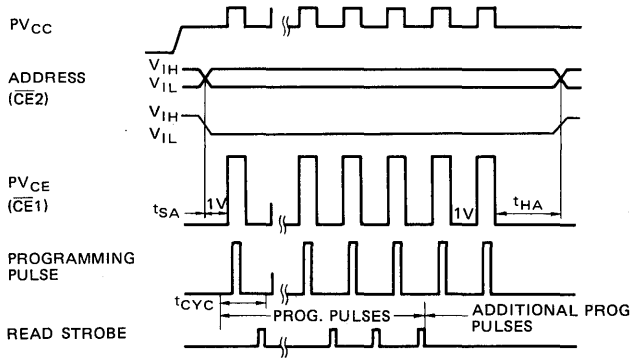
AC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW}(1)	10	11	12	μs
Programming Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r(3)	–	–	2	μs
Programming Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f(5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP}(6)	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
PV_{CE} Hold Time	t_{HP}(7)	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(8)	10	–	–	μs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

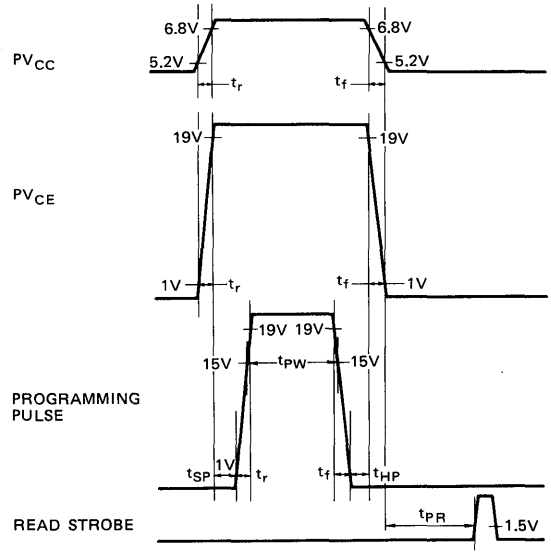
Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

4

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



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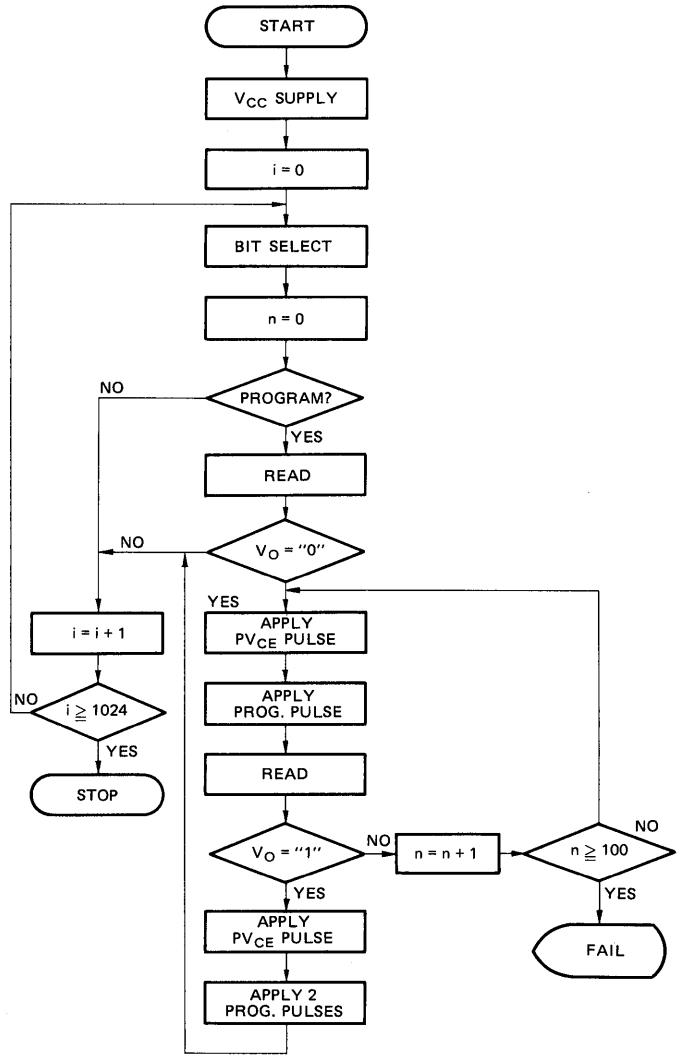
PROGRAMMING INFORMATION (Cont'd)

PROGRAMMING PROCEDURE

1. Apply power; V_{CC}=PV_{CC}, GND= 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O=low. (In the case of V_O=high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125mA and duration of t_{PW} (11μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O=low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O=high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

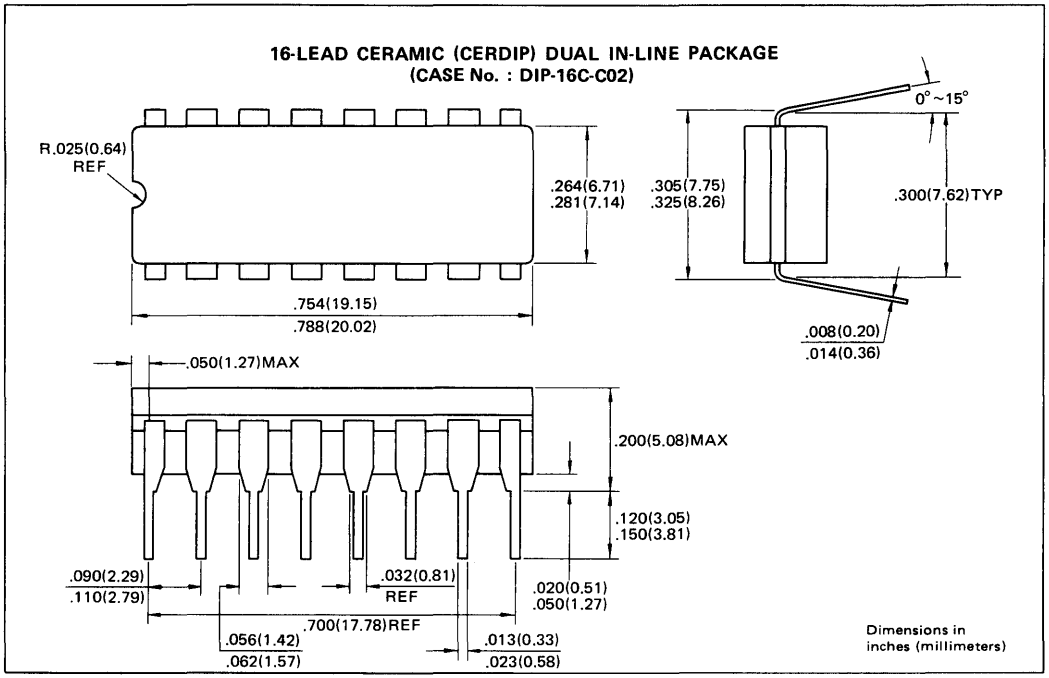
Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

Fig. 29 — PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)



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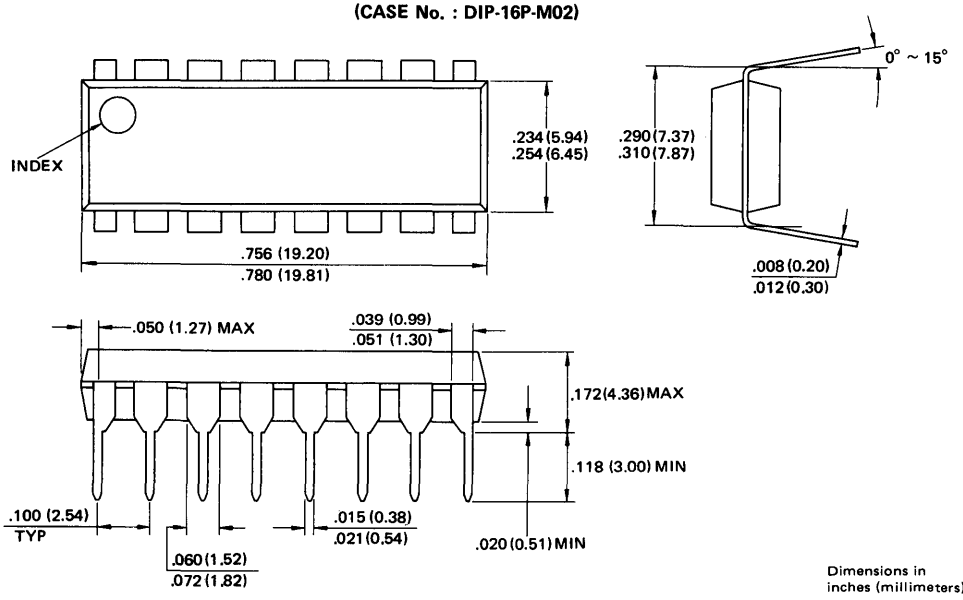
PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M02)



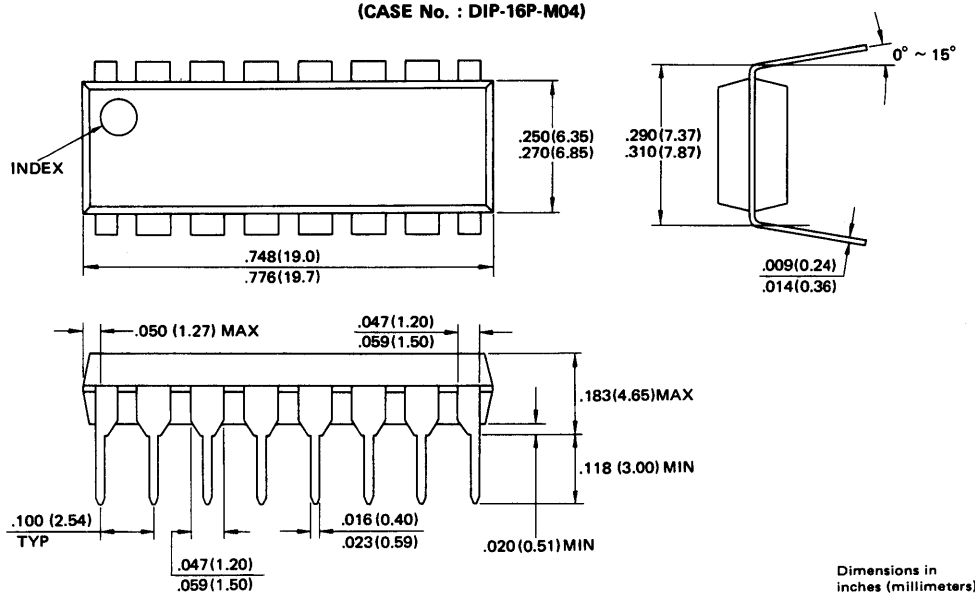
Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



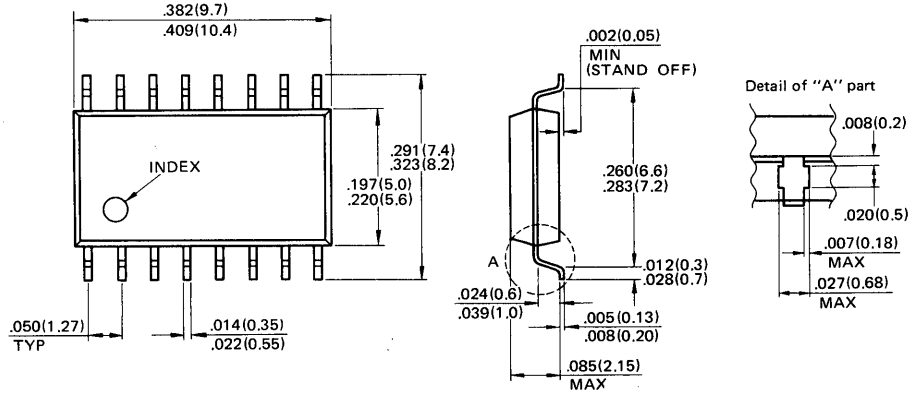
Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS

PLASTIC FPT (Suffix: -PF)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)

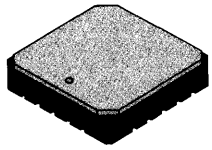


Dimensions in
inches (millimeters)

4

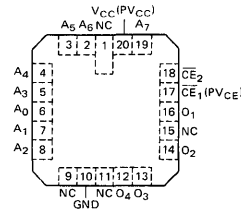
PACKAGE DIMENSIONS

CERAMIC LCC (Suffix: -TV)

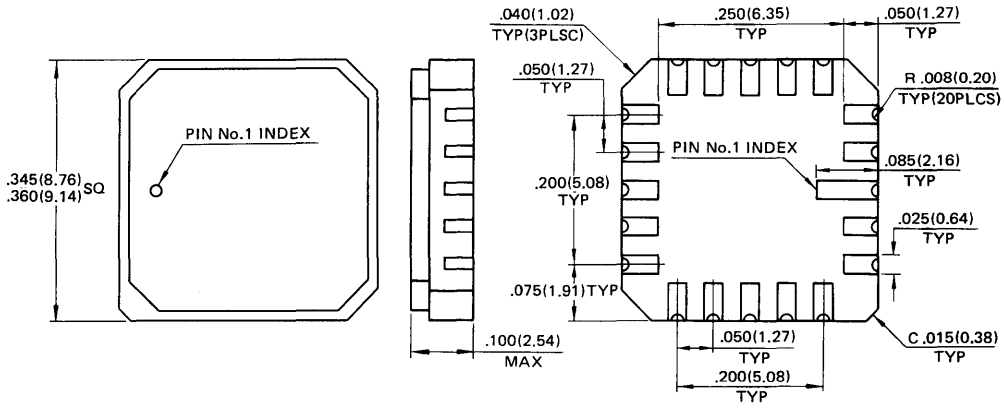


LCC-20C-F02

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-20C-F02)



Dimension in inches
and (millimeters)

4

FUJITSU

PROGRAMMABLE SCHOTTKY 2048-BIT READ ONLY MEMORY

MB7115E/H
MB7116E/H/Y
MB7115L
MB7116L

November 1987
Edition 2.0

SCHOTTKY 2048-BIT DEAP PROM (512 WORDS x 4 BITS)

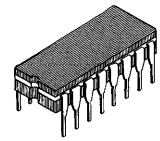
The Fujitsu MB 7115 and MB 7116 are high speed Schottky TTL electrically field programmable read only memories organized as 512 words by 4 bits. With uncommitted collector outputs provided on the MB 7115 and three-state outputs on the MB 7116, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

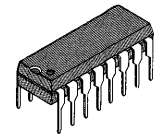
The sophisticated passive isolation termed SVG (Shallow V-Groove) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

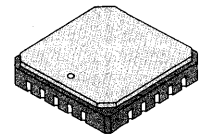
- Single +5V supply voltage.
- 512 words x 4 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programing.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time
  - Y : 20ns typ, 30ns max.
  - H : 20ns typ, 35ns max.
  - E : 20ns typ, 45ns max.
  - L : 40ns typ, 60ns max.
- TTL compatible inputs and outputs.
- Open collector outputs (MB7115)
- 3-state outputs (MB7116)
- Chip enable lead for simplified memory expansion.
- Standard 16 pin Ceramic (Cerdip) DIP (Suffix: –Z)
- Standard 16 pin Plastic DIP (Suffix: –M)
- Standard 20 pad Ceramic (Frit Seal) LCC (Suffix: –TV)
- JEDEC approved pin out.



CERAMIC PACKAGE
DIP-16C-C02

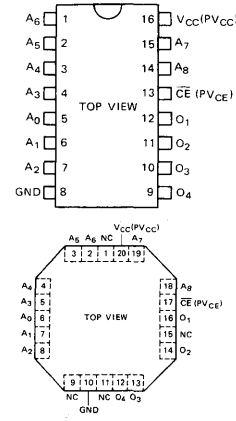


PLASTIC PACKAGE
DIP-16P-M04



CERAMIC PACKAGE
LCC-20C-F02

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

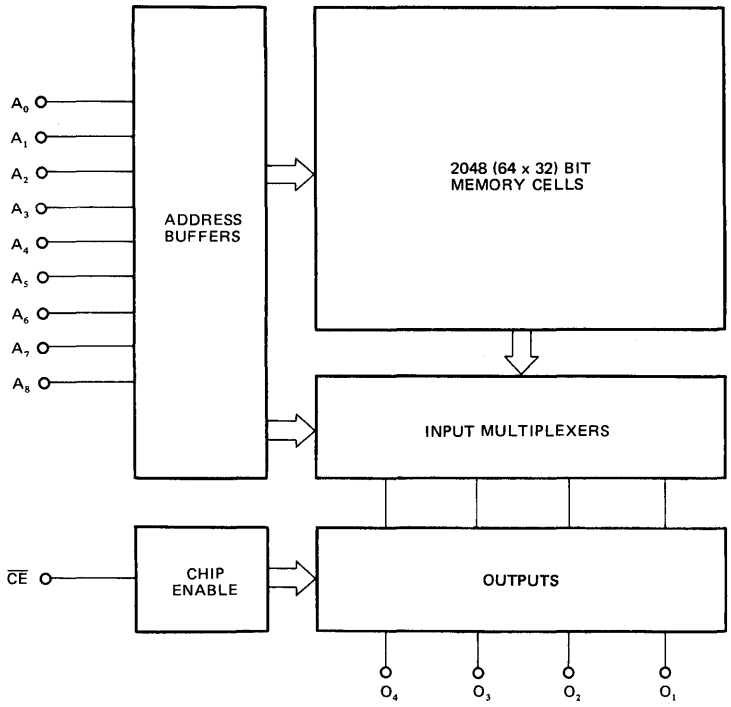
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CCP}	-0.5 to +7.5	V
Input Voltage		V_{IN}	-1.5 to +5.5	V
Input Voltage (during programming)		V_{IPRG}	22.5	V
Output Voltage (driung programming)		V_{OPRG}	-0.5 to +22.5	V
Input Current		I_{IN}	- 20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+150	mA
Storage Temperature	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-40 to +125	
Output Voltage		V_{OUT}	-0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

Fig. 1 – MB 7115/7116 BLOCK DIAGRAM



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CAPACITANCE (f=1MHz, V_{CC}=+5V, V_{IN}=+2V, T_A=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	12	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	5.5	V
Ambient Temperature	T_A	0	–	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

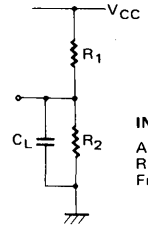
Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	μA
Output Low Voltage (I_{OL} = 10mA)		V_{OL}			0.45	V
Output Low Voltage (I_{OL} = 16mA)		V_{OL}			0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)	MB 7115	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4V, chip disabled)	MB 7116	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.5V, chip disabled)	MB 7116	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	E/H/Y	I_{CC}		70**	120	mA
	L			40**	50	
Output High Voltage (I_O = -2.4mA)	MB 7116	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB 7116	I_{OS}*	-15		-60	mA

Note: * Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$=0.4 V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

** This value denotes conditions at T_A=25°C and V_{CC} =+5.0V

4

Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

	MB 7115/MB 7116		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

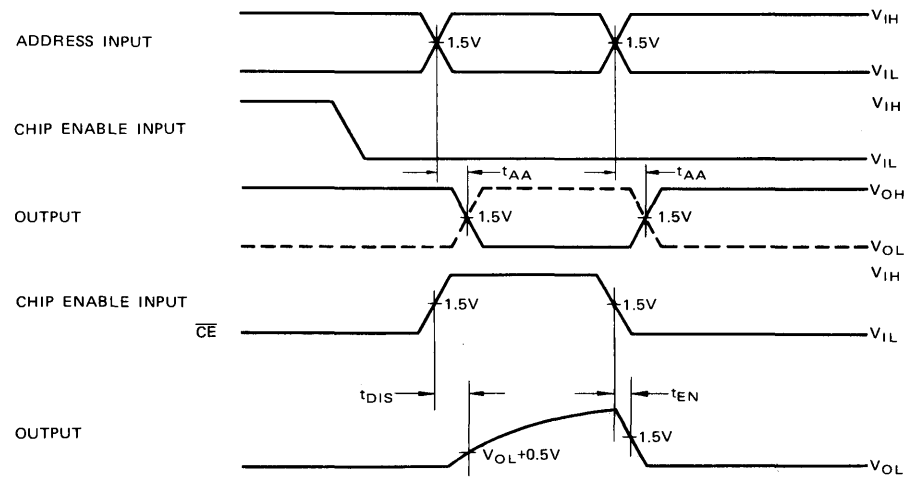
AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	L		E		H		MB7116Y		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	40*	60**	20	45	20	35	20	30	ns
Output Disable Time	t_{DIS}	20	50	15	30	15	30	10	25	ns
Output Enable Time	t_{EN}	30	50	15	30	15	30	15	25	ns

(*7115L: 45ns **7115L: 70ns)

OPERATION TIMING DIAGRAM



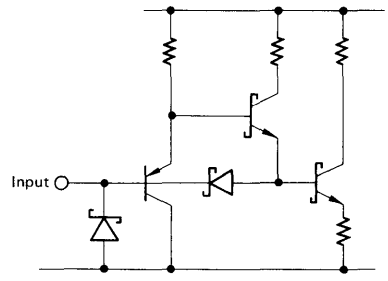
Note: Output disable time is the time taken for the output to reach a high impedance state when the chip enable is taken disable. Output enable time is the time taken for the output to become active when the chip enable is taken enable. The high impedance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

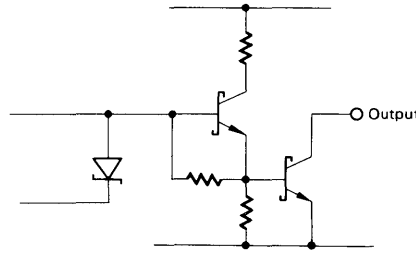
Fig. 3 – MB 7115/7116 INPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7116 (3-state) compared to 0mA for the MB 7115 (open-collector).

Fig. 4 – MB 7115 OUTPUT



THREE-STATE OUTPUT

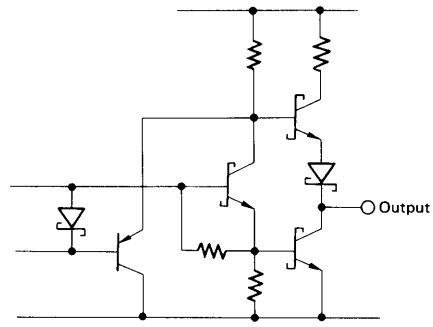
A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists

that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB 7116 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

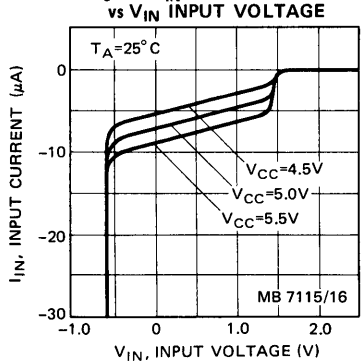

Fig. 7 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

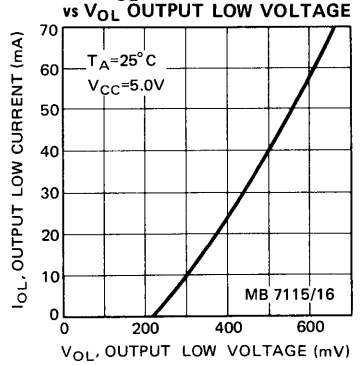

Fig. 8 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

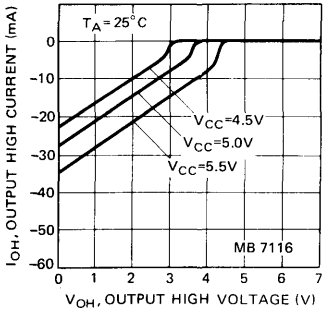

Fig. 9 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

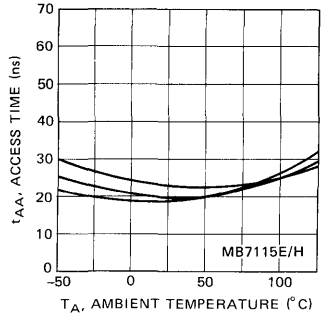

Fig. 10 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

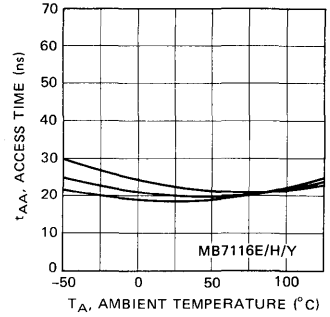

Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

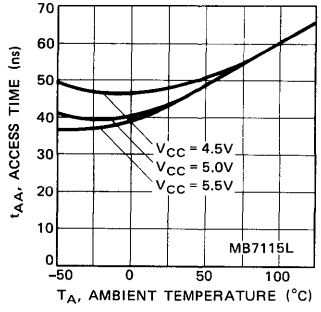

Fig. 12 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

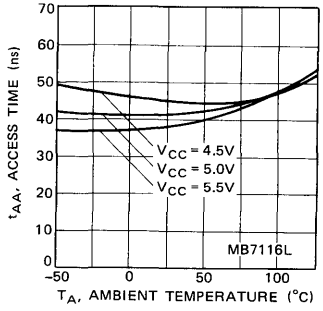

Fig. 13 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

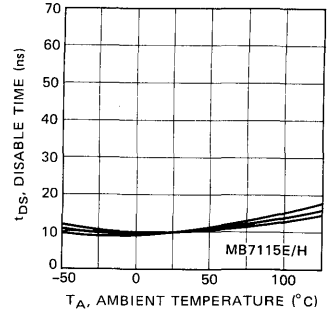

Fig. 14 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

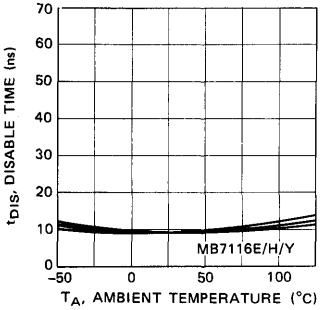

Fig. 15 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

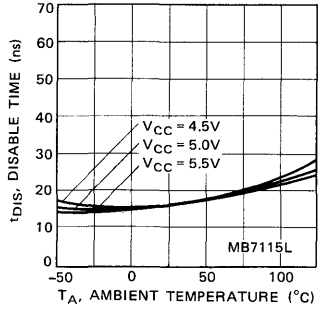

Fig. 16 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

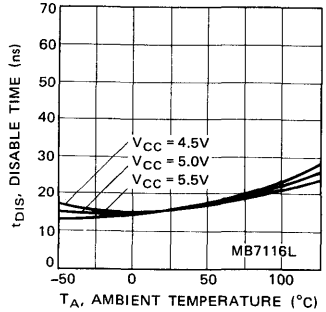

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Fig. 17 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

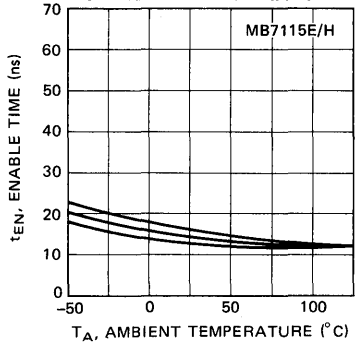


Fig. 18 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

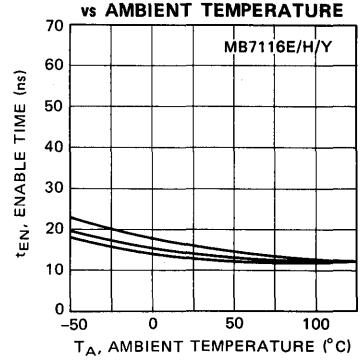


Fig. 19 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

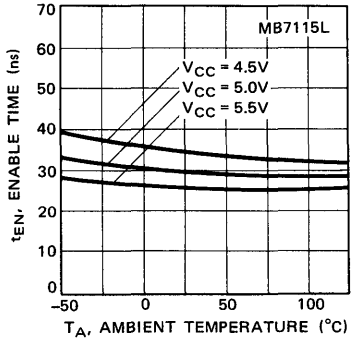


Fig. 20 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

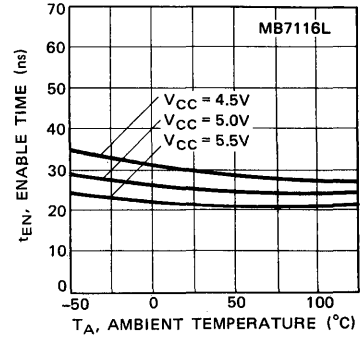


Fig. 21 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

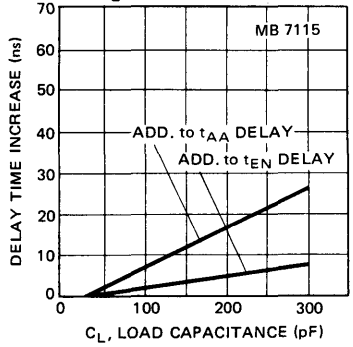
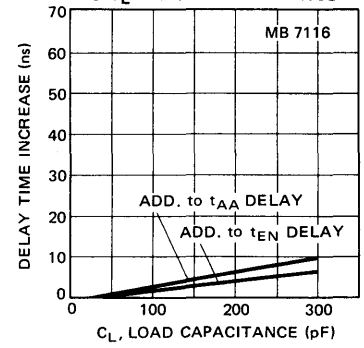


Fig. 22 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



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PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

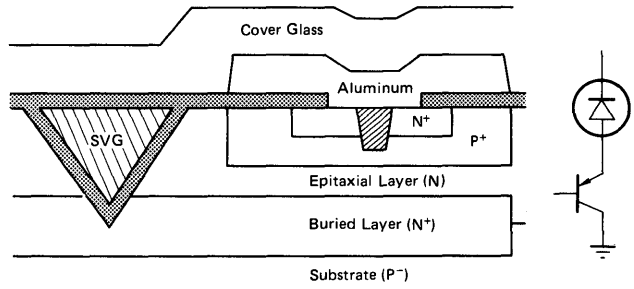
The Fujitsu MB 7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate (Fig. 23).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Groove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathod of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

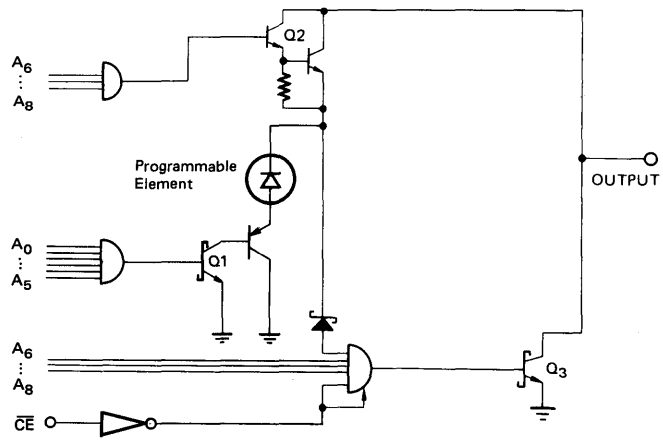
Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

Fig. 23— PROGRAMMED CELL (CROSS SECTION)



Programmed by DEAP (Diffused Eutectic Aluminum Process)

Fig. 24— INTERNAL PROGRAMMING CIRCUIT



4

PROGRAMMING INFORMATION (continued)

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

"As shown in Fig. 24, transistors, Q_1 and Q_2, are turned on to select the desired bit for programming by using ten address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q_2 and memory cell into transistor Q_1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH} = 2.4V and V_{CC} = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		110	120	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	–	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS (T_A = 25°C)

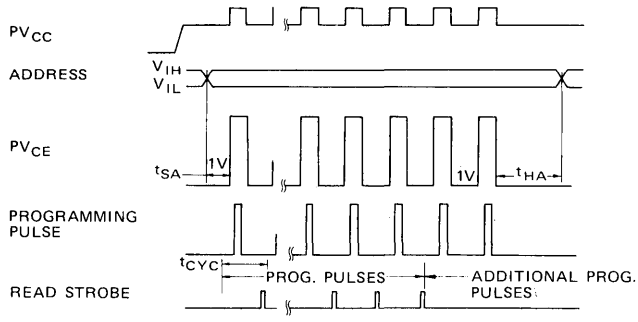
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW}(1)	10	11	12	μs
Programming Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r(3)	–	–	2	μs
Programming Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f(5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP}(6)	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
PV_{CE} Hold Time	t_{HP}(7)	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(8)	10	–	–	μs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

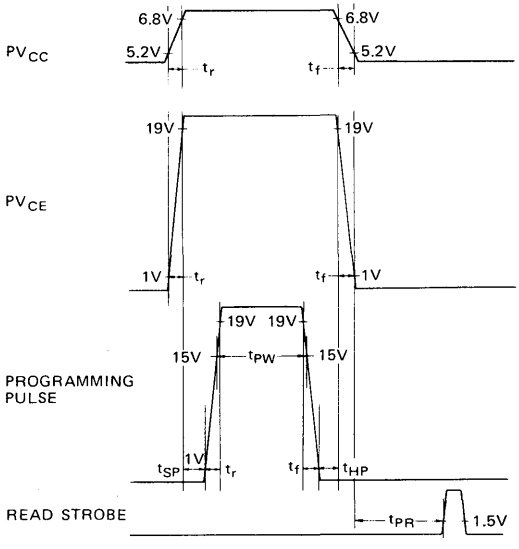
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE

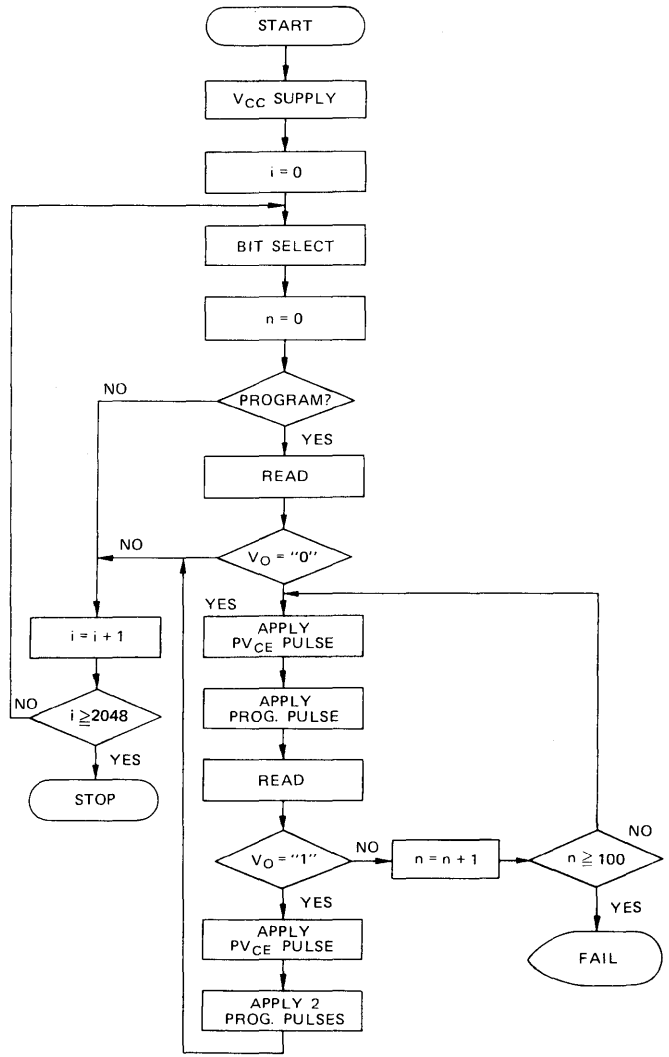


PROGRAMMING PROCEDURE

1. Apply power; V_{CC}=PV_{CC}, GND= 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O=low. (In the case of V_O=high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125 mA and duration of t_{PW} (11μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O=low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O=high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

Fig. 25 – PROGRAMMING FLOW CHART

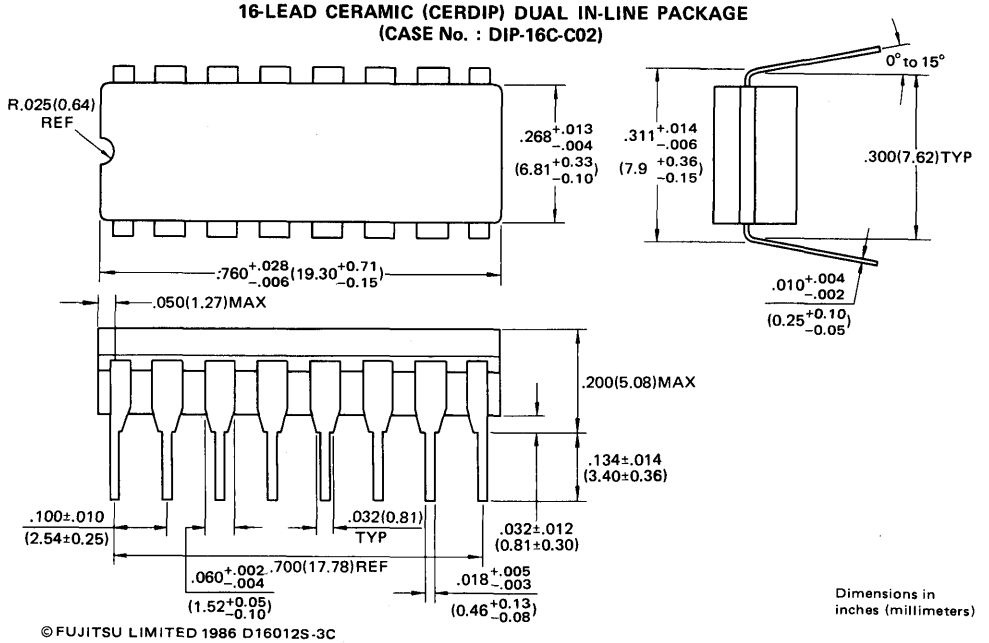


4

PACKAGE DIMENSIONS

(Suffix: -Z)

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)



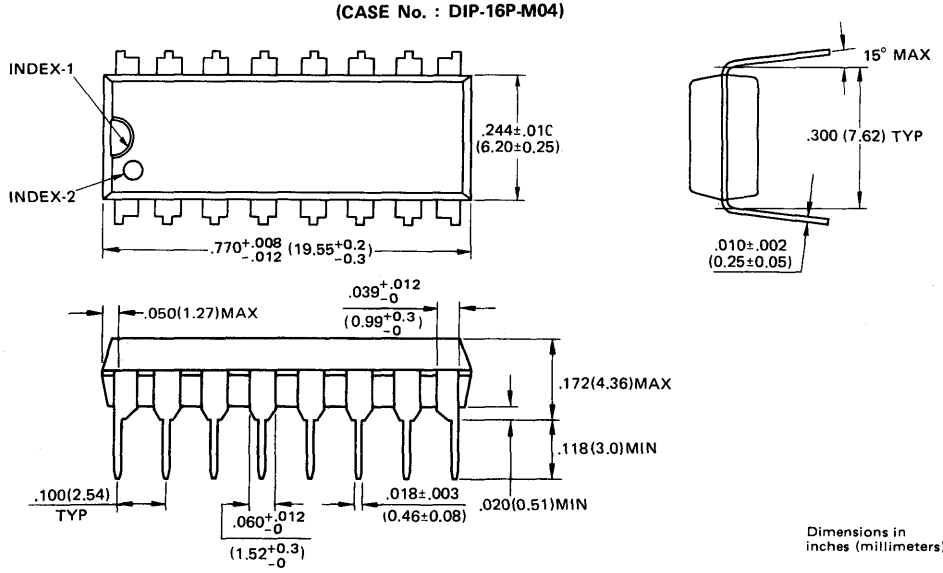
Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

(Suffix: -M)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)

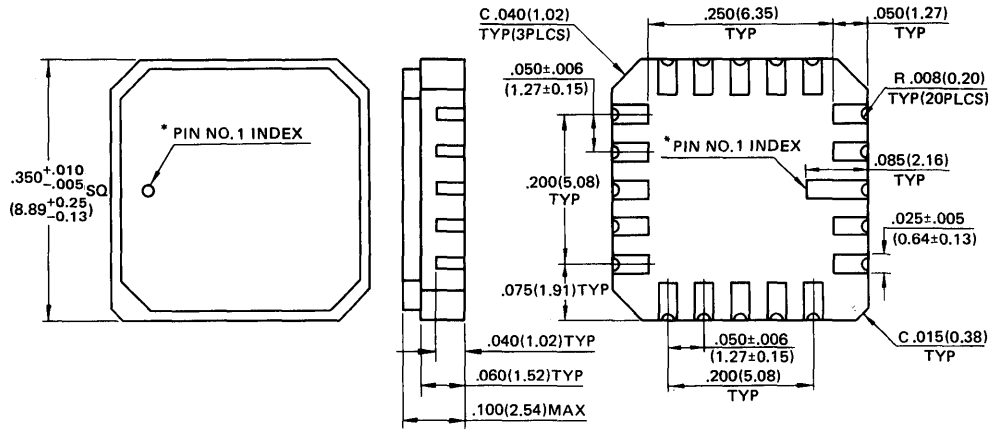


4

PACKAGE DIMENSIONS

(Suffix: -TV)

20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE NO.: LCC-20C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in
inches (millimeters)

4

FUJITSU

PROGRAMMABLE SCHOTTKY 2048 READ ONLY MEMORY

MB 7117E/H
MB 7118E/H
MB 7117L
MB 7118L

June 1987
Edition 2.0

SCHOTTKY 2048 BIT DEAP PROM (256 WORDS X 8 BITS)

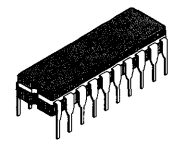
The Fujitsu MB 7117 and MB 7118 are high speed schottky TTL electrically field programmable read only memories organized as 256 words by 8-bits. With uncommitted collector outputs provided on the MB 7117 and three-state outputs on the MB 7118 memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable Deap (Diffused Eutectic Aluminum Process) according to simple programming procedures.

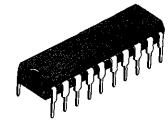
The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

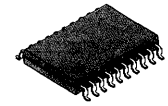
- Single +5V supply voltage.
- 256 words x 8 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by Deap (diffused eutectic aluminum process).
- Simplified and lower power programming.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing
- Fast access time
  H: 25ns typ, 35ns max
  E: 25ns typ, 45ns max
  L: 35ns typ, 60ns max
- TTL compatible inputs and outputs.
- Open collector outputs (MB 7117)
- 3-state outputs (MB 7118)
- Two chip enable leads for simplified memory expansion.
- Standard 20 pin Ceramic (Cerdip) DIP (Suffix: -Z)
- Standard 20 pin Plastic DIP (Suffix: -M)
- Standard 20 pin Plastic FPT (Suffix: -PF)
- Standard 20 pad Ceramic LCC (Suffix: -TV)
- JEDEC approved pin out



CERAMIC PACKAGE
DIP-20C-C01



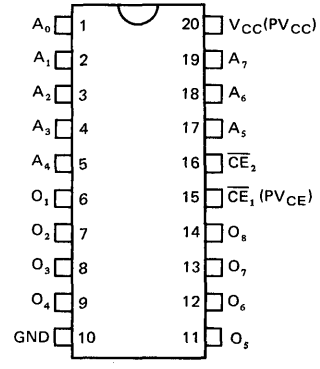
PLASTIC PACKAGE
DIP-20P-M02



PLASTIC PACKAGE
FPT-20P-M02

LCC-20C-F02: See page 16

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

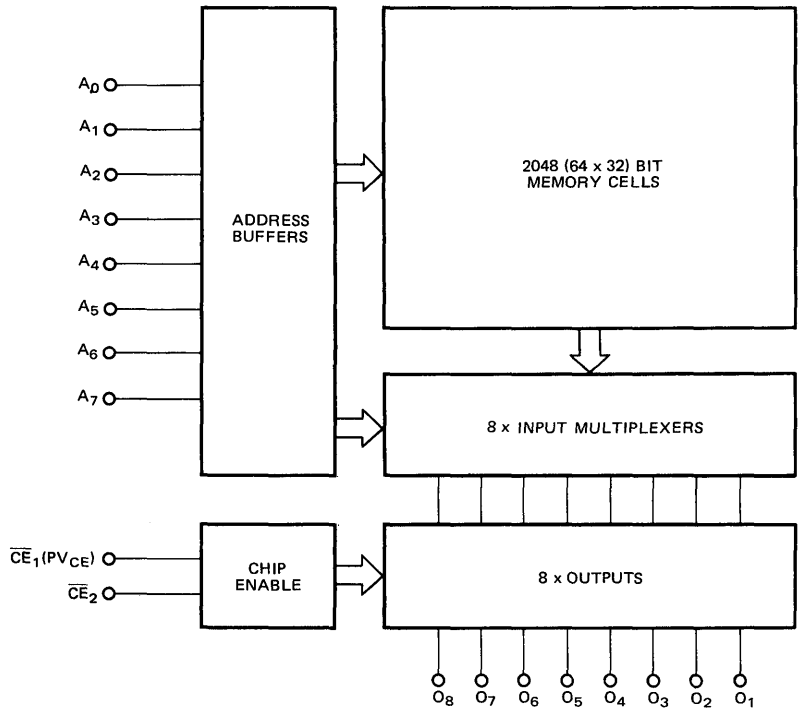
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CCP}	-0.5 to +7.5	V
Input Voltage		V_{IN}	-1.5 to +5.5	V
Input Voltage (during programming)		V_{PRG}	22.5	V
Output Voltage (during programming)		V_{PRG}	-0.5 to +22.5	V
Input Current		I_{IN}	- 20	mA
Input Current (during programming)		I_{PRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{PRG}	+150	mA
Storage Temperature	Ceramic	T_{stg}	-65 to +150	°C
	Plastic		-40 to +125	
Output Voltage		V_{OUT}	-0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – MB 7117 / 7118 BLOCK DIAGRAM



CAPACITANCE (f=1MHz, V_{CC}=+5V, V_{IN}=+2V, T_A=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	12	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	5.5	V
Ambient Temperature	T_A	0	–	75	°C

DC CHARACTERISTICS

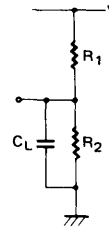
(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 4.5V)		I_{R1}			40	μA
Input Leakage Current (V_{IH} = 5.5V)		I_{R2}			1.0	mA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	μA
Output Low Voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output Low Voltage (I_{OL} = 16mA)		V_{OL}			0.50	V
Output Leakage Current (V_O = 2.4V, Chip disabled)	MB 7117	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4V, chip disabled)	MB 7118	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.45V, chip disabled)	MB 7118	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	E/H	I_{CC}		80	140	mA
	L			60	75	
Output High Voltage (I_O = -2.4mA)	MB 7118	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB 7118	I_{OS}*	-15		-60	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{ICE}}$=0.4V) and the programmed bit is addressed. These characteristics cannot be tested pior to programming, but are guaranteed by factor testing.

4

Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

	MB 7117 / MB 7118		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

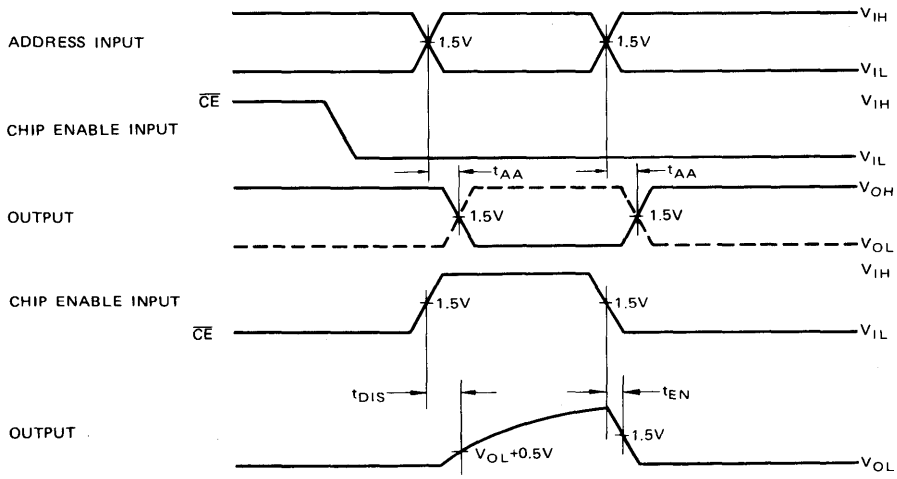
AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	L		E		H		Unit
		Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	35	60	25	45	25	35	ns
Output Disable Time	t_{DIS}	20	40	15	30	15	30	ns
Output Enable Time	t_{EN}	20	40	15	30	15	30	ns

4

OPERATION TIMING DIAGRAM



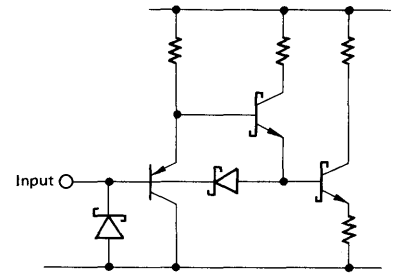
Note: Output disable time is the time taken for the output to reach a high resistance state when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

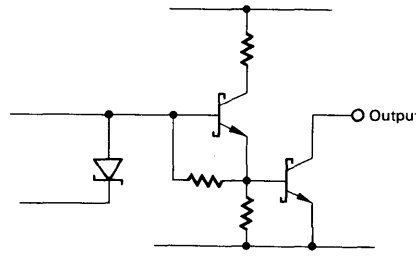
Fig. 3 – MB 7117/7118 INPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7118 (3-state) compared to 0mA for the MB 7117 (open-collector)

Fig. 4 – MB 7117 OUTPUT



THREE-STATE OUTPUT

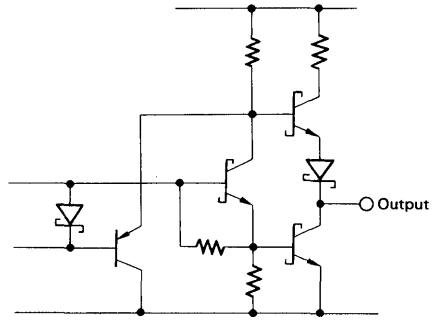
A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists

that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB 7118 OUTPUT



TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

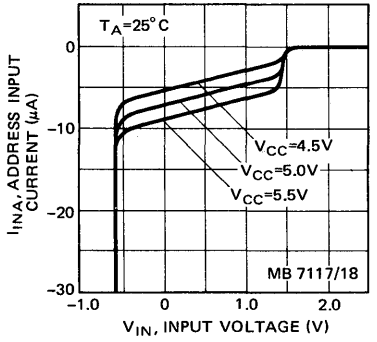


Fig. 7 – I_{INC} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

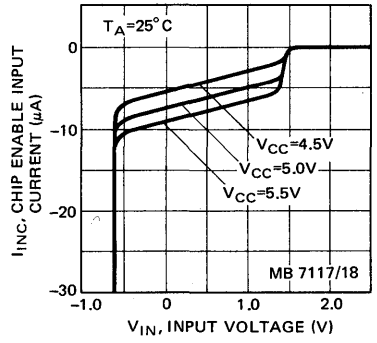


Fig. 8 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

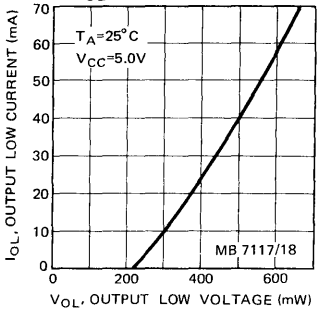


Fig. 9 – I_{OH} OUTPUT HIGH CURRENT vis V_{OH} OUTPUT HIGH VOLTAGE

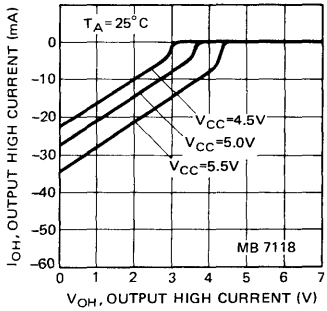


Fig. 10 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

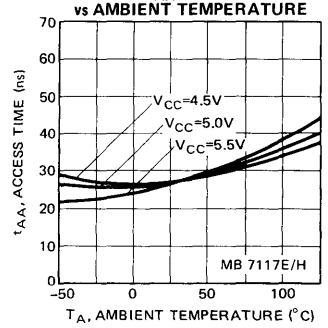


Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

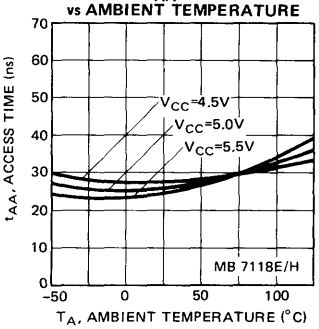


Fig. 12 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE

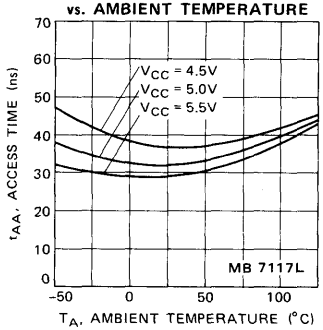


Fig. 13 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE

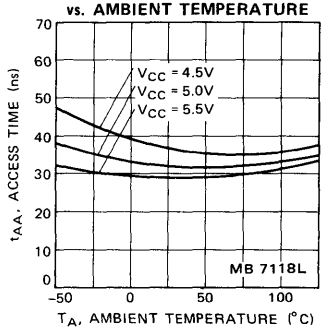


Fig. 14 – t_{DS} DISABLE TIME vs AMBIENT TEMPERATURE

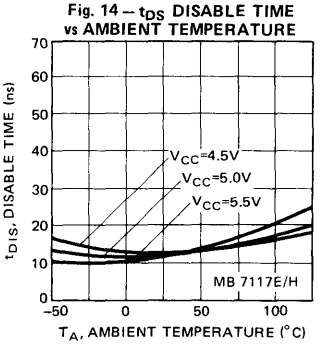
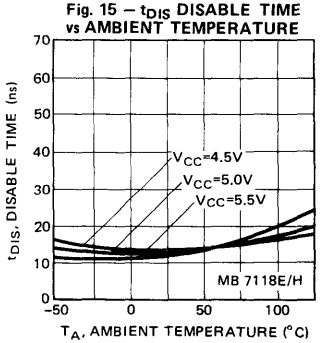


Fig. 15 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE



4

Fig. 16 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

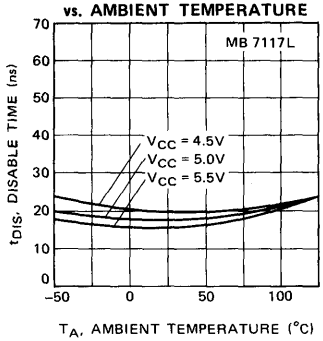


Fig. 17 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

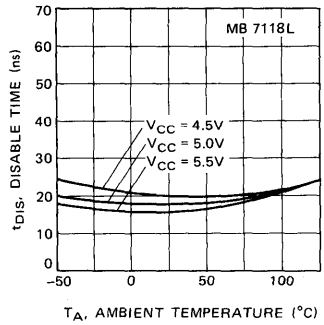
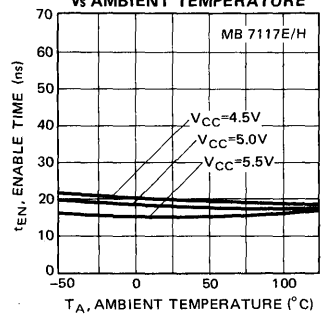


Fig. 18 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE



4

Fig. 19 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

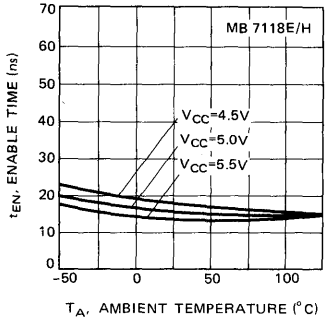


Fig. 20 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE

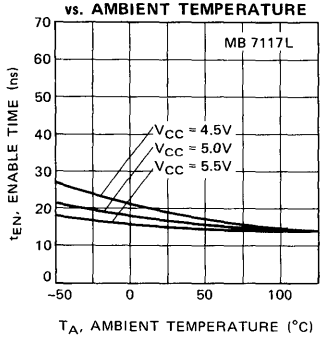


Fig. 21 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE

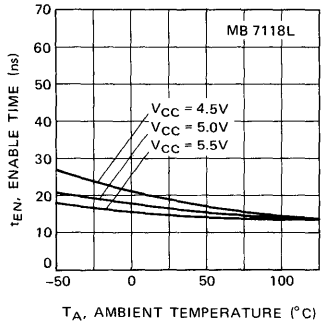


Fig. 22 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

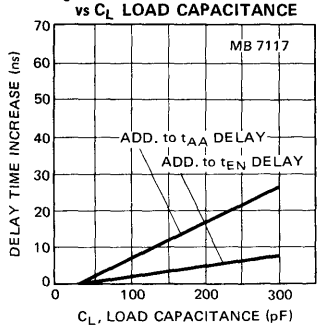
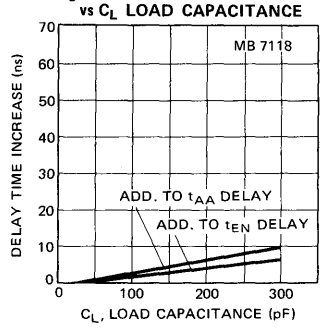


Fig. 23 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB 7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate (Fig. 24).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Groove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

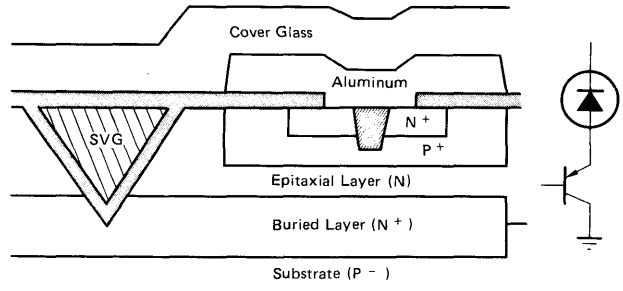
In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

SPECIAL FACTORY TESTING

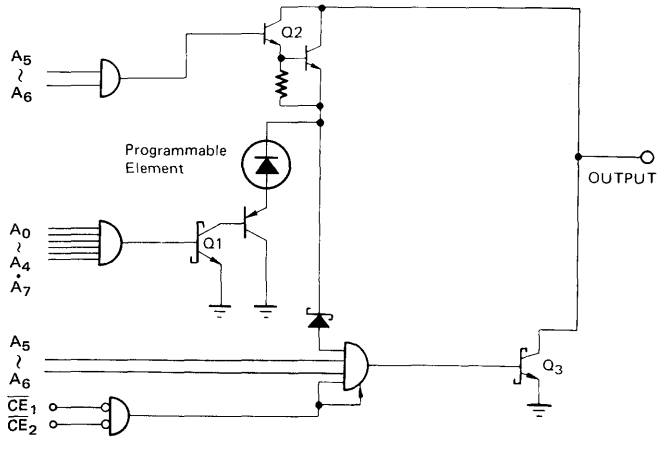
Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test

Fig. 24 – PROGRAMMED CELL (CROSS SECTION)



▨ Programmed by DEAP (Diffused Eutectic Aluminum Process)

Fig. 25 – INTERNAL PROGRAMMING CIRCUIT



4

PROGRAMMING INFORMATION (continued)

cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

"As shown in Fig. 25. transistors, Q_1 and Q_2, are turned on to select the desired bit for programming by using eight address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q_2 and memory cell into transistor Q_1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH}=2.4V and V_{CC}=7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated loactions of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	–	0.8	V
Input HIgh Voltage	V_{IH}		2.0	–	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	–	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	–	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS ($T_A = 25°C$)

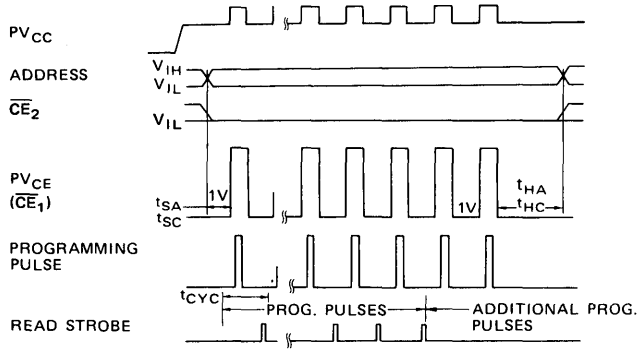
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW} (1)	10	11	12	μs
Programming Pulse Rise Time	t_r (2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r (2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r (3)	–	–	2	μs
Programming Pulse Fall Time	t_f (4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f (4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f (5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP} (6)	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
Chip Enable Input Hold Time	t_{HC}	2	–	–	μs
PV_{CE} Hold Time	t_{HP} (7)	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (8)	10	–	–	μs
Programming Pulse Number	n	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

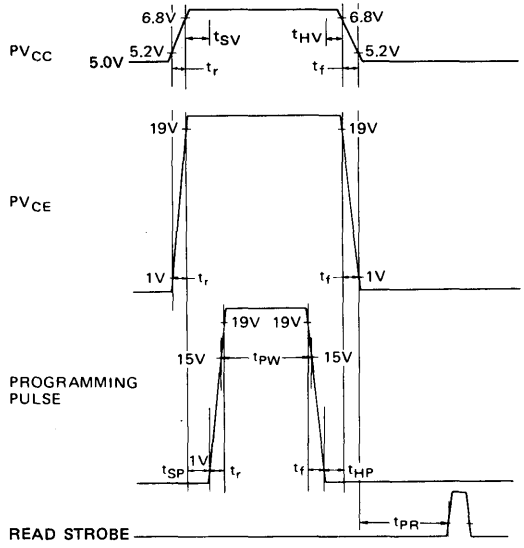
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE

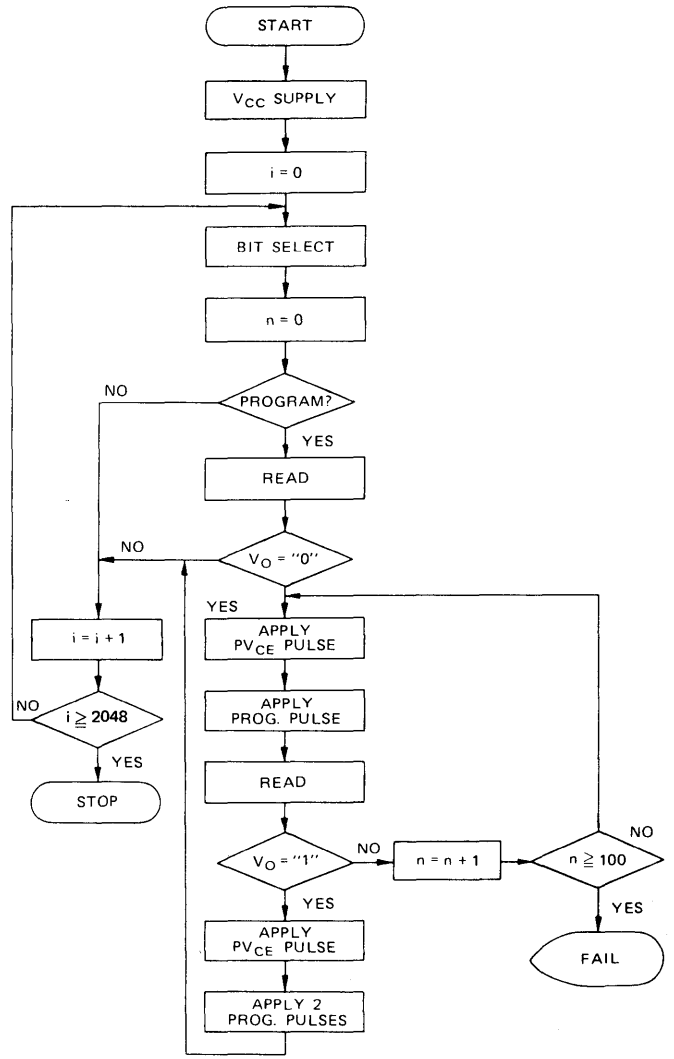


PROGRAMMING PROCEDURE

1. Apply power; V_{CC} = PV_{CC}, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125 mA and duration of t_{PW} (11 μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

Fig. 26 – PROGRAMMING FLOW CHART

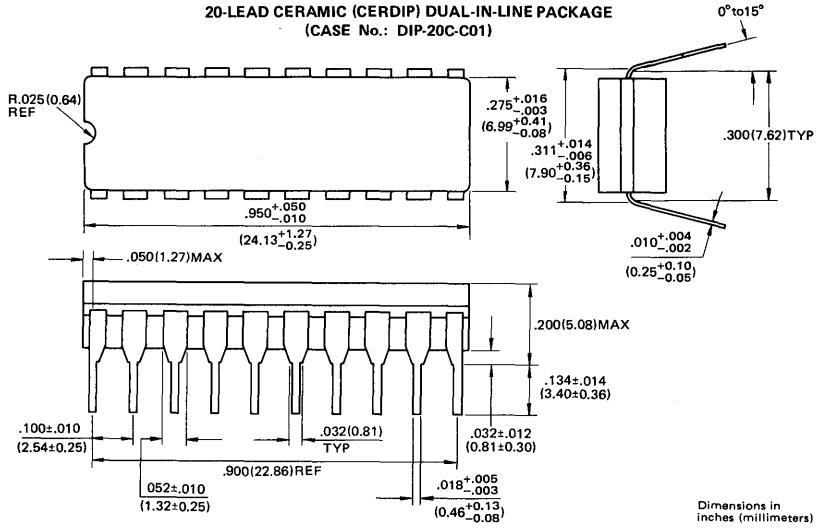


4

PACKAGE DIMENSIONS

CERAMIC DIP (: -Z)

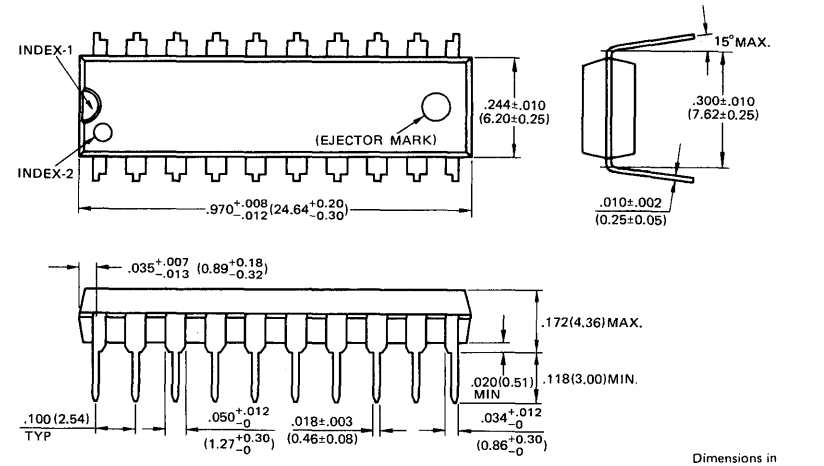
20-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20C-C01)



Dimensions in inches (millimeters)

PLASTIC DIP (: -P)

20-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)

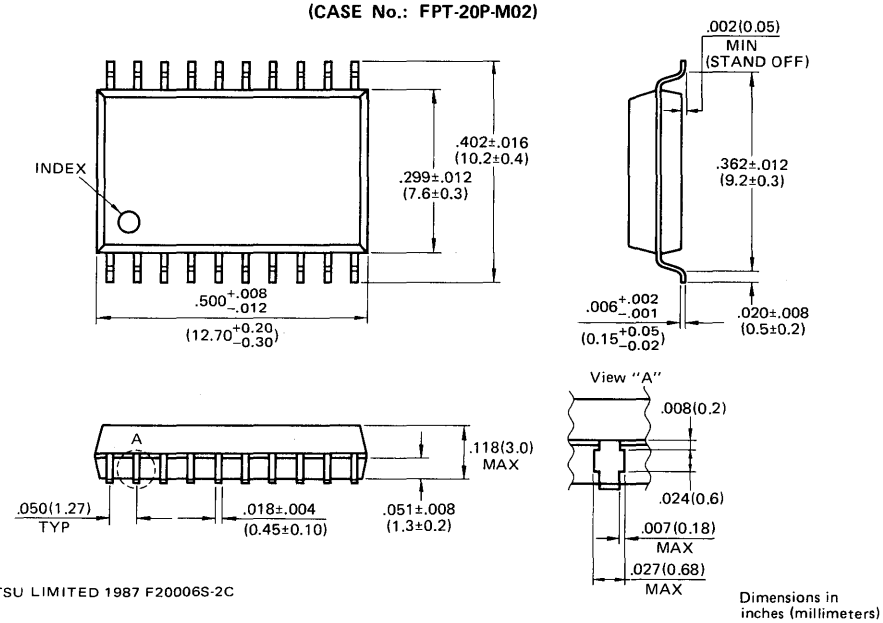


Dimensions in inches (millimeters).

PACKAGE DIMENSIONS

PLASTIC FPT (: -PF)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M02)

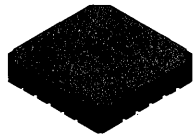


Dimensions in
inches (millimeters)

4

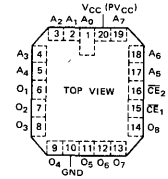
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

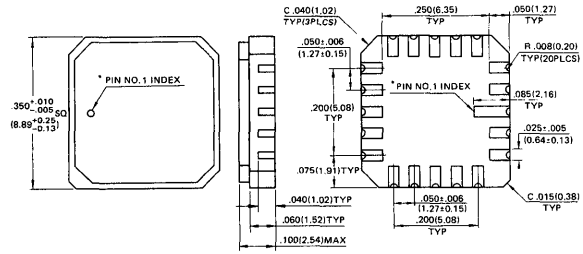


LCC-20C-F02

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE NO.: LCC-20C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

4

FUJITSU

PROGRAMMABLE SCHOTTKY 4096-BIT READ ONLY MEMORY

MB7121E/H
MB7122E/H/Y
MB7121L
MB7122L

December 1987
Edition 3.0

SCHOTTKEY 4096-RT DEAP PROM (1024 WORDS X 4 BITS)

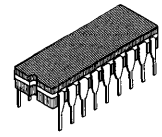
The Fujitsu MB7121 and MB7122 are high speed Schottky TTL electrically field programmable read only memories organized as 1024 words by 4 bits. With uncommitted collector outputs provided on the MB7121 and three-state outputs on the MB7122, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

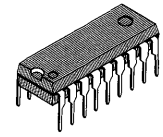
The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extemely high programmability.

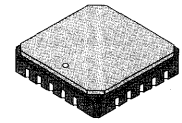
- Single +5V supply voltage.
- 1024 words x 4 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time
  Y : 25ns typ, 30ns max.
  H : 25ns typ, 35ns max.
  E : 25ns typ, 45ns max.
  L : 40ns typ, 60ns max.
- TTL compatible inputs and outputs.
- Open collector outputs (MB7121)
- 3 state outputs (MB7122)
- Two chip enable leads for simplified memory expansion.
- Standard 18 - pin Ceramic (Cerdip) DIP
  (Suffix: -Z)
- Standard 18 - pin Plastic DIP
  (Suffix: -M)
- Standard 20 - pad Ceramic (Frit Seal) LCC
  (Suffix: -TV)
- JEDEC approved pin output.



CERAMIC PACKAGE
DIP-18C-C01

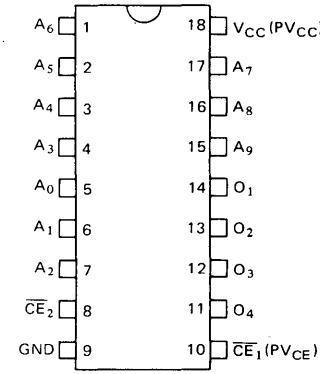


PLASTIC PACKAGE
DIP-18P-M02



CERAMIC PACKAGE
LCC-20C-F02

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See page 16

ABSOLUTE MAXIMUM RATINGS (See NOTE)

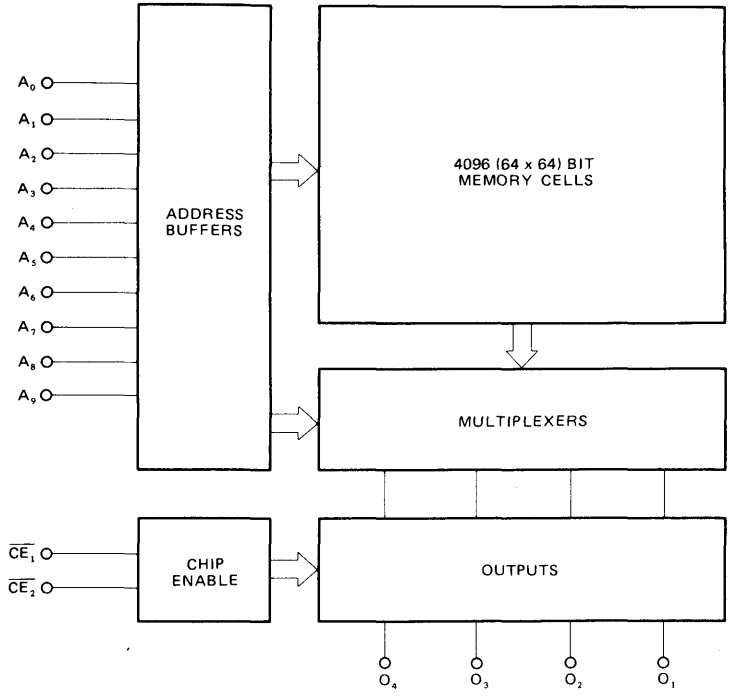
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CCP}	−0.5 to +7.5	V
Input Voltage		V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)		V_{IPRG}	22.5	V
Output Voltage (during programming)		V_{OPRG}	−0.5 to +22.5	V
Input Current		I_{IN}	−20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+150	mA
Storage Temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to + 125	
Output Voltage		V_{OUT}	−0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – MB 7122 BLOCK DIAGRAM



CAPACITANCE (f=1MHz, V_{CC}=+5V, V_{IN}=+2V, T_A=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	12	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	5.5	V
Ambient Temperature	T_A	0	–	75	°C

DC CHARACTERISTICS

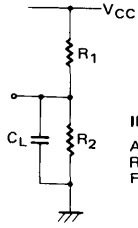
(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	μA
Output Low Voltage (I_{OL} = 10mA)		V_{OL}			0.45	V
Output Low Voltage (I_{OL} = 16mA)		V_{OL}			0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)	MB7121	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4V, chip disabled)	MB7122	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.5V, chip disabled)	MB7122	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	E/H/Y	I_{CC}		105**	150	mA
	L			40**	50	
Output High Voltage (I_O = -2.4mA)	MB7122	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB7122	I_{OS}*	-15		-60	mA

Note: *Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

**This value denotes conditions at T_A = 25°C and V_{CC} = +5.0V.

Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

	MB 7121/MB 7122		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

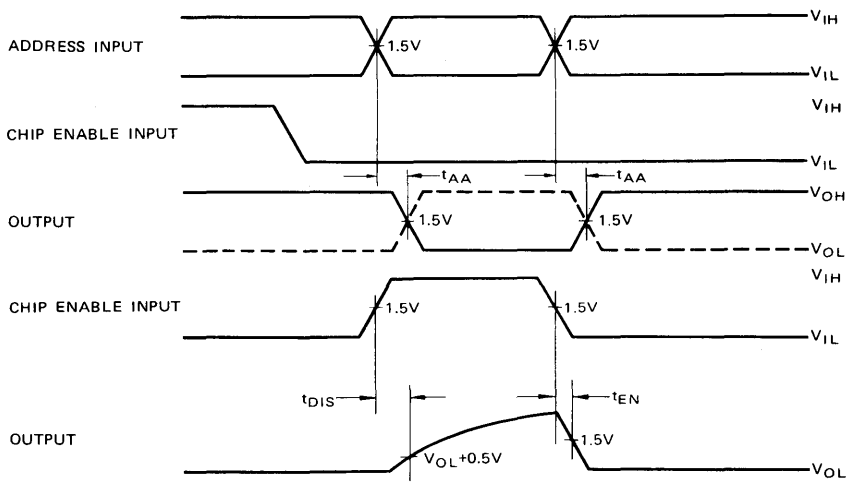
AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	L		E		H		MB7122Y		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	40*	60**	25	45	25	35	25	30	ns
Output Disable Time	t_{DIS}	20	50	15	30	15	30	15	25	ns
Output Enable Time	t_{EN}	30	50	15	30	15	30	15	25	ns

(* 7121L: 45ns **7121L: 70ns)

OPERATION TIMING DIAGRAM



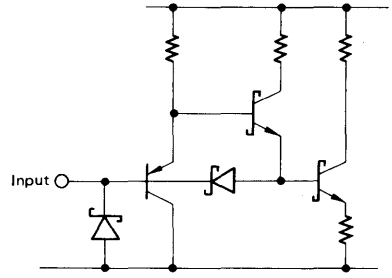
Note: Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

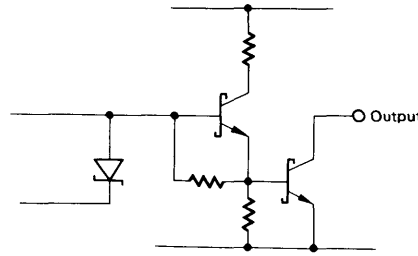
Fig. 3 – MB 7121/7122 INPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7122 (3-state) compared to 0mA for the MB 7121 (open-collector).

Fig. 4 – MB 7121 OUTPUT



THREE-STATE OUTPUT

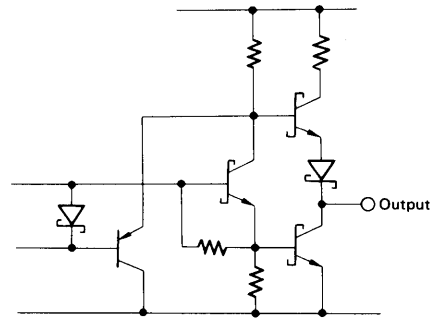
A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists

that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB 7122 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{INA} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

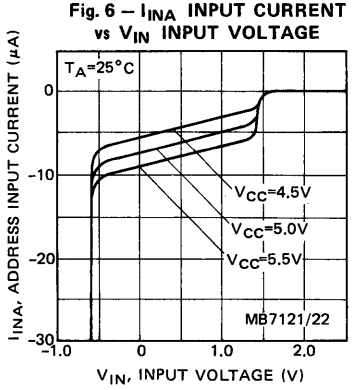

Fig. 7 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

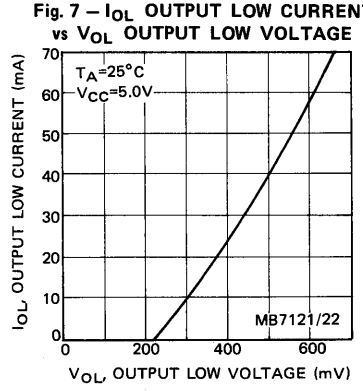

Fig. 8 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

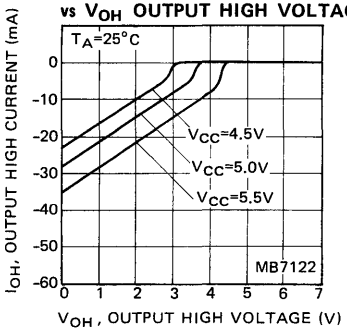

Fig. 9 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

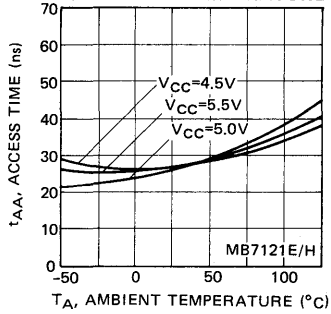

Fig. 10 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

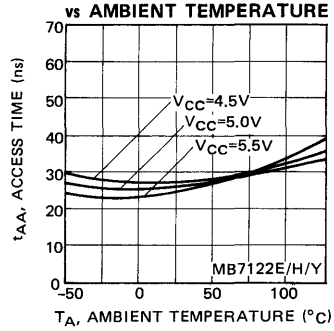

Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

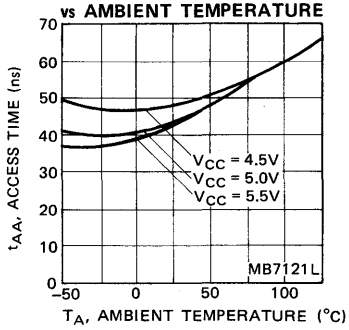

Fig. 12 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

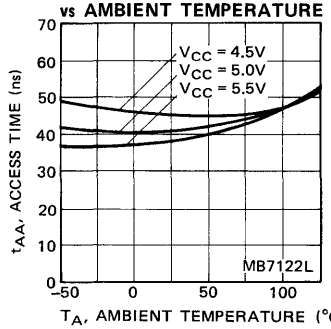

Fig. 13 – t_{DS} DISABLE TIME vs AMBIENT TEMPERATURE

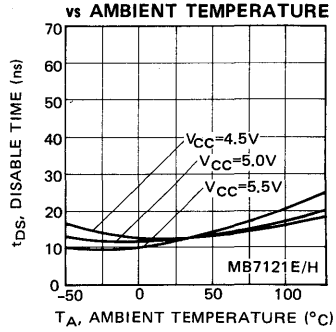

Fig. 14 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

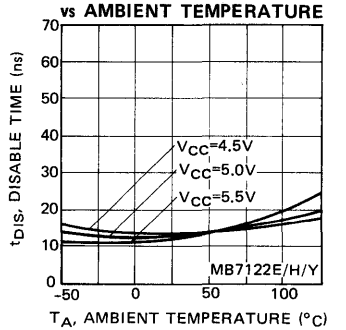

Fig. 15 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

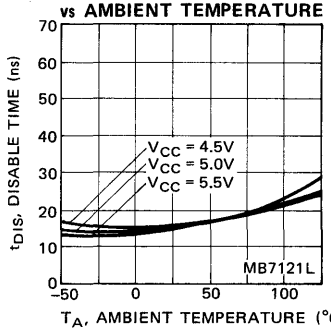

Fig. 16 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

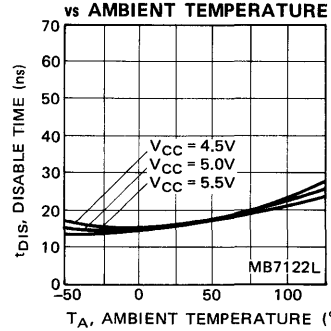

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Fig. 17 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

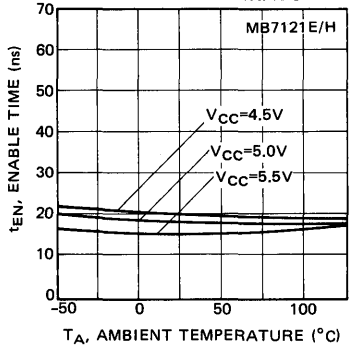


Fig. 18 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

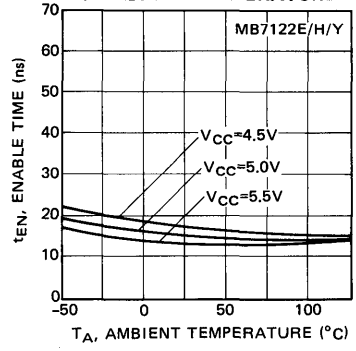


Fig. 19 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

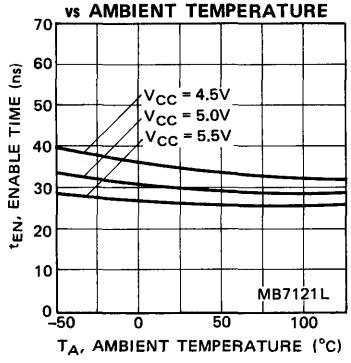


Fig. 20 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

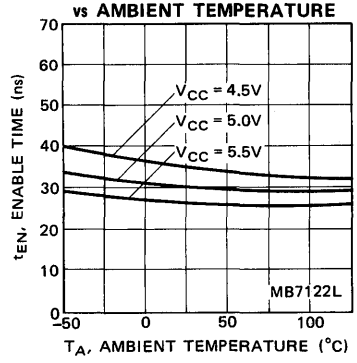


Fig. 21 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

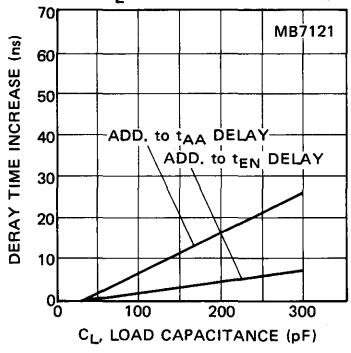
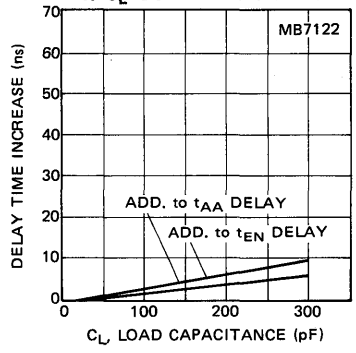


Fig. 22 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



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PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB 7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate (Fig. 23).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Groove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the function decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test

Fig. 23 – PROGRAMMED CELL (CROSS SECTION)

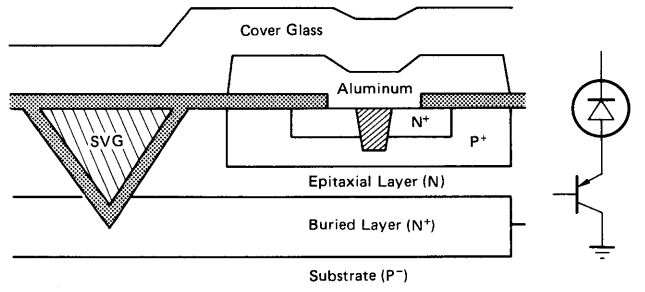
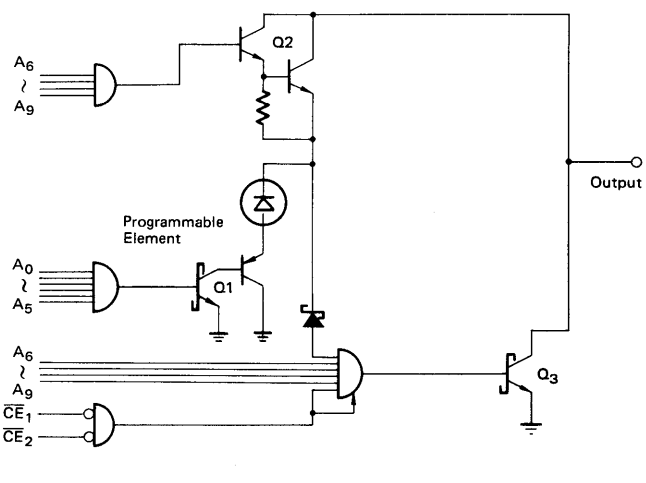


Fig. 24 – INTERNAL PROGRAMMING CIRCUIT



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PROGRAMMING INFORMATION (continued)

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

"As shown in Fig. 24, transistors, Q_1 and Q_2, are turned on to select the desired bit for programming by using eight address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q_2 and memory cell into transistor Q_1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH} = 2.4V and V_{CC} = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	–	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	–	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS ($T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW} (1)	10	11	12	μs
Programming Pulse Rise Time	t_r (2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r (2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r (3)	–	–	2	μs
Programming Pulse Fall Time	t_f (4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f (4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f (5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP} (6)	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
Chip Enable Input Hold Time	t_{HC}	2	–	–	μs
PV_{CE} Hold Time	t_{HP} (7)	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (8)	10	–	–	μs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

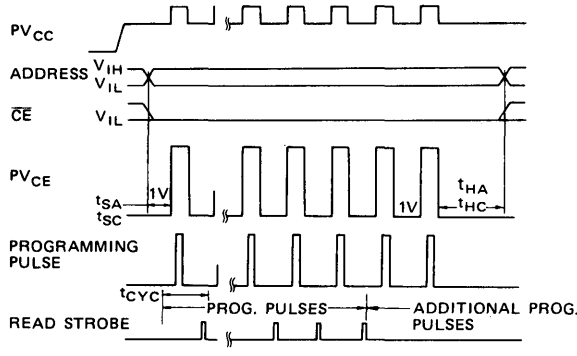
Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

4

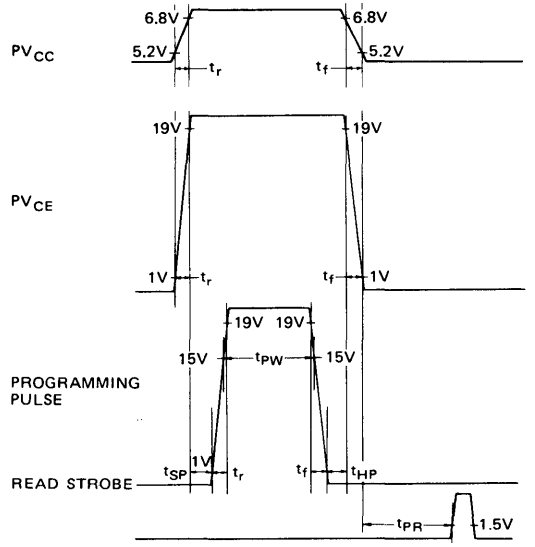
PROGRAMMING INFORMATION (continued)

4

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE

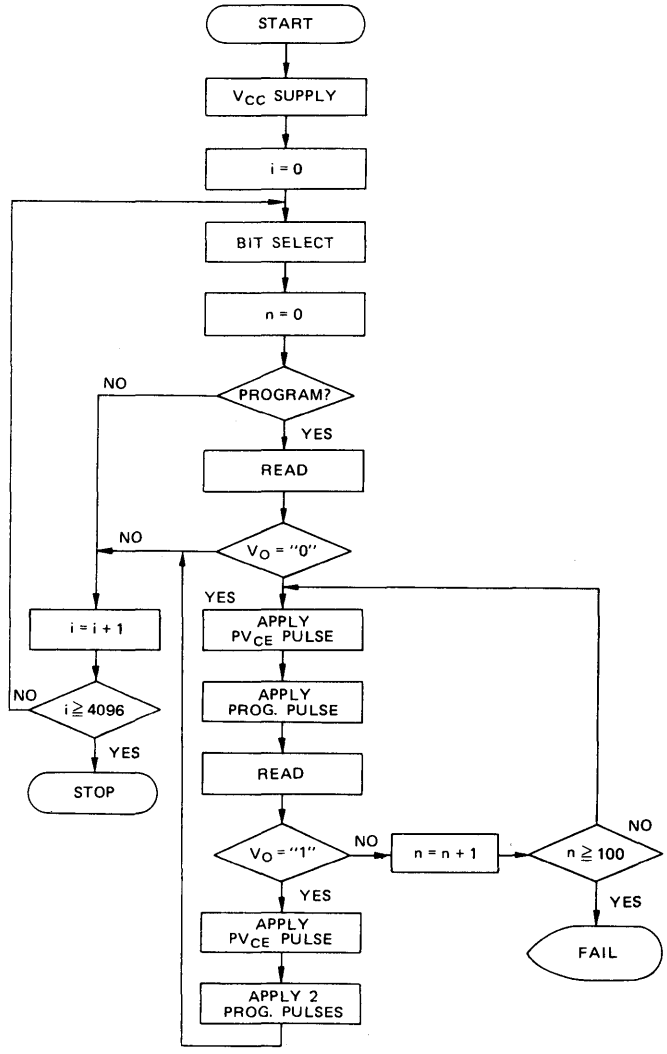


PROGRAMMING PROCEDURE

1. Apply power; V_{CC}=PV_{CC}, GND= 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O=low. (In the case of V_O=high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 120 mA and duration of t_{PW} (10μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O=low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O=high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

Fig. 25 – PROGRAMMING FLOW CHART

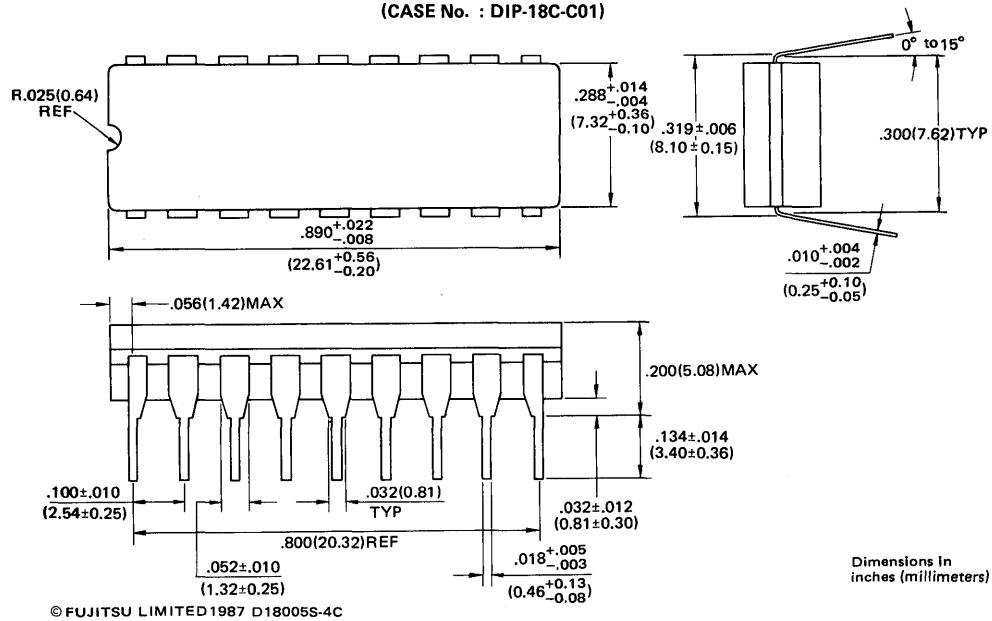


4

PACKAGE DIMENSIONS

(Suffix: -Z)

18-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-18C-C01)



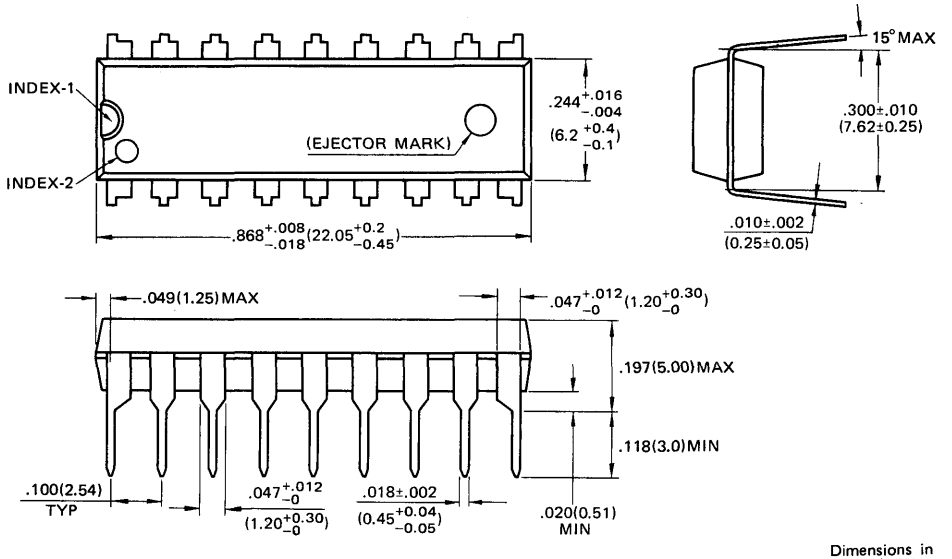
Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS

(Suffix: -M)

18-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M02)



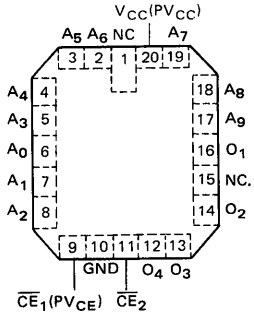
Dimensions in inches (millimeters)

4

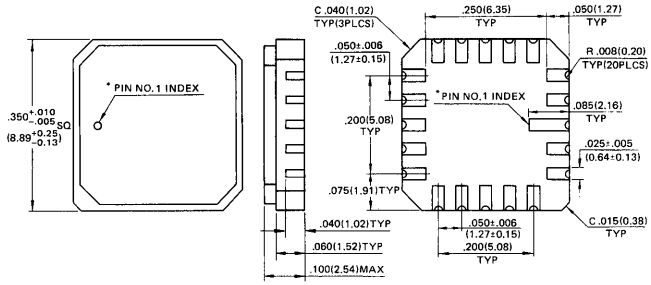
PACKAGE DIMENSIONS

(Suffix: -TV)

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE NO.: LCC-20C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

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FUJITSU

PROGRAMMABLE SCHOTTKY 4096-BIT READ ONLY MEMORY

MB 7123E/H
MB 7124E/H/Y
MB 7123L
MB 7124L

June 1987
Edition 3.0

SCHOTTKY 4096-BIT DEAP PROM (512 WORDS X 8 BITS)

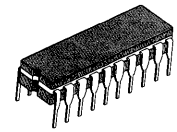
The Fujitsu MB 7123 and MB 7124 are high speed Schottky TTL electrically field programmable read only memories organized as 512 words by 8 bits. With uncommitted collector outputs provided on the MB 7123 and three-state outputs on the MB 7124, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

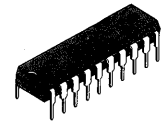
The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

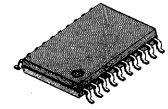
- Single +5V supply voltage.
- 512 words x 8 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (diffused Eutectic Aluminum process).
- Simplified and lower power programming.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time, 25ns typ
  Y: 30ns max. H: 35ns max.
  E: 45ns max.
- Fast access time, 35 ns typ.
  L: 60 ns max.
- TTL compatible inputs and outputs.
- Open collector outputs (MB 7123)
- 3-state outputs (MB 7124)
- One chip enable leads for simplified memory expansion.
- Standard 20 pin Ceramic (Cerdip) DIP (Suffix: -Z)
  Standard 20 pin Plastic DIP (Suffix: -P)
  Standard 20 pin Plastic FPT (Suffix: -PF)
  Standard 20 pad Ceramic LCC (Suffix: -TV)
- JEDEC approved pin out.



CERAMIC PACKAGE
DIP-20C-C01



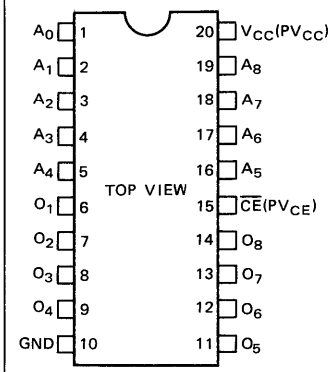
PLASTIC PACKAGE
DIP-20P-M02



PLASTIC PACKAGE
FPT-20P-M02

LCC-20C-F02: See page 16

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 16

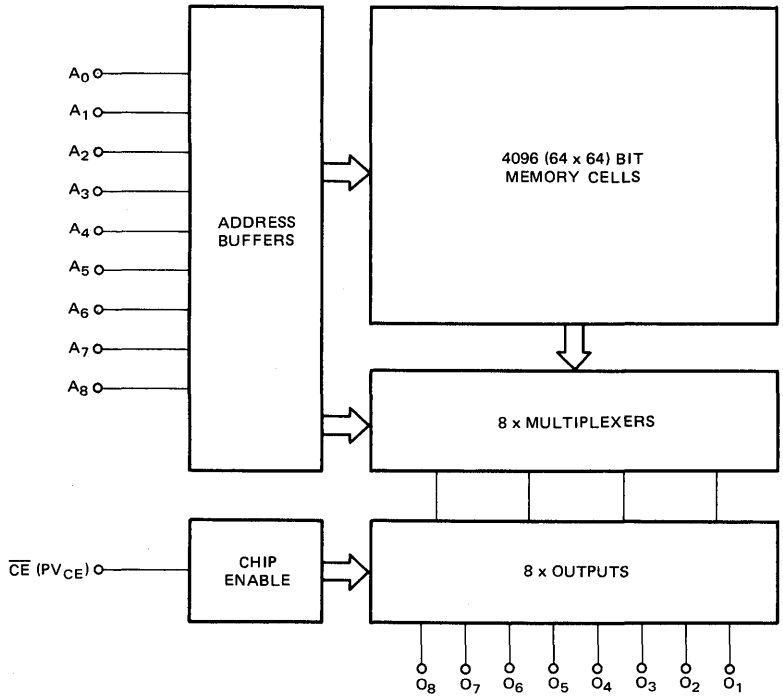
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CCP}	-0.5 to +7.5	V
Input Voltage		V_{IN}	-1.5 to +5.5	V
Input Voltage (during programming)		V_{PRG}	22.5	V
Output Voltage (during programming)		V_{PRG}	-0.5 to +22.5	V
Input Current		I_{IN}	-20	mA
Input Current (during programming)		I_{PRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{PRG}	+150	mA
Storage Temperature	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-40 to +125	
Output Voltage		V_{OUT}	-0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 7123/7124 BLOCK DIAGRAM



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CAPACITANCE (f=1MHz, V_{CC}=+5V, V_{IN}=+2V, T_A=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			12	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}			0.8	V
Input High Voltage	V_{IH}	2.0			V
Ambient Temperature	T_A	0		75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45 V)		I_F			-250	μA
Output Low Voltage (I_{OL} = 10mA)		V_{OL}			0.45	V
Output Low Voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output Leakage Current (V_O = 2.4 V, chip disabled)	MB 7123	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4 V, chip disabled)	MB 7124	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.45 V, chip disabled)	MB 7124	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18 mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	E/H/Y	I_{CC}		120	170	mA
	L			60	75	
Output High Voltage (I_O = -2.4 mA)	MB 7124	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB 7124	I_{OS}*	-15		-60	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{ICE}=0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

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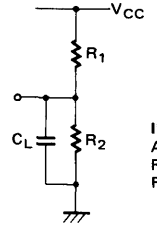
Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS
Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

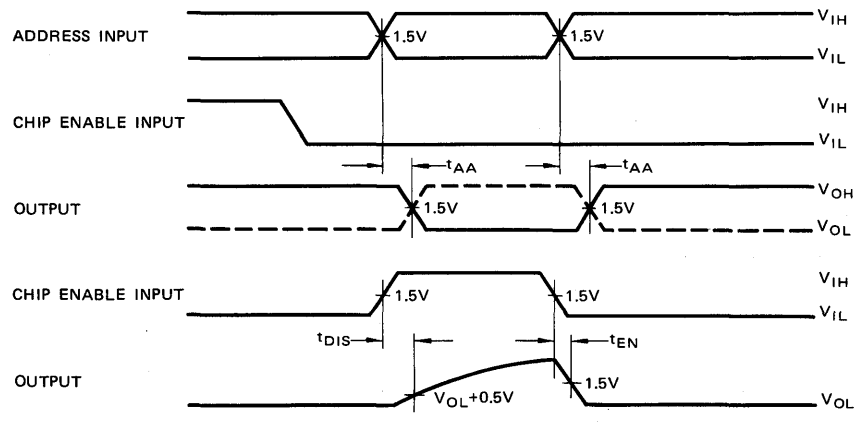
	MB 7123/7124		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless othersise noted.)

Parameter	Symbol	L		E		H		MB 7124Y		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	35	60	25	45	25	35	25	30	ns
Output Disable Time	t_{DIS}	20	40	15	30	15	30	15	25	ns
Output Enable Time	t_{EN}	20	40	15	30	15	30	15	25	ns

OPERATION TIMING DIAGRAM



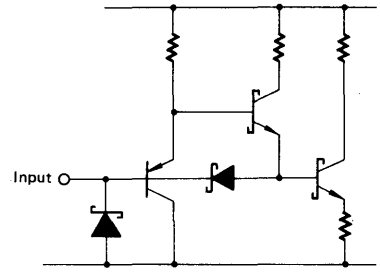
Note: Output disable time is the time taken for the output to reach a high resistance state when chip enable is taken high. Output enable time is the time taken for the output to become active when chip enable is taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

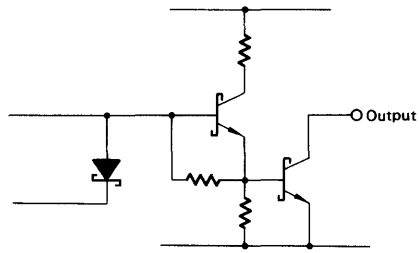
Fig. 3 – MB 7123/7124 INPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7124 (3-state) compared to 0mA for the MB 7123 (open-collector).

Fig. 4 – MB 7123 OUTPUT



THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

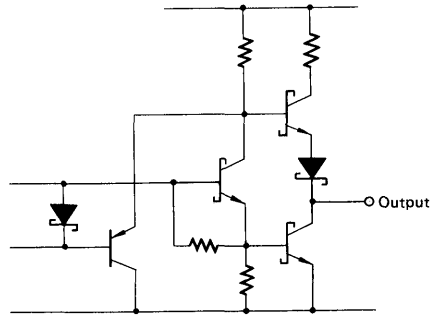
In the case where two devices are on at the same time, the possibility exists

4

that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions in unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB 7124 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{IN} INPUT CURRENT vs. V_{IN} INPUT VOLTAGE

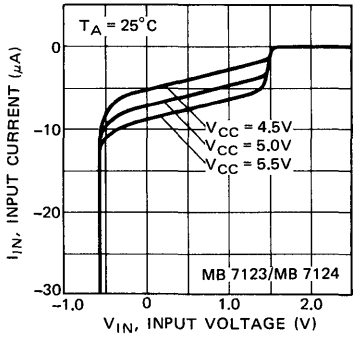

Fig. 7 – I_{OH} OUTPUT HIGH CURRENT vs. V_{OH} OUTPUT HIGH VOLTAGE

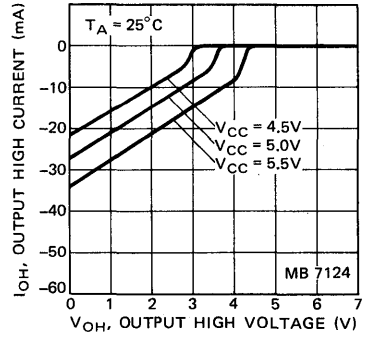

Fig. 8 – I_{IL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

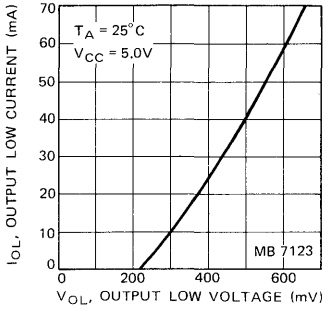

Fig. 9 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

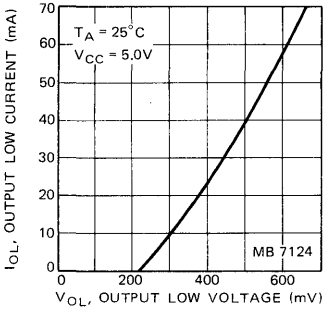

Fig. 10 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

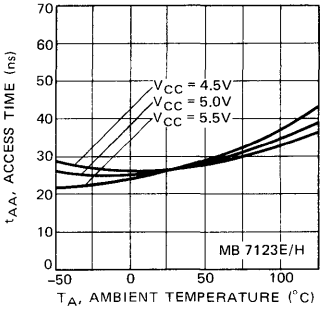

Fig. 11 – t_{AA}, ACCESS TIME vs AMBIENT TEMPERATURE

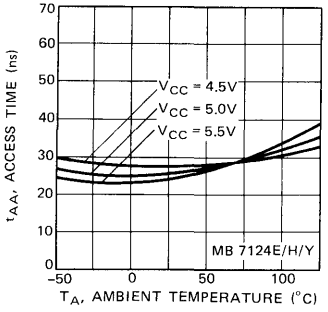

Fig. 12 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

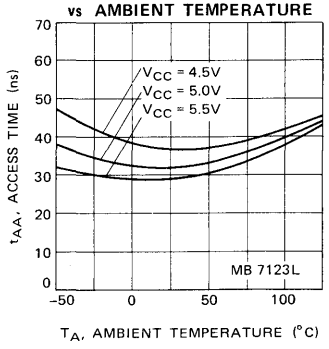

Fig. 13 - t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

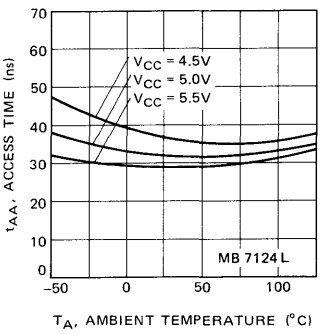

Fig. 14 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

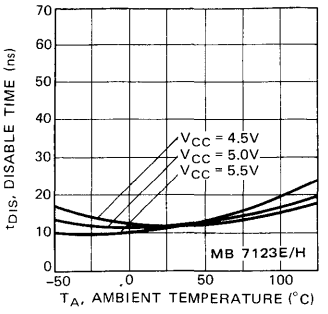

Fig. 15 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

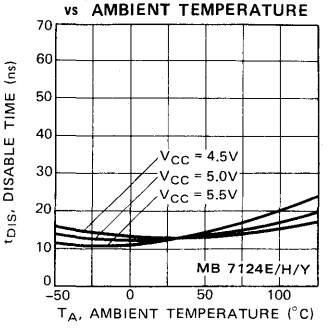

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Fig. 16 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

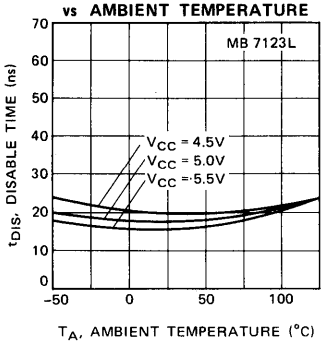


Fig. 17 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

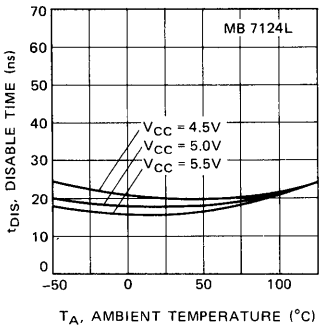


Fig. 18 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

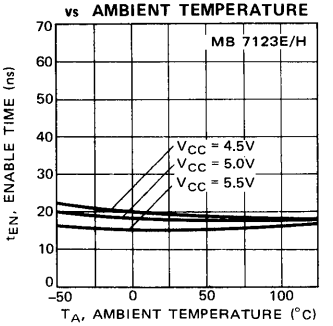


Fig. 19 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

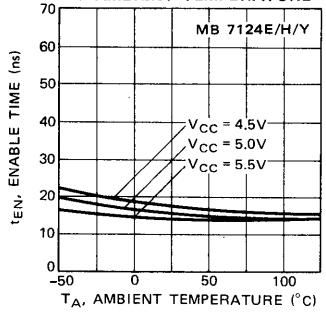


Fig. 20 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

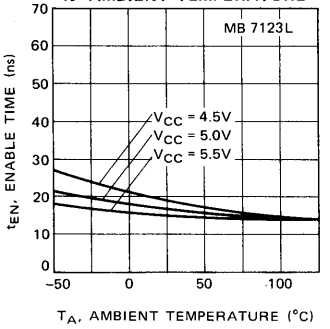


Fig. 21 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

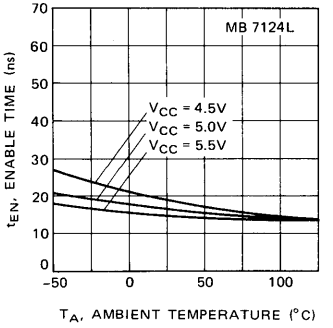


Fig. 22 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

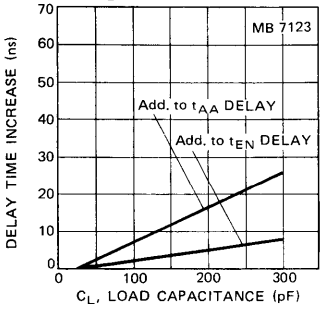
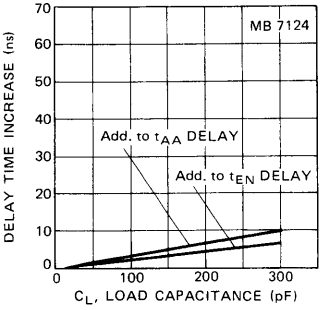


Fig. 23 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB 7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, and N^+ epitaxial layer, and a P^- substrate (Fig. 24).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Groove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

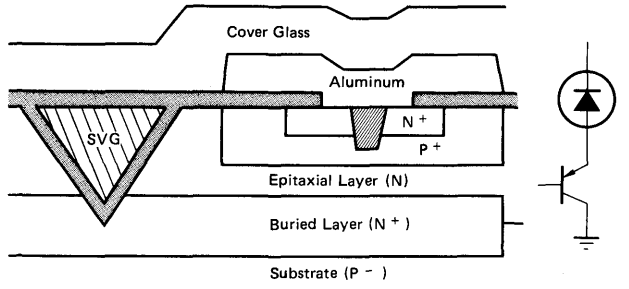
In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

SPECIAL FACTORY TESTING

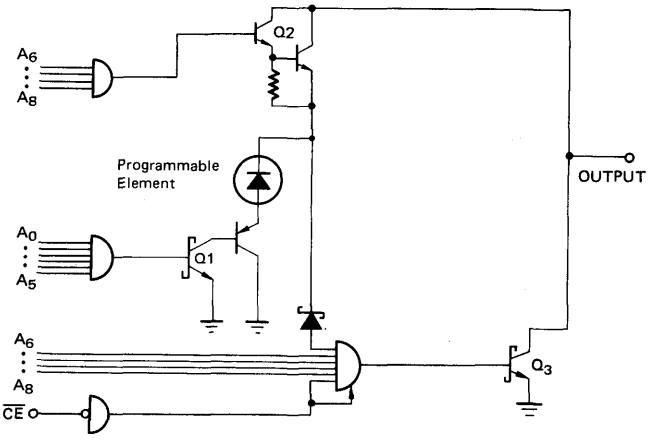
Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test

Fig. 24 – PROGRAMMED CELL (CROSS SECTION)



Programmed by DEAP (Diffused Eutectic Aluminum Process)

Fig. 25 – INTERNAL PROGRAMMING CIRCUIT



4

PROGRAMMING INFORMATION (continued)

cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

"As shown in Fig. 25, transistors, Q_1 and Q_2, are turned on to select the desired bit for programming by using nine address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q_2 and memory cell into transistor Q_1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH}=2.4V and V_{CC}=7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated loactions of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	125	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	—	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS (T_A = 25°C)

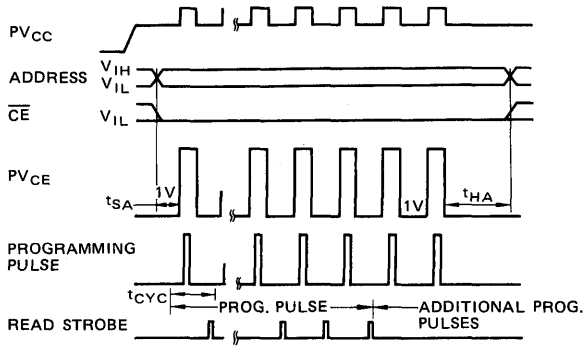
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW}(1)	10	11	12	μs
Programming Pulse Rise Time	t_r(2)			2	μs
PV_{CE} Pulse Rise Time	t_r(2)			2	μs
PV_{CC} Pulse Rise Time	t_r(3)			2	μs
Programming Pulse Fall Time	t_f(4)			2	μs
PV_{CE} Pulse Fall Time	t_f(4)			2	μs
PV_{CC} Pulse Fall Time	t_f(5)			2	μs
Address Input Set-up Time	t_{SA}	2			μs
Chip Enable Input Set-up Time	t_{SC}	2			μs
PV_{CE} Set-up Time	t_{SP}(6)	4			μs
Address Input Hold Time	t_{HA}	2			μs
Chip Enable Input Hold Time	t_{HC}	2			μs
PV_{CE} Hold Time	t_{HP}(7)	2			μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(8)	10			μs
Programming Pulse Number				100	Times
Programming Time/Bit		120	150	6120	μs/bit
Additional Programming Pulse Number		2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

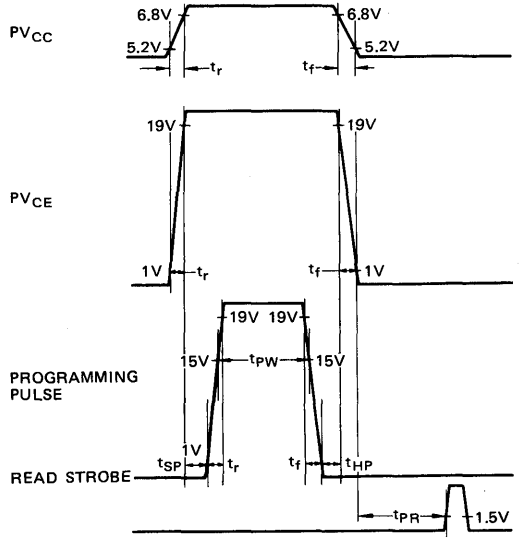
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE

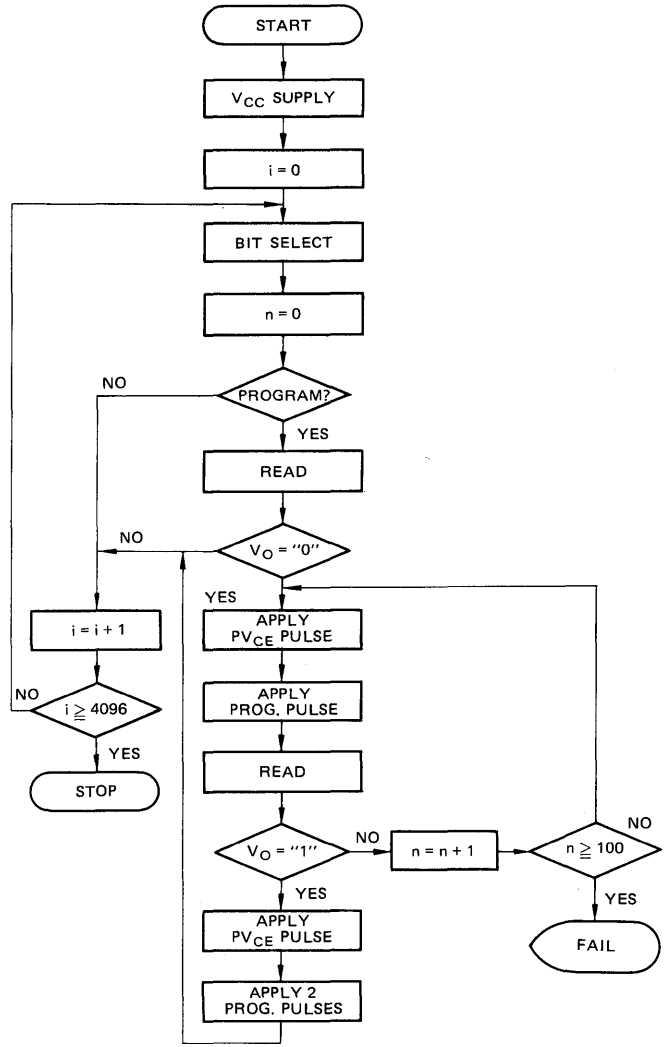


PROGRAMMING PROCEDURE

1. Apply power; $V_{CC} = PV_{CC}$, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 120 mA and duration of t_{PW} (10μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C ± 2°C)

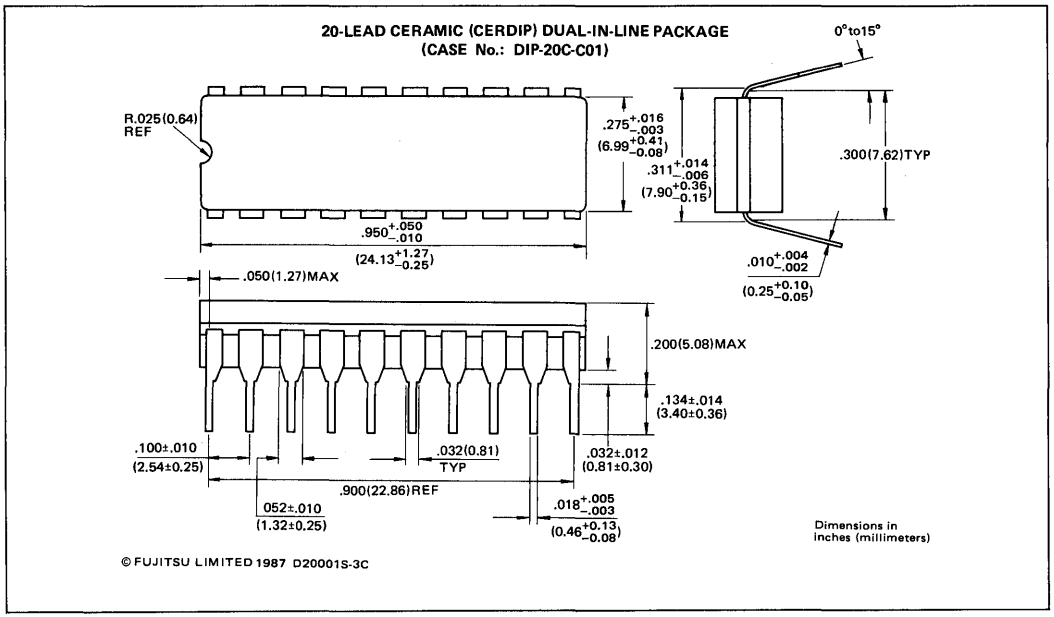
Fig. 26 – PROGRAMMING FLOW CHART



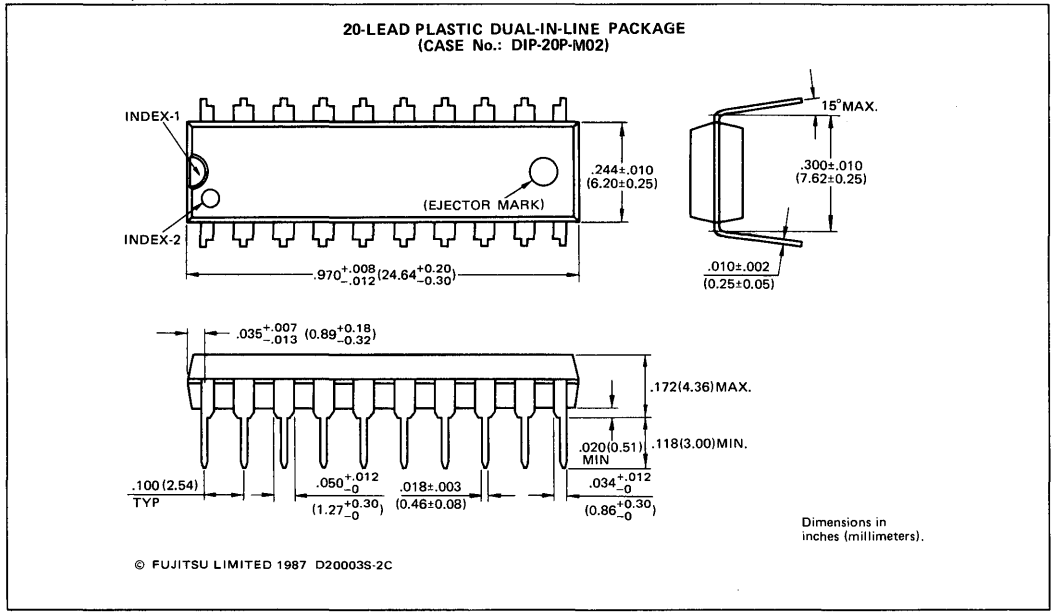
4

PACKAGE DIMENSIONS

CERAMIC DIP (: -Z)



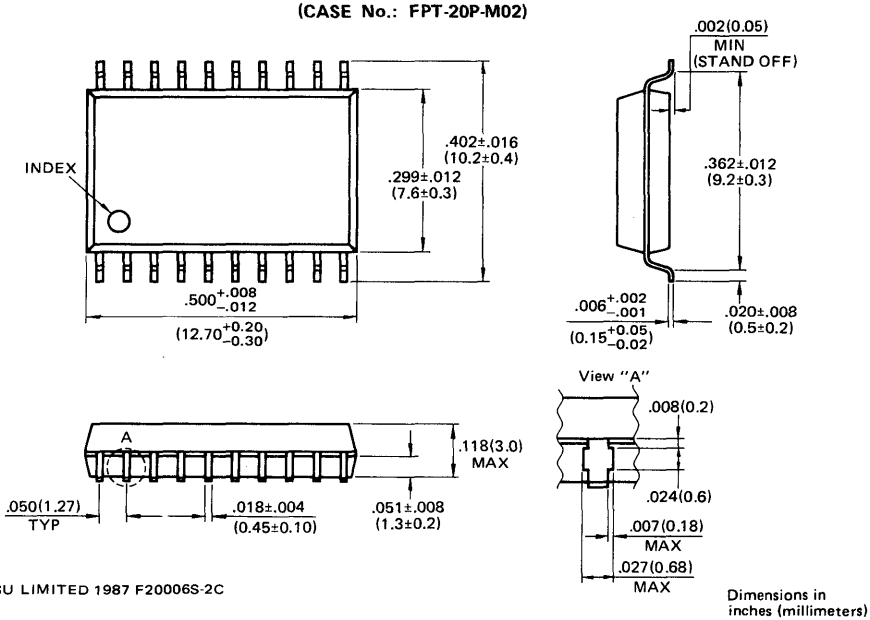
PLASTIC DIP (: -P)



PACKAGE DIMENSIONS

PLASTIC FPT (: -PF)

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M02)

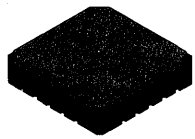


Dimensions in
inches (millimeters)

4

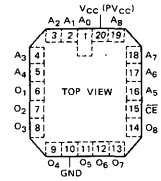
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

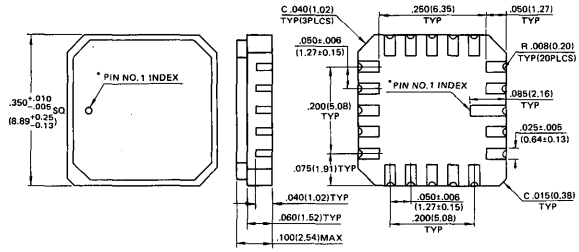


LCC-20C-F02

PAD CONFIGURATION



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE NO.: LCC-20C-F02)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in inches (millimeters)

4

FUJITSU

PROGRAMMABLE SCHOTTKY 8192-BIT READ ONLY MEMORY

MB7127E/H
MB7128E/H/Y
MB7127L
MB7128L

November 1987
Edition 2.0

SCHOTTKY 8192-BIT DEAP PROM (2048 WORDS X 4 BITS)

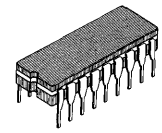
The Fujitsu MB 7127 and MB 7128 are high speed schottky TTL electrically field programmable read only memories organized as 2048 words by 4 bits. With uncommitted collector outputs provided on the MB 7127 and three-state outputs on the MB 7128, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable Deap (Diffused Eutectic Aluminum Process) according to simple programming procedures.

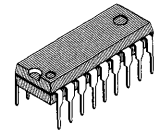
The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

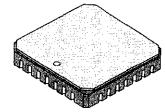
- Single +5V supply voltage.
- 2048 words x 4 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffsed Eutectic Aluminum Process).
- Simplified and lower power programing.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time
  - Y : 25ns typ, 35ns max.
  - H : 30ns typ, 45ns max.
  - E : 30ns typ, 55ns max.
  - L : 40ns typ, 70ns max.
- TTL compatible inputs and outputs.
- Open collector outputs (MB 7127)
- 3-state outputs (MB7128)
- Chip enable lead for simplified memory expansion.
- Standard 18 pin Ceramic (Cerdip) DIP (Suffix: –Z)
- Standard 18 pin Plastic DIP (Suffix: –M)
- Standard 28 pad Ceramic (Metal Seal) LCC (Suffix: –CV)
- JEDEC approved pin out.



CERAMIC PACKAGE
DIP-18C-C01

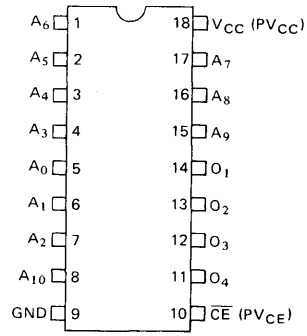


PLASTIC PACKAGE
DIP-18P-M02



CERAMIC PACKAGE
LCC-28C-A01

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 16

ABSOLUTE MAXIMUM RATINGS (See NOTE)

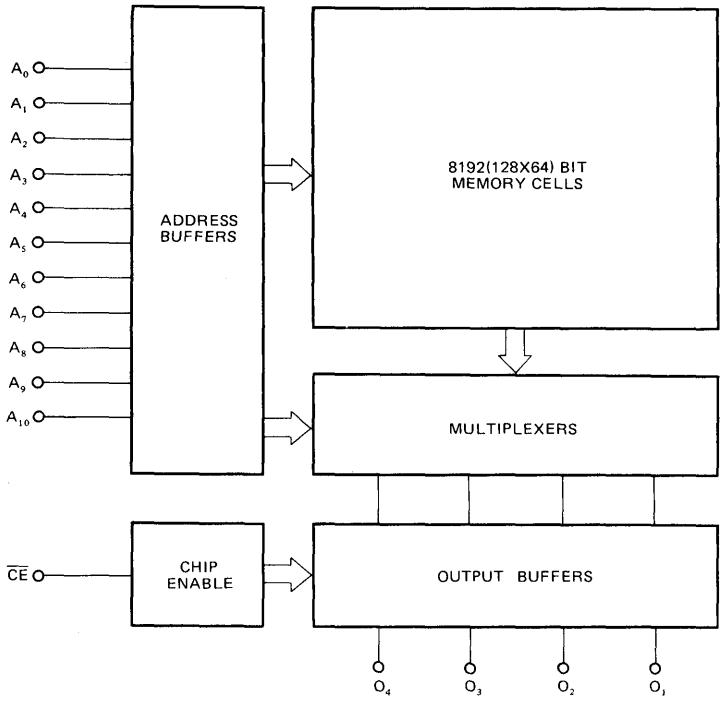
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CCP}	-0.5 to +7.5	V
Input Voltage		V_{IN}	-1.5 to 5.5	V
Input Voltage (during programming)		V_{IPRG}	22.5	V
Output Voltage (during programming)		V_{OPRG}	-0.5 to +22.5	V
Input Current		I_{IN}	-20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+150	mA
Storage Temperature	CERAMIC	T_{stg}	-65 to +150	°C
	PLASTIC		-40 to +125	
Output Voltage		V_{OUT}	-0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – MB7127/7128 BLOCK DIAGRAM



4

CAPACITANCE ($f = 1MHz$, $V_{CC} = +5V$, $V_{IN} = +2V$, $T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0		0.8	V
Input High Voltage	V_{IH}	2.0		5.5	V
Ambient Temperature	T_A	0		75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

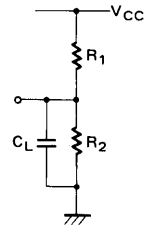
Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	μA
Output Low Voltage	I_{OL} = 10mA	V_{OL}			0.45	V
	I_{OL} = 16mA				0.50	
Output Leakage Current (V_O = 2.4V, Chip disabled)	MB7127	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4V, Chip disabled)	MB7128	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.45V, Chip disabled)	MB7128	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	E/H/Y	I_{CC}		110**	155	mA
	L			42**	60	
Output High Voltage (I_O = -2.4mA)	MB7128	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB7128	I_{OS}*	-15		-60	mA

Note: *Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{CE} = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

**This value denotes conditions at T_A = 25°C and V_{CC} = +5.0V.

4

Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS
Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

	MB7127/MB7128		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

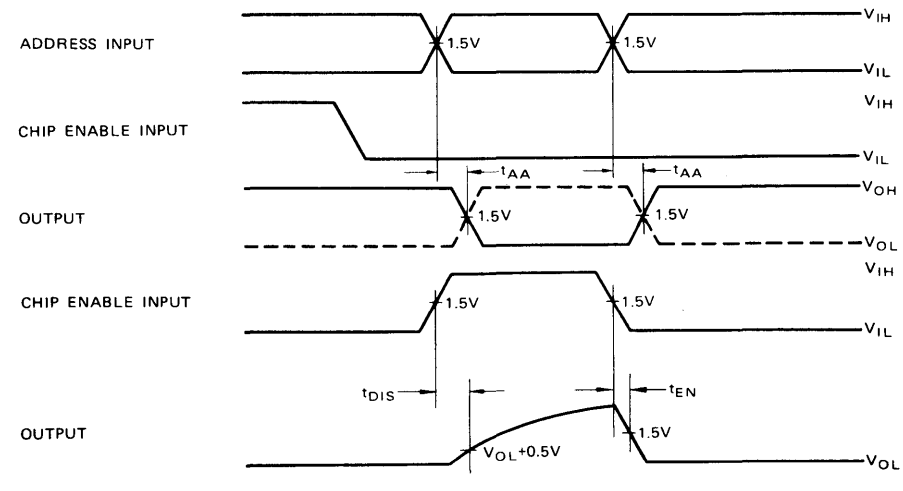
AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	L		E		H		MB 7128Y		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ.	Max.	
Access Time (via address input)	t_{AA}	40	70	30	55	30	45	25	35	ns
Output Disable Time	t_{DIS}	15	50	15	40	15	30	15	25	ns
Output Enable Time	t_{EN}	25	50	15	40	15	30	15	25	ns

4

OPERATION TIMING DIAGRAM



Note: Output disable time is the time taken for the output to reach a high resistance state when chip enable is taken high. Output enable time is the time taken for the output to become active when chip enable is taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7128 (3-state) compared to 0mA for the MB7127 (open-collector).

THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists

Fig. 3– MB7127/7128 INPUT

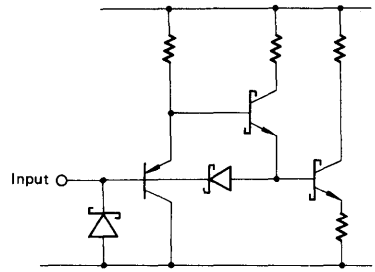
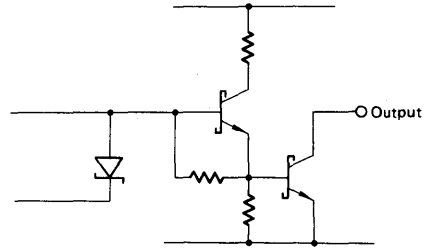


Fig. 4 – MB7127 OUTPUT

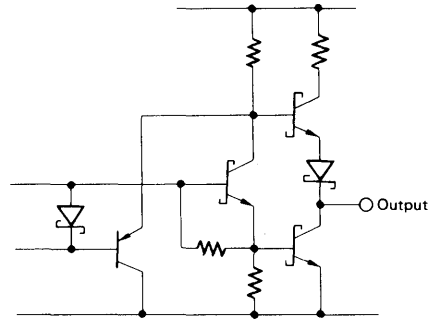


4

that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB7128 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

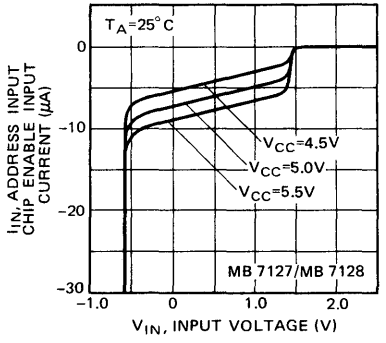

Fig. 7 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

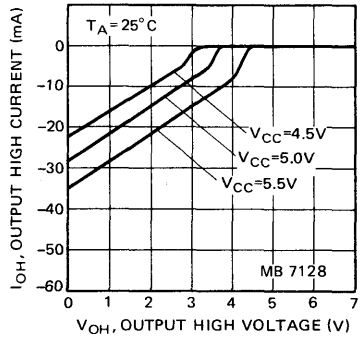

Fig. 8 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

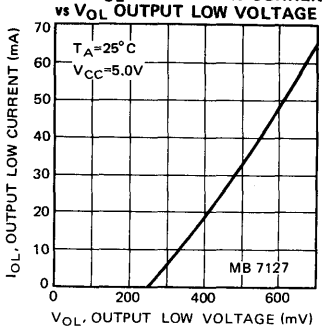

Fig. 9 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

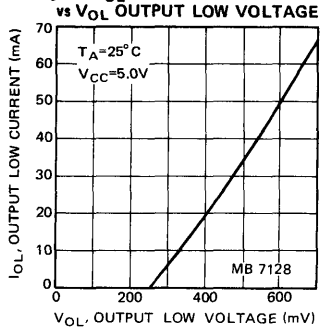

Fig. 10 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

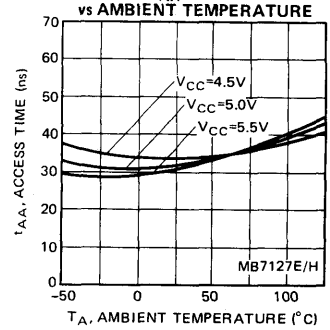

Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

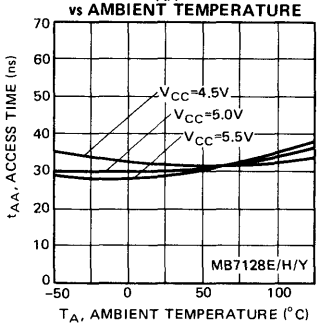

Fig. 12 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE

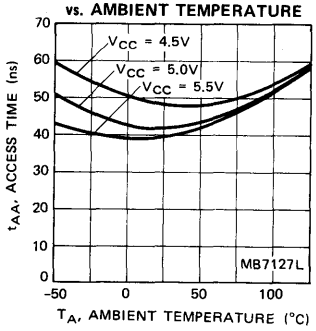

Fig. 13 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE

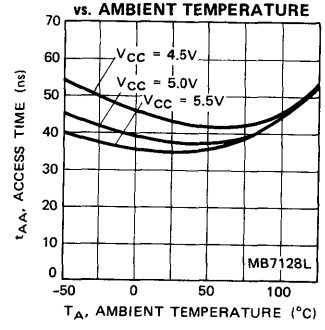

Fig. 14 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

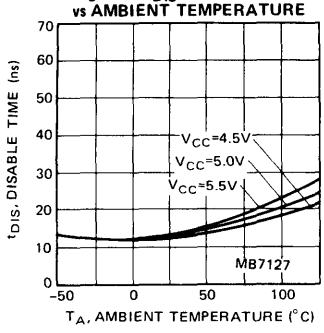

Fig.15 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

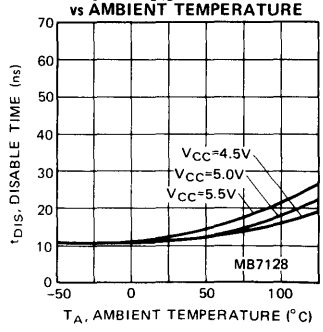

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Fig. 16 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

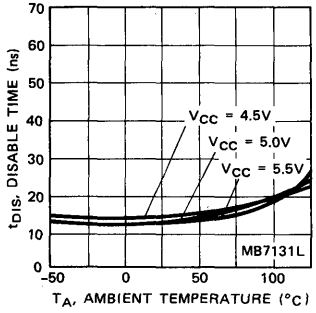


Fig. 17 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

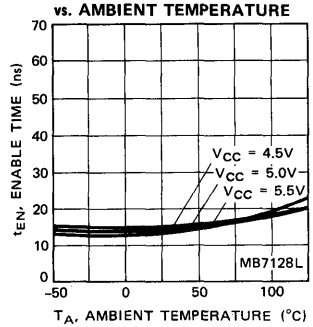


Fig. 18 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

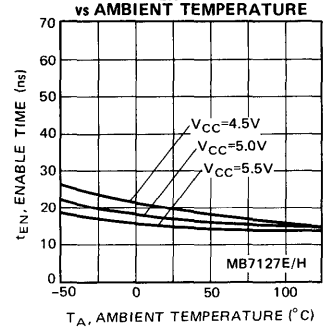


Fig. 19 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

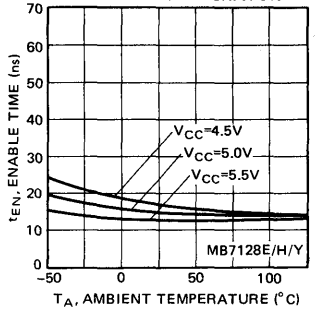


Fig. 20 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE

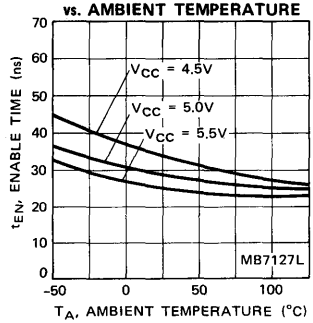


Fig. 21 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE

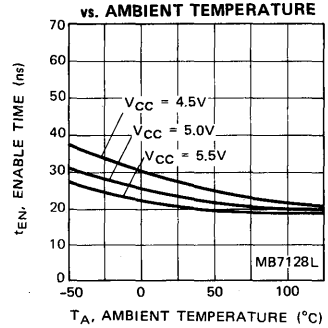


Fig. 22 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

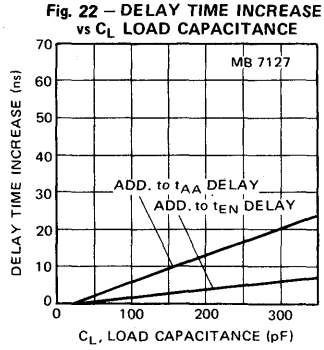
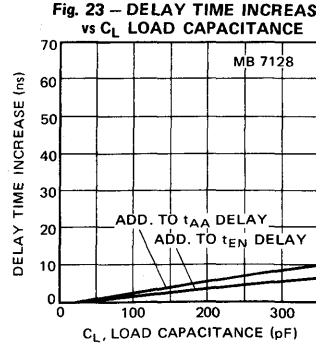


Fig. 23 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

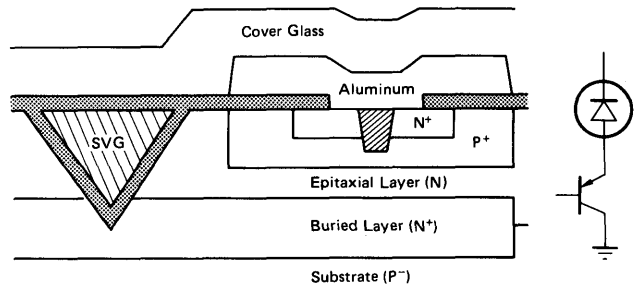
The Fujitsu MB 7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate (Fig. 24).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Groove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

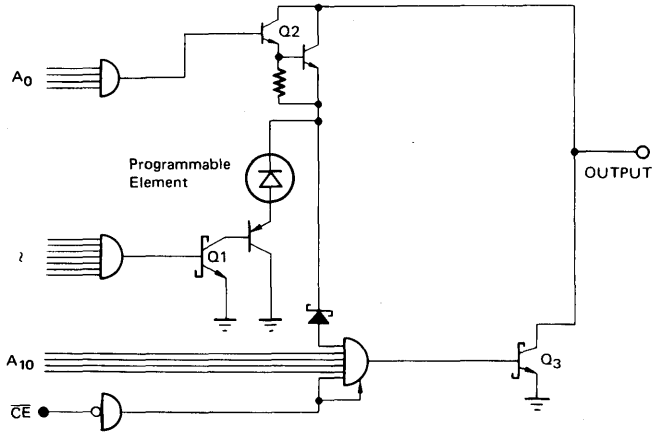
Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

Fig. 24— PROGRAMMED CELL (CROSS SELECTION)



Programmed by DEAP (Diffused Eutectic Aluminum Process)

Fig. 25 — INTERNAL PROGRAMMING CIRCUIT



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PROGRAMMING INFORMATION (continued)

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

"As shown in Fig. 25, transistors, Q_1 and Q_2, are turned on to select the desired bit for programming by using eight address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q_2 and memory cell into transistor Q_1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH} = 2.4V and V_{CC} = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH}		2.0		5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120		130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS (T_A = 25°C)

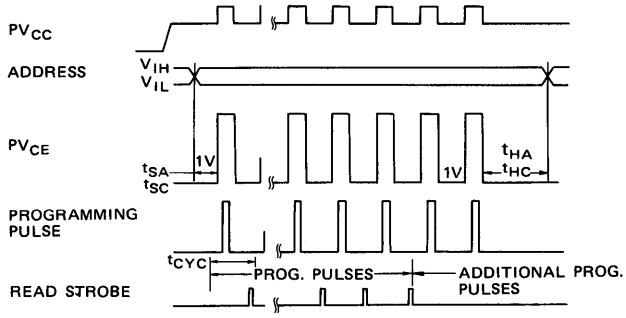
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW}(1)	10	11	12	μs
Programming Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r(3)	–	–	2	μs
Programming Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f(5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP}(6)	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
Chip Enable Input Hold Time	t_{HC}	2	–	–	μs
PV_{CE} Hold Time	t_{HP}(7)	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(8)	10	–	–	μs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



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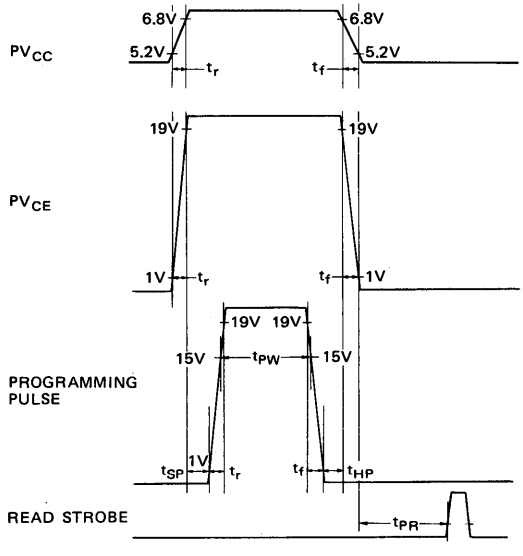
ONE DETAILED PROGRAMMING CYCLE

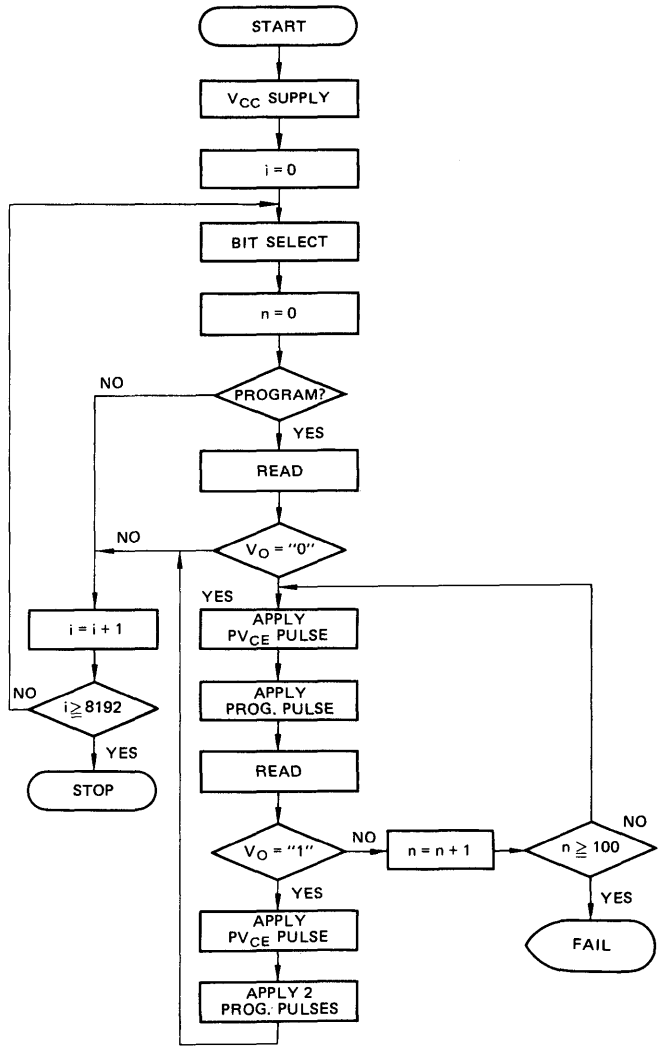


PROGRAMMING PROCEDURE

1. Apply power; $V_{CC} = PV_{CC}$, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 120mA and duration of t_{PW} (10μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

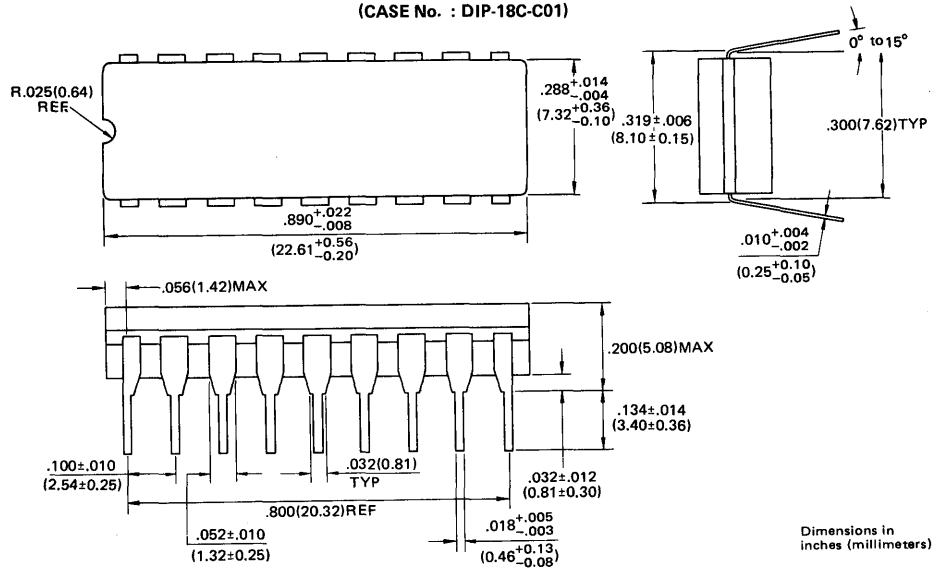
Fig. 26 – PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

(Suffix: -Z)

18-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-18C-C01)



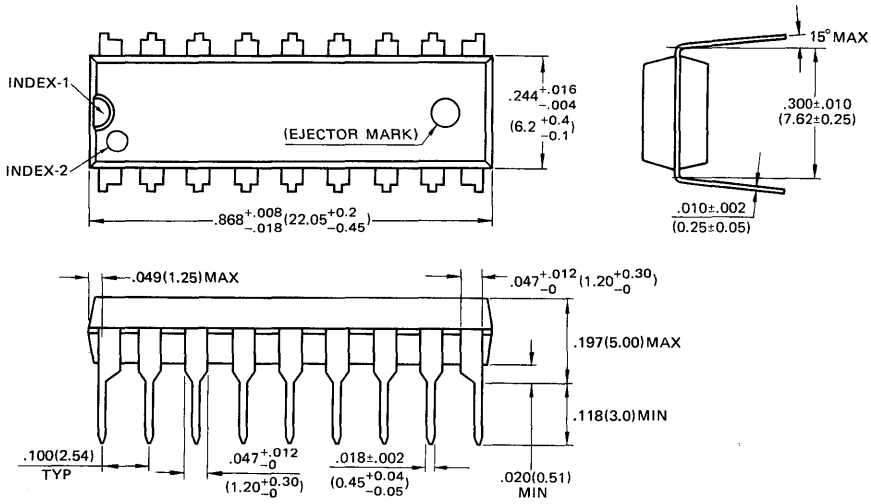
Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS

(Suffix: -M)

18-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M02)



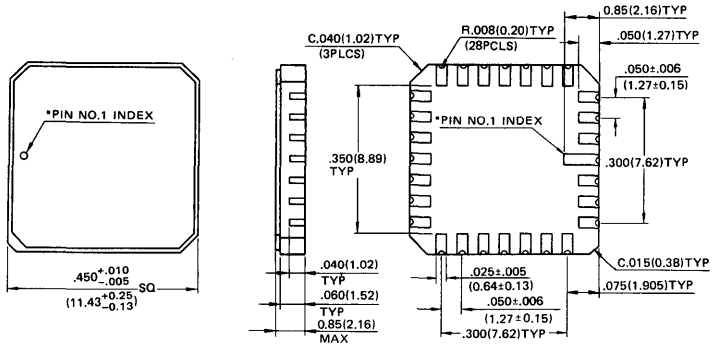
Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

(Suffix: -CV)

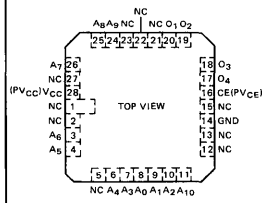
28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A01)



*Shape of Pin No.1 index: Subject to change without notice

Dimensions in inches (millimeters)

PAD CONFIGURATION



4

FUJITSU

PROGRAMMABLE SCHOTTKY 8192-BIT READ ONLY MEMORY

MB7131E/H/L
MB7132E/H/Y/L
MB7131E-SK/H-SK/L-SK
MB7132E-SK/H-SK/Y-SK/L-SK

January 1988
Edition 2.0

SCHOTTKY 8192-BIT DEAP PROM (1024 WORDS X 8 BITS)

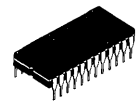
The Fujitsu MB 7131 and MB 7132 are high speed schottky TTL electrically field programmable read only memories organized as 1024 words by 8 bits. With uncommitted collector outputs provided on the MB 7131 and three-state outputs on the MB 7132, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level silicon) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

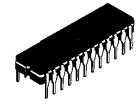
The sophisticated passive isolation termed IOP (Isolation by Oxide and Poly-silicon) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

- Single +5V supply voltage.
- 1024 words x 8 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffsed Eutectic Aluminum Process).
- Simplified and lower power programing.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time
  - Y : 25ns typ, 35ns max.
  - H : 30ns typ, 45ns max.
  - E : 30ns typ, 55ns max.
  - L : 40ns typ, 70ns max.
- TTL compatible inputs and outputs.
- Open collector outputs (MB 7131)
- 3-state outputs (MB7132)
- Chip enable lead for simplified memory expansion.
- Standard 24 pin Ceramic (Cerdip) DIP (Suffix: –Z)
- Standard 24 pin Plastic DIP (Suffix: –M)
- Standard 24 pin Ceramic (Metal Seal) FPT (Sufficx: –CF)
- Standard 38 pad Ceramic (Metal Seal) LCC (Suffix: –CV)
- JEDEC approved pin out.



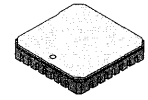
CERAMIC PACKAGE
DIP-24C-C01



CERAMIC PACKAGE
DIP-24C-C04(-SK)

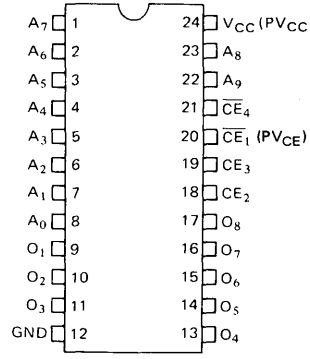
PLASTIC PACKAGE
DIP-24P-M02

CERAMIC PACKAGE
FPT-24C-A01



CERAMIC PACKAGE
LCC-28C-A01

PIN ASSIGNMENT



ICC PAD CONFIGURATION : See page 16

ABSOLUTE MAXIMUM RATINGS (See NOTE)

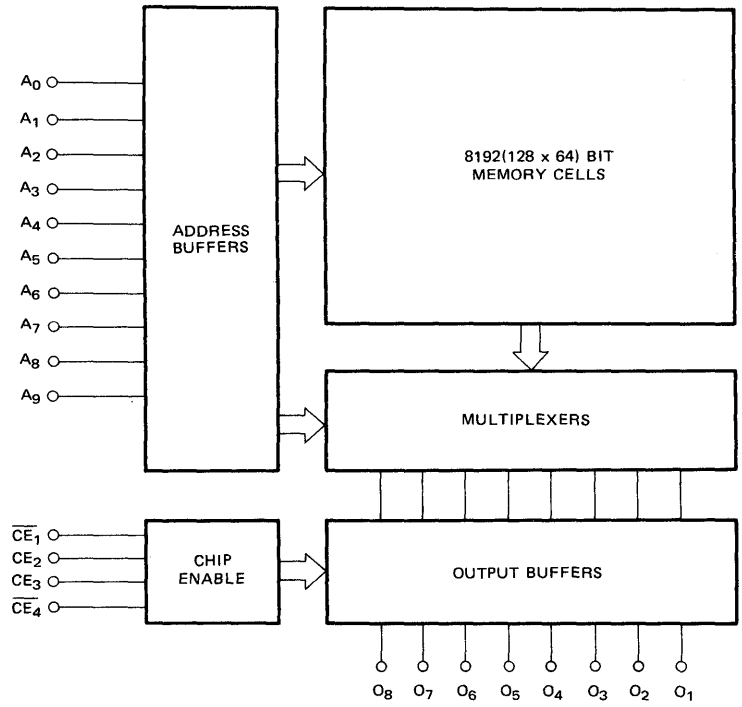
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	–0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CCP}	–0.5 to +7.5	V
Input Voltage		V_{IN}	–1.5 to 5.5	V
Input Voltage (during programming)		V_{IPRG}	22.5	V
Output Voltage (during programming)		V_{OPRG}	–0.5 to +22.5	V
Input Current		I_{IN}	–20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+150	mA
Storage Temperature	CERAMIC	T_{stg}	–65 to +150	V
	PLASTIC		–40 to +125	
Output Voltage		VOUT	–0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – MB7131/7132 BLOCK DIAGRAM



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CAPACITANCE ($f = 1MHz$, $V_{CC} = +5V$, $V_{IN} = +2V$, $T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	5.5	V
Ambient Temperature	T_A	0	–	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	μA
Output Low Voltage (I_{OL} = 16mA)	I_{OL} = 10mA	V_{OL}			0.45	V
	I_{OL} = 16mA				0.50	
Output Leakage Current (V_O = 2.4V, Chip disabled)	MB7131	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4V, Chip disabled)	MB7132	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.45V, Chip disabled)	MB7132	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)	E/H/Y	I_{CC}		125**	175	mA
	L			45**	60	
Output High Voltage (I_O = -2.4mA)	MB7132	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB7132	I_{OS}*	-15		-60	mA

Note: *Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

**This value denotes conditions at T_A = 25°C and V_{CC} = +5.0V.

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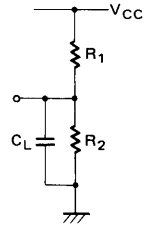
Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS
Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

	MB7131/MB7132		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	L		E		H		MB 7132Y/Y-SK		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	40	70	30	55	30	45	25	35	ns
Output Disable Time	t_{DIS}	15	50	15	40	15	30	15	25	ns
Output Enable Time	t_{EN}	25	50	15	40	15	30	15	25	ns

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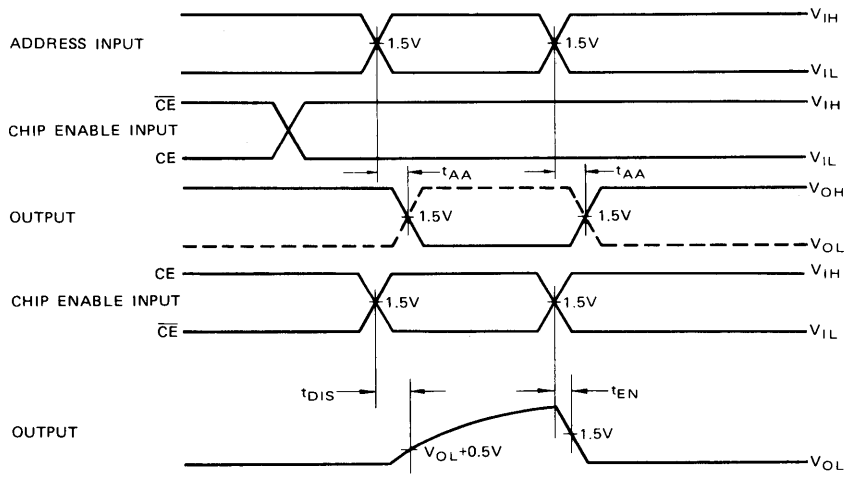
OPERATION TIMING DIAGRAM



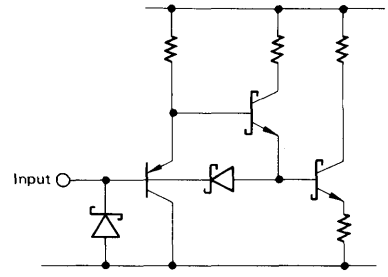
Note: Output disable time is the time taken for the output to reach a high resistance state when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Shottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

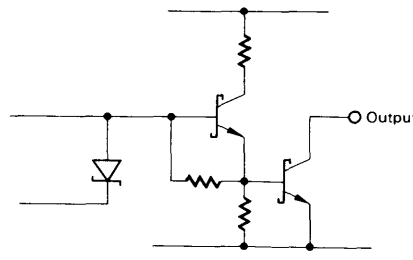
Fig. 3 – MB 7131/7132 INPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7132 (3-state) compared to 0mA for the MB 7131 (open-collector)

Fig. 4 – MB7131 OUTPUT



THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists

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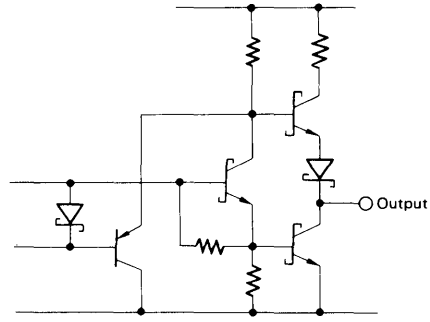
that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB 7132 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

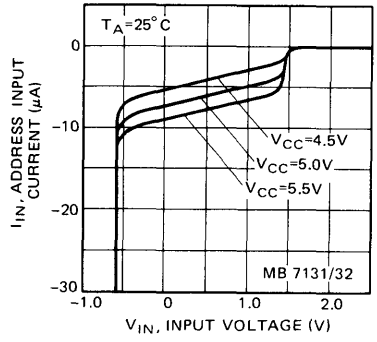

Fig. 7 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

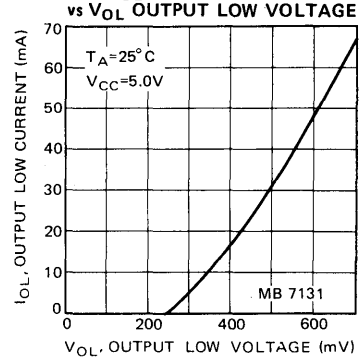

Fig. 8 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

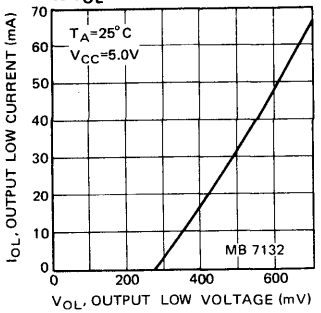

Fig. 9 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

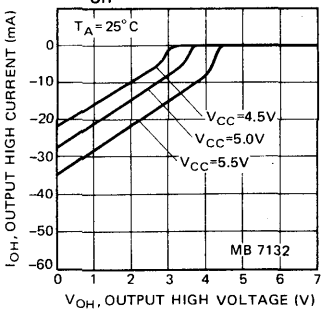

Fig. 10 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

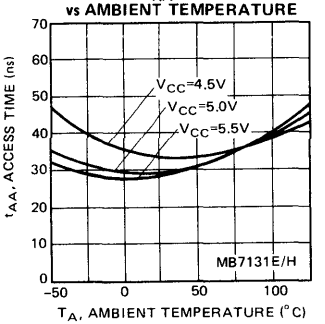

Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

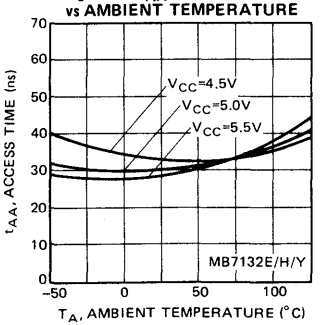

Fig. 12 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE

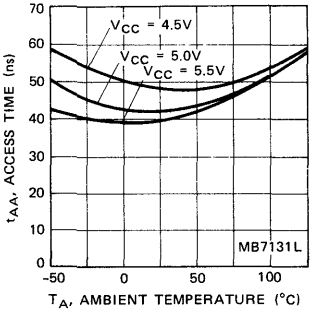

Fig. 13 – t_{AA} ACCESS TIME vs. AMBIENT TEMPERATURE

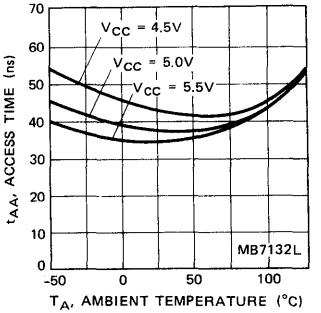

Fig. 14 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

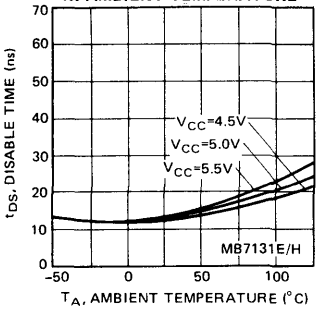

Fig. 15 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

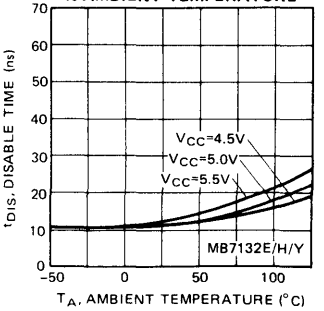

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Fig. 16 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

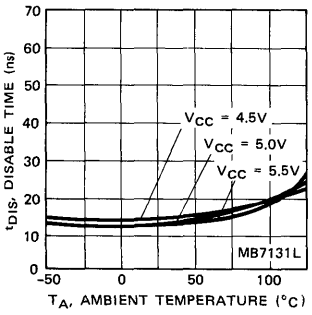


Fig. 17 – t_{DIS} DISABLE TIME vs. AMBIENT TEMPERATURE

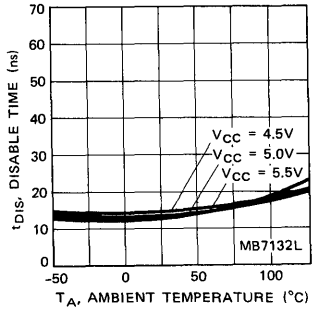


Fig. 18 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

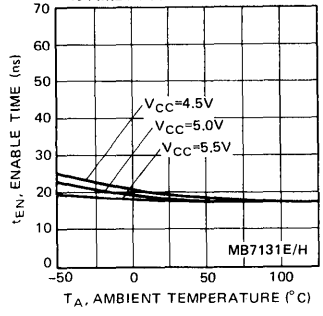


Fig. 19 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

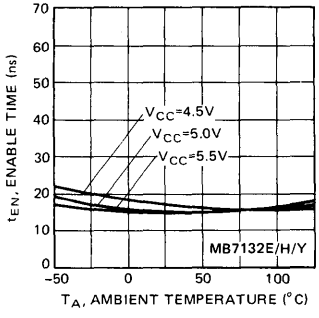


Fig. 20 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE

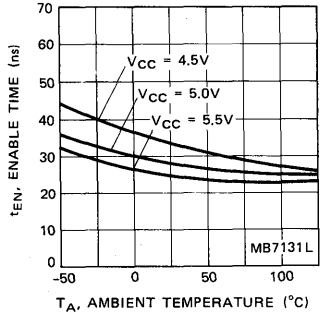


Fig. 21 – t_{EN} ENABLE TIME vs. AMBIENT TEMPERATURE

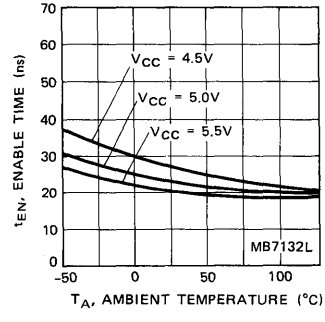


Fig. 22 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

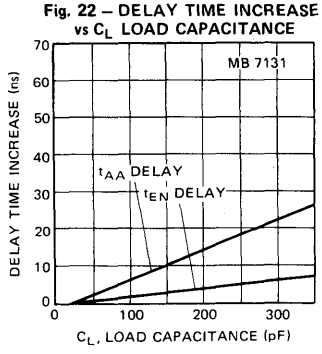
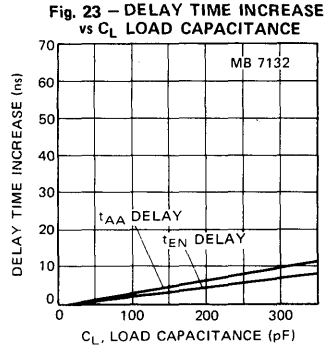


Fig. 23 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

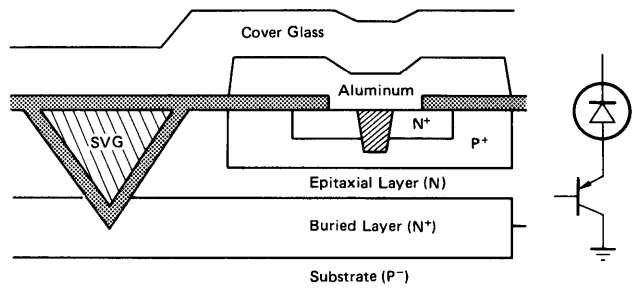
The Fujitsu MB 7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate (Fig. 24).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Groove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

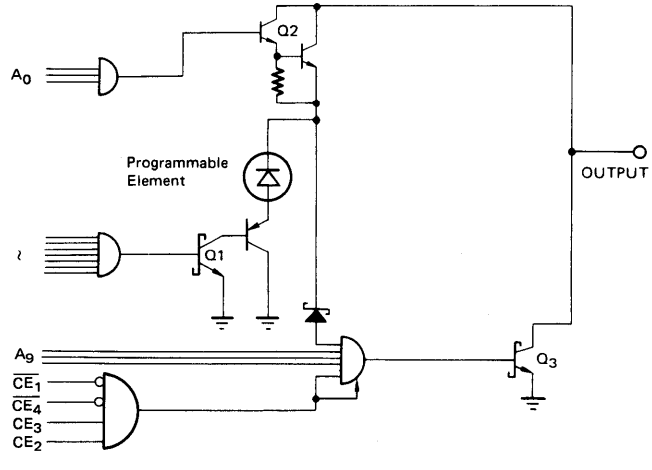
Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

Fig. 24 — PROGRAMMED CELL (CROSS SECTION)



Programmed by DEAP (Diffused Eutectic Aluminum Process)

Fig. 25 — INTERNAL PROGRAMMING CIRCUIT



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SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

"As shown in Fig. 25, transistors, Q_1 and Q_2, are turned on to select the desired bit for programming by using eight address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q_2 and memory cell into transistor Q_1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH} = 2.4V and V_{CC} = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

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DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH}		2.0		5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120		130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS (T_A = 25°C)

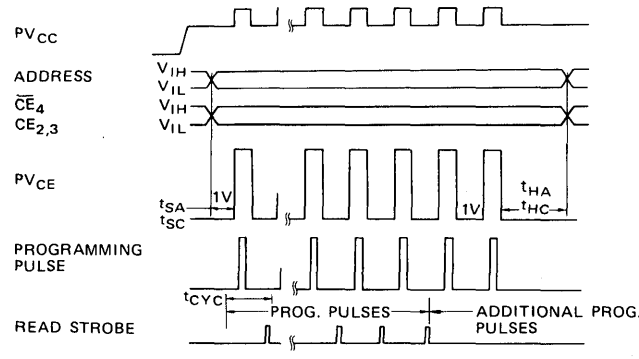
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW}(1)	10	11	12	μs
Programming Pulse Rise Time	t_r(2)	—	—	2	μs
PV_{CE} Pulse Rise Time	t_r(2)	—	—	2	μs
PV_{CC} Pulse Rise Time	t_r(3)	—	—	2	μs
Programming Pulse Fall Time	t_f(4)	—	—	2	μs
PV_{CE} Pulse Fall Time	t_f(4)	—	—	2	μs
PV_{CC} Pulse Fall Time	t_f(5)	—	—	2	μs
Address Input Set-up Time	t_{SA}	2	—	—	μs
Chip Enable Input Set-up Time	t_{SC}	2	—	—	μs
PV_{CE} Set-up Time	t_{SP}(6)	4	—	—	μs
Address Input Hold Time	t_{HA}	2	—	—	μs
Chip Enable Input Hold Time	t_{HC}	2	—	—	μs
PV_{CE} Hold Time	t_{HP}(7)	2	—	—	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(8)	10	—	—	μs
Programming Pulse Number	—	—	—	100	Times
Programming Time/Bit	—	120	150	6120	μs/bit
Additional Programming Pulse Number	—	2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

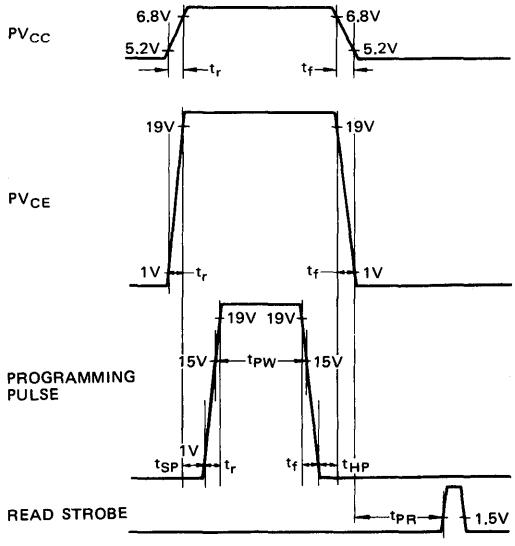
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



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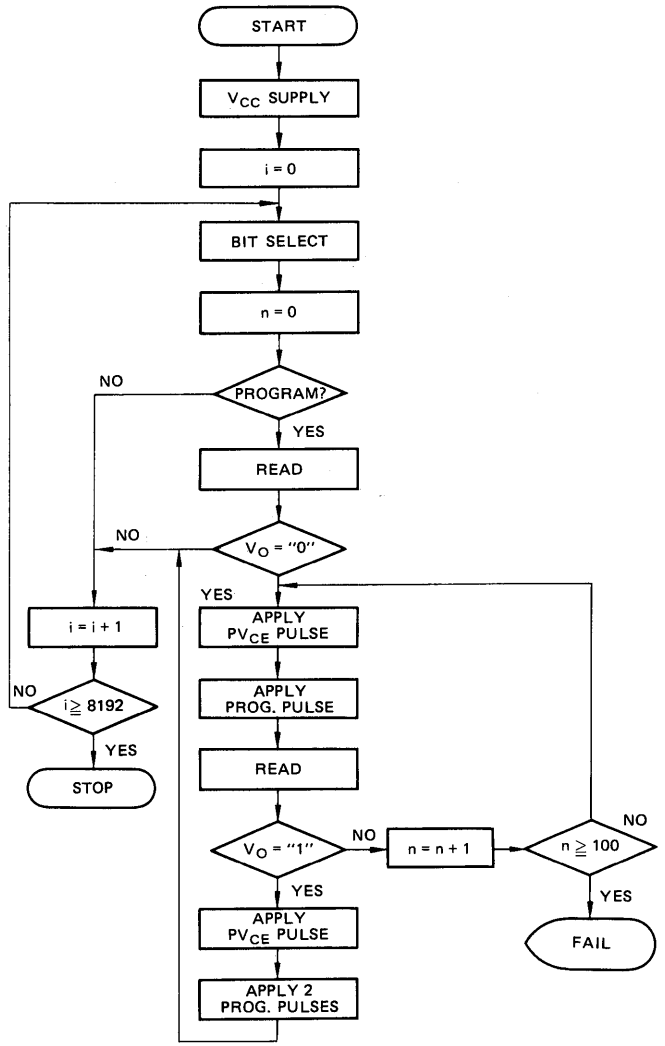
PROGRAMMING PROCEDURE

1. Apply power; $V_{CC} = PV_{CC}$, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 120mA and duration of t_{PW} (11μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

Fig. 26 – PROGRAMMING FLOW CHART



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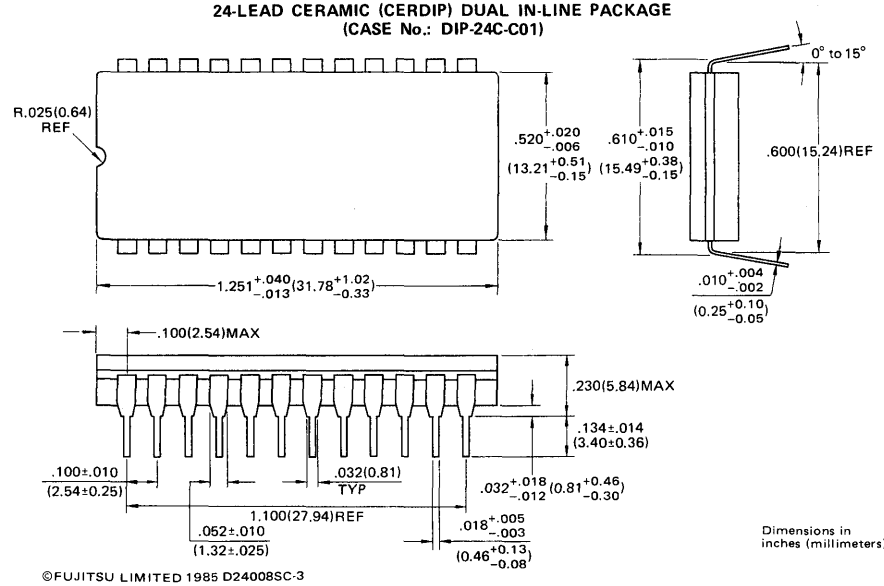
PACKAGE DIMENSIONS

(Suffix: -Z)

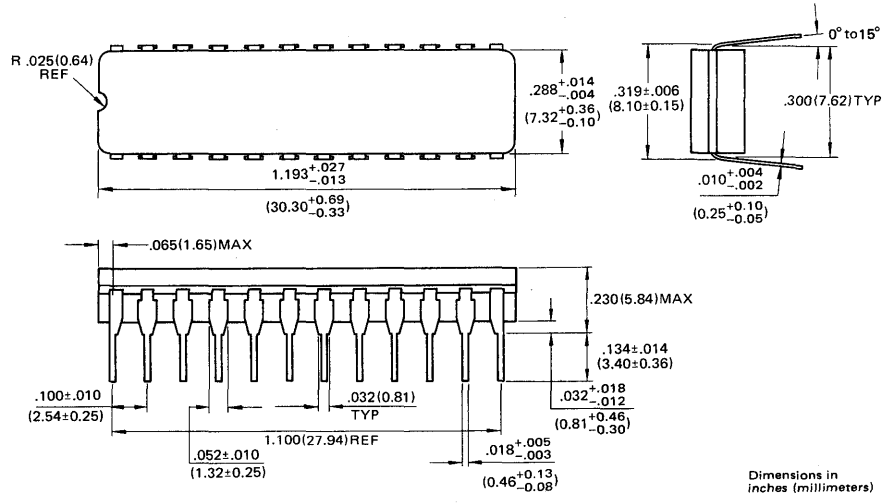
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C01)



Dimensions in inches (millimeters)

(Suffix: -Z)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C04)

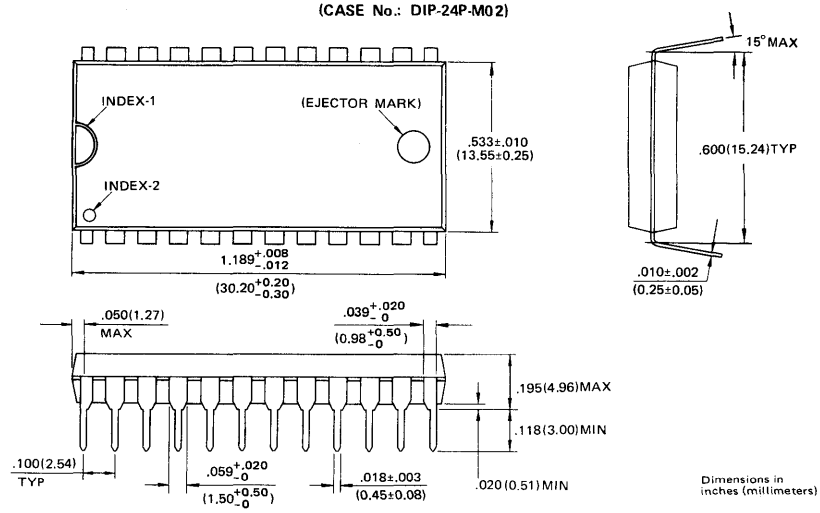


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

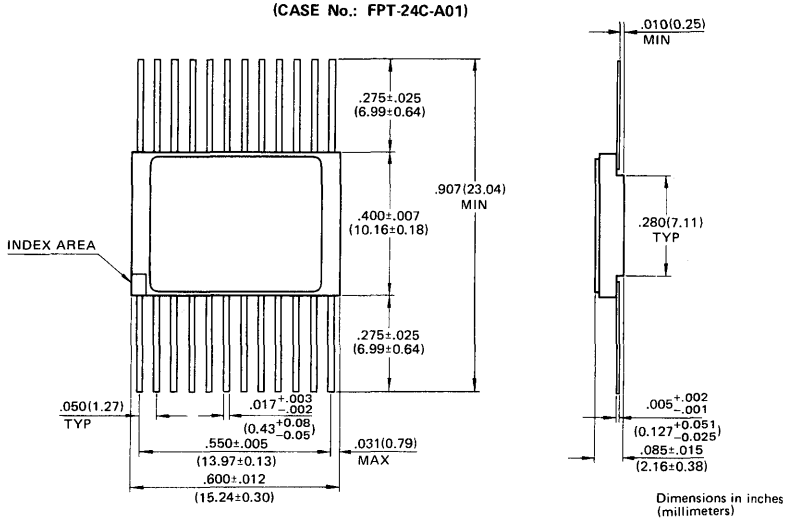
(Suffix: -M)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M02)



(Suffix: -CF)

24-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(CASE No.: FPT-24C-A01)



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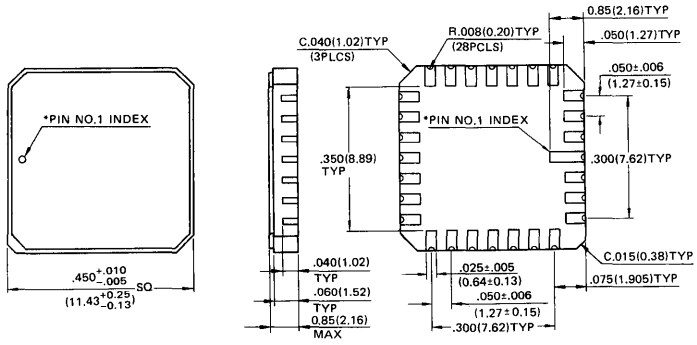
PACKAGE DIMENSIONS

(Suffix: -CV)

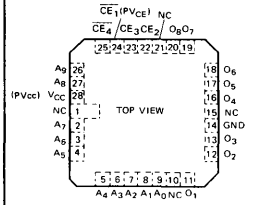
28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A01)



*Shape of Pin No.1 index: Subject to change without notice

Dimensions in inches (millimeters)

PAD CONFIGURATION



4

FUJITSU

PROGRAMMABLE SCHOTTKY 16384-BIT READ ONLY MEMORY

MB 7133E/H
MB 7134E/H/Y

November 1985
Edition 2.0

SCHOTTKY 16384-BIT DEAP PROM (4096 WORDS X 4 BITS)

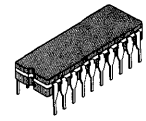
This Fujitsu MB 7133 and MB 7134 are high speed Schottky TTL electrically field programmable read only memories organized as 4096 words by 4 bits. With uncommitted collector output provided on the MB 7133 and three-state outputs on the MB 7134, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic Level "ones" can be programmed by the highly reliable Deap (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Poly-silicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

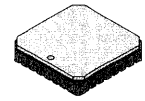
The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

- Single +5V supply voltage.
- 4096 words x 4 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by Deap (diffused eutectic aluminum process).
- Simplified and lower power programming.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time, 35ns typ
  MB 7134Y: 35ns max.
  H : 45ns max.
  E : 55ns max.
- TTL compatible inputs and outputs.
- Open collector (MB 7133)
- 3-state outputs (MB 7134)
- Two chip enables lead for simplified memory expansion.
- Standard 20 pin DIP package (: -CZ)
  Standard 28 pad LCC (: -CV)



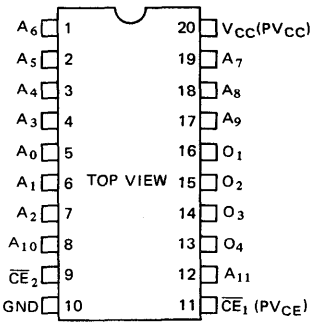
CERAMIC PACKAGE
DIP-20C-C03

CERAMIC PACKAGE
LCC-28C-A01



CERAMIC PACKAGE
LCC-28C-A02

PIN ASSIGNMENT



LCC PAD CONFIGURATION:
See Page 15 and 16

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	-0.5 to +7.5	V
Input Voltage	V_{IN}	-1.5 to 5.5	V
Input Voltage (during programming)	V_{IPRG}	22.5	V
Output Voltage	V_{OUT}	-0.5 to V_{CC}	V
Output Voltage (during programming)	V_{OPRG}	-0.5 to +22.5	V
Input Current	I_{IN}	-20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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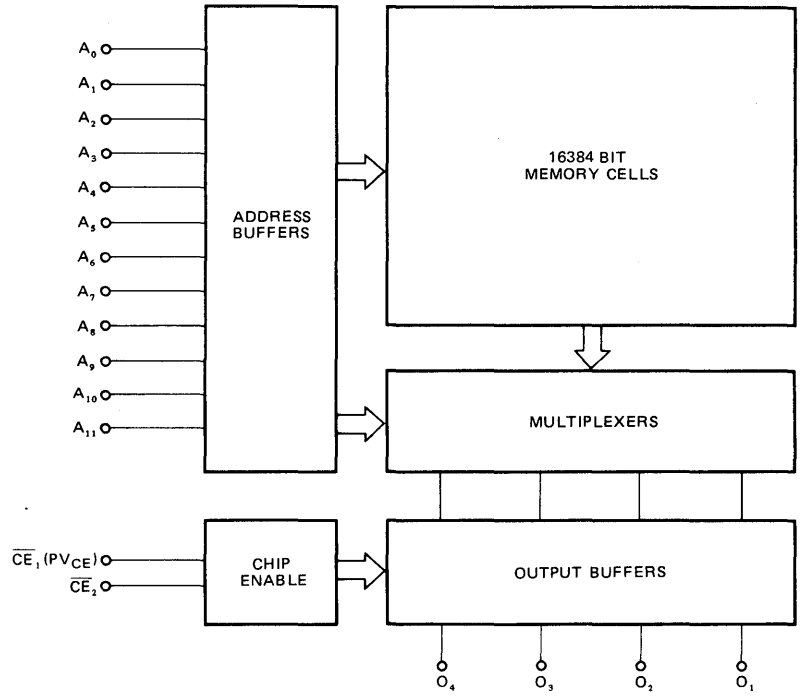
Fig. 1 – MB 7134 BLOCK DIAGRAM



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CAPACITANCE (f=1MHz, V_{CC}=+5V, V_{IN}=+2V, T_A=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	5.5	V
Ambient Temperature	T_A	0	–	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	μA
Output Low Voltage (I_{OL} = 10mA)		V_{OL}			0.45	V
Output Low Voltage (I_{OL} = 16mA)		V_{OL}			0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)	MB 7133	I_{OLK}			40	μA
	MB 7134	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.45V, chip disabled)	MB 7134	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}		120	170	mA
Output High Voltage (I_O = -2.4mA)	MB 7134	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB 7134	I_{OS}*	-15		-60	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{I\overline{CE}}$=0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

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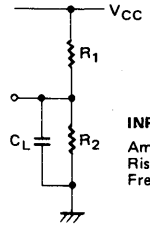
Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

	MB 7133/MB 7134		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	E		H		MB 7134Y		Unit
		Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	35	55	35	45	28	35	ns
Output Disable Time	t_{DIS}		40		40		30	ns
Output Enable Time	t_{EN}		40		40		30	ns

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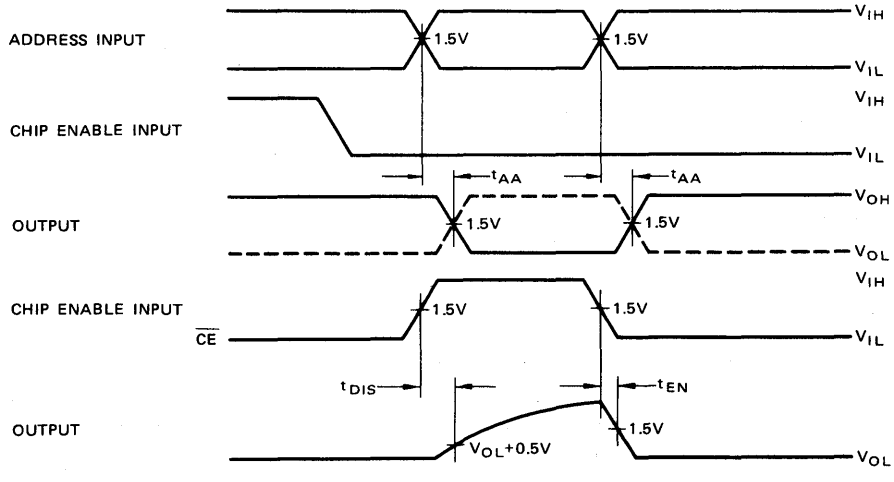
OPERATION TIMING DIAGRAM



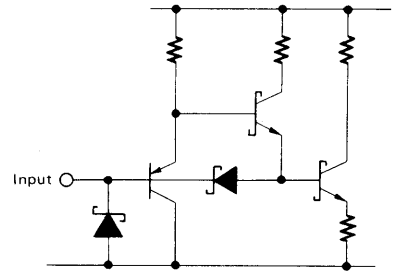
Note: Output disable time is the time taken for the output to reach a high resistance state when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

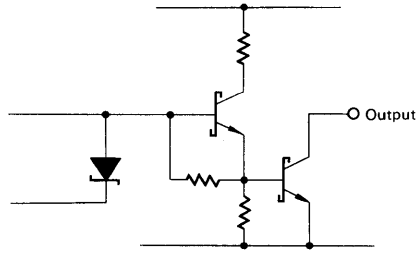
Fig. 3 – MB 7133/MB 7134 INPUT



OPEN COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7134 (3-state) compared to 0mA for the MB 7133 (open-collector)

Fig. 4 – MB 7133 OUTPUT



THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low

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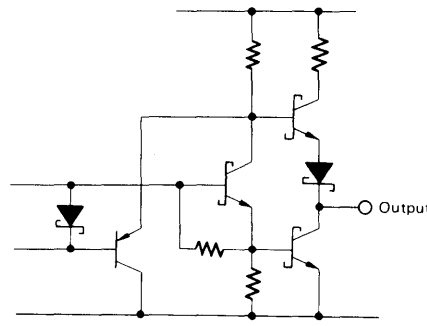
impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB 7134 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

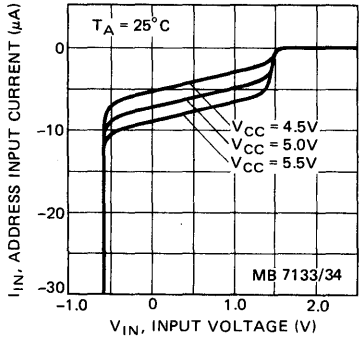

Fig. 7 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

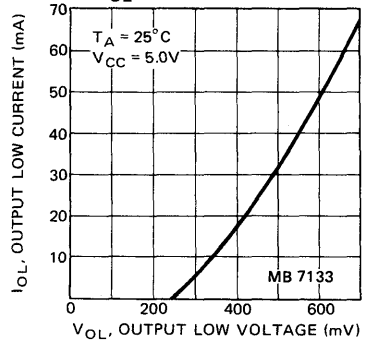

Fig. 8 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

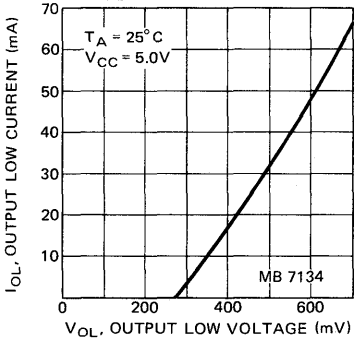

Fig. 9 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

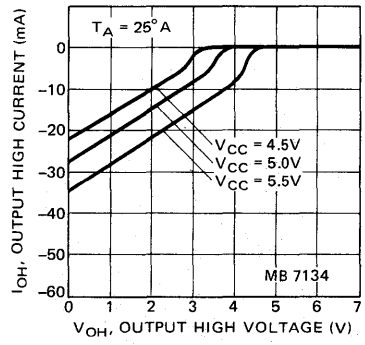

Fig. 10 – t_{AA}, ACCESS TIME vs AMBIENT TEMPERATURE

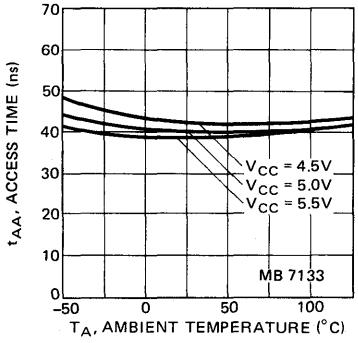

Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

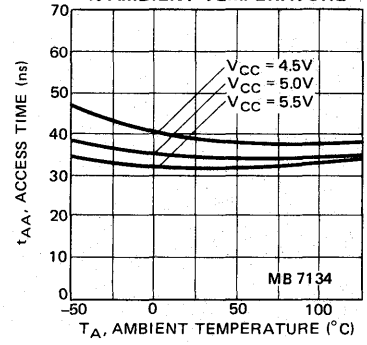

Fig. 12 – t_{DIS}, DISABLE TIME vs AMBIENT TEMPERATURE

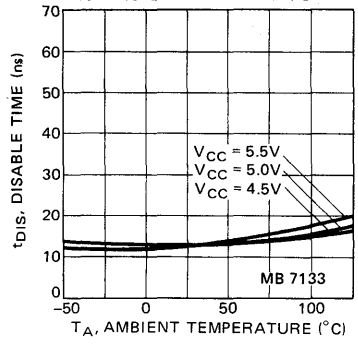

Fig. 13 – t_{DIS}, DISABLE TIME vs AMBIENT TEMPERATURE

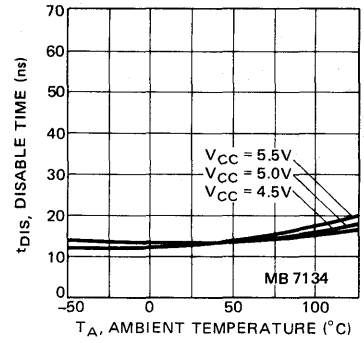

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Fig. 14 – t_{EN}, ENABLE TIME vs AMBIENT TEMPERATURE

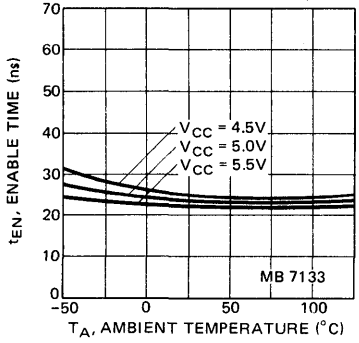


Fig. 15 – t_{EN}, ENABLE TIME vs AMBIENT TEMPERATURE

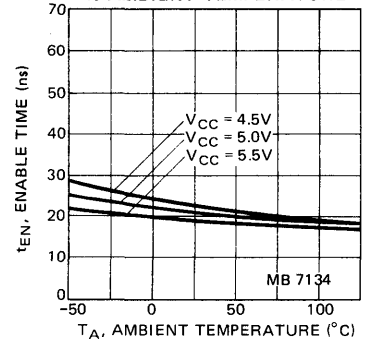


Fig. 16 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

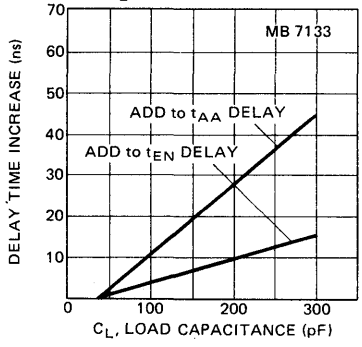
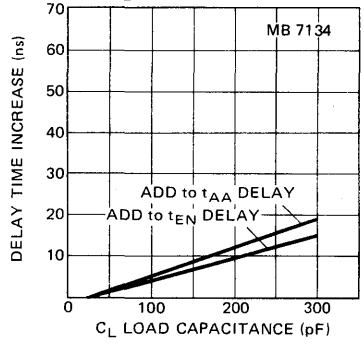


Fig. 17 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



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PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB 7100 series Schottky PROM is fabricated using Schottky TTL technology, passive isolation technology known as Isolation by Oxide and Poly-silicon (IOP), which is achieved by thin-epitaxial and Shallow V-Grooving (SVG), Diffused Eutectic Aluminum Process (Deap) technology with fine emitter and pulse programming method which achieve high-speed operation, high-speed programming, high programmability and high reliability.

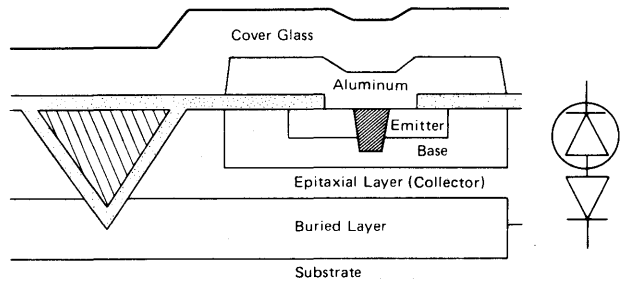
One memory cell is originally structured with a base-open NPN transistor and then programmed by shorting the base-emitter junction, i.e. shorted junction type cell which is achieved by eutectically melting aluminum and silicon adjacent to the P-N junction of cell diode with relatively low temperature, i.e. Deap technology.

Fast programming time of typically 150μs/bit is achieved with a fine emitter cell which requires less programming energy; the result is negligible thermal stress. This high reliability feature virtually eliminates aluminum migration in the programmed cell. Further, Fujitsu advanced technology allows very high programmability.

SPECIAL FACTORY TESTING

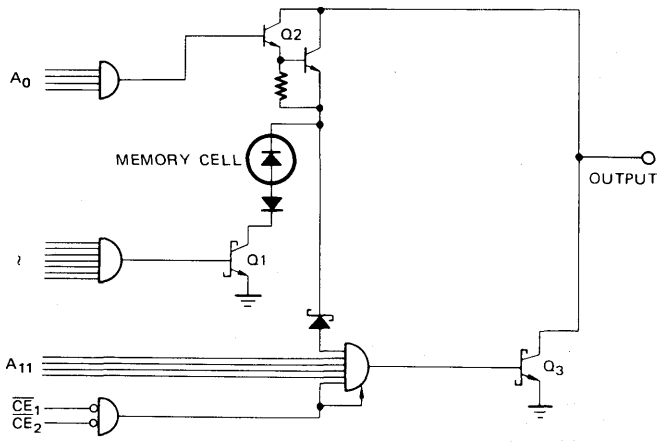
Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

Fig. 18 – PROGRAMMED CELL (CROSS SECTION)



▨ Programmed by diffused eutectic aluminum process (DEAP)

Fig. 19 – INTERNAL PROGRAMMING CIRCUIT



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PROGRAMMING INFORMATION (continued)

PROGRAMMING

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using twelve address inputs to turn on transistors Q1 and Q2. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the output voltage indicates that the selected bit is in the logic one state.

To assure that the element is programmed properly, two additional programming pulses are applied immediately after an output voltage indicates conduction in the programmed bit.

One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified when all chip enables are taken enable. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH} = 2.4V and V_{CC} = 7V at 25°C ambient temperature.

RELIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	–	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	–	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS (T_A = 25°C)

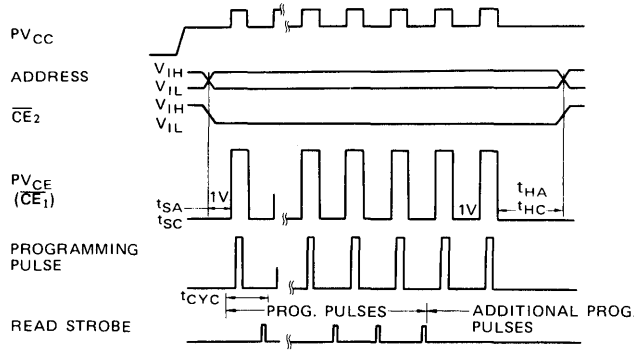
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW}(1)	10	11	12	μs
Programming Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r(3)	–	–	2	μs
Programming Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f(5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP}(6)	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
Chip Enable Input Hold Time	t_{HC}	2	–	–	μs
PV_{CE} Hold Time	t_{HP}(7)	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(8)	10	–	–	μs
Programming Pulse Number	n	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

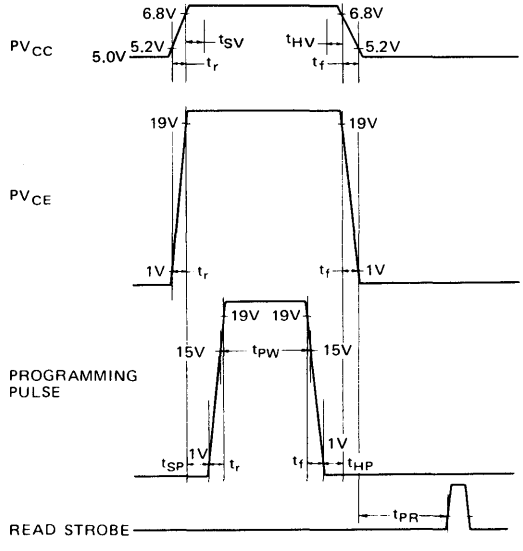
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE

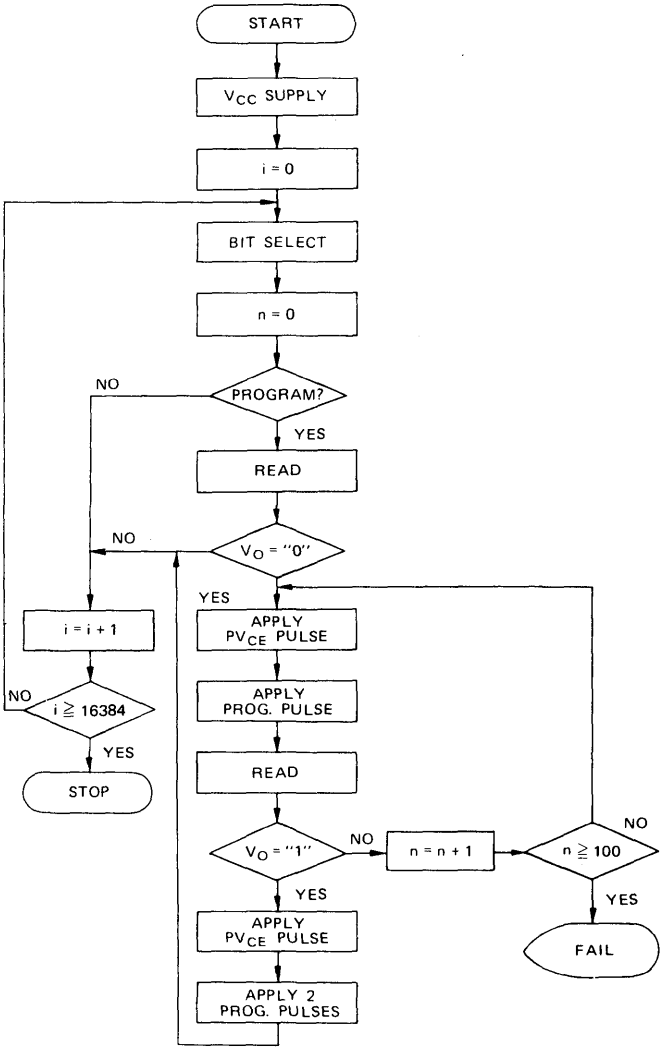


PROGRAMMING PROCEDURE

1. Apply power; V_{CC}=PV_{CC}, GND= 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O=low. (In the case of V_O=high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125 mA and duration of t_{PW} (11μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O=low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O=high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

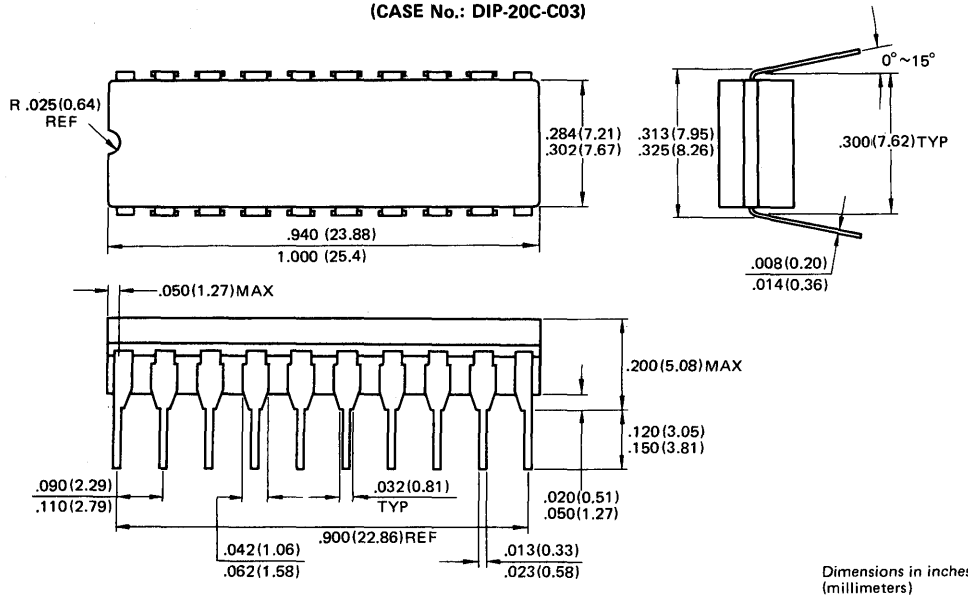
Fig. 20 – PROGRAMMING FLOW CHART



4

PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

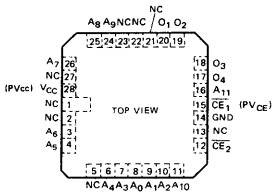


Dimensions in inches
(millimeters)

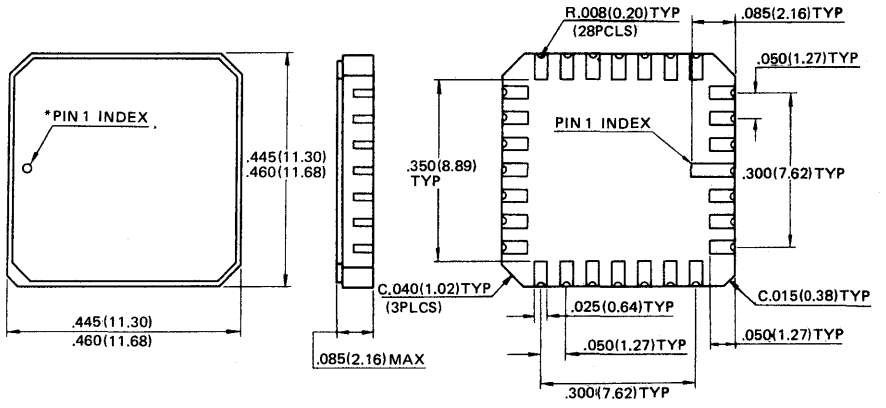
4

PACKAGE DIMENSIONS

PAD CONFIGURATION



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A01)



Dimensions in inches
(millimeters)

*Shape of Pin 1 index : Subject to change without notice

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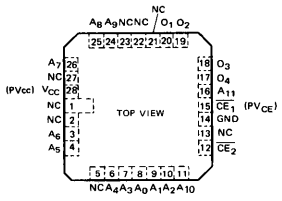
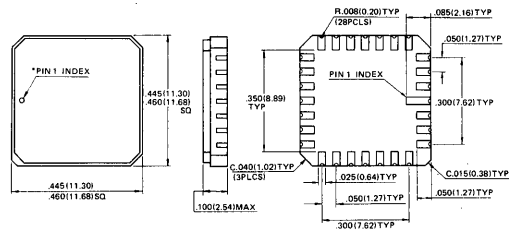
PACKAGE DIMENSIONS

PAD CONFIGURATION



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A02)



*Shape of Pin 1 index : Subject to change without notice

Dimensions in inches
(millimeters)

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FUJITSU

PROGRAMMABLE SCHOTTKY 16384-BIT READ ONLY MEMORY

MB7137E/H
MB7138E/H/Y
MB7137E-SK/H-SK
MB7138E-SK/H-SK/Y-SK

December 1987
Edition 2.0

SCHOTTKY 16384-BIT DEAP PROM (2048 OWRDS X 8 BITS)

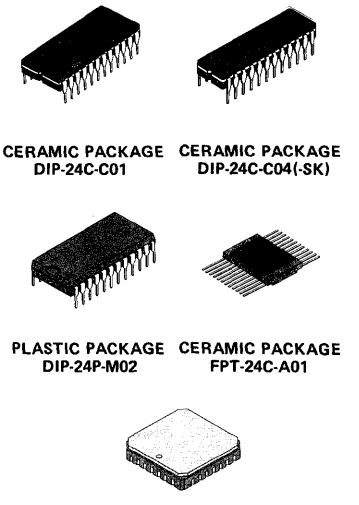
The Fujitsu MB7137 and MB7138 are high speed Schottky TTL electrically field programmable read only memories organized as 2048 words by 8 bits. With uncommitted collector outputs provided on the MB7137 and three-state outputs on the MB7138, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP(Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extemely high programmability.

- Single +5V supply voltage.
- 2048 words x 8 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time,35ns typ.
  Y : 35ns max. (MB7138)
  H : 45ns max.
  E : 55ns max.
- TTL compatible inputs and outputs.
- Open collector outputs (MB7137)
- 3 state outputs (MB7138)
- Three chip enable leads for simplified memory expansion.
- 300/600 mil standard 24-pin Ceramic (Cerdip) DIP
  (Suffix: -Z)
- Standard 24-pin Plastic DIP
  (Suffix: -M)
- Standard 24-pin Ceramic (Metal Seal) FPT
  (Suffix: -CF)
- Standard 28-pad Ceramic (Metal Seal) LCC
  (Suffix: -CV)
- JEDEC approved pin out.



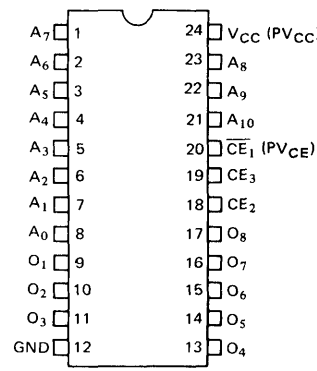
CERAMIC PACKAGE DIP-24C-C01 | CERAMIC PACKAGE DIP-24C-C04(-SK)

PLASTIC PACKAGE DIP-24P-M02 | CERAMIC PACKAGE FPT-24C-A01

CERAMIC PACKAGE LCC-28C-A02

4

PIN ASSIGNMENT



LCC PAD CONFIGURATION : See page 16

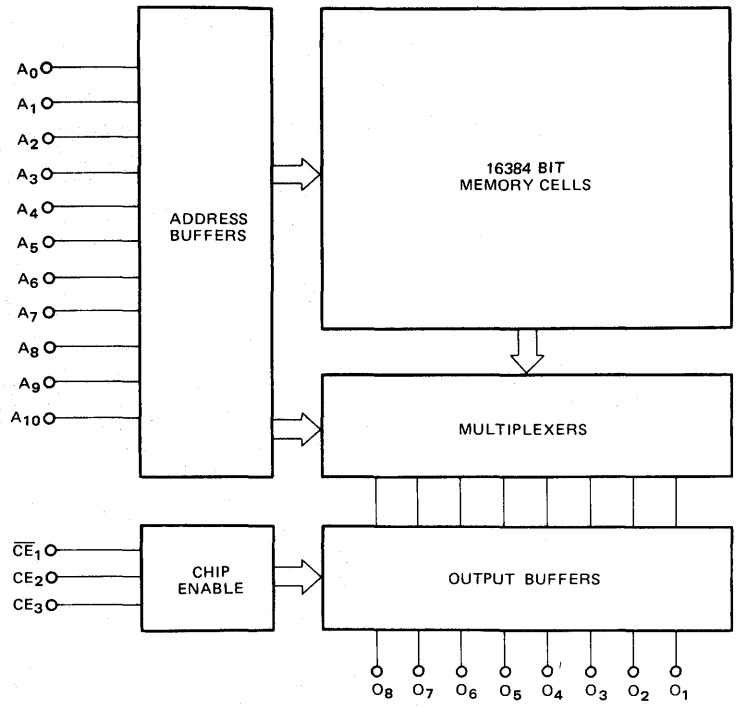
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CCP}	-0.5 to +7.5	V
Input Voltage		V_{IN}	-1.5 to +5.5	V
Input Voltage (during programming)		V_{IPRG}	22.5	V
Output Voltage (during programming)		V_{OPRG}	-0.5 to +22.5	V
Input Current		I_{IN}	-20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+150	mA
Storage Temperature	Ceramic	T_{STG}	-65 to +150	°C
	Plastic		-40 to +125	
Output Voltage		V_{OUT}	-0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 7137/7138 BLOCK DIAGRAM



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CAPACITANCE (f=1MHz, V_{CC}=+5V, V_{IN}=+2V, T_A=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	5.5	V
Ambient Temperature	T_A	0	–	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

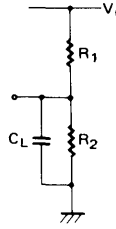
Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45V)		I_F			–250	μA
Output Low Voltage	I_{OL} = 10mA	V_{OL}			0.45	V
	I_{OL} = 16mA				0.50	
Output Leakage Current (V_O = 2.4V, chip disabled)	MB7137	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4V, chip disabled)	MB7138	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.5V, chip disabled)	MB7138	I_{OIL}			–40	μA
Input Clamp Voltage (I_{IN} = –18mA)		V_{IC}			–1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}		130**	180	mA
Output High Voltage (I_O = –2.4mA)	MB7138	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB7138	I_{OS}*	–15		–60	mA

Note: * Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4 V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

** This value denotes conditions at T_A = 25°C and V_{CC} = +5.0V.

4

Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

	MB 7137/MB 7138		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

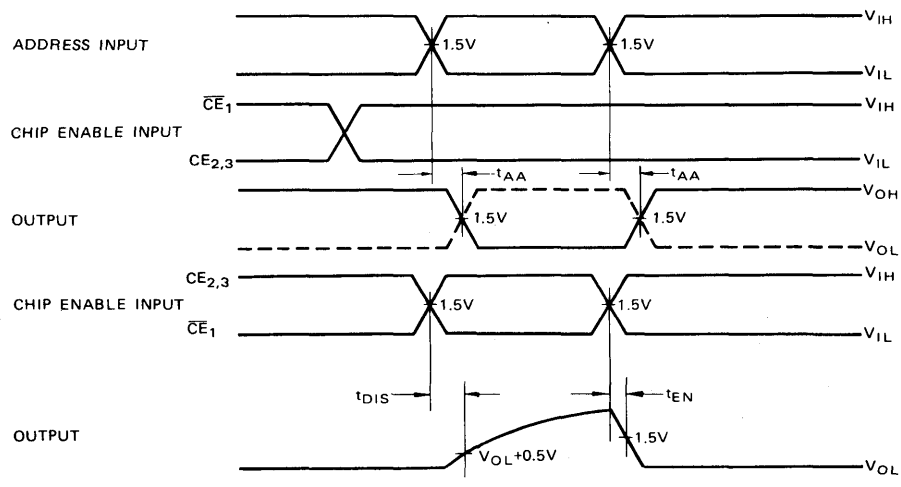
AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	E		H		MB7138Y/Y-SK		Unit
		Typ	Max	Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	35	55	35	45	30	35	ns
Output Disable Time	t_{DIS}	15	40	15	40	15	30	ns
Output Enable Time	t_{EN}	20	40	20	40	20	30	ns

4

OPERATION TIMING DIAGRAM



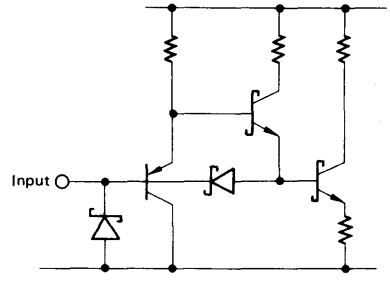
Note: Output disable time is the time taken for the output to reach a high resistance state when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Shottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

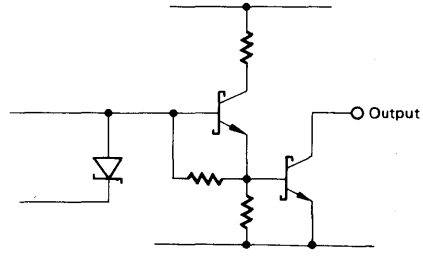
Fig. 3 – MB 7137/7138 INPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7138 (3-state) compared to 0mA for the MB 7137 (open-collector)

Fig. 4 – MB 7137 OUTPUT



THREE-STATE OUTPUT

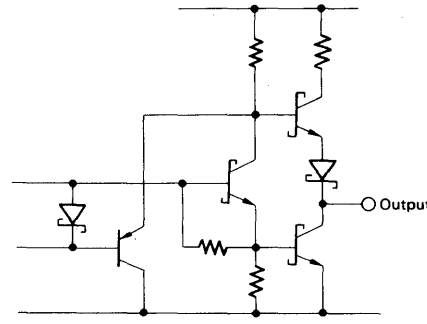
A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists

that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB 7138 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

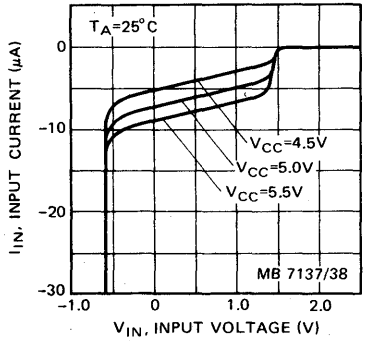

Fig. 7 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

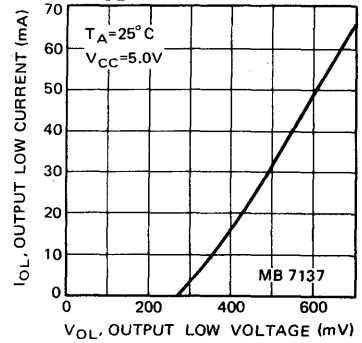

Fig. 8 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

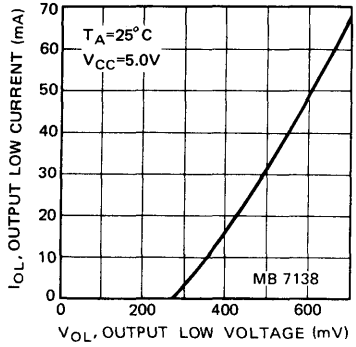

Fig. 9 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE

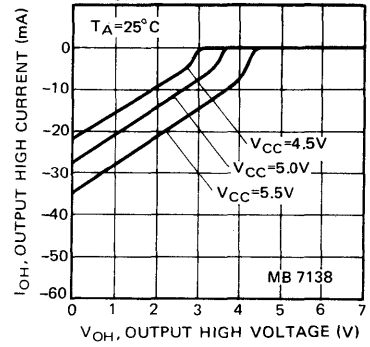

Fig. 10 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

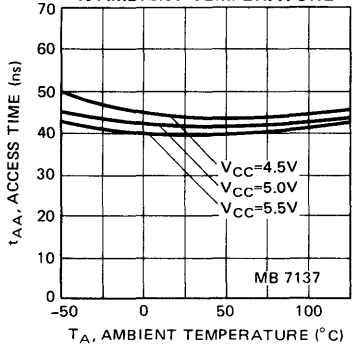

Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

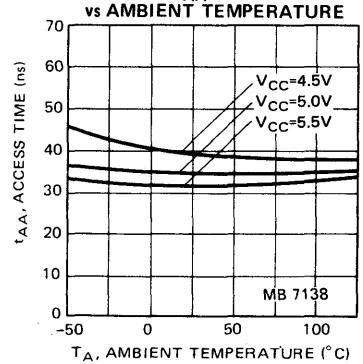

Fig. 12 – t_{DS} DISABLE TIME vs AMBIENT TEMPERATURE

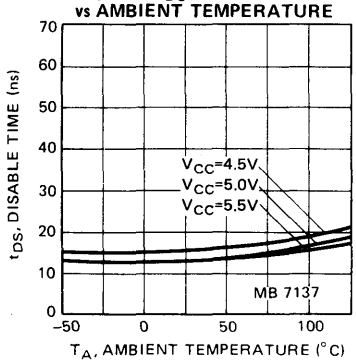

Fig. 13 – t_{DIS} DISABLE TIME vs AMBIENT TEMPERATURE

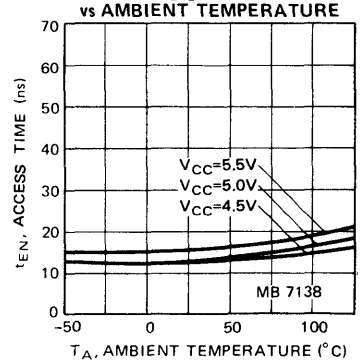

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Fig. 14 – t_{EN} ENABLE TIME vs AMBIENT TEMPERATURE

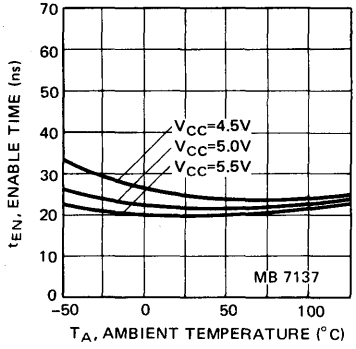


Fig. 15 – t_{EN} ACCESS TIME vs AMBIENT TEMPERATURE

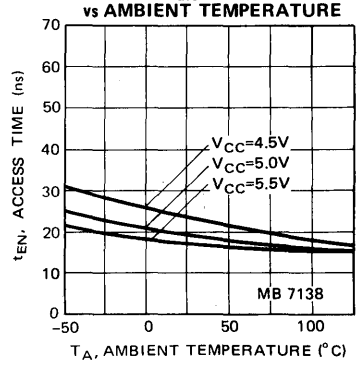


Fig. 16 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

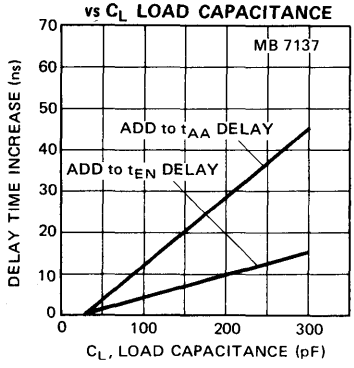
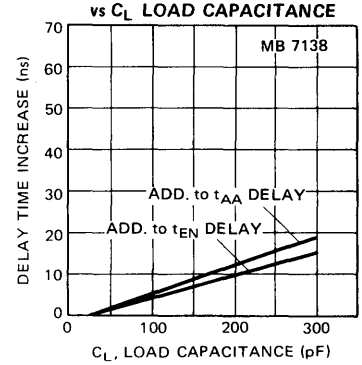


Fig. 17 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



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PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB 7100 series is the junction-shorting Schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate (Fig. 18).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the passive isolation named SVG (Shallow V-Groove). The vertical structure of the junction-shorting memory cell makes a high packing density possible.

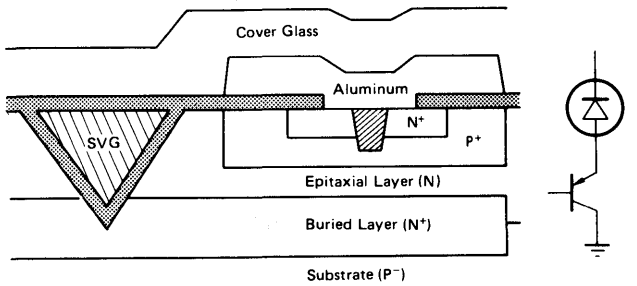
In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the function decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

SPECIAL FACTORY TESTING

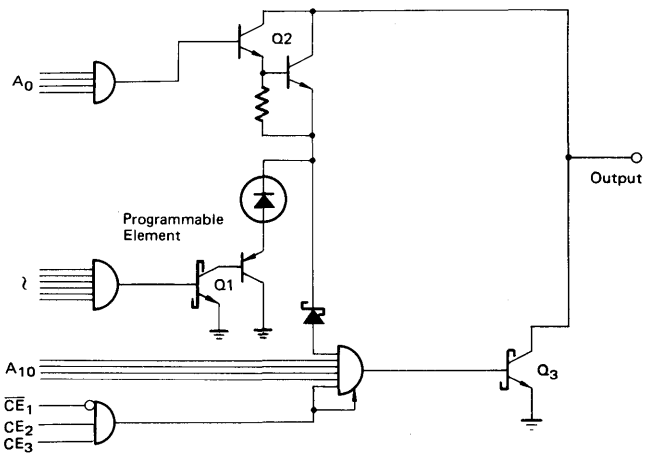
Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test

Fig. 18 – PROGRAMMED CELL (CROSS SECTION)



Programmed by DEAP (Diffused Eutectic Aluminum Process)

Fig. 19 – INTERNAL PROGRAMMING CIRCUIT



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cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

"As shown in Fig. 19, transistors, O_1 and O_2, are turned on to select the desired bit for programming by using nine address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor O_3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor O_2 and memory cell into transistor O_1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at $V_{OH} = 2.4V$ and $V_{CC} = 7.0V$ at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	–	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	–	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW} (1)	10	11	12	μs
Programming Pulse Rise Time	t_r (2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r (2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r (3)	–	–	2	μs
Programming Pulse Fall Time	t_f (4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f (4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f (5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP} (6)	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
Chip Enable Input Hold Time	t_{HC}	2	–	–	μs
PV_{CE} Hold Time	t_{HP} (7)	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (8)	10	–	–	μs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

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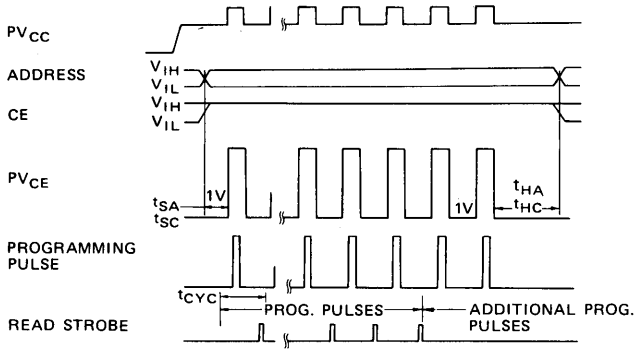
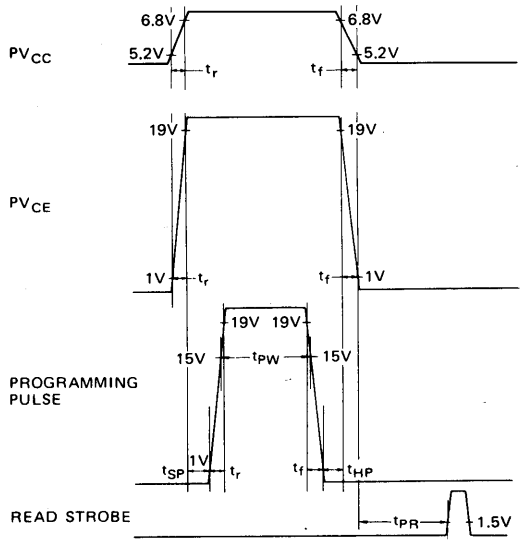
PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



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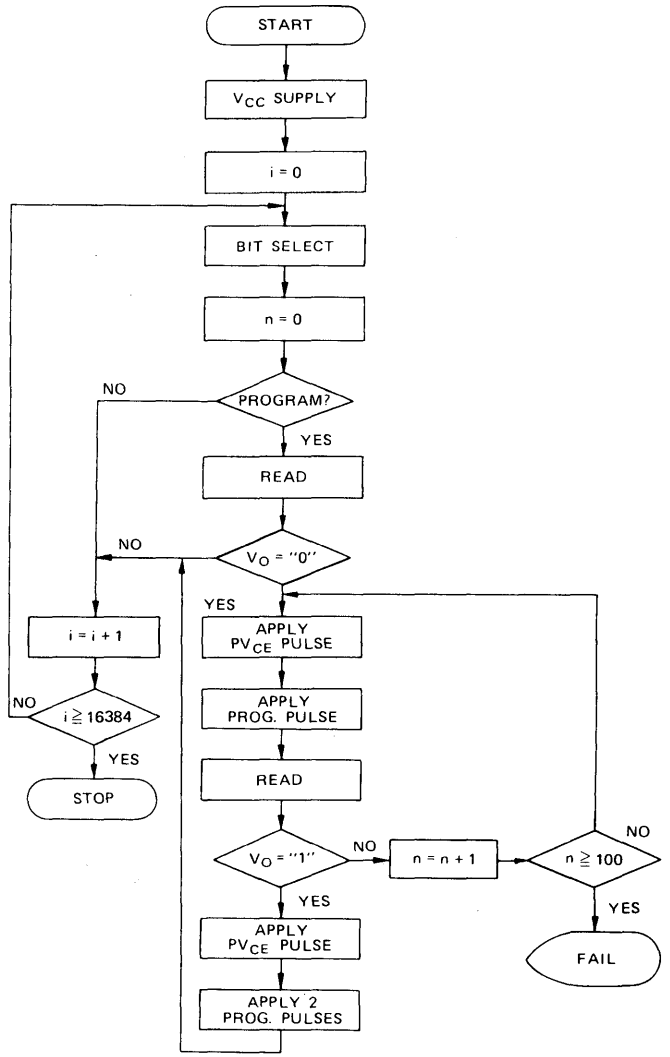
PROGRAMMING PROCEDURE

1. Apply power; V_{CC}=PV_{CC}, GND=0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O=low. (In the case of V_O=high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125 mA and duration of t_{PW} (11μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O=low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μs).
   b) In the case of V_O=high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

Fig. 20 – PROGRAMMING FLOW CHART



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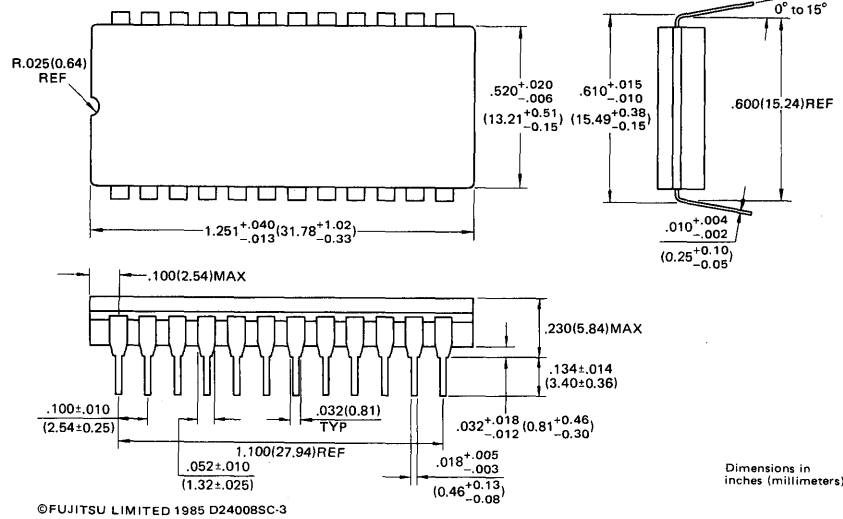
PACKAGE DIMENSIONS

(Suffix: -Z)

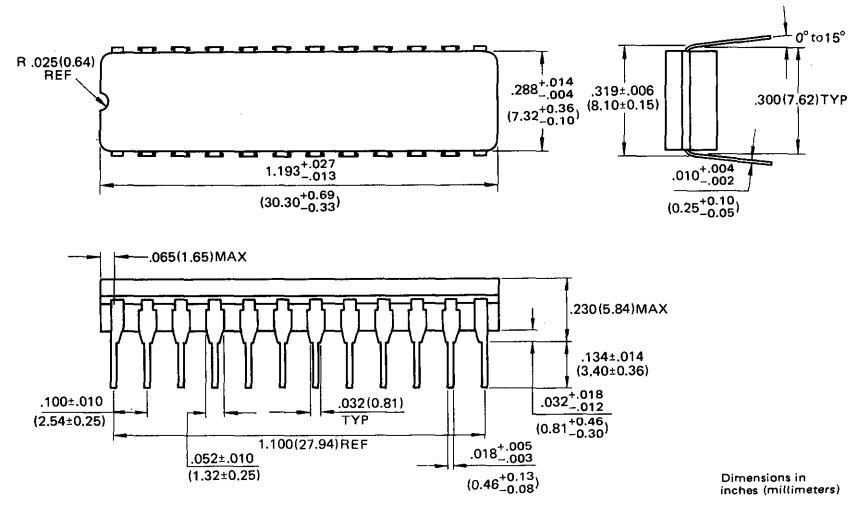
24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C01)



Dimensions in inches (millimeters)

(Suffix: -Z)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C04)

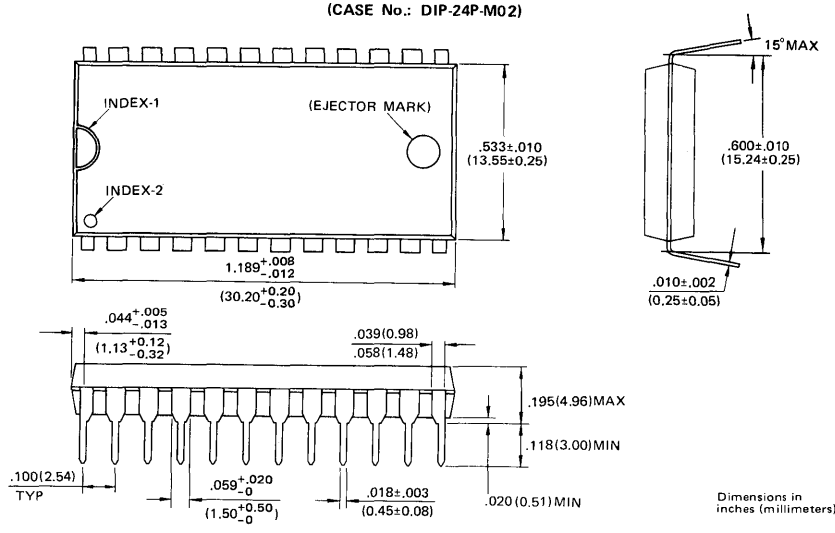


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

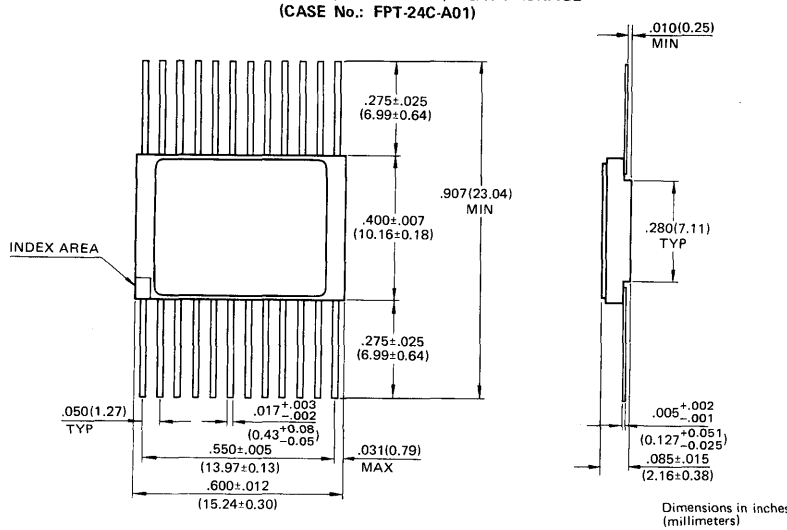
(Suffix: -M)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M02)



(Suffix: -CF)

24-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(CASE No.: FPT-24C-A01)



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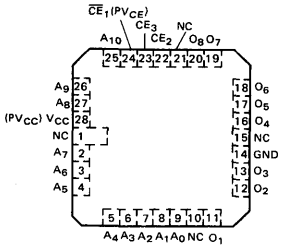
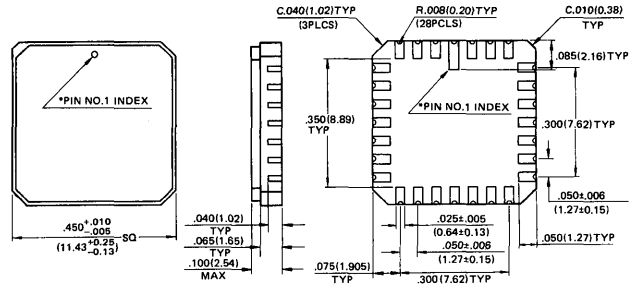
PACKAGE DIMENSIONS

(Suffix: -CV)

PAD ASSIGNMENT



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A02)



*Shape of Pin NO. 1 index : Subject to change without notice

Dimensions in inches (millimeters)

4

FUJITSU

PROGRAMMABLE SCHOTTKY 32768-BIT READ ONLY MEMORY

MB7142E/H

November 1988
Edition 4.0

SCHOTTKY 32768-BIT DEAP PROM (4096 WORDS x 8 BITS)

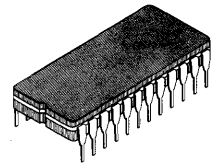
The Fujitsu MB7142 is high speed schottky TTL electrically field programmable read only memory organized as 4096 words by 8 bits. With threestate outputs, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP(Diffused Eutectic Aluminum Process) according to simple programming procedures.

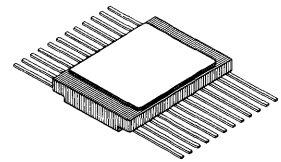
The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

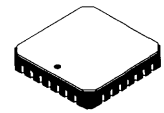
- Single +5V supply voltage.
- 4096 words x 8 bits organization , fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time, 45ns typ.
  E: 65ns max.
  H: 55ns max.
- TTL compatible inputs and outputs.
- 3 State outputs.
- Two chip enable pins for simplified memory expansion.
- Standard 24-pin Ceramic DIP
- Standard 24-pin Ceramic FPT
- Standard 28-pad Ceramic LCC
- JEDEC approved pin out



CERAMIC PACKAGE
DIP-24C-C-03



CERAMIC PACKAGE
FPT-24C-A01



CERAMIC PACKAGE
LCC-28C-A01

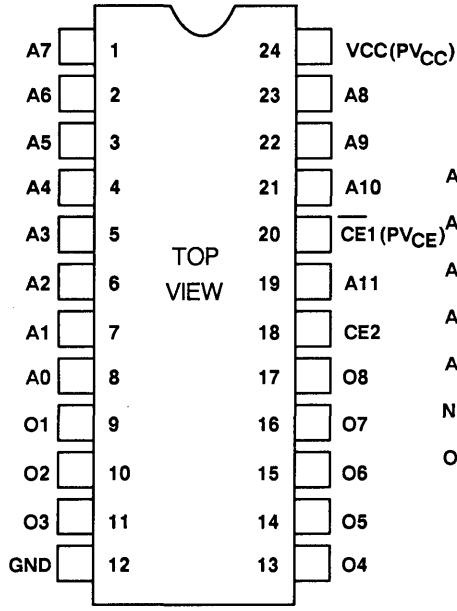
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CCP}	-0.5 to +7.5	V
Input Voltage	V_{IN}	-1.5 to 5.5	V
Input Voltage(during programming)	V_{IPRG}	22.5	V
Output Voltage(during programming)	V_{OPRG}	-0.5 to +22.5	V
Input Current	I_{IN}	-20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Output Voltage	V_{OUT}	-0.5 to 5.5	V

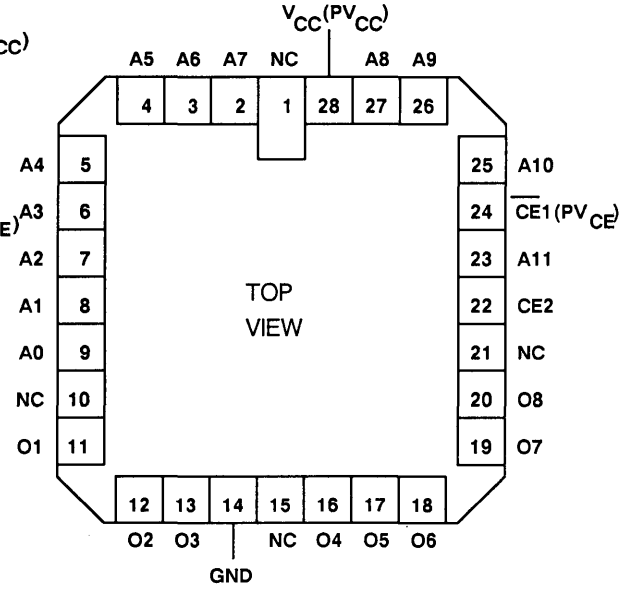
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT



PAD CONFIGURATION



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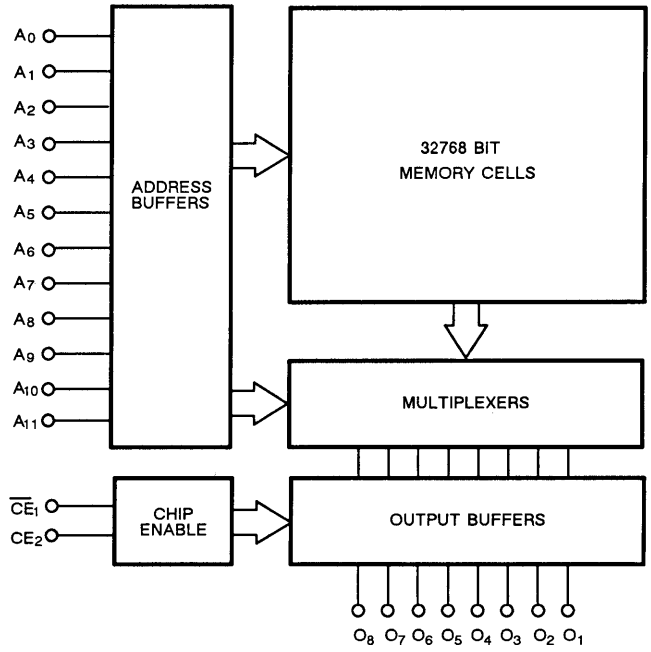
MB7142 MODE SELECTION

MODE	$\overline{CE1}$	CE2	Output $O_1 \sim O_8$
READ	V_{IL}	V_{IH}	D_{OUT}
CHIP-DISABLE	V_{IH}	*	HZ
	*	V_{IL}	
WRITE	PV_{CE}	*	HZ

* : any TTL level
HZ : high-impedance
D_{OUT} : memory answer
PV_{CE} : 20V (see programming information)

Fig. 1 — MB7142 BLOCK DIAGRAM



CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25 °C)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	5.5	V
Ambient Temperature	T_A	0	-	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	µA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	µA
Output Low Voltage	I_{OL} = 10mA	V_{OL}			0.45	V
	I_{OL} = 16mA				0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)		I_{OIH}			40	µA
Output Leakage Current (V_O = 0.45V, chip disabled)		I_{OIL}			-40	µA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}		140**	185	mA
Output High Voltage (I_O = -2.4mA)		V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)		I_{OS}*	-15		-60	mA

Note: * Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4V, V_{CE} = 2.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

** This value denotes conditions at T_A=25°C and V_{CC} = +5.0V

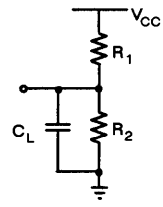


Fig. 2 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

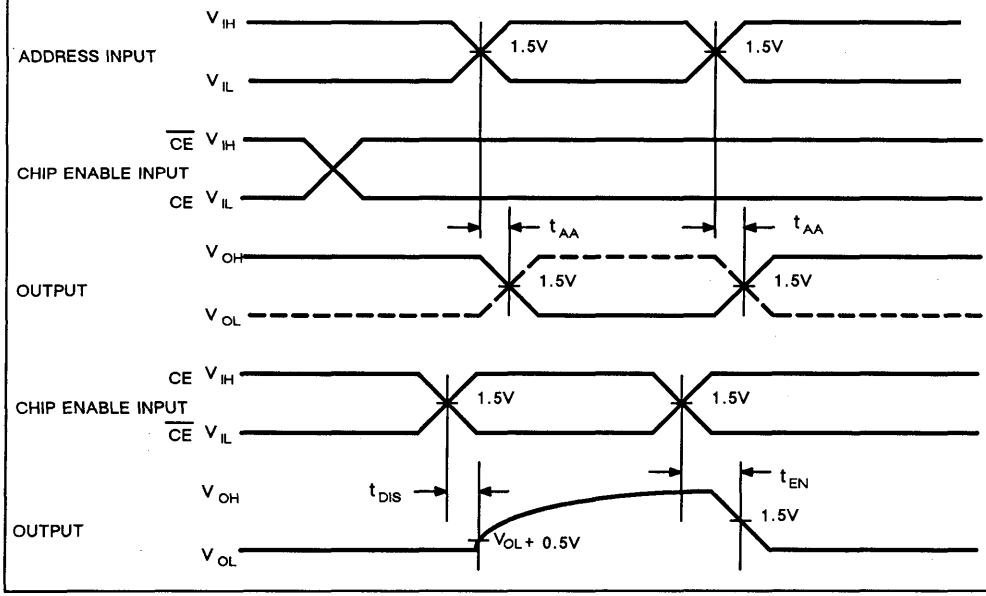
	MB7142		
	R_1	R_2	C_L
t_{AA}	300 Ω	600 Ω	30pF
t_{DIS}	300 Ω	600 Ω	30pF
t_{EN}	300 Ω	600 Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter	Symbol	E		H		Unit
		Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	45	65	45	55	ns
Output Disable Time	t_{DIS}	15	40	15	40	ns
Output Enable Time	t_{EN}	20	40	20	40	ns

OPERATION TIMING DIAGRAM



Note: Output disable time is the time taken for the output to reach a high resistance when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

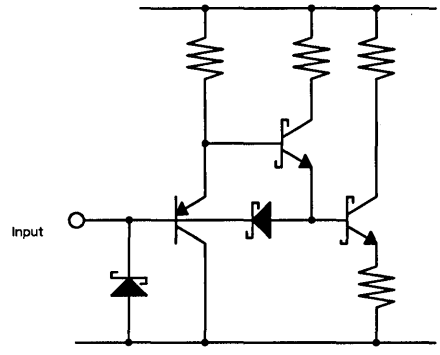
4

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Fig. 3 - MB7142 INPUT



THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 4 - MB7142 OUTPUT

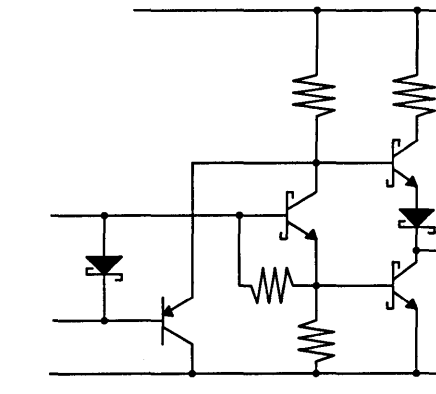


Fig.5-I_{IN} INPUT CURRENT VS. V_{IN} INPUT VOLTAGE

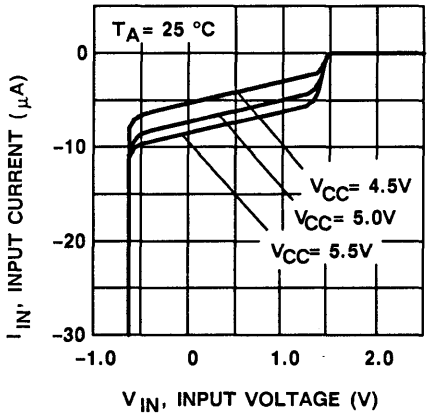


Fig.6-I_{OL} OUTPUT LOW CURRENT VS. V_{OL} OUTPUT LOW VOLTAGE

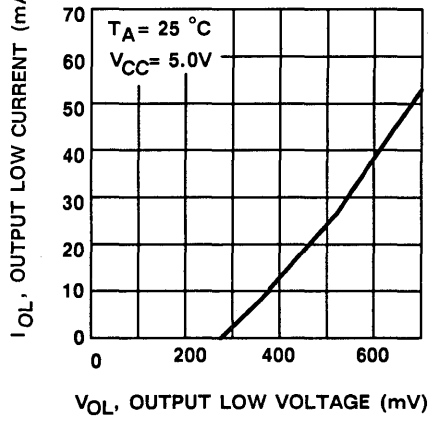


Fig.7-I_{OH} OUTPUT HIGH CURRENT VS. V_{OH} OUTPUT HIGH VOLTAGE

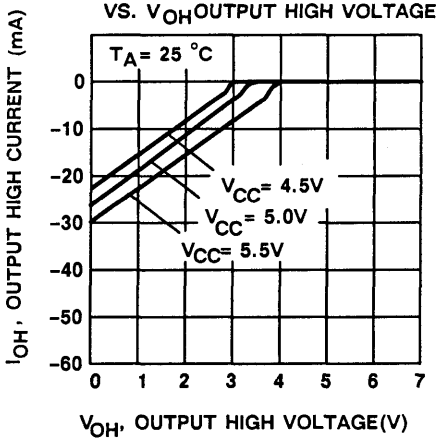


Fig.8-t_{AA} ACCESS TIME VS. AMBIENT TEMPERATURE

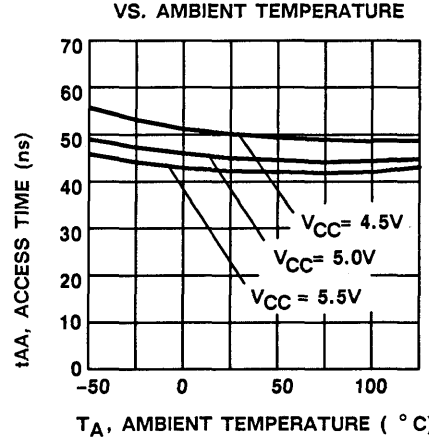


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Fig.9-t_{DIS} DISABLE TIME VS. AMBIENT TEMPERATURE

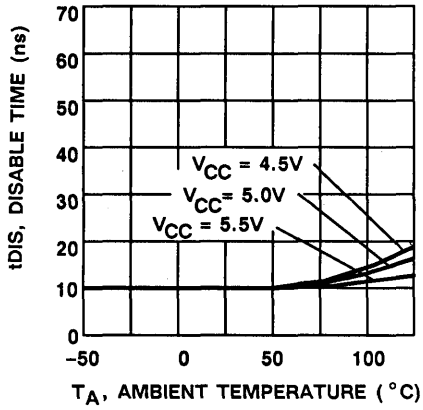

Fig.10-t_{EN} ENABLE TIME VS. AMBIENT TEMPERATURE

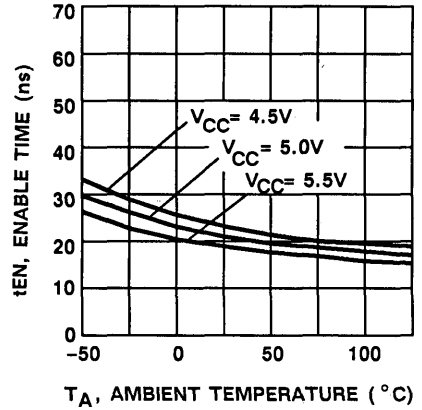

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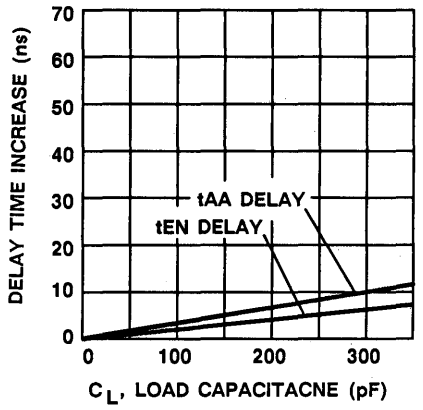
Fig.11-DELAY TIME INCREASE VS. C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB7100 series is the junction-shorting schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate(Fig. 12).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the pasive isolation named SVG (Shallow V-Groove).

The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

Fig. 12 - PROGRAMMED CELL (CROSS SECTION)

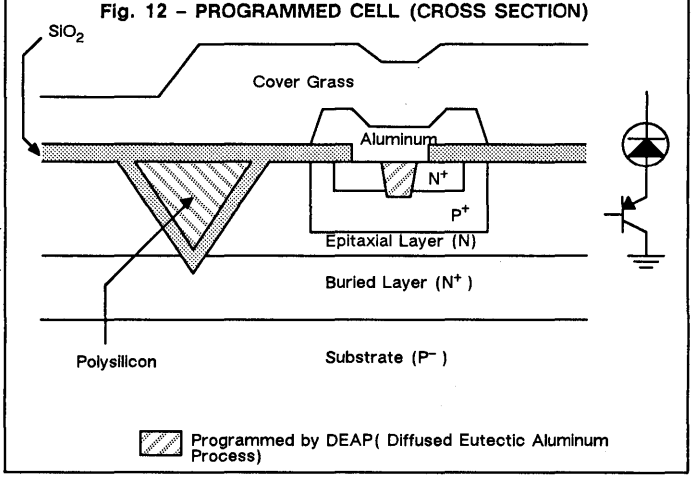
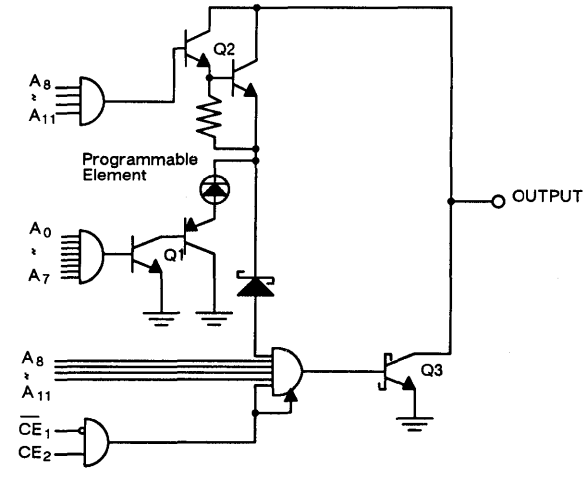


Fig. 13 - INTERNAL PROGRAMMING CIRCUIT



4

PROGRAMMING INFORMATION (continued)

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

As shown in Fig. 13, transistors, Q1 and Q2, are turned on to select the desired bit for programming by using twelve address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q2 and memory cell into transistor Q1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified when all of chip enables are taken enable. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{CC}= 2.4V and V = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH}		2.0		5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	V
Programming Pulse Current	I_{PRG}		120		130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS (T_A = 25°C)

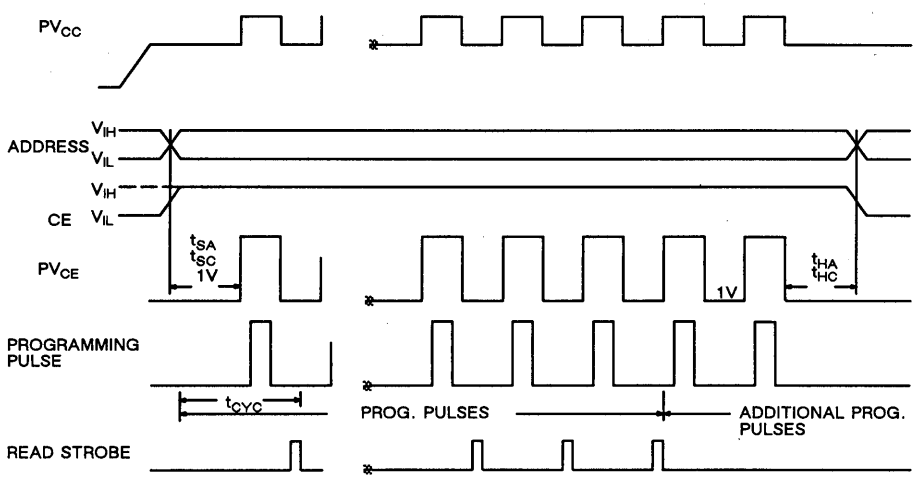
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	µs
Programming Pulse Width	t_{PW} (1)	10	11	12	µs
Programming Pulse Rise Time	t_r (2)	–	–	2	µs
PV_{CE} Pulse Rise Time	t_r (3)	–	–	2	µs
PV_{CC} Pulse Rise Time	t_r (4)	–	–	2	µs
Programming Pulse Fall Time	t_f (5)	–	–	2	µs
PV_{CE} Pulse Fall Time	t_f (6)	–	–	2	µs
PV_{CC} Pulse Fall Time	t_f (7)	–	–	2	µs
Address Input Set-up Time	t_{SA}	2	–	–	µs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	µs
PV_{CE} Set-up Time	t_{SP} (8)	4	–	–	µs
Address Input Hold Time	t_{HA}	2	–	–	µs
Chip Enable Input Hold Time	t_{HC}	2	–	–	µs
PV_{CE} Hold Time	t_{HP} (9)	2	–	–	µs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (10)	10	–	–	µs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	µs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Note: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 1V to 19V.
(4) From 5.2V to 6.8V.
(5) From 19V to 1V (200Ω load).
(6) From 19V to 1V.
(7) From 6.8V to 5.2V.
(8) From PV_{CE} pulse 19V to programming pulse 1V.
(9) From programming pulse 1V to PV_{CE} pulse 19V.
(10) From PV_{CE} pulse 1V to read strobe.

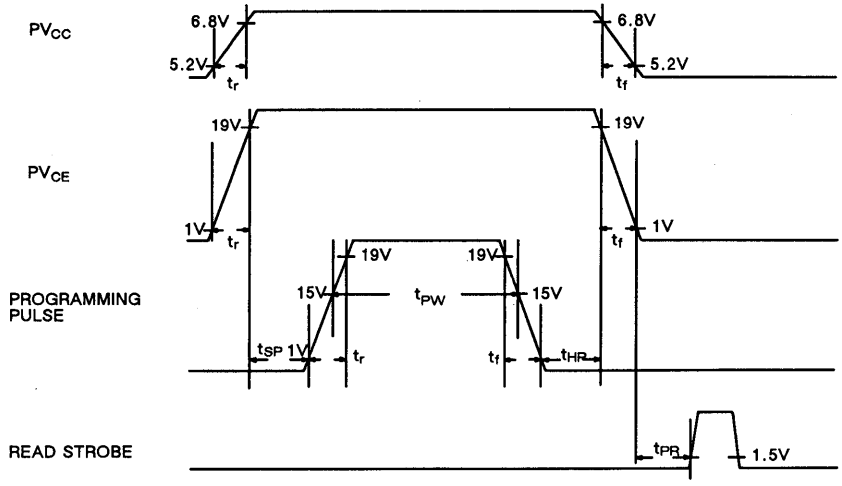
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



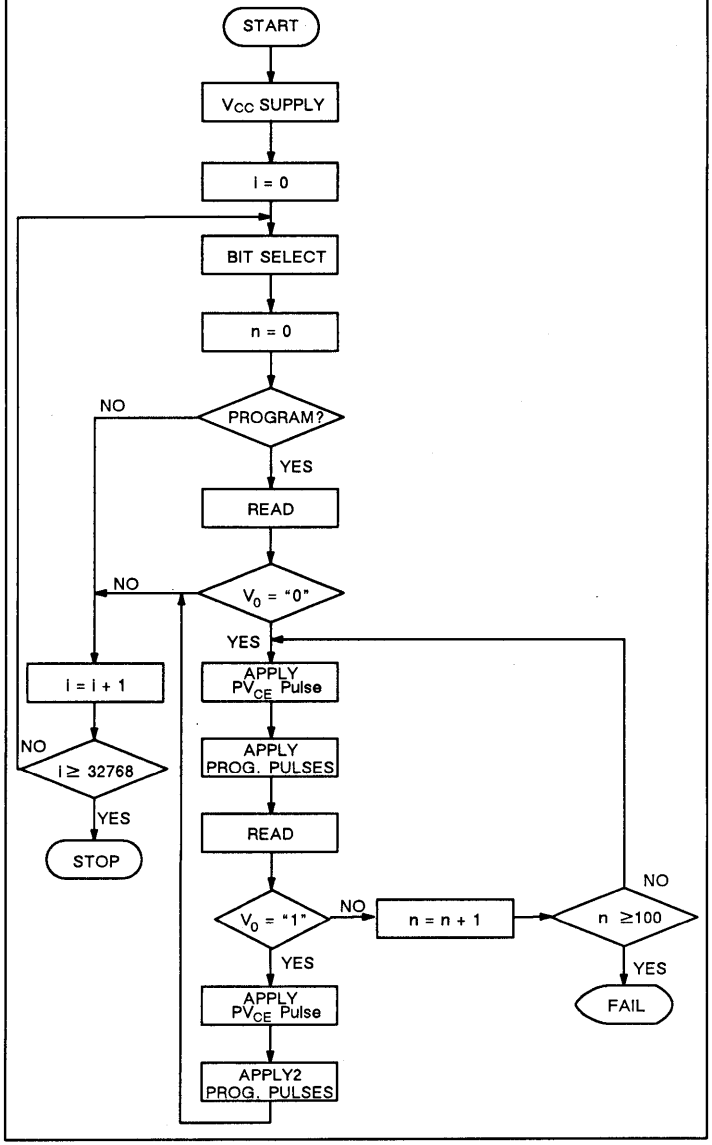
PROGRAMMING INFORMATION (continued)

PROGRAMMING PROCEDURE

1. Apply power; $V_{CC} = PV_{CC}$, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125mA and duration of t_{PW}(11μS) after a delay of t_{SP}(4μS).
6. Read the output V_O after a delay of t_{PR}(10μS).
   a) In the case of V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μS)
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA}(2μS).

Note
1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C ± 2°C)

Fig. 14 – PROGRAMMING FLOW CHART

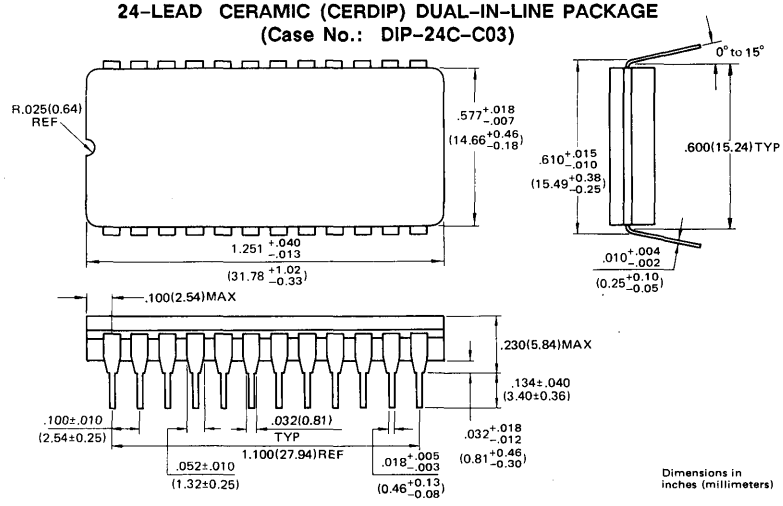


4

PACKAGE DIMENSIONS

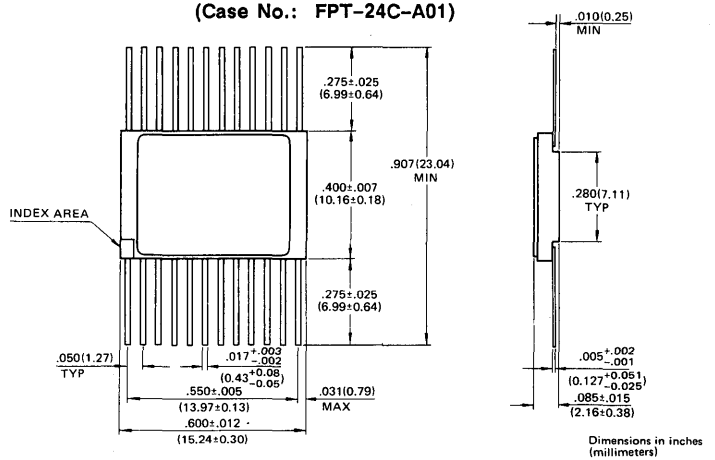
Standard 24-pin Ceramic DIP (Suffix: -Z)

24-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(Case No.: DIP-24C-C03)



Standard 24-pin Ceramic Flat Package (Suffix: -CF)

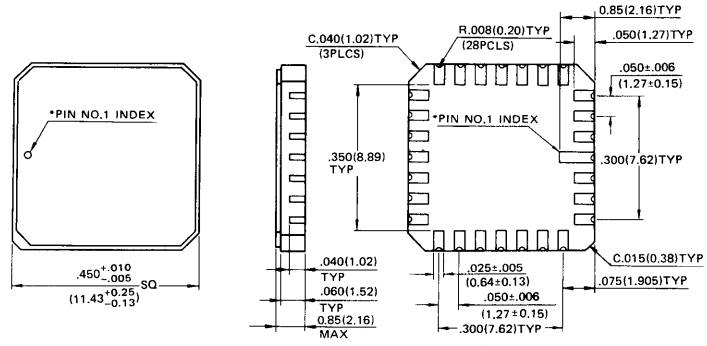
24-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(Case No.: FPT-24C-A01)



PACKAGE DIMENSIONS

Standard 28-pad Ceramic LCC (Suffix: -CV)

28-pad CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(Case No.: LCC-28C-A01)



*Shape of Pin No.1 index: Subject to change without notice

Dimensions in inches (millimeters)

4

FUJITSU

PROGRAMMABLE SCHOTTKY 65536-BIT READ ONLY MEMORY

MB7144E/H

SCHOTTKY 65,536-BIT DEAP PROM (8192 WORDS X 8 BITS)

November 1988
Edition 4.0

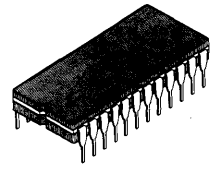
The Fujitsu MB7144 is high speed schottky TTL electrically field programmable read only memory organized as 8192 words by 8 bits. With threestate outputs, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP(Diffused Eutectic Aluminum Process) according to simple programming procedures.

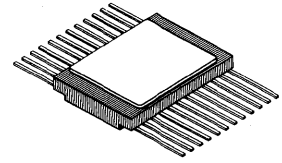
The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

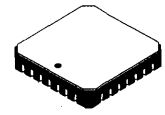
- Single +5V supply voltage.
- 8192 words x 8 bits organization , fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time, 40ns typ.
  E: 65ns max.
  H: 55ns max.
- TTL compatible inputs and outputs.
- 3-State outputs.
- One chip enable pin for simplified memory expansion.
- Standard 24-pin Ceramic DIP
- Standard 24-pin Ceramic FPT
- Standard 28-pad Ceramic LCC
- JEDEC approved pin out



CERAMIC PACKAGE
DIP-24C-C01



CERAMIC PACKAGE
FPT-24C-A02



CERAMIC PACKAGE
LCC-28C-A01

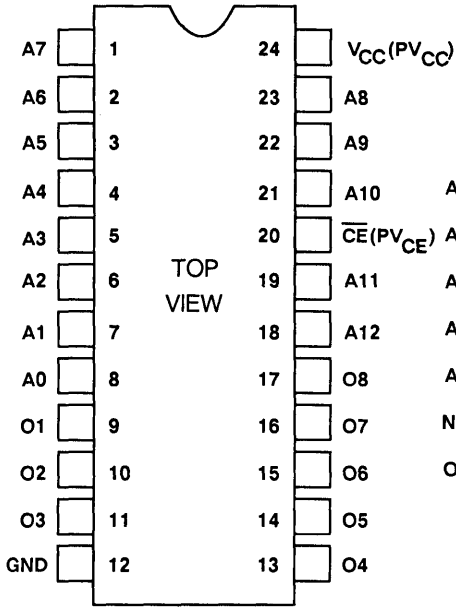
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CCP}	-0.5 to +7.5	V
Input Voltage	V_{IN}	-1.5 to 5.5	V
Input Voltage(during programming)	V_{IPRG}	22.5	V
Output Voltage(during programming)	V_{OPRG}	-0.5 to +22.5	V
Input Current	I_{IN}	-20	mA
Input Current (during programming)	I_{IPRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Output Voltage	V_{OUT}	-0.5 to 5.5	V

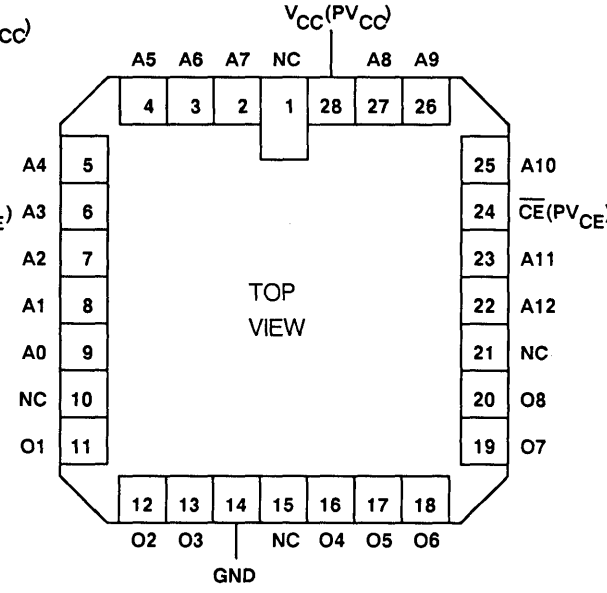
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN ASSIGNMENT



PAD CONFIGURATION

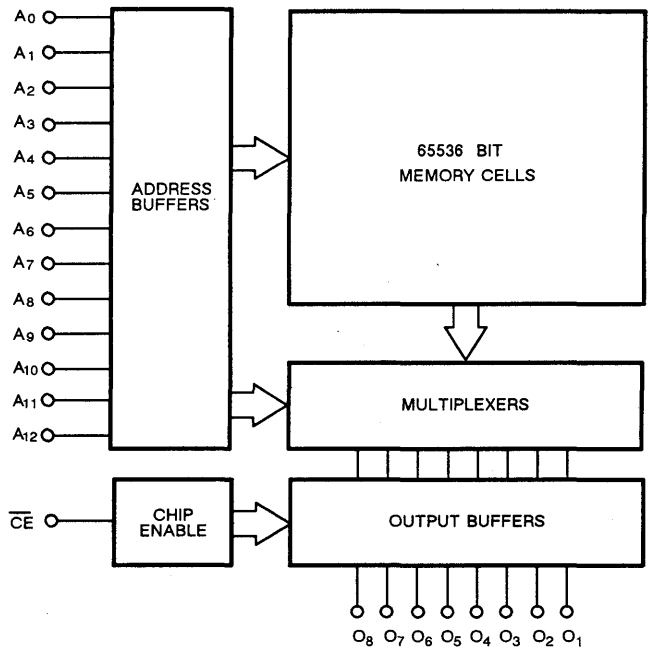


MB7144 MODE SELECTION

MODE	$\overline{CE}1$	Output $O_1 \sim O_8$
READ	V_{IL}	D_{OUT}
CHIP-DISABLE	V_{IH}	HZ
WRITE	PV_{CE}	HZ

HZ : high-impedance
D_{OUT} : memory answer
PV_{CE} : 20V (see programming information)

Fig. 1 — MB7144 BLOCK DIAGRAM



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CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25 °C)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	5.5	V
Ambient Temperature	T_A	0	-	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	µA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	µA
Output Low Voltage	I_{OL} = 10mA	V_{OL}			0.45	V
	I_{OL} = 16mA				0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)		I_{OIH}			40	µA
Output Leakage Current (V_O = 0.45V, chip disabled)		I_{OIL}			-40	µA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}		160	190	mA
Output High Voltage (I_O = -2.4mA)		V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)		I_{OS}*	-15		-60	mA

Note: * Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

** This value denote conditions at T_A=25°C and V_{CC} = +5.0V

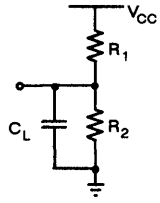


Fig. 2 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

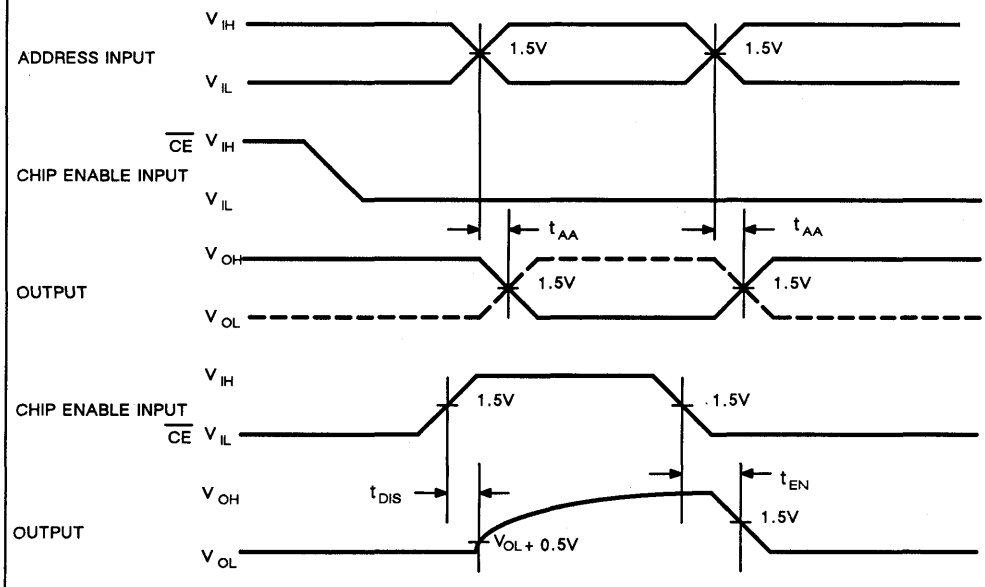
	MB7144		
	R_1	R_2	C_L
t_{AA}	300 Ω	600 Ω	30pF
t_{DIS}	300 Ω	600 Ω	30pF
t_{EN}	300 Ω	600 Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter	Symbol	E		H		Unit
		Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	40	65	40	55	ns
Output Disable Time	t_{DIS}	20	40	20	40	ns
Output Enable Time	t_{EN}	25	40	25	40	ns

OPERATION TIMING DIAGRAM



Note: Output disable time is the time taken for the output to reach a high resistance when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

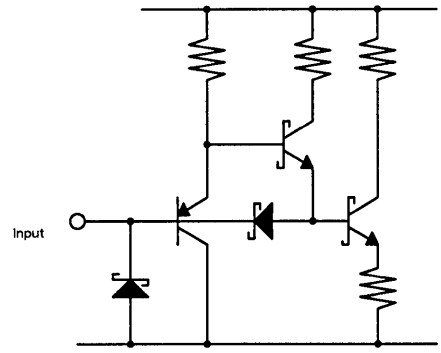
4

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Fig. 3 - MB7144 INPUT



THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 4 - MB7144 OUTPUT

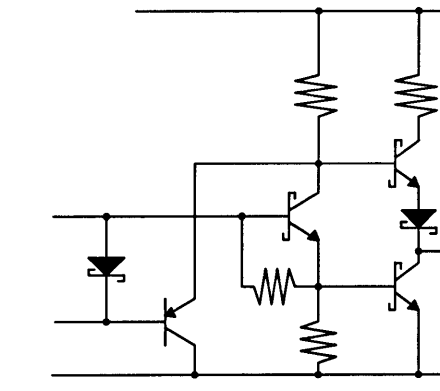


Fig.5-I_{IN} INPUT CURRENT VS. V_{IN} INPUT VOLTAGE

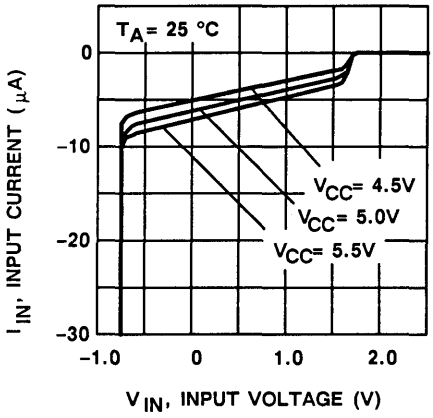


Fig.6-I_{OL} OUTPUT LOW CURRENT VS. V_{OL} OUTPUT LOW VOLTAGE

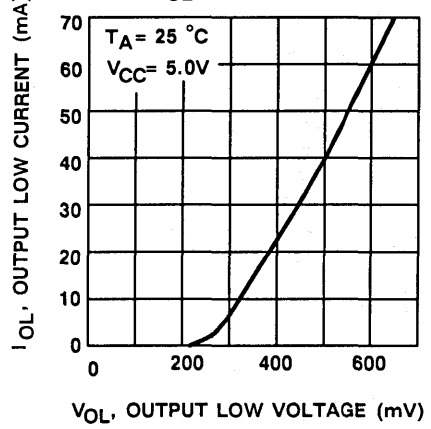


Fig.7-I_{OH} OUTPUT HIGH CURRENT VS. V_{OH} OUTPUT HIGH VOLTAGE

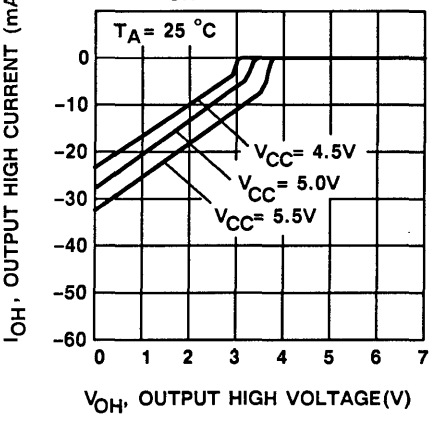


Fig.8-t_{AA} ACCESS TIME VS. AMBIENT TEMPERATURE

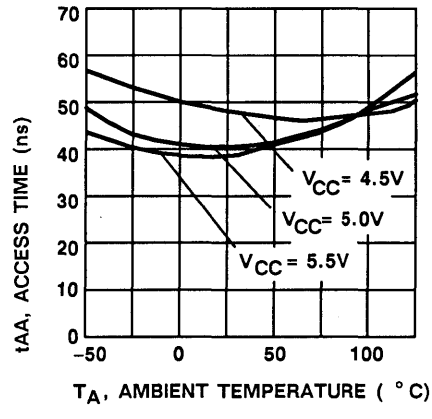


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Fig.9-t_{DIS} DISABLE TIME VS. AMBIENT TEMPERATURE

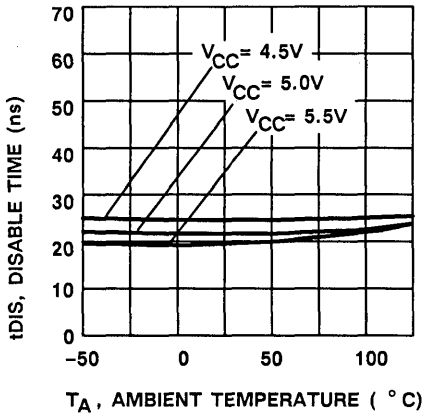

Fig.10-t_{EN} ENABLE TIME VS. AMBIENT TEMPERATURE

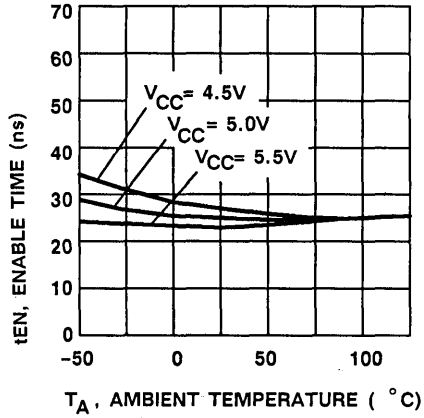

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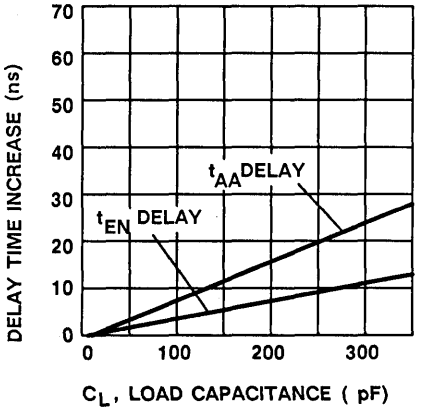
Fig.11-DELAY TIME INCREASE VS. C_L LOAD CAPACITANCE



PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB7100 series is the junction-shorting schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate(Fig. 12).

Each word line island is divided by passive isolations named IOP (Isolation by Oxide and Poly-silicon), and each memory cell in the same island is divided by the pasive isolation named SVG (Shallow V-Groove).

The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

Fig. 12 - PROGRAMMED CELL (CROSS SECTION)

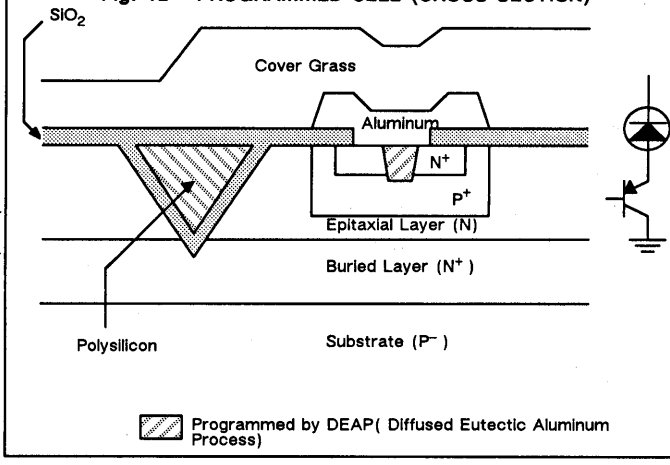
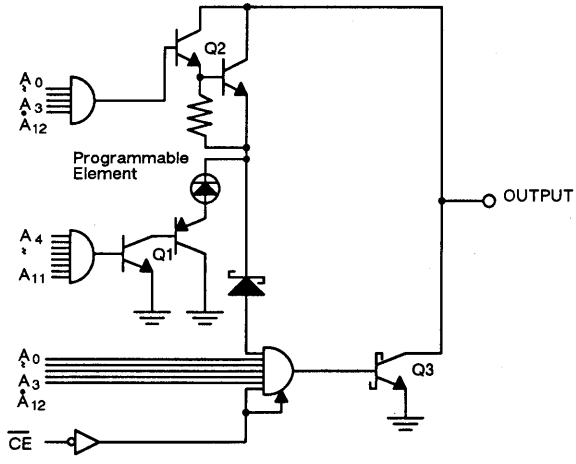


Fig. 13 - INTERNAL PROGRAMMING CIRCUIT



4

PROGRAMMING INFORMATION (continued)

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

As shown in Fig. 13, transistors, Q1 and Q2, are turned on to select the desired bit for programming by using thirteen address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q2 and memory cell into transistor Q1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified when all of chip enables are taken enable. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{CC}= 2.4V and V$_{OH}$ = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH}		2.0		5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	V
Programming Pulse Current	I_{PRG}		120		130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS (T_A = 25°C)

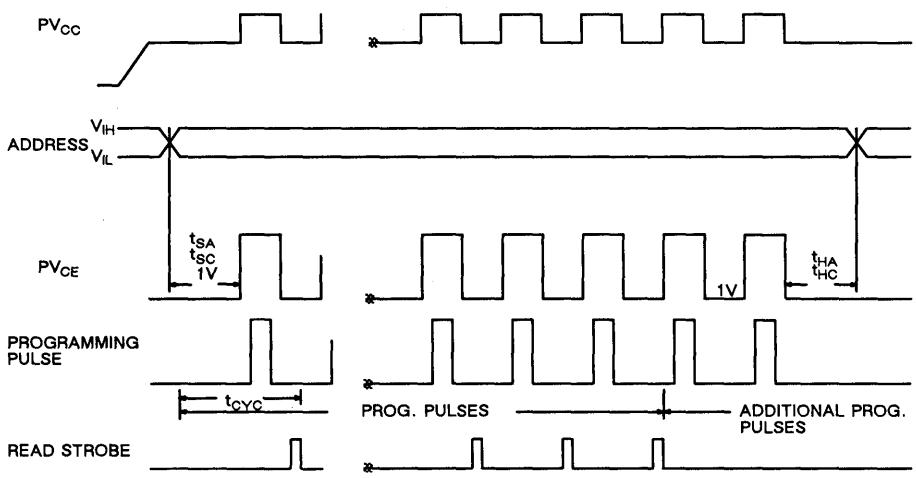
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	µs
Programming Pulse Width	t_{PW} (1)	10	11	12	µs
Programming Pulse Rise Time	t_r (2)	–	–	2	µs
PV_{CE} Pulse Rise Time	t_r (3)	–	–	2	µs
PV_{CC} Pulse Rise Time	t_r (4)	–	–	2	µs
Programming Pulse Fall Time	t_f (5)	–	–	2	µs
PV_{CE} Pulse Fall Time	t_f (6)	–	–	2	µs
PV_{CC} Pulse Fall Time	t_f (7)	–	–	2	µs
Address Input Set-up Time	t_{SA}	2	–	–	µs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	µs
PV_{CE} Set-up Time	t_{SP} (8)	4	–	–	µs
Address Input Hold Time	t_{HA}	2	–	–	µs
Chip Enable Input Hold Time	t_{HC}	2	–	–	µs
PV_{CE} Hold Time	t_{HP} (9)	2	–	–	µs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (10)	10	–	–	µs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	µs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Note: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 1V to 19V.
(4) From 5.2V to 6.8V.
(5) From 19V to 1V (200Ω load).
(6) From 19V to 1V.
(7) From 6.8V to 5.2V.
(8) From PV_{CE} pulse 19V to programming pulse 1V.
(9) From programming pulse 1V to PV_{CE} pulse 19V.
(10) From PV_{CE} pulse 1V to read strobe.

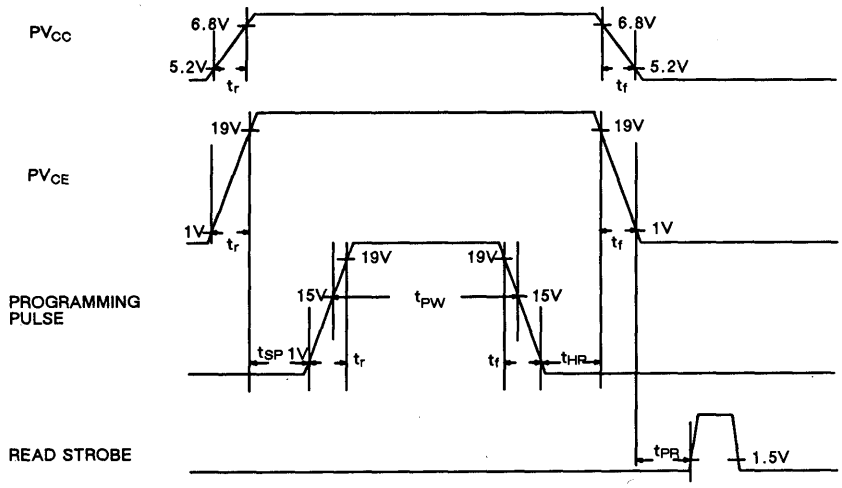
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



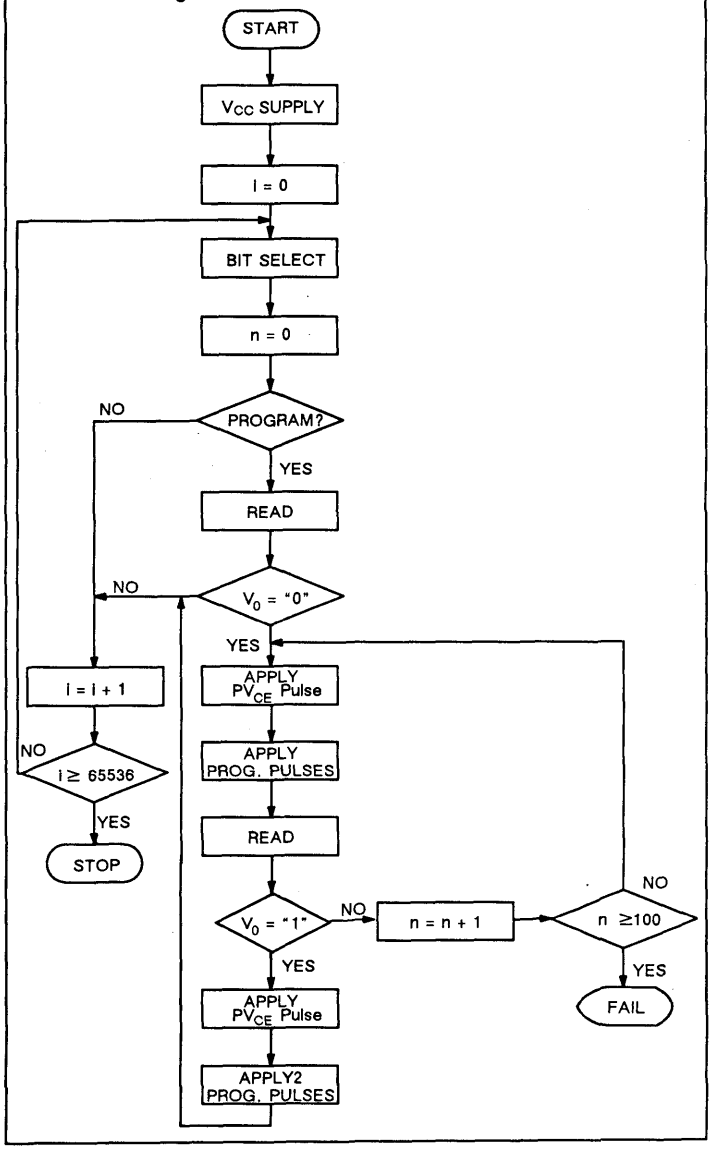
PROGRAMMING INFORMATION (continued)

PROGRAMMING PROCEDURE

1. Apply power; V_{CC} = PV_{CC}, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125mA and duration of t_{PW}(11μS) after a delay of t_{SP}(4μS).
6. Read the output V_O after a delay of t_{PR}(10μS).
   a) In the case of V_O = low, repeat steps "4","5" and "6" with cycle time of t_{CYC} (50μS)
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA}(2μS).

Note
1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C ± 2°C)

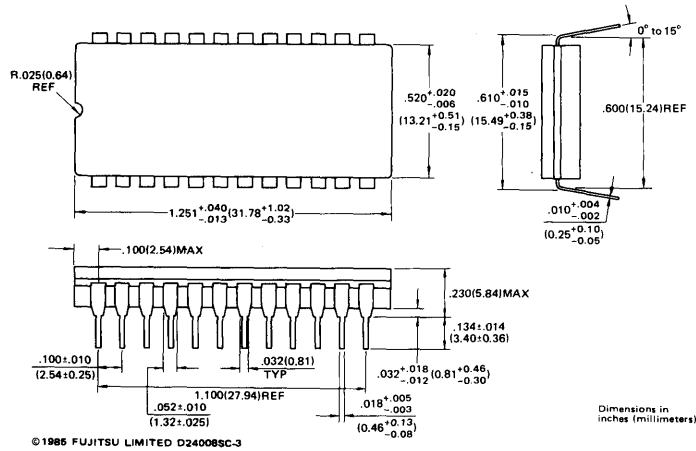
Fig. 14 - PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

Standard 24-pin Ceramic DIP (Suffix: -Z)

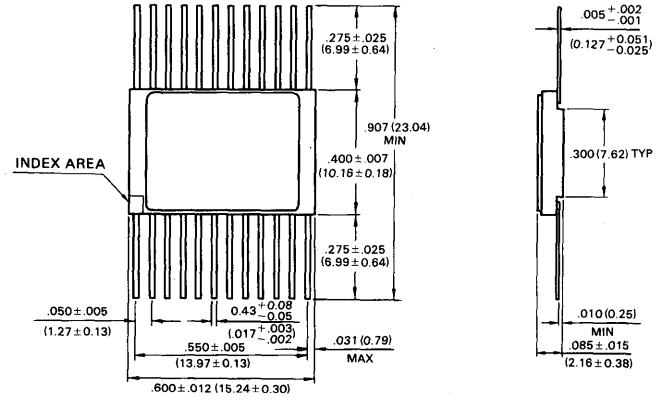
24-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(Case No.: DIP-24C-C01)



Dimensions in inches (millimeters)

Standard 24-pin Ceramic Flat Package (Suffix: -CF)

24-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(Case No.: FPT-24C-A02)

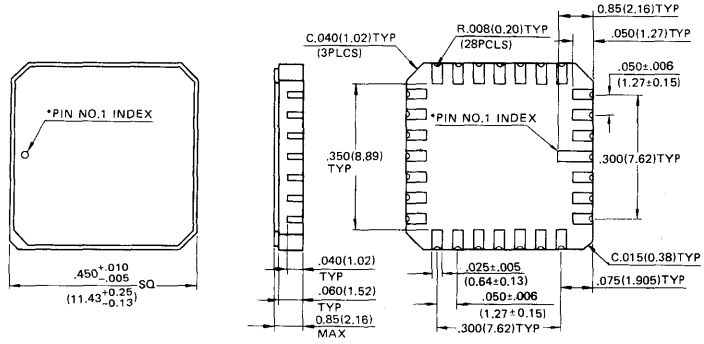


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS

Standard 28-pad Ceramic LCC (Suffix: -CV)

28-pad CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(Case No.: LCC-28C-A01)



*Shape of Pin No.1 index: Subject to change without notice

Dimensions in inches (millimeters)

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FUJITSU

PROGRAMMABLE SCHOTTKY 16384-BIT READ ONLY MEMORY

MB 7151E/H
MB 7152E/H/Y

February 1983
Edition 1.0

SCHOTTKY 16384-BIT DEAP PROM (4096 WORDS X 4 BITS)

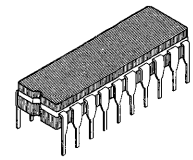
The Fujitsu MB 7151 and MB 7152 are high speed schottky TTL electrically field programmable read only memorys organized as 4096 words by 4 bits. With uncommitted collector output provided on the MB 7151 and three-state outputs on the MB 7152, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic Level "ones" can be programmed by the highly reliable Deap (Diffused Eutectic Aluminum Process) according to simple programming procedures.

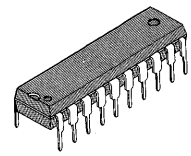
The sophisticated passive isolation termed IOP (Isolation by Oxide and Poly-silicon) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

- Single +5V supply voltage.
- 4096 words x 4 bits organization, fully decoded.
- Proven high programmability and reliability.
- Programming by Deap (diffused eutectic aluminum process).
- Simplified and lower power programming.
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time, 35ns type
  MB 7152Y: 35ns max.
  H : 45ns max.
  E : 55ns max.
- TTL compatible inputs and outputs.
- Open collector output (MB 7151)
- 3-state outputs (MB 7152)
- Two chip enable leads for simplified memory expansion.
- 300 mil 20-pin DIP package.

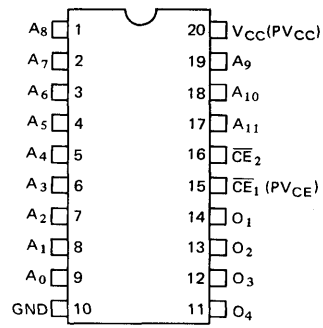


CERAMIC PACKAGE
DIP-20C-C03



PLASTIC PACKAGE
DIP-20P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input Voltage	V_{IN}	−1.5 to 5.5	V
Input Voltage (during programming)	V_{PRG}	22.5	V
Output Voltage (during programming)	V_{PRG}	−0.5 to +22.5	V
Input Current	I_{IN}	−20	mA
Input Current (during programming)	I_{PRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{PRG}	+150	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Output Voltage	V_{OUT}	−0.5 to V_{CC}	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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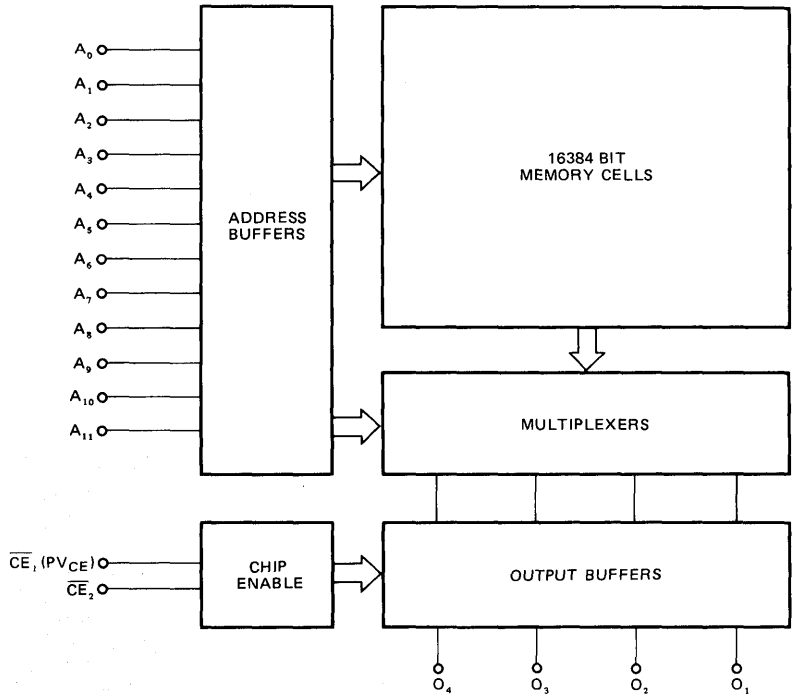
Fig. 1 – MB 7151/MB 7152 BLOCK DIAGRAM



CAPACITANCE (f=1MHz, V_{CC}=+5V, V_{IN}=+2V, T_A=25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I	–	–	10	pF
Output Capacitance	C_O	–	–	15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	5.5V	V
Ambient Temperature	T_A	0	–	75	°C

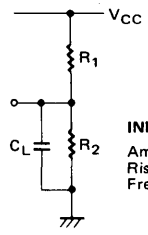
DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH}=4.5V)		I_{R1}			40	μA
Input Leakage Current (V_{IH}=5.5V)		I_{R2}			1.0	mA
Input Load Current (V_{IL}=0.45V)		I_F			-250	μA
Output Low Voltage (I_{OL}=16mA)		V_{OL}			0.50	V
Output Leakage Current (V_O=2.4V, chip disabled)	MB 7151	I_{OLK}			40	μA
	MB 7152	I_{OIH}			40	μA
Output Leakage Current (V_O=0.45V, chip disabled)	MB 7152	I_{OIL}			-40	μA
Input Clamp Voltage (I_{IN}=-18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN}=OPEN or GND)		I_{CC}		120	170	mA
Output High Voltage (I_O=-2.4mA)	MB 7152	V_{OH}*	2.4			V
Output Short Circuit Current (V_O=GND)	MB 7152	I_{OS}*	-15		-60	mA

***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{I\overline{CE}}$=0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

Fig. 2 – AC TEST CONDITIONS



INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

	MB 7151/MB 7152		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	E		H		MB 7152Y		Unit
		Type	Max	Typ	Max.	Typ	Max	
Access Time (via address input)	t_{AA}	35	55	35	45	28	35	ns
Output Disable Time	t_{DIS}		40		40		30	ns
Output Enable Time	t_{EN}		40		40		30	ns

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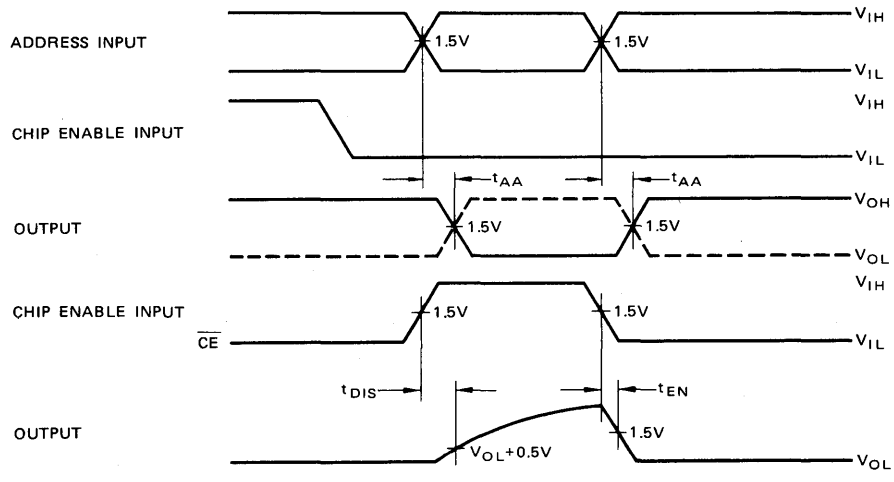
OPERATION TIMING DIAGRAM



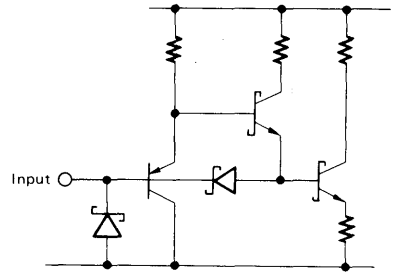
Note: Output disable time is the time taken for the output to reach a high resistance state when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Shottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

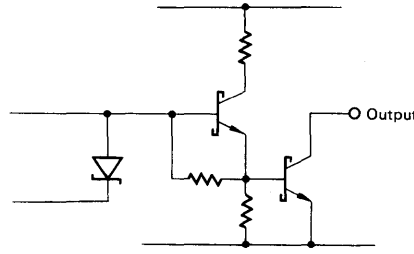
Fig. 3 – MB 7151/MB 7152 INPUT



OPEN-COLLECTOR OUTPUT

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB 7152 (3-state) compared to 0mA for the MB 7151 (open-collector)

Fig. 4 – MB 7151 OUTPUT



THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low

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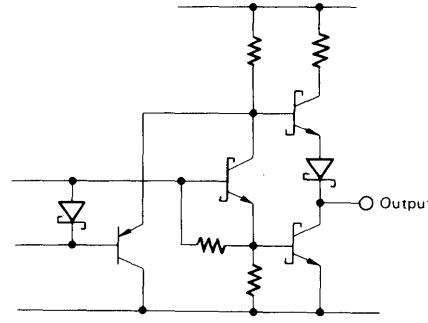
impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 5 – MB 7152 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig. 6 – I_{IN} INPUT CURRENT vs V_{IN} INPUT VOLTAGE

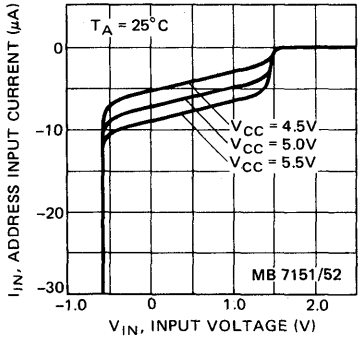


Fig. 7 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

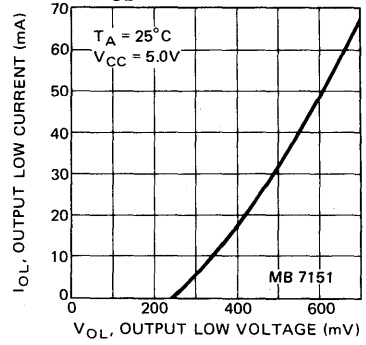


Fig. 8 – I_{OL} OUTPUT LOW CURRENT vs V_{OL} OUTPUT LOW VOLTAGE

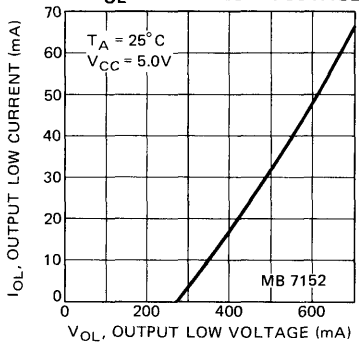
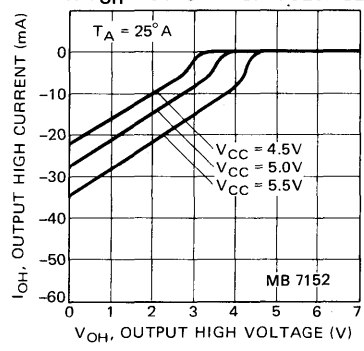


Fig. 9 – I_{OH} OUTPUT HIGH CURRENT vs V_{OH} OUTPUT HIGH VOLTAGE



MB 7153 MB 7152

Fig. 10 – t_{AA}, ACCESS TIME vs AMBIENT TEMPERATURE

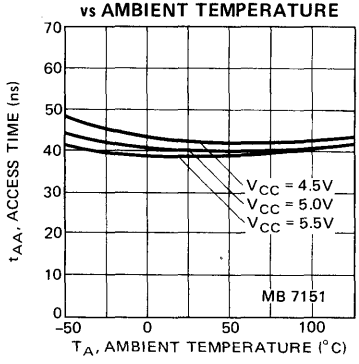


Fig. 11 – t_{AA} ACCESS TIME vs AMBIENT TEMPERATURE

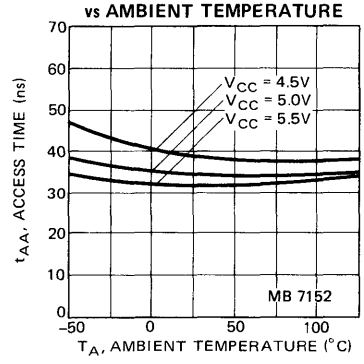


Fig. 12 – t_{DIS}, ACCESS TIME vs AMBIENT TEMPERATURE

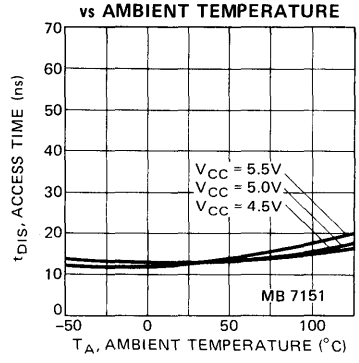


Fig. 13 – t_{DIS}, ACCESS TIME vs AMBIENT TEMPERATURE

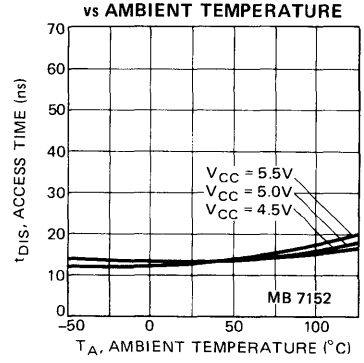


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Fig. 14 – t_{EN}, ACCESS TIME vs AMBIENT TEMPERATURE

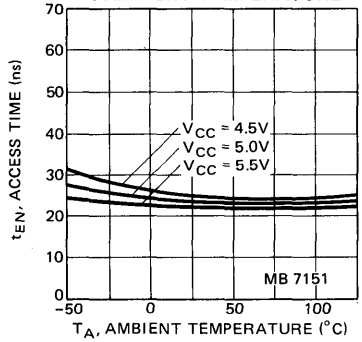


Fig. 15 – t_{EN}, ACCESS TIME vs AMBIENT TEMPERATURE

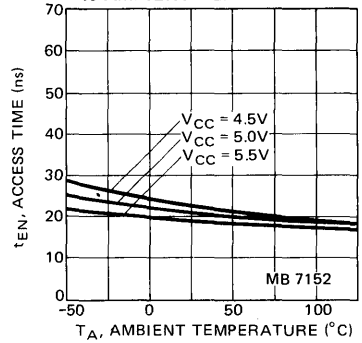


Fig. 16 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE

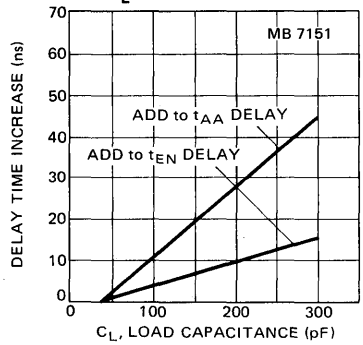
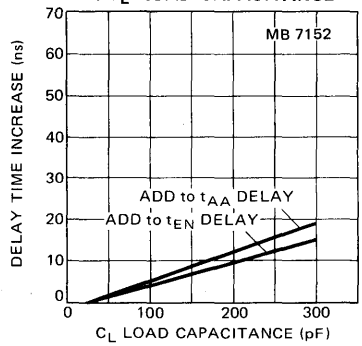


Fig. 17 – DELAY TIME INCREASE vs C_L LOAD CAPACITANCE



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PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB 7100 series Schottky PROM is fabricated using Schottky TTL technology, passive isolation technology known as Isolation by Oxide and Poly-silicon (IOP), which is achieved by thin-epitaxial and Shallow V-Grooving (SVG), Diffused Eutectic Aluminum Process (Deap) technology with fine emitter and pulse programming method which achieve high-speed operation, high-speed programming, high programmability and high reliability.

One memory cell is originally structured with a base-open NPN transistor and then programmed by shorting the base-emitter junction, i.e. shorted junction type cell which is achieved by eutectically melting aluminum and silicon adjacent to the P-N junction of cell diode with relatively low temperature, i.e. Deap technology.

Fast programming time of typically 150μs/bit is achieved with a fine emitter cell which requires less programming energy; the result is negligible thermal stress. This high reliability feature virtually eliminates aluminum migration in the programmed cell. Further, Fujitsu advanced technology allows very high programmability.

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

Fig. 13 – PROGRAMMED CELL (CROSS SECTION)

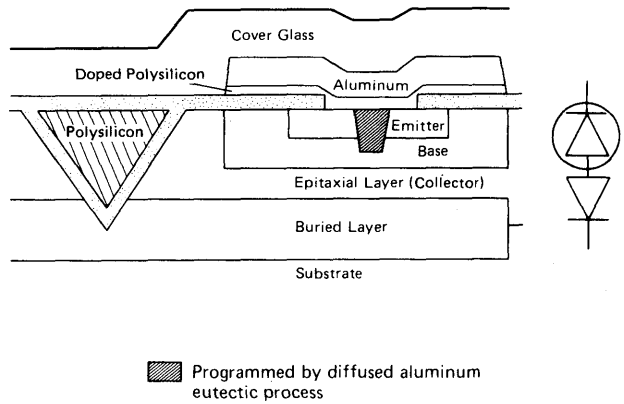
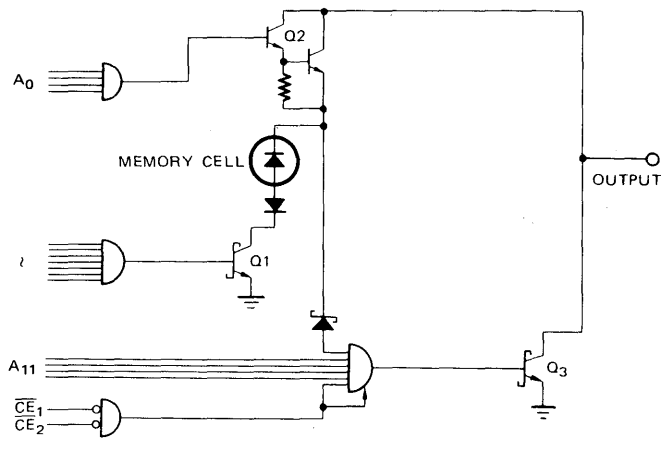


Fig. 14 – INTERNAL PROGRAMMING CIRCUIT



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PROGRAMMING INFORMATION (continued)

PROGRAMMING

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using eleven address inputs to turn on transistors Q1 and Q2. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transistor Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the output voltage indicates that the selected bit is in the logic one state.

To assure that the element is programmed properly, two additional programming pulses are applied immediately after an output voltage indicates conduction in the programmed bit.

One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified when all chip enables are taken enable. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH} = 2.4V and V_{CC} = 7V at 25°C ambient temperature.

RELIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

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DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0	–	0.8	V
Input HIgh Voltage	V_{IH}		2.0	–	5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming Pulse Current	I_{PRG}		120	–	130	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230	–	260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

AC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	μs
Programming Pulse Width	t_{PW}(1)	10	11	12	μs
Programming Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CE} Pulse Rise Time	t_r(2)	–	–	2	μs
PV_{CC} Pulse Rise Time	t_r(3)	–	–	2	μs
Programming Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CE} Pulse Fall Time	t_f(4)	–	–	2	μs
PV_{CC} Pulse Fall Time	t_f(5)	–	–	2	μs
Address Input Set-up Time	t_{SA}	2	–	–	μs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	μs
PV_{CE} Set-up Time	t_{SP}(6)	4	–	–	μs
Address Input Hold Time	t_{HA}	2	–	–	μs
Chip Enable Input Hold Time	t_{HC}	2	–	–	μs
PV_{CE} Hold Time	t_{HP}(7)	2	–	–	μs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR}(8)	10	–	–	μs
Programming Pulse Number	n	–	–	100	Times
Programming Time/Bit	–	120	150	6120	μs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Notes: (1) Stipulated 200Ω load and 15V.
(2) From 1V to 19V (200Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (200Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

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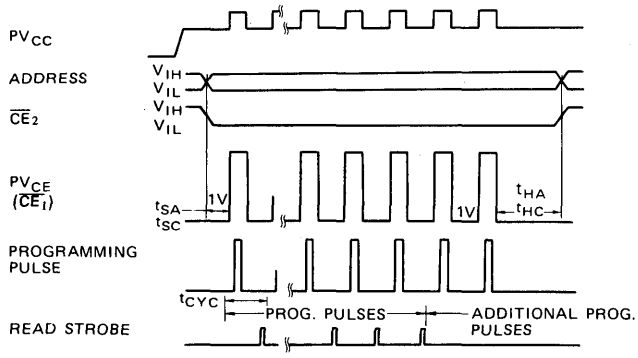
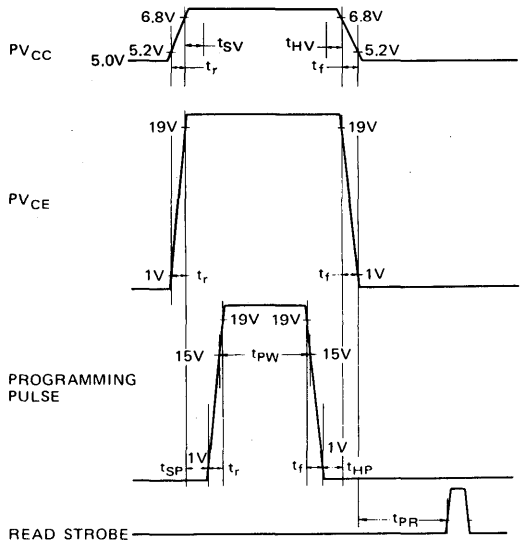
PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE

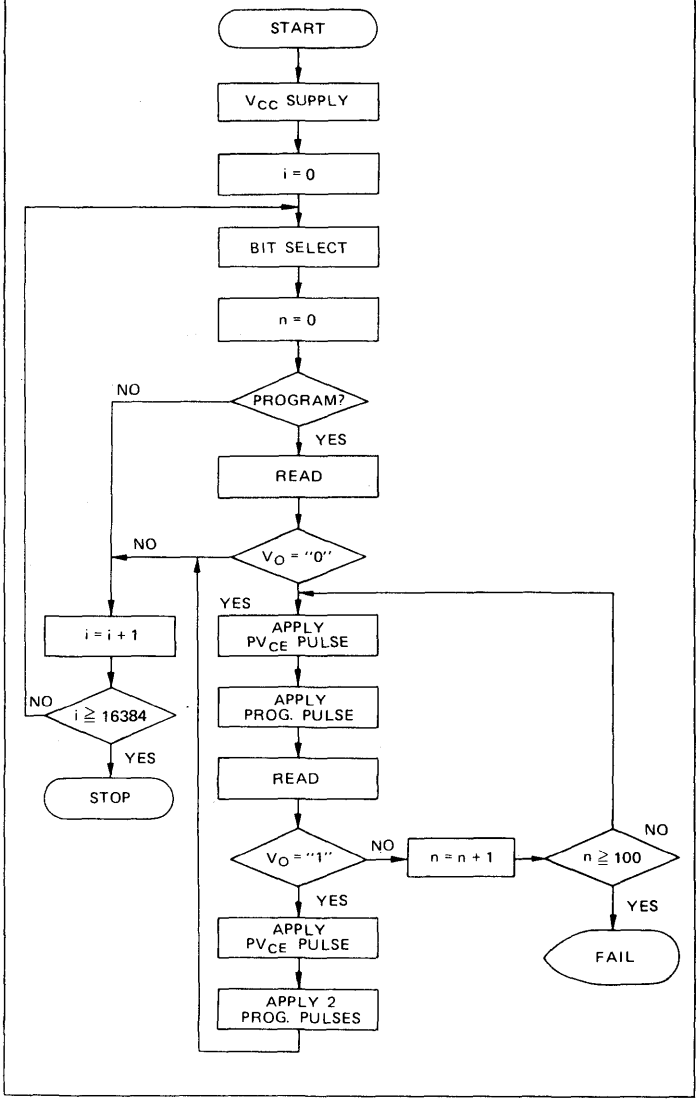


PROGRAMMING PROCEDURE

1. Apply power; $V_{CC}=PV_{CC}$, GND= 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O=low. (In the case of V_O=high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125 mA and duration of t_{PW} (11μs) after a delay of t_{SP} (4μs).
6. Read the output V_O after a delay of t_{PR} (10μs).
   a) In the case of V_O=low, repeat steps "4", "5" and "6" with cycle time of t_{CYC}(50μs).
   b) In the case of V_O=high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA}(2μs).

Note 1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C±2°C)

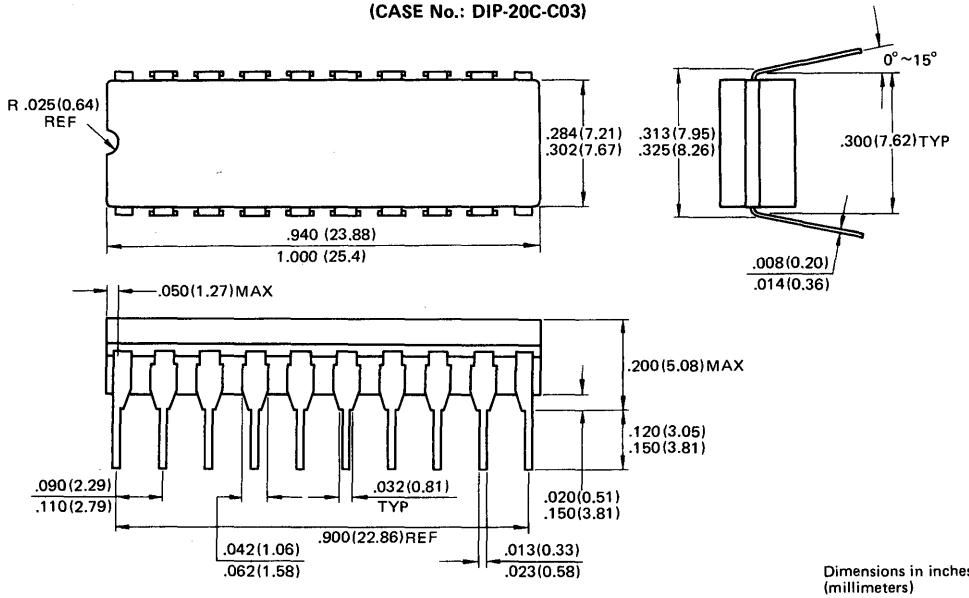
Fig. 4 – PROGRAMMING FLOW CHART



4

PACKAGE DIMENSIONS

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)

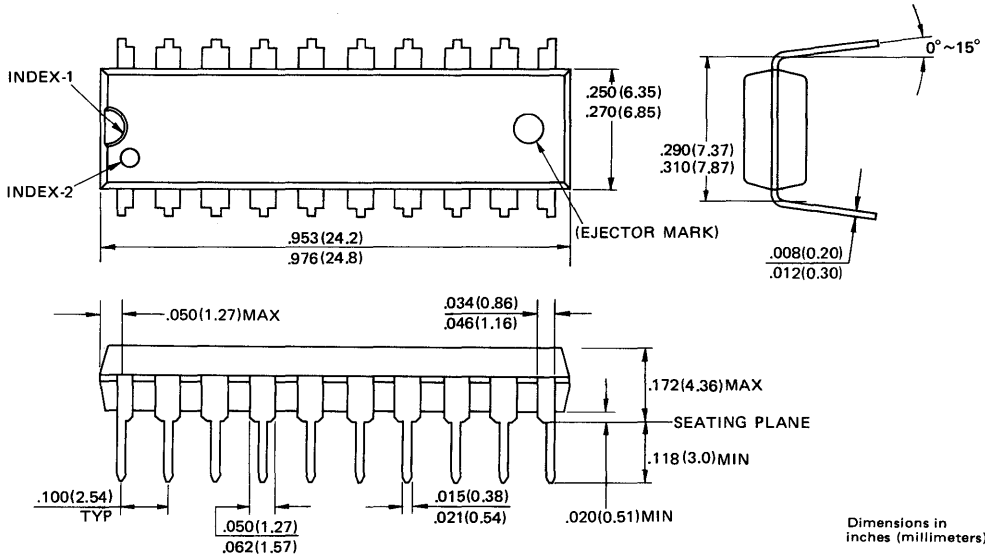


Dimensions in inches
(millimeters)

4

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



4

FUJITSU

PROGRAMMABLE SCHOTTKY 16384-BIT READ ONLY MEMORY

MB71A38-25 MB71A38-35

August 1988
Edition 2.0

SCHOTTKY 16384-BIT DEAP PROM (2048 WORDS X 8 BITS)

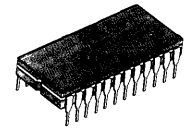
The Fujitsu MB71A38 is high speed schottky TTL electrically field programmable read only memory organized as 2048 words by 8 bits. With threestate outputs, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP(Diffused Eutectic Aluminum Process) according to simple programming procedures.

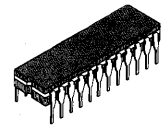
The sophisticated passive isolation termed U-FOX (U-groove isolation with thick Field OXide process) with thin epitaxial layer and schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

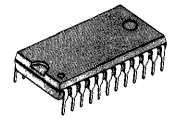
- Single +5V supply voltage.
- 2048 words x 8 bits organization , fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time 18ns typ, 25/35 ns max
- TTL compatible inputs and outputs.
- 3 State outputs.
- Three chip enable pins for simplified memory expansion.
- 24-pin Ceramic (Cerdip) DIP(300 &600 mil)
- 24-pin Plastic DIP (300 & 600mil)



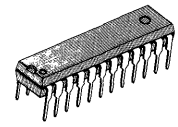
CERAMIC PACKAGE
DIP-24C-C01



CERAMIC PACKAGE
DIP-24C-C04(-SK)



PLASTIC PACKAGE
DIP-24P-M02



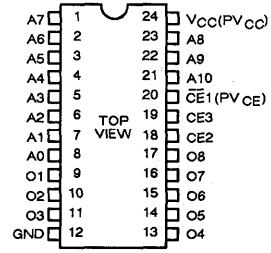
PLASTIC PACKAGE
DIP-24P-M03(-SK)

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	0.5 to + 7.0	V
Power Supply Voltage (during programming)		V_{CCP}	-0.5 to +7.5	V
Input Voltage		V_{IN}	-1.5 to 5.5	V
Input Voltage(during programming)		V_{IPRG}	22.5	V
Output Voltage(during programming)		V_{OPRG}	-0.5 to +22.5	V
Input Current		I_{IN}	-20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+75	mA
Storage Temperature	CERAMIC	T_{stg}	-65 to +150	°C
	PLASTIC		-40 to +125	
Output Voltage		V_{OUT}	-0.5 to 5.5	V

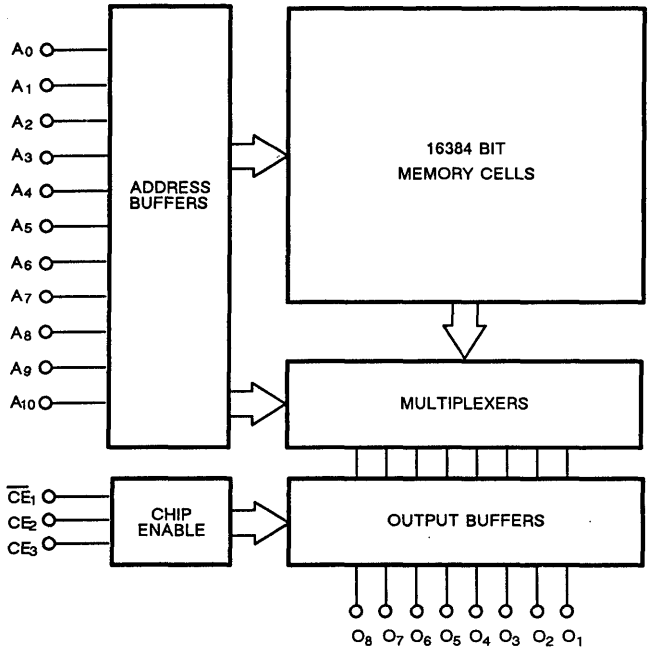
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB71A38 BLOCK DIAGRAM



4

CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25 °C)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	5.5	V
Ambient Temperature	T_A	0	-	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	µA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	µA
Output Low Voltage	I_{OL} = 10mA	V_{OL}			0.45	V
	I_{OL} = 16mA				0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)		I_{OIH}			40	µA
Output Leakage Current (V_O = 0.45V, chip disabled)		I_{OIL}			-40	µA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}		80**	120	mA
Output High Voltage (I_O = -2.4mA)		V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)		I_{OS}*	-15		-60	mA

Note: * Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

** This value denote conditions at T_A=25°C and V_{CC} = +5.0V

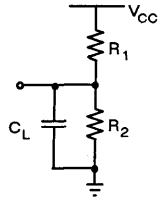


Fig. 2 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

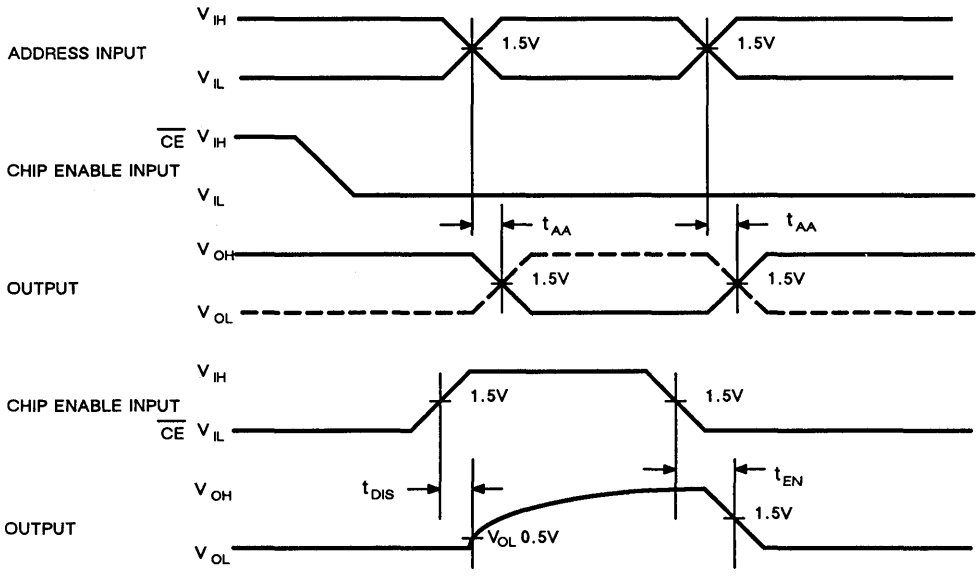
	MB71A38		
	R_1	R_2	C_L
t_{AA}	300 Ω	600 Ω	30pF
t_{DIS}	300 Ω	600 Ω	30pF
t_{EN}	300 Ω	600 Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter	Symbol	MB71A38-25		MB71A38-35		Unit
		Typ	Max	Typ	Max	
Address Time (via address input)	t_{AA}	18	25	18	35	ns
Output Disable Time	t_{DIS}	10	20	10	25	ns
Output Enable Time	t_{EN}	12	20	12	25	ns

OPERATION TIMING DIAGRAM



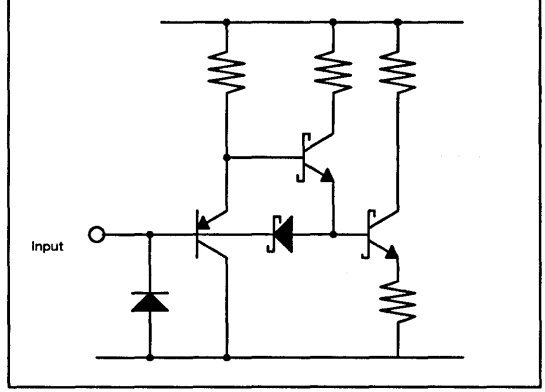
Note: Output disable time is the time taken for the output to reach a high resistance when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Fig. 3 - MB71A38 INPUT



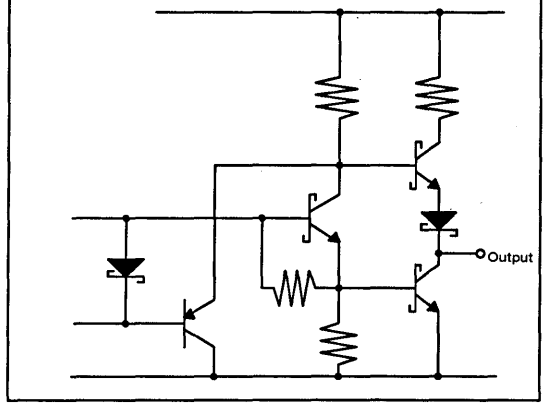
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 4 - MB71A38 OUTPUT



4

TYPICAL CHARACTERISTICS CURVES

Fig.5-I_{IN} INPUT CURRENT VS. V_{IN} INPUT VOLTAGE

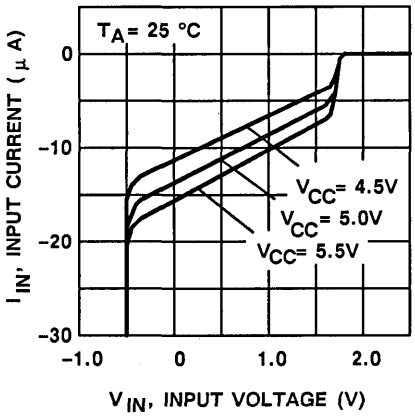


Fig.6-I_{OL} OUTPUT LOW CURRENT VS. V_{OL} OUTPUT LOW VOLTAGE

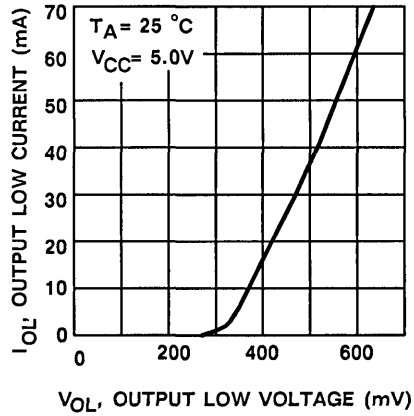


Fig.7-I_{OH} OUTPUT HIGH CURRENT VS. V_{OH} OUTPUT HIGH VOLTAGE

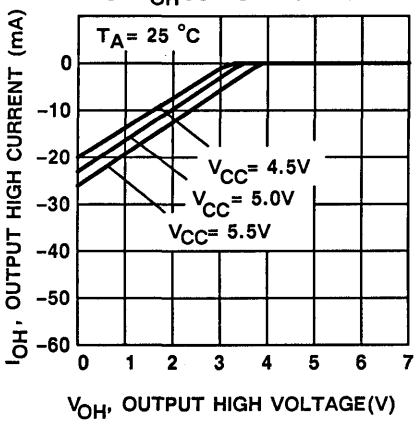
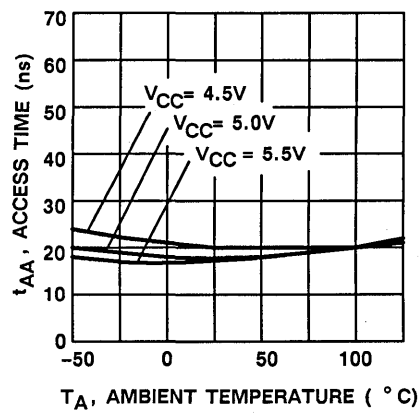


Fig.8-t_{AA} ACCESS TIME VS. AMBIENT TEMERATUERE



4

TYPICAL CHARACTERISTICS CURVES

Fig.9-t_{DIS} DISABLE TIME VS. AMBIENT TEMPERATURE

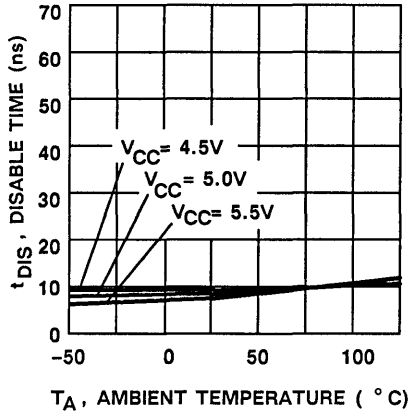


Fig.10-t_{EN} ENABLE TIME VS. AMBIENT TEMPERATURE

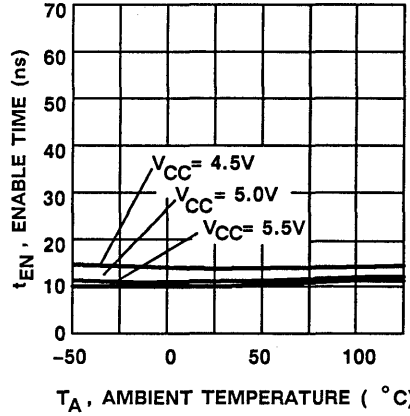
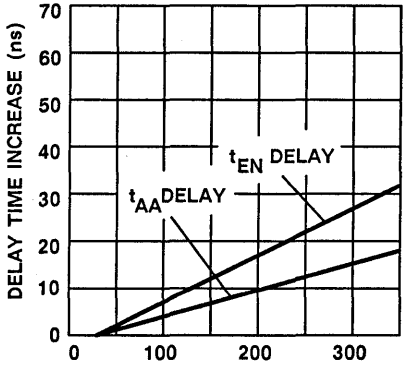


Fig.11-DELAY TIME INCREASE VS. C_L LOAD CAPACITANCE



4

PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB71A00 series is the junction-shorting schottky PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor. The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate(Fig. 12).

Each memory cell is divided by passive isolations named U-FOX (U-groove isolation with thick Field OXide process).

The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process"(DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

Fig.12 - PROGRAMMED CELL (CROSS SECTION)

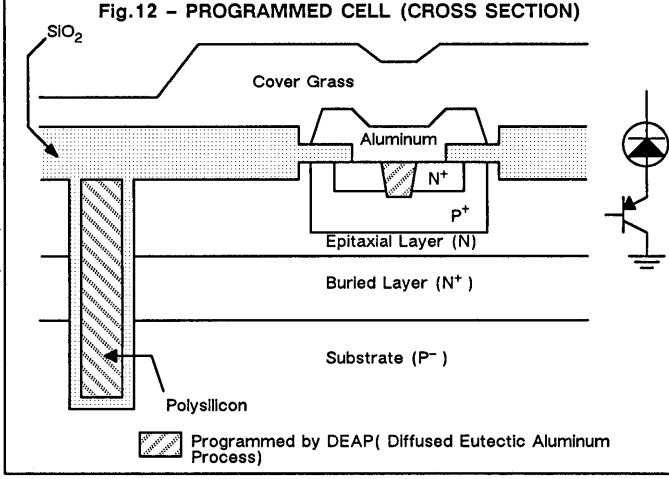
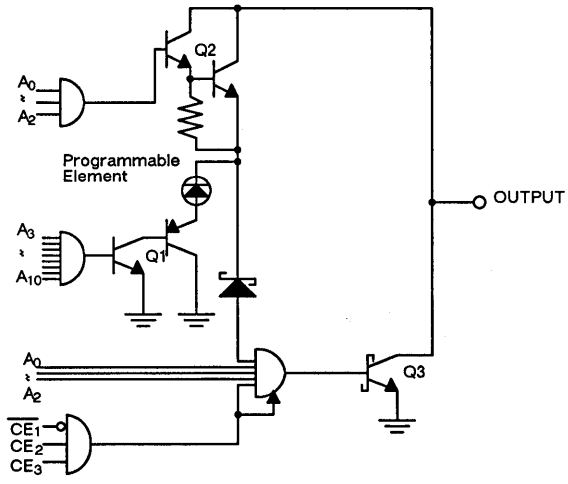


Fig. 13 - INTERNAL PROGRAMMING CIRCUIT



PROGRAMMING INFORMATION (continued)

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

As shown in Fig. 13, transistors, Q1 and Q2, are turned on to select the desired bit for programming by using eleven address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q2 and memory cell into transistor Q1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH}= 2.4V and V_{CC}= 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (TA = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH}		2.0		5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	V
Programming Pulse Current	I_{PRG}		70		75	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS (TA = 25°C)

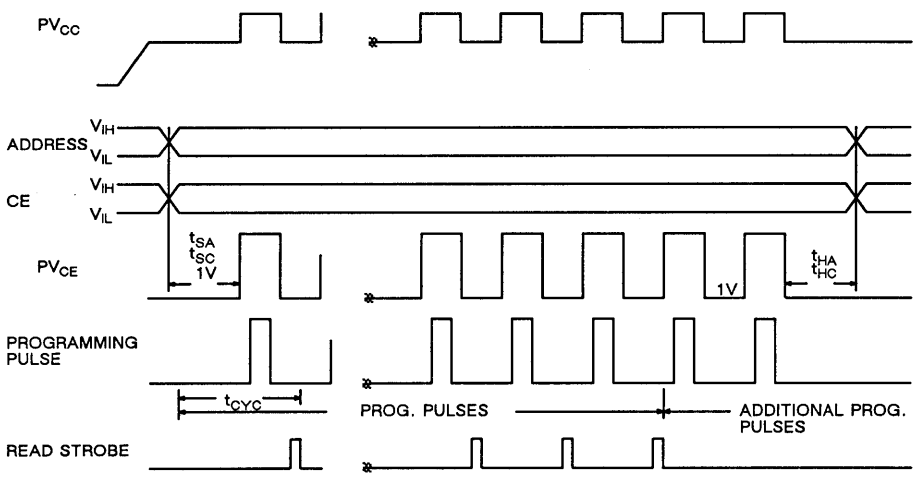
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	µs
Programming Pulse Width	t_{PW} (1)	10	11	12	µs
Programming Pulse Rise Time	t_r (2)	–	–	2	µs
PV_{CE} Pulse Rise Time	t_r (2)	–	–	2	µs
PV_{CC} Pulse Rise Time	t_r (3)	–	–	2	µs
Programming Pulse Fall Time	t_f (4)	–	–	2	µs
PV_{CE} Pulse Fall Time	t_f (4)	–	–	2	µs
PV_{CC} Pulse Fall Time	t_f (5)	–	–	2	µs
Address Input Set-up Time	t_{SA}	2	–	–	µs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	µs
PV_{CE} Set-up Time	t_{SP} (6)	4	–	–	µs
Address Input Hold Time	t_{HA}	2	–	–	µs
Chip Enable Input Hold Time	t_{HC}	2	–	–	µs
PV_{CE} Hold Time	t_{HP} (7)	2	–	–	µs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (8)	10	–	–	µs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	µs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Note: (1) Stipulated 400Ω load and 15V.
(2) From 1V to 19V (400Ω load).
(3) From 5.2V to 6.8V (30Ω load).
(4) From 19V to 1V (400Ω load).
(5) From 6.8V to 5.2V (30Ω load).
(6) From PV_{CE} pulse 19V to programming pulse 1V.
(7) From programming pulse 1V to PV_{CE} pulse 19V.
(8) From PV_{CE} pulse 1V to read strobe.

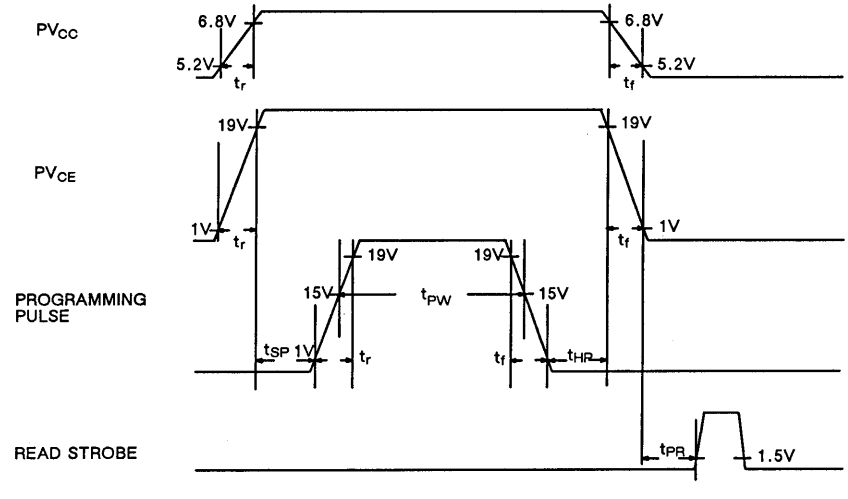
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



4

PROGRAMMING INFORMATION (continued)

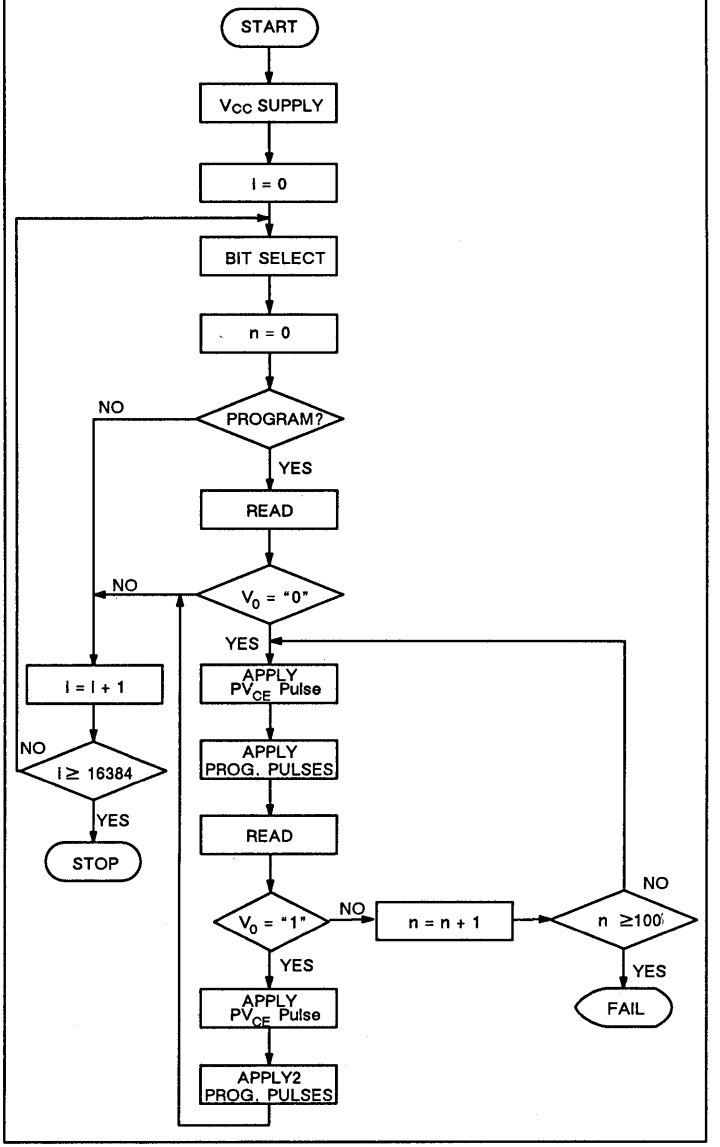
PROGRAMMING PROCEDURE

1. Apply power; $V_{CC} = PV_{CC}$, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 62.5mA and duration of t_{PW} (11μS) after a delay of t_{SP} (4μS).
6. Read the output V_O after a delay of t_{PR} (10μS).
   a) In the case of V_O = low, repeat steps "4","5" and "6" with cycle time of t_{CYC} (50μS)
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μS).

Note

1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C ±2°C)

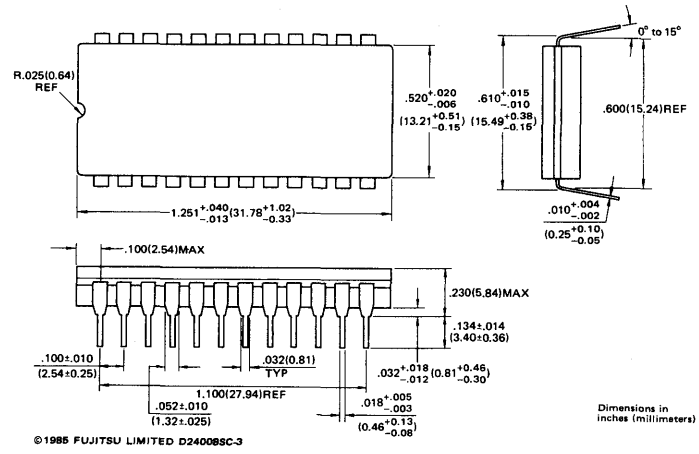
Fig. 14 – PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

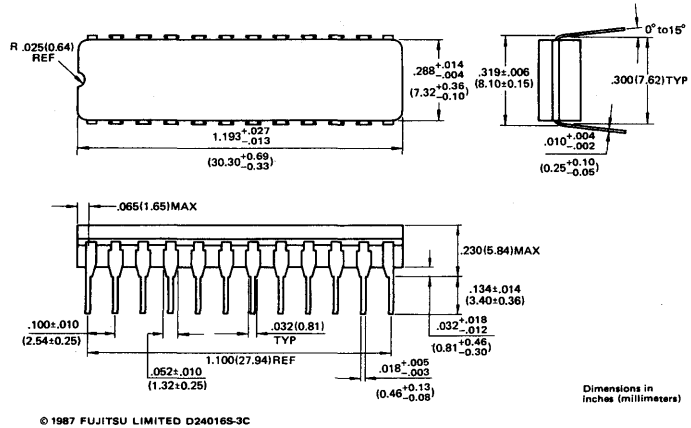
Standard 24-pin Ceramic DIP (Suffix: -Z)

24-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(Case No.: DIP-24C-C01)



Standard 24-pin Ceramic DIP (Suffix: -Z)

24-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(Case No.: DIP-24C-C04)

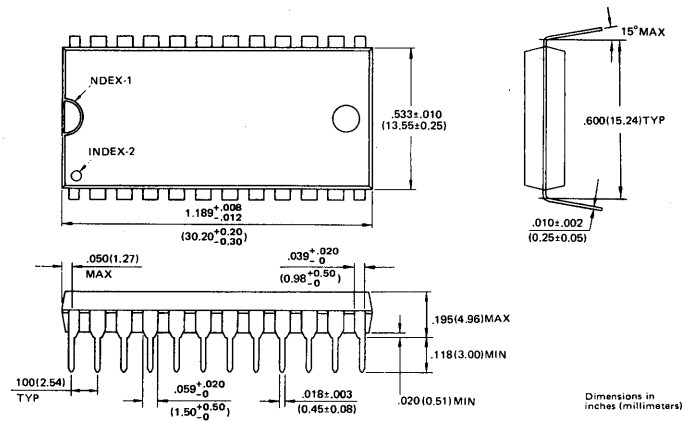


4

PACKAGE DIMENSIONS

Standard 24-pin Plastic DIP (Suffix: -M)

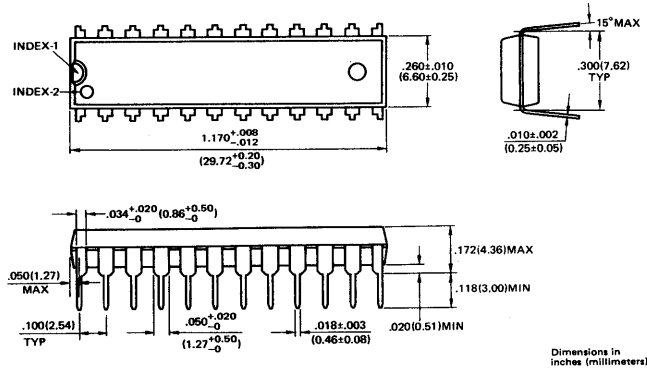
24-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(Case No.: DIP-24P-M02)



4

Standard 24-pin Plastic DIP (Suffix: -M)

24-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(Case No.: DIP-24P-M03)



FUJITSU

PROGRAMMABLE BICMOS 65536-BIT READ ONLY MEMORY

MB71C44-35
MB71C44-45

Bi-CMOS 65536-BIT DEAP PROM (8192 WORDS X 8 BITS)

November 1988
Edition 1.0

PRELIMINARY

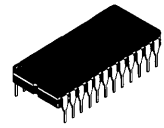
The Fujitsu MB71C44 is high speed Bi-CMOS TTL electrically field programmable read only memory organized as 16384 words by 8 bits. With threestate outputs, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP(Diffused Eutectic Aluminum Process) according to simple programming procedures.

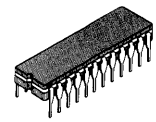
The sophisticated passive isolation termed U-FOX (U-groove isolation with thick Field OXide process) with thin eptaxial layer and Bi-CMOS TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

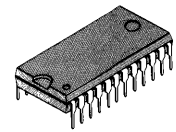
- Single +5V supply voltage.
- 8192 words x 8 bits organization , fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time 25 ns typ, 35/45 ns max
- TTL compatible inputs and outputs.
- 3-State outputs.
- One chip enable pin for simplified memory expansion.
- 24-pin Ceramic (Cerdip) DIP(300 & 600 mil)
- 24-pin Plastic DIP (300 & 600mil)
- 24-pin Ceramic (Metal Seal) FPT
- 28-pad Ceramic(Metal Seal) LCC



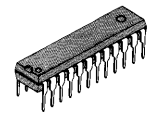
CERAMIC PACKAGE
DIP-24C-C01



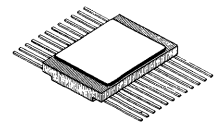
CERAMIC PACKAGE
DIP-24C-C04(-SK)



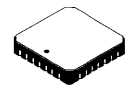
PLASTIC PACKAGE
DIP-24P-M02



PLASTIC PACKAGE
DIP-24P-M03(-SK)



CERAMIC PACKAGE
FPT-24C-A01



CERAMIC PACKAGE
LCC-28C-A01

ABSOLUTE MAXIMUM RATINGS (see NOTE)

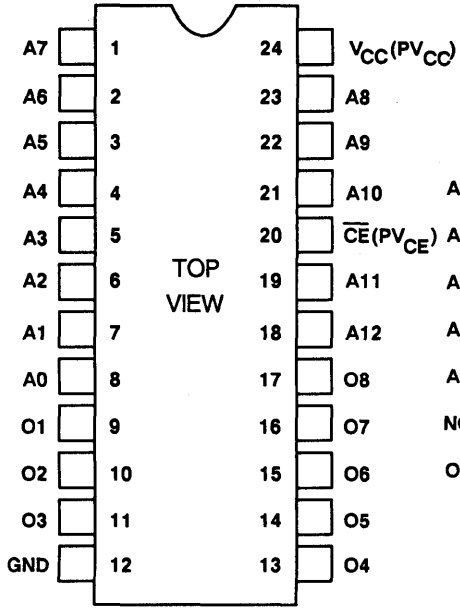
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	-0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CCP}	-0.5 to +7.5	V
Input Voltage		V_{IN}	-1.5 to 5.5	V
Input Voltage(during programming)		V_{IPRG}	22.5	V
Output Voltage(during programming)		V_{OPRG}	-0.5 to +22.5	V
Input Current		I_{IN}	-20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+75	mA
Storage Temperature	CERAMIC	T_{stg}	-65 to +150	°C
	PLASTIC		-40 to +125	
Output Voltage		V_{OUT}	-0.5 to 5.5	V

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

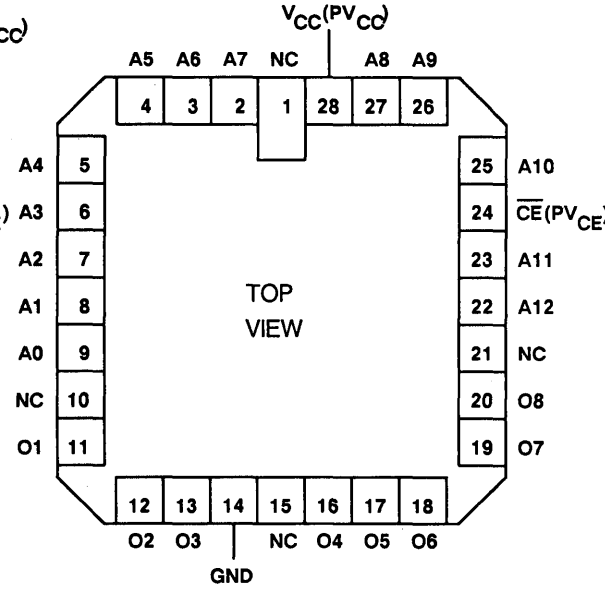
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

PIN ASSIGNMENT



PAD CONFIGURATION



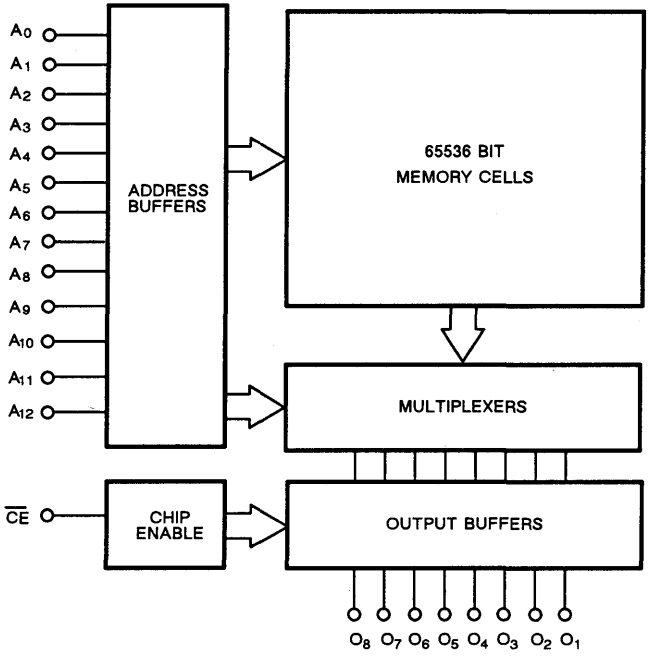
MB71C44 MODE SELECTION

MODE	$\overline{CE1}$	Output $O_1 \sim O_8$
READ	V_{IL}	D_{OUT}
CHIP-DISABLE	V_{IH}	HZ
WRITE	PV_{CE}	HZ

HZ : high-impedance
D_{OUT} : memory answer
PV_{CE} : 20V (see programming information)

PIN CONFIGURATIONS

Fig. 1 — MB71C44 BLOCK DIAGRAM



CAPACITANCE (f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25 °C)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	5.5	V
Ambient Temperature	T_A	0	-	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	µA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	µA
Output Low Voltage	I_{OL} = 10mA	V_{OL}			0.45	V
	I_{OL} = 16mA				0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)		I_{OIH}			40	µA
Output Leakage Current (V_O = 0.45V, chip disabled)		I_{OIL}			-40	µA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}		40**	60	mA
Output High Voltage (I_O = -2.4mA)		V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)		I_{OS}*	-15		-60	mA

Note: * Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

** This value denote conditions at T_A=25°C and V_{CC} = +5.0V

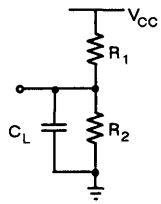


Fig. 2 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

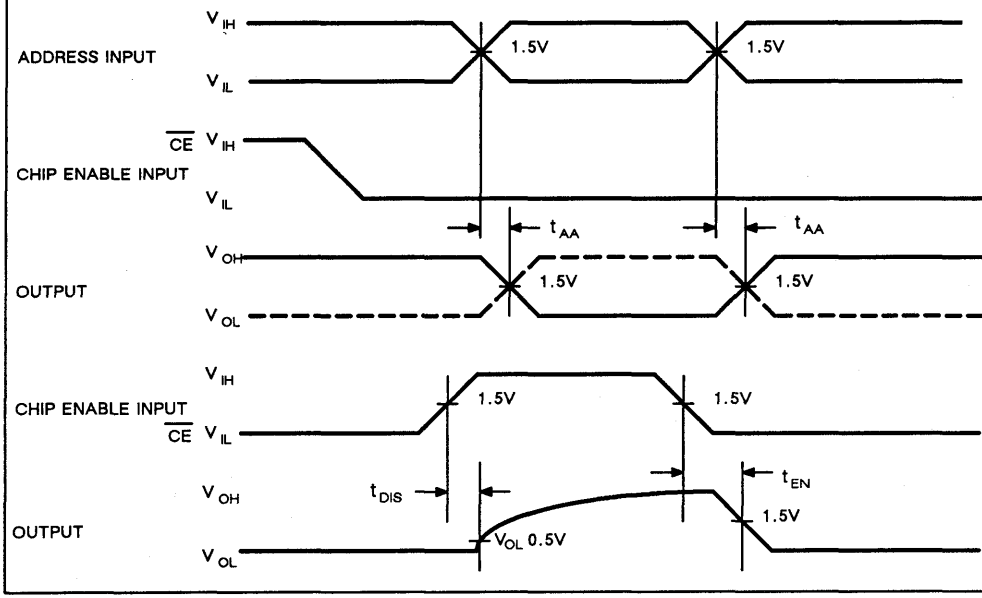
	MB71C44		
	R_1	R_2	C_L
t_{AA}	300 Ω	600 Ω	30pF
t_{DIS}	300 Ω	600 Ω	30pF
t_{EN}	300 Ω	600 Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter	Symbol	MB71C44-35		MB71C44-45		Unit
		Typ	Max	Typ	Max	
Access Time (via address input)	t_{AA}	25	35	25	45	ns
Output Disable Time	t_{DIS}	15	25	15	30	ns
Output Enable Time	t_{EN}	15	25	15	30	ns

OPERATION TIMING DIAGRAM



Note: Output disable time is the time taken for the output to reach a high resistance when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

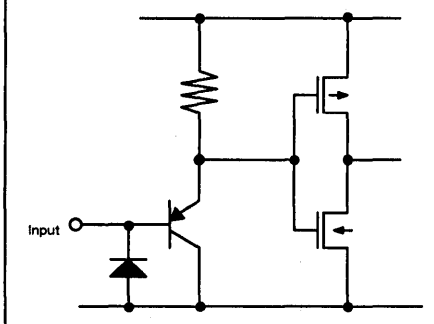
4

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, Bi-CMOS TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Fig. 3 - MB71C44 INPUT



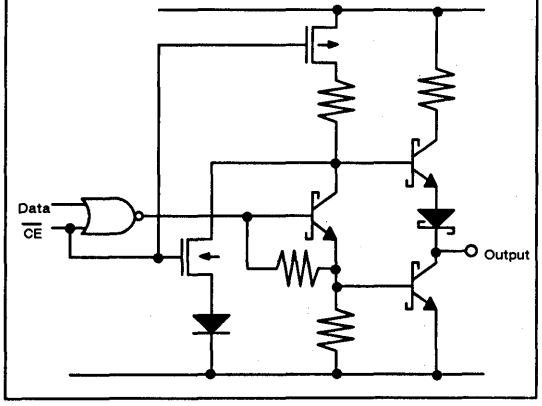
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Bi-CMOS TTL circuit technology is used to achieve high-speed operation.

Fig. 4 - MB71C44 OUTPUT



TYPICAL CHARACTERISTICS CURVES

Fig.5-I_{IN} INPUT CURRENT VS. V_{IN} INPUT VOLTAGE

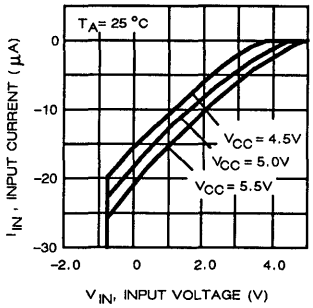


Fig.6-I_{OL} OUTPUT LOW CURRENT VS. V_{OL} OUTPUT LOW VOLTAGE

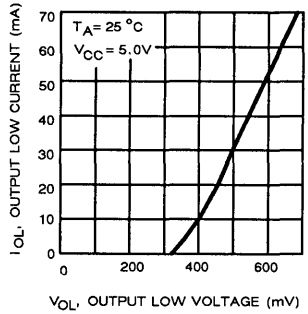


Fig.7-I_{OH} OUTPUT HIGH CURRENT VS. V_{OH} OUTPUT HIGH VOLTAGE

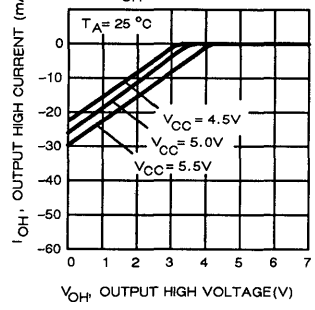


Fig.8-t_{AA} ACCESS TIME VS. AMBIENT TEMERATUERE

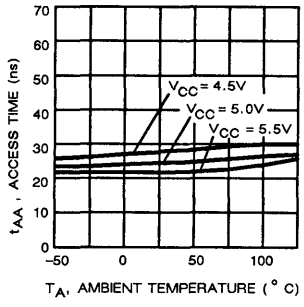


Fig.9-t_{DIS} DISABLE VS. AMBIENT TEMPERATURE

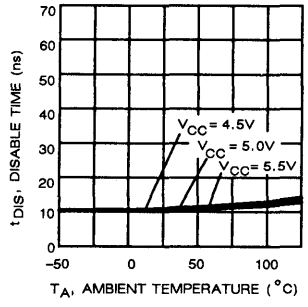


Fig.10-t_{EN} ENABLE TIME VS. AMBIENT TEMPERATURE

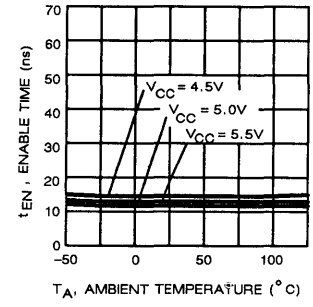
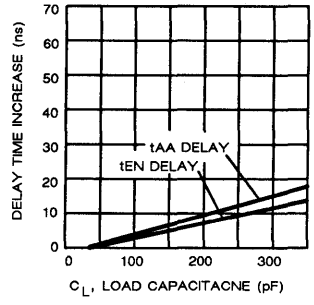


Fig.11-DELAY TIME INCREASE VS. C_L LOAD CAPACITANCE



4

PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB71C00 series is the junction-shorting Bi-CMOS PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor.

The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate(Fig. 5).

Each memory cell is divided by passive isolations named U-FOX (U-groove isolation with thick Field OXide process).

The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process" (DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

Fig. 5 - PROGRAMMED CELL (CROSS SECTION)

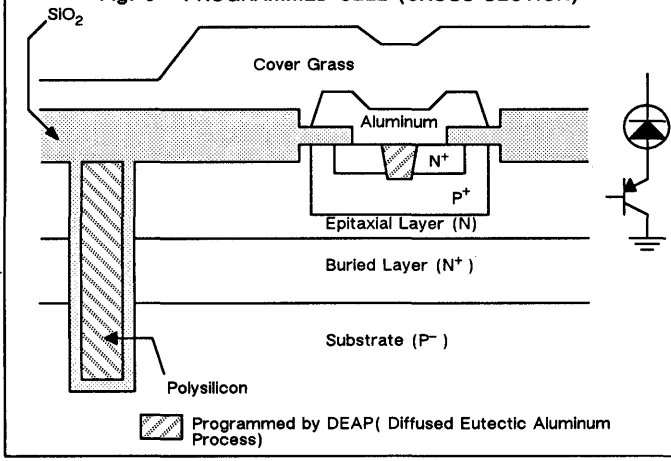
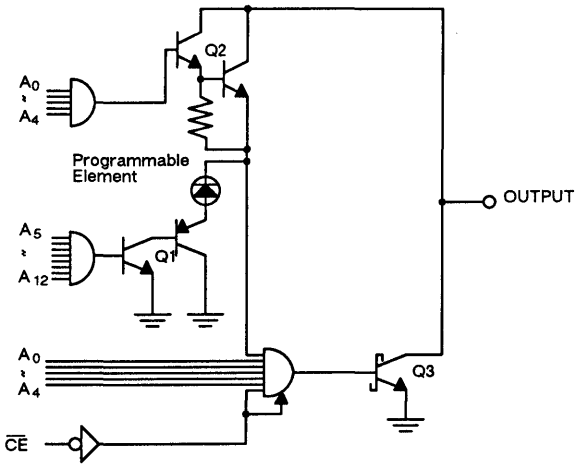


Fig. 6 - INTERNAL PROGRAMMING CIRCUIT



PROGRAMMING INFORMATION (continued)

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

As shown in Fig. 6, transistors, Q1 and Q2, are turned on to select the desired bit for programming by using thirteen address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q2 and memory cell into transistor Q1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified when all of chip enables are taken enable. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{CC}= 2.4V and V = 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH}		2.0		5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	V
Programming Pulse Current	I_{PRG}		70		75	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS (TA = 25°C)

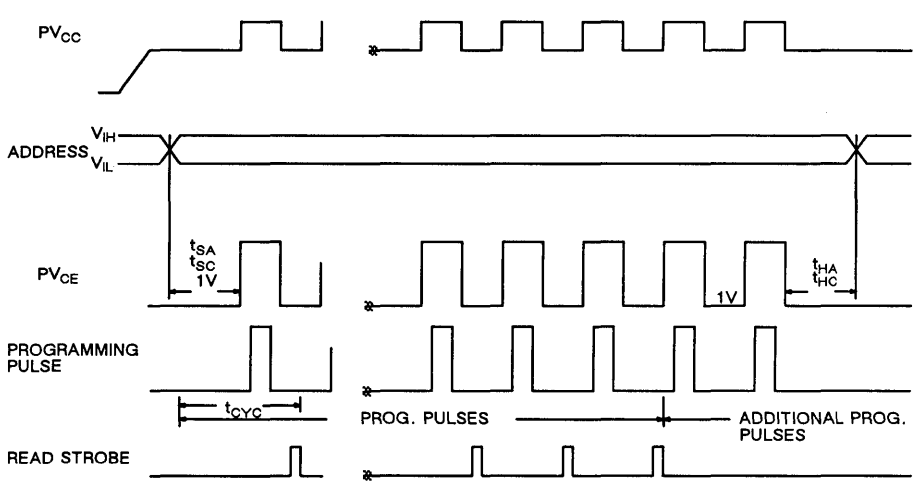
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	µs
Programming Pulse Width	t_{PW} (1)	10	11	12	µs
Programming Pulse Rise Time	t_r (2)	–	–	2	µs
PV_{CE} Pulse Rise Time	t_r (3)	–	–	2	µs
PV_{CC} Pulse Rise Time	t_r (4)	–	–	2	µs
Programming Pulse Fall Time	t_f (5)	–	–	2	µs
PV_{CE} Pulse Fall Time	t_f (6)	–	–	2	µs
PV_{CC} Pulse Fall Time	t_f (7)	–	–	2	µs
Address Input Set-up Time	t_{SA}	2	–	–	µs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	µs
PV_{CE} Set-up Time	t_{SP} (8)	4	–	–	µs
Address Input Hold Time	t_{HA}	2	–	–	µs
Chip Enable Input Hold Time	t_{HC}	2	–	–	µs
PV_{CE} Hold Time	t_{HP} (9)	2	–	–	µs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (10)	10	–	–	µs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	µs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Note: (1) Stipulated 400Ω load and 15V.
(2) From 1V to 19V (400Ω load).
(3) From 1V to 19V.
(4) From 5.2V to 6.8V.
(5) From 19V to 1V (400Ω load).
(6) From 19V to 1V.
(7) From 6.8V to 5.2V.
(8) From PV_{CE} pulse 19V to programming pulse 1V.
(9) From programming pulse 1V to PV_{CE} pulse 19V
(10) From PV_{CE} pulse 1V to read strobe.

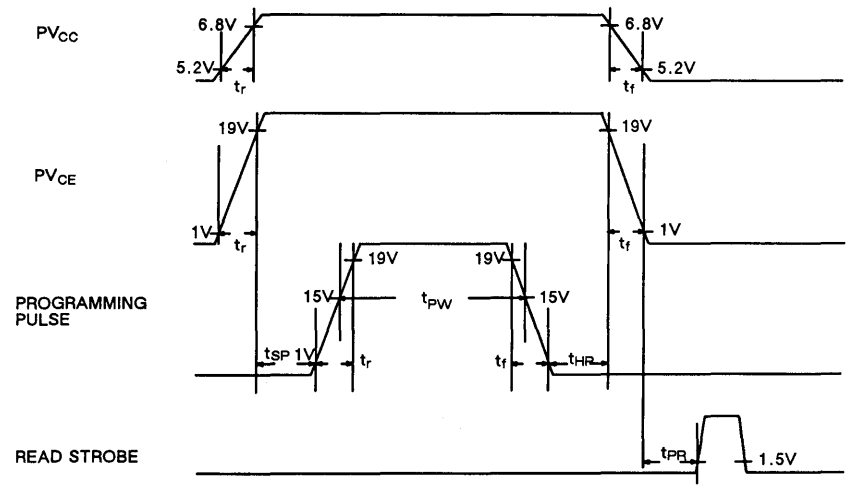
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



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PROGRAMMING INFORMATION (continued)

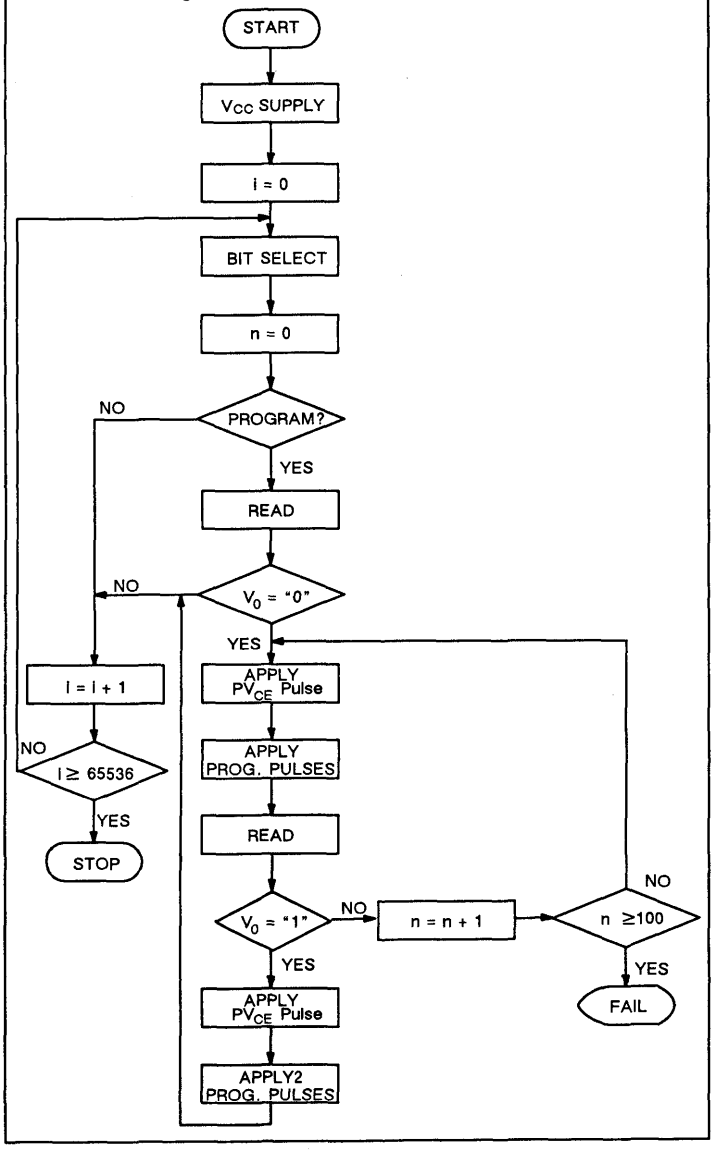
PROGRAMMING PROCEDURE

1. Apply power; V_{CC} = PV_{CC}, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 62.5mA and duration of t_{PW} (11μS) after a delay of t_{SP} (4μS).
6. Read the output V_O after a delay of t_{PR} (10μS).
   a) In the case of V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μS)
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μS).

Note

1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C ±2°C)

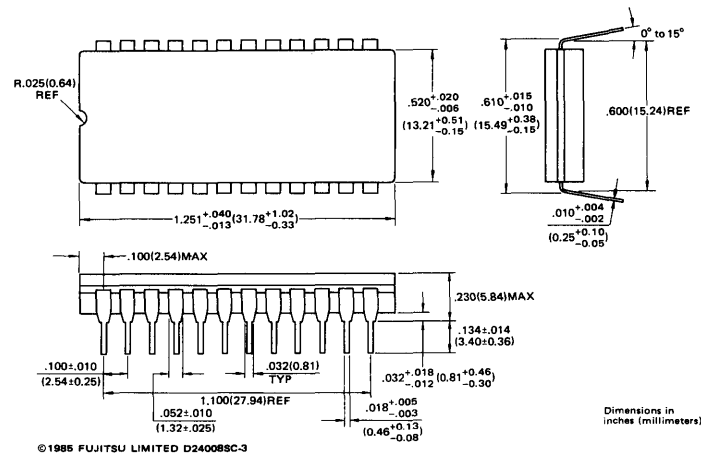
Fig. 7 - PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

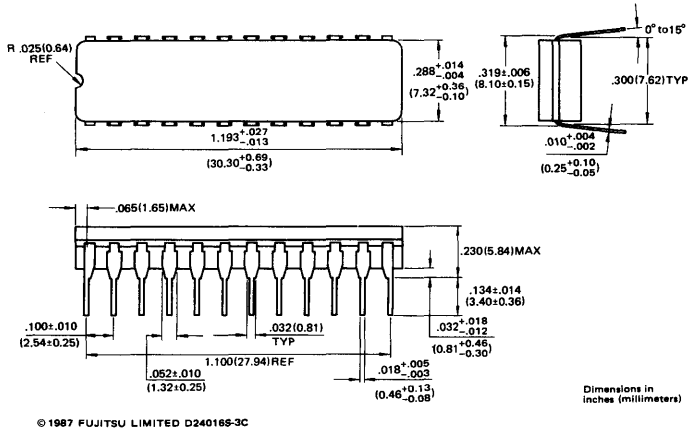
Standard 24-pin Ceramic (Cerdip) DIP (Suffix: -Z)

24-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(Case No.: DIP-24C-C01)



Standard 24-pin Ceramic (Cerdip) DIP (Suffix: -Z)

24-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(Case No.: DIP-24C-C04)



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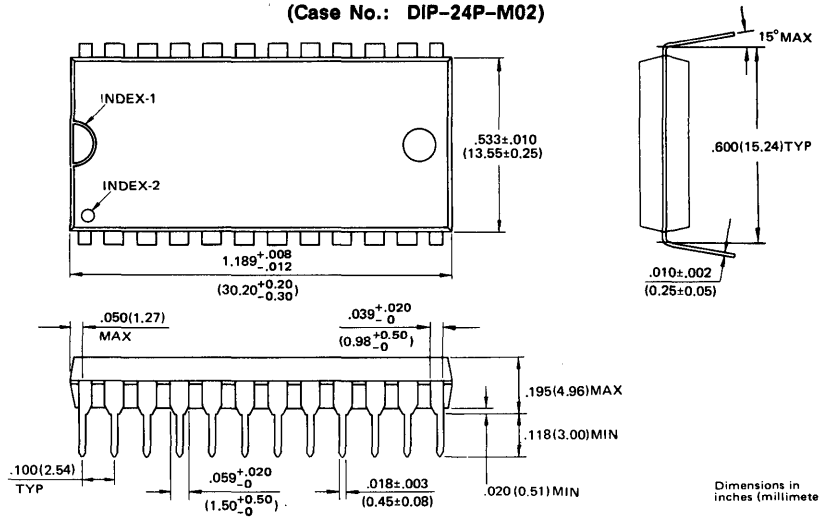
PACKAGE DIMENSIONS

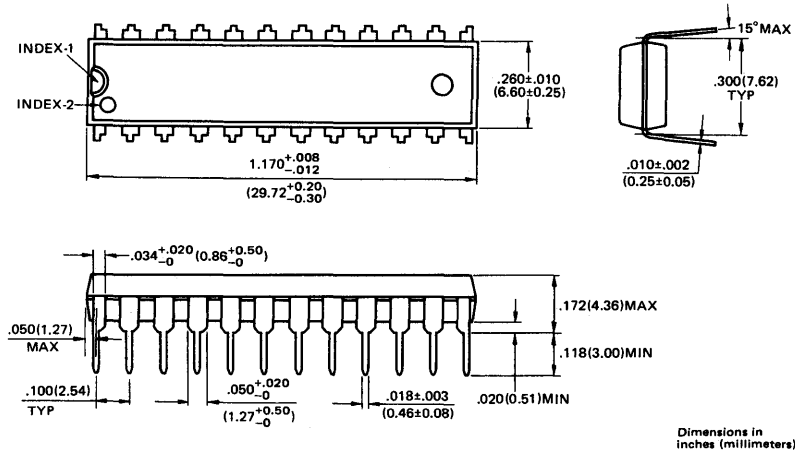
Standard 24-pin Plastic DIP (Suffix: -P)

24-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(Case No.: DIP-24P-M02)



Standard 24-pin Plastic DIP (Suffix: -P)

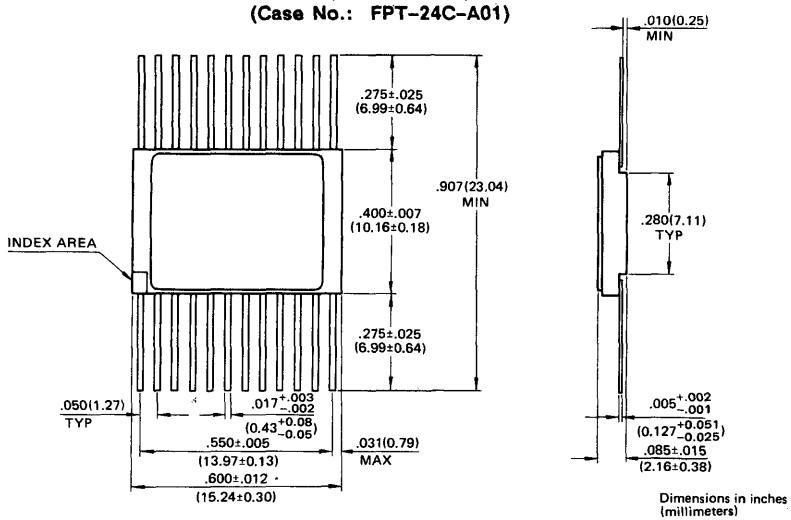
24-LEAD PLASTIC SKINNY DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M03)



PACKAGE DIMENSIONS

Standard 24-pin Ceramic (Metal Seal) FPT (Suffix: -CF)

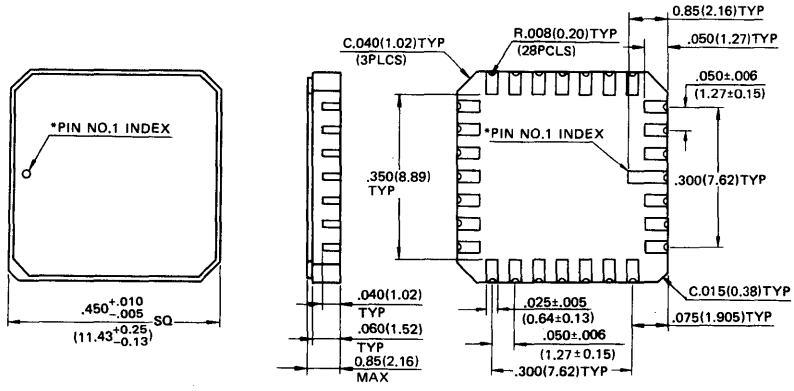
24-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(Case No.: FPT-24C-A01)



Dimensions in inches (millimeters)

Standard 28-pad Ceramic (Metal Seal) LCC (Suffix: -CV)

28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(Case No.: LCC-28C-A01)



*Shape of Pin No.1 index: Subject to change without notice

Dimensions in inches (millimeters)

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FUJITSU

PROGRAMMABLE BICMOS 131072-BIT READ ONLY MEMORY

MB71C46-35 MB71C46-45

August 1988
Edition 2.0

Bi-CMOS 131072-BIT DEAP PROM (16384 WORDS x 8 BITS)

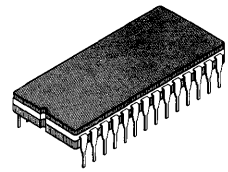
The Fujitsu MB71C46 is high speed BICMOS TTL electrically field programmable read only memory organized as 16384 words by 8 bits. With threestate outputs, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP(Diffused Eutectic Aluminum Process) according to simple programming procedures.

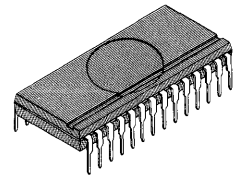
The sophisticated passive isolation termed U-FOX (U-groove isolation with thick Field OXide process) with thin eptaxial layer and BICMOS TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

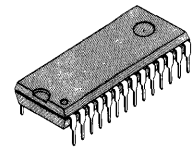
- Single +5V supply voltage.
- 16384 words x 8 bits organization , fully decoded.
- Proven high programmability and reliability.
- Programming by DEAP (Diffused Eutectic Aluminum Process).
- Simplified and lower power programming
- Low current PNP inputs.
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques.
- Fast access time 30ns typ, 35* /45 ns max
- TTL compatible inputs and outputs.
- 3 State outputs.
- Four chip enable pins for simplified memory expansion.
- 28-pin Ceramic (Cerdip) DIP
- 28-pin Plastic DIP (400 & 600mil)



CERAMIC PACKAGE
DIP-28C-C02



PLASTIC PACKAGE
DIP-28P-M02



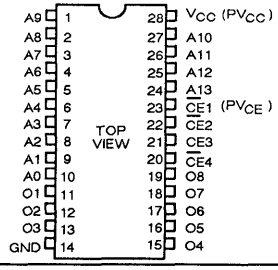
PLASTIC PACKAGE
DIP-28P-M03

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	0.5 to + 7.0	V
Power Supply Voltage (during programming)		V_{CCP}	-0.5 to +7.5	V
Input Voltage		V_{IN}	-1.5 to 5.5	V
Input Voltage(during programming)		V_{IPRG}	22.5	V
Output Voltage(during programming)		V_{OPRG}	-0.5 to +22.5	V
Input Current		I_{IN}	-20	mA
Input Current (during programming)		I_{IPRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{OPRG}	+75	mA
Storage Temperature	CERAMIC	T_{stg}	-65 to +150	°C
	PLASTIC		-40 to +125	
Output Voltage		V_{OUT}	-0.5 to 5.5	V

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

* Under development

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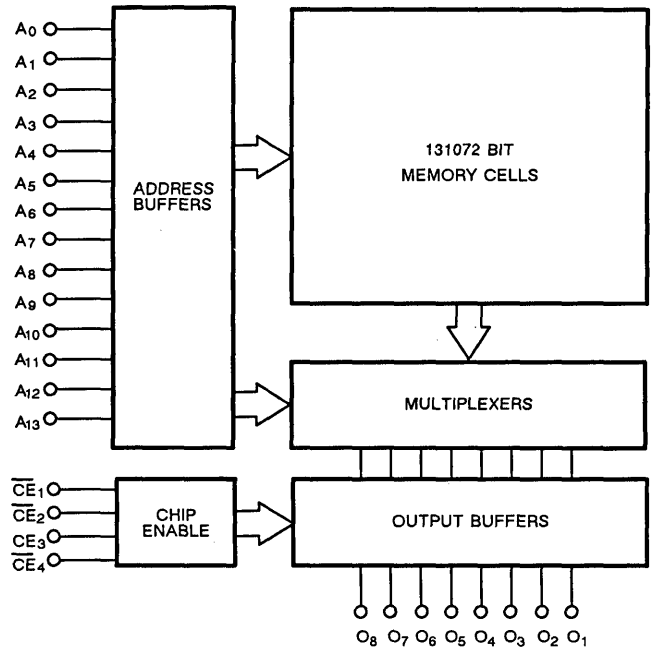
Fig. 1 — MB71C46 BLOCK DIAGRAM



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CAPACITANCE (f = 1MHz, V_{CC}= +5V, V_{IN} = +2V, T_A= 25 °C)

Parameter	Symbol	Values			Unit
		Min	Typ	Max	
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			15	pF

GUARANTEED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	5.5	V
Ambient Temperature	T_A	0	-	75	°C

DC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5V)		I_R			40	µA
Input Load Current (V_{IL} = 0.45V)		I_F			-250	µA
Output Low Voltage	I_{OL} = 10mA	V_{OL}			0.45	V
	I_{OL} = 16mA				0.50	V
Output Leakage Current (V_O = 2.4V, chip disabled)		I_{OIH}			40	µA
Output Leakage Current (V_O = 0.45V, chip disabled)		I_{OIL}			-40	µA
Input Clamp Voltage (I_{IN} = -18mA)		V_{IC}			-1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}		40**	60	mA
Output High Voltage (I_O = -2.4mA)		V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)		I_{OS}*	-15		-60	mA

Note: * Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{CE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factor testing.

** This value denote conditions at T_A=25°C and V_{CC} = +5.0V

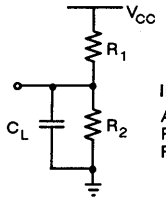


Fig. 2 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

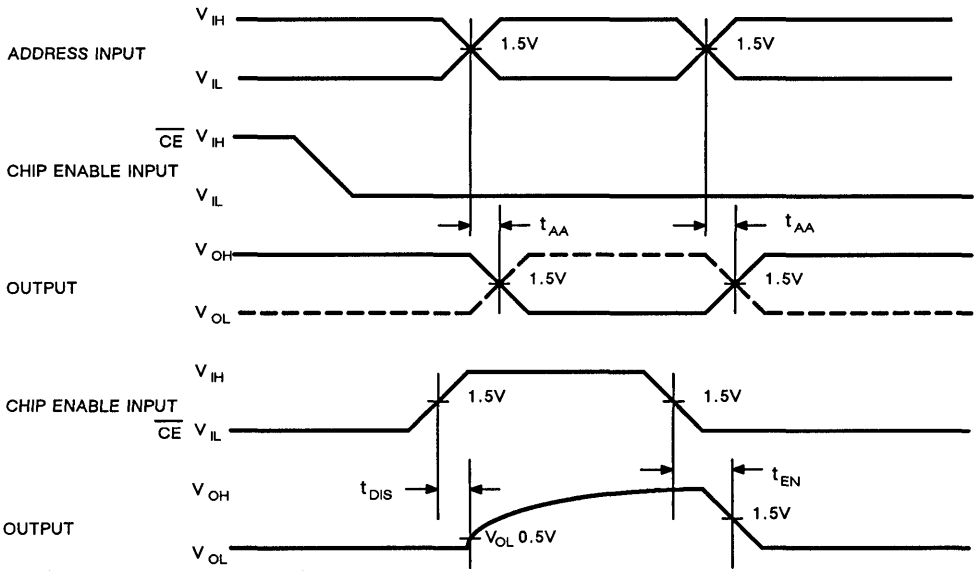
	MB71C46		
	R_1	R_2	C_L
t_{AA}	300 Ω	600 Ω	30pF
t_{DIS}	300 Ω	600 Ω	30pF
t_{EN}	300 Ω	600 Ω	30pF

AC CHARACTERISTICS

(Full guaranteed operating conditions unless otherwise noted)

Parameter	Symbol	MB71C46-35 *		MB71C46-45		Unit
		Typ	Max	Typ	Max	
Address Time (via address input)	t_{AA}	(25)	(35)	30	45	ns
Output Disable Time	t_{DIS}	(15)	(25)	15	30	ns
Output Enable Time	t_{EN}	(15)	(25)	15	30	ns

OPERATION TIMING DIAGRAM



Note: Output disable time is the time taken for the output to reach a high resistance when some of chip enables is taken disable. Output enable time is the time taken for the output to become active when all of chip enables are taken enable. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

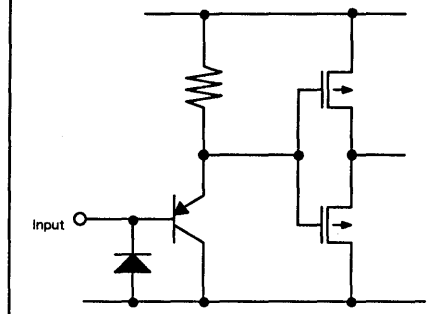
*** Under Development**

INPUT/OUTPUT CIRCUIT INFORMATION

INPUT

In the input circuit, BICMOS TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Fig. 3 - MB71C46 INPUT



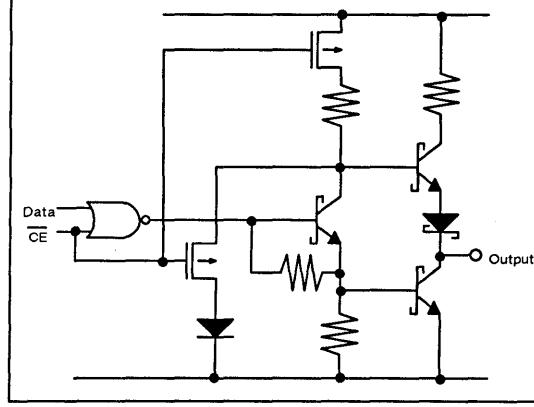
THREE-STATE OUTPUT

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, BICMOS TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

Fig. 4 - MB71C46 OUTPUT



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TYPICAL CHARACTERISTICS CURVES

Fig.5-I_{IN} INPUT CURRENT VS. V_{IN} INPUT VOLTAGE

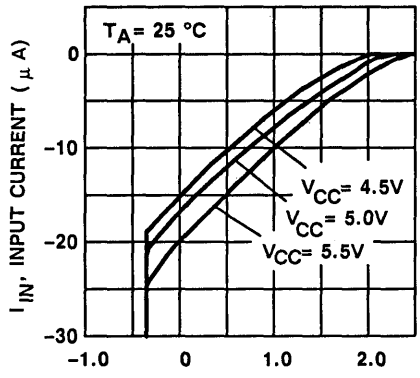


Fig.6-I_{OL} OUTPUT LOW CURRENT VS. V_{OL} OUTPUT LOW VOLTAGE

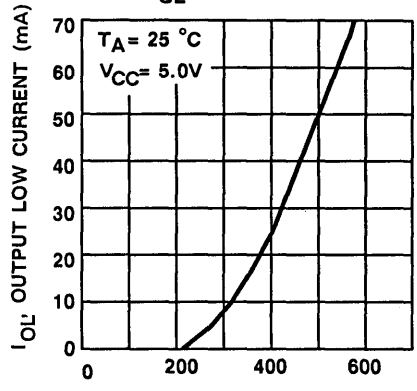


Fig.7-I_{OH} OUTPUT HIGH CURRENT VS. V_{OH} OUTPUT HIGH VOLTAGE

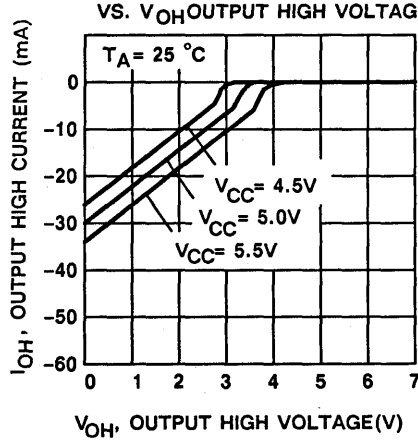
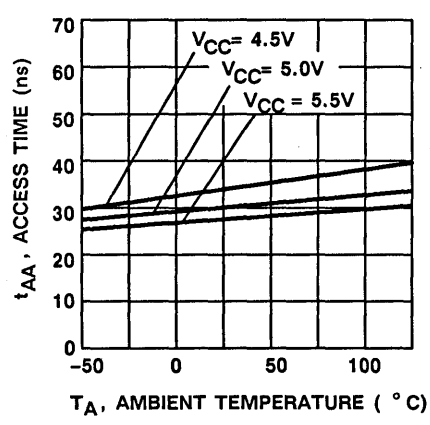


Fig.8-t_{AA} ACCESS TIME VS. AMBIENT TEMERATUERE



TYPICAL CHARACTERISTICS CURVES

Fig.9-t_{DIS} DISABLE TIME VS. AMBIENT TEMPERATURE

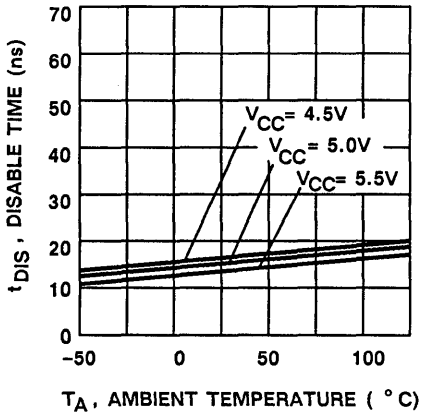


Fig.10-t_{EN} ENABLE TIME VS. AMBIENT TEMPERATURE

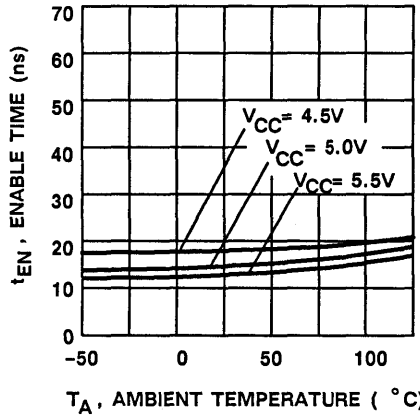
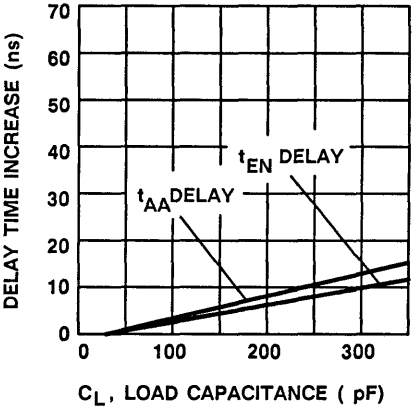


Fig.11-DELAY TIME INCREASE VS. C_L LOAD CAPACITANCE



4

PROGRAMMING INFORMATION

FUJITSU PROM TECHNOLOGY

The Fujitsu MB71C00 series is the junction-shorting Bi-CMOS PROM. A memory cell consists of a programmable element of a PN diode and a vertically connected PNP transistor.
The current blocking state of the reverse diode is changed to the current conducting state of the shorted-junction diode by programming. The programming element of the PN diode uses the N^+ and P^+ diffusion layer, the PNP transistor uses a P^+ diffusion layer, an N^+ epitaxial layer, and a P^- substrate(Fig. 12).

Each memory cell is divided by passive isolations named U-FOX (U-groove isolation with thick Field OXide process).

The vertical structure of the junction-shorting memory cell makes a high packing density possible.

In programming, reverse current pulses are applied to the cathode of the PN diode. This increases the temperature at the junction. When the temperature reaches the point where the silicon and aluminum form a eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and results in junction shorting. This program technique was therefore named "Diffused Eutectic Aluminum Process"(DEAP).

Once the junction is shorted, the power dissipation at the junction decreases to less than one fifth, and the temperature decreases. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

Fig. 12 - PROGRAMMED CELL (CROSS SECTION)

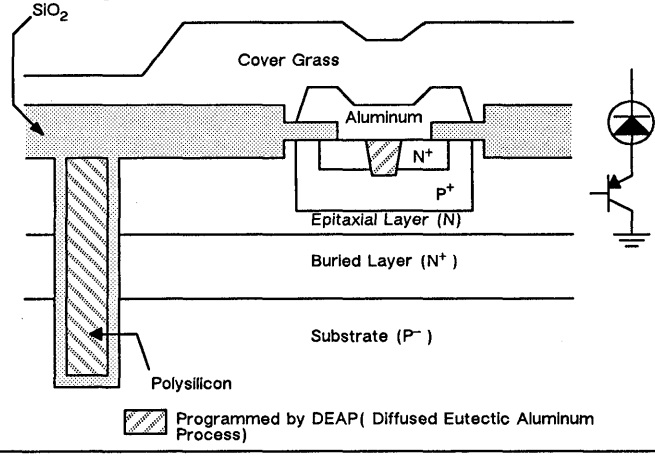
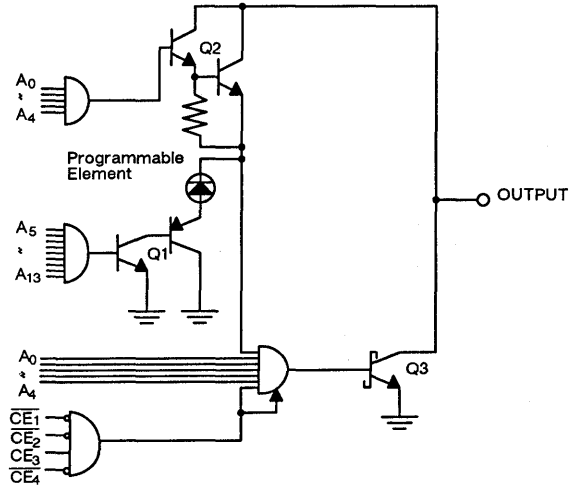


Fig. 13 - INTERNAL PROGRAMMING CIRCUIT



PROGRAMMING INFORMATION (continued)

SPECIAL FACTORY TESTING

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

PROGRAMMING (in electrical view)

The device is manufactured with outputs low (positive logic "zero") in all storage cells. An output at the selected cell is changed to high (logic "one") by programming.

As shown in Fig. 13, transistors, Q1 and Q2, are turned on to select the desired bit for programming by using fourteen address inputs. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through transistor Q2 and memory cell into transistor Q1. This programming current changes the programmable element to the conducting state.

The pulse train is stopped and two additional programming pulses are then applied to assure that the element is programmed properly, as soon as the output voltage indicates that the selected cell is in the logic "one" state. One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

VERIFICATION

After the device has been programmed, the correct program pattern can be verified by taking chip enable input low. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4mA at V_{OH}= 2.4V and V_{CC}= 7.0V at 25°C ambient temperature.

LIABILITY

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

4

DC SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		0		0.8	V
Input High Voltage	V_{IH}		2.0		5.25	V
Power Supply Voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	V
Programming Pulse Current	I_{PRG}		70		75	mA
PV_{CE} Pulse Voltage	PV_{CE}		20	20	22	V
Programming Pulse Clamp Voltage	V_{PRG}		20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}		230		260	mA
Reference Voltage for a Prog. "1"	V_{REF}		1.0	1.5	2.4	V

PROGRAMMING INFORMATION (continued)

AC SPECIFICATIONS (TA = 25°C)

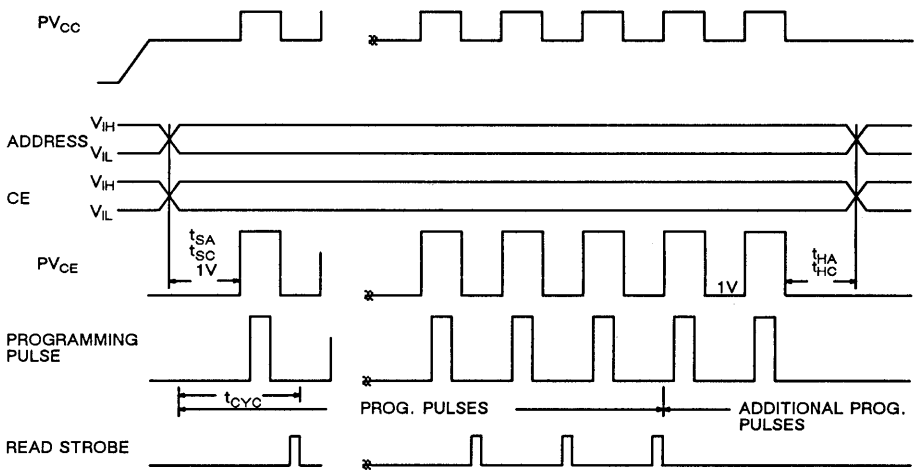
Parameter	Symbol	Min	Typ	Max	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	µs
Programming Pulse Width	t_{PW} (1)	10	11	12	µs
Programming Pulse Rise Time	t_r (2)	–	–	2	µs
PV_{CE} Pulse Rise Time	t_r (3)	–	–	2	µs
PV_{CC} Pulse Rise Time	t_r (4)	–	–	2	µs
Programming Pulse Fall Time	t_f (5)	–	–	2	µs
PV_{CE} Pulse Fall Time	t_f (6)	–	–	2	µs
PV_{CC} Pulse Fall Time	t_f (7)	–	–	2	µs
Address Input Set-up Time	t_{SA}	2	–	–	µs
Chip Enable Input Set-up Time	t_{SC}	2	–	–	µs
PV_{CE} Set-up Time	t_{SP} (8)	4	–	–	µs
Address Input Hold Time	t_{HA}	2	–	–	µs
Chip Enable Input Hold Time	t_{HC}	2	–	–	µs
PV_{CE} Hold Time	t_{HP} (9)	2	–	–	µs
PV_{CE} Pulse Trailing Edge to Read Strobe Time	t_{PR} (10)	10	–	–	µs
Programming Pulse Number	–	–	–	100	Times
Programming Time/Bit	–	120	150	6120	µs/bit
Additional Programming Pulse Number	–	2	2	2	Times

Note: (1) Stipulated 400Ω load and 15V.
(2) From 1V to 19V (400Ω load).
(3) From 1V to 19V (200Ω load).
(4) From 5.2V to 6.8V (30Ω load).
(5) From 19V to 1V (400Ω load).
(6) From 19V to 1V (200Ω load).
(7) From 6.8V to 5.2V (30Ω load).
(8) From PV_{CE} pulse 19V to programming pulse 1V.
(9) From programming pulse 1V to PV_{CE}pulse 19V
(10) From PV_{CE} pulse 1V to read strobe.

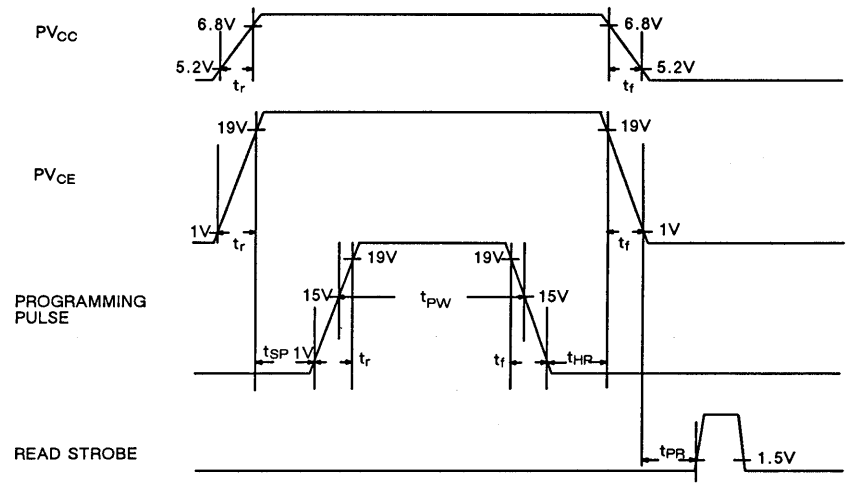
4

PROGRAMMING INFORMATION (continued)

TYPICAL WAVEFORMS



ONE DETAILED PROGRAMMING CYCLE



4

PROGRAMMING INFORMATION (continued)

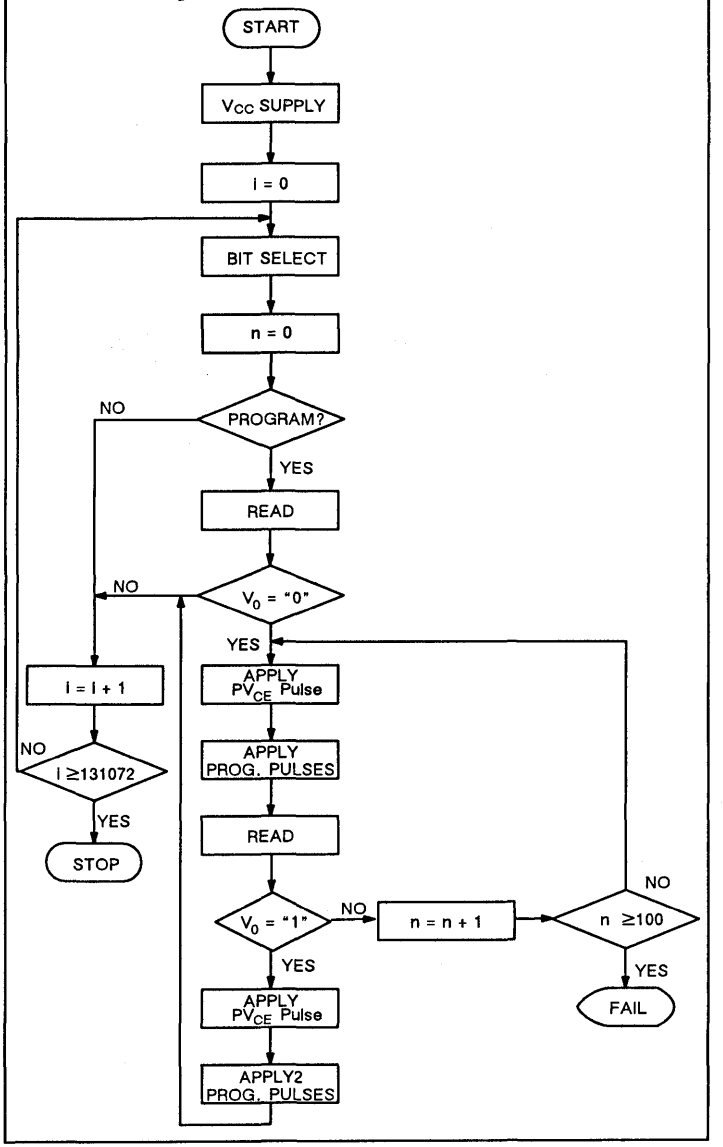
PROGRAMMING PROCEDURE

1. Apply power; $V_{CC} = PV_{CC}$, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 62.5mA and duration of t_{PW} (11μS) after a delay of t_{SP} (4μS).
6. Read the output V_O after a delay of t_{PR} (10μS).
   a) In the case of V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50μS)
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2μS).

Note

1) Programming must be done bit by bit.
2) Ambient temperature during programming must be room temperature. (25°C ± 2°C)

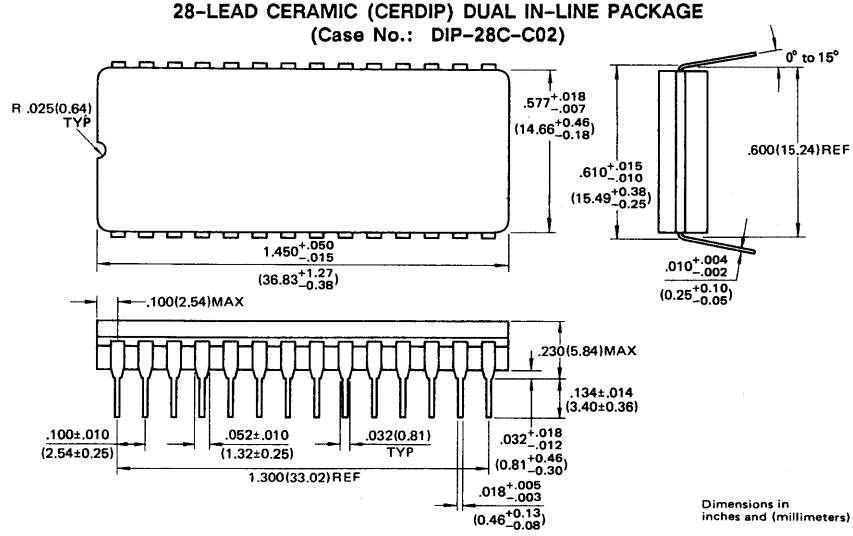
Fig. 14 – PROGRAMMING FLOW CHART



PACKAGE DIMENSIONS

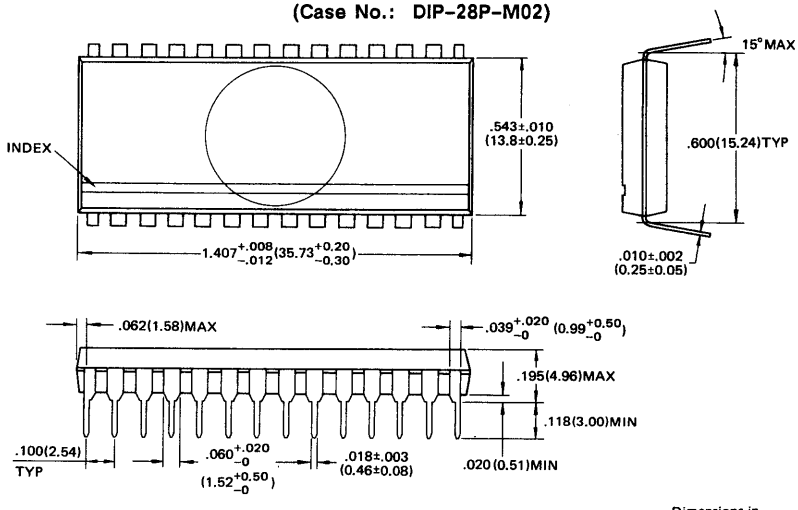
Standard 28-pin Ceramic DIP (Suffix: -Z)

28-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(Case No.: DIP-28C-C02)



Standard 28-pin Plastic DIP (Suffix: -M)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-28P-M02)



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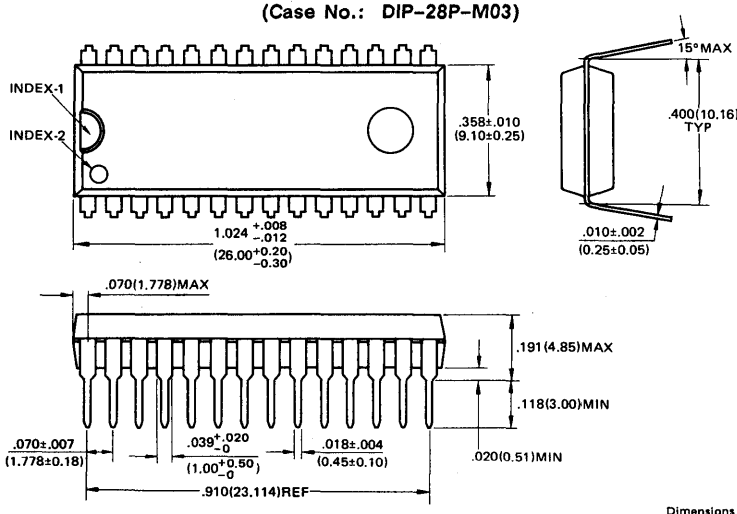
PACKAGE DIMENSIONS

Standard 28-pin Plastic DIP (Suffix: -M)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(Case No.: DIP-28P-M03)



Dimensions in
inches (millimeters)

4

FUJITSU

SCHOTTKY 4096-BIT REGISTERED OUTPUT PROM

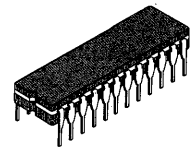
MB 7226RA-20/-25/-25W
MB 7226RA-20L/-25L/-25LW
MB 7226RS-20/-25/-25W

June 1987
Edition 3.0

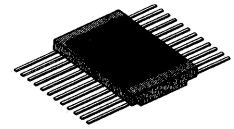
SCHOTTKY 4,096-BIT REGISTERED OUTPUT PROM

The Fujitsu MB 7226 is a 4 Kbit bipolar programmable read-only memory circuit, with registered output (output data is latched in a register). The output register can be initialized to a field-programmable initial value or all 1s, either synchronously (MB 7226RS) or asynchronously (MB 7226RA). Three-state outputs can also be enabled either synchronously or asynchronously, in either model. DEAP memory cells are used to provide fast and reliable programming.

- 512 word x 8 bit PROM data organization
- Power supply current:
  170 mA max (MB 7226RA/RS)
  100 mA max (MB 7226RA-L)
- Fast clock access time:
  20 ns (MB 7226RA-20/20L)
  (MB 7226RS-20)
  25 ns (MB 7226RA-25/25L/25W/25LW)
  (MB 7226RS-25/25W)
- Output register for data reads
- Register can be initialized to a field programmable initial value or all 1s.
- Register can be initialized synchronously (MB 7226RS) or asynchronously (MB 7226RA).
- Single-supply +5 V operation
- TTL-compatible I/O
- Fast Schottky bipolar circuitry
- Low current inputs
- Three-state outputs
- Outputs can be enabled either synchronously or asynchronously.
- DEAP (diffused eutectic aluminum process) memory cells are reliable and easily programmed.
- Test cells allow extensive testing of AC, DC, and programming characteristics before shipment.



CERAMIC PACKAGE
DIP-24C-C04

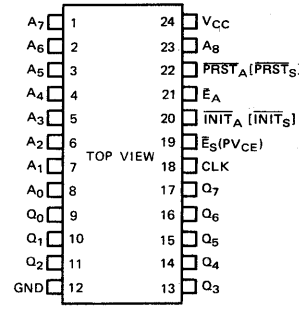


CERAMIC PACKAGE
FPT-24C-A01

LCC-28C-A01: See Page 15

4

PIN ASSIGNMENT



Symbols in blankets : MB 7226RS

LCC PAD CONFIGURATION: See Page 15

ABSOLUTE MAXIMUM RATINGS

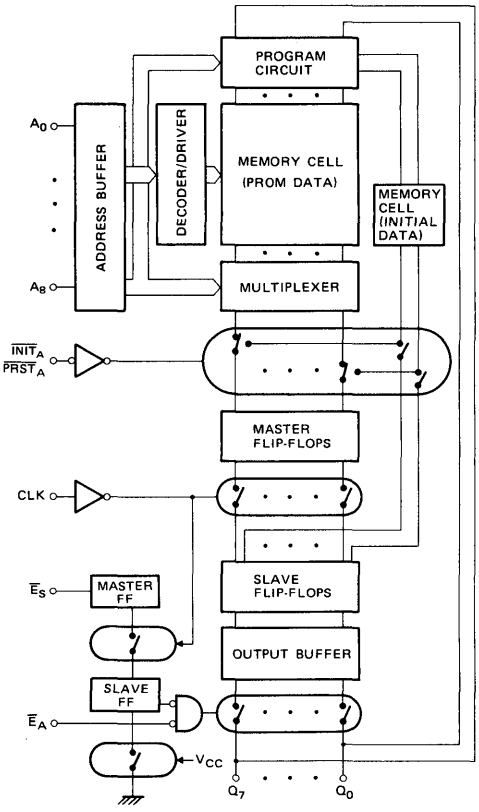
Parameter	Symbol	Rating	Unit
Power-supply voltage	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-1.5 to +5.5	V
Input current	I_{IN}	-20	mA
Output current	I_{OUT}	+100	mA
Power-supply voltage (during programming)	V_{CCP}	-0.5 to +7.5	V
Input voltage (during programming)	V_{IPRG}	+22.5	V
Input current (during programming)	I_{IPRG}	+270	mA
Output voltage (during programming)	V_{OPRG}	-0.5 to +22.5	V
Output current (during programming)	I_{OPRG}	+150	mA
Storage temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

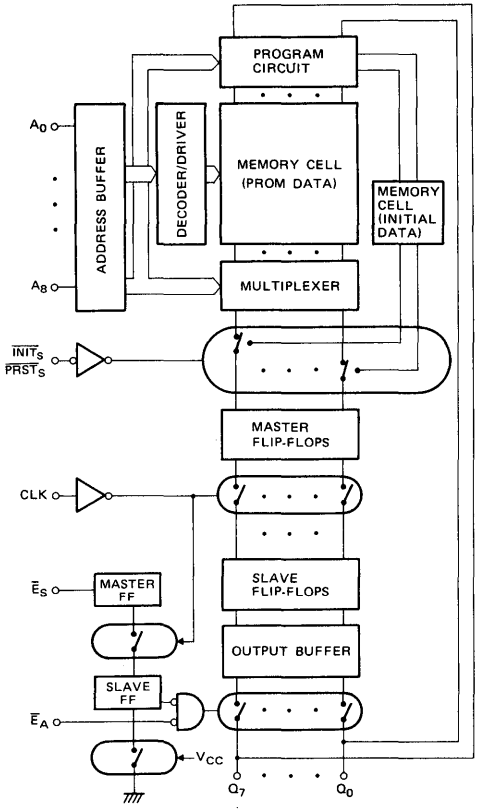
Fig. 1 – MB 7226RA BLOCK DIAGRAM



Input					Output	Operating mode	Remarks
$\overline{PRST}_A$	$\overline{INIT}_A$	CLK	$\overline{E}_A$	$\overline{E}_S$			
L	L	X	L	L	H	*1	
L	H	X	L	L	INITIAL DATA (H)	INITIALIZE	PROGRAMMED
H	L	X	L	L	INITIAL DATA	INITIALIZE	PRO-GRAMMABLE
H	H	↑	L	L	PROM DATA	LOAD REGISTER	
X	X	↑	X	H	Z	CHIP DISABLE	
X	X	X	H	X	Z	CHIP DISABLE	

*1 When the $\overline{PRST}_A$ and $\overline{INIT}_A$ inputs are brought high at the same time, the output cannot be determined eighter H or L.

Fig. 2 – MB 7226RS BLOCK DIAGRAM



Input					Output	Operating mode	Remarks
$\overline{PRST}_S$	$\overline{INIT}_S$	CLK	$\overline{E}_A$	$\overline{E}_S$			
L	L	↑	L	L	–	–	
L	H	↑	L	L	INITIAL DATA (H)	INITIALIZE	PROGRAMMED
H	L	↑	L	L	INITIAL DATA	INITIALIZE	PRO-GRAMMABLE
H	H	↑	L	L	PROM DATA	LOAD REGISTER	
X	X	↑	X	H	Z	CHIP DISABLE	
X	X	X	H	X	Z	CHIP DISABLE	

1. READ OPERATIONS

1.1 Overview (see Figures 1 and 2)

During PROM reads, data is shifted through a register, made of master-slave flip-flops, before appearing at the outputs. When a new address is applied to the address inputs (A_0 through A_8), new data appears in the master register. At the next clock pulse this data is transferred to the slave register. The slave register data appears at the three-state outputs when both chip-enable inputs are low. (Outputs are automatically disabled during power-up, when the inputs are in an indeterminate state.) For synchronous operation, the $\overline{E}_A$ input is kept low. Bringing the $\overline{E}_S$ input low will then enable the outputs at the next clock pulse, while bringing $\overline{E}_S$ high will disable them at the next clock pulse. For asynchronous operation, the $\overline{E}_S$ input is kept low. Bringing $\overline{E}_A$ low will then immediately enable the outputs, while bringing it high will immediately disable them.

If the $\overline{INIT}$ or $\overline{PRST}$ input is brought low the register latch is loaded with a field-programmable initial value ($\overline{INIT}$) or all 1s ($\overline{PRST}$), rather than with PROM data. In the MB 7226RS the master register is loaded immediately, and the contents are transferred to the slave register at the next clock pulse. In the MB 7226RA both the master and slave registers are loaded immediately.

1.2 Timing Considerations

a) PROM Data Read (see Figure 3)

After an address change, address setup time $t_S(A)$ must elapse before the master register contains valid new PROM data. The clock must then rise, within address hold time $t_H(A)$, to shift the data to the slave register. The data will appear at the outputs within clock access time $t_A(CLK)$ after the rising edge of the clock, if the outputs had been previously enabled.

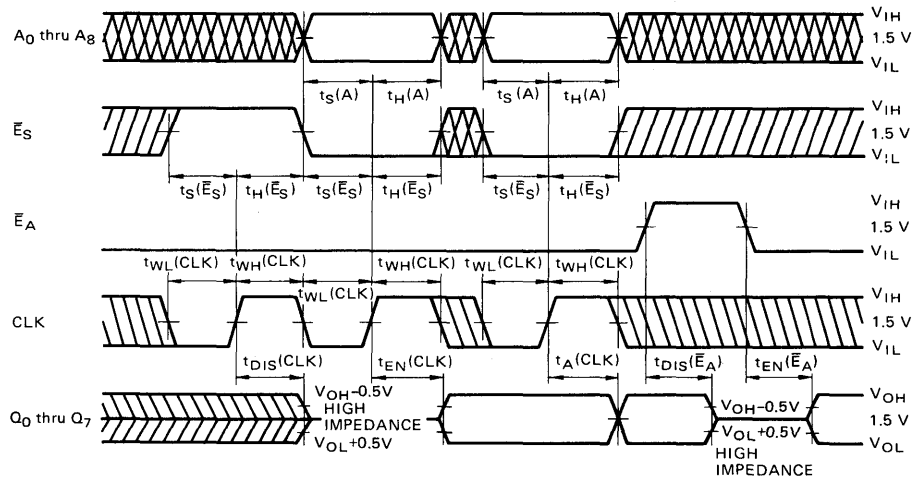
If the outputs were disabled when the data was shifted, and are subsequently enabled by bringing $\overline{E}_A$ low, asynchronous chip enable time $t_{EN}(\overline{E}_A)$ must elapse before the data appears at the outputs.

If $\overline{E}_S$ is brought low to enable the outputs, clock enable time $t_{EN}(CLK)$ must elapse after the rising edge of the next clock. During this time the data from the master register is shifted to the slave register and appears at the outputs.

In the MB 7226RA, when the registers have been initialized by $\overline{INIT}$ or $\overline{PRST}$, and the initialize input is then brought high to select PROM data, asynchronous initialize recovery time t_R ($\overline{INIT}_A$) or t_R ($\overline{PRST}_A$) must elapse after the clock signal is applied.

4

Fig. 3 – PROM DATA READ TIMING*1



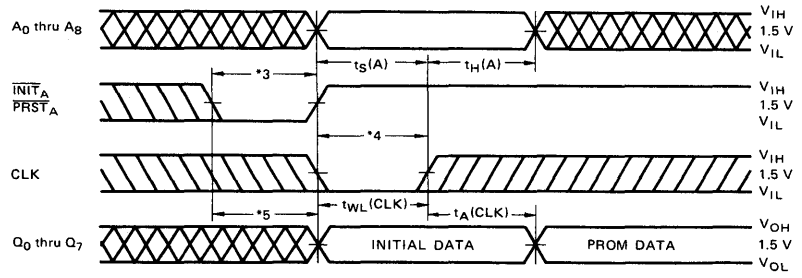
Note: *1 $\overline{INIT}$ and $\overline{PRST}$ are high.

b) Initial Data Read (see Figures 4 and 5)

In the MB 7226RA, after the $\overline{INIT}$ or $\overline{PRST}$ input is brought low, asynchronous initialize access time t_A ($\overline{INIT}_A$) or t_A ($\overline{PREST}_A$) must elapse before the initial data appears at the outputs.

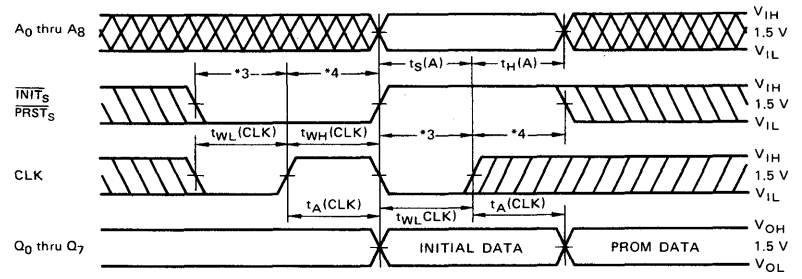
In the MB 7226RS, after the $\overline{INIT}$ or $\overline{PRST}$ input is brought low, synchronous initialize access time t_A ($\overline{INIT}_S$) or t_A ($\overline{PRST}_S$) must elapse before valid initial data appears in the master register. It is then shifted and output in the same manner as PROM data.

Fig. 4 – ASYNCHRONOUS INITIAL DATA READ TIMING (MB 7226RA)*1



Notes: *1 $\overline{E}_A$, $\overline{E}_S$ inputs are low.
*2 ⊠ Don't care.
*3 t_{WL} ($\overline{INIT}_A$), t_{WL} ($\overline{PRST}_A$)
*4 t_R ($\overline{INIT}_A$), t_R ($\overline{PRST}_A$)
*5 t_A ($\overline{INIT}_A$), t_A ($\overline{PRST}_A$)

Fig. 5 – SYNCHRONOUS INITIAL DATA READ TIMING (MB 7226RS)*1



Notes: *1 $\overline{E}_A$, $\overline{E}_S$ inputs are low.
*2 ⊠ Don't care.
*3 t_S ($\overline{INIT}_S$), t_S ($\overline{PRST}_S$)
*4 t_H ($\overline{INIT}_S$), t_H ($\overline{PRST}_S$)

DATA READ SPECIFICATIONS

Table 1 – Guaranteed Operating Conditions

Parameter	Symbol	MB 7226RA-20/-25/-20L/-25L MB7226RS-20/-25			MB 7226RA-25W/-25LW MB 7226RS-25W			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Power-supply voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
Input low voltage	V_{IL}	0	–	0.8	0	–	0.8	V
Input high voltage	V_{IH}	2.0	–	5.5	2.0	–	5.5	V
Ambient temperature	T_A	0	–	75	–55	–	+125	°C

Table 2 – AC CHARACTERISTICS

Parameter	Symbol	Typ	MB 7226RA/ RS-20		MB 7226RA/ RS-25/-25W		Typ	MB 7226RA -20L		MB 7226RA -25L/-25LW		Unit	Remarks
			Min	Max	Min	Max		Min	Max	Min	Max		
Address setup time	$t_S(A)$	20	30		35		35	50		60		ns	
Address hold time	$t_H(A)$	–5	0		0		–5	0		0		ns	
Clock access time	$t_A(CLK)$	15		20		25	15		20		25	ns	
Clock pulse width	$t_{WH}(CLK)$ $t_{WL}(CLK)$	10	20		20		10	20		20		ns	
Synchronous enable setup time	$t_S(\overline{E}_S)$	5	10		15		5	10		15		ns	
Synchronous enable hold time	$t_H(\overline{E}_S)$	0	5		5		0	5		5		ns	
Asynchronous initialize access time	$t_A(\overline{INIT}_A)$ $t_A(\overline{PRST}_A)$	17		25		25	17		25		25	ns	MB 7226RA
Asynchronous initialize recovery time	$t_R(\overline{INIT}_A)$ $t_R(\overline{PRST}_A)$	8	20		20		8	20		20		ns	MB 7226RA
Asynchronous initialize pulse width	$t_{WL}(\overline{INIT}_A)$ $t_{WL}(\overline{PRST}_A)$	12	20		20		12	20		20		ns	MB 7226RA
Synchronous initialize setup time	$t_S(\overline{INIT}_S)$ $t_S(\overline{PRST}_S)$	11	20		25		TBD	TBD		TBD		ns	MB 7226RS
Synchronous initialize hold time	$t_H(\overline{INIT}_S)$ $t_H(\overline{PRST}_S)$	–5	0		0		TBD	TBD		TBD		ns	MB 7226RS
Clock enable time	$t_{EN}(CLK)$	18		25		30	18		25		30	ns	
Asynchronous enable time	$t_{EN}(\overline{E}_A)$	15		25		30	15		25		30	ns	
Clock disable time*2	$t_{DIS}(CLK)$	18		25		30	18		25		30	ns	
Asynchronous disable time*2	$t_{DIS}(\overline{E}_A)$	11		25		30	11		25		30	ns	

Notes: *1 At $T_A = 25°C$ and $V_{CC} = 5.0V$.
*2 Measured at a point on the output waveform 0.5V from the active output level.

4

Table 3 — DC CHARACTERISTICS (Under Guaranteed Operating Conditions)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Input current		I_{IH}	V_{IH} = 5.5 V	–	–	40	μA
		I_{IL}	V_{IL} = 0.45 V	–	–	-250	μA
Input clamp voltage		V_{IC}	I_I = -18 mA	–	–	-1.2	V
Output low voltage		V_{OL}	I_{OL} = 10 mA	–	–	0.45	V
			I_{OL} = 16 mA	–	–	0.5	V
Output leakage current (Chip disabled)		I_{OIL}	V_O = 0.45 V	–	–	-40	μA
		I_{OIH}	V_O = 2.4 V	–	–	40	μA
Output high voltage*1		V_{OH}	I_{OH} = -2.4 mA	2.4	–	–	V
Output short-circuit current*1		I_{OS}	V_O = 0 V	-15	–	-60	mA
Power supply current	MB 7226RA/RS	I_{CC}	V_I = Open or 0 V		120	170	mA
	MB 7226RA-L				70	100	

Note: *1 Denotes guaranteed characteristics of the output high-level state when the chip is enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

Table 4 — TERMINAL CAPACITANCE (T_A = 25°C, V_{CC} = +5.0 V, VIN = +2.0 V, f = 1 MHz)

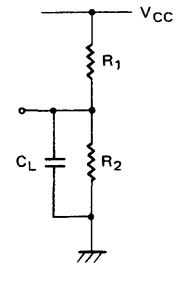
Parameter	Symbol	Typ.	Max.	Unit
Input terminal capacitance	C_{IN}	–	10	pF
Output terminal capacitance	C_{OUT}	–	15	pF

Fig. 6 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

LOAD CONDITION



R_1 ..... 300Ω
R_2 ..... 600Ω
C_L 50pF

2. FABRICATION TECHNOLOGY

2.1 Input/Output Circuits

The inputs use Schottky TTL circuitry to achieve a fast response time. A PNP transistor is used in the first stage to minimize switching current. Protection diodes are also included.

The three-state outputs (high, low; and high-impedance states) combine the advantages of totem-pole outputs (high noise immunity, fast rise time, ample line-driving capacity) and direct connection to bus-oriented systems. Schottky TTL circuitry is used for fast operation. A PNP transistor in the output circuit minimizes the load on the chip enable circuitry.

2.2 Memory Cells

The memory cells in the MB 7226 are of the junction-shorting type, using DEAP (Diffused Eutectic Aluminum Process) technology. They are initially all in the 0 (low voltage) state. In this state, the cell's programmable element, a PN diode, blocks current flow. During programming, the diode's junction is shorted, allowing it to conduct current, and permanently changing the cell's state to 1 (high).

By applying reverse current pulses to the diode's cathode, the temperature at the junction is raised. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and shorts the junction. The power dissipation at the junction immediately drops to less than one fifth, thus lowering the temperature. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

In the memory cell array, the word line islands are divided by IOP (Isolation by Oxide and Poly-silicon) passive isolation. Memory cells in the same island are divided by SVG (Shallow V-Groove) passive isolation. The vertically structured memory cells permit a high packing density.

4

3. PROGRAMMING

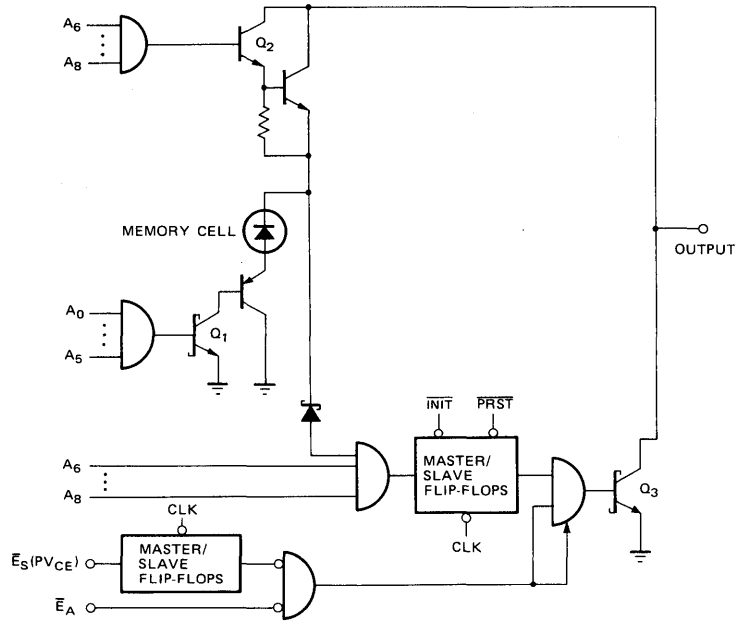
3.1 Overview (see Figure 7)

As shipped, all the bits in the MB 7226 are in the 0 (low) state. In programming, individual cells are addressed and a programming current applied, to change that bit's state to 1. Only one bit at a time can be programmed, because the internal decoding circuitry can only sink one unit of programming current at a time.

A data word is first selected, using the normal address inputs. The decoded address lines turn on transistors Q1 and Q2. When the PV_{CE} level is applied to the $\overline{E}_S$ input, the chip outputs are disabled, turning off transistor Q3. Programming pulses are applied to the output of a single bit, eventually shorting the diode attached to Q1. At this point, if the output is read, it will be in the 1 (high) state. Two additional programming pulses are then applied, to ensure reliability.

Initial data is programmed in the same way, except that the address inputs are kept low, and $\overline{INIT}$ is applied an init pulse, to select the initial data word rather than a PROM data word.

Fig. 7 – INTERNAL PROGRAMMING CIRCUIT



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3.2 Procedure

1) Apply power to the device (V_{CC} = 5 V, GND = 0 V).
2) Set $\overline{E}_A$ and $\overline{E}_S$ both low. Set $\overline{INIT}$ and $\overline{PRST}$ both high to select PROM data for programming, or set initialize inputs and address inputs low to select Initial data.
3) Select the desired bit. And in case of Initial data, apply an init pulse.
4) Apply a clock pulse.
5) Read the output to confirm that the desired bit is in fact 0. If not, go on to the next bit.
6) Raise the V_{CC} terminal to PV_{CC} (7 V).
7) Raise the $\overline{E}_S$ terminal to PV_{CE} (20 V).
8) Apply a clock pulse.
9) Apply a programming pulse (125 mA, 11 μs) to the output (Q_X) of the desired bit.
10) Return PV_{CC} to 5 V and PV_{CE} to 0 V. And in case of initial data, apply an init pulse.
11) Apply a clock pulse.
12) After a delay of t_{PR} (5 μs), read the output voltage V_O.
    a) If V_O is still low, repeat steps (6) through (12), allowing t_{CYC} (50 μs) for each cycle, up to 100 times.
    b) If V_O is high, apply two additional programming pulses, to ensure reliable retention.
13) If there are more bits to be programmed, repeat steps (3) through (12).

3.3 Liability

Fujitsu performs an extensive series of tests to ensure device performance before shipping. However, 100% programmability is not guaranteed. Furthermore, it is imperative that the programming specifications be rigorously adhered to in order to achieve a satisfactory programming yield.

Fujitsu will not accept responsibility for any device found defective if it was not programmed according to these specifications. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

Fig. 8(a) – PROGRAMMING TIMING CHART

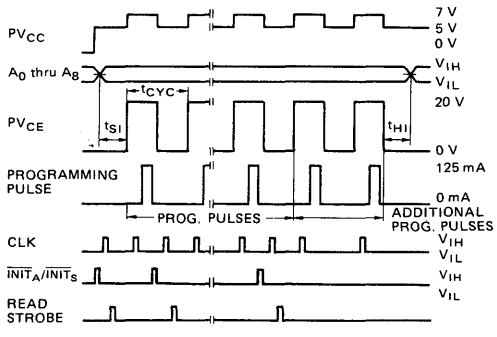

Fig. 8(b) – ONE DETAILED PROGRAMMING CYCLE

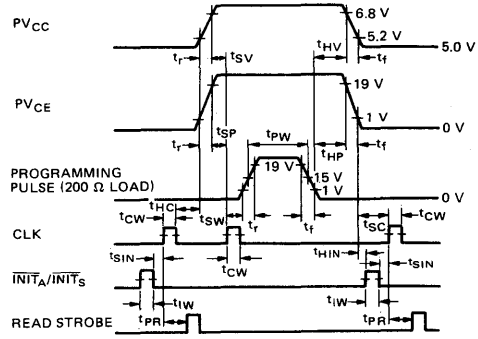

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Table 5 – PROGRAMMING SPECIFICATIONS, DC

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.25	V
Power-supply voltage	V_{CC}	4.75	5.0	5.25	V
Power-supply current	I_{CC}			200	mA
PV_{CC} power-supply voltage	PV_{CC}	6.7	7.0	7.3	V
PV_{CC} power-supply current	PI_{CC}			300	mA
Programming pulse current	I_{PRG}	120		130	mA
Programming pulse clamp voltage	V_{PRG}	20	20	22	V
PV_{CE} pulse voltage	PV_{CE}	20	20	22	V
PV_{CE} pulse clamp current	PI_{CE}	230		260	mA
PV_{AO} pulse voltage	PV_{AO}	10		22	V
PV_{AO} pulse clamp current	PI_{AO}	10			mA
Reference level for output high voltage	V_{REF}	1.0	1.5	2.4	V

Table 6 – PROGRAMMING SPECIFICATIONS, AC

Parameter	Symbol	Min.	Typ.	Max.	Unit
Programming pulse cycle time	t_{CYC}	40	50	60	μs
Programming pulse width	t_{PW}	10	11	12	μs
Clock pulse width	t_{CW}	0.5			μs
Programming pulse rise time	t_r			2	μs
PV_{CC} pulse rise time	t_r			2	μs
PV_{CE} pulse rise time	t_r			2	μs
Programming pulse fall time	t_f			2	μs
PV_{CC} pulse fall time	t_f			2	μs
PV_{CE} pulse fall time	t_f			2	μs
Input setup time	t_{SI}	2			μs
PV_{CC} pulse setup time	t_{SV}	2			μs
PV_{CE} pulse setup time	t_{SP}	2			μs
Programming pulse setup time	t_{SW}	2			μs
Input hold time	t_{HI}	2			μs
PV_{CC} pulse hold time	t_{HV}	2			μs
PV_{CE} pulse hold time	t_{HP}	2			μs
Clock pulse setup time	t_{SC}	5			μs
Clock pulse hold time	t_{HC}	5			μs
Init pulse setup time	t_{SIN}	0.5			μs
Init pulse hold time	t_{HIN}	2			μs
Init pulse width	t_{IW}	0.5			μs
Clock pulse rising edge to read strobe time	t_{PR}	5			μs
Number of programming pulses	n			100	pulses
Programming time/bit		120		6120	μs/bit
Number of additional programming pulses		2		2	pulses

TYPICAL CHARACTERISTICS CURVES

DC CHARACTERISTICS

Fig. 9 – I_{IN} INPUT CURRENT vs. V_{IN} INPUT VOLTAGE

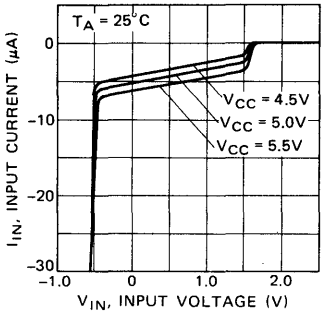


Fig. 10 – I_{OH} OUTPUT HIGH CURRENT vs. V_{OH} OUTPUT HIGH VOLTAGE

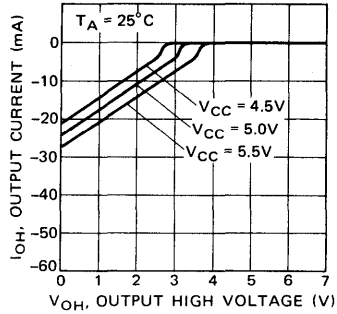
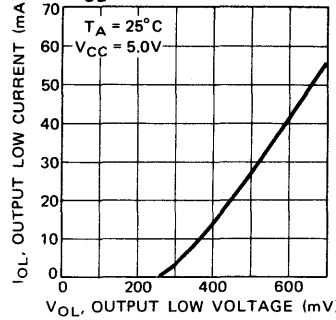


Fig. 11 – I_{OL} OUTPUT LOW CURRENT vs. V_{OL} OUTPUT LOW VOLTAGE



AC CHARACTERISTICS

Fig. 12 – t_S(A) ADDRESS SETUP TIME vs. AMBIENT TEMPERATURE

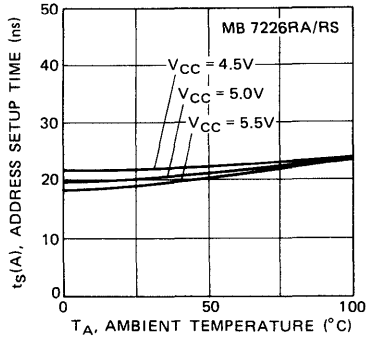


Fig. 13 – t_S(A) ADDRESS SETUP TIME vs AMBIENT TEMPERATURE

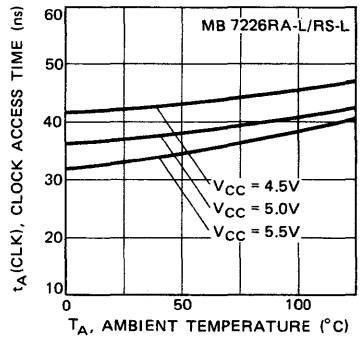


Fig. 14 – t_H(A) ADDRESS HOLD TIME vs. AMBIENT TEMPERATURE

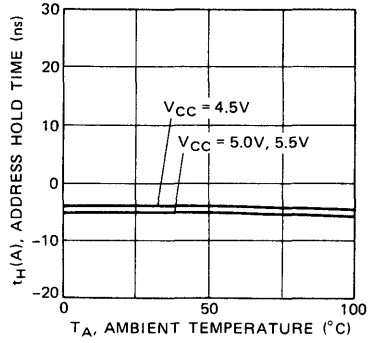


Fig. 15 – t_A(CLK) CLOCK ACCESS TIME vs. AMBIENT TEMPERATURE

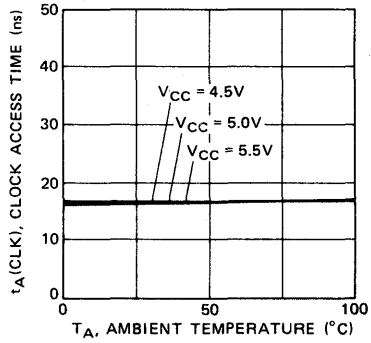


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Fig. 16 – t_{WH}(CLK) AND t_{WL}(CLK) CLOCK PULSE WIDTH vs. AMBIENT TEMPERATURE

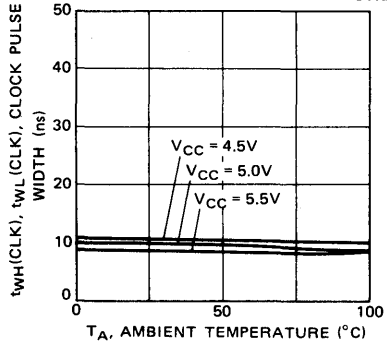


Fig. 17 – t_S ($\overline{E}_S$) SYNCHRONOUS ENABLE SETUP TIME vs. AMBIENT TEMPERATURE

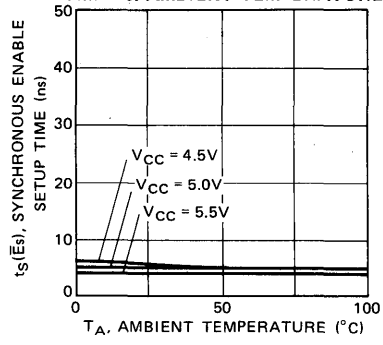


Fig. 18 – t_H ($\overline{E}_S$) SYNCHRONOUS ENABLE HOLD TIME vs. AMBIENT TEMPERATURE

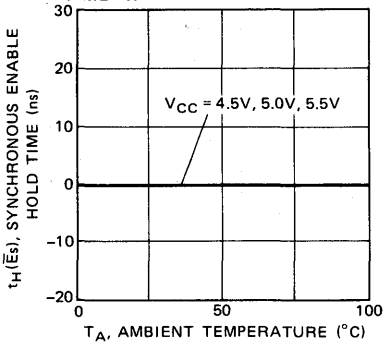


Fig. 19 – t_A ($\overline{INIT}_A$) AND t_A ($\overline{PRST}_A$) ASYNCHRONOUS INITIALIZE ACCESS TIME vs. AMBIENT TEMEPRATURE

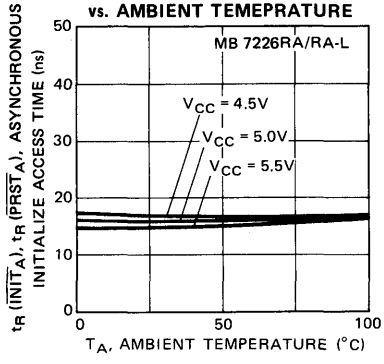


Fig. 20 – t_R ($\overline{INIT}_A$) AND t_R ($\overline{PRST}_A$) ASYNCHRONOUS INITIALIZE RECOVERY TIME vs. AMBIENT TEMPERATURE

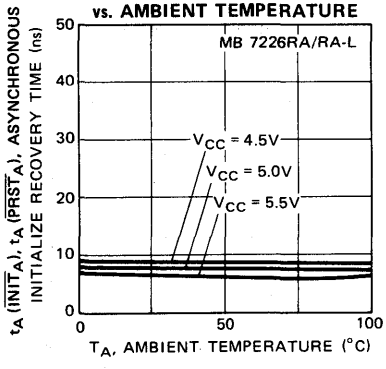


Fig. 21 – t_{WL} ($\overline{INIT}_A$) AND t_{WL} ($\overline{PRST}_A$) ASYNCHRONOUS INITIALIZE PULSE WIDTH vs. AMBIENT TEMPERATURE

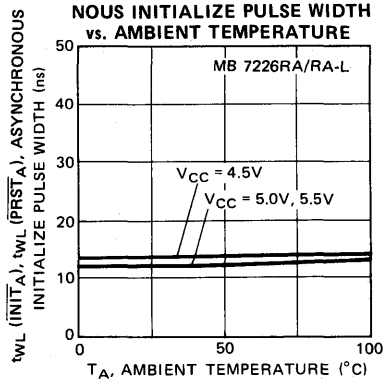


Fig. 22 – t_S ($\overline{INIT}_S$) AND t_S ($\overline{PRST}_S$) ASYNCHRONOUS INITIALIZE SETUP TIME vs. AMBIENT TEMPERATURE

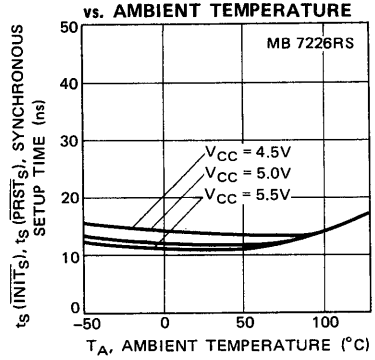


Fig. 23 – t_H ($\overline{INIT}_S$) AND t_H ($\overline{PRST}_S$) SYNCHRONOUS INITIALIZE HOLD TIME vs. AMBIENT TEMPERATURE

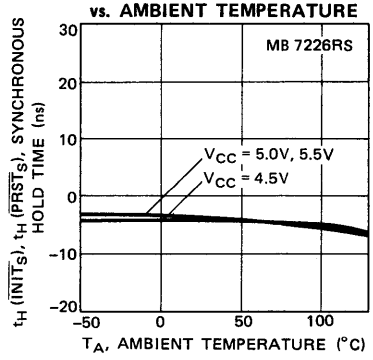


Fig. 24 – t_{EN}(CLK) CLOCK ENABLE TIME vs. AMBIENT TEMPERATURE

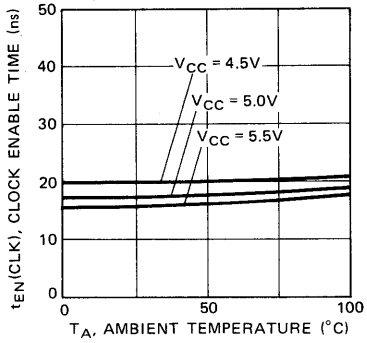
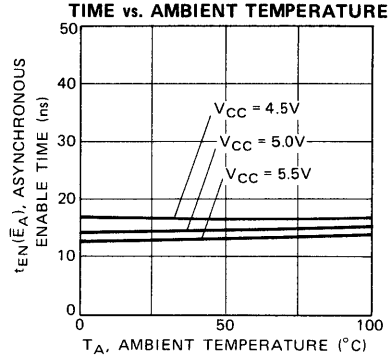


Fig. 25 – t_{EN}($\overline{E}_A$) ASYNCHRONOUS ENABLE TIME vs. AMBIENT TEMPERATURE



26 – t_{DIS}(CLK) CLOCK DISABLE TIME vs. AMBIENT TEMPERATURE

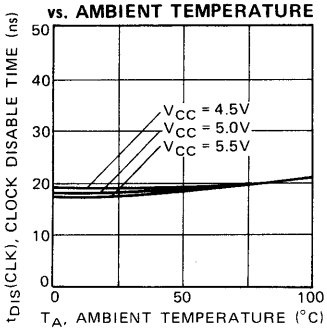


Fig. 27 – t_{DIS}($\overline{E}_A$) ASYNCHRONOUS DISABLE TIME vs. AMBIENT TEMPERATURE

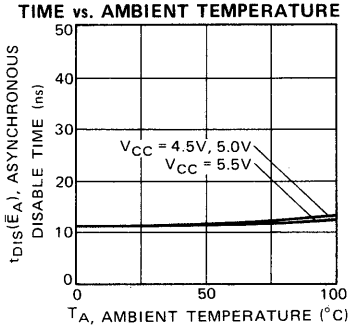
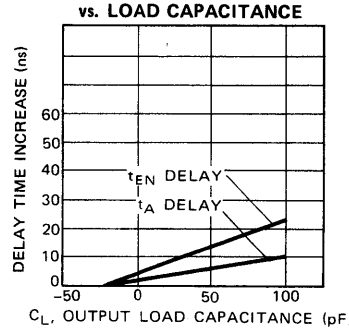


Fig. 28 – DELAY TIME INCREASE vs. LOAD CAPACITANCE



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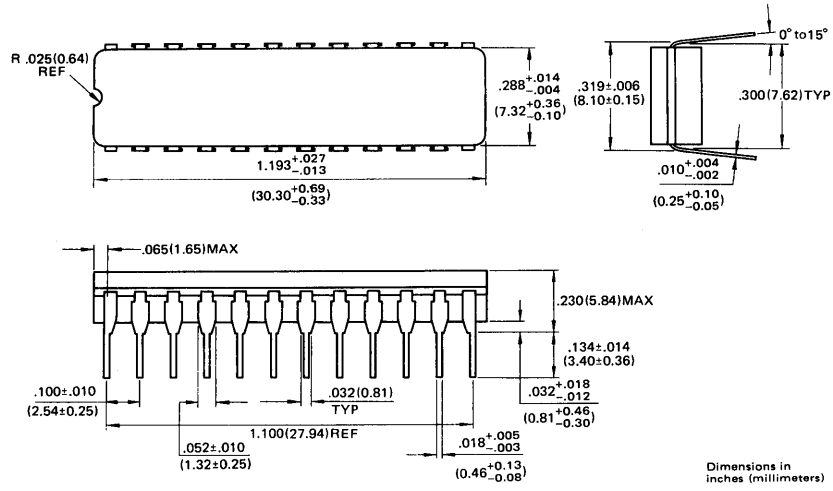
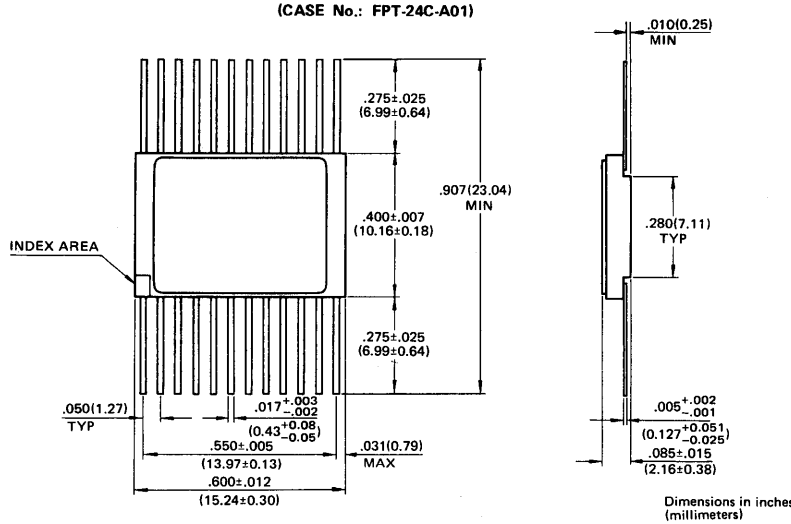
PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C04)

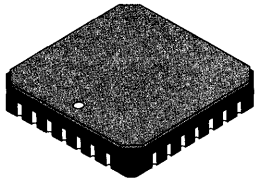


Dimensions in inches (millimeters)

24-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(CASE No.: FPT-24C-A01)

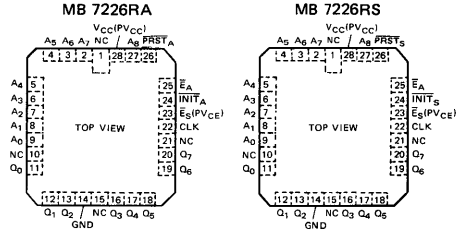


Dimensions in inches (millimeters)



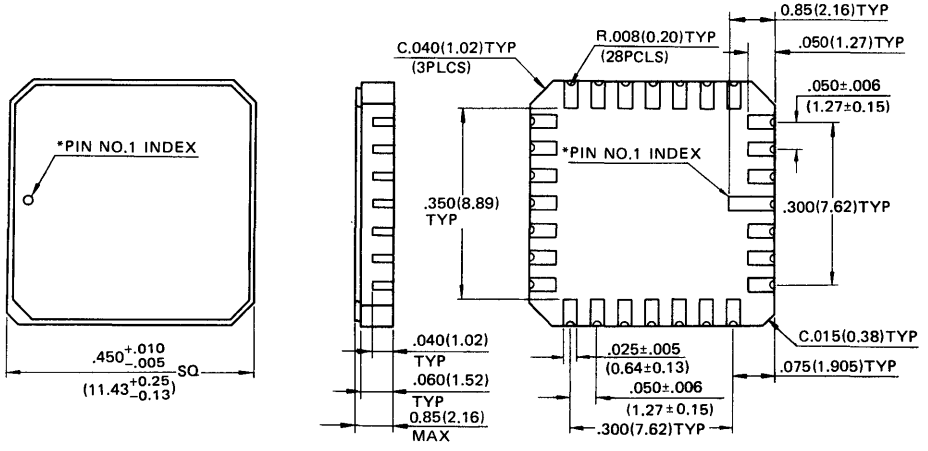
LCC-28C-A01

PAD CONFIGURATION



(LCC-28C-A01) (LCC-28C-A01)

28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A01)



*Shape of Pin No.1 index: Subject to change without notice

Dimensions in
inches (millimeters)

4

FUJITSU

SCHOTTKY 8192-BIT REGISTERED OUTPUT PROM

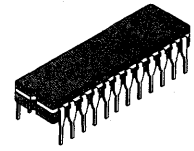
MB 7232RA-20/-25
MB 7232RA-25W
MB 7232RS-20/-25
MB 7232RS-25W

June 1987
Edition 2.0

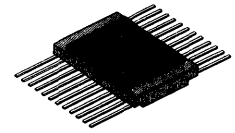
SCHOTTKY 8,192-BIT REGISTERED OUTPUT PROM

The Fujitsu MB 7232 is an 8 Kbit bipolar programmable read-only memory circuit, with registered output (output data is latched in a register). The output register can be initialized to a field programmable value, either synchronously (MB 7232RS) or asynchronously (MB 7232RA). Three-state outputs can also be enabled either synchronously or asnchronously, in either model. DEAP memory cells are used to provide fast and reliable programming.

- 1024 word x 8 bit PROM data organization
- Fast clock access time:
  20 ns (MB 7232RA/RS-20)
  25 ns (MB 7232RA/RS-25/-25W)
- Register can be initialized synchronously (MB 7232RS) or asynchronously (MB 7232RA).
- Single +5 V operation
- TTL-compatible I/O
- Low current inputs
- Three-state outputs
- Outputs can be enabled either synchronously or asynchronously.
- Outputs are kept disabled on power-up.
- DEAP (diffused eutectic aluminum process) memory cells are reliable and easily programmed.
- Test cells allow extensive testing of AC, DC, and programming characteristics before shipment.



CERAMIC PACKAGE
DIP-24C-C04

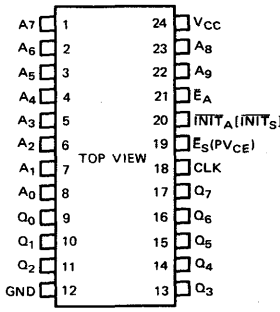


CERAMIC PACKAGE
FPT-24C-A01

LCC-28C-A01: See Page 15

4

PIN ASSIGNMENT



Symbols in blankets : MB 7232RS

LCC PAD CONFIGURATION: See Page 15

ABSOLUTE MAXIMUM RATINGS

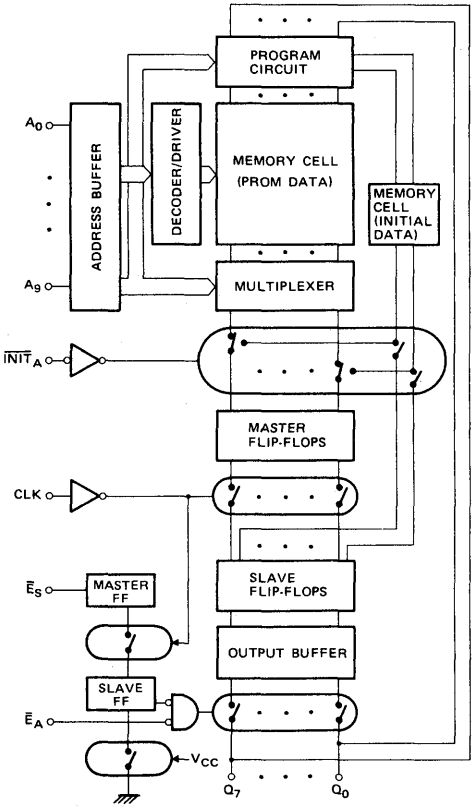
Parameter	Symbol	Rating	Unit
Power-supply voltage	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-1.5 to +5.5	V
Input current	I_{IN}	-20	mA
Output current	I_{OUT}	+100	mA
Power-supply voltage (during programming)	V_{CCP}	-0.5 to +7.5	V
Input voltage (during programming)	V_{IPRG}	+22.5	V
Input current (during programming)	I_{IPRG}	+270	mA
Output voltage (during programming)	V_{OPRG}	-0.5 to +22.5	V
Output current (during programming)	I_{OPRG}	+150	mA
Storage temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

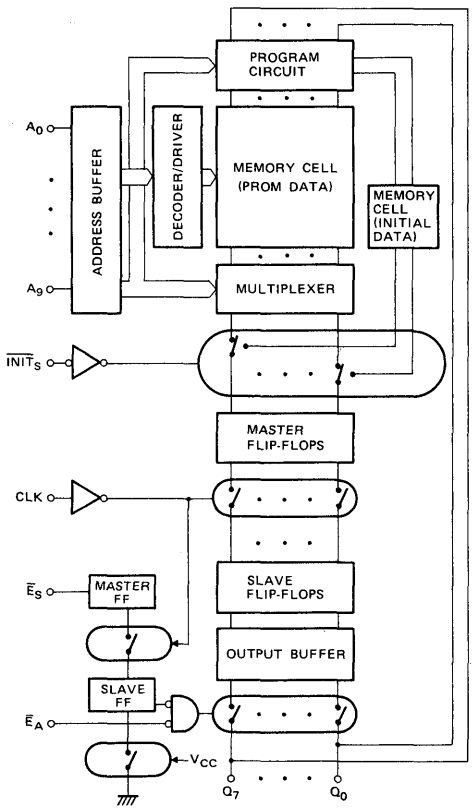
4

Fig. 1 – MB 7232RA BLOCK DIAGRAM



Input				Output	Operating mode	Remarks
$\overline{INIT}_A$	CLK	$\overline{E}_A$	$\overline{E}_S$			
L	X	L	L	INITIAL DATA	INITIALIZE	PRO-GRAMMABLE
H	↑	L	L	PROM DATA	LOAD REGISTER	
X	↑	X	H	Z	CHIP DISABLE	
X	X	H	X	Z	CHIP DISABLE	

Fig. 2 – MB 7232RS BLOCK DIAGRAM



Input				Output	Operating mode	Remarks
$\overline{INIT}_S$	CLK	$\overline{E}_A$	$\overline{E}_S$			
L	↑	L	L	INITIAL DATA	INITIALIZE	PRO-GRAMMABLE
H	↑	L	L	PROM DATA	LOAD REGISTER	
X	↑	X	H	Z	CHIP DISABLE	
X	X	H	X	Z	CHIP DISABLE	

1. READ OPERATIONS

1.1 Overview (see Figures 1 and 2)

During PROM reads, data is shifted through a register latch, made of master-slave flip-flops, before appearing at the outputs. When a new address is applied to the address inputs (A_0 through A_9), new data appears in the master register. At the next clock pulse this data is transferred to the slave register.

Both of the chip enable inputs must be low in order for the data in the slave register to appear at the outputs (Q_0 through Q_7). If the $\overline{E}_S$ input is already low, bringing the asynchronous chip enable ($\overline{E}_A$) low immediately enables the outputs. With $\overline{E}_A$ low, bringing the synchronous chip enable ($\overline{E}_S$)low enables the outputs at the next clock pulse. Likewise, when the outputs are enabled, bringing either input high will cause them to be disabled, in other words put into a high-impedance state. When $\overline{E}_A$ is brought high, the outputs are immediately disabled, whereas when $\overline{E}_S$ is brought high, they are disabled after the next clock pulse.

If the $\overline{INIT}$ input is brought low the register latch is loaded with a field-programmable initial value, rather than with PROM data. In the MB 7232RS the master register is loaded immediately, and the contents are transferred to the slave register at the next clock pulse. In the MB 7232RA both the master and slave registers are loaded immediately.

1.2 Timing Considerations

a) PROM Data Read (see Figure 3)

After an address change, address setup time $t_S(A)$ must elapse before the master register contains valid new PROM data. The clock must then rise, within address hold time $t_H(A)$, to shift the data to the slave register. The data will appear at the outputs within clock access time $t_A(CLK)$ after the rising edge of the clock, if the outputs had been previously enabled.

If the outputs were disabled when the data was shifted, and are subsequently enabled by bringing $\overline{E}_A$ low, asynchronous chip enable time $t_{EN}(\overline{E}_A)$ must elapse before the data appears at the outputs.

If $\overline{E}_S$ is brought low to enable the outputs, clock enable time $t_{EN}(CLK)$ must elapse after the rising edge of the next clock. During this time the data from the master register is shifted to the slave register and appears at the outputs.

In the MB 7232RA, when the registers have been initialized by $\overline{INIT}$, and $\overline{INIT}$ is then brought high to select PROM data, asynchronous initialize recovery time $t_R(\overline{INIT}_A)$ must elapse after the clock signal is applied.

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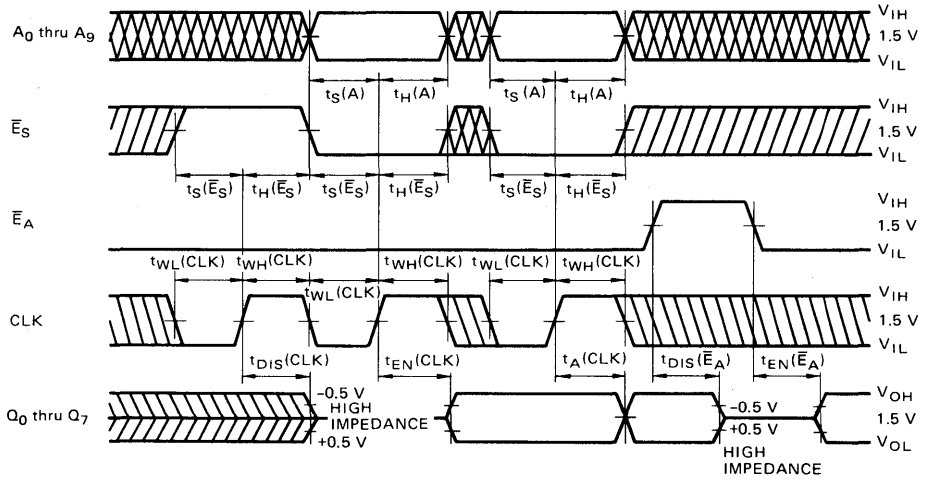
Fig. 3 – PROM DATA READ TIMING *1



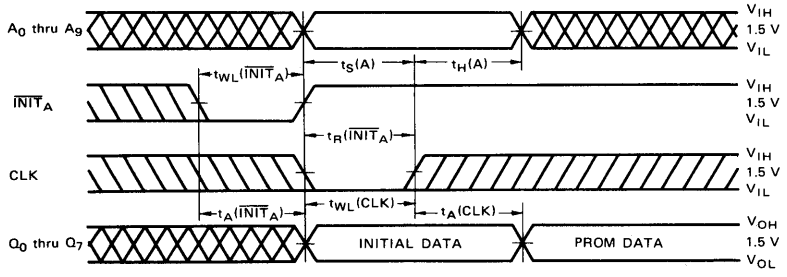
Note: *1 $\overline{INIT}$ is high.

b) Initial Data Read (see Figures 4 and 5)

In the MB 7232RA, after the $\overline{INIT}$ input is brought low, asynchronous initialize access time $t_A(\overline{INIT}_A)$ must elapse before the initial data appears at the outpus.

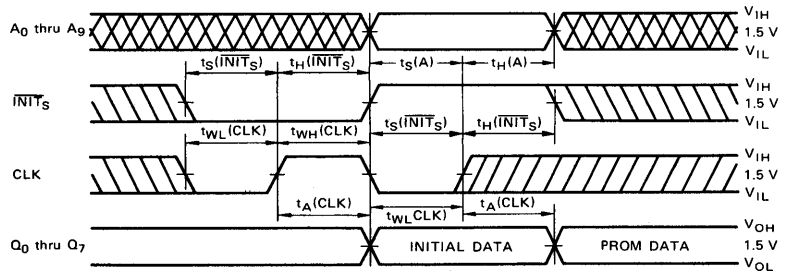
In the MB 7232RS, after the $\overline{INIT}$ input is brought low, synchronous initialize access time $t_A(\overline{INIT}_S)$ must elapse before valid initial data appears in the master register. It is then shifted and output in the same manner as PROM data.

Fig. 4 – ASYNCHRONOUS INITIAL DATA READ TIMING (MB 7232RA) *1



Notes: *1 $\overline{E}_A$, $\overline{E}_S$ input are low.
*2 ⊠ Don't care.

Fig. 5 – Synchronous Initial Data Read Timing (MB 7232RS) *1



Notes: *1 $\overline{E}_A$, $\overline{E}_S$ input are low.
*2 ⊠ Don't care.

DATA READ SPECIFICATIONS

Table 1 – Guaranteed Operating Conditions

Parameter	Symbol	MB 7232RA-20/-25 MB 7232RS-20/-25			MB 7232RA-25W MB 7232RS-25W			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Power-supply voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
Input low voltage	V_{IL}	0	–	0.8	0	–	0.8	V
Input high voltage	V_{IH}	2.0	–	5.5	2.0	–	5.5	V
Ambient temperature	T_A	0	–	75	-55	–	+125	°C

Table 2 – AC CHARACTERISTICS

Parameter	Symbol	Typ.	MB 7232RA-20 MB 7232RS-20		MB 7232RA-25/-25W MB 7232RS-25/-25W		Unit	Remarks
			Min.	Max.	Min.	Max.		
Address setup time	t_S(A)	20	30		35		ns	
Address hold time	t_H(A)	–5	0		0		ns	
Clock access time	t_A(CLK)	15		20		25	ns	
Clock pulse width	t_{WH}(CLK) / t_{WL}(CLK)	10	20		20		ns	
Synchronous enable setup time	$t_S(\overline{E}_S)$	5	10		15		ns	
Synchronous enable hold time	$t_H(\overline{E}_S)$	0	5		5		ns	
Asynchronous initialize access time	$t_A(\overline{INIT}_A)$	20		30		30	ns	MB 7232RA
Asynchronous initialize recovery time	$t_R(\overline{INIT}_A)$	11	20		20		ns	MB 7232RA
Asynchronous initialize pulse width	$t_{WL}(\overline{INIT}_A)$	13	20		20		ns	MB 7232RA
Synchronous initialize setup time	$t_S(\overline{INIT}_S)$	11	20		20		ns	MB 7232RS
Synchronous initialize hold time	$t_H(\overline{INIT}_S)$	–5	0		0		ns	MB 7232RS
Clock enable time	t_{EN}(CLK)	18		25		30	ns	
Asynchronous enable time	$t_{EN}(\overline{E}_A)$	15		25		30	ns	
Clock disable time*2	t_{DIS}(CLK)	18		25		30	ns	
Asynchronous disable time*2	$t_{DIS}(\overline{E}_A)$	11		25		30	ns	

Notes: *1 At T_A = 25°C and V_{CC} = 5.0 V.
*2 Measured at a point on the output waveform 0.5 V from the active output level.

4

Table 3 — DC CHARACTERISTICS (Under Guaranteed Operating Conditions)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input current	I_{IH}	V_{IH} = 5.5 V	–	–	40	μA
	I_{IL}	V_{IL} = 0.45 V	–	–	-250	μA
Input clamp voltage	V_{IC}	I_I = -18 mA	–	–	-1.2	V
Output low voltage	V_{OL}	I_{OL} = 10 mA	–	–	0.45	V
		I_{OL} = 16 mA	–	–	0.5	V
Output leakage current (Chip disabled)	I_{OIL}	V_O = 0.45 V	–	–	-40	μA
	I_{OIH}	V_O = 2.4 V	–	–	40	μA
Output high voltage*1	V_{OH}	I_{OH} = -2.4 mA	2.4	–	–	V
Output short-circuit current*1	I_{OS}	V_O = 0 V	-15	–	-60	mA
Power supply current	I_{CC}	V_I = Open or 0 V		140	185	mA

Note: *1 Denotes guaranteed characteristics of the output high-level state when the chip is enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

Table 4 — TERMINAL CAPACITANCE (T_A = 25°C, V_{CC} = +5.0 V, VIN = +2.0 V, f = 1 MHz)

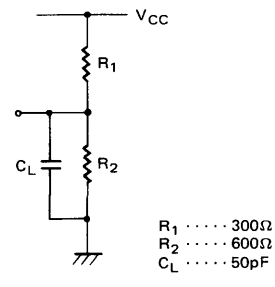
Parameter	Symbol	Typ.	Max.	Unit
Input terminal capacitance	C_{IN}	–	10	pF
Output terminal capacitance	C_{OUT}	–	15	pF

Fig. 6 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5ns from 1V to 2V
Frequency 1MHz

LOAD CONDITION



R_1 ..... 300Ω
R_2 ..... 600Ω
C_L 50pF

2. FABRICATION TECHNOLOGY

2.1 Input/Output Circuits

The inputs use Schottky TTL circuitry to achieve a fast response time. A PNP transistor is used in the first stage to minimize switching current. Protection diodes are also included.

The three-state outputs (high, low, and high-impedance states) combine the advantages of totem-pole outputs (high noise immunity, fast rise time, ample line-driving capacity) and direct connection to bus-oriented system. Schottky TTL circuitry is used for fast operation. A PNP transistor in the output circuit minimizes the load on the chip enable circuitry.

2.2 Memory Cells

The memory cells in the MB 7232 are of the junction-shorting type, using DEAP (Diffused Euteotic Aluminum Process) technology. They are initially all in the 0 (low voltage) state. In this state, the cell's programmable element, a PN diode, blocks current flow. During programming, the diode's junction is shorted, allowing it to conduct current, and permanently changing the cell's state to 1 (high).

By applying reverse current pulses to the diode's cathode, the temperature at the junction is raised. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and shorts the junction. The power dissipation at the junction immediately drops to less than one fifth, thus lowering the temperature. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

In the memory cell array, the word line islands are divided by IOP (Isolation by Oxide and Poly-silicon) passive isolation. Memory cells in the same island are divided by SVG (Shallow V-Groove) passive isolation. The vertically structured memory cells permit a high packing density.

4

3. PROGRAMMING

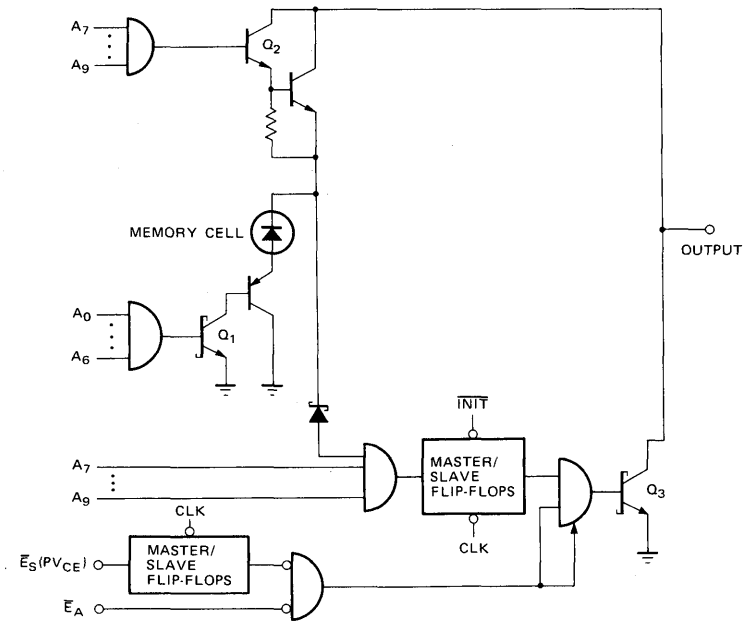
3.1 Overview (see Figure 6)

As shipped, all the bits in the MB 7232 are in the 0 (low) state. In programming, individual cells are addressed and a programming current applied, to change that bit's state to 1. Only one bit at a time can be programmed, because the internal decoding circuitry can only sink one unit of programming current at a time.

The word containing the desired bit is first selected, using the normal address inputs. The decoded address lines turn on transistors Q_1 and Q_2. When the PV_{CE} level is applied to the $\overline{E}_S$ input, the chip outputs are disabled, turning off transistor Q_3. Programming pulses are applied to the output of the desired bit, eventually fusing the diode attached to Q_1. At this point, if the output is read, it will be in the 1 (high) state. Two additional programming pulses are then applied, to ensure reliability.

Initial data is programmed in the same way, except that the address inputs are kept low, and $\overline{INIT}$ is applied an init pulse, to select the initial data word rather than a PROM data word.

Fig. 7 – PROGRAMMABLE MEMORY CELL



3.2 Procedure

1) Apply power to the device (V_{CC} = 5 V, GND = 0 V).
2) Set $\overline{E_A}$ and $\overline{E_S}$ both low. Set $\overline{INIT}$ input high to select PROM data for programming, or set initialize inputs and address inputs low to select initial data.
3) Select the desired bit.
4) Apply a clock pulse.
5) Read the output to confirm that the desired bit is in fact 0. If not, go on to the next bit.
6) Raise the V_{CC} terminal to PV_{CC} (7 V).
7) Raise the $\overline{E_S}$ terminal to PV_{CE} (20 V).
8) Apply a clock pulse.
9) Apply a programming pulse (125 mA, 11 μs) to the output (Q_X) of the desired bit.
10) Return PV_{CC} to 5 V and PV_{CE} to 0 V. And in case of initial data, apply an init pulse.
11) Apply a clock pulse.
12) After a delay of t_{PR} (5 μs), read the output voltage V_O.
    a) If V_O is still low, repeat steps (6) through (12), allowing t_{CYC} (50 μs) for each cycle, up to 100 times.
    b) If V_O is high, apply two additional programming pulses, to ensure reliable retention.
13) If there are more bits to be programmed, repeat steps (3) through (12).

3.3 Liability

Fujitsu performs an extensive series of tests to ensure device performance before shipping. However, 100% programmability is not guaranteed. Furthermore, it is imperative that the programming specifications be rigorously adhered to in order to achieve a satisfactory programming yield.

Fujitsu will not accept responsibility for any device found defective if it was not programmed according to these specifications. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

Fig. 8 a) – PROGRAMMING TIMING CHART

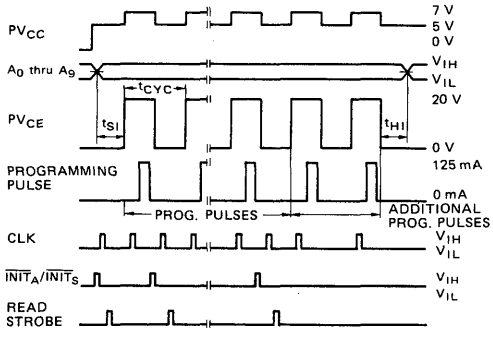


Fig. 8 b) – ONE DETAILED PROGRAMMING CYCLE

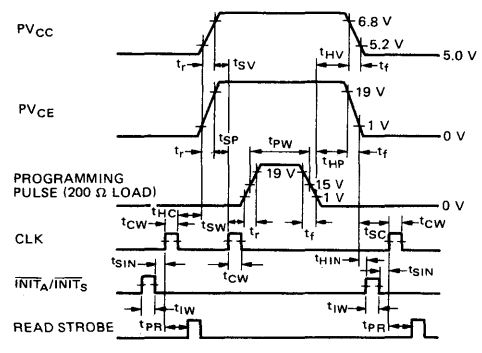


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Table 5 – PROGRAMMING SPECIFICATIONS, DC

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.25	V
Power-supply voltage	V_{CC}	4.75	5.0	5.25	V
Power-supply current	I_{CC}			200	mA
PV_{CC} power-supply voltage	PV_{CC}	6.7	7.0	7.3	V
PV_{CC} power-supply current	PI_{CC}			300	mA
Programming pulse current	I_{PRG}	120		130	mA
Programming pulse clamp voltage	V_{PRG}	20	20	22	V
PV_{CE} pulse voltage	PV_{CE}	20	20	22	V
PV_{CE} pulse clamp current	PI_{CE}	230		260	mA
PV_{AO} pulse voltage	PV_{AO}	10		22	V
PV_{AO} pulse clamp current	PI_{AO}	10			mA
Reference level for output high voltage	V_{REF}	1.0	1.5	2.4	V

Table 6 – PROGRAMMING SPECIFICATIONS, AC

Parameter	Symbol	Min.	Typ.	Max.	Unit
Programming pulse cycle time	t_{CYC}	40	50	60	μs
Programming pulse width	t_{PW}	10	11	12	μs
Clock pulse width	t_{CW}	0.5			μs
Programming pulse rise time	t_r			2	μs
PV_{CC} pulse rise time	t_r			2	μs
PV_{CE} pulse rise time	t_r			2	μs
Programming pulse fall time	t_f			2	μs
PV_{CC} pulse fall time	t_f			2	μs
PV_{CE} pulse fall time	t_f			2	μs
Input setup time	t_{SI}	2			μs
PV_{CC} pulse setup time	t_{SV}	2			μs
PV_{CE} pulse setup time	t_{SP}	2			μs
Programming pulse setup time	t_{SW}	2			μs
Input hold time	t_{HI}	2			μs
PV_{CC} pulse hold time	t_{HV}	2			μs
PV_{CE} pulse hold time	t_{HP}	2			μs
Clock pulse setup time	t_{SC}	5			μs
Clock pulse hold time	t_{HC}	5			μs
Init pulse setup time	t_{SIN}	0.5			μs
Init pulse hold time	t_{HIN}	2			μs
Init pulse width	t_{IW}	0.5			μs
Clock pulse rising edge to read strobe time	t_{PR}	5			μs
Number of programming pulses	n			100	pulses
Programming time/bit		120		6120	μs/bit
Number of additional programming pulses		2		2	pulses

TYPICAL CHARACTERISTICS CURVES

DC CHARACTERISTICS

Fig. 9 – I_{IN} INPUT CURRENT vs. V_{IN} INPUT VOLTAGE

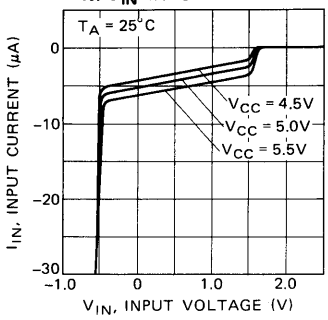


Fig. 10 – I_{OH} OUTPUT HIGH CURRENT vs. V_{OH} OUTPUT HIGH VOLTAGE

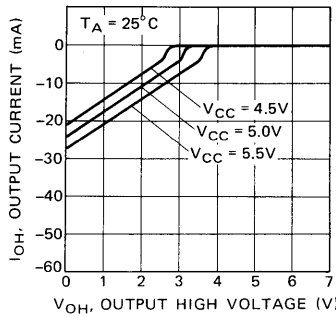
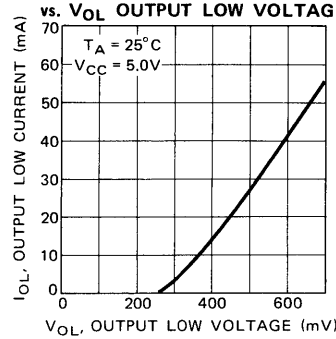


Fig. 11 – I_{OL} OUTPUT LOW CURRENT vs. V_{OL} OUTPUT LOW VOLTAGE



AC CHARACTERISTICS

Fig. 12 – t_S(A) ADDRESS SETUP TIME vs. AMBIENT TEMPERATURE

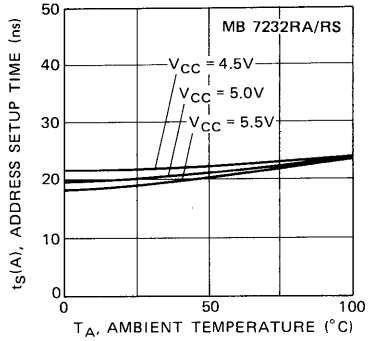


Fig. 13 – t_H(A) ADDRESS HOLD TIME vs. AMBIENT TEMPERATURE

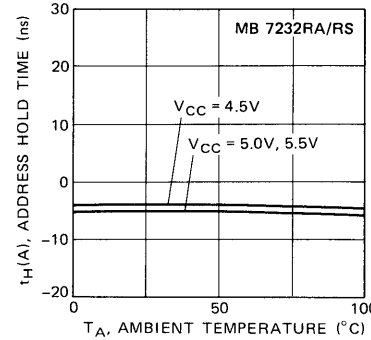


Fig. 14 – t_A(CLK) CLOCK ACCESS TIME vs. AMBIENT TEMPERATURE

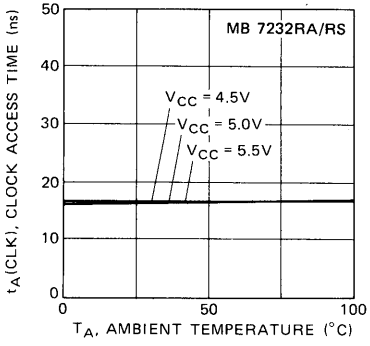


Fig. 15 – t_{WH}(CLK) AND t_{WL}(CLK) CLOCK PULSE WIDTH vs. AMBIENT TEMPERATURE

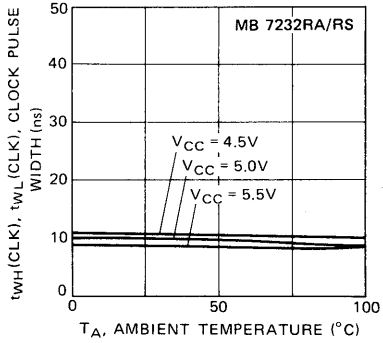


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Fig. 16 – t_S ($\overline{E_S}$) SYNCHRONOUS ENABLE SETUP TIME vs. AMBIENT TEMPERATURE

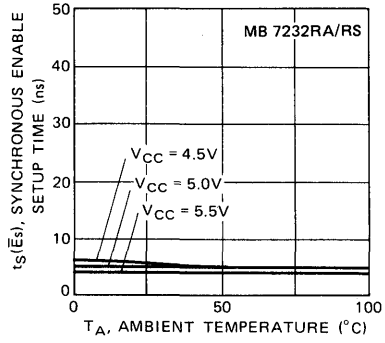


Fig. 17 – t_H ($\overline{E_S}$) SYNCHRONOUS ENABLE HOLD TIME vs. AMBIENT TEMPERATURE

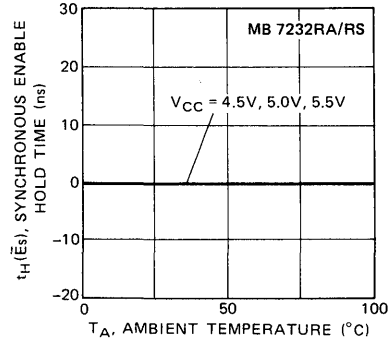


Fig. 18–t_A ($\overline{INIT_A}$) ASYNCHRONOUS INITIALIZE ACCESS TIME vs. AMBIENT TEMPERATURE

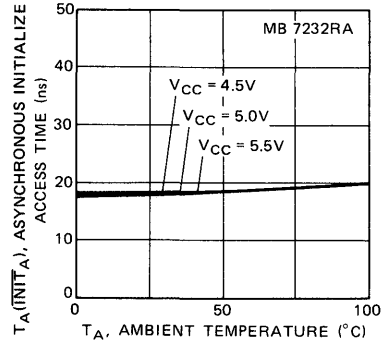


Fig. 19–t_R ($\overline{INIT_A}$) ASYNCHRONOUS INITIALIZE RECOVERY TIME vs. AMBIENT TEMPERATURE

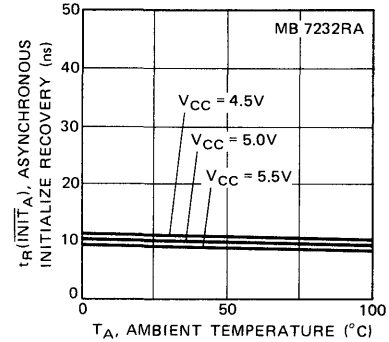


Fig. 20–t_{WL} ($\overline{INIT_A}$) ASYNCHRONOUS INITIALIZE PULSE WIDTH vs. AMBIENT TEMPERATURE

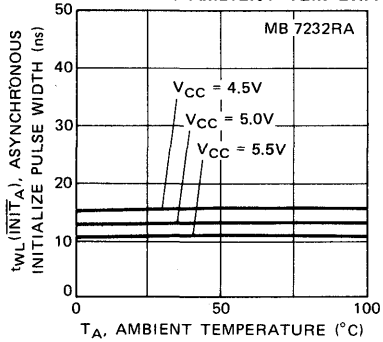


Fig. 21 – t_S ($\overline{INIT_S}$) SYNCHRONOUS INTIALIZE SETUP TIME vs. AMBIENT TEMPERATURE

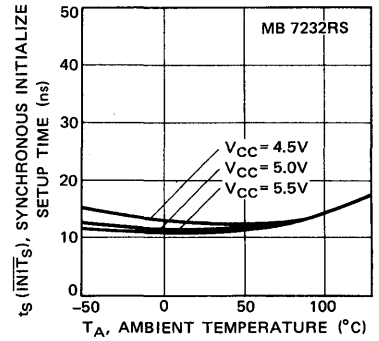


Fig. 22 – t_H ($\overline{INIT_S}$) SYNCHRONOUS INITIALIZE HOLD TIME vs. AMBIENT TEMPERATURE

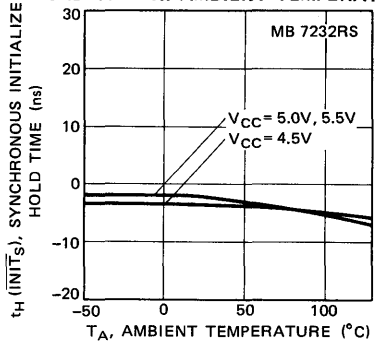


Fig. 23 – t_{EN}(CLK) CLOCK ENABLE TIME vs. AMBIENT TEMPERATURE

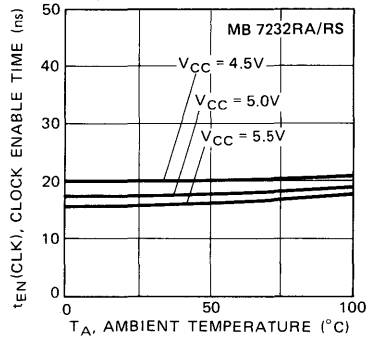


Fig. 24 – t_{EN}($\overline{E}_A$) ASYNCHRONOUS ENABLE TIME vs. AMBIENT TEMPERATURE

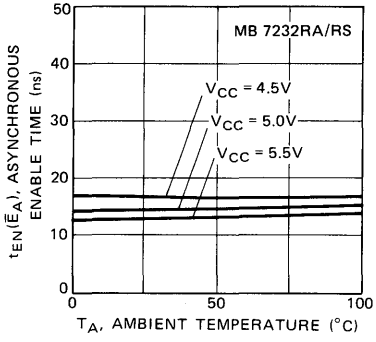


Fig. 25 – t_{DIS}(CLK) CLOCK DISABLE TIME vs. AMBIENT TEMPERATURE

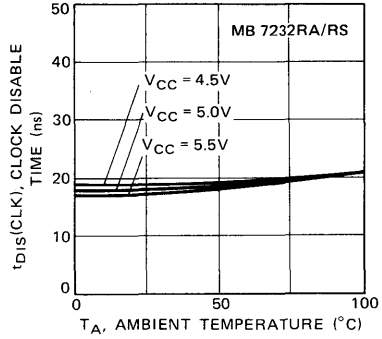


Fig. 26 – t_{DIS}($\overline{E}_A$) ASYNCHRONOUS DISABLE TIME vs. AMBIENT TEMPERATURE

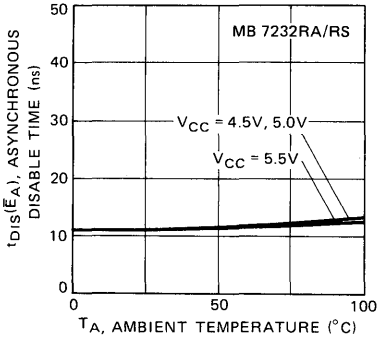
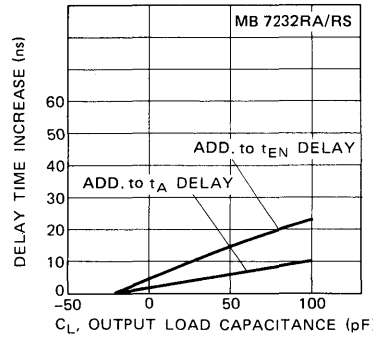


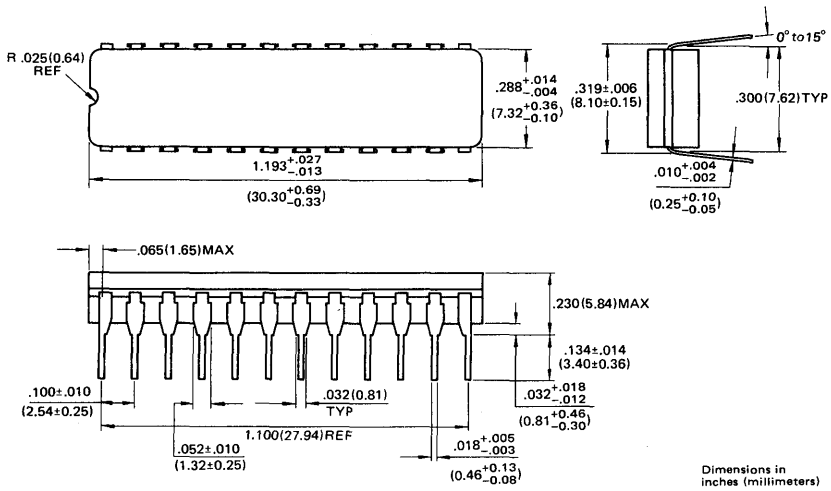
Fig. 27 – DELAY TIME INCREASE vs. LOAD CAPACITANCE



4

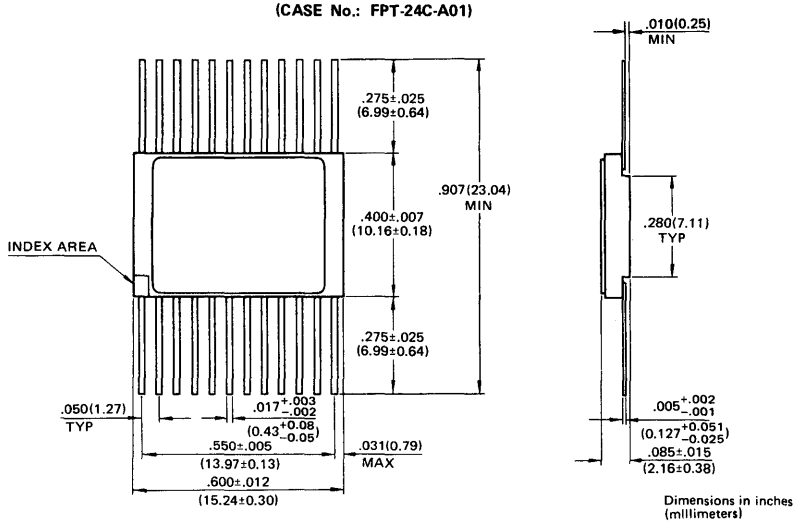
PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C04)

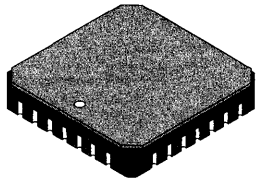


Dimensions in inches (millimeters)

24-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(CASE No.: FPT-24C-A01)

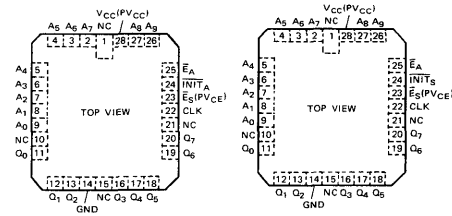


Dimensions in inches (millimeters)



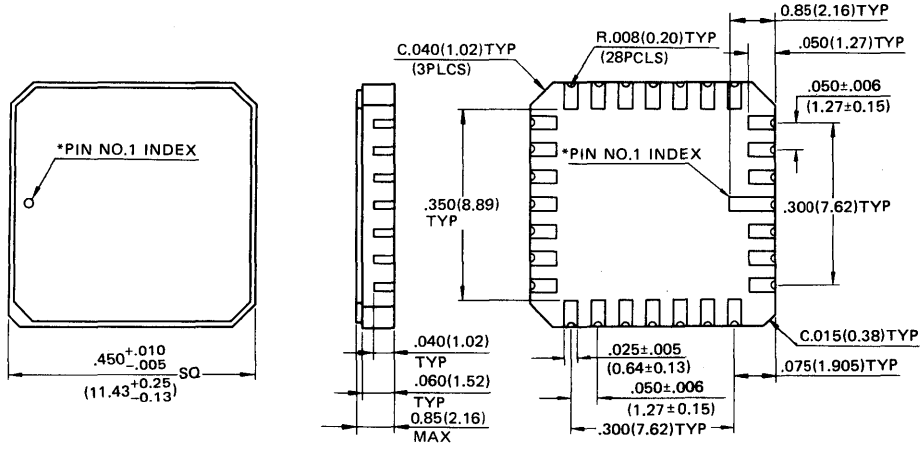
LCC-28C-A01

PAD CONFIGULATION



(LCC-28C-A01) (LCC-28C-A01)

28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A01)



*Shape of Pin No.1 index: Subject to change without notice

Dimensions in
inches (millimeters)

4

4

FUJITSU

SCHOTTKY 16384-BIT REGISTERED OUTPUT PROM

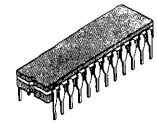
MB7238RA-20/25
MB7238RA-25W
MB7238RS-20/25
MB7238RS-25W

May 1988
Edition 1.0

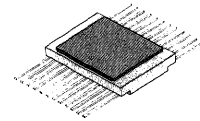
SCHOTTKY 16,384-BIT REGISTERED OUTPUT PROM

The Fujitsu MB7238 is a 16 Kbit bipolar programmable read-only memory circuit, with registered output (output data is latched in a register). The output register can be initialized to a field programmable value, either synchronously (MB7238RS) or asynchronously (MB7238RA). Three-state outputs can also be enabled either synchronously or asynchronously, in either model. DEAP (diffused eutectic aluminum process) memory cells are used to provide fast and reliable programming.

- 2048 word x 8 bit PROM data organization
- Fast clock access time:
  - — 20 ns (MB7238RA/RS-20)
  - — 25 ns (MB7238RA/RS-25)
- Output register can be preset to a field-programmable value.
- Register can be initialized synchronously (MB7238RS) or asynchronously (MB7238RA).
- Single +5 V operation
- TTL compatible I/O
- Low current inputs
- Three-state outputs
- Outputs can be enabled either synchronously or asynchronously.
- Outputs are kept disabled on power-up.
- DEAP memory cells are reliable and easily programmed.
- Test cells allow extensive testing of AC, DC and programming characteristics before shipment.



CERAMIC PACKAGE
DIP-24C-C04

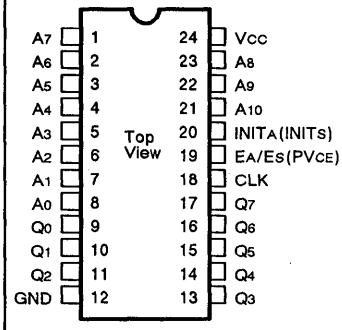


CERAMIC PACKAGE
FPT-24C-A02

See LCC-28C-A01

4

PIN ASSIGNMENT



Symbols in blankets: MB7238RS

See LCC PAD CONFIGURATION

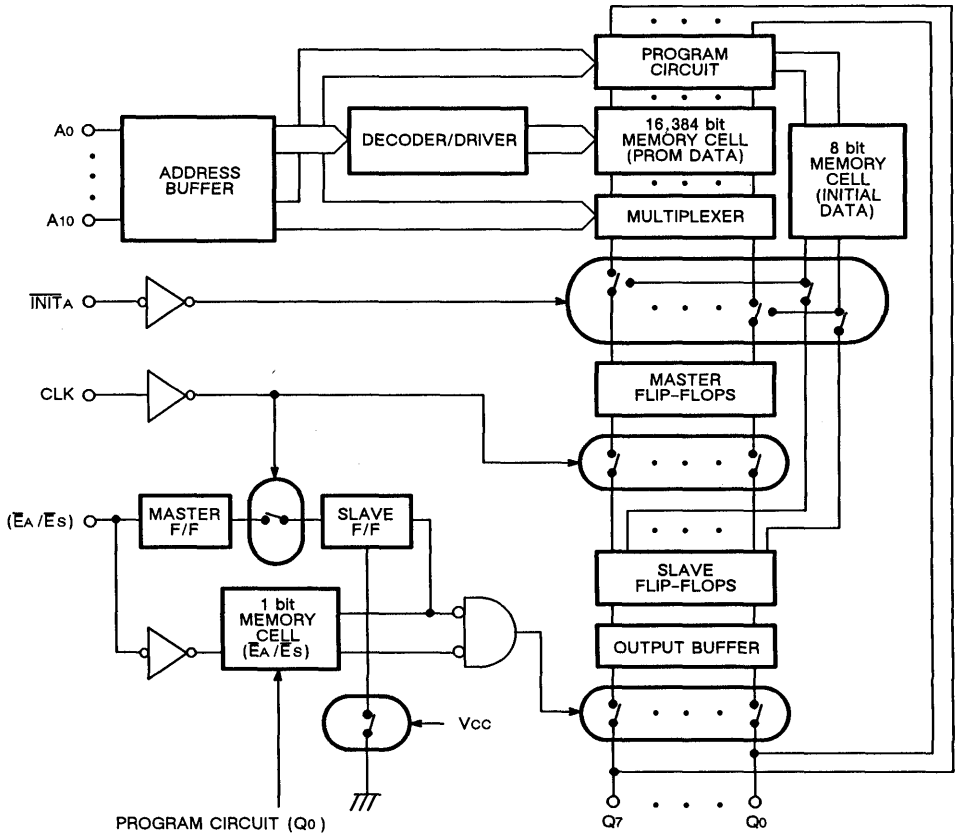
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-1.5 to +5.5	V
Input Current	I_{IN}	-20	mA
Output Current	I_{OUT}	+100	mA
Power Supply Voltage (during programming)	V_{CCP}	-0.5 to +7.5	V
Input Voltage (during programming)	V_{IPRG}	+22.5	V
Input Current (during programming)	I_{IPRG}	+270	mA
Output Voltage (during programming)	V_{OPRG}	-0.5 to +22.5	V
Output Current (during programming)	I_{OPRG}	+150	mA
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

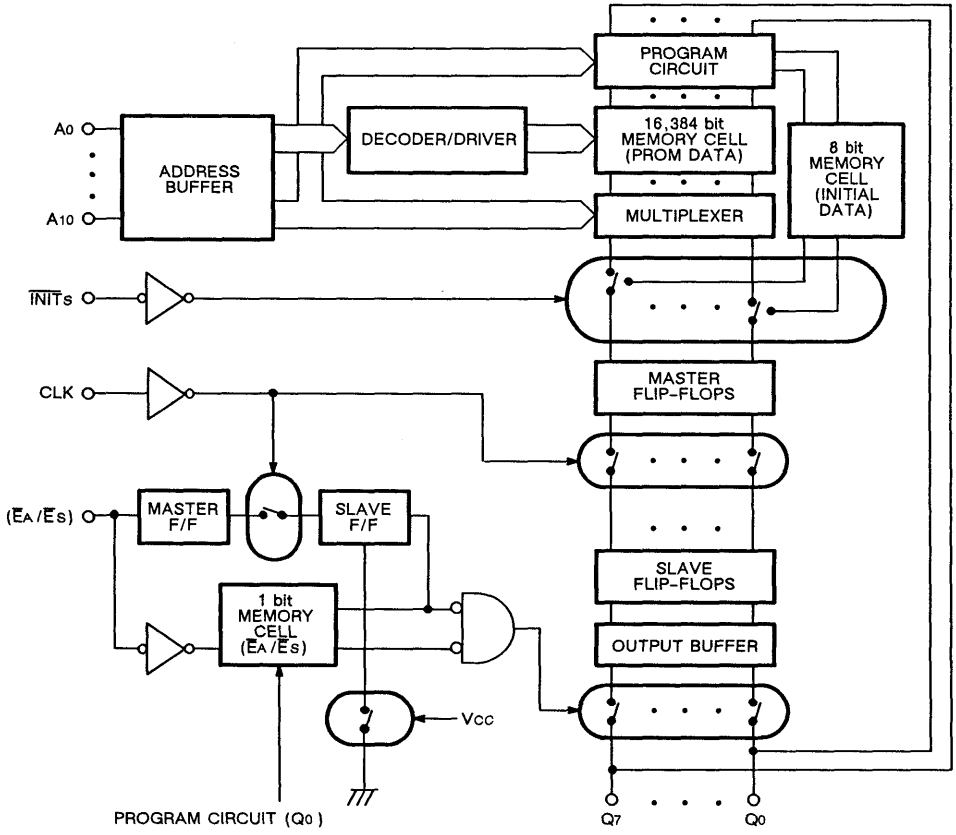
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB7238RA BLOCK DIAGRAM



Input				Output	Operating Mode	Remarks
$\overline{INIT}_A$	CLK	$\overline{E}_A$	$\overline{E}_S$			
L	X	L	—	Initial Data	Initialize	E_A Mode
H	↑	L	—	PROM Data	Load Register	
X	X	H	—	Z	Chip Disable	
L	X	—	L	Initial Data	Initialize	E_S Mode
H	↑	—	L	PROM Data	Load Register	
X	↑	—	H	Z	Chip Disable	

Fig. 2 — MB7238RS BLOCK DIAGRAM



Input				Output	Operating Mode	Remarks
INITs	CLK	EA	Es			
L	↑	L	—	Initial Data	Initialize	EA Mode
H	↑	L	—	PROM Data	Load Register	
X	X	H	—	Z	Chip Disable	
L	↑	—	L	Initial Data	Initialize	Es Mode
H	↑	—	L	PROM Data	Load Register	
X	↑	—	H	Z	Chip Disable	

4

READ OPERATIONS

OVERVIEW (SEE FIGURES 1 AND 2)

During PROM reads, data is shifted through a register latch, made of master-slave flip-flops, before appearing at the outputs. When a new address is applied to the address inputs (A_0 through A_{10}), new data appears in the master register. At the next clock pulse this data is transferred to the slave register. The MB7238 only has one chip enable pin $\overline{E}_A/\overline{E}_S$. $\overline{E}_A/\overline{E}_S$ pin is normally $\overline{E}_A$ mode, but you can change $\overline{E}_A$ mode to $\overline{E}_S$ mode (see page 11).

The chip enable input must be low in order for the data in the slave register to appear at the outputs (Q_0 through Q_7). Bringing the asynchronous chip enable ($\overline{E}_A$) low immediately enables the outputs. And bringing the synchronous chip enable ($\overline{E}_S$) low enables the outputs at the next clock pulse. Likewise, when the outputs are enabled, bringing either of the inputs high will cause them to be disabled, e.g., put into a high-impedance state. When $\overline{E}_A$ is brought high, the outputs are immediately disabled, whereas when $\overline{E}_S$ is brought high, they are disabled after the next clock pulse.

If the $\overline{INIT}$ input is brought low the register latch is loaded with a field-programmable initial value, rather than with PROM data. In the MB7238RS the master register is loaded immediately, and the contents are transferred to the slave register at the next clock pulse. In the MB7238RA both the master and slave registers are loaded immediately.

TIMING CONSIDERATIONS

Data Read (see Figure 3)

After an address change, address setup time t_S (A) must elapse before the master register contains valid new PROM data. The clock must then rise, within address hold time t_H (A), to shift the data to the slave register. The data will appear at the outputs within clock access time t_A (CLK) after the rising edge of the clock, if the outputs had been previously enabled.

If the outputs were disabled when the data was shifted, and are subsequently enabled by bringing $\overline{E}_A$ low, asynchronous chip enable time t_{EN} ($\overline{E}_A$) must elapse before the data appears at the outputs.

If $\overline{E}_S$ is brought low to enable the outputs, clock enable time t_{EN} (CLK) must elapse after the rising edge of the next clock. During this time the data from the master register is shifted to the slave register and appears at the outputs.

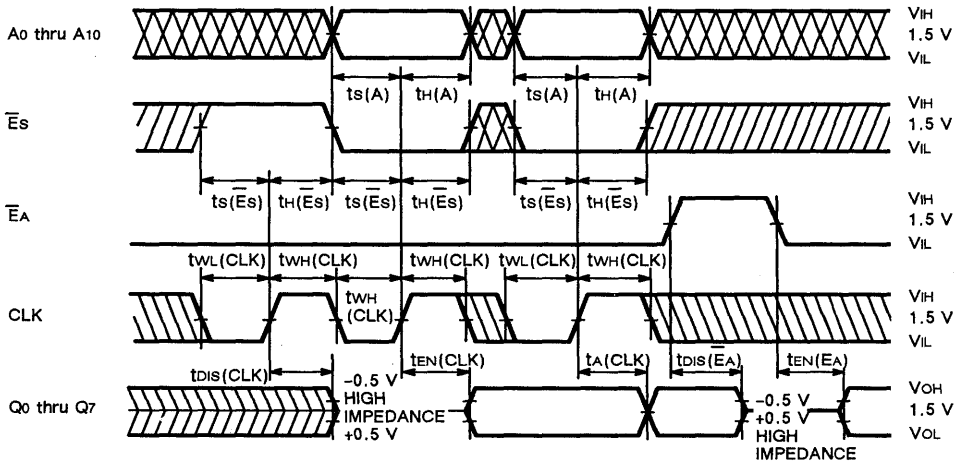
In the MB7238RA, when the registers have been initialized by $\overline{INIT}$, and $\overline{INIT}$ is then brought high to select PROM data, asynchronous initialize recovery time t_R ($\overline{INIT}_A$) must elapse after the clock signal is applied.

Initial Data Read (see Figures 4 and 5)

In the MB7238RA, after the $\overline{INIT}$ input is brought low, asynchronous initialize access time t_A ($\overline{INIT}_A$) must elapse before the initial data appears at the outputs.

In the MB7238RS, after the $\overline{INIT}$ input is brought low, synchronous initialize setup time t_S ($\overline{INIT}_S$) must elapse before valid initial data appears in the master register. It is then shifted and output in the same manner as PROM data.

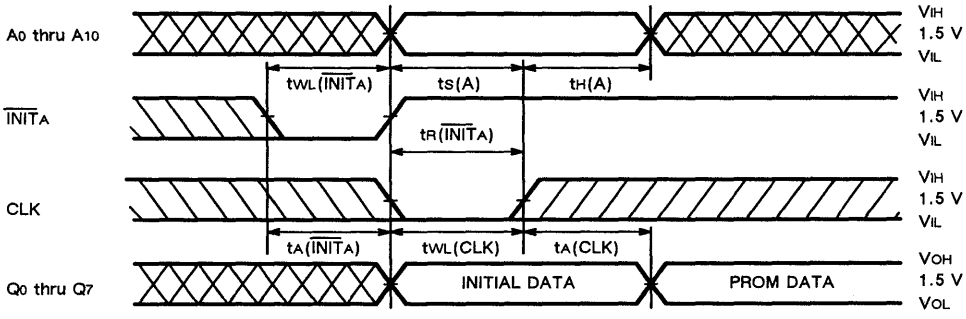
Fig. 3 — PROM DATA READ TIMING *1



Note:
*1. $\overline{INIT}$ is high.

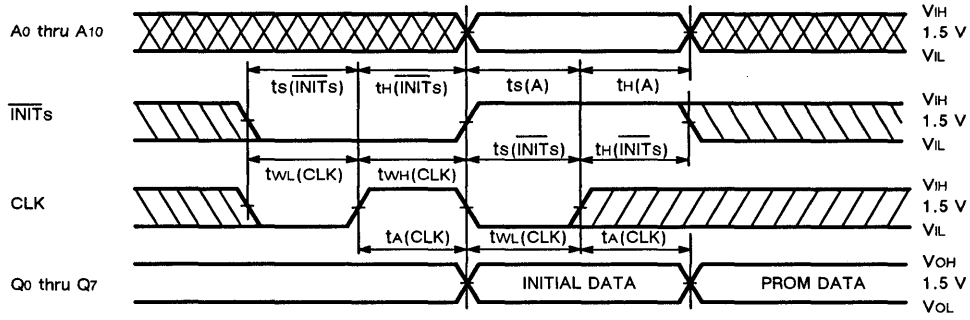
4

Fig. 4 — ASYNCHRONOUS INITIAL DATA READ TIMING (MB7238RA) *1



Notes:
*1. $\overline{EA}/\overline{Es}$ input is low.
*2. XX Don't care.

Fig. 5 — SYNCHRONOUS INITIAL DATA READ TIMING (MB7238RS)*1



Notes:
*1. $\overline{E}_A/\overline{E}_S$ Input are low.
*2. ⊠ Don't care.

4

DATA READ SPECIFICATIONS

Table 1—Guaranteed Operating Conditions

Parameter	Symbol	MB7238RA-20/-25 MB7238RS-20/-25			MB7238RA-25W MB7238RS-25W			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	0	—	0.8	0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.5	2.0	—	5.5	V
Ambient Temperature	T_A	0	—	75	-55	—	+125	°C

AC CHARACTERISTICS

Parameter	Symbol	Typical	MB7238RA-20 MB7238RS-20		MB7238RA-25 MB7238RS-25		MB7238RA-25W MB7238RS-25W		Unit	Remarks
			Min	Max	Min	Max	Min	Max		
Address Setup Time	t_S (A)	28	40	—	45	—	45	—	ns	—
Address Hold Time	t_H (A)	-8	0	—	0	—	0	—	ns	—
Clock Access Time	t_A (CLK)	15	—	20	—	25	—	25	ns	—
Clock Pulse Width	t_{WH} (CLK) / t_{WL} (CLK)	10	20	—	20	—	20	—	ns	
Synchronous Enable Setup Time	t_S ($\overline{E_S}$)	5	10	—	15	—	15	—	ns	—
Synchronous Enable Hold Time	t_H ($\overline{E_S}$)	0	5	—	5	—	5	—	ns	—
Asynchronous Initialize Access Time	t_A ($\overline{INIT_A}$)	20	—	30	—	35	—	35	ns	MB7238RA
Asynchronous Initialize Recovery Time	t_R ($\overline{INIT_A}$)	11	20	—	25	—	25	—	ns	MB7238RA
Asynchronous Initialize Pulse Width	t_{WL} ($\overline{INIT_A}$)	13	20	—	20	—	20	—	ns	MB7238RA
Synchronous Initialize Setup Time	t_S ($\overline{INIT_S}$)	15	25	—	30	—	30	—	ns	MB7238RS
Synchronous Initialize Hold Time	t_H ($\overline{INIT_S}$)	-10	0	—	0	—	0	—	ns	MB7238RS
Clock Enable Time	t_{EN} (CLK)	18	—	25	—	30	—	30	ns	—
Asynchronous Enable Time	t_{EN} ($\overline{E_A}$)	15	—	25	—	30	—	30	ns	—
Clock Disable Time *2	t_{DIS} (CLK)	18	—	25	—	30	—	30	ns	—
Asynchronous Disable Time *2	t_{DIS} ($\overline{E_A}$)	11	—	25	—	30	—	30	ns	—

Notes:
*1. At T_A = 25°C and V_{CC} = 5.0 V.
*2. Measured at a point on the output waveform 0.5 V from the active output level.

4

DC CHARACTERISTICS (Under Guaranteed Operating Conditions)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Current	I_{IH}	V_{IH} = 5.5V	—	—	40	µA
	I_{IL}	V_{IL} = 0.45 V	—	—	-250	µA
Input Clamp Voltage	V_{IC}	I_I = -18 mA	—	—	-1.2	V
Output Low Voltage	V_{OL}	I_{OL} = 10 mA *3	—	—	0.45	V
		I_{OL} = 16 mA	—	—	0.5	V
Output Leakage Current (Chip Disabled)	I_{OIL}	V_O = 0.45 V	—	—	-40	µA
	I_{OIH}	V_O = 2.4 V	—	—	40	µA
Output High Voltage *1	V_{OH}	I_{OH} = -2.4 mA	2.4	—	—	V
Output Short-Circuit Current *1	I_{OS}	V_O = 0 V	-15	—	-60	mA
Power Supply Current	I_{CC}	V_I = Open or 0 V	—	140 *2	185	mA

Notes:
*1. Denotes guaranteed characteristics of the output high-level state when the chip is enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.
*2. T_A = 25°C and V_{CC} = 5.0 V.
*3. This is not applied for W-version.

4

TERMINAL CAPACITANCE

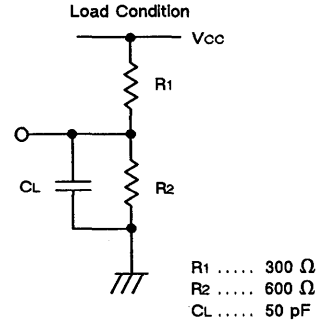
(T_A = 25°C, V_{CC} = +5.0 V, V_{IN} = +2.0 V, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Terminal Capacitance	C_{IN}	—	10	pF
Output Terminal Capacitance	C_{OUT}	—	15	pF

Fig. 6 — AC TEST CONDITIONS

INPUT CONDITIONS

Amplitude ..... 0 V to 3 V
Rise and Fall Time ..... 5 ns from 1 V to 2 V
Frequency ..... 1 MHz



FABRICATION TECHNOLOGY

INPUT/OUTPUT CIRCUITS

The inputs use Schottky TTL circuitry to achieve a fast response time. A PNP transistor is used in the first stage to minimize switching current. Protection diodes are also included.

The three-state outputs (high, low, and high-impedance states) combine the advantages of totem-pole outputs (high noise immunity, fast rise time, ample line-driving capacity) and direct connection to a bus-oriented system. Schottky TTL circuitry is used for fast operation. A PNP transistor in the output circuit minimizes the load on the chip enable circuitry.

MEMORY CELLS

The memory cells in the MB7238 are of the junction-shorting type, using DEAP technology. They are initially all in the 0 (low voltage) state. In this state, the cell's programmable element, a PN diode, blocks current flow. During programming, the diode's junction is shorted, allowing it to conduct current, thus permanently changing the cell's state to 1 (high).

By applying reverse current pulses to the diode's cathode, the temperature at the junction is raised. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and shorts the junction. The power dissipation at the junction immediately drops to less than one fifth, thus lowering the temperature. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

In the memory cell array, the word line islands are divided by IOP (Isolation by Oxide and Poly-silicon) passive isolation. Memory cells in the same island are divided by SVG (Shallow V-Groove) passive isolation. The vertically structured memory cells permit a high packing density.

4

PROGRAMMING

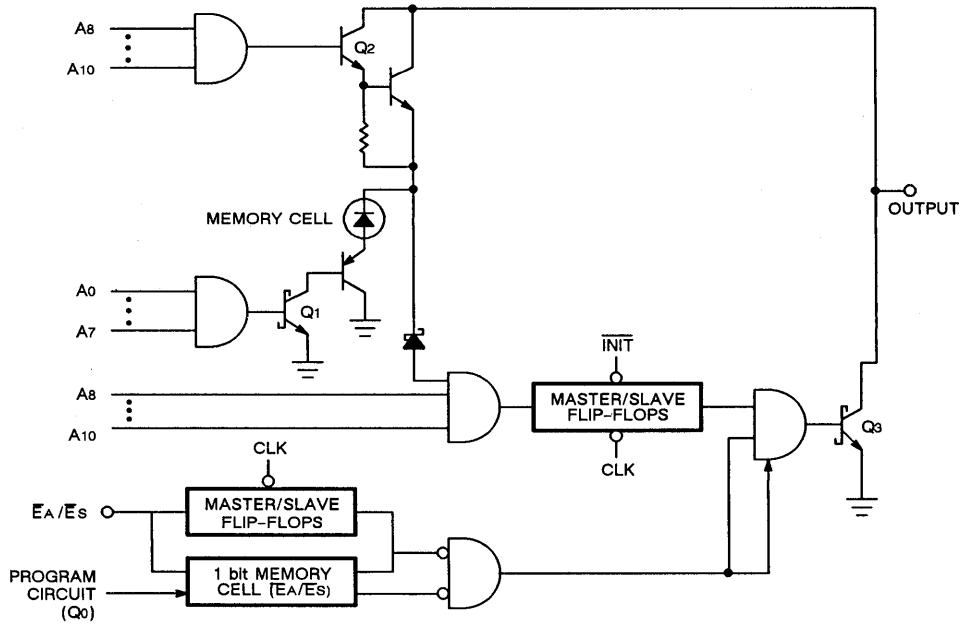
OVERVIEW (See Figure 7)

As shipped, all the bits in the MB7238 are in the 0 (low) state. In programming, individual cells are addressed and a programming current applied, to change that bit's state to 1. Only one bit at a time can be programmed, because the internal decoding circuitry can only sink one unit of programming current at a time.

The word containing the desired bit is first selected, using the normal address inputs. The decoded address lines turn on transistors Q_1 and Q_2. When the PV_{CE} level is applied to the $\overline{E}_A/\overline{E}_S$ input, the chip outputs are disabled, turning off transistor Q_3. Programming pulses are applied to the output of the desired bit, eventually fusing the diode attached to Q_1. At this point, if the output is read, it will be in the 1 (high) state. Two additional programming pulses are then applied, to ensure reliability.

Initial data is programmed in the same way, except that the address inputs are kept low, and $\overline{INIT}$ is applied to an $\overline{INIT}$ pulse, to select the initial data word rather than a PROM data word.

Fig. 7 — PROGRAMMABLE MEMORY CELL



PROCEDURE

1) Apply power to the device (V_{CC} = 5 V, GND = 0 V).
2) Set $\overline{E}_A/\overline{E}_S$ low. Set $\overline{INIT}$ input high to select PROM data for programming, or set initialize inputs and address inputs low to select initial data.
3) Select the desired bit.
4) Apply a clock pulse.
5) Read the output to confirm that the desired bit is in fact 0. If not, go on to the next bit.
6) Raise the V_{CC} terminal to PV_{CC} (7 V).
7) Raise the $\overline{E}_A/\overline{E}_S$ terminal to PV_{CE} (20 V).
8) Apply a clock pulse.
9) Apply a programming pulse (125 mA, 11 μS) to the output (Q_X) of the desired bit.
10) Return PV_{CC} to a 5 V and PV_{CE} to 0 V. And in case of initial data, apply an $\overline{INIT}$ pulse.
11) Apply a clock pulse.
12) After a delay of t_{PR} (5 μs), read the output voltage V_O.
    a) If V_O is still low, repeat steps (6) through (12), allowing t_{CYC} (50 μs) for each cycle, up to 100 times.
    b) If V_O is high, apply two additional programming pulses, to ensure reliable retention.
13) If there are more bits to be programmed, repeat steps (3) through (12).

LIABILITY

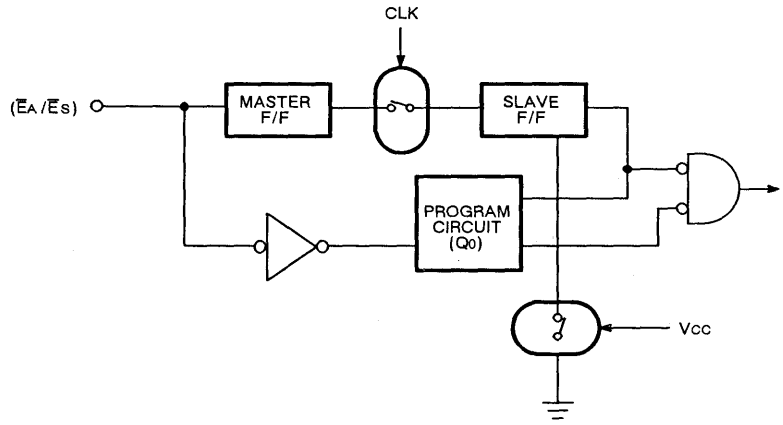
Fujitsu performs an extensive series of tests to ensure device performance before shipping. However, 100% programmability is not guaranteed. Furthermore, it is imperative that the programming specifications be rigorously adhered to in order to achieve a satisfactory programming yield.

Fujitsu will not accept responsibility for any device found defective if it was not programmed according to these specifications. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of suspected defective memory cells.

CHANGING $\overline{E}_A$ INPUT TO $\overline{E}_S$ INPUT

The MB7238 has only one chip enable pin, $\overline{E}_A$. However, this can be changed to an $\overline{E}_S$ input, by programming a special memory cell. The programming method is similar to that described above for PROM and initial data, the only differences being that address line A_0 is raised to 20 V, and programming pulses are applied only to output Q_0. Also, when reading the output voltage to confirm programming, the state of the special memory cell is reflected in the outputs, Q_0.

Fig. 8 — ENABLE INPUT PROGRAMMING CIRCUIT



PROCEDURE

1) Apply power to the device (V_{CC} = 5 V, GND = 0 V).
2) Set $\overline{E}_A$ low. Raise A_0 to PV_{AO} (20 V), and set all the other address lines low. Set the $\overline{INIT}$ input low.
3) Apply a clock pulse.
4) Read the Q_0 output to confirm that it is in fact 0. If not, no programming is necessary.
5) Raise the V_{CC} terminal to PV_{CC} (7 V).
6) Raise the $\overline{E}_A$ terminal to PV_{CE} (20 V).
7) Apply a clock pulse.
8) Apply a programming pulse (125 mA, 11 µs) to output terminal Q_0.
9) Return PV_{CC} to 5 V and PV_{CE} to 0 V.
10) Apply a clock pulse.
11) After a delay of t_{PR} (5 µs), read the output voltage V_O.
    a) If V_O is still low, repeat steps (5) through (11), allowing t_{CYC} (50 µs) for each cycle, up to 100 times.
    b) If V_O is high, apply two additional programming pulses, to ensure reliable retention.

LIABILITY

Fujitsu performs an extensive series of tests to ensure device performance before shipping. However, 100% programmability is not guaranteed. Furthermore, it is imperative that the programming specifications be rigorously adhered to in order to achieve a satisfactory programming yield.

Fujitsu will not accept responsibility for any device found defective if is was not programmed according to these specifications. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of suspected defective memory cells.

Fig. 9a – PROGRAMMING TIMING CHART

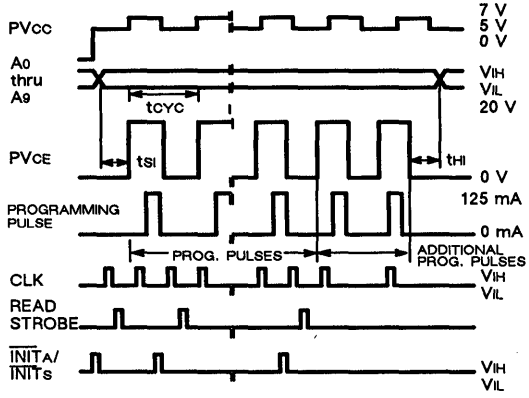
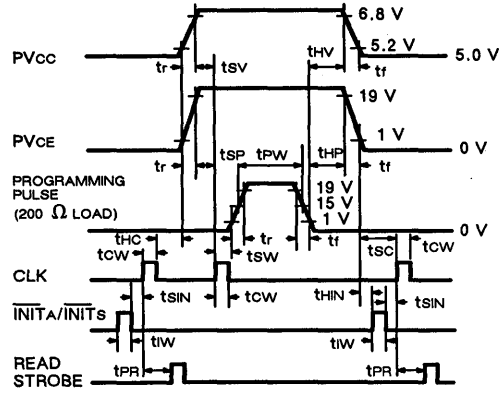


Fig. 9b – ONE DETAILED PROGRAMMING CYCLE



4

PROGRAMMING SPECIFICATIONS, DC

Parameter	Symbol	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	0	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	5.25	V
Power-supply Voltage	V_{CC}	4.75	5.0	5.25	V
Power-supply Current	I_{CC}	—	200	—	mA
PV_{CC} Power-supply Voltage	PV_{CC}	6.7	7.0	7.3	V
PV_{CC} Power-supply Current	PI_{CC}	—	—	300	mA
Programming Pulse Current	I_{PRG}	120	—	130	mA
Programming Pulse Clamp Voltage	V_{PRG}	20	20	22	V
PV_{CE} Pulse Voltage	PV_{CE}	20	20	22	V
PV_{CE} Pulse Clamp Current	PI_{CE}	230	—	260	mA
PV_{AO} Pulse Voltage	PV_{AO}	10	—	22	V
PV_{AO} Pulse Clamp Current	PI_{AO}	10	—	—	mA
Reference Level for Output High Voltage	V_{REF}	1.0	1.5	2.4	V

PROGRAMMING SPECIFICATIONS, AC

Parameter	Symbol	Min	Max	Typ	Unit
Programming Pulse Cycle Time	t_{CYC}	40	50	60	µs
Programming Pulse Width	t_{PW}	10	11	12	µs
Clock Pulse Width	t_{CW}	0.5	—	—	µs
Programming Pulse Rise Time	t_r	—	—	2	µs
PV_{CC} Pulse Rise Time	t_r	—	—	2	µs
PV_{CE} Pulse Rise Time	t_r	—	—	2	µs
Programming Pulse Fall Time	t_f	—	—	2	µs
PV_{CC} Pulse Fall Time	t_f	—	—	2	µs
PV_{CE} Pulse Fall Time	t_f	—	—	2	µs
Input Setup Time	t_{SI}	2	—	—	µs
PV_{CC} Pulse Setup Time	t_{SV}	2	—	—	µs
PV_{CE} Pulse Setup Time	t_{SP}	2	—	—	µs
Programming Pulse Setup Time	t_{SW}	2	—	—	µs
Input Hold Time	t_{HI}	2	—	—	µs
PV_{CC} Pulse Hold Time	t_{HV}	2	—	—	µs
PV_{CE} Pulse Hold Time	t_{HP}	2	—	—	µs
Clock Pulse Setup Time	t_{SC}	5	—	—	µs
Clock Pulse Hold Time	t_{HC}	5	—	—	µs
Init Pulse Setup Time	t_{SIN}	0.5	—	—	µs
Init Pulse Hold Time	t_{HIN}	2	—	—	µs
Init Pulse Width	t_{IW}	0.5	—	—	µs
Clock Pulse Rising Edge to Read Strobe Time	t_{PR}	5	—	—	µs
Number of Programming Pulses	n	—	—	100	pulses
Programming Time/Bit	—	120	—	6120	µs/bit
Number of Additional Programming Pulses	—	2	—	2	pulses

4

TYPICAL PERFORMANCE CHARACTERISTICS

DC CHARACTERISTICS

Fig. 10 – I_{IN} Input Current vs. V_{IN} Input Voltage

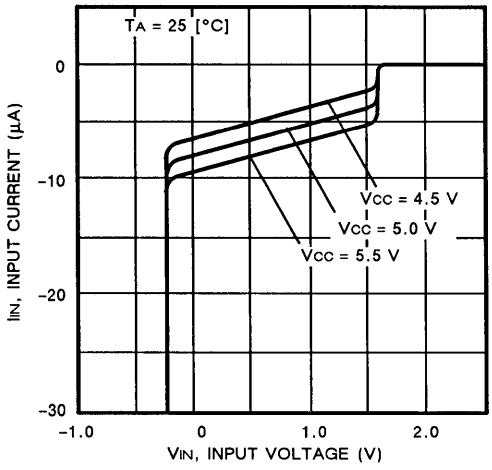


Fig. 11 – I_{OH} Output High Current vs. V_{OH} Output High Voltage

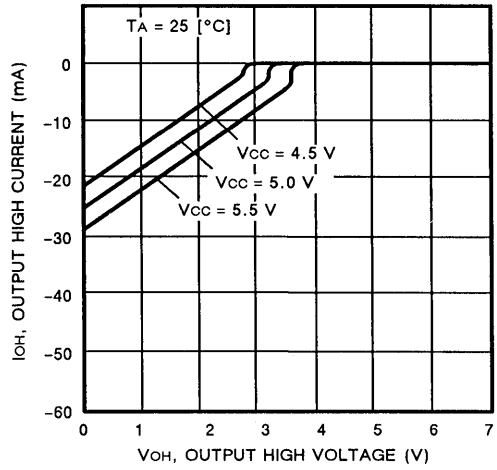
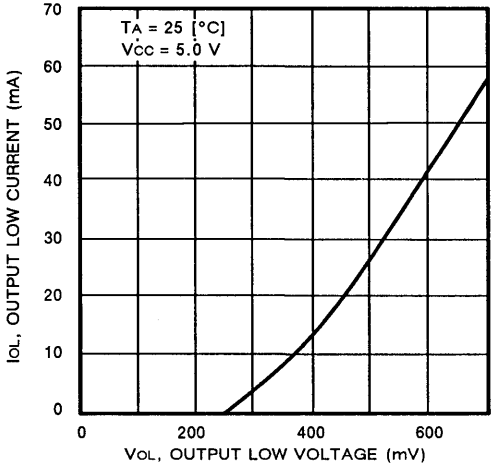


Fig. 12 – I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



4

DC CHARACTERISTICS (Cont.)

Fig. 13 – tS (A) Address Setup Time vs. Ambient Temperature

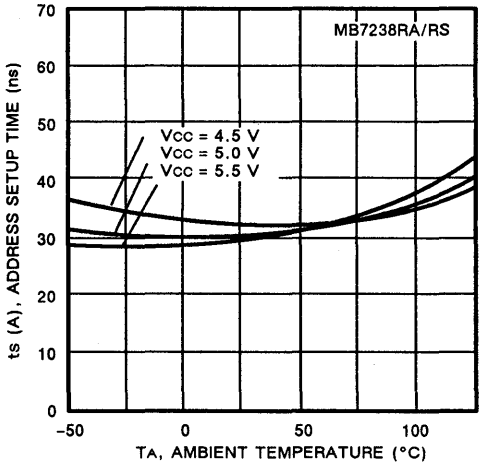


Fig. 14 – tH(A) Address Hold Time vs. Ambient Temperature

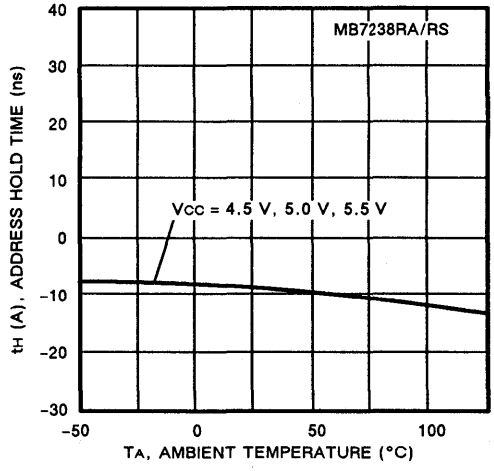


Fig. 15 – tA (CLK) Clock Access Time vs. Ambient Temperature

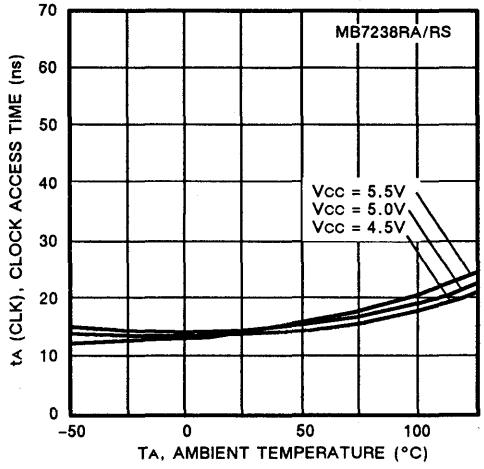
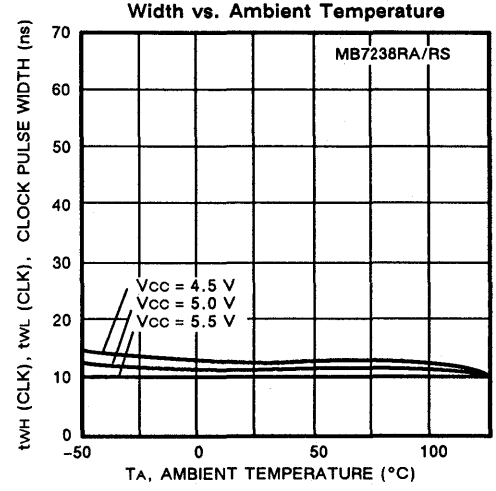


Fig. 16 – tWH (CLK) and tWL (CLK) Clock Pulse Width vs. Ambient Temperature



4

DC CHARACTERISTICS (Cont.)

Fig. 17 – t_S ($\overline{E_S}$) Synchronous Enable SetupTime vs. Ambient Temperature

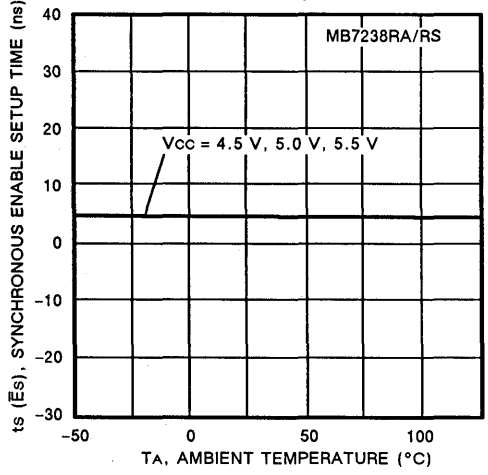


Fig. 18 – t_H ($\overline{E_S}$) Synchronous Enable Hold Time vs. Ambient Temperature

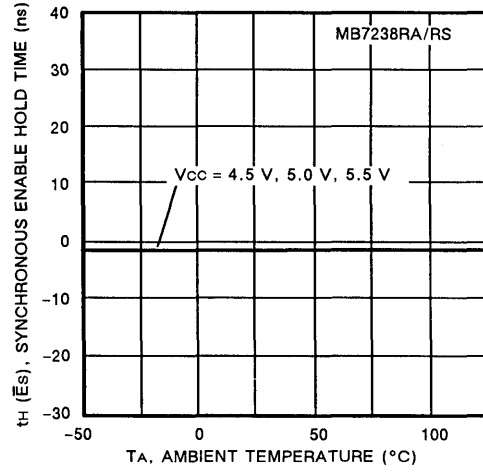


Fig. 19 – t_A ($\overline{INIT_A}$) Asynchronous Initialize Access Time vs. Ambient Temperature

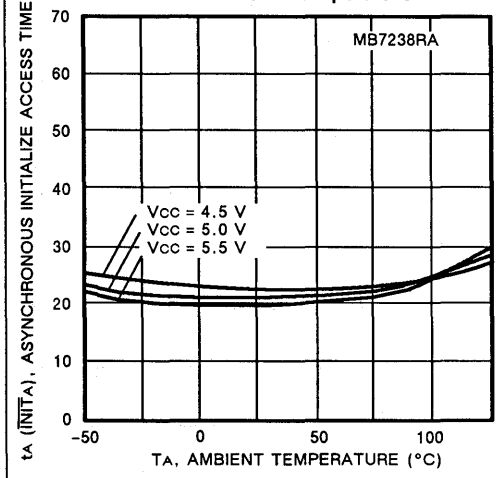
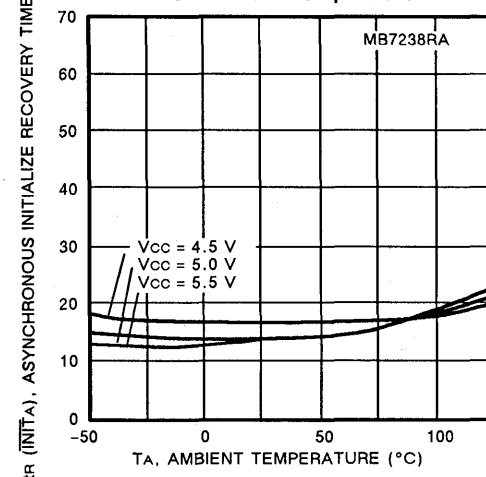


Fig. 20 – t_R ($\overline{INIT_A}$) Asynchronous Initialize Recovery Time vs. Ambient Temperature



4

DC CHARACTERISTICS (Cont.)

Fig. 21 – t_{WL} ($\overline{INITA}$) Asynchronous Initialize Pulse Width vs. Ambient Temperature

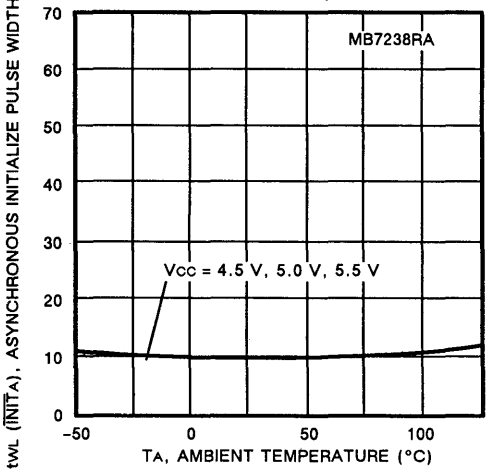


Fig. 22 – t_S ($\overline{INITs}$) Synchronous Initialize Setup Time vs. Ambient Temperature

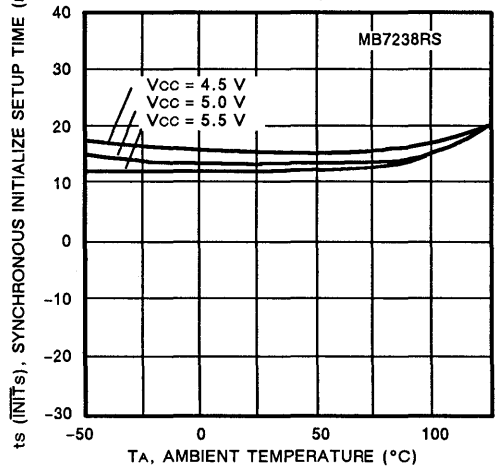


Fig. 23 – t_H ($\overline{INITs}$) Synchronous Initialize Hold Time vs. Ambient Temperature

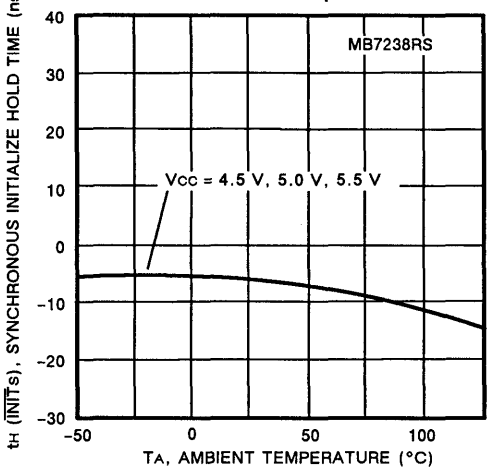
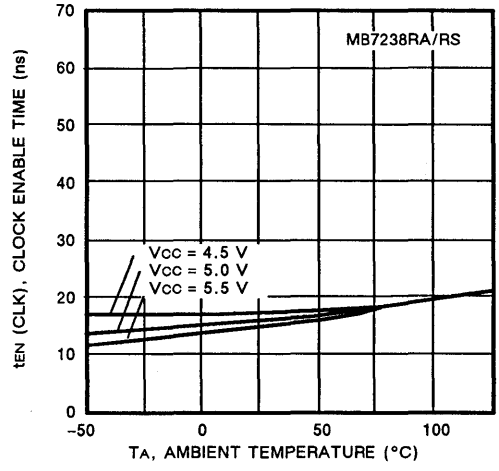


Fig. 24 – t_{EN} (CLK) Clock Enable Time vs. Ambient Temperature



4

DC CHARACTERISTICS (Cont.)

Fig. 25 – t_{EN} ($\overline{E}_A$) Asynchronous Enable Time vs. Ambient Temperature

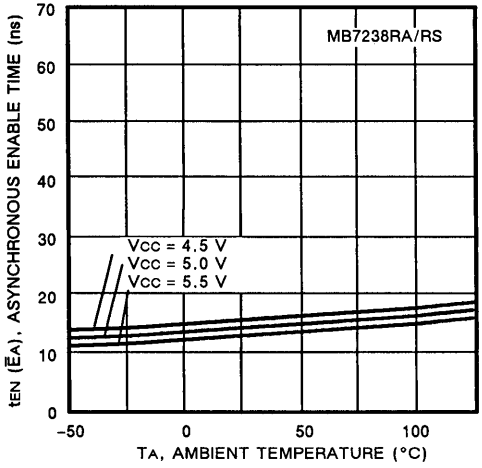


Fig. 26 – t_{DIS} (CLK) Clock Disable Time vs. Ambient Temperature

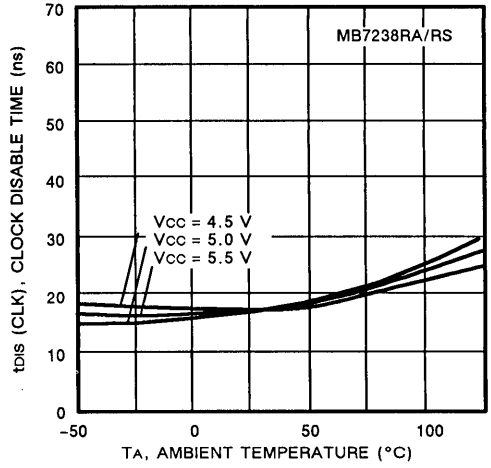


Fig. 27 – t_{DIS} ($\overline{E}_A$) Asynchronous Disable Time vs. Ambient Temperature

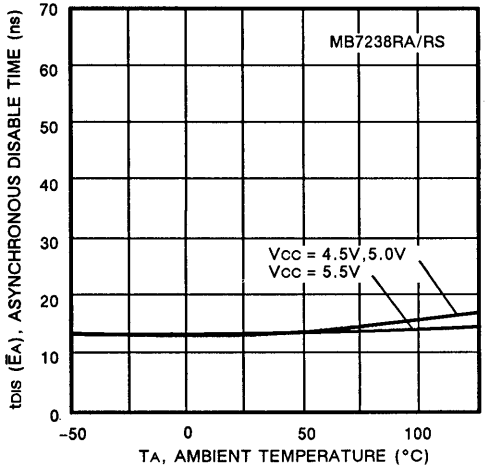
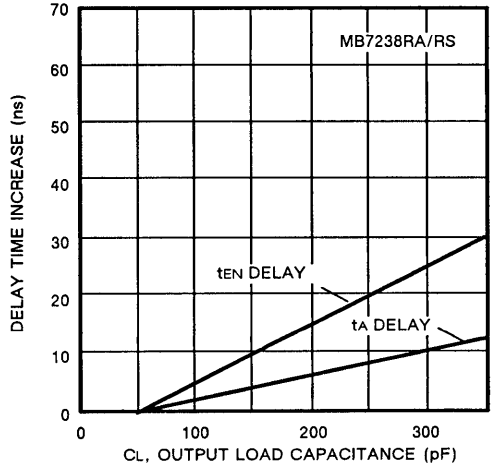


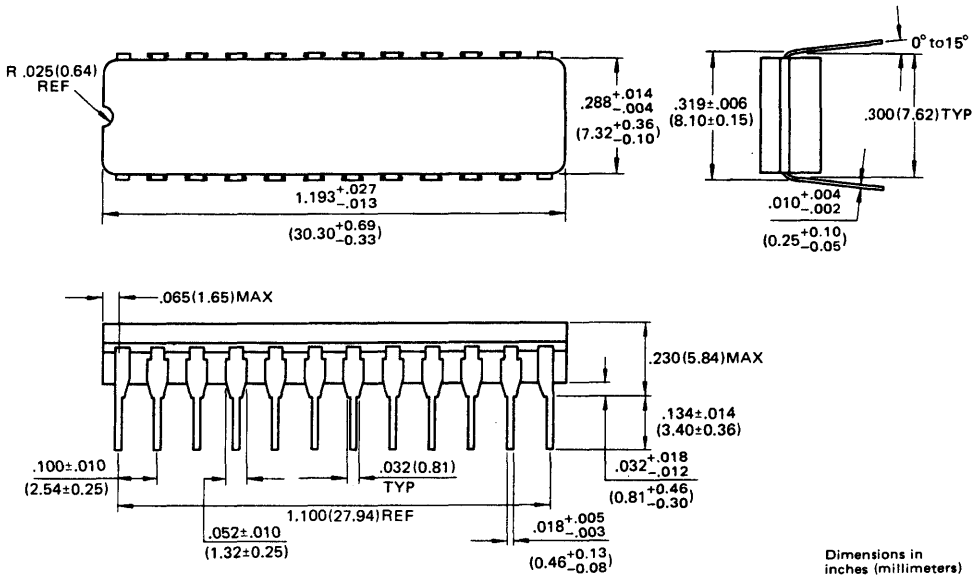
Fig. 28 – Delay Time Increase vs. Load Capacitance



4

PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C04)

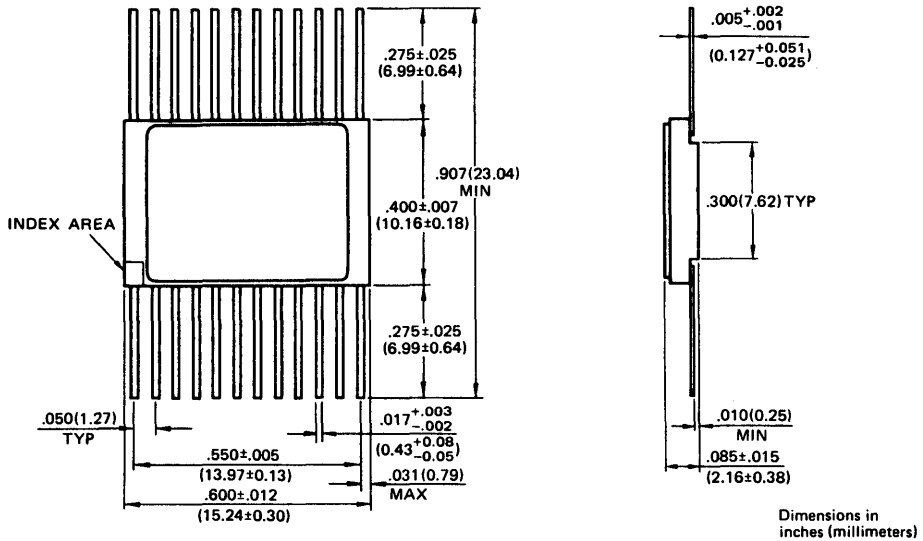


Dimensions in inches (millimeters)

4

PACKAGE DIMENSIONS (Continued)

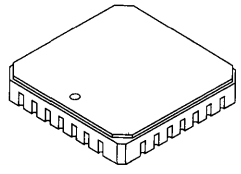
24-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(CASE No.: FPT-24C-A02)



Dimensions in
inches (millimeters)

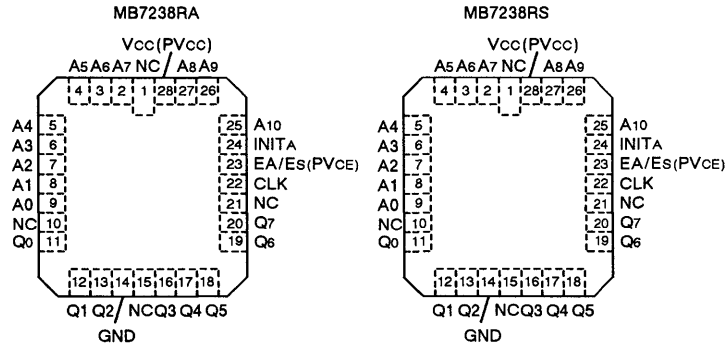
4

PACKAGE DIMENSIONS (Continued)

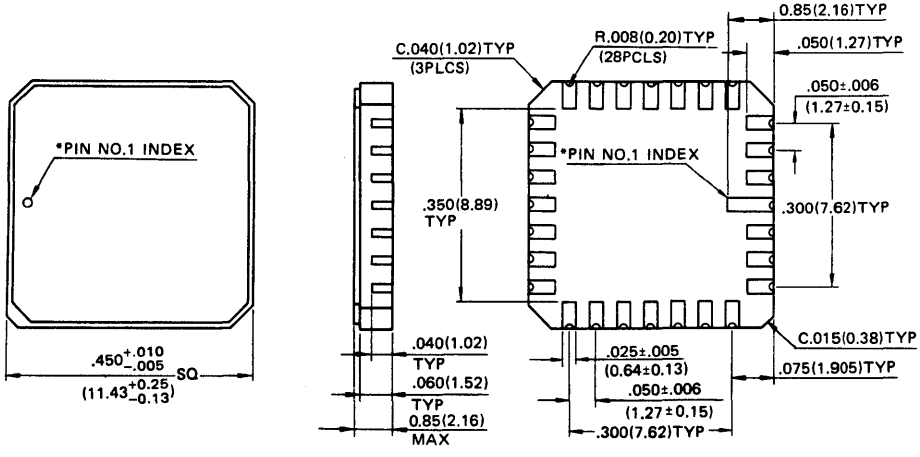


LCC-28C-A01

PAD CONFIGURATION



28-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-28C-A01)



*Shape of Pin No.1 index: Subject to change without notice

Dimensions in inches (millimeters)

4

4

Section 5

Quality and Reliability

5

5

■ Quality Control at Fujitsu

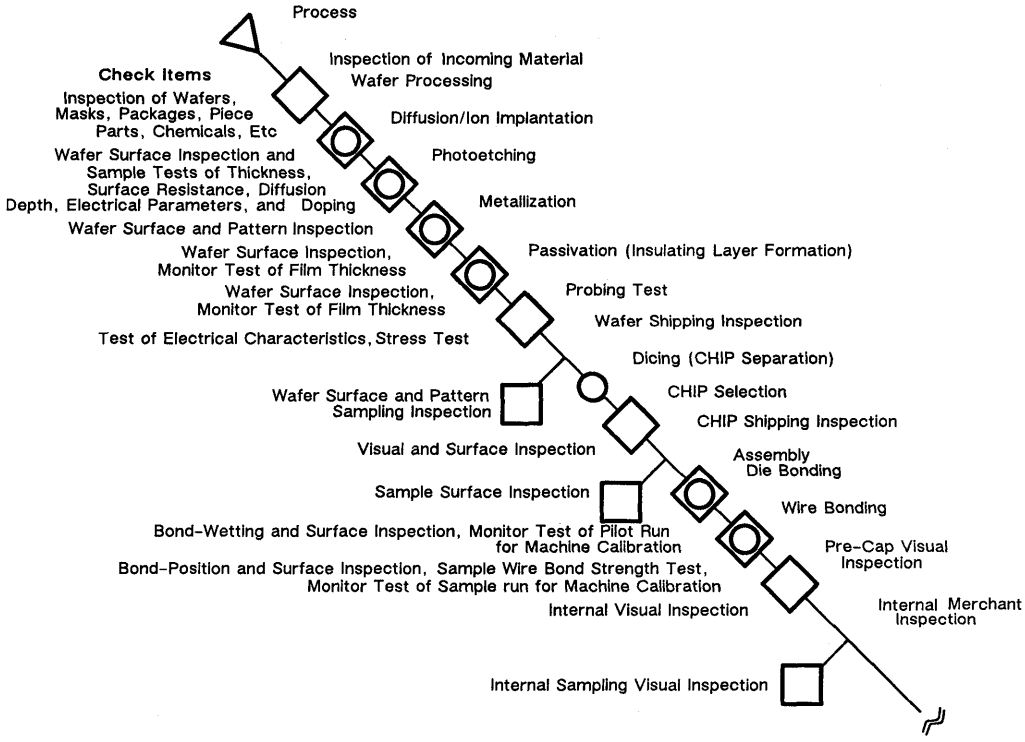
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end on the Fujitsu factory floor. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

Quality Control Flowchart



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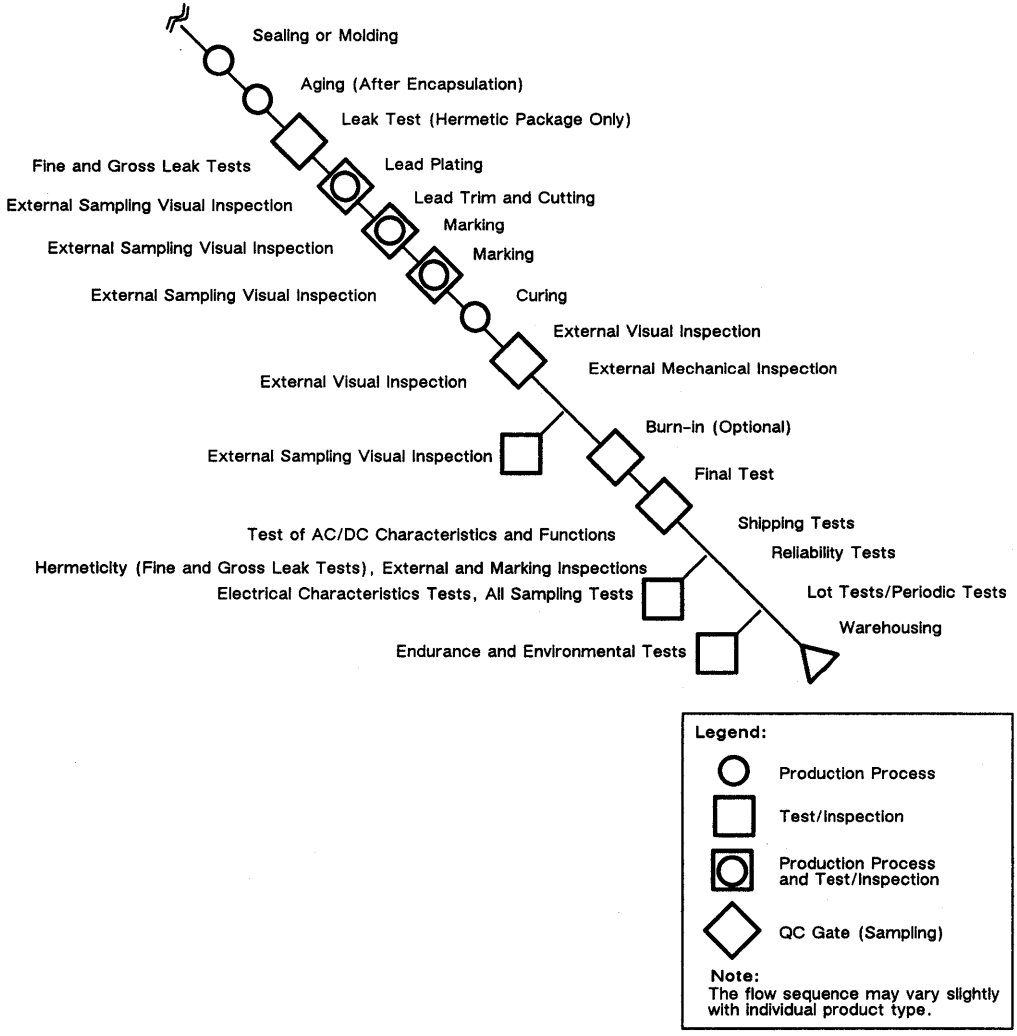
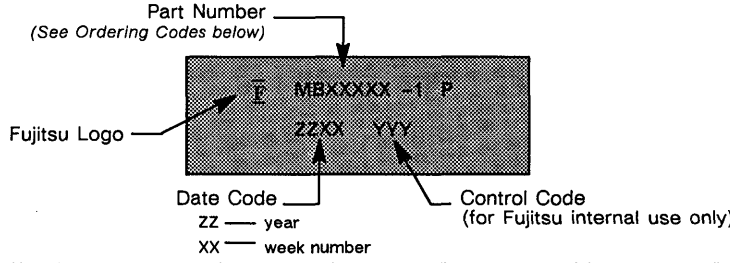

Sealing or Molding
Aging (After Encapsulation)
Leak Test (Hermetic Package Only)
Fine and Gross Leak Tests
Lead Plating
External Sampling Visual Inspection
Lead Trim and Cutting
Marking
External Sampling Visual Inspection
Marking
External Sampling Visual Inspection
Curing
External Visual Inspection
External Mechanical Inspection
External Visual Inspection
Burn-in (Optional)
External Sampling Visual Inspection
Final Test
Shipping Tests
Test of AC/DC Characteristics and Functions
Reliability Tests
Hermeticity (Fine and Gross Leak Tests), External and Marking Inspections
Lot Tests/Periodic Tests
Electrical Characteristics Tests, All Sampling Tests
Warehousing
Endurance and Environmental Tests
Legend:
Production Process
Test/Inspection
Production Process and Test/Inspection
QC Gate (Sampling)
Note:
The flow sequence may vary slightly with individual product type.

Section 6

Ordering Information

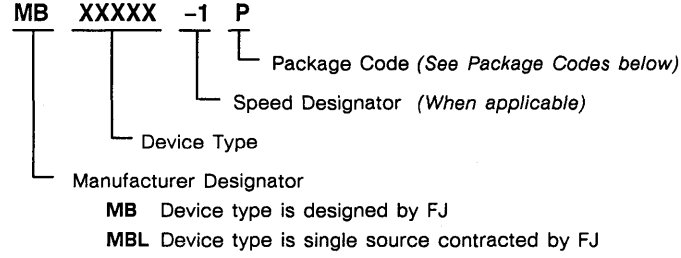
6

■ Product Marking



Note: Marking formats may vary, depending on the product. The country of origin appears on all finished parts.

■ Ordering Codes



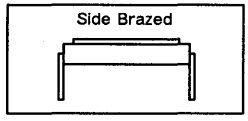
Note: Regarding ordering code, please contact your Fujitsu sales office for more information.

■ Package Codes

Ceramic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	TV,CV
PGA (Pin Grid Array)	CR
DIP (Side Brazed) 1	C
DIP (CERDIP) 2	Z
Shrink DIP	CSH
Flatpack	ZF
SOJ (Single Outline Junction)	CJ

Plastic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	PV
PLCC (Leaded Chip Carrier)	PD
PGA (Pin Grid Array)	PR
DIP (Dual In-line Package)	P,M
Shrink DIP	PSH
Flatpack	PF
Single In-line, Straight Leads	PS
Single In-line, Zig-zag Leads	PSZ,PZ
SOJ (Single Outline Junction)	PJ

1



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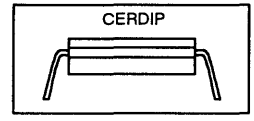

Section 7

Sales Information

7

Introduction to Fujitsu

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly-owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to include one research and development division, two marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The research and development division, Advanced Products Division (APD), using US-based engineering, has jointly developed RISC for Sun Microsystems and Ethernet®, a chip set used in local area networks. APD also markets a full line of SPARC™ RISC processors, peripheral chips, and evaluation boards, as well as EtherStar™, the first VLSI device to integrate both StarLan™ and Ethernet protocols into one device.

The Microwave and Optoelectronics Division (MOD) markets GaAs, FETs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

Fujitsu Microelectronics, Inc. (Continued)

The largest FMI marketing division is the Integrated Circuits Division (ICD).

Memory and programmable devices marketed by ICD include the following:

- DRAMs
- EPROMs
- EEPROMs
- NOVRAMs
- CMOS masked ROMs
- CMOS SRAMs
- Bipolar PROMs
- ECL RAMs
- STRAMs (self-timed RAM)
- Ultra High speed ECL/ECL—TTL Translator Circuits
- Linear ICs and transistors

ASIC products offered by ICD include the following:

- CMOS, ECL, and BiCMOS gate arrays
- CMOS standard cells

Customer support and customer training for ASIC products are available through the following FMI design centers:

- San Jose
- Dallas
- Atlanta
- Chicago
- Boston

Microcomputer and communications products offered by ICD include the following:

- 4-bit MCUs
- 8- and 16-bit MPUs
- SCSI and controllers
- DSPs
- Prescalers
- PLLs

Fujitsu Microelectronics, Inc. (Continued)

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, FMI opened the Gresham Manufacturing Division to manufacture ASIC products and DRAMs. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Components of America**, markets connectors, keyboards, plasma displays, relays, and hybrid ICs.

Fujitsu Mikroelektronik GmbH (European Sales Center)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a wholly-owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Europe. The wide range of ICs, LSI memories, microprocessors, and ASIC products are noted throughout Europe for design excellence and unmatched reliability. Branch offices are located in Munich, London, Paris, Stockholm, and Milan.

Fujitsu Microelectronics Ireland, Ltd. (European Production Center)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980 in the suburbs of Dublin as Fujitsu's European Production Center for integrated circuits. FME assembles DRAMs, EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd. (European Design Center)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with highly sophisticated CAD systems to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Pacific Asia Ltd. (Asian/Oceanian Sales Center)

Fujitsu Microelectronics Pacific Asia Ltd. (FMP) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

SPARC™ is a trademark of Sun Microsystems, Inc.
Ethernet® is a registered trademark of Xerox Corporation.
EtherStar™ is a trademark of Fujitsu Microelectronics, Inc.
StarLAN™ is a trademark of AT&T.

■ Integrated Circuits Corporate Headquarters

FUJITSU LIMITED
Communications and Electronics

Marunouchi Headquarters
6-1, Marunouchi 1-chome
Chiyoda-ku, Tokyo 100
Japan
Tel: (03) 216-3211
Telex: 781-22833
FAX: (03) 213-7174

For integrated circuits marketing information please contact the following:

Japan

FUJITSU LIMITED

Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg.
6-1, Marunouchi 1-chome
Chiyoda-ku, Tokyo 100
Japan
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Telex: 781-2224361
FAX: (03) 216-9771

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Integrated Circuits Division
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San Jose, CA 95134-1804
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Telex: 910-338-0190
FAX: (408) 432-9044

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FUJITSU MIKROELEKTRONIK GmbH

Lyoner Strasse 44-48
Arabella Centre 9. OG
D-6000 Frankfurt 71
Federal Republic of Germany
Tel: (069) 66320
Telex: 441963
FAX: (069) 6632122

Asia

FUJITSU MICROELECTRONICS PACIFIC ASIA LIMITED

805 Tsimshatsui Centre
West Wing
66 Mody Road, Tsimshatsui East
Kowloon, Hong Kong
Tel: (03) 732-0100
Telex: 31959 FUJIS HX
FAX: (03) 722-7984

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FAX: (408) 725-8746

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Fujitsu Microelectronics, Inc.
Century Centre
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Suite 510
Irvine, CA 92714
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FAX: (714) 724-8778

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3500 Parkway Lane
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Norcross, GA 30092
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FAX: (404) 441-2016

ILLINOIS (Chicago)
Fujitsu Microelectronics, Inc.
One Pierce Place
Suite 910
Itasca, IL 60143-2681
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FAX: (312) 250-8591

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FAX: (617) 964-3301

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FAX: (612) 454-0601

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Horizon Corporate Center
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Mt. Laurel, NJ 08054
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FAX: (609) 727-9797

NEW YORK (Hauppauge)
Fujitsu Microelectronics, Inc.
601 Veterans Memorial Highway
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Hauppauge, NY 11788-1054
Tel: (516) 361-6565
FAX: (516) 361-6480

OREGON (Portland)
Fujitsu Microelectronics, Inc.
5285 SW Meadows Road
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Lake Oswego, OR 97035-9998
Tel: (503) 684-4545
FAX: (503) 684-4547

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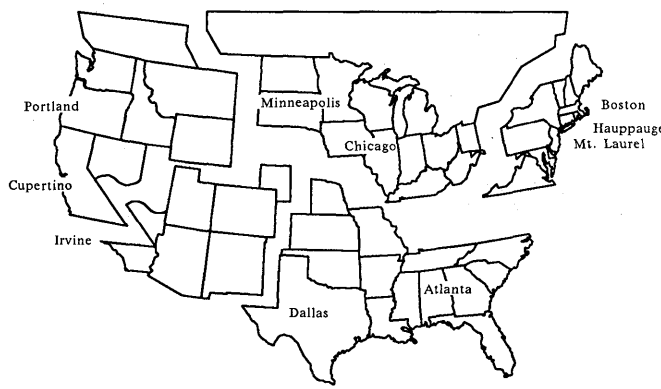
Fujitsu Microelectronics, Inc.
14785 Preston Road
Suite 670
Dallas, TX 75240
Tel: (214) 233-9394
FAX: (214) 386-7917



7

■ Representatives — USA

Alabama
The Novus Group, Inc.
2905 Westcorp Blvd.
Suite 120
Huntsville, AL 35805
Tel: (205) 534-0044
FAX: (205) 534-0186

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Aztech Component Sales Inc.
15230 N 75th Street
Suite 1031
Scottsdale, AZ 85260
Tel: (602) 991-6300
FAX: (602) 991-0563

California
Harvey King, Inc.
6393 Nancy Ridge Drive
San Diego, CA 92121
Tel: (619) 587-9300
FAX: (619) 587-0507

Infinity Sales, Inc.
4500 Campus Drive
Suite 300
Newport Beach, CA 92660
Tel: (714) 833-0300
FAX: (714) 833-0303

Norcomp
3350 Scott Blvd., #24
Santa Clara, CA 95054
Tel: (408) 727-7707
FAX: (408) 986-1947

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2140 Professional Drive
Suite 200
Roseville, CA 95661
Tel: (916) 782-8070
FAX: (916) 782-8073

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Front Range Marketing
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Boulder, CO 80303
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FAX: (303) 447-0371

Connecticut
Conntech Sales, Inc.
182 Grand Street
Suite 318
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Tel: (203) 754-2823
FAX: (203) 573-0538

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Semtronic Associates, Inc.
657 Maitland Avenue
Altamonte Springs, FL 32701
Tel: (407) 831-8233
FAX: (407) 831-2844

Semtronic Associates, Inc.
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Tel: (813) 461-4675
FAX: (813) 442-2234

Semtronic Associates, Inc.
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Ft. Lauderdale, FL 33309
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FAX: (208) 343-9887

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Tel: (312) 790-9886
FAX: (312) 790-4078

Indiana
Fred Dorsey & Associates
3518 Eden Place
Carmel, IN 46032
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FAX: (317) 844-4843

Iowa
Electromec Sales
1500 2nd Avenue
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Cedar Rapids, IA 52403
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FAX: (319) 362-6535

Kansas
C-Tron
805 S Clairborne
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Tel: (913) 829-0073
FAX: (913) 829-0429

Maryland
Arbotek Associates
102 W. Joppa Road
Towson, MD 21204
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FAX: (301) 337-2781

Massachusetts
Mill-Bern Associates
2 Mack Road
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Tel: (617) 932-3311
FAX: (617) 932-0511

Michigan
Greiner Associates, Inc.
15324 E. Jefferson Avenue
Suite 12
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FAX: (313) 499-0665

■ Representatives — USA (Continued)

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1601 E Highway 13
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C-Tron
3910 Old Highway 94 South
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St. Charles, MO 63303
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FAX: (314) 447-5214

New Jersey
BGR Associates
Evesham Commons
525 Route 73
Suite 100
Marlton, NJ 08053
Tel: (609) 983-1020
FAX: (609) 983-1879

Technical Applications & Marketing
91 Clinton Road
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Fairfield, NJ 07006
Tel: (201) 575-4130
FAX: (201) 575-4563

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Quality Components
3343 Harlem Road
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Tel: (716) 837-5430
FAX: (716) 837-0662

Quality Components
116 Fayette Street
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FAX: (315) 682-2277

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Spectrum ESD
8925 Galloway Trail
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FAX: (414) 543-9288

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Tel: (416) 236-2355
FAX: (416) 236-3387

Pipe-Thompson Limited
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FAX: (613) 258-7649

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Tel: (36) 303029
Telex: 1773470 ONVIME

Representatives — Puerto Rico

Semtronic Associates
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3313 S. Memorial Highway
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California
Image Electronics
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Insight Electronics
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Marshall Industries
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El Monte, CA 91731
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Marshall Industries
336 Los Coches Street
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(408) 942-4600

Marshall Industries
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Rancho Cordova, CA 95670
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San Diego, CA 92131
(619) 578-9600

Merit Electronics
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San Jose, CA 95131
(408) 434-0800

Western Microtechnology
1637 North Brian
Orange, CA 92667
(714) 637-0200

Western Microtechnology
6837 Nancy Ridge Drive
San Diego, CA 92121
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Western Microtechnology
12900 Saratoga Ave.
Saratoga, CA 95070
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(203) 265-3822

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Orange, CT 06477
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(305) 977-4880

Milgray Electronics
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(407) 647-5747

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(813) 855-2351

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