SCSI

Small Computer Systems Interface

MB87030

Synchronous/Asynchronous Protocol Controller

Users Manual

FUJITSU

Fujitsu Limited

Fujitsu Microelectronics, Inc.

Fujitsu Mikroelektronik GmbH

Small Computer Systems Interface

MB87030

Synchronous/Asynchronous Protocol Controller

Users Manual

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information in this publication has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for any inaccuracies.

The information conveyed in this publication does not convey any license under the patent rights of Fujitsu Limited.

Fujitsu reserves the right to change specifications without notice.

MB87030 Synchronous/Asychronous Protocol Controller User's Manual is published by the U.S. Technical Publications Department, Fujitsu Microelectronics, 3320 Scott Blvd., Santa Clara, CA 95054-3197, (408) 727-1700 ext. 2414.

Printed in the U.S.A.

Edition 1.0 (Phase 1)

May, 1986

Fujitsu Limited
Furukawa Sogo Bldg., 6-1
Marunouchi 2-Chome, Chiyoda-ku
Tokyo 100, Japan
Phone National (03) 216-3211
Phone International 81-3-216-3211
Telex: 2224361 FT TOR J

Fujitsu Microelectronics, Inc.
3320 Scott Blvd.
Santa Clara, CA 95054-3197
Phone: (408) 727-1700
Telex: (910) 338-0190

Fujitsu Mikroelektronik GmbH
Arabella Center 9, OG/A
Lyoner Straβe 44-48 D-6000
Frankfurt 71, F.R. Germany
Phone 069/66 320
Telex 0411 963

PREFACE

The Fujitsu MB87030 (SPC: SCSI Protocol Controller) is a CMOS LSI circuit developed to control the small computer system interface (SCSI).

This manual explains the functions and use of the MB87030.

It consists of the following chapters:

To effectively apply this LSI circuit's functions, you must be familiar with SCSI functions and interface control procedures.

Note: Fujitsu reserves the right to change functions or characteristics to improve the design of the LSI circuit without prior notice.

CONTENTS

CONTENTS (Cont'd)

ILLUSTRATIONS AND TABLES

ILLUSTRATIONS

TABLES

CHAPTER 1

OUTLINE

1.1 GENERAL DESCRIPTION

The MB87030 (SPC: SCSI Protocol Controller) is a CMOS LSI circuit designed to make control of the small computer system interface (SCSI) easier. The MB87030, which can control all the SCSI interface signals and handle almost all the interface control procedures, can be used as a peripheral LSI circuit for an 8- or 16-bit MPU to realize high-level SCSI control. This LSI circuit has an 8-byte FIFO data buffer register and a transfer byte counter that is 24 bits long. Its wide range of applications allows not only asynchronous mode transfer but also synchronous mode transfer with an offset of 8 bytes at maximum. Furthermore, MB87030 can serve as either an INITIATOR or a TARGET device for the SCSI, and can therefore be used for either an I/O controller or a host adapter. (Note: In this manual, MB87030 is referred to as SPC)

1.2 FEATURES

- Full support for SCSI control
- Serves as either INITIATOR or TARGET device
- Synchronous mode transfer with a programmable offset, up to eight bytes
- Data transfer speed programmable at four rates (in synchronous mode transfer)
- Data transfer up to 4 MBPS allowed
- Eight-byte data buffer register incorporated
- Transfer byte counter, 24 bits long, incorporated
- Independent data transfer bus
- Applicable to the single-ended alternative and the differential alternative for SCSI
- Single +5 V supply
- Low power dissipation
- TTL-compatible inputs/outputs
- PGA 88-pin ceramic package

1.3 ELECTRICAL CHARACTERISTICS

1.3.1 Absolute Maximum Ratings*

Rating	Symbol	Min.	Max.	Unit
Supply Voltage	V_{DD}	V_{SS}** - 0.5	7.0	V
Input Voltage	V_I	V_{SS}** - 0.5	V_{DD} + 0.5	V
Output Voltage	V_O	V_{SS}** - 0.5	V_{DD} + 0.5	V
Storage Temperature (Ceramic)	T_{stg}	-65	+150	°C
Temperature Under Bias (Ceramic)	T_{bias}	-40	+125	°C
Output Current***	I_{OS}	-40	+70	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** V_{SS} = 0 V

*** Not more than one output may be shorted at a time for a maximum duration of one second.

1.3.2 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.2			V
Input Low Voltage	V_{IL}			0.8	V
Operating Temperature	T_A	0		70	°C

1.3.3 DC Characteristics
(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DDS}	Steady state *			100	µA
Power Dissipation	P_D			300		mW
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	4.2		V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA	V_{SS}		0.4	V
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{LI}	V_I=0 - V_{DD}	-10		10	µA
Input Leakage Current	I_{LZ}	3-state V_I=0 - V_{DD}	-10		10	µA

* Note: $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$

1.3.4 Capacitance
(T_A = 25 °C, $V_{DD} = V_I$ = 0 V, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}			9	pF
Output Pin Capacitance	C_{OUT}			9	pF
I/O Pin Capacitance	$C_{I/O}$			11	pF

1.4 PHYSICAL DIMENSIONS

The MB87030 is packaged in an 88-pin ceramic package. Figure 1.4.1 shows the dimensions of the package.

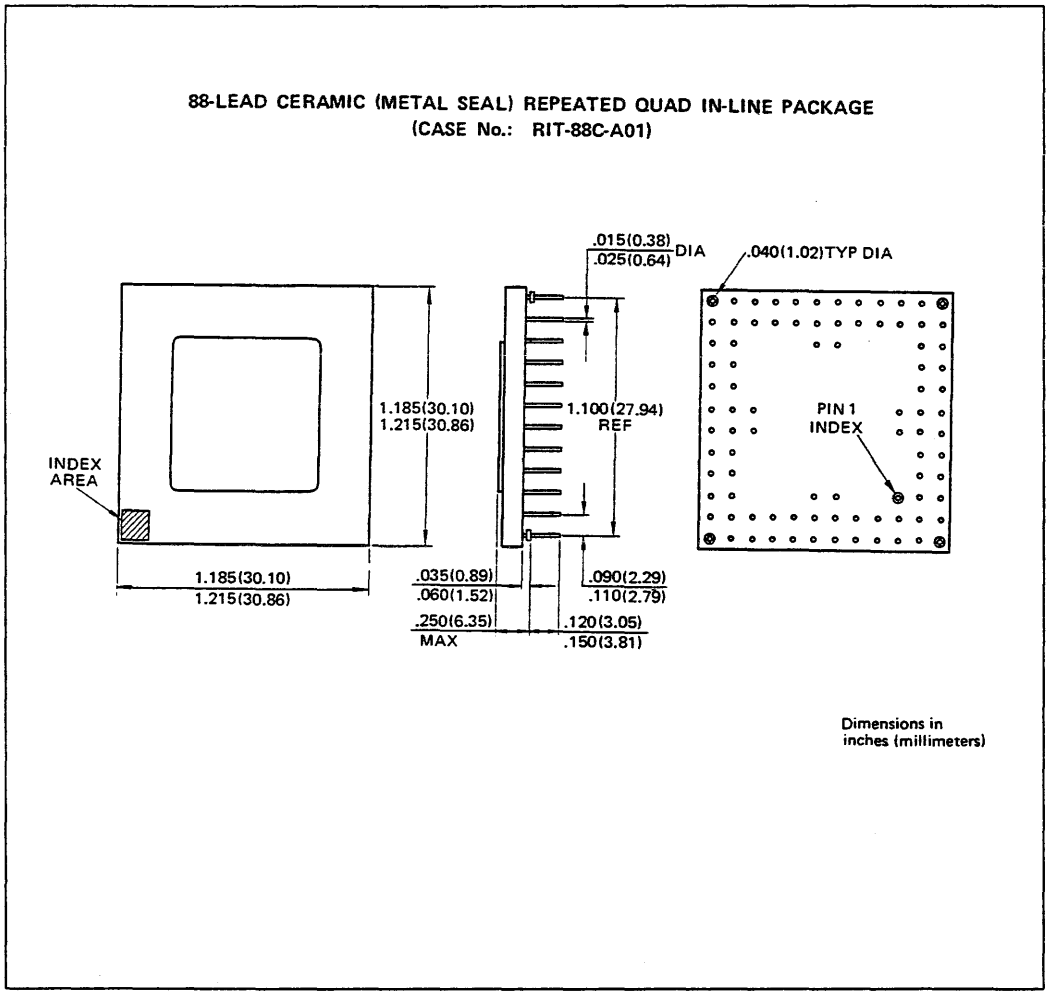


Figure 1.4.1 Dimensions of Package

CHAPTER 2

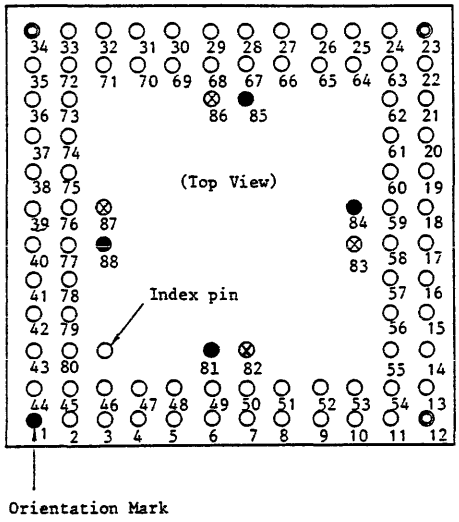
INPUT/OUTPUT TERMINALS

2.1 PIN ASSIGNMENTS

Figure 2.1.1 shows the arrangement of pins on this LSI.

2.2 INPUT/OUTPUT SIGNALS

Table 2.1.1 lists the input/output signals and their functions. In this table, the plus and minus signs have the following meaning:
+: Indicates an active-high signal.
−: Indicates an active-low signal.



No.	I/O	Signal name	No.	I/O	Signal name	No.	I/O	Signal name	No.	I/O	Signal name
1	I	HIN	23	O	SDBOP	45	I	A1	67	O	SDBE5
2	I/O	HDBO	24	O	SDBE7	46	I	A2	68	O	SDBE4
3	I/O	1	25	I	SDBI7	47	I	A3	69	I	SDBI4
4	I/O	2	26	O	SDBE6	48	I/O	D4	70	O	SDBO3
5	I/O	3	27	O	SDBO5	49	I/O	D5	71	I	SDBI2
6	I/O	4	28	I	SDBI5	50	I/O	D6	72	O	SDBO1
7	I/O	5	29	O	SDBO4	51	I/O	D7	73	O	SDBE0
8	I/O	6	30	O	SDBE3	52	I/O	DP	74	I	SDBI0
9	I/O	7	31	I	SDBI3	53	O	INTR	75	I	$\overline{RST}$
10	I/O	P	32	O	SDBO2	54	I	I/OI	76	O	DREQ
11	O	INIT	33	O	SDBE2	55	I	C/DI	77	I	$\overline{WT}$
12	O	TARG	34	I	SDBI1	56	I	SELI	78	I	$\overline{WIG}$
13	O	I/OO	35	O	SDBE1	57	I	MSG1	79	I/O	D2
14	O	C/DO	36	O	SDBOO	58	I	REQI	80	I/O	D3
15	O	SELO	37	I	$\overline{CS}$	59	I	RSTI	81	Power supply	VSS
16	O	MSGO	38	I	$\overline{CLK}$	60	I	ACKI	82	Power supply	VDD
17	O	REQO	39	I	$\overline{RD}$	61	I	BSYI	83	Power supply	VDD
18	O	RSTO	40	I	$\overline{RDG}$	62	I	ANTI	84	Power supply	VSS
19	O	ACKO	41	I	DRESP	63	I	SDBIP	85	Power supply	VSS
20	O	BSYO	42	I/O	D0	64	O	SDBO7	86	Power supply	VDD
21	O	ATNO	43	I/O	D1	65	O	SDBO6	87	Power supply	VDD
22	O	SDBEP	44	I	A0	66	I	SDBI6	88	Power supply	VSS

Figure 2.1.1 Pin assignments

Table 2.1.1 Input/output signals (Continued on next sheet)

Signal name	Polarity	I/O	Pin	Q'ty	Function
V_{DD}		I	82 83 86 87	4	+5 V power supply
V_{SS}		I	81 84 85 88	4	Ground (0 V)
$\overline{CLK}$	-	I	38	1	A clock input for controlling the SPC internal operation and the data transfer speed.
$\overline{RST}$	-	I	75	1	An asynchronous reset signal for clearing the internal circuits in SPC.
$\overline{CS}$	-	I	37	1	A selection enable signal for accessing an internal register in SPC. When this input signal is active, the following input/output signals are valid: $\overline{RD}$, $\overline{RDG}$ $\overline{WT}$, $\overline{WTG}$ A3 to A0 D7 to D0, DP
A3 A2 A1 A0	+	I	47 46 45 44	4	Address input signals for selecting an internal register in SPC. MSB: A3, LSB: A0 When $\overline{CS}$ input is active, read/write is enabled in an internal register selected by these address inputs via data bus lines D7 to D0 and DP.
$\overline{RD}$ $\overline{RDG}$	-	I	39 40	2	These strobe inputs are used for reading out the contents of the SPC internal register, and are effective only when $\overline{CS}$ input is active. While $\overline{RDG}$ input is active, the contents of an internal register selected by A3 to A0 inputs are placed on data bus lines D7 to D0 and DP. For a data transfer cycle in the program transfer mode, the trailing edge of $\overline{RD}$ input is used as a timing signal indicating the end of data read.
$\overline{WT}$	-	I	77	1	This strobe input is used for writing data into an SPC internal register, and is effective only when $\overline{CS}$ input is active. On the trailing edge of this signal, data placed on data bus lines D7 to D0 and DP are loaded into an internal register selected by A3 to A0 inputs. (Except when A3 = A2 = A1 = A0 = 'H') For a data transfer cycle in the program transfer mode, the trailing edge of this signal is used as a timing signal indicating data-ready state.
$\overline{WTG}$	-	I	78	1	While this signal is active, data placed on data bus lines D7 to D0 and DP are output to HDB7 to HDB0 and HDBP if the following input conditions are satisfied: $\overline{CS}$ = 'L' A3 = A2 = A1 = A0 = 'H' HIN = 'H'

Table 2.1.1 Input/output signals (Continued on next sheet)

<table>
<tr><th>Signal name</th><th>Polarity</th><th>I/O</th><th>Pin</th><th>Q'ty</th><th>Function</th></tr>
<tr><td>D7
D6
D5
D4
D3
D2
D1
D0
DP</td><td>+</td><td>I/O</td><td>51
50
49
48
80
79
43
42
52</td><td>9</td><td>Used for write/read data into/from an internal register in SPC. This data bus is three-state and bidirectional.
MSB: D7
LSB: D0
Odd parity bit: DP
When the $\overline{CS}$ and $\overline{RDG}$ inputs are active, the contents of the internal register are output to the data bus (read operation). In operations other than read, this data bus is kept at a high impedance level.</td></tr>
<tr><td>INTR</td><td>+</td><td>O</td><td>53</td><td>1</td><td>Requests an interrupt to indicate completion of SPC internal operation or occurrence of an error. Interrupt masking is allowed except for an interrupt caused by RSTI input (reset condition in SCSI). When an interrupt request is permitted, the INTR signal remains active until the cause of the interrupt is cleared.</td></tr>
<tr><td>SDBI7
SDBI6
SDBI5
SDBI4
SDBI3
SDBI2
SDBI1
SDBI0
SDBIP</td><td>+</td><td>I</td><td>25
66
28
69
31
71
34
74
63</td><td>9</td><td>Used as input from the SCSI data bus.
MSB: SDBI7
LSB: SDBI0
Odd parity bit: SDBIP
Parity checking for the SCSI data bus is programmable.</td></tr>
<tr><td>SDBO7
SDBO6
SDBO5
SDBO4
SDBO3
SDBO2
SDBO1
SDBO0
SDBOP</td><td>+</td><td>O</td><td>64
65
27
29
70
32
72
36
23</td><td>9</td><td>Used as outputs to the SCSI data bus.
MSB: SDBO7
LSB: SDBO0
Odd parity bit: SDBOP
If the bus driver is an open collector type, there signals can be supplied directly to the driver circuit. If the bus driver is a three-state type, these signals are used as data, and the SDBE7 to SDBE0 and SDBEP signals are used as drive enable signals.</td></tr>
<tr><td>SDBE7
SDBE6
SDBE5
SDBE4
SDBE3
SDBE2
SDBE1
SDBE0
SDBEP</td><td>+</td><td>O</td><td>24
26
67
68
30
33
35
73
22</td><td>9</td><td>Used as drive enable signals (corresponding to respective bit positions) where a three-state buffer is used for the SCSI data bus. SDBE7 to SDBE0 and SDBEP correspond to SDBO7 to SDBO0 and SDBOP, respectively. The relationship with SCSI bus phase is shown below.
<table>
<tr><th colspan="2" rowspan="2">SCSI bus phase</th><th colspan="2">SDBOn</th><th colspan="2">SDBEn</th></tr>
<tr><th>(ID)</th><th>($\overline{ID}$)</th><th>(ID)</th><th>($\overline{ID}$)</th></tr>
<tr><td colspan="2">BUS FREE</td><td>'L'</td><td>'L'</td><td>'L'</td><td>'L'</td></tr>
<tr><td colspan="2">ARBITRATION</td><td>'H'</td><td>'L'</td><td>'H'</td><td>'L'</td></tr>
<tr><td colspan="2">SELECTION/RESELECTION</td><td>D</td><td>D</td><td>'H'</td><td>'H'</td></tr>
<tr><td rowspan="2">Information transfer</td><td>SPC → SCSI</td><td>D</td><td>D</td><td>'H'</td><td>'H'</td></tr>
<tr><td>SPC ← SCSI</td><td>'L'</td><td>'L'</td><td>'L'</td><td>'L'</td></tr>
</table>
• (ID) indicates a bit position corresponding to the SCSI bus device ID, and ($\overline{ID}$) indicates other bit position.
• D denotes that a valid information is sent out.</td></tr>
</table>

Table 2.1.1 Input/output signals (Continued on next sheet)

<table>
<tr><th>Signal name</th><th>Polarity</th><th>I/O</th><th>Pin</th><th>Q'ty</th><th>Function</th></tr>
<tr><td>SELI
BSYI
REQI
ACKI
MSGI
C/DI
I/OI
ATNI
RSTI</td><td>+</td><td>I</td><td>56
61
58
60
57
55
54
62
59</td><td>9</td><td>Used for receiving SCSI control signals. The outputs of the SCSI receiver circuit can be connected directly.
Note: Waveform distortion or any other disturbance should not occur in the REQI and ACKI signals which are used as timing control signals for sequencing data transfer.</td></tr>
<tr><td>SELO
BSYO
REQO
ACKO
MSGO
C/DO
I/OO
ATNO
RSTO</td><td>+</td><td>O</td><td>15
20
17
19
16
14
13
21
18</td><td>9</td><td>Used for outputting SCSI control signals. The following signals become active only when SPC serves as a TARGET; otherwise, these signals are always low.
REQO, MSGO, C/DO, I/OO
The following signals become active only when SPC serves as an INITIATOR; otherwise, these signals are always low.
ACKO, ATNO</td></tr>
<tr><td>INIT
TARG</td><td>+</td><td>O</td><td>11
12</td><td>2</td><td>Used for indicating the SPC operation state. These signals are also available as control signals for the SCSI driver/receiver circuit.
<table>
<tr><th>INIT</th><th>TARG</th><th>Status</th></tr>
<tr><td>'L'</td><td>'L'</td><td>SPC is not connected with SCSI.</td></tr>
<tr><td>'L'</td><td>'H'</td><td>SPC is executing RESELECTION phase, or is operating as a TARGET.</td></tr>
<tr><td>'H'</td><td>'L'</td><td>SPC is executing SELECTION phase, or is operating as an INITIATOR.</td></tr>
</table></td></tr>
<tr><td>DREQ</td><td>+</td><td>O</td><td>76</td><td>1</td><td>At a data transfer cycle in DMA mode, the DREQ signal is used to indicate a request for data transfer between SPC and the external buffer memory. In DMA mode, data is routed as shown below.
• Output operation
External buffer memory
↓
HDB7 to HDB0, and HDBP pins
↓
SPC internal data buffer register (8 bytes)
↓
SDBO7 to SDBO0 and SDBOP pins
↓
(SCSI)</td></tr>
</table>

Table 2.1.1 Input/output signals (Continued)

Signal name	Polarity	I/O	Pin	Q'ty	Function
					• Input operation (SCSI) ↓ SDBI7 to SDBI0 and SDBIP pins ↓ SPC internal data buffer register (8 bytes) ↓ HDB7 to HDB0 and HDBP pins ↓ External buffer memory ↓ In an output operation, this signal becomes active to request data transfer from the external buffer memory when the SPC internal data buffer register has free space available. In an input operation, it becomes active to request data transfer to the external buffer memory when the SPC internal buffer register contains valid data.
DRESP	+	I	41	1	Used as an response signal to the above data transfer request signal (DREQ) in DMA mode data transfer cycle. Pin DRESP must be supplied with a pulse signal at the end of each byte that is transferred. In an output operation, SPC uses the trailing edge of the DRESP signal for sampling data on HDB7 to HDB0 and HDBP bus lines. In an input operation, SPC holds data to be transferred onto HDB7 to HDB0 and HDBP bus lines until the trailing edge of the DRESP signal.
HDB7 HDB6 HDB5 HDB4 HDB3 HDB2 HDB1 HDB0 HDBP	+	I/O	9 8 7 6 5 4 3 2 10	9	Three-state, bidirectional data bus for transferring data to/from the external buffer memory in DMA mode data transfer cycle. MSB: HDB7 LSB: HDB0 Odd parity bit: HDBP The data transmission direction depends on the HIN input signal. HIN HDBn Operation 'L' Input mode Output 'H' Output mode Input
HIN	+	I	1	1	This signal indicates transmission direction along data bus lines HDB7 to HDB0 and HDBP in DMA transfer mode. Transmission direction must be coordinated with the SPC internal operation to be executed. When the HIN signal is low, data bus lines HDB7 to HDB0 and HDBP are put in the high impedance state (input mode). When the HIN signal is high, they are put in the output mode.

CHAPTER 3

FUNCTIONS

3.1 FUNCTIONAL BLOCKS

Figure 3.1.1 shows the SPC functional block diagram.
SPC mainly consists of the following functional blocks:

(1) Internal register block
(2) MPU interface control block
(3) Bus phase control block
(4) Arbitration/selection sequence control block
(5) Transfer sequence control block
(6) Transfer byte counter block
(7) Data buffer register block

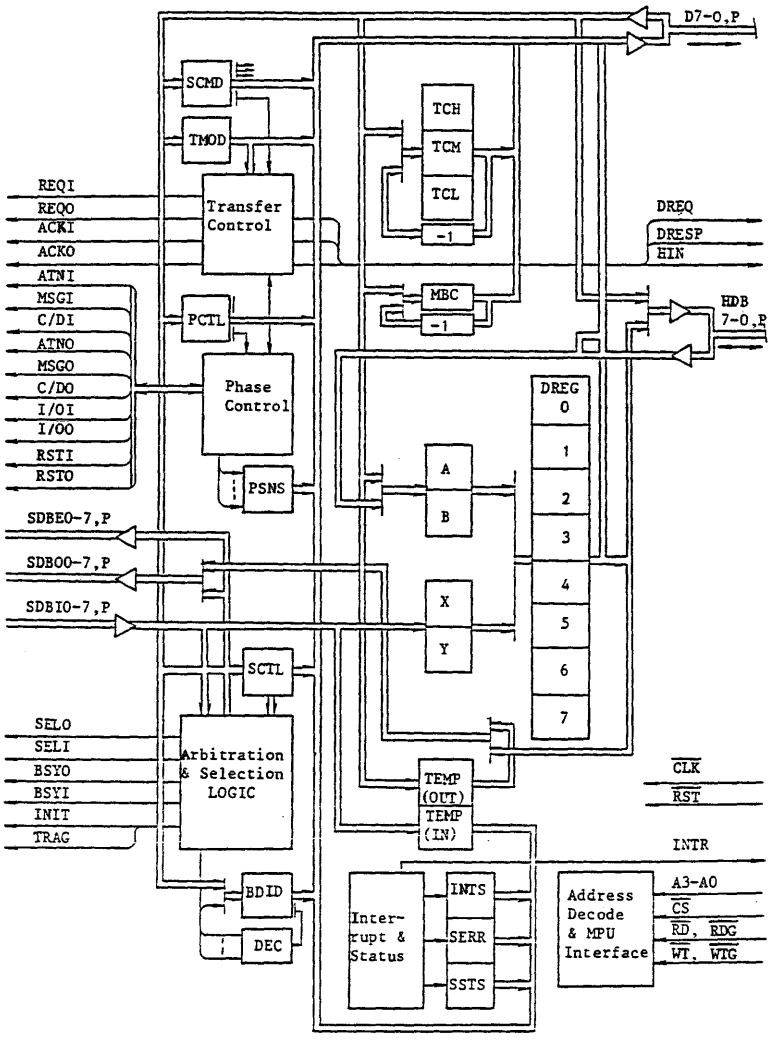


Figure 3.1.1 SPC functional block diagram

3.2 INTERNAL REGISTER

SPC has internal registers consisting of 17 bytes that are accessible from an external circuit. These internal registers are used for controlling SPC internal operation and indicating SPC processing status/result status.

3.2.1 Addressing

A unique address is assigned to each internal register, and a particular register is identified by address bits A3 to A0. Table 3.2.1 shows internal register addressing.

3.2.2 Internal Register Assignments

Table 3.2.2 shows the bit assignment to each internal register.
When accessing an internal register (in read/write), remember the following:

(1) The internal register block includes the read-only/write-only register and those having different meanings in read and write operations.
(2) A write to the read-only register is ignored.
(3) If the write-only register is read out, the data and parity bit are undefined.
(4) At bit positions indicating "____" for a write in Table 3.2.2, either 1 of 0, or may be written.

Table 3.2.1 Internal register addressing

$\overline{CS}$	A3	A2	A1	A0	OP	Register Name	Abbr.
0	0	0	0	0	R/W	Bus Device ID	BDID
0	0	0	0	1	R/W	SPC Control	SCTL
0	0	0	1	0	R/W	Command	SCMD
0	0	0	1	1	R/W	Transfer Mode	TMOD
0	0	1	0	0	R	Interrupt Sense	INTS
					W	Reset Interrupt	
0	0	1	0	1	R	Phase Sense	PSNS
					W	SPC Diagnostic Control	SDGC
0	0	1	1	0	R	SPC Status	SSTS
					W	---	
0	0	1	1	1	R	SPC Error Status	SERR
					W	---	
0	1	0	0	0	R/W	Phase Control	PCTL
0	1	0	0	1	R	Modified Byte Counter	MBC
					W	---	
0	1	0	1	0	R/W	Data Register	DREG
0	1	0	1	1	R/W	Temporary Register	TEMP
0	1	1	0	0	R/W	Transfer Counter High	TCH
0	1	1	0	1	R/W	Transfer Counter Middle	TCM
0	1	1	1	0	R/W	Transfer Counter Low	TCL
0	1	1	1	1	R/W	External Buffer	EXBF

Table 3.2.2 Internal register bit assignment (Continued on next sheet)

No.	Name (Abbr.)	OP	7	6	5	4	3	2	1	0	P
1	Bus Device ID (BDID)	R	SCSI Bus Device ID								
			#7	#6	#5	#4	#3	#2	#1	#0	'0'
		W	—					SCSI Bus Device ID			—
								ID4	ID2	ID1	
2	SPC Control (SCTL)	R	Reset and Dis-able	Control Reset	Diag Mode	ARBIT Enable	Parity Enable	Select Enable	Reselect Enable	INT Enable	P
		W									
3	Command (SCMD)	R	Command Code			RST Out	Inter-cept Xfer	Transfer Modifier			P
		W						PRG Xfer	'0'	Term. Mode	
4	Transfer Mode (TMOD)	R	Sync. Xfer	Max. Transfer Offset			Min. Transfer Period		'0'	'0'	P
		W		4	2	1	2	1			
5	Phase Control (PCTL)	R	Bus Free Inter-rupt Enable	'0'				Transfer Phase			P
		W						MSG Out	C/D Out	I/D Out	
6	Phase Sense (PSNS)	R	REQ	ACK	ATN	SEL	BSY	MSG	C/D	I/O	P
		W	—								—
7	Data Register (DREG)	R	Internal Data Register (8 Byte FIFO)								P
		W	Bit7	6	5	4	3	2	1	0	
8	Transfer Counter High (TCH)	R	Transfer Counter High (MSB)								P
		W	Bit23	22	21	20	19	18	17	16	
9	Transfer Counter Mid. (TCM)	R	Transfer Counter Middle (2nd Byte)								P
		W	Bit15	14	13	12	11	10	9	8	
10	Transfer Counter Low (TCL)	R	Transfer Counter Low (LSB)								P
		W	Bit7	6	5	4	3	2	1	0	
11	Interrupt Sense (INTS)	R	Sele-cted	Rese-lected	Dis-Con-nected	Com-mand Com-plete	Ser-vice Re-quired	Time Out	SPC Hard Error	Reset Condi-tion	P
		W	Reset Interrupt								—
12	SPC Status (SSTS)	R	Connected		SPC Busy	Xfer in Pro-gress	SCSI RST	TC=0	DREG Status		P
			INIT	TARG					FULL	EMPTY	
		W	—								—

Table 3.2.2 Internal register bit assignment (Continued)

No.	Name (Abbr.)	OP	7	6	5	4	3	2	1	0	P
13	SPC Error Status (SERR)	R	Data Error SCSI	Data Error SPC	'0'	'0'	TC P-Error	Phase Error	Short Period	Offset Error	P
		W	—								—
14	Temporary Register (TEMP)	R	Temporary Data (Input: From SCSI) Bit7	6	5	4	3	2	1	0	P
		W	Temporary Data (Output: to SCSI) Bit7	6	5	4	3	2	1	0	P
15	External Buffer (EXBF)	R	External Buffer								P
		W	Bit7	6	5	4	3	2	1	0	
16	Modified Byte Counter (MBC)	R	'0'				MBC Bit3	2	1	0	P
		W	—								—
17	SPC Diagnostic Control (SDGC)	R	—								—
		W	Diag REQ	Diag ACK	—		Diag BSY	Diag MSG	Diag C/D	Diag I/O	—

3.3 MAJOR OPERATIONS

3.3.1 MPU Interface Control Block

The MPU interface control block selects a specified internal register and controls a read/write operation. Also, this block generates an interrupt and indicates its cause. (This is done to report the result status of SPC internal operation, and the detection of an error, if encountered.)

3.3.2 Bus Phase Control Block

The bus phase control block generates a specified bus phase for SCSI and controls its sequence of executions. Also, this block supervises SCSI status, and responds to the bus phase being executed if necessary.

3.3.3 Arbitration/Selection Sequence Control Block

This sequence control block executes the ARBITRATION phase with the SCSI-specified timing and obtains permission to use the SCSI bus. Then, it carries out the SELECTION/RESELECTION phase and checks the response from the selected/reselected device. Also, this block detects the SELECTION/RESELECTION phase on SCSI, and checks the bus device ID specified in the internal register against that specified on the SCSI data bus. Then, if this block finds that SPC has been selected by another SCSI bus device, it executes the response sequence for the SELECTION/RESELECTION phase.

3.3.4 Transfer Sequence Control Block

This sequence control block controls the DATA IN/OUT, COMMAND, STATUS, and MESSAGE IN/OUT phases to be executed in SCSI. The following two modes are available for execution of these transfer phases:

(1) Manual transfer mode
In manual transfer mode, the MPU interface is used for transferring data and sending/receiving/checking the REQ/ACK signals on SCSI.

(2) Hardware transfer mode
In hardware transfer mode, SPC controls the SCSI transfer sequence according to the transfer mode and transfer byte count specified in the internal registers, and reports the end result of transfer. Asynchronous and synchronous mode transfer operations can be executed. In the asynchronous mode transfer operation, the REQ and ACK signals are controlled by the interlock protocol. In the synchronous mode transfer operation, a maximum of eight-byte offset is available for the DATA IN/OUT phase. The hardware transfer mode is subdivided into two according to the data routing:

(a) Program transfer mode
Data is routed via MPU interface in the following data paths:
SCSI ↔ Data buffer register ↔ Data bus lines D7 to D0 and DP.

(b) DMA mode
Data is routed using DREQ and DRESP signals for DMA control in the following data paths:
SCSI ↔ Data buffer register ↔ Data bus lines HDB7 to HDB0 and HDBP.

3.3.5 Transfer Byte Counter Block

This counter indicates the transfer byte count used for hardware transfer mode operation in SPC. It consists of 24 bits. Except for execution of a special transfer operation (padding), the transfer byte counter is decresed by one each time one byte of data is transferred on SCSI. The transfer byte counter is also used as a timer for supervising the waiting time for a response to be returned from the selected SCSI bus device during execution of the selection/reselection phase. On the MPU interface, the transfer byte counter is treated as three separate internal registers (TCH, TCM, TCL), each being one byte long.

3.3.6 Data Buffer Register Block

The data buffer register block is used in execution of a hardware transfer mode operation in SPC. It has a capacity of eight bytes, and operates on the FIFO principle for each byte. In an input operation (from SCSI to SPC), data received from SCSI is loaded into the buffer register. In DMA mode, transfer request signal DREQ is generated to the external buffer memory. Also, in program transfer mode, data can be read out from this buffer register. In an output operation (from SPC to SCSI), data supplied from the MPU interface (program transfer mode) or external buffer memory (DMA mode) is loaded into the buffer register and then sent to SCSI. In this case, a maximum of eight bytes of data is prefetched into SPC. The MPU interface treats 8-byte data buffer register as if it was a one-byte internal register. In an input operation, the byte locations holding valid data are selected in succession for reading out. In an output operation, the empty byte locations are selected in succession for writing in.

CHAPTER 4

OPERATIONAL DESCRIPTION

4.1 BDID REGISTER

OP	7	6	5	4	3	2	1	0	P
R	Bit Significant Bus Device ID								
	#7	#6	#5	#4	#3	#2	#1	#0	'0'
W	—					SCSI Bus Device ID			
						ID4	ID2	ID1	—

Write Operation (Bits 2 to 0):

The BDID register specifies an SCSI bus device identifier (ID) with a three-bit binary number. This setting must be completed before resetting the SCTL register's bit 7 (Reset & Disable). Bits 2 to 0 are not affected by any resetting except power on reset.

Read Operation:

The BDID register indicates an SCSI physical device address (bus device ID) with each bit. An SCSI physical device address is decoded from the values at bits 2 to 0 specified in a write operation to the BDID register described above. One of the bits is 'one', the others are all 'zeros'. The SCSI bus usage priority is assigned in descending order from bit 7 to bit 0. Using a bus device ID indicated in this register, SPC executes the ARBITRATION phase. Also, if a SELECTION/RESELECTION phase condition occurs in SCSI, the value of the SCSI data bus is checked against the contents of this register to see whether the SPC has been selected/reselected or not.

4.2 SCTL REGISTER

OP	7	6	5	4	3	2	1	0	P
R	Reset & Disable	Control Reset	Diag Mode	ARBIT Enable	Parity Enable	Select Enable	Reselect Enable	INT Enable	P
W									

Bit 7: Reset & Disable

Bit 7 indicates a reset instruction to the internal registers and control circuits in SPC. When this bit is 1, SPC is reset and logically disconnected from SCSI (put in the disable state). Execution of the hardware reset ($\overline{RST}$ input = 'L') causes this bit to be 1. To enable the SCSI operation, bit 7 must be made zero to release the disable state.

Bit 6: Control Reset

Bit 6 instructs resetting of the data transfer control circuit in SPC. That is, the data transfer control circuit is reset when this bit is 1. Even if the control reset is executed by this bit during the SPC operates with SCSI, the SPC keeps connected state with SCSI. The reset function of this bit should be used for resetting the data transfer control circuit while it is connected with SCSI. More specifically, it should be used when an error is indicated by bit 1 (SPC Hardware Error) of the INTS register during execution of the SCSI transfer phase or when a timeout occurs before completion of Transfer command execution (supervised by the MPU program). Bit 1 (SPC Hardware Error) of the INTS register and the SERR register are cleared by the reset function of this bit.

Note: This reset function initializes the SPC transfer control circuit. So, when the SPC serves as an INTIATOR, the following consideration is required:

- Since the REQ signal may be received during resetting, the first byte should be transferred in manual mode after resetting.

Bit 5: Diagnostic Mode

When bit 5 is 1, SPC enters a diagnostic mode and is disconnected from SCSI. A diagnostic mode allows pseudo-execution of the SCSI operation using the SDGC register (to be explained later).

Bit 4: Arbitration Enable

Bit 4 indicates whether the ARBITRATION phase is executable in SCSI or not.
1 ... ARBITRATION phase executable
0 ... ARBITRATION phase nonexecutable
With this bit set to 1, the Select command causes SPC to execute the ARBITRATION phase. And, if the SPC win the arbitration, it executes the SELECTION/RESELECTION phase. With this bit set to 0, the Select command causes SPC to execute the SELECTION phase without the ARBITRATION phase. As long as bit 4 is 0, SPC returns no response to a reselection request from other SCSI bus device. That is, no response is made even if bit 1 (Reselect Enable) of this register is set to 1. Remember that bit 4 must be set correctly before clearing bit 7 (Reset & Disable) of the SCTL register. Note also that this bit should not be changed in other than a diagnostic mode after clearing bit 7 of the SCTL register.

Bit 3: Parity Enable

Bit 3 indicates whether the parity of data received from the SCSI data bus is to be checked or not.
1 ... Parity of the data received from the SCSI data bus is checked.
0 ... Parity of the data received from the SCSI data bus is not checked.
Regardless of the value of this bit, the parity of the data to be sent to the SCSI data bus is ensured. Also, the parity of the data on the SPC internal data bus is always checked. While SPC is connected with SCSI, this bit should not be changed.

A parity check is carried out in the following cases:

(1) When checking an ID value placed on the data bus upon detection of the SELECTION/RESELECTION phase in SCSI:
Detection of a parity error causes no response to the SELECTION/RESELECTION phase even if the SCSI bus device ID has been matched.

(2) When receiving data from SCSI in an input transfer sequence:
If a parity error is detected in a data byte, the relevant parity bit value is corrected and the data byte with the corrected parity is sent to the MPU/DMA data bus.

Bit 2: Select Enable

1 ... SPC responds as a TARGET device to the SELECTION phase in SCSI.
0 ... SPC does not respond to the SELECTION phase in SCSI.

Note: If SPC has already detected the SELECTION phase during an attempt to set this bit to 0, SPC responds to the SELECTION phase as a TARGET device. In this case, the 0 setting is effective for the subsequent SELECTION phase (with no response).

Bit 1: Reselect Enable

1 ... SPC responds as an INITIATOR to the RESELECTION phase in SCSI.
0 ... SPC does not respond to the RESELECTION phase in SCSI.

Note: If SPC has already detected the RESELECTION phase during an attempt to set this bit to 0, SPC responds to the RESELECTION phase as an INITIATOR. In this case, the 0 setting is effective for the subsequent RESELECTION phase (with no response).

Bit 0: Interrupt Enable

Bit 0 serves as a mask for enabling/disabling an interrupt (INTR) output from the SPC.

1 ... Interrupt enabled
0 ... Interrupt disabled

An interrupt due to a RESET condition detected in SCSI cannot be masked. Regardless of the value of this bit, an interrupt event is always indicated in the INTS register. This makes available poll-mode control in an interrupt disabled state.

4.3 SCMD REGISTER

OP	7	6	5	4	3	2	1	0	P
R / W	Command Code			RST Out	Inter-cept Xfer	Transfer Modifier PRG Xfer	'0'	Term. Mode	p

4.3.1 Register Functions

The SCMD register is used for giving a command to SPC. Writing into this register causes SPC to initiate the command processing specified at bits 7 to 5.

Bit 7 to 5: Command Code

Bit 7	6	5	Command
0	0	0	Bus Release
0	0	1	Select
0	1	0	Reset ATN
0	1	1	Set ATN
1	0	0	Transfer
1	0	1	Transfer Pause
1	1	0	Reset ACK/REQ
1	1	1	Set ACK/REQ

Bit 4: RST Out

If bit 7 (Reset & Disable) of the SCTL register is 0, setting 1 in bit 4 of this SCMD register sends the RST signal (RSTO pin) to SCSI. When bit 4 is set to 1, a command being executed or waiting for execution in SPC is cleared and all signals to SCSI other than RST are deactivated. To ensure for the SCSI timing requirements, MPU must maintain this bit at 1 for more than 25 microseconds.

Note: If the RST signal (RSTI pin) is received from SCSI with this bit set to 0, the operation sequence is as follows:

- A command being executed or waiting for execution in the SPC is cleared.
- All signals to the SCSI are deactivated.
- An interrupt condition (non-maskable) is generated.

Whenever bit 7 (Reset & Disable) of the SCTL register is 0, the SPC always accepts the RST signal from the SCSI.

Bit 3: Intercept Transfer

Bit 3 specifies the special data transfer mode. It is valid only when SPC serves as an INITIATOR.

This bit should be set to 1 together with the Set ATN, Set ACK/REQ, or Bus Release command (Bus Release command has no effect when SPC has been connected with SCSI as an INITIATOR). And, this bit should be reset together with the Reset ACK/REQ command. (When two or more bytes are transferred using the Set ACK/REQ and Reset ACK/REQ commands, this bit must be reset on issuance of the Reset ACK/REQ command for the last byte.) With bit 3 of SCMD register set to 1, executing manual transfer (MPU-controlled transfer using the Set ACK/REQ and Reset ACK/REQ commands) does not change the contents of the eight-byte data buffer register in SPC. Therefore, if a TARGET changes bus phase to such as MESSAGE IN during execution of the DATA OUT phase, this intercept transfer mode makes it possible to optionally restart the DATA OUT phase at the end of the interrupting phase. The phase change during transfer execution is reported by a 'service required' interrupt. To execute this intercept transfer mode, bit 3 of SCMD register must be set to 1 prior to the resetting of an interrupt (an interrupt must be reset after bit 3 is set to 1). Even when not using the intercept transfer mode, bit 3 may be specified for resetting a 'service required' interrupt. In this case, bit 3 must be set/reset together with the Bus Release command. For more details, see the description of bit 3 (Service Required) of the INTS register.

Bits 2 to 0: Transfer Modifier

Bits 2 to 0 are used as a field for specifying the execution mode of the information transfer phase. A value must be set in this field when the Transfer command is issued. If any of the following commands are issued during execution of the Transfer command, this field's value must not be changed:

- Set ATN
- Transfer Pause
- Reset ACK/REQ

Bit 2: Program Transfer

1 ... Data is transferred between the MPU and the data buffer register in SPC.

0 ... Data is transferred in the DMA mode in which the SPC signals a transfer request to the external buffer memory.

Bit 1: Unused

Bit 1 must always be set to 0.

Bit 0: Termination Mode

Bit 0 provides different functions depending on the SPC operation mode. When SPC serves as an INITIATOR, bit 0 specifies the following operations:

1 ... Even after the transfer byte counter reaches 0 during execution of the Transfer command, data transfer is continued if the REQ signal arrives from a TARGET in the same phase. if an output operation is in progress, all 0 bits (with a parity bit set to 1) are transmitted as data. During an input operation, the received data is ignored. But parity is checked if it is enabled (Parity Enable). The above data transfer is referred to as padding transfer, which is effective only when the DATA IN or DATA OUT phase is executed. Padding transfer is executed only within SPC, and a transfer request is not signalled to the external buffer memory even if the DMA transfer mode is specified. Padding transfer is maintained until a TARGET changes the bus phase. In the padding transfer mode, if the Transfer command is issued with the initial value of the transfer byte counter set to 0, execution of padding transfer is started with the first byte. To carry out an output operation in this case, the TEMP register must be set to X'00' prior to issuance of the Transfer command.

0 ... Transfer command execution terminates when the transfer byte counter reaches 0. The Transfer command must be reissued for receiving the next REQ signal from a TARGET.

When SPC serves as a TARGET, bit 0 specifies the following operations:

1 ... If a parity error is detected in the received data during execution of the Transfer command for input, the current transfer sequence is immediately stopped to terminate Transfer command execution.

0 ... Even if a parity error is detected in the received data during execution of the Transfer command for input, the current transfer sequence is continued until the transfer byte counter reaches 0.

4.3.2 Command Functions

(1) Bus Release command
When SPC acts as a TARGET role, the Bus Release command instructs a transition to the BUS FREE phase. During execution of the information transfer phase, the Transfer Pause command must be issued to halt the data transfer operation prior to this command. Otherwise, the SCSI bus sequence is not ensured. The Bus Release command may also be used to cancel the Select command waiting for the bus to become free. Note that the Bus Release command is ignored if SPC has already started the ARBITRATION or SELECTION phase.

(2) Select command
The select command requests the SELECTION/RESELECTION phase to be started. It shall be issued only when the SPC is not connected with SCSI. When the SPC receives this command, it carries out the following operation upon detection of the BUS FREE phase is SCSI.

a. When bit 4 (Arbitration Enable) of the SCTL register is set to 1:
After the BUS FREE phase has been detected, SPC executes the ARBITRATION phase to try to obtain bus usage permission. If the SPC has lost the arbitration, the Select command terminates its execution. If the SPC has won the arbitration, SPC executes the SELECTION or RESELECTION phase. The SELECTION phase is executed when bit 0 (I/O Out) of the PCTL register is set to 0, and the RESELECTION phase is executed when it is set to 1.

b. When bit 4 (Arbitration Enable) of the SCTL register is set to 0:
After the BUS FREE phase has been detected, SPC executes the SELECTION phase.

Before this command is issued, the following settings must be made in either of the above cases:

a. PCTL register
Specify the phase to be executed at bit 0 (I/O Out).
0 ... SELECTION phase to be executed
1 ... RESELECTION phase to be executed
Note that whenever bit 4 (Arbitration Enable) of the SCTL register is set to 0, the SELECTION phase is executed regardless a value of bit 0 (I/O Out) of the PCTL register.

b. Set ATN command
Issue the Set ATN command if it is required to assert an ATN signal at the SELECTION phase.

c. TEMP register
In the TEMP register, specify a value to be sent to the SCSI data bus during execution of the SELECTION/RESELECTION phase.

d. TCH and TCM registers
Specify a response (BSY signal) waiting supervisory time for execution of the SELECTION/RESELECTION phase. The supervisory time T_{SL} should be calculated as follows:
Assuming that the value of TCH and TCM is N (MSB: TCH, LSB: TCM);
When N does not equal 0, $T_{SL} = (N \times 256 + 15) \times T_{CLF} \times 2$. When N equals 0, T_{SL} = infinite. Where, T_{CLF} is a cycle time of the clock signal supplied to the $\overline{CLK}$ pin of SPC.

e. TCL register
Specify a period of time (T_{WAIT}) from the moment when both BSY and SEL signals become inactive on SCSI upon detection of the BUS FREE phase to the moment when SPC initiates the ARBITRATION/SELECTION phase. Parameters (X'00') to (X'0F') can be specified in the TCL register. The average TWAIT value can be derived using the following equation:

$T_{WAIT} = [(TCL + 6] \times T_{CLF}$ $[(TCL) + 7] \times T_{CLF}$
Where,

(TCL): A set value in the TCL register.

T_{CLF}: A cycle time of the clock signal supplied to the $\overline{CLK}$ pin of SPC.

Table 4.3.1 lists the values recommended to be set in the TCL register.

Table 4.3.1 Values recommended to be set in TCL register for use of Select command

T_{CLF} (ns)	TCL	T_{WAIT} (average) (ns)
125 - 180	$(04)_{16}$	1,250 - 1,980
140 - 200	$(03)_{16}$	1,260 - 2,000

In ARBITRATION phase execution by the Select command, the bus device identifier (ID) which is sent to the SCSI data bus is the value specified in the BDID register. The following equation can be used to obtain the period of time (TARB) required from the moment when the arbitration is started (BSY signal assertion) to the moment when the bus usage priority is examined:

$T_{ARB} = 32 \times T_{CLF}$
Where, T_{CLF} indicates a cycle time of the clock signal supplied to the $\overline{CLK}$ pin of SPC. After SELECTION/RESELECTION phase execution is started, a time-out interrupt occurs if no response is acknowledged within the supervisory time specified in the TCH and TCM registeres. When a time-out interrupt occurs, the SPC holds the current execution state of SELECTION/RESELECTION phase for SCSI. However, until the time-out interrupt condition is reset, SPC executes no operation to the response from the bus device being selected. Either of the following procedures can be used for a time-out interrupt:

a. Restart of SELECTION/RESELECTION phase
After specifying a new supervisory time in the TCH, TCM and TCL registers, reset the time-out interrupt condition. Then, SPC will restart the SELECTION/RESELECTION phase in progress. At this time, changing the TEMP register contents can alter the value being sent to the SCSI data bus.
New supervisory time T_{SL}' is expressed as follows:
Assuming TCH, TCM and TCL value to be N' (MSB: TCH, LSB: TCL);
$T_{SL}' = N' \times T_{CLF} \times 2$ $(N' \neq 0)$
Where, T_{CLF} indicates a cycle time of the clock signal supplied to $\overline{CLK}$ pin of the SPC.

b. Termination of SELECTION/RESELECTION phase
When a time-out interrupt occurs, the values of TCH, TCM and TCL registers are 0. Resetting the time-out interrupt condition in this state causes SPC to deactivate all signals to SCSI and terminate the SELECTION/RESELECTION phase unless the BSY signal is returned. If the BSY signal is returned when the interrupt condition is being reset, then SPC executes a normal sequence to complete the Select command. To reset a time-out interrupt condition, set bit 2 of the INTS register to 1. If the Select command has been issued with initial setting of 0 for TCH and TCM registers, the time-out interrupt does not occur. However, the above time-out interrupt resetting procedure must be carried out to terminate the SELECTION/RESELECTION phase in progress. If SPC recognizes a response from the selected/reselected device during SELECTION/RESELECTION phase execution, SPC executes an interface sequence to serve as an INITIATOR (at SELECTION phase) or TARGET (at RESELECTION phase), then SPC is connected with SCSI as a relevant role. When the Select command is issued, the SPC status is indicated in the SSTS register. Figure 4.3.1 shows the status transitions.

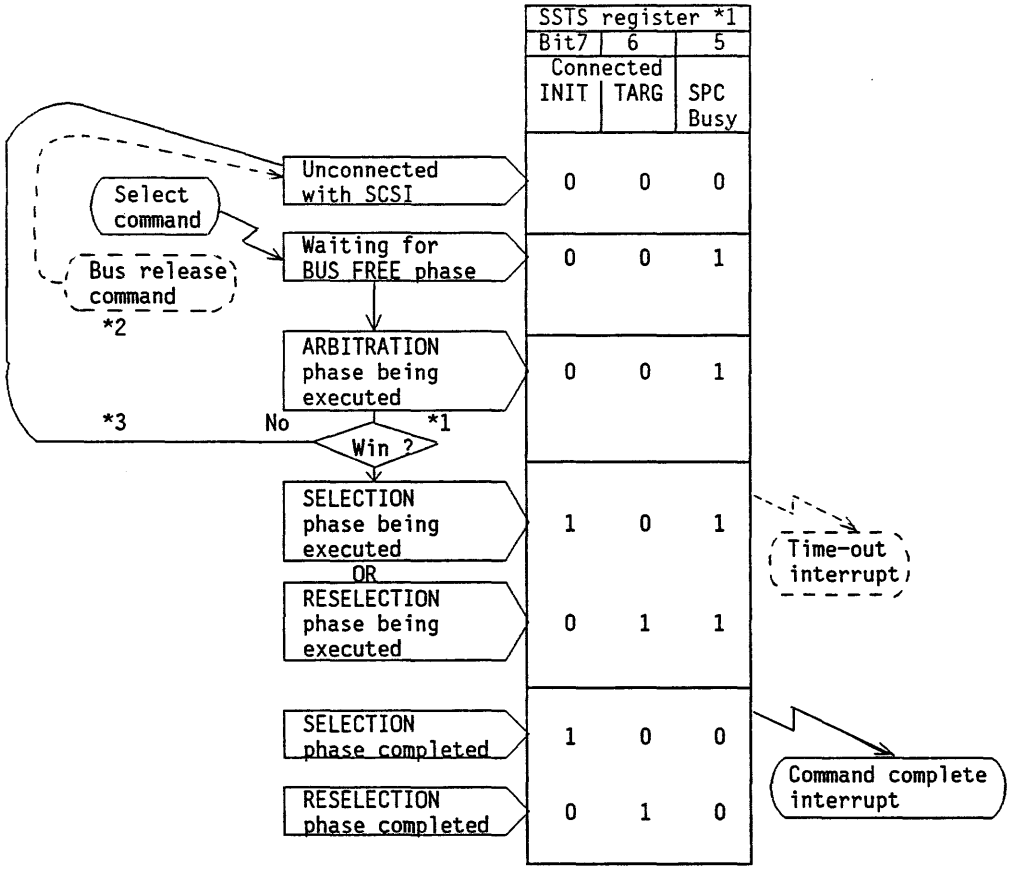


Fig. 4.3.1 Status transitions in Select command execution

*1: Check the SPC status after the elapsed time (shown below) following issuance of the Select command:
(1) If Arbitration Enable bit is set to 0 the minimum waiting time is 22 x (Clock cycle: T_{CLF})
(2) If Arbitration Enable bit is set to 1 the minimum waiting time is (55 + Set value in TCL) x (Clock cycle: T_{CLF})

*2: The Select command waiting for BUS FREE phase can be canceled using the Bus Release command. However, if the bus becomes free simultaneously with issuance of the Bus Release command, the Select command remains valid to execute the ARBITRATION and SELECTION/RESELECTION phases. The MPU program must make sure that the Select command has been canceled after more than four clock cycles passed since the Bus Release command (write to SCMD register) was issued.

*3: If the SPC lost the arbitration, the Select command terminates automatically (a command complete interrupt does not occur). In this case, note that the TCL register contents are unpredictable. When issuing the Select command again, be sure to specify the relevant value (see (2)-e, TCL register in Section 4.3.2) again in the TCL register.

(3) Set ATN command

The Set ATN command is valid only when the SPC will act as an INITIATOR role. If this command is issued prior to the Select command, the ATN signal is sent to SCSI at SELECTION phase execution. If the Set ATN command is issued while the SPC is connected with SCSI as an INITIATOR, the ATN signal is sent to SCSI immediately. When the parity checking for the SCSI data bus is enabled and SPC detects a parity error in the data received from SCSI (during execution of the input transfer operation in hardware transfer mode), the ATN signal is sent to SCSI regardless of the Set ATN command. (See Figure 4.3.2) The assertion of ATN signal is retained until the condition described on item (4) Reset ATN command in this section is satisfied. However, the ATN signaling condition held in SPC, by the Set ATN command issued prior to the Select command, is cleared, if:

a. the Select command is canceled by the Bus Release command, or
b. a selected/reselected interrupt occurs before execution of the SELECTION phase.

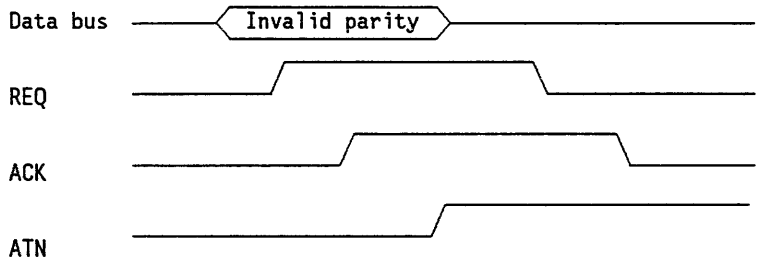


Fig. 4.3.2 ATN signal generation in data transfer

(4) Reset ATN command

The Reset ATN command is used to reset the ATN signal being sent to SCSI. If SPC generates an ATN signal (due to a parity error in the received data) during execution of the hardware transfer mode operation, do not issue this command to reset the ATN signal until execution of the current Transfer command has completed. Also, to reset the ATN signal in manual transfer mode, execute the Reset ATN command before the ACK signal is sent to SCSI. In the following cases, SPC automatically resets the ATN signal without the Reset ATN command:

a. On occurrence of a disconnected interrupt.
b. On sending the last byte during execution of the MESSAGE OUT phase in hardware transfer mode. (See Figure 4.3.3.)

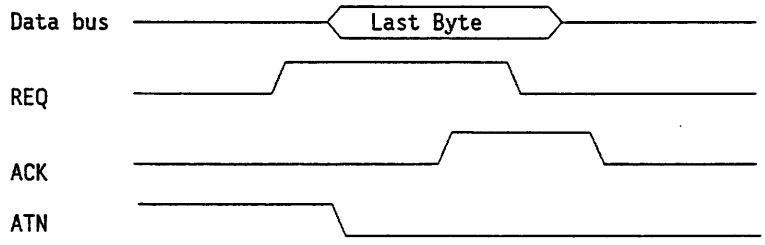


Fig. 4.3.3 ATN signal resetting in MESSAGE OUT phase

(5) Transfer command

The transfer command executes the following information transfer phases in SCSI:

- DATA IN/OUT phase
- STATUS phase
- COMMAND phase
- MESSAGE IN/OUT phase

The transfer operation initiated by this command is referred to as a hardware transfer operation, the sequence of which is controlled by SPC. Before issuing the Transfer command, be sure to set up the following:

a. Transfer byte counters (TCH, TCM, TCL)
   Set the byte count of the data to be transferred. (MSB: TCH, LSB: TCL)

b. Bits 2 to 0 of the PCTL register
   Set a pattern indicating the phase to be executed.

c. TMOD register
   Set detailed transfer mode.

When SPC serves as a TARGET, it executes the information transfer phase specified in the PCTL register and terminates the Transfer command when any of the following conditions is encountered:

a. End of transferring data of the byte count specified in the transfer byte counter.

b. Receipt of the Transfer Pause command.

c. Detection of a parity error in the received data during an input operation with bit 0 (Termination Mode) of the SCMD register set to 1.
   (When the parity checking is enabled)

When SPC serves as an INITIATOR, it starts the transfer operation as follows:

a. If the REQ signal is received before the Transfer command is issued, SPC compares the phase requested by the SCSI with that specified in the PCTL register at receipt of this command. Then, if they match, SPC starts the transfer operation.

b. If the REQ signal has not been received when the Transfer command is issued, SPC makes this command wait for execution. Then, if the phase specified in the PCTL register matches that requested by SCSI on receipt of the REQ signal, SPC starts the transfer operation. In the above phase comparison, if a phase mismatch occurs, the Transfer command is nullified, then SPC generates a service required interrupt. On occurrence of this interrupt, check the PSNS register for the phase requested by SCSI, and issue the Transfer command again or carry out manual transfer.

When SPC serves as an INITIATOR, Transfer command execution terminates when any of the following conditions is encountered:

a. In other than the padding transfer mode, Transfer command execution terminates when the transfer of data of the byte count specified in the transfer byte counter is completed, or when another information transfer phase is requested by the TARGET.

b. In the padding transfer mode, Transfer command execution terminates when another information transfer phase is requested by the TARGET.

c. Transfer command execution terminates when disconnected interrupt occurs.

(6) Transfer Pause command

The Transfer Pause command prematurely halts a hardware transfer operation initiated by the Transfer command when SPC serves as a TARGET. Note that the Transfer Pause command cannot be used when SPC serves as an INITIATOR. On receipt of this command, SPC performs the following:

a. Stops sending a new REQ signal to SCSI, in an input operation.

b. Stops sending a transfer request (DREQ) signal to the external buffer memory, in a DMA mode output operation.

Note: For an output operation in program transfer mode, a write to the data buffer register is not allowed after this command has been issued.

Then, the hardware transfer operation terminates when the internal data buffer register in SPC becomes empty.

(7) Set ACK/REQ command

The Set ACK/REQ command is used to set ACK or REQ signals for SCSI during execution of manual transfer. When SPC acts as an INITIATOR, this command causes the ACK signal to be sent. When SPC acts as a TARGET, it causes the REQ signal to be sent. In manual transfer mode, data is transferred via the TEMP register. In this case, the pattern (kind) of the information transfer phase to be executed must be preset at bits 2 to 0 of the PCTL register. During execution of manual transfer, the transfer byte counter remains unchanged. Figures 4.3.4 and 4.3.5 show the manual transfer procedures.

(8) Reset ACK/REQ command

The Reset ACK/REQ command is used to reset the ACK or REQ signals for SCSI. When SPC acts as an INITIATOR, this command resets the ACK signal. When SPC acts as a TARGET, it resets the REQ signal. Use this command in execution of manual transfer. See Figure 4.3.4 and 4.3.5 for the manual transfer procedures. Also, when SPC serves as an INITIATOR, the Reset ACK/REQ command must be issued to reset the ACK signal for the last byte in the MESSAGE IN phase of the hardware transfer mode. In the MESSAGE IN phase, the end of the Transfer command is reported with the ACK signal for the last byte being asserted. The MPU program checks the validity of the received message first, then issues this command. In this case, the ATN signal, if necessary, may be sent out using the Set ATN command prior to this command.

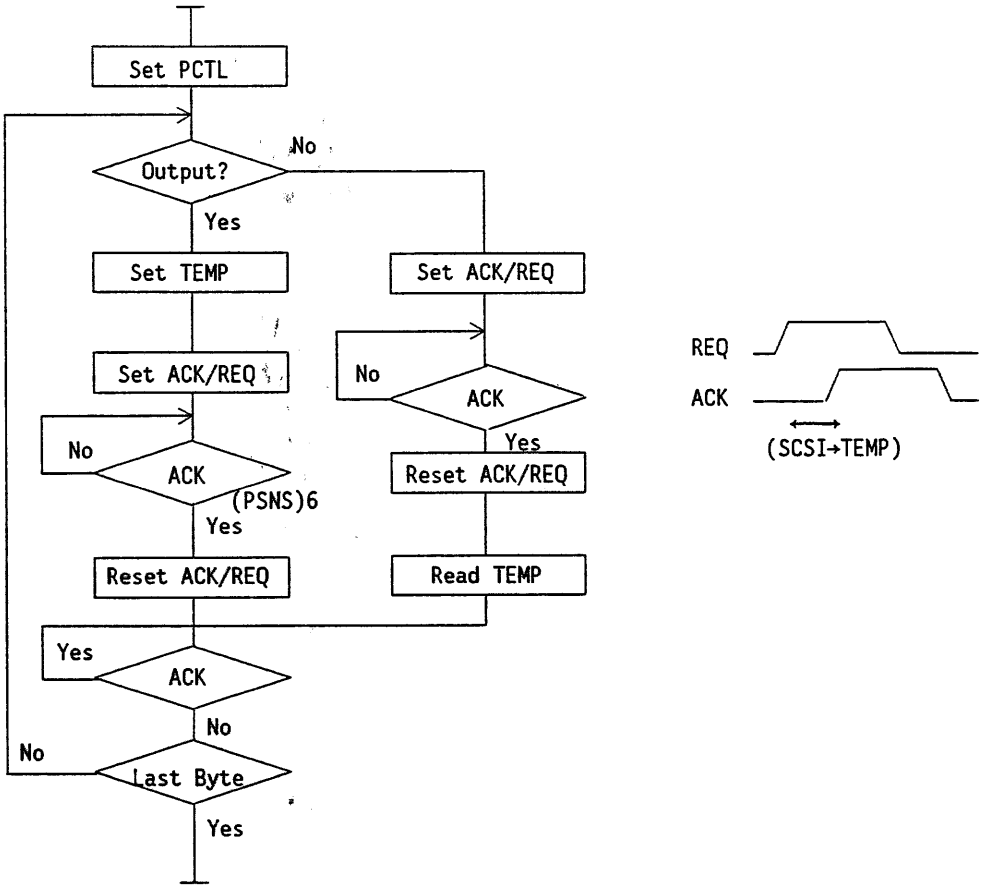


Fig. 4.3.4 Manual transfer procedure (SPC serving as a TARGET)

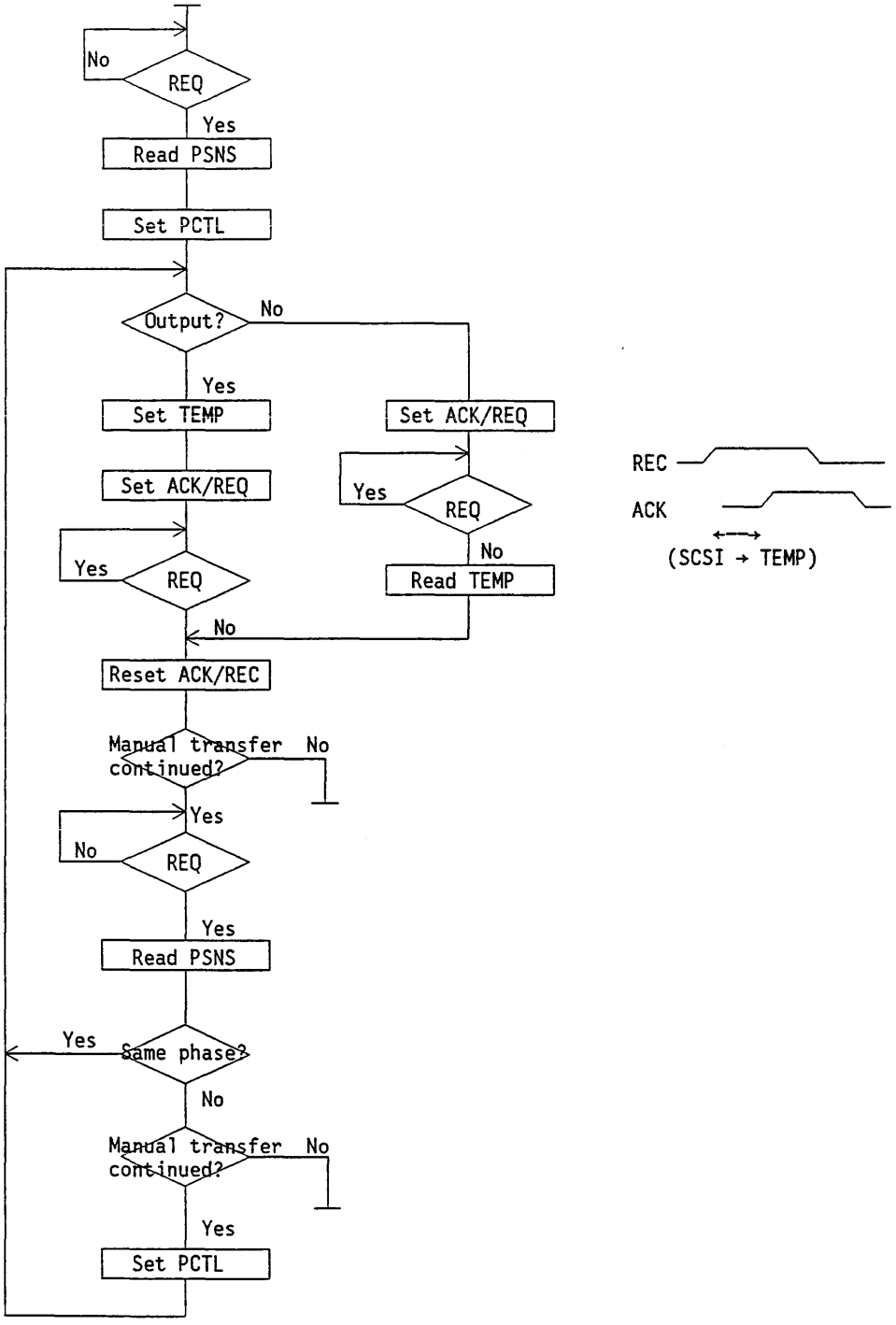


Fig. 4.3.5 Manual transfer procedure (SPC serving as an INITIATOR)

4.3.3 Command Termination Report

(1) Immediate commands

The followings are immediate type commands which terminate operations immediately after being issued. For these commands, SPC does not report termination.

- Set ATN
- Reset ATN
- Set ACK/REQ
- Reset ACK/REQ

(2) Interrupt commands

For the following commands, an interrupt occurs at the end of execution. The interrupt cause is indicated in the INTS register.

- Select
- Transfer

(3) Non-interrupt commands

The following commands terminate with different timings depending on the SPC operation being executed. Check the termination status according to the status information in the SSTS register.

	Termination status (SSTS register)			
	Bit 7 INIT	6 TARG	5 SPC Busy	4 Xfer in Prg.
Transfer Pause	0	1	0	0
Bus Release *1	0	0	0	0

*1: If a selected/reselected interrupt condition is detected immediately after termination of the Bus Release command, an interrupt occurs and either the INIT or TARG bit is set.

4.3.4 Command Issuance Timing

Issuance of a command requires a write to the SCMD register. SPC synchronizes a write to the SCMD register with a clock supplied from the $\overline{CLK}$ pin, and then starts executing the command specified at bits 7 to 5. Figure 4.3.6 shows the command execution timing. When issuing commands successively, leave an interval between them for more than the sync-loss period (four clock cycles) in SPC.

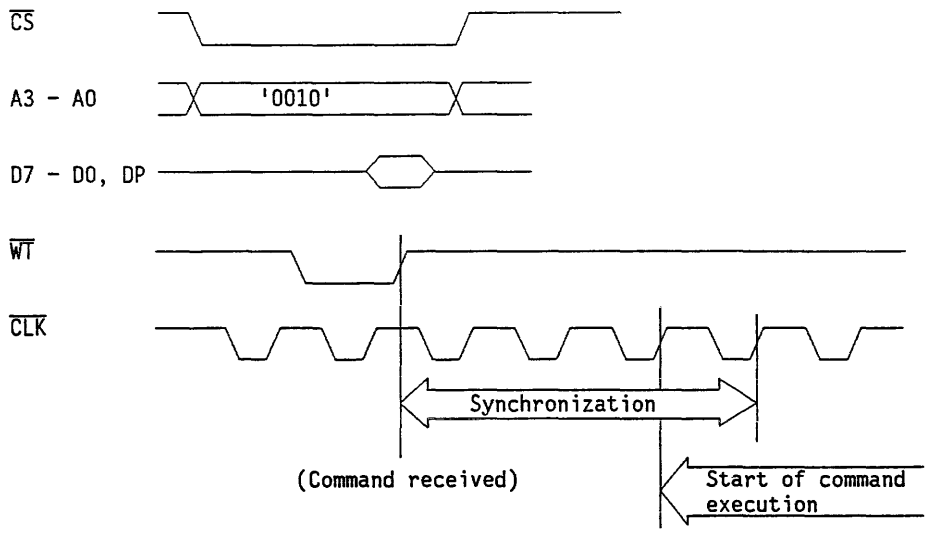


Fig. 4.3.6 Command execution timing

4.4 TMOD REGISTER

OP	7	6	5	4	3	2	1	0	P
R/W	Sync. Xfer	MAX. Transfer Offset			MIN. Transfer Period		'0'	'0'	P
		4	2	1	2	1			

4.4.1 Register Functions

Bit 7: Synchronous Transfer

1 .. Indicates that the DATA IN/OUT phase is executed in synchronous transfer mode. The COMMAND, STATUS, and MESSAGE IN/OUT phases are executed in asynchronous transfer mode disregarding the setting at this bit.

0 .. Indicates that the DATA IN/OUT phase is executed in asynchronous transfer mode.

Bits 6 to 4: Maximum Transfer Offset

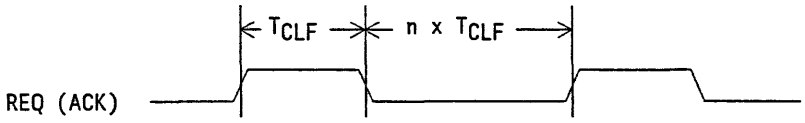
Bits 6 to 4 indicate a maximum value of the REQ/ACK offset to be used in synchronous transfer mode.

Bit 6	Bit 5	Bit 4	Maximum offset value
0	0	0	8
0 - 1	0 - 1	1 - 1	1 - 7

When SPC serves as a TARGET, it sends the REQ signal in advance within the specified maximum offset value. When SPC serves as an INITIATOR, it can receive the REQ signal and input data within the specified maximum offset value. If the maximum offset value is exceeded in reception of the REQ signal, an error condition is detected at bit 0 (Transfer Offset Error) of the SERR register.

Bits 3 and 2: Transfer Period

Bits 3 and 2 indicate a parameter for determining the minimum repeat cycle of the REQ and ACK signals in synchronous transfer mode. Specify a period between the trailing edge of the REQ (ACK) signal and the leading edge of the next REQ (ACK) signal in multiples of a clock signal cycle (T_{CLF}) supplying at the $\overline{CLK}$ pin of SPC.
Figure 4.4.1 shows an example of transfer period setting.
In synchronous transfer mode, the REQ (ACK) signal pulse width (Typical) equals a cycle of the clock signal (T_{CLF}) supplied to the $\overline{CLK}$ pin.



			Setting examples; Maximum transfer speeds		
Bit 3	Bit 2	n	T_{CLF} = 125 ns	T_{CLF} = 136 ns	T_{CLF} = 166 ns
0	0	1	4.00 MBPS	3.68 MBPS	3.01 MBPS
0	1	2	2.67	2.45	2.01
1	0	3	2.00	1.84	1.51
1	1	4	1.60	1.47	1.21

Fig. 4.4.1 Transfer period setting

4.4.2 Transfer Mode Setting Timing

The TMOD register value determines the way the DATA IN/OUT phase is executed. When SPC serves as a TARGET, specify the DATA IN/OUT phase (C/D, MSG = 00) in the PCTL register. And, before issuing the Transfer command, be sure to complete TMOD register setting. When SPC acts as an INITIATOR, be sure to specify a correct value before the target initiates the DATA IN/OUT phase. A TARGET's phase changing time and the period from it until transmission of the first REQ signal are unpredictable; therefore, set the transfer mode with the following timing:

(1) After completion of SELECTION phase

a. Before issuing the Transfer command for execution of the COMMAND phase, or

b. Before resetting the ACK signal for the last byte in the MESSAGE IN phase (before issuing the Reset ACK command) if a SYNCHRONOUS DATA TRANSFER REQUEST message is transmitted at the end of the command phase.

(2) After reselected interrupt

a. Before issuing the Reset ACK command in the MESSAGE IN phase (IDENTIFY).

4.5 PCTL REGISTER

OP	7	6	5	4	3	2	1	0	P
R/W	Bus Free Interrupt Enable	'0'				MSG Out	C/D Out	I/O Out	P

Bit 7: Bus Free Interrupt Enable

With bit 7 set to 1, detection of the BUS FREE phase on the SCSI causes a disconnected interrupt to occur. To prevent an undesired interrupt occurring, be sure to set bit 7 to 0 when:

- Issuing the Select command, or
- Resetting a 'disconnected' interrupt.

Bit 2: MSG Out

Bit 1: C/D Out

Bit 0: I/O Out

When SPC serves as a TARGET, specify the information transfer phase to be executed in SCSI. These bit values are sent to SCSI as MSG, C/D and I/O signals.

When SPC acts as an INITIATOR, specify the pattern indicating the transfer phase to be executed. Before executing the transfer operation, the specified transfer phase pattern is compared with a bus phase actually requested by the TARGET. Then, if they match, the transfer operation is initiated. Table 4.5.1 shows how to set a transfer phase. Use bit 0 (I/O Out) to specify the phase to be executed with the Select command. See 4.3.2 (2) - Select command for details.

Table 4.5.1 Transfer phase setting

Bit 2 MSG Out	Bit 1 C/D Out	Bit 0 I/O Out	SCSI transfer phase
0	0	0	Data Out
0	0	1	Data In
0	1	0	Command
0	1	1	Status
1	0	0	Unused
1	0	1	Unused
1	1	0	Message Out
1	1	1	Message IN

4.6 DATA BUFFER REGISTER (DREG)

OP	7	6	5	4	3	2	1	0	P
R/W	Internal Data Register (8 Bytes FIFO)								
	Bit 7	6	5	4	3	2	1	0	P

SPC's internal data buffer register consists of eight bytes and operates on the FIFO principle. When executing the Transfer command in program transfer mode, MPU transfers data using this register. Figure 4.6.1 shows the DREG access procedure to be taken in program transfer mode. A write to/read from this register is performed on the FIFO principle. Therefore, never repeat accessing more than the number of times required.

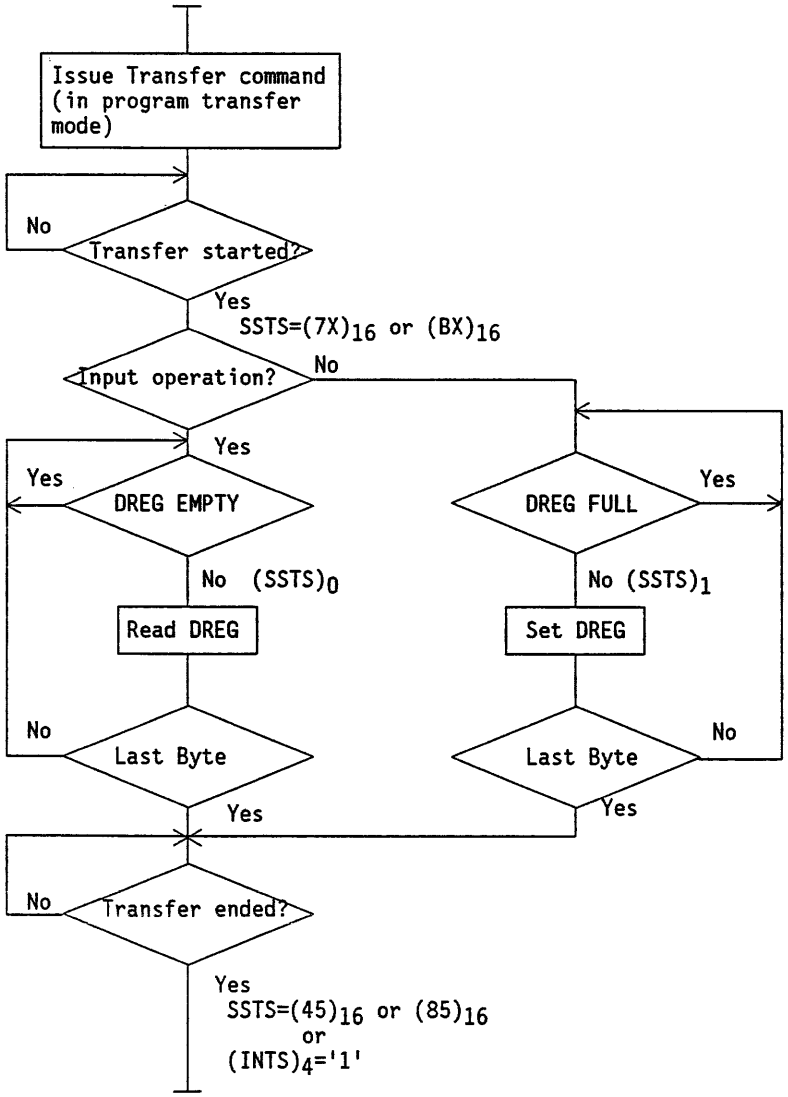


Fig. 4.6.1 DREG access procedure in program transfer mode

4.7 TEMP REGISTER

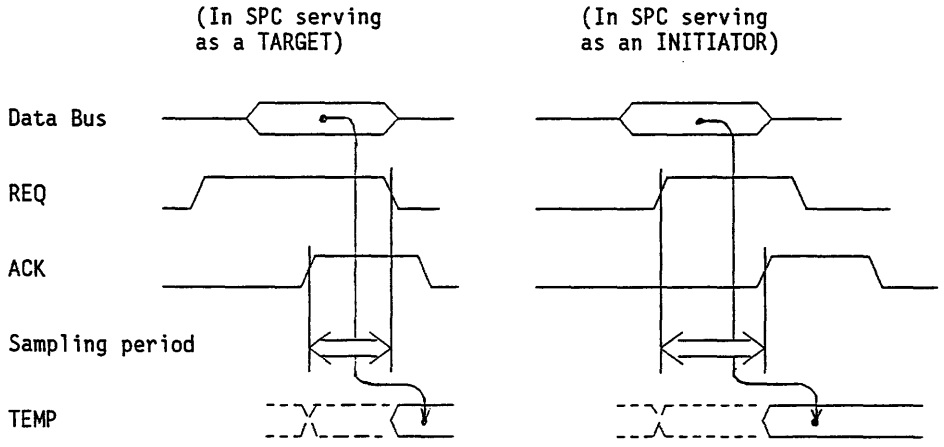
OP	7	6	5	4	3	2	1	0	P
R	Temporary Data (Input: From SCSI)								
	Bit 7	6	5	4	3	2	1	0	P
W	Temporary Data (Output: To SCSI)								
	Bit 7	6	5	4	3	2	1	0	P

The TEMP register is used for controlling the SCSI data bus except when hardware transfer is executed. It consists of two bytes, each of which is dedicated exclusively to receiving/sending data.

(1) Data receiving element (read only)

a. When a SELECTION/RESELECTION phase is detected in SCSI, the contents on the SCSI data bus are saved in the TEMP register. If a selected/reselected interrupt occurs, a bus device can be identified by the TEMP register contents.

b. For a manual transfer input operation, the contents on the SCSI data bus are saved in the timing sequence shown in Figure 4.7.1



Fir. 4.7.1 Data bus save in manual transfer input operation

(2) Data sending element (write only)

1) Before issuing the Select command, set the contents to be sent to the SCSI data bus in the SELECTION/RESELECTION phase.

2) For a manual transfer output operation, set the data to be sent out.

4.8 TRANSFER BYTE COUNTER (TCH, TCM, TCL)

OP	7	6	5	4	3	2	1	0	P
R/W	TCH: Transfer Counter (MSB)								
	Bit 23	22	21	20	19	18	17	16	P
R/W	TCM: Transfer Counter (2nd Byte)								
	Bit 15	14	13	12	11	10	9	8	P
R/W	TCL: Transfer Counter (LSB)								
	Bit 7	6	5	4	3	2	1	0	P

The transfer byte counter consists of three bytes and functions as a down counter. In execution of a hardware transfer operation, it is decreased by one each time one byte of data is transferred over SCSI. It indicates the remaining byte count of data to be transferred. In the Select command execution, this counter operates as a response waiting time supervisory timer and sequence control counter. See 4.3.2 (2) - Select command and (5) - Transfer command for transfer byte counter initialization. While the transfer byte counter is operating, do not carry out a read/write.

4.9 PSNS REGISTER

OP	7	6	5	4	3	2	1	0	P
R	REQ	ACK	ATN	SEL	BSY	MSG	C/D	I/O	P

When bit 5 (Diagnostic Mode) of the SCTL register is set to 0, the PSNS register indicates the control signal status on SCSI (input signals to SPC).

		- SPC input pins -
Bit 7	REQ	REQI
6	ACK	ACKI
5	ATN	ATNI
4	SEL	SELI
3	BSY	BSYI
2	MSG	MSGI
1	C/D	C/DI
0	I/O	I/OI

When bit 5 (diagnostic Mode) of the SCTL register is set to 1, the PSNS register indicates the status of control signals sent from SPC to SCSI. In the SCSI pseudo operation using the SDGC register, the PSNS register can be used to check the SCSI control signal status. A read from this register is allowed at any time regardless of the SPC condition. Bit 5 (ATN) of this register indicates the ATN signal status on SCSI:
When SPC serves as a TARGET, receipt of the ATN signal is indicated in this register but does not have any effect on other operations. The MPU program examines the ATN signal status at the following times in sequence and responds to the ATTENTION condition from SCSI:

(1) When a selected interrupt occurs
(2) When the RESELECTION phase has completed
(3) When the Transfer command has been completed
(4) During execution of the Transfer command

When the ATN signal is detected, the Transfer Pause command can halt the transfer operation for transition to the MESSAGE OUT phase.

(5) During execution of manual transfer

4.10 SSTS REGISTER

OP	7	6	5	4	3	2	1	0	P
R	Connected INIT	TARG	SPC Busy	Xfer in Progress	SCSI Reset In	TC=0	DREG FULL	Status EMPTY	P

4.10.1 Register Functions

The SSTS register indicates the SPC internal status, which can be read out at any time.

Bit 7 and 6: Connected (INIT, TARG)

These bits indicate the Connecting status between the SPC and SCSI.

Bit 7: INIT	Bit 6: TARG	State
0	0	Not connected with SCSI.
1	0	SPC serves as an INITIATOR: • During execution of the SELECTION phase and after its completion. • After a reselected interrupt
0	1	SPC serves as a TARGET: • During execution of the RESELECTION phase and at its completion. • After a selected interrupt
1	1	Undefined

Bit 5: SPC Busy

Bit 5 indicates that a command is being executed or is waiting to be executed.

Bit 4: Transfer in Progress

Bit 4 indicates that a hardware transfer operation is being executed or the SCSI is requesting information transfer phase.

Bit 3: SCSI Reset In

Bit 3 indicates the RST signal status on SCSI (input signal to the RSTI pin of SPC).

Bit 2: TC = 0 (Transfer Counter Zero)

Bit 2 indicates that the transfer byte counter (TCH, TCM, TCL) has reached 0.

Bits 1 and 0: DREG Status (Full, Empty)

These bits indicate the status of the internal data buffer register. When executing a hardware transfer operation in program transfer mode, determine the data buffer register access timing by using these bit values.

Bit 1: FULL	Bit 0: EMPTY	Data buffer register status
0	0	Holds 1 to 7 bytes of data.
0	1	Empty.
1	0	Holds 8 bytes of data, leaving no free space.
1	1	Undefined

4.10.2 SPC Status

SPC status is represented by combinations of status bits 7 to 4 of this register. Table 4.10.1 lists the combinations of these bits and SPC status.

Table 4.10.1 SPC operating status indications

SSTS register				SPC operating status
Bit 7: INIT	Bit 6: TARG	Bit 5: SPC Busy	Bit 4: Xfer in Progress	
0	0	0	0	SPC is not connected with SCSI. SPC does not hold a command waiting to be execution.
0	0	1	0	SPC is not connected with SCSI. But SPC holds the Select command, which is waiting for BUS FREE phase. Or it is executing ARBITRATION phase.
0	1	0	0	SPC serves as a TARGET. No operation is being executed in SCSI, or manual transfer is being executed.
0	1	1	0	SPC is executing RESELECTION phase on SCSI.
0	1	1	1	SPC serves as a TARGET. Hardware transfer operation (Transfer command) is being executed.
1	0	0	0	SPC serves as an INITIATOR. No operation is being executed in SCSI, or manual transfer is being executed.
1	0	0	1	SPC serves as an INITIATOR. Although SPC has received a REQ signal from SCSI, it is not ready to start transfer operation because no Transfer command has been issued or transfer phase does not match.
1	0	1	0	SPC is executing the SELECTION phase on SCSI.
1	0	1	1	SPC serves as an INITIATOR. Hardware transfer operation (Transfer command) is being executed.

4.11 INTS REGISTER

OP	7	6	5	4	3	2	1	0	P
R	Sele-cted	Resele-cted	Dis-Connected	Command Complete	Service Required	Time Out	SPC Hardware Error	Reset Condi-tion	P
W	Reset Interrupt								-

4.11.1 Register Functions

The INTS register is used to indicate the cause of an interrupt and reset it. An interrupt issued by SPC (INTR pin) can be masked by bit 0 (INT Enable) of the SCTL register (except an interrupt whose cause is indicated at bit 0 [RESET condition]). To clear an interrupt, set 1 at the corresponding bit position in this register. Note that only the interrupt condition specified by 1 is reset. The bit positions having 0s remain unchanged (corresponding interrupt conditions are maintained). In this register, two or more interrupts may be reset at the same time.

4.11.2 Interrupt Processing

(1) Selected interrupt (Bit 7)

Bit 7 indicates that SELECTION phase in SCSI has resulted in SPC being selected from another bus device (INITIATOR). When the SELECTION phase is detected, SPC checks the contents of the SCSI data bus. If the following conditions are satisfied, SPC executes a response sequence on SCSI, then generate a selected interrupt.

a. The ID specified in the BDID register is selected.
b. There or more bits not including the parity bit are not set to 1.
c. When the parity checking is enabled, a parity bit value is correct.

In the SELECTION phase, the TEMP register holds the value of SCSI data bus. SPC serves as a TARGET from when this interrupt occurs until when the Bus Release command is issued or the RESET condition is detected in SCSI. During this period, SPC asserts BSY signal to SCSI. Before issuing the Bus Release command, be sure to reset the cause of this interrupt.

(2) Reselected interrupt (Bit 6)

Bit 6 indicates that RESELECTION phase in SCSI has resulted in SPC being reselected from another bus device (TARGET). When the RESELECTION phase is detected, SPC checks the contents of the SCSI data bus. If the following conditions are satisfied, SPC executes a response sequence on SCSI, then generate a reselected interrupt.

a. The ID specified in the BDID register is selected.
b. Only two bits not including the parity bit are set to 1.
c. When the parity checking is enabled, a parity bit value is correct.

In the RESELECTION phase, the TEMP register holds the value of the SCSI data bus. SPC serves as an INITIATOR from when this interrupt occurs until when the disconnected interrupt occurs or the RESET condition is detected in SCSI. Before starting the transfer operation in SCSI, be sure to reset the cause of this interrupt. If the disconnected interrupt is indicated together with the reselected interrupt, reset both of these interrupts simultaneously.

(3) Disconnected interrupt (Bit 5)

Bit 5 indicates that the BUS FREE phase has been detected in SCSI when bit 7 (Bus Free Interrupt Enable) the PCTL register is set to 1. Also, when SPC serves as on INITIATOR, bit 5 indicates transition to the BUS FREE phase in SCSI. After this interrupt condition has occurred, the next SELECTION/RESELECTION phase may be executed in SCSI. But, SPC does not respond to SCSI until this interrupt condition is reset. If the disconnected interrupt condition is detected during hardware transfer (Transfer command) execution with SPC serving as an INITIATOR, the SCSI operation stops but the SPC internal transfer sequence continues until one of the following events is encountered:

a. The internal data buffer register becomes empty in an input operation.

b. The data prefetch sequence to the internal data buffer register is completed in an output operation.

When a disconnected interrupt occurs, check the SSTS register to confirm if the transfer operation has been completed.

(4) Command complete interrupt (Bit 4)

Bit 4 indicates that the Select command/Transfer command operation has been completed.

a. Completion of Select command
This interrupt indicates that SPC has acknowledged a response (BSY signal) from the selected bus device in SELECTION/RESELECTION phase execution. It indicates that the SELECTION/RESELECTION phase has completed in SCSI. SPC serves as an INITIATOR after the SELECTION phase has been executed, and it serves as a TARGET after the RESELECTION phase has been executed.

b. Completion of Transfer command (when SPC serves as a TARGET)
This interrupt indicates that the transferring data of the byte count specified in the transfer byte counter has been completed. Or, in an input operation with bit 0 (Termination Mode) of the SCMD register set to 1, this interrupt indicates the stop of transfer due to parity error is detected in the data received from SCSI. In either case, this interrupt occurs after checking that the ACK signal for the REQ signal of the last byte is inactive on SCSI at asynchronous mode transfer. Or, this interrupt occurs after checking that the number of ACK signals received matches the number of REQ signals transmitted at synchronous mode transfer.

c. Completion of Transfer command (when SPC serves as an INITIATOR)
When padding mode transfer is not specified, this interrupt indicates that the transferring data of the byte count specified in the transfer byte counter has been completed. When padding mode transfer is performed, this interrupt indicates that the current transfer operation has been terminated due to another transfer phase is requested in SCSI. In this case, the service required interrupt occurs at the same time. In the MESSAGE IN phase, this interrupt occurs while the ACK signal to the last byte is held active. Before resetting this interrupt, be sure to issue the Reset ACK/REQ command.

(5) Service required interrupt (Bit 3)

This interrupt occurs if the SPC serving as an INITIATOR is put in either of the following conditions. It indicates a request for MPU program intervention.

a. SPC has received the Transfer command, but cannot start the transfer operation because the transfer phase specified by bits 2 to 0 of the PCTL register does not match that requested in SCSI.

b. SPC has stopped the current hardware transfer operation (Transfer command) because of a request for another transfer phase in SCSI. In this case, the transfer operation in SCSI stops immediately, but the SPC internal transfer sequence continues until one of the following events is encountered:

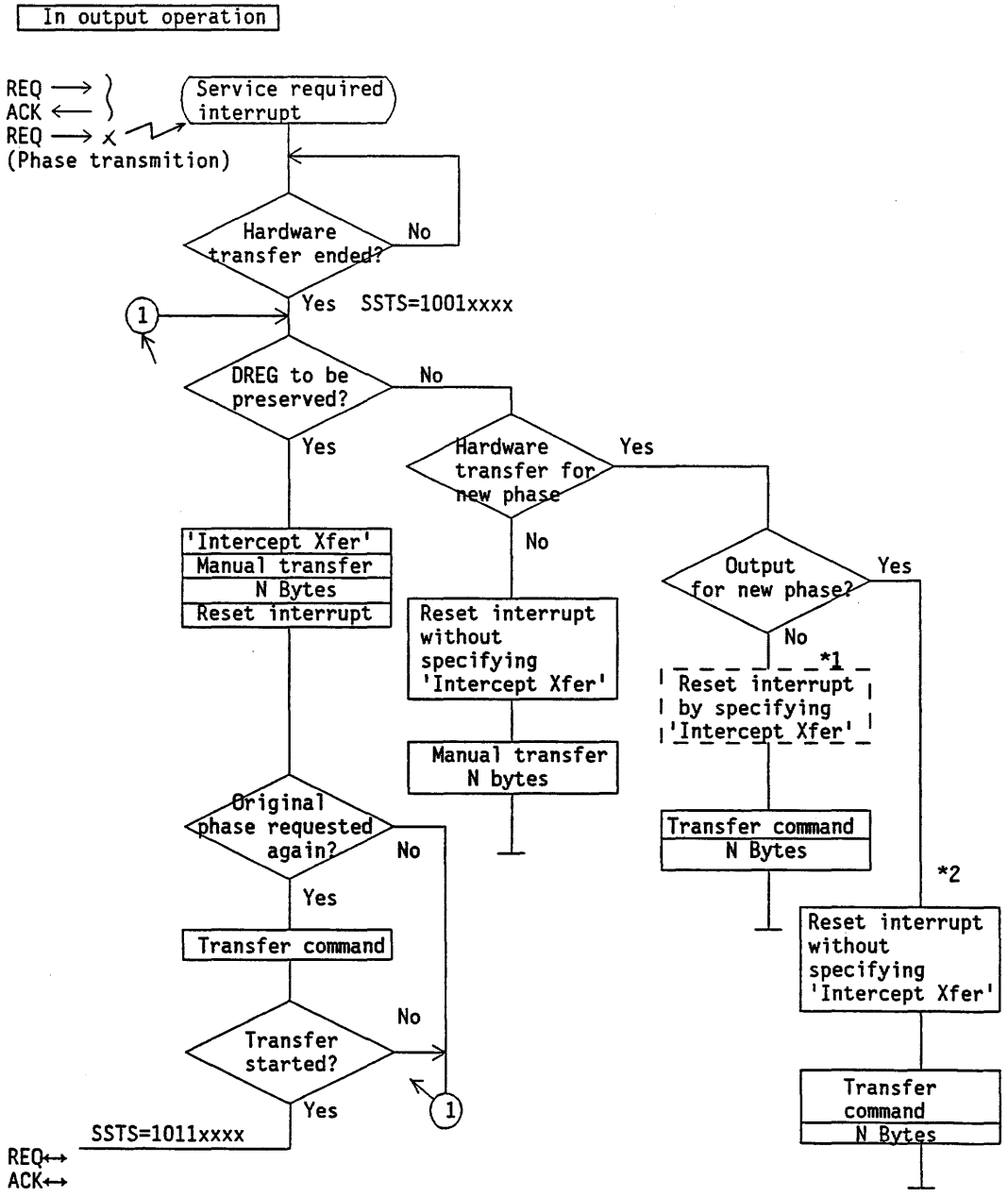
- Input operation
  The internal data buffer register becomes empty.

- Output operation
  The data prefetch sequence to the internal data buffer register is completed.

Therefore, when this interrupt occurs, read out the SSTS register and check if the SPC internal transfer operation is completed. If the service required interrupt occurs during an output operation, the data prefetched in the SPC internal data buffer register may remain (not be sent to SCSI). For how to handle the remaining data (up to eight bytes), see the interrupt processing procedure described below. When the service required interrupt occurs, the MPU program examines a transfer phase request from SCSI and proceeds to execute the transfer operation using one of the following procedures. Figures 4.11.1 and 4.11.2 show examples of interrupt processing procedure.

a. Hardware transfer
   The MPU program specifies the transfer phase pattern requested by SCSI as bit 2 to 0 of the PCTL register, and reissues the Transfer command.

b. Manual transfer
   If this interrupt occurs during an output operation, the remaining data in the SPC internal data buffer register may have to be preserved. In this case, with bit 3 (Intercept Transfer) of the SCMD register set to 1, perform manual transfer and interrupt resetting. When the interrupted original transfer phase (output) is requested again after manual transfer by the above processing procedure, the suspended transfer operation can be restarted using the remaining data held in the data buffer register.

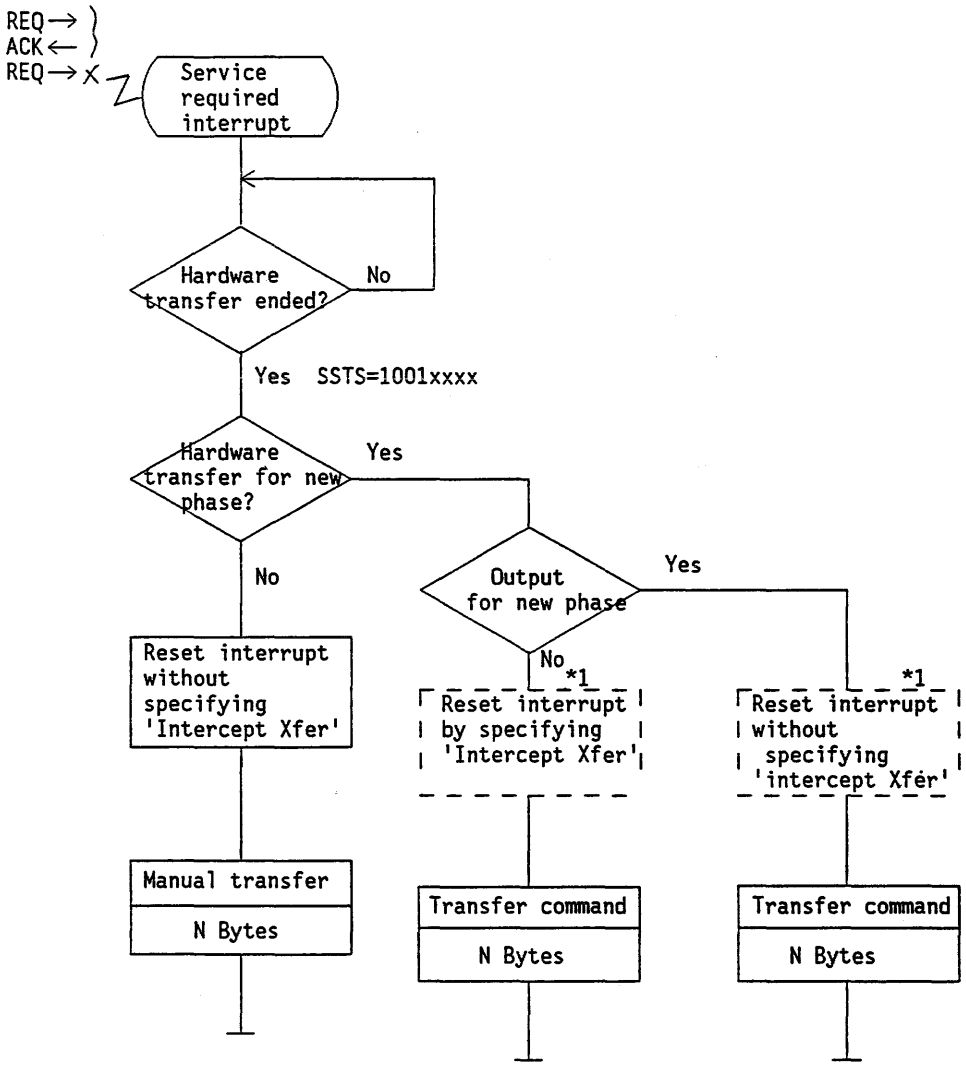


*1. An interrupt needs not always be reset. The interrupt is reset automatically when the Transfer command starts hardware transfer.

*2. If the interrupt is reset, the data prefetched in the internal data buffer register before a change of phase is detected is lost.

Fig. 4.11.1 Service required interrupt processing procedure (1)

In input operation



*1: An interrupt need not always be reset. The interrupt (service required) is reset automatically when the Transfer command starts hardware transfer.

Fig. 4.11.2 Service required interrupt processing procedure (2)

(6) Time-out interrupt (Bit 2)

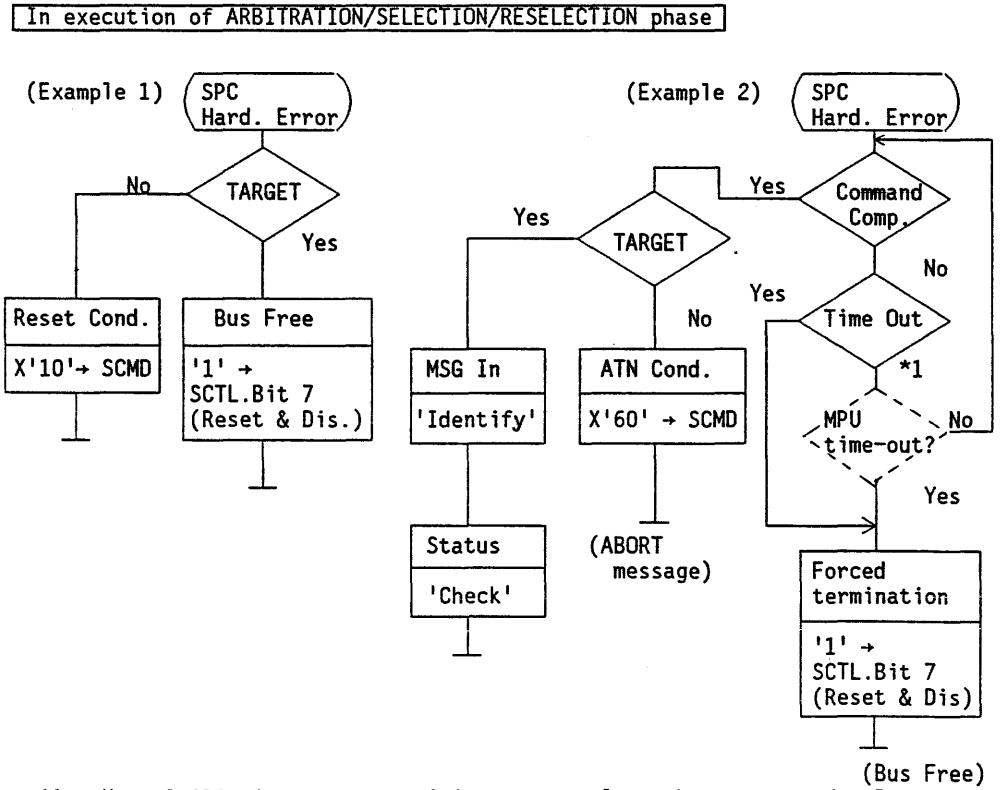
This interrupt indicates that the selected bus device has not responded within the predetermined supervisory time after SPC initiates the SELECTION/RESELECTION phase. See 4.3.2 (2) - Select command for details of the supervisory time setting procedure and the interrupt processing procedure.

(7) SPC hardware error interrupt (Bit 1)

This interrupt indicates that SPC has detected one of the following error indications in the SERR register:

- TC parity error
- Phase error
- Short transfer period
- Transfer offset error

See 4.12 - SERR register for details of these errors. When this interrupt occurs, SPC does not stop the operation being executed (for any error cause). Since the normal operational sequence and end report cannot always be guaranteed in this case, the MPU program must be used for SPC control and bus phase control of SSCI.
Figures 4.11.3 to 4.11.5 show examples of error control processing.



*1: Normal SPC time-out supervision cannot always be guaranteed. Be sure to perform time supervision using the MPU program.

Fig. 4.11.3 Example of control processing for SPC-detected error (1)

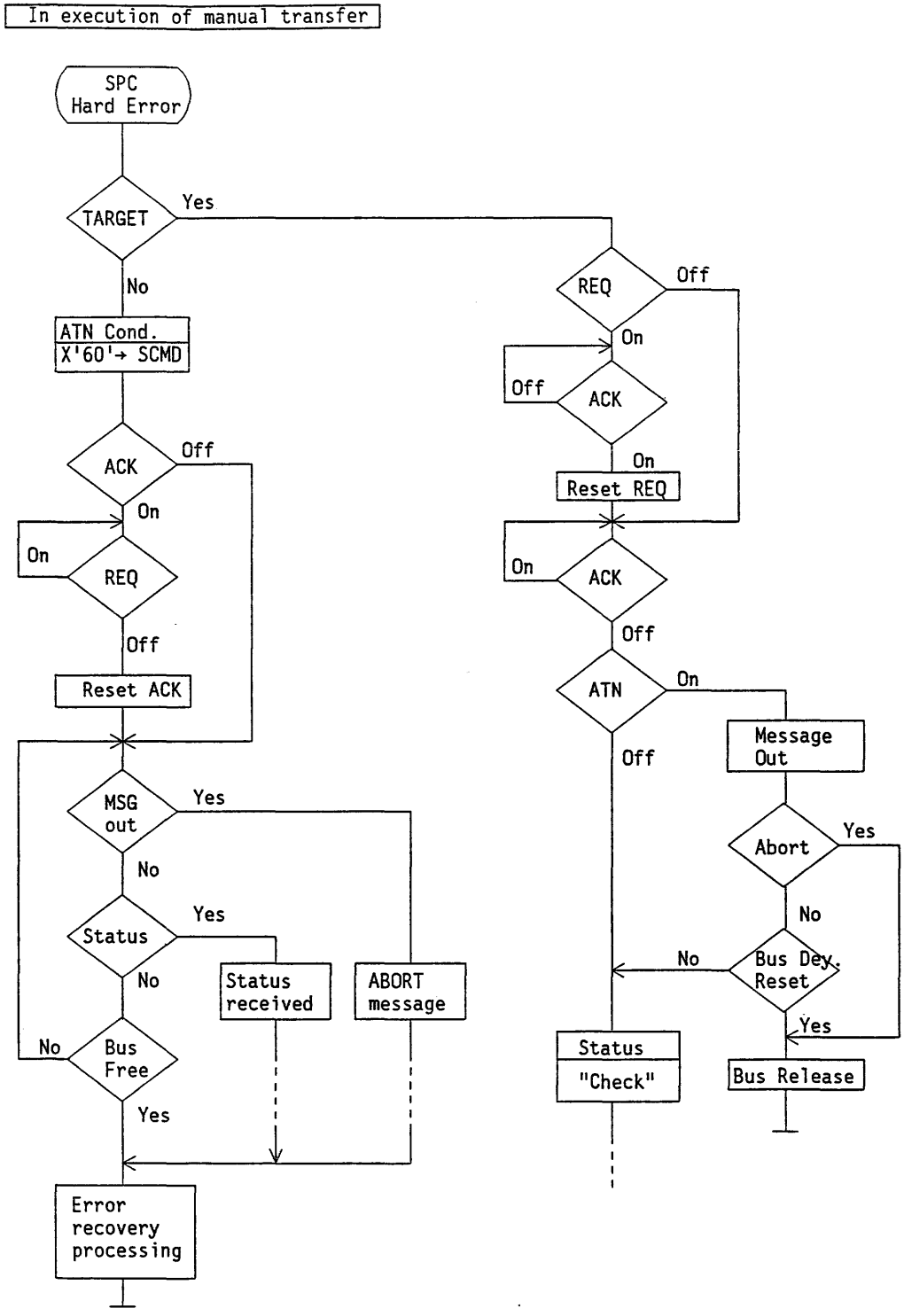
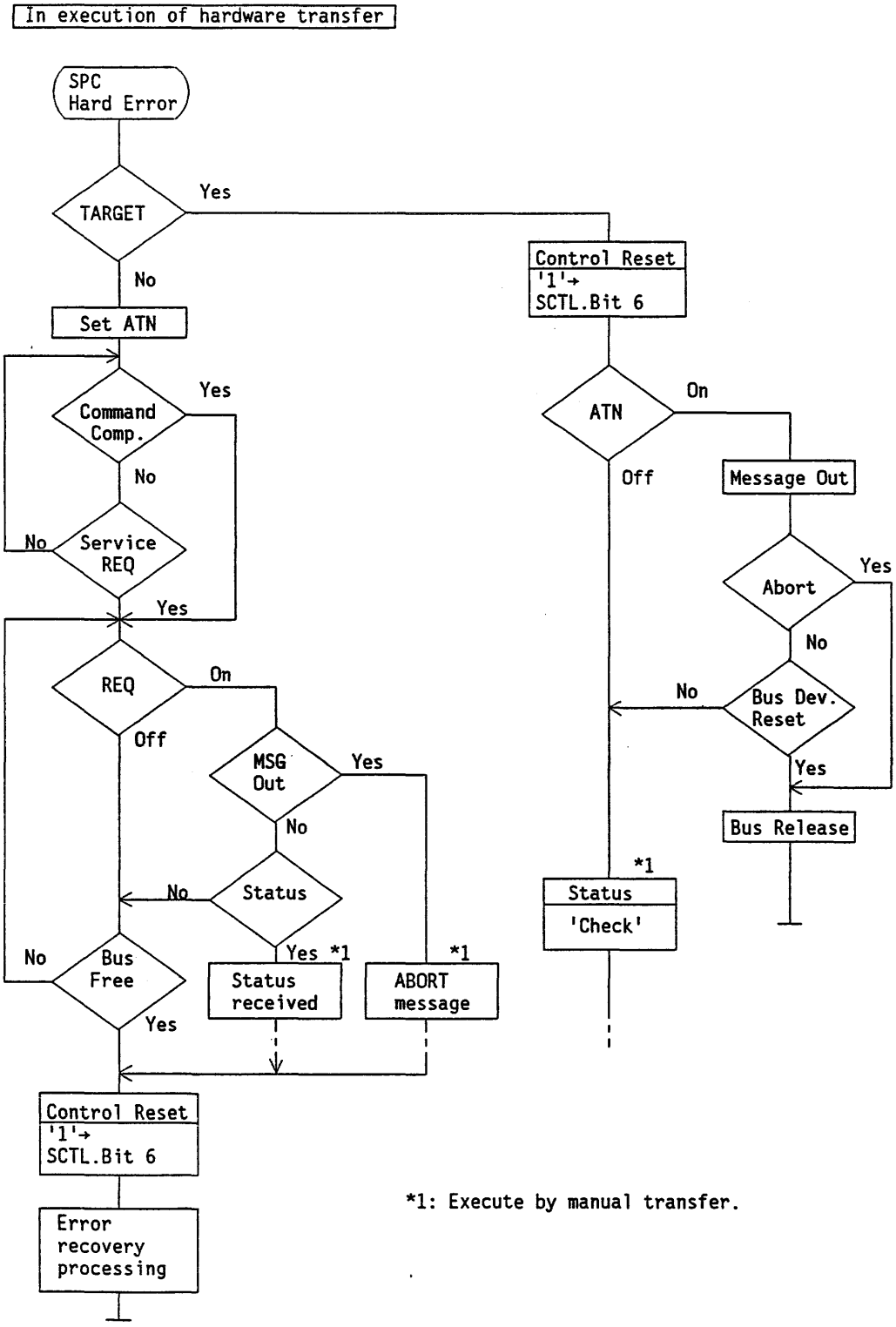


Fig. 4.11.4 Example of control processing for SPC-detected error (2)



*1: Execute by manual transfer.

Fig. 4.11.5 Example of control processing for SPC-detected error (3)

(8) Reset condition interrupt (Bit 0)

This interrupt indicates that the RESET condition has been detected in SCSI. Note that this interrupt cannot be masked. The reset condition persists for an unpredictable period of time. After making sure that bit 3 (Reset In) of the SSTS register becomes to 0, MPU must reset this interrupt condition. The reset condition interrupt may occur regardless of whether SPC is connected with SCSI or not. When SPC is connected with SCSI, occurrence of this interrupt causes SPC to immediately deactivate a signal being sent to SCSI. Then SPC proceeds to the BUS FREE phase. When SPC is executing a command, occurrence of this interrupt causes SPC to terminate its operation and reset its internal state. However, the following internal registers hold the control information unchanged:

- BDID register
- SCMD register
- PCTL register
- SCTL register
- TMOD register
- Transfer byte counter

Until this interrupt is reset, the SPC internal reset state is maintained even if the RESET condition is released in SCSI. Therefore, SPC does not respond even when a new bus phase (e.g. SELECTION) is executed in SCSI.

4.12 SERR REGISTER

OP	7	6	5	4	3	2	1	0	P
R	Data Error SCSI	Data Error SPC	'0'	'0'	TC Parity Error	Phase Error	Short Xfer Period	Xfer Offset Error	P

4.12.1 Register Functions

The SERR register provides details of an error detected in SPC. An SPC hardware error interrupt occurs if an error is indicated at any of bits 3 to 0.

Bits 7 and 6: Data Error

These bits indicate that a parity error has been detected in the transferred data during transfer phase execution in SCSI. Table 4.12.1 lists the data error indication bit patterns and the relevant SPC operations. When changing the transfer phase in SCSI, these error indication bits must be reset.

Table 4.12.1 Data error indication bit patterns in transfer phase

Bit 7	Bit 6	
Data Error SCSI	SPC	SPC operations
0	0	No parity error was detected in the transferred data.
0	1	During execution of an output operation in hardware transfer mode, a parity error was detected in the data to be sent to SCSI. The parity is checked regardless of the value of bit 3 (Parity Enable) of the SCTL register. The erroneous data (parity bit value) is corrected and then sent to SCSI.
1	1	A parity error was detected in the data received from SCSI during an input operation. The parity is checked only when bit 3 (Parity Enable) of the SCTL register is set to 1. After an error is detected, the parity bit is corrected. If the SPC serving as an INITIATOR detects this error during hardware transfer execution, it generates an ATN signal to SCSI. (See Figure 4.3.2) In this case, the MPU program must reset this error condition before the ATN signal is reset. If the SPC serving as a TARGET detects this error during hardware transfer execution, it follows the specification at bit 0 (Termination Mode) of the SCMD register. See 4.3 - SCMD register for detailed.
1	0	Undefined

Bit 3: TC Parity Error

Bit 3 indicates that a parity error occurred while the transfer byte counter (TCH, TCM, TCL) was being decreased.

Bit 2: Phase Error

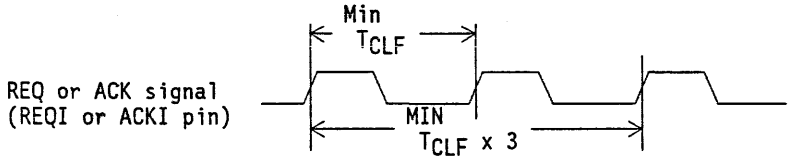
When SPC serves as an INITIATOR, the transfer phase has been changed in SCSI during hardware transfer mode operation (service required interrupt occurs). In this case, bit 2 indicates that:

(1) The new phase is a synchronous transfer mode DATA IN phase.

(2) The REQ signal has been received two or more times before the MPU program complete an interrupt processing and issue the Transfer command for the new phase. In this case, SPC cannot receive data and return the ACK signal normally.

Bit 1: Short Transfer Period

Bit 1 indicates that the REQ/ACK signal (input signal to REQI/ACKI pin) has a cycle exceeding the specified input range. (See Figure 4.12.1.) If this error occurs, the transfer sequence executed by SPC is not guaranteed.



T_{CLF}: A cycle of the clock signal supplied to SPC.

Fig. 4.12.1 Specified input cycle of REQ/ACK signal

Bit 0: Transfer Offset Error

Bit 0 indicates that one of the following errors has been detected during synchronous mode transfer. The offset value referred to below denotes the REQ ACK maximum offset value specified in the TMOD register.

(1) When SPC serves as a TARGET:

- The number of ACK signals received exceeds that of REQ signals transmitted.
- The number of REQ signals transmitted exceeds the offset value (SPC malfunction).

(2) When SPC serves as an INITIATOR:

- The number of REQ signals received exceeds the offset value.
- The number of ACK signals transmitted exceeds that of REQ signals received (SPC malfunction).

If this error occurs, the transfer sequence executed by SPC is not guaranteed.

4.12.2 Error Reset

To reset an error indication in the SERR register, do one of the following:

(1) Generate SCSI RESET condition (X'10' → SCMD)
(2) Reset & disable (Bit 7 of SCTL register)
(3) Control reset (Bit 6 of SCTL register)
(4) Interrupt (SPC hardware error) reset (X'02' → INTS)
Bits 7 and 6 (Data Error) of this register do not cause an interrupt, but can be reset by this means.

4.13 MBC REGISTER

OP	7	6	5	4	3	2	1	0	P
R	'0'				MBC				
					Bit 3	2	1	0	P

The MBC register controls the data count during transfer between the SPC internal data buffer register and the MPU (program transfer mode) or external buffer memory (DMA mode). When data is written into the TCL register, its four low-order bits are set as an initial value for MBC register. In an output operation, data is prefetched into the SPC internal data buffer register. Each time one byte is prefetched, the MBC register is decreased by one. Data prefetch stops when the transfer byte counter is decreased below 15 and the MBC register reaches 0.
In an input operation, data received from SCSI is stored in the internal data buffer register. Each time data is sent to the MPU or external buffer memory, the MBC register is decreased. The difference between the transfer byte counter and the MBC register corresponds to the byte count of data remaining in the internal data buffer register. While SPC is executing a DMA mode transfer operation, this register must not be read out.

4.14 EXTERNAL BUFFER REGISTER (EXBF)

OP	7	6	5	4	3	2	1	0	P
R/W	External Buffer								P
	Bit 7	6	5	4	3	2	1	0	

This register's address is reserved for access from the MPU data bus (D7 to D0, DP) to the DMA data bus (HDB7 to HDB0, HDBP) (not exist as an internal register in SPC). As shown in Fig. 4.14.1, the MPU program can execute a write/read to/from the external buffer memory by using this virtual register.

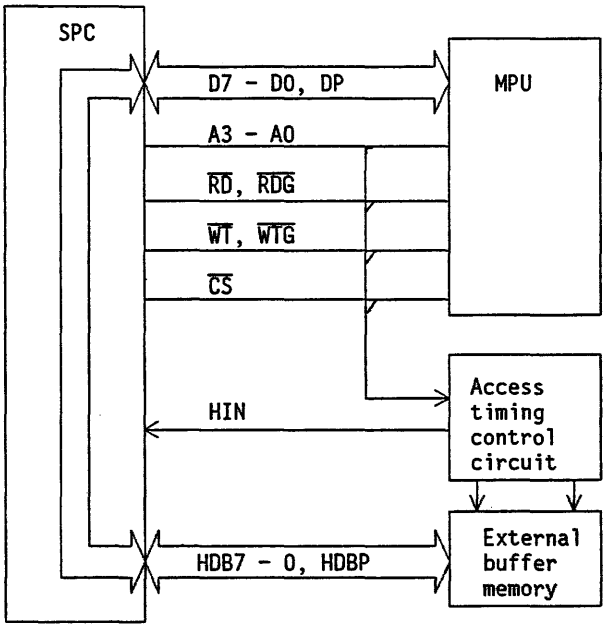


Fig. 4.14.1 Access from MPU to external buffer memory

4.15 SDGC REGISTER

OP	7	6	5	4	3	2	1	0	P
W	Diag REQ	Diag ACK	—	—	Diag BSY	Diag MSG	Diag C/D	Diag I/O	—

The SDGC register is used to operate SPC in diagnostic mode (with bit 5 [Diag Mode] of the SCTL register set to 1). To simulate the SCSI operation, the SDGC register bits are used as having alternative SCSI control signal lines.
In diagnostic mode, the SDGC register is used to check SPC internal operation. The diagnostic mode stops signaling to SCSI and nullifies input signals from SCSI except the data bus signals. The SPC internal operation can be performed in the ordinary manner. To check SPC internal operation, the MPU can manipulate the SDGC register's bits to generate input signals from SCSI.

The following bus phases can be simulated:

1) BUS FREE
2) ARBITRATION (Always win)
3) SELECTION (For INITIATE operation)
4) RESELECTION (For TARGET operation)
5) Information transfer (Input data manipulation not allowed in an input operation)

4.16 INITIALIZATION

SPC is in the reset state when the input to $\overline{RST}$ pin is low (hardware reset) or bit 7 (Reset & Disable) of the SCTL register is set to 1. SPC-SCSI operation is disabled until the SPC reset state is released. The MPU program shall release the reset state after initializing the SPC internal registers. The following SPC internal registers remain unchanged even in the SPC reset state:

- BDID register
- TMOD register
- Transfer byte counter
- SCMD register
- PCTL register
- TEMP register (for sending)

At the moment power is turned on, the contents of these internal registers are unpredictable even though hardware reset ($\overline{RST}$ input = low) is executed. After $\overline{RST}$ input is released, the MPU program shall initialize SPC as shown in Figure 4.16.1.

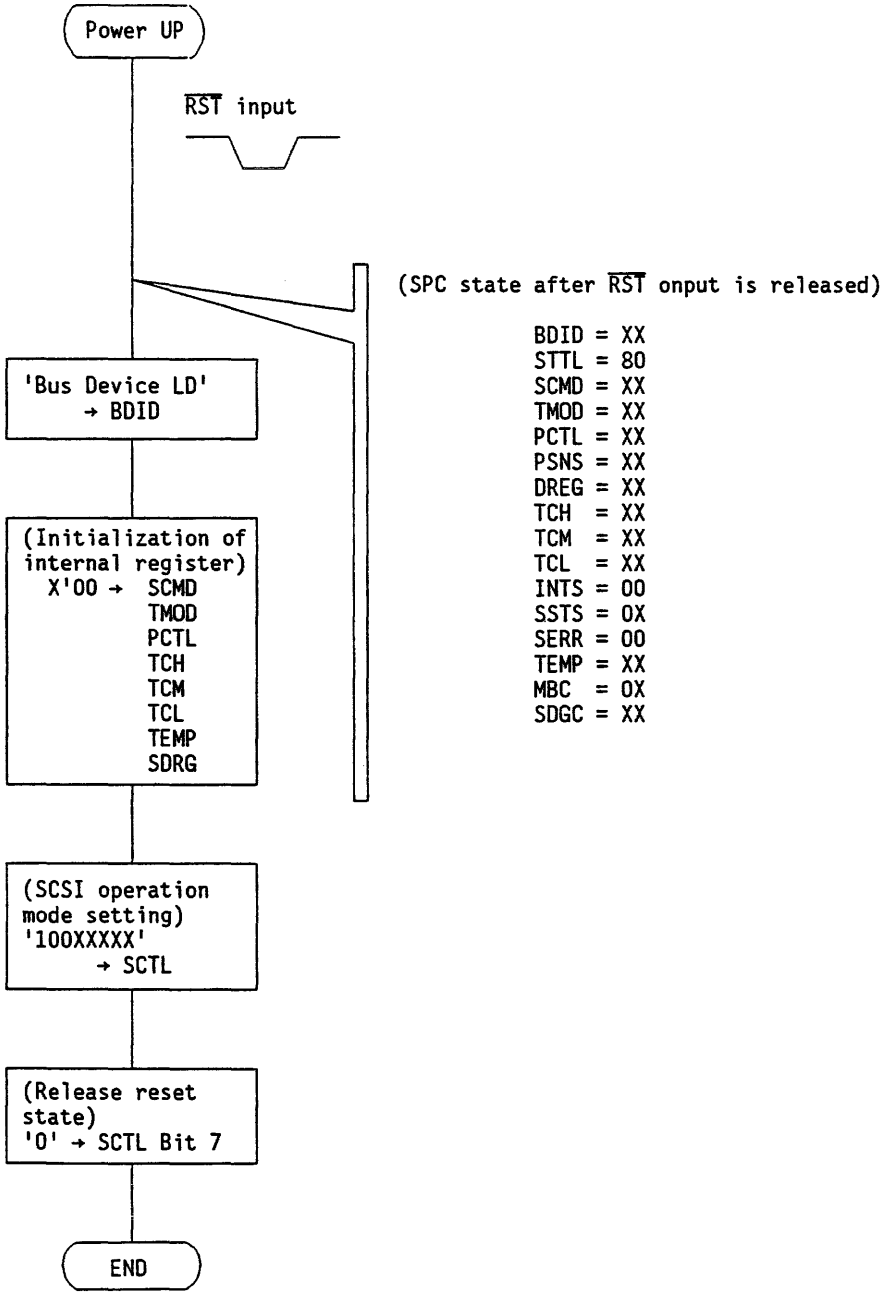


Fig. 4.16.1 SPC initialization (at power-on)

CHAPTER 5

EXAMPLES OF EXTERNAL CIRCUIT CONNECTIONS

Figure 5.1.1 shows the external circuit blocks that can be connected with this LSI circuit. The external circuit configuration depends on the application environment, purpose of use and performance required of this LSI. Examples of application of this LSI circuit are given below.

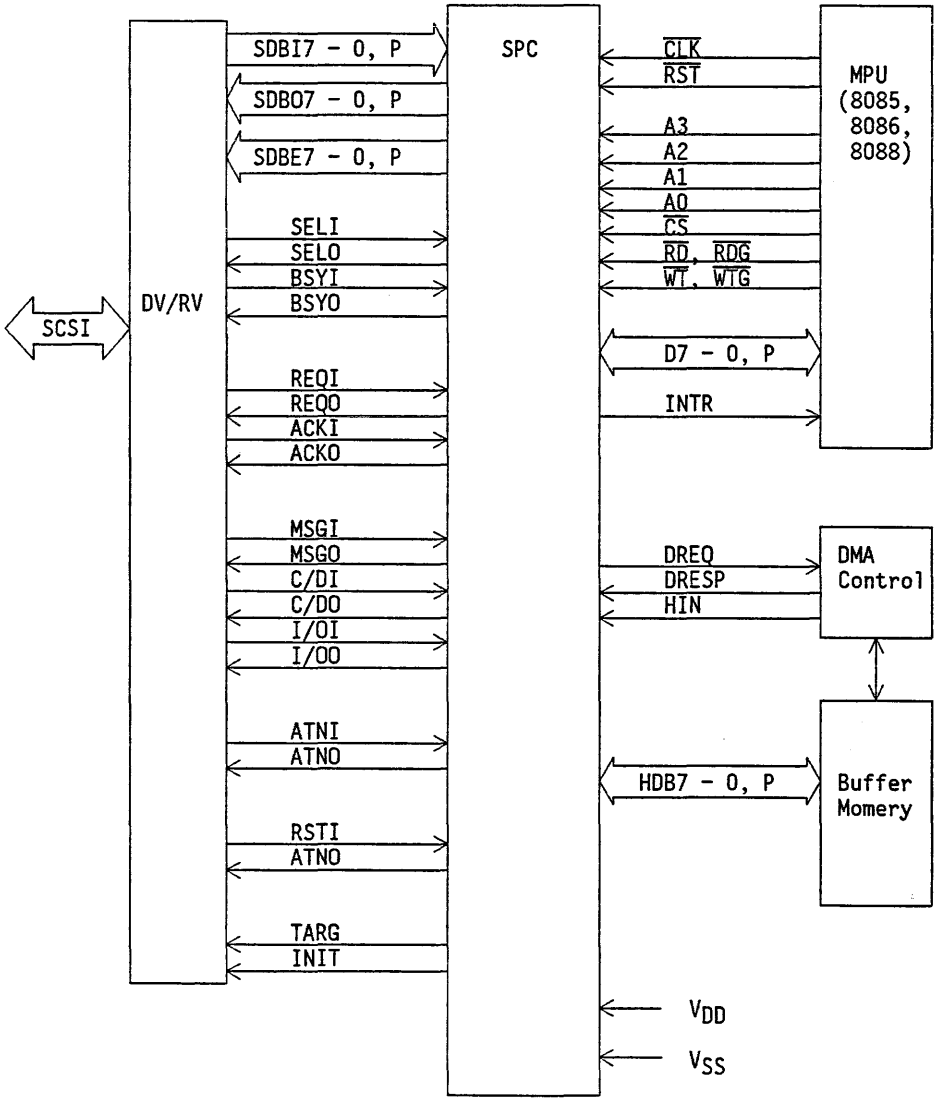


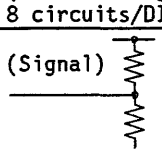
Fig. 5.1.1 Examples of external circuit connections

5.1 SCSI DRIVER/RECEIVER CIRCUITS

5.1.1 Single Ended Type

Figure 5.1.2 shows a example of the connection of the SPC and the SCSI single ended type driver/receiver circuit. Table 5.1.1 lists the major components of this SCSI driver/receiver circuit.

Table 5.1.1 Major components of single ended type SCSI driver/receiver circuit (example)

Component	Part No.	Manufacturer	Characteristics	Q'ty
REQ/ACK signal driver	MB412 *	Fujitsu	(Tri-state buffer circuit) 2 circuits/DIP 14	1
REQ/ACK signal receiver	MB413 * Resistor Resistor Capacitor	Fujitsu - - -	4 circuits/DIP 16 390Ω ±2% 1/4 W 200Ω ±2% 1/4 W 0.1μF/50 V Ceramic	1 1 1 1
Other signal driver	MB463 *	Fujitsu	(Open-collector buffer circuit) 4 circuits/DIP 14	4
Other signal receiver	74LS240	Fujitsu TI	(Schmitt trigger inverter) 8 circuits/DIP 20	2
Terminator (Required only when the driver/receiver is located at either end of SCSI)	-	-		18 elements

* Note : The MB412 is compatible with the SN7519.
The MB413 is compatible with the Am26LS32.
The MB463 is compatible with the SN7438.

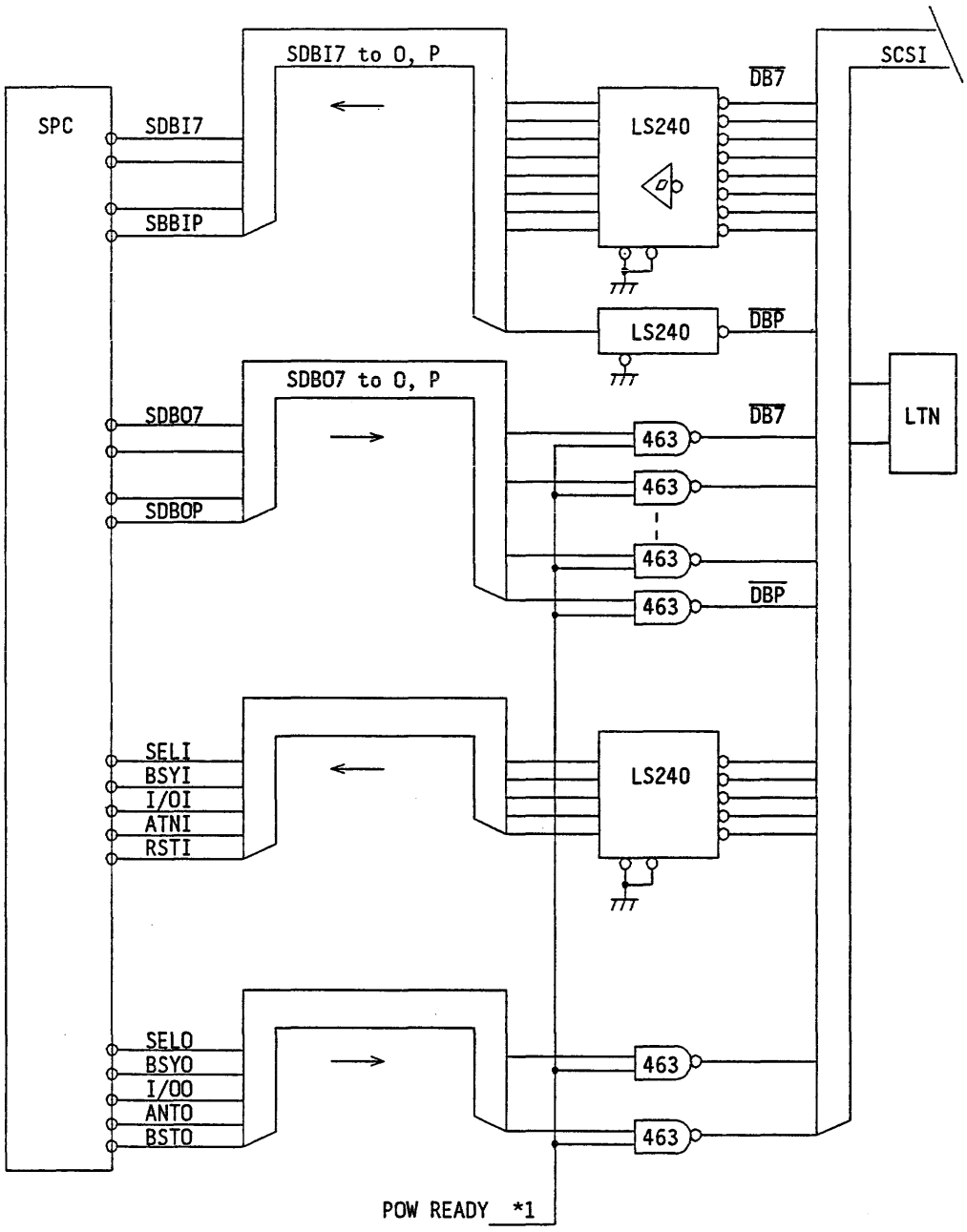
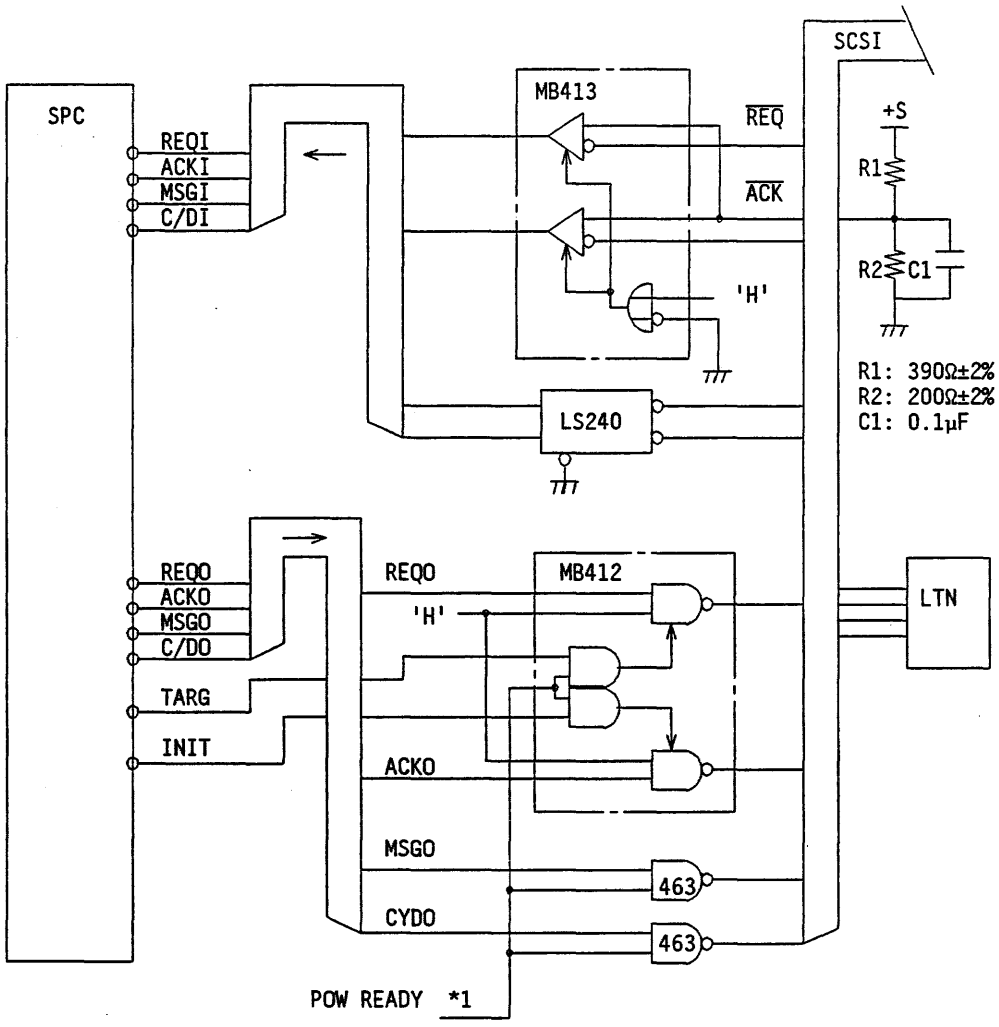


Fig. 5.1.2 Example of single ended type SCSI driver/receiver circuit
(continued on next sheet)



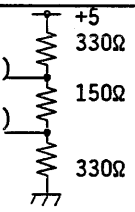
*1: It is recommended to protect against noise generated at power on/off.

Fig. 5.1.2 Example of single ended type SCSI driver/receiver circuit (continued)

5.1.2 Differential Type

Figure 5.1.3 shows a example of the connection of the SPC and the SCSI differential type driver/receiver circuit. Table 5.1.2 lists the major components of this SCSI driver/receiver.

Table 5.1.2 Major components of differential type SCSI driver/receiver circuit (example)

Component	Part No.	Manufacturer	Characteristics	Q'ty
Driver/receiver (Common to all signals)	SN75176	TI	(Differential transceiver) 1DV +1RV/Dip 8	18
Terminator (Required only when the driver/receiver is located at either end of SCSI)	-	-		18 elements

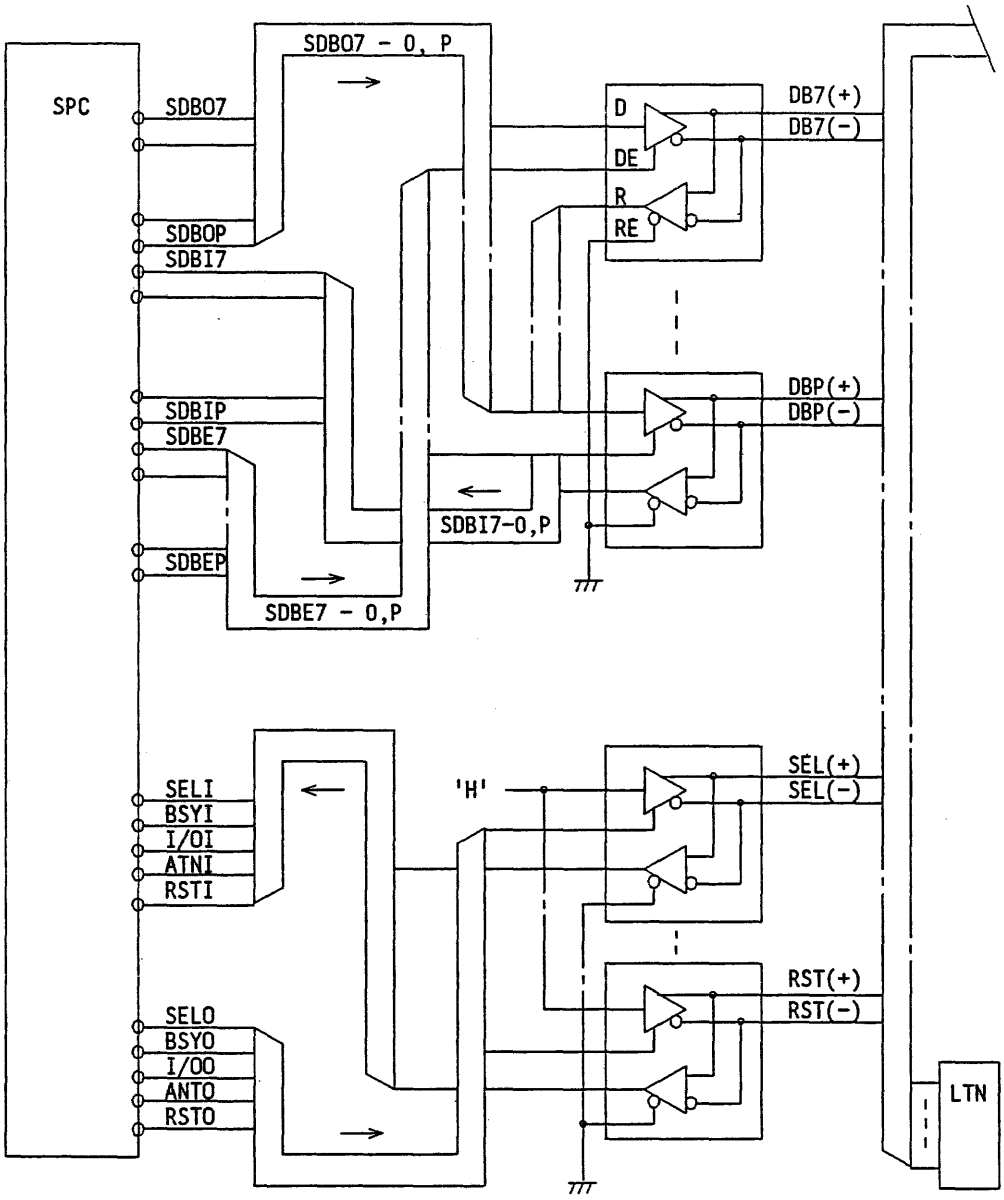


Fig. 5.1.3 Example of differential type SCSI driver/receiver circuit
(continued on next sheet)

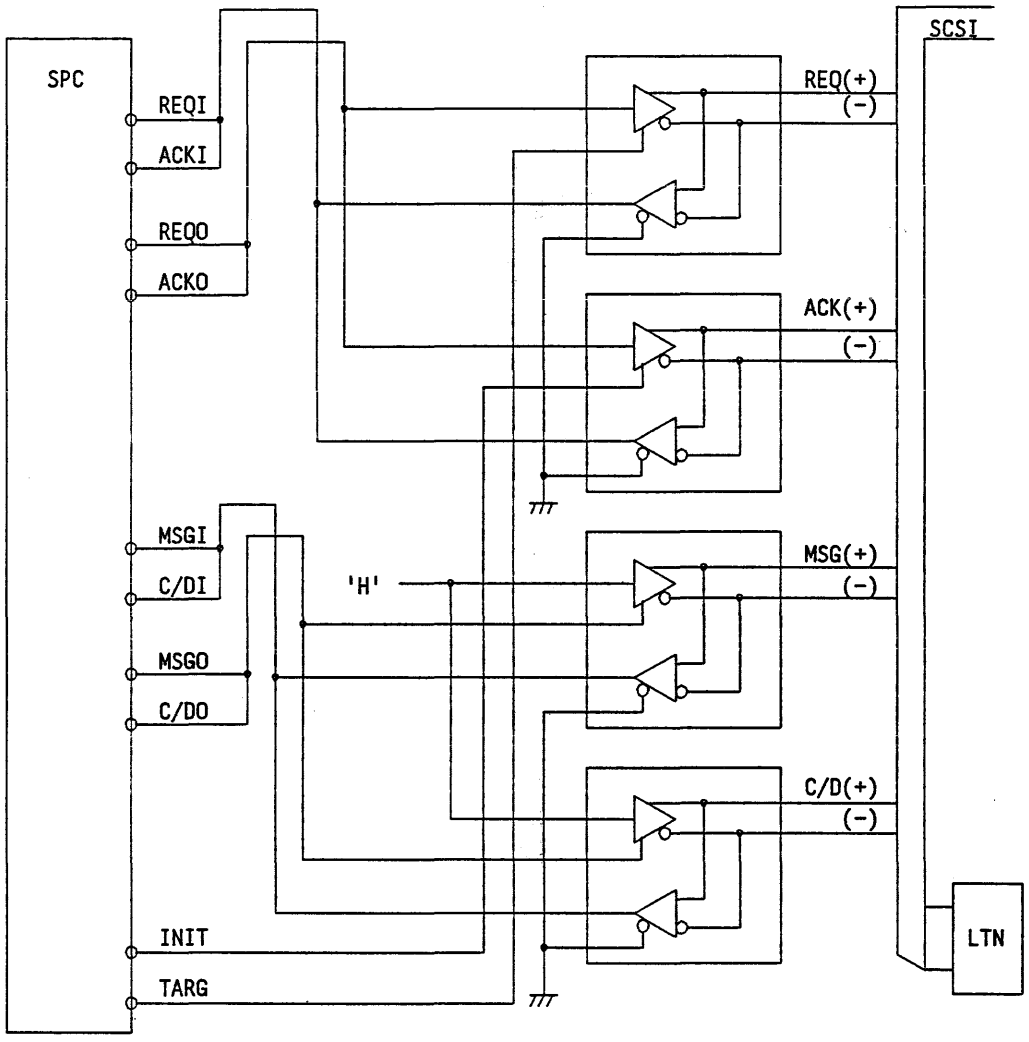


Fig. 5.1.3 Example of differential type SCSI driver/receiver circuit (continued)

5.2 EXTERNAL DATA BUFFER

To provide a buffer area for high-speed data transfer or a temporary storage for data to be transferred, the external data buffer memory can be connected to SPC as shown in Figure 5.1.1. In this case, a buffer control circuit is required to control the timing of data transfer between SPC and external buffer memory. To execute the transfer phase on SCSI, specify DMA transfer mode for SPC. SPC accesses the external buffer memory with the timing sequences shown in Figures 5.2.1 and 5.2.2. Data is transferred via the DMA data bus lines (HDB7 to HDB0, HDBP). The transfer direction must be specified externally using the HIN signal. When requesting access to the external buffer memory, SPC makes the DREQ signal active. In an input operation, the DREQ signal is sent out when the SPC internal data buffer register (8 bytes) holds data received from SCSI. In an output operation, the DREQ signal is sent out when data corresponding to the byte count specified in the transfer byte counter is not all prefetched, and when the internal data buffer register has free byte locations available. The external buffer control circuit must return the DRESP signal in response to the DREQ signal on completion of transferring each byte. DRESP is a pulse signal whose trailing edge is used to indicate the end of transfer. The DREQ signal is held active as long as the above conditions exist in SPC (this signal is not a transfer request signal for each byte). The access interface signals (DREQ, DRESP, HIN, HDB7 to HDB0, HDBP) to the external buffer memory are asynchronous with an SPC clock signal supplied to the $\overline{CLK}$ pin.

(1) HIN signal puts the DMA data bus (HDB7 to 0, P) in an output mode. However, the value on the DMA data bus is unpredictable until data is loaded into the SPC internal data buffer register from SCSI.

(2) After receiving data from SCSI, SPC issues the DREQ signal (transfer request) to the external buffer memory. At this time, valid data is placed on the DMA data bus.

(3) Data on the DMA data bus is held until the trailing edge of the DRESP signal.

(4) After the DRESP signal is received, valid data is unloaded from the SPC internal data buffer register. Then, the DREQ signal becomes inactive to stop transfer with the external buffer memory until the next data becomes available.

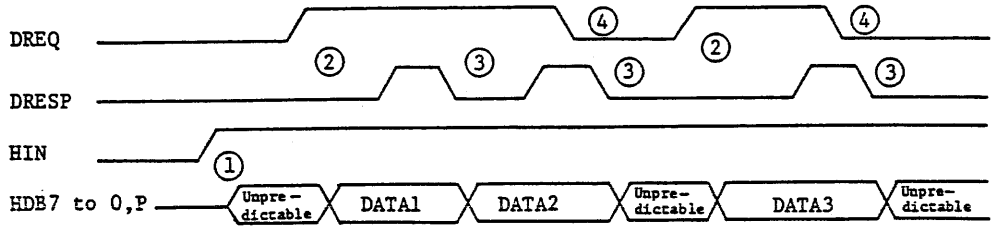


Fig. 5.2.1 Transfer with external data buffer (input operation)

(1) As long as the HIN signal is low, the DMA data bus (HDB7 to 0, P) is in an input mode.

(2) A transfer request (DREQ) signal is issued when the SPC internal data buffer register has free byte locations available for prefetching data.

(3) The external buffer control circuit puts data onto the DMA data bus and also sends the DRESP signal in response. On the trailing edge of the DRESP signal, SPC loads data from the DMA bus into the internal data buffer register.

(4) When no free location is available in the SPC internal data buffer register, the DREQ signal becomes inactive. Then, transfer from the external buffer memory is stopped until the next data prefetch becomes available.

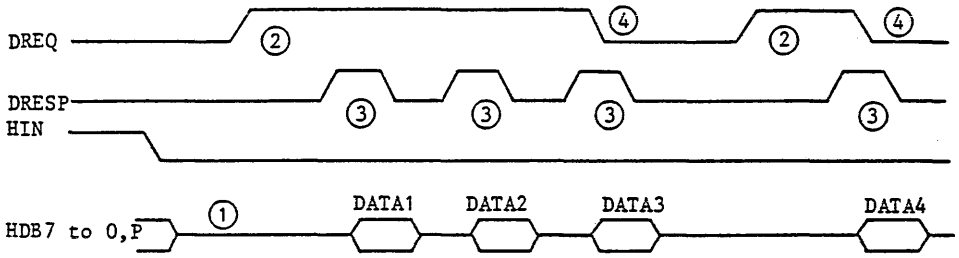


Fig. 5.2.2 Transfer to external data buffer (output operation)

CHAPTER 6

AC CHARACTERISTICS

In this chapter, the input/output signal timing is specified, under the following conditions:

(1) Operating temperature

T_A = 0 to 70 °C

(2) Power supply voltage

V_{DD} = 4.75 to 5.25 V

(3) Input/output condition

The input/output condition in section 1.3 "Electrical Specifications" should be satisfied.

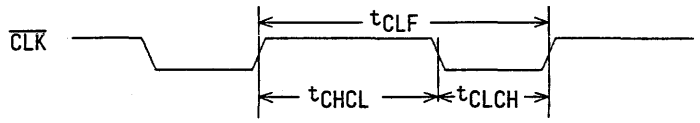
(4) Timing measurement

To be specified at the input/output pins of this LSI circuit.

6.1 MPU INTERFACE

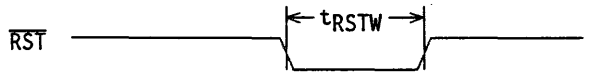
6.1.1 Clock Signal

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{CLF}	Clock Cycle	125		200	ns
t_{CHCL}	Clock High	65			ns
t_{CLCH}	Clock Pulse Width (Low)	40			ns



6.1.2 Reset Signal

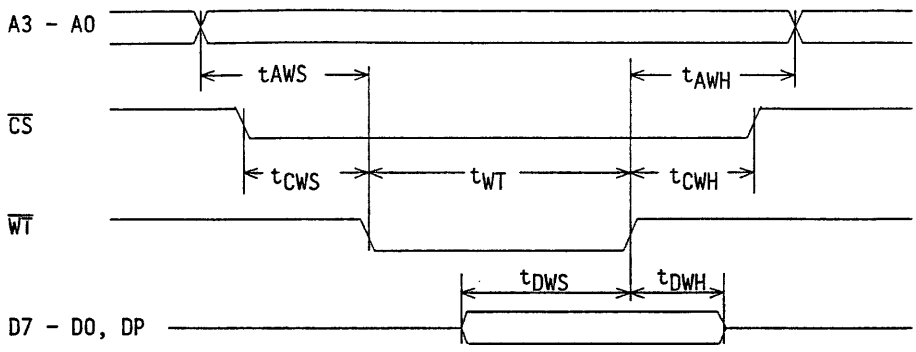
Symbol	Parameter	MIN	TYP	MAX	Unit
t_{RSTW}	Reset Pulse Width	50			ns



6.1.3 Write Cycle

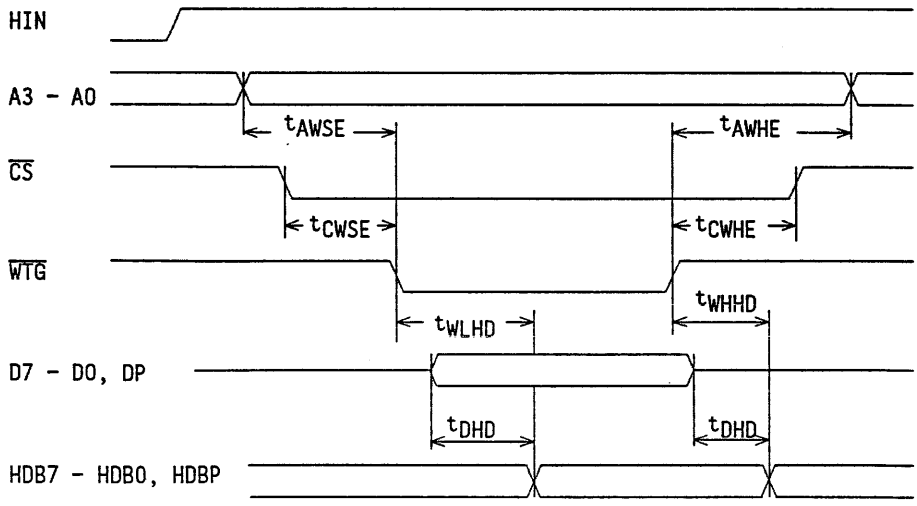
(1) Registers other than EXBF

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{AWS}	Address Setup	35			ns
t_{AWH}	Address Hold	5			ns
t_{CWS}	$\overline{CS}$ Setup	20			ns
t_{CWH}	$\overline{CS}$ Hold	5			ns
t_{DWS}	Data Bus Setup	25			ns
t_{DWH}	Data Bus Hold	20			ns
t_{WT}	$\overline{WT}$ pulse Width	50			ns



(2) EXBF register

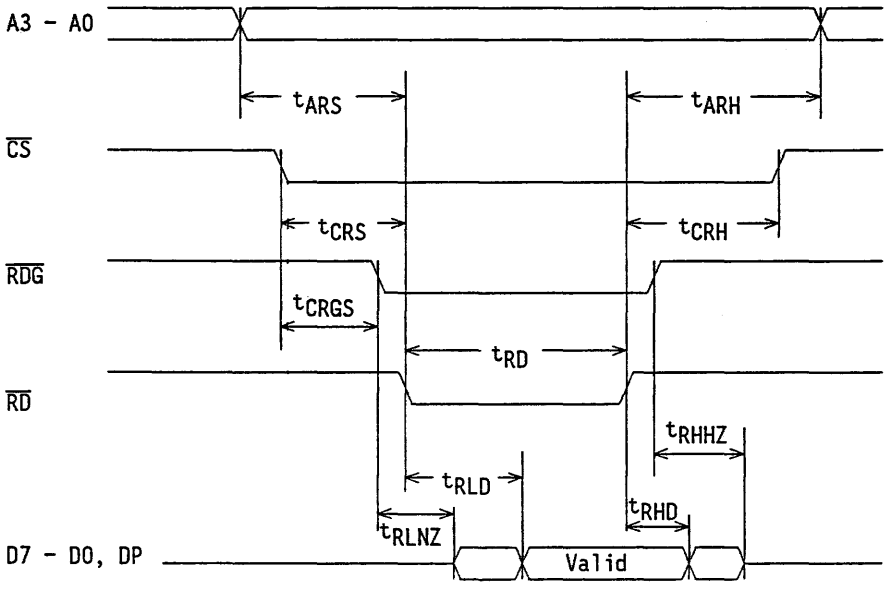
Symbol	Parameter	MIN	TYP	MAX	Unit
t_{AWSE}	Address Setup	20			ns
t_{AWHE}	Address Hold	5			ns
t_{CWSE}	$\overline{CS}$ Setup	5			ns
t_{CWHE}	$\overline{CS}$ Hold	5			ns
t_{WLHD}	$\overline{WTG}$ Low → DMA Data Bus (HDB7 to 0, P)			60	ns
t_{WHHD}	$\overline{WTG}$ High → DMA Data Bus (HDB7 to 0, P)	10			ns
t_{DHD}	MPU Data Bus (D7 to 0, P) DMA Data Bus (HDB7 to 0, P)	10		50	ns



6.1.4 Read Cycle

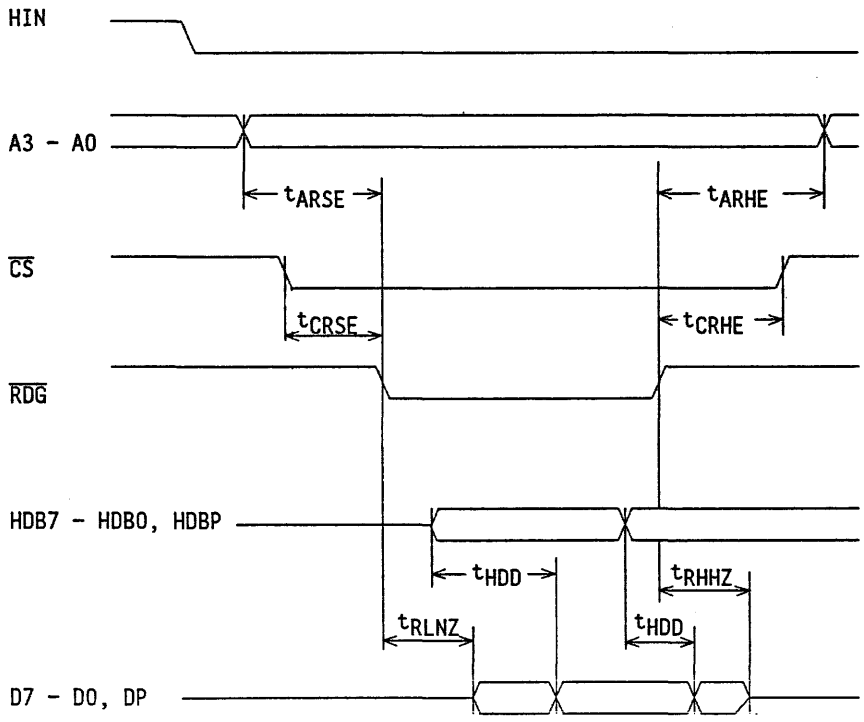
(1) Registers other than EXBF

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{ARS}	Address Setup	35			ns
t_{ARH}	Address Hold	5			ns
t_{CRS}	$\overline{CS}$ Setup (RD)	5			ns
t_{CRH}	$\overline{CS}$ Hold	5			ns
t_{RD}	$\overline{RD}$ Pulse Width	50			ns
t_{RLNZ}	$\overline{RDG}$ Low → Data Output	10		45	ns
t_{RHHZ}	$\overline{RDG}$ High → D7 to 0, P High Z			40	ns
t_{RLD}	$\overline{RD}$ Low → Data Establish			85	ns
t_{RHD}	$\overline{RD}$ High → Data hold	10			ns
t_{CRGS}	$\overline{CS}$ Setup (RDG)	5			ns



(2) EXBF register

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{ARSE}	Address Setup	35			ns
t_{ARHE}	Address Hold	5			ns
t_{CRSE}	$\overline{CS}$ Setup	5			ns
t_{CRHE}	$\overline{CS}$ Hold	5			ns
t_{RLNZ}	$\overline{RDG}$ Low → Data Output	10		45	ns
t_{RHHZ}	$\overline{RDG}$ High → D7 to 0,P High Z			40	ns
t_{HDD}	DMA Data Bus (HDB7 to 0, P) to MPU Data Bus (D7 to 0, P)	5		50	ns

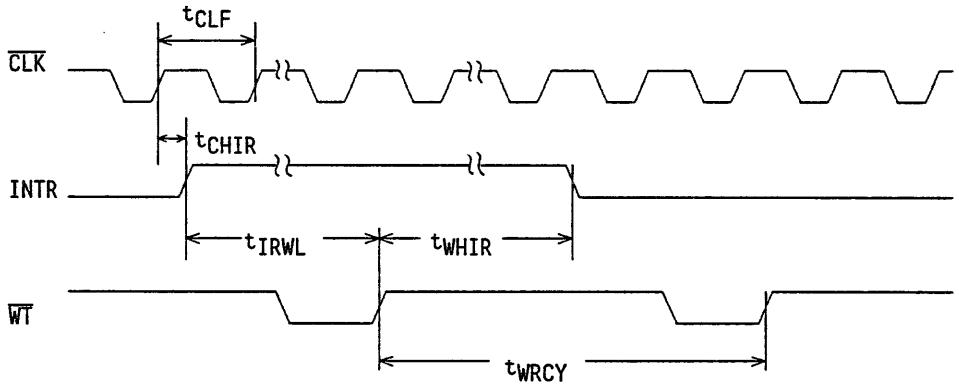


6.1.5 Interrupt

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{CHIR}	$\overline{CLK}$ High → INTR High	5		45	ns
t_{IRWL}	INTR → $\overline{WT}$	5			ns
t_{WHIR}	$\overline{WT}$ High → INTR Low (Interrupt Reset)	t_{CLF} + 10		$2t_{CLF}$ + 50	ns
t_{WRCY}	Interrupt Reset Cycle time *1	$4t_{CLF}$			ns

t_{CLF} : See 6.1.1

*1 : When interrupt reset is continued.

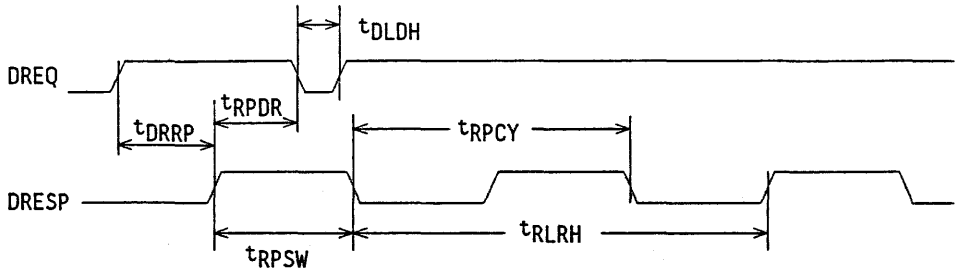


6.2 DMA INTERFACE

6.2.1 Access Timing

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{DRRP}	DREQ High → DRESP High	t_{CLF}			ns
t_{RPDR}	DRESP High → DREQ Low			80	ns
t_{DLDH}	DREQ Low → DREQ High	5			ns
t_{RPSW}	DRESP Pulse Width	50			ns
t_{RPCY}	DRESP Cycle Time (1)	$2t_{CLF}$			ns
t_{RLRH}	DRESP Cycle Time (2)	$3t_{CLF}$			ns

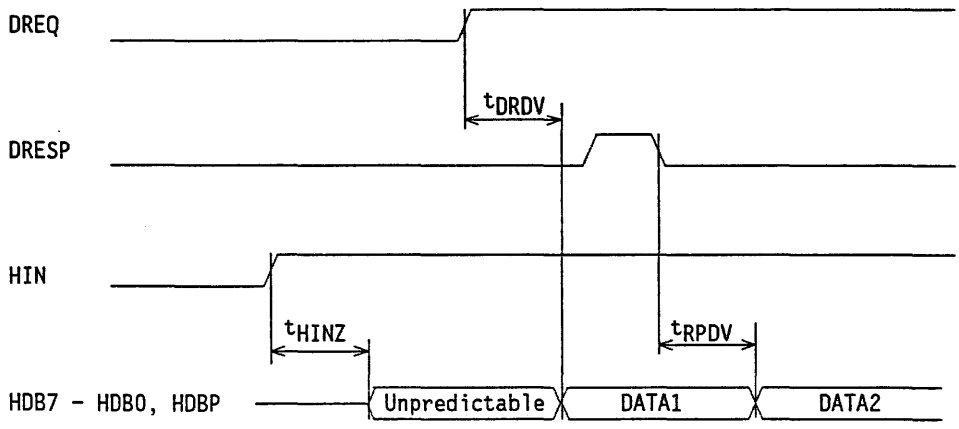
t_{CLF} : See 6.1.1



6.2.2 Input Operation

(SPC to External data buffer)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{HINZ}	HIN High → HDB7 to 0, P Data Output	10		40	ns
t_{DRDV}	DREQ High → Data Establish			85	ns
t_{RPDV}	DRESP Low → Data Change	15		75	ns

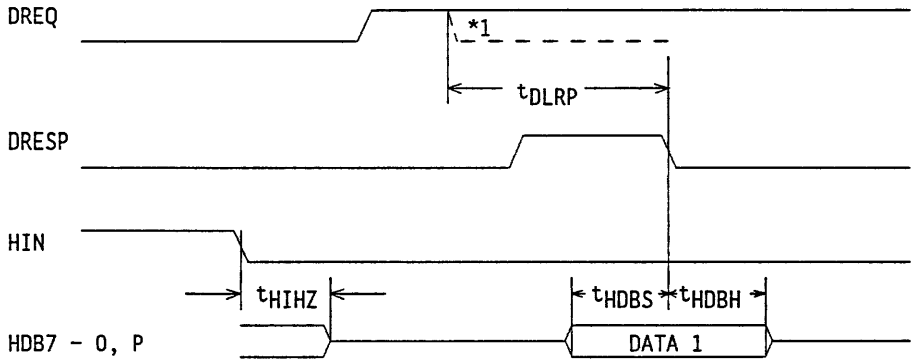


6.2.3 Output Operation

(External data buffer to SPC)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{HIHZ}	HIN Low → HDB7 to 0,P High Z			35	ns
t_{HDBS}	Data Bus Setup	20			ns
t_{HDBH}	Data Bus Hold	20			ns
t_{DLRP}	DREQ Low → DRESP *1			$5t_{CLF}$	ns

t_{CLF} : See 6.1.1



*1 In the following cases, the DREQ signal becomes inactive asynchronously with the DRESP signal to stop refetching data during an output operation:

- When the Transfer Pause command is issued in the SPC serving as a TARGET
- When the Transfer Phase is changed in the SPC serving as an INITIATOR

In these cases, the last DRESP signal response must not exceed t_{DLRP}.

6.3 SCSI INTERFACE

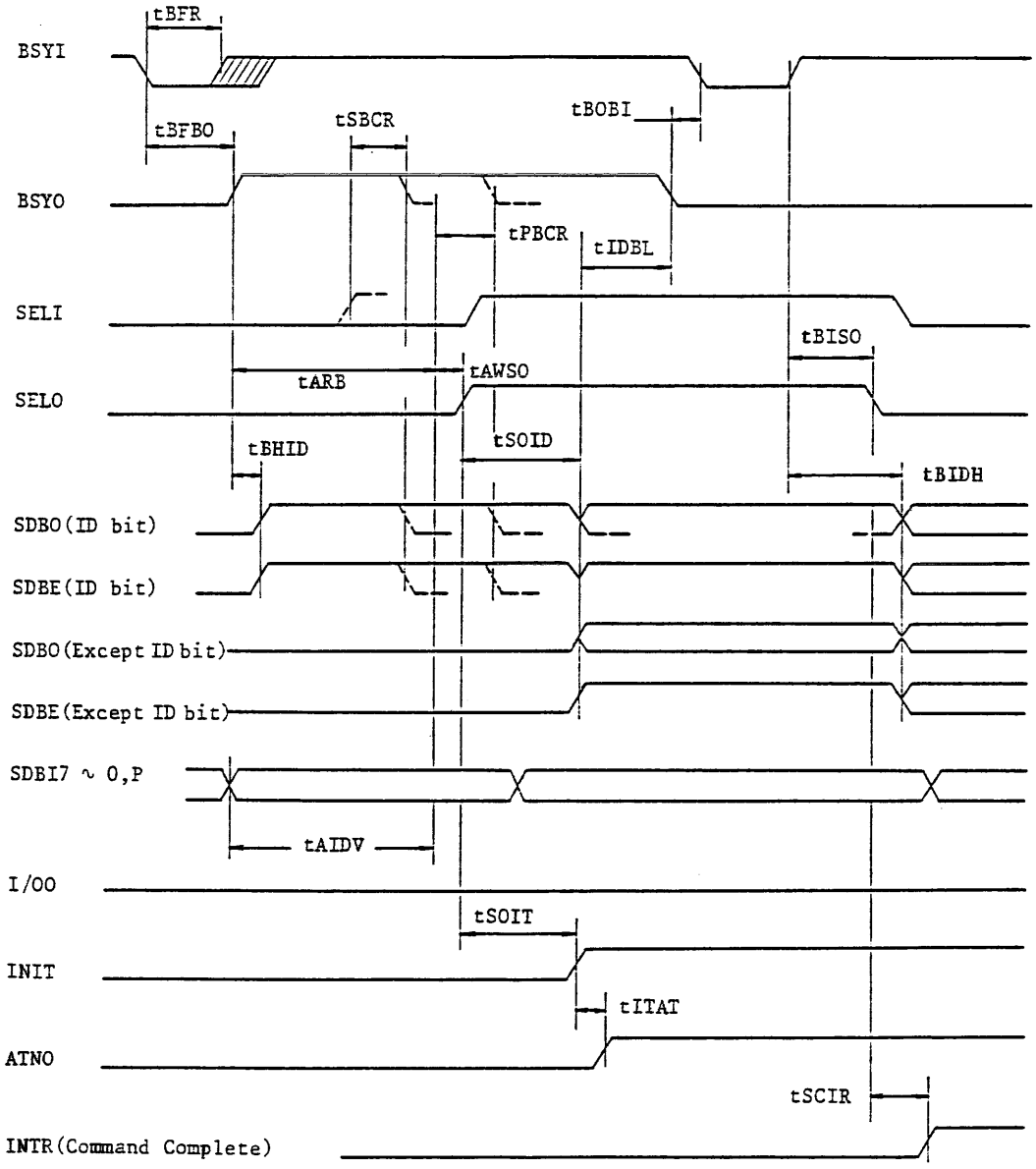
6.3.1 SELECTION Phase

(1) INITIATOR (With arbitration)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{BFR}	Bus Free Time	$4t_{CLF}$ + 50			ns
t_{BFBO}	BSYI Low → BSYO High (Start of arbitration)	(6+n) x t_{CLF} + 5		(7+n) x t_{CLF} + 65	ns
t_{BHID}	BSYO High → ID Bit High	5		55	ns
t_{ARB}	BSYO High → Prioritize	$32t_{CLF}$ - 40			ns
t_{AIDV}	Data Bus Valid (High Priority Bit) → Prioritize	70			ns
	Data Bus Valid (Low Priority Bit) → Prioritize	5			ns
t_{AWSO}	Bus Usage Permission Granted → SELO High	5		45	ns
t_{SOID}	SELO High → Data Bus (ID) Send	$11t_{CLF}$ - 30			ns
t_{SOIT}	SELO High → INIT High	$11t_{CLF}$ - 50			ns
t_{ITAT}	INIT High → ATNO High	10		55	ns
t_{IDBL}	Data Bus (ID) Send → BSYO Low	$2t_{CLF}$ - 80			ns
t_{BOBI}	BSYO Low → BSYI Low	5		t_{CLF}	ns
t_{BISO}	BSYI High → SELO Low	$2t_{CLF}$ + 5			ns
t_{BIDH}	BSYI High → Data Bus (ID) Hold	$2t_{CLF}$ + 5			ns
t_{SCIR}	SELO Low → INTR High			75	ns
t_{SBCR}	SELI High → BSYO, ID Bit Low			$3t_{CLF}$ + 115	ns
t_{PBCR}	Prioritize → BSYO, ID Bit Low			125	ns

t_{CLF} : See 6.1.1

n : TCL register set value (See 4.3.2 (2) - Select command.)

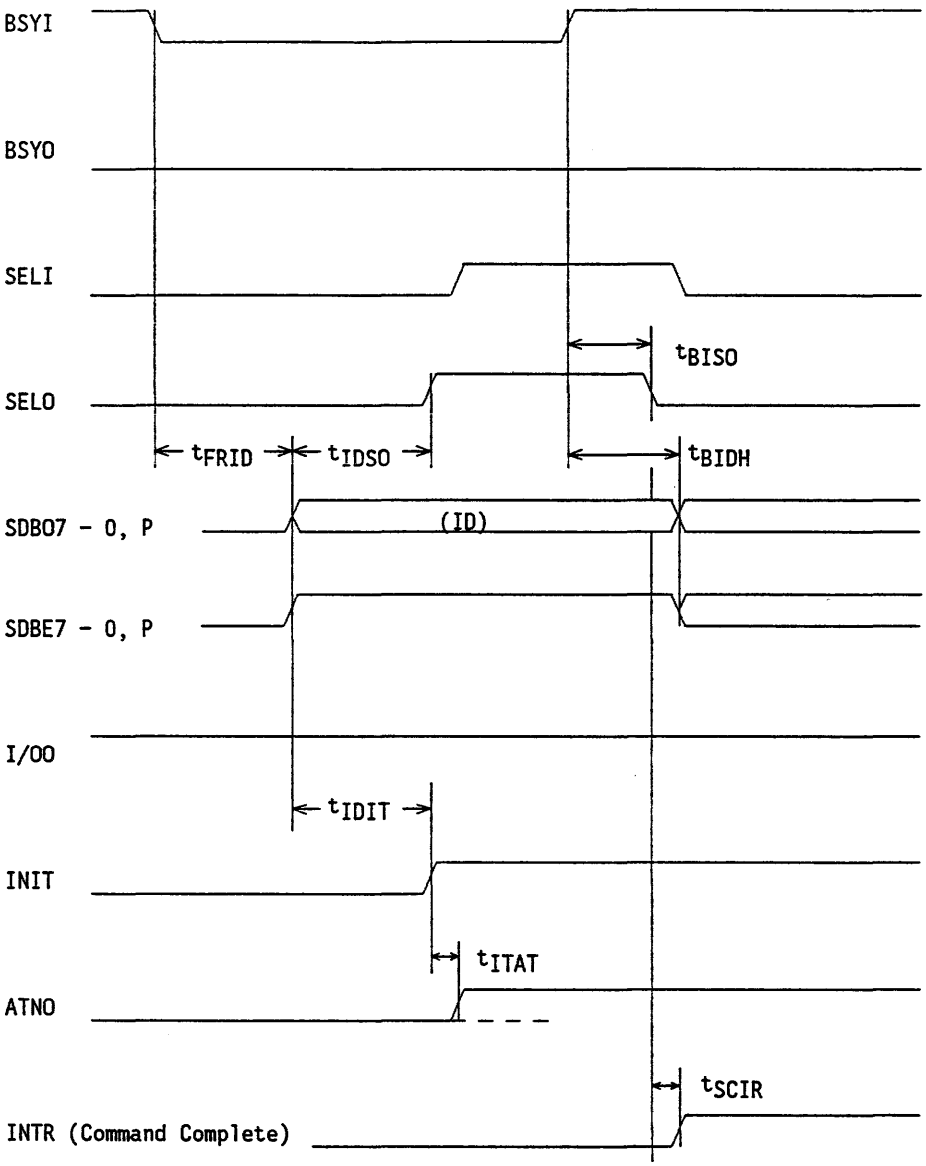

tBFR
BSYI
tBFBO
tSBCR
tBOBI
BSYO
tPBCR
tIDBL
SELI
tBISO
tARB
tAWSO
SELO
tBHID
tSOID
tBIDH
SDBO(ID bit)
SDBE(ID bit)
SDBO(Except ID bit)
SDBE(Except ID bit)
SDBI7 ∿ 0,P
tAIDV
I/OO
tSOIT
INIT
tITAT
ATNO
tSCIR
INTR(Command Complete)

(2) INITIATOR (Without arbitration)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{FRID}	Bus Free → Data Bus (ID) Send	$(6+n) \times t_{CLF} + 5$		$(7+n) \times t_{CLF} + 85$	ns
t_{IDSO}	ID Send → SELO High	$11t_{CLF} - 80$			ns
t_{IDIT}	ID Send → INIT High	$11t_{CLF} - 80$			ns
t_{ITAT}	INIT High → ATNO High	10		55	ns
t_{BISO}	BSYI High → SELO Low	$2t_{CLF} + 5$			ns
t_{BIDH}	BSYI High → Data Bus (ID) Hold	$2t_{CLF} + 5$			ns
t_{SCIR}	SELO Low → INTR High			75	ns

t_{CLF} : See 6.1.1

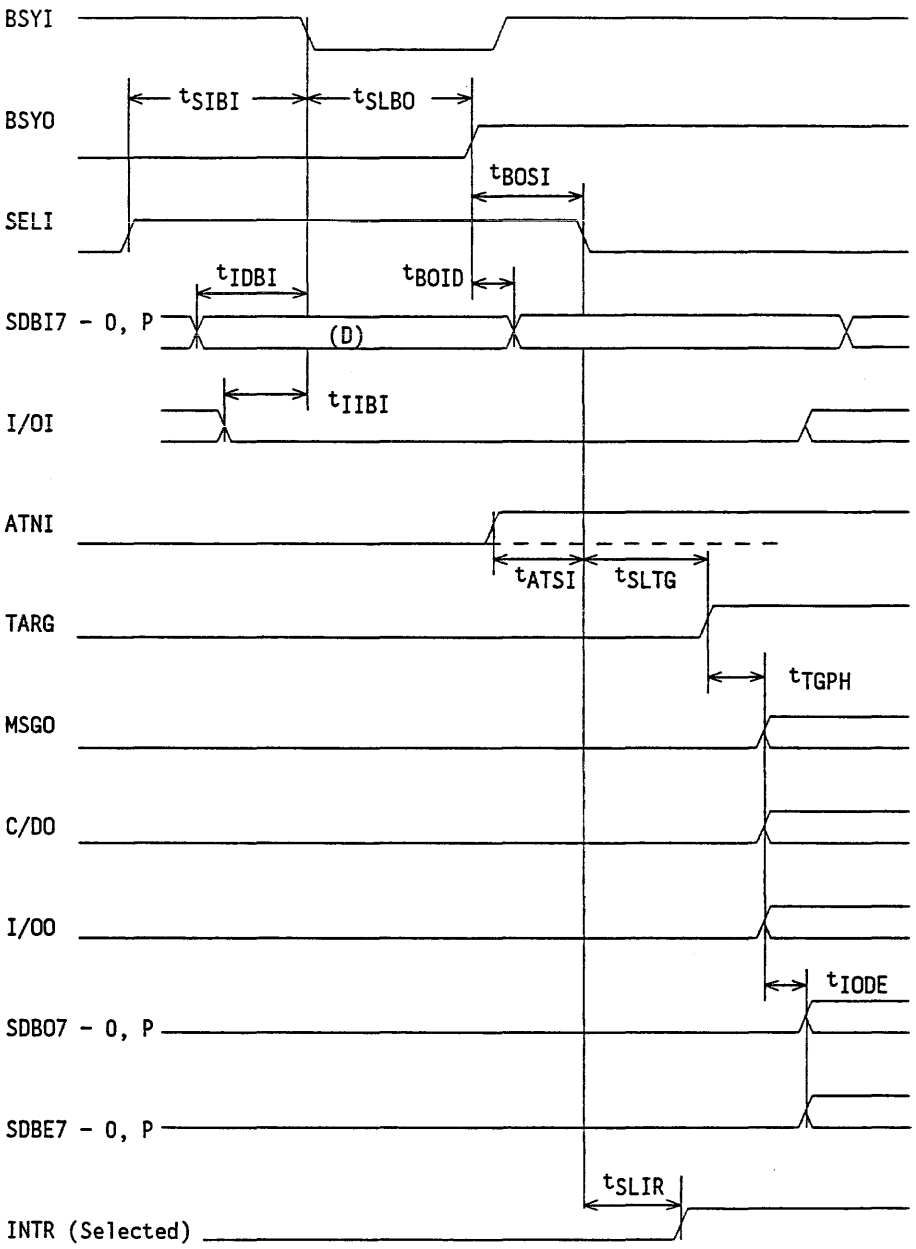
n : TCL register set value (See 4.3.2 (2) - Select command.)


BSYI
BSYO
SELI
SELO
tBISO
tFRID
tIDSO
tBIDH
SDBO7 - 0, P
(ID)
SDBE7 - 0, P
I/OO
tIDIT
INIT
tITAT
ATNO
tSCIR
INTR (Command Complete)

(3) TARGET (With arbitration)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{FIBI}	SELI High → BSYI Low	5			ns
t_{IDBI}	Data Bus (ID) Valid → BSYI Low	5			ns
t_{IIBI}	I/OI Low → BSYI Low	5			ns
t_{SLBO}	BSYI Low → BSYO High (Response time)	$4t_{CLF} + 5$		$5t_{CLF} + 60$	ns
t_{BOID}	BSYO High → Data Bus (ID) Hold	15			ns
t_{BOSI}	BSYO High → SELI Low	5			ns
t_{ATSI}	ATNI High → SELI Low	5			ns
t_{SLTG}	SELI Low → TARG High	$3t_{CLF} + 5$		$4t_{CLF} + 60$	ns
t_{TGPH}	TARG High → Phase Signal Output	10			ns
t_{IODE}	I/OO High → Data Bus Enable	$3t_{CLF} + 5$			ns
t_{SLIR}	SELI Low → INTR High			$3t_{CLF} + 65$	ns

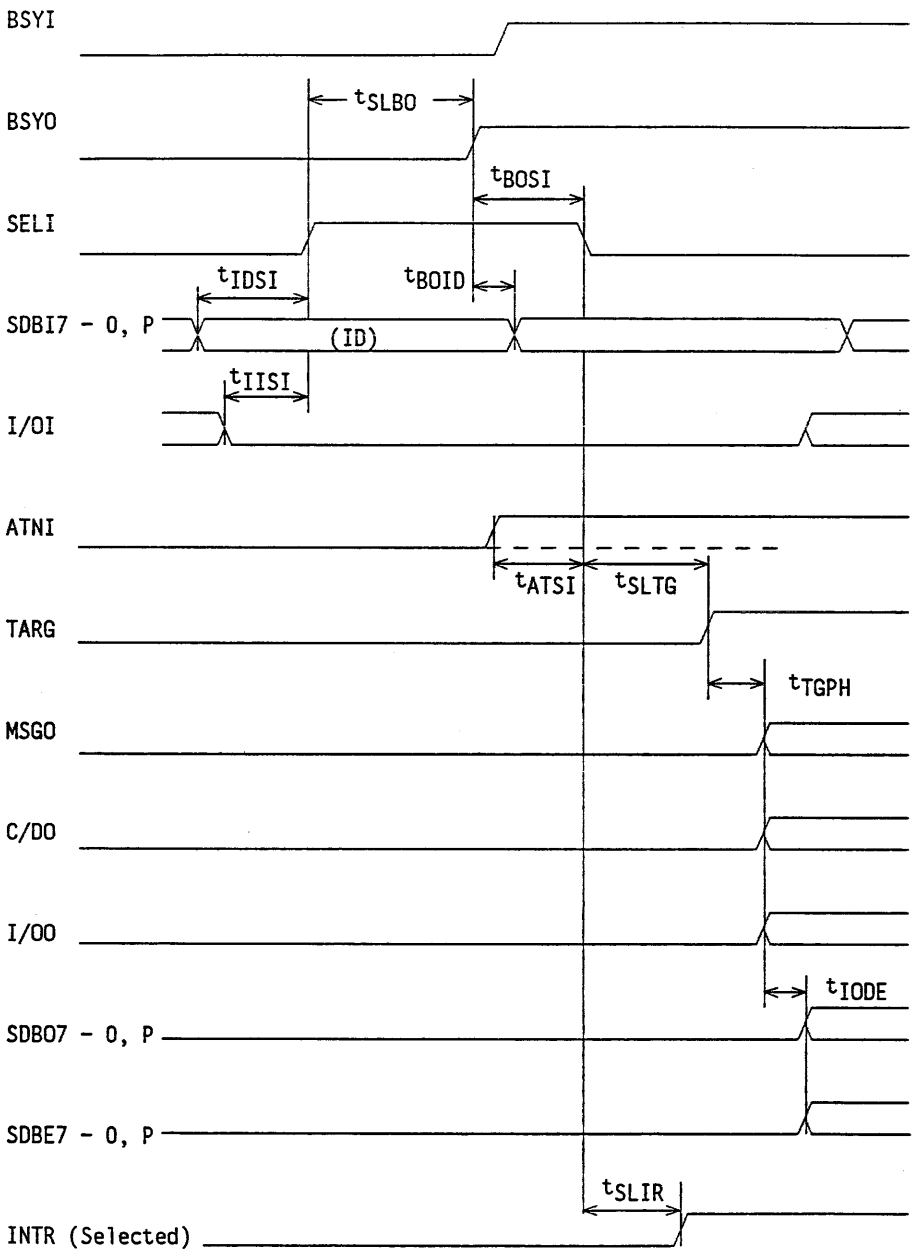
t_{CLF} : See 6.1.1


BSYI
BSYO
SELI
SDBI7 - 0, P
I/OI
ATNI
TARG
MSGO
C/DO
I/OO
SDBO7 - 0, P
SDBE7 - 0, P
INTR (Selected)
tSIBI
tSLBO
tBOSI
tIDBI
tBOID
(D)
tIIBI
tATSI
tSLTG
tTGPH
tIODE
tSLIR

(4) TARGET (Without arbitration)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{IDSI}	Data Bus (ID) Valid → SELI High	5			ns
t_{IISI}	I/OI Low → SELI High	5			ns
t_{SLBO}	SELI High → BSYO High (Response time)	$2t_{CLF}$ + 5		$3t_{CLF}$ + 65	ns
t_{BOID}	BSYO High → Data Bus (ID) Hold	15			ns
t_{BOSI}	BSYO High → SELI Low	5			ns
t_{ATSI}	ATNI High → SELI Low	5			ns
t_{SLTG}	SELI Low → TARG High	$3t_{CLF}$ + 5		$4t_{CLF}$ + 60	ns
t_{TGPH}	TARG High → Phase Signal Output	10			ns
t_{IODE}	I/OO High → Data Bus Enable	$3t_{CLF}$ + 5			ns
t_{SLIR}	SELI Low → INTR High			$3t_{CLF}$ + 65	ns

t_{CLF} : See 6.1.1


BSYI
BSYO
tSLBO
tBOSI
SELI
tIDSI
tBOID
SDBI7 - 0, P
(ID)
tIISI
I/OI
ATNI
tATSI
tSLTG
TARG
tTGPH
MSGO
C/DO
I/OO
tIODE
SDBO7 - 0, P
SDBE7 - 0, P
tSLIR
INTR (Selected)

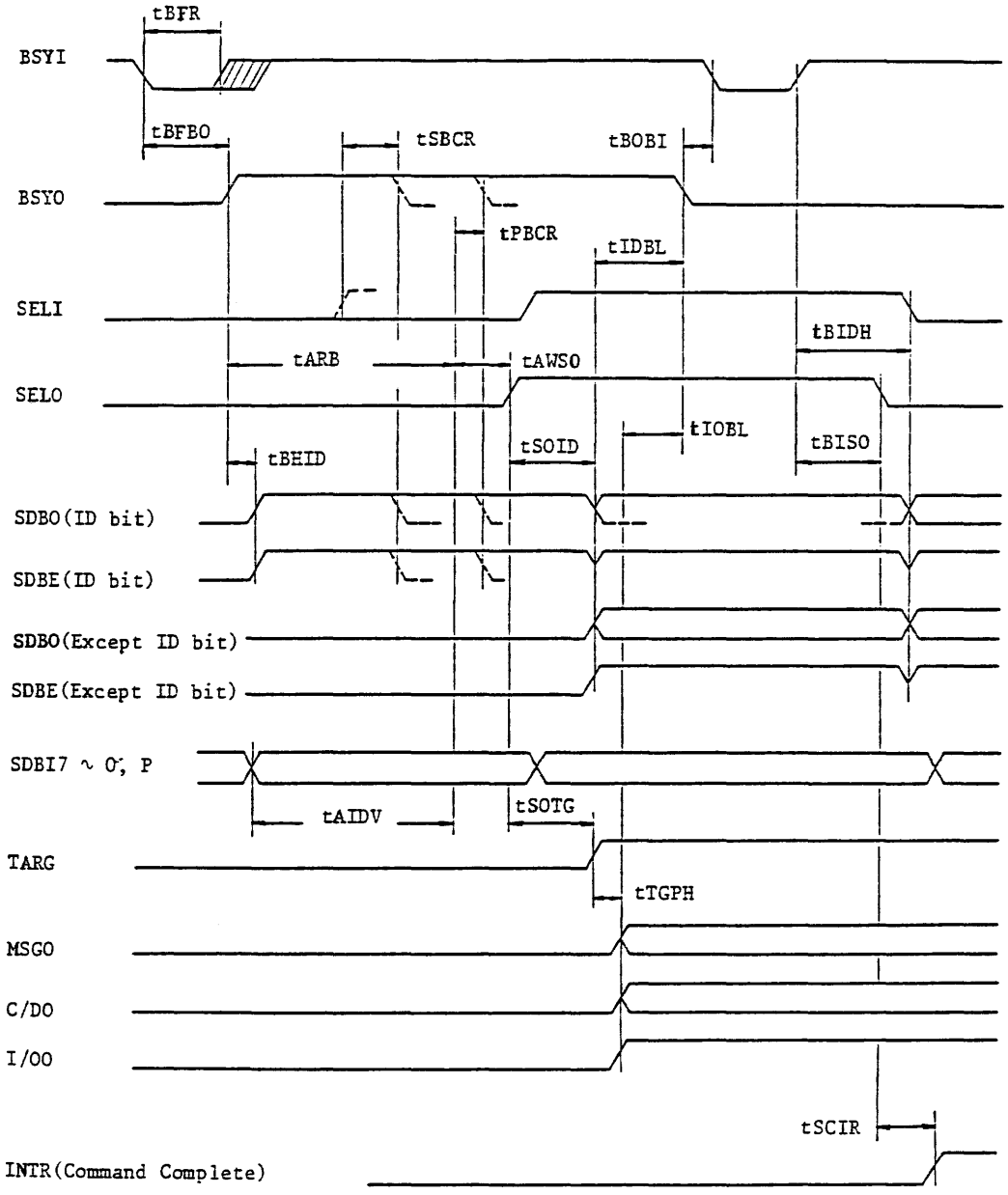
6.3.2 RESELECTION Phase

(1) TARGET

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{BFR}	Bus Free Time	$4t_{CLF}$ + 50			ns
t_{BFBO}	BYSI Low → BSYO High (Start of Arbitration)	(6+n) x t_{CLF} + 5		(7+n) x t_{CLF} + 65	ns
t_{BHID}	BSYO High → ID Bit High	5		55	ns
t_{ARB}	BSYO High → Prioritize	$32t_{CLF}$ - 40			ns
t_{AIDT}	Data Bus Valid (High Priority Bit) → Prioritize	70			ns
	Data Bus Valid (Low Priority Bit) → Prioritize	5			ns
t_{AWSO}	Bus Usage Permission Grant → SELO High	5		45	ns
t_{SOID}	SELO High → Data Bus (ID) Send	$11t_{CLF}$ - 30			ns
t_{SOTG}	SELO High → TARG High	$11t_{CLF}$ - 50			ns
t_{TGPH}	TARG High → Phase Signal Send			35	ns
t_{IOBL}	I/OO High → BSYO Low	$2t_{CLF}$ - 80			ns
t_{IDBL}	Data Bus (ID) Send → BSYO Low	$2t_{CLF}$ - 80			ns
t_{BOBI}	BSYO Low → BSYI Low	5		t_{CLF}	ns
t_{BISO}	BSYI High → SELO Low	$2t_{CLF}$ + 5			ns
t_{BIDH}	BSYI High → Data Bus (ID) Hold	$2t_{CLF}$ + 5			ns
t_{SCIR}	SELO Low → INTR High			75	ns
t_{SBCR}	SELI High → BSYO, ID Bit Low			$3t_{CLF}$ + 115	ns
t_{PBCR}	Prioritize → BSYO, ID Bit Low			125	ns

t_{CLF} : See 6.1.1

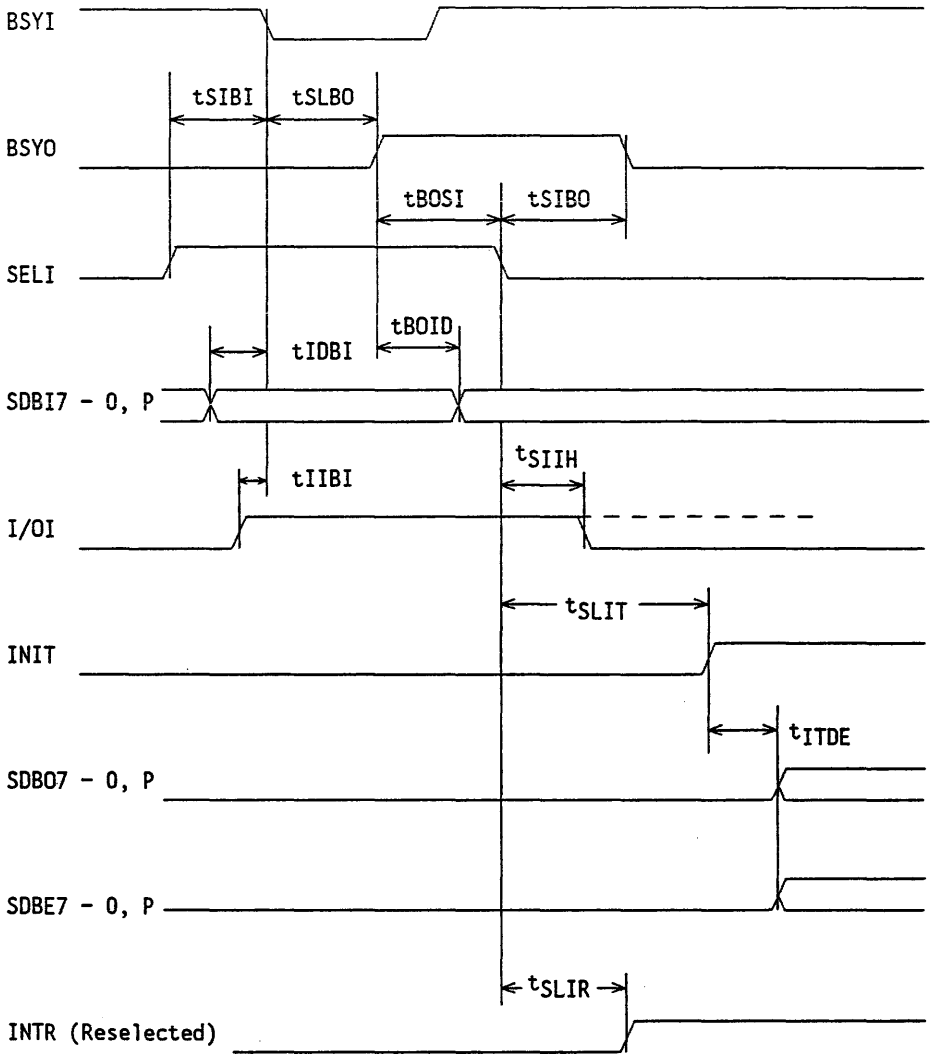
n : tCL register set value (See 4.3.2 (2) - Select command.)


tBFR
BSYI
tBFBO
tSBCR
tBOBI
BSYO
tPBCR
tIDBL
SELI
tBIDH
tARB
tAWSO
SELO
tIOBL
tSOID
tBISO
tBHID
SDBO(ID bit)
SDBE(ID bit)
SDBO(Except ID bit)
SDBE(Except ID bit)
SDBI7 ~ 0, P
tAIDV
tSOTG
TARG
tTGPH
MSGO
C/DO
I/OO
tSCIR
INTR(Command Complete)

(2) INITIATOR

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{SIBI}	SELI High → BSYI Low	5			ns
t_{IDBI}	Data Bus (ID) Valid → BSYI Low	5			ns
t_{IIBI}	I/OI Low → BSYI Low	5			ns
t_{SLBO}	BSYI Low → BSYO High (Response time)	$4t_{CLF} + 5$		$5t_{CLF} + 60$	ns
t_{BOID}	BSYO High → Data Bus (ID) Hold	15			ns
t_{BOSI}	BSYO High → SELI Low	5			ns
t_{SIBO}	SELI Low → BSYO Low	$2t_{CLF} + 5$		$3t_{CLF} + 15$	ns
t_{SIIH}	SELI Low → I/OI Hold	$3t_{CLF} + 20$			ns
t_{SLIR}	SELI Low → INTR High			$3t_{CLF} + 65$	ns
t_{SLIT}	SELI Low → INIT High	$3t_{CLF} + 5$		$4t_{CLF} + 65$	ns
t_{ITDE}	INIT High → Data Bus Enable (With I/OI at low level)	10			ns

t_{CLF} : See 6.1.1

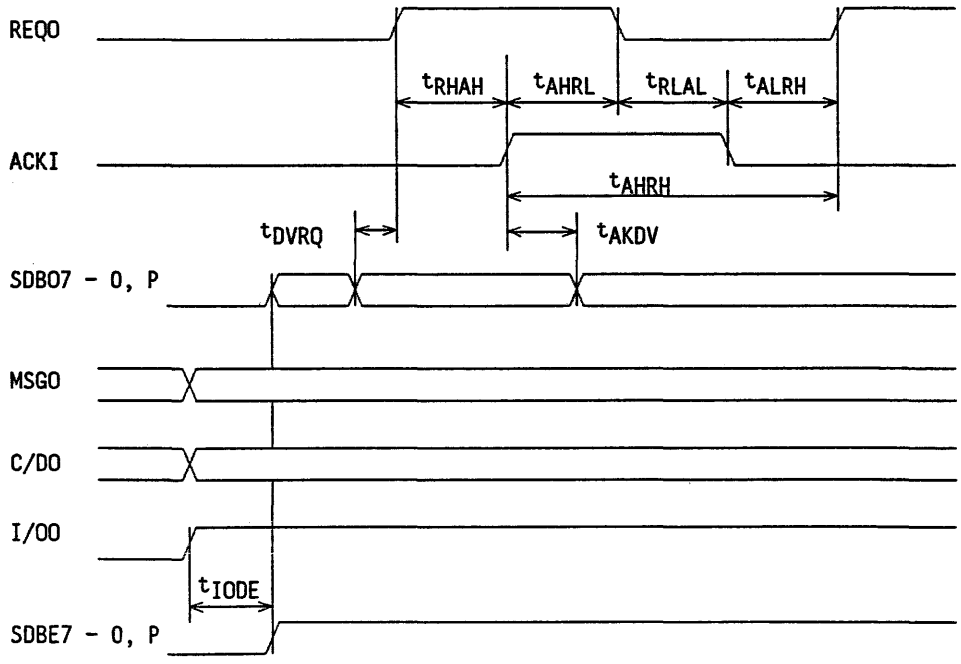

BSYI
tSIBI
tSLBO
BSYO
tBOSI
tSIBO
SELI
tBOID
tIDBI
SDBI7 - 0, P
tSIIH
tIIBI
I/OI
tSLIT
INIT
tITDE
SDBO7 - 0, P
SDBE7 - 0, P
tSLIR
INTR (Reselected)

6.3.3 Transfer Phase

(1) Asynchronous transfer output (TARGET)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{IODE}	I/OO High → Data Bus Enable	$3t_{CLF} + 5$			ns
t_{DVRQ}	Data Bus Valid → REQO High	$2t_{CLF} - 80$			ns
t_{AKDV}	ACKI High → Data Bus Hold	15			ns
t_{RHAH}	REQO High → ACKI High	20			ns
t_{AHRL}	ACKI High → REQO Low	10		55	ns
t_{RLAL}	REQO Low → ACKI Low	5			ns
t_{ALRH}	ACKL Low → REQO High	10			ns
t_{AHRH}	ACKI High → REQO High	$2t_{CLF} + 5$			ns

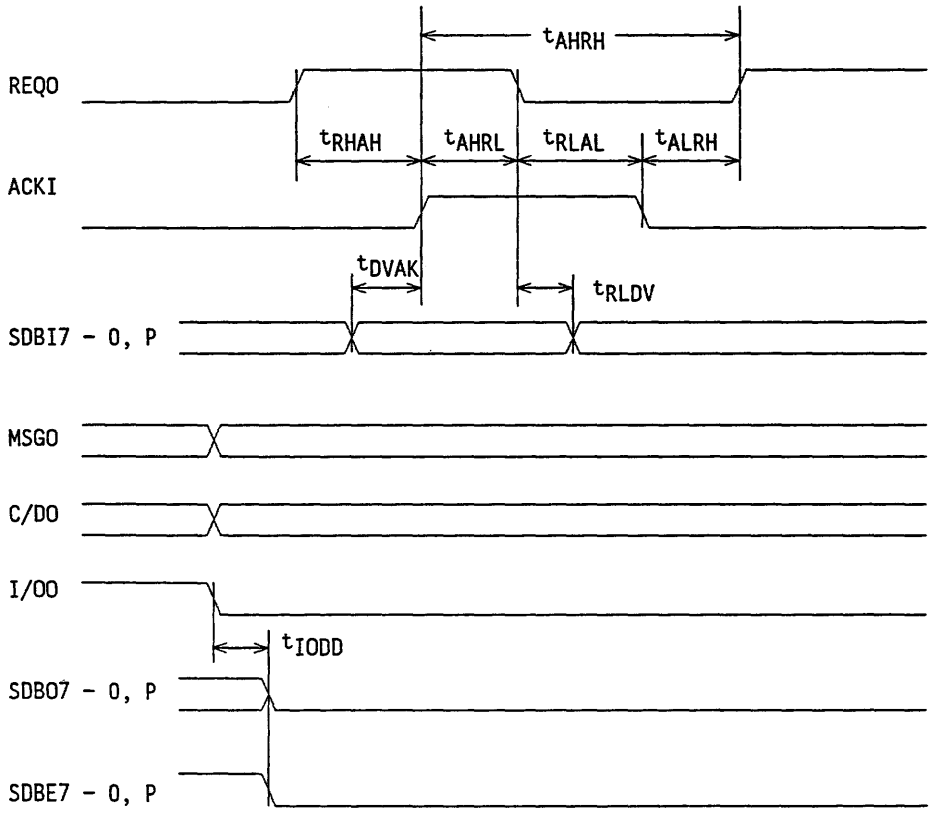
t_{CLF} : See 6.1.1



(2) Asynchronous transfer input (TARGET)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{IODD}	I/OO Low → Data Bus Disable			40	ns
t_{DVAK}	Data Bus Valid → ACKI High	10			ns
t_{RLDV}	REQO Low → Data Bus Hold	25			ns
t_{RHAH}	REQO High → ACKI High	20			ns
t_{AHRL}	ACKI High → REQO Low	10		55	ns
t_{RLAL}	REQO Low → ACKI Low	5			ns
t_{ALRH}	ACKI Low → REQO High	10			ns
t_{AHRH}	ACKI High → REQO High	$2t_{CLF} + 5$			ns

t_{CLF} : See 6.1.1.

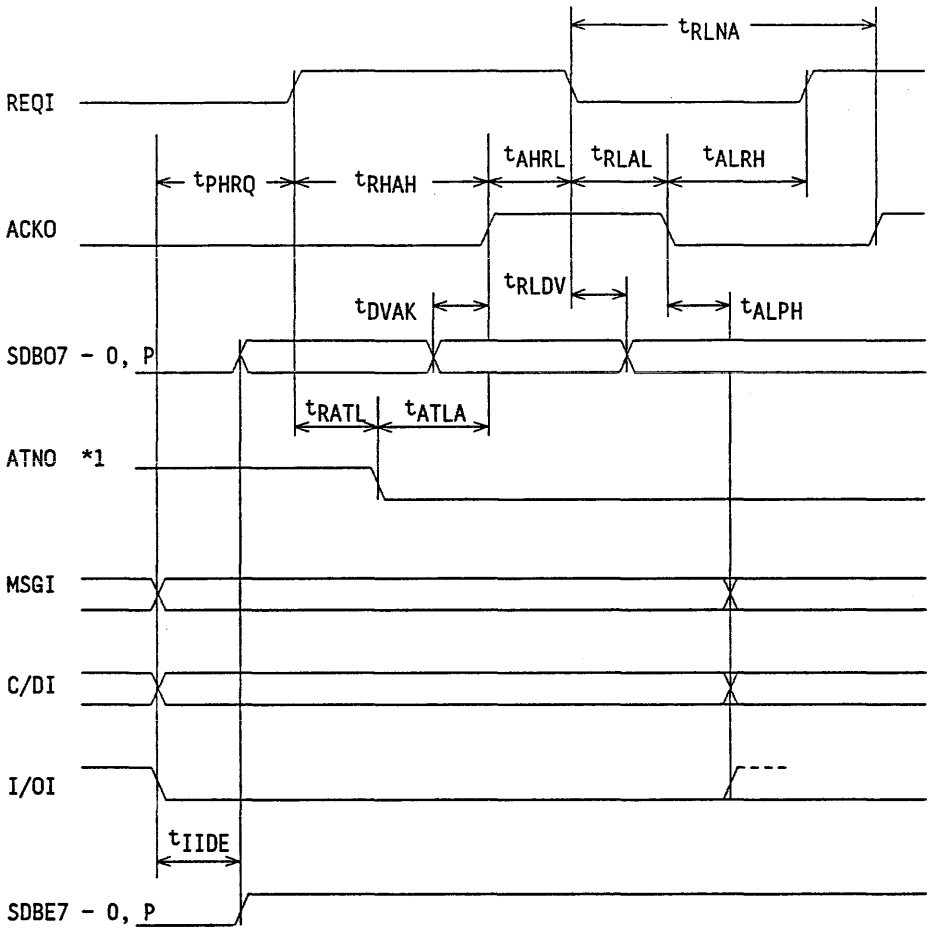


(3) Asynchronous transfer output (INITIATOR)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{IIDE}	I/OI Low → Data Bus Enable	20			ns
t_{PHRQ}	Phase Specify → REQI High	100			ns
t_{ALPH}	ACKO Low → Phase Change	10			ns
t_{RATL} *1	REQI High → ATNO Low	$2t_{CLF} + 5$			ns
t_{ATLA} *1	ATNO Low → ACKO High	$t_{CLF} - 20$			ns
t_{DVAK}	Data Bus Valid → ACKO High	$2t_{CLF} - 80$			ns
t_{RLDV}	REQI Low → Data Bus Hold	20			ns
t_{RHAH}	REQI High → ACKO High	15			ns
t_{AHRL}	ACKO High → REQI Low	5			ns
t_{RLAL}	REQI Low → ACKO Low	10			ns
t_{ALRH}	ACKO Low → REQI High	10			ns
t_{RLNA}	REQI Low → ACKO High	$2t_{CLF} + 5$			ns

t_{CLF} : See 6.1.1

*1 : With these timings, the ATNO signal is reset only when the last byte is sent at the MESSAGE OUT phase.

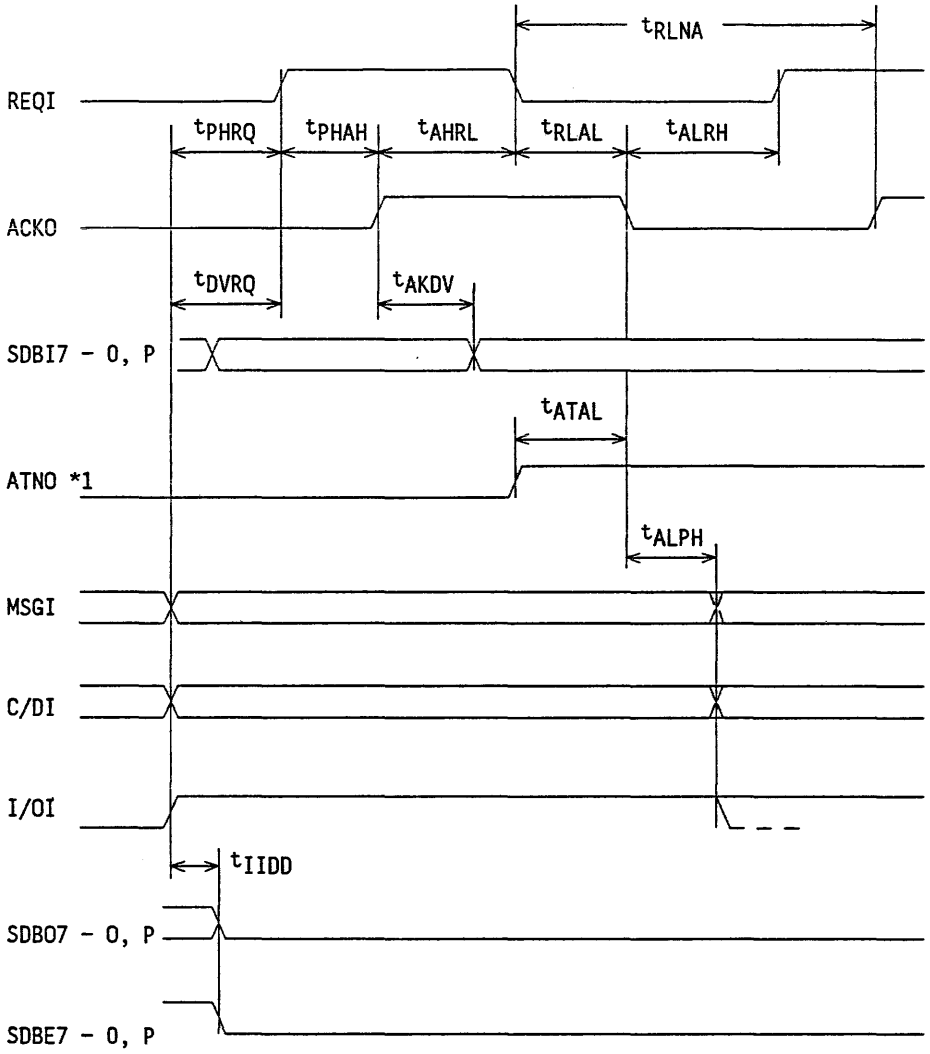

tRLNA
REQI
tPHRQ
tRHAH
tAHRL
tRLAL
tALRH
ACKO
tRLDV
tDVAK
tALPH
SDBO7 - 0, P
tRATL
tATLA
ATNO *1
MSGI
C/DI
I/OI
tIIDE
SDBE7 - 0, P

(4) Asynchronous transfer input (INITIATOR)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{IIDD}	I/OI High → Data Bus Disable			70	ns
t_{PHRQ}	Phase Specify → REQI High	100			ns
t_{ALPH}	ACKO Low → Phase Change	10			ns
t_{DVRQ}	Data Bus Valid → REQI High	10			ns
t_{AKDV}	ACKO High → Data Bus Hold	15			ns
t_{RHAH}	REQI High → ACKO High	15			ns
t_{AHRL}	ACKO High → REQI Low	5			ns
t_{RLAL}	REQI Low → ACKO Low	10			ns
t_{ALRH}	ACKO Low → REQI High	10			ns
t_{RLNA}	REQI Low → ACKO High	t_{CLF} + 5			ns
t_{ATAL} *1	ATNO High → ACKO Low	t_{CLF} - 20			ns

t_{CLF} : See 6.1.1

*1 With this timing, the ATNO signal is sent only when the parity checking is enabled and a parity error is detected in the input data.

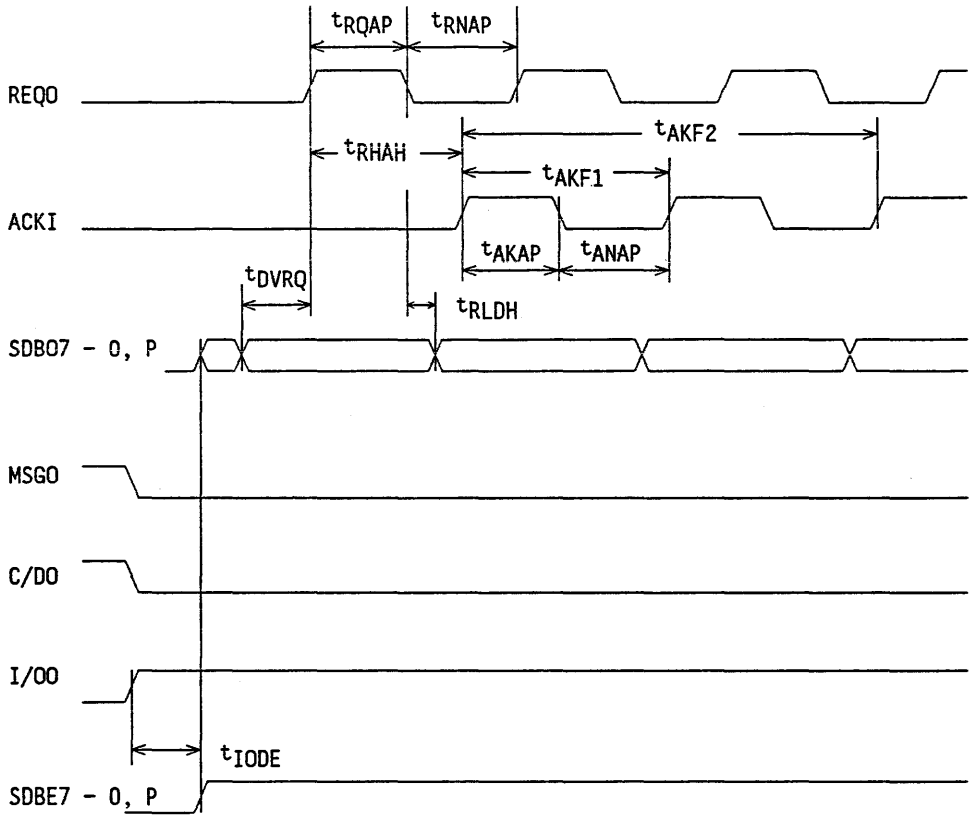

tRLNA
REQI
tPHRQ
tPHAH
tAHRL
tRLAL
tALRH
ACKO
tDVRQ
tAKDV
SDBI7 - 0, P
tATAL
ATNO *1
tALPH
MSGI
C/DI
I/OI
tIIDD
SDBO7 - 0, P
SDBE7 - 0, P

(5) Synchronous transfer output (TARGET)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{IODE}	I/OO High → Data Bus Enable	$3t_{CLF} + 5$			ns
t_{DVRQ}	Data Bus Valid → REQO High	$t_{CLF} + 5$ or $nt_{CLF} - 40$			ns
t_{RQAP}	REQO Assertion Period	$t_{CLF} - 10$			ns
t_{RNAP}	REQO Nonassertion Period	$nt_{CLF} - 10$			ns
t_{RLDH}	REQO Low → Data Bus Hold	5			ns
t_{RHAH}	REQO High → ACKI High	5			ns
t_{AKF1}	ACKI cycle time (1)	t_{CLF}			ns
t_{AKF2}	ACKI cycle time (2)	$3t_{CLF}$			ns
t_{AKAP}	ACKI Assertion Period	50			ns
t_{ANAP}	ACKI Nonassertion Period	50			ns

t_{CLF} : See 6.1.1

n : TMOD register set value (See Fig. 4.4.1)

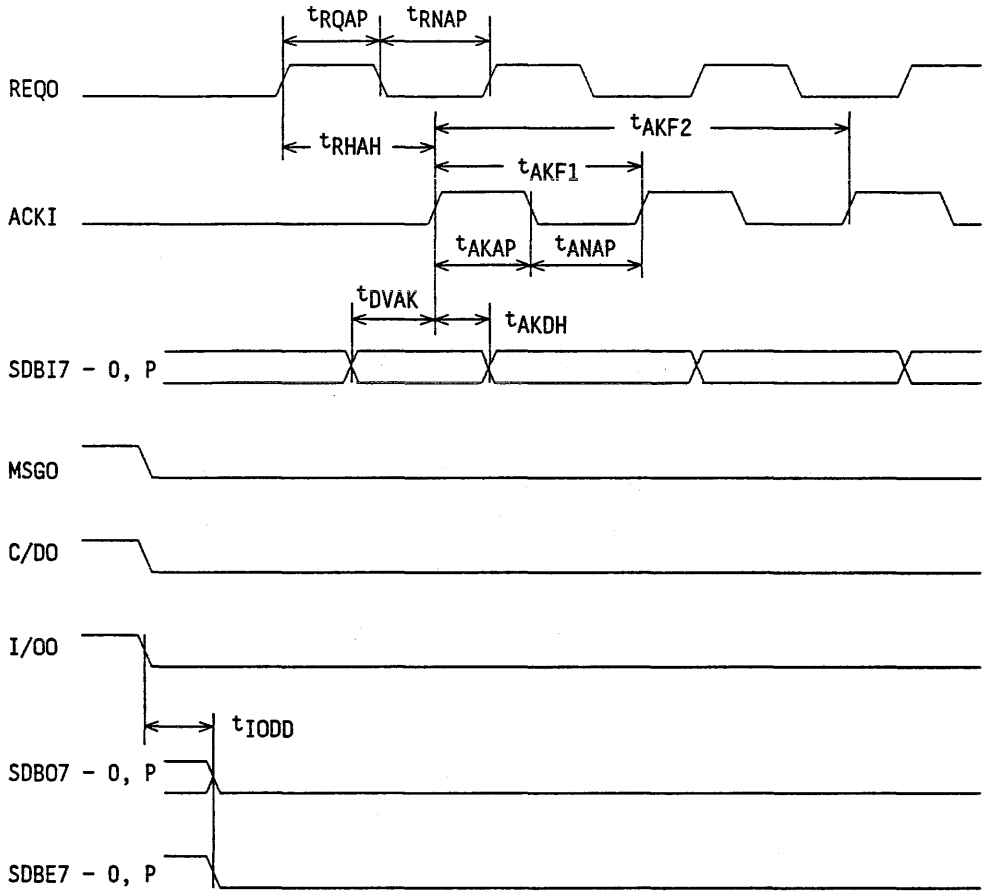

tRQAP
tRNAP
REQO
tAKF2
tRHAH
tAKF1
ACKI
tAKAP
tANAP
tDVRQ
tRLDH
SDBO7 - 0, P
MSGO
C/DO
I/OO
tIODE
SDBE7 - 0, P

(6) Synchronous transfer input (TARGET)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{IODD}	I/OO Low → Data Bus Disable			40	ns
t_{RQAP}	REQO Assertion Period	t_{CLF} - 10			ns
t_{RNAP}	REQO Nonassertion Period	nt_{CLF} -10			ns
t_{RHAH}	REQO High → ACKI High	5			ns
t_{AKAP}	ACKI Assertion Period	50			ns
t_{ANAP}	ACKI Nonassertion Period	50			ns
t_{AKF1}	ACKI Cycle time (1)	t_{CLF}			ns
t_{AKF2}	ACKI Cycle time (2)	$3t_{CLF}$			ns
t_{DVAK}	Data Bus Valid → ACKI High	10			ns
t_{AKDH}	ACKI High → Data Bus Hold	40			ns

t_{CLF} : See 6.1.1

n : TMOD register set value (See Fig. 4.4.1)

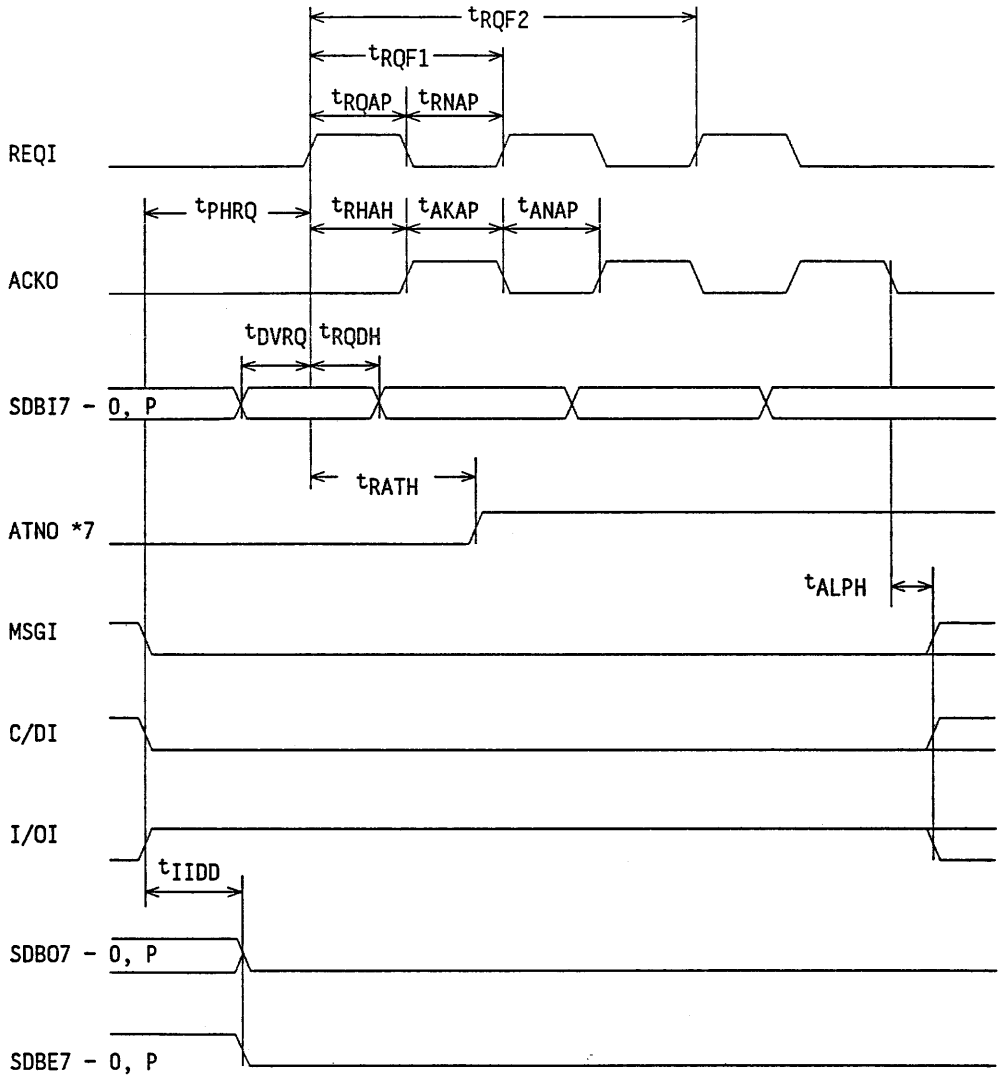

tRQAP
tRNAP
REQO
tRHAH
tAKF2
tAKF1
ACKI
tAKAP
tANAP
tDVAK
tAKDH
SDBI7 - 0, P
MSGO
C/DO
I/OO
tIODD
SDBO7 - 0, P
SDBE7 - 0, P

(7) Synchronous transfer Output (INITIATOR)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{IIDE}	I/OI Low → Data Bus Enable	20			ns
t_{PHRQ}	Phase Specify → REQI High	100			ns
t_{ALPH}	ACKO Low → Phase Change	10			ns
t_{RQAP}	REQI Assertion Period	50			ns
t_{RNAP}	REQI Nonassertion Period	50			ns
t_{RQF1}	REQI Cycle time (1)	t_{CLF}			ns
t_{RQF2}	REQI Cycle time (2)	$3t_{CLF}$			ns
t_{RHAH}	REQI High → ACKO High	$3t_{CLF} + 5$			ns
t_{AKAP}	ACKO Assertion Period	$t_{CLF} - 10$			ns
t_{ANAP}	ACKO Nonassertion Period	$nt_{CLF} - 10$			ns
t_{DTAK}	Data Bus Valid → ACKO High	$t_{CLF} + 5$ or $nt_{CLF} - 40$			ns
t_{ALDH}	ACKO Low → Data Bus Hold	5			ns

t_{CLF} : See 6.1.1

n : TMOD register set value (See Fig. 4.4.1)


tRQF2
tRQF1
tRQAP
tRNAP
REQI
tPHRQ
tRHAH
tAKAP
tANAP
ACKO
tDVRQ
tRQDH
SDBI7 - 0, P
tRATH
ATNO *7
tALPH
MSGI
C/DI
I/OI
tIIDD
SDBO7 - 0, P
SDBE7 - 0, P

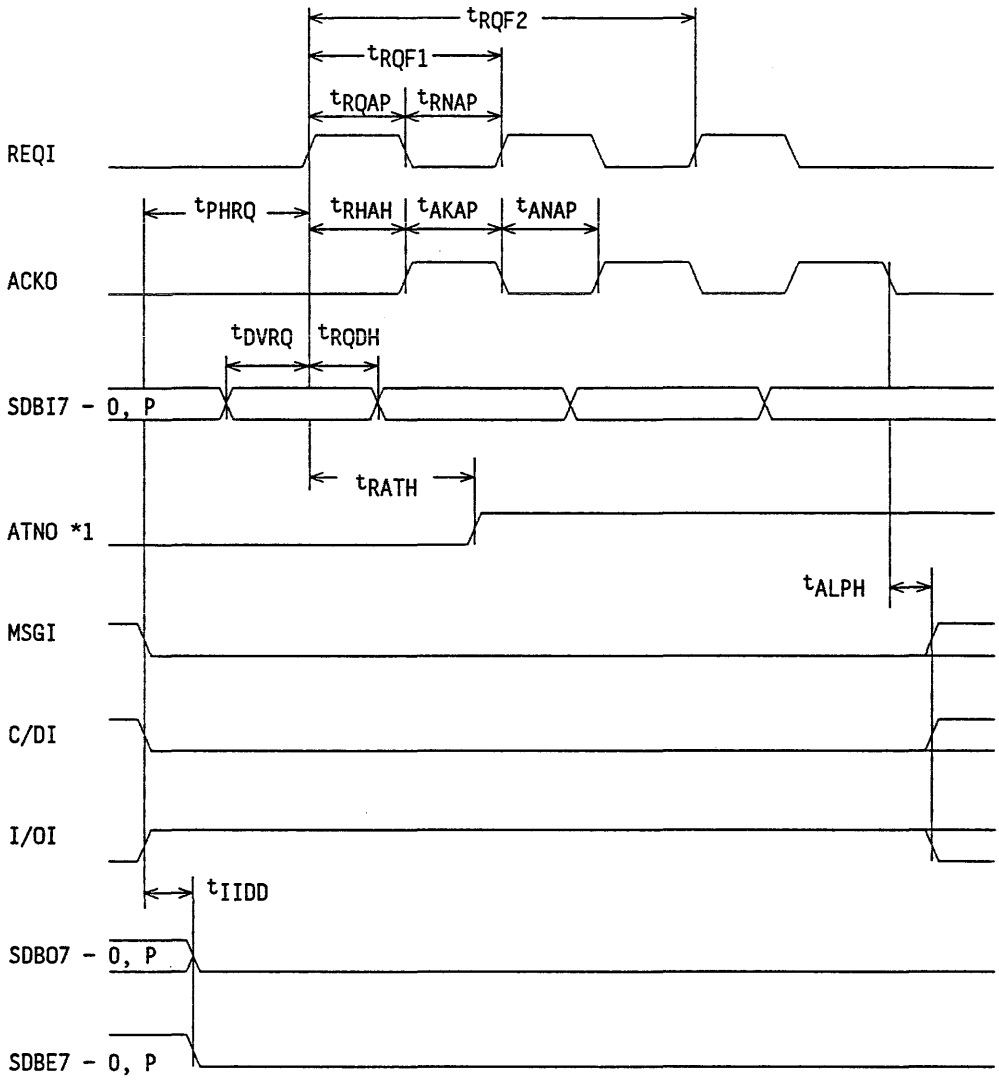
(8) Synchronous transfer input (INITIATOR)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{IDD}	I/OI High → Data Bus Disable			70	ns
t_{PHRQ}	Phase Specify → REQI High	100			ns
t_{ALPH}	ACKO Low → Phase Change	10			ns
t_{DVRQ}	Data Bus Valid → REQI High	10			ns
t_{RQDH}	REQI High → Data Bus Hold	40			ns
t_{RQAP}	REQI Assertion Period	50			ns
t_{RNAP}	REQI Nonassertion Period	50			ns
t_{RQF1}	REQI Cycle time (1)	t_{CLF}			ns
t_{RQF2}	REQI Cycle time (2)	$3t_{CLF}$			ns
t_{RHAH}	REQI High → ACKO High	$3t_{CLF} + 5$			ns
t_{AKAP}	ACKO Assertion Period	$t_{CLF} - 10$			ns
t_{ANAP}	ACKO Nonassertion Period	$nt_{CLF} - 10$			ns
t_{RATH} *1	REQI High → ATNO High	$3t_{CLF} + 5$			ns

t_{CLF} : See 6.1.1

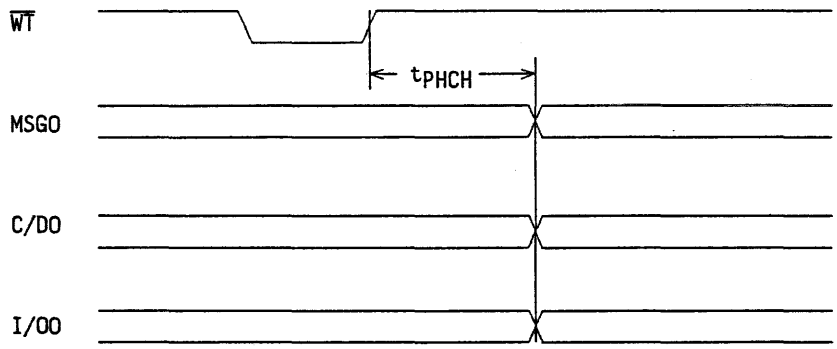
n : TMOD register set value (See Fig. 4.4.1)

*1 ANTO signal is sent only when the parity checking is enabled and a parity error is detected in the input data.


tRQF2
tRQF1
tRQAP
tRNAP
REQI
tPHRQ
tRHAH
tAKAP
tANAP
ACKO
tDVRQ
tRQDH
SDBI7 - 0, P
tRATH
ATNO *1
tALPH
MSGI
C/DI
I/OI
tIIDD
SDBO7 - 0, P
SDBE7 - 0, P

(9) Transfer phase change (TARGET)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{PHCH}	$\overline{WT}$ High → MSGO, C/DO, I/OO (PCTL register)	15		70	ns

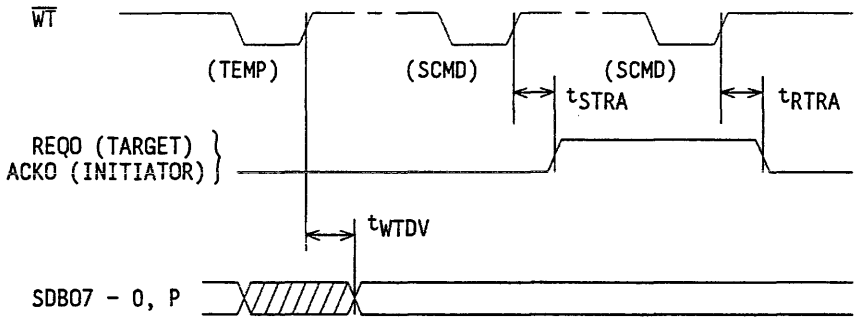


(10) Manual transfer

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{WTDV}	$\overline{WT}$ High → Data Bus Valid (TEMP register output)			60	ns
t_{STRA}	$\overline{WT}$ High → REQO, ACKO High (Set ACK/REQ command)	$2t_{CLF} + 5$		$3t_{CLF} + 60$	ns
t_{RTRA}	$\overline{WT}$ High → REQO, ACKO Low (Reset ACK/REQ command)	$2t_{CLF} + 5$		$3t_{CLF} + 60$	ns

t_{CLF} : See 6.1.1

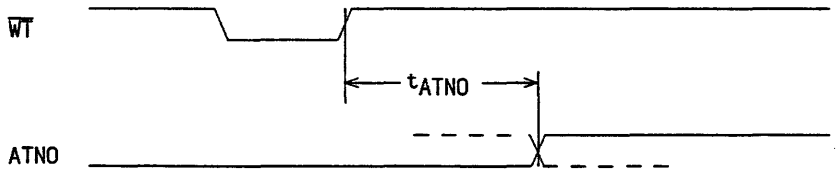
Note: Timing sequences not shown here conform to the asynchronous transfer timing sequence.



6.3.4 Attention Condition (INITIATOR)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{ATNO}	$\overline{WT}$ High → ATNO High/Low (Set ATN command and Reset ATN command)	$2t_{CLF} + 5$		$3t_{CLF} + 60$	ns

t_{CLF} : See 6.1.1

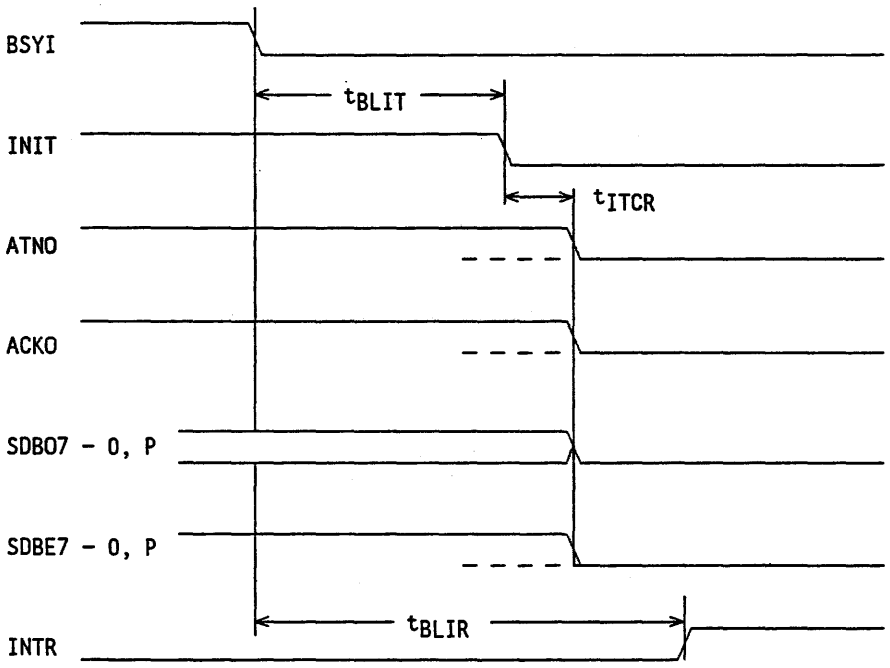


6.3.5 BUS FREE

(1) INITIATOR (Disconnected)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{BLIT}	BSYI Low → INIT Low			$5t_{CLF}$ + 70	ns
t_{ITCR}	INIT Low → Bus Clear			$5t_{CLF}$ + 65	ns
t_{BLIR}	BSYI Low → INTR High			$6t_{CLF}$ + 75	ns

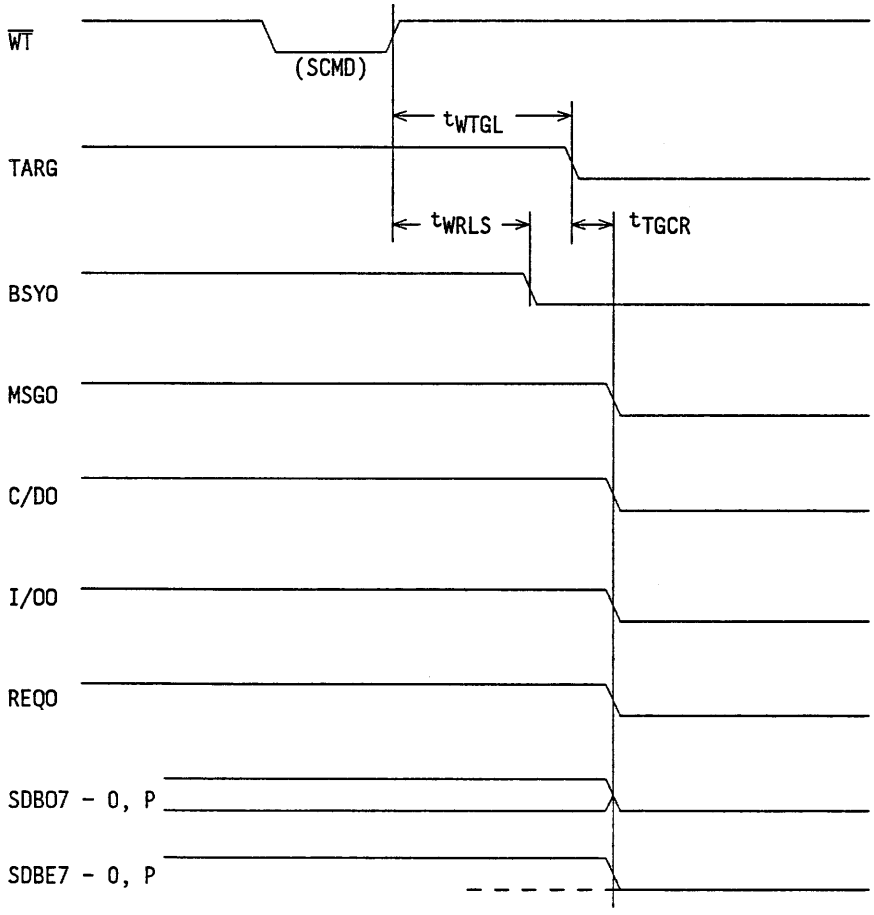
t_{CLF} : See 6.1.1



(2) TARGET (Bus Release command)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{WRLS}	$\overline{WT}$ High → BSYO Low (SCMD register)			$3t_{CLF}$ + 55	ns
t_{WTGL}	$\overline{WT}$ High → TARG Low (SCMD register)			$3t_{CLF}$ + 55	ns
t_{TGCR}	TARG Low → Bus Clear			95	ns

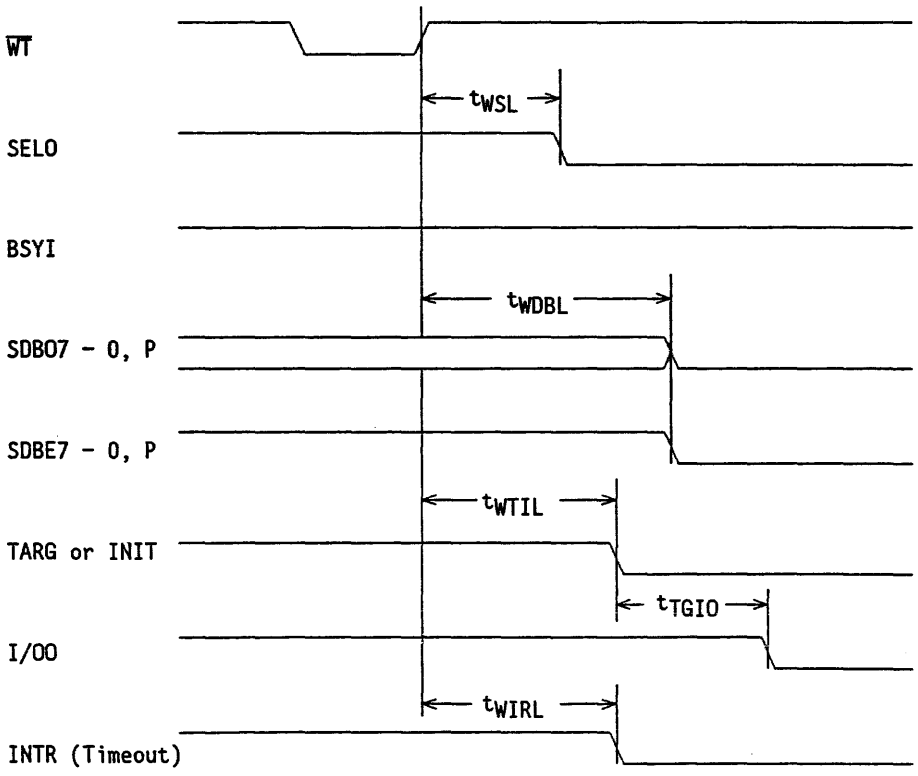
t_{CLF} : See 6.1.1



(3) SELECTION / RESELECTION phase stop (time-out)

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{WSL}	$\overline{WT}$ High → SELO Low (INTS register)			$3t_{CLF}$ + 55	ns
t_{WDBL}	$\overline{WT}$ High → Data Bus Disable (INTS register)			$3t_{CLF}$ + 100	ns
t_{WTIL}	$\overline{WT}$ High → TARG or INIT Low (INTS register)			$3t_{CLF}$ + 70	ns
t_{TGIO}	TARG Low → I/O0 Low			30	ns
t_{WIRL}	$\overline{WT}$ High → INTR Low (INTS register)			$3t_{CLF}$ + 65	ns

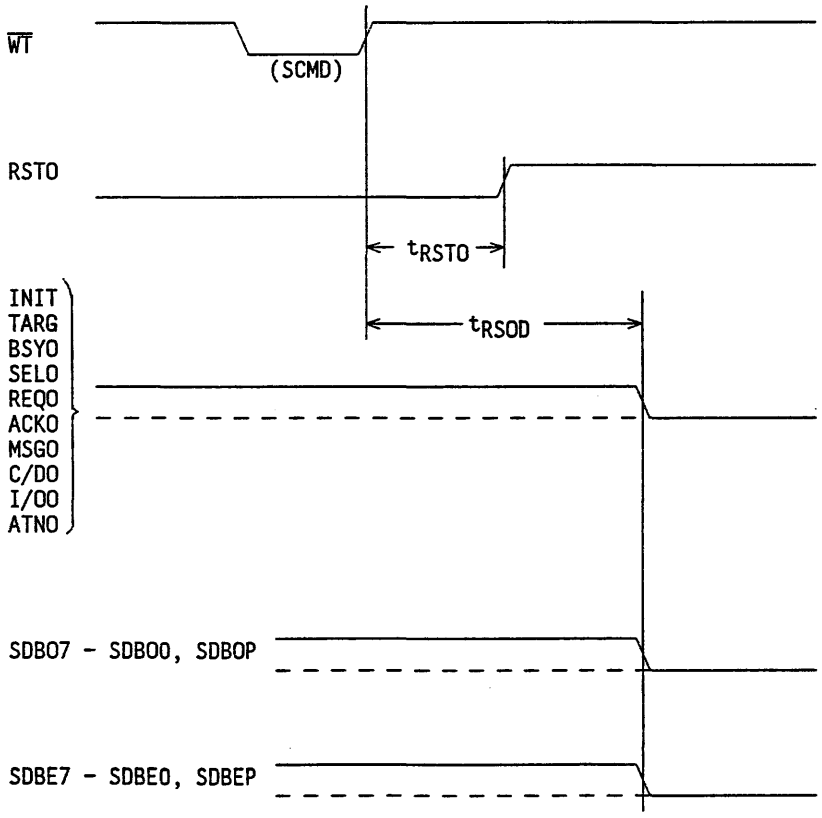
t_{CLF} : See 6.1.1.



6.3.6 Reset Condition

(1) RST signal sending

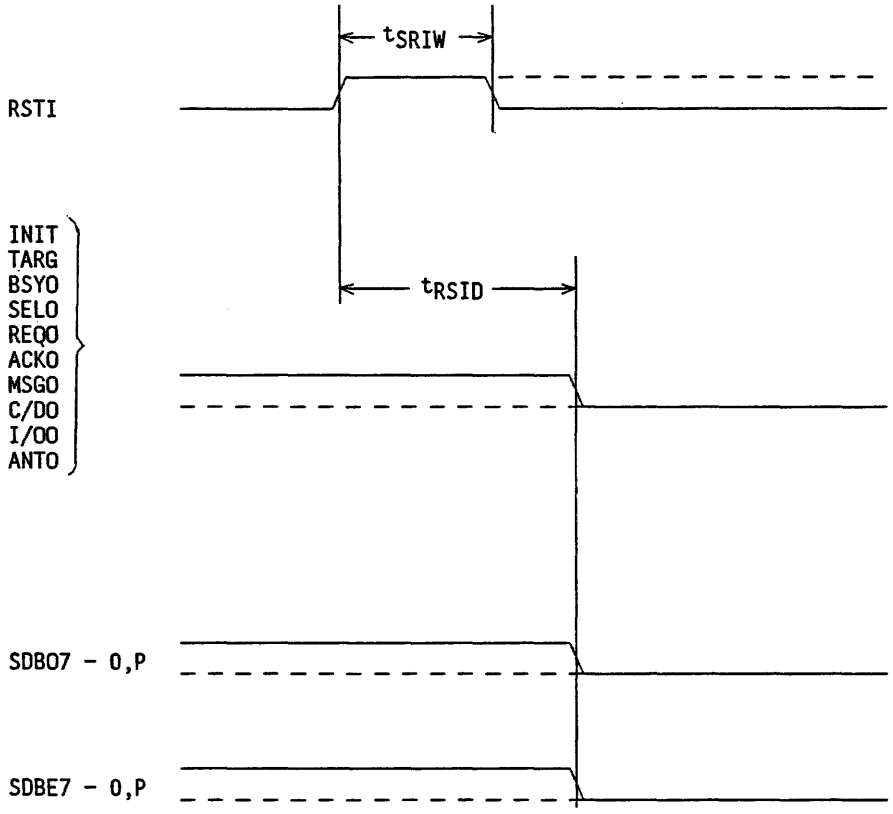
Symbol	Parameter	MIN	TYP	MAX	Unit
t_{RSTO}	$\overline{WT}$ High (bit 4 of SCMD register) → RSTO	5		35	ns
tRSOD	Reset Delay			115	ns



(2) RST signal receiving

Symbol	Parameter	MIN	TYP	MAX	Unit
t_{SRIN}	RSTI Pulse Width	$3t_{CLF}$			ns
t_{RSID}	Reset Delay			$4t_{CLF}$ + 115	ns

t_{CLF} : See 6.1.1



FUJITSU LIMITED
Communications and Electronics

6-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100, Japan
Phone: National (03) 216-3211 International (Int'l Prefix) 81-3-216-3211 Telex: J22833 Cable: "FUJITSULIMITED TOKYO"

For further information please contact:
FUJITSU LIMITED
Semiconductors Marketing: Furukawa Sogo Bldg., 6-1, Marunouchi 2-chome, Chiyoda-ku, Tokyo 100, Japan
Phone: National (03) 216-3211 International (Int'l Prefix) 81-3-216-3211 Telex: 222436 FTTOR J
FUJITSU MICROELECTRONICS, INC.:
3320 Scott Blvd., Santa Clara, CA 95054-3197, U.S.A.
Phone: 408-562-1000 Telex: 910-338-0190 FUJITSU SNTA
FUJITSU MIKROELEKTRONIK GmbH.:
Arabella Center 9. OG./A
Lyoner Straße 44-48 D-6000 Frankfurt 71, F.R. Germany
Phone: 069/66 320 Telex: 0411 963

Printed in USA