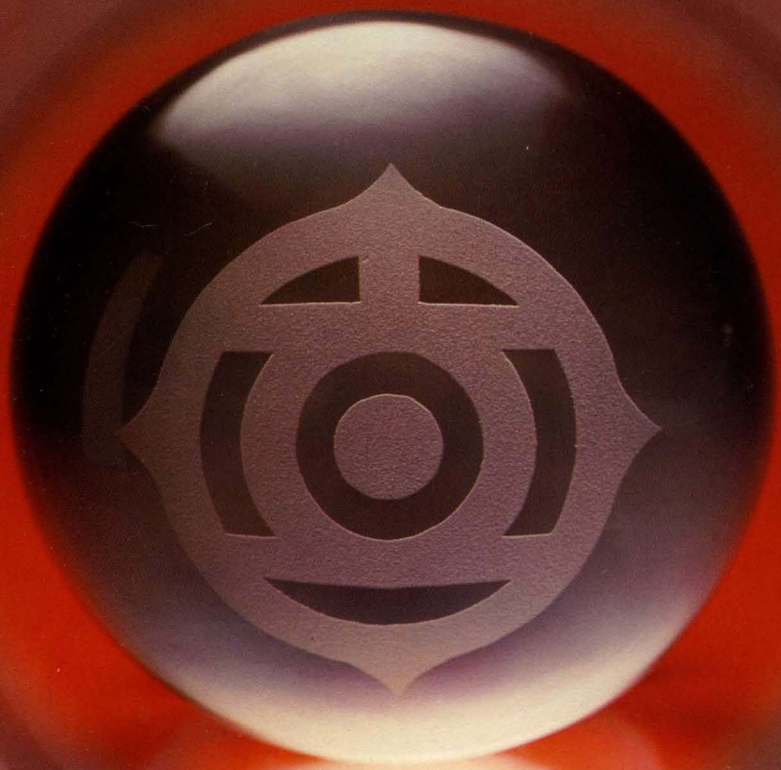
HLN1000

HITACHI Full Line Condensed Catalog



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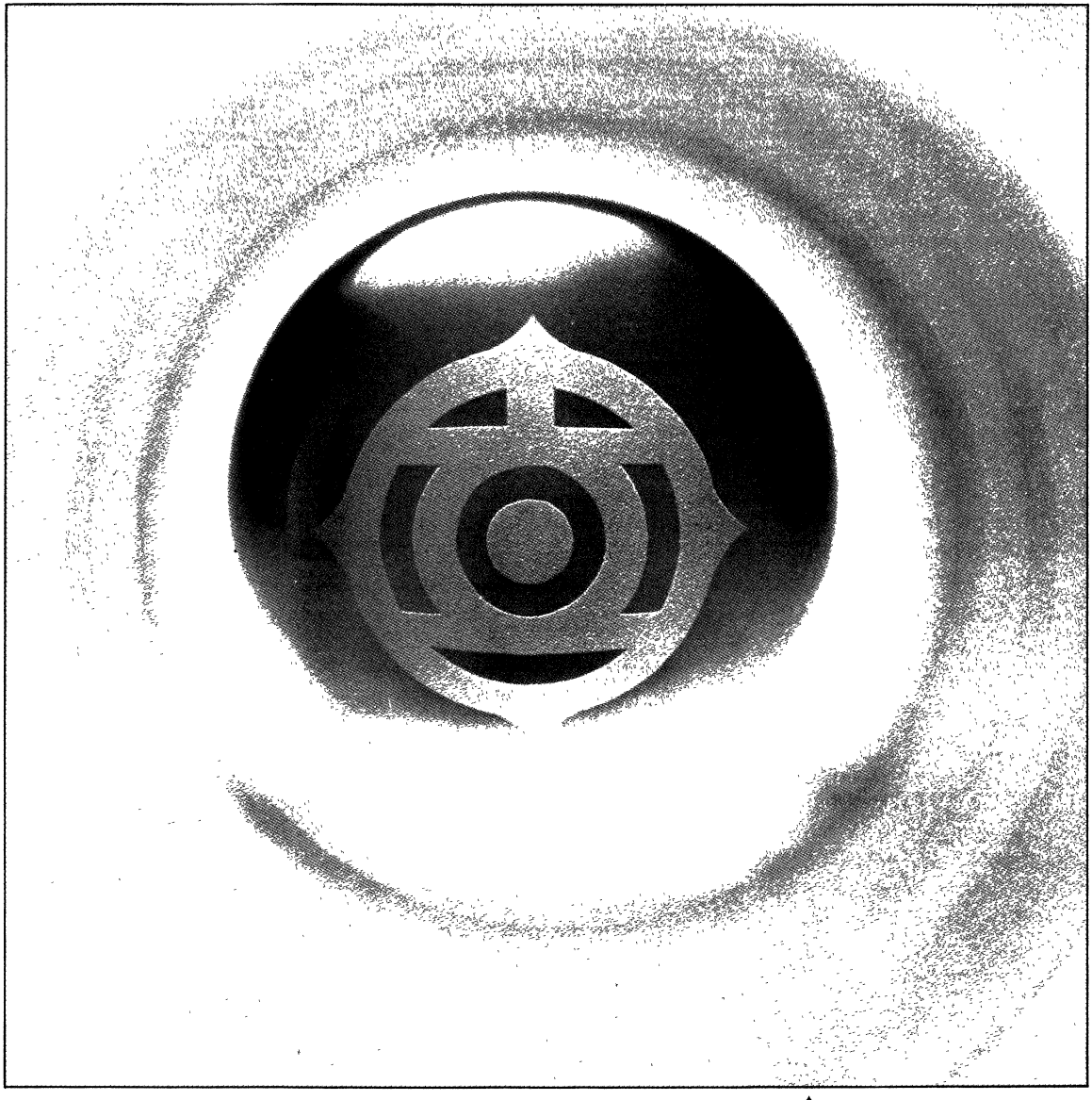
HITACHI FULL LINE CONDENSED CATALOG



HITACHI

FOR YOUR CONVENIENCE . . .

This catalog contains a complete listing of all major Hitachi product lines in a condensed, quick-reference-style format.

Refer to the table of contents for instant identification of product families.

Comprehensive index pages list specific products by catalog part numbers and their location page numbers.

The catalog is divided into sections containing all related products within each product line category.

For page layout data refer to the typical page illustrated below:

FREE LITERATURE
The HITACHI HLN- symbol shown on selected pages indicates the availability of comprehensive Data Sheets or other descriptive material for each product designated by a **H**ITACHI **L**ITERATURE **N**UMBER.

Example:
. . . HLN-101 indicates the availability of a comprehensive Product Data Sheet number HLN 101 . . . yours upon request.

Contact your nearest HITACHI sales office, representative or distributor for free literature.

PART NUMBER
Principal features of each item are listed in brief "one line" descriptions.

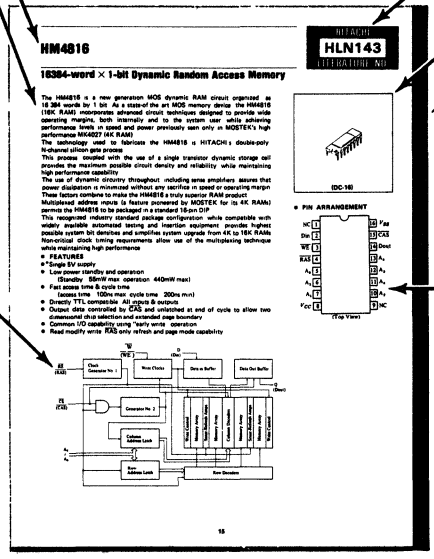
FEATURES
Principal features of each item are listed in brief "one line" identification.

BLOCK DIAGRAM
The equivalent schematic of the product is illustrated, where applicable.

PRODUCT ILLUSTRATION
An illustration of the basic product is shown on each page, identifying the product packaging, pin terminals, etc., for instant visual identification of product configuration.

COLOR-CODED PAGE EDGE
For easy indexing of sections.

PIN ARRANGEMENT
A plan view drawing illustrates the sequential pattern of termination pins.



HITACHI

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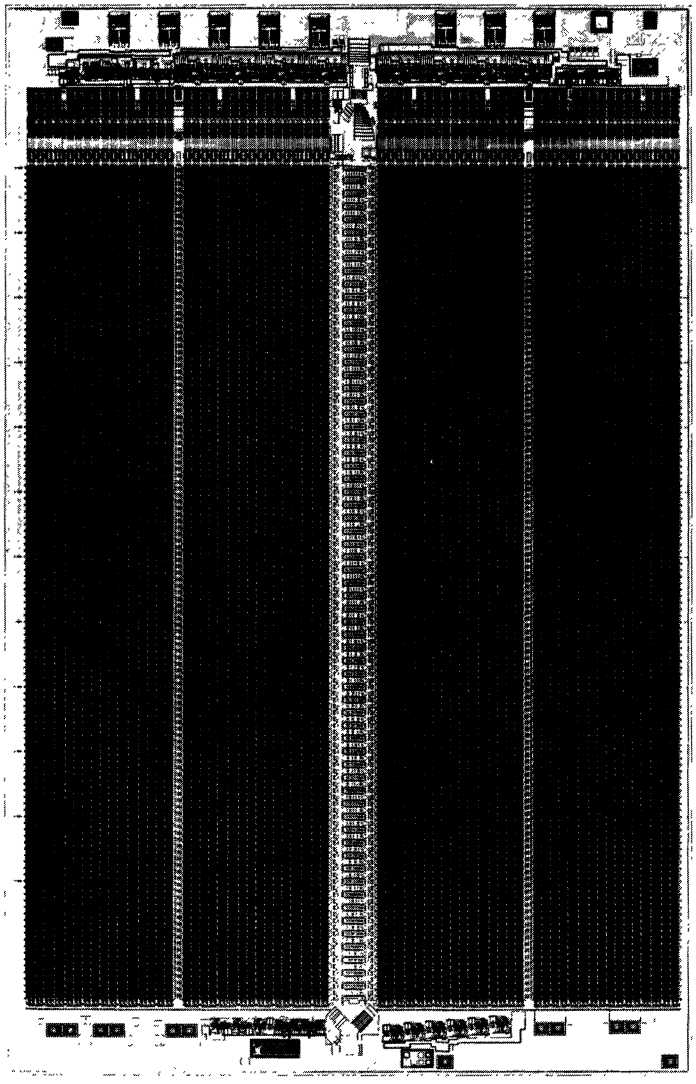
SECTION 1

HITACHI
HLN100
LITERATURE NO.

MOS MEMORIES



Die Photo of New 64K Static CMOS RAM, HM6264

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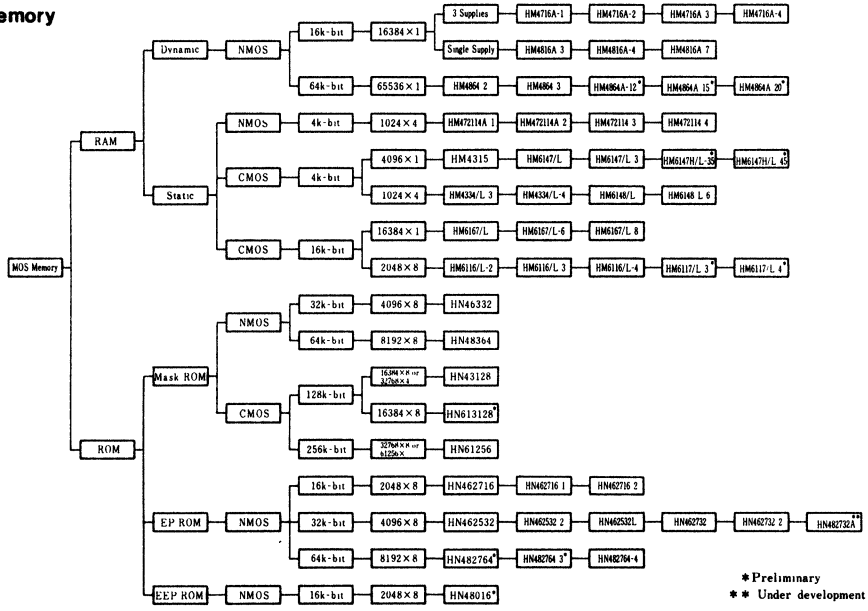
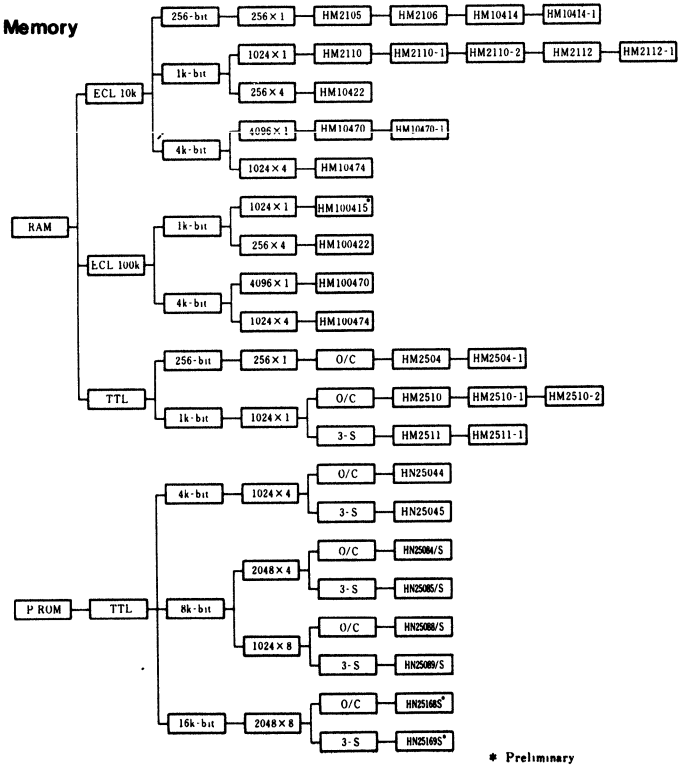
CURRENT LINE OF HITACHI IC MEMORIES

●MOS Memory



* Preliminary
** Under development

●Bipolar Memory



* Preliminary

■TYPICAL CHARACTERISTICS OF MOS MEMORY

●MOS RAM

Mode	Total Bit	Type No.	Process	Organization (word ×bit)	Access Time (ns) max	Cycle Time (ns) min	Supply Voltage (V)	Power Dissipation (W)	Package** Pin No.	C	G	P	FP	Replacement
Static	4k-bit	HM472114A-1	NMOS	1024×4	150	150	+5	0.2	18		●	●		
		HM472114A-2			200	200					●	●		2114L-2
		HM472114-3			300	300					●	●		2114L-3
		HM472114-4			450	450					●	●		2114L-4
		HM4334-3	CMOS	1024×4	300	460	+5	10μ/20m	18		●	●		HM-6514
		HM4334-4			450	640					●	●		
		HM4334-3L			300	460		10μ/20m				●		
		HM4334-4L			450	640						●		
		HM6148	CMOS	1024×4	70	70	+5	0.1m/0.2	18		●	●		2148
		HM6148-6			85	85					●	●		2148-6
		HM6148L			70	70		5μ/0.2				●		
		HM6148L-6			85	85						●		
		HM4315	CMOS	4096×1	450	640	+5	10μ/20m	18			●		HM-6504
		HM6147	CMOS	4096×1	70	70	+5	0.1m/75m	18		●	●		2147
		HM6147-3			55	55					●	●		2147-3
		HM6147L			70	70		5μ/5m				●		
		HM6147L-3			55	55						●		
		HM6147H-35*	CMOS	4096×1	35	35	+5	0.1m/0.15	18		●	●		2147H-1
		HM6147H-45*			45	45					●	●		2147H-2
		HM6147HL-35*			35	35		5μ/0.15				●		
		HM6147HL-45*			45	45						●		
	16k-bit	HM6116-2	CMOS	2048×8	120	120	+5	0.1m/0.18	24		●	●	●	
		HM6116-3			150	150					●	●	●	
		HM6116-4			200	200					●	●	●	
		HM6116L-2			120	120		20△μ/0.16			●	●	●	
		HM6116L-3			150	150					●	●	●	
		HM6116L-4			200	200					●	●	●	
		HM6117-3*	CMOS	2048×8	150	150	+5	0.1m/0.2	24			●	●	
		HM6117-4*			200	200						●	●	
		HM6117L-3*			150	150		10μ/0.2				●	●	
		HM6117L-4*			200	200						●	●	
		HM6167	CMOS	16384×1	70	70	+5	25m/0.15	20		●	●		2167
		HM6167-6			85	85					●	●		2167-6
		HM6167-8			100	100					●	●		2167-8
		HM6167L			70	70		5μ/0.15				●		
		HM6167L-6			85	85						●		
		HM6167L-8			100	100						●		
Dynamic	16k-bit	HM4716A-1	NMOS	16384×1	120	320	+12, +5, −5	0.35	16		●	●		
		HM4716A-2			150	320					●	●		MK4116-2
		HM4716A-3			200	375					●	●		MK4116-3
		HM4716A-4			250	410					●	●		MK4116-4
		HM4816A-3	NMOS	16384×1	100	235	+5	11m/0.15	16		●	●		2118-3
		HM4816A-3E			105	200					●	●		
		HM4816A-4			120	270					●	●		2118-4
		HM4816A-7			150	320					●	●		2118-7
	64k-bit	HM4864-2	NMOS	65536×1	150	270	+5	20m/0.33	16		●	●		
		HM4864-3			200	335					●	●		
		HM4864A-12*			120	230		20m/0.275			●	●		
		HM4864A-15*			150	260					●	●		
		HM4864A-20*			200	330					●	●		

* Preliminary △HM6116LP Series : 10μW

** The package codes of P, G, C, and FP are applied to the package materials as follows.
P : Plastic DIP, G : Cerdip, C : Side-brazed Ceramic DIP, FP : Small Sized Flat Package.

■TYPICAL CHARACTERISTICS OF MOS MEMORY

●MOS ROM

Program	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns) max	Supply Voltage (V)	Power Dissipation (W)	Package*** Pin No.	C	G	P	Replacement
Mask	32k-bit	HN46332	NMOS	4096×8	350	+5	0.25	24			●	
	64k-bit	HN48364		8192×8	350		0.225	24			●	
	128k-bit	HN43128	CMOS	16384×8 32768×4	6000		3m	28			●	
		HN613128*		16384×8	250		5μ/0.1	28			●	
	256k-bit	HN61256		32768×8 65536×4	3000		3m	28			●	
U. V. Erasable & Electrically	16k-bit	HN462716	NMOS	2048×8	450	+5	0.555	24	●	●		2716
		HN462716-1			350		0.555			●		2716-1
		HN462716-2			390					●		2716-2
	32k-bit	HN462532	NMOS	4096×8	450	+5	0.858	24	●	●		TMS2532
		HN462532-2			390					●		
		HN462532L			450		0.543			●		TMS25L32
		HN462732	NMOS	4096×8	450	+5	0.788	24	●	●		2732
		HN462732-2			390					●		
		HN482732A-20**	NMOS	4096×8	200	+5	—	24		●		2732A-2
		HN482732A-25**			250					●		2732A
		HN482732A-30**			300					●		2732A-3
	64k-bit	HN482764*	NMOS	8192×8	250	+5	0.555	28	●	●		2764
		HN482764-3*			300				●	●		2764-3
		HN482764-4			450				●	●		
Electrically Erasable	16k-bit	HN48016*	NMOS	2048×8	350	+5	0.3	24			●	

* Preliminary

** Under development

*** The package codes of P, G, and C are applied to the package materials as follows.
P : Plastic DIP, G : Cerdip, C : Side-brazed Ceramic DIP

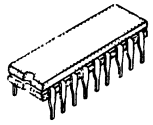
HM472114A-1, HM472114A-2, HM472114AP-1, HM472114AP-2

HITACHI
HLN101
LITERATURE NO.

1024-word × 4-bit Static Random Access Memory

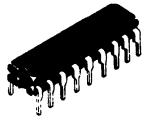
- Fast Access Time . . . . . HM472114A-1 150ns (max.)
  HM472114A-2 200ns (max.)
- Low Operating Power . . . . . 200mW (typ.)
- Single +5V Supply
- Completely Static Memory . . . . . No Clock or Refresh Required
- Fully TTL Compatible . . . . . All Inputs and Output
- Common Data Input and Output Using Three-state Outputs
- N-channel Si Gate MOS Technology
- Pin Equivalent with Intel 2114L Series

HM472114A-1, HM472114A-2



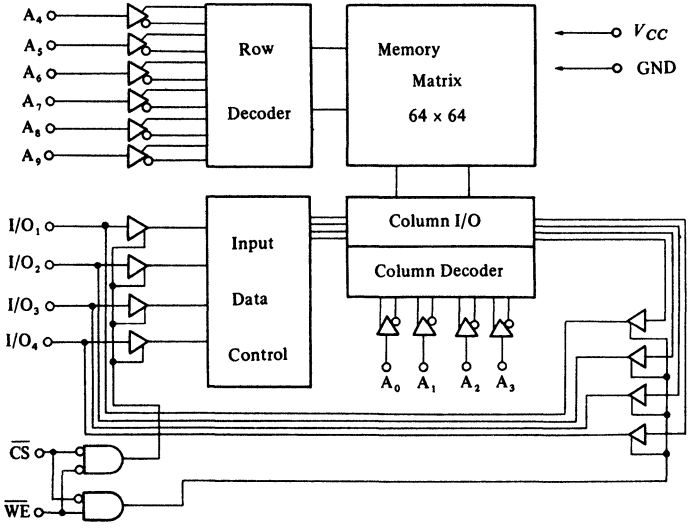
(DG-18)

HM472114AP-1, HM472114AP-2

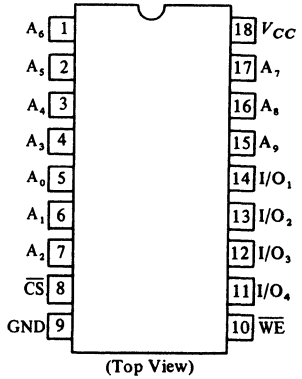


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

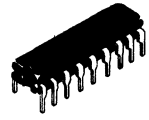
HM472114AP-3, HM472114AP-4

HITACHI
HLN103
LITERATURE NO.

1024-word × 4-bit Static Random Access Memory

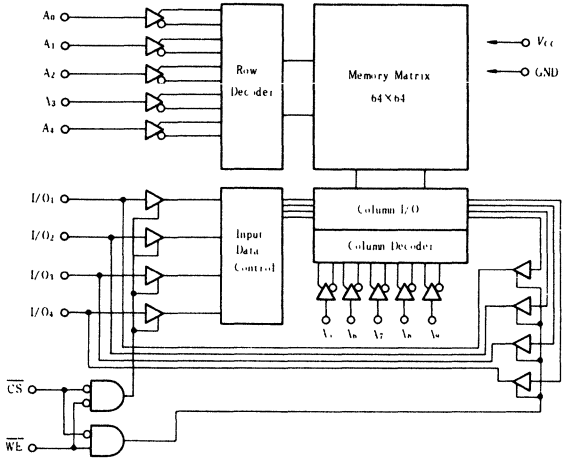
- Fast Access Time ..... HM47211P-3 300 ns (max.)
  HM47211P-4 450 ns (max.)
- Low Operating Power ..... 200mW (typ)
- Single +5V Supply Voltage
- Completely Static Memory ..... No Clock or Refresh Required
- Directly TTL Compatible ..... All Inputs and Outputs
- Common Data Inputs and Output
- Three-state Outputs
- DC Standby Mode ..... Reduces V_{CC}
- N-channel Si Gate MOS Technology
- Interchangeable with Intel 2114L Series

HM472114P-3, HM472114P-4

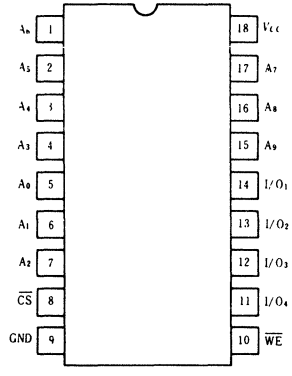


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

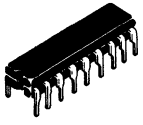
HM4334P-3, HM4334P-4

HITACHI
HLN115
LITERATURE NO.

1024-word × 4-bit Static CMOS RAM

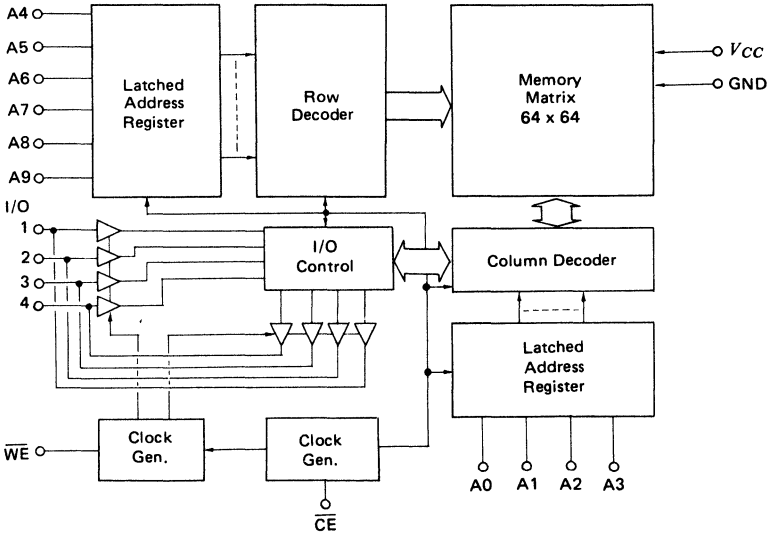
■ FEATURES

- Single 5V Supply
- Low Power Standby and Low Power Operation; Standby: 10 μW (typ.)
  Operation: 20 mW (typ.)
- Fast Access Time; HM4334P-3: 300 ns (max.)
  HM4334P-4: 450 ns (max.)
- Directly TTL Compatible: All inputs and outputs
- Common Data Input and Output using Three-state Outputs
- On Chip Address Register

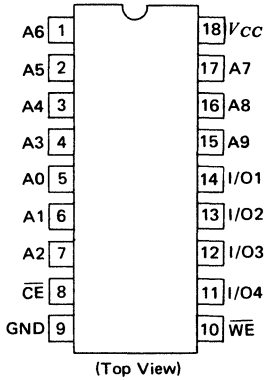


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



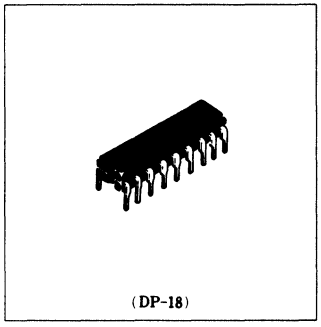
(Top View)

HM4334LP-3, HM 4334LP-4

1024-word × 4-bit Static CMOS RAM

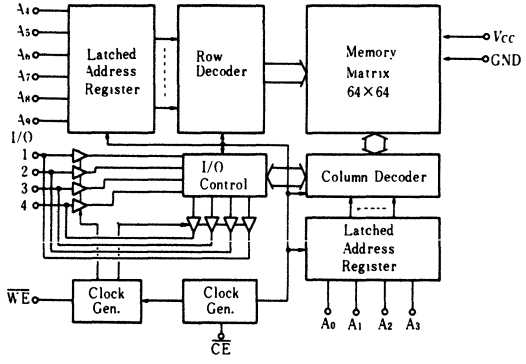
■FEATURES

- Single 5V Supply
- Low Power Standby and Low Power Operation; Standby: 10μW (typ.) Operation: 20mW (typ.)
- Fast Access Time; HM4334P-3L: 300 ns (max.) (5V±5%) HM4334P-4L: 450 ns (max.) (5V±10%)
- Directly TTL Compatible: All inputs and outputs
- Common Data Input and Output using Three-state Outputs
- On Chip Address Register

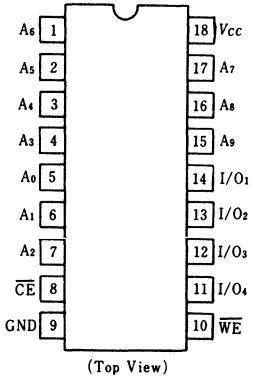


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

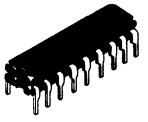
HM6148P, HM6148P-6

HITACHI
HLN110
LITERATURE NO.

1024-word × 4-bit High Speed Static CMOS RAM

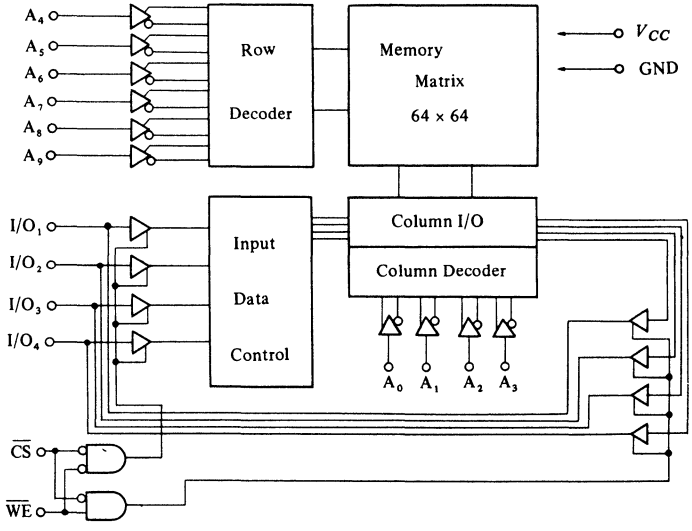
■ FEATURES

- Single 5 V Supply
- Fast Access Time . . . . . HM6148P 70 ns (max)
  HM6148P-6 85 ns (max)
- Low Power Standby and Low Power Operation; Standby : 100 μW (typ)
  Operation : 200 mW (typ)
- Completely Static RAM; No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Three State Output
- Common Data Input and Output
- Pin-Out Compatible with Intel 2148

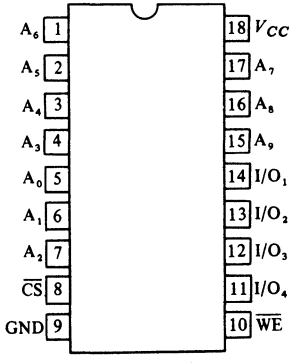


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

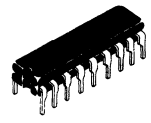
HM6148LP, HM6148LP-6

HITACHI
HLN108
LITERATURE NO.

1024-word × 4-bit High Speed Static CMOS RAM

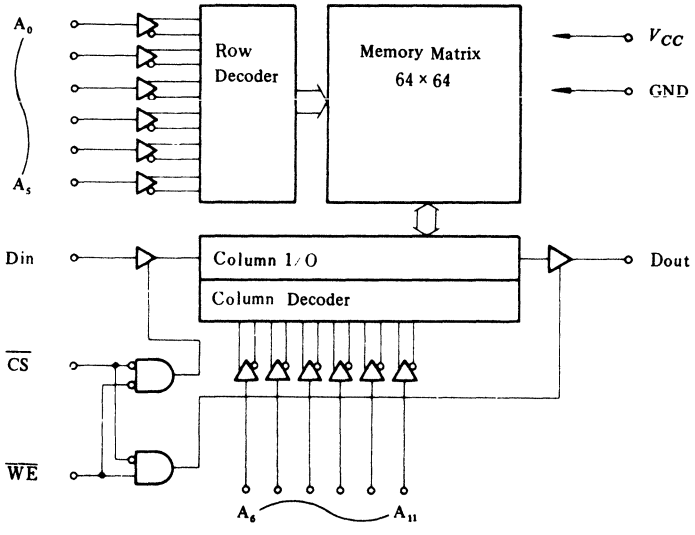
■ FEATURES

- Single 5V Supply
- Fast Access Time . . . . . HM6148LP 70 ns (max)
  HM6148LP-6 85 ns (max)
- Low Power Standby and Low Power Operation; Standby : 10 μW (typ)
  Operation : 200mW (typ)
- Completely Static RAM; No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Three State Output
- Common Data Input and Output
- Capability of Battery Back Up Operation
- Pin-Out Compatible with Intel 2148

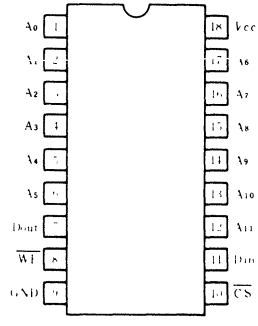


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

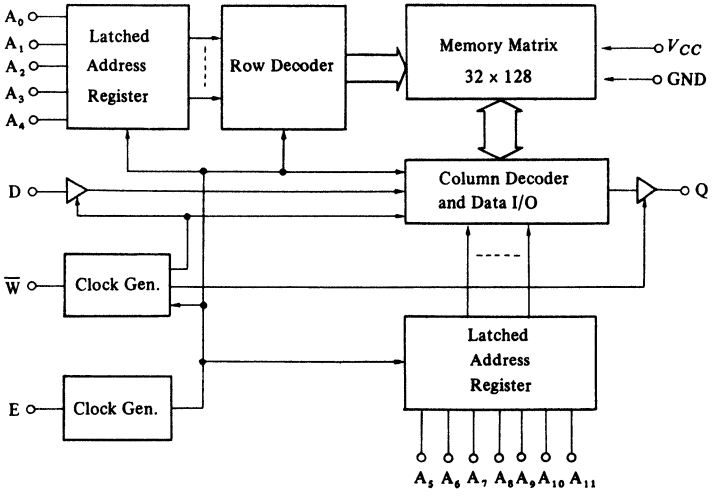
HM4315P

HITACHI
HLN114
LITERATURE NO.

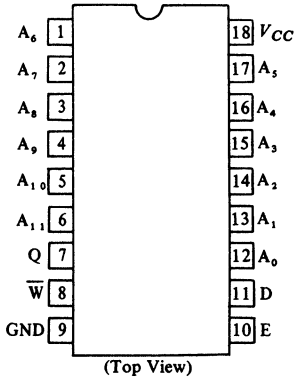
4096-word × 1-bit Static Random Access Memory

- Low Power Standby . . . . . 10μW typ.
- Low Power Operation . . . . . 20mW typ.
- Data Retention 2.0V
- Fast Access Time . . . . . 450ns max.
- TTL/CMOS Compatible Input/Output
- On Chip Address Register
- Si Gate CMOS Technology

(DP-18)



■ PIN ARRANGEMENT



(Top View)

HM6147, HM6147-3, HM6147P, HM6147P-3

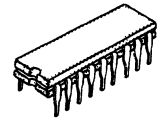
HITACHI
HLN104
LITERATURE NO.

4096-word × 1-bit High Speed Static CMOS RAM

■ FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby: 100 μW typ., Operation: 75mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

HM6147, HM6147-3

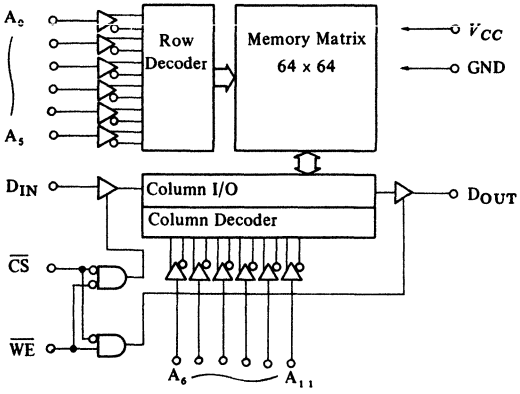


(DG-18)

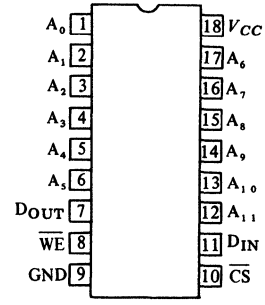
HM6147P, HM6147P-3

(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

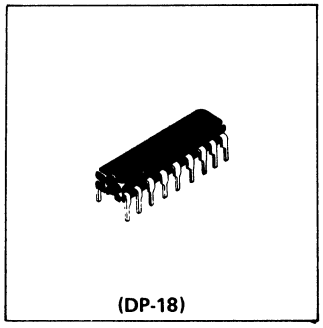
HM6147LP, HM6147LP-3

HITACHI
HLN105
LITERATURE NO.

4096-word × 1-bit High Speed Static CMOS RAM

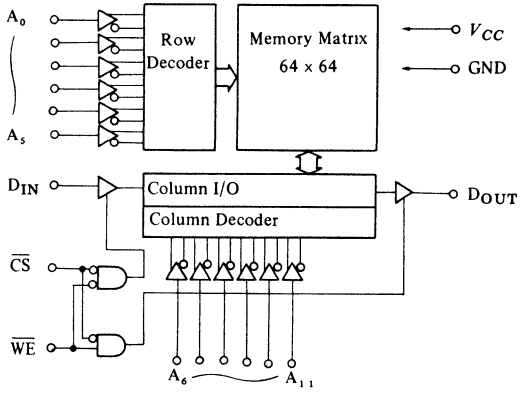
■ FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 55ns/70ns Max.
- Low Power Standby and Low Power Operation, Standby: 5μW typ., Operation: 75mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power–On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Capability of Battery Back up Operation
- Pin-out Compatible with Intel 2147 NMOS STATIC RAM

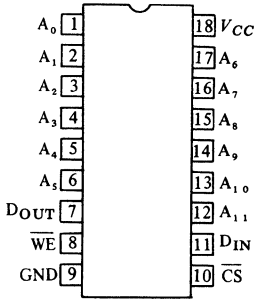


(DP-18)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HM6147H-35, HM6147H-45, HM6147HP-35, HM6147HP-45

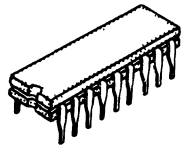
—Preliminary—

4096-word × 1-bit High Speed Static CMOS RAM

■FEATURES

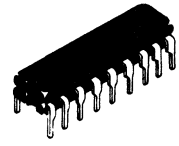
- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 35ns/45ns Max.
- Low Power Standby and Low Power Operation, Standby: 100μW typ., Operation: 150mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM

HM6147H-35, HM6147H-45



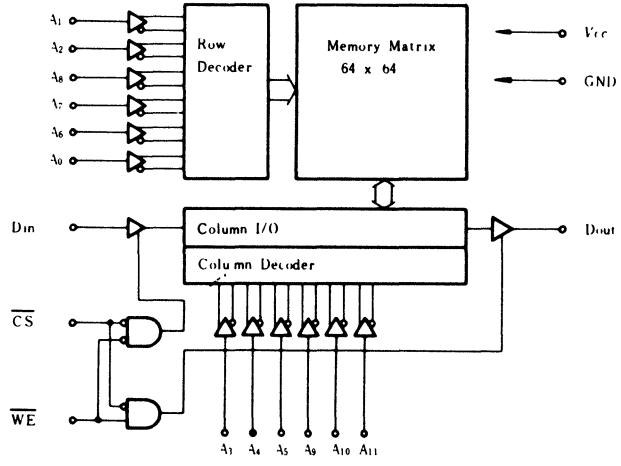
(DG-18)

HM6147HP-35, HM6147HP-45

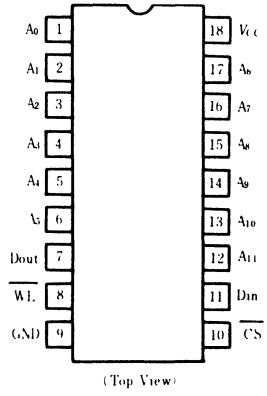


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



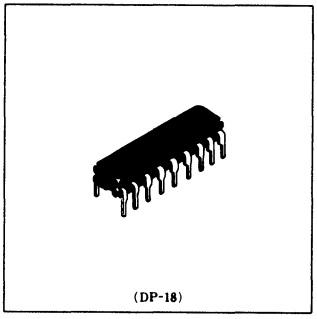
(Top View)

HM6147HLP-35, HM6147HLP-45 —Preliminary—

4096-word × 1-bit High Speed Static RAM

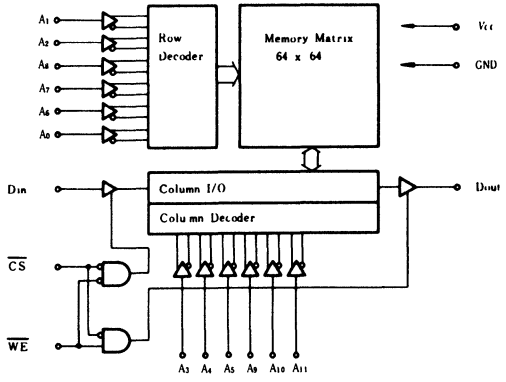
■FEATURES

- Single 5V Supply and High Density 18 Pin Package
- High Speed: Fast Access Time 35ns/45ns Max.
- Low Power Standby and Low Power Operation, Standby; 5μW typ., Operation: 150mW typ.
- Completely Static Memory — No Clock nor Timing Strobe Required
- No Peak Power–On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible — All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM
- Capable of Battery Back up Operation

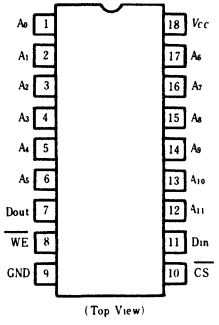


(DP-18)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

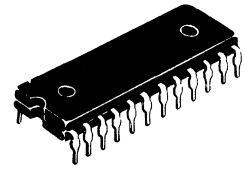
HM6116P-2, HM6116P-3, HM6116P-4

HITACHI
HLN111
LITERATURE NO.

2048-word × 8-bit High Speed Static CMOS RAM

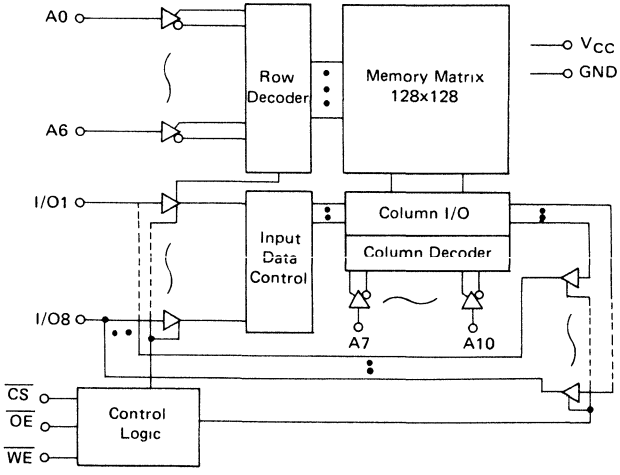
■ FEATURES

- Single 5V Supply and High Density 24 pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 100μW (typ.)
  Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

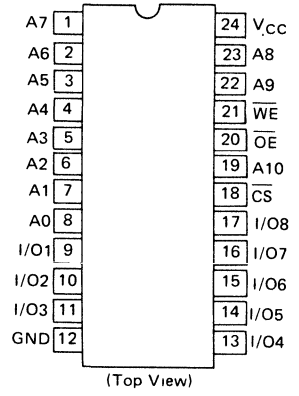


(DP-24)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HM6116FP-2, HM6116FP-3, HM6116FP-4

—Preliminary—

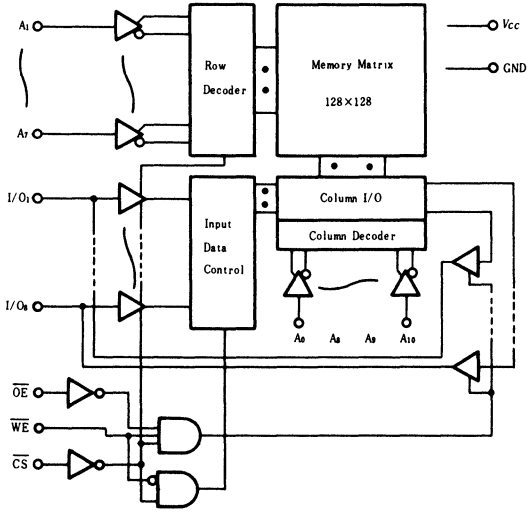
2048-word × 8-bit High Speed Static CMOS RAM

■FEATURES

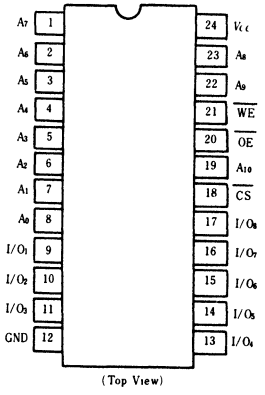
- High Density Small-Sized Package
- Projection Area Redueced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby Standby: 100μW (typ.)
- Low Power Operation; Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

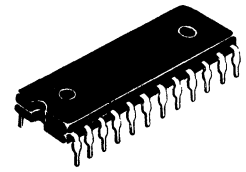
HM6116LP-2, HM6116LP-3, HM6116LP-4

HITACHI
HLN112
LITERATURE NO.

2048-word × 8-bit High Speed Static CMOS RAM

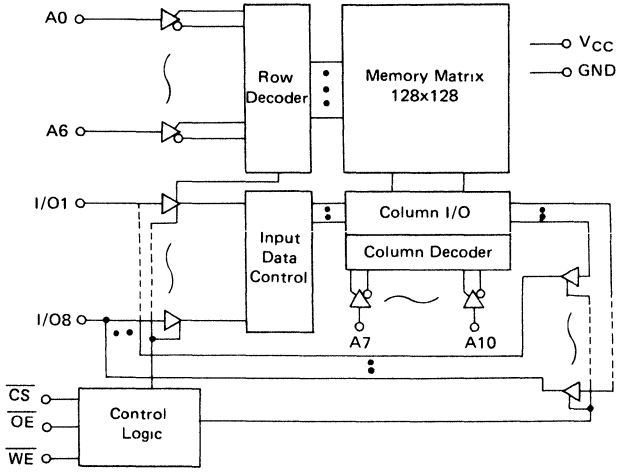
■ FEATURES

- Single 5V Supply and High Density 24 pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 20μW (typ.)
  Operation: 160mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

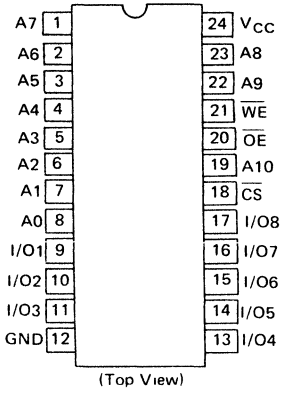


(DP-24)

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

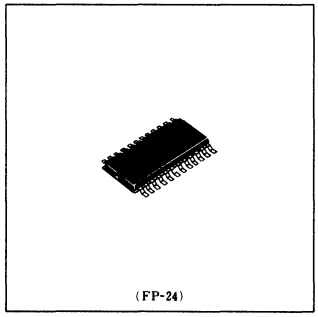
HM6116LFP-2, HM6116LFP-3, HM6116LFP-4

—Preliminary—

2048-word × 8-bit High Speed Static CMOS RAM

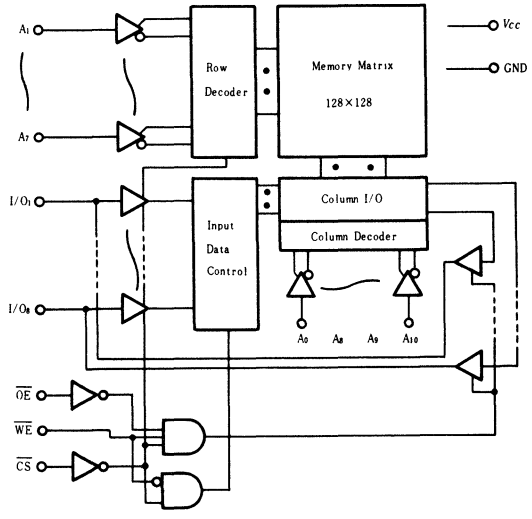
■FEATURES

- High Density Small-sized Package
- Projection Area Redueced to One-Thirds of conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation; Standby: 10μW (typ.) Operation: 160mW (typ.)
- Completely Static RAM: No Clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

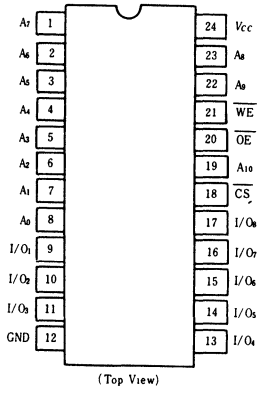


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



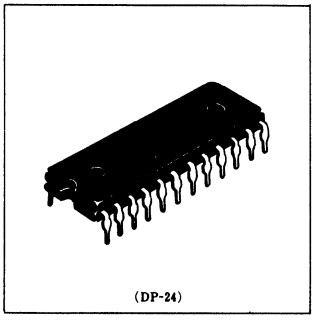
(Top View)

HM6117P-3, HM6117P-4 —Preliminary—

2048-word × 8-bit High Speed Static CMOS RAM

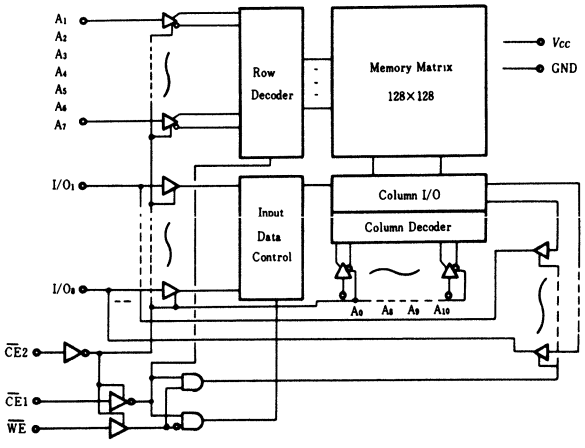
■FEATURES

- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Low Power Operation: Standby: 100μW (typ.) Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

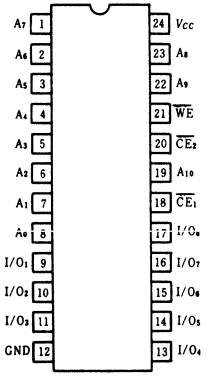


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

HM6117FP-3, HM6117FP-4

Preliminary—

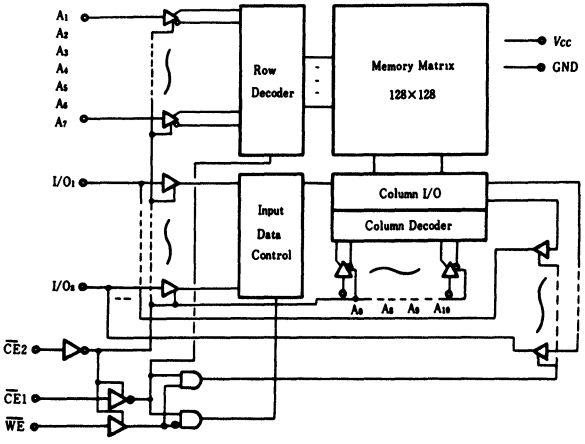
2048-word × 8-bit High Speed Static CMOS RAM

■FEATURES

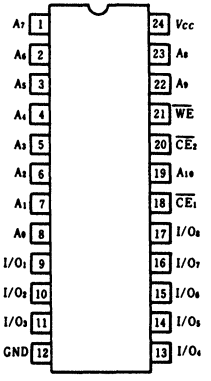
- High Density Small Sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply and High Density 24 pin Package.
- High Speed: Fast Access Time 150ns/200ns (max.)
- Low Power Standby and Low Power Operation: Standby: 100μW (typ.) Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



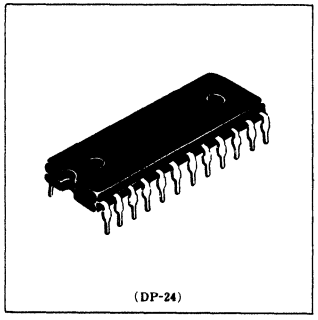
(Top View)

HM6117LP-3, HM6117LP-4 —Preliminary—

2048-word × 8-bit High Speed Static CMOS RAM

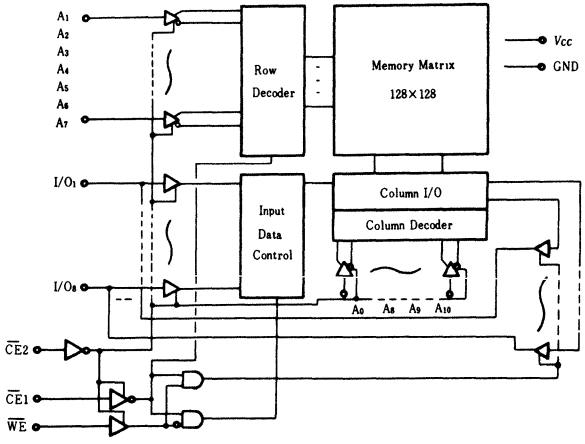
■FEATURES

- Single 5V Supply and High Density 24 Pin Package.
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation;
  Standby: 10μW (typ.) Two Chip Enable Input for Battery Back up
  Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

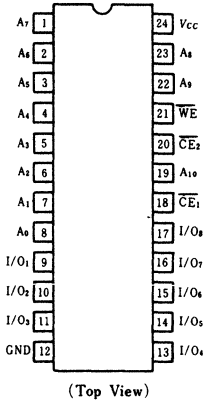


(DP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



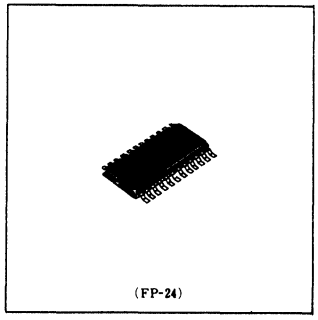
(Top View)

HM6117LFP-3, HM6117LFP-4 —Preliminary—

2048-word × 8-bit High Speed Static CMOS RAM

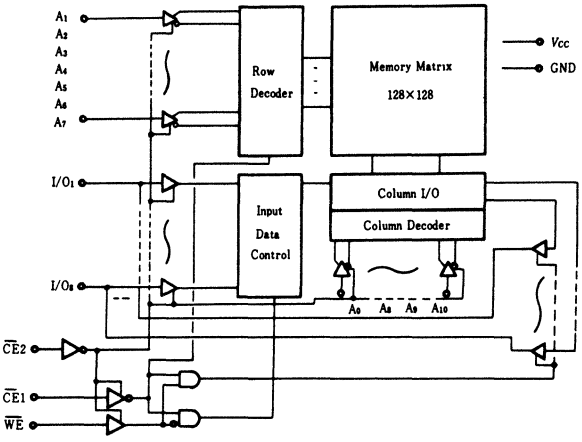
■FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 150ns/200ns max.
- Low Power Standby and Low Power Operation;
  Standby: 10μW (typ.) Two Chip Enable Input for Battery Back up
  Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

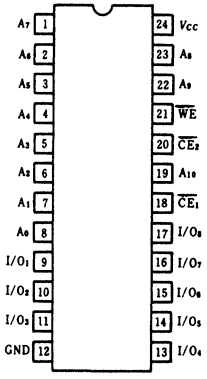


(FP-24)

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

HM6167, HM6167-6, HM6167-8, HM6167P, HM6167P-6, HM6167P-8

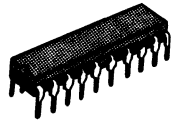
HITACHI
HLN113
LITERATURE NO.

16384-word × 1-bit High Speed Static CMOS RAM

■FEATURES

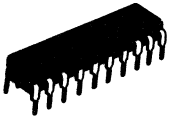
- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time – 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 25mW Typ. and Operating 150mW Typ.
- Completely Static Memory . . . . . No Clock nor Refresh Required
- Fully TTL Compatible – All Inputs and Output
- Separate Data Input and Output . . . . . Three State Output
- Pin-Out Compatible with Intel 2167 Series

HM6167, HM6167-6,
HM6167-8



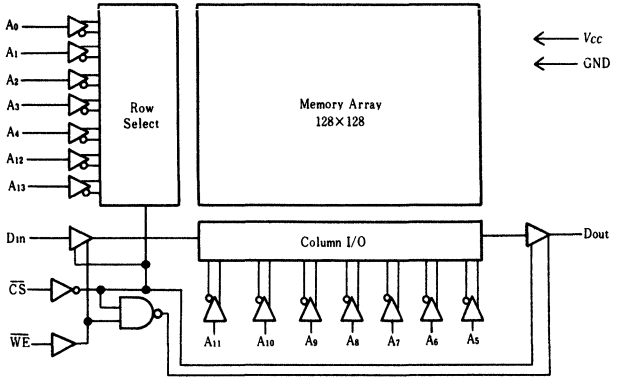
(DG-20)

HM6167P, HM6167P-6,
HM6167P-8

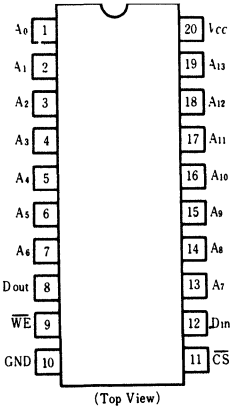


(DP-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

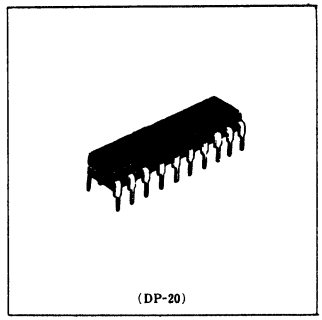
HM6167LP, HM6167LP-6, HM6167LP-8

HITACHI
HLN109
LITERATURE NO.

16384-word × 1-bit High Speed Static CMOS RAM

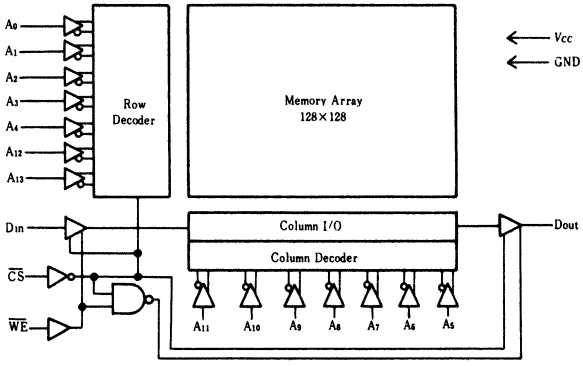
■FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 5μW (typ) and Operating 150mW (typ.)
- Completely Static Memory. . . . . .No Clock or Refresh Required
- Fully TTL Compatible. . . . . .All Inputs and Output
- Separate Data Input and Output . . . . . .Three State Output
- Capable of Battery Back up Operation

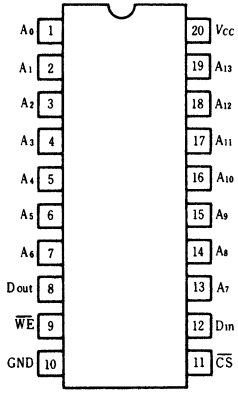


(DP-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

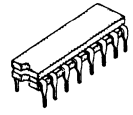
HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM4716AP-1, HM4716AP-2 HM4716AP-3, HM4716AP-4

HITACHI
HLN143
LITERATURE NO.

16384-word × 1-bit Dynamic Random Access Memory

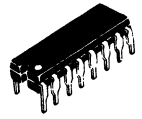
The HM4716A is a 16,384 word by 1 bit MOS random access memory circuit fabricated with HITACHI's double poly N-channel silicon gate process for high performance and high functional density. The HM4716A uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation. Multiplexed address inputs permit the HM4716A to be packaged in a standard 16 pin DIP on 0.3 inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The HM4716A is designed to facilitate upgrading of the 16-pin 4K RAM. However, the data output latch incorporated in the present 4K design is not appropriate for 16K RAM's. This new generation of memory products (16K RAM's) requires a slightly modified output stage to allow more system flexibility. Instead of the conventional latch, the HM4716A output is controlled by the Column Address Storobe ($\overline{CE}$). Data out of the HM4716A will remain valid from the access time from the Column Address Strobe unitl $\overline{CE}$ goes into precharge (logic 1). However, in early write cyles ($\overline{W}$ active low before $\overline{CE}$ goes low), the data output will remain in the high impedance (open-circuit) state throughout the entire cycle. This type of output operation results in some very significant system implications.

HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4



(DG-16A)

HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4



(DP-16)

1. Common I/O Operation

If all write operation are handled in the "early write" mode, then data in can be connected directly to data-out on a printed circuit board.

2. Data Output Control

Data well remain valid at the output during a read cycle from TCELQV until $\overline{CE}$ returns to precharge.

This allows data to be valid from one cycle up until a new memory cycle begins.

3. Two Methods of Chip Selection

Both CE and/or $\overline{RE}$ can be decoded for chip selection.

4. Refresh

Refreshing can be accomplished every 2ms by either of the two following methods:

(1) normal read or write cycles on 128 addresses, A0 to A6.

(2) $\overline{RE}$ only cycles on 128 addresses, A0 to A6.

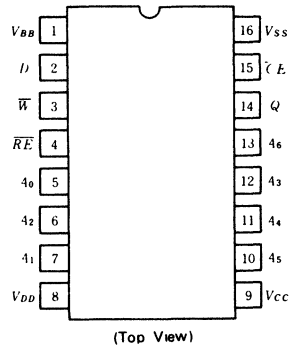
A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

$\overline{RE}$ only regreshes results in a substantial reduction in operating power.

5. Page Mode Operation

The HM4716A is designed for page mode operation.

■ **PIN ARRANGEMENT**



(Top View)

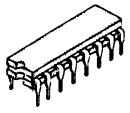
HM4816A-3, HM4816A-3E, HM4816A-4, HM4816A-7, HM4816AP-3, HM4816AP-3E, HM4816AP-4, HM4816AP-7

16384-word × 1-bit Dynamic Random Access Memory

The HM4816A is a new generation MOS dynamic RAM circuit organized as 16,384 words by 1 bit. As a state-of-the art MOS memory device, the HM4816A (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power.

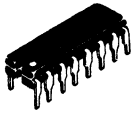
The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the HM4816A a truly superior RAM product. Multiplexed address inputs permits the HM4816A to be packaged in standard 16-pin DIP. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

HM4816A-3, HM4816A-3E,
HM4816A-4, HM4816A-7



(DG-16B)

HM4816AP-3, HM4816AP-3E,
HM4816AP-4, HM4816AP-7



(DP-16)

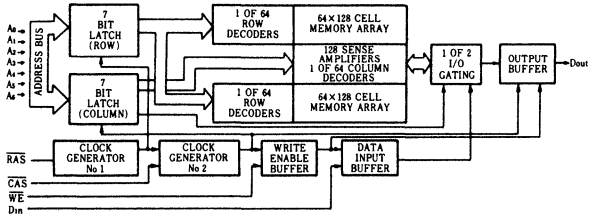
■ FEATURES

- Single 5V supply
  Low power standby and operation
  (Standby: 11mW max., operation: 150mW max.)
- Fast access time & cycle time

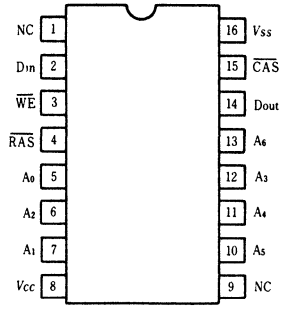
	HM4816A-3 HM4816AP-3	HM4816A-3E HM4816AP-3E	HM4816A-4 HM4816AP-4	HM4816A-7 HM4816AP-7
Maximum Access Time (ns)	100	105	120	150
Read, Write Cycle (ns)	235	200	270	320
Read-Modify-Write Cycle (ns)	285	235	320	410

- Directly TTL compatible: All inputs & outputs
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary.
- Common I/O capability using "easy write" operation.
- Read modify write, $\overline{RAS}$ only refresh and page mode capability
- Only 128 refresh cycle required every 2ms
- Compatible with Intel 2118-3/-4/-7

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HM4864-2, HM4864-3, HM4864P-2, HM4864P-3

HITACHI
HLN144
LITERATURE NO.

65536-word × 1-bit Dynamic Random Access Memory

The HM4864 is a 65,536-words by 1-bit, MOS random access memory circuit fabricated with HITACHI's double-poly N-channel silicon gate process for high performance and high functional density. The HM4864 uses a single transistor dynamic storage cell and dynamic control circuitry to achieve high speed and low power dissipation.

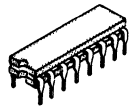
Multiplexed address inputs permit the HM4864 to be packaged in a standard 16 pin DIP on 0.3 inch centers.

This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of +5V with ±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs, on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The HM4864 also incorporates several flexible timing/operating modes.

In addition to the usual read,write, and read-modify-write cycles, the HM4864 is capable of delayed write cycles, page-mode operation and $\overline{RAS}$-only refresh.

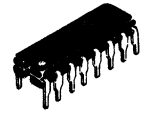
Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

HM4864-2, HM4864-3



(DG-16A)

HM4864P-2, HM4864P-3

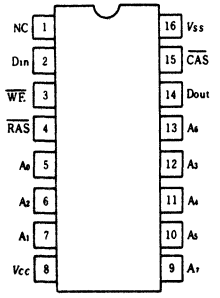


(DP-16)

■ FEATURES

- Recognized industry standard 16-pin configuration
- 150ns access time, 270ns cycle time (HM4864-2, HM4864P-2)
- 200ns access time, 335ns cycle time (HM4864-3, HM4864P-3)
- Single power supply of +5V±10% with a built-in V_{BB} generator
- Low Power; 330 mW active. 20 mW standby (max)
- The inputs TTL compatible, low capacitance, and protected against static charge
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- 128 refresh cycle

■ PIN ARRANGEMENT



(Top View)

HN462716G

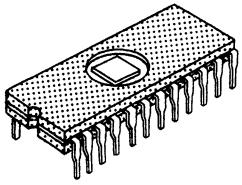
HITACHI
HLN160
LITERATURE NO.

2048-word × 8-bit UV Erasable and Electrically Programmable Read Only Memory

The HN462716G is a 2048 word by 8 bit erasable and electrically programmable ROMs. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

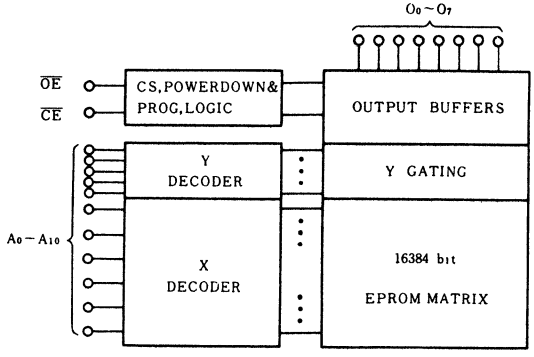
- Single Power Supply ..... +5V ±5%;
- Simple Programming .....Program Voltage: +25V DC
  Programs with One 50ms Pulse
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded-on Chip Address Decode
- Access Time ..... 450ns Max.
- Low Power Dissipation .....555mW Max. Active Power
  213mW Max. Standby Power
- Three State Output ..... OR-Tie Capability
- Interchangeable with Intel 2716

HN462716G

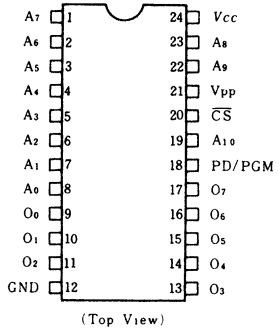


(DG-24B)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

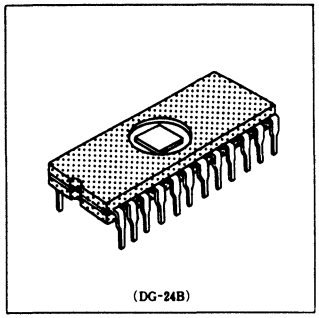


HN462716G-1, HN462716G-2

2048-word × 8-bit U.V. Erasable and Electrically Programmable Read Only Memory

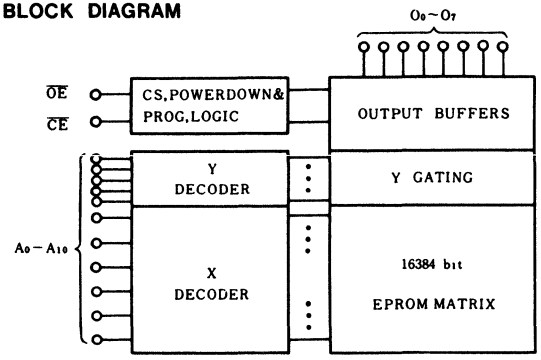
The HN462716 is a 2048 word by 8 bit erasable and electrically programmable ROMs. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to exposes the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

- Single Power Supply ····· +5V ±5%;
- Simple Programming ····· Program Voltage: +25V DC
  Programs with One 50ms Pulse
- Static ····· No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded-on Chip Address Decode
- Access Time ····· 350ns Max.: HN462716G-1
  390ns Max.: HN462716G-2
- Low Power Dissipation ···· 555mW Max. Active Power
  161mW Max. Standby Power
- Three State Output ····· OR-Tie Capability
- Interchangeable with Intel 2716

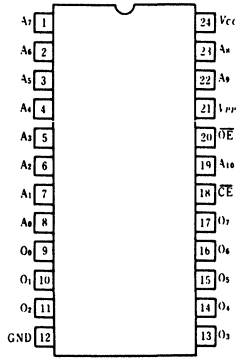


(DG-24B)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

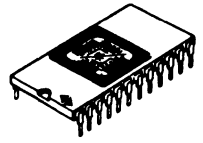
HN462532, HN462532G, HN462532G-2

HITACHI
HLN161
LITERATURE NO.

4096-word × 8-bit U.V. and Erasable and Programmable Read Only Memory

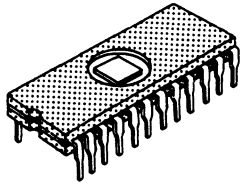
The HN462532 is a 4096 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 24-pin, dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

HN462532



(DC-24C)

HN462532G
HN462532G-2

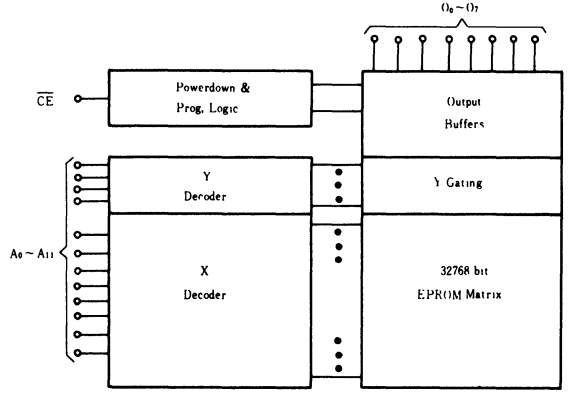


(DG-24B)

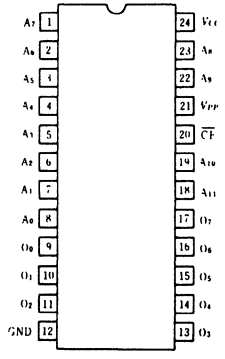
■ FEATURES

- Single Power Supply ..... +5V ±5%
- Simple Programming ..... Program Voltage: +25V D.C.
  Program with One 50ms Pulse
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-Chip Address Decode
- Access Time ..... 450ns (max.) HN462532/G
  390ns (max.) HN462532G-2
- Low Power Dissipation .... 858mW (max) Active Power
  201mW (max) Standby Power
- Three Stste Output ..... OR-Tie Capability
- Compatible with TMS2532

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



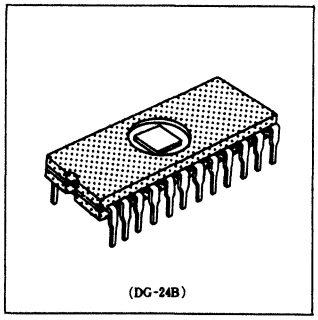
(Top View)

HN482732AG SERIES

—Under Development—

4096-word × 8-bit U.V. Erasable and Programmable Read Only Memory

The HN482732A is a 4096-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 24 pin dual-in-line package with transparent lid.
The transparent lid on the package allow the memory content to be erased with ultraviolet light.

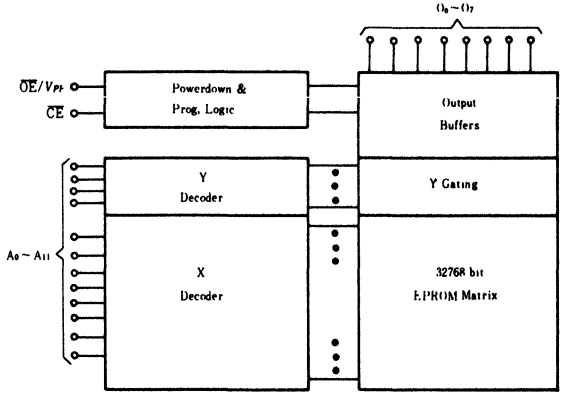


(DG-24B)

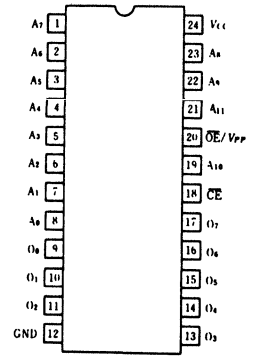
■ FEATURES

- Single Power Supply ..... +5V ±5%
- Simple Programming ..... Program Voltage: +21V D.C
  Program with one 50ms Pulse
- Static..... No clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time ..... HN482732AG-20 200ns (max)
  HN482732AG-25 250ns (max)
  HN482732AG-30 300ns (max)
- Absolute Max. Rating of Vpp Pin ... 28V
- Low Stand-by Current ..... 35mA (max)
- Compatible with Intel 2732A

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HN482764, HN482764-3, HN482764G, HN482764G-3

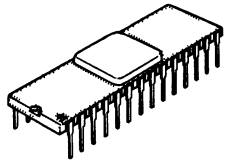
—Preliminary—

HITACHI
HLN164
LITERATURE NO.

8192-word × 8-bit U.V. Erasable and Programmable Read Only Memory

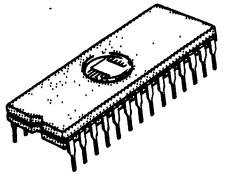
The HN482764 is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

HN482764, HN482764-3



(DC-28B)

HN482764G, HN482764G-3

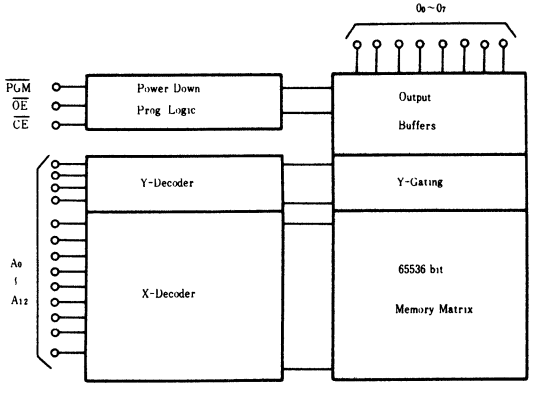


(DG-28)

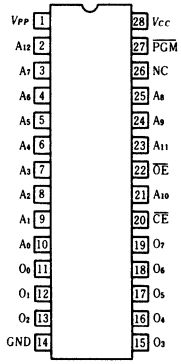
■ FEATURES

- Single Power Supply ..... +5V ± 5%
- Simple Programming ..... Program Voltage: +21V D.C.
  Program with one 50ms Pulse
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time..... HN482764/G 250ns max
  HN482764/G-3 300ns max
- Absolute Max. Rating of Vpp pin ... 28V
- Low Stand-by Current..... 35mA max.
- Compatible with Intel 2764

■ BLOCK DIAGRAM



■ PIN ARRANGMENT



(Top View)

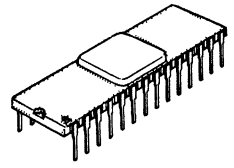
HN482764-4, HN482764G-4

HITACHI
HLN165
LITERATURE NO.

8192-word × 8-bit U.V. Erasable and Programmable Read Only Memory

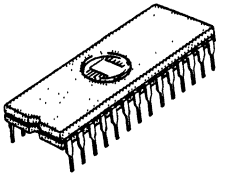
The HN482764 is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

HN482764-4



(DC-28B)

HN482764G-4

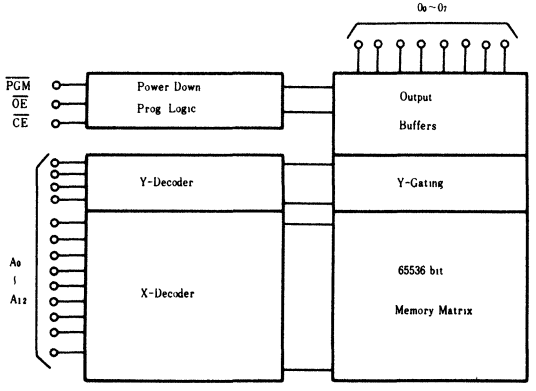


(DG-28)

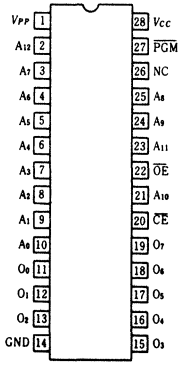
■ FEATURES

- Single Power Supply ..... +5V ±5%
- Simple Programming ..... Program Voltage: +21V D.C.
  Program with one 50ms Pulse
- Static ..... No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time..... 450ns max.
- Absolute Max. Rating of Vpp Pin ... 28V
- Low Stand-by Current..... 35mA max.
- Compatible with Intel 2764

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



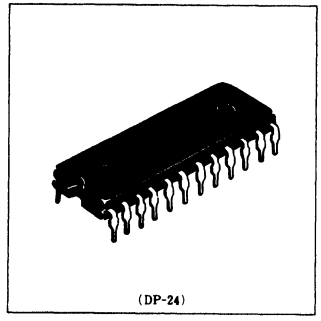
(Top View)

HN48016P

HITACHI
HLN163
LITERATURE NO.

2048-word × 8-bit Electrically Erasable and Programmable ROM

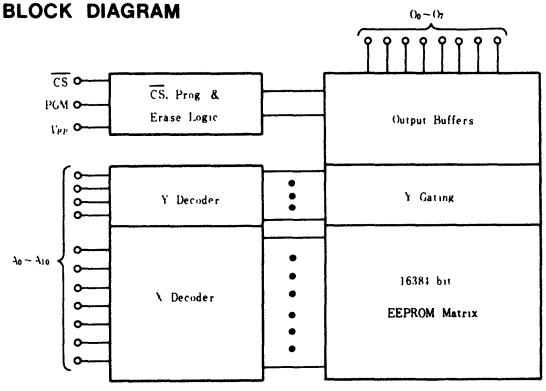
This device operates from a single power supply and features fast single address location programming. All the words are erased by one TTL level pulse. Erasing the bit pattern and programming new pattern can be made within 42 seconds.


(DP-24)

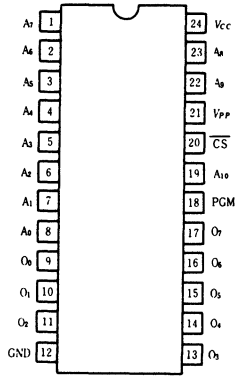
■ FEATURES

- Single Power Supply ..... +5V ±5%
- Simple Programming ..... Program voltage: +25V D.C.
  Program with one 20ms pulse.
- Electrically Erasing ..... Erase Voltage: +25V D.C.
  Erase all words with one 200ms pulse.
- Fully Static ..... No clocks required.
- Inputs and Outputs TTL compative during read, program and erase mode.
- Fully Decoded ..... On-Chip Address Decode.
- Access Time ..... 350ns Max.
- Low Power Dissipation .... 300mW Max.
- Three State Output ..... OR-Tie Capability
- Pin-out Compatible with Intel 2716.

■ BLOCK DIAGRAM



■ PIN. ARRANGEMENT

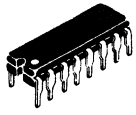


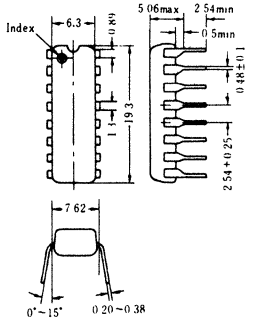
(Top View)

PACKAGING INFORMATION (Dimensions in mm)

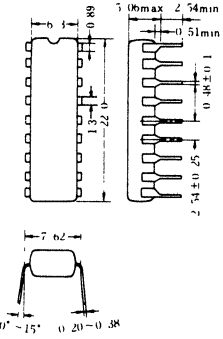
• DUAL-IN-LINE PLASTIC

• DP-16

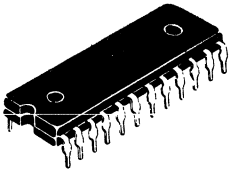


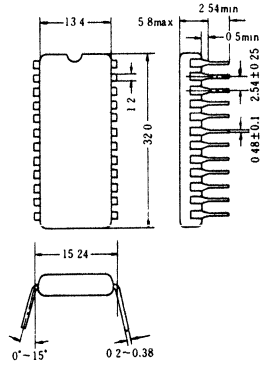


• DP-18



• DP-24



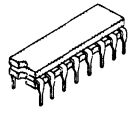


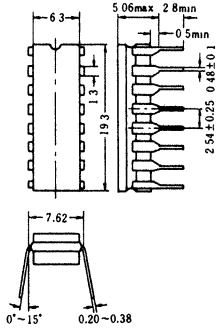
Applicable ICs

DP-16	HM4716AP-1, HM4716AP-2, HM4716AP-3, HM4716AP-4,
DP-18	HM472114AP-1, HM472114AP-2, HM472114P-3, HM472114P-4, HM4334P-3, HM4334P-4, HM6148P, HM6148P-6, HM6148LP, HM6148LP-6, HM4315P, HM6147P, HM6147P-3, HM6147LP, HM6147LP-3
DP-24	HM6116P-2, HM6116P-3, HM6116P-4, HM6116LP-2, HM6116LP-3, HM6116LP-4, HN462316EP, HN46332P, HN48364P, HN48016P

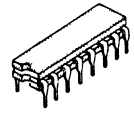
• DUAL-IN-LINE CERAMIC (Glass-sealed)

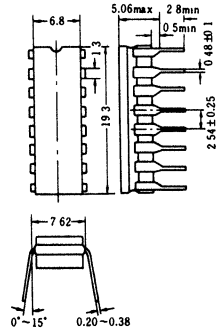
• DG-16



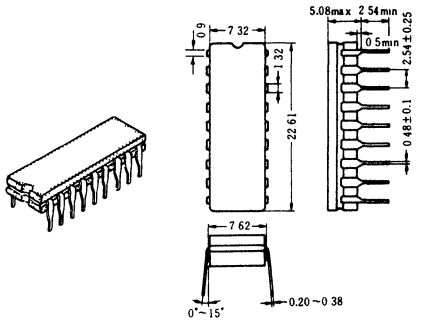


• DG-16A

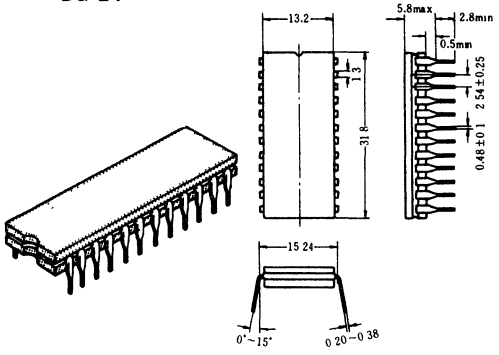




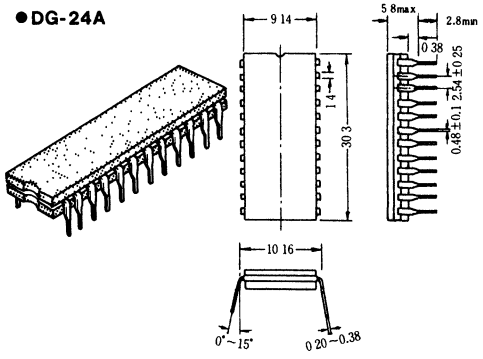
● DG-18



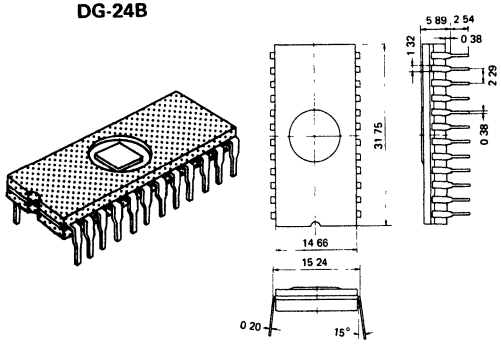
● DG-24



● DG-24A



DG-24B

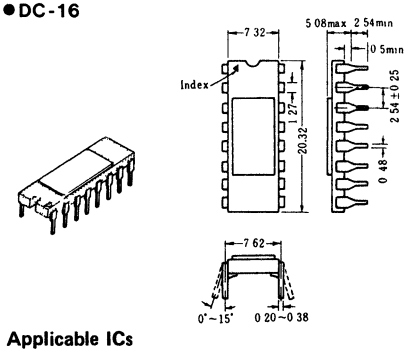


Applicable ICs

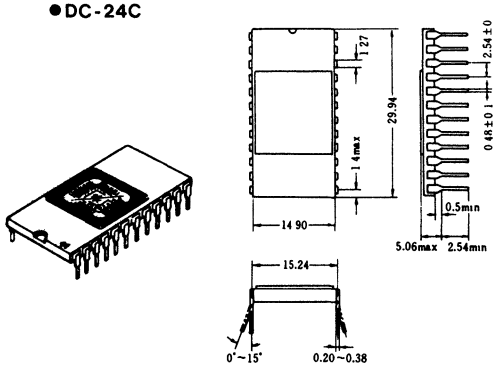
DG-16	HM2105, HM2106, HM10414, HM10414-1 HM2504, HM2504-1, HD2912
DG-16A	HM4716A-1, HM4716A-2, HM4716A-3, HM4716A-4, HM2110, HM2110-1, HM2110-2, HM2112, HM2112-1, HM2510, HM2510-1, HM2510-2, HM2511, HM2511-1, HD2916, HD2923
DG-18	HM72114A-1, HM472114A-2, HM472114-3 HM472114-4, HM10470, HM10470-1, HN25044, HN25045, HN25084, HN25085
DG-24	HN25088, HN25089
DG-24A	HM10422, HM100422
DG-24B	HN462716G

● **DUAL-IN-LINE CERAMIC (with Lid)**

● DC-16



● DC-24C



Applicable ICs

DC-16	HM4816, HM4864-2, HM4864-3
DC-24C	HN462716, HN462532, HN462732

64K Dynamic Ram

	MANUFACTURER		HITACHI		FUJITSU		INTEL	
	ITEM	UNIT	HM 4864-2	HM 4864-3	MB 8264-15	MB 8264-20	12164-5	12164-6
	T_{ACC}	ns	150	200	150	200	150	200
FUNCT	NO. 1 P/N		NC		NC (Hidden Refresh)			
FUNCT	Refresh	Cycle	128		128			
DC	Abs. Max.	V	7		7		7.5	
DC	I_{CC} OP'N	mA	60		45		67	60
DC	I_{CC} STDBY	mA	3.5		5		8	
DC	V_{IH} min/max	V	2.4/6.5		2.4/6.5		2.4/7.0	
DC	V_{IL} min/max	V	−1.0/0.8		−1.0/0.8		−2.0/0.8	
	trc	ns	270	335	320	330	300	375
	trwc	ns	270	335	350	375	345	435
	tcac	ns	100	135	100	135	85	110
	trcd	ns	50	65	50	65	35/65	45/90
	trp	ns	100	120	100	120	140	165
	tasr	ns	0	0	0	0	0	0
	trah	ns	20	25	15	20	25	35
	tasc	ns	−10	−10	0	0	0	0
	tcah	ns	45	55	45	55	35	45
	trcs	ns	0	0	0	0	0	0
	trch	ns	0	0	0	0	0	0
	twch	ns	45	55	45	55	45	55
	twp	ns	45	55	45	55	45	55
	trwl	ns	45	55	60	80	60	80
	tcwl	ns	45	55	60	80	60	80
	tds	ns	0	0	0	0	0	0
	tdh	ns	45	55	45	55	45	55
	twcs	ns	−20	−20	−10	−10	0	0
	trwd	ns	110	145	120	160	130	175
	tcwd	ns	60	80	70	95	65	85
	tcrp	ns	−20	−20	0	0		
	tref	ns	2	2	2	2		

Industry Cross Reference

MITSUBISHI (Old Spec)		MOSTEK		MOTOROLA		T.I.		
M 58764-15	M 58764-20	MK 4164-10	MK 4164-20	MCM 6664-15	6664-20	TMS 4164-15	TMS 4164-20	TMS 4164-25
150	200	100	120	150	200	150	200	250
NC		REF		REF		N/C		
256		128		128		256		
7		7		7		6		
54.5		60		50		37		
9		4		5		5		
2.4/6.5		2.4/V_{CC}+1		2.4/7.0		2.4/V_{dd}+0.3		
−1.0/0.8		−2.0/0.8		−1.0/0.8		−1.0/0.8		
310	375	235	265	300	330	280	350	410
325	395	260	315	300	330	280	350	410
100	135	50	60	75	100	100	135	165
50	65	50	60	75	100	50	65	85
150	165	125	135	100	120	100	120	150
0	0	0	0	0	0	0	0	0
25	25	10	10	20	25	20	25	35
−5	−5	0	0	0	0	−5	−5	−5
45	55	15	20	45	55	45	55	75
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
45	55	35	40	45	55	60	80	110
45	55	30	35	45	55	45	55	75
50	70	35	40	45	55	60	80	100
50	70	35	40	45	55	60	80	100
0	0	0	0	0	0	0	0	0
45	55	35	40	45	55	60	80	100
−10	−10	0	0	−10	−10	−5	−5	−5
110	145	110	120	120	155	90	130	190
60	80	50	60	45	55	40	50	60
−20	−20	—	—	−10	−10	0	0	0
4	4	2	2	2	2	4	4	4

Courtesy of Hitachi America, Ltd. December 1, 1980

16K BIT (2K X 8) STATIC RAM

ITEM/TYPE		HM6116P			TC5516P			TM2016P		
MAKER		HITACHI			TOSHIBA			TOSHIBA		
PROCESS		CMOS 3 um T_{ox} = 50 nm			CMOS 3 um T_{ox} = 70 nm Contact Hole 2 um□			NMOS		
CHIP SIZE (mm^2)		4.76 × 5.50 = 26.2			5.06 × 5.77 = 29.2					
MEMORY CELL	Cell Size (um^2)	28 × 32 = 896			33 × 34 = 1,122					
	Organization	High Resistance Single Poly Sil.			6 Trs CMOS					
PIN FUNCTION	PIN NO.	NAME	R	W	NAME	R	W	NAME	R	W
	18	$\overline{CS}$	L	L	$\overline{CE_2}$	L	L	$\overline{CS}$	L	L
	20	$\overline{OE}$	L	X	$\overline{CE_1}$	L	L	$\overline{OE}$	L	X
	21	$\overline{WE}$	H	L	R/$\overline{W}$	H	L	$\overline{WE}$	H	L
OUTLINE		24 Pin Plastic			24 Pin Plastic			24 Pin Plastic		
DC CHARACTER-ISTICS	V_{cc} Voltage	5V ±10%			5V ±10%			5V ±10%		
	V_{in} (V_{il}) (V_{ih})	(−1.0, 0.8) (2.2, 6.0)			(−0.3, 0.8) (2.2, V_{cc}+0.3)			(−0.5, 0.8) (2.2 V_{cc}+1.0)		
	I_{cc}	70/60/60 mA Max			40 mA Typ			120/100 mA Max		
	I_{sb}	12/12/12 mA Max						15/15 mA Max		
	I_{sb1}	0.1/0.1/0.1 mA Max			50 μA Max			(Turn-on Peak Cur) 30 mA Max		
	I_{ol} (0.4V Max)	4/2.1/2.1 mA			2.0 mA			2.1 mA		
	I_{oh} (2.4V Min)	−1.0/−1.0/−1.0 mA			−1.0 mA			−1.0 mA		
READ (Unit: ns)	t_{AA}	120/150/200 Max			250 Max			100/150 Max		
	t_{ACS}	120/150/200 Max			250 Max			100/150 Max		
	t_{OE}	80/100/120 Max			100 Max			35/55 Max		
	t_{CLZ}	10/15/15 Min			10 Min			10/10 Min		
	t_{CHZ}	40/50/60 Max			80 Max			40/55 Max		
	t_{OLZ}	10/15/15 Min			10 Min			5/5 Min		
	t_{CW}	70/90/120 Min			200 Min			90/120 Min		
	t_{AW}	105/120/140 Min			250 Min			90/120 Min		
	t_{AS}	20/20/20 Min			50 Min			20/20 Min		
	t_{WP}	70/90/120 Min			200 Min			70/100 Min		
	t_{WR}	5/10/10 Min			0 Min			10/10 Min		
	t_{DH}	5/10/10 Min			0 Min			10/15 Min		
		CMOS-NMOS Low Power-High Speed			Memory Cell CMOS Input Level Is Not Good I_{sb1} Is Small I_{cc} Is Not Decided			NMOS Hi Speed		

NOTE: Harris has announced CMOS 6516 2K X 8 w/preliminary data sheet only.
Data is insufficient to be included in this Cross Reference.

INDUSTRY CROSS REFERENCE

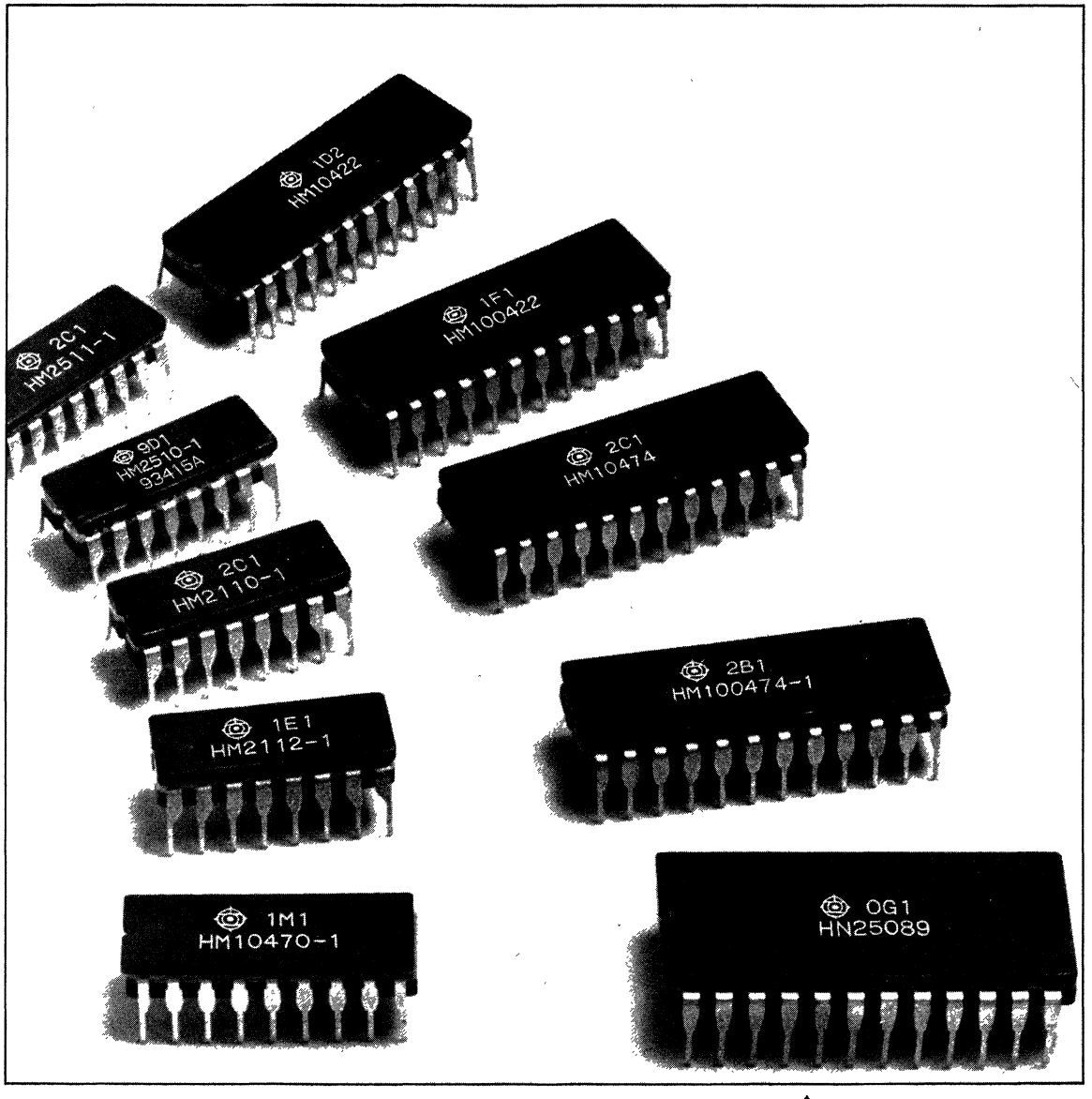
M58725			MSM2128			MK4802			HN462716			TMS4016		
MITSUBISHI			OKI			MOSTEK			HITACHI			TI		
NMOS 3 um T_{ox} = 50 nm V_{th} 3 Types			3 um NMOS			Poly 5 um NMOS						4.5 um NMOS		
4.65 × 6.00 = 27.9			5.0 × 6.2 = 31.0						5.3 × 4.96 = 26.3			25.8		
980			1,122						22 × 33 = 484			1,032		
High Resistance Double Poly Sil			High Resistance						EPROM			4MOS + 2R		
NAME	**R**	**W**	**NAME**	**R**	**W**	**NAME**	**R**	**W**	**NAME**	**R**	**W**	**NAME**	**R**	**W**
$\overline{S}$	L	L	$\overline{CS}$	L	L	$\overline{CE}$	L	L	$\overline{CE}$	L	L	$\overline{S}$	L	L
$\overline{OE}$	L	H	$\overline{OE}$	L	X	$\overline{OE}$	L	X	$\overline{OE}$	L	H	$\overline{G}$	L	X
$\overline{WE}$	H	L	$\overline{WE}$	H	L	$\overline{WE}$	H	H	$\overline{V_{pp}}$	H	25V	$\overline{W}$	H	L
24 Pin Plastic			24 Pin Ceramic						24 Pin Cerdip			24 Pin Plastic		
5V ±10%			5V ±10%			5V ±10%			5V ±5%			5V ±5%		
(−0.5, 0.8) (2.0, 6.0)			(−0.3, 0.8) (2.0, 6.0)			(−2.0, 0.8) (2.0, 7.0)			(−0.1, 0.8) (2.0, V_{cc} +1.0)			(−1.0, 0.8) (2.0, 5.25)		
80/80 mA Max			120 mA Max			125 mA Typ			100 mA Max			(65 Typ) 95 mA Max		
10/10 mA Max			No Stand-by			15 mA Typ			35 mA Max					
			No Stand-by											
3.2 mA			2.1 mA			4.0 mA			2.1 mA			2 mA		
−1.0 mA			−1.0 mA			−1.0 mA			−0.4 mA			−0.2 mA		
150/200 Max			200 Max			70/90/120/200 Max			450 Max			450 Max		
150/200 Max			70 Max			35/45/60/100 Max			450 Max			150 Max		
50/60 Max			70 Max			35/45/60/100 Max			120 Max			150 Max		
10/20 Min			0 Min											
40/50 Max			TBD			35/45/60/100 Max			100 Max			120 Max		
			0 Min											
100/120 Min			120 Min									400 Min		
120/140 Min			120 Min											
20/20 Min			0 Min			0/0/0/0 Min						0 Min		
80/100 Min			120 Min			30/40/45/60 Min						400 Min		
0/0 Min			20 Min			45/55/75/130 Min						0 Min		
10/10 Min			0 Min			10/10/10/10 Min						0 Min		
			No Power Down			Clock Type Possible To Be Used As Static Min Write Cycle Address Activated						No Power Down C_{in} = 8 pF C_{out} = 12 pF		

Courtesy of Hitachi America, Ltd.
December '80

SECTION 2

BIPOLAR MEMORIES

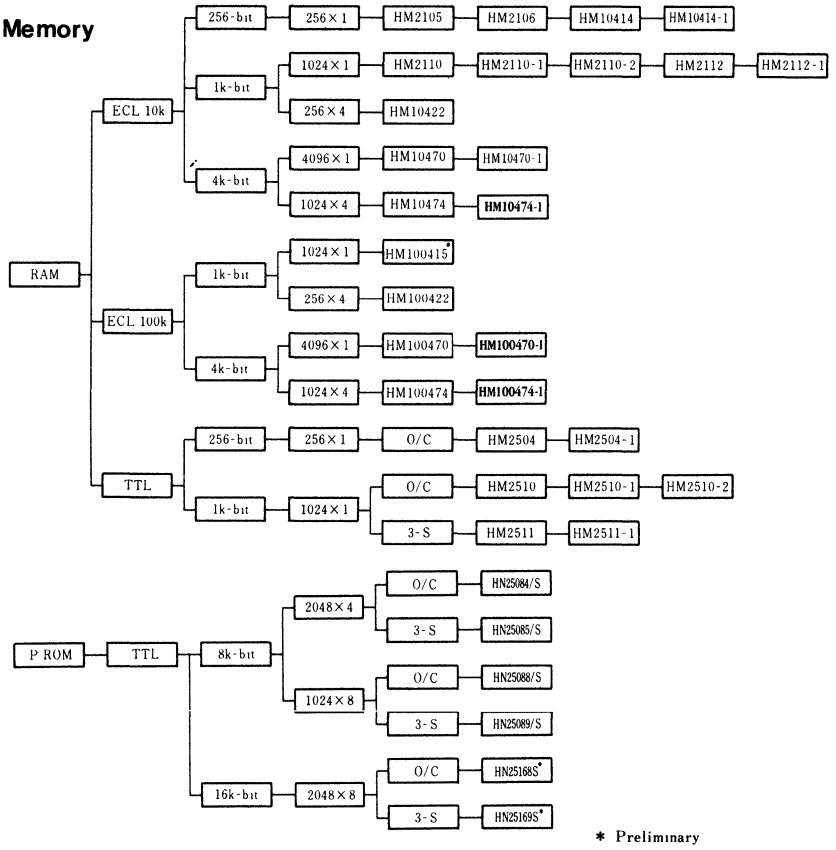
HITACHI
HLN100
LITERATURE NO.



HITACHI

BIPOLAR MEMORY FAMILY TREE

● Bipolar Memory



* Preliminary

■TYPICAL CHARACERISTICS OF BIPOLAR MEMORY

●Bipolar RAM

Level	Total Bit	Type No.	Organization (word × bit)	Output	Access Time (ns) max	Supply Voltage (V)	Power Dissipation (mW/bit)	Package** Pin No.	Package** F	Package** G	Package** P	Replacement
ECL 10k	256-bit	HM2105	256×1	Open Emitter	35	−5.2	1.8	16		●		F10410
		HM2106			15		1.8			●		
		HM10414			10		2.8			●		F10414
		HM10414-1			8					●		
	1k-bit	HM2110	1024×1		35		0.5			●		F10415
		HM2110-1			25					●		F10415A
		HM2110-2			20					●		
		HM2112			10		0.8			●		
		HM2112-1			8					●		
		HM10422	256×4		10		0.8	24		●		F10422
	4k-bit	HM10470	4096×1		25		0.2	18		●		F10470
		HM10470-1			15					●		
		HM10474	1024×4		25		0.2	24		●		F10474
ECL 100k	1k-bit	HM100415*	1024×1		10	−4.5	0.6	16		●		F100415
		HM100422	256×4		10		0.8	24	●	●		F100422
	4k-bit	HM100470	4096×1		25		0.2	18		●		F100470
		HM100474	1024×4		25		0.2	24	●	●		F100474
TTL	256-bit	HM2504	256×1	Open Collector	55	+5	1.8	16		●		93411
		HM2504-1			45					●		93411A
	1k-bit	HM2510	1024×1		70		0.5			●		
		HM2510-1			45					●		93415
		HM2510-2			35					●		93415A
		HM2511		3-state	70		0.5			●		
		HM2511-1			45					●		93425

●Bipolar PROM

Level	Total Bit	Type No.	Organization (word × bit)	Output	Access Time (ns) max	Supply Voltage (V)	Power Dissipation (mW)	Package** Pin No.	Package** F	Package** G	Package** P	Replacement
TTL	8k-bit	HN25084	2048×8	Open Collector	60	+5	550	18		●		82S184
		HN25085		3-state						●		82S185
		HN25084S*		Open Collector	50		550			●		
		HN25085S*		3-state						●		
		HN25088	1024×8	Open Collector	60		600	24		●		82S180
		HN25089		3-state						●		82S181
		HN25088S*		Open Collector	50		600			●		
		HN25089S*		3-state						●		
	16k-bit	HN25168S*	2048×8	Open Collector	60		600	24		●		82S190
		HN25169S*		3-state						●		82S191

* Preliminary

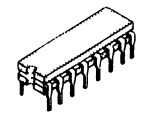
** The package codes of F, G, and P are applied to the package material as follows.
F . Flat Package, G : Cerdip, P . Plastic DIP

HM2110, HM2110-1, HM2110-2

HITACHI
HLN201
LITERATURE NO.

The HM2110 Series item is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time . . . . . 10ns (max.)
- Address access time . . . . . HM2110: 35ns (max.)
  HM2110-1: 25ns (max.)
  HM2110-2: 20ns (max.)
- Power consumption . . . . . 0.5mW/bit (typ)
- Output obtainable by Wired-OR (open emitter).



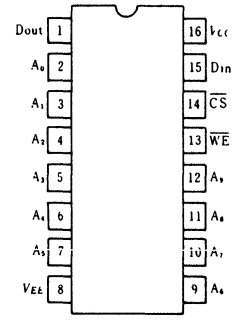
(DG-16A)

■TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

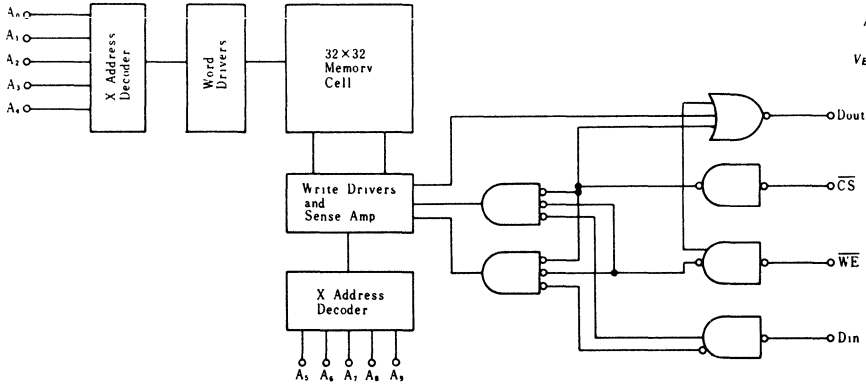
× : irrelevant
* : Read out noninverted

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM

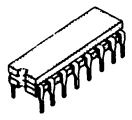


HM2112, HM2112-1

HITACHI
HLN204
LITERATURE NO.

1024-word × 1-bit Fully Decoded Random Access Memory

The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.



(DG-16A)

■ FEATURES

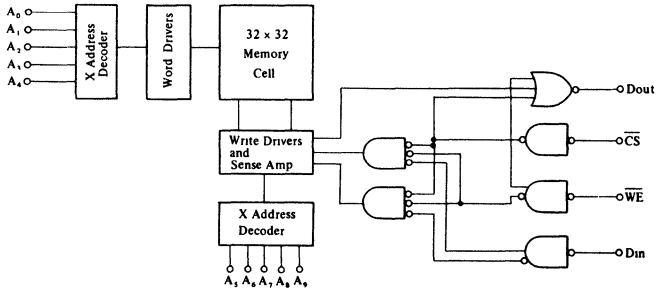
- Level ..... 10k ECL Compatible
- Construction ..... 1024-word by 1-bit
- Address Access Time ..... HM 2112 10ns (max.)
  HM2112-1 8ns (max.)
- Chip Select Access Time ..... 6ns (max.)
- Power Consumption ..... 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)

■ TRUTH TABLE

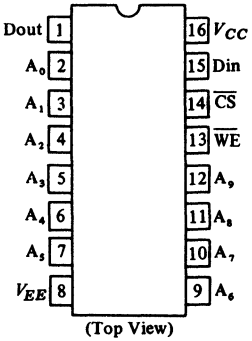
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

X : Irrelevant * : Read out noniverted

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

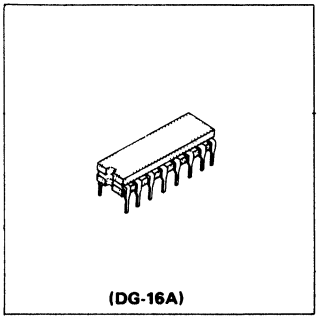
HM2510, HM2510-1, HM2510-2

HITACHI
HLN209
LITERATURE NO.

1024-word × 1-bit Fully Decoded Random Access Memory

The HM 2510 Series item is a 1024-word x 1-bit read/write random access memory developed for application to buffer memories, control memories, high-speed main memories, etc. It is a fully decoded, read/write, random access memory perfectly compatible with standard DTL and TTL logic families, desigend as an open collector output type for simplicity of expansion.

- Level ..... TTL compatible
- Construction ..... 1024-word x 1 bit
- Read access time ..... HM2510: 70ns (max.)
  HM2510-1: 45ns (max.)
  HM2510-2: 35ns (max.)
- Chip select access time ..... HM2510: 40ns (max.)
  HM2510-1: 30ns (max.)
  HM2510-2: 25ns (max.)
- Power consumption 0.5mW/bit
- Output ..... Open collector



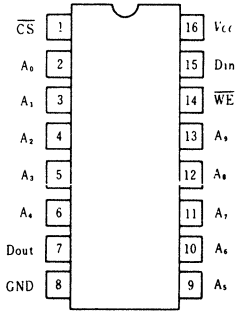
(DG-16A)

■TRUTH TABLE

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	×	Dout *	Read

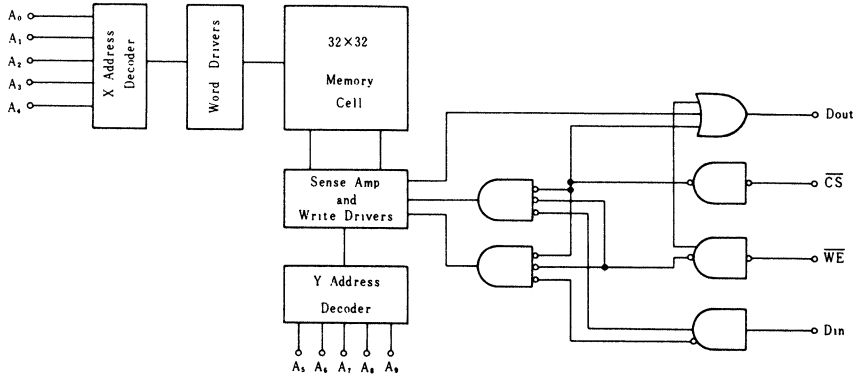
× : Don't care
* : Read out non-inverted

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



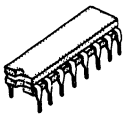
HM2511, HM2511-1

HITACHI
HLN212
LITERATURE NO.

1024-word × 1-bit Fully Decoded Random Access Memory

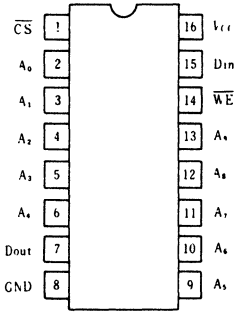
The HM2511 Series item is a 1024-word x 1-bit read/write random access memory with tri-state output developed for application to buffer memories, control memories, high-speed main memories, etc. It is a fully decoded, read/write, random access memory perfectly compatible with standard DTL and TTL logic families.

- Level ..... TTL compatible
- Construction ..... 1024-word x 1 bit
- Read access time ..... HM2511: 70ns (max)
  HM2511-1: 45ns (max)
- Chip select access time ..... HM2511: 40ns (max)
  HM2511-1: 30ns (max)
- Power consumption ..... 0.5 mW/bit
- Output ..... tri-state



(DG-16A)

■ PIN ARRANGEMENT



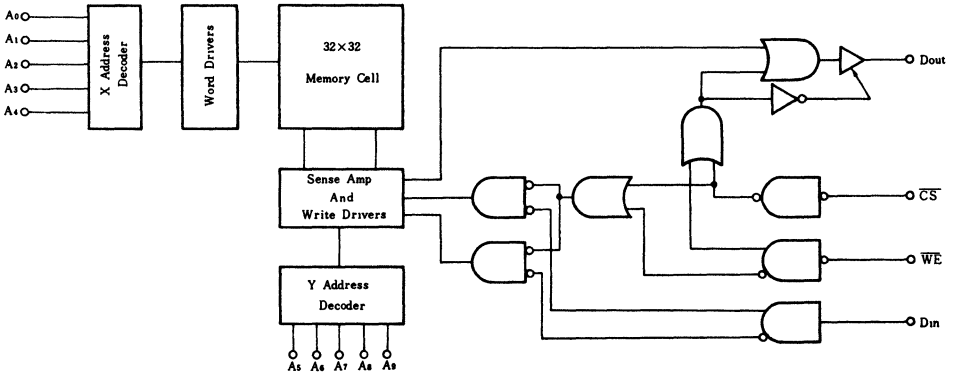
(Top View)

■ TRUTH TABLE

Input			Output Open Collector	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	High Z	Not Selected
L	L	L	High Z	Write "0"
L	L	H	High Z	Write "1"
L	H	×	Dout *	Read

× : Don't care
* : Read out noninverted

■ BLOCK DIAGRAM



HM10414, HM10414-1

HITACHI
HLN202
LITERATURE NO.

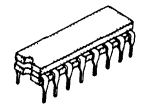
256-word × 1-bit Fully Decoded Random Access Memory

The HM10414 is ECL 10K compatible, 256-word x 1-bit, read/write, random access memory developed for high speed systems such as scratch pad and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10414 is encapsulated in cerdip-16pin package, compatible with Fairchild's F10414.

- Fully compatible with 10K ECL level
- Address access time; HM10414: 10ns (max.)
  HM10414-1: 8ns (max.)
- Write pulse width: 6ns (min.)
- Three chip select pins
- Output obtainable by wired-OR (open emitter)



(DG-16)

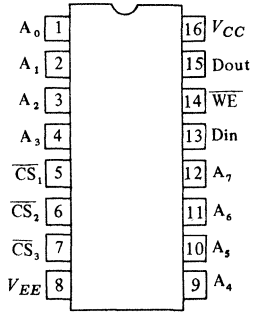
■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
any one H	X	X	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	X	Dout*	Read

X : Don't care

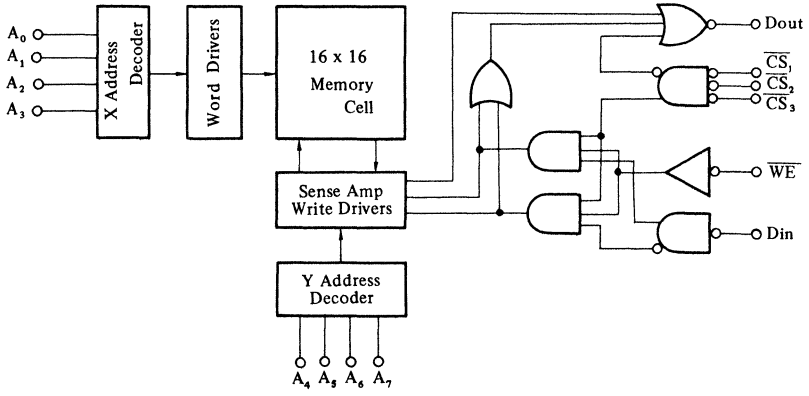
* : Read out non-inverted

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM10422

HITACHI
HLN205
LITERATURE NO.

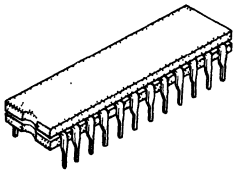
256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24pin package, or 24pin flat package, compatible with Fairchild's F10422.

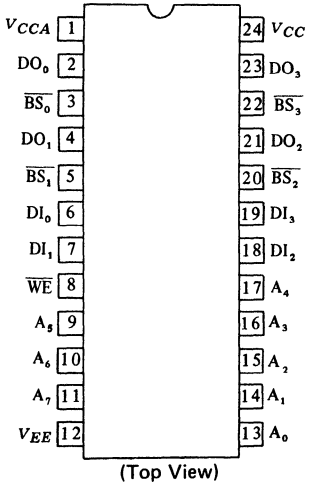


(DG-24A)

■ FEATURES

- 256-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns(min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



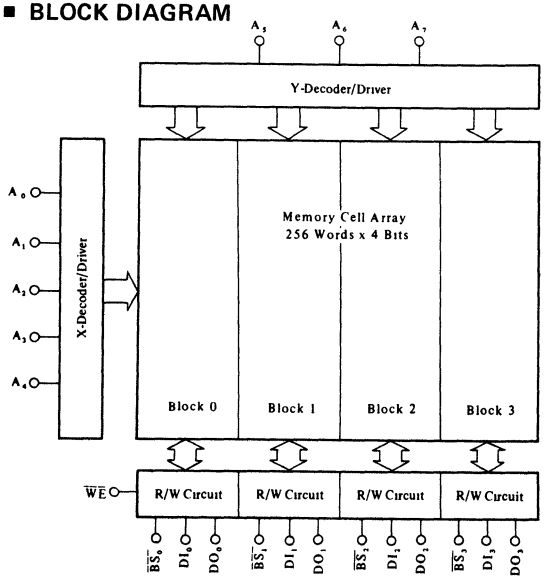
(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes: X ; irrelevant
* ; Read Out Noninvert

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM10470, HM10470-1

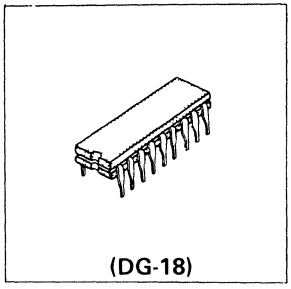
HITACHI
HLN206
LITERATURE NO.

4096-word × 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10470 is encapsulated in cerdip-18pin package, compatible with Fairchild's F10470.

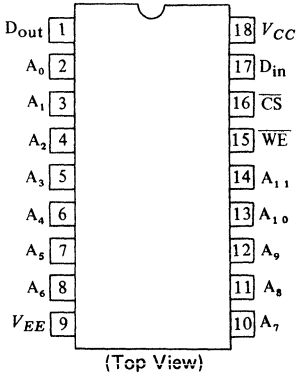


(DG-18)

■ FEATURES

- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM 10470 25 ns (max)
  HM 10470-1 15 ns (max)
- Write pulse width: HM 10470 20 ns (min)
  HM 10470-1 15 ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT

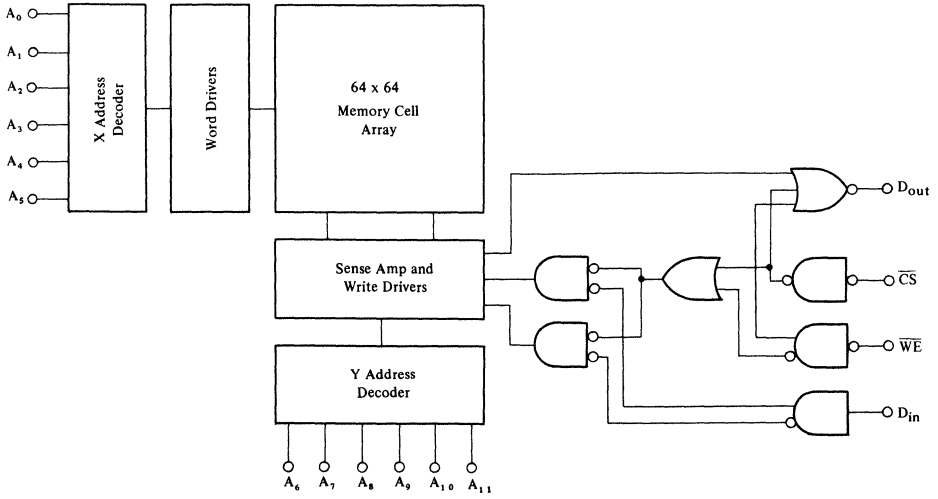


■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes) X; Irrelevant
*; Read Out Noninvert

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM10474, HM10474-1

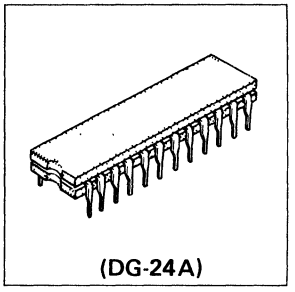
HITACHI
HLN207
LITERATURE NO.

1024-word × 4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.



(DG-24A)

■ FEATURES

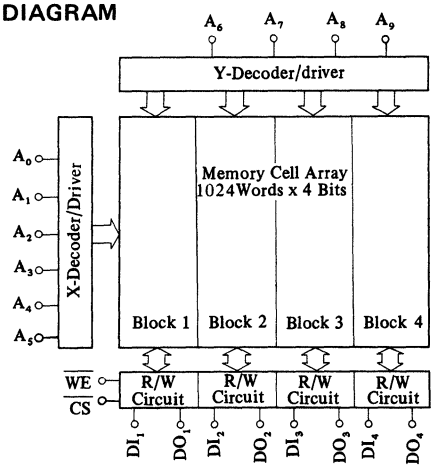
- 1024-word x 4bit organization
- Fully compatible with 10k ECL level
- Address access time: HM 10474 25 ns (max)
  HM 10474-1 15 ns (max)
- Write pulse width: HM 10474
  HM 10474-1 15 ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

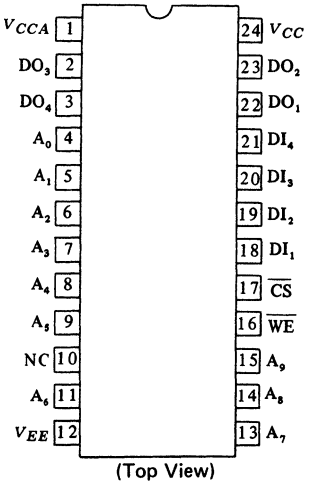
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	x	x	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	x	Dout*	Read

Notes : x,
*,

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

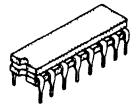
HM100415

HITACHI
HLN213
LITERATURE NO.

1024-word × 1-bit Fully Decoded Random Access Memory

The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer memories which require very high speeds.

The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.



(DG-16A)

■ FEATURES

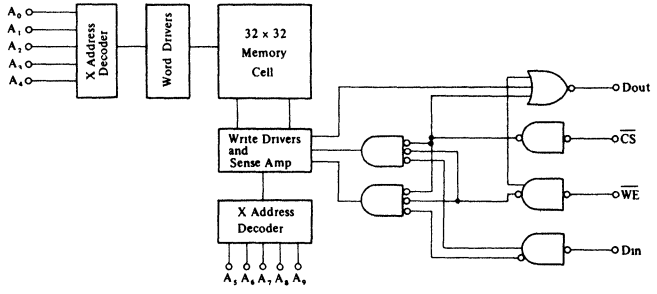
- Level ..... 100K ECL Compatible
- Organization ..... 1024-word by 1-bit
- Address Access Time ..... 10ns (max.)
- Chip Select Access Time ..... 5ns (max.)
- Power Consumption ..... 0.6mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)

■ TRUTH TABLE

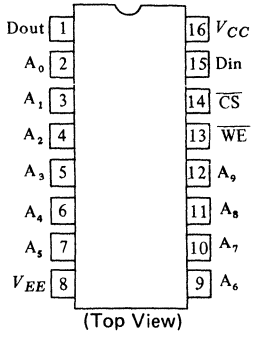
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

X : *:

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HM100422

HITACHI
HLN203
LITERATURE NO.

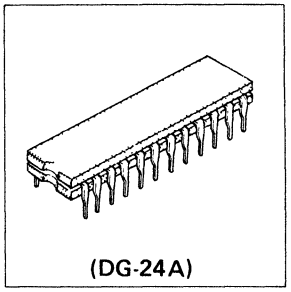
256-word × 4-bit Fully Decoded Random Access Memory

The HM100422 is ECL 100K compatible, 256-word x 4-bit, read/write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.



(DG-24A)

■ FEATURES

- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

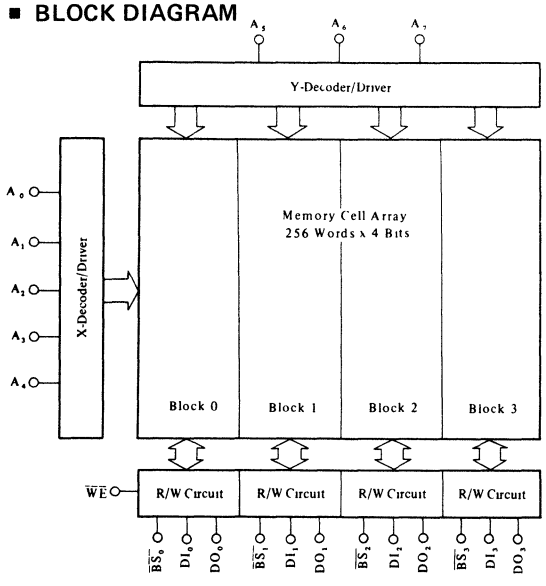
■ TRUTH TABLE

Item			Output	Mode
$\overline{BS}$	$\overline{WE}$	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

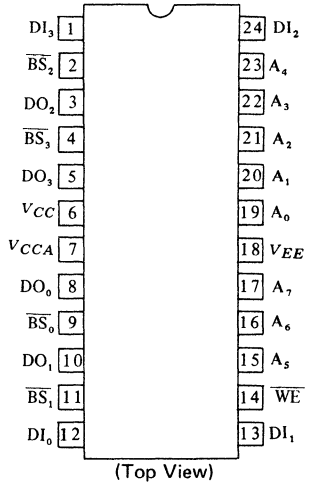
Notes: X ; irrelevant

* ; Read Out Noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM100470, HM100470-1

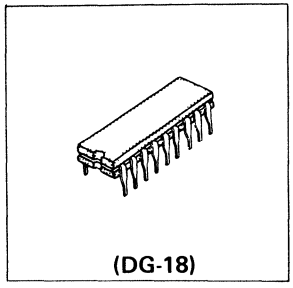
HITACHI
HLN214
LITERATURE NO.

4096-word × 1-bit Fully Decoded Random Access Memory

The HM100470 is ECL 100k compatible, 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.



(DG-18)

■ FEATURES

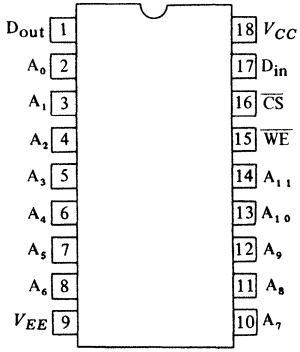
- 4096-word x 1-bit organization
- Fully compatible with 100k ECL level
- Address access time: HM 100470 25 ns (max)
  HM 100470-1 15 ns (max)
- Write pulse width: HM 100470
  HM 100470-1 15 ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	x	x	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	x	Dout*	Read

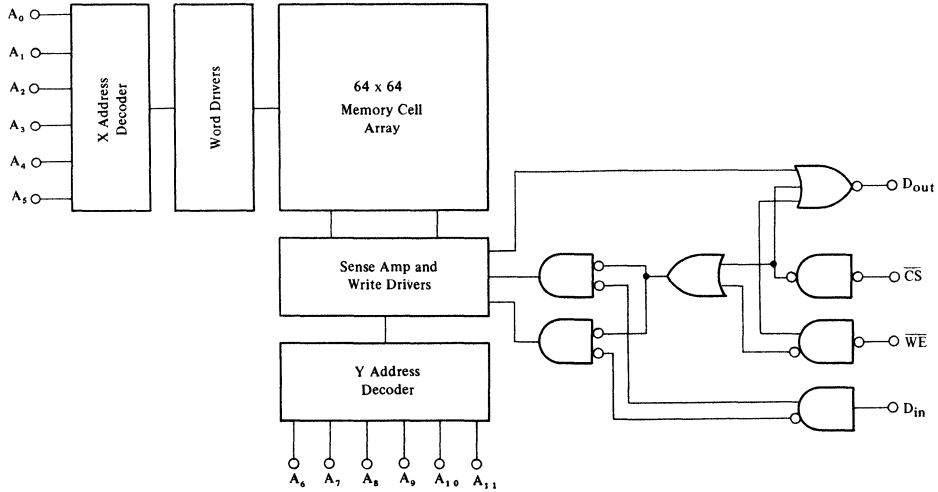
Notes : x,
*,

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



HM100474, HM100474-1

HITACHI
HLN215
LITERATURE NO.

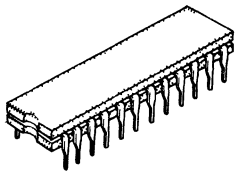
1024-word × 4-bit Fully Decoded Random Access Memory

The HM100474 is ECL 100k compatible, 1024-words x 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

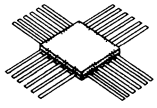
The HM100474 is encapsulated in cerdip-24pin and flat-24pin package, compatible with Fairchild's F100474.

HM100474/-1



(DG-24A)

HM100474F/-1



(FG-24)

■ FEATURES

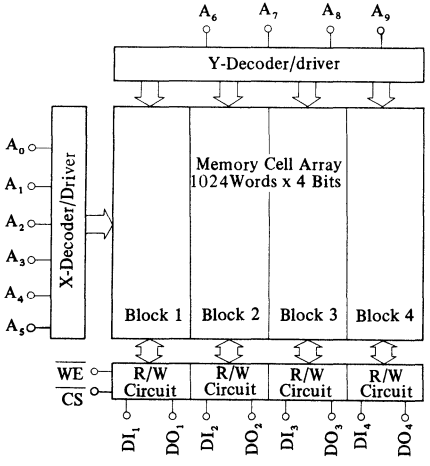
- 1024-word x 4-bit organization
- Fully compatible with 100k ECL level
- Address access time: HM 100474 25 ns (max)
  HM 100474-1 15 ns (max)
- Write pulse width: HM 100474 20 ns (min)
  HM 100474-1 15 ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

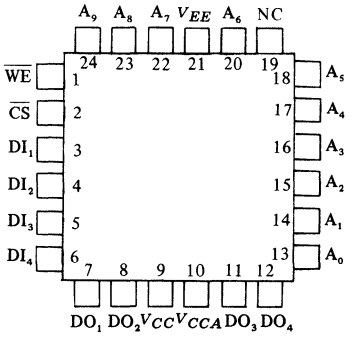
Notes : X, Irrelevant
*, Read Out Noninverted

■ BLOCK DIAGRAM



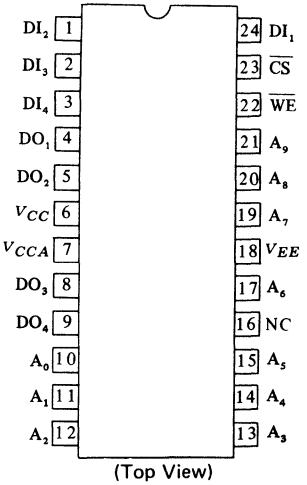
■ PIN ARRANGEMENT

HM100474F/-1



(Top View)

HM100474/-1



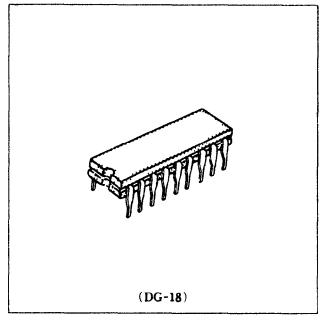
(Top View)

HN25084S, HN25085S

—Preliminary—

2048-word × 4-bit Programmable Read Only Memories

The HITACHI HN25084S and HN25085S are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit read only memories organized as 2048 words by 4 bits with on-chip address decoding and one chip enable input. The HN25084S and HN25085S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.



■ FEATURES

- 2048 words x 4 bits organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 25 ns typ. (50 ns max)
- Medium power consumption: 550 mW typ.
- One chip enable input for memory expansion
- Open collector outputs (HN25084S)/Three-state outputs (HN25085S)
- Standard cerdip 18-pin dual in-line package

■ OPERATION

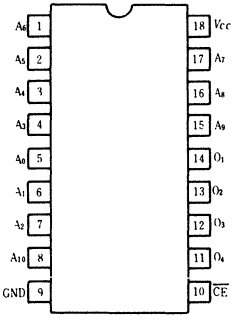
- **Programming**

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the eleven address inputs in TTL level. The device is disabled by bringing $\overline{CE}$ to a logic "one". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic "one" state, an additional pulse train is applied, then is stopped.

- **Reading**

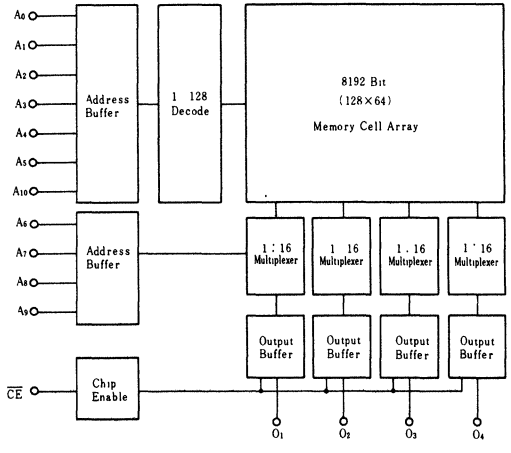
To read the memory the device is enabled by bringing $\overline{CE}$ to a logic "zero". The outputs then correspond to the data programmed in the selected word.

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



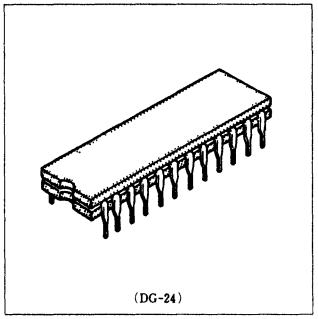
Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HN25088S, HN25089S

—Preliminary—

1024-word × 8-bit Programmable Read Only Memories

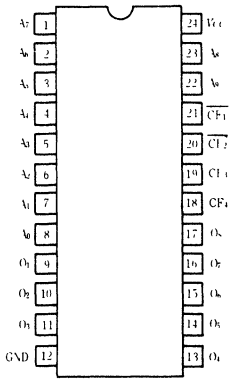
The HITACHI HN25088S and HN25089S are high speed electrically programmable, fully decoded TTL Bipolar 8192 bit-read only memories organized as 1024 words by 8 bits with on-chip address decoding and four chip enable inputs. The HN25088S and HN25089S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.


(DG-24)

■ FEATURES

- 1024 words x 8 bits organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 25 ns typ. (50 ns max)
- Medium power consumption: 600 mW typ.
- Four chip enable inputs for memory expansion
- Open collector outputs (HN25088S)/Three-state outputs (HN25089S)
- Standard cerdip 24-pin dual in-line package

■ PIN ARRANGEMENT



(Top View)

■ OPERATION

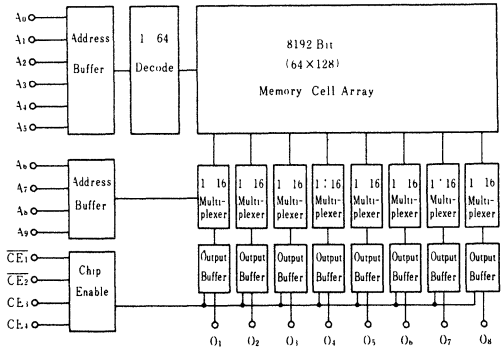
- **Programming**

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired word is selected by the ten address inputs in TTL level. The device is disabled by bringing $\overline{CE1}$ and/or $\overline{CE2}$ to as logic "one" or CE3 and/or CE4 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

- **Reading**

To read the memory the device is enabled by bringing $\overline{CE1}$ and $\overline{CE2}$ to a logic "zero", CE3 and CE4 to a logic "one". The outputs then corresponed to the data programmed in the selected word.

■ LOGIC DIAGRAM

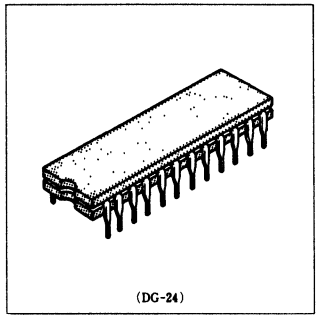


Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HN25168S, HN25169S —Preliminary—

2048-word × 8-bit Programmable Read Only Memories

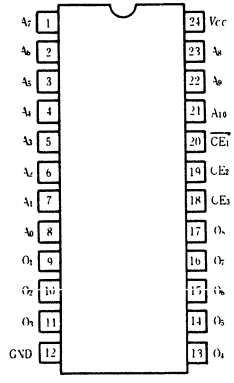
The HITACHI HN25168S and HN25169S are high speed electrically programmable, fully decoded TTL Bipolar 16384 bit read only memories organized as 2048 words by 8 bits with on-chip address decoding and three chip enable inputs. The HN25168S and HN25166S are fabricated with logic level "zeros" (low); logic level "ones" (high) can be electrically programmed in the selected bit locations. The same address inputs are used for both programming and reading.


(DG-24)

■ FEATURES

- 2048 words x 8 bits organization (fully decoded)
- DTL/TTL compatible inputs and outputs
- Fast read access time: 40 ns typ. (60 ns max)
- Medium power consumption: 600 mW typ.
- Three chip enable inputs for memory expansion.
- Open collector outputs (HN25168S)/Three-state outputs (HN25169S)
- Standard cerdip 24-pin dual in-line package

■ PIN ARRANGEMENT



(Top View)

■ OPERATION

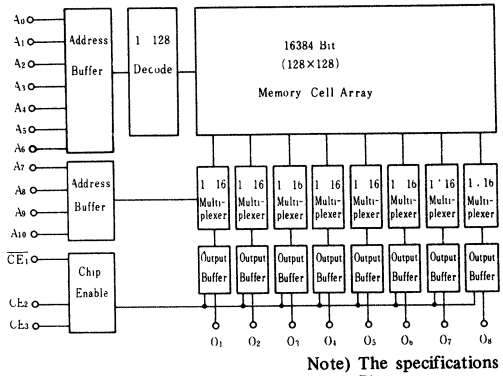
- **Programming**

A logic one can be permanently programmed into a selected bit location by using programming equipment. First, the desired world is selected by the eleven address inputs in TTL level. The device is disabled by bringing $\overline{CE1}$ to as logic "one" or CE2 and/or CE3 to a logic "zero". Then a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse is applied, then is stopped.

- **Reading**

To read the memory the device is enabled by bringing $\overline{CE1}$ to a logic "zero", CE2 and CE3 to a logic "one". The outputs then corresponed to the data programmed in the selected word.

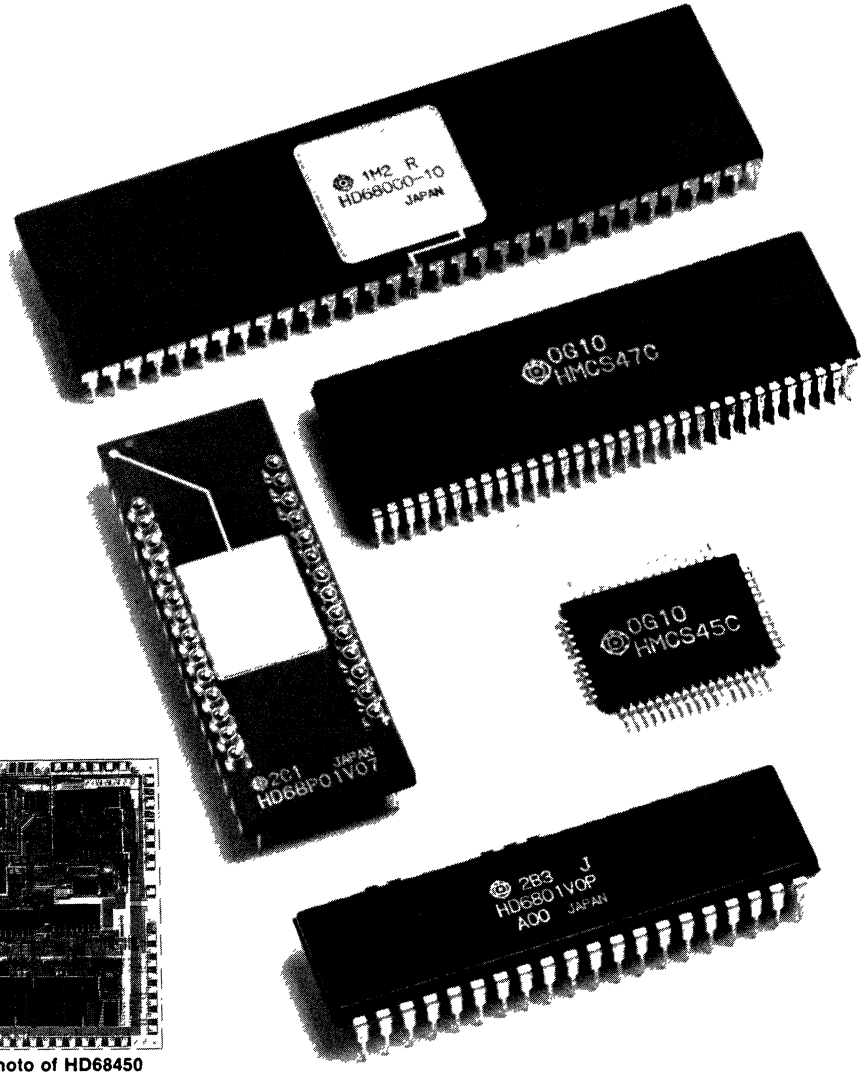
■ LOGIC DIAGRAM



Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

SECTION 3

MICROPROCESSORS



Die Photo of HD68450

HITACHI

An Unprecedented Commitment to Quality and Reliability . . .

As quality and reliability become increasingly important concerns, Hitachi continues to improve its efforts to provide the best possible product. The experience gained in shipping millions of microprocessors and peripheral LSIs for critical and demanding automotive and industrial applications is reflected in every product we sell. Each unit shipped receives 100% dynamic high-temperature burn-in, a quality assurance effort unparalleled in the semiconductor industry, and another reason why Hitachi is the Symbol of Semiconductor Quality, Worldwide.

QUALITY ASSURANCE FLOW FOR ASSEMBLY AND TEST (all microprocessor and microcomputer products):

	PROCESS	INSPECTION LEVEL	QC CRITERIA	REMARKS
1	Dicing	—	—	—
2	Chip Visual	100%	Visual	100x
3	Lot Acceptance	AQL = 0.25%*	Visual	100x
4	Die Attachment	—	—	Au-Si
5	Patrol Inspection	Once/Day/Machine	Visual	—
6	Wire Bonding	—	—	Al Ultrasonic
7	Patrol Inspection	Once/Day/Machine	Visual	
		Once/Week/Machine	Bond Dimension	
			Bond Strength	
8	Visual Inspection	100%	Visual	20x
9	Lot Acceptance	AQL = 0.25%*	Visual	20x
10	Seal	—	—	A-Sn Alloy
11	Temperature Cycle	100%	—	-55°C -25°C -150°C 10 Cycles
12	Hermeticity	100%	Fine and Gross	Hermetic Packages Only
13	Plating	—	—	Tin (Sn)
14	Lead Trim	—	—	—
15	Visual Inspection	100%	Visual	
16	Lot Acceptance	AQL = 0.25%	Visual	
17	Burn-in	100%	—	Dynamic Ta = 125°C
18	Electrical Test	100%	DC, AC, Functional	Ta = 70°C
19	Marking	—	—	
20	Electrical	100%	DC	
21	Visual Inspection	100%	External Visual	
22	Lot Acceptance	AQL = 0.25%*	Electrical	
		AQL = 0.65%	External Visual	

*Combined DC, AC and functional

HITACHI MICROPROCESSOR/PERIPHERAL CROSS REFERENCE

Hitachi is in the process of converting many microprocessor part numbers to "industry standard" generic part numbers. A complete list showing both the "old" and "new" part numbers is shown in figure 1. The use of industry standard part numbers will greatly simplify the interface between Hitachi and our customers

Beginning JULY 1, 1981, all orders should be entered using the "new" part numbers only

Note that during the conversion process, product shipped by Hitachi will be marked 1 of 2 ways (see figure 2).

1) marked with the "old" Hitachi part number ..

or

2) marked with a dual number ("old" and "new")

At the completion of the conversion (approximately JANUARY 1, 1982) all product will be shipped with the dual marking (2 above)

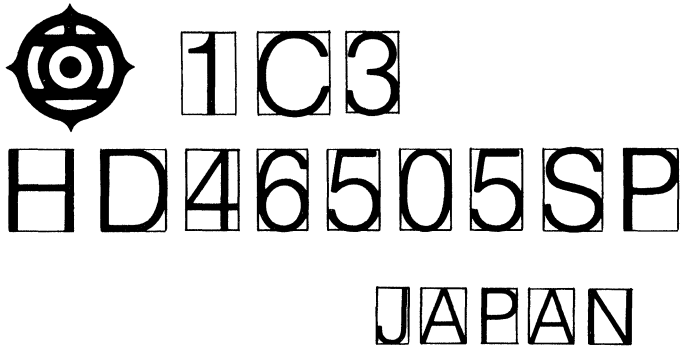
If this conversion plan poses problems, or you have any questions, please contact Hitachi Microprocessor Marketing

Description	"old" HITACHI number	"new" HITACHI number	MOTOROLA number
16/32 bit microprocessing unit, 8 mhz	——— ———	**HD68000-8**	MC68000L
16/32 bit microprocessing unit, 6 mhz	——— ———	**HD68000-6**	MC68000L6
16/32 bit microprocessing unit, 4 mhz	——— ———	**HD68000-4**	MC68000L4
8/16 bit microprocessing unit, 1mhz	HD6809P	**HD6809P**	MC6809P
8/16 bit microprocessing unit, 1.5mhz	HD68A09P	**HD68A09P**	MC68A09P
8/16 bit microprocessing unit, 2mhz	HD68B09P	**HD68B09P**	MC68B09P
8 bit microprocessing unit, 1mhz	HD46800DP	**HD6800P**	MC6800P
8 bit microprocessing unit, 1.5mhz	HD468A00P	**HD68A00P**	MC68A00P
8 bit microprocessing unit, 2mhz	HD468B00P	**HD68B00P**	MC68B00P
8 bit microprocessing unit, 1mhz with clock and 128 bytes RAM	HD46802SP	**HD6802SP**	MC6802P
8 bit microprocessing unit, 1mhz with clock and 256 bytes RAM	——— ———	**HD6802WP**	——— ———
8 bit CMOS microprocessor with I/O	——— ———	**HD6303P**	——— ———
8 bit NMOS microprocessor with I/O, 1 mhz	——— ———	**HD6803P**	MC6803P
8 bit NMOS microprocessor with I/O, 1.25 mhz	——— ———	**HD6303P-1**	MC6803P-1
8 bit microprocessing unit with clock, 1 mhz	——— ———	**HD6808SP**	MC6808P
128 x 8 static RAM, 450ns access time	HM46810P	**HM6810P**	MC6810P
128 x 8 static RAM, 360ns access time	HM468A10P	**HM68A10P**	MC68A10P
Peripheral interface adapter, 1mhz	HD46821P	**HD6821P**	MC6821P
Peripheral interface adapter, 1.5mhz	HD468A21P	**HD68A21P**	MC68A21P
Peripheral interface adapter, 2mhz	HD468B21P	**HD68B21P**	MC68B21P
Programmable timer module, 1mhz	——— ———	**HD6840P**	MC6840P
Programmable timer module, 1.5mhz	——— ———	**HD68A40P**	MC68A40P
Programmable timer module, 2mhz	——— ———	**HD68B40P**	MC68B40P
Floppy disk controller, 1mhz	HD46503SP	**HD6843SP**	MC6843P
Floppy disk controller, 1.5mhz	HD46503SP-1	**HD68A43SP**	MC68A43P
8 bit DMA controller, 1mhz	HD46504RP	**HD6844P**	MC6844P
8 bit DMA controller, 1.5mhz	HD46504RP-1	**HD68A44P**	MC68A44P
8 bit DMA controller, 2mhz	HD46504RP-2	**HD68B44P**	MC68B44P
CRT controller, 1mhz	HD46505RP	**HD6845RP**	MC6845P
CRT controller, 1.5mhz	HD46505RP-1	**HD68A45RP**	MC68A45P
CRT controller, 2mhz	HD46505RP-2	**HD68B45RP**	MC68B45P
CRT controller (enhanced), 1 mhz	HD46505SP	**HD6845SP**	——— ———
CRT controller (enhanced), 1.5mhz	HD46505SP-1	**HD68A45SP**	——— ———
CRT controller (enhanced), 2mhz	HD46505SP-2	**HD68B45SP**	——— ———
ROM, I/O, Timer combo, 1mhz	——— ———	**HD6846P**	MC6846P
Asynchronous comm interface, 1mhz	HD46850P	**HD6850P**	MC6850P
Asynchronous comm interface, 1.5mhz	HD468A50P	**HD68A50P**	MC68A50P
Synchronous comm interface, 1mhz	HD46852P	**HD6852P**	MC6852P
Synchronous comm interface, 1.5mhz	HD468A52P	**HD68A52P**	MC68A52P
Analog data acquisition unit, 1mhz	HD46508P	**HD46508P**	——— ———
Analog data acquisition unit, 1.5mhz	HD46508P-1	**HD46508P-1**	——— ———
Analog data acquisition unit, 1mhz (enhanced)	HD46508PA	**HD46508PA**	——— ———
Analog data acquisition unit, 1.5mhz (enhanced)	HD46508PA-1	**HD46508PA-1**	——— ———
CMOS real time clock with RAM	——— ———	**HD146818P**	MC146818P

Figure 1. Hitachi Microprocessor/Peripheral Cross Reference

NEW HITACHI MICROPROCESSOR NUMBERING SYSTEM

(a) Present marking



(b) New marking

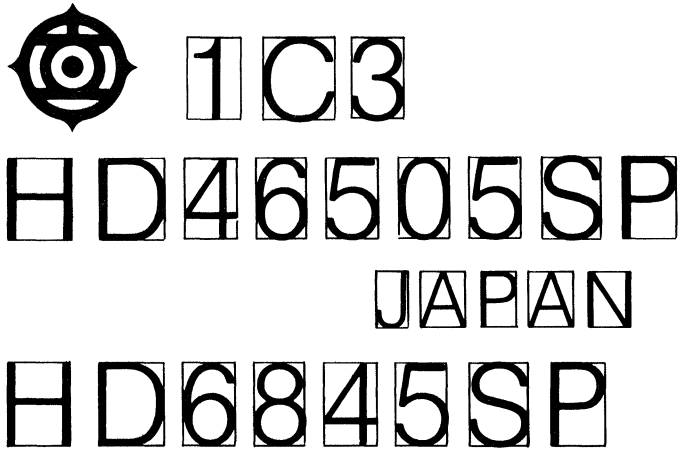


Figure 2.

HD6800, HD68A00, HD68B00

HITACHI
HLN001
LITERATURE NO.

MPU (Micro Processing Unit)

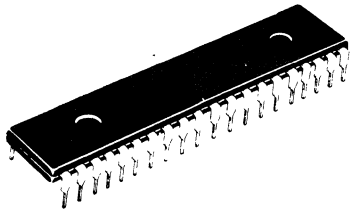
The HD6800 is a monolithic 8-bit microprocessor forming the central control function for Hitachi's HMCS6800 family. Compatible with TTL, the HD6800 as with all HMCS6800 system parts, requires only one 5V power supply, and no external TTL devices for bus interface. The HD68A00 and HD68B00 are high speed versions.

The HD6800 is capable of addressing 65K bytes of memory with its 16-bit address lines. The 8-bit data bus is bi-directional as well as 3-state, making direct memory addressing and multiprocessing applications realizable.

■ FEATURES

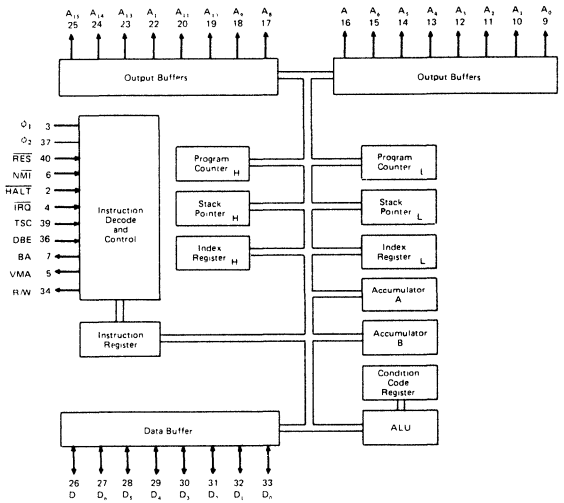
- Versatile 72 Instruction – Variable Length (1~3 Byte)
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- Maskable Interrupt
- Separate Non-Maskable Interrupt – Internal Registers Saved in Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Accessing (DMA) and Multiple Processor Capability
- Clock Rates as High as 2.0 MHz (HD6800 ··· 1 MHz, HD68A00 ··· 1.5 MHz, HD68B00 ··· 2.0 MHz)
- Halt and Single Instruction Execution Capability
- Compatible with MC6800, MC68A00 and MC68B00

HD6800P, HD68A00P, HD68B00P

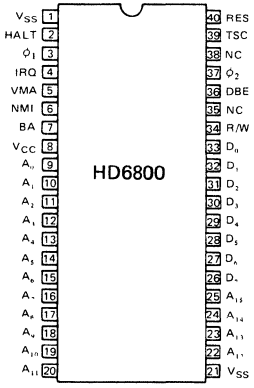


(DP-40)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HD6802

HITACHI
HLN003
LITERATURE NO.

MPU (Microprocesssor with Clock and RAM)

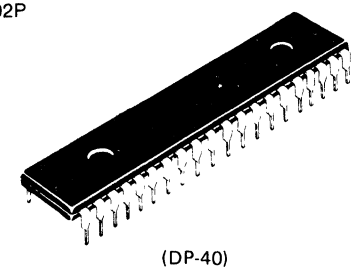
The HD6802 is a monolithic 8-bit microprocessor that contains all the registers and accumulators of the present HD6800 plus an internal clock oscillator and driver on the same chip. In addition, the HD6802 has 128 bytes of RAM on the chip located at hex addresses 0000 to 007F. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation.

The HD6802 is completely software compatible with the HD6800 as well as the entire HMCS6800 family of parts. Hence, the HD6802 is expandable to 65K words.

■ FEATURES

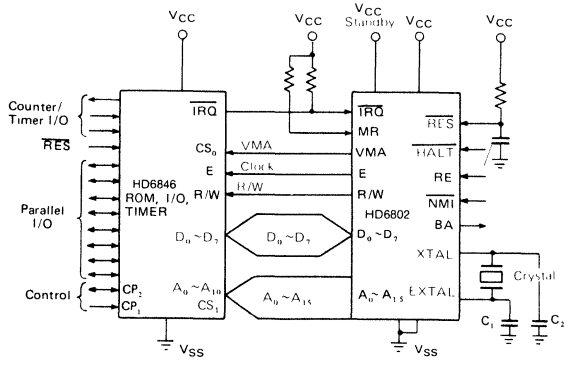
- On-Chip Clock Circuit
- 128 × 8 Bit On-Chip RAM
- 32 Bytes of RAM are Retainable
- Software-Compatible with the HD6800
- Expandable to 65K words
- Standard TTL-Compatible Inputs and Outputs
- 8 Bit Word Size
- 16 Bit Memory Addressing
- Interrupt Capability
- Compatible with MC6802

HD6802P

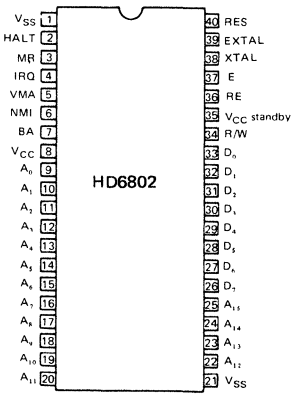


(DP-40)

■ MINIMUM SYSTEM



■ PIN ARRANGEMENT



(Top View)

HD6802W

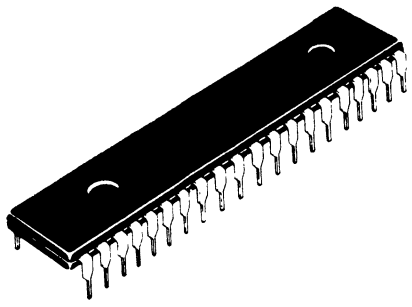
MPU (Microprocessor with Clock and RAM)

HD6802W is the enhanced version of HD6802 which contains MPU, clock and 256 bytes RAM. Internal RAM has been extended from 128 to 256 bytes to increase the capacity of system read/write memory for handling temporary data and manipulating the stack.

The internal RAM is located at hex addresses 0000 to 00FF. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation.

The HD6802W is completely software compatible with the HD6800 as well as the entire HMCS6800 family of parts. Hence, the HD6802W is expandable to 65k words.

HD6802WP

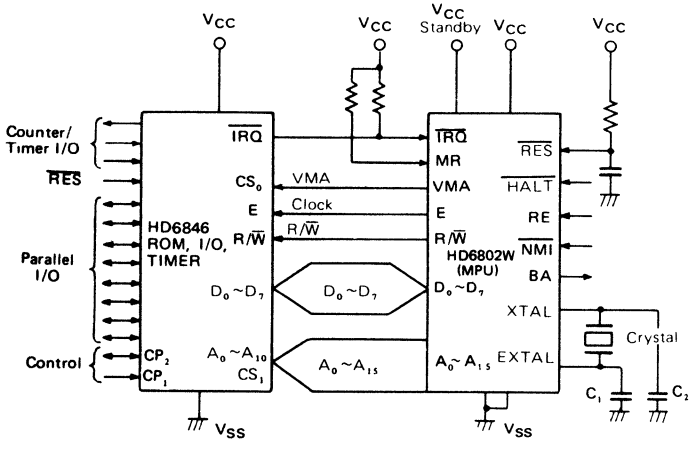


(DP-40)

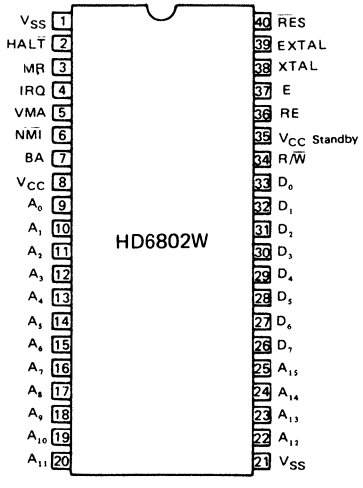
■ FEATURES

- On-Chip Clock Circuit
- 256 × 8 Bit On-Chip RAM
- 32 Bytes of RAM are Retainable
- Software-Compatible with the HD6800, HD6802
- Expandable to 65k words
- Standard TTL-Compatible Inputs and Outputs
- 8 Bit Word Size
- 16 Bit Memory Addressing
- Interrupt Capability

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



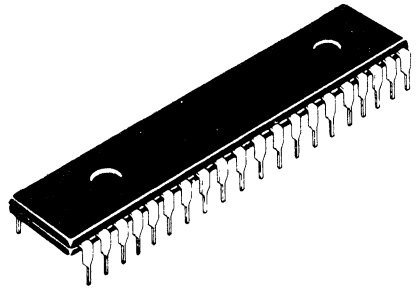
(Top View)

HD6303, HD63A03, HD63B03

CMOS MPU (Microprocessing Unit)
ADVANCE INFORMATION

The HD6303 is an 8-bit CMOS micro processing unit which has the completely compatible instruction set with the HD6301V0. 128 bytes RAM, Serial Communication Interface (SCI), parallel I/O terminals as well as three functions of timer on-chip are incorporated in the HD6303. It is bus compatible with HMCS6800 and can be expanded up to 65k words. Like the HMCS6800 family, I/O level is TTL compatible with +5.0V single power supply. As the HD6303 is CMOS MPU, power dissipation is extremely low. And also Sleep Mode and Stand-By Mode which the HD6303 has for low power dissipation make lower power application possible.

HD6303P
HD63A03P
HD63B03P

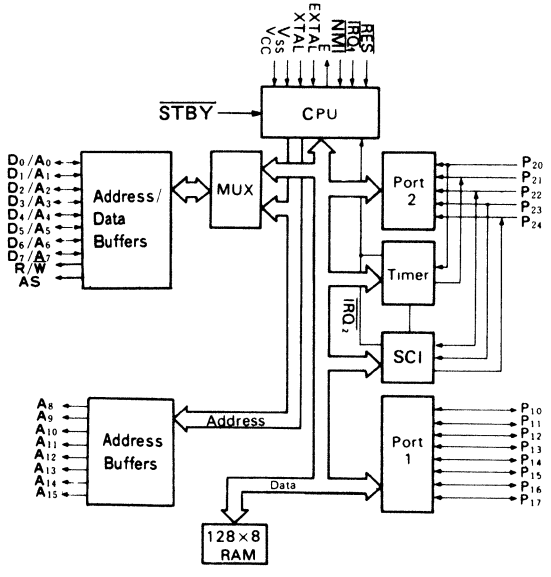


(DP-40)

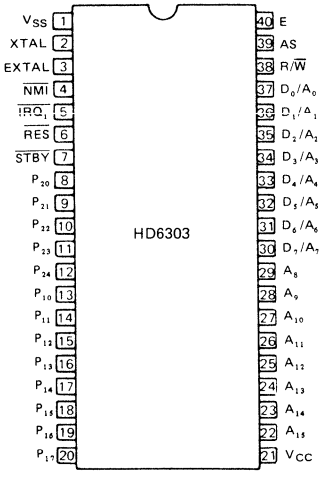
■ FEATURES

- Object Code Upward Compatible with the HD6800, HD6802, HD6801
- Abundant On-Chip Functions Compatible with the HD6301V0; 128 Bytes RAM, 13 Parallel I/O Lines (including Timer, SCI I/O Terminals), 16-bit Timer, Serial Communication Interface (SCI)
- Low Power Consumption Mode; Sleep Mode, Stand-By Mode
- Minimum Instruction Cycle Time
  1μs (f=1MHz), 0.67μs (f=1.5MHz), 0.5μs (f=2.0MHz)
- Bit Manipulation, Bit Test Instruction
- Error Detecting Function; Address Trap, Op Code Trap
- Up to 65k Words Address Space

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TYPE OF PRODUCTS

Type No.	Bus Timing
HD6303	1.0 MHz
HD63A03	1.5 MHz
HD63B03	2.0 MHz

HD6809, HD68A09, HD68B09

HITACHI
HLN005
LITERATURE NO.

MPU (Micro Processing Unit)

The HD6809 is a revolutionary high performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the HMCS6800 family has major architectural improvements which include additional registers, instructions and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The HD6809 has the most complete set of addressing modes available on any 8-bit microprocessor today.

The HD6809 has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications.

HD46800D COMPATIBLE

- Hardware — Interfaces with All HMCS6800 Peripherals
- Software — Upward Source Code Compatible Instruction Set and Addressing Modes

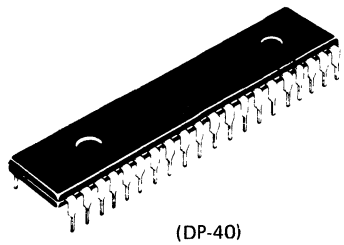
■ ARCHITECTURAL FEATURES

- Two 16-bit Index Registers
- Two 16-bit Indexable Stack Pointers
- Two 8-bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

■ HARDWARE FEATURES

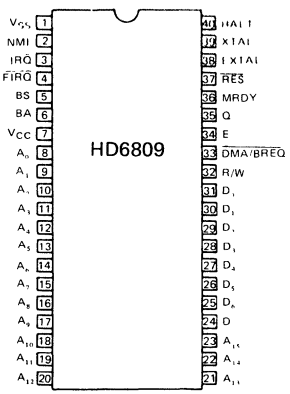
- On Chip Oscillator
- $\overline{\text{DMA/BREQ}}$ Allows DMA Operation or Memory Refresh
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- MRDY Input Extends Data Access Times for Use With Slow Memory
- Interrupt Acknowledge Output Allows Vectoring By Devices
- SYNC Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle RESET
- Single 5-Volt Supply Operation
- NMI Blocked After RESET Until After First Load of Stack Pointer
- Early Address Valid Allows Use With Slower Memories
- Early Write-Data for Dynamic Memories
- Compatible with MC6809, MC68A09 and MC68B09

HD6809P, HD68A09P, HD68B09P



(DP-40)

■ PIN ARRANGEMENT



■ SOFTWARE FEATURES

- 10 Addressing Modes
  - HMCS6800 Upward Compatible Addressing Modes
  - Direct Addressing Anywhere in Memory Map
  - Long Relative Branches
  - Program Counter Relative
  - True Indirect Addressing
  - Expanded Indexed Addressing:

HD6809E, HD68A09E, HD68B09E

MPU (Microprocessing Unit) PRELIMINARY

The HD6809E is a revolutionary high performance 8-bit microprocessor which supports modern programming techniques such as position independence, reentrancy, and modular programming.

This third-generation addition to the HMCS6800 family has major architectural improvements which include additional registers, instructions and addressing modes.

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The HD6809E has the most complete set of addressing modes available on any 8-bit microprocessor today.

The HD6809E has hardware and software features which make it an ideal processor for higher level language execution or standard controller applications. External clock inputs are provided to allow synchronization with peripherals, systems or other MPUs.

HD6800 COMPATIBLE

- Hardware — Interfaces with All HMCS6800 Peripherals
- Software — Upward Source Code Compatible Instruction Set and Addressing Modes

■ **ARCHITECTURAL FEATURES**

- Two 16-bit Index Registers
- Two 16-bit Indexable Stack Pointers
- Two 8-bit Accumulators can be Concatenated to Form One 16-Bit Accumulator
- Direct Page Register Allows Direct Addressing Throughout Memory

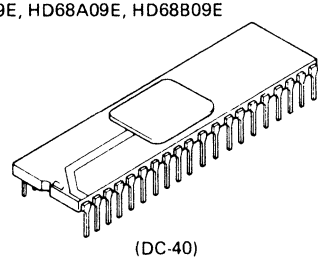
■ **HARDWARE FEATURES**

- External Clock Inputs, E and Q, Allow Synchronization
- TSC Input Controls Internal Bus Buffers
- LIC Indicates Opcode Fetch
- AVMA Allows Efficient Use of Common Resources in A Multiprocessor System
- BUSY is a Status Line for Multiprocessing
- Fast Interrupt Request Input Stacks Only Condition Code Register and Program Counter
- Interrupt Acknowledge Output Allows Vectoring By Devices
- SYNC Acknowledge Output Allows for Synchronization to External Event
- Single Bus-Cycle RESET
- Single 5-Volt Supply Operation
- NMI Blocked After RESET Until After First Load of Stack Pointer
- Early Address Valid Allows Use With Slower Memories
- Early Write-Data for Dynamic Memories

■ **SOFTWARE FEATURES**

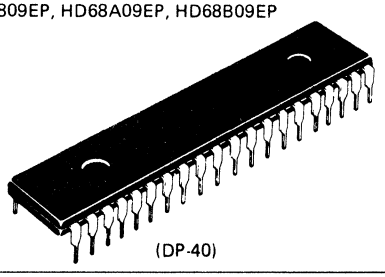
- 10 Addressing Modes
  - HMCS6800 Upward Compatible Addressing Modes
  - Direct Addressing Anywhere in Memory Map
  - Long Relative Branches
  - Program Counter Relative
  - True Indirect Addressing
  - Expanded Indexed Addressing
    - 0, 5, 8, or 16-bit Constant Offsets
    - 8, or 16-bit Accumulator Offsets
    - Auto-Increment/Decrement by 1 or 2
- Improved Stack Manipulation
- 1464 Instruction with Unique Addressing Modes
- 8 x 8 Unsigned Multiply
- 16-bit Arithmetic

HD6809E, HD68A09E, HD68B09E



(DC-40)

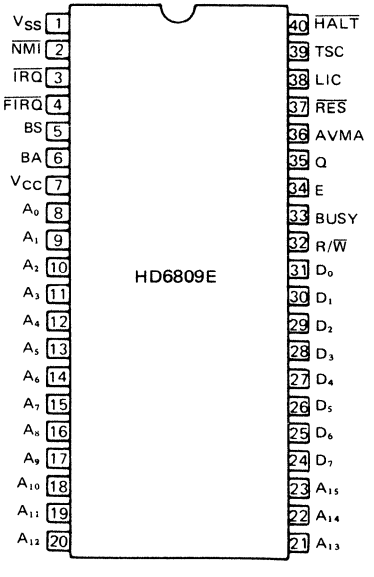
HD6809EP, HD68A09EP, HD68B09EP



(DP-40)

- Transfer/Exchange All Registers
- Push/Pull Any Registers or Any Set of Registers
- Load Effective Address

■ **PIN ARRANGEMENT**



(Top View)

HD6821, HD68A21, HD68B21

HITACHI
HLN006
LITERATURE NO.

PIA (Peripheral Interface Adapter)

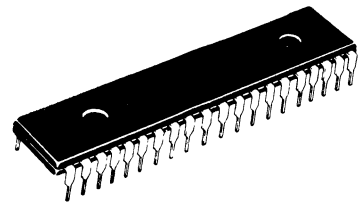
The HD6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the HD6800 Microprocessing Unit(MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bi-directional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

■ FEATURES

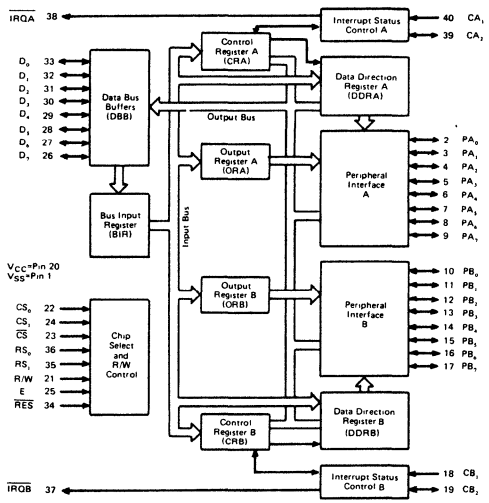
- Two Bi-directional 8-Bit Peripheral Data Bus for interface to Peripheral devices
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- N Channel Silicon Gate MOS
- Compatible with MC6821, MC68A21 and MC68B21

HD6821P, HD68A21P, HD68B21P

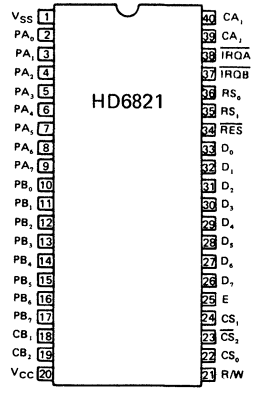


(DP-40)

■ BLOCK DIATRAM



■ PIN ARRANGEMENT



(Top View)

HD6840, HD68A40, HD68B40

HITACHI
HLN008
LITERATURE NO.

PTM (Programmable Timer Module)

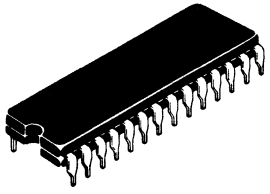
The HD6840 is a programmable subsystem component of the HMCS6800 family designed to provide variable system time intervals.

The HD6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The HD6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

■ FEATURES

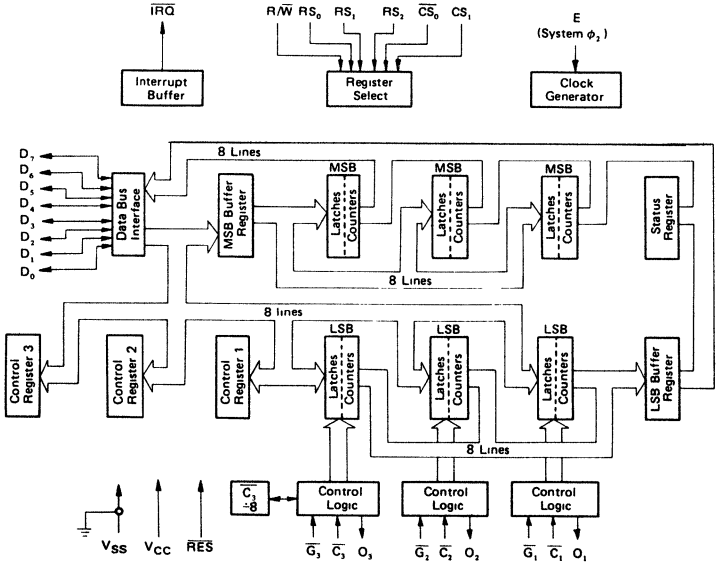
- Operates from a Single 5 Volts Power Supply
- Fully TTL Compatible
- Single System Clock Required (E)
- Selectable Prescaler on Timer 3 Capable of 4 MHz for the HD6840, 6 MHz for the HD68A40 and 8 MHz for the HD68B40
- Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- Readable Down Counter Indicates Counts to Go to Time-Out
- Selectable Gating for Frequency or Pulse-Width Comparison
- $\overline{RES}$ Input
- Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
- Three Maskable Outputs

HD6840P, HD68A40P, HD68B40P

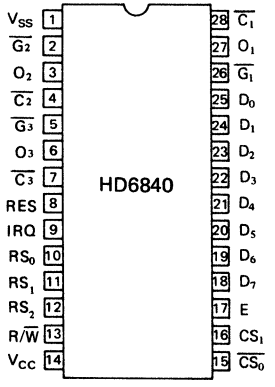


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HD6843S, HD68A43S

HITACHI
HLN010
LITERATURE NO.

FDC (Floppy Disk Controller)

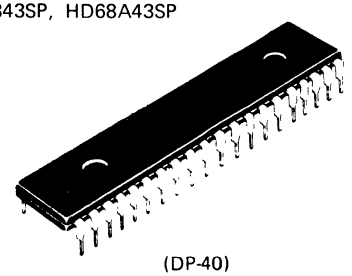
The HD6843SP Floppy Disk Controller performs the complex MPU/Floppy interface function. The FDC was designed to optimize the balance between the "Hardware/Software" in order to achieve integration of all key functions and maintain flexibility.

The FDC can interface a wide range of drives with a minimum of external hardware. Multiple drives can be controlled with the addition of external multiplexing rather than additional FDC's.

■ FEATURES

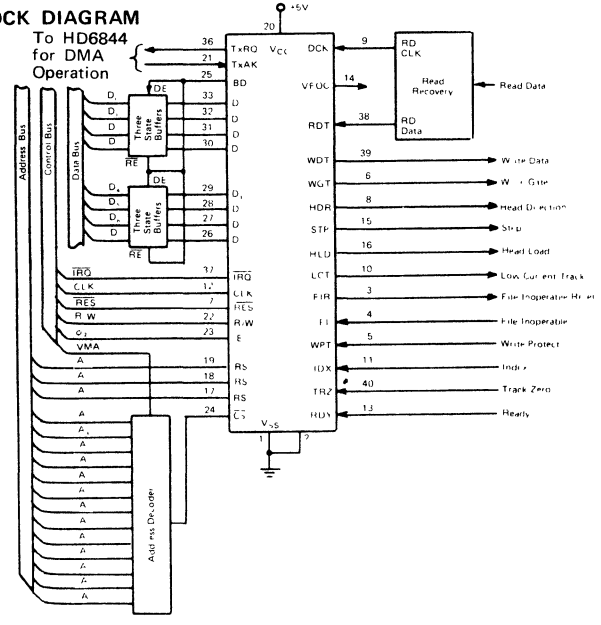
- Format compatible with IBM3740
- User Programmable read/write format
- Ten powerful macro-commands
- Macro End Interrupt allows parallel processing of MPU and FDC
- Controls multiple Floppies with external multiplexing
- Direct interface with HMCS6800
- Programmable seek and settling times enable operation with a wide range of Floppy drives
- Offers both Programmed Controlled I/O (PCIO) and DMA data transfer mode
- Free-Format read or write
- Single 5-volt power supply
- All registers directly accessible
- Compatible with MC6843

HD6843SP, HD68A43SP

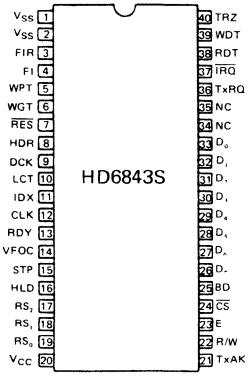


(DP-40)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HD6844P, HD68A44P

HITACHI
HLN011
LITERATURE NO.

DMAC (Direct Memory Access Controller)

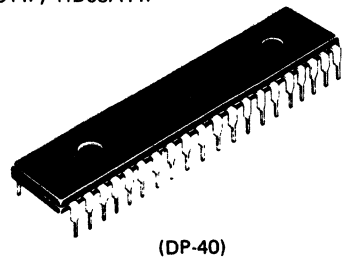
The HD6844 Direct Memory Access Controller (DMAC) performs the function of transferring data directly between memory and peripheral device controllers. It controls the address and data buses in place of the MPU in bus organized systems such as the HMCS6800 Microprocessor System.

The bus interface of the HD6844 includes select, read/write, interrupt, transfer request/grant, and bus interface logic to allow the data transfer over an 8-bit bidirectional data bus. The functional configuration of the DMAC is programmed via the data bus. The internal structure provides for control and handling of four individual channels, each of which is separately configured. Programmable control registers provide control for the transfer location and length, individual channel control and transfer mode configuration, priority of servicing, data chaining, and interrupt control. Status and control lines provide control to the peripheral controllers.

The mode of transfer for each channel can be programmed as cycle-stealing or a burst transfer mode.

Typical applications would be with the Floppy Disk Controller (FDC), etc..

HD6844P, HD68A44P

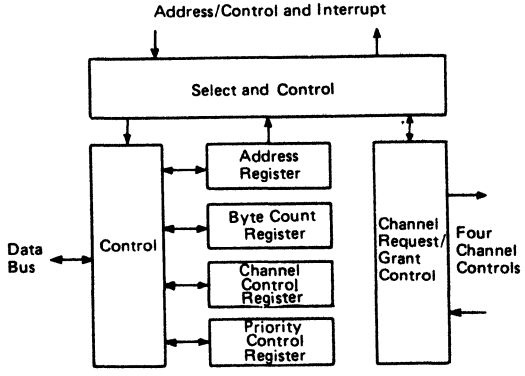


(DP-40)

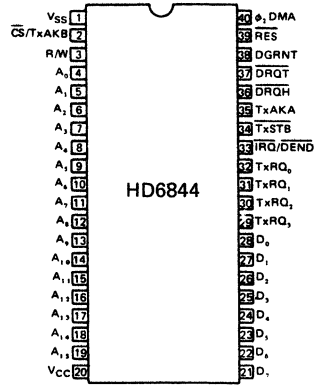
■ FEATURES

- Four DMA Channels, Each Having a 16-Bit Address Register and a 16-Bit Byte Count Register
- 1 M Byte/Sec (HD6844P), 1.5 M Byte/Sec (HD68A44P) Maximum Data Transfer Rate
- Selection of Fixed or Rotating Priority Service Control
- Separate Control Bits for Each Channel
- Data Chain Function
- Address Increment or Decrement Update
- Programmable Interrupts and DMA End to Peripheral Controllers
- Compatible with MC6844

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HD6845S, HD68A45S, HD68B45S

HITACHI
HLN013
LITERATURE NO.

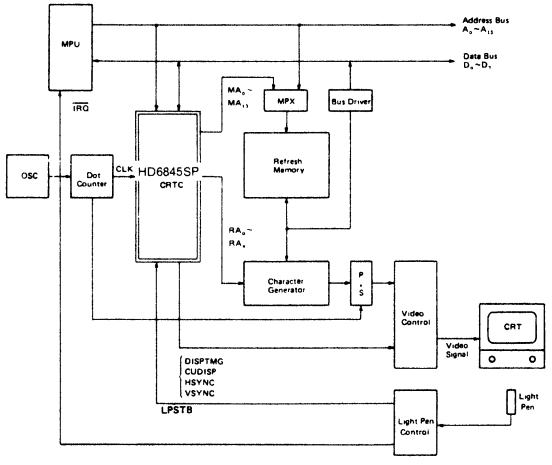
CRTC (CRT Controller)

The CRTC is a LSI controller which is designed to provide an interface for microcomputers to raster scan type CRT displays. The CRTC belongs to the HMCS6800 LSI Family and has full compatibility with MPU in both data lines and control lines. Its primary function is to generate timing signal which is necessary for raster scan type CRT display according to the specification programmed by MPU. The CRTC is also designed as a programmable controller, so applicable to wide-range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

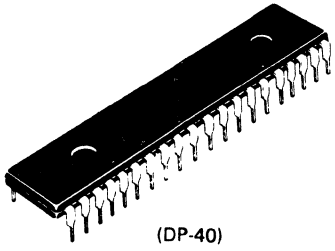
■ FEATURES

- Number of Displayed Characters on the Screen, Vertical Dot Format of One Character, Horizontal and Vertical Sync Signal, Display Timing Signal are Programmable
- 3.7 MHz High Speed Display Operation
- Line Buffer-less Refreshing
- 14-bit Refresh Memory Address Output (16k Words max. Access)
- Programmable Interlace/Non-interlace Scan Mode
- Built-in Cursor Control Function
- Programmable Cursor Height and its Blink
- Built-in Light Pen Detection Function
- Paging and Scrolling Capability
- TTL Compatible
- Single +5V Power Supply
- Upward compatible with MC6845

■ SYSTEM BLOCK DIAGRAM

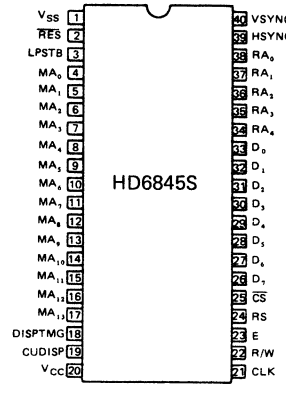


HD6845SP, HD68A45SP, HD68B45SP



(DP-40)

■ PIN ARRANGEMENT



(Top View)

■ ORDERING INFORMATION

CRTC	Bus Timing	CRT Display Timing
HD6845SP	1.0 MHz	3.7 MHz max.
HD68A45SP	1.5 MHz	
HD68B45SP	2.0 MHz	

COMBO (Combination ROM I/O Timer)

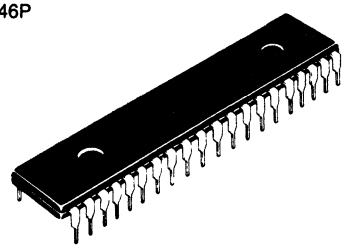
The HD6846 combination chip provides the means, in conjunction with the HD6802, to develop a basic 2-chip microcomputer system. The HD6846 consists of 2048 bytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable timer-counter.

This device is capable of interfacing with the HD6802 (basic HD6800, clock and 128 bytes of RAM) as well as the HD6800 if desired. No external logic is required to interface with most peripheral devices.

■ FEATURES

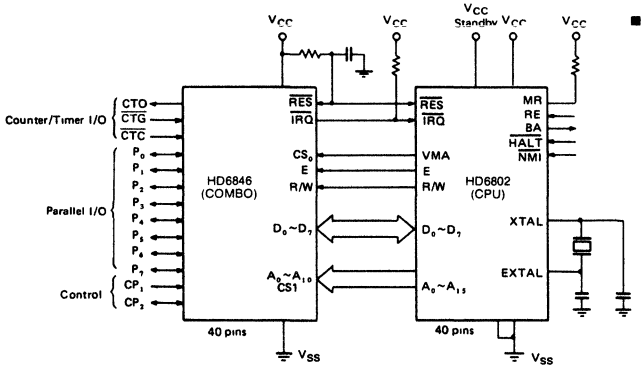
- 2048 8-Bit Bytes of Mask-Programmable ROM
- 8-Bit Bidirectional Data Port for Parallel Interface plus Two Control Lines
- Programmable Interval Timer-Counter Functions
- Programmable I/O Peripheral Data, Control and Direction Registers
- Compatible with the Complete HMCS6800 Microcomputer Product Family
- TTL-Compatible Data and Peripheral Lines
- Single 5-Volt Power Supply
- Compatible with MC6846

HD6846P



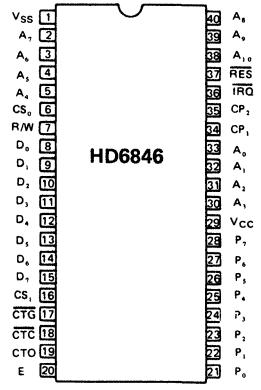
(DP-40)

■ TYPICAL MICROCOMPUTER



This is a block diagram of a typical cost effective microcomputer The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip It is not intended that this system be limited to this function but that it be expandable with other parts in the HMCS6800 Microcomputer family.

■ PIN ARRANGEMENT



(Top View)

HD6850, HD68A50

HITACHI
HLN015
LITERATURE NO.

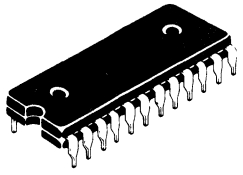
ACIA (Asynchronous Communication Interface Adapter)

The HD6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the HMCS6800 Microprocessing Unit.

The bus interface of the HD6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking.

The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation three control lines are provided.

HD6850P, HD68A50P

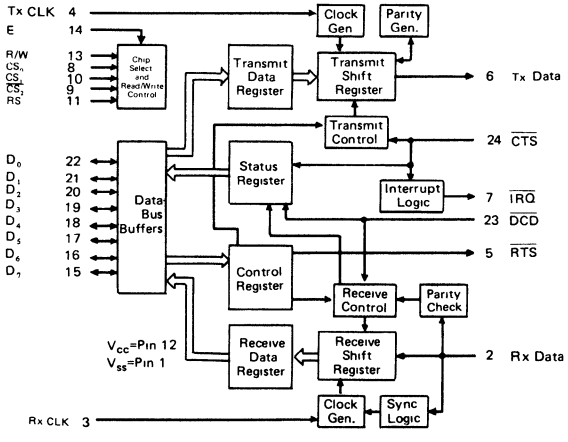


(DP-24)

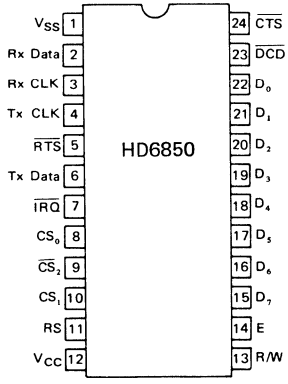
■ FEATURES

- Serial/Parallel Conversion of Data
- Eight and Nine-bit Transmission
- Insertion and Deleting of Start and Stop Bit
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Peripheral/Modem Control Functions (Clear to Send $\overline{CTS}$, Request to Send $\overline{RTS}$, Data Carier Detect $\overline{DCD}$)
- Optional ÷ 1, ÷ 16, and ÷ 64 Clock Modes
- Up to 500kbps Transmission
- Programmable Control Register
- N-channel Silicon Gate Process
- Compatible with MC6850 and MC68A50

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HD6852, HD68A52

HITACHI
HLN016
LITERATURE NO

SSDA (Synchronous Serial Data Adapter)

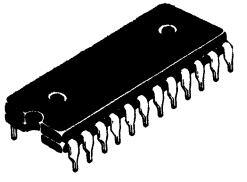
The HD6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the HMCS6800 Microprocessor systems.

The bus interface of the HD6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization.

Programmable control registers provide control for variable word length, transmit control, receive control, synchronization control and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include data communications terminals, floppy disk controllers, cassette or cartridge tape controllers and numerical control systems.

HD6852P, HD68A52P

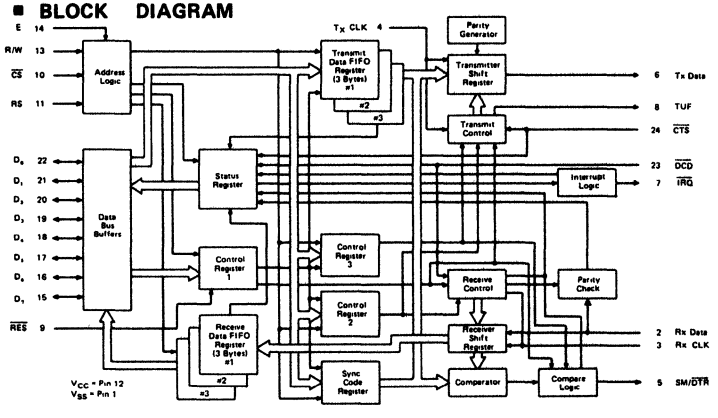


(DP-24)

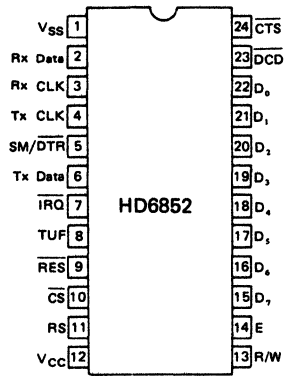
■ FEATURES

- Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- Character Synchronization on One or Two Sync Codes
- External Synchronization Available for Parallel-Serial Operation
- Programmable Sync Code Register
- Up to 600kbps Transmitter
- Peripheral/Modem Control Functions
- Three Bytes of FIFO Buffering on Both Transmit and Receive
- 6, 7, or 8 Bit Data Transmission
- Optional Even and Odd Parity
- Parity, Overrun, and Underflow Status
- Compatible with MC6852 and MC68A52

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HD146818

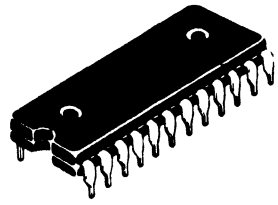
RTC (Real Time Clock plus RAM) PRELIMINARY

The HD146818 is a HMCS6800 peripheral CMOS device which combines three unique features: a complete time-of-day clock with alarm and one hundred calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of Low-power static RAM.

This device includes HD6801, HD6301 multiplexed bus interface circuit and 8085's multiplexed bus interface as well, so it can be directly connected to HD6801, HD6301 and 8085.

The Real-Time Clock plus RAM has two distinct uses. First, it is designed as battery powered CMOS part including all the common battery backed-up functions such as RAM, time, and calender. Secondly, the HD146818 may be used with a CMOS microprocessor to relieve the software of timekeeping work-load and to extend the available RAM of an MPU such as the HD6301.

HD146818P

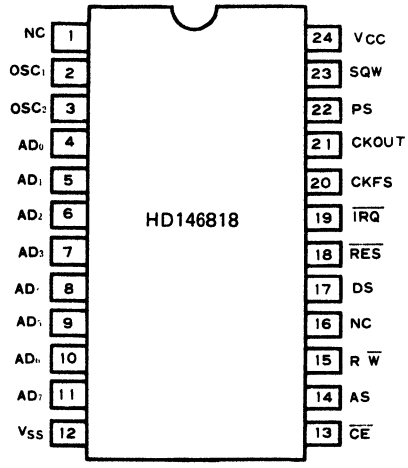


(DP-24)

■ FEATURES

- Time-of-Day Clock and Calendar
  - Counts Seconds, Minutes, and Hours of the Day
  - Counts Days of Week, Date, Month, and Year
- Binary or BCD Representation of Time, Calendar, and Alarm
- 12- or 24 Hour Clock with AM and PM in 12-Hour Mode
- Automatic End of Month Recognition
- Automatic Leap Year Compensation
- Interfaced with Software as 64 RAM Locations
  - 14 Bytes of Clock and Control Register
  - 50 Bytes of General Purpose RAM
- Three Interrupt are Separately Software Maskable and Test-able
  - Time-of-Day Alarm, Once-per-Second to Once-per-Day
  - Periodic Rates from 30.5μs to 500ms
  - End-of-Clock Update Cycle
- Programmable Square-Wave Output Signal
- Three Time Base Input Options
  - 4.194304 MHz
  - 1.048576 MHz
  - 32.768 kHz
- Clock Output May be used as Microprocessor Clock Input
  - At Time Base Frequency ÷4 or ÷1
- Multiplexed Bus Interface Circuit of HD6801, HD6301 and 8085
- Low-Power, High-Speed, High-Density CMOS
- Motorola MC146818 Compatible

■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} *	-0.3 ~ +7.0	V
Input Voltage	V_{in} *	-0.3 ~ +7.0	V
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

(NOTE) Permanent LSI damage may occur if maximum rating are exceeded. Normal operation should be under recomended operating condition. If these conditions are exceeded, it could affect reliability of LSI.

HD46508, HD46508-1

HITACHI
HLN018
LITERATURE NO.

ADU (Analog Data Acquisition Unit) PRELIMINARY

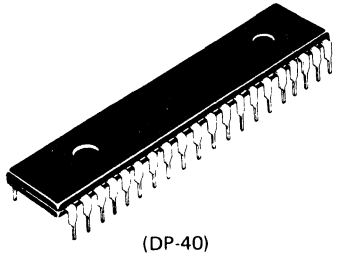
The HD46508 is a monolithic NMOS device with a 10-bit analog-to-digital converter, a programmable voltage comparator, a 16-channel analog multiplexer and HMCS6800 microprocessor family compatible interface.

Each of 16 analog inputs is either converted to a digital data by the analog-to-digital converter or compared with the specified value by the programmable comparator. The analog-to-digital converter uses successive approximation method as the conversion technique. It's intrinsic resolution is 10 bits but it can be 8 bits if the programmer so desires. The programmable voltage comparator compares the input voltage with the value specified by the programmer. The result (greater than, or smaller than) is reflected to the flag in the status register.

The device can expand its capability by controlling the external circuits such as sample holder, pre-amplifier and external multiplexer.

With these features, this device is ideally suited to applications such as process control, machine control and vehicle control.

HD46508P, HD46508P-1, HD46508PA, HD46508PA-1

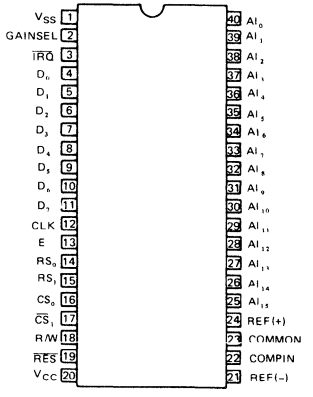


(DP-40)

■ FEATURES

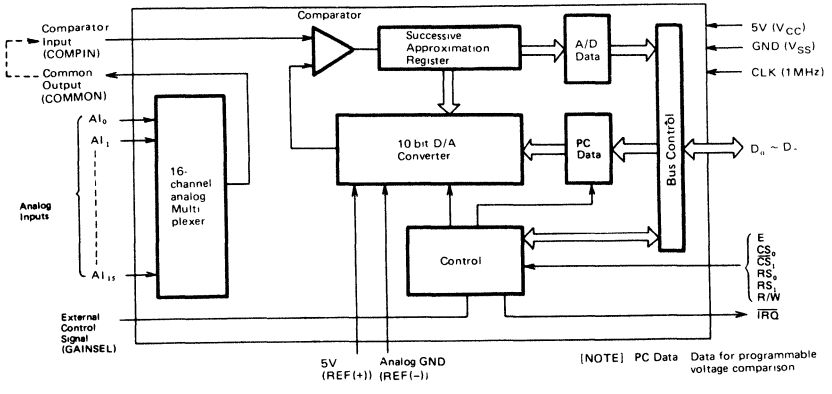
- 16-channel Analog multiplexer
- Programmable A/D Converter resolution (10-bit or 8-bit)
- Programmable Voltage comparison (PC)
- Conversion Time 100μs (A/D), 13μs(PC)
- External Sample and Hold Circuit Control
- Auto Range-switching Control of External Amplifier
- Waiting Function for the Settling Time of External Amplifier
- Interrupt Control (Only for A/D conversion)
- Single +5V Power Supply
- Compatible with HMCS6800 Bus (The connection with other Asynchronous Buses possible)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ORDERING INFORMATION

ADU	Bus Timing	Non Linearity*
HD46508PA	1 MHz	±1 LSB
HD46508PA-1	1.5 MHz	
HD46508P	1 MHz	±3 LSB
HD46508P-1	1.5 MHz	

* Specification for 10 bit A/D conversion

HD68000

HITACHI
HLN022
LITERATURE NO.

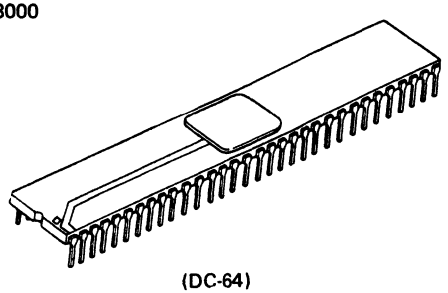
MPU (Micro Processing Unit) PRELIMINARY

Advances in semiconductor technology have provided the capability to place on a singie silicon chip a microprocessor at least an order of magnitude higher in performance and circuit complexity than has been previously available. The HD68000 is one of such VLSI microprocessors. It combines state-of-the-art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessor.

The resources available to the HD68000 user consist of the following.

As shown in the programming model, the HD68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0-A6) and the system stack pointer may be used as software stack pointers and base address registers. In addition, these registers may be used for word and long word address operations. All 17 registers may be used as index registers.

HD68000

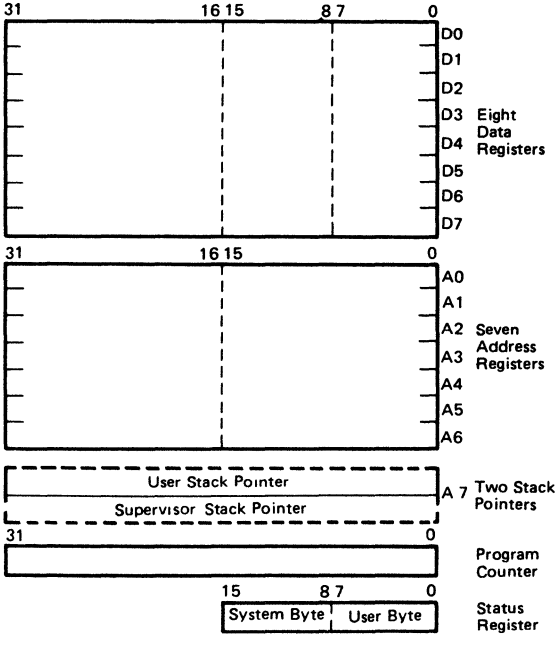


(DC-64)

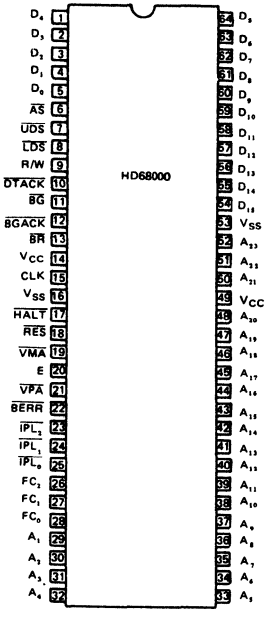
■ FEATURES

- 32-Bit Data and Address Registers
- 16 Megabyte Direct Addressing Range
- 56 Powerful Instruction Types
- Operations on Five Main Data Types
- Memory Mapped I/O
- 14 Addressing Modes
- Compatible with MC68000L

■ PROGRAMMING MODEL



■ PIN ARRANGEMENT



(Top View)

These information and specification are subject to change without notice.

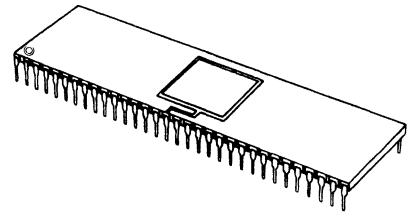
DMAC (Direct Memory Access Controller)
ADVANCE INFORMATION

HD68450 is a DMA Controller for the HMCS68000 16-bit microprocessor system. Increasingly large amounts of data are being processed by the 16-bit microprocessor systems and, consequently, the ability to transfer large amounts of data in a large memory space becomes a necessity. HD68450 has been designed to meet this requirement in a highly efficient manner.

HD68450 has 4 independent DMA channels of operation with programmable channel priorities. It can handle data sizes of byte, word (16-bits), and longword (32-bits), and has a direct addressing range of 16 megabytes. It performs 16-bit DMA transfers on an asynchronous bus as well as synchronous transfers with 8-bit HMCS6800 peripheral LSI's using the enable signal. It outputs function code signal for memory management and it can handle bus error, halt, and retry operations to compliment the highly reliable HMCS68000 system.

The transfer modes of HD68450 consists of transfer between memory and peripheral device, and also between memories. Transfer of blocks of data can be done by using the continue mode, array chain mode, or linked array chain mode. Single addressing mode is provided for transfer between memory and device having the same port size, as well as dual addressing mode for different port sizes. In the dual addressing mode, transfer is done in two bus cycles – memory to DMAC, then DMAC to device. As can be seen by its many features, HD68450 is a highly intelligent device to meet the different data transfer requirements for each individual applications.

HD68450

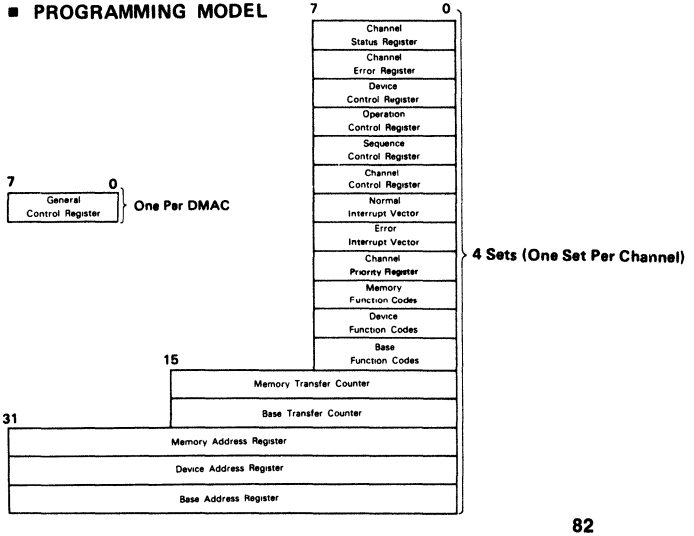


(DC-64)

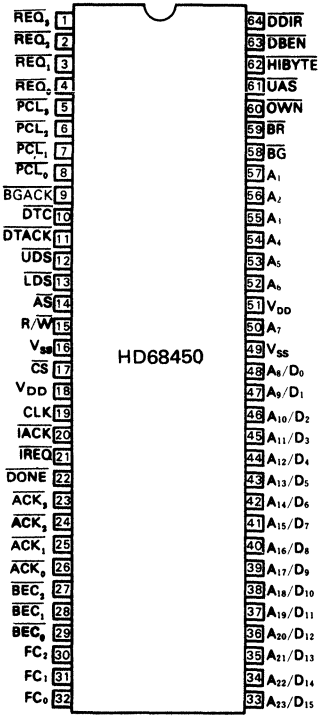
■ FEATURES

- HMCS68000 Bus Compatible
- Interfaces Directly with HMCS68000/HMCS6800 Peripherals
- Memory-to-Device, Device-to-Memory, and Memory-to-Memory Transfers.
- Continue Mode and Array Chained, Linked Array Chained Operations
- 4 Independent Channels with Programmable Priorities
- Handles Byte, Word, and Longword Data Sizes
- External Request Mode and Auto-Request Mode
- Maximum Transfer Rate of 2 Mega Word/Sec

■ PROGRAMMING MODEL



■ PIN ARRANGEMENT



(Top View)

PACKAGE INFORMATION

Packages are classified into 3 types; dual-in-line plastic, dual-in-line ceramic (glass-sealed) and dual-in-line ceramic (with lid), according to the quality of material used for packaging.

Type	Function	Package*			
		Pin No.	C**	G	P
HD6800	Micro Processing Unit	40	O		O
HD68A00			O		O
HD68B00			O		O
HD6802S	Microprocessor with Clock and RAM	40	O		O
HD6809	8/16 Bit Micro Processing Unit	40	O		O
HD68A09			O		O
HD68B09			O		O
HD6821	Peripheral Interface Adapter	40	O		O
HD68A21			O		O
HD68B21			O		O
HD6840	Programmable Timer Module	40			
HD68A40			O		O
HD68B40					
HD6850	Asynchronous Communications Interface Adapter	24	O		O
HD68A50			O		O
HD6852	Synchronous Serial Data Adapter	24	O		O
HD68A52			O		O
HD6846	Combination ROM I/O Timer	40	O		O
HD6843S	Floppy Disk Controller	40	O		O
HD68A43S			O		O
HD6844	Direct Memory Access Controller	40	O		O
HD68A44			O		O
HD6845	CRT Controller	40	O		O
HD68A45			O		O
HD68B45			O		O
HD46508	Analog Data Acquisition Unit	40			O
HD46508-1					O
HD68000-4	16/32 Bit Microprocessor	64			
HD68000-6			O-std.		
HD68000-8					
HD68450-4	16 Bit Direct Memory Access Controller	64			
HD68450-6			O-std.		
HD68450-8					

* The package codes of C, G and P are applied to the package materials as follows
C, Ceramic with Lid
G; Glass — Sealed Ceramic
P, Plastic
** Special Order Only

8-Bit Single-Chip Microcomputer Series

Because of versatile functions, low cost and ease of use, 8-bit single-chip microcomputers are widely used. Hitachi's 8-bit single-chip microcomputers consist of the HD6805 NMOS family, developed for control of relatively small systems, the HD6801 NMOS family, suited for applications requiring high-precision, high-speed processing, and the HD6301 CMOS family that feature the low power consumption characteristic of CMOS while maintaining and enhancing the functionality and performance of the HD6801 family. Utilizing state of the art 3μm process techniques, these LSI devices outperform conventional products in both functionality and data processing capability. Table 1 compares the characteristics of HD6805 and HD6801 families.

Evaluation kits and cross software are available to help users with program development systems implementation.

HD6805 Family

The HD6805 family consists of the HD6805S0, HD6805U0, and HD6805V0. They are all supplied in standard 28- or 40-pin DIL plastic packages. In additions, new versions incorporating 8-bit A/D converters powerful timers and wider I/O ports are being developed. Instruction sets of the HD6805 family are all interchangeable. This enables the use of common programs, thus making it easy to meet the demand to upgrade application systems.

- **Specifications:**
  - ROM 1k-byte to 4k-byte
  - RAM 64-byte to 96-byte
  - I/O ports 20 to 32

- **CPU Architecture:**

The architecture of the HD6805 family has the following characteristics:

- Bit operation instructions and bit test/branch instructions are very powerful.
- Memory and I/O are located in the same address space.
- Several address modes may be used.
- The stack system is quite flexible.

Thanks to powerful bit instructions, any bit can be set or cleared at any output port. Also, it is possible to subject any bit to test or conditional branching at any input port. Thus, all the processing necessary for bit I/O operations can be executed by one instruction. Similarly, it is possible to set, clear, test and subject to conditional branching any bit at any RAM address. Specifically, all RAM bits can be readily utilized. As software flags in a program by means of the bit instructions. With these abundant bit instructions, the HD6805 family is suitable for small-scale control where point input and point output are common practices. Because indirect register, modification and other index modes are powerful, effective use can be made of address modes for table reference on ROM, reduction of the average number of bytes in a program, and other purposes. Since the multiple interrupt and subroutine call instructions of the HD6805 family are automatically saved and returned by the stack pointer, almost unlimited nesting is possible.

- **On-Chip memory and Peripheral Functions:**

On-chip RAM, ROM and I/O are arranged in a common address space. Further, various on-chip memory are available, permitting an optimum choice for each individual application. To make the most use of available device pins, the I/O ports for each device can collectively be designated by the program for use either as input or output ports. With its high drive current capacity, port B can directly drive not only TTL but also darlington and LED circuits. Port D contains seven voltage comparators whose input voltage logical decision threshold levels can be set externally. The use of port D enables the direct input of logical threshold levels other than TTL without employing any external signal level conversion.

Table 1. Comparison between HD6801 Family and HD6805 Family

Description / Classification	Instruction System	Memory	I/O Port	Timer	Serial	A/D
HD6801 Family	•Extended from HD6800 •16-bit operation possible •Multiplication possible	•External memory addition possible in memory extension mode •Standby possible	•TTL compatable •I/O data strobe signal control	•Pulse generation •Pulse width measuring •Clock timer	•Start-stop type •Synchronous transmission-reception	———
HD6805 Family	•Single-type instructions •Bit operation instructions •Bit test instructions •Look-up table reference capability	•On-chip ROM & RAM only	•TTL compatable •CMOS compatable •Darlington drive possible •Voltage comparator provided	•Clock timer •Pulse counter [Pulse generation Pulse width measuring]	———	[Successive approximation type 8-bit A/D converter]

* [ ] = Function of the machine being developed.

Fig. 1 shows a block diagram of the HD6805V0, and Fig. 2 exemplifies the use of the I/O ports of the HD6805 family.

HD6801 Family

The HD6801 family consists of the HD6801S0 and HD6801V0, both available in 40-pin DIL standard packages. The HD6801 family ranks above the HD6805 family. It is a family of high-performance, multi-function 8-bit single-chip microcomputers incorporating CPUs with powerful, high-speed instruction sets that are equivalent to, or even superior to the CPUs of standard microprocessor units. Abundant memory (such as ROM and RAM) multi-function timers, serial communication control circuity, and various peripheral functions are all incorporated on one chip.

- **Specifications**
  - On-board ROM: 2k-byte to 4k-byte
  - On-board RAM: 128-byte
  - I/O ports: 29
- **CPU Architecture**

The characteristics of the HD6801 family's CPU architecture are as follows:

- Its instruction set has been expanded from that of the HMCS6800.
- It contains such high-level instructions as multiplication and 16-bit operations.
- Its branch (and some other instructions) are faster than those of the HMCS6800.
- By adding external memory, its address space can be expanded up to 65k-word, thereby supporting applications other than those programmed in its on-board ROM and without sacrificing operating speed or other performance items.

Hence the HD6801 family is a family of microcomputers that can perform high-speed, high-precision data processing.

- **On-board Memories and Peripheral Functions**

The most important peripheral function incorporated in the HD6801 family is a start-stop communication control function that enables simultaneous execution of data transmission and reception. The data transfer rate can be set by the program. The start-stop communication control function is especially useful for communication terminals and computer printers. The on-board 16-bit timer is enhanced that, in addition to ordinary time measurements, the measurement of the input pulse widths and also the generation of pulses of programmable width are attainable with high accuracy.

Fig. 3 shows a function block diagram of the HD6801S0, Fig. 4 shows a block diagram of an incorporated communication control circuit, and Fig. 5 shows a block diagram of an incorporated timer.

HD6301 Family

The HD6301 family consists of the HD6301V, which incorporates CPU, ROM, RAM, I/O ports and other peripheral functions. The HD6301 family is a high-performance, power-efficient product that is equivalent, or superior to the high-performance NMOS single-chip microcomputer

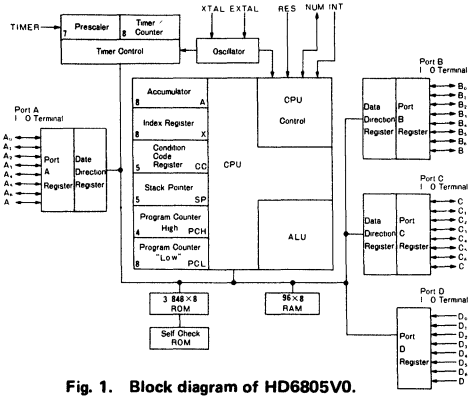


Fig. 1. Block diagram of HD6805V0.

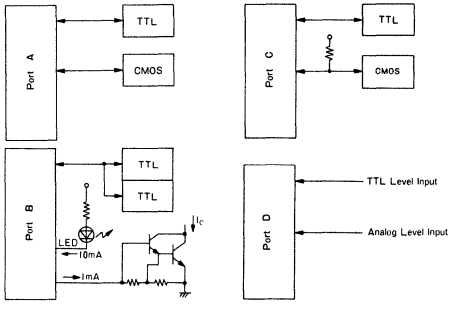


Fig. 2. An example of HD6805 family I/O ports in use.

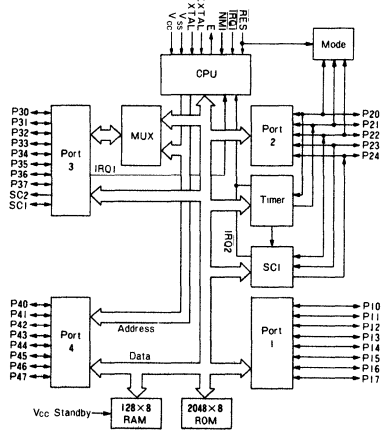


Fig. 3. Block diagram of HD6801S0.

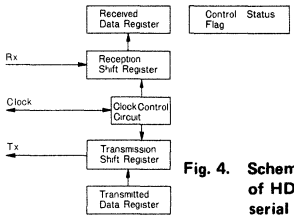


Fig. 4. Schematic block diagram of HD6801S0 serial communication control section.

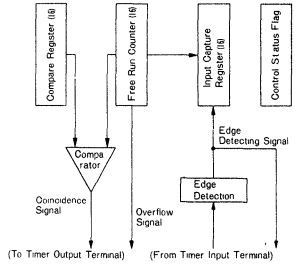


Fig. 5. Schematic block diagram of HD6801S0 timer.

type HD6801. This power is accomplished by the combination of latest 3μm CMOS techniques and microprogram control approach.

- **Functions**

The instruction set of the HD6301 family has been expanded from that of the HD6801 family. Its enhanced characteristics include the addition of true bit operating instructions (set, clear, invert and test), which were an advantage of the HD6805 family. 4k-bytes of ROM, 128-bytes of RAM, multi-function timer (compatible with the HD6801 family) and communications control circuitly have been incorporated on the chip.

The HD6301 family also has an operation code trap and an address trap function. Therefore, when any undefined operation code is fetched or any instruction is fetched from an unusable address, it generates an internal interruption of the highest priority. These error detecting and processing functions are effective for the prevention of system run-away due to system noise and program error with a resultant increase in debug efficiency during the course of program development.

- **Performance**

To increase instruction execution speed, two measures were taken; (1) reducing the number of instruction execution cycles through the introduction of extensive pipeline control, and (2) increasing the clock frequency. Consequently, the minimum instruction execution cycle (1 cycle) of the HD6301 family now equals 0.7μs* (when the clock frequency is 1.5MHz). The power consumed by the HD6301V0 is 30mW during operation (1MHz), 3mW in the sleep mode (1MHz), and not more than 0.3mW in standby. This is a remarkable improvement when compared with conventional NMOS/HMOS approaches.

- **Power-efficient Operation**

In addition to the ordinary operation mode, the HD6301 family has two low-power-consumption modes; sleep and power-down.

In the sleep mode, the CPU stops processing, with the internal state of CPU, output port latch, RAM and other status remaining unchanged. Meanwhile, the timer, serial communication control and interrupt control sections continue to function. Even in the sleep mode, clocking, data transmission and reception, and pulse generation can be accomplished. In the sleep mode, the HD6301 consumes only one-tenth the power consumed during normal operation. When the "sleep" instruction is executed, the operation mode changes to the sleep mode. The normal operation mode returns when an interrupt request is made from an external terminal or timer to the CPU, whereupon the interrupted job or requested routine starts. The sleep mode is a state in which the system remains inoperative is done in such a manner that the interrupted job can be resumed any time. (This state is often referred to as a "hot startable" state.)

The use of the sleep mode enables power consumption to be effectively reduced in any system whose CPU need not be operated at all times. A good example is a system that conducts much data transmission, reception and clocking, but in which computing and other CPU-related operations account for only about 10 percent of the total operation time. In this case, the mean power consumption can be cut by as much as 80 percent. Another power-saving opportunity is the power-down mode, in which all device operation stops. In the power-down mode, the contents of the on-board RAM remain intact. Accordingly, the system can be protected against power interruption by ordinary saving and returning methods. The HD6301's power consumption in the power-down mode drops to 1 percent, or even less, of the level in normal operation. When an input is supplied through a special terminal the HD6301 switches from operation or sleep mode into the power-down mode. To return to the former mode. A reset-start is necessary.

Table 2 shows key specifications of the HD6301V. Fig. 6 shows a system block diagram, and Fig. 7 shows a mode transition diagram.

Table 2. Specifications of HD6301V0

Description	Specification
Instruction set	• Expanded from HD6801S0 • Augmented bit operation and test instructions
On-board memory	• ROM. 4k-byte • RAM 128-byte
Function	• Multi-function 16k-bit timer (same as HD6801S0) • Start-stop serial communication circuit (same as HD6801S0)
System extension	• Single-chip mode • Non-multiple extension mode (64k-byte maximum) • Multiple extension mode (64k-byte maximum)
I/O port	29 I/O common ports
Error processing	Address and operation code trap
Operating speed	• All instructions are single cycle • Frequency 9 1MHz ~ 1.5MHz*
Power consumption	• Operation mode 30mW (1Mhz) Sleep Mode 3mW (1MHz) Power-down mode 0 3mW

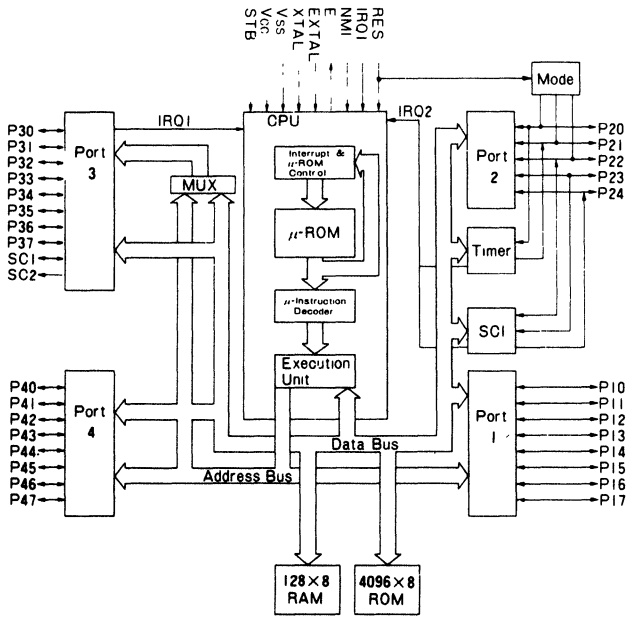


Fig. 6. Block diagram of HD6301.

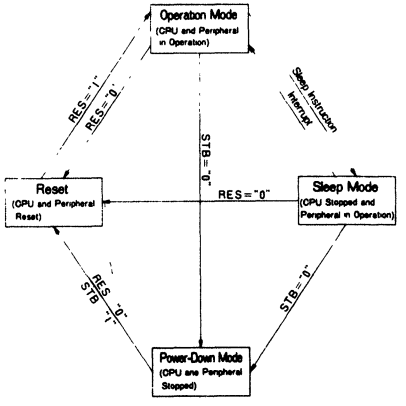


Fig. 7. Mode transition diagram of HD6301V.

8-Bit Single-Chip Microcomputer Series

HMCS6800 Series 8-bit single-chip microcomputers are divided into two families:

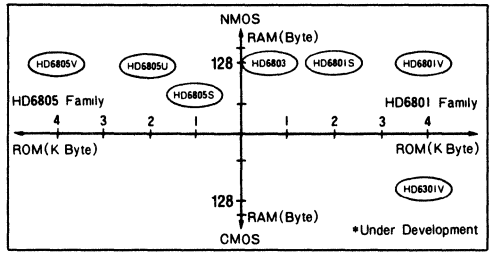
The HD6801 Family is designed for "high-end" equipment applications. These microcomputers contain a CPU, oscillator, ROM, RAM, TIMER, and serial and parallel I/O ports. In addition, the revolutionary HD6301V is fabricated using a high-performance CMOS process and is upward compatible with the HD6801.

The HD6805 Family is a very low-cost series of microcomputers ideally suited for controller-type applications. These microcomputers contain a CPU, on-chip oscillator, ROM, RAM, and I/O ports.

FEATURES

- Versatile interrupt handling
- Powerful indexed addressing
- Full set of conditional branches
- Memory mapped I/O
- 16-bit timer (6801/6301)
- 8-bit programmable timer with 7-bit programmable pre-scaler (6805)
- 8 × 8 multiply (6801/6301)
- Sleep operation for power saving (6301)
- True bit manipulation (6805)

OUTLINE OF 8-BIT SINGLE-CHIP MICROCOMPUTER



8-BIT SINGLE-CHIP CHARACTERISTICS

	Type Number		HD6801S	HD6801V	HD6803	HD6301V	HD6805S	HD6805U	HD6805V
LSI Characteristics	Process		NMOS	NMOS	NMOS	CMOS	NMOS	NMOS	NMOS
	Supply Voltage		5V	5V	5V	5V	5V	5V	5V
	Operating Temperature**		0~70°C	0~70°C	0~70°C	0~70°C	0~70°C	0~70°C	0~70°C
	Package		DP-40 DC-40	DP-40 DC-40	DP-40 DC-40	DP-40 DC-40	DP-28 DC-28	DP-40 DC-40	DP-40 DC-40
Function	Memory	ROM (K Byte)	2	4	–	4	1.1	2	4
		RAM (Byte)	128	128	128	128	64	96	96
	I/O		29	29	13	29	20	32	32
	Timer (bit)		16	16	16	16	8***	8***	8***
	Serial Comm. Interface		Yes	Yes	Yes	Yes	No	No	No
	Other Features		• Data Retention Capability • Single-Chip or External Memory	• Data Retention Capability • Single-Chip or External Memory	• Multiplexed Address and Data • Add External EPROMs for HD6801 Emulation	• 0.3 mW Max. (Sleep) • 30mW Max. (Active) • Single-Chip or External Memory	• Vectored Interrupts • Self-Check Mode • Master Reset	• Voltage Comparator • Self-Check Mode • Master Reset	• Voltage Comparator • Self-Check Mode • Master Reset
	Compatibility		MC6801	–	MC6803	–	MC6805P2	–	–

** Wide Temperature Range (-40~+85°C). Please contact Hitachi America, Ltd.
*** Timer: 8-Bit programmable Timer with 7-Bit programmable pre-scaler.

Support Products

A characteristic of single-chip microcomputers is that the user can set his own program in the LSI's ROM area. Hence, several support tools to help the user develop his own programs are called for:

- **Evaluation Kit**

An evaluation kit is comprised of a main board an emulation section, and a pocketable console that varies from type to type. An assembler and text editor are available in the form of EPROMs. The characteristics of evaluation kits are as follows:

- Conductive to easy program development.
- Capable of hardware debugging. When connected to a prototype system being developed by the user.
- Connectable to a console typewriter.
- Capable of storing the developed program by writing to EPROM (HN462716).

Some examples of evaluation kits are given below.

(1) Development of a Simple System Program

An evaluation kit for this use consists of a main board, emulation section, and hand-held console. It is used at the machine language level.

(2) Development of Paper-tape-based Program

This evaluation kit consists of a main board, emulation section and terminal, plus an assembler and text editor. A paper tape source program is made by use of the assembly language, which can be assembled or edited on the main board.

- **Cross Software**

Table 3 lists the assemblers for the 8-bit single-chip microcomputers.

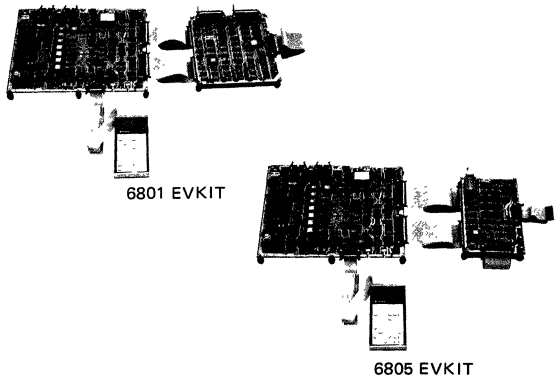


Fig. 8. Photographs of Evaluation Kits.

Assembler for Evaluation Kit

This assembler assembles a source program, written in HD6801 or HD6805 assembly level language, on paper tape. The object program is outputted on paper tape in absolute address form (S-type object format). Direct output to the evaluation kit memory is also possible. In this case, a source program developed using the cross assembler is inputted to the Evaluation Kit.

- Cross Assembler for Development System

This cross assembler is capable of efficient assembling on a floppy disk basis. The source program is inputted from a file on the floppy disk, and the object program is outputted on a file too.

The assemblers for the HD6801 and HD6301 are provided with macro, conditional assembly, and relocatable object output functions. The relocatable object can be linked and relocated with other object programs by the linkage editor which is a feature of the Floppy Disk Operating System (FDOS).

The HD6805 cross assembler outputs the object program on a floppy disk file in absolute address form, so that it can readily written into EPROM or output on paper tape.

- **Cross Assembler for an Intel MDS [system]:**

This cross assembler (for Intel's development system [MDS]) operates under the control of OS and ISIS-II. Capable of conditional assembly, it outputs an object program, in hexadecimal paper tape format, on a Floppy Disk. The ISIS-II command converts the object program into an object file of absolute address form.

It is also possible to write the object program prepared by the HD6801 cross assembler into EPROM (HN462716) and debug using the evaluation kit.

Table 3. List of Cross Software Products

Host Machine \ Applicable Device	6805	6801	6301
Evaluation kit	○	○	△
Intel MDS	△	△	△

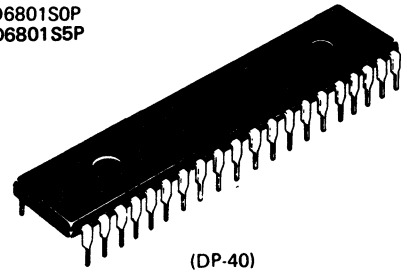
○ Available
△ Under development
△ Under evaluation
* With macro function
** With relocatable object output function

HD6801S0, HD6801S5

MCU (Microcomputer Unit)

The HD6801S MCU is an 8-bit microcomputer system which is compatible with the HMCS6800 family of parts. The HD6801S MCU is object code compatible with the HD6800 with improved execution times of key instructions plus several new 16-bit and 8-bit instructions including an 8x8 unsigned multiply with 16-bit result. The HD6801S MCU can operate as a single - chip microcomputer or be expanded to 65k words. The HD6801S MCU is TTL compatible and requires one +5.0 volt power supply. The HD6801S MCU has 2k bytes of ROM and 128 bytes of RAM on chip. Serial Communications interface (S.C.I.), and parallel I/O as well as a three function 16-bit timer. Features and Block diagram of the HD6801S include the following:

HD6801S0P
HD6801S5P

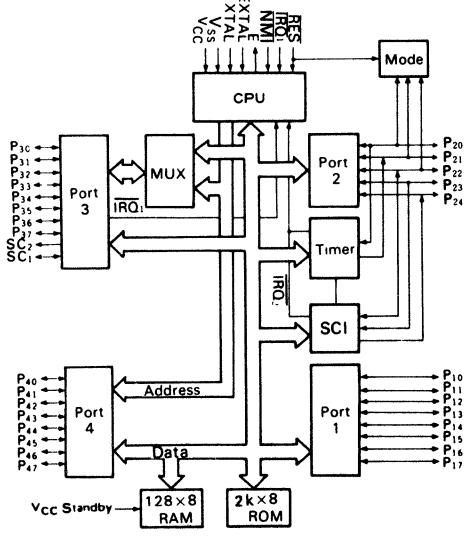


(DP-40)

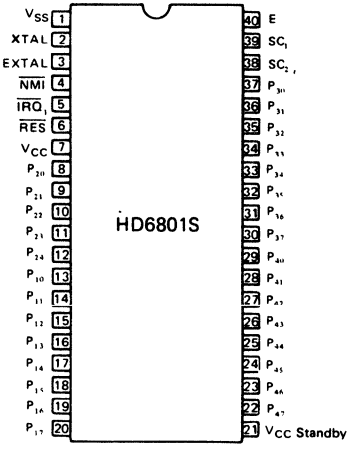
■ FEATURES

- Expanded HMCS6800 Instruction Set
- 8 x 8 Multiply
- On-Chip Serial Communications Interface (S.C.I.)
- Object Code Compatible With The HD6800 MPU
- 16-Bit Timer
- Single Chip Or Expandable To 65k Words
- 2k Bytes Of ROM
- 128 Bytes Of RAM (64 Bytes Retainable On Power Down)
- 29 Parallel I/O Lines And 2 Handshake Control Lines
- Internal Clock/Divided-By-Four Circuitry
- TTL Compatible Inputs And Outputs
- Interrupt Capability
- Compatible with MC6801

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TYPE OF PRODUCTS

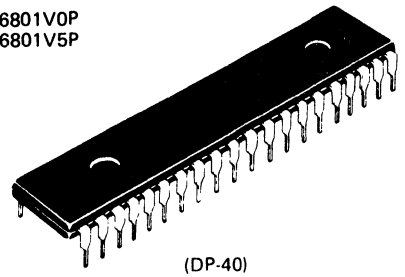
MCU	Bus Timing
HD6801S0	1 MHz

HD6801V0, HD6801V5

MCU (Microcomputer Unit) PRELIMINARY

The HD6801V MCU is an 8-bit microcomputer system which is compatible with the HD6801S except the ROM size. The HD6801V MCU is object code compatible with the HD6800 with improved execution times of key instructions plus several new 16-bit and 8-bit instructions including an 8×8 unsigned multiply with 16-bit result. The HD6801V MCU can operate as a single chip microcomputer or be expanded to 65k words. The HD6801V MCU is TTL compatible and requires one +5.0 volt power supply. The HD6801V MCU has 4k bytes of ROM and 128 bytes of RAM on chip. Serial Communications interface (SCI), and parallel I/O as well as a three function 16-bit timer. Features and Block diagram of the HD6801V include the following:

HD6801V0P
HD6801V5P

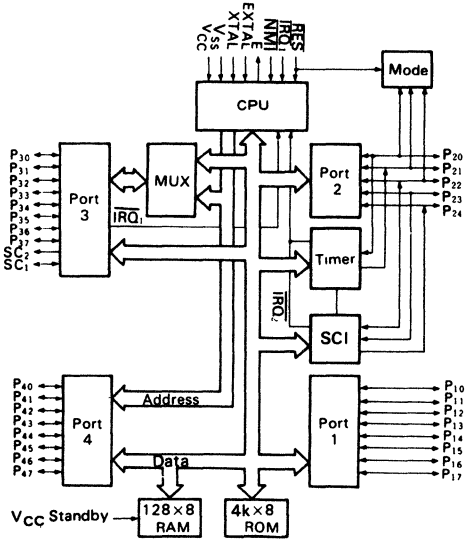


(DP-40)

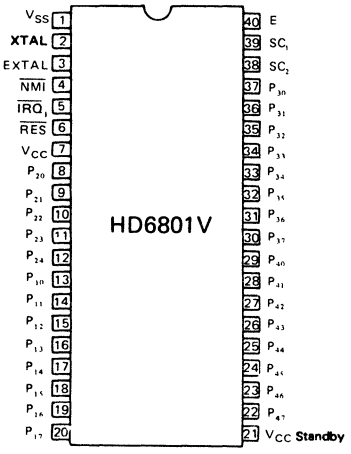
■ FEATURES

- Expanded HMCS6800 Instruction Set
- 8 x 8 Multiply
- On-Chip Serial Communications Interface (SCI)
- Object Code Compatible With The HD6800 MPU
- 16-Bit Timer
- Single Chip Or Expandable To 65k Words
- 4k Bytes Of ROM
- 128 Bytes Of RAM (64 Bytes Retainable On Power Down)
- 29 Parallel I/O Lines And 2 Handshake Control Lines
- Internal Clock/Divided-By-Four Circuitry
- TTL Compatible Inputs And Outputs
- Interrupt Capability
- Compatible with MC6801 (except ROM size)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TYPE OF PRODUCTS

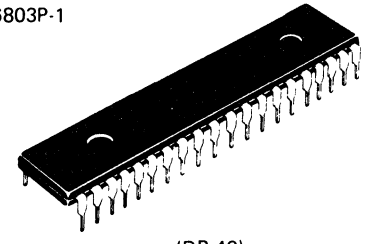
MCU	Bus Timing
HD6801V0	1 MHz

HD6803, HD6803-1

MPU (Microprocessing Unit)

The HD6803 MPU is an 8-bit microcomputer system which is compatible with the HMCS6800 family of parts. The HD6803 MPU is object code compatible with the HD6800 with improved execution times of key instructions plus several new 16-bit and 8-bit instructions including an 8 x 8 unsigned multiply with 16-bit result. The HD6803 MPU can be expanded to 65k words. The HD6803 MPU is TTL compatible and requires one +5.0 volt power supply. The HD6803 MPU has 128 bytes of RAM, Serial Communications interface (S.C.I.), and parallel I/O as well as a three function 16-bit timer. Features and Block diagram of the HD6803 include the following:

HD6803P
HD6803P-1

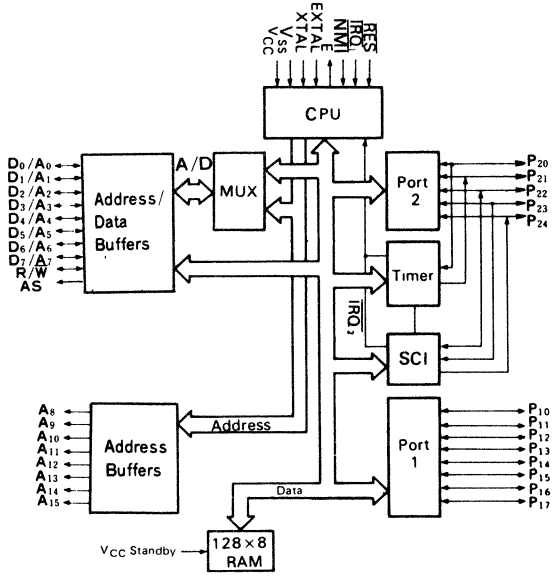


(DP-40)

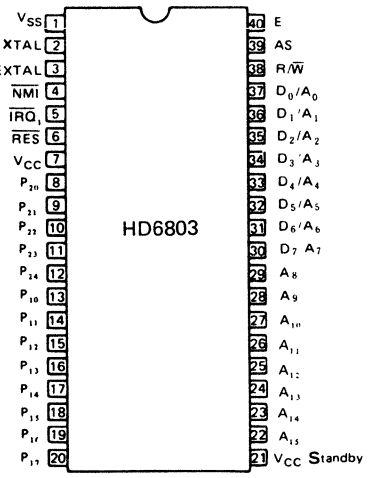
■ FEATURES

- Expanded HMCS6800 Instruction Set
- 8 x 8 Multiply
- On-Chip Serial Communications Interface (S.C.I.)
- Object Code Compatible With The HD6800 MPU
- 16-Bit Timer
- Expandable to 65k Words
- Multiplexed Address and Data
- 128 Bytes Of RAM (64 Bytes Retainable On Power Down)
- 13 Parallel I/O Lines
- Internal Clock/Divided-By-Four
- TTL Compatible Inputs And Outputs
- Interrupt Capability
- Compatible with MC6803

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TYPE OF PRODUCTS

Type No.	Bus Timing
HD6803	1.0MHz
HD6803-1	1.25MHz

HD6805S1

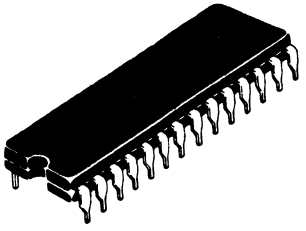
MCU (Microcomputer Unit)

The HD6805S1 is the 8-bit Microcomputer Unit (MCU) which contains a CPU, on-chip clock, ROM, RAM, I/O and timer. It is designed for the user who needs an economical microcomputer with the proven capabilities of the HD 6800-based instruction set.

The following are some of the hardware and software highlights of the MCU.

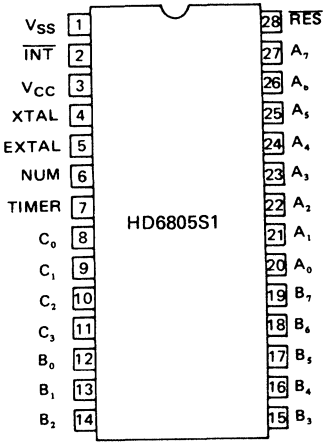
- **HARDWARE FEATURES**
- 8-Bit Architecture
- 64 Bytes of RAM
- Memory Mapped I/O
- 1100 Bytes of User ROM
- Internal 8-Bit Timer with 7-Bit Prescaler
- Vectored Interrupts – External and Timer
- 20 TTL/CMOS Compatible I/O Lines; 8 Lines LED Compatible
- On-Chip Clock Circuit
- Self-Check Mode
- Master Reset
- Low Voltage Inhibit
- Complete Development System Support by Evaluation kit
- 5 Vdc Single Supply
- Compatible with MC6805P2
- **SOFTWARE FEATURES**
- Similar to HD6800
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instructions
- Versatile Interrupt Handing
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Brancnes
- Memory Usable as Registers/Flags
- Single Instruction Memory Examine/Change
- 10 Powerful Addressing Modes
- All Addressing Modes Apply to ROM, RAM and I/O
- Compatible with MC6805P2

HD6805S1P



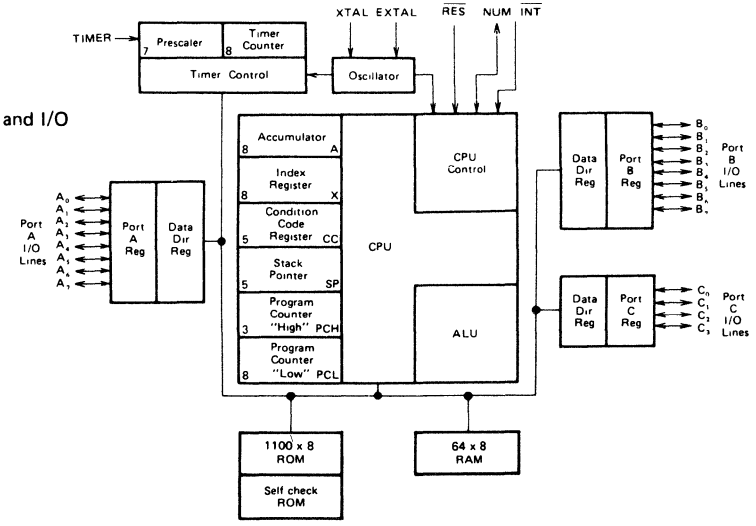
(DP-28)

■ **PIN ARRANGEMENT**



(Top View)

■ **BLOCK DIAGRAM**



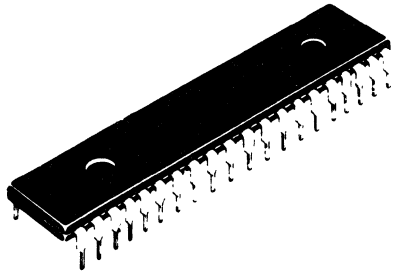
HD6805U1

MCU (Microcomputer Unit)

The HD6805U1 is the 8-bit Microcomputer Unit (MCU) which contains a CPU, on-chip clock, ROM, RAM, I/O and timer. It is designed for the user who needs an economical microcomputer with the proven capabilities of the HD6800-based instruction set.

The following are some of the hardware and software highlights of the MCU.

HD6805U1P



(DP-40)

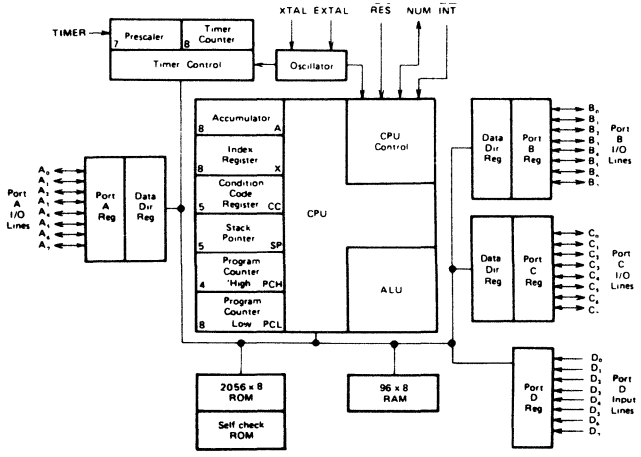
■ HARDWARE FEATURES

- 8-Bit Architecture
- 96 Bytes of RAM
- Memory Mapped I/O
- 2056 Bytes of User ROM
- Internal 8-Bit Timer with 7-Bit Prescaler
- Vectored Interrupts – External and Timer
- 24 I/O Ports + 8 Input Port
  (8 Lines LED Compatible; 7 Voltage Comparator Inputs)
- On-Chip Clock Circuit
- Self-Check Mode
- Master Reset
- Low Voltage Inhibit
- Complete Development System Support by Evaluation Kit
- 5 Vdc Single Supply

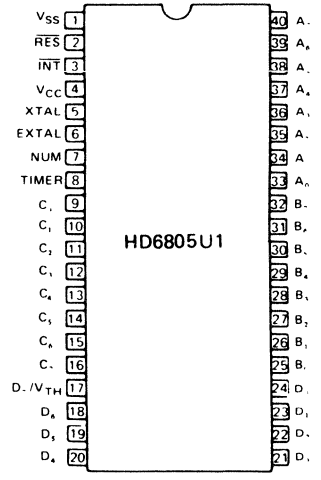
■ SOFTWARE FEATURES

- Similar to HD6800
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instructions
- Versatile Interrupt Handing
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Branches
- Memory Usable as Registers/Flags
- Single Instruction Memory Examine/Change
- 10 Powerful Addressing Modes
- All Addressing Modes Apply to ROM, RAM and I/O Compatible Instruction Set with MC6805P2

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

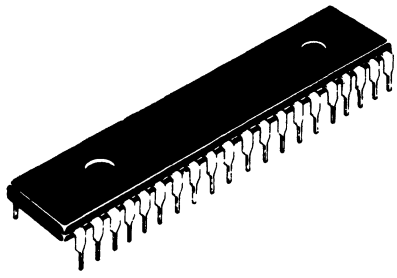
HD6805V1

MCU (Microcomputer Unit)

The HD6805V1 is the 8-bit Microcomputer Unit (MCU) which contains a CPU, on-chip clock, ROM, RAM, I/O and timer. It is designed for the user who needs an economical microcomputer with the proven capabilities of the HD6800-based instruction set.

The following are some of the hardware and software highlights of the MCU.

HD6805V1P



(DP-40)

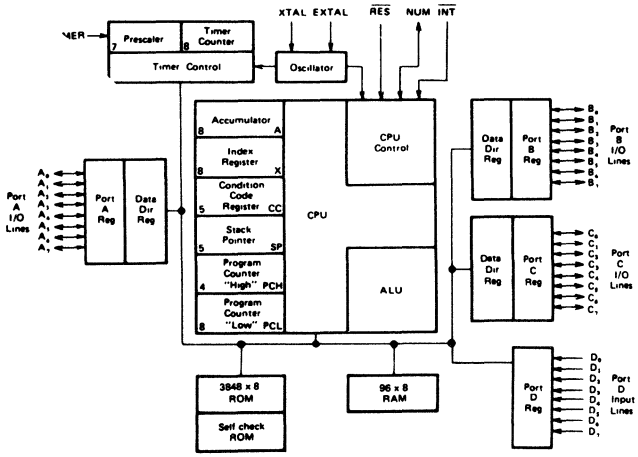
■ HARDWARE FEATURES

- 8-Bit Architecture
- 96 Bytes of RAM
- Memory Mapped I/O
- 3848 Bytes of User ROM
- Internal 8-Bit Timer with 7-Bit Prescaler
- Vectored Interrupts — External and Timer
- 24 I/O Ports + 8 Input Port
  (8 Lines LED Compatible; 7 Voltage Comparator Inputs)
- On-Chip Clock Circuit
- Self-Check Mode
- Master Reset
- Low Voltage Inhibit
- Complete Development System Support by Evaluation Kit
- 5 Vdc Single Supply

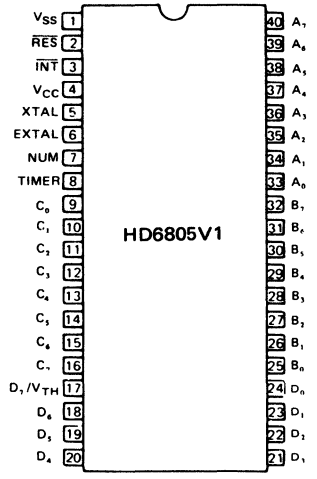
■ SOFTWARE FEATURES

- Similar to HD6800
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instructions
- Versatile Interrupt Handing
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Branches
- Memory Usable as Registers/Flags
- Single Instruction Memory Examine/Change
- 10 Powerful Addressing Modes
- All Addressing Modes Apply to ROM, RAM and I/O
- Compatible Instruction Set with MC6805P2

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

HD6805W0

MCU (Microcomputer Unit) PRELIMINARY

The HD6805W0 is an 8-bit microcomputer unit (MCU) which contains a CPU, on-chip clock, ROM, RAM, standby RAM, A/D Converter, I/O and two timers. This MCU is a member of the HD6805 family but compared with HD6805S, it is a single-chip microcomputer with strengthened internal functions of standby RAM, A/D Converter, timers and I/O.

The following are some of the hardware and software highlights of the MCU.

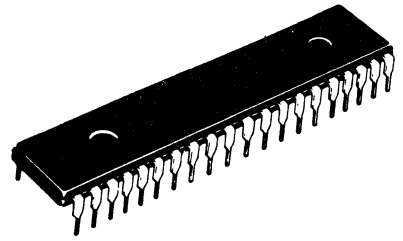
■ HARDWARE FEATURES

- 8-Bit Architecture
- 96 Bytes of RAM
  (8 bytes are standby RAM functions)
- Memory Mapped I/O
- 3834 Bytes of User ROM
- Internal 8-Bit Timer (Timer 1) with 7-Bit Prescaler
- Internal 8-Bit Programmable Timer (Timer 2)
- Interrupts – 2 External and 4 Timers
- 23 TTL/CMOS compatible I/O Lines; 8 Lines LED Direct Drive
- 8-Bit, 4-channel Internal A/D Converter
- Internal Clock Circuit
- Self-Check Mode
- Master Reset
- Low Voltage Inhibit
- Complete Development System Support by Evaluation Kit
- 5 Vdc Single Supply

■ SOFTWARE FEATURES

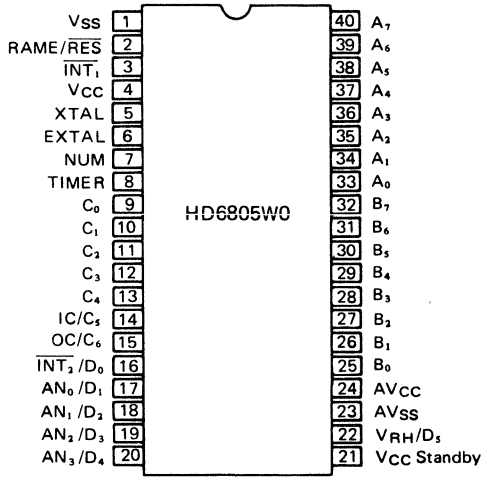
- Similar to HD6800
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instructions
- Versatile Interrupt Handing
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Branches
- Memory Usable as Registers/Flags
- Single Instruction Memory Examine/Change
- 10 Powerful Addressing Modes
- All Addressing Modes Apply to ROM, RAM and I/O
- Compatible with MC6805P2, HD6805S1 and HD6805V1

HD6805W0P



(DP-40)

■ PIN ARRANGEMENT



(Top View)

HD6301V0, HD63A01V0, HD63B01V0

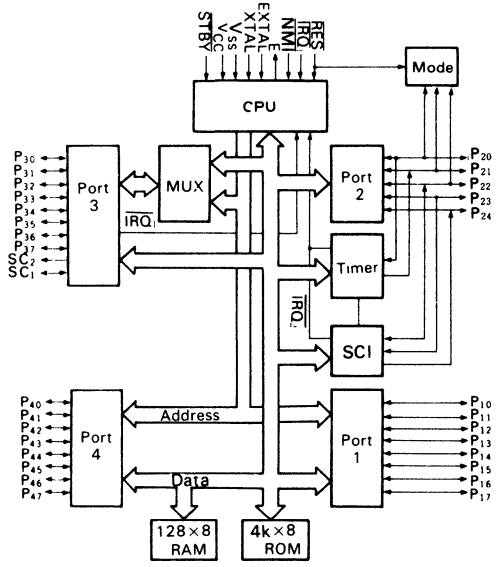
CMOS MCU (Microcomputer Unit) PRELIMINARY

The HD6301V0 is an 8-bit CMOS single-chip microcomputer unit, Object Code compatible with the HD6801. 4kB ROM, 128 bytes RAM, Serial Communication Interface (SCI), parallel I/O terminals as well as three functions of timer on chip are incorporated in the HD6301V0. It is bus compatible with HMCS6800, provided with some additional functions such as an improved execution time of key instruction plus several new instructions of operation to increase system throughput. The HD6301V0 can be expanded up to 65k words. Like the HMCS6800 family, I/O level is TTL compatible with +5.0V single power supply. By using the Hitachi's 3μm CMOS process, low power consumption is realized. And as lower power dissipation mode, HD6301V0 has Sleep Mode and Stand-By Mode. So flexible low power consumption application is possible.

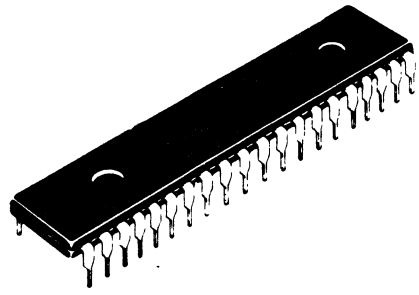
■ FEATURES

- Object Code Upward Compatible with HD6801 Family
- Abundant On-Chip Functions Compatible with HD6801V0; 4kB ROM,128 Bytes RAM,29 Parallel I/O Lines, 2 Lines of Data Strobe, 16-bit Timer, Serial Communication Interface
- Low Power Consumption Mode: Sleep Mode, Standby Mode
- Minimum Instruction Cycle Time
  1μs (f=1MHz), 0.67μs (f=1.5MHz), 0.5μs (f=2MHz)
- Bit Manipulation, Bit Test Instruction
- Protection from System Burst: Address Trap, Op-Code Trap
- Up to 65k Words Address Space
- Wide Operation Range
  V_{CC}=3 to 6V (f=0.5MHz), f=0.1 to 1.5MHz (V_{CC}=5V ±10%), f=0.1 to 2.0MHz (V_{CC}=5V ±5%)

■ BLOCK DIAGRAM

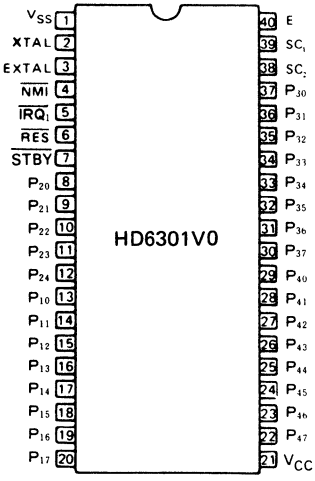


HD6301V0P, HD63A01V0P, HD63B01V0P



(DP-40)

■ PIN ARRANGEMENT



(Top View)

■ TYPE OF PRODUCTS

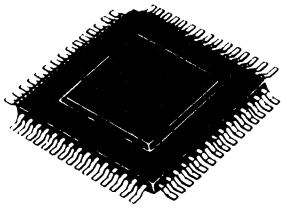
Type No.	Bus Timing
HD6301V0	1 MHz
HD63A01V0	1.5 MHz
HD63B01V0	2 MHz

HD63L05

CMOS MCU (Microcomputer Unit) PRELIMINARY

The HD63L05 is a CMOS single-chip microcomputer suitable for low-voltage and low-current operation. Having CPU functions similar to those of the HMCS6800 family, the HD63L05 is equipped with a 4k bytes ROM, 96 bytes RAM, I/O, timer, 8 bits A/D, and LCD (6 x 7 segments) drivers, all on one chip.

HD63L05



(FP-60A)

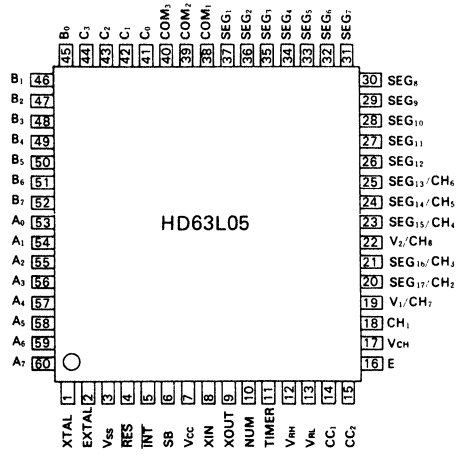
■ HARDWARE FEATURES

- 3V Power Supply
- 8-Bit Architecture
- Built-in 4k Bytes ROM (Mask ROM)
- Built-in 96 Bytes RAM
- 20 Parallel I/O Ports
- Built-in 6 x 7 Segments LCD Driver Capability
- Built-in 8-Bit Timer
- Built-in 8-Bit A/D Converter
- Program Halt Function for Low Power Dissipation
- Stand-by Input Terminal for Data Holding

■ SOFTWARE FEATURES

- An Instruction Set Similar to That of The HMCS6800 Family (Compatible with The HD6805S)
- HMCS6800 Family Software Development System Is Applicable

■ PIN ARRANGEMENT



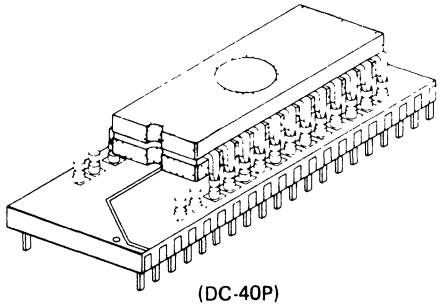
(Top View)

HD68P01S0, HD68P01V07,

MCU (Microcomputer Unit) PRELIMINARY

The HD68P01 is an 8-bit single chip microcomputer unit (MCU) which significantly enhances the capabilities of the HMCS6800 family of parts. It can be used in production systems to allow for easy firmware changes with minimum delay or it can be used to emulate the HD6801 for software development. It includes 128 bytes of RAM, Serial Communications Interface (SCI), parallel I/O and a three function Programmable Timer on chip, and 2048 bytes, 4096 bytes or 8192 bytes of EPROM on package. It includes an upgrade HD6800 microprocessing unit (MPU) while retaining upward source and object code compatibility. Execution times of key instructions have been improved and several new instructions have been added including an unsigned 8 by 8 multiply with 16-bit result. The HD68P01 can function as a monolithic microcomputer or can be expanded to a 65k byte address space. It is TTL compatible and requires one +5 volt power supply. A summary of HD68P01 features includes:

HD68P01S0, HD68P01V07



(DC-40P)

■ FEATURES

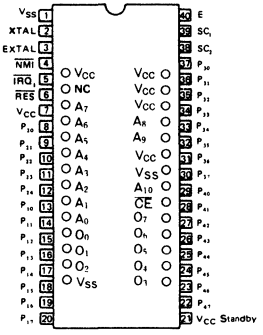
- Expanded HMCS6800 Instruction Set
- 8 x 8 Multiply Instruction
- Serial Communications Interface (SCI)
- Upward Source and Object Code Compatible with HD6800
- 16-bit Three-function Programmable Timer
- Applicable to All Type of EPROM
  - 2048 bytes; HN462716
  - 4096 bytes; HN462732
  - 8192 bytes; HN482764
- 128 Bytes of RAM (64 bytes Retainable on Powerdown)
- 29 Parallel I/O and Two Handshake Control Line
- Internal Clock Generator with Divide-by-Four Output
- Full TTL Compatibility
- Full Interrupt Capability
- Single-Chip or Expandable to 65k Bytes Address Space
- Bus compatible with HMCS6800 Family

■ TYPE OF PRODUCTS

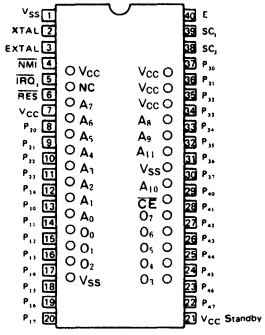
Type No.	Bus Timing	EPROM Type No.
HD68P01S0	1 MHz	HN462716
HD68P01V07	1 MHz	HN462732

■ PIN ARRANGEMENT (Top View)

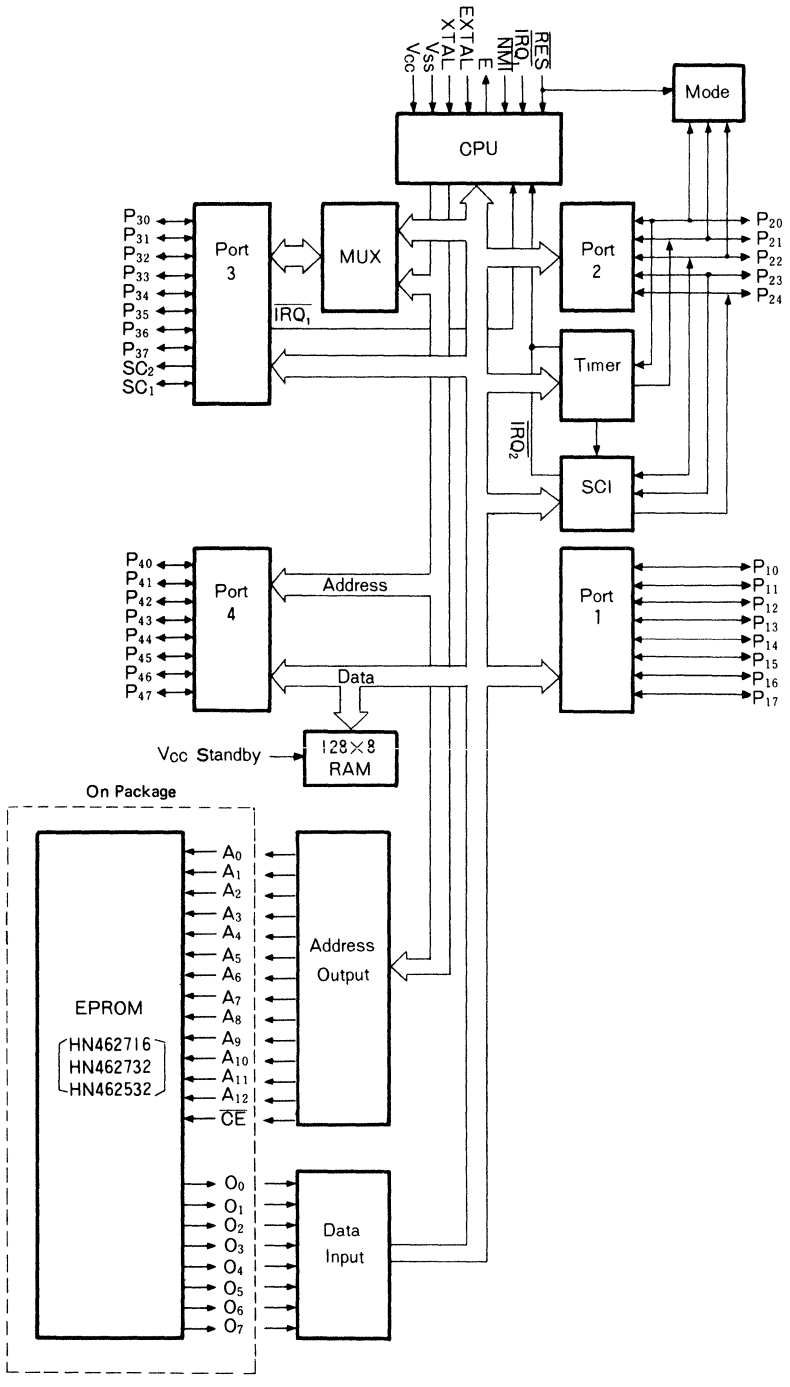
HD68P01S0



HD68P01V07



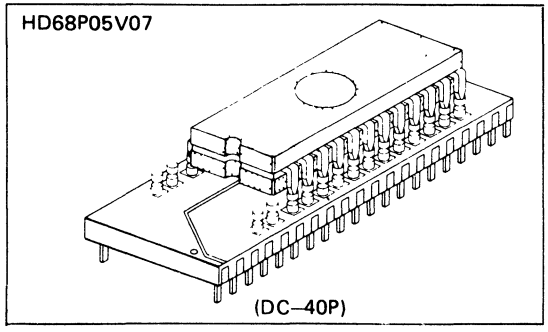
■ BLOCK DIAGRAM



HD68P05V07

MCU (Microcomputer Unit) PRELIMINARY

The HD68P05V07 is the 8-bit Microcomputer Unit (MCU) which contains a CPU, on-chip clock, RAM, I/O and Timer. It is designed for the user who needs an economical microcomputer with the proven capabilities of the HD6800-based instruction set. Setting EPROM on the package, this MCU has the equivalent function as the HD6805U and HD6805V. HD68P05V07 uses HN462732 as EPROM. The following are some of the hardware and software highlights of the MCU:



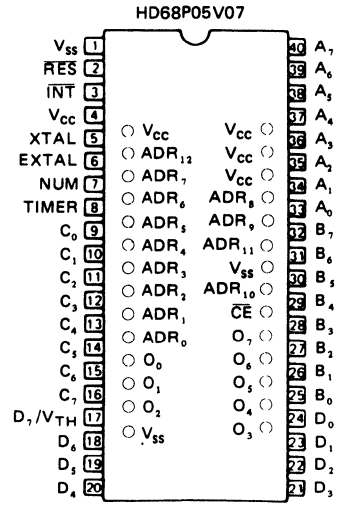
■ **HARDWARE FEATURES**

- 8-Bit Architecture
- 96 Bytes of RAM
- Memory Mapped I/O
- Internal 8-Bit Timer with 7-Bit Prescaler
- Vectored Interrupts – External, Timer and Software
- 24 I/O Ports + 8 Input Port
  (8 Lines LED Compatible; 7 Voltage Comparator Inputs)
- On-Chip Clock Circuit
- Master Reset
- Complete Development System Support by Evaluation Kit
- 5 Vdc Single Supply

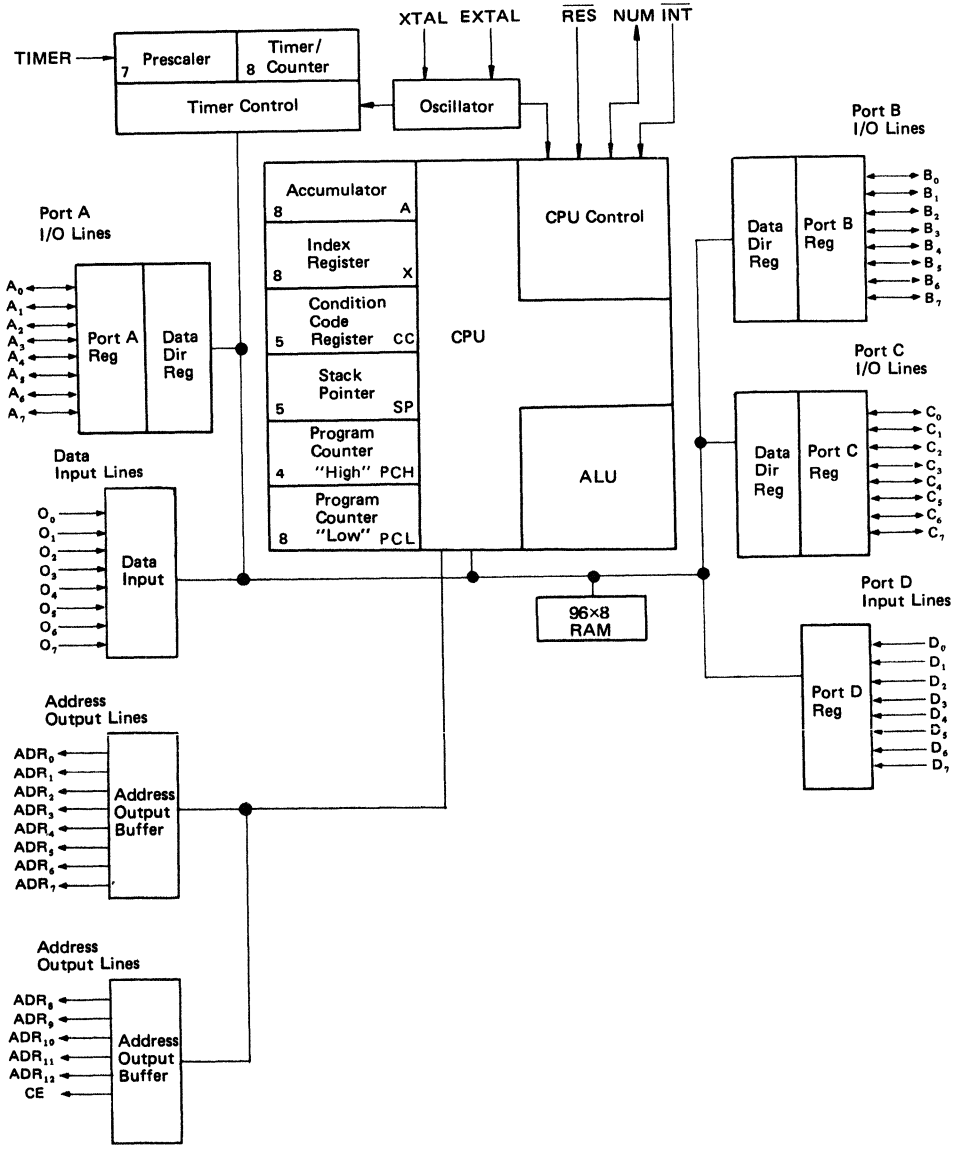
■ **SOFTWARE FEATURES**

- Similar to HD6800
- Byte Efficient Instruction Set
- Easy to Program
- True Bit Manipulation
- Bit Test and Branch Instructions
- Versatile Interrupt Handing
- Powerful Indexed Addressing for Tables
- Full Set of Conditional Branches
- Memory Usable as Registers/Flags
- Single Instruction Memory Examine/Change
- 10 Powerful Addressing Modes
- All Addressing Modes Apply to ROM, RAM and I/O
- Compatible Instruction Set with HD6805

■ **PIN ARRANGEMENT (Top View)**



■ BLOCK DIAGRAM



4-Bit Microcomputers-HMCS40 Series

Outline

Hitachi has introduced nine 4-bit single-chip microcomputers known as the HMCS40 series. They have found wide applications in both household and industrial fields. The following five new products have just been added to the line: HMCS47C (CMOS with 4k words of ROM); HMCS45A, HMCS44A and HMCS43 (PMOS for use with a ceramic filter type of oscillator); and the HMCS43S (PMOS 28-pin DIL with 1k word of ROM).

HMCS47C·CMOS with 4k words of ROM

The HMCS47C is an expanded ROM version of the HMCS45C, ROM capacity has been increased to 4,096 words, and RAM capacity to 256 x 4-bits. By doubling the operating frequency, the instruction cycle time has been decreased from 10μs to 5μs. The instruction set, pin arrangement and package type are the same as the HMCS45C. Table 1 compares the HMCS47C to the HMCS45C.

With increased memory capacity and operation speed, one HMCS47C can substitute for two chips of conventional smaller-capacity. Resulting in a decrease in systems cost and package area. A more sophisticated 42-pin variation, (the HMCS46S), is also under development.

HMCS45A/HMCS44A/HMCS43 PMOSs Incorporating Ceramic Filter Oscillator

The current HMCS45A, HMCS44A and HMCS43 work with conventional crystal type or external RC networks. They are now available incorporating oscillators compatible with external ceramic filters, thus offering a wide choice for users. Since the frequency stability of a ceramic filter oscillator falls within a ±2 percent range, these new products are suited for applications calling for high precision control. Figs. 1 and 2 show the difference in external oscillator components and pin arrangements. These new variations are identical with the current products in terms of functionality and electric characteristics.

The user can specify the desired oscillator type in the "I/O type specification form" that is to be filled out when ordering ROMs. When "incorporated RC oscillation" and "external" are specified, the ROM is masked using the conventional product with an RC oscillator. When "incorporated ceramic filter oscillation" is specified, the ROM is masked using the newly developed product with the ceramic filter oscillator.

HMCS43C·PMOS 1k word ROM 28-pin DIL

This is a variation of the current HMCS43. Input and output pins have been reduced been so it now comes in a 28-pin DIL package. It is suited for applications where wide I/O is not required and small devices package area is important. The standby function of the HMCS43 has been dropped. In all other respects, the HMCS43S is identical with the HMCS43. Fig. 3 shows the pin arrangement of the HMCS43S. Table 2 lists the main specifications differences of the new products.

Fig. 1. Difference in external oscillator component.

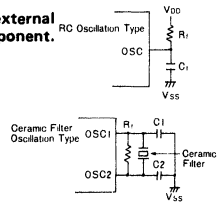


Table 1. Comparison between the H MCS47C and the HMCS45C

Description	HMCS47C	HMCS45C
ROM	4,096 x 10 bit (Program and pattern ROM undistinguished)	2,048 x 10 bit (Program ROM) 128 x 10 bit (Pattern ROM)
RAM	256 x 4 bit	160 x 4 bit
Instruction cycle time	5μs	10μs
Power consumed	1mA (typ)	0.4mA (typ)

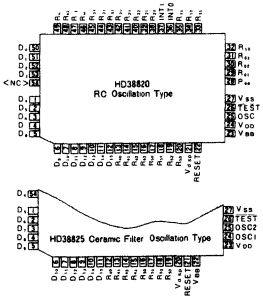


Fig. 2. Difference in pin arrangement between the RC oscillation type and ceramic filter oscillation.

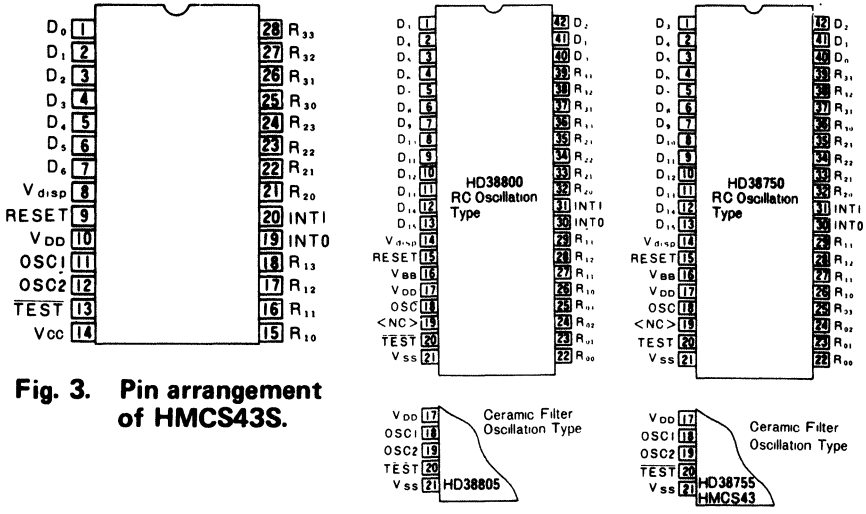


Fig. 3. Pin arrangement of HMCS43S.

Table 2. Key Specifications of the New HMCS40 Series

Classification / Description / Designation		HMCS47C HD44860	HMCS45A HD38825	HMCS44A HD38805	HMCS43 HD38755	HMCS43S HD38757	Unit
Process		CMOS	PMOS	PMOS	PMOS	PMOS	–
Package		FP–54	FP–54	DP–42	DP–42	DP–28	–
Supply voltage		5	-10	-10	-10	-10	V
Power consumption	In operation	1	17	17	11	11	mA
	On standby	0.01	2	2	1	–	mA
ROM	Program	4,096 x 10	2,048 x 10	2,048 x 10	1,024 x 10	1,024 x 10	bit
	Pattern		128 x 10	128 x 10	64 x 10	64 x 10	bit
RAM		256 x 4	160 x 4	160 x 4	80 x 4	80 x 4	bit
Stack register		4	4	4	3	3	–
Input/output		44	44	32	32	19	–
Interrupt	External	2	2	2	2	2	–
	Timer/counter	Provided	Provided	Provided	Provided	Provided	–
Standby function		Provided (Halt)	Provided (RAM hold)	Provided (RAM hold)	Provided (RAM hold)	–	–
On board oscillator		Provided	Provided	Provided	Provided	Provided	–
Power on reset		Provided	Provided	Provided	Provided	Provided	–

4-Bit Single-Chip HMCS40 Microcomputer Series

The HMCS40 Series are high-performance, low-cost 4-bit single-chip microcomputers designed for dedicated applications using PMOS, CMOS, or NMOS LSI process technologies.

The Instruction Set of each chip is consistent across the product line, allowing for easy expansion within the family.

FEATURES

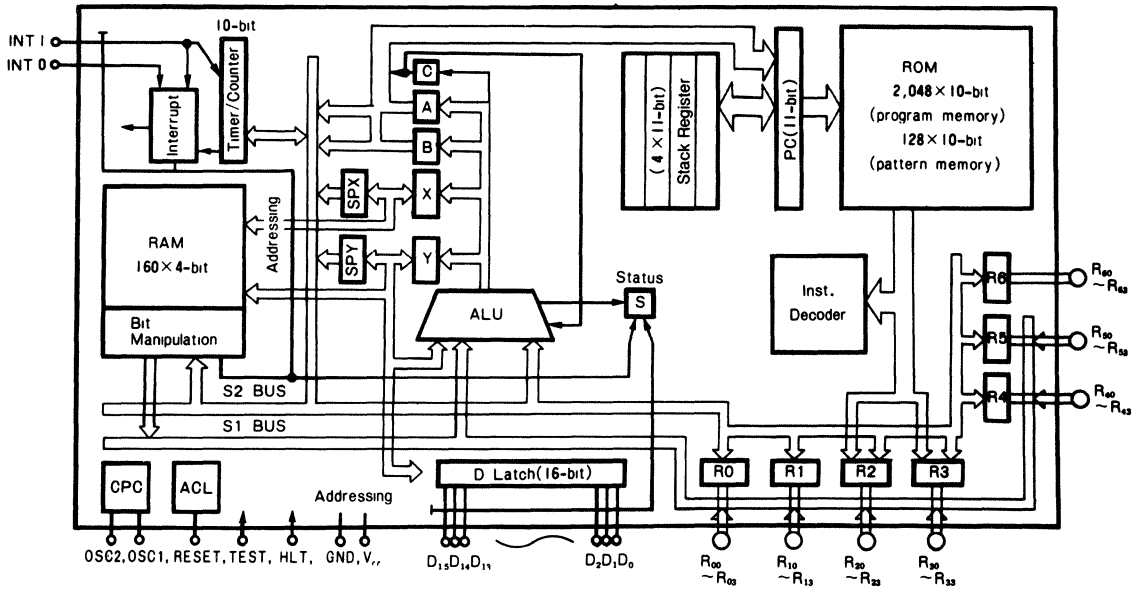
- A full line: PMOS/CMOS/NMOS
  0.5 ~ 4K words ROM
  32 ~ 256 words RAM
  22 ~ 44 I/O Lines
- All instructions (except one) are single-cycle
- Pattern generation instruction (table reference capability)
- Powerful interrupt function (except HMCS42/42C)
- Three interrupt sources { Two external interrupt lines / One timer/event counter
- High voltage output (50V): PMOS (for direct vacuum fluorescent drive)
- Low-power dissipation (2mW): CMOS
- High-speed (2μs cycle time): NMOS
- Built-in clock pulse generator (or you can use an external clock)
- Built-in power-on-reset circuitry
- Battery backup: PMOS and CMOS (except HMCS42)
- I/O options (user selectable at each pin)
  PMOS: pull-up resistor/open drain
  CMOS: pull-up resistor/open drain/CMOS output
  NMOS: pull-up resistor

HMCS40 SERIES PRODUCT CHARACTERISTICS

	Family Name		HMCS42	HMCS42C	HMCS43	HMCS43C	HMCS44A	HMCS44C	*HMCS44N
LSI Characteristics	Process		PMOS	CMOS	PMOS	CMOS	PMOS	CMOS	NMOS
	Supply Voltage	(V)	-10	5	-10	5	-10	5	5
	Power Dissipation	(mW)	100	1.5	100	2	150	2	450
	Max. I/O Terminal Voltage	(V)	-50	10****	-50	10****	-50	10****	5
	Output Characteristics		1.8V/10mA 1.8V/3mA	2.4V/-1mA 0.8V/1.6mA	1.8V/10mA 1.8V/3mA	2.4V/-1mA 0.8V/1.6mA	1.8V/10mA 1.8V/3mA	2.4V/-1mA 0.8V/1.6mA	1.6mA/0.4V
	Operating Temperature Range	(°C)	-20~+75**	-20~+75**	-20~+75**	-20~+75**	-20~+75**	-20~+75**	-20~+75**
	Package		DP-28	DP-28	DP-42	DP-42	DP-42	DP-42	DP-42
Function	Memory	ROM (bits)	512x10 32x10***	512x10 32x10***	1,024x10 64x10***	1,024x10 64x10***	2,048x10 128x10***	2,048x10 128x10***	2,048x10 128x10***
		RAM (bits)	32x4	32x4	80x4	80x4	160x4	160x4	160x4
	Registers		4	4	6	6	8	8	6
	Stack Registers		2	2	3	3	4	4	4
	I/O Ports	Data Input	22 4x1	22 4x1	32 4x1	32 4x1	32 –	32 –	32 –
		Discrete Input	–	–	–	–	–	–	–
		Data Output	4x2	4x2	4x2	4x2	–	–	–
		Discrete Output	1x6	1x6	1x12	1x12	–	–	–
		Data Input/Output	–	–	4x1	4x1	4x4	4x4	4x4
		Discrete Input/Output	1x4	1x4	1x4	1x4	1x16	1x16	1x16
	Interrupts	External	–	–	2	2	2	2	2
		Timer	–	–	Yes	Yes	Yes	Yes	Yes
		Event Counter	–	–	Yes	Yes	Yes	Yes	Yes
	Instructions	Number of Instructions	51	51	71	71	71	71	71
		Cycle Time (μs)	10	10	10	10	10	10	2
	Clock Pulse Generator		Yes (External)						
	Power on Reset								
	Battery Backup		–	Halt	RAM Hold			Halt	–
Evaluation Chip			HD38750E HD44850E	HD44850E	HD38750E HD44850E	HD44850E	HD44850E	HD44850E	*HD44860E

* Under Development.
** – 40 ~ + 85 °C (Special Request); please contact Hitachi America, Ltd.
*** Pattern Memory
**** Applied to NMOS open drain outputs Supply Voltage + 0 3 (V) is applied to other pins

HMCS45C BLOCK DIAGRAM



OUTLINE OF THE HMCS40 SERIES

HMCS45A	HMCS45C	*HMCS46C	HMCS47C
PMOS	CMOS	CMOS	CMOS
-10	5	5	5
150	2	4	4
-50	10****	5	5
1.8V/10mA 1.8V/3mA	2.4V/-1mA 0.8V/1.6mA	2.4V/-1mA 0.8V/1.6mA	2.4V/-1mA 0.8V/1.6mA
-20~+75**	-20~+75**	-20~+75**	-20~+75**
FP-54	FP-54	DP-42	FP-54
2,048x10 128x10***	1,048x10 128x10***	4,096x10	4,096x10
160x4	160x4	256x4	256x4
6	6	6	6
4	4	4	4
44: –	44: –	32: –	44: –
44: –	44: –	32: –	44: –
44: 4x1	44: 4x1	32: –	44: 4x1
44: –	44: –	32: –	44: –
44: 4x6	44: 4x6	32: 4x4	44: 4x6
44: 1x16	44: 1x16	32: 1x16	44: 1x16
2	2	2	2
Yes	Yes	Yes	Yes
Yes	Yes	Yes	Yes
71	71	71	71
10	10	5	5
Yes (External)			
RAM Hold: Halt		Halt	Halt
HD44850E		HD44855E	

LCD Drive Devices-LCD-II and LCD-III

HITACHI HLN2000 LITERATURE NO.

HITACHI HLN2001 LITERATURE NO.

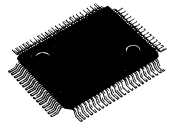
The use of liquid crystal display (LCD) devices has long been limited to pocket computers and watches. They have recently found increasingly wide acceptance in home appliances, industrial equipment and many other types of consumer equipment. LCDs have many merits, such as lower power consumption, freedom in display pattern design, abundant information resulting from high-density patterns, and easy interface formation with MOS devices. When combined with power-efficient CMOS devices, LCD is become particularly suited for use in equipment requiring battery drive or backup. With the development of multi-color LCDs, improvement in time-division drive characteristic, expansion of operating temperature, and other improvements, LCDs will be applied to an ever widing variety of products and fields. Hitachi has developed the LCD-III machine, a 4-bit CMOS microcomputer containing the LCD drive circuitry, Hitachi has also developed the LCD-II, a controller driver circuit employing a dot matrix type of cutout for English and numeric characters, and the HD44100, which is a driver circuit that can be connected to a LCD-II or LCD-III device to enlarge their display function, the HD44100 may be connected to any microcomputer to enable it to give a liquid crystal display.

Time Division	Liquid Crystal Display: Operation Margin	Display Quality	Signal Line Required
Small (Duty ratio high)	Wide	High	Many
Large (Duty ratio low)	Narrow	Low	Few

Table 1. Functions and Characteristics of LCD-III

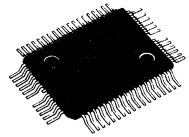
Description		Specification	
Designation		HD44790	HD44795
Process		CMOS	
Supply voltage		5V	3V
Instruction cycle		10μs	20μs
Power consumption		0.4mA	0.1mA
Package		80-pin flat package	
Function		4-bit single chip microcomputer with LCD drive circuitry	
ROM	Program	2,048-word x 10-bit	
	Pattern	128-word x 10-bit	
RAM	Data RAM	160-word x 4-bit	
	Display RAM		
Stack register		4	
Input/output	4-bit data	4-bit x 4	
	1-bit discrete data	1-bit x 16	
Interruption	Input	2	
	Timer/counter	Provided	Crystal oscillation for timer
LCD drive	Scanning spot (common)	4	
	Signal line (segment)	32	Extendable to 96 segments
	Duty ratio	1/4, 1/3, 1/2, static	
	Bias	1/3, 1/2	
	Display method	Program-generated LCD RAM segment data is automatic	

LCD-II, LCD-III



80 Pin Flat Plastic Package

HD44100



60 Pin Flat Plastic Package

LCD-III (HD44790 and HD44795)

• Microcomputer Function

The microcomputer function of the LCD-III is equivalent to that of the HMCS44C, a device in the HMCS40 series. Complete with 32 general-purpose I/O lines 2 external interrupt inputs, and a timer-counter, the LCD-III can perform powerful control and arithmetic functions. With an on-chip oscillator or external crystal the clock function is easily realized. The incorporated standby (or holding) function permits design of extremely a power-efficient systems.

• LCD Function

The number of display divisions is important to LCD devices and their relationship can be expressed as follows:

With the LCD-III a user can choose the optimum duty ratio from 1/4, 1/3, 1/2 and static based, so the best-suited value can be set for each application. The LCD-III contains 32 signal lines (for segment signals), which can be expanded to 96 by specifying the extension mode (program option) and connecting the HD44100 externally. Since all display data are generated by the program, 7-segment, 14-segment, or graphic displays can be efficiently realized.

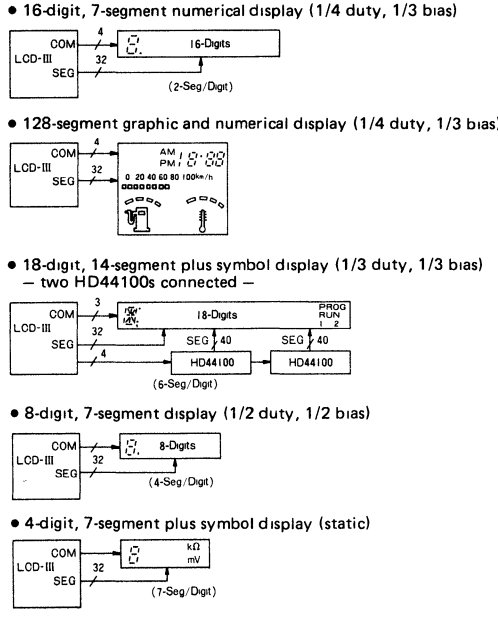


Fig. 1. Examples of LCD-III's liquid crystal display.

- **Development Support Tools**

Since the instruction set of the LCD-III is identical with that of the HMCS40 series, full use of programs for these can be used. All cross software and the low cost H40EVKIT (program development system) are directly applicable to the LCD-III. All the user need buy is the evaluation board (H40LCEV00) for the LCD-III. New program can be HE or CE developed economically and efficiently.

- **Cross Assembler**

For use with the IBM360, IBM370, Intel MDS, Motorola EXORciser, H68SD5.

- **Evaluation Board**

H40LCEV00

- **Program Development System**

Combination of H40EVKIT and H40LCEV00

LCD-II (HD44780)

- **Outline**

The LCD-II is a CMOS controller-driver circuit that drives a 5 x 7-dot or 5 x 10-dot English and numerical dot matrix liquid crystal display according to the character data received from a 4-bit or 8-bit microcomputer. It contains all display functions needed for the display data RAM, character generators ROM and RAM, scanning spot drive circuit, and signal line drive circuit. It is most often applied to make up an English and numerical dot matrix type LCD system.

- **Functions and Characteristics**
  - Power-efficient CMOS process
  - 80-pin flat plastic package
  - Character data RAM ..... 80-word x 8-bit (80 digits)
  - Large-capacity character generator ROM

    5 x 7-dot ..... 160 ┐
    5 x 10-dot ..... 32 ┘ 192

    Rewritable according to the user's request.

- **Character generator RAM (512-bit)**

  5 x 7-dot 8
  5 x 10-dot 4

  The character pattern written from the CPU enables free character display.

- **Abundant instruction functions**

The instruction functions include full character data RAM clearing, cursor control, display shift and display blinking.

- **Display output**

  Scanning spot ..... 16 (Duty ratio 1/8, 1/11 and 1/16)
  Signal line ... 40 (Extandable to 360 by external connection of the HD44100 outside)

- **No. of displayable digits**

Duty Ratio	Type Face	LCD-II Alone	Expansion by each HD44100	Maximum
1/8	5 x 7 dots	8 digits	8 digits	80 digits
1/11	5 x 10 dots	8 digits	8 digits	80 digits
1/16	5 x 7 dots	16 digits	16 digits	80 digits

- **Exchangeable with 4-bit and 8-bit CPU interface programs**

- **Applications**

Portable computer, word processors, portable terminal equipment, electronic translators, electronic typewriters, general-purpose data terminals, industrial controllers, etc.

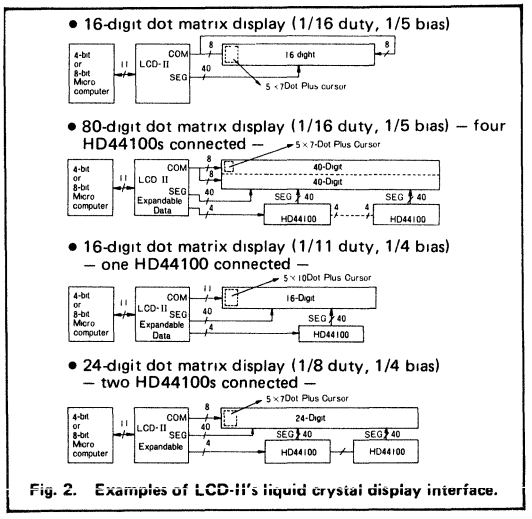


Fig. 2. Examples of LCD-II's liquid crystal display interface.

HD44100

- **Outline**

The HD44100 is a CMOS driver circuit incorporating two channels of 20-bit bidirectional shift register, latch, and liquid crystal display drive circuit. Receiving serial data from a CPU or controller circuit, the HD44100 latches and converts the data into liquid crystal display drive waveform. When two channels are connected in series. The HD44100 may be used as a 40-signal-line drive circuit. It can also give time-division display by using one channel for scanning spot drive and the other for signal line drive. When a plurality of HD44100s are connected, a large-capacity LCD circuit results.

- **Functions and Characteristics**
  - Power-efficient CMOS process
  - 60-pin flat plastic package
  - 20-bit bidirectional shift register, latch and liquid crystal display drive circuit x 2 channels
  - Freely selectable display duty ratio and bias
  - Large-capacity display permitting series connection

- Interface for CPU or controller circuit ..... 1 for serial data and 3 for control signal
- Functions required of CPU or control circuit ..... display data generation and serial transfer to HD44100, control of display timing

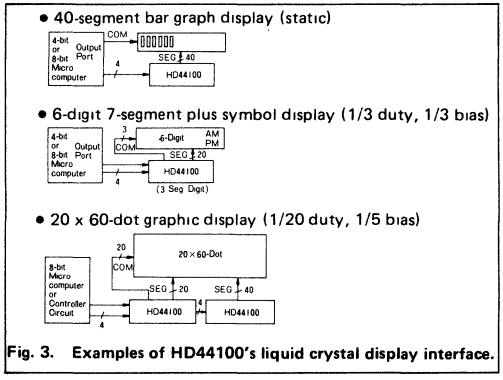


Fig. 3. Examples of HD44100's liquid crystal display interface.

Software/Hardware Development Systems

Hitachi Development Systems enable a user to develop complete integrated hardware and suitable software with considerable efficiency.

Support capabilities are provided from complete systems to low-cost evaluation kits and cross assemblers. The user can select the most suitable tools from the Hitachi lineup. Hitachi's resident engineering group can also design user application software upon request.

Development Systems for HMCS40 Series

SUPPORT HARDWARE

HMCS40 Series support hardware allows development and debugging of users software for the 4-bit microcomputer family

HMCS40 SERIES SUPPORT SOFTWARE

HMCS40 Series cross assemblers allow development of 4-bit microcomputer software utilizing the customer's existing development equipment in a "host computer" mode

EVALUATION KITS

H40EVKIT H40EVKIT2 (under development)

The Evaluation Kit is a single board-type development tool that includes "debugger," "assembler," and "text editor" functions When a TTY is connected, functionality expands to all program development (up to prototype hardware debugging)

CROSS ASSEMBLERS

Type Number	Host Computer	Media	Source Program Format	Object Program Format
S40XAM1	32-Bit HITACHI-M Series	MT Memory 100K Byte	Card	Paper Tape
S40XAM1	32-Bit IBM 370	MT Memory 100K Byte	Card	Paper Tape
S40EXR1	8-Bit Motorola EXORcisor-II	Floppy Disk	Floppy Disk	EPROM
S40MDS1	8-Bit Intel MDS220/230	Floppy Disk	Floppy Disk	EPROM
S40XAE-1	8-Bit H40EVKIT 6800 Base	EPROM Memory 4K Byte	Paper Tape	Paper Tape

EVALUATION BOARDS

H43EV00 H45CEV00
H40LCEV00 H40NEV00 (under development)
H47CEV00 (under development)

The Evaluation Board consists of an evaluation chip and sockets for EPROM Program evaluation and operation (in-circuit emulation) of prototype hardware is possible by connecting the card through an edge connector to the users prototype hardware.

EVALUATION CHIPS

HD38750E HD44850E
HD44855E HD44860E

Evaluation Chips are ROM-less versions of the HMCS40 Family Program evaluation· operational check of prototype hardware single-step debugging is possible.

Note: HD44855E is a universal chip External PMOS level translation is required to emulate PMOS microcomputers

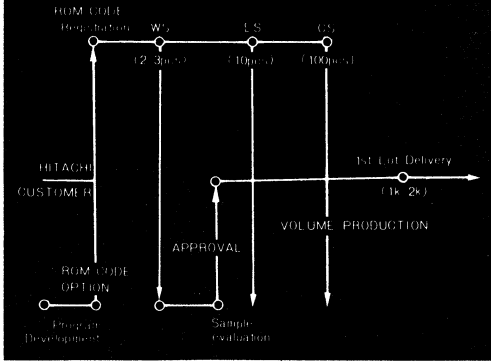
HMCS40 Series Support System Lineup

Tool	Family / Type	PMOS				CMOS							NMOS
		42	43	44A	45A	42C	43C	44C	45C	46C	47C	LCD-III	44N
Evaluation Kit	H40EVKIT	•	•	•	•	•	•	•	•			•	
	H40EVKIT2*									•	•		•
Evaluation Board	H43EV00	•	•										
	H45CEV00	•	•	•	•	•	•	•	•				
	H47CEV00*									•	•		
	H40NEV00*												•
	H40LCEV00											•	
Evaluation Chip	HD38750E	•	•										
	HD44850E	•	•	•	•	•	•	•	•				
	HD44855E									•	•	•	
	HD44860E*												•

* Under Development.

Hitachi 4-Bit/8-Bit Single-Chip Microcomputer Development Schedule

1. Development Schedule



2. Remarks

- Hitachi's manufacturing process starts upon receipt of customer's ROM code and I/O option list.
- Customer's program media (ROM code): three sets of EPROMs or paper tapes.
- WS: working samples (first run parts suitable for checking device functionality).
- ES: engineering samples (qualification grade devices).
- CS: commercial samples (first production delivery).
- WS and ES units provided free of charge (part of mask cost).
- ROM code should be submitted only after full debugging and simulation . . . changes in ROM code require a new mask charge.
- Detailed schedule: please contact Hitachi America, Ltd.

Hitachi Single Chip H68SD5 Microcomputer Development System

The H68SD5 is a development system for HITACHI 4-bit and 8-bit single chip microcomputers.
It is an all-in-one type compact HD6800 based CRT/Key board microcomputer terminal with one Floppy disk driver and has standard interface for the TTY (RS-232C or TTL level) and printer (Centronics parallel interface). The EPROM writer and the second Floppy disk driver are optionally available.

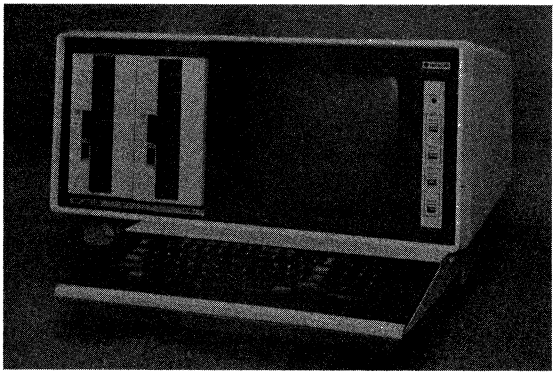
Features

- Supports the system development for 8-bit and 4-bit single chip microcomputers – HD6801/6301 series, HD6805/6305 series and HMCS 40 series
- Disk based low cost system
- Provides the Text Editor, Assembler, Emulator and EPROM Writer controlled by FDOS-III
- 56K-byte RAMs
- Allows linking between the H68SD5 and the I/O devices (TTY and Printer)
- Easy to debug user's prototype system using the Emulator Module

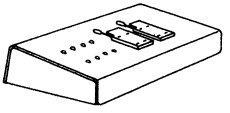
SYSTEM CONFIGULATION

H68SD5

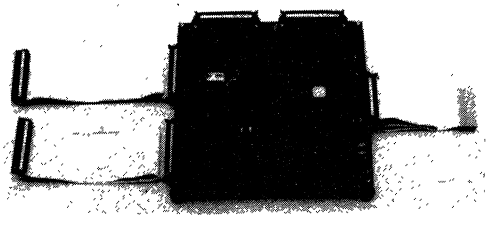
FDD* FDD



*OPTION

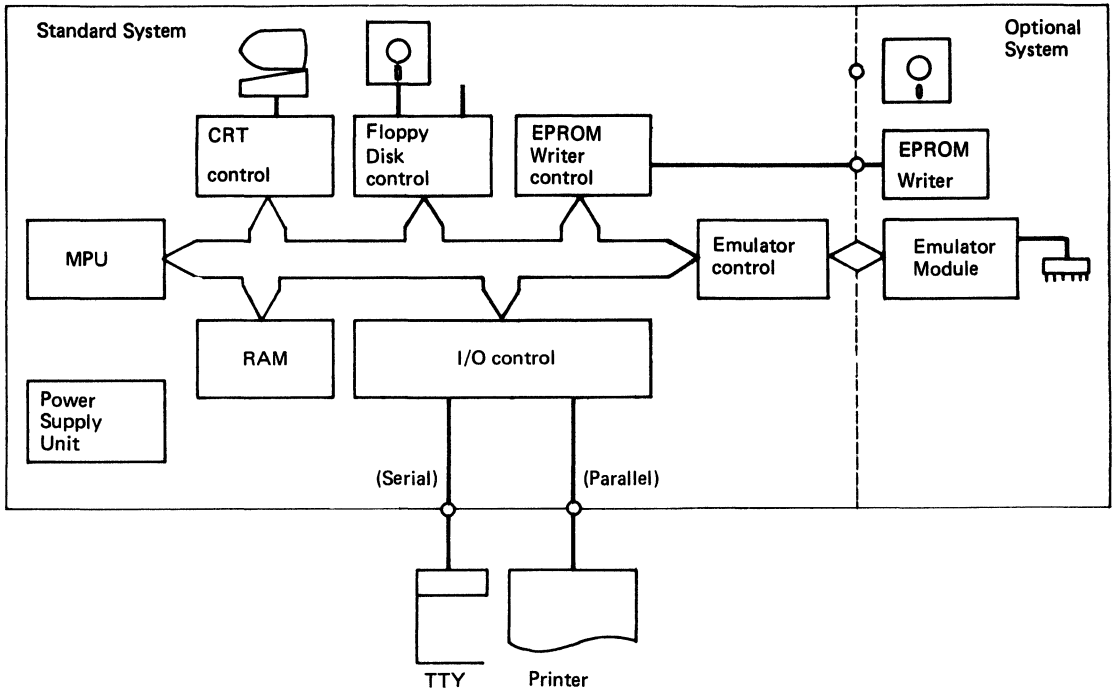


EPROM WRITER*



EMULATOR MODULE* (HD6801/6301 series / HD6805/6305 series / HMCS40 series)

■ Hardware

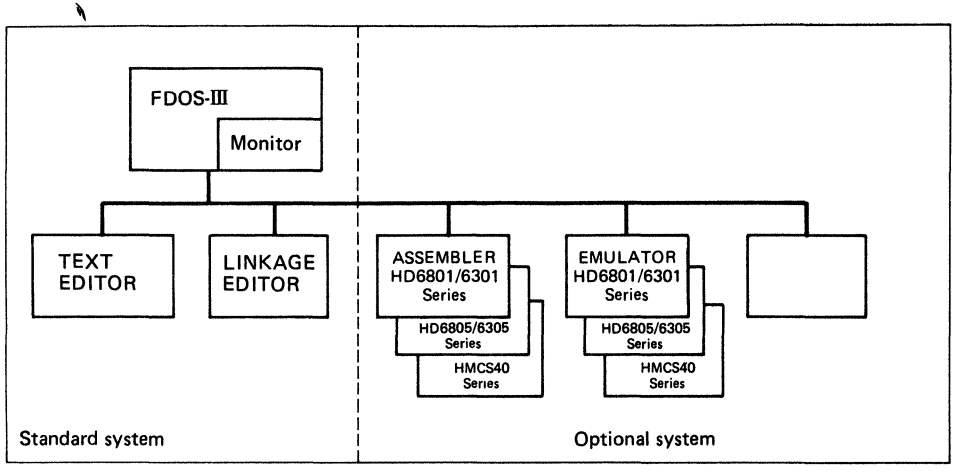


As shown in the above figure, the standard system of the H68SD5 consists of a power supply unit, 7 function blocks, a console display and one Floppy disk driver. User's system can be developed easily with this Floppy disk based system.
It is possible to emulate user's prototype system by linking the Emulator Module which is provided for each single chip microcomputer.

The functions of the Emulator Module are as follows.

- Direct link to user's system
- Provides the I/O ports, ROM and RAM which emulate the internal operation of the MCU (Microcomputer Unit)
- Eight break points
- Reset and abort functions
- Object program load/punch

■ Software



Software functions

Monitor

The monitor is core for operation of the H68SD5

- Controls the FDOS-III and I/O devices

FDOS-III

The FDOS-III is the operating system which controls the H68SD5.

- Allows Floppy disk based operation (from programming through debugging)
- Allows conversational operation with the CRT/Keyboard

Assembler

The Assembler converts a source program to an object program in an absolute/relocatable form.

Text Editor

The Text Editor allows modifying and editing of a source program.

- Allows a delete and insert of a statement
- Allows a change and search of a character string

Linkage Editor

The Linkage Editor allows relocation and linking of relocatable objects generated by the Assembler (Only for HD6801/6301 series)

Emulator

The Emulator is used for software debugging and user's prototype system emulation.

- Provides displaying and changing the contents of registers/memory
- Provides setting, displaying and changing break points
- Allows user's program trace and single-step execution

EPROM Writer

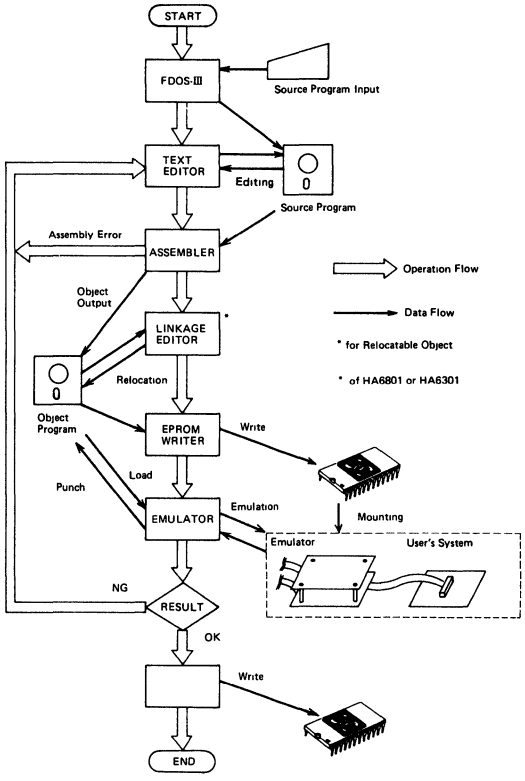
The EPROM Writer writes a program into the EPROM.

- For the HN462532, HN462716, HN462732 and HN48016
- Verifies data written in the EPROM
- Allows copying from an EPROM to another one
- Blank check

■ Specification

Item	Specification
Main board	MPU: HD6800 RAM: 56K-byte dynamic RAM Monitor: 4K-byte ROM
Floppy disk driver	Memory capacity: Approx. 250K-byte (77 tracks, 26 sector, 128 byte) Format: FDOS recording format based on IBM 3740 data format Recording density: 3268 BPI (bit per inch)
Console display	Picture size: 12 inches, black/green Display form: Laster scan Display character numbers: 80 characters x 24 lines
I/O interface	TTY (Serial interface) Printer (Centronics parallel interface)
Power supply	Voltage: AC90V to 127V or AC180V to 254V Frequency: 50Hz, 60Hz ±1Hz
Temperature	Operating: 10°C to 35°C Storage: -10°C to 50°C
Humidity	Operating: 20% to 80% RH (without dew) Storage: 10% to 80% RH (without dew)
Expansion equipment	EPROM Writer Emulator Module

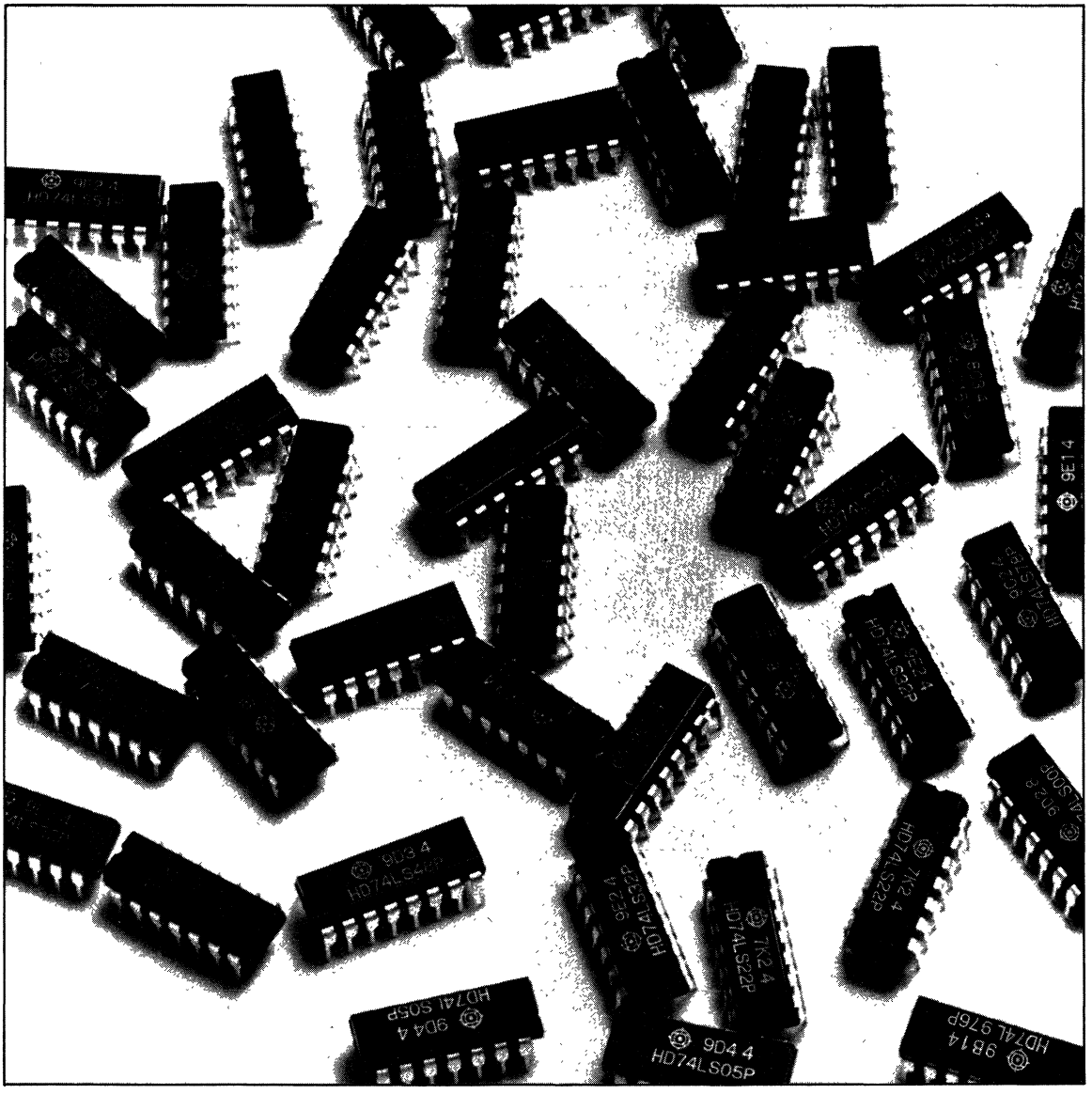
■ Procedure of Program Development



Note) The specifications of this system are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

SECTION 4

BIPOLAR LOGIC



HITACHI

74LS LOGIC FAMILY

74LS PRODUCT LINE BY PART NUMBER

CAT NO.	DESCRIPTION
HD74LS00	Quadruple 2-input Positive NAND Gates
HD74LS01	Quadruple 2-input Positive NAND Gates (with open collector outputs)
HD74LS02	Quadruple 2-input Positive NOR Gates
HD74LS03	Quadruple 2-input Positive NAND Gates (with open collector outputs)
HD74LS04	Hex Inverters
HD74LS05	Hex Inverters (with open collector outputs)
HD74LS08	Quadruple 2-input Positive AND Gates
HD74LS09	Quadruple 2-input Positive AND Gates (with open collector outputs)
HD74LS10	Triple 3-input Positive NAND Gates
HD74LS11	Triple 3-input Positive AND Gates
HD74LS12	Triple 3-input Positive NAND Gates (with open collector outputs
HD74LS13	Dual 4-input Positive NAND Schmitt Triggers
HD74LS14	Hex Schmitt Trigger Inverters
HD74LS15	Triple 3-input AND Gates (with open collector outputs)
HD74LS20	Dual 4-input Positive NAND Gates
HD74LS21	Dual 4-input Positive AND Gates
HD74LS22	Dual 4-input Positive NAND Gates (with open collector outputs)
HD74LS26	Quadruple 2-input High-voltage Interface NAND Gates
HD74LS27	Triple 3-input Positive NOR Gates
HD74LS30	8-input Positive NAND Gates
HD74LS32	Quadruple 2-input Positive OR Gates
HD74LS37	Quadruple 2-input Positive NAND Buffers
HD74LS38	Quadruple 2-input Positive NAND Buffers (with open collector outputs)
HD74LS40	Dual 4-input Positive NAND Buffers
HD74LS42	BCD-to-Decimal Decoders
HD74LS47	BCD-to-Seven Segment Decoders/-Drivers (with 15V outputs)
HD74LS48	BCD-to-Seven Segment Decoders/Drivers
HD74LS49	BCD-to-seven Segment Decoders/Drivers
HD74LS51	2-wide 2-input, 2-wide 3-input AND-OR-INVERT Gates
HD74LS54	4-wide 2-input, 3-input AND-OR-INVERT Gates
HD74LS55	2-wide 4-input AND-OR-INVERT Gates
HD74LS73	Dual J-K Negative Edge-triggered Flip-Flops (with clear)
HD74LS74A	Dual D-type Positive Edge-triggered Flip-Flops
HD74LS75	Quadruple Latches
HD74LS76	Dual J-K Negative Edge-triggered Flip-Flops (with Preset and clear)
HD74LS77	4-bit Bistable Latches
HD74LS78	Dual J-K Negative Edge-triggered Flip-Flops (with preset, common, clear, and common clock)
HD74LS83A	4-bit Binary Full Adders
HD74LS85	4-bit Magnitude Comparators
HD74LS86	Quadruple Exclusive-OR Gates
HD74LS90	Decade Counters
HD74LS91	8-bit Shift Registers
HD74LS92	Divide-by-Twelve Counters
HD74LS93	4-bit Binary Counters
HD74LS95B	4-bit Shift Registers
HD74LS96	5-bit Shift Registers (Dual parallel-in, parallel-out)
HD74LS107	Dual J-K Negative Edge-triggered Flip-Flops (with clear)
HD74LS109A	Dual J-K Negative Edge-triggered Flip-Flops (with preset and clear)
HD74LS112	Dual J-K Negative Edge-triggered Flip-Flops (with preset and clear)
HD74LS113	Dual J-K Negative Edge-triggered Flip-Flops (with preset)
HD74LS114	Dual J-K Negative Edge-triggered Flip-Flops (with preset, common clock, and common clear)
HD74LS122	Retriggerable Monostable Multivibrators (with clear)
HD74LS123	Dual Retriggerable Monostable Multivibrators (with clear)
HD74LS125A	Quadruple Bus Buffer Gates with three-state outputs (inverting)
HD74LS126A	Quadruple Bus Buffer Gates with three-state outputs (noninverting)
HD74LS132	Quadruple 2-input NAND Schmitt Triggers
HD74LS136	Quadruple Exclusive-OR Gates (with open collector outputs)
HD74LS138	3-to-8-line Decoders/Demultiplexers
HD74LS139	Dual 2-to-4-line Decoders/Demultiplexers
HD74LS145	BCD-to-Decimal Decoders/Drivers (with 15V outputs)
HD74LS148	8-to-3-line Octal Priority Encoders
HD74LS151	1-of-8-line Data Selectors/Multiplexers
HD74LS152	1-of-8-line Data Selectors/Multiplexers

74LS LOGIC FAMILY

74LS PRODUCT LINE BY PART NUMBER

CAT NO.	DESCRIPTION
HD74LS153	Dual 4-to-1-line Data Selectors/Multiplexers
HD74LS154	4-to-16-line Data Selectors/Multiplexers
HD74LS155	Dual 2-to-4-line Decoders/Demultiplexers
HD74LS156	Dual 2-to-4-line Decoders/Demultiplexers (with open collector outputs)
HD74LS157	Quadruple 2-to-1-line Data Selectors/Multiplexers
HD74LS158	Quadruple 2-to-1-line Data Selectors/Multiplexers
HD74LS160	Synchronous Decade Counters
HD74LS161	Synchronous 4-bit Binary Counters
HD74LS162	Fully Synchronous Decade Counters
HD74LS163	Fully Synchronous 4-bit Binary Counters
HD74LS164	8-bit Parallel-out Shift Registers
HD74LS173	4-bit D-type Registers (with three-state outputs)
HD74LS174	Hex D-type Flip-Flops (with clear)
HD74LS175	Quadruple D-type Flip-Flops (with clear)
HD74LS181	Arithmetic Logic Unit/Function Generators
HD74LS190	Synchronous Up/Down Decade Counters (single clock line)
HD74LS191	Synchronous Up/Down 4-bit Binary Counters (single clock line)
HD74LS192	Synchronous Up/Down Decade Counters (dual clock lines)
HD74LS193	Synchronous Up/Down 4-bit Binary Counters (dual clock lines)
HD74LS194A	4-bit Bidirectional Universal Shift Registers
HD74LS195A	4-bit Parallel Access Shift Registers
HD74LS221	Dual Monostable Multivibrators (with Schmitt trigger inputs)
HD74LS240	Octal Buffers/Line Drivers/Line Receivers (inverted three-state outputs)
HD74LS241	Octal Buffers/Line Drivers/Line Receivers (noninverted three-state outputs)
HD74LS242	Quadruple Bus transceivers (wtih three-state outputs)
HD74LS243	Quadruple Bus Transceivers (with three-state outputs)
HD74LS244	Octal Buffers/Line Drivers/Line Receivers (noninverted three-state outputs)
HD74LS245	Octal Bus Transceivers (noninverted three-state outputs)
HD74LS247	BCD-to-Seven Segment Decoders/Drivers (with 15V outputs)
HD74LS248	BCD-to-Seven Segment Decoders/Drivers
HD74LS249	BCD-to-Seven Segment Decoders/Drivers
HD74LS251	1-of-8-line Data Selectors/Multiplexers (with three-state outputs)
HD74LS253	Dual Data Selectors/Multiplexers (with three-state outputs)
HD74LS257	Quadruple 2-to-1-line Data Selectors/Multiplexers (with three-state outputs)
HD74LS258	Quadruple 2-to-1-line Data Selectors/Multiplexers (with three-state outputs)
HD74LS259	8-bit Addressable Latches
HD74LS266	Quadruple 2-input Exclusive-NOR Gates (with open collector outputs)
HD74LS279	Quadruple $\overline{S}$-$\overline{R}$ Latches
HD74LS280	9-bit Odd/Even Parity Generators/Checkers
HD74LS283	4-bit Binary Full Adders
HD74LS290	Decade Counters
HD74LS293	4-bit Binary Counters
HD74LS295B	4-bit Right-shift, Left-shift Registers (with three-state outputs)
HD74LS298	Quadruple 2-input Multiplexers (with storage)
HD74LS299	8-bit Universal Shift/Storage Registers (with three-state outputs)
HD74LS365A	Hex Bus Buffers/Drivers (with three-state outputs)
HD74LS366A	Hex Bus Buffers/Drivers (with three-state outputs)
HD74LS367A	Hex Bus Drivers (with three-state outputs)
HD74LS368A	Hex Bus Drivers (with three-state outputs)
HD74LS375	Quadruple Bistable Latches
HD74LS386	Quadruple 2-input Exclusive-OR Gates
HD74LS390	Dual 4-bit Decade Counters
HD74LS393	Dual 4-bit Binary Counters
HD74LS490	Dual 4-bit Decade Counters
HD74LS668	Synchronous Decade Up/Down Counters
HD74LS669	Synchronous 4-bit Binary Up/Down Counters

74LS LOGIC FAMILY

74LS PRODUCT LINE BY FUNCTION

CAT NO.	DESCRIPTION
■ NAND/NOR/AND/OR Gates	
HD74LS00	Quad. 2-input Positive NAND Gates
HD74LS01	Quad. 2-input Positive NAND Gates (with open collector outputs)
HD74LS02	Quad. 2-input Positive NOR Gates
HD74LS03	Quad. 2-input Positive NAND Gates (with open collector Gates
HD74LS04	Hex Inverters
HD74LS05	Hex Inverters (with open collector outputs)
HD74LS08	Quad. 2-input Positive AND Gates
HD74LS09	Quad. 2-input Positive AND Gates (with open collector outputs)
HD74LS10	Triple 3-input Positive NAND Gates
HD74LS11	Triple 3-input Positive AND Gates
HD74LS12	Triple 3-input Positive NAND Gates (with open collector outputs)
HD74LS13	Dual 4-input Schmitt NAND Gates
HD74LS14	Hex Schmitt-trigger Inverters
HD74LS15	Triple 3-input Positive AND Gates (with open collector outputs)
HD74LS20	Dual 4-input Positive NAND Gates
HD74LS21	Dual 4-input Positive AND Gates
HD74LS22	Dual 4-input Positive NAND Gates (with open collector outputs)
HD74LS26	Quad. 2-input High-voltage Interface NAND Gates
HD74LS27	Triple 3-input Positive NOR Gates
HD74LS30	8-input Positive NAND Gates
HD74LS32	Quad. 2-input Positive OR Gates
HD74LS37	Quad. 2-input Positive NAND Buffers
HD74LS38	Quad. 2-input Positive NAND Buffers (with open collector outputs)
HD74LS40	Dual 4-input Positive NAND Buffers
HD74LS125A	Quad. Bus Buffer Gates with three-state outputs (inverting)
HD74LS126A	Quad. Bus Buffer Gates with three-state outputs (noninverting)
HD74LS132	Quad. 2-input Positive NAND Schmitt Triggers
■ AND-OR-INVERT Gates	
HD74LS51	2-wide 2-input, 2-wide 3-input AND-OR-INVERT Gates
HD74LS54	4-wide 2-input, 3-input AND-OR-INVERT Gates
HD74LS55	2-wide 4-input AND-OR-INVERT Gates
■ BUS BUFFERS/DRIVERS/TRANSCEIVERS	
HD74LS240	Octal Buffers/Line Drivers/Line Receivers (inverted three-state outputs)
HD74LS241	Octal Buffers/Line Drivers/Line Receivers (noninverted three-state out.)
HD74LS242	Quad. Bus Transceivers (with three-state outputs)
HD74LS243	Quad. Bus Transceivers (with three-state outputs)
HD74LS244	Octal Buffers/Line Drivers/Line Receivers (inverted three-state outputs)
HD74LS245	Octal Bus Transceivers (with noninverted three-state outputs)
HD74LS365A	Hex Bus Buffers/Drivers (with three-state outputs)
HD74LS366A	Hex Bus Buffers/Drivers (with three-state outputs)
HD74LS367A	Hex Bus Buffers/Drivers (with three-state outputs)
HD74LS368A	Hex Bus Buffers/Drivers (with three-state outputs)
■ FLIP-FLOPS	
HD74LS73	Dual J-K Flip-Flops
HD74LS74A	Dual D-type Edge-triggered Flip-Flops
HD74LS78	Dual J-K Flip-Flops (with PR and CLR, and common CK)
HD74LS107	Dual J-K Flip-Flops
HD74LS109A	Dual J-K Positive Edge-triggered Flip-Flops (with PR and CLR)
HD74LS112	Dual J-K Negative Edge-triggered Flip-Flops (with PR and CLR)
HD74LS113	Dual J-K Negative Edge-triggered Flip-Flops (with PR)
HD74LS114	Dual J-K Negative Edge-triggered Flip-Flops (with PR, common CLR, and common CK)
HD74LS122	Retriggerable Monostable Multivibrators
HD74LS123	Dual Retriggerable Monostable Multivibrators
HD74LS174	Hex D-type (Flip-Flops (with CLR)
HD74LS175	Quad. D-type Flip-Flops (with CLR)
HD74LS221	Dual Monostable Multivibrators (with Schmitt Trigger)
■ COUNTERS	
HD74LS90	Decade Counters
HD74LS92	Divide-by-Twelve Counters
HD74LS160	Synchronous Decade Counters
HD74LS161	Synchronous 4-bit Binary Counters
HD74LS162	Fully Synchronous Decade Counters
HD74LS163	Fully Synchronous 4-bit Binary Counters

HD74LS190	Synchronous Decade Up/Down Counters
HD74LS191	Synchronous 4-bit Binary Up/Down Counters
HD74LS192	Synchronous Decade Up/Down Counters
HD74LS193	Synchronous 4-bit Binary Up/Down Counters
HD74LS290	Decade Counters
HD74LS293	4-bit Binary Counters
HD74LS390	Dual 4-bit Decade Counters
HD74LS393	Dual 4-bit Binary Counters
HD74LS490	Dual 4-bit Decade Counters
HD74LS668	Synchronous Decade Up/Down Counters
HD74LS669	Synchronous 4-bit Binary Up/Down Counters

■ 4-BIT, 5-BIT SHIFT/STORAGE REGISTERS

HD74LS95B	4-bit Right-shift, Left-shift Registers
HD74LS96	5-bit Shift Registers (Dual parallel-in, parallel-out)
HD74LS173	4-bit D-type Registers (with three-state outputs)
HD74LS194A	4-bit Parallel-in, Parallel-out Bidirectional Shift Registers
HD74LS195A	4-bit Parallel-in, Parallel-out Shift Registers (J-K inputs for first stage)
HD74LS295B	4-bit Right-shift, Left-shift Register

■ 8-BIT SHIFT REGISTERS

HD74LS91	8-bit Shift Registers
HD74LS164	8-bit Parallel-out Shift Registers
HD74LS166	Parallel-load 8-bit Shift Registers
HD74LS299	8-bit Universal Shift/Storage Registers

■ ENCODERS

HD74LS148	8-to-3-line Priority Encoders

■ DECODERS/DEMULTIPLEXERS

HD74LS42	BCD-to-Decimal Decoders
HD74LS138	3-8-line Decoders
HD74LS139	Dual 2-to-4-line Decoders/Demultiplexers
HD74LS154	4-to-16-line Decoders/Demultiplexers
HD74LS155	Dual 2-to-4-line Decoders/Demultiplxers
HD74LS156	Dual 2-to-4-line Decoders/Demultiplexers (with open collector outputs)

■ DECODERS/LAMP DRIVERS/BUFFERS

HD74LS145	BCD-to-Decimal Decoders/Drivers (with 15V outputs)
HD74LS47	BCD-to-Seven Segment Decoders/Drivers (with 15V outputs)
HD74LS48	BCD-to-Seven Segment Decoders/Drivers
HD74LS49	BCD-to-Seven Segment Decoders/Drivers
HD74LS247	BCD-to-Seven Segment Decoders/Drivers (with 15V outputs)
HD74LS248	BCD-to-Seven Segment Decoders/Drivers
HD74LS249	BCD-to-Seven Segment Decoders/Drivers

■ LATCHES

HD74LS75	Quad. Bistable Latches
HD74LS77	4-bit Bistable Latches
HD74LS279	Quad. $\overline{S}$-$\overline{R}$ Latches
HD74LS259	8-bit Addressable Latches
HD74LS375	4-bit Bistable Latches

■ ARITHMETIC ELEMENTS

HD74LS83A	4-bit Binary Full Adders
HD74LS85	4-bit Magnitude Comparators
HD74LS86	Quad. 2-input Exclusive-OR Gates
HD74LS136	Quad. 2-input Exclusive-OR Gates (with open collector outputs)
HD74LS181	4-bit Arithmetic Logic Units/Function Generators
HD74LS266	Quad. 2-input Exclusive-NOR Gates (with open collector outputs)
HD74LS280	9-Bit Odd/Even Parity Generators/Checkers
HD74LS283	4-bit Binary Full Adders (with fast carry)
HD74LS386	Quad. 2-input Exclusive-OR Gates

■ DATA SELECTORS/MULTIPLEXERS

HD74LS151	8-bit Data Selectors/Multiplexers (with strobe)
HD74LS152	8-bit Data Selectors/Multiplexers
HD74LS153	Dual 4-to-1-line Data Selectors/Multiplexers
HD74LS157	Quad. 2-to-1-line Data Selectors/Multiplexers
HD74LS158	Quad. 2-to-1-line Data Selectors/Multiplexers
HD74LS251	8-bit Data Selectors/Multiplexers (with strobe and three-state outputs)

HD74LS253	Dual 4-to-1-line Data Selectors/ Multiplexers (with three-state outputs)
HD74LS257	Quad. 2-to-1-line Data Selectors/ Multiplexers (with three-state outputs)
HD74LS258	Quad. 2-to-1-line Data Selectors/ Multiplexers (with three-state outputs)
HD74LS298	Quad. 2-input Multiplexers (with storage)

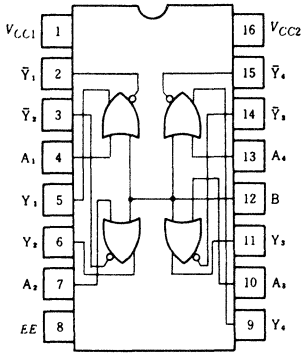
10K LOGIC FAMILY

HD10101	Quadruple OR/NOR Gates
HD10102	Quadruple 2-input NOR Gates
HD10104	Quadruple 2-input AND Gates
HD10105	Triple 2-3-2-input OR/NOR Gates
HD10106	Triple 4-3-3-input NOR Gates
HD10107	Triple 2-input Exclusive-OR/NOR Gates
HD10109	Dual 4-5-input OR/NOR Gates
HD10110	Dual 3-input 3-output OR Gates
HD10111	Dual 3-input 3-output NOR Gates
HD10116	Triple Line Receivers
HD10117	Dual 2-wide 2-3-input OR-AND/OR-AND-INVERT Gates
HD10118	Dual 2-wide 3-input OR-AND Gates
HD10119	4-wide 4-3-3-3-input OR/AND Gate
HD10121	4-wide OR-AND/OR-AND-INVERT Gate
HD10124	Quadruple TTL-to-ECL Translators
HD10125	Quadruple ECL-to-TTL Translators
HD10130	Dual Latches
HD10131	Dual Type-D Master-Slave Flip Flops
HD10132	Dual Multiplexers with Latch and Common Reset
HD10133	Quadruple Latches
HD10134	Multiplexer with Latch
HD10136	Universal Hexadecimal Counter
HD10145	64-bit Register File (RAM)
HD10147	128-bit Random Access Memory
HD10148	64-bit Random Access Memory
HD10160	12-bit Parity Generator/Checker
HD10161	Binary-to-1-of-8 Decoder (Low)
HD10162	Binary-to-1-of-8 Decoder (High)
HD10164	8-line Multiplexer
HD10174	Dual 4-to-1 Multiplexers
HD10175	Quintuple Latches
HD10179	Look-Ahead Carry Block
HD10180	Dual High Speed Adders/Subtractors
HD10181	4-bit Arithmetic Logic Unit/Function Generator
HD10209	Dual High Speed 4-5 input OR/NOR Gates
HD10210	Dual High Speed 3-input 3-output OR Gates
HD10211	Dual High Speed 3-input 3-output NOR Gates
HD10230	Dual High Speed Latches
HD10231	Dual High Speed Type-D Master-Slave Flip Flops

HD10101

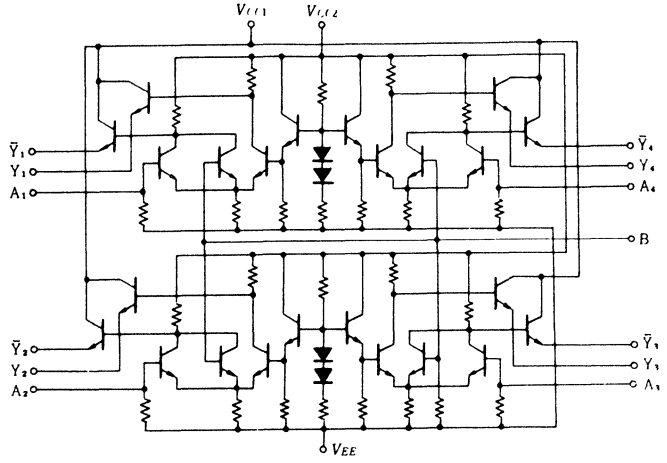
Quadruple OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

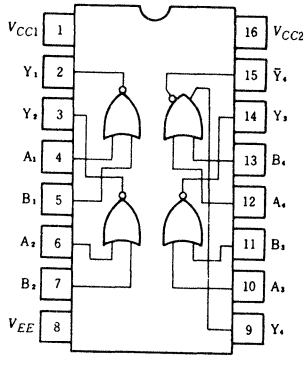
■CIRCUIT SCHEMATIC



HD10102

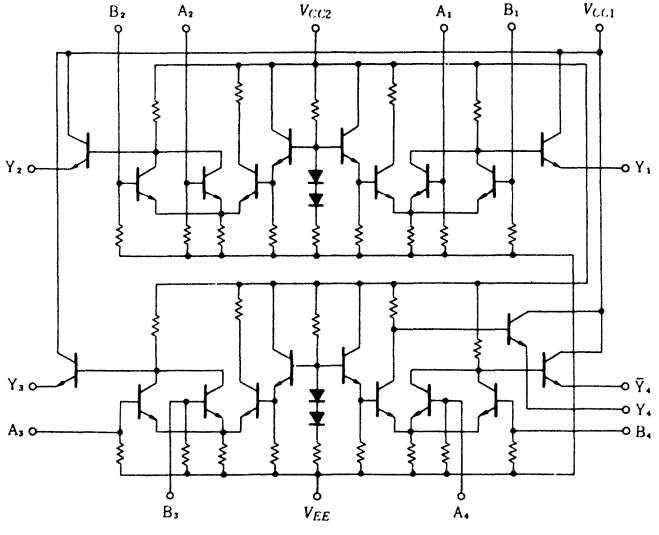
Quadruple 2-input NOR Gates

■PIN ARRANGEMENT



(Top View)

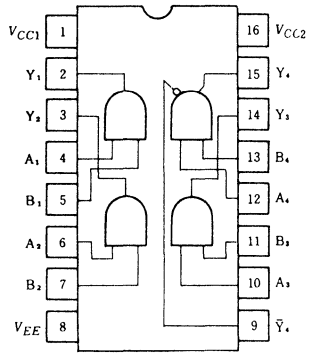
■CIRCUIT SCHEMATIC



HD10104

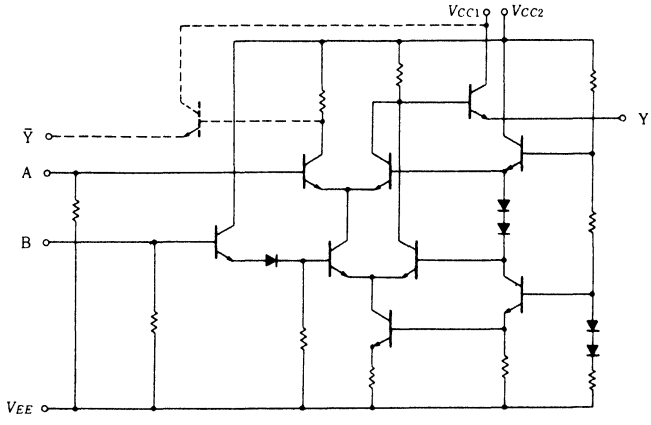
Quadruple 2-input AND Gates

■PIN ARRANGEMENT



(Top View)

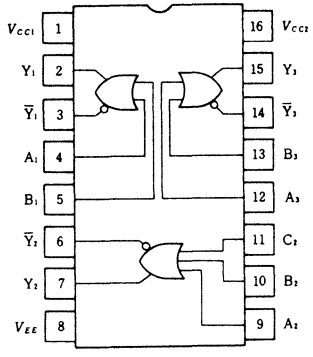
■CIRCUIT SCHEMATIC (¼)



HD10105

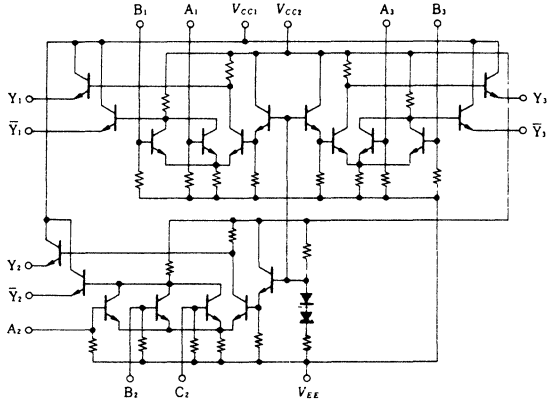
Triple 2-3-2 input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

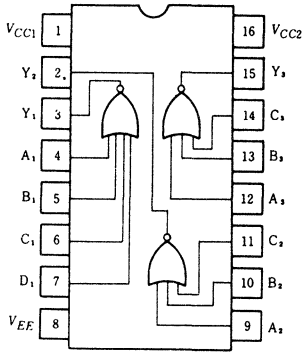
■CIRCUIT SCHEMATIC



HD10106

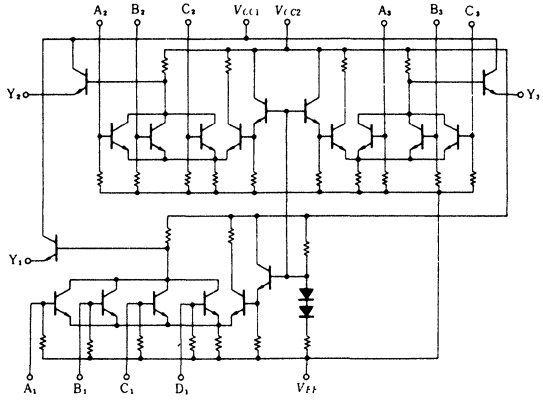
Triple 4-3-3 input NOR Gates

■PIN ARRANGEMENT



(Top View)

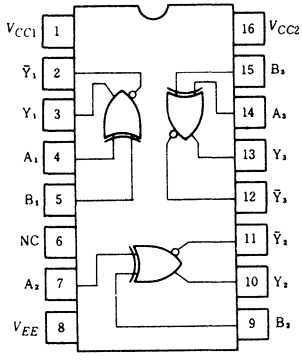
■CIRCUIT SCHEMATIC



HD10107

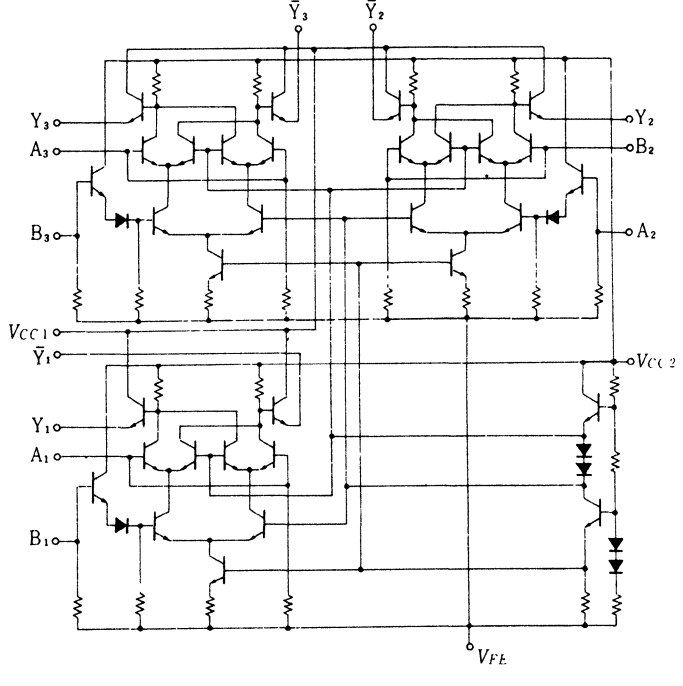
Triple 2-input Exclusive-OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

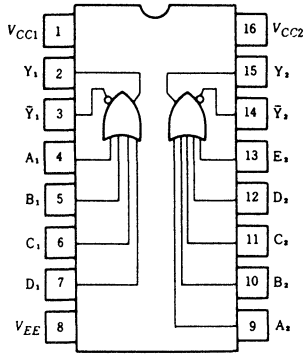
■CIRCUIT SCHEMATIC



HD10109

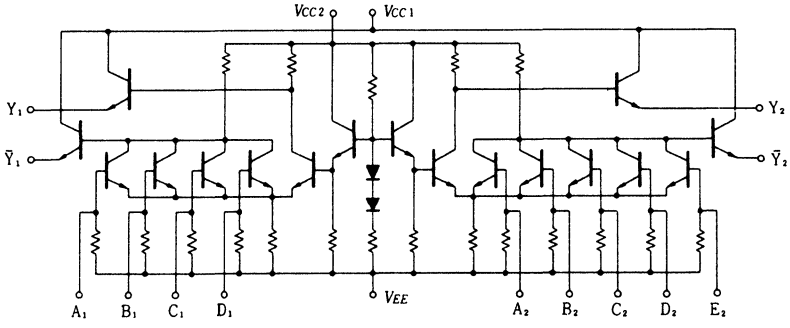
Dual 4-5 input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

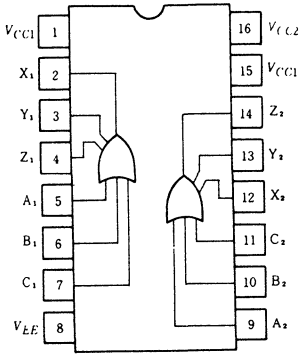
■CIRCUIT SCHEMATIC



HD10110

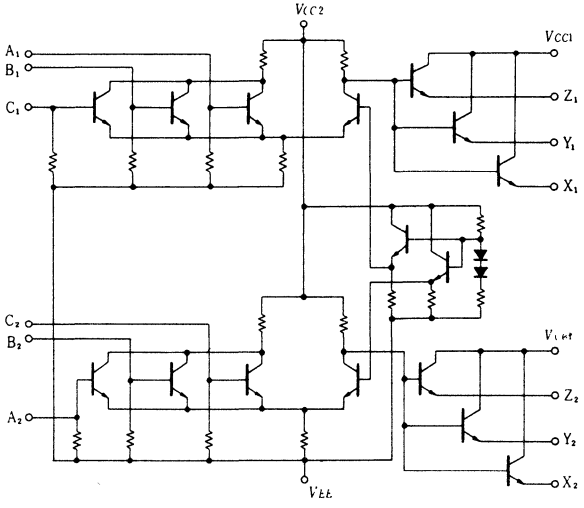
Dual 3-input 3-output OR Gates

■PIN ARRANGEMENT



(Top View)

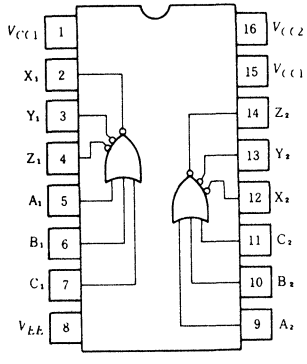
■CIRCUIT SCHEMATIC



HD10111

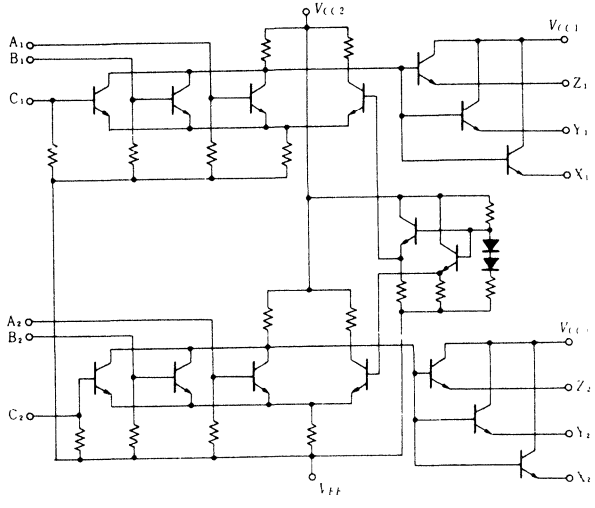
Dual 3-input 3-output NOR Gates

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC

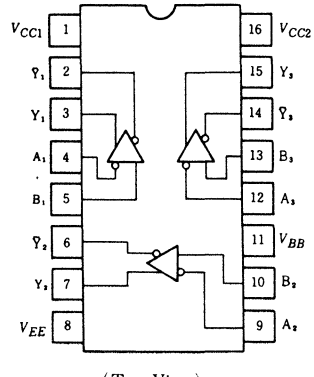


HD10116

Triple Line Receivers

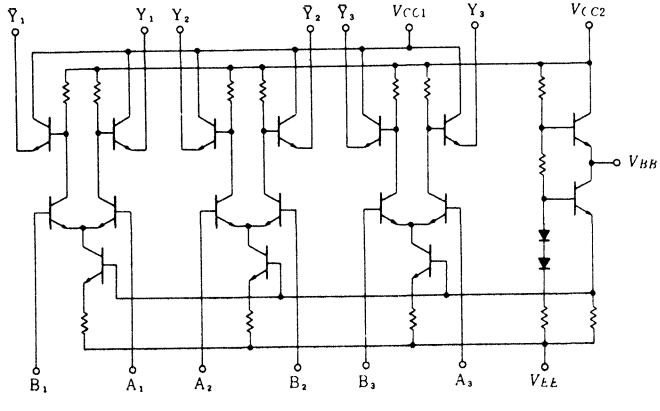
The HD10116 is designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current source provides these receivers with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent upsetting the current source bias network.

■PIN ARRANGEMENT



(Top View)

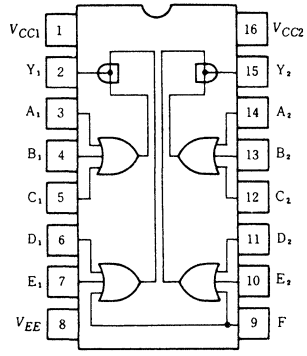
■CIRCUIT SCHEMATIC



HD10117

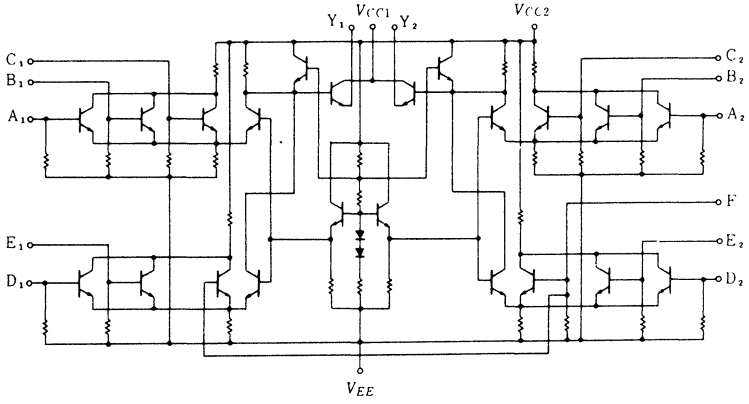
Dual 2-wide 2-3-input OR-AND/OR-AND INVERT Gates

■PIN ARRANGEMENT



(Top View)

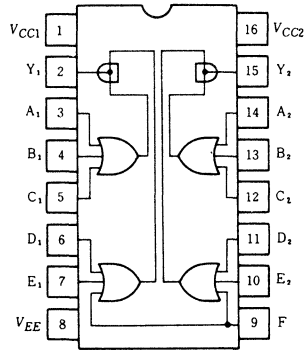
■CIRCUIT SCHEMATIC



HD10118

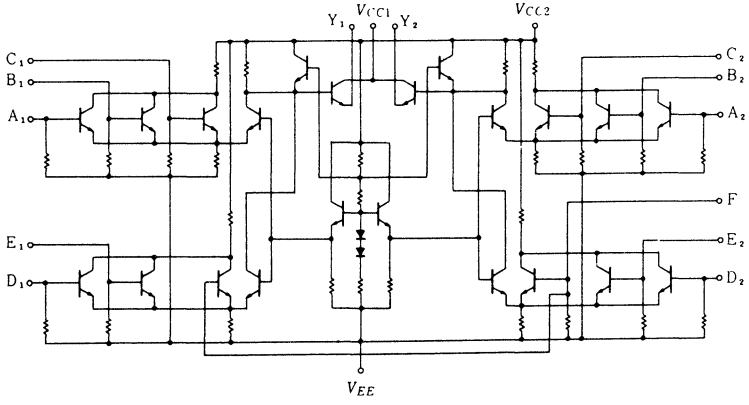
Dual 2-wide 3-input OR-AND Gates

■PIN ARRANGEMENT



(Top View)

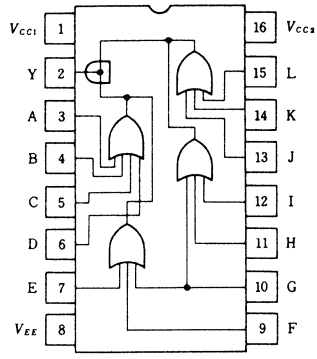
■CIRCUIT SCHEMATIC



HD10119

4-wide 4-3-3-3-input OR/AND Gate

■PIN ARRANGEMENT



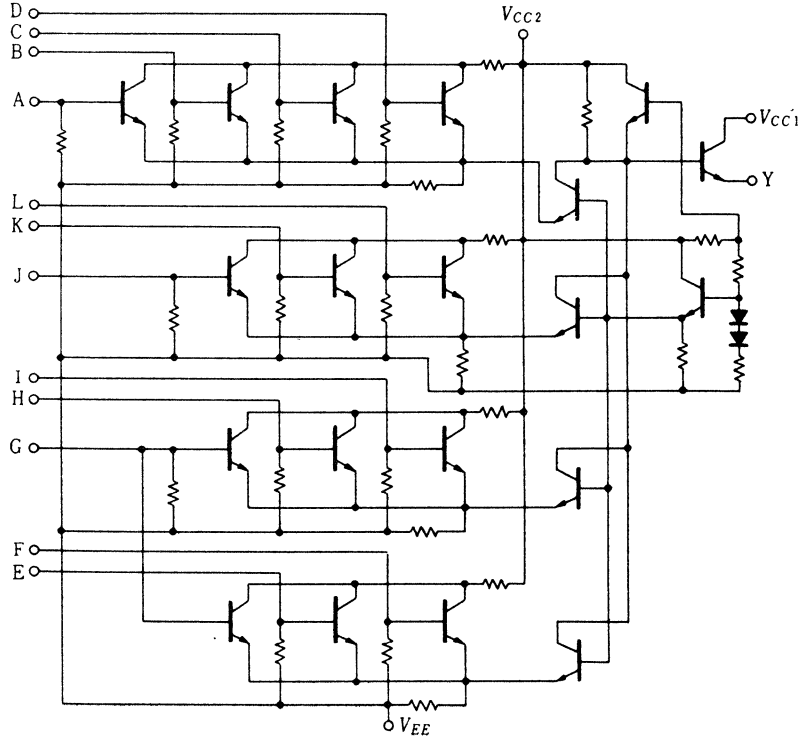
(Top View)

■FUNCTION TABLE

Inputs												Outputs
A	B	C	D	E	F	G	H	I	J	K	L	Y
L	L	L	L	×	×	×	×	×	×	×	×	L
×	×	×	×	L	L	L	×	×	×	×	×	L
×	×	×	×	×	×	L	L	L	×	×	×	L
×	×	×	×	×	×	×	×	×	L	L	L	L
Notes 1												H

Notes) 1. Each input of OR gates are combined to high.
2. X: Don't Care

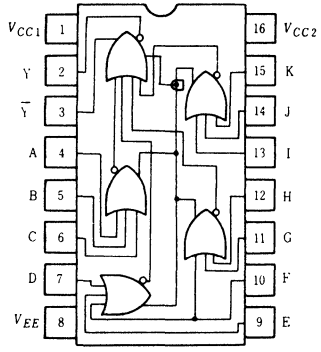
■CIRCUIT SCHEMATIC



HD10121

4-wide OR-AND/OR-AND-INVERT Gate

■PIN ARRANGEMENT



(Top View)

HD10124

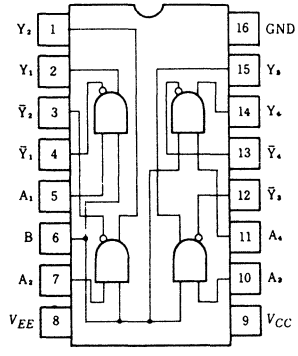
Quadruple TTL-to-ECL Translators

The HD10124 is a quad translator for interfacing data and control signals between a saturated logic section and the ECL section of digital systems. The device has TTL compatible inputs, and ECL complementary open-emitter outputs that allow use as an inverting/noninverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a ECL high logic state.

Power supply requirements are ground, +5.0V, and −5.2V. The DC levels are standard or Schottky TTL in, ECL 10K out.

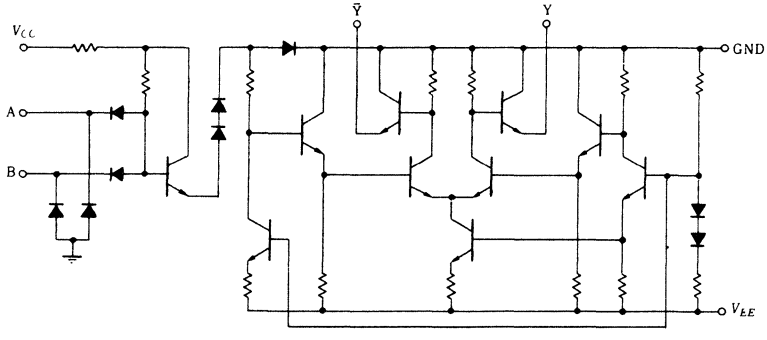
An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the ECL equipment, where the signal can be received by any of the ECL receivers or the HD10125 ECL to TTL translator.

■PIN ARRANGEMENT



(Top View)

■CIRCUIT SCHEMATIC



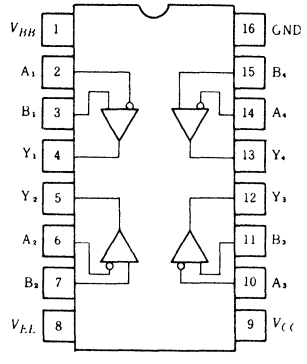
HD10125

Quadruple ECL-to-TTL Translators

The HD10125 is a quad translator for interfacing data and control signals between the ECL section and saturated logic sections of digital systems. The HD10125 incorpolates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/ noninverting translator or as a differential line receiver.

The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs go to a low logic level whenever the inputs are left floating. Power supply requirements are ground, +5V and –5.2V. The HD10125 has a fanout of 10 TTL loads. The DC levels are ECL 10K in and Schottky TTL or standard TTL out. The device has an input common mode noise rejection of ±1.0V.

■PIN ARRANGEMENT



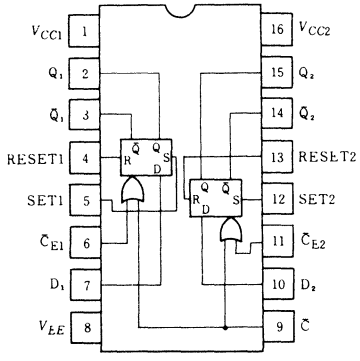
(Top View)

HD10130

Dual Latches

The HD10130 is a clocked dual D-type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode the enable inputs perform the function of controlling the common clock ($\overline{C}$). Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state a change in the information present at the data inputs will not affect the output information. The set and reset inputs for not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

■PIN ARRANGEMENT



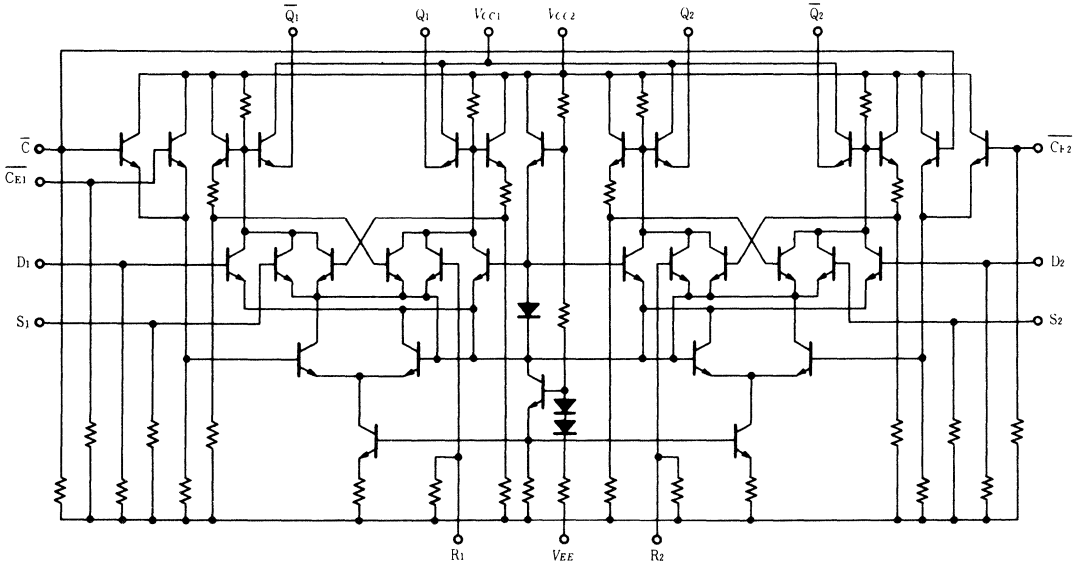
(Top View)

■FUNCTION TABLE

D	$\overline{C}$	$\overline{C}_E$	Q_{n+1}
L	L	L	L
H	L	L	H
×	L	H	Q_n
×	H	L	Q_n
×	H	H	Q_n

× Don't care

■CIRCUIT SCHEMATIC



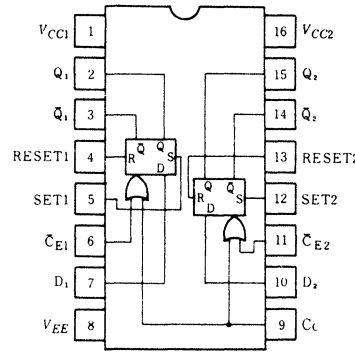
HD10131

Dual Type-D Master-Slave Flip Flops

The HD10131 is a dual master-slave type D flip-flop. Asynchronous Set(S) and Reset(R) override Clock(C_C) and $\overline{\text{Clock Enable}}$($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the $\overline{\text{Clock Enable}}$ inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data(D) input will not affect the output information at any other time due to master-slave construction.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

●R-S

R	S	Q_{n+1}	$\bar{Q}_{n+1}$
L	L	Q_n	$\bar{Q}_n$
L	H	H	L
H	L	L	H
H	H	×	×

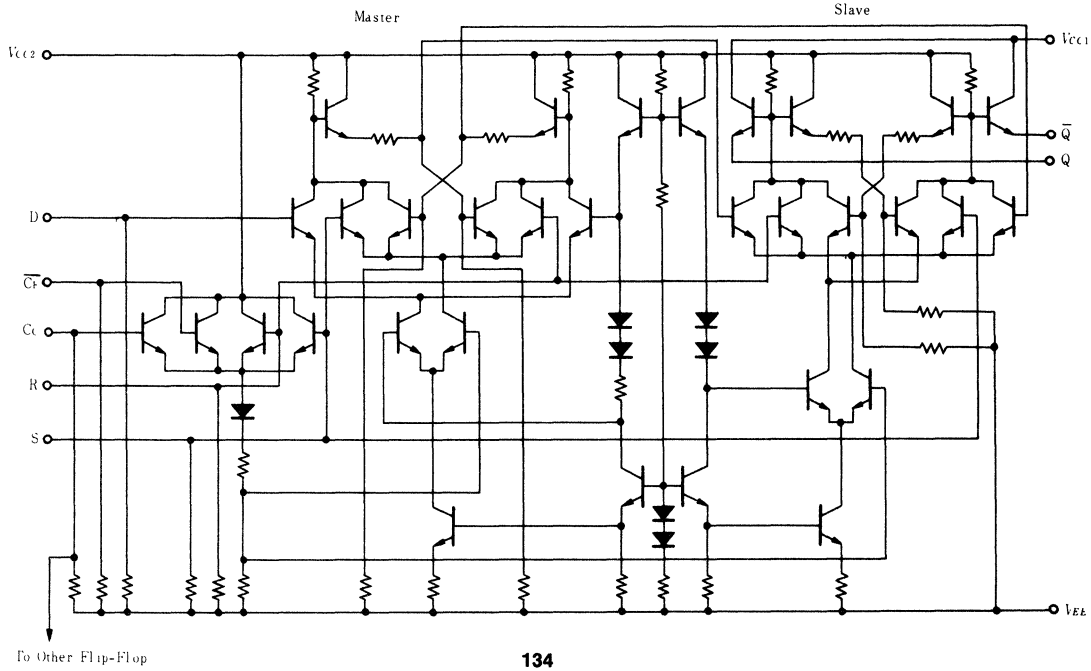
×. Not Defined

●Clock

C	D	Q_{n+1}
L	×	Q_n
↑	L	L
↑	H	H

Notes) 1. Don't Care
2. $C=\overline{CE}+C_C$
3. A ↑ is a clock transition from a low to a high state.

■CIRCUIT SCHEMATIC



HD10132

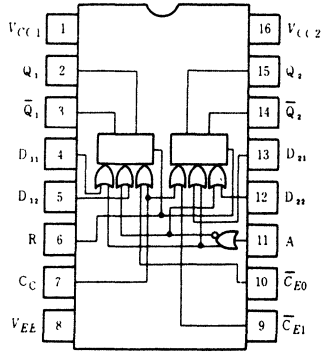
Dual Multiplexers with Latch and Common Reset

The HD10132 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to used to clock the latch, the clock enable($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock(C_C). The data select(A) input determines which data input is enabled. A high(H) level enables data inputs D12 and D22 and a low(L) level enables data inputs D11 and D21.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state a change in the information present at the data inputs will not affect the output information.

The reset input is enabled when the clock is in the high state and disabled when the clock is in the high state, and disabled when the clock is low.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

R	D	C_C	$\overline{C_E}$	Q_{n+1}
×	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
×	H	L	L	H
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	×	×	H	L

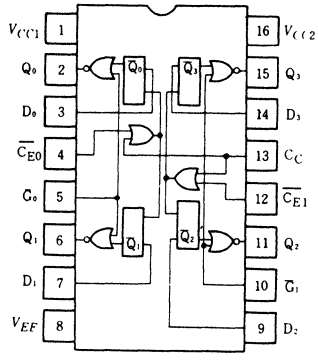
Notes) 1. Don't care.
2. $Dn=(\overline{A}\cdot Dn_1)+(A\cdot Dn_2)$

HD10133

Quadruple Latches

The HD10133 is a high speed, low power quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock. The outputs are gated when the output enable($\overline{G}$) is low. All four latches may be clocked at one time with the common clock(C_C), or each half may be clocked separately with its clock enable ($\overline{CE}$).

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

$\overline{G}$	C	D	Q_{n+1}
H	×	×	L
L	L	×	Q_n
L	H	L	L
L	H	H	H

Notes) × : Don't care.
$C = C_C + \overline{C}_E$

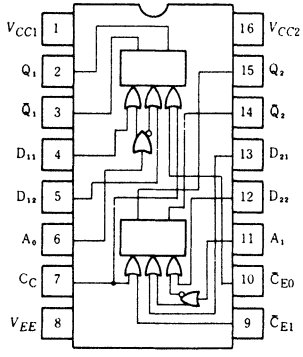
HD10134

Multiplexer with Latch

The HD10134 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock(C_C).

The data select inputs determine which data input is enabled. A high(H) level on the A0 input enables data input D12 and a low(L) level on the A0 input enables data input D11. A high(H) level on the A1 input enables data input D22 and a low(L) level on the A1 input enables data input D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

C	A_0	D_{11}	D_{12}	Q_{n+1}
L	L	L	×	L
L	L	H	×	H
L	H	×	L	L
L	H	×	H	H
H	×	×	×	Q_n

Notes) × : Don't care.
$C=\overline{C}_E+C_C$

HD10136

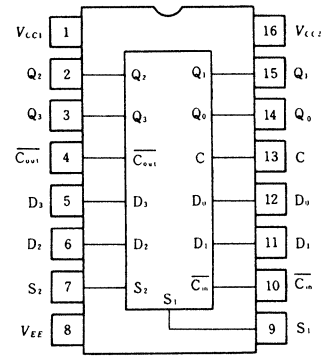
Universal Hexadecimal Counter

The HD10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous counter feature makes the HD10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs(D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

■PIN ARRANGEMENT



(Top View)

■FUNCTION SELECT TABLE

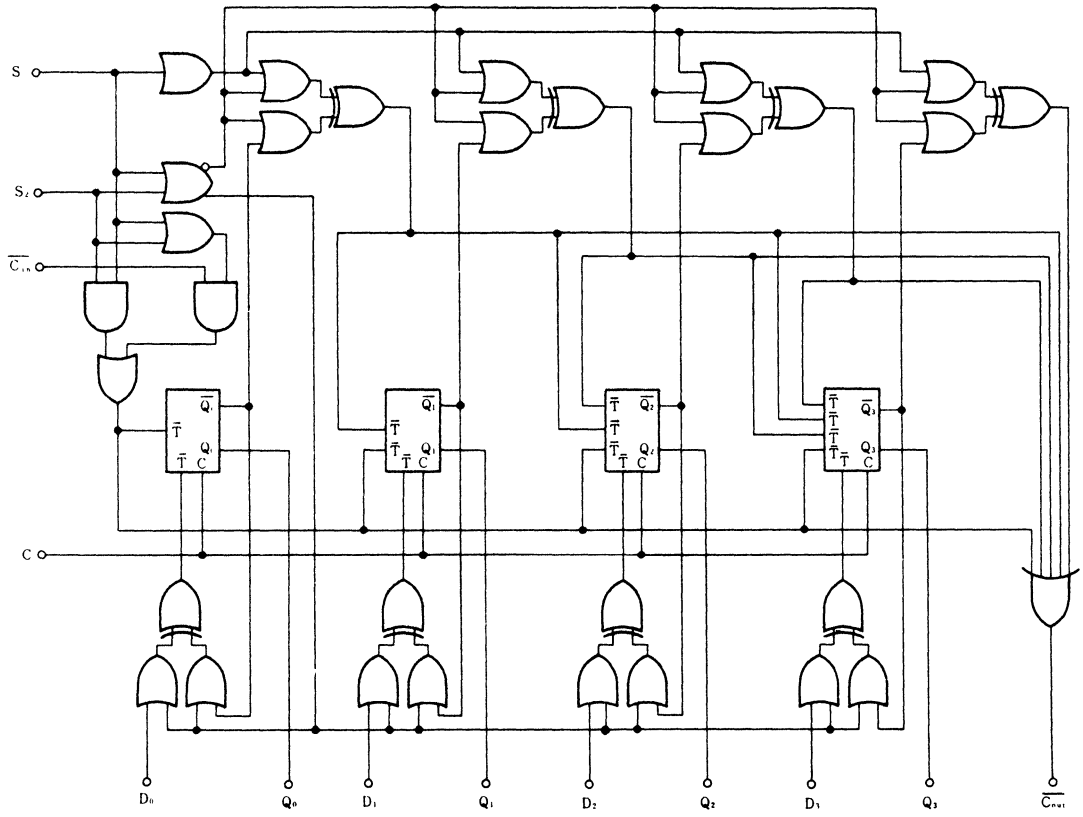
S_1	S_2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

■TRUTH TABLE

Inputs								Outputs				
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{Cin}$	C	Q_0	Q_1	Q_2	Q_3	$\overline{Cout}$
L	L	L	L	H	H	×	↑	L	L	H	H	L
L	H	×	×	×	×	L	↑	H	L	H	H	H
L	H	×	×	×	×	L	↑	L	H	H	H	H
L	H	×	×	×	×	L	↑	H	H	H	H	L
L	H	×	×	×	×	H	L	H	H	H	H	H
L	H	×	×	×	×	H	↑	H	H	H	H	H
H	H	×	×	×	×	×	↑	H	H	H	H	H
L	L	H	H	L	L	×	↑	H	H	L	L	L
H	L	×	×	×	×	L	↑	L	H	L	L	H
H	L	×	×	×	×	L	↑	H	L	L	L	H
H	L	×	×	×	×	L	↑	L	L	L	L	L
H	L	×	×	×	×	L	↑	H	H	H	H	H

Notes) 1. × : Don't care.
2. A ↑ is defined as a clock input transition from a low to a high logic level.

■BLOCK DIAGRAM



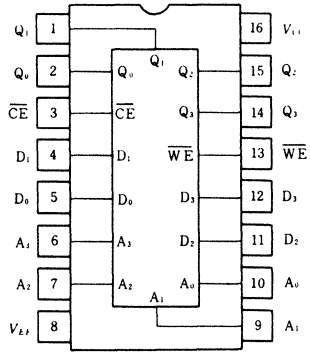
HD10145

64-bit Register File (RAM)

The HD10145 is a 16 word x 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 through A3. The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance. The operating mode of the RAM($\overline{CE}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode- the output is low and the data present at Dn is stored at the selected address.

With $\overline{WE}$ high the chip is in the read mode- The data state at the selected memory location is presented non-inverted at Qn.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

Mode	Inputs			Output
	$\overline{CE}$	$\overline{WE}$	D	Q
Write "L"	L	L	L	L
Write "H"	L	L	H	L
Read	L	H	×	Q
Disabled	H	×	×	L

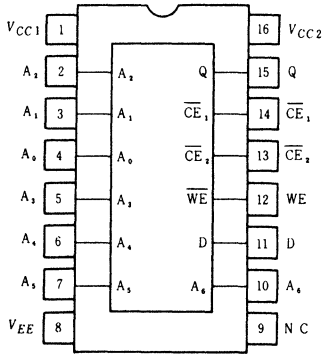
Note) × : Don't care

HD10147

128-bit Random Access Memory

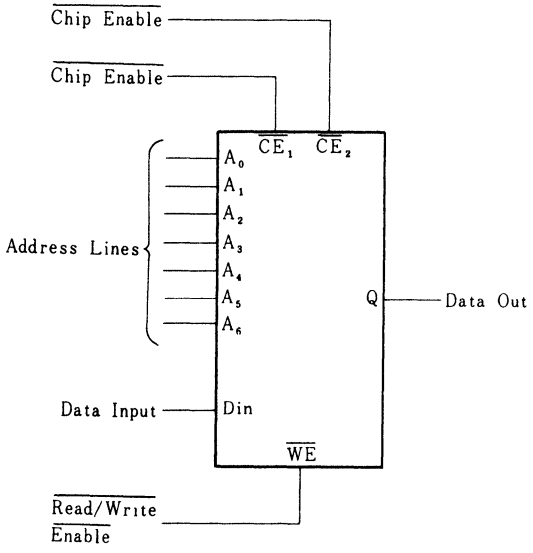
The HD10147 is a fast 128-word x 1-bit RAM. Bit selection is achieved by means of a 7-bit address, A0 through A6. The active-low chip selects and fast chip select access time allow easy memory expansion up to 512 words without affecting system performance. The operating mode ($\overline{CE}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode- the output is low and the data present at Dn is stroed at the selected address. With $\overline{WE}$ high the chip is in the read mode- the data state at the selected memory location is presented non-inverted at Dout.

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■FUNCTION TABLE

Mode	Input				Output
	$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	Din	Dout
Write "L"	L	L	L	L	L
Write "H"	L	L	L	H	L
Read	L	L	H	×	Q
Disabled	H	L	×	×	L
	L	H	×	×	L

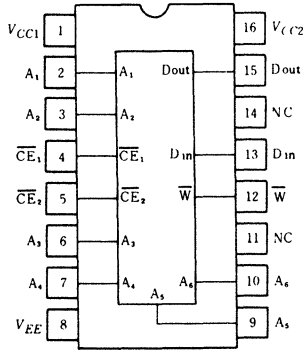
Note) × : Don't care.

HD10148

64-bit Random Access Memory

The HD10148 is a fast 64-word x 1-bit RAM. Bit selection is achieved by means of a 6-bit address, A0 through A5. The active low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance. The operating mode ($\overline{CE}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode- The output is low and the data present at Din is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode- the data state at the selected memory location is presented non-inverted at Dout.

■PIN ARRANGEMENT



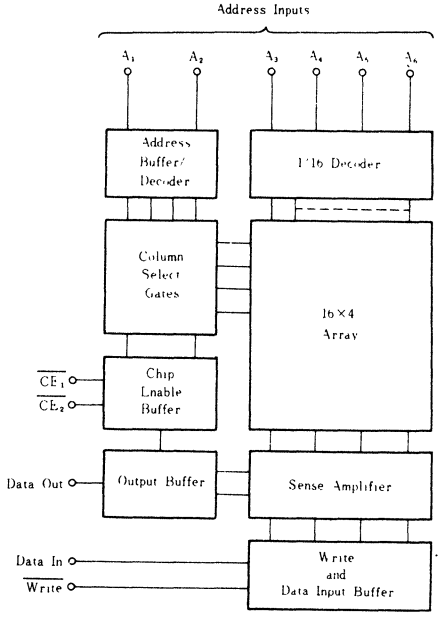
(Top View)

■FUNCTION TABLE

Mode	Inputs			Output
	$\overline{CE}$	$\overline{WE}$	Din	Dout
Write "L"	L	L	L	L
Write "H"	L	L	H	L
Read	L	H	×	Q
Disabled	H	×	×	L

× : Don't care.
$\overline{CE}=\overline{CE_1}+\overline{CE_2}$

■BLOCK DIAGRAM



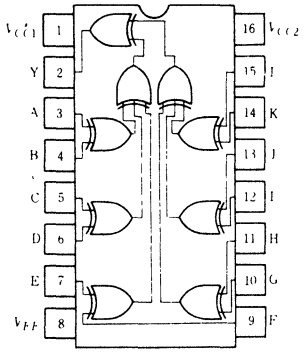
HD10160

12-bit Parity Generator/Checker

The HD10160 consists of nine Exclusive-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high.

Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

Inputs	Output
Sum of High Level Inputs	Y
Even	H
Odd	L

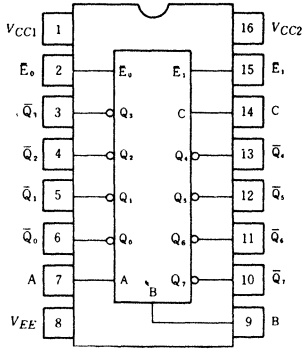
HD10161

Binary to-1-of-8 Decoder (Low)

The HD10161 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high. The HD10161 is a true parallel decoder.

No series gating is used internally, eliminating unequal delay time found in other decoders. This design provides the identical 4ns delay from any address or enable input to any output.

■ PIN ARRANGEMENT



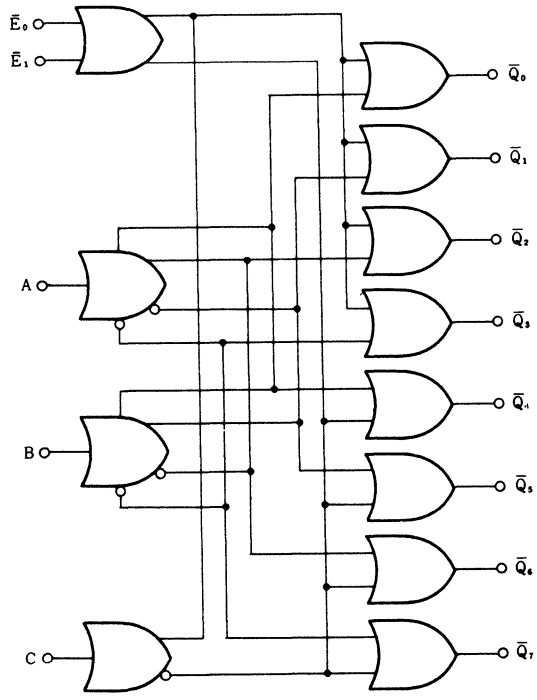
(Top View)

■ FUNCTION TABLE

Enable Inputs		Inputs			Outputs							
$\overline{E}_1$	$\overline{E}_0$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	×	×	×	×	H	H	H	H	H	H	H	H
×	H	×	×	×	H	H	H	H	H	H	H	H

× : Don't Care

■ BLOCK DIAGRAM

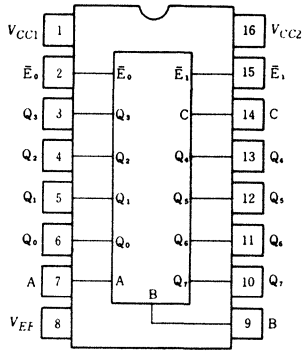


HD10162

Binary to-1-of-8 Decoder (High)

The HD10162 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low. The HD10162 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

■ PIN ARRANGEMENT



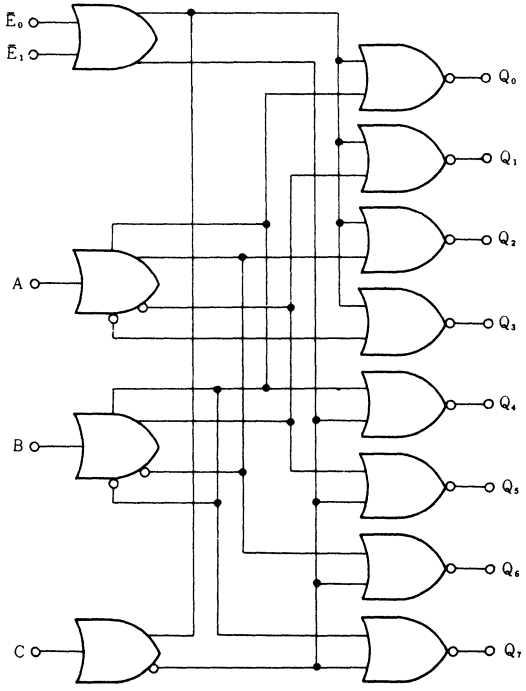
(Top View)

■ FUNCTION TABLE

Enable Inputs		Inputs			Outputs							
$\overline{E}_0$	$\overline{E}_1$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	×	×	×	×	L	L	L	L	L	L	L	L
×	H	×	×	×	L	L	L	L	L	L	L	L

× : Don't Care

■ BLOCK DIAGRAM

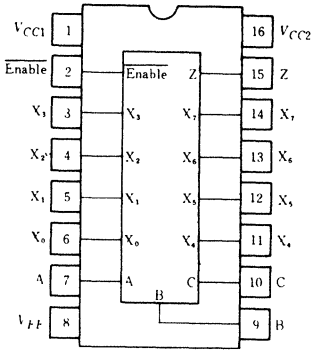


HD10164

8-line Multiplexer

The HD10164 can be used whenever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the HD10164 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The HD10164 can be connected directly to a data bus, due to its open emitter output and output enable.

■ PIN ARRANGEMENT



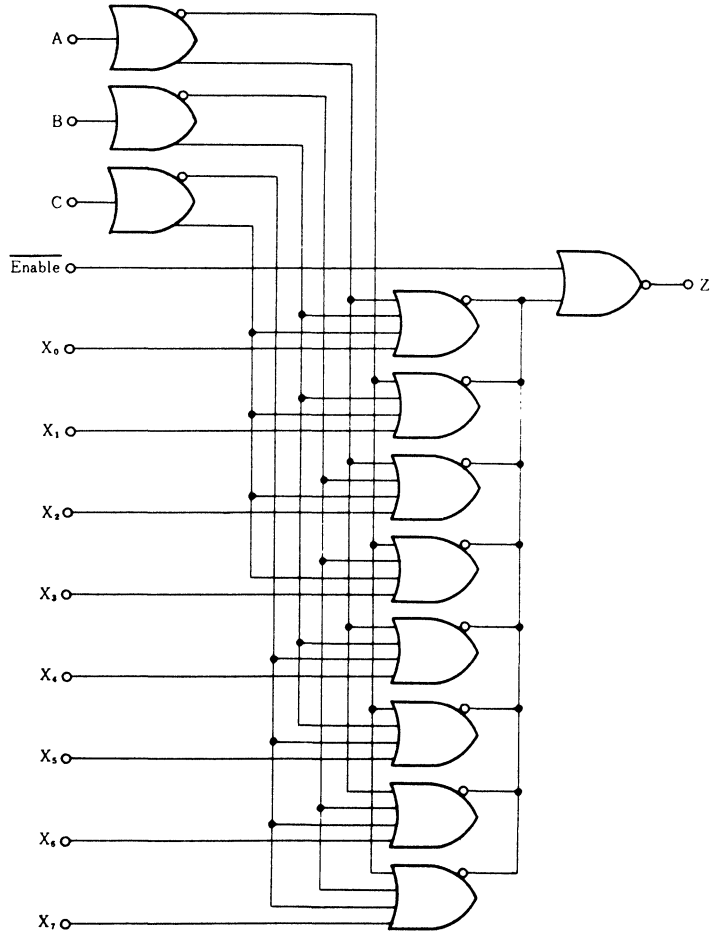
(Top View)

■ FUNCTION TABLE

$\overline{Enable}$	Address Inputs			Z
	C	B	A	
L	L	L	L	X_0
L	L	L	H	X_1
L	L	H	L	X_2
L	L	H	H	X_3
L	H	L	L	X_4
L	H	L	H	X_5
L	H	H	L	X_6
L	H	H	H	X_7
H	×	×	×	L

× : Don't Care

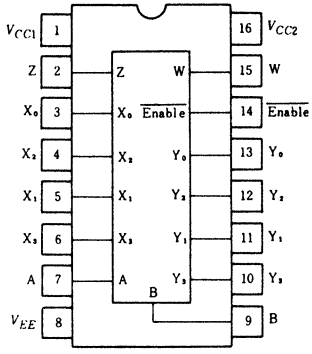
■ BLOCK DIAGRAM



HD10174

Dual 4-to-1 Multiplexers

■ PIN ARRANGEMENT



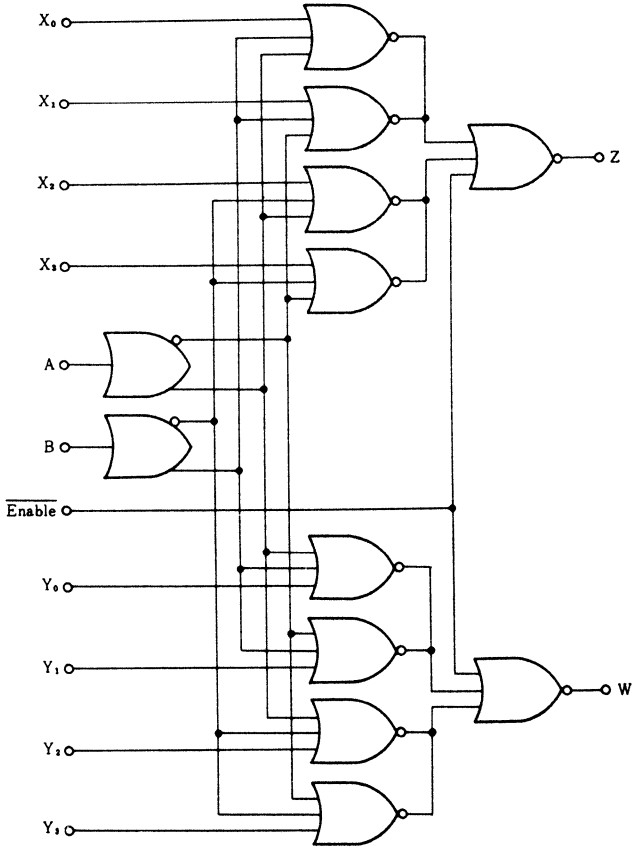
(Top View)

■ FUNCTION TABLE

Enable	Address Inputs		Outputs	
$\overline{E}$	B	A	Z	W
H	×	×	L	L
L	L	L	X_0	Y_0
L	L	H	X_1	Y_1
L	H	L	X_2	Y_2
L	H	H	X_3	Y_3

× : Don't Care

■ BLOCK DIAGRAM



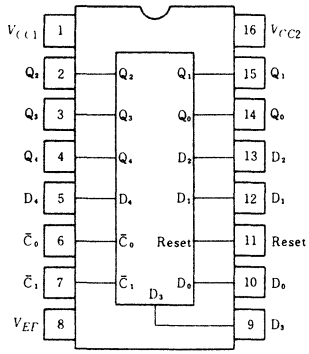
HD10175

Quintuple Latches

The HD10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latches on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

■ PIN ARRANGEMENT



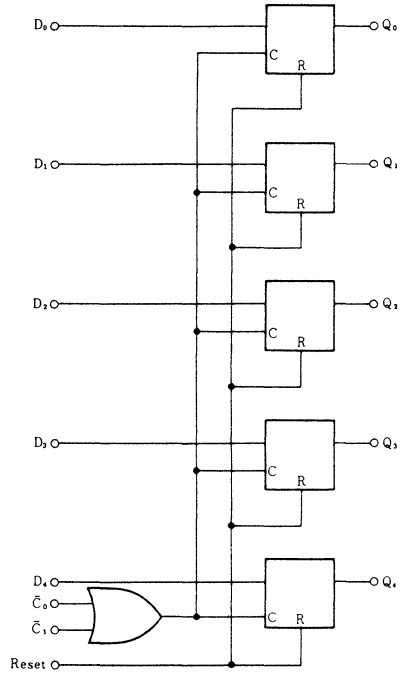
(Top View)

■ FUNCTION TABLE

D	C_0	C_1	Reset	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
×	H	×	L	Q_n
×	×	H	L	Q_n
×	H	×	H	L
×	×	H	H	L

× : Don't Care

■ BLOCK DIAGRAM

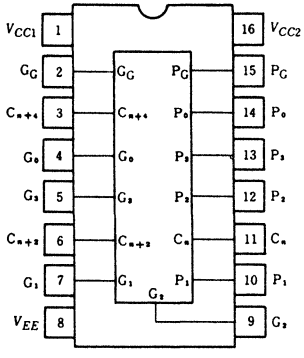


HD10179

Look-Ahead Carry Block

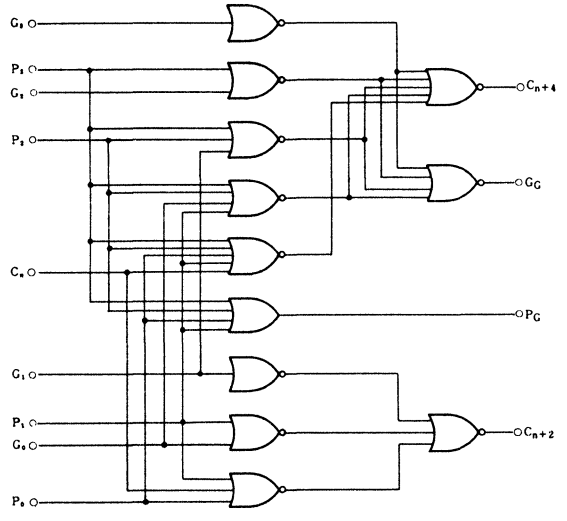
The HD10179 is a high speed, low power, standard ECL complex function that is designed to perform the look-ahead carry function. This device can be used with the HD10181 4-unit ALU directly, or with the HD10180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM

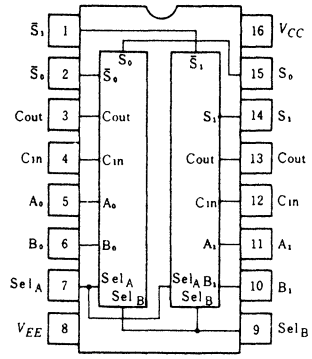


HD10180

Dual High Speed Adders/Subtractors

The HD10180 is a high speed, low power, general-purpose adder/subtractor. Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, $\overline{\text{Sum}}$, and Carry-out. The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B.

■ PIN ARRANGEMENT



(Top View)

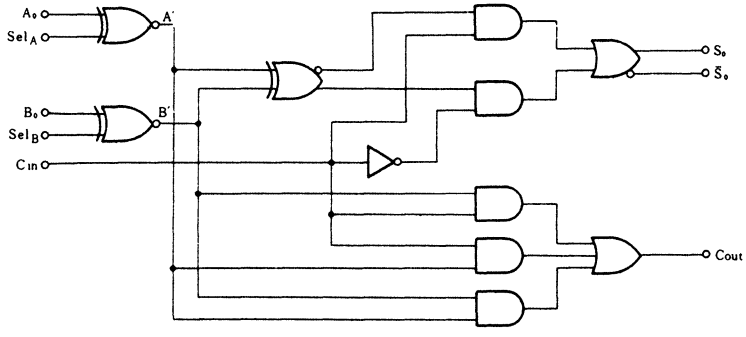
■ FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S = A + B
H	L	S = A − B
L	H	S = B − A
L	L	S = 0 − A − B

■ FUNCTION TABLE

Function	Inputs					Outputs			Function	Inputs					Outputs			
	Sel_A	Sel_B	A_0	B_0	Cin	S_0	$\overline{S_0}$	Cout		Sel_A	Sel_B	A_0	B_0	Cin	S_0	$\overline{S_0}$	Cout
ADD	H	H	L	L	L	L	H	L	REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	H	H	L	L	H	H	L	L		L	H	L	L	H	L	H	H
	H	H	L	H	L	H	L	L		L	H	L	H	L	L	H	H
	H	H	L	H	H	L	H	H		L	H	L	H	H	H	L	H
	H	H	H	L	L	H	L	L		L	H	H	L	L	L	H	L
	H	H	H	L	H	L	H	H		L	H	H	L	H	H	L	L
	H	H	H	H	L	L	H	H		L	H	H	H	L	H	L	L
	H	H	H	H	H	H	L	H		L	H	H	H	H	L	H	H
SUBTRACT	H	L	L	L	L	H	L	L		L	L	L	L	L	L	H	H
	H	L	L	L	H	L	H	H		L	L	L	L	H	H	L	H
	H	L	L	H	L	L	H	L		L	L	L	H	L	H	L	L
	H	L	L	H	H	H	L	L		L	L	L	H	H	L	H	H
	H	L	H	L	L	L	H	H		L	L	H	L	L	H	L	L
	H	L	H	L	H	H	L	H		L	L	H	L	H	L	H	H
	H	L	H	H	L	H	L	L		L	L	H	H	L	L	H	L
	H	L	H	H	H	L	H	H		L	L	H	H	H	H	L	L

■ BLOCK DIAGRAM

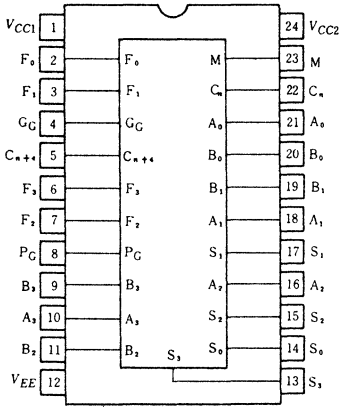


HD10181

4-bit Arithmetic Logic Unit/Function Generator

The HD10181 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S1 through S3) as indicated in the table of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

■ PIN ARRANGEMENT



(Top View)

■ FUNCTIONS OF PIN NUMBER

Pin No.	Function
A_3, A_2, A_1, A_0	Word A Inputs
B_3, B_2, B_1, B_0	Word B Inputs
S_3, S_2, S_1, S_0	Function-Select Inputs
C_n	Ripple-Carry Input
M	Mode Control Input
F_3, F_2, F_1, F_0	Function Outputs
P_G	Carry Propagate Output
C_{n+4}	Ripple-Carry Output
G_G	Carry-Generate Output

■ FUNCTION TABLE

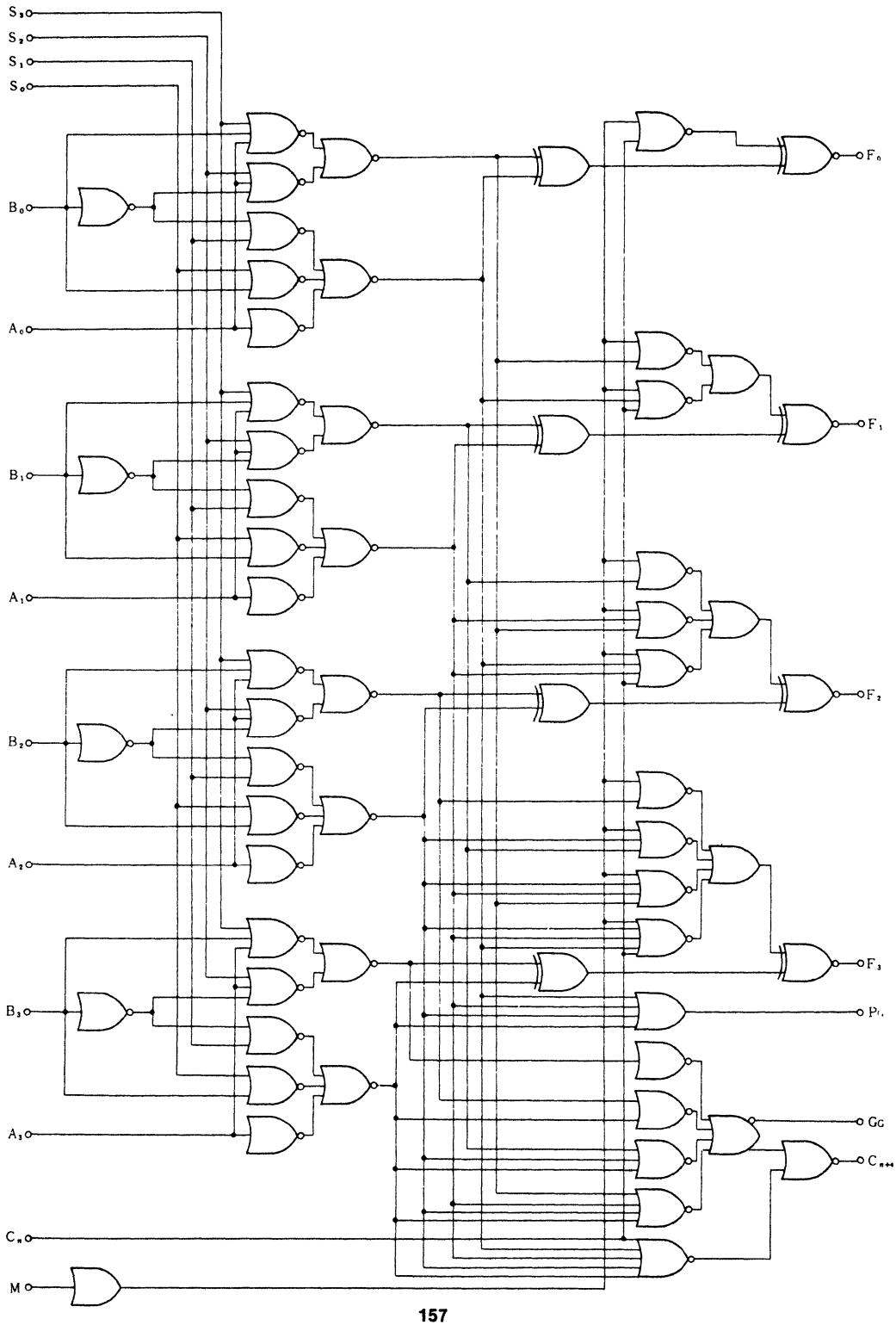
1. Positive Logic

Function Select				Logic Function (M="H")	Arithmetic Operation (M="L", Cn="L")
$\overline{S}_3$	$\overline{S}_2$	$\overline{S}_1$	$\overline{S}_0$	F	F
L	L	L	L	$F=\overline{A}$	$F=A+0$
L	L	L	H	$F=\overline{A}+\overline{B}$	$F=A+(A\cdot\overline{B})$
L	L	H	L	$F=\overline{A}+B$	$F=A+(A\cdot B)$
L	L	H	H	F="H"	$F=A\times 2$
L	H	L	L	$F=\overline{A}\cdot\overline{B}$	$F=(A+B)+0$
L	H	L	H	$F=\overline{B}$	$F=(A+B)+(A\cdot\overline{B})$
L	H	H	L	$F=A\cdot B$	$F=A+B$
L	H	H	H	$F=A+\overline{B}$	$F=A+(A+B)$
H	L	L	L	$F=\overline{A}\cdot B$	$F=(A+\overline{B})+0$
H	L	L	H	$F=A\oplus B$	$F=A-B-1$
H	L	H	L	$F=B$	$F=(A+\overline{B})+(A\cdot B)$
H	L	H	H	$F=A+B$	$F=(A+\overline{B})+A$
H	H	L	L	F="L"	F=−1 (two's complement)
H	H	L	H	$F=A\cdot\overline{B}$	$F=(A\cdot\overline{B})-1$
H	H	H	L	$F=A\cdot B$	$F=(A\cdot B)-1$
H	H	H	H	$F=A$	$F=A-1$

2. Negative Logic

Function Select				Logic Function (M="H")	Arithmetic Operation (M="L", Cn="H")
S_3	S_2	S_1	S_0	F	F
L	L	L	L	$F=\overline{A}$	$F=A-1$
L	L	L	H	$F=\overline{A+B}$	$F=A+(A+\overline{B})$
L	L	H	L	$F=\overline{A}\cdot B$	$F=A+(A+B)$
L	L	H	H	F="L"	$F=A\times 2$
L	H	L	L	$F=\overline{A\cdot B}$	$F=(A\cdot B)-1$
L	H	L	H	$F=\overline{B}$	$F=(A\cdot B)+(A+\overline{B})$
L	H	H	L	$F=A\oplus B$	$F=A+B$
L	H	H	H	$F=A\cdot\overline{B}$	$F=A+(A\cdot B)$
H	L	L	L	$F=\overline{A}+B$	$F=(A\cdot\overline{B})-0$
H	L	L	H	$F=A\cdot B$	$F=A-B-1$
H	L	H	L	$F=B$	$F=(A\cdot\overline{B})+(A+B)$
H	L	H	H	$F=A\cdot B$	$F=(A\cdot\overline{B})+A$
H	H	L	L	F="H"	F=−1 (two's complement)
H	H	L	H	$F=A+\overline{B}$	$F=(A+\overline{B})+0$
H	H	H	L	$F=A+B$	$F=(A+B)+0$
H	H	H	H	$F=A$	$F=A+0$

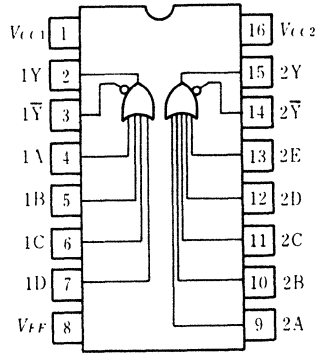
■ BLOCK DIAGRAM



HD10209

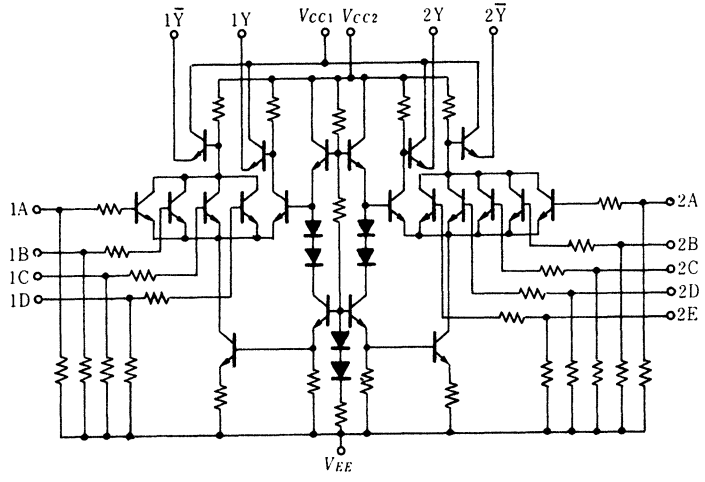
Dual High Speed 4-5 input OR/NOR Gates

■PIN ARRANGEMENT



(Top View)

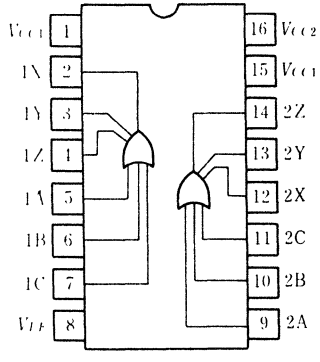
■CIRCUIT SCHEMATIC



HD10210

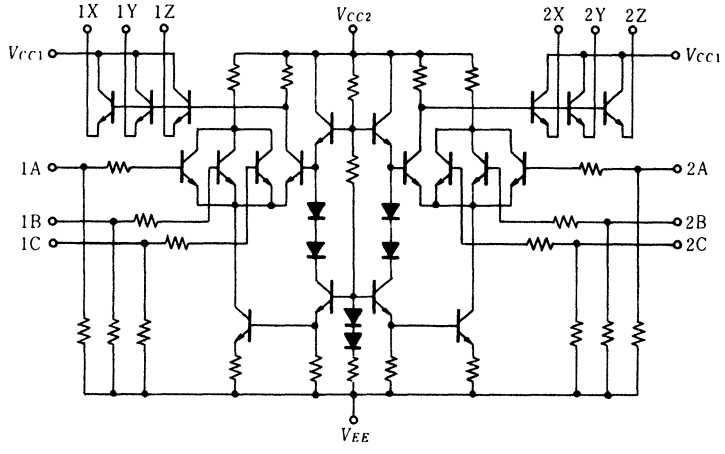
Dual High Speed 3-input OR Gates

■PIN ARRANGEMENT



(Top View)

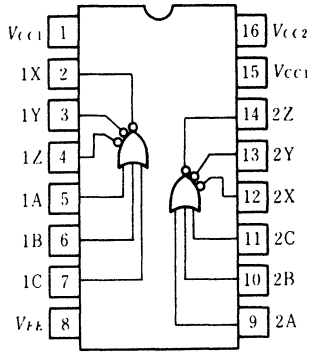
■CIRCUIT SCHEMATIC



HD10211

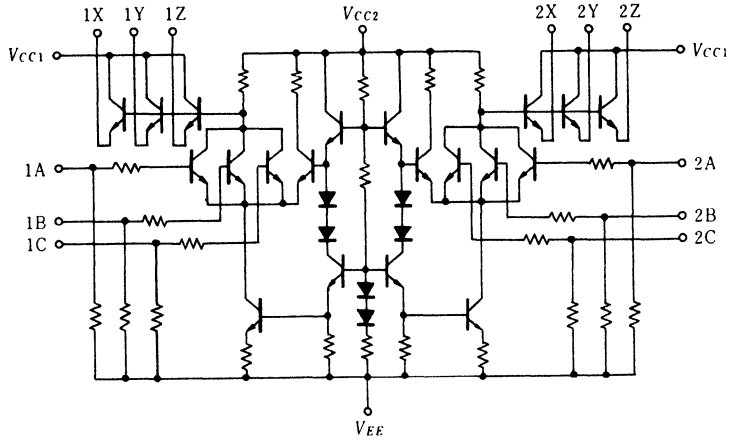
Dual High Speed 3-input 3-output NOR Gates

■ PIN ARRANGEMENT



(Top View)

■ CIRCUIT SCHEMATIC

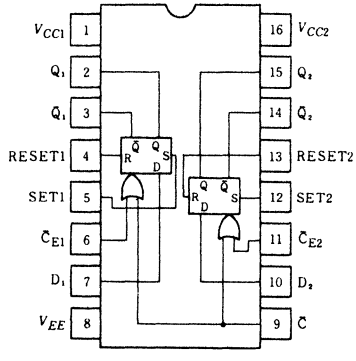


HD10230

Dual High Speed Latches

The HD10230 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock($\overline{C}$). Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{CE}$ or both are high.

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION

D	$\bar{C}$	$\bar{C}_E$	Q_{n+1}
L	L	L	L
H	L	L	H
×	L	H	Q_n
×	H	L	Q_n
×	H	H	Q_n

× : Don't Care

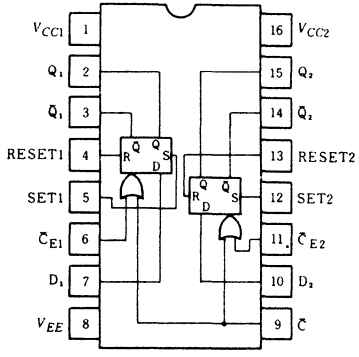
HD10231

Dual High Speed Type-D Master-Slave Flip Flops

The HD10231 is a dual master-slave type D flip-flop. Asynchronous Set(S) and Reset(R) override Clock ($\overline{C_C}$) and Clock Enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data(D) input will not affect the output information at any other time due to master-slave construction.

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

● R-S

R	S	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	Q_n	$\overline{Q}_n$
L	H	H	L
H	L	L	H
H	H	×	×

× : Don't Care

● CLOCK

C	D	Q_{n+1}
L	×	Q_n
↑	L	L
↑	H	H

1. × : Don't Care
2. $C = \overline{C_E} + \overline{C_C}$
3. ↑ : transition from low to high

HITACHI
HLN041
LITERATURE NO.

PRODUCTION STATUS

Device	Function	Production Status	
		Samples	Volume
HD100101	Triple 5-Input OR/NOR Gates	NOW	NOW
HD100102	Quint. 2-Input OR/NOR Gates	NOW	NOW
HD100107	Quint. Exclusive OR/NOR Gates	NOW	NOW
HD100112	Quadruple Drivers	NOW	NOW
HD100114	Quint. Differential Line Receivers	NOW	NOW
HD100117	Triple 2-Wide OR-AND/OR-AND-INVERT Gates	NOW	NOW
HD100118	5-Wide OR-AND/OR-AND-INVERT Gates	NOW	NOW
HD100122	9-Bit Buffers	NOW	NOW
HD100123	Hex Bus Drivers	NOW	NOW
HD100124	TTL to ECL Translator	3Q82	4Q82
HD100125	ECL to TTL Translator	3Q82	4Q82
HD100130	Triple D-Type Latches	NOW	NOW
HD100131	Triple D-Type Flip Flops	NOW	NOW
HD100136	4-Stage Counter/Shift Register	4Q81	1Q82
HD100141	8-Bit Shift Registers	NOW	NOW
HD100142	4 × 4 Content Addressable Memory	1Q82	2Q82
HD100145	16 × 4 Read/Write Register	NOW	NOW
HD100150	Hex D-Type Latches	NOW	NOW
HD100151	Hex D-Type Flip Flops	NOW	SEPT.
HD100155	Quad. Multiplexers/Latchers	4Q81	1Q82
HD100156	Mask-Merge	4Q81	1Q82
HD100158	8-Bit Shift Matrix	NOW	NOW
HD100160	Dual Parity Generators/Checkers	NOW	NOW
HD100163	Dual 8-Input Multiplexers	NOW	NOW
HD100164	16-Input Multiplexers	NOW	NOW
HD100165	Universal Priority Encoder	NOW	NOW
HD100166	9-Bit Comparators	NOW	NOW
HD100170	Universal Demultiplexers/Decoders	NOW	NOW
HD100171	Triple 4-Input Multiplexers with Enable	NOW	NOW
HD100179	Carry Look-Ahead	4Q81	1Q82
HD100180	Fast 6-Bit Adder	4Q81	1Q82
HD100181	4-Bit Binary/BCD ALU	1Q82	2Q82
HD100182	9-Bit Wallace Tree Adder	2Q83	4Q83
HD100183	2 × 8 Bit Recoder Multiplier	2Q83	4Q83
HD100194	Quint. Duplex Bus Driver (Transceiver)	2Q83	4Q83

ECL 100K
LOGIC FAMILY

100K ECL LOGIC FAMILY

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1. OUTLINE

With the increase of the information mass, the computer system requires high speed, large capacity and high reliability. To satisfy the needs, development of the semiconductor components with high speed, high integration and high reliability has been needed, and the simple mounting and the easier handling were indispensable at the same time. Hitachi has developed the 100K series which operate at a high speed (three times faster than HD10K series) and which immune from the influence by the temperature and power variations. The 100K series employ the 3μm fine pattern process and the ion implantation process, and that realizes the above mentioned high performances. The figures of merit at the gates of typical digital ICs are shown in table 1 and figure 1. The following tables shows the electrical characteristics of HD100K series.

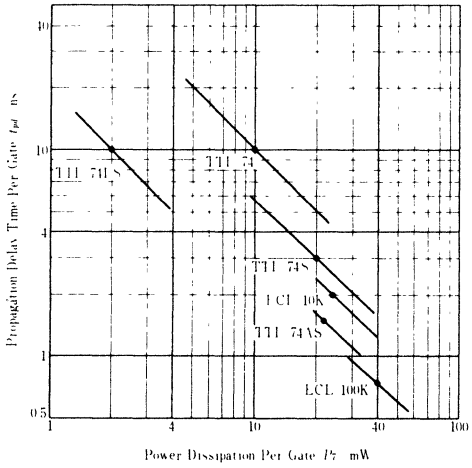


Fig.1 Propagation Delay Time vs. Power Dissipation

Table 1. Comparison of the Speed-Power Product

	HD100K	HD10K	HD74	HD74S	HD74LS
Propagation Delay Time	0.75 ns	2 ns	10 ns	3 ns	10 ns
Power Dissipation	40 mW	25 mW	10 mW	20 mW	2 mW
Speed-Power Product	30 pJ	50 pJ	100 pJ	60 pJ	20 pJ

Table 2. Electrical Characteristics ($Ta = 0 \sim +85$°C, $V_{EE} = -4.5$ V, V_{CC} : GND)

Symbol	Item	min	typ	max	Unit	Conditions	
V_{OH}	Output Voltage High	−1025	−955	−880	mV	$V_{IN} = V_{IH\ max}$	
V_{OL}	Output Voltage Low	−1810	−1705	−1620	mV	or $V_{IL\ min}$	$R_L = 50\Omega$
V_{OHA}	Output Threshold Voltage High	−1035	—	—	mV	$V_{IN} = V_{IH\ min}$	$V_{TT} = -2$ V
V_{OLA}	Output Threshold Voltage Low	—	—	−1610	mV	or $V_{IL\ max}$	
V_{IH}	Input Voltage High	−1165	—	−880	mV		
V_{IL}	Input Voltage Low	−1810	—	−1475	mV		
I_{IL}	Input Current Low	0.5	—	—	μA	$V_{IN} = V_{IL\ min}$	

Table 3. Maximum Ratings

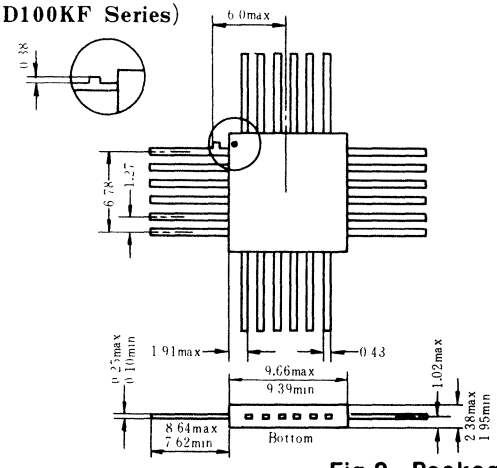
Item	Symbol	Rating	Unit
Supply Voltage*	V_{EE}	−7.0	V
Input Voltage*	V_{in}	0~V_{EE}	V
Output Current	I_O	50	mA
Surge Output Current	$I_{O(surge)}$	100	mA
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65~+150	°C

*Value at V_{CC} and V_{CCA} = GND

Table 4. Recommended Operating Conditions

Item	Symbol	Value	Unit
Operating Temperature Range	T_A	0~85	°C
Supply Voltage Range	V_{EE}	−4.2~−5.7	V

● 24 Pin Ceramic Flat Package
(HD100KF Series)



● 24 Pin Ceramic Dual-in-line Package
(HD100K Series)

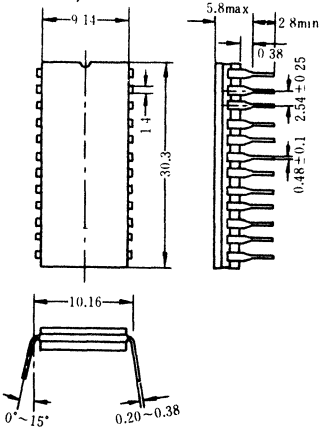


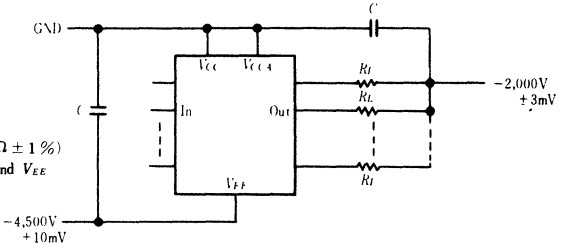
Fig.2 Package (Dimensions in mm)

2. FEATURES OF HD100K SERIES

- On-chip complementary output
  Built-in complementary output requires no application of inverters, and it avoids the problems of number of external parts, power dissipation, propagation delay and so on.
- High input impedance and low output impedance
  Due to the high input impedance (compared with TTL), more fan-out is obtained, and various circuit confideration is realized.
- Stability
  Built-in temperature and voltage compensation circuits assure the stable output characteristics within all the temperature and the voltage ranges.
- Compatibility
  HD100K series is fully compatible with F100K series on pin configulation, functions and characteristics.

3. DEFINITION OF SYMBOLS AND TESTING METHOD

3.1. DC Characteristics

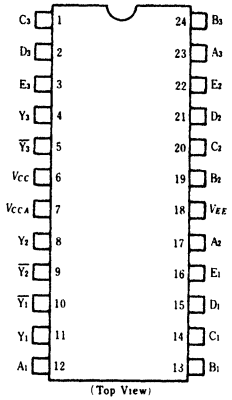


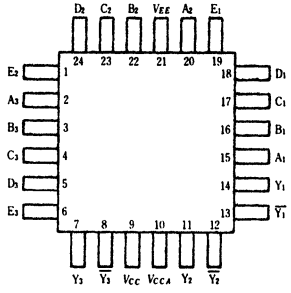
Note) 1. All outputs are loaded with 50Ω to GNG (50Ω ± 1%)
2. Decoupling 0.1μF (25V) from GND to V_{CC} and V_{EE}
3. The tolerance of to shall be ± 2°C

HD100101

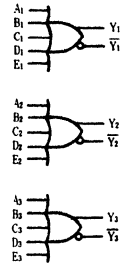
Triple 5-input OR/NOR Gates

■ PIN ARRANGEMENT





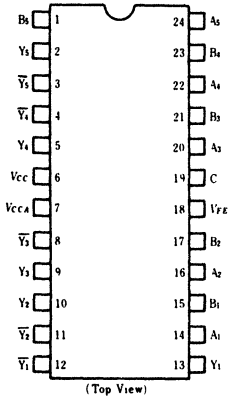
■ LOGIC DIAGRAM

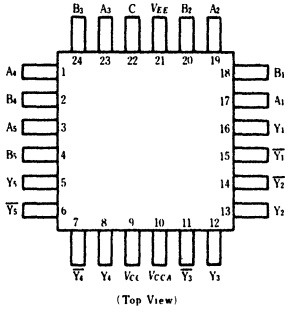


HD100102

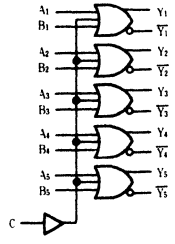
Quintuple 2-input OR/NOR Gates

■ PIN ARRANGEMENT





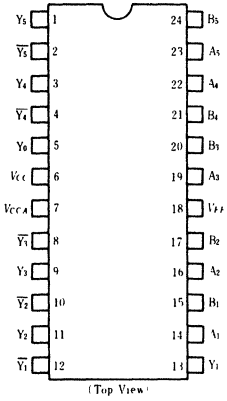
■ LOGIC DIAGRAM

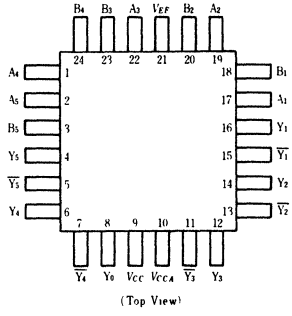


HD100107

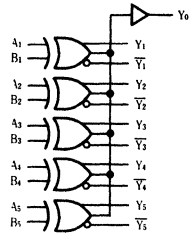
Quintuple Exclusive-OR/NOR Gates

■ PIN ARRANGEMENT





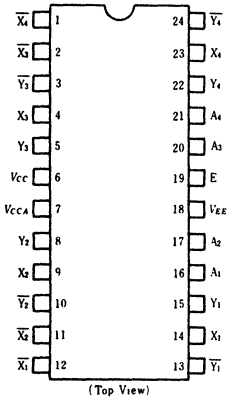
■ LOGIC DIAGRAM

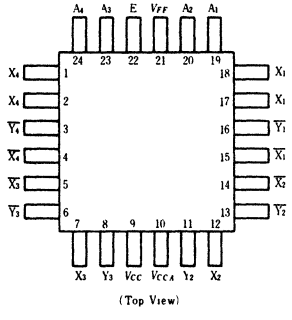


HD100112

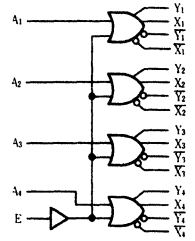
Quadruple Drivers

■ PIN ARRANGEMENT





■ LOGIC DIAGRAM



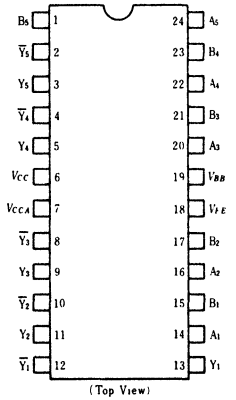
HD100114

Quint. Differential Line Receivers

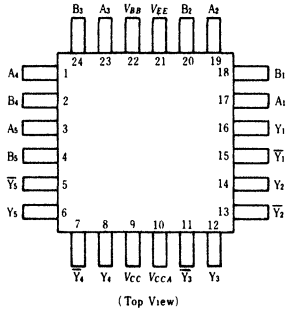
The HD100114 is a Quint. Differential Amp. with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single ended reception. Active current sources provide common mode rejection of 1.5V in either the positive or negative direction.

A defined output state exists if both inputs are at the same potential between and including $-V_{EE}$ and V_{CC}. The defined state is logic high on outputs $\overline{Yn}$.

■ PIN ARRANGEMENT

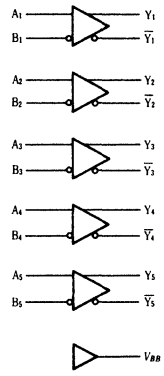


(Top View)



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

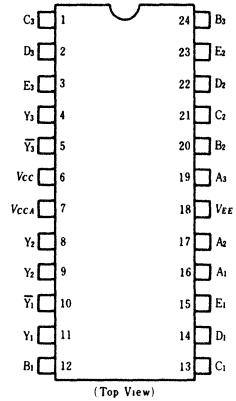
Input		Output	
A_n	B_n	Y_n	$\overline{Y_n}$
H	V_{BB}	H	L
L	V_{BB}	L	H
V_{BB}	H	L	H
V_{BB}	L	H	L
$A_n - B_n \geq 0.15$ V		H	L
$A_n - B_n \leq 0.0$ V		L	H
$0.0 < A_n - B_n < 0.15$ V		*	*
Open	Open	L	H
V_{CC}	V_{CC}	L	H
V_{EE}	V_{EE}	L	H

H = High level
L = Low level
V_{BB} = Base bias voltage
* = Undefined

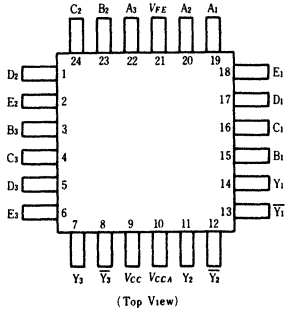
HD100117

Triple 2-wide OR-AND/OR-AND-INVERT Gates

■ PIN ARRANGEMENT

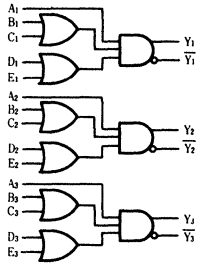


(Top View)



(Top View)

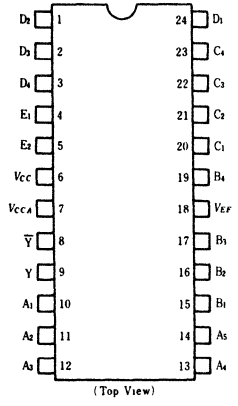
■ LOGIC DIAGRAM



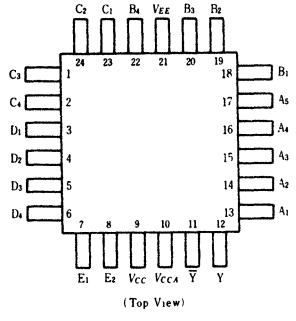
HD100118

5-wide OR-AND/OR-AND-INVERT Gates

■ PIN ARRANGEMENT

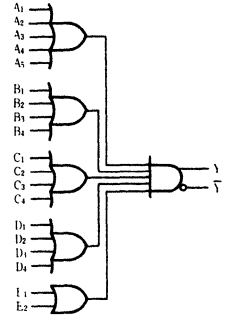


(Top View)



(Top View)

■ LOGIC DIAGRAM

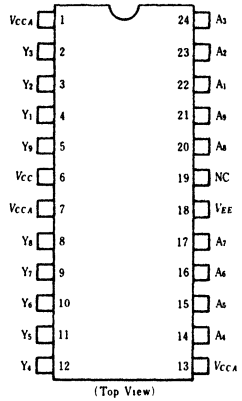


HD100122

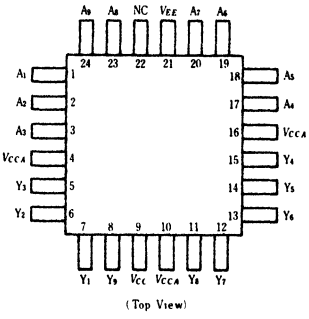
9-bit Buffers

The HD100122 contains nine independent, high speed, buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus oriented systems where minimal output loading or bus isolation is desired.

■ PIN ARRANGEMENT



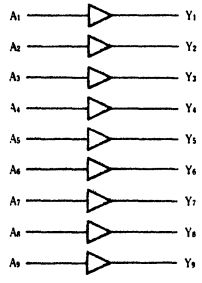
(Top View)



(Top View)

Note) NC : No connection

■ LOGIC DIAGRAM

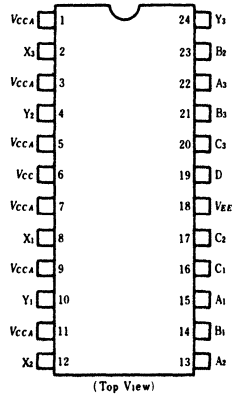


HD100123

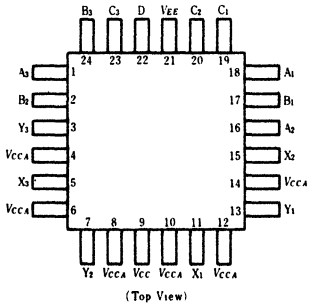
Hex Bus Drivers

The HD100123 contains six bus drivers capable of driving terminated lines with terminations as low as 25Ω. To reduce crosstalk, each output has its respective ground connection and transition times were designed to be longer than on other HD100K devices.
The driver itself performs the positive logic AND of a data input (A, B inputs) and the OR of two select inputs (C, D inputs).
The output voltage low level is designed to be more negative than normal ECL outputs.
This allows an emitter-follower output transistor to turn off when the termination supply is −2.0V ±10%, and thus present a high impedance to the data bus.

■ PIN ARRANGEMENT

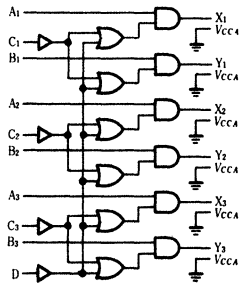


(Top View)



(Top View)

■ LOGIC DIAGRAM

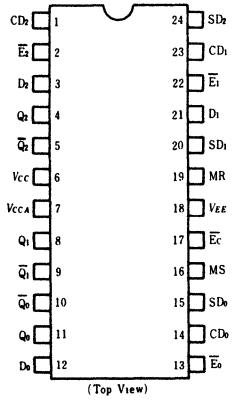


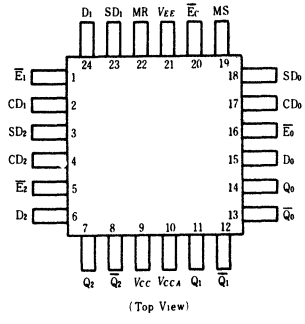
HD100130

Triple D-type Latches

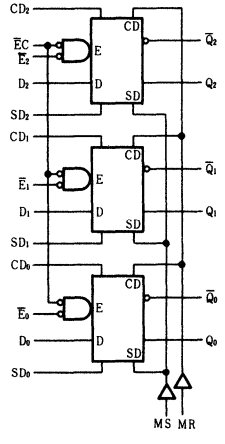
The HD100130 contains three D-type latches with true and complement outputs and with Common Enable ($\overline{Ec}$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{En}$), Direct Set (SDn) and Direct Clear (CDn) inputs.
The Q output follows its Data (D) input when both $\overline{En}$ and $\overline{Ec}$ are low. When either $\overline{En}$ or $\overline{Ec}$ or both are high, a latch stores the last valid data present on its Dn input before $\overline{En}$ or $\overline{Ec}$ went high. Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs.
The individual CDn and SDn also override the Enable inputs.

■ PIN ARRANGEMENT





■ LOGIC DIAGRAM



■ TRUTH TABLE

D_n	$\overline{E_n}$	$\overline{Ec}$	MS SD_n	MR CD_n	Q_n
L	L	L	L	L	L
H	L	L	L	L	H
×	H	×	L	L	*
×	×	H	L	L	*
×	×	×	H	L	H
×	×	×	L	H	L
×	×	×	H	H	U

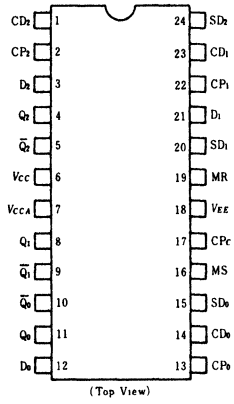
H = High level
L = Low level
× = Immaterial
* = Ratains data present before $\overline{E}$ positive transition
U = Undefined

HD100131

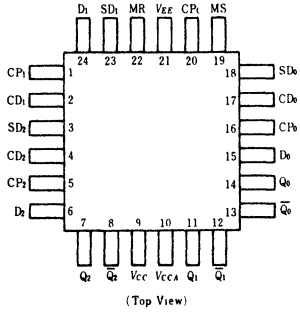
Triple D-type Flip Flops

The HD100131 contains three D-type Master-Slave Flip Flops with true and complement outputs, a Common Clock (CPc), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual clocks (CPn), Direct Set (SDn) and Direct Clear (CDn) inputs. Data enters a master when both CPn and CPc are low and transfers to a slave when CPn or CPc (or both) go high.
The Master Set, Master Reset and individual CDn and SDn inputs override the Clock inputs.

■ PIN ARRANGEMENT

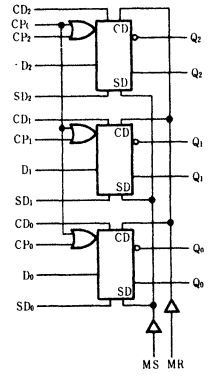


(Top View)



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

D_n	CP_n	CP_C	MS SD_n	MR CD_n	Q_{n+1}
L	↑	L	L	L	L
H	↑	L	L	L	H
L	L	↑	L	L	L
H	L	↑	L	L	H
×	H	×	L	L	Q_n
×	×	H	L	L	Q_n
×	×	×	H	L	H
×	×	×	L	H	L
×	×	×	H	H	U

H = High level
L = Low level
× = Immaterial
U = Undefined
↑ = Clock transition from low level to high level

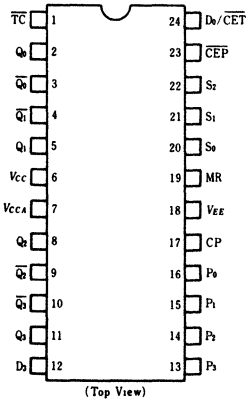
HD100136

4-stage Counter/Shift Register

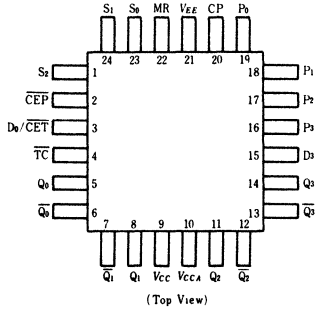
The HD100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (Sn) inputs determine the mode of operation, as shown in the mode select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multi-stage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (Do) input for shift-up operation.

For shift-down operation D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes low when the counter reaches 15 in the count/up mode or 0 in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $Do/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multi-stage counting or shift-up operation. The individual Preset (Pn) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A high signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the fli-flops. In addition, asynchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops.

■ PIN ARRANGEMENT



(Top View)



(Top View)

■ FUNCTION SELECT TABLE

S_0	S_1	S_2	Function
L	L	L	Load
L	H	L	Shift down
H	H	L	Shift up
L	L	H	Count down
L	H	H	Count up
H	H	H	Hold
H	L	L	Complement
H	L	H	Clear

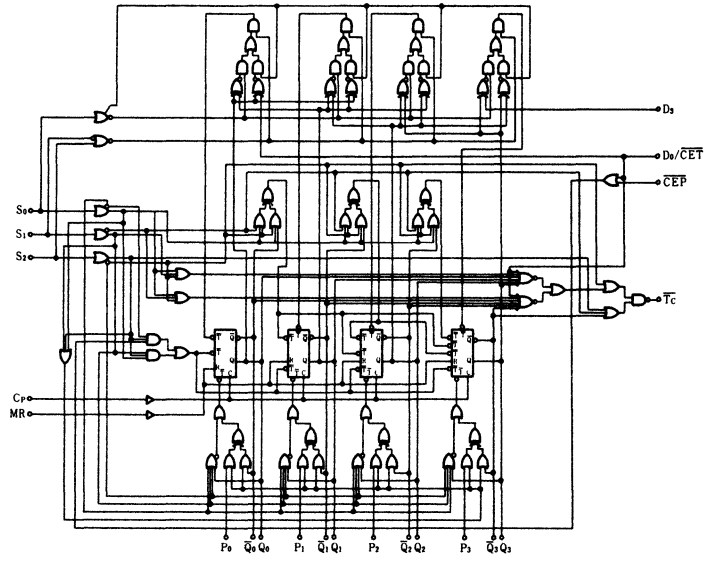
H = High level
L = Low level

■ TRUTH TABLE

IN												OUT					Mode
S_0	S_1	S_2	C_P	M_R	CEP	D_0/$\overline{CET}$	D_3	P_3	P_2	P_1	P_0	Q_3	Q_2	Q_1	Q_0	$\overline{TC}$	
L	L	L	↑	L	×	×	×	H	L	H	H	H	L	H	H	L	Load ☆
H	H	H	↑	L	×	×	×	×	×	×	×	H	L	H	H	H	Hold
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	L	L	H	Count up(max)
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	L	H	H	
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	H	L	H	
L	H	H	↑	L	L	L	×	×	×	×	×	H	H	H	H	L	
L	H	H	↑	L	L	L	×	×	×	×	×	L	L	L	L	H	
L	H	H	↑	L	L	L	×	×	×	×	×	L	L	L	H	H	
L	H	H	×	L	L	H	×	×	×	×	×	L	L	L	H	H	($\overline{CET}$ inhibit)
L	H	H	×	L	H	L	×	×	×	×	×	L	L	L	H	H	($\overline{CEP}$ inhibit)
H	H	H	↑	L	×	×	×	L	H	L	L	L	H	L	L	L	Load ☆
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	H	H	H	Count down(min)
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	H	L	H	
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	L	H	H	
L	L	H	↑	L	L	L	×	×	×	×	×	L	L	L	L	L	
L	L	H	↑	L	L	L	×	×	×	×	×	H	H	H	H	H	
L	L	H	↑	L	L	L	×	×	×	×	×	H	H	H	L	H	
H	L	L	↑	L	×	×	×	×	×	×	×	L	L	L	H	L	Complement
H	L	H	↑	L	×	L	×	×	×	×	×	L	L	L	L	H	Clear
H	H	L	↑	L	×	H	L	×	×	×	×	L	L	L	H	L	Shift up
H	H	L	↑	L	×	L	L	×	×	×	×	L	L	H	L	L	
H	H	L	↑	L	×	H	L	×	×	×	×	L	H	L	H	L	
H	H	L	↑	L	×	L	L	×	×	×	×	H	L	H	L	H	
×	×	×	×	H	×	×	×	×	×	×	×	L	L	L	L	L	Clear(MR)
L	H	L	↑	L	×	L	H	×	×	×	×	H	L	L	L	H	Shift down
L	H	L	↑	L	×	L	L	×	×	×	×	L	H	L	L	L	
L	H	L	↑	L	×	L	H	×	×	×	×	H	L	H	L	H	
L	H	L	↑	L	×	L	L	×	×	×	×	L	H	L	H	L	

× = Immaterial
☆ = each LOAD data
↑ = CP positive transition

■ LOGIC DIAGRAM

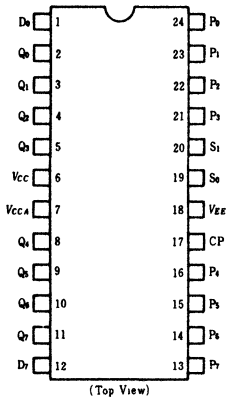


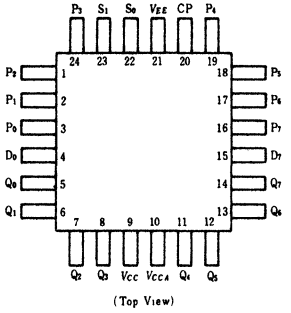
HD100141

8-bit Shift Registers

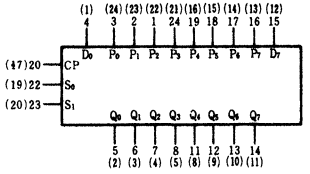
The HD100141 contains eight clocked D-type flip flops with individual inputs (Pn) and outputs (Qn) for parallel operation, and with serial inputs (Dn) and steering logic for bidirectional shifting.
The flip flops accept input data a set-up time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.
The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Function Sheet Table.

■ PIN ARRANGEMENT





■ LOGIC SYMBOL



■ FUNCTION SHEET TABLE

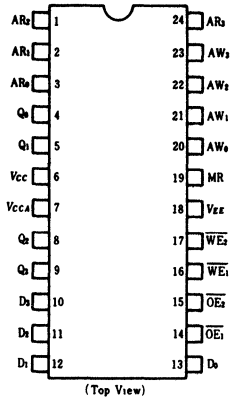
Function	Input					Output							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↑	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↑	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↑	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↑	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	← No Change →							
Hold	X	X	X	X	H	← No Change →							
Hold	X	X	X	X	L	← No Change →							

H = High Level
L = Low Level
X = Don't Care
↑ = Low to High transition

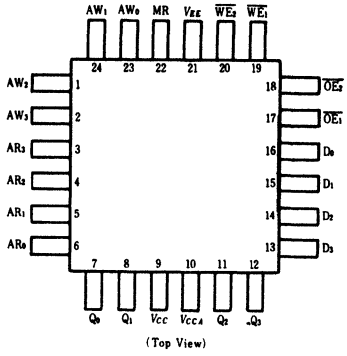
HD100145

16 × 4 Read/Write Register File

■ PIN ARRANGEMENT

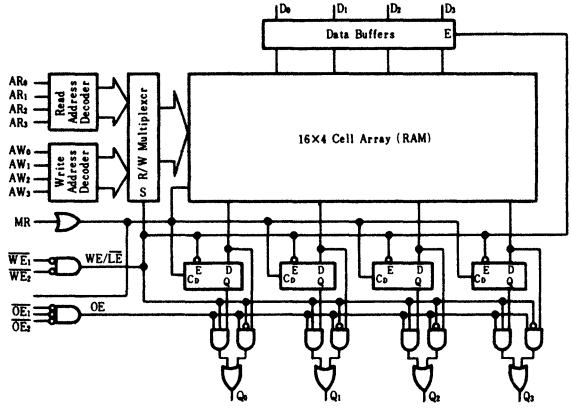


(Top View)



(Top View)

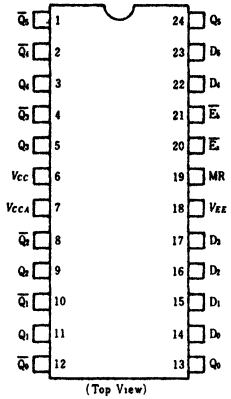
■ LOGIC DIAGRAM



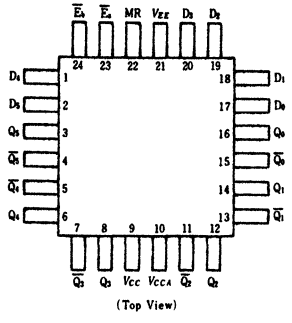
HD100150

Hex D-Type Latches

■ PIN ARRANGEMENT



(Top View)



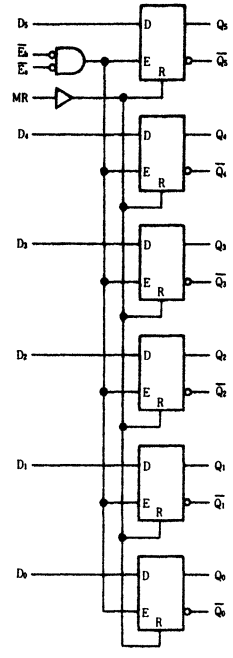
(Top View)

■ TRUTH TABLE (each latch)

Dn	$\overline{Ea}$	$\overline{Eb}$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
×	H	×	L	*
×	×	H	L	*
×	×	×	H	L

H = High Level
L = Low Level
× = Immaterial
* = Retains data present before $\overline{E}$ positive transition

■ LOGIC DIAGRAM

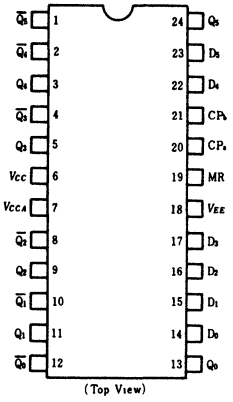


HD100151

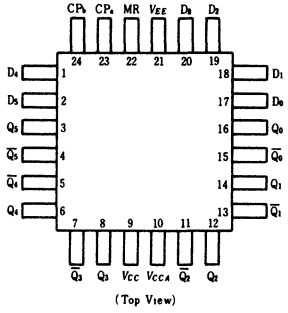
Hex D-type Flip Flops

HD100151 contains six master/slave flip flops with True and Complement outputs. A pair of Common Clock inputs (CPa and CPb) and common Master Reset (MR) input. Data enters a master when both CPa and CPb are low and transfers to the slave when CPa or CPb (or both) go high. The MR inputs overrides all other inputs and makes the Q outputs low.

■ PIN ARRANGEMENT



(Top View)



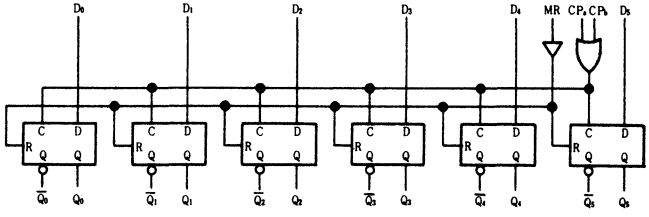
(Top View)

■ TRUTH TABLE (Each Flip Flop)

D_n	CP_a	CP_b	MR	$Q_{n(t+1)}$
L	↑	L	L	L
H	↑	L	L	H
L	L	↑	L	L
H	L	↑	L	H
×	H	↑	L	$Q_{n(t)}$
×	↑	H	L	$Q_{n(t)}$
×	×	×	H	L

× : Immaterial
t, t+1 : Time before and after CP positive transition

■ LOGIC DIAGRAM



HD100155

Quad. Multiplexers/Latches

The HD100155 contains four transparent latches, each of which can accept and store data from two sources. When both Enable (En) inputs are low, the data that appears at an output is controlled by the Select (Sn) inputs, as shown in the operating mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs low for the case where the latch is transparent (both Enables are low) and can steer a high signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1.

A positive-going signal on either Enable input latches the outputs. A high signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs low.

■ OPERATING MODE TABLE

CONTROLS				OUTPUT
$\overline{E_1}$	$\overline{E_2}$	$\overline{S_0}$	S_1	Q_n
H	×	×	×	latched*
×	H	×	×	latched*
L	L	L	L	D_{0n}
L	L	L	H	$D_{0n}+D_{1n}$
L	L	H	L	L
L	L	H	H	D_{1n}

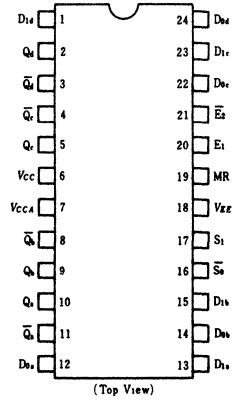
H = High Level
L = Low Level
× = Immaterial
* = Stores data present before $\overline{E}$ went high.

■ TRUTH TABLE

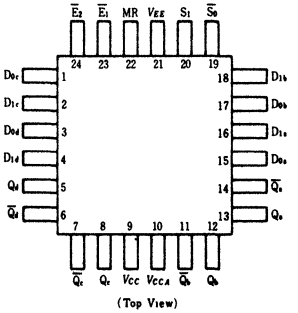
Input							Output	
MR	$\overline{E_1}$	$\overline{E_2}$	S_1	$\overline{S_0}$	D_{1a} D_{1b} D_{1c} D_{1d}	D_{0a} D_{0b} D_{0c} D_{0d}	$\overline{Q_a}$ $\overline{Q_b}$ $\overline{Q_c}$ $\overline{Q_d}$	Q_a Q_b Q_c Q_d
H	×	×	×	×	×	×	H	L
L	L	L	H	H	H	×	L	H
L	L	L	H	H	L	×	H	L
L	L	L	L	L	×	H	L	H
L	L	L	L	L	×	L	H	L
L	L	L	L	H	×	×	H	L
L	L	L	H	L	H	×	L	H
L	L	L	H	L	×	H	L	H
L	L	L	H	L	L	L	H	L
L	H	×	×	×	×	×	No Change	
L	×	H	×	×	×	×	No Change	

H = High Level
L = Low Level
× = Immaterial

■ PIN ARRANGEMENT

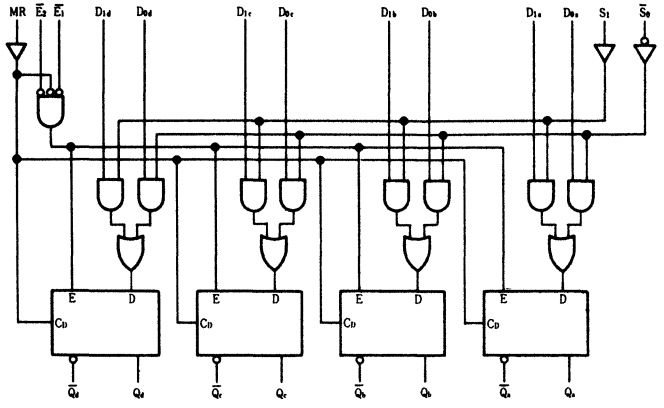


(Top View)



(Top View)

■ LOGIC DIAGRAM

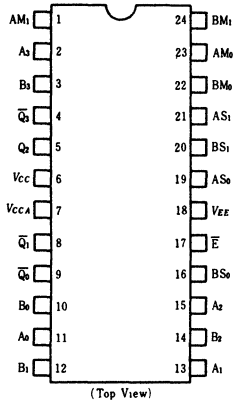


HD100156

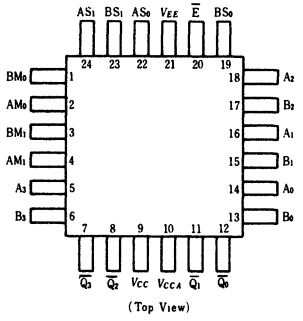
Mask-merge

The HD100156 merges two 4-bit words to form a 4-bit output word. The AMj enable allows the merge of An into Bn by one, two, or three places (per the ASj value) from the left. The BMj enable similarly allows the merge of Bn into An from the left (per the BSj value). The Bn merge overrides the An merge when both are enabled.
This means An first merges into Bn and Bn then merges into the An merge. A Bn address (BSj) greater than or equal to the An address (ASj) thus forces the outputs to all Bn.
The merge outputs feed 4 latches, which have a common enable ($\overline{E}$) input. All inputs have a 50kΩ (typ.) pull-down resistor tied to V_{EE}.
All four outputs do not have pull-down resistors, so they have wired-OR capability and will require external resistors.

■ PIN ARRANGEMENT

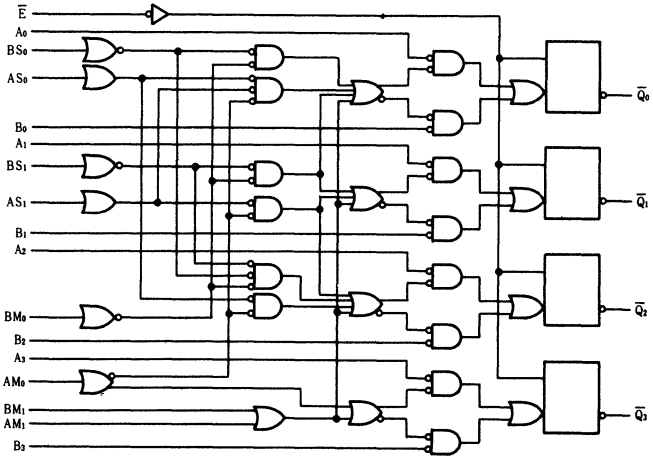


(Top View)



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE

Input									Output				
BM_1	BM_0	AM_1	AM_0	BS_1	BS_0	AS_1	AS_0	$\overline{E}$	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	
×	×	H	×	×	×	×	×	L	B_0	B_1	B_2	B_3	
H	×	×	×	×	×	×	×	L	B_0	B_1	B_2	B_3	
L	L	L	L	×	×	×	×	L	A_0	A_1	A_2	A_3	
L	L	L	H	×	×	L	L	L	B_0	B_1	B_2	B_3	
L	L	L	H	×	×	L	H	L	A_0	B_1	B_2	B_3	
L	L	L	H	×	×	H	L	L	A_0	A_1	B_2	B_3	
L	L	L	H	×	×	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	×	×	L	A_0	A_1	A_2	A_3	
L	H	L	L	L	H	×	×	L	B_0	A_1	A_2	A_3	
L	H	L	L	H	L	×	×	L	B_0	B_1	A_2	A_3	
L	H	L	L	H	H	×	×	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	L	L	B_0	A_1	B_2	B_3	
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	B_3	
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	ADDRESS (BS) > ADDRESS (AS)
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
×	×	×	×	×	×	×	×	H	Q_0	Q_1	Q_2	Q_3	

H = High Level
L = Low Level
× = Don't Care

HD100158

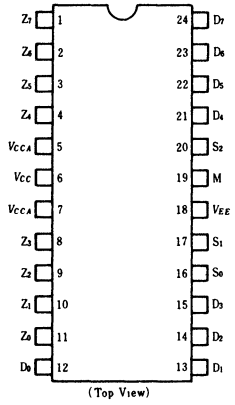
8-bit Shift Matrix

The HD100158 contains a combinatorial network which performs the function of an 8-bit shift matrix. Three control lines (Sn) are internally decoded and define the number of places which an 8-bit word present at the inputs (Dn) is shifted to the left and presented at the outputs (Zn). A Mode Control input (M) is provided which if low, forces low all outputs to the right of the one that contain D_7. This operation is sometimes referred to as "low backfill".

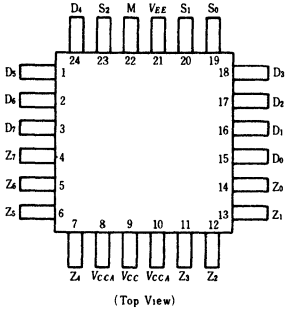
If M is high, an end-round shift is performed such that D_0 appears at the output to the right of the one that contains D_7.

This operation is commonly referred to as "barrel shifting".

■ PIN ARRANGEMENT



(Top View)



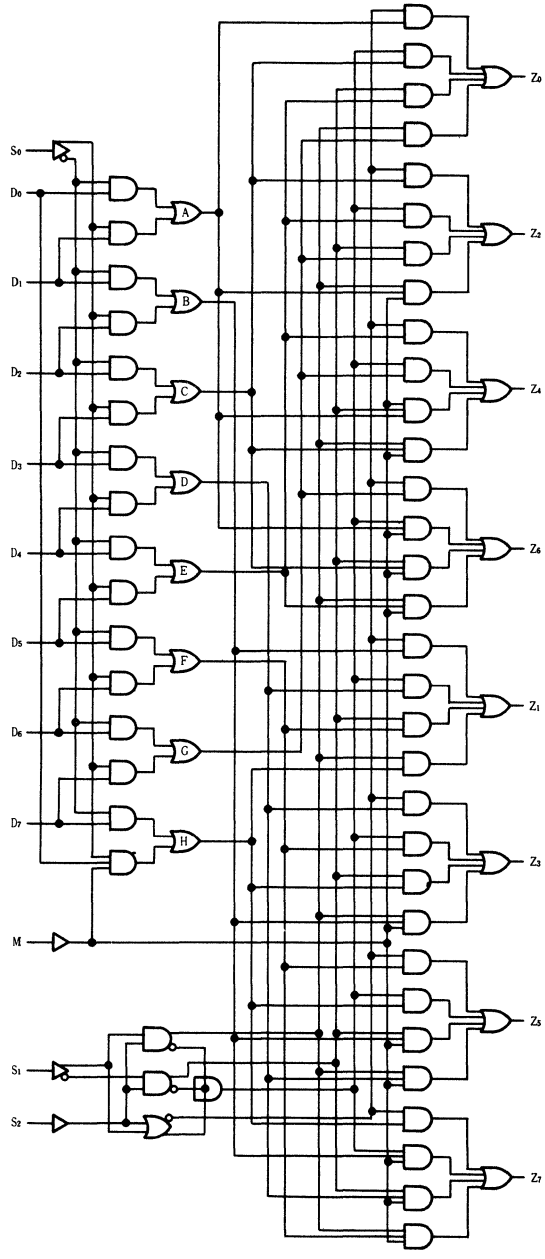
(Top View)

■ TRUTH TABLE

INPUT				OUTPUT							
M	S_0	S_1	S_2	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
×	L	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
L	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L
L	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	L	L
L	H	H	L	D_3	D_4	D_5	D_6	D_7	L	L	L
L	L	L	H	D_4	D_5	D_6	D_7	L	L	L	L
L	H	L	H	D_5	D_6	D_7	L	L	L	L	L
L	L	H	H	D_6	D_7	L	L	L	L	L	L
L	H	H	H	D_7	L	L	L	L	L	L	L
H	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0
H	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1
H	H	H	L	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2
H	L	L	H	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3
H	H	L	H	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4
H	L	H	H	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5
H	H	H	H	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6

H = High level
L = Low level
× = Immaterial

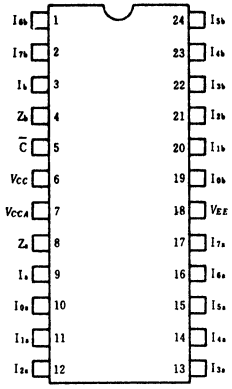
■LOGIC DIAGRAM



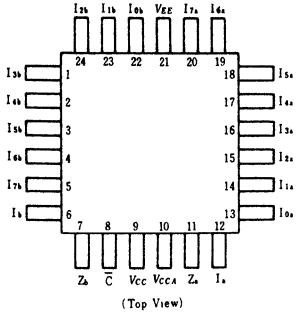
HD100160

Dual Parity Generators/Checkers

■ PIN ARRANGEMENT

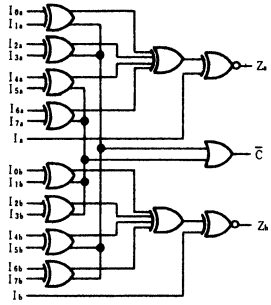


(Top View)



(Top View)

■ LOGIC DIAGRAM



■ TRUTH TABLE (each half)

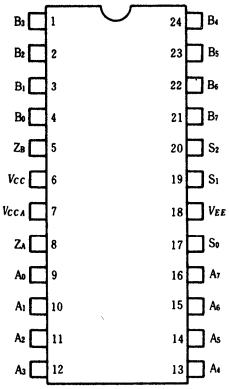
Sum of High Input	Output Z
EVEN	H
ODD	L

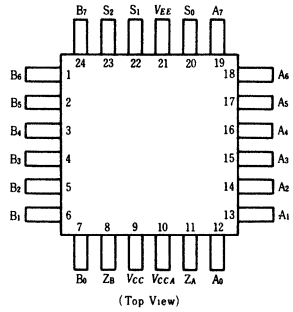
$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$

HD100163

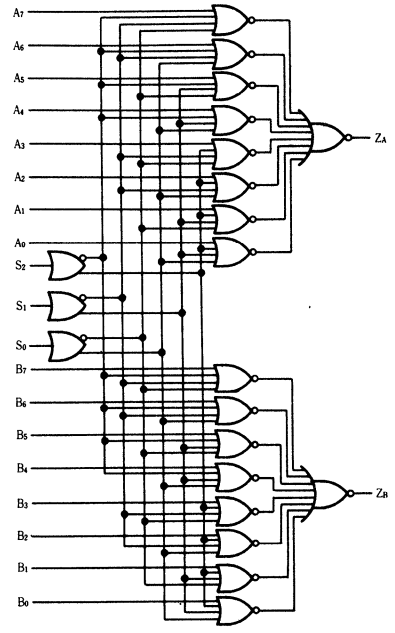
Dual 8-input Multiplexers

■ PIN ARRANGEMENT





■ LOGIC DIAGRAM



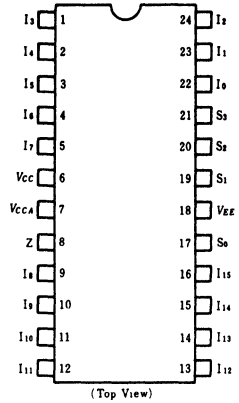
■ TRUTH TABLE

Input											Output
Address			Data								
S_2	S_1	S_0	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	
L L	L L	L L	×	×	×	×	×	×	×	L H	L H
L L	L L	H H	×	×	×	×	×	×	L H	×	L H
L L	H H	L L	×	×	×	×	×	L H	×	×	L H
L L	H H	H H	×	×	×	×	L H	×	×	×	L H
H H	L L	L L	×	×	×	L H	×	×	×	×	L H
H H	L L	H H	×	×	L H	×	×	×	×	×	L H
H H	H H	L L	×	L H	×	×	×	×	×	×	L H
H H	H H	H H	L H	×	×	×	×	×	×	×	L H

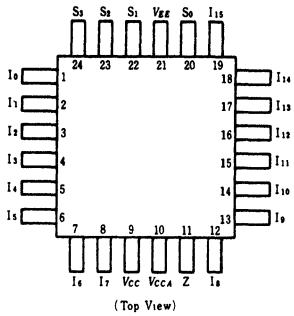
HD100164

16-input Multiplexer

■ PIN ARRANGEMENT



(Top View)

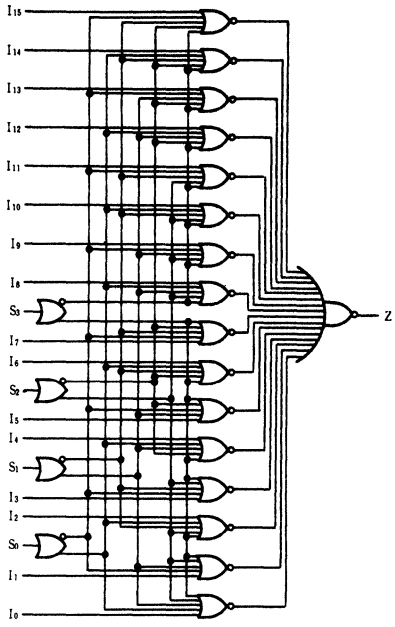


(Top View)

■ TRUTH TABLE

S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

■ LOGIC DIAGRAM



HD100165

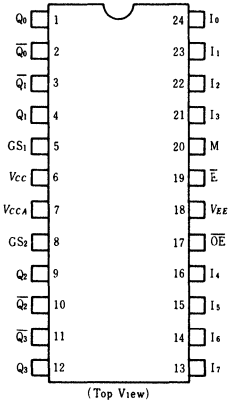
Universal Priority Encoder

The HD100165 contains eight input latches with a Common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a high signal. The circuit operates as a dual 4-input encoder when the Mode Control input (M) is low, and as a single 8-input encoder when M is high.

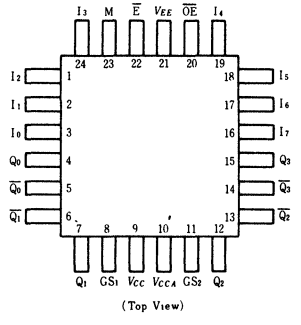
In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with I_0-I_3. Q_2, Q_3 and GS_2 operate with I_4-I_7.

A GS output goes low when its pertinent inputs are all low. Inputs are latched wher. $\overline{E}$ goes high. A high signal on the Output Enable ($\overline{OE}$) input forces all Q outputs low and GS outputs high. Expansion to acommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group.

■ PIN ARRANGEMENT



(Top View)



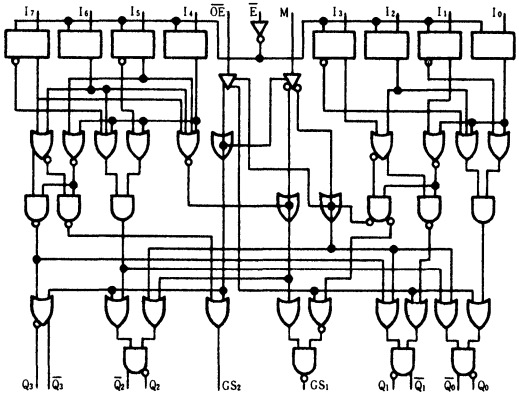
(Top View)

■ TRUTH TABLE

$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	×	×	×					L	L			H	
L	L	L	L	H	×	×					H	L			H	
L	L	L	L	L	H	×					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	×	×	×			L	L		H
L	L	L					L	H	×	×			H	L		H
L	L	L					L	L	H	×			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	×	×	×	×	×	×	×	L	L	L	L	H	H
L	L	H	L	H	×	×	×	×	×	×	H	L	L	L	H	H
L	L	H	L	L	H	×	×	×	×	×	L	H	L	L	H	H
L	L	H	L	L	L	H	×	×	×	×	H	H	L	L	H	H
L	L	H	L	L	L	L	H	×	×	×	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	×	×	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	×	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
×	H	×	×	×	×	×	×	×	×	×	L	L	L	L	H	H
H	L	L	×	×	×	×	×	×	×	×	*	*	*	*	*	*
H	L	H	×	×	×	×	×	×	×	×	*	*	*	*	*	*

H = High Level
L = Low Level
* = Stores data present before $\overline{E}$ went high.

■ LOGIC DIAGRAM



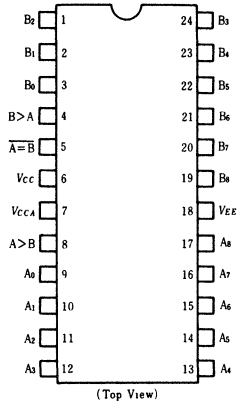
HD100166

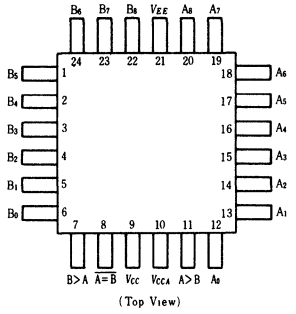
9-bit Comparators

The HD100166 is a 9-bit Magnitude Comparator which compares the arithmetic value of two 9-bit words and indicates whether one word is greater than, or equal to the other.

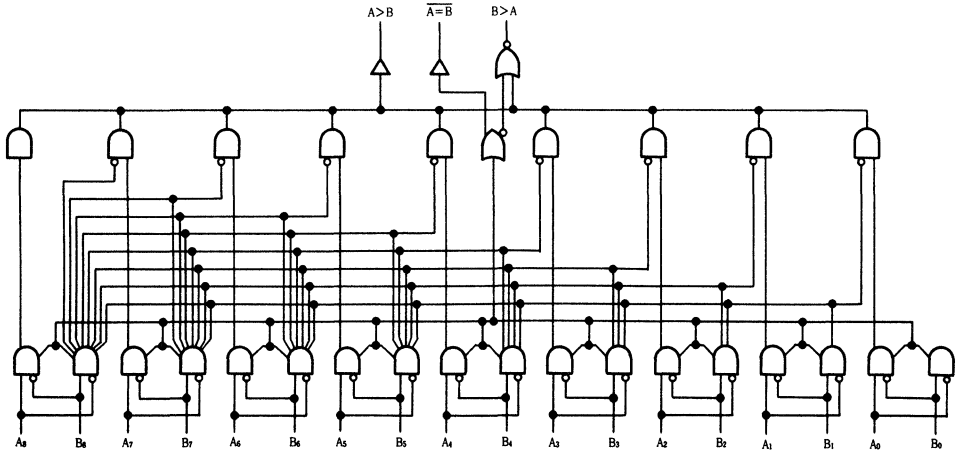
The outputs do not have pull down resistors, which provides the wire OR functions by tying several outputs together.

■ PIN ARRANGEMENT





■ LOGIC DIAGRAM



■ TRUTH TABLE

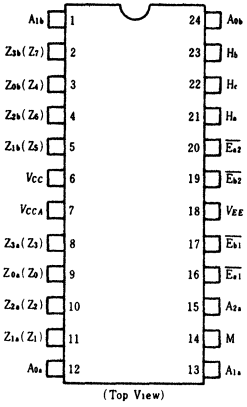
Input										Output		
A_8 B_8	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	A>B	B>A	$\overline{A=B}$
H L									H	L	H
L H									L	H	H
$A_8=B_8$	H L								H	L	H
$A_8=B_8$	L H								L	H	H
$A_8=B_8$	$A_7=B_7$	H L							H	L	H
$A_8=B_8$	$A_7=B_7$	L H							L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	H L						H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	L H						L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	H L					H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	L H					L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	H L				H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	L H				L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	H L			H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	L H			L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	H L		H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	L H		L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	H L	H	L	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	L H	L	H	H
$A_8=B_8$	$A_7=B_7$	$A_6=B_6$	$A_5=B_5$	$A_4=B_4$	$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L

H = High Level
L = Low Level
Blank = Don't care

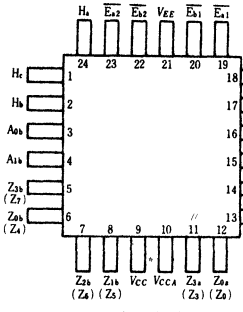
HD100170

Universal Demultiplexers/Decoders

■ PIN ARRANGEMENT

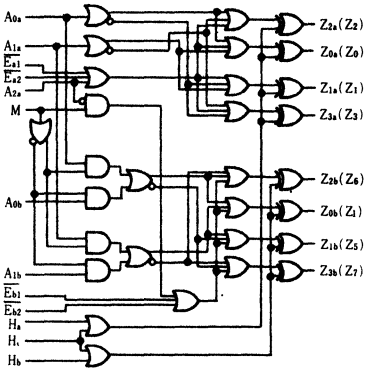


(Top View)



(Top View)

■ LOGIC DIAGRAM



(Z_n) for 1-of-8 applications

■ TRUTH TABLE

● Dual 1-of-4 Mode ($M=A_{2a}=H_C=L$)

Input				Active High Output ($H_a, H_b=H$)				Active Low Output ($H_a, H_b=L$)			
$\overline{E_{a1}}$	$\overline{E_{a2}}$	A_{1a}	A_{0a}	Z_{0a}	Z_{1a}	Z_{2a}	Z_{3a}	Z_{0a}	Z_{1a}	Z_{2a}	Z_{3a}
$\overline{E_{b1}}$	$\overline{E_{b2}}$	A_{1b}	A_{0b}	Z_{0b}	Z_{1b}	Z_{2b}	Z_{3b}	Z_{0b}	Z_{1b}	Z_{2b}	Z_{3b}
H	×	×	×	L	L	L	L	H	H	H	H
×	H	×	×	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

● Single 1-of-8 Mode ($M=H$: $A_{0b}=A_{1b}=H_a=H_b=L$)

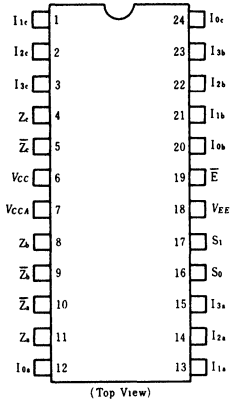
Input					Active High Output ($H_C=H$)*							
$\overline{E_1}$	$\overline{E_2}$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	×	×	×	×	L	L	L	L	L	L	L	L
×	H	×	×	×	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

*for H_C=Low, Output states are complemented.

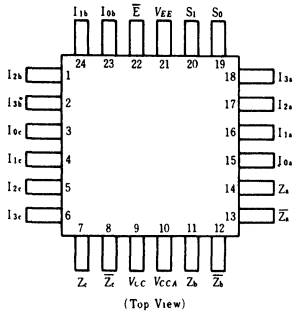
HD100171

Triple 4-input Multiplexers with Enable

■ PIN ARRANGEMENT



(Top View)

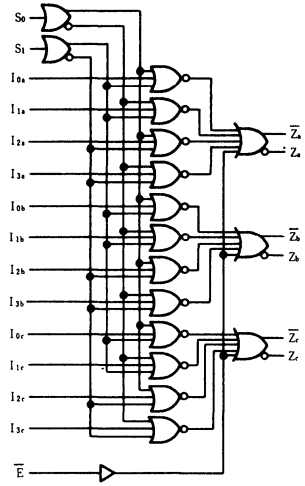


(Top View)

■ TRUTH TABLE

$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0n}
L	H	L	I_{1n}
L	L	H	I_{2n}
L	H	H	I_{3n}
H	×	×	L

■ LOGIC DIAGRAM



HD100422

HITACHI
HLN203
LITERATURE NO.

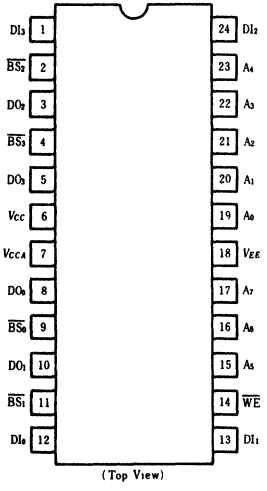
256-word × 4-bit Fully Decoded Random Access Memory

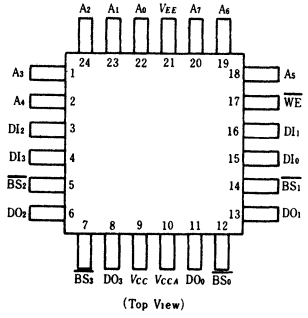
The HM100422 is ECL 100K compatible, 256-word x 4-bit, read/write, random access memory developed for high speed system such as scratch pads and control/buffer storages.
Four active low Block Select lines are provided to select each block independently.
The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.
The HM100422 is encapsulated in cerdip-24pin package, compatible with Fairchild's F100422.

■ FEATURES

- 256-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipaiton: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ PIN ARRANGEMENT



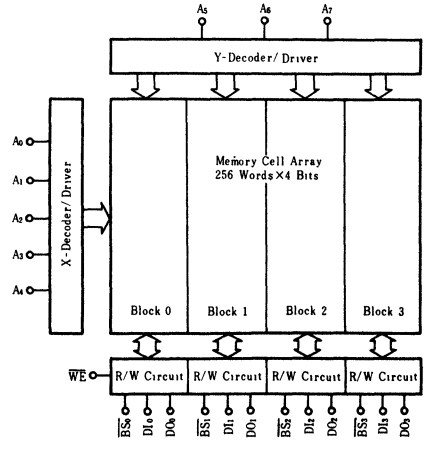


■ TRUTH TABLE

Item			Output	Mode
$\overline{BS}$	$\overline{WE}$	D_{IN}		
H	×	×	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	D_{out}*	Read

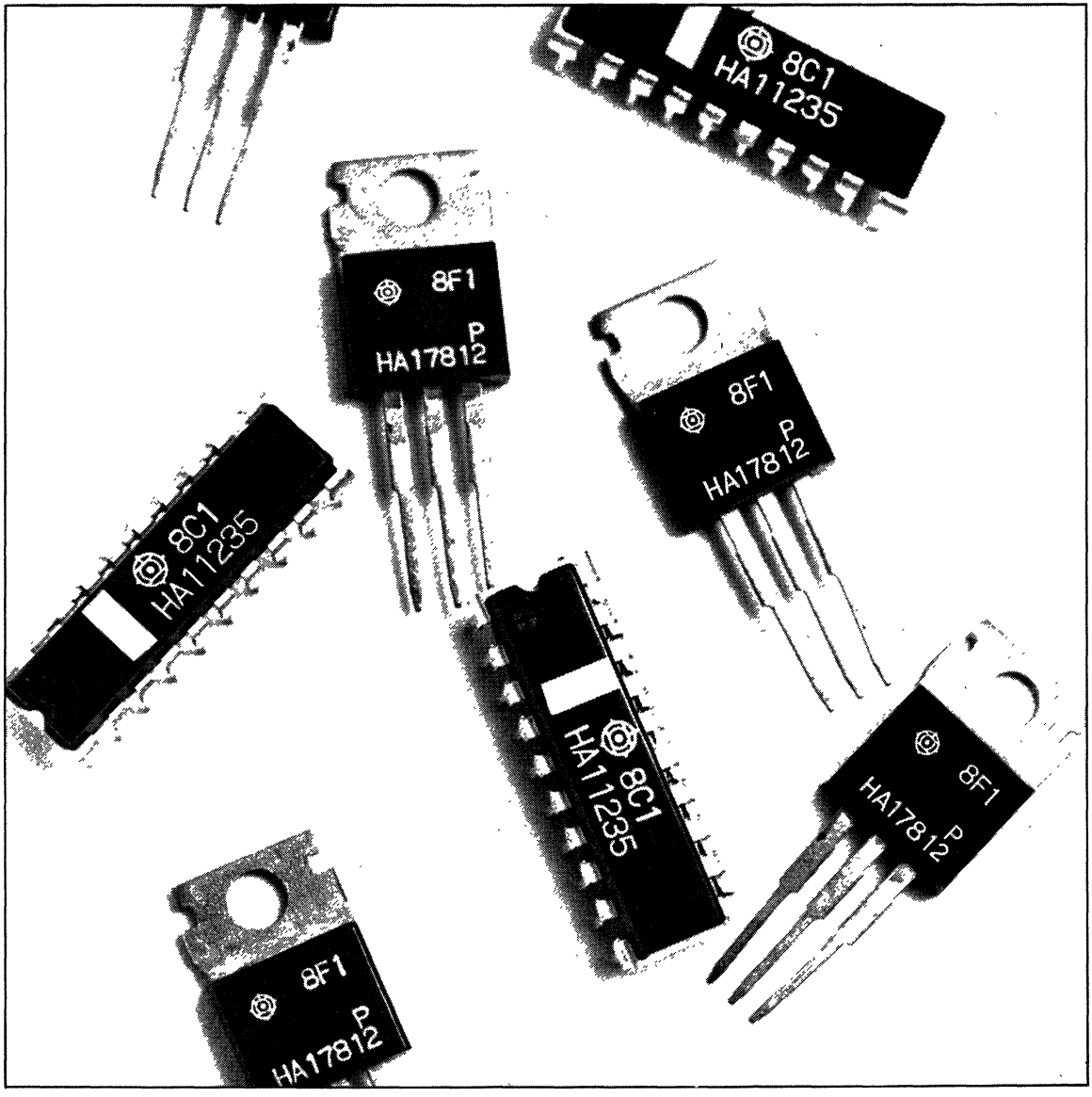
Notes) × : irrelevant
* : Read out noninvert.

■ BLOCK DIAGRAM



SECTION 5

LINEAR



HITACHI

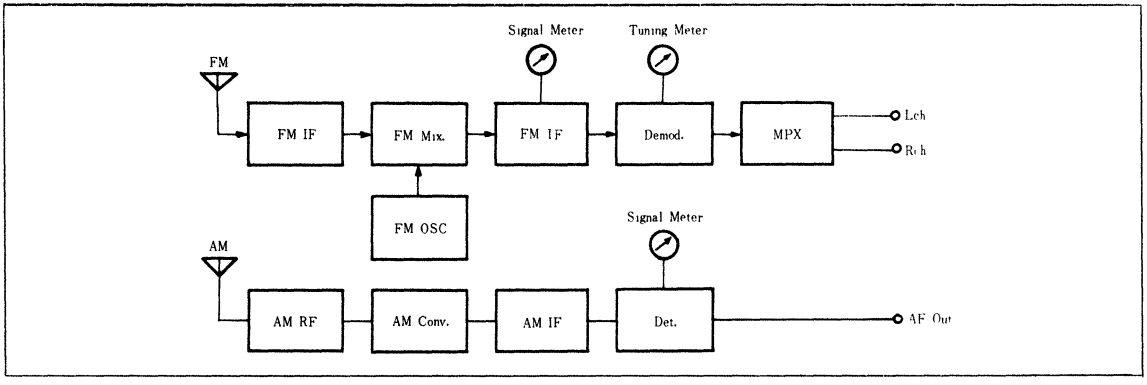
QUICK REFERENCE GUIDE

■ FM/AM RECEIVER

Type No.	Outline	Electrical Performance						Recommended Application			Remarks
		AM-RF Conv.	AM-IF Amp.	AM Det.	FM-IF Amp.	FM Demod.	Other	Tuner Receiver	Radio	Car Use	
HA11225	DP-16				●	●	Muting Tuning Meter Signal Meter	●			Muting level variable S/N : 84dB typ.
HA12411	DP-16				●	●	Muting Tuning Meter Signal Meter	○		●	
HA12412	DP-16				●	●	Muting Tuning Meter Signal Meter	●			Tuning meter short-circuit for AM-band
HA12413	DP-16		●	●	●	●	Audio Amp., Muting Tuning Meter Signal Meter	○	●		V_{CC}=3~16V. Low operating current
HA12417	SP-16	●	●	●						●	Good strong field
HA12418	SP-16				●	●	Muting Tuning Meter Signal Meter	○		●	

■ FM STEREO DEMODULATOR

Type No.	Outline	Electrical Performance				Recommended Application			Remarks
		Demodulation System	Pilot Canceller	Post Amp.	Lamp Driver	Tuner Receiver	Radio	Car Use	
HA12016	DP-16	PLL	●	●	●	●			S/N : 88dB typ. G_V : 12.5dB typ.
HA12018	SP-16	PLL			●		●	●	G_V : −1.4dB Low supply voltage operation



■ OUTLINE

SP-16

DP-16

■ POWER IC LINE UP

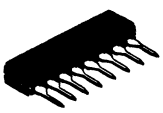
Type No.	Outline	Maximum Ratings		Electrical Characteristics			Recommended Application				Remarks
							Hi Fi Amp.	Car Use	Cassette Tape Recorder	Home Stereo	
		P_T(W)	V_{CC}(V)	P_{out}(W)	R_L(Ω)	V_{CC}(V)					
HA1374	SP-10TA	7.2	22	3.0×2	8	15			○	●	2 channel built-in
HA1374A	SP-10TA	7.2	25	4.0×2	8	17			○	●	2 channel built-in
HA1377	SP-12T	15	18	5.8×2	4	13.2		●	○		2 channel buit-in
HA1377A	SP-12T	15	18	5.8×2	4	13.2		●	○		2 channel built-in
				17							BTL connection
HA1388	SP-12T	15	18	18	4	13.2		●		○	BTL system
HA1389/R	SP-10TA	7.2	30	7	8	22			○	●	
HA1392	SP-12T	15	20	4.3×2	4	12			●	○	2 channel built-in
				6.8×2	4	15					
HA1394	SP-12T	15	35	8.2×2	8	25			○	●	2 channel built-in
HA1397	SP-12T	30	±30	20	8	±22	●			○	2 supplies system
HA1398	SP-12T	15	18	5.8×2	4	13.2		●	○		2 channel built-in

■ PREAMPLIFIER IC LINE UP

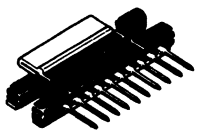
Type No.	Outline	Maximum Ratings		Electrical Characteristics				Recommended Application				Remarks
				Noise	THD (%)	$G_{V(OL)}$ (dB)	V_{out} (V)	Hi Fi Amp.	Car Use	Cassette Tape Recorder	Home Stereo	
		P_T(mW)	V_{CC}(V)									
HA12012	SP-8	250	20	$V_{n(in)}$ 0.98μV	0.07	105	2.5		●		○	2 channel built-in
HA12017	SP-8	500	±26.5	$V_{n(out)}$ 1.15mV	0.002	105	14.7	●			○	2 supplies system

■ OUTLINE

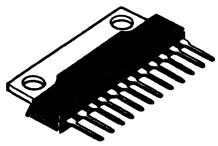
SP-8



SP-10TA

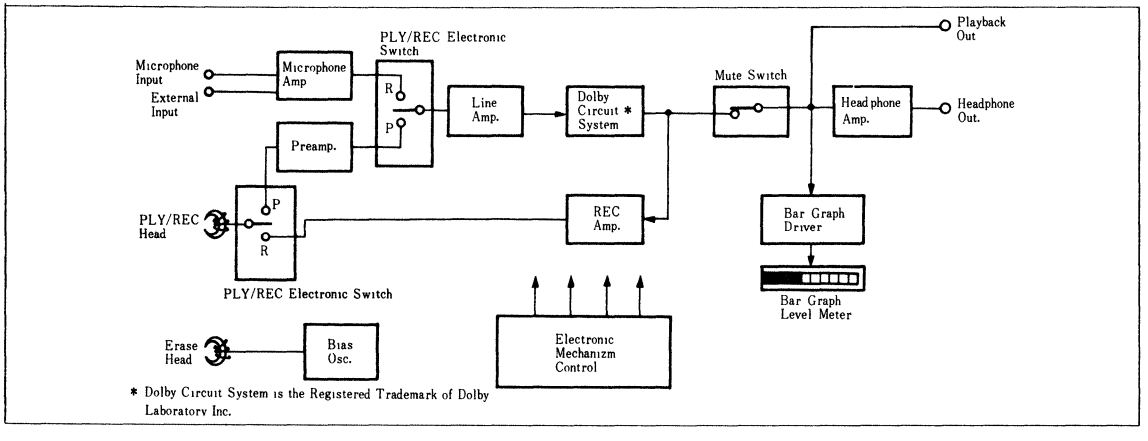


SP-12T



■ CASSETTE TAPE DECK

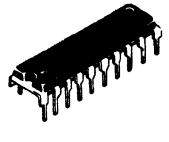
Type No.	Outline	Electrical Performance					Remarks
		PLY/REC Amp.	Headphone Amp.	Mechanizm Control	Electronic Switch	Other	
HA12001W	DP-22			●			
HA12005	DP-16	●			●		
HA12006	DP-16-2		●		●		PLY/REC Switch, Head Switch, Mute Switch, etc
HA12010	DP-16					12 point linear-scale bar-graph display	Suitable for digital indication of level meter
HA12019	DP-16					11 point log.-scale bar-graph display	



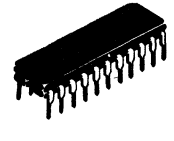
■ OUTLINE

DP-16

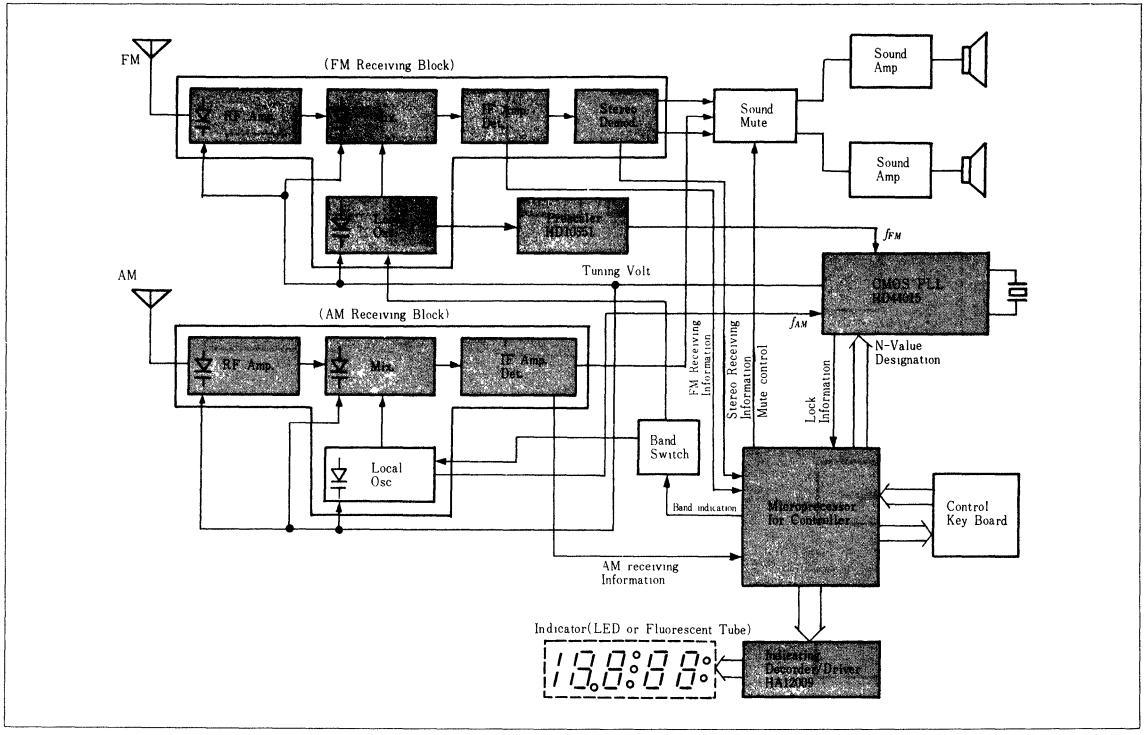
DP-16-2



DP-22



■ PLL FREQUENCY SYNTHESIZER TUNING SYSTEM

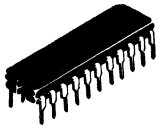


Type No.	Outline	Device	System Block	Function	Remarks
HD10551	SP-8	ECL	Prescaler	Guarantee of divide on 150MHz. Selection 1/10, 1/11, 1/20, 1/22, 1/40 and 1/44	
HD44015	DP-22	CMOS	PLL	Able to synthesize all band receiver (FM/SW/MW/LW)	
HD44752	DP-42 FP-54	CMOS	Microprocessor Controller	4 bit 1 chip microcomputer ● Function of receiving memory ● Manual scan ● Automatic scan ● Time display/timer	HD44752 is controller for 4 band European use. HD44753 is controller for FM and MW band in American and Japanese use
HD44753					
HA12009	DP-42	Bipolar	Indicating Decoder/Driver	Frequency display and time display in FM/AM 2 band tuner.	Able to drive both LED and fluorescent tube displays

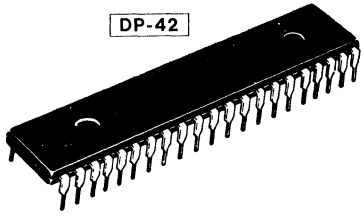
■ OUTLINE

SP-8

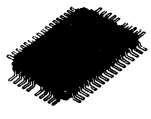
DP-22



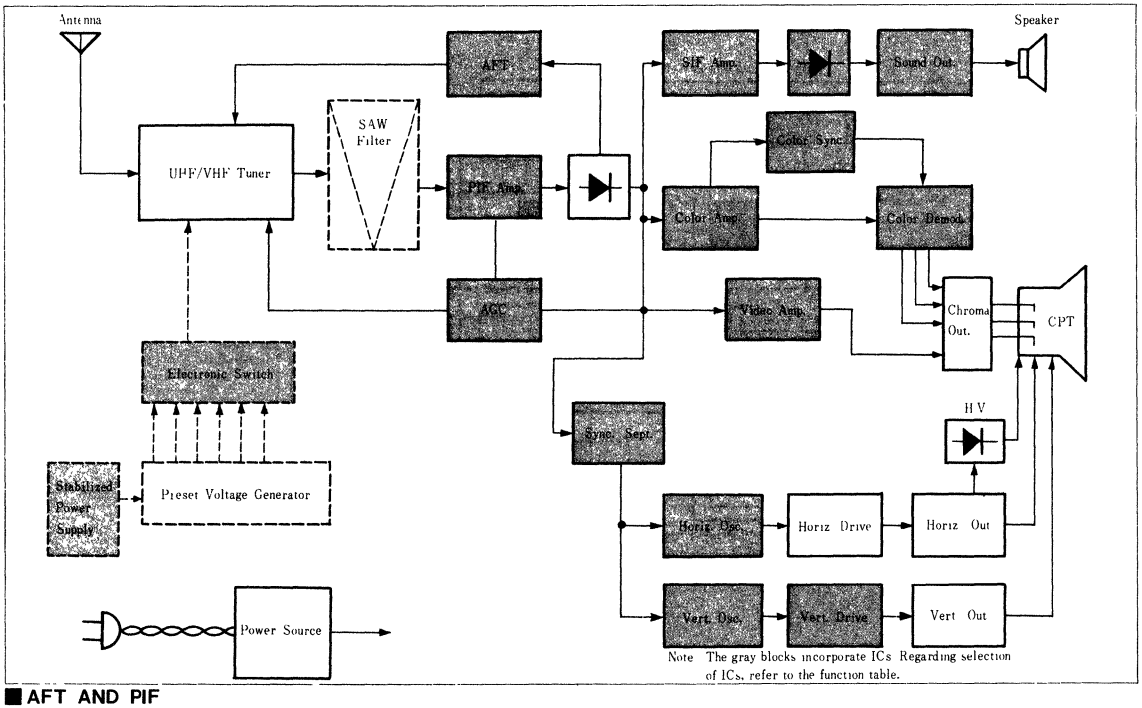
DP-42



FP-54



■ COLOR TV BLOCK DIAGRAM



Note The gray blocks incorporate ICs Regarding selection of ICs, refer to the function table.

■ AFT AND PIF

Type No.	Outline	Electrical Performance						Recommended Application		Remarks
		AFT	PIF Amp.	RF AGC	Video Det.	Supply Voltage (V)	Other	Color	B/W	
HA11215A	DP-24	●	●	● Forward	●	12	with Video Amp.	●		direct coupled SAW filter
HA11221	DP-16	—	●	● Reverse	● Quasi Sync. Det.	11	with Sync. Sept.		●	
HA11238	DP-22	●	●	● Forward	● Quasi Sync. Det.	12	with Video Amp.	●		direct coupled SAW filter
HA11440	DP-16	●	●	● Reverse	● Quasi Sync. Det.	12	with Video Amp.	●		direct coupled SAW filter

■ COLOR AND VIDEO SIGNAL PROCESSING

Type No.	Outline	Electrical Performance					Recommended Application		Remarks
		Color Amp.	Color Sync.	Color Demod.	Video Amp.	Supply Voltage (V)	Color	B/W	
HA11401	DP-16	—	—	—	● Tint, Brightness	12	●		Sync. Sept., Pedestal Clamp, Blanking
HA11412A	DP-28	●	●	●	● Brightness Control	12	●		Tint DC Control
HA11431	DP-28	●	●	●	● Brightness Control	12	●		Tint DC Control, Blanking Circuit
HA11436	DP-28	●	●	●	● Brightness Control	12	●		with Auto. Flesh Control

■ SYNCHRONOUS SIGNAL PROCESSING AND DEFLECTION

Type No.	Outline	Electrical Performance							Recommended Application		Remarks
		Sync. Sept.	Horiz. Osc.	Horiz. Drive.	Vert. Osc.	Vert. Drive	Vert. Out.	Supply Voltage (V)	Color	B/W	
HA11244	DP-16	—	●	●	●	●	—	12	●	●	with X-ray protection
HA11409	DP-16	—	—	—	—	—	—	12	●	●	VIR use
HA11423	DP-16-2	●	●	—	●	—	—	12	●		with X-ray protection and blanking circuit
HA1385	DP-5T	—	—	—	—	—	●	110	●		dual power supply

■ SOUND SIGNAL PROCESSING

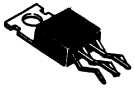
Type No.	Outline	Electrical Performance					Recommended Application		Remarks
		SIF Amp.	Discrim.	AF Amp.	Power Amp.	Supply Voltage (V)	Color	B/W	
HA11229	DP-14	●	● Sync. Det.	●	—	5.5	—	●	Low voltage operation (3 to 8V)
TDA1035S	QP-12T	●	●	●	●	24	●	●	DC volume control, Input/Output for VCR

■ OTHER FUNCTION

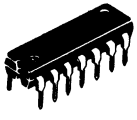
Type No.	Outline	Function	Recommended Application
HZT33	D-35	High stabilized zener IC of 33V	Preset voltage supply for electronic tuning

■ OUTLINE

DP-5T

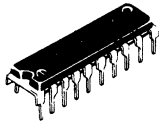


DP-14

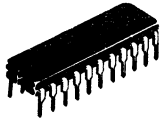


DP-16

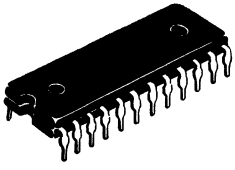
DP-16-2



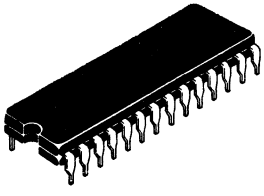
DP-22



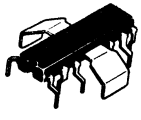
DP-24



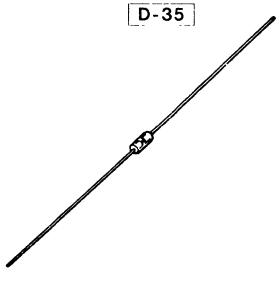
DP-28



QP-12T



D-35



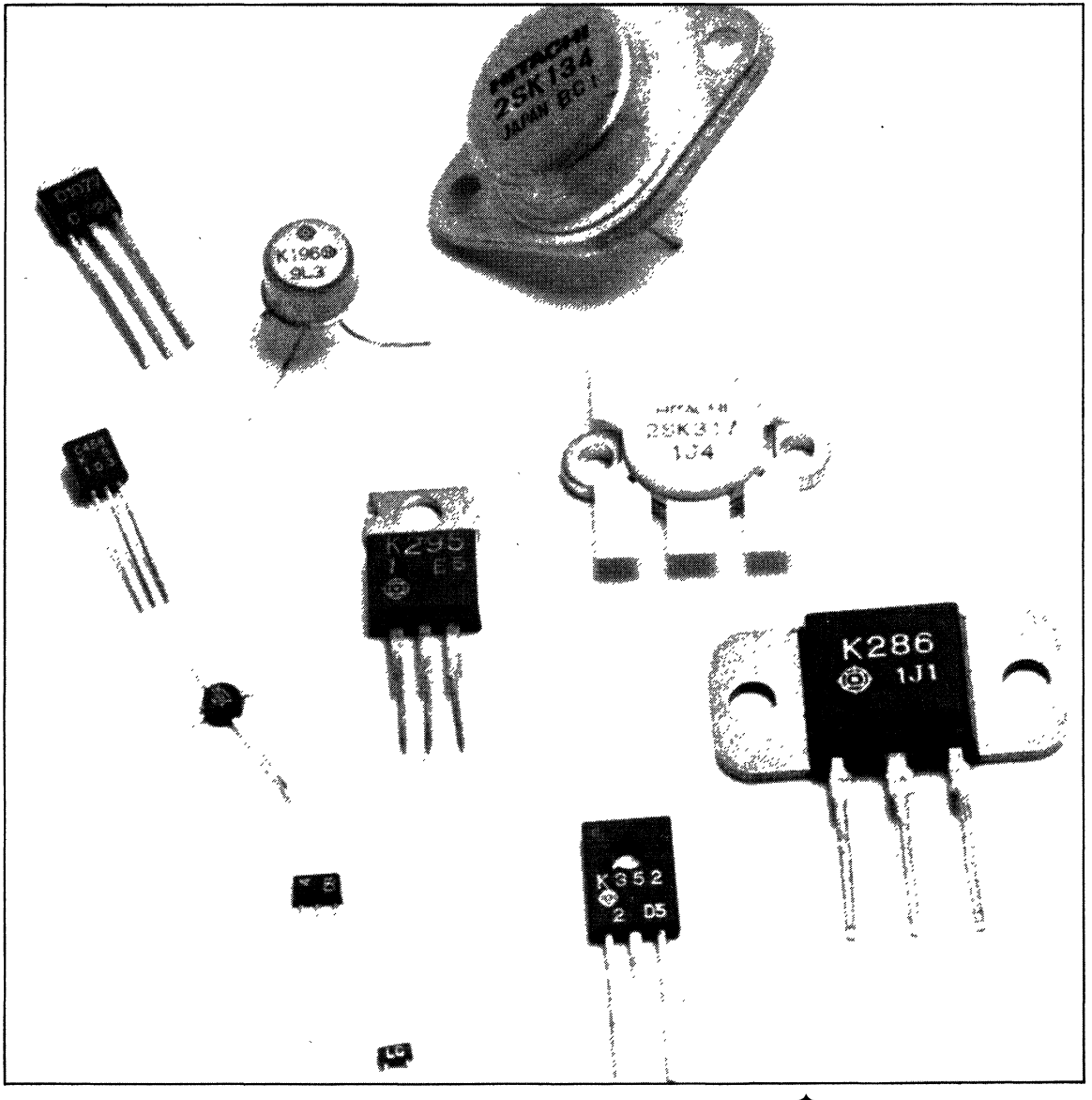
INDUSTRIAL LINEAR CIRCUITS

■ LINEAR ICs

Functions			HITACHI Type No.	Package Code					Cross-reference
				M	P	PS	G	GS	
Operational Amplifiers	General Purpose		HA17741			DP-8		DG-8	Fairchild μA741C
	High Speed		HA17715	T-100					Fairchild μA715C
	Dual		HA17458			DP-8		DG-8	NS LM1458
			HA17747		DP-14		DG-14		Fairchild μA747C
			HA17904			DP-8		DG-8	NS LM2904
	Quad.		HA17301		DP-14		DG-14		Motorola MC3301
			HA17902		DP-14		DG-14		NS LM2902
Voltage Comparators	Single		HA1813			DP-8			
	Universal		HA1812			DP-8		DG-8	
	Dual		HA17903			DP-8		DG-8	NS LM2903
			HA1807				DG-14		
	Quad.		HA17901		DP-14		DG-14		NS LM2901
Voltage Regulators	Variable	2~37V, 150mA	HA17723				DG-14		Fairchild μA723C
	Fixed	5V, 1A	HA17805		T-220AB				Fairchild μA7805C
		6V, 1A	HA17806		T-220AB				Fairchild μA7806C
		7V, 1A	HA17807		T-220AB				
		8V, 1A	HA17808		T-220AB				Fairchild μA7808C
		12V, 1A	HA17812		T-220AB				Fairchild μA7812C
		15V, 1A	HA17815		T-220AB				Fairchild μA7815C
		18V, 1A	HA17818		T-220AB				Fairchild μA7818C
		24V, 1A	HA17824		T-220AB				Fairchild μA7824C
		5V, 0.5A	HA178M05		T-220AB				Fairchild μA78M05C
		6V, 0.5A	HA178M06		T-220AB				Fairchild μA78M06C
		7V, 0.5A	HA178M07		T-220AB				
		8V, 0.5A	HA178M08		T-220AB				Fairchild μA78M08C
		12V, 0.5A	HA178M12		T-220AB				Fairchild μA78M12C
		15V, 0.5A	HA178M15		T-220AB				Fairchild μA78M15C
		18V, 0.5A	HA178M18		T-220AB				Fairchild μA78M18C
		20V, 0.5A	HA178M20		T-220AB				Fairchild μA78M20C
		24V, 0.5A	HA178M24		T-220AB				Fairchild μA78M24C
	Switching Regulator Controller		HA17524		DP-16		DG-16		Silicon General SG3524
A/D, D/A Converters	8-bit Double Integral Type A/D		HA16613		DP-28				
	8-bit D/A		HA17408		DP-16		DG-16		AMD AM1408
Other Functions	Differential Video Amp.		HA17733	T-100					Fairchild μA733C
	5 Transistor Arrays		HA1127				DG-14		RCA CA3045
	Precision Timers		HA17555			DP-8		DG-8	Signetics NE555
	Monostable Multivibrators		HA1607			DP-8			
	Micromotor Speed Controller		HA16503		DP-14				
	Light-measurement Amp. for Camera		HA16506		DP-14				
			HA16564		DP-14				
	Coin Sensor		HA16603		DP-16				
	Electric Leakage Breaker		HA16604		SP-8				
	Burner Controller		HA16605W		DP-20				

SECTION 6

DISCRETES



HITACHI

HITACHI POWER MOS FETs

INTRODUCTION

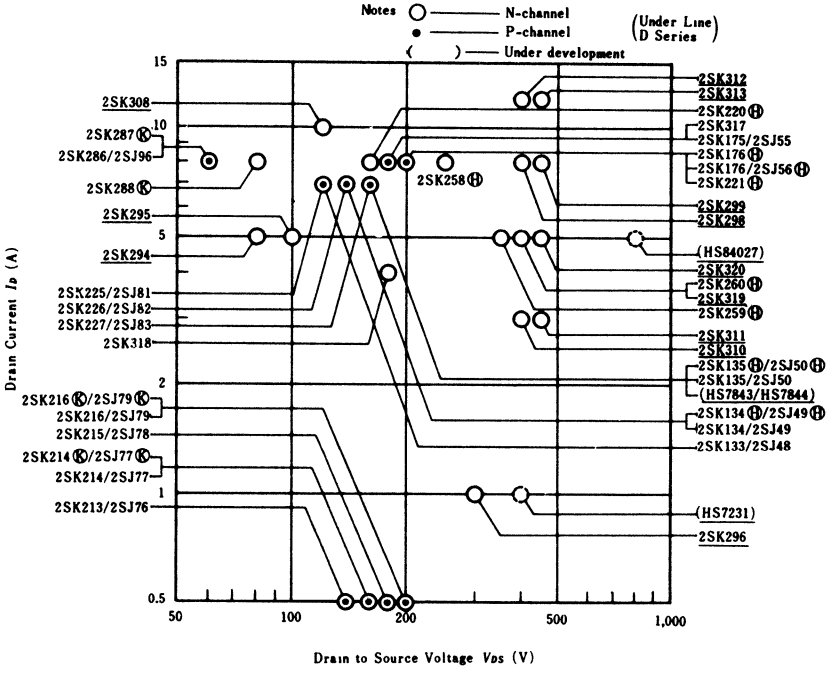
In 1977, HITACHI was the first in the world to develop and mass-produce 100 Watt Complementary Power MOS FETs. Since then, Power MOS FETs have been used in a variety of fields as an ideal power device with high switching speed and high resistance to electrically induced failure. HITACHI Power MOS FET technology has consistently advanced in the areas of on-resistance, voltage and current handling capability and packaging.

There are two basic Power MOS FET structures: Vertical Type and Lateral Type. The advantages of Vertical Types are: a) Drain Case and b) low on-resistance and low loss. Advantages of Lateral Types are: a) Source Case, b) high resistance to electrical destruction, and c) high frequency response. HITACHI has both types to meet various requirements. The Vertical Types are called "D Series," and the Lateral Types are called "S Series."

POWER MOS FET FEATURES:

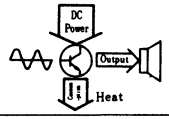
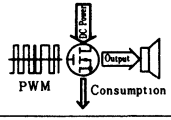
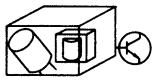
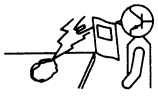
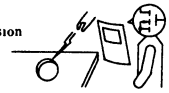
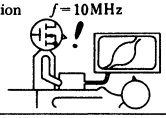
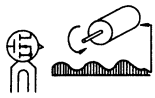
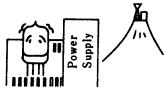
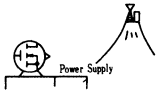
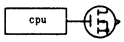
A. Excellent frequency response and high switching speed. (No carrier storage effects.)
B. High resistance to electrical destruction. (No current concentration effects.)
C. Easy parallel connection for higher power applications.
D. Minimum drive power. (Voltage controlled device.)

Power MOS FETs show extreme advantages, not only in new fields where conventional power devices are inadequate, but also in existing fields where conventional devices are already in use.



HITACHI POWER MOS FETs

■Wide Variations of Power MOS FETs

Applications	Function	Features		Type No.
		Bipolar Transistor	Power MOS FET	
Audio Out.	(1) Linear Power Amplifier (2) PWM Power Amp.			2SK213～216 2SJ76～79 2SK286/2SJ96 2SK133～135 2SJ48～50 2SK225～227 2SJ81～83 2SK175～176 2SJ55～56 (HS7843/7844)
High-speed Power Switching	(1) Switching Regulator (2) DC-DC Converter (3) DC-AC Inverter (4) Arcing Machine	f=20～50kHz 	f=100～1000kHz Small Size, Light Weight 	2SK221Ⓗ 2SK258Ⓗ 2SK260Ⓗ 2SK176, 2SJ56 2SK298, 299 2SK312, 313 (HS84027) (HS7231)
		f=1～20kHz 	f=500kHz High Precision 	
Ultrasonic Applications	(1) Medical Diagnosis (2) Sonar (3) Heating, Washing	f=2～3MHz 	High Resolution f=10MHz 	2SK296 2SK294 2SK216
Motor Control	(1) Motor Drive		Smooth Cycling 	2SK176 2SK298～299 2SK312～313 2SK308
Communi-cation System	(1) MW, SW Transmitter (2) HF, VHF Transmitter		Small Size Lower Power 	2SK221Ⓗ 2SK258Ⓗ 2SK260Ⓗ 2SK176, 2SJ56 2SK298, 299 2SK317, 2SK318
Other	(1) IC Interface (2) Analog Switch (3) Character Display		High Speed Low Driving Power 	2SK216, 2SK294 2SK288, 2SK296 2SK134, 2SK176 2SK308

( ) : Under development

MAIN CHARACTERISTICS OF HITACHI POWER MOS FETs

• **D Series**

Type No.		Maximum Ratings				Electrical Characteristics					Outline
N-ch	P-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}** (W)	$R_{ON}(\Omega)$ typ	$R_{ON}(\Omega)$ max	t_{on} (ns)	t_{off} (ns)	f_c (MHz)	
2SK347	—	400	±20	1	19	4.5	9.0	—	—	—	T-24L
2SK352	—	250	±9	0.3	8	30	50	—	—	250	T-126
2SK345	2SJ101	40	±20	5	30	0.3	0.4	40	70	—	T-220AB
2SK346	2SJ102	60									
2SK294	—	80				0.4	0.56	40	70	5	
2SK295	—	100									
2SK296	—	300		1		2.5	4.0	20	70	10	
2SK310	—	400		3		2.5	4.0	25	70	10	
2SK311	—	450									
2SK319	—	400		5	50	1.1	1.83	50	120	5	
2SK320	—	450									
2SK343	2SJ99	140	±20	8	100	0.3	0.5	100	90	2	T-22
2SK344	2SJ100	160									
2SK308	—	120	±20	10	100	0.2	0.3	60	160	4	T-3
(HS84033)	—	250				0.4	—	—	—	—	
2SK298	—	400		8		1.1	1.75	50	120	5	
2SK299	—	450									
2SK312	—	400		12	125	0.67	0.9	70	200	3	
2SK313	—	450									
2SK351	—	800		5		1.67	3.0	100	300	2	

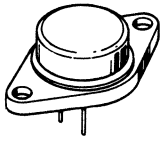
• **S Series**

Type No.		Maximum Ratings				Electrical Characteristics					Outline
N-ch	P-ch	V_{DSS} (V)	V_{GSS} (V)	I_D (A)	P_{ch}** (W)	R_{on} (Ω) typ	R_{on} (Ω) max	t_{on} (ns)	t_{off} (ns)	f_t (MHz)	
2SK213	2SJ76	*140	±15	0.5	30	8/10	—	20	30	40/30	T-220AB
2SK214	2SJ77	*160									
2SK214Ⓚ	2SJ77Ⓚ	160									
2SK215	2SJ78	*180									
2SK216	2SJ79	*200									
2SK216Ⓚ	2SJ79Ⓚ	200									
2SK286	2SJ96	* 60	±20	8	100	0.5	0.8	80/100	110/250	3/2	T-22
2SK287Ⓚ	—	60				0.5	0.6	25	350	2	
2SK288Ⓚ	—	80									
2SK225	2SJ81	*120	±15	7		1.0	1.7	180/230	60/110	3/2	
2SK226	2SJ82	*140									
2SK227	2SJ83	*160									
2SK133	2SJ48	*120	±14	7	100	1.0	1.7	180/230	60/110	3/2	T-3
2SK134	2SJ49	*140									
2SK134Ⓗ	2SJ49Ⓗ							90/150	110/210		
2SK135	2SJ50	*160						180/230	110/110		
2SK135Ⓗ	2SJ50Ⓗ							90/150	110/210		
2SK175	2SJ55	*180	±20	8	125	1.0	1.7	270/330	90/120	2/1	
2SK176	2SJ56	*200									
2SK176Ⓗ	2SJ56Ⓗ	200						60	200		
2SK220Ⓗ	—	160	±20	8	100	1.0	1.5	25	45	50	
2SK221Ⓗ	—	200		8	125	0.8	1.1	25	140	7	
2SK258Ⓗ	—	250									
2SK259Ⓗ	—	350		5	125	2.5	3.0	25	140	7	
2SK260Ⓗ	—	400									
2SK317	—	180	±20	8	120	0.95	1.25	—	—	300	T-40
2SK318	—			4	70	1.9	2.5				

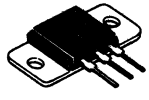
* ; V_{DSX} ** T_c=25℃

■OUTLINE

T-3
EIAJ; TC-3, TB-3
JEDEC, TO-3



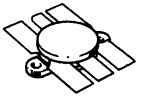
T-22
HPAK



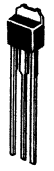
T-126
JEDEC; TO-126mod

T-220AB
EJAJ; SC-46
JEDEC; TO-220AB

T-40
RFPAK



T-24L
DPAK



HITACHI LASER DIODES

HITACHI
HLN501
LITERATURE NO.

■ FEATURES

- Wide Selection of Wavelength for Various Applications, Visible, Infrared and Long wavelength.
- Continuous or Pulsed Operation up to 50°C.
- Various Types of Package.
- Low Operating Current.
- Fully Stabilized Fundamental Mode.

■ CHARACTERISTICS OF LASER DIODES

• Absolute Maximum Ratings

Package Outline	Type No.	Allowable Output Power P_o* (mW)	Reverse Voltage V_R (V)	Operating Temp. T_{opr} (°C)	Storage Temp. T_{stg} (°C)
Open-Air Type	HLP1400	15	2	0 ~ +50	0 ~ +60
	HLP2400	3			
	HLP3400	10			
	HLP5400	5			
Hermetic Seal Type	HL780IE, HL780IG	5		0 ~ +50	−40 ~ +60
	HLP1600, HLP1700	15			
	HLP2600, HLP2700	3			
	HLP3600, HLP3700	10			
	HLP5600, HLP5700	5			
Fiber Pigtail Type	HLP1500	6			
	HLP2500	1.5			
	HLP3500	3			
	HLP5500	1.2			

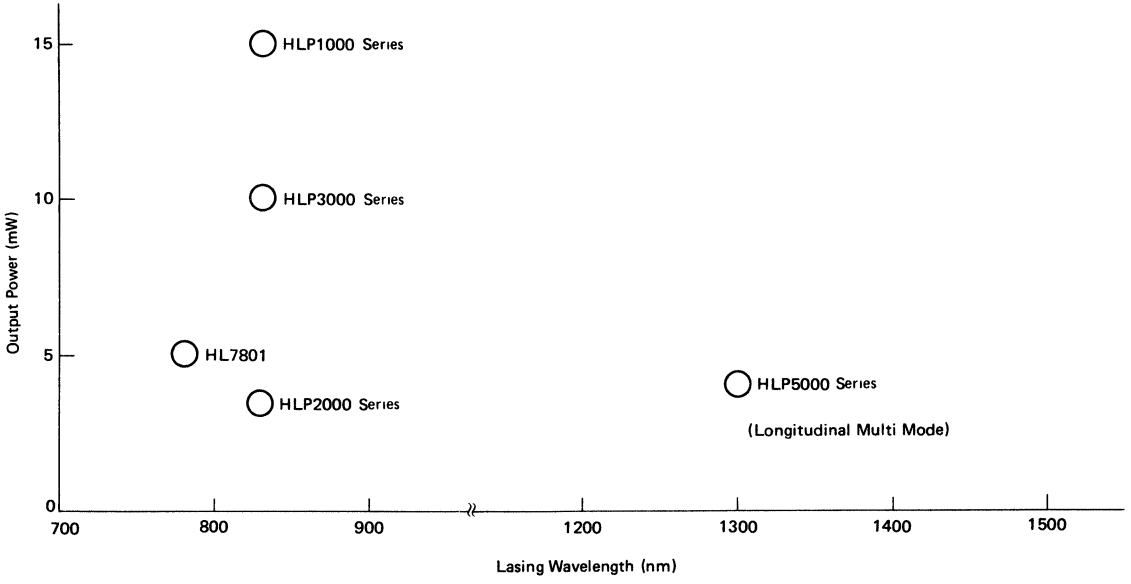
* Free of kink below this value

• Optical and Electrical Characteristics

Package Outline	Type No.	Peak Wavelength λ_p (nm)			Beam Divergence $\theta_{//} \times \theta_{\perp}$* (deg)	Test Condition P_o (mW)	Threshold Current Ith (mA)	Output Power P_o (mW)		Monitor Power P_m (mW)	Test Condition I_F (mA)
		min	typ	max	typ		typ	min	typ	min	
Open-Air Type	HLP1400	800	830	850	12 × 26	10	70	4	5	2	Ith + 25
	HLP2400				25 × 35	2	20	1	1.5	0.5	Ith + 5
	HLP3400				25 × 35	6	35	4	6	1.0	Ith + 15
	HLP5400	–	1300	–	30 × 40	3	50	1.5	3	–	Ith + 20
Hermetic Seal Type	HL780IE, HL780IG	760	780	800	15 × 27	3	60	–	3	(0.1mA)**	Ith + 15
	HLP1600, HLP1700	800	830	850	12 × 26	10	70	4	5	0.2	Ith + 25
	HLP2600, HLP2700				25 × 35	2	20	1	1.5	0.05	Ith + 5
	HLP3600, HLP3700				25 × 35	6	35	4	6	0.1	Ith + 15
	HLP5600, HLP5700	–	1300	–	30 × 40	3	50	1.5	3	–	Ith + 20
Fiber Pigtail Type	HLP1500	800	830	850	–	4	70	2	3	0.5	Ith + 25
	HLP2500				–	1.0	20	0.5	0.8	0.1	Ith + 5
	HLP3500				–	2	35	1.5	2	0.3	Ith + 15
	HLP5500	–	1300	–	–	0.5	50	0.4	0.7	0.05	Ith + 20

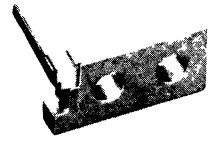
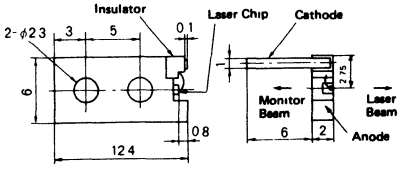
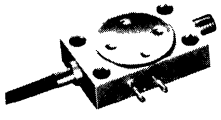
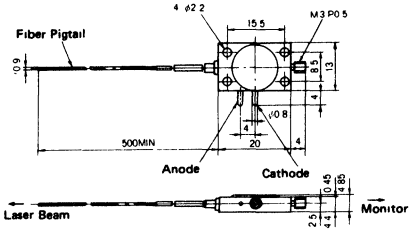
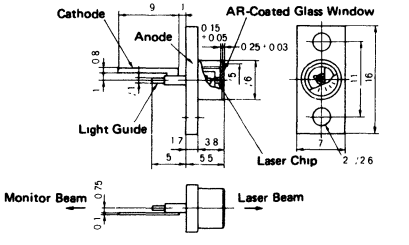
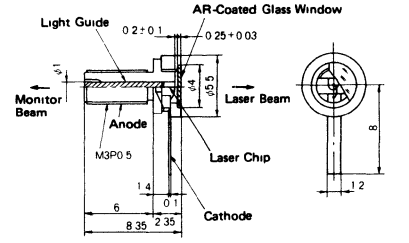
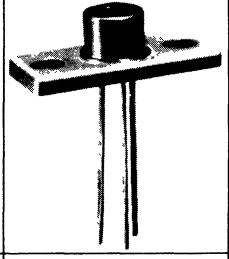
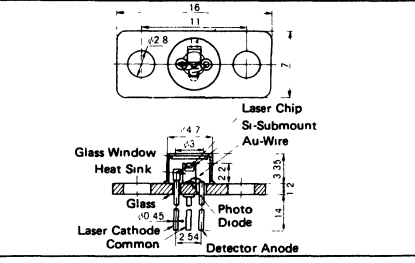
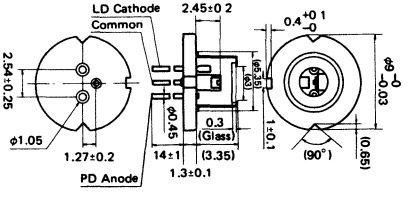
* The beam divergence is the full beam width at half maximum points, parallel and perpendicular to the junction plane.
** The monitor output current is defined as the short current of the photo diode which is included in the package.

- **Map of Wavelength vs. Output Power**



■ PACKAGE

Five types of packages are currently available.
Especially the type 500 is a hermetically sealed package.

Package	Outline	Dimensional Outline (unit in mm)	Feature
400 type			The laser is mounted on an uncapped stem, facilitating close access to the chip. Moreover, the stray capacitance for the lead terminal can be minimalized. Therefore it is convenient for experimental use.
500 type			The device is provided with a fiber pigtail and monitor output-guide, and is hermetically sealed. <Standard Fiber> Numerical Aperture : 0.2 Core Diameter : 50 μm Outer Diameter : 125 μm Jacket Diameter : 900 μm Refractive Index : GI Length of Pigtail : 50 cm
600 type			The type 600 and 700 are general purpose packages with AR-Coated glass window. They are also provided with a monitor output guide.
700 type			
E type			The type E is provided with a photo detector for power stabilization and so on. It results in the simplified automatic power control circuit (APC).
G type			The type G is provided with a photo detector for power stabilization and so on. It results in the simplified automatic power control circuit (APC).

HITACHI INFRARED EMITTING DIODES

HITACHI
HLN401
LITERATURE NO.

■ FEATURES

- High Power Output ····· 10 ~ 60 mW
- Wide Selection of Wavelength ····· 735 ~ 905 nm
  By changing the mixed crystal ratio "x" of material $Ga_{1-x}Al_xAs$,
  the peak wavelength can be selected within the range of 735 ~ 905 nm.
- Excellent Monochromacy ····· Spectral Width 30 nm.
- Excellent Frequency Response ····· Rise and Fall Time 12 ns.

■ SELECTION GUIDE

Series (Type No.)	Package	Feature	λ_p typ (nm)	Optical Output Power P_O (typ)							
				10 mW	15 mW	20 mW	25 mW	30 mW	40 mW	50 mW	60 mW
HLP Series	 T-type	Open-Air type Close access to optics	760			HLP20TA		HLP30TA	HLP40TA		
			800					HLP30TB	HLP40TB	HLP50TB	HLP60TB
			840					HLP30TC	HLP40TC	HLP50TC	HLP60TC
			880					HLP30TD	HLP40TD	HLP50TD	HLP60TD
	 R-type	Open-Air type Close access to optics	760			HLP20RA		HLP30RA	HLP40RA		
			800					HLP30RB	HLP40RB	HLP50RB	HLP60RB
			840					HLP30RC	HLP40RC	HLP50RC	HLP60RC
			880					HLP30RD	HLP40RD	HLP50RD	HLP60RD
	 RG-type	Hermetic Seal type Easy to handle	760	HLP20RGA	HLP30RGA	HLP40RGA					
			800		HLP30RGB	HLP40RGB	HLP50RGB	HLP60RGB			
			840		HLP30RGC	HLP40RGC	HLP50RGC	HLP60RGC			
			880		HLP30RGD	HLP40RGD	HLP50RGD	HLP60RGD			
	 RL-type	Hermetic Seal type Easy to handle sharp directional	760	HLP20RLA	HLP30RLA	HLP40RLA					
			800		HLP30RLB	HLP40RLB	HLP50RLB	HLP60RLB			
			840		HLP30RLC	HLP40RLC	HLP50RLC	HLP60RLC			
			880		HLP30RLD	HLP40RLD	HLP50RLD	HLP60RLD			
HLP-W Series	 T-type	Sharp directional	760			HLP20WTA		HLP30WTA	HLP40WTA		
			800					HLP30WTB	HLP40WTB	HLP50WTB	HLP60WTB
			840					HLP30WTC	HLP40WTC	HLP50WTC	HLP60WTC
			880					HLP30WTD	HLP40WTD	HLP50WTD	HLP60WTD
	 R-type	Sharp directional	760			HLP20WRA		HLP30WRA	HLP40WRA		
			800					HLP30WRB	HLP40WRB	HLP50WRB	HLP60WRB
			840					HLP30WRC	HLP40WRC	HLP50WRC	HLP60WRC
			880					HLP30WRD	HLP40WRD	HLP60WRD	HLP60WRD
	 RG-type	Hermetic Seal type Easy to handle	760	HLP20WRGA	HLP30WRGA	HLP40WRGA					
			800		HLP30WRGB	HLP40WRGB	HLP50WRGB	HLP60WRGB			
			840		HLP30WRGC	HLP40WRGC	HLP50WRGC	HLP60WRGC			
			880		HLP30WRGD	HLP40WRGD	HLP50WRGD	HLP60WRGD			
(HE-8401F)	 F-type	With Fiber	790 ~ 890	200 μW							

■ CHARACTERISTICS OF INFRARED EMITTING DIODES

● Absolute Maximum Ratings

Item	Symbol	Open-Air Type T, R-type	Hermetic Seal Type RG, RL-type	Fiber Pigtail Type F-type	Unit
Forward Current	I_F	250 (230*)	250(230*)	150	mA
Reverse Current	V_R	3	3	3	V
Power Dissipation	P_d	600	600	–	mW
Operating Temp.	T_{opr}	−20 ~ +40**	−20 ~ +60	−10 ~ +60	°C
Storage Temp.	T_{stg}	−40 ~ +60**	−40 ~ +80	−20 ~ +70	°C

* Value at λ_p = 760 nm ** Storage and operating conditions must be taken under humidity of lower than 40%.

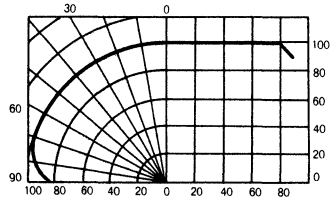
● Optical and Electrical Characteristics

Item	Symbol	Test Condition	T, R, RG, RL-type			F-type			Unit
			min	typ	max	min	typ	max	
Output Power	P_o	I_F = 100 mA	–	–	–	100	200	–	μW
		I_F = 200 mA	Refer to selection guide			–	–	–	mW
Peak Wavelength	λp	I_F = 100 mA	–	–	–	790	840	890	nm
		I_F = 200 mA	Refer to selection guide			–	–	–	
Spectral Width	Δλ	I_F = 100 mA	–	–	–	–	30	40	nm
		I_F = 200 mA	–	30	35	–	–	--	
Forward Voltage	V_F	I_F = 100 mA	–	–	–	–	1.8	2.5	V
		I_F = 200 mA	–	1.7(2.3*)	2.3(2.6*)	–	–	–	
Reverse Current	I_R	V_R = 3V	–	–	30	–	--	10	μA
Capacitance	C_j	V_R = 0, f = 1MHz	–	30	--	–	30	–	pF
Rise and Fall Time	t_r, t_f		–	12(20*)	–	–	12	–	ns
Cut-Off Frequency	f_C	I bias = 100mA, 30% mod, -3dB	–	30	–	–	30	–	MHz

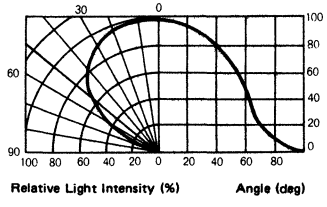
* Value at λ_p = 760 nm

● Radiation Patterns

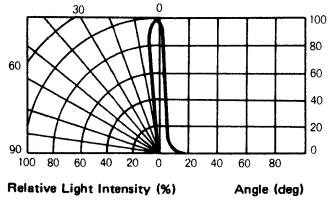
HLP Series (T, R-type)



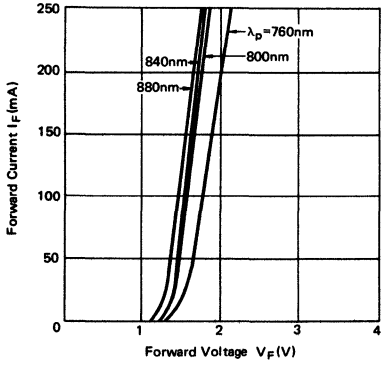
HLP Series (RG-type)
HLP-W Series



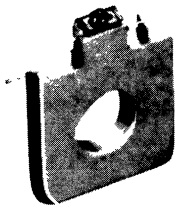
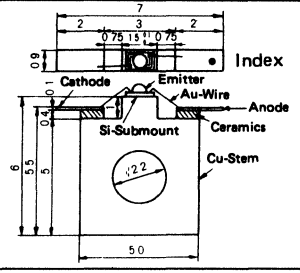
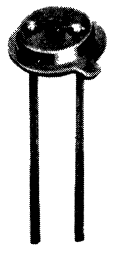
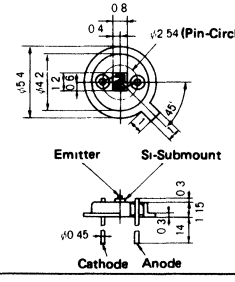
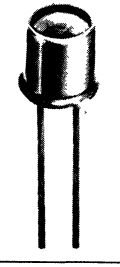
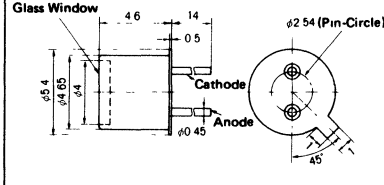
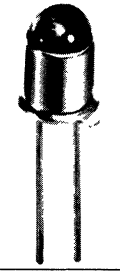
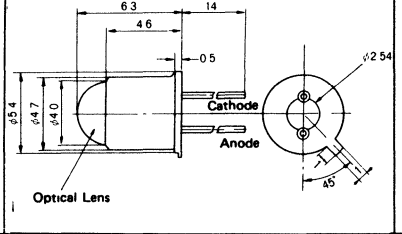
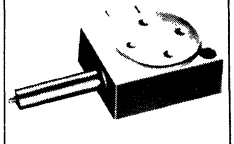
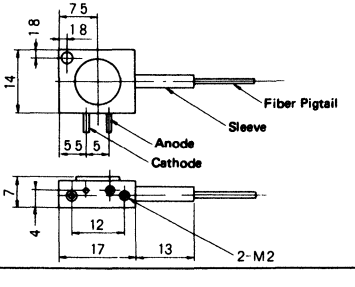
HLP Series (RL-type)



● Forward Characteristics (HLP, HLP-W Series)



■ PACKAGE

Package		Outline	Dimensional Outline (unit in mm)	Feature
Open-Air Type	T-type			A chip is mounted on a flat metal stem, designed to be conveniently used as a diode array. This type is suitable for multi-assembling with high density.
	R-type			The R type is capable of close accessing to the optics.
Hermetically Seal Type	RG-type			The RG type is hermetically sealed using a flat glass, highly reliable.
	RL-type			The RL type is hermetically sealed using a optical lens and has the characteristics of sharp directional beam divergence. The focal length is about 7 mm.
Fiber Pigtail Type	F-type			The F type is provided with a fiber pigtail and suitable for fiber communication. <Standard Fiber> Numerical Aperture : 0.2 Core Diameter : 85 μm Clad Diameter : 125 μm Refractive Index : SI Length of pigtail : 50 cm

SECTION 7

POWER THYRISTORS

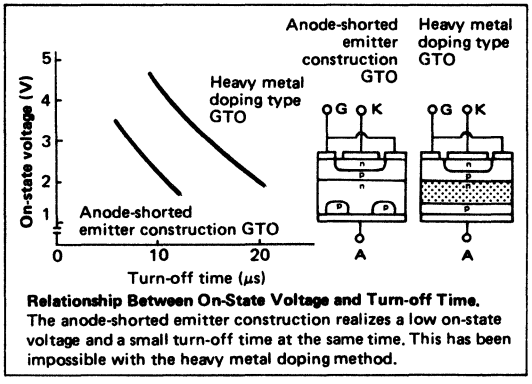
HITACHI

HITACHI GATE TURN-OFF THYRISTOR (GTO)

GTO thyristors permit main current to be turned on or off by plus or minus gate pulse current. Therefore, they do away with commutation circuits and permit high frequency operation, thus making it possible to miniaturize the size of inverters and choppers and increase their performance.

The Hitachi GTO Thyristor adopts an anode shorted emitter construction. This feature simultaneously allows low on-state voltage and high speed. Besides, its stable high temperature characteristics make Hitachi GTO Thyristors ideal for many applications.

The Hitachi GTO Thyristors are available in wide series to meet the customer needs for AC 230 V and 460 V line applications.



Relationship Between On-State Voltage and Turn-off Time. The anode-shorted emitter construction realizes a low on-state voltage and a small turn-off time at the same time. This has been impossible with the heavy metal doping method.

Main Applications

AVAF Inverter	Variable speed control of electric motors for fan, compressor and pump drive.
CVCF Inverter	AC Power supplies for computers, instrumentation, communication equipment, etc.
Chopper	NC machine tools, electric automobiles, forklifts and electro-driven vehicles.
High-frequency power supplies	Induction heating and welding machines.
Electrical home appliances	Induction-heated cooking devices and control of various appliance drive motors.

Hitachi GTO Series

Items \ Type	GFT 20A6	GFT 50A6	GFF 90A6	GFP 450A8	GFT 20B12	GFT 50B12	GFF 90B12	GFF 200E12	GFF 300B12	GFP 600C16	GFP 100B25
Repetitive Peak Off-state Voltage (V_{DRXM})	600 V	600 V	600 V	800 V	1,200 V	1,200 V	1,200 V	1,200 V	1,200 V	1,600 V	2,500 V
Repetitive Controllable On-state Current (I_{TCM})	20 A	50 A	90 A	450 A	20 A	50 A	90 A	200 A	300 A	600 A	1,000 A
Peak On-state Voltage (V_{TM})	2.4 V	2.5 V	2.3 V	2.0 V	3.0 V	3.1 V	2.8 V	3.8 V	3.2 V	2.5 V	2.5 V
Gate Turn-on Time (tgt) (Typical)	2 μs	2 μs	2 μs	3 μs	3 μs	3 μs	3 μs	3 μs	4 μs	5 μs	5 μs
Gate Turn-off Time (tgq) (Typical)	4.5 μs	4.5 μs	4.5 μs	5 μs	4.5 μs	4.5 μs	4.5 μs	4.5 μs	10 μs	11 μs	21 μs
Package	TO-66	TO-3	TO-3 Flat Base	Press Pack	TO-66	TO-3	TO-3 Flat Base	Flat Base	Flat Base	Press Pack	Press Pack

Specifications are subject to change without notice.

TRIACS

(ISOLATED TO-3 FLAT BASE)

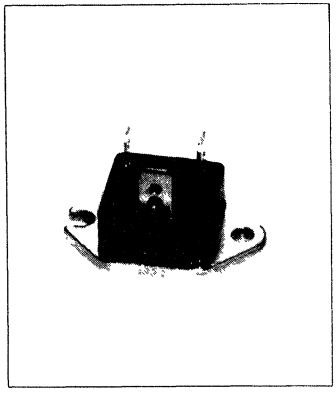
FEATURES:

- Electrically isolated TO-3 flat base package and FASTON terminals.
- High surge current capability.
- Low on-state voltage.
- 1500 or 2000V (RMS) isolation voltage (1 minute).
- Selected types available for an inductive load operation.

T_J, T_{STG} = −40 ~ +125° C

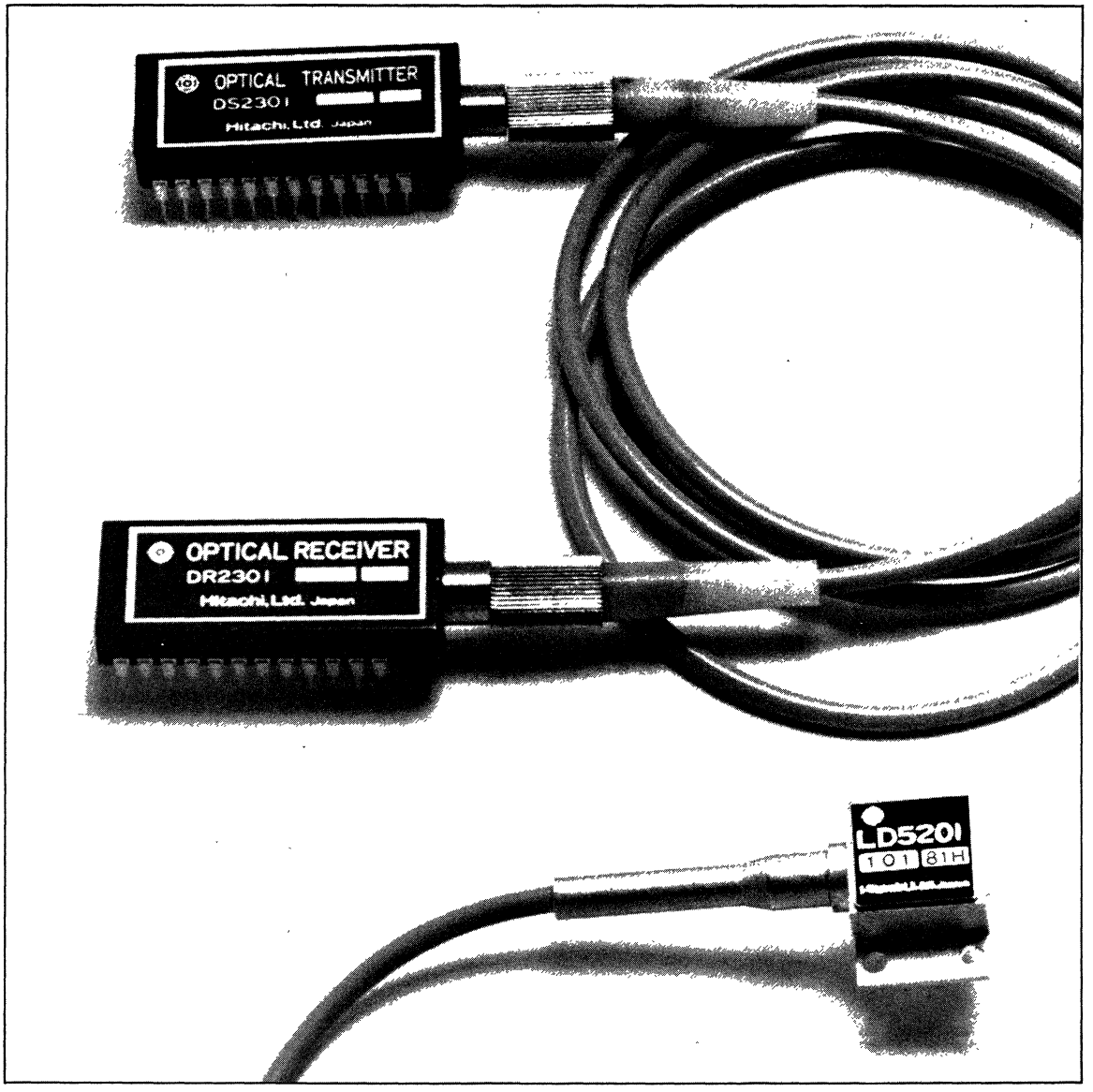
TYPE	V_{DRM} (V)	I_T (RMS) @T_C (A) (C)	I_{TSM} (50Hz) (A)	V_{TM} @I_{TM} (V) (A)	I_{GT}/V_{GT} (mA) (V)	I_{DRM} @V_{DRM} (mA)	di/dt (A/μs)	dv/dt (COMM) (V_{RMS})	V_{ISO}
FSM16C2L	200	16 @76	150	1.5 @23	50/2.5	0.2	20	10	2500
FSM16C4L	400								2500
FSM16C6L	600								2500
FSM20C2L	200	20 @74	180	1.5 @28	50/2.5	0.2	20	10	2500
FSM20C4L	400								2500
FSM20C6L	600								2500
FSM30C2L	200	30 @63	275	1.5 @45	50/2.5	0.2	20	10	2500
FSM30C4L	400								2500
FSM30C6L	600								2500

I_{GT}, V_{GT}: MT2(+)/G(+), MT2 (+)/G(−), MT2(−)/G(−)
Viso: Isolation voltage between a terminal and the flat base.



SECTION 8

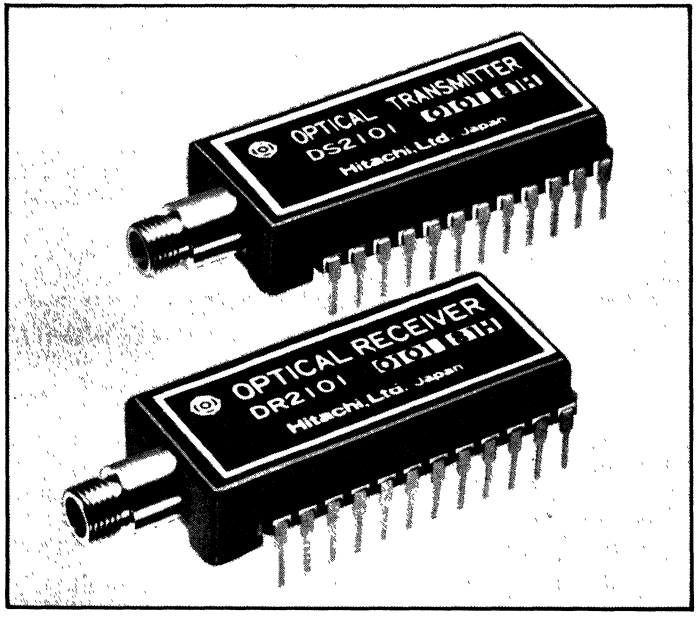
FIBER OPTIC COMMUNICATION DEVICES



HITACHI

FIBER OPTIC DIGITAL MODULES
DS2101, DR2101

—Preliminary—

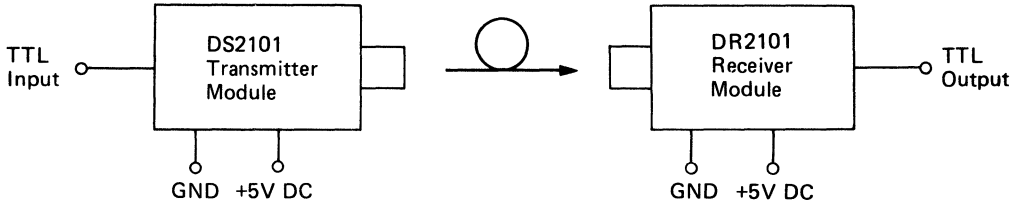


FEATURES

- DC to 2 M bits/sec data rate
- 2 km transmission length
- Operation on single 5V supply
- TTL compatible interface
- Wide dynamic range
- No shielding required
- DIP (Dual Inline Package) pin arrangement
- Couples to wide variety of fibers

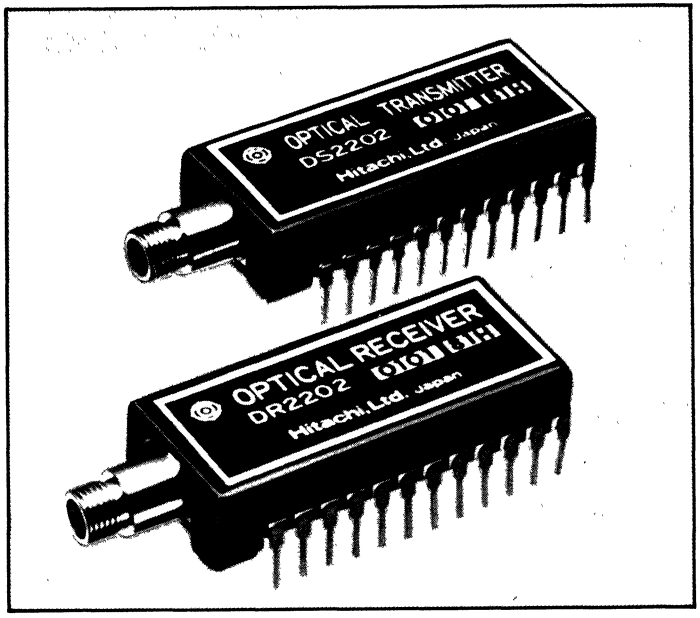
DESCRIPTION

Hitachi DS2101 and DR2101 Fiber Optic Digital Modules are the transmitter and receiver for a high-sensitivity, low-speed TTL Fiber Optic Data Link. The DS 2101 transmitter module operates from a TTL input and launches 300 μW of optical power into a 200 μm, 0.5 N.A. optical fiber. The DR2101 receiver module, optimized for low noise and maximum sensitivity, will operate with only a 0.2 μW optical power input. Input data must be encoded such that its short-term average value is constant and average duty cycle is 50 percent. Both modules have full internal power supply regulation and provide adjustment-free operation over the full operating temperature range. For easy interfacing the modules contain an integrated optical connector providing a plugable interface that couples optical power efficiently to wide variety of optical fibers.



FIBER OPTIC DIGITAL MODULES
DS2202, DR2202

—Preliminary—

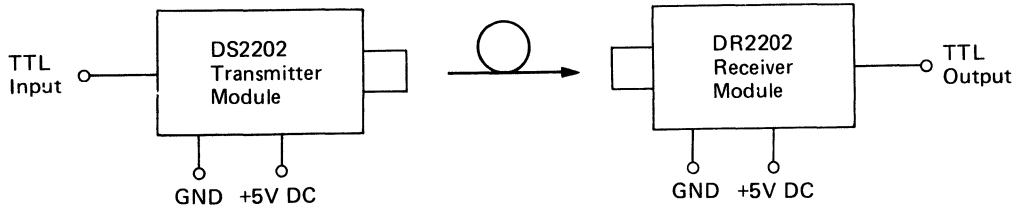


FEATURES

- 0.1 M bits to 10 M bits/sec data rate
- 1 km transmission length
- Operation on single 5V supply
- TTL compatible interface
- Wide dynamic range
- No shielding required
- DIP (Dual Inline Package) pin arrangement
- Couples to wide variety of fibers

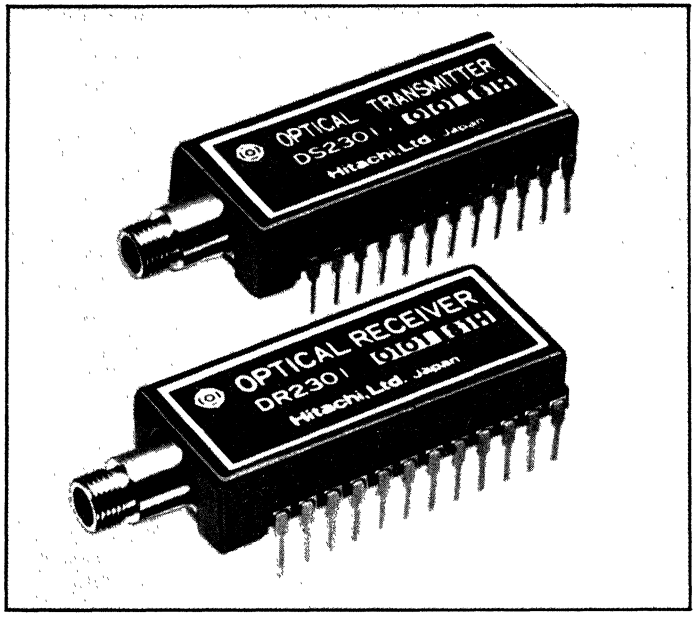
DESCRIPTION

Hitachi DS2202 and DR2202 Fiber Optic Digital Modules are the transmitter and receiver for a high-sensitivity, high-speed TTL Fiber Optic Data Link. The DS2202 transmitter module operates from a TTL input and launches 5 μW of optical power into an 80 μm, 0.2 N.A. optical fiber. The DR2202 receiver module, optimized for low noise and maximum sensitivity, will operate with only a 0.5 μW optical power input. Input data must be encoded such that its short-term average value is constant and average duty cycle is 50 percent. Both modules have full internal power supply regulation and provide adjustment-free operation over the full operating temperature range. For easy interfacing the modules contain an integrated optical connector providing a plugable interface that couples optical power efficiently to wide variety of optical fibers.



FIBER OPTIC DIGITAL MODULES
DS2301, DR2301

—Preliminary—



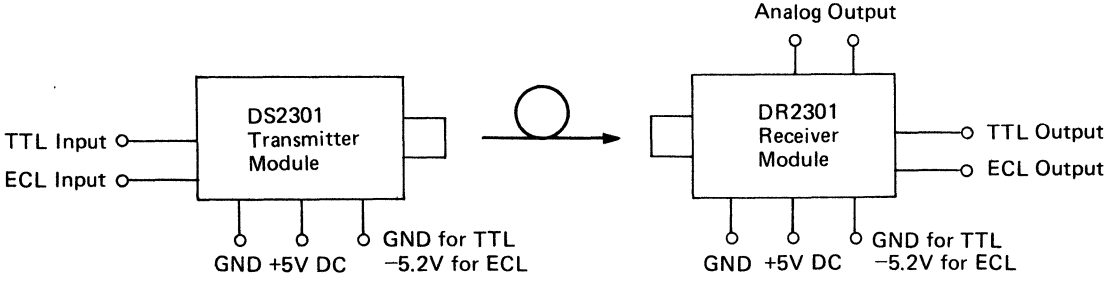
FEATURES

- 0.1 M bits to 32 M bits/sec data rate
- 3 km transmission length
- TTL/ECL compatible interface
- Operation on single 5V supply for TTL (+5V and −5.2V supplies for ECL)
- Wide dynamic range
- No shielding required
- DIP (Dual Inline Package) pin arrangement
- Couples to wide variety of fibers

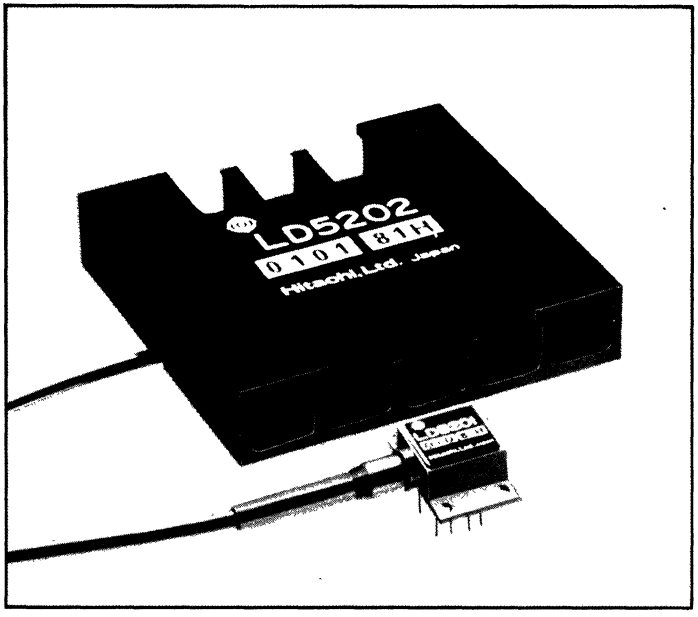
DESCRIPTION

Hitachi DS2301 and DR2301 Fiber Optic Digital Modules are the transmitter and receiver for a high-sensitivity, high-speed TTL or ECL Fiber Optic Data Link. The DS2301 transmitter module operates from a TTL or an ECL input and launches 100 μW of optical power into an 80 μm, 0.2 N.A. optical fiber. The DR2301 receiver module, optimized for low noise and high speed, will operate with only a 0.5 μW optical power input. Input data must be encoded such that its short-term average value is constant and its average duty cycle is 50 percent. Both modules comprise TTL and ECL interfaces which are selectable with TTL input/output terminals and V_{EE} power supply.

For easy interfacing without problems of source or detector/fiber alignment, the modules contain an integrated optical connector providing a plugable interface that couples optical power efficiently to wide variety of optical fibers.



LASER DIODE MODULES
LD2201, LD2202, LD2221, LD5201, LD5202, LD5221



FEATURES

- Suitable for long-distance, high bit rate fiber optic transmissions
- Continuous or pulsed operation up to 60°C
- Fully stabilized fundamental mode TE_{00} oscillation
- Hermetically sealed package
- Fiber pigtail type with monitor diode and thermo-electric cooler

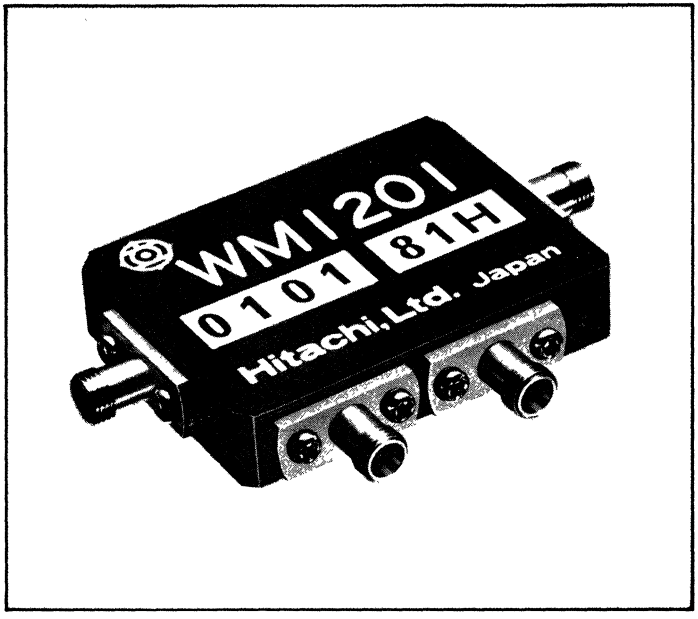
DESCRIPTION

The Hitachi LD2000 and 5000 series are extremely compact, highly efficient, reliable laser sources for optical transmission systems and measuring instruments. LD2000 and 5000 series have a typical peak emission wavelength of 0.83 μm and 1.3 μm, respectively. These modules are unique because they have stable oscillation in a fundamental transverse mode and have hermetically sealed packages with monitor diode and thermo-electric cooler. Under modulated conditions, they can respond to speeds exceeding 1 GHz.

Model No.	Outline
LD2201	Short wavelength Laser Diode Module
LD2202	Short wavelength Laser Diode Module with thermo-electric cooler
LD2221	Short wavelength Laser Diode Module (high stable optical characteristics)
LD5201	Long wavelength Laser Diode Module
LD5202	Long wavelength Laser Diode Module with thermo-electric cooler
LD5221	Long wavelength Laser Diode Module (high stable optical characteristics)

OPTICAL WAVELENGTH MULTIPLEXERS DEMULTIPLEXERS WM1201, WM1210, WM1310

—Preliminary—



FEATURES

- Optical interference filter type used in W.D.M. transmissions
- Small, lightweight, solid construction
- Applicable to various kinds of fiber
- Easy to handle
- Low insertion loss

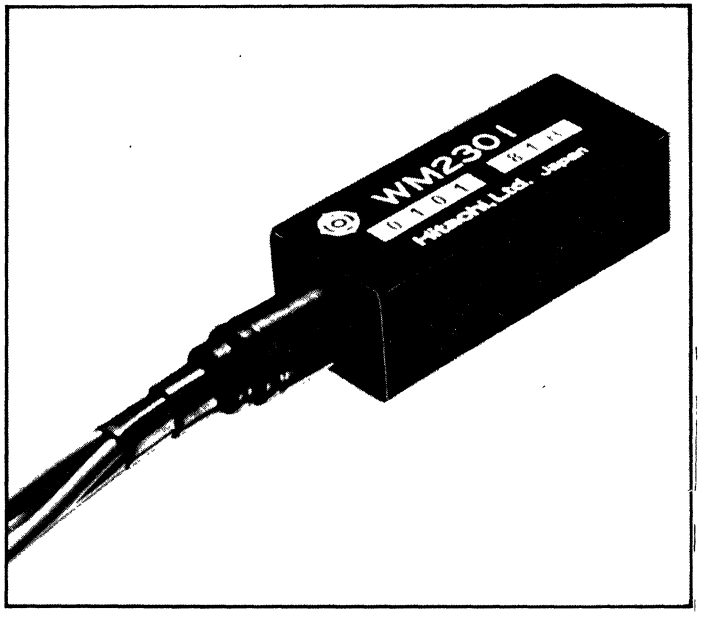
DESCRIPTION

The Hitachi optical wavelength multiplexers/demultiplexers are used for wavelength division multiplexing transmission systems. These devices comprise optical interference filters as wavelength selective components.

Model No.	Outline
WM1201	Two-wavelength Multiplexer/Demultiplexer (short wavelength)
WM1210	Two-wavelength Multiplexer/Demultiplexer (long wavelength)
WM1310	Three-wavelength Multiplexer/Demultiplexer (long wavelength)

OPTICAL WAVELENGTH MULTIPLEXERS DEMULTIPLEXERS WM2201, WM2301

—Preliminary—



FEATURES

- Used in W.D.M. Transmissions
- Simplicity of structure and ease of arrangement since concave grating is used.
- Low loss and sharp cutoff characteristics
- Narrow interchannel wavelength spacing

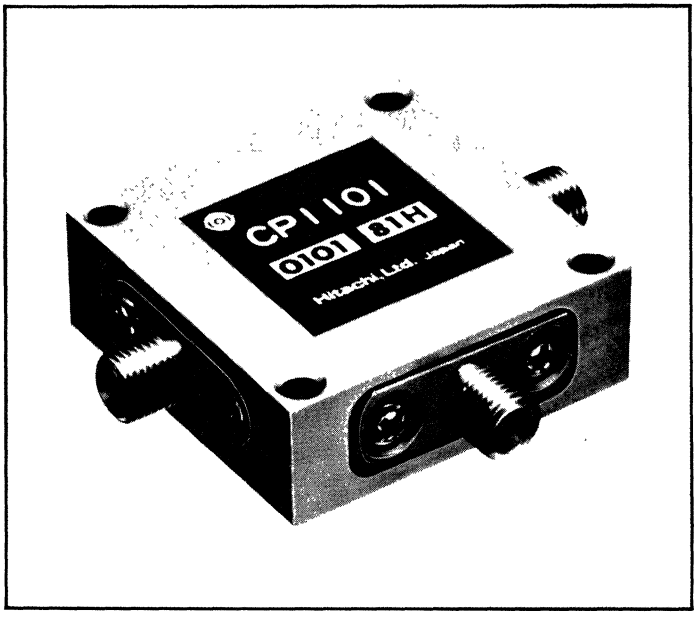
DESCRIPTION

The Hitachi optical wavelength multiplexers/demultiplexers are suited to wavelength division multiplexing transmission systems. These devices comprise concave grating which can separate or combine a number of waves without additional wavelength selective components. Since an aberration-corrected concave grating is used, these devices have low loss and sharp cutoff characteristics.

Model No.	Outline
WM2201	Two-wavelength Multiplexer/Demultiplexer (long wavelength)
WM2301	Three-wavelength Multiplexer/Demultiplexer (long wavelength)

OPTICAL DIRECTIONAL COUPLERS CP1X0X, CP1X1X

—Preliminary—



FEATURES

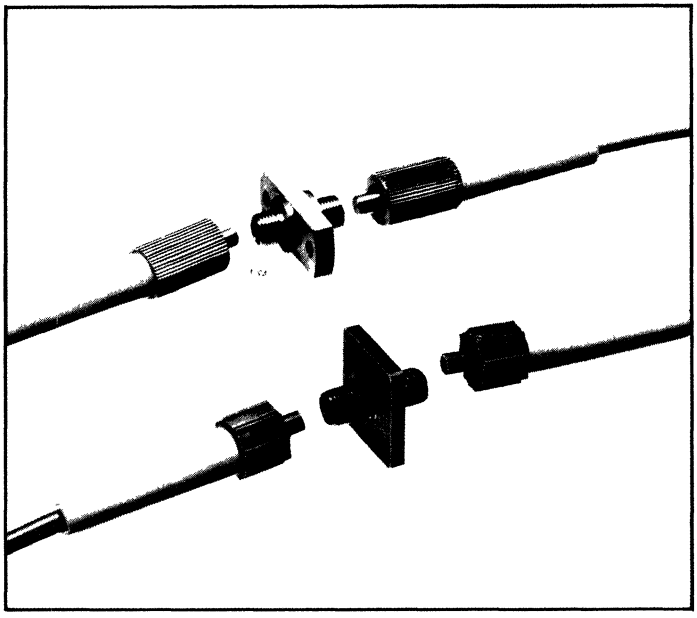
- Small, lightweight, solid construction
- Applicable to various kinds of fiber
- Easy to handle

DESCRIPTION

Hitachi optical directional couplers are used for dividing and coupling optical signals in optical-fiber transmission systems. These devices have many applications, such as monitors for supervising transmission line and tap-off couplers for end terminals of optical data bus, CATV etc.

Model No.	Outline
CP1X0X	Directional coupler for short wavelength
CP1X1X	Directional coupler for long wavelength

OPTICAL FIBER CONNECTORS CNXXOX, CNXX3X



FEATURES

- A high precision optical connector with very low connection loss
- No center, alignment type
- Easy, smooth connector assembly in the field
- High environmental reliability
- Low cost

DESCRIPTION

The Hitachi optical fiber connector CN series for optical fiber transmission is classified into a stainless type (CNXX0X) and plastic type (CNXX3X). The stainless-type connectors are manufactured by precision production technology and are characterized by low connection loss and high environmental reliability. The plastic-type connectors are manufactured by the precision-molding technique and are characterized by low cost and light weight.

OUTLINE

Stainless Type (CNXX0X)

Model No.	Type	Fiber	
		Core dia. (μm)	Clad dia. (μm)
CN1101	Plug	200	250
CN1102		80	125
CN1103		50	125
CN2101	Adaptor	–	–
CN2102			
CN3101	Receptacle	–	–
CN3102			

Plastic Type (CNXX3X)

Model No.	Type	Fiber	
		Core dia. (μm)	Clad dia. (μm)
CN1131	Plug	200	250
CN1132		80	125
CN2131	Adaptor	–	–
CN2132			
CN3131	Receptacle	–	–
CN3132			

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