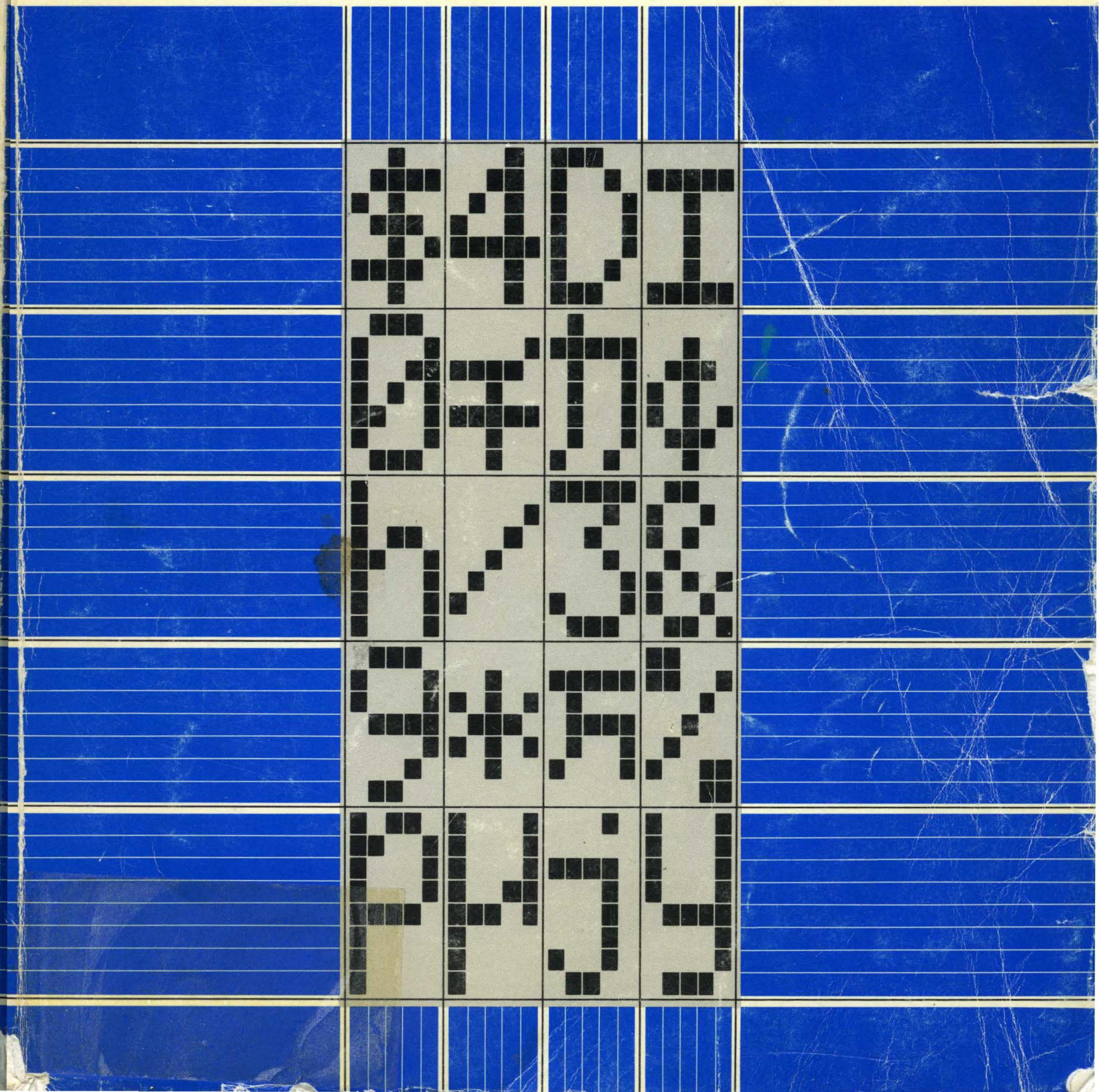
HITACHI

LIQUID CRYSTAL DISPLAY MODULES



HITACHI Liquid Crystal Display Modules

1987

PREFACE

Hitachi Dot Matrix Liquid Crystal Display (LCD) Module was developed to display numerals, alphabet, symbols, graphics, etc.

The twisted-nematic type liquid crystal, with a high contrast ratio was used. Hitachi Dot Matrix LCD Module has been widely used as a display component for portable data terminal equipment, word processors, electronic tabletop calculators, telecommunications equipment throughout the world.

This brochure describes the electrical and optical characteristics, external dimensions and precautions in handling the standard type of products.

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January 1987

Printed in U.S.A.

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Liquid Crystal Display Modules

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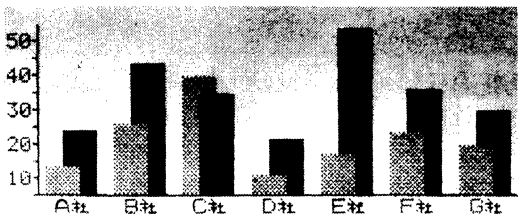
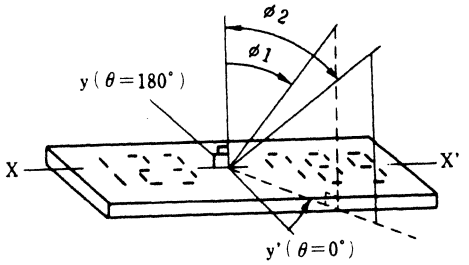
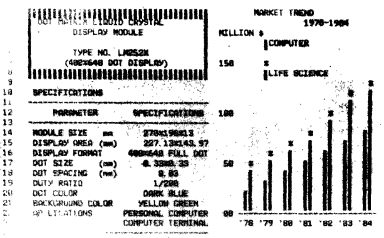
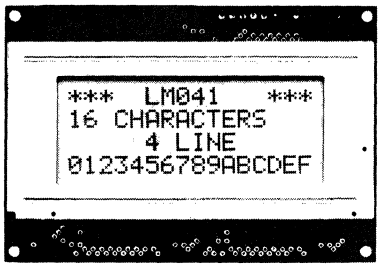
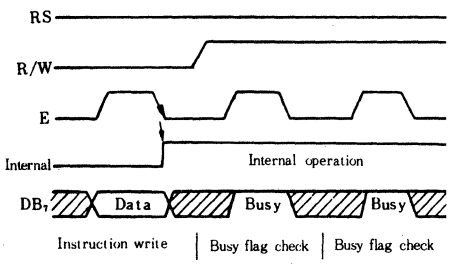




M15	C_5H_9O ⟨⬡⟩-⟨⬡⟩CN
M21	$C_7H_{15}O$ ⟨⬡⟩-⟨⬡⟩CN
M24	$C_8H_{17}O$ ⟨⬡⟩-⟨⬡⟩CN







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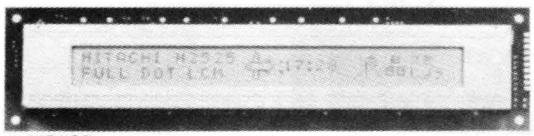
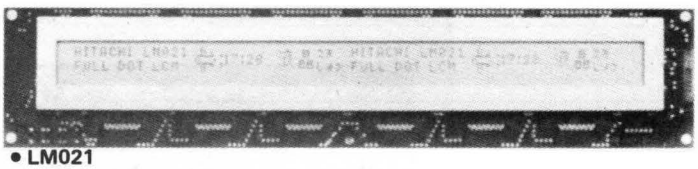
HITACHI LCM PRODUCT LINE 1

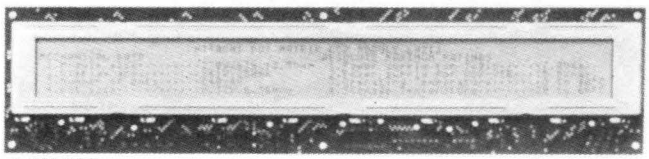
• GRAPHIC LCD MODULE



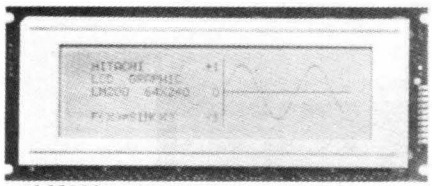
• H2525



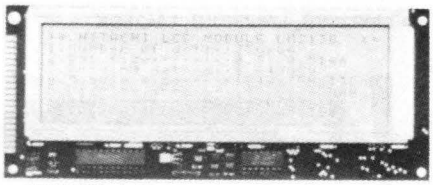
• LM021



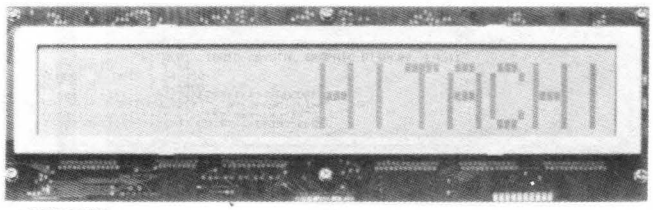
• LM212



• LM200



•LM213XB, LM213B



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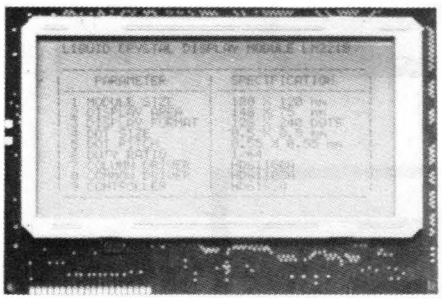
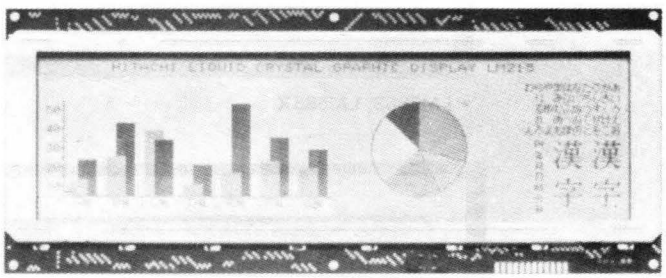
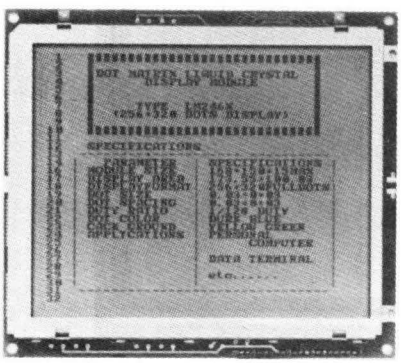


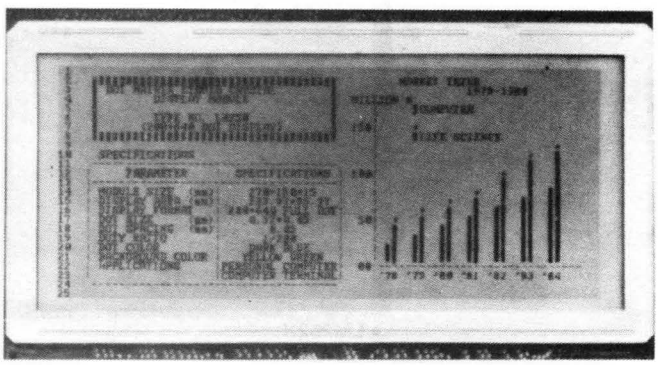
•LM221B, LM238XB



•LM215XB, LM224XB, LM240S



• LM246X



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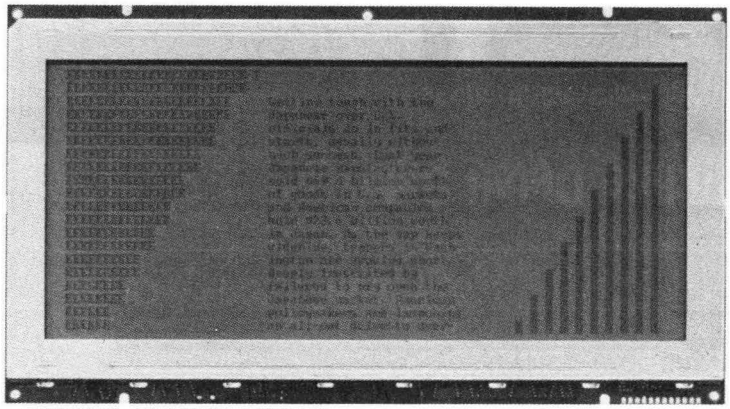
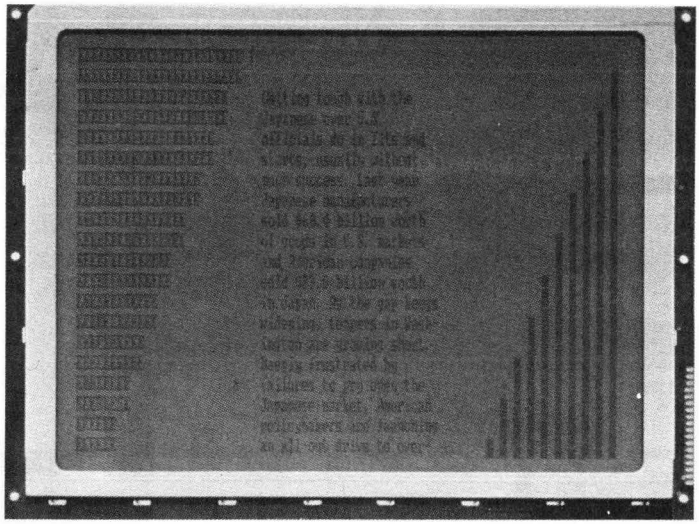
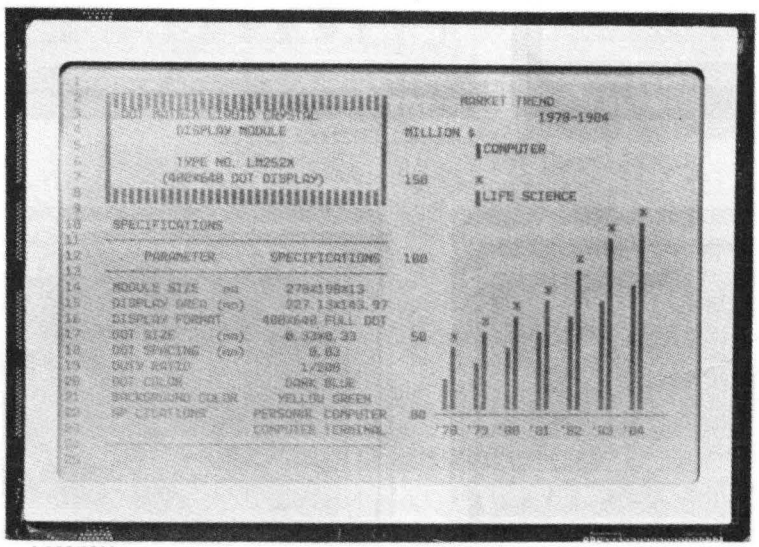


• LM236SB, LM236XB, LM250X



• LM585S, LM585X



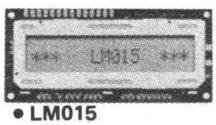
• LM252X

HITACHI

• LCD MODULE WITH BUILT-IN CONTROLLER LSI

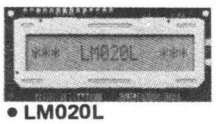
• LM054

• H2570

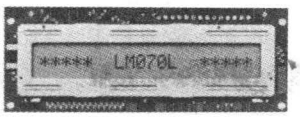


• LM015

• LM568AF



• LM020L

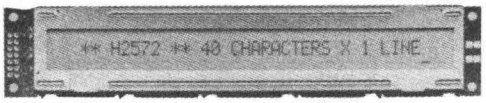


• LM070L

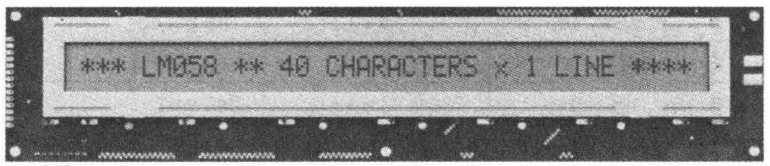
• LM038

• LM027

• H2571

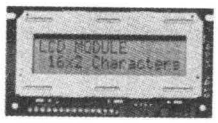


• H2572



• LM058

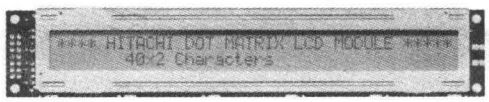
•LM052L
•LM075L



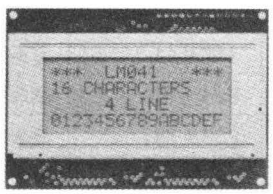
•LM016L •LM068L
•LM074L

•LM032
•LM061L

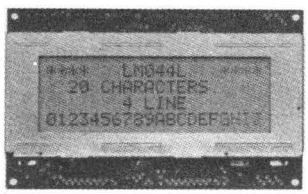
• LM017L



• LM018L



• LM041L



• LM044L

• SEGMENT TYPE LCD MODULE

• LM039

TABULATED DATA FOR HITACHI GRAPHICS MODULES

Part No.	No. of Pixels H × W	External Size L × W × Th (Max)	Effective View Area L × W	Pixel Size	Duty	Power Supply		Power Consumption
						V_{DD}-V_{SS}	V_{EE}-V_{SS}	
H2525	20 × 239	220 × 53 × 15	163 × 17	0.55 × 0.55	1/20	+5	–5	20
LM021	24 × 479	290 × 60 × 13	245 × 19	0.43 × 0.55	1/24	+5	–5	30
LM212	48 × 640	270 × 63 × 14	241 × 25	0.32 × 0.38	1/48	+5	–5	50
LM200	64 × 240	180 × 75 × 14	132 × 39	0.48 × 0.48	1/32	+5	–5	25
LM213B	64 × 256	184 × 75 × 12	149.6 × 43	0.51 × 0.51	1/64	+5	–9	250
LM213XB	64 × 256	184 × 75 × 12	149.6 × 43	0.51 × 0.51	1/64	+5	–9	250
LM211XB	64 × 480	270 × 82 × 13	240 × 38	0.44 × 0.44	1/64	+5	–9	130
LM266XP	100 × 640	288 × 72 × 13	243 × 42	0.33 × 0.33	1/100	+5	–19	140
LM551XT	128 × 128	88 × 86 × 14	54 × 54	0.35 × 0.35	1/128	+5	–20	175
LM221XB	128 × 240	180 × 120 × 14	148 × 75	0.50 × 0.50	1/64	+5	–13.5	130
LM238XB	128 × 240	180 × 120 × 14	148 × 75	0.50 × 0.50	1/64	+5	–13.5	250
LM215XB	128 × 480	270 × 110 × 12	242 × 69	0.43 × 0.43	1/64	+5	–10	100
LM224XB	128 × 480	270 × 110 × 12	242 × 69	0.43 × 0.43	1/64	+5	–11	100
LM240S	128 × 480	270 × 110 × 12	242 × 69	0.43 × 0.43	1/128	+5	–14.5	120
LM225X	200 × 640	270 × 150 × 13	239 × 104	0.32 × 0.46	1/100	+5	–13.5	400
LM236XB	200 × 640	270 × 149 × 13	239 × 104	0.32 × 0.46	1/100	+5	–14.5	170
LM250X	200 × 640	270 × 150 × 13	239 × 104	0.32 × 0.46	1/200	+5	–21.5	190
LM585X	200 × 640	260 × 195 × 13	220 × 166	0.29 × 0.74	1/100	+5	–14.5	170
LM246X	320 × 256	168 × 150 × 14	142 × 115	0.43 × 0.43	1/128	+5	–20	175
LM252X	400 × 640	270 × 198 × 13	236 × 153.6	0.33 × 0.33	1/200	+5	–21.5	240
COMPACT VERSIONS								
LM258X	64 × 240	149 × 57 × 13	117 × 41	0.44 × 0.44	1/64	+5	–12.0	100
LM254X	200 × 640	270 × 150 × 13	224 × 100	0.32 × 0.46	1/200	+5	–21.5	190
LM280X	200 × 640	270 × 104 × 11	236 × 78	0.33 × 0.33	1/200	+5	–21.5	190
LM282XP	400 × 640	270 × 198 × 14	236 × 153.6	0.33 × 0.33	1/200	+5	–21.5	240

Operating Temperature °C	Storage Temperature °C	Weight	Power Supply	Built-in LSI	Recommended Controller		Part No.
0 ~ +50	−20 ~ +60	100	Double	HD44104	HD61830	CB1020R/CB1055R	**H2525**
0 ~ +50	−20 ~ +60	150	Double	HD44100	HD61830	CB1020R/CB1055R	**LM021**
0 ~ +50	−20 ~ +60	170	Single	MSM5839	HD61830	CB1026R/CB1056R	**LM212**
0 ~ +50	−20 ~ +60	150	Double	HD44104	HD61830	CB1020R/CB1055R	**LM200**
0 ~ +50	−20 ~ +60	180	Double	HD61830 + HD44104	Built-in	—	**LM213B**
0 ~ +40	−20 ~ +60	180	Double	HD61830 + HD44104	Built-in	—	**LM213XB**
0 ~ +40	−20 ~ +60	180	Double	MSM5839/5238	HD61830	CB1026R/CB1056R	**LM211XB**
0 ~ +40	−20 ~ +60	200	Double	MSM5839/HD61105	HD63645F	—	**LM266XP**
0 ~ +40	−20 ~ +60	125	Double	HD61104/105	HD63645F	—	**LM551XT**
0 ~ +50	−20 ~ +60	210	Double	HD61100/103	HD61830	CB1026R/CB1056R	**LM221XB**
0 ~ +40	−20 ~ +60	220	Double	HD61100/103 + 61830B	Built-in	—	**LM238XB**
0 ~ +40	−20 ~ +60	320	Double	HD61100/103	HD61830	CB1030R/CB1057R	**LM215XB**
0 ~ +40	−20 ~ +60	320	Double	HD61100/103	HD61830B	—	**LM224XB**
0 ~ +50	−20 ~ +60	320	Double	MSM5279/5278	V6355/MSM6255	—	**LM240S**
0 ~ +40	−20 ~ +60	450	Double	HD61100/103	HD61830B	CB1040R/CB1058R	**LM225X**
0 ~ +40	−20 ~ +60	450	Double	MSM5279/5278	V6355/MSM6255	—	**LM236XB**
0 ~ +40	−20 ~ +60	450	Double	HD61104/105	HD63645F	—	**LM250X**
0 ~ +40	−20 ~ +60	540	Double	MSM5279/5278	V6355/MSM6255	—	**LM585X**
0 ~ +40	−20 ~ +60	265	Double	HD61104/105	HD63645F	—	**LM246X**
0 ~ +40	−20 ~ +60	540	Double	HD61104/105	HD63645F	—	**LM252X**
0 ~ +40	−20 ~ +60	110	Double	HD61100/103	HD61830	CB1020R/CB1055R	**LM258X**
0 ~ +40	−20 ~ +60	400	Double	HD61104/105	HD63645F	—	**LM254X**
0 ~ +40	−20 ~ +60	310	Double	HD61104/105	HD63645F	—	**LM280X**
0 ~ +40	−20 ~ +60	540	Double	HD61104/105	HD63645F	—	**LM282XP**

TABULATED DATA

	Part No.	Char. L By Line	External Size L × W × Th (Max)	Effective View L × W	Character Size W × H	Font Size W × H	Duty	
1 LINE SERIES	LM054	8 × 1	84 × 44 × 12	61 × 15.8	6.5 × 9.4	5 × 8	1/8	
	H2570	16 × 1	80 × 36 × 12	64.5 × 13.8	63.15 × 7.9	5 × 11	1/11	
	LM015	16 × 1	80 × 36 × 12	64.5 × 13.8	3.15 × 5.5	5 × 8	1/8	
	LM568AF	16 × 1	122 × 33 × 12	99 × 13	4.84 × 8.06	5 × 7 w/cursor	1/8	
	LM020L	16 × 1	80 × 36 × 12	64.5 × 13.8	3.07 × 5.73	5 × 8	1/16	
	LM070L	20 × 1	105 × 39 × 11	84 × 13	3.2 × 5.2	5 × 7 w/cursor	1/8	
	LM038	20 × 1	182 × 35.5 × 13	154 × 15.3	6.7 × 9.4	5 × 7 w/cursor	1/8	
	LM027	24 × 1	126 × 36 × 12	100 × 13.8	3.15 × 7.9	5 × 11	1/11	
	H2571	32 × 1	174.5 × 33 × 13.4	132.5 × 14	3.15 × 7.9	5 × 11	1/11	
	H2572	40 × 1	182 × 35.5 × 13	154 × 15.3	3.15 × 7.9	5 × 11	1/11	
	LM058	40 × 1	290 × 60 × 13	245 × 19	4.82 × 8.18	5 × 8	1/8	
2 LINE SERIES	LM052L	16 × 2	80 × 36 × 12	64.5 × 13.8	2.95 × 3.8	5 × 8	1/16	
	LM075L	16 × 2	80 × 36 × 12	64.5 × 13.8	2.95 × 3.8 6.60 × 9.4 (numeric)	5 × 8	1/16	
	LM016L	16 × 2	84 × 44 × 12	61 × 15.8	2.95 × 4.86	5 × 8	1/16	
	LM068L	16 × 2	83 × 43 × 11	61 × 17.6	2.95 × 4.86	5 × 8	1/16	
	LM074L	16 × 2	84 × 44 × 12	61 × 15.8	2.95 × 4.86 6.51 × 11.5 (numeric)	5 × 8	1/16	
	LM032L	20 × 2	116 × 39 × 13	83 × 18.6	3.2 × 4.85	5 × 8	1/16	
	LM061L	20 × 2	115 × 39 × 13	83 × 18.6	3.2 × 4.85	5 × 8	1/16	
	LM060L	24 × 2	116 × 39 × 13	83 × 18.6	2.7 × 4.85	5 × 8	1/16	
	LM017L	32 × 2	174.5 × 33 × 13.4	141.2 × 16.75	3.45 × 4.85	5 × 8	1/16	
	LM018L	40 × 2	182 × 35.5 × 13	154 × 15.3	3.2 × 4.85	5 × 8	1/16	
4 LINE SERIES	LM041L	16 × 4	87 × 60 × 12	61.8 × 25.2	2.95 × 4.15	5 × 8	1/16	
	LM044L	20 × 4	98 × 60 × 12	76 × 25.2	2.95 × 4.15	5 × 8	1/16	
COMPACT VERSIONS								
	LM104L	16 × 2	80 × 30 × 11	62 × 15.1	2.96 × 4.86	5 × 8	1/16	
	LM105L	20 × 2	95 × 30 × 11	76.7 × 15.1	3.2 × 4.85	5 × 8	1/16	
	LM107L	40 × 2	170 × 30 × 11	152.6 × 15.1	3.2 × 4.85	5 × 8	1/16	
L.E.D. BACKLIGHT VERSIONS								
	LM087LN	16 × 1	90 × 36 × 14	64.5 × 13.8	3.07 × 5.73	5 × 8	1/16	
	LM086LN	6 × 2	90 × 36 × 14	64.5 × 13.8	2.95 × 3.8	5 × 8	1/16	
	LM093LN	16 × 2	90 × 44 × 14	61 × 16.3	2.96 × 4.86	5 × 8	1/16	
	LM091LN	20 × 2	126 × 39 × 14	83 × 18.6	3.2 × 4.85	5 × 8	1/16	
	LM092LN	40 × 2	192 × 35.5 × 16	154 × 15.3	3.2 × 4.85	5 × 8	1/16	

Power Supply		Power Consumption	Operating Temperature °C	Storage Temperature °C	Weight (g)	Power Supply	Built-in LSI Controller and Driver	Part No.
V_{DD}-V_{SS}	V_{EE}-V_{SS}							
+5	0	10	0 ~ +50	−20 ~ +70	25	Single	HD44780	**LM054**
+5	0	10	0 ~ +50	−20 ~ +70	25	Single	HD44780 + HD44100 or MSM5259	**H5270**
+5	0	10	0 ~ +50	−20 ~ +70	25	Single		**LM015**
+5	0	10	0 ~ +50	−20 ~ +70	30	Single		**LM568AF**
+5	0	10	0 ~ +50	−20 ~ +70	25	Single	HD44780	**LM020L**
+5	0	10	0 ~ +50	−20 ~ +70	40	Single	HD44780 + HD44100 or MSM5259	**LM070L**
+5	0	10	0 ~ +50	−20 ~ +70	65	Single		**LM038**
+5	0	10	0 ~ +50	−20 ~ +70	40	Single		**LM027**
+5	0	10	0 ~ +50	−20 ~ +70	60	Single		**H2571**
+5	0	10	0 ~ +50	−20 ~ +70	65	Single		**H2572**
+5	0	10	0 ~ +50	−20 ~ +70	150	Single		**LM058**
+5	0	15	0 ~ +50	−20 ~ +70	25	Single		**LM052L**
+5	0	15	0 ~ +50	−20 ~ +70	25	Single		**LM075L**
+5	0	15	0 ~ +50	−20 ~ +70	25	Single		**LM016L**
+5	0	15	0 ~ +50	−20 ~ +70	25	Single		**LM068L**
+5	0	15	0 ~ +50	−20 ~ +70	25	Single		**LM074L**
+5	0	15	0 ~ +50	−20 ~ +70	50	Single		**LM032L**
+5	0	15	0 ~ +50	−20 ~ +70	50	Single		**LM061L**
+5	0	15	0 ~ +50	−20 ~ +70	60	Single		**LM060L**
+5	0	15	0 ~ +50	−20 ~ +70	60	Single		**LM017L**
+5	0	15	0 ~ +50	−20 ~ +70	65	Single		**LM018L**
+5	0	15	0 ~ +50	−20 ~ +70	60	Single		**LM041L**
+5	0	15	0 ~ +50	−20 ~ +70	65	Single		**LM044L**
+5	0	15	0 ~ +50	−20 ~ +70	25	Single	HD44780 + HD44100 or MSM5259	**LM104L**
+5	0	15	0 ~ +50	−20 ~ +70	50	Single		**LM105L**
+5	0	15	0 ~ +50	−20 ~ +70	65	Single		**LM107L**
+5	0	150	0 ~ +50	−20 ~ +70	40	Single	HD44780	**LM087LN**
+5	0	400	0 ~ +50	−20 ~ +70	50	Single	HD44780 + HD44100 or MSM5259	**LM086LN**
+5	0	400	0 ~ +50	−20 ~ +70	50	Single		**LM093LN**
+5	0	550	0 ~ +50	−20 ~ +70	65	Single		**LM091LN**
+5	0	850	0 ~ +50	−20 ~ +70	80	Single		**LM092LN**

SEMICUSTOM

We provide liquid-crystal module with optional specifications as follows. Table 1 shows LCD module already in production.

A: Black coated metal frame
T: Transflective type for installing the EL
H: Available in extended temperature range (operating −10°C ~ +70°C, storage: −40°C ~ +80°C), driven by double power supply.
L: Duty = 1/16, available with single power circuit +5V.
N: Electroluminescent panel

How to read the table.
●: Under production
○: Unable to produce technically.
Blank: Able to develop on customer's request.

Table 1. Semicustom List

	No.	Part No.	No. of Display W×H	OPTIONAL SPECIFICATIONS							Remarks
				A	T	H	LT	HT	N	12:00 Viewing	
Graphics Displays	1	H2525	20×239				○	○			
	2	LM021	24×479				○	○		LM607	
	3	LM212	48×640			○	○	○			
	4	LM200	64×240		●	●	○	●		LM523	
	5	LM213XB	64×256		○	○	○	○	●		
	6	LM211XB	64×480			○	○	○			
	7	LM266XP	100×640			○	○	○			
	8	LM221B	128×240			○	○	○			
	9	LM238XB	128×240			○	○	○			
	10	LM215XB	128×480			○	○	○			
	11	LM224XB	128×480			○	○	○			
	12	LM240S	128×480			○	○	○			
	13	LM225X	200×640			○	○	○			
	14	LM236XB	200×640			○	○	○			
	15	LM250X	200×640			○	○	○			
	16	LM585X	200×640			○	○	○			
	17	LM246X	256×320			○	○	○			
	18	LM252X	400×640			○	○	○			
	19	LM258X	64×240			○	○	○			
	20	LM254X	200×640			○	○	○			
	21	LM280X	200×640			○	○	○			
	22	LM282X	400×640			○	○	○			
Character Displays	23	LM054	8×1		●	●	○			LM094	
	24	H2570	16×1		●	●	○	●			
	25	LM015	16×1		●		○			LM056	
	26	LM568AF	16×1	●			○				
	27	LM020L	16×1							LM089L	
	28	LM070L	20×1								
	29	LM038	20×1		●	●	○	●			
	30	LM027	24×1		●		○				
	31	H2571	32×1		●	●	○	●		LM033	
	32	H2572	40×1	●	●	●	○				
	33	LM058	40×1		●		○				
	34	LM052L	16×2							LM071L	
	35	LM075L	16×2								
	36	LM016L	16×2	●	●	●	●	●		LM507L	
	37	LM068L	16×2								
	38	LM074L	16×2								
	39	LM032L	20×2		●	●	●				
	40	LM061L	20×2		●	●		●		LM082L	
	41	LM060L	24×2								
	42	LM017L	32×2		●	●	●	●			
	43	LM018L	40×2		●	●	●	●		LM035L	
	44	LM041L	16×4	●		●	●	○			
	45	LM044L	20×4				●	○		LM083L	
	46	LM104L	16×2		○	○		○			
	47	LM105L	20×2		○	○		○			
	48	LM107L	40×2		○	○		○			
	49	LM039	16×1	●	○		○	○	○		

HITACHI LCD DRIVER LINE-UP

- General

Type No.	Function & features	Supply logic	V_{DD}-V_{EE}	LCD driver		Package
				Duty	Driver	
HD44100H	LCD Driver • Internal shift register: 20 bit x 2	5 V	10 V	Free	40	FP-60
HD61100A	LCD Driver • Internal shift register: 80 bit High speed operation: 2.4MHz	5 V	16.5 V	Free	80	FP-100

- Segment display

Type No.	Function & features	Supply logic	V_{DD}-V_{EE}	LCD driver		Package
				Duty	Driver	
HD61602	7 Segment LCD Driver • Low power: 0.5 mW (5 V) • Internal LCD power supply	2.2 ~ 5.5 V	2.2 ~ 5.5 V	Static 1/2, 1/3 1/4	51	FP-80
HD61603	7 Segment LCD Driver • Low power: 0.5 mW (5 V)	2.2 ~ 5.5 V	2.2 ~ 5.5 V	Static	64	FP-80

- Character display

Type No.	Function & features	Supply logic	V_{DD}-V_{EE}	LCD driver		Package
				Duty	Driver	
LCD II (HD44780)	LCD Controller/driver • No. of chracter: 80 max • Character generator: 192 • Font: 5 x 7 or 5 x 10	5 V	—	1/8, 1/11 1/16	Com. 16 Seg. 40	FP-80
HD43160AH	LCD Controller • No. of chracter: 80 max • Character generator: 160 • Font: 5 x 7 or 5 x 11	5 V	—	1/8, 1/12 1/16	—	FP-54

- Graphic display

Type No.	Function & features	Supply logic	V_{DD}-V_{EE}	LCD driver		Package
				Duty	Driver	
HD44102CH	Segment driver (1/32 duty) • Internal RAM: 8 x 50 x 4 bit • Direct display of RAM data	5 V	10 V	1/8, 1/12, 1/16, 1/24, 1/32	Seg. 50	FP-80
HD44103CH	Common driver (1/32 duty) • Internal timing generator	5 V	10.5 V		Com. 20	FP-60
HD44105H	Common driver (1/64 duty) • Large No. of LCD driver	5 V	10.5 V	1/8, 1/12, 1/16, 1/24, 1/32, 1/64	Com. 32	FP-60
HD61830	LCD Controller for graphic • Grafic or character mode • Character generator: 192	5 V	—	Static ~ 1/128	—	FP-60
HD61830B	LCD Controller for graphic • High speed shift: 2.4 MHz	5 V	—	Static ~ 1/128	—	FP-60
HD61102	Segment driver (1/64 duty) • Internal RAM: 8 x 64 x 8 bit • Direct display of RAM data	5 V	15 V	1/48, 1/64, 1/100, 1/128	Seg. 64	FP-100
HD61103A	Common driver (1/64 duty) • Internal timing generator	5 V	16.5 V		Com. 64	FP-100

PERFORMANCE DATA 2

FEATURES

1. Various types are available, from small-size module for character display, to large-size module for graphic display.
2. All modules include driver LSI on board. Some modules also include controller LSI.
3. When using graphic liquid crystal display module, use our recommendable control circuit board that simplifies the display system.
4. Due to its small size and light weight, compact display equipment can be constructed. Also, low driving voltage and low power consumption make battery power operation possible.

APPLICATIONS

1. Portable data terminal equipment
2. Word processors
3. Telephone applications
4. Facsimile machines
5. Personal computers
6. POS terminal equipment
7. Electronic typewriters
8. Measuring instruments
9. Other display devices

MAXIMUM RATINGS

Electric maximum ratings

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply for logic	$V_{DD} - V_{SS}$	Refer to individual specification		V	
Power supply for LCD drive	$V_{DD} - V_O$			V	
Input voltage	V_I			V	
Static electricity		–	100	V	See note

Note Electro-static discharge resistance is tested by charging a condenser with a capacity of 200pF and discharging it by contact with an interface connector pin.

Environmental conditions

Item	Operating		Non-operating		Remarks
	Min.	Max.	Min.	Max.	
Ambient temperature	Refer to individual specifications				No dew
Humidity	Note				
Vibration	–	0.5G	–	2G	
Shock	–	3G	–	50G	XYZ 3 directions
Corrosion gas	No corrosion gas				

Note Humidity conditions are as follows.

Number of dots / Ambient temperature (Ta)	Under 128 x 240	128 x 240 or over
Ta ≦ 40°C	95% RH max.	85% RH max.
Ta > 40°C (Below maximum temperature)	Below maximum absolute humidity of 40°C 95% RH	Below maximum absolute humidity of 40°C 85% RH

OPTICAL DATA

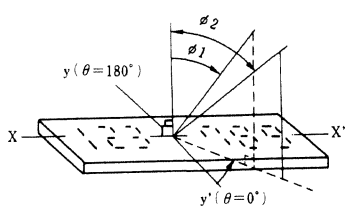
Gray type · S type (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Units	Notes to see
Viewing angle	$\phi 2-\phi 1$	K=1.4	20	–	–	deg.	1, 2, 7
Contrast ratio	K	$\phi=25°$ $\theta=0°$	–	3	–	–	3
Response time (rise)	t_r	$\phi=25°$ $\theta=0°$	–	200	400	ms	4
				250	400		4, 5
				150	250		4, 6
Response time (fall)	t_f	$\phi=25°$ $\theta=0°$	–	200	400	ms	4
				250	400		4, 5
				150	250		4, 6

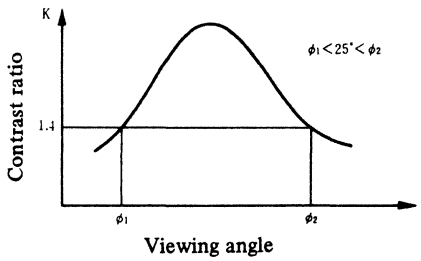
X type (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Units	Notes to see
Viewing angle	$\phi 2-\phi 1$	K = 1.4	–	40	–	deg.	8
Contrast ratio	K	$\phi = 10°, \theta = 0°$	–	3 to 6	–	–	
Response time (rise)	t_r	$\phi = 10°, \theta = 0°$	–	250	400	ms	
Response time (fall)	t_f	$\phi = 10°, \theta = 0°$	–	350	450	ms	

Note 1. Definition of θ and ϕ

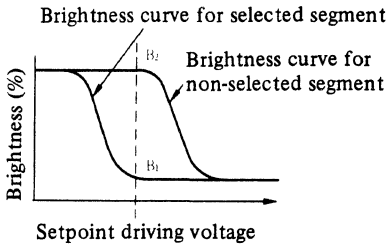


Note 2. Definition of viewing angle $\phi 1$, and $\phi 2$

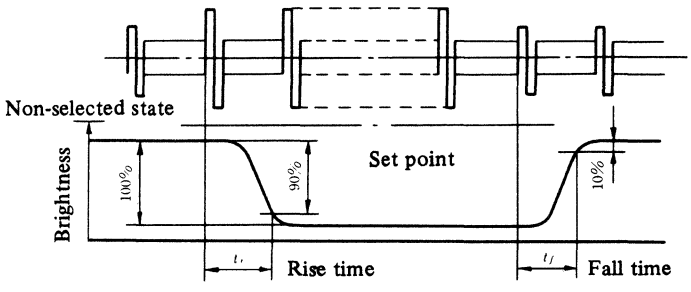


Note 3. Definition of contrast "K"

$$K = \frac{\text{Brightness of non-selected segment } (B_2)}{\text{Brightness of selected segment } (B_1)}$$



Note 4. Definition of optical response



Note 5. Applied models
LM054 • LM020L • LM038 • H2570 • LM015 • LM027 • H2571 • H2572
LM016L • LM032L • LM017L • LM018L • LM041L • LM044L • LM052L • LM568AF
LM070L • LM060L • LM075L • LM068L • LM074L • LM061L

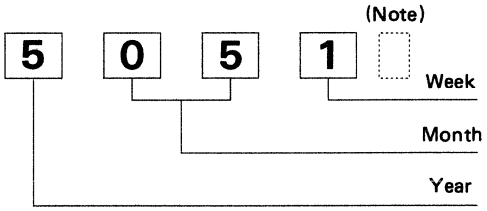
Note 6. Applied models
H2525 • LM200 • LM021 • LM213B • LM212

Note 7. Typical viewing angle of following models is 20°.
LM200 • LM213B • LM212 • LM240S

Note 8. Applied models
LM213XB • LM211XB • LM266XP • LM238XB • LM215XB • LM224XB • LM258X
LM254X • LM280X • LM282XP • LM246X • LM225X • LM236XB • LM250X
LM252X • LM585X • LM221XB • LM551XT

LOT MARK

(1) Lot mark
Lot number of Hitachi LCD module is shown by four digit number as follows.



(Note) Some products have alphabet at the end.

Year mark

Year	Figure
1985	5
1986	6
1987	7
1988	8
1989	9
1990	0

Month mark

Month	Figure	Month	Figure
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sept.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week mark

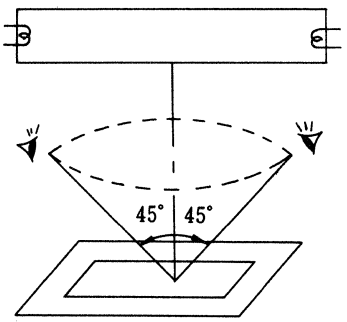
Week (Day)	Figure
21~27	1
28~ 3	2
4~10	3
11~17	4
18~20	5

(2) Location of lot mark
Indicated on the printed circuit board as below.

Ex.: 5051

APPEARANCE STANDARD

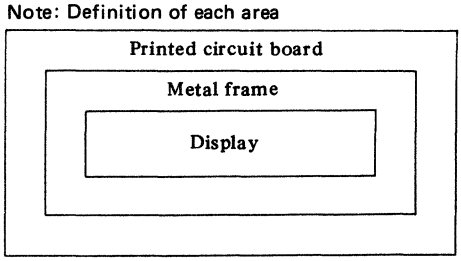
(1) Appearance inspection conditions
Visual inspection under single 20W fluorescent lamp with eyes to LCD distance 25 cm and lamp to LCD distance 25 to 30 cm.
Viewing angle should be smaller than 45°.



(2) Appearance standard

No.	Items	Criteria			Applied area
1	Scratches	Distinguished one is not acceptable. (To be judged by HITACHI limit sample)			Display
2	Dents				
3	Wrinkles in polarizer				
4	Bubbles	Average dia. D (mm)		Max. number acceptable	
		1.0 < D		0	
		0.5 < D ≦ 1.0		1	
		0.3 < D ≦ 0.5		5	
		D ≦ 0.3		Ignore	
5	Stains, foreign materials	Filamentous			
		Length (mm)	Thickness (mm)	Max. number acceptable	
		Ignore	0.02 ≧	Ignore	
		2.0 ≧	0.03 ≧	6	
		1.0 ≧	0.06 ≧	6	
		Round			
		Average dia. D (mm)		Max. number acceptable	
		D < 0.25		Ignore	
		0.25 ≦ D < 0.35		4	
		0.35 ≦ D		None	
		Those can be wiped out easily are acceptable.			All
6	Interference fringe	Distinguished one is not acceptable. (To be judged by HITACHI limit sample)			Display
7	Non-display	There should be none			
8	Chipped glass	If it has nothing to do with function, ignore.			Printed circuit board
9	Dimensions	Refer to individual acceptance specifications.			All
10	Dark spots	Average dia. D (mm)		Max. number acceptable	Display
		0 < 0.1		Ignore	
		0.1 ≦ D < 0.3		3	

Note: Definition of each area



STRUCTURE AND DRIVING PRINCIPLES OF LIQUID CRYSTAL DISPLAYS

General

A liquid crystal is an intermediate phase between the liquid and solid states. Outwardly, it appears to be a liquid, but electrically and optically, it shows the properties of a crystal. Liquid crystals are used in liquid crystal displays.

Types of Liquid Crystal Displays

Type	Description	
TN	An electric field moves the molecules of the liquid crystal from a twisted alignment to vertical alignment. The display employs polarizer. This type is the most widely used at present. (Detailed below)	Polarizer, Voltage OFF, Transparent (white); Voltage ON, Opaque (black)
Guest-host	An electric field moves the molecules of a liquid crystal containing dye molecules. This type has better viewing angle properties than the TN type, and a bright color display is possible.	Voltage OFF, Dye, Colored light; Voltage ON, Transparent

Note: TN: Twisted Nematic

Basic structure of a Liquid Crystal Display (TN type)

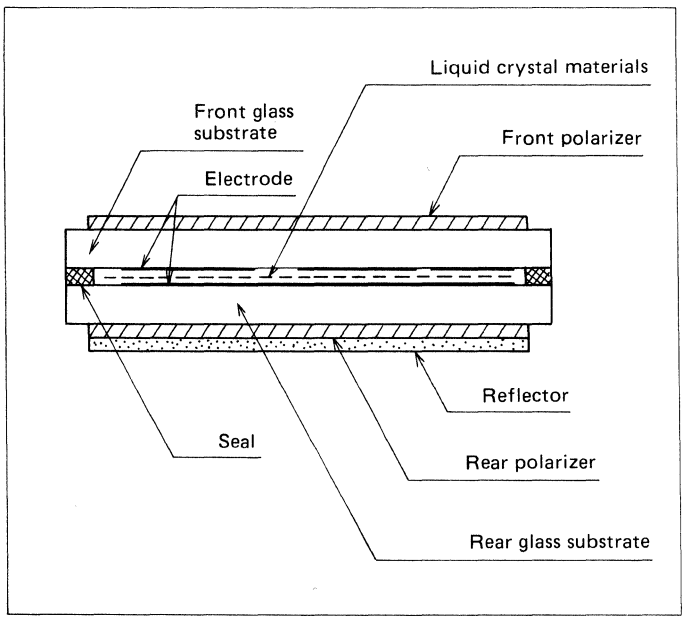


Fig. 1.1 Basic structure

Driving principle (TN type)

A liquid crystal display could be described as an electronic shutter that is transparent when no voltage is applied but becomes opaque when the voltage is turned on (or vice versa). This effect is used to display numerals, characters, and other patterns. The principle of operation of a liquid crystal display is shown in Fig. 1.2.

(1) The liquid crystal display is sandwiched between two polarizers, whose axes of polarization usually are crossed by 90°.

(2) When there is no voltage, the molecules of the liquid crystal are aligned with a 90° twist, and rotate the plane of polarization of the light by 90°, as in Fig. 1.2 (a), so that the light passes through both polarizers.

(3) When a voltage is applied, the molecules of the liquid crystal align perpendicular to the substrate, so that the light is cut off by the second polarizer, as in Fig. 1.2 (b).

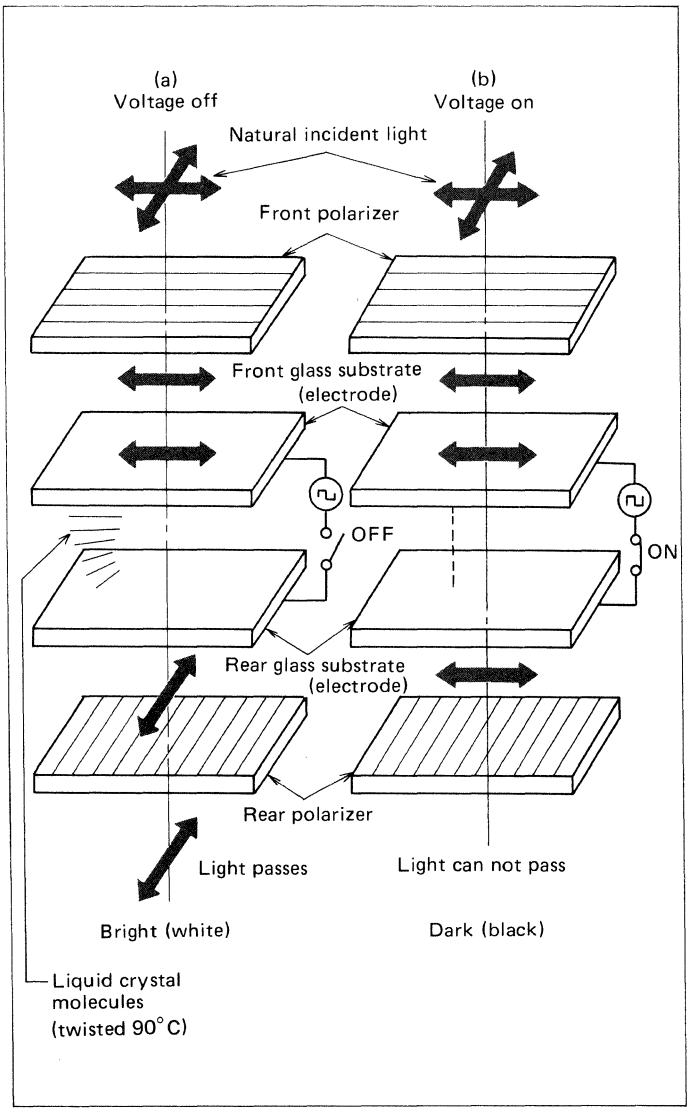
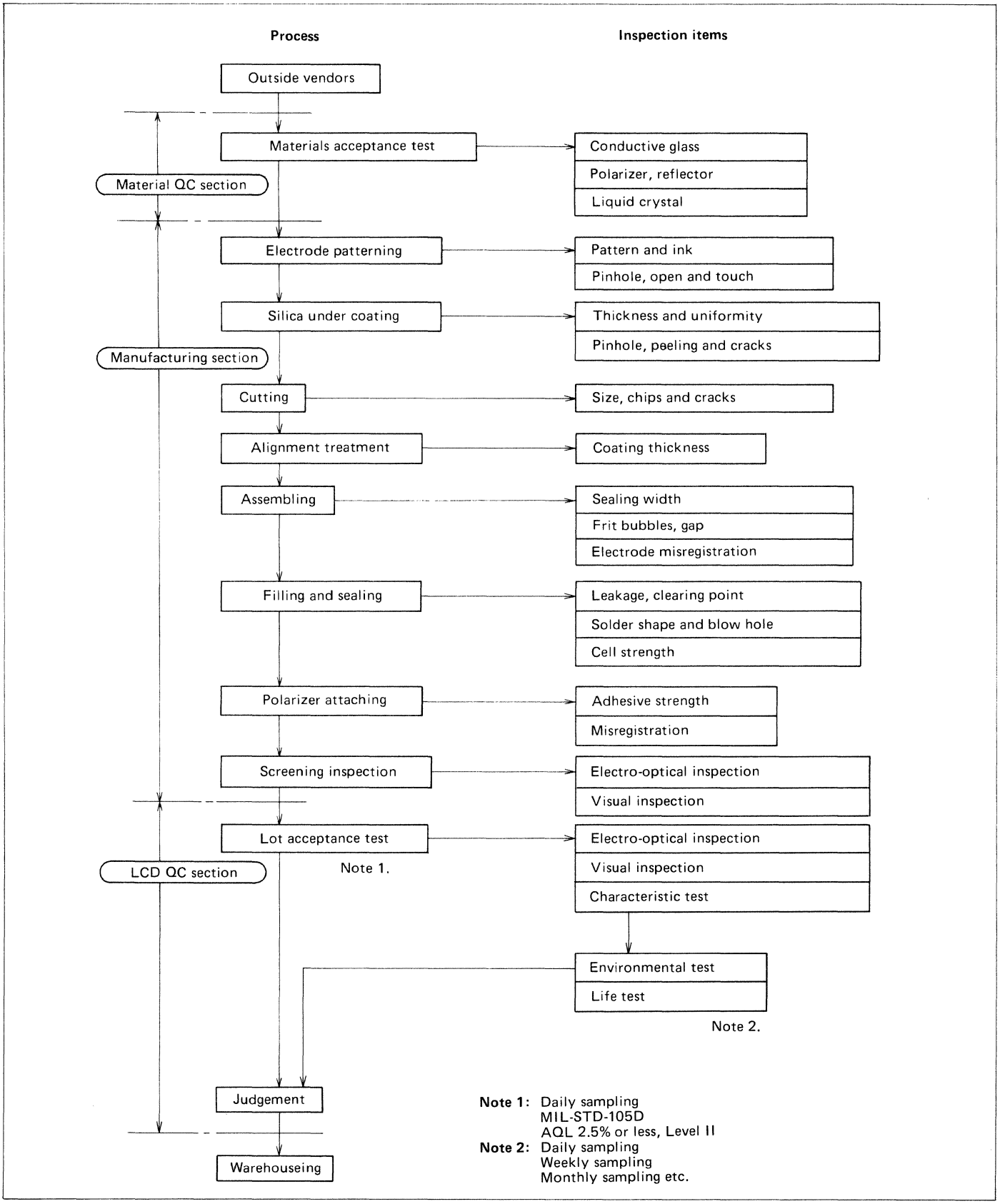


Fig. 1.2 Principle of operation

RELIABILITY OF LCD

Inspection procedure for LCD



Reliability test data of LCM (Standard temperature range type)

No.	Item	Condition	Time
1	High temperature operating	50°C normal operating drive	500 h
2	Temperature cycle operating	0°C 2 h, 50°C 6 h cycles, normal operating drive	1000 h
3	High temperature storage	70°C	500 h
4	High temp. and humidity storage	40°C 95% RH (Note)	100 h
5	Low temperature storage	–20°C	500 h
6	Heat shock	70°C 0.5 h, –20°C 0.5 h	24 cycles
7	Vibration operating	10 ~ 50 Hz, 1G, 51 ~ 300Hz, 0.5G X, Y, Z normal operating drive	1 h each
8	Vibration non-operating	10 ~ 50 Hz, 1G, 51 ~ 300Hz, 0.5G	1 h each
9	Shock	50G 15 ms ± X, Y, Z	1 time each
10	UV test	Sunshine weathermeter 43°C	60 h

Note: Module must be stored in non dew condition under testing.

Reliability test data of LCM (Wide temperature range type)

No.	Item	Condition	Time
1	High temperature operating	70°C normal operating drive	500 h
2	Temperature cycle operating	–10°C 2 h, 70°C 6 h cycles, normal operating drive	1000 h
3	High temperature storage	80°C	500 h
4	High temp. and humidity storage	55°C 95% RH (Note)	250 h
5	Low temperature storage	–40°C	500 h
6	Heat shock	80°C 0.5 h, –30°C 0.5 h	24 cycles
7	Vibration operating	10 ~ 50 Hz, 1G, 51 ~ 300Hz, 0.5G X, Y, Z normal operating drive	1 h each
8	Vibration non-operate	10 ~ 50 Hz, 1G, 51 ~ 300Hz, 0.5G	1 h each
9	Shock	50G 15 ms ± X, Y, Z	1 time each
10	UV test	Sunshine weathermeter 43°C	60 h

Note: Module must be stored in non dew condition under testing.

Note: 'X' type LCMs not applicable to above tables.

Results of reliability tests

Tables 5.1 and 5.2 show the results of reliability tests. The operating lifetime test and several of the other tests will be analyzed below to provide a full description of the reliability of the liquid crystal display.

Table 5.1 Results of lifetime and environmental tests of Hitachi liquid crystal displays

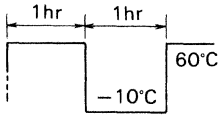
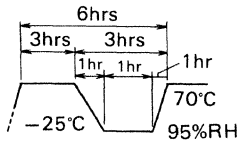
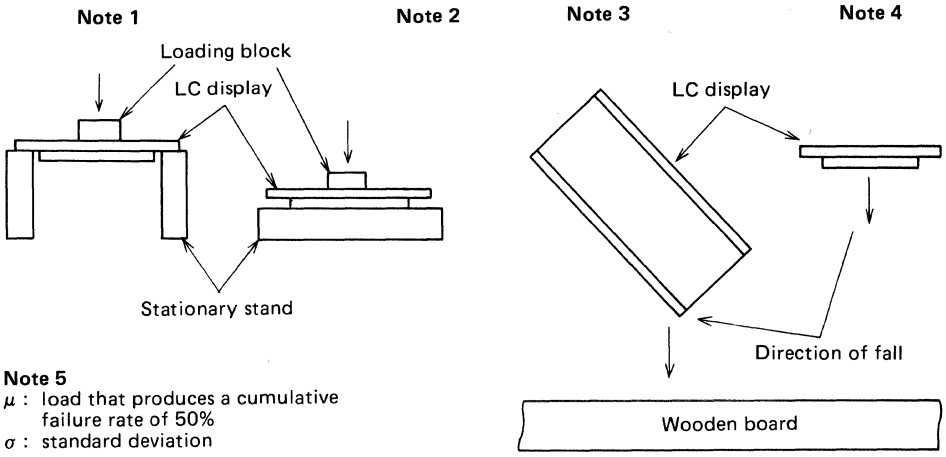
Test items	With polarizer and reflector?	Test conditions	Test time	No. of units tested	Failure rate (%)
1. High-temperature lifetime	Yes	60°C, 5V, 32Hz	7,000 h	50	0
		30°C, 12V, 32Hz	7,000 h	40	
2. Exposure to high temperature and humidity	No	70°C, 95% RH	100 h	360	0
	Yes	40°C, 95% RH	1,000 h	90	
3. Temperature cycle	No		30 cycles	90	0
4. Temperature & humidity cycle	No		30 cycles	90	0
5. Exposure to high temperature	No	70°C	1,000 h	240	0
		95°C	100 h	240	0
	Yes	60°C	1,000 h	100	0
6. Exposure to low temperature	Yes	−30°C	1,000 h	100	0
		−40°C	800 h	90	0
7. Low and high atms. pressure	Yes	25°C, 0.01 mmHg	96 h	50	0
		25°C, 2,280 mmHg	96 h	50	0
8. Exposure to ultraviolet light	Yes	Carbon arc	500 h	10	0
		Outdoor exposure	3,000 h	10	
9. Polarizer & reflector reliability	Yes	30°C, 55°C, 70°C Dry	5,000 h	30	0
		70°C Dry	1,000 h	240	
		95°C Dry	100 h	240	
		40°C, 50°C, 70°C, 90% RH	5,000 h	30	

Table 5.2 Results of mechanical tests of Hitachi liquid crystal displays

Test items	With polarizer and reflector?	Test conditions	Test time	No. of units tested	Failure rate (%)
1. Immersion	No	Warm water (+70°C) Cold water (+15°C)	20 cycles	500	0
2. Saltwater spray	No	MIL-STD-202DM 101C	96 h	50	0
3. Vibration	Yes	MIL-STD-202DM 201A	2 h	50	0
4. Impact	Yes	Impact time: 0.5 ms		20	μ = 1,250 G σ = 150 G
5. Static load	Yes	Loading speed: 1 mm/min Note 1	Note 5	20	μ = 14.8 kg σ = 0.6 kg
		Loading speed: 1 mm/min Note 2		20	μ = 19 kg σ = 2 kg
6. Drop	Yes	Note 3	—	20	μ = 360 cm σ = 70 cm
		Note 4	—	20	μ = 120 cm σ = 30 cm



Note 5
μ : load that produces a cumulative failure rate of 50%
σ : standard deviation

Operating lifetime

As shown in Fig. 5.1, in a voltage-accelerated lifetime test (voltage = 100 VAC), the cumulative failure rate after 600 hours was 10%, but at voltages of 12 VAC and 5 VAC (60°C), there were still no failures after 7,000 hours. The inferred relation between applied voltage and lifetime is shown in Fig. 5.2. For a typical practical voltage of 3.1 V, the lifetime is estimated to be in excess of 90,000 hours (10 years). A DC voltage lifetime test showed no failures after 3,000 hours (at 5 VDC). This test establishes the strong insulation qualities of Hitachi liquid crystal displays.

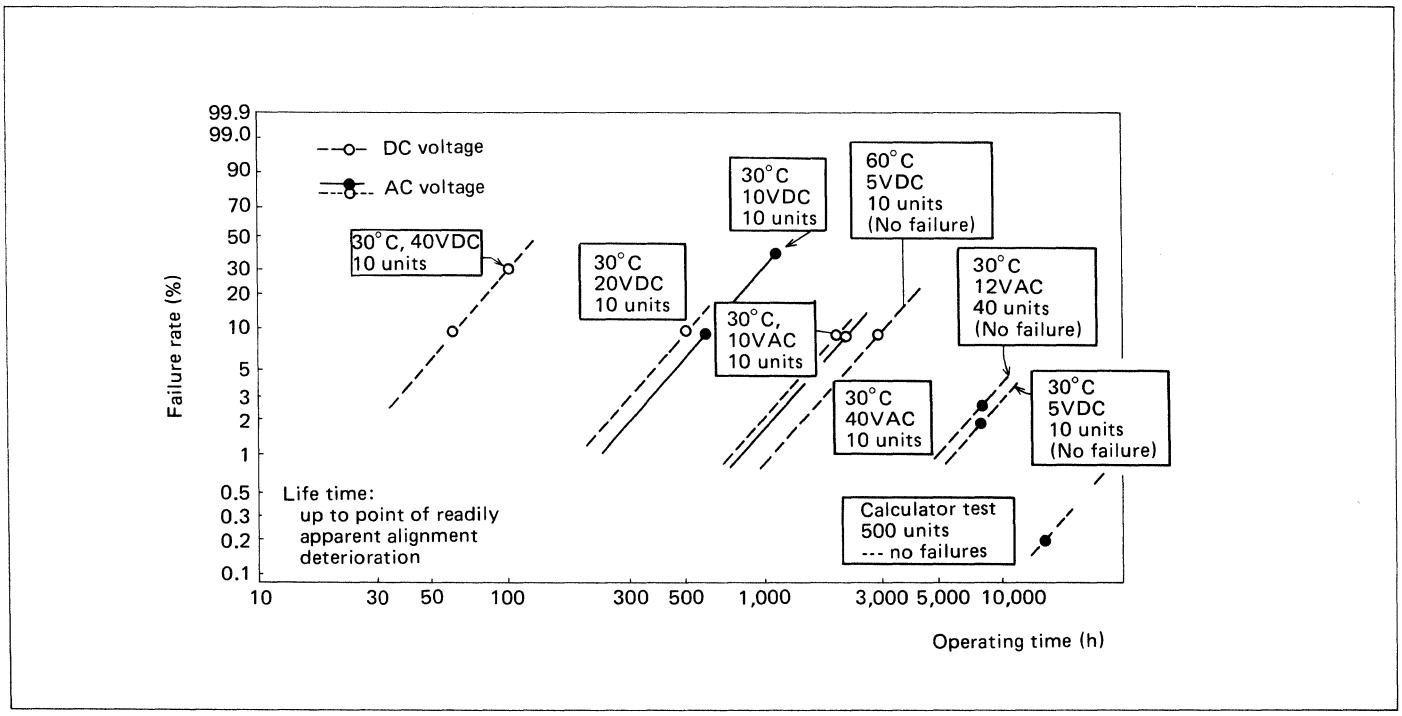


Fig. 5.1 Results of voltage-accelerated lifetime tests of Hitachi liquid crystal displays

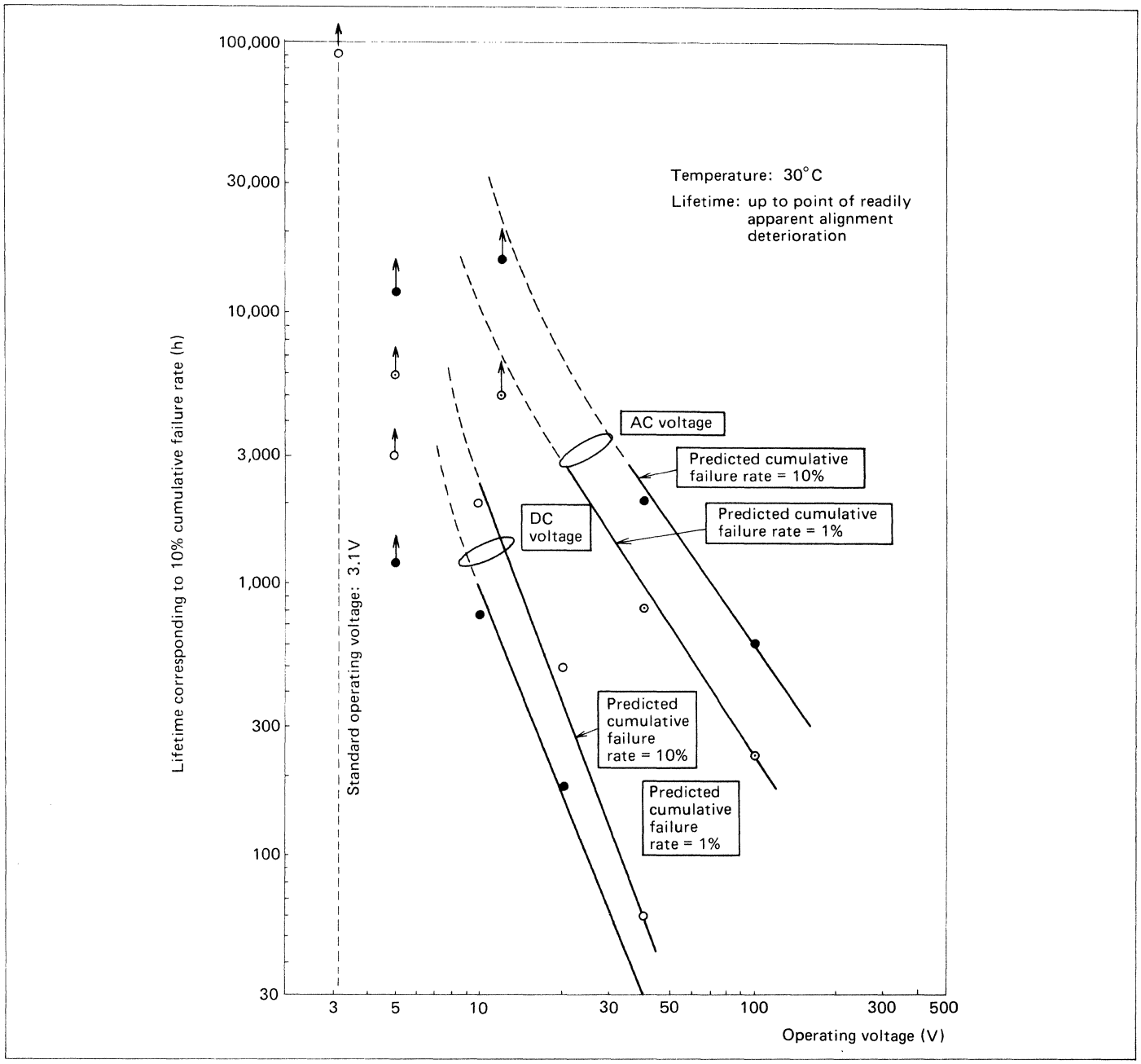


Fig. 5.2 Dependence of liquid crystal display lifetime on AC and DC voltage

High temperature and humidity test

Figure 5.3 shows the results of reliability tests under high temperature and humidity. There were no failures after 100 hours at 70°C and 95% RH, and 10% failures after 250 hours. There were two failures modes: Character blurring caused by segment widening, and loss of seal. At 40°C and 95% RH there were no failures after 100 hours and only 1% failures after 3,000 hours. The inferred relation between temperature and lifetime is shown in Fig. 5.4. According to Fig. 5.4, at a normal temperature of 25°C and relative humidity of 95%, a lifetime of more than 90,000 hours (10 years) can be expected.

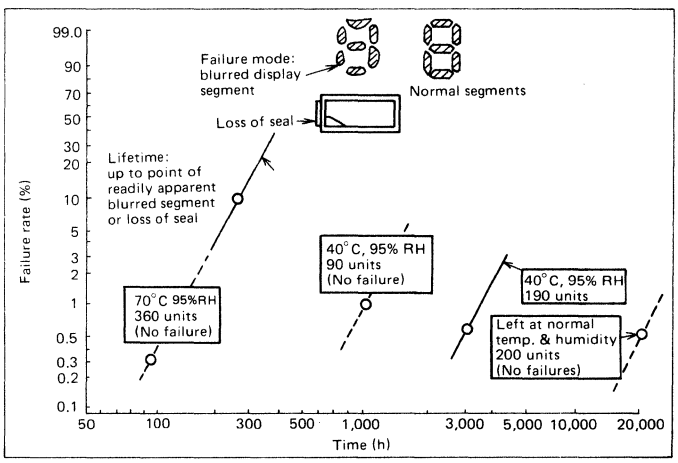


Fig. 5.3 Reliability under high temperature and humidity

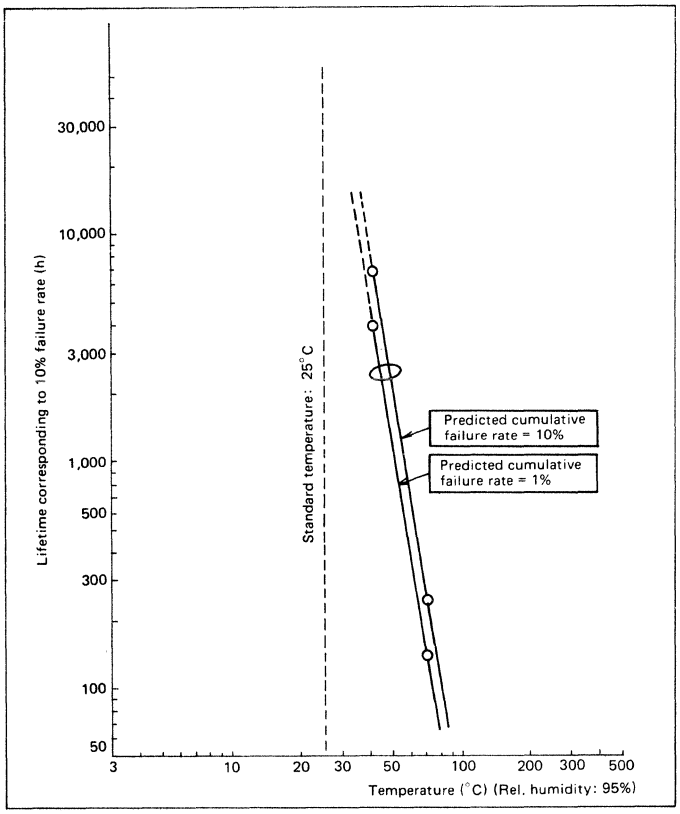


Fig. 5.4 Dependence of lifetime on temperature under high humidity conditions

Polarizer

Figure 5.5 shows the changes in contrast that occur when the liquid crystal display is left exposed to high temperature, and Fig. 5.6 shows the similar changes that occur when high temperature is accompanied by high humidity. The results indicate that the polarizer can easily withstand high temperature, but is apt to experience deterioration of polarization under high humidity. At 40°C and 90% RH there are essentially no problems, but contrast is lost after 400 hours at 50°C and 95% RH, and after 30 hours at 70°C and 95% RH. When a liquid crystal display is used in any device, it is therefore necessary to protect the polarizer against moisture.

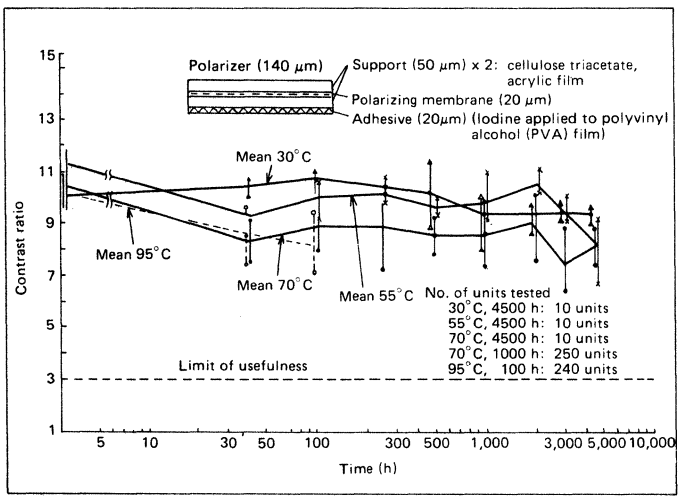


Fig. 5.5 Lifetime of polarizer at high temperature

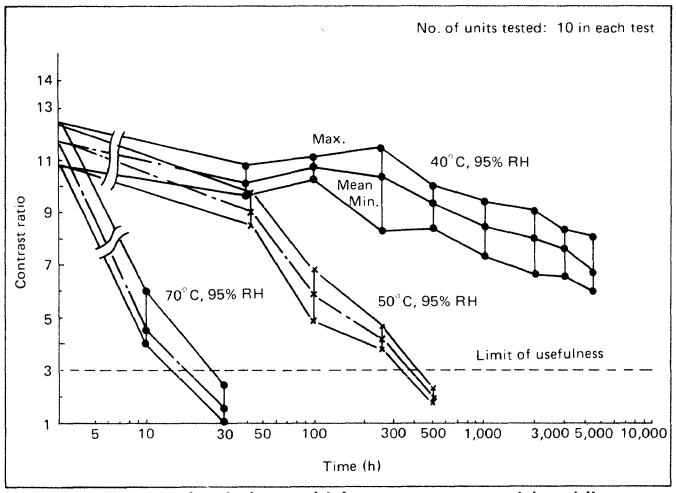


Fig. 5.6 Lifetime of polarizer at high temperature and humidity

Ultraviolet irradiation

The results of ultraviolet irradiation tests by exposure to sunlight and to a carbon arc lamp are shown in Fig. 5.7, as increase in current drain with irradiation time. In both tests the increase is slight; the display shows extremely stable properties. Increased current drain shortens the life of the battery and leads to a rise in V_{th1}, but the initial current drain of Hitachi liquid crystal displays is so small that it can be increased several-fold without significant effect.

Figure 5.8 compares the spectra of the carbon arc light and sunlight. The ultraviolet component, which would be expected to harm the liquid crystal, is stronger in the carbon arc light.

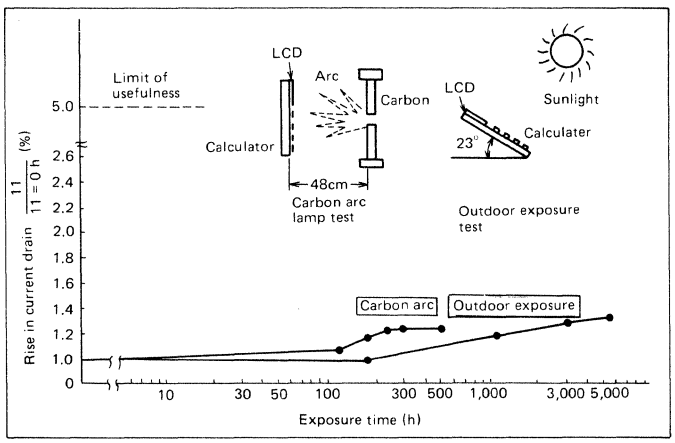


Fig. 5.7 Carbon arc lamp and outdoor exposure tests

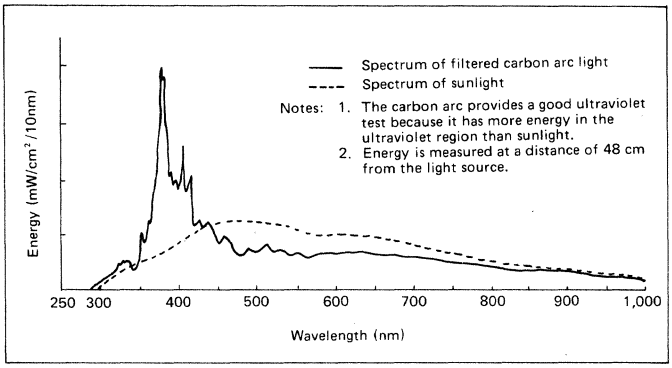
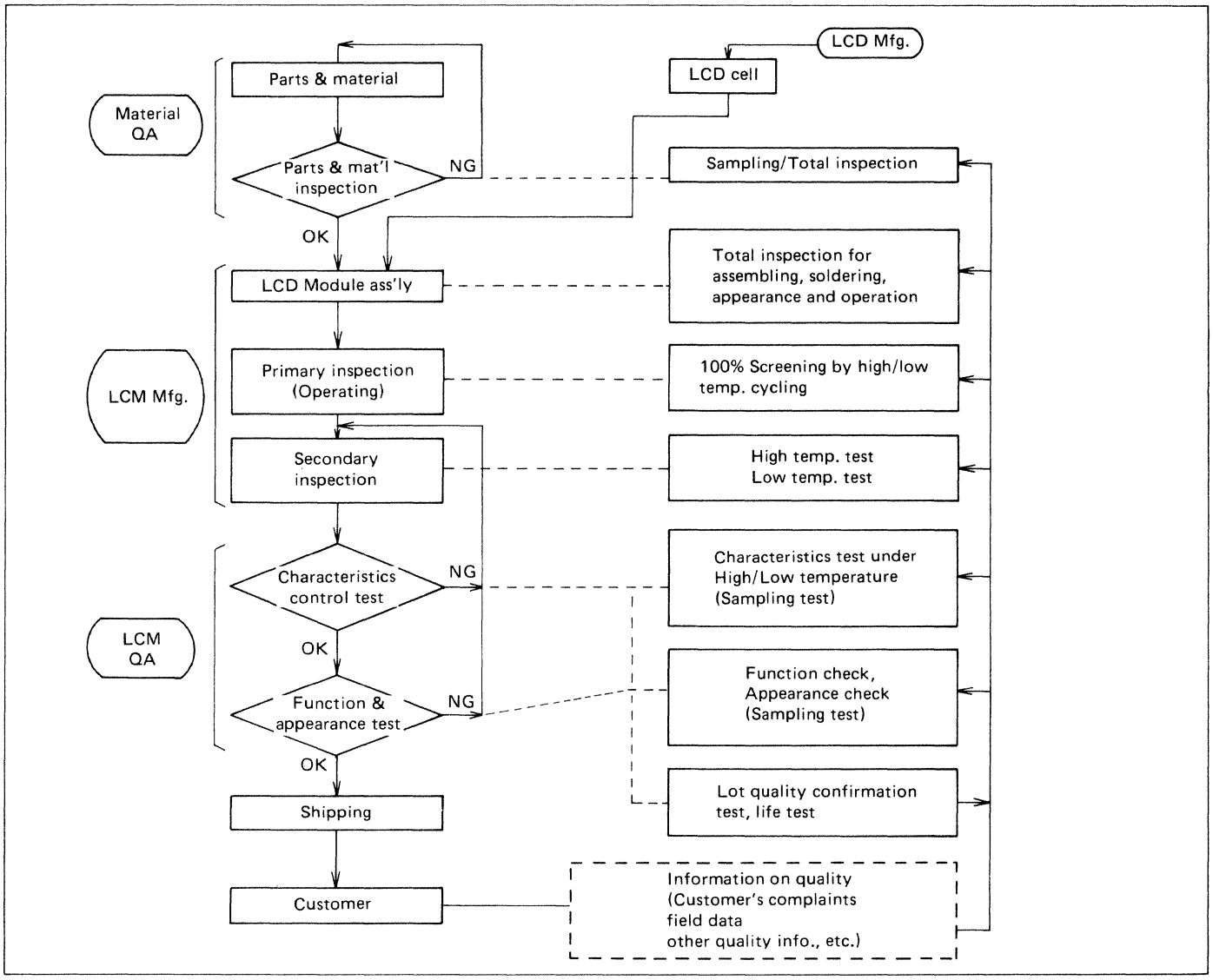


Fig. 5.8 The spectra of the carbon arc light and sunlight

RELIABILITY OF LCM

Quality assurance system flow chart for LCM



BASIC LCM USAGE 3

HOW TO USE LCD MODULE

1. Liquid crystal display

LCD is composed of glass and polarizer. The following precautions are recommended when handling LCD's.

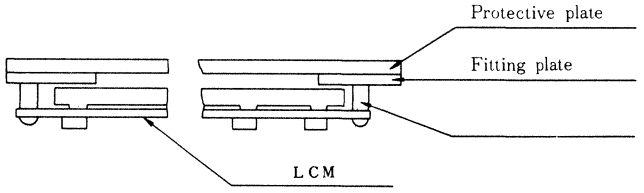
(1) Please keep the temperature within the specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.
(2) Do not touch, push or rub the exposed polarizers with any hard object.
(3) PETROLEUM BENZIN is recommended for cleaning the surface of LCD's. Front/rear polarizers and reflectors are made of organic substances and will be damaged by such chemicals as acetone, toluene, ethanol and isopropyl alcohol.
(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.
(5) Wipe off water drops immediately. Contact with water over a long period of time may cause deformation or color fading.
(6) Avoid contact with oils.
(7) Condensation on the surface and contact terminals will damage, stain or dirty the polarizers. After products are tested at low temperatures they must be warmed up in a container before coming in contact with room temperature air.
(8) Do not place anything on the display area to avoid leaving marks on.
(9) Do not touch the display area with bare hands. This will stain the display area and degradate insulation between terminals. (Some cosmetics are detrimental to the polarizers).
(10) As glass is fragile, it may crack or chip during handling especially on the edges. Please avoid dropping or jarring.

2. Liquid crystal display module

Installing LCD module

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Follow these rules when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the LCD.



(2) When assembling the LCM into other equipment, the spacer to be fit between the LCM and the fitting plate should have enough height to avoid causing any stress to the module surface. Refer to the individual specifications for measurements. The measurement tolerance should be ±0.1 mm.

Precaution for handling LCD modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

(1) Do not alter, modify or change the shape of the tab on the metal frame.
(2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.
(3) Do not damage or modify the pattern wiring on the printed circuit board.
(4) Absolutely do not modify the zebra rubber strip (conductive rubber) or touch it with another object.
(5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.
(6) Do not drop, bend or twist LCM.

Electro-static discharge control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handling LCM.
(2) Before removing LCM from its packing case or incorporating it into a set, be sure that the module and your body have the same electric potential.
(3) When soldering the terminal of LCM, make certain that the AC power source for the soldering iron does not leak.
(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced by sparks coming from the commutator of the motor.
(5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.
(6) To reduce the generation of static electricity, be careful that the air in the work is not too dry. (A relative humidity of 50% ~ 60% is recommended.)

Precaution for soldering to the LCM

(1) Observe the following when soldering lead wire, connector cable, etc., to the LCM.
- Soldering iron temperature: 280°C ±10°C
- Soldering time: 3 ~ 4 sec.
- Solder: eutectic solder

If soldering flux is used, be sure to remove any remaining flux after finishing the soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When removing the electroluminescent panel from the PC board, be sure that the solder has completely melted first. If you try to pull the components apart before the solder is completely melted, the soldered pad on the PC board could be damaged.

3. Precautions for operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (V_0)
Adjust V_0 to show the best contrast.

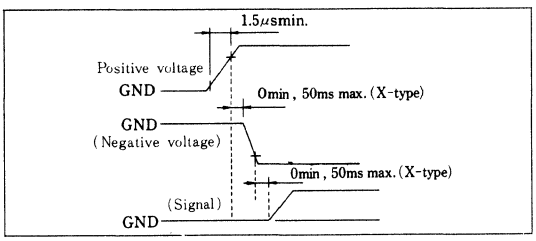
(2) Driving an LCD in the voltage above the limit shortens its life.

(3) Response time is greatly delayed at temperatures below the operating temperature range. The display area becomes dark blue at temperatures above this range. However, this does not mean the LCD will be damaged. It will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit.
Therefore, it must be used under the relative condition of 40°C, 50% RH.

(6) When turning on power, input each signal after the positive/negative voltage becomes stable.



4. Storage

When storing LCDs as spares for some years, the following precautions are necessary:

(1) Store them in a sealed polyethylene bag. If properly sealed, there's no need for dessicant.

(2) Store them in a dark place; do not expose to sunlight or fluorescent light. Keep the temperature between 0°C and 35°C.

(3) The polarizer surface should not come in contact with any other object. (We advise you to store them in the container in which they were shipped).

(4) Environmental conditions

(a) Humidity
Observe the following conditions both in storage and in operation.
(i) Number of dots: Under 128 x 240
Ta < 40°C . . . 95% RH or less
Ta ≧ 40°C . . . Below maximum absolute humidity of 40°C 95% RH
(ii) Number of dots: 128 x 240 or over
Ta < 40°C . . . . 85% RH or less
Ta ≧ 40°C . . . . Below maximum absolute humidity of 40°C 85% RH

(b) Exposure to high humidity and temperature
(i) Do not leave them for more than 168 hrs. at 40°C 95% RH (When number of dots is 128 x 240 or over . . . . . 40°C 85% RH)
(ii) Do not leave them for more than 168 hrs. at 60°C.
(iii) As for X-type LCM, should not be left for more than 48 hrs. at –20°C.

Note: Ta = ambient temperature

5. How to handle the electroluminescent panel

(For transflective type LCM)

Selection of electroluminescent panel

(1) The electroluminescent panel is inserted between the liquid crystal display (LCD) and printed circuit board of a liquid crystal module (LCM). Therefore, it is essential to select an electroluminescent panel that is insulated on both the PC board side and the LCD side.
It is especially important to make sure that the electroluminescent panel is insulated on the PC board side, as the wiring of the through-hole portion is exposed.

(2) It is recommended that you use an electroluminescent panel with insulated ends as shown in the diagram below. If the ends of the electroluminescent panel are exposed, a short might occur with the liquid crystal module, resulting in damage to the module.

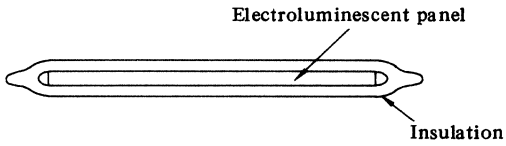


Fig. 1 Cross section of electroluminescent panel (Model not drawn to scale)

(3) Select the electroluminescent panel that is the right size for each liquid crystal module. There is a recommended size for each standard Hitachi liquid crystal module. Information on panel sizes is available upon request.

Installing the electroluminescent panel

(1) A cross section of the LCM construction is illustrated in Fig. 2. The gaps at either end through which the electroluminescent panel is inserted are made of conductive rubber (interconnectors).
When inserting the electroluminescent panel, be especially careful not to move the conductive rubber. Do not push the rubber with the edge of the panel, as the rubber might be moved from its proper position. This could damage the connection between the LCD and the PC board, resulting in a display failure.

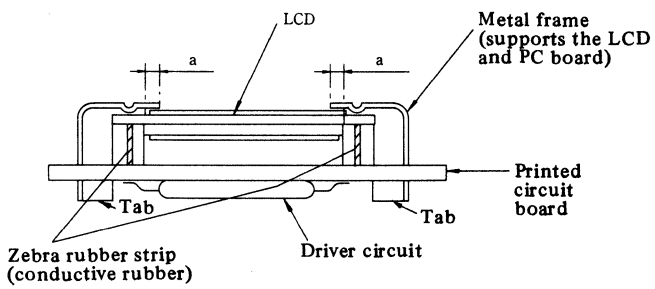


Fig. 2 Cross section of a liquid crystal module

(2) Since high voltage is applied to the feeder terminal of the electroluminescent panel, be careful to install the panel such that the feeder terminal does not touch the front panel or the PC board. (The voltage is high in comparison with that applied to the C-MOS drive circuit used in the liquid crystal module.)
If the feeder terminal is touching the front panel or PC board when the lighting voltage is applied to the panel, the drive circuit and LCD will fail. There is also the possibility that other circuits (e.g. controller on the set side, MPU, etc.) may be adversely affected by the passage of voltage through the interface.

(3) Install the electroluminescent panel such that the luminous part coincides with the window frame (effective display area) of the LCM front panel.
The distance between the window frame of the front panel and the conductive rubber (dimension a in Fig. 2) varies with each liquid crystal module, but an average is about 2.0 mm.
When determining the position where the electroluminescent panel is to be installed, be careful not to move the conductive rubber with the panel.

(4) Observe the following standards when soldering the electroluminescent panel to the PC boards.
- Soldering iron temperature: 280°C ±10°C
- Soldering time: 3 ~ 4 sec.
- Solder: eutectic solder

If soldering flux is used, be sure to remove any remaining flux after finishing the soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(5) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering gun.

(6) When removing the electroluminescent panel from the PC board, be sure that the solder has completely melted first. If you try to pull the components apart before the solder is completely melted, the soldered pad on the PC board could be damaged.

5.3 Drive circuit of electroluminescent panel

(1) The luminance and life time of an electroluminescent panel vary depending on the drive voltage and frequency. Therefore, it is recommended that you select the drive circuit suggested by the electroluminescent panel manufacturer. Using the recommended product will assure the optimum brightness and working life of the electroluminescent panel.

FORMATION OF LIQUID CRYSTAL

No.	Liquid crystal	Description	Oral dosage (LD50 Value)	Inhalation toxicity	Skin irritations	Allergic reaction	Malformation possibility	Data source
1.	HFK-110	Mixture of Schiff base type RO ⬡ CH=N ⬡ R'	1.0 ml/kg (mouse)	No effects (mouse)	No effects (mouse)	Did not occur (mouse)		Hitachi
2.	LIXON 6302	Mixture of Schiff base type RO ⬡ CH=N ⬡ R'	<10 ml/kg (mouse)		Scabs and blood clots noted but disappeared after dosing was stopped (rabbit)			Chisso Corpo-ration
3.	LIXON 7102	Mixture of Schiff base type RO ⬡ CH=N ⬡ CN	<10 ml/kg (mouse)		Small blood clots noted but disappeared after dosing was stopped (rabbit)			Chisso Corpo-ration
4.	GR-2	Mixture of biphenyl type R ⬡ = ⬡ CN	<10 ml/kg (mouse)		Small blood clots and scabs noted but dis-appeared after dosing was stopped (rabbit)			Chisso Corpo-ration
5.	R0-TN-100	Mixture of ester type R ⬡ C00 ⬡ CN	<8.0 g/kg (mouse)					Hoffman
6.	R0-TN-200	Mixture of Schiff base type R ⬡ CH=N ⬡ CN	~1.1 g/kg (mouse)	(being planned by Hoffman)	No effects (guinea pig)	Did not occur (guinea pig)		Hoffman
7.	K15	C_5H_9 ⬡ - ⬡ CN	4.1 g/kg (rat)		No effects (rabbit)			BDH
8.	K21	C_7H_{15} ⬡ - ⬡ CN	1.6 g/kg (rat)		Small red spots of one rabbit out of 10	Note 3		BDH
9.	M15	C_5H_9O ⬡ - ⬡ CN	<1.6 g/kg (rat)		No effects (rabbit)			BDH
10.	M21	$C_7H_{15}O$ ⬡ - ⬡ CN	<20.0 g/kg (rat)		No effects (rabbit)			BDH
11.	M24	$C_8H_{17}O$ ⬡ - ⬡ CN	16.0 g/kg (rat)		No effects (rabbit)			BDH
12.	E7	Mixture of biphenyl type R ⬡ - ⬡ CN					No effects	BDH
13.	TN-132	Mixture of pyrimidine type R ⬡(N,N) - ⬡ -CN	1.2 g/kg (rat, mouse)					

Note 1) Animals in parentheses were used in the experiment. **Note** 2) No data for blank columns. **Note** 3) Eye irritations are being checked. No effects have been noted.

Safety

(1) It is recommended to crush damaged or unnecessary LCD's into pieces and wash off liquid crystal by using solvents such as acetone and ethanol, which should be burned up later.

(2) If any liquid leaks out of a damaged glass cell and comes in contact with your hands, please wash it off well with soap and water.

(3) Concerning LC material (reference)—mice, rats, rabbits, and guinea pigs are normally used as human substitutes in experiments using liquid crystal. The data sheet indicates that liquid crystal is not harmful to humans even if mistakenly eaten.

EXPLANATIONS ON ABOVE DATA CHART

The data sheet shows what can happen to animals that are fed typical liquid crystal materials. Among the samples, Nos. 1 to 4 and No. 6 are rarely used for display purposes and should be used only as a reference.

The column for oral dosage (LD50 value) shows the effects on animals that have mistakenly eaten liquid crystal.

LD50 is the value that can kill 50% of those being dosed by grams per 1 kg weight. The value differs for each animal and can not be directly applied to humans. This data can be used as a guide.

Values in this data, 1.6 g ~ 20 g/kg, are equivalent to the LD50 value of organic solvents (ethyl alcohol and acetone) generally used.

Using the smallest data sheet value (No. 8, 9 LD50 = 1.6 g/kg) and assuming that a child weighing 10 kg at the liquid crystal, the result will be:

LD50 1.6 g/kg (rat) 16 g/10 kg (child)

This means that eating 16 g at one time will kill 50% of the children eating the liquid crystal.

The quantity of liquid crystal contained in one LCD (LR238-C, 260 x 130mm) is about 200 mg. When the LCD breaks down, most of it adheres to the glass surface because of surface tension and does not flow out.

Possibility of flowing out into the mouth when the broken LCD is put in the mouth is less than 1/100 of the total quantity. this means that the amount entering the mouth is: 200 mg max. x 1/100 = 2 mg.

The 2 mg is about 1/8000 of 16 g/10 kg of LD50 (dose for child) and has no effect on humans.

No problems if the liquid crystal remaining on hands or fingers is washed off with soap.

GRAPHICS MODULE DETAIL DATA 4

LIQUID CRYSTAL GRAPHIC DISPLAY MODULE

A wide range of graphic modules are available, and are all characterized by low power consumption, high contrast and wide viewing angle.

- Attachable controller LSI
  (HD61830 • HD61830B)
- Control circuit board
  (CB1020R • CB1026R • CB1030R • CB1040R • CB1055R • CB1056R • CB1057R • CB1058R)

COLOR TONE

In order to improve the contrast and viewing angle of the large graphics panels, a new L.C.D. effect has been introduced called X-type. It offers a 50% improvement in display visibility compared to the traditional grey L.C.D. The display concerned has an X or S suffix after the part number (e.g., LM240S, LM225X).

Please note, however, that the display has a different background color from the normal grey-type. The S-type display has a yellowish grey background coloration while the X-type has a yellow-green background. Also there will be a slight color change with temperature, thereby limiting the temperature range of the device. (Please refer to the data sheets.)

CONTROLLER LSI HD61830·HD61830B

■ **Graphic LCD Module Controller LSI**

■ **Applied types: (1) H2525 · LM021 · LM212 · LM200 · LM211XB · LM221XB · LM215XB (HD61830 is to be used)**
(2) LM224XB · LM225X (HD61830B is to be used)
(3) LM213B · LM213XB · LM238XB (HD61830 is built-in)

The HD61830 is a dot matrix liquid crystal graphic display controller LSI that stores the display data sent from an 8-bit microcomputer in the external RAM to generate dot matrix liquid crystal driving signals.

It is possible to select the graphic mode in which the 1-bit data of the external RAM corresponds to the ON/OFF state of 1 dot on liquid crystal display and the character mode in which characters are displayed by storing character codes in the external RAM and developing them into the dot patterns with the internal character generator ROM. Both modes can be provided for various applications.

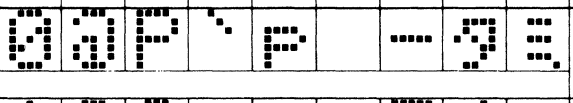
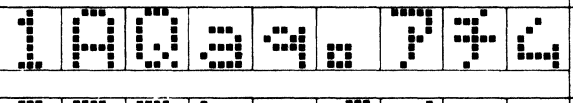
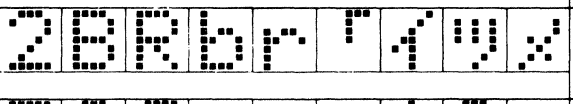
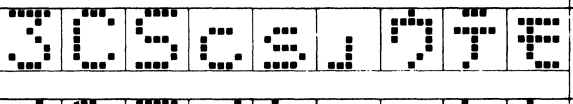
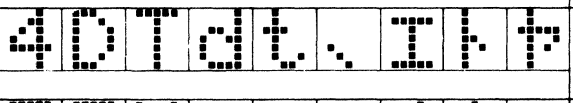
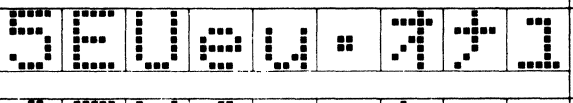
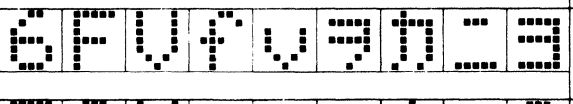
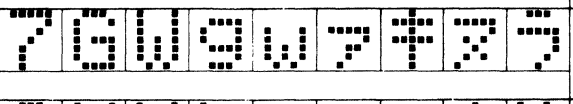
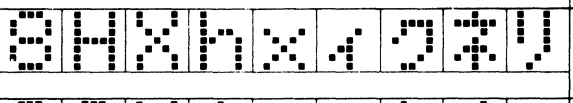
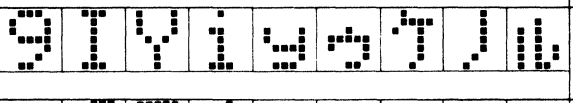
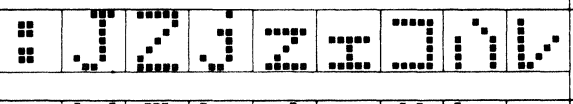
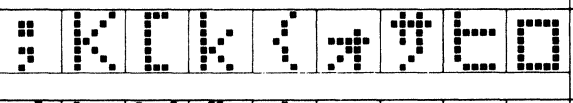
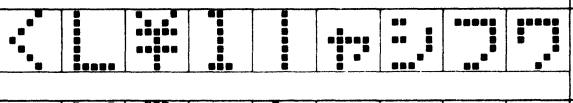
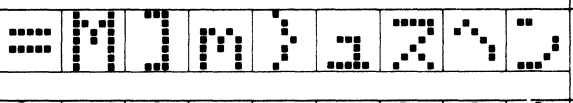
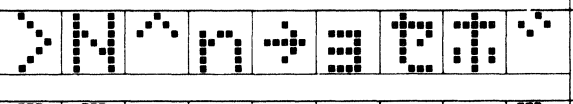
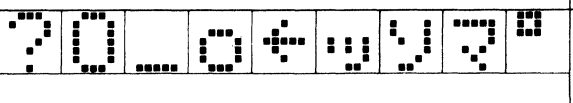
The HD61830 is produced in the CMOS process. Thus, the combination with a CMOS microcomputer can accomplish a liquid crystal display device with lower power consumption.

■ **Specifications:**

- Display control capacity
- Graphic mode – 512k dots (2^{16} bytes)
- Character mode – 4096 characters (2^{12} characters)
- Internal character generator ROM – 7360 bits
  Character fonts 5 x 7 dots 160 types
  Character fonts 5 x 10 dots 32 types
  Total 192 types
  (Can be extended to 4k byte max.)
- Interfaceable to 8-bit MPU
- Display duty (Can be selected by a program)
  Static to 1/128 duty selectable
- Various instruction functions
  Scroll, cursor ON/OFF, blink, character blink, screen clear, bit manipulation
- Display method – A or B types selectable
  (A or B: waveform)
- Internal oscillator (with external resistor and capacitor)
- Low power consumption
- Power supply: Single +5V
- CMOS process
- 60-pin flat plastic package

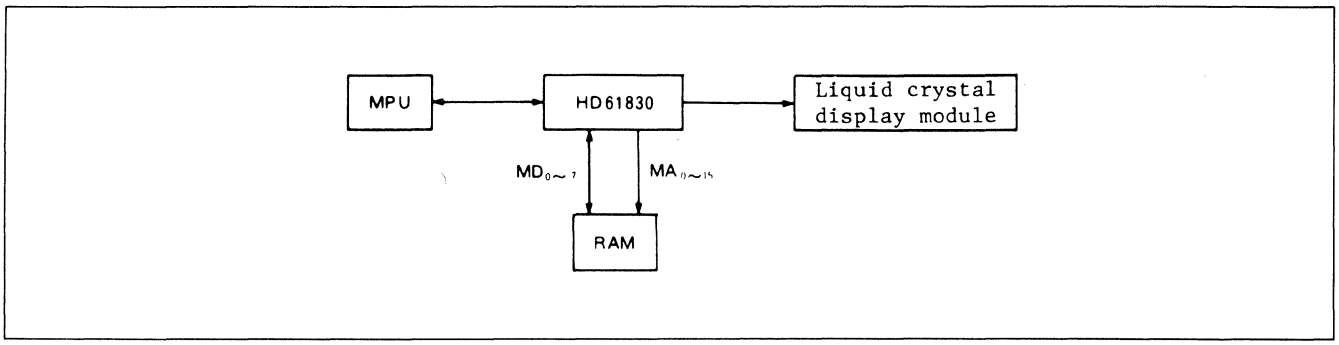
(Notes) HD61830B is a high speed and memory low power consumption version of HD61830. The difference between HD61830 and HD61830B are as follows:
(1) Internal oscillation circuit
(2) Additional memory control signals
(3) Connection method in master/slave mode
If you need detailed information, please refer to "Hitachi MOS LSI data book LCD driver LSI" or contact following office.
Hitachi America Ltd. Semiconductor & Integrated Circuit Divsion
2210 O'Toole Avenue, San Jose, CA 95131, Telephone: (408) 435-8300

Internal Character Generator Patterns and Character Codes

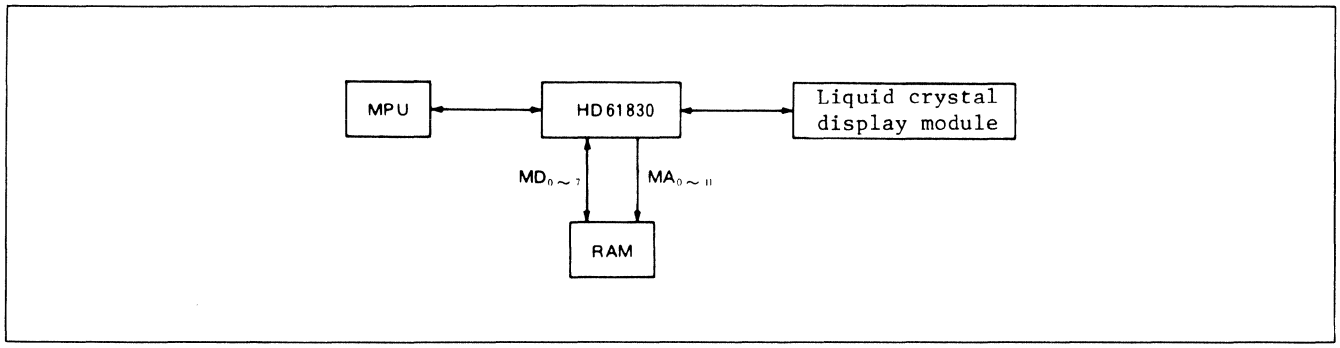
Lower 4 bit \ Higher 4 bit	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000												
××××0001												
××××0010												
××××0011												
××××0100												
××××0101												
××××0110												
××××0111												
××××1000												
××××1001												
××××1010												
××××1011												
××××1100												
××××1101												
××××1110												
××××1111												

EXAMPLE OF CONFIGURATION

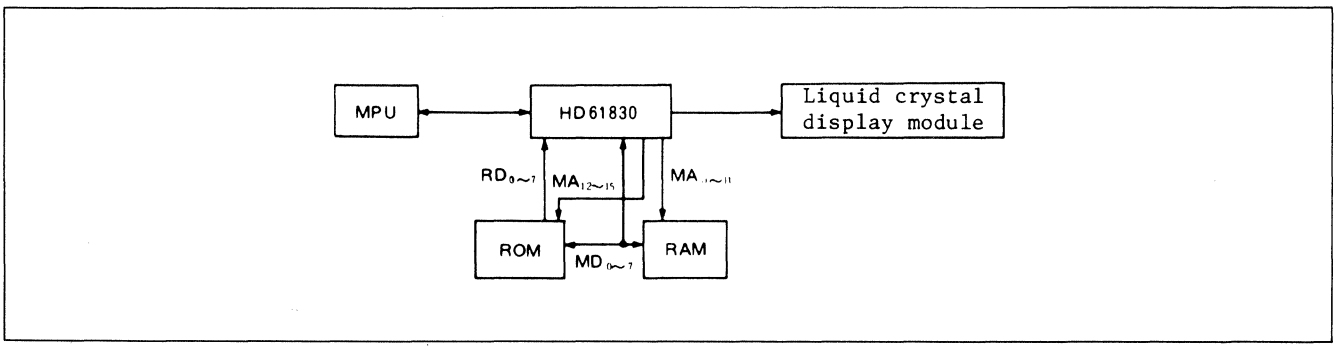
- Graphic Mode



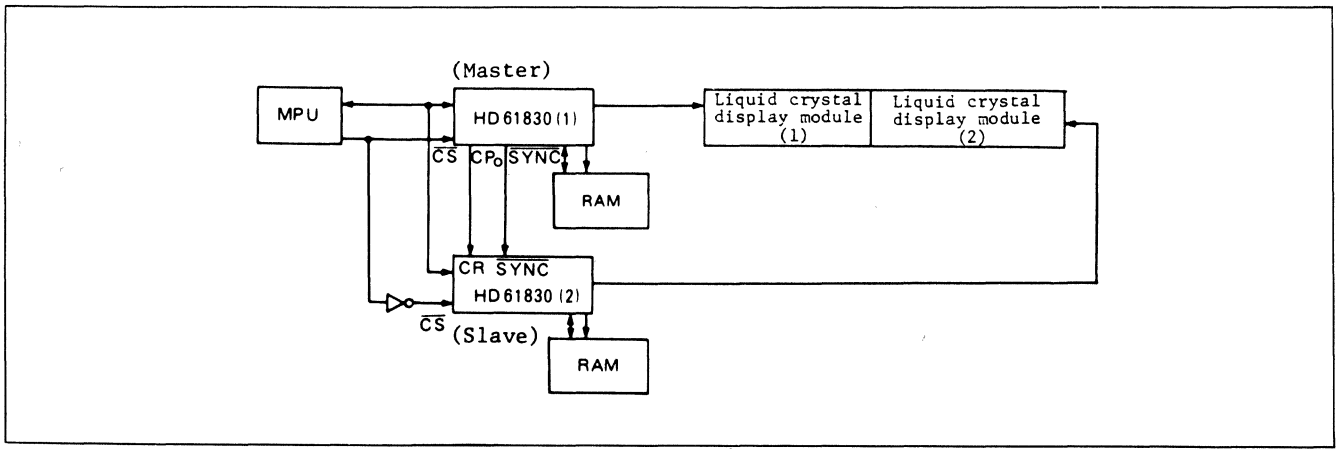
- Character Mode (1) (Internal Character Generator)



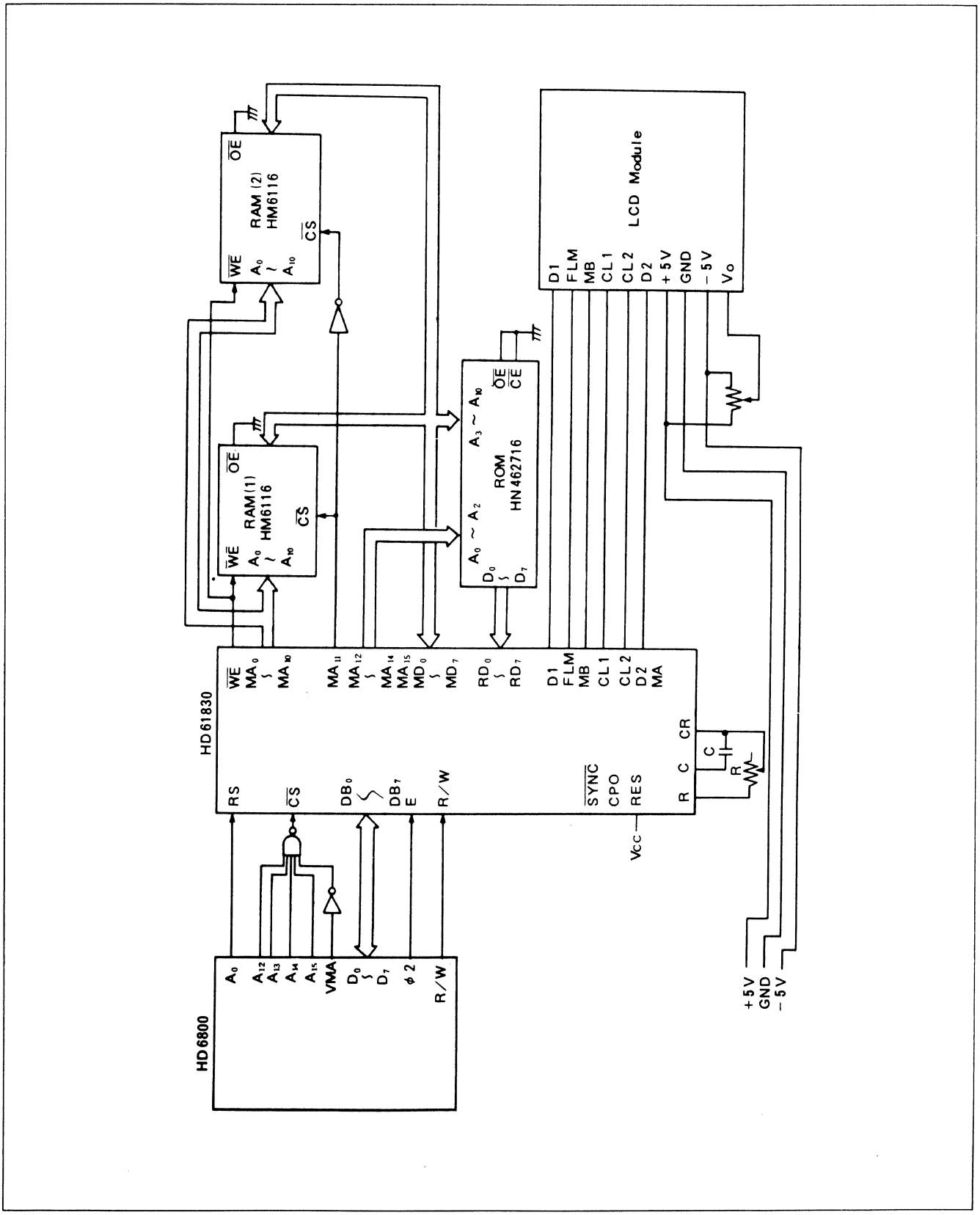
- Character Mode (2) (External Character Generator)



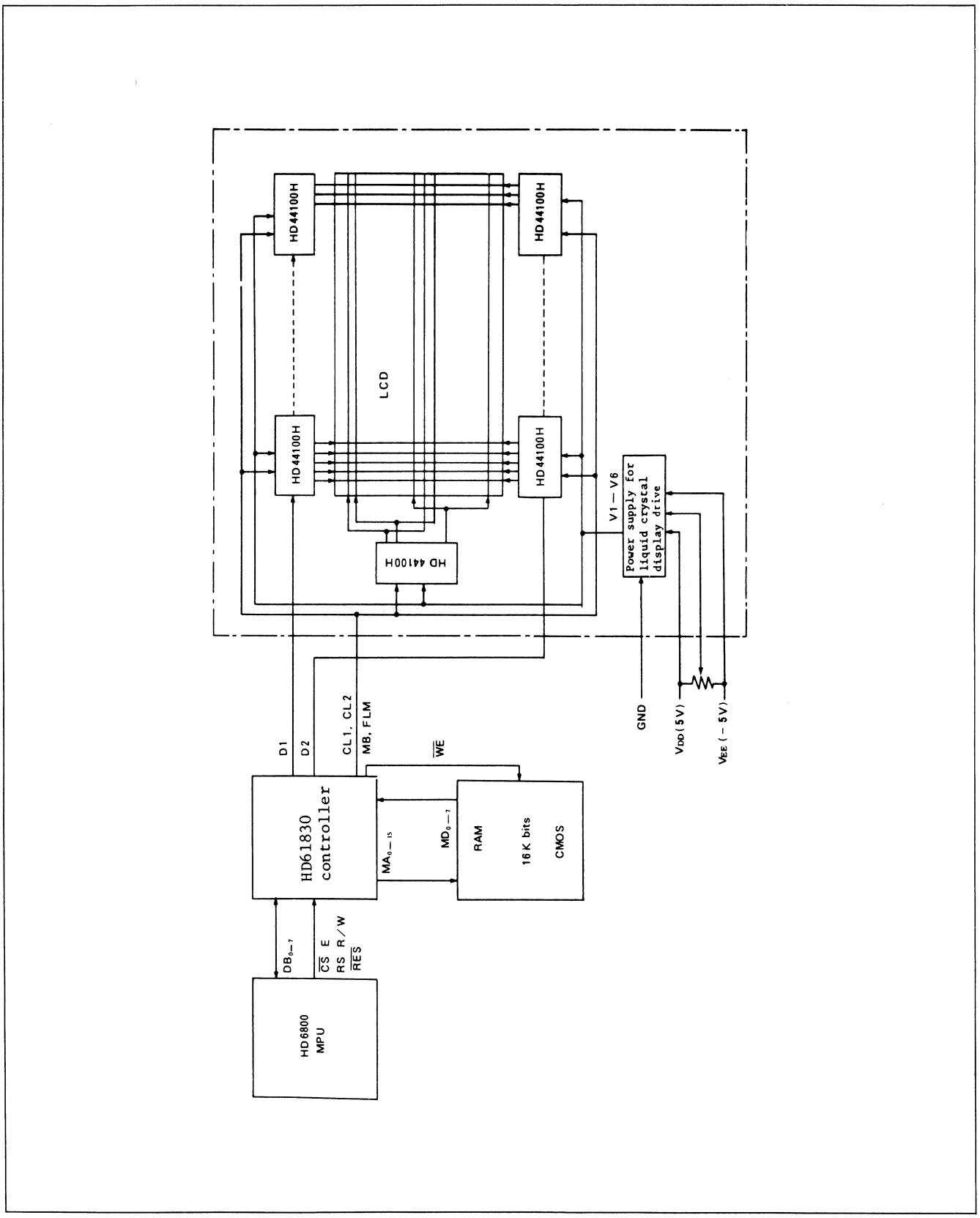
- Parallel Operation



APPLICATION (Character Mode, External CG, Character Font 8x8)



APPLICATION (Graphic Mode)



CONTROL CIRCUIT BOARD

CB1020R, CB1026R, CB1030R, CB1040R
CB1055R, CB1056R, CB1057R, CB1058R

- **BUILT-IN CONTROLLER LSI HD61830/HD61830B**
- **Applied models: Control circuit board can be applied to following models.**
  CB1020R(1)/CB1055R(2): LM021 H2525 LM200 LM258X
  CB1026R(1)/CB1056R(2): LM021 H2525 LM200 LM211XB LM212 LM221XB
  CB1030R(1)/CB1057R(2): LM215XB
  CB1040R(1)/CB1058R(2): LM225X

CB1020R, CB1026R, CB1030R and CB1040R (mounted with controller LSI HD61830 or HD61830B and a socket for the refresh memory) are control circuit boards for graphic display modules.

They allow direct connection to the MPU's bus line. The HD61830 controls signal generation and data conversion required for a liquid crystal display (LCD) moudle. This simplifies the graphic display system. These control circuit boards operate in graphic and character mode. In graphic mode, refresh memory contents are displayed on the LCD to allow display of figures, graphs and pictures.

In character mode, the 8-bit parallel code for each character is converted to the corresponding dot pattern by the character generator in the control circuit boards and displayed on the LCD. The built-in character generator converts 192 characters including 160 characters and 32 special pattern characters. An additional character generator for character patterns required by the user can also be mounted.

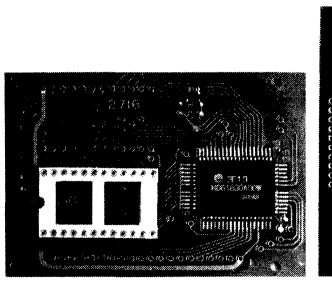
Item \ Model	CB1020R	CB1026R
Controller (Built-in)	HD61830 x 1 pc.	HD61830 x 1 pc.
Refresh RAM	Up to 2k bytes	Up to 4k bytes
External ROM	Up to 2k bytes	Up to 4k bytes
Dimensions (mm)	78 x 53	82 x 76
LCD module to be driven	LM021, H2525 LM200, LM258X	LM021, H2525, LM200, LM211XB, LM212, LM258X

Items \ Model	CB1030R	CB1040R
Controller (Built-in)	HD61830 x 2 pcs.	HD61830B x 2 pcs.
Refresh RAM	Up to 8k bytes	Up to 16k bytes
External ROM	Up to 4k bytes	Up to 8k bytes
Dimensions (mm)	125 x 85	150 x 140
LCD module to be driven	LM215XB	LM225X

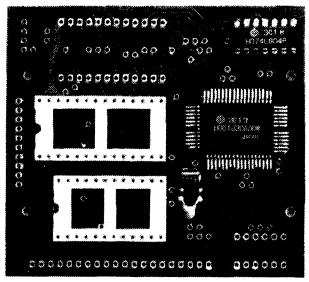
Notes

(1) Since IC socket is used in these models for the purpose of circuit experiment, etc., do not use them where any vibration or shock might occur. Otherwise the connection between IC socket and IC will be loose which leads to poor connection.
Please consult us when using control circuit board to these products.

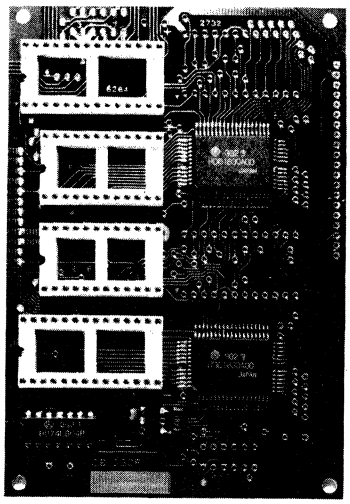
(2) These are models without IC socket.



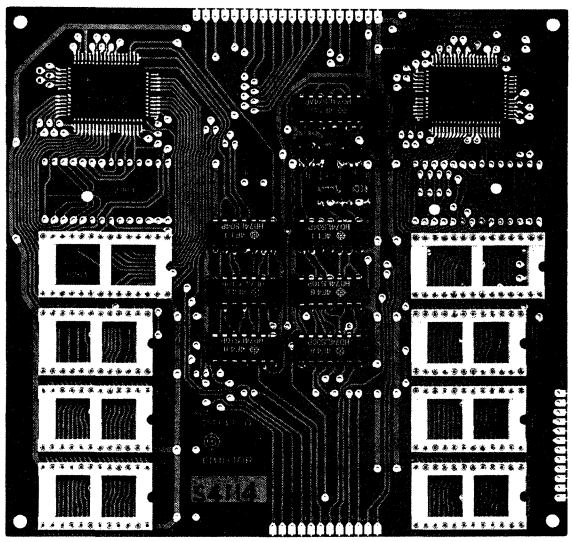
CB1020R



CB1026R



CB1030R



CB1040R

SECTION 4

H2525

- 239dot (W) x 20 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size	220W x 53H x 15T (max.) mm
Effective display area	163W x 17H mm
Number of dots	239W x 20H dot
Dot size	0.55W x 0.55H mm
Dot pitch	0.65W x 0.65H mm
Weight	about 100g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V, V_{EE}=−5.0V±0.25V

Input "high" voltage (V_{iH})	0.7 x V_{DD}V min.
Input "low" voltage (V_{iL})	0.3 x V_{DD}V max.
Clock frequency (f_{CL2})	210 kHz min.
	300 kHz typ.
	390 kHz max.
Power supply current (I_{DD})	3mA typ.
(I_{EE})	1 mA typ.

(D_1, D_2 = GND, f_{CL2} = 300 kHz)

Power supply for LCD drive (Recommended) (V_O-V_{EE})

Duty = 1/20

Ta= 0°C	5.5V typ.
Ta=25°C	5.0V typ.
Ta=50°C	4.0V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM single indicates the begining of each display cycle.
2	M	H/L	Control signal for a.c. driving
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D1	H/L	Serial row data
5	CL2	H→L	Clock signal for shifting the serial data
6	V_{DD}(+5V)	–	Power supply for logic circuit
7	V_{SS}(GND)	–	Ground
8	V_{EE}(−5V)	–	Power supply for LC driving
9	V_O	–	Operating voltage for LC driving
10	NC	–	No connection

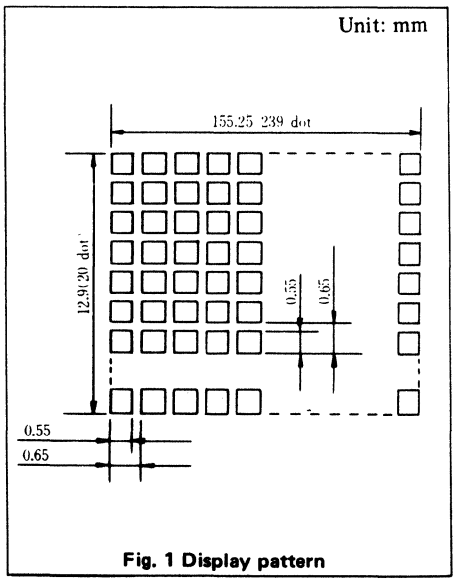


Fig. 1 Display pattern

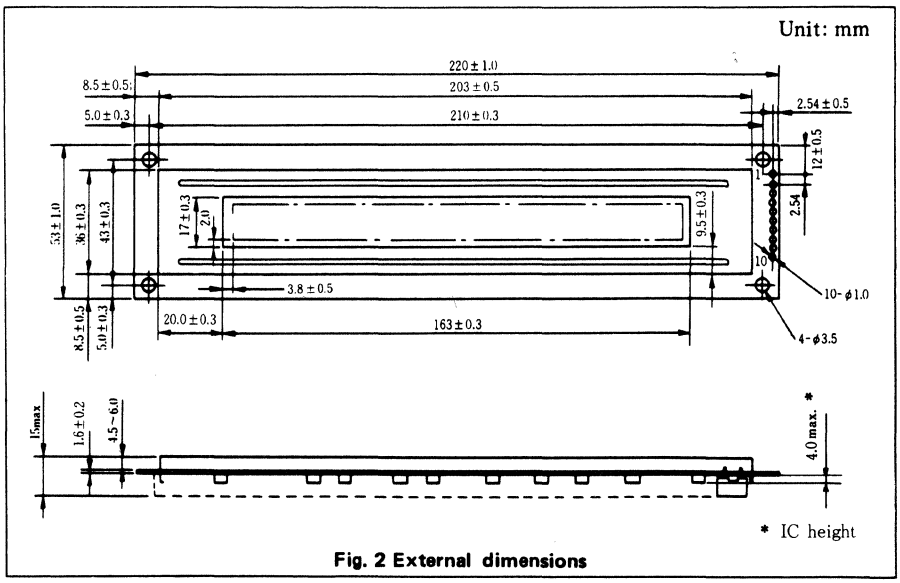


Fig. 2 External dimensions

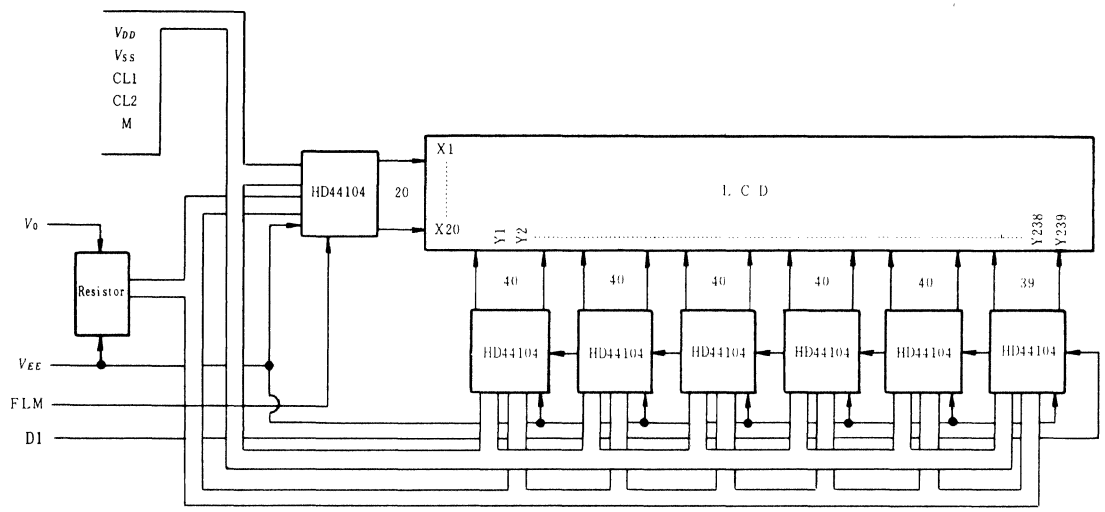
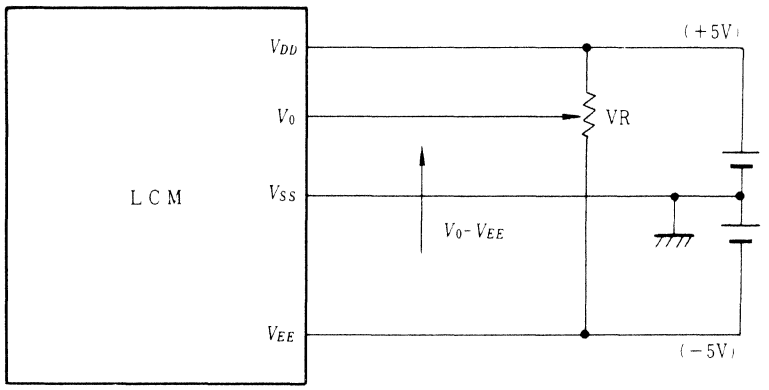


Fig. 3 Block diagram



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	500	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	–	–	ns
Clock pulse width (Low level)	t_{CWL}	800	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	300	–	–	ns
FLM set up time	t_{FSU}	300	–	–	ns
M delay time	t_{DM}	−1000	0	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	300	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CL1 may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ± 2 Hz or 60 Hz ± 2 Hz) to prevent LCD flicker.

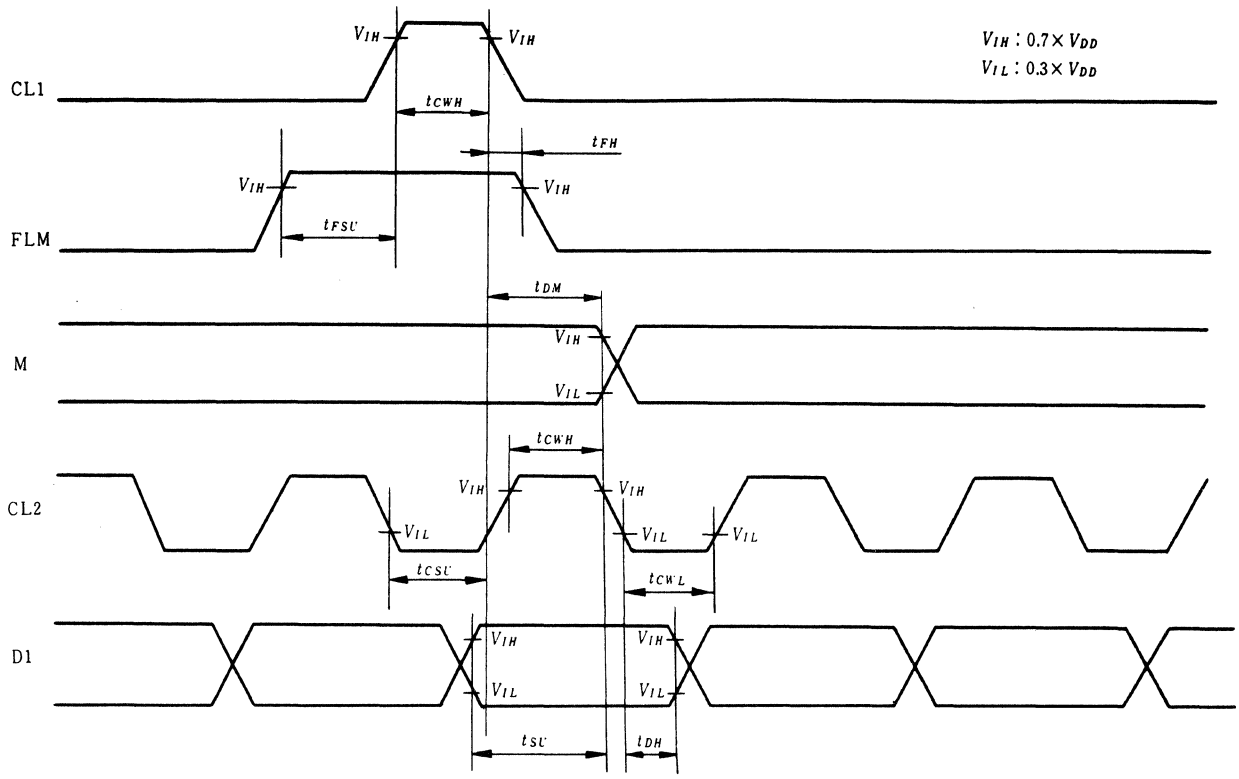


Fig. 5 Interface timing (data write)

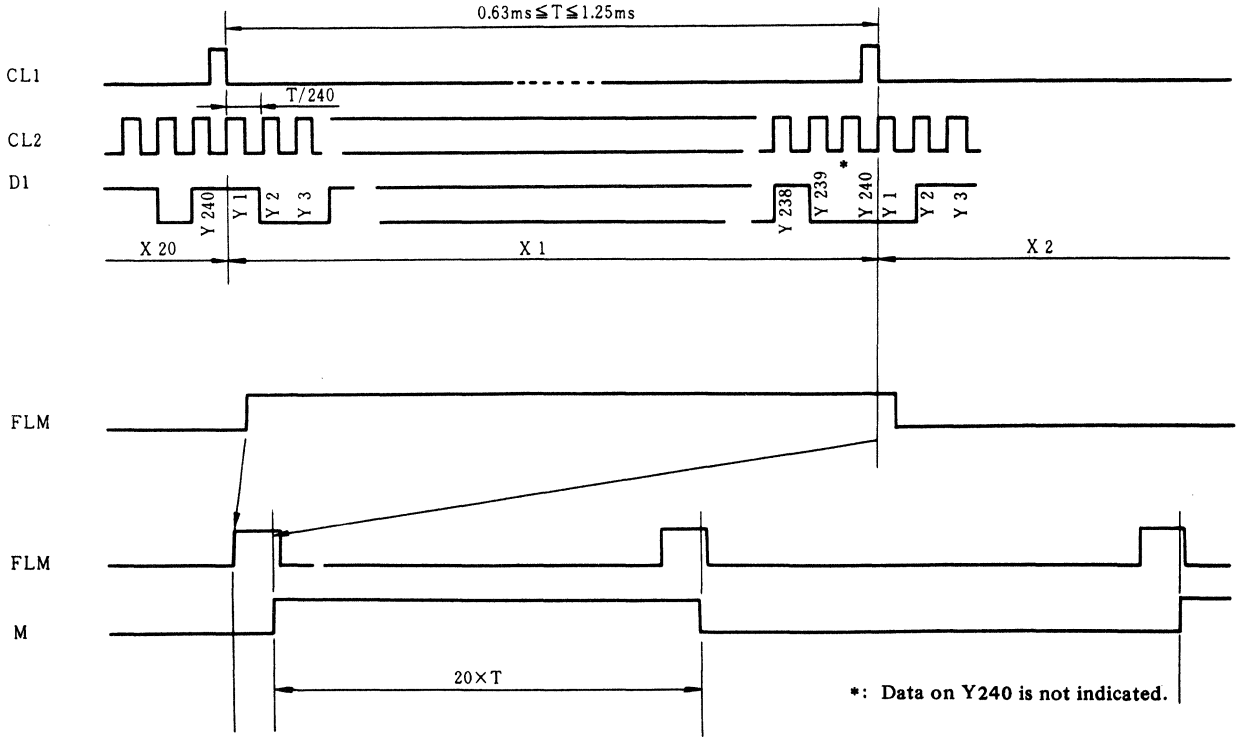


Fig. 6 Interface timing (data read)

LM021

- 479 dot (W) x 24 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 290W x 60H x 13T (max.) mm
Effective display area . . . . . 245W x 19H mm
Number of dots . . . . . 479W x 24H dot
Dot size . . . . . 0.43W x 0.55H mm
Dot pitch . . . . . 0.48W x 0.6H mm
Weight . . . . . about 150g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$) . . .	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V, V_{EE}=−5.0V±0.25V
Input "high" voltage (V_{iH}) . . . . . 0.7 x V_{DD}V min.
Input "low" voltage (V_{iL}) . . . . . 0.3 x V_{DD}V max.
Clock frequency (f_{CL2}) . . . . . 230 kHz min.
350 kHz typ.
460 kHz max.
Power supply current (I_{DD}) . . . . . 4mA typ.
(I_{EE}) . . . . . 2mA typ.
(D_1, D_2=GND, f_{CL2}= 350 kHz)
Power supply for LCD drive (Recommended) (V_O-V_{EE})
Duty = 1/24
Ta= 0°C . . . . . 6.0 V typ.
Ta=25°C . . . . . 5.4 V typ.
Ta=50°C . . . . . 4.4 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM signal indicates the beginning of each display cycle.
2	M	H/L	Control signal for a.c. driving.
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D1	H/L	Serial row data
5	D2	H/L	Serial row data
6	CL2	H→L	Clock signal for shifting the serial data
7	V_{DD}(+5V)	–	Power supply for logic circuit
8	V_{SS}(GND)	–	Ground
9	V_{EE}(−5V)	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

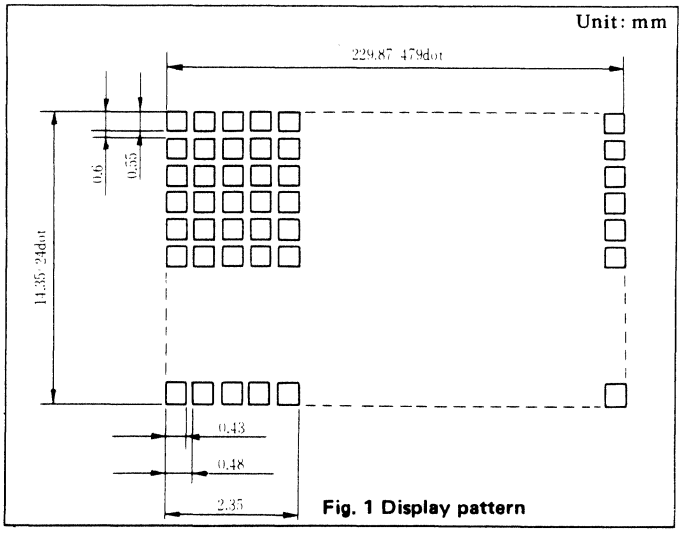


Fig. 1 Display pattern

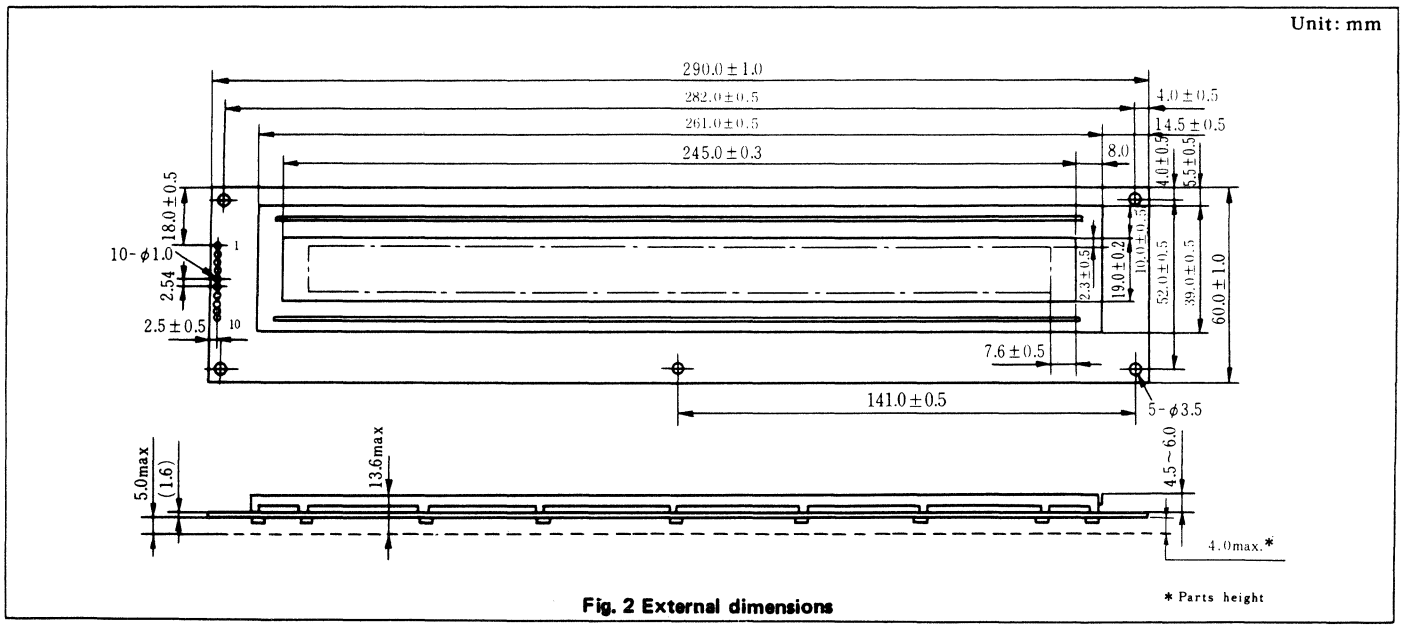
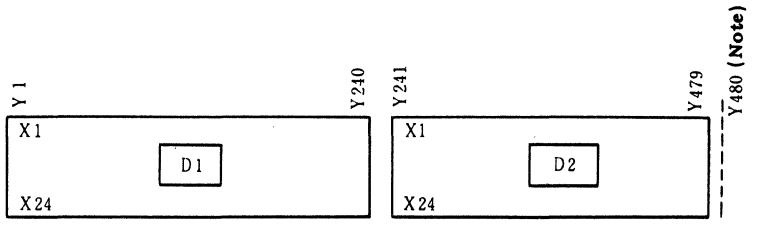


Fig. 2 External dimensions

SECTION 4



Note: Y480 is a dummy line.

Fig. 3 Correspondence of display with data

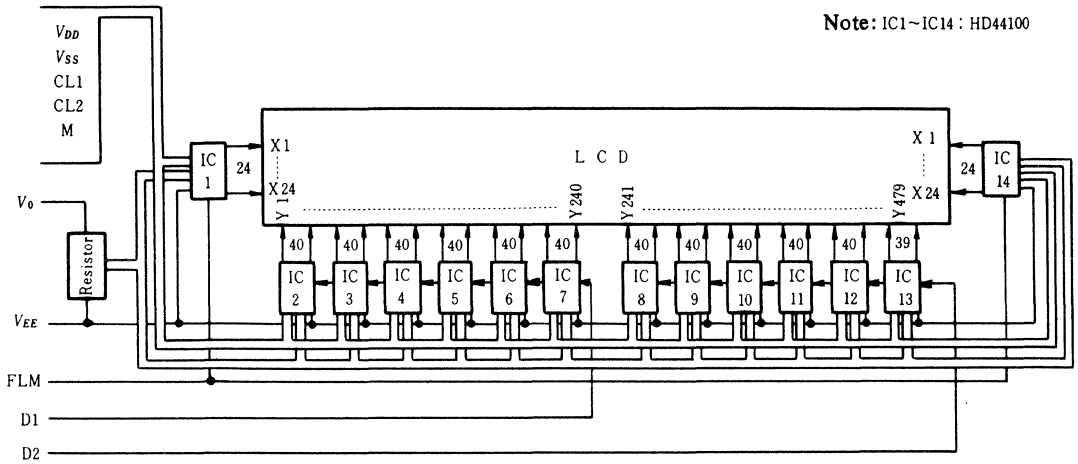
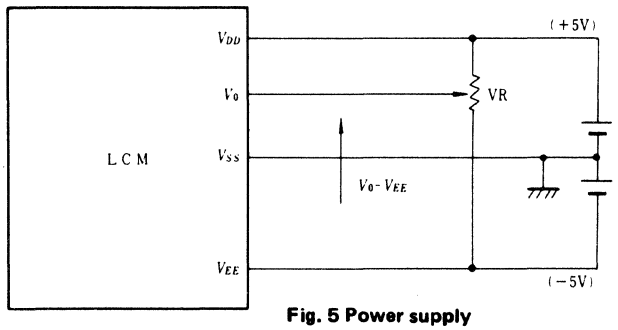


Fig. 4 Block diagram



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	500	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	–	–	ns
Clock pulse width (Low level)	t_{CWL}	800	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	300	–	–	ns
FLM set up time	t_{FSU}	300	–	–	ns
M delay time	t_{DM}	−1000	0	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	300	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CL1 may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

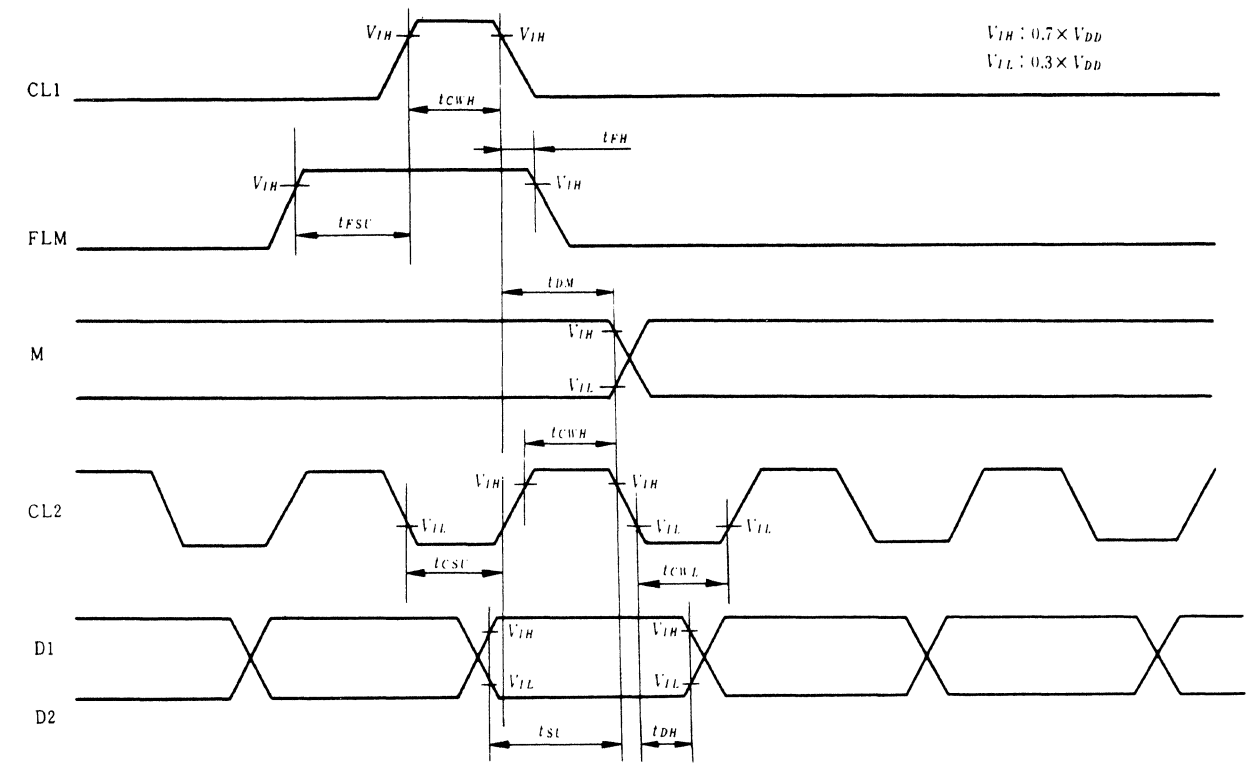


Fig. 6 Interface timing (data write)

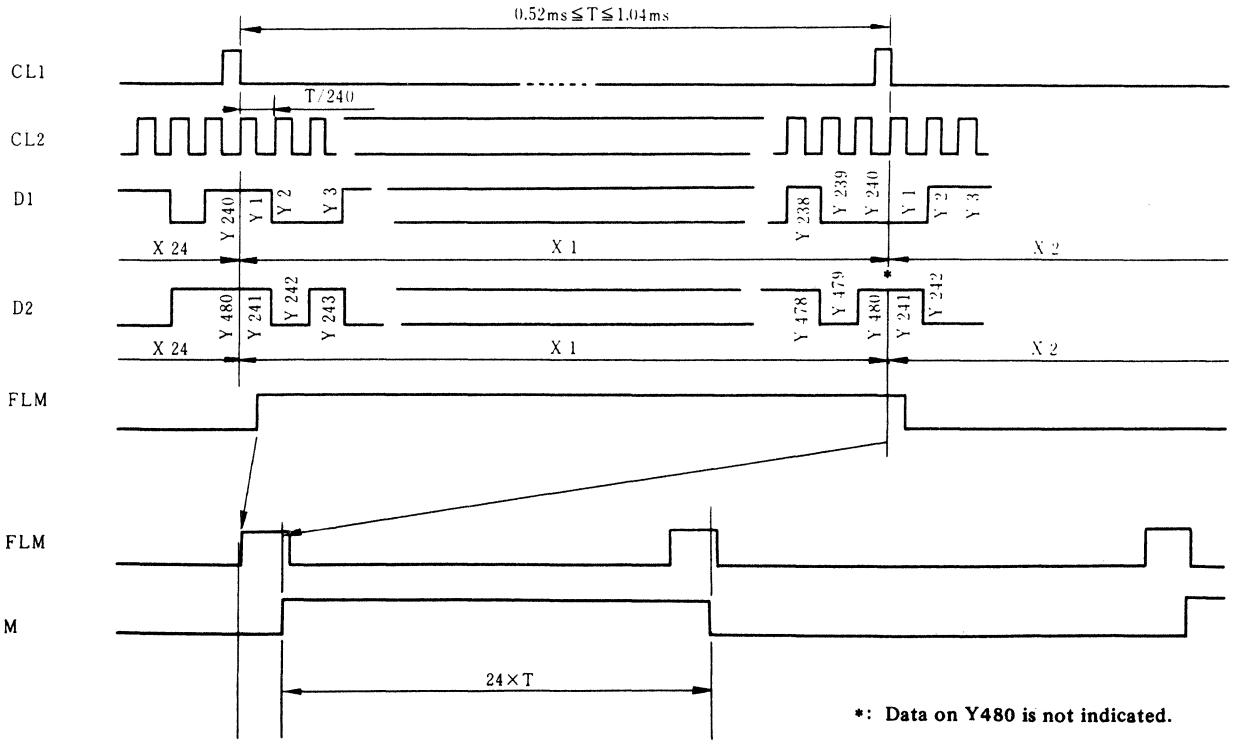


Fig. 7 Interface timing (data read)

LM212

- 640 dot(W) x 48 dot(H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see section 6).

OPTICAL DATA . . . . . .See page 15.

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 63H x 13.8T (max.) mm
Effective display area	241W x 25H mm
Number of dots	640W x 48H dot
Dot size	0.32W x 0.38H mm
Dot pitch	0.37W x 0.43H mm
Weight	about 175 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	15.0 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0V ±0.25V, V_{EE} = −9V (V_{EE} is internally generated)

Input "high" voltage (Vi_H)	3.5	V_{DD}V
Input "low" voltage (Vi_L)	0	1.5 V max.
Clock frequency (f_{CL2})	1,075 kHz min.	
	1,152 kHz typ.	
	1,228 kHz max.	
Power supply current (I_{DD})	10 mA typ.	

(D_1, D_2 = GND, f_{CL2} = 1,152 kHz)

Power supply for LCD drive (Recommended) ($V_{DD} - V_O$)
Duty = 1/48

Ta = 0°C	12.5 V typ.
Ta = 25°C	11.0 V typ.
Ta = 40°C	9.7 V typ.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (left half)
2	FLM	H	The FLM signal indicates the beginning of each display cycle
3	M	H/L	Control signal for AC driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data (right half)
7	V_{DD}(+5V)	–	Power supply for logic circuit
8	V_{SS}	–	Ground
9	V_{EE}(−10V)	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

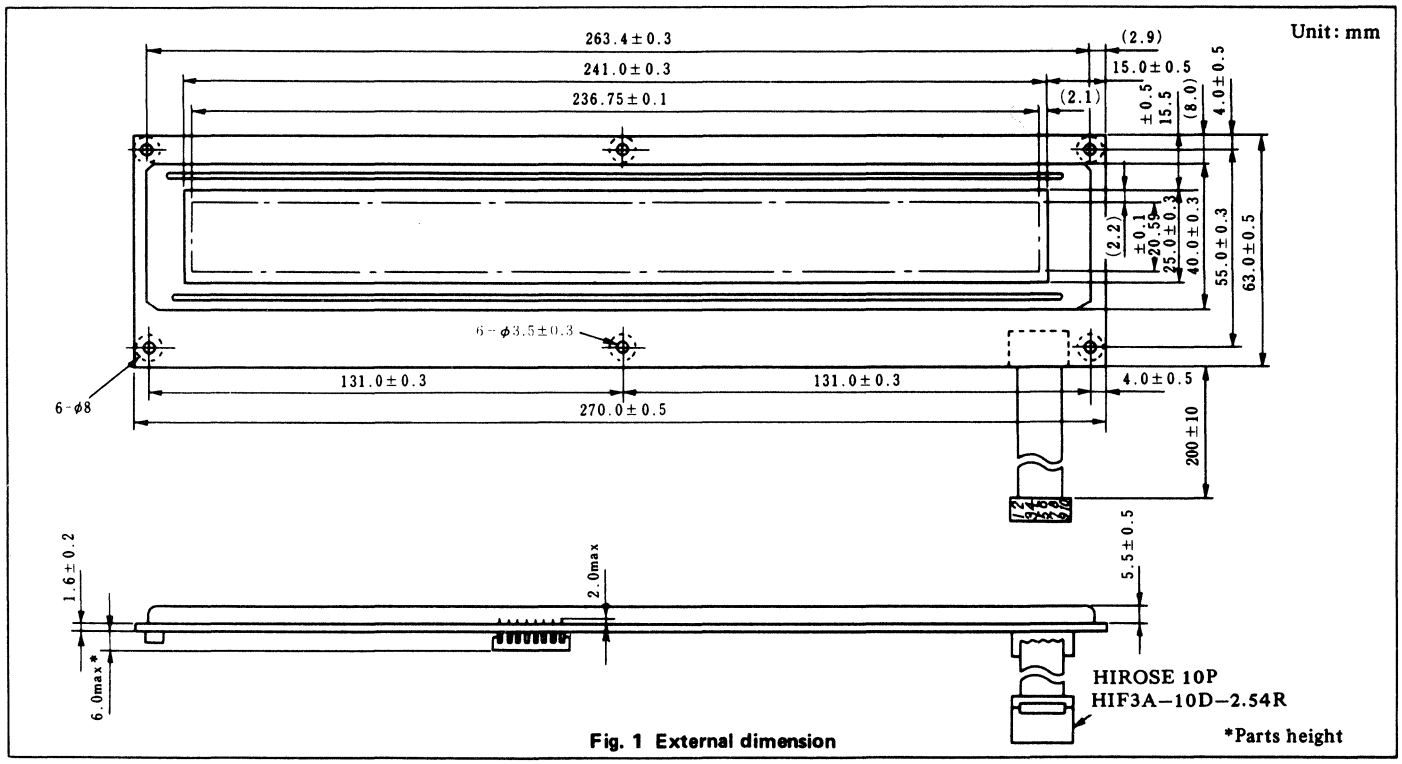


Fig. 1 External dimension

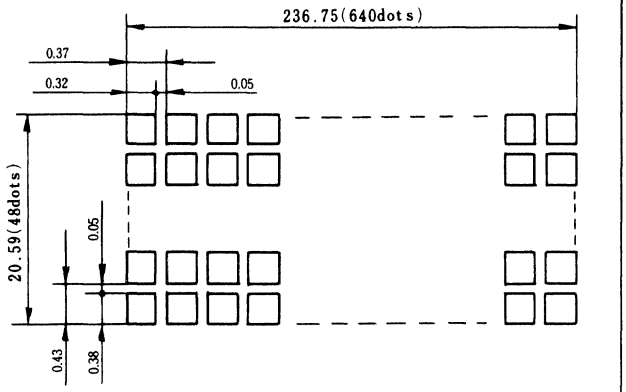


Fig. 2 Display pattern

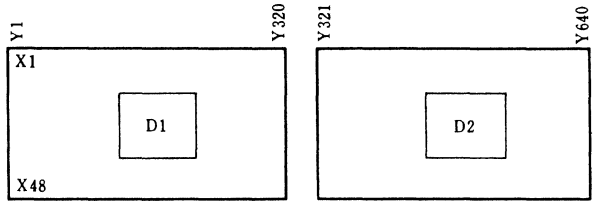
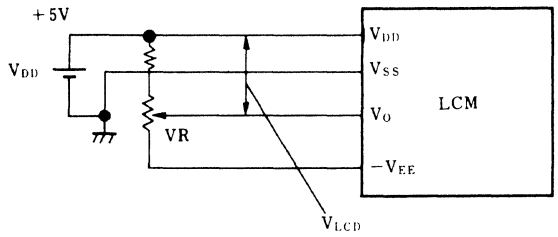
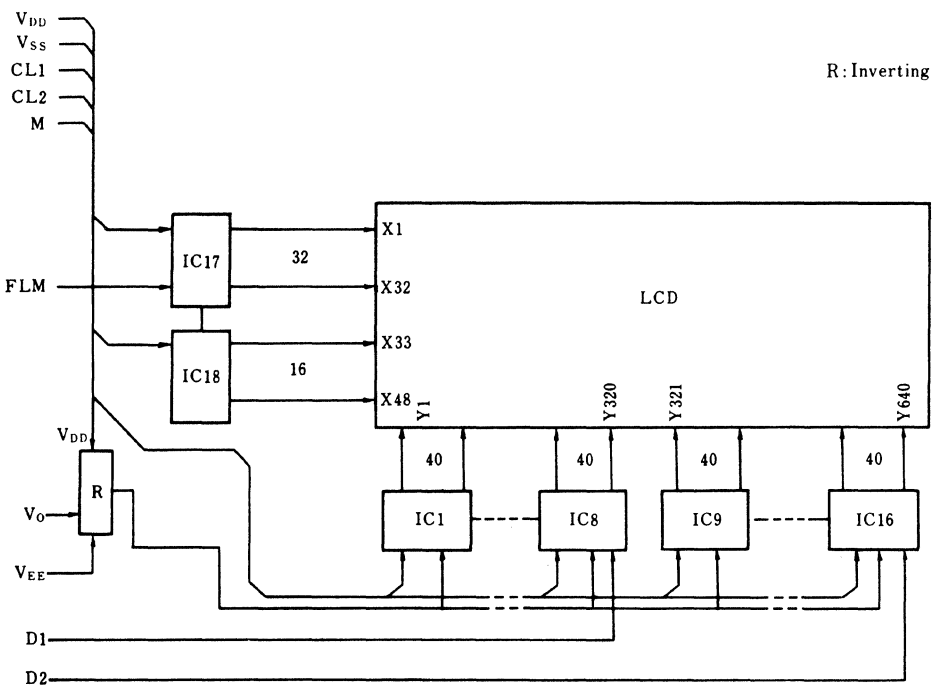


Fig. 3 Correspondence of display with data



R: 30 ~ 50kΩ
VR: 20kΩ
V_{LCD}: Operating voltage for LC driving

Fig. 4 Power supply



R: Inverting voltage regulator

Fig. 5 Block diagram

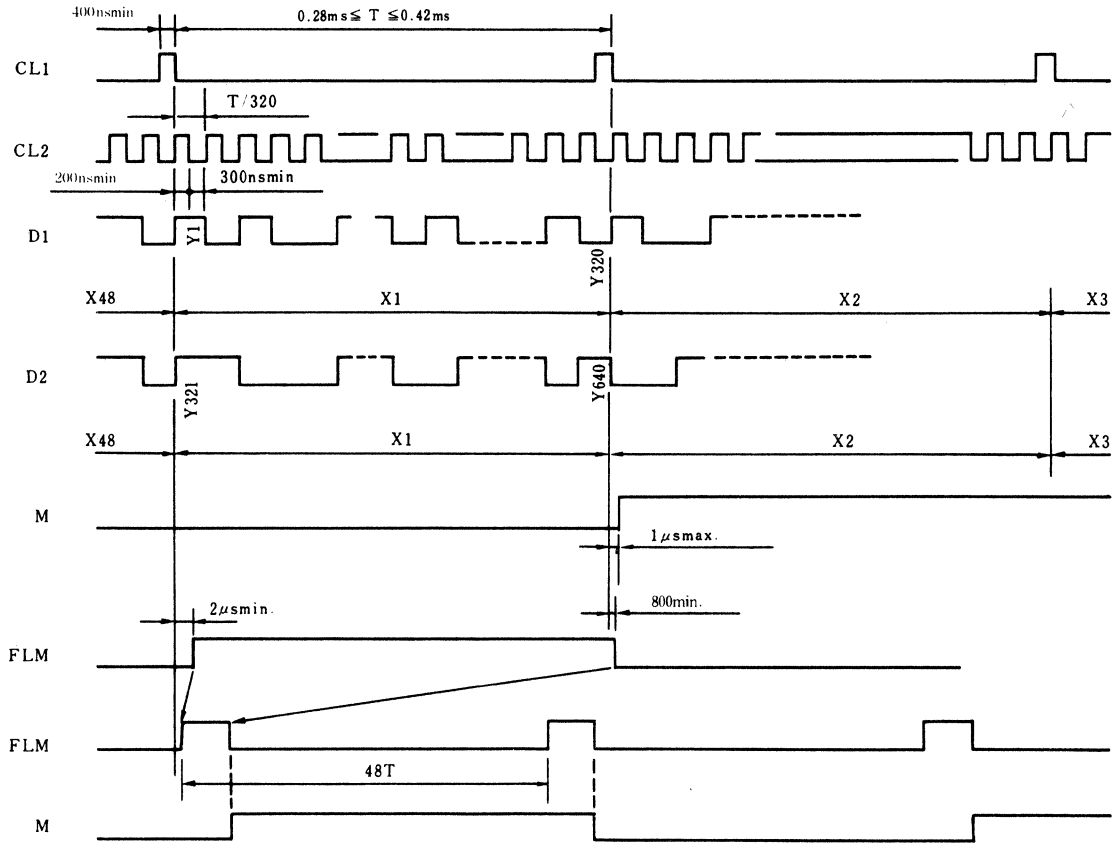


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	1228	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	200	–	–	ns
Clock pulse width (Low level)	t_{CWL}	300	–	–	ns
Clock set up time	t_{CSU}	540	–	–	ns
Data set up time	t_{SU}	40	–	–	ns
FLM set up time	t_{FSU}	100	–	–	ns
M delay time	t_{DM}	–	–	+1000	ns (Note 2)
FLM hold time	t_{FH}	800	–	–	ns
Data hold time	t_{DH}	400	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CLI may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

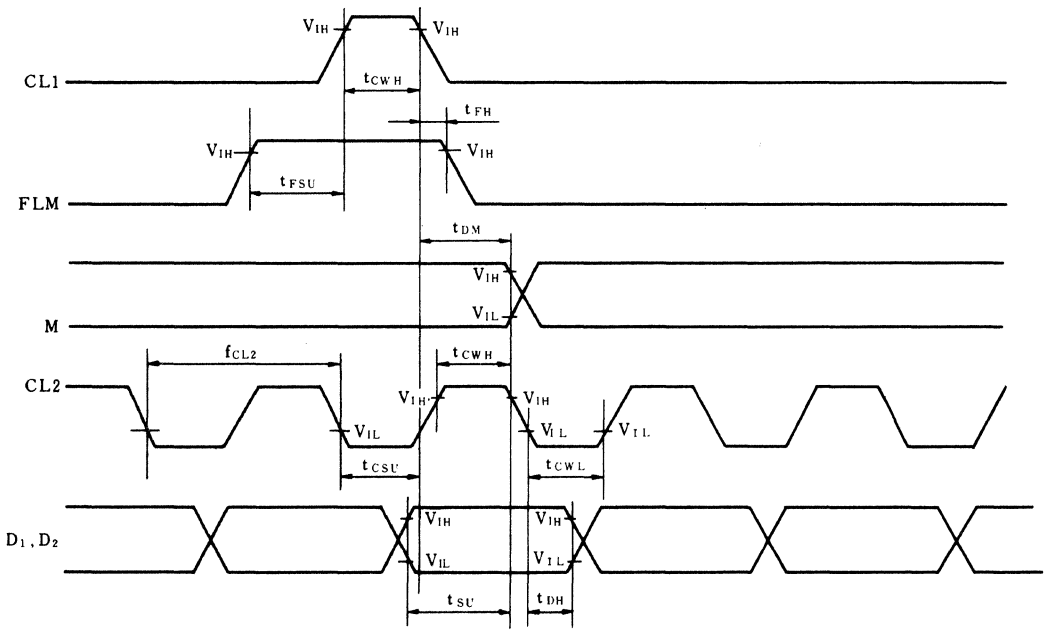


Fig. 7 Interface timing

LM200

- 240 dot (W) x 64 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 180W x 75H x 13.8T (max.) mm
Effective display area . . . . . 132W x 39H mm
Number of dots . . . . . 240W x 64H dot
Dot size . . . . . 0.48W x 0.48H mm
Dot pitch . . . . . 0.53W x 0.53H mm
Weight . . . . . about 150g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$) . . .	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V, V_{EE}=−5.0V±0.25V
Input "high" voltage (V_{iH}) . . . . . 0.7 x V_{DD}V min.
Input "low" voltage (V_{iL}) . . . . . 0.3 x V_{DD}Vmax.
Clock frequency (f_{CL2}) . . . . . 390 kHz min.
460 kHz typ.
520 kHz max.
Power supply current (I_{DD}) . . . . . 5mA typ.
(D_1, D_2=GND, f_{CL2}=460 kHz)
Power supply for LCD drive (Recommended) (V_O-V_{EE})
Duty = 1/32
Ta= 0°C . . . . . 8.1 V typ.
Ta=25°C . . . . . 7.4 V typ.
Ta=50°C . . . . . 6.5 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data
2	FLM	H	The FLM signal indicates the beginning of each display cycle.
3	M	H/L	Control signal for a.c. driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers.
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data
7	V_{DD}(+5V)		Power supply for logic circuit
8	V_{SS}(GND)	–	Ground
9	V_{EE}(−5V)	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

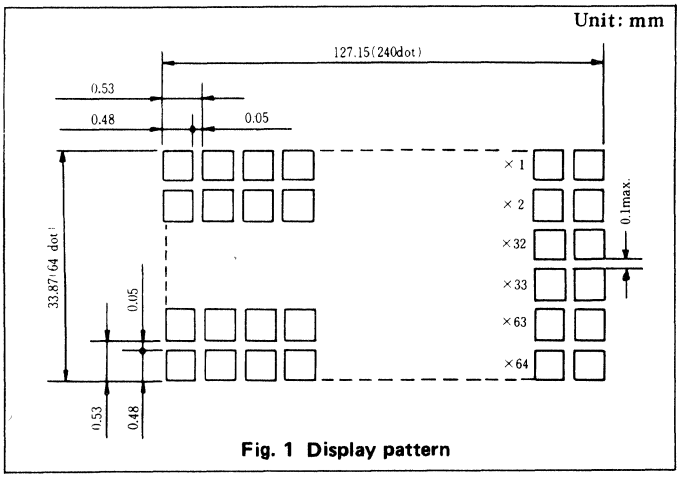


Fig. 1 Display pattern

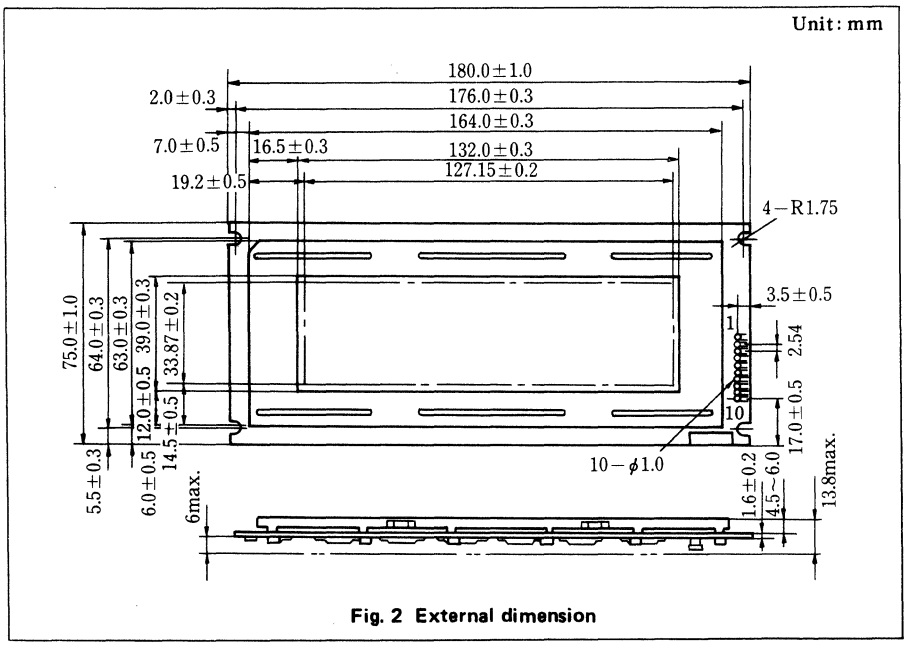


Fig. 2 External dimension

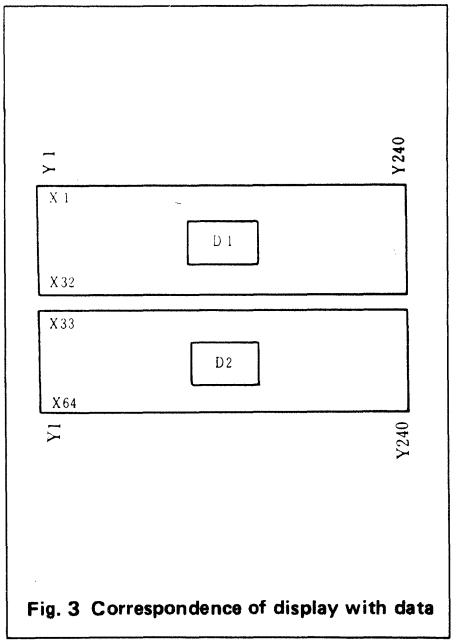


Fig. 3 Correspondence of display with data

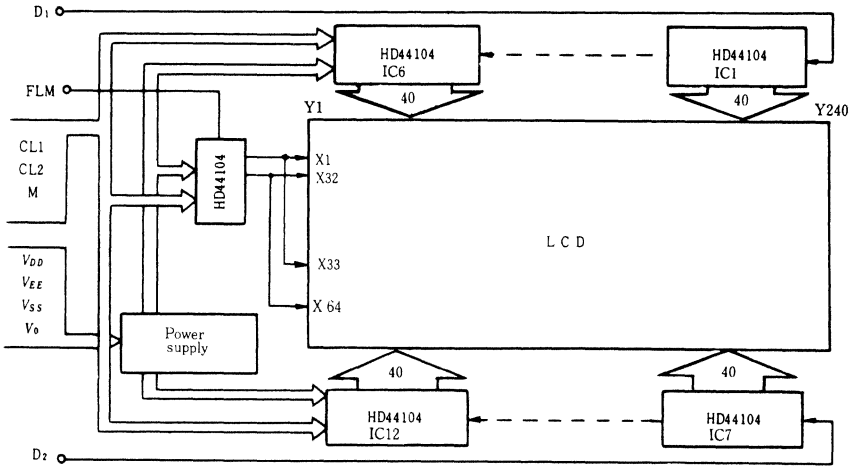
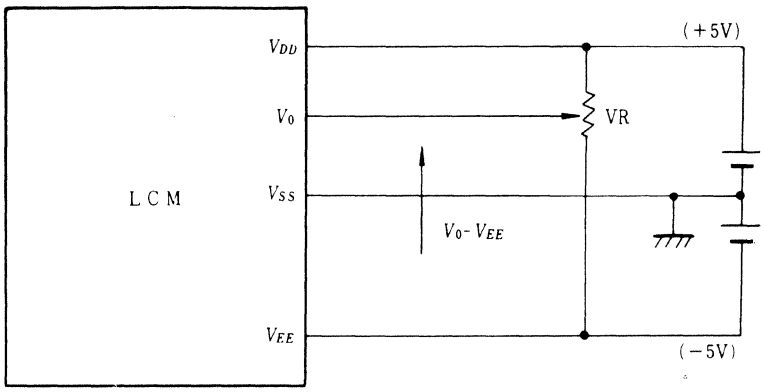


Fig. 4 Block diagram



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	520	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	–	–	ns
Clock pulse width (Low level)	t_{CWL}	800	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	300	–	–	ns
FLM set up time	t_{FSU}	300	–	–	ns
M delay time	t_{DM}	−1000	0	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	300	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CL1 may be in the range of ± 1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

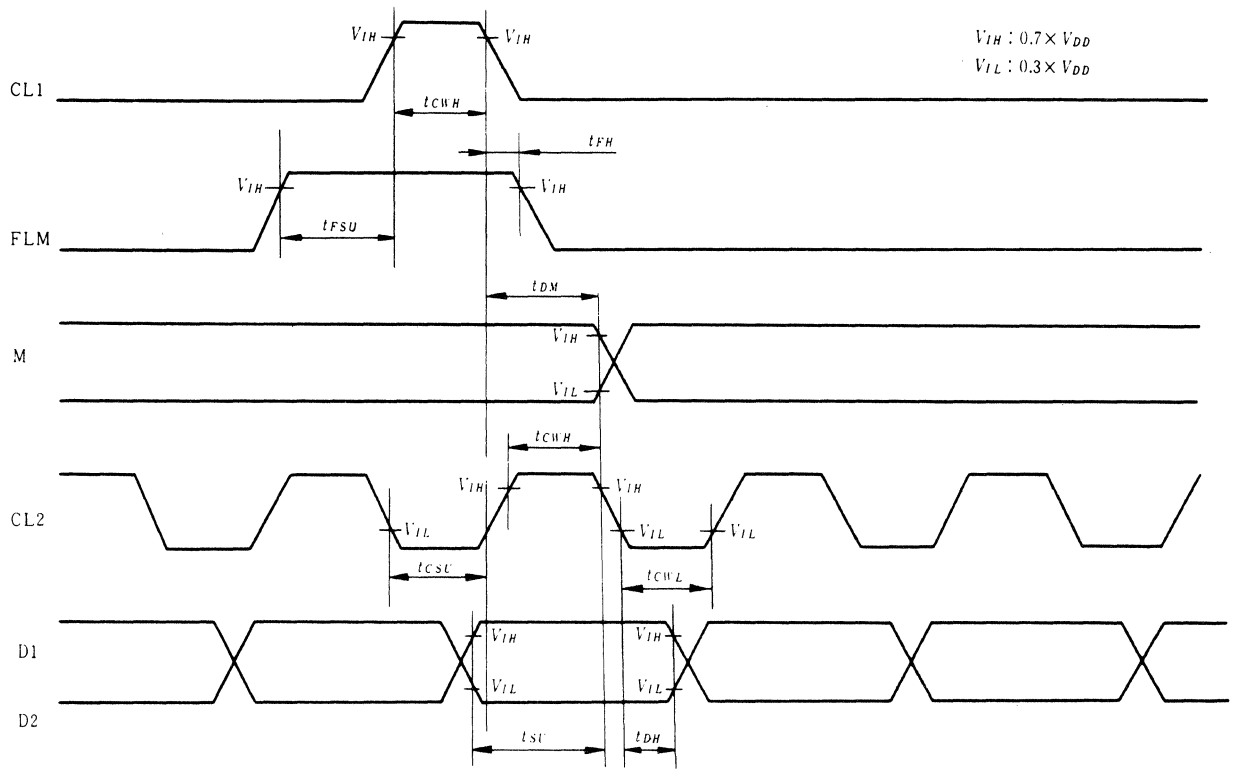


Fig. 6 Interface timing (data write)

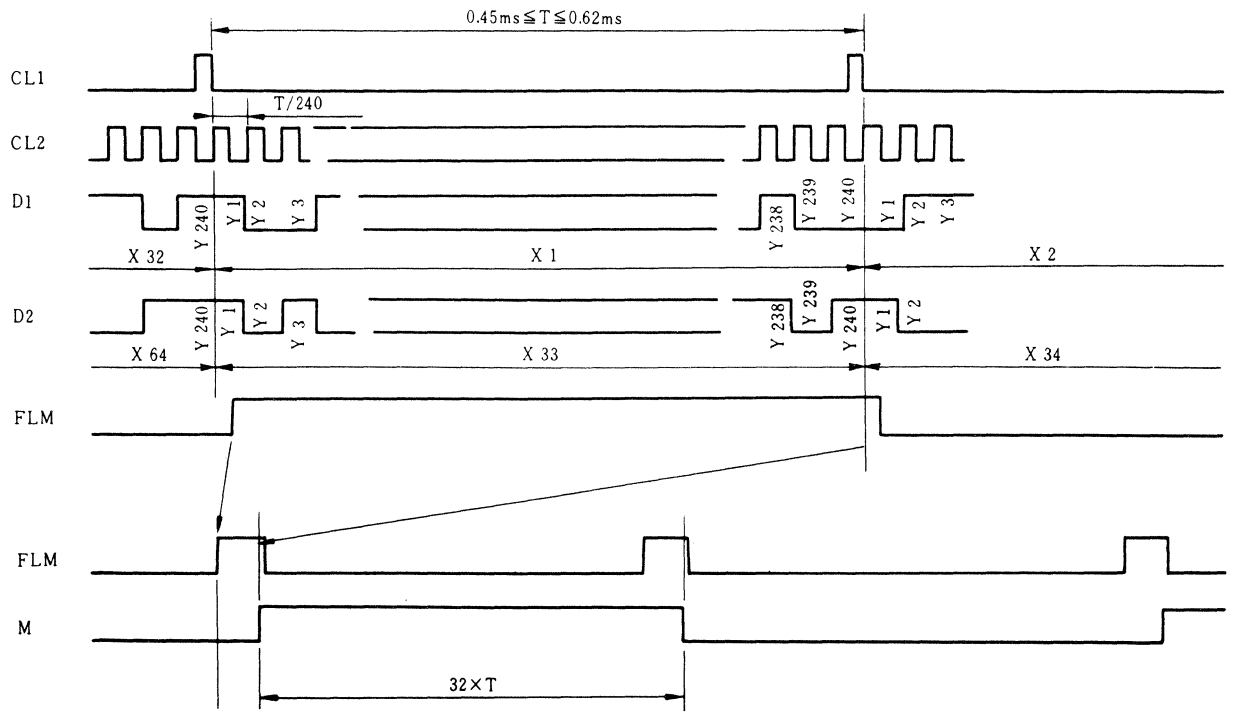


Fig. 7 Interface timing

LM213B

- 256 dot(W) x 64 dot(H) graphic and alpha-numeric display
- Controller LSI HD61830 is built-in (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size	184W x 75H x 12T (max.) mm
Effective display area	149.6W x 43H mm
Number of dots	256W x 64H mm
Dot size	0.51W x 0.51H mm
Dot pitch	0.56W x 0.56H mm
Weight	about 150 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	15.0 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

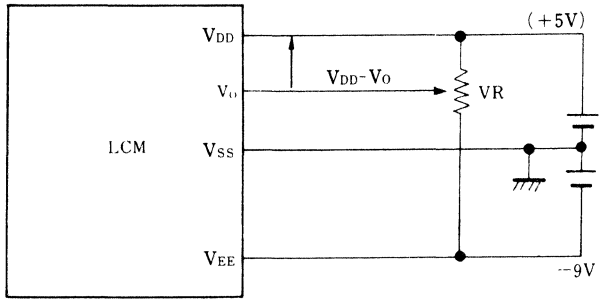
Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V,
V_{EE} = −9.0V $^{+5\%}_{-10\%}$

Operating internal frequency F_{CP1}	500 kHz
F_{CP2}	1.2 MHz
Power consumption	250 mW
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$) Duty = 1/64	
Ta = 0°C	13.2 V typ.
Ta = 25°C	11.7 V typ.
Ta = 40°C	10.2 V typ.

OPTICAL DATA .....See page 15.

INTERFACE TABLE

Pin No.	Symbol	Pin No.	Symbol
1	V_{SS} (GND)	11	DB4
2	V_{DD} (+5V)	12	DB5
3	V_0	13	DB6
4	RS	14	DB7
5	R/W	15	$\overline{CS}$
6	E	16	$\overline{RES}$
7	DB0	17	V_{EE} (−9 V)
8	DB1	18	N.C
9	DB2	19	N.C
10	DB3	20	N.C



V_{DD}-V_O: LCD driving voltage
VR: 10 kΩ ~ 20 kΩ

Fig. 1 Power supply

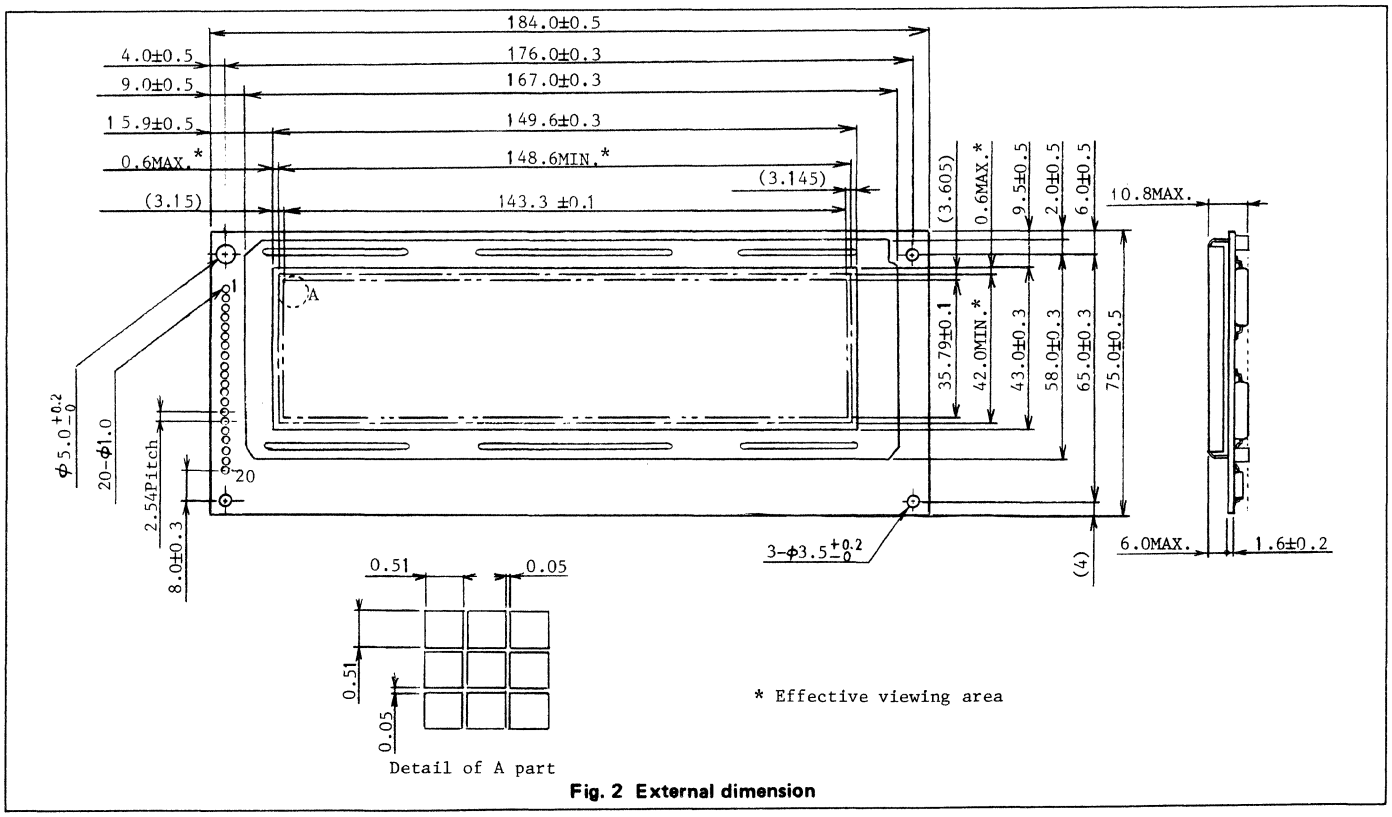


Fig. 2 External dimension

SECTION 4

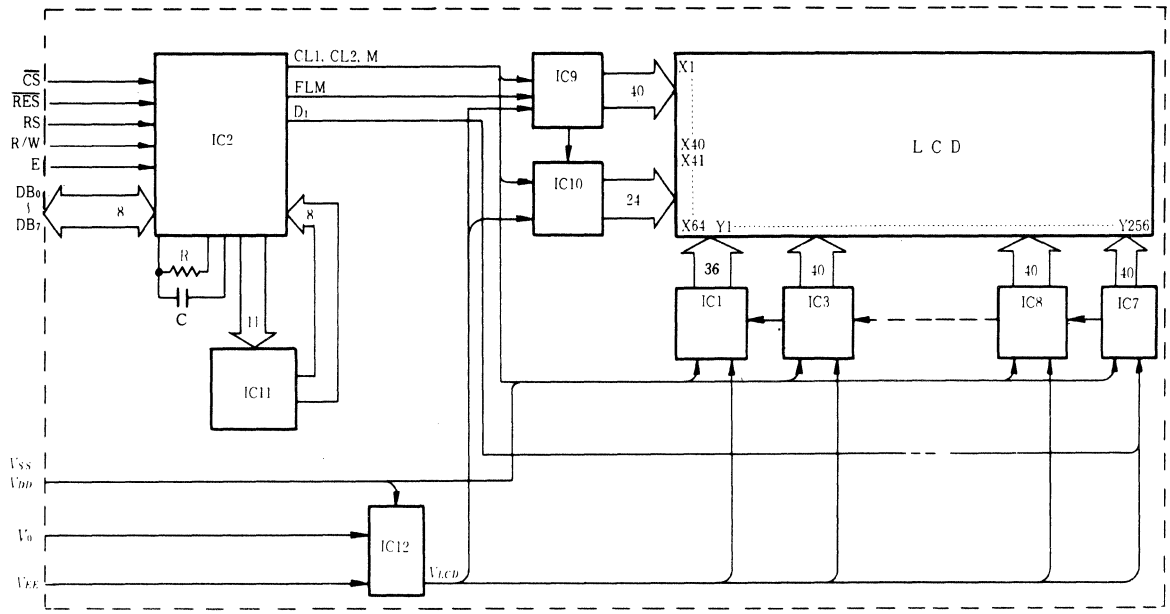


Fig. 3 Block diagram

TIMING CHARACTERISTICS

Item		Symbol	Min.	Typ.	Max.	Unit
Cycle time of 'E'		t_{CYC}	1.0	–	–	μs
Pulse width of 'E'	H level	t_{WEH}	0.45	–	–	μs
	L level	t_{WEL}	0.45	–	–	μs
Pulse raise time of 'E'		t_{Er}	–	–	25	ns
Pulse fall time of 'E'		t_{Ef}	–	–	25	ns
Set up time of CS, R/W, RS		t_{AS}	140	–	–	ns
Set up time of Input Data		t_{DIS}	225	–	–	ns
Data delay time		t_{DD}	–	–	225	ns
Hold time of Data		t_H	10	–	–	ns
Hold time of CS, R/W, RS		t_{AS}	10	–	–	ns

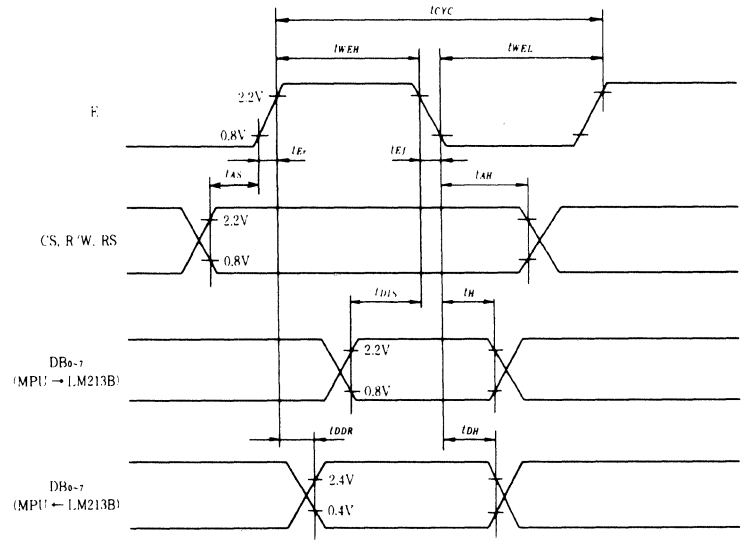


Fig. 4 Interface timing (MPU ⇔ LM213B)

LM213XB

- 256 dot(W) x 64 dot(H) graphic and alpha-numeric display
- Controller LSI HD61830 is built-in (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size	184W x 75H x 12T (max.) mm
Effective display area	149.6W x 43H mm
Number of dots	256W x 64H mm
Dot size	0.51W x 0.51H mm
Dot pitch	0.56W x 0.56H mm
Weight	about 150 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.0 V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	15.0 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V,
V_{EE} = −9.0V $^{+5\%}_{-10\%}$

Operating internal frequency F_{CP1}	500 kHz
F_{CP2}	1.2 MHz
Power consumption	250 mW
Power supply for LCD drive (Recommended) ($V_{DD} - V_O$)	Duty = 1/64
Ta = 0°C	15.0 V typ.
Ta = 25°C	14.0 V typ.
Ta = 40°C	13.5 V typ.

OPTICAL DATA ..... See page 15.

INTERFACE TABLE

Pin No.	Symbol	Pin No.	Symbol
1	V_{SS} (GND)	11	DB4
2	V_{DD} (+5V)	12	DB5
3	V_0	13	DB6
4	RS	14	DB7
5	R/W	15	$\overline{CS}$
6	E	16	$\overline{RES}$
7	DB0	17	V_{EE} (−10.5V)
8	DB1	18	N.C
9	DB2	19	N.C
10	DB3	20	N.C

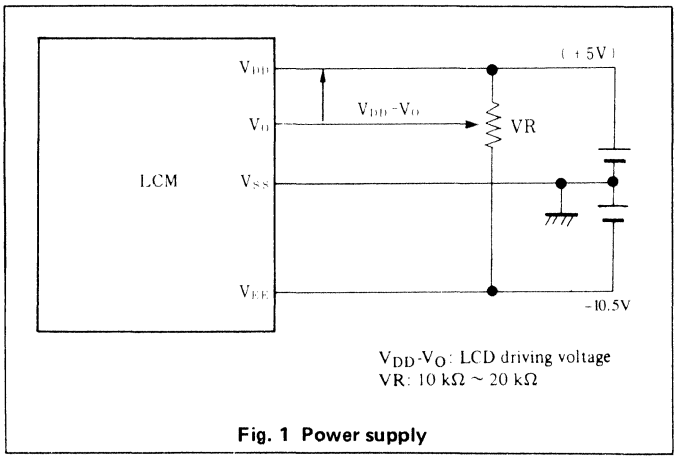


Fig. 1 Power supply

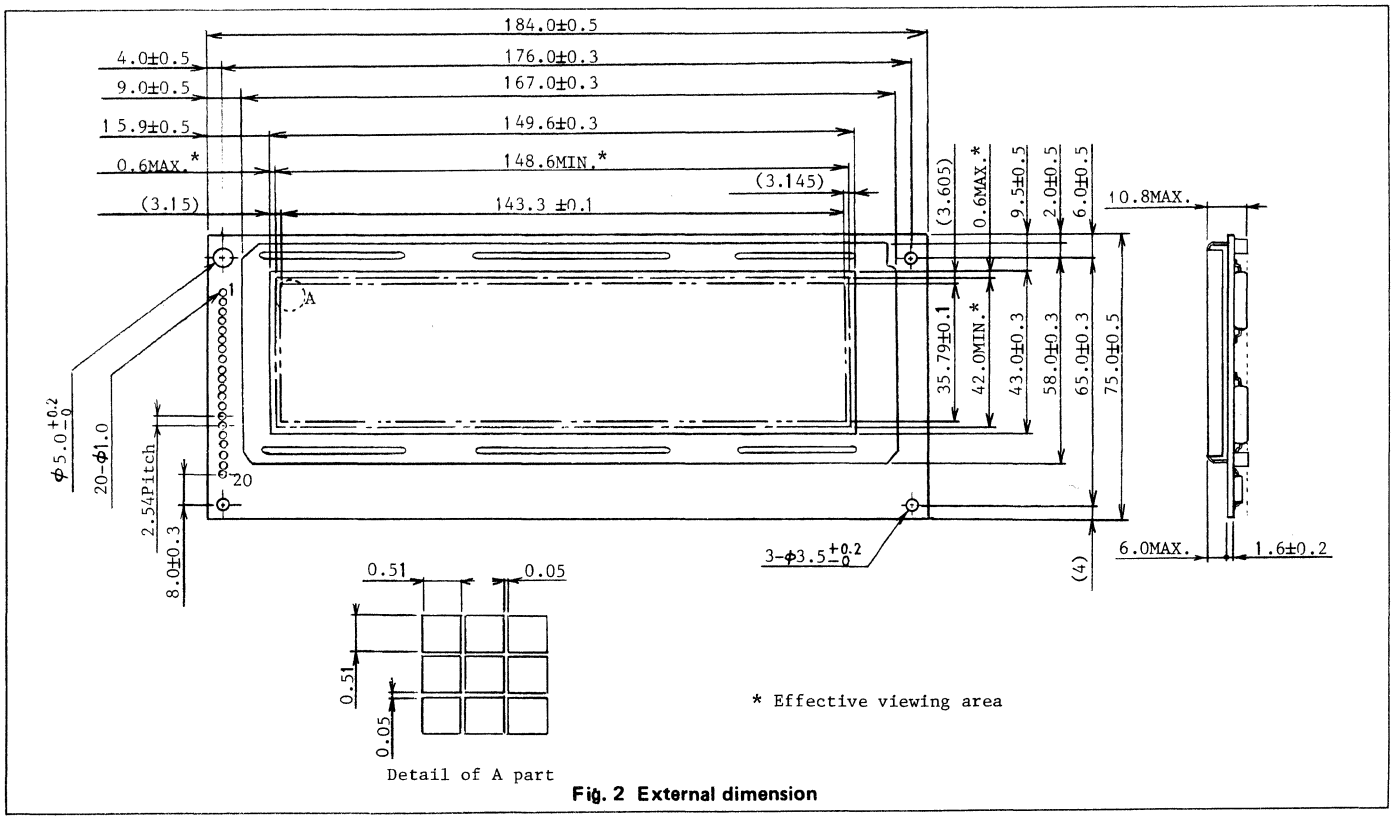


Fig. 2 External dimension

SECTION 4

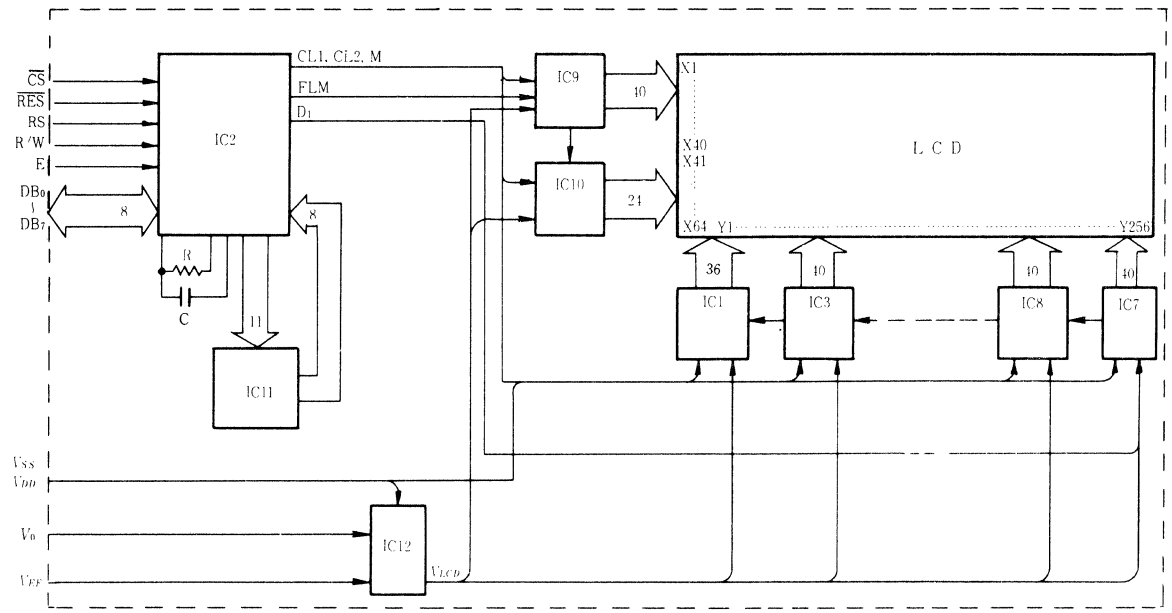


Fig. 3 Block diagram

TIMING CHARACTERISTICS

Item		Symbol	Min.	Typ.	Max.	Unit
Cycle time of 'E'		t_{CYC}	1.0	–	–	μs
Pulse width of 'E'	H level	t_{WEH}	0.45	–	–	μs
	L level	t_{WEL}	0.45	–	–	μs
Pulse raise time of 'E'		t_{Er}	–	–	25	ns
Pulse fall time of 'E'		t_{Ef}	–	–	25	ns
Set up time of CS, R/W, RS		t_{AS}	140	–	–	ns
Set up time of Input Data		t_{DIS}	225	–	–	ns
Data delay time		t_{DD}	–	–	225	ns
Hold time of Data		t_H	10	–	–	ns
Hold time of CS, R/W, RS		t_{AS}	10	–	–	ns

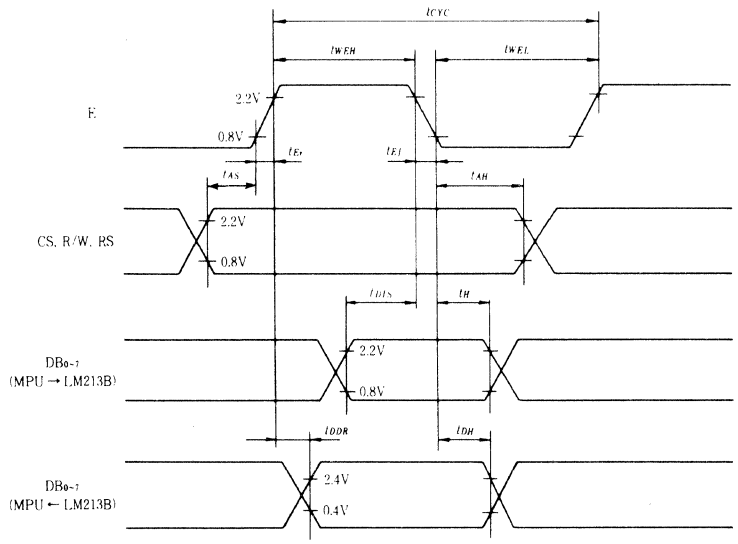


Fig. 4 Interface timing (MPU ⇔ LM213B)

LM211XB

- 480 dot(W) x 64 dot(H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 82H x 13T (max.) mm
Effective display area	240W x 38H mm
Number of dots	480W x 64H dot
Dot size	0.44W x 0.44H mm
Dot pitch	0.49W x 0.49H mm
Weight	about 180 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.0 V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	16.0 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V,
V_{EE} = −9.0V ± 0.45 V

Input "high" voltage (Vi_H)	0.7 x V_{DD} V min.
Input "low" voltage (Vi_L)	0.3 x V_{DD} V max.
Clock frequency (f_{CL2})	610 kHz min.
	920 kHz typ.
	1200 kHz max.
Power supply current (I_{DD})	16 mA typ.
(I_{EE})	6 mA typ.

Power supply for LCD drive (Recommended) (V_{DD} − V_O)
Duty = 1/64

Ta = 0°C	15.0 V typ.
Ta = 25°C	14.0 V typ.
Ta = 40°C	13.5 V typ.

OPTICAL DATA . . . . . See page 15.

INTERFACE TABLE

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (left half)
2	FLM	H	The FLM signal indicates the beginning of each display cycle
3	M	H/L	Control signal for AC driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data (right half)
7	V_{DD}(+5V)	—	Power supply for logic circuit
8	V_{SS}	—	Ground
9	V_{EE}(-9.0V)	—	Power supply for LC driving
10	V_O	—	Operating voltage for LC driving

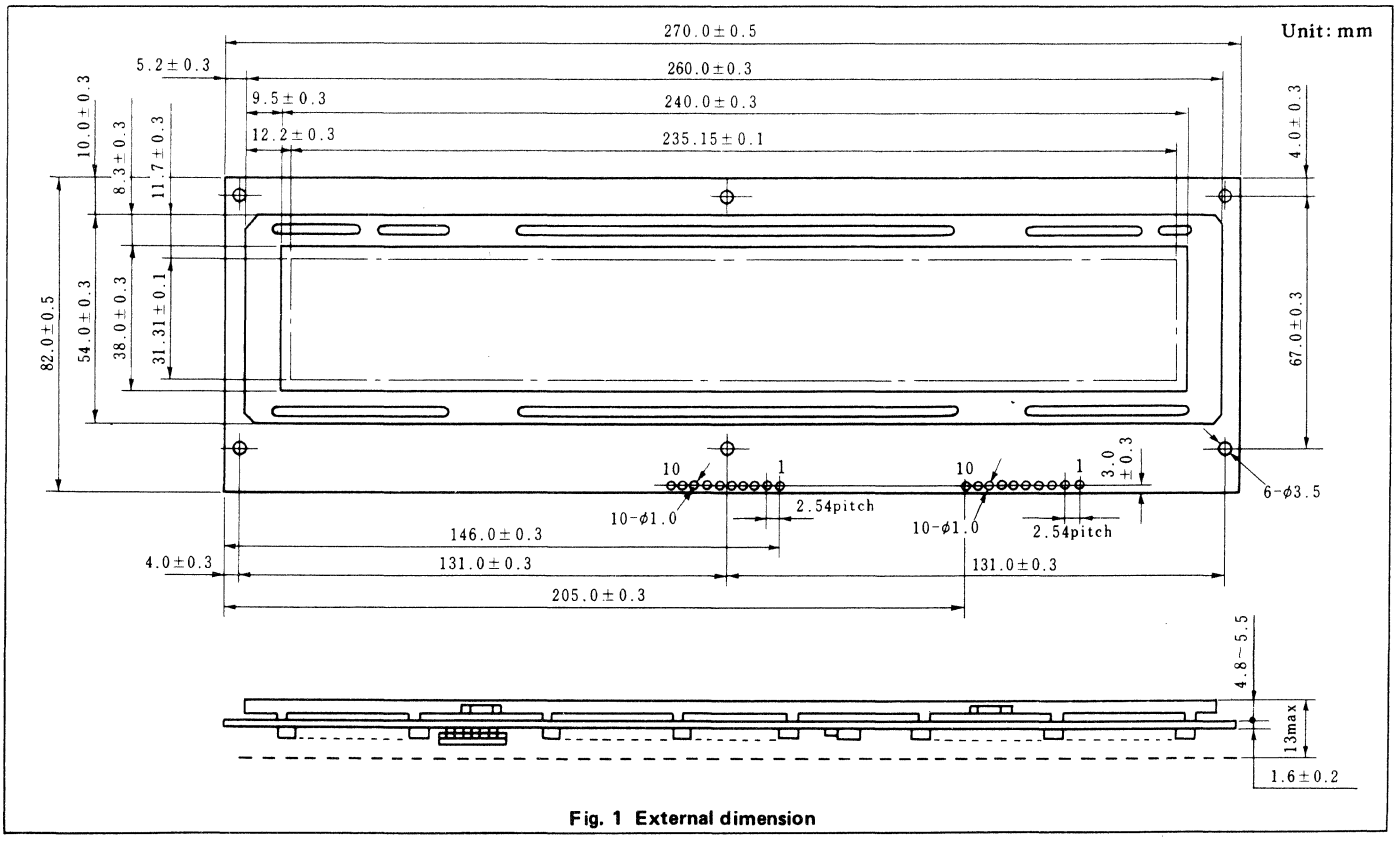


Fig. 1 External dimension

SECTION 4

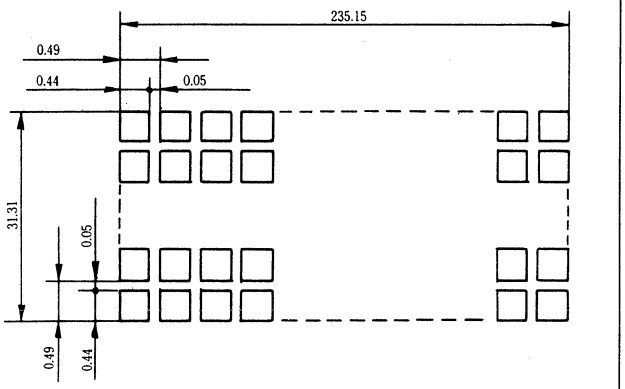


Fig. 2 Display pattern

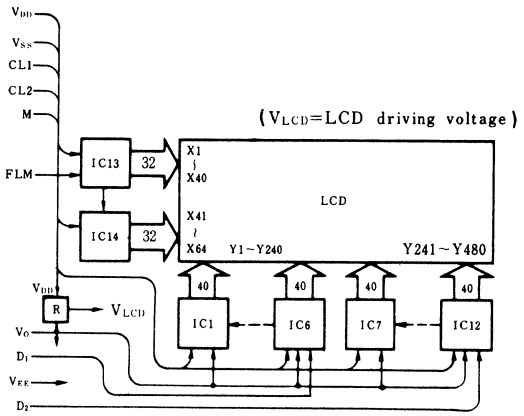
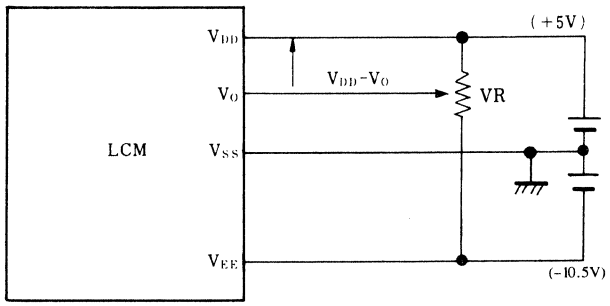


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10 kΩ ~ 20 kΩ

Fig. 4 Power supply

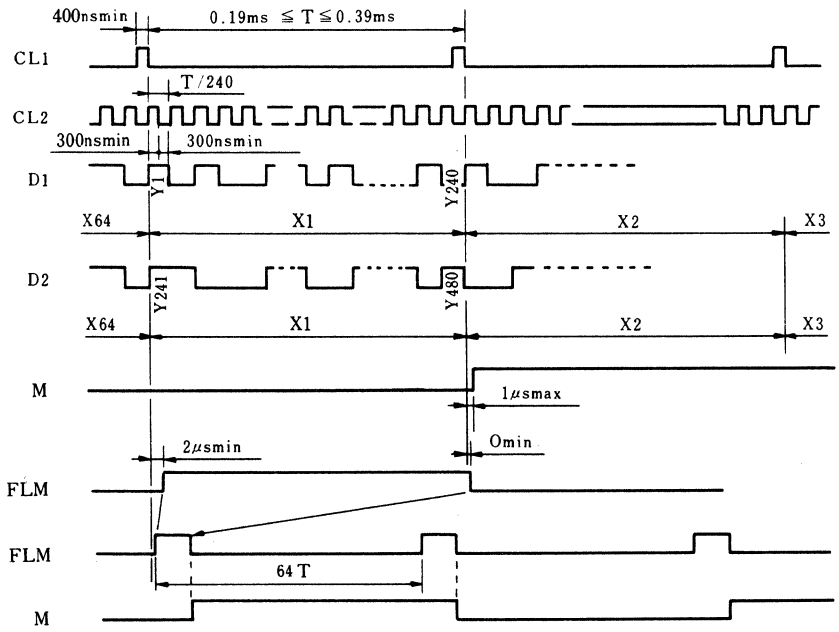


Fig. 5 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	f_{CL2}	–	–	1200	kHz (Note 1)
Clock pulse width (High level)	t_{CWH1}	400	–	–	ns
	t_{CWH}	300	–	–	
Clock pulse width (Low level)	t_{CWL}	300	–	–	ns
Clock set up time	t_{CSU}	300	–	–	ns
Data set up time	t_{SU}	200	–	–	ns
FLM set up time	t_{FSU}	200	–	–	ns
M delay time	t_{DM}	−1000	–	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	200	–	–	ns

Notes 1. Optimum frequency for the highest contrast depends on the type of module.
2. Timing of M signal to CL1 may be in the range of ±1000ns.
3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50 Hz ±2 Hz or 60 Hz ±2 Hz) to prevent LCD flicker.

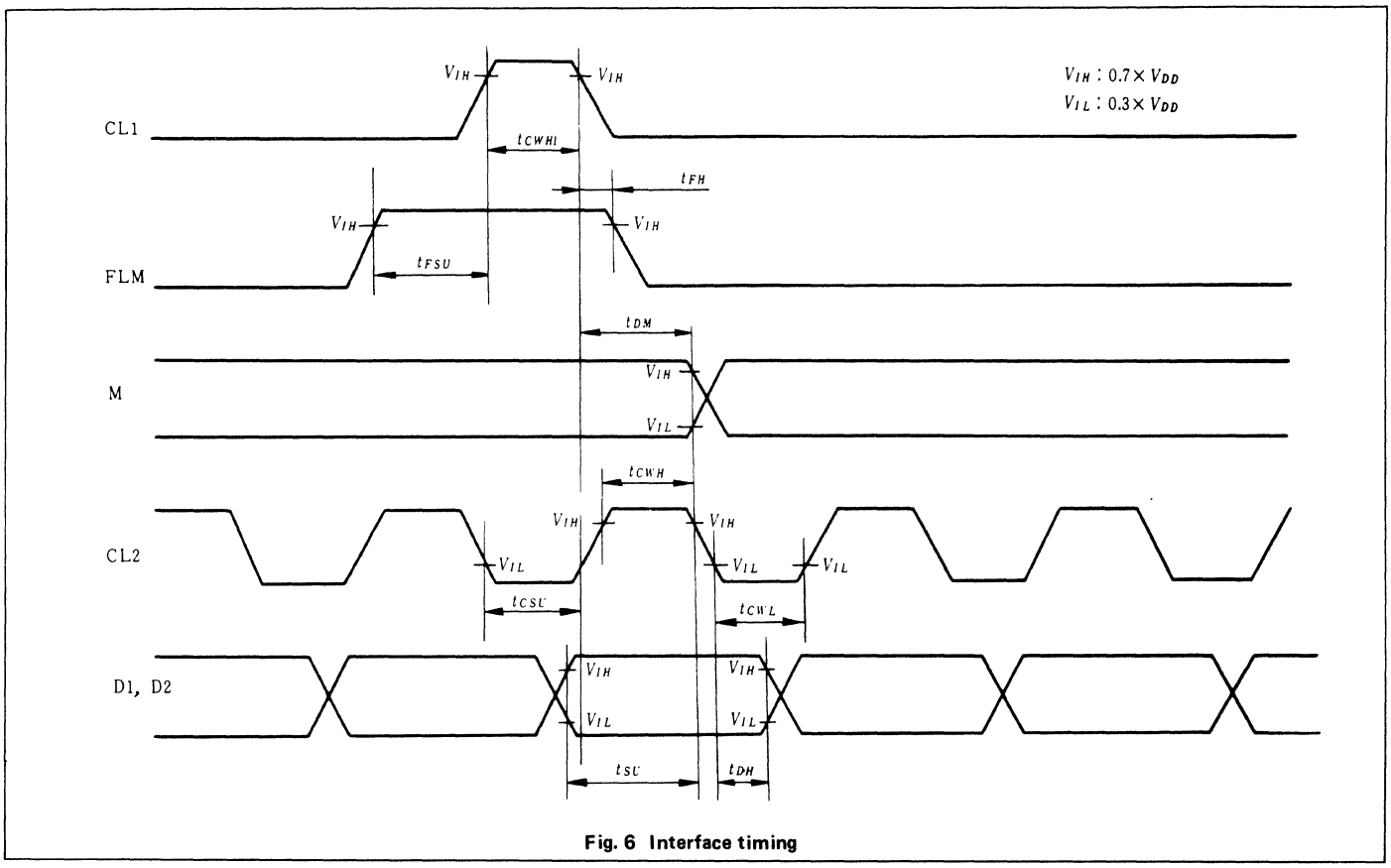


Fig. 6 Interface timing

LM266XP

FEATURES

- 640(W) dots × 100(H) dots graphic and alphanumeric display
- Attachable controller: HD63645F

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .287.5W × 71.5H × 13T (max.) mm
Effective display area . . . . . .243W × 42H mm
Number of dots . . . . . .640W × 100H dots
Dot size . . . . . .0.33W × 0.33H mm
Dot pitch. . . . . .0.36W × 0.36H mm
Weight 250g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	−0.3	7.0V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	−0.3	28.0V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} + 0.3V
Operating temperature (Ta) (Note 2)	0 ~	+ 40°C
Storage temperature (Tstg) (Note 3)	−20 ~	+ 60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V, V_L = −19.0 V ± 0.95 V
Input "high" voltage (V_{IH}) . . . . . .0.7 × V_{DD} ~ V_{DD}V
Input "low" voltage (V_{IL}) . . . . . .0 ~ 0.3 × V_{DD}V
Power supply current for logic (I_{DD}) (Note 4). . . . . .8 mA max.
Power supply current for LCD drive (I_{EE}) (Note 4). . . . .6 mA max.
Frame frequency (f_{FLM}). . . . . .78 Hz typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_L$) (Note 5).
Duty = 1/200

Ta = 0°C . . . . . .19.5 V typ.
Ta = 25°C . . . . . .18.5 V typ.
Ta = 40°C . . . . . .17.8 V typ.

Notes 1. Applied to CL1, CL2, D0 ~ D3, FLM and M.
2. The color of the display may change into blue if operated at maximum temperature. It is recommended to use it between 0°C ~ 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. V_{DD} = +5V, $V_{DD} - V_L$ = 24V, D0 ~ D3 = 1010, f_{FLM} = 78 Hz
5. Viewing angle = 10°
6. To avoid damage during excessive shock environments, we recommend a support post be placed under the PCB by the customer.

OPTICAL DATA . . . . . .See page 15

INTERNAL PIN CONNECTION

Pin No.	symbol	Function
1	V_{DD}	Power supply for logic circuit
2	V_{SS}	Ground
3	V_{VB}	Connected to metal frame (GND)
4	VL	Power supply for IC driving
5	CL1	Date latch
6	M	Control signal for AC driving
7	FLM	The FLM signal indicating the beginning of each display cycle
8	CL_2	Data shift
9	D0	Data
10	D1	
11	D2	
12	D3	

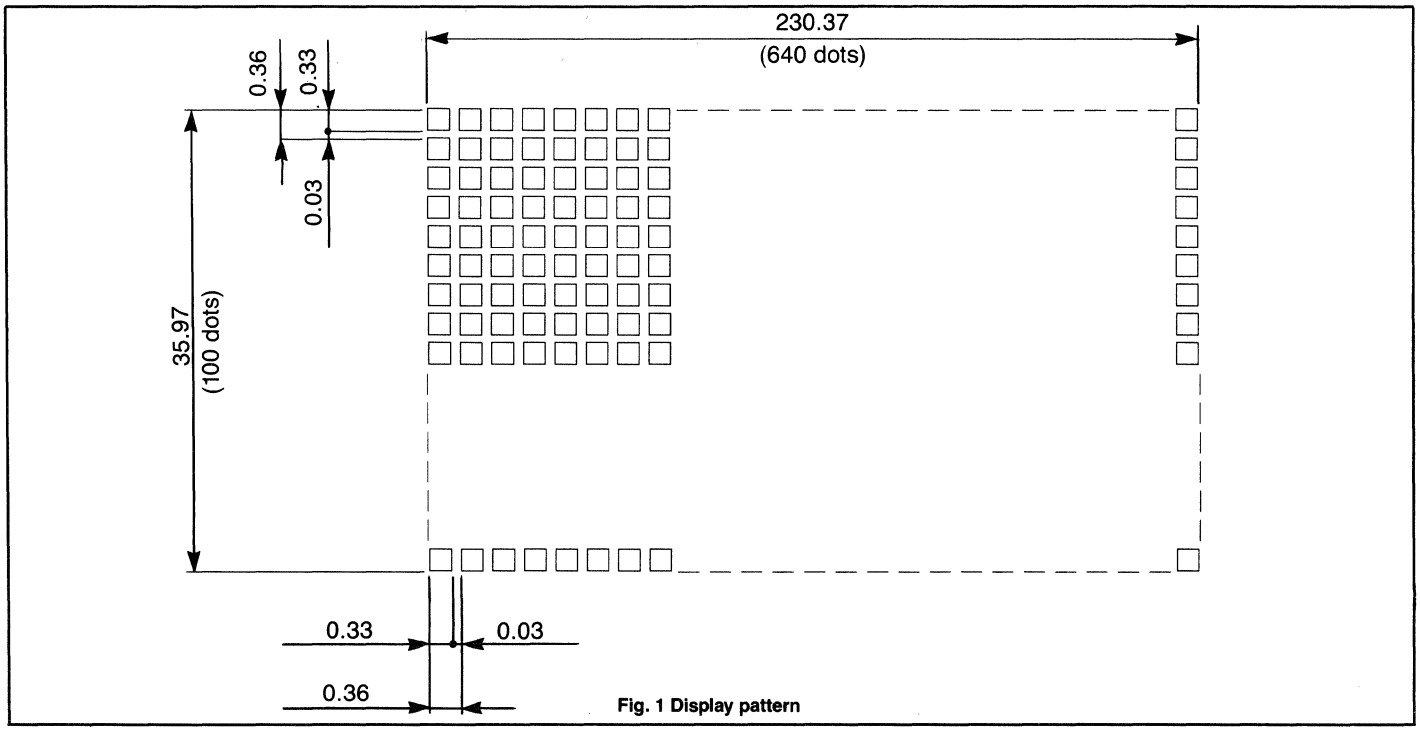


Fig. 1 Display pattern

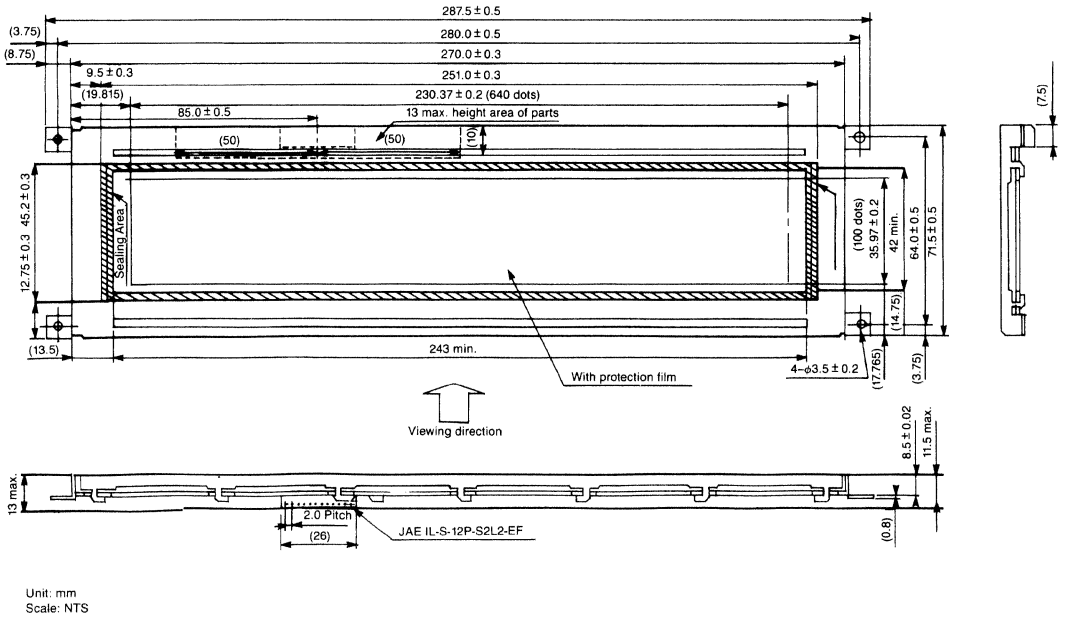


Fig. 2 External dimension

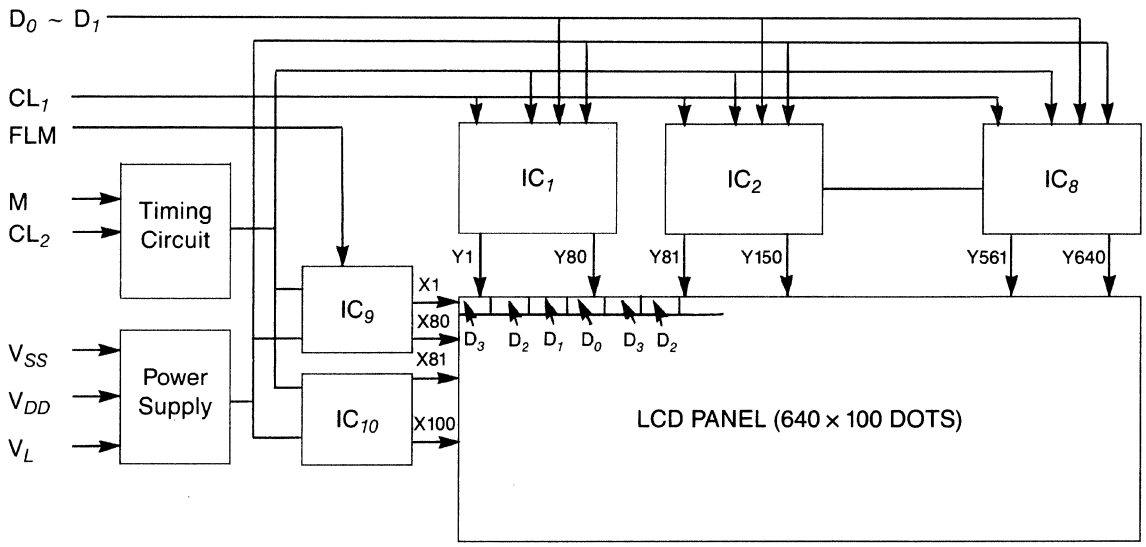


Fig. 3 Block diagram

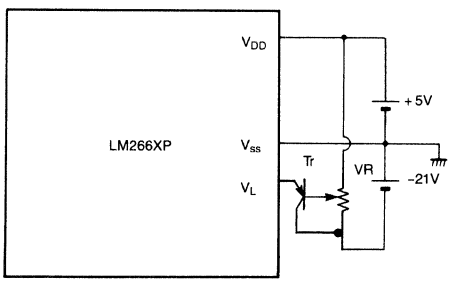


Fig. 4 Power supply

SECTION 4

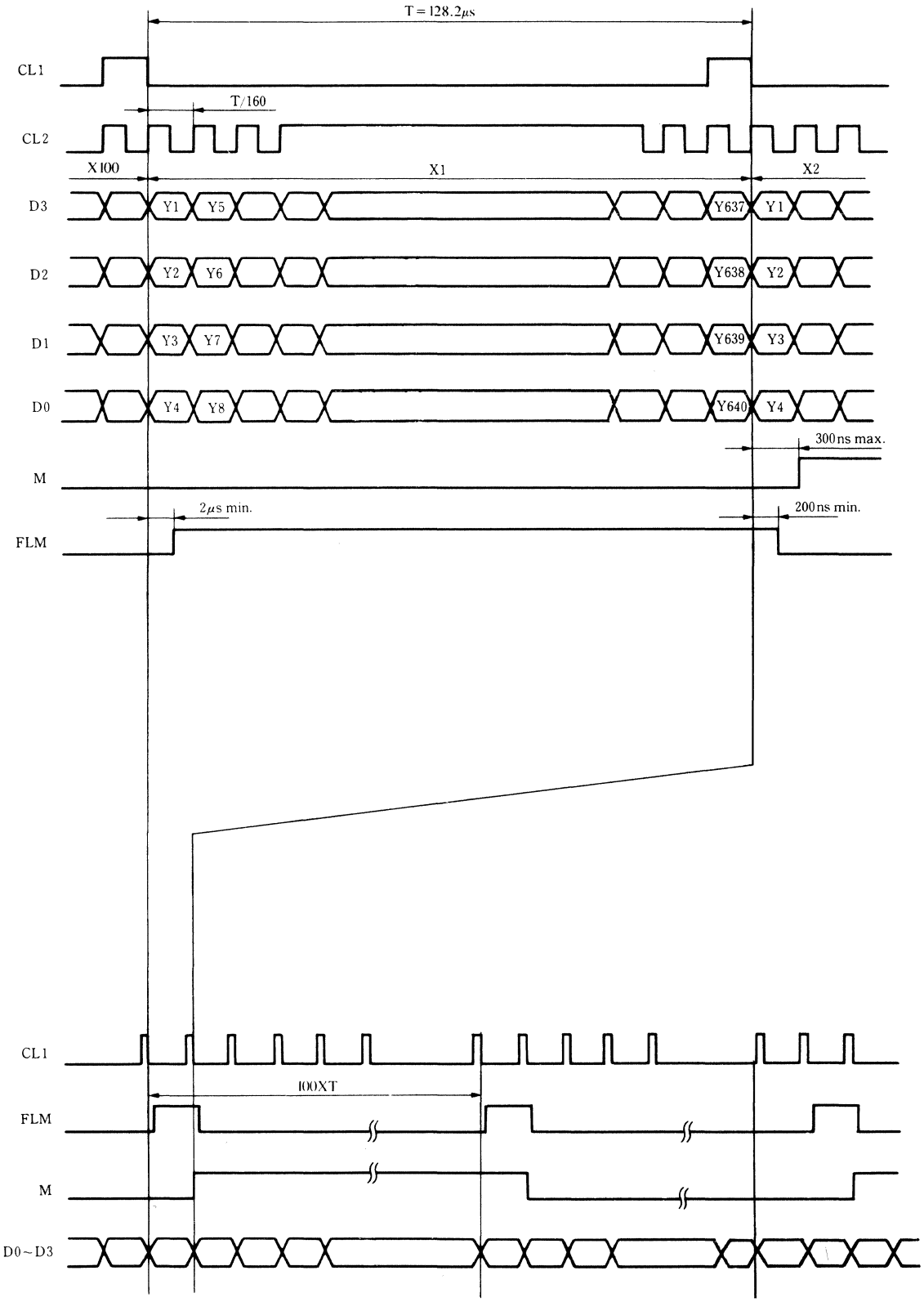


Fig. 5 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 Cycle Time	t_{CYC}	410	—	—	ns
CL2 Pulse With (H)	t_{CWH}	150	—	—	ns
CL2 Pulse Width (L)	t_{CWL}	150	—	—	ns
CL1 Setup Time	t_{SCL2}	150	—	—	ns
CL1 Hole Time	t_{HCL2}	150	—	—	ns
Clock Rise/Fall Time	t_r, t_f	—	—	30	ns
Data Setup	t_{DSU}	100	—	—	ns
Data Hold	t_{DH}	100	—	—	ns
M Signal Delay Time	t_{CM}	—	—	300	ns
FLM Setup Time	t_{FS}	200	—	—	ns
FLM Hold Time	t_{FH}	200	—	—	ns

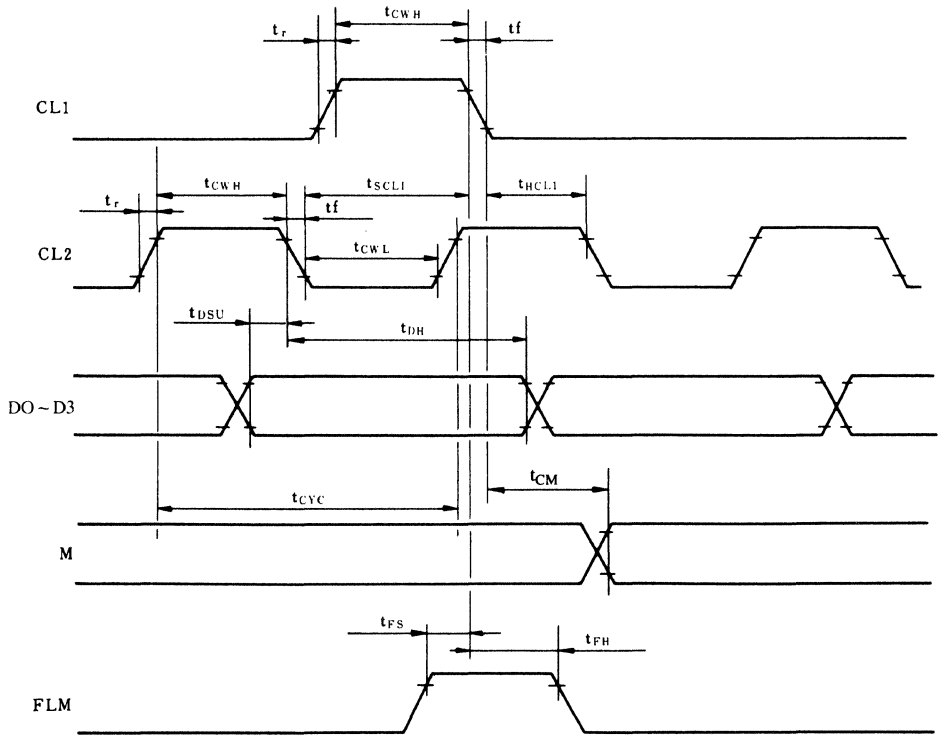


Fig. 6 Interface timing

LM551XT

FEATURES

- 128(W) dots × 128(H) dots graphic and alphanumeric display
- Attachable controller: HD63645F

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 88W × 86H × 14.0T (max.) mm
Effective display area . . . . . 54.0W × 54.0H mm
Number of dots . . . . . 128W × 128H dots
Dot size . . . . . 0.35W × 0.35H mm
Dot pitch . . . . . 0.38W × 0.38H mm
Weight . . . . . 125 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	−0.3	7.0V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	−0.3	28.0V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} + 0.3V
Operating temperature (Ta) (Note 2)	0 ~ +40°C	
Storage temperature (Tstg) (Note 3)	−20 ~ +60°C	

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 ± 0.25 V, V_{EE} = −20 ± 0.75 V
Input "high" voltage (V_{IH}) . . . . . 0.7 × V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) . . . . . 0 ~ 0.3 × V_{DD} V
Power supply current for logic (I_{DD}) (Note 4) . . . . . 4 mA typ.
Power supply current for LCD drive (I_{EE}) (Note 4) . . . . . 2 mA typ.
Frame frequency (f_{FLM}) . . . . . 65 Hz min.
70 Hz typ.
75 Hz max.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
1/200 Duty (Note 3)
Ta = 0°C . . . . . 22.5 V typ.
Ta = 25°C . . . . . 21.5 V typ.
Ta = 40°C . . . . . 20.2 V typ.

Notes 1. Applied to CL1, CL2, D0 ~ D3, FLM and M.
2. The color of the display may change into blue if operated at maximum temperature. It is recommended to use it between 0°C ~ 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. V_{DD} = +5V, $V_{DD} - V_0$ = 21.5V, D0 ~ D3 = 1010, FLM = 70 Hz
5. Viewing angle = 10°

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D3	H/L	Data
2	D2	H/L	Data
3	FLM	H	The FLM signal indicating the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H → L	Data latch
6	CL2	H → L	Data shift
7	D1	H/L	Data
8	D0	H/L	Data
9	V_{DD}	–	Power supply for logic circuit
10	V_{SS}	–	Ground
11	V_{EE}	–	Power supply for LC driving
12	V_0	–	Operating voltage for LC driving

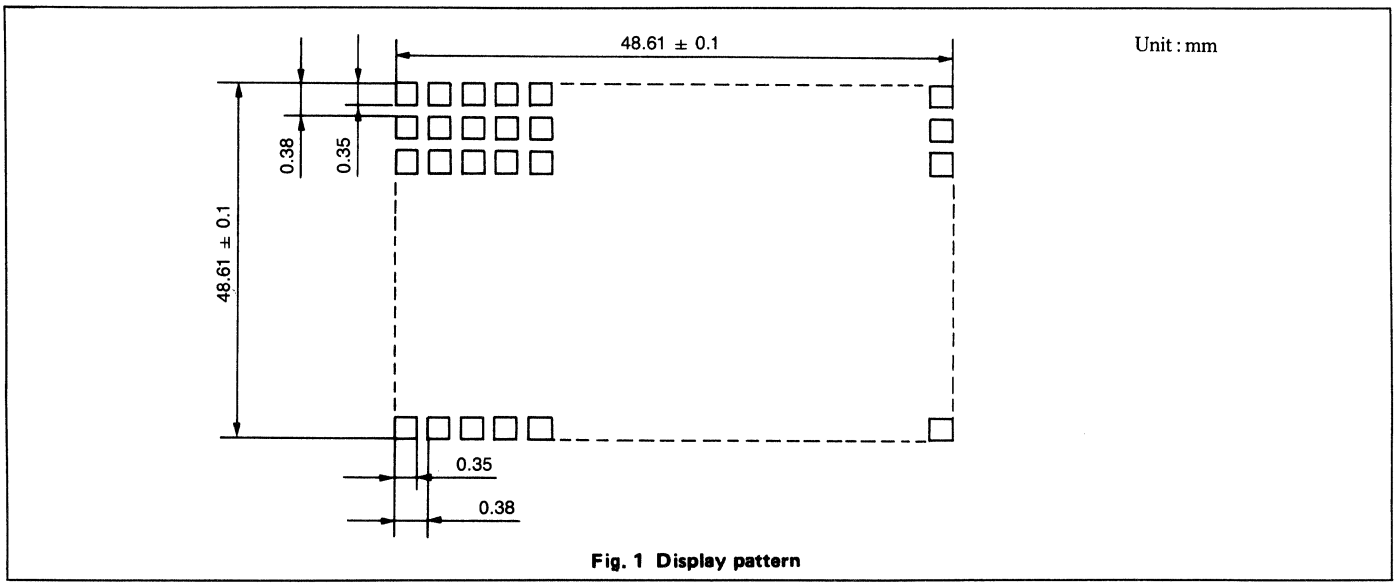


Fig. 1 Display pattern

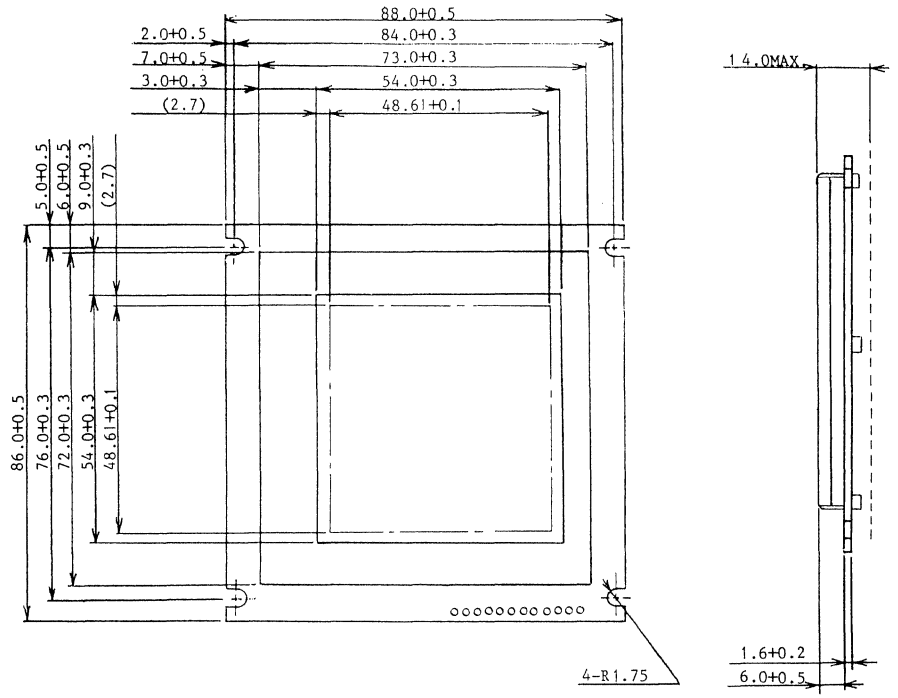


Fig. 2 External dimension

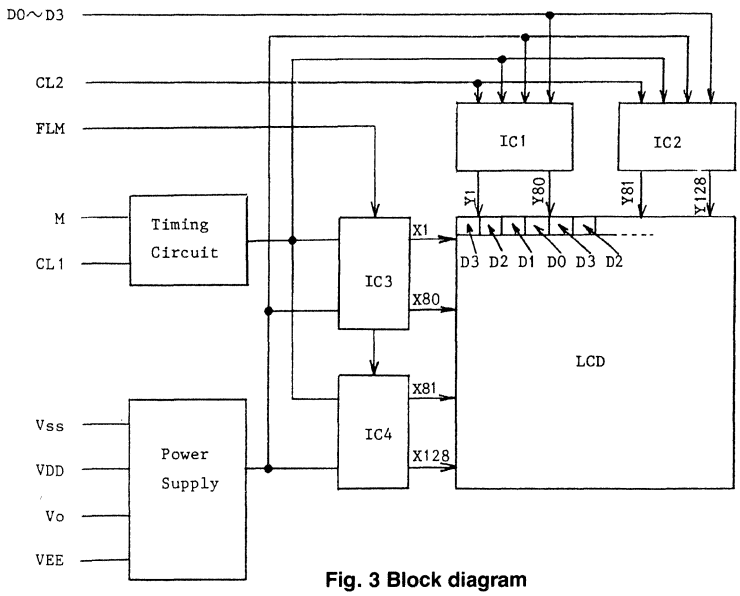
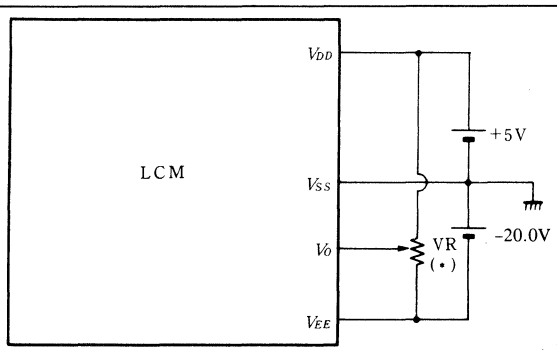


Fig. 3 Block diagram



*VR: 10~20kΩ

Fig. 4 Power supply

SECTION 4

Observe the following sequencing when turning power supply on and off.

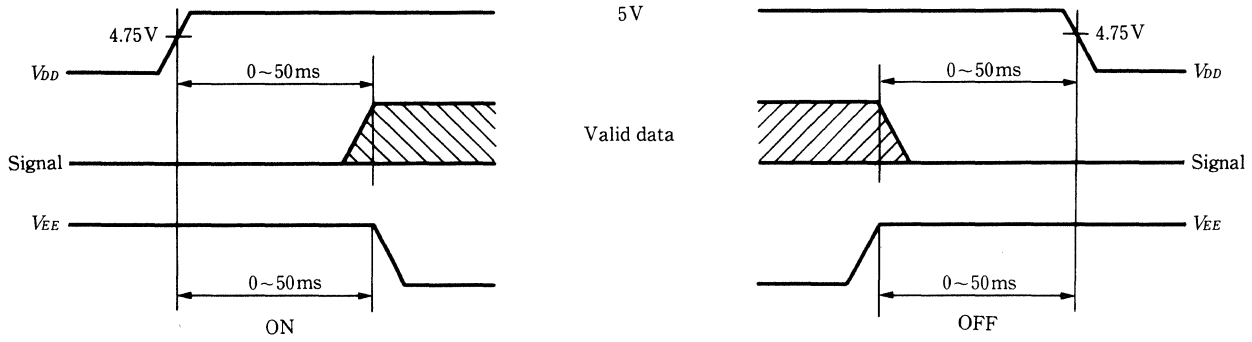


Fig. 5 Voltage sequencing

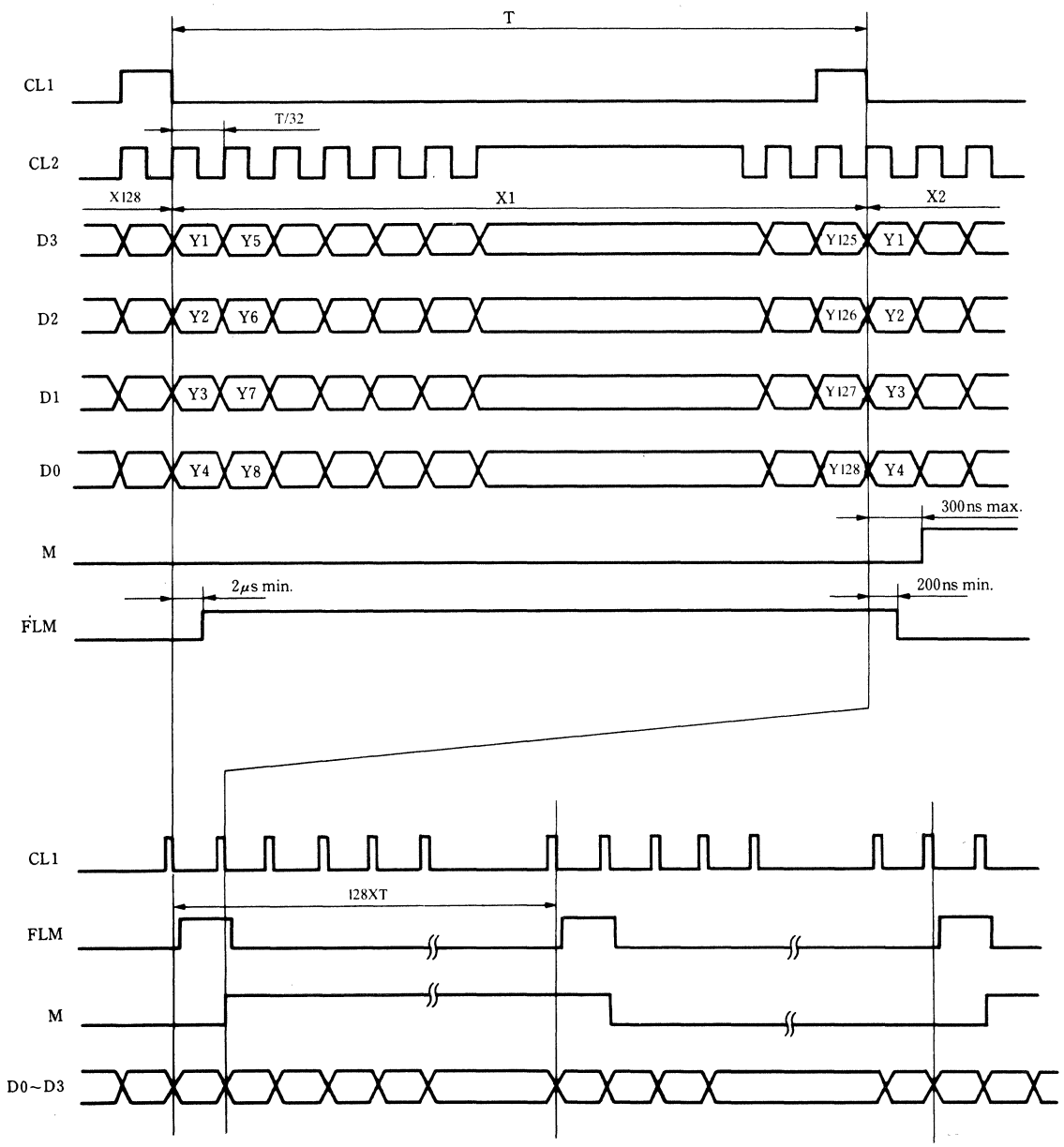


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	410	–	–	ns
CL2 pulse width	t_{CWH}	150	–	–	ns
CL2 pulse width	t_{CWL}	150	–	–	ns
CL1 set up time	t_{SCL1}	150	–	–	ns
CL1 hold time	t_{HCL1}	150	–	–	ns
Clock rise, fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	200	–	–	ns

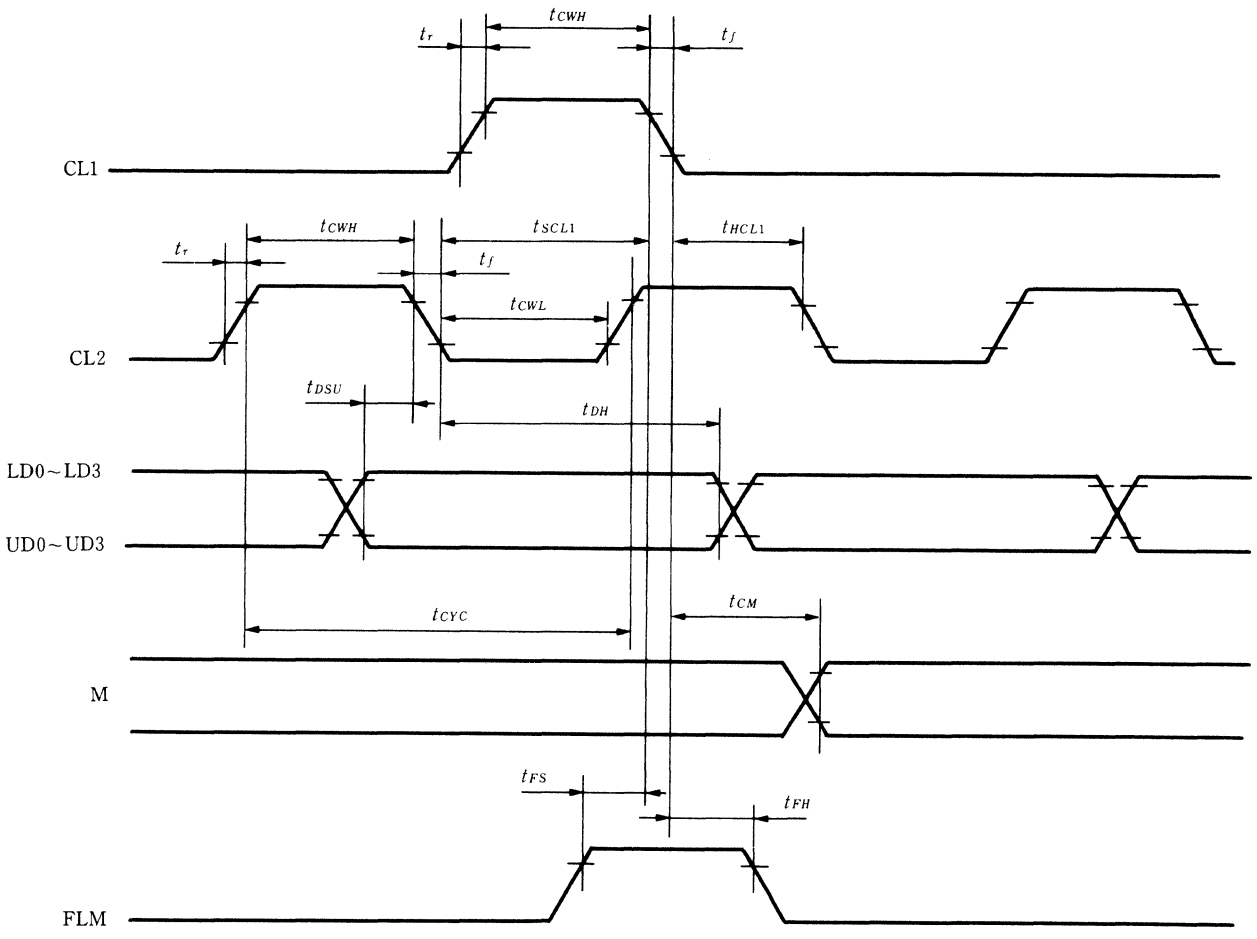


Fig. 7 Interface timing

LM221XB

- 240 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size	180W x 120H x 13.8T (max.) mm
Effective display area	148W x 75.0H mm
Number of dots	240W x 128H dot
Dot size	0.50W x 0.50H mm
Dot pitch	0.55W x 0.55H mm
Weight	about 210 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	V_{SS}	V_{DD} V
Operating temperature (Ta) (Note 2)	0	40°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, $V_{DD} - V_{SS}$ = 5.0V ±0.25V,
$V_{EE} - V_{SS}$ = 13.5V ±0.25V

Input "high" voltage (V_{IH}) (Note 1)	0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) (Note 1)	0 ~ 0.3 x V_{DD} V
Clock frequency (f_{CL2})	1.08 MHz min.
	1.15 MHz typ.
	1.23 MHz max.
Power supply current (I_{DD})	6 mA typ.

(D_1, D_2 = GND) (f_{CL2} = 1.15 MHz) ($V_{DD} - V_0$ = 12.9V)

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/64

Ta = 0°C	17.3 V typ.
Ta = 25°C	16.4 V typ.
Ta = 40°C	15.7 V typ.

OPTICAL DATA See page 15.

Notes 1. Applied to CL1, CL2, D1 ~ D2, M, FLM.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data
2	FLM	H	The FLM signal indicates the beginning of each display cycle
3	M	H/L	Control signal for AC driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data
7	V_{DD}	–	Power supply for logic circuit
8	V_{SS}	–	Ground
9	V_{EE}	–	Power supply for LC driving
10	V_0	–	Operating voltage for LC driving

Unit: mm

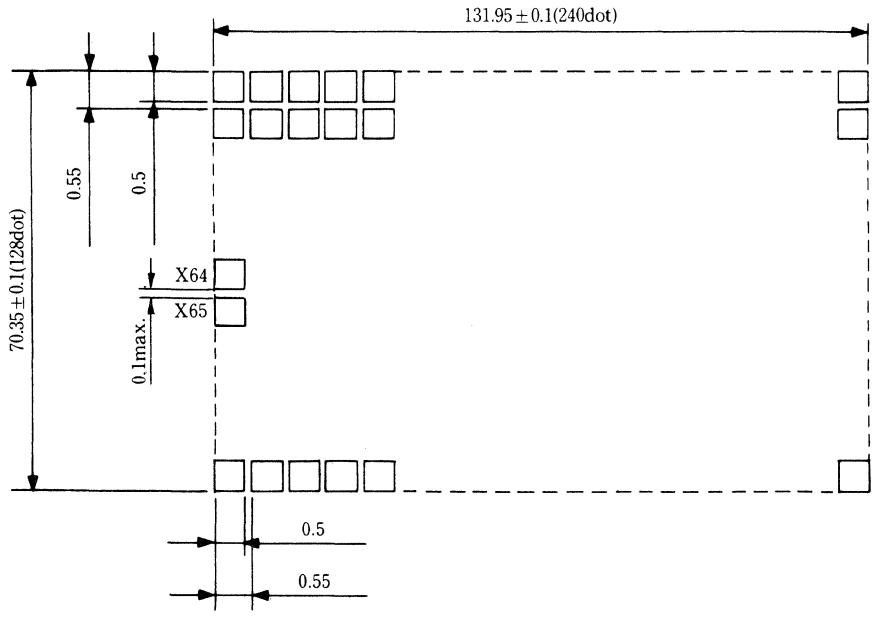
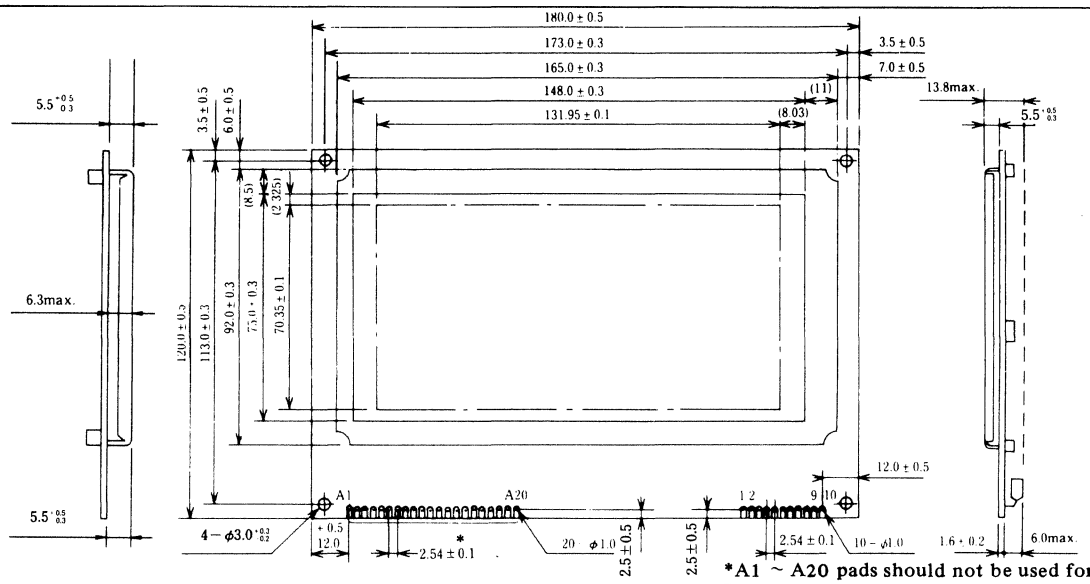


Fig. 1 Display pattern



*A1 ~ A20 pads should not be used for LM221B.
Do not connect any signals to these pads.
Use pin No. 1 ~ 10 for interface.

Fig. 2 External dimensions

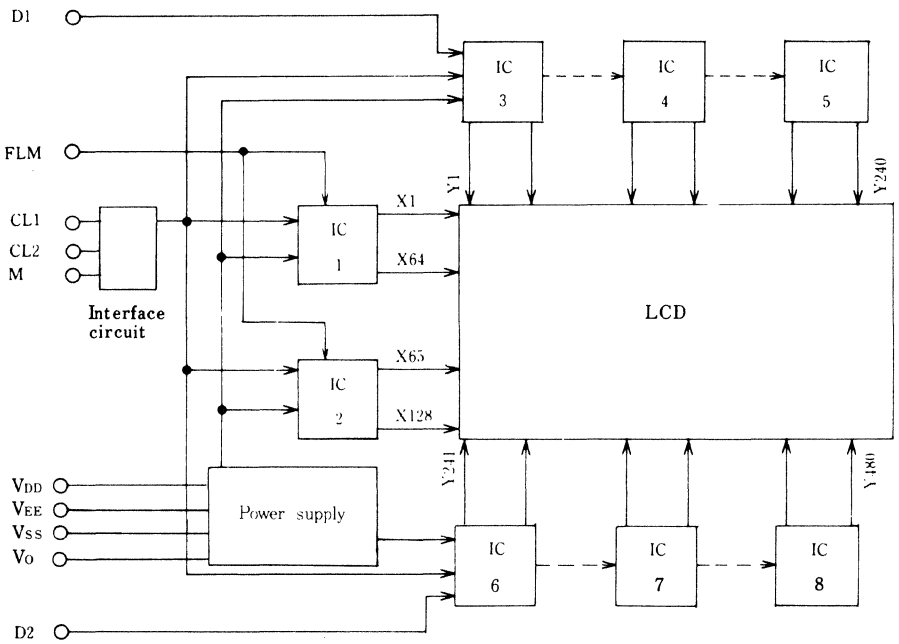
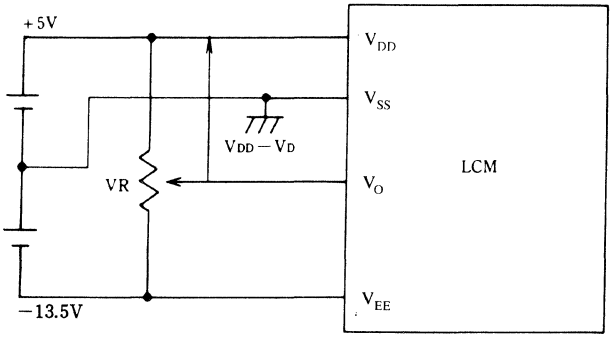


Fig. 3 Block diagram



VDD − V0: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply

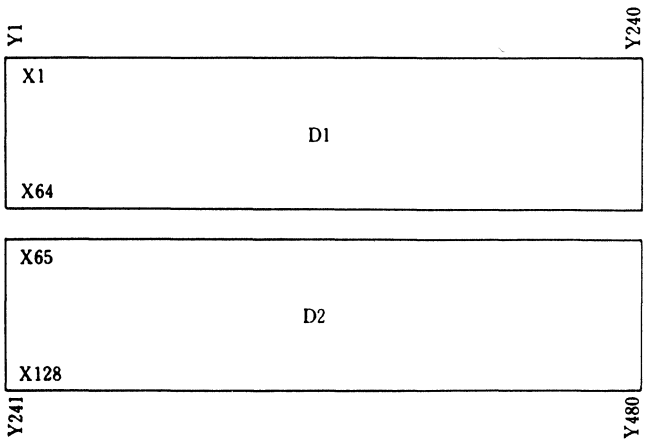


Fig. 5 Correspondence of display with data

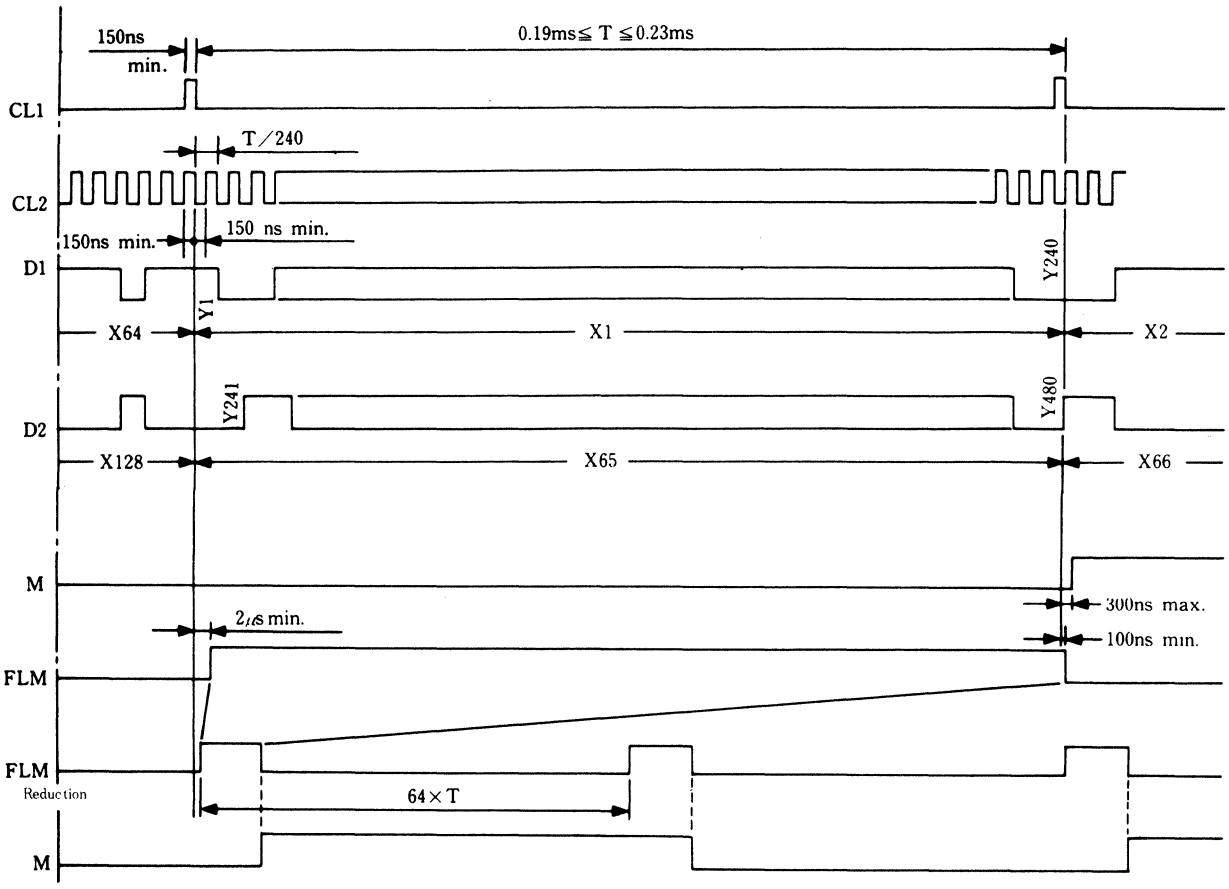


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	810	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	100	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

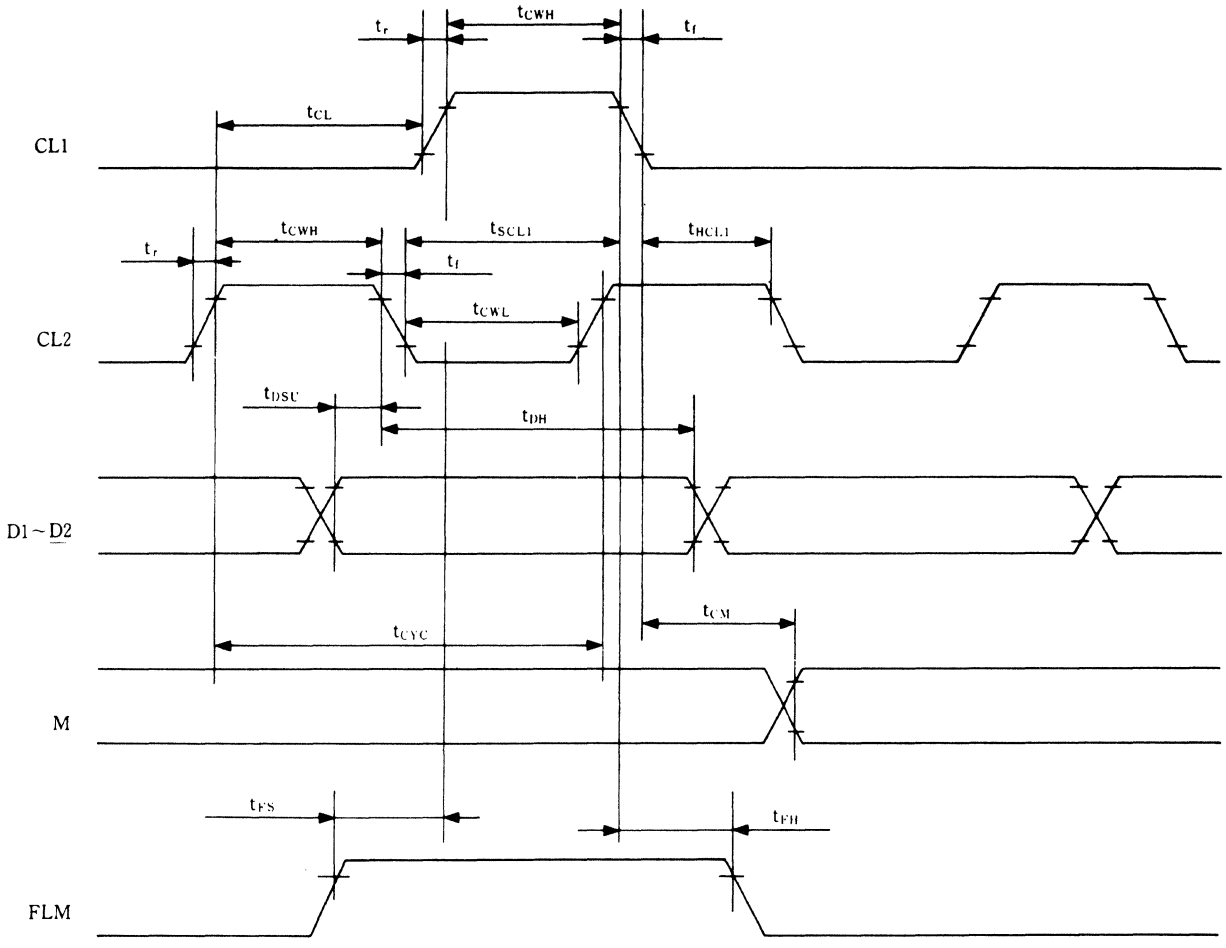


Fig. 7 Interface timing

LM238XB

- 240 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Controller LSI HD61830 is built-in (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size	180W x 120H x 13.8T (max.) mm
Effective display area	148W x 75.0H mm
Number of dots	240W x 128H dot
Dot size	0.50W x 0.50H mm
Dot pitch	0.55W x 0.55H mm
Weight	about 220 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	V_{SS}	V_{DD} V
Operating temperature (Ta) (Note 2)	0	~40°C
Storage temperature (Tstg) (Note 3)	−20	~60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, $V_{DD} - V_{SS}$ = 5.0V ±0.25V,
$V_{EE} - V_{SS}$ = −13.5V ±0.25V

Input "high" voltage (V_{IH})	2.2 V min.
Input "low" voltage (V_{IL})	0.8 V max.
Clock frequency (f_{CL2}) (Internal clock)	1.2 MHz max.
Input leak current (I_{IN})	−5 ~ 5 μA
Output leak current (I_{OUT})	−10 ~ 10 μA
Power consumption (V_{DD} = 5V, Ta = 25°C, $V_{DD} - V_0$ = 13.7V)	250 mW max.

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/64

Ta = 0°C	17.3 V typ.
Ta = 25°C	16.4 V typ.
Ta = 40°C	15.7 V typ.

OPTICAL DATA .See page 15.

Notes 1. Applied to CL1, CL2, D1 ~ D2, M, FLM.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Function
A1	V_{SS} (0V)	Ground
A2	V_{DD} (+5V)	Power supply for logic
A3	V_0	Power supply for LCD drive
A4	RS	Register select
A5	R/W	Read/write
A6	E	Enable
A7 ~ 14	DB0 ~ DB7	Data bus
A15	$\overline{CS}$	Chip select
A16	$\overline{RES}$	Reset
A17	V_{EE} (−13.5V)	Power supply
A18 ~ 20	N.C	No connection

Unit: mm

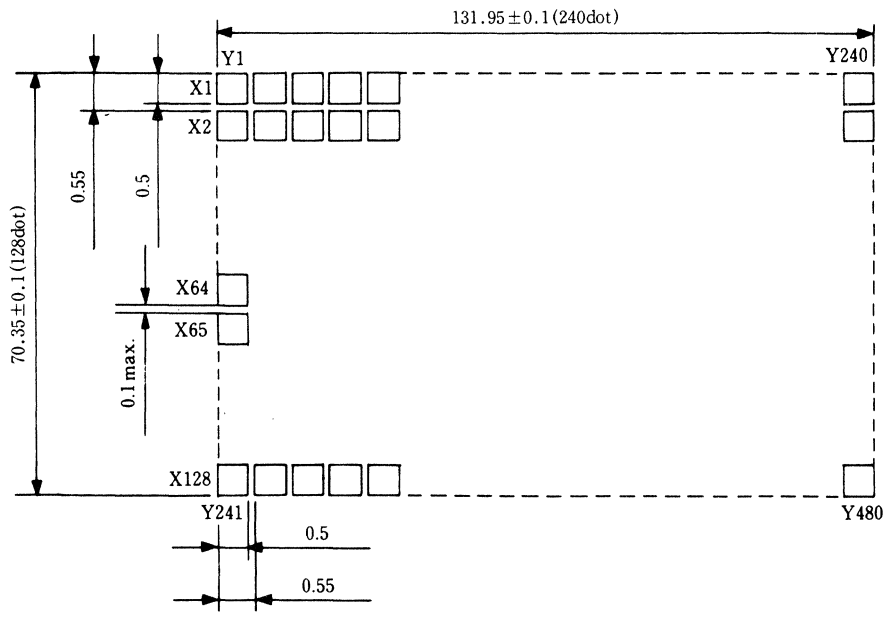
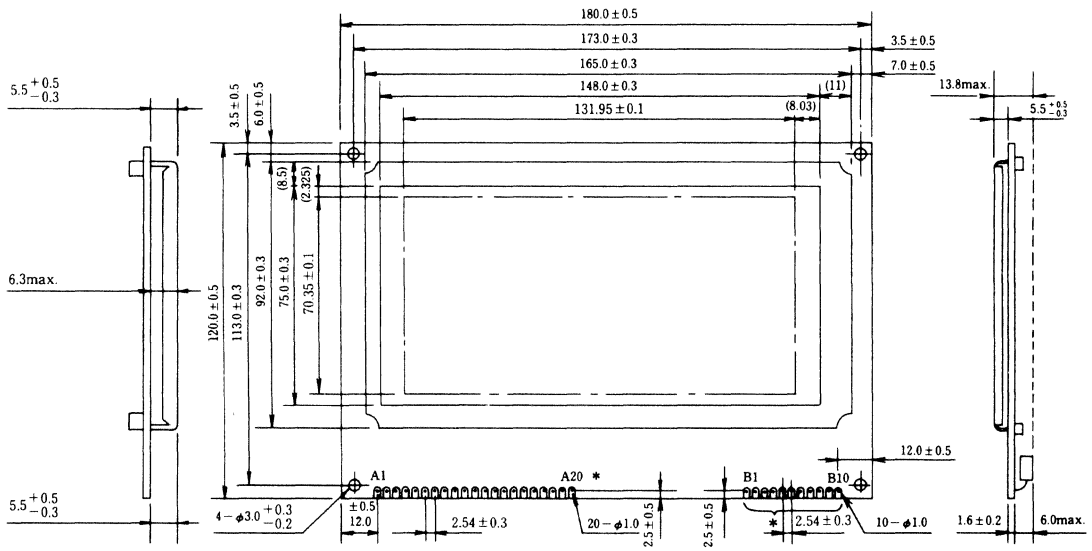


Fig. 1 Display pattern

HITACHI

Unit: mm



*B1 ~ B10 pads should not be used for LM238XB.
Do not connect any signals to these pads.
Use A1 ~ A20 for interface.

Fig. 2 External dimension

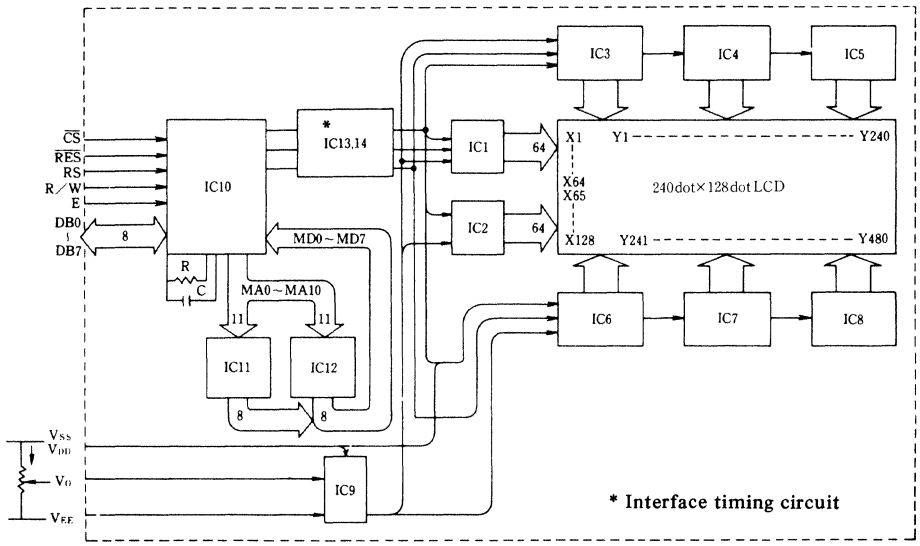


Fig. 3 Block diagram

$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

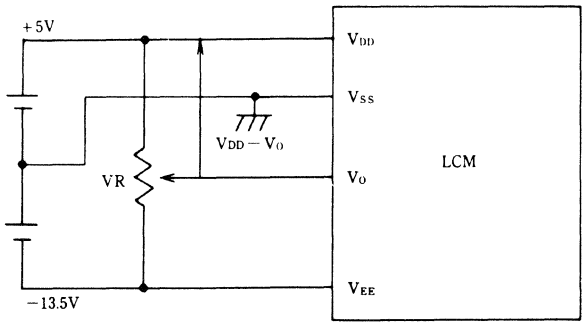


Fig. 4 Power supply

$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

SECTION 4

TIMING CHARACTERISTICS

Item		Symbol	Min.	Typ.	Max.	Unit
Enable cycle time		t_{CYC}	1.0	–	–	μs
Enable pulse width	H level	t_{WEH}	0.45	–	–	μs
	L level	t_{WEL}	0.45	–	–	μs
Enable rise time		t_{Er}	–	–	25	ns
Enable fall time		t_{Ef}	–	–	25	ns
CS, R/W, RS set up time		t_{AS}	140	–	–	ns
Data set up time		t_{DIS}	225	–	–	ns
Data delay time		t_{DD}	–	–	225	ns
Data hold time		t_H	10	–	–	ns
CS, R/W, RS →hold time		t_{AH}	10	–	–	ns

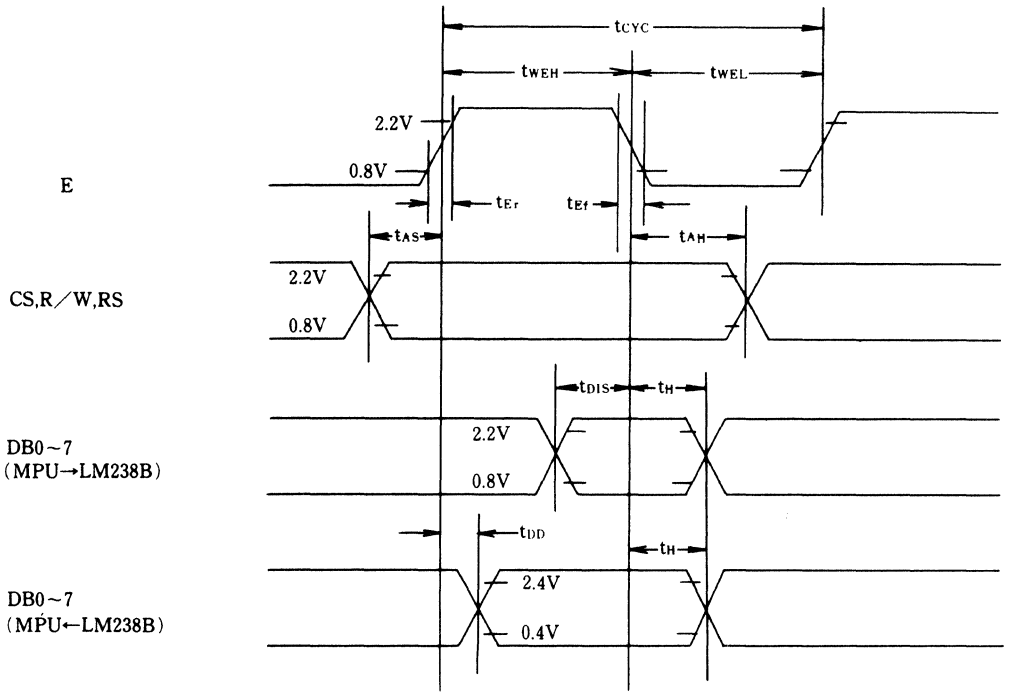


Fig. 5 Interface timing (MPU ↔ LM238B)

LM215XB

- 480 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830 (see section 6).
- Color tone: LM215XB . . . . . .yellowgreen

MECHANICAL DATA (Nominal dimensions)

Module size	270W x 110H x 11.5T (max.) mm
Effective display area	242W x 69H mm
Number of dots	480W x 128H dot
Dot size	0.43W x 0.43H mm
Dot pitch	0.48W x 0.48H mm
Weight	about 320 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} V
Operating temperature (Ta) (Note 2)	0	40°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V,
V_{EE} = −10.0 V ±0.25 V

Input "high" voltage (V_{IH}) (Note 1) . 0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) (Note 1) . . . . 0 ~ 0.3 x V_{DD} V
Clock frequency (f_{CL2}) . . . . . 1.08 MHz min.
1.15 MHz typ.
1.23 MHz max.

Power supply current (I_{DD}) . . . . . 6 mA typ.
(I_{EE}) . . . . . 3 mA typ.
(D_1 ~ D_4 = GND) (f_{CL2} = 1.15 MHz)
V_{DD} − V_0: 14.5

Power supply for LCD drive (Recommended)($V_{DD} - V_0$)
Duty = 1/64

Ta = 0°C . . . . . .15.5 V typ.
Ta = 25°C . . . . . .14.5 V typ.
Ta = 40°C . . . . . .14.0 V typ.

OPTICAL DATA . . . . . .See page 15.

Notes 1. Applied to CL1, CL2, D1 ~ D4, M, FLM.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (upper left half)
2	D2	H/L	Serial row data (lower left half)
3	FLM	H	The FLM signal indicates the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H→L	The CL1 latches the serial data in the shift registers
6	CL2	H→L	Clock signal for shifting the serial data
7	D3	H/L	Serial row data (upper right half)
8	D4	H/L	Serial row data (lower right half)
9	V_{DD}(+5V)	–	Power supply for logic circuit
10	V_{SS} (0V)	–	Ground
11	VEE(−10V)	–	Power supply for LC driving
12	V_O	–	Operating voltage for LC driving

Unit: mm

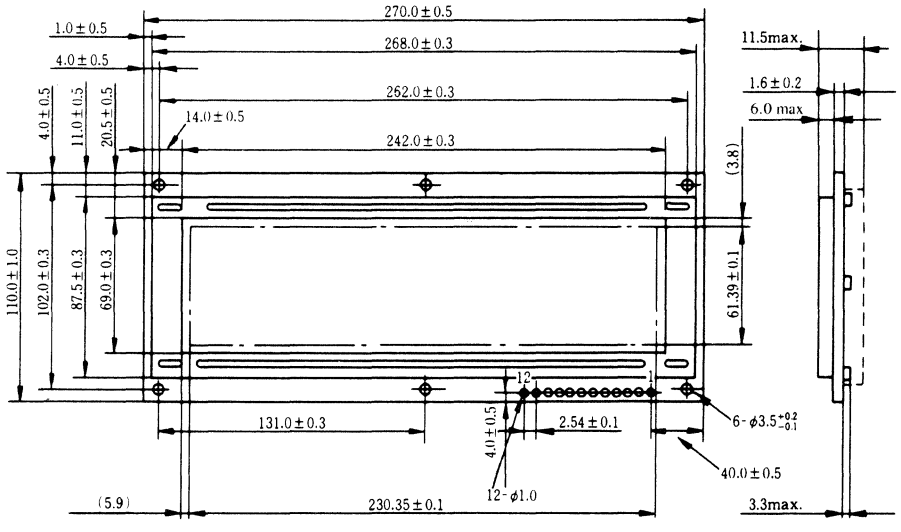


Fig. 1 External dimension

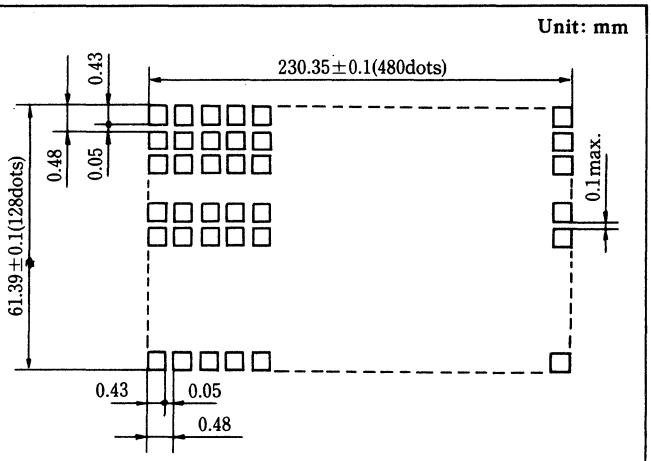


Fig. 2 Display pattern

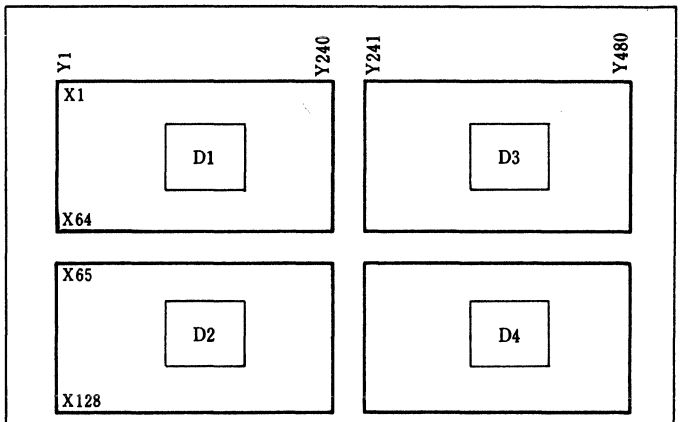
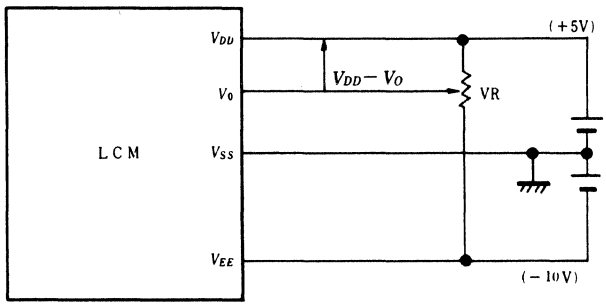
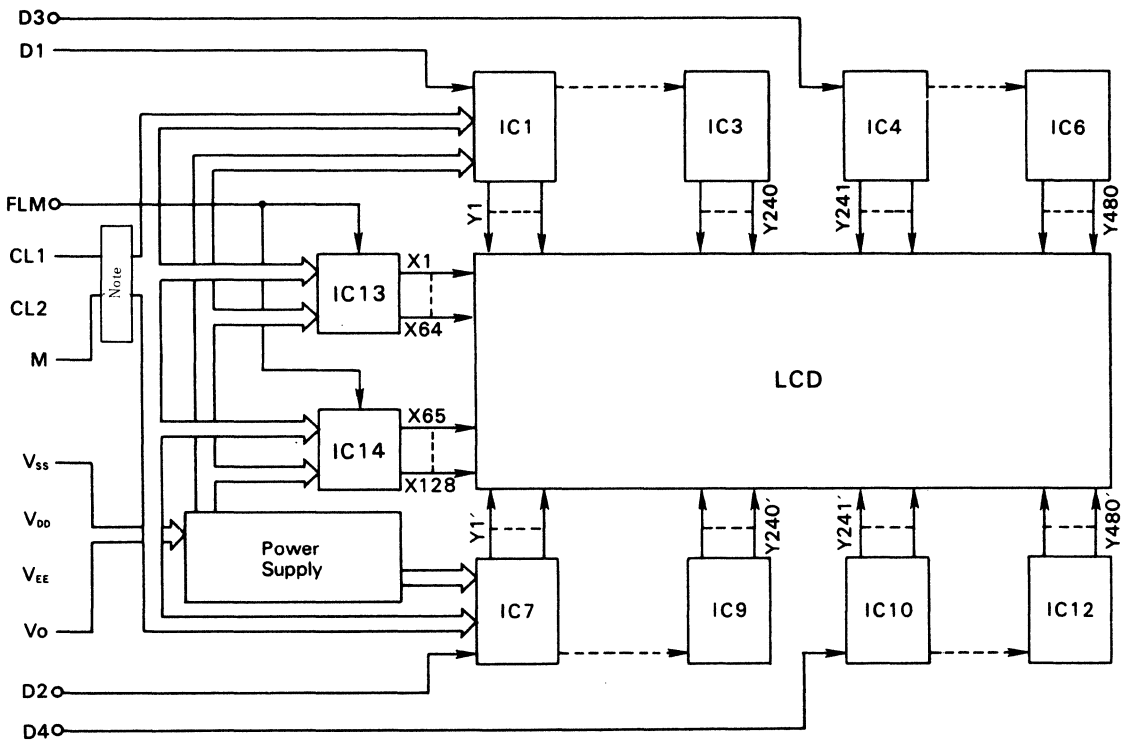


Fig. 3 Correspondence of display with data



V_{DD}-V_O: Operating voltage for LC driving
VR: 10 kΩ ~ 20 kΩ

Fig. 4 Power supply



Note: Interface timing circuit

Fig. 5 Block diagram

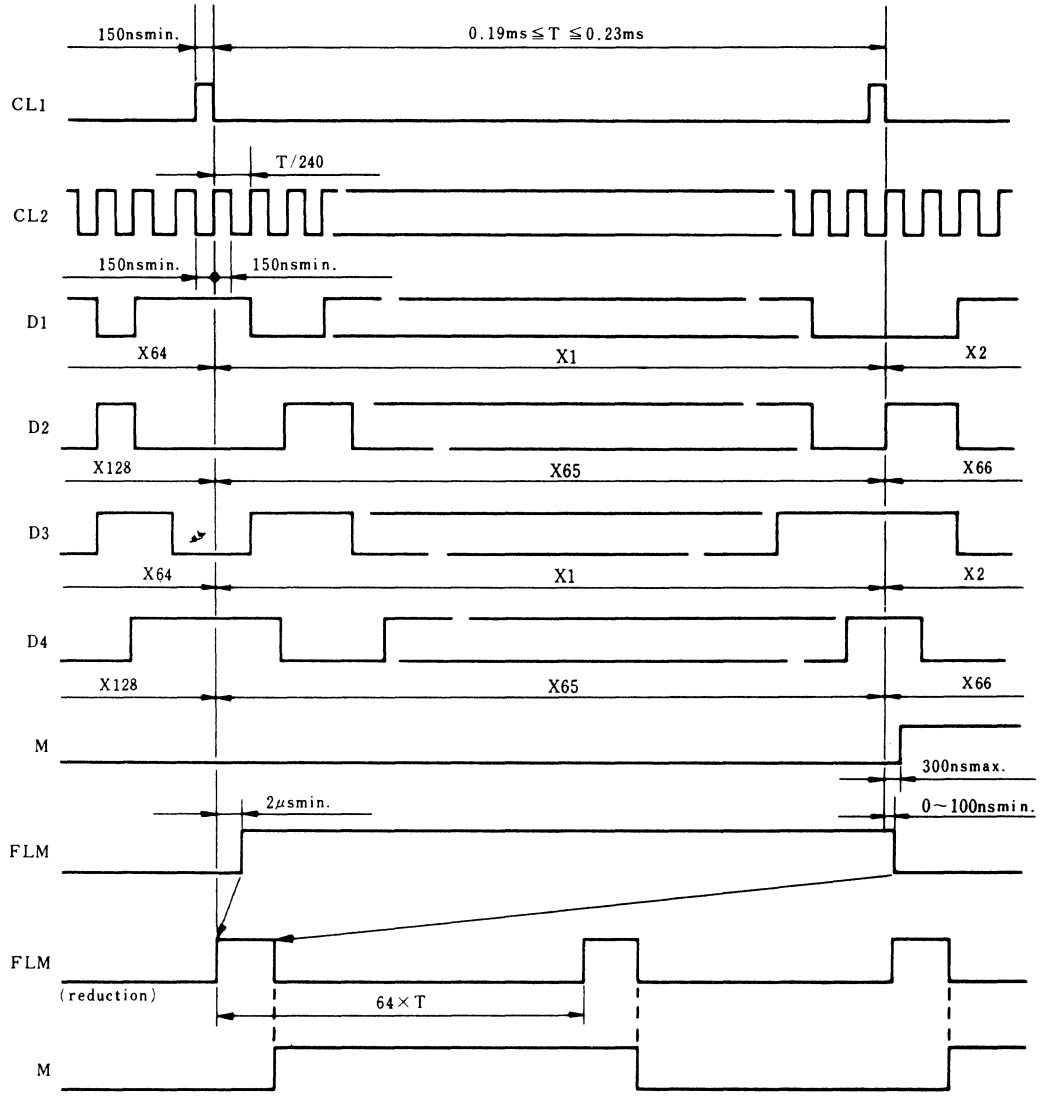


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	810	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	100	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

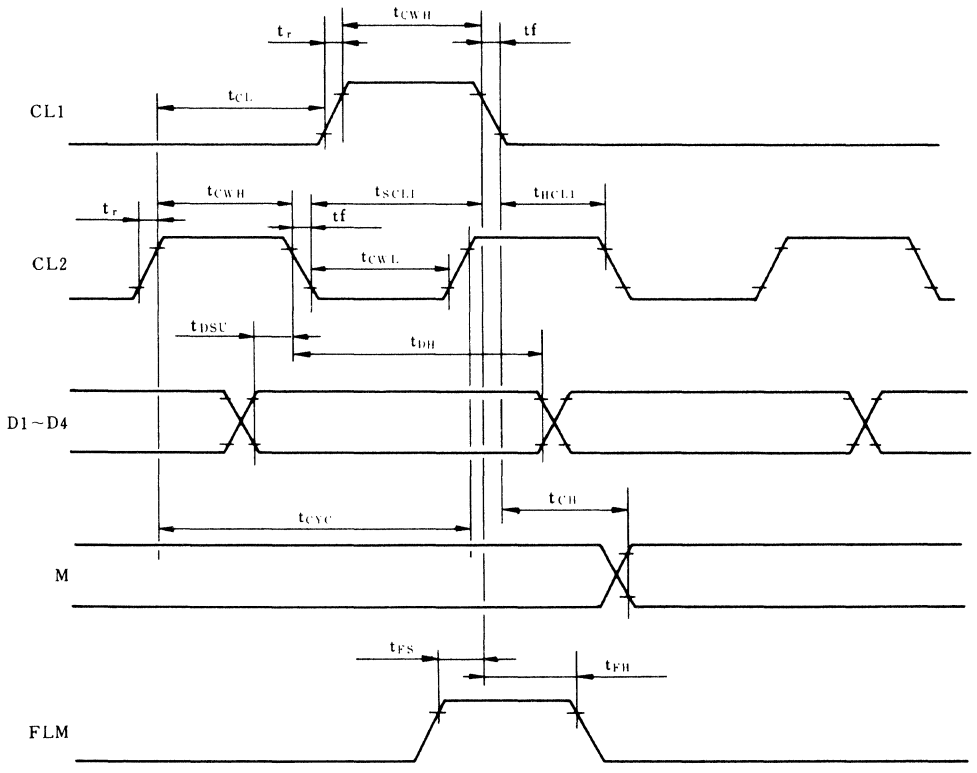


Fig. 7 Interface timing

LM224XB

- 480 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830B (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 270W x 110H x 11.5T (max.) mm
Effective display area . . . . . 242W x 69H mm
Number of dots . . . . . 480W x 128H dot
Dot size . . . . . 0.43W x 0.43H mm
Dot pitch . . . . . 0.48W x 0.48H mm
Weight . . . . . about 320 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$) . . .	0	19.0 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} V
Operating temperature (Ta) (Note 2)	0	40°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, $V_{DD} - V_{SS}$ = 5.0 V ±0.25 V,
$V_{EE} - V_{SS}$ = 11.0 V ±0.5 V
Input "high" voltage (V_{IH}) . . . . . 0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) . . . . . 0 ~ 0.3 x V_{DD} V
Clock frequency (f_{CL2}) . . . . . 2.15 MHz min.
2.30 MHz typ.
2.40 MHz max.
Power supply current (I_{DD}) . . . . . 10 mA typ.
(I_{EE}) . . . . . 3 mA typ.
(D_1, D_2 = GND) (f_{CL2} = 2.30 MHz) ($V_{DD} - V_0$ = 16.0V)
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/64
Ta = 0°C . . . . . 15.5 V typ.
Ta = 25°C . . . . . 14.5 V typ.
Ta = 40°C . . . . . 14.0 V typ.

OPTICAL DATA . . . . . See page 15.

Notes 1. Applied to CL1, CL2, D1, D2, M, FLM.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Data signal
2	D2	H/L	Data signal
3	FLM	H	The FLM signal indicates the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H→L	The CL1 latches the serial data in the shift registers
6	CL2	H→L	Clock signal for shifting the serial data
7	NC	–	
8	NC	–	
9	V_{DD}	–	Power supply for logic circuit
10	V_{SS}	–	Ground
11	V_{EE}	–	Power supply for LC driving
12	V_O	–	Operating voltage for LC driving

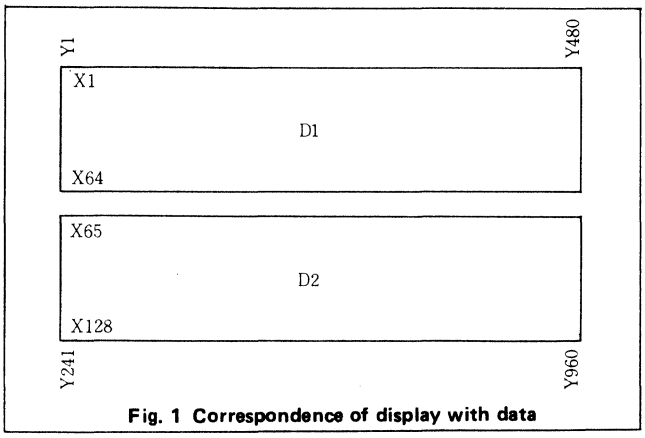


Fig. 1 Correspondence of display with data

Unit: mm

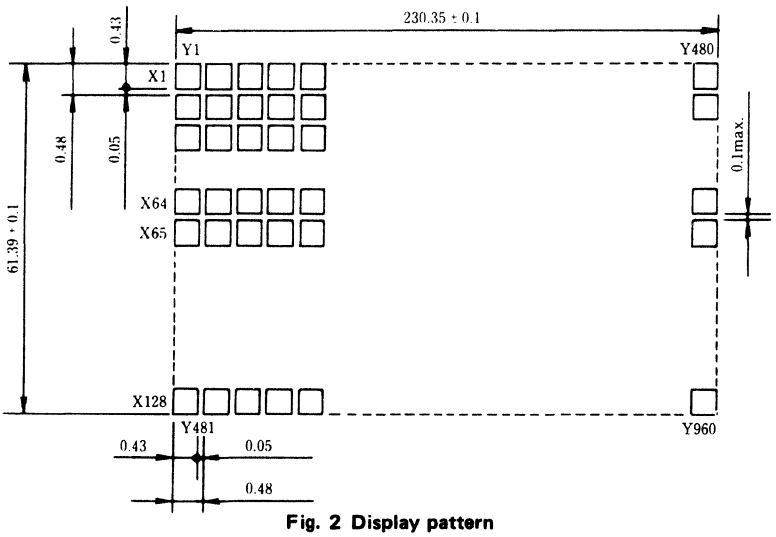


Fig. 2 Display pattern

SECTION 4

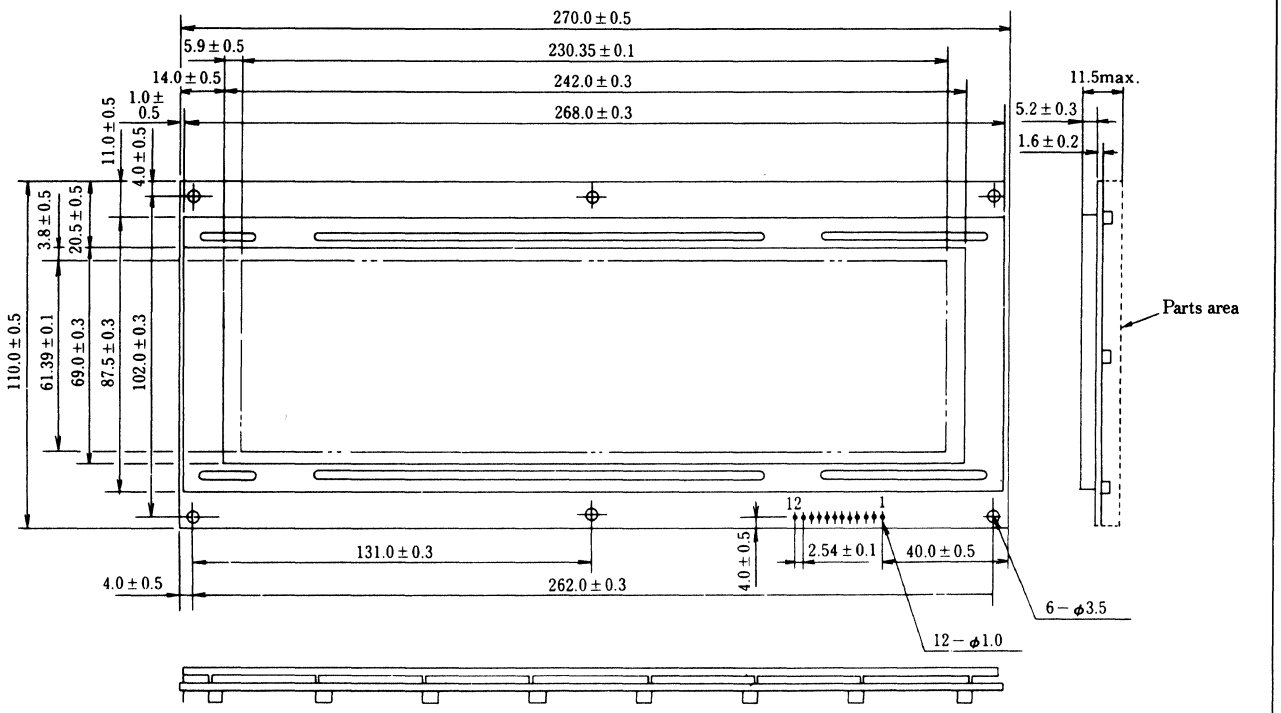


Fig. 3 External dimension

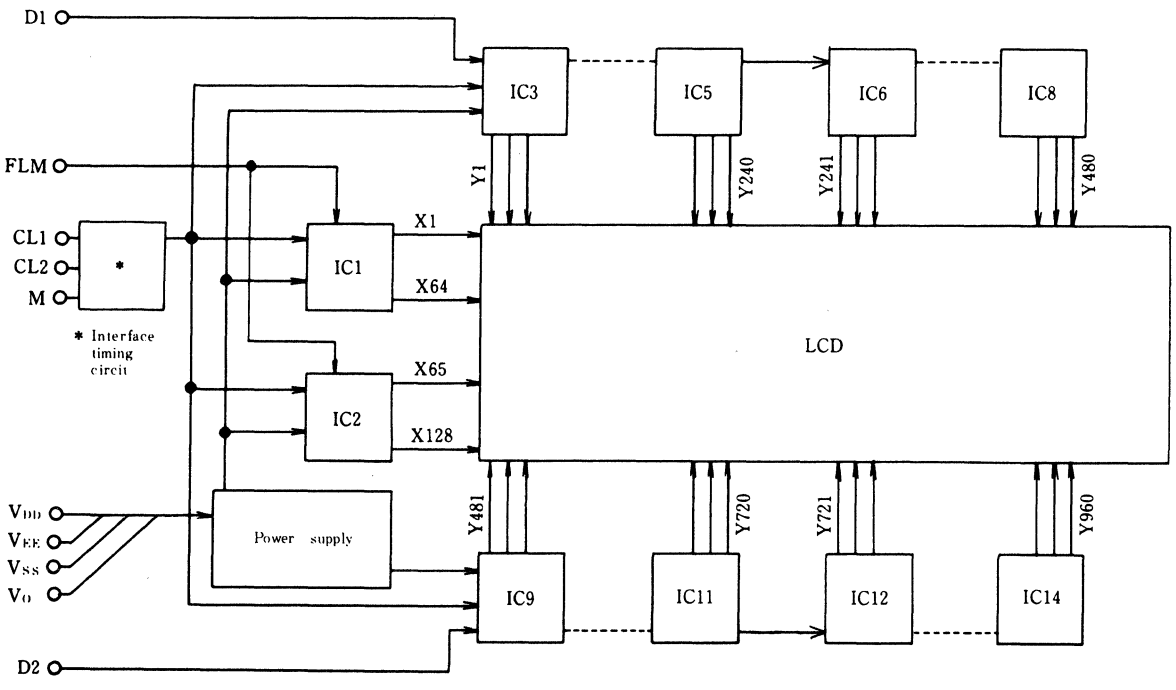


Fig. 4 Block diagram

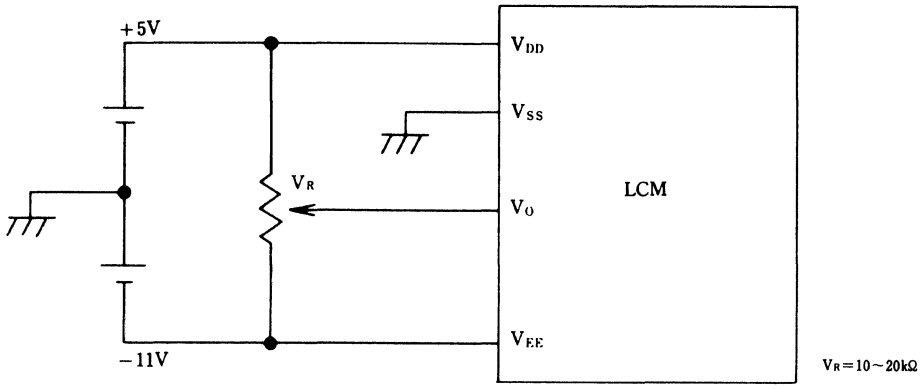


Fig. 5 Power supply

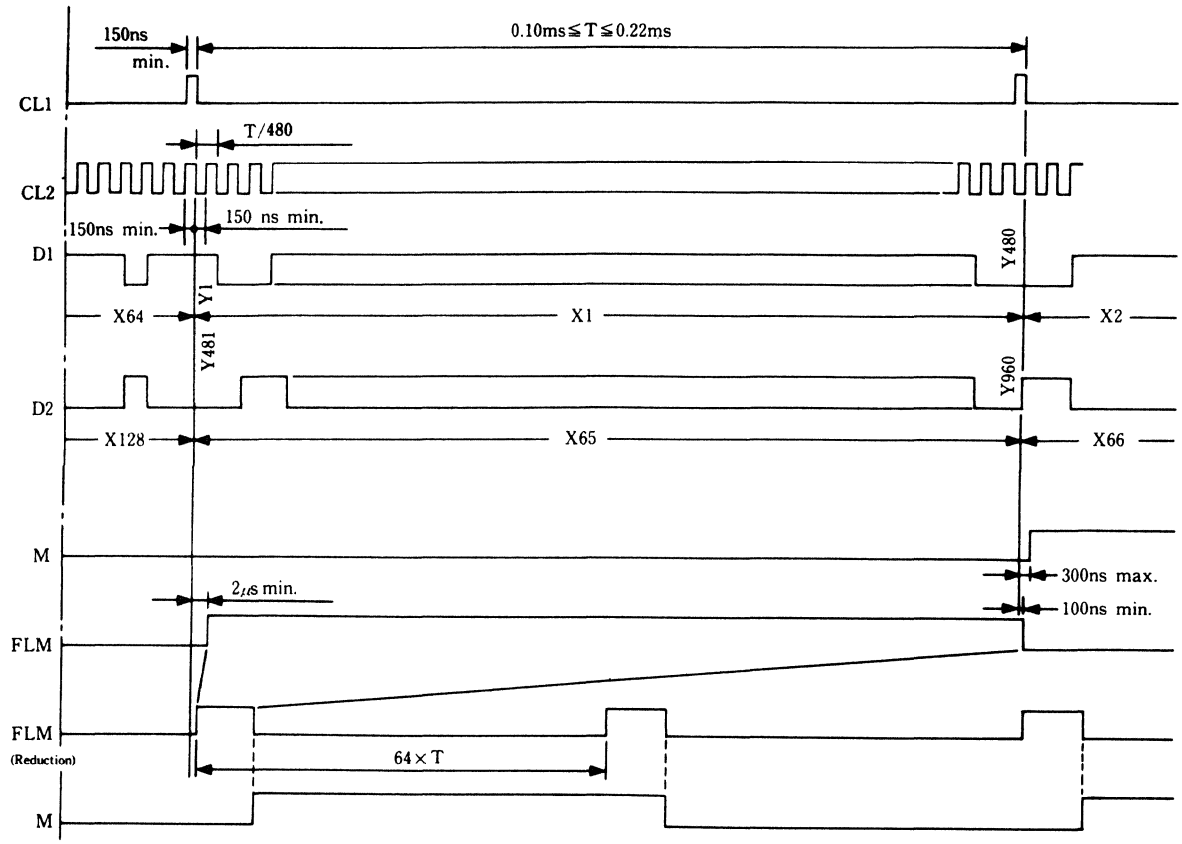


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	417	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

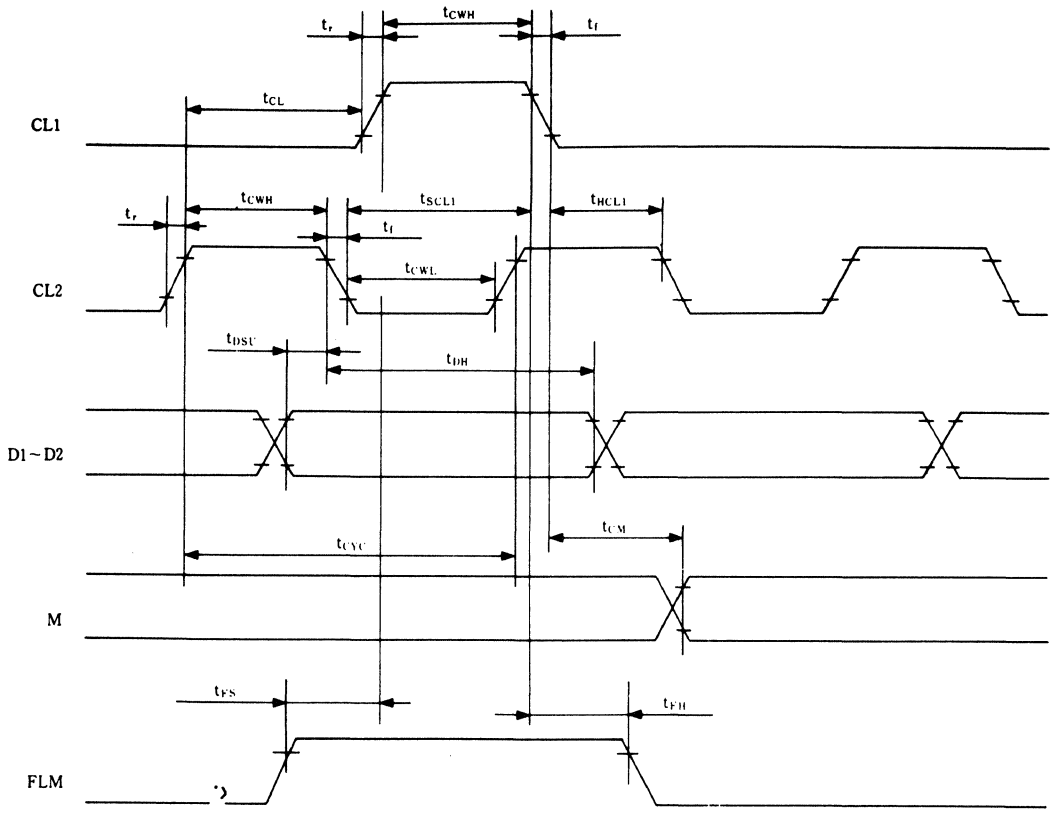


Fig. 7 Interface timing

LM240S

- 480 dot (W) x 128 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: MSM6255GSK or MSM6265GSK

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 270W x 110H x 11.5T (max.) mm
Effective display area . . . . . 242W x 69H mm
Number of dots . . . . . 480W x 128H dot
Dot size . . . . . 0.43W x 0.43H mm
Dot pitch . . . . . 0.48W x 0.48H mm
Weight . . . . . about 320 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	22 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V,
V_{EE} = −14.5 V ±0.5 V

Input "high" voltage (V_{IH}) . . . . . 0.8 x V_{DD} V min.
Input "low" voltage (V_{IL}) . . . . . 0.2 x V_{DD} V max.
Clock frequency (f_{CP}) . . . . . 1.00 MHz min.
1.07 MHz typ.
1.15 MHz max.
Power supply current (I_{DD}) . . . . . 10 mA typ.
(I_{EE}) . . . . . 8 mA typ.
(D_1, D_2 = GND) (f_{CP} = 1.07 MHz) ($V_{DD} - V_0$ = 15.8V)
(D_3, D_4 = GND)
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/128
Ta = 0°C . . . . . 17.1 V typ.
Ta = 25°C . . . . . 15.8 V typ.
Ta = 40°C . . . . . 14.6 V typ.

OPTICAL DATA . . . . . .See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D0	H/L	Serial row data
2	D1	H/L	Serial row data
3	FRAME	H	Frame frequency (Indicating the beginning of each display cycle)
4	N C	–	–
5	LOAD	H/L	The CL1 latches the serial data in the shift registers
6	CP	H/L	Clock signal for shifting the serial data
7	D2	H/L	Serial row data
8	D3	H/L	Serial row data
9	V_{DD}	–	Power supply for logic circuit
10	V_{SS}	–	Ground
11	V_{EE}	–	Power supply for LC driving
12	V_0	–	Operating voltage for LC driving
13	ECLK	H/L	Enable clock
14	N C	–	–
15	N C	–	–

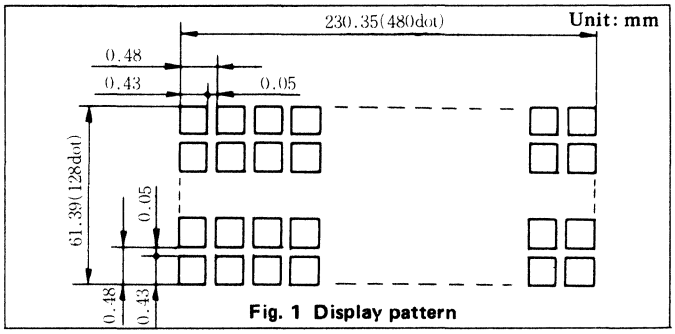


Fig. 1 Display pattern

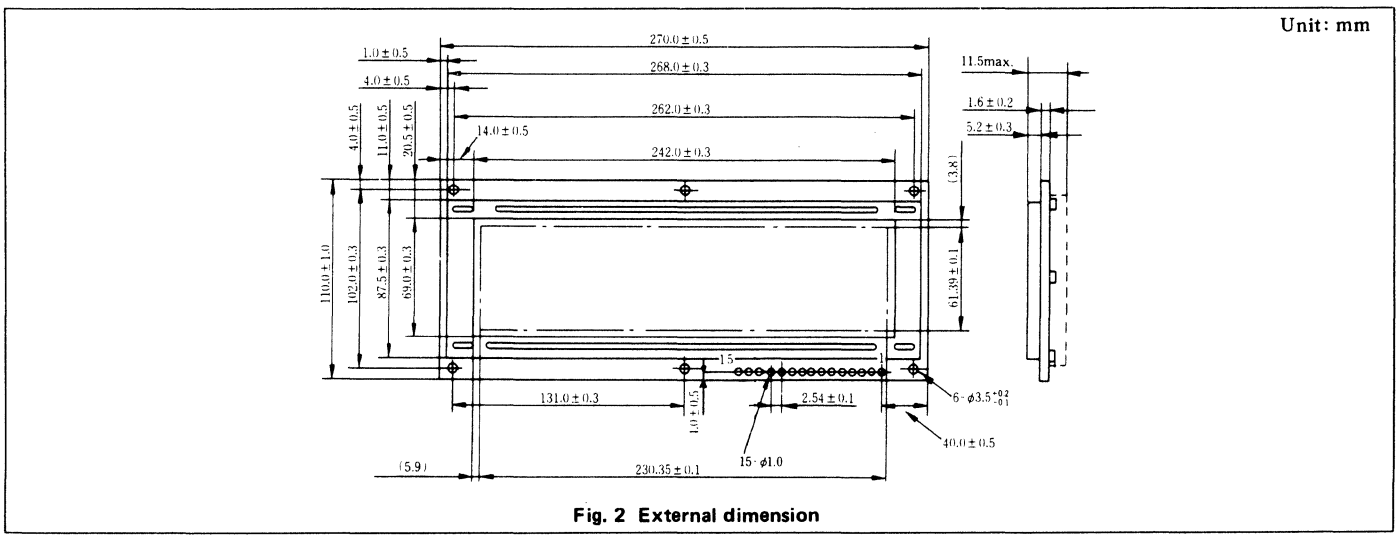


Fig. 2 External dimension

SECTION 4

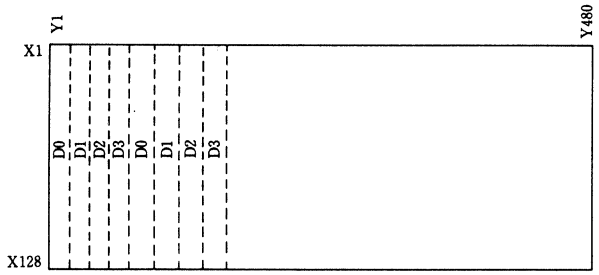


Fig. 3 Correspondence of display with data

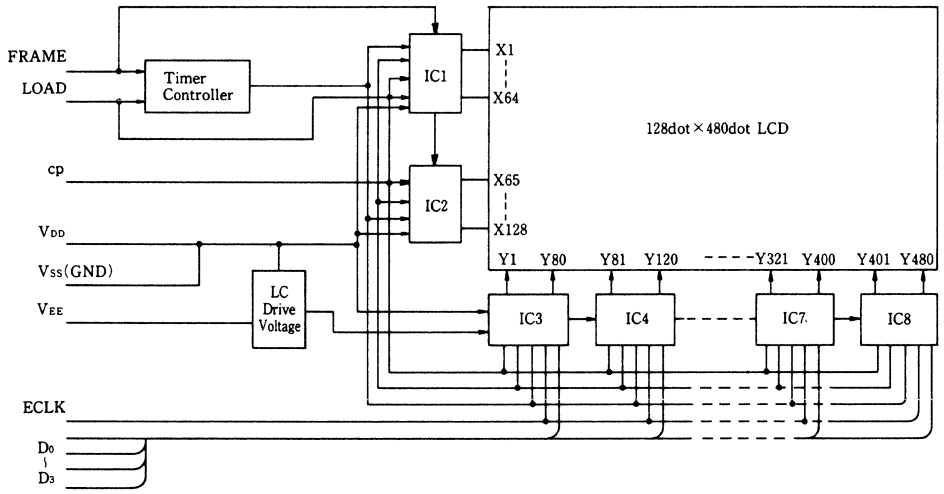
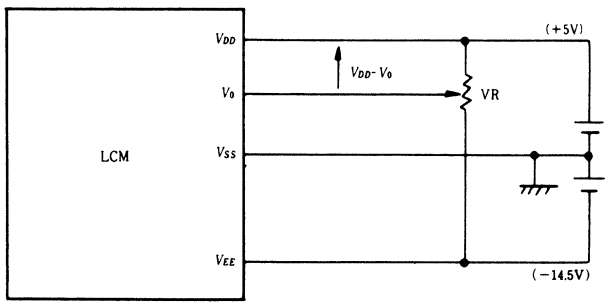
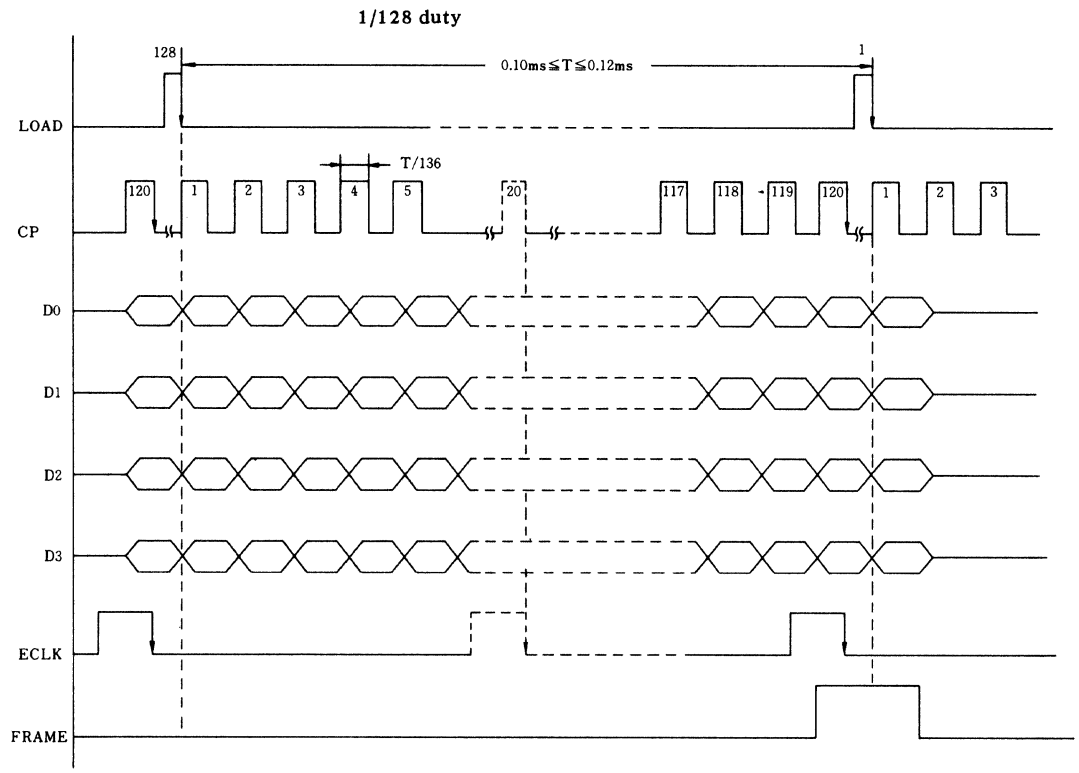


Fig. 4 Block diagram



V_{DD} ~ V_0 : Operating voltage for LC driving
VR: 10kΩ ~ 20kΩ

Fig. 5 Power supply



Notes 1. When using control LSI MSM6255GSK.
2. There is CP pulse interrupting time of sixteen pulses between CP (120) and CP (1).

Fig. 6 Interface timing

TIMING CHARACTERISTICS

(V_{DD} = 5V ± 10%, Ta = −20 ~ +85°C, CL = 15μF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" delay time	t_{PLH} t_{PHL}	–	–	–	200	ns
Maximum clock frequency	f_{CP}	DUTY = 50%	–	–	1.3	MHz
CP ECLK pulse width	t_W	–	125	–	–	ns
LOAD pulse width	$t_{W\ (L)}$	–	125	–	–	ns
Set up time	t_{setup}	–	100	–	–	ns
CP → LOAD time	t_{CL}	–	250	–	–	ns
LOAD → CP time	t_{LC}	–	0	–	–	ns
Hold time	t_{hold}	–	100	–	–	ns
Rise, fall time	t_r t_f	–	–	–	50	ns
LOAD rise, fall time	$t_{r\ (L)}$ $t_{f\ (L)}$	–	–	–	1	μs
CP → ECLK time	t_{CE}	–	0	–	–	ns
ECLK → CP time	t_{EC}	–	150	–	–	ns

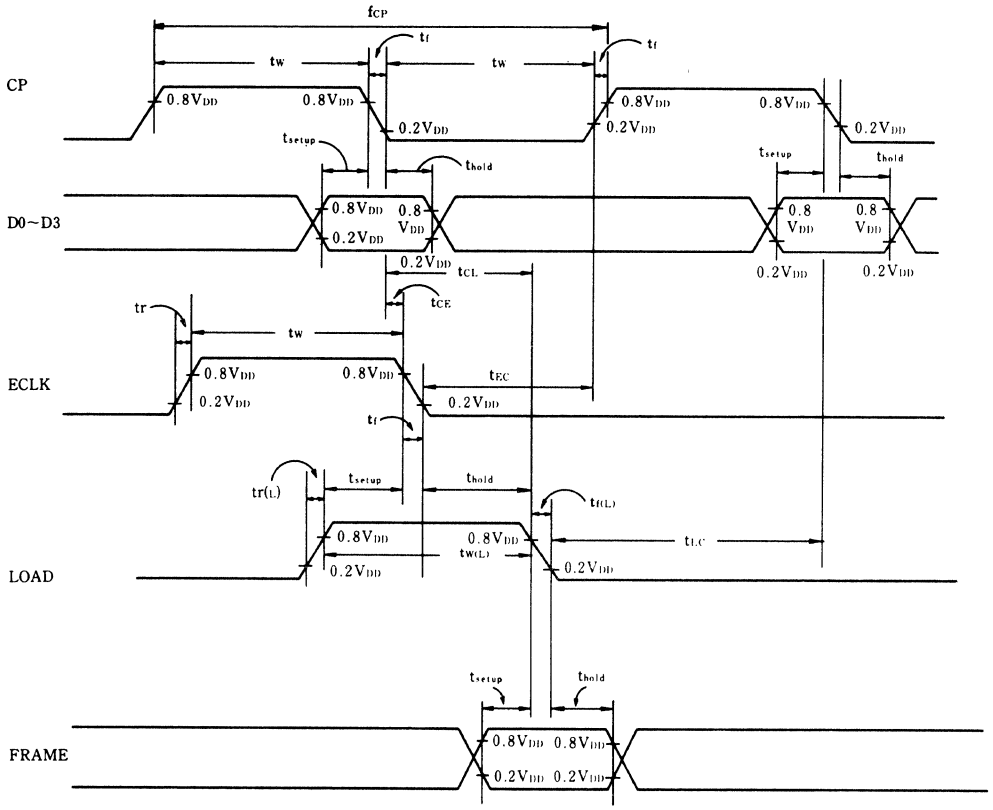


Fig. 7 Interface timing

LM225X

- 640 dot (W) x 200 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD61830B (see section 6).
- Color tone: LM225X . . . . . .yellowgreen

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 270W x 150H x 13.0T (max.) mm
Effective display area . . . . . 239W x 104H mm
Number of dots . . . . . 640W x 200H dot
Dot size . . . . . 0.32W x 0.46H mm
Dot pitch . . . . . 0.35W x 0.49H mm
Weight . . . . . about 450 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	19.0 V
Input voltage (Vi) (Note 1)	V_{SS}	V_{DD} V
Operating temperature (Ta) (Note 2)	0	40°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, $V_{DD} - V_{SS}$ = 5.0 V ±0.25 V,
$V_{EE} - V_{SS}$ = −13.5 V ±0.25 V
Input "high" voltage (V_{IH}) . . . . . 0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) . . . . . 0 ~ 0.3 x V_{DD} V
Clock frequency (f_{CL2}) . . . . . 2.13 MHz min.
2.28 MHz typ.
2.46 MHz max.
Power supply current (I_{DD}) . . . . . 6 mA typ.
(I_{EE}) . . . . . 3 mA typ.
(D_1, D_2 = GND) (f_{CL2} = 2.28 MHz) ($V_{DD} - V_0$ = 14.0V)
(D_3, D_4 = GND)
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/100

Ta = 0°C . . . . . .16.7 V typ.
Ta = 25°C . . . . . .15.8 V typ.
Ta = 40°C . . . . . .15.2 V typ.

OPTICAL DATA . . . . . See page 15.

Notes 1. Applied to CL1, CL2, D1 ~ D4, M, FLM.
2. When operated at maximum temperature, the display may be changed into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data (upper left half)
2	D2	H/L	Serial row data (lower left half)
3	FLM	H	The FLM signal indicates the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H→L	The CL1 latches the serial data in the shift registers
6	CL2	H→L	Clock signal for shifting the serial data
7	D3	H/L	Serial row data (upper right half)
8	D4	H/L	Serial row data (lower right half)
9	V_{DD}	–	Power supply for logic circuit
10	V_{SS}	–	Ground
11	V_{EE}	–	Power supply for LC driving
12	V_O	–	Operating voltage for LC driving

Unit: mm

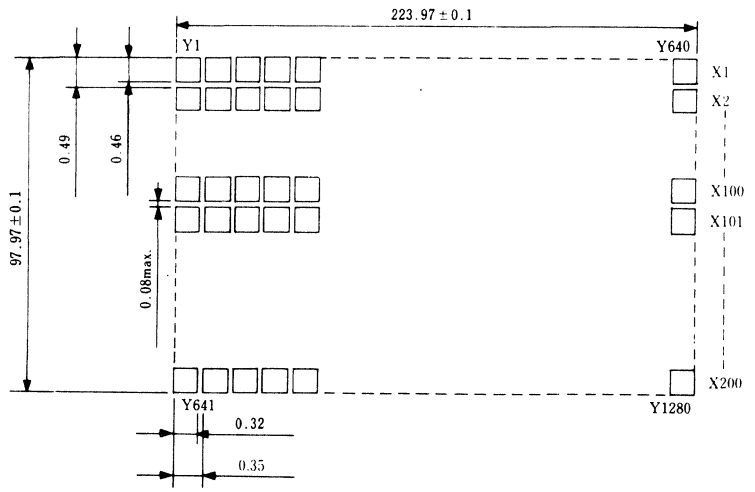


Fig. 1 Display pattern

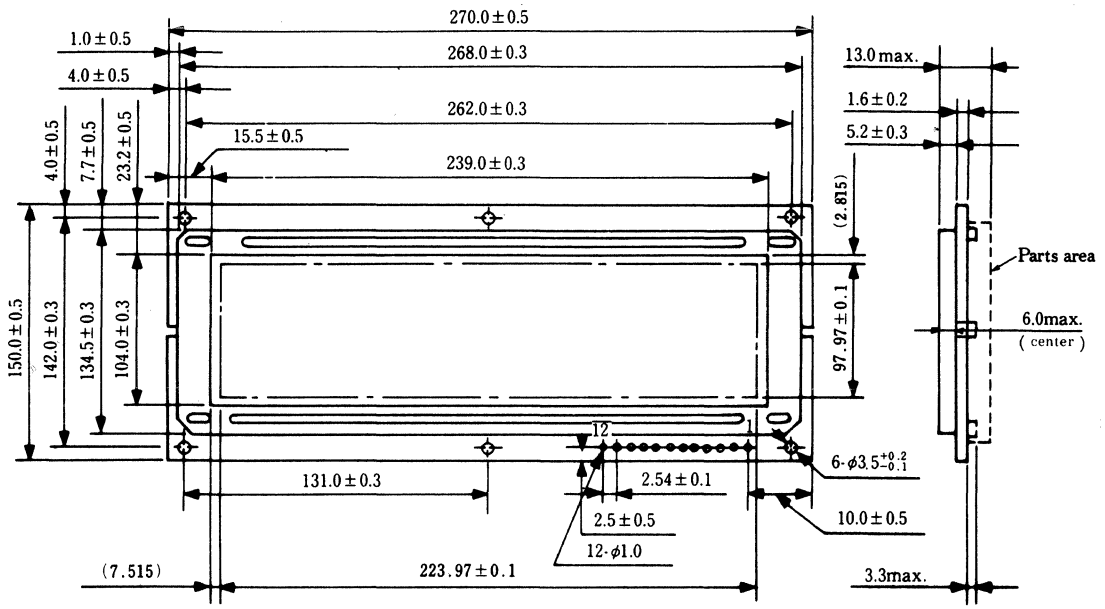


Fig. 2 External dimension

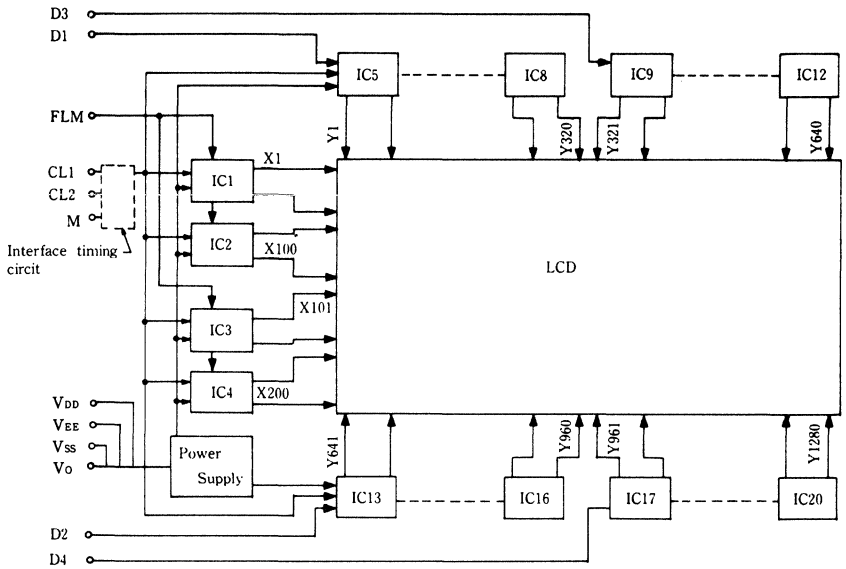


Fig. 3 Block diagram

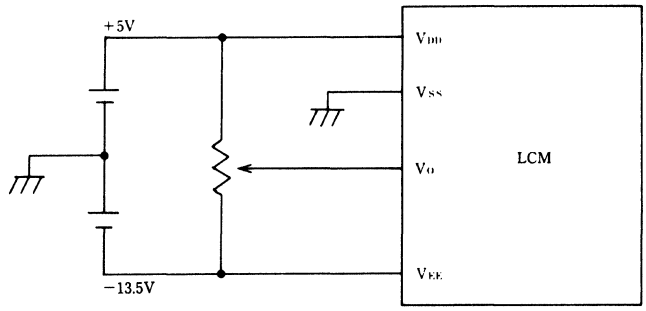


Fig. 4 Power supply

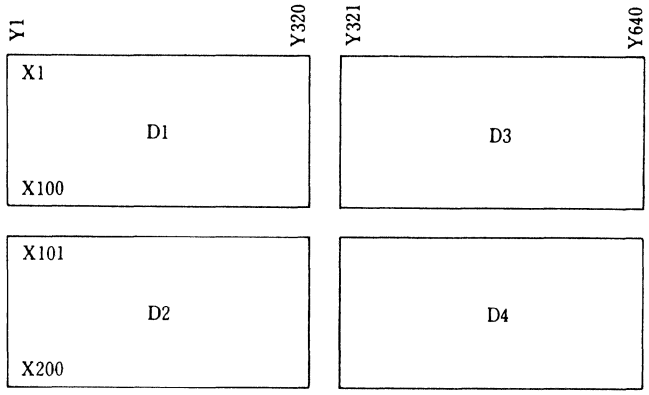


Fig. 5 Correspondence of display with data

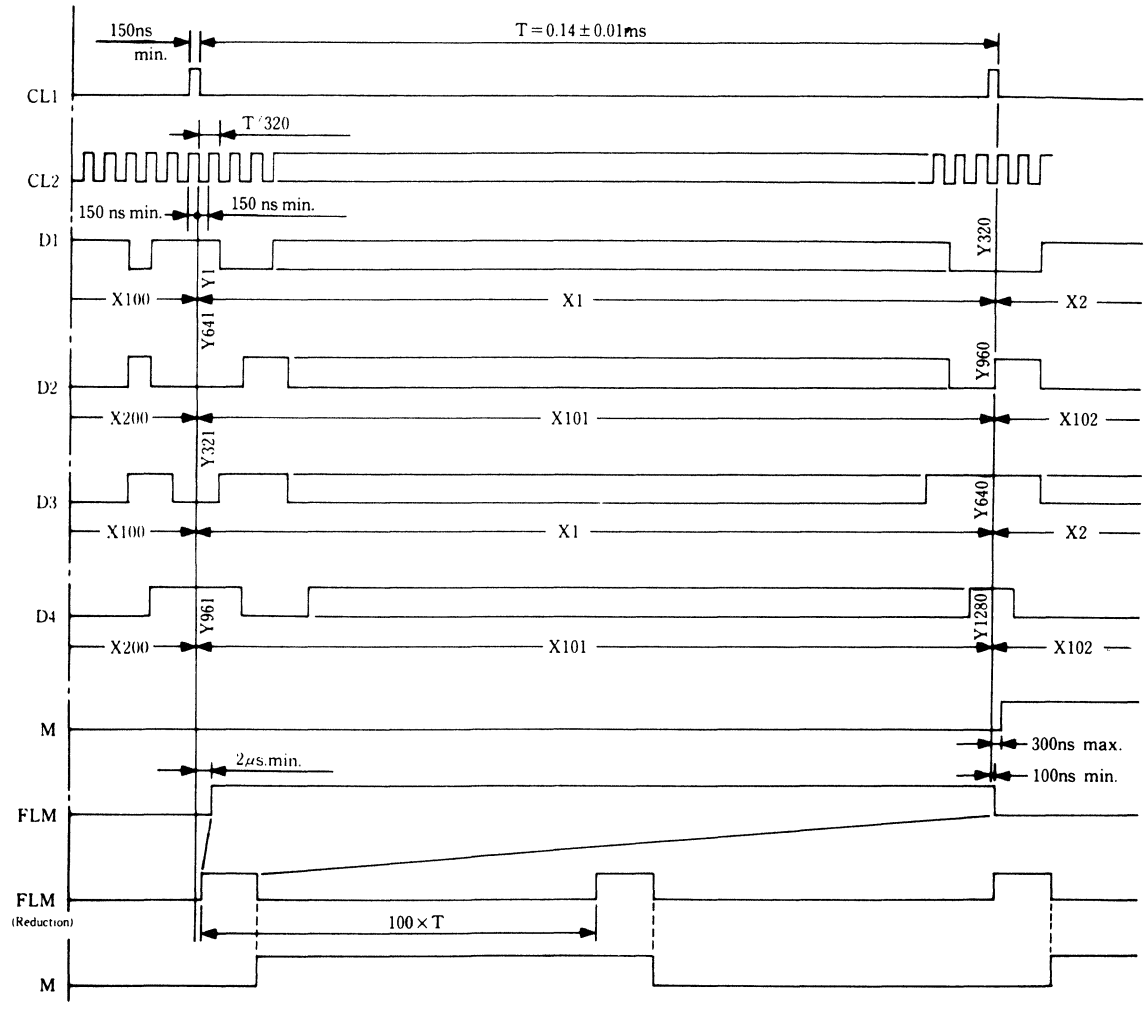


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	400	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	100	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

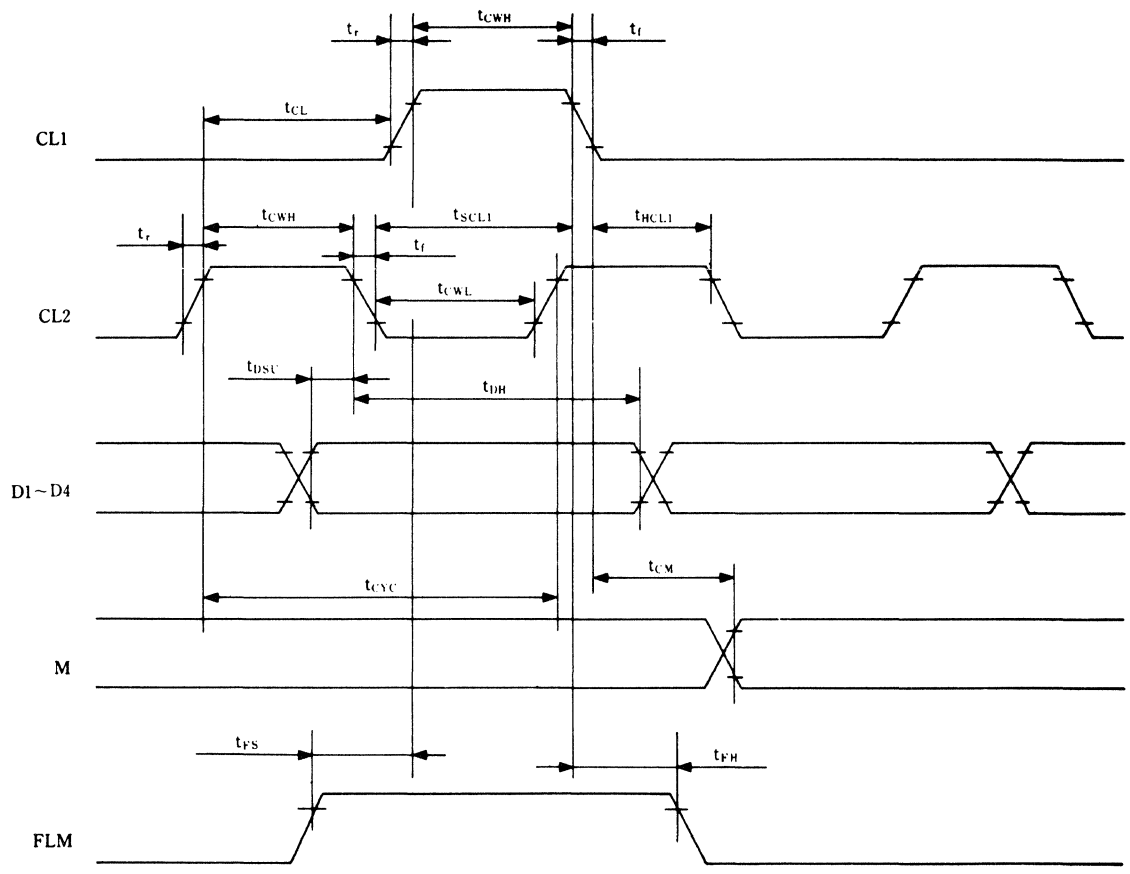


Fig. 7 Interface timing

LM236XB

- 640 dot (W) x 200 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: MSM6255GSK or MSM6265GSK
- Color tone: LM236XB . . . . . Yellowgreen

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 270W x 149H x 13.0T (max.) mm
Effective display area . . . . . 239W x 104H mm
Number of dots . . . . . 640W x 200H dot
Dot size . . . . . 0.32W x 0.46H mm
Dot pitch . . . . . 0.35W x 0.49H mm
Weight . . . . . about 450 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic (V_{DD})	0	6.5 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	22 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD}+0.3V
Operating temperature (Ta) (Note 2)	0	40°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V,
V_{EE} = −14.5 V ±0.5 V

Input "high" voltage (V_{IH}) (Note 1) . 0.8 x V_{DD} ~ V_{DD}V
Input "low" voltage (V_{IL}) (Note 1) . . . . 0 ~ 0.2 x V_{DD}V
Power supply current (I_{DD}) (Note 4) . . . . . 5 mA typ.
(I_{EE}) (Note 4) . . . . . 4 mA typ.
Frame frequency (f_{FRAME}) . . . . . 70 Hz min.
75 Hz typ.
80 Hz max.
Input capacitance (C_{in}) (f_{CP} = 1 MHz) . . . . . 150 pF typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
(Note 5) Duty = 1/100

Ta = 0°C . . . . . .16.7 V typ.
Ta = 25°C . . . . . .15.8 V typ.
Ta = 40°C . . . . . .15.2 V typ.

OPTICAL DATA . . . . . See page 15.

Notes 1. Applied to FRAME, LOAD, DF, ECLK, CP, UD0 ~ UD3, LD0 ~ LD3.
2. When operated at maximum temperature, the display may change into blue color.
It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. When viewing angle is 25°.
5. In case of V_{DD} = +5V, $V_{DD} - V_0$ = 15V, DF = 75 Hz, UD0 ~ UD3 = V_{SS} and LD0 ~ LD3 = V_{SS}.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1 ~ 4	UD0 ~ UD3	H/L	Data (upper half)
5	ECLK	H	Chip enable clock
6	FRAME	H	Frame frequency (Indicating the beginning of each display cycle)
7	DF	H/L	Control signal for AC driving
8	LOAD	H→L	Data latch
9	CP	H→L	Data shift
10 ~ 13	LD0 ~ LD3	H/L	Data (lower half)
14	V_{DD}	—	Power supply for logic circuit
15	V_{SS}	—	Ground
16	V_{EE}	—	Power supply for LC driving
17	V_0	—	Operating voltage for LC driving

SECTION 4

Unit: mm

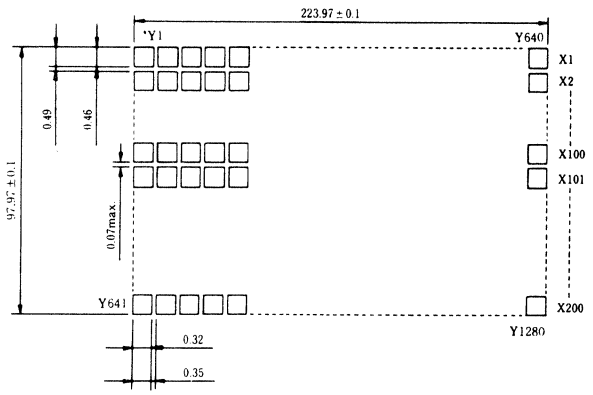
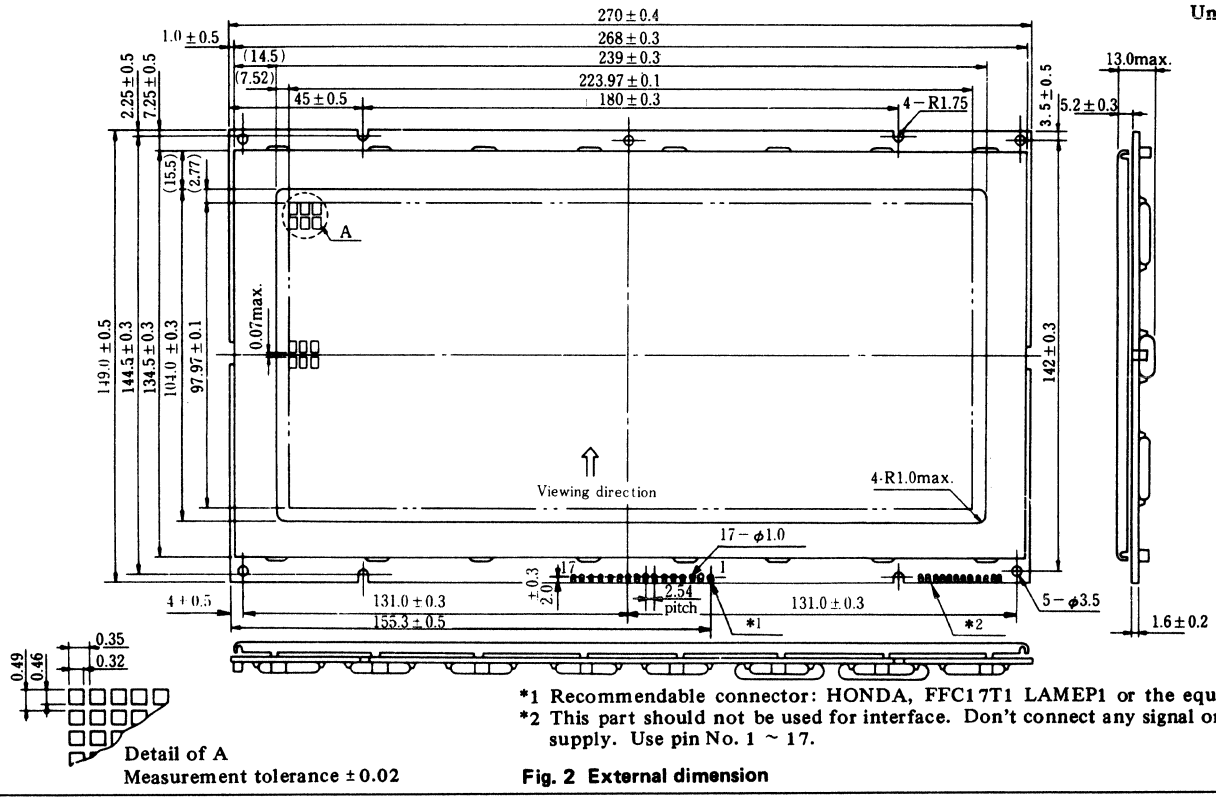
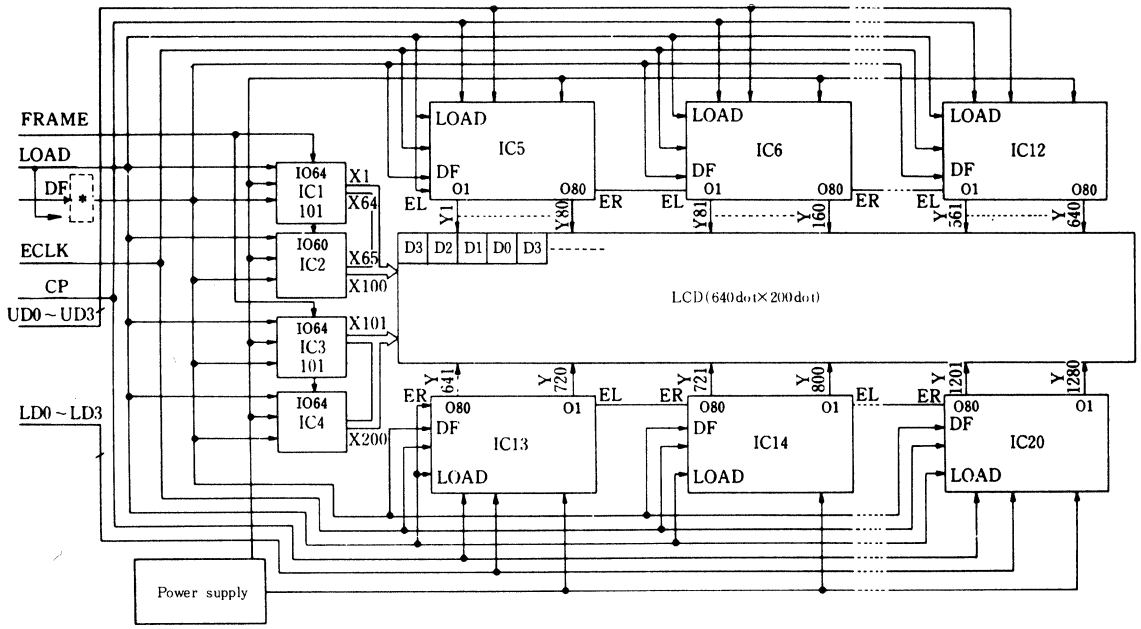


Fig. 1 Display pattern



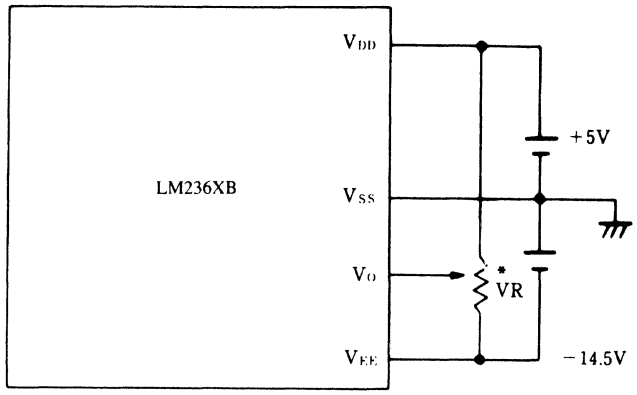
*1 Recommendable connector: HONDA, FFC17T1 LAMEP1 or the equivalent.
*2 This part should not be used for interface. Don't connect any signal or power supply. Use pin No. 1 ~ 17.

Fig. 2 External dimension



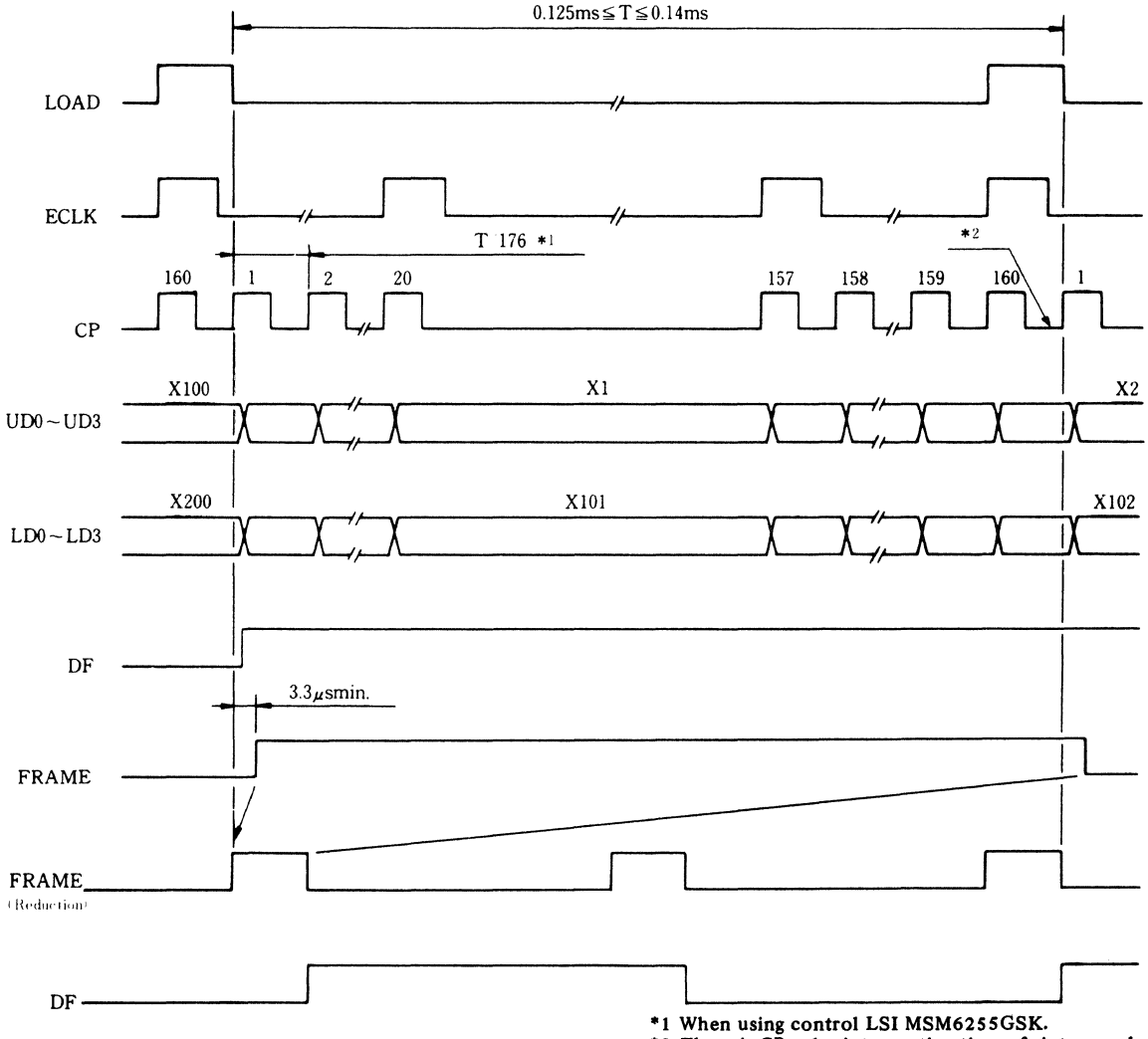
*. ⬚ Interface timing circuit

Fig. 3 Block diagram



* VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply



*1 When using control LSI MSM6255GSK.
*2 There is CP pulse interrupting time of sixteen pulse between CP (160) and CP (1).

Fig. 5 Interface timing

TIMING CHARACTERISTICS

(V_{DD} = 5V ±10%, Ta = −20 ~ +85°C, CL = 15 μF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" delay time	t_{PLH} t_{PHL}	–	–	–	200	ns
Frequency of maximum clock	f_{CP}	DUTY = 50%	–	–	1.41	MHz
CP ECLK pulse width	t_W	–	125	–	–	ns
LOAD pulse width	t_W (L)	–	125	–	–	ns
Set up time	t_{setup}	–	100	–	–	ns
CP →LOAD time	t_{CL}	–	250	–	–	ns
LOAD →CP time	t_{LC}	–	0	–	–	ns
Hold time	t_{hold}	–	100	–	–	ns
Rise, Fall time	t_r t_f	–	–	–	50	ns
LOAD rise, fall time	t_r (L) t_f (L)	–	–	–	1	μs
CP →ECLK time	t_{CE}	–	0	–	–	ns
ECLK →CP time	t_{EC}	–	150	–	–	ns

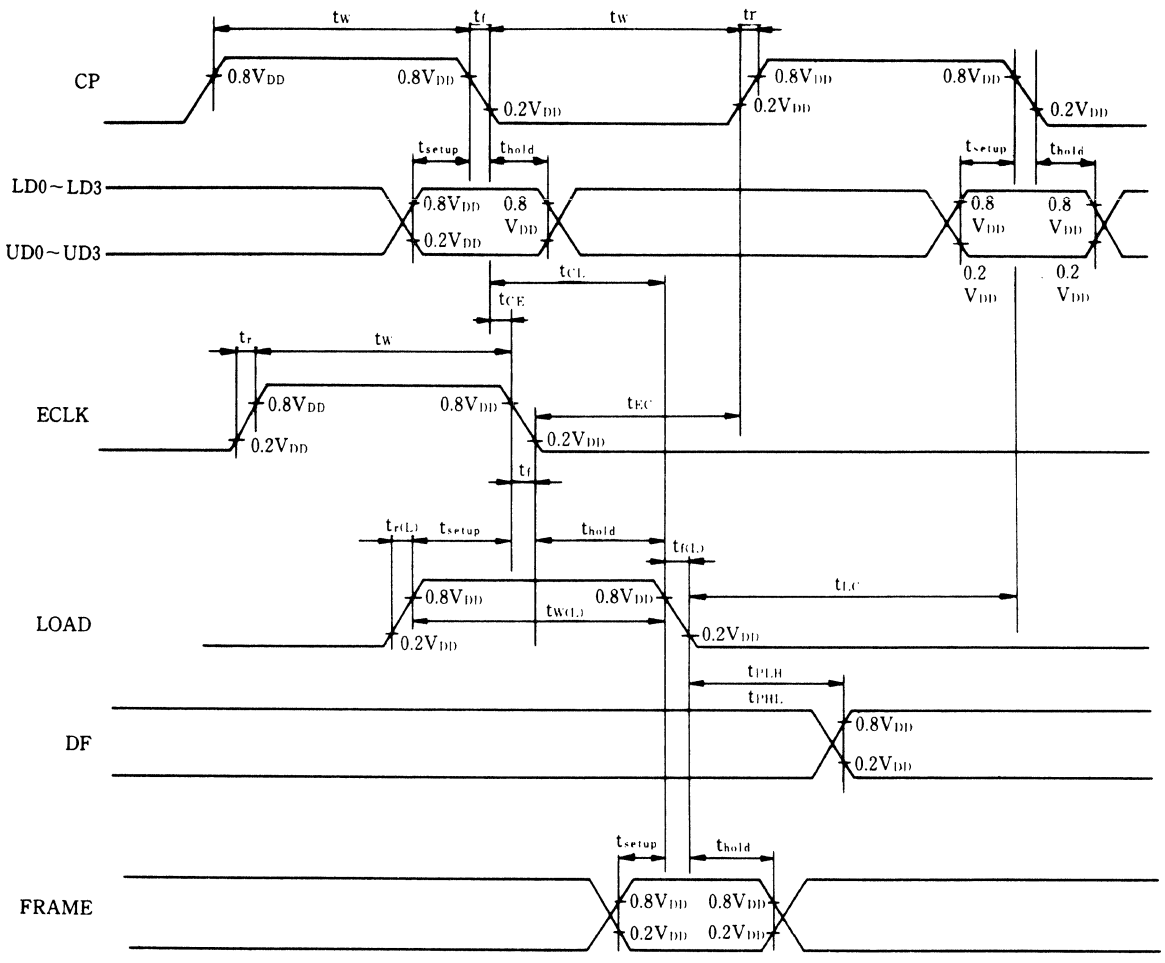


Fig. 6 Interface timing

LM250X

FEATURES

640(W) dots x 200(H) dots graphic and alphanumeric display
Attachable controller: HD63645F

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 270W x 150H x 13.5T (max.) mm
Effective display area . . . . . 239.0W x 104.0H mm
Number of dots . . . . . 640W x 200H dots
Dot size . . . . . 0.32W x 0.46H mm
Dot pitch . . . . . 0.35W x 0.49H mm
Weight . . . . . 450 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	−0.3	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	−0.3	28.0 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD}+ 0.3 V
Operating temperature (Ta) (Note 2)	0 ~ +40°C	
Storage temperature (Tstg) (Note 3)	−20 ~ +60°C	

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V, V_{EE} = −21.5 V ±1 V
Input "high" voltage (V_{IH}) . . . . . 0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) . . . . . 0 ~ 0.3 x V_{DD} V
Power supply current for logic (I_{DD}) (Note 4) . . . 8 mA typ.
Power supply current for LCD drive (I_{EE})(Note 4) . 7 mA typ.
Frame frequency (f_{FLM}) . . . . . 65 Hz min.
70 Hz typ.
75 Hz max.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
1/200 Duty (Note 5)
Ta = 0°C . . . . . 23.0 V typ.
Ta = 25°C . . . . . 21.7 V typ.
Ta = 40°C . . . . . 20.8 V typ.

Notes 1. Applied to CL1, CL2, D0 ~ D3, FLM and M.
2. The color of the display may change into blue if operated at maximum temperature. It is recommended to use it between 0°C ~ 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. V_{DD} = +5V, $V_{DD} - V_0$ = 23V, D0 ~ D3 = 1010 . . . . . , f_{FLM} = 70 Hz
5. Viewing angle = 10°

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D3	H/L	Data
2	D2	H/L	Data
3	FLM	H	The FLM signal indicating the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H→L	Data latch
6	CL2	H→L	Data shift
7	D1	H/L	Data
8	D0	H/L	Data
9	V_{DD}	–	Power supply for logic circuit
10	V_{SS}	–	Ground
11	V_{EE}	–	Power supply for LC driving
12	V_0	–	Operating voltage for LC driving

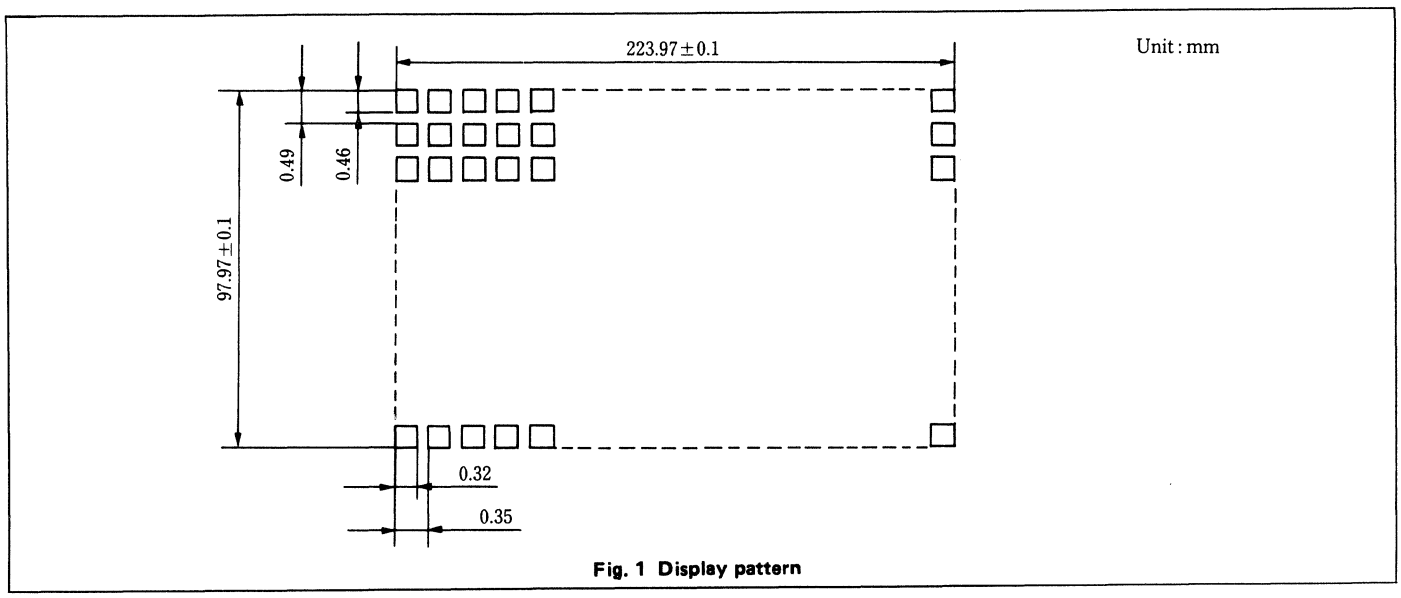


Fig. 1 Display pattern

Unit : mm

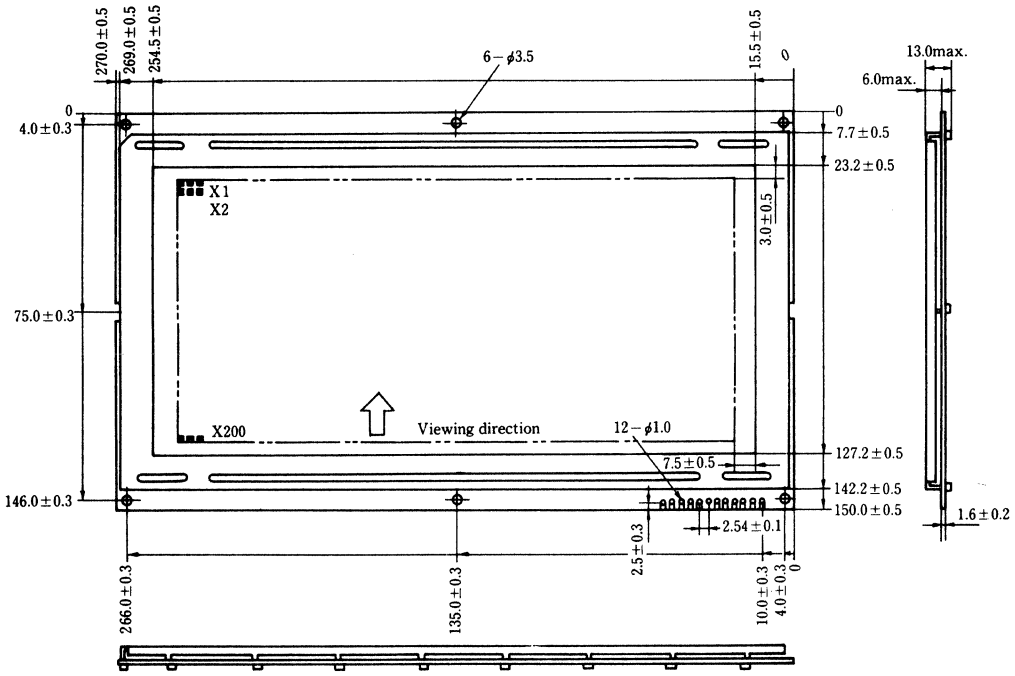


Fig. 2 External dimensions

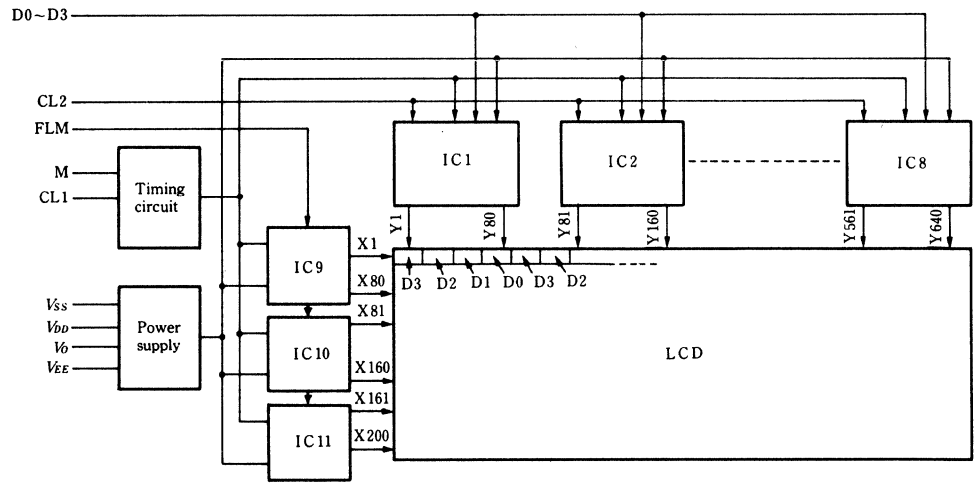
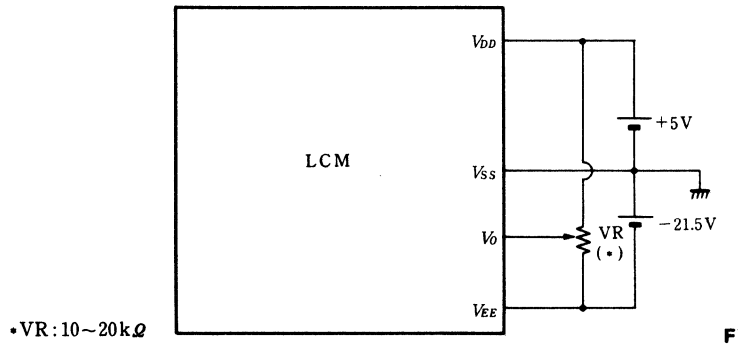


Fig. 3 Block diagram



•VR : 10~20kΩ

Fig. 4 Power supply

Observe the following sequencing when turning power supply on and off.

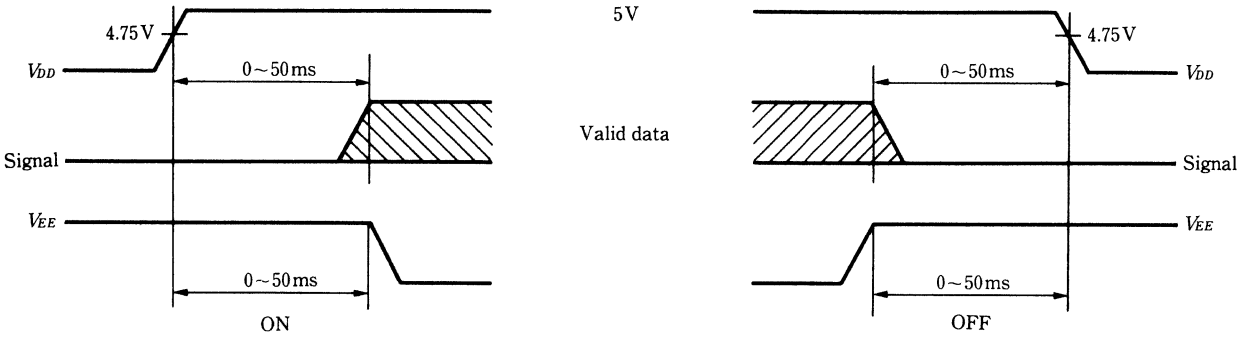


Fig. 5 Voltage sequencing

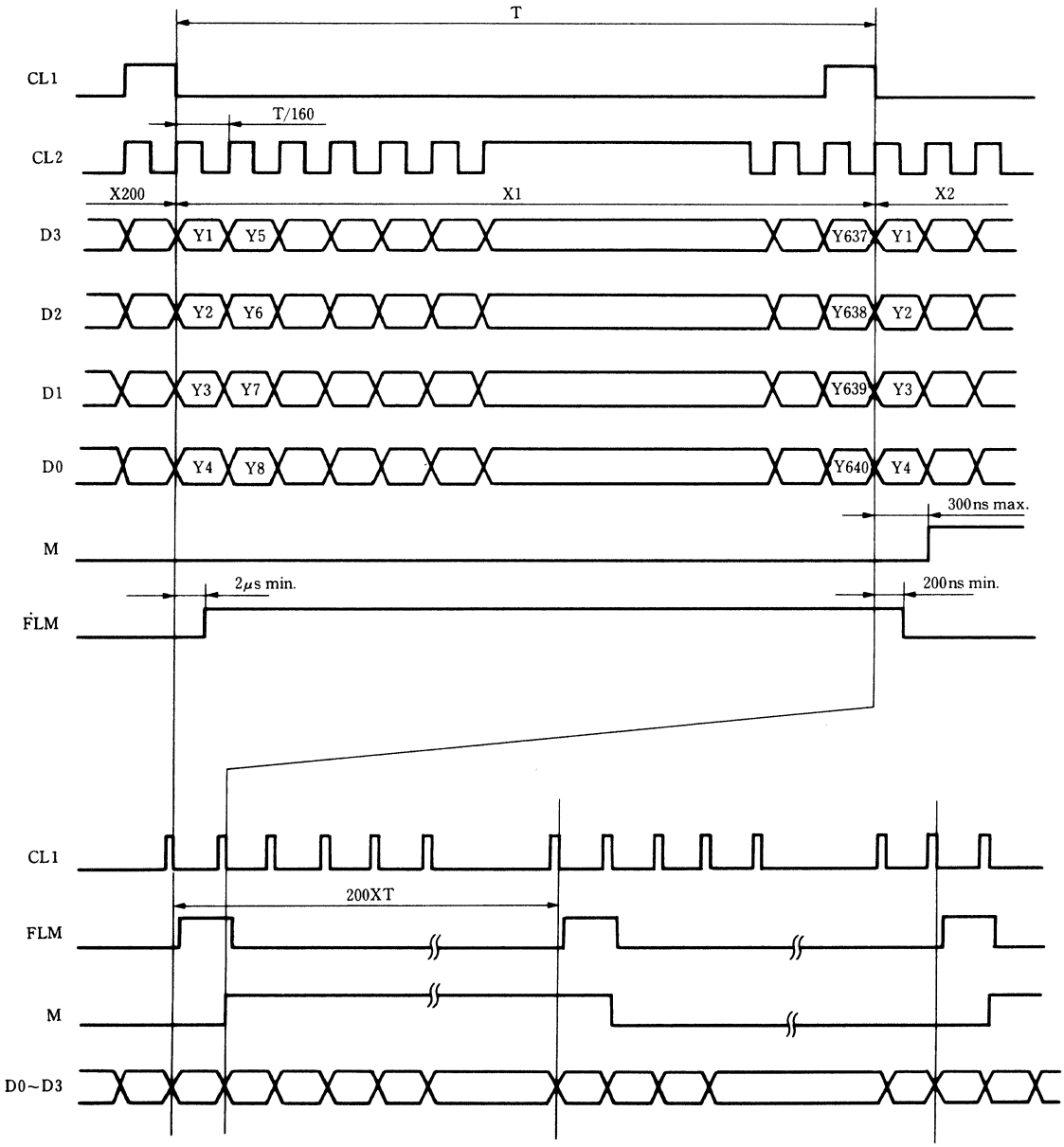


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	410	–	–	ns
CL2 pulse width	t_{CWH}	150	–	–	ns
CL2 pulse width	t_{CWL}	150	–	–	ns
CL1 set up time	t_{SCL1}	150	–	–	ns
CL1 hold time	t_{HCL1}	150	–	–	ns
Clock rise, fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	200	–	–	ns

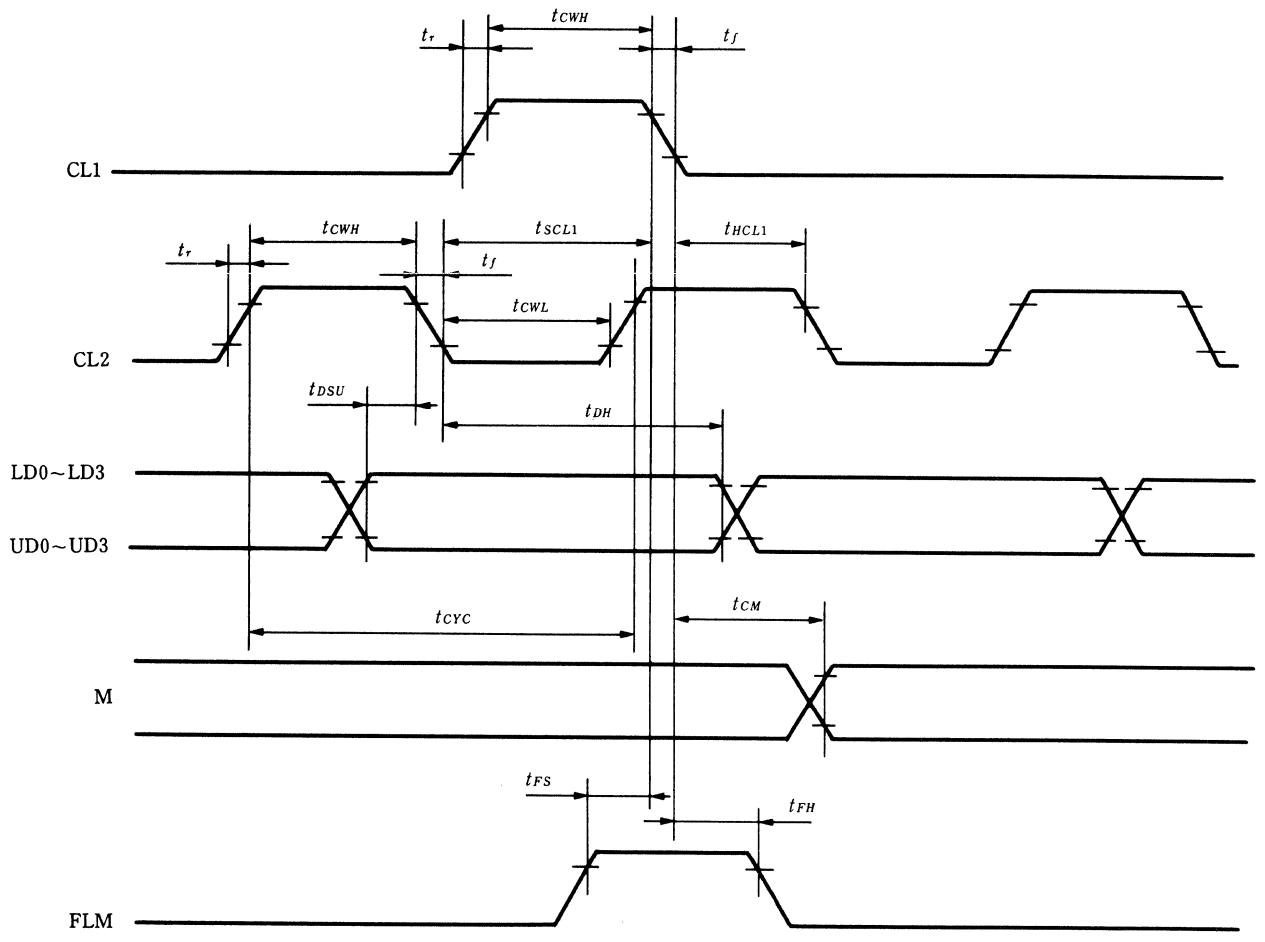


Fig. 7 Interface timing

LM585X

- 640 dot (W) x 200 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: MSM6255GSK or MSM6265GSK
- Color tone: LM585X . . . . . Yellowgreen

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 260W x 195H x 12.5T (max.) mm
Effective display area . . . . . 220W x 166H mm
Number of dots . . . . . 640W x 200H dot
Dot size . . . . . 0.29W x 0.74H mm
Dot pitch . . . . . 0.32W x 0.77H mm
Weight . . . . . about 540 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic (V_{DD})	0	6.5 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	0	22 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} + 0.3 V
Operating temperature (Ta) (Note 2)	0	40°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V,
$V_{DD} - V_{EE}$ = 19.5 V ±0.5 V

Input "high" voltage (V_{IH}) . . . . . 0.8 x V_{DD} V min.
Input "low" voltage (V_{IL}) . . . . . 0.2 x V_{DD} V max.
Power supply current (I_{DD}) (Note 4) . . . . . 5 mA typ.
(I_{EE}) (Note 4) . . . . . 4 mA typ.
Frame frequency (f_{FRAME}) . . . . . 70 Hz min.
75 Hz typ.
80 Hz max.
Input capacitance (C_{in}) (f_{CP} = 1 MHz) . . . . . 150 pF typ.

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$) (Note 5) Duty = 1/100

Ta = 0°C . . . . . 16.7 V typ.
Ta = 25°C . . . . . 15.8 V typ.
Ta = 40°C . . . . . 15.2 V typ.

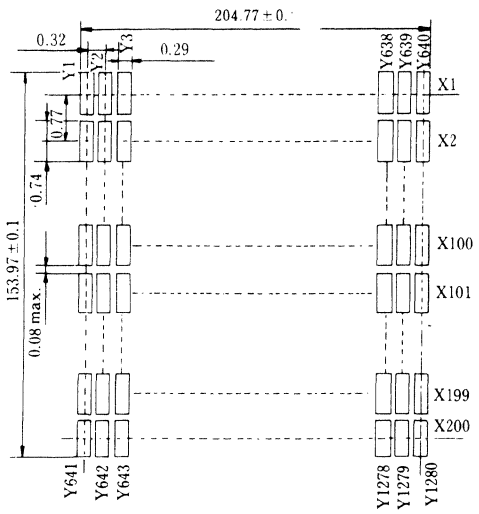
OPTICAL DATA . . . . . See page 15.

Notes 1. Applied to FRAME, LOAD, DF, ECLK, CP, UD0 ~ UD3, and LD0 ~ LD3.
2. When operated at maximum temperature, the display may change into blue color.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. When viewing angle is 25°.
5. In the case of V_{DD} = +5V, $V_{DD} - V_0$ = 15V, DF = 75 Hz, UD0 ~ UD3 = 0V and LD0 ~ LD3 = 0V.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1 ~ 4	UD0 ~ UD3	H/L	Data (upper half)
5	ECLK	H	Chip enable clock
6	FRAME	H	Frame frequency (Indicating the beginning of each display cycle)
7	DF	H/L	Control signal for AC driving
8	LOAD	H → L	Data latch
9	CP	H → L	Data shift
10 ~ 13	LD0 ~ LD3	H/L	Data (lower half)
14	V_{DD}	—	Power supply for logic circuit
15	V_{SS}	—	Ground
16	V_{EE}	—	Power supply for LC driving
17	V_0	—	Operating voltage for LC driving
18	NC	—	—

Unit: mm

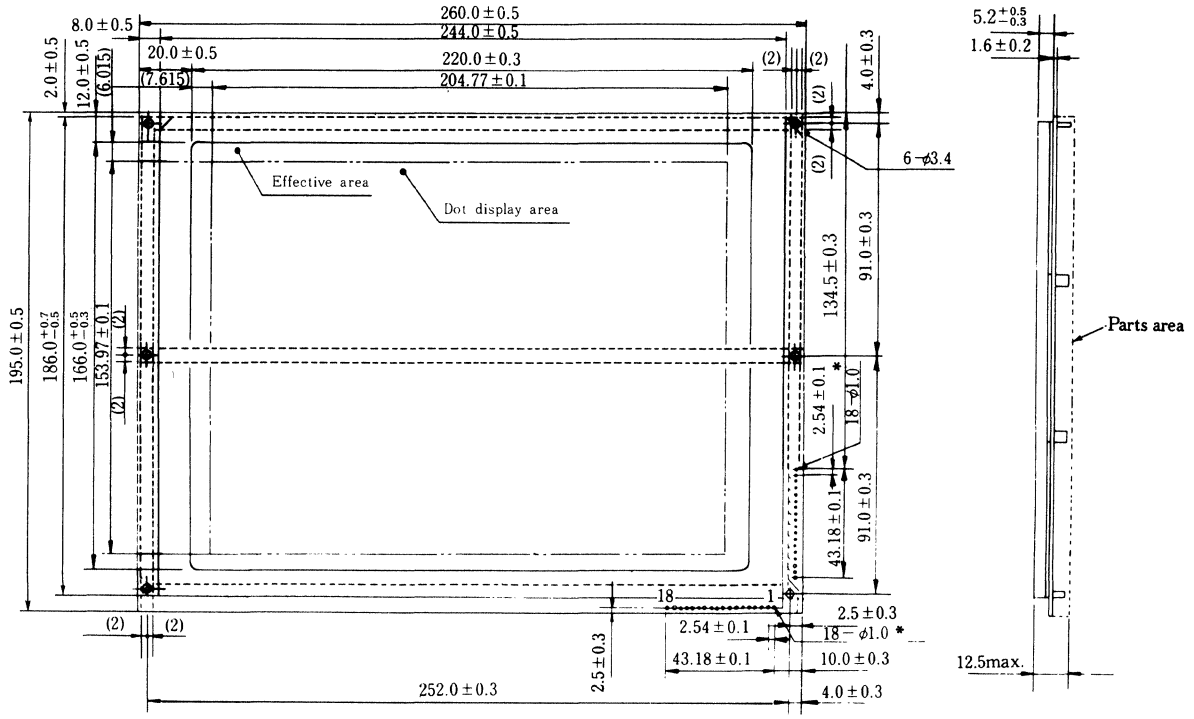


Note: Tolerance for dimensions not especially specified: ±0.1 mm

Fig. 1 Detail of dot pattern

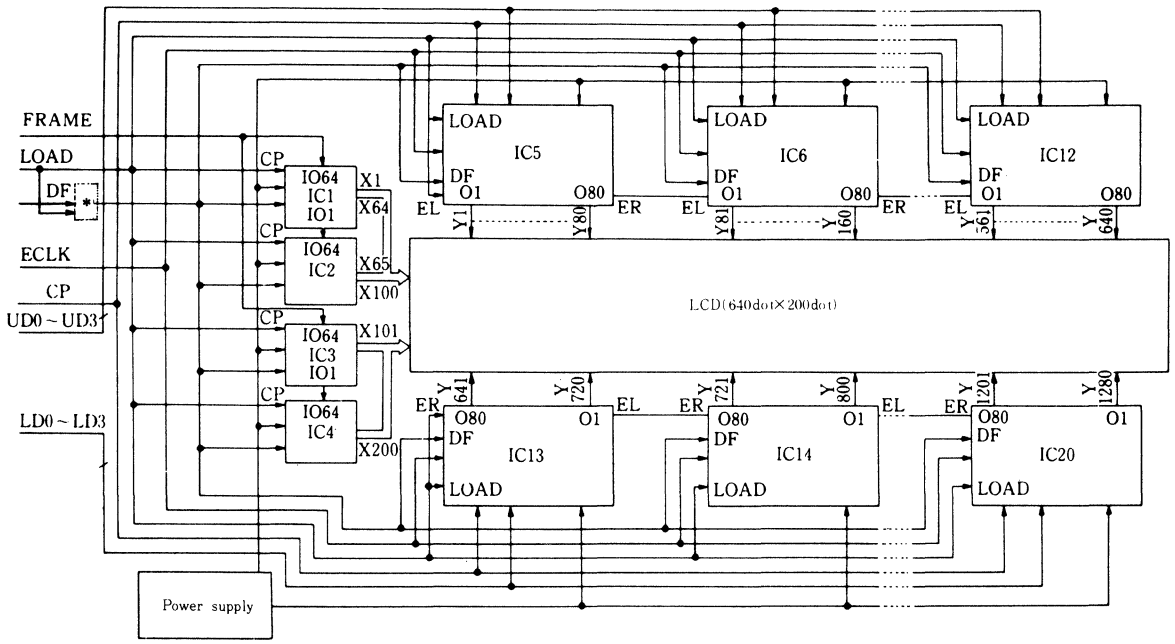
SECTION 4

Unit: mm



* Whichever can be used for interface.

Fig. 2 External dimension



* Interface timing circuit

Fig. 3 Block diagram

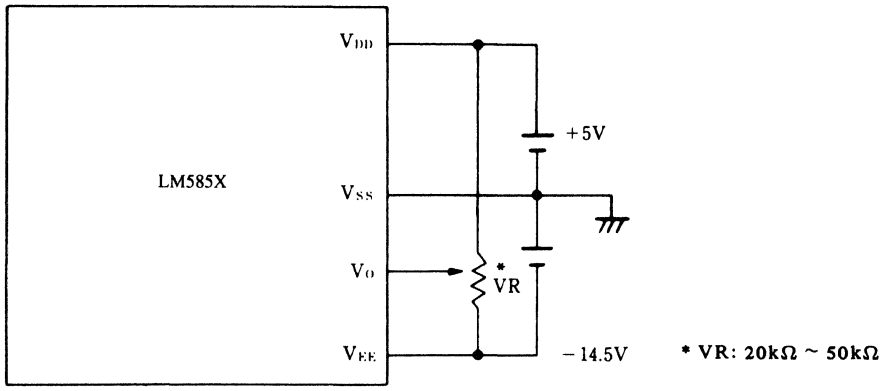
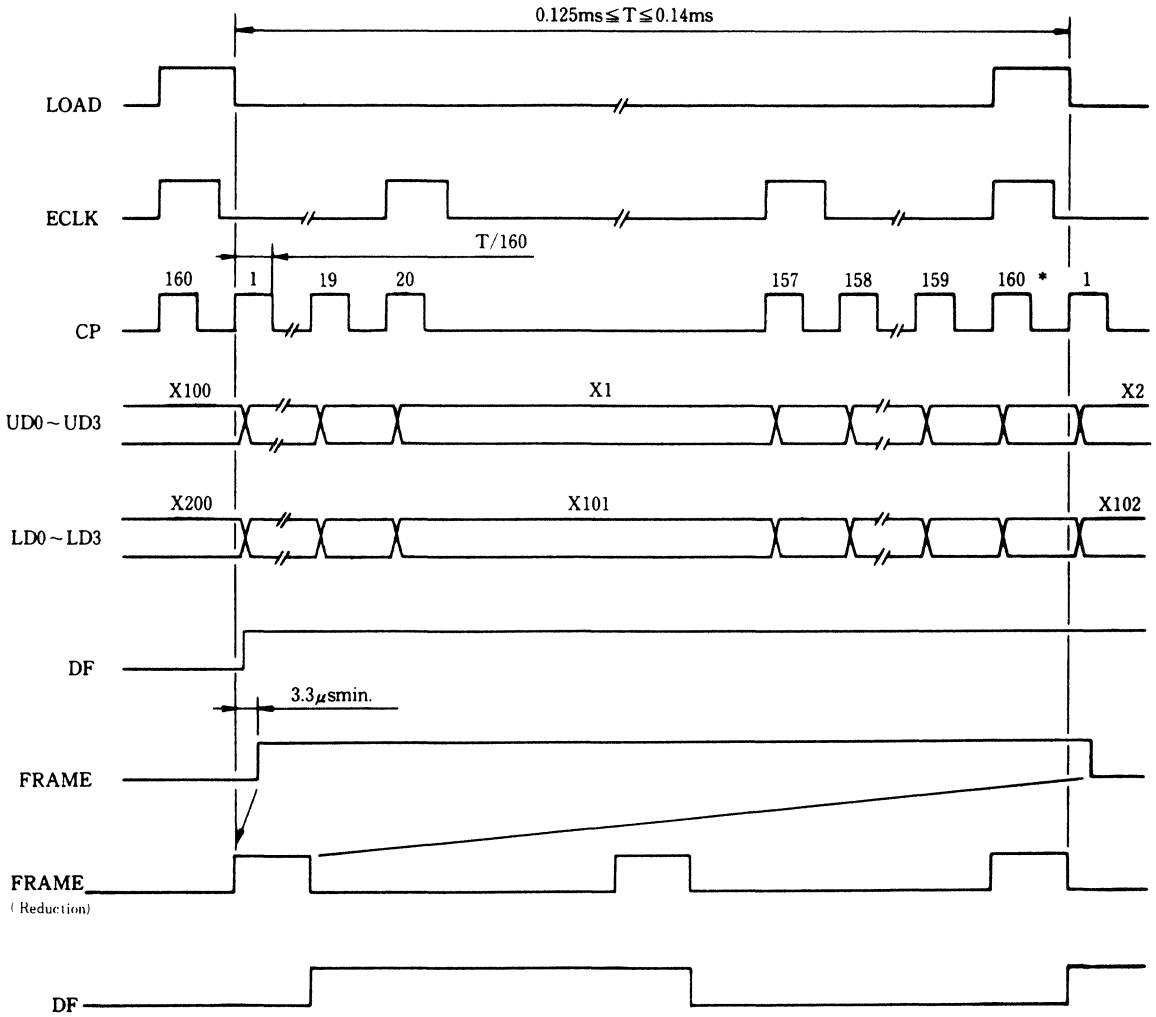


Fig. 4 Power supply



* There is CP pulse interrupting time of sixteen pulse between CP (160) and CP (1).

Fig. 5 Interface timing

TIMING CHARACTERISTICS

(V_{DD} = 5V ±10%, Ta = −20 ~ +85° C, CL = 15 μF)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" delay time	t_{PLH} t_{PHL}	–	–	–	200	ns
Frequency of maximum clock	f_{CP}	DUTY = 50%	–	–	1.41	MHz
CP ECLK pulse width	t_W	–	125	–	–	ns
LOAD pulse width	t_W (L)	–	125	–	–	ns
Set up time	t_{setup}	–	100	–	–	ns
CP → LOAD time	t_{CL}	–	250	–	–	ns
LOAD → CP time	t_{LC}	–	0	–	–	ns
Hold time	t_{hold}	–	100	–	–	ns
Rise, Fall time	t_r t_f	–	–	–	50	ns
LOAD rise, fall time	t_r (L) t_f (L)	–	–	–	1	μs
CP → ECLK time	t_{CE}	–	0	–	–	ns
ECLK → CP time	t_{EC}	–	150	–	–	ns

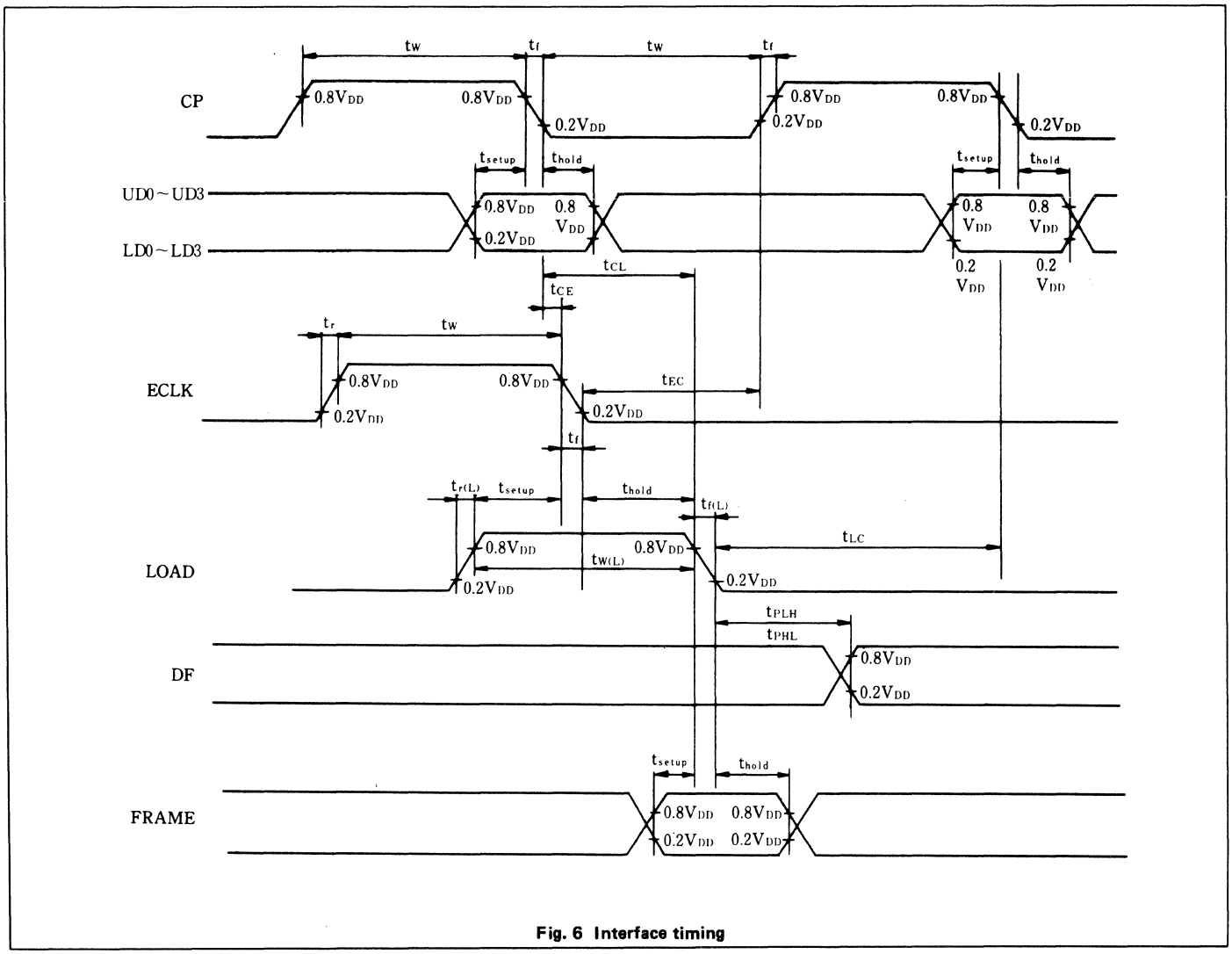


Fig. 6 Interface timing

LM246X

- 320 dot (W) x 256 dot (H) graphic and alpha-numeric display
- Attachable controller LSI: HD63645F

MECHANICAL DATA (Nominal dimensions)

Module size	168W x 150H x 13.5T (max.) mm
Effective display area	142W x 115H mm
Number of dots	320W x 256H dot
Dot size	0.38W x 0.38H mm
Dot pitch	0.43W x 0.43H mm
Weight	about 265 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	−0.3	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	−0.3	28.0 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD}+0.3V
Operating temperature (Ta) (Note 2)	0	40°C
Storage temperature (Tstg) (Note 3)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0V ±0.25V,
V_{EE} = −20V ±0.75V

Input "high" voltage (V_{IH})	0.7 x V_{DD}V min.
Input "low" voltage (V_{IL})	0.3 x V_{DD}V max.
Power supply current (I_{DD}) (Note 4)	5.0 mA typ.
(I_{EE}) (Note 4)	4.0 mA typ.
Frame frequency (f_{FLM})	65 Hz min.
	70 Hz typ.
	75 Hz max.

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/128 (Note 5)

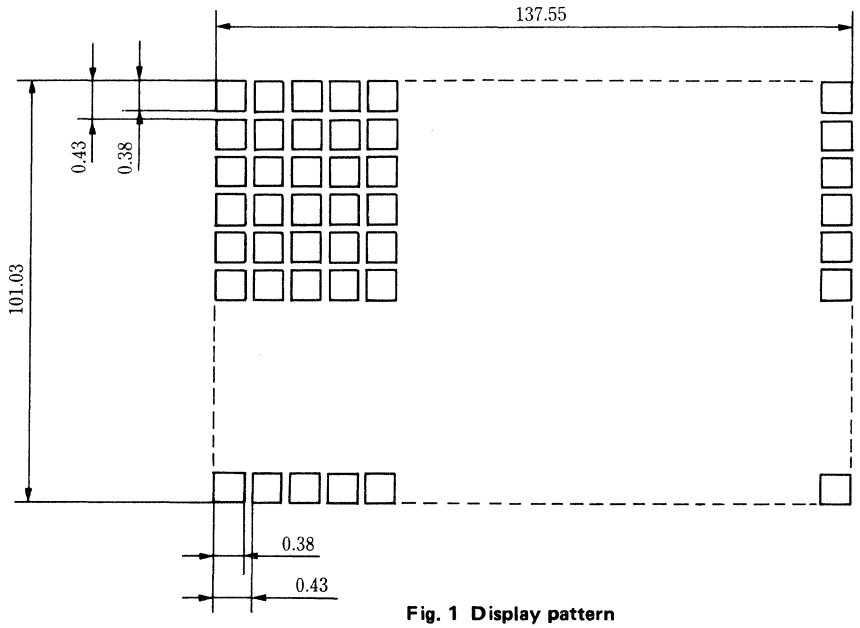
Ta = 0°C	22.5 V typ.
Ta = 25°C	21.5 V typ.
Ta = 40°C	20.2 V typ.

OPTICAL DATA . . . . . See page 15.

Notes
1. Applied to CL1, CL2, D0 ~ D3, FLM.
2. When operated at maximum temperature, the display may be changed into blue color. It is recommended to use it between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. In case of V_{DD} = +5V, $V_{DD} - V_O$ = 22.5V, D0 ~ D3 = 1010, f_{FLM} = 75 Hz.
5. When viewing angle is 25°.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1 ~ 4	UD0 ~ UD3	H/L	Data (upper half)
5	NC	–	
6	FLM	H	The FLM signal indicating the beginning of each display cycle
7	NC	–	
8	CL_1	H → L	Data latch
9	CL_2	H → L	Data shift
10 ~ 13	LD0 ~ LD3	H/L	Data (lower half)
14	V_{DD}	–	Power supply for logic circuit
15	V_{SS}	–	GND
16	V_{EE}	–	Power supply for LC driving
17	V_0	–	Operating voltage for LC driving
18, 19	NC	–	
20	MFG (V_{SS})	–	Connected to metal frame (GND)



Unit : mm

Fig. 1 Display pattern

Measurement tolerance ±0.06

Unit: mm

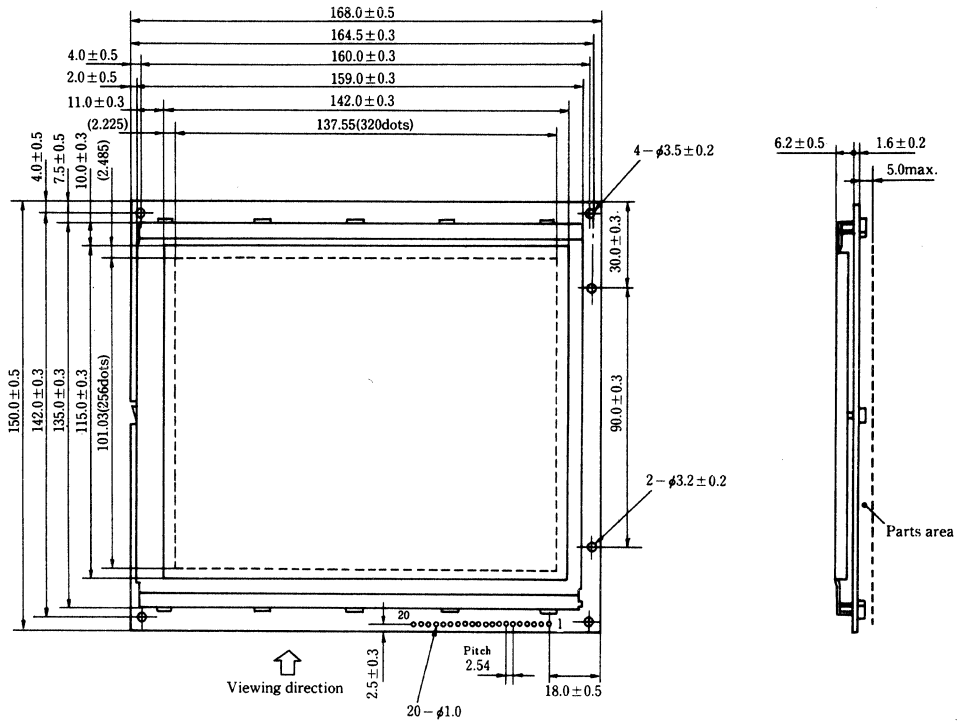
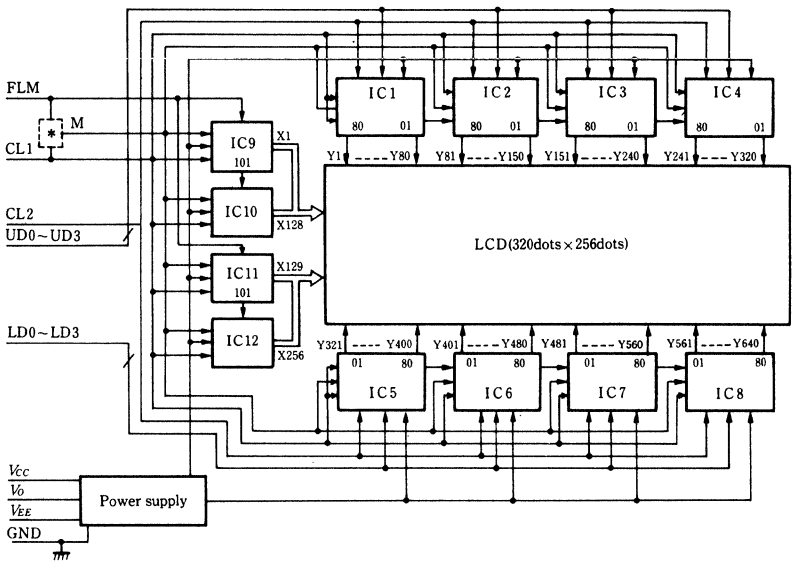
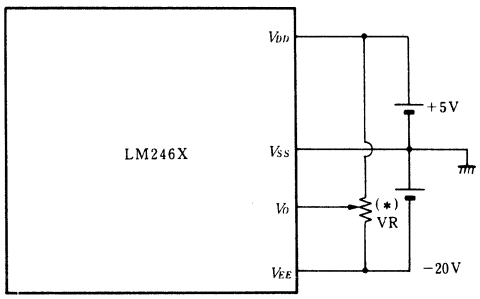


Fig. 2 External dimensions



* Interface timing circuit

Fig. 3 Block diagram



*VR = 10kΩ ~ 20kΩ.

Fig. 4 Power supply

Observe the following sequencing when turning power supply on and off.

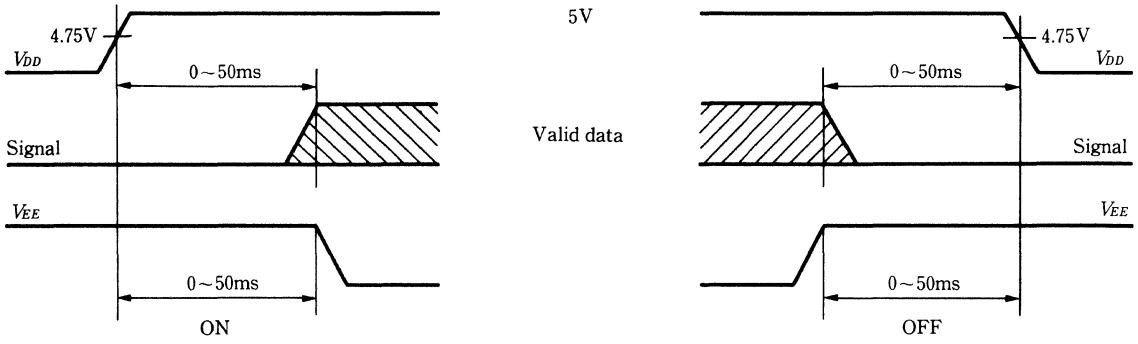


Fig. 5 Voltage sequencing

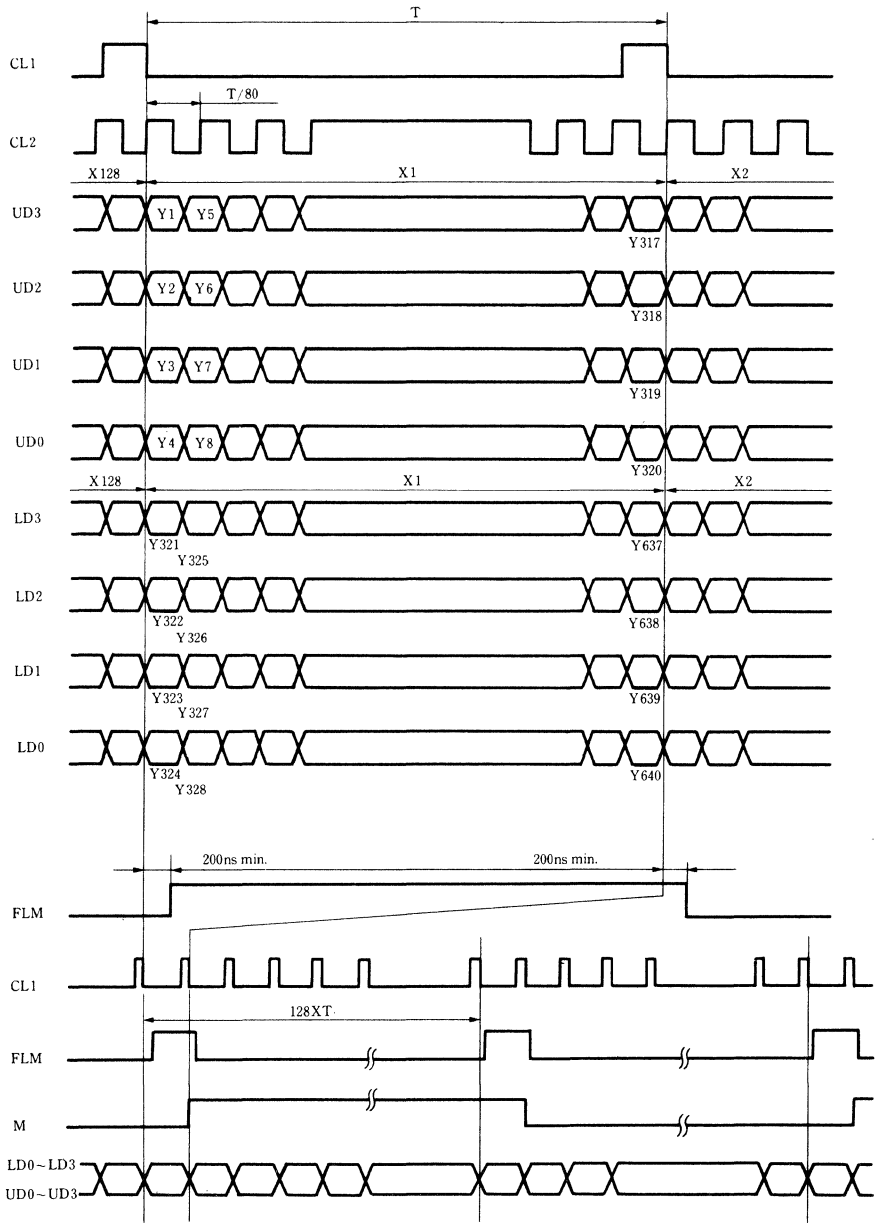


Fig. 6 Interface timing

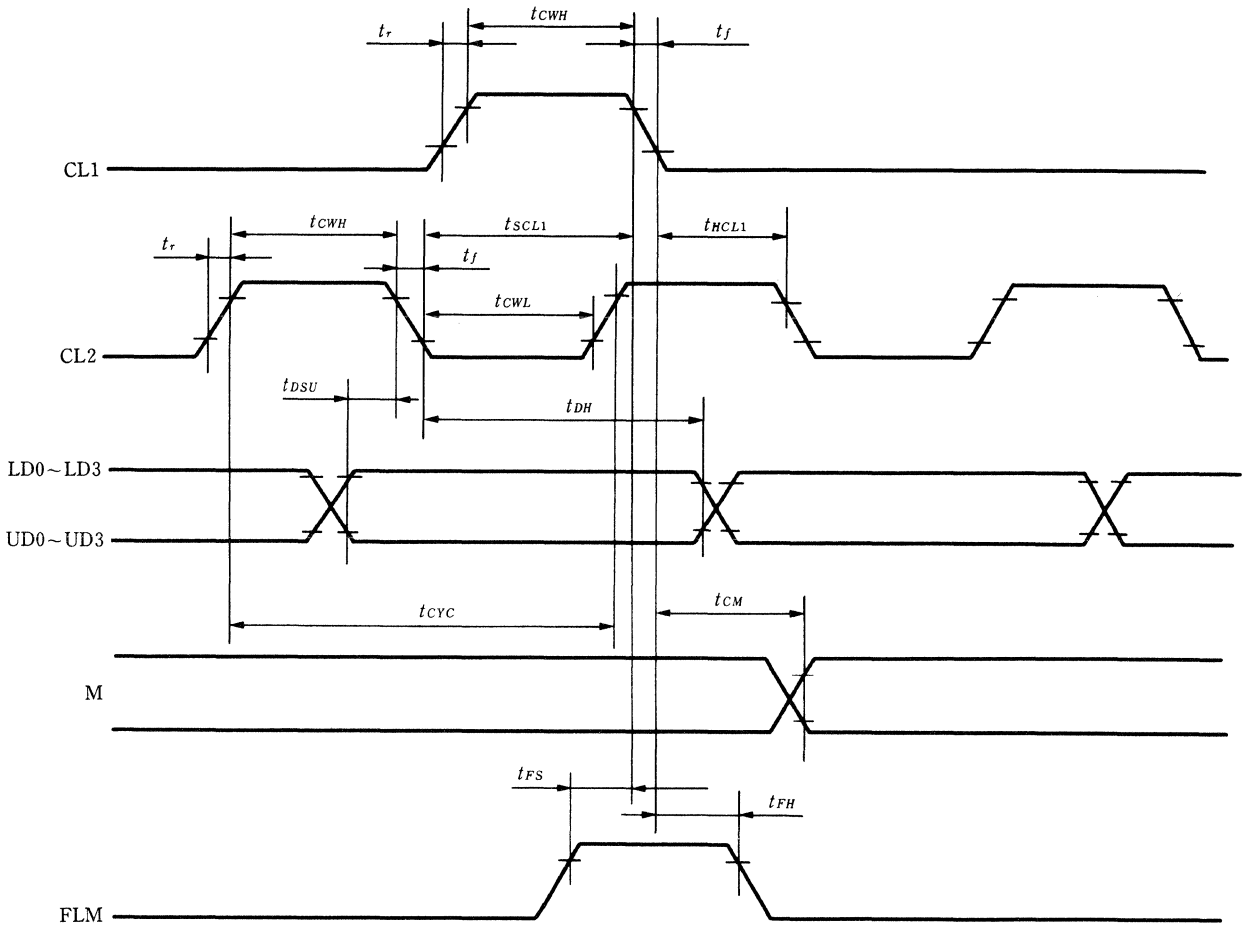


Fig. 7 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	330	–	–	ns
CL2 pulse width	t_{CWH}	125	–	–	ns
CL2 pulse width	t_{CWL}	125	–	–	ns
CL1 set up time	t_{SCL1}	80	–	–	ns
CL1 hold time	t_{HCL1}	80	–	–	ns
Clock rise, fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	200	–	–	ns

LM252X

FEATURES

- 640(W) dot x 400(H) dot graphic and alphanumeric display
- Attachable controller LSI: HD63645F

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 270W x 198H x 13.5T (max.) mm
Effective display area . . . . . 236.0W x 153.6H mm
Number of dots . . . . . 640W x 400H dots
Dot size . . . . . 0.33W x 0.33H mm
Dot pitch . . . . . 0.36W x 0.36H mm
Weight . . . . . 540 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	−0.3	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$) .	−0.3	28.0 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} +0.3V
Operating temperature (Ta) (Note 2)	0	~ +40°C
Storage temperature (Tstg) (Note 3)	−20	~ +60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25V, V_{EE} = −21.5 V ±1V
Input "high" voltage (V_{iH}) (Note 1) . . . . . 0.7 V_{DD} V min.
Input "Low" voltage (V_{iL}) . . . . . 0.3 V_{DD} V max.
Power supply current for logic (I_{DD}) (Note 4) . . . 8 mA typ.
Power supply current for LCD drive (I_{EE}) (Note 4). 7 mA typ.
Frame frequency (f_{FLM}) . . . . . 65 Hz min.
70 Hz typ.
75 Hz max.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
1/200 Duty (Note 5)
Ta = 0°C . . . . . 23.0 V typ.
Ta = 25°C . . . . . 21.7 V typ.
Ta = 40°C . . . . . 20.8 V typ.

Notes 1. Applied to CL1, CL2, UD0 ~ UD3, LD0 ~ LD3, M and FLM.
2. The color of the display may change into blue if operated at maximum temperature. It is recommended to use between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. V_{DD} = +5V, $V_{DD} - V_0$ = 23.0V, UD0 ~ UD3, LD0 ~ LD3 = 1010 . . . . . , f_{FLM} = 70 Hz.
5. Viewing angle = 10°

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1 ~ 4	UD0 ~ UD3 (1) (4)	H/L	Data (Upper half)
5	NC	–	–
6	FLM	H	The FLM signal indicating the beginning of each display cycle
7	M	H/L	Control signal for AC driving
8	CL1	H→L	Data latch
9	CL2	H→L	Data shift
10 ~ 13	LD0 ~ LD3 (10) (13)	H/L	Data (Lower half)
14	V_{DD}	–	Power supply for logic circuit
15	V_{SS}	–	Ground
16	V_{EE}	–	Power supply for LC driving
17	V_0	–	Operating voltage for LC driving
18 ~ 20	NC	–	–

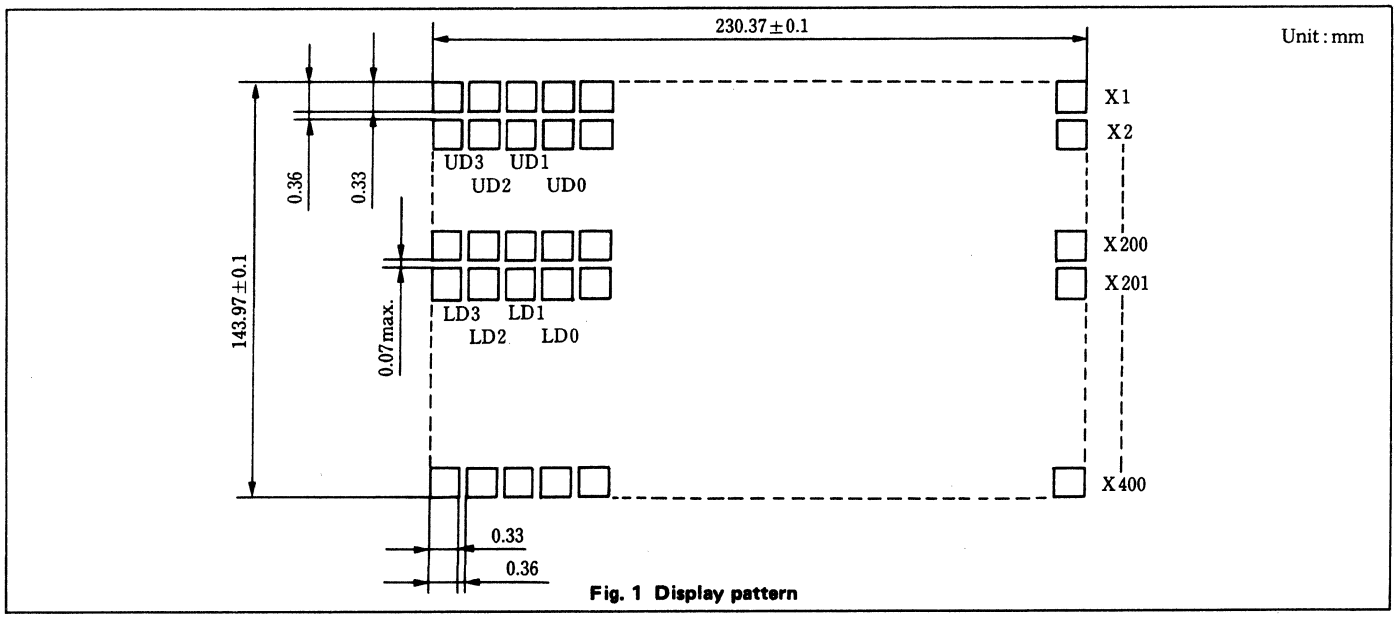


Fig. 1 Display pattern

Unit : mm

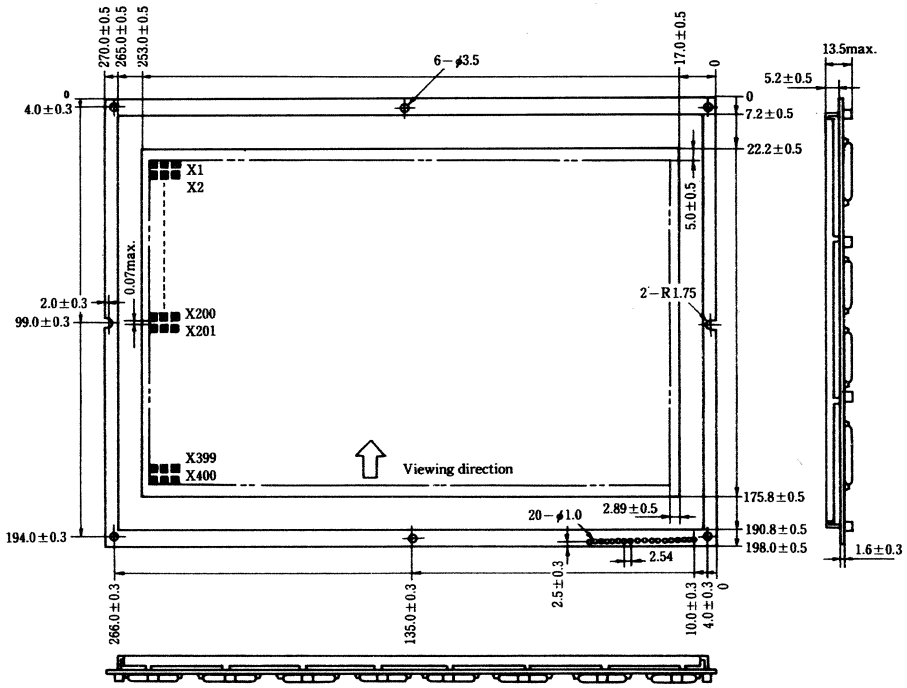
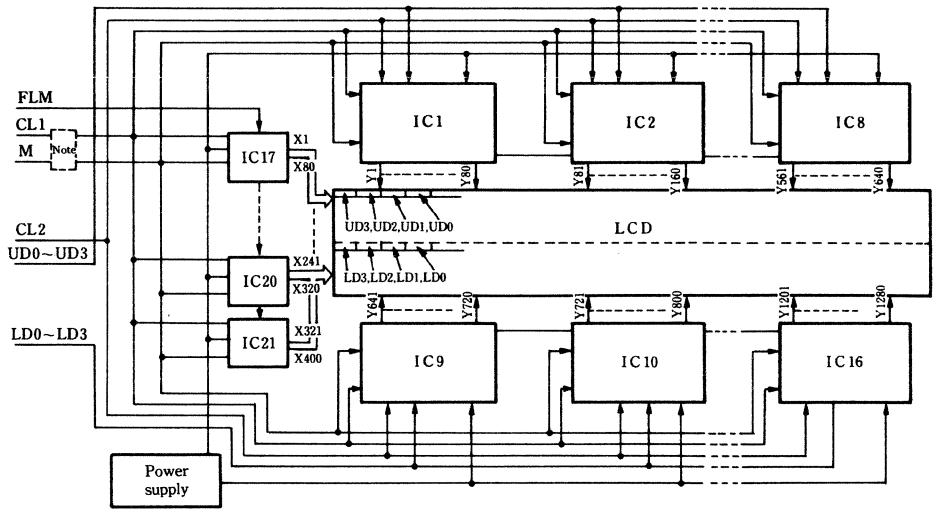
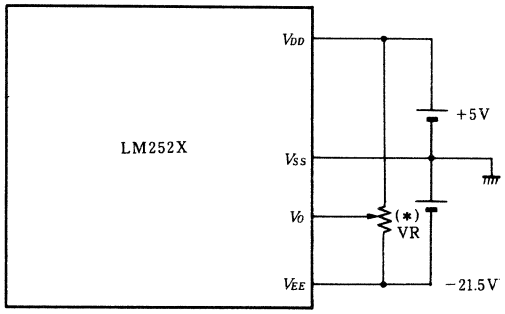


Fig. 2 External dimensions



Note : Interface timing circuit

Fig. 3 Block diagram



*VR : 10~20kΩ

Fig. 4 Power supply

Observe the following sequencing when turning power supply on and off.

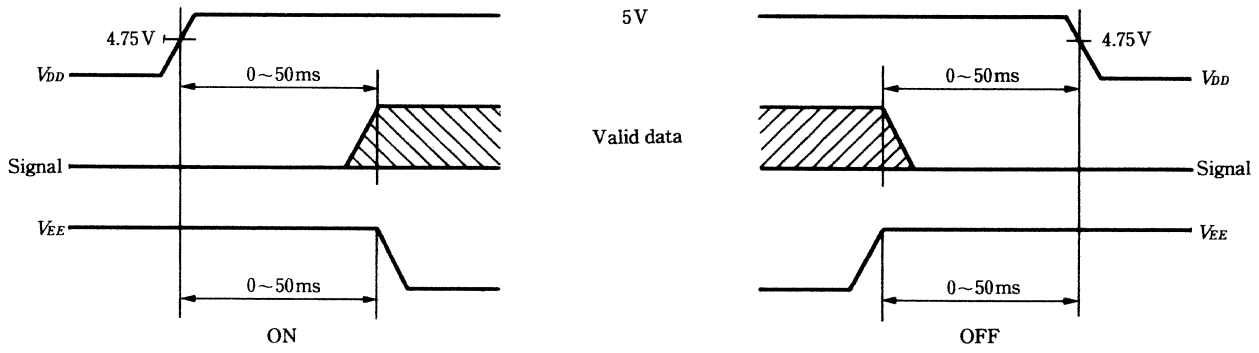


Fig. 5 Voltage sequencing

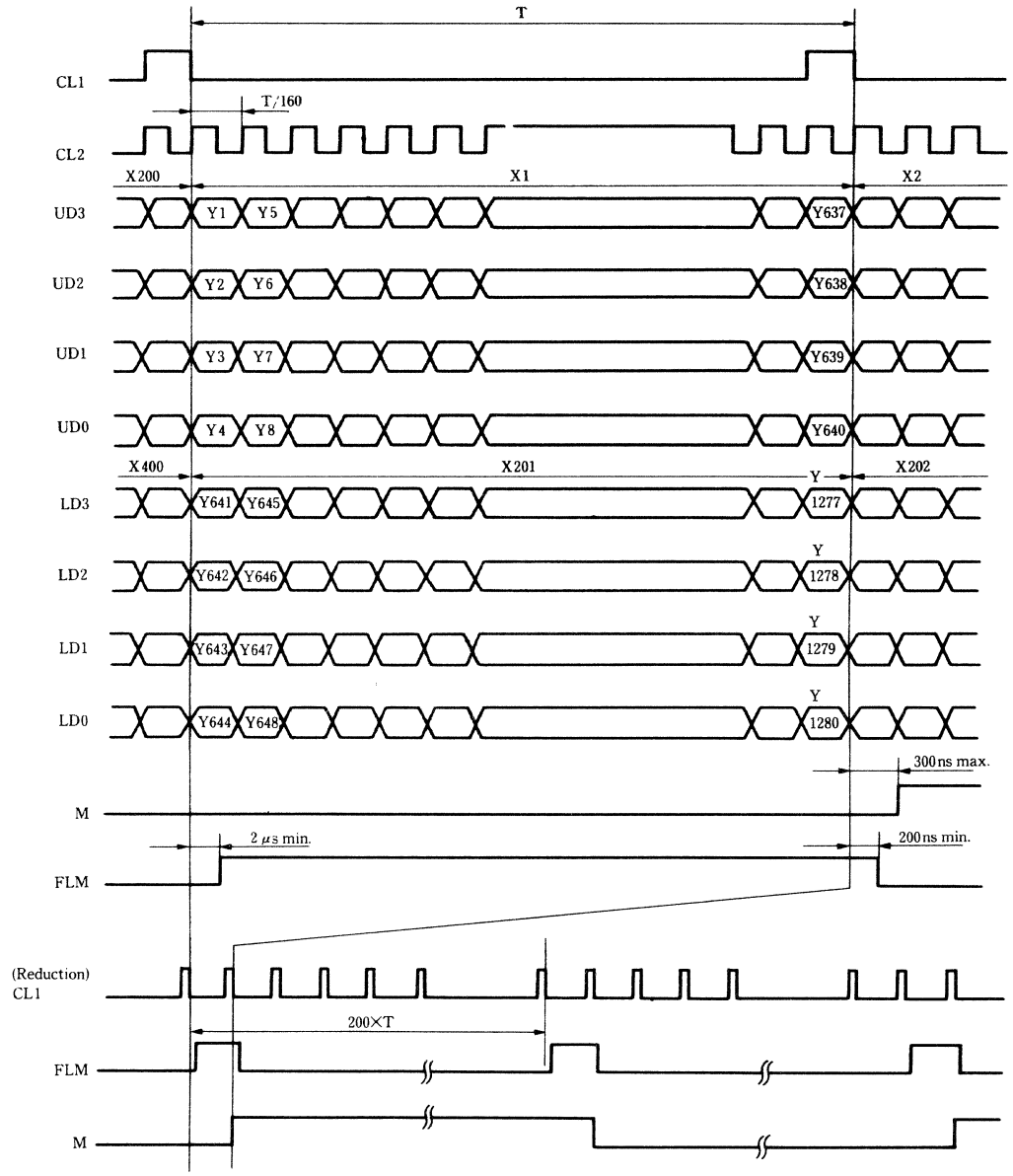


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	410	–	–	ns
CL2 pulse width	t_{CWH}	150	–	–	ns
CL2 pulse width	t_{CWL}	150	–	–	ns
CL1 set up time	t_{SCL1}	150	–	–	ns
CL1 hold time	t_{HCL1}	150	–	–	ns
Clock rise, fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	200	–	–	ns

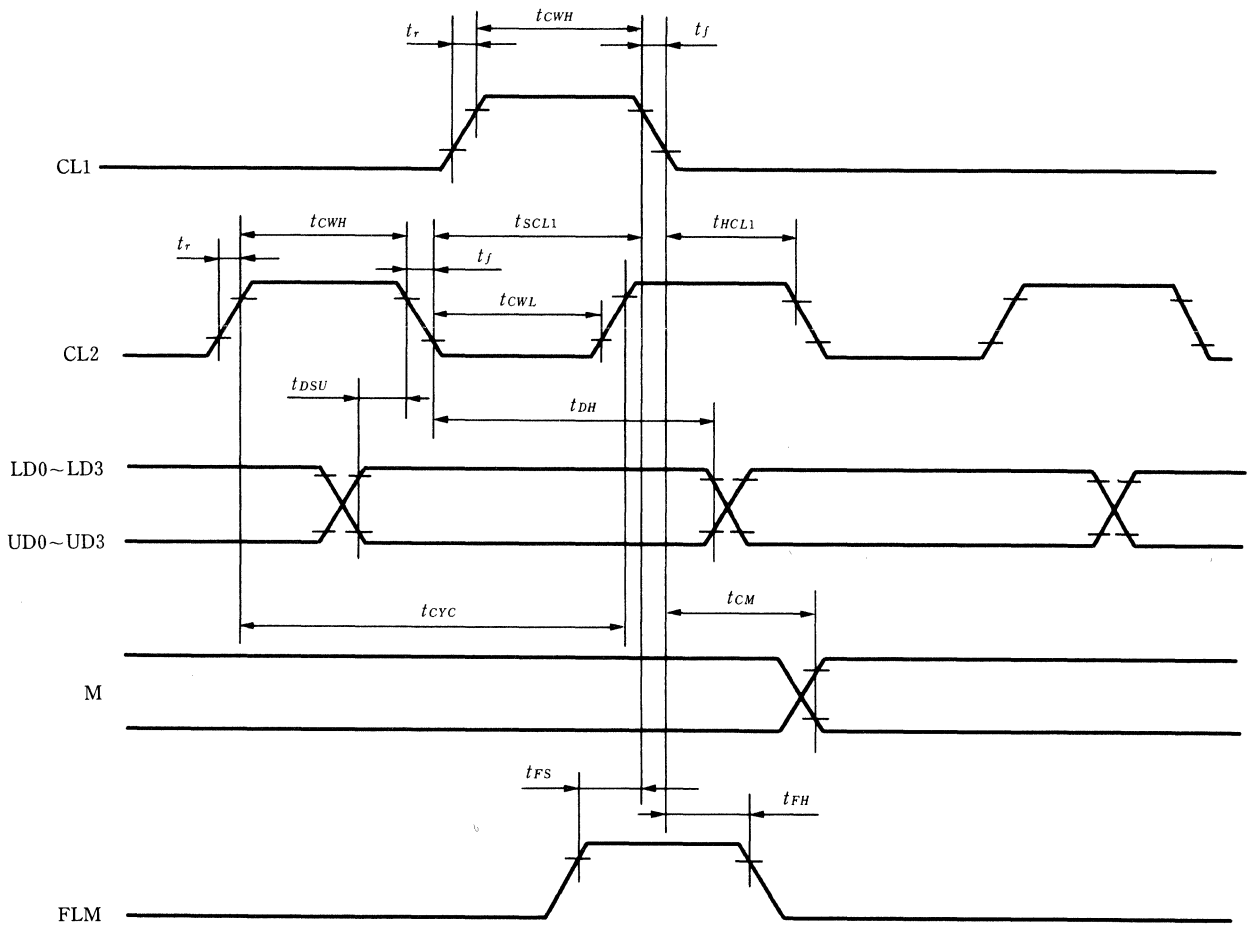


Fig. 7 Interface timing

COMPACT VERSION GRAPHICS LCD MODULES

LM258X

- 240 dot (W) × 64 dot (H) graphic and alphanumeric display
- Attachable controller: HD61830 (see section 6).

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 149W × 57H × 13T (max.) mm
Effective display area . . . . . 117W × 41H mm
Number of dots . . . . . 240W × 64H dot
Dot size . . . . . 0.44W × 0.44H mm
Dot pitch . . . . . 0.47W × 0.47H mm
Weight 110g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	− 0	19.0V
Input voltage (Vi)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	40°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0V ±0.25V, V_{EE} = −5.0V ±0.25V
Input "high" voltage (V_{IH}) . . . . . 0.7 × V_{DD}V min.
Input "low" voltage (V_{IL}) . . . . . 0.3 × V_{DD}V max.
Clock frequency (f_{CL2}) . . . . . 1080 kHz min.
1150 kHz type.
1200 kHz max.
Power supply current (I_{DD}) . . . . . 6 mA typ.
(D2 = GND, f_{CL2} = 1150 kHz, $V_{DD} - V_0$ = 14.8V)
Power supply for LCD drive (Recommended) ($V_O - V_{EE}$)
Duty = 1/64
Ta = 0°C . . . . . 15.5 V typ.
Ta = 25°C . . . . . 14.8 V typ.
Ta = 40°C . . . . . 14.1 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D	H/L	Serial row data
2	FLM	H	The FLM signal indicates the beginning of each display cycle.
3	M	H/L	Control signal for AC driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers.
5	CL2	H→L	Clock signal for shifting the serial data
6	N.C.	—	—
7	V_{DD}(+5V)	—	Power supply for logic circuit
8	V_{SS}(GND)	—	Ground
9	V_{EE}(−12V)	—	Power supply for LC driving
10	VO	—	Operating voltage for LC driving

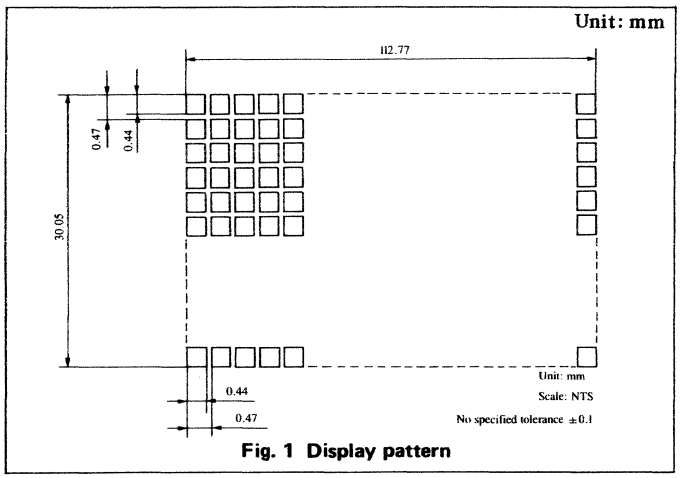


Fig. 1 Display pattern

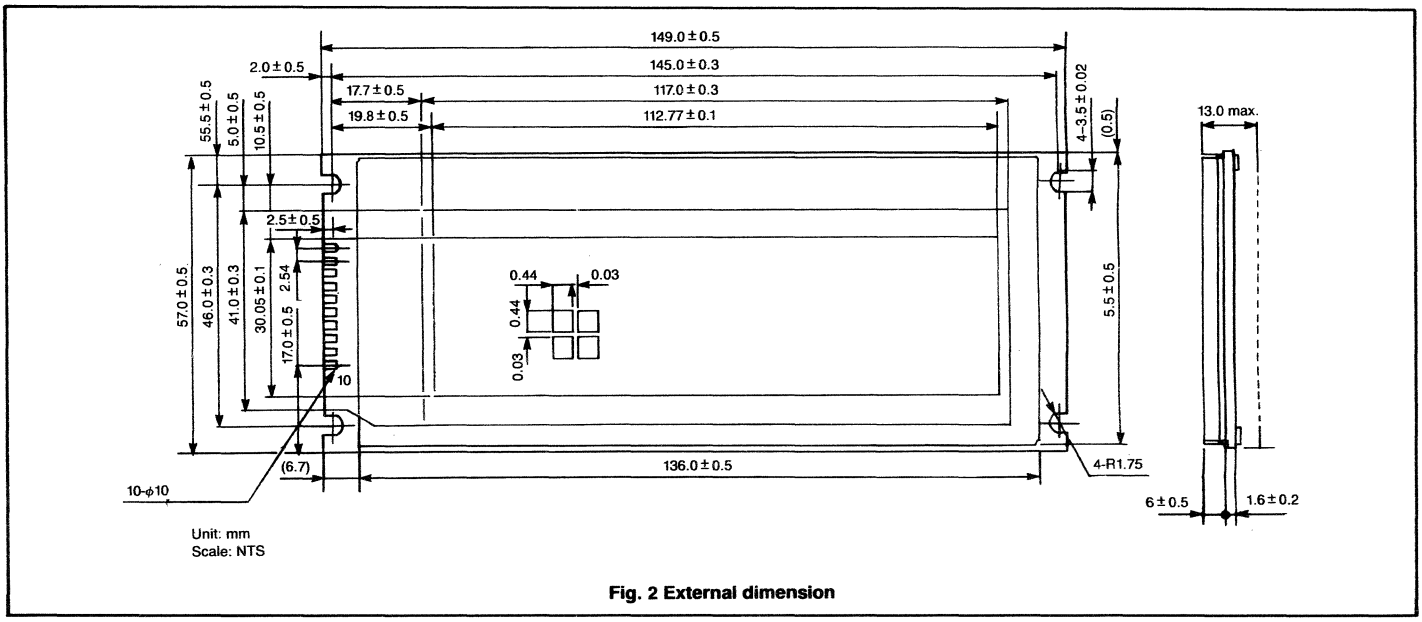


Fig. 2 External dimension

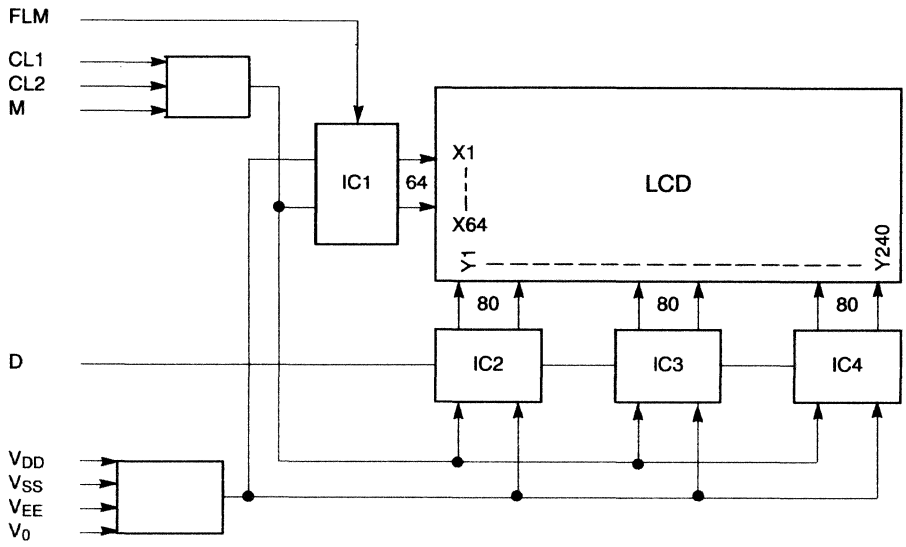


Fig. 3 Block diagram

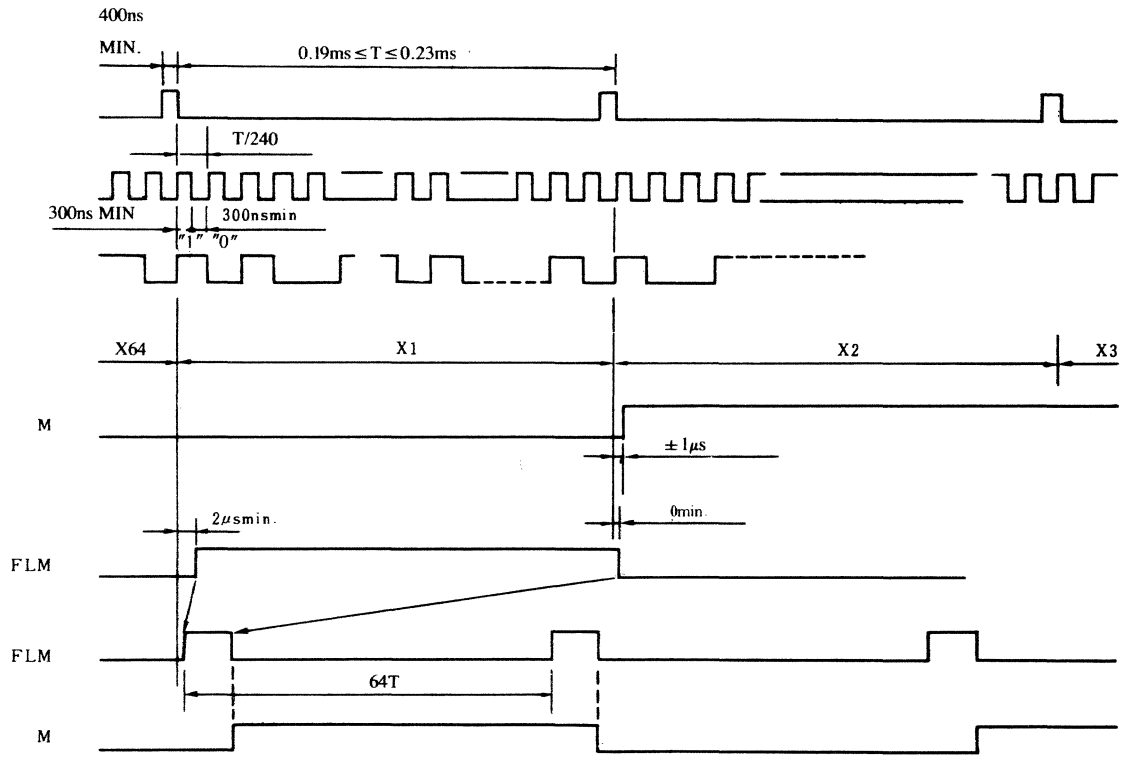


Fig. 4 Interface timing

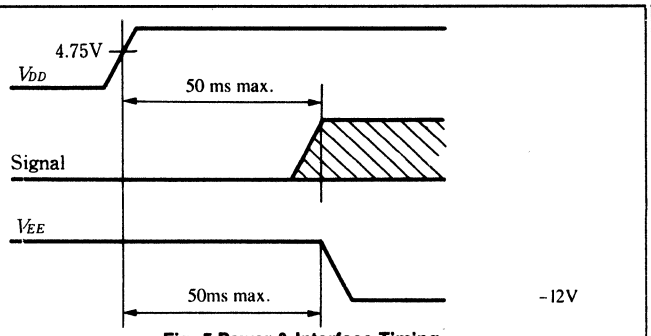


Fig. 5 Power & Interface Timing

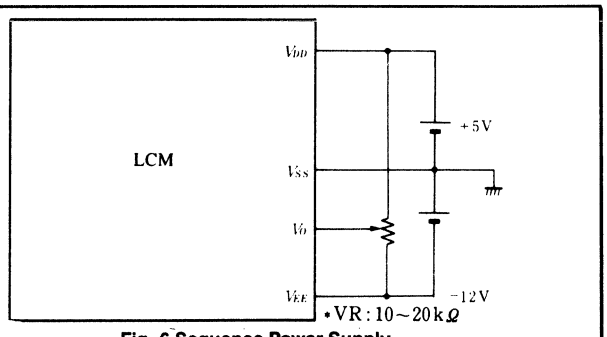


Fig. 6 Sequence Power Supply

TIMING CHARACTERISTICS

Item	Symbol	min.	typ.	max.	Unit
CL2 cycle time	t_{CYC}	810	–	–	ns
CL2 pulse width (H)	t_{CWH}	150	–	–	ns
CL2 pulse width (L)	t_{CWL}	150	–	–	ns
CL1 set up time (1)	t_{SCL1}	150	–	–	ns
CL1 set up time (2)	t_{HCL1}	150	–	–	ns
Clock rise/fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
CL1 delay time	t_{CL}	150	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	100	–	–	ns

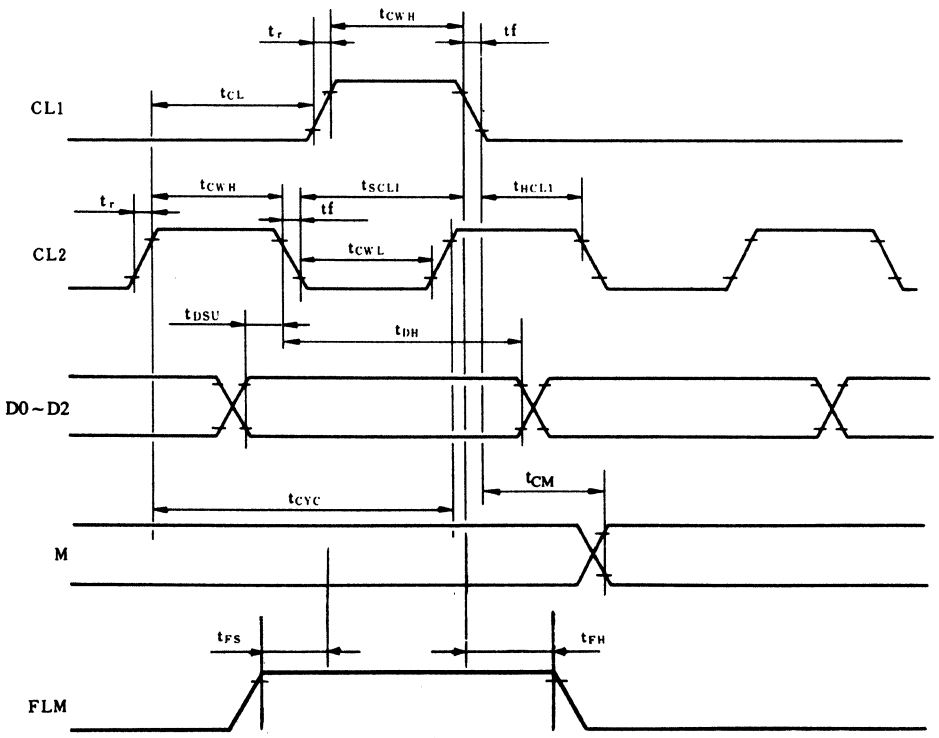


Fig. 7 Interface timing

LM254X

FEATURES

640(W) dots x 200(H) dots graphic and alphanumeric display
Attachable controller: HD63645F

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .270W × 150H × 13.0T (max.) mm
Effective display area . . . . . .224.0W × 98.0H mm
Number of dots . . . . . .640W x 200H dots
Dot size . . . . . 0.32W x 0.46H mm
Dot pitch . . . . . 0.35W x 0.49H mm
Weight . . . . . 450 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	−0.3	7.0 V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	−0.3	28.0 V
Input voltage (Vi) (Note 1)	−0.3	V_{DD}+ 0.3 V
Operating temperature (Ta) (Note 2)	0 ~ +40°C	
Storage temperature (Tstg) (Note 3)	−20 ~ +60°C	

ELECTRICAL CHARACTERISTICS

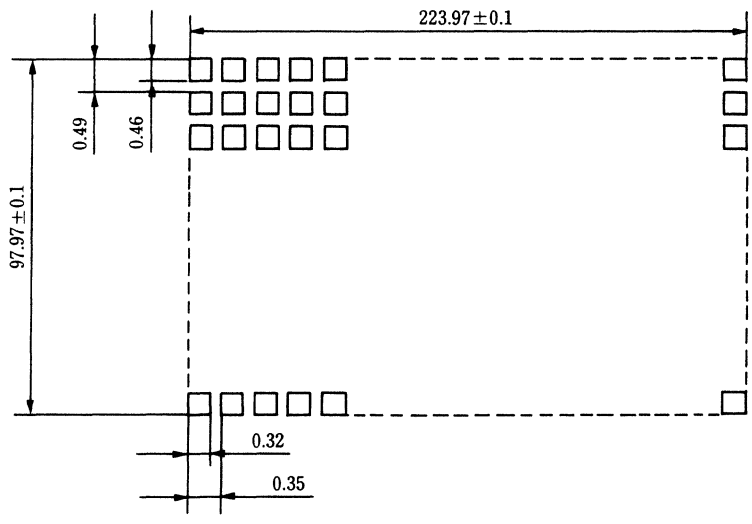
Ta = 25°C, V_{DD} = 5.0 V ±0.25 V, V_{EE} = −21.5 V ±1 V
Input "high" voltage (V_{IH}) . . . . . .0.7 x V_{DD} ~ V_{DD} V
Input "low" voltage (V_{IL}) . . . . . 0 ~ 0.3 x V_{DD} V
Power supply current for logic (I_{DD}) (Note 4) . . . 8 mA typ.
Power supply current for LCD drive (I_{EE})(Note 4) . 7 mA typ.
Frame frequency (f_{FLM}) . . . . . .65 Hz min.
70 Hz typ.
75 Hz max.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
1/200 Duty (Note 5)
Ta = 0°C . . . . . 23.0 V typ.
Ta = 25°C . . . . . 21.7 V typ.
Ta = 40°C . . . . . 20.8 V typ.

Notes 1. Applied to CL1, CL2, D0 ~ D3, FLM and M.
2. The color of the display may change into blue if operated at maximum temperature. It is recommended to use it between 0°C ~ 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. V_{DD} = +5V, $V_{DD} - V_L$ = 21.7V, D0 ~ D3 = 1010, f_{FLM} = 70 Hz.
5. Viewing angle = 10°.

OPTICAL DATA . . . . . See page 15.

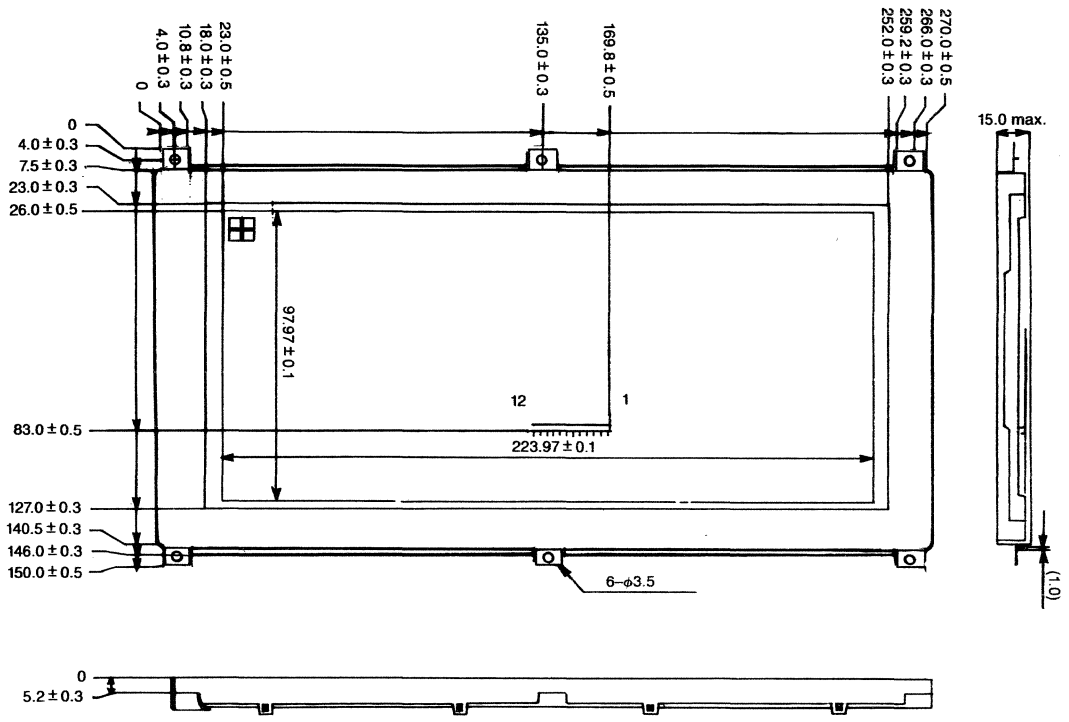
INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D3	H/L	Data
2	D2	H/L	Data
3	FLM	H	The FLM signal indicating the beginning of each display cycle
4	M	H/L	Control signal for AC driving
5	CL1	H→L	Data latch
6	CL2	H→L	Data shift
7	D1	H/L	Data
8	D0	H/L	Data
9	V_{DD}	–	Power supply for logic circuit
10	V_{SS}	–	Ground
11	V_{EE}	–	Power supply for LC driving
12	V_0	–	Operating voltage for LC driving



Unit : mm

Fig. 1 Display pattern



Note 1: Interface pin connection is located on the bottom side (LSI side).

Unit: mm
Scale: NTS

Fig. 2 External dimension

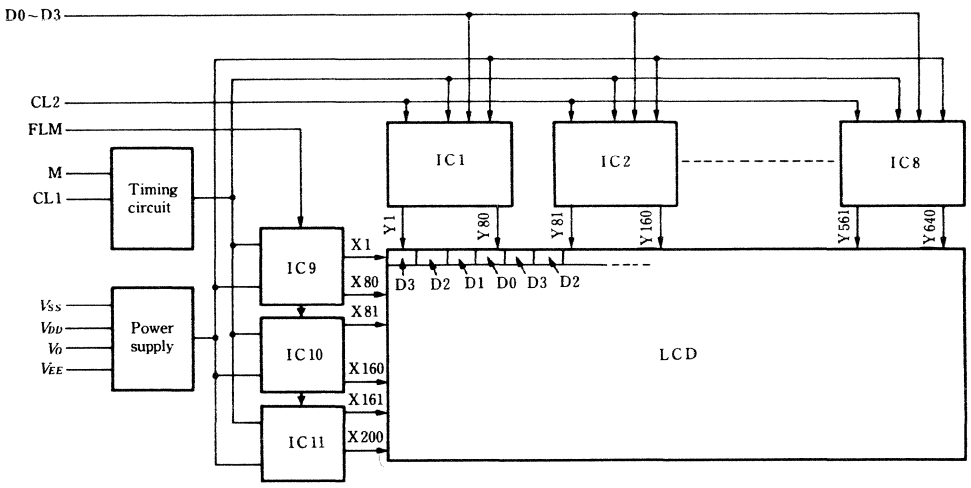
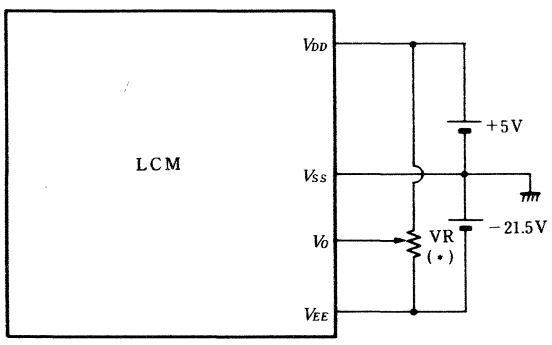


Fig. 3 Block diagram



•VR: 10~20kΩ

Fig. 4 Power supply

Observe the following sequencing when turning power supply on and off.

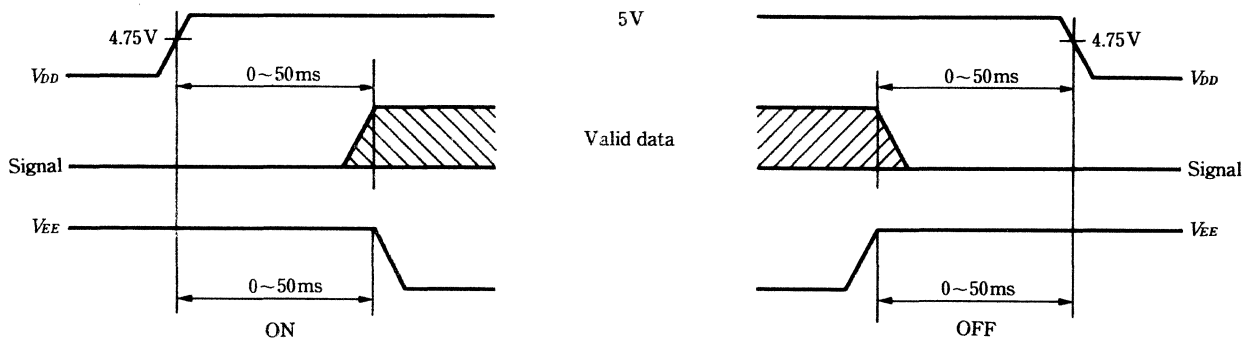


Fig. 5 Voltage sequencing

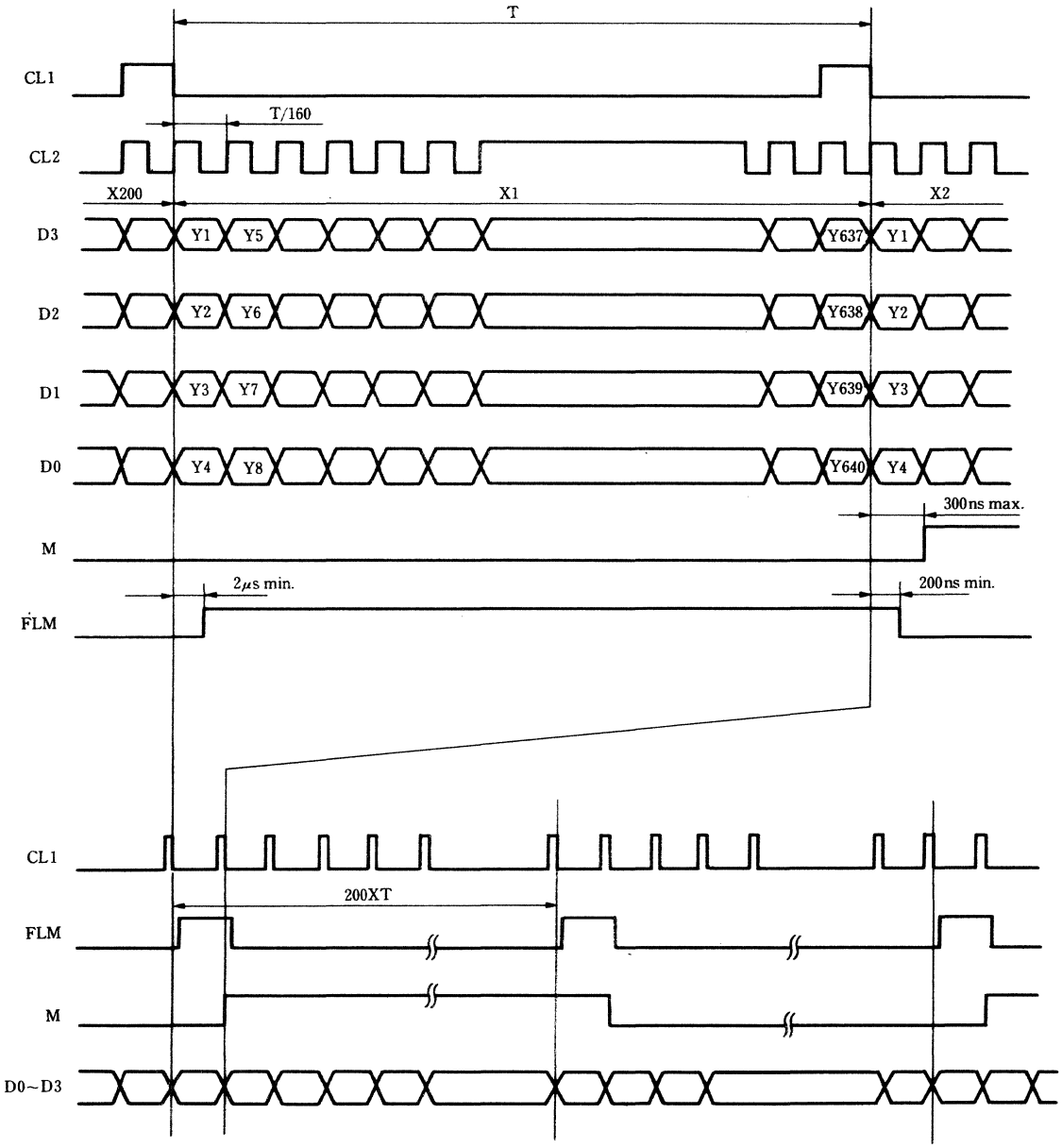


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	410	–	–	ns
CL2 pulse width	t_{CWH}	150	–	–	ns
CL2 pulse width	t_{CWL}	150	–	–	ns
CL1 set up time	t_{SCL1}	150	–	–	ns
CL1 hold time	t_{HCL1}	150	–	–	ns
Clock rise, fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	200	–	–	ns

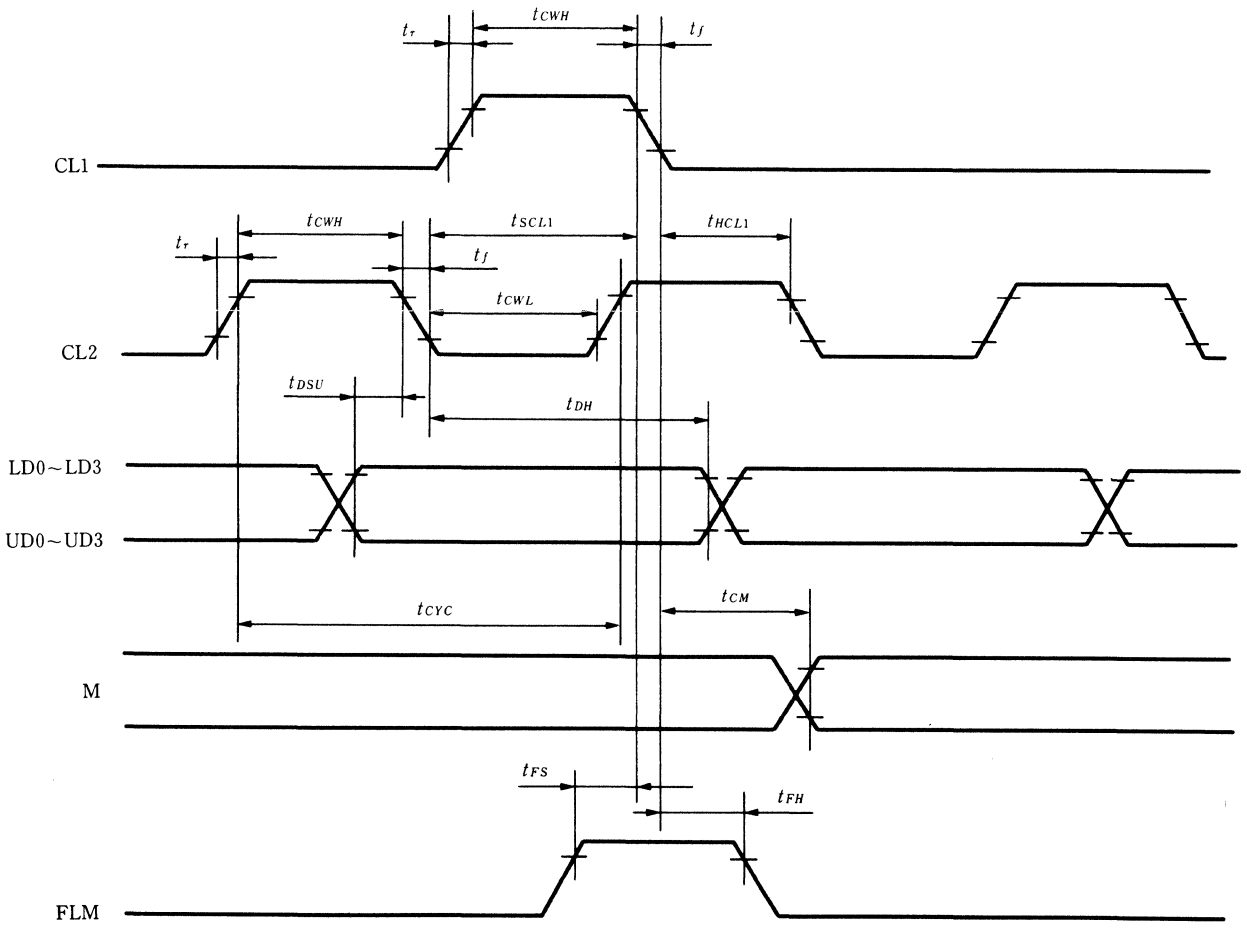


Fig. 7 Interface timing

LM280X

FEATURES

- 640(W) dots × 200(H) dots graphic and alphanumeric display
- Attachable controller: HD63645F

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .270W × 104H × 11T (max.) mm
Effective display area . . . . . .236.4W × 78.0H mm
Number of dots . . . . . .640W × 200H dots
Dot size . . . . . .0.33W × 0.33H mm
Dot pitch. . . . . .0.36W × 0.36H mm

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic (V_{DD} – V_{SS})	–0.3	7.0V
Power supply for LCD drive (V_{DD} – V_{EE})	–0.3	28.0V
Input voltage (Vi) (Note 1)	–0.3	V_{DD} + 0.3V
Operating temperature (Ta) (Note 2)	0 ~ +40°C	
Storage temperature (Tstg) (Note 3)	–20 ~ +60°C	
Humidity (Note 4)	No dew	

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 ± 0.25 V, V_{EE} = –21.5 ± 1 V
Input "high" voltage (V_{IH}) . . . . . .0.7 × V_{DD} V max.
Input "low" voltage (V_{IL}) . . . . . .0.3 × V_{DD}V max.
Power supply current for logic (I_{DD}) (Note 2). . . . . .8 mA typ.
Power supply current for LCD drive (I_{EE}) (Note 2). . . . . .7 mA typ.
Frame frequency (f_{FLM}) . . . . . .65 Hz min.
70 Hz typ.
75 Hz max.
Power supply for LCD drive (Recommended) (V_{DD} – V_0) 1/200 Duty (Note 3)
Ta = 0°C . . . . . 23.0 V typ.
Ta = 25°C . . . . . 21.7 V typ.
Ta = 40°C . . . . . 20.8 V typ.

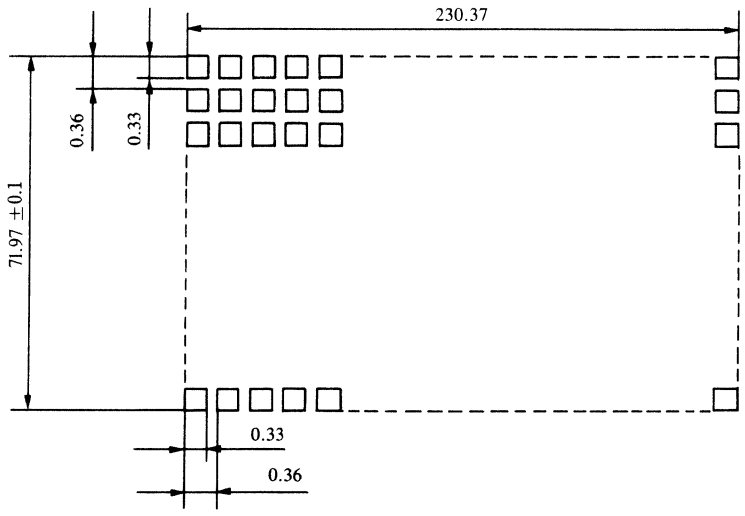
Notes 1. Applied to CL1, CL2, D0 ~ D3, FLM and M.
2. V_{DD} = +5V, V_{DD} – V_0 = 23V, D0 ~ D3 = 1010, FLM = 70 Hz
3. Viewing angle = 10°

Notes 1. Applied to CL1, CL2, D0 ~ D3, FLM and M.
2. The color of the display may change into blue if operated at maximum temperature.
3. Do not leave it for more than 168 hrs. at 60°C.
4. Ta ≤ 40°C . . . . . 85% Rmax.
Ta > 40°C . . . . . Absolute humidity must be below absolute humidity of 85% RH at 40°C.

OPTICAL DATA . . . . . See page 15

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D3	H/L	Data
2	D2	H/L	Data
3	FLM	H	The FLM signal indicating the beginning of each display cycle.
4	M	H/L	Control signal for AC driving
5	CL1	H→L	Data latch
6	CL2	H→L	Data shift
7	D1	H/L	Data
8	D0	H/L	Data
9	V_{DD}	—	Power supply for logic circuit
10	V_{SS}	—	Ground
11	V_{EE}	—	Power supply for LC driving
12	VO	—	Operating voltage for LC driving



Unit : mm

Fig. 1 Display pattern

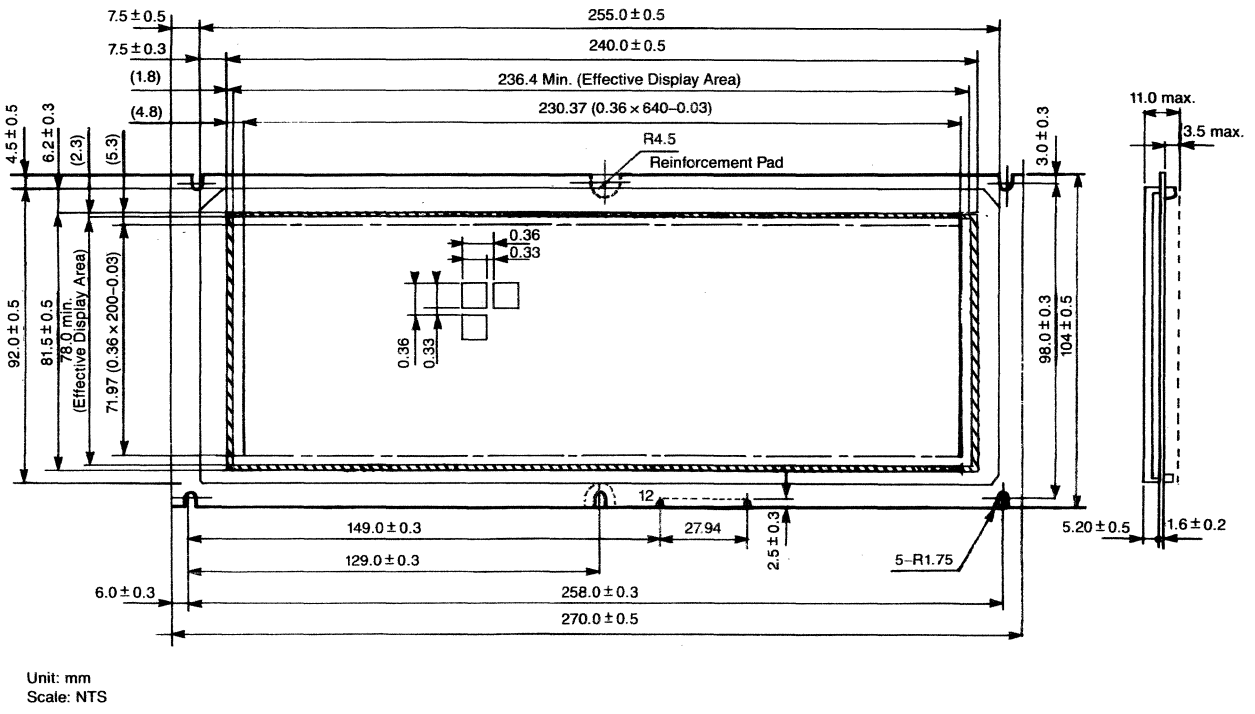


Fig. 2 External dimension

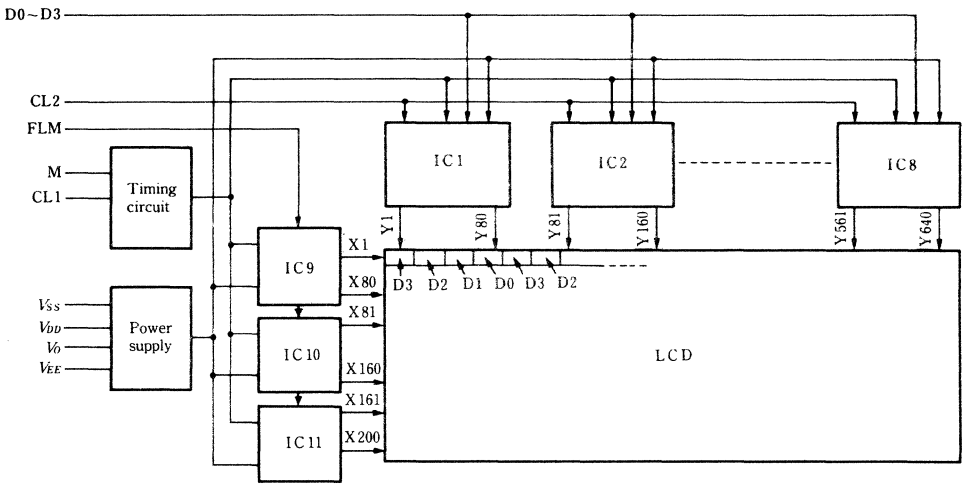
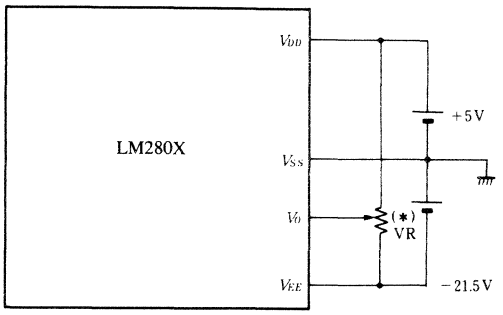


Fig. 3 Block diagram



*VR : 10~20kΩ

Fig. 4 Power supply

Observe the following sequencing when turning power supply on and off.

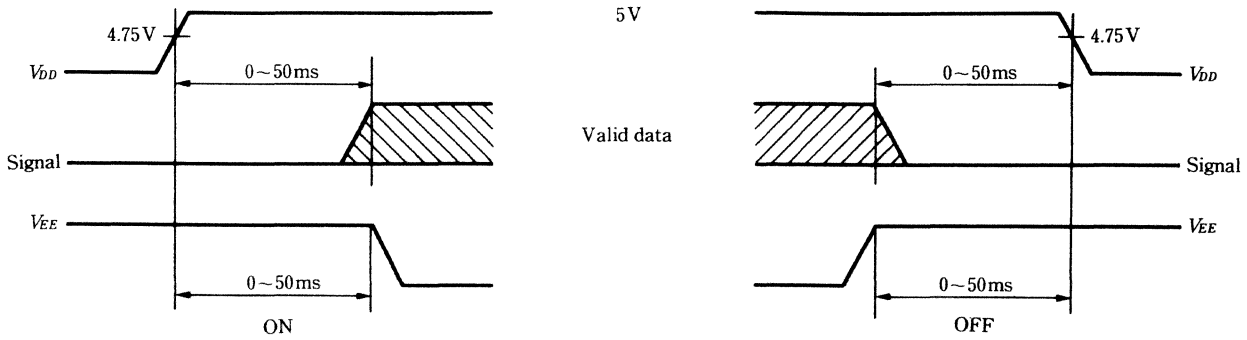


Fig. 5 Voltage sequencing

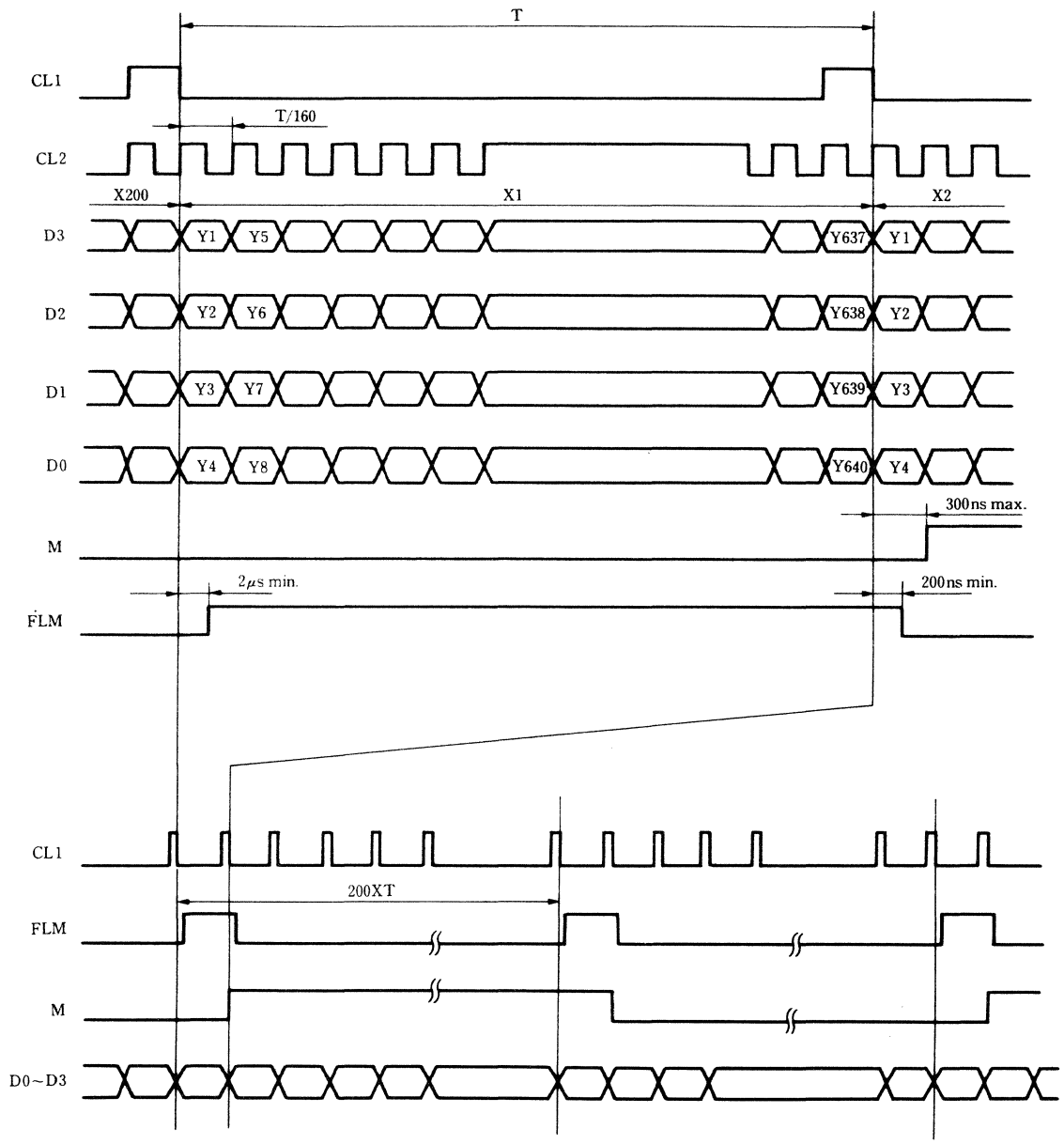


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	410	–	–	ns
CL2 pulse width	t_{CWH}	150	–	–	ns
CL2 pulse width	t_{CWL}	150	–	–	ns
CL1 set up time	t_{SCL1}	150	–	–	ns
CL1 hold time	t_{HCL1}	150	–	–	ns
Clock rise, fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	200	–	–	ns

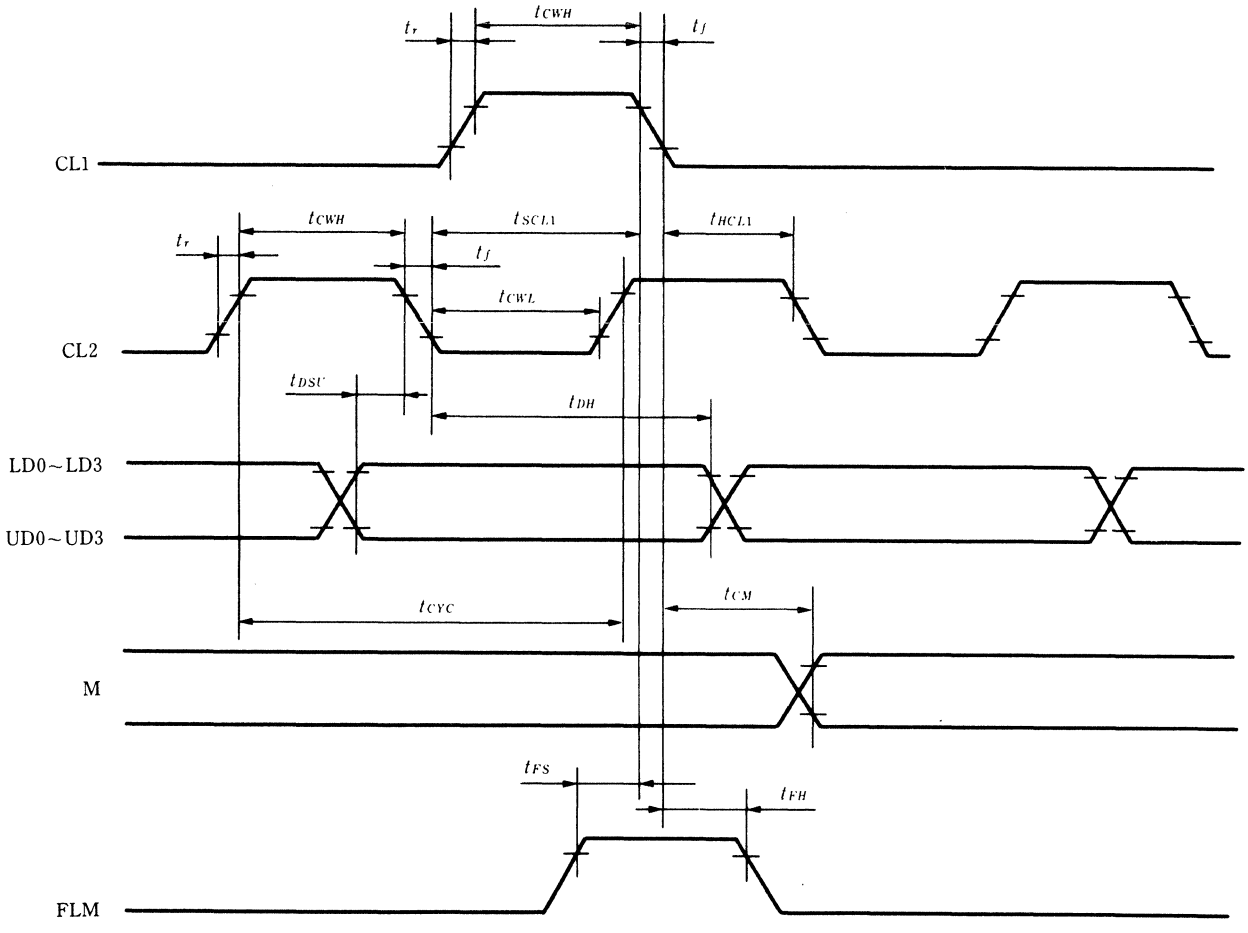


Fig. 7 Interface timing

LM282XP

FEATURES

- 640(W) dots × 400(H) dots graphic and alphanumeric display
- Attachable controller: HD63645F

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .270W × 198H × 11.0T (max.) mm
Effective display area . . . . . .236.0W × 153.6H mm
Number of dots . . . . . .640W × 400H dots
Dot size . . . . . .0.33W × 0.33H mm
Dot pitch. . . . . .0.36W × 0.36H mm
Weight. . . . . .540 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	−0.3	7.0V
Power supply for LCD drive ($V_{DD} - V_{EE}$)	−0.3	28.0V
Input voltage (Vi) (Note 1)	−0.3	V_{DD} + 0.3V
Operating temperature (Ta) (Note 2)	0 ~ +40°C	
Storage temperature (Tstg) (Note 3)	−20 ~ +60°C	

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V, V_{EE} = −21.5 V ± 1 V
Input "high" voltage (V_{IH}) (Note 1) . . . . . .0.7 × V_{DD} V max.
Input "low" voltage (V_{IL}) . . . . . .0.3 × V_{DD} V max.
Power supply current for logic (I_{DD}) (Note 4). . . . . .8 mA typ.
Power supply current for LCD drive (I_{EE}) (Note 4). . . . . .7 mA typ.
Frame frequency (f_{FLM}) . . . . . .65 Hz min.
70 Hz typ.
75 Hz max.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$) 1/200 Duty (Note 5)
Ta = 0°C . . . . . .23.0 V typ.
Ta = 25°C . . . . . .21.7 V typ.
Ta = 40°C . . . . . .20.8 V typ.

Notes 1. Applied to CL1, CL2, UD0 ~ UD3, LD0 ~ LD3, M and FLM.
2. The color of the display may change into blue if operated at maximum temperature. It is recommended to use between 0°C and 40°C.
3. Do not leave it for more than 168 hrs. at maximum or minimum temperature.
4. V_{DD} = +5V, $V_{DD} - V_0$ = 23.0V, UD0 ~ UD3, LD0 ~ LD3 = 1010 . . . . . , f_{FLM} = 70 Hz.
5. Viewing angle = 10°

OPTICAL DATA . . . . . .See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1 ~ 4	UD0 ~ UD3 (1) (4)	H/L	Data (Upper half)
5	NC	–	–
6	FLM	H	The FLM signal indicating the beginning of each display cycle
7	M	H/L	Control signal for AC driving
8	CL1	H → L	Data latch
9	CL2	H → L	Data shift
10 ~ 13	LD0 ~ LD3 (10) (13)	H/L	Data (Lower half)
14	V_{DD}	–	Power supply for logic circuit
15	V_{SS}	–	Ground
16	V_{EE}	–	Power supply for LC driving
17	V_0	–	Operating voltage for LC driving
18 ~ 20	NC	–	–

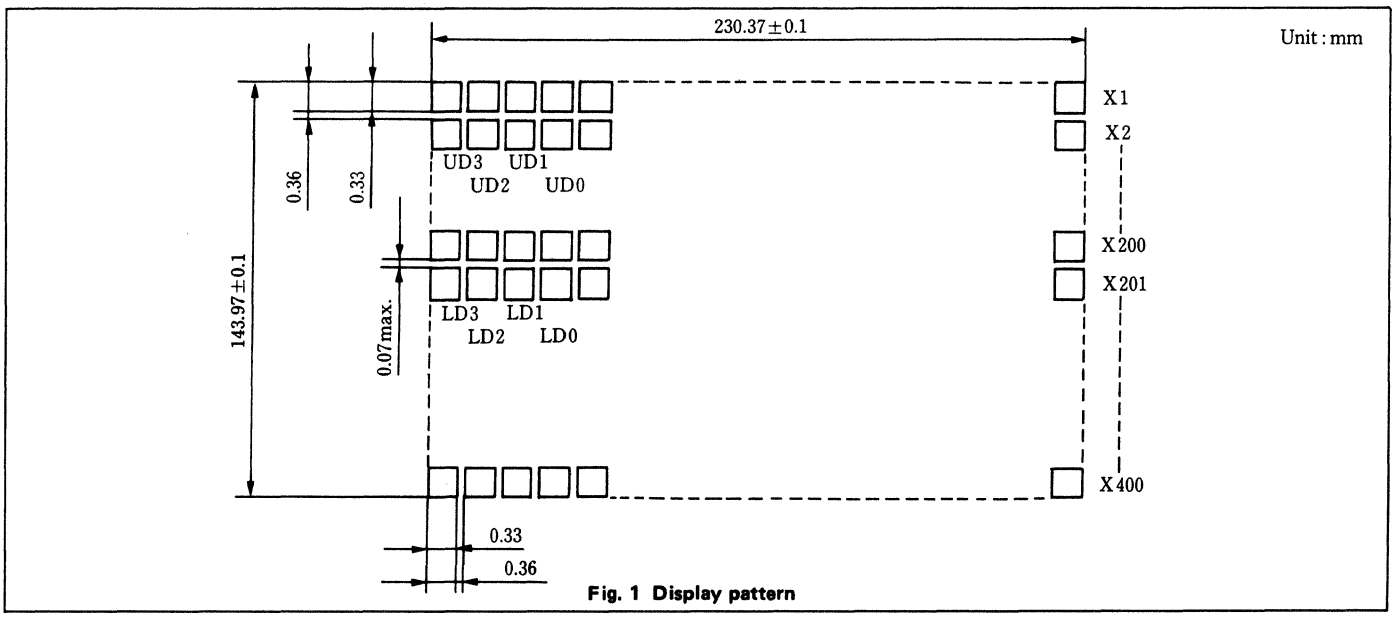


Fig. 1 Display pattern

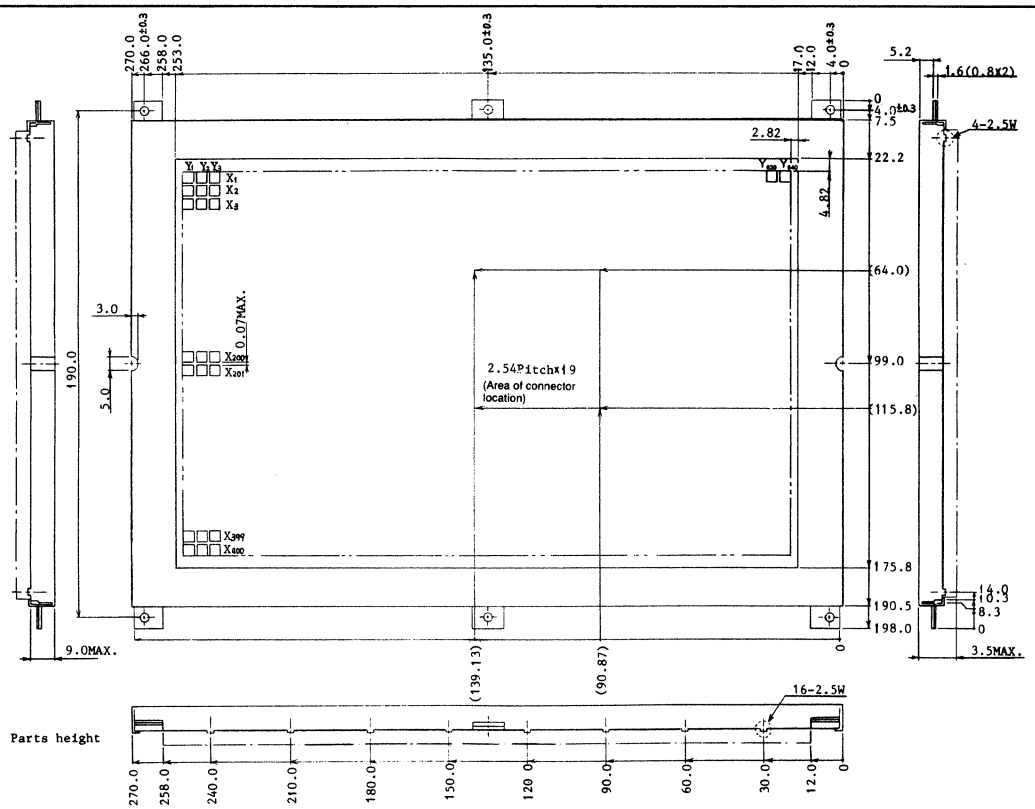
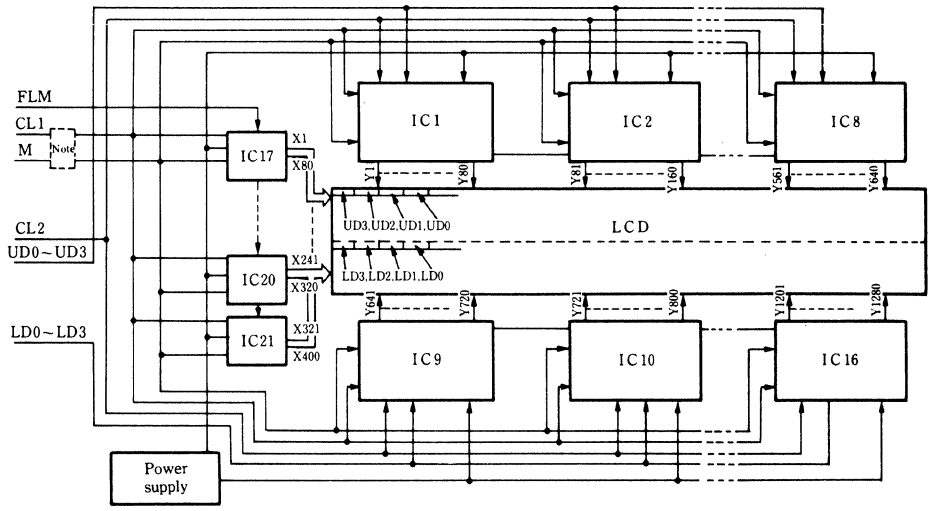
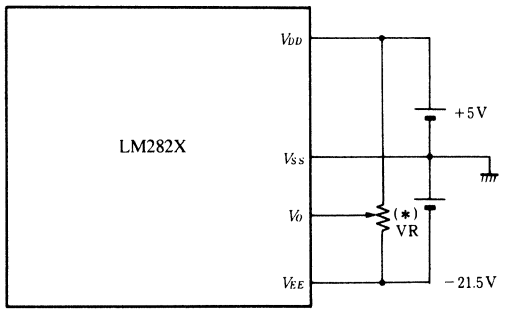


Fig. 2 External dimension



Note: Interface timing circuit

Fig. 3 Block diagram



*VR: 10~20kΩ

Fig. 4 Power supply

Observe the following sequencing when turning power supply on and off.

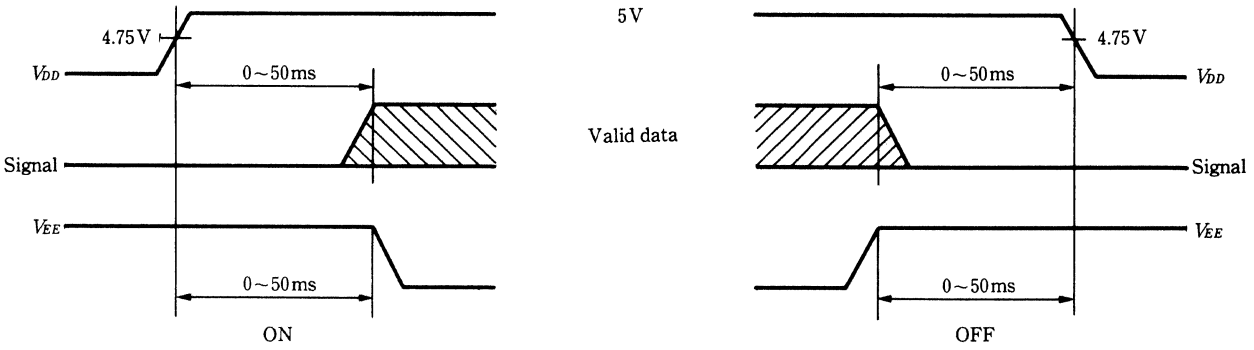


Fig. 5 Voltage sequencing

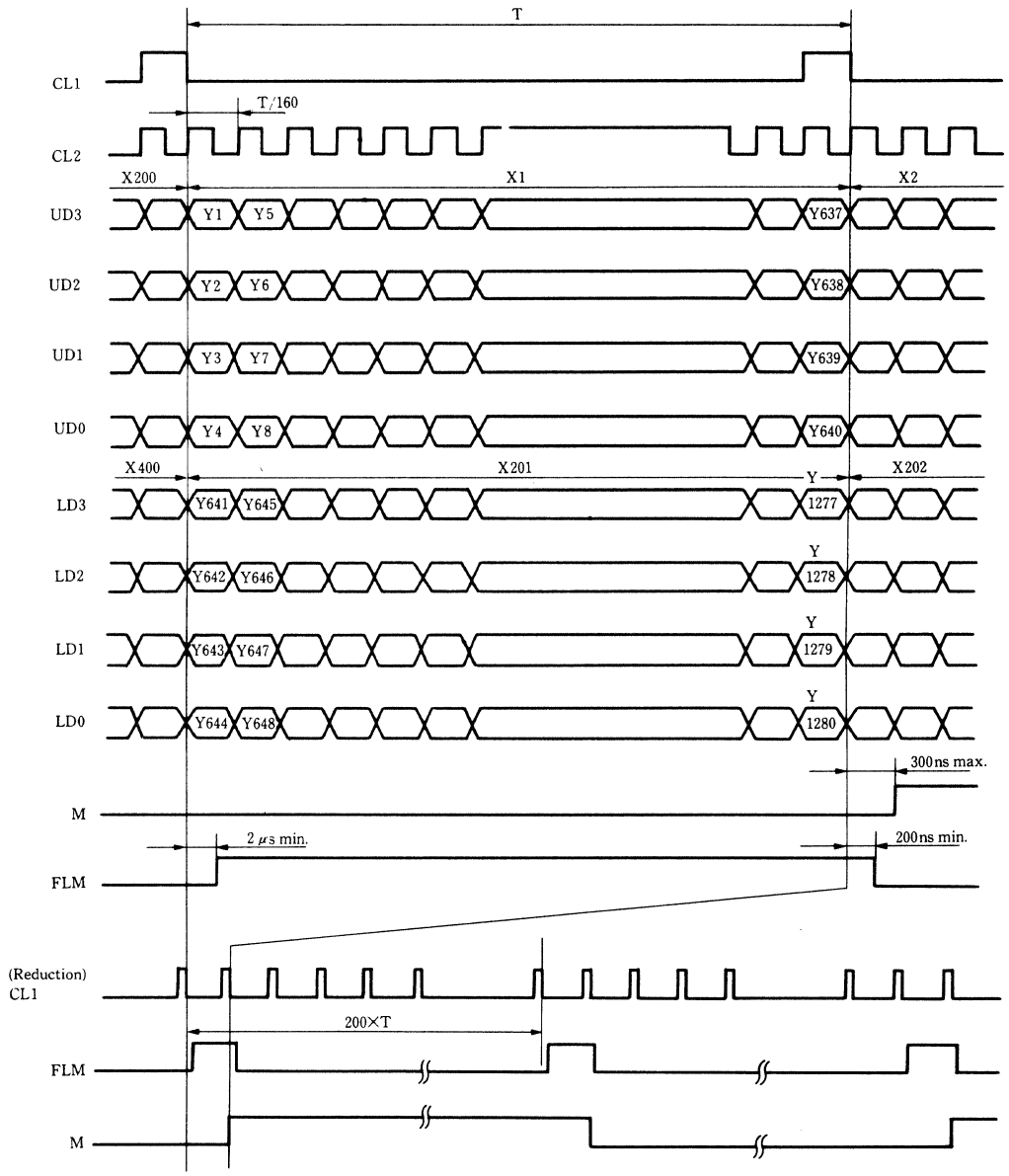


Fig. 6 Interface timing

TIMING CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit
CL2 cycle time	t_{CYC}	410	–	–	ns
CL2 pulse width	t_{CWH}	150	–	–	ns
CL2 pulse width	t_{CWL}	150	–	–	ns
CL1 set up time	t_{SCL1}	150	–	–	ns
CL1 hold time	t_{HCL1}	150	–	–	ns
Clock rise, fall time	t_r, t_f	–	–	30	ns
Data set up time	t_{DSU}	100	–	–	ns
Data hold time	t_{DH}	100	–	–	ns
M delay time	t_{CM}	–	–	300	ns
FLM set up time	t_{FS}	200	–	–	ns
FLM hold time	t_{FH}	200	–	–	ns

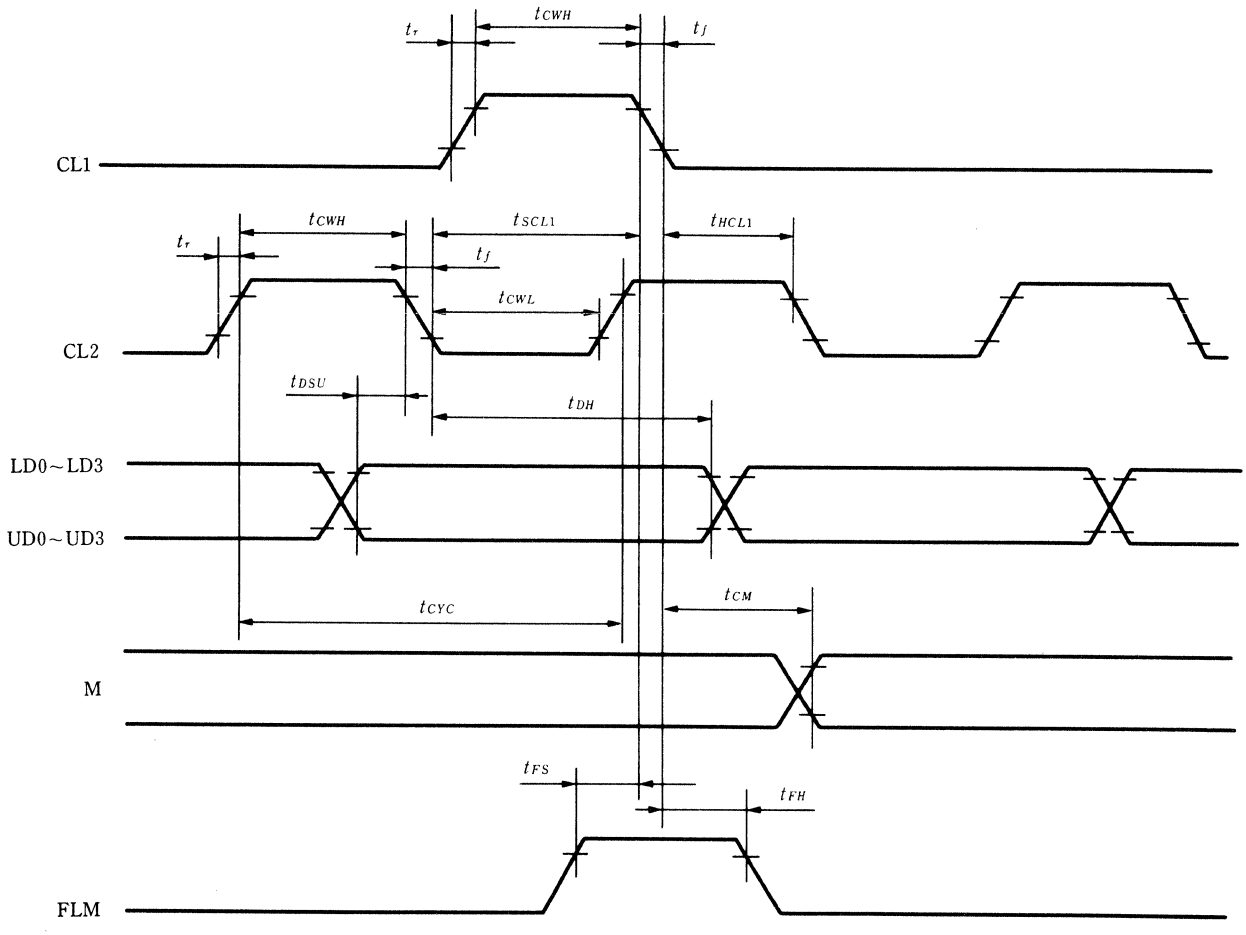


Fig. 7 Interface timing

CHARACTER MODULE DETAIL DATA 5

SEGMENT TYPE LCD MODULE

This is a segment type LCD module containing the controller LSI for numerical display.

LM039

- 7 segment x 16 digits
- Controller LSI μPD7225G is built-in
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size ..... 87.0W x 27.5H x 11.0T (max.) mm
Effective display area ..... 64.7W x 13.3H mm
Character size ..... 2.2W x 6.4H mm
Character pitch ..... 3.9 mm

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V
Input "high" voltage (V_{IH}) ..... 0.7 V_{DD} V min.
Input "low" voltage (V_{IL}) ..... 0.3 V_{DD} V max.
Output "high" voltage (V_{OH})
($-I_{OH}$ = 10 μA) ..... V_{DD} − 0.5 V min.
Output "low" voltage (V_{OL})
(I_{OL} = 100 μA) ..... 0.5 V max.
Power supply current (I_{DD})
(V_{DD} = 5.0 V) ..... 0.21 mA typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Du = 1/4

Power supply for LCD drive (Recommended) ($V_{DD} - V_0$)
Duty = 1/4
Ta = 0°C ..... 3.32 V typ.
Ta = 25°C ..... 3.15 V typ.
Ta = 50°C ..... 2.70 V typ.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Function
1	V_{SS}	Ground
2	V_{DD}	Power supply positive (5V)
3	V_0	LCD driving voltage
4	$\overline{SCK}$	Serial clock input
5	SI	Serial input
6	$\overline{CS}$	Chip select input
7	$\overline{BUSY}$	Busy output
8	C/$\overline{D}$	Command/Data select
9	$\overline{RESET}$	Reset input
10	NC	No connection

Unit: mm

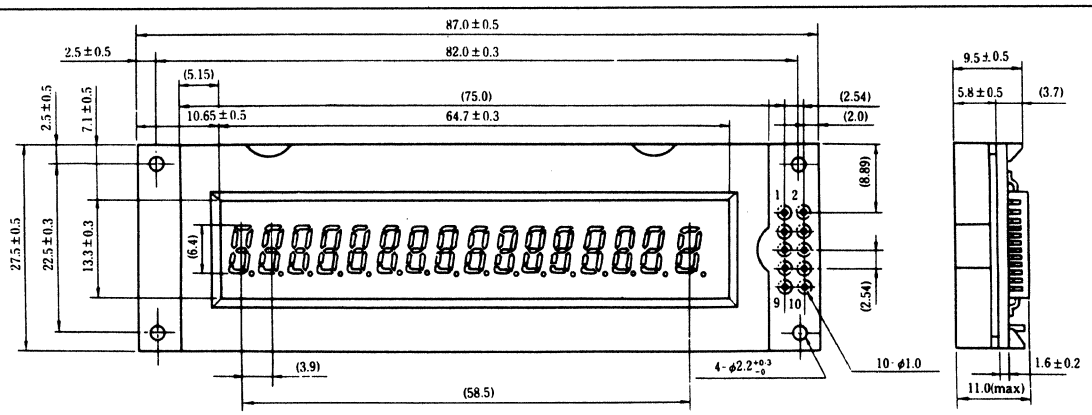


Fig. 1 External dimension

Unit: mm

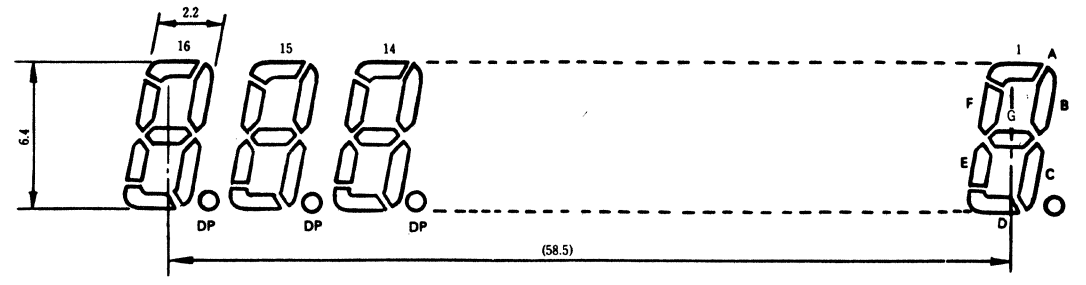
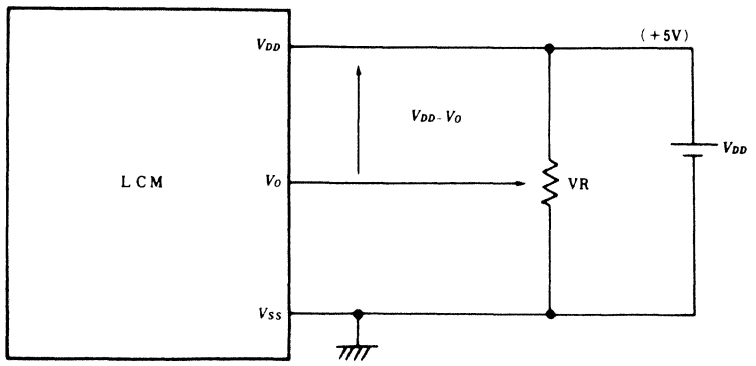


Fig. 2 Display pattern

HITACHI



$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 3 Power supply

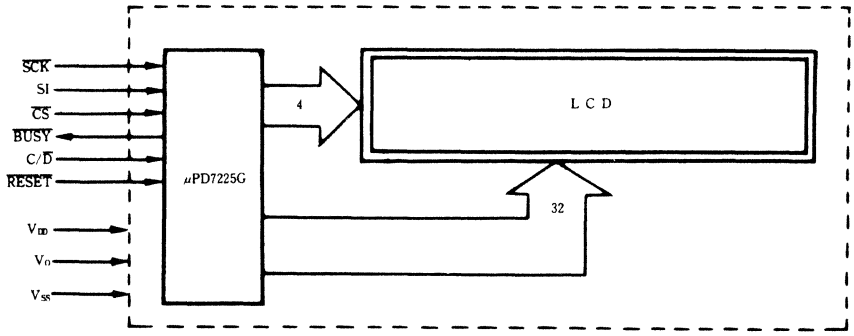


Fig. 4 Block diagram

INTERFACE TIMING

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle	t_{CYK}		900			ns
$\overline{SCK}$ pulse width high	t_{WHK}		400			ns
$\overline{SCK}$ pulse width low	t_{WLK}		400			ns
$\overline{BUSY}\downarrow \rightarrow \overline{SCK}\downarrow$ hold time	t_{HBK}		0			ns
SI setup time to $\overline{SCK}\uparrow$	t_{SIK}		100			ns
SI hold time after $\overline{SCK}\uparrow$	t_{HKI}		200			ns
8th $\overline{SCK}\uparrow \rightarrow \overline{BUSY}\downarrow$ delay time	t_{DKB}	CL = 50pF			3	μs
$\overline{CS}\downarrow \rightarrow \overline{BUSY}\downarrow$ delay time	t_{DCSB}	CL = 50pF			1.5	μs
C/$\overline{D}$ setup time to 8th $\overline{SCK}\uparrow$	t_{SDK}		9			μs
C/$\overline{D}$ hold time after 8th $\overline{SCK}\uparrow$	t_{HKD}		1			μs
$\overline{CS}$ hold time after 8th $\overline{SCK}\uparrow$	t_{HKCS}		1			μs
$\overline{CS}$ pulse width high	t_{WHCS}		40			μs
$\overline{CS}$ pulse width low	t_{WLCS}		40			μs

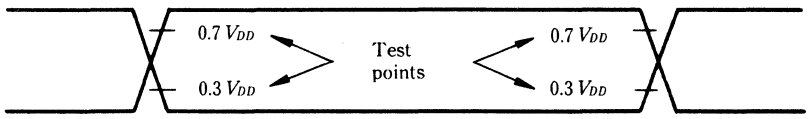


Fig. 5 A.C Timing Measurement voltage

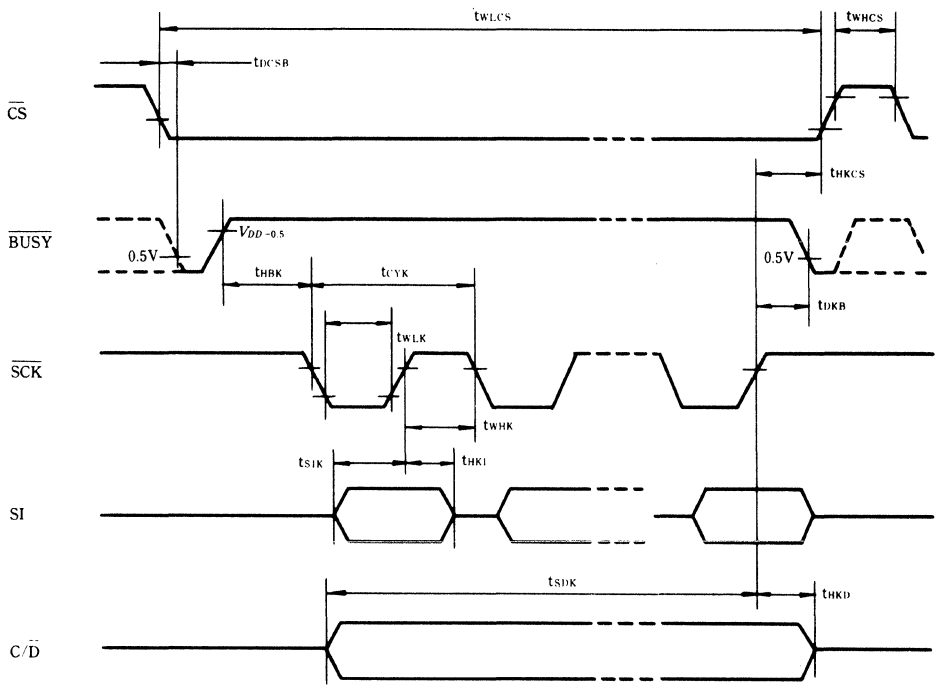


Fig. 6 Timing waveforms

Note : Power on sequence

(1) Power supply voltage should be applied to LCD module as figure 7.

(2) Input signals should not be applied to LCD module before power supply voltage is applied and reaches to specified voltage (5V ±0.5V).

If above sequence is not kept, C-MOS LSIs of LCD modules may be damaged due to latch up problem.

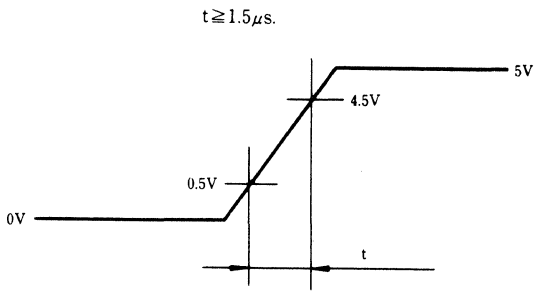


Fig. 7 Power supply voltage

DEOODED DISPLAY RAM DATA

Display byte (HEX)	Character	4-backplane multiplex Display RAM address N+1	N
0 0	0.	D	7
0 1	1.	O	6
0 2	2.	E	3
0 3	3.	A	7
0 4	4.	3	6
0 5	5.	B	5
0 6	6.	F	5
0 7	7.	O	7

Display byte (HEX)	Character	4-backplane multiplex Display RAM address N+1	N
0 8	8.	F	7
0 9	9.	F	7
0 A	A.	2	0
0 B	b.	F	1
0 C	C.	D	1
0 D	d.	A	0
0 E	E.	E	4
0 F	F.	O	0

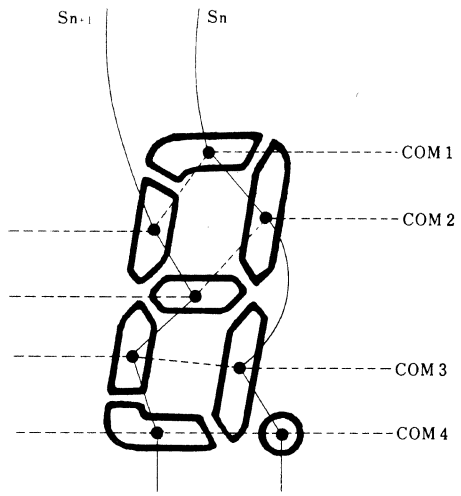


Fig. 8 Connection diagram

COMMAND

Command	Description	Instruction code								
		Binary								HEX
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1. MODE SET	Initialize the μPD7225 1) LCD Drive Configuration 2) LCD Bias Voltage Configuration 3) LCD Frame Frequency	0	1	0	0	0	0	1	0	42
2. UNSYNCHRONOUS DATA TRANSFER	Synchronize Display RAM data transfer to Display Latch with $\overline{CS}$	0	0	1	1	0	0	0	0	30
3. SYNCHRONOUS DATA TRANSFER	Synchronize Display RAM data transfer to Display Latch with LCD Drive Cycle	0	0	1	1	0	0	0	1	31
4. INTERRUPT DATA TRANSFER	Interrupt Display RAM data transfer to Display Latch	0	0	1	1	1	0	0	0	38
5. LOAD DATA POINTER	Load Data Pointer with 5 bits of Immediate Data	1	1	1	D_4	D_3	D_2	D_1	D_0	EO~FF
6. CLEAR DISPLAY RAM	Clear the Display RAM and reset the Data Pointer	0	0	1	0	0	0	0	0	20
7. WRITE DISPLAY RAM	Write 4 bits of Immeditae Data to the Display RAM Location addressed by the Data Pointer : Increment Data Pointer	1	1	0	1	D_3	D_2	D_1	D_0	DO~DF
8. AND DISPLAY RAM	Perform a Logical AND between the Display RAM data addressed by the Data Pointer and 4 bits of Immediate Data : Write result to same Display RAM Location. Increment Data Pointer	1	0	0	1	D_3	D_2	D_1	D_0	90~9F
9. OR DISPLAY RAM	Perform a Logical OR between the Display RAM data addressed by the Data Pointer and 4 bits of Immediate Data : Write result to same Display RAM Location : Increment Data Pointer	1	0	1	1	D_3	D_2	D_1	D_0	BO~BF
10. ENABLE SEGMENT DECODER	Start use of the Segment Decoder	0	0	0	1	0	1	0	1	15
11. DISABLE SEGMENT DECODER	Stop use of the Segment Decoder	0	0	0	1	0	1	0	0	14
12. ENABLE DISPLAY	Turn on the LCD	0	0	0	1	0	0	0	1	11
13. DISABLE DISPLAY	Turn off the LCD	0	0	0	1	0	0	0	0	10
14. CLEAR BLINKING RAM	Clear the Blinking RAM and reset the Data Pointer	0	0	0	0	0	0	0	0	00
15. WRITE BLINKING RAM	Write 4 bits of Immediate Data to the Blinking RAM Location addressed by the Data Pointer : Increment Data Pointer	1	1	0	0	D_3	D_2	D_1	D_0	CO~CF
16. AND BLINKING RAM	Perform a Logical AND between Blinking RAM data addressed by the Data Pointer and 4 bits of Immediate Data : Write result to same Blinking RAM Location : Increment Data Pointer	1	0	0	0	D_3	D_2	D_1	D_0	80~8F
17. OR BLINKING RAM	Perform a Logical OR between Blinking RAM data addressed by the Data Pointer and 4 bits of Immediate Data : Write resuit to same Blinking Location : Increment Data Pointer	1	0	1	0	D_3	D_2	D_1	D_0	AO~AF
18. ENABLE BLINKING	Start Segment Blinking at the Frequency Specified by 1 bit of immediata Data	0	0	0	1	1	0	1	D_0	1A~1B
19. DISABLE BLINKING	Stop Segment Blinking	0	0	0	1	1	0	0	0	18

LCD MODULE WITH BUILT-IN CONTROLLER LSI

This is a dot matrix LCD module containing the controller LSI HD44780 (LCD-II) for character display. Functions such as control, refresh, and display are operated by the built-in controller LSI, HD44780 (LCD-II).

This LCD module can display 160 type JIS characters and symbols and 32 type special characters and symbols. This LCD module can be interfaced to the 4-bit or 8-bit MPU, so the character display and the display shift can be easily operated by using control commands. This LCD module also contains the character generator RAM, hence user's patterns can be displayed.

LM054

- 8 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5 V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 84W x 44H x 12D (max.) mm
Effective display area . . . . . 61W x 15.8H mm
Character size (5 x 7 dots) . . . . . 6.45W x 9.4H mm
Character pitch . . . . . 7.15 mm
Dot size . . . . . 1.25W x 1.3H mm
Weight . . . . . about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
2.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/8
Ta = 0°C . . . . . 4.2 V typ.
Ta = 25°C . . . . . 3.7 V typ.
Ta = 50°C . . . . . 3.2 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

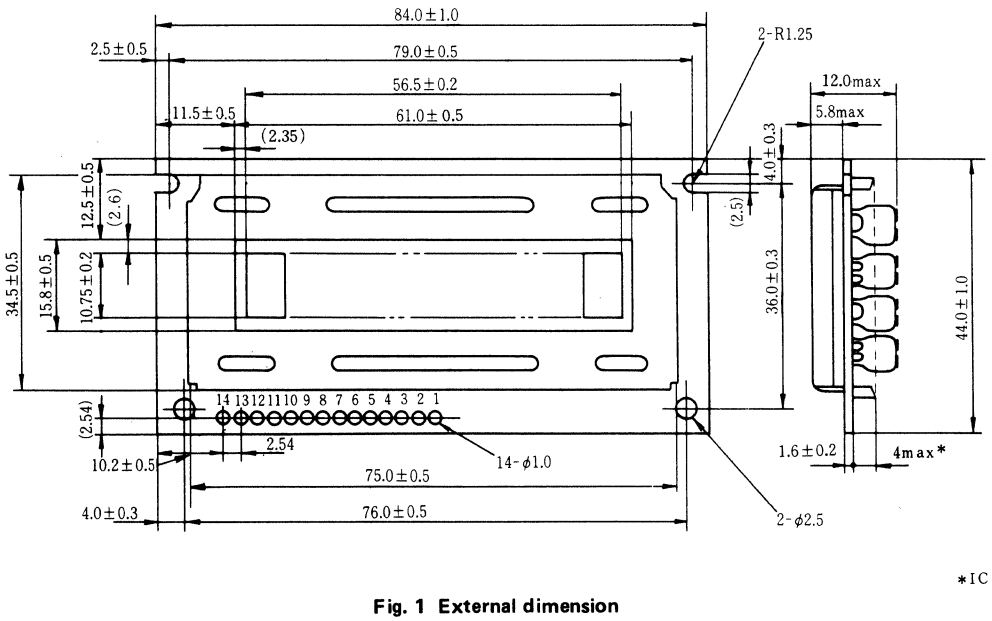


Fig. 1 External dimension

HITACHI

Unit: mm

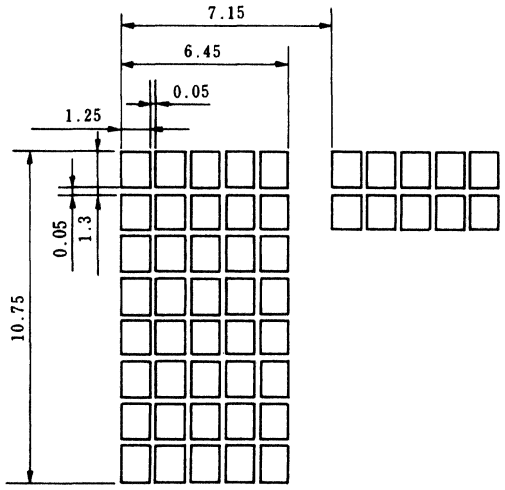


Fig. 2 Display pattern

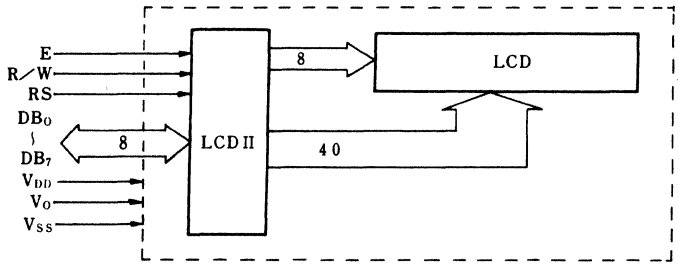


Fig. 3 Block diagram

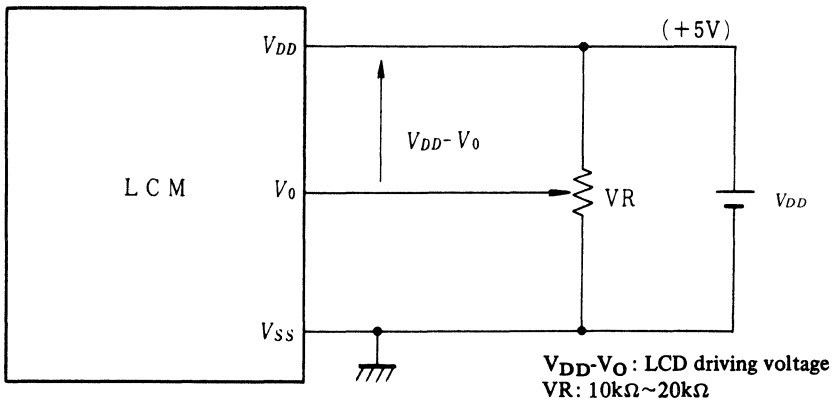


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

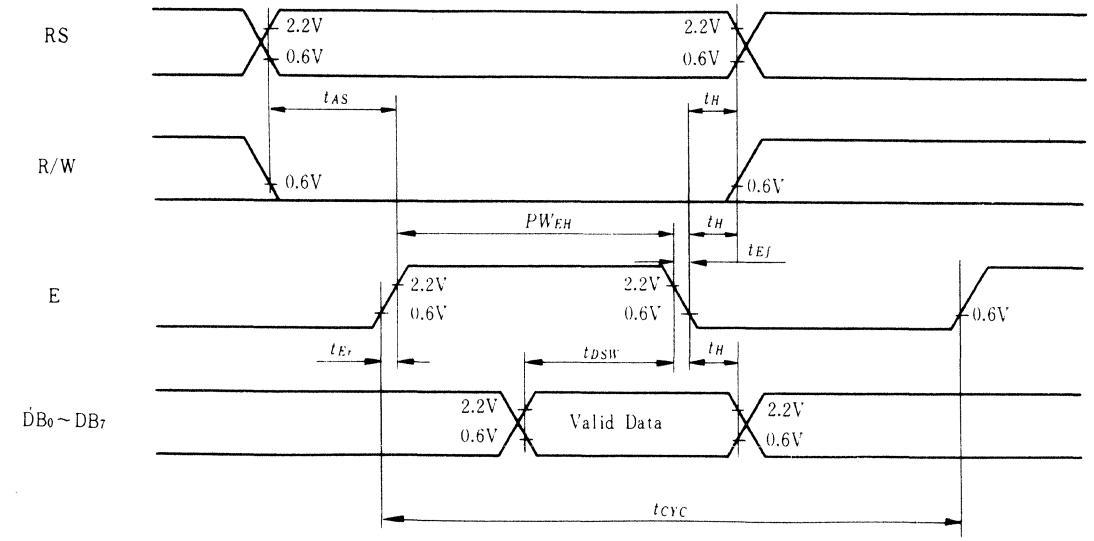


Fig. 5 Interface timing (data write)

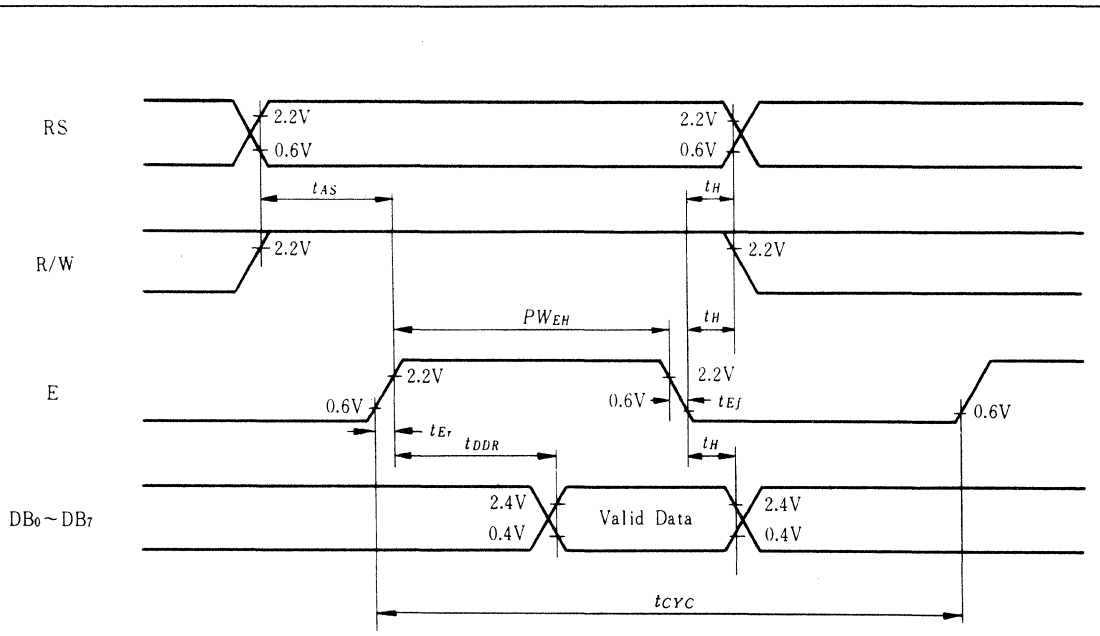


Fig. 6 Interface timing (data read)

H2570

- 16 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	80W x 36H x 12D (max) mm
Effective display area	64.5W x 13.8H mm
Character size (5 x 10 dots)	3.15W x 7.9H mm
Character pitch	3.75 mm
Dot size	0.55W x 0.7H mm
Weight	about 25g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.	
Input "low" voltage (Vi_L)	0.6 V max.	
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.	
Output low voltage (V_{OL}) (I_{OL} = 1.6 mA)	0.4 V max.	
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	0.5 mA typ.	2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

	Duty = 1/8	Duty = 1/11
Ta = 0°C	3.95	4.15 V typ.
Ta = 25°C	3.7	3.8 V typ.
Ta = 50°C	3.3	3.3 V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

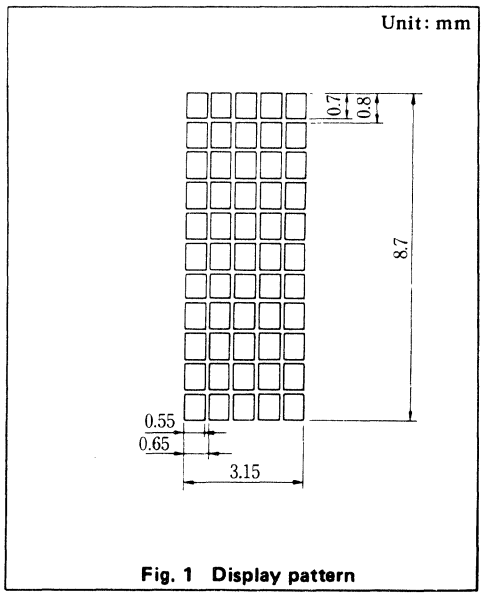


Fig. 1 Display pattern

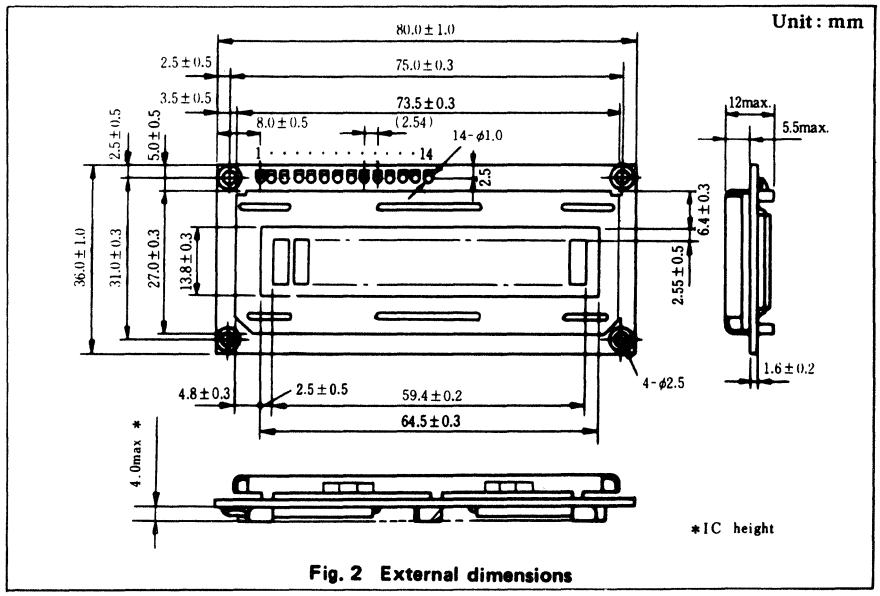


Fig. 2 External dimensions

SECTION 5

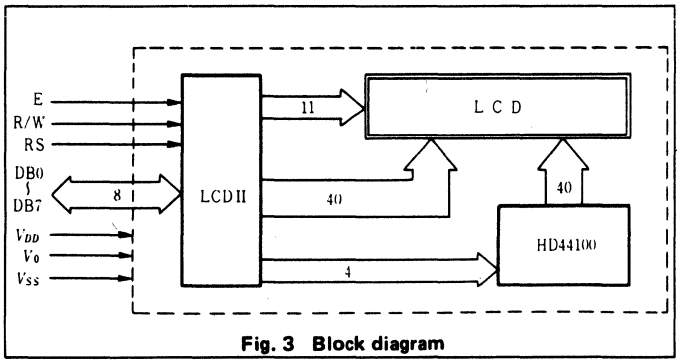


Fig. 3 Block diagram

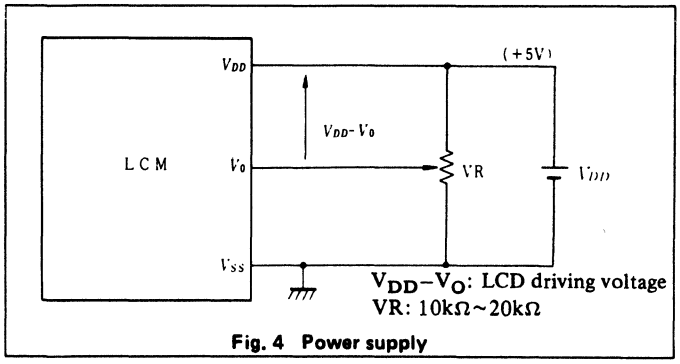


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

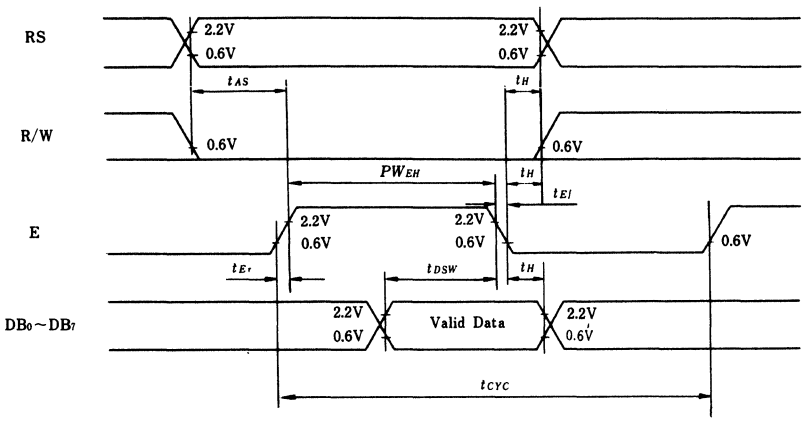


Fig. 5 Interface timing (data write)

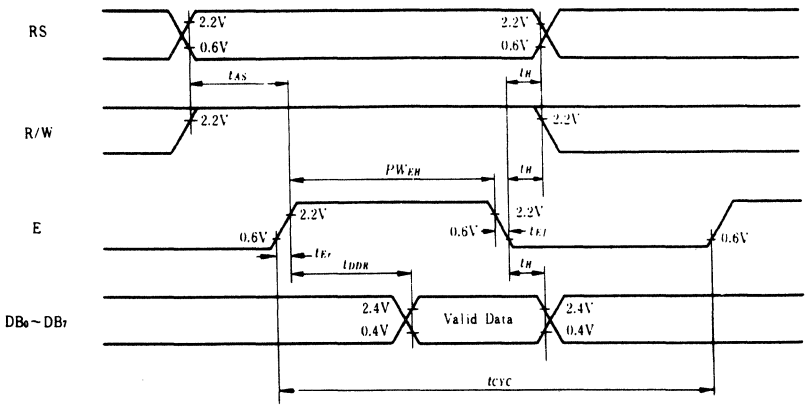


Fig. 6 Interface timing (data read)

LM015

- 16 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 80W x 36H x 12D (max) mm
Effective display area . . . . . 64.5W x 13.8H mm
Character size (5 x 7 dots) . . . . . 3.15W x 5.5H mm
Character pitch . . . . . 3.75 mm
Dot size . . . . . 0.55W x 0.7H mm
Weight . . . . . about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$) . . .	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$) .	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0V ± 0.25 V
Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL}= 1.6 mA) . . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 0.5 mA typ.
2.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/8
Ta = 0°C . . . . . 3.95 V typ.
Ta = 25°C . . . . . 3.7 V typ.
Ta = 50°C . . . . . 3.3 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

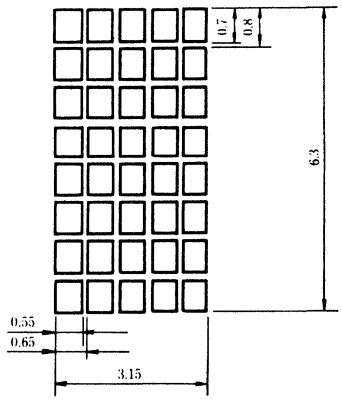


Fig. 1 Display pattern

Unit: mm

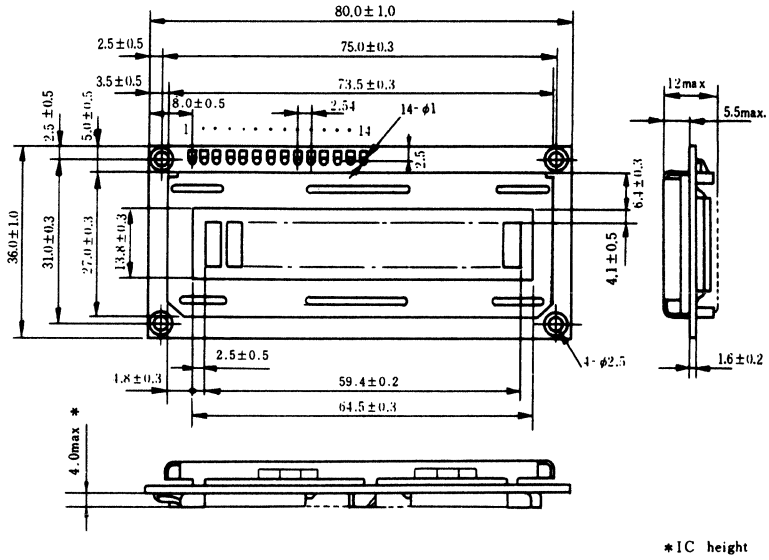


Fig. 2 External dimensions

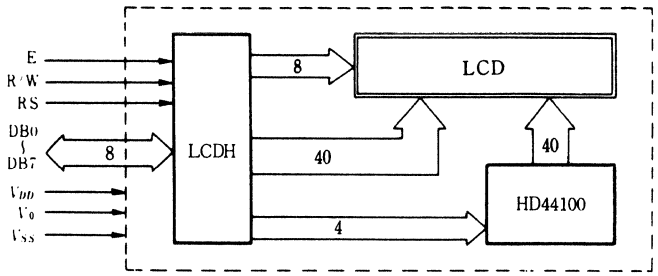
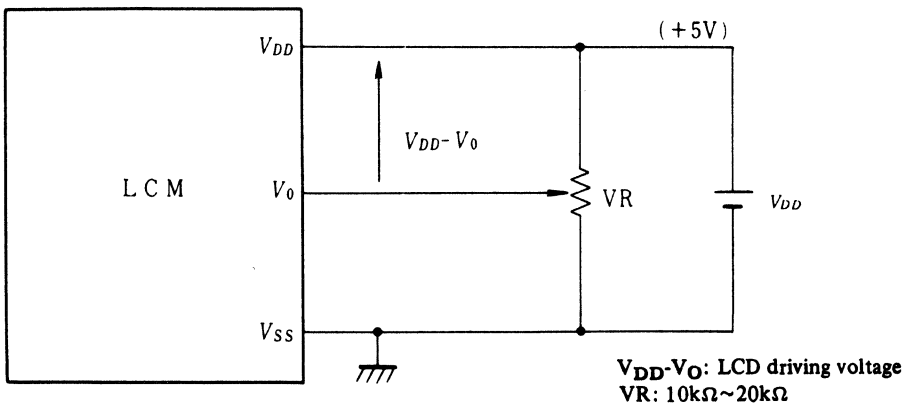


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

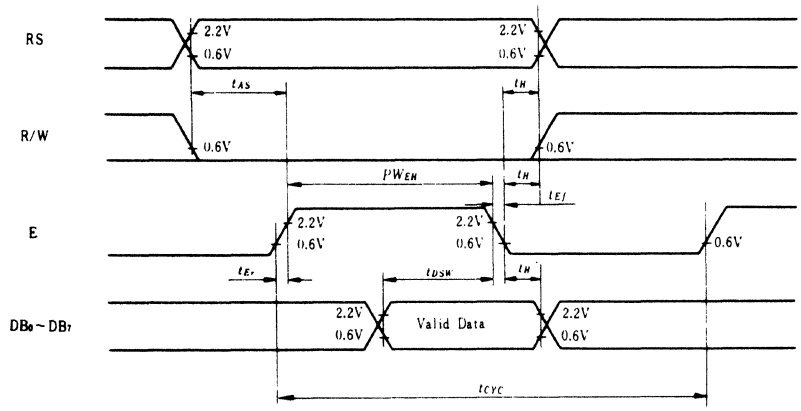


Fig. 5 Interface timing (data write)

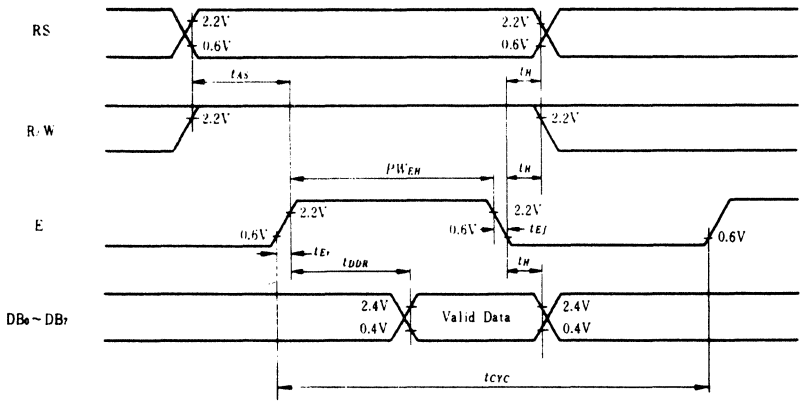


Fig. 6 Interface timing (data read)

LM568AF

- 16 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 122W x 33H x 12.0T (max.) mm
Effective display area . . . . . 99W x 13H mm
Character size (5 x 7 dots) . . . . . 4.84W x 8.06H mm
Character pitch . . . . . 6.0 mm
Dot size . . . . . 0.92W x 1.1H mm
Weight . . . . . about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$) . . .	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$) .	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0V ± 0.25 V
Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
2.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/8
Ta = 0°C . . . . . 4.1 V typ.
Ta = 25°C . . . . . 3.9 V typ.
Ta = 50°C . . . . . 3.7 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

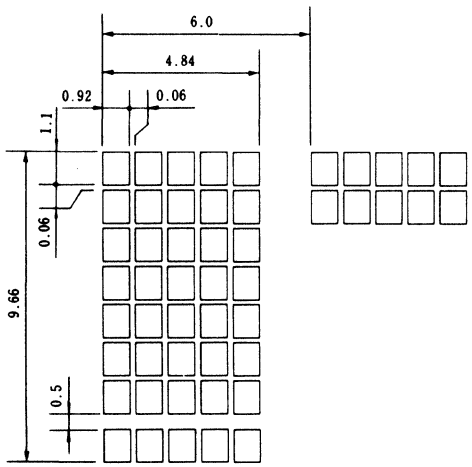


Fig. 1 Display pattern

Unit: mm

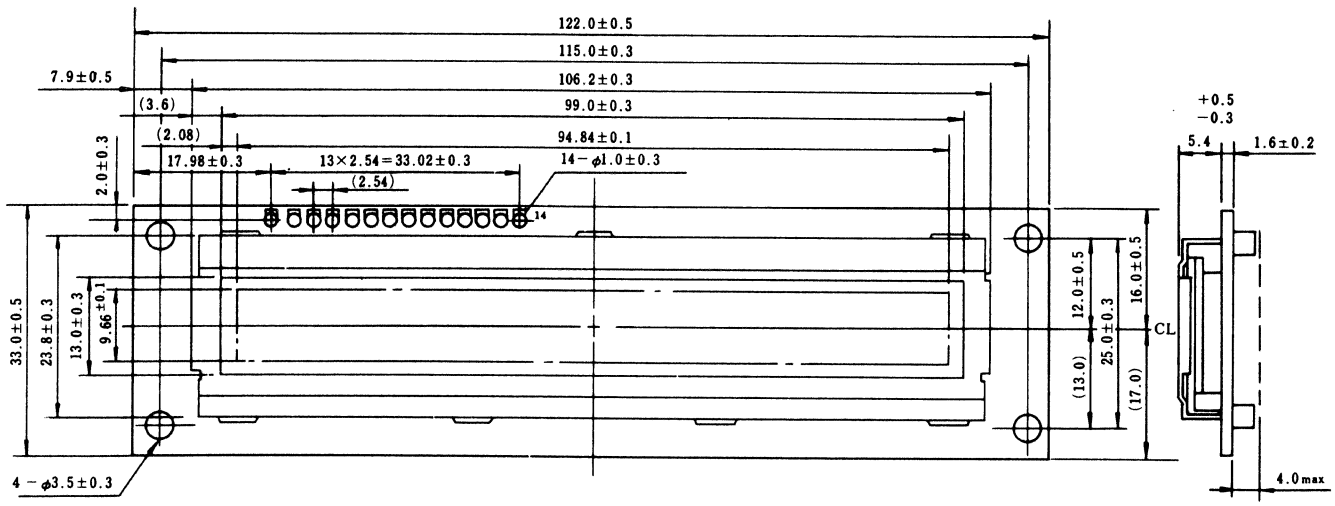


Fig. 2 External dimension

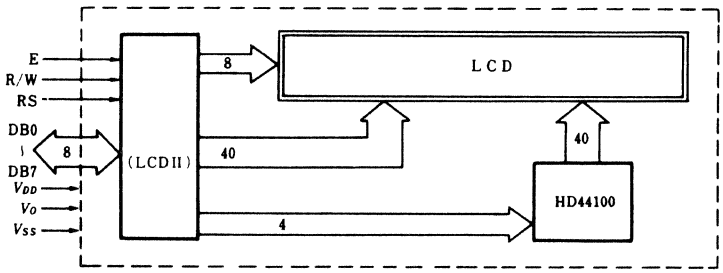
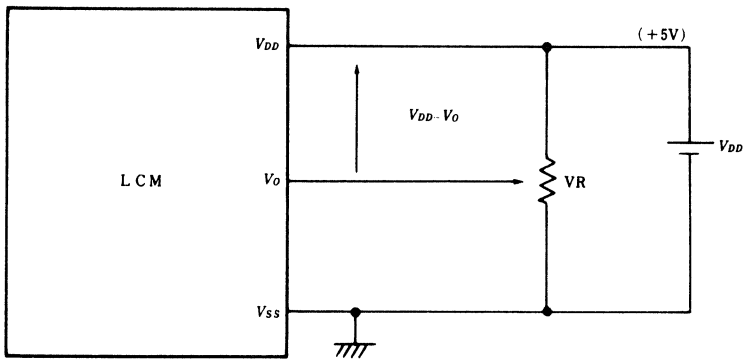


Fig. 3 Block diagram



$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

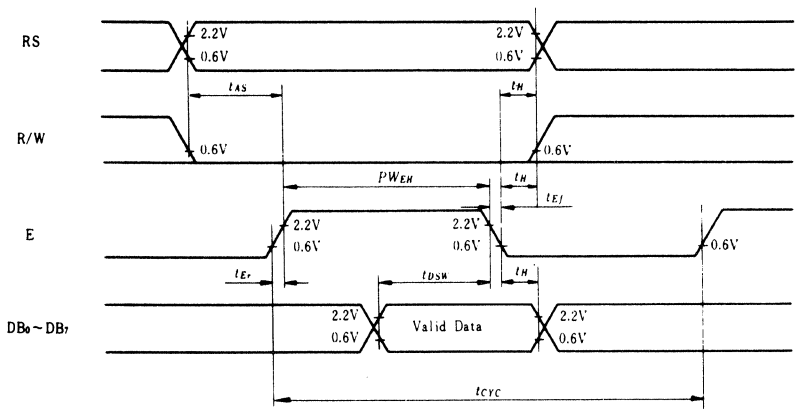


Fig. 5 Interface timing (data write)

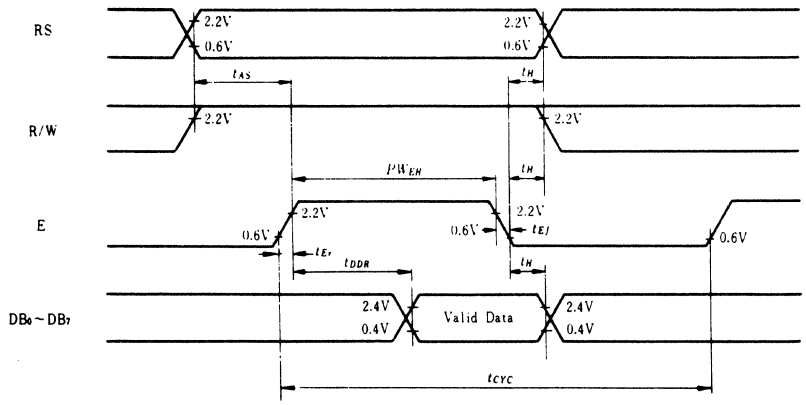


Fig. 6 Interface timing (data read)

LM020L

- 16 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	80W x 36H x 12T (max.) mm
Effective display area	64.5W x 13.8H mm
Character size (5 x 7 dots)	3.07W x 5.73H mm
Characrer pitch	3.77 mm
Dot size	0.55W x 0.75H mm
Weight	about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ.
	2.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)	Duty = 1/16
Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

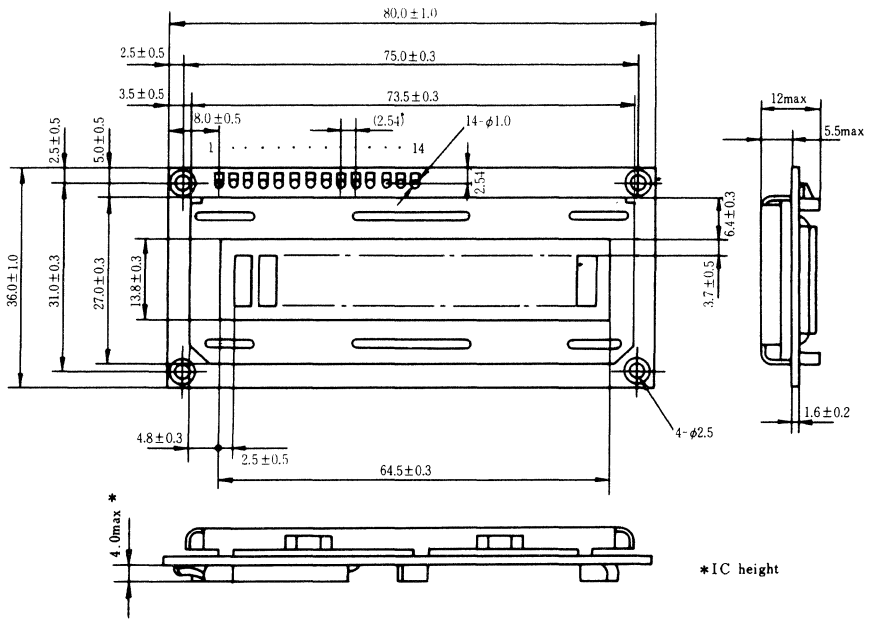


Fig. 1 External dimension

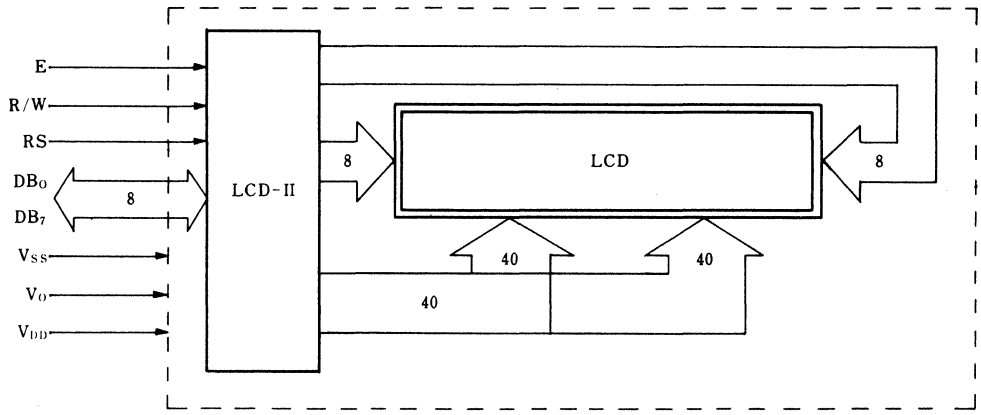


Fig. 2 Block diagram

Unit: mm

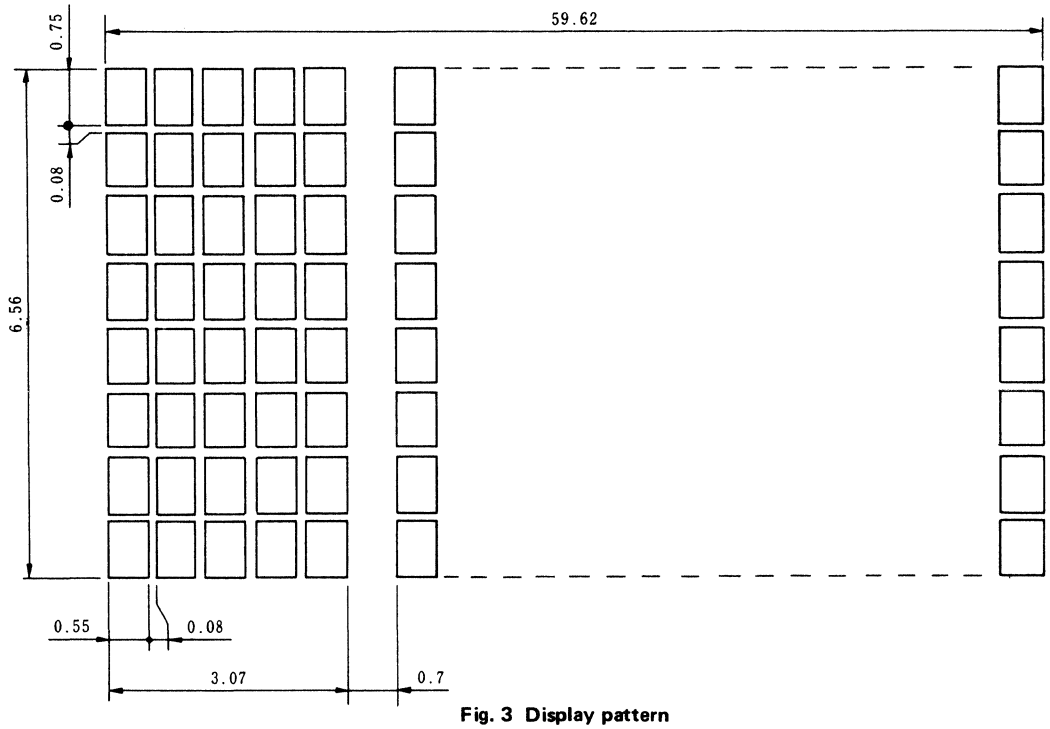
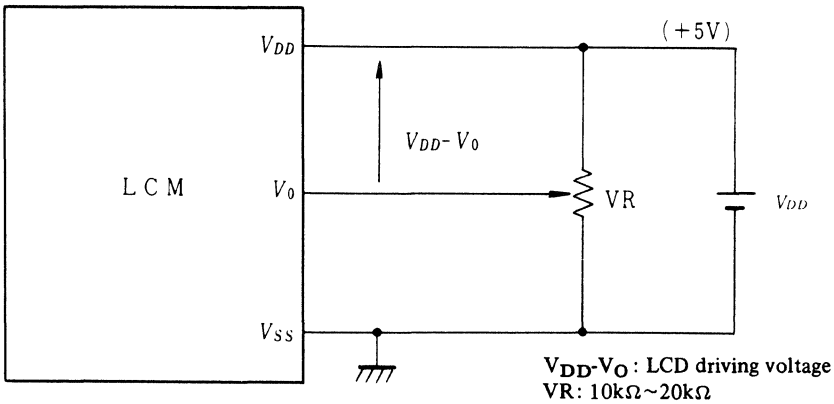


Fig. 3 Display pattern



V_{DD}-V_O : LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

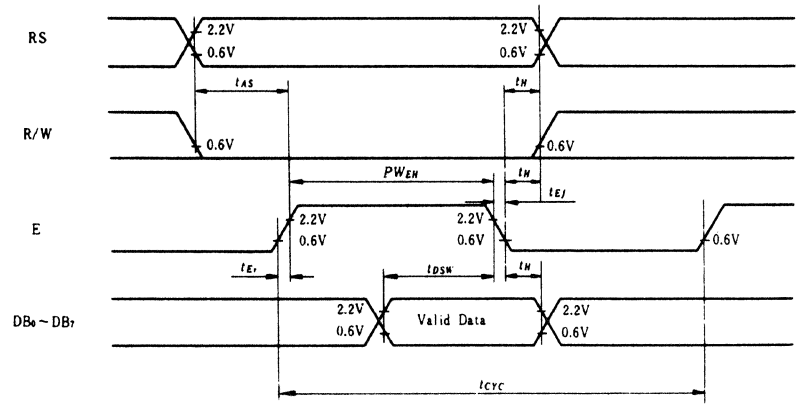


Fig. 5 Interface timing (data write)

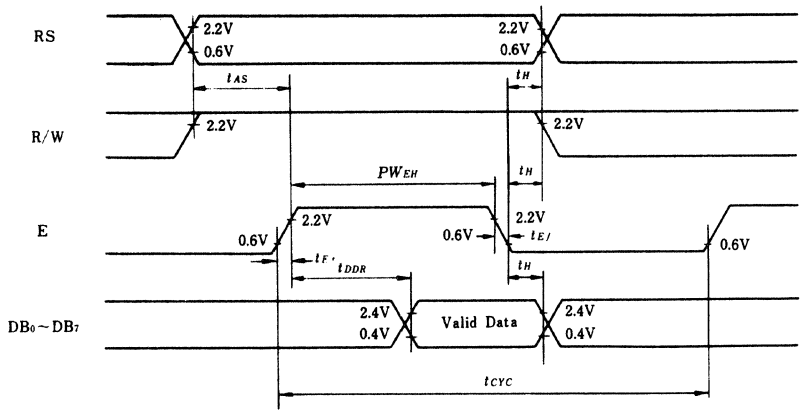


Fig. 6 Interface timing (data read)

LM070L

- 20 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	105W x 39H x 11T (max.) mm
Effective display area	84W x 13.0H mm
Character size (5 x 7 dots)	3.2W x 5.2H mm
Character pitch	3.9 mm
Dot size	0.6W x 0.7H mm
Weight	about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	6.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	2.0 mA typ. 3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$) Duty = 1/8	
Ta = 0°C	3.95 V typ.
Ta = 25°C	3.70 V typ.
Ta = 50°C	3.30 V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

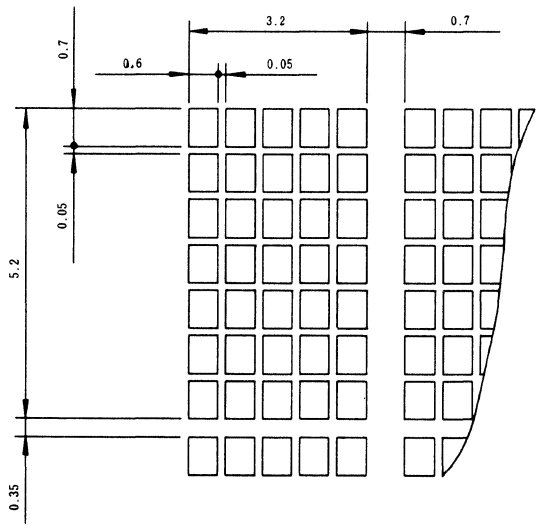


Fig. 1 Display pattern

Unit: mm

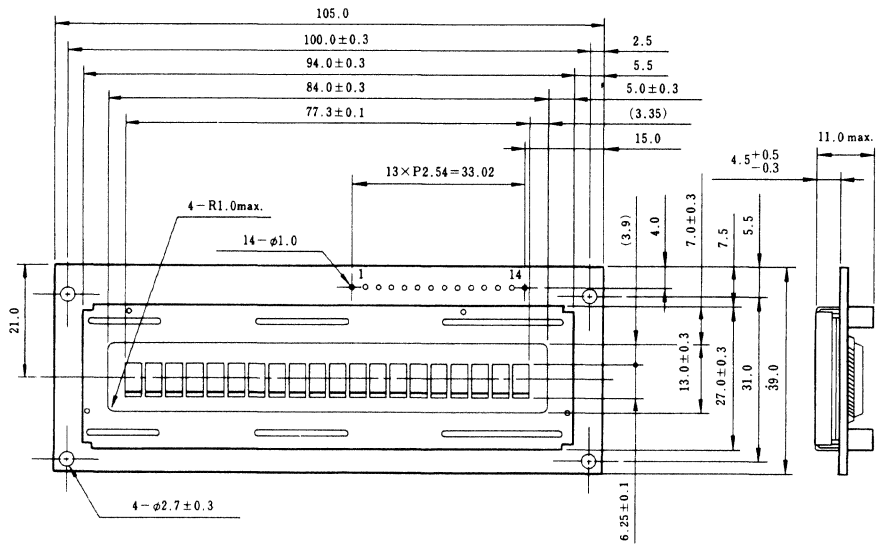
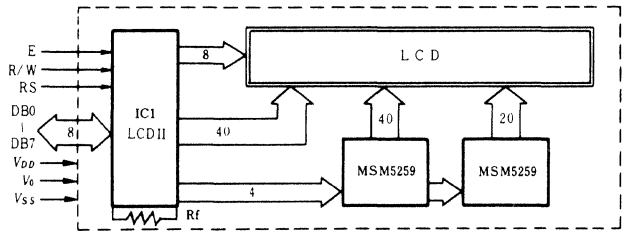
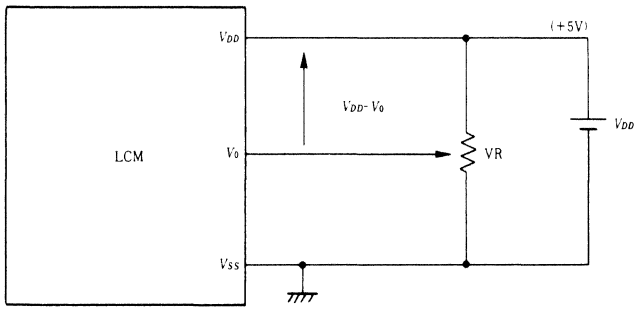


Fig. 2 External dimension



Rf=91kΩ

Fig. 3 Block diagram



$V_{DD} - V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

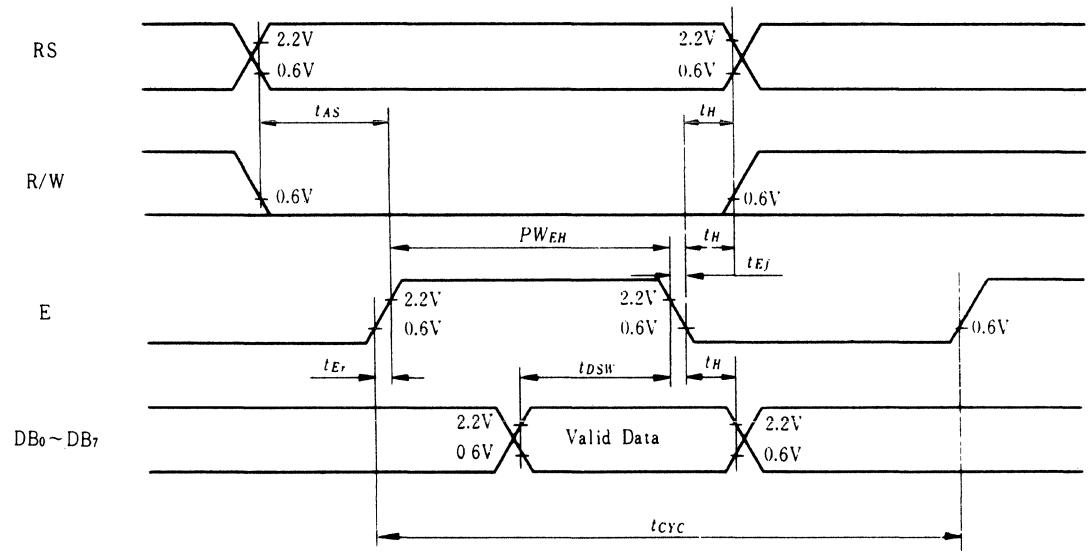


Fig. 5 Interface timing (data write)

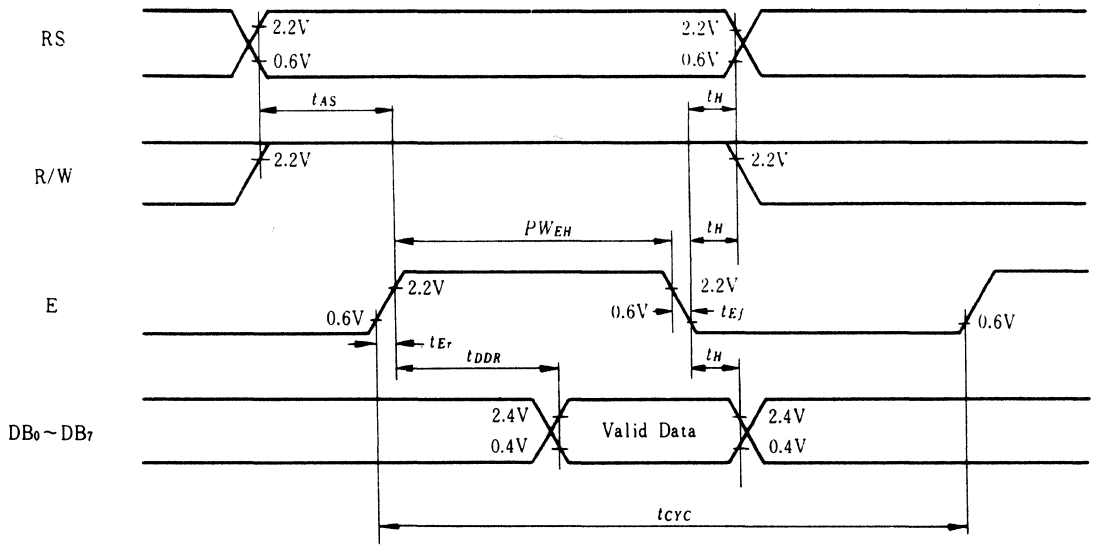


Fig. 6 Interface timing (data read)

LM038

- 20 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 182W x 35.5H(max.) x 13D (max.) mm
Effective display area . . . . . 154.0W x 15.3H mm
Character size (5 x 7 dots) . . . . . 6.7W x 9.4H mm
Character pitch . . . . . 7.4 mm
Dot size . . . . . 1.3W x 1.3H mm
Weight . . . . . about 65 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V
Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 2.5 mA typ.
5.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/8
Ta = 0°C . . . . . 4.1 V typ.
Ta = 25°C . . . . . 3.7 V typ.
Ta = 50°C . . . . . 3.1 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

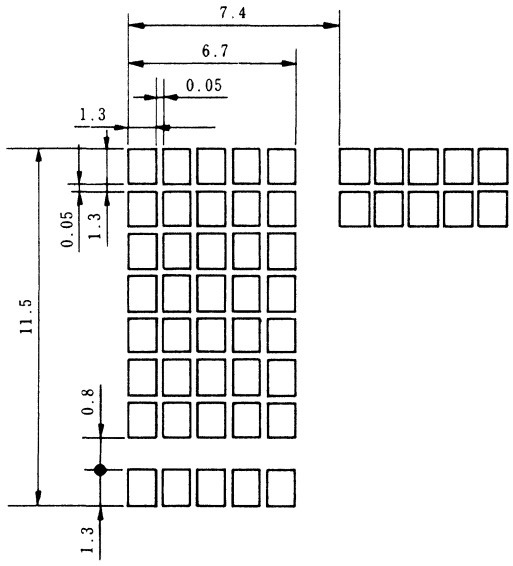


Fig. 1 Display pattern

Unit: mm

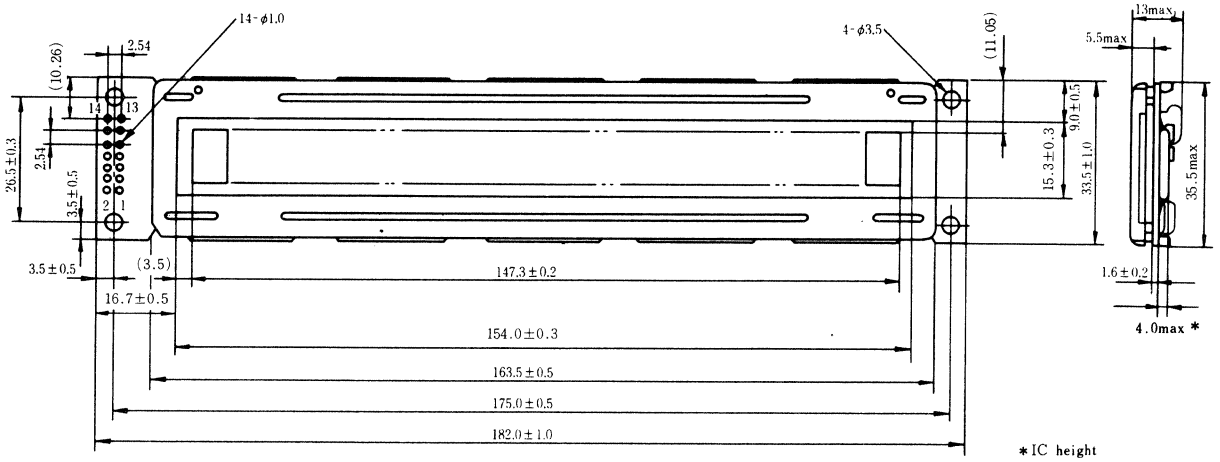
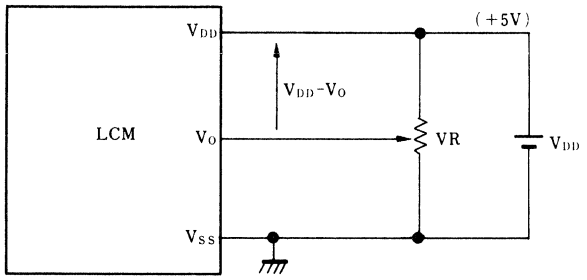


Fig. 2 External dimension



V_{DD}-V_O: LCD driving voltage
VR: 10 kΩ ~ 20 kΩ

Fig. 3 Power supply

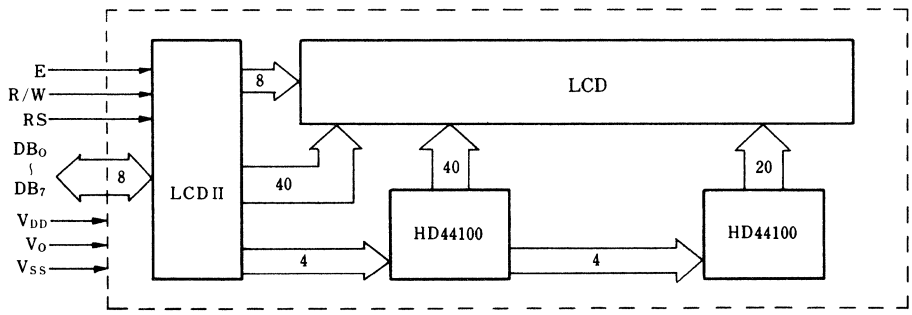


Fig. 4 Block diagram

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

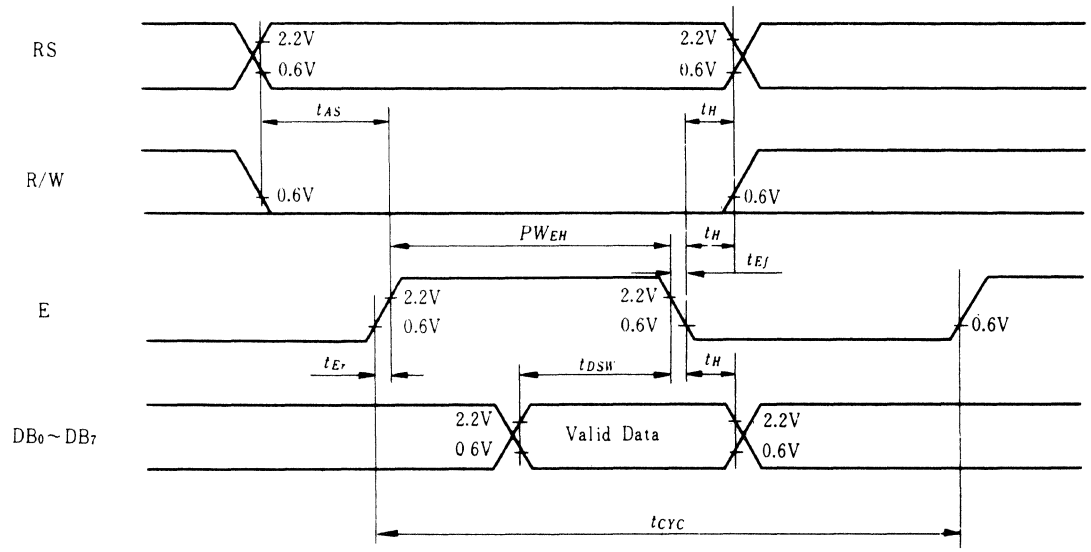


Fig. 5 Interface timing (data write)

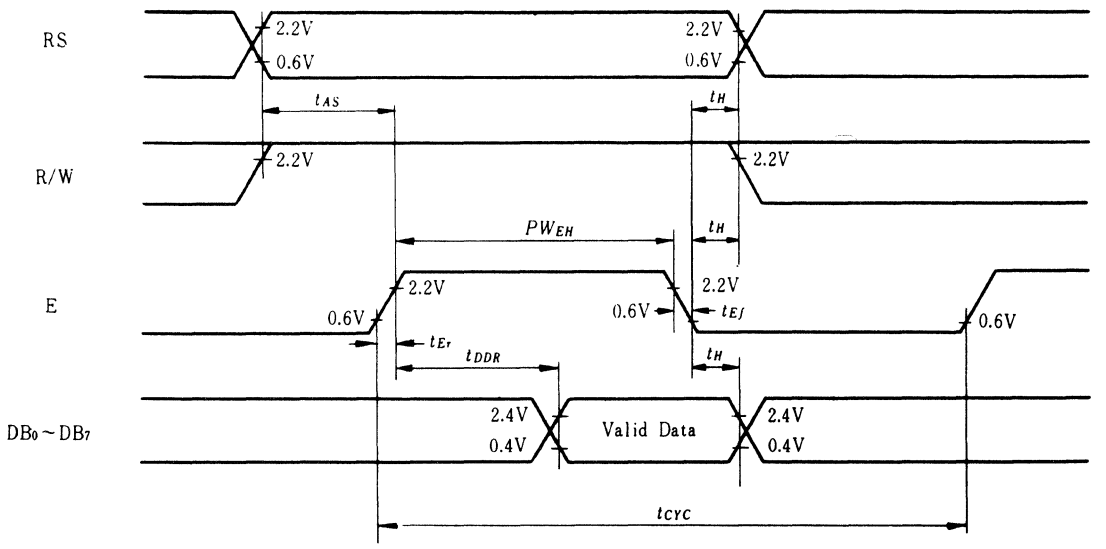


Fig. 6 Interface timing (data read)

LM027

- 24 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 126W x 36H x 12T (max.) mm
Effective display area . . . . . 100W x 13.8H mm
Character size (5 x 10 dots) . . . . . 3.15W x 7.9H mm
Character pitch . . . . . 3.75 mm
Dot size . . . . . 0.55W x 0.7H mm
Weight . . . . . about 40 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$=0.2 mA) . . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

	Duty = 1/8	Duty = 1/11
Ta = 0°C	4.0	4.2 V typ.
Ta = 25°C	3.7	3.8 V typ.
Ta = 50°C	3.3	3.3 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

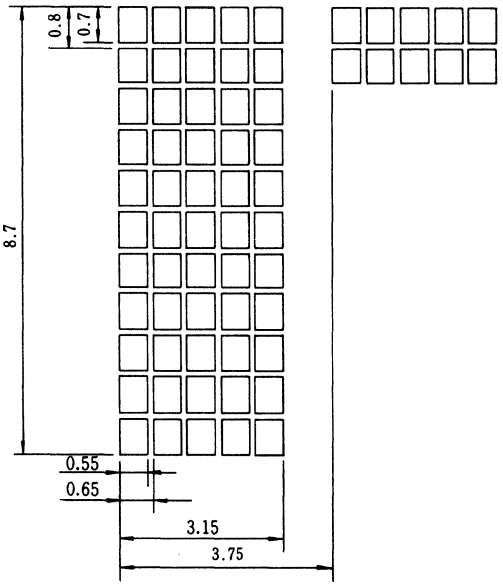


Fig. 1 Display pattern

Unit: mm

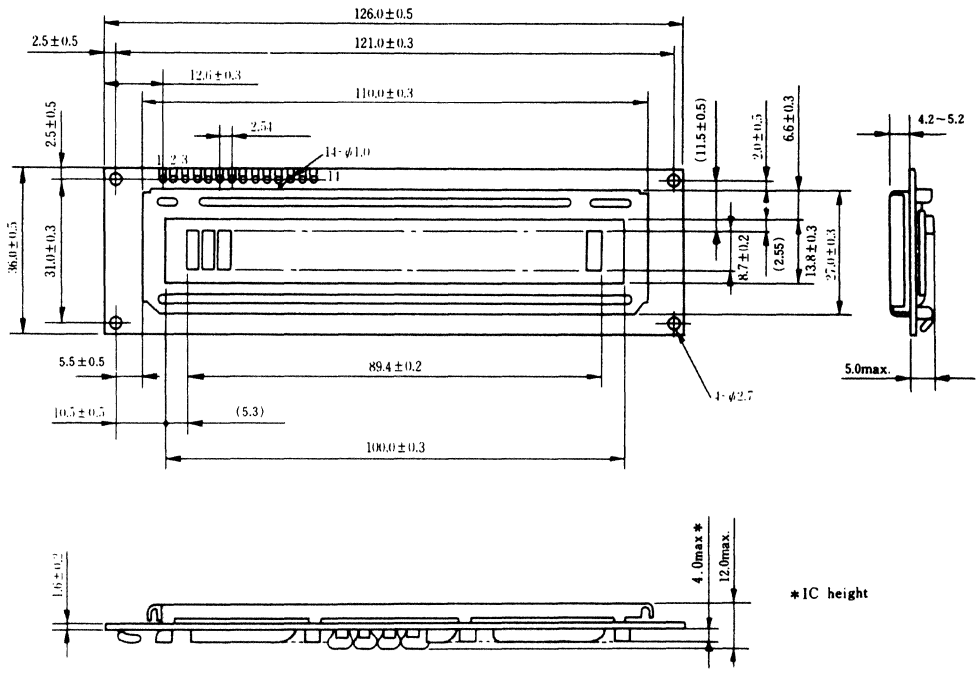


Fig. 2 External dimensions

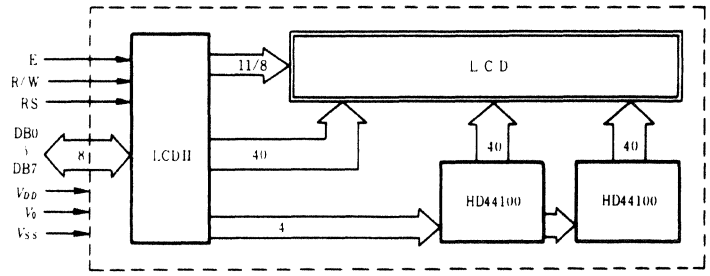


Fig. 3 Block diagram

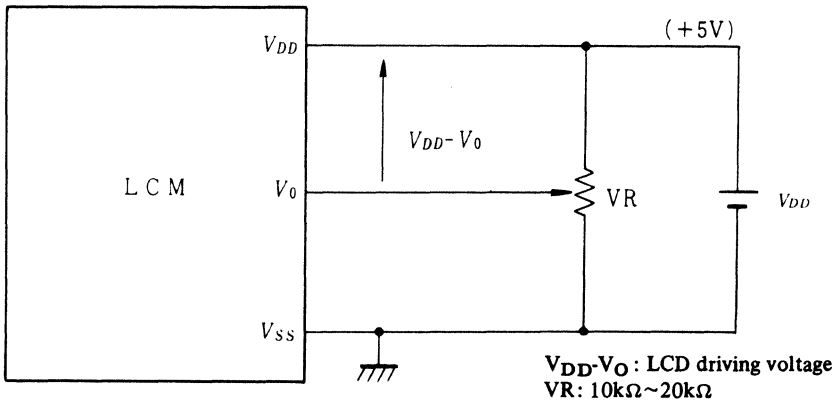


Fig. 4 Power supply

SECTION 5

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

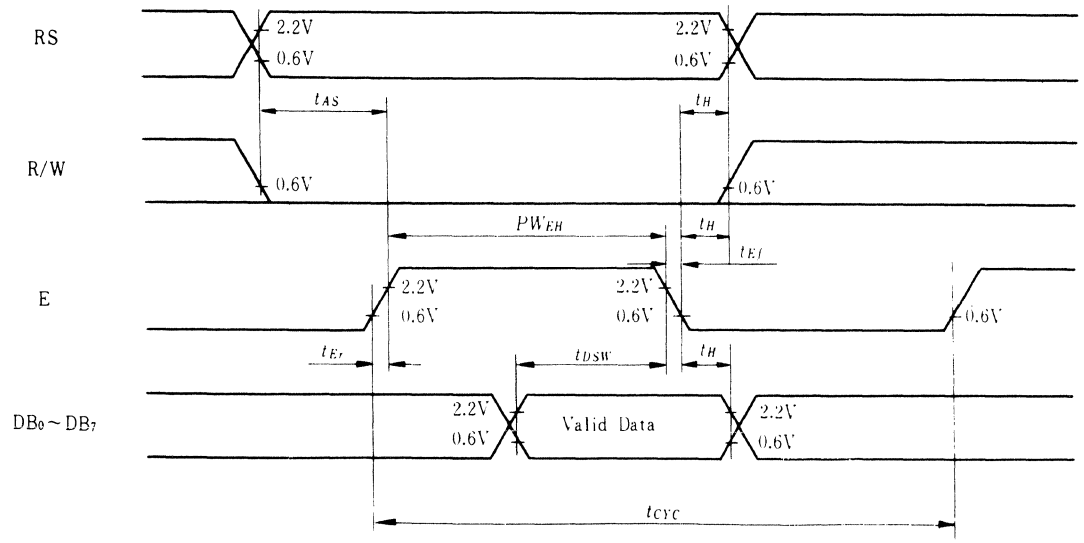


Fig. 5 Interface timing (data write)

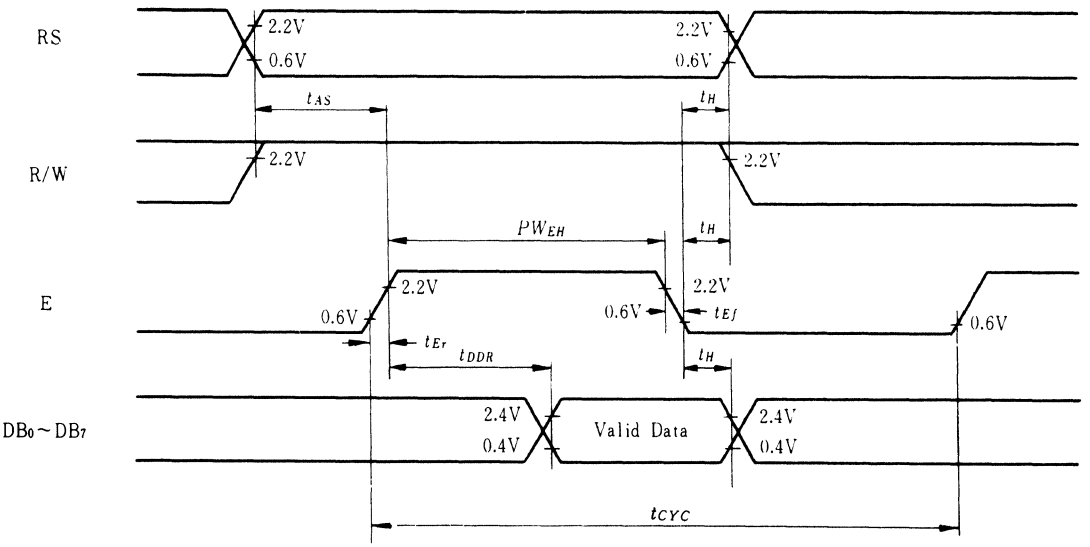


Fig. 6 Interface timing (data read)

H2571

- 32 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . 174.5W x 33.0H (max.) x 13.4T (max.) mm
Effective display are . . . . . 132.5W x 14.0H mm
Character size (5 x 10 dots) . . . . . 3.15W x 7.9H mm
Character pitch . . . . . 3.85 mm
Dot size . . . . . 0.55W x 0.7H mm
Weight . . . . . about 60 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$) . . .	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2mA) . . 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

	Duty = 1/8	Duty = 1/11
Ta = 0°C	3.95	4.15V typ.
Ta = 25°C	3.7	3.8V typ.
Ta = 50°C	3.3	3.3V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

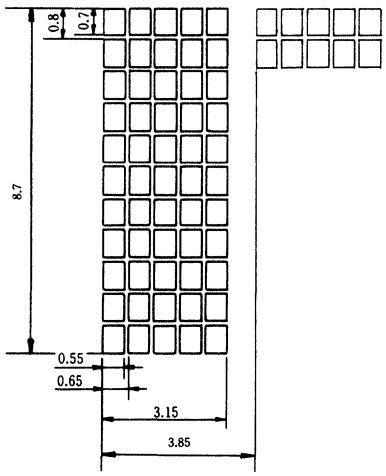


Fig. 1 Display pattern

Unit: mm

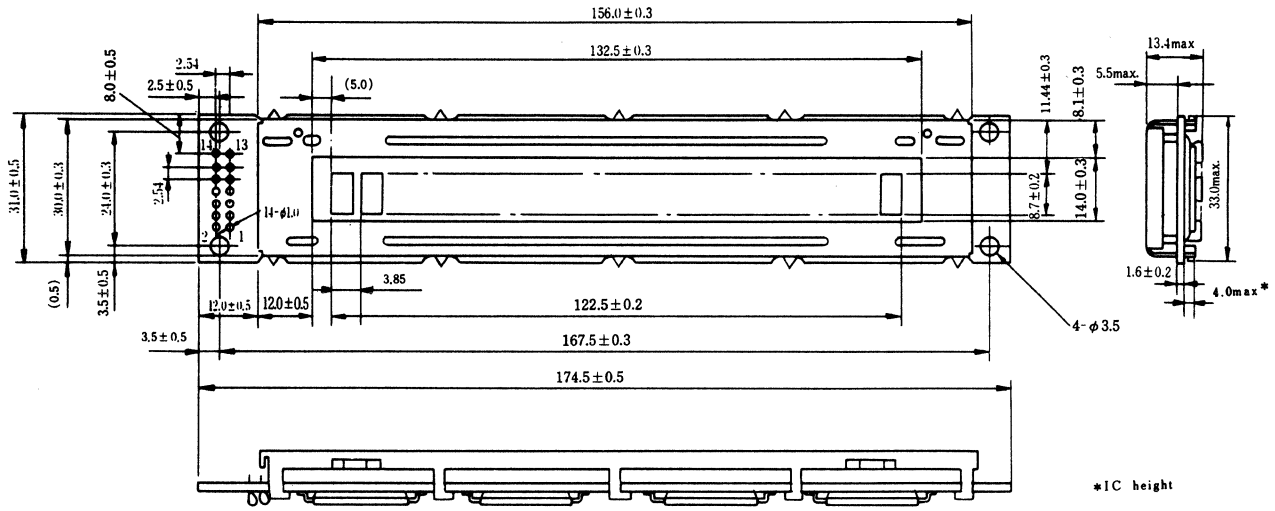


Fig. 2 External dimensions

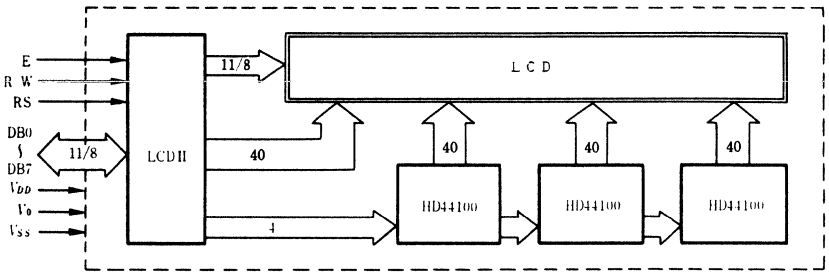


Fig. 3 Block diagram

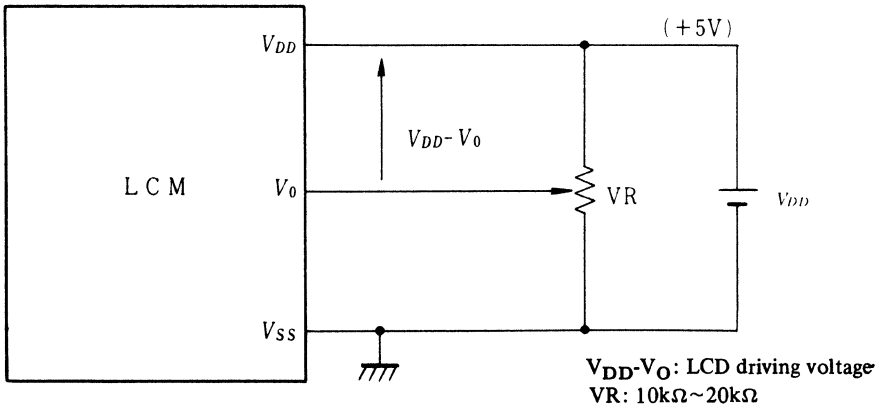


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

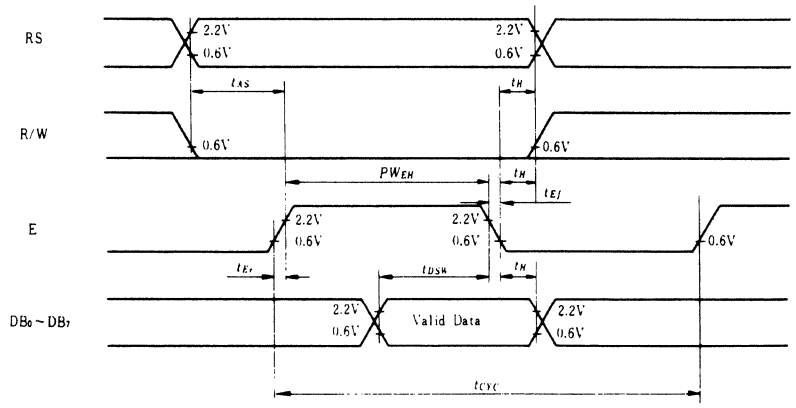


Fig. 5 Interface timing (data write)

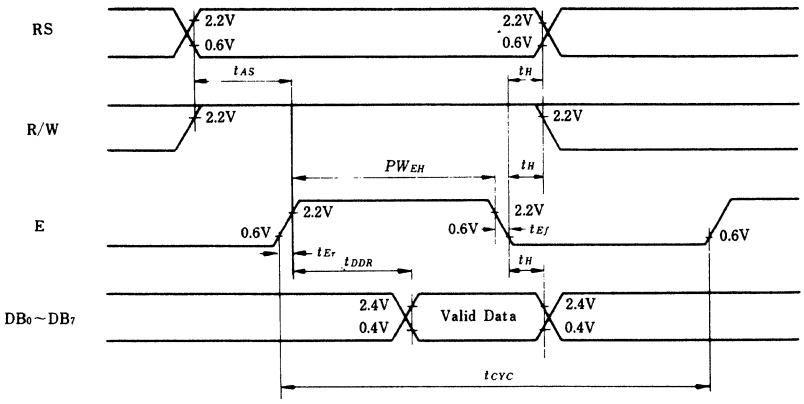


Fig. 6 Interface timing (data read)

H2572

- 40 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size .... 182W x 35.5H (max.) x 13T (max.) mm
Effective display area ..... 154.0W x 15.3H mm
Character size (5 x 10 dots) ..... 3.15W x 7.9H mm
Character pitch ..... 3.75 mm
Dot size ..... 0.55W x 0.7H mm
Weight ..... about 65 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) ..... 2.2 V min.
Input "low" voltage (Vi_L) ..... 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA). . 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL}= 1.6 mA) . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
2.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

	Duty = 1/8	Duty = 1/11
Ta = 0°C	3.95	4.15 V typ.
Ta = 25°C	3.7	3.8 V typ.
Ta = 50°C	3.3	3.3 V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

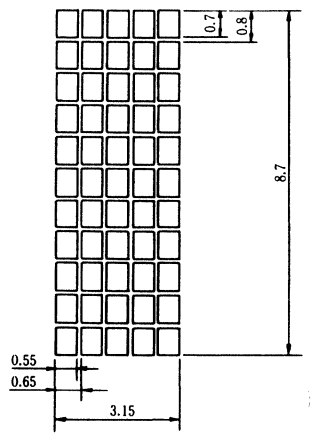


Fig. 1 Display pattern

HITACHI

Unit: mm

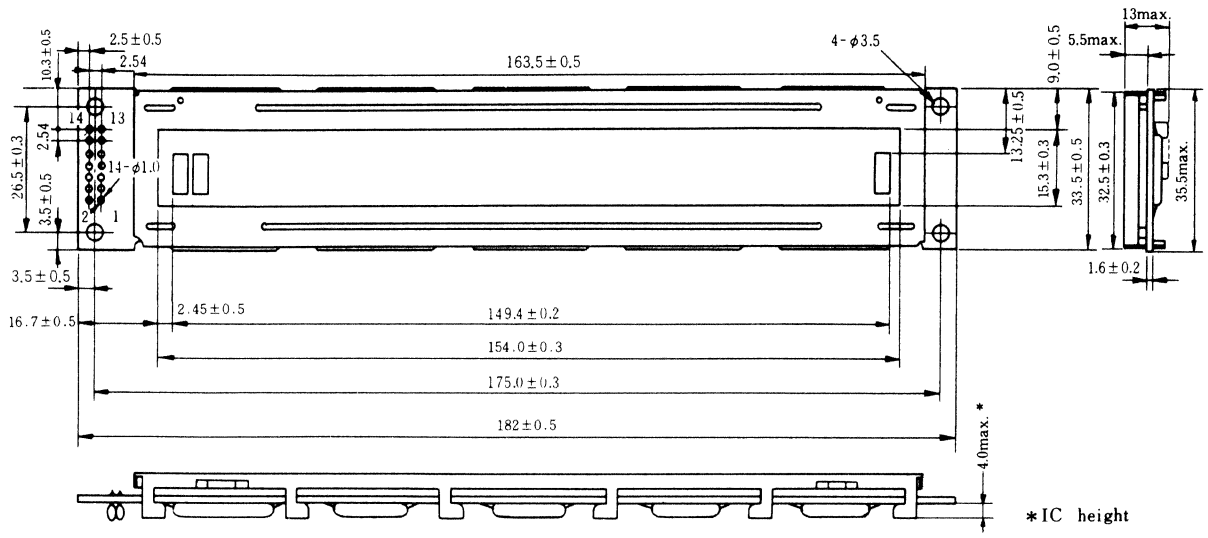


Fig. 2 External dimensions

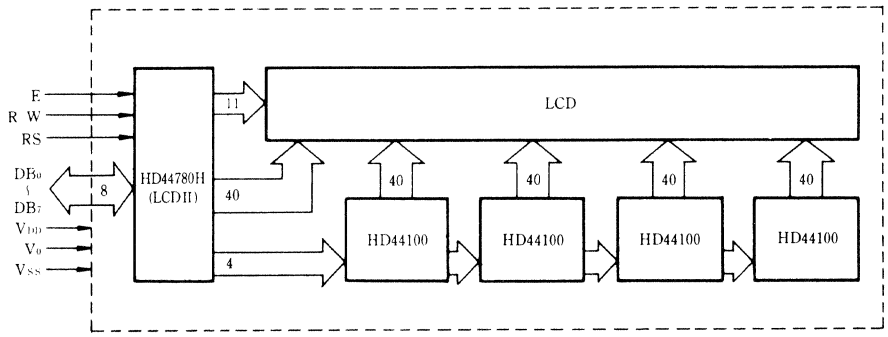


Fig. 3 Block diagram

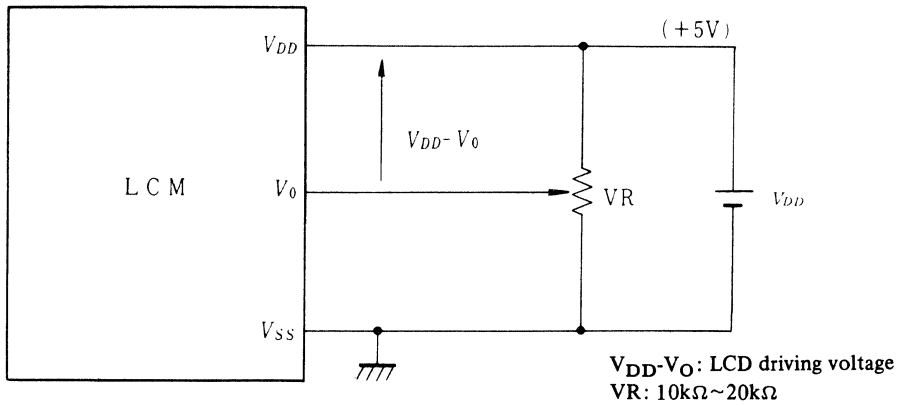


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

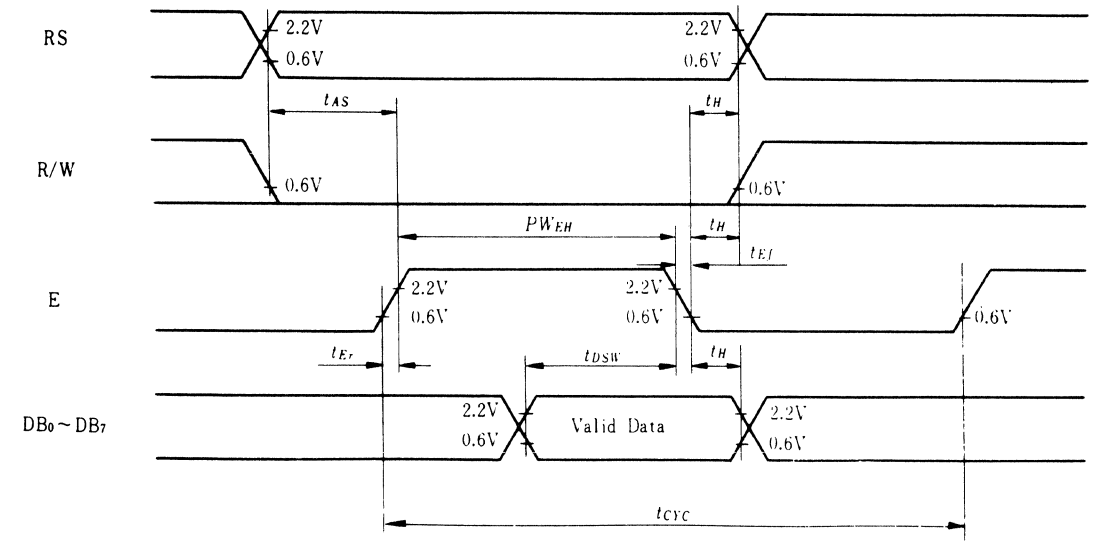


Fig. 5 Interface timing (data write)

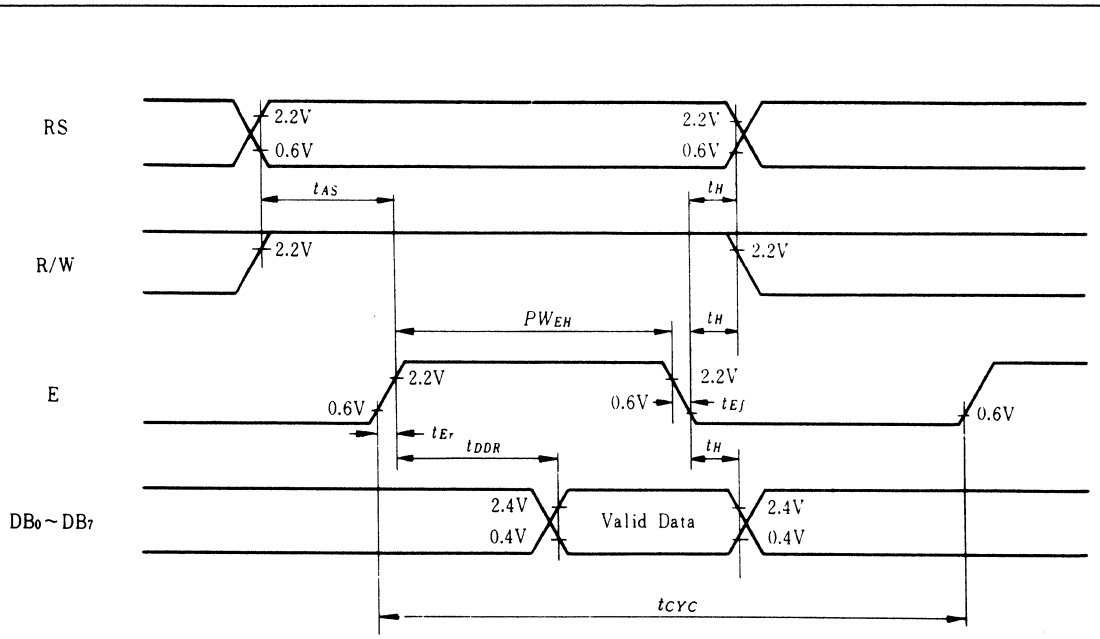


Fig. 6 Interface timing (data read)

LM058

- 40 character x 1 line
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size ..... 290W x 60H x 13.0T (max.) mm
Effective display area ..... 245W x 19.0H mm
Character size (5 x 7 dots) ..... 4.82W x 8.18H mm
Character pitch ..... 5.82 mm
Dot size ..... 0.9W x 1.1H mm
Weight ..... about 150 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) ..... 2.2 V min.
Input "low" voltage (Vi_L) ..... 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA) ... 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) .... 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) .. 0.5 mA typ.
2.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/8
Ta = 0°C ..... 4.3 V typ.
Ta = 25°C ..... 3.9 V typ.
Ta = 50°C ..... 3.3 V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

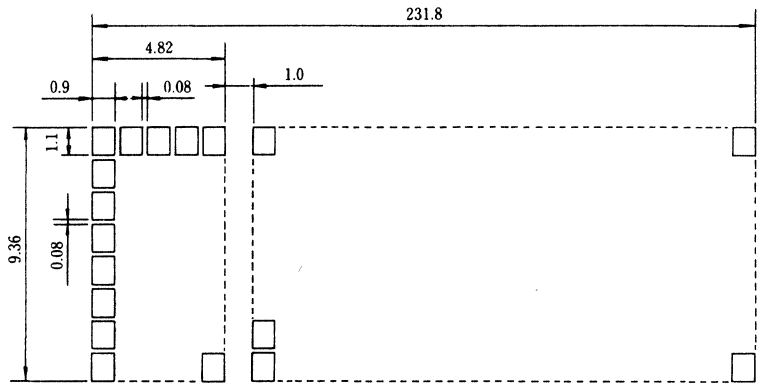


Fig. 1 Display pattern

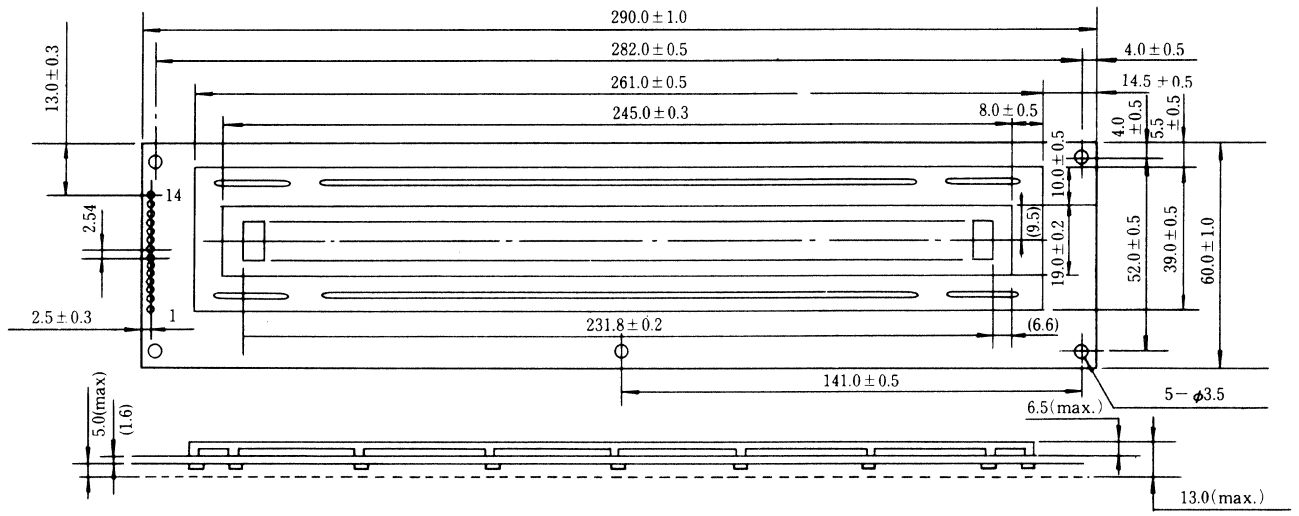


Fig. 2 External dimension

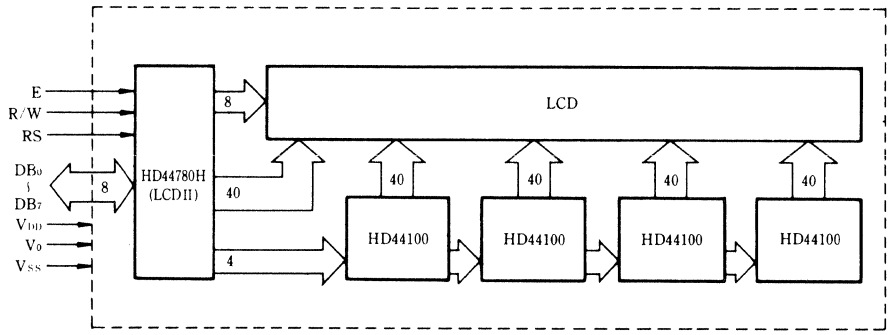


Fig. 3 Block diagram

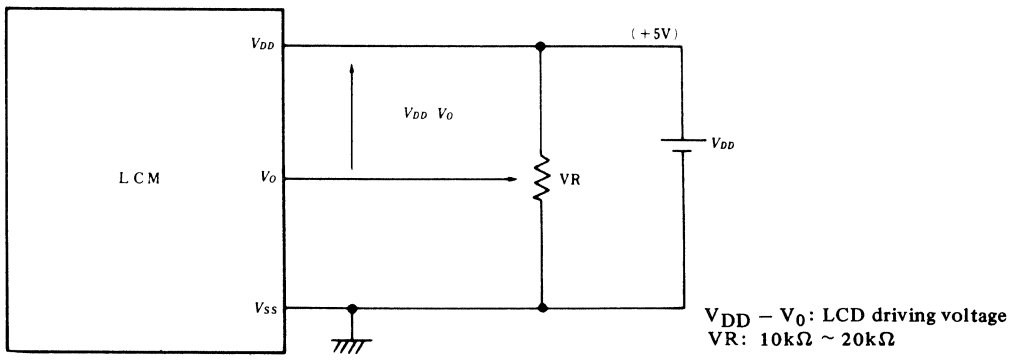


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

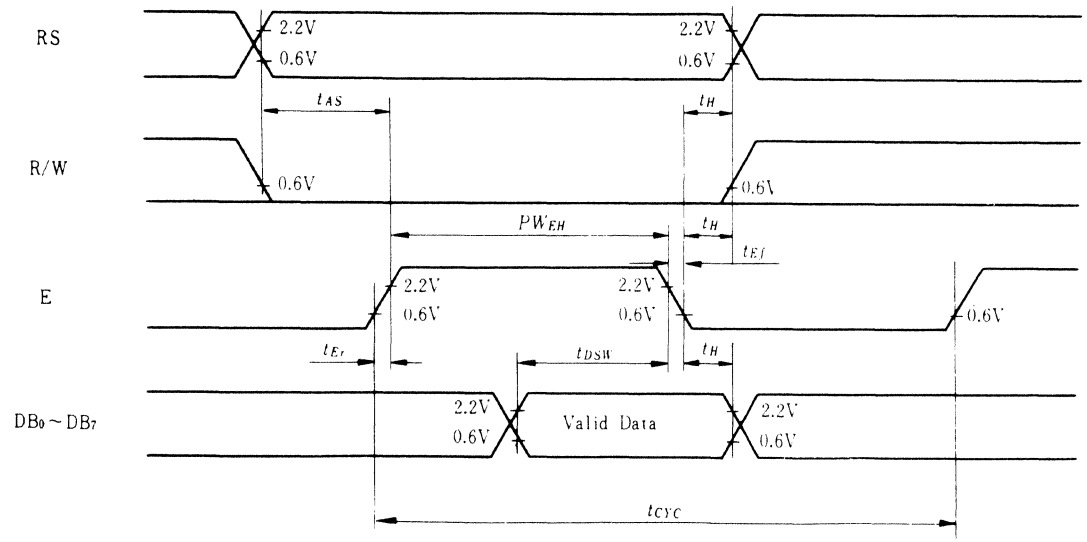


Fig. 5 Interface timing (data write)

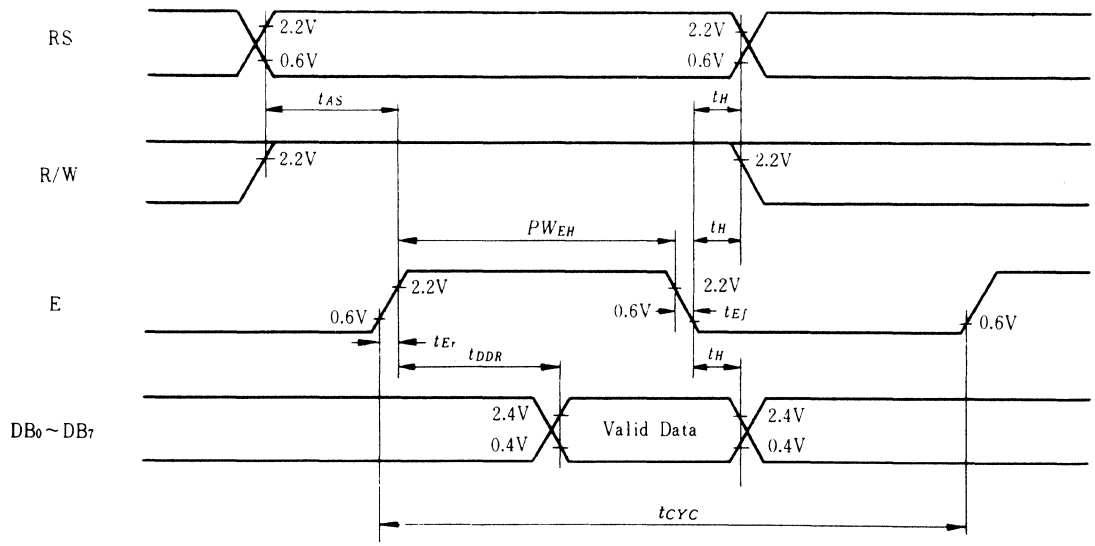


Fig. 6 Interface timing (data read)

LM052L

- 16 character x 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	80W x 36H x 11T (max.) mm
Effective display area	64.5W x 13.8H mm
Character size (5 x 7 dots)	2.95W x 3.8H mm
Character pitch	3.65 mm
Dot size	0.55W x 0.5H mm
Weight	about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	–20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$) Duty = 1/16	
Ta = 0°C	4.2 V typ.
Ta = 25°C	4.0 V typ.
Ta = 50°C	3.6 V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	V_{SS}	–	0V — Power supply
2	V_{DD}	–	+5V — Power supply
3	V_O	–	– — Power supply
4	RS	H/L	L: Instruction code input H: Data input
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)
6	E	H, H→L	Enable signal
7	DB0	H/L	Data bus line Note (1), (2)
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

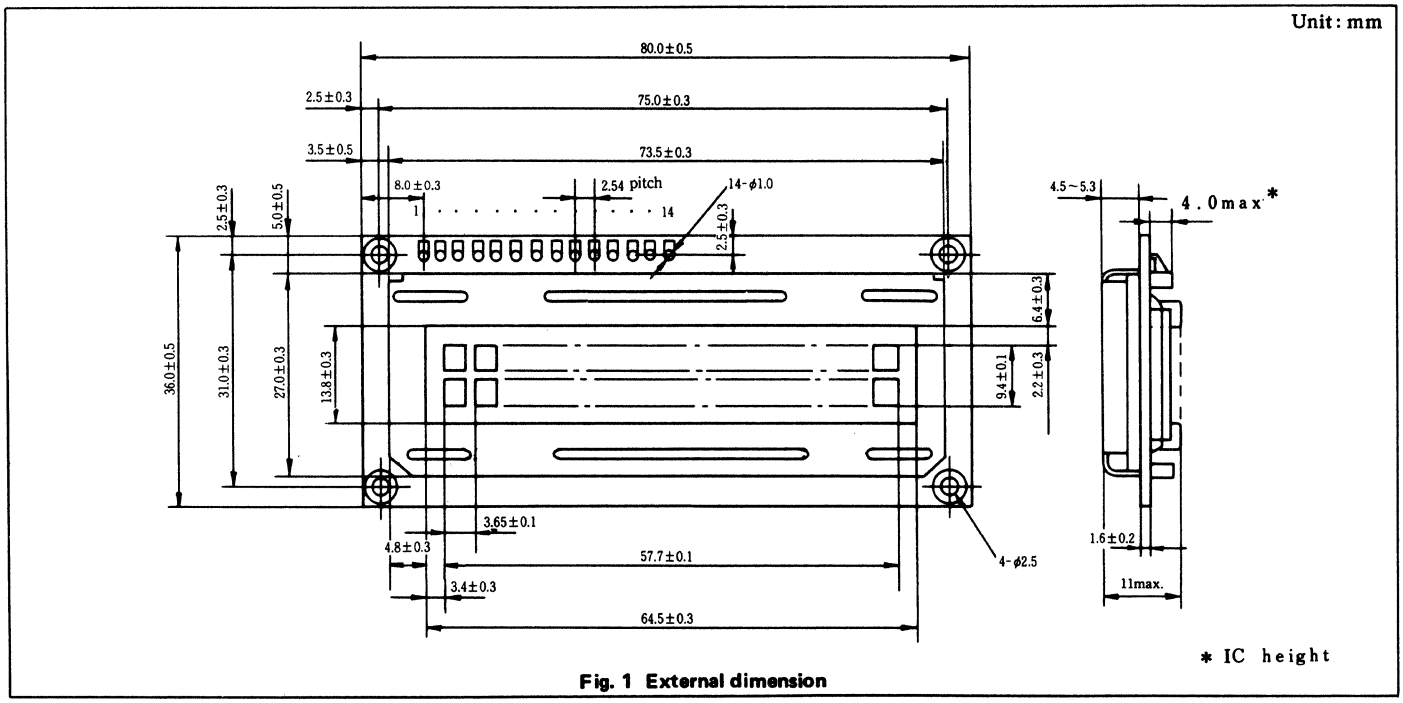


Fig. 1 External dimension

HITACHI

Unit: mm

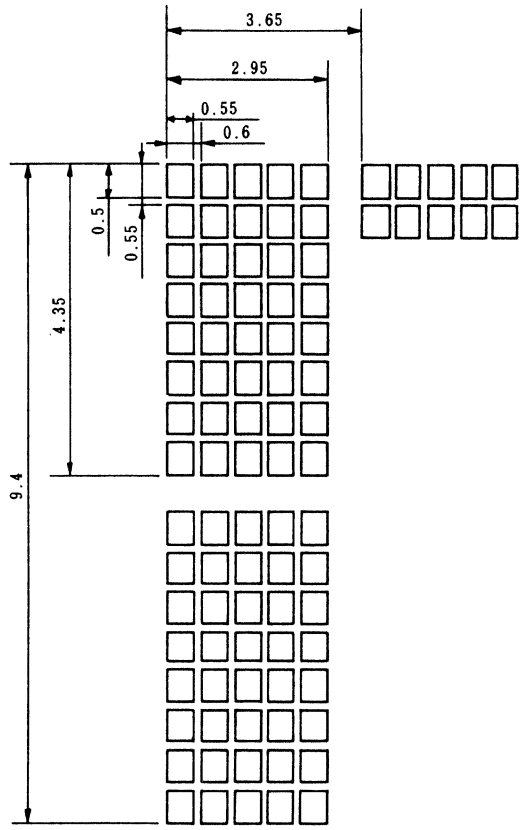


Fig. 2 Display pattern

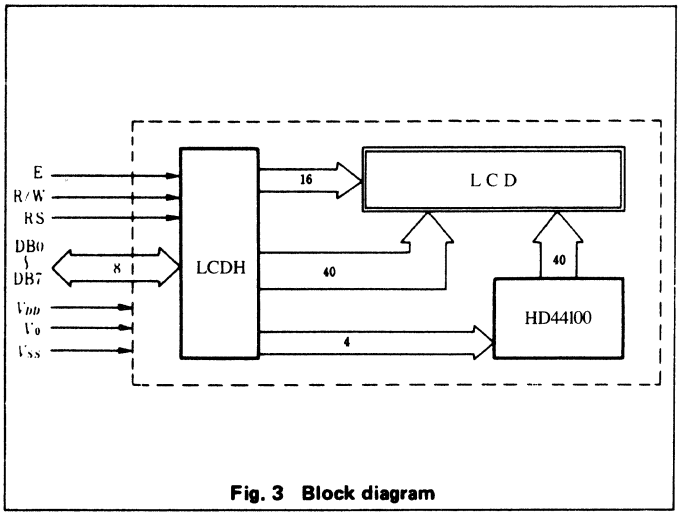


Fig. 3 Block diagram

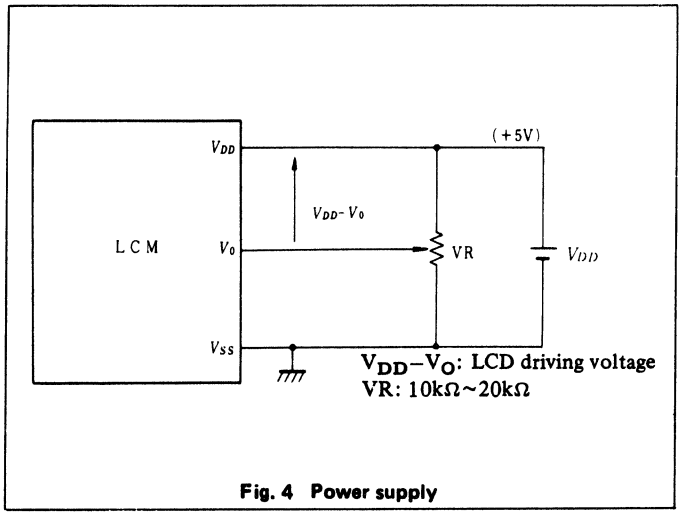


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

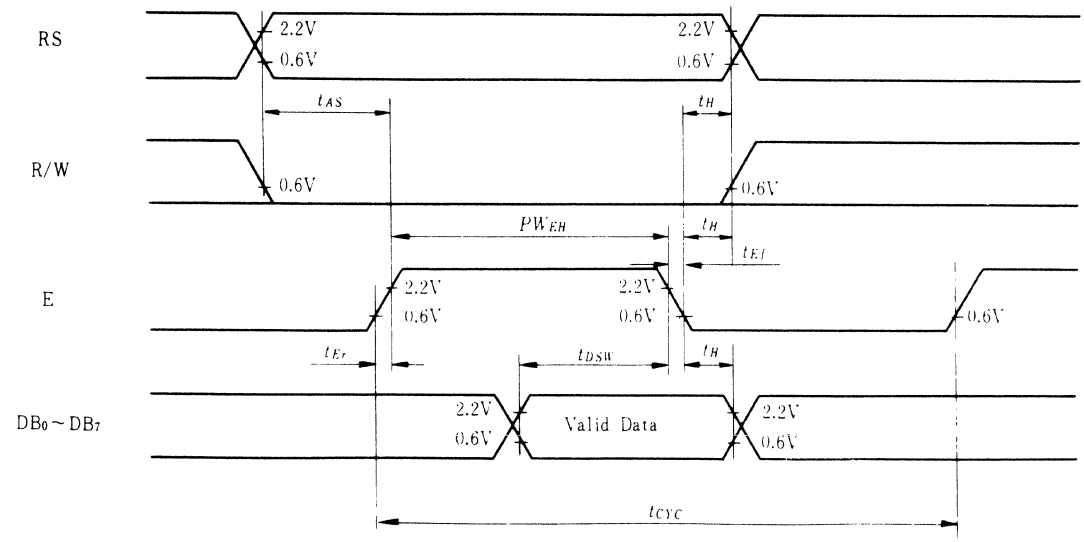


Fig. 5 Interface timing (data write)

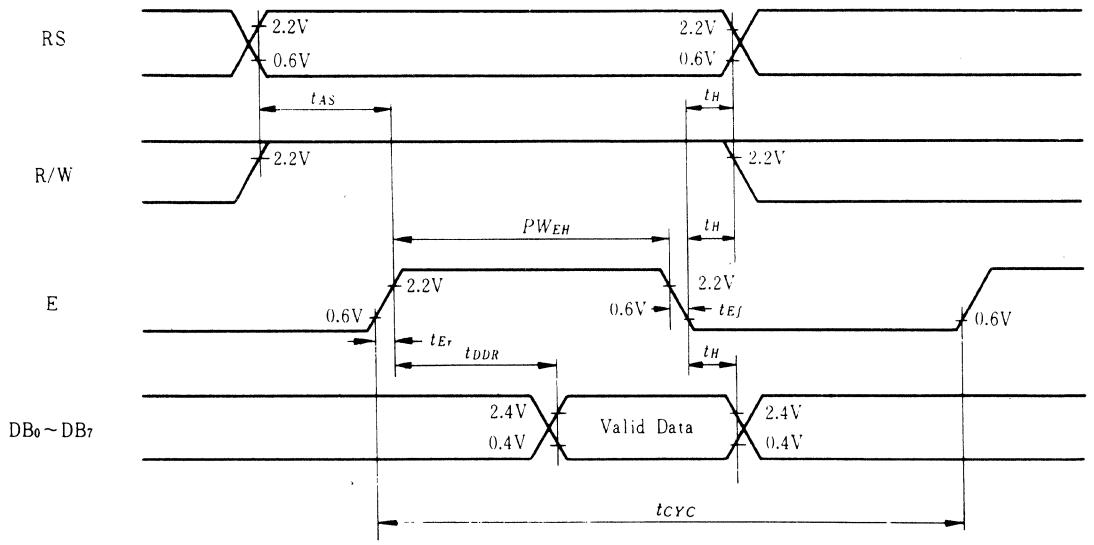


Fig. 6 Interface timing (data read)

LM075L

- 16 character x 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply
- Large numeral font set (see page 176).

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 80W x 36H x 11T (max.) mm
Effective display area . . . . . 64.5W x 13.8H mm
Character size (5 x 7 dots) . . . . . 2.95W x 3.8H mm
Character pitch . . . . . 3.65 mm
Dot size . . . . . 0.55W x 0.5H mm
Weight . . . . . about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta = 0°C . . . . . 4.2 V typ.
Ta = 25°C . . . . . 4.0 V typ.
Ta = 50°C . . . . . 3.6 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

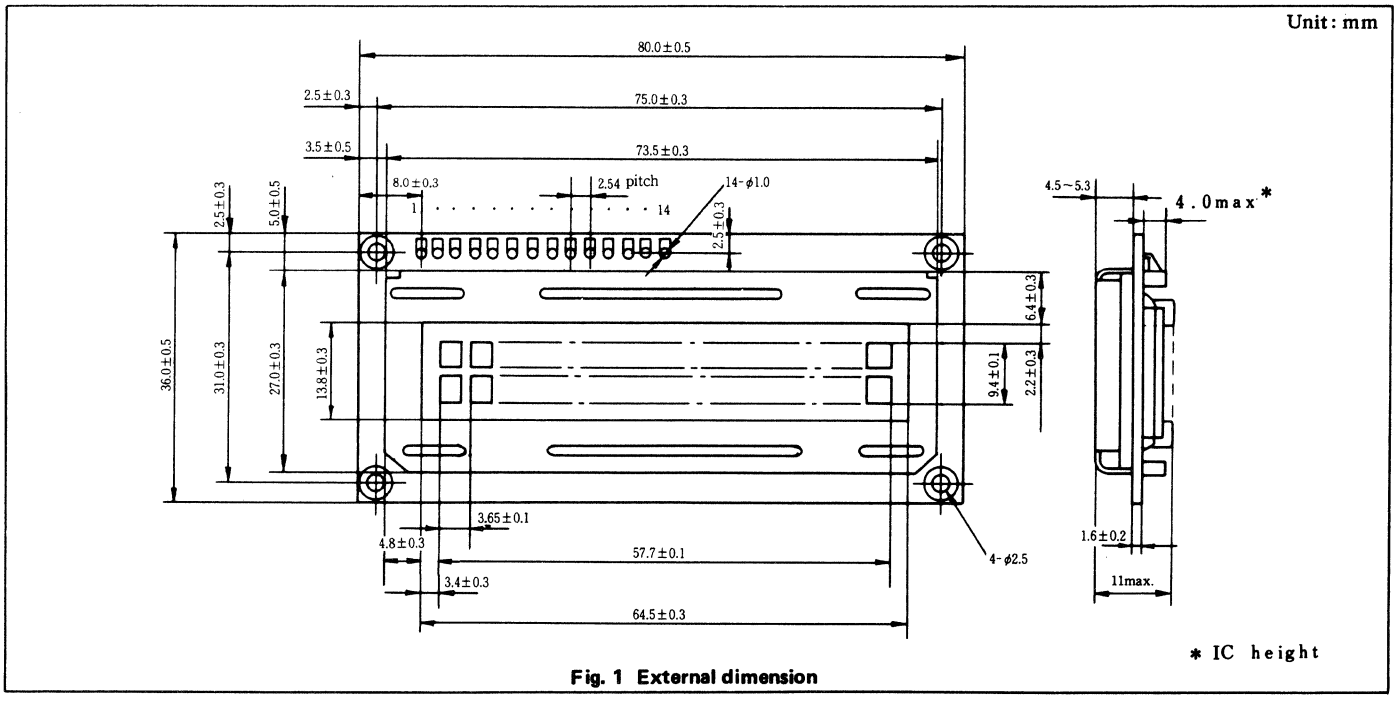


Fig. 1 External dimension

Unit: mm

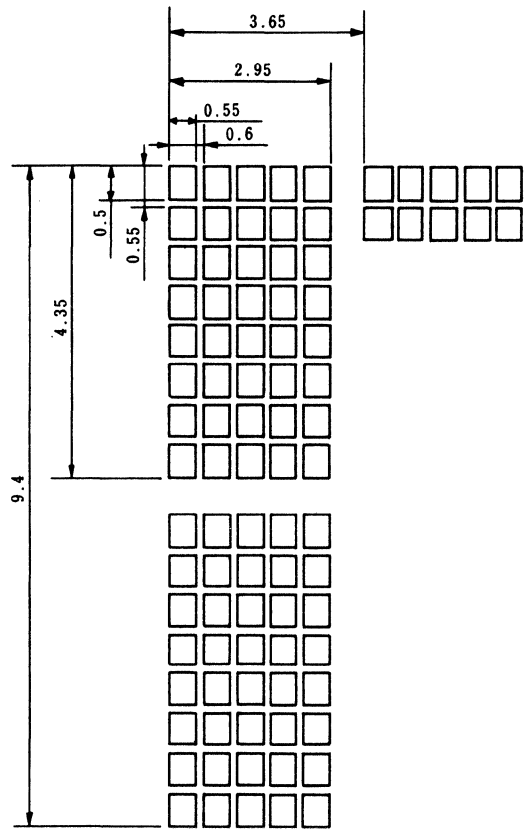


Fig. 2 Display pattern

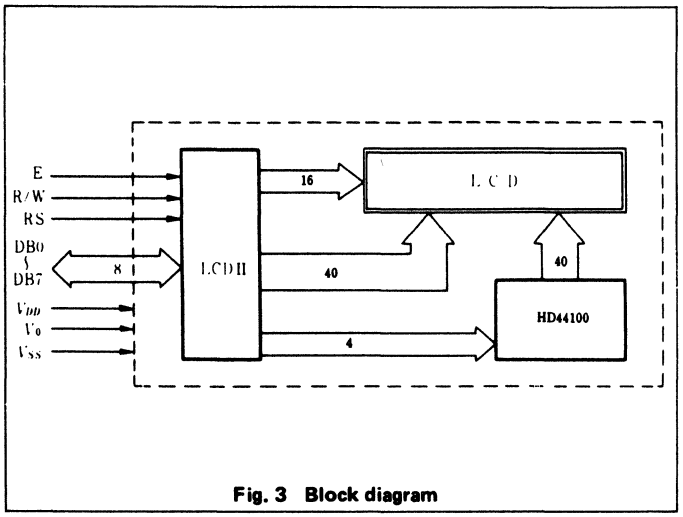


Fig. 3 Block diagram

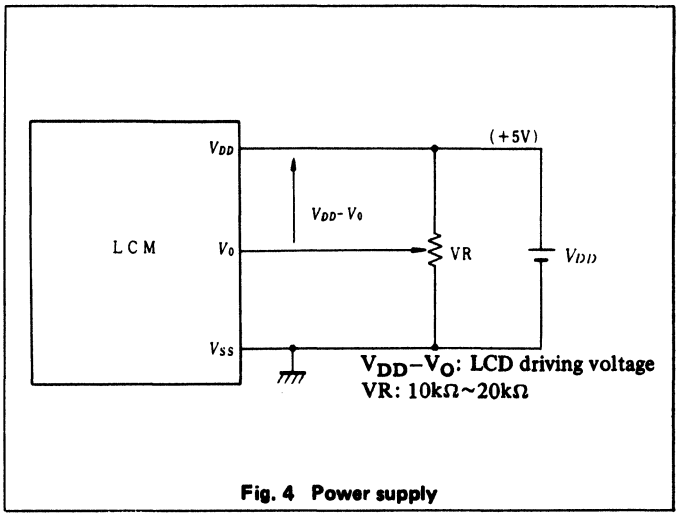


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

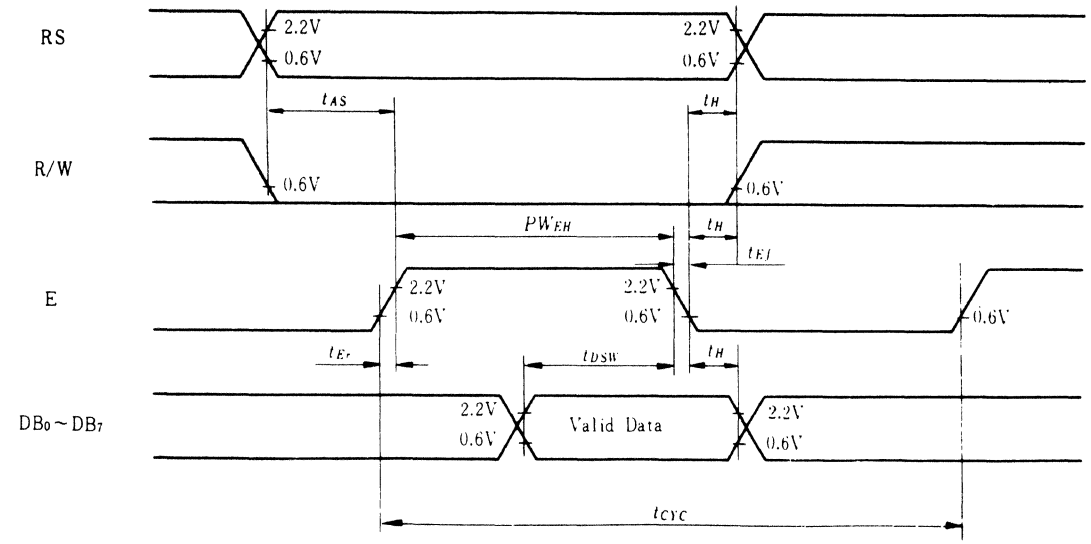


Fig. 5 Interface timing (data write)

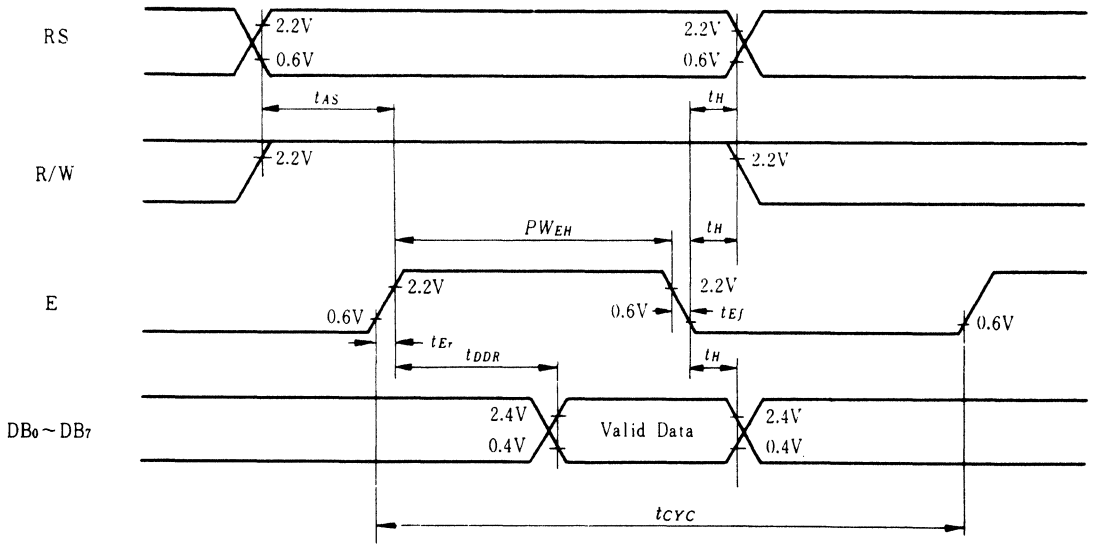


Fig. 6 Interface timing (data read)

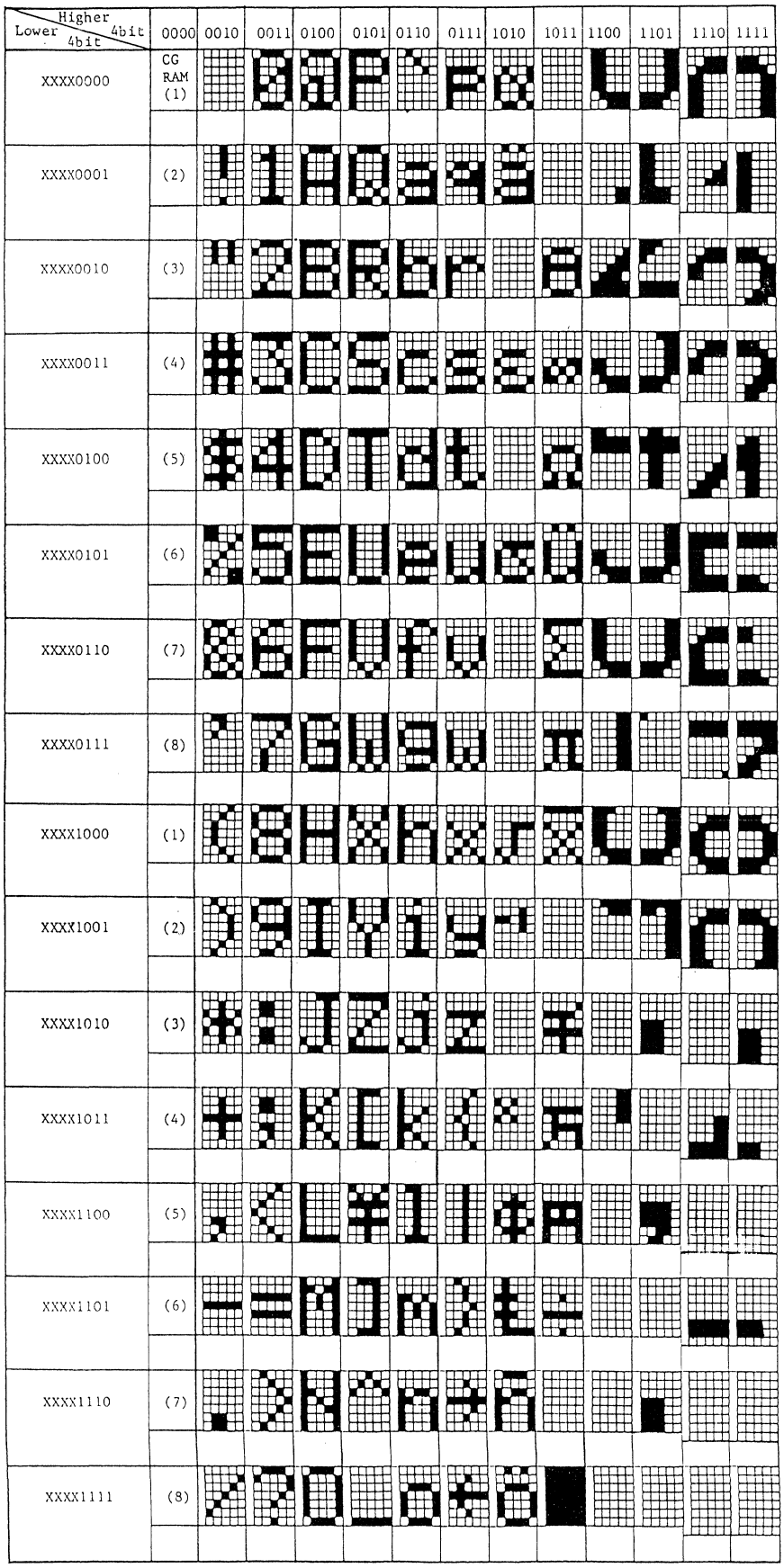


Fig. 7 Character dot pattern

LM016L

- 16 character x 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	84W x 44H x 12T (max.) mm
Effective display area	61W x 15.8H mm
Character size (5 x 7 dots)	2.96W x 4.86H mm
Character pitch	3.55 mm
Dot size	0.56W x 0.66H mm
Weight	about 35 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temeprature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)	Duty = 1/16
Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

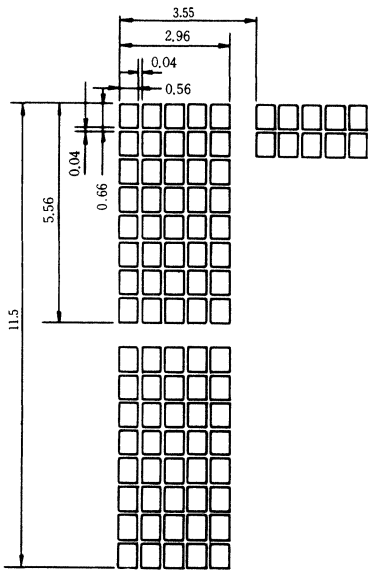


Fig. 1 Display pattern

SECTION 5

Unit: mm

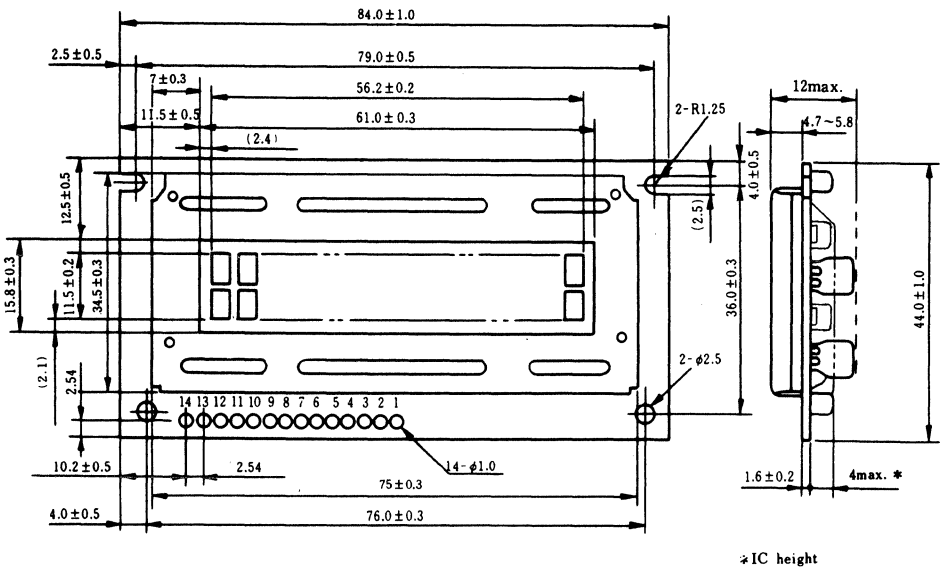


Fig. 2 External dimensions

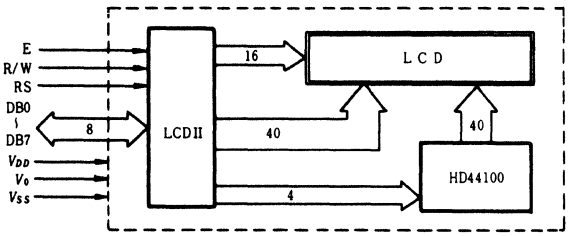


Fig. 3 Block diagram

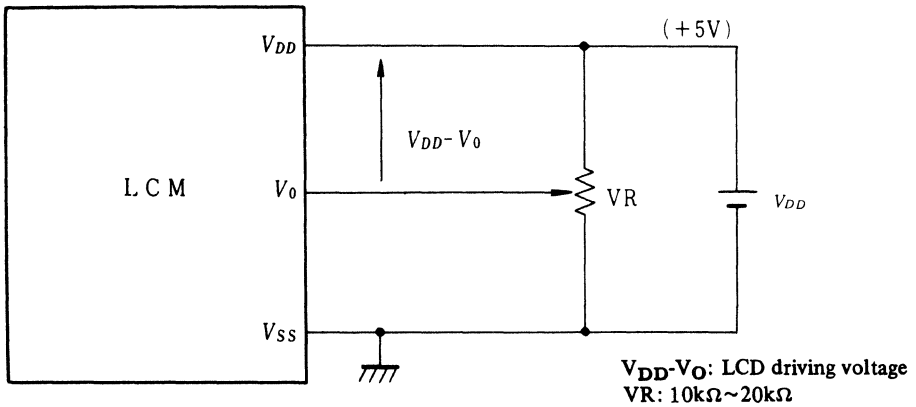


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

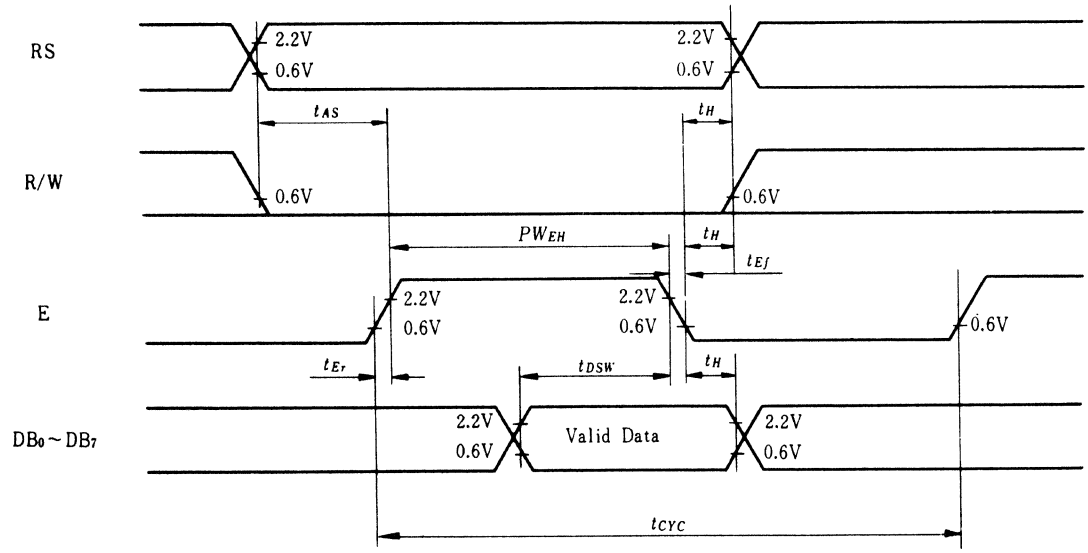


Fig. 5 Interface timing (data write)

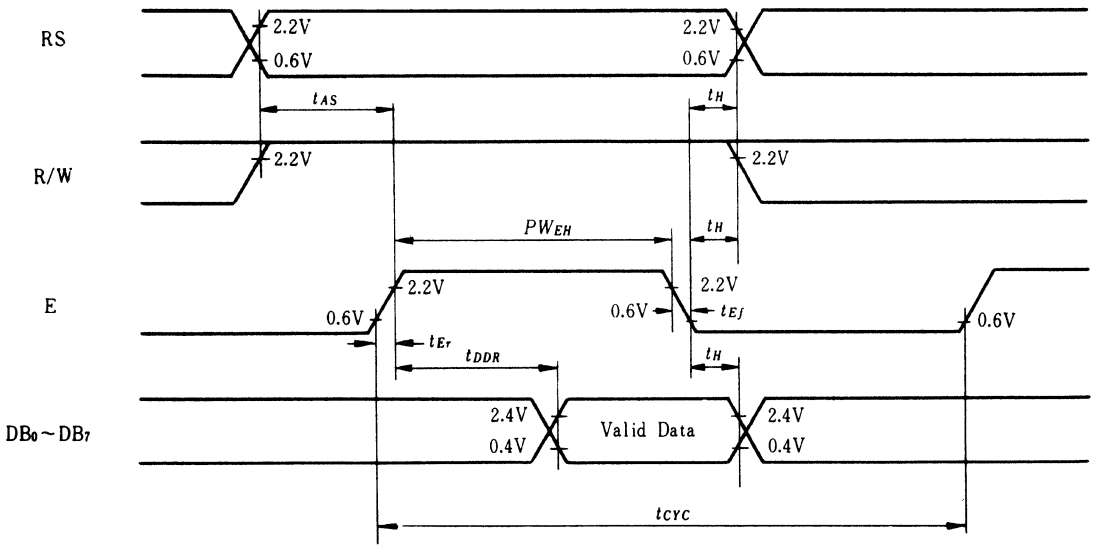


Fig. 6 Interface timing (data read)

LM068L

- 16 character x 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .83.0W x 43.0H x 11T (max.) mm
Effective display area . . . . . .61W x 17.6H mm
Character size (5 x 7 dots) . . . . . 2.96W x 4.86H mm
Character pitch . . . . . 3.55 mm
Dot size . . . . . 0.56W x 0.66H mm
Weight . . . . . about 35 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	16.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temeprature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V
Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . . 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta = 0°C . . . . . 4.6 V typ.
Ta = 25°C . . . . . 4.4 V typ.
Ta = 50°C . . . . . 4.2 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

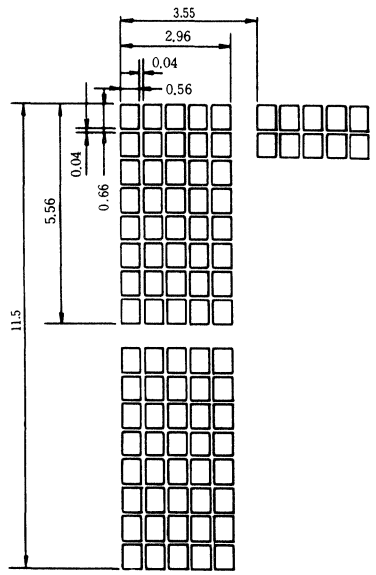


Fig. 1 Display pattern

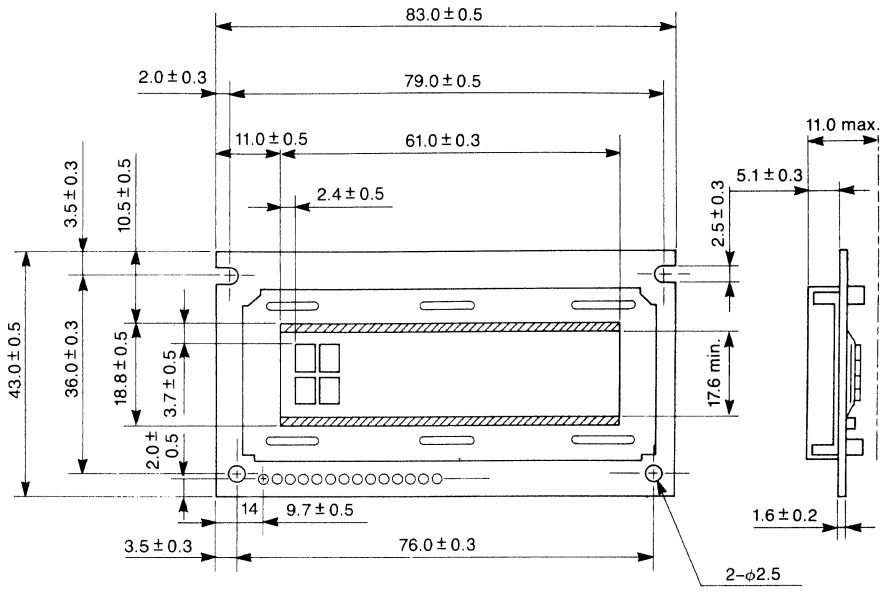


Fig. 2 External dimension

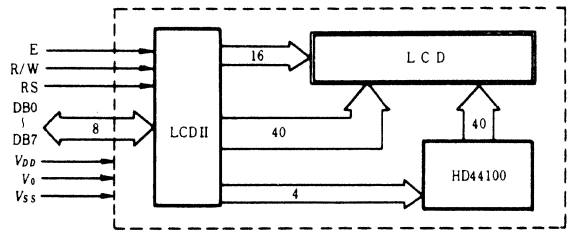


Fig. 3 Block diagram

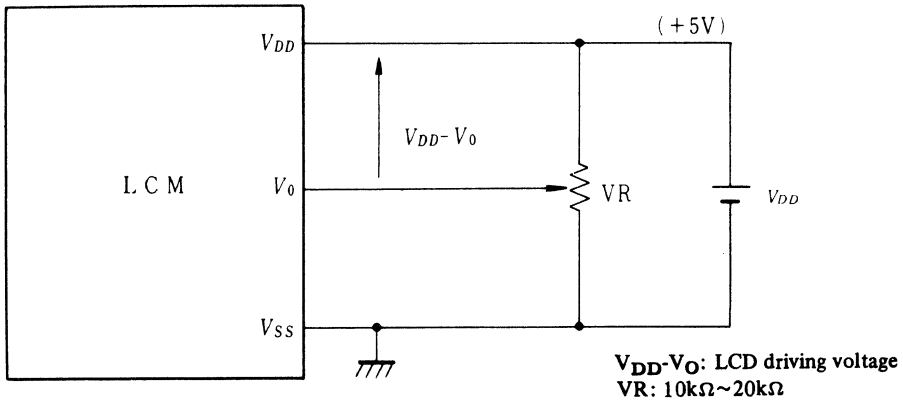


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

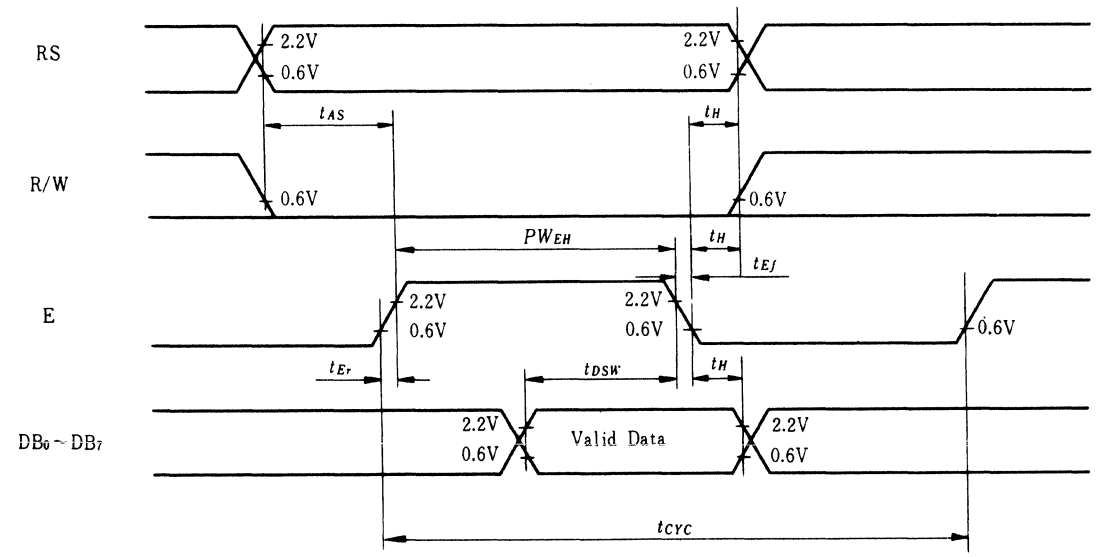


Fig. 5 Interface timing (data write)

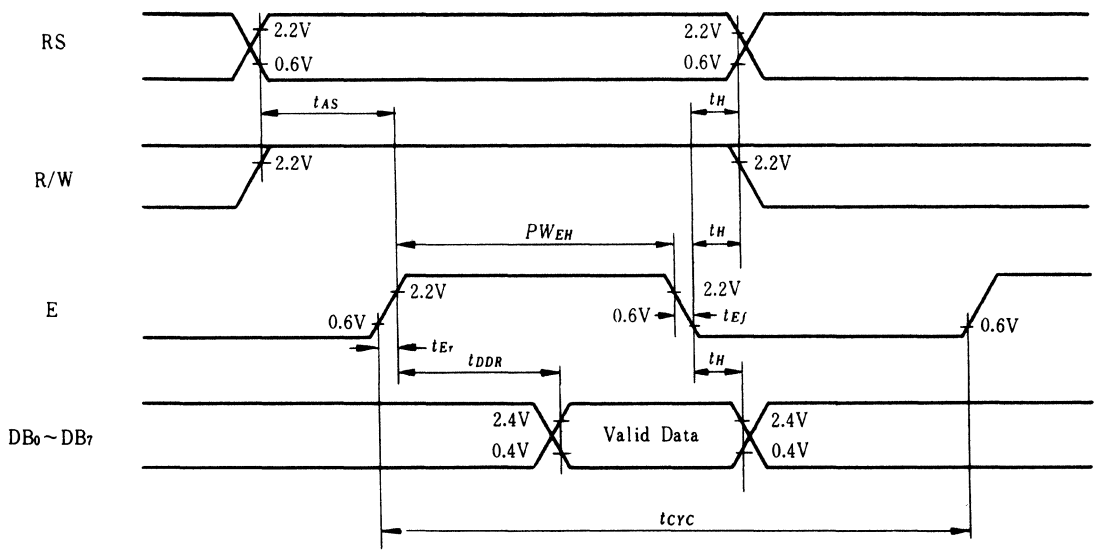


Fig. 6 Interface timing (data read)

LM074L

- 16 character × 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply
- Large numeral font set (see page 186).

MECHANICAL DATA (Nominal dimensions)

Module size	84W x 44H x 12T (max.) mm
Effective display area	61W x 15.8H mm
Character size (5 x 7 dots)	2.96W x 4.86H mm
Character pitch	3.55 mm
Dot size	0.56W x 0.66H mm
Weight	about 35 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temeprature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 3.0 mA max.

Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)

Duty = 1/16

Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

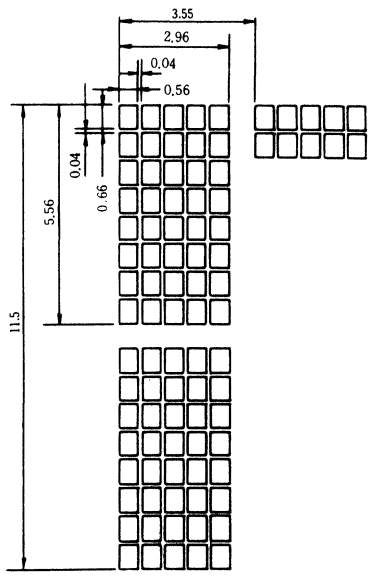


Fig. 1 Display pattern

Unit: mm

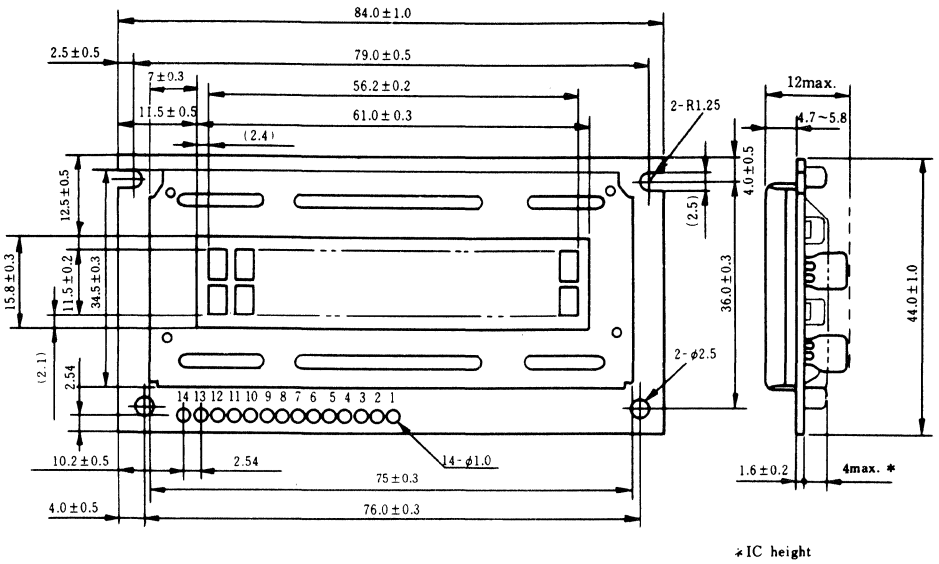


Fig. 2 External dimensions

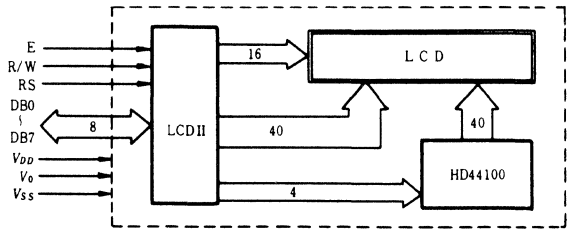


Fig. 3 Block diagram

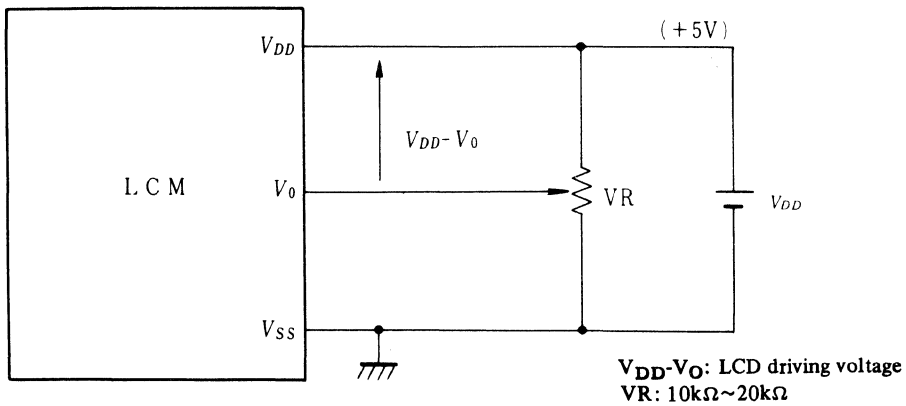


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

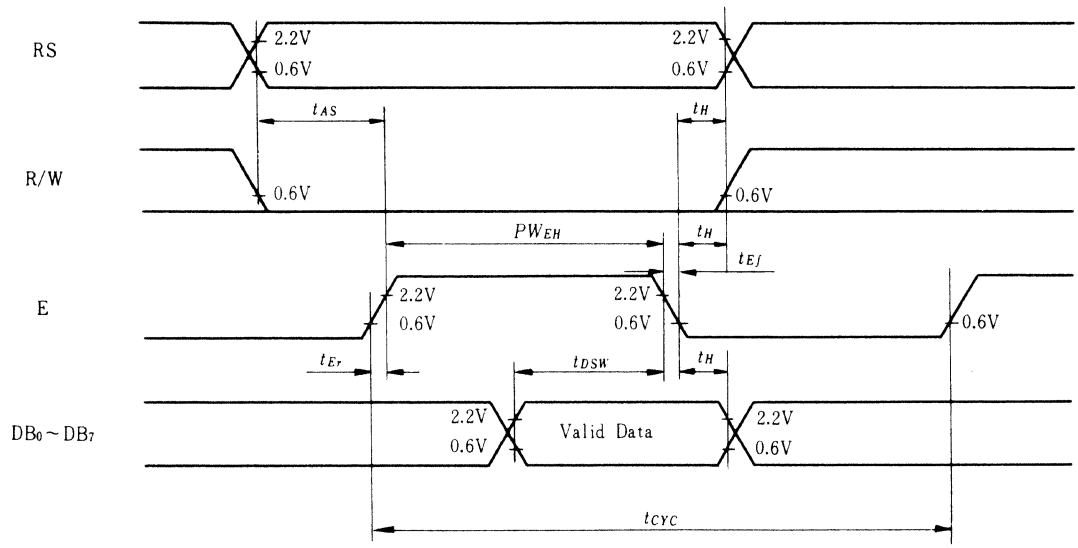


Fig. 5 Interface timing (data write)

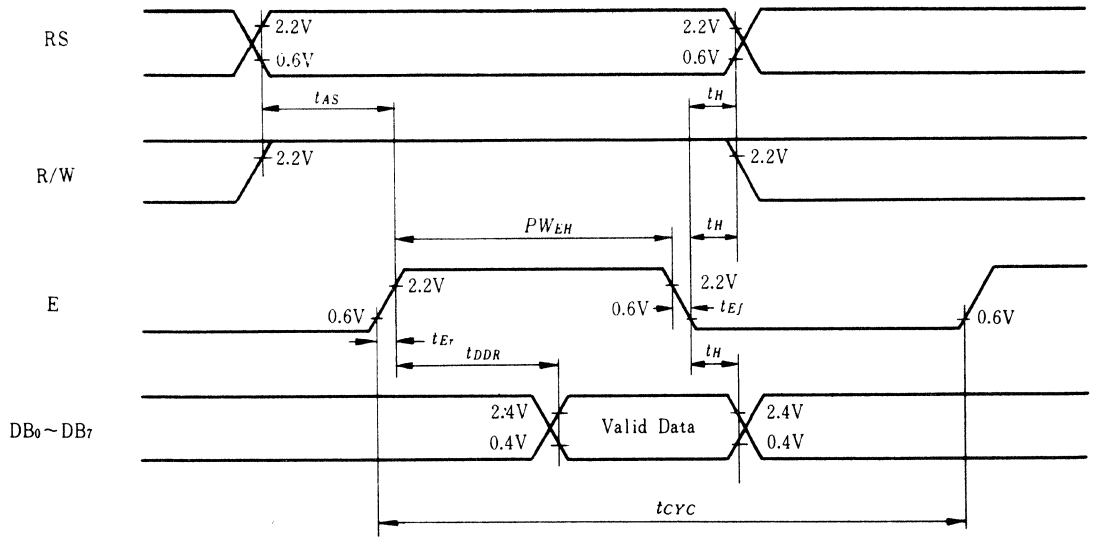


Fig. 6 Interface timing (data read)

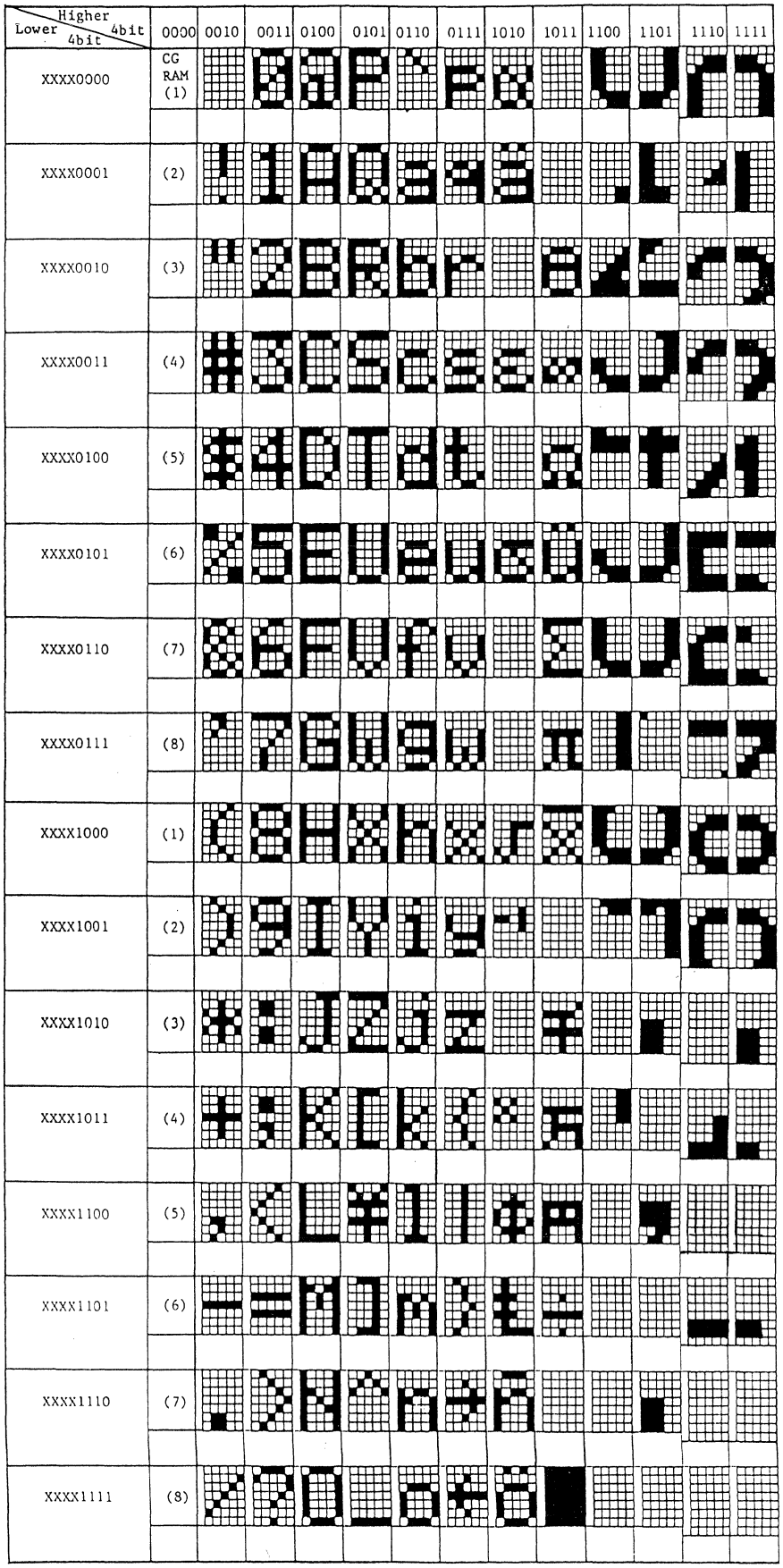


Fig. 7 Character dot pattern

LM032L

- 20 character x 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .116W x 39H (max.) x 13T (max.) mm
Effective display area . . . . . 83W x 18.6H mm
Character size (5 x 7 dots) . . . . . 3.2W x 4.85H mm
Character pitch . . . . . 3.7 mm
Dot size . . . . . 0.6W x 0.65H mm
Weight . . . . . about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V
Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . 2.4V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) . . 0.4V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 1.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta = 0°C . . . . . 4.6 V typ.
Ta = 25°C . . . . . 4.2 V typ.
Ta = 50°C . . . . . 3.5 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

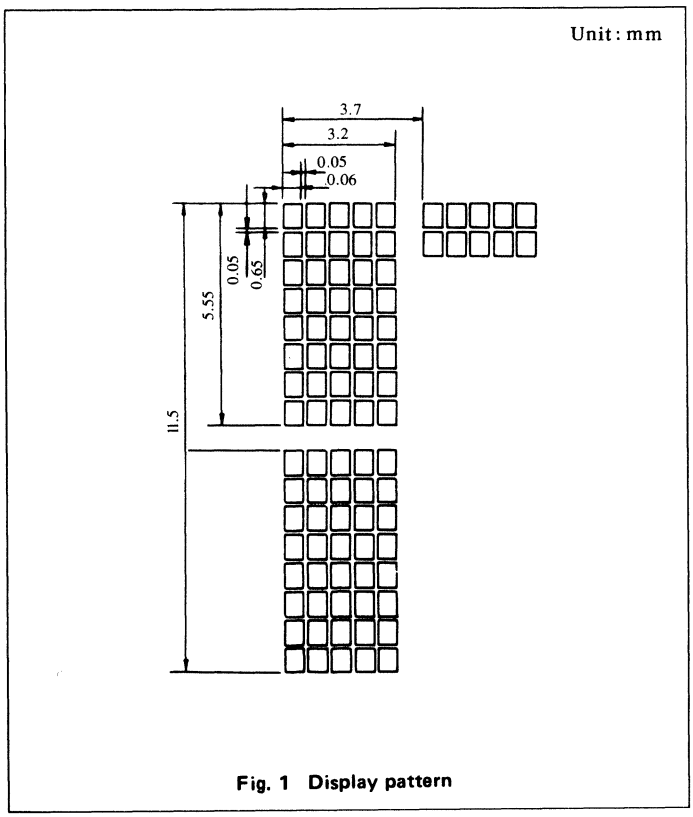


Fig. 1 Display pattern

Unit: mm

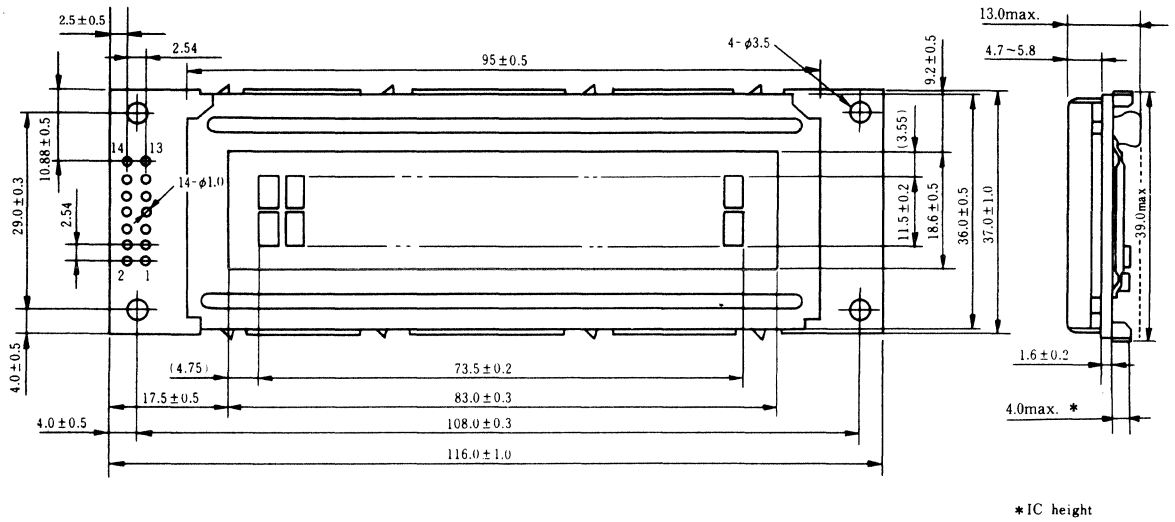


Fig. 2 External dimensions

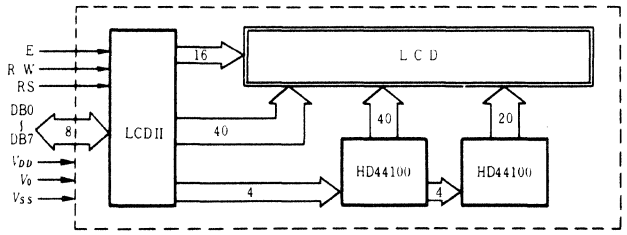
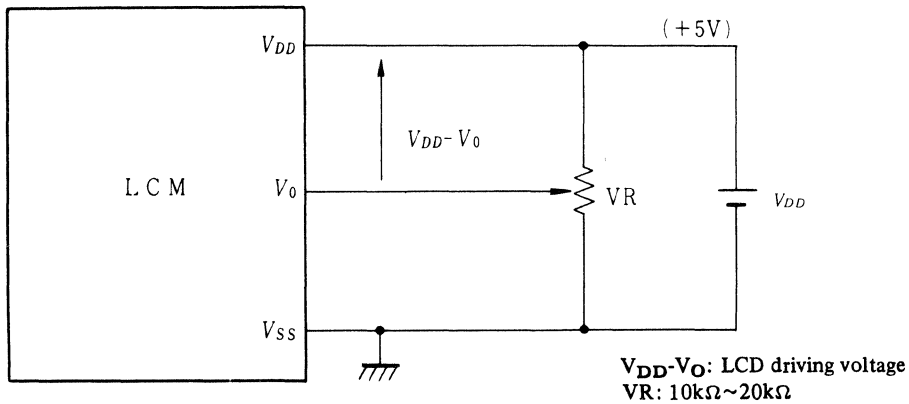


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

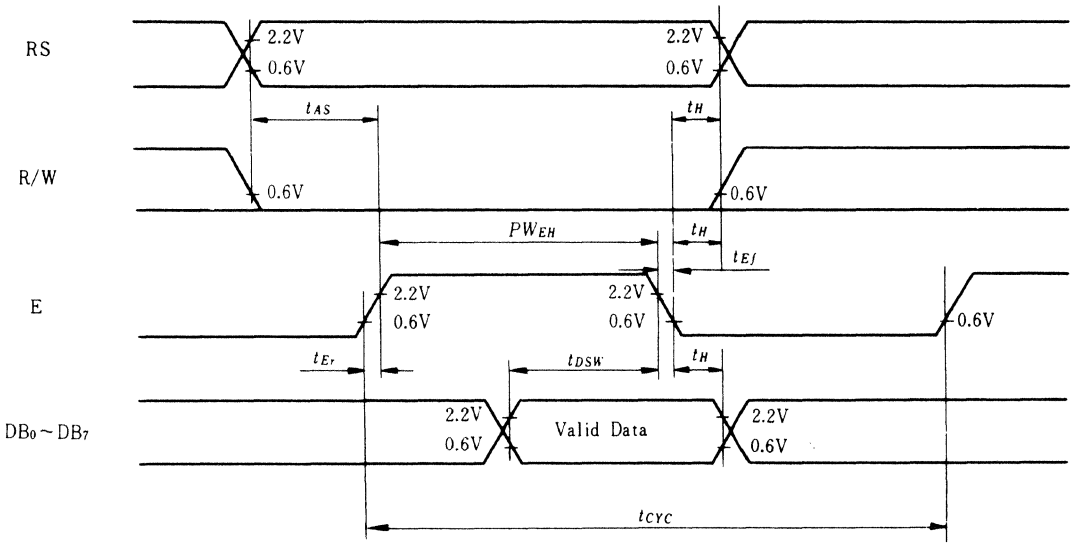


Fig. 5 Interface timing (data write)

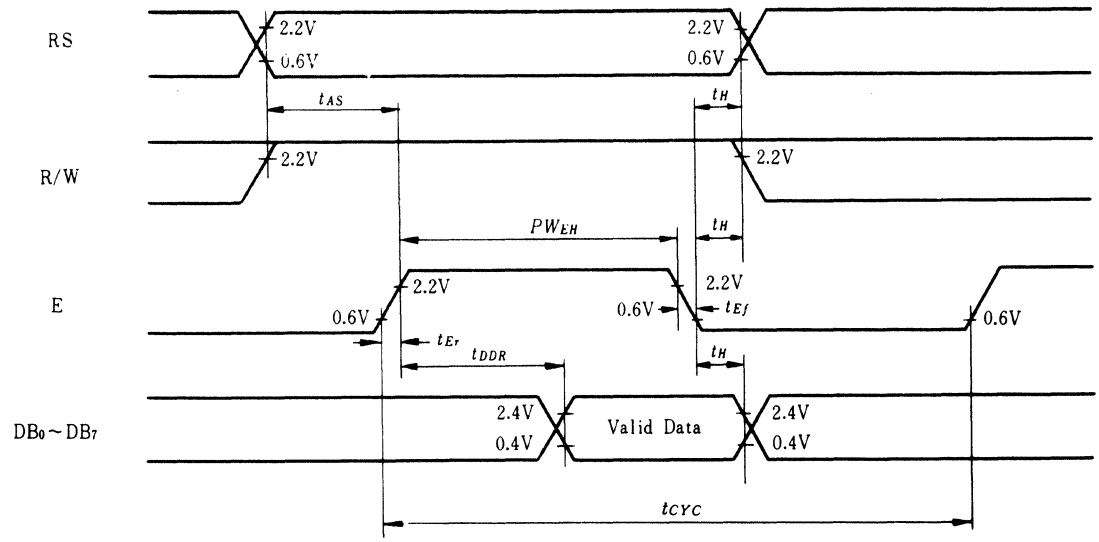


Fig. 6 Interface timing (data read)

LM061L

SUMMARY

- 20 Character x 2 lines
- Built-in control LSI HD44780 type (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .115W x 39H x 13D (max.) mm
Effective display area . . . . . 83W x 18.6H mm
Character size (5 x 7 dots) . . . . . 3.2W x 4.85H mm
Pitch . . . . . 3.7 mm
Dot size . . . . . 0.6W x 0.65H mm
Weight . . . . . about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	6.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	–20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V
Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . .1.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Du=1/16
at Ta = 0°C . . . . . .4.6 V typ.
at Ta = 25°C . . . . . .4.4 V typ.
at Ta = 50°C . . . . . .4.2 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Note:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

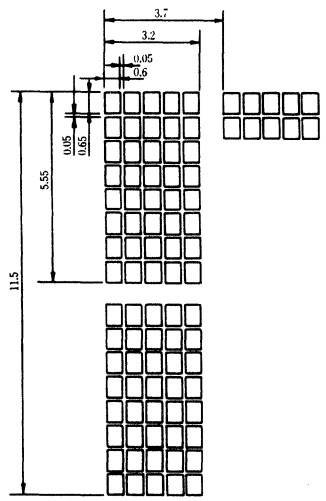
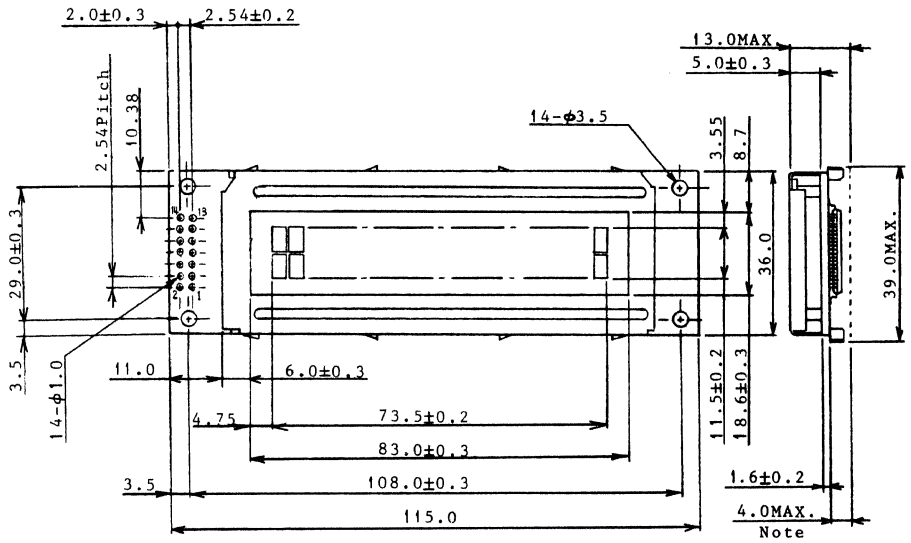


Fig. 1 Display pattern

m



Note : IC hight
Unit : mm
Scale: NTS
No specified tolerance +0.5

Fig. 2 External dimensions

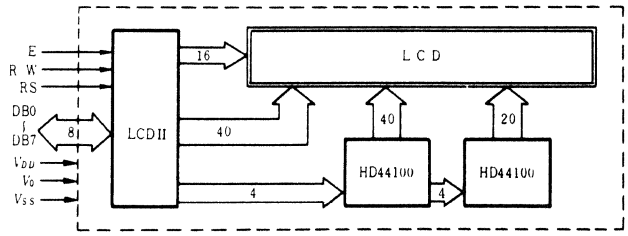
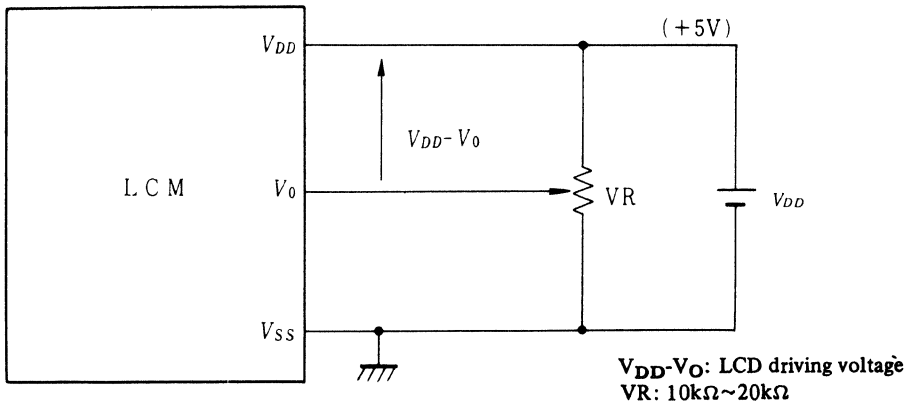


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

SECTION 5

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

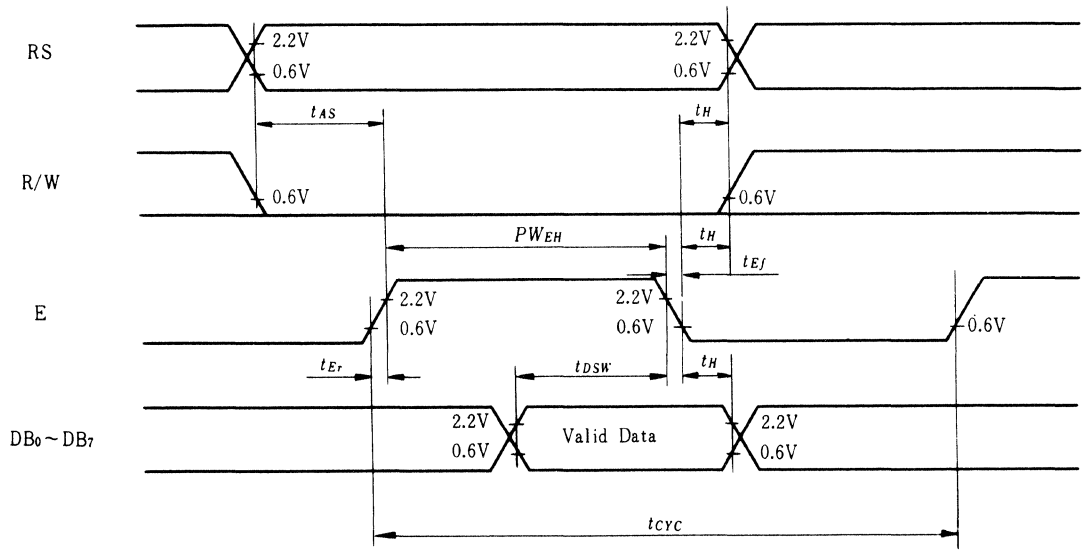


Fig. 5 Interface timing (data write)

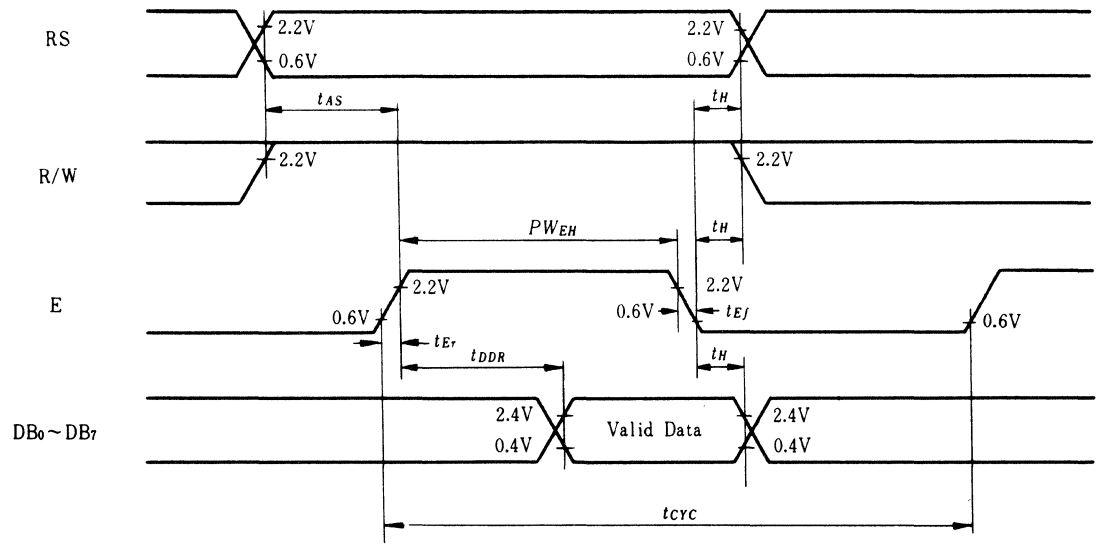


Fig. 6 Interface timing (data read)

LM060L

- 24 character x 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 116W x 39H (max.) x 13T (max.) mm
Effective display area . . . . . 83W x 18.6H mm
Character size (5 x 7 dots) . . . . . 2.7W x 4.85H mm
Character pitch . . . . . 3.2 mm
Dot size . . . . . 0.5W x 0.65H mm
Dot pitch . . . . . 0.55W x 0.7H mm
Weight . . . . . about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) 2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA) . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 2.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta = 0°C . . . . . 4.6 V typ.
Ta = 25°C . . . . . 4.4 V typ.
Ta = 50°C . . . . . 3.2 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

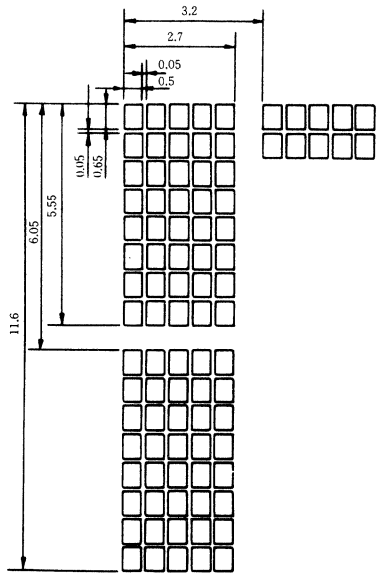


Fig. 1 Display pattern

SECTION 5

Unit: mm

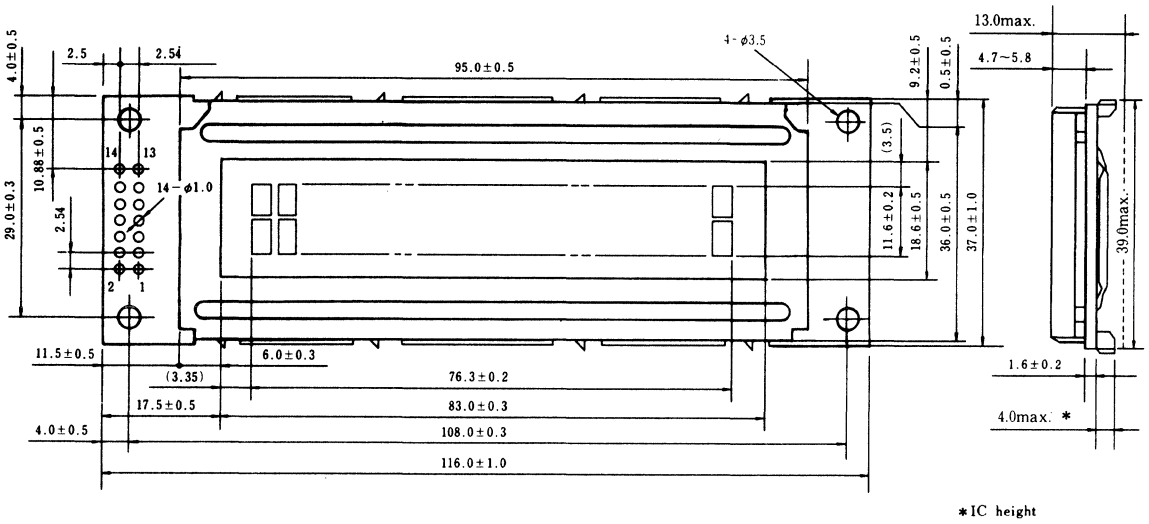
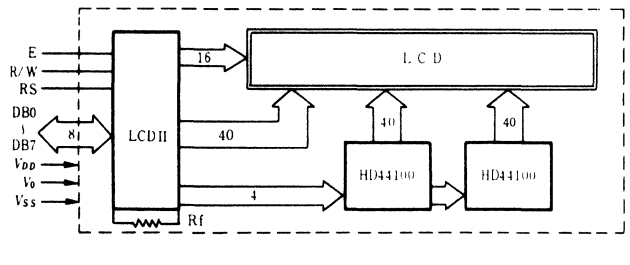
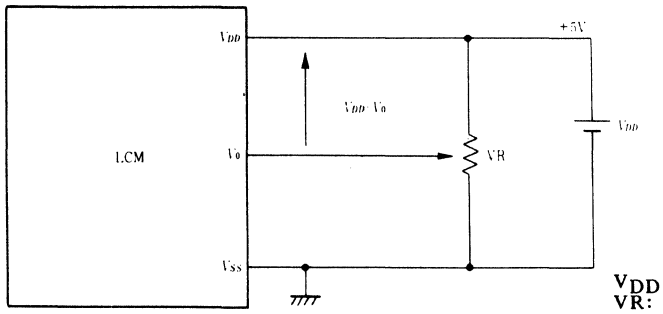


Fig. 2 External dimensions



Rf = 200kΩ

Fig. 3 Block diagram



$V_{DD} \sim V_0$: LCD driving voltage
VR: 10kΩ ~ 20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

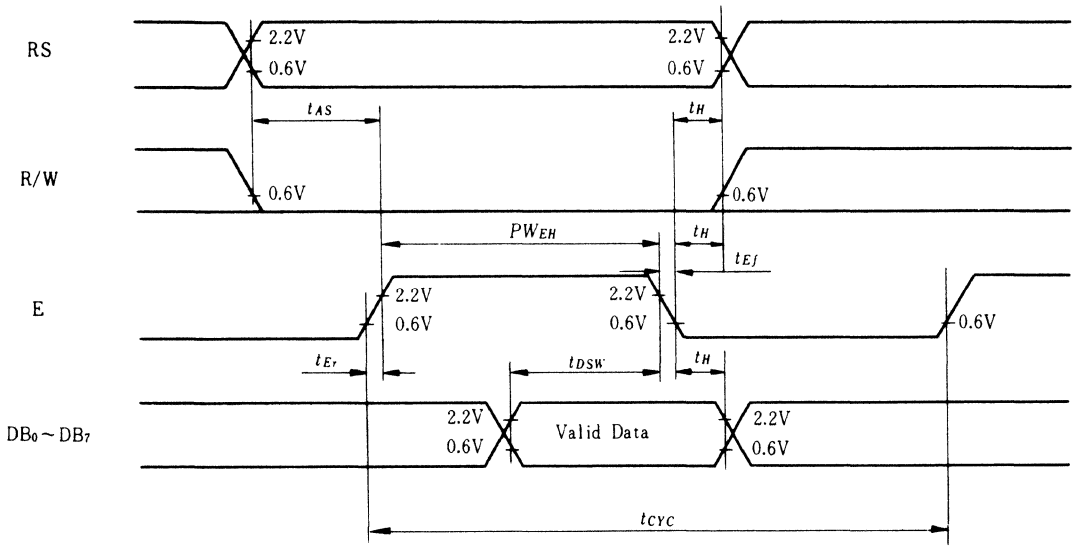


Fig. 5 Interface timing (data write)

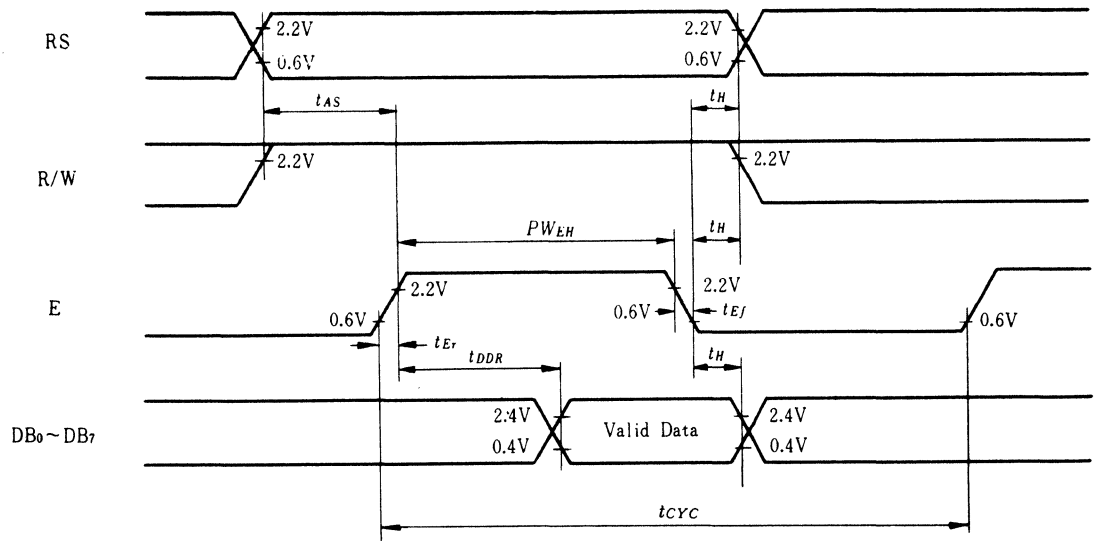


Fig. 6 Interface timing (data read)

LM017L

- 32 character x 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . 174.5W x 33H (max.) x 13.4T (max.) mm
Effective display area . . . . . 141.19W x 16.75H mm
Character size (5 x 7 dots) . . . . . 3.45W x 4.85H mm
Character pitch . . . . . 4.2 mm
Dot size . . . . . 0.65W x 0.65H mm
Weight . . . . . about 60g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
power supply for LCD drive ($V_{DD}-V_O$) .	0	13.5V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V ±0.25V
Input "high" voltage (V_{IH}) . . . . . 2.2V min.
Input "low" voltage (V_{IL}) . . . . . 0.6V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA) . 2.4V min.
Output "low" voltage (V_{OL}) (I_{OL}=1.2mA) . . 0.4 Vmax.
Power supply current (I_{DD}) (V_{DD}=5.0V) . . 1.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta=0°C . . . . . 4.6 V typ.
Ta=25°C . . . . . 4.4 V typ.
Ta=50°C . . . . . 4.2 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

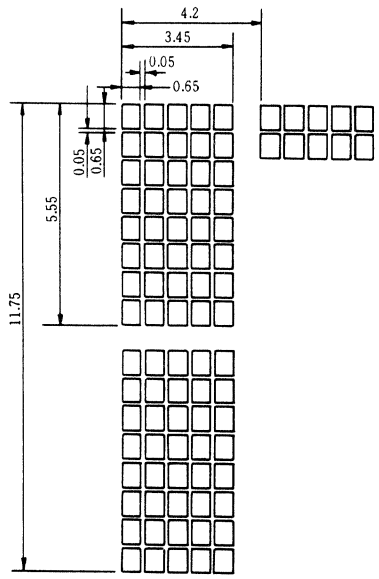


Fig. 1 Display pattern

Unit: mm

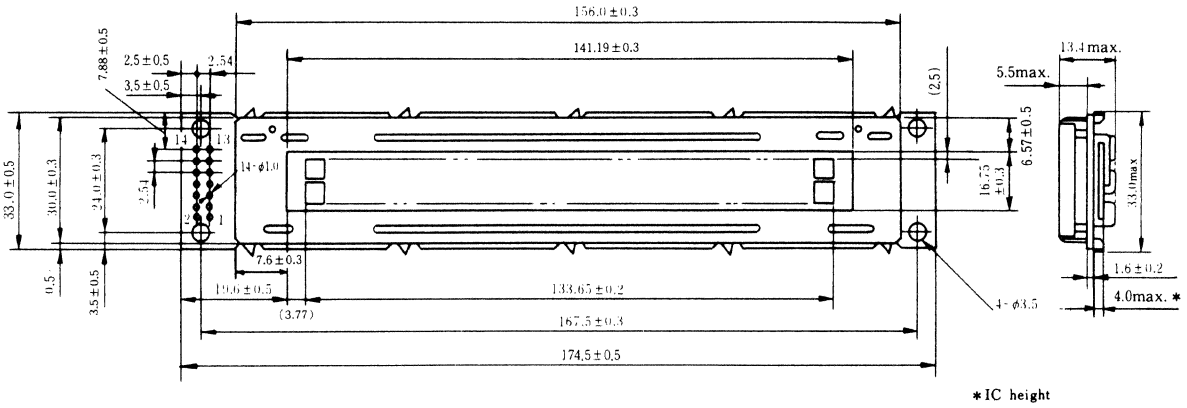


Fig. 2 External dimensions

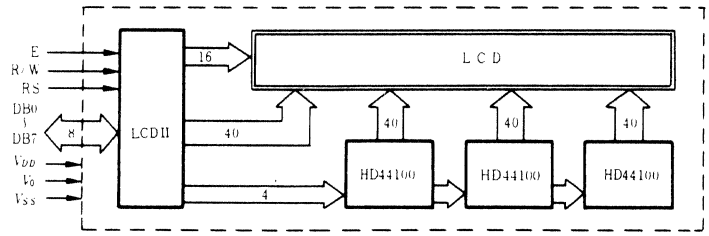


Fig. 3 Block diagram

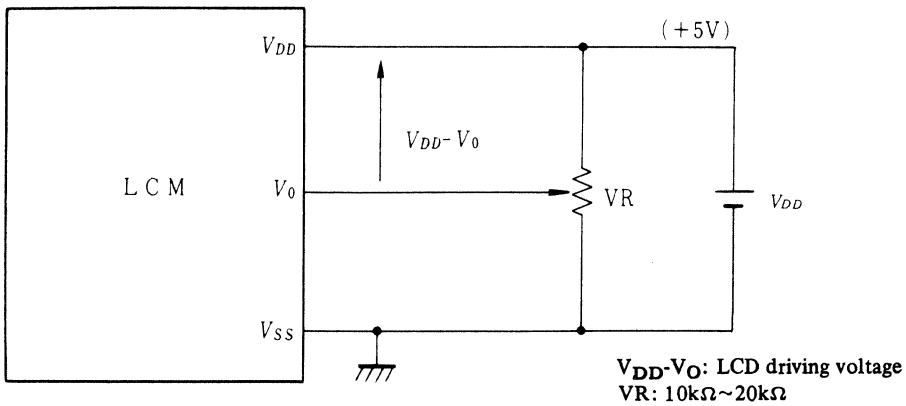


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

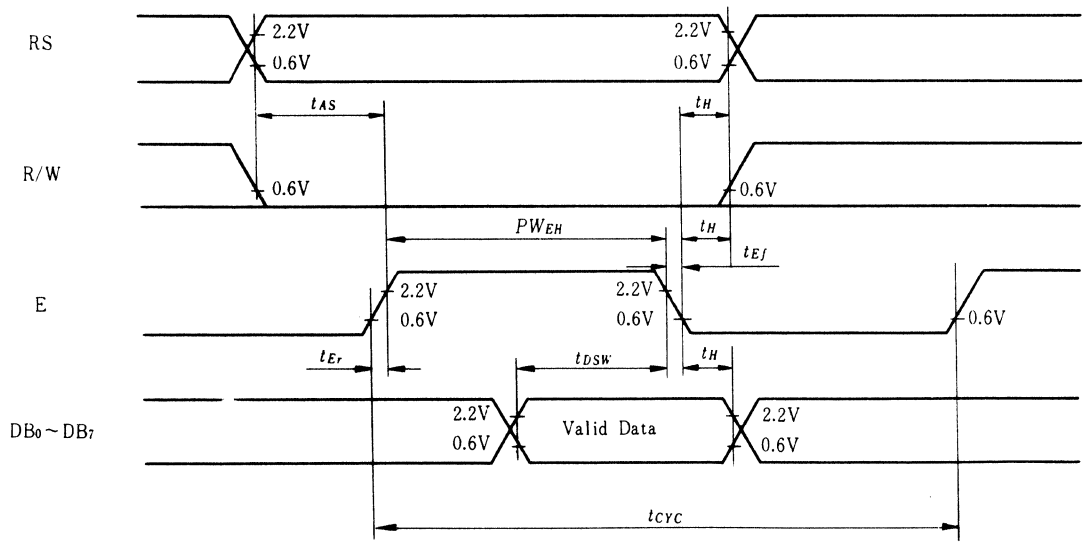


Fig. 5 Interface timing (data write)

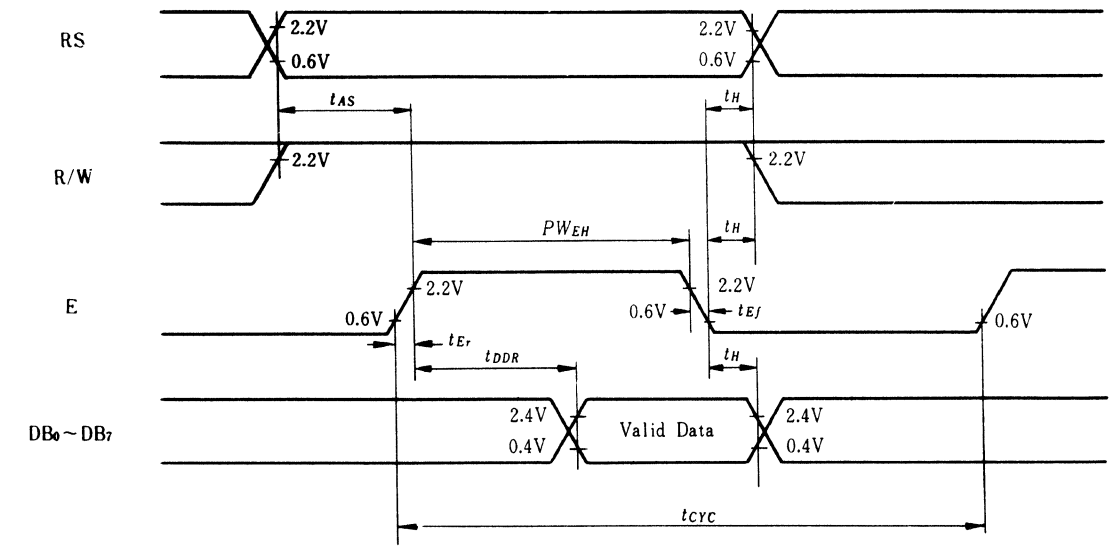


Fig. 6 Interface timing (data read)

LM018L

- 40 character x 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size .... 182W x 35.5H (max.) x 13T (max.) mm
Effective display area ..... 154.0W x 15.3H mm
Character size (5 x 7 dots) ..... 3.2W x 4.85H mm
Character pitch..... 3.7 mm
Dot size ..... 0.6W x 0.65H mm
Weight ..... about 65g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V ±0.25V
Input "high" voltage (V_{IH}) ..... 2.2V min.
Input "low" voltage (V_{IL}) ..... 0.6V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA) . 2.4V min.
Output "low" voltage (V_{OL}) (I_{OL}=1.2mA) ... 0.4V max.
Power supply current (I_{DD}) (V_{DD}=5.0V) ... 3.0 mA typ.
4.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta=0°C .....4.6 V typ.
Ta=25°C .....4.4 V typ.
Ta=50°C .....4.2 V typ.

OPTICAL DATA ..... See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

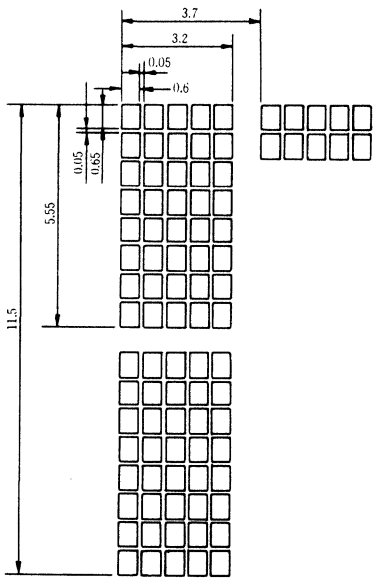


Fig. 1 Display pattern

SECTION 5

Unit: mm

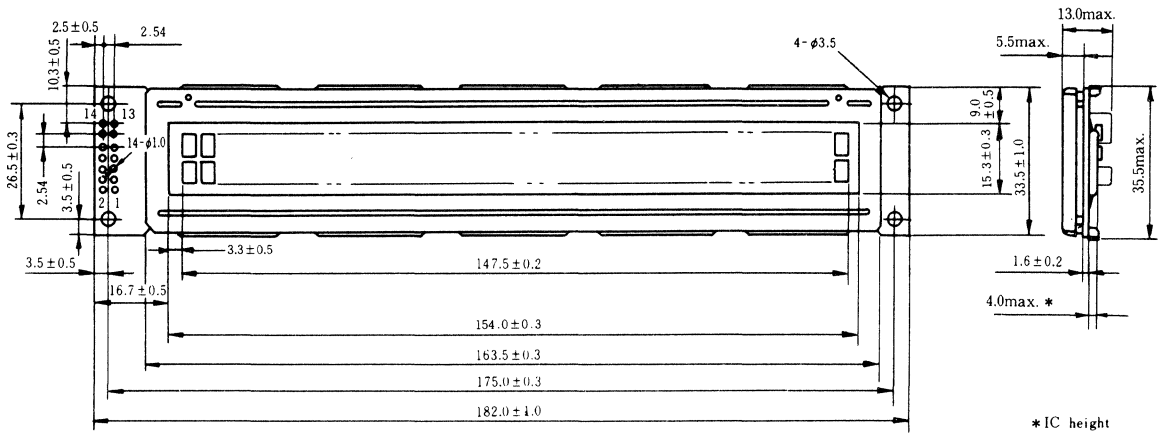


Fig. 2 External dimensions

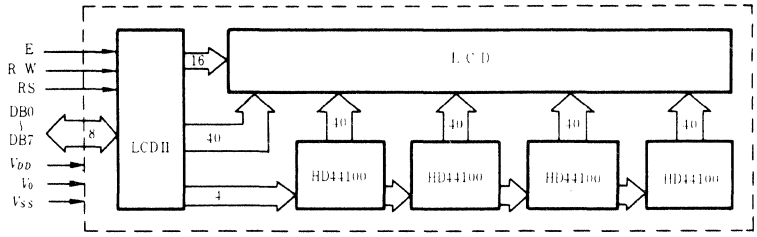


Fig. 3 Block diagram

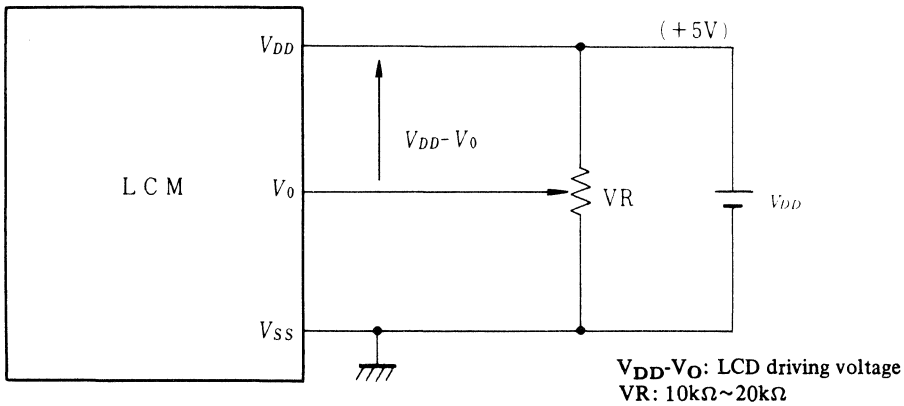


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

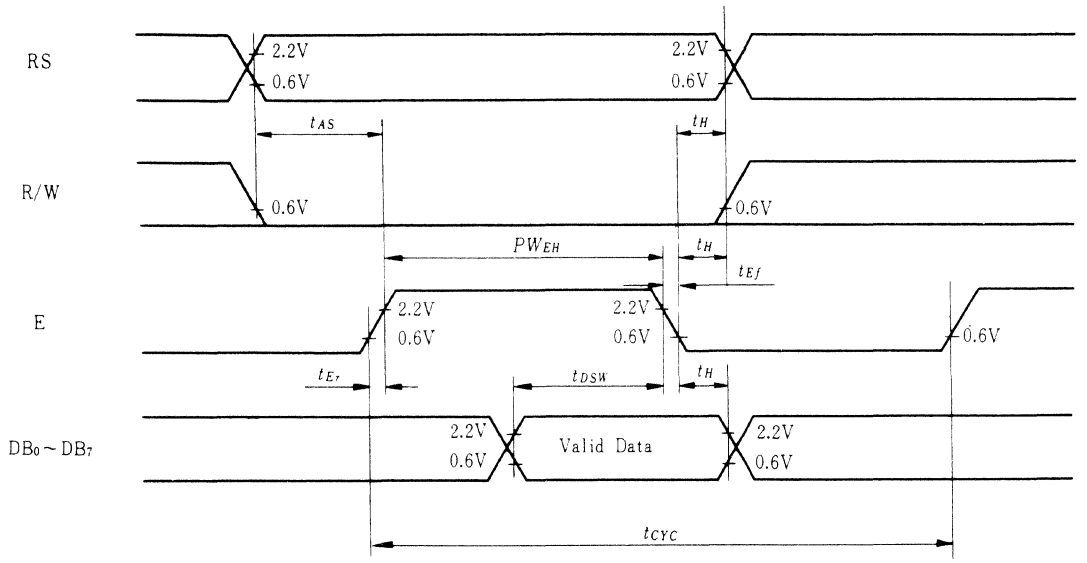


Fig. 5 Interface timing (data write)

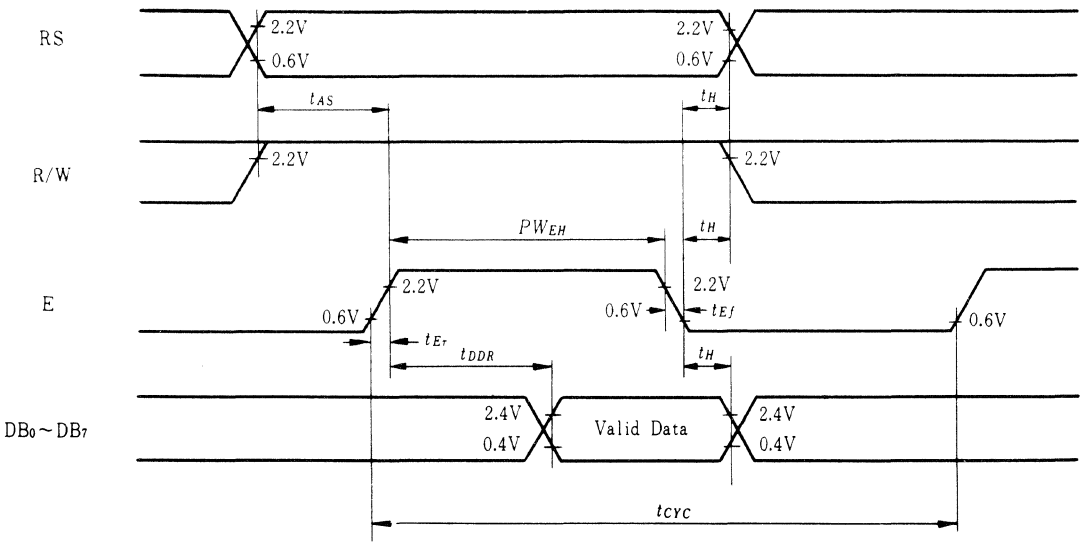


Fig. 6 Interface timing (data read)

LM041L

- 16 character x 4 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 87W x 60H x 12T (max.) mm
Effective display area . . . . . 61.8W x 25.2H mm
Character size (5 x 7 dots) . . . . . 2.95W x 4.15H mm
Character pitch . . . . . 3.55 mm
Dot size . . . . . 0.55W x 0.55H mm
Weight . . . . . about 60g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5V
Input voltage (V_I)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V
Input "high" voltage (V_{IH}) . . . . . 2.2V min.
Input "low" voltage (V_{IL}) . . . . . 0.6V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA) . 2.4V min.
Output "low" voltage (V_{OL}) (I_{OL}=1.2mA) . . . 0.4V max.
Power supply current (I_{DD}) (V_{DD}=5.0V) . . . 3.0 mA typ.
4.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta=0°C . . . . . 4.6 V typ.
Ta=25°C . . . . . 4.4 V typ.
Ta=50°C . . . . . 4.2 V typ.

OPTICAL DATA . . . . . See page 15.

Unit: mm

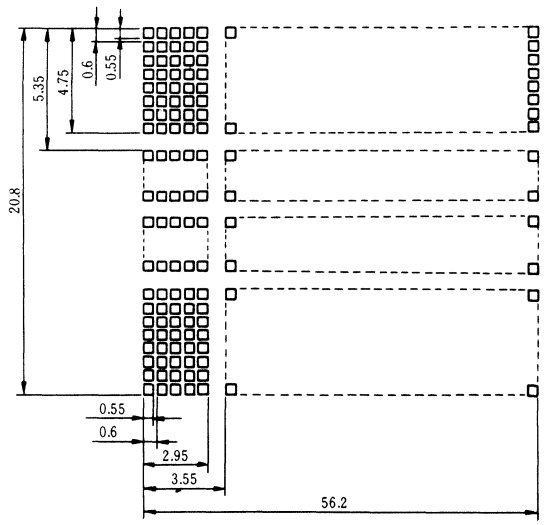


Fig. 1 Display pattern

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

DISPLAY POSITION AND DD RAM ADDRESS

Character No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
2nd line	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF
3rd line	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
4th line	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF

Notes:

(1) 80 ~ DF are described in hexidecimal for DD RAM address.
(2) The set to HD44780 are "N = "1", F = "0" (2 lines 5 x 7 + cursol)."
(3) DD RAM address is no series in line. Address set is necessary to change the lines.
(4) Circuit is equal to 32 characters by 2 lines type.
(5) In case of executing shift, first line and third line are shifted continuously, also second line and fourth line. Therefore it happens that display of third line is transferred to first line.

Unit: mm

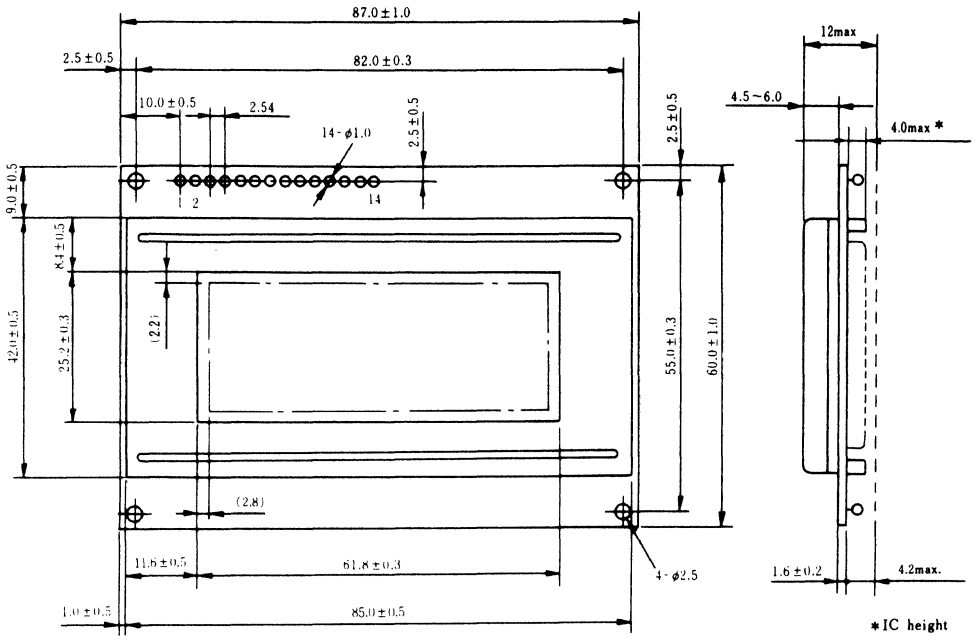


Fig. 2 External dimensions

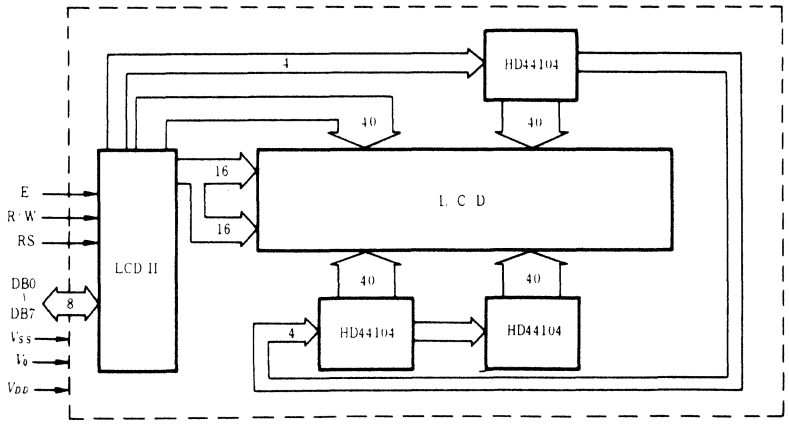
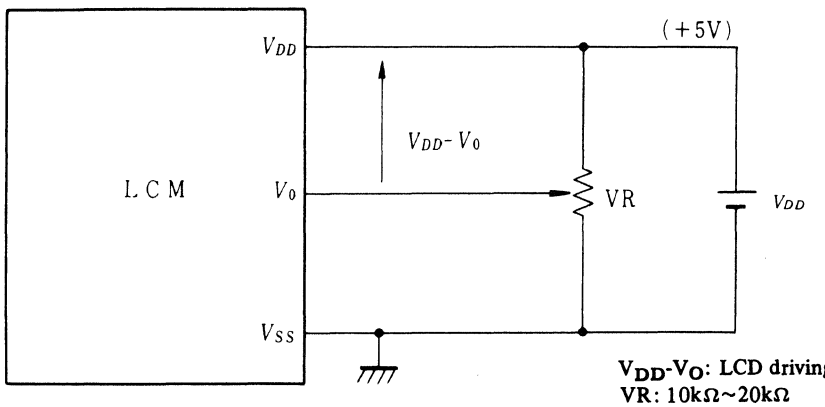


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

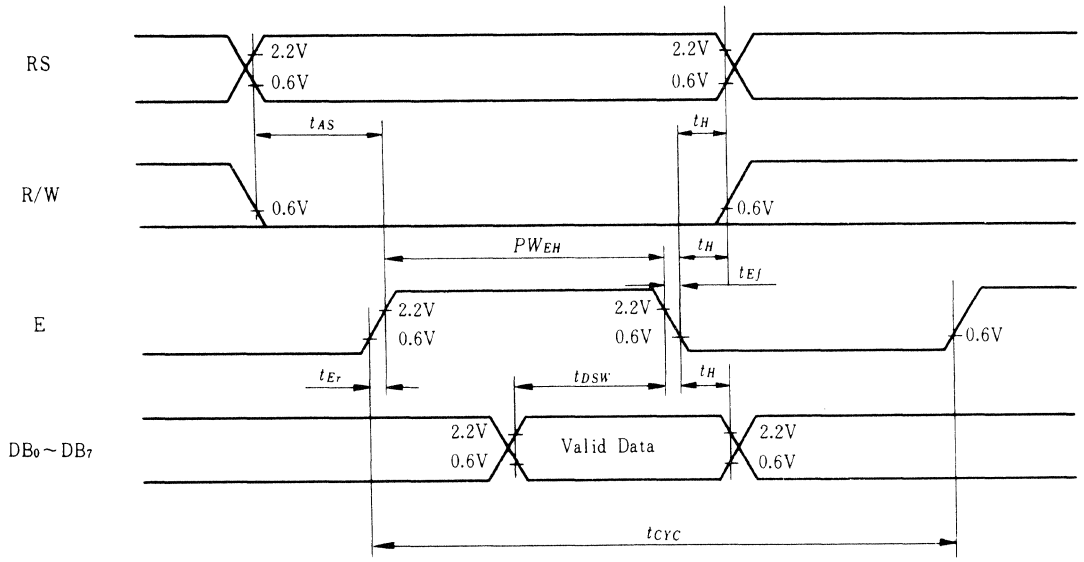


Fig. 5 Interface timing (data write)

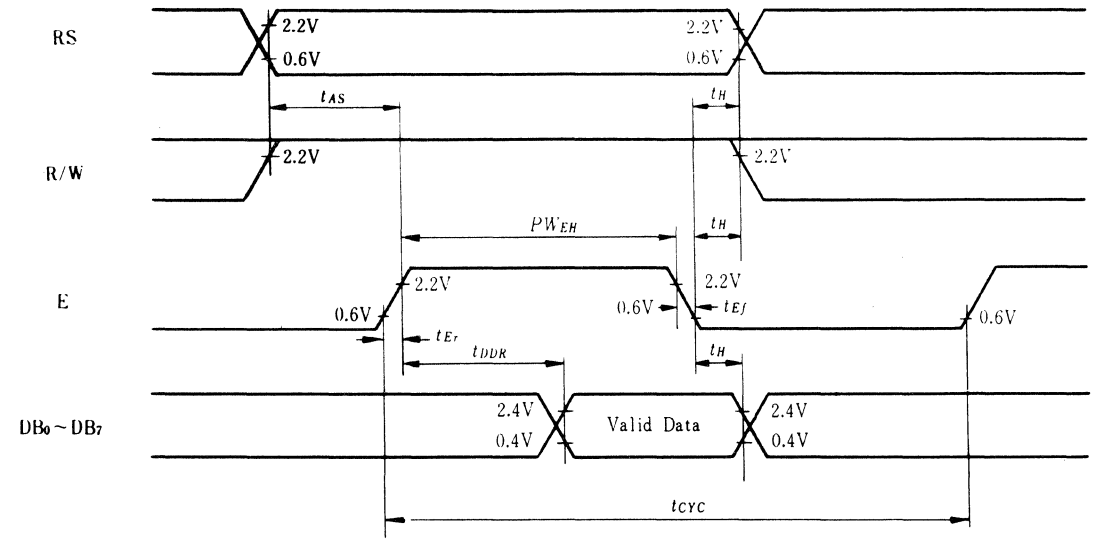


Fig. 6 Interface timing (data read)

LM044L

- 20 character x 4 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size	98W x 60H x 12T (max.) mm
Effective display area	76.0W x 25.2H mm
Character size (5 x 7 dots)	2.95W x 4.15H mm
Character pitch	3.55 mm
Dot size	0.55W x 0.55H mm
Weight	about 65 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H)	2.2 V min.
Input "low" voltage (Vi_L)	0.6 V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA)	2.4 V min.
Output "low" voltage (V_{OL}) (I_{OL} = 1.2 mA)	0.4 V max
Power supply current (I_{DD}) (V_{DD} = 5.0 V)	1.0 mA typ. 3.5 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)	Duty = 1/16
Ta = 0°C	4.6 V typ.
Ta = 25°C	4.4 V typ.
Ta = 50°C	4.2 V typ.

OPTICAL DATA ..... See page 15.

Unit: mm

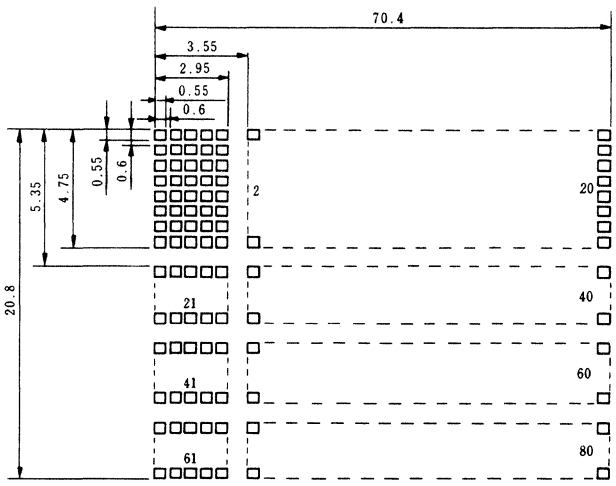


Fig. 1 Display pattern

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

DISPLAY POSITION AND DD RAM ADDRESS

Character No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1st line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93
2nd line	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3
3rd line	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
4th line	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7

Notes:

(1) 80 ~ E7 are described in hexidecimal for DD RAM address.

(2) Function setting of HD44780 should be "N = "1", F = "0" (2 lines of 5 x 7 + cursol).

(3) DD RAM address is no series in line. Address setting is necessary to change the lines.

(4) Circuit is equal to 40 characters by 2 lines type.

(5) In case of executing shift, first line and third line are shifted continuously, also second line and fourth line. Therefore it happens that display of third line is transferred to first line.

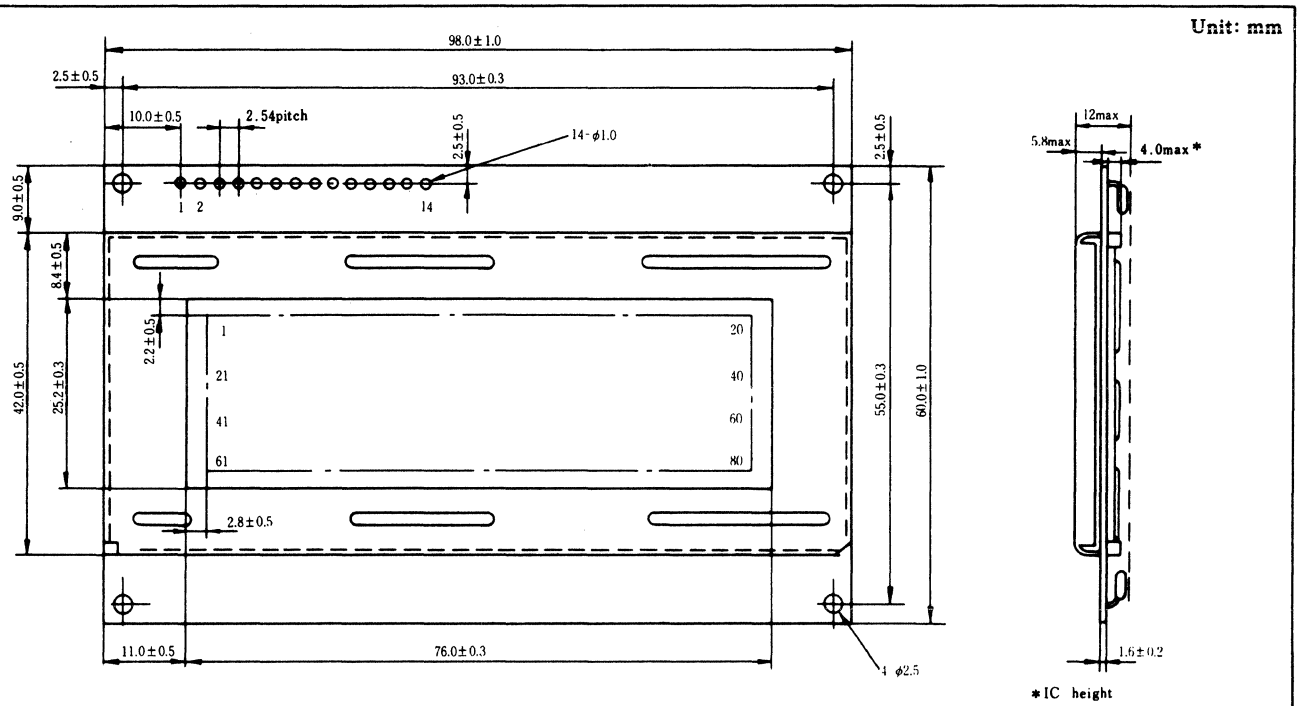


Fig. 2 External dimension

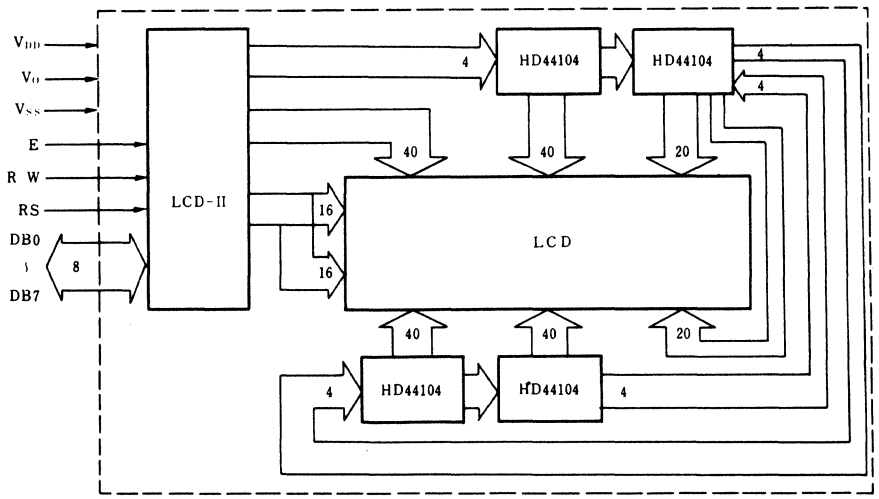
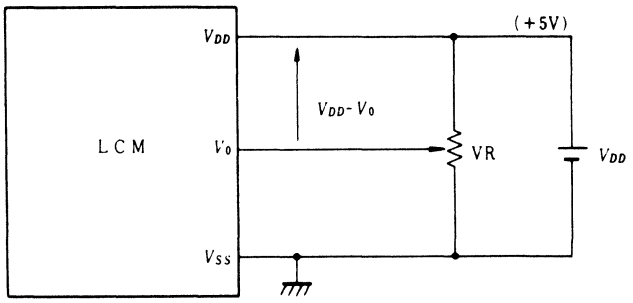


Fig. 3 Block diagram



V_{DD}-V_O: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

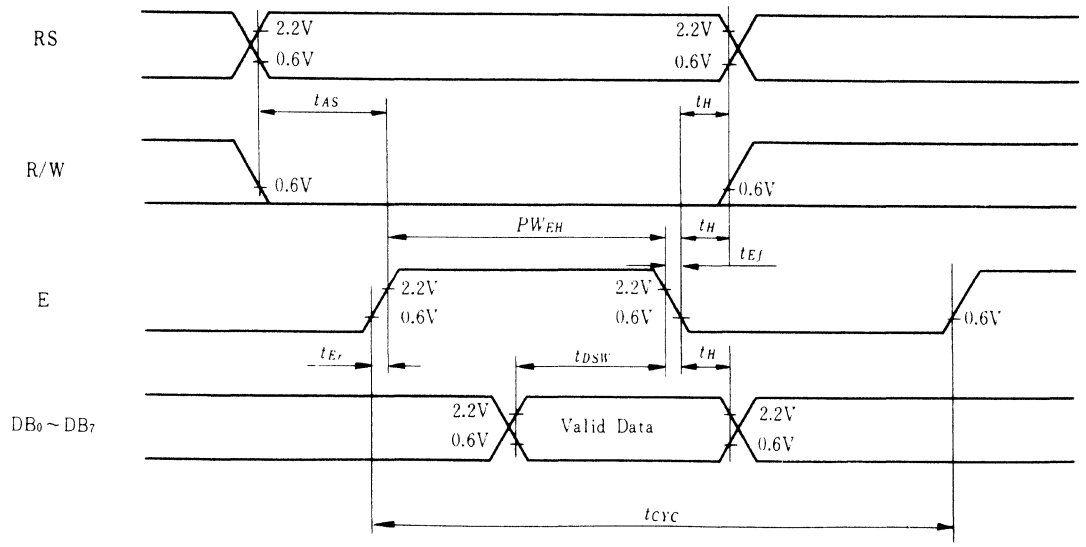


Fig. 5 Interface timing (data write)

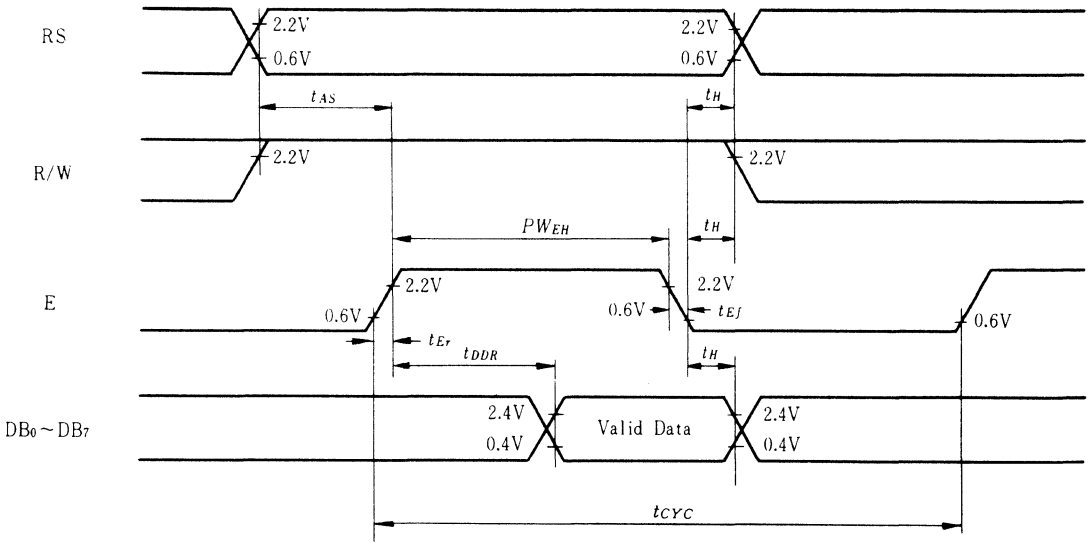


Fig. 6 Interface timing (data read)

COMPACT VERSION CHARACTER LCD MODULES

LM104L

SUMMARY

- 16 Character x 2 lines
- Built-in control LSI HD44780 type (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .80W x 30H x 11D (max.) mm
Effective display area . . . . . .62W x 15.1H mm
Character size (5 x 10 dots) . . . . . .29.5W x 4.56H mm
Pitch . . . . . .3.55 mm
Dot size . . . . . .0.55W x 0.66H mm
Weight . . . . . .about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	6.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 2.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Du=1/16
at Ta = 0°C . . . . . 4.6 V typ.
at Ta = 25°C . . . . . 4.4 V typ.
at Ta = 50°C . . . . . 4.2 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Note:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7, and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

(3) Effective display area

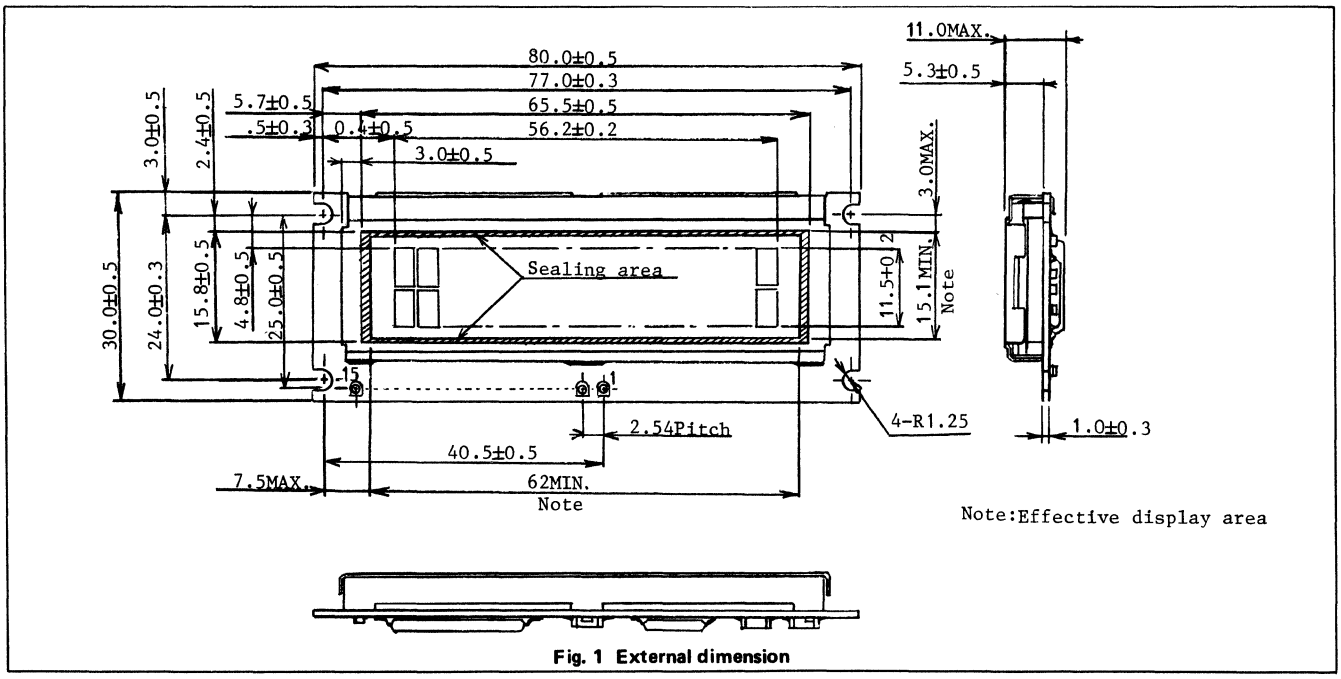


Fig. 1 External dimension

HITACHI

Unit: mm

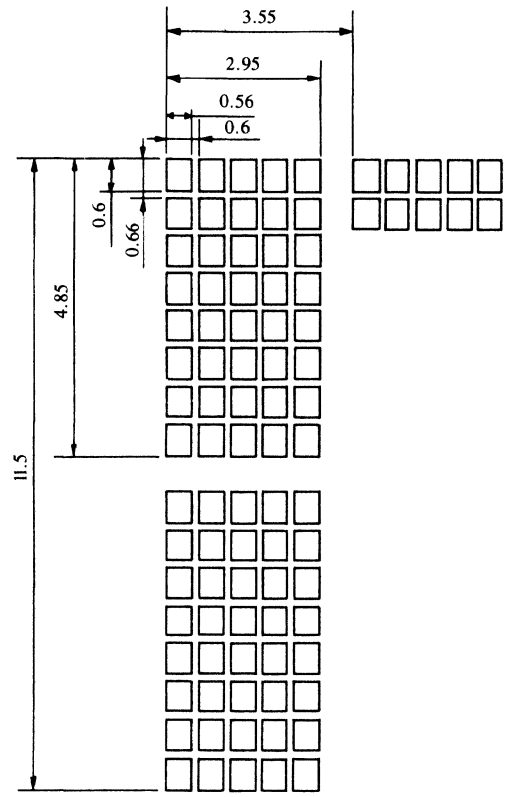


Fig. 2 Display pattern

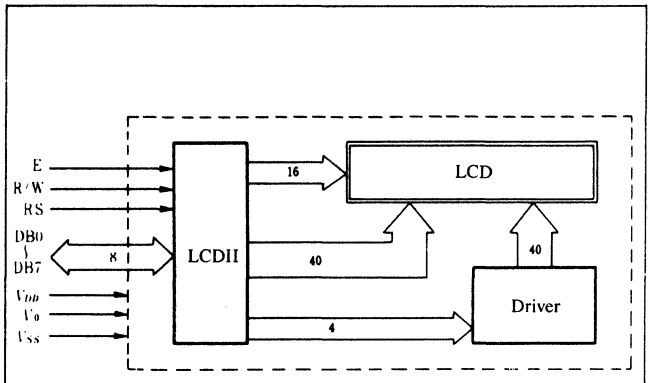


Fig. 3 Block diagram

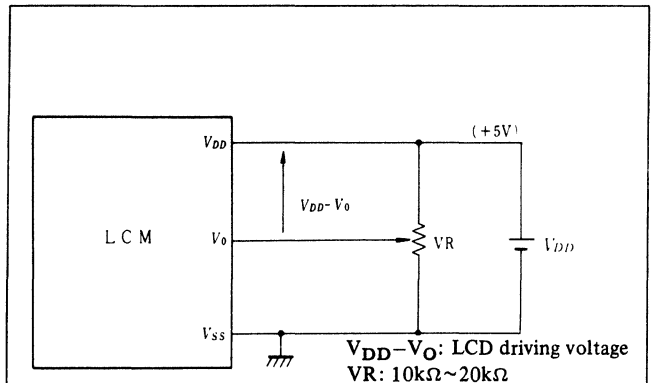


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

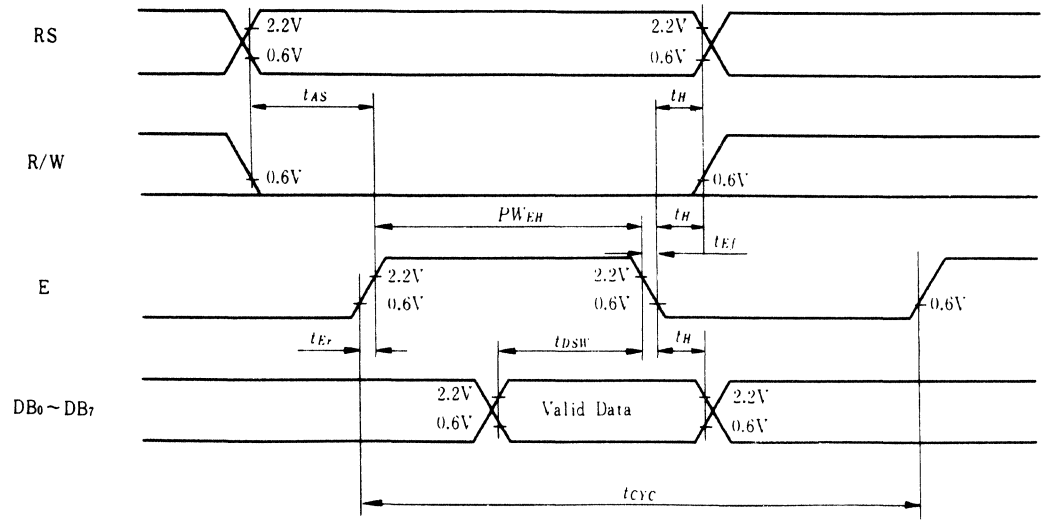


Fig. 5 Interface timing (data write)

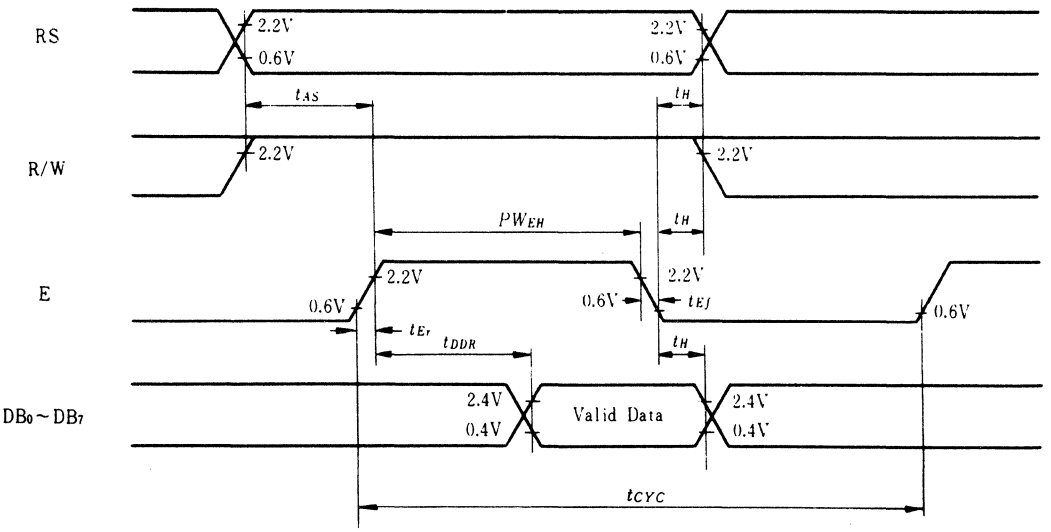


Fig. 6 Interface timing (data read)

LM105L

SUMMARY

- 20 Character x 2 lines
- Built-in control LSI HD44780 type (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .95W x 30H x 11T (max.) mm
Effective display area . . . . . .76.7W x 15.1H mm
Character size (5 x 7 dots) . . . . . 3.2W x 4.85H mm
Pitch . . . . . 3.7 mm
Dot size . . . . . 0.6W x 0.65H mm
Weight . . . . . about 50 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	6.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ± 0.25 V

Input "high" voltage (Vi_H) . . . . . 2.2 V min.
Input "low" voltage (Vi_L) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2 mA) . . 2.4 V min.
Output low voltage (V_{OL}) (I_{OL} = 1.2 mA) . . . . 0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V) . . 2.0 mA typ.
3.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Du=1/16
at Ta = 0°C . . . . . 4.6 V typ.
at Ta = 25°C . . . . . 4.2 V typ.
at Ta = 50°C . . . . . 3.5 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Note:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

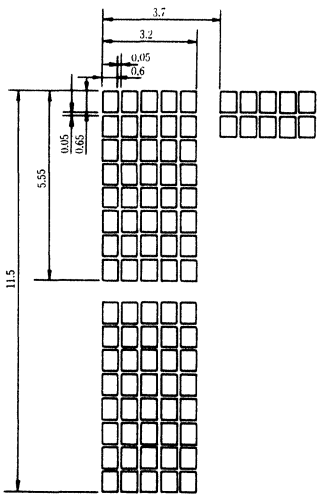


Fig. 1 Display pattern

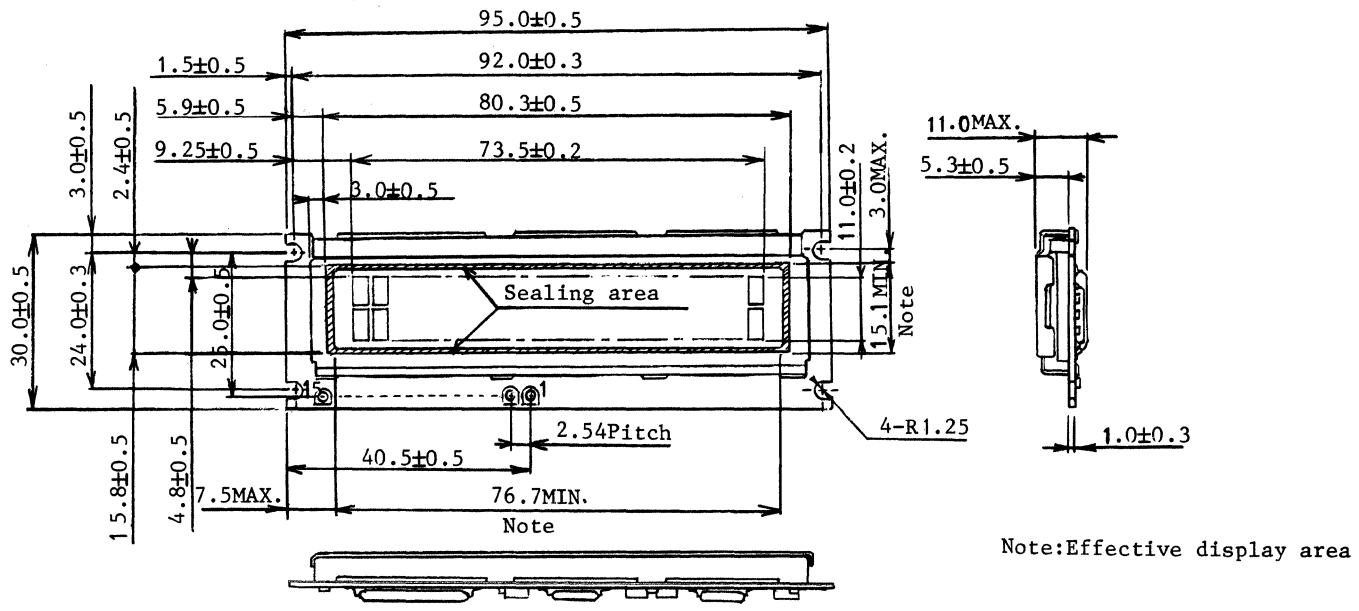


Fig. 2 External dimension

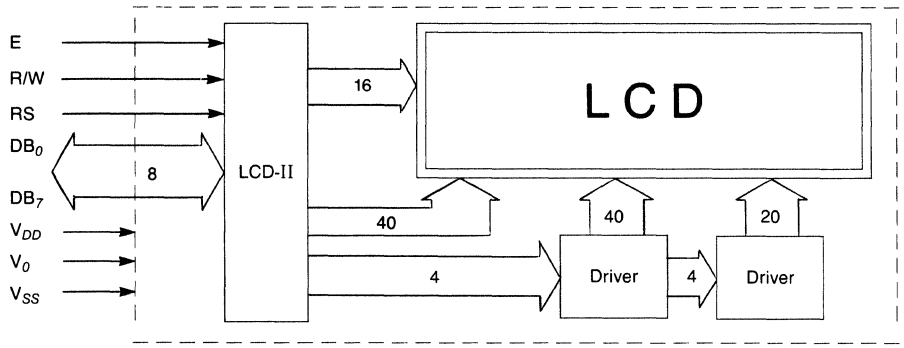


Fig. 3 Block diagram

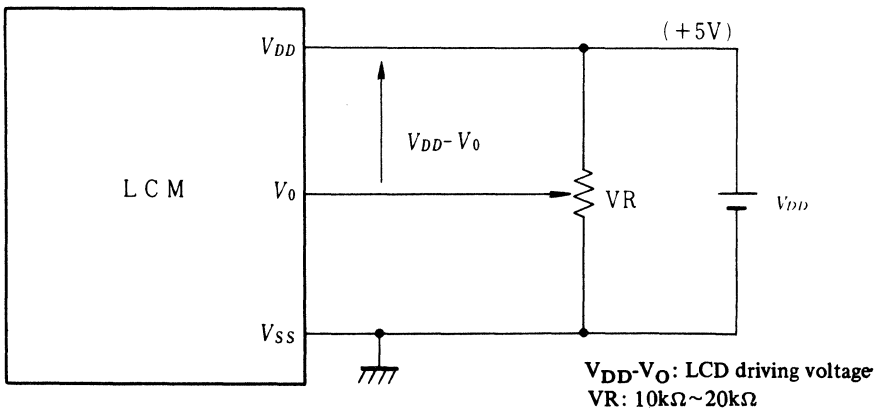


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

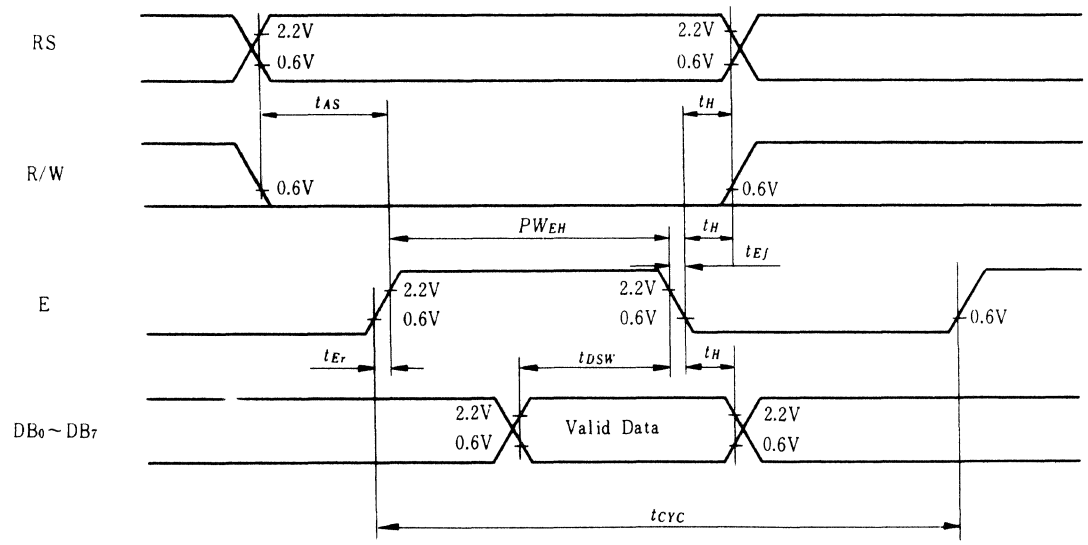


Fig. 5 Interface timing (data write)

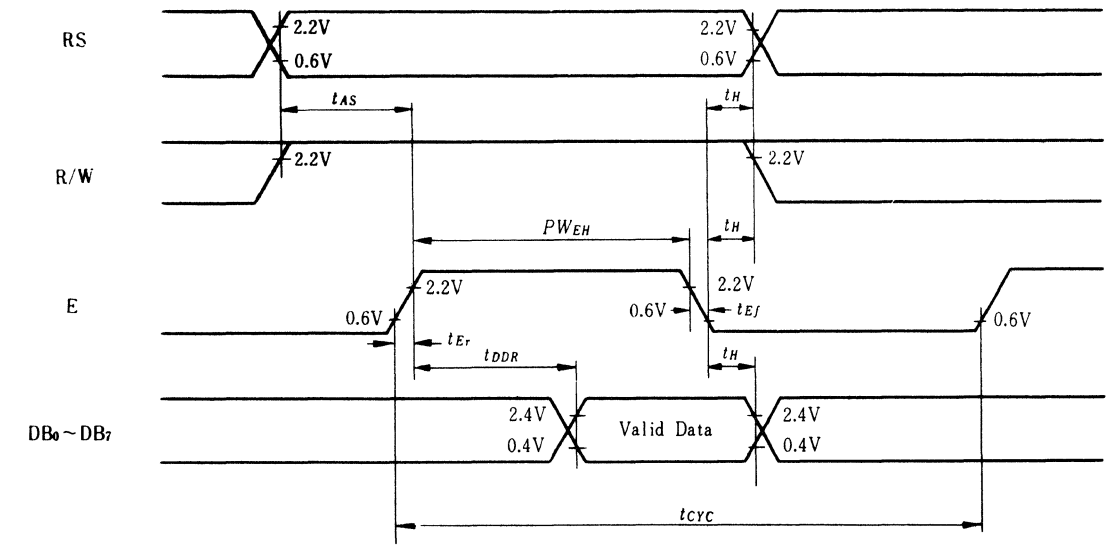


Fig. 6 Interface timing (data read)

LM107L

- 40 character x 2 lines
- Controller LSI HD44780 is built-in (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . .170 x 30 (max.) x 11 (max.) mm
Effective display area . . . . . .152.6W x 15.1H mm
Character size (5 x 7 dots) . . . . . 3.2W x 4.85H mm
Character pitch . . . . . 3.7 mm
Dot size . . . . . 0.6W x 0.65H mm
Weight . . . . . about 65g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	6.5 V
Power supply for LCD drive ($V_{DD}-V_O$)	0	6.5 V
Input voltage (V_i)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V ±0.25V
Input "high" voltage (V_{iH}) . . . . . 2.2V min.
Input "low" voltage (V_{iL}) . . . . . 0.6V max.
Output "high" voltage (V_{OH}) ($-I_{OH}$=0.2mA) . 2.4V min.
Output "low" voltage (V_{OL}) (I_{OL}=1.2mA) . . . 0.4V max.
Power supply current (I_{DD}) (V_{DD}=5.0V) . . . 3.0 mA typ.
4.0 mA max.
Power supply for LCD drive (Recommended) ($V_{DD}-V_O$)
Duty = 1/16
Ta=0°C . . . . . .4.6 V typ.
Ta=25°C . . . . . .4.4 V typ.
Ta=50°C . . . . . .4.2 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Notes:

In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

Unit: mm

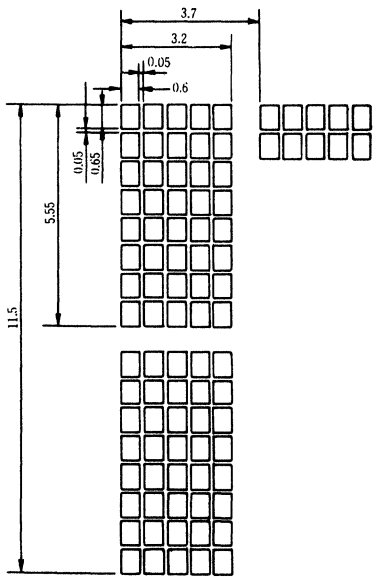
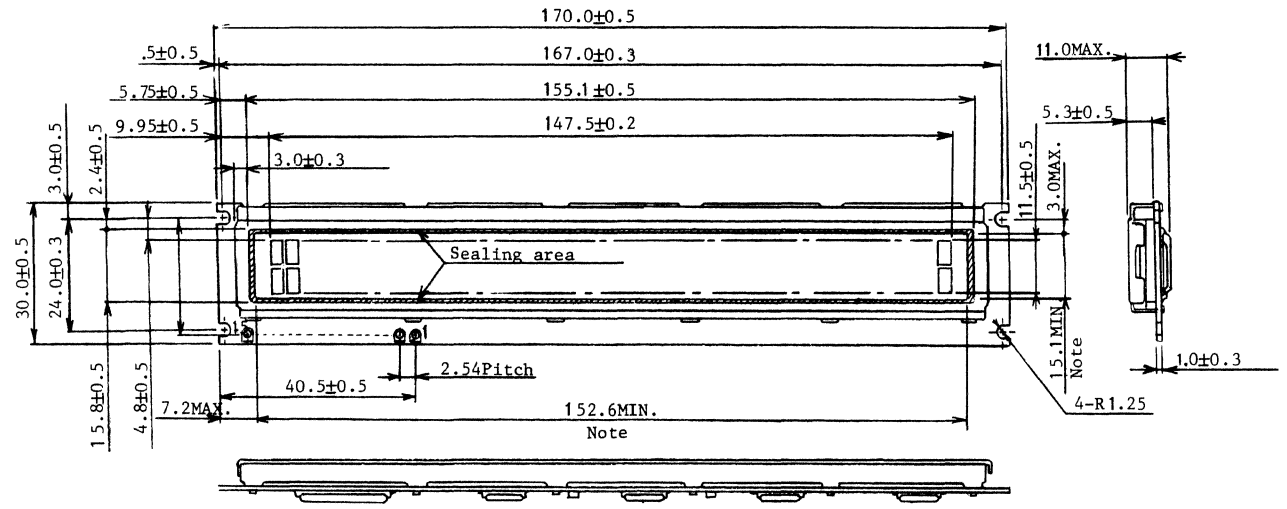


Fig. 1 Display pattern



Note: Effective display area

Fig. 2 External dimension

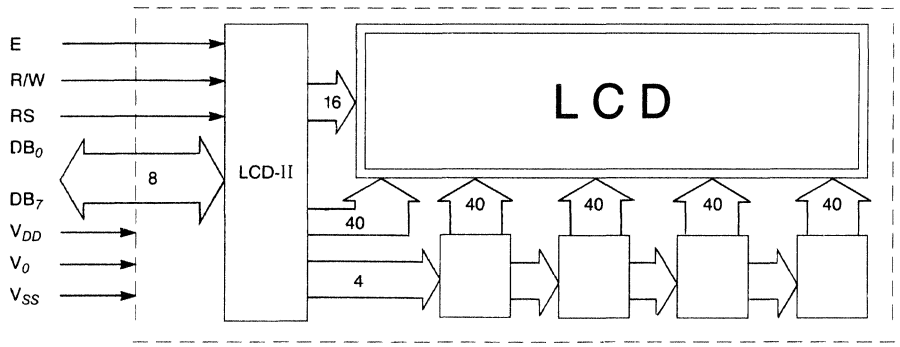


Fig. 3 Block diagram

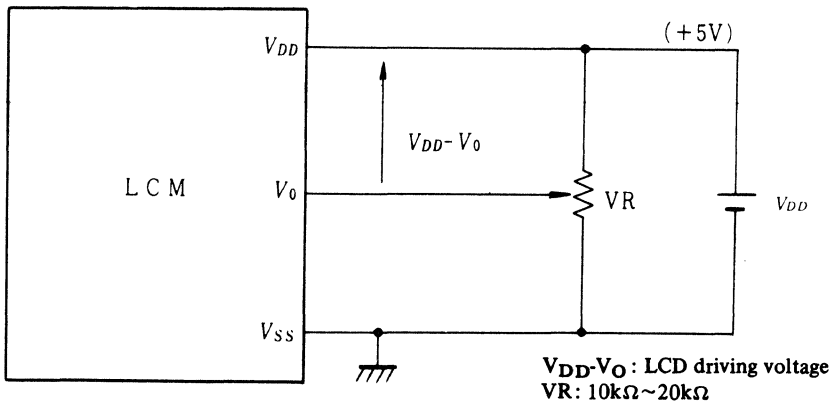


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{WEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

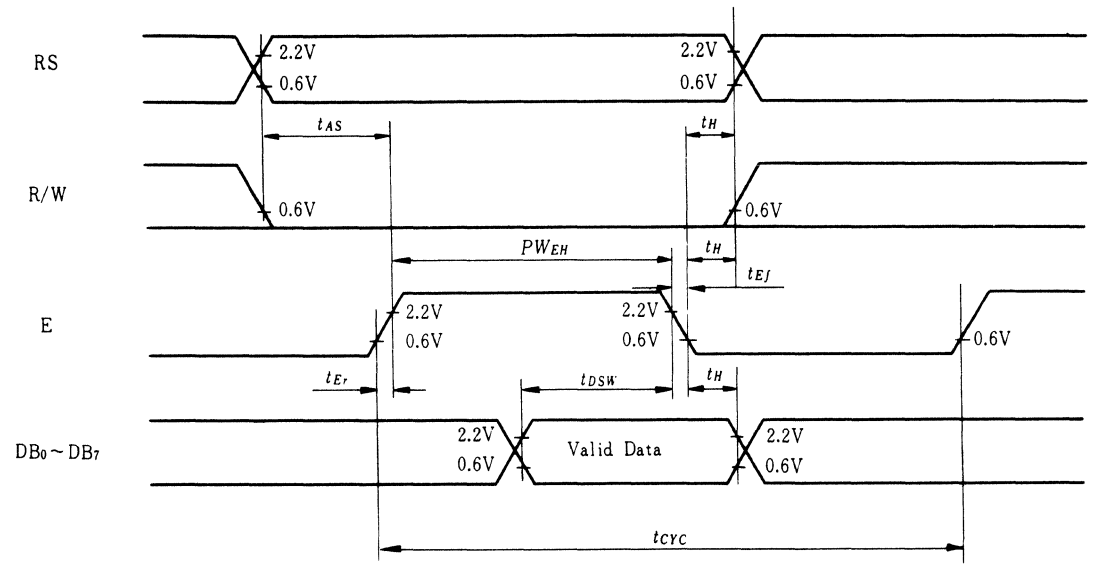


Fig. 5 Interface timing (data write)

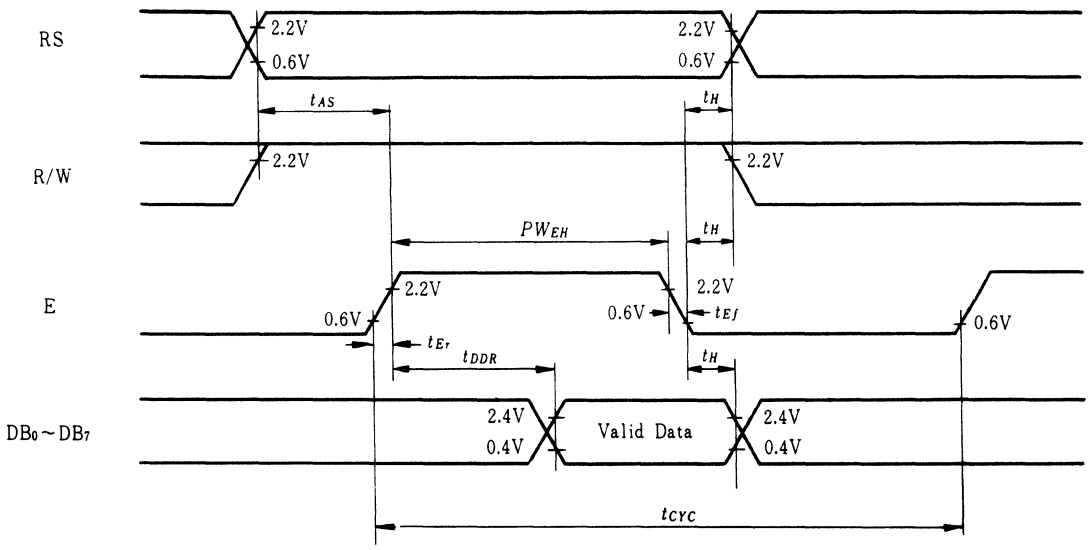


Fig. 6 Interface timing (data read)

LED BACKLIGHT CHARACTER LCD MODULES

LM087LN

FEATURES

- 16 character × 1 line w/LED backlighting
- Built-in controller LSI HD44780 type (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size .....90.0W × 36H × 14D (max.) mm
Effective display area.....64.5W × 13.8H mm
Character size (5 × 7 dots).....3.07W × 5.73H mm
Pitch.....3.77 mm
Dot size .....0.55W × 0.75H mm
Weight .....about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_O$)	0	13.5 V
Power supply for LED		60mA
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	-20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V
Input "high" voltage (V_{IH}) .....2.2 V min.
Input "low" voltage (V_{IL}) .....0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2mA).....2.4 V min.
Output low voltage (V_{OL}) ($-I_{OL}$ = 1.2mA).....0.4 V max.
Power supply current (I_{DD}) (V_{DD} = 5.0 V).....1.0 mA typ.
3.0 mA max.
Power supply LED (V_{LED} = 5.0 V).....30 mA typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_O$)
Du = 1/16
Ta = 0°C .....4.6 V typ.
Ta = 25°C .....4.4 V typ.
Ta = 50°C .....4.2 V typ.

OPTICAL DATA.....See page 15

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L : Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L : Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V_{LED}	—	+5V	Power supply

Note:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

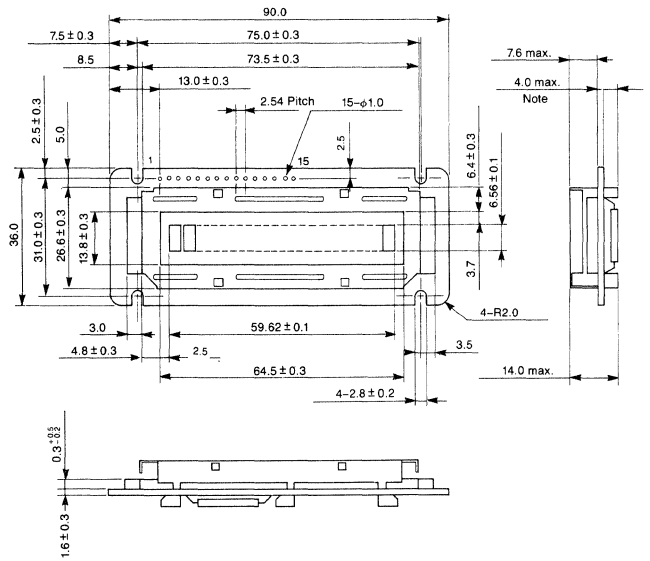


Fig. 1 External dimension

HITACHI

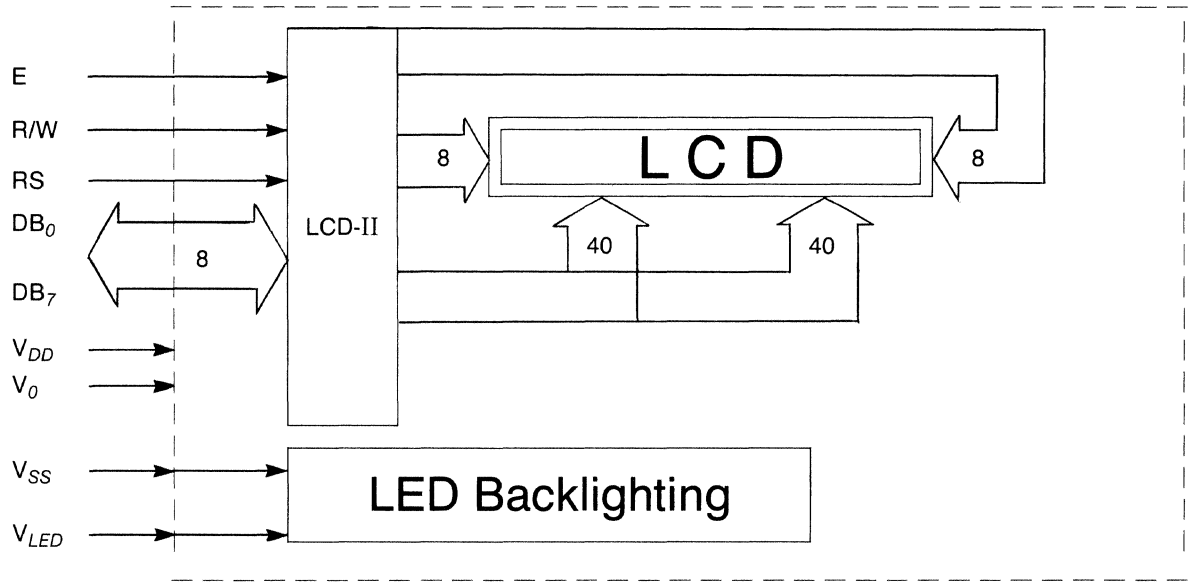


Fig. 2 Block diagram

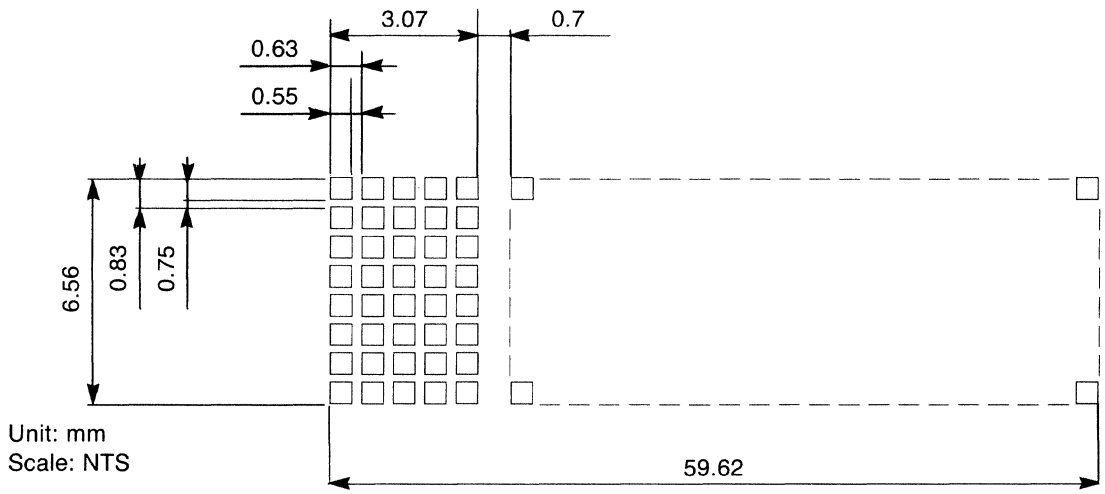


Fig. 3 Display pattern

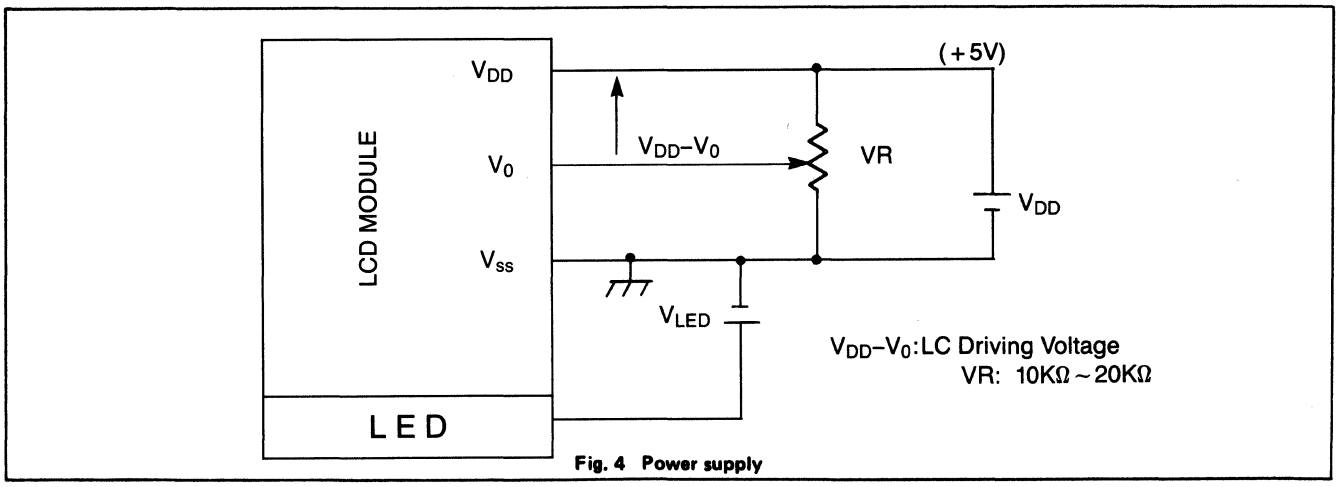


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	min.	typ.	max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

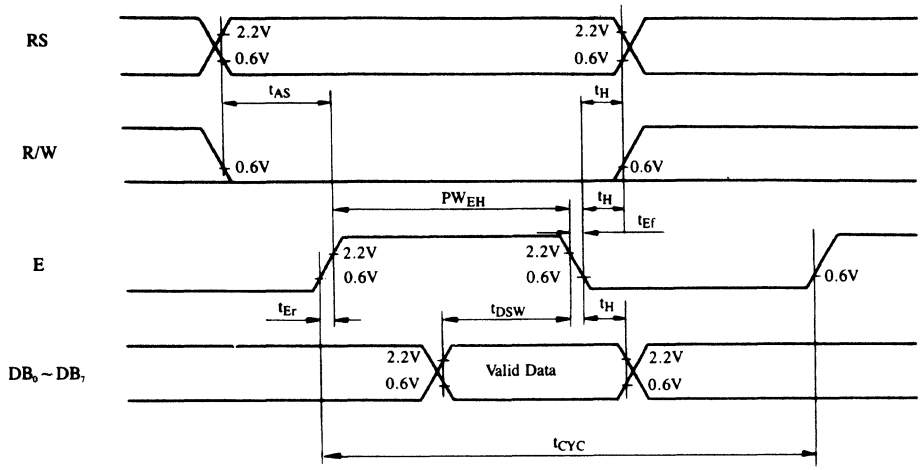


Fig. 5 Interface timing (data write)

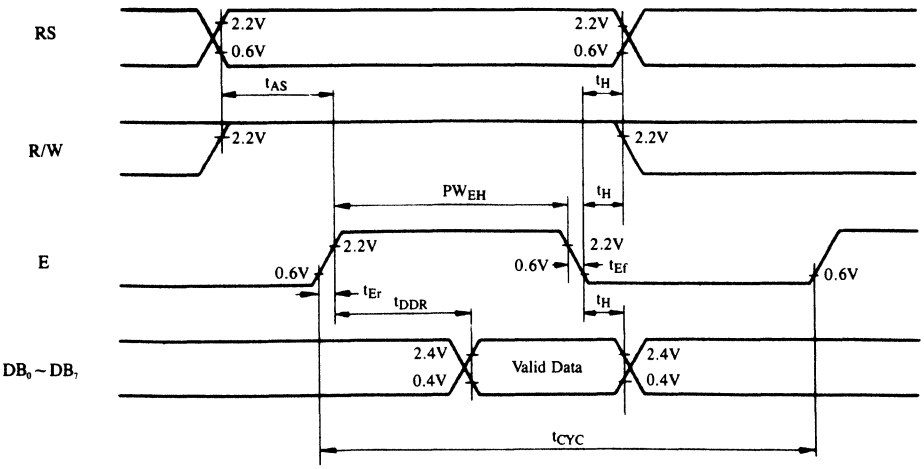


Fig. 6 Interface timing (data read)

LM086LN

FEATURES

- 16 character × 2 lines w/LED backlighting
- Built-in controller LSI HD44780 type (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 90W × 36H × 14D (max.) mm
Effective display area . . . . . 64.5W × 13.8H mm
Character size (5 × 10 dots) . . . . . 2.95W × 3.8H mm
Pitch . . . . . 3.65 mm
Dot size . . . . . 0.55W × 0.5H mm
Weight . . . . . about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_O$)	0	13.5 V
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	–20	70°C

ELECTRICAL CHARACTERISTICS

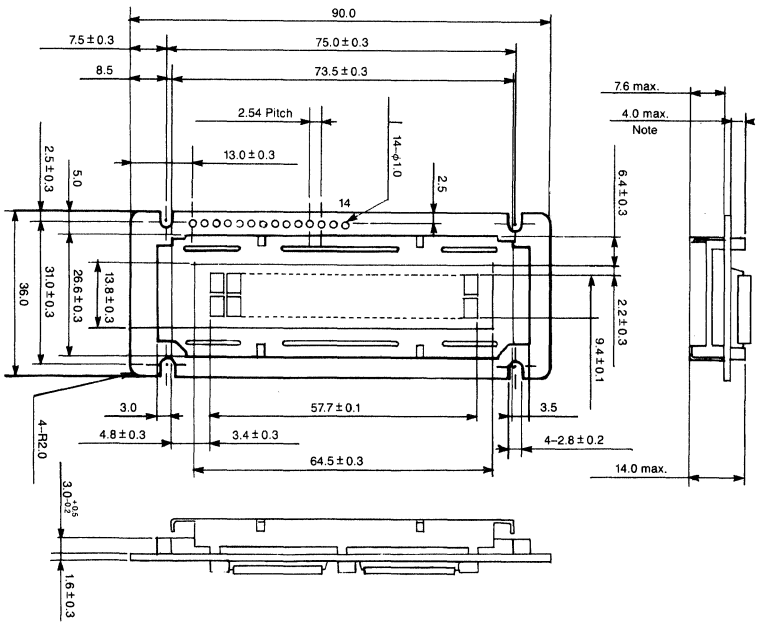
Ta = 25°C, V_{DD} = 5.0 V ±0.25 V
Input "high" voltage (V_{IH}) . . . . . 2.2 V min.
Input "low" voltage (V_{IL}) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2mA) . . . . . 2.4 V min.
Output low voltage (V_{OL}) ($-I_{OL}$ = 1.2mA) . . . . . 0.4 V max.
Power supply current (V_{DD} = 5.0 V) . . . . . 30 mA typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_O$)
Du = 1/16
Ta = 0°C . . . . . 4.6 V typ.
Ta = 25°C . . . . . 4.4 V typ.
Ta = 50°C . . . . . 4.2 V typ.

OPTICAL DATA . . . . . See page 15.

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	–	0V	Power supply
2	V_{DD}	–	+5V	
3	V_O	–	–	
4	RS	H/L	L: Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L: Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		

Note:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.



Unit: mm
Scale: NTS

Fig. 1 External dimension

HITACHI

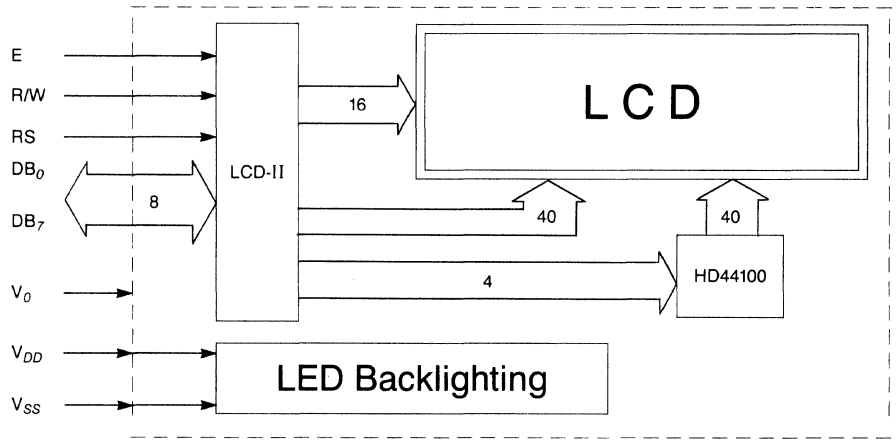
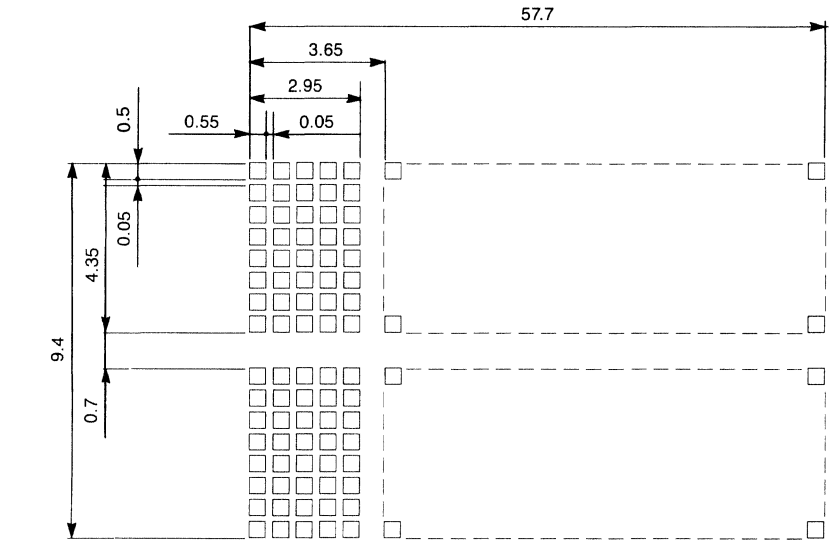


Fig. 2 Block diagram



Unit: mm
Scale: NTS

Fig. 3 Display pattern

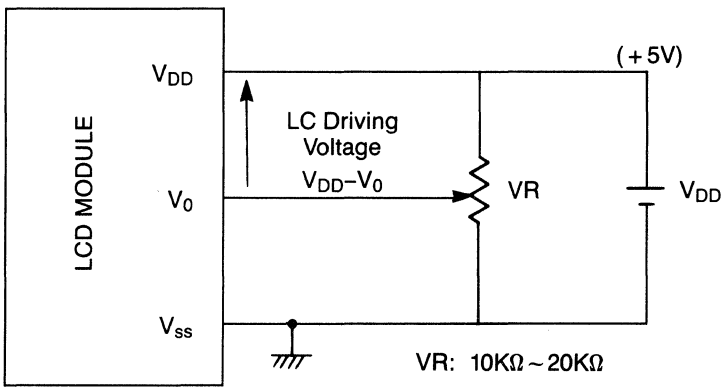


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	min.	typ.	max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

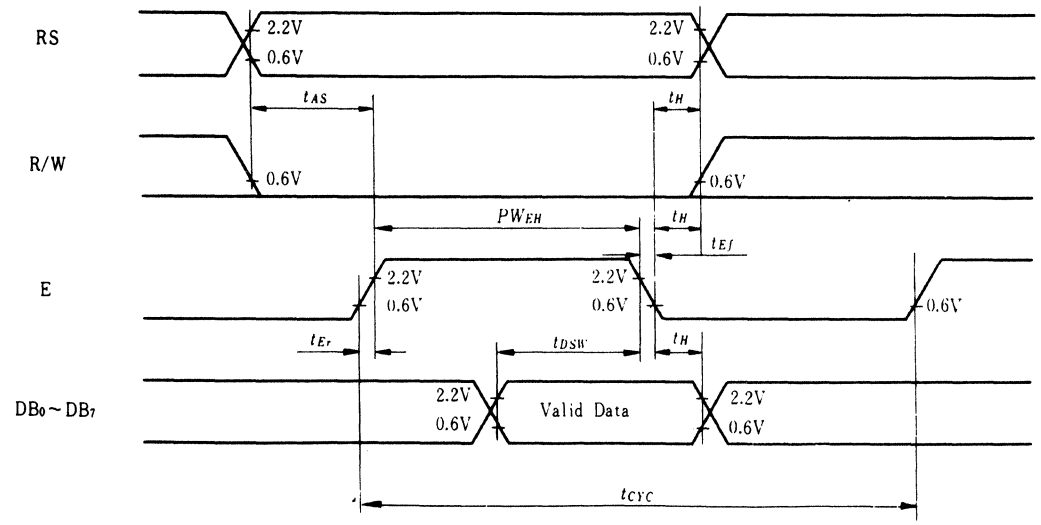


Fig. 5 Interface timing (data write)

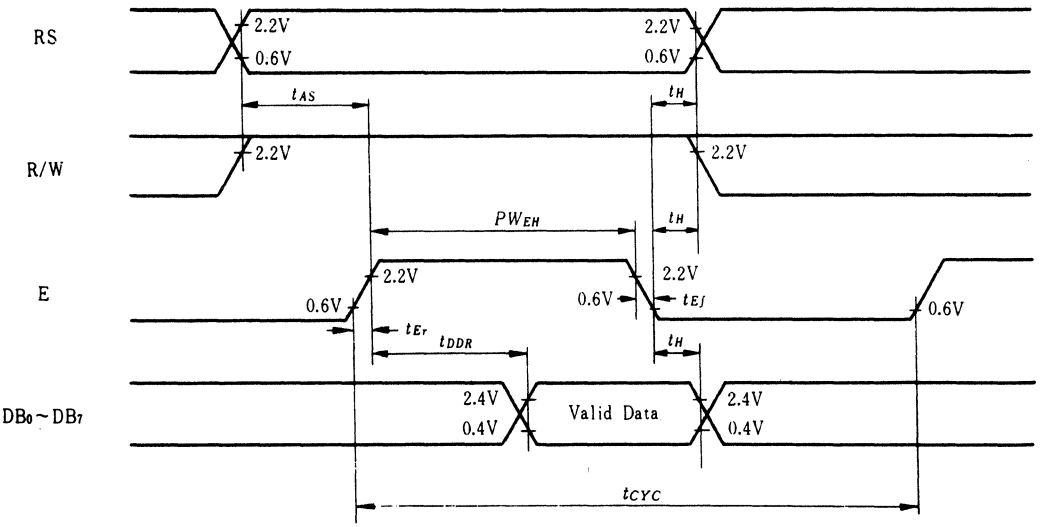


Fig. 6 Interface timing (data read)

LM093LN

SUMMARY

- 16 character × 2 lines w/LED backlighting
- Built-in controller LSI HD44780 type (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size .....90W × 44H × 13.8D (max.) mm
Effective display area .....61W × 16.3H mm
Character size (5 × 7 dots) .....2.96W × 4.86H mm
Pitch .....3.55 mm
Dot size .....0.56W × 0.66H mm
Weight .....about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_O$)	0	13.5 V
Power supply for LED		160mA
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

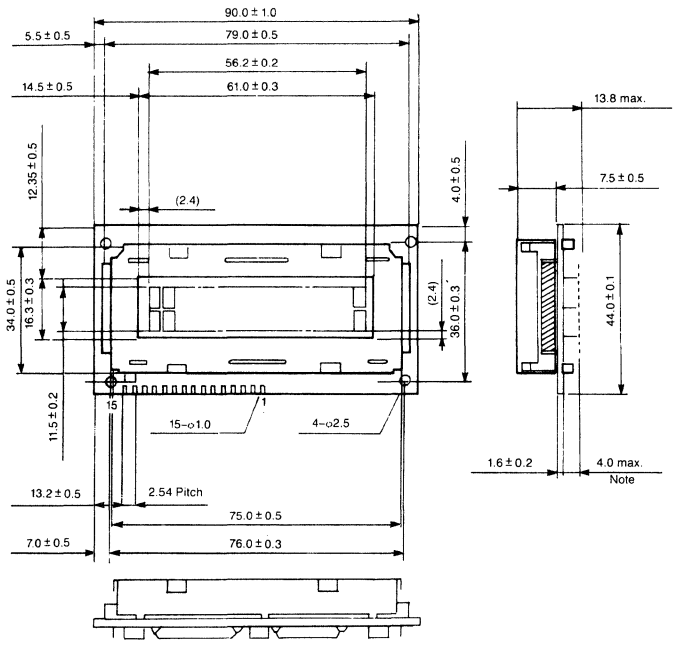
Ta = 25°C, V_{DD} = 5.0 V ±0.25 V
Input "high" voltage (V_{IH}) .....2.2 V min.
Input "low" voltage (V_{IL}) .....0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2mA) .....2.4 V min.
Output low voltage (V_{OL}) ($-I_{OL}$ = 1.2mA) .....0.4 V max.
3.0 mA max.
Power supply LED (V_{LED} = 5.0 V) .....80 mA typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_O$)
Du = 1/16
Ta = 0°C .....4.6 V typ.
Ta = 25°C .....4.4 V typ.
Ta = 50°C .....4.2 V typ.

OPTICAL DATA .....See page 15

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L : Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L : Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V_{LED}	—	+5V	Power supply

Note:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.



Unit: mm
Scale: NTS

Fig. 1 External dimension

SECTION 5

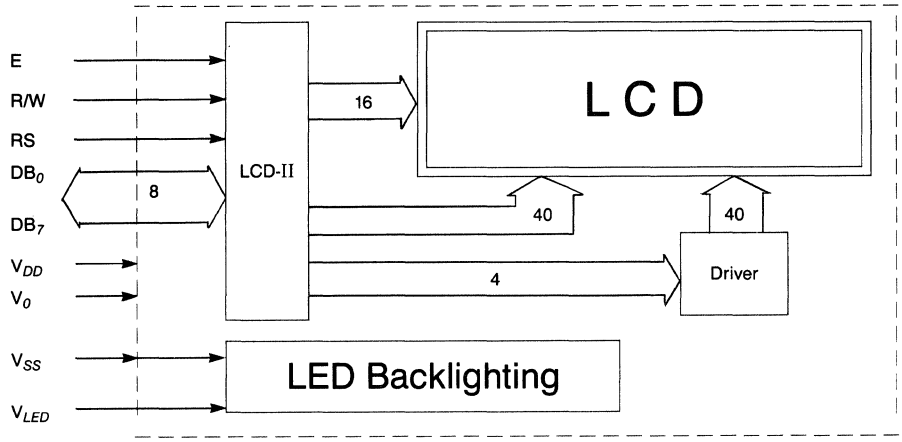


Fig. 2 Block diagram

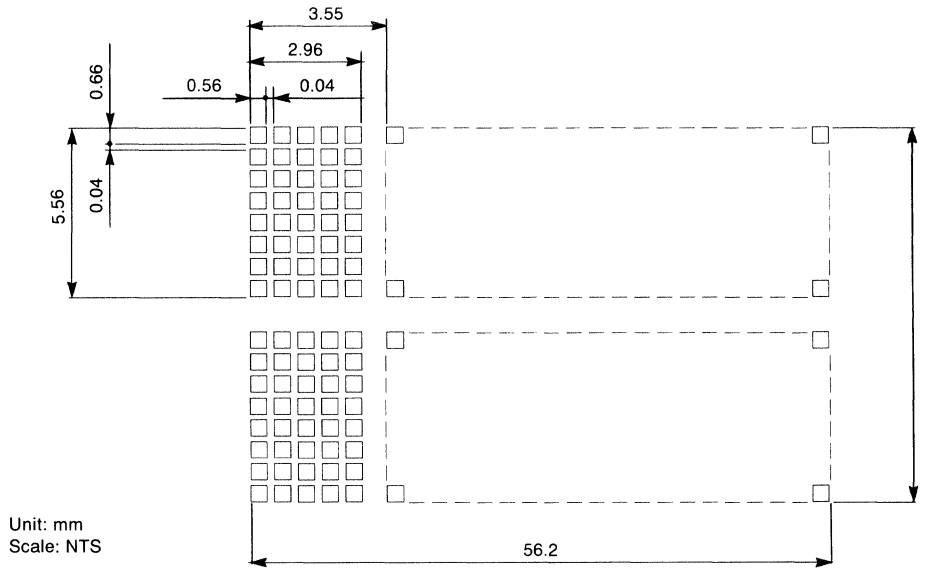


Fig. 3 Display pattern

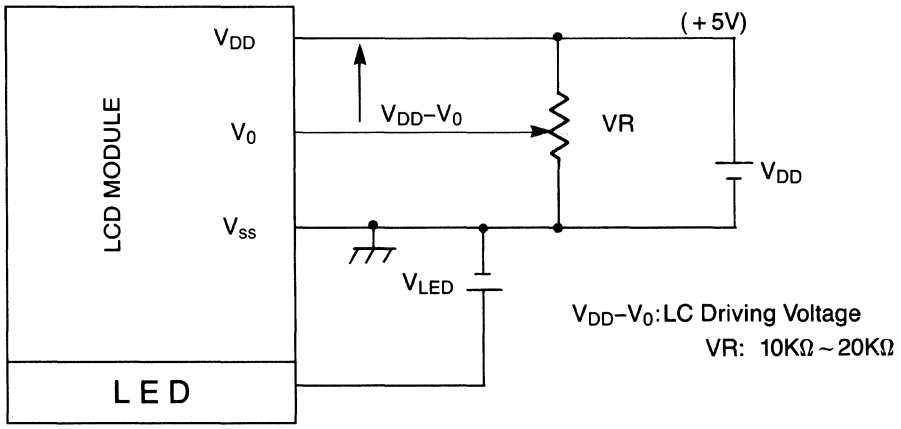


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	min.	typ.	max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

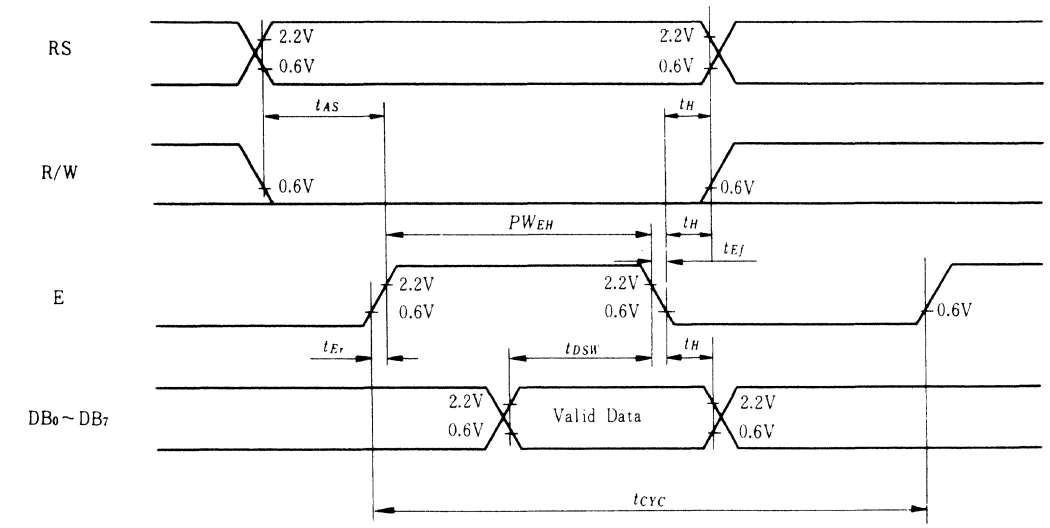


Fig. 5 Interface timing (data write)

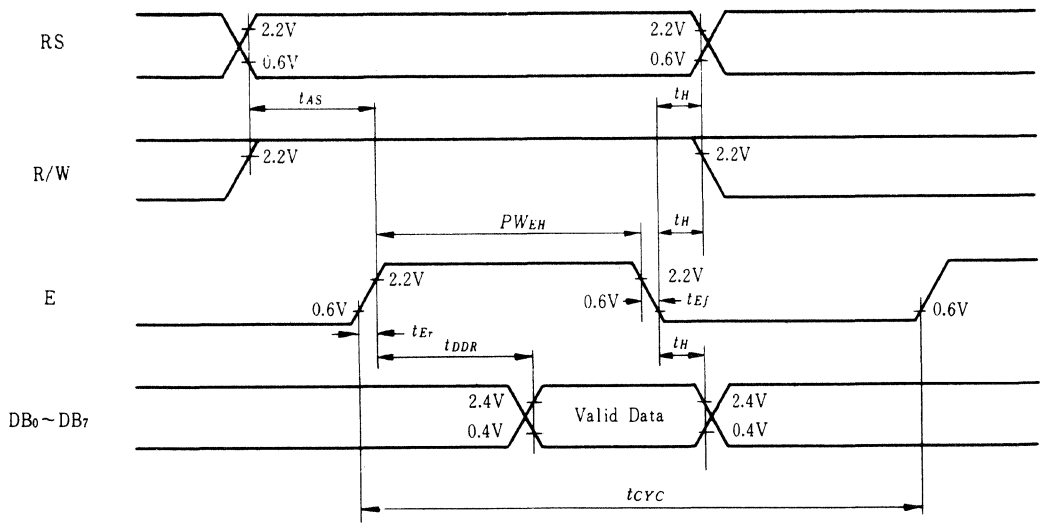


Fig. 6 Interface timing (data read)

LM091LN

SUMMARY

- 20 character × 2 lines w/LED backlighting
- Built-in controller LSI HD44780 type (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 126W × 39H × 14D (max.) mm
Effective display area . . . . . 83W × 18.6H mm
Character size (5 × 7 dots) . . . . . 3.2W × 4.85H mm
Pitch . . . . . 3.7 mm
Dot size . . . . . 0.6W × 0.65H mm
Weight . . . . . about 25 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD} - V_{SS}$)	0	7.0 V
Power supply for LCD drive ($V_{DD} - V_O$)	0	13.5 V
Power supply for LED		220mA
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V
Input "high" voltage (V_{IH}) . . . . . 2.2 V min.
Input "low" voltage (V_{IL}) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2mA) . . . . . 2.4 V min.
Output low voltage (V_{OL}) ($-I_{OL}$ = 1.2mA) . . . . . 0.4 V max.
3.0 mA max.
Power supply LED (V_{LED} = 5.0 V) . . . . . 110 mA typ.
Power supply for LCD drive (Recommended) ($V_{DD} - V_O$)
Du = 1/16
Ta = 0°C . . . . . 4.6 V typ.
Ta = 25°C . . . . . 4.2 V typ.
Ta = 50°C . . . . . 3.5 V typ.

OPTICAL DATA . . . . . See page 15

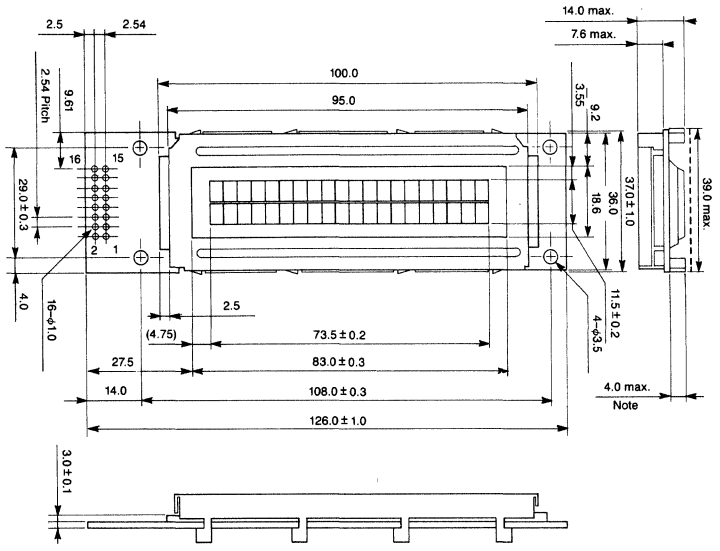
INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L : Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L : Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V_{LED}	—	+5V	Power supply
16	N.C.	—	—	

Note:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).

(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.



Unit: mm

Fig. 1 External dimension

HITACHI

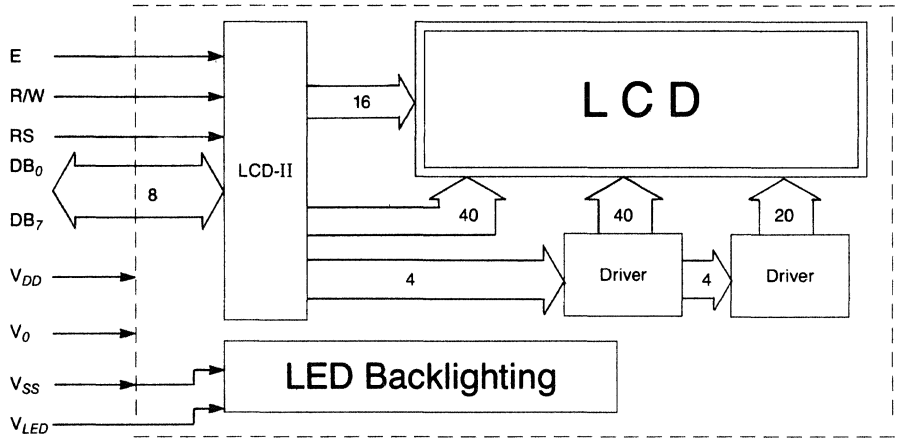
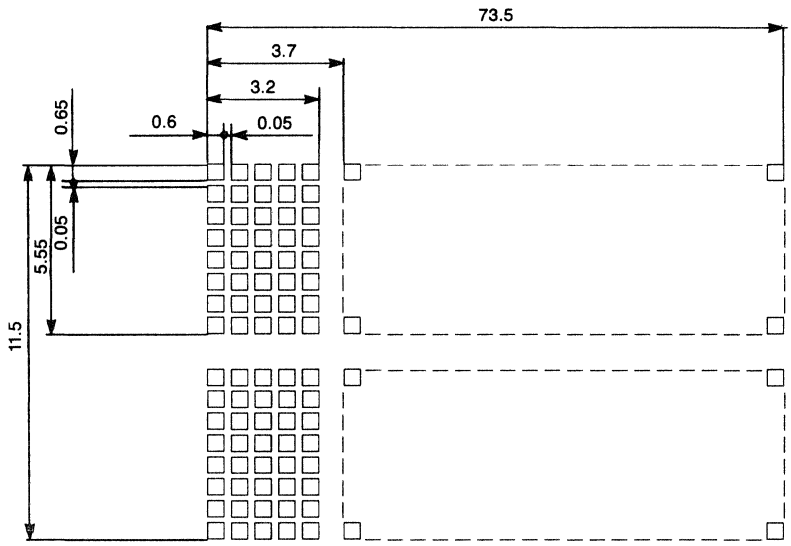


Fig. 2 Block diagram



Unit: mm
Scale: NTS

Fig. 3 Display pattern

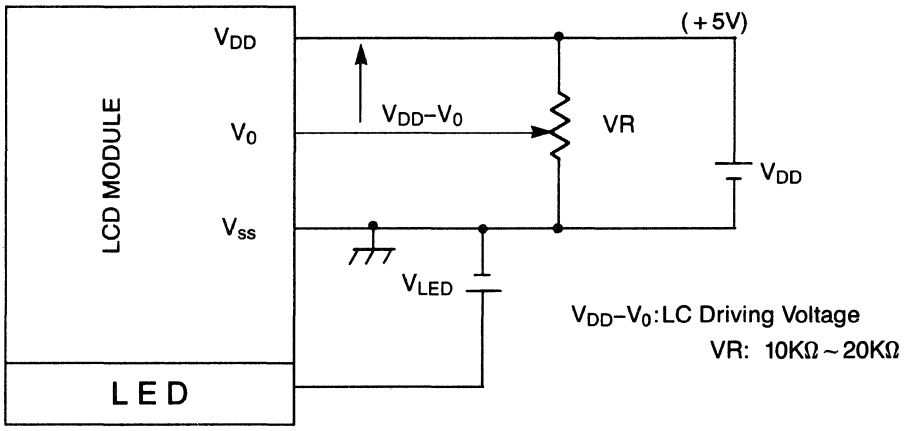


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	min.	typ.	max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

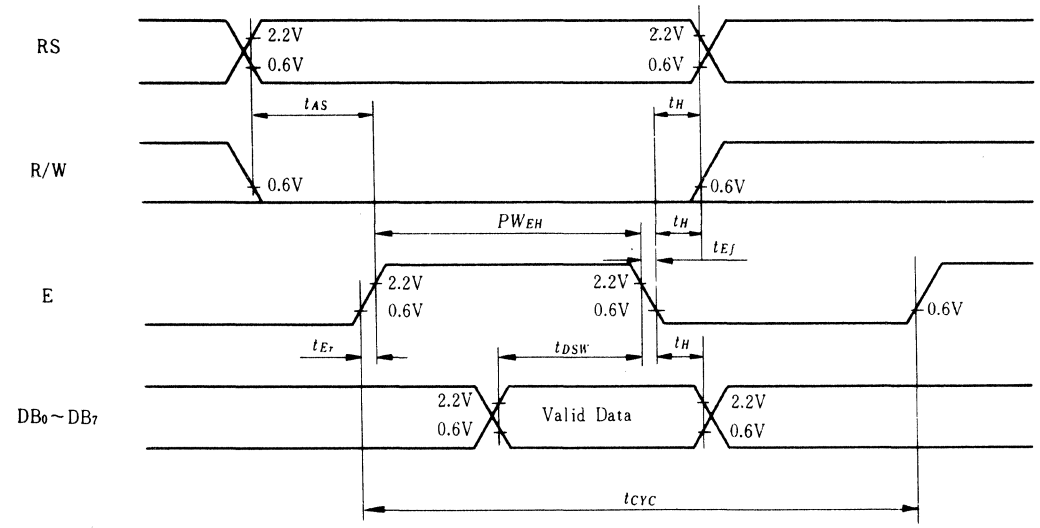


Fig. 5 Interface timing (data write)

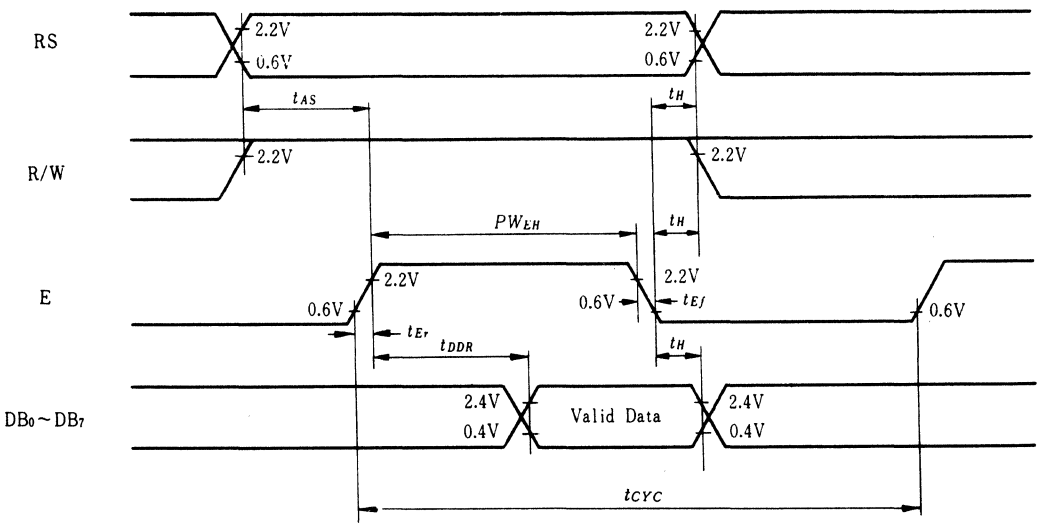


Fig. 6 Interface timing (data read)

LM092LN

SUMMARY

- 40 character × 2 lines w/LED backlighting
- Built-in controller LSI HD44780 type (see section 6).
- +5V single power supply

MECHANICAL DATA (Nominal dimensions)

Module size . . . . . 192W × 35.5H × 15.5D (max.) mm
Effective display area . . . . . 154W × 15.3H mm
Character size (5 × 7 dots) . . . . . 3.2W × 4.85H mm
Pitch . . . . . 3.7 mm
Dot size . . . . . 0.6W × 0.65H mm
Weight . . . . . about 65 g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic (V_{DD} – V_{SS})	0	7.0 V
Power supply for LCD drive (V_{DD} – V_O)	0	13.5 V
Power supply for LED		340mA
Input voltage (Vi)	V_{SS}	V_{DD} V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	–20	70°C

ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5.0 V ±0.25 V
Input "high" voltage (V_{IH}) . . . . . 2.2 V min.
Input "low" voltage (V_{IL}) . . . . . 0.6 V max.
Output high voltage (V_{OH}) ($-I_{OH}$ = 0.2mA) . . . . . 2.4 V min.
Output low voltage (V_{OL}) ($-I_{OL}$ = 1.2mA) . . . . . 0.4 V max.
3.0 mA max.
Power supply LED (V_{LED} = 5.0 V) . . . . . 170 mA typ.
Power supply for LCD drive (Recommended) (V_{DD} – V_O)
Du = 1/16
Ta = 0°C . . . . . 4.6 V typ.
Ta = 25°C . . . . . 4.4 V typ.
Ta = 50°C . . . . . 4.2 V typ.

OPTICAL DATA . . . . . See page 15

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function	
1	V_{SS}	—	0V	Power supply
2	V_{DD}	—	+5V	
3	V_O	—	—	
4	RS	H/L	L : Instruction code input H: Data input	
5	R/W	H/L	H: Data read (LCD module→MPU) L : Data write (LCD module←MPU)	
6	E	H, H→L	Enable signal	
7	DB0	H/L	Data bus line Note (1), Note (2)	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V_{LED}	—	+5V	Power supply
16	N.C.	—	—	

Note:
In the HD44780, the data can be sent in either 4-bit 2-operation or 8-bit 1-operation so that it can interface to both 4 and 8 bit MPU's.
(1) When interface data is 4 bits long, data is transferred using only 4 buses of DB_4~DB_7 and DB_0~DB_3 are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of DB_4~DB_7 when interface data is 8 bits long) is transferred first and then lower order 4 bits (contents of DB_0~DB_3 when interface data is 8 bits long).
(2) When interface data is 8 bits long, data is transferred using 8 data buses of DB_0~DB_7.

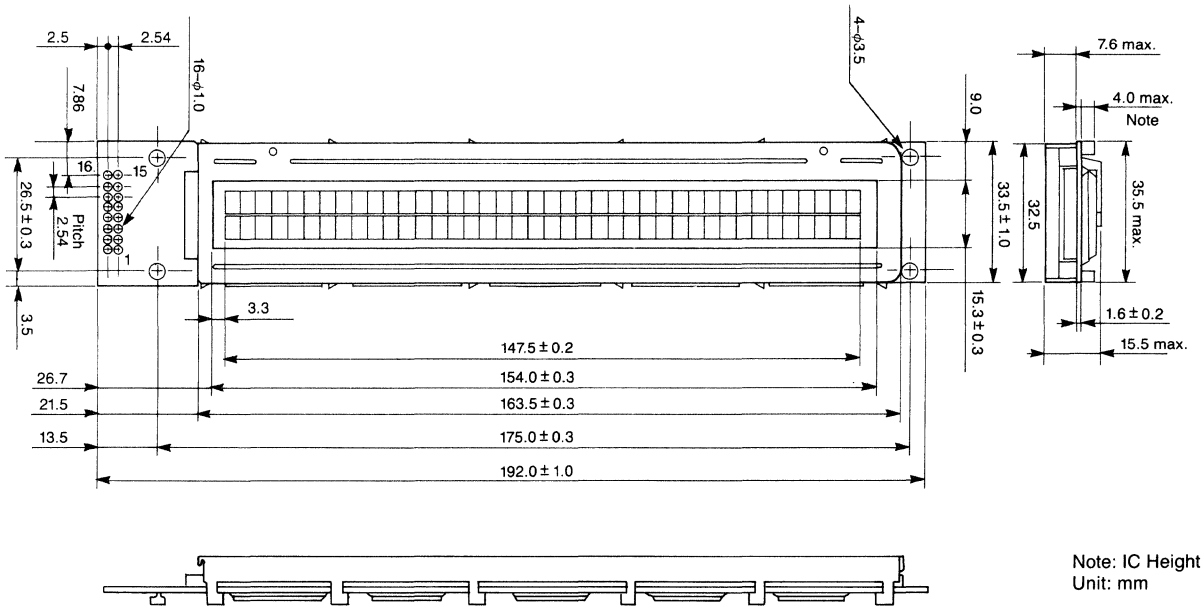


Fig. 1 External dimension

SECTION 5

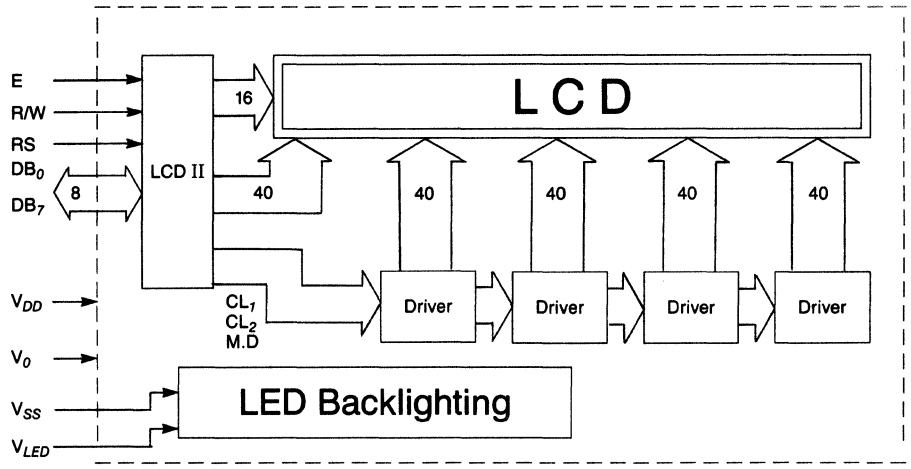


Fig. 2 Block diagram

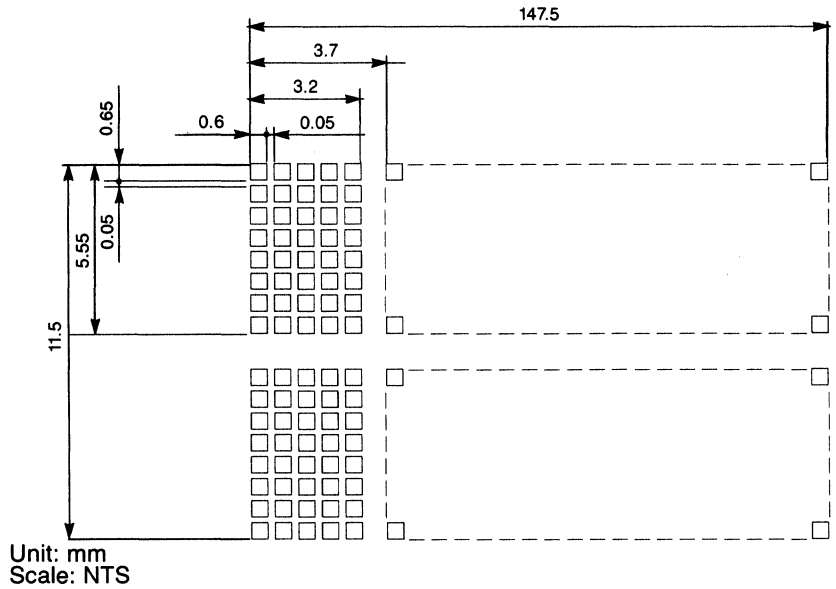


Fig. 3 Display pattern

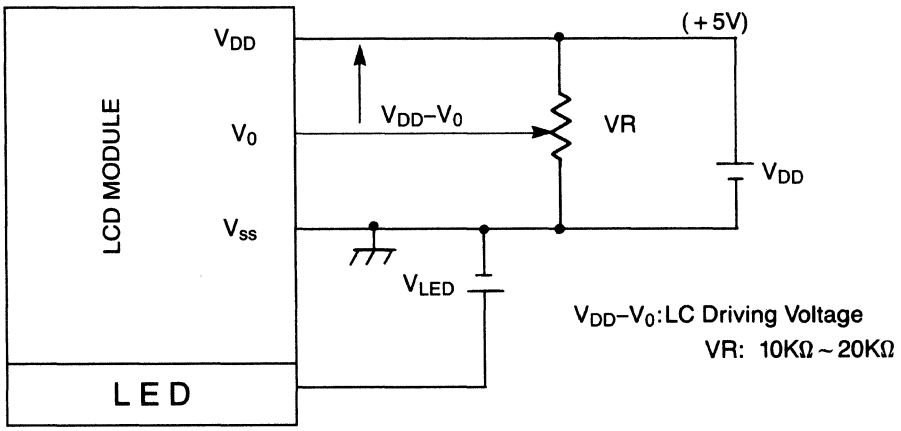


Fig. 4 Power supply

TIMING CHARACTERISTICS

Item	Symbol	Test condition	min.	typ.	max.	Unit
Enable cycle time	t_{cyc}	Fig. 5, Fig. 6	1.0	–	–	μs
Enable pulse width	P_{wEH}	Fig. 5, Fig. 6	450	–	–	ns
Enable rise/fall time	t_{Er}, t_{Ef}	Fig. 5, Fig. 6	–	–	25	ns
RS, R/W set up time	t_{AS}	Fig. 5, Fig. 6	140	–	–	ns
Data delay time	t_{DDR}	Fig. 6	–	–	320	ns
Data set up time	t_{DSW}	Fig. 5	195	–	–	ns
Hold time	t_H	Fig. 5, Fig. 6	20	–	–	ns

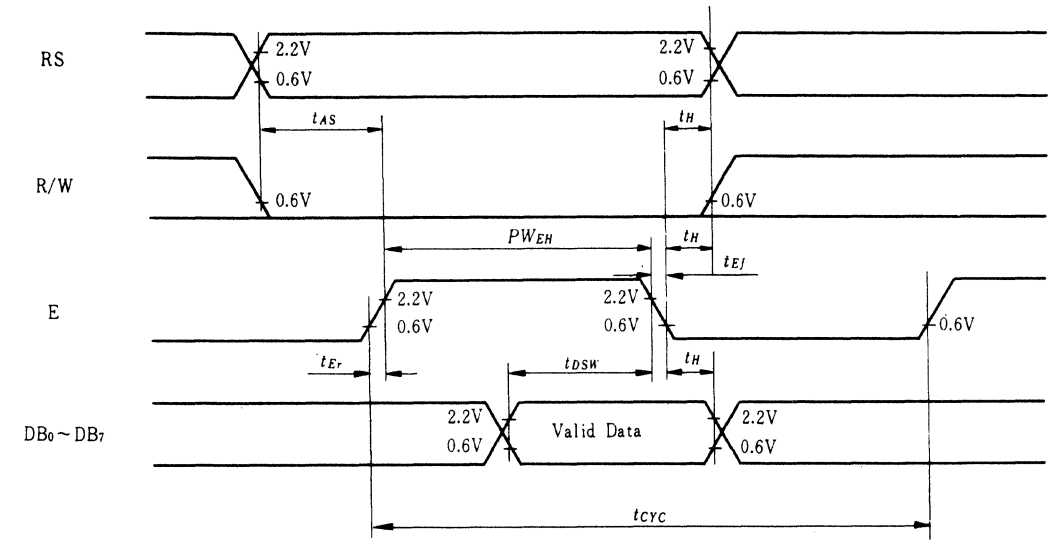


Fig. 5 Interface timing (data write)

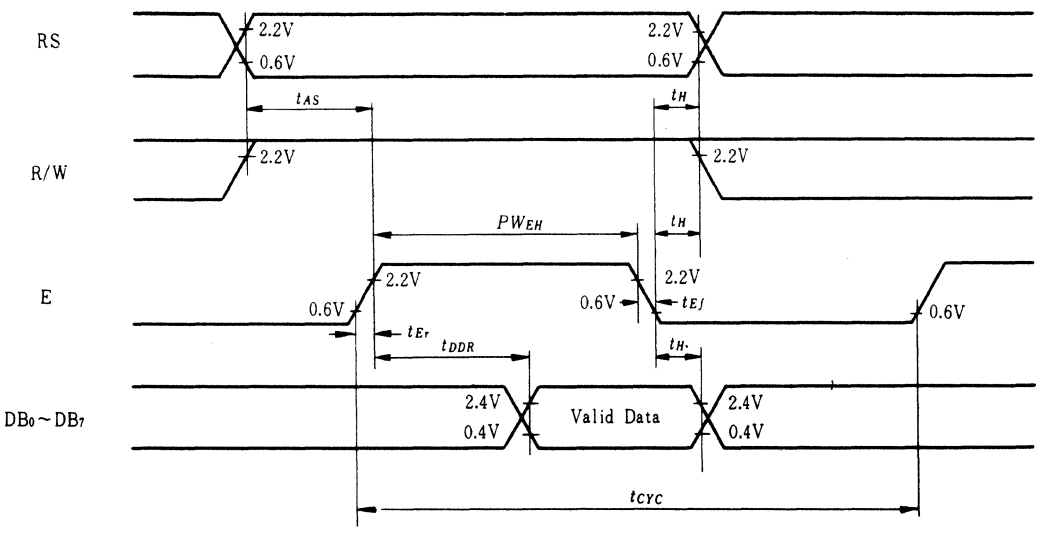


Fig. 6 Interface timing (data read)

CONTROLLER APPLICATION NOTES 6

APPENDIX

- **HD44780 Controller Data for Hitachi Character LCM's**
- **CB1020R • CB1026R • CB1030R • CB1040R • Hitachi Graphics LCM Controller Card including HD61830 • HD61830B**

HOW TO USE HITACHI'S BUILT-IN CONTROLLER DRIVER LCD-II (HD44780) DOT MATRIX LCD MODULE

■ INTRODUCTION

The LCD-II (HD44780) is a dot matrix liquid crystal display controller & driver LSI that displays alphanumerics, kana characters and symbols. It drives dot matrix liquid crystal display under 4-bit or 8-bit microcomputer or microprocessor control. All the functions required for dot matrix liquid crystal display drive are internally provided on one chip.

The user can complete dot matrix liquid crystal display systems with less number of chips by using the LCD-II (HD44780). If a driver LSI HD44100H is externally connected to the HD44780, up to 80 characters can be displayed.

The LCD-II is produced in the CMOS process. Therefore, the combination of the LCD-II with a CMOS microcomputer or microprocessor can accomplish a portable battery-drive device with lower power dissipation.

■ FEATURES

- Capable of interfacing to 4-bit or 8-bit MPU.
- Display data RAM . . . . . 80 x 8 bits (80 characters, max.)
- Character generator ROM . . . .
  Character font 5 x 7 dots: 160 characters
  Character font 5 x 10 dots: 32 characters
- Both display data and character generator RAMs can be read from the MPU.
- Wide range of instruction functions
  Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Display character blink, Cursor shift, Display shift
- Internal automatic reset circuit at power ON. (Internal reset circuit)

1. Applicable type

(1) 1 line series
LM054 • H2570 • LM015 • LM568AF • LM020L • LM070L • LM038 • LM027 • H2571 • LM058

(2) 2 line series
LM052L • LM016L • LM032L • LM060L • LM017L • LM018L • LM075L • LM074L • LM068L • LM061L

(3) 4 lines series
LM041L • LM044L

(4) Compact version
LM104L • LM105L • LM107L

2. Connecting MPU with LCM

2.1 Driver circuit block diagram

Figure 1 shows the driver circuit block diagram of LCM with built-in controller LSI. Controller LSI HD44780 (LCD-II) is built-in this LCM. Also extended LCD driver LSI is built in the LCM that displays more than 16 digits.

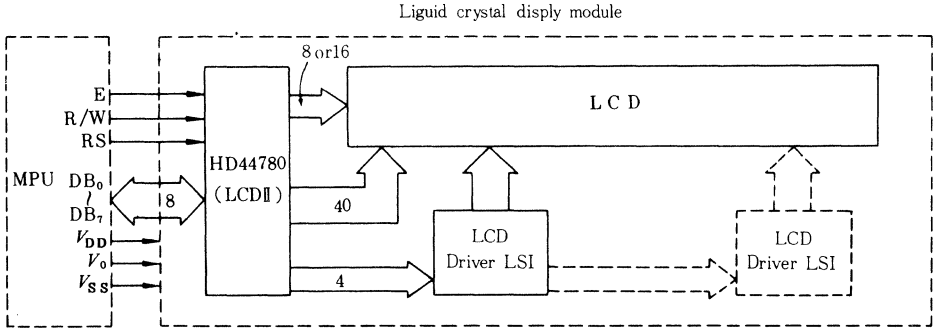


Fig. 1 Driver circuit block diagram

2.2 Interfacing to MPU

In the HD44780, data can be sent in either 4-bit 2-operation or 8-bit 1-operation so it can interface to both 4 and 8 bit MPU's.

(1) When interface data is 4-bits long, data is transferred using only 4 buses: $DB_4 \sim DB_7$. $DB_0 \sim DB_3$ are not used. Data transfer between the HD44780 and the MPU completes when 4-bit data is transferred twice. Data of the higher order 4 bits (contents of $DB_4 \sim DB_7$ when interface data is 8 bits long) is transferred first, then the lower order 4 bits (content of $DB_0 \sim DB_3$ when interface data is 8 bits long) is transferred. Check the busy flag after 4-bit data has been transferred twice (one instruction). A 4-bit 2-operation will then transfer the busy flag and address counter data.

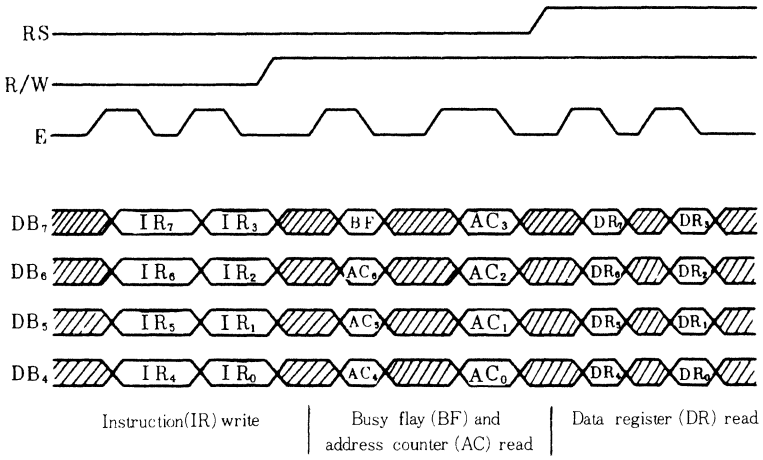


Fig. 2 4-bit data transfer example

(2) When interface data is 8 bit long, data is transferred using the 8 data buses of $DB_0 \sim DB_7$.

2.3 Interface to MPU

(1) Interface to 8-bit MPU

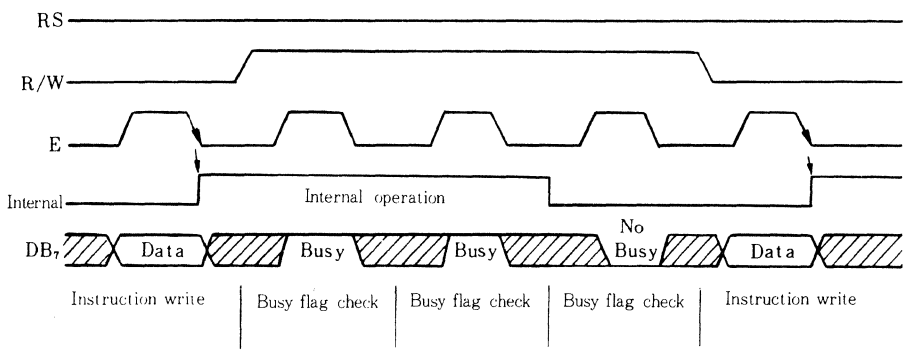


Fig. 3 Example of busy flag check timing sequence

(1) When connecting to 8-bit MPU through PIA

Fig. 4 is an example of using a PIA or I/O port (for single chip microcomputer) as an interface device. Input and output of the device is TTL compatible.

In the example, PB_0 to PB_7 are connected to the data buses DB_0 to DB_7 and PA_0 to PA_2 are connected to E, R/W and RS respectively. Pay attention to the timing relation between E and other signals when reading or writing data and using PIA as an interface.

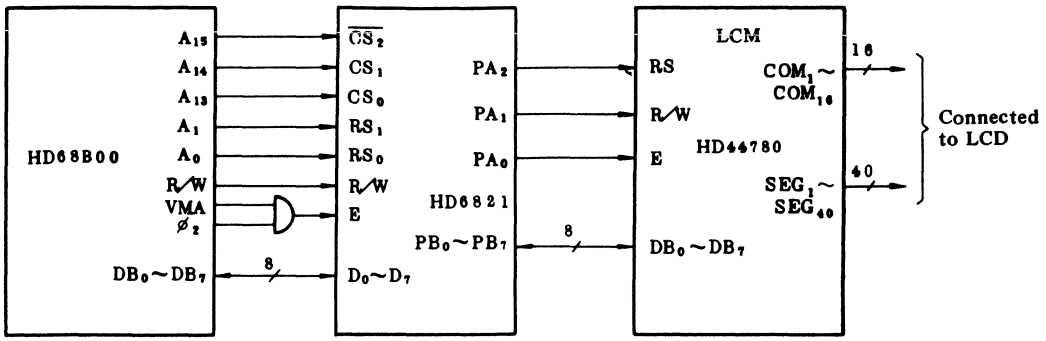
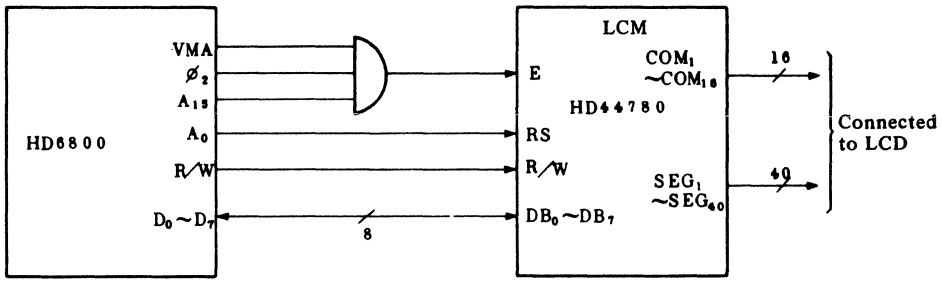
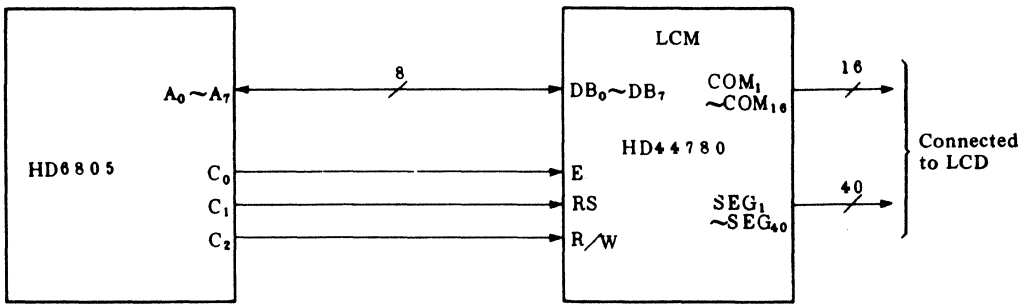


Fig. 4 Example of interface to HD68B00 using PIA (HD68B21)

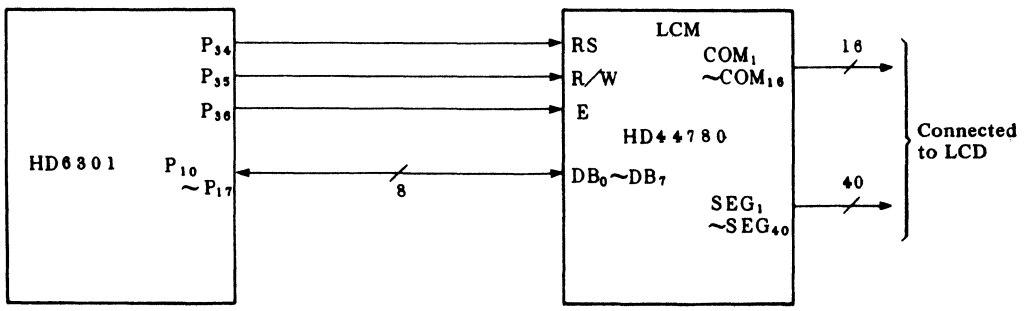
② Connecting directly to the 8 bit MPU bus line



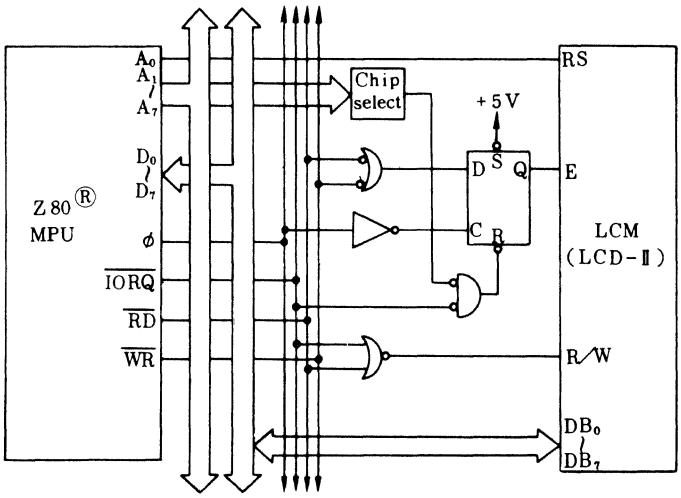
③ Example of interfacing to the HD6805



④ Example of interfacing to the HD6301



⑤ Example of interfacing to Z80 MPU



Note: 280 is the trademark of ZILOG, U.S.A.

(a) Above circuit is an example of connection with Z80 MPU and HD44780A00 as an I/O equipment. It can be used as a part of memories by using MREQ signal.

(b) A0 signal can be used for RS signal.
A0 = 0: Instruction register is selected.
A0 = 1: Data register is selected.

(c) In order to check busy flag, transfer the data of $DB_0 \sim DB_7$ to A register (accumulator) by executing In/Out instruction. After that, busy flag can be easily checked by examining DB_7.

⑥ Example of interfacing to 80 CPU family

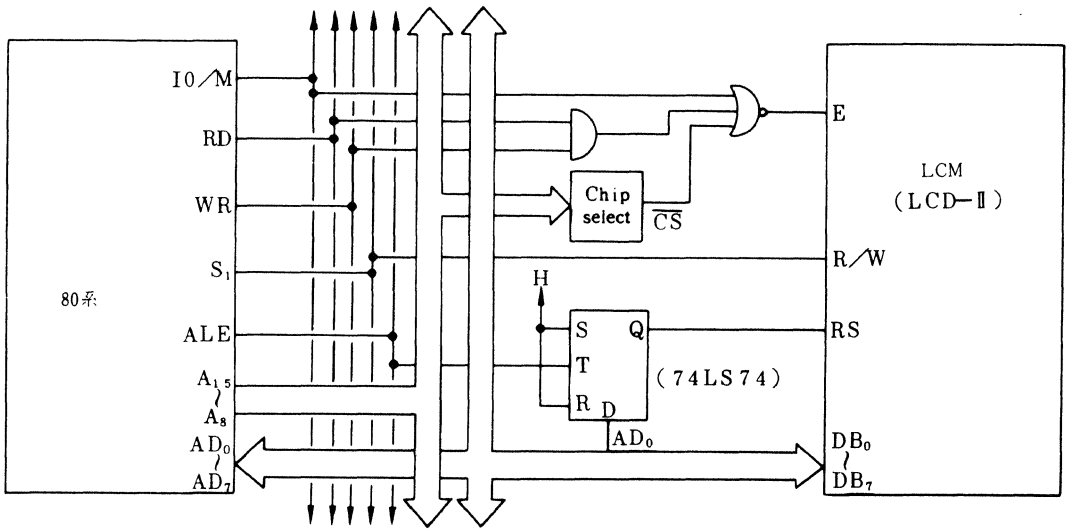


Fig. 5 Example of connection with LCM being used as a part of memories on the determined address.

Figure 5 is an example of connection with LCD module being used as a part of memories on the determined address.

Generates RS signal (Register Select signal) by latching the content of AD_0 at the rising edge of ALE signal. By using this method, you can obtain RS signal from the AD_0 among 8 bit addresses generated at the clock of the first machine cycle. In case of using LCD module as an I/O equipment, chip select signal is necessarily activated when IO/M signal is "High" level.

Furthermore, by using A8 for RS signal, the interface is easily realized.

By both methods, busy flag can be checked by storing status data into A register (Accumulator) and examining the bit 7 by software.

(2) Interface to 4-bit MPU

The HD44780 can be connected to a 4-bit MPU through the 4-bit MPU I/O port. If the I/O port has enough bits, data can be transferred in 8-bit lengths, but if the bits are insufficient, the transfer is made in two operations of 4 bits each (with designation of interface data length for 4 bits). In the latter case, the timing sequence becomes somewhat complex. (See Fig. 6)

Fig. 7 shows an example of interface to the HMCS43C. Note that 2 cycles are needed for the busy flag check as well as the data transfer. 4-bit operation is selected by program.

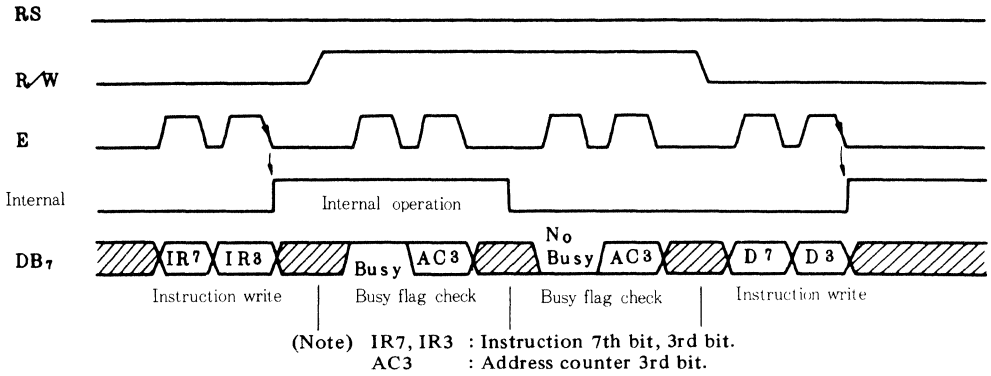


Fig. 6 An example of 4 bit data transfer timing sequence

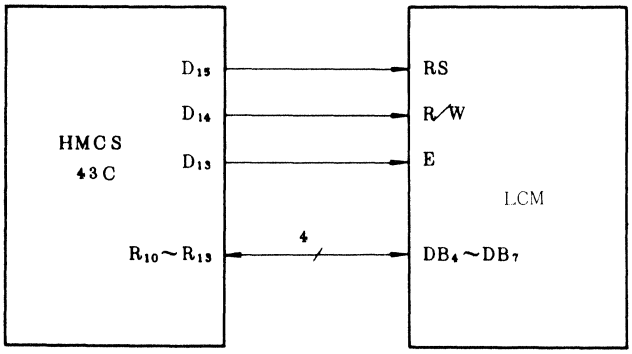


Fig. 7 Example of interface to the HMCS43C

3. Precautions on constituting hardwares

3.1 Chip select

HD44780 has no CS (chip select) terminals. Therefore, when this LSI is connected directly to Data Bus line not through PIA and so on, add the circuit that inhibits the output of Enable signal at the address which is not assigned for HD44780.

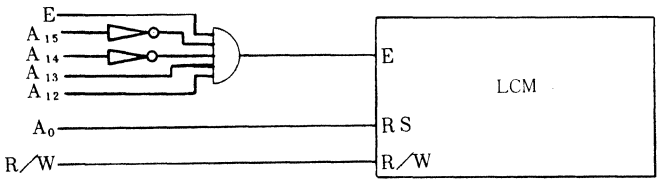


Fig. 8 Example of addresses $(3000)_{16}$ ~ $(3FFF)_{16}$ being assigned for HD44780

3.2 Ability of driving bus line

DB_0 to DB_7 can drive one TTL or capacitance of 130 pF.

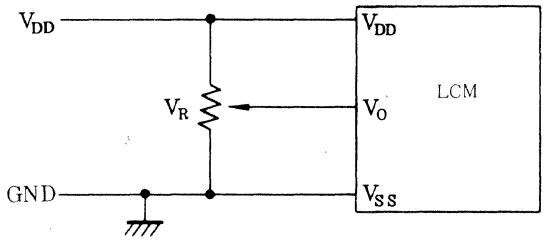
The data bus terminals have three-state constructions and remain in high impedance state while Enable signal being low level.

Since the data bus has pull up MOS, it outputs high level voltage during the data bus being opened.

3.3 Power supply voltage for liquid crystal display drive

At Interface of liquid crystal display module, there are three power supply terminals, V_{DD}, GND, and V_0. LCD module is driven by the voltage that is equal to $V_{DD} - V_0$, when supplying power for liquid crystal display drive to V_0 terminal. Since suitable voltage of power supply for LCD shifts according to temperature change adjust supplying power to LCD by referring to Fig. 9 or Fig. 10.

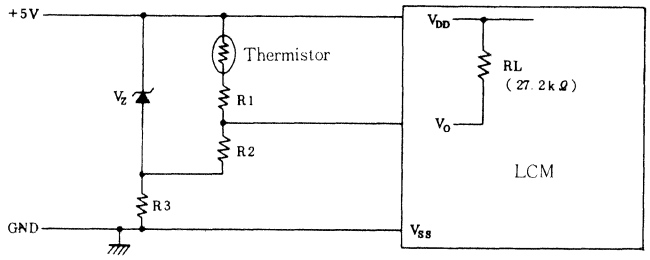
(1) Example of variable driving voltage by a variable resistance (VR)
The driving voltage can be changed by VR to compensate the influence of surrounding temperature.



Recommended V_R value = 10kΩ ~ 20kΩ

Fig. 9 Variable driving voltage circuit

(2) Example of a thermal compensator circuit
When setting the voltage, refer to Table-1



Thermistor { RT = 15kΩ (Ta = 25°C), B = 4300

Fig. 10 Example of a thermal compensator circuit

Table 1

Duty	Recommended driving voltage		Typical circuit parameter			
	Ta (°C)	$V_{DD} - V_O$ (V)	V_Z (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)
1 / 8	0	4.0	4.5	2.2	2.8	1.0
	25	3.7				
	50	3.3				
1 / 11	0	4.3	4.5	2.2	3.2	0.3
	25	3.9				
	50	3.3				
1 / 16	0	4.6	5.0	0.1	1.3	0.1
	25	4.4				
	50	4.2				

4. Initialization

4.1 Initializing by internal reset circuit

The HD44780 automatically initializes (resets) when power is turned on using the internal reset circuit. The following instructions are executed in initialization. The busy flag (BF) is kept in busy state until initialization ends. (BF = 1) The busy state is 10 ms after V_{CC} rises to 4.5 V.

(1) Display clear
(2) Function set ..... DL = 1 : 8 bit long interface data
N = 0 : 1-line display
F = 0 : 5 x 7 dot character font
(3) Display ON/OFF control ..... D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF
(4) Entry mode set .... I/D = 1 : +1 (increment)
S = 0 : No shift

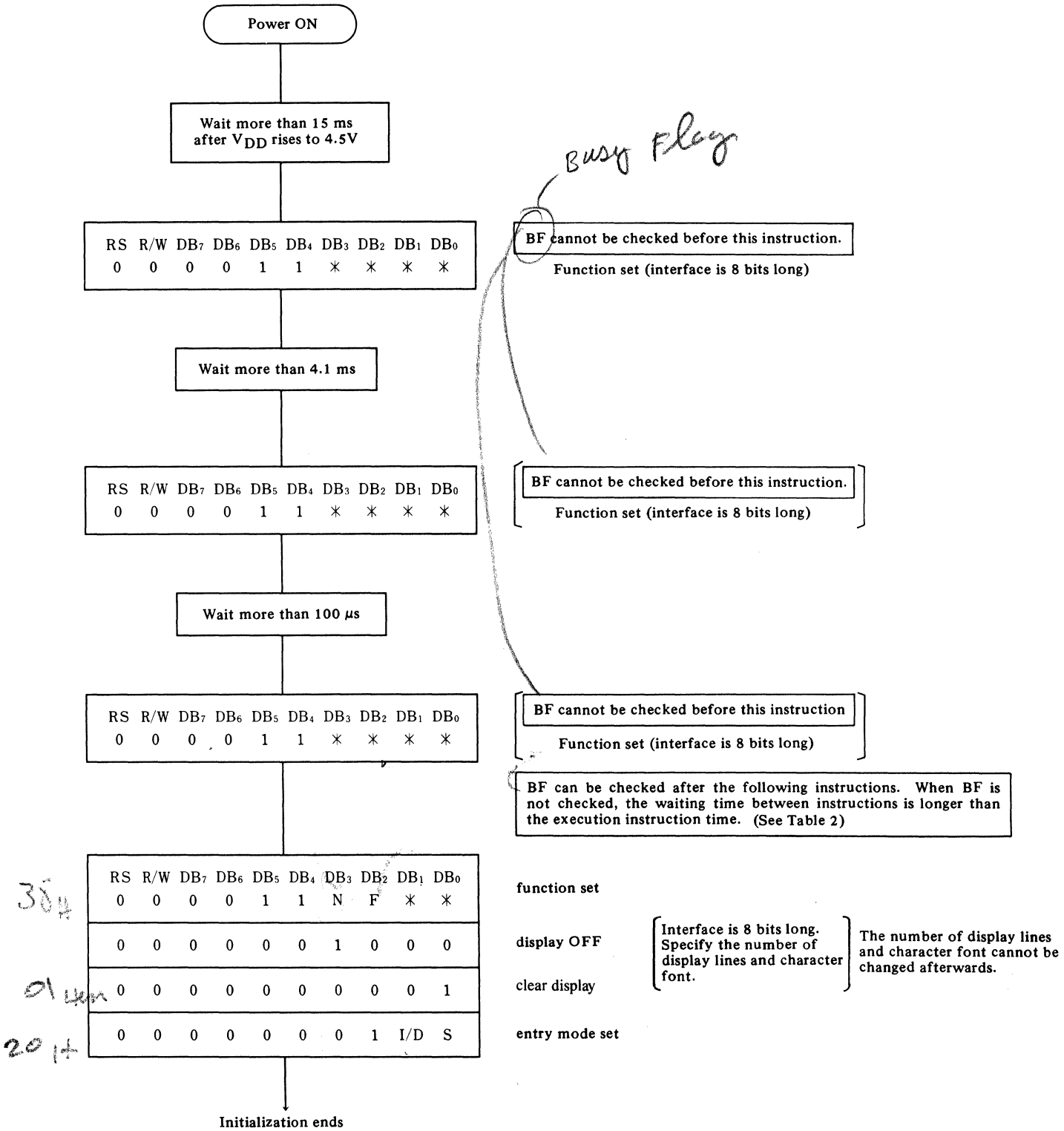
(5) Write DD RAM
When the rise time of power supply (0.2 → 4.5) is out of the range 0.1 ms ~ 10 ms, or when the low level width of power OFF (less than 0.2 V) is less than 1 ms, the internal reset circuit will not operate normally.
In this case, initialization will not be performed normally. Initialize by MPU according to "4.2 initializing by instruction" at the head of program.

4.2 Initializing by instruction

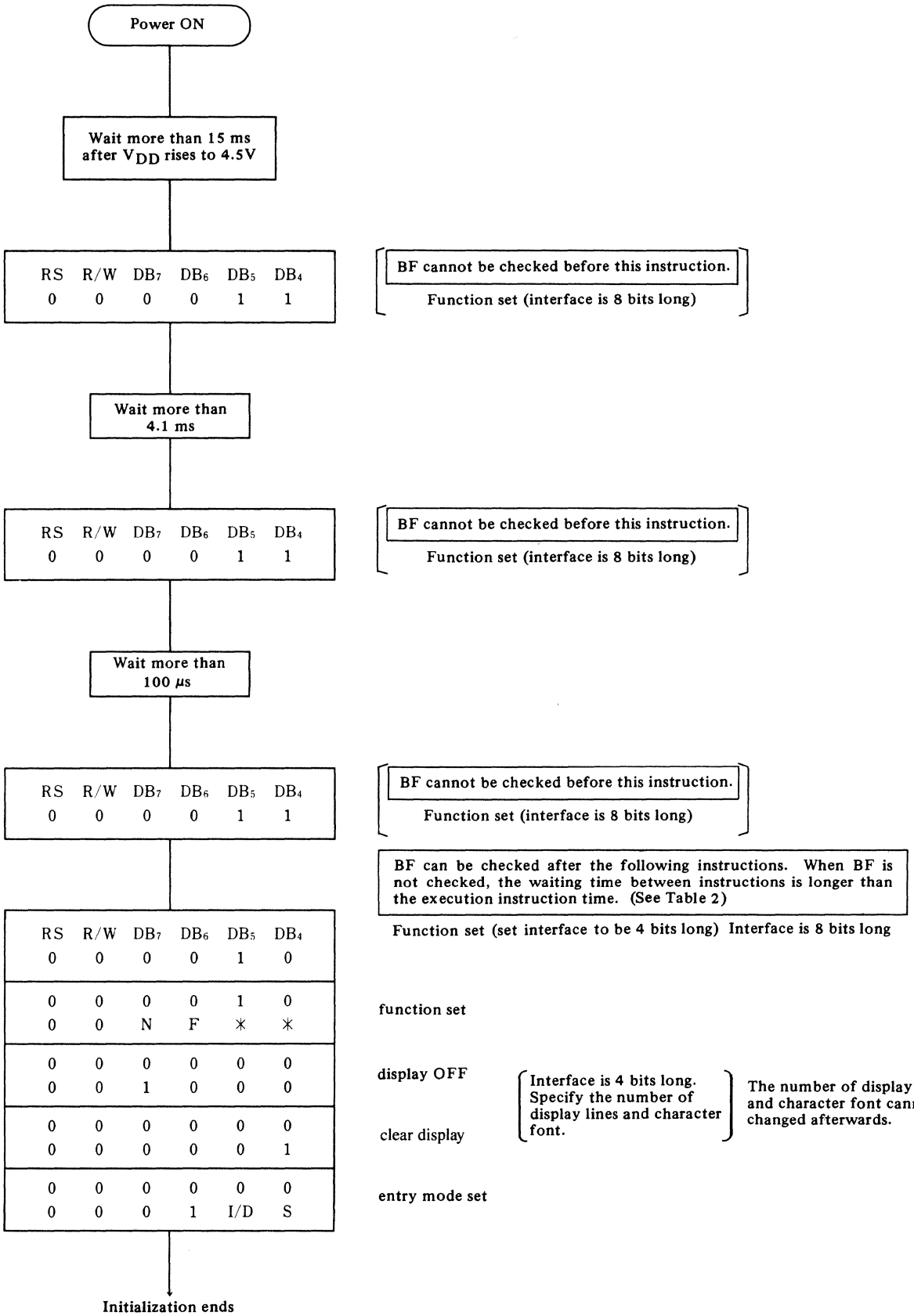
If the power supply conditions for correctly operating the internal reset circuit are not met, initialization by instruction is required.

Use the following procedure for initialization.

(1) When interface is 8 bits long.



(2) When interface is 4 bits long



5. Instruction

5.1 Outline

Only two HD44780 registers, the Instruction Register (IR) and the Data Register (DR) can be directly controlled by the MPU. Prior to internal operation start, control information is temporarily stored in these registers, to allow interface from HD44780 internal operation to various types of MPUs which operate in different speeds or to allow interface to peripheral control ICs. HD44780 internal operation is determined by signals sent from the MPU. These signals include register selection signals (RS), read/write signals (R/W) and data bus signals ($DB_0 \sim DB_7$), and are called instructions, here. Table 2 shows the instructions and their execution time. Details are explained in subsequent sections.

Instructions are of 4 types, those that,

(1) Designate HD44780 functions such as display format, data length, etc.
(2) Give internal RAM addresses.
(3) Perform data transfer with internal RAM
(4) Others

In normal use, category (3) instructions are used most frequently. However, automatic incrementing by +1 (or decrementing by −1) of HD44780 internal RAM addresses after each data write lessens the MPU program load. The display shift is especially able to perform concurrently with display data write, enabling the user to develop systems in minimum time with maximum programming efficiency. For an explanation of the shift function in its relation to display, see 5.3.

When an instruction is executing during internal operation, no instruction other than the busy flag/address read instruction will be executed.

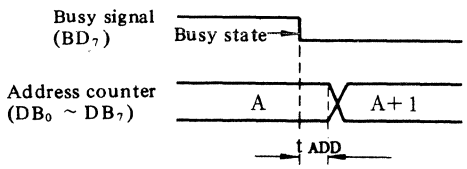
Because the busy flag is set to "1" while an instruction is being executed, check to make sure it is on "1" before sending an instruction from the MPU.

Note 1

Make sure the HD44780 is not in the busy state (BF = 0) before sending the instruction from the MPU to the HD44780. If the instruction is sent without checking the busy flag, the time between first and next instructions is much longer than the instruction time. See Table 2 for a list of each instruction execution time.

Note 2

After executing instruction of writing data to CG/DD RAM or reading data from CG/DD RAM, RAM address counter is automatically incremented by 1 (or decremented by 1). In this case, this shift is executed after Busy Flag is set to "Low". t_{ADD} is stipulated the time from the fall edge of busy flag to the end of address counter's renewal.



t_{ADD} depends on the operating frequency

$$t_{ADD} = \frac{1.5}{f_{CP} \text{ or } f_{osc}} \text{ (s)}$$

Table 2 Instructions

Instruction	Code										Description	Execution time (when fosc is 250 kHz) Note 1	Execution time (when fosc is 160 kHz) Note 2
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	82 μs ~ 1.64 ms	120 μs ~ 4.9 ms
Return home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	40 μs ~ 1.6 ms	120 μs ~ 4.8 ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40 μs	120 μs
Display ON/ OFF control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40 μs	120 μs
Cursor and display shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents	40 μs	120 μs
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lines (L) and character font (F).	40 μs	120 μs
Set CG RAM address.	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs	120 μs
Set DD RAM address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs	120 μs
Read busy flag & address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	1μs	1 μs
Write data to CG or DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs	120 μs
Read data to CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs	120 μs
	I/D = 1: Increment (+1) I/D = 0: Decrement (−1) S = 1: Accompanies display shift. S/C = 1: Display shift S/C = 0: Cursor move R/L = 1: Shift to the right. R/L = 0: Shift to the left. DL = 1: 8 bits DL = 0: 4 bits N = 1: 2 lines N = 0: 1 line F = 1: 5 x 10 dots F = 0: 5 x 7 dots BF = 1: Internally operating BF = 0: Can accept instruction										DD RAM: Display data RAM CG RAM: Character generator RAM A_{CG}: CG RAM address A_{DD}: DD RAM address Corresponds to cursor address. AC: Address counter used for both of DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fosc is 270 kHz: $40\ \mu s \times \frac{250}{270} = 37\ \mu s$	

*No effect

Notes 1. Applied to models driven by 1/8 duty or 1/11 duty.
2. Applied to models driven by 1/16 duty.

SECTION 6

5.2 Description of details

(1) Clear display

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	1

Writes space code "20" (hexadecimal) (character pattern for character code "20" must be blank pattern) into all DD RAM addresses. Sets DD RAM address 0 in address counter. Returns display to its original status if it was shifted. In other words, the display disappears and the cursor or blink go to the left edge of the display (the first line if 2 lines are displayed). Set I/D = 1 (Increment Mode) of Entry Mode. S of Entry Mode doesn't change.

(2) Return home

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	0	0	0	0	*

* No effect

Sets the DD RAM address 0 in address counter. Returns display to its original status if it was shifted. DD RAM contents do not change. The cursor or blink go to the left edge of the display (the first line if 2 lines are displayed).

(3) Entry mode set

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	0	0	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM. The cursor or blink moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S is 1; to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM when writing into or reading out from the CG RAM does it shift when S = 0.

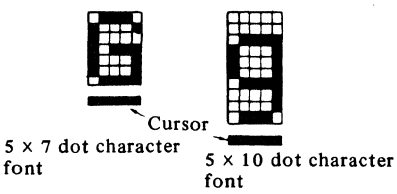
(4) Display ON/OFF control

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	0	1	D	C	B

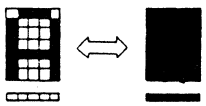
D: The display is ON when D = 1 and OFF when D = 0. When off due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

C: The cursor displays when C = 1 and does not display when C = 0. Even if the cursor disappears, the function of I/D, etc. does not change during display data write. The cursor is displayed using 5 dots in the 8th line when the 5 x 7 dot character font is selected and 5 dots in the 11th line when the 5 x 10 dot character font is selected.

B: The character indicated by the cursor blinks when B = 1. The blink is displayed by switching between all blank dots and display characters at 409.6 ms interval when f_{CP} or f_{osc} = 250 kHz. The cursor and the blink can be set to display simultaneously. (The blink frequency changes according to the reciprocal of f_{CP} or f_{osc}. $409.6 \times \frac{250}{270} = 379.2$ ms when f_{CP} = 270 kHz.)



(a) Cursor Display Example



(b) Blink Display Example

(5) Cursor or display shift

	RS	R/W	DB_7							DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* No effect

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display, the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time. When the displayed data is shifted repeatedly each line only moves horizontally. The 2nd line display does not shift into the 1st line position.

S/C	R/L	
0	0	Shifts the cursor position to the left. (AC is decremented by one.)
0	1	Shifts the cursor position to the right. (AC is incremented by one.)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

Address counter (AC) contents do not change if the only action performed is shift display.

(6) Function set

	RS	R/W	DB_7						DB_0
Code	0	0	0	0	1	DL	N	F	*	*

* No effect

DL: Sets interface data length. Data is sent or received in 8 bit lengths ($DB_7 \sim DB_0$) when DL = 1 and in 4 bit lengths ($DB_7 \sim DB_4$) when DL = 0.
When the 4 bit length is selected, data must be sent or received twice.

N: Sets number of display lines.

F: Sets character font.

(Note) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed unless the interface data length is changed.

N F	No. of display lines	Character font	Duty factor	Remarks
0 0	1	5 x 7 dots	1/8	
0 1	1	5 x 10 dots	1/11	
1 *	2	5 x 7 dots	1/16	Cannot display 2 lines with 5 x 10 dot character font.

* No effect

(7) Set CG RAM address

	RS	R/W	DB_7						DB_0
Code	0	0	0	1	A	A	A	A	A	A

← Higher Order Bits Lower Order Bits →

Sets the CG RAM address into the address counter in binary AAAAAA. Data is then written or read from the MPU for the CG RAM.

(8) Set DD RAM address

	RS	R/W	DB_7							DB_0
Code	0	0	1	A	A	A	A	A	A	A

← Higher Order Bits lower Order Bits →

Sets the DD RAM address into the address counter in binary AAAAAAA. Data is then written or read from the MPU for the DD RAM.

However, when N = 0 (1-line display), AAAAAAA is "00" ~ "4F" (hexadecimal),
when N = 1 (2-line display), AAAAAAA is "00" ~ "27" (hexadecimal) for the first line, and "40" ~ "67" (hexadecimal) for the second line.

(9) Read busy flag & address

	RS	R/W	DB_7							DB_0
Code	0	1	BF	A	A	A	A	A	A	A

← Higher Order Bits Lower Order Bits →

Reads the busy flag (BF) that indicates the system is now internally operating by a previously received instruction. BF = 1 indicates that internal operation is in progress. The next instruction will not be accepted until BF is set to "0". Check the BF status before the next wire operation.

At the same time, the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM addresses, and its value is determined by the previous instruction. Address contents are the same as in Items (7) and (8).

(10) Write data to CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	0	D	D	D	D	D	D	D	D

← Higher Order Bits Lower Order Bits →

Writes binary 8 bit data DDDDDDDD to the CG or the DD RAM. Whether the CG or DD RAM is to be written into is determined by the previous specification of CG RAM or DD RAM address setting. After write, the address is automatically incremented or decremented by 1 according to entry mode. The entry mode also determines display shift.

(11) Read data from CG or DD RAM

	RS	R/W	DB_7							DB_0
Code	1	1	D	D	D	D	D	D	D	D
	← Higher Order Bits							Lower Order Bits →		

Reads binary 8 bit data DDDDDDDD from the CG or DD RAM. The previous designation determines whether the CG or DD RAM is to be read. Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction. If you don't, the first read data will be invalidated. When serially executing the "read" instruction, the next address data is normally read from the second read. The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM's address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However, display shift is not executed no matter what the entry mode is.

(Note) The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot than be read out even if "read" instructions are executed. The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM), just before reading out execute the "read" instruction from the second time the "read" instruction is serial.

5.3 Instruction and display correspondence

(1) 8-bit operation, 8-digit x 1-line display (using internal reset)

Following table shows an example of 8-bit x 1-line display in 8-bit operation.

The HD44780 functions must be set by Function Set prior to display. Since the display data RAM can store data for 80 characters, as explained before, the RAM can be used for displays like the lightening board when combined with display shift operation.

Since the display shift operation changes display position only and DD RAM contents remain unchanged, display data entered first can be output when the return home operation is performed.

8 bit operation, 8-digit 1-line display example (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 0 0 * *		Sets to 8-bit operation and selects 1-line display lines and character font. (Number of display lines and character fonts cannot be changed hereafter.)
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right at the time of write to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HI_	Writes "I".
7	⋮	⋮	
8	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
9	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	•HITACHI_	Sets mode for display shift at the time of write.
10	Write Data to CG RAM/DD RAM 1 0 0 0 1 0 0 0 0 0	ITACHI_	Writes "Space".
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	TACHI M_	Writes "M".
12	⋮	⋮	
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	MICROKO_	Writes "0".
14	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
15	Cursor or Display Shift 0 0 0 0 0 1 0 0 * *	MICROKO	Shifts only the cursor position to the left.
16	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 0 0 1 1	ICROCO	Writes "C" (correction). The display moves to the left.
17	Cursor or Diaplay Shift 0 0 0 0 0 1 1 1 * *	MICROCO	Shifts the display and cursor position to the right.
18	Cursor or Display Shift 0 0 0 0 0 1 0 1 * *	MICROCO_	Shifts display and cursor position to the right.
19	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ICROCOM_	Writes "M".
20	⋮	⋮	
21	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI	Returns both display and cursor to the original position (Address 0).

(2) 4-bit operation, 8-digit x 1-line display (using internal reset)

The program must set functions prior to 4-bit operation. The following table shows an example. When power is turned on, 8-bit operation is automatically selected and the first write is performed as an 8-bit operation. Since nothing is connected to $DB_0 \sim DB_3$, a rewrite is then required. However, since one operation is completed in two access of 4-bit operation, a rewrite is needed as a function (see the following table).

Thus, $DB_4 \sim DB_7$ of the function set is written twice.

4 bit operation, 8-digit 1-line display (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_4 0 0 0 0 1 0		Sets to 4-bit operation. In this case, operation is handled as 8 bits by initialization, and only this instruction completes with one write.
3	Function Set 0 0 0 0 1 0 0 0 0 0 * *		Sets 4-bit operation and selects 1-line display and 5 x 7 dot character font. 4-bit operation starts from this point on and resetting is needed. (Number of display lines and character fonts cannot be changed hereafter.)
4	Display ON/OFF Control 0 0 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. Entire display is in space mode because of initialization.
5	Entry Mode Set 0 0 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
6	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 1 0 0 0	H_	Writes "H". The cursor is incremented by one and shifts to the right.

Hereafter, control is the same as 8-bit operation.

(3) 8-bit operation, 8-digit x 2-line display

For 2-line display, the cursor automatically moves from the first to the second line after the 40th digit of the 1st line has been written. Thus, if there are only 8 characters in the first line, the DD RAM address must again be set after the 8th character is completed. (See the following table) Note that the first and second lines of the display shift are performed. In the example, the display shift is performed when the cursor is on the second line. However, if shift operation is performed when the cursor is on the first line, both the first and second lines move together. When you repeat the shift, the display of the second display will only move within each line many times.

8 bit operation, 8-digit x 2-line display example (using internal reset)

No.	Instruction	Display	Operation
1	Power supply ON (HD44780 is initialized by the internal reset circuit)		Initialized. No display appears.
2	Function Set RS R/W DB_7 ~ DB_0 0 0 0 0 1 1 1 0 * *		Sets to 8-bit operation and selects 2-line display and 5 x 7 dot character font.
3	Display ON/OFF Control 0 0 0 0 0 0 1 1 1 0	_	Turns on display and cursor. All display is in space mode because of initialization.
4	Entry Mode Set 0 0 0 0 0 0 0 1 1 0	_	Sets mode to increment the address by one and to shift the cursor to the right, at the time of write, to the DD/CG RAM. Display is not shifted.
5	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 0	H_	Write "H". The DD RAM has already been selected by initialization when the power is turned on. The cursor is incremented by one and shifted to the right.
6	⋮	⋮	
7	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 0 0 1	HITACHI_	Writes "I".
8	Set DD RAM Address 0 0 1 1 0 0 0 0 0 0	HITACHI _	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
9	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	HITACHI M_	Writes "M".
10	⋮	⋮	
11	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 1 1	HITACHI MICROCO_	Writes "0".
12	Entry Mode Set 0 0 0 0 0 0 0 1 1 1	HITACHI MICROCO_	Sets mode for display shift at the time of write.
13	Write Data to CG RAM/DD RAM 1 0 0 1 0 0 1 1 0 1	ITACHI ICROCOM_	Writes "M". Display is shifted to the right. The first and second lines' shift are operated at the same time.
14	⋮	⋮	
15	Return Home 0 0 0 0 0 0 0 0 1 0	HITACHI MICROCOM	Returns both display and cursor to the original position (Address 0).

6. Precaution on programming

(1) Instruction of function set

Perform the function at the head of program that accesses HD44780 before executing all instructions, and not change the data of the Instruction Register in the program. The data of function register can be changed by the program as follows;

a. • Changing of DL (Data Length)
   • Perform the instruction appointed in 4.2 (2), when DL is changed from 8-bit length to 4-bit length mode.
   • Perform the instruction appointed in 4.2 (1), when DL is changed from 4-bit length to 8-bit length mode.

b. • Changing of N (Column Number)
   • Perform the instruction of function set after executing instruction of display clear or display off.

In this case, sequence of AC and DD RAM must be changed. Thus, rewrite the address set register after that.

c. • Changing of F (Font)
   • There is no problem in this case, but for dual-line display, the font mode of 5 x 11 cannot be selected (this mode is forbidden by hardware).

When N or F is changed, power supply voltage for LCD must be changed. If not changed, crosstalk will appear, or contrast will be poor.

(2) Busy flag check

HD44780 is produced in the CMOS process, therefore internal executing time is long. Standard time is 40 $\mu s \sim$ 1.6 ms. (This varies by instruction)

When the high speed MPU controls it, check the busy flag before performing instruction or reading data.

While internal operation is active, Enable signal is not accepted. (Enable signal at reading status register for checking busy flag is accepted) Busy flag signal is output through DB_7, as shown in Table 3, when RS = "0", R/W = "1", and Enable = "1".

(3) Input of unidentified instruction code

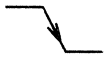
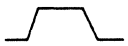
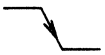
Undefined instruction code of HD44780 is only as follows;

RS	R/W	$DB_7 \sim DB$
0	0	0 ~

(Others are included to defined instruction)

When the undefined instruction code is loaded to HD44780, it accepts the code, but does not change the internal states (RAM and other status of Flags). Busy state, however continues for maximum 40 μs by the acceptance of the code.

Table 3 The relation between the operation and the combination of RS, R/W

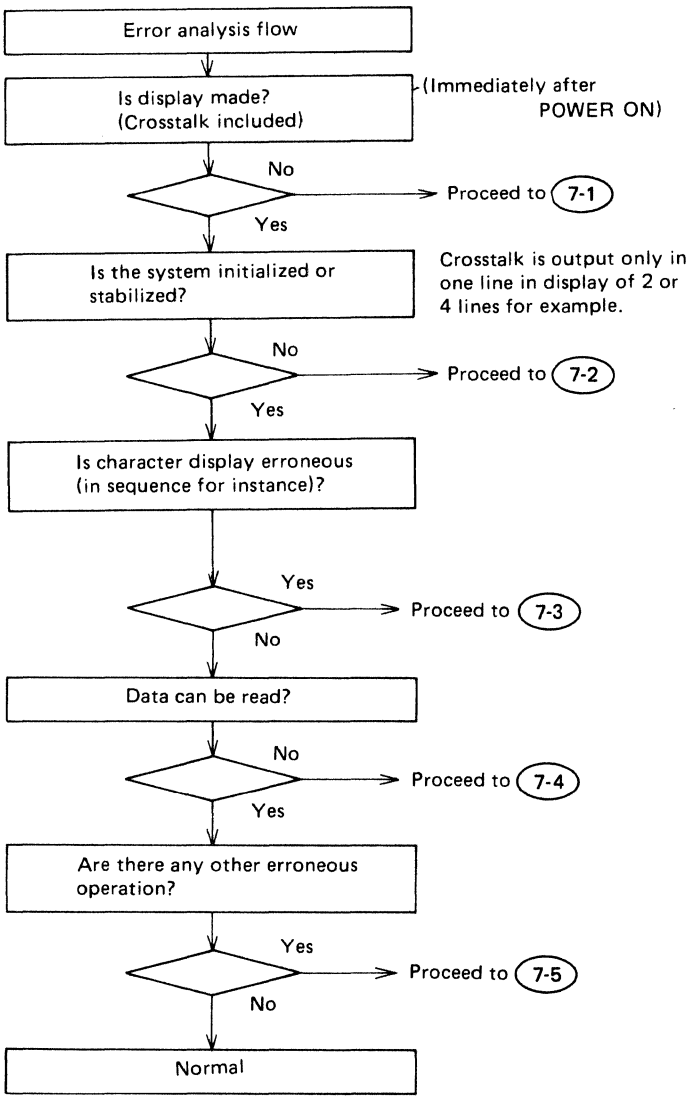
RS	RW	E	OPERATION
0	0		Write instruction code
0	1		Read busy flag and address counter
1	0		Write data
1	1		Read data

When performing data and instruction code by 4 bit, transfer RS, R/W every time.

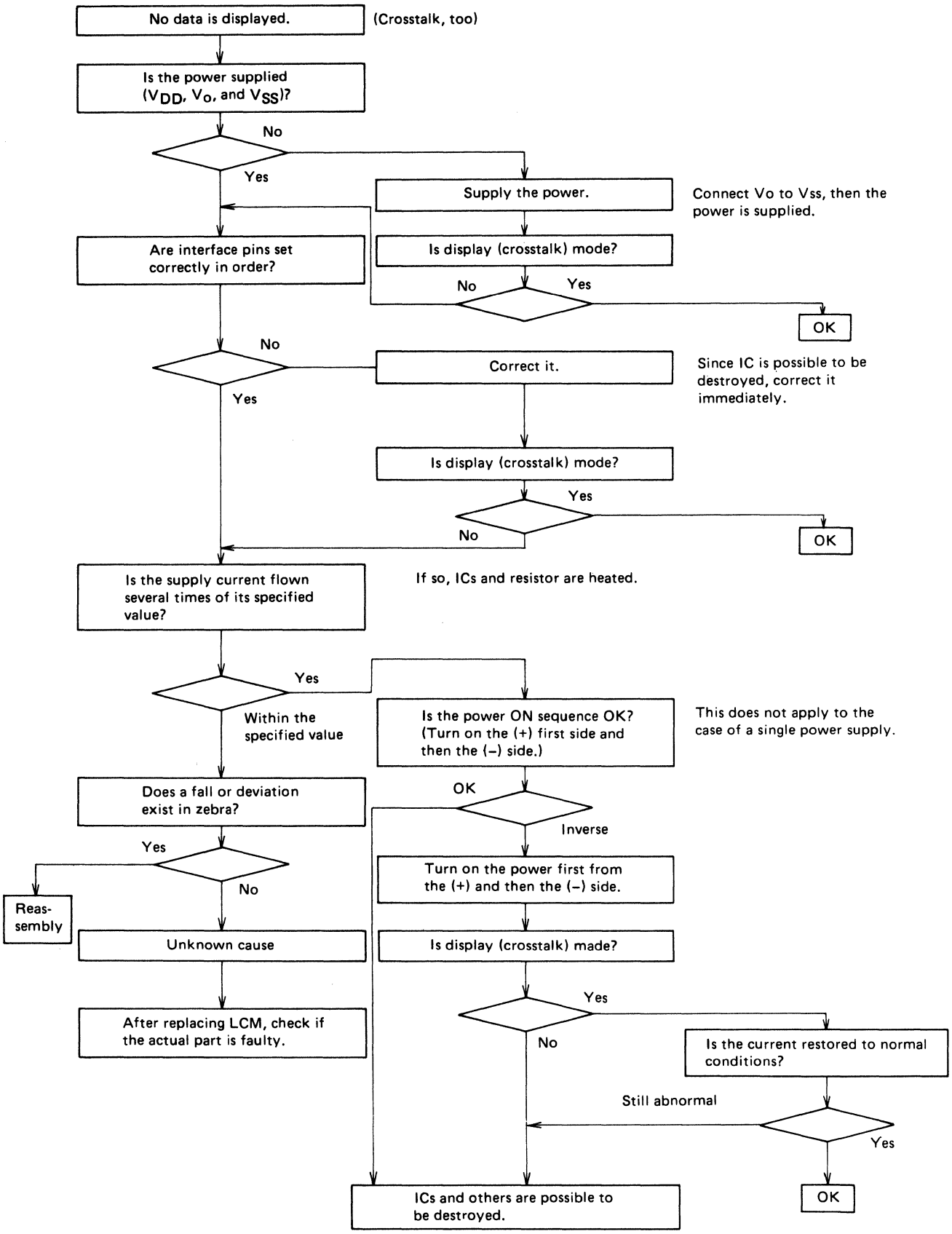
7. How to check trouble

Follow the flowchart below to check errors.

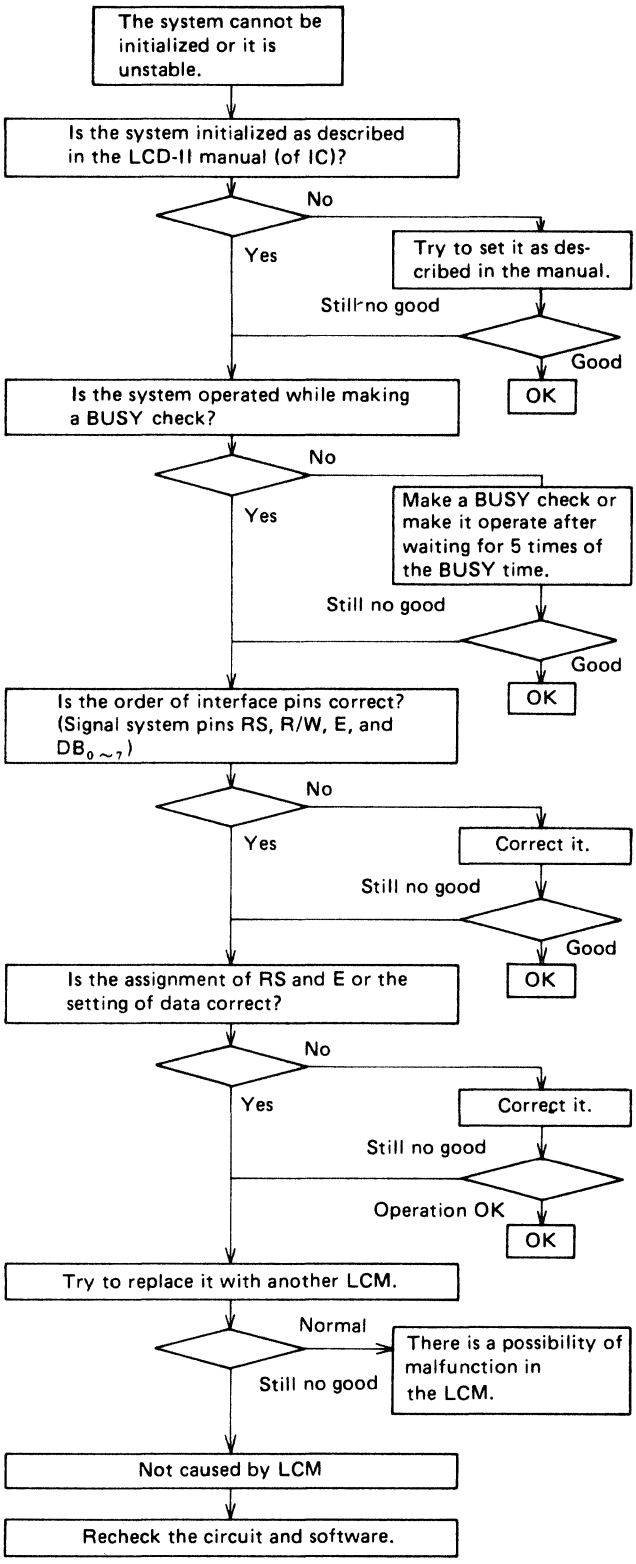
■ **Error analysis flowchart**



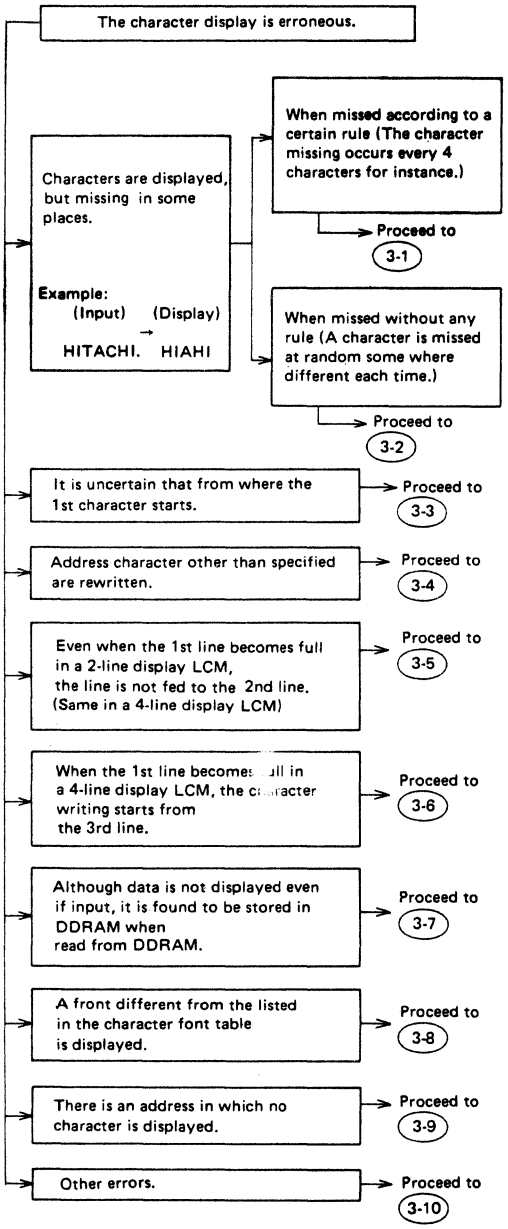
7.1 No data is displayed (Crosstalk too)



7.2 The system cannot be initialized or it is unstable.



7.3 The character display is erroneous.



(3-1)

Data is fed too fast. → Retry it while making a BUSY check. It is still too fast even when the BUSY check is made. → The function of LCD-II is no good.

(3-2)

Data is fed too fast. → Retry it while making a BUSY check.

(3-3)

The address Set command is not included in the initialization.

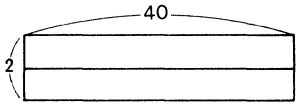
→ Although the address is so designed to be set to "00" at the power ON according to the Power ON Reset function of the LCD-II itself, this Power ON Reset function does not work in some cases according to the power ON conditions.

(3-4)

When no error exists in the software, the function of LCD-II is no good.

(3-5)

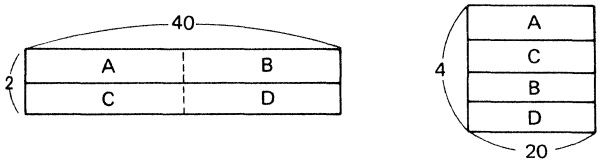
The 2-line display LCM is electrically composed of 40 characters x 2 lines, but it displays 16 characters or 20 characters partly. When 16 characters are written (in the 1st line) and the data at the 17th character is input as it is, it is entered in the 17th character in the 1st line and its is neither displayed on the screen. It is therefore necessary to set the address [LF] between the 16th caracter and 17th character.



[LF] : line feed

(3-6)

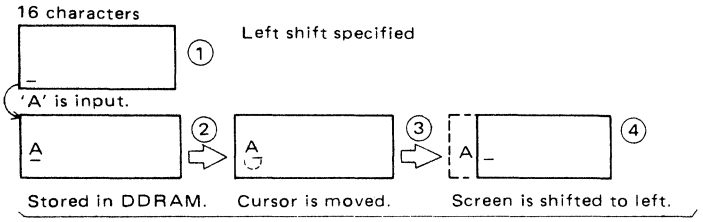
The 4-line display LCM is composed as shown in the right figure. Consequently, when written continuously from the 1st line, the data is written as A → B. When displayed in 4 lines, the data is moved from the 1st line to the 3rd line. It is therefore necessary to set the address of [LF] in this case.



(3-7)

The display ON/OFF flag is turned to the OFF side. (This flag is by no means set unless turned to the ON side.).

When employing the shift function together, the screen is shifted each time a data is written and the data can not be seen on the screen in some cases. It is therefore necessary to correct the application of the shift function.



* Since this operation is carried out in a moment, what can be seen is the status of ① and ④ only. Although not displayed in appearance, the data is stored in the DDRAM.

(3-8)

Defective CGROM font → IC is faulty.

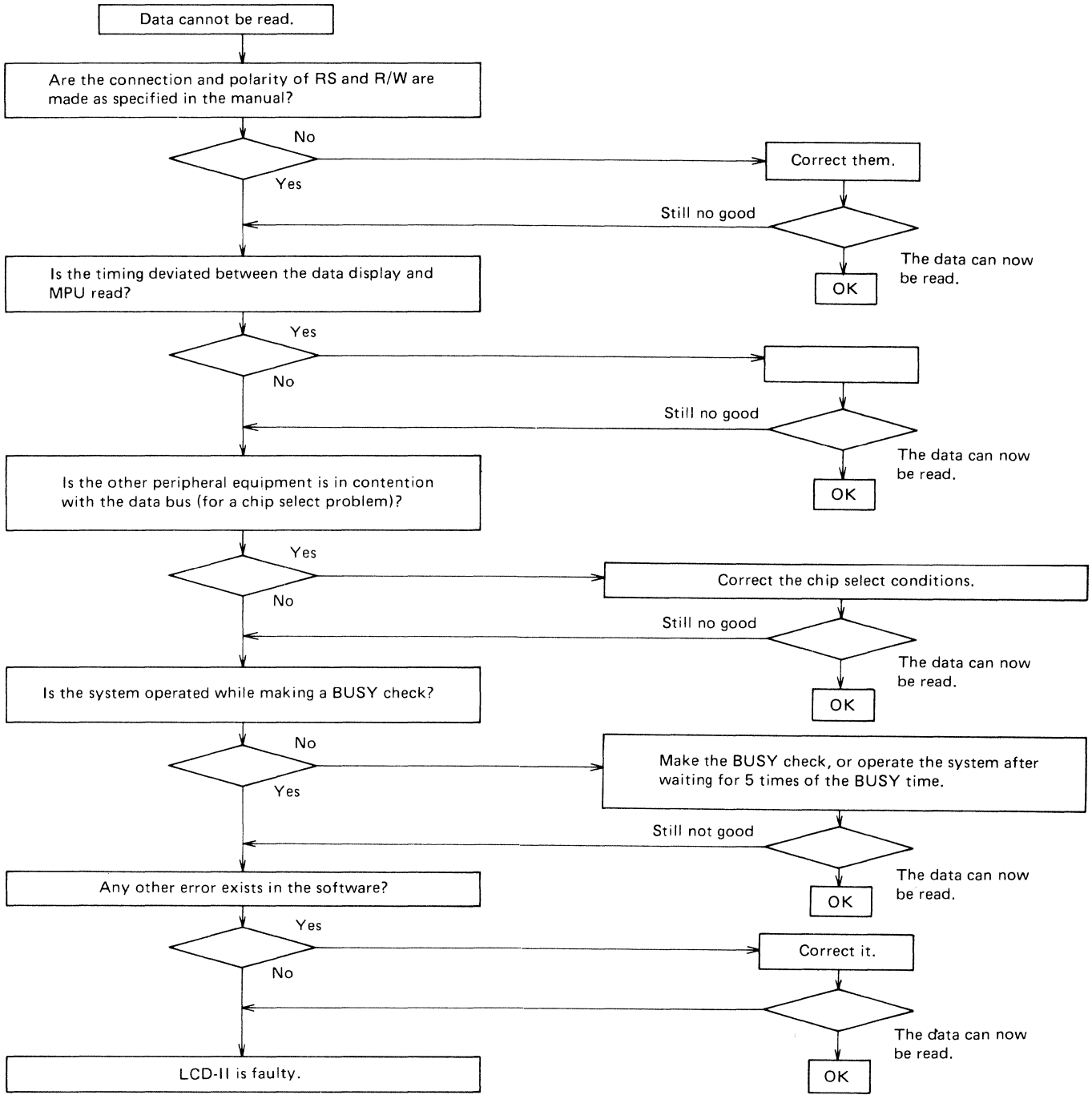
(3-9)

If no error exists in the software, the IC is faulty.

(3-10)

Contact our agent for any other erroneous event.

7.4 Data cannot be read



7.5 Others

Others

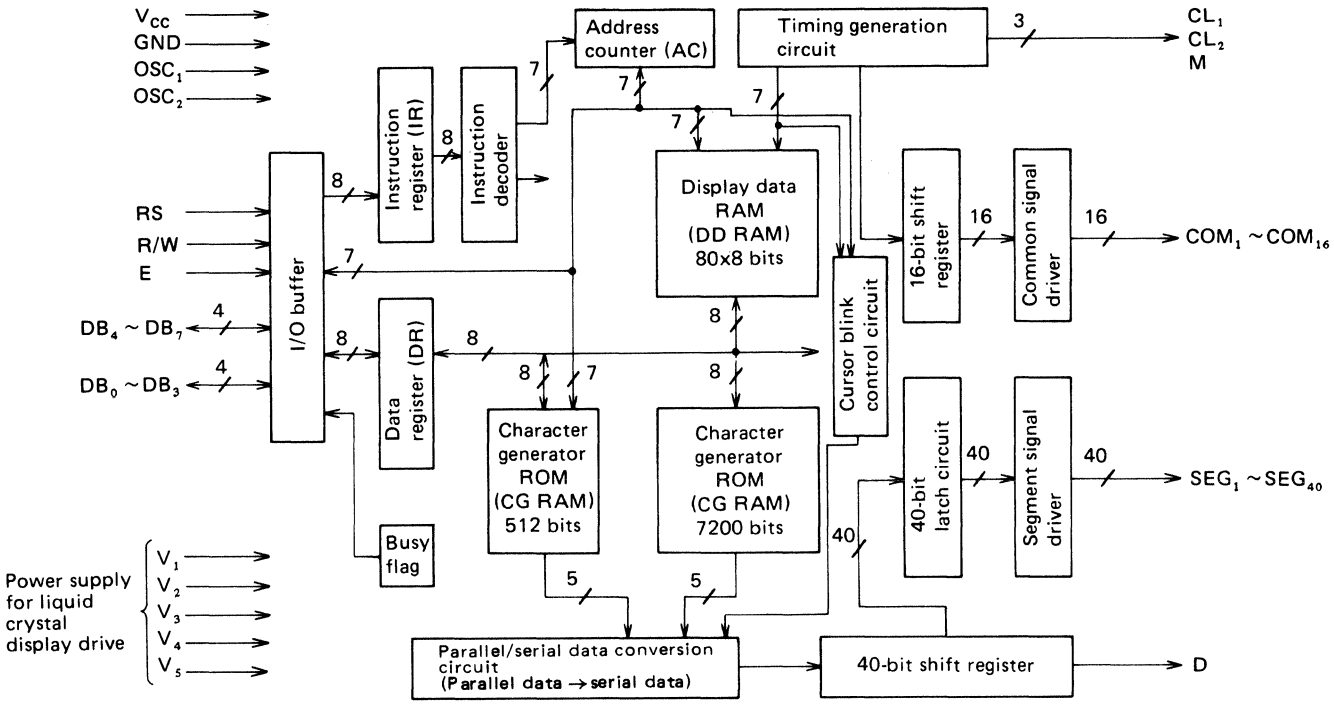
↓

Check the following:

- Use conditions
- Erroneous events
- Contents of operation before and after the error event occurrence
- Flowchart, if possible. (The program, if given, can not be decoded.)

8. Block diagram and function of each block

8.1 Block diagram of HD44780 interior



8.2 Function of each block

(1) Register

The HD44780 has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes such as display clear and cursor shift, and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written from the MPU but not read by the MPU.

The DR temporarily stores data to be written into the DD RAM or the CG RAM and data to be read out from DD RAM or CG RAM. Data written into the DR from the MPU is automatically written into the DD RAM or the CG RAM by internal operation. The DR is also used for data storage when reading data from the DD RAM or the CG RAM. When address information is written into the IR, data is read into the DR from the DD RAM or the CG RAM by internal operation. Data transfer to the MPU is then completed by the MPU reading DR. After the MPU reads the DR, data in the DD RAM or CG RAM at the next address is sent to the DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Table 4 Register selection

RS	R/W	E	Operation
0	0	⌐	IR write as internal operation (Display clear, etc.)
0	1	⌐‾⌐	Read busy flag (DB_7) and address counter (DB_0 ~ DB_6)
1	0	⌐	DR write as internal operation (DR to DD or CG RAM)
1	1	⌐‾⌐	DR read as internal operation (DD or CG RAM to DR)

(2) Busy flag (BF)

When the busy flag is "1", the HD44780 is in the internal operation mode, and the next instruction will not be accepted. As Table 4 shows, the busy flag is output to DB_7 when RS = 0 and R/W = 1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address counter (AC)

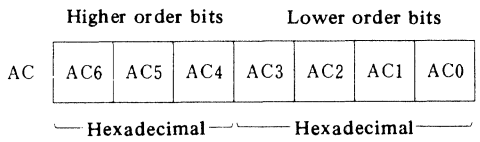
The address counter (AC) assigns addresses to DD and CG RAMs. When an instruction for address is written in IR, the address information is sent from IR to AC. Selection of either DD or CG RAM is also determined concurrently by the instruction.

After writing into (or reading from) DD or CG RAM display data, AC is automatically incremented by +1 (or decremented by −1). AC contents are output DB_0 ~ DB_6 when RS = 0 and R/W = 1, as shown in Table 4.

(4) Display data RAM (DD RAM)

The display data RAM (DD RAM) stores display data represented in 8-bit character codes. Its capacity is 80 x 8 bits, or 80 characters. The display data RAM (DD RAM) that is not used for display can be used as a general data RAM. Relations between DD RAM addresses and positions on the liquid crystal display are shown below.

The DD RAM address (A_{DD}) is set in the Address Counter (AC) and is represented in hexadecimal.



(Ex.) DD RAM address "4E"

1	0	0	1	1	1	0
4			E			

1-line display (N = 0)

	1	2	3	4	5					79	80	← display position
1-line	00	01	02	03	04					4E	4F	← DD RAM address

(a) When the display characters are less than 80, the display begins at the head position. For example, 8 characters using one HD44780 are displayed as:

	1	2	3	4	5	6	7	8	← display position
1-line	00	01	02	03	04	05	06	07	← DD RAM address

When the display shift operation is performed, the DD RAM address moves as:

	01	02	03	04	05	06	07	08
(Left shift display)								
	4F	00	01	02	03	04	05	06
(Right shift display)								

(b) 16-character display using an HD44780 and an HD44100H is as shown below:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address

└——HD44780 display——┘└——HD44100H display——┘

When the display shift operation is performed, the DD RAM address moves as:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	(Left shift display)
4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	(Right shift display)

(c) The relation between display position and DD RAM address when the number of display digits is increased through the use of one HD44780 and two or more HD44100H's can be considered an extension of (b). Since the increase can be 8 digits for each additional HD44100H, up to 80 digits can be displayed by externally connecting 9 HD44100H's.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	73	74	75	76	77	78	79	80	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	48	49	4A	4B	4C	4D	4E	4F	← DD RAM address

└—HD44780 display—┘└—HD44100H (1) display—┘└—HD44100H (2) ~ (8) display—┘└—HD44100H (9) display—┘

2-line display (N = 1)

	1	2	3	4	5		39	40	← display position
1-line	00	01	02	03	04	.....	26	27	← DD RAM address
2-line	40	41	42	43	44	.....	66	67	

(a) When the number of display characters is less than 40 x 2 lines, the 2 lines from the head are displayed. Note that the first line end address and the second line start address are not consecutive. For example, when an HD44780 is used, 8 characters x 2 lines are displayed as:

	1	2	3	4	5	6	7	8	← display position
1-line	00	01	02	03	04	05	06	07	← DD RAM address
2-line	40	41	42	43	44	45	46	47	

When display shift is performed, the DD RAM address move as:

01	02	03	04	05	06	07	08	(Left shift display)
41	42	43	44	45	46	47	48	

27	00	01	02	03	04	05	06	(Right shift display)
67	40	41	42	43	44	45	46	

(b) 16 character x 2 line are displayed when an HD44780 and an HD44100H are used

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	

└——HD44780 display——┘└——HD44100H display——┘

When display shift is performed, the DD RAM address moves as follows:

01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

(Left shift display)

27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

(Right shift display)

(c) The relation between display position and DD RAM address when the number of display digits is increased by using one HD44780 and two or more HD44100H's, can be considered an extension of (b).

Since the increase can be 8 digits x 2 lines for each additional HD44100H, up to 40 digits x 2 lines can be displayed by connecting 4 HD44780's externally.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		33	34	35	36	37	38	39	40	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	·····	20	21	22	23	24	25	26	27	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	·····	60	61	62	63	64	65	66	67	

└— HD44780 display —┘ └— HD44100 (1) display —┘ └— HD44100H (2) (3) display —┘ └— HD44100H (4) —┘

(d) Display position and DD RAM address for LM020L.

Character NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM address	00	01	02	03	04	05	06	07	40	41	42	43	44	45	46	47

(Note) Shift display is as same as that of 8 char. x 2 line type.

(e) Display position and DD RAM address for LM041L.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	
3-line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
4-line	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	

(f) Display position and DD RAM address for LM044L.

	1行	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	← display position
1-line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	← DD RAM address
2-line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	
3-line	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	
4-line	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67	

(Note) Shift display is as same as 2-line type.

(5) Character generator ROM (CG ROM)

The character generator ROM generates 5 x 7 dot or 5 x 10 dot character patterns from 8-bit character codes. It can generate 160 types of 5 x 7 dot character patterns and 32 types of 5 x 10 dot character patterns. Tables 5 (1) and 5 (2) show the relation between character codes and character patterns in the Hitachi standard HD44780A00. User defined character patterns are also available by mask-programming ROM. For details, see "The LCD-II (HD44780) Breadboard User's Manual".

(6) Character generator RAM (CG RAM)

The character generator RAM is the RAM with which the user can rewrite character patterns by program. With 5 x 7 dots, 8 types of character patterns can be written and with 5 x 10 dots 4 types can be written. Write the character codes in the left columns of Tables 6 (1) and 6 (2) to display character patterns stored in CG RAM.

Table 5 shows the relation between CG RAM addresses and data and display patterns.

As Table 5 shows, an area that is not used for display can be used as a general data RAM.

(7) Timing generation circuit

The timing generation circuit generates timing signals to operate internal circuits such as DD RAM, CG ROM and CG RAM. RAM read timing needed for display and internal operation timing by MPU access are separately generated so they do not interfere with each other. Therefore, when writing data to the DD RAM, for example, there will be no undesirable influence, such as flickering, in areas other than the display area. This circuit also generates timing signals to operate the externally connected driver LSI HD44100H.

(8) Liquid crystal display driver circuit

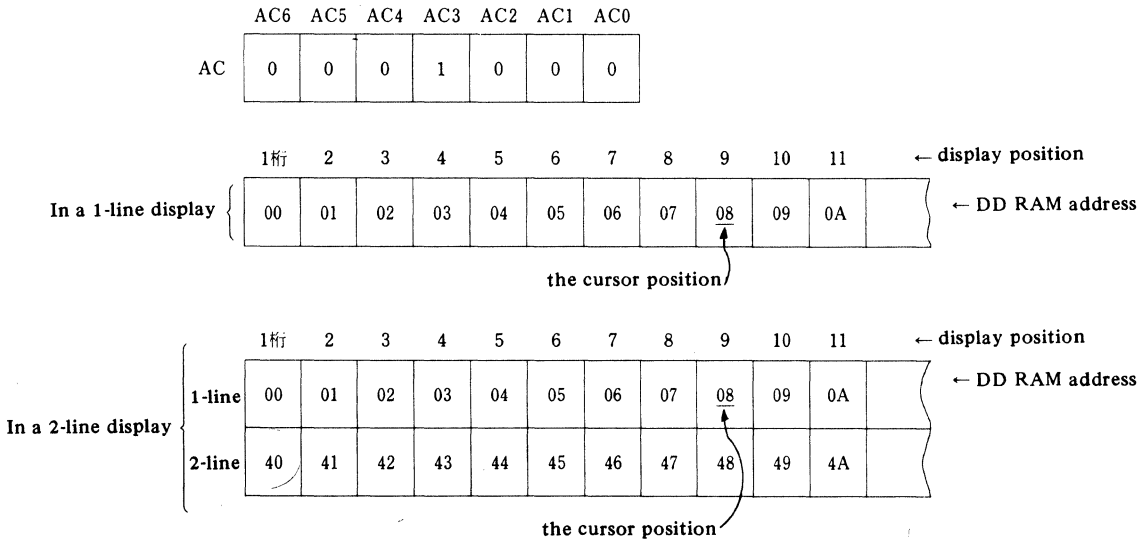
The liquid crystal display driver circuit consists of 16 common signal drivers and 40 segment signal drivers. When character font and number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, the other common signal drivers continue to output non-selection waveforms. The segment signal driver has essentially the same configuration as the driver LSI HD44100H. Character pattern data is sent serially through a 40-bit shift register and latched when all needed data has arrived. The latched data controls the driver for generating drive waveform outputs.

The serial data is sent to the HD44100H, externally connected in cascade, used for display digit number extension. Send of serial data always starts at the display data character pattern corresponding to the last address of the display data RAM (DD RAM). Since serial data is latched when the display data character pattern, corresponding to the starting address, enters the internal shift register, the HD44780 drives the head display. The rest displays, corresponding to latter addresses, are added with each additional HD44100H.

(9) Cursor/Blink control circuit

This is the circuit that generates the cursor or blink. The cursor or the blink appear in the digit residing at the display data RAM (DD RAM) address set in the address counter (AC).

When the address counter is $(08)_{16}$, a cursor position is:



(Note) The cursor or blink appears when the address counter (AC) selects the character generator RAM (CG RAM). But the cursor and blink are meaningless.
The cursor or blink is displayed in the meaningless position when AC is the CG RAM address.

Table 5

CORRESPONDENCE BETWEEN CHARACTER CODES AND CHARACTER PATTERN

(1) 5 x 10 dot, applied type: H2570, H2571, H2572, LM027

Lower 4bit \ Higher 4bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
××××0000	CG RAM (1)												
××××0001	(2)												
××××0010	(3)												
××××0011	(4)												
××××0100	(5)												
××××0101	(6)												
××××0110	(7)												
××××0111	(8)												
××××1000	(1)												
××××1001	(2)												
××××1010	(3)												
××××1011	(4)												
××××1100	(5)												
××××1101	(6)												
××××1110	(7)												
××××1111	(8)												

Note 1. CG RAM is a character generator RAM having a storage function of character pattern which enable to change freely by users program.
Note 2. When line setting at initialization is 2 lines (N = 1), pattern becomes 5 × 7 dot.

(2) 5 × 7 dot, applied type: LM054, H2570, LM015, LM568AF, LM020L, LM070L, LM038, LM027, H2571, H2572, LM058, LM052L, LM016L, LM032L, LM060L, LM017L, LM018L, LM041L, LM044L, LM068L, LM061L, LM104L, LM105L, LM107L

Note: CG ROM is a character generator RAM having a storage function of character pattern which enable to change freely by users program.

Table 6 Relation between CG RAM addresses and character code (DD RAM) and character pattern (CG RAM data).

(1) For 5 x 7 dot character pattern

Character Codes (DD RAM Data) 7 6 5 4 3 2 1 0 ←Higher Lower→	CG RAM Address 5 4 3 2 1 0 ←Higher Lower→	Character Patterns (CG RAM Data) 7 6 5 4 3 2 1 0 ←Higher Lower→	
0 0 0 0 ✳ 0 0 0	0 0 0	✳ ✳ ✳ 1 1 1 1 0	Character Pattern Example (1)
	0 0 1	1 0 0 0 1	
	0 1 0	1 0 0 0 1	
	0 1 1	1 1 1 1 0	
	1 0 0	1 0 1 0 0	
	1 0 1	1 0 0 1 0	
	1 1 0	1 0 0 0 1	
	1 1 1	✳ ✳ ✳ 0 0 0 0 0	← Cursor Position
0 0 0 0 ✳ 0 0 1	0 0 0	✳ ✳ ✳ 1 0 0 0 1	Character Pattern Example (2)
	0 0 1	0 1 0 1 0	
	0 1 0	1 1 1 1 1	
	0 1 1	0 0 1 0 0	
	1 0 0	1 1 1 1 1	
	1 0 1	0 0 1 0 0	
	1 1 0	0 0 1 0 0	
	1 1 1	✳ ✳ ✳ 0 0 0 0 0	
0 0 0 0 ✳ 1 1 1	0 0 0	✳ ✳ ✳	✳ No effect
	0 0 1		
	1 1 1 1 0 0		
	1 0 1		
	1 1 0		
	1 1 1	✳ ✳ ✳	

(Note) 1: Character code bits 0 ~ 2 correspond to CG RAM address bits 3 ~ 5 (3 bits: 8 types).

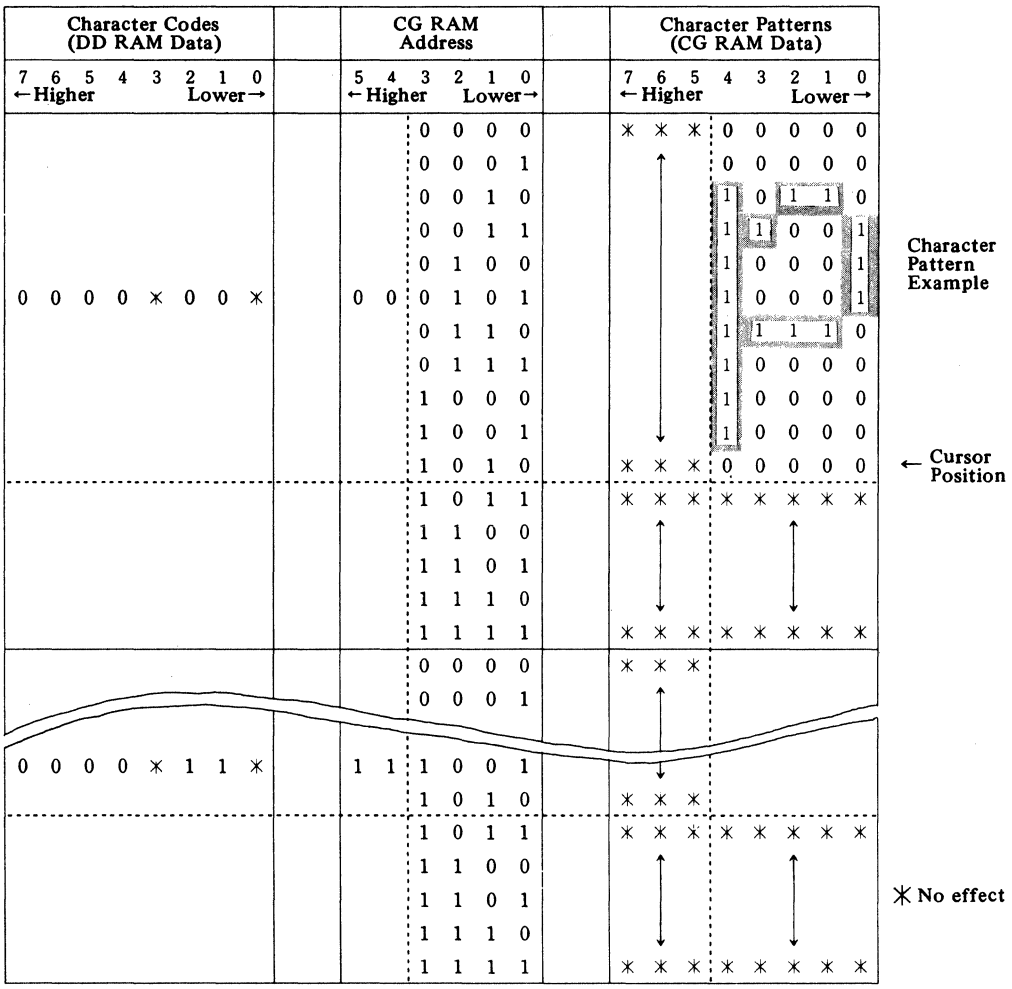
2: CG RAM address bits 0 ~ 2 designate character pattern line position. The 8th line is the cursor position and display is performed in logical OR by the cursor.
Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1", bit 1 lights up regardless of cursor existence.

3: Character pattern row positions correspond to CG RAM data bits 0 ~ 4, as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5 ~ 7 are not used for display, they can be used for the general data RAM.

4: As shown in Tables 3 and 4, CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 3 is a ineffective bit, the "R" display in the character pattern example, is selected by character code "00" (hexadecimal) or "08" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

(2) For 5 x 10 dot character pattern



(Note) 1: Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types).

2: CG RAM address bits 0 ~ 3 designate character pattern line position. The 11th line is the cursor position and display is performed in logical OR with cursor.
Maintain the 11th line data corresponding to the cursor display position in the "0" state for cursor display. When the 11th line data is "1", bit 1 lights up regardless of cursor existence. Since the 12th ~ 16th lines are not used for display, they can be used for the general data RAM.

3: Character pattern row positions are the same as 5 x 7 dot character pattern positions.

4: CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 0 and 3 are ineffective bits, "P" display in the character pattern example is selected by character code "00", "01", "08" and "09" (hexadecimal).

5: "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

HOW TO USE HITACHI'S CONTROL CIRCUIT BOARD WITH HD61830/HD61830B GRAPHIC CONTROLLER IC.

- CB1020R up to 160K pixel resolution
- CB1026R up to 320K pixel resolution
- CB1030R up to 2 × 320K pixel resolution
- CB1040R up to 2 × 640K pixel resolution

1. GENERAL

CB1020R, CB1026R and CB1030R (mounted with control LSI HD61830 and a socket for the refresh memory) are control circuit boards for graphic display modules.

They allow direct connection to the MPU's bus line. The HD61830 controls signal generation and data conversion required for a liquid crystal display (LCD) module. This simplifies the graphic display system.

These control circuit boards operate in graphic and character mode. In graphic mode, refresh memory contents are displayed on the LCD to allow display of figures, graphs, and pictures.

In character mode, the 8-bit parallel code for each character is converted to the corresponding dot pattern by the character generator in the control circuit boards and displayed on the LCD. The built-in character converts generates 192 characters including 160 JIS characters and 32 special pattern characters. An additional character generator for character patterns required by the user can also be mounted.

Model	Controller	Refresh RAM	External ROM	LCD module to be driven
CB1020R	HD61830 x 1 pc	Up to 2k bytes	Up to 2k bytes	LM200, LM021, H2525
CB1026R	HD61830 x 1 pc	Up to 4k bytes	Up to 4k bytes	LM200, LM021, LM212, LM211YB
CB1030R	HD61830 x 2 pcs	Up to 4k bytes (both master and slave)	Up to 4k bytes (both master and slave)	LM215XB

Note 1: The control circuit boards are shipped with the generating frequency set for driving the following LCD modules. If any other LCD module is to be used, refer to 7.2.

Control circuit board	LCD module
CB1020R	LM200
CB1026R	LM211XB
CB1030R	LM215XB

Device to be provided separately by the user: Refresh memory RAM

Note 2: Prepare any of the following devices according to the application.

(1) Hitachi HM6116 (CMOS, 2k bytes static RAM) 1 pc
(2) Hitachi HM6116 (CMOS, 2k bytes static RAM) 2 pcs
(3) Hitachi HM6264 (CMOS, 8k bytes static RAM) 1 pc

Note 3: To prevent problems after completing equipment design, an operation check with a sample is recommended in the design stage.

Note 4: If control circuit boards are to be used differently from the instructions given in this manual,

2. CONTROL CIRCUIT BOARDS

2.1 CB1020R

CB1020R is equipped with a control LSI (HD61830×1 pc) and a socket for refresh memory (up to 2k bytes) CB1020R is suitable for use with graphic display modules LM200 (64×240 dots), LM021 (24×479 dots) and H2525 (20×239 dots). An additional character generator ROM (up to 2k bytes) can be mounted to cope with the user's own character patterns.

Note 1: CB1020R is shipped conditioned for driving the LM200. If any other LCD module is to be used, refer to 7.2.

Note 2: Device to be provided separately by the user:
Refresh memory Hitachi HM6116 (CMOS 2048×8 static RAM) or its equivalent: 1 pc

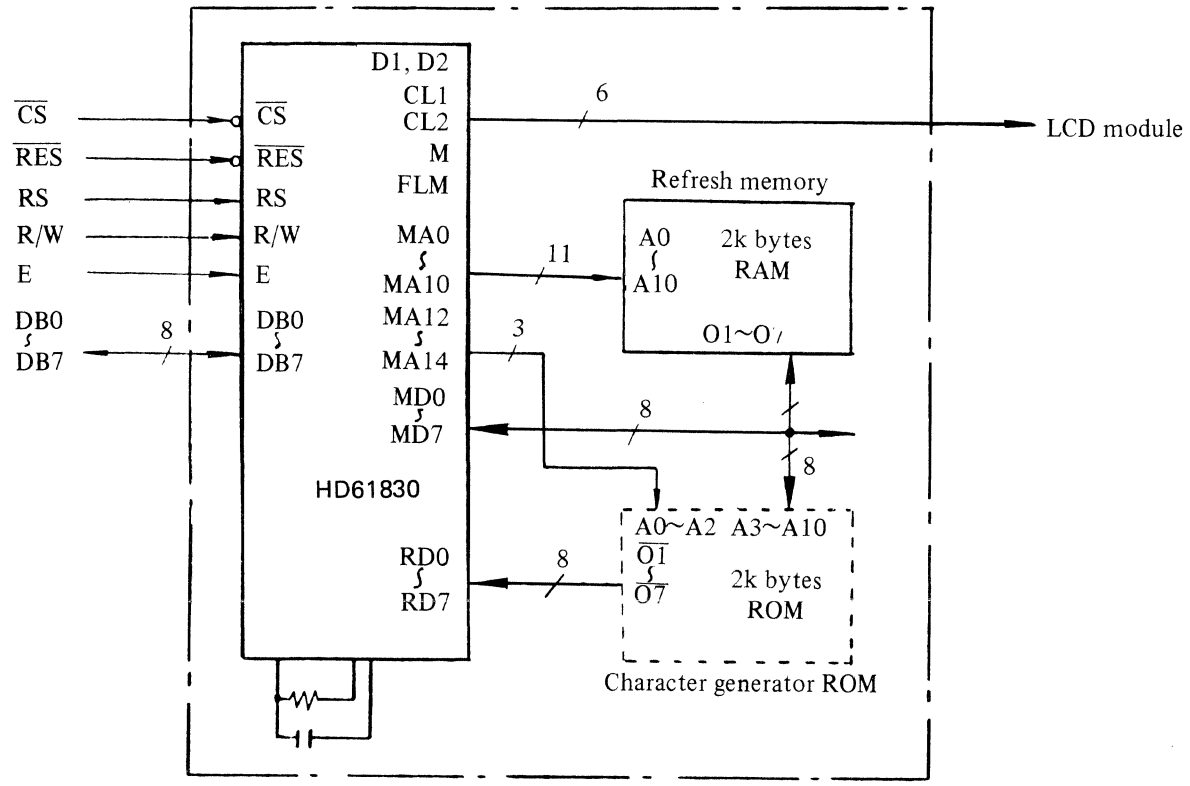


Fig. 2.1.1 CB1020R BLOCK DIAGRAM

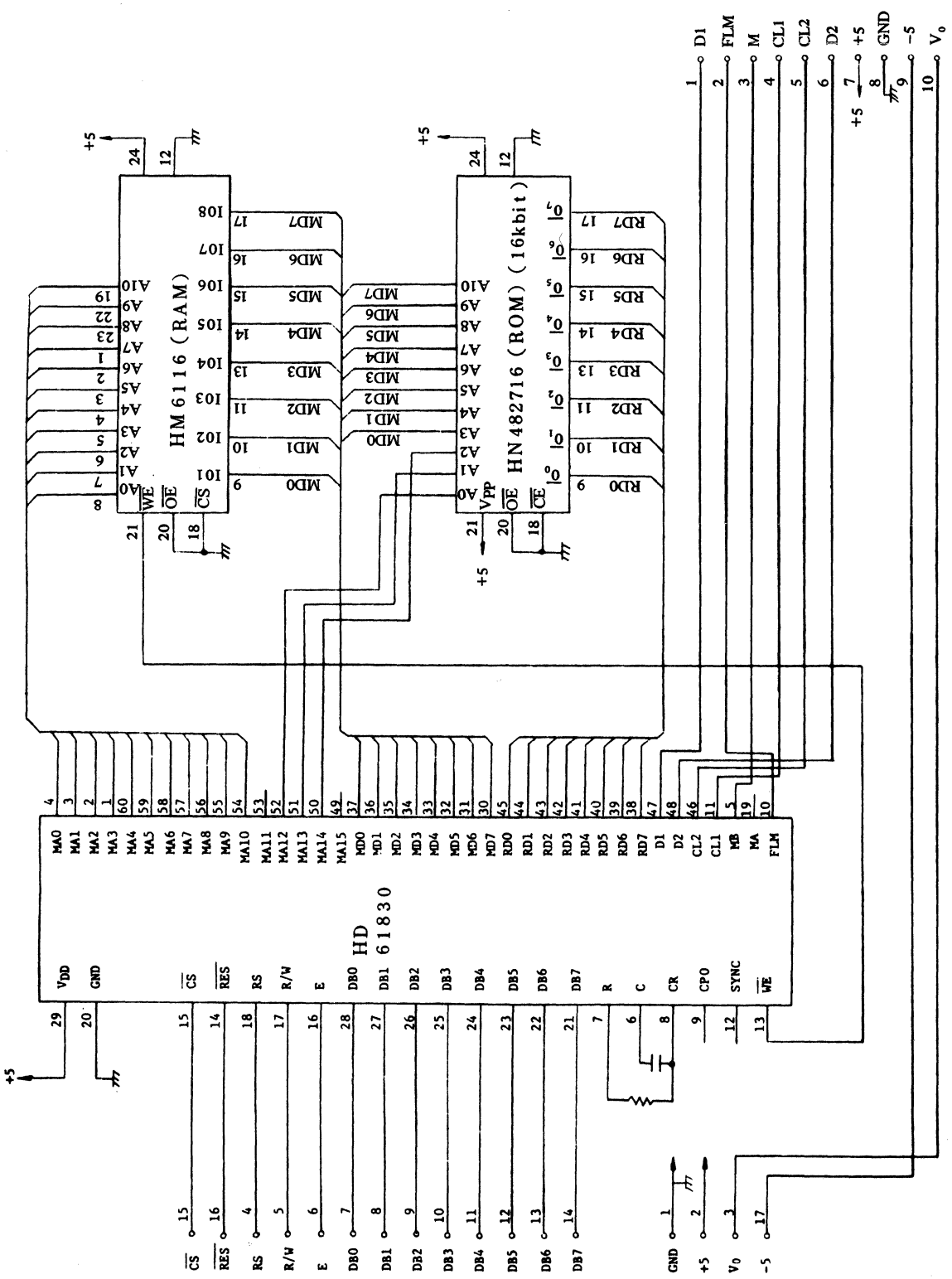


Fig. 2.1.2 CB1020R CIRCUIT DIAGRAM

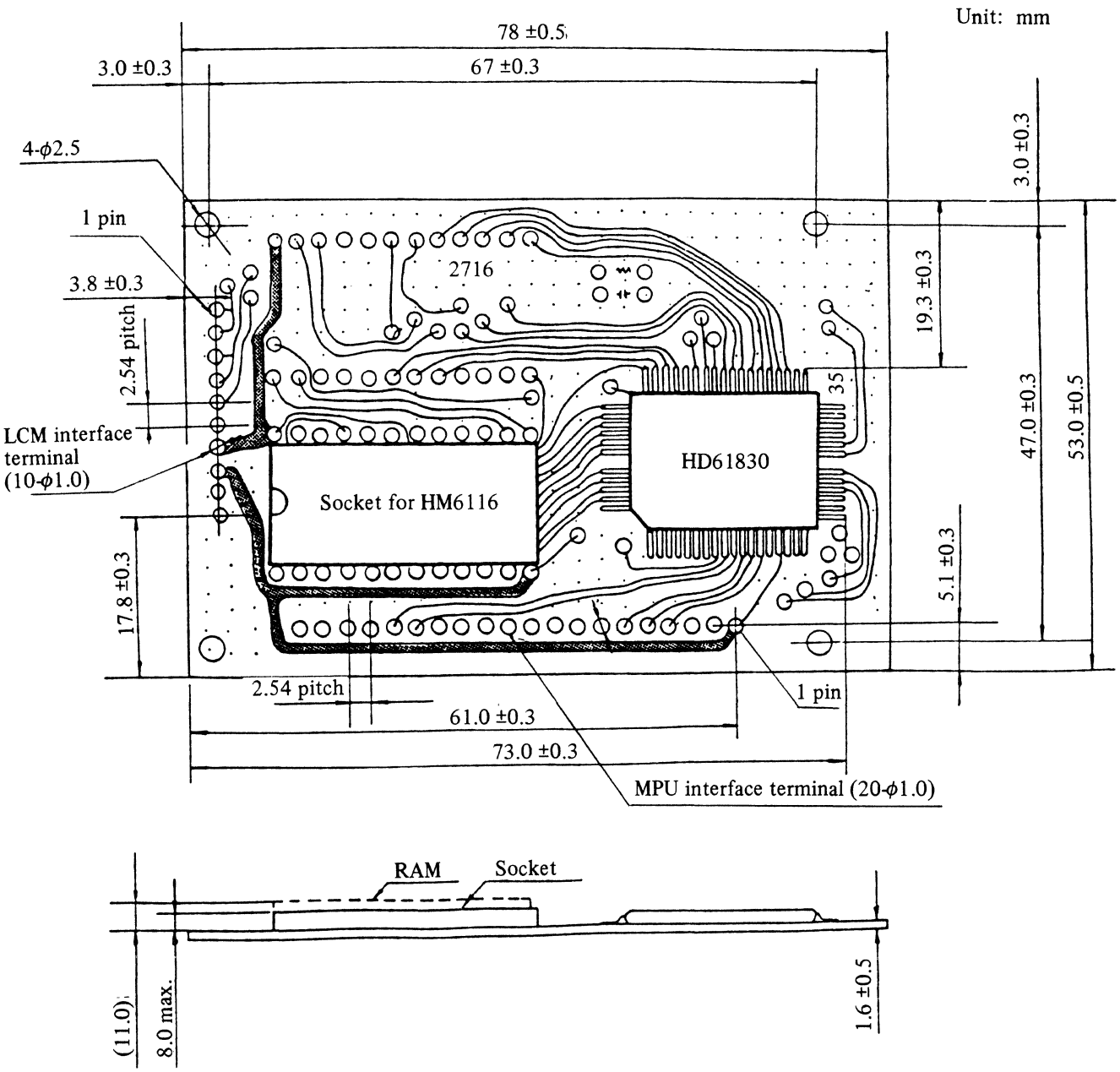


Fig. 2.1.3 DIMENSIONAL OUTLINE OF CB1020R

Table 2.1.1 CB1020R Interface Pin Arrangement

(1) LCD module interface

Pin No.	Signal name (Note 1)
1	D1
2	FLM
3	M
4	CL1
5	CL2
6	D2
7	V_{DD} (+5V)
8	V_{SS} (GND)
9	V_{EE} (-5V)
10	Vo

Note 1: Pin arrangement same as LM200.
Pin arrangement is different than LM021 and H2525.
Careful connection is necessary.
For pin arrangement of LM200, LM021, and H2525, see their catalogs.

(2) MPU interface

Pin No.	Signal name
1	V_{SS} (GND)
2	V_{DD} (+5V)
3	Vo (Note 1)
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	$\overline{CS}$
16	$\overline{RES}$
17	V_{EE} (-5V) (Note 1)
18	N.C
19	N.C
20	N.C

Note 1: Although V_O and V_{EE} are not used in CB1020R, they are provided for supply to the LCD module. (Fig. 5.1.)

(3) Interface hole diameter

1.0 mm holes are used in the MPU and LCD modules.

2.2 CB1026R

CB1026R is equipped with a control LSI (HD61830×1 pc) and a socket for refresh memory (up to 4k bytes) CB1026R is suitable for use with graphic display modules LM212 (48×640 dots), LM211 (64×480 dots) and LM200 (64×240 dots). An additional character generator ROM (up to 4k bytes) can be mounted to cope with the user's own character patterns.

Note 1: CB1026R is shipped with a generating frequency set for driving LM211. If any other LCD module is to be used, refer to 7.2.

Note 2: Prepare any of the following refresh memories according to the application:

(1) Hitachi HM6116 (CMOS, 2k bytes static RAM) 1 pc

(2) Hitachi HM6116 (CMOS, 2k bytes static RAM) 2 pcs

(3) Hitachi HM6264 (CMOS, 8k bytes static RAM) 1 pc

(Memory capacity of over 4k bytes cannot be controlled.)

A combination with other than the above refresh memories is not acceptable. Connect pins on the printed circuit board according to the indicated refresh memory (Table 3.1).

Note 3: Use Hitachi HN462732 as a character generator ROM.

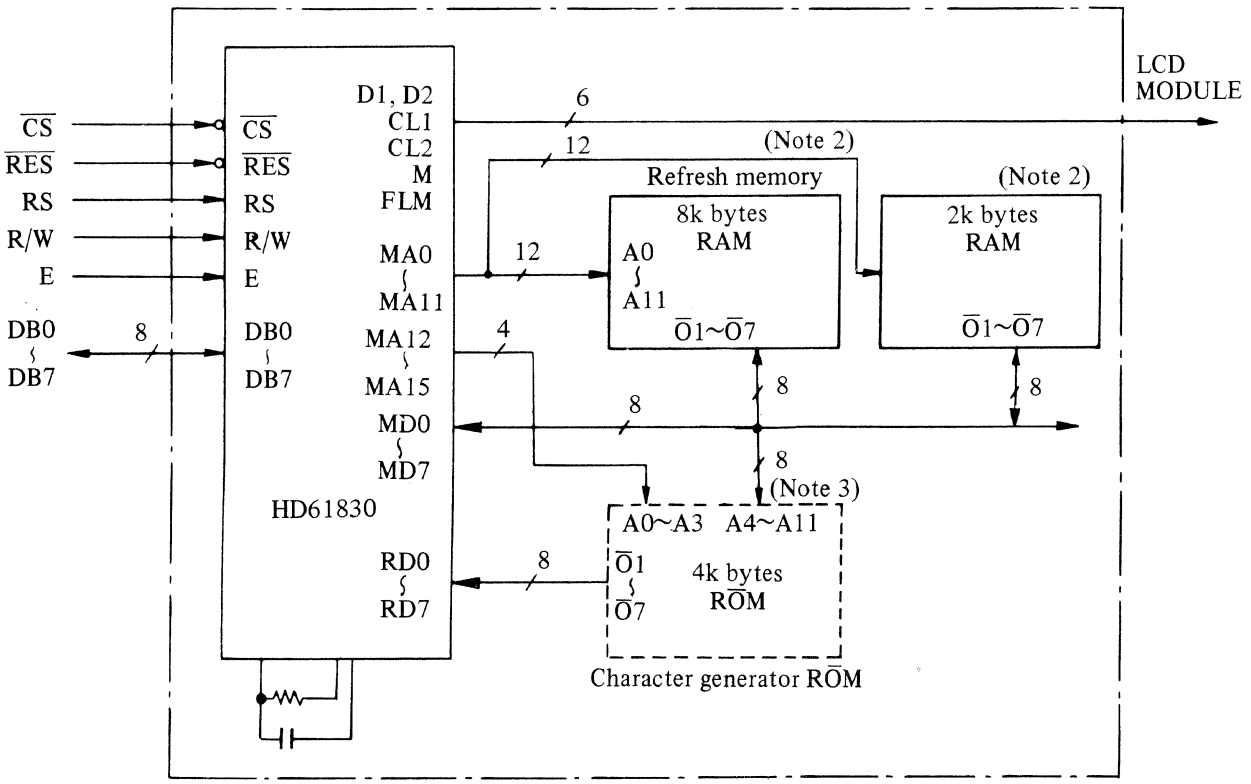
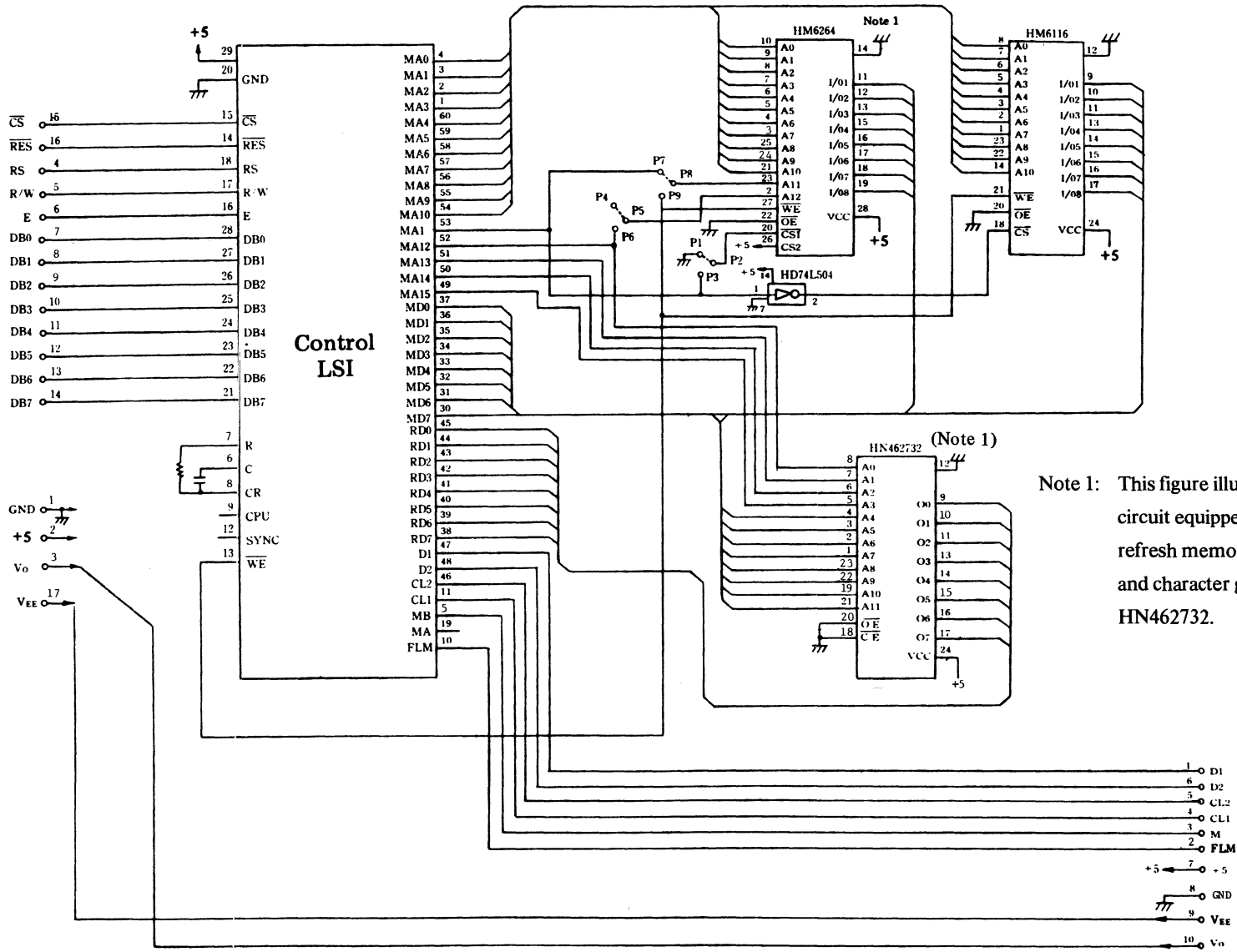
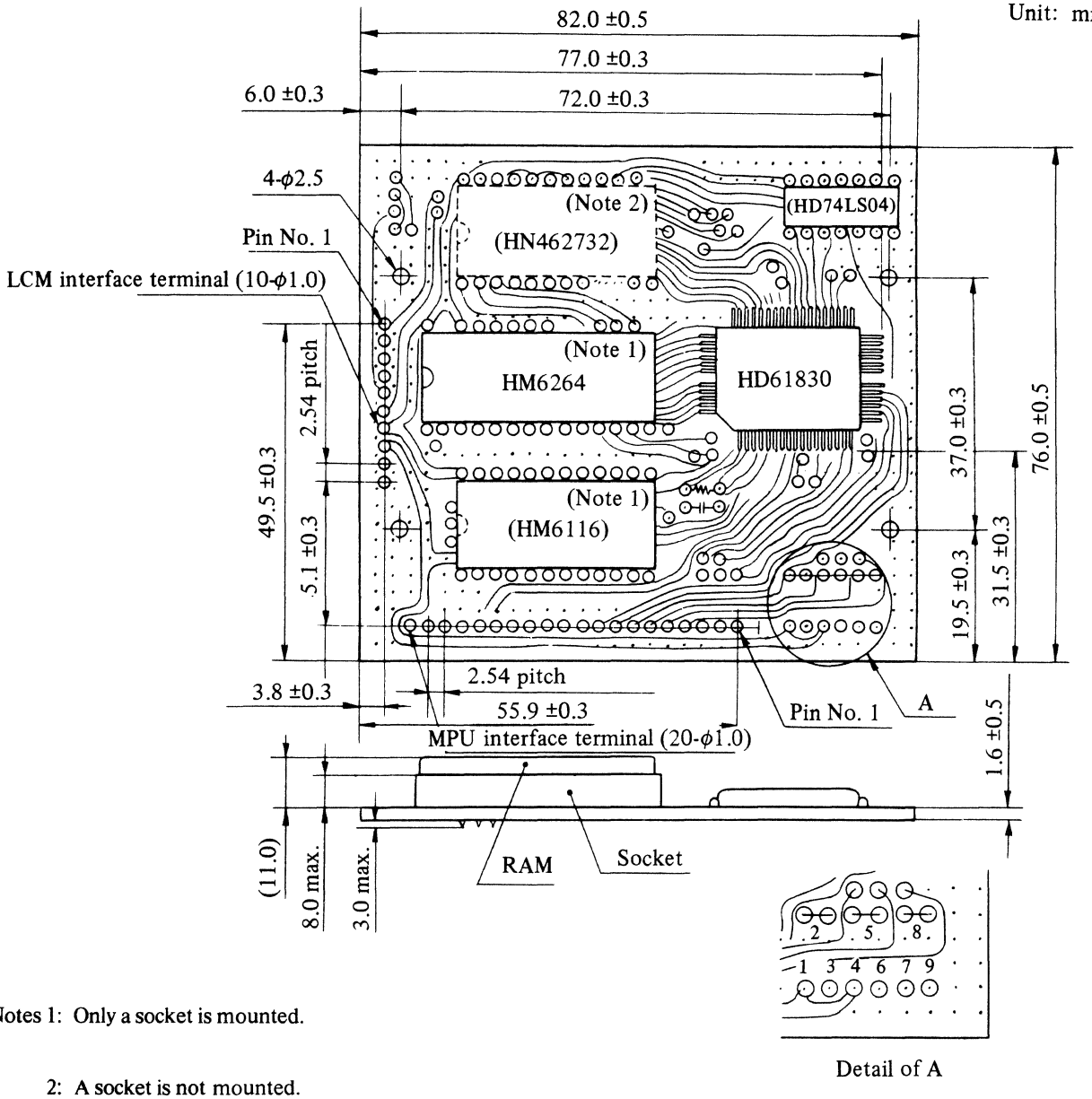


Fig. 2.2.1 CB1026R BLOCK DIAGRAM



Note 1: This figure illustrates a circuit equipped with refresh memory HM6264 and character generator HN462732.

Fig. 2.2.2 CB1026R CIRCUIT DIAGRAM



Detail of A

Notes 1: Only a socket is mounted.

2: A socket is not mounted.

Fig. 2.2.3 CB1026R DIMENSIONAL OUTLINE

Table 2.2.1 CB1026R Interface Pin Arrangement

(1) LCD module interface

Pin No.	Signal name (Note 1)
1	D1
2	FLM
3	M
4	CL1
5	CL2
6	D2
7	V_{DD} (+5V)
8	V_{SS} (GND)
9	V_{EE} (Note 2)
10	Vo (Note 2)

Note 1: Pin arrangement same as LM211 and LM200.
Pin arrangement is different than LM021 and H2525.
Careful connection is necessary.

Note 2: V_{EE} and Vo vary depending on an LCD module to be used. See LCD module catalog.

(2) MPU Interface

Pin No.	Signal name
1	V_{SS} (GND)
2	V_{DD} (+5V)
3	Vo (Note 1)
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	$\overline{CS}$
16	$\overline{RES}$
17	V_{EE} (Note 1)
18	N.C
19	N.C
20	N.C

Note 1: Although Vo and V_{EE} are not used in CB1026R, they are provided for supply to the LCD module. (Fig. 5.1.)
V_{EE} and Vo vary depending on an LCD module to be used. See LCD module catalog.

(3) Interface hole diameter

1.0 mm holes are used in the MPU and LCD modules.

2.3 CB1030R

CB1030R controls an LCD module, such as LM215 (128×480 dots), which divides the active area and is made of two CB1026R boards.

CB1030R uses two control LSIs (HD61830). These have a master-slave relationship.

For the block diagram and circuit diagram of the CB1030R, see the block diagram and circuit diagram of CB1026R.

Note 1: CB1030R is shipped with generating frequency set for driving LM215. If any other LCD module is to be used, refer to 7.2. CB1030R can also be used with LM212, LM211, LM200, LM021, and H2525. The pin arrangement is only the same as LM215.

Note 2: Prepare any of the following refresh memories according to the application:

(1) Hitachi HM6116 (CMOS, 2k bytes static RAM) 1 pc

(2) Hitachi HM6116 (CMOS, 2k bytes static RAM) 2 pcs

(3) Hitachi HM6264 (CMOS, 8k bytes static RAM) 1 pc

(Memory capacity of over 4k bytes cannot be controlled.)

Master and slave can be independently composed of RAM(s).

(Example: Master: one HM6264 chip; Slave: two HM6116 chips)

A combination with other than the above refresh memories is not acceptable. Connect pins on the printed circuit board using the indicated refresh memory (Table 3.1).

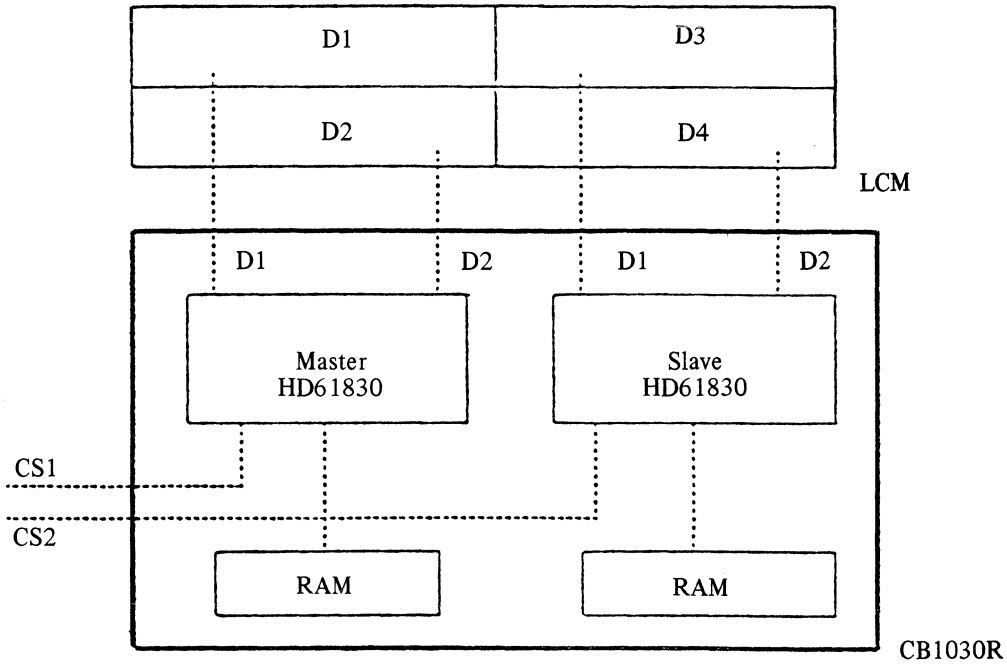


Fig. 2.3.1 RELATIONSHIPS BETWEEN CB1030R AND SCREEN AREA DIVISION (EXAMPLE WITH LM215)

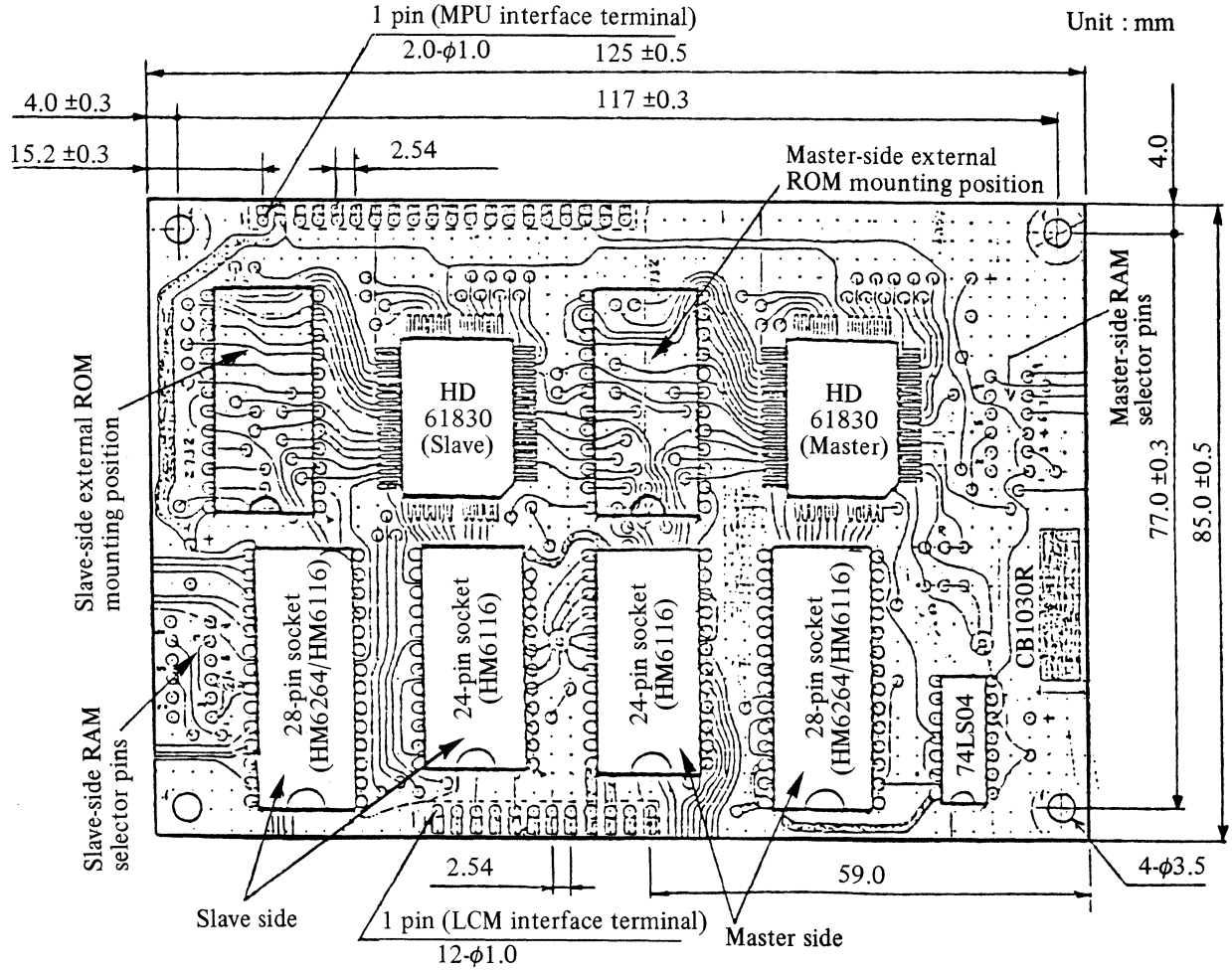


Fig. 2.3.2 CB1030R DIMENSIONAL OUTLINE

Table 2.3.1 CB1030R Interface Pin Arrangement

(1) LCD module interface

Pin No.	Signal name (Note 1)
1	D1
2	D2
3	FLM
4	M
5	CL1
6	CL2
7	D3
8	D4
9	V_{DD}
10	V_{SS}
11	V_{EE}
12	Vo

(2) MPU interface

Pin No.	Signal name
1	V_{SS} (GRD)
2	V_{DD} (+5V)
3	Vo
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	CS1 (Note 2)
16	RES
17	V_{EE}
18	CS2 (Note 2)
19	N.C
20	N.C

Note 1: Pin arrangement same as LM215XB.
Pin arrangement is different than LM021, LM211XB, LM200 and H2525. Careful connection is necessary.

Note 2: CB1030R uses two HD61830 chips. CS1 and CS2 are provided for chip selection.
CS1 = 0 (L) Selects master HD61830.
CS2 = 0 (L) Selects slave HD61830.
Input signals other than CS1 and CS2 are connected in common to both HD61830s.
When CB1030R is not selected, set CS1 and CS2 to level 1 (H).

3. EXPLANATION OF EACH PART

3.1 HD61830

This is a special control LSI for the graphic LCD module. It generates the timing signal and controls the data for LCD modules.

Selection between graphic and character modes as well as LCD drive conditions must be initialized through the data bus (DB0 to DB7). For initialization, see 8. The control LSI also has active area scroll, bit set, and bit clear functions.

For details, see HD61830 catalog.

3.2 Refresh Memory

The refresh memory, a static RAM, stores display data. In character mode operation, the character data is written as 8-bit parallel code in this RAM. Display is controlled by the address (MA0 to MA11) from HD61830. Read data is converted to the corresponding dot pattern by the character generator ROM in HD61830 (or an external character generator ROM) for display on the LCD.

In graphic mode, the HD61830 dot pattern is written in this RAM for display.

For correspondence between the RAM address and the active area, see 9.

Reading from or writing in this RAM is carried out through HD61830. Direct MPU reading or writing is impossible.

3.3 RAM Selections for Use with CB1026R and CB1030R

The following three selections are available for combination of RAMs that can be mounted in the CB1026R and CB1030R.

(1) HM6116 (2k bytes) ×1 pc

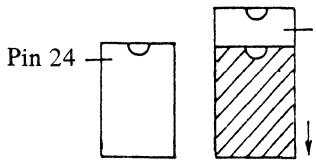
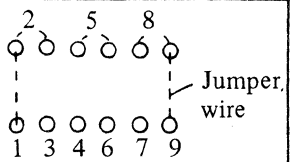
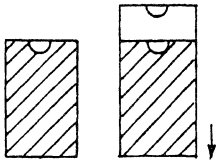
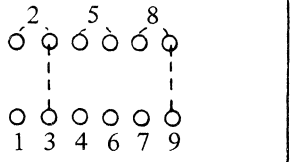
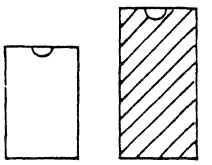
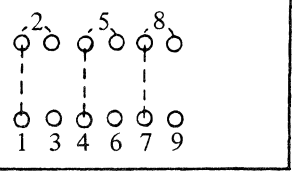
(2) HM6116 (2k bytes) ×2 pcs

(3) HM6264 (8k bytes) ×1 pc

(Memory capacity of over 4k bytes cannot be controlled.)

Correspondence between RAM combinations and pin connections are shown in Table 3.1 below. Each pin connection for each combination of the above three must be provided by connecting pins on the printed circuit board with jumper wires (Table 3.1).

Table 3.1 RAM and Pin Connections

RAM	Socket in which RAMs are mounted	Pin connections
2k-bytes RAM x 1 pc.		
2k-bytes RAM x 2 pc.		
8k-bytes RAM x 1 pc.		

3.4 Character Generator ROM

This is an external ROM (Hitachi HN462732 or its equivalent) to be mounted when the user requires special character patterns. It controls up to 4k bytes, or patterns for 512 characters*. For the pattern generation method, see Fig. 13.1 CB1020R uses Hitachi HN462716 ROM, which controls up to 2k bytes, or its equivalent.

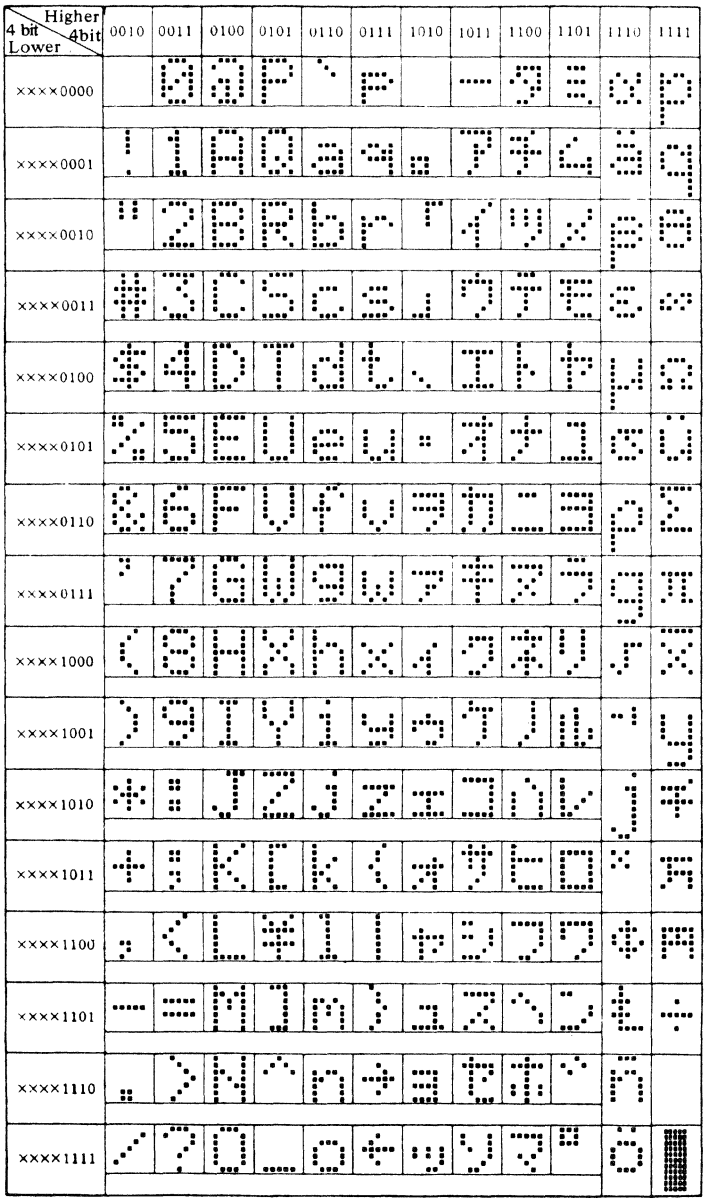
Use of both internal character generator ROM and external ROM is inhibited (ROM to be used must be designated at initialization). To use the external ROM, all patterns to be used must be generated.

* The number of character patterns varies depending on Vp (vertical character pitch) and Hp (horizontal character pitch) specified.

3.5 Patterns Generated by Character Generator ROM in HD61830

Table 3.2 shows the character patterns generated by the internal ROM.

Table 3.2 HD61830 Font Table



Every code beginning with 0000 or not defined is displayed as blank.

4. INTERFACE EXAMPLES WITH MPUs

Figures 4.1 to 4.3 show interface examples with various MPUs. In designing an actual interface circuit, consider the timing chart shown in 12.

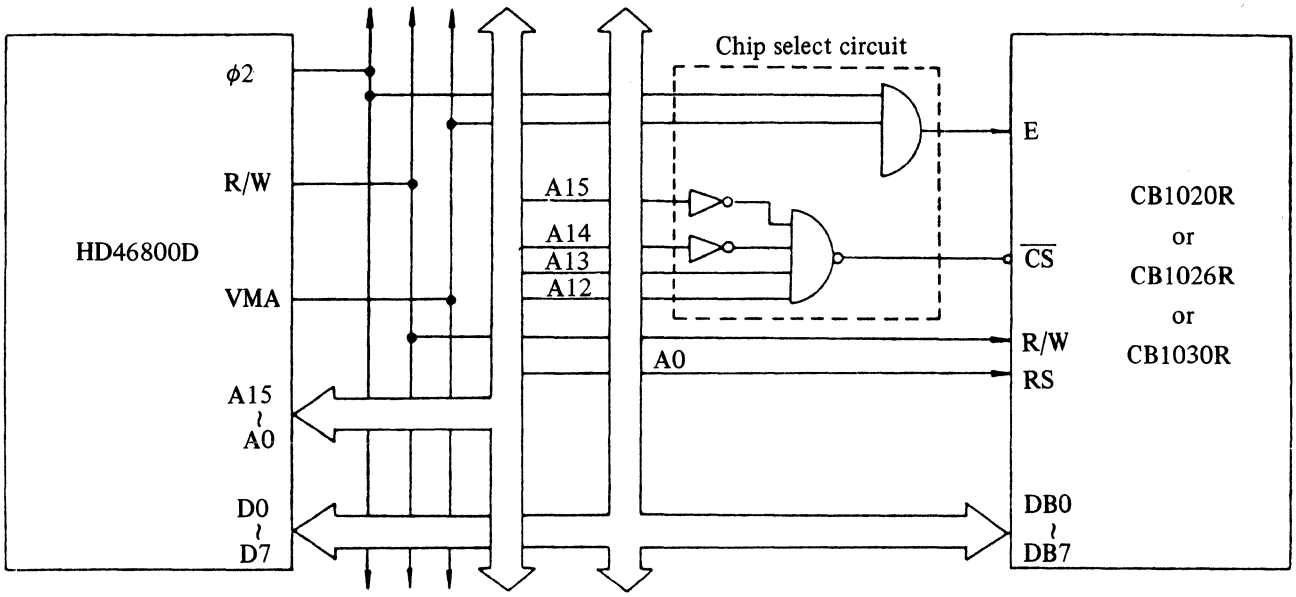


Fig. 4.1 Interface example with HD46800

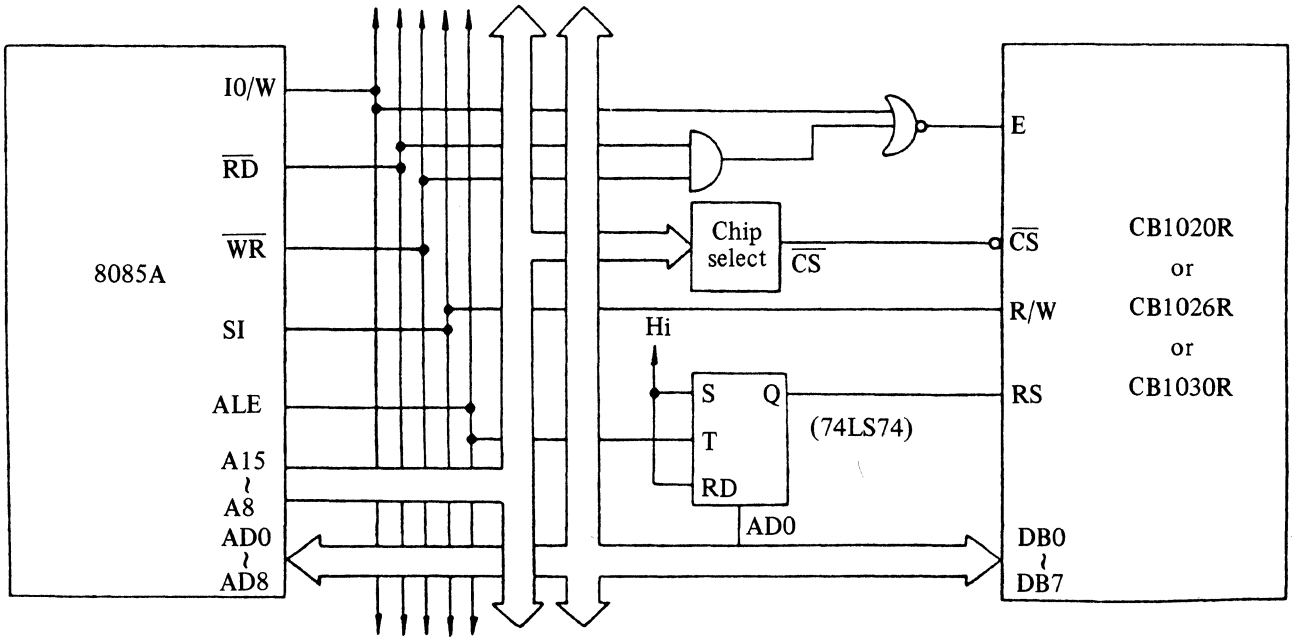


Fig. 4.2 Interface example with 8085A

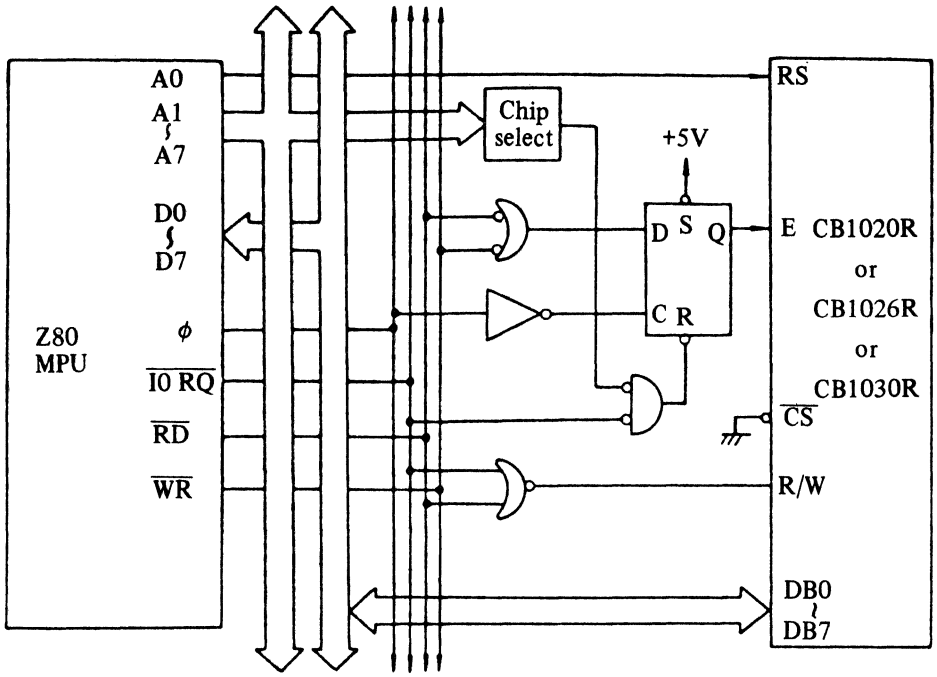


Fig. 4.3 Interface example with Z80

5. LCD DRIVE VOLTAGE SUPPLY

All power voltages are supplied to the control circuit board and are output to the LCD (Fig. 5.1). V_O and V_{EE} simply pass the control circuit board.

The method in Fig. 5.2 is recommended for supplying LCD drive voltage V_O. The method in Fig. 5.3 may be used because V_O and V_{EE} are used only in the LCD module. Select either way according to the control circuit board mounting position and the variable resistor location.

For recommended drive voltages, see LCD module catalog.

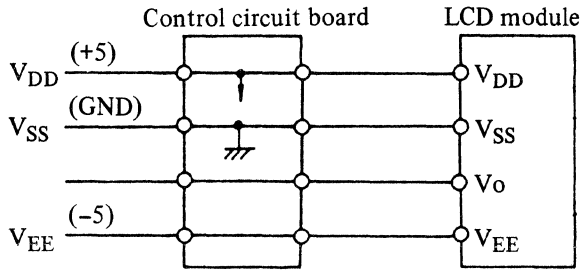
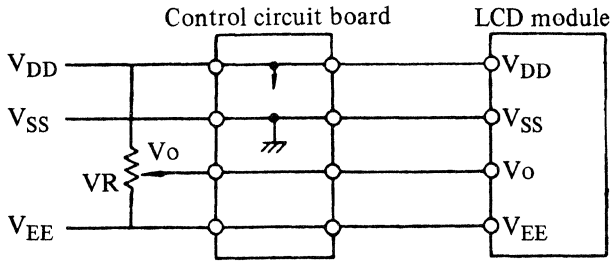
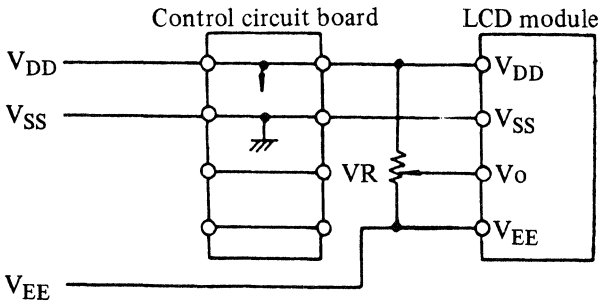


Fig. 5.1 Power Lines



VR: 10kΩ~20kΩ

Fig. 5.2 Example of Variable Resistor Connection (1)



VR: 10kΩ~20kΩ

Fig. 5.3 Example of Variable Resistor Connection (2)

6. POWER SEQUENCE AND $\overline{\text{RES}}$ PIN

6.1 Power Sequence

CMOS LSIs are used in the control circuit board and LCD module. Always supply the power as in the sequence in Figure 6.1. Each input signal must be kept at GND level until the +5 V source voltage is stabilized. If a signal is input before stabilization of the source voltage, latch-up may occur.

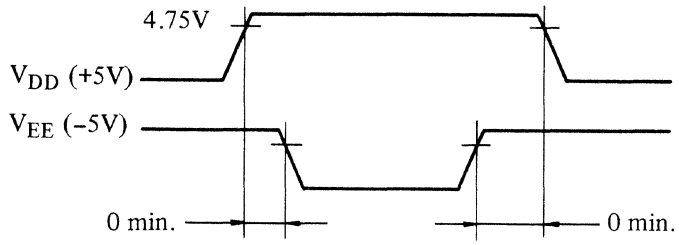


Fig. 6.1 Power Sequence

6.2 $\overline{\text{RES}}$ Pins

$\overline{\text{RES}}$ pin has these functions:

(1) Clearing each register in HD61830.

(2) Resetting BUSY flag (enabling E signal receiving)

Because the BUSY flag status is unstable after power on, provide the C and R reset circuit (Fig. 6.2). $\overline{\text{RES}}$ signal input during operation clears the registers in the control LSI causing LCD driving conditions to become faulty. An abnormal display will result. Although reinitialization restores normal status, $\overline{\text{RES}}$ signal input during operation must be avoided. If $\overline{\text{RES}}$ signal is applied during operation, execute initialization immediately after $\overline{\text{RES}}$ signal input. $\overline{\text{RES}}$ signal pulse width must be 1 μs through 2 ms to avoid disturbance of LCD driving conditions during $\overline{\text{RES}}$ signal input.

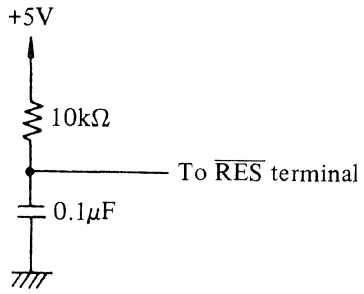


Fig. 6.2 Reset Circuit

7. INITIALIZATION AND BUSY SIGNAL

7.1 Initialization

Table 7.1 shows HD61830 instructions. Table 7.2 shows mode data bit functions.

In initialization, always designate the display mode and LCD drive conditions (instructions No. 1 through No. 4 in Table 7.1).

Designation of other instructions is not necessary at initialization.

Setting (writing in each register) in HD61830 is effected by designation of the register number after writing the data. This setting method is similar to the CRT controller (CRTC).

Fig. 7.1 shows an example of the initialization flowchart.

Since the register pointer designates the same register until setting of a new register number, sequential register number specifications are necessary for initializing data writing.

Table 7.3 shows an example of initializing data for LM211, LM021, and H2525.

Caution: Instructions No. 2 through No. 4 in Table 7.1 must be executed immediately after power on and must not be changed during operation. Reset conditions after $\overline{RES}$ signal input must be the same as those first specified.

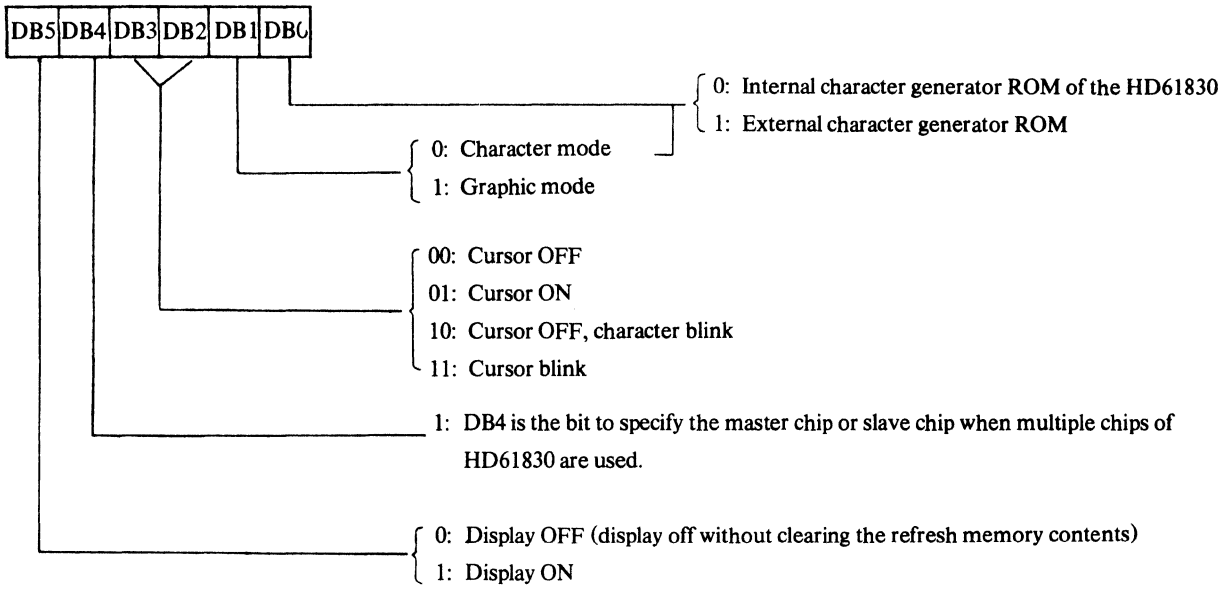
Table 7.1 HD61830 Instruction List

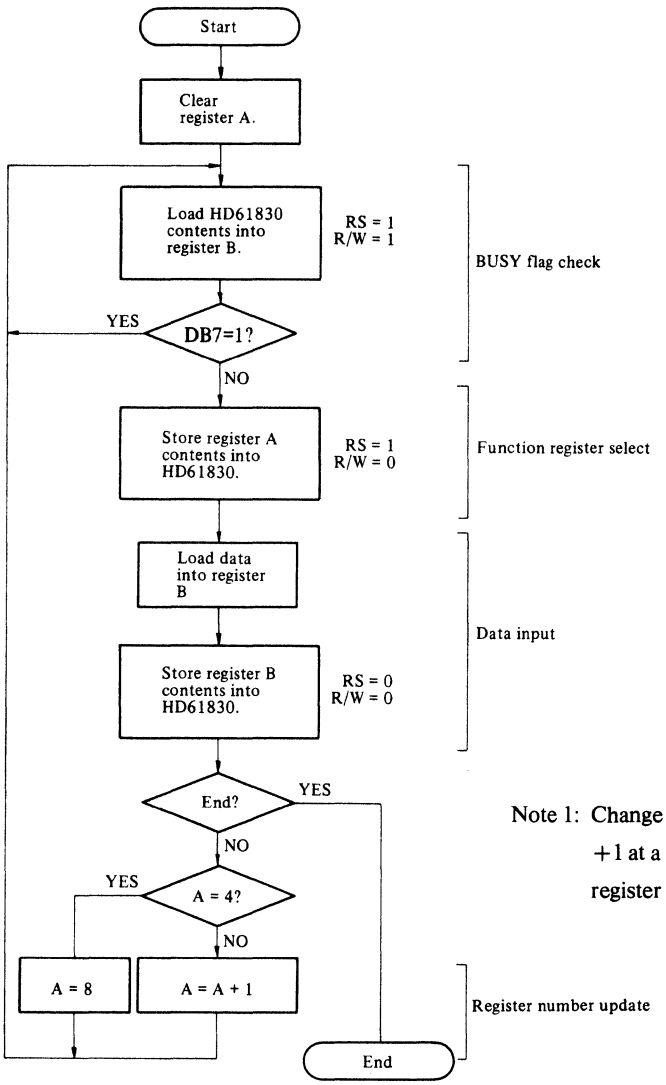
Register									Data									
No.	R/W	RS	DB7~DB4	DB3	DB2	DB1	DB0	Function	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	0	0	0	0	0	Mode control	0	0	0	0	Mode data (Note 1)					
2	0	1	0	0	0	0	1	Vertical/horizontal character pitch	0	0	(Vp – 1) B				0	(Hp – 1) B		
3	0	1	0	0	0	1	0	Number of characters per line/ number of bytes	0	0	0	(HN – 1) B						
4	0	1	0	0	0	1	1	Number of vertical dots	0	0	0	(NX – 1) B						
5	0	1	0	0	1	0	0	Cursor position	0	0	0	0	0	0	(CP – 1) B			
6	0	1	0	1	0	0	0	Display starting address (least significant) (Lower)	0	0	Address data							
7	0	1	0	1	0	0	1	Display starting address (most significant) (Upper)	0	0	0	0	0	0	Address data			
8	0	1	0	1	0	1	0	Cursor address (least significant)	0	0	Address data							
9	0	1	0	1	0	1	1	Cursor address (most significant) (Upper)	0	0	0	0	0	0	Address data			
10	0	1	0	1	1	0	0	Refresh memory write	0	0	Character code/bit data							
11	0	1	0	1	1	0	1	Refresh memory read	1	0	Refresh memory data							
12	0	1	0	1	1	1	0	Bit clear	0	0	0	0	0	0	0	(BN) B		
13	0	1	0	1	1	1	1	Bit set	0	0	0	0	0	0	0	(BN) B		
14	–	–	–	–	–	–	–	BUSY signal read	1	1	BF	*	*	*	*	*	*	*

Notes 1. See Table 7.2.

2. HP: Specify 6, 7, or 8.
3. HN $\leqq$ 128: If the active area is divided, specify the number of characters/number of bytes per block (an even number of 2-128).
4. NX = Number of duties $\leqq$ 128
5. BF = 0 (ready to receive signal E)
   BF = 1 (during internal processing)

Table 7.2 Mode Data





Note 1: Change the register number normally +1 at a time, but in No. 5 to No. 6 of Table 7.1, register numbers are not continuous.

Fig. 7.1 Initialization Flowchart (Example)

Table 7.3 Initializing Data (Example)

No.	LM211XB		LM200		LM021		H2525	
	Character	Graphic	Character	Graphic	Character	Graphic	Character	Graphic
1	34	32	34	32	34	32	34	32
2	75	77	75	77	75	77	75	77
3	27	1F	27	1F	27	1F	27	1F
4	3F	3F	1F	1F	17	17	13	13
5	07	07	07	07	07	07	07	07
6	00	00	00	00	00	00	00	00
7	00	00	00	00	00	00	00	00
8	00	00	00	00	00	00	00	00
9	00	00	00	00	00	00	00	00

Notes: 1. Numbers same as in Table 7.1.
2. Character mode uses 6 × 8 dots/character and internal ROM.
3. Graphic mode uses 256 dots per line.

7.2 BUSY Signal

HD61830 has an independent oscillator to generate the LCD drive timing. All HD61830 internal operations and refresh memory read/write operations use the clock signal generated by this internal oscillator. This oscillator operates in perfect a synchronism with the clock on the MPU side. In processing instructions from the MPU and data writing, data bus contents are first latched in the buffer register in HD61830 by the enable signal (E signal) and then processed according to the internal clock signal. Generally, the time equivalent to two internal clock puleses (3.5 μs min) or more is necessary for one operation (processing), so that the processing speed does not match the MPU. To ensure processing of received instructions and data, the flag to inhibit the E signal is set in HD61830 during LSI processing.
BUSY signal duration depends on the function in Table 7.4.

Table 7.4 BUSY Signal Duration

Function	BUSY		
	Generation/ Nongeneration	max.	min.
Setting register No.	None	1μs	–
Setting data in register	Generation	2 × t_{CL2}	t_{CL2}
Refresh RAM read/write	Generation	(2 + Hp) t_{CL2}	2 × t_{CL2}
Bit write/clear	Generation	2 (Hp + 1) t_{CL2}	(2 + Hp) t_{CL2}

Notes: 1. t_{CL2} (internal clock signal cycle)
LM215XB ..... 0.87 μs (typ.)
LM212 ..... 0.87 μs (typ.)
LM211XB ..... 1.1 μs (typ.)
LM200 ..... 2.2 μs (typ.)
LM021 ..... 3.0 μs (typ.)
H2525 ..... 3.5 μs (typ.)

2. Hp (horizontal character pitch) 6, 7 or 8

3. The time from the E signal falling edge (↘) is indicated.

To ensure the correct HD61830 internal operation, send and receive instructions while checking the BUSY signal. If obliged to use the equipment without checking the BUSY signal, allow for at least three times the duration listed in Table 7.4 below.

BUSY time varies with frequency f_{CL2} of CB1026R, whose t_{CL2} is set for use in the LM211. Consult a Hitachi office when using the CB1026R in other than LM211.

BUSY signal is used only in HD61830 and not directly output from LSI. Checking the HD61830 busy state from the MPU side uses the BUSY signal read function in the sequence shown in Fig. 7.2. Fig. 7.1 shows a flowchart example.

Minimum E signal cycle time of 1.0 μs in 12 is the time for a BUSY check and register number setting (Fig. 7.2). It does not mean that HD61830 is able to process an instruction within a minimum cycle time of 1 μs.

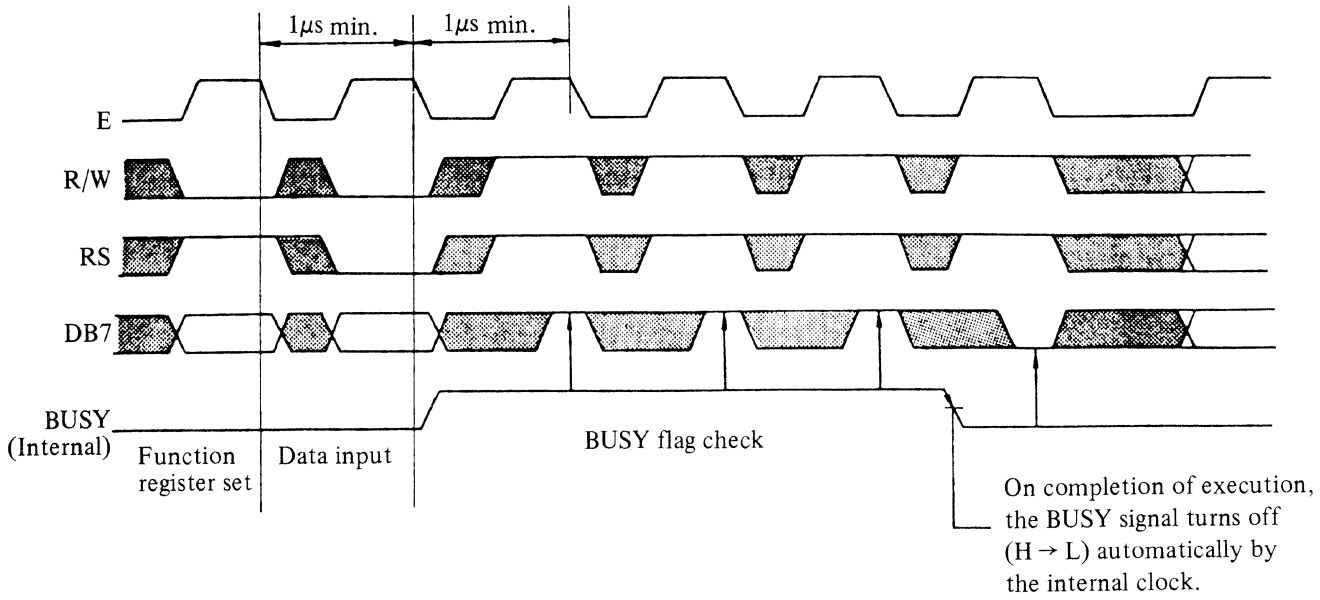


Fig. 7.2 BUSY Check Sequence

8. INSTRUCTION CODE

8.1 Mode Control (Table 7.1, No. 1)

Specify the HD61830 operation mode.

This instruction controls the character/graphic mode, cursor on/off/blink, master/slave, and display on/off.

When DB1 is set to 1, and DB0, DB2 and DB3 are set to 0, HD61830 is set to the graphic mode. The character generator and cursor function are disabled.

When DB1 is set to 0, HD61830 is set to the character mode. The character generator designation (DB0) and cursor control (DB2, DB3) are enabled.

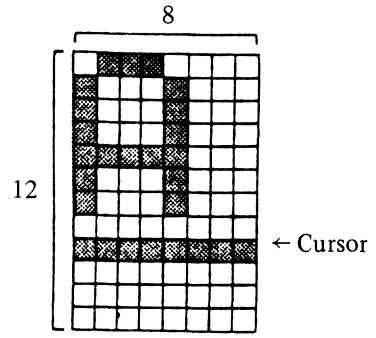
The blink cycle is determined by the internal oscillator frequency. It is generally 0.2 to 0.4 sec.

8.2 Vertical/Horizontal Character Pitch (Table 7.1, No. 2)

When HD61830 is used in character mode, specify the number of dots per character in the vertical and horizontal directions. The number of dots in the horizontal direction will be 6, 7, or 8. Since the character generator font consists of 5×7 or 5×11 dots, specifying 12 in the vertical direction and 8 in the horizontal direction would cause the character display to be justified to the left top (Fig. 8.1).

Use hex for number specification.

Data 0 for dots other than the character portion and cursor is generated in HD61830.



Range of Vp and Hp:

$7 \leqq (Vp-1) \leqq 15$
$5 \leqq (Hp-1) \leqq 7$] Character mode

$(Vp-1) = **$ (invalid)
$5 \leqq (Hp-1) \leqq 7$] Graphic mode

Fig. 8.1 display Pattern (Example)

8.3 Number of Characters per Line/Number of Bytes (Table 7.1, No. 3)

Specify the number of characters per line in the horizontal direction and the number of bytes for graphic display.

Calculating formulas follow.

Character mode:

$$H_N = \frac{\text{Number of dots in horizontal direction}}{Hp}$$

Graphic mode:

$$H_N = \frac{\text{Number of dots in horizontal direction}}{8}$$

Use hex for specification.

If the calculated HN is not an integer, raise the fractional part for specification.

Always specify an even number. Specifying an odd number is inhibited.

For the module whose active area is divided into 2 blocks, specify the number of characters/number of bytes per block. For LM211, for example, the active area is divided as in Fig. 8.2. Specify 240÷8=30 (1E in hex).

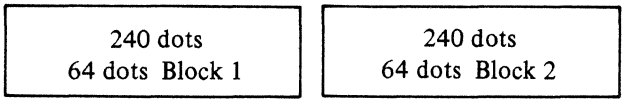


Fig. 8.2 (1) LM211 Active Area Division

If $H_N \times H_P$ exceeds the number of dots, the character at the right end of the active area is displayed completely. The character at the left end may be imperfectly displayed (Fig. 8.2 (2)).

8.4 Number of Vertical Dots (Fig. 7.1, No. 4)

Specify in hex the number of dots in the vertical direction.

Specify the number of dots irrespective of graphic mode or character mode.

Specifications of the number of characters per line/number of bytes and the number of vertical dots determine the LCD drive timing. The specifications must match those of the LCD module as much as possible. Specifying values deviating greatly from LCD module specifications may cause display flickering or fading.

For a module divided into two blocks in the vertical direction, specify the number of vertical dots in one block. For example, the LM200 is divided as shown in Fig. 8.3, and so specify 32 (1F in hex).

If HN=36, HP=7 and number of horizontal dots=240:

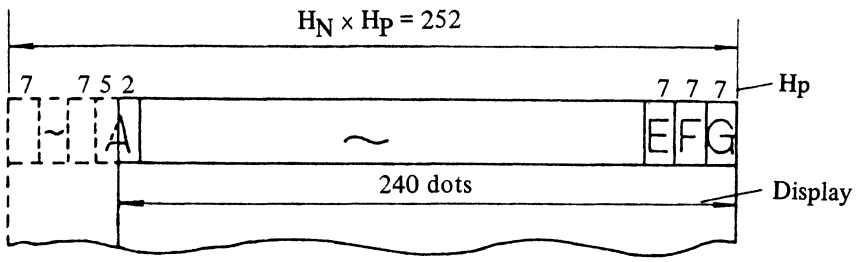


Fig. 8.2 (2) Display Example for HN×HP Number of Dots

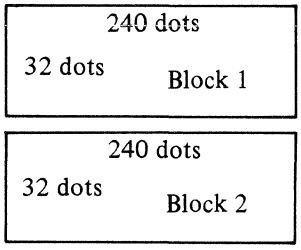


Fig. 8.3 LM200 Active Area Division

8.5 Cursor Position (Table 7.1, No. 5)

Specify the cursor lighting position. Observe VP≧CP.

If CP=8 is specified, the cursor is displayed on the 9th line from the top (Fig. 8.1).

The number of cursor dots in the horizontal direction is the same as the HP value.

Blinking also occurs in the range of VP and HP in the vertical and horizontal directions.

8.6 Start Address (Table 7.1, No. 6 and No. 7)

Specify the most significant 8 bits and least significant 8 bits of the display start address. Usually, specify $(0000)_{16}$. Changing the display start address enables display to start from an arbitrary address in the refresh memory. Scrolling is thus easy.

In any of LM211, LM200, LM021, H2525, and LM212, the start address data is displayed at the top left of the active area.

For scrolling details, see 11.

8.7 Cursor Address (Table 7.1, No. 8 and No. 9)

Specify an address in the refresh memory.

Because the cursor address is automatically incremented (+1), address setting is unnecessary after setting the first address for continuous data writing in continuous addresses. If addresses are discontinuous, an address setting is required each time.

The cursor address includes a lower address (8 bits) and an upper address. In setting the cursor address, observe the following instructions:

1	When both a lower address and upper address are to be set:	Set the lower address first, and then the upper address.
2	When a lower address only is to be set:	After setting the lower address, set the upper address again.
3	When an upper address only is to be set:	Set the upper address. It is not necessary to set the lower address again.

The cursor address counter is a 16-bit up-counter with the set and reset function. When the N'th bit changes from 1 to 0, the (N+1)'th bit counts up.

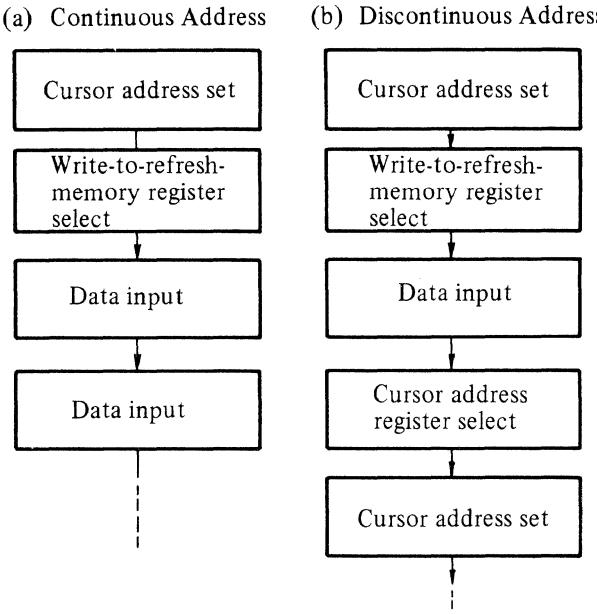
If a lower address is so set that MSB (8th bit) of the lower counter changes from 1 to 0, LSB (1st bit) of the upper counter counts up. In setting the cursor address, handle the setting of lower address and higher address as consecutive instructions of two bytes.

8.8 Writing in Refresh Memory (Table 7.1, No. 10)

This function writes the display data.

Usually, this function is executed in a pair with the cursor address setting in the sequence shown in Fig. 8.4.

In the graphic mode, the data is inverted in writing and display (Fig. 8.5). Either invert the data for each byte at the time of data preparation or use the inversion program (Fig. 8.6).



In specifying an internal ROM in the character mode, code patterns not defined in Table 3.2 are all displayed as blank.

Fig. 8.4 Data Writing Sequence

8.9 Reading from Refresh Memory (Table 7.1, No. 11)

This function reads the refresh memory contents for input to the MPU. The reading sequence is similar to that in Fig. 8.4.

Data inversion in read/write into the MPU does not occur.

The data read immediately after address setting becomes insignificant because of circuit operation. It shall thus be ignored. Data read the second time is normal. The cursor advances 1 position as the data is read once.

Data being read is always the one behind the cursor.

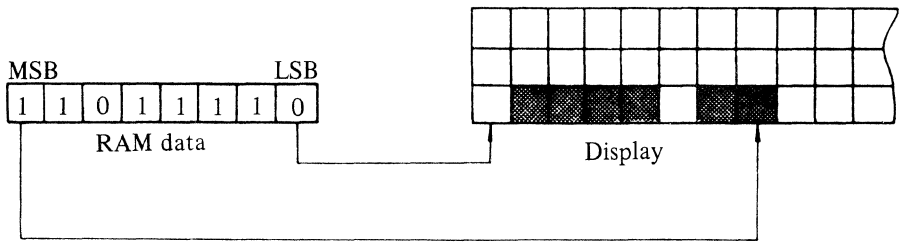


Fig. 8.5 Data Inversion in Graphic Mode

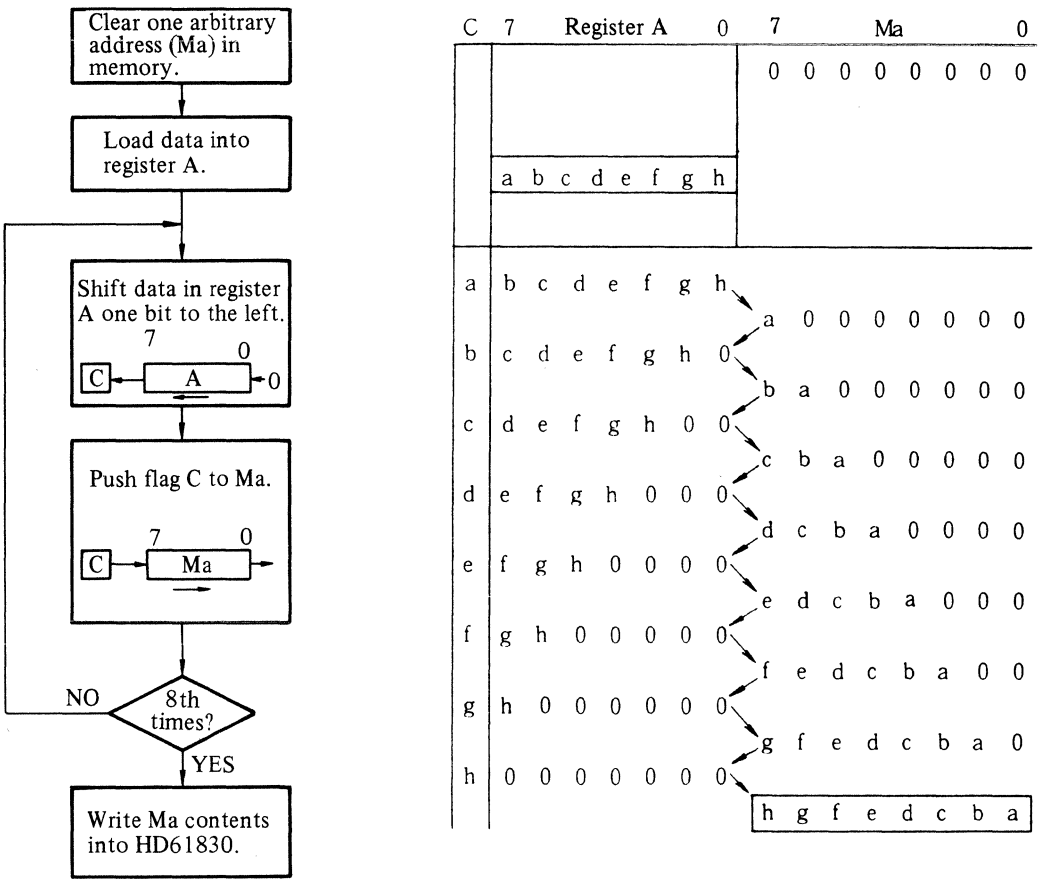


Fig. 8.6 Data Inversion

8.10 Bit Clear and Bit Set (Table 7.1, No. 12 and No. 13)

Only one bit of the data (8 bits) at the address designated by the address counter can be operated. These functions must be used in paired state with the cursor address set. In character mode, the character pattern changes. In the graphic mode, only one dot changes. If bit set and bit clear are repeated without address setting, the address is incremented one by one.

Correspondence between the bit data and display is shown in Fig. 8.7.

8.11 BUSY Signal Read (Table 7.1, No. 14)

This function checks if HD61830 is busy.

The BUSY signal is output to DB7 when this function is executed. Otherwise, the BUSY signal is not output from the LSI. DB6 through DB0 contains insignificant data.

For sure MPU instruction execution, write a program to proceed with processing while executing the BUSY check.

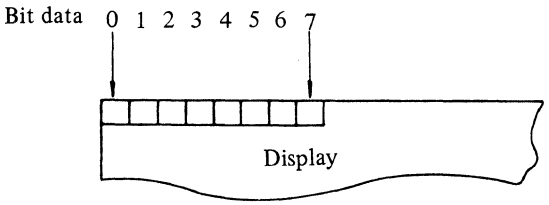


Fig. 8.7 Relationship between Bit Data and Display

9. RELATIONSHIPS BETWEEN CURSOR ADDRESS, START ADDRESS, REFRESH RAM, AND LCD DISPLAY

Character mode ..... Fig. 9.1

Graphic mode ..... Fig. 9.2

For active area division, the addresses are electrically contiguous vertically and horizontally (Figs. 9.1 and 9.2).

In character mode, the most significant 4 bits of the address (MA12-MA15) is used for scanning the vertical pitch. External control is thus impossible.

In graphic mode, the horizontal character pitch (HP) is limited to 8 dots and the RAM data is displayed as it is one the LCD. Data is inverted for each byte (8.8).

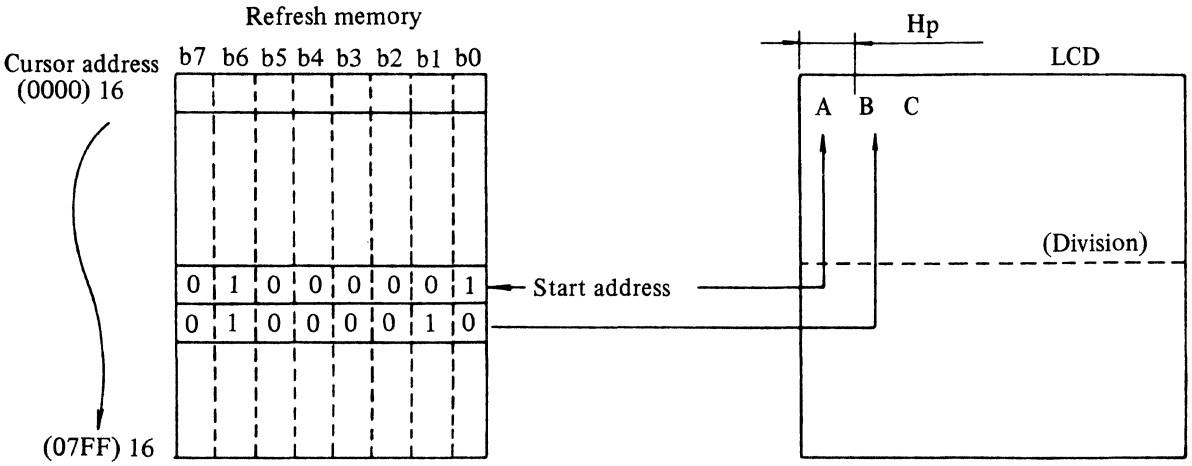


Fig. 9.1 Character Mode

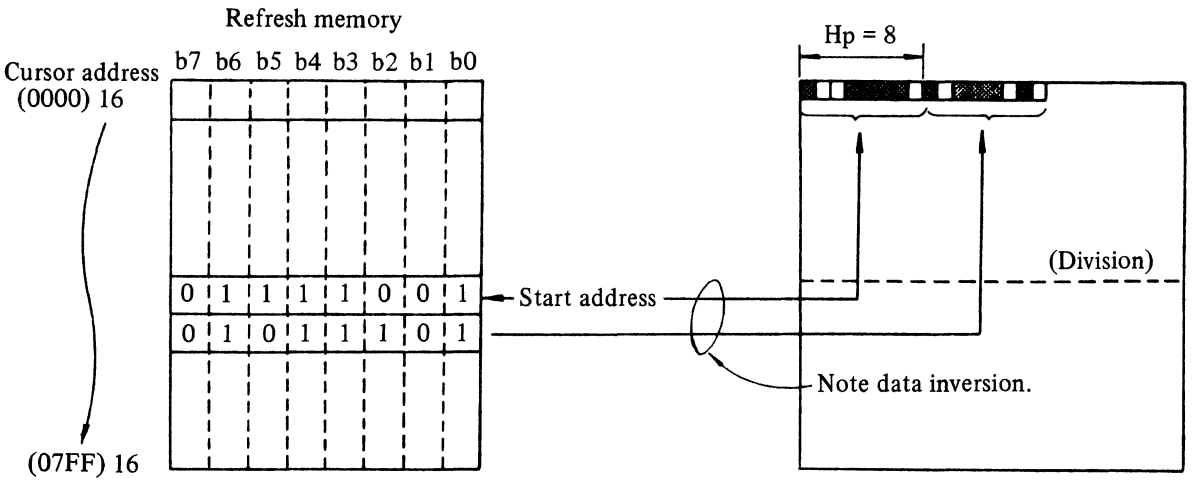


Fig. 9.2 Graphic Mode

10. SCROLLING

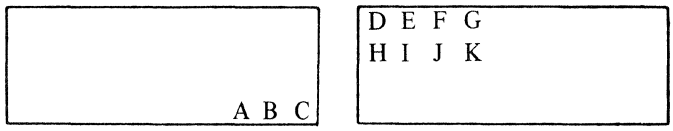
Start address is usually set to $(0000)_{16}$. The active area can be scrolled by changing this value.
Pay attention to these points:

(1) In character mode, scrolling in one character unit (VP value for the number of lines) is possible.

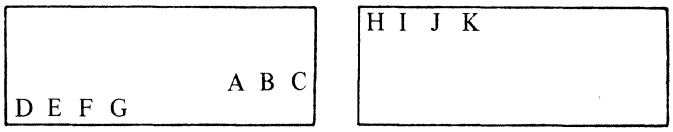
(2) In graphic mode, scrolling in one byte unit is possible.

(3) The least significant address and the most significant address of the refresh RAM are apparently co tiguous to provide the endless form. The range of addresses displayed in the active area is the start a dress + (HN×NX/VP).
(In the graphic mode, VP=1. When the number of dots of the LCD module is different from t number expressed by HN and NX, this is not applied.)
Information in all RAM addresses can be displayed irrespective of the display size.

(4) If the active area is horizontally divided into 2 blocks in a module like LM211, changing the start address causes the data in the top line of the right block to be shifted to the bottom line of the block. (Fig.10.1.)
Note this point in scrolling.



Before start address change



After start address change

Fig. 10.1 Scrolling for Horizontal Division (Example)

(5) For horizontal scrolling in the graphic mode, HN must be specified as 2^N (N = an integer of 1, If other than 2^N, the display at scrolling time will become unclear.

(6) Display shifting in scrolling
When the start address is changed by one address, the whole display is shifted by one character byte (8 bits) to the left. Left end data is displayed at the right end of the preceding line.

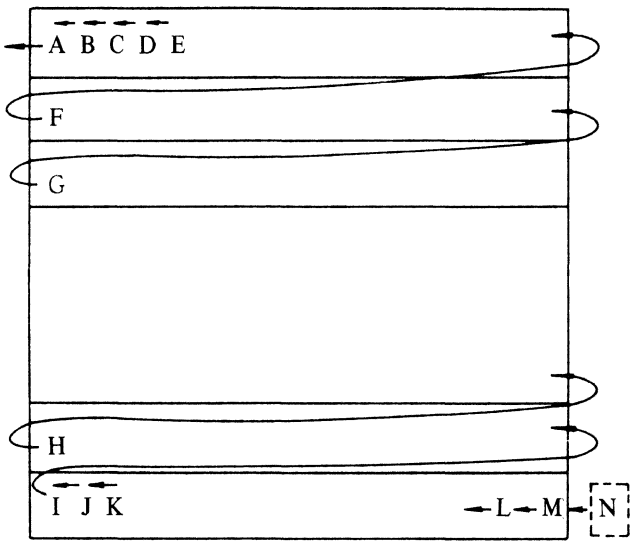


Fig. 10.2 Display Shifting in Scrolling

11. ELECTRICAL CHARACTERISTICS

11.1 Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage	V_{DD}	0 ~ 7.0	V
Input voltage	V_T	0 ~ V_{DD}	V
Operating temperature	Topr	0 ~ +50	°C
Storage temperature	Tstg	-20 ~ +70	°C

Notes: (1) V_{EE} is not used in the control circuit board.
V_{EE} varies depending on models of the LCD module. For details, see the individual catalog of the LCD module to be used.

(2) V_O range must be $V_{DD} \geqq V_O \geqq V_{EE}$

11.2 Electrical Characteristics

(V_{DD} = 5V ±5%, GND = 0V, Ta = 0°C to 50°C)

Item	Symbol	Test condition	min.	typ.	max.	Unit	Terminal
Input voltage (TTL compatible)	V_{IH}		2.2	–	V_{DD}	V	DB0~7, CS, E, R/W, RS, $\overline{RES}$ (Note 3)
	V_{IL}		0	–	0.8	V	
Output voltage (TTL compatible)	V_{OH}	I_{OH} = -0.6mA	V_{DD}-0.4	–	V_{DD}	V	DB0~7
	V_{OL}	I_{OL} = +1.6mA	0	–	0.4	V	
Output voltage	V_{OHC}	I load = ±0.6mA	V_{DD}-0.4	–	V_{DD}	V	M, FLM, CL1, CL2, D1, D2
	V_{OLC}		0	–	0.4	V	
Input leak current	Iin		–	–	5	μA	
Output leak current	I_{OL}		–	–	10	μA	
Operating frequency	F_{CP1}		–	–	1	MHz	Note (1)
Power dissipation	P_W	V_{DD} = 5V, Ta = 25°C	–	–	30	mW	Note (2)

Notes: (1) Internal frequency

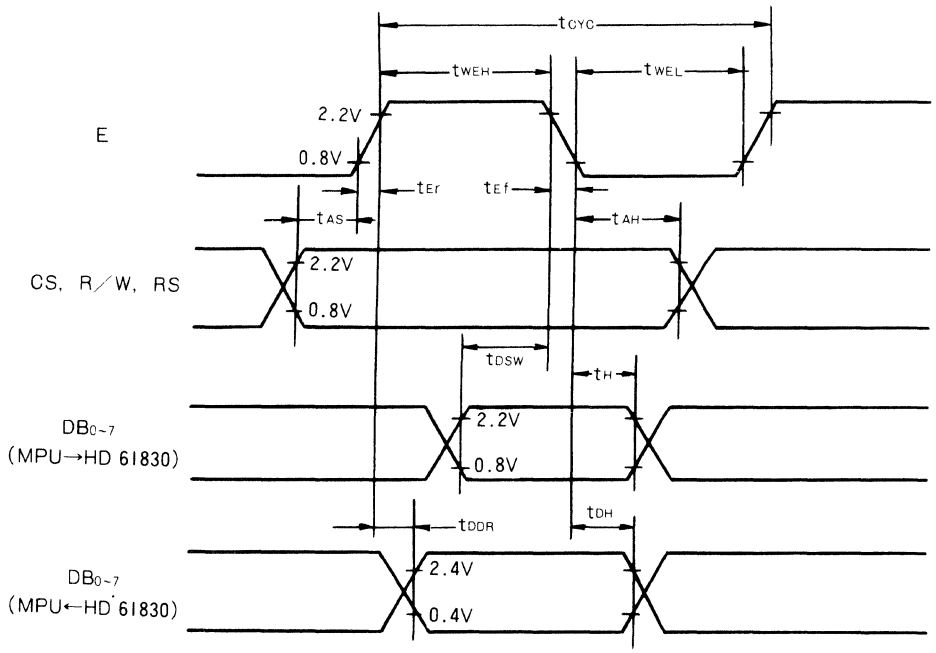
(2) Refresh RAM current consumption is excluded. 60 mW max. for CB1030R.

(3) $\overline{RES}$: V_{IH} = 3.0 V, V_{IL} = 0.8 V

12. TIMING CHARACTERISTICS

12.1 Interface Timing (MPU ←→ Control circuit board)

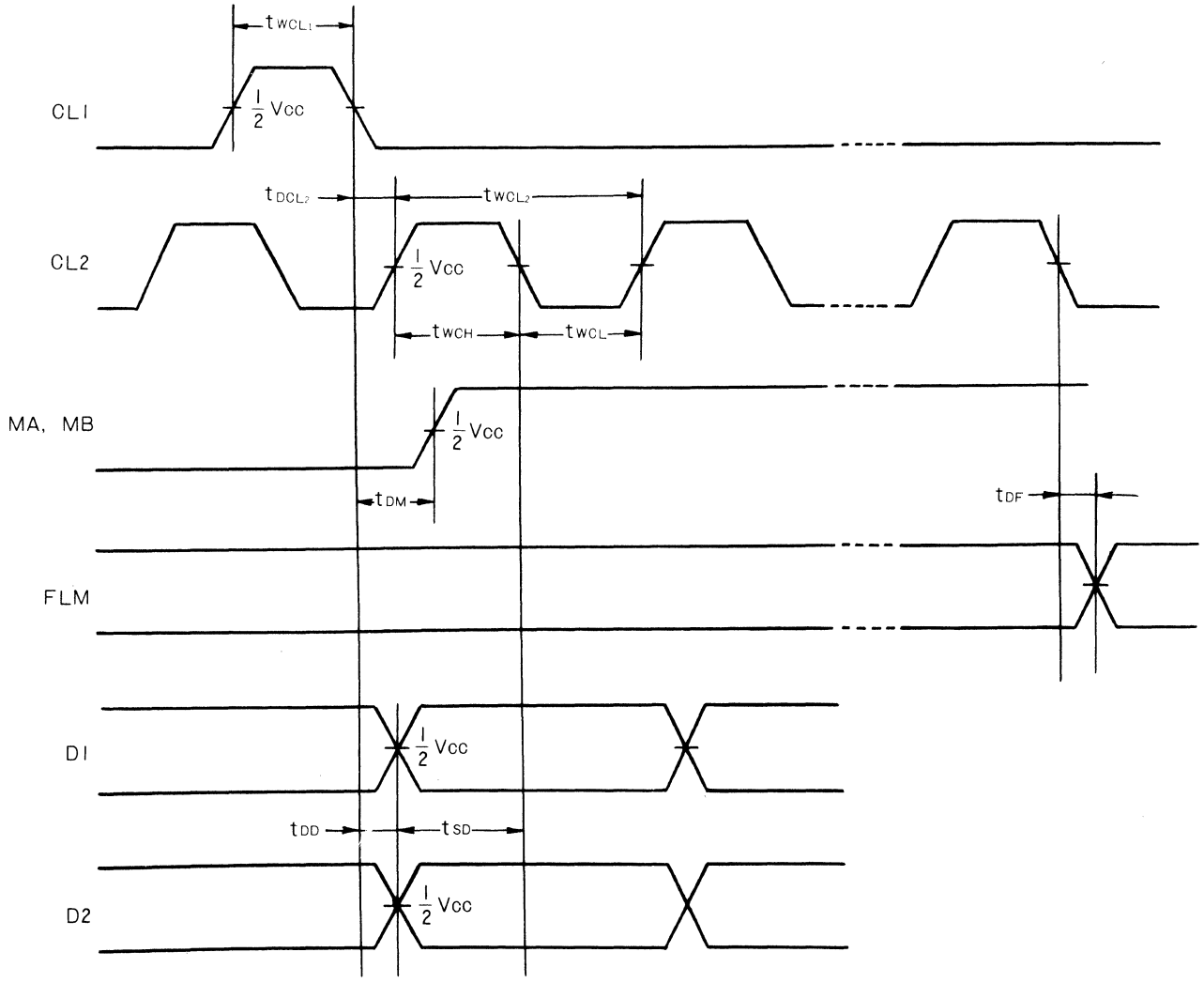
Item		Symbol	min.	typ.	max.	Unit
Enable cycle time		t_{CYC}	1.0	–	–	μs
Enable pulse width	H level	t_{WEH}	0.45	–	–	μs
	L level	t_{WEL}	0.45	–	–	μs
Enable pulse rise time		t_{Er}	–	–	25	ns
Enable pulse fall time		t_{Ef}	–	–	25	ns
Setup time of CS, R/W, RS		t_{AS}	140	–	–	ns
Setup time of input data		t_{DIS}	225	–	–	ns
Data delay time		t_{DD}	–	–	225	ns
Hold time of data		t_H	10	–	–	ns
Hold time of CS, R/W, RS		t_{AS}	10	–	–	ns
Pulse width of $\overline{RES}$		t_{WRES}	1μs	–	2ms	–



12.2 Interface Timing (Control Circuit Board ⟶ LCD Module)

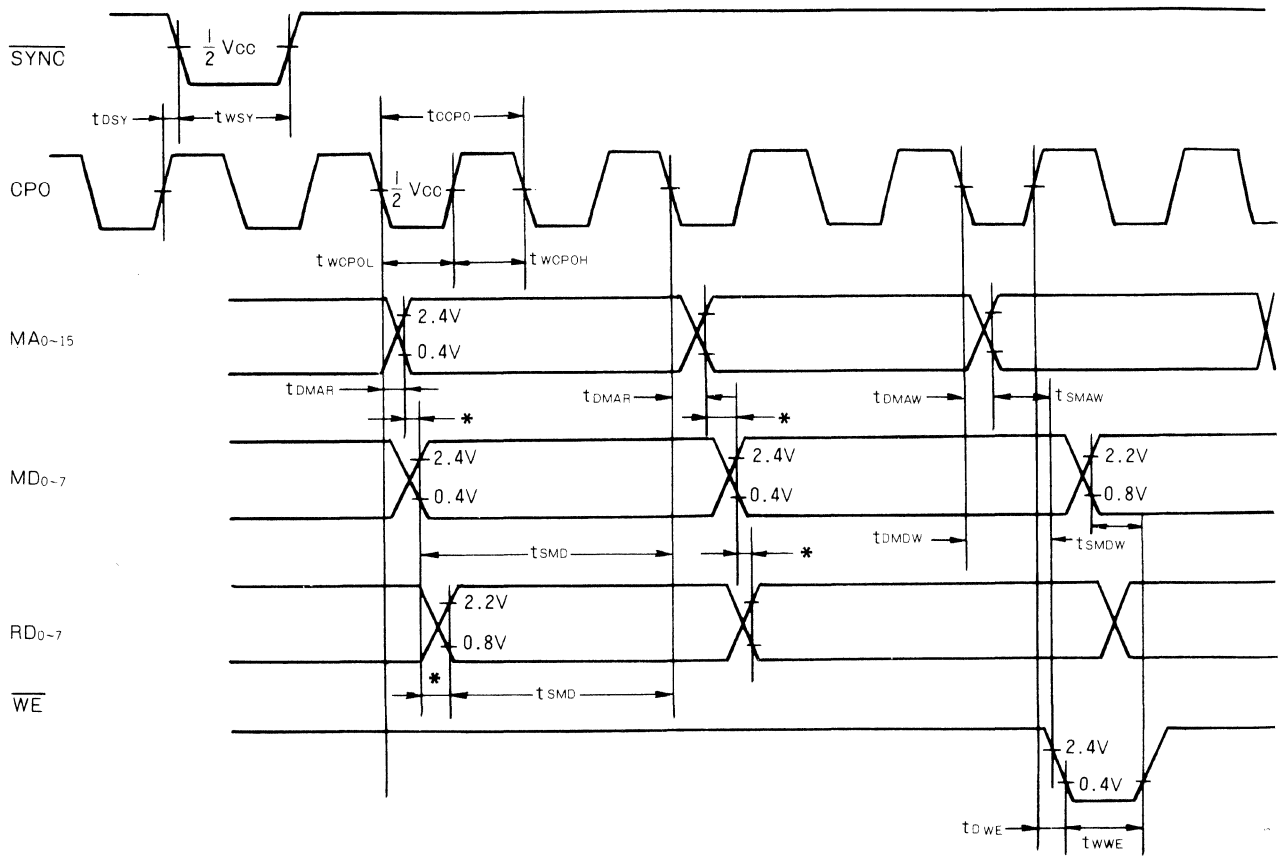
Item		Symbol	min.	typ.	max.	Unit
CL1 pulse width		t_{WCL1}	450	–	–	ns
CL2 delay time		t_{DCL2}	–	–	200	ns
CL2 cycle time		t_{WCL2}	900	–	–	ns
CL2 pulse width	H level	t_{WCH}	450	–	–	ns
	L level	t_{WCL}	450	–	–	ns
M delay time		t_D	–	–	300	ns
FLM delay time		t_{DF}	–	–	300	ns
Data delay time		t_{DD}	–	–	200	ns
Data setup time		t_{SD}	250	–	–	ns

Note (1) When output is no load.



12.3 Refresh RAM Access/External ROM Access Timing

The time is not directly output from the control circuit board and is described for reference.



Item		Symbol	min.	typ.	max.	Unit
$\overline{\text{SYNC}}$ delay time		t_{DSY}	–	–	200	ns
$\overline{\text{SYNC}}$ pulse width	L level	t_{WSY}	900	–	–	ns
Cycle time		t_{CCPO}	900	–	–	ns
CPO pulse width	H level	t_{WCPOH}	450	–	–	ns
	L level	t_{WCPOL}	450	–	–	ns
MA0–15 refresh time		t_{DMAR}	–	–	200	ns
Write MA0–15 address delay time		t_{DMAW}	–	–	200	ns
Write MD0–7 data delay time		t_{DMDW}	–	–	200	ns
Setup time of MD0–7, RD0–7		t_{SMD}	900	–	–	ns
Memory address setup time		t_{SMAW}	250	–	–	ns
Memory data setup time		t_{SMDW}	250	–	–	ns
$\overline{\text{WE}}$ delay time		t_{DWE}	–	–	200	ns
$\overline{\text{WE}}$ pulse width	L level	t_{WWE}	450	–	–	ns

Notes: (1) When output is no load.

(2) * is delay time of external ROM and refresh RAM.

13. EXTERNAL ROM PATTERN GENERATION

Fig. 13.1 shows the correspondence between the ROM address and data.
Write the 8-bit data corresponding to dot on/off for each address.
A0-A3 show the scanning address. To display the pattern of the external ROM, write the codes of the most significant 4 bits and least significant 4 bits (8 bits in total) (A3-A10) in the refresh RAM. A corresponding character pattern is then displayed on the LCD. The display range depends on the HP value.

HP = 6: Data at $\overline{0}6$ and $\overline{0}7$ is not displayed.
HP = 7: Data at $\overline{0}7$ is not displayed.
HP = 8: All data at $\overline{0}1$ through $\overline{0}7$ is displayed.

In CB1020R, address wiring is done for HN462716 (2k bytes EPROM). Maximum dots per character is 8×8. In CB1026 and CB1030R, address wiring is done for HN462732 (4k bytes EPROM).
The maximum number of dots per character is 8×8.

14. APPLICABLE CONNECTOR

Any connector whose pitch is 2.54mm and pin diameter is less than 0.9-0.8mm can be used.
The following connectors manufactured by Japan Aviation Electronics Industry, Ltd. are available.

PS-20PE-S4T1-PN1 (20 pins) for MPU interface
PS-10PE-S4T1-PN1 (10 pins) for LCD interface ..... For CB1020R and CB1026R
PS-12PE-S4T1-PN1 (12 pins) for LCD interface ..... For CB1030R

UPPER 4 bit / LOWER 4 bit	A10	A9	A8	A7	0								0								0	1
					0								0								0	1
					0								0								1	1
					0								1								0	1
A6 A5 A4 A3	A2	A1	A0		O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7		
0 0 0 0	0	0	0		1	1	1	1	0	0	0	0	0	1	1	1	0	0	0	0		
	0	0	1		1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0		
	0	1	0		1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0		
	0	1	1		1	1	1	1	0	0	0	0	1	0	0	0	1	0	0	0		
	1	0	0		1	0	1	0	0	0	0	0	1	0	1	0	1	0	0	0		
	1	0	1		1	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0		
	1	1	0		1	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0		
	1	1	1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
0 0 0 1	0	0	0		1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0		
	0	0	1		1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0		
	0	1	0		1	1	1	0	0	1	0	0	0	1	0	0	0	0	0	1		
	0	1	1		0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0		
	1	0	0		0	0	0	1	0	0	0	0	0	0	0	1	0	1	0	0		
	1	0	1		0	0	1	0	0	1	1	1	0	0	0	0	1	0	0	0		
	1	1	0		0	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0		
	1	1	1		1	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0		
0 0 1 0	0	0	0																			
1 1 1 1	1	1	1																			

Fig. 13.1 External ROM Pattern Generation

1 General

The CB1040R (mounted with control LSI and a socket for the refresh memory) is a control circuit board for graphic display modules LM225 (200 x 640 dots)'s exclusive.
The CB1040R allows direct connection to the MPU bus line. The New LCTC* controls timing signal generation and data conversion required for a liquid crystal display (LCD) module, resulting in simplification of the graphic display system configuration. The CB1040R operates in the graphic and character modes. In the graphic mode, the contents of the refresh memory are displayed as is on the LCD to allow display of figures, graphs, and pictures.
In the character mode, the 8-bit parallel code for each character is converted to the corresponding dot pattern by the character generator in the CB1040R and displayed on the LCD. The built-in character generator converts 192 characters consisting of 160 JIS characters and 32 special pattern characters. An additional character general for character patterns required by the customer may also be mounted. As a new function, a C/G signal (input) capability is added for controlling the refresh address from an external device when the character mode is switched over to the graphic mode and vice versa.

The refresh memory, which uses static RAM, offers RAM selection of either 8 kbytes or 2 kbytes. Also, an external ROM may be used as a character generator, but the ROM similarly offers two selections, 4 kbytes and 8 kbytes. For further details, refer to "4.3 RAM Selections and 4.4 Character Generator ROM".

Note 1. The CB1040R has the oscillation frequency (f_{CL2}) set to LM225. So, it cannot be used except for a module which drives at the same frequency as that of LM225.

Note 2. The CB1040R does not have RAM and ROM mounted in when shipped. The customer is requested to prepare applicable RAM and ROM by referring to the information given in item 2. Please mount the RAM or ROM on the board after loosening the fixed screw.
There is a possibility for PCB and some ports to be destroy by some strength.

Note 3. The CB1040R is developed as a PCB for design and review of a display system using LM225. When using this product in large quantities, consult us for required specifications.

* New LCTC: High Speed Liquid Crystal Timing Controller

2 CB1040R Block Diagram

Fig. 2.1 shows a block diagram of the CB1040R.

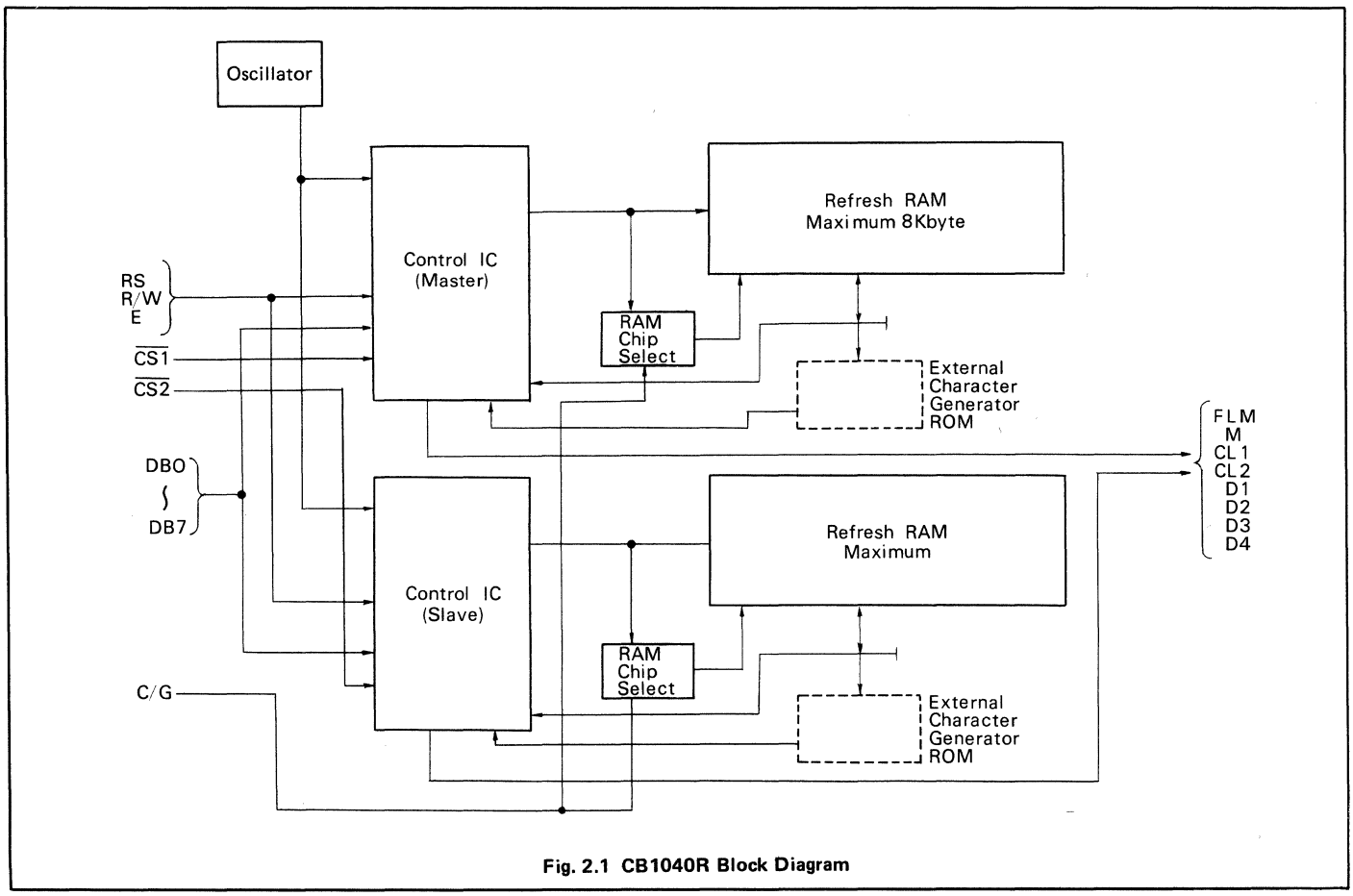


Fig. 2.1 CB1040R Block Diagram

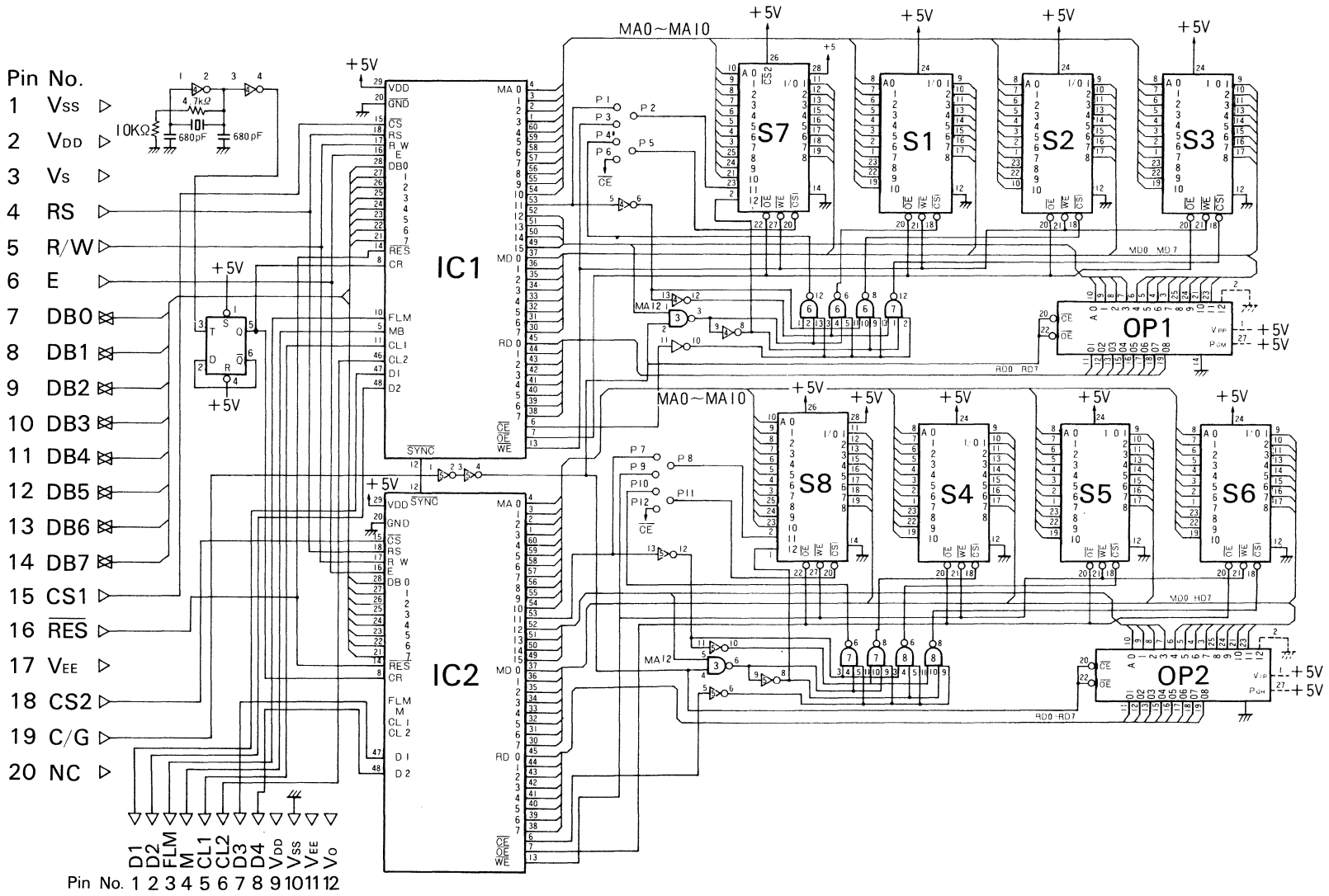


Fig. 3.1 CB1040R Circuit

4 Explanation of Each Part

4.1 Control LSI (New LCTC)

This is a special control LSI for the graphic LCD display module. It generates the timing signal and controls the data for LCD display modules. Selection between the graphic and character modes as well as LCD drive conditions shall be initialized through the data bus (DB0 to DB7).
The control LSI also has active area scroll, bit set, and bit clear functions.

4.2 Refresh Memory

The refresh memory, a static RAM, stores display data. In the character mode operation, the character data is written as 8-bit parallel code in this RAM. Display is controlled by the address (MA0 to MA12) from the control LSI. The read data is converted to the corresponding dot pattern by the character generator ROM in the control LSI (or the external character generator ROM) for display on the LCD.
In the graphic mode operation, the dot pattern from the control LSI is written in this RAM for display. (See paragraph 10 for the correspondence between the RAM address and the active area.)
Reading from or writing in this RAM is carried out through the control LSI Direct reading or writing from the MPU is impossible.

4.3 RAM Selections

The Hitachi HM6116 (2kbyte-SRAM) or HM6264 (8kbyte-SRAM) are available for combination of RAM's that can be mounted in the CB1040R.
The correspondence between RAM combinations and pin connections are shown in Table 4.1 below. Each pin connection for each combination of the above three should be provided by connecting pins on the printed-circuit board with jumper wires as shown in Table 4.1.

Caution

Use the RAM with the access time of less than 200 ns and the ROM with the access time of less than 250 ns. If the access time is other than as indicated above, timing with the control LSI may not be attained, resulting in erratic operation (error display).

4.4 Character Generator ROM

This is the ROM (Hitachi HN482732AG: 4 kbyte EP-ROM, HN482764AG: 8 kbyte EP-ROM or the equivalent) to be mounted when the user requires special character patterns. It controls up to 4 kbytes, or patterns for 512 characters. (See paragraph 15 for the pattern generation method.)
Use of both internal character generator ROM and external ROM is inhibited. (The ROM to be used shall be designated at the time of initialization.)
To use the external ROM, all using patterns shall be generated. The ROM is required for both the master and the slave. (Two are required.)
To mount these ROM, proceed as shown below.

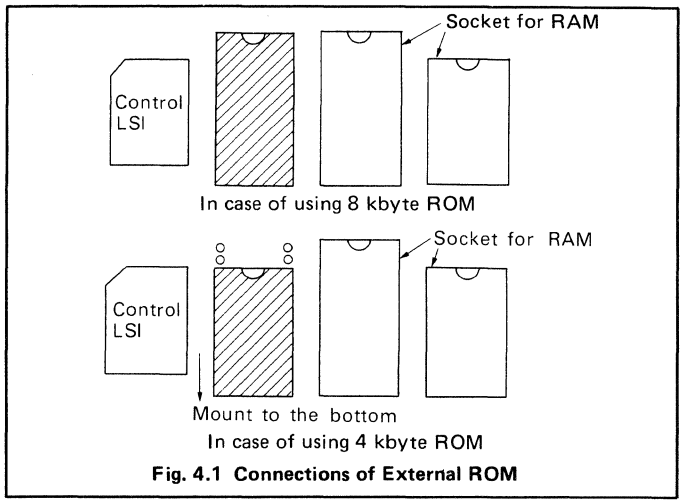


Fig. 4.1 Connections of External ROM

4.5 Patterns Generated Character Generator ROM in control LSI

Table 4.2 shows the character patterns generated by the internal ROM.

Table 4.1 RAM Pin Connections

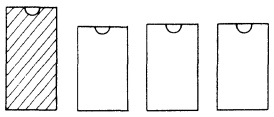
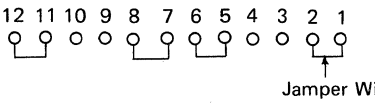
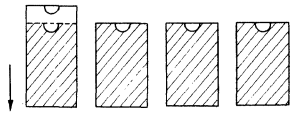
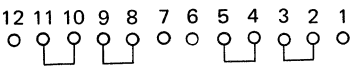
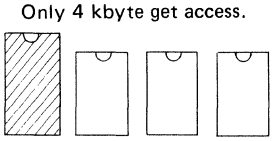
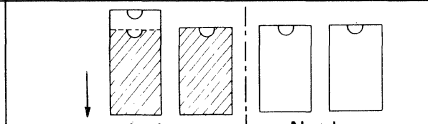
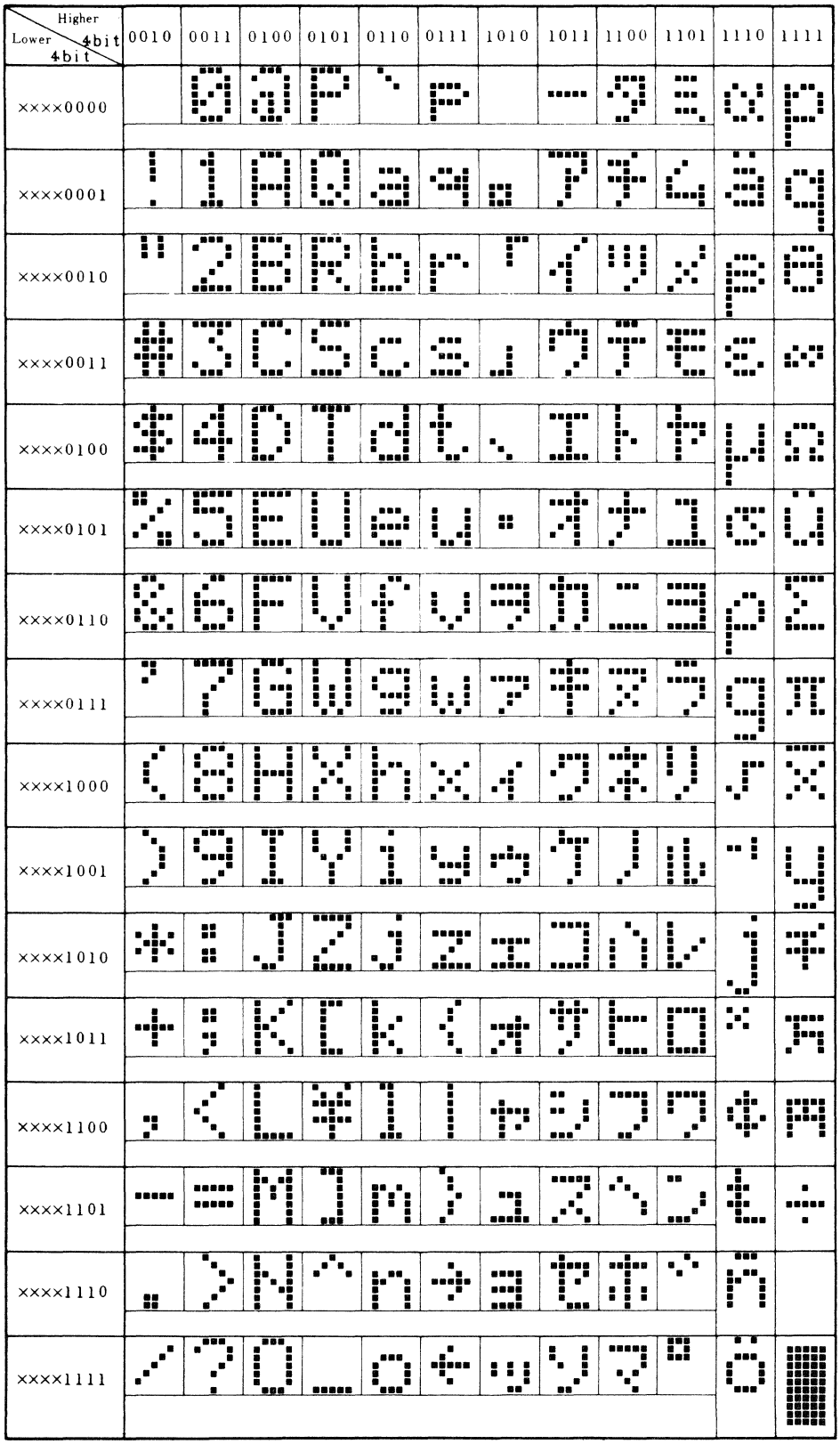
No	MODE	RAM	Socket in which RAMs are mounted (Master & Slave are common mounting.)	PIN CONNECTIONS (See Fig. 5.1 Pin for RAM)
I	Graphic Character	HM6264 (8 kbyte) x 1 pc.		
II	Graphic Character	HM6116 (2 kbyte) x 4 pcs.		
III	Character	HM6264 (8 kbyte) x 1 pc.		Same with No. I
IV	Character	HM6116 (2 kbyte) x 2 pcs.		Same with No. II

Table 4.2 Control LSI Font Table



Every code beginning with 0000 or not defined is displayed as a blank.

5 Dimensional Outline and Interface Pin Arrangement

5.1 Dimensional Outline

Unit: mm

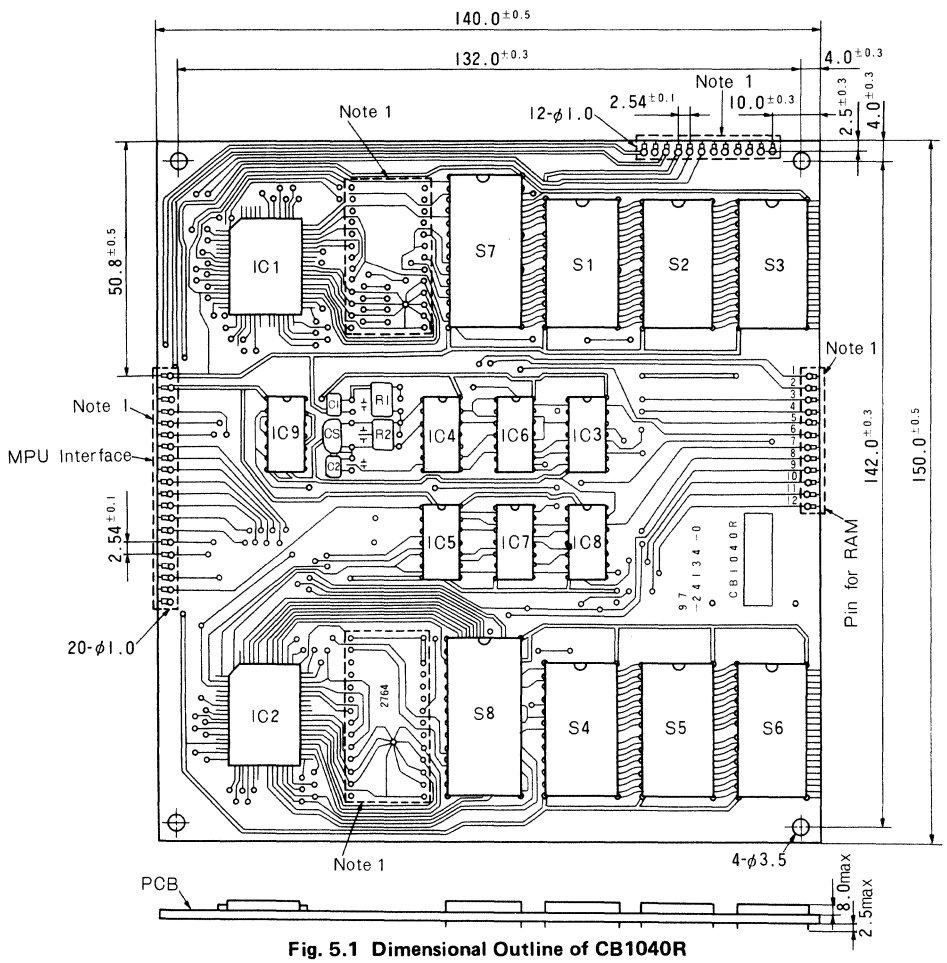


Fig. 5.1 Dimensional Outline of CB1040R

5.2 Interface Pin Arrangement

(1) LCD display module interface

LCM Interface

Pin No.	Signal Name
1	D1
2	D2
3	FLM
4	M
5	CL1
6	CL2
7	D3
8	D4
9	V_{DD}
10	V_{SS}
11	V_{EE}
12	V_0

Note:
(1) The pin arrangement is the same as that of the LM225.

(2) MPU interface

Pin No.	Signal Name
1	V_{SS}
2	V_{DD}
3	V_0
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3

Pin No.	Signal Name
11	DB4
12	DB5
13	DB6
14	DB7
15	$\overline{CS1}$
16	$\overline{RES}$
17	V_{EE}
18	$\overline{CS2}$
19	C/G
20	N.C.

Note:
Although V_0 and V_{EE} are not used in the CB1040R, they are provided for supply to the LCD module. (See Fig. 8.1.)
The CB1040R is the same as the conventional control board hitherto available, except that the C/G signal function is added to it. For detailed information about the C/G signal function, refer to "6. C/G Signal".

(3) Interface hole diameter

Through holes of 1.0 mm are adopted in both the MPU and LCD module.

6 C/G Signal

The C/G signal is an input signal for switching the connection of address to the refresh memory in selection of the character mode and the graphic mode.
In the graphic mode, it is set to H level, while in the character mode, it is set to L level.
The C/G signal is needed for the following reason:
The control LSI is provided with 16 address lines, MA0 to MA15 as address for the refresh memory, but the address effective for RAM varies as given in Table 6.1, depending upon the operation mode.

Table 6.1

Operation Mode	Valid Address	Required Address Range for One Block
Graphic	MA0 to MA15	8 kbyte/control LSI (MA0 to MA12 ... when HP = 8)
Character	MA0 to MA11	1 kbyte/control LSI (MA0 to MA9 ... when HP = 6, VP = 8)

In the character mode, MA12 to MA15 (higher-order 4 bits) are used as raster address so that MA12 to MA15 cannot be kept connected directly to the RAM.
To make possible a switchover between the character mode and the graphic mode in the CB1040R, it is necessary to connect at least MA12 to the RAM in the graphic mode, and to disconnect it from the RAM in the character mode. Because the control LSI does not have this switchover function, the switchover signal is input from outside to electrically connect to, and disconnect from RAM of MA12. This signal is the C/G signal.
Signals (RS, R/W, DB0 to DB7, CS1, CS2) other than the C/G signal are all fetched into the control board in synchronization with the E signal, but the C/G signal is directly fed to the address control circuit. So, address control is made without anything to do with the E signal. When the C/G signal is input, the address sequence of the RAM changes, and the display is rendered insignificant (nonsense). To preclude the possibility of such display, use the display ON/OFF commands to switch the mode while synchronizing the C/G signal with the E signal.
At that time, the C/G signal should be switched while the E signal that sends out a mode control command is H level.

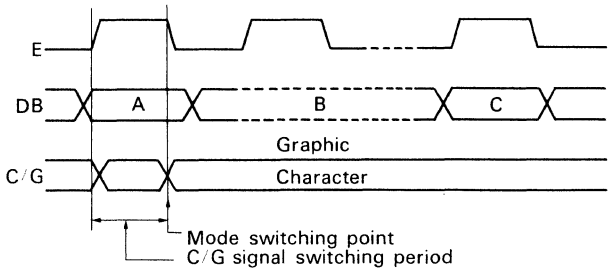


Fig. 6.1 Mode Switching Point C/G Signal Switching Period

A : Turn OFF the mode control command display.
Switch between graphic mode and character mode.
B : Execute commands such as for busy check and data transfer.
C : Turn ON the mode control command display.

7 Example of Interfaces with MPUs

Fig. 7.1 shows example of interfaces with various MPUs. In designing an actual interface circuit, consider the timing chart shown in paragraph 15.

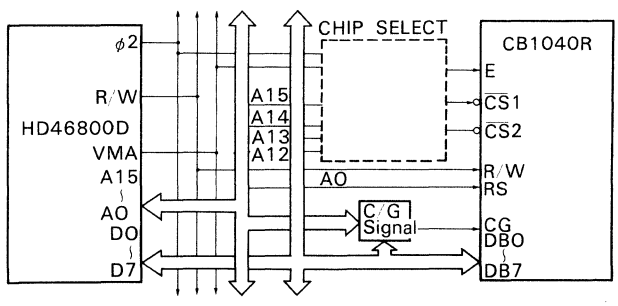


Fig. 7.1 Example of Interface with HD46800

Note: Concerning interfaces with another MPUs, we will inform in future.

8 LCD Drive Voltage Supply

All power voltages are supplied to the CB1040R and are output to the LCD module as shown in Fig. 8.1. V_O and V_{EE} simply pass the CB1040R.
The method shown in Fig. 8.2 is recommended for supplying LCD drive voltage V_O, but the method shown in Fig. 8.3 may be used because V_O and V_{EE} are used only in the LCD module. Select either way according to the CB1040R mounting position and the variable resistor location.
The LCD is driven by the potential difference between V_{DD} and V_O ($V_{DD} - V_O$). (See the Catalog for recommended drive voltage values for the LM225.)

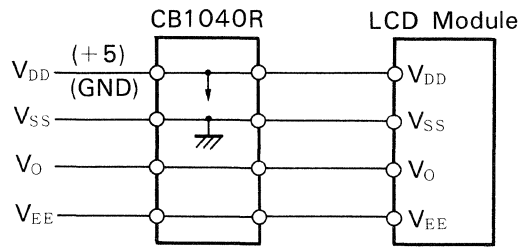


Fig. 8.1 Power Lines

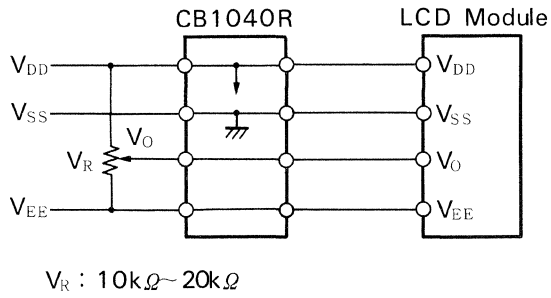


Fig. 8.2 Example of Variable Resistor Connection (1)

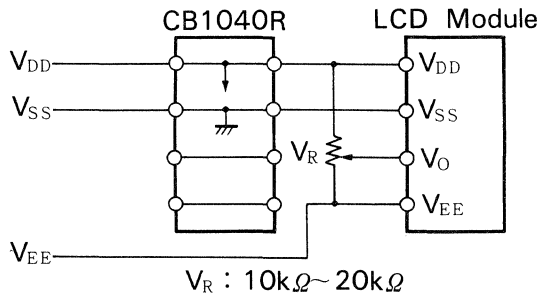


Fig. 8.3 Example of Variable Resistor Connection (2)

9 Power Sequence and $\overline{RES}$ Pin

9.1 Power Sequence

CMOS LSIs are used in the CB1040R and LCD display module. Always supply the power as in the sequence shown in Fig. 9.1. Each input signal shall be kept at the GND level until the +5V source voltage is stabilized. If a signal is input before stabilization of the source voltage, latch up may occur.

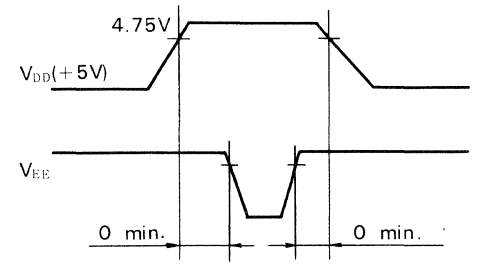


Fig. 9.1 Power Sequence

9.2 $\overline{RES}$ Pin

The $\overline{RES}$ pin has two following functions:

(1) Clearing each register in New LCTC.

(2) Resetting BUSY flag (enabling E signal receiving)
Since the BUSY flag status is unstable after power on, provide the C and R reset circuit. Input of the $\overline{RES}$ signal clears the registers in control LSI to make the LCD driving condition faulty to disable normal display. Although reinitialization restores normal status, input of the $\overline{RES}$ signal during operation should be prevented.
If application of the $\overline{RES}$ signal is obliged during operation, execute initial setting immediately after the $\overline{RES}$ signal is input. The pulse width of the $\overline{RES}$ signal should be 1 μs through 2 ms to avoid disturbance of LCD driving conditions during input of the $\overline{RES}$ signal.

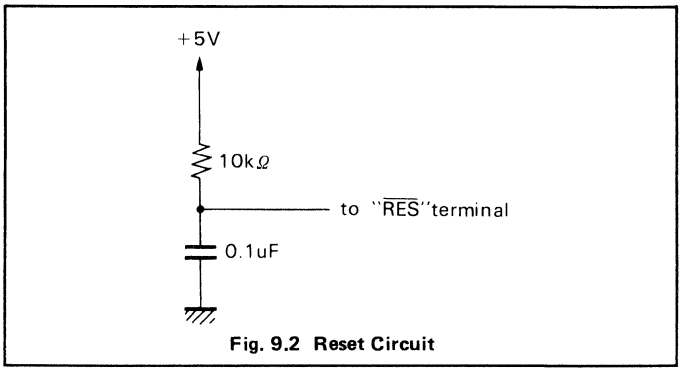


Fig. 9.2 Reset Circuit

10 Initialization and Busy Signal

10.1 Initialization

Tables 10.1 and 10.2 show the control LSI instructions and mode data bit functions respectively.

For initialization, it is necessary to proceed as below:

(1) Specify the master/slave for control LSI

(2) Set the liquid crystal module drive condition.

(3) Set the initial values of display start address and cursor address.

Key in No. 1 (mode control) to No. 9 (cursor address lower) in the sequence (one example) indicated and then initialize. Write all mode control data DB2 to DB4, excepting the master slave designation and cursor designation, on the master side and the slave side.

When initialization is made, relations between the block and the RAM address are as shown in Fig. 10-2, and in the character mode, the cursor is shown below the character at the upper left corner. (But when the refresh memory has not been cleared, random characters appear on the screen.)

Designation of other instructions may be omitted at initialization. Setting (writing in each register) in the control LSI is effected by designation of the register number succeeded by writing data.

The setting method is similar to that of the CRT controller (CRTC).

Fig. 10.1 shows an example of the initialization flow-chart. Since the register pointer designates the same register until setting of a new register number, sequential register number specifications are necessary for initializing data writing.

An operation example from power on to display on the LCD (LM225 in this example) is shown in Fig. 16.1.

Caution:

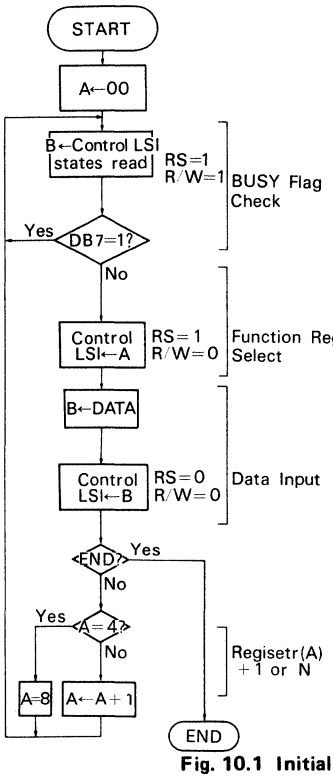
Instructions No. 2 through No. 4 in Table 10.1 shall be executed immediately after power on and should not be changed during operation.

The conditions in resetting after the $\overline{RES}$ signal is input should also be the same as those specified first.

Table 10.1 Control LSI Instruction List

Register									Data									
No.	R/W	RS	DB7 ~ DB4	DB3	DB2	DB1	DB0	Function	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	0	0	0	0	0	Mode control	0	0	0	0	Mode data (Note 1)					
2	0	1	0	0	0	0	1	Vertical/horizontal character pitch	0	0	(Vp-1)$_B$				0	(Hp-1)$_B$		
3	0	1	0	0	0	1	0	Number of characters per line/number of bytes	0	0	0	(HN-1)$_B$						
4	0	1	0	0	0	1	1	Number of vertical dots	0	0	0	(NX-1)$_B$						
5	0	1	0	0	1	0	0	Cursor position	0	0	0	0	0	0 (Note6)	(CP-1)$_B$			
6	0	1	0	1	0	0	0	Display starting address (least significant) (Lower)	0	0	Address data							
7	0	1	0	1	0	0	1	Display starting address (most significant) (Upper)	0	0	0	0	0	0 (Note6)	Address data			
8	0	1	0	1	0	1	0	Cursor address (least significant) (Lower)	0	0	Address data							
9	0	1	0	1	0	1	1	Cursor address (most significant) (Upper)	0	0	0	0	0	0	Address data			
10	0	1	0	1	1	0	0	Refresh memory write	0	0	Character code/bit data							
11	0	1	0	1	1	0	1	Refresh memory read	1	0	Refresh memory data							
12	0	1	0	1	1	1	0	Bit clear	0	0	0	0	0	0	0	(BN)$_B$		
13	0	1	0	1	1	1	1	Bit set	0	0	0	0	0	0	0	(BN)$_B$		
14	–	–	–	–	–	–	–	BUSY signal read	1	1	BF	*	*	*	*	*	*	*

Notes: 1. See Table 10.2.
2. HP: Specify 6, 7, or 8.
3. HN $\leqq$ 128: If the active area is divided, specify the number of characters/number of bytes per block. (Even number of 2 ~ 128)
4. NX = Number of duties $\leqq$ 128.
5. BF = 0 (E signal being received) BF = 1 (during internal processing).
6. Character mode: "0".
Graphic mode: Address data.

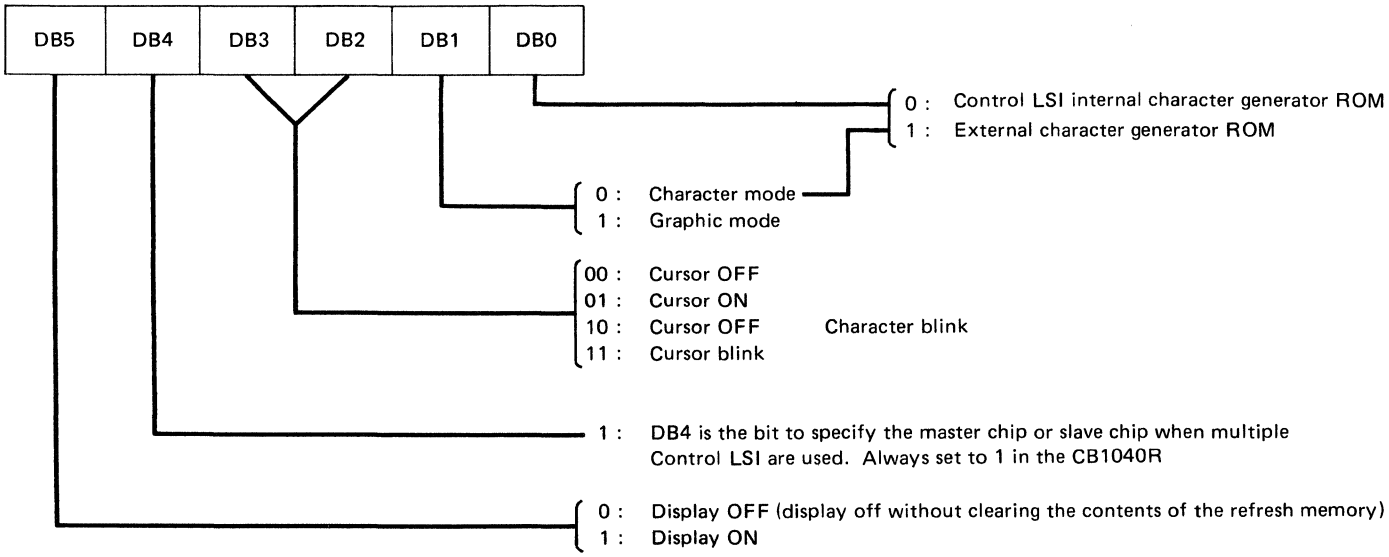


Note 1: A, B; MPU Internal Register

Note 2: Change the register number normally +1 at a time, but in No. 5 to No. 6 of Table 10.1, register numbers are not continuous.

Fig. 10.1 Initialization Flowchart (Example)

Table 10.2 Mode Data



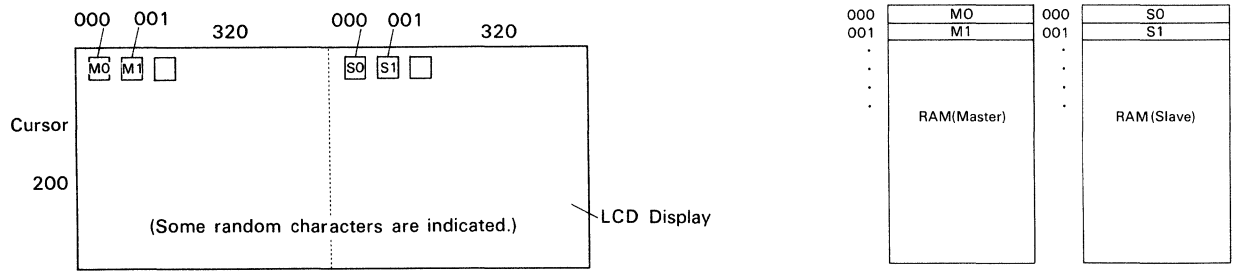


Fig. 10.2 Relationship between the display and RAM address.

10.2 Busy Signal

The control LSI has an independent oscillator to generate the LCD drive timing. All control LSI internal operations and refresh memory read/write operations use the clock signal generated by this internal oscillator. This oscillator operates in perfect a synchronism with the clock on the MPU side. In processing instructions from the MPU and data writing, the contents of the data bus are first latched in the buffer register in the control LSI by the enable signal (E signal), then processed according to the internal clock signal starts. Generally, the time equivalent to two internal clock pulses or more is necessary for one operation (processing) so that the processing speed does not match that of the MPU.

To ensure processing of received instructions and data, the flag to inhibit the E signal is set in the control LSI during processing in the LSI.

This flag is called the Busy Signal.

The duration of the Busy Signal depends on the function as shown in Table 10.3.

Table 10.3 Busy Signal Duration

Function	Busy		
	Generation/ nongeneration	Max.	Min.
Setting register No.	None	1 μs	–
Setting data in register	Generation	2 x t_{CL2}	t_{CL2}
Refresh RAM read/write	Generation	(2 + Hp)t_{CL2}	2 x t_{CL2}
Bit write/clear	Generation	2 (Hp + 1)t_{CL2}	(2 + Hp)t_{CL2}

Notes: 1. t_{CL2} (Internal clock signal cycle) LM225 . . . 450 ns (typ.)
2. Hp (Horizontal character pitch) 6, 7 or 8.
3. The time from the E signal falling edge (⌐_) is shown.

To ensure the correct internal operation of the Control LSI, send and receive instructions while checking the Busy Signal. If it is obliged to use machine without checking the Busy Signal, be sure to allow for at least three times the duration listed in Table 8.4 below.

The Busy Signal is used only in the LSI and not directly output from the control LSI. Checking the busy state of the control LSI from the MPU side uses the Busy Signal read function in the sequence shown in Fig. 10.3.

Fig. 10.1 shows an example flowchart.

The minimum E signal cycle time of 1.0 μs in paragraph 14 is the time for Busy check and register number setting as shown in Fig. 10.3. It does not mean that the control LSI is able to process an instruction within a minimum cycle time of 1 μs.

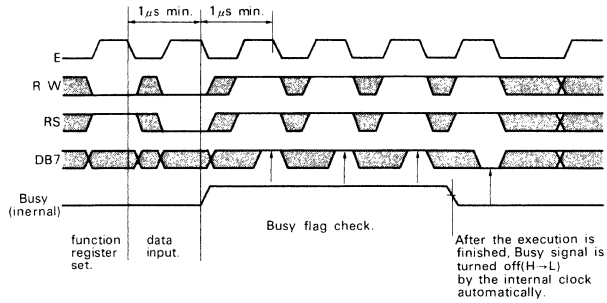


Fig. 10.3 Busy Check Sequence

11 Explanation of Instruction Code

11.1 Mode Control (Table 10.1, No. 1)

Specify the operation mode of the control LSI.

This instruction controls the character/graphic mode, cursor on/off/blink and master/slave, display on/off.

When DB1 is set to 1, and DB0, DB2 and DB3 are set to 0, the control LSI is set in the graphic mode. In this case, the function of character generator and cursor are ignored.

When DB1 is set to 0, the control LSI is set in the character mode, and the character generator designation (DB0) and cursor control (DB2, DB3) are validated.

The blink cycle is determined by the internal oscillator frequency. It is generally (0.2) to (0.4) sec.

11.2 Vertical/Horizontal Character Pitch (Table 10.1, No. 2)

Specify the number of dots per character in the vertical and horizontal directions. The number of dots in the horizontal direction shall be specified as 6, 7, or 8. Since the font of the character generator consists of 5 x 7 or 5 x 11 dots, specifying 12 in the vertical direction and 8 in the horizontal direction causes character display justified to the left top as shown in Fig. 11.1. in the graphic mode, Vp data is ignored but $H_P - 1 = 7$ shall be specified.

Use hexadecimal notation for number specification.

The data 0 for dots other than the character portion and cursor is generated in the control LSI.

Limit of V_P and H_P

$7 \leqq (V_P - 1) \leqq 15$
$5 \leqq (H_P - 1) \leqq 7$ } Character Mode

$(V_P - 1) = **$ (Not effect)
$(H_P - 1) = 7$ } Graphic Mode

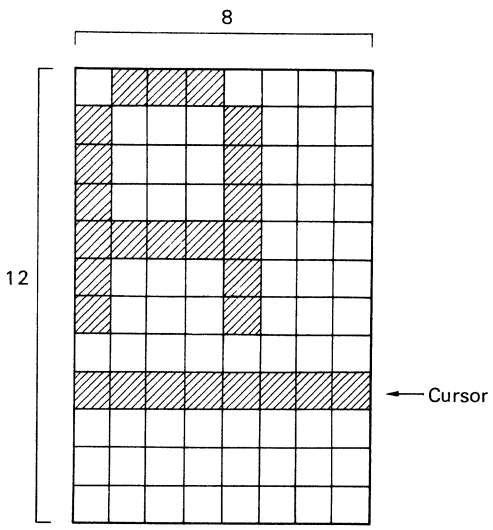


Fig. 11.1 Display Pattern (Example)

11.3 Number of Characters per Line/Number of Bytes (Fig. 10.1, No. 3)

Specify the number of characters per line in the horizontal direction and the number of bytes for graphic display.
The calculating formulas are as follows:
Character mode

$$H_N = \frac{\text{Number of dots in horizontal direction}}{H_P}$$

Graphic mode

$$H_N = \frac{\text{Number of dots in horizontal direction}}{8}$$

Use hexadecimal notation for specification.

If the calculated H_N is not an integer, count the decimal fraction as 1 or 2 for specification. Always specify an even number. Specifying an odd number is inhibited.
For the module whose active area is divided into 2 blocks, specify the number of characters/number of bytes per block. For the LM225 for example, the active area is divided as shown in Fig. 11.2, so specify 320 ÷ 8 = 40 (27 in hexadecimal notation.)

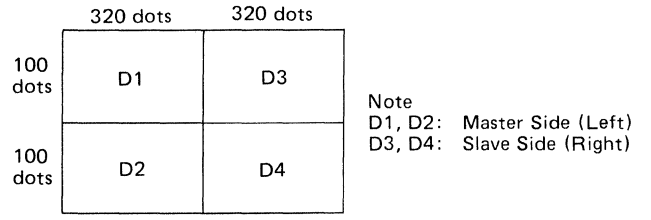


Fig. 11.2 (1) LM225 Active Area Division

If H_N x H_P exceeds the number of dots, the character at the right end of the active area is displayed fully, but the character at the left end may be displayed in imperfect state. See Fig. 11.2 (2).

11.4 Number of Vertical Dots (Fig. 10.1, No. 4)

Specify the number dots in the vertical direction in hexadecimal notation.
Specify the number of dots irrespective of the graphic mode or character mode.
Specifications of the number of characters per line/number of bytes and the number of vertical dots determine the LCD drive timing. The specifications should match those of the LCD module as far as possible. Specifying values extremely different from LCD module specifications may cause display flickering or fading.
For a module divided into two blocks in the vertical direction, specify the number of vertical dots in one block. For example, the LM225 is divided as shown in Fig. 11.2, so specify 100 (63 hexadecimal notation).
If H_N = 50, H_P = 7 and number of horizontal dots = 320;

H_N x H_P = 50 x 7 = 350 dots > 320 dots

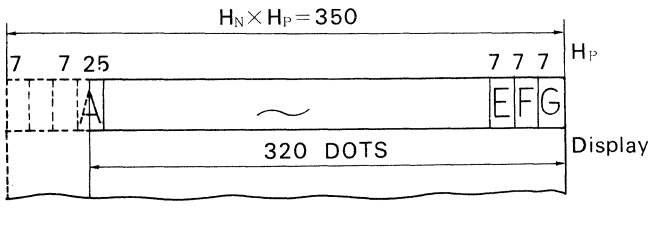


Fig. 11.2 (2) Display Example for H_N x Hp > Number for Dots

11.5 Cursor Position (Table 10.1, No. 5)

Specify the cursor lighting position. Observe $V_P \geqq C_P$.
If C_P = 8 is specified, the cursor is displayed on the 9th line from the top. The number of cursor dots in the horizontal direction is the same as the value of H_P. Blinking also occurs in the range of V_P and H_P in the vertical and horizontal directions.

11.6 Start Address (Table 10.1, Nos. 6 and 7)

Specify the most significant 8 bits and least significant 8 bits of the display start address. Generally, specify $(0000)_{16}$. Changing the display start address enables display starting from an arbitrary address in the refresh memory so that scrolling can be executed easily. The start address data is displayed at the top left position of the active area. See Section 11 for details of the scrolling operation.

11.7 Cursor Address (Table 10.1, Nos. 8 and 9)

Specify an address in the refresh memory. Since the cursor address is automatically incremented (+1), address setting is unnecessary after setting the first address in case of continuous data writing in contiguous addresses. If addresses are discontiguous, address setting is required each time.
Contents: The cursor address is divided into lower address (8 bits) and the upper address, but setting should be made in close observance of the following restrictive information.

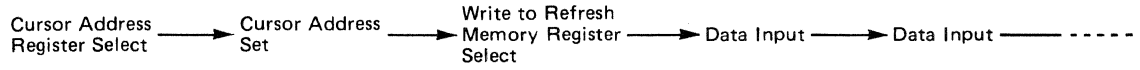
1	When it is desired to rewrite (set) both lower address and upper address.	First set lower address and then upper address.
2	When it is desired to rewrite lower address only.	After setting the lower address, be sure to set the upper address once again.
3	When it is desired to rewrite upper address only.	Set upper address. Setting the lower address once again is not required.

The cursor address counter is a 16 bit up counter with set and reset functions. When Nth bit is changed from "1" to "0", N + 1 bit therefrom counts up.
So, when the lower address is set, when setting is made so that the lower MSB (8th bit) is changed from "1" to "0", LSB (1st bit) of the upper counter counts up. Therefore, the cursor address setting should be made with the lower and upper settings as 2 byte continuous instructions.

11.8 Writing in Refresh Memory (Table 10.1, No. 10)

The function to write the display data.
Generally executed in a pair with the cursor address setting in the sequence shown in Fig. 11.3.
In the graphic mode, the data is inverted in writing and display as shown in Fig. 11.4.
Either invert the data for each byte at the time of data preparation or use the inversion program as shown in Fig. 11.5.

(a) Continuous Address



(b) Discontinuous Address

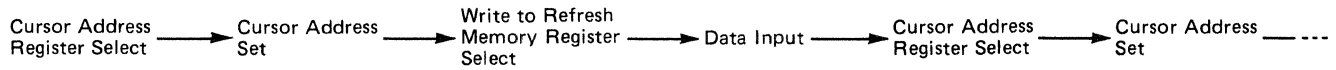


Fig. 11.3 Data Writing Sequence

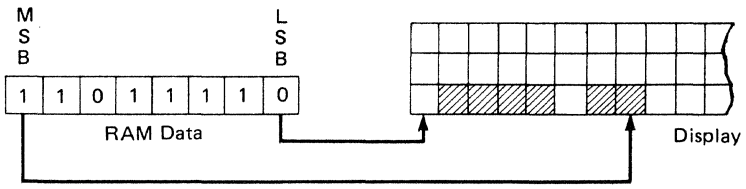
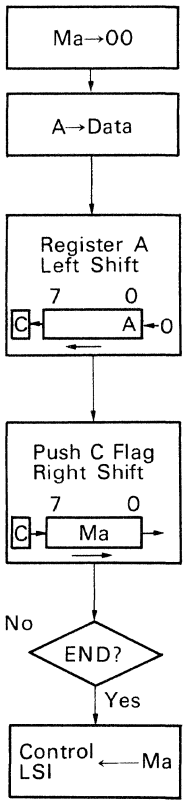
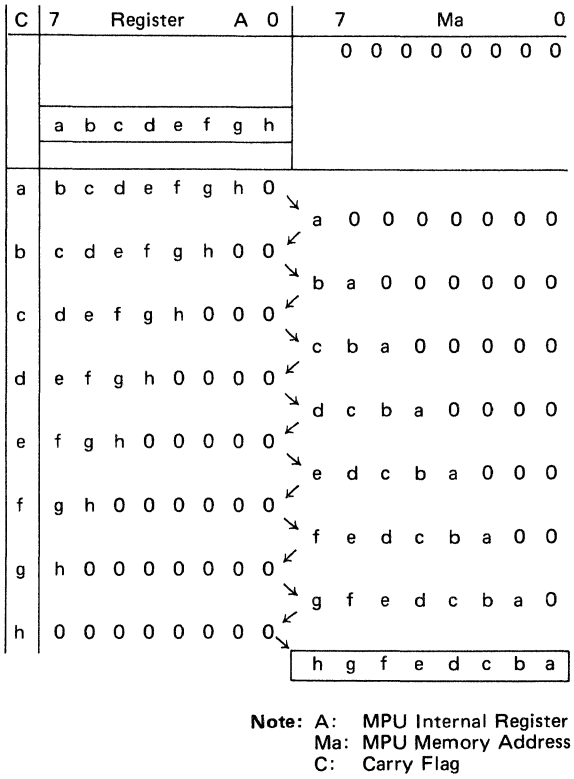


Fig. 11.4 (1) Data Inversion in Graphic Mode





Note: A: MPU Internal Register
Ma: MPU Memory Address
C: Carry Flag

Fig. 11.5 Data Inversion

11.9 Reading from Refresh Memory (Table 10.1, No. 11)

The function to read the refresh memory contents for input to the MPU. The reading sequence is similar to that shown in Fig. 11.3.

The data inversion is read/write operation from and to the MPU does not occur.

The data read immediately after address setting becomes insignificant because of circuit operation, so it shall be ignored. The data read the second time is normal. The cursor advances 1 position as the data is read once. It must be noted that the data being read is always the one behind the cursor.

11.10 Bit Clear and Bit Set (Table 10.1, Nos. 12 and 13)

Only one bit of the data (8 bits) at the address designated by the address counter can be operated. These functions shall be used in paired state with the cursor address set. In the character mode, the character pattern changes. In the graphic mode, only one dot changes. If bit set and bit clear are repeated continuously without address setting, the address is incremented by 1. The correspondence between the bit data and display is as shown in Fig. 11.4.

11.11 Busy Signal Read (Table 10.1, No. 14)

This function shall be used to check whether the control LSI is busy or not. The Busy Signal is output to DB7 when this function is executed. Otherwise, the Busy Signal is not output from the LSI. DB6-0 contains insignificant data. For sure execution of the instruction from the MPU write a program to proceed with processing while executing Busy checks.

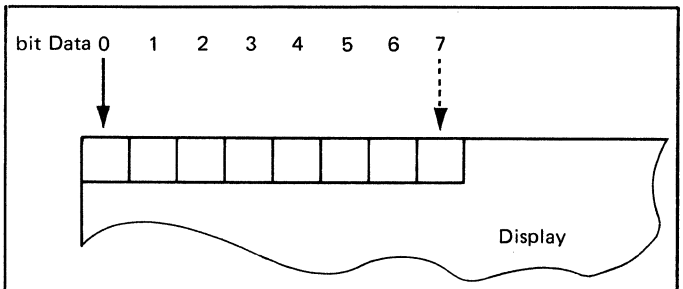


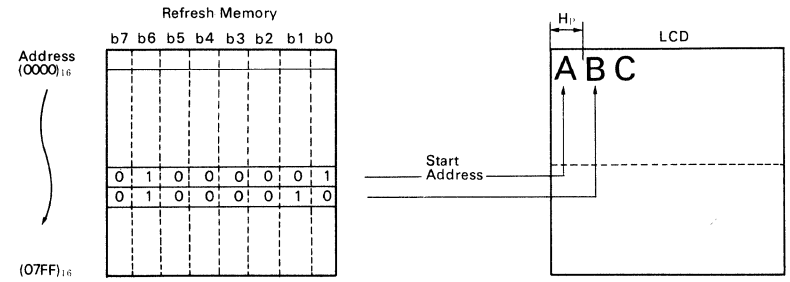
Fig. 11.6 Relationship between Bit Data and Display

12 Relationships between Cursor Address, Start Address, Refresh RAM, and LCD Display

Character mode . . . . . See Fig. 12.1.
Graphic mode . . . . . See Fig. 12.2.

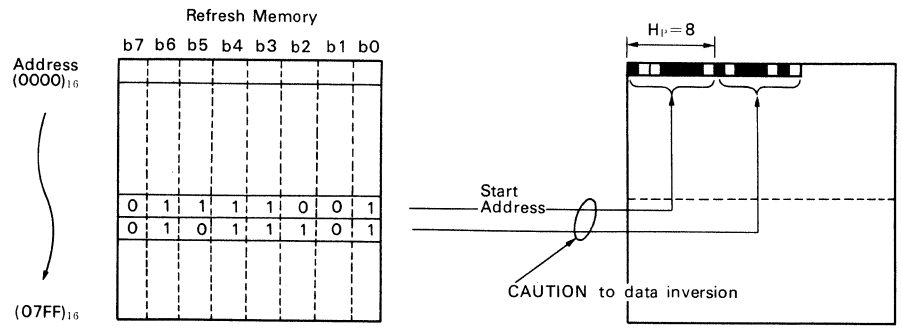
Even in case of active area division, the addresses are electrically contiguous vertically or horizontally.

In the character mode, the most significant 4 bits of the address (MA12 ~ MA15) is used for scanning of the vertical pitch, so external control is impossible. In the graphic mode, the horizontal character pitch (H_P) is limited to 8 dots and the RAM data is displayed as it is on the LCD. However, pay attention to data inversion in each byte as described in Section 11.8.



Note: In the case of the character mode, the method of writing on the master side (left side: D_1, D_2) and the slave side (right side: D_3, D_4) is the same.

Fig. 12.1 Character Mode



Note: In the case of the graphic mode, the method of writing on the master side (left side: D_1, D_2) and the slave side (right side: D_3, D_4) is the same.

Fig. 12.2 Graphic Mode

13 Scrolling Operation

The start address is generally set to $(0000)_{16}$. Changing this value enables an active area scrolling operation.
Pay attention to the following points:

(1) In the character mode, scrolling in one character unit (V_P value for the number of lines) is possible.
(2) In the graphic mode, scrolling in one byte (8 bits) unit is possible.
(3) The least significant address and the most significant address of the refresh RAM are apparently contiguous to provide the endless form. The range of addresses displayed in the active area is the start address + (H_N X N_X/ Vp).
(In the graphic mode V_P = 1. When the number of dots of the LCD module is different from the number expressed by H_N and N_X, this is not applied.)
Irrespective of the display size, information in all addresses of the RAM can be displayed.
(4) If the active area is horizontally divided into 2 blocks in a module like LM225, changing the starting address causes the data in the top line of the right block to be shifted to the bottom line of the left block. (See Fig. 13.1.)
Pay attention to this point when carrying out the scrolling operation.
(5) In case of horizontal scrolling in the graphic mode, H_N shall be specified as 2^N (N = 1, 2, ... : integer).
In other than 2^N, display at the time of scrolling will become out of order.
(6) Display shifting in scrolling operation
When the start address is changed by one address, whole display is shifted by 1 character or 1 byte (8 bits) toward the left. The data at the left end is displayed at the right end of the preceding line.

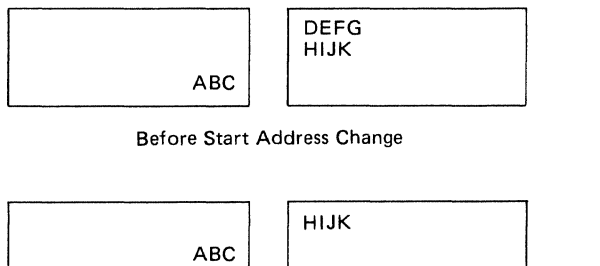


Fig. 13.1 Scrolling in Case of Horizontal Division (Example)

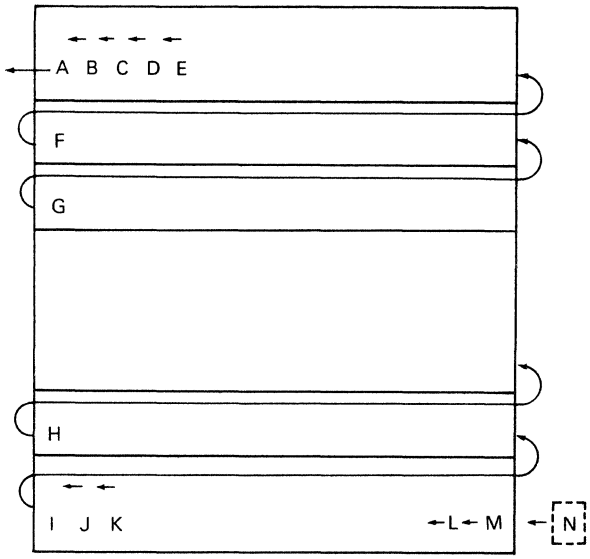


Fig. 13.2 Display Shifting in Scrolling Operation

14 Electrical Characteristics

14.1 Maximum Ratings

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}	0 to 7.0	V
Input Voltage	V_I	0 to V_{DD}	V
Operating Temperature	Topr	0 to 50	°C
Storage Temperature	Tstg	−20 to 70	°C

Notes: (1) V_{EE} is generally 11.0 volts.
(2) The range of V_0 shall be $V_{DD} \geqq V_0 \geqq V_{EE}$.

14.2 Electrical Characteristics

(V_{DD} = 5V ±5%, GND = 0V, Ta = 0°C to 50°C)

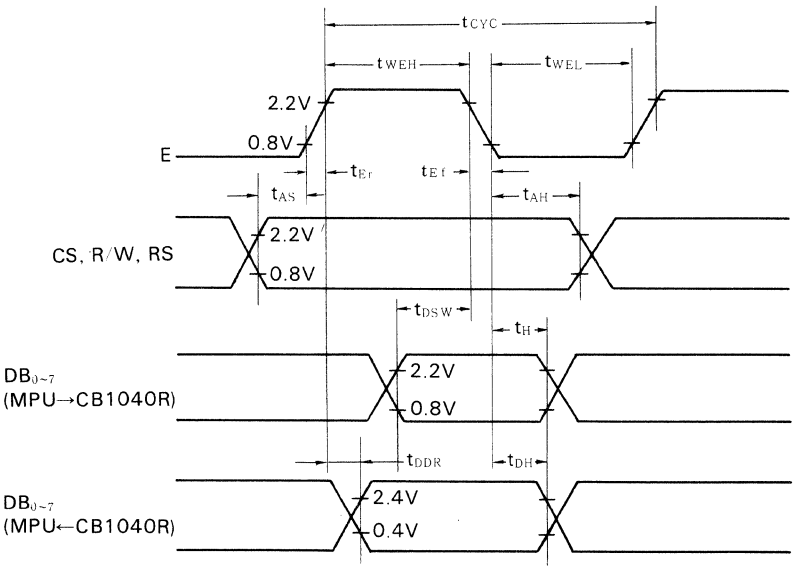
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Terminal
Input Voltage (TTL compatible)	V_{IH}		2.2	–	V_{DD}	V	DB0 ~ 7, $\overline{CS1}$, 2, E, R/W, RS, $\overline{RES}$ (Note: 3)
	V_{IL}		0	–	0.8	V	
Output Voltage (TTL compatible)	V_{OH}	I_{OH} = –0.6 mA	V_{DD}-0.4	–	V_{DD}	V	DB0 ~ 7,
	V_{OL}	I_{OL} = ±1.6 mA	0	–	0.4	V	
Output Voltage	V_{OHC}	Iload = ±0.6 mA	V_{DD}-0.4	–	V_{DD}	V	M, FLM, CL1, CL2, D1, D2
	V_{OLC}		0	–	0.4	V	
Input Leak Current	I_{in}		–	–	5	μA	
Output Leak Current	I_{OL}		–	–	10	μA	
Operating Frequency	F_{CP1}		–	–	2.4	MHz	Note (1)
Power Dissipation	P_W	V_{DD} = 5V, T_A = 25°C	–	–	80	mW	Note (2)

Notes: (1) Internal frequency.
(2) Excluding the refresh RAM and ROM current consumption.
(3) $\overline{RES}$: V_{IH} = 3.0V, V_{IL} = 0.8V.

15 Timing Characteristics

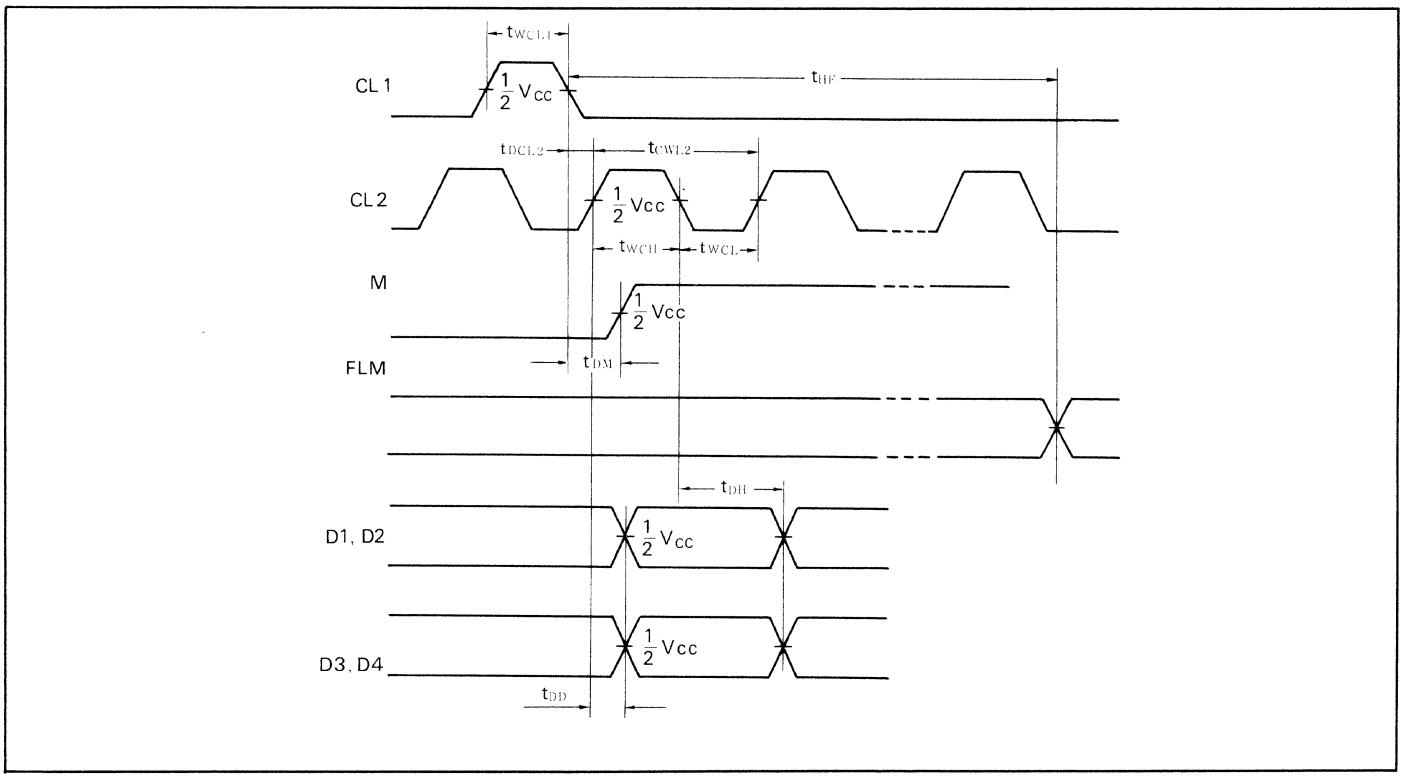
15.1 MPU Interface (MPU ↔ CB1040R)

Items		Symbol	Min.	Typ.	Max.	Unit
Cycle Time of "E"		t_{CYC}	1.0	–	–	μs
Pulse Width of "E"	H Level	t_{WEH}	0.45	–	–	μs
	L Level	t_{WEL}	0.45	–	–	μs
Pulse Raise Time of "E"		t_{Er}	–	–	25	ns
Pulse Fall Time of "E"		t_{Ef}	–	–	25	ns
Set Up Time of $\overline{CS}$, R/W, RS		t_{AS}	140	–	–	ns
Set Up Time of Input Data		t_{DIS}	225	–	–	ns
Data Delay Time		t_{DD}	–	–	225	ns
Data Hold Time		t_H	10	–	–	ns
Hold Time of $\overline{CS}$, R/W, RS		t_{AS}	10	–	–	ns
Pulse Width of $\overline{RES}$		t_{WRES}	1μs	–	2 ms	–



15.2 LCM Interface (CB1040R ↔ LCM)

Items		Symbol	Min.	Typ.	Max.	Unit
Pulse Width of "CL1"		t_{WCL1}	150	–	–	ns
Delay Time of "CL2"		t_{DCL2}	–	–	50	ns
Cycle Time of "CL2"		t_{WCL2}	416	–	–	ns
Pulse Width of "CL2"	H Level	t_{WCH}	150	–	–	ns
	L Level	t_{WCL}	150	–	–	ns
Delay Time of "M"		t_{DM}	−200	–	200	ns
Hold Time of "FLM"		t_{HF}	1000	–	–	ns
Delay Time of D1 ~ D4		t_{DD}	–	–	50	ns
Hold Time of D1 ~ D4		t_{DH}	100	–	–	ns



16 External ROM Pattern Generation

Fig. 16.1 shows the correspondence between the ROM address and data.
Write the 8-bit data corresponding to dot on/off for each address. A0 ~ A3 show the scanning address. To display the pattern of the external ROM, write the codes of the most significant 4 bits and least significant 4 bits (total 8 bits) (A3 ~ A10) in the refresh RAM. Then, the corresponding character pattern is displayed on the LCD. However, the display range depends on the value of H_P.
Specifying $H_P = 6$; Data at O_6 and O_7 are not displayed.
Specifying $H_P = 7$; Data at O_7 is not displayed.
Specifying $H_P = 8$; All data at O_1 through O_7 are displayed.

17 Applicable Connector

Any connector whose pitch is 2.54 mm and pin diameter less than 0.9 ~ 0.8 mm can be used.
For example, the following connectors manufactured by Japan Aviation Electronics Industry, Ltd.
For MPU interface (20 pins) PS-20PE-S4T1-PN1
For LCD interface (12 pins) PS-12PE-S4T1-PN1

Higher A11				0								0								0
4 bits A10				0								0								0
Lower A9				0								0								1
4 bits A8				0								1								0
A7 A6 A5 A4	A3	A2	A1	A0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	
0 0 0 0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
	0	0	1	1	1	1	1	1	0	0	0	0	1	0	0	0	0	0	1	0	
	0	1	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	
	0	1	0	1	1	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	
	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	
	0	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	
	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	
	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	
	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0 0 0 1	0	0	0	0																	
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Note: Data of A4 ~ A11 belong character code.

Fig. 16.1 External ROM Pattern Generation

18 Example of Usage

Condition: Character mode (internal ROM used)
Character pitch 8 x 8

No.	Contents of Execution	Command	Image Display
1	Power ON		
2	Master LSI initialize	See Fig. 10.1	Random character display pattern appears at 1/100 duty.
3	Slave LSI initialize	See Fig. 10.1	
4	Master side refresh RAM clear (blank code input)	Make CS1 "L" Refresh Memory Write Designation Blank Code (20) Input Input made in all addresses of refresh memory (on master side)?	Blank Random character display Master side Slave side
5	Slave side: Refresh RAM clear	Make CS2 "L" Repeat No. 4 Routine	Blank Blank
6	Address set (on master side)	Make CS1 "L" Set Master Home Position (000) in Cursor Address	Cursor lights
7	Data input	Refresh Memory Write Designation Enter Character Codes 40 Times Mode Control Cursor OFF	Cursor moves to 2nd line. Cursor is caused to disappear by running this command.
8	LSI switchover	Make CS2 "L" Set Cursor Address to Slave Home Position (000) Mode Control Cursor ON	Cursor lights on 1st line of slave side.
9	Data input	Refresh Memory Write Designation Enter Character Codes 40 Times Mode Control Cursor OFF	Move cursor to 2nd line Cursor is caused to disappear by running this command.
10	LSI switching	Make CS1 "L" Set Cursor Address to Head of Address in 2nd Line. Mode Control Cursor ON Data Input	Cursor lights on 2nd line.

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January 1987

Printed in U.S.A.