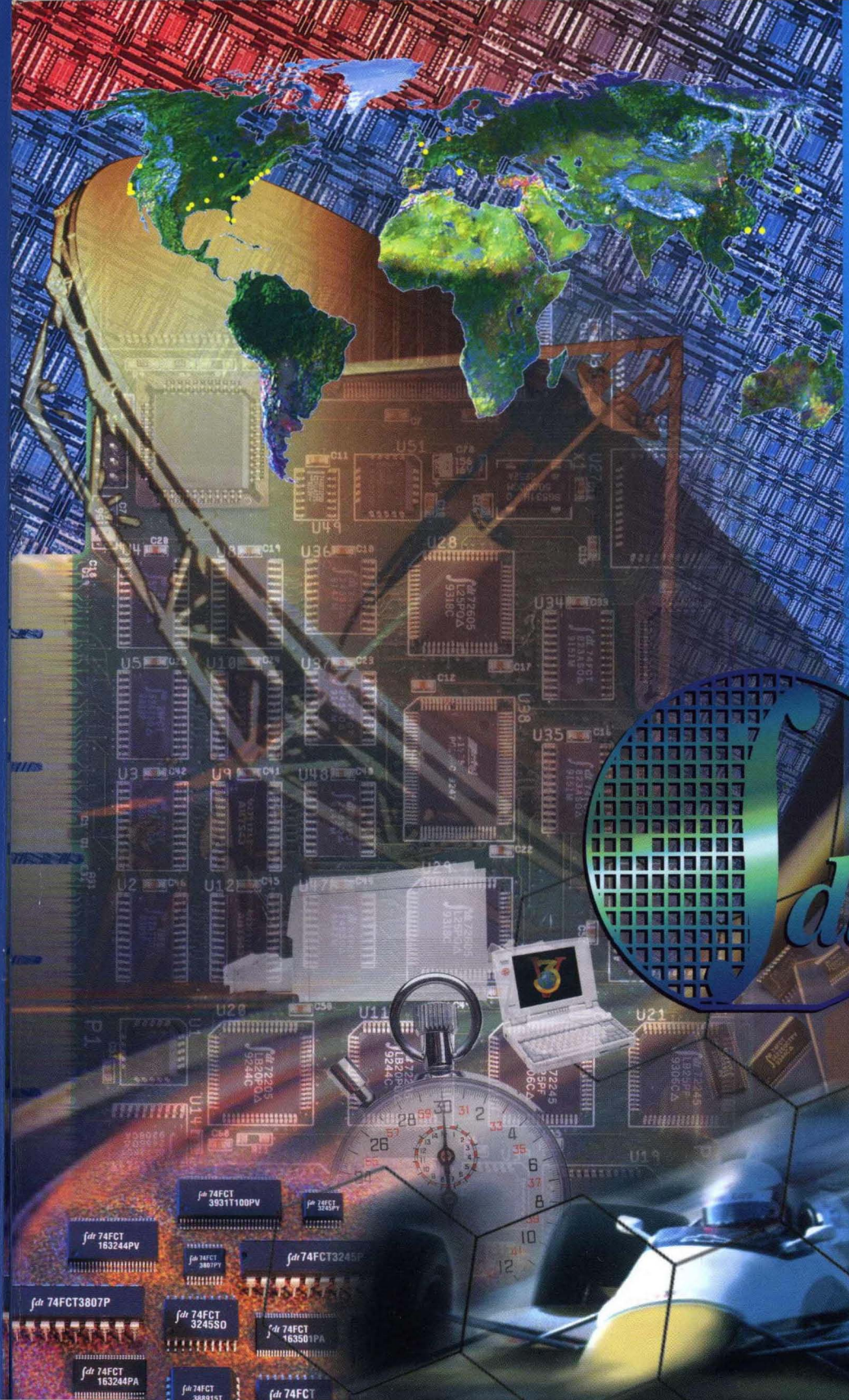
1995

HIGH-PERFORMANCE LOGIC DATA BOOK

5VOLT & 3.3VOLT

Integrated Device Technology, Inc.



5VOLT & 3.3VOLT
OCTOBER 1995

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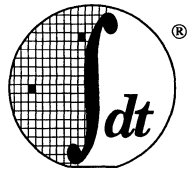

Integrated Device Technology, Inc.

OCTOBER 1995
HIGH-PERFORMANCE LOGIC DATA BOOK

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CONTENTS OVERVIEW

For ease of use for our customers, Integrated Device Technology provides four separate data books: High-Performance Logic, Specialized Memories and Modules, RISC and RISC SubSystems, and Static RAM.

IDT's 1994 Logic Data Book is comprised of new and revised data sheets on Double-Density 5V logic products, Octal 5V Logic products, CMOS-Level Output, 3.3V Logic products, Clock Management products, and Complex Logic products. Also included is a current packaging section for the products included in this book.

The 1994 High-Performance Logic Data Book's Table of Contents contains a listing of the products contained in this data book only (in the past, we have included products that appeared in other IDT data books). The numbering scheme for the book is consistent with the 1990–92 data books. The number at the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e., 5.5 would be the fifth data sheet in the fifth section). The number in the lower right-hand corner is the page number for that particular data sheet.

Integrated Device Technology, Inc. is a recognized leader in high-speed CMOS technology and produces a broad line of products. This enables us to provide a complete CMOS solution to designers of high-performance digital systems. Not only do our product lines include industry standard devices, they also feature products with faster speeds, lower power, and package and/or architectural benefits that allow designers to significantly improve system performance.

To find ordering information: Ordering Information for all products in this book appears in Section 1, along with the Package Outline Index, Product Selector Guides, Ordering Information, and Standard Logic Timing Diagrams. Reference data on our Technology Capabilities and Quality Commitments is included in separate sections (2 and 3, respectively).

To find product data: Start with the Table of Contents, organized by product line (page 1.2), or with the Numeric Table of Contents (page 1.4). These indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION—contain initial descriptions (subject to change) for products that are in development, including features and block diagrams.

PRELIMINARY—contain descriptions for products soon to be, or recently released to production, including features, pinouts, and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL—contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types, and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types, and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

1995 LOGIC DATA BOOK
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QUALITY AND RELIABILITY

PACKAGE DIAGRAM OUTLINES

DOUBLE DENSITY 5V LOGIC PRODUCTS

BALANCED DRIVE OUTPUT (with Series Resistors)

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CMOS-LEVEL OUTPUT

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CMOS-LEVEL OUTPUT (CONTINUED)

3.3V LOGIC PRODUCTS

DOUBLE-DENSITY

OCTALS

BIDIRECTIONAL 3V TO 5V TRANSLATORS

CLOCK MANAGEMENT PRODUCTS

5V CLOCK DRIVERS/BUFFERS

3.3V CLOCK DRIVERS/BUFFERS

5V PLL CLOCK GENERATORS

3.3V PLL CLOCK GENERATORS

BUS SWITCH PRODUCTS

5V BUS SWITCH (5Ω)

5V BUS SWITCH (28Ω)

COMPLEX LOGIC PRODUCTS

DSP AND MICROSLICE™ PRODUCTS

DSP AND MICROSLICE™ PRODUCTS

READ/WRITE BUFFER/BUS MULTIPLEXER PRODUCTS

ERROR DETECTION AND CORRECTION PRODUCTS

IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

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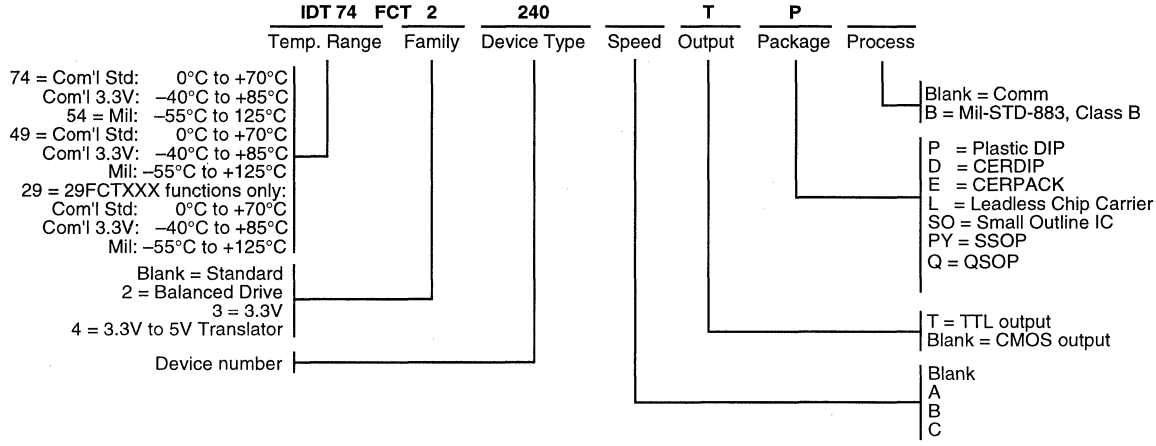
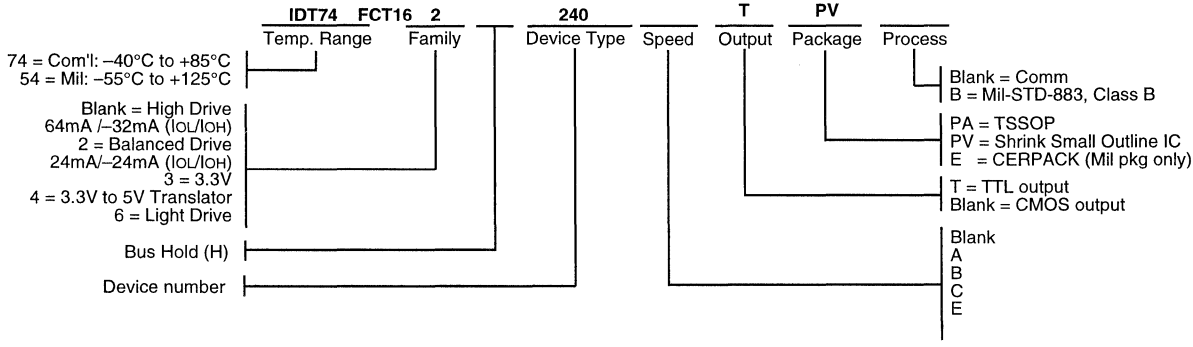
NUMERICAL TABLE OF CONTENTS (CONTINUED)

ORDERING INFORMATION

FCTXXX, FCTXXXT

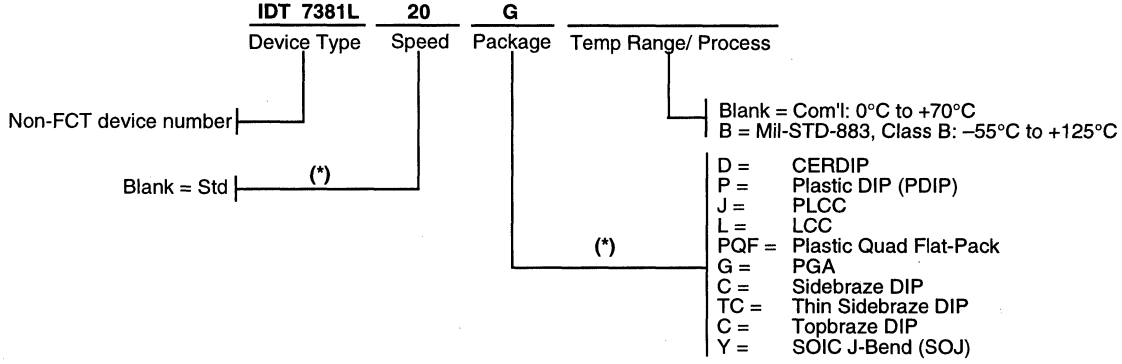


FCT16XXX, 16XXXT (Double Density)



ORDERING INFORMATION

NON-FCT DEVICES



- Please refer to table below for speed and package availability.

NON-FCT DEVICE REFERENCE TABLE

Device	Speed		Package
	Commercial	Military	
49C402	Std., A, B	Std., A, B	PGA, PLCC
49C460	Std., A, B, C, D	Std., A, B, C, D	PGA, PLCC
49C465	Std., A	Std., A	PQF, PGA
49C466	Std.	Std.	PQF, PGA
7210L	25, 35, 45, 55, 65	30, 40, 55, 65, 75	PGA, PDIP, PLCC, Topbraze
7216L	20, 25, 35, 45, 55, 65	25, 30, 40, 55, 65, 75	PGA, PDIP, PLCC, Topbraze
7217L	20, 25, 35, 45, 55, 65	25, 30, 40, 55, 65, 75	PGA, PDIP, PLCC, Topbraze
7381L	20, 25, 30, 40, 55	25, 30, 35, 45, 65	PLCC, PGA
73720	Std.	Std.	PQF, PLCC

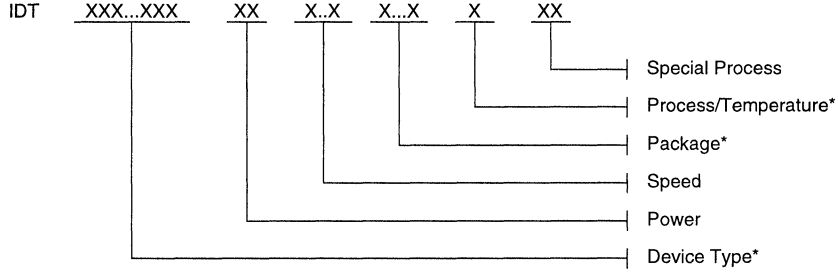
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard product's power.
   "L" or "LA" is used for lower power than the standard product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

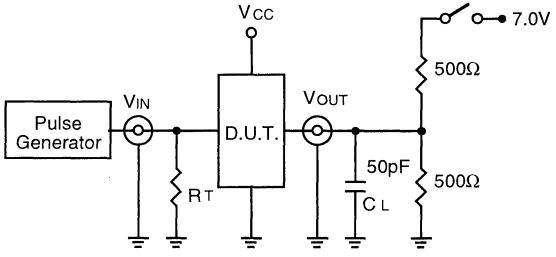
IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

EXAMPLE FOR SUBSYSTEM MODULES

See Ordering Information (section 1.4), page 2.

TEST CIRCUITS AND WAVEFORMS
FCTXXX, FCTXXXT, FCT16XXXT - 5V FAMILIES

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

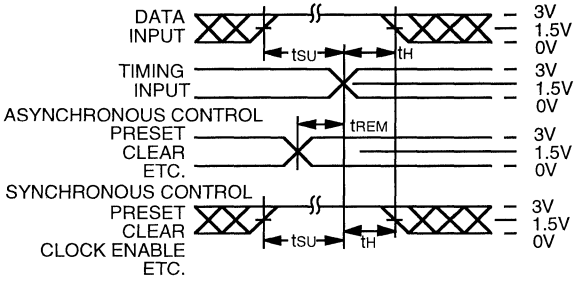
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

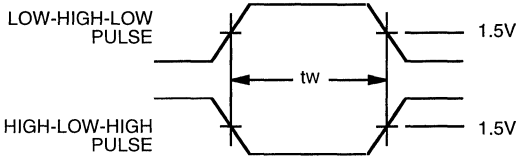
CL= Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

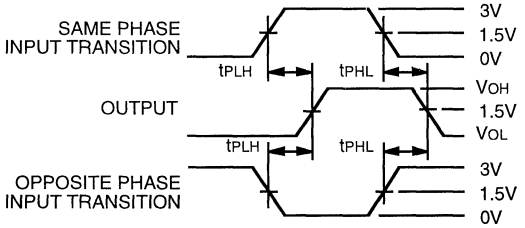
SET-UP, HOLD AND RELEASE TIMES



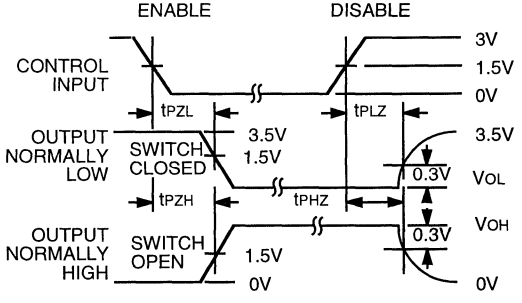
PULSE WIDTH



PROPAGATION DELAY

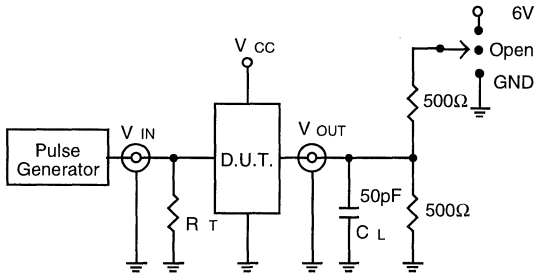


ENABLE AND DISABLE TIMES



TEST CIRCUITS AND WAVEFORMS
FCT3XXX AND FCT163XXX - 3.3V FAMILY

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

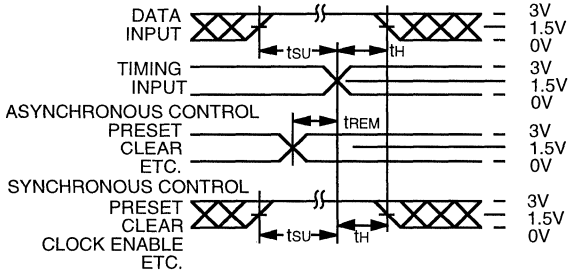
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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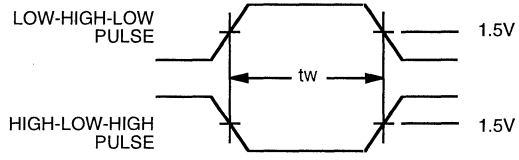
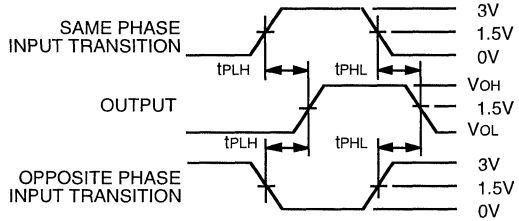
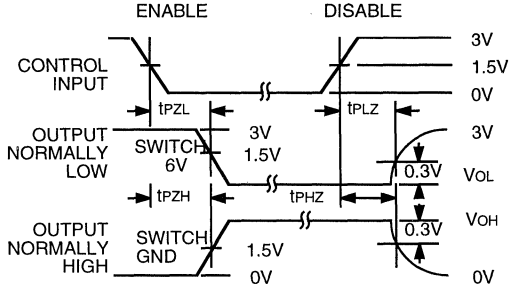


PROPAGATION DELAY



ENABLE AND DISABLE TIMES



SECTION 2
TECHNOLOGY AND CAPABILITIES
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2

TECHNOLOGY AND CAPABILITIES

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 Static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CMOS technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of its extremely fast CMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Manufacturing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive, and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM , FCT logic, high-density modules, FIFOs, multi-port memories, BiCMOS ECL I/O memories, RISC SubSystems, and the 32- and 64-bit RISC microprocessor families complement each other to provide high-speed CMOS solutions for a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families, and additional product families are being introduced. Contact your IDT field representative or factory marketing engineer for information on the most current product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of militarized products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has 88 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-89891	7198
5962-89892	6198
5962-89690	6116
5962-38294	7164
5962-89692	7188
5962-89712	71982
5962-89790	71682
SMP	**IDT**
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133SA/7143SA
5962-88665	7133LA/7143LA
5962-89764	7134
5962-91508	7006
5962-91617	7025
5962-91662	7024
5962-93153	7014S
FIFO	**IDT**
5962-87531	7201LA
5962-86846	72404L
5962-88669	7203S
5962-89568	7204L
5962-89536	7202LA
5962-89863	7201SA
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L
5962-90715	7204S
5962-91677	7205L

SMD	
5962-93177	7206L
5962-92069	72141L
5962-92101	72215LB
5962-93138	72220L
5962-92057	72225LB
5962-93189	72245LB
5962-91757	72200L
CLP	**IDT**
5962-87708	39C10B & C
5962-88533	49C460A/B/C
5962-88613	39C60/A
5962-88643	49C410
5962-86873	7216L
5962-87686	7217L
5962-88733	7210
5962-92122	49C465/A
LOGIC	**IDT**
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646/A
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88653	54FCT645/A

SMD	
5962-88654	54FCT640/A
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
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5962-89730	54FCT543/A
5962-90901	29FCT52A/B/C
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5962-92211	54FCT257T/AT/CT
5962-92215	54FCT273T/AT/CT
5962-92216	54FCT299T/AT/CT
5962-92217	54FCT373T/AT/CT
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5962-92234	54FCT521T/AT/BT/CT
5962-92236	54FCT534T/AT/CT
5962-92220	54FCT540T/AT/CT
5962-92237	54FCT541T/AT/CT
5962-92221	54FCT543T/AT/CT
5962-92238	54FCT573T/AT/CT
5962-92222	54FCT574T/AT/CT
5962-92244	54FCT645T/AT/CT
5962-92223	54FCT646T/AT/CT
5962-92246	54FCT652T/AT/CT
5962-92225	54FCT821AT/BT/CT
5962-92229	54FCT823AT/BT/CT
5962-92230	54FCT825AT/BT/CT
5962-92247	54FCT827AT/BT/CT
RISC	**IDT**
5962-94550	79R3081E

SMD

SRAM	IDT
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-89891	7198
5962-89892	6198
5962-89690	6116
5962-38294	7164
5962-89692	7188
5962-89712	71982
5962-89790	71682

SMP	IDT
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133SA/7143SA
5962-88665	7133LA/7143LA
5962-89764	7134
5962-91508	7006
5962-91617	7025
5962-91662	7024
5962-93153	7014S

FIFO	IDT
5962-87531	7201LA
5962-86846	72404L
5962-88669	7203S
5962-89568	7204L
5962-89536	7202LA
5962-89863	7201SA
5962-89523	72403L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L
5962-90715	7204S
5962-91677	7205L
5962-93177	7206L
5962-92069	72141L
5962-92101	72215LB
5962-93138	72220L
5962-92057	72225LB
5962-93189	72245LB
5962-91757	72200L

CLP	IDT
5962-87708	39C10B & C
5962-88533	49C460A/B/C
5962-88613	39C60/A
5962-88643	49C410
5962-86873	7216L
5962-87686	7217L
5962-88733	7210
5962-92122	49C465/A

LOGIC	IDT
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646/A
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88653	54FCT645/A
5962-88654	54FCT640/A
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89732	54FCT241/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-89730	54FCT543/A
5962-90901	29FCT52A/B/C
5962-92205	29FCT520AT/BT/CT
5962-92157	49FCT805/A/806/A
5962-92233	54FCT138T/AT/CT
5962-92208	54FCT157T/AT/CT
5962-92209	54FCT161T/AT/CT
5962-92210	54FCT163T/AT/CT
5962-90669	54FCT193/A
5962-92213	54FCT240T/AT/CT
5962-92232	54FCT241T/AT/CT
5962-92203	54FCT244T/AT/CT
5962-92214	54FCT245T/AT/CT
5962-92211	54FCT257T/AT/CT
5962-92215	54FCT273T/AT/CT
5962-92216	54FCT299T/AT/CT
5962-92217	54FCT373T/AT/CT
5962-92218	54FCT374T/AT/CT
5962-92219	54FCT377T/AT/CT
5962-92212	54FCT399T/AT/CT
5962-92234	54FCT521T/AT/BT/CT
5962-92236	54FCT534T/AT/CT
5962-92220	54FCT540T/AT/CT
5962-92237	54FCT541T/AT/CT
5962-92221	54FCT543T/AT/CT
5962-92238	54FCT573T/AT/CT
5962-92222	54FCT574T/AT/CT
5962-92244	54FCT645T/AT/CT
5962-92223	54FCT646T/AT/CT
5962-92246	54FCT652T/AT/CT
5962-92225	54FCT821AT/BT/CT
5962-92229	54FCT823AT/BT/CT
5962-92230	54FCT825AT/BT/CT
5962-92247	54FCT827AT/BT/CT

RISC	IDT
5962-94550	79R3081E

RADIATION HARDENED TECHNOLOGY

On an order by order basis IDT can manufacture and supply radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices survive in hostile radiation environments. In Total Dose, Dose Rate, and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply most of its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

KNOWN GOOD DIE

Emerging high performance electronic systems require smaller and smaller form-factors. IDT is meeting these design challenges by offering Known Good Die (KGD) in addition to its broad array of small form-factor packages. The IDT KGD manufacturing process enables IDT to offer die that have received the same electrical tests, burn-in, and speed sorting at elevated temperatures as shipped packaged products. Via IDT KGD, users are able to manufacture cost-efficient and reliable multi-chip modules (MCMs), hybrids, and other high-density interconnect products. All IDT KGD, at the completion of their test flow, receive 100% die visual inspection and are packed within Gel-Pak™ containers. The Gel-Pak™ containers are then placed in vacuum sealed ESD wrappers prior to shipping. Delivered KGD products have superior yield, quality, and reliability over standard raw die offerings. Most IDT products can be offered as "KGD", and commercial, industrial or military temperatures can be considered.

THE PRODUCTIVITY REVOLUTION

New microprocessor-based systems enhance productivity by improving the accessibility and usability of information. By connecting systems through a network, data can be transmitted instantly, anywhere in the world. Using affordable computing systems, information can be located, retrieved, analyzed, and displayed as needed.

The systems that provide these capabilities are built around the microprocessor, and IDT's products maximize the potential of these microprocessor-based systems. As sales of these productivity-enhancing systems grow, so do the markets for IDT products.

INNOVATIVE PRODUCTS FOR MORE PRODUCTIVE SYSTEMS

IDT markets products from four product groups: SRAMs, Specialty Memory Products, Logic products, and RISC Microprocessors.

Our strategy is to define, develop, and manufacture products that help our customers deliver greater value to their customers. We develop products in partnership with customers who are leaders in markets that fuel the productivity revolution, such as high-performance desktop and server computing, data communications and networking, and office automation. These customers use our products to build systems that are faster, less costly, and more productive.

Our customers are also building systems that are energy-efficient. Designers are developing 3.3V systems to comply with the governmental Energy Star requirements. We have a competitive advantage because our CMOS VII technology was specifically designed to maintain higher speeds at this lower voltage.

Customers using high-performance microprocessors to build desktop computers and file servers can improve the performance of their products by incorporating cache memory systems. Cache memory systems are constructed with high-speed SRAMs, cache tag memories, and control logic. We are a recognized technology leader in SRAMs and the world's leading supplier of cache tag memories. Today, we supply these products both as discrete components and in the form of complete high-density cache memory modules used with PowerPC™, Intel 486™, Pentium™ processor, and our own RISC microprocessors. We are working with manufacturers of both the microprocessors and their associated chipsets to develop new cache memory products that will maximize the performance of future microprocessor-based systems.

Customers building digital data communications and networking equipment use FIFO and dual-port memory products that are designed for these applications. FIFOs and dual-ports are uniquely suited to exchanging data between systems that operate at different speeds or use different protocols, a common requirement in communications systems. We are the market leader in these SMP product areas, and we have introduced the industry's largest number of product and technology innovations over the years. Development work is now under way to design a family of products for the emerging ATM (Asynchronous Transfer Mode) market, which is expected to grow dramatically over the next several years.

Every high-performance system needs high-speed logic parts to connect memories, microprocessors, communications circuits, and other system components. We have been the performance leader in high-speed FCT logic devices since we pioneered these products in 1985, and we currently offer more than 150 different logic products. We have also introduced two new ultra-small packaging choices for our logic products, ideal for use in compact desktop and portable systems, as well as in PCMCIA cards, which are credit-card sized modules that add functionality to personal computers.

Customers who build high-performance office automation and communications systems are taking advantage of our family of 32-bit and 64-bit software-compatible RISC microprocessors, based on the extendable architecture developed by MIPS Technologies. The 20+ different microprocessors in our RISC family offer customers a wider range of price/performance choices than competing microprocessor families. Software compatibility allows designers to choose one microprocessor for a particular product and then easily upgrade to a higher-performing version, in many cases simply by removing one device and plugging in another. Our 32-bit RISC microprocessor products are winning acceptance in a variety of embedded applications, including laser printers, network routers, and graphics display terminals.

In fiscal 1994, we introduced our 64-bit R4600™ Orion™ processor. This microprocessor provides leading-edge performance for embedded applications, such as laser printers and networking systems, and is also used in file servers and workstations that run UNIX® and Microsoft's new Windows NT™ operating systems.

ADVANCING OUR OWN PRODUCTIVITY

We participate in the productivity revolution both as a technology enabler and as a beneficiary. While our products enhance the productivity of our customers' microprocessor-based systems, we improve our own internal productivity by developing new manufacturing technologies, re-engineering workflows, and by adopting new electronic systems.

One of the primary ways we increase internal productivity is by developing and implementing advanced technologies. New process technologies result in smaller die, and new production equipment allows the use of larger wafers. The combination of smaller die and larger wafers allows us to generate significantly more devices per wafer. Migrating to an advanced 0.6-micron CMOS fabrication process in fiscal 1994 not only resulted in smaller die, it also improved product performance, increased yields, and lowered unit costs. Our new CMOS VIII 0.5-micron process is expected to extend our

process technology momentum.

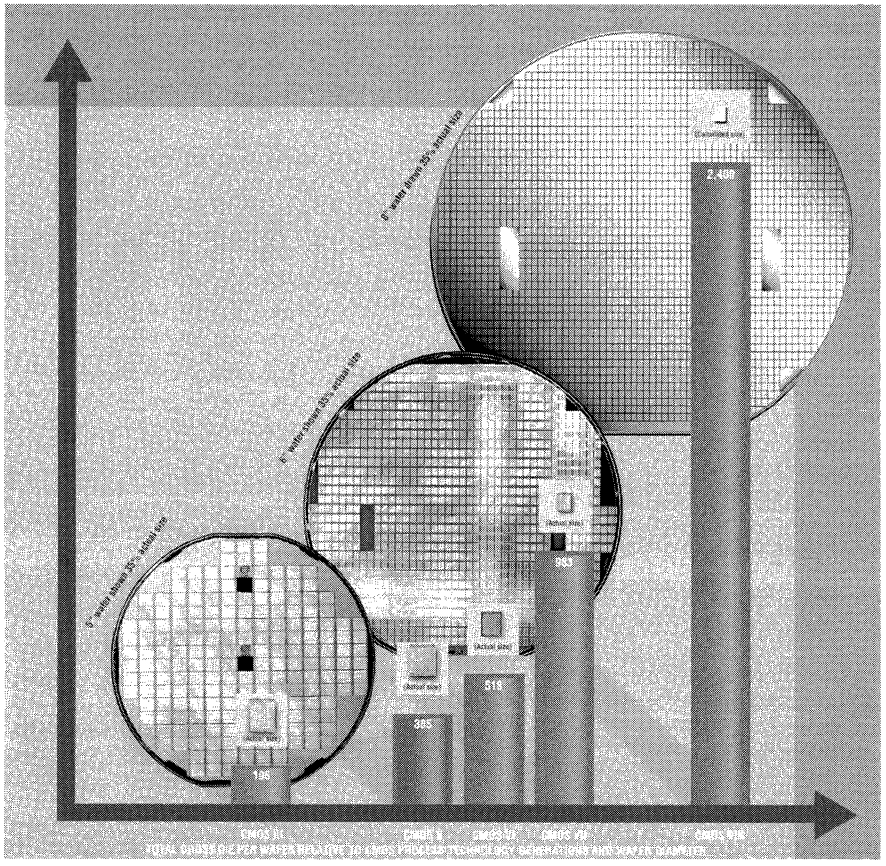
Because we have our own fabrication facilities, we control critical manufacturing operations, giving us a competitive advantage as we continue to improve our productivity. IDT has two sub-micron 6" wafer fabrication facilities, located in San José and Salinas, California, and a high-volume assembly and test facility in Penang, Malaysia. To support future growth, we have built a new sub-micron 8" wafer fabrication facility in Hillsboro, Oregon that will be fully operational in fiscal 1997, and an additional 40,000-square-foot building for test and assembly in Penang.

Manufacturing productivity is also improved by adjusting work schedules to increase the output from equipment already in place and improving product development cycles. Updated computer-aided design tools shorten product design times and improve the functionality of new product prototypes. For example, the R4600 Orion processor was designed by Quantum Effect Design, Inc., an IDT affiliate operating on-site, in just 21 months, which is a remarkably short development cycle for such a complex product.

Improvements in quality are the direct result of improvements in productivity. Our manufacturing quality levels have been improving for several years. In fiscal 1993, IDT was one of the first semiconductor companies to achieve ISO 9000 registration for wafer fabrication activities. ISO 9000 is a worldwide quality systems standard, and certification provides an important competitive advantage in both domestic and international markets. All of our manufacturing facilities are now ISO 9000 certified.

Customer service and support have been directly enhanced by many of our productivity improvements. New planning and scheduling systems allow us to improve our efficiency and predictability for meeting delivery commitments to customers. Expanded computer systems allow the migration of order services to field sales offices, bringing support closer to the customer. Increased use of EDI (Electronic Data Interchange) allows customers to directly enter orders and check order status, resulting in more timely information with less paperwork.

Improving productivity continues to be a key issue for technology companies. By continuing to improve internal productivity and manufacture quality products that support the productivity revolution, we expect to enhance the value of our company to our shareholders, our employees, and our customers.



SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-I-38535, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform Class S processing per MIL-STD-883 and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/ aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

SECTION 3
QUALITY AND RELIABILITY
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QSP–QUALITY, SERVICE AND PERFORMANCE

Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Continuous Quality Improvement (CQI) process. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the quality of their actions.

IDT QUALITY PHILOSOPHY

"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

IDT's ASSURANCE STRATEGY FOR CQI

Measurable standards are essential to the success of CQI. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.

PRODUCT FLOW

DEVELOPMENT
|
FAB
|
ASSEMBLY
|
TEST
|
SHIP

Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.

SERVICE FLOW

ORDER ENTRY
|
PRODUCTION CONTROL
|
SHIPPING
|
CUSTOMER SUPPORT

These systems and controls concentrate on CQI by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the CQI process into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing
To accomplish CQI during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality -of -service we give our customers. Services is also constantly monitored for improvement.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the CQI process, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly impinges on the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier also has to adopt these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to CQI is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer.When failures are found at the customer's incoming inspection, in the production line, or the field application, the Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers that have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following that credo IDT and our cusotmers will be successful in the coming decade.With the implementation of the CQI strategy within the company, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests, patterned after MIL-STD-883, Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull and ball shear tests to ensure the integrity of the wire bond process, patterned after MIL-STD-883, Method 2011, Condition D.

5. **Pre-Cap Visual:** Before encapsulation, all product lots are visually inspected (using LTPD 5 sampling plan) to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum polymerization of the epoxy mold compound so as to enhance moisture resistance characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in for 16 hours at +125°C minimum (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers. Products are identified with the assembly and test locations.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

TABLE 1

This table defines the device class screening procedures for IDT's high reliability products in conformance with MIL-STD-883C.

Monolithic Hermetic Package Final Processing Flow

	CLASS-S		CLASS-B		CLASS-C [1]	
OPERATION	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**
BURN-IN	1015 Cond. D, 240 Hrs @ 125°C or equivalent	100%	1015 Cond. D, 160 Hrs. @ 125°C min or equivalent	100%	Per applicable device specification	100%
POST BURN-IN ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification +25, -55 and 125°C	100%	Per applicable device specification +25, -55 and 125°C	100%	Per applicable [2] device specification	100%
Group A ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification and 5005	Sample	Per applicable device specification and 5005	Sample	Per applicable [2] device specification	Sample
MARK/LEAD STRAIGHTENING	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
FINAL ELECTRICAL TEST	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%
FINAL VISUAL/PACK	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
QUALITY CONFORMANCE INSPECTION	5005 Group B, C, D.	Sample	5005 Group B,C,D.	Sample	IDT Spec	Sample
QUALITY SHIPPING INSPECTION (Visual/Plant Clearance)	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%

NOTES:
1. Class-C = IDT commercial spec. for hermetic and plastic packages
2. Typical 0°C, 70°C, Extended -55°C +125°C

SECTION 4
PACKAGE DIAGRAM OUTLINES
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PACKAGE DIAGRAM OUTLINES

4

THERMAL PROFILE AND PACKAGE DIAGRAM OUTLINE INDEX

Package	Description	θja	θjc	Thermal Figure Number	Package Diagram Page Number
SSOP (PY)					
SO20-7	20-Pin Shrink Small Outline Package	110	55	1	1
SO24-7	24-Pin Shrink Small Outline Package	100	55	1	1
SO28-7	28-Pin Shrink Small Outline Package	90	55	—	1
SSOP (PV)					
SO48-1	48-Pin Shrink Small Outline Package	80	45	1	3
SO56-1	56-Pin Shrink Small Outline Package	70	45	1	3
QSOP (Q)					
SO16-7	16-Pin Quarter Size Outline Package	150	60	—	5
SO20-8	20-Pin Quarter Size Outline Package	135	60	—	5
SO24-8	24-Pin Quarter Size Outline Package	115	60	—	5
SO28-9	28-Pin Quarter Size Outline Package	100	60	—	5
TSSOP (PA)					
SO48-2	48-Pin Thin Shrink Small Outline Package	93	50	2	7
SO56-2	56-Pin Thin Shrink Small Outline Package	84	50	2	7
SOIC (SO)					
SO16-1	16-Pin Small Outline IC (gull wing)	105	38	—	5
SO18-1	18-Pin Small Outline IC (gull wing)	95	35	—	5
SO20-2	20-Pin Small Outline IC (gull wing)	90	33	—	5
SO24-2	24-Pin Small Outline IC (gull wing)	75	28	—	5
SO28-2	28-Pin Small Outline IC (gull wing)	67	25	—	6
PDIP (P)					
P16-1	16-Pin Plastic DIP (300 mil)	105	55	—	8
P18-1	18-Pin Plastic DIP (300 mil)	95	55	—	9
P20-1	20-Pin Plastic DIP (300 mil)	85	55	—	9
P22-1	22-Pin Plastic DIP (300 mil)	80	55	—	8
P24-1	24-Pin Plastic DIP (300 mil)	77	55	—	9

Package	Description	θja	θjc	Thermal Figure Number	Package Diagram Page Number
CERDIP (D)					
D16-1	16-Pin CERDIP (300 mil)	95	35	—	21
D20-1	20-Pin CERDIP (300 mil)	85	30	—	21
D24-1	24-Pin CERDIP (300 mil)	75	25	—	21
SIDEBRAZE DIP (C)					
C48-2	48-Pin Sidebraze DIP (600 mil)	55	8	—	22
C64-2	64-Pin Sidebraze DIP (900 mil)	25	8	—	23
LCC (L)					
L20-2	20-Pin Leadless Chip Carrier (square)			5	24
L28-1	28-Pin Leadless Chip Carrier (square)			5	24
L32-1	32-Pin Leadless Chip Carrier (rectangular)			5	24
CERPACK (E)					
E16-1	16-Lead CERPACK	85	20	—	25
E20-1	20-Lead CERPACK	80	17	—	25
E24-1	24-Lead CERPACK	75	15	—	25
E48-1	48-Lead CERPACK	68	12	7	26
E56-1	56-Lead CERPACK	63	11	7	26
PLCC (J)					
J68-1	68-Pin Plastic Leaded Chip Carrier (square)	40	20	—	15
PGA (G)					
G68-1	68-Lead Pin Grid Array (cavity up)	45	5	10	27
G84-1	84-Lead Pin Grid Array (cavity up)			10	28
G144-2	144-Lead Pin Grip Array (cavity up—R3001)	30	5	11	29
G208-1	208-Lead Pin Grid Array (cavity down)	30	—	12	30
PLASTIC QUAD FLAT-PACK (PQF)					
PQ80-1	80-Lead Plastic Quad Flatpack (EIAJ)	53	8	—	17
PQ144-2	144-Lead Plastic Quad Flatpack (EIAJ)	45	17	—	20
PQ208-2	208-Lead Plastic Quad Flatpack (EIAJ)	35	17	13	20

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CMOS process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_o \exp \left[\frac{Ea}{k} \left(\frac{1}{T_O} - \frac{1}{T_J} \right) \right]$$

where

t_A = lifetime at elevated junction (T_J) temperature
t_O = normal lifetime at normal junction (T_O) temperature
E_a = activation energy (ev)
k = Boltzmann's constant (8.617×10^{-5}ev/k)
i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

IDT recommends the maximum junction temperature be limited to:

$$T_J \text{ max} = 150°C$$

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883_ to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package materials and package geometry. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

where

$$\theta_{JC} = \frac{T_J - T_C}{P} \qquad \theta_{CA} = \frac{T_C - T_A}{P}$$

θ = Thermal resistance
J = Junction
P = Operational power of device (dissipated)
T_A = Ambient temperature in degree celsius
T_J = Temperature of the junction
T_C = Temperature of case/package
θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.

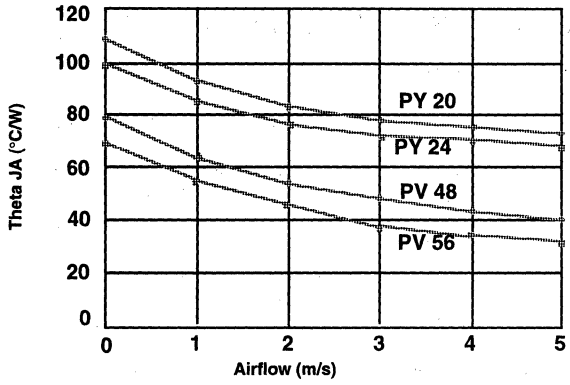


Figure 1. 20/24-Pin SSOPs
Theta JA

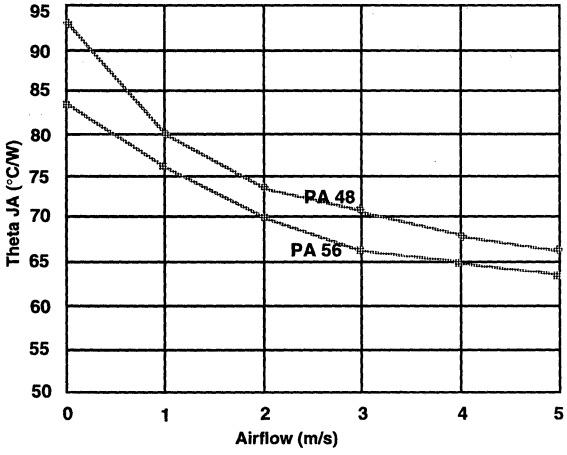
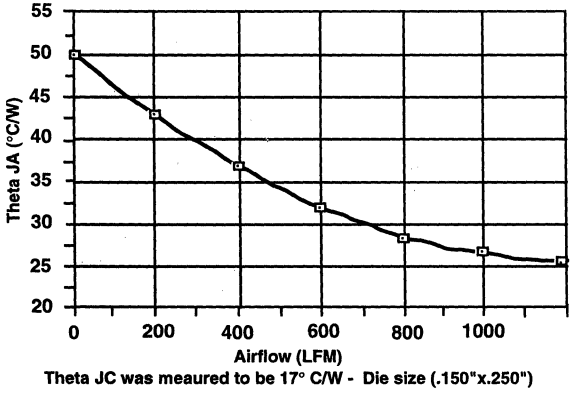


Figure 2. 48/56 Pin TSSOP



Theta JC was meaured to be 17° C/W - Die size (.150"x.250")

Figure 3. 32-Pin SOIC (SO)
Theta JA

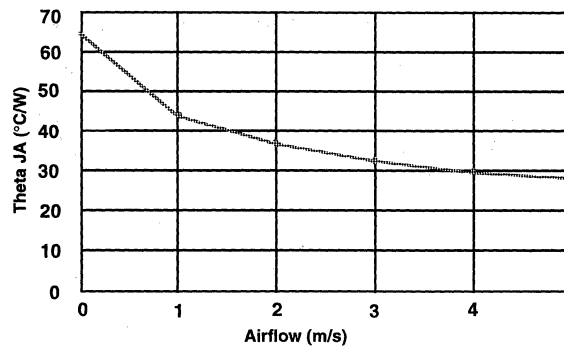


Figure 4. 28-Pin Plastic Dip
Theta JA

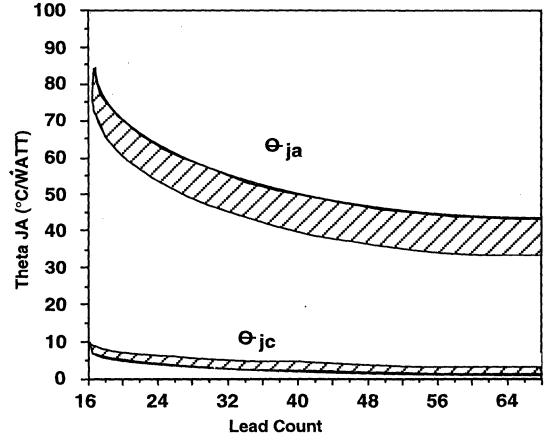


Figure 5. LCC (L)
Theta JA/Theta JC

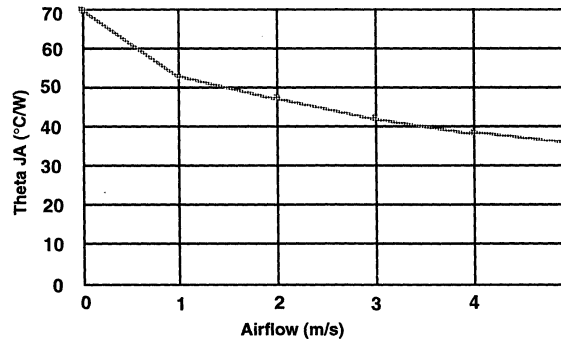


Figure 6. 28-Pin CERPACK

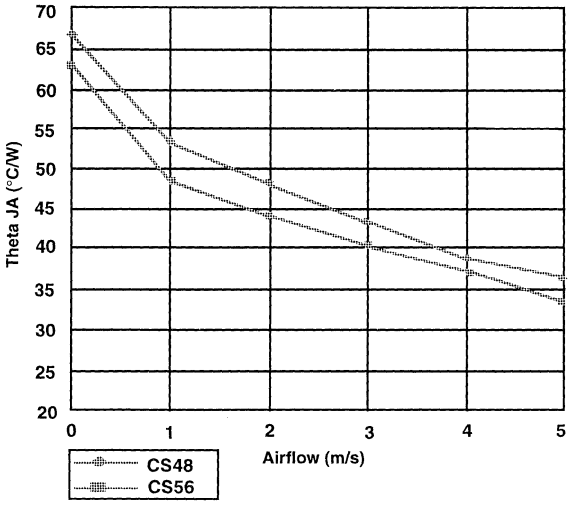


Figure 7. 48/56-Pin CERPACK
Theta JA

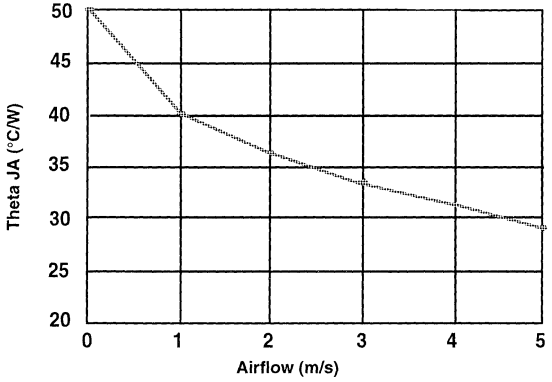


Figure 8. 32-Pin PLCC

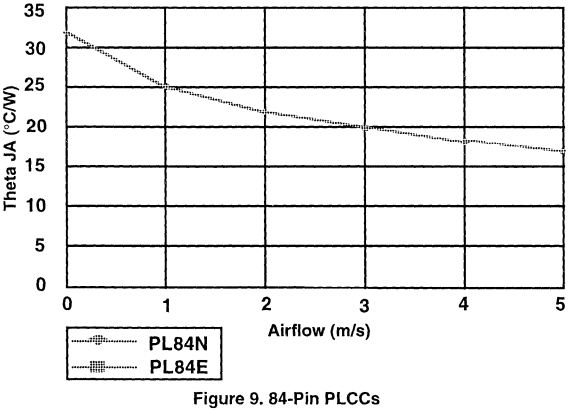


Figure 9. 84-Pin PLCCs
Normal & Enhanced

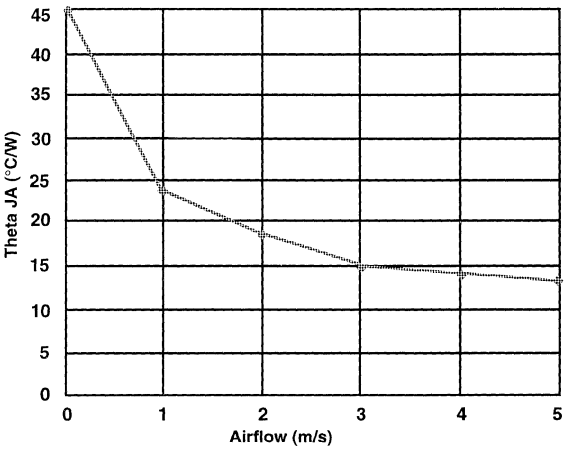


Figure 10. 68-Pin PGA
Theta JA
Cavity Up without internal heatsink

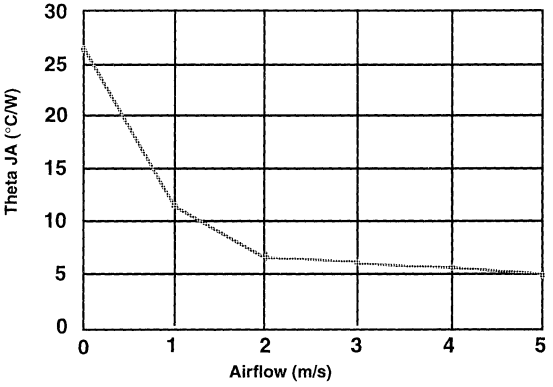


Figure 11. 144-Pin PGA
Theta JA
Cavity Down with CuW internal heatsink

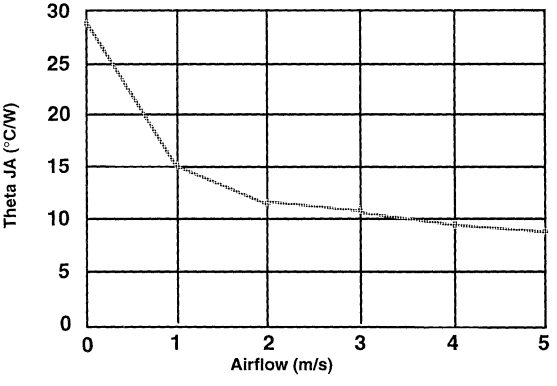
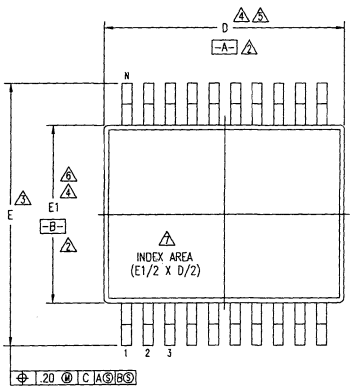


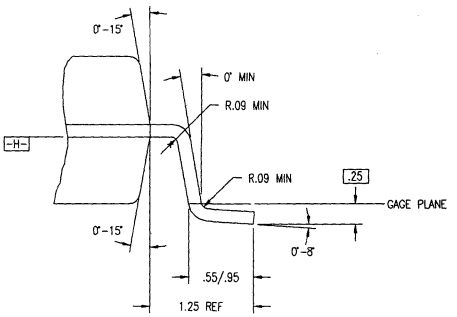
Figure 12. 208-Pin PGA
Theta JA
Cavity Down without internal heatsink

4

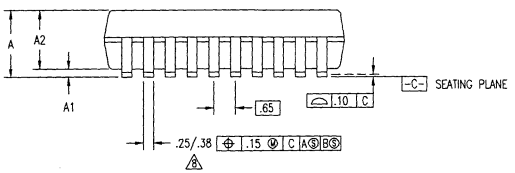
SSOP

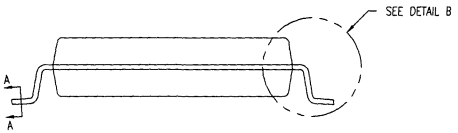
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20286	00	INITIAL RELEASE	04/15/91	T. VU
24536	01	ADD 28 LD	07/27/93	T. VU
27493	02	REDRAW TO JEDEC FORMAT	03/15/95	

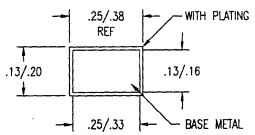




DETAIL B







SECTION A-A

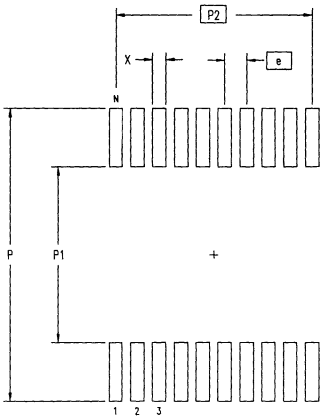
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL	ANGULAR		
XX±	±		
XXX±			
XXXX±			
APPROVALS	DATE	TITLE PY PACKAGE OUTLINE 5.3 mm BODY WIDTH SSOP .65 mm PTICH	
DRAWN AA	04/15/91		
CHECKED		SIZE C	DRAWING No. PSC-4032 REV 02
		DO NOT SCALE DRAWING	SHEET 1 OF 2

SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
20286	00	INITIAL RELEASE	04/15/91	T. VU
24536	01	ADD 28 LD	07/27/93	T. VU
27493	02	REDRAW TO JEDEC FORMAT	03/15/95	

SYMBOL	DWG # S020-7 JEDEC VARIATION AE			NOTE	DWG # S024-7 JEDEC VARIATION AG			NOTE	DWG # S028-7 JEDEC VARIATION AH			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	1.73	1.86	1.99		1.73	1.86	1.99		1.73	1.86	1.99	
A1	.05	.13	.21		.05	.13	.21		.05	.13	.21	
A2	1.68	1.73	1.78		1.68	1.73	1.78		1.68	1.73	1.78	
D	7.07	7.20	7.33	4,5	8.07	8.20	8.33	4,5	10.07	10.20	10.33	4,5
E	7.65	7.80	7.90	3	7.65	7.80	7.90	3	7.65	7.80	7.90	3
E1	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6
N	20				24				28			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX
P	8.60	8.80	8.60	8.80	8.60	8.80
P1	5.10	5.30	5.10	5.30	5.10	5.30
P2	5.85 BSC		7.15 BSC		8.45 BSC	
X	.30	.40	.30	.40	.30	.40
e	.65 BSC		.65 BSC		.65 BSC	
N	20		24		28	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .20 mm PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .20 mm PER SIDE

7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .13 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

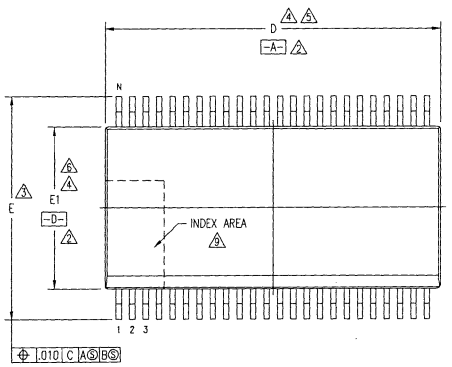
10 ALL DIMENSIONS ARE IN MILLIMETERS

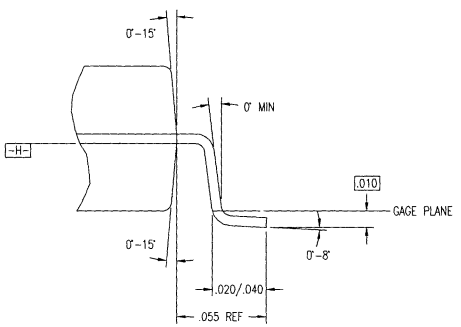
11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-150, VARIATION AE, AG & AH

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE	PY PACKAGE OUTLINE 5.3 mm BODY WIDTH SSOP .65 mm PTICH
DRAWN dd	04/15/91		
CHECKED		SIZE C	DRAWING No. PSC-4032 REV 02
		DO NOT SCALE DRAWING	SHEET 2 OF 2

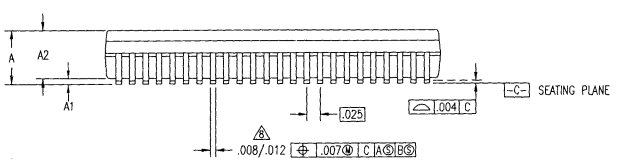
SSOP (Continued)

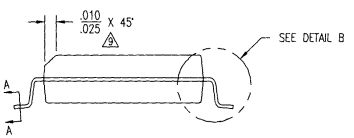
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

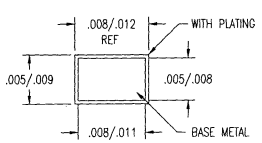




DETAIL B







SECTION A-A

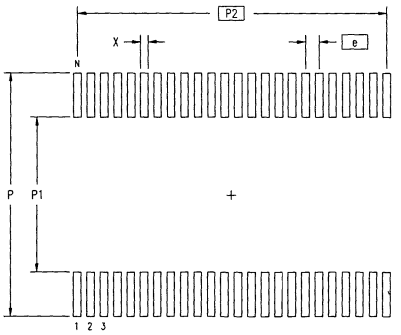
TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
APPROVALS / DRAWN / CHECKED	DATE: 06/15/90	TITLE: PV PACKAGE OUTLINE .300" BODY WIDTH SSOP .025" PITCH	
		SIZE: C	DRAWING No.: PSC-4029 REV: 02
		DO NOT SCALE DRAWING	SHEET 1 OF 2

SSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

SYMBOL	DWG # SO48-1 JEDEC VARIATION AA			NOTE	DWG # SO56-1 JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.102	.110		.095	.102	.110	
A1	.008	.012	.016		.008	.012	.016	
A2	.088	.090	.092		.088	.090	.092	
D	.620	.625	.630	4,5	.720	.725	.730	4,5
E	.395	.405	.420	3	.395	.405	.420	3
E1	.291	.295	.299	4,6	.291	.295	.299	4,6
N	48				56			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

10 ALL DIMENSIONS ARE IN INCHES

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARATION AA & AB

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN	06/15/90
CHECKED	

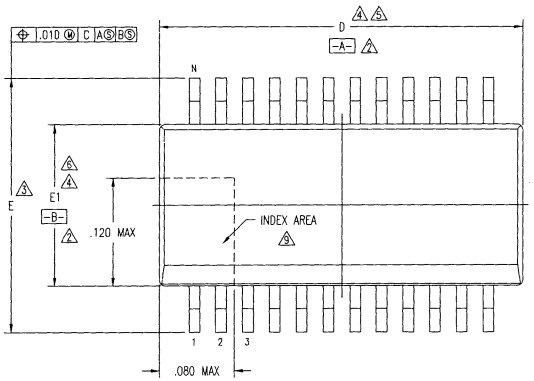
TITLE PV PACKAGE OUTLINE
.300" BODY WIDTH SSOP
.025" PITCH

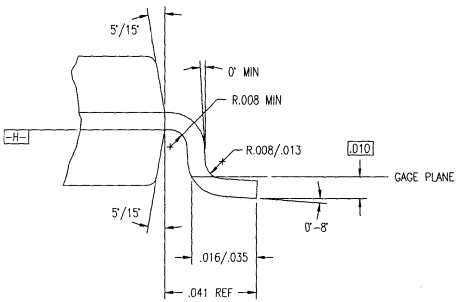
SIZE C | DRAWING No. PSC-4029 | REV 02

DO NOT SCALE DRAWING | SHEET 2 OF 2

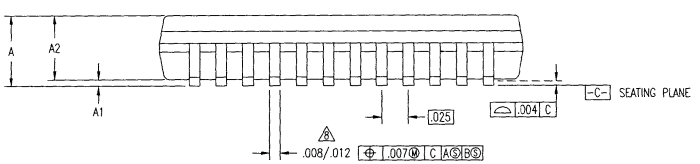
QSOP

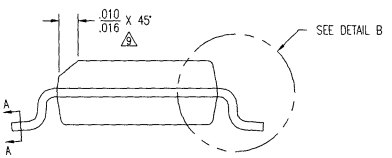
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
25338	00	INITIAL RELEASE	12/16/93	T. VU
27495	01	REDRAW TO JEDEC FORMAT	03/10/95	T. VU
28047	02	ADD 28 LD	08/15/95	

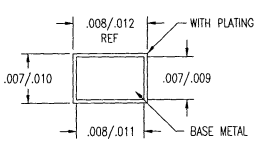




DETAIL B







SECTION A-A

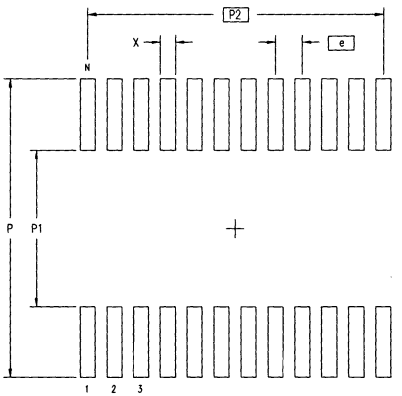
TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS	DATE	TITLE	PC PACKAGE OUTLINE .150" BODY WIDTH SSOP .025" PITCH
DRAWN AA	12/15/93		
CHECKED		SIZE C	DRAWING No. PSC-4040 REV 02
		DO NOT SCALE DRAWING	SHEET 1 OF 2

QSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
25338	00	INITIAL RELEASE	12/16/93	T. VU
27495	01	REDRAW TO JEDEC FORMAT	03/10/95	T. VU
28047	02	ADD 28 LD	08/15/95	

DWG #	SO16-7				DWG #	SO20-8			DWG #	SO24-8			DWG #	SO28-9		
SYMBOL	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE	JEDEC VARIATION AF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.061	.064	.068		.061	.064	.068		.061	.064	.068		.061	.064	.068	
A1	.004	.006	.010		.004	.006	.010		.004	.006	.010		.004	.006	.010	
A2	.055	.058	.061	11	.055	.058	.061	11	.055	.058	.061	11	.055	.058	.061	11
D	.189	.194	.196	4,5	.337	.342	.344	4,5	.337	.342	.344	4,5	.386	.390	.394	4,5
E	.230	.236	.244	3	.230	.236	.244	3	.230	.236	.244	3	.230	.236	.244	3
E1	.150	.155	.157	4,6	.150	.155	.157	4,6	.150	.155	.157	4,6	.150	.155	.157	4,6
N	16				20				24				28			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.274	.282	.274	.282	.274	.282	.274	.282
P1	.142	.150	.142	.150	.142	.150	.142	.150
P2	.175 BSC		.225 BSC		.275 BSC		.325 BSC	
X	.010	.018	.010	.018	.010	.018	.010	.018
e	.025 BSC		.025 BSC		.025 BSC		.025 BSC	
N	16		20		24		28	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

10 ALL DIMENSIONS ARE IN INCHES

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-137, VARIATION AB, AD, AE & AF. EXCEPTIONS: JEDEC DIMENSION A2 MAX IS .059

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN dd	12/15/93
CHECKED	

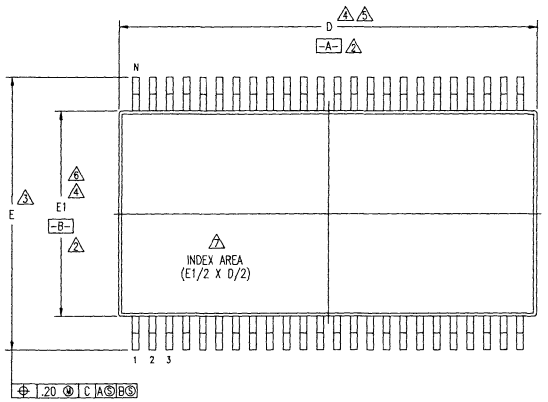
TITLE PC PACKAGE OUTLINE
.150" BODY WIDTH SSOP
.025" PITCH

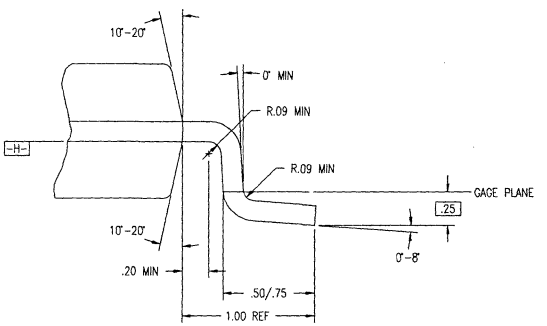
SIZE C | DRAWING No. PSC-4040 | REV 02

DO NOT SCALE DRAWING | SHEET 2 OF 2

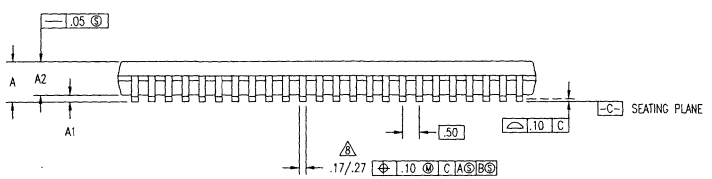
TSSOP

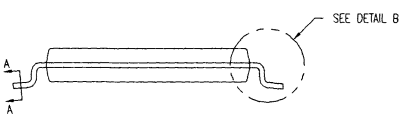
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

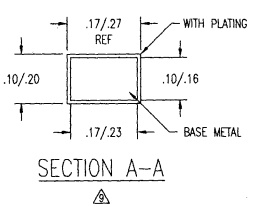




DETAIL B







SECTION A-A

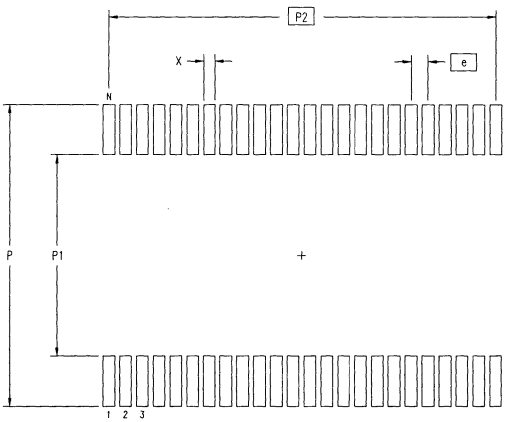
TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS	DATE	TITLE	PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH
DRAWN dd	01/15/93		
CHECKED			
		SIZE C	DRAWING No. PSC-4039 REV 03
		DO NOT SCALE DRAWING	SHEET 1 OF 2

TSSOP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

SYMBOL	DWG # S048-2 JEDEC VARIATION ED			NOTE	DWG # S056-2 JEDEC VARIATION EE			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.10		–	–	1.10	
A1	.05	–	.15		.05	–	.15	
A2	.85	1.00	1.05		.85	1.00	1.05	
D	12.40	12.50	12.60	4,5	13.90	14.00	14.10	4,5
E	7.95	8.10	8.25	3	7.95	8.10	8.25	3
E1	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6
N	48				56			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50 BSC		13.50 BSC	
X	.30	.40	.30	.40
e	.50 BSC		.50 BSC	
N	48		56	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE

7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

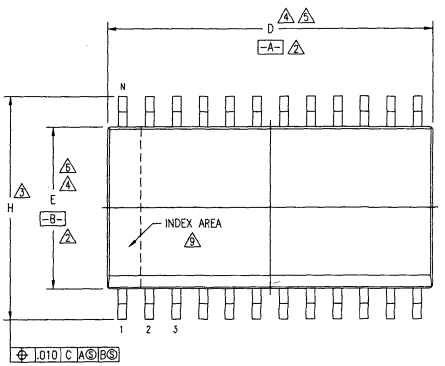
10 ALL DIMENSIONS ARE IN MILLIMETERS

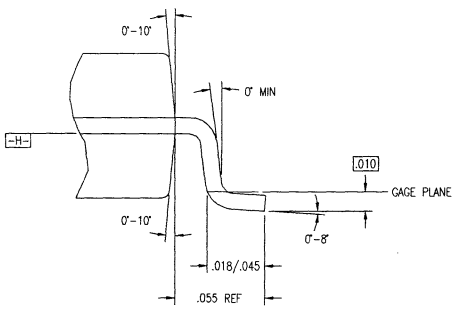
11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–153, VARIATION ED & EE

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS	DATE	TITLE	PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH
DRAWN dd	01/15/93		
CHECKED		SIZE C	DRAWING No. PSC-4039 REV. 03
		DO NOT SCALE DRAWING	SHEET 2 OF 2

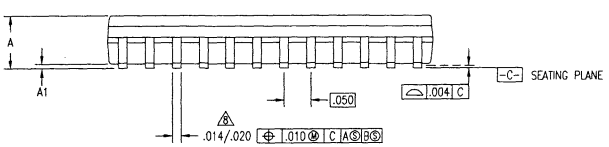
SOIC

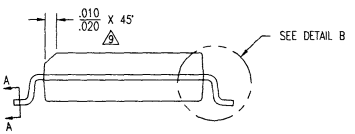
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27643	06	REDRAW TO JEDEC FORMAT	03/15/95	

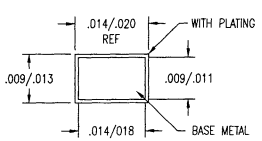




DETAIL B







SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
DECIMAL ANGULAR XX± ± XXX± XXXX±				
APPROVALS	DATE	TITLE PS PACKAGE OUTLINE .300" BODY WIDTH SOIC .050" PITCH		
DRAWN AA	03/15/89			
CHECKED		SIZE C	DRAWING No. PSC-4007	REV 06
		DO NOT SCALE DRAWING		SHEET 1 OF 3

SOIC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27643	06	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	SO16-1				DWG #	SO18-1			DWG #	SO20-2			DWG #	SO24-2			DWG #	SO28-2		
SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.100	.104		.095	.100	.104		.095	.100	.104		.095	.100	.104		.095	.100	.104	
A1	.005	.008	.012		.005	.008	.012		.005	.008	.012		.005	.008	.012		.005	.008	.012	
D	.403	.408	.413	4,5	.447	.454	.462	4,5	.497	.504	.511	4,5	.600	.607	.614	4,5	.700	.706	.712	4,5
E	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6	.292	.296	.299	4,6
H	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3	.400	.406	.419	3
N	16				18				20				24				28			

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION H TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

10 ALL DIMENSIONS ARE IN INCHES

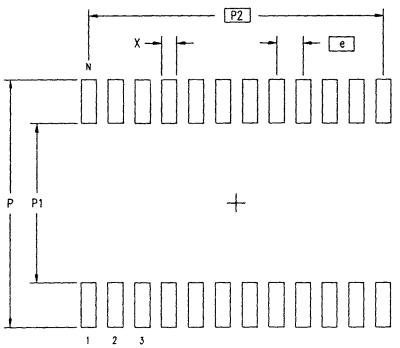
11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-013, VARIATION AA, AB, AC, AD & AE

TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS	DATE	TITLE	PS PACKAGE OUTLINE .300" BODY WIDTH SOIC .050" PITCH
DRAWN dd	03/15/89		
CHECKED		SIZE C	DRAWING No. PSC-4007 REV 06
		DO NOT SCALE DRAWING	SHEET 2 OF 3

SOIC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27643	06	REDRAW TO JEDEC FORMAT	03/15/95	

LAND PATTERN DIMENSIONS

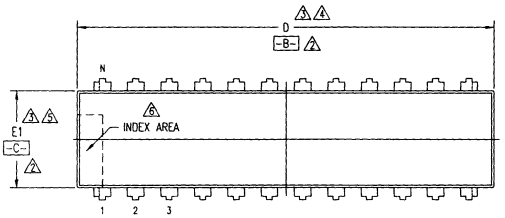


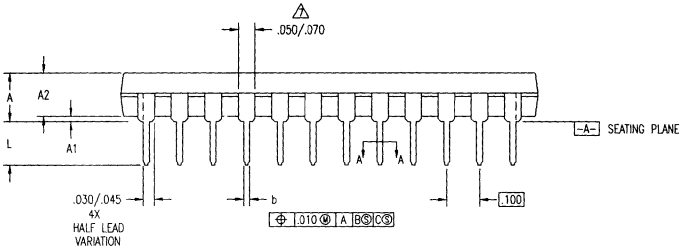
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.456	.464	.456	.464	.456	.464	.456	.464	.456	.464
P1	.292	.300	.292	.300	.292	.300	.292	.300	.292	.300
P2	.350 BSC		.400 BSC		.450 BSC		.550 BSC		.650 BSC	
X	.024	.032	.024	.032	.024	.032	.024	.032	.024	.032
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
N	16		18		20		24		28	

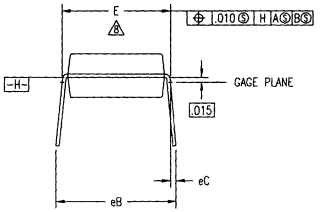
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL XX± XXX± XXXX±	ANGULAR ±		
APPROVALS	DATE	TITLE PS PACKAGE OUTLINE .300" BODY WIDTH SOIC .050" PITCH	
DRAWN AA	03/15/89		
CHECKED		SIZE C	DRAWING No. PSC-4007 REV 06
		DO NOT SCALE DRAWING	SHEET 3 OF 3

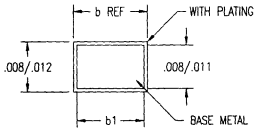
PLASTIC DIP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27653	06	REDRAW TO JEDEC FORMAT	03/15/95	









SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL ANGULAR XX± ± XXX± XXXX±			
APPROVALS	DATE	TITLE PD 16,18,20,22 & PT 24 PKG OUTLINE .300" BODY WIDTH PDIP .100" PITCH	
DRAWN dd	10/15/88		
CHECKED			
		SIZE C	DRAWING No. PSC-4000 REV 06
		DO NOT SCALE DRAWING	SHEET 1 OF 2

PLASTIC DIP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27653	06	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	P16-1				DWG #	P18-1			DWG #	P20-1			DWG #	P22-1			DWG #	P24-1		
SYMBOL	JEDEC VARIATION BB (HALF LEAD)			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION BD (HALF LEAD)			NOTE	JEDEC VARIATION AF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.140	-	.165		.140	-	.165		.145	-	.165		.145	-	.165		.145	-	.165	
A1	.015	-	.035		.015	-	.035		.015	-	.035		.015	-	.035		.015	-	.035	
A2	.115	.130	.150		.115	.130	.150		.115	.130	.150		.115	.130	.150		.115	.130	.150	
D	.745	.755	.760	3,4	.885	.900	.910	3,4	1.020	1.030	1.040	3,4	1.050	1.055	1.060	3,4	1.240	1.250	1.255	3,4
E	.300	.310	.325	8	.300	.310	.325	8	.300	.310	.325	8	.300	.310	.320	8	.300	.310	.320	8
E1	.247	.254	.260	3,5	.247	.254	.260	3,5	.240	.260	.280	3,5	.240	.255	.270	3,5	.250	.260	.275	3,5
b	.015	-	.022		.015	-	.020		.015	-	.020		.015	-	.022		.015	-	.020	
b1	.015	-	.020		.015	-	.018		.015	-	.018		.015	-	.020		.015	-	.018	
eB	.310	-	.370		.310	-	.370		.310	-	.370		.310	-	.370		.310	-	.370	
eC	.000	-	.040		.000	-	.040		.000	-	.040		.000	-	.040		.000	-	.040	
L	.120	.135	.150		.120	.135	.150		.120	.135	.150		.120	.135	.150		.120	.135	.150	
N	16				18				20				22				24			

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .010 PER SIDE
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEEED .010 PER SIDE
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .010 MAXIMUM TOTAL PER LEAD
8. DIMENSION E IS MEASURED ON THE OUTSIDE SURFACE OF THE LEADS AT THE GAGE OF .015 BELOW DATUM PLANE -H-
9. ALL DIMENSIONS ARE IN INCHES
10. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-001, VARIATION BB (HALF LEAD), AC, AD, BD (HALF LEAD) & AF

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS | DATE
DRAWN AA | 10/15/88
CHECKED

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

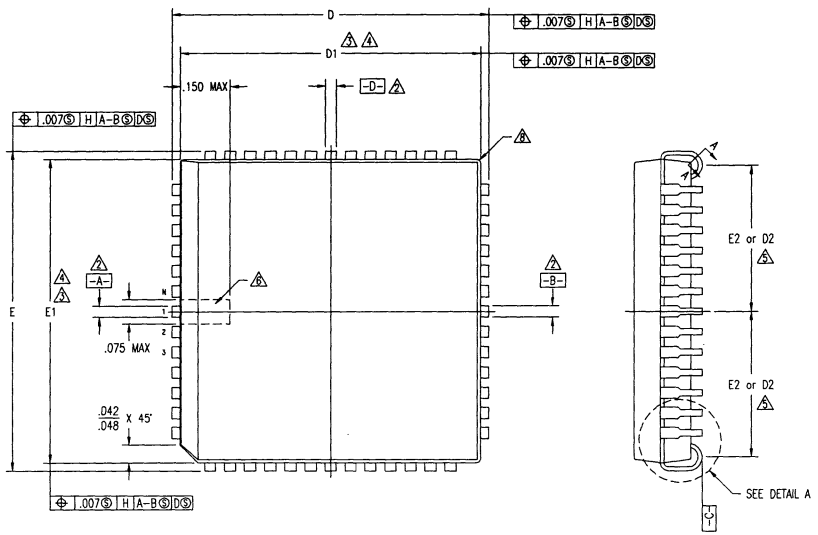
TITLE PD 16,18,20,22 & PT 24 PKG OUTLINE
.300" BODY WIDTH PDIP
.100" PITCH

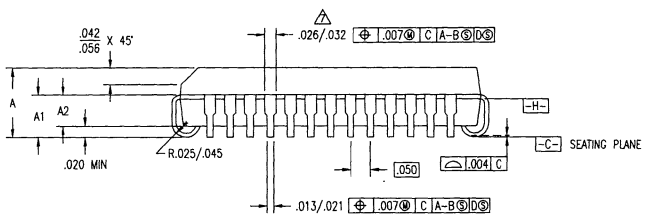
SIZE C | DRAWING No. PSC-4000 | REV 06

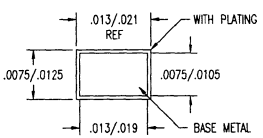
DO NOT SCALE DRAWING | SHEET 2 OF 2

PLCC

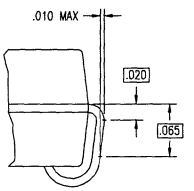
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

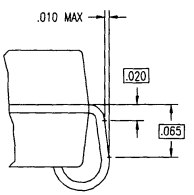






SECTION A-A





DETAIL A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL ANGULAR XX± ± XXX± XXXX±			
APPROVALS	DATE	TITLE	PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN dd	08/15/89		
CHECKED		SIZE C	DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING	SHEET 1 OF 3

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	J28-1				DWG #	J44-1				DWG #	J52-1				DWG #	J68-1				DWG #	J84-1			
SYMBOL	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE	JEDEC VARIATION AF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.165	.172	.180		.165	.172	.180		.165	.172	.180		.165	.172	.180		.165	.172	.180	
A1	.095	.105	.115		.095	.105	.115		.095	.105	.115		.095	.105	.115		.095	.105	.115	
A2	.062	–	.083		.062	–	.083		.062	–	.083		.062	–	.083		.059	–	.080	
D	.485	.490	.495		.685	.690	.695		.785	.790	.795		.985	.990	.995		1.185	1.190	1.195	
D1	.450	.453	.456	3,4	.650	.653	.656	3,4	.750	.753	.756	3,4	.950	.953	.956	3,4	1.150	1.154	1.156	3,4
D2	.195	.205	.215	5	.295	.305	.315	5	.345	.355	.365	5	.445	.455	.465	5	.545	.555	.565	5
E	.485	.490	.495		.685	.690	.695		.785	.790	.795		.985	.990	.995		1.185	1.190	1.195	
E1	.450	.453	.456	3,4	.650	.653	.656	3,4	.750	.753	.756	3,4	.950	.953	.956	3,4	1.150	1.154	1.156	3,4
E2	.191	.205	.219	5	.291	.305	.319	5	.341	.355	.369	5	.441	.455	.469	5	.541	.555	.569	5
N	28				44				52				68				84			

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. DATUMS [A–B] AND [–D–] TO BE DETERMINED AT DATUM PLANE [–H–]
3. DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [–H–]
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
5. DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [–C–] CONTACT POINT
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS–018, VARIATION AB, AC, AD, AE & AF. EXCEPTIONS: JEDEC MAXIMUM BASE METAL LEAD WIDTH IS .018

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN dd	08/15/89
CHECKED	

TITLE: PL PACKAGE OUTLINE
SQUARE PLCC
.050 PITCH

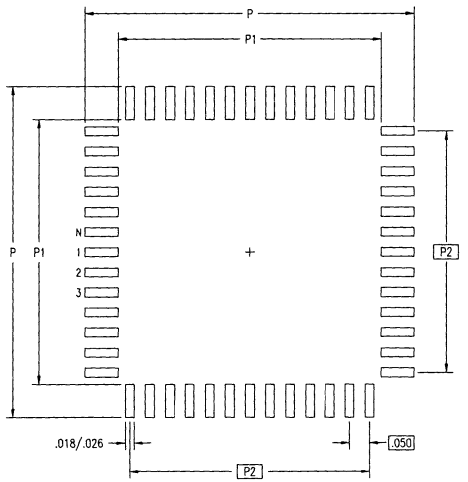
SIZE	DRAWING No.	REV
C	PSC–4008	06

DO NOT SCALE DRAWING — SHEET 2 OF 3

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.520	.528	.720	.728	.820	.828	1.020	1.028	1.220	1.228
P1	.354	.362	.554	.562	.654	.662	.854	.862	1.054	1.062
P2	.300 BSC		.500 BSC		.600 BSC		.800 BSC		1.000 BSC	
N	28		44		52		68		84	

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		

APPROVALS	DATE
DRAWN dd	08/15/89
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

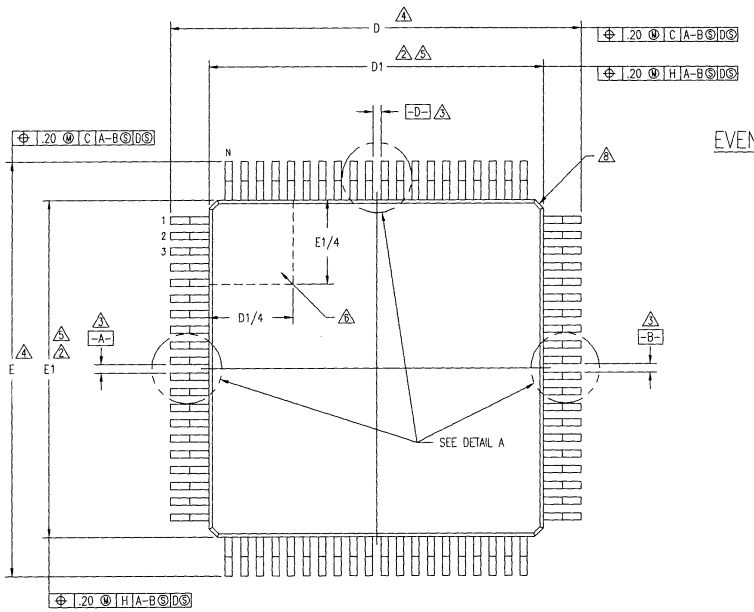
TITLE PL PACKAGE OUTLINE
SQUARE PLCC
.050 PITCH

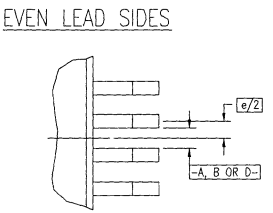
SIZE	DRAWING No.	REV
C	PSC-4008	06

DO NOT SCALE DRAWING — SHEET 3 OF 3

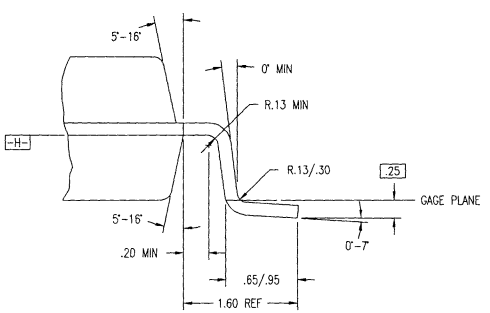
PQFP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27649	04	REDRAW TO JEDEC FORMAT	01/24/92	

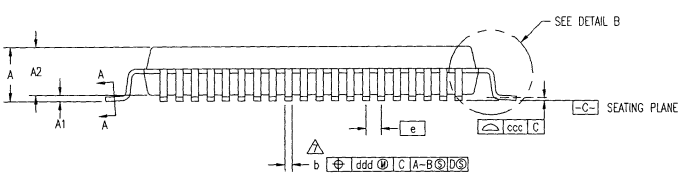


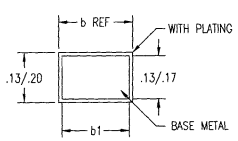


DETAIL A



DETAIL B





SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
DECIMAL ANGULAR XX± ± XXX± XXXX±			
APPROVALS	DATE	TITLE	PM PACKAGE OUTLINE 14.0 X 14.0 X 2.0 mm PQFP 1.60/.25 MAX FORM
DRAWN AA	01/15/92		
CHECKED		SIZE C	DRAWING No. PSC-4035 REV 04
		DO NOT SCALE DRAWING	SHEET 1 OF 2

PQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27649	04	REDRAW TO JEDEC FORMAT	01/24/92	

DWG #	PQ80-1			
SYMBOL	JEDEC VARIATION BE-2			NOTE
	MIN	NOM	MAX	
A	–	–	2.35	
A1	–	–	.25	
A2	1.95	2.00	2.10	
D	16.95	17.20	17.45	4
D1	13.90	14.00	14.10	5,2
E	16.95	17.20	17.45	4
E1	13.90	14.00	14.10	5,2
N	80			
e	.65 BSC			
b	.22	–	.35	7
b1	.22	.30	.32	
ccc	–	–	.10	
ddd	–	–	.13	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

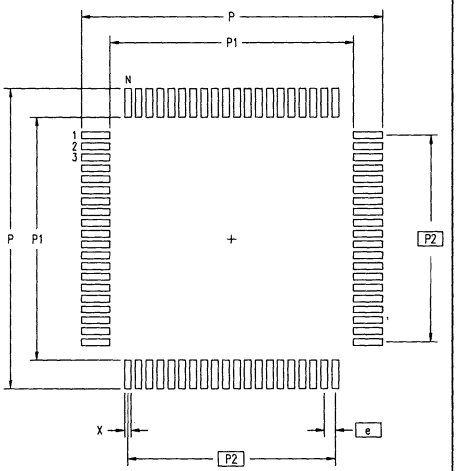
8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-108, VARIATION BE-2

LAND PATTERN DIMENSIONS



	MIN	MAX
P	17.80	18.00
P1	14.40	14.60
P2	12.35 BSC	
X	.30	.50
e	.65 BSC	
N	80	

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS	DATE
DRAWN dd	01/15/92
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

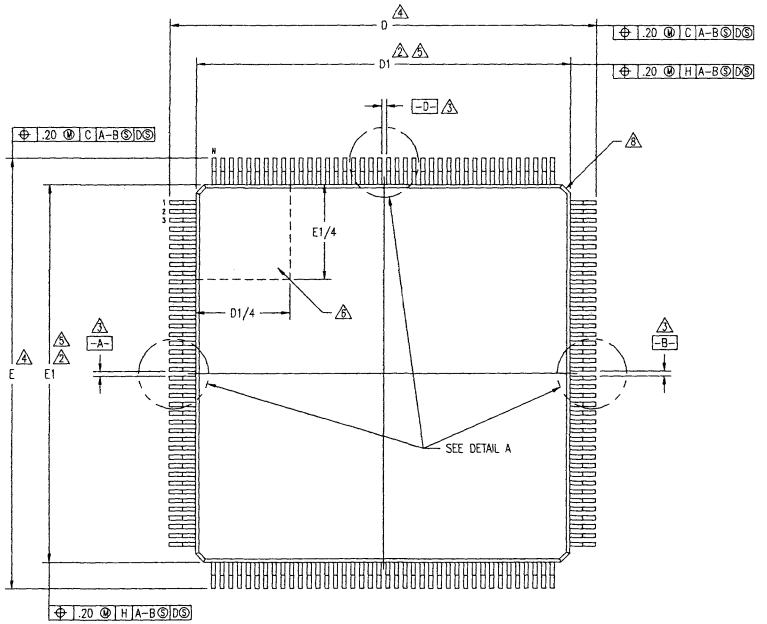
TITLE PM PACKAGE OUTLINE
14.0 X 14.0 X 2.0 mm PQFP
1.60/.25 MAX FORM

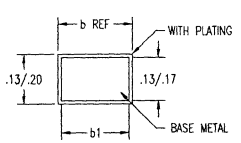
SIZE	DRAWING No.	REV
C	PSC-4035	04

DO NOT SCALE DRAWING SHEET 2 OF 2

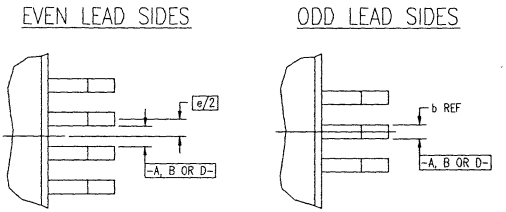
PQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27657	00	MOVE FROM PSC-4035 REDRAW TO JEDEC FORMAT	03/15/95	

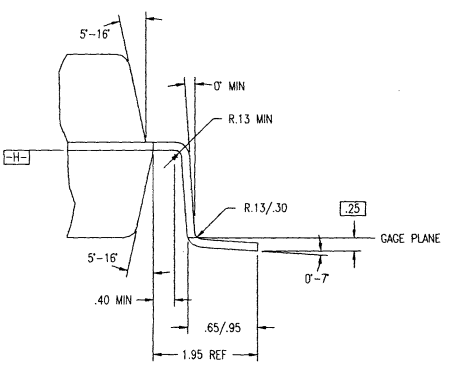




SECTION A-A



DETAIL A



DETAIL B

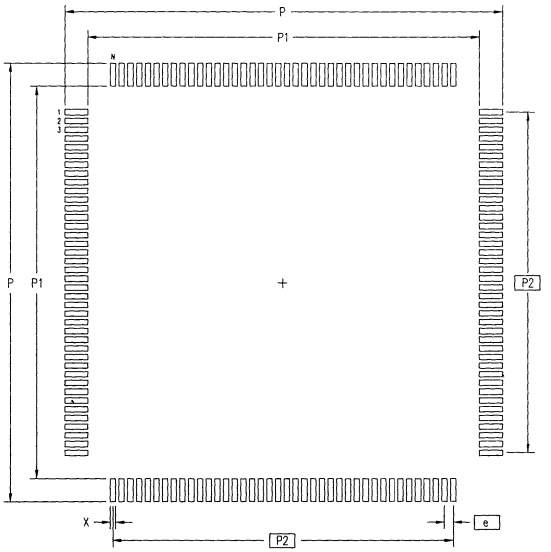
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
DECIMAL XX± XXX± XXXX±	ANGULAR ±			
APPROVALS	DATE	TITLE	PM PACKAGE OUTLINE 28.0 X 28.0 X 3.4 mm PQFP 1.95/.25 MIN FORM	
DRAWN JU	03/15/94			
CHECKED		SIZE	DRAWING No.	REV
		C	PSC-4049	00
		DO NOT SCALE DRAWING		SHEET 1 OF 2

PQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27657	00	MOVE FROM PSC-4035 REDRAW TO JEDEC FORMAT	03/15/95	

	DWG #		PQ144-2		DWG #		PQ160-2		DWG #		PQ208-2	
SYMBOL	JEDEC VARIATION DC-1			NOTE	JEDEC VARIATION DD-1			NOTE	JEDEC VARIATION –			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	3.45	–	4.07		3.45	–	4.07		3.45	–	4.07	
A1	.25	–	–		.25	–	–		.25	–	–	
A2	3.18	3.42	3.65		3.18	3.42	3.65		3.18	3.42	3.65	
D	31.80	31.90	32.00	4	31.80	31.90	32.00	4	31.80	31.90	32.00	4
D1	27.90	28.00	28.10	5,2	27.90	28.00	28.10	5,2	27.90	28.00	28.10	5,2
E	31.80	31.90	32.00	4	31.80	31.90	32.00	4	31.80	31.90	32.00	4
E1	27.90	28.00	28.10	5,2	27.90	28.00	28.10	5,2	27.90	28.00	28.10	5,2
N	144				160				208			
e	.65 BSC				.65 BSC				.50 BSC			
b	.22	–	.35	7	.22	–	.35	7	.17	–	.27	7
b1	.22	.30	.32		.22	.30	.32		.17	.20	.23	
aaa	–	–	.12		–	–	.12		–	–	.08	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX
P	32.50	32.70	32.50	32.70	32.50	32.70
P1	28.40	28.60	28.40	28.60	28.40	28.60
P2	22.75 BSC		25.35 BSC		25.50 BSC	
X	.30	.50	.30	.50	.30	.40
e	.65 BSC		.65 BSC		.50 BSC	
N	144		160		208	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE [-C-]

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

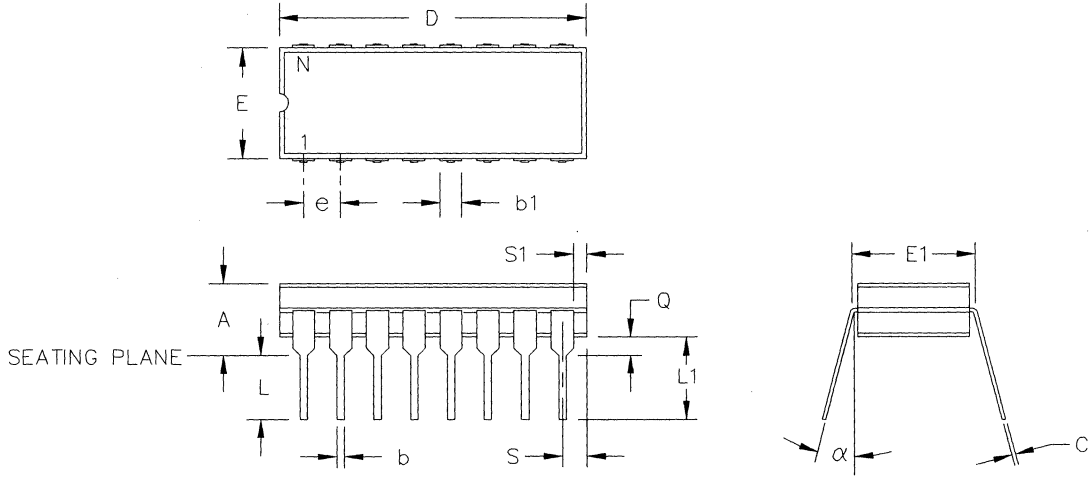
9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THE 144 & 160 LD OUTLINES CONFORM TO JEDEC PUBLICATION 95 REGISTRATION MO-112, VARIATION DC-1 & DD-1 RESPECTIVELY

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS / DRAWN JTV 03/15/94 / CHECKED	TITLE PM PACKAGE OUTLINE 28.0 X 28.0 X 3.4 mm PQFP 1.95/.25 MIN FORM	
	SIZE C / DRAWING No. PSC-4049	REV 00
	DO NOT SCALE DRAWING	SHEET 2 OF 2

DUAL IN-LINE PACKAGES

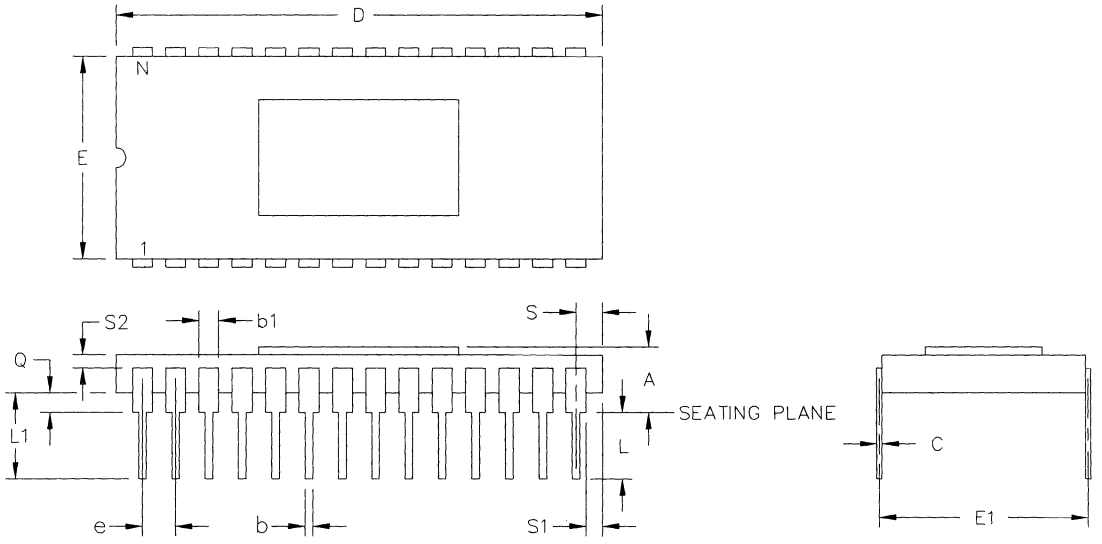


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16-40 LEAD CERDIP

DWG #	D16-1		D20-1		D24-1		D40-1	
# OF LDS (N)	16		20		24		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.200	.140	.200	.140	.200	.160	.220
b	.015	.021	.015	.021	.015	.021	.014	.023
b1	.045	.060	.045	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.014	.008	.014
D	.750	.830	.935	1.060	1.240	1.280	2.020	2.070
E	.285	.310	.285	.310	.285	.310	.510	.600
E1	.290	.320	.290	.320	.300	.320	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.200
L1	.150	–	.150	–	.150	–	.150	–
Q	.015	.055	.015	.060	.015	.060	.020	.060
S	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)



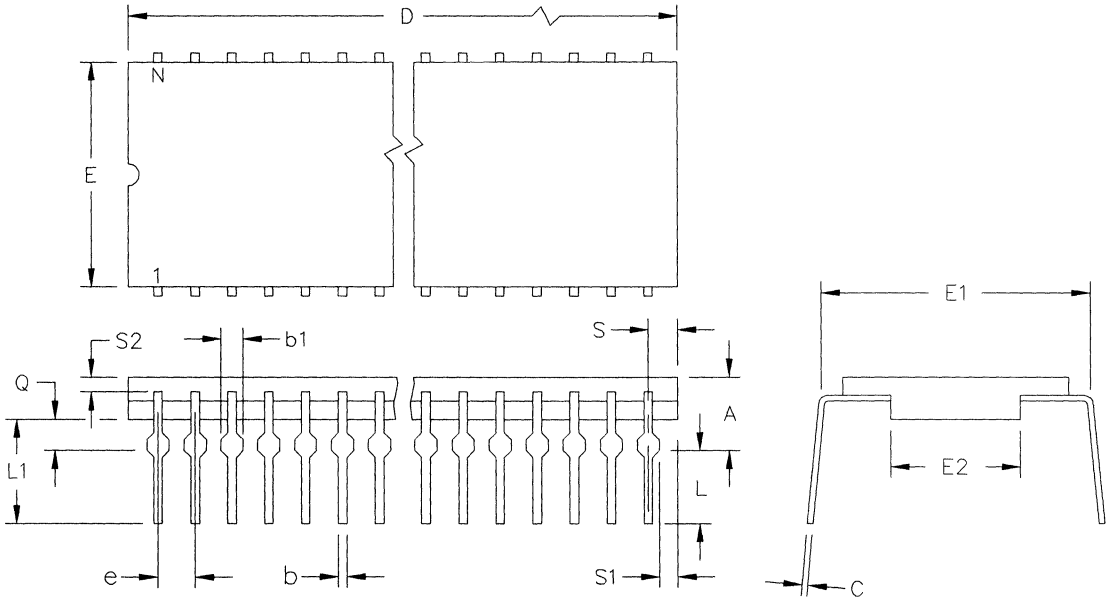
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

48 LEAD SIDE BRAZE (600 MIL)

DWG #	C48-2	
# OF LDS (N)	48	
SYMBOL	MIN	MAX
A	.100	.190
b	.015	.023
b1	.045	.060
C	.008	.012
D	2.370	2.430
E	.550	.610
E1	.595	.620
e	.100 BSC	
L	.125	.175
L1	.150	–
Q	.020	.060
S	.030	.065
S1	.005	–
S2	.005	–

DUAL IN-LINE PACKAGES (Continued)

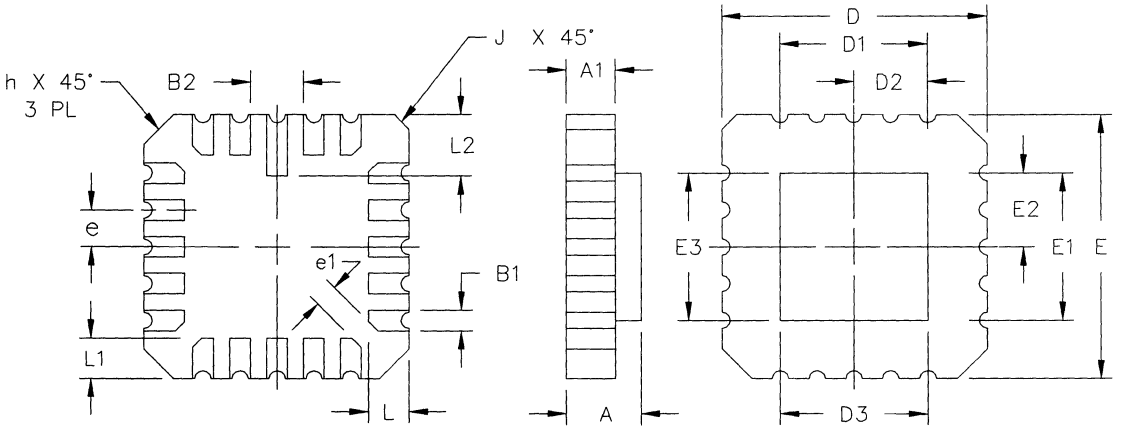
64 LEAD TOP BRAZE (900 MIL)

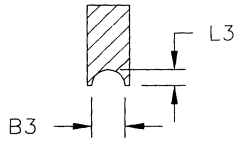


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	C64-2	
# OF LDS (N)	64	
SYMBOL	MIN	MAX
A	.120	.180
b	.015	.021
b1	.045	.060
C	.009	.012
D	3.170	3.240
E	.790	.810
E1	.880	.915
E2	.640	.660
e	.100 BSC	
L	.125	.160
L1	.150	–
Q	.020	.100
S	.030	.065
S1	.005	–
S2	.005	–

LEADLESS CHIP CARRIERS



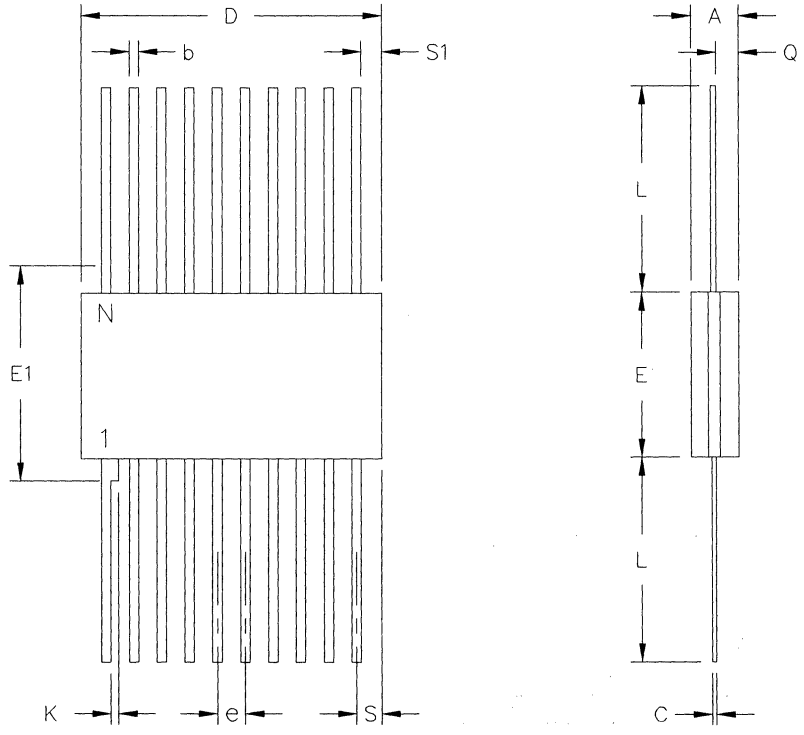


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–44 LEAD LCC (SQUARE)

DWG #	L20–2		L28–1		L44–1	
# OF LDS (N)	20		28		44	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120
A1	.054	.066	.050	.088	.054	.088
B1	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660
D1/E1	.200 BSC		.300 BSC		.500 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC	
D3/E3	–	.358	–	.460	–	.560
e	.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055
L1	.045	.055	.045	.055	.045	.055
L2	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11	

CERPACKS

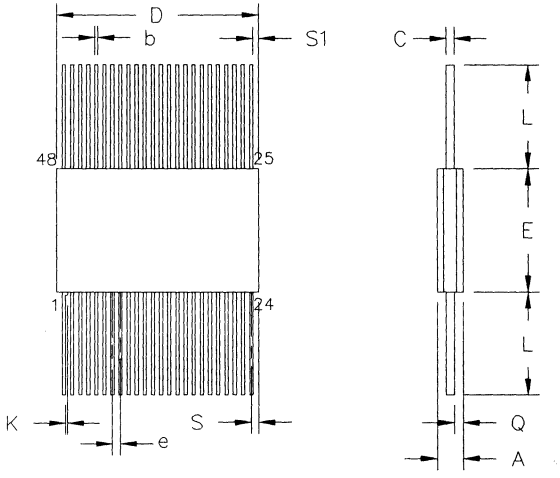


NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

16–24 LEAD CERPACK

DWG #	E16–1		E20–1		E24–1	
# OF LDS (N)	16		20		24	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090
b	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006
D	.370	.430	–	.540	–	.640
E	.245	.285	.245	.300	.300	.420
E1	–	.305	–	.305	–	.440
e	.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040
S	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–

CERPACKS (Continued)

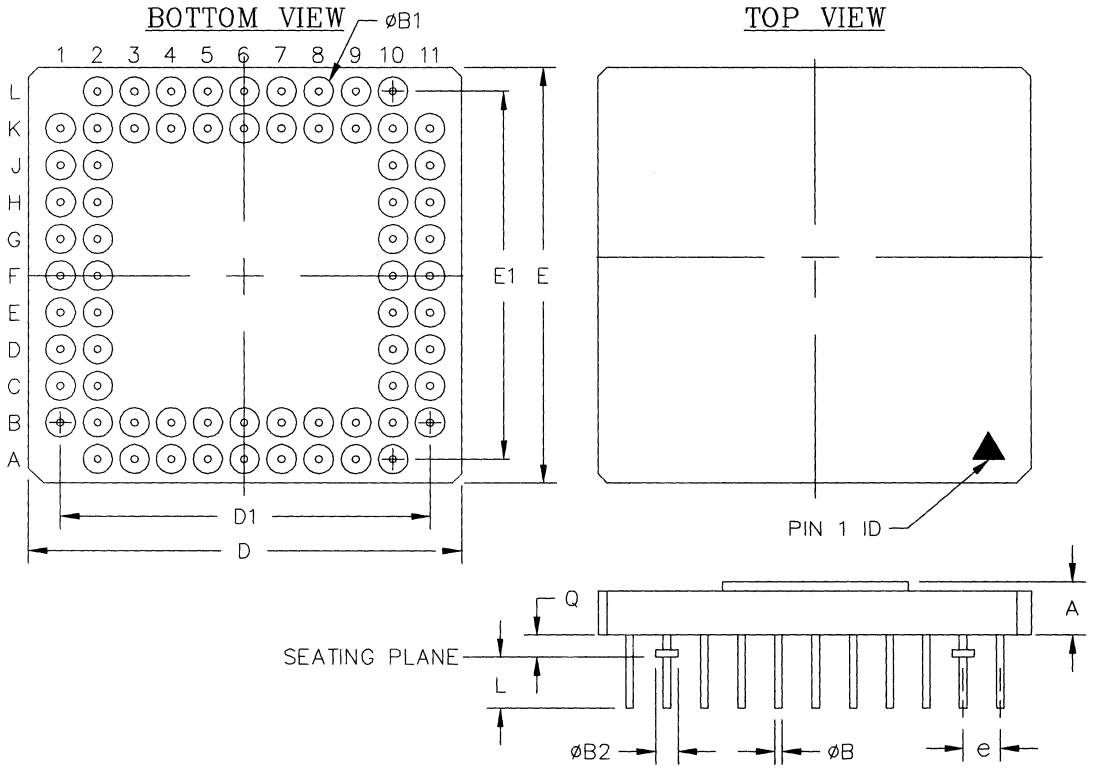


NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.
4. THIS DWG REPRESENTS A 48 LEAD CERPACK.

48–56 LEAD CERPACK (.025" LEAD PITCH)

DWG #	E48–1		E56–1	
# OF LDS (N)	48		56	
SYMBOL	MIN	MAX	MIN	MAX
A	.075	.095	.075	.095
b	.008	.013	.008	.013
C	.0045	.006	.0045	.006
D	.610	.640	.710	.740
E	.370	.390	.370	.390
e	.025 BSC		.025 BSC	
K	.003	.007	.003	.007
L	.250	.370	.250	.370
Q	.025	.045	.025	.045
S	–	.035	–	.035
S1	.005	–	.005	–

PIN GRID ARRAYS

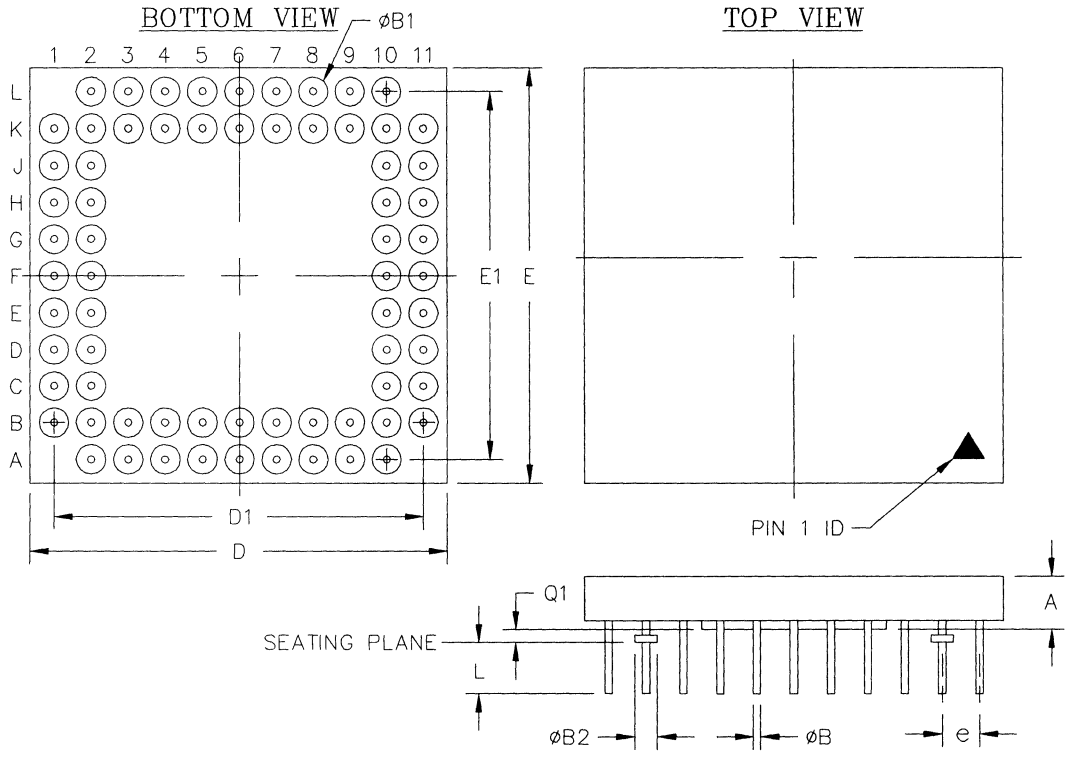


68 PIN PGA (CAVITY UP)

DWG #	G68-1	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.140	1.180
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)



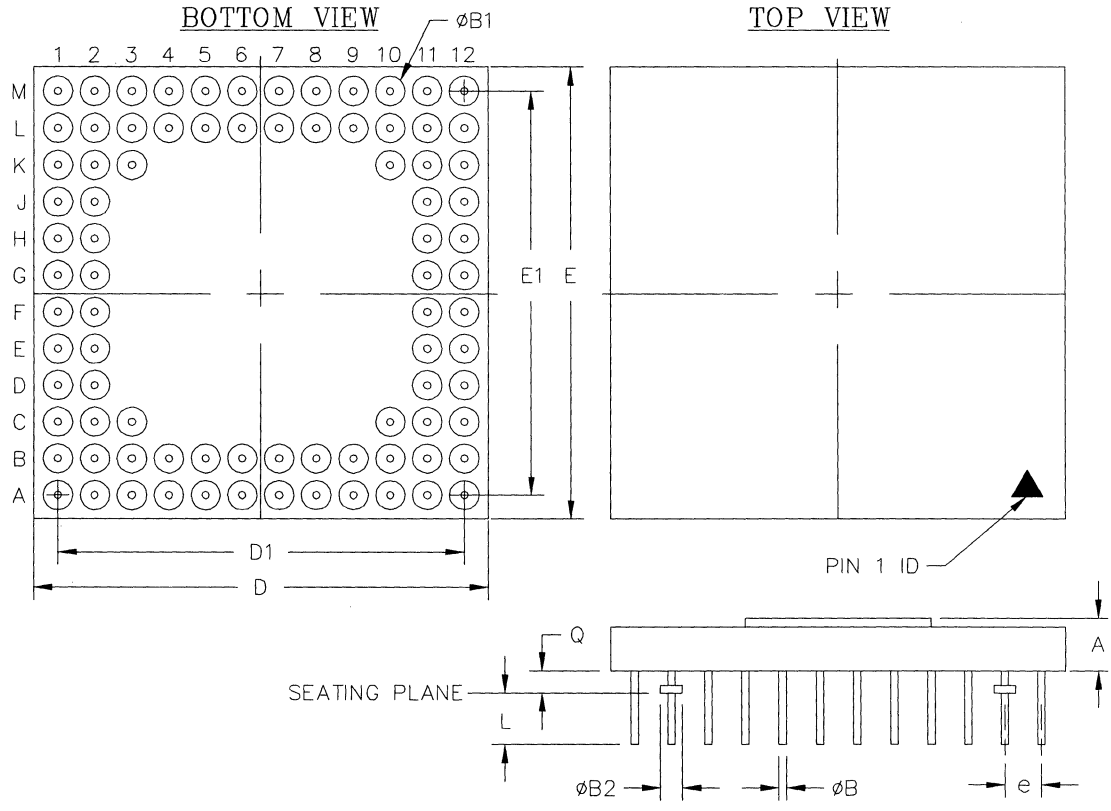
68 PIN PGA (CAVITY DOWN)

DWG #	G68-2	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.077	.095
ØB	.016	.020
ØB1	.060	.080
ØB2	.040	.060
D/E	1.098	1.122
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q1	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

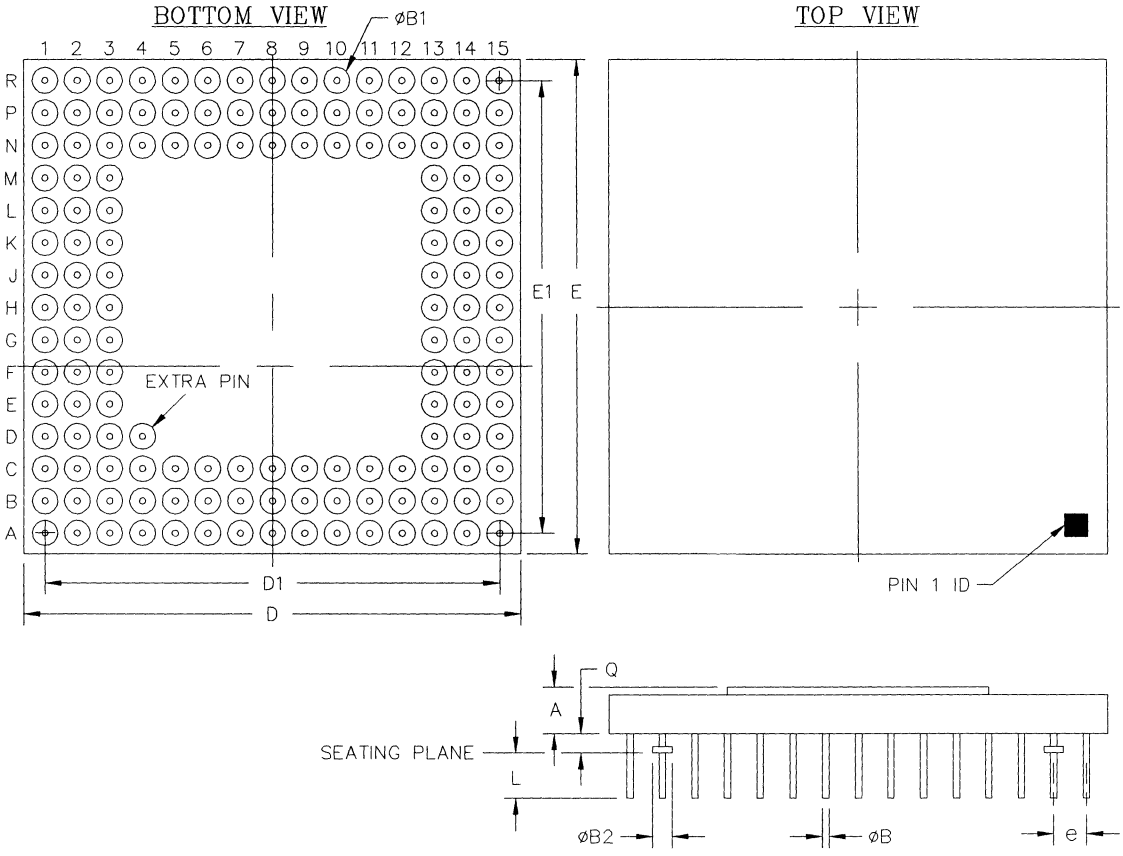
84 PIN PGA (CAVITY UP – 12 X 12 GRID)



DWG #	G84-1	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.077	.145
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.180	1.235
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.025	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)



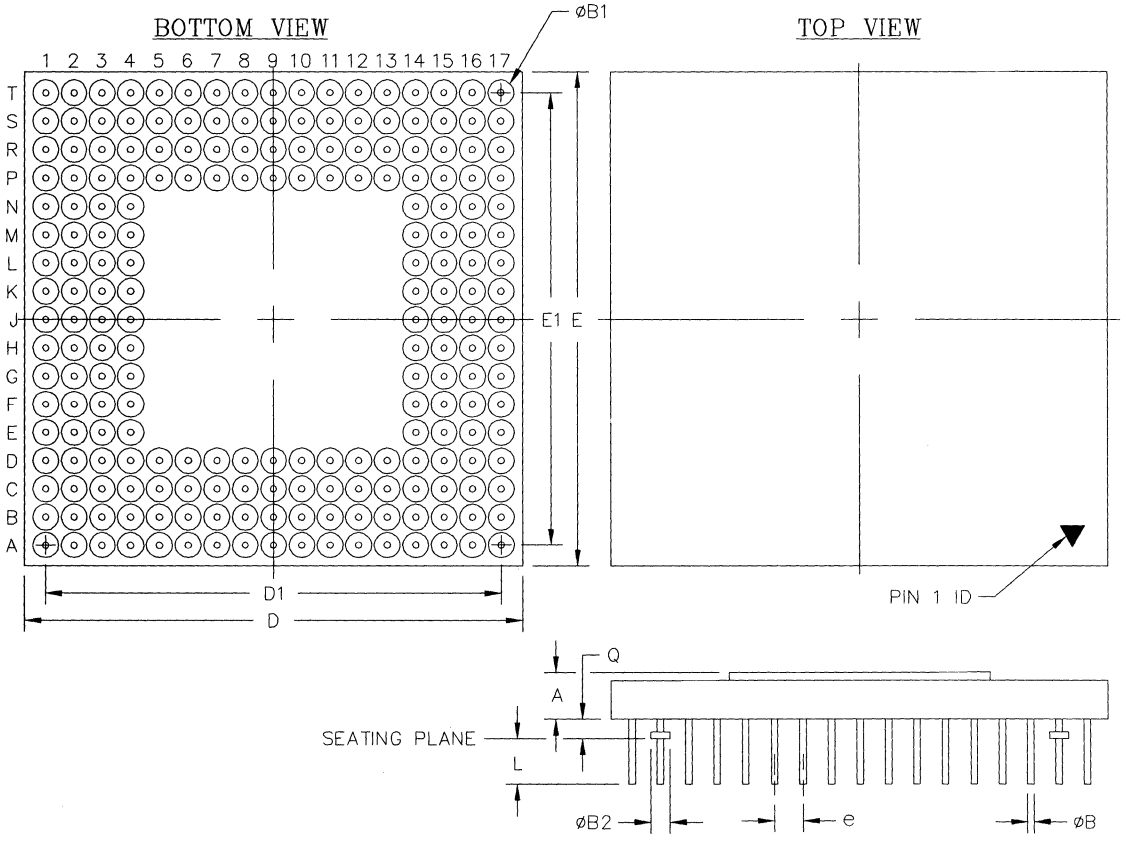
144 PIN PGA (CAVITY UP)

DWG #	G144-2	
# OF PINS (N)	145	
SYMBOL	MIN	MAX
A	.082	.125
øB	.016	.020
øB1	.060	.080
øB2	.040	.060
D/E	1.559	1.590
D1/E1	1.400 BSC	
e	.100 BSC	
L	.120	.140
M	15	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.
6. EXTRA PIN (D-4) ELECTRICALLY CONNECTED TO D-3.

PIN GRID ARRAYS (Continued)

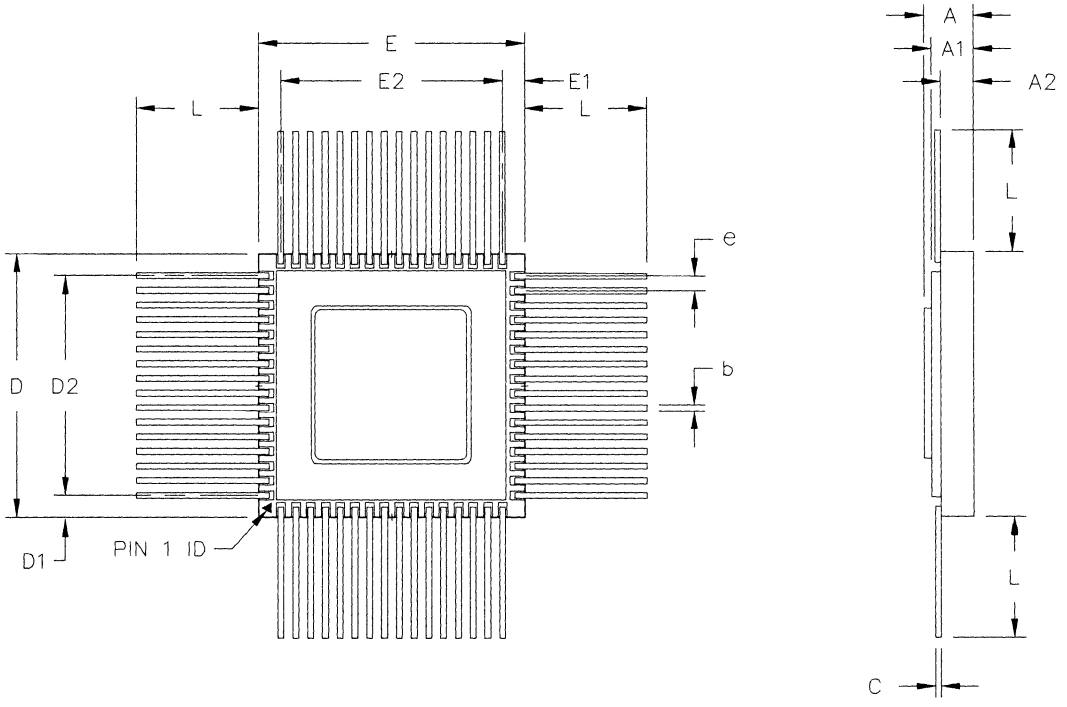
208 PIN PGA (CAVITY UP)



DWG #	G208-1	
# OF PINS (N)	208	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.732	1.780
D1/E1	1.600 BSC	
e	.100 BSC	
L	.120	.140
M	17	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

FLATPACKS



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

48–64 LEAD QUAD FLATPACK

DWG #	F48–1		F64–1	
# OF LDS (N)	48		64	
SYMBOL	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.054	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D/E	–	.750	.885	.915
D1/E1	.100 REF		.075 REF	
D2/E2	.550 BSC		.750 BSC	
e	.050 BSC		.050 BSC	
L	.350	.450	.350	.450
ND/NE	12		16	

FCT-T DOUBLE-DENSITY LOGIC

IDT's FCT-T Double-Density Logic family of 16-, 18-, and 20-bit components has been designed for use in standard TTL-Logic applications. Double-Density features the highest speed Logic available and the lowest power dissipation in the industry.

IDT offers several output configurations including Balanced Drive, Light Drive, High Drive and 3.3 Volt. All Double-Density Logic is guaranteed to have less than 500ps pin-to-pin skew, making the output timing highly predictable in high-speed busses. These components come in several speed grades from standard speed up to "E" speed, with 3.2ns propagation delay providing an easy system performance upgrade path. The components are available in space-saving SSOP and TSSOP packages which have a high ratio of ground pins to outputs, reducing ground bounce and output noise levels.

All IDT FCT-T Logic components have input hysteresis. In addition, several of the Double-Density components have input Bus Hold which retains the last known state on a 3-state bus.[1]

Balanced Drive

Balanced Drive Double-Density Logic (FCT162xxxT) is intended for general-purpose applications requiring high speed, low power and low noise. Balanced Drive has series output resistors which reduce the drive current of the devices to ±24mA minimum, at the guaranteed Logic thresholds of 400mV and 2.4V respectively, helping to reduce transmission line noise, ringing, ground bounce, crosstalk, EMI and other noise related problems. Balanced Drive also has a balanced line driving capability, and will drive ±115mA (typical) at the 1.5V level, giving equal line driving currents for both the Logic HIGH transition and Logic LOW transition. Balanced drive is the fastest TTL Logic available for loads less than 200pF.

Light Drive

Light Drive (FCT166xxxT) is intended for point-to-point line driving applications where there is limited output loading. Light Drive has series terminating resistors which will limit the current level of the device to ±8mA minimum. Light Drive has balanced line driving capability and will drive ±48mA (typical) at the 1.5V level, easing line termination problems. The series termination resistors in Light Drive approximate adding a 25 ohm series resistor to an industry standard 64mA drive part, such as High Drive. Light Drive has advantages over a series resistor including very low ground bounce (typ 0.25V) and reduced part count. First incident wave switching should be achieved with Light Drive for loads of less than 50pF. Light Drive is recommended for applications which would otherwise require series termination resistors, applications which are noise sensitive, and applications where the output loading is not excessive. Light Drive is the quietest family available for loads of 100pF or less and is available in speed grades up to "C" speed.

High Drive

High Drive (FCT16xxxT) has +64/-32mA output drive capability, making it an excellent choice for use as a back plane driver. For loads in excess of 200pF, High Drive "E" speed is the fastest Logic available. For applications requiring hot insertion, High Drive supports Power Off Disable which will allow swapping of cards in powered systems. (See Application Note 102 for Power Off Disable design requirements). High Drive is compatible with industry standard high current BiCMOS and bipolar families.

3.3V

Double-Density (FCT163xxx) 3.3V Logic has superior performance characteristics and lower power dissipation than competing technologies. The data sheet specifications for 3.3V Double-Density components can be found in the 3.3V section of this data book.

Bus Hold

Bus-hold (FCT16xHxxxT) is available on several of the IDT Double-Density components. Bus-hold will retain the last known state on an input if the driving source goes to a high-impedance state. The hold current is approximately equivalent to adding a 3.3K pull-up or pull-down resistor to the input, but will hold the present state rather than always pull one direction. Bus-hold eliminates the need for pull up resistors on 3-state busses.

[1] Application Note 117, which can be found in the *IDT High-Speed CMOS Logic Design Guide,* contains additional device characteristics and applications information.

SECTION 5
DOUBLE-DENSITY 5V PRODUCTS
TABLE OF CONTENTS

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT16240T/AT/CT/ET
IDT54/74FCT162240T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16240T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162240T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

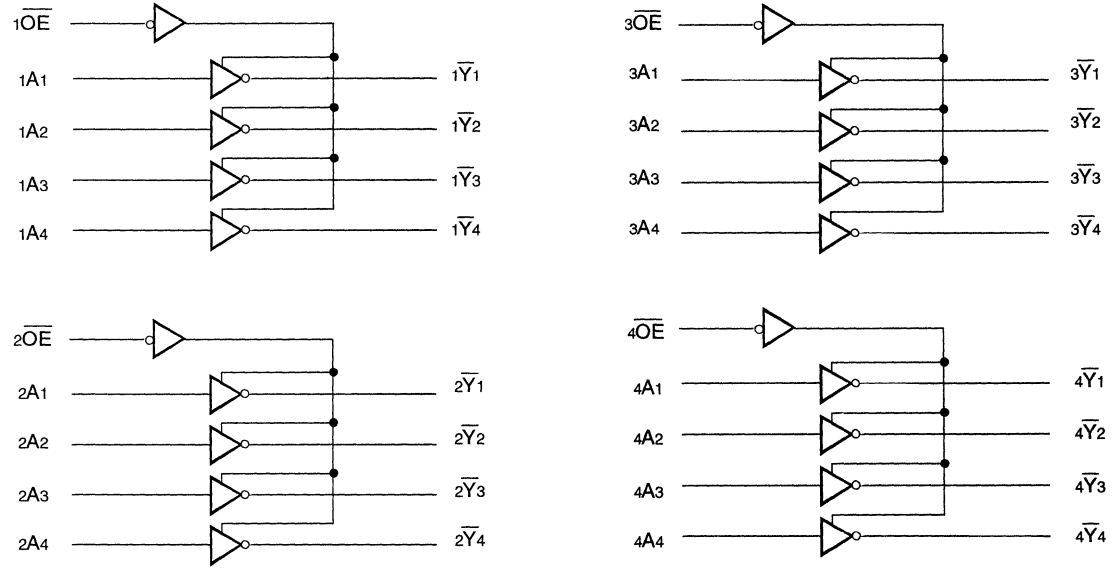
The FCT16240T/AT/CT/ET and FCT162240T/AT/CT/ET 16-bit buffer/line drivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices offer bus/backplane interface capability with improved packing density. The flow-through organization of signal pins simplifies layout. The three-state controls are designed to operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

The FCT16240T/AT/CT/ET are ideally suited for driving high capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162240T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times– reducing the need for external series terminating resistors. The FCT162240T/AT/CT/ET are plug-in replacements for FCT16240T/AT/CT/ET and 54/74ABT16240 for on-board interface applications.

5

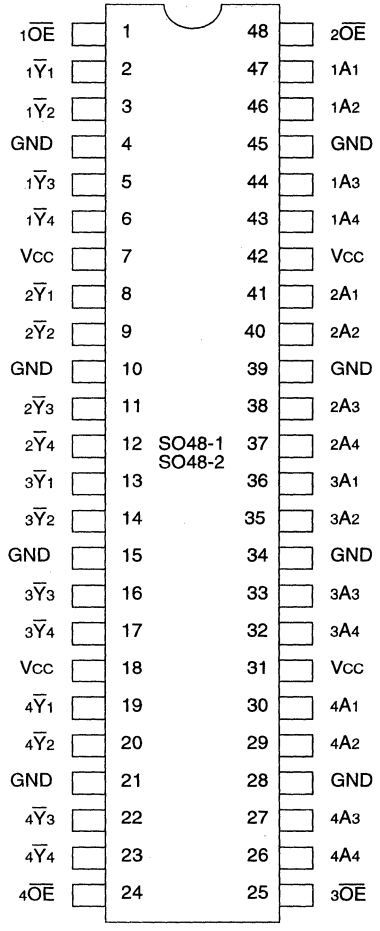
FUNCTIONAL BLOCK DIAGRAM



2541 drw 01

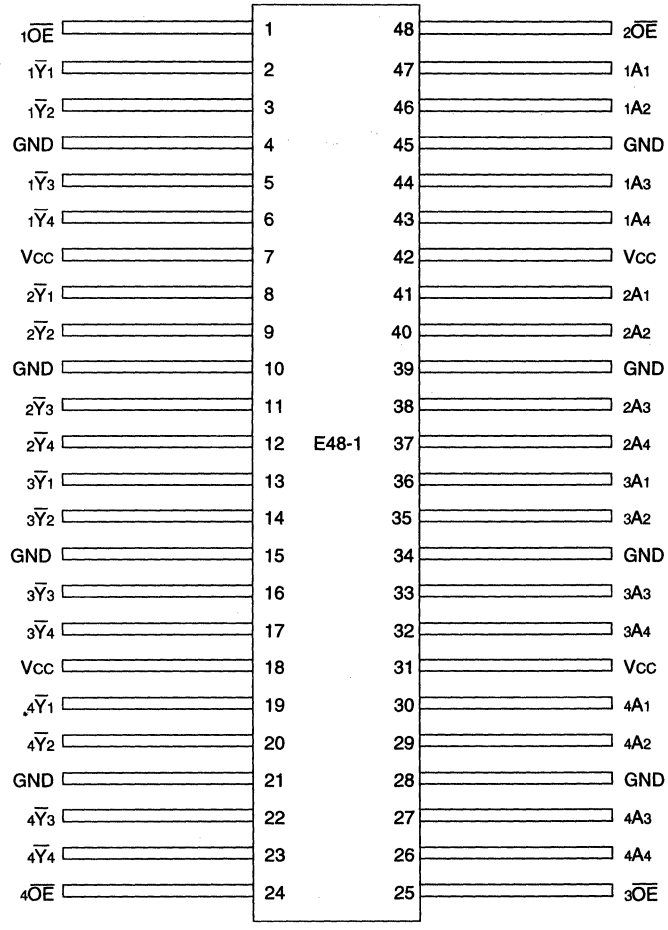
2541 drw 02

PIN CONFIGURATIONS



2541 drw 03

SSOP
TSSOP
TOP VIEW



2541drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs
$x\overline{Y}x$	3-State Outputs

2541 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	$x\overline{Y}x$
L	L	H
L	H	L
H	X	Z

NOTE: 2541 tbl 02

1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2541 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2541 lnk 04

1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2541 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16240T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2541 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162240T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2541 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

2541 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16240T/162240T				FCT16240AT/162240AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to x$\overline{Y}$x	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

Symbol	Parameter	Condition[1]	FCT16240CT/162240CT				FCT16240ET/162240ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to x$\overline{Y}$x	C_L = 50pF R_L = 500Ω	1.5	4.3	1.5	4.7	1.5	3.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.2	1.5	5.7	1.5	3.6	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

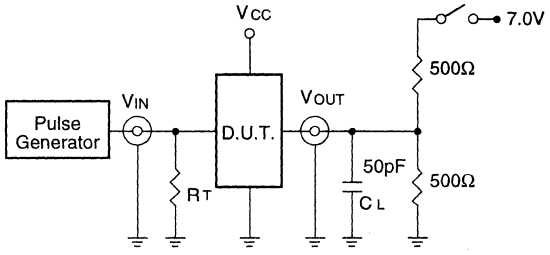
NOTES:

2541 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2541 drw 05

SWITCH POSITION

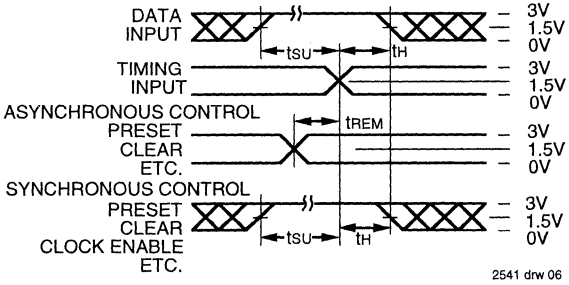
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2541 lnk 10

DEFINITIONS:

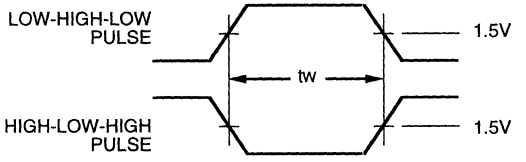
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



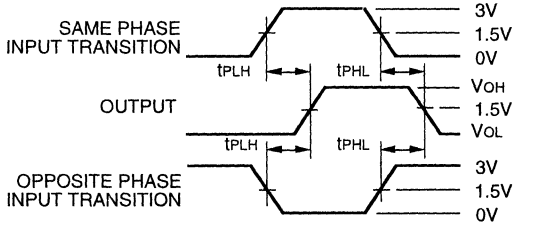
2541 drw 06

PULSE WIDTH



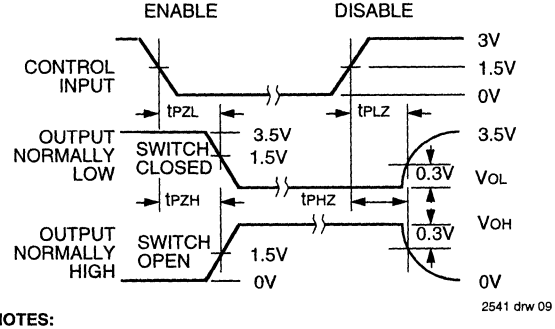
2541 drw 07

PROPAGATION DELAY



2541 drw 08

ENABLE AND DISABLE TIMES



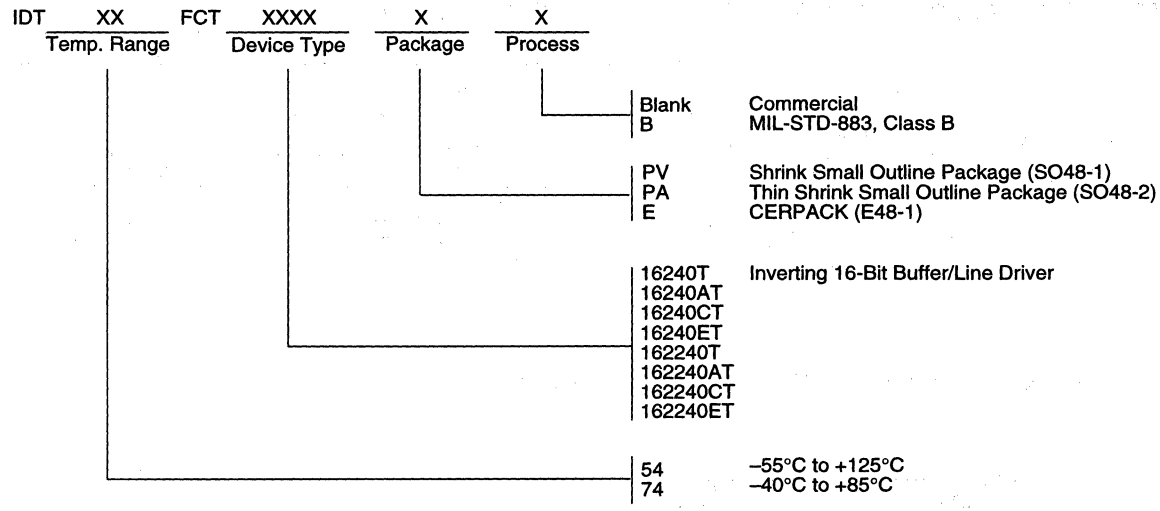
2541 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

5

ORDERING INFORMATION



2541 drw 10

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT16244T/AT/CT/ET
IDT54/74FCT162244T/AT/CT/ET
IDT54/74FCT166244T/AT/CT
IDT54/74FCT162H244T/AT/CT/ET
ADVANCE INFORMATION

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤ 1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
- **Features for FCT16244T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162244T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT166244T/AT/CT:**
  - Light Drive Balanced Output: ±8mA (commercial), ±6mA (military)
  - Minimal system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.25V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162H244T/AT/CT/ET:**
  - Bus Hold retains last active bus state during 3-state
  - Eliminates the need for external pull up resistors

DESCRIPTION:

The 16-Bit Buffer/Line Driver is for bus interface or signal buffering applications requiring high speed and low power dissipation. These devices have a flow through pin organization, and shrink packaging to simplify board layout. All inputs are designed with hysteresis for improved noise margin. The three-state controls allow independent 4-bit, 8-bit or combined 16-bit operation. These parts are plug in replacements for 54/74ABT16244 where higher speed, lower noise or lower power dissipation levels are desired.

The FCT16244T/AT/CT/ET are ideally suited for driving high capacitance loads (>200pF) and low impedance backplanes. These "high drive" buffers are designed with power off disable capability to allow "live insertion" of boards when used in a backplane interface.

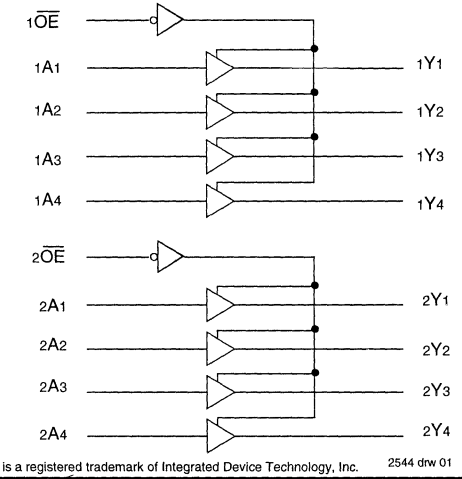
The FCT162244T/AT/CT/ET have balanced output current levels and current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times, reducing the need for external series terminating resistors while still providing very high speed operation for loads of less than 200pF.

The FCT166244T/AT/CT are suited for very low noise, point-to-point driving where there is a single receiver, or a very light lumped load (<50pF). The buffers are designed to limit the output current to levels which will avoid noise and ringing on the signal lines without using external series terminating resistors.

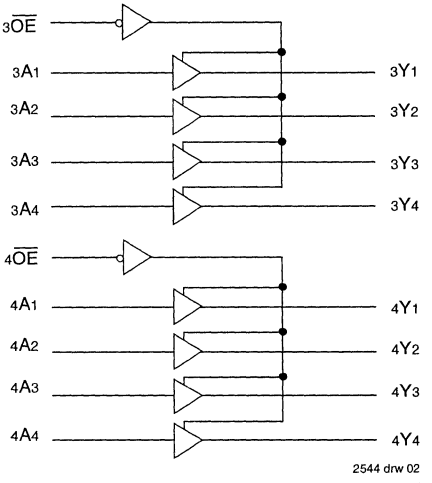
The FCT162H244T/AT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

5

FUNCTIONAL BLOCK DIAGRAM

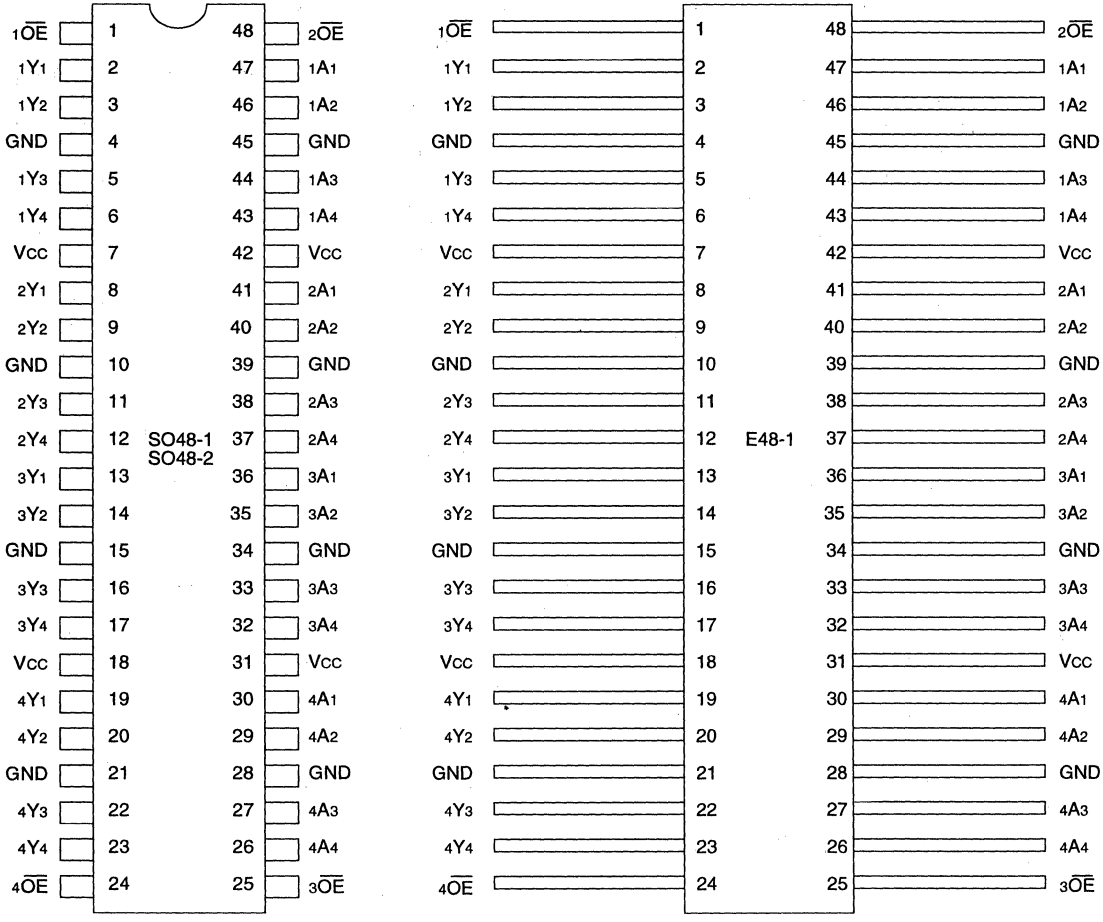


2544 drw 01



2544 drw 02

PIN CONFIGURATIONS



PIN DESCRIPTION

Pin Names	Description
x$\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs(1)
xYx	3-State Outputs

2544 tbl 01

NOTE:
1. On FCT16xH these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2544 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT and FCT166XXXT output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT and FCT166XXXT.

FUNCTION TABLE(1)

Inputs		Outputs
$x\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

2544 tbl 02

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2544 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

5

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)(5)			—	—	±1	
I_{IL}	Input LOW Current (Input pins)(5)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)(5)			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2544 lnk 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter		Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	Standard Input[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
		Standard I/O[5]			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I_{IL}	Input LOW Current[4]	Standard Input[5]		V_I = GND	—	—	±1	
		Standard I/O[5]			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I_{BHH}	Bus Hold Sustain Current[4]	Bus Hold Input	V_{CC} = Min.	V_I = 2.0V	–50	—	—	µA
I_{BHL}				V_I = 0.8V	+50	—	—	
I_{OZH}	High Impedance Output Current (3-State Output pins)[5,6]		V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}				V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage		V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current		V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis		—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current		V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2544 lnk 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.
6. Does not include Bus Hold I/O pins.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xDIR = $x\overline{OE}$= GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
		xDIR = $x\overline{OE}$ = GND One Bit Toggling fi = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
		xDIR = $x\overline{OE}$ = GND Sixteen Bits Toggling fi = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2540 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16646T/162646T				FCT16646AT/162646AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR or x$\overline{OE}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR or x$\overline{OE}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2540 tbl 09

Symbol	Parameter	Condition[1]	FCT16646CT/162646CT				FCT16646ET/162646ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	1.5	5.4	1.5	6.0	1.5	3.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR or x$\overline{OE}$ to Bus		1.5	7.8	1.5	8.9	1.5	4.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR or x$\overline{OE}$ to Bus		1.5	6.3	1.5	7.7	1.5	4.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	3.8	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to Bus		1.5	6.2	1.5	7.0	1.5	4.2	—	—	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0.0	—	—	—	ns
t_W	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

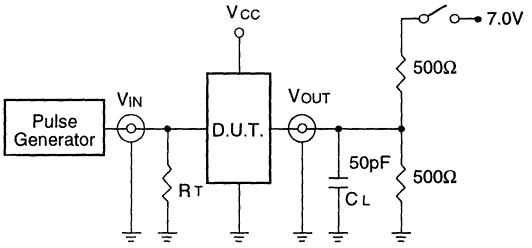
NOTES:

2540 tbl10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2556 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

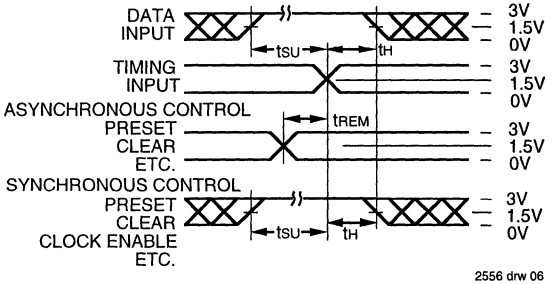
2556 lnk 10

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.

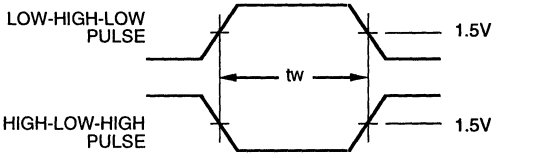
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



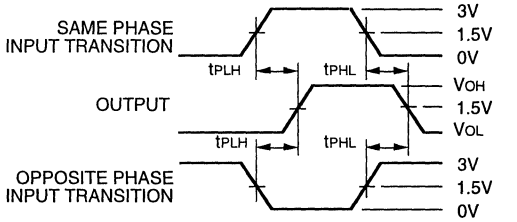
2556 drw 06

PULSE WIDTH



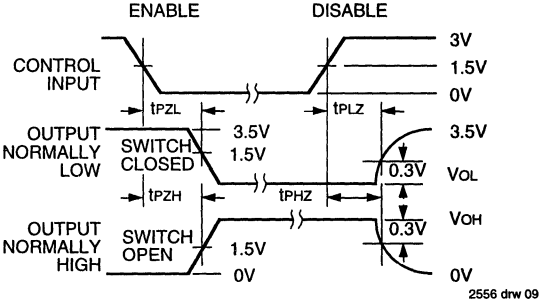
2556 drw 07

PROPAGATION DELAY



2556 drw 08

ENABLE AND DISABLE TIMES

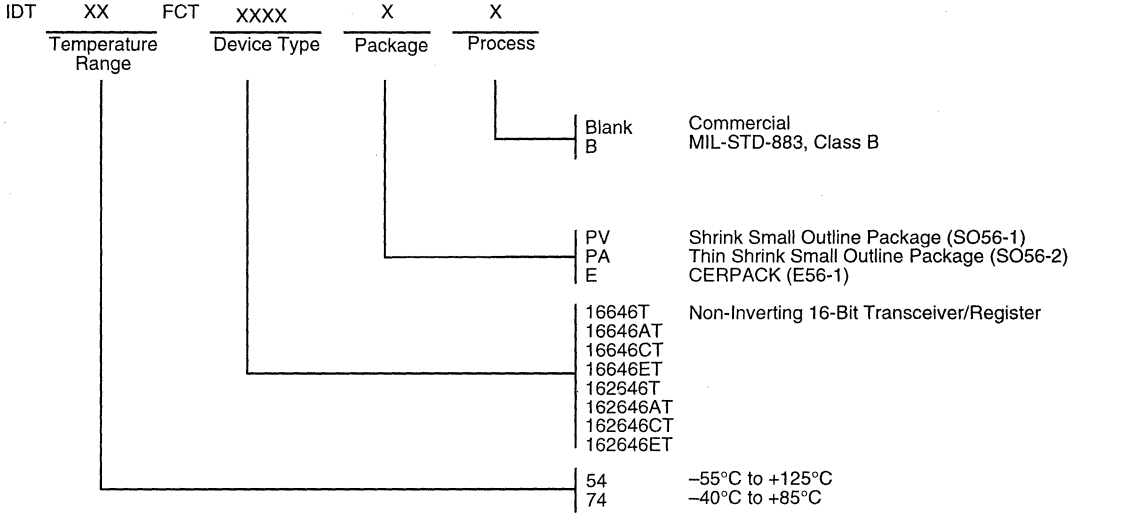


2556 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

ORDERING INFORMATION



2540 drw 14

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTERS

IDT54/74FCT16652T/AT/CT/ET
IDT54/74FCT162652T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16652T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162652T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

The FCT16652T/AT/CT/ET and FCT162652T/AT/CT/ET 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. For example, the xOEAB and $x\overline{OEBA}$ signals control the transceiver functions.

The xSAB and xSBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A LOW input level selects real-time data and a HIGH level selects stored data.

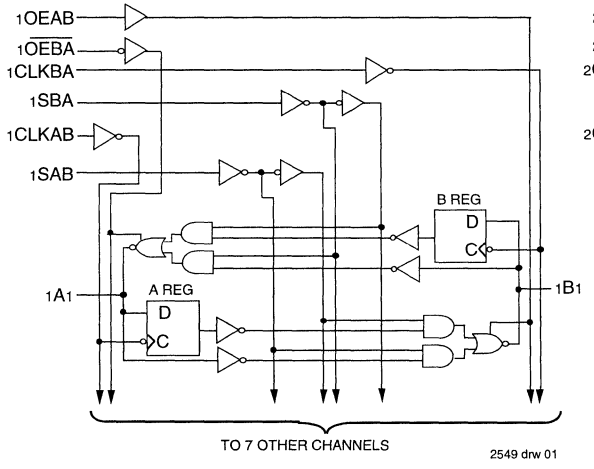
Data on the A or B data bus, or both, can be stored in the internal D-flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (xCLKAB or xCLKBA), regardless of the select or enable control pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

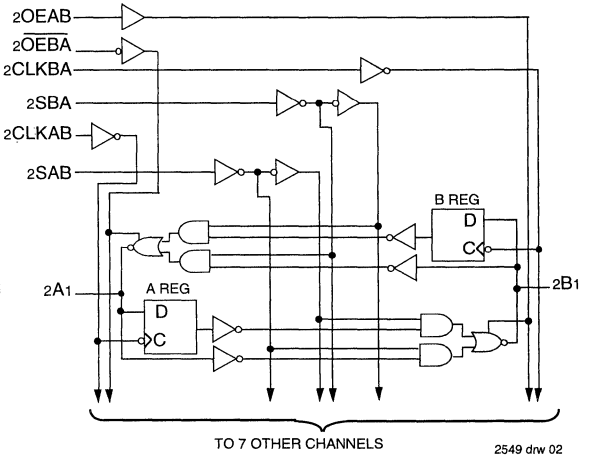
The FCT16652T/AT/CT/ET are ideally suited for driving high capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162652T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162652T/AT/CT/ET are plug-in replacements for the FCT16652T/AT/CT/ET and ABT16652 for on-board bus interface applications.

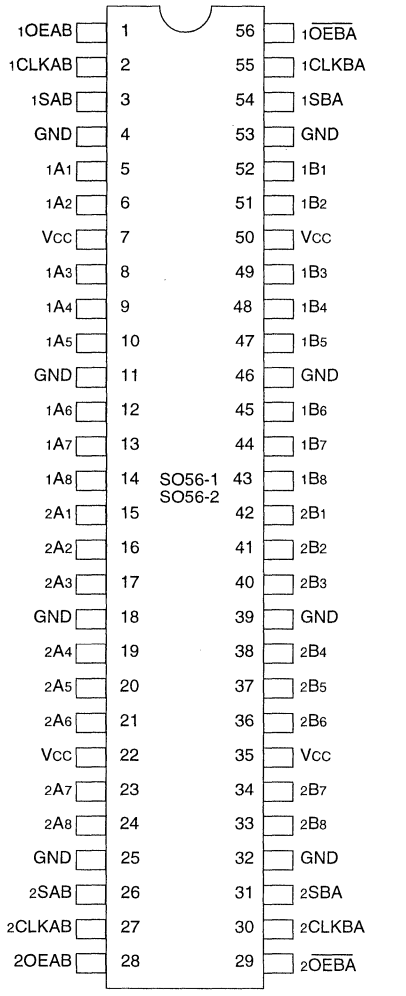
5

FUNCTIONAL BLOCK DIAGRAM



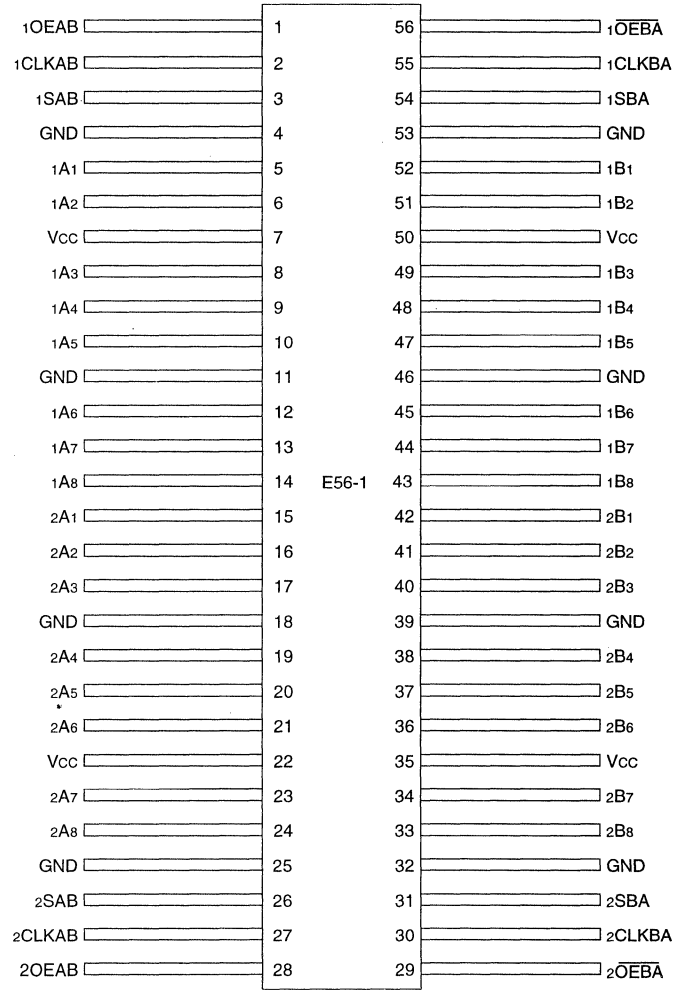


PIN CONFIGURATIONS



2549 drw 03

SSOP/ TSSOP TOP VIEW



2549 drw 04

CERPACK TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, x$\overline{OEBA}$	Output Enable Inputs

2549 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2549 lnk 02
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE[2]

Inputs						Data I/O[1]		Operation or Function
xOEAB	x$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[1]	Store A, Hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified[1]	Input	Hold A, Store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

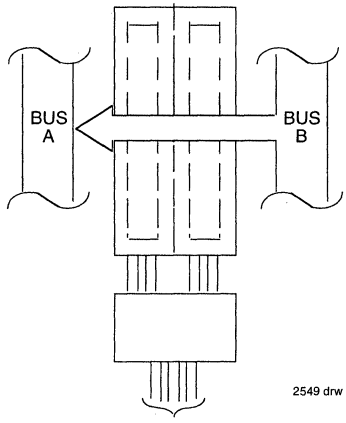
NOTES: 2549 tbl 03
1. The data output functions may be enabled or disabled by various signals at the xOEAB or x$\overline{OEBA}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered to load both registers.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

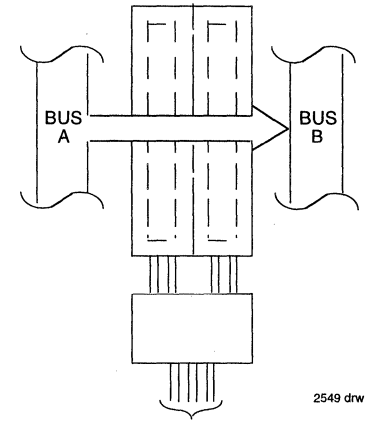
NOTES: 2549 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

5



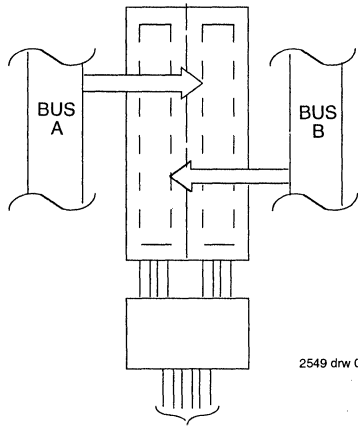
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



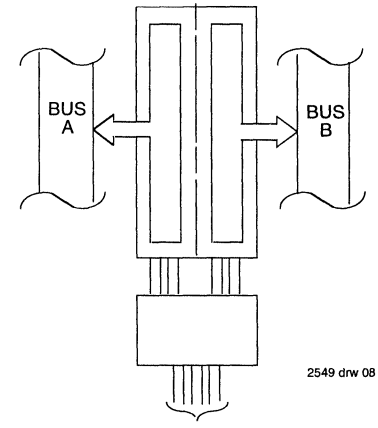
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2549 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16652T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2549 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162652T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2549 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xOEAB = x$\overline{OEBA}$=GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
		xOEAB = x$\overline{OEBA}$=GND One Bit Toggling fi = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
		xOEAB = x$\overline{OEBA}$=GND Sixteen Bits Toggling fi = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2549 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16652T/162652T				FCT16652AT/162652AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPZH tPZL	Output Enable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
tPHZ tPLZ	Output Disable Time xOEAB or x$\overline{OEBA}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2549 tbl 09

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Symbol	Parameter	Condition[1]	FCT16652CT/162652CT				FCT16652ET/162652ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	3.8	—	—	ns
tPZH tPZL	Output Enable Time xOEAB or x$\overline{OEBA}$ to Bus		1.5	7.8	1.5	8.9	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time xOEAB or x$\overline{OEBA}$ to Bus		1.5	6.3	1.5	7.7	1.5	4.0	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		1.5	6.2	1.5	7.0	1.5	4.2	—	—	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0.0	—	—	—	ns
tW	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

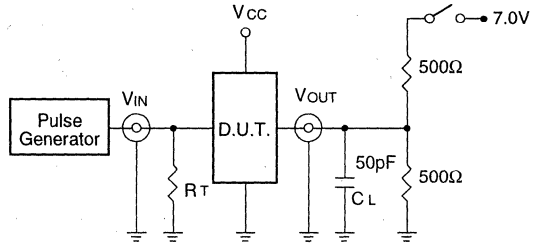
NOTES:

2549 tbl10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2549 drw 05

SWITCH POSITION

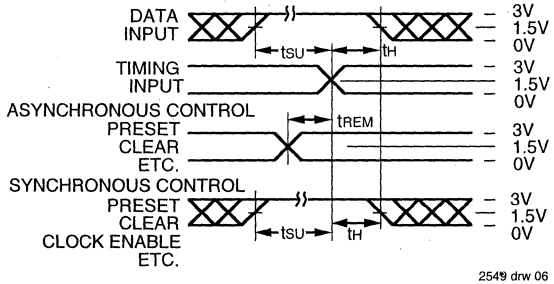
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2549 lnk 10

DEFINITIONS:

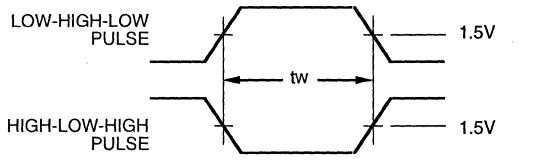
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



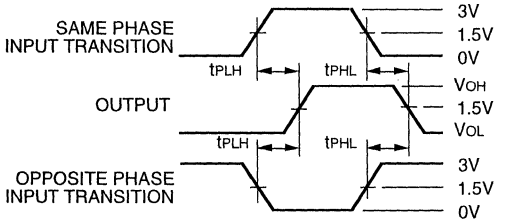
2549 drw 06

PULSE WIDTH



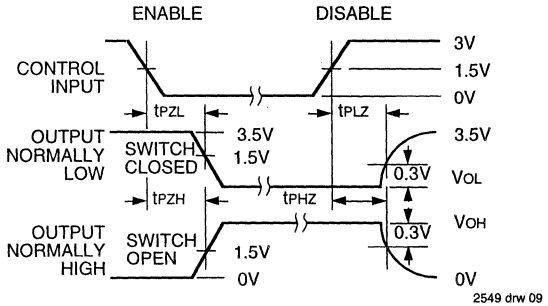
2549 drw 07

PROPAGATION DELAY



2549 drw 08

ENABLE AND DISABLE TIMES

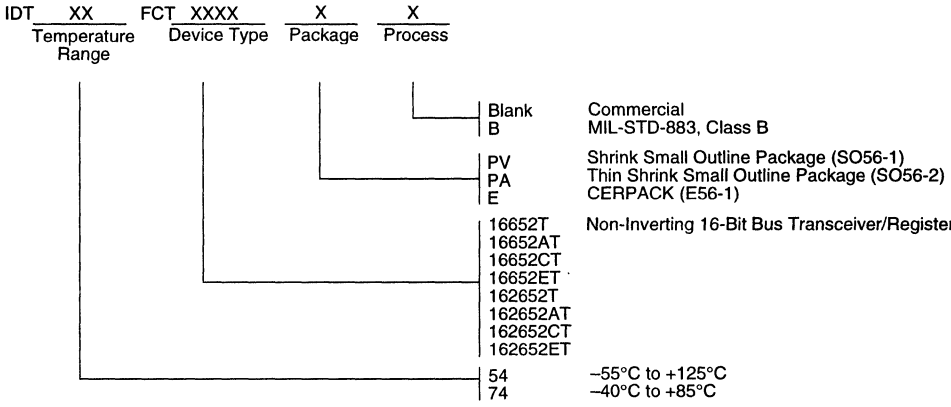


2549 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2549 drw 14

5

Integrated Device Technology, Inc.

FAST CMOS 18-BIT R/W BUFFER

IDT54/74FCT162701T/AT

FEATURES:

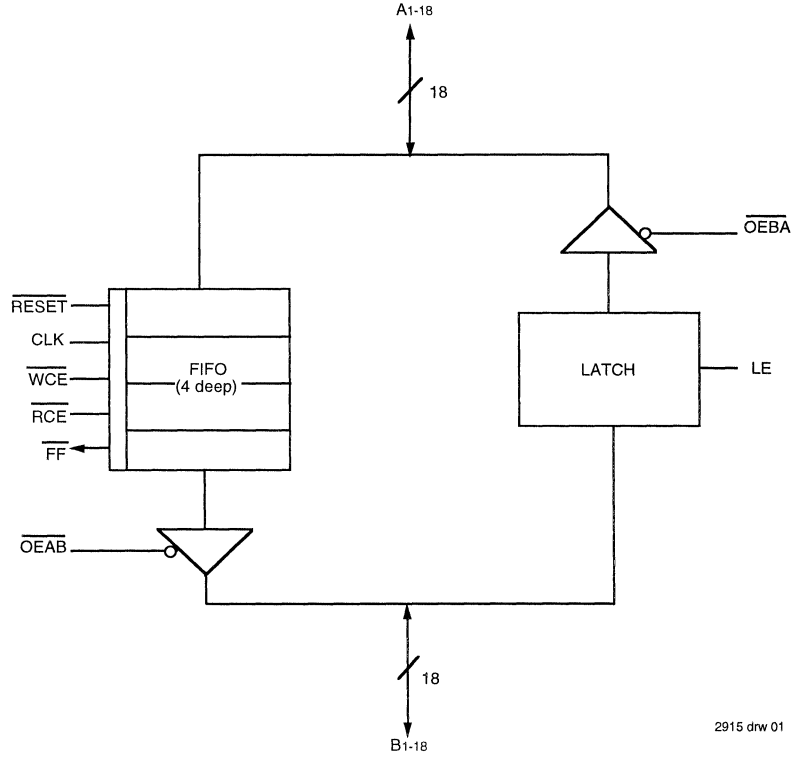
- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Low input and output leakage ≤1μA (max.)**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- Ideal for new generation x86 write-back cache solutions
- Suitable for modular x86 architectures
- Four deep write FIFO
- Latch in read path
- Synchronous FIFO reset

DESCRIPTION:

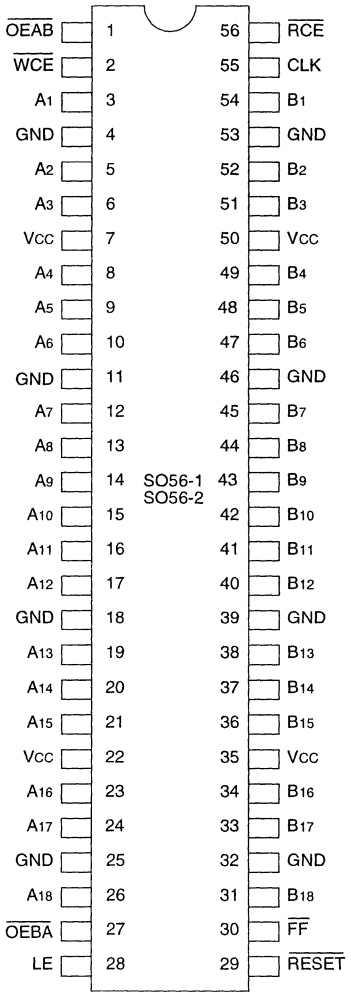
The FCT162701T/AT is an 18-bit Read/Write buffer with a four deep FIFO and a read-back latch. It can be used as a read/write buffer between a CPU and memory or to interface a high-speed bus and a slow peripheral. The A-to-B (write) path has a four deep FIFO for pipelined operations. The FIFO can be reset and a FIFO full condition is indicated by the full flag ($\overline{FF}$). The B-to-A (read) path has a latch. A HIGH on LE, allows data to flow transparently from B-to-A. A LOW on LE allows the data to be latched on the falling edge of LE.

The FCT162701T/AT has a balanced output drive with series termination. This provides low ground bounce, minimal undershoot and controlled output edge rates.

FUNCTIONAL BLOCK DIAGRAM

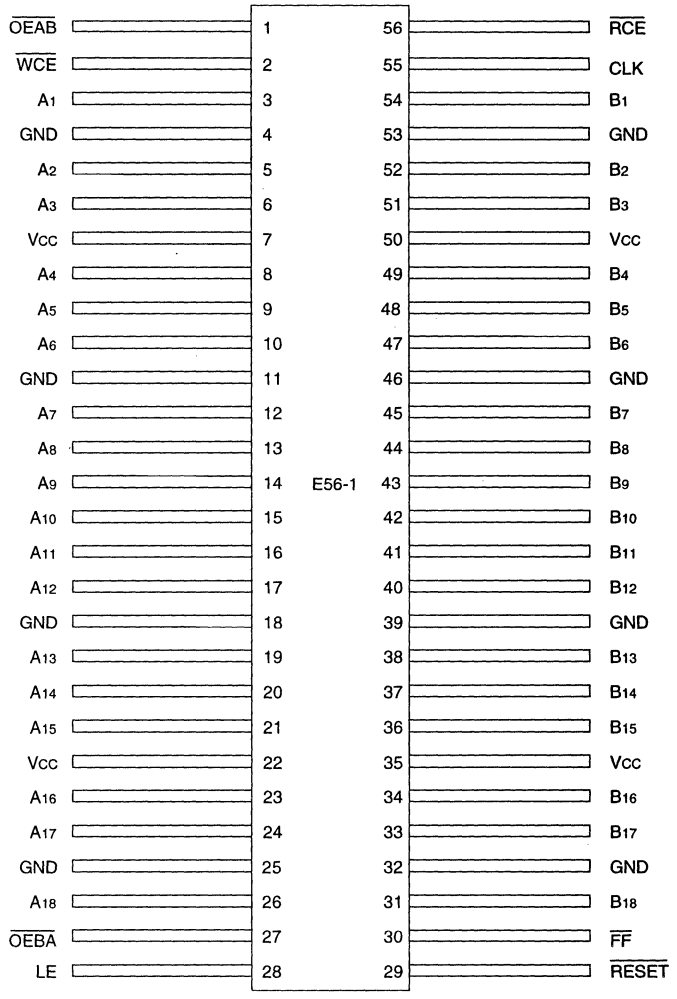


PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2915 drw 02



CERPACK
TOP VIEW

2915 drw 03

5

PIN DESCRIPTION

Pin Names	I/O	Description
A_{1-18}	I/O	18 bit I/O port.
B_{1-18}	I/O	18 bit I/O port.
CLK	I	Clock for write path FIFO. Clocks data into FIFO when $\overline{WCE}$ is low, clocks data out of FIFO when $\overline{RCE}$ is low. When FIFO is full all further writes to the FIFO are inhibited. When FIFO is empty all reads from the FIFO are inhibited. CLK also resets the FIFO when $\overline{RESET}$ is low.
$\overline{WCE}$	I	Enable pin for FIFO input clock.
$\overline{RCE}$	I	Enable pin for FIFO output clock.
$\overline{FF}$	O	Write path FIFO full flag. Goes low when FIFO is full.
$\overline{RESET}$	I	Synchronous FIFO reset - when low CLK resets the FIFO. The FIFO pointers are initialized to the "empty" condition and FIFO output is forced high (all ones). The FIFO full flag ($\overline{FF}$) will be high immediately after reset.
$\overline{OEAB}$	I	Output Enable pin for B port.
$\overline{OEBA}$	I	Output Enable pin for A port.
LE	I	Read path latch enable pin. When high, data flows transparently from B port to A port, B data is latched on the falling edge of LE.

2915 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2915 lnk 02

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2915 lnk 03

NOTE:

1. This parameter is measured at characterization but not tested.

FUNCTIONAL DESCRIPTION:

This device is useful as a read/write buffer for modular high end designs. It provides multi-level buffering in the write path and single deep buffering in the read path, and is suited to write back cache implementation. The read path provides a transparent latch.

The four deep FIFO uses one clock with two clock enable pins, $\overline{WCE}$ and $\overline{RCE}$ to clock data in and out. The FIFO has an external full flag which goes LOW when the FIFO is full. Internal read and write pointers keep track of the words stored in the FIFO. A write attempt to a full FIFO is ignored. An attempt to read from an empty FIFO will have no effect and the last read data remains at the output of the FIFO. The FIFO may be reset by the synchronous $\overline{RESET}$ input. This resets the read and write pointers to the original "empty" condition and also sets all B outputs = 1. Simultaneous read and write attempts (clock data into FIFO as well as clock data out of FIFO) are possible except on FIFO empty and full boundaries. When the FIFO is empty, and a simultaneous read and write is attempted, the read is ignored while the write is executed. If the same is attempted when the FIFO is full, the write is ignored while the read is executed. Normal operation of the four deep FIFO in the write path is independent of the read path operation.

Power, ground and data pin positions on the FCT162701T match those on the FCT16501T/162501T, allowing an easy upgrade.

APPLICATIONS: 486 INTERFACE

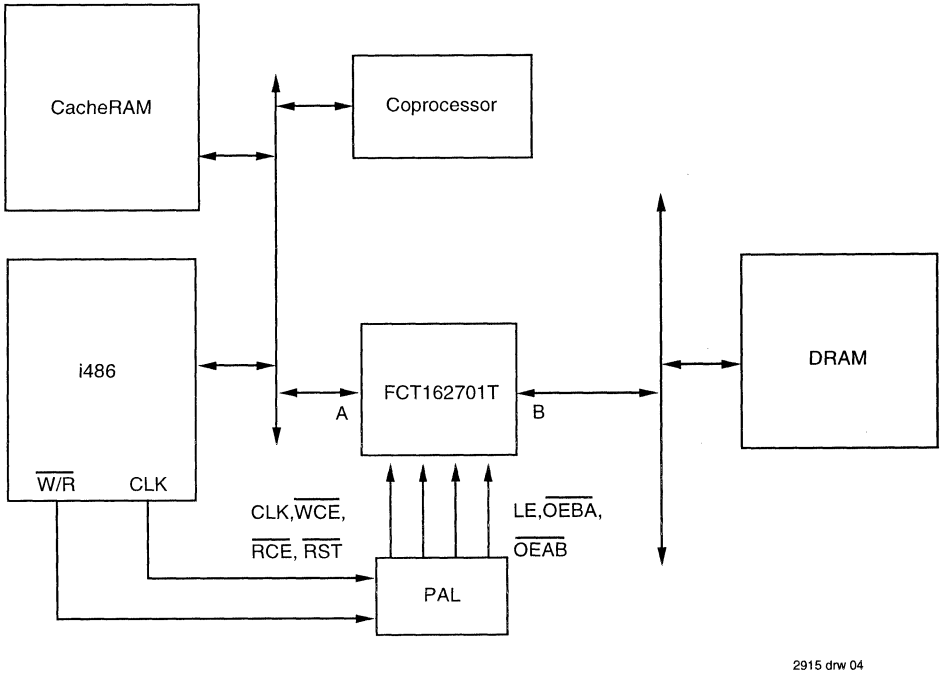


Figure 1. FCT162701T Application Example

5

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2915 lnk 04

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2915 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	1.5	mA
$I_{CCD (CLK)}$	Dynamic Power Supply Current due to clock switching[4]	V_{CC} = Max. Outputs Open	CLK Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	180	240	µA/ MHz
$I_{CCD (O/P)}$	Dynamic Power Supply Current due to output switching[4]		One Bit Toggling 50% Duty Cycle		—	80	120	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle		V_{IN} = V_{CC} V_{IN} = GND	—	1.8	2.9[5]	mA
		$\overline{OEAB}$ = GND; $\overline{OEBA}$ = V_{CC} LE = $\overline{WCE}$ = $\overline{RCE}$ = GND $\overline{RESET}$ = V_{CC} All Inputs Low		V_{IN} = 3.4V V_{IN} = GND	—	2.1	3.7[5]	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle		V_{IN} = V_{CC} V_{IN} = GND	—	2.2	3.5	
		$\overline{OEAB}$ = GND; $\overline{OEBA}$ = V_{CC} LE = $\overline{WCE}$ = $\overline{RCE}$ = GND $\overline{RESET}$ = V_{CC} One Bit Toggling at fo = 5MHz 50% Duty Cycle		V_{IN} = 3.4V V_{IN} = GND	—	2.7	5.0	

2915 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN}) = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD (CLK)} \times f_{CP} + I_{CCD (O/P)} \times f_O N_O$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameter		Test Conditions[1]	FCT162701T		FCT162701AT		
			Min.[2]	Max.[2]	Min.[2]	Max.[2]	Unit
PROPAGATION DELAYS							
1	B_{1-18} to A_{1-18}	Read path/latch	1.5	6.5	1.5	5.5	ns
2	LE (Low to Hi) to A_{1-18}	Read path/latch	1.5	5.7	1.5	4.7	ns
3	CLK to $\overline{FF}$	Write path	2	7.0	2	6.0	ns
4	CLK to B_{1-18}	Write path	1	6.0	1	5.2	ns
SETUP & HOLD TIMES[3]							
5	A_{1-18} to CLK (Low to Hi) Setup	Write path	2.5	—	2.5	—	ns
6	A_{1-18} to CLK (Low to Hi) Hold	Write path	0	—	0	—	ns
7	B_{1-18} to LE (Hi to Low) Setup	Read path/latch	3	—	3	—	ns
8	B_{1-18} to LE (Hi to Low) Hold	Read path/latch	0	—	0	—	ns
9	$\overline{WCE}$, $\overline{RCE}$ (Low) to CLK Setup	Write path	3	—	3	—	ns
10	$\overline{WCE}$, $\overline{RCE}$ (Low) to CLK Hold	Write path	0	—	0	—	ns
11	$\overline{RESET}$ (Low) to CLK Setup	Write path	3	—	3	—	ns
12	$\overline{RESET}$ (Low) to CLK Hold	Write path	0	—	0	—	ns
ENABLE & DISABLE TIMES[3]							
13	$\overline{OEBA}$ Low to A_{1-18} Enable	Write path	1.5	7.0	1.5	6.0	ns
14	$\overline{OEBA}$ High to A_{1-18} Disable	Write path	1.5	6.0	1.5	5.0	ns
15	$\overline{OEAB}$ Low to B_{1-18} Enable	Read path	1.5	7.0	1.5	6.0	ns
16	$\overline{OEAB}$ High to B_{1-18} Disable	Read path	1.5	6.0	1.5	5.0	ns
MINIMUM PULSE WIDTHS							
17	CLK HIGH or LOW Pulse Width	Write path	3.0	—	3.0	—	ns
18	LE HIGH Pulse Width	Read path/latch	3.0	—	3.0	—	ns

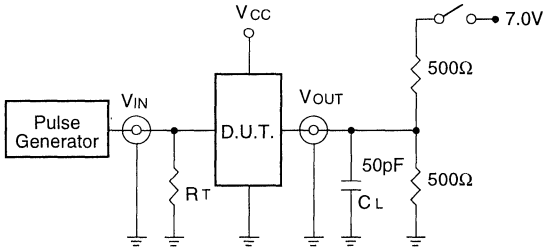
NOTES:

2915 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2915 drw 04

SWITCH POSITION

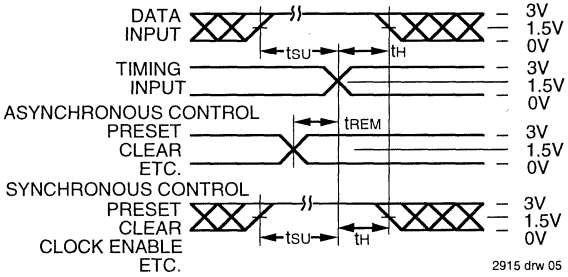
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2915 lnk 07

DEFINITIONS:

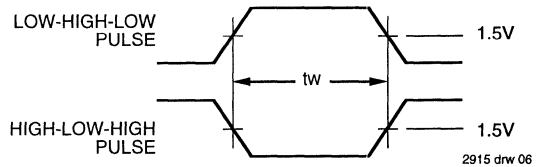
CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



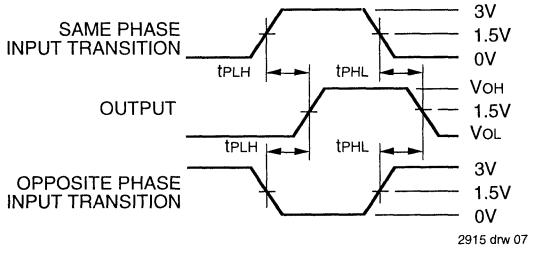
2915 drw 05

PULSE WIDTH



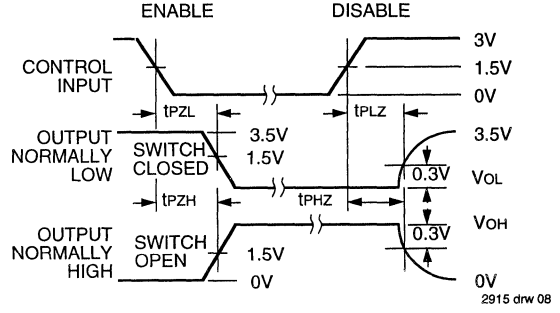
2915 drw 06

PROPAGATION DELAY



2915 drw 07

ENABLE AND DISABLE TIMES

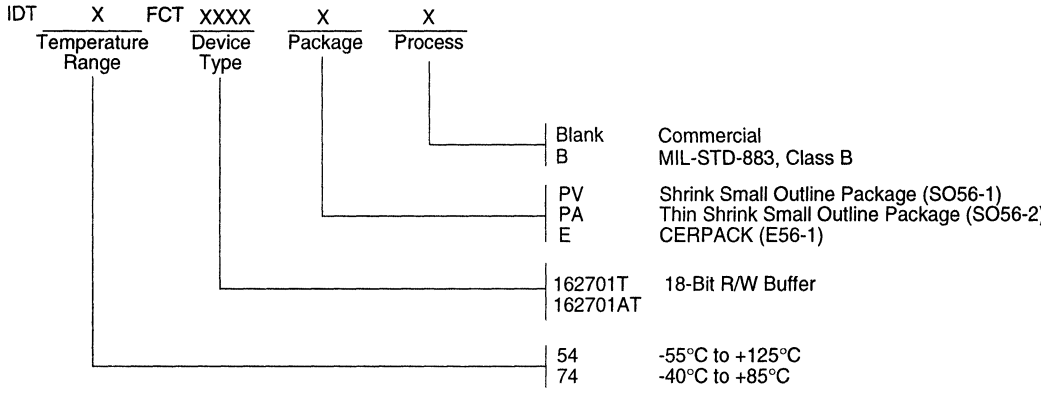


2915 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

ORDERING INFORMATION



2915 drw 09

Integrated Device Technology, Inc.

FAST CMOS 18-BIT REGISTER

IDT54/74FCT16823AT/BT/CT/ET
IDT54/74FCT162823AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16823AT/BT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162823AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

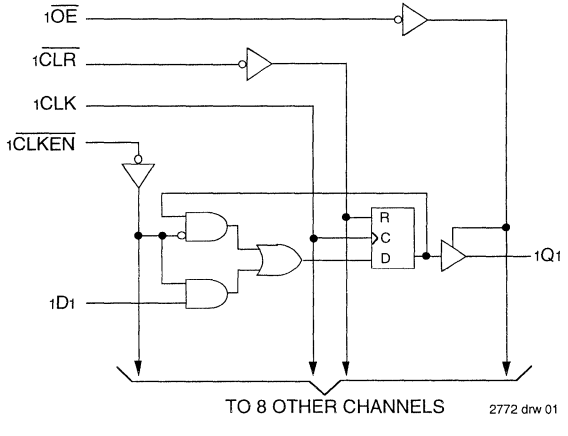
The FCT16823AT/BT/CT/ET and FCT162823AT/BT/CT/ET 18-bit bus interface registers are built using advanced, dual metal CMOS technology. These high-speed, low-power registers with clock enable (x$\overline{CLKEN}$) and clear (x$\overline{CLR}$) controls are ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

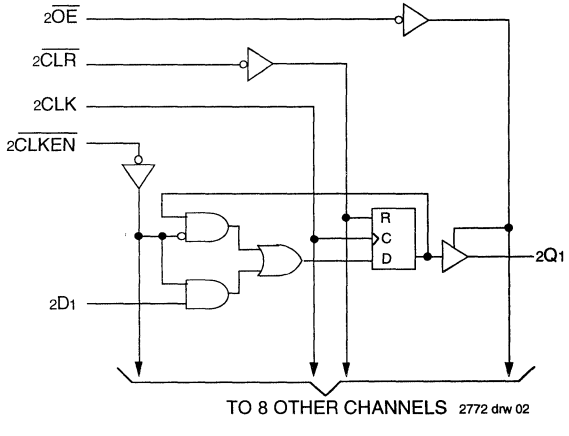
The FCT16823AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162823AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times – reducing the need for external series terminating resistors. The FCT162823AT/BT/CT/ET are plug-in replacements for the FCT16823AT/BT/CT/ET and ABT16823 for on-board interface applications.

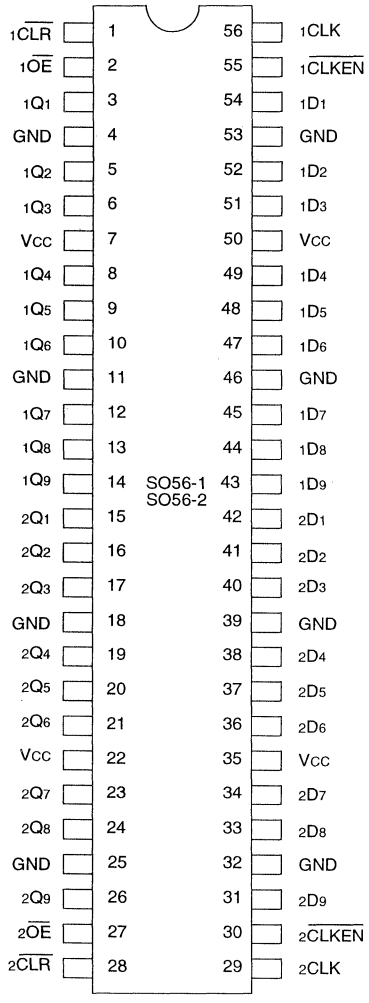
5

FUNCTIONAL BLOCK DIAGRAM



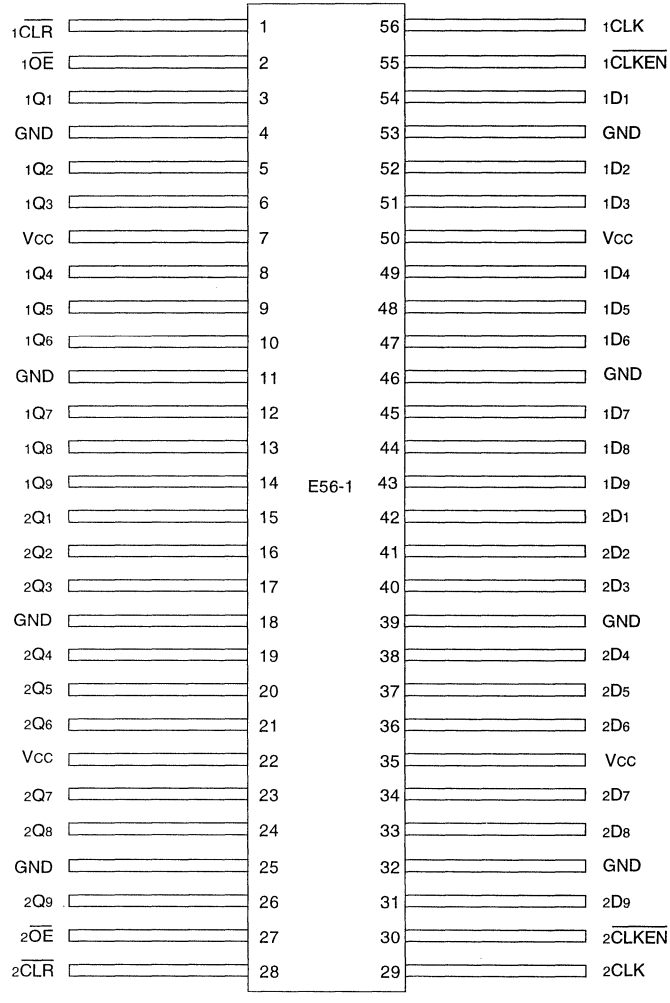


PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2772 drw 03



CERPACK
TOP VIEW

2772 drw 04

PIN DESCRIPTION

Pin Names	Description
xDx	Data inputs
xCLK	Clock Inputs
$x\overline{CLKEN}$	Clock Enable Inputs (Active LOW)
$x\overline{CLR}$	Asynchronous clear Inputs (Active LOW)
$x\overline{OE}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

2772 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2772 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

FUNCTION TABLE(1)

Inputs					Outputs	
$x\overline{OE}$	$x\overline{CLR}$	$x\overline{CLKEN}$	xCLK	xDx	xQx	Function
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q(2)	Hold
H	H	L	↑	L	Z	Load
H	H	L	↑	H	Z	
L	H	L	↑	L	L	
L	H	L	↑	H	H	

NOTES: 2772 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before indicated steady-state input conditions were established.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2772 lnk 04

1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2772 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16823T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2772 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162823T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2772 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xOE = $xCLKEN$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	2.7	mA
		xOE = $xCLKEN$ = GND at fi = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.2	7.1[5]	
		xOE = $xCLKEN$ = GND at fi = 2.5MHz 50% Duty Cycle Eighteen Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	9.2	22.1[5]	

2772 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16823AT/162823AT				FCT16823BT/162823BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	
t_{PHL}	Propagation Delay x$\overline{CLR}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	C_L = 5pF[5] R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	
t_{SU}	Set-up Time HIGH or LOW xDx to xCLK	C_L = 50pF R_L = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW xDx to xCLK		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		4.0	—	4.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		2.0	—	2.0	—	0	—	0	—	ns
t_W	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	ns
t_W	x$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	ns
t_{REM}	Recovery Time x$\overline{CLR}$ to xCLK		6.0	—	7.0	—	6.0	—	6.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2772 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16823CT/162823CT				FCT16823ET/162823ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLK to xQx	CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.4	—	—	ns
		CL = 300pF[5] RL = 500Ω	1.5	12.5	1.5	13.5	1.5	8.0	—	—	
tPHL	Propagation Delay x$\overline{CLR}$ to xQx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	4.4	—	—	ns
tPZH tPZL	Output Enable Time x$\overline{OE}$ to xQx	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	4.4	—	—	ns
		CL = 300pF[5] RL = 500Ω	1.5	12.5	1.5	13.5	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time x$\overline{OE}$ to xQx	CL = 5pF[5] RL = 500Ω	1.5	6.2	1.5	6.2	1.5	3.6	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.5	1.5	6.5	1.5	3.6	—	—	
tSU	Set-up Time HIGH or LOW xDx to xCLK	CL = 50pF RL = 500Ω	3.0	—	3.0	—	1.5	—	—	—	ns
tH	Hold Time HIGH or LOW xDx to xCLK		1.5	—	1.5	—	0.0	—	—	—	ns
tSU	Set-up Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		3.0	—	3.0	—	2.5	—	—	—	ns
tH	Hold Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		0	—	0	—	0.0	—	—	—	ns
tW	xCLK Pulse Width HIGH or LOW		6.0	—	6.0	—	3.0[4]	—	—	—	ns
tW	x$\overline{CLR}$ Pulse Width LOW		6.0	—	6.0	—	3.0[4]	—	—	—	ns
tREM	Recovery Time x$\overline{CLR}$ to xCLK		6.0	—	6.0	—	3.0	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

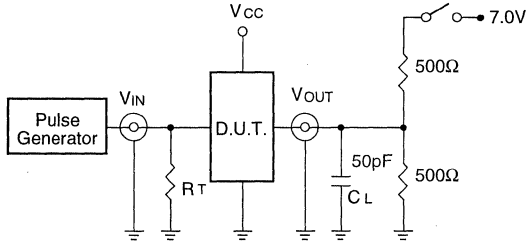
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

2772 tbl 10

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2772 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

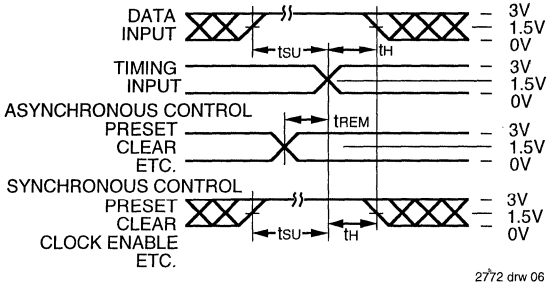
2772 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

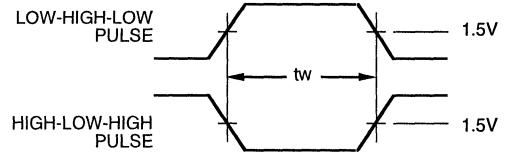
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



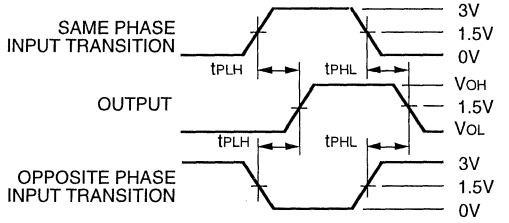
2772 drw 06

PULSE WIDTH



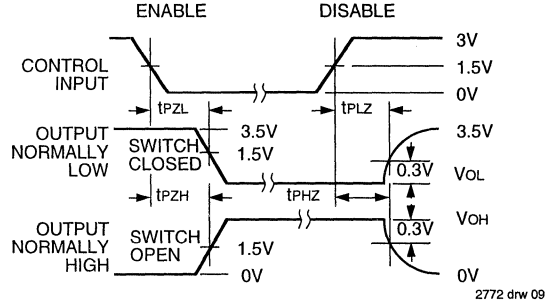
2772 drw 07

PROPAGATION DELAY



2772 drw 08

ENABLE AND DISABLE TIMES

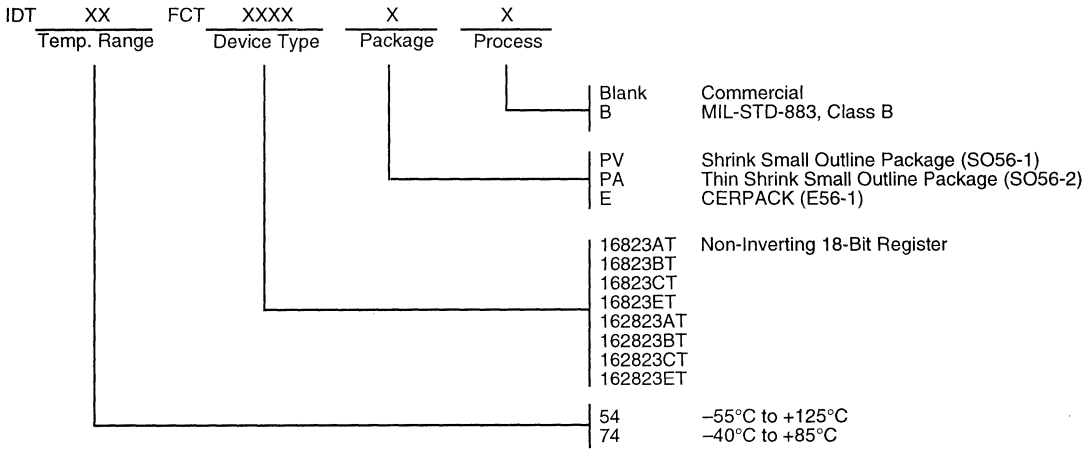


2772 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2772 drw 10

5

Integrated Device Technology, Inc.

FAST CMOS 20-BIT BUFFERS

IDT54/74FCT16827AT/BT/CT/ET
IDT54/74FCT162827AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16827AT/BT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162827AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

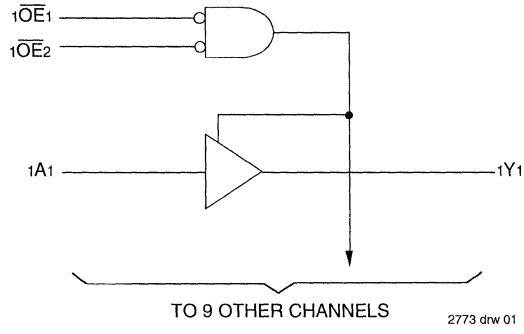
DESCRIPTION:

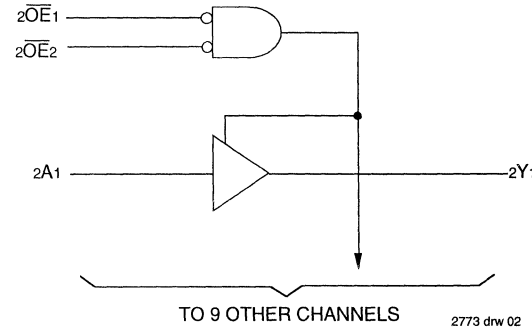
The FCT16827AT/BT/CT/ET and FCT162827AT/BT/CT/ET 20-bit buffers are built using advanced dual metal CMOS technology. These 20-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pair of NAND-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16827AT/BT/CT/ET are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

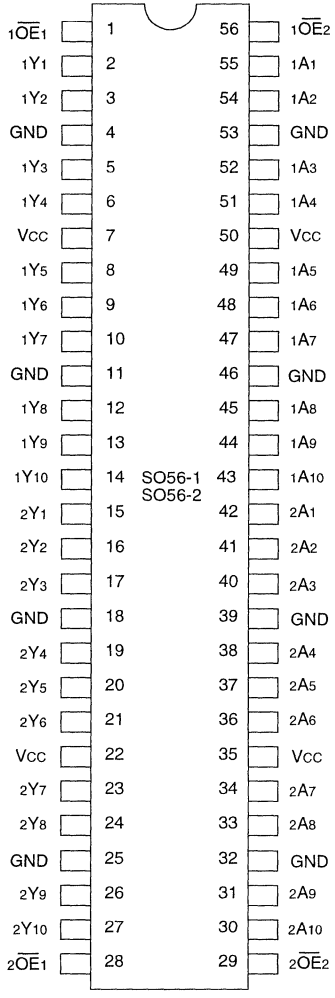
The FCT162827AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162827AT/BT/CT/ET are plug-in replacements for the FCT16827AT/BT/CT/ET and ABT16827 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



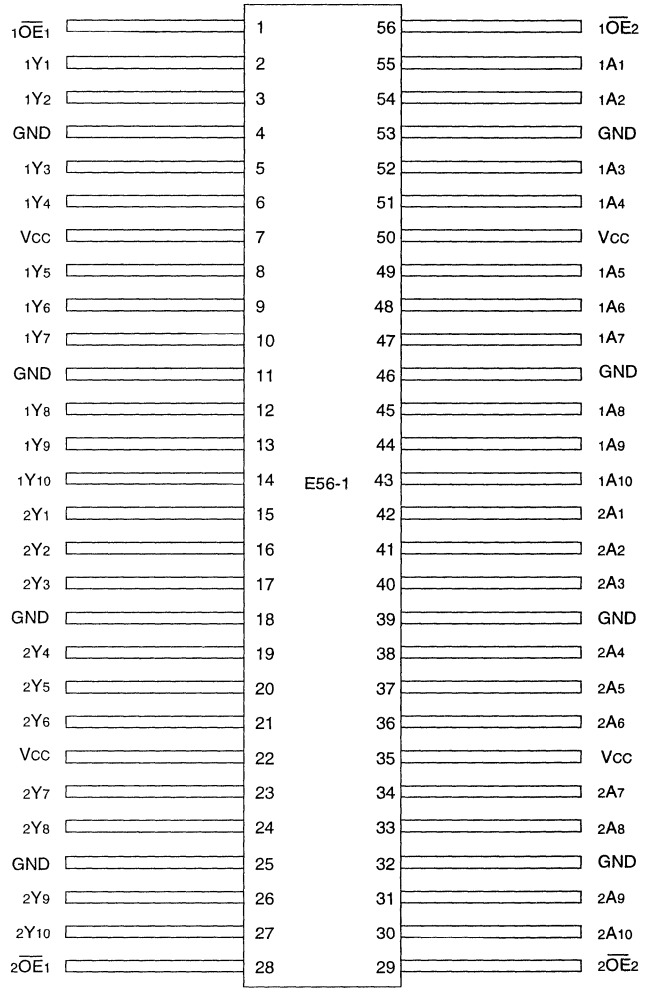


PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2773 drw 03



CERPACK
TOP VIEW

2773 drw 04

5

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}x$	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2773 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2773 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

FUNCTION TABLE(1)

Inputs			Outputs
$x\overline{OE}_1$	$x\overline{OE}_2$	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

2773 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2773 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2773 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2773 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2773 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}_1 = x\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $x\overline{OE}_1 = x\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}_1 = x\overline{OE}_2$ = GND Twenty Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.0	20.5[5]	

2773 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16827AT/162827AT				FCT16827BT/162827BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$x to xYx	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$x to xYx	C_L = 5pF[4] R_L = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2773 tbl 09

Symbol	Parameter	Condition[1]	FCT16827CT/162827CT				FCT16827ET/162827ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	4.4	1.5	5.0	1.5	3.2	—	—	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	10.0	1.5	11.0	1.5	7.0	—	—	
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$x to xYx	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	4.8	—	—	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	—	—	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$x to xYx	C_L = 5pF[4] R_L = 500Ω	1.5	5.7	1.5	6.7	1.5	4.0	—	—	ns
		C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	7.0	1.5	4.0	—	—	
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

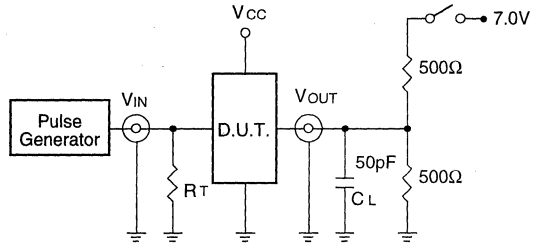
2773 tbl 10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This condition is guaranteed but not tested.

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2773 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

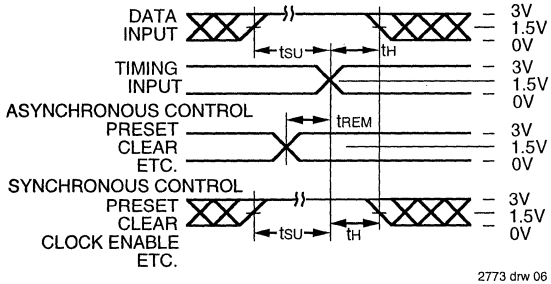
2773 lnk 11

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

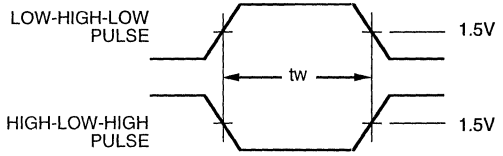
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



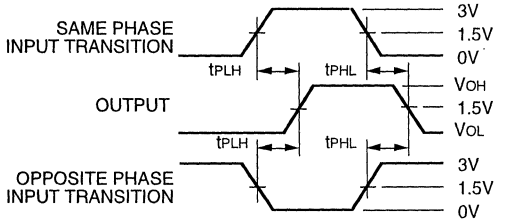
2773 drw 06

PULSE WIDTH



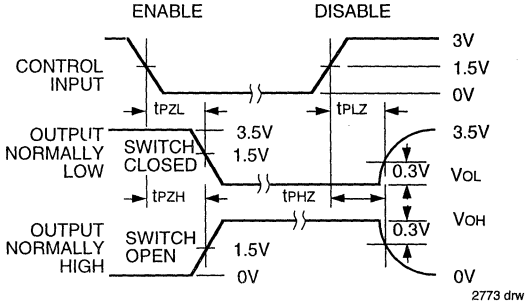
2773 drw 07

PROPAGATION DELAY



2773 drw 08

ENABLE AND DISABLE TIMES

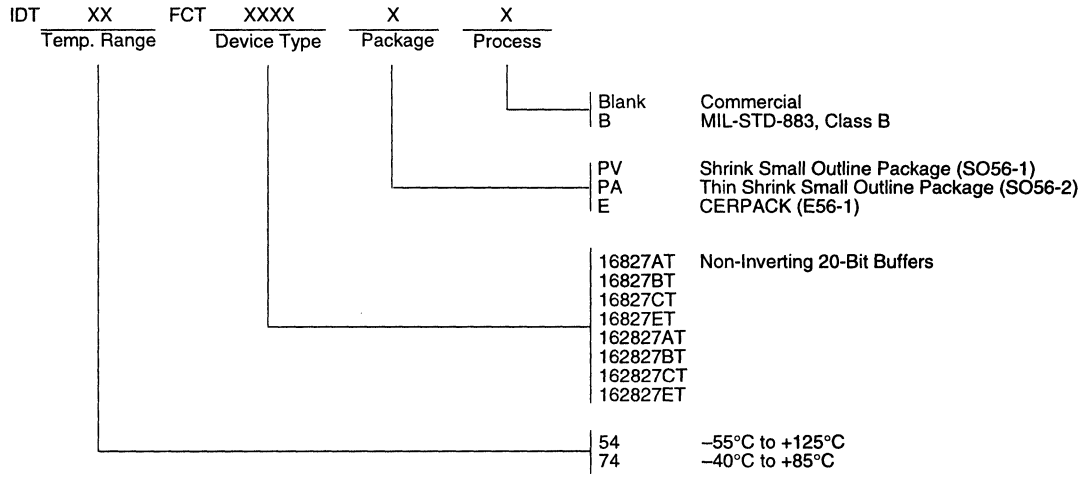


2773 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2773 drw 10

5

Integrated Device Technology, Inc.

FAST CMOS 20-BIT TRANSPARENT LATCHES

IDT54/74FCT16841AT/BT/CT/ET
IDT54/74FCT162841AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16841AT/BT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162841AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

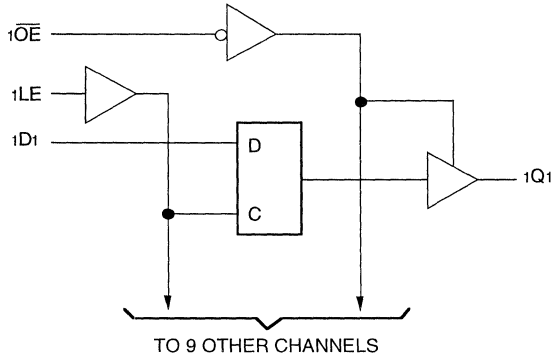
DESCRIPTION:

The FCT16841AT/BT/CT/ET and FCT162841AT/BT/CT/ET 20-bit transparent D-type latches are built using advanced dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 10-bit latches or one 20-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

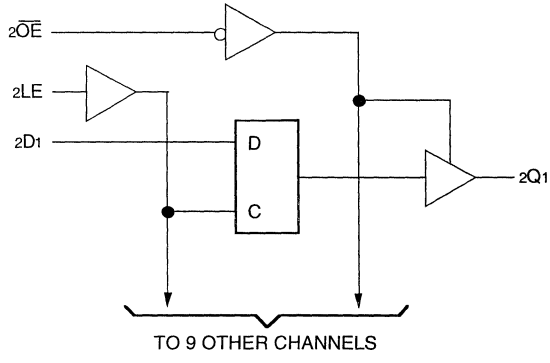
The FCT16841AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162841AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162841AT/BT/CT/ET are plug-in replacements for the FCT16841AT/BT/CT/ET and ABT16841 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM

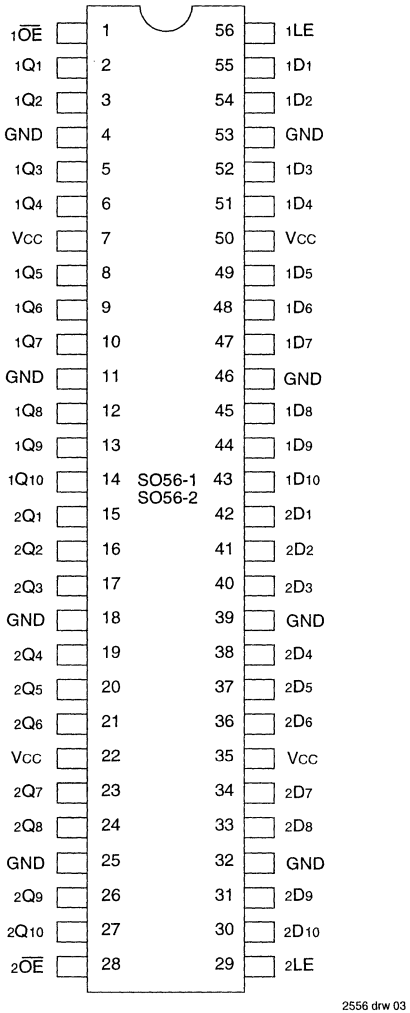


2556 drw 01



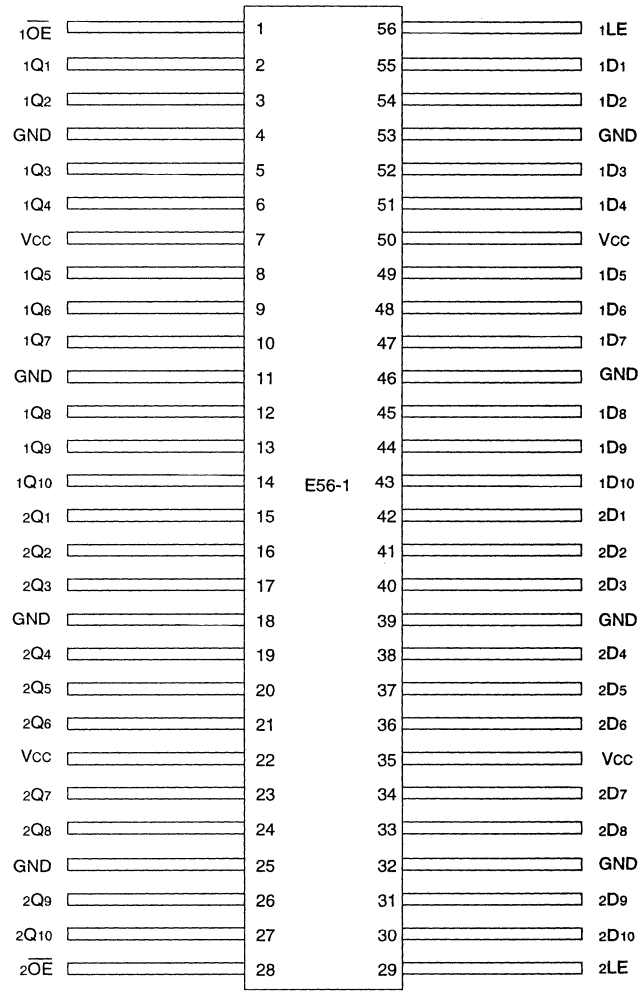
2556 drw 02

PIN CONFIGURATIONS



2556 drw 03

SSOP
TSSOP
TOP VIEW



2556 drw 04

CERPACK
TOP VIEW

5

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active HIGH)
$x\overline{OE}$	Output Enable Input (Active LOW)
xQx	3-State Outputs

2556 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xDx	xLE	$x\overline{OE}$	xQx
H	H	L	H
L	H	L	L
X	L	L	Q[2]
X	X	H	Z

2556 tbl 02

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before xLE HIGH-to-LOW Transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2556 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2556 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2556 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16841T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2556 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162841T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2556 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.5[5]	
		50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} Twenty Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.0	20.5[5]	

2556 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16841AT/162841AT				FCT16841BT/162841BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xDx to xQx (LE = HIGH)	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
t_{PLH} t_{PHL}	Propagation Delay xLE to xQx	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	C_L = 5pF[5] R_L = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	
t_{SU}	Set-Up Time HIGH or LOW, xDx to xLE	C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time HIGH or LOW, xDx to xLE		2.5	—	3.0	—	2.5	—	2.5	—	ns
t_W	xLE Pulse Width HIGH		4.0[4]	—	5.0	—	4.0[4]	—	4.0[4]	—	ns
$t_{SK(o)}$	Output skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
2556 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

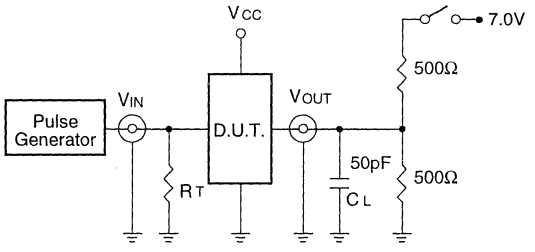
Symbol	Parameter	Condition[1]	FCT16841CT/162841CT				FCT16841ET/162841ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xDx to xQx (LE = HIGH)	C_L = 50pF R_L = 500Ω	1.5	5.5	1.5	6.3	1.5	3.4	—	—	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	13.0	1.5	15.0	1.5	7.5	—	—	
t_{PLH} t_{PHL}	Propagation Delay xLE to xQx	C_L = 50pF R_L = 500Ω	1.5	6.4	1.5	6.8	1.5	3.7	—	—	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	15.0	1.5	16.0	1.5	7.5	—	—	
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.3	1.5	4.4	—	—	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	9.0	—	—	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	C_L = 5pF[5] R_L = 500Ω	1.5	5.7	1.5	6.0	1.5	3.6	—	—	ns
		C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	6.3	1.5	3.6	—	—	
t_{SU}	Set-Up Time HIGH or LOW, xDx to xLE	C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	1.0	—	—	—	ns
t_H	Hold Time HIGH or LOW, xDx to xLE		2.5	—	2.5	—	1.0	—	—	—	ns
t_W	xLE Pulse Width HIGH		4.0[4]	—	4.0[4]	—	3.0[4]	—	—	—	ns
$t_{SK(o)}$	Output skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2556 tbl 10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2556 drw 05

SWITCH POSITION

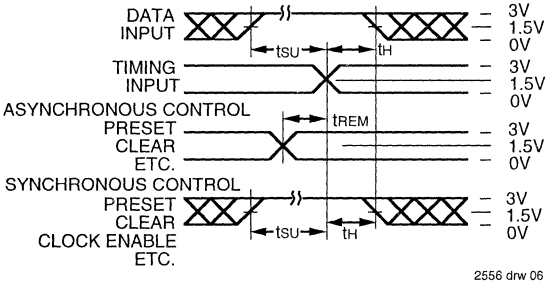
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2556 lnk 11

DEFINITIONS:

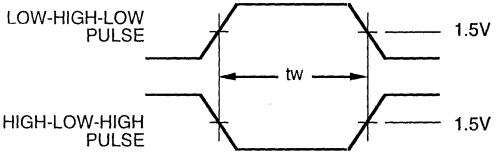
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



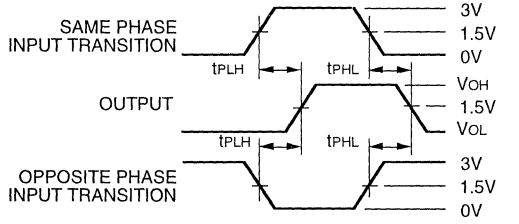
2556 drw 06

PULSE WIDTH



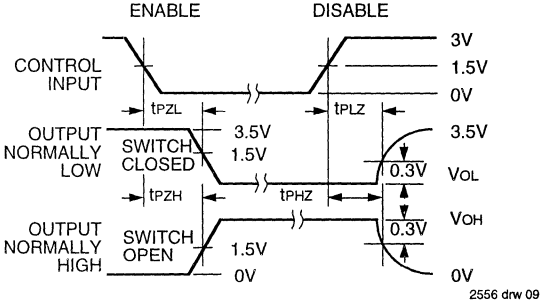
2556 drw 07

PROPAGATION DELAY



2556 drw 08

ENABLE AND DISABLE TIMES



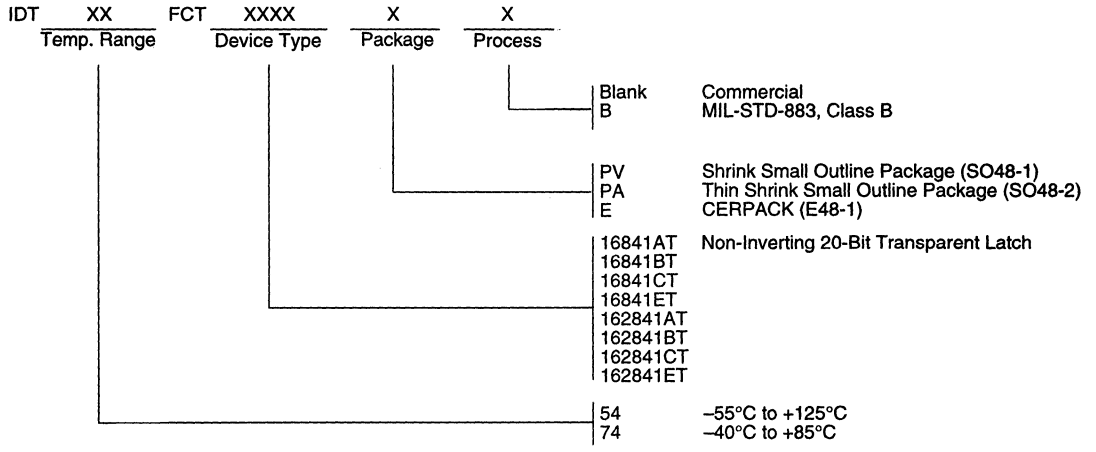
2556 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

5

ORDERING INFORMATION



2556 drw 10

Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16952AT/BT/CT/ET
IDT54/74FCT162952AT/BT/CT/ET
IDT54/74FCT162H952AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤ 1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
- **Features for FCT16952AT/BT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162952AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162H952AT/BT/CT/ET:**
  - Bus Hold retains last active bus state during 3-state
  - Eliminates the need for external pull up resistors

DESCRIPTION:

The FCT16952AT/BT/CT/ET and FCT162952AT/BT/CT/ET 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type registered transceivers with separate input and output control for independent control of data flow in either direction. For example, the A-to-B Enable ($xCEAB$) must be LOW to enter data from the A port. xCLKAB controls the clocking function. When xCLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. $xOEAB$ performs the output enable function on the B port. Data flow from the B port to A port is similar but requires using $xCEBA$, xCLKBA, and $xOEBA$ inputs. Full 16-bit operation is achieved by tying the control pins of the independent transceivers together.

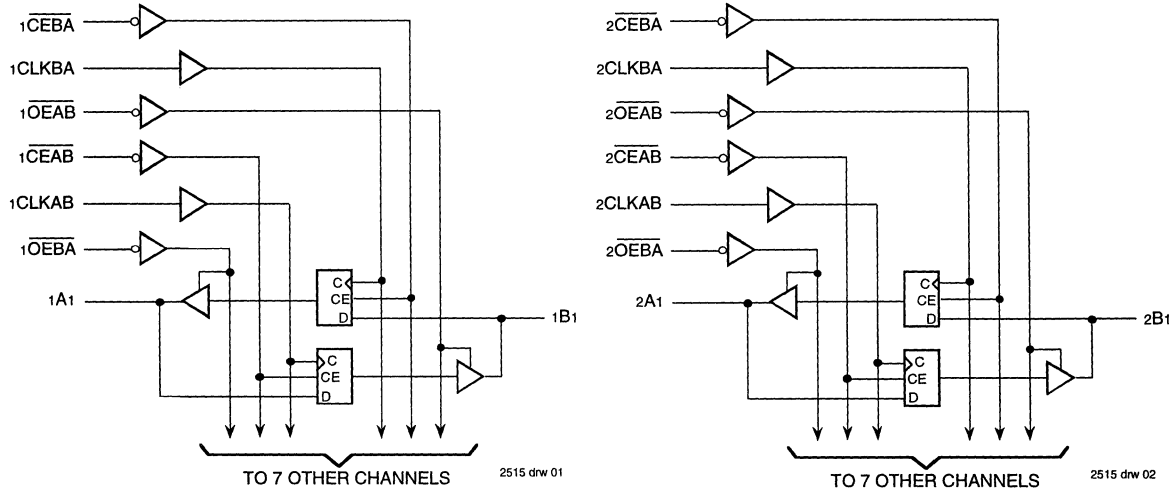
The FCT16952AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability allowing "live insertion" of boards when used as backplane drivers.

The FCT162952AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162952AT/BT/CT/ET are plug-in replacements for the FCT16952AT/BT/CT/ET and ABT16952 for on-board bus interface applications.

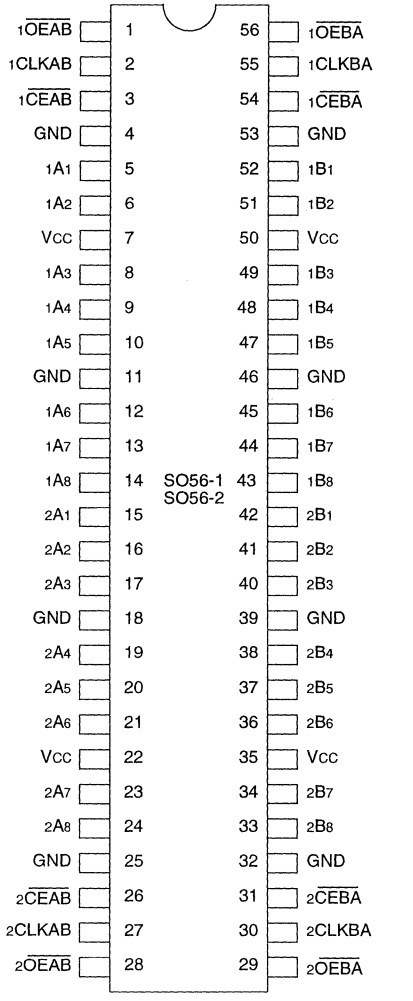
The FCT162H952AT/BT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

5

FUNCTIONAL BLOCK DIAGRAM

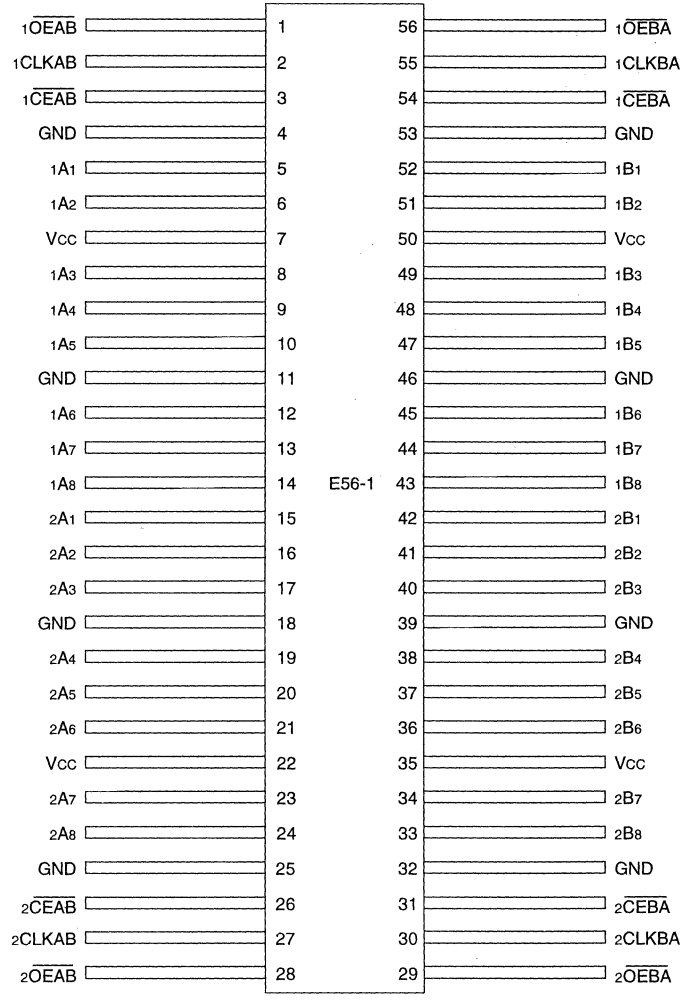


PIN CONFIGURATIONS



2515 drw 03

SSOP
TSSOP
TOP VIEW



2515 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$xOEAB$	A-to-B Output Enable Input (Active LOW)
$xOEBA$	B-to-A Output Enable Input (Active LOW)
$xCEAB$	A-to-B Clock Enable Input (Active LOW)
$xCEBA$	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs(1)
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs(1)

NOTE: 2515 tbl 01
1. On FCT16xH952T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

FUNCTION TABLE(1,3)

Inputs				Outputs
$xCEAB$	xCLKAB	$xOEAB$	xAx	xBx
H	X	L	X	B(2)
X	L	L	X	B(2)
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES: 2515 tbl 02
1. A-to-B data flow is shown: B-to-A data flow is similar but uses, $xCEBA$, xCLKBA, and $xOEBA$.
2. Level of B before the indicated steady-state input conditions were established.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High-impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2515 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2515 lnk 04
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2515 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16952T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2515 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162952T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2515 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter		Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	Standard Input[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
		Standard I/O[5]			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I_{IL}	Input LOW Current[4]	Standard Input[5]		V_I = GND	—	—	±1	
		Standard I/O[5]			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I_{BHH}	Bus Hold Sustain Current[4]	Bus Hold Input	V_{CC} = Min.	V_I = 2.0V	–50	—	—	µA
I_{BHL}				V_I = 0.8V	+50	—	—	
I_{OZH}	High Impedance Output Current (3-State Output pins)[5,6]		V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}				V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage		V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current		V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis		—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current		V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2515 lnk 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.
6. Does not include Bus Hold I/O pins.

5

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $x\overline{OEAB}$ or $x\overline{OEBA}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max., Outputs Open f_{CP}= 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2515 tbl 09

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16952AT/162952AT				FCT16952BT/162952BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time $xOEBA$, $xOEAB$ to xAx, xBx		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
tPHZ tPLZ	Output Disable Time $xOEBA$, $xOEAB$ to xAx, xBx		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
tSU	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.0	—	2.0	—	1.5	—	1.5	—	ns
tSU	Set-up Time, HIGH or LOW $xCEAB$, $xCEBA$ to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $xCEAB$, $xCEBA$ to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	Pulse Width HIGH or LOW xCLKAB or xCLKBA[4]		3.0	—	3.0	—	3.0	—	3.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2515 tbl 10

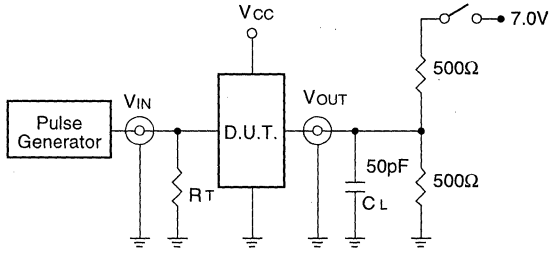
Symbol	Parameter	Condition[1]	FCT16952CT/162952CT				FCT16952ET/162952ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	CL = 50pF RL = 500Ω	2.0	6.3	2.0	7.3	1.5	3.7	—	—	ns
tPZH tPZL	Output Enable Time $xOEBA$, $xOEAB$ to xAx, xBx		1.5	7.0	1.5	8.0	1.5	4.4	—	—	ns
tPHZ tPLZ	Output Disable Time $xOEBA$, $xOEAB$ to xAx, xBx		1.5	6.5	1.5	7.5	1.5	3.6	—	—	ns
tSU	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	1.5	—	—	—	ns
tH	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		1.5	—	1.5	—	0	—	—	—	ns
tSU	Set-up Time, HIGH or LOW $xCEAB$, $xCEBA$ to xCLKAB, xCLKBA		3.0	—	3.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW $xCEAB$, $xCEBA$ to xCLKAB, xCLKBA		2.0	—	2.0	—	0	—	—	—	ns
tW	Pulse Width HIGH or LOW xCLKAB or xCLKBA[4]		3.0	—	3.0	—	3.0	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

2515 tbl 11

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2515 drw 05

SWITCH POSITION

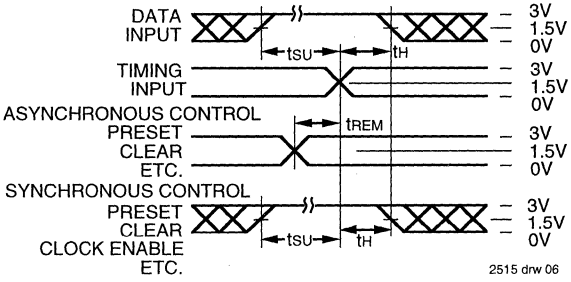
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2515 lnk 12

DEFINITIONS:

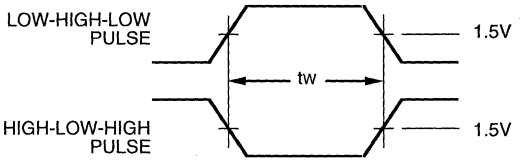
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



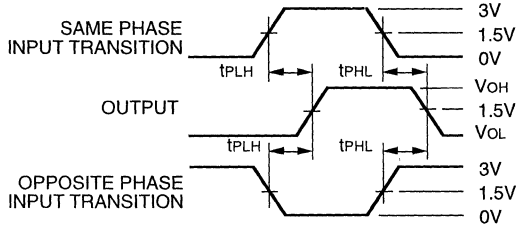
2515 drw 06

PULSE WIDTH



2515 drw 07

PROPAGATION DELAY



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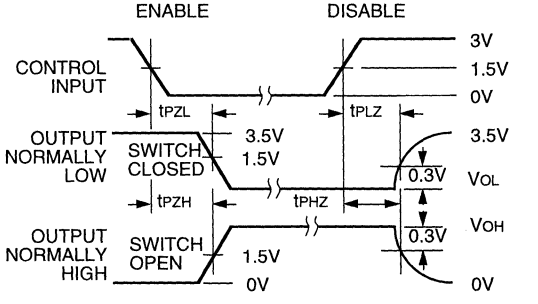
ENABLE AND DISABLE TIMES

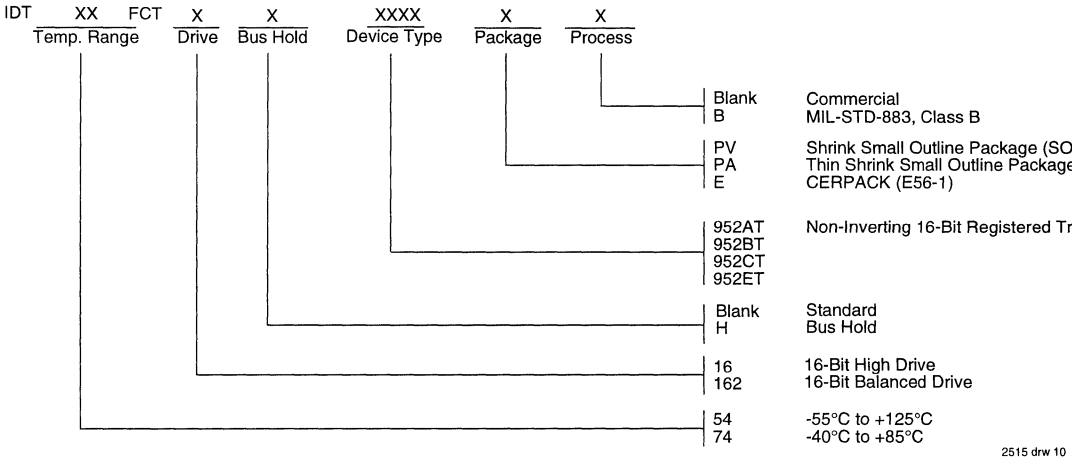


2515 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2515 drw 10

5

FCT-T OCTAL LOGIC

FCT-T Octal Logic has been designed for use in standard TTL-Logic applications. The family features high speed with low power dissipation. The family consists of a large variety of functions including bus interface products, counters, multiplexers, comparators, and other devices. There are two output configurations available which are the industry standard High Drive and the low-noise Balanced Drive. All components come in several performance grades, ranging from industry standard FAST™ speeds to today's state-of-the-art speeds, providing an easy system upgrade path. For systems migrating from 5V to 3.3V, FCT3xxx components provide a drop in replacement for FCT-T components without a speed compromise.

FCT-T Octals are TTL-compatible CMOS Logic components. By combining sub 0.5 micron CMOS technology with TTL output voltage levels, the advantages of the low static power dissipation of CMOS can be retained, while low dynamic power dissipation and lower noise levels of TTL can be achieved. This combination provides lower overall power dissipation than can be obtained from comparable bipolar, CMOS and biCMOS families.

FCT-T Balanced Drive

Balanced Drive Octal Logic (FCT2xxxT) is intended for general purpose applications requiring high speed, low power and low noise. Balanced Drive has series output resistors which reduce the drive current of the devices to +12/–15mA minimum at the Logic thresholds of 500mV and 2.4V respectively, helping to reduce transmission line noise, ringing, ground bounce, crosstalk, EMI and other noise related problems. Balanced Drive also will drive ±48mA (typical) at the 1.5V level, giving equal line driving currents and matching edge rates for both the Logic HIGH transition and Logic LOW transition. Balanced Drive is the family of choice for loads of less-than 200pF.

FCT-T High Drive

High Drive Octal Logic (FCTxxxT) is fully compatible with industry standard TTL Logic families. High Drive comes in a variety of speed grades, allowing an upgrade path to higher system performance unlike single speed grade families. Most high drive components have 64mA output drive capability, making them an excellent choice for heavy bus and back plane drivers.

FCT 3.3V

FCT 3.3V Octal Logic (FCT3xxx) is leading the industry's move to 3.3V. FCT 3.3V components are function and AC spec compatible with equivalent FCT-T components. These devices offer significant advantages in low power dissipation and speed over standard CMOS, bipolar, and biCMOS families. The 3.3V data sheets are located in the 3.3V section of this data book.

FAST is a trademark of National Semiconductor, Inc.

SECTION 6
OCTAL 5V PRODUCTS
TABLE OF CONTENTS

TTL-LEVEL WITH HIGH DRIVE OUTPUT (CONTINUED)

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

IDT29FCT52AT/BT/CT/DT
IDT29FCT2052AT/BT/CT
IDT29FCT53AT/BT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for 29FCT52/29FCT53T:**
  - A, B, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
- **Features for 29FCT2052T:**
  - A, B and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

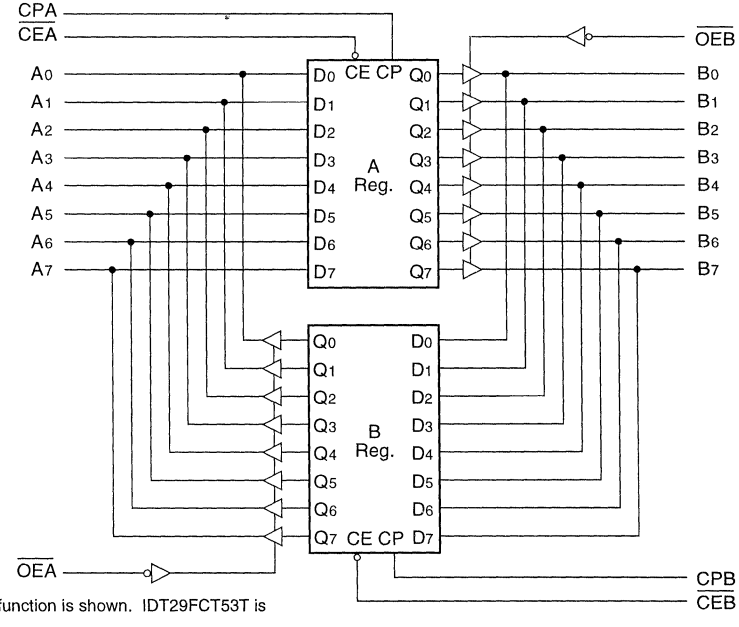
DESCRIPTION:

The IDT29FCT52AT/BT/CT/DT and IDT29FCT53AT/BT/CT are 8-bit registered transceivers built using an advanced dual metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52AT/BT/CT/DT and IDT29FCT2052AT/BT/CT are non-inverting options of the IDT29FCT53AT/BT/CT.

The IDT29FCT2052AT/BT/CT has balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The IDT29FCT2052T part is a plug-in replacement for IDT29FCT52T part.

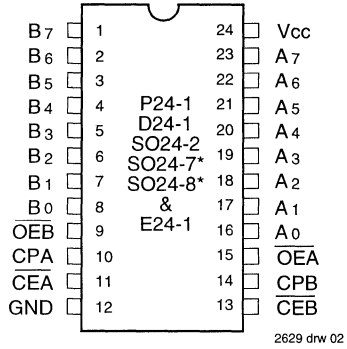
FUNCTIONAL BLOCK DIAGRAM(1)



NOTE:
1. IDT29FCT52T/IDT29FCT2052T function is shown. IDT29FCT53T is the inverting option.

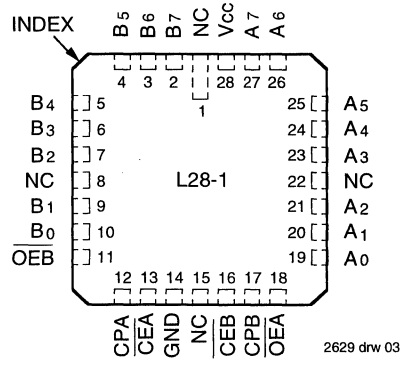
2629 drw 01

PIN CONFIGURATIONS



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

* For 29FCT52/29FCT2052AT/BT/CT only



LCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
A_{0-7}	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B_{0-7}	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B_{0-7} lines. When $\overline{OEB}$ is HIGH, the B_{0-7} outputs are in the high-impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A_{0-7} lines. When $\overline{OEA}$ is HIGH, the A_{0-7} outputs are in the high-impedance state.

2629 tbl 01

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REGISTER FUNCTION TABLE[1]
(Applies to A or B Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

2629 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition

OUTPUT CONTROL[1]

	Internal	Y-Outputs		
$\overline{OE}$	Q	52/2052	53	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

2629 tbl 03

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2529 lnk 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2640 lnk 05

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2629 tbl 06

OUTPUT DRIVE CHARACTERISTICS FOR 29FCT52T/29FCT53T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2629 tbl 07

OUTPUT DRIVE CHARACTERISTICS FOR 29FCT2052T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

2629 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ or $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND One Bit Toggling at fi = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4V	FCTxxxT	—	2.0	5.5	
			V_{IN} = GND	FCT2xxxT		1.1	4.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND Eight Bits Toggling at fi = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	3.8	7.3[5]	
				FCT2xxxT	—	1.5	4.0[5]	
			V_{IN} = 3.4V	FCTxxxT	—	6.0	16.3[5]	
			V_{IN} = GND	FCT2xxxT	—	3.8	13.0[5]	

2629 tbl 09

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	29FCT52AT/53AT 29FCT2052AT				29FCT52BT/53BT 29FCT2052BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CPA, CPB to An, Bn	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
tPZH tPZL	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
tSU	Set-up Time, HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time, HIGH or LOW An, Bn to CPA, CPB		2.0	—	2.0	—	1.5	—	1.5	—	ns
tSU	Set-up Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	3.0	—	3.0	—	ns
tH	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	Clock Pulse Width HIGH or LOW[3]		3.0	—	3.0	—	3.0	—	3.0	—	ns

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Symbol	Parameter	Condition[1]	29FCT52CT/53CT 29FCT2052CT				29FCT52DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CPA, CPB to An, Bn	CL = 50pF RL = 500Ω	2.0	6.3	2.0	7.3	2.0	4.5	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	7.0	1.5	8.0	1.5	5.6	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	6.5	1.5	7.5	1.5	4.3	—	—	ns
tSU	Set-up Time, HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	1.5	—	—	—	ns
tH	Hold Time, HIGH or LOW An, Bn to CPA, CPB		1.5	—	1.5	—	1.0	—	—	—	ns
tSU	Set-up Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	2.0	—	—	—	ns
tH	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	1.0	—	—	—	ns
tW	Clock Pulse Width HIGH or LOW[3]		3.0	—	3.0	—	3.0	—	—	—	ns

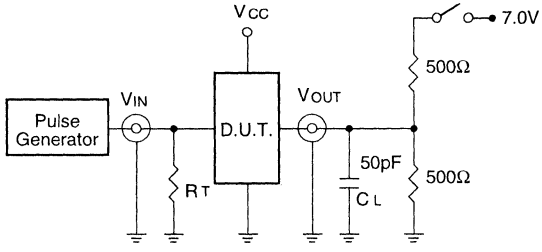
NOTES:
2629 tbl 11

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2629 drw 03

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

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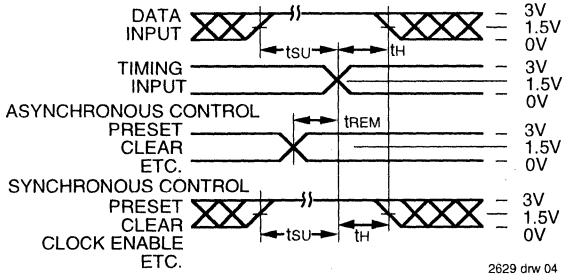
DEFINITIONS:

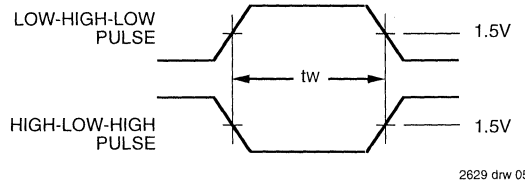
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



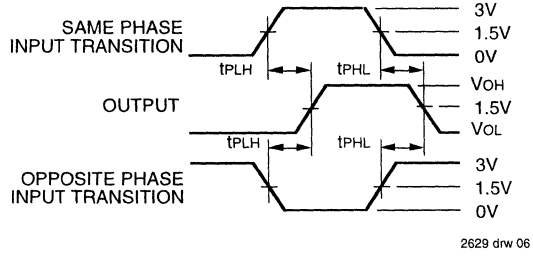
2629 drw 04

PULSE WIDTH

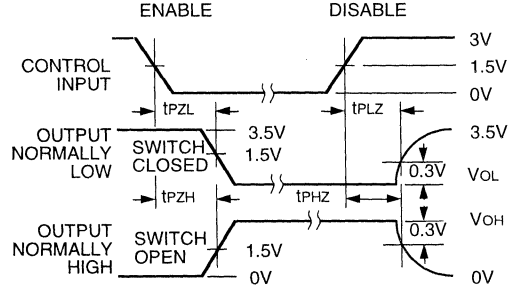


2629 drw 05

PROPAGATION DELAY



2629 drw 06

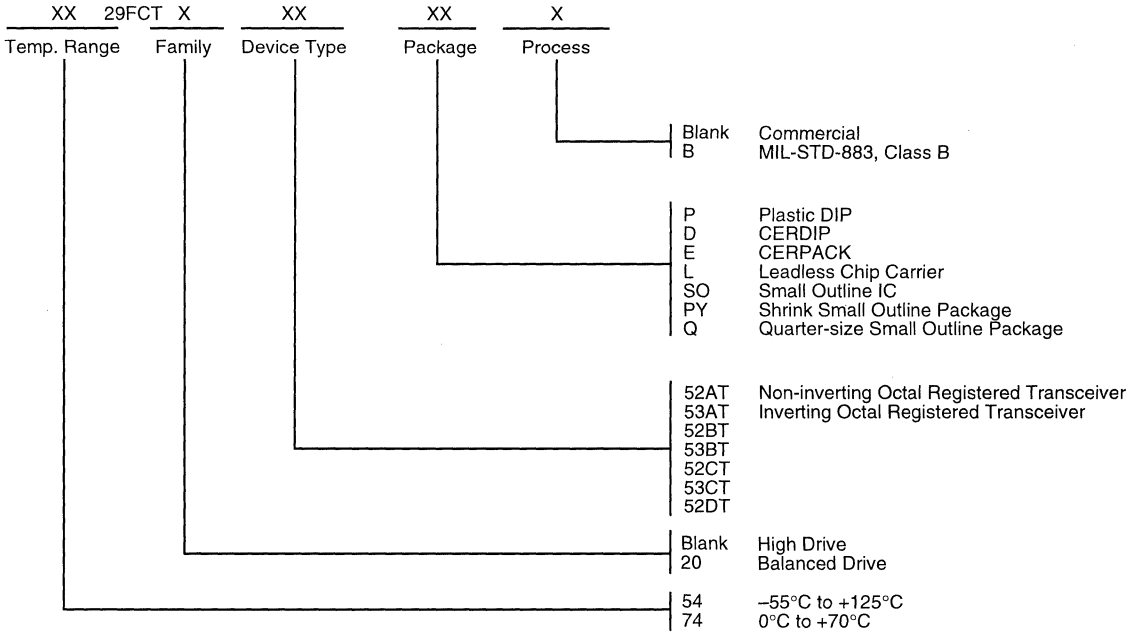


2629 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2629 drw 08

6

Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTERS

IDT29FCT520AT/BT/CT/DT
IDT29FCT521AT/BT/CT/DT

FEATURES:

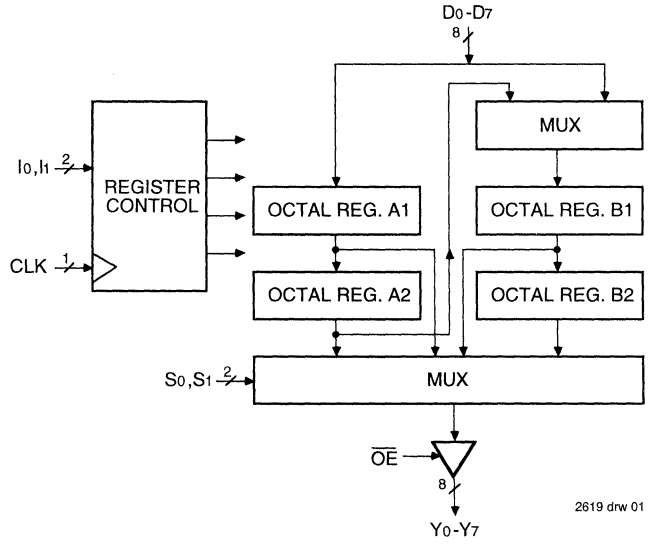
- A, B, C and D speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

DESCRIPTION:

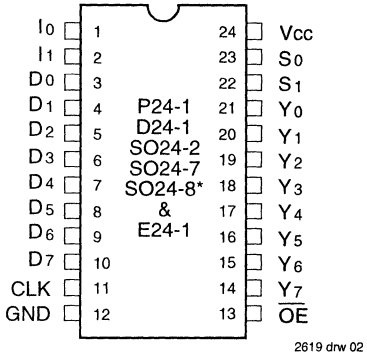
The IDT29FCT520AT/BT/CT/DT and IDT29FCT521AT/BT/CT/DT each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520AT/BT/CT/DT when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. In the IDT29FCT521AT/BT/CT/DT, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). This transfer also causes the first level to change. In either part I=3 is for hold.

FUNCTIONAL BLOCK DIAGRAM

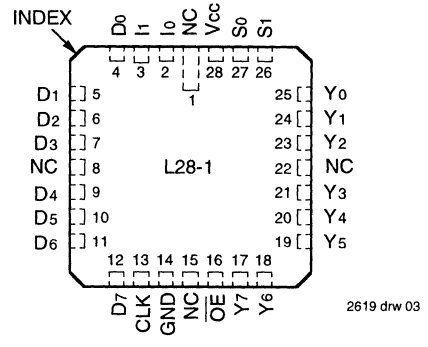


PIN CONFIGURATIONS



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

*FCT520 only



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
D_n	Register input Port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I_0, I_1	Instruction inputs. See Figure 1 and instruction Control Tables.
S_0, S_1	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
$\overline{OE}$	Output enable for 3-state output port.
Y_n	Register output port.

2619 tbl 01

REGISTER SELECTION

S_1	S_0	Register
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1

2619 tbl 02

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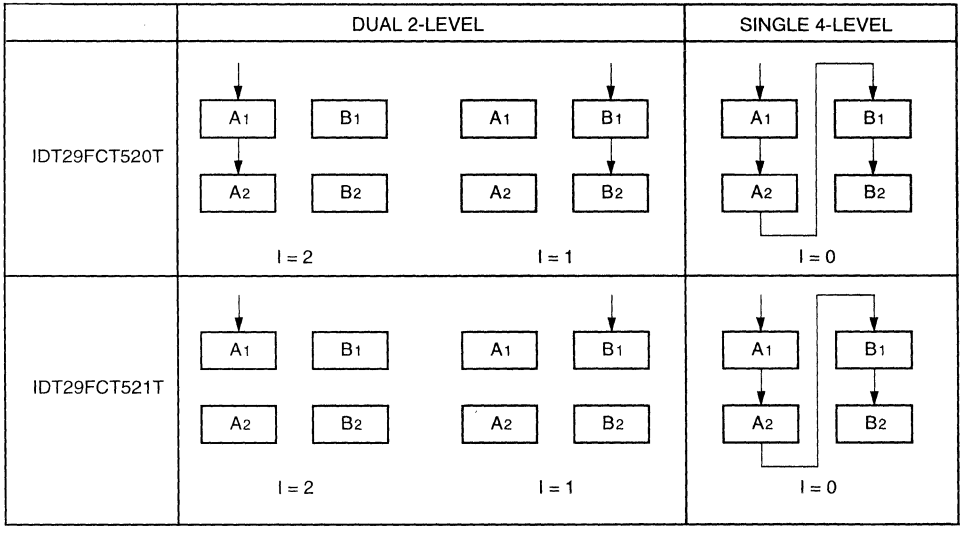

NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

2619 drw 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2619 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2619 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance(4)	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

NOTES: 2619 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current, TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.0	16.3[5]	

2619 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT520AT/521AT				FCT520BT/521BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PHL} t_{PLH}	Propagation Delay CLK to Yn	C_L = 50pF R_L = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	ns
t_{PHL} t_{PLH}	Propagation Delay S_0 or S_1 to Yn		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	ns
t_{SU}	Set-up Time, HIGH or LOW Dn to CLK		5.0	—	6.0	—	2.5	—	2.8	—	ns
t_H	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{SU}	Set-up Time, HIGH or LOW I_0 or I_1 to CLK		5.0	—	6.0	—	4.0	—	4.5	—	ns
t_H	Hold Time, HIGH or LOW I_0 or I_1 to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	ns
t_W	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	ns

2619 tbl 07

Symbol	Parameter	Condition[1]	FCT520CT/521CT				FCT520DT/521DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PHL} t_{PLH}	Propagation Delay CLK to Yn	C_L = 50pF R_L = 500Ω	2.0	6.0	2.0	7.0	2.0	5.2	—	—	ns
t_{PHL} t_{PLH}	Propagation Delay S_0 or S_1 to Yn		2.0	6.0	2.0	7.0	2.0	4.8	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW Dn to CLK		2.5	—	2.8	—	1.5	—	—	—	ns
t_H	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW I_0 or I_1 to CLK		4.0	—	4.5	—	2.0	—	—	—	ns
t_H	Hold Time, HIGH or LOW I_0 or I_1 to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	6.0	1.5	6.0	1.5	4.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	6.0	1.5	7.0	1.5	4.0	—	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		5.5	—	6.0	—	3.0	—	—	—	ns

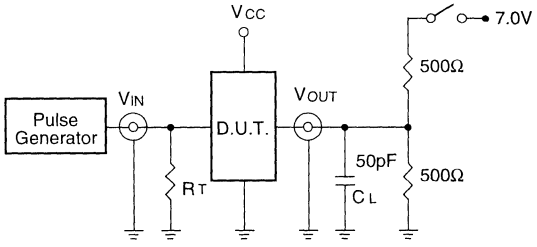
NOTES:

2619 tbl 08

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2619 drw 05

SWITCH POSITION

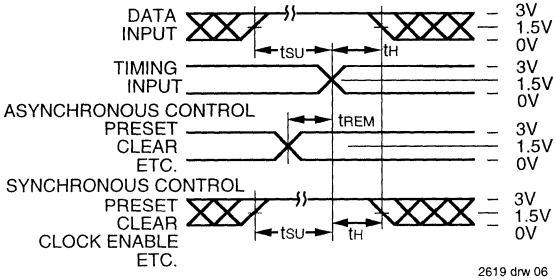
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2619 lnk 09

DEFINITIONS:

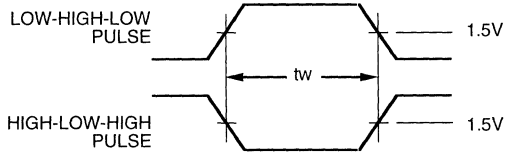
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



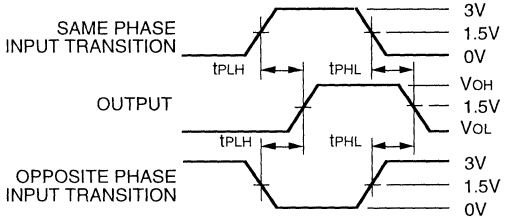
2619 drw 06

PULSE WIDTH



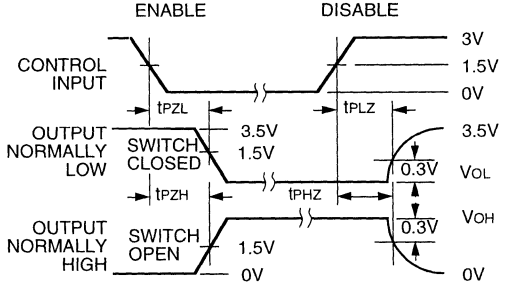
2619 drw 07

PROPAGATION DELAY



2619 drw 08

ENABLE AND DISABLE TIMES



2619 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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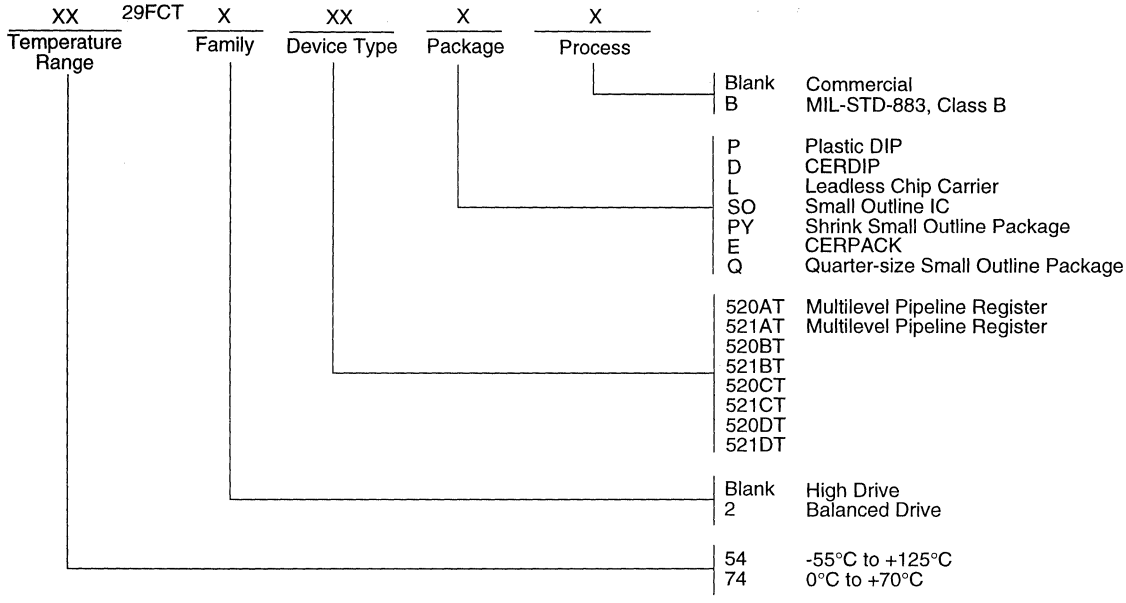
ORDERING INFORMATION



2619 drw 10

Integrated Device Technology, Inc.

FAST CMOS 1-OF-8 DECODER WITH ENABLE

IDT54/74FCT138T/AT/CT

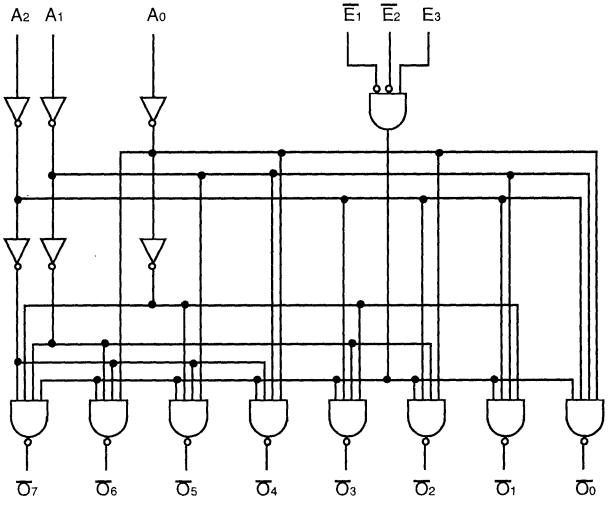
FEATURES:

- Std., A and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

DESCRIPTION:

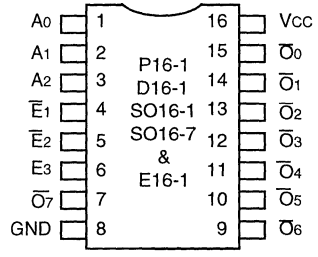
The IDT54/74FCT138T/AT/CT are 1-of-8 decoders built using an advanced dual metal CMOS technology. The IDT54/74FCT138T/AT/CT accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The IDT54/74FCT138T/AT/CT features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138T/AT/CT devices and one inverter.

FUNCTIONAL BLOCK DIAGRAM



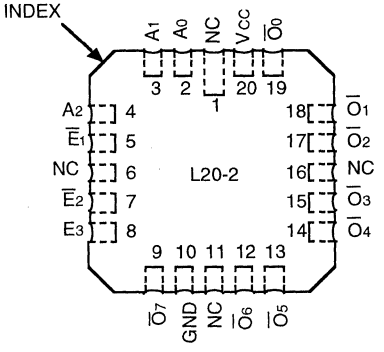
2570 drw 01

PIN CONFIGURATIONS



2570 drw 02

DIP/SOIC/QSOP/CERPACK
TOP VIEW



2570 drw 03

LCC
TOP VIEW

6

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$–$\overline{O}_7$	Outputs (Active LOW)

2570 tbl 01

FUNCTION TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

2570 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2570 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2570 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2570 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Toggle $\overline{E}_1$, $\overline{E}_2$ or E_3 50% Duty Cycle fo = 10MHz One Input and One Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	5.0	

NOTES:
2570 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_o = Output Frequency
   N_o = Number of Outputs at f_o
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

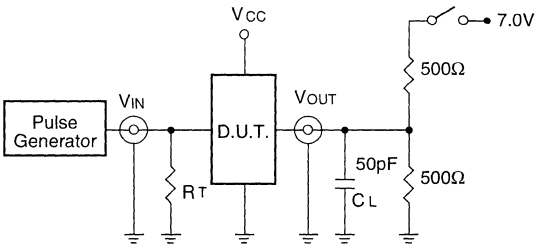
			FCT138T				FCT138AT				FCT138CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.8	1.5	7.8	1.5	5.1	1.5	6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	ns

NOTES:
2570 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2570 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

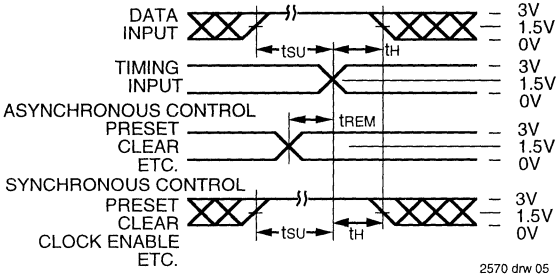
2570 tbl 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

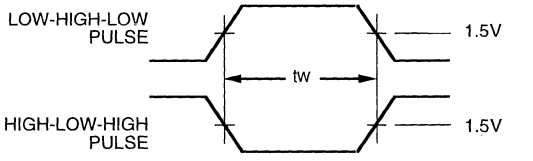
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



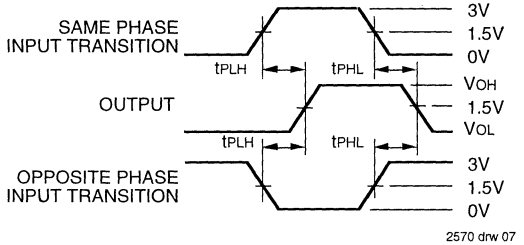
2570 drw 05

PULSE WIDTH



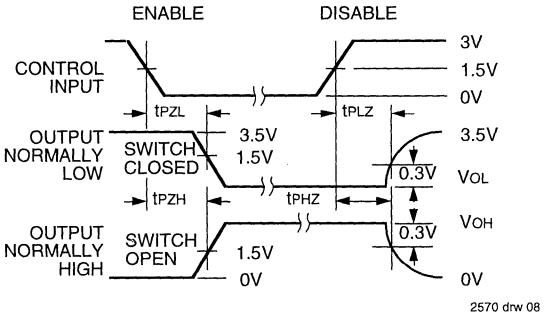
2570 drw 06

PROPAGATION DELAY



2570 drw 07

ENABLE AND DISABLE TIMES



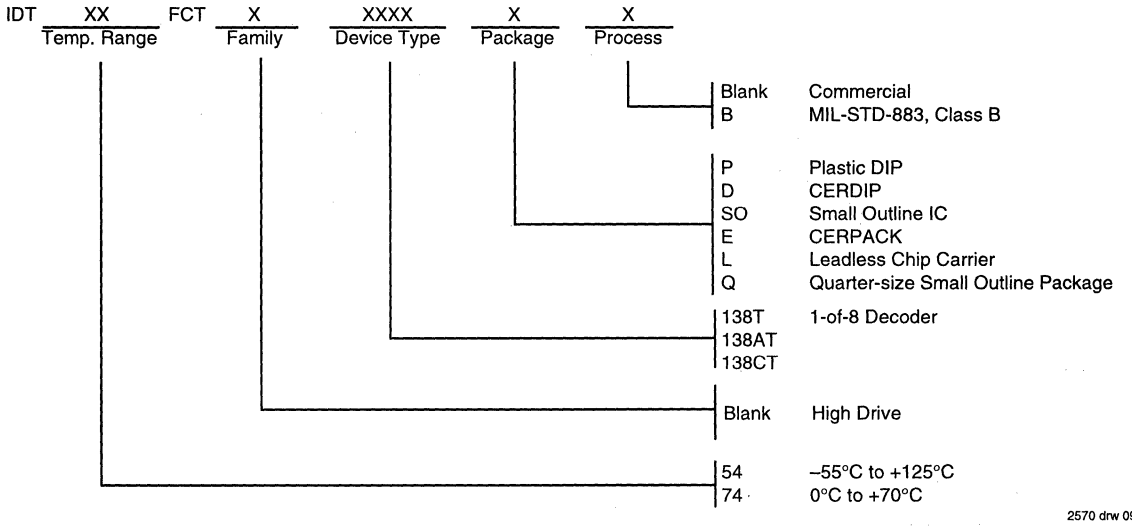
2570 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

6

ORDERING INFORMATION



2570 drw 09

Integrated Device Technology, Inc.

FAST CMOS DUAL 1-OF-4 DECODER WITH ENABLE

IDT54/74FCT139T/AT/CT

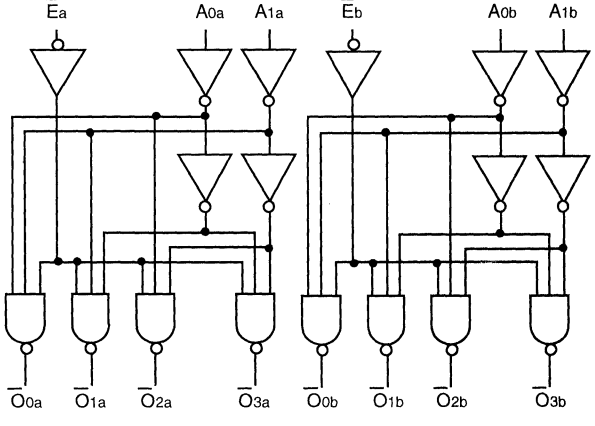
FEATURES:

- Std., A and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

DESCRIPTION:

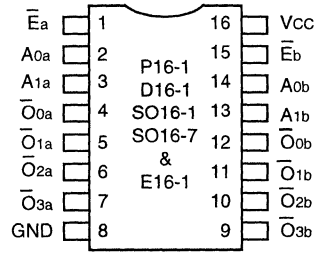
The IDT54/74FCT139T/AT/CT are dual 1-of-4 decoders built using an advanced dual metal CMOS technology. These devices have two independent decoders, each of which accept two binary weighted inputs (A_0-A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

FUNCTIONAL BLOCK DIAGRAM



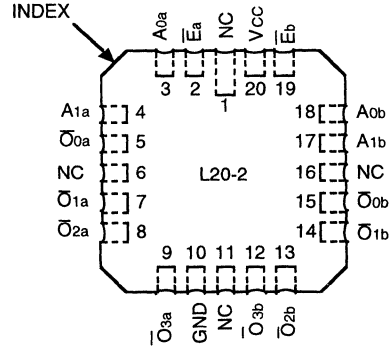
2566 drw 01

PIN CONFIGURATIONS



DIP/SOIC/QSOP/CERPACK
TOP VIEW

2566 drw 02



2566 drw 03

LCC
TOP VIEW

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2566 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

PIN DESCRIPTION

Pin Names	Description
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{O}_0$ - $\overline{O}_3$	Outputs (Active LOW)

2566 tbl 01

FUNCTION TABLE(1)

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

2566 tbl 02

NOTE:
1. H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2566 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2566 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_O = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	4.0	mA
		50% Duty Cycle One Input and One Output Toggling	V_{IN} = 3.4V V_{IN} = GND	—	1.8	5.0	
		V_{CC} = Max. Outputs Open f_O = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	7.0[5]	
		50% Duty Cycle One Input Toggling on Each Decoder Two Outputs Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	9.0[5]	

2566 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

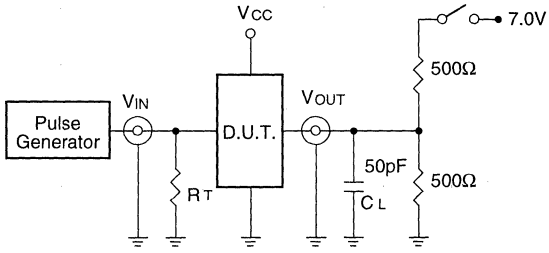
			FCT139T				FCT139AT				FCT139CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Parameter	Description	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.9	1.5	7.8	1.5	5.0	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_n$		1.5	8.0	1.5	9.0	1.5	5.5	1.5	7.2	1.5	4.8	1.5	5.8	ns

2566 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2566 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

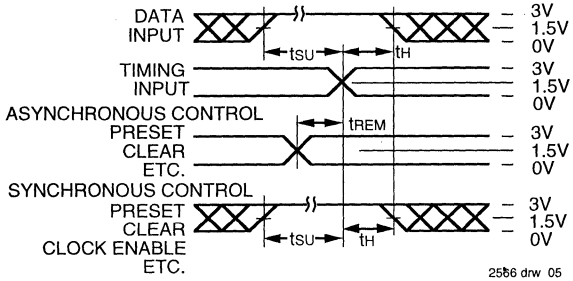
2566 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

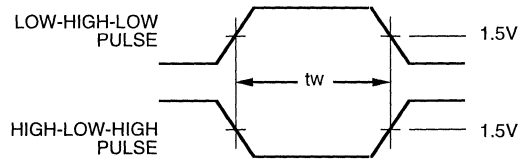
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



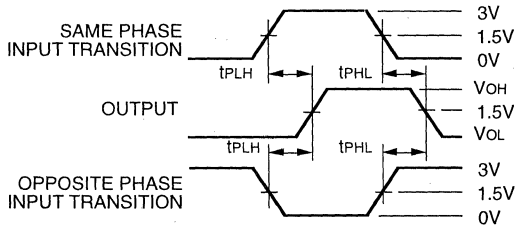
2566 drw 05

PULSE WIDTH



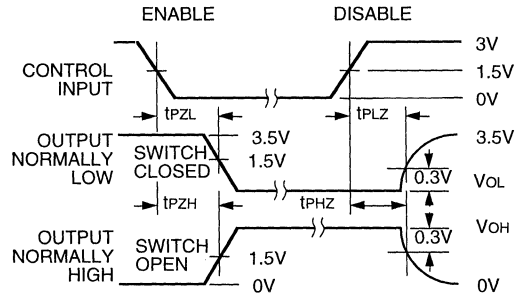
2566 drw 06

PROPAGATION DELAY



2566 drw 07

ENABLE AND DISABLE TIMES

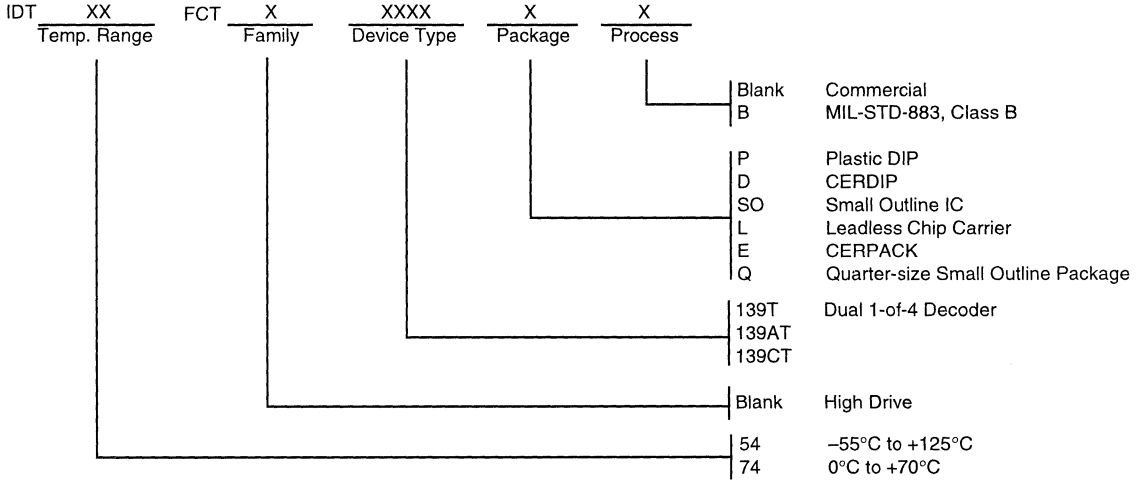


2566 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2566 drw 09

6

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT MULTIPLEXER

IDT54/74FCT151T/AT/CT

FEATURES:

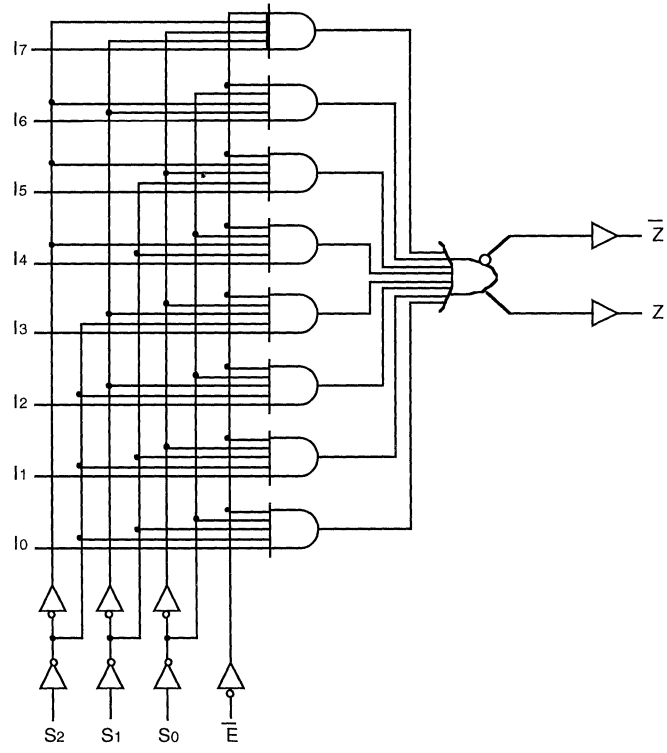
- Std., A, and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

DESCRIPTION:

The IDT54/74FCT151T/AT/CT are high-speed 8-input multiplexers built using an advanced dual metal CMOS technology. They select one bit of data from up to eight sources under the control of three select inputs. Both assertion and negation outputs are provided.

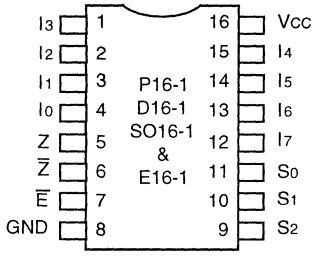
The IDT54/74FCT151T/AT/CT has a common Active-LOW enable ($\overline{E}$) input. When $\overline{E}$ is LOW, data from one of eight inputs is routed to the complementary outputs according to the 3-bit code applied to the Select (S_0-S_2) inputs. A common application of the 'FCT151 is data routing from one of eight sources.

FUNCTIONAL BLOCK DIAGRAM



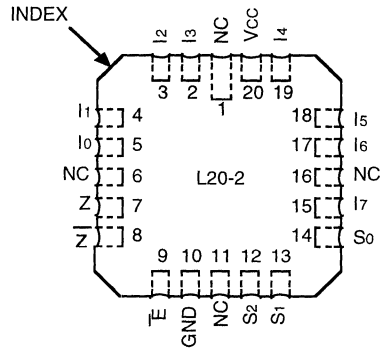
2635 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2635 drw 02



2635 drw 03

LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2635 lnk 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2635 lnk 02

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I_0 - I_7	Data Inputs
S_0 - S_2	Selects Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Data Output
$\overline{Z}$	Inverted Data Output

2635 tbl 03

FUNCTION TABLE(1)

Inputs				Outputs	
S_2	S_1	S_0	$\overline{E}$	Z	$\overline{Z}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I_0}$
L	L	H	L	I_1	$\overline{I_1}$
L	H	L	L	I_2	$\overline{I_2}$
L	H	H	L	I_3	$\overline{I_3}$
H	L	L	L	I_4	$\overline{I_4}$
H	L	H	L	I_5	$\overline{I_5}$
H	H	L	L	I_6	$\overline{I_6}$
H	H	H	L	I_7	$\overline{I_7}$

2635 tbl 04

NOTE:
1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't care, Z = High Impedance.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current[4]	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}			V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2635 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	QuiescentPower Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$= GND One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	3.5	7.5	

NOTES:

2635 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT151T				IDT54/74FCT151AT				IDT54/74FCT151CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay S_N to $\overline{Z}$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	10.0	1.5	6.6	1.5	7.4	1.5	5.6	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay S_N to Z		1.5	10.5	1.5	11.5	1.5	6.8	1.5	7.6	1.5	5.8	1.5	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		1.5	7.0	1.5	7.5	1.5	5.6	1.5	6.3	1.5	4.8	1.5	5.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z		1.5	9.5	1.5	11.0	1.5	5.8	1.5	6.6	1.5	5.0	1.5	5.7	ns
t_{PLH} t_{PHL}	Propagation Delay I_N to $\overline{Z}$		1.5	6.5	1.5	7.5	1.5	5.2	1.5	5.8	1.5	4.4	1.5	4.9	ns
t_{PLH} t_{PHL}	Propagation Delay I_N to Z		1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns

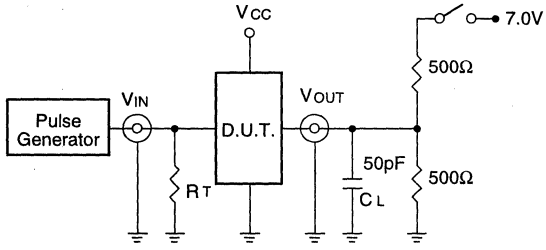
NOTES:

2635 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2635 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

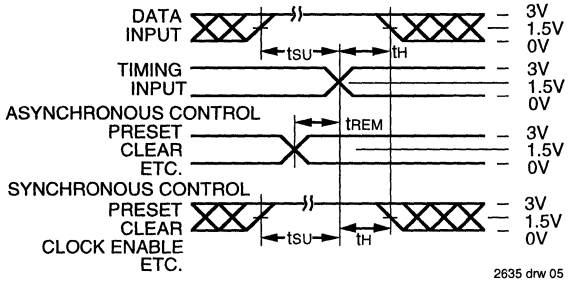
2635 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

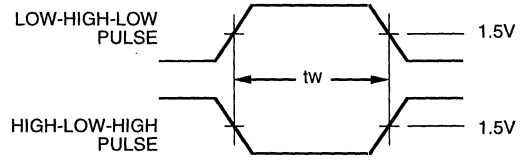
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



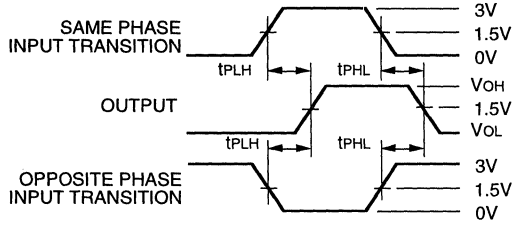
2635 drw 05

PULSE WIDTH



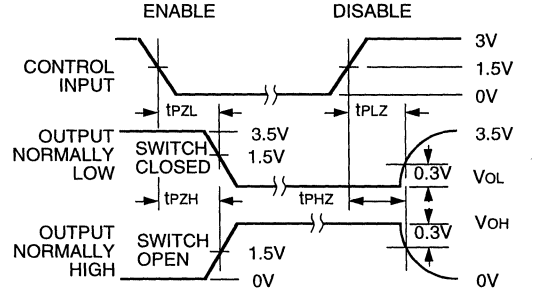
2635 drw 06

PROPAGATION DELAY



2635 drw 07

ENABLE AND DISABLE TIMES

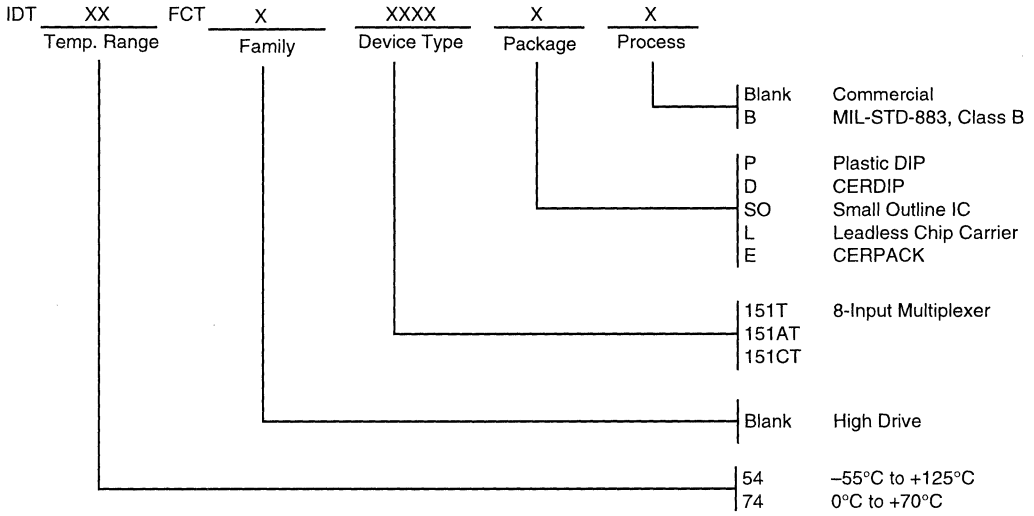


2635 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2635 drw 09

6

Integrated Device Technology, Inc.

FAST CMOS QUAD 2-INPUT MULTIPLEXER

IDT54/74FCT157T/AT/CT/DT
IDT54/74FCT257T/AT/CT/DT

FEATURES:

- Std., A, C and D speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

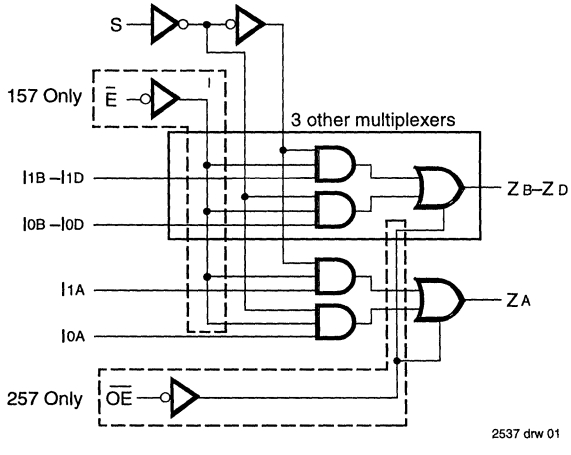
DESCRIPTION:

The IDT54/74FCT157T/AT/CT/DT and IDT54/74FCT257T/AT/CT/DT are high-speed quad 2-input multiplexers built using an advanced dual metal CMOS technology. Four bits of data from two sources can be selected using the common select input. The four buffered outputs present the selected data in the true (non-inverting) form.

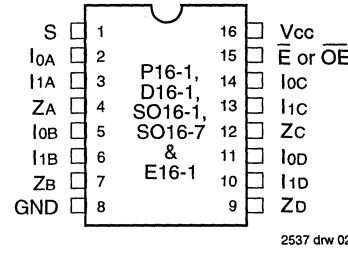
The IDT54/74FCT157T/AT/CT/DT has a common, active-LOW, enable input. When the enable input is not active, all four outputs are held LOW. A common application of 'FCT157T is to move data from two different groups of registers to a common bus. Another application is as a function generator. The 'FCT157T can generate any four of the 16 different functions of two variables with one variable common.

The IDT54/74FCT257T/AT/CT/DT has a common Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, all outputs are switched to a high-impedance state allowing the outputs to interface directly with bus-oriented systems.

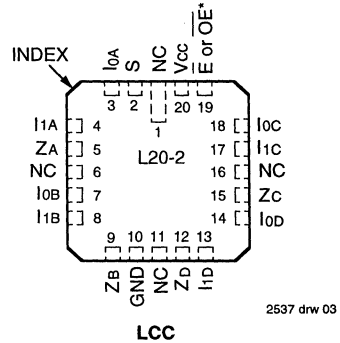
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOIC/QSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

* Ē for FCT157, $\overline{OE}$ for FCT257.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xDIR = x$\overline{OE}$= GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
		xDIR = x$\overline{OE}$ = GND One Bit Toggling fi = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
		xDIR = x$\overline{OE}$ = GND Sixteen Bits Toggling fi = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2540 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16646T/162646T				FCT16646AT/162646AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPZH tPZL	Output Enable Time xDIR or x$\overline{OE}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
tPHZ tPLZ	Output Disable Time xDIR or x$\overline{OE}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2540 tbl 09

Symbol	Parameter	Condition[1]	FCT16646CT/162646CT				FCT16646ET/162646ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	3.8	—	—	ns
tPZH tPZL	Output Enable Time xDIR or x$\overline{OE}$ to Bus		1.5	7.8	1.5	8.9	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time xDIR or x$\overline{OE}$ to Bus		1.5	6.3	1.5	7.7	1.5	4.0	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		1.5	6.2	1.5	7.0	1.5	4.2	—	—	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0.0	—	—	—	ns
tW	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

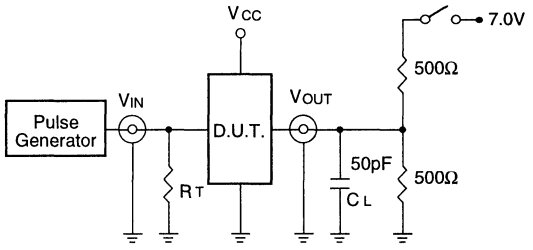
NOTES:

2540 tbl10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2556 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

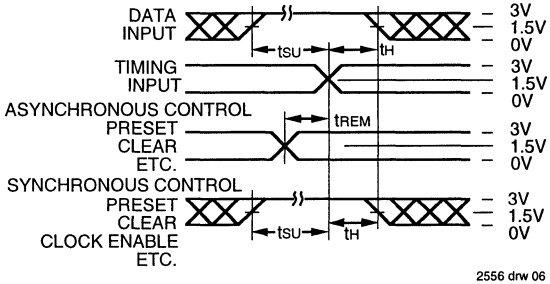
2556 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

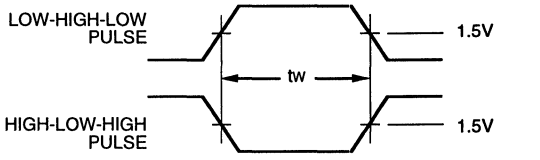
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



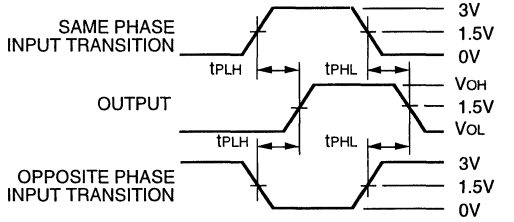
2556 drw 06

PULSE WIDTH



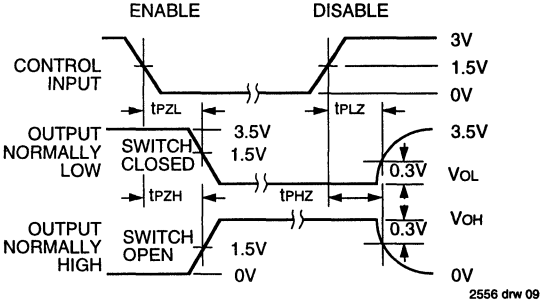
2556 drw 07

PROPAGATION DELAY



2556 drw 08

ENABLE AND DISABLE TIMES

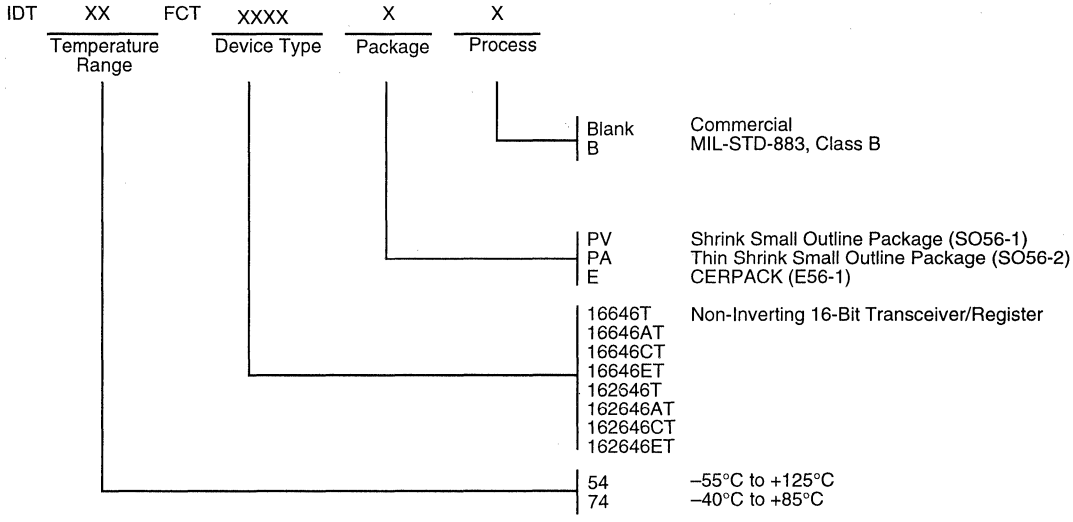


2556 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2540 drw 14

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BUS TRANSCEIVER/ REGISTERS

IDT54/74FCT16652T/AT/CT/ET
IDT54/74FCT162652T/AT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16652T/AT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162652T/AT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

The FCT16652T/AT/CT/ET and FCT162652T/AT/CT/ET 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit bus transceivers with 3-state D-type registers. For example, the xOEAB and $x\overline{OEBA}$ signals control the transceiver functions.

The xSAB and xSBA control pins are provided to select either real time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real time data. A LOW input level selects real-time data and a HIGH level selects stored data.

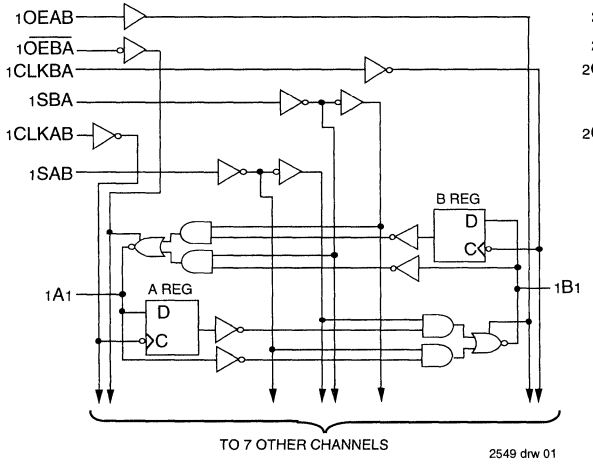
Data on the A or B data bus, or both, can be stored in the internal D-flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (xCLKAB or xCLKBA), regardless of the select or enable control pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16652T/AT/CT/ET are ideally suited for driving high capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

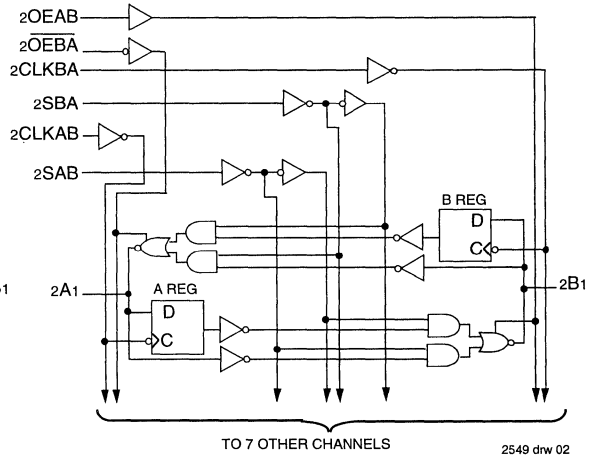
The FCT162652T/AT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162652T/AT/CT/ET are plug-in replacements for the FCT16652T/AT/CT/ET and ABT16652 for on-board bus interface applications.

5

FUNCTIONAL BLOCK DIAGRAM

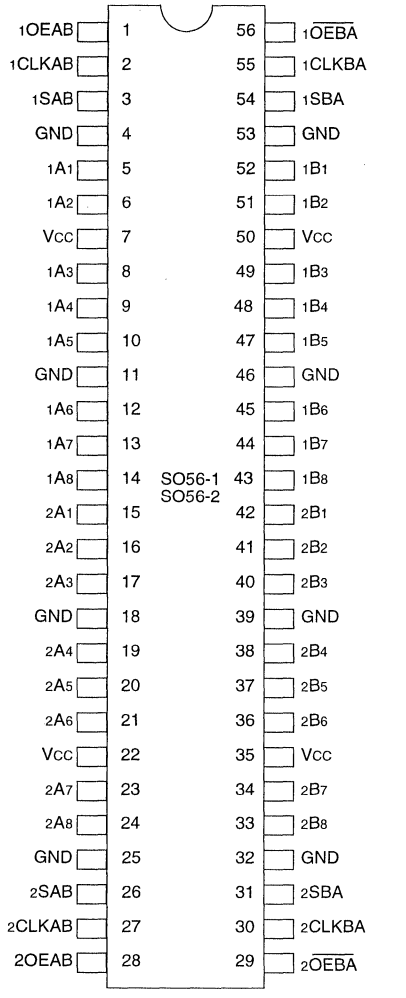


2549 drw 01



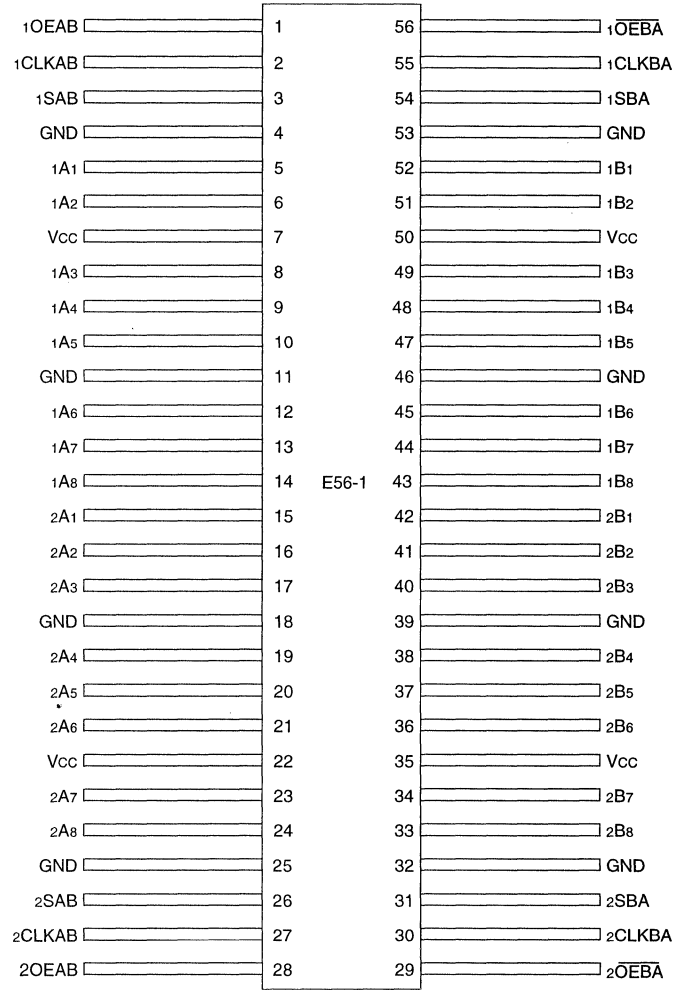
2549 drw 02

PIN CONFIGURATIONS



2549 drw 03

SSOP/ TSSOP TOP VIEW



2549 drw 04

CERPACK TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, x$\overline{OEBA}$	Output Enable Inputs

2549 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE:
1. This parameter is measured at characterization but not tested.

2549 lnk 02

FUNCTION TABLE[2]

Inputs						Data I/O[1]		Operation or Function
xOEAB	x$\overline{OEBA}$	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[1]	Store A, Hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified[1]	Input	Hold A, Store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

NOTES:
1. The data output functions may be enabled or disabled by various signals at the xOEAB or x$\overline{OEBA}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered to load both registers.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition

2549 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

2549 tbl 04

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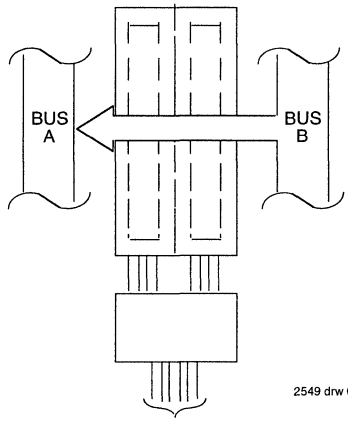
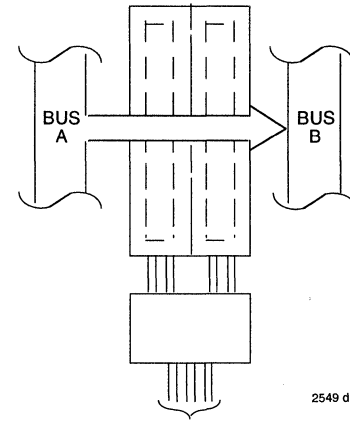


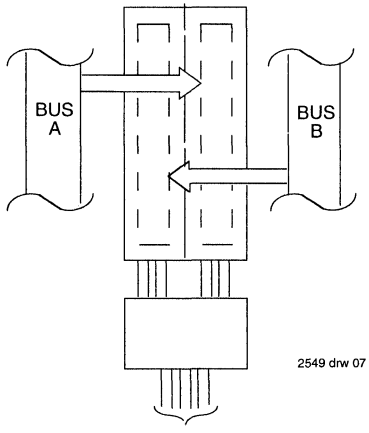
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



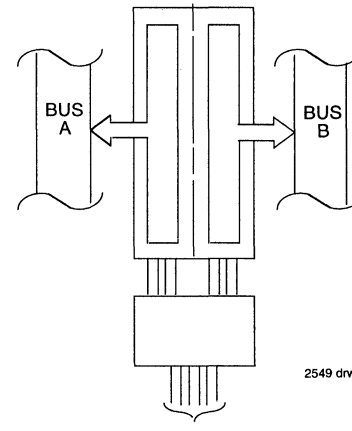
xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	H	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xOEAB	$\overline{xOEBA}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA TO A AND/OR B

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2549 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16652T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2549 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162652T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2549 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xOEAB = x$\overline{OEBA}$=GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
		xOEAB = x$\overline{OEBA}$=GND One Bit Toggling fi = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
		xOEAB = x$\overline{OEBA}$=GND Sixteen Bits Toggling fi = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2549 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16652T/162652T				FCT16652AT/162652AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPZH tPZL	Output Enable Time xOEAB or $x\overline{OEBA}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
tPHZ tPLZ	Output Disable Time xOEAB or $x\overline{OEBA}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2549 tbl 09

Symbol	Parameter	Condition[1]	FCT16652CT/162652CT				FCT16652ET/162652ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	3.8	—	—	ns
tPZH tPZL	Output Enable Time xOEAB or $x\overline{OEBA}$ to Bus		1.5	7.8	1.5	8.9	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time xOEAB or $x\overline{OEBA}$ to Bus		1.5	6.3	1.5	7.7	1.5	4.0	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	3.8	—	—	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		1.5	6.2	1.5	7.0	1.5	4.2	—	—	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	0.0	—	—	—	ns
tW	Clock Pulse Width HIGH or LOW		5.0	—	5.0	—	3.0[4]	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

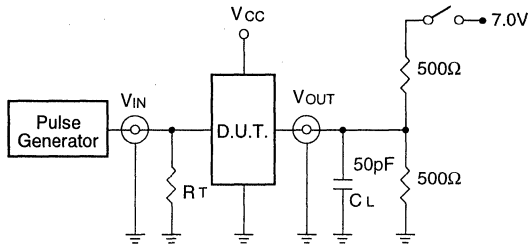
NOTES:

2549 tbl10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2549 drw 05

SWITCH POSITION

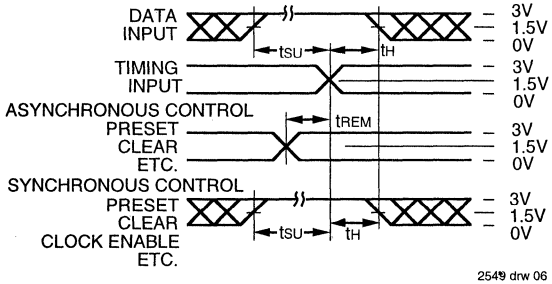
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2549 lnk 10

DEFINITIONS:

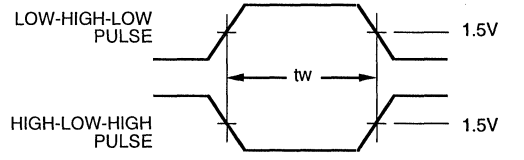
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



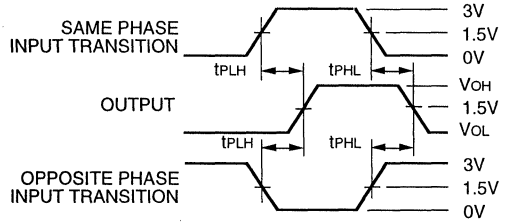
2549 drw 06

PULSE WIDTH



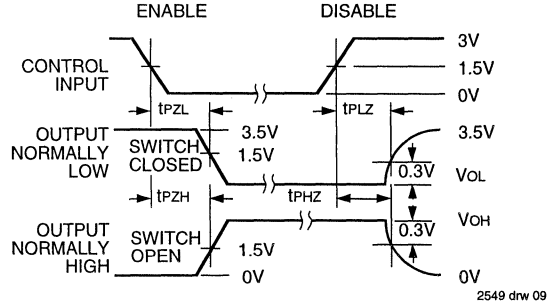
2549 drw 07

PROPAGATION DELAY



2549 drw 08

ENABLE AND DISABLE TIMES

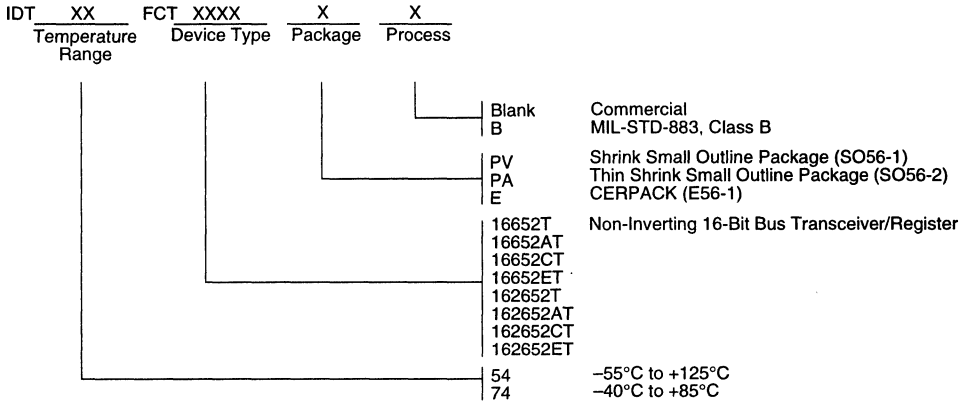


2549 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2549 drw 14

5

Integrated Device Technology, Inc.

FAST CMOS 18-BIT R/W BUFFER

IDT54/74FCT162701T/AT

FEATURES:

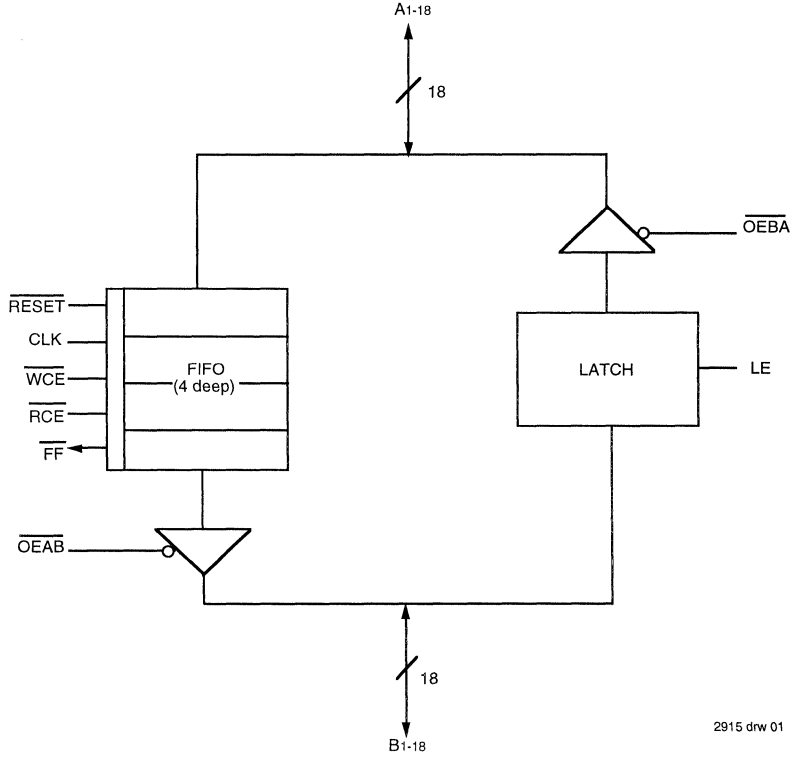
- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- **Low input and output leakage ≤1μA (max.)**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- Ideal for new generation x86 write-back cache solutions
- Suitable for modular x86 architectures
- Four deep write FIFO
- Latch in read path
- Synchronous FIFO reset

DESCRIPTION:

The FCT162701T/AT is an 18-bit Read/Write buffer with a four deep FIFO and a read-back latch. It can be used as a read/write buffer between a CPU and memory or to interface a high-speed bus and a slow peripheral. The A-to-B (write) path has a four deep FIFO for pipelined operations. The FIFO can be reset and a FIFO full condition is indicated by the full flag ($\overline{FF}$). The B-to-A (read) path has a latch. A HIGH on LE, allows data to flow transparently from B-to-A. A LOW on LE allows the data to be latched on the falling edge of LE.

The FCT162701T/AT has a balanced output drive with series termination. This provides low ground bounce, minimal undershoot and controlled output edge rates.

FUNCTIONAL BLOCK DIAGRAM



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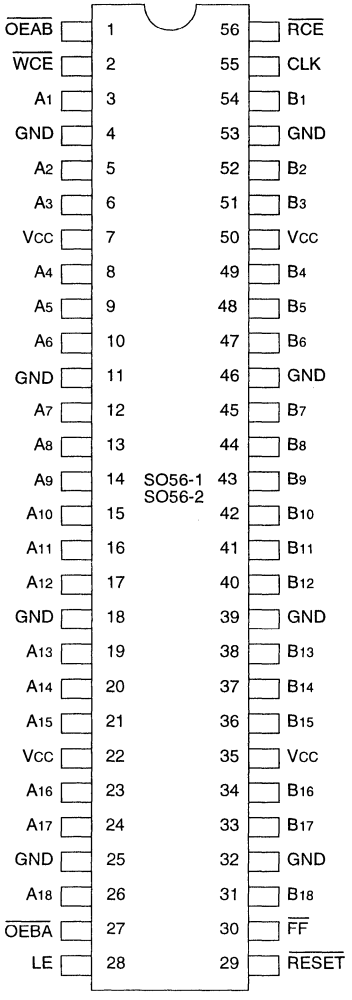
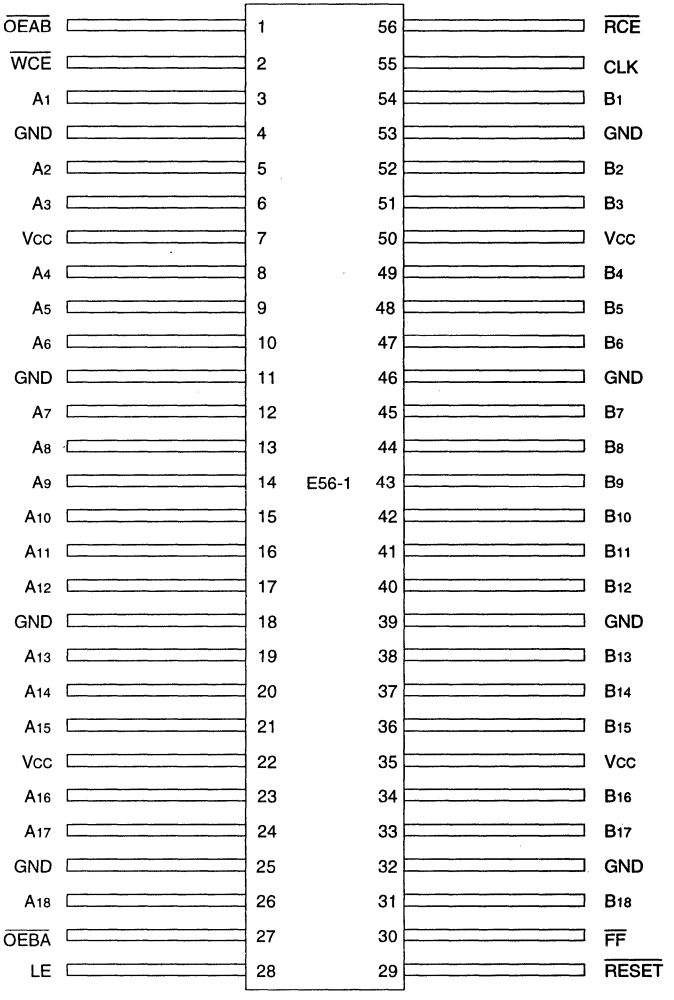
PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2915 drw 02



CERPACK
TOP VIEW

2915 drw 03

5

PIN DESCRIPTION

Pin Names	I/O	Description
A_{1-18}	I/O	18 bit I/O port.
B_{1-18}	I/O	18 bit I/O port.
CLK	I	Clock for write path FIFO. Clocks data into FIFO when $\overline{WCE}$ is low, clocks data out of FIFO when $\overline{RCE}$ is low. When FIFO is full all further writes to the FIFO are inhibited. When FIFO is empty all reads from the FIFO are inhibited. CLK also resets the FIFO when $\overline{RESET}$ is low.
$\overline{WCE}$	I	Enable pin for FIFO input clock.
$\overline{RCE}$	I	Enable pin for FIFO output clock.
$\overline{FF}$	O	Write path FIFO full flag. Goes low when FIFO is full.
$\overline{RESET}$	I	Synchronous FIFO reset - when low CLK resets the FIFO. The FIFO pointers are initialized to the "empty" condition and FIFO output is forced high (all ones). The FIFO full flag ($\overline{FF}$) will be high immediately after reset.
$\overline{OEAB}$	I	Output Enable pin for B port.
$\overline{OEBA}$	I	Output Enable pin for A port.
LE	I	Read path latch enable pin. When high, data flows transparently from B port to A port, B data is latched on the falling edge of LE.

2915 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2915 lnk 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2915 lnk 03

NOTE:
1. This parameter is measured at characterization but not tested.

FUNCTIONAL DESCRIPTION:

This device is useful as a read/write buffer for modular high end designs. It provides multi-level buffering in the write path and single deep buffering in the read path, and is suited to write back cache implementation. The read path provides a transparent latch.

The four deep FIFO uses one clock with two clock enable pins, $\overline{WCE}$ and $\overline{RCE}$ to clock data in and out. The FIFO has an external full flag which goes LOW when the FIFO is full. Internal read and write pointers keep track of the words stored in the FIFO. A write attempt to a full FIFO is ignored. An attempt to read from an empty FIFO will have no effect and the last read data remains at the output of the FIFO. The FIFO may be reset by the synchronous $\overline{RESET}$ input. This resets the read and write pointers to the original "empty" condition and also sets all B outputs = 1. Simultaneous read and write attempts (clock data into FIFO as well as clock data out of FIFO) are possible except on FIFO empty and full boundaries. When the FIFO is empty, and a simultaneous read and write is attempted, the read is ignored while the write is executed. If the same is attempted when the FIFO is full, the write is ignored while the read is executed. Normal operation of the four deep FIFO in the write path is independent of the read path operation.

Power, ground and data pin positions on the FCT162701T match those on the FCT16501T/162501T, allowing an easy upgrade.

APPLICATIONS: 486 INTERFACE

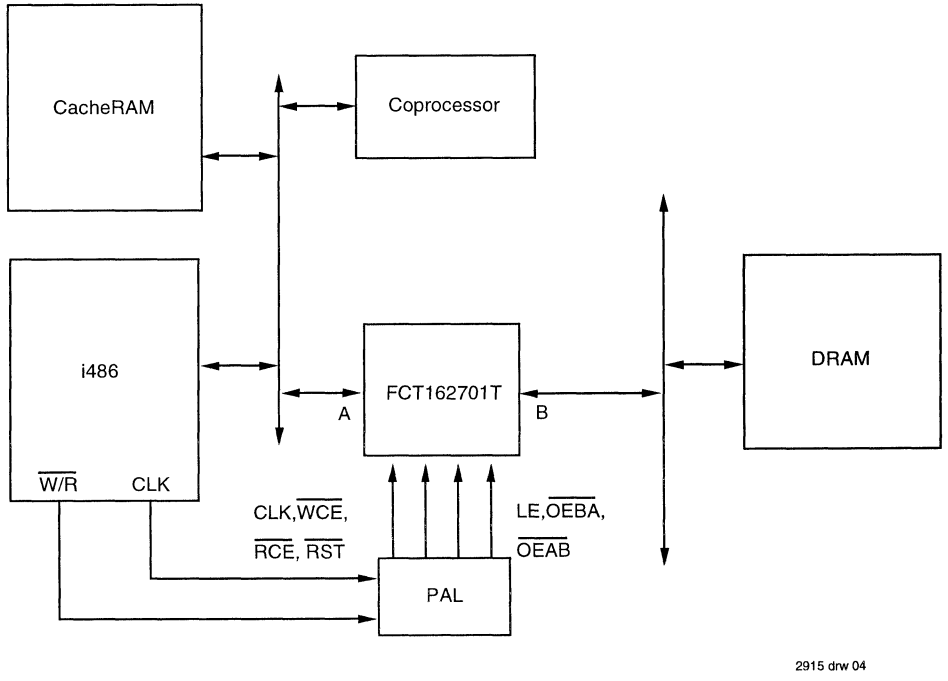


Figure 1. FCT162701T Application Example

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2915 lnk 04

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2915 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	1.5	mA
I_{CCD} (CLK)	Dynamic Power Supply Current due to clock switching[4]	V_{CC} = Max. Outputs Open	CLK Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	180	240	µA/ MHz
I_{CCD} (O/P)	Dynamic Power Supply Current due to output switching[4]		One Bit Toggling 50% Duty Cycle		—	80	120	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle		V_{IN} = V_{CC} V_{IN} = GND	—	1.8	2.9[5]	mA
		$\overline{OEAB}$ = GND; $\overline{OEBA}$ = V_{CC} LE = $\overline{WCE}$ = $\overline{RCE}$ = GND $\overline{RESET}$ = V_{CC} All Inputs Low		V_{IN} = 3.4V V_{IN} = GND	—	2.1	3.7[5]	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle		V_{IN} = V_{CC} V_{IN} = GND	—	2.2	3.5	
		$\overline{OEAB}$ = GND; $\overline{OEBA}$ = V_{CC} LE = $\overline{WCE}$ = $\overline{RCE}$ = GND $\overline{RESET}$ = V_{CC} One Bit Toggling at fo = 5MHz 50% Duty Cycle		V_{IN} = 3.4V V_{IN} = GND	—	2.7	5.0	

2915 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN}) = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD (CLK)} \times f_{CP} + I_{CCD (O/P)} \times f_O N_O$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   fo = Output Frequency
   N_O = Number of Outputs at fo

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

	Parameter	Test Conditions[1]	FCT162701T		FCT162701AT		
			Min.[2]	Max.[2]	Min.[2]	Max.[2]	Unit
PROPAGATION DELAYS							
1	B_{1-18} to A_{1-18}	Read path/latch	1.5	6.5	1.5	5.5	ns
2	LE (Low to Hi) to A_{1-18}	Read path/latch	1.5	5.7	1.5	4.7	ns
3	CLK to $\overline{FF}$	Write path	2	7.0	2	6.0	ns
4	CLK to B_{1-18}	Write path	1	6.0	1	5.2	ns
SETUP & HOLD TIMES[3]							
5	A_{1-18} to CLK (Low to Hi) Setup	Write path	2.5	—	2.5	—	ns
6	A_{1-18} to CLK (Low to Hi) Hold	Write path	0	—	0	—	ns
7	B_{1-18} to LE (Hi to Low) Setup	Read path/latch	3	—	3	—	ns
8	B_{1-18} to LE (Hi to Low) Hold	Read path/latch	0	—	0	—	ns
9	$\overline{WCE}$, $\overline{RCE}$ (Low) to CLK Setup	Write path	3	—	3	—	ns
10	$\overline{WCE}$, $\overline{RCE}$ (Low) to CLK Hold	Write path	0	—	0	—	ns
11	$\overline{RESET}$ (Low) to CLK Setup	Write path	3	—	3	—	ns
12	$\overline{RESET}$ (Low) to CLK Hold	Write path	0	—	0	—	ns
ENABLE & DISABLE TIMES[3]							
13	$\overline{OEBA}$ Low to A_{1-18} Enable	Write path	1.5	7.0	1.5	6.0	ns
14	$\overline{OEBA}$ High to A_{1-18} Disable	Write path	1.5	6.0	1.5	5.0	ns
15	$\overline{OEAB}$ Low to B_{1-18} Enable	Read path	1.5	7.0	1.5	6.0	ns
16	$\overline{OEAB}$ High to B_{1-18} Disable	Read path	1.5	6.0	1.5	5.0	ns
MINIMUM PULSE WIDTHS							
17	CLK HIGH or LOW Pulse Width	Write path	3.0	—	3.0	—	ns
18	LE HIGH Pulse Width	Read path/latch	3.0	—	3.0	—	ns

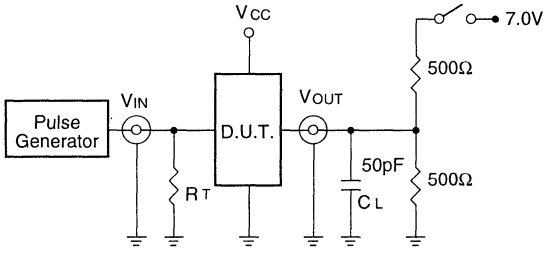
NOTES:

2915 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2915 drw 04

SWITCH POSITION

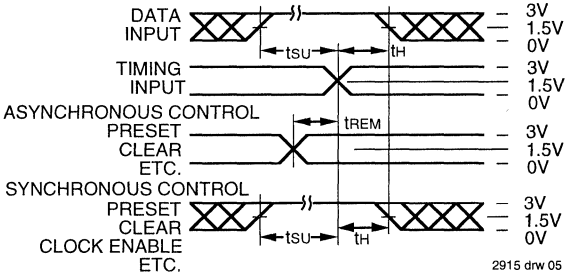
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2915 lnk 07

DEFINITIONS:

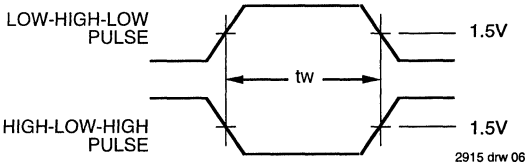
CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



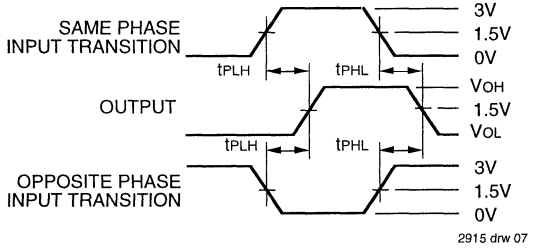
2915 drw 05

PULSE WIDTH



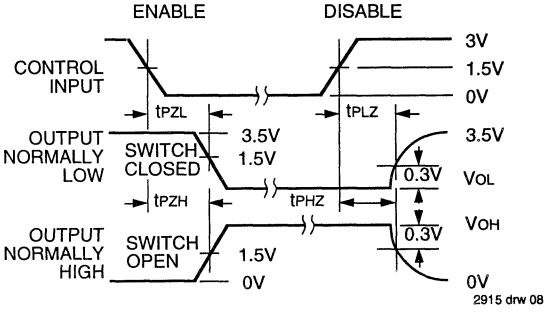
2915 drw 06

PROPAGATION DELAY



2915 drw 07

ENABLE AND DISABLE TIMES



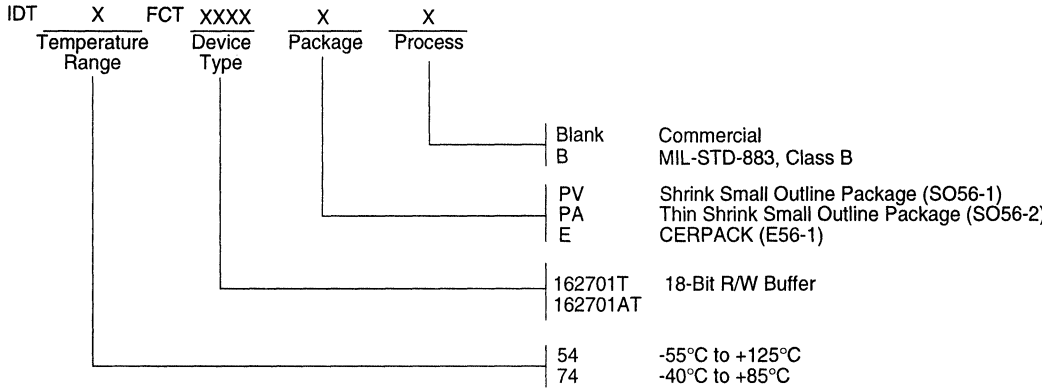
2915 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

5

ORDERING INFORMATION



2915 drw 09

Integrated Device Technology, Inc.

FAST CMOS 18-BIT REGISTER

IDT54/74FCT16823AT/BT/CT/ET
IDT54/74FCT162823AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16823AT/BT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162823AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

DESCRIPTION:

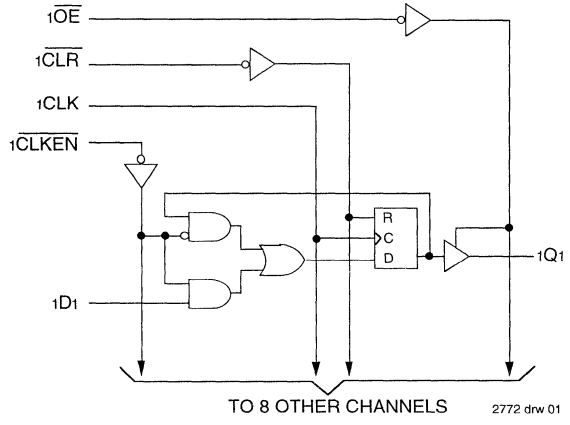
The FCT16823AT/BT/CT/ET and FCT162823AT/BT/CT/ET 18-bit bus interface registers are built using advanced, dual metal CMOS technology. These high-speed, low-power registers with clock enable (x$\overline{CLKEN}$) and clear (x$\overline{CLR}$) controls are ideal for parity bus interfacing in high-performance synchronous systems. The control inputs are organized to operate the device as two 9-bit registers or one 18-bit register. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

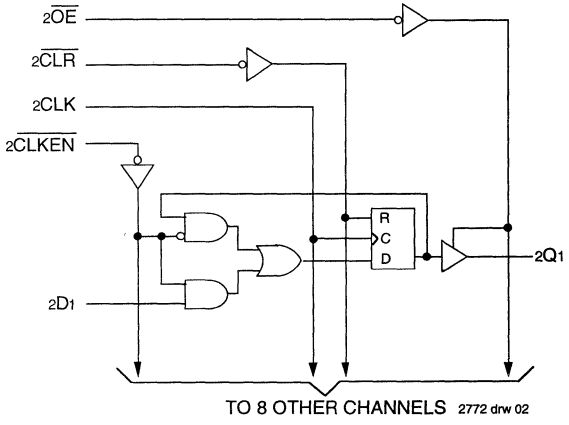
The FCT16823AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162823AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times – reducing the need for external series terminating resistors. The FCT162823AT/BT/CT/ET are plug-in replacements for the FCT16823AT/BT/CT/ET and ABT16823 for on-board interface applications.

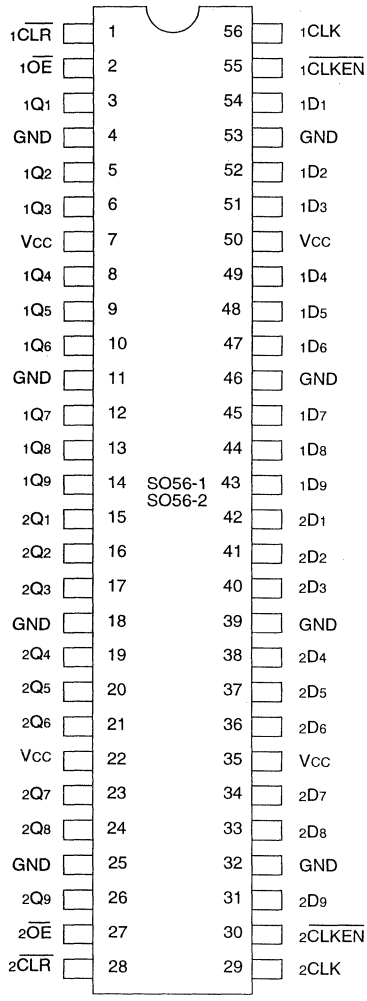
5

FUNCTIONAL BLOCK DIAGRAM



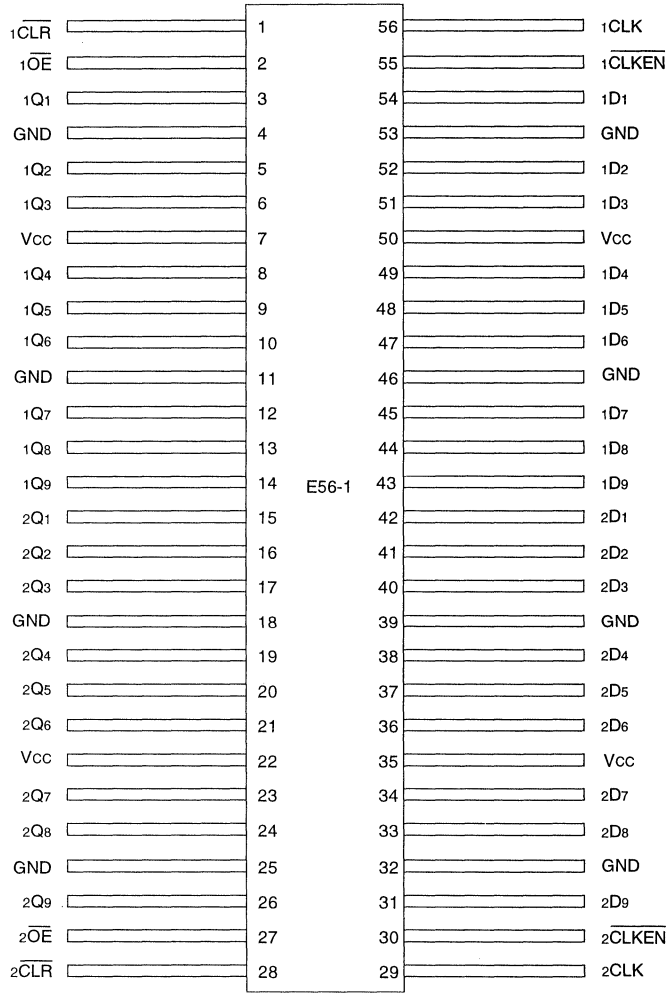


PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2772 drw 03



CERPACK
TOP VIEW

2772 drw 04

PIN DESCRIPTION

Pin Names	Description
xDx	Data inputs
xCLK	Clock Inputs
$x\overline{CLKEN}$	Clock Enable Inputs (Active LOW)
$x\overline{CLR}$	Asynchronous clear Inputs (Active LOW)
$x\overline{OE}$	Output Enable Inputs (Active LOW)
xQx	3-State Outputs

2772 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2772 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

FUNCTION TABLE(1)

Inputs					Outputs	
$x\overline{OE}$	$x\overline{CLR}$	$x\overline{CLKEN}$	xCLK	xDx	xQx	Function
H	X	X	X	X	Z	High Z
L	L	X	X	X	L	Clear
L	H	H	X	X	Q(2)	Hold
H	H	L	↑	L	Z	Load
H	H	L	↑	H	Z	
L	H	L	↑	L	L	
L	H	L	↑	H	H	

2772 tbl 02

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before indicated steady-state input conditions were established.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2772 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

5

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2772 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16823T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2772 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162823T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2772 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = $x\overline{CLKEN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	2.7	mA
		$x\overline{OE}$ = $x\overline{CLKEN}$ = GND at fi = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.2	7.1[5]	
		$x\overline{OE}$ = $x\overline{CLKEN}$ = GND at fi = 2.5MHz 50% Duty Cycle Eighteen Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	9.2	22.1[5]	

2772 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16823AT/162823AT				FCT16823BT/162823BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	
t_{PHL}	Propagation Delay x$\overline{CLR}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	C_L = 5pF[5] R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	
t_{SU}	Set-up Time HIGH or LOW xDx to xCLK	C_L = 50pF R_L = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW xDx to xCLK		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		4.0	—	4.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		2.0	—	2.0	—	0	—	0	—	ns
t_W	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	ns
t_W	x$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	ns
t_{REM}	Recovery Time x$\overline{CLR}$ to xCLK		6.0	—	7.0	—	6.0	—	6.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2772 tbl 09

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16823CT/162823CT				FCT16823ET/162823ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQx	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	7.0	1.5	4.4	—	—	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	8.0	—	—	
t_{PHL}	Propagation Delay x$\overline{CLR}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	8.5	1.5	4.4	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	4.4	—	—	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	9.0	—	—	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	C_L = 5pF[5] R_L = 500Ω	1.5	6.2	1.5	6.2	1.5	3.6	—	—	ns
		C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	6.5	1.5	3.6	—	—	
t_{SU}	Set-up Time HIGH or LOW xDx to xCLK	C_L = 50pF R_L = 500Ω	3.0	—	3.0	—	1.5	—	—	—	ns
t_H	Hold Time HIGH or LOW xDx to xCLK		1.5	—	1.5	—	0.0	—	—	—	ns
t_{SU}	Set-up Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		3.0	—	3.0	—	2.5	—	—	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		0	—	0	—	0.0	—	—	—	ns
t_W	xCLK Pulse Width HIGH or LOW		6.0	—	6.0	—	3.0[4]	—	—	—	ns
t_W	x$\overline{CLR}$ Pulse Width LOW		6.0	—	6.0	—	3.0[4]	—	—	—	ns
t_{REM}	Recovery Time x$\overline{CLR}$ to xCLK		6.0	—	6.0	—	3.0	—	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

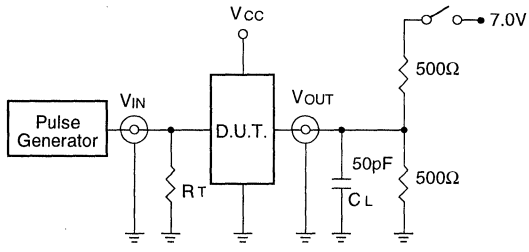
NOTES:
2772 tbl 10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2772 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

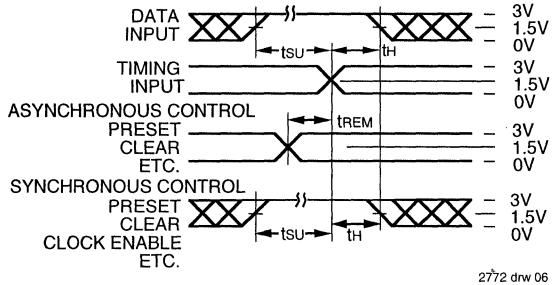
2772 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

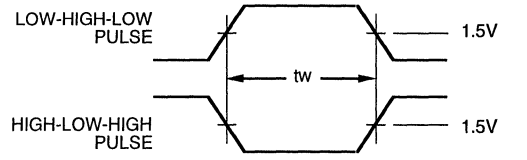
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



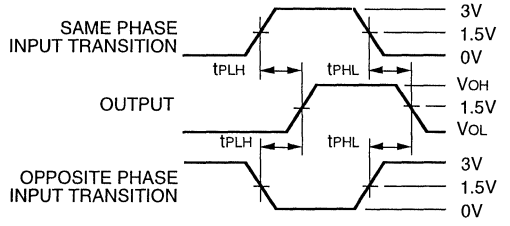
2772 drw 06

PULSE WIDTH



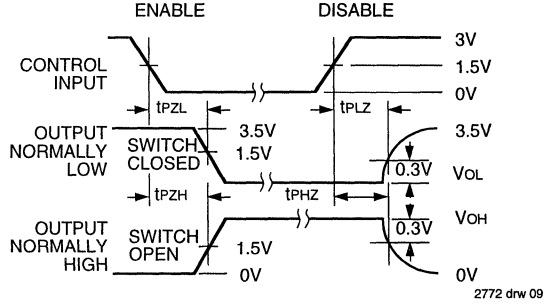
2772 drw 07

PROPAGATION DELAY



2772 drw 08

ENABLE AND DISABLE TIMES

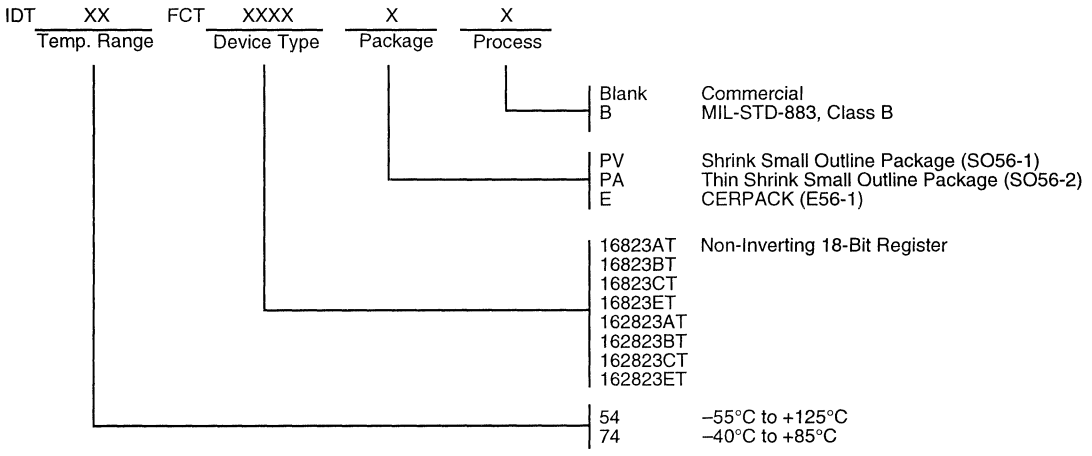


2772 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2772 drw 10

5

Integrated Device Technology, Inc.

FAST CMOS 20-BIT BUFFERS

IDT54/74FCT16827AT/BT/CT/ET
IDT54/74FCT162827AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16827AT/BT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162827AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

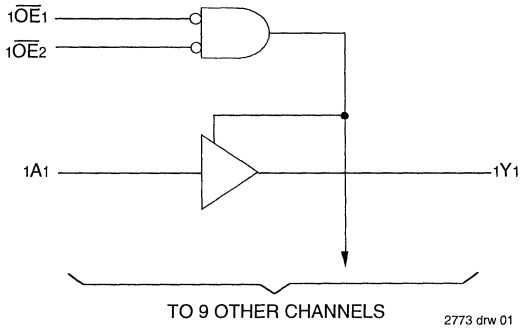
DESCRIPTION:

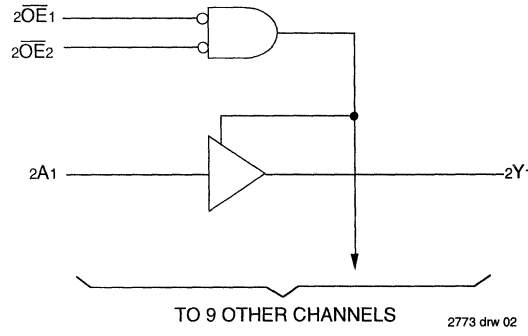
The FCT16827AT/BT/CT/ET and FCT162827AT/BT/CT/ET 20-bit buffers are built using advanced dual metal CMOS technology. These 20-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pair of NAND-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT16827AT/BT/CT/ET are ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

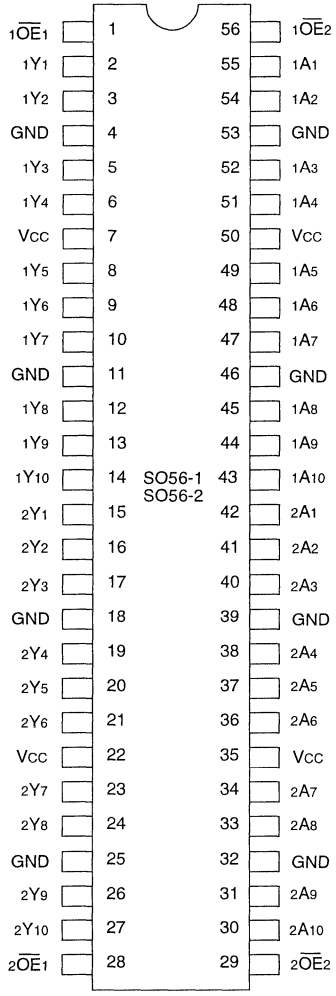
The FCT162827AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162827AT/BT/CT/ET are plug-in replacements for the FCT16827AT/BT/CT/ET and ABT16827 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM



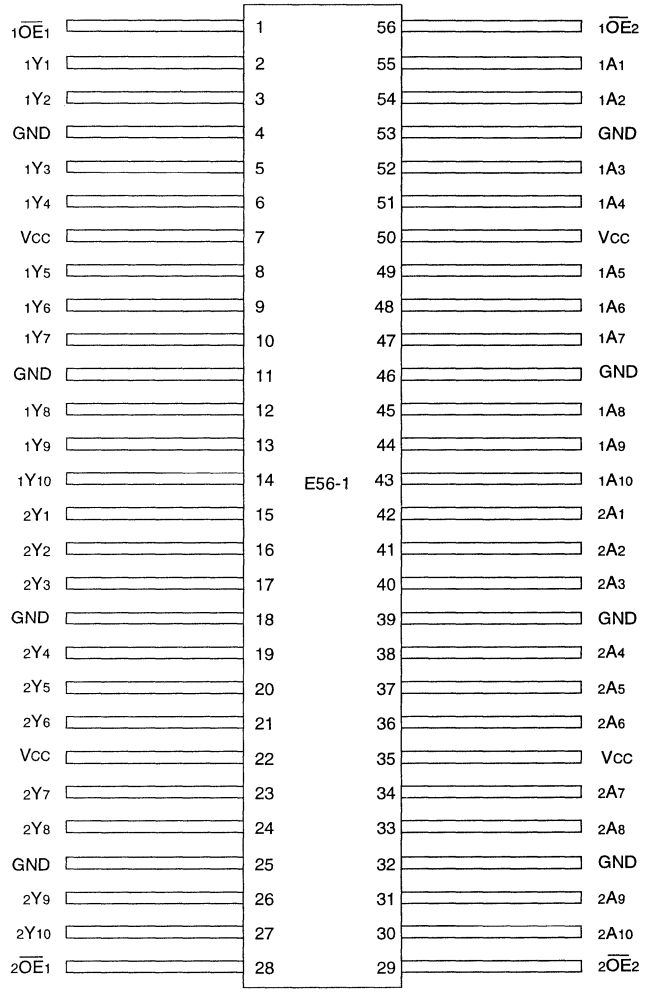


PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2773 drw 03



CERPACK
TOP VIEW

2773 drw 04

5

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}x$	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2773 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2773 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

FUNCTION TABLE(1)

Inputs			Outputs
$x\overline{OE}_1$	$x\overline{OE}_2$	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

2773 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2773 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2773 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2773 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2773 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND Twenty Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.0	20.5[5]	

2773 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16827AT/162827AT				FCT16827BT/162827BT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay xAx to xYx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
tPZH tPZL	Output Enable Time x$\overline{OE}$x to xYx	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF[4] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time x$\overline{OE}$x to xYx	CL = 5pF[4] RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2773 tbl 09

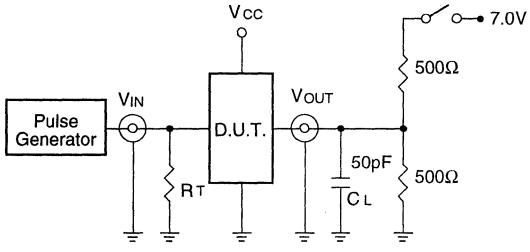
			FCT16827CT/162827CT				FCT16827ET/162827ET				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
tPLH tPHL	Propagation Delay xAx to xYx	CL = 50pF RL = 500Ω	1.5	4.4	1.5	5.0	1.5	3.2	—	—	ns
		CL = 300pF[4] RL = 500Ω	1.5	10.0	1.5	11.0	1.5	7.0	—	—	
tPZH tPZL	Output Enable Time x$\overline{OE}$x to xYx	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	4.8	—	—	ns
		CL = 300pF[4] RL = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time x$\overline{OE}$x to xYx	CL = 5pF[4] RL = 500Ω	1.5	5.7	1.5	6.7	1.5	4.0	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.0	—	—	
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2773 tbl 10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This condition is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2773 drw 05

SWITCH POSITION

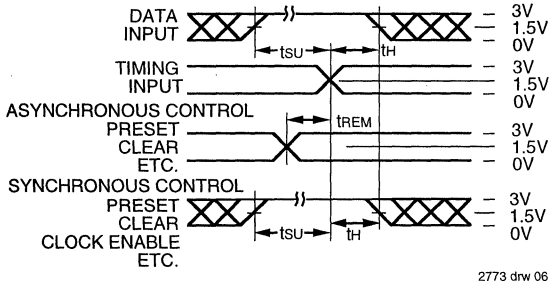
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2773 lnk 11

DEFINITIONS:

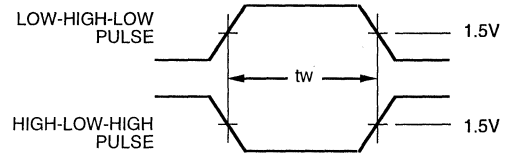
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



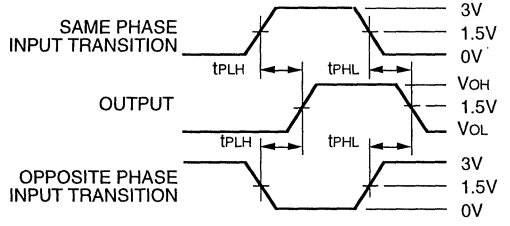
2773 drw 06

PULSE WIDTH



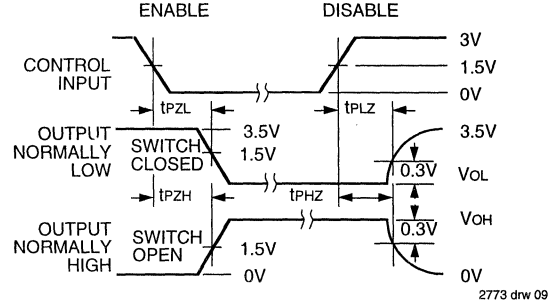
2773 drw 07

PROPAGATION DELAY



2773 drw 08

ENABLE AND DISABLE TIMES

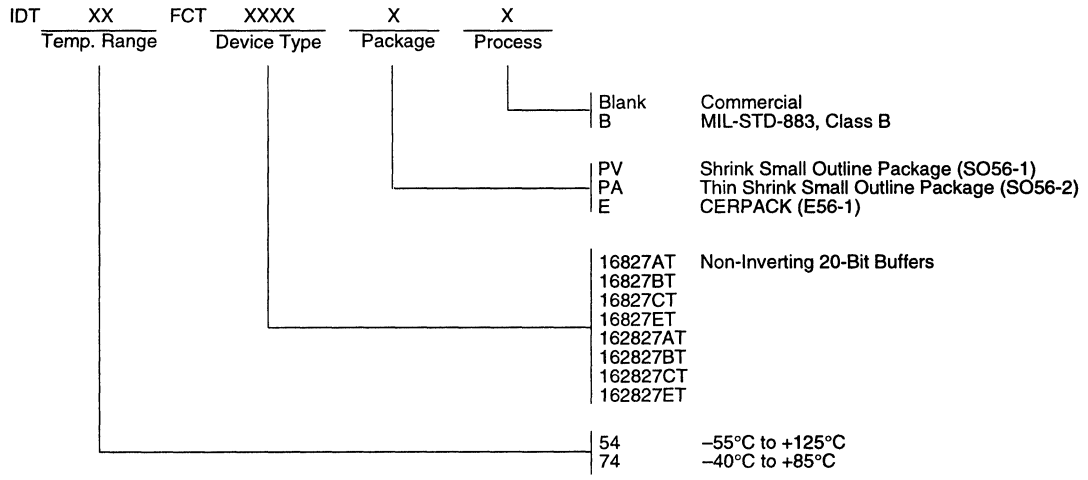


2773 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2773 drw 10

5

Integrated Device Technology, Inc.

FAST CMOS 20-BIT TRANSPARENT LATCHES

IDT54/74FCT16841AT/BT/CT/ET
IDT54/74FCT162841AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
  - V_{CC} = 5V ±10%
- **Features for FCT16841AT/BT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162841AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

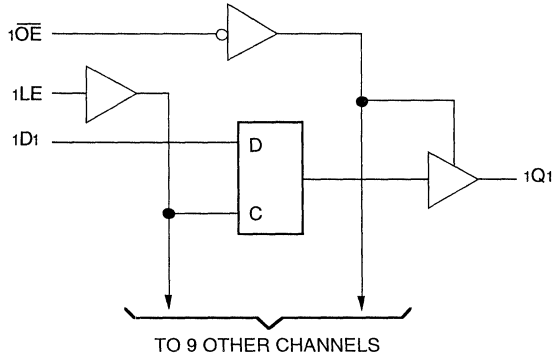
DESCRIPTION:

The FCT16841AT/BT/CT/ET and FCT162841AT/BT/CT/ET 20-bit transparent D-type latches are built using advanced dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 10-bit latches or one 20-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

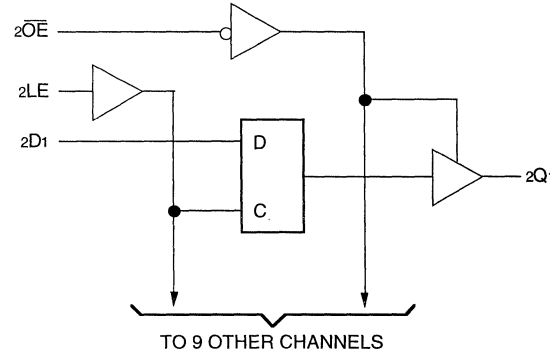
The FCT16841AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability to allow "live insertion" of boards when used as backplane drivers.

The FCT162841AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162841AT/BT/CT/ET are plug-in replacements for the FCT16841AT/BT/CT/ET and ABT16841 for on-board interface applications.

FUNCTIONAL BLOCK DIAGRAM

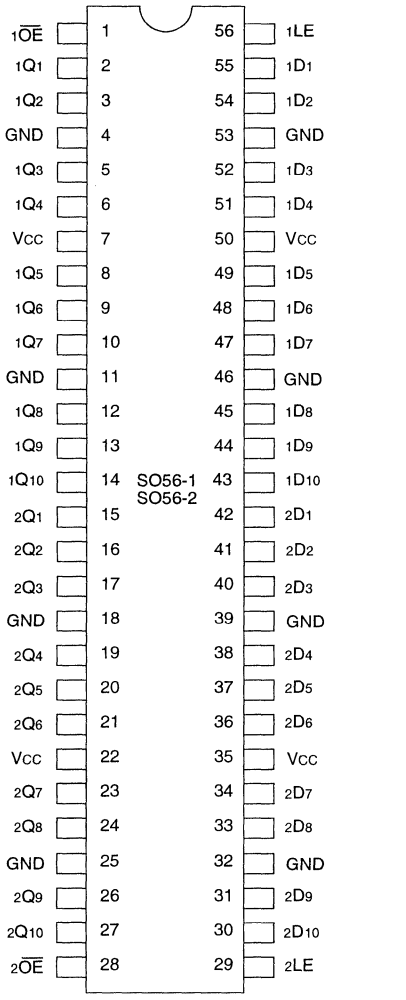


2556 drw 01

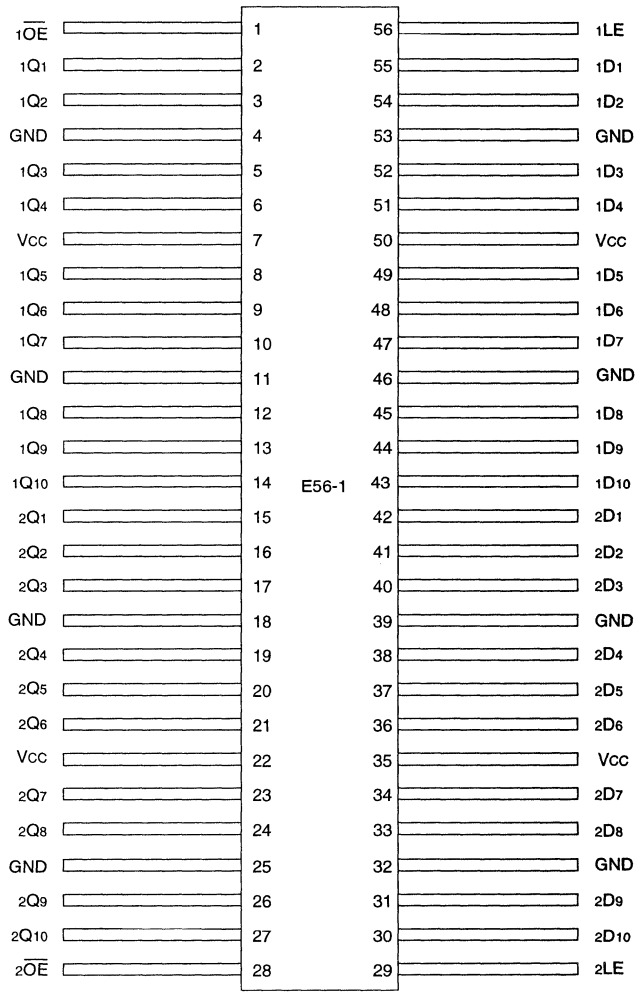


2556 drw 02

PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW



CERPACK
TOP VIEW

5

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active HIGH)
$x\overline{OE}$	Output Enable Input (Active LOW)
xQx	3-State Outputs

2556 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xDx	xLE	$x\overline{OE}$	xQx
H	H	L	H
L	H	L	L
X	L	L	Q[2]
X	X	H	Z

2556 tbl 02

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before xLE HIGH-to-LOW Transition.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2556 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2556 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2556 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16841T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2556 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162841T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2556 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.5[5]	
		50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} Twenty Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	8.0	20.5[5]	

2556 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT16841AT/162841AT				FCT16841BT/162841BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xDx to xQx (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
		CL = 300pF[5] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay xLE to xQx	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
		CL = 300pF[5] RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	
tPZH tPZL	Output Enable Time x$\overline{OE}$ to xQx	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
		CL = 300pF[5] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	
tPHZ tPLZ	Output Disable Time x$\overline{OE}$ to xQx	CL = 5pF[5] RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	
tSU	Set-Up Time HIGH or LOW, xDx to xLE	CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		2.5	—	3.0	—	2.5	—	2.5	—	ns
tW	xLE Pulse Width HIGH		4.0[4]	—	5.0	—	4.0[4]	—	4.0[4]	—	ns
tSK(o)	Output skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

NOTES:
2556 tbl 09

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

5

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

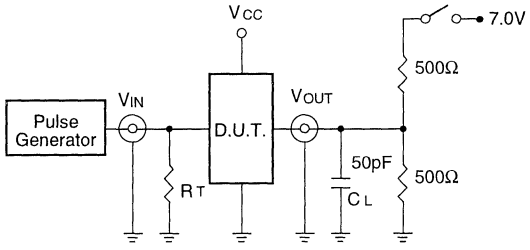
Symbol	Parameter	Condition[1]	FCT16841CT/162841CT				FCT16841ET/162841ET				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xDx to xQx (LE = HIGH)	C_L = 50pF R_L = 500Ω	1.5	5.5	1.5	6.3	1.5	3.4	—	—	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	13.0	1.5	15.0	1.5	7.5	—	—	
t_{PLH} t_{PHL}	Propagation Delay xLE to xQx	C_L = 50pF R_L = 500Ω	1.5	6.4	1.5	6.8	1.5	3.7	—	—	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	15.0	1.5	16.0	1.5	7.5	—	—	
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.3	1.5	4.4	—	—	ns
		C_L = 300pF[5] R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	9.0	—	—	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to xQx	C_L = 5pF[5] R_L = 500Ω	1.5	5.7	1.5	6.0	1.5	3.6	—	—	ns
		C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	6.3	1.5	3.6	—	—	
t_{SU}	Set-Up Time HIGH or LOW, xDx to xLE	C_L = 50pF R_L = 500Ω	2.5	—	2.5	—	1.0	—	—	—	ns
t_H	Hold Time HIGH or LOW, xDx to xLE		2.5	—	2.5	—	1.0	—	—	—	ns
t_W	xLE Pulse Width HIGH		4.0[4]	—	4.0[4]	—	3.0[4]	—	—	—	ns
$t_{SK(o)}$	Output skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

2556 tbl 10

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This limit is guaranteed but not tested.
5. This condition is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2556 drw 05

SWITCH POSITION

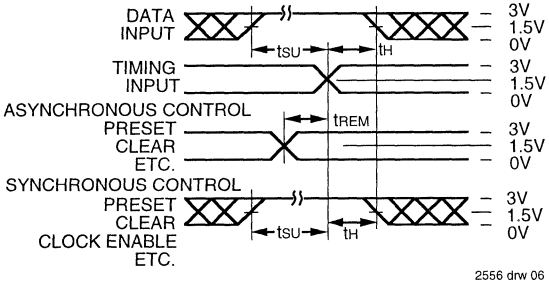
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2556 lnk 11

DEFINITIONS:

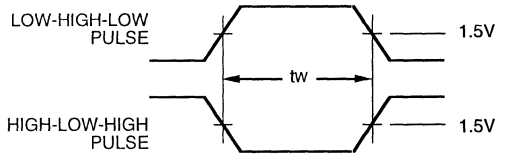
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



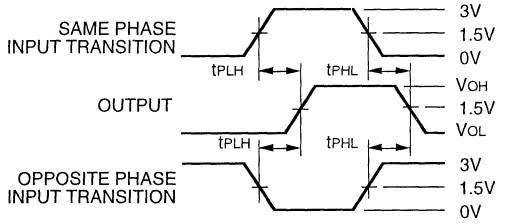
2556 drw 06

PULSE WIDTH



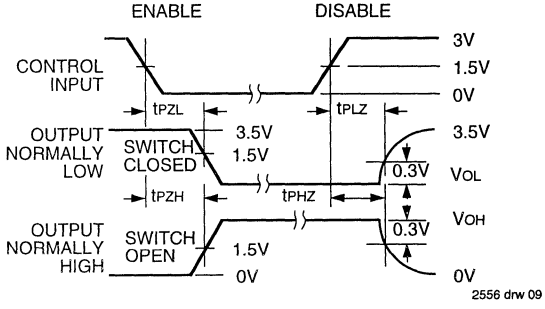
2556 drw 07

PROPAGATION DELAY



2556 drw 08

ENABLE AND DISABLE TIMES

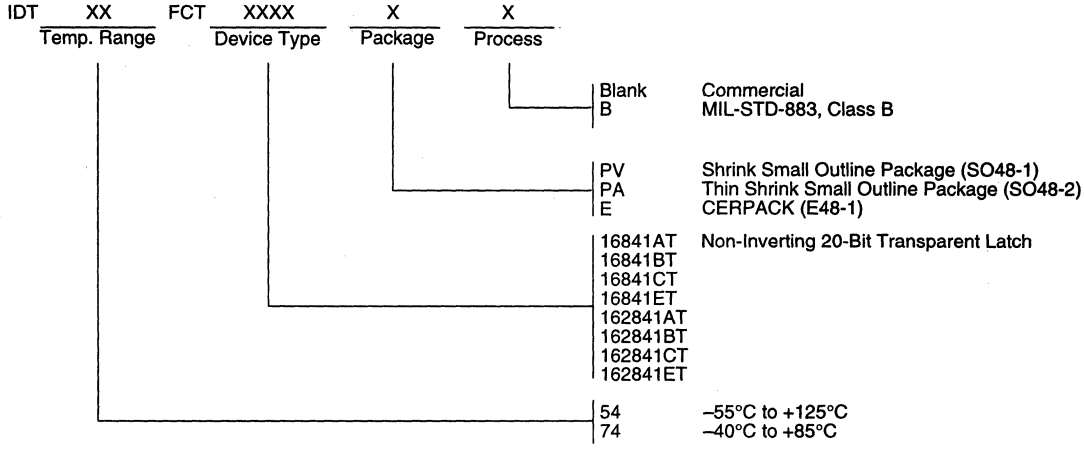


2556 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2556 drw 10

Integrated Device Technology, Inc.

FAST CMOS 16-BIT REGISTERED TRANSCEIVER

IDT54/74FCT16952AT/BT/CT/ET
IDT54/74FCT162952AT/BT/CT/ET
IDT54/74FCT162H952AT/BT/CT/ET

FEATURES:

- **Common features:**
  - 0.5 MICRON CMOS Technology
  - **High-speed, low-power CMOS replacement for ABT functions**
  - **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
  - **Low input and output leakage ≤ 1μA (max.)**
  - ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
  - 25 mil pitch SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
  - Extended commercial range of -40°C to +85°C
- **Features for FCT16952AT/BT/CT/ET:**
  - High drive outputs (-32mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162952AT/BT/CT/ET:**
  - Balanced Output Drivers: ±24mA (commercial), ±16mA (military)
  - Reduced system switching noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C
- **Features for FCT162H952AT/BT/CT/ET:**
  - Bus Hold retains last active bus state during 3-state
  - Eliminates the need for external pull up resistors

DESCRIPTION:

The FCT16952AT/BT/CT/ET and FCT162952AT/BT/CT/ET 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type registered transceivers with separate input and output control for independent control of data flow in either direction. For example, the A-to-B Enable ($x\overline{CEAB}$) must be LOW to enter data from the A port. xCLKAB controls the clocking function. When xCLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. $x\overline{OEAB}$ performs the output enable function on the B port. Data flow from the B port to A port is similar but requires using $x\overline{CEBA}$, xCLKBA, and $x\overline{OEBA}$ inputs. Full 16-bit operation is achieved by tying the control pins of the independent transceivers together.

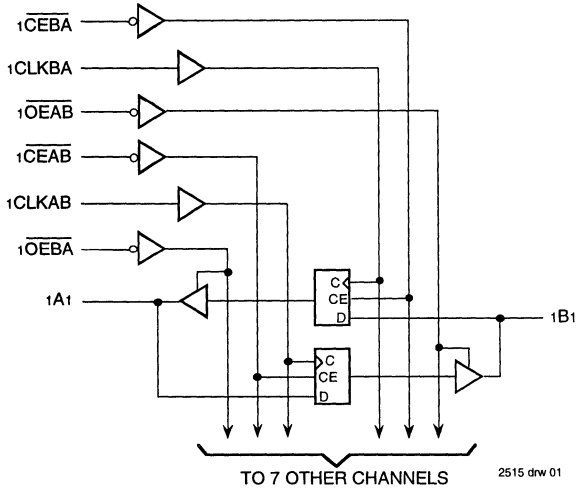
The FCT16952AT/BT/CT/ET are ideally suited for driving high-capacitance loads and low-impedance backplanes. The output buffers are designed with power off disable capability allowing "live insertion" of boards when used as backplane drivers.

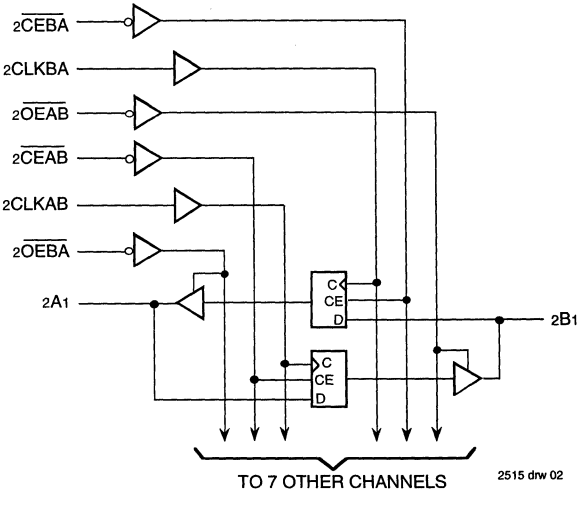
The FCT162952AT/BT/CT/ET have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors. The FCT162952AT/BT/CT/ET are plug-in replacements for the FCT16952AT/BT/CT/ET and ABT16952 for on-board bus interface applications.

The FCT162H952AT/BT/CT/ET have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

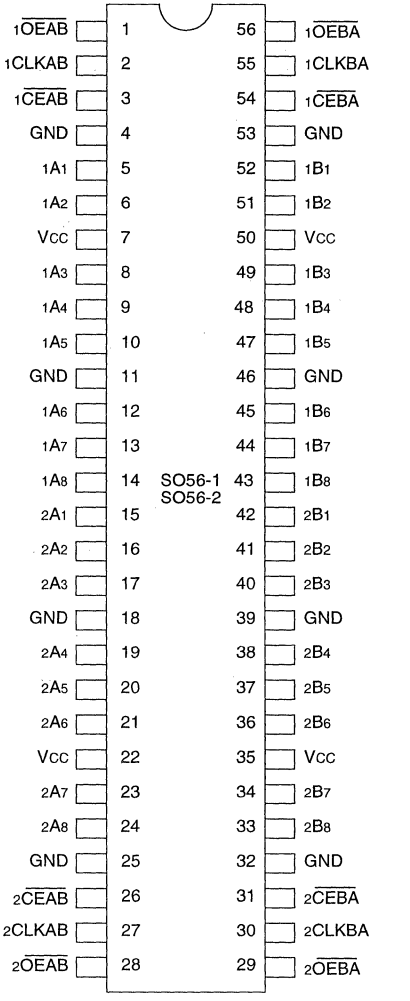
5

FUNCTIONAL BLOCK DIAGRAM



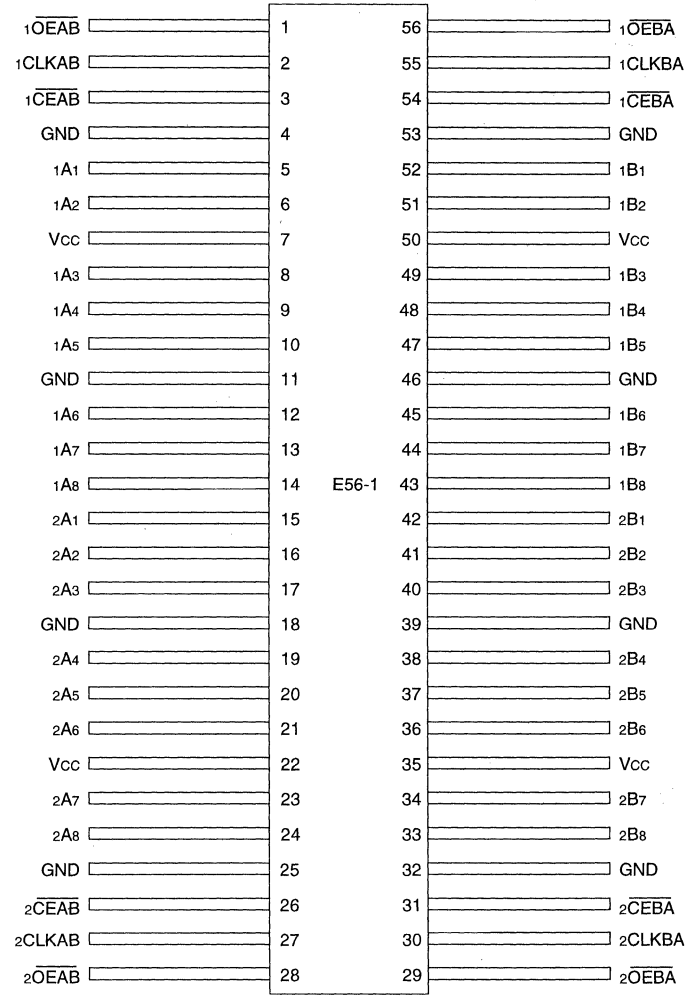


PIN CONFIGURATIONS



2515 drw 03

SSOP
TSSOP
TOP VIEW



2515 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$xOEAB$	A-to-B Output Enable Input (Active LOW)
$xOEBA$	B-to-A Output Enable Input (Active LOW)
$xCEAB$	A-to-B Clock Enable Input (Active LOW)
$xCEBA$	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs(1)
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs(1)

NOTE: 2515 tbl 01
1. On FCT16xH952T these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

FUNCTION TABLE(1,3)

Inputs				Outputs
$xCEAB$	xCLKAB	$xOEAB$	xAx	xBx
H	X	L	X	B(2)
X	L	L	X	B(2)
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES: 2515 tbl 02
1. A-to-B data flow is shown: B-to-A data flow is similar but uses, $xCEBA$, xCLKBA, and $xOEBA$.
2. Level of B before the indicated steady-state input conditions were established.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High-impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2515 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXXT Output and I/O terminals.
3. Output and I/O terminals for FCT162XXXT.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2515 lnk 04
1. This parameter is measured at characterization but not tested.

5

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2515 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT16952T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2515 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT162952T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –16mA MIL. I_{OH} = –24mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA MIL. I_{OL} = 24mA COM'L.	—	0.3	0.55	V

2515 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter		Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level		Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level		Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	Standard Input[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
		Standard I/O[5]			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I_{IL}	Input LOW Current[4]	Standard Input[5]		V_I = GND	—	—	±1	
		Standard I/O[5]			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
I_{BHH}	Bus Hold Sustain Current[4]	Bus Hold Input	V_{CC} = Min.	V_I = 2.0V	–50	—	—	µA
I_{BHL}				V_I = 0.8V	+50	—	—	
I_{OZH}	High Impedance Output Current (3-State Output pins)[5,6]		V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}				V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage		V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current		V_{CC} = Max., V_O = GND[3]		–80	–140	–225	mA
V_H	Input Hysteresis		—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current		V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

2515 lnk 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.
6. Does not include Bus Hold I/O pins.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $x\overline{OEAB}$ or $x\overline{OEBA}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.8	1.7	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.3	3.2	
		V_{CC} = Max., Outputs Open f_{CP}= 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	6.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	8.3	20.0[5]	

2515 tbl 09

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT16952AT/162952AT				FCT16952BT/162952BT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
t_{SU}	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time, HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_W	Pulse Width HIGH or LOW xCLKAB or xCLKBA[4]		3.0	—	3.0	—	3.0	—	3.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	ns

2515 tbl 10

			FCT16952CT/162952CT				FCT16952ET/162952ET				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	C_L = 50pF R_L = 500Ω	2.0	6.3	2.0	7.3	1.5	3.7	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	7.0	1.5	8.0	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx		1.5	6.5	1.5	7.5	1.5	3.6	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	1.5	—	—	—	ns
t_H	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		1.5	—	1.5	—	0	—	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		3.0	—	3.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CEAB}$, x$\overline{CEBA}$ to xCLKAB, xCLKBA		2.0	—	2.0	—	0	—	—	—	ns
t_W	Pulse Width HIGH or LOW xCLKAB or xCLKBA[4]		3.0	—	3.0	—	3.0	—	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	—	ns

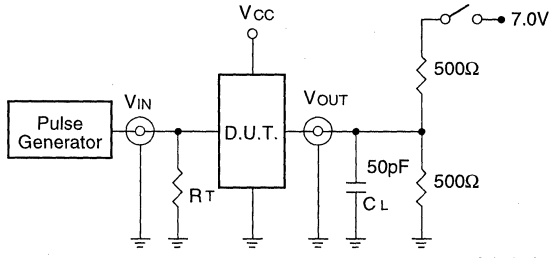
2515 tbl 11

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.

5

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2515 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

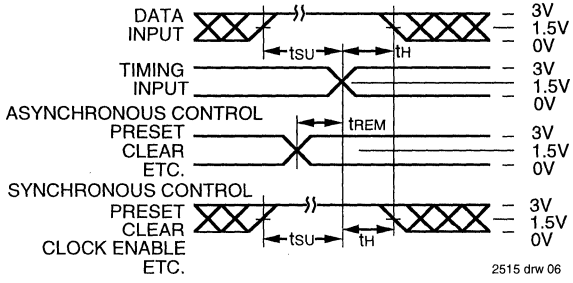
2515 lnk 12

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

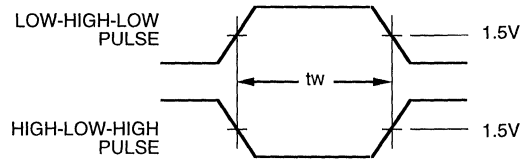
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



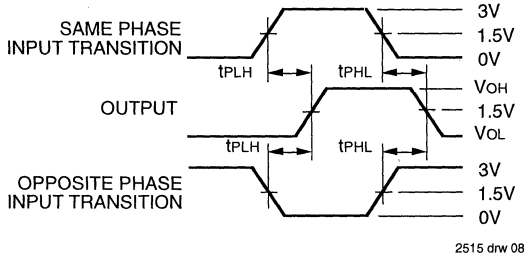
2515 drw 06

PULSE WIDTH



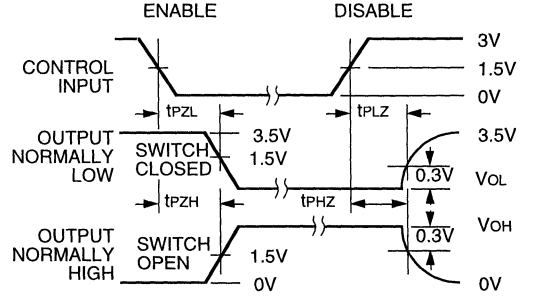
2515 drw 07

PROPAGATION DELAY



2515 drw 08

ENABLE AND DISABLE TIMES

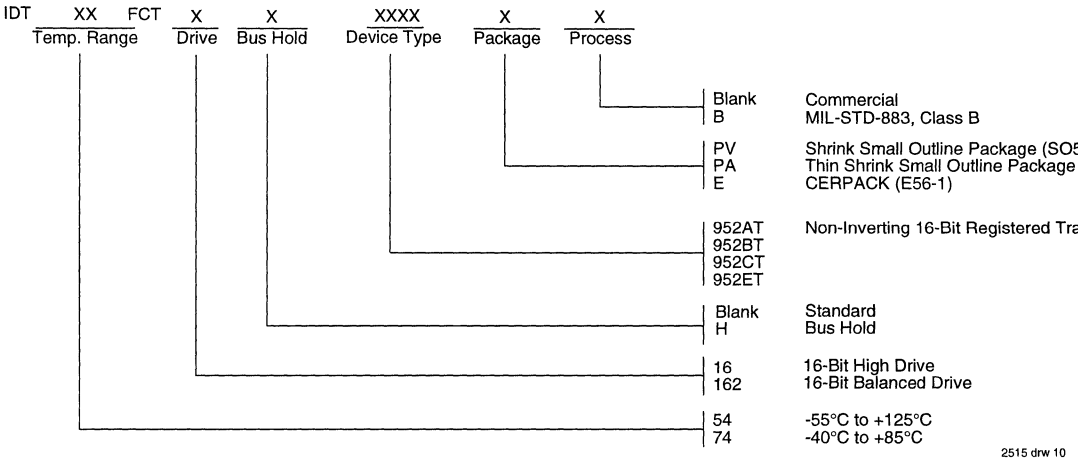


2515 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2515 drw 10

5

FCT-T OCTAL LOGIC

FCT-T Octal Logic has been designed for use in standard TTL-Logic applications. The family features high speed with low power dissipation. The family consists of a large variety of functions including bus interface products, counters, multiplexers, comparators, and other devices. There are two output configurations available which are the industry standard High Drive and the low-noise Balanced Drive. All components come in several performance grades, ranging from industry standard FAST™ speeds to today's state-of-the-art speeds, providing an easy system upgrade path. For systems migrating from 5V to 3.3V, FCT3xxx components provide a drop in replacement for FCT-T components without a speed compromise.

FCT-T Octals are TTL-compatible CMOS Logic components. By combining sub 0.5 micron CMOS technology with TTL output voltage levels, the advantages of the low static power dissipation of CMOS can be retained, while low dynamic power dissipation and lower noise levels of TTL can be achieved. This combination provides lower overall power dissipation than can be obtained from comparable bipolar, CMOS and biCMOS families.

FCT-T Balanced Drive

Balanced Drive Octal Logic (FCT2xxxT) is intended for general purpose applications requiring high speed, low power and low noise. Balanced Drive has series output resistors which reduce the drive current of the devices to +12/–15mA minimum at the Logic thresholds of 500mV and 2.4V respectively, helping to reduce transmission line noise, ringing, ground bounce, crosstalk, EMI and other noise related problems. Balanced Drive also will drive ±48mA (typical) at the 1.5V level, giving equal line driving currents and matching edge rates for both the Logic HIGH transition and Logic LOW transition. Balanced Drive is the family of choice for loads of less-than 200pF.

FCT-T High Drive

High Drive Octal Logic (FCTxxxT) is fully compatible with industry standard TTL Logic families. High Drive comes in a variety of speed grades, allowing an upgrade path to higher system performance unlike single speed grade families. Most high drive components have 64mA output drive capability, making them an excellent choice for heavy bus and back plane drivers.

FCT 3.3V

FCT 3.3V Octal Logic (FCT3xxx) is leading the industry's move to 3.3V. FCT 3.3V components are function and AC spec compatible with equivalent FCT-T components. These devices offer significant advantages in low power dissipation and speed over standard CMOS, bipolar, and biCMOS families. The 3.3V data sheets are located in the 3.3V section of this data book.

FAST is a trademark of National Semiconductor, Inc.

SECTION 6
OCTAL 5V PRODUCTS
TABLE OF CONTENTS

TTL-LEVEL WITH BALANCED DRIVE OUTPUT

TTL-LEVEL WITH HIGH DRIVE OUTPUT

TTL-LEVEL WITH HIGH DRIVE OUTPUT (CONTINUED)

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

IDT29FCT52AT/BT/CT/DT
IDT29FCT2052AT/BT/CT
IDT29FCT53AT/BT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for 29FCT52/29FCT53T:**
  - A, B, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
- **Features for 29FCT2052T:**
  - A, B and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

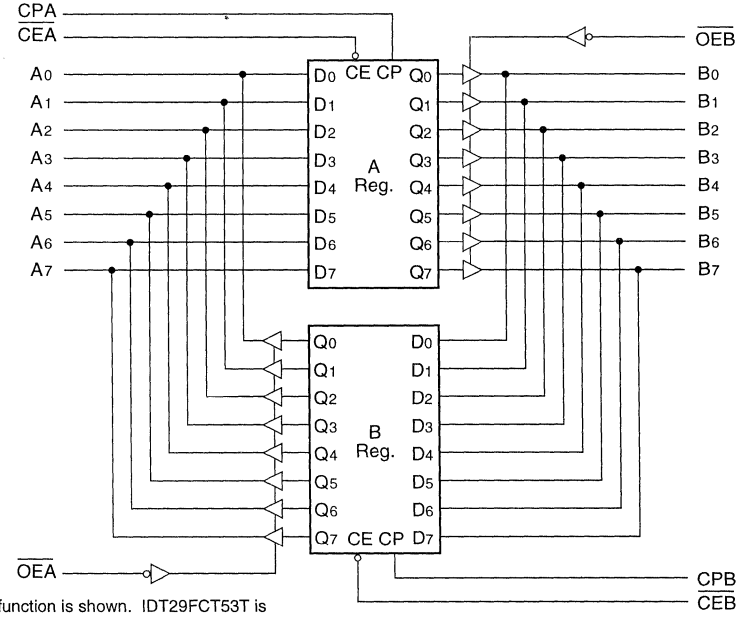
DESCRIPTION:

The IDT29FCT52AT/BT/CT/DT and IDT29FCT53AT/BT/CT are 8-bit registered transceivers built using an advanced dual metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52AT/BT/CT/DT and IDT29FCT2052AT/BT/CT are non-inverting options of the IDT29FCT53AT/BT/CT.

The IDT29FCT2052AT/BT/CT has balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The IDT29FCT2052T part is a plug-in replacement for IDT29FCT52T part.

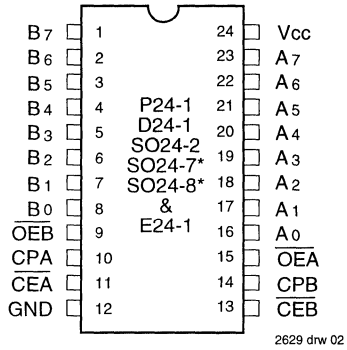
FUNCTIONAL BLOCK DIAGRAM(1)



NOTE:
1. IDT29FCT52T/IDT29FCT2052T function is shown. IDT29FCT53T is the inverting option.

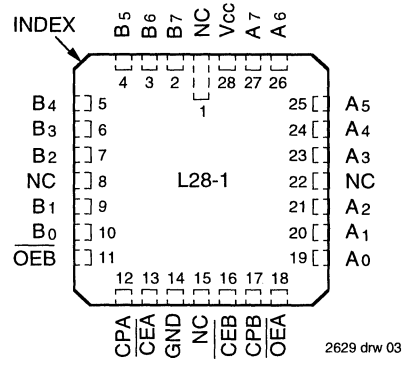
2629 drw 01

PIN CONFIGURATIONS



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

* For 29FCT52/29FCT2052AT/BT/CT only



LCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
A_{0-7}	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B_{0-7}	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B_{0-7} lines. When $\overline{OEB}$ is HIGH, the B_{0-7} outputs are in the high-impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A_{0-7} lines. When $\overline{OEA}$ is HIGH, the A_{0-7} outputs are in the high-impedance state.

2629 tbl 01

6

REGISTER FUNCTION TABLE[1]
(Applies to A or B Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

2629 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition

OUTPUT CONTROL[1]

	Internal	Y-Outputs		
$\overline{OE}$	Q	52/2052	53	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

2629 tbl 03

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2529 lnk 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2640 lnk 05

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2629 tbl 06

OUTPUT DRIVE CHARACTERISTICS FOR 29FCT52T/29FCT53T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2629 tbl 07

OUTPUT DRIVE CHARACTERISTICS FOR 29FCT2052T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

2629 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ or $\overline{OE}_B$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND One Bit Toggling at fi = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4V	FCTxxxT	—	2.0	5.5	
			V_{IN} = GND	FCT2xxxT		1.1	4.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND Eight Bits Toggling at fi = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	3.8	7.3[5]	
				FCT2xxxT	—	1.5	4.0[5]	
			V_{IN} = 3.4V	FCTxxxT	—	6.0	16.3[5]	
			V_{IN} = GND	FCT2xxxT	—	3.8	13.0[5]	

2629 tbl 09

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	29FCT52AT/53AT 29FCT2052AT				29FCT52BT/53BT 29FCT2052BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to An, Bn	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
t_{SU}	Set-up Time, HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time, HIGH or LOW An, Bn to CPA, CPB		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	3.0	—	3.0	—	ns
t_H	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		3.0	—	3.0	—	3.0	—	3.0	—	ns

2629 tbl 10

Symbol	Parameter	Condition[1]	29FCT52CT/53CT 29FCT2052CT				29FCT52DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to An, Bn	C_L = 50pF R_L = 500Ω	2.0	6.3	2.0	7.3	2.0	4.5	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	7.0	1.5	8.0	1.5	5.6	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	6.5	1.5	7.5	1.5	4.3	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	1.5	—	—	—	ns
t_H	Hold Time, HIGH or LOW An, Bn to CPA, CPB		1.5	—	1.5	—	1.0	—	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	2.0	—	—	—	ns
t_H	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	1.0	—	—	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		3.0	—	3.0	—	3.0	—	—	—	ns

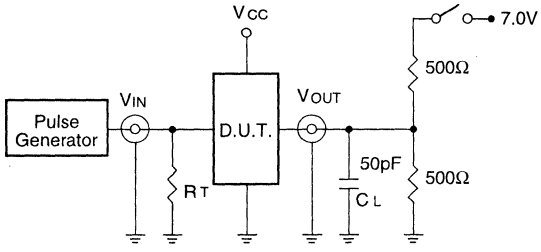
NOTES:
2629 tbl 11

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2629 drw 03

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

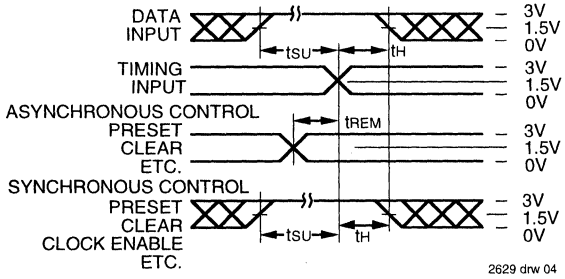
2629 lnk 12

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

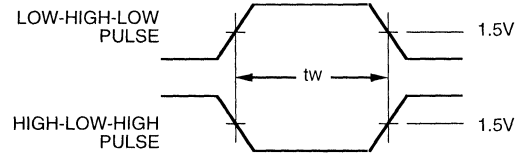
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



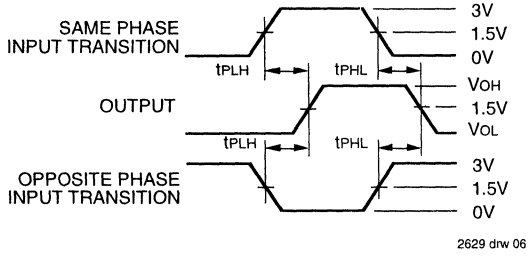
2629 drw 04

PULSE WIDTH

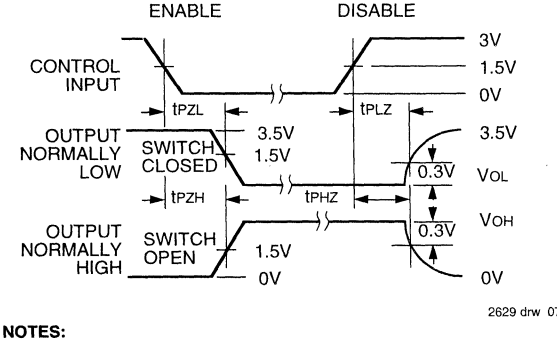


2629 drw 05

PROPAGATION DELAY



2629 drw 06

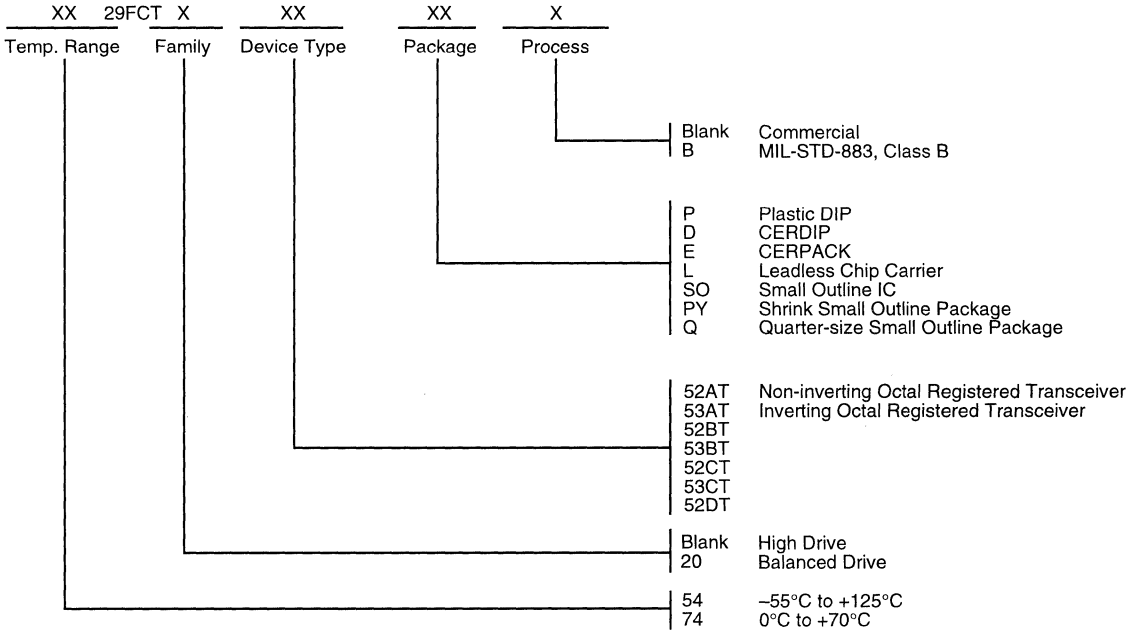


2629 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2629 drw 08

6

Integrated Device Technology, Inc.

MULTILEVEL PIPELINE REGISTERS

IDT29FCT520AT/BT/CT/DT
IDT29FCT521AT/BT/CT/DT

FEATURES:

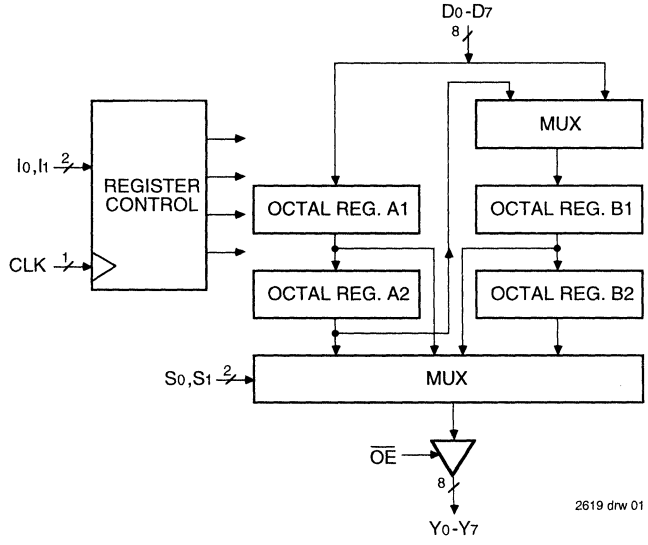
- A, B, C and D speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

DESCRIPTION:

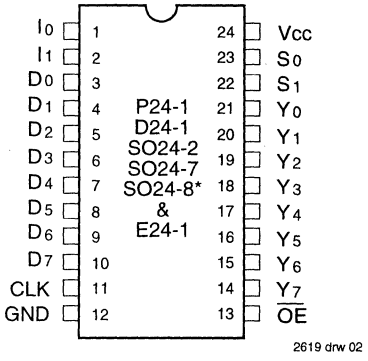
The IDT29FCT520AT/BT/CT/DT and IDT29FCT521AT/BT/CT/DT each contain four 8-bit positive edge-triggered registers. These may be operated as a dual 2-level or as a single 4-level pipeline. A single 8-bit input is provided and any of the four registers is available at the 8-bit, 3-state output.

These devices differ only in the way data is loaded into and between the registers in 2-level operation. The difference is illustrated in Figure 1. In the IDT29FCT520AT/BT/CT/DT when data is entered into the first level (I = 2 or I = 1), the existing data in the first level is moved to the second level. In the IDT29FCT521AT/BT/CT/DT, these instructions simply cause the data in the first level to be overwritten. Transfer of data to the second level is achieved using the 4-level shift instruction (I = 0). This transfer also causes the first level to change. In either part I=3 is for hold.

FUNCTIONAL BLOCK DIAGRAM

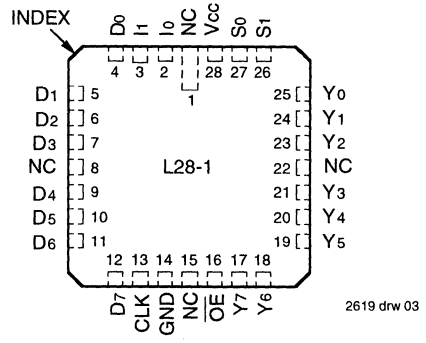


PIN CONFIGURATIONS



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

*FCT520 only



LCC
TOP VIEW

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
D_n	Register input Port.
CLK	Clock input. Enter data into registers on LOW-to-HIGH transitions.
I_0, I_1	Instruction inputs. See Figure 1 and instruction Control Tables.
S_0, S_1	Multiplexer select. Inputs either register A_1, A_2, B_1 or B_2 data to be available at the output port.
$\overline{OE}$	Output enable for 3-state output port.
Y_n	Register output port.

2619 tbl 01

REGISTER SELECTION

S_1	S_0	Register
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1

2619 tbl 02

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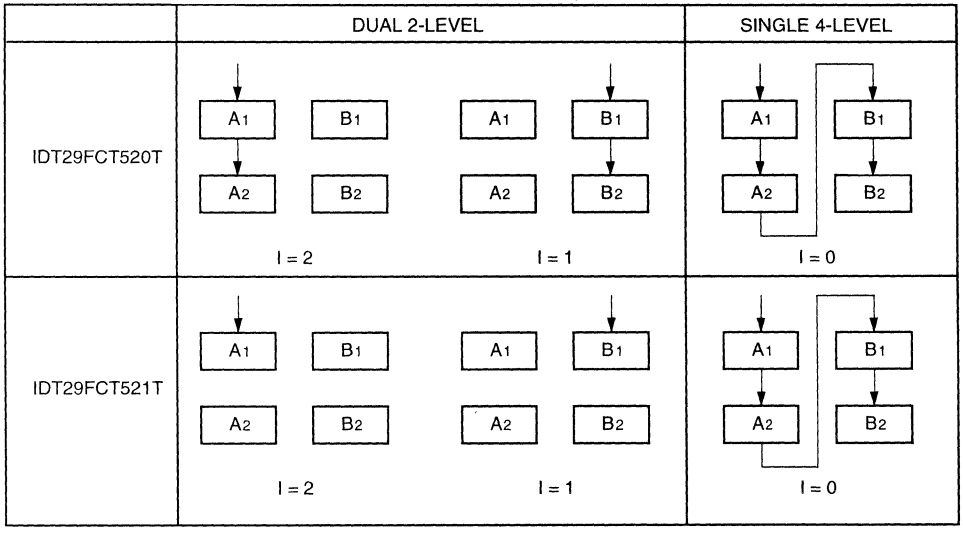


NOTE:
1. I = 3 for hold.

Figure 1. Data Loading in 2-Level Operation

2619 drw 04

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2619 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2619 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance(4)	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

NOTES: 2619 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current, TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.0	16.3[5]	

2619 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL HIgh Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT520AT/521AT				FCT520BT/521BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PHL} t_{PLH}	Propagation Delay CLK to Yn	C_L = 50pF R_L = 500Ω	2.0	14.0	2.0	16.0	2.0	7.5	2.0	8.0	ns
t_{PHL} t_{PLH}	Propagation Delay S_0 or S_1 to Yn		2.0	13.0	2.0	15.0	2.0	7.5	2.0	8.0	ns
t_{SU}	Set-up Time, HIGH or LOW Dn to CLK		5.0	—	6.0	—	2.5	—	2.8	—	ns
t_H	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{SU}	Set-up Time, HIGH or LOW I_0 or I_1 to CLK		5.0	—	6.0	—	4.0	—	4.5	—	ns
t_H	Hold Time, HIGH or LOW I_0 or I_1 to CLK		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	12.0	1.5	13.0	1.5	7.0	1.5	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	15.0	1.5	16.0	1.5	7.5	1.5	8.0	ns
t_W	Clock Pulse Width HIGH or LOW		7.0	—	8.0	—	5.5	—	6.0	—	ns

2619 tbl 07

Symbol	Parameter	Condition[1]	FCT520CT/521CT				FCT520DT/521DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PHL} t_{PLH}	Propagation Delay CLK to Yn	C_L = 50pF R_L = 500Ω	2.0	6.0	2.0	7.0	2.0	5.2	—	—	ns
t_{PHL} t_{PLH}	Propagation Delay S_0 or S_1 to Yn		2.0	6.0	2.0	7.0	2.0	4.8	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW Dn to CLK		2.5	—	2.8	—	1.5	—	—	—	ns
t_H	Hold Time, HIGH or LOW Dn to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW I_0 or I_1 to CLK		4.0	—	4.5	—	2.0	—	—	—	ns
t_H	Hold Time, HIGH or LOW I_0 or I_1 to CLK		2.0	—	2.0	—	1.0	—	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	6.0	1.5	6.0	1.5	4.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	6.0	1.5	7.0	1.5	4.0	—	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		5.5	—	6.0	—	3.0	—	—	—	ns

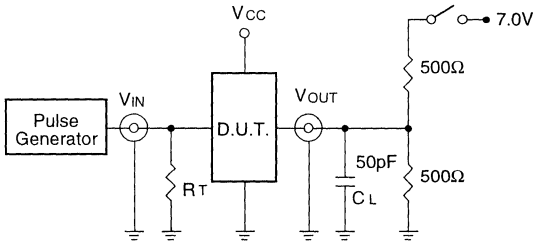
NOTES:

2619 tbl 08

1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2619 drw 05

SWITCH POSITION

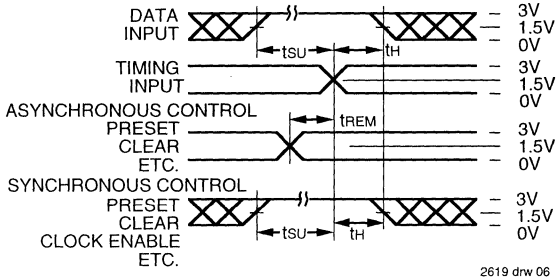
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2619 lnk 09

DEFINITIONS:

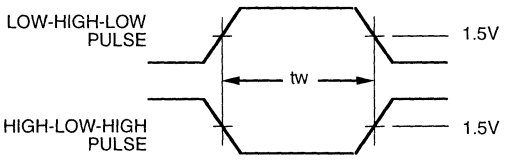
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



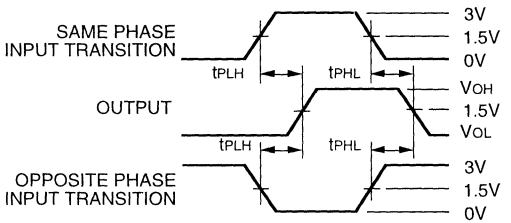
2619 drw 06

PULSE WIDTH



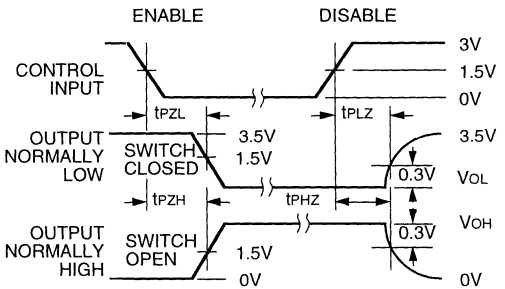
2619 drw 07

PROPAGATION DELAY



2619 drw 08

ENABLE AND DISABLE TIMES



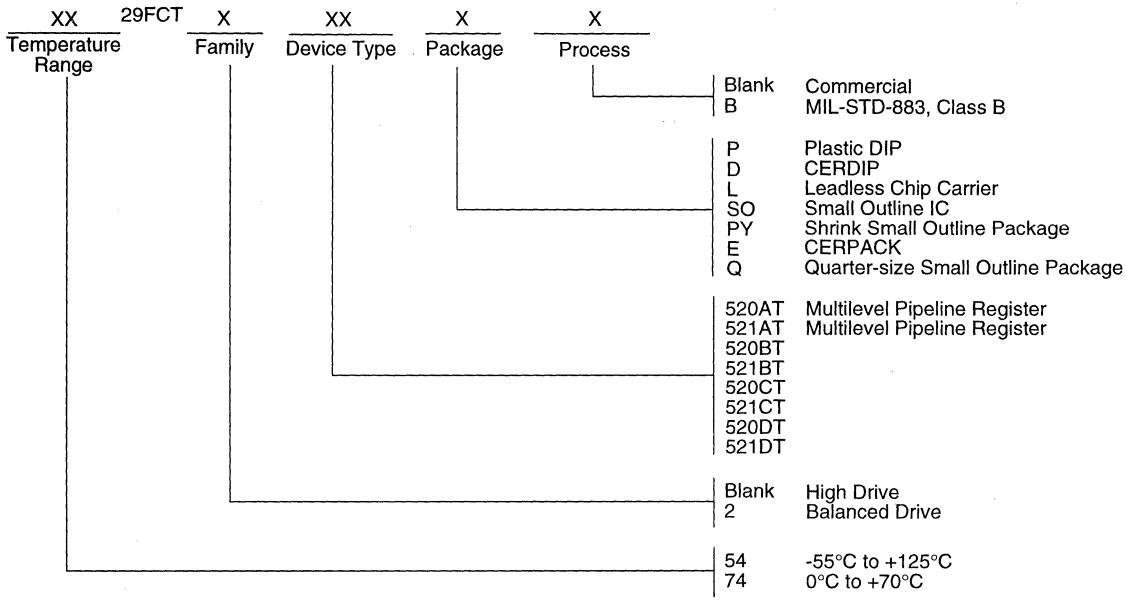
2619 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

6

ORDERING INFORMATION



2619 drw 10

Integrated Device Technology, Inc.

FAST CMOS 1-OF-8 DECODER WITH ENABLE

IDT54/74FCT138T/AT/CT

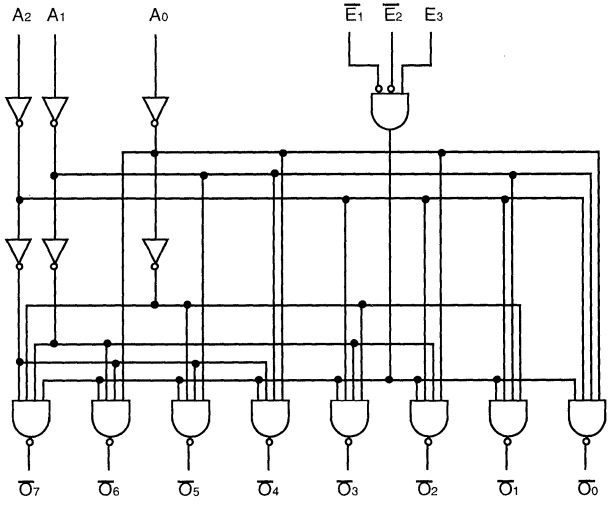
FEATURES:

- Std., A and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

DESCRIPTION:

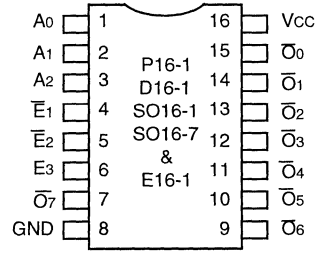
The IDT54/74FCT138T/AT/CT are 1-of-8 decoders built using an advanced dual metal CMOS technology. The IDT54/74FCT138T/AT/CT accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$). The IDT54/74FCT138T/AT/CT features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four IDT54/74FCT138T/AT/CT devices and one inverter.

FUNCTIONAL BLOCK DIAGRAM



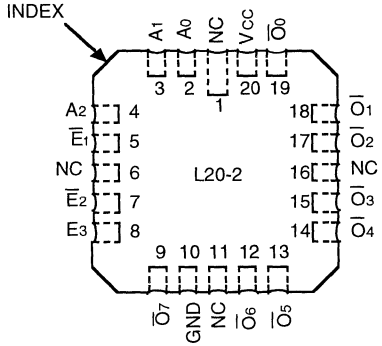
2570 drw 01

PIN CONFIGURATIONS



2570 drw 02

DIP/SOIC/QSOP/CERPACK TOP VIEW



2570 drw 03

LCC TOP VIEW

PIN DESCRIPTION

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$–$\overline{O}_7$	Outputs (Active LOW)

2570 tbl 01

FUNCTION TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

2570 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2570 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2570 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2570 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Toggle $\overline{E}_1$, $\overline{E}_2$ or E_3 50% Duty Cycle f_o = 10MHz One Input and One Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	5.0	

NOTES:
2570 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_o)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_o = Output Frequency
   N_o = Number of Outputs at f_o
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

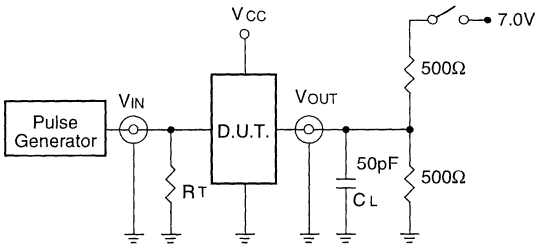
			FCT138T				FCT138AT				FCT138CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.8	1.5	7.8	1.5	5.1	1.5	6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	ns
t_{PLH} t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$		1.5	9.0	1.5	12.5	1.5	5.9	1.5	8.0	1.5	5.2	1.5	6.1	ns

NOTES:
2570 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2570 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

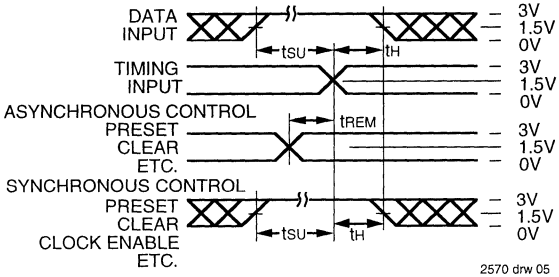
2570 tbl 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

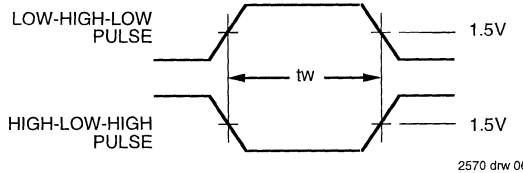
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



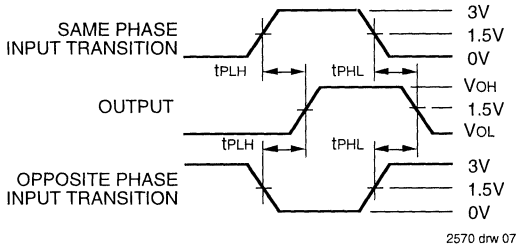
2570 drw 05

PULSE WIDTH



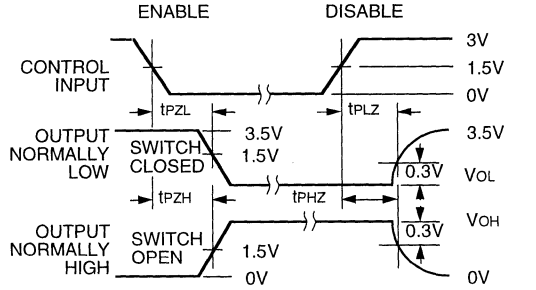
2570 drw 06

PROPAGATION DELAY



2570 drw 07

ENABLE AND DISABLE TIMES



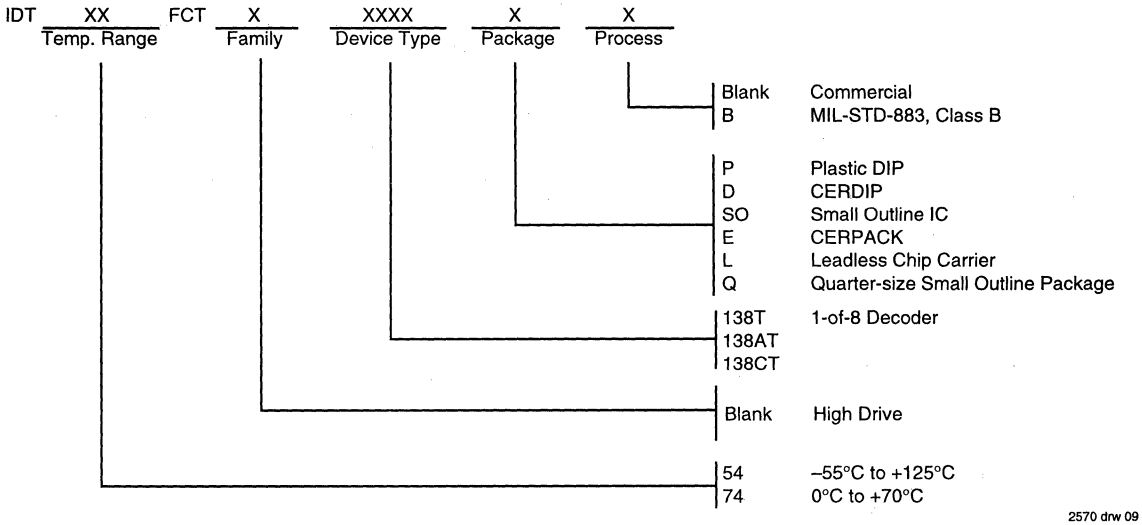
2570 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

6

ORDERING INFORMATION



2570 drw 09

Integrated Device Technology, Inc.

FAST CMOS DUAL 1-OF-4 DECODER WITH ENABLE

IDT54/74FCT139T/AT/CT

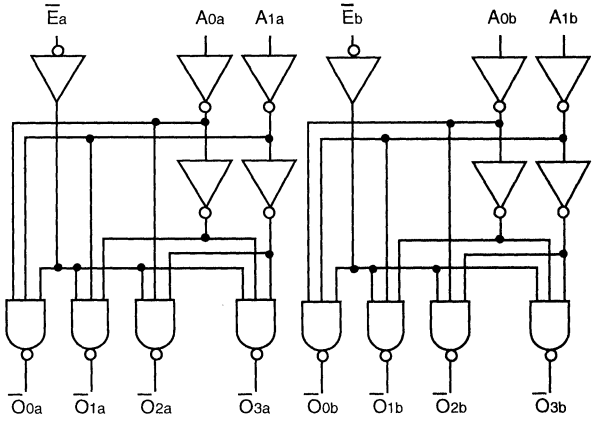
FEATURES:

- Std., A and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

DESCRIPTION:

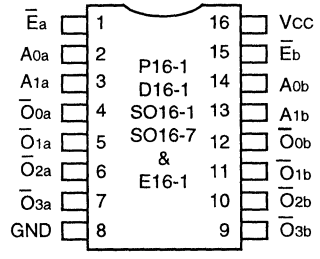
The IDT54/74FCT139T/AT/CT are dual 1-of-4 decoders built using an advanced dual metal CMOS technology. These devices have two independent decoders, each of which accept two binary weighted inputs (A_0-A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH, all outputs are forced HIGH.

FUNCTIONAL BLOCK DIAGRAM



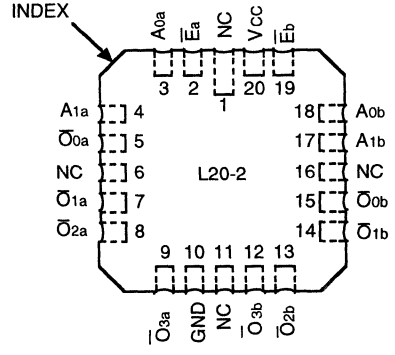
2566 drw 01

PIN CONFIGURATIONS



DIP/SOIC/QSOP/CERPACK
TOP VIEW

2566 drw 02



2566 drw 03

LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2566 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

PIN DESCRIPTION

Pin Names	Description
A_0, A_1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{O}_0$ - $\overline{O}_3$	Outputs (Active LOW)

2566 tbl 01

FUNCTION TABLE(1)

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

2566 tbl 02

NOTE:
1. H = HIGH Voltage Level; L = LOW Voltage Level; X = Don't Care

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2566 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2566 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.3	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_O = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	4.0	mA
		50% Duty Cycle One Input and One Output Toggling	V_{IN} = 3.4V V_{IN} = GND	—	1.8	5.0	
		V_{CC} = Max. Outputs Open f_O = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	7.0[5]	
		50% Duty Cycle One Input Toggling on Each Decoder Two Outputs Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	9.0[5]	

2566 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

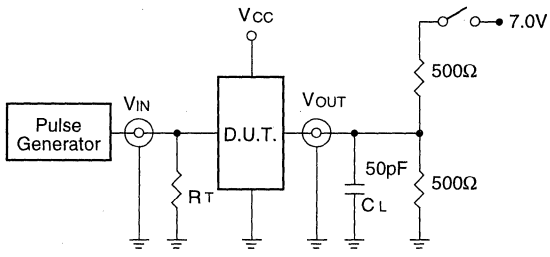
			FCT139T				FCT139AT				FCT139CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Parameter	Description	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A_0 or A_1 to $\overline{O}_n$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	12.0	1.5	5.9	1.5	7.8	1.5	5.0	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{O}_n$		1.5	8.0	1.5	9.0	1.5	5.5	1.5	7.2	1.5	4.8	1.5	5.8	ns

2566 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2566 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

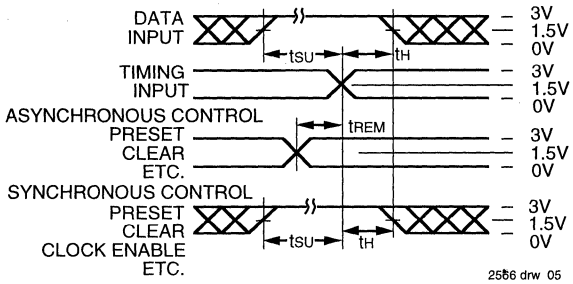
2566 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

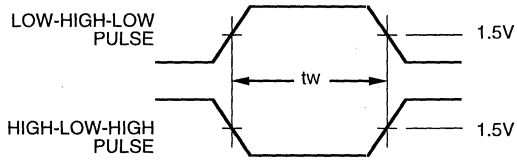
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



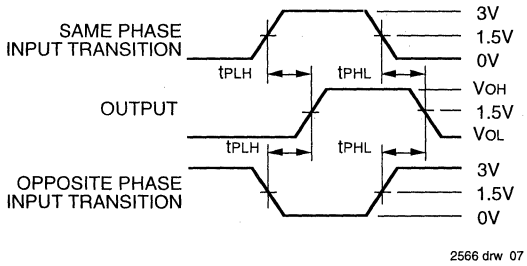
2566 drw 05

PULSE WIDTH



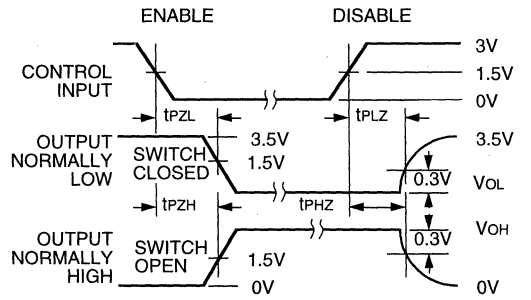
2566 drw 06

PROPAGATION DELAY



2566 drw 07

ENABLE AND DISABLE TIMES

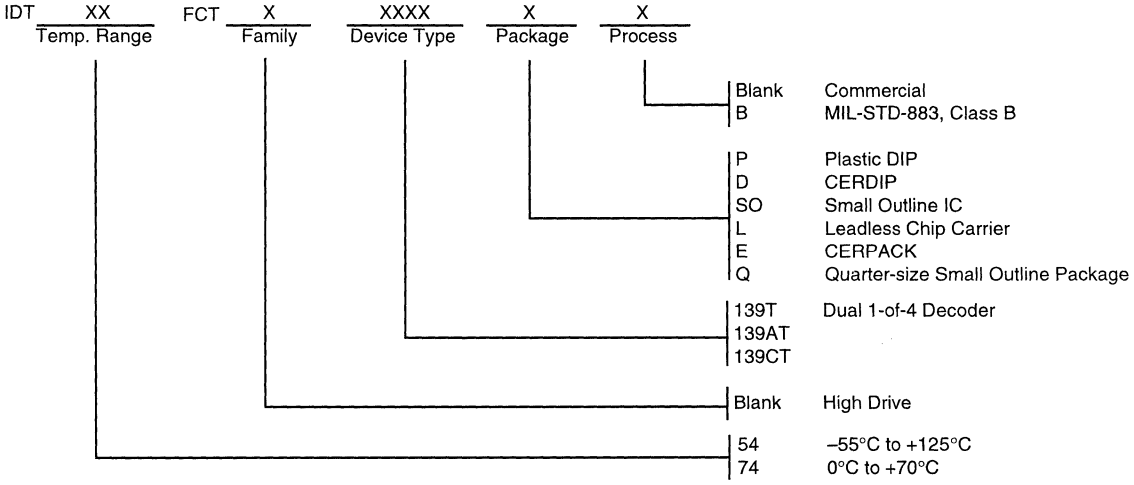


2566 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2566 drw 09

6

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT MULTIPLEXER

IDT54/74FCT151T/AT/CT

FEATURES:

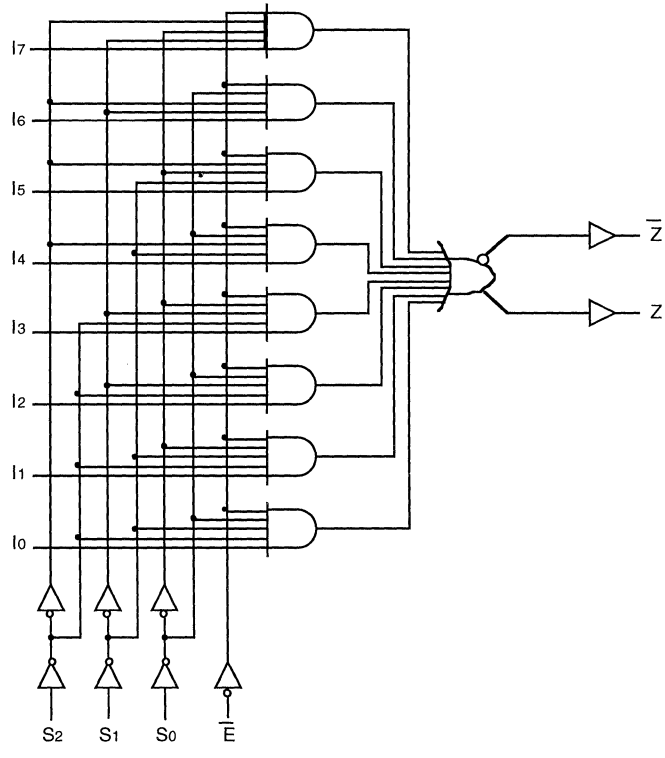
- Std., A, and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

DESCRIPTION:

The IDT54/74FCT151T/AT/CT are high-speed 8-input multiplexers built using an advanced dual metal CMOS technology. They select one bit of data from up to eight sources under the control of three select inputs. Both assertion and negation outputs are provided.

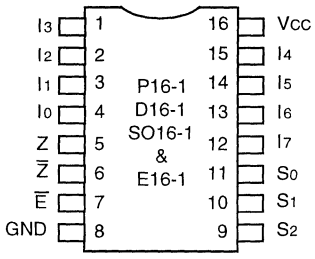
The IDT54/74FCT151T/AT/CT has a common Active-LOW enable ($\overline{E}$) input. When $\overline{E}$ is LOW, data from one of eight inputs is routed to the complementary outputs according to the 3-bit code applied to the Select (S_0-S_2) inputs. A common application of the 'FCT151 is data routing from one of eight sources.

FUNCTIONAL BLOCK DIAGRAM



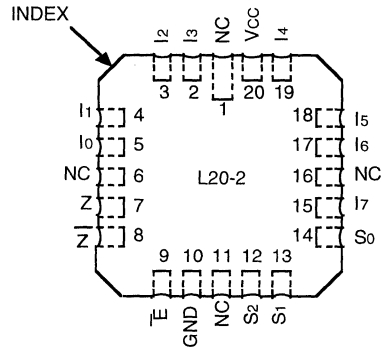
2635 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2635 drw 02



2635 drw 03

LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2635 lnk 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2635 lnk 02

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
I_0 - I_7	Data Inputs
S_0 - S_2	Selects Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Data Output
$\overline{Z}$	Inverted Data Output

2635 tbl 03

FUNCTION TABLE(1)

Inputs				Outputs	
S_2	S_1	S_0	$\overline{E}$	Z	$\overline{Z}$
X	X	X	H	L	H
L	L	L	L	I_0	$\overline{I_0}$
L	L	H	L	I_1	$\overline{I_1}$
L	H	L	L	I_2	$\overline{I_2}$
L	H	H	L	I_3	$\overline{I_3}$
H	L	L	L	I_4	$\overline{I_4}$
H	L	H	L	I_5	$\overline{I_5}$
H	H	L	L	I_6	$\overline{I_6}$
H	H	H	L	I_7	$\overline{I_7}$

NOTE: 2635 tbl 04

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't care, Z = High Impedance.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current[4]	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}			V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2635 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	QuiescentPower Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	6.5	mA
		50% Duty Cycle $\overline{E}$ or $\overline{OE}$= GND One Input Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	7.5	

2635 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_O = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT151T				IDT54/74FCT151AT				IDT54/74FCT151CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay S_N to $\overline{Z}$	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	10.0	1.5	6.6	1.5	7.4	1.5	5.6	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay S_N to Z		1.5	10.5	1.5	11.5	1.5	6.8	1.5	7.6	1.5	5.8	1.5	6.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		1.5	7.0	1.5	7.5	1.5	5.6	1.5	6.3	1.5	4.8	1.5	5.4	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z		1.5	9.5	1.5	11.0	1.5	5.8	1.5	6.6	1.5	5.0	1.5	5.7	ns
t_{PLH} t_{PHL}	Propagation Delay I_N to $\overline{Z}$		1.5	6.5	1.5	7.5	1.5	5.2	1.5	5.8	1.5	4.4	1.5	4.9	ns
t_{PLH} t_{PHL}	Propagation Delay I_N to Z		1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.1	1.5	4.7	1.5	5.2	ns

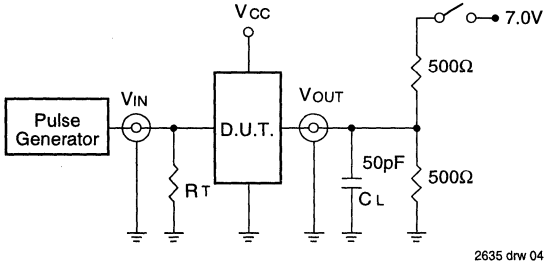
NOTES:

2635 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2635 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

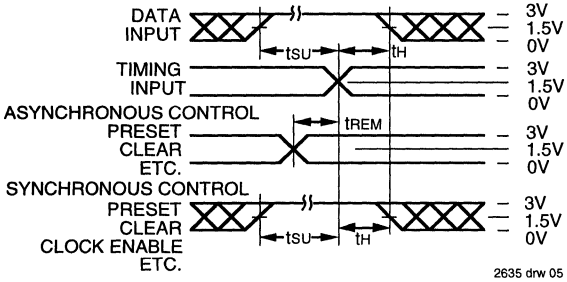
2635 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

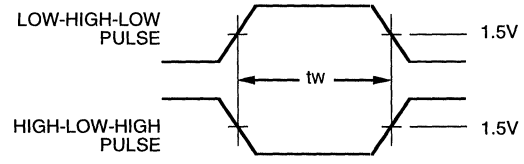
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



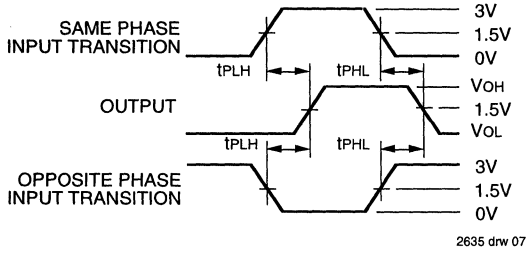
2635 drw 05

PULSE WIDTH



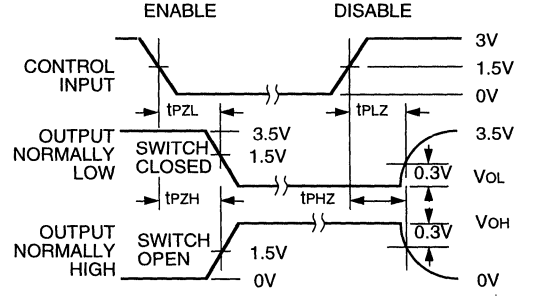
2635 drw 06

PROPAGATION DELAY



2635 drw 07

ENABLE AND DISABLE TIMES

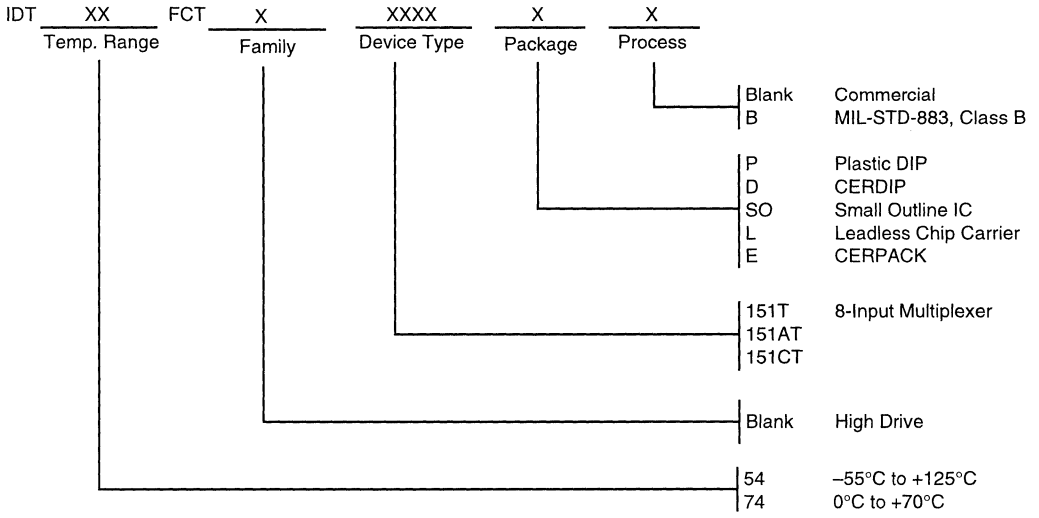


2635 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2635 drw 09

6

Integrated Device Technology, Inc.

FAST CMOS QUAD 2-INPUT MULTIPLEXER

IDT54/74FCT157T/AT/CT/DT
IDT54/74FCT257T/AT/CT/DT

FEATURES:

- Std., A, C and D speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

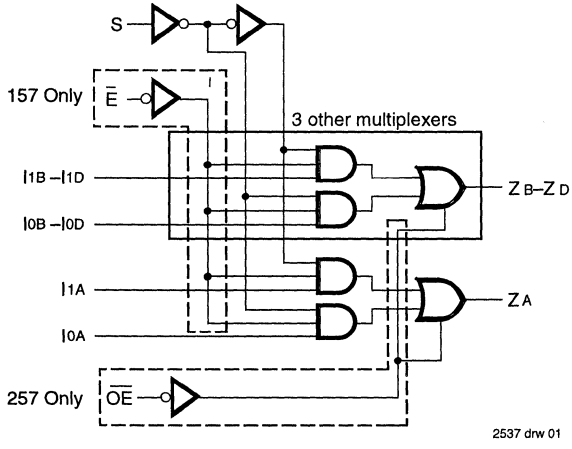
DESCRIPTION:

The IDT54/74FCT157T/AT/CT/DT and IDT54/74FCT257T/AT/CT/DT are high-speed quad 2-input multiplexers built using an advanced dual metal CMOS technology. Four bits of data from two sources can be selected using the common select input. The four buffered outputs present the selected data in the true (non-inverting) form.

The IDT54/74FCT157T/AT/CT/DT has a common, active-LOW, enable input. When the enable input is not active, all four outputs are held LOW. A common application of 'FCT157T is to move data from two different groups of registers to a common bus. Another application is as a function generator. The 'FCT157T can generate any four of the 16 different functions of two variables with one variable common.

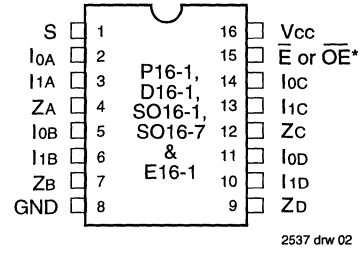
The IDT54/74FCT257T/AT/CT/DT has a common Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, all outputs are switched to a high-impedance state allowing the outputs to interface directly with bus-oriented systems.

FUNCTIONAL BLOCK DIAGRAM



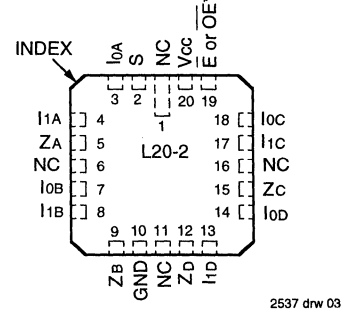
2537 drw 01

PIN CONFIGURATIONS



2537 drw 02

DIP/SOIC/QSOP/CERPACK
TOP VIEW



2537 drw 03

LCC
TOP VIEW

* $\overline{E}$ for FCT157, $\overline{OE}$ for FCT257.

PIN DESCRIPTION

Pin Names	Description
I_{0A}–I_{0D}	Source 0 Data Inputs
I_{1A}–I_{1D}	Source 1 Data Inputs
$\overline{E}$	Enable Input (Active LOW)–FCT157T
$\overline{OE}$	Output Enable (Active LOW)–FCT257T
S	Select Input
Z_A–Z_D	Outputs

2537 tbl 01

FUNCTION TABLE[1]

Inputs				Output Z_N	
$\overline{E}/\overline{OE}$	S	I_0	I_1	157	257
H	X	X	X	L	Z
L	H	X	L	L	L
L	H	X	H	H	H
L	L	L	X	L	L
L	L	H	X	H	H

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

2537 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:

2537 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

2537 lnk 04

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output[4]	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	Current		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA MIL.	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.				
			I_{OH} = –12mA MIL.	2.0	3.0	—	V
			I_{OH} = –15mA COM'L.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 32mA MIL.	—	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA COM'L.				
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.
5. This parameter is guaranteed but not tested.

2537 tbl 05

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = Vcc V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_O = 10MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.5	
		V_{IN} = Vcc Outputs Open f_O = 2.5MHz 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND Four Bits Toggling	V_{IN} = Vcc V_{IN} = GND	—	1.5	3.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	2.5	7.5[5]	

2537 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – FCT157T/AT/CT/DT

			54/74FCT157T				54/74FCT157AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay In to Zn	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	7.0	1.5	5.0	1.5	5.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Zn		1.5	10.5	1.5	12.0	1.5	6.0	1.5	7.4	ns
t_{PLH} t_{PHL}	Propagation Delay S to Zn		1.5	10.5	1.5	12.0	1.5	7.0	1.5	8.1	ns

2537 tbl 07

			54/74FCT157CT				54/74FCT157DT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay In to Zn	C_L = 50pF R_L = 500Ω	1.5	4.3	1.5	5.0	1.5	3.9	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Zn		1.5	4.8	1.5	5.9	1.5	4.4	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay S to Zn		1.5	5.2	1.5	6.0	1.5	4.6	—	—	ns

2537 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE – FCT257T/AT/CT/DT

			54/74FCT257T				54/74FCT257AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay In to Zn	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	7.0	1.5	5.0	1.5	5.8	ns
t_{PLH} t_{PHL}	Propagation Delay S to Zn		1.5	10.5	1.5	12.0	1.5	7.0	1.5	8.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.5	1.5	10.0	1.5	7.0	1.5	8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	6.0	1.5	8.0	1.5	5.5	1.5	5.8	ns

2537 tbl 09

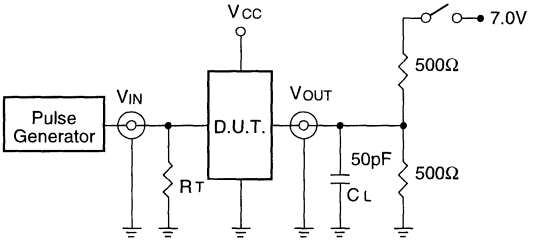
			54/74FCT257CT				54/74FCT257DT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay In to Zn	C_L = 50pF R_L = 500Ω	1.5	4.3	1.5	5.0	1.5	3.9	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay S to Zn		1.5	5.2	1.5	6.0	1.5	4.4	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	6.0	1.5	6.8	1.5	4.4	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.0	1.5	5.3	1.5	4.4	—	—	ns

2537 tbl 10

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delay.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2537 drw 04

SWITCH POSITION

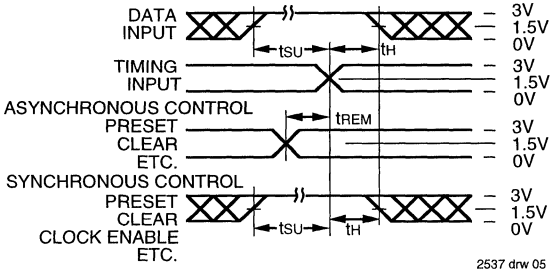
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2537 lnk 11

DEFINITIONS:

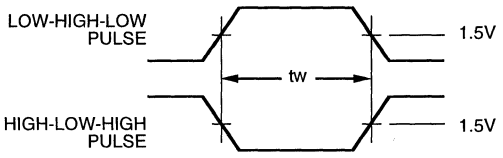
CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



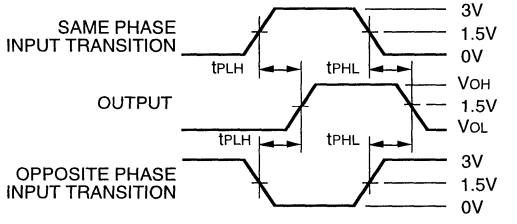
2537 drw 05

PULSE WIDTH



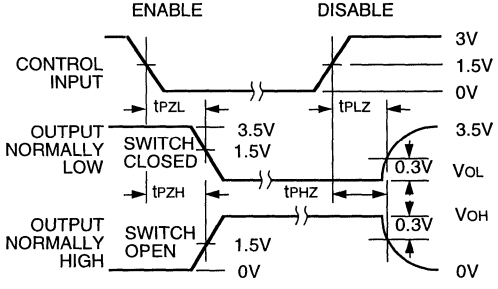
2537 drw 06

PROPAGATION DELAY



2537 drw 07

ENABLE AND DISABLE TIMES



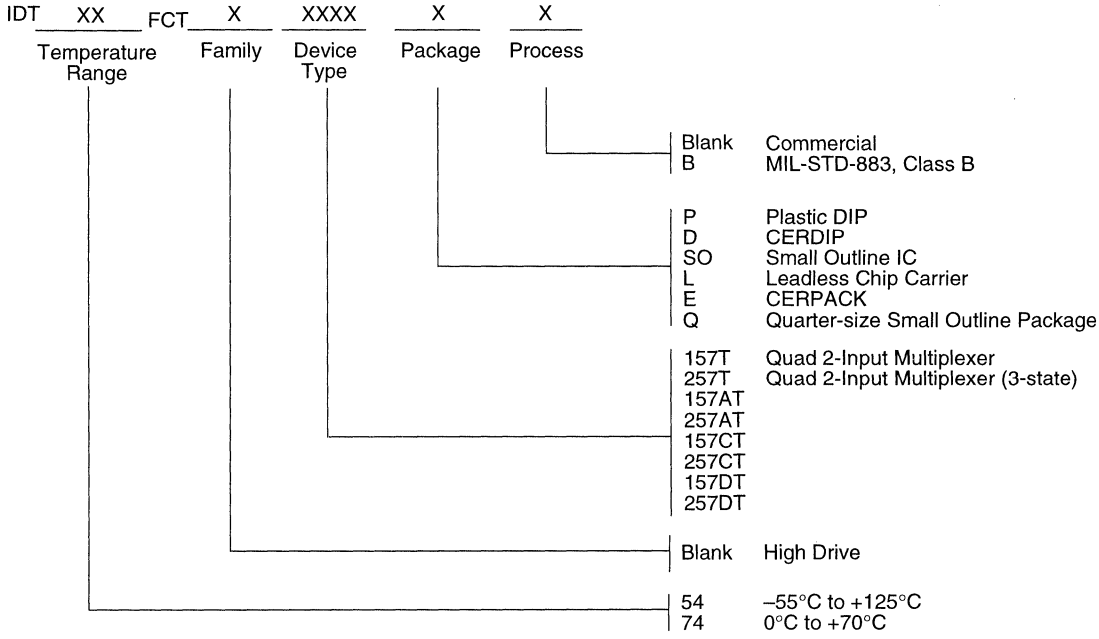
2537 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

6

ORDERING INFORMATION



2537 drw 09

Integrated Device Technology, Inc.

FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161T/AT/CT
IDT54/74FCT163T/AT/CT

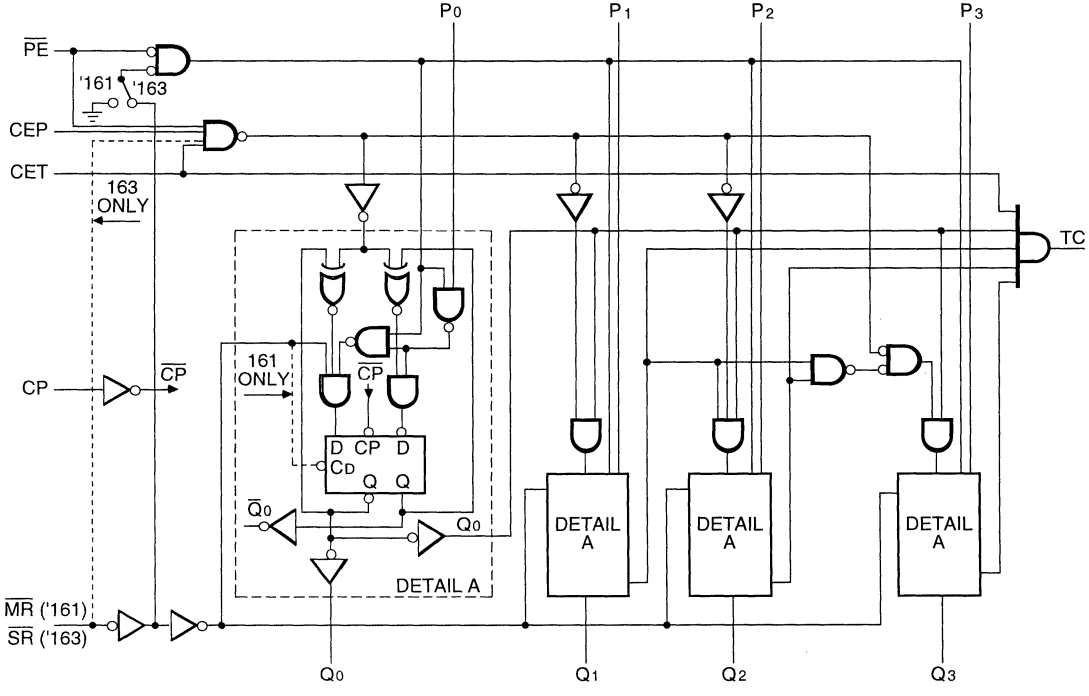
FEATURES:

- Std., A and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

DESCRIPTION:

The IDT54/74FCT161T/163T, IDT54/74FCT161AT/163AT and IDT54/74FCT161CT/163CT are high-speed synchronous modulo-16 binary counters built using an advanced dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-stage counters. The IDT54/74FCT161T/AT/CT have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163T/AT/CT have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

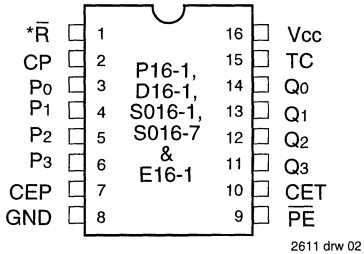
FUNCTIONAL BLOCK DIAGRAMS



2611 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

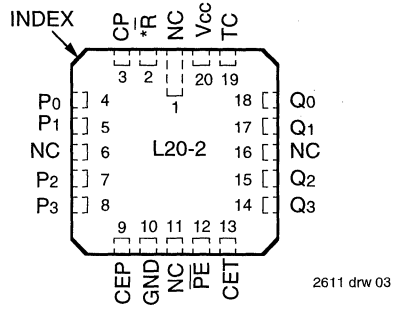
PIN CONFIGURATIONS



2611 drw 02

DIP/SOIC/QSOP/CERPACK TOP VIEW

*MR for '161
*SR for '163



2611 drw 03

LCC TOP VIEW

PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P0-3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0-3	Flip-Flop Outputs
TC	Terminal Count Output

2611 tbl 01

FUNCTION TABLE(2)

$\overline{SR}$(1)	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES: 2611 tbl 02
1. 163 only.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2611 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2611 lnk 04
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	COM'L[5]	2.0V	—	—	V
			MIL	2.7V	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL}= 32mA MIL. I_{OL}= 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2611 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.
5. Clock pin requires a minimum V_{IH} of 2.5V.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current [4]	V_{CC} = Max., Outputs Open Load Mode $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle $\overline{CEP}$ = $\overline{CET}$ = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.3[5]	

2611 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT161T IDT54/74FCT163T				IDT54/74FCT161AT IDT54/74FCT163AT				IDT54/74FCT161CT IDT54/74FCT163CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH)	CL = 50pF RL = 500Ω	2.0	11.0	2.0	11.5	2.0	7.2	2.0	7.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input LOW)		2.0	9.5	2.0	10.0	2.0	6.2	2.0	6.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to TC		2.0	15.0	2.0	16.5	2.0	9.8	2.0	10.8	2.0	7.4	2.0	8.3	ns
tPLH tPHL	Propagation Delay CET to TC		1.5	8.5	1.5	9.0	1.5	5.5	1.5	5.9	1.5	5.2	1.5	5.6	ns
tPHL	Propagation Delay $\overline{MR}$ to Qn ('161)		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.1	2.0	6.0	2.0	6.6	ns
tPHL	Propagation Delay $\overline{MR}$ to TC ('161)		2.0	11.5	2.0	12.5	2.0	7.5	2.0	8.2	2.0	7.0	2.0	7.7	ns
tSU	Set-up Time, HIGH or LOW Pn to CP		5.0	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
tH	Hold Time, HIGH or LOW Pn to CP		1.5	—	2.0	—	1.5	—	2.0	—	1.5	—	2.0	—	ns
tSU	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.5	—	13.5	—	9.5	—	11.5	—	9.5	—	11.5	—	ns
tH	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time, HIGH or LOW CEP or CET to CP		11.5	—	13.0	—	9.5	—	11.0	—	9.5	—	11.0	—	ns
tH	Hold Time, HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
tW	Clock Pulse Width (Load) HIGH or LOW		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	ns
tW	Clock Pulse Width (Count) HIGH or LOW		7.0	—	8.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns
tW	$\overline{MR}$ Pulse Width, LOW ('161)		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	ns
tREM	Recovery Time $\overline{MR}$ to CP ('161)		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

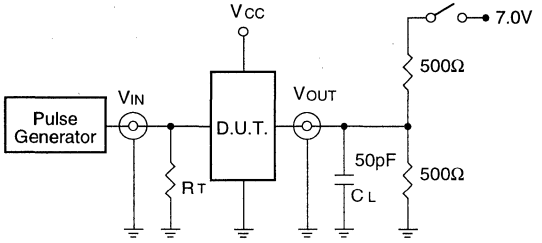
NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

2611 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2611 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

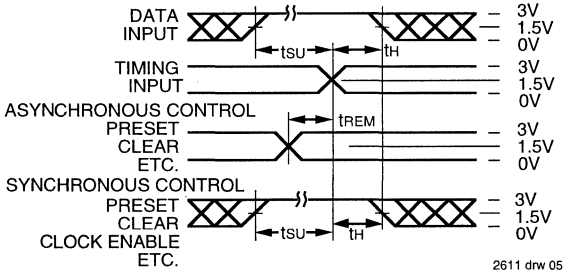
2611 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

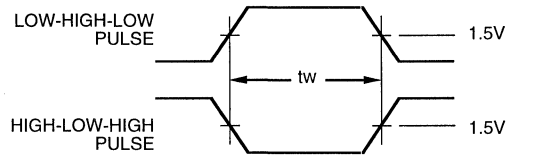
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



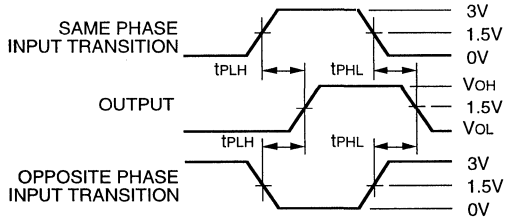
2611 drw 05

PULSE WIDTH



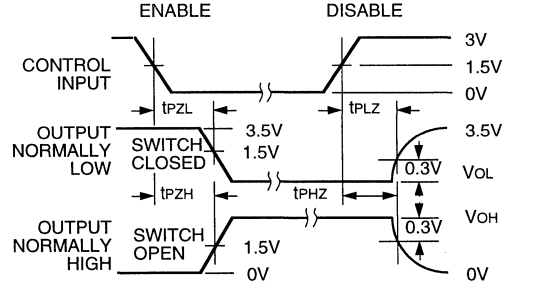
2611 drw 06

PROPAGATION DELAY



2611 drw 07

ENABLE AND DISABLE TIMES

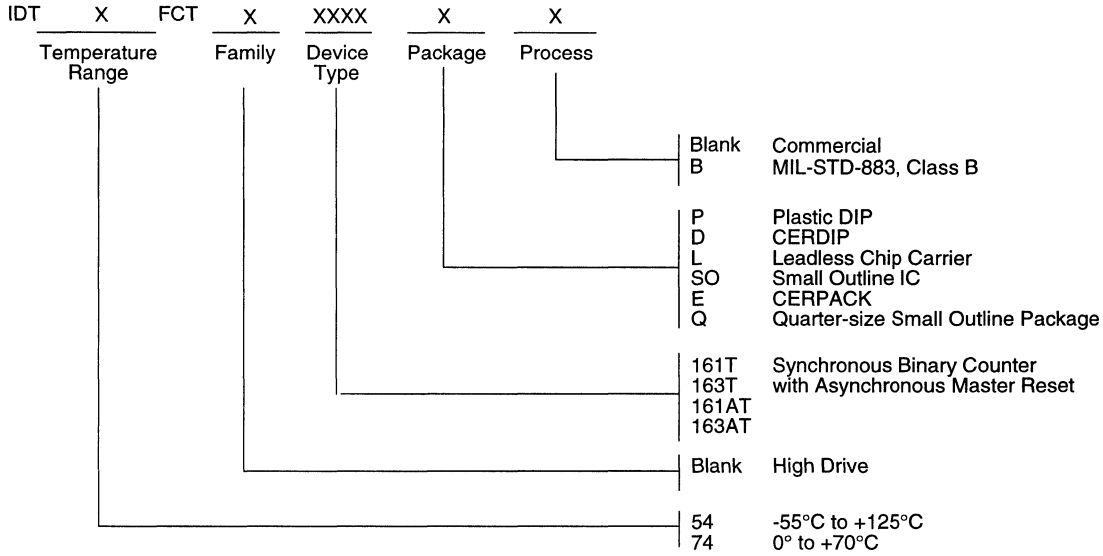


2611 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2611 drw 09

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUFFER/LINE DRIVERS

IDT54/74FCT240T/AT/CT/DT - 2240T/AT/CT
IDT54/74FCT241T/AT/CT/DT - 2241T/AT/CT
IDT54/74FCT244T/AT/CT/DT - 2244T/AT/CT
IDT54/74FCT540T/AT/CT
IDT54/74FCT541/2541T/AT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT240T/FCT241T/FCT244T/FCT540T/FCT541T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 64mA I_{OL})
- **Features for FCT2240T/FCT2241T/FCT2244T/FCT2541T:**
  - Std., A and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

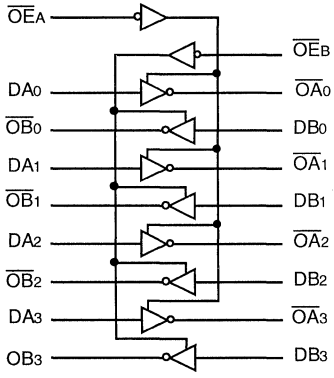
DESCRIPTION:

The IDT octal buffer/line drivers are built using an advanced dual metal CMOS technology. The FCT240T/FCT2240T, FCT241T/FCT2241T and FCT244T/FCT2244T are designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitter/receivers which provide improved board density.

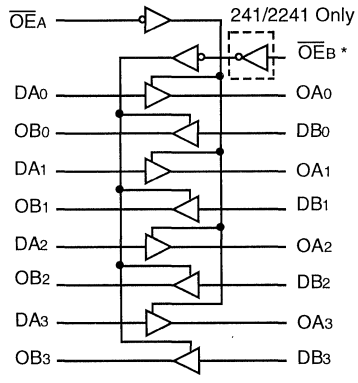
The FCT540T and FCT541T/FCT2541T are similar in function to the FCT240T/FCT2240T and FCT244T/FCT2244T, respectively, except that the inputs and outputs are on opposite sides of the package. This pinout arrangement makes these devices especially useful as output ports for microprocessors and as backplane drivers, allowing ease of layout and greater board density.

The FCT2240T, FCT2241T, FCT2244T and FCT2541T have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAMS

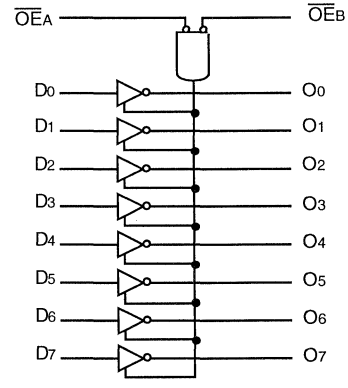


FCT240/2240T



FCT241/2241T/244/2244T

*$\overline{OE}_B$ for 241/2241T, $\overline{OE}_B$ for 244/2244T



FCT540/541/2541T

*Logic diagram shown for 'FCT540. 'FCT541/2541T is the non-inverting option.

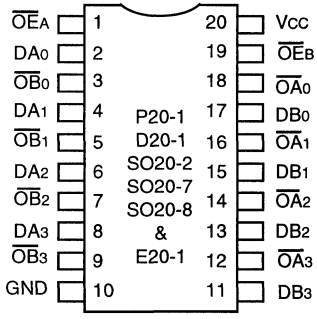
2565 drw 01

2565 drw 02

2565 drw 03

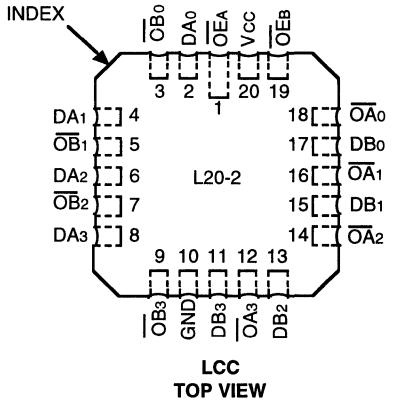
PIN CONFIGURATIONS

FCT240/2240T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

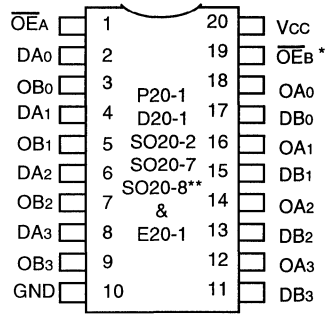
2565 drw 04



LCC
TOP VIEW

2565 drw 07

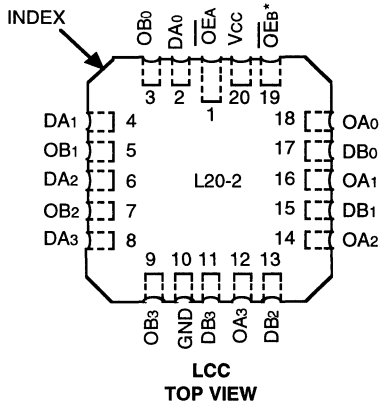
FCT241/2241T/244/2244T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

*OEB for FCT241/2241T, OEB for FCT244/2244T
**FCT244/2244T/AT/CT/DT only

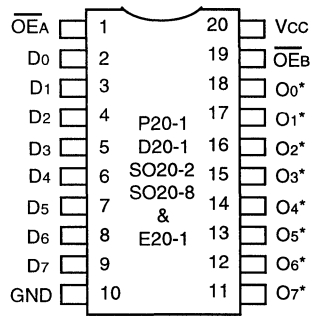
2565 drw 05



LCC
TOP VIEW

2565 drw 08

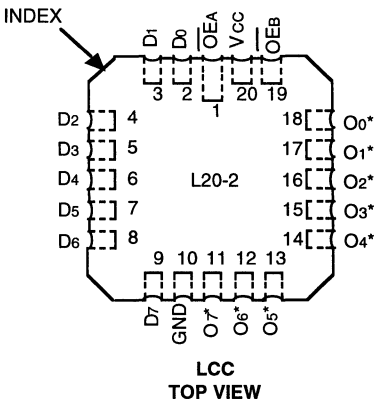
FCT540/541/2541T



DIP/SOIC/QSOP/CERPACK
TOP VIEW

*Ox for 540, Ox for 541/2541T

2565 drw 06



LCC
TOP VIEW

2565 drw 09

6

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3–State Output Enable Inputs (Active LOW)
OE_B[1]	3–State Output Enable Input (Active HIGH)
Dxx	Inputs
Oxx	Outputs

NOTE: 2565 tbl 01
1. OE_B for FCT241/2241 only.

FUNCTION TABLE

Inputs[1]				Outputs[1]				
$\overline{OE}_A$	$\overline{OE}_B$	OE_B[2]	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

NOTES: 2565 tbl 02
1. H = High Voltage Level
   X = Don't Care
   L = Low Voltage Level
   Z = High Impedance
2. OE_B for FCT 241/2241 only.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2565 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2565 lnk 04
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2565 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT240/241/244/540/541T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA

2565 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT2240/2241/2244/2541T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

2565 lnk 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND or	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
		$\overline{OE}_A$ = GND, OE_B = V_{CC} One Input Toggling 50% Duty Cycle		FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT FCT2xxxT	— —	1.5 0.6	3.5 2.2	mA
		50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND or	V_{IN} = 3.4	FCTxxxT	—	1.8	4.5	
		$\overline{OE}_A$ = GND, OE_B = V_{CC} One Bit Toggling	V_{IN} = GND	FCT2xxxT		0.9	3.2	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT FCT2xxxT	— —	3.0 1.2	6.0[5] 3.4[5]	
		50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND or	V_{IN} = 3.4	FCTxxxT	—	5.0	14.0[5]	
		$\overline{OE}_A$ = GND, OE_B = V_{CC} Eight Bits Toggling	V_{IN} = GND	FCT2xxxT	—	3.2	11.4[5]	

2565 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT240/2240T

Symbol	Parameter	Condition[1]	FCT240T FCT2240T				FCT240AT FCT2240AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DN to $\overline{O}$N	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	ns
tPZH tPZL	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	ns

2565 tbl 09

Symbol	Parameter	Condition[1]	FCT240CT FCT2240CT				FCT240DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DN to $\overline{O}$N	CL = 50pF RL = 500Ω	1.5	4.3	1.5	4.7	1.5	3.6	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.2	1.5	5.7	1.5	4.0	—	—	ns

2565 tbl 10

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT241/2241T/244/2244T

Symbol	Parameter	Condition[1]	FCT241T/244T FCT2241T/2244T				FCT241AT/244AT FCT2241AT/2244AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
tPZH tPZL	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

2565 tbl 11

Symbol	Parameter	Condition[1]	FCT241CT/244CT FCT2241CT/2244CT				FCT241DT/244DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DN to ON	CL = 50pF RL = 500Ω	1.5	4.1	1.5	4.6	1.5	3.6	—	—	ns
tPZH tPZL	Output Enable Time		1.5	5.8	1.5	6.5	1.5	4.8	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	5.2	1.5	5.7	1.5	4.0	—	—	ns

2565 tbl 12

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT540/541/2541T

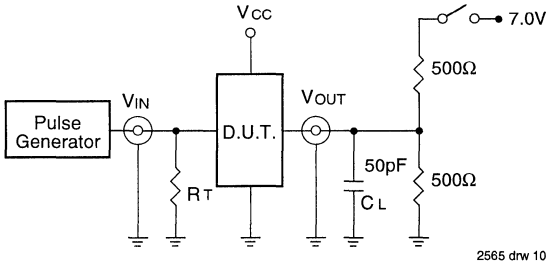
Symbol	Parameter	Condition[1]	FCT540T/541T FCT2541T				FCT540AT/541AT FCT2541AT				FCT540CT/541CT FCT2541CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O}_N$ FCT540	C_L = 50pF R_L = 500Ω	1.5	8.5	1.5	9.5	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.7	ns
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N FCT541/2541T		1.5	8.0	1.5	9.0	1.5	4.8	1.5	5.1	1.5	4.1	1.5	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	10.0	1.5	10.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	9.5	1.5	10.0	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns

2565 tbl 13

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2565 drw 10

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

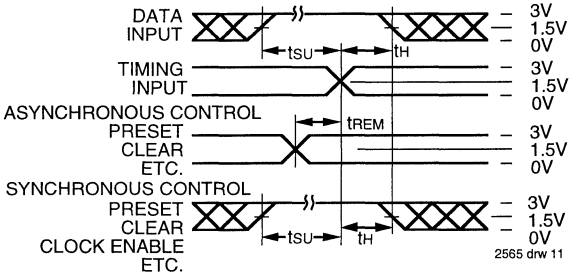
2565 drw 14

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.

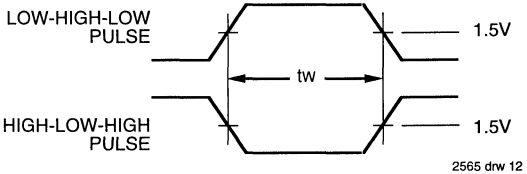
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



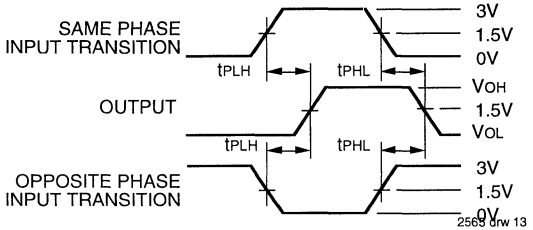
2565 drw 11

PULSE WIDTH



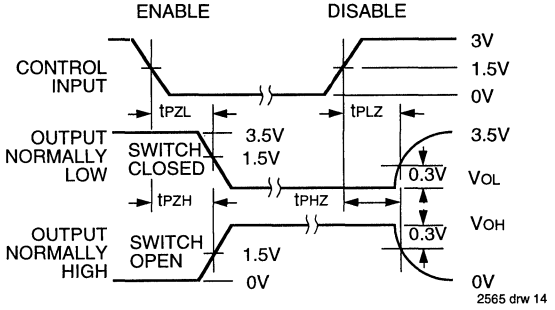
2565 drw 12

PROPAGATION DELAY



2565 drw 13

ENABLE AND DISABLE TIMES



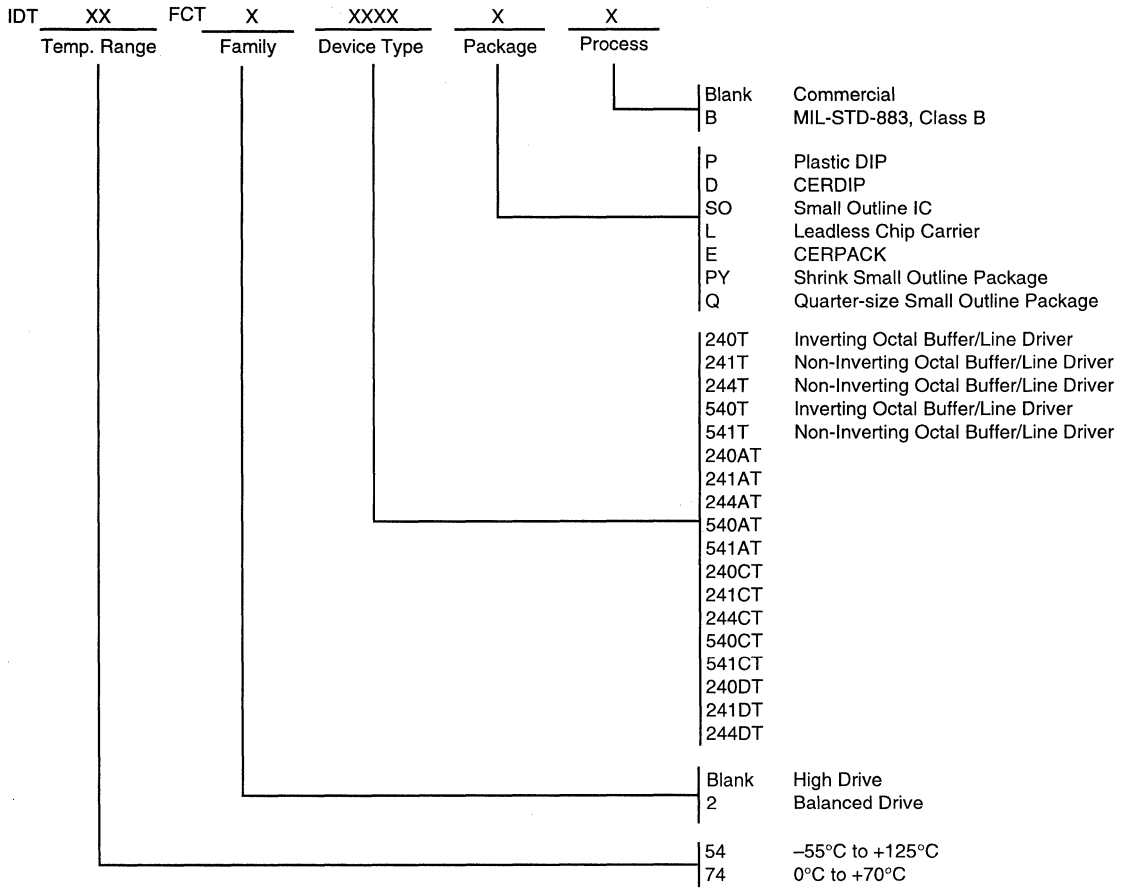
2565 drw 14

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

6

ORDERING INFORMATION



2565 drw 15

Integrated Device Technology, Inc.

FAST CMOS OCTAL BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT245T/AT/CT/DT - 2245T/AT/CT
IDT54/74FCT640T/AT/CT
IDT54/74FCT645T/AT/CT/DT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT245T/FCT640T/FCT645T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 64mA I_{OL})
- **Features for FCT2245T:**
  - Std., A and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

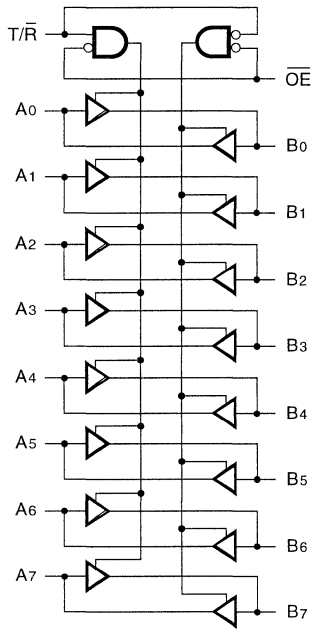
DESCRIPTION:

The IDT octal bidirectional transceivers are built using an advanced dual metal CMOS technology. The FCT245T/FCT2245T, FCT640T and FCT645T are designed for asynchronous two-way communication between data buses. The transmit/receive (T/$\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The FCT245T/FCT2245T and FCT645T transceivers have non-inverting outputs. The FCT640T has inverting outputs.

The FCT2245T has balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times- reducing the need for external series terminating resistors. The FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

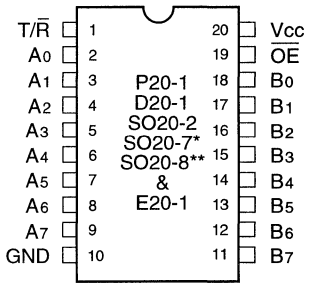
FUNCTIONAL BLOCK DIAGRAM



FCT245T/2245T, FCT645T are non-inverting options.
FCT640T is the inverting options.

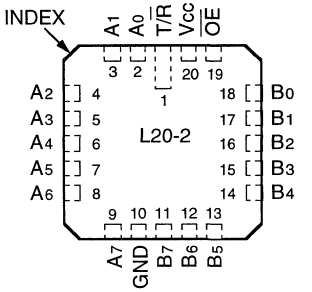
2539 drw 01

PIN CONFIGURATIONS



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW
*FCT245T/2245T, FCT645T only.
**FCT245T/2245T, FCT640T

2539 drw 02



LCC
TOP VIEW

2539 drw 03

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-State Outputs
B_0-B_7	Side B Inputs or 3-State Outputs

2539 tbl 01

FUNCTION TABLE(2)

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A(1)
L	H	Bus B Data to Bus B(1)
H	X	High Z State

2539 tbl 02

NOTES:
1. 640 is inverting from input to output.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2539 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (TA = +25°C, F = 1.0MHZ)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2539 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2539 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT245T/640T/645T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA

2539 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT2245T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

2539 lnk 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = T/$\overline{R}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_i = 10MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND One Bit Toggling	V_{IN} = V_{CC}	FCTxxxT	—	1.5	3.5	mA
			V_{IN} = GND	FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4	FCTxxxT	—	1.8	4.5	
			V_{IN} = GND	FCT2xxxT		0.9	3.2	
		V_{CC} = Max. Outputs Open f_i = 2.5MHz 50% Duty Cycle $\overline{OE}$ = T/$\overline{R}$ = GND Eight Bits Toggling	V_{IN} = V_{CC}	FCTxxxT	—	3.0	6.0[5]	
			V_{IN} = GND	FCT2xxxT	—	1.2	3.4[5]	
			V_{IN} = 3.4	FCTxxxT	—	5.0	14.0[5]	
			V_{IN} = GND	FCT2xxxT	—	3.2	11.4[5]	

2539 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT245T FCT2245T				FCT245AT FCT2245AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns

2534 tbl 09

Symbol	Parameter	Conditions[1]	FCT245CT FCT2245CT				FCT245DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	1.5	4.1	1.5	4.5	1.5	3.8	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		1.5	5.8	1.5	6.2	1.5	5.0	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		1.5	4.8	1.5	5.2	1.5	4.3	—	—	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	5.8	1.5	6.2	1.5	5.0	—	—	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	4.8	1.5	5.2	1.5	4.3	—	—	ns

2534 tbl 10

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT640T				FCT640AT				FCT640CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay A to B, B to A	CL = 50 pF RL = 500Ω	2.0	7.0	2.0	8.0	1.5	5.0	1.5	5.3	1.5	4.4	1.5	4.7	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to A or B		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to A or B		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns
tPZH tPZL	Output Enable Time T/$\overline{R}$ to A or B[3]		2.0	13.0	2.0	16.0	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.2	ns
tPHZ tPLZ	Output Disable Time T/$\overline{R}$ to A or B[3]		2.0	10.0	2.0	12.0	1.5	5.0	1.5	6.0	1.5	4.8	1.5	5.2	ns

NOTES:

2534 tbl 11

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT645T				FCT645AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	1.5	9.5	1.5	11.0	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	11.0	1.5	12.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	12.0	1.5	13.0	1.5	5.0	1.5	6.0	ns

2534 tbl 12

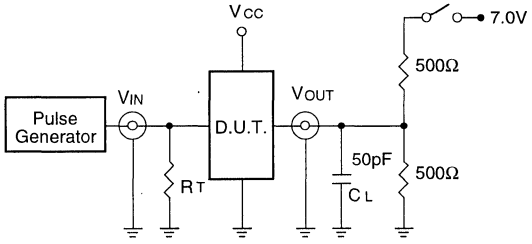
Symbol	Parameter	Conditions[1]	FCT645CT				FCT645DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50 pF R_L = 500Ω	1.5	4.1	1.5	4.5	1.5	3.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	5.8	1.5	6.2	1.5	5.0	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	4.8	1.5	5.2	1.5	4.3	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time T/$\overline{R}$ to A or B[3]		1.5	5.8	1.5	6.2	1.5	5.0	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time T/$\overline{R}$ to A or B[3]		1.5	4.8	1.5	5.2	1.5	4.3	—	—	ns

2534 tbl 13

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2534 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

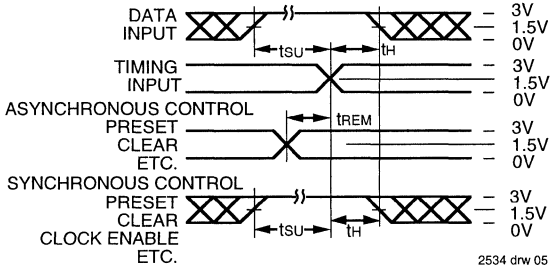
2534 lnk 14

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

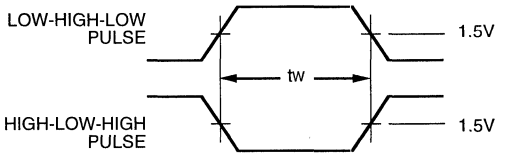
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



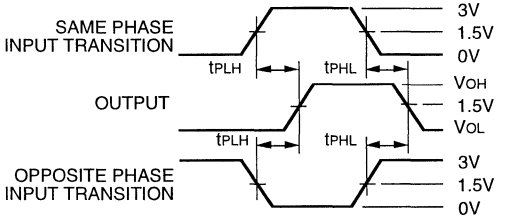
2534 drw 05

PULSE WIDTH



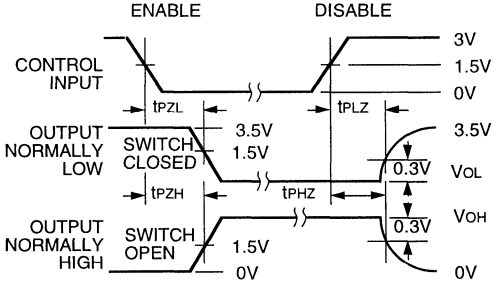
2534 drw 06

PROPAGATION DELAY



2534 drw 07

ENABLE AND DISABLE TIMES



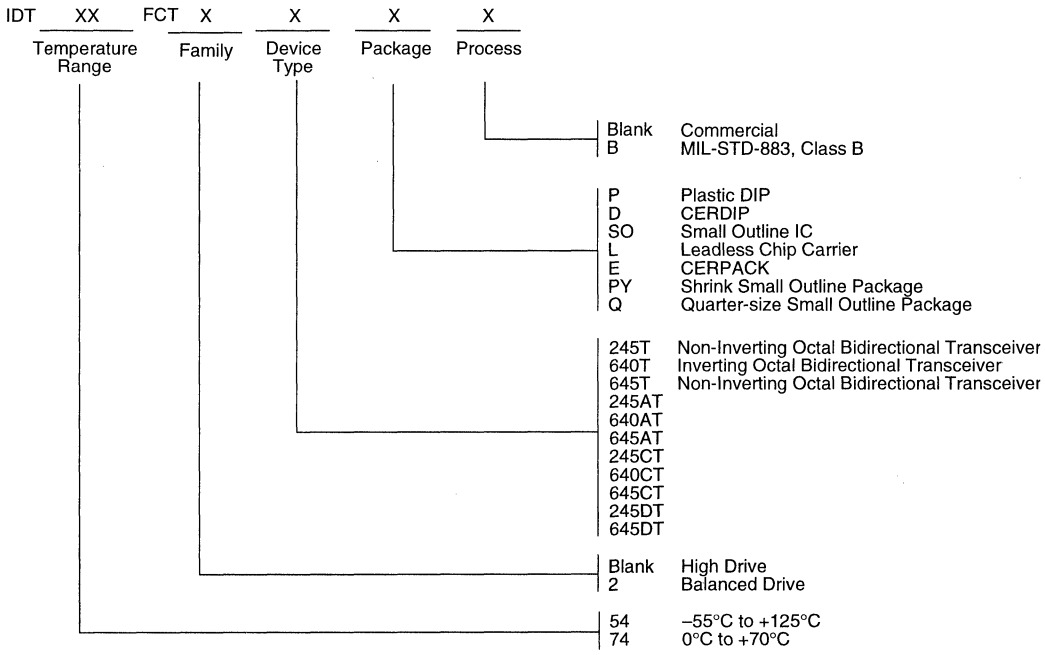
2534 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

6

ORDERING INFORMATION



2539 drw 09

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH MASTER RESET

IDT54/74FCT273T/AT/CT

FEATURES:

- Std., A, and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

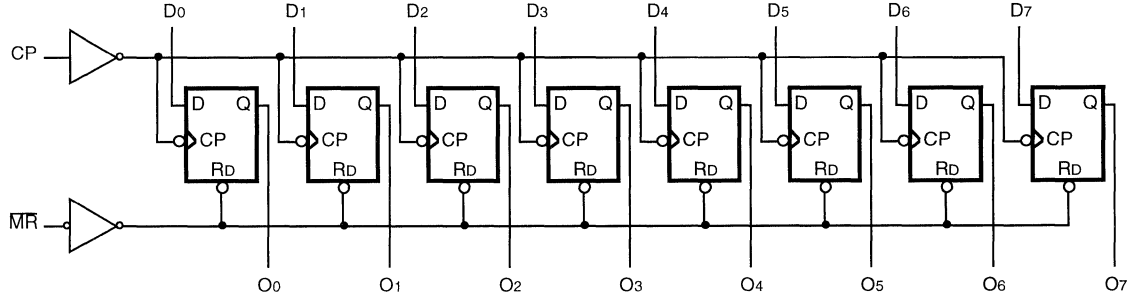
DESCRIPTION:

The IDT54/74FCT273T/AT/CT are octal D flip-flops built using an advanced dual metal CMOS technology. The IDT54/74FCT273T/AT/CT have eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output.

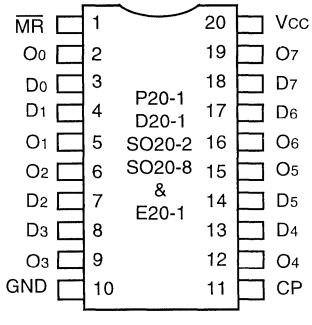
All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

FUNCTIONAL BLOCK DIAGRAM



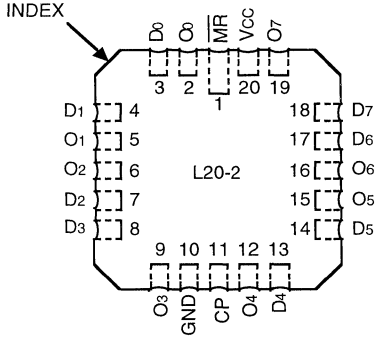
2568 drw 03

PIN CONFIGURATIONS



2568 drw 01

DIP/SOIC/QSOP/CERPACK TOP VIEW



2568 drw 02

LCC TOP VIEW

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
D_N	Data Inputs
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
O_N	Data Outputs

2568 tbl 01

FUNCTION TABLE[1]

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

NOTE: 2568 tbl 02

1. H = HIGH voltage level steady state
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
   L = LOW voltage level steady state
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2568 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2568 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2568 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test parameter for this parameter is ±5µA at T_A = -55°C.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{MR}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
		$\overline{MR}$ = V_{CC} One Bit Toggling at fi = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
		$\overline{MR}$ = V_{CC} Eight Bits Toggling at fi = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.0	16.3[5]	

2568 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT273T				IDT54/74FCT273AT				IDT54/74FCT273CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	5.8	2.0	6.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to O_N		2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	2.0	6.1	2.0	6.8	ns
t_{SU}	Set-up Time HIGH or LOW D_N to CP		3.0	—	3.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_N to CP		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns
t_{REM}	Recovery Time $\overline{MR}$ to CP		4.0	—	5.0	—	2.0	—	2.5	—	2.0	—	2.5	—	ns

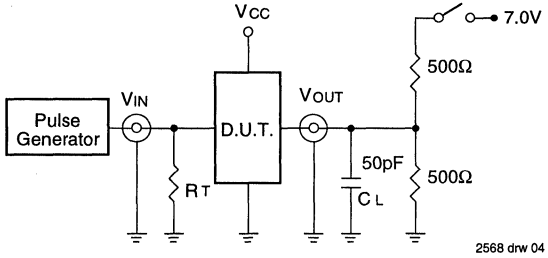
2568 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2568 drw 04

SWITCH POSITION

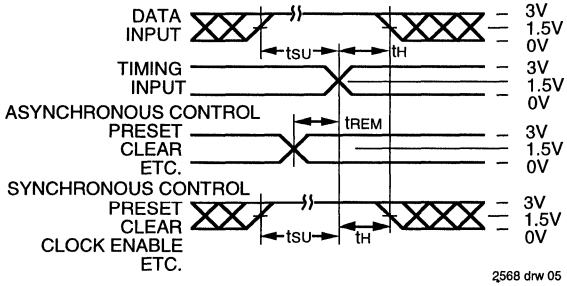
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2568 lnk 08

DEFINITIONS:

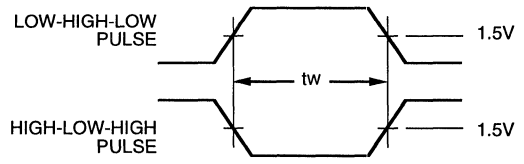
CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



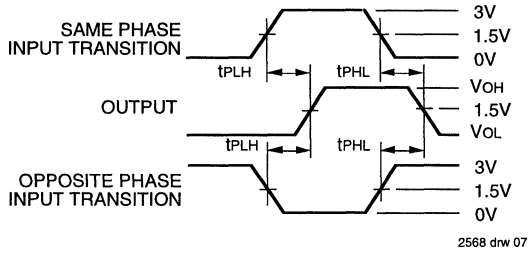
2568 drw 05

PULSE WIDTH



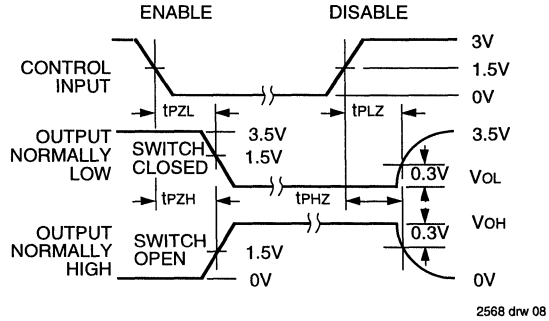
2568 drw 06

PROPAGATION DELAY



2568 drw 07

ENABLE AND DISABLE TIMES

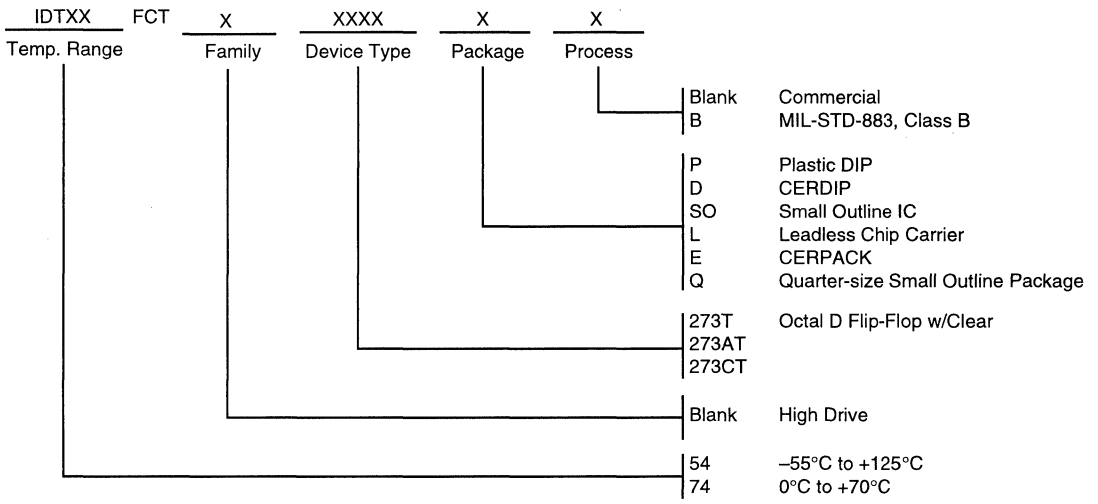


2568 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

ORDERING INFORMATION



2568 drw 09

6

Integrated Device Technology, Inc.

FAST CMOS 8-INPUT UNIVERSAL SHIFT REGISTER

IDT54/74FCT299T/AT/CT

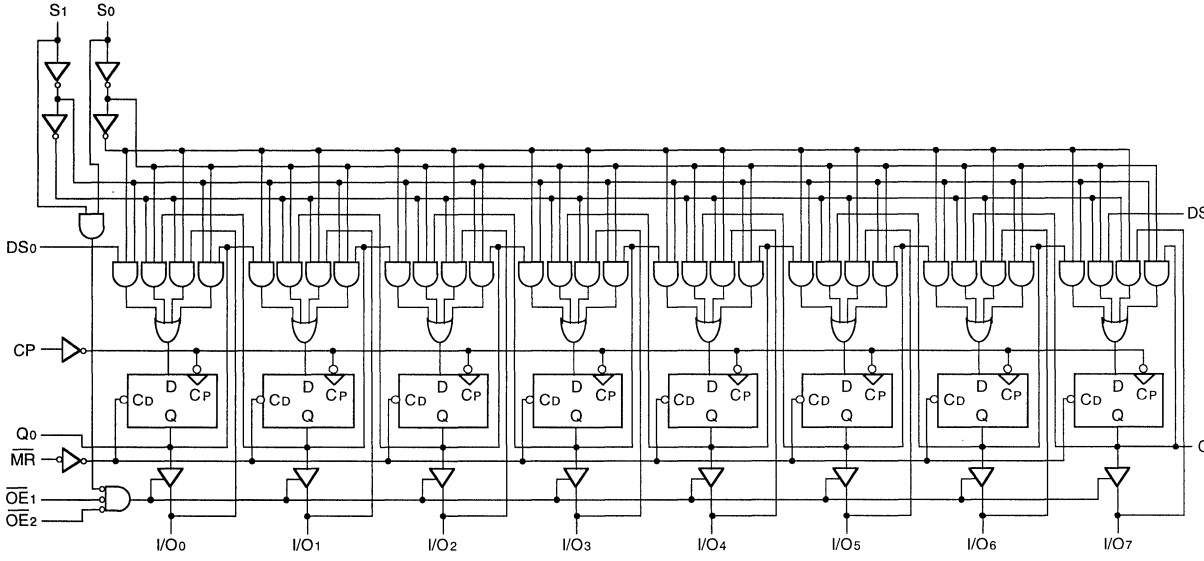
FEATURES:

- Std., A and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

DESCRIPTION:

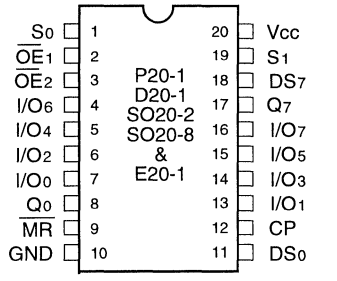
The IDT54/74FCT299T/AT/CT are built using an advanced dual metal CMOS technology. The IDT54/74FCT299T/AT/CT are 8-input universal shift/storage registers with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

FUNCTIONAL BLOCK DIAGRAM



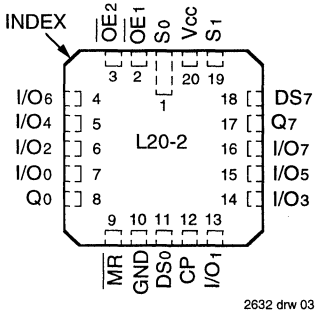
2632 drw 01

PIN CONFIGURATIONS



2632 drw 02

DIP/SOIC/QSOP/CERPACK
TOP VIEW



2632 drw 03

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
CP	Clock Pulse Input (Active Edge Rising)
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE_1}$, $\overline{OE_2}$	3-State Output Enable Inputs (Active LOW)
I/O_0–I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
O_0, O_7	Serial Outputs

2632 tbl 01

FUNCTION TABLE[1]

Inputs				
$\overline{MR}$	S_1	S_0	CP	Response
L	X	X	X	Asynchronous Reset Q_0–Q_7 = LOW
H	H	H	↑	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↑	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	↑	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

2632 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2632 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2632 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max., V_I = 2.7V		—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max., V_I = 0.5V		—	—	±1	µA
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = Vcc (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.,[3] V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH}= –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2632 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current [4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_1 = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current [6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND $\overline{MR}$ = V_{CC} S_0 = S_1 = V_{CC} DS_0 = DS_7 = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.0	16.3[5]	

2632 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

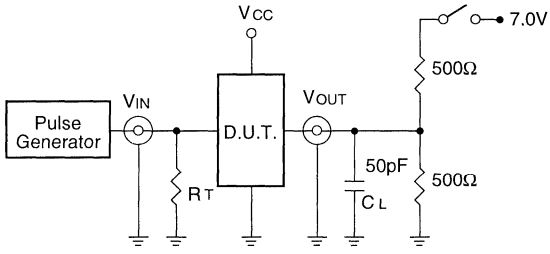
Symbol	Parameter	Condition[1]	IDT54/74FCT299T				IDT54/74FCT299AT				IDT54/74FCT299CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_0 or Q_7	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	14.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/On		2.0	12.0	2.0	12.0	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7		2.0	10.0	2.0	10.5	2.0	7.2	2.0	9.5	2.0	6.5	2.0	7.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/On		2.0	15.0	2.0	15.0	2.0	8.7	2.0	11.5	2.0	6.5	2.0	7.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$n to I/On		1.5	11.0	1.5	15.0	1.5	6.5	1.5	7.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$n to I/On		1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	1.5	6.0	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW S_0 or S_1 to CP		7.5	—	7.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
t_{SU}	Set-up Time HIGH or LOW I/On, DS_0 or DS_7 to CP		5.5	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
t_H	Hold Time HIGH or LOW S_0 or S_1 to CP		1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_H	Hold Time HIGH or LOW I/On, DS_0 or DS_7 to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
t_W	$\overline{MR}$ Pulse Width LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns
t_{REM}	Recovery Time		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum units are guaranteed but not tested on Propagation Delays.

2619 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2632 drw 04

SWITCH POSITION

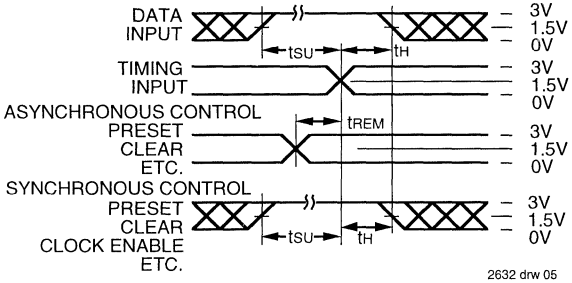
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2632 lnk 08

DEFINITIONS:

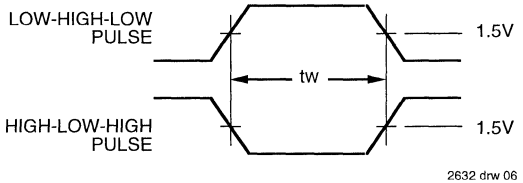
C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



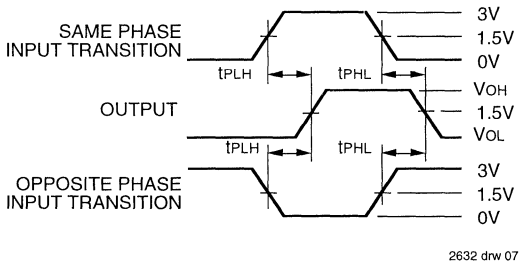
2632 drw 05

PULSE WIDTH



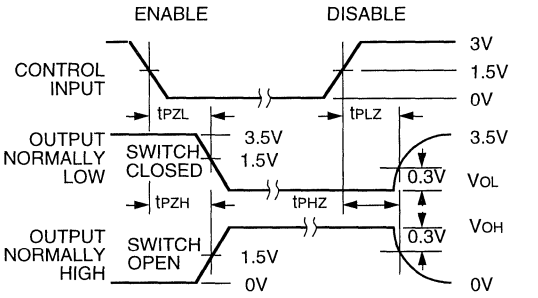
2632 drw 06

PROPAGATION DELAY



2632 drw 07

ENABLE AND DISABLE TIMES



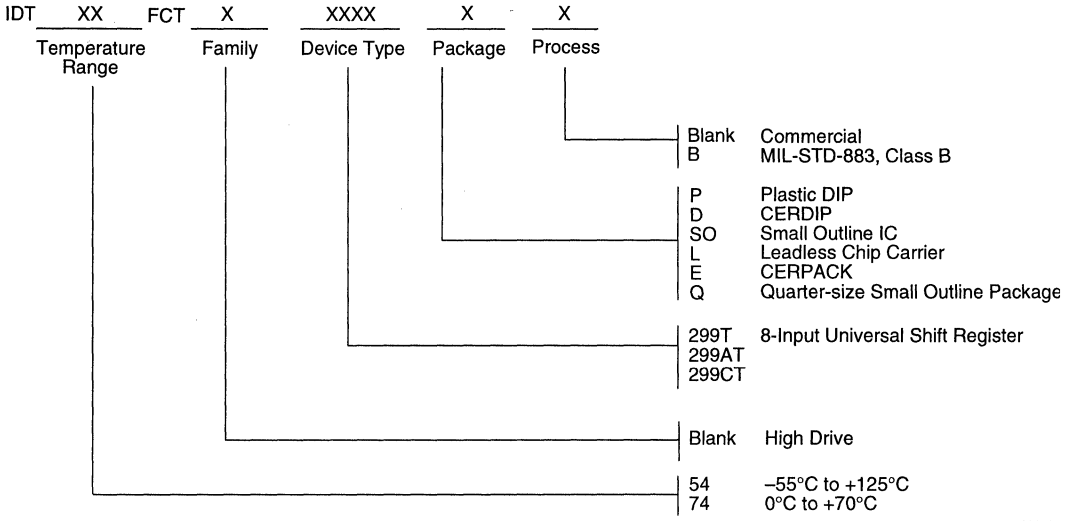
2632 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

6

ORDERING INFORMATION



2632 drw 09

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT373T/AT/CT/DT - 2373T/AT/CT
IDT54/74FCT533T/AT/CT
IDT54/74FCT573T/AT/CT/DT - 2573T/AT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT373T/FCT533T/FCT573T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 48mA I_{OL})
  - Power off disable outputs permit "live insertion"
- **Features for FCT2373T/FCT2573T:**
  - Std., A and C speed grades
  - Resistor output (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

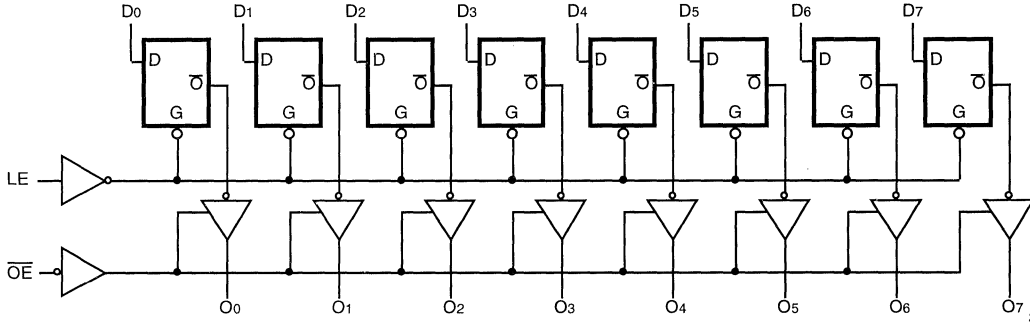
DESCRIPTION:

The FCT373T/FCT2373T, FCT533T and FCT573T/FCT2573T are octal transparent latches built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high- impedance state.

The FCT2373T and FCT2573T have balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

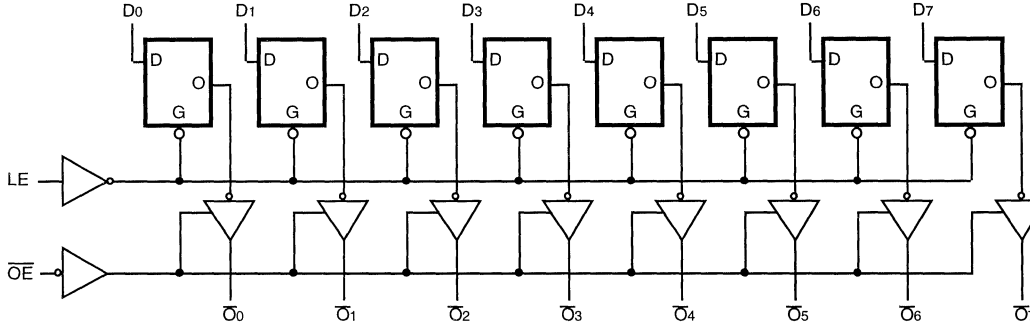
6

FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT373T/2373T AND IDT54/74FCT573T/2573T



2564 cnv* 01

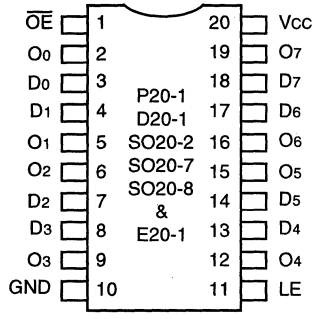
FUNCTIONAL BLOCK DIAGRAM IDT54/74FCT533T



2564 cnv* 02

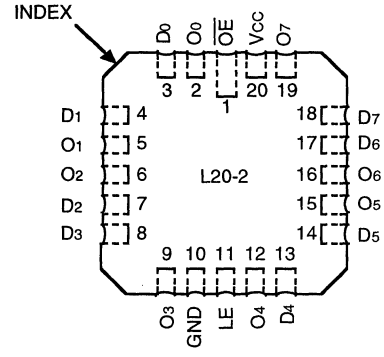
PIN CONFIGURATIONS

IDT54/74FCT373/2373T



2564 cnv* 03

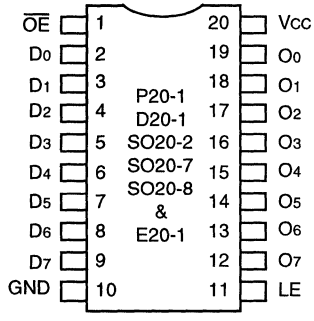
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



2564 cnv* 04

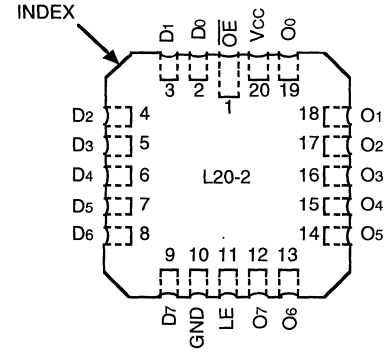
LCC
TOP VIEW

IDT54/74FCT573/2573T



2564 cnv* 05

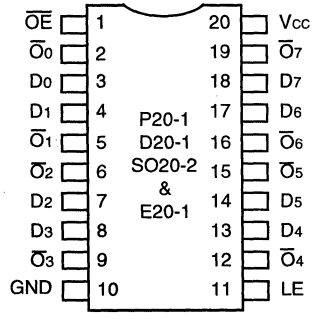
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



2564 cnv* 06

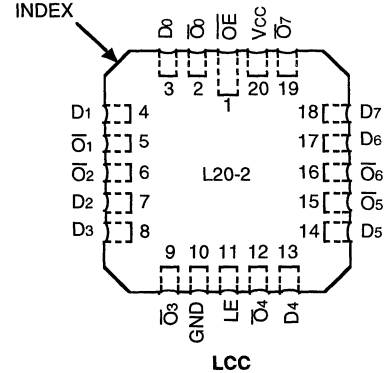
LCC
TOP VIEW

IDT54/74FCT533



2564 cnv* 07

DIP/SOIC/CERPACK
TOP VIEW



2564 cnv* 08

LCC
TOP VIEW

FUNCTION TABLE (533)[1]

Inputs			Outputs
D_N	LE	$\overline{OE}$	$\overline{O}_N$
H	H	L	L
L	H	L	H
X	X	H	Z

2564 tbl 01

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

FUNCTION TABLE (373 and 573)[1]

Inputs			Outputs
D_N	LE	$\overline{OE}$	O_N
H	H	L	H
L	H	L	L
X	X	H	Z

2564 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
D_N	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_N	3-State Outputs
$\overline{O}_N$	Complementary 3-State Outputs

2564 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2564 lnk 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2564 lnk 05

NOTE:
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2564 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT373T/533T/573T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

2564 lnk 07

OUTPUT DRIVE CHARACTERISTICS FOR FCT2373T/2573T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

2564 lnk 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
				FCTxxxT	—	1.8	4.5	
				FCT2xxxT		0.9	3.2	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	3.0	6.0[5]	
				FCT2xxxT	—	1.2	3.4[5]	
				FCTxxxT	—	5.0	14.0[5]	
				FCT2xxxT	—	3.2	11.4[5]	

2564 tbl 09

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			FCT373T/2373T/573T/2573T				FCT373AT/2373AT/573AT/2573AT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Conditions[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	ns

2564 tbl 10

			FCT373CT/2373CT/573CT/2573CT				FCT373DT/573DT				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Conditions[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	4.2	1.5	5.1	1.5	3.8	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		2.0	5.5	2.0	8.0	2.0	4.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.5	1.5	6.3	1.5	4.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.0	1.5	5.9	1.5	4.0	—	—	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to LE		2.0	—	2.0	—	1.5	—	—	—	ns
t_H	Hold Time HIGH or LOW, D_N to LE		1.5	—	1.5	—	1.0	—	—	—	ns
t_W	LE Pulse Width HIGH[3]		5.0	—	6.0	—	3.0	—	—	—	ns

2564 tbl 11

			FCT533T				FCT533AT				FCT533CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Conditions[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to $\overline{O_N}$	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	12.0	1.5	5.2	1.5	5.6	1.5	4.2	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O_N}$		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.8	2.0	5.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	11.0	1.5	12.5	1.5	6.5	1.5	7.5	1.5	5.5	1.5	6.3	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	8.5	1.5	5.5	1.5	6.5	1.5	5.0	1.5	5.9	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to LE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to LE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

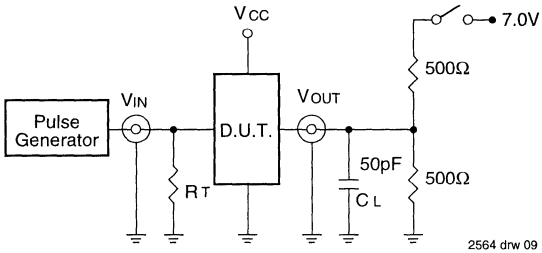
NOTES:

2564 tbl 12

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2564 drw 09

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

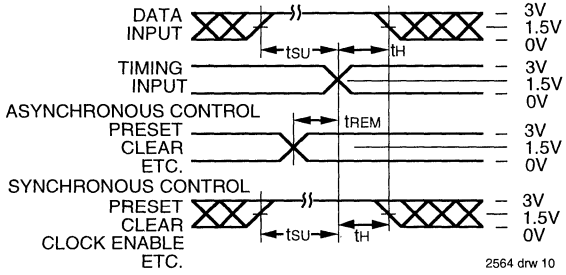
2564 lnk 13

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.

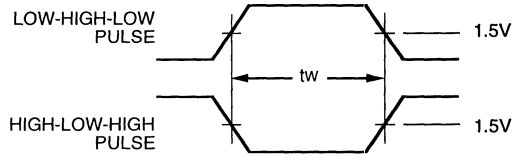
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



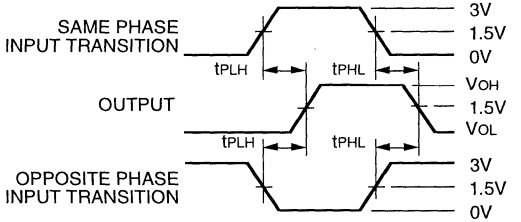
2564 drw 10

PULSE WIDTH



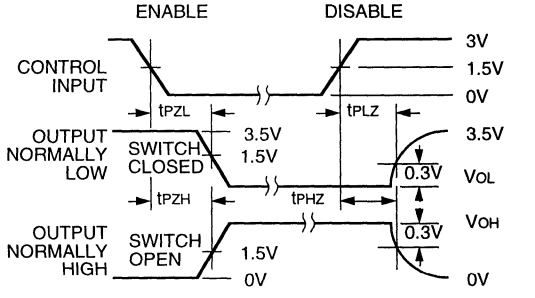
2564 drw 11

PROPAGATION DELAY



2564 drw 12

ENABLE AND DISABLE TIMES



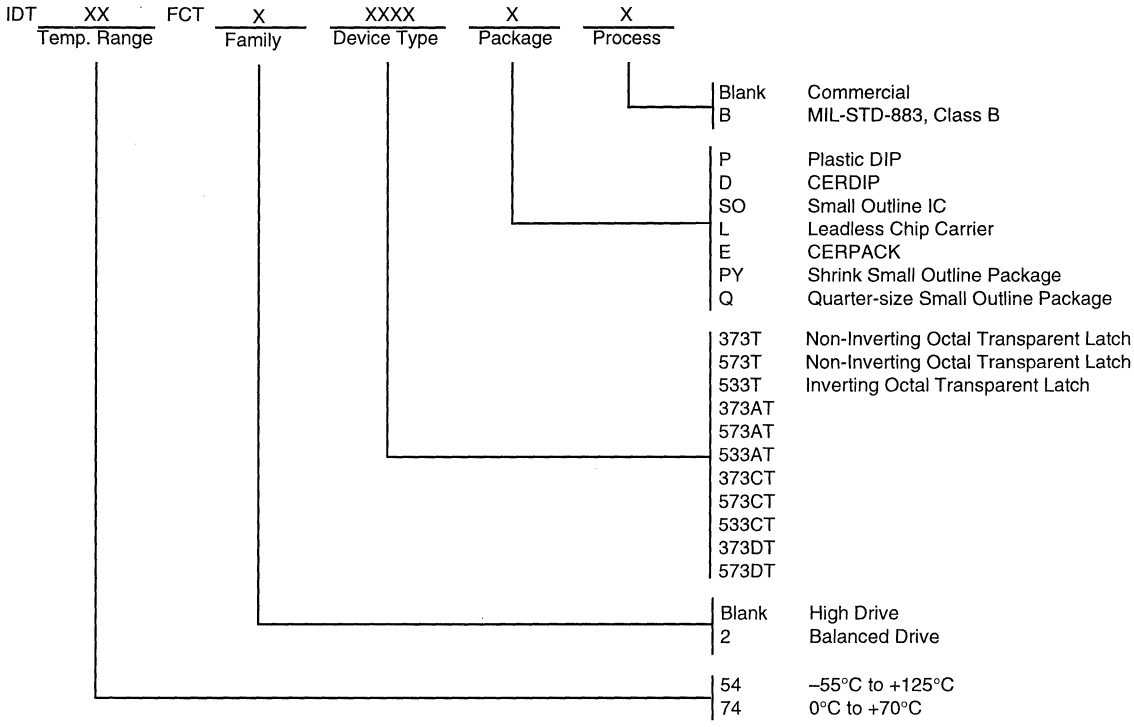
2564 drw 13

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

6

ORDERING INFORMATION



2564 drw 14

Integrated Device Technology, Inc.

FAST CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT374T/AT/CT/DT - 2374T/AT/CT
IDT54/74FCT534T/AT/CT
IDT54/74FCT574T/AT/CT/DT - 2574T/AT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT374T/FCT534T/FCT574T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- **Features for FCT2374T/FCT2574T:**
  - Std., A, and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

DESCRIPTION

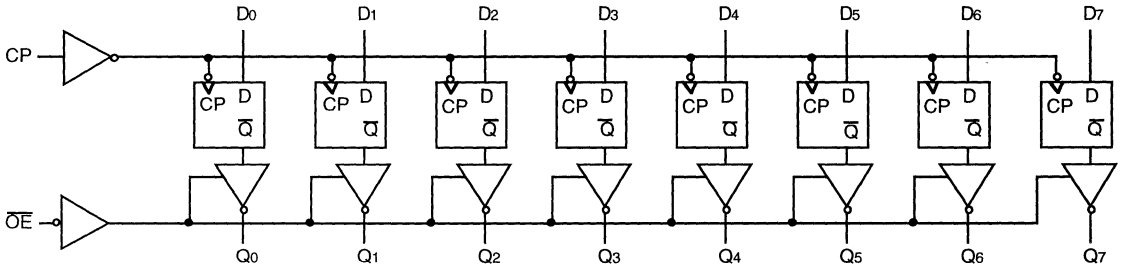
The FCT374T/FCT2374T, FCT534T and FCT574T/FCT2574T are 8-bit registers built using an advanced dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance state.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

The FCT2374T and FCT2574T have balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

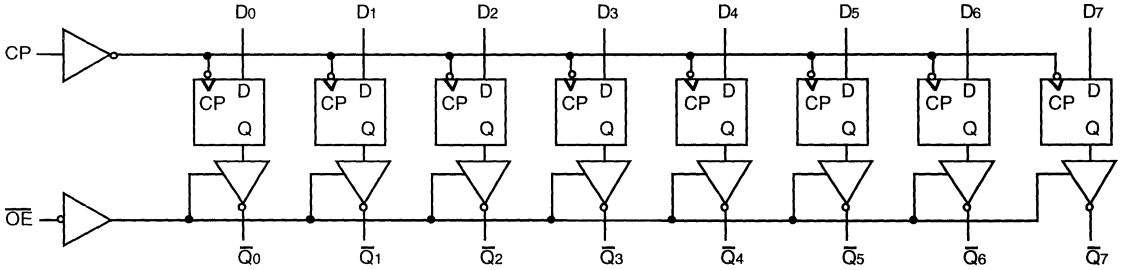
6

FUNCTIONAL BLOCK DIAGRAM FCT374/FCT2374T AND FCT574/FCT2574T



2569 drw 01

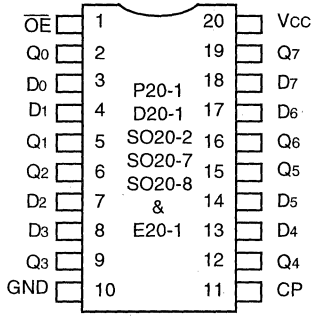
FUNCTIONAL BLOCK DIAGRAM FCT534T



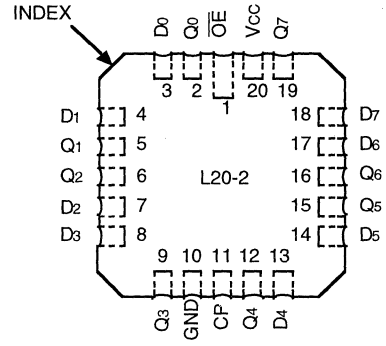
2569 drw 02

PIN CONFIGURATIONS

IDT54/74FCT374T



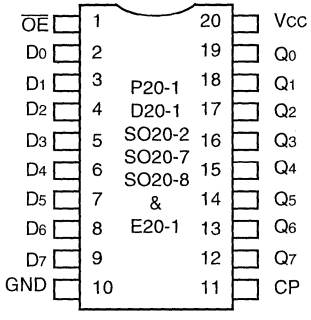
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



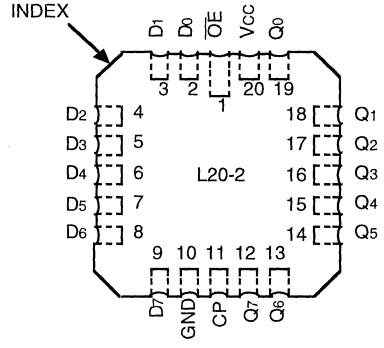
2569 drw 03

LCC
TOP VIEW

IDT54/74FCT574T



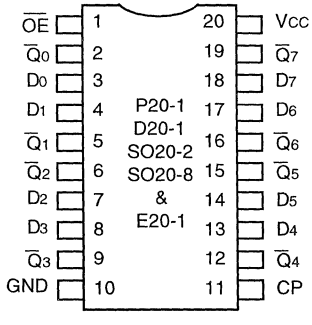
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



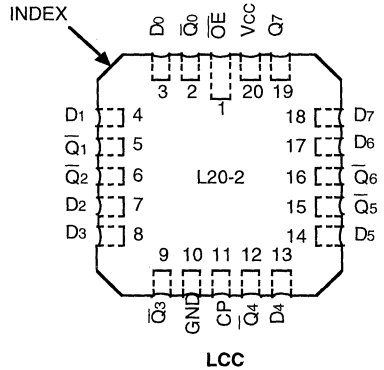
2569 drw 04

LCC
TOP VIEW

IDT54/74FCT534T



DIP/SOIC/QSOP/CERPACK
TOP VIEW



2569 drw 05

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
D_N	D flip-flop data inputs
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
Q_N	3-state outputs, (true)
$\overline{Q}_N$	3-state outputs, (inverted)
$\overline{OE}$	Active LOW 3-state Output Enable input

2569 tbl 01

FUNCTION TABLE[1]

	Inputs			534		374/574	
				Outputs	Internal	Outputs	Internal
Function	$\overline{OE}$	CP	D_N	$\overline{Q}_N$	Q_N	Q_N	$\overline{Q}_N$
HI-Z	H	L	X	Z	NC	Z	NC
	H	H	X	Z	NC	Z	NC
LOAD REGISTER	L	↑	L	H	L	L	H
	L	↑	H	L	H	H	L
	H	↑	L	Z	L	Z	H
	H	↑	H	Z	H	Z	L

NOTE:

2569 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:

2569 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

2569 lnk 04

1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2569 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT374T/534T/574T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA

2569 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT2374T/2574T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

2569 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	2.0	5.5	
				FCT2xxxT		1.1	4.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	3.8	7.3[5]	
				FCT2xxxT	—	1.5	4.0[5]	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	6.0	16.3[5]	
				FCT2xxxT	—	3.8	13.0[5]	

2569 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT374T/534T/574T FCT2374T/2574T				FCT374AT/534AT/574AT FCT2374AT/2574AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_N[3]	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to CP		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns

2569 tbl 09

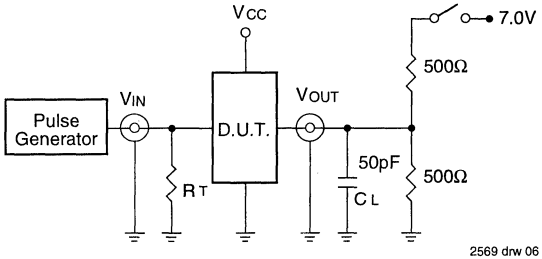
Symbol	Parameter	Conditions[1]	FCT374CT/534CT/574CT FCT2374CT/2574CT				FCT374DT/574DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_N[3]	C_L = 50pF R_L = 500Ω	2.0	5.2	2.0	6.2	2.0	4.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	5.5	1.5	6.2	1.5	4.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	5.0	1.5	5.7	1.5	4.0	—	—	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to CP		2.0	—	2.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW, D_N to CP		1.5	—	1.5	—	1.0	—	—	—	ns
t_W	CP Pulse Width HIGH or LOW[4]		5.0	—	6.0	—	3.0	—	—	—	ns

NOTES:
2569 tbl 10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. O_N for FCT374/2374T and FCT574/2574T, $\overline{O}_N$ for FCT534T.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2569 drw 06

SWITCH POSITION

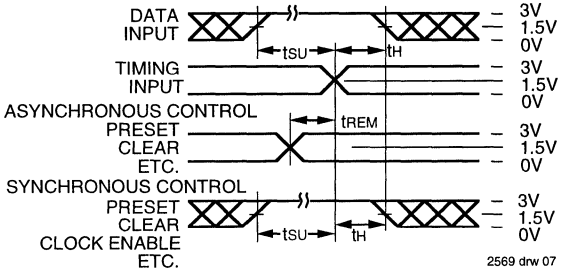
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

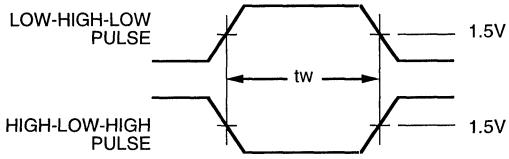
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



2569 drw 07

PULSE WIDTH



2569 drw 08

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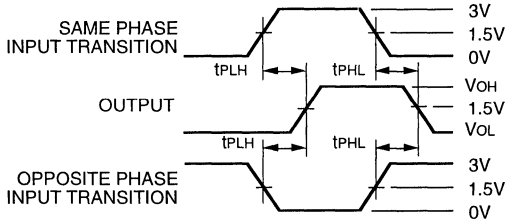
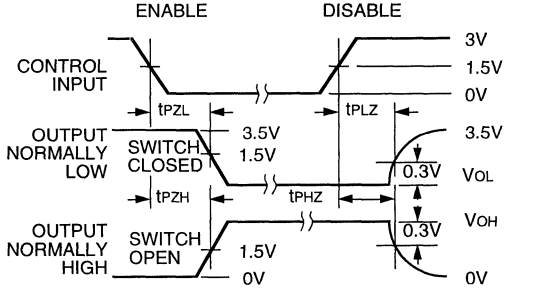
PROPAGATION DELAY



2569 drw 09

ENABLE AND DISABLE TIMES

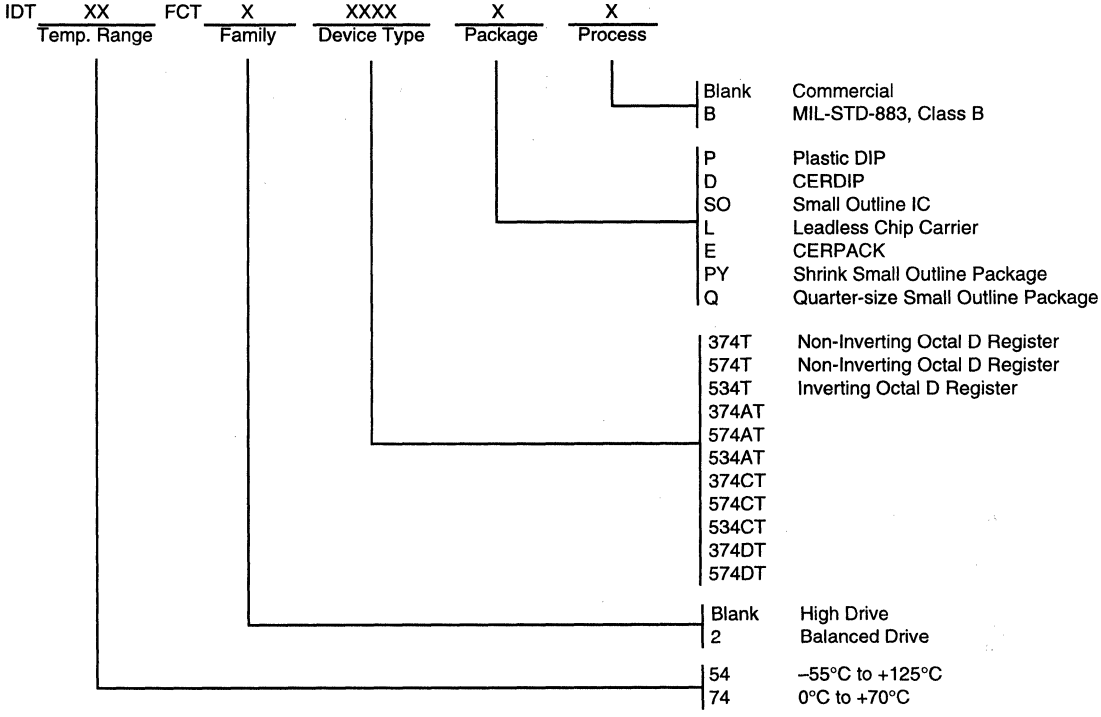


2569 drw 10

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2569 drw 11

Integrated Device Technology, Inc.

FAST CMOS OCTAL D FLIP-FLOP WITH CLOCK ENABLE

IDT54/74FCT377T/AT/CT/DT

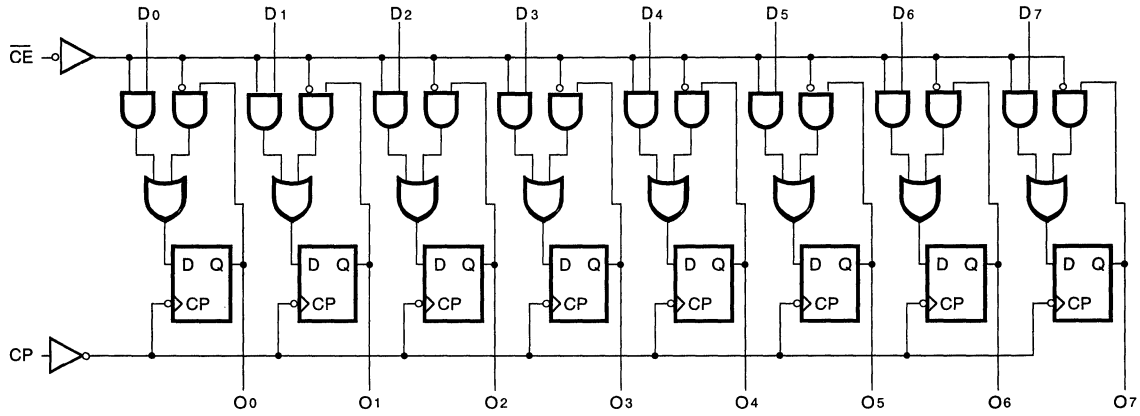
FEATURES:

- Std., A, C and D speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, QSOP, CERPACK and LCC packages

DESCRIPTION:

The IDT54/74FCT377T/AT/CT/DT are octal D flip-flops built using an advanced dual metal CMOS technology. The IDT54/74FCT377T/AT/CT/DT have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

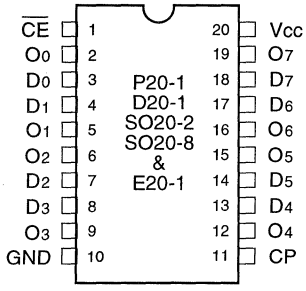
FUNCTIONAL BLOCK DIAGRAM



2630 drw 01

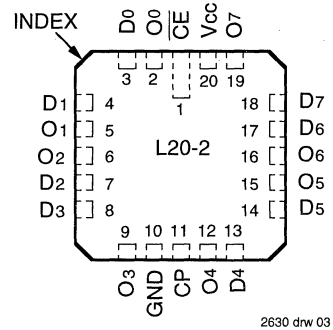
6

PIN CONFIGURATIONS



2630 drw 02

DIP/SOIC/QSOP/CERPACK
TOP VIEW



2630 drw 03

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$D_0 - D_7$	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
$O_0 - O_7$	Data Outputs
CP	Clock Pulse Input

2630 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2630 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

FUNCTION TABLE(1)

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold	↑	h	X	No Change
	H	H	X	No Change

2630 tbl 02

NOTE:
1. H = HIGH Voltage Level
   h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   L = LOW Voltage Level
   l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2630 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2630 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.
5. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
		$\overline{CE}$ = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
		$\overline{CE}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.0	16.3[5]	

2639 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FCT377T				FCT54/74FCT377AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to On	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	15.0	2.0	7.2	2.0	8.3	ns
t_{SU}	Set-Up Time HIGH or LOW Dn to CP		2.5	—	3.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Dn to CP		2.0	—	2.5	—	1.5	—	1.5	—	ns
t_{SU}	Set-Up Time HIGH or LOW $\overline{CE}$ to CP		4.0	—	4.0	—	3.5	—	3.5	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width, HIGH or LOW		7.0	—	7.0	—	6.0	—	7.0	—	ns

2630 tbl 06

Symbol	Parameter	Condition[1]	IDT54/74FCT377CT				FCT54/74FCT377DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to On	C_L = 50pF R_L = 500Ω	2.0	5.2	2.0	5.5	2.0	4.4	—	—	ns
t_{SU}	Set-Up Time HIGH or LOW Dn to CP		2.0	—	2.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW Dn to CP		1.5	—	1.5	—	1.0	—	—	—	ns
t_{SU}	Set-Up Time HIGH or LOW $\overline{CE}$ to CP		3.5	—	3.5	—	3.0	—	—	—	ns
t_H	Hold Time HIGH or LOW $\overline{CE}$ to CP		1.5	—	1.5	—	0.0	—	—	—	ns
t_W	Clock Pulse Width, HIGH or LOW		6.0	—	7.0	—	3.0	—	—	—	ns

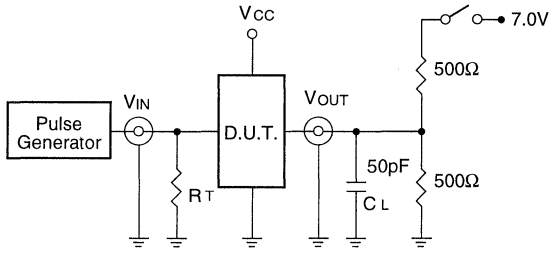
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2630 tbl 07

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2630 drw 04

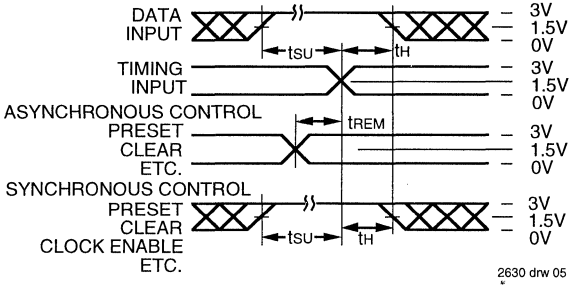
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS: 2630 lnk 08

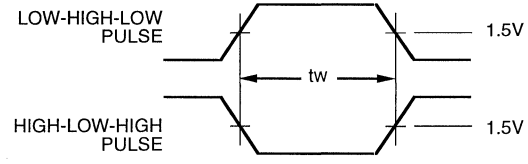
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



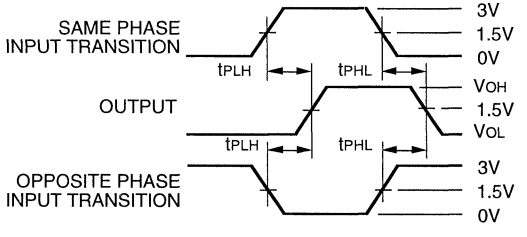
2630 drw 05

PULSE WIDTH



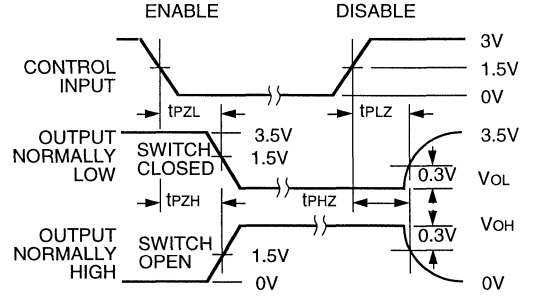
2630 drw 06

PROPAGATION DELAY



2630 drw 07

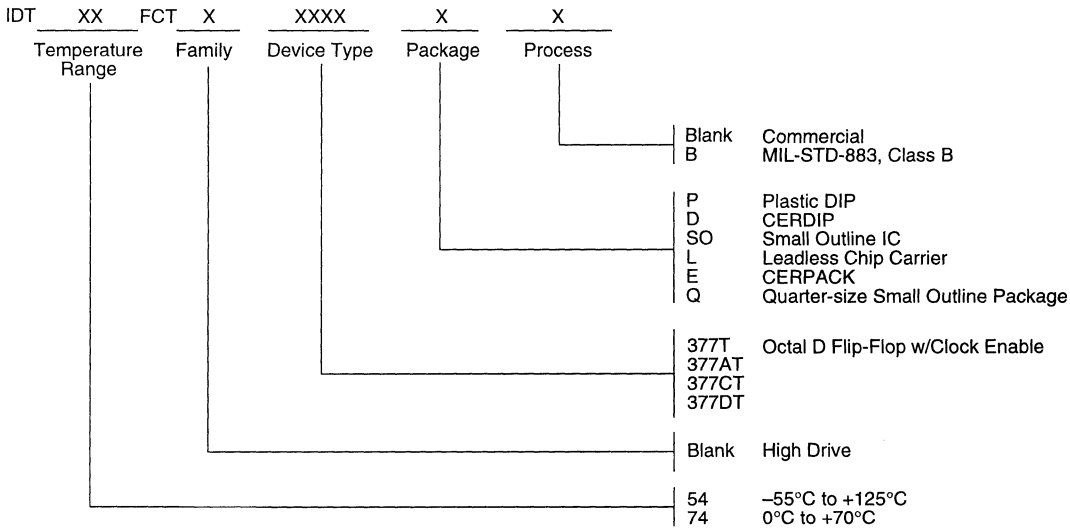
ENABLE AND DISABLE TIMES



2630 drw 08

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2630 drw 09

6

Integrated Device Technology, Inc.

FAST CMOS QUAD DUAL-PORT REGISTER

IDT54/74FCT399T/AT/CT

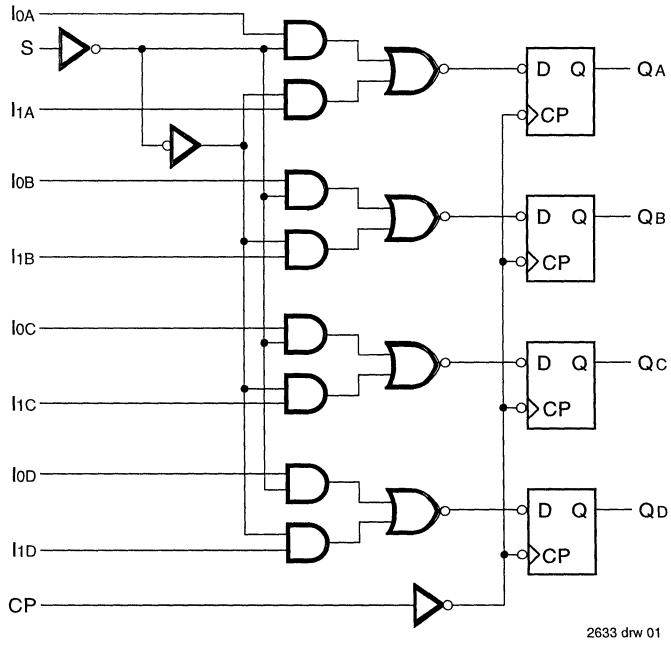
FEATURES:

- Std., A, and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

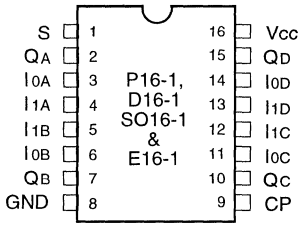
DESCRIPTION:

The IDT54/74FCT399T/AT/CT are high-speed quad dual-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0X}, I_{1X}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input for predictable operation.

FUNCTIONAL BLOCK DIAGRAM

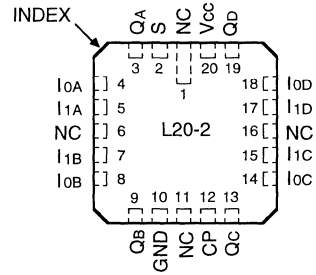


PIN CONFIGURATIONS



2633 drw 03

DIP/SOIC/CERPACK TOP VIEW



2633 drw 02

LCC TOP VIEW

PIN DESCRIPTION

Pin Names	Description
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
I_{0A} – I_{0D}	Data Inputs from Source 0
I_{1A} – I_{1D}	Data Inputs from Source 1
Q_A – Q_D	Register True Outputs

2633 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
S	**I_0**	**I_1**	**Q**
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

2633 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   h = HIGH Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   l = LOW Voltage Level one set-up time prior to the LOW-to-HIGH clock transition
   X = Immaterial

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2633 lnk 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2633 lnk 04

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max(3)., V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2633 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
		One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
		Four Bits Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	5.0	12.3[5]	

2633 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

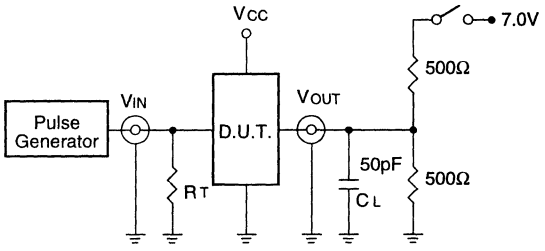
Symbol	Parameter	Condition[1]	IDT54/74FCT399T				IDT54/74FCT399AT				IDT54/74FCT399CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	3.0	10.0	3.0	11.5	2.5	7.0	2.5	7.5	2.5	6.1	2.5	6.6	ns
t_{SU}	Set-up Time HIGH or LOW I_n to CP		4.0	—	4.5	—	3.5	—	4.0	—	3.5	—	4.0	—	ns
t_H	Hold Time HIGH or LOW I_n to CP		1.0	—	1.5	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW S to CP		9.0	—	9.5	—	8.5	—	9.0	—	8.5	—	9.0	—	ns
t_H	Hold Time HIGH or LOW S to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
t_W	CP Pulse Width HIGH or LOW		5.0	—	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

2633 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2633 drw 04

SWITCH POSITION

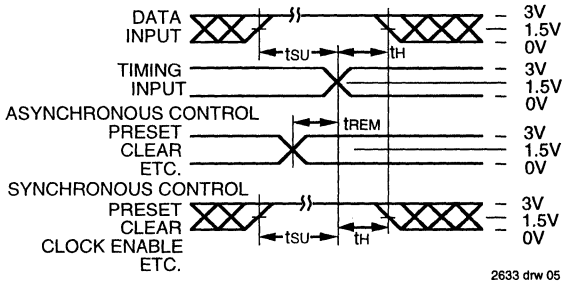
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2633 lnk 08

DEFINITIONS:

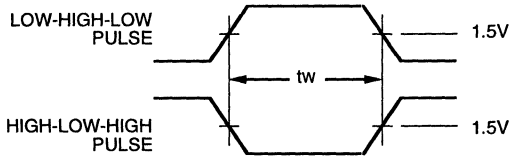
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



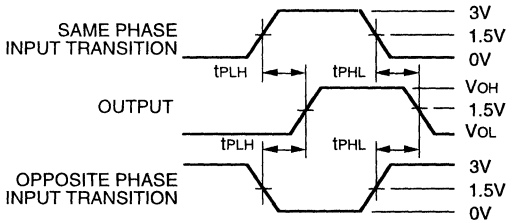
2633 drw 05

PULSE WIDTH



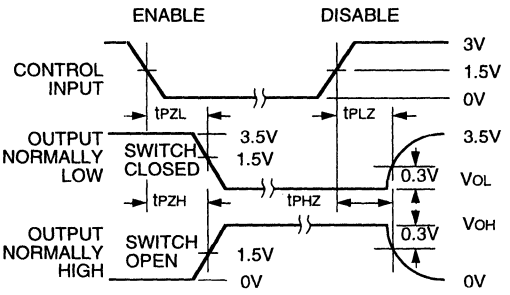
2633 drw 06

PROPAGATION DELAY



2633 drw 07

ENABLE AND DISABLE TIMES



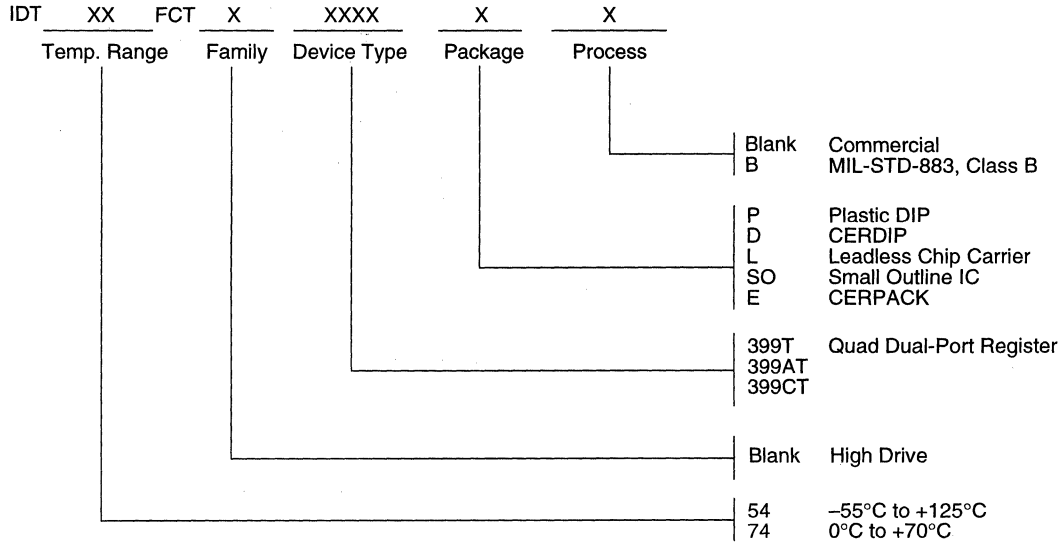
2633 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

6

ORDERING INFORMATION



2633 drw 09

Integrated Device Technology, Inc.

FAST CMOS 8-BIT IDENTITY COMPARATOR

IDT54/74FCT521T
IDT54/74FCT521AT
IDT54/74FCT521BT
IDT54/74FCT521CT

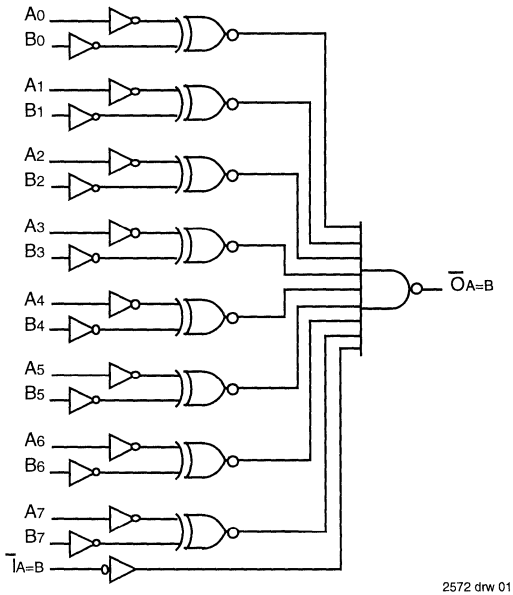
FEATURES:

- Std., A, B and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

DESCRIPTION:

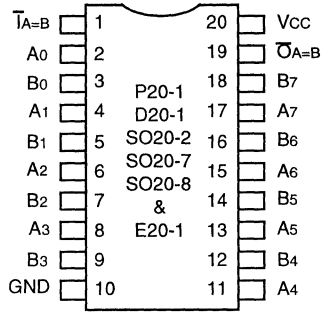
The IDT54/74FCT521T/AT/BT/CT are 8-bit identity comparators built using an advanced dual metal CMOS technology. These devices compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

FUNCTIONAL BLOCK DIAGRAM



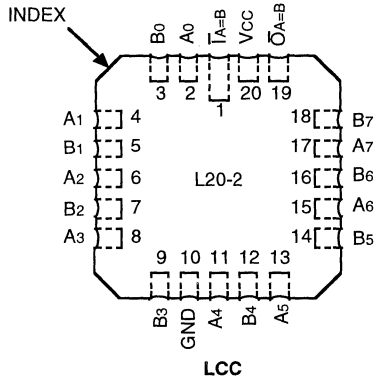
2572 drw 01

PIN CONFIGURATIONS



2572 drw 02

DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



2572 drw 03

LCC
TOP VIEW

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
A_0 - A_7	Word A Inputs
B_0 - B_7	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)

2572 tbl 01

FUNCTION TABLE[1]

Inputs		Output
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

2572 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   *A_0 = B_0, A_1 = B_1, A_2 = B_2, etc.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2572 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2572 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.01	1	mA

2572 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
		f_i = 10MHz One Bit Toggling 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.5	

NOTES:

2572 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			IDT54/74FCT521T				IDT54/74FCT521AT				IDT54/74FCT521BT				IDT54/74FCT521CT				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay An or Bn to $\overline{O}_{A=B}$	CL = 50pF RL = 500Ω	1.5	11.0	1.5	15.0	1.5	7.2	1.5	9.5	1.5	5.5	1.5	7.3	1.5	4.5	1.5	5.1	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$		1.5	10.0	1.5	9.0	1.5	6.0	1.5	7.8	1.5	4.6	1.5	6.0	1.5	4.1	1.5	4.5	ns

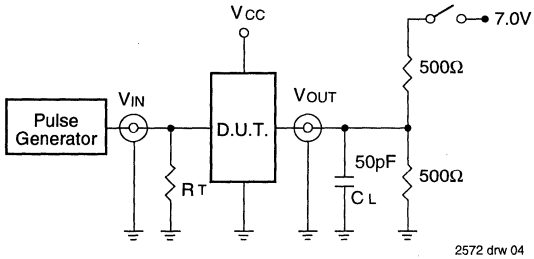
NOTES:

2572 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2572 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

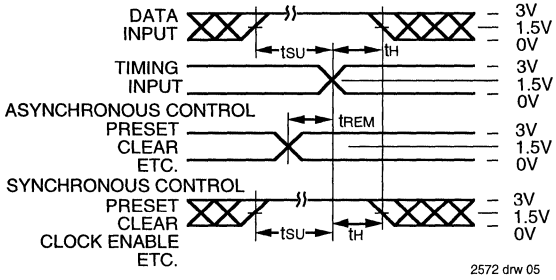
2572 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

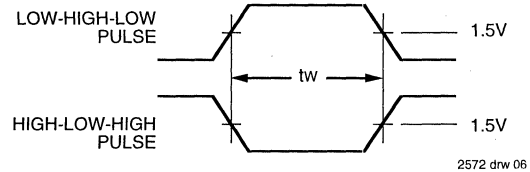
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



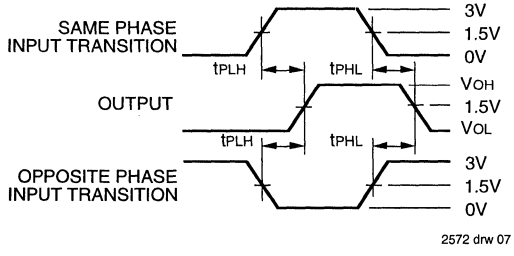
2572 drw 05

PULSE WIDTH



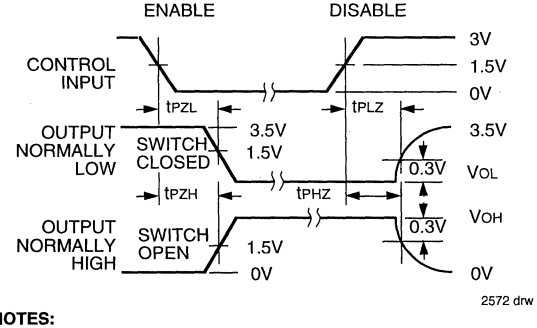
2572 drw 06

PROPAGATION DELAY



2572 drw 07

ENABLE AND DISABLE TIMES

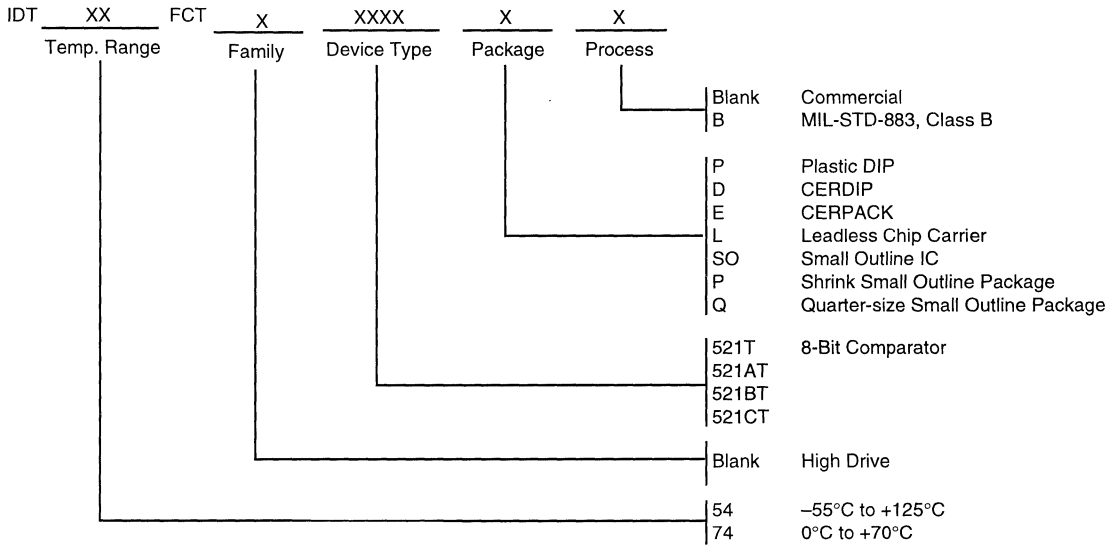


2572 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2572 drw 09

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL LATCHED TRANSCEIVER

IDT54/74FCT543T/AT/CT/DT
IDT54/74FCT2543T/AT/CT

FEATURES:

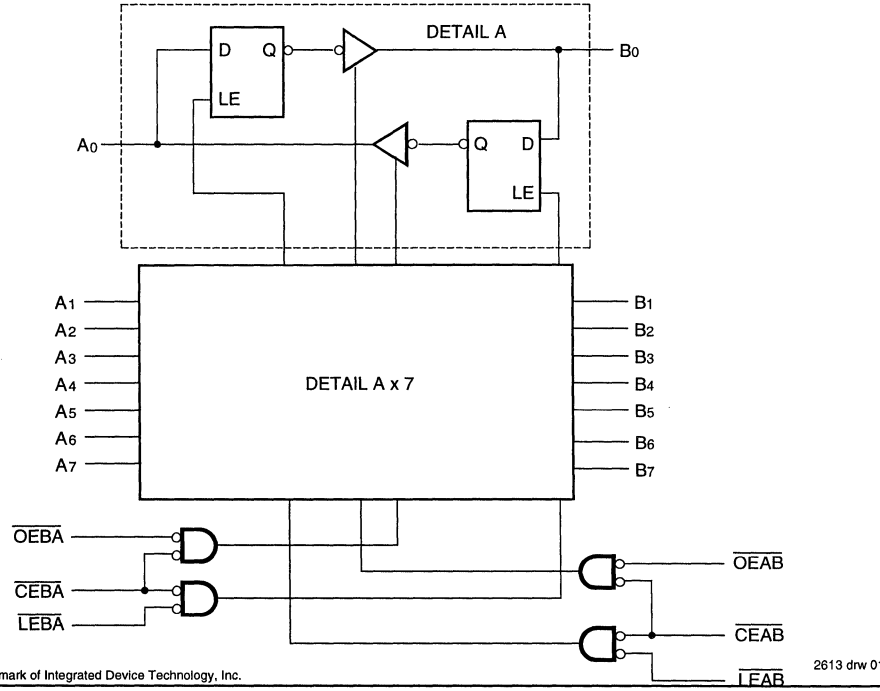
- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT543T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
- **Features for FCT2543T:**
  - Std., A, and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

DESCRIPTION:

The FCT543T/FCT2543T is a non-inverting octal transceiver built using an advanced dual metal CMOS technology. This device contains two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0–A_7 or to take data from B_0–B_7, as indicated in the Function Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

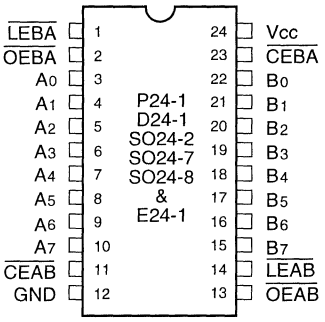
The FCT2543T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAM



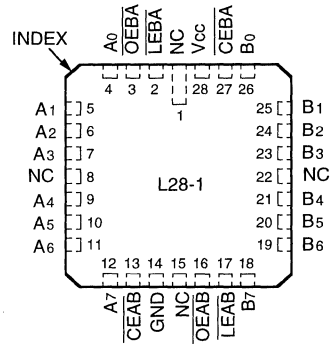
2613 drw 01

PIN CONFIGURATIONS



2613 drw 02

DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



2613 drw 03

LCC
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A0–A7	A-to-B Data Inputs or B-to-A 3-State Outputs
B0–B7	B-to-A Data Inputs or A-to-B 3-State Outputs

2613 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2613 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

FUNCTION TABLE(1, 2)

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B0–B7
H	—	—	Storing	High Z
—	H	—	Storing	—
—	—	H	—	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

2613 tbl 02

NOTES:
1. * Before $\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   — = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2613 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

6

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2613 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR 543T/AT/CT/DT

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2613 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR 2543T/AT/CT/DT

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

2613 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4V V_{IN} = GND	FCTxxxT	—	2.0	5.5	
				FCT2xxxT	—	1.1	4.2	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	3.8	7.3[5]	
				FCT2xxxT	—	1.5	4.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	FCTxxxT	—	6.0	16.3[5]	
				FCT2xxxT	—	3.8	13.0[5]	

2613 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT543T/ FCT2543T				FCT543AT/ FCT2543AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparant Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	1.5	8.5	1.5	10.0	1.5	6.5	1.5	7.5	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		1.5	12.5	1.5	14.0	1.5	8.0	1.5	9.0	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		1.5	12.0	1.5	14.0	1.5	9.0	1.5	10.0	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		1.5	9.0	1.5	13.0	1.5	7.5	1.5	8.5	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		3.0	—	3.0	—	2.0	—	2.0	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	2.0	—	2.0	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	ns

2513 tbl 09

Symbol	Parameter	Condition[1]	FCT543CT/ FCT2543CT				FCT543DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparant Mode An to Bn or Bn to An	CL = 50pF RL = 500Ω	1.5	5.3	1.5	6.1	1.5	4.4	—	—	ns
tPLH tPHL	Propagation Delay $\overline{LEBA}$ to An, $\overline{LEAB}$ to Bn		1.5	7.0	1.5	8.0	1.5	5.0	—	—	ns
tPZH tPZL	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		1.5	8.0	1.5	9.0	1.5	5.4	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn		1.5	6.5	1.5	7.5	1.5	4.3	—	—	ns
tSU	Set-up Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	1.5	—	—	—	ns
tH	Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$		2.0	—	2.0	—	1.5	—	—	—	ns
tW	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	3.0[3]	—	—	—	ns

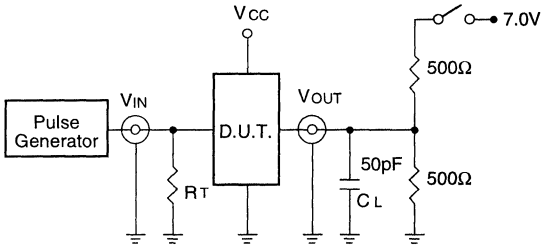
NOTES:

2513 tbl 10

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2513 drw 05

SWITCH POSITION

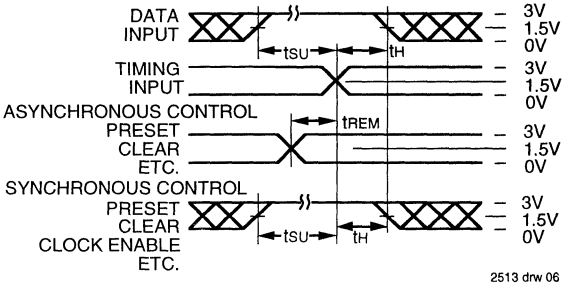
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2513 lnk 11

DEFINITIONS:

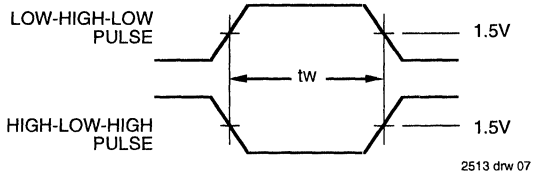
CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



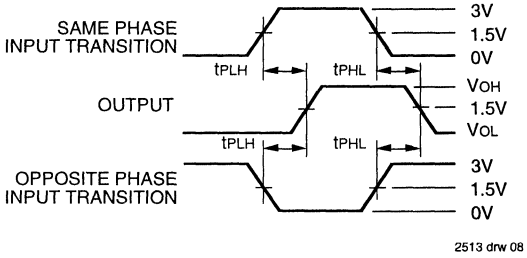
2513 drw 06

PULSE WIDTH



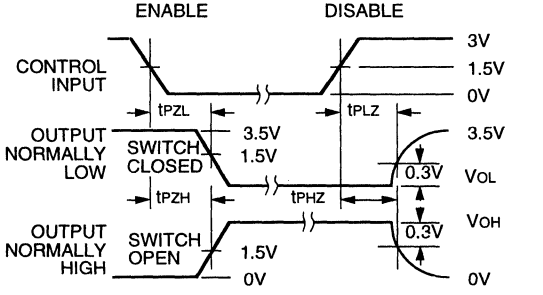
2513 drw 07

PROPAGATION DELAY



2513 drw 08

ENABLE AND DISABLE TIMES

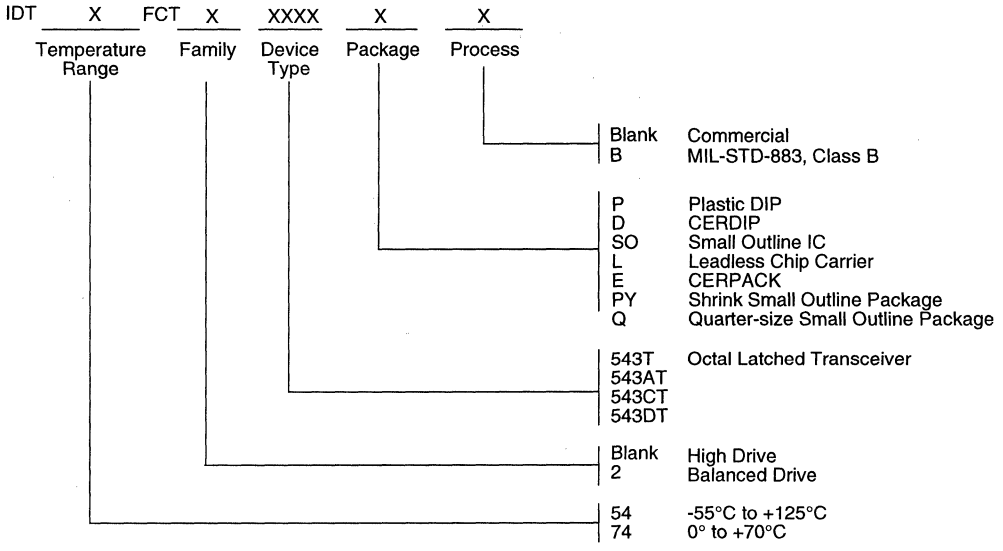


2513 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

ORDERING INFORMATION



2613 drw 10

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVER (OPEN DRAIN)

IDT54/74FCT621T/AT

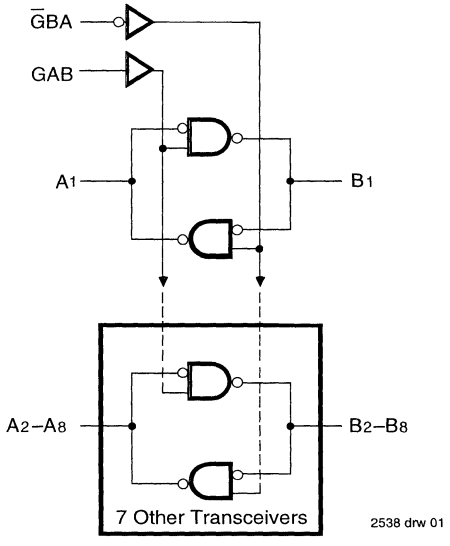
FEATURES:

- Std. and A speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

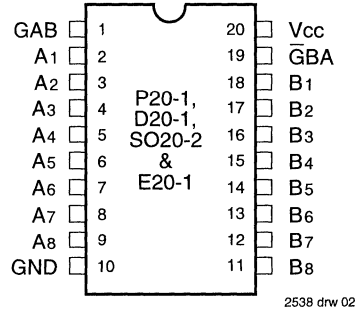
DESCRIPTION:

The IDT54/74FCT621T/AT is an octal transceiver with non-inverting Open-Drain bus compatible outputs in both send and receive directions. The B bus outputs are capable of sinking 64mA providing very good capacitive drive characteristics. These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

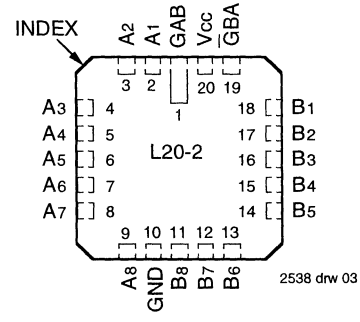
FUNCTIONAL BLOCK DIAGRAM (1)



PIN CONFIGURATIONS



DIP/SOIC/CERPACK TOP VIEW



LCC TOP VIEW

6

PIN DESCRIPTION

Pin Names	Description
$\overline{G}$BA, GAB	Enable Inputs
$A_1 - A_8$	A Inputs or Open-drain Outputs
$B_1 - B_8$	B Inputs or Open-drain Outputs

2538 tbl 01

FUNCTION TABLE(1)

Enable Inputs		
$\overline{G}$BA	GAB	Function
L	L	B data to A bus
H	H	A data to B bus
H	L	OFF
L	H	B data to A bus A data to B bus

NOTE: 2538 tbl 02

1. H = HIGH Voltage Level.
   L = LOW Voltage Level.
   OFF = HIGH if pull-up resistor is connected to Open-Drain output.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2538 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2538 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[5]	V_{CC} = Max., V_I = 2.7V		—	—	±1	µA
I_{IL}	Input LOW Current[5]	V_{CC} = Max., V_I = 0.5V		—	—	±1	µA
I_I	Input HIGH Current[5]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N= –18mA		—	–0.7	–1.2	V
I_{OH}	Output HIGH Current	V_{CC} = Max. V_{IN} = V_{IH} or V_{IL}	V_{OH} = Vcc (Max.)	—	—	20	µA
V_{OL}	Output LOW Voltage (B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.[4] I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_{OL}	Output LOW Voltage (A Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.[4] I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or Vo ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = max., V_{IN} = GND or Vcc		—	0.01	1	mA

2538 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/MHz
I_C	Total Power Supply Current[6,7]	V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} One Bit Toggling at f_i =10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.5	
		V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND or V_{CC} Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	6.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	14.0[5]	

NOTES: 2538 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
7. This test is performed with outputs tied to GND through a pull-down resistor.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

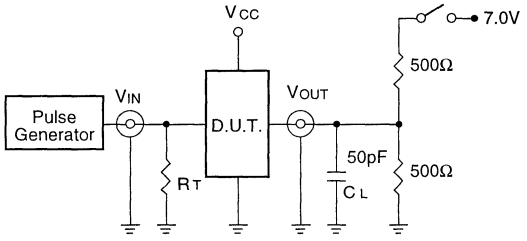
Symbol	Parameter	Condition[1]	IDT54/74FCT621T				IDT54/74FCT621AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH}	Propagation Delay A to B	C_L = 50pF R_L = 500Ω	5.5	13.0	5.5	13.5	5.5	12.0	5.5	12.5	ns
t_{PHL}			1.5	8.5	1.5	9.5	1.5	6.8	1.5	7.6	
t_{PLH}	Propagation Delay B to A		5.5	12.5	5.5	13.0	5.5	12.0	5.5	12.5	ns
t_{PHL}			1.5	8.0	1.5	9.0	1.5	6.4	1.5	7.2	
t_{PLH}	Propagation Delay $\overline{G}$BA to A		5.5	14.0	5.5	14.5	5.5	13.0	5.5	13.5	ns
t_{PHL}			1.5	8.5	1.5	9.5	1.5	6.8	1.5	7.6	
t_{PLH}	Propagation Delay GAB to B		5.5	14.0	5.5	14.5	5.5	13.0	5.5	13.5	ns
t_{PHL}			1.5	8.0	1.5	9.0	1.5	6.4	1.5	7.2	

NOTES: 2538 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2538 drw 03

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

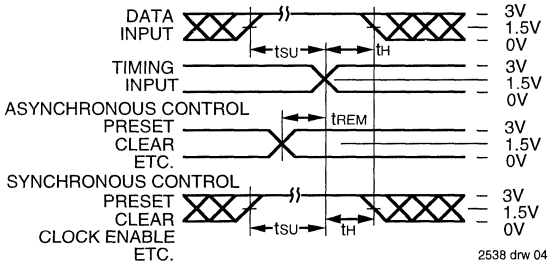
2538 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

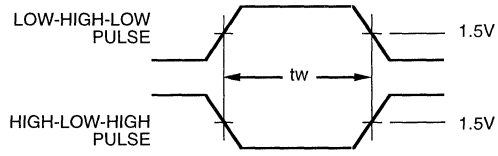
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



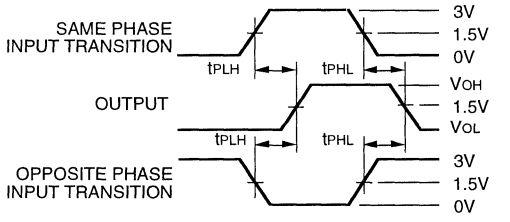
2538 drw 04

PULSE WIDTH



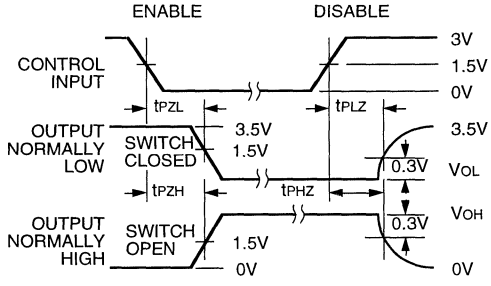
2538 drw 05

PROPAGATION DELAY



2538 drw 06

ENABLE AND DISABLE TIMES



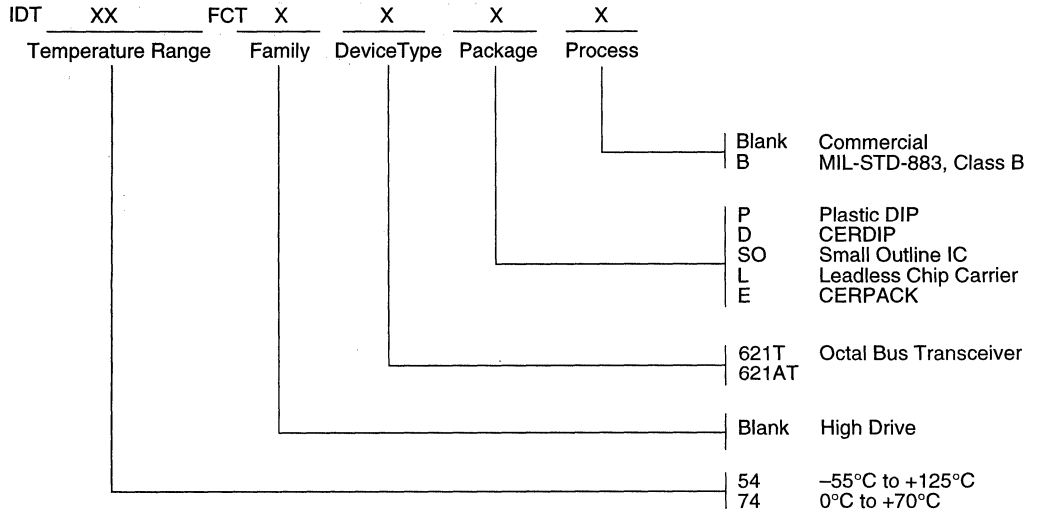
2538 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

6

ORDERING INFORMATION



2538 drw 08

Integrated Device Technology, Inc.

FAST CMOS OCTAL BUS TRANSCEIVERS (3-STATE)

IDT54/74FCT620T/AT/CT
IDT54/74FCT623T/AT/CT

FEATURES:

- Std., A and C speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - V_{OH} = 3.3V (typ.)
  - V_{OL} = 0.3V (typ.)
- High drive outputs (-15mA I_{OH}, 64mA I_{OL})
- Power off disable outputs permit "live insertion"
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

DESCRIPTION

The IDT54/74FCT623T/AT/CT is a non-inverting octal transceiver with 3-state bus-driving outputs in both the send and receive directions. The B bus outputs are capable of sinking 64mA and sourcing up to 15mA, providing very good capacitive drive characteristics.

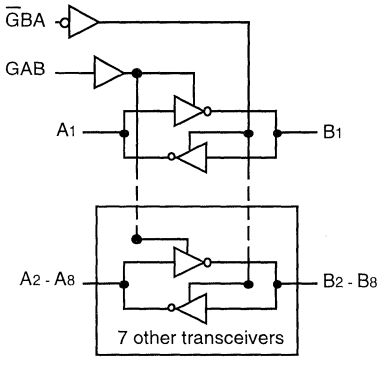
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

One important feature of the IDTFCT620T/AT/CT and IDTFCT623T/AT/CT is the Power Down Disable capability. When the GAB and $\overline{GBA}$ inputs are conditioned to put the device in high-Z state, the I/O ports will maintain high impedance during power supply ramps and when V_{CC} = 0V. This is a desirable feature in back-plane applications where it may be necessary to perform "live" insertion and removal of cards for on-line maintenance. It is also a benefit in systems with multiple redundancy where one or more redundant cards may be powered-off.

The IDTFCT620T/AT/CT is the inverting option of the IDTFCT623T/AT/CT.

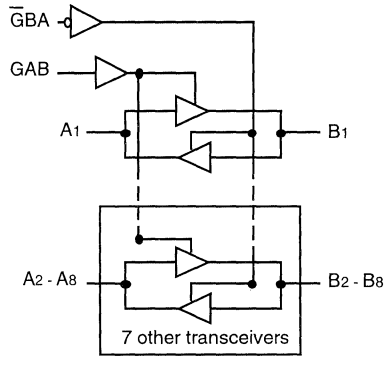
6

FUNCTIONAL BLOCK DIAGRAMS



FCT620T/AT/CT

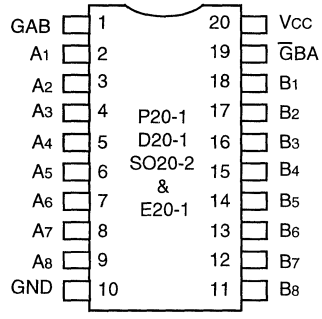
2563 drw 01



FCT623T/AT/CT

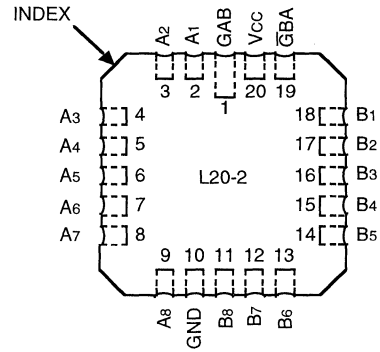
2563 drw 02

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

2563 drw 03



LCC
TOP VIEW

2563 drw 04

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
$\overline{G}BA$, GAB	Enable Inputs
A_1 - A_8	A Bus Inputs or 3-State Outputs
B_1 - B_8	B Bus Inputs or 3-State Outputs

2563 tbl 01

FUNCTION TABLE(1)

Enable Inputs		Outputs	
$\overline{G}BA$	GAB	FCT620	FCT623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus $\overline{A}$ data to B bus	B data to A bus A data to B bus

2563 tbl 02

NOTES:
1. H = HIGH Voltage Level
2. L = LOW Volage Level
3. Z = High-Impedance (OFF) state

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2563 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2563 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[5]	V_{CC} = Max., V_I = 2.7V		—	—	±1	µA
I_{IL}	Input LOW Current[5]	V_{CC} = Max., V_I = 0.5V		—	—	±1	µA
I_I	Input HIGH Current[5]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage (A and B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage (A Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL.[4] I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_{OL}	Output LOW Voltage (B Bus)	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.[4] I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage[6]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	µA

2563 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.
5. The test limit for this parameter is ±5µA at T_A = –55°C.
6. This parameter is guaranteed but not tested.

6

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{G}BA$ = GAB = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{G}BA$ = GAB = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.5	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{G}BA$ = GAB = GND Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	6.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.0	14.0[5]	

2563 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT620T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT620T				54/74FCT620AT				54/74FCT620CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay $\overline{A}$n to Bn	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	5.2	1.5	6.0	1.5	4.5	1.5	5.1	ns
tPLH tPHL	Propagation Delay $\overline{B}$n to An		1.5	7.0	1.5	8.0	1.5	5.2	1.5	6.0	1.5	4.5	1.5	5.1	ns
tPZH tPZL	Output Enable Time $\overline{G}$BA to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time $\overline{G}$BA to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPZH tPZL	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

2563 tbl 07

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR FCT623T/AT/CT

Symbol	Parameter	Condition[1]	54/74FCT623T				54/74FCT623AT				54/74FCT623CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay An to Bn	CL = 50pF RL = 500Ω	1.5	7.5	1.5	9.0	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPLH tPHL	Propagation Delay Bn to An		1.5	7.5	1.5	9.5	1.5	5.5	1.5	6.3	1.5	4.8	1.5	5.4	ns
tPZH tPZL	Output Enable Time $\overline{G}$BA to An		1.5	9.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time $\overline{G}$BA to An		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns
tPZH tPZL	Output Enable Time GAB to Bn		1.5	9.0	1.5	10.5	1.5	7.0	1.5	8.0	1.5	6.1	1.5	6.9	ns
tPHZ tPLZ	Output Disable Time GAB to Bn		1.5	8.0	1.5	9.0	1.5	6.5	1.5	7.4	1.5	5.6	1.5	6.4	ns

NOTES:

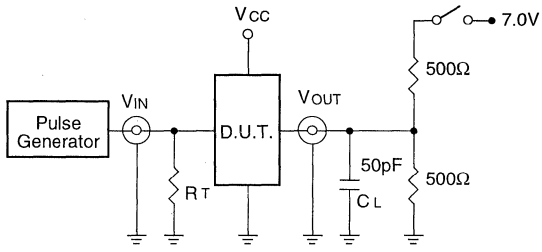
2563 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2563 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

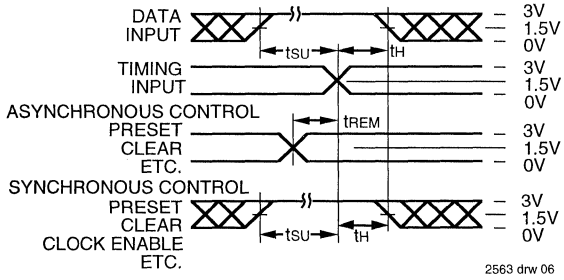
2563 lnk 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

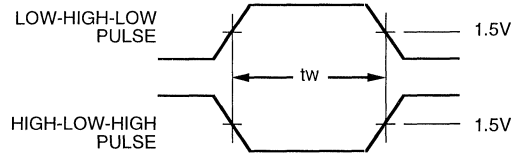
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



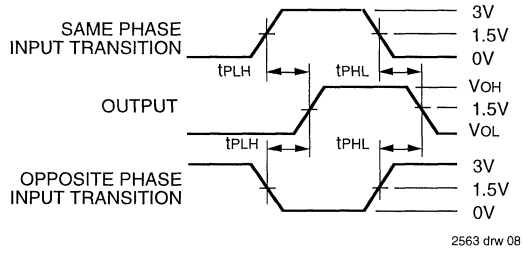
2563 drw 06

PULSE WIDTH



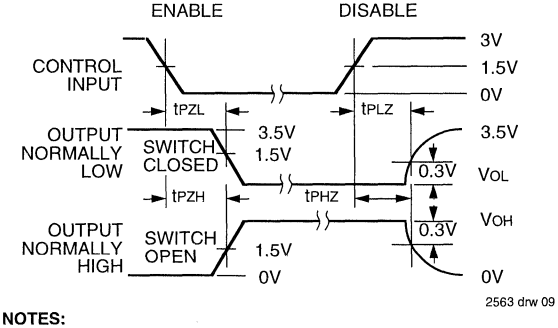
2563 drw 07

PROPAGATION DELAY



2563 drw 08

ENABLE AND DISABLE TIMES

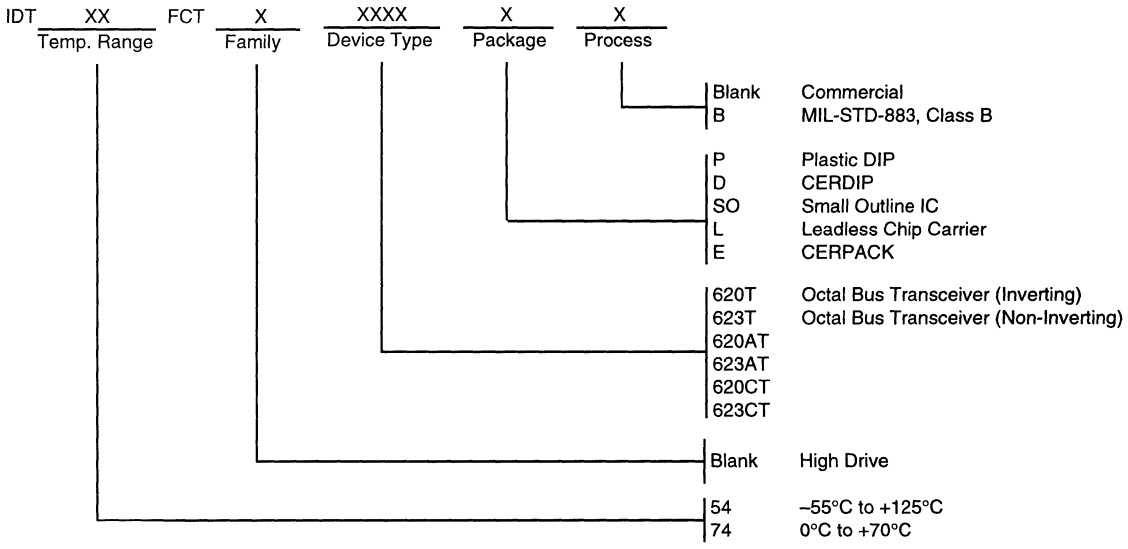


2563 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2563 drw 10

6

Integrated Device Technology, Inc.

FAST CMOS OCTAL TRANSCEIVER/ REGISTERS (3-STATE)

IDT54/74FCT646T/AT/CT/DT - 2646T/AT/CT
IDT54/74FCT648T/AT/CT
IDT54/74FCT652T/AT/CT/DT - 2652T/AT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT646T/648T/652T:**
  - Std., A, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 64mA I_{OL})
  - Power off disable outputs permit "live insertion"
- **Features for FCT2646T/2652T:**
  - Std., A, and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

DESCRIPTION:

The FCT646T/FCT2646T/FCT648T/FCT652T/2652T consist of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

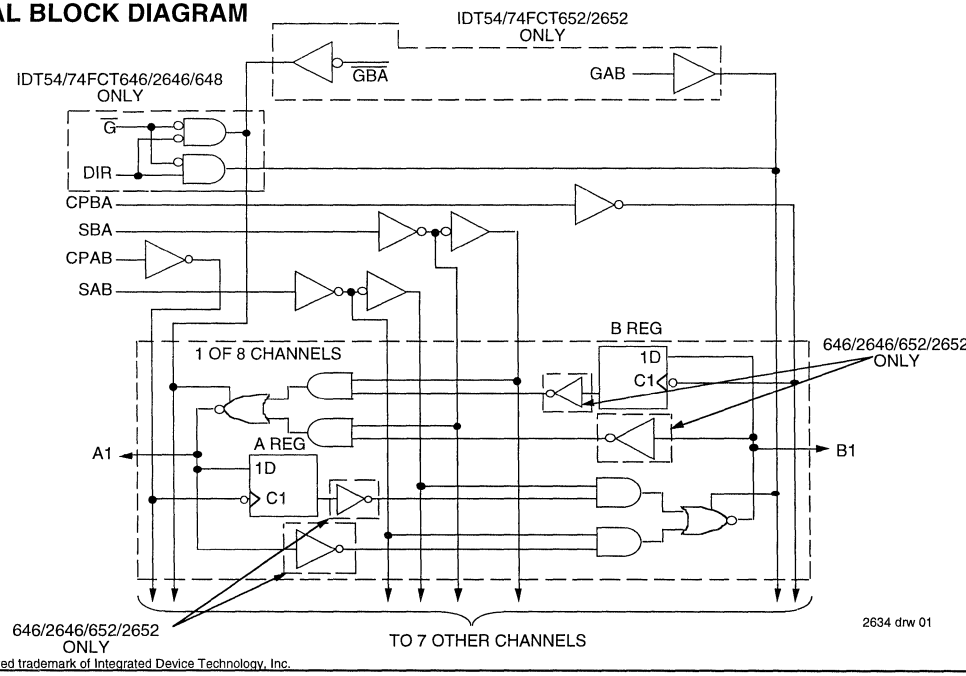
The FCT652T/FCT2652T utilize GAB and $\overline{GBA}$ signals to control the transceiver functions. The FCT646T/FCT2646T/FCT648T utilize the enable control ($\overline{G}$) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

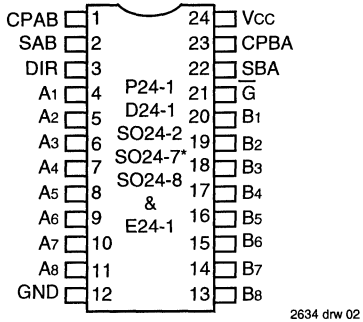
The FCT26xxT have balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2xxxT parts are plug-in replacements for FCTxxxT parts.

FUNCTIONAL BLOCK DIAGRAM

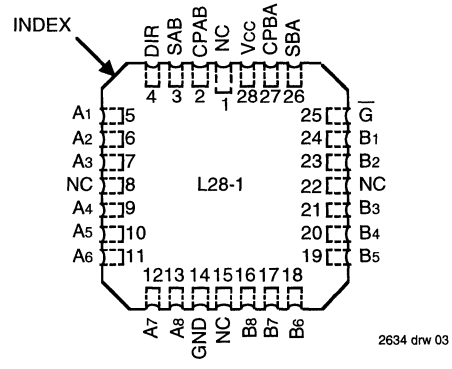


PIN CONFIGURATIONS

FCT646/FCT2646T
FCT648



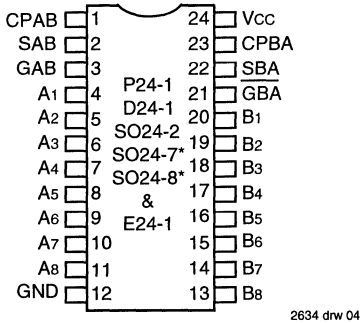
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



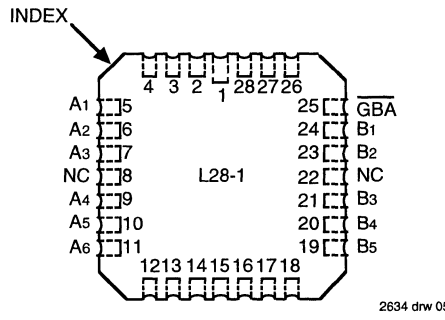
LCC
TOP VIEW

* FCT646/2646T/AT/CT/DT only

FCT652/FCT2652T



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

* FCT652/2652T/AT/CT/DT only

PIN DESCRIPTION

Pin Names	Description
A1 - A8	Data Register A Inputs Data Register B Outputs
B1 - B8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (646/648)
GAB, $\overline{GBA}$	Output Enable Inputs (652)

2634 tbl 01

6

FUNCTION TABLE (646/648)

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	FCT646T/FCT2646T	FCT648T
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

2634 tbl 02

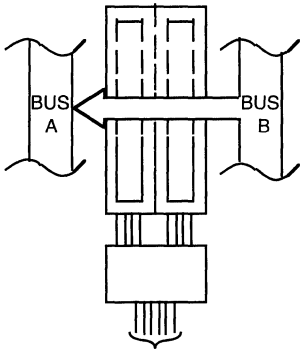
FUNCTION TABLE (652)

Inputs						Data I/O		Operation or Function
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	FCT652T/FCT2652T
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[1]	Store A, Hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified[1]	Input	Hold A, Store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

2634 tbl 03

NOTES:

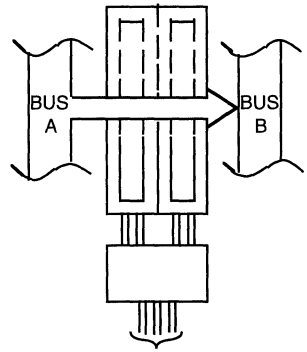
1. The data output functions may be enabled or disabled by various signals at the GAB or GBA inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, ≠ = LOW-to-HIGH transition.
3. $\overline{A}$ in B Register.
4. $\overline{B}$ in A Register.



652/2652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
646/2646/ 648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A

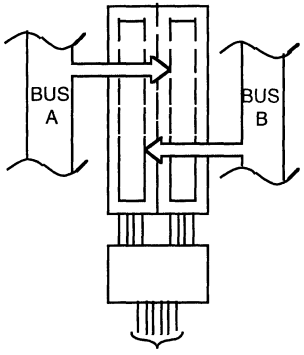
2634 drw 06



652/2652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X
646/2646/ 648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X

REAL-TIME TRANSFER BUS A TO B

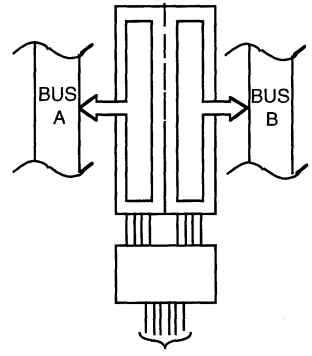
2634 drw 07



652/2652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X
646/2646/ 648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X

STORAGE FROM A AND/OR B

2634 drw 08



652/2652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or	H or	H	H
646/2646/ 648 (1)	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or	X	H
	H	L	H or	X	H	X

TRANSFER STORES DATA TO A AND/OR B

2634 drw 09

NOTE:
1. 646/2646/648 cannot transfer data to A bus and B bus simultaneously.

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2634 lnk 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

2634 lnk 05

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(4)	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(4)		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(4)		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current(4)	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2634 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT646T/648T/652T

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage(5)	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2634 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT2646T/2652T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

NOTES:

2634 lnk 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5μA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	0.15	0.25	mA/ MHz
				FCT2xxxT	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	1.5	3.5	mA
				FCT2xxxT	—	0.6	2.2	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	2.0	5.5	
				FCT2xxxT		1.1	4.2	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCTxxxT	—	3.8	7.3[5]	
				FCT2xxxT	—	1.5	4.0[5]	
			V_{IN} = 3.4 V_{IN} = GND	FCTxxxT	—	6.0	16.3[5]	
				FCT2xxxT	—	3.8	13.0[5]	

NOTES:

2634 tbl 08

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	646/648/652T 2646/2652T				646/648/652AT 2646/2652AT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPZH tPZL	Output Enable Time, $\overline{G}$, DIR to Bus[3]		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
tPHZ tPLZ	Output Disable Time, $\overline{G}$, DIR to Bus[3]		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
tW	Clock Pulse Width, HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns

2634 tbl 09

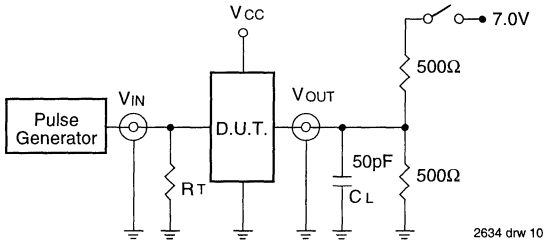
Symbol	Parameter	Condition[1]	646/648/652CT 2646/2652CT				646/652DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50pF RL = 500Ω	1.5	5.4	1.5	6.0	1.5	4.4	—	—	ns
tPZH tPZL	Output Enable Time, $\overline{G}$, DIR to Bus[3]		1.5	7.8	1.5	8.9	1.5	5.0	—	—	ns
tPHZ tPLZ	Output Disable Time, $\overline{G}$, DIR to Bus[3]		1.5	6.3	1.5	7.7	1.5	4.3	—	—	ns
tPLH tPHL	Propagation Delay Clock to Bus		1.5	5.7	1.5	6.3	1.5	4.4	—	—	ns
tPLH tPHL	Propagation Delay SBA or SAB to Bus		1.5	6.2	1.5	7.0	1.5	5.0	—	—	ns
tSU	Set-up Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	—	—	ns
tH	Hold Time HIGH or LOW Bus to Clock		1.5	—	1.5	—	1.0	—	—	—	ns
tW	Clock Pulse Width, HIGH or LOW[4]		5.0	—	5.0	—	3.0	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. GAB, $\overline{GBA}$ to Bus for 652.
4. This parameter is guaranteed but not tested.

2634 tbl 10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2634 drw 10

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

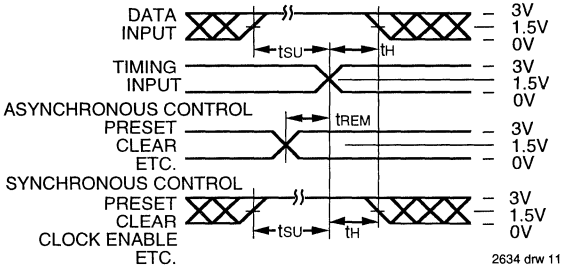
2634 lnk 11

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

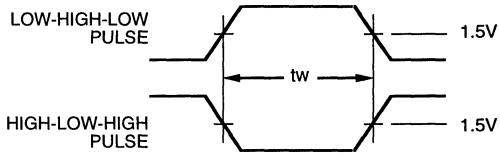
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



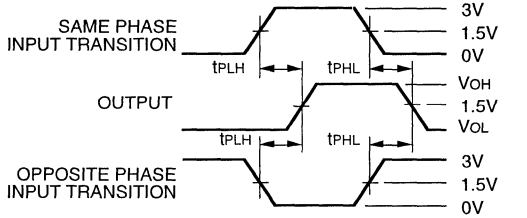
2634 drw 11

PULSE WIDTH



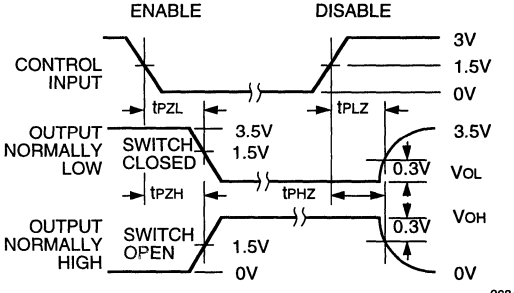
2634 drw 12

PROPAGATION DELAY



2634 drw 13

ENABLE AND DISABLE TIMES



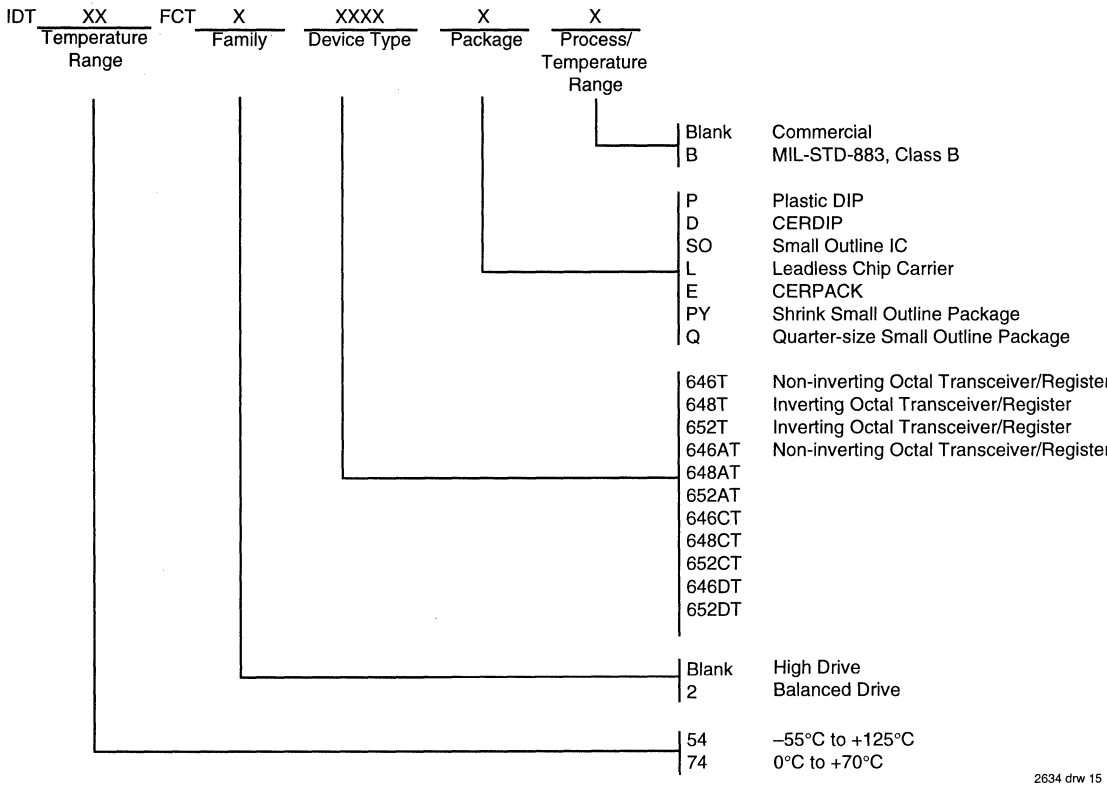
2634 drw 14

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

6

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH-PERFORMANCE CMOS BUS INTERFACE REGISTERS

IDT54/74FCT821AT/BT/CT
IDT54/74FCT823AT/BT/CT/DT
IDT54/74FCT825AT/BT/CT

FEATURES:

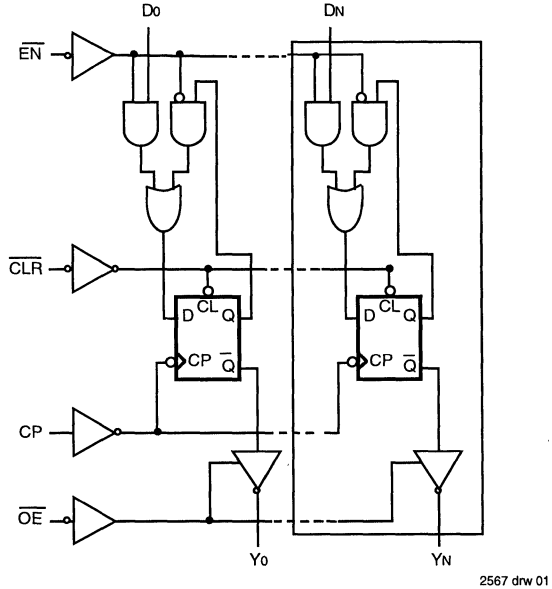
- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT821T/FCT823T/FCT825T:**
  - A, B, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 48mA I_{OL})
  - Power off disable outputs permit "live insertion"

DESCRIPTION:

The FCT82xT series is built using an advanced dual metal CMOS technology. The FCT82xT series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The FCT821T are buffered, 10-bit wide versions of the popular FCT374T function. The FCT823T are 9-bit wide buffered registers with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) – ideal for parity bus interfacing in high-performance microprogrammed systems. The FCT825T are 8-bit buffered registers with all the FCT823T controls plus multiple enables ($\overline{OE1}$, $\overline{OE2}$, $\overline{OE3}$) to allow multi-user control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

The FCT82xT high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in high-impedance state.

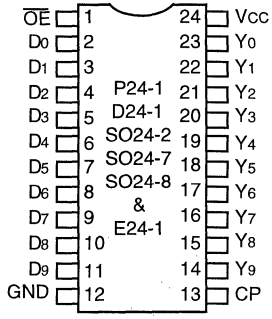
FUNCTIONAL BLOCK DIAGRAM



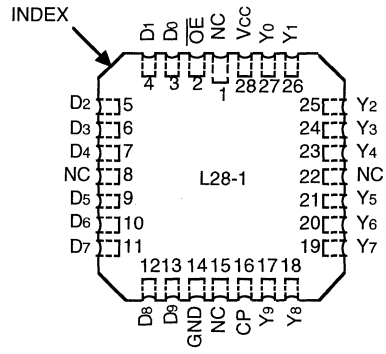
2567 drw 01

PIN CONFIGURATIONS

FCT821 10-BIT REGISTER



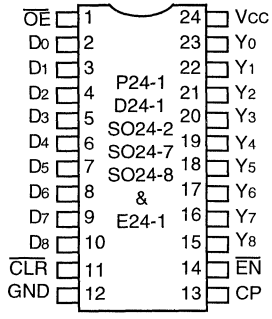
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



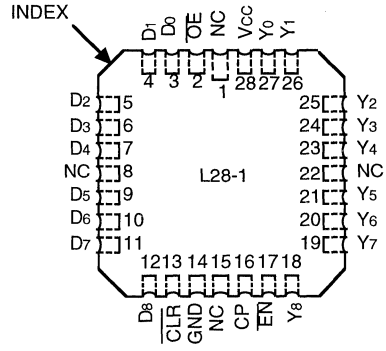
2567 drw 02

LCC
TOP VIEW

FCT823 9-BIT REGISTER



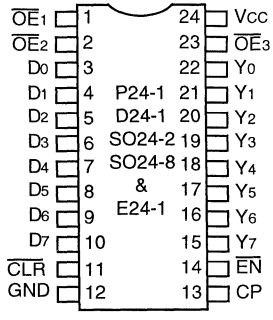
DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



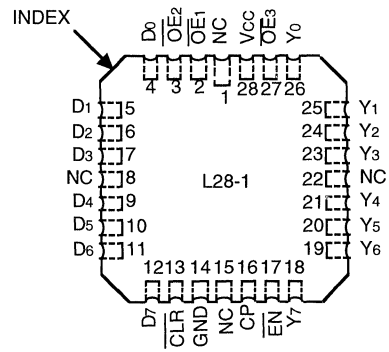
2567 drw 03

LCC
TOP VIEW

FCT825 8-BIT REGISTER



DIP/SOIC/QSOP/CERPACK
TOP VIEW



2567 drw 04

LCC
TOP VIEW

PIN DESCRIPTION

Names	I/O	Description
D_I	I	The D flip-flop data inputs.
$\overline{CLR}$	I	When the clear input is LOW and $\overline{OE}$ is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_I	O	The register 3-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y I outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

2567 tbl 01

FUNCTION TABLE[1]

Inputs					Internal/ Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

NOTE: 2567 tbl 02

1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2567 lnk 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2567 lnk 04

1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2567 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT821/823/825T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2567 lnk 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = $\overline{EN}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
		$\overline{OE}$ = $\overline{EN}$ = GND One Bit Toggling at fi = 5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	2.0	5.5	
		V_{CC} = Max. Outputs Open f_{CP}= 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	
		$\overline{OE}$ = $\overline{EN}$ = GND Eight Bits Toggling at fi = 2.5MHz 50% Duty Cycle	V_{IN} = 3.4V V_{IN} = GND	—	6.0	16.3[5]	

2567 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT821/823/825AT				FCT821/823/825BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to YI ($\overline{OE}$ = LOW)	CL = 50pF RL = 500Ω	1.5	10.0	1.5	11.5	1.5	7.5	1.5	8.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	20.0	1.5	20.0	1.5	15.0	1.5	16.0	
tSU	Set-up Time HIGH or LOW DI to CP	CL = 50pF RL = 500Ω	4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW DI to CP		2.0	—	2.0	—	1.5	—	1.5	—	ns
tSU	Set-up Time HIGH or LOW $\overline{EN}$ to CP		4.0	—	4.0	—	3.0	—	3.0	—	ns
tH	Hold Time HIGH or LOW $\overline{EN}$ to CP		2.0	—	2.0	—	0	—	0	—	ns
tPHL	Propagation Delay, $\overline{CLR}$ to YI		1.5	14.0	1.5	15.0	1.5	9.0	1.5	9.5	ns
tREM	Recovery Time $\overline{CLR}$ to CP		6.0	—	7.0	—	6.0	—	6.0	—	ns
tW	Clock Pulse Width HIGH or LOW		7.0	—	7.0	—	6.0	—	6.0	—	ns
tW	$\overline{CLR}$ Pulse Width LOW		6.0	—	7.0	—	6.0	—	6.0	—	ns
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF[4] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to YI	CL = 5pF[4] RL = 500Ω	1.5	7.0	1.5	8.0	1.5	6.5	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	7.5	1.5	8.0	

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

2567 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT821/823/825CT				FCT823DT		Unit
			Com'l.		Mil.		Com'l.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to Y_I ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	7.0	1.5	5.0	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	8.5	
t_{SU}	Set-up Time HIGH or LOW D_I to CP	C_L = 50pF R_L = 500Ω	3.0	—	3.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW D_I to CP		1.5	—	1.5	—	1.0	—	ns
t_{SU}	Set-up Time HIGH or LOW $\overline{EN}$ to CP		3.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW $\overline{EN}$ to CP		0	—	0	—	0	—	ns
t_{PHL}	Propagation Delay, $\overline{CLR}$ to Y_I		1.5	8.0	1.5	8.5	1.5	5.0	ns
t_{REM}	Recovery Time $\overline{CLR}$ to CP		6.0	—	6.0	—	3.0	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		6.0	—	6.0	—	3.0	—	ns
t_W	$\overline{CLR}$ Pulse Width LOW[3]		6.0	—	6.0	—	3.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_I	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	8.0	1.5	4.8	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	12.5	1.5	13.5	1.5	9.0	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y_I	C_L = 5pF[4] R_L = 500Ω	1.5	6.0	1.5	6.0	1.5	4.0	ns
		C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	6.5	1.5	4.0	

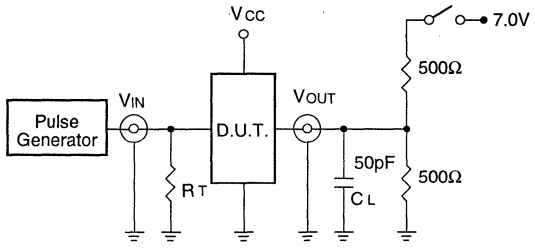
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. This condition is guaranteed but not tested.

2567 tbl 09

6

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2567 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

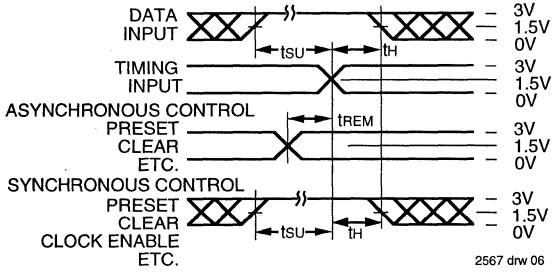
2567 lnk 10

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

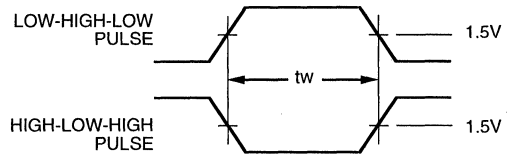
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



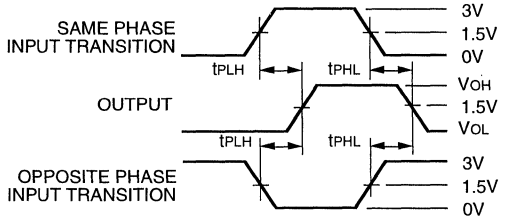
2567 drw 06

PULSE WIDTH



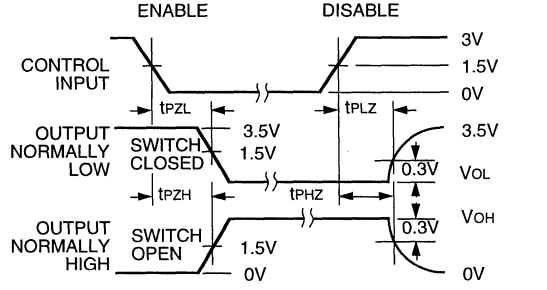
2567 drw 07

PROPAGATION DELAY



2567 drw 08

ENABLE AND DISABLE TIMES

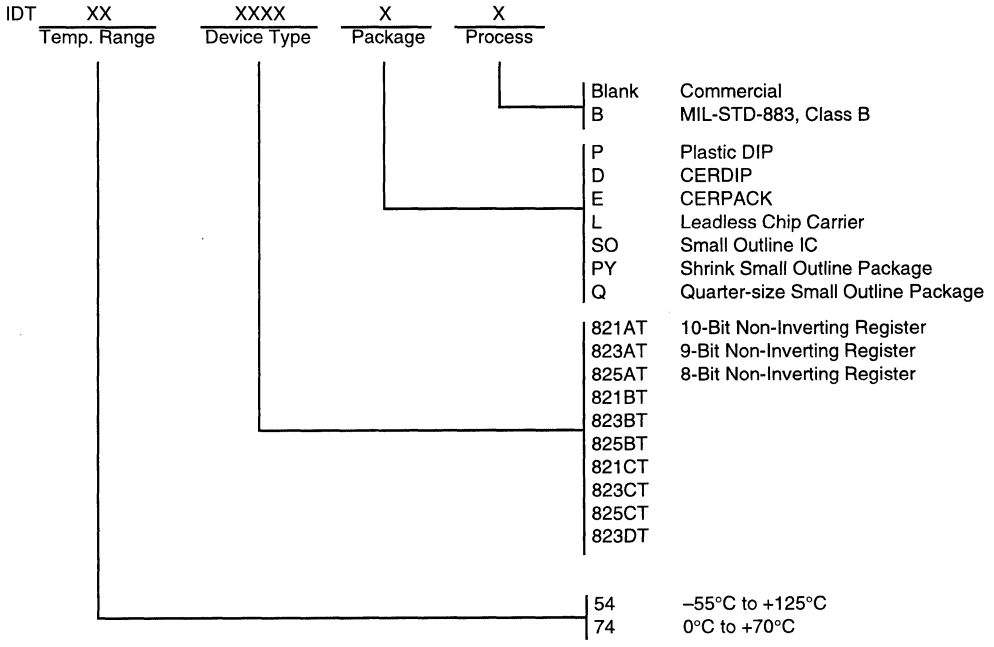


2567 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2567 drw 10

6

Integrated Device Technology, Inc.

FAST CMOS 10-BIT BUFFERS

IDT54/74FCT827AT/BT/CT/DT
IDT54/74FCT2827AT/BT/CT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT827T:**
  - A, B, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 48mA I_{OL})
- **Features for FCT2827T:**
  - A, B and C speed grades
  - Resistor outputs (-15mA I_{OH}, 12mA I_{OL} Com.)
    (-12mA I_{OH}, 12mA I_{OL} Mil.)
  - Reduced system switching noise

DESCRIPTION:

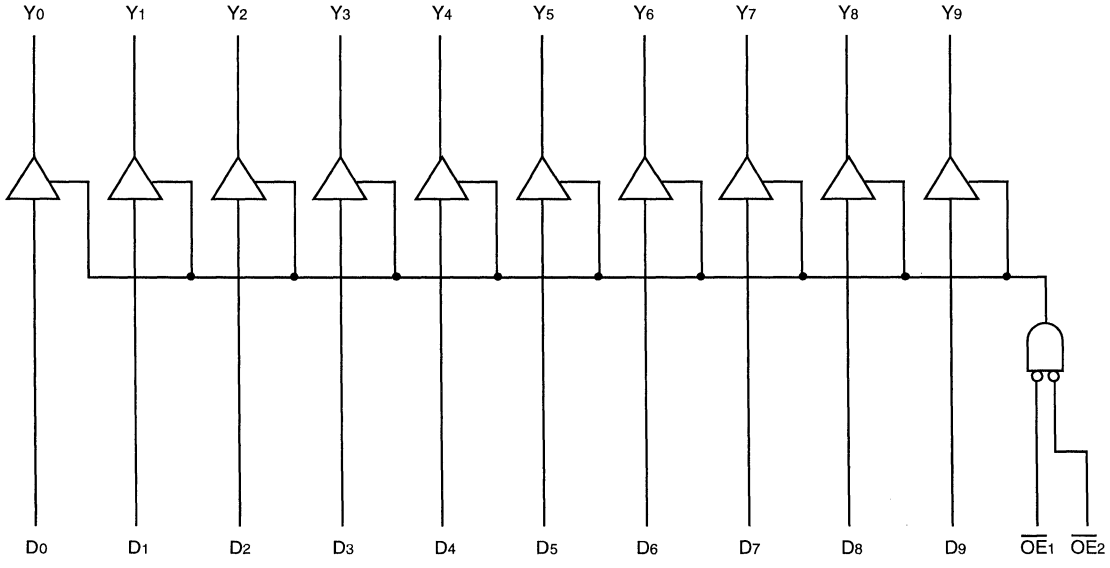
The FCT827T is built using an advanced dual metal CMOS technology.

The FCT827T/FCT2827T 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the FCT827T high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes to ground and all outputs are designed for low-capacitance bus loading in high-impedance state.

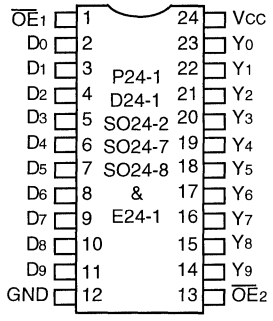
The FCT2827T has balanced output drive with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. FCT2827T parts are plug-in replacements for FCT827T parts.

FUNCTIONAL BLOCK DIAGRAM



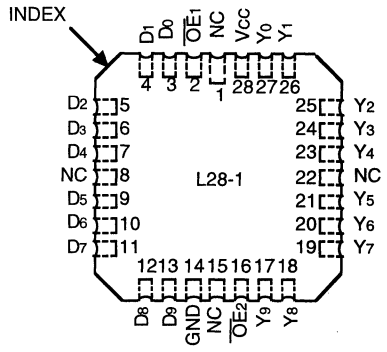
2573 drw 01

PIN CONFIGURATIONS



2573 drw 02

DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW



2573 drw 03

LCC
TOP VIEW

PIN DESCRIPTION

Names	I/O	Description
$\overline{OE}_I$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

2573 tbl 01

FUNCTION TABLE[1]

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, Z = High Impedance

2573 tbl 02

6

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2573 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

2573 lnk 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2573 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA

2573 lnk 06

OUTPUT DRIVE CHARACTERISTICS FOR FCT2827T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		16	48	—	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V[3]		–16	–48	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA	—	0.3	0.50	V

2573 lnk 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]			—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_1 = \overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	FCT827T	—	0.15	0.25	mA/ MHz
				FCT2827T	—	0.06	0.12	
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND One Bit Toggling	V_{IN} = V_{CC}	FCT827T	—	1.5	3.5	mA
			V_{IN} = GND	FCT2827T	—	0.6	2.2	
			V_{IN} = 3.4V	FCT827T	—	1.8	4.5	
			V_{IN} = GND	FCT2827T	—	0.9	3.2	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}_1 = \overline{OE}_2$ = GND Eight Bits Toggling	V_{IN} = V_{CC}	FCT827T	—	3.0	6.0[5]	
			V_{IN} = GND	FCT2827T	—	1.2	3.4[5]	
			V_{IN} = 3.4V	FCT827T	—	5.0	14.0[5]	
			V_{IN} = GND	FCT2827T	—	3.2	11.4[5]	

2573 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

6

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	FCT827AT/FCT2827AT				FCT827BT/FCT2827BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	ns
		CL = 300pF[3] RL = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
tPZH tPZL	Output Enable Time $\overline{OE}$I to YI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		CL = 300pF[3] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$I to YI	CL = 5pF[3] RL = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		CL = 50pF RL = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	

2573 tbl 09

Symbol	Parameter	Condition[1]	FCT827CT/FCT2827CT				FCT827DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI	CL = 50pF RL = 500Ω	1.5	4.4	1.5	5.0	1.5	3.8	—	—	ns
		CL = 300pF[3] RL = 500Ω	1.5	10.0	1.5	11.0	1.5	7.5	—	—	
tPZH tPZL	Output Enable Time $\overline{OE}$I to YI	CL = 50pF RL = 500Ω	1.5	7.0	1.5	8.0	1.5	5.0	—	—	ns
		CL = 300pF[3] RL = 500Ω	1.5	14.0	1.5	15.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time $\overline{OE}$I to YI	CL = 5pF[3] RL = 500Ω	1.5	5.7	1.5	6.7	1.5	4.3	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	7.0	1.5	4.3	—	—	

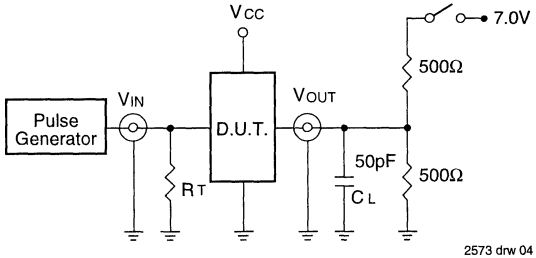
NOTES:

2573 tbl 10

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These conditions are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2573 drw 04

SWITCH POSITION

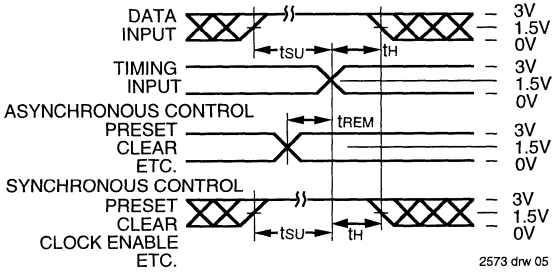
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2573 lnk 11

DEFINITIONS:

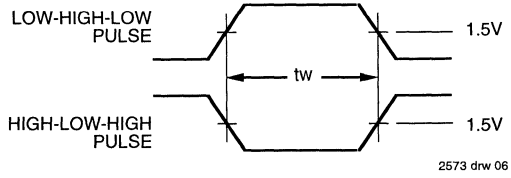
CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



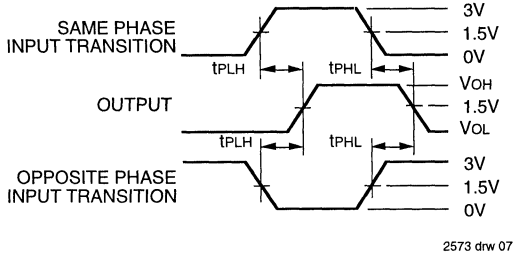
2573 drw 05

PULSE WIDTH



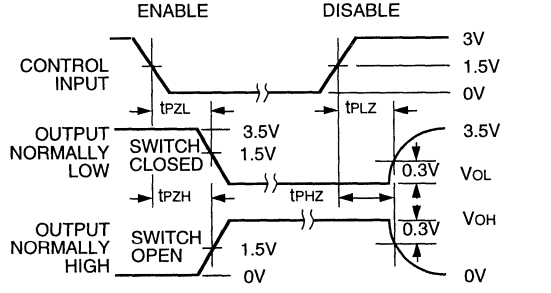
2573 drw 06

PROPAGATION DELAY



2573 drw 07

ENABLE AND DISABLE TIMES



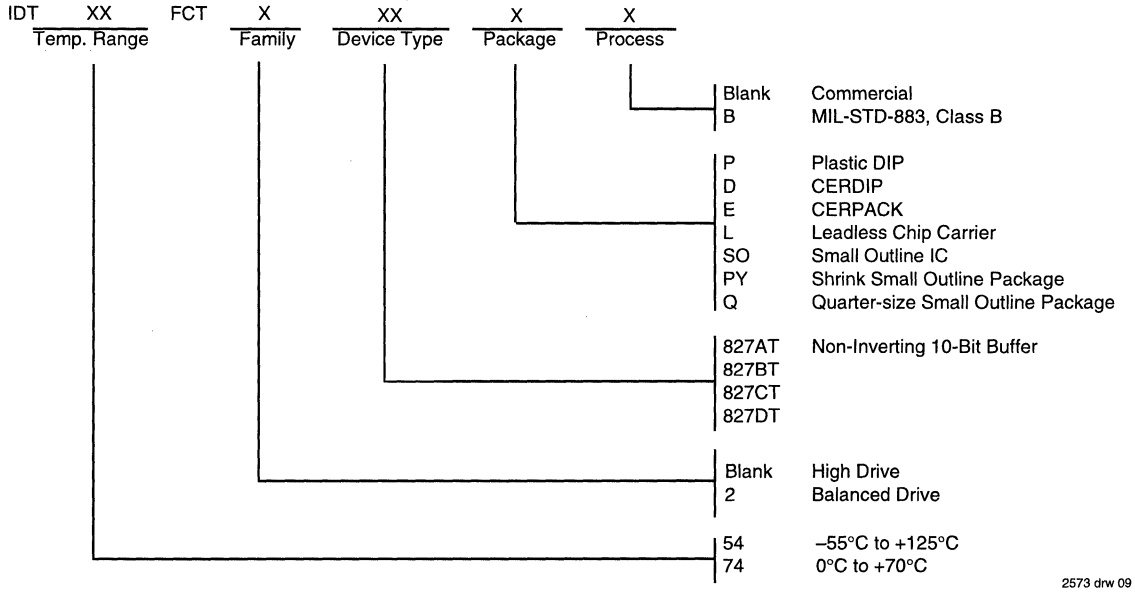
2573 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

6

ORDERING INFORMATION



2573 drw 09

Integrated Device Technology, Inc.

FAST CMOS BUS INTERFACE LATCHES

IDT54/74FCT841AT/BT/CT/DT

FEATURES:

- **Common features:**
  - Low input and output leakage ≤1μA (max.)
  - CMOS power levels
  - True TTL input and output compatibility
    - V_{OH} = 3.3V (typ.)
    - V_{OL} = 0.3V (typ.)
  - Meets or exceeds JEDEC standard 18 specifications
  - Product available in Radiation Tolerant and Radiation Enhanced versions
  - Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
  - Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages
- **Features for FCT841T:**
  - A, B, C and D speed grades
  - High drive outputs (-15mA I_{OH}, 48mA I_{OL})
  - Power off disable outputs permit "live insertion"

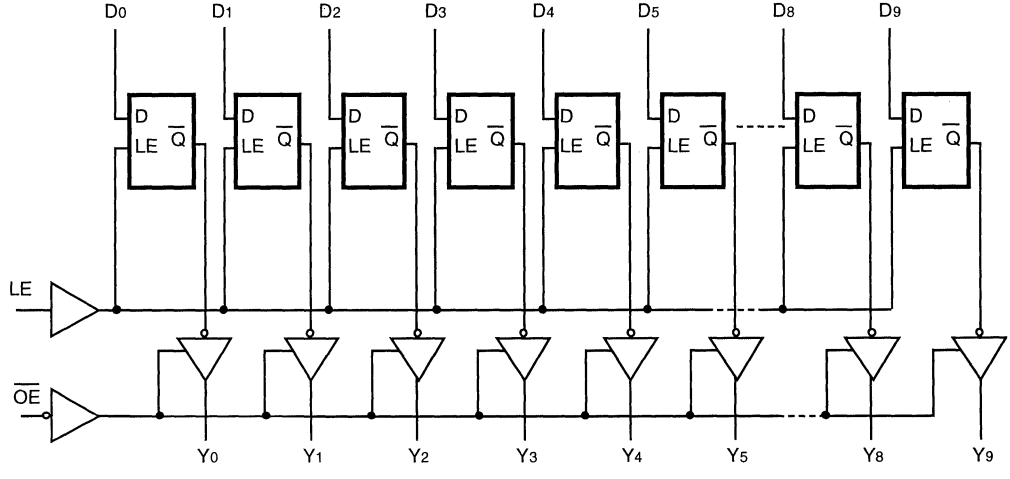
DESCRIPTION:

The FCT8xxT series is built using an advanced dual metal CMOS technology.

The FCT8xxT bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The FCT841T are buffered, 10-bit wide versions of the popular FCT373T function. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

All of the FCT8xxT high-performance interface family can drive large capacitive loads, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes to ground and all outputs are designed for low-capacitance bus loading in high-impedance state.

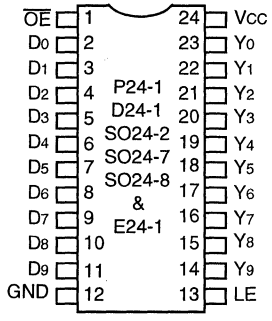
FUNCTIONAL BLOCK DIAGRAM



2571 drw 01

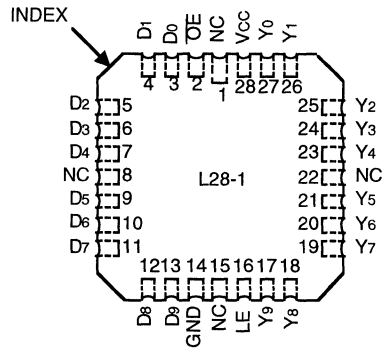
6

PIN CONFIGURATIONS



DIP/SOIC/SSOP/QSOP/CERPACK
TOP VIEW

2571 drw 02



LCC
TOP VIEW

2571 drw 03

PIN DESCRIPTION

Name	I/O	Description
D_I	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_I	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs V_I are in high-impedance (off) state.

2571 tbl 01

FUNCTION TABLE[1]

Inputs			Internal	Output	
$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE:
2571 tbl 02
1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:
2571 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
2571 lnk 04
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]		V_I = 0.5V	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

2571 lnk 05

OUTPUT DRIVE CHARACTERISTICS FOR FCT841T

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

2571 lnk 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4 V_{IN} = GND	— —	1.5 1.8	3.5 4.5	mA
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4 V_{IN} = GND	— —	3.0 5.0	6.0[5] 14.0[5]	

2571 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions[1]	FCT841AT				FCT841BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	13.0	1.5	15.0	
tPLH tPHL	Propagation Delay LE to YI	CL = 50pF RL = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	16.0	1.5	20.0	1.5	15.5	1.5	18.0	
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI	CL = 50pF RL = 500Ω	1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
		CL = 300pF[4] RL = 500Ω	1.5	23.0	1.5	25.0	1.5	14.0	1.5	15.0	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Y I	CL = 5pF[4] RL = 500Ω	1.5	7.0	1.5	9.0	1.5	6.0	1.5	6.5	ns
		CL = 50pF RL = 500Ω	1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	
tSU	Data to LE Set-up Time	CL = 50pF RL = 500Ω	2.5	—	2.5	—	2.5	—	2.5	—	ns
tH	Data to LE Hold Time		2.5	—	3.0	—	2.5	—	2.5	—	ns
tW	LE Pulse Width HIGH[3]		4.0	—	5.0	—	4.0	—	4.0	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

2571 tbl 08

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

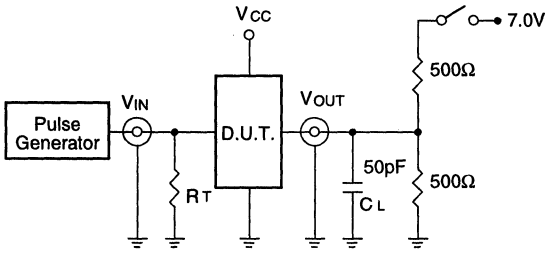
Symbol	Parameter	Conditions[1]	FCT841CT				FCT841DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay DI to YI (LE = HIGH)	CL = 50pF RL = 500Ω	1.5	5.5	1.5	6.3	1.5	4.2	—	—	ns
		CL = 300pF[4] RL = 500Ω	1.5	13.0	1.5	15.0	1.5	8.0	—	—	
tPLH tPHL	Propagation Delay LE to YI	CL = 50pF RL = 500Ω	1.5	6.4	1.5	6.8	1.5	4.0	—	—	ns
		CL = 300pF[4] RL = 500Ω	1.5	15.0	1.5	16.0	1.5	8.0	—	—	
tPZH tPZL	Output Enable Time $\overline{OE}$ to YI	CL = 50pF RL = 500Ω	1.5	6.5	1.5	7.3	1.5	4.8	—	—	ns
		CL = 300pF[4] RL = 500Ω	1.5	12.0	1.5	13.0	1.5	9.0	—	—	
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Y I	CL = 5pF[4] RL = 500Ω	1.5	5.7	1.5	6.0	1.5	4.0	—	—	ns
		CL = 50pF RL = 500Ω	1.5	6.0	1.5	6.3	1.5	4.0	—	—	
tSU	Data to LE Set-up Time	CL = 50pF RL = 500Ω	2.5	—	2.5	—	1.5	—	—	—	ns
tH	Data to LE Hold Time		2.5	—	2.5	—	1.0	—	—	—	ns
tW	LE Pulse Width HIGH[3]		4.0	—	4.0	—	3.0	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.
4. These conditions are guaranteed but not tested.

2571 tbl 09

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2571 drw 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

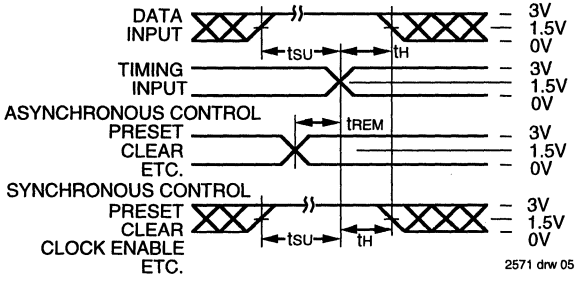
2571 lnk 11

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

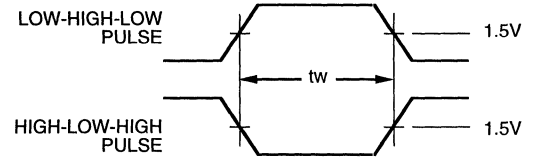
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



2571 drw 05

PULSE WIDTH



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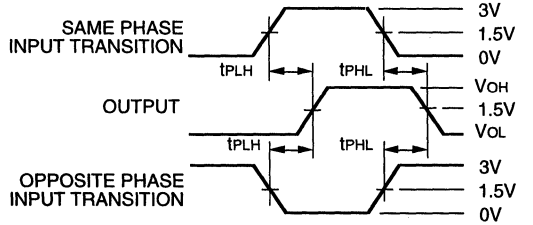
PROPAGATION DELAY



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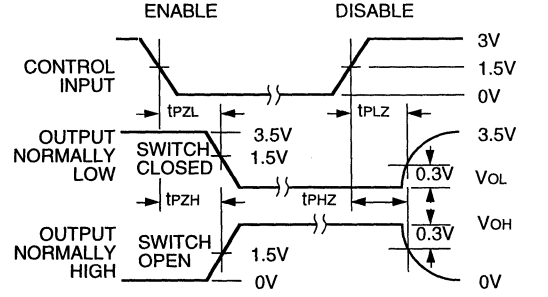
ENABLE AND DISABLE TIMES

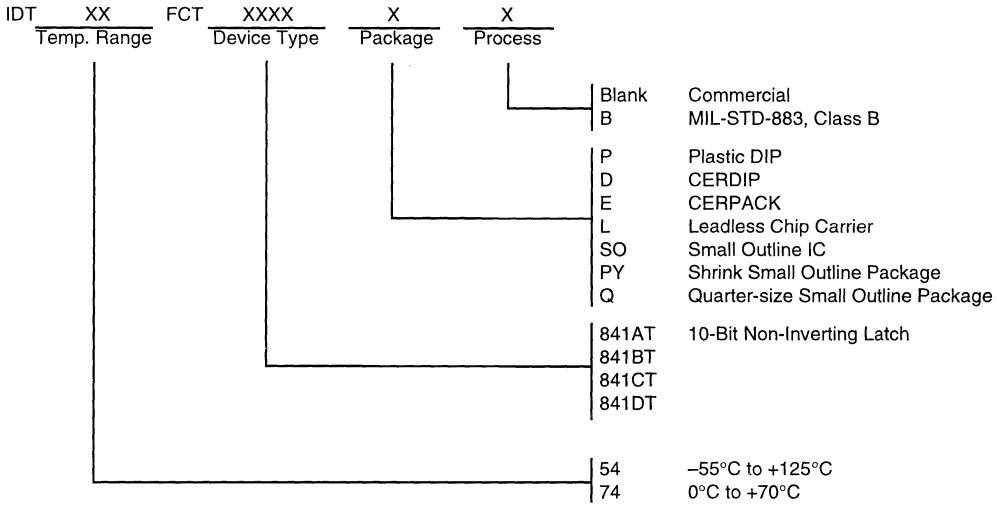


2571 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2571 drw 09

6

FCT CMOS LOGIC

Standard FCT Logic has been designed for high-speed applications which require CMOS rail output voltage levels. The family is pin- and function-compatible with most industry standard bipolar and CMOS Logic families.

FCT Logic is recommended for all applications that require the higher voltage swing of CMOS outputs, and is a significant speed upgrade to AC, ACT, HC, HCT and other standard CMOS components. In applications that can utilize the lower voltage swing of TTL outputs, one of the lower noise FCT-T families should be used instead.

SECTION 7
OCTAL 5V PRODUCTS
TABLE OF CONTENTS

This entire section is available on the IDT electronic data system. Whether you are using the IDT World Wide Web page on the Internet (www.idt.com), ftp server or Fax-On-Demand (1-800-9-IDT-FAX (for U.S. callers); 1-408-492-8391 (outside U.S.)), you will be prompted for a document i.d. number which is listed in the far right column. The data will be immediately downloaded to you.

3.3-VOLT FCT LOGIC PRODUCTS

IDT offers a complete line of FCT 3.3V products for use in general 3.3V applications, especially those requiring high speed and/or low power dissipation. This family includes both the 16-bit, Double-Density devices (FCT163xxx), and the 8-bit, Octal devices (FCT3xxx). In addition, IDT provides FCT 3.3V clock buffers and PLL clock generators to support low-voltage system clocking needs. For 5V-to-3.3V translation, any of the unidirectional 3.3V components may be used. For bi-directional operation a 5V-to-3.3V translator (74FCT164245T) may be used.

IDT's 3.3V components have pinouts and AC specifications that match those of comparable 5V functions. These components are available in several speed grades from standard speed up to "C" speed with 4.1ns propagation delay, providing an easy system performance upgrade path or a simple 5V-to-3.3V conversion.

All of IDT's 3.3V Logic components have series output resistors which reduce line noise, ringing, ground bounce, EMI and other noise related problems. In some applications, these resistors eliminate the need for line termination, or increase system reliability.

The power dissipation levels in IDT's 3.3V FCT Logic are lower than those available in any competing technology. IDT's sub-0.5 micron CMOS technology allows lower dynamic switching currents than found in competing 0.6 micron or 0.8 micron technologies. Also since IDT's FCT 3.3V processes are CMOS, the static power dissipation is negligible compared to levels in BiCMOS technologies.

IDT provides complete data sheet specifications for all 3.3V components over both the extended power supply voltage range of 2.7 to 3.6V and the normal power supply range of 3.0 to 3.6V. The extended range is useful for unregulated battery operation while systems that are restricted to the normal voltage will see improved performance characteristics.

The IDT FCT 3.3V components are compliant with the JEDEC standards for LVCMOS components. FCT 3.3V Logic is also interface compliant with JEDEC standards for LVTTL, but FCT is capable of lower power dissipation levels than the biCMOS processes of LVTTL. The following data sheets list the device specifications. Application Note 124, which is available in the *IDT High-Speed Logic CMOS Design Guide,* contains additional device characteristic and application information.

FCT 3.3V Double-Density

FCT 3.3V Double-Density Logic is available in a variety of functions that are pin- and function-compatible with 5V, 16-bit components, allowing a quick upgrade path from 5V to 3.3V operation. All Double-Density components are specified with a maximum output skew of 500ps. IDT's Double-Density 3.3V components have negligible static power dissipation, and the lowest dynamic power dissipation in the industry, due to the sub 0.5 micron CMOS technology used. Double-Density components are available in SSOP, TSSOP and CERPAK configurations.

FCT 3.3V Octals

FCT 3.3V octals are available in standard functions allowing a quick upgrade from 5V to 3.3V operation. All FCT 3.3V octals retain the low power dissipation of IDT's CMOS process. FCT 3.3V octal components are available in SSOP, SOIC, QSOP, CERPAK and other popular configurations.

FCT 3.3V Clock Generators and Clock Buffers

IDT manufactures several FCT high-speed, low-skew clock buffers and clock generators. These components have been designed for very low-skew clock distribution applications. Due to the low-power dissipation in IDT's CMOS process, these components are capable of high-frequency operation beyond those of competing technologies.

SECTION 8
3.3V LOGIC PRODUCTS
TABLE OF CONTENTS

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BUFFER/LINE DRIVER

IDT54/74FCT163244/A/C

FEATURES:

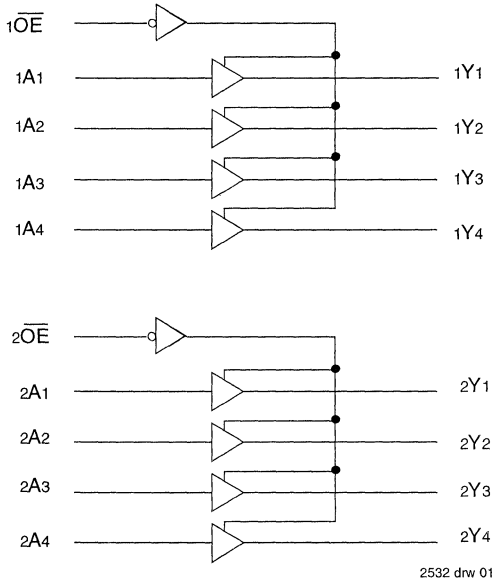
- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

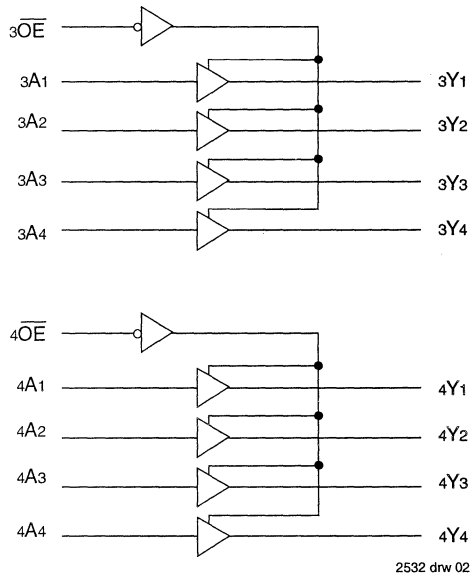
The FCT163244/A/C 16-bit buffer/line drivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices offer bus/backplane interface capability with improved packing density. These devices have a flow-through organization for simplifying board layout. The three-state controls operate these devices in a Quad-Nibble, Dual-Byte or single 16-bit word mode. All inputs are designed with hysteresis for improved noise margin.

The inputs of the FCT163244/A/C can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system. Thus, the FCT163244/A/C can be used as buffers to connect 5V components to a 3.3V bus.

FUNCTIONAL BLOCK DIAGRAM



2532 drw 01



2532 drw 02

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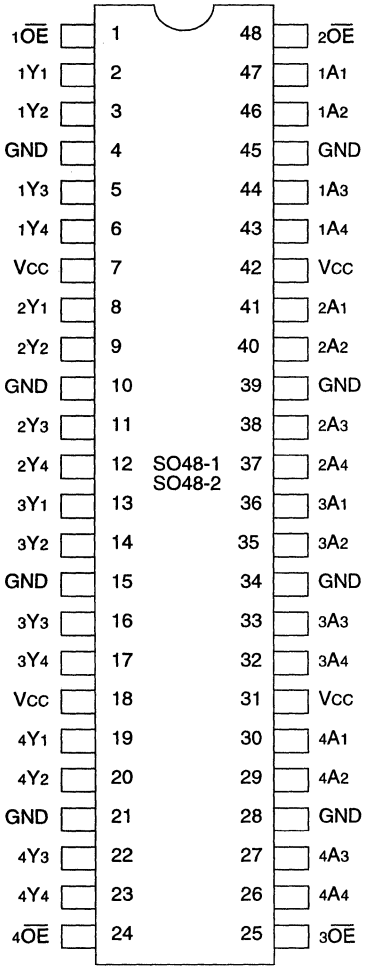
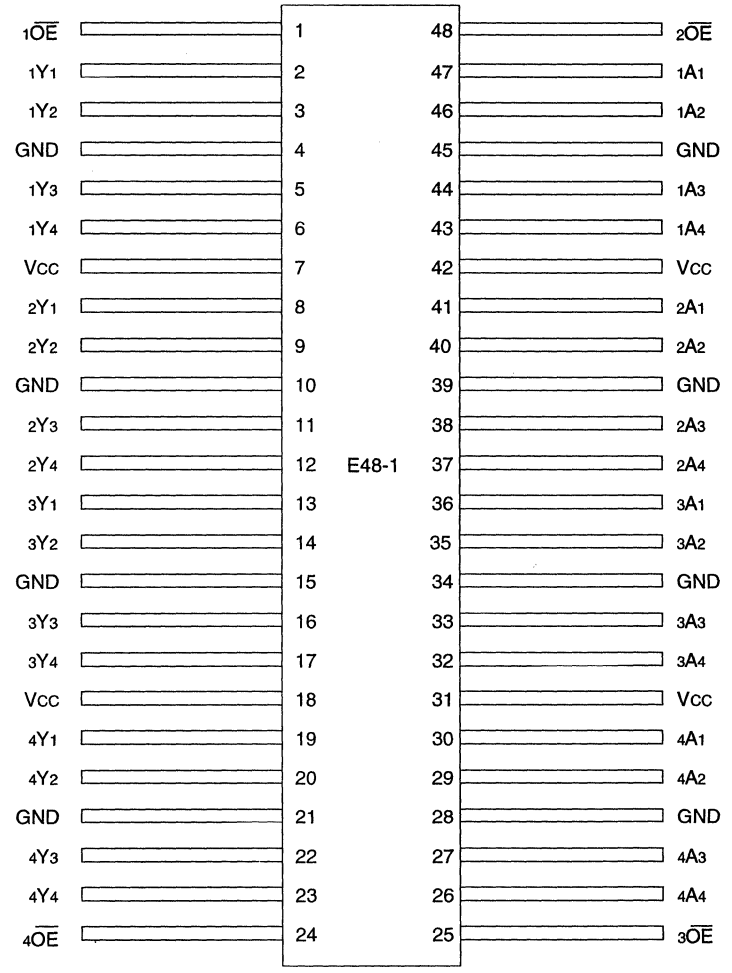
The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



2532 drw 03

SSOP
TSSOP
TOP VIEW



2532 drw 04

CERPACK
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2532 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

2532 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 2532 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2532 lnk 04
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	Vcc+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
I_{CCZ}			MIL.	—	0.1	100	

2532 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open 50% Duty Cycle $x\overline{OE}$ = GND One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.5	0.8	mA
		50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.5	0.8	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	2.0	3.0[5]	
		50% Duty Cycle $x\overline{OE}$ = GND Sixteen Bits Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	2.0	3.3[5]	

2532 tbl 06

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

			FCT163244				FCT163244A				FCT163244C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	1.5	4.1			ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8			ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	1.5	5.2			ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5			ns

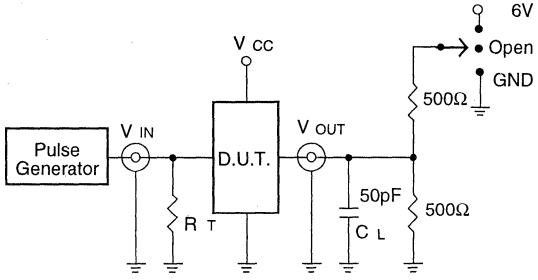
2532 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

8

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2532 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

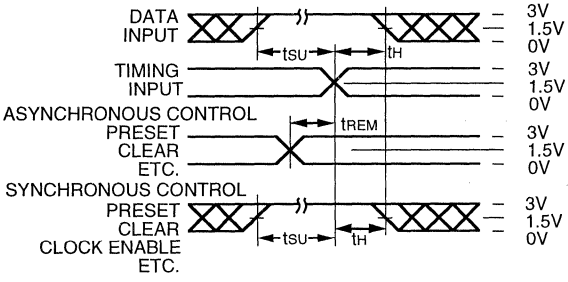
2532 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

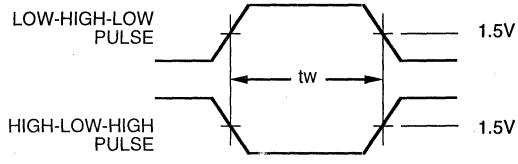
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



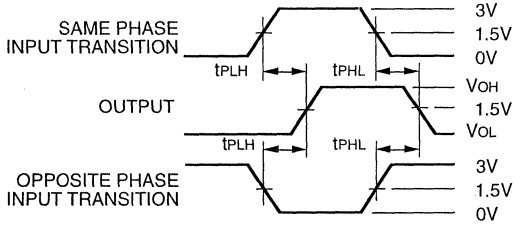
2532 drw 06

PULSE WIDTH



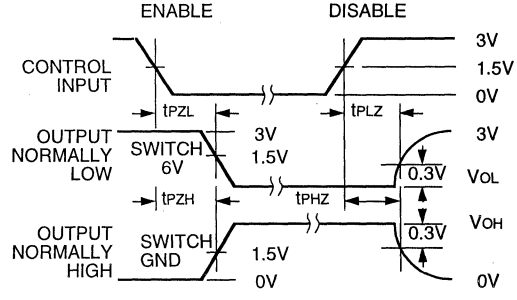
2532 drw 07

PROPAGATION DELAY



2532 drw 08

ENABLE AND DISABLE TIMES

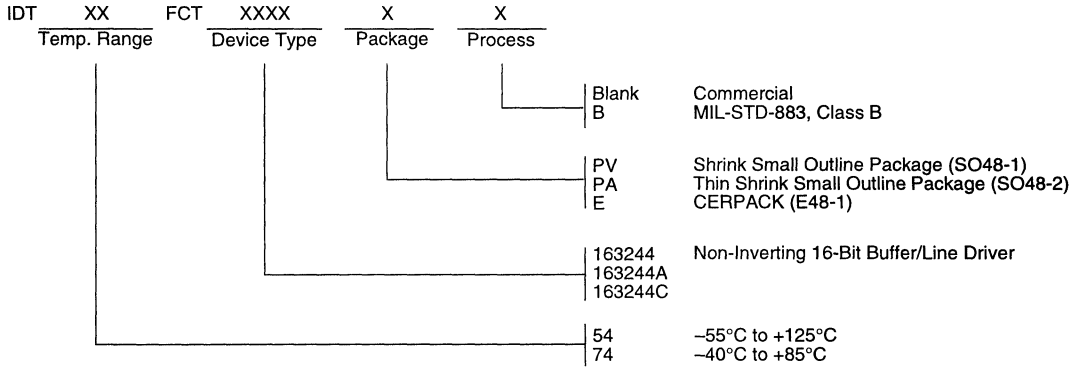


2532 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION



2532 tbl 07

8

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT163245/A/C

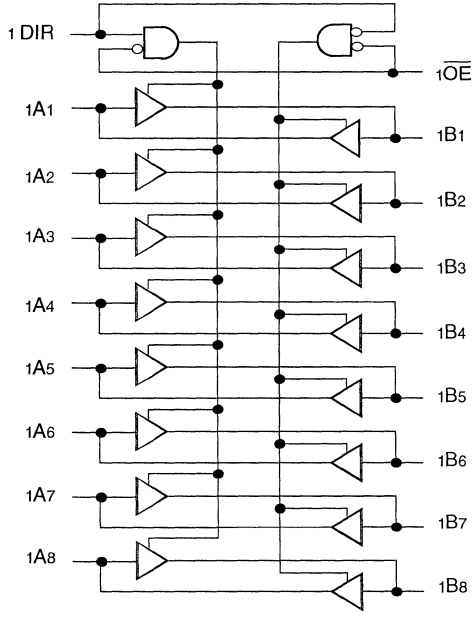
FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

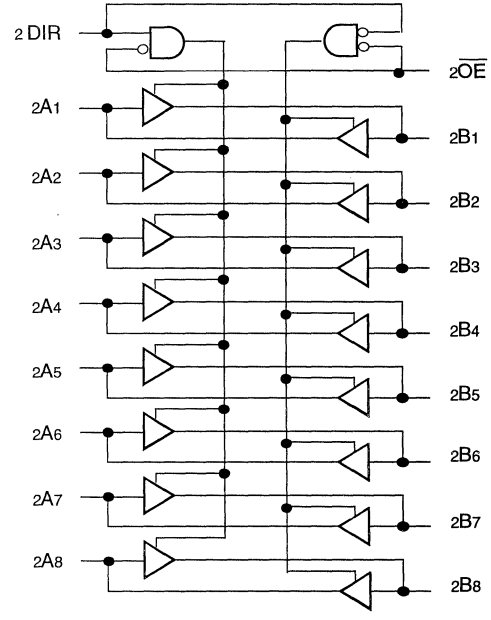
DESCRIPTION:

The FCT163245/A/C 16-bit transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The Direction and Output Enable controls are designed to operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin ($x\overline{OE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

FUNCTIONAL BLOCK DIAGRAM

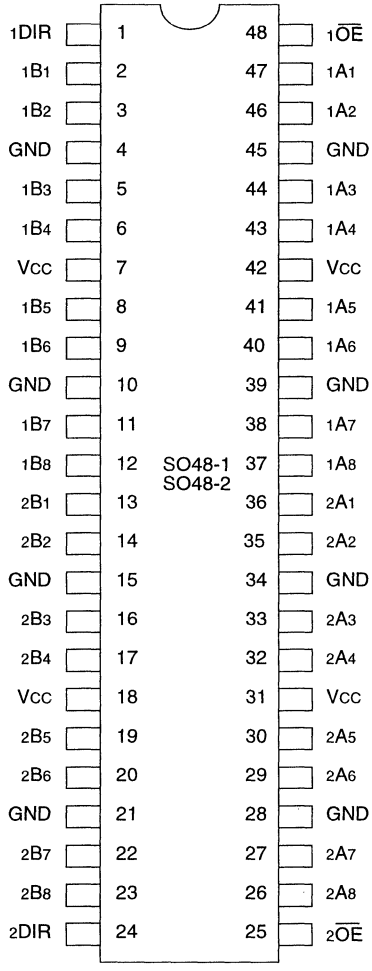


2554 drw 01



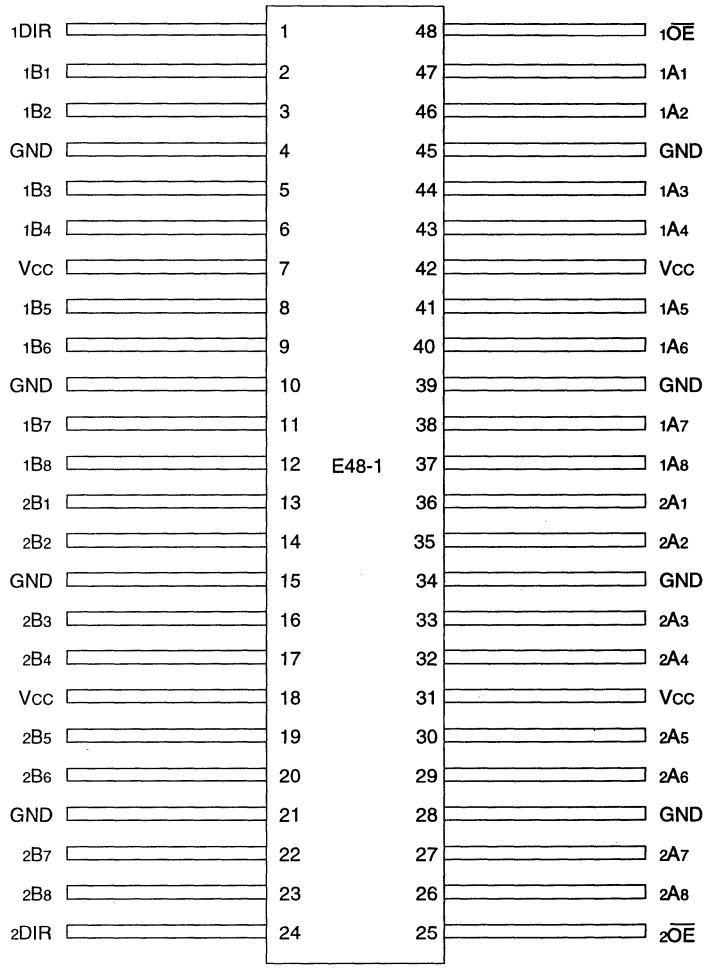
2554 drw 02

PIN CONFIGURATIONS



2554 drw 03

SSOP
TSSOP
TOP VIEW



2554 drw 04

CERPACK
TOP VIEW

8

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs
xBx	Side B Inputs or 3-State Outputs

2554 tbl 01

FUNCTION TABLE(1)

Inputs		Outputs
$x\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE: 2554 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 2554 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2554 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

2554 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

8

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = xDIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.5	0.8	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.5	0.8	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.0	3.0[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	2.0	3.3[5]	

2554 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

			FCT163245				FCT163245A				FCT163245C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	1.5	4.1	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to A or B[5]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	1.5	5.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to A or B[5]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	1.5	4.8	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

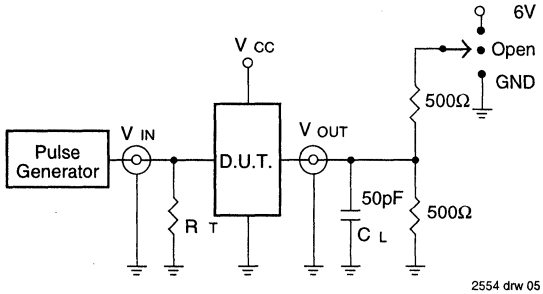
2554 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
5. This parameter is guaranteed but not tested.

8

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2554 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

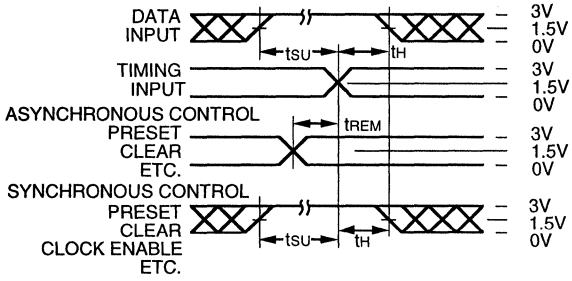
2554 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

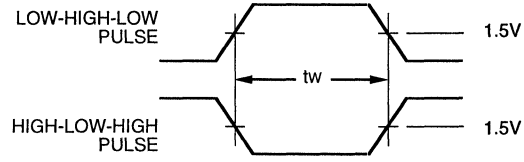
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



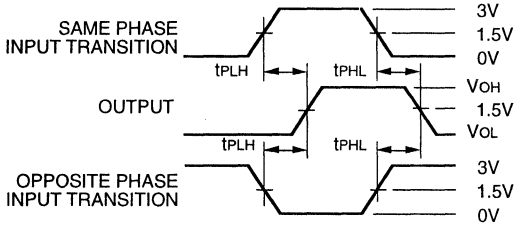
2554 drw 06

PULSE WIDTH



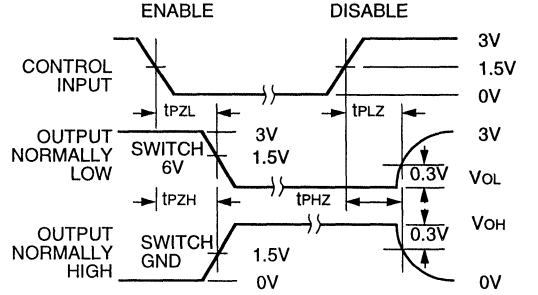
2554 drw 07

PROPAGATION DELAY



2554 drw 08

ENABLE AND DISABLE TIMES

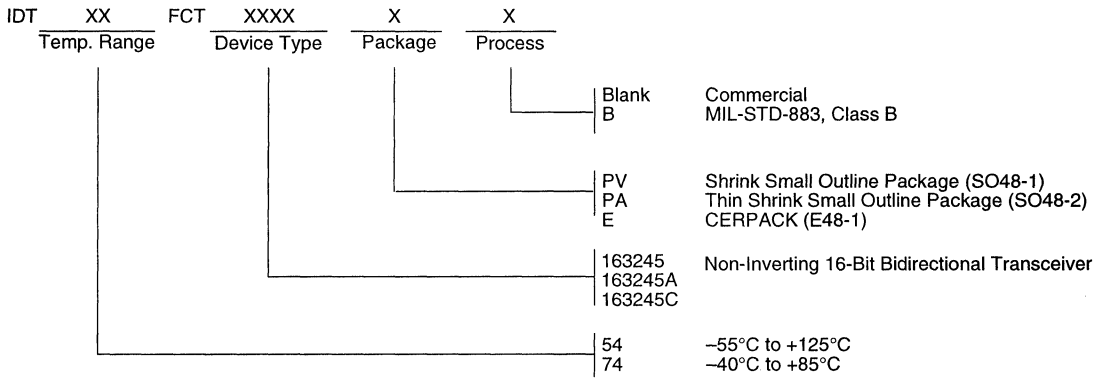


2554 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION



2554 drw 10

8

Integrated Device Technology, Inc.

3.3V CMOS ADDRESS/ CLOCK DRIVER

IDT54/74FCT163344/A/C
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

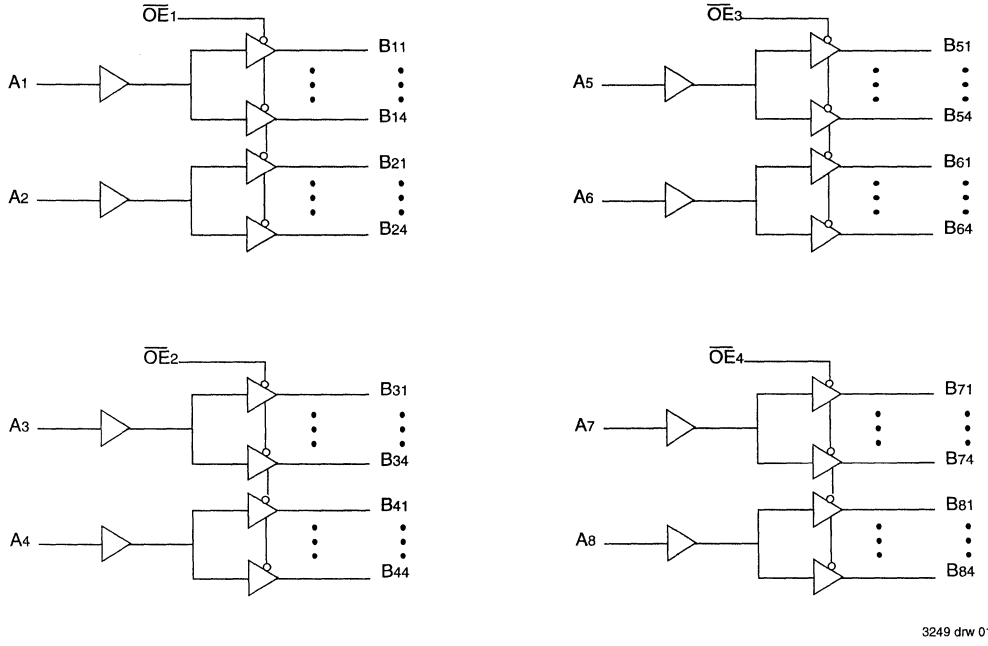
The FCT163344/A/C is a 1:4 address line driver built using advanced dual metal CMOS technology. This high-speed, low power device provides the ability to fanout to memory arrays. Eight banks, each with a fanout of 4, and 3-state control provide efficient address distribution. One or more banks may be used for clock distribution.

The FCT163344/A/C have series current limiting resistors. These offer low ground bounce, minimal undershoot and controlled output fall times, reducing the need for external series terminating resistors.

A large number of power and ground pins ensure reduced noise levels. All inputs are designed with hysteresis for improved noise margins.

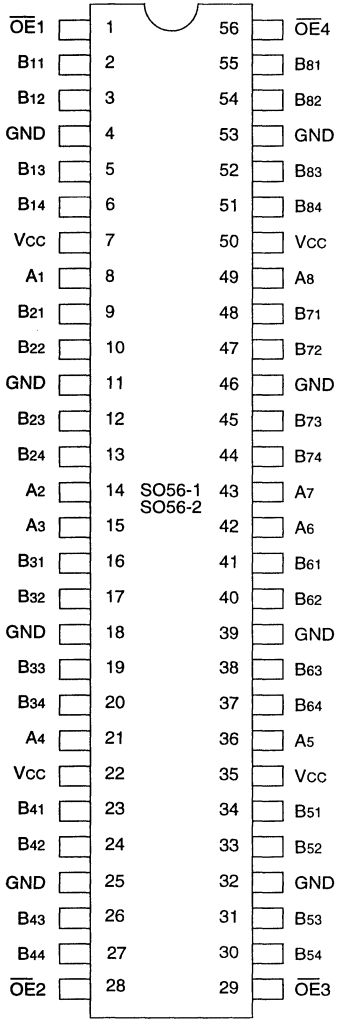
The inputs of the FCT163344/A/C can be driven from either 3.3V or 5V device. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM



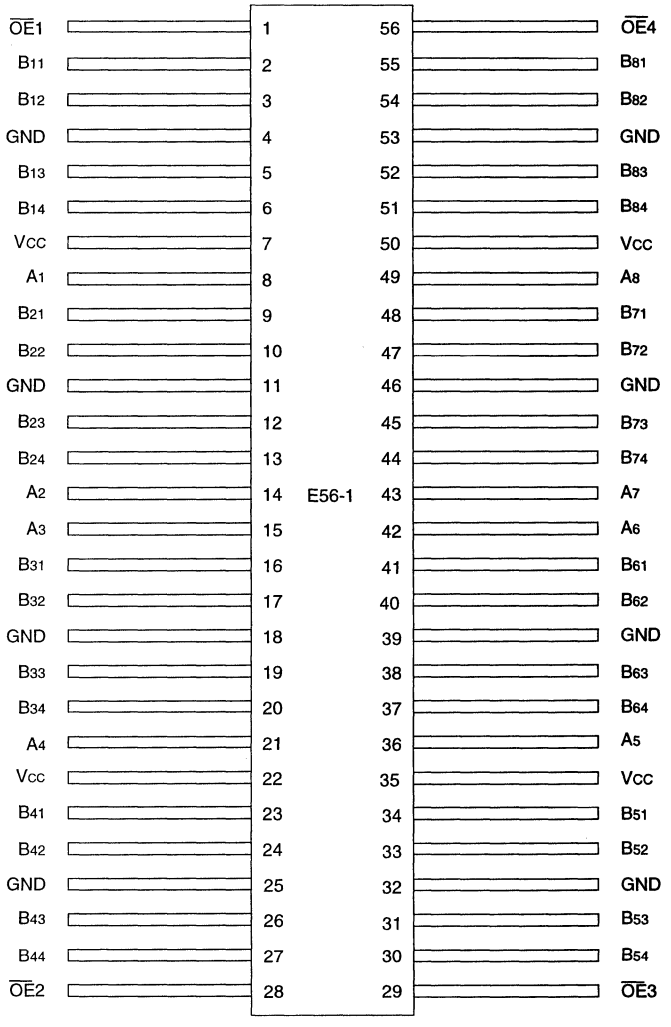
3249 drw 01

PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

3249 drw 02



CERPACK
TOP VIEW

3249 drw 03

8

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}x$	3–State Output Enable Inputs (Active LOW)
Ax	Inputs
Bxx	3-State Outputs

3249 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

3249 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

FUNCTION TABLE(1)

Inputs		Outputs
$\overline{OE}x$	Ax	Bxx
L	L	L
L	H	H
H	X	Z

3249 tbl 02

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

3249 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

3249 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

8

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} -0.6V[3]		—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}x$ = GND One Input Bit Toggling Four Output Bits Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—			µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE}x$ = GND One Input Bit Toggling Four Output Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—			mA
			V_{IN} = V_{CC} -0.6V V_{IN} = GND	—			
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}x$ = GND Eight Input Bits Toggling Thirty Two Output Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—			
			V_{IN} = V_{CC} -0.6V V_{IN} = GND	—			

3249 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[5]

Symbol	Parameter	Condition[1]	FCT163344				FCT163344A				FCT163344C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Ax to Bxx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	1.5	4.3	1.5	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$x to Bx		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	1.5	5.8	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$x to Bx		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	1.5	5.2	1.5	5.7	ns
$t_{SK1(o)}$	Skew between outputs of same bank and same package (same transition)[3,4]		—	0.75	—	0.75	—	0.5	—	0.5	—	0.35	—	0.35	ns
$t_{SK2(o)}$	Skew between outputs of all banks of same package (A1 thru A8 tied together)[3,4]		—	1.0	—	1.0	—	0.5	—	0.5	—	0.5	—	0.5	ns

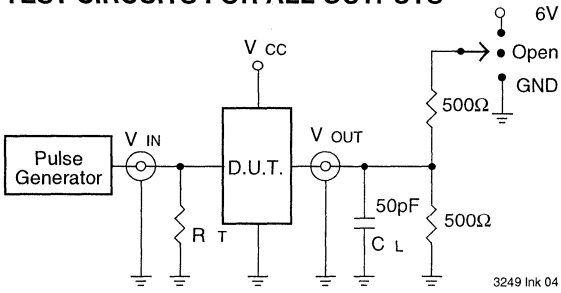
3249 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.
5. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

8

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



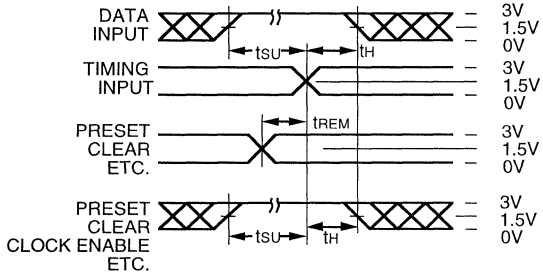
3249 lnk 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

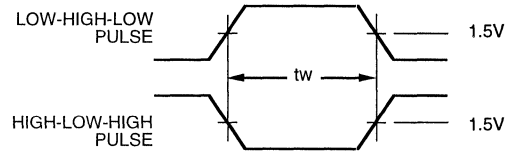
3249 lnk 08

SET-UP, HOLD AND RELEASE TIMES



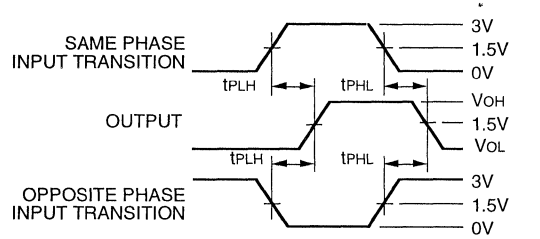
3249 lnk 05

PULSE WIDTH



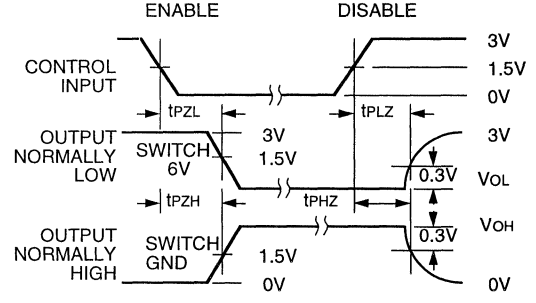
3249 lnk 06

PROPAGATION DELAY



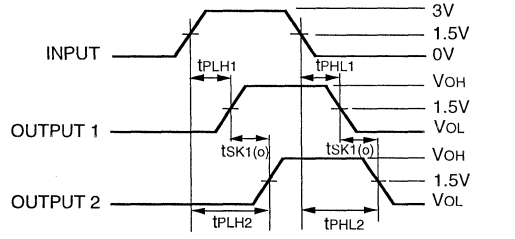
3249 lnk 07

ENABLE AND DISABLE TIMES



3249 lnk 09

OUTPUT SKEW - tSKn(o)



$t_{SKn(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PLH1}|$

3249 lnk 08

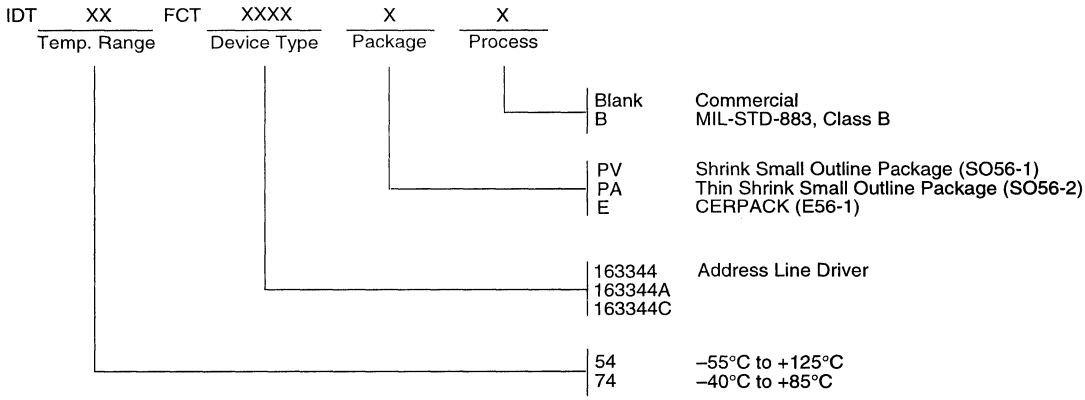
NOTE:

1. For $t_{SK1}(o)$ OUTPUT1 and OUTPUT 2 are in the same bank, For $t_{SK2}(o)$ OUTPUT1 and OUTPUT 2 are in different banks on the same part.

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If Vcc is below 3V, input voltage swings should be adjusted not to exceed Vcc.

ORDERING INFORMATION



3249 drw 10

8

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT TRANSPARENT LATCH

IDT54/74FCT163373/A/C

FEATURES:

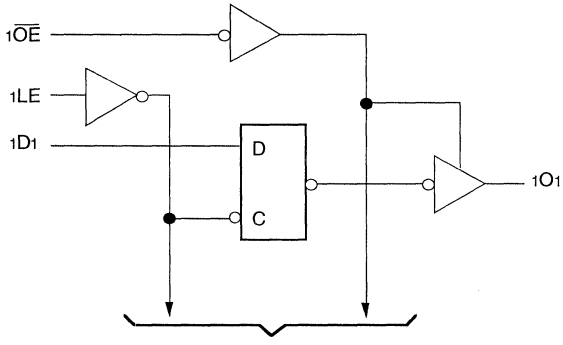
- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

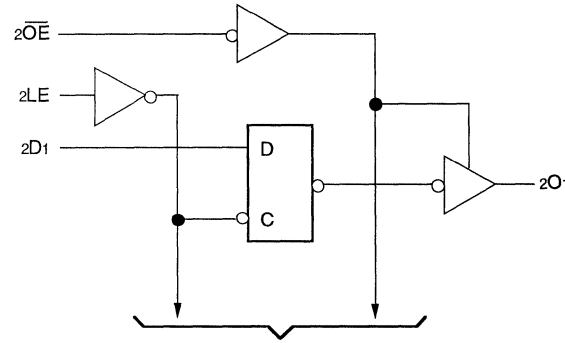
The FCT163373/A/C 16-bit transparent D-type latches are built using advanced dual metal CMOS technology. These high-speed, low-power latches are ideal for temporary storage of data. They can be used for implementing memory address latches, I/O ports, and bus drivers. The Output Enable and Latch Enable controls are organized to operate each device as two 8-bit latches or one 16-bit latch. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The inputs of FCT163373/A/C can be driven from either 3.3V or 5V devices. This feature allows the use of these transparent latches as translators in a mixed 3.3V/5V supply system. With xLE inputs HIGH, the FCT163373/A/C can be used as buffers to connect 5V components to a 3.3V bus.

FUNCTIONAL BLOCK DIAGRAM

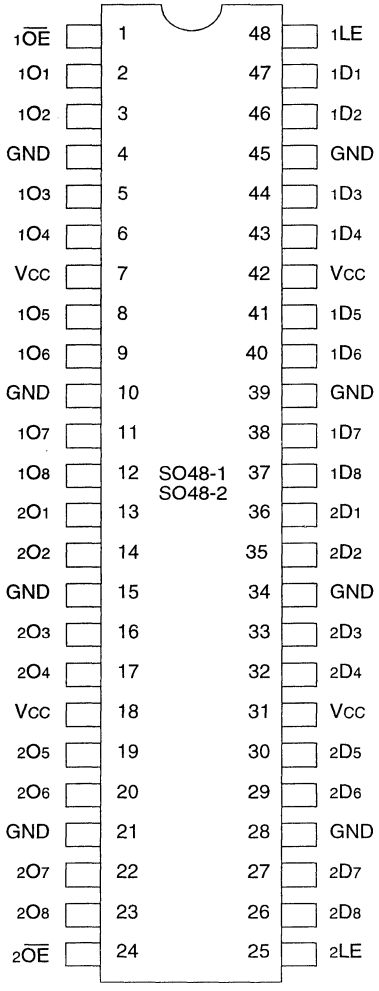


2601 drw 01



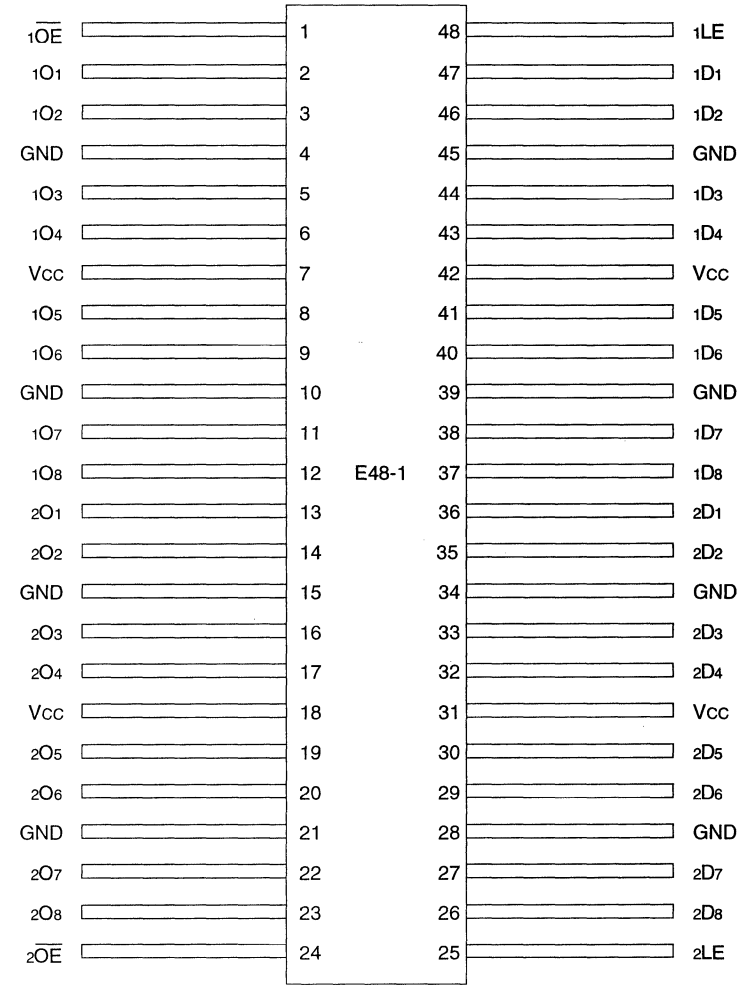
2601 drw 02

PIN CONFIGURATIONS



2601 drw 03

SSOP
TSSOP
TOP VIEW



2601 drw 04

CERPACK
TOP VIEW

8

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xLE	Latch Enable Input (Active HIGH)
$x\overline{OE}$	Output Enable Input (Active LOW)
xOx	3-State Outputs

2601 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xDx	xLE	$x\overline{OE}$	xOx
H	H	L	H
L	H	L	L
X	X	H	Z

2601 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

2601 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2601 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

2601 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

8

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open x$\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle x$\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.5	0.8	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.5	0.8	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle x$\overline{OE}$ = GND xLE = V_{CC} Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.0	3.0[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	2.0	3.3[5]	

2601 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

Symbol	Parameter	Condition[1]	FCT163373				FCT163373A				FCT163373C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay xDx to xOx	CL = 50pF RL = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	1.5	4.2	—	—	ns
tPLH tPHL	Propagation Delay xLE to xOx		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	2.0	5.5	—	—	ns
tPZH tPZL	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	1.5	5.5	—	—	ns
tPHZ tPLZ	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	1.5	5.0	—	—	ns
tSU	Set-up Time HIGH or LOW, xDx to xLE		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW, xDx to xLE		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
tW	xLE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	5.0	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

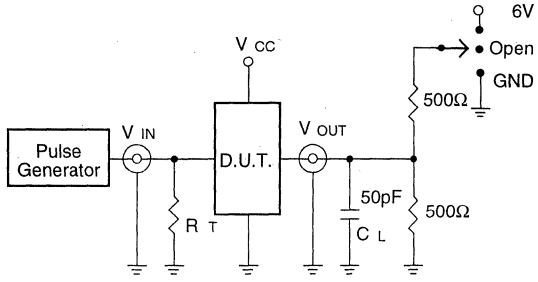
2601 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

8

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2601 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

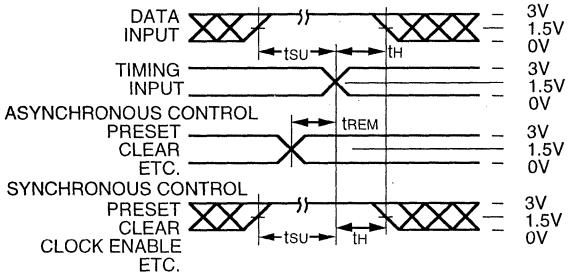
2601 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

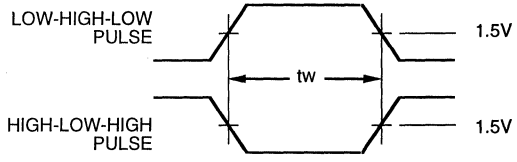
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



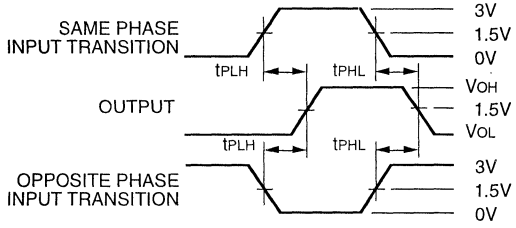
2601 drw 06

PULSE WIDTH



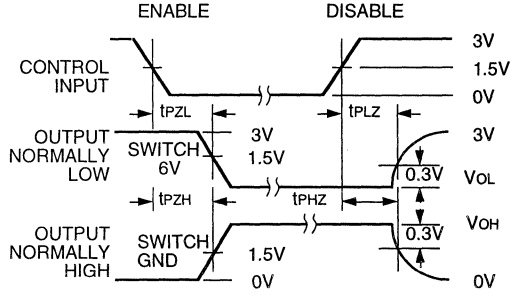
2601 drw 07

PROPAGATION DELAY



2601 drw 08

ENABLE AND DISABLE TIMES

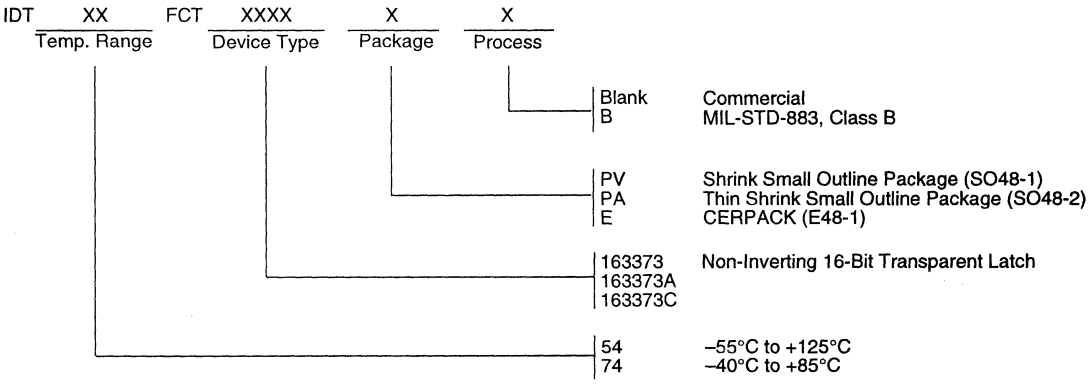


2601 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION



2601 drw 10

8

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT REGISTER (3-STATE)

IDT54/74FCT163374/A/C

FEATURES:

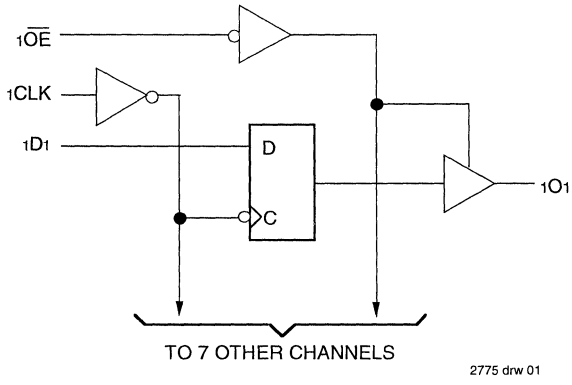
- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

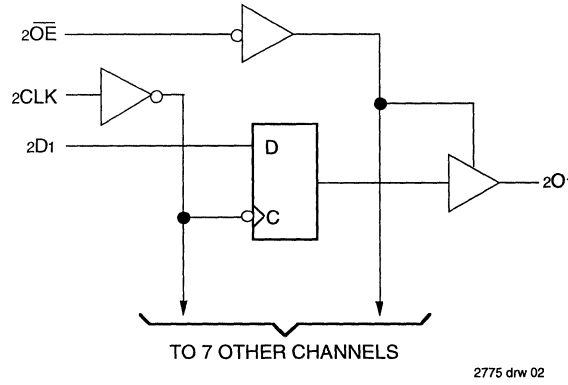
The FCT163374/A/C 16-bit edge-triggered D-type registers are built using advanced dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable (x$\overline{OE}$) and clock (xCLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

The inputs of FCT163374/A/C can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM

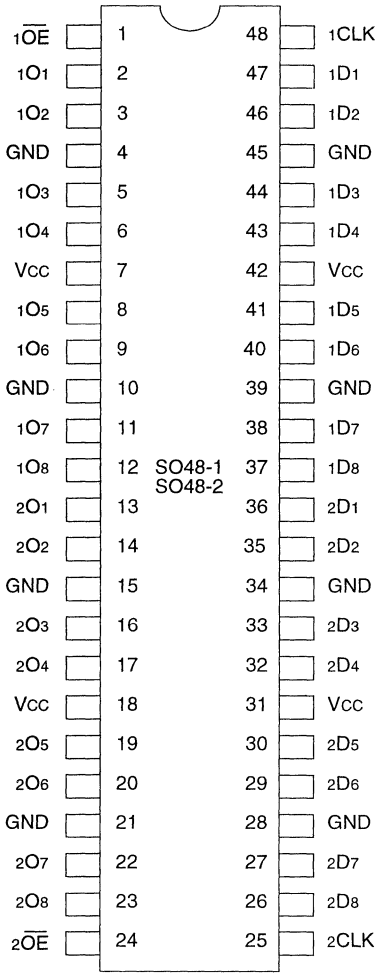


2775 drw 01



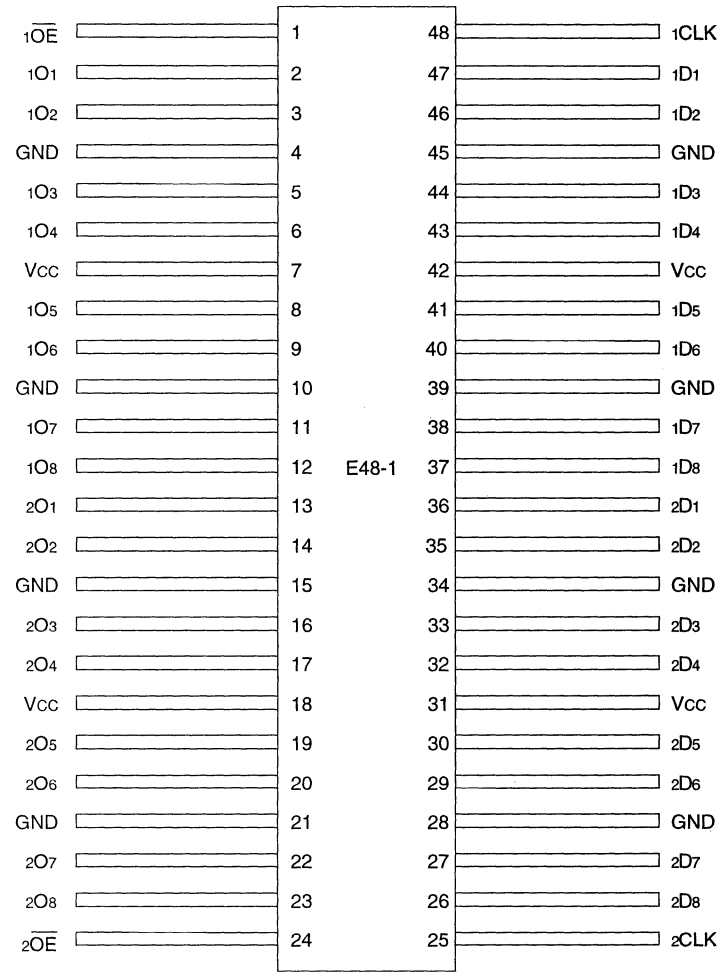
2775 drw 02

PIN CONFIGURATIONS



2775 drw 03

SSOP
TSSOP
TOP VIEW



2775 drw 04

CERPACK
TOP VIEW

8

PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs
xCLK	Clock Inputs
xOx	3-State Outputs.
$x\overline{OE}$	3-State Output Enable Input (Active LOW)

2775 tbl 01

FUNCTION TABLE[1]

Function	Inputs			Outputs
	xDx	xCLK	$x\overline{OE}$	xOx
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH transition

2775 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES:

2775 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE:

2775 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

NOTES:

2775 lnk 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}$ = GND 50% Duty Cycle One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.5	0.8	mA
		$x\overline{OE}$ = GND f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.5	0.8	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	2.5	3.8[5]	
		$x\overline{OE}$ = GND f_i = 2.5MHz 50% Duty Cycle Sixteen Bits Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	2.5	4.0[5]	

2775 tbl 07

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

			FCT163374				FCT163374A				FCT163374C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLK to xOx	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	2.0	5.2	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	1.5	5.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	1.5	5.0	—	—	ns
t_{SU}	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
t_W	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

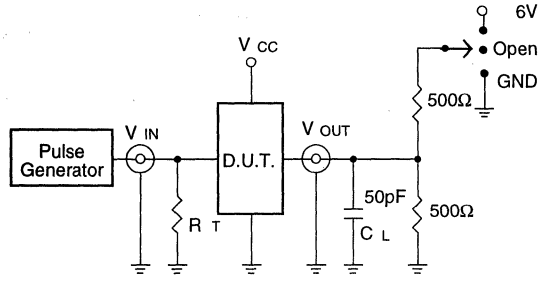
NOTES:
2775 tbl 08

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delay and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

8

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2775 drw 05

SWITCH POSITION

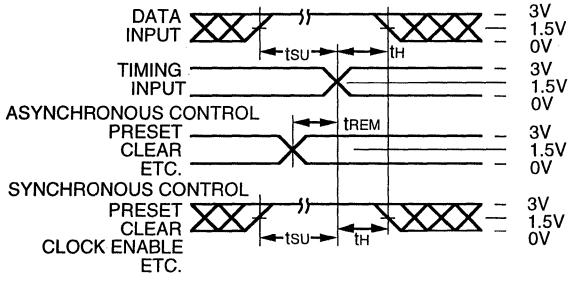
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

2775 lnk 09

DEFINITIONS:

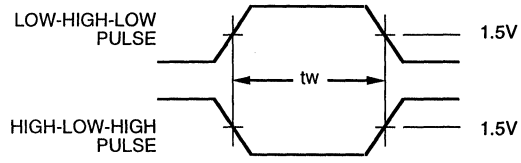
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



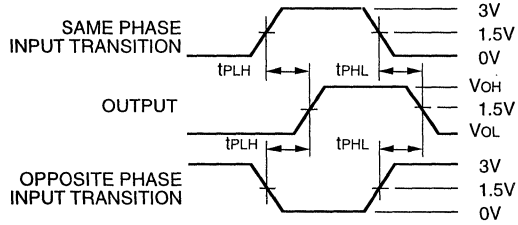
2775 drw 06

PULSE WIDTH



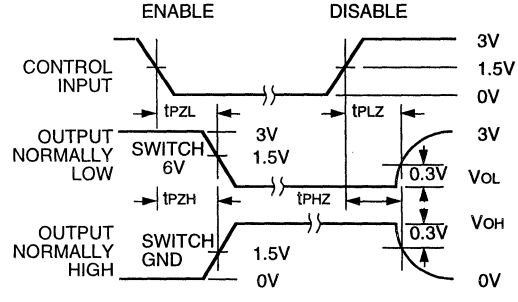
2775 drw 07

PROPAGATION DELAY



2775 drw 08

ENABLE AND DISABLE TIMES

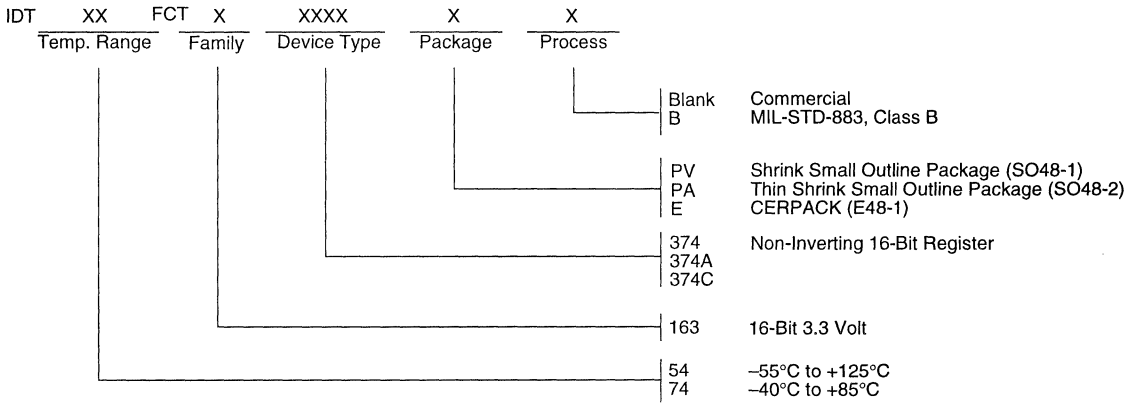


2775 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION



2775 drw 10

8

Integrated Device Technology, Inc.

3.3V CMOS 18-BIT REGISTERED TRANSCEIVER

IDT54/74FCT163501/A/C

FEATURES:

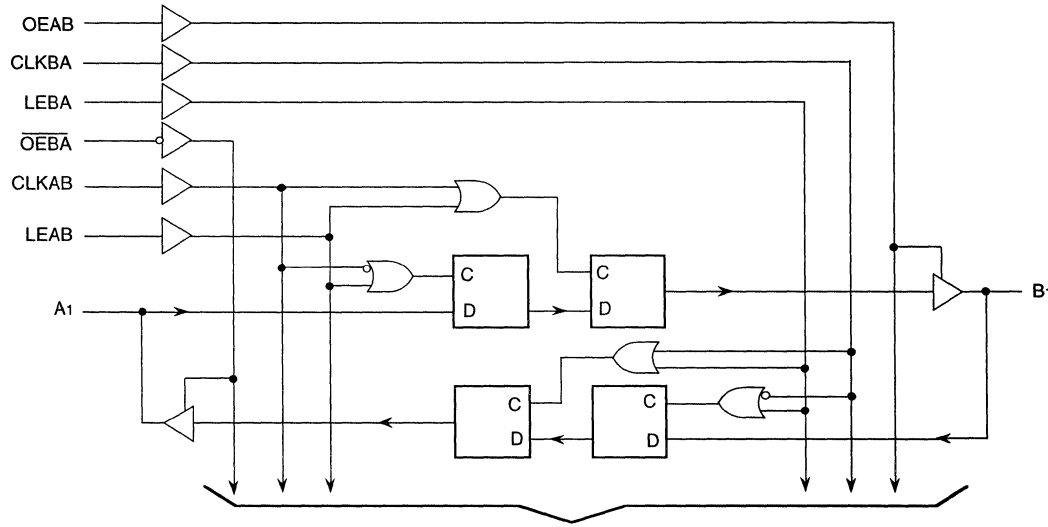
- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

The FCT163501/A/C 18-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power 18-bit registered bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch enable (LEAB and LEBA) and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB. OEAB performs the output enable function on the B port. Data flow from B port to A port is similiar but requires using $\overline{OEBA}$, LEBA and CLKBA. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

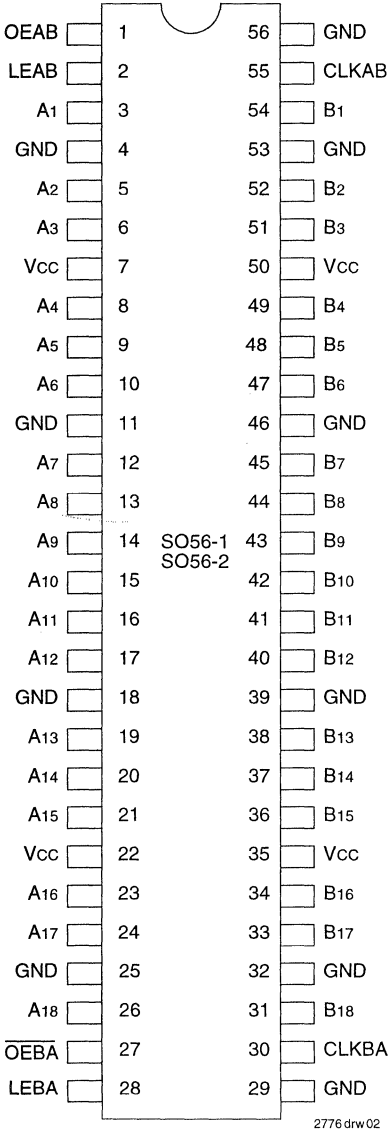
The FCT163501/A/C have series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM

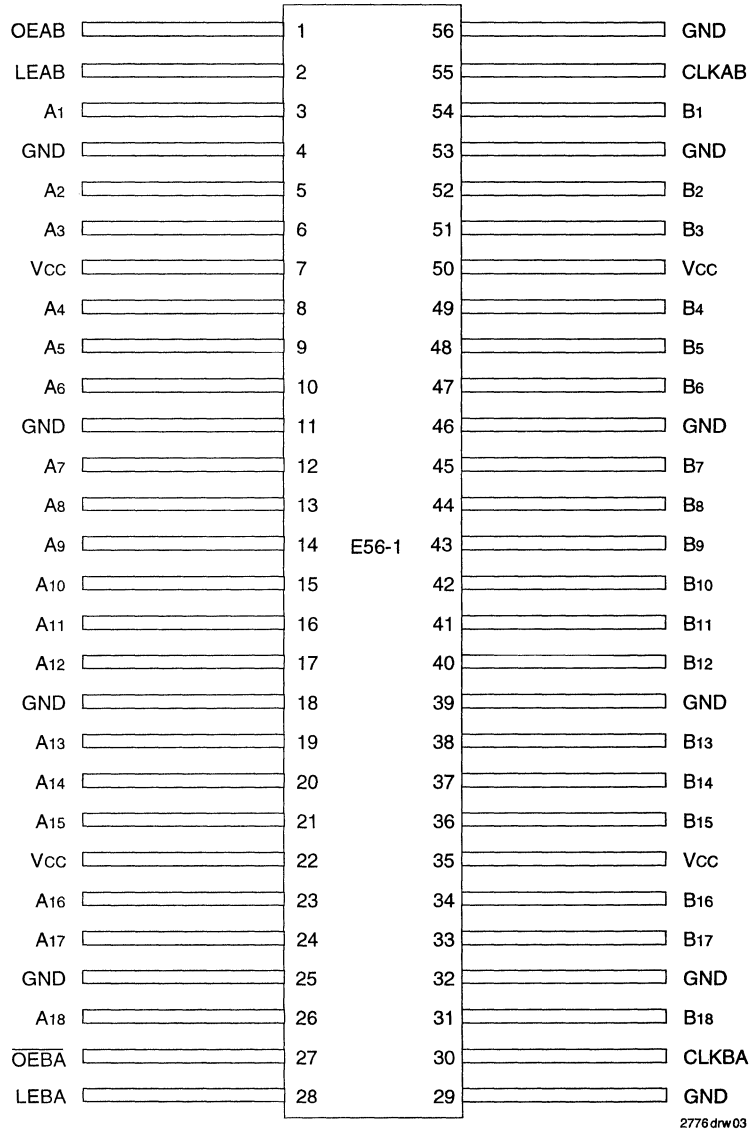


2776 drw 01

PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW



CERPACK
TOP VIEW

8

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

2776 tbl 01

FUNCTION TABLE[1,4]

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B[2]
H	L	H	X	B[3]

2776 tbl 02

NOTES:
1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

2776 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

2776 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	Vcc+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	Vcc = Max.	VI = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		VI = Vcc	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		VI = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		VI = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	Vcc = Max.	VO = Vcc	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		VO = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	Vcc = 3.3V, V_{IN} = V_{IH} or V_{IL}, VO = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	Vcc = 3.3V, V_{IN} = V_{IH} or V_{IL}, VO = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	Vcc = Min.	I_{OH} = –0.1mA	Vcc–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		Vcc = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	Vcc = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		Vcc = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	Vcc = Max., VO = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

2776 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = Vcc –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

8

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND 50% Duty Cycle One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND fi = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.0	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.6	1.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND fi = 2.5MHz 50% Duty Cycle Eighteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.0[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	3.0	5.3[5]	

2776 tbl 08

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + fiN_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   fi = Input Frequency
   N_i = Number of Inputs at fi

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

Symbol	Parameter		Condition[1]	FCT163501				FCT163501A				FCT163501C				Unit
				Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
f_{MAX}	CLKAB or CLKBA frequency		C_L = 50pF	—	100	—	100	—	150	—	150	—	150	—	—	MHz
t_{PLH} t_{PHL}	Propagation Delay Ax to Bx or Bx to Ax		R_L = 500Ω	1.5	6.5	1.5	7.5	1.5	5.1	1.5	5.6	1.5	4.6	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx			1.5	7.5	1.5	8.0	1.5	5.6	1.5	6.0	1.5	5.3	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx			1.5	8.0	1.5	9.0	1.5	5.6	1.5	6.0	1.5	5.3	—	—	ns
t_{PLH} t_{PHL}	Output Enable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	8.0	1.5	9.0	1.5	6.0	1.5	6.4	1.5	5.6	—	—	ns
t_{PZH} t_{PZL}	Output Disable Time $\overline{OEBA}$ to Ax, OEAB to Bx			1.5	7.5	1.5	8.0	1.5	5.6	1.5	6.0	1.5	5.2	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA			4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
t_H	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA			0	—	0	—	0	—	0	—	0	—	—	—	ns
t_{SU}	Set-up Time HIGH or LOW	Clock LOW		4.0	—	4.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
	Ax to LEAB, Bx to LEBA	Clock HIGH		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
t_H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA			1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
t_W	LEAB or LEBA Pulse Width HIGH[5]			3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
t_W	CLKAB or CLKBA Pulse Width HIGH or LOW[5]			3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	—	—	ns
$t_{SK(o)}$	Output Skew[3]			—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

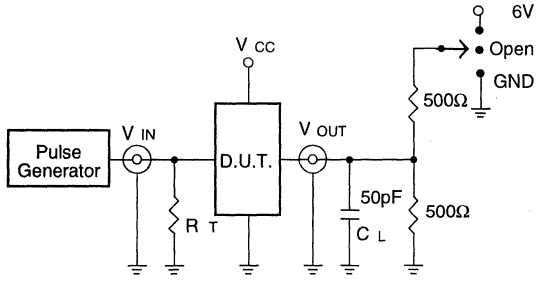
2776 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
5. This parameter is guaranteed but not tested.

8

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2776 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

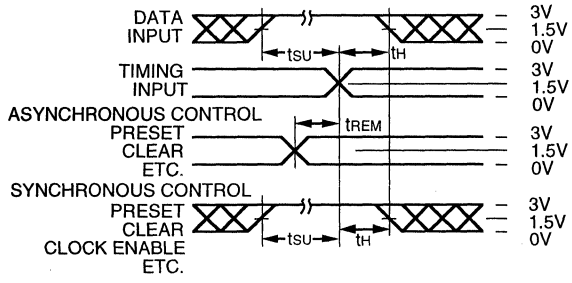
2776 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

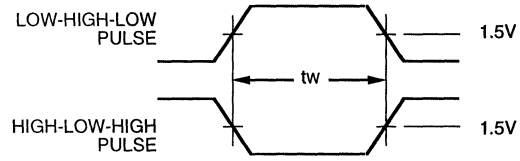
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



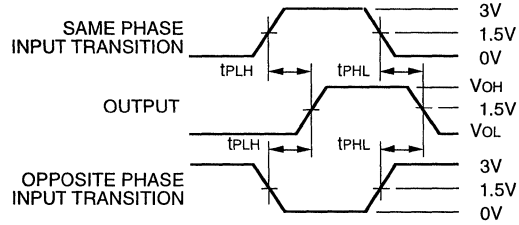
2776 drw 06

PULSE WIDTH



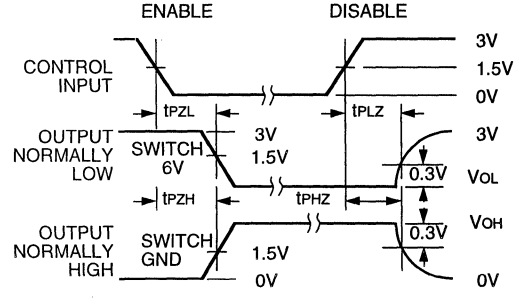
2776 drw 07

PROPAGATION DELAY



2776 drw 08

ENABLE AND DISABLE TIMES

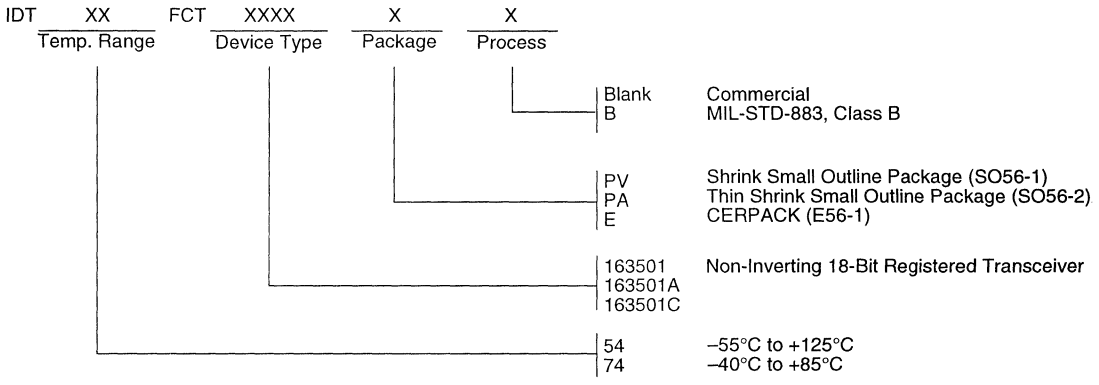


2776 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION



2776 drw 10

8

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT LATCHED TRANSCEIVER

IDT54/74FCT163543/A/C
ADVANCE INFORMATION

FEATURES:

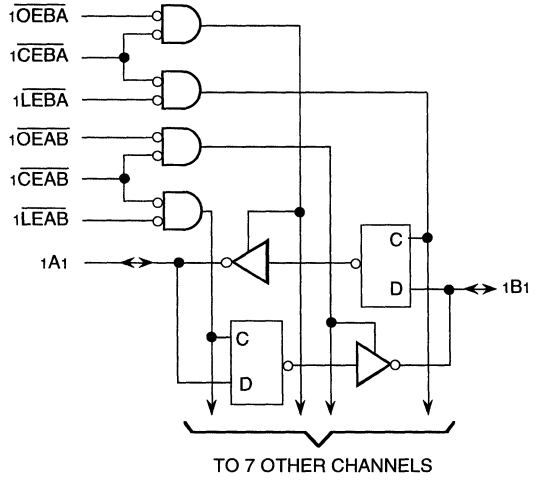
- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

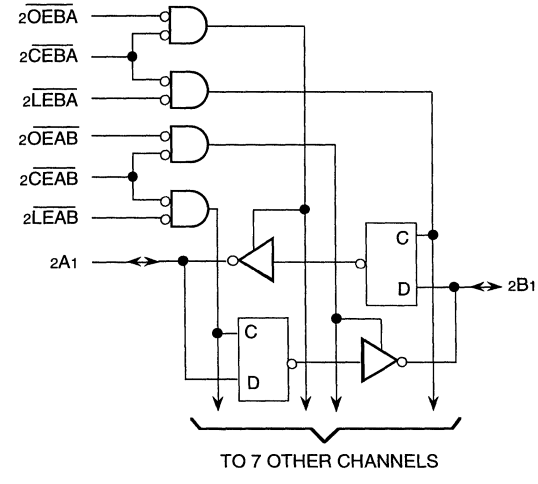
The FCT163543/A/C 16-bit latched transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type latched transceivers with separate input and output control to permit independent control of data flow in either direction. For example, the A-to-B Enable ($xCEAB$) must be LOW in order to enter data from the A port or to output data from the B port. $xLEAB$ controls the latch function. When $xLEAB$ is LOW, the latches are transparent. A subsequent LOW-to-HIGH transition of $xLEAB$ signal puts the A latches in the storage mode. $xOEAB$ performs output enable function on the B port. Data flow from the B port to the A port is similar but requires using $xCEBA$, $xLEBA$, and $xOEBA$ inputs. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163543/A/C have series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM

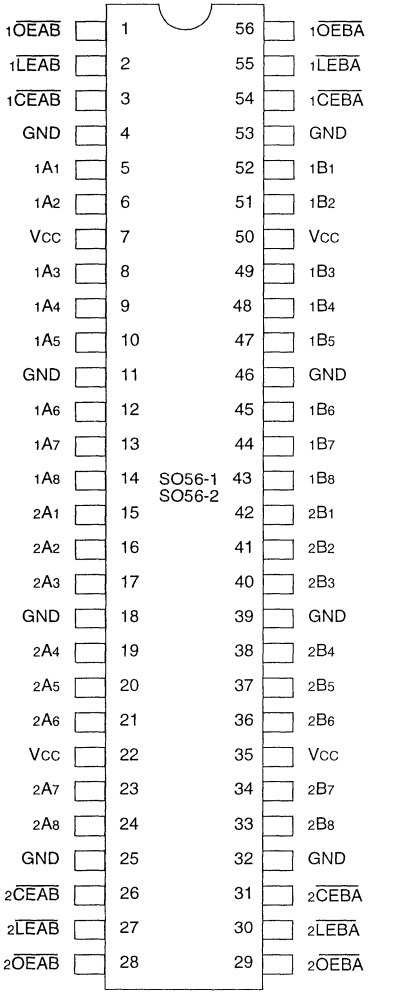


3250 drw 01



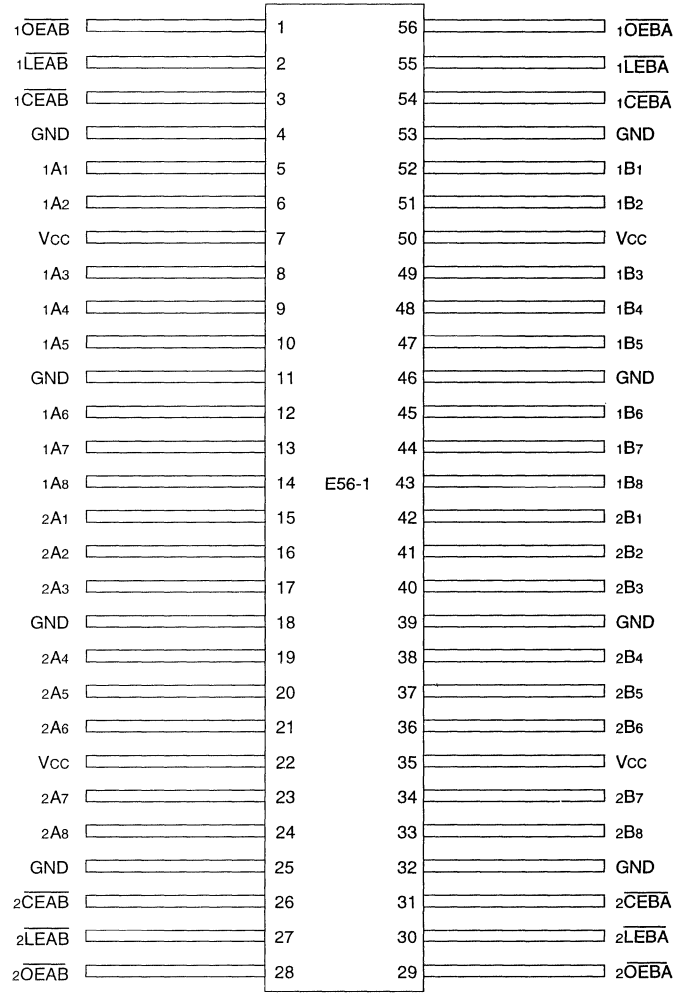
3250 drw 02

PIN CONFIGURATIONS



3250 drw 03

SSOP
TSSOP
TOP VIEW



3250 drw 04

CERPACK
TOP VIEW

8

PIN DESCRIPTION

Pin Names	Description
$xOEAB$	A-to-B Output Enable Input (Active LOW)
$xOEBA$	B-to-A Output Enable Input (Active LOW)
$xCEAB$	A-to-B Enable Input (Active LOW)
$xCEBA$	B-to-A Enable Input (Active LOW)
$xLEAB$	A-to-B Latch Enable Input (Active LOW)
$xLEBA$	B-to-A Latch Enable Input (Active LOW)
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

3250 tbl 01

FUNCTION TABLE[1, 3]

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$xCEAB$	$xLEAB$	$xOEAB$	xAx to xBx	xBx
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous[2] A Inputs

NOTES: 3250 tbl 02

1. A-to-B data flow shown; B-to-A flow control is the same, except using $xCEBA$, x $LEBA$ and $xOEBA$.
2. Before $xLEAB$ LOW-to-HIGH Transition
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 3250 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 3250 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

3250 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

8

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} –0.6V[3]		—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open x$\overline{CEAB}$ and x$\overline{OEAB}$ = GND x$\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$= GND x$\overline{CEBA}$ = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.0	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.6	1.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz 50% Duty Cycle x$\overline{LEAB}$, x$\overline{CEAB}$ and x$\overline{OEAB}$= GND x$\overline{CEBA}$ = V_{CC} Sixteen Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.0[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	2.4	4.3[5]	

3250 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

Symbol	Parameter	Condition[1]	FCT163543				FCT163543A				FCT163543C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Transparent Mode xAx to xBx or xBx to xAx	CL = 50pF RL = 500Ω	1.5	8.5	1.5	10.0	1.5	6.5	1.5	7.5	1.5	5.3	—	—	ns
tPLH tPHL	Propagation Delay $x\overline{LEBA}$ to xAx, $x\overline{LEAB}$ to xBx		1.5	12.5	1.5	14.0	1.5	8.0	1.5	9.0	1.5	7.0	—	—	ns
tPZH tPZL	Output Enable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	12.0	1.5	14.0	1.5	9.0	1.5	10.0	1.5	8.0	—	—	ns
tPHZ tPLZ	Output Disable Time $x\overline{OEBA}$ or $x\overline{OEAB}$ to xAx or xBx $x\overline{CEBA}$ or $x\overline{CEAB}$ to xAx or xBx		1.5	9.0	1.5	13.0	1.5	7.5	1.5	8.5	1.5	6.5	—	—	ns
tSU	Set-up Time HIGH or LOW xAx or xBx to $x\overline{LEAB}$ or $x\overline{LEBA}$		3.0	—	3.0	—	2.0	—	2.0	—	2.0	—	—	—	ns
tH	Hold Time HIGH or LOW xAx or xBx to $x\overline{LEAB}$ or $x\overline{LEBA}$		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	—	—	ns
tW	$x\overline{LEBA}$ or $x\overline{LEAB}$ Pulse Width LOW		5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	—	—	ns
tSK(o)	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

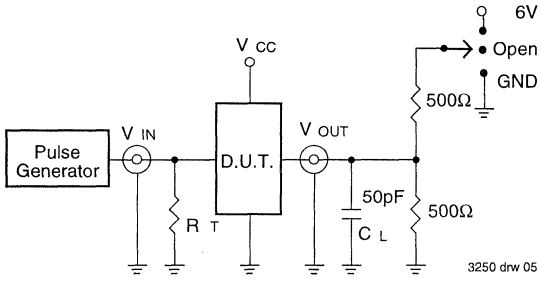
3250 tbl 07

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, Normal Range. For Vcc = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

8

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

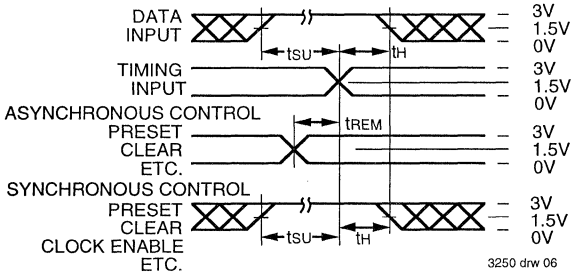
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS: 3250 lnk 08

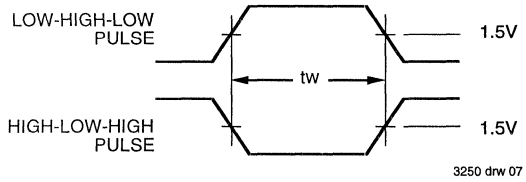
C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

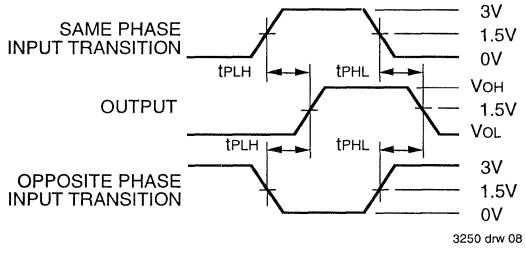
SET-UP, HOLD AND RELEASE TIMES



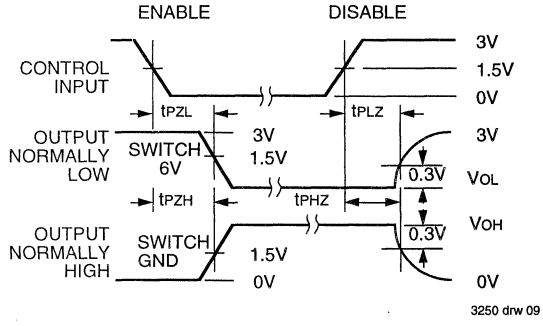
PULSE WIDTH



PROPAGATION DELAY



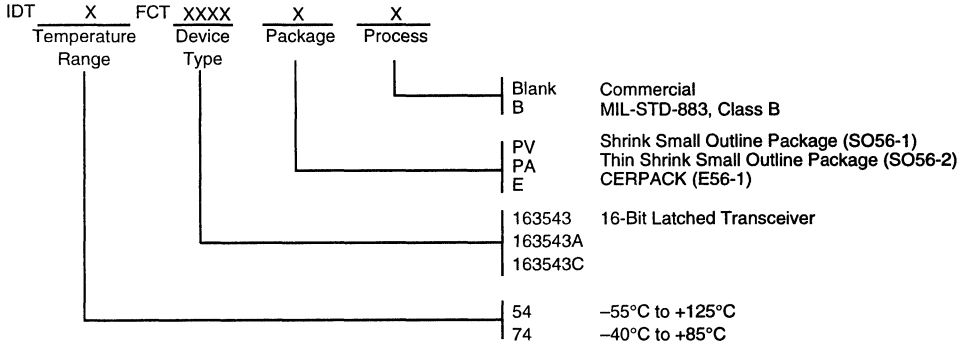
ENABLE AND DISABLE TIMES



NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION



3250 drw 10

8

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT BUS TRANSCEIVER/ REGISTERS

IDT54/74FCT163646/A/C

FEATURES:

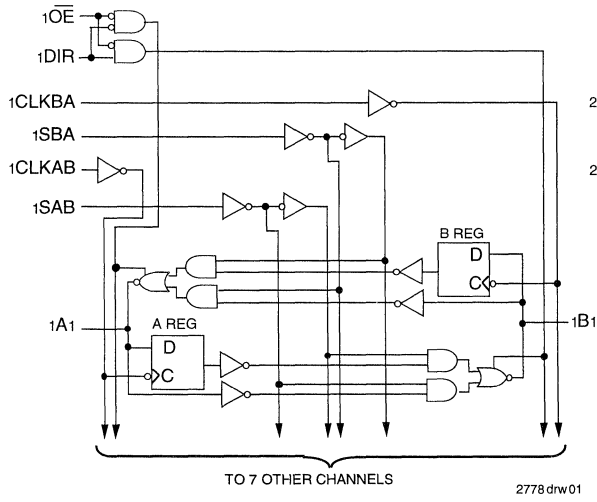
- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

DESCRIPTION:

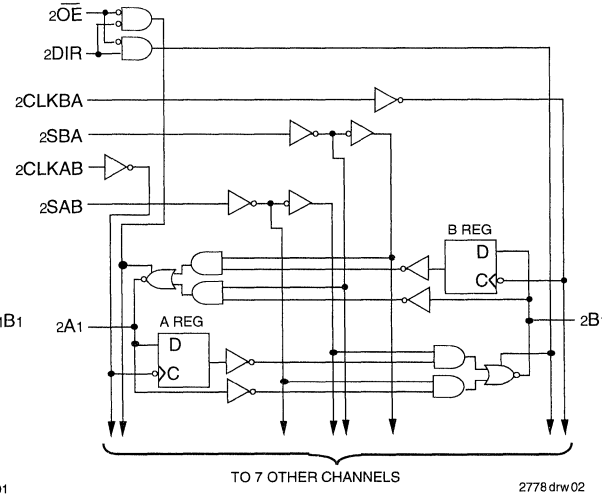
The FCT163646/A/C 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independant 8-bit bus transceivers with 3-state D-type registers. The control circuitry is organized for multiplexed transmission of data between A bus and B bus either directly or from the internal storage registers. Each 8-bit transceiver/register features direction control (xDIR), over-riding Output Enable control ($x\overline{OE}$) and Select lines (xSAB and xSBA) to select either real-time data or stored data. Separate clock inputs are provided for A and B port registers. Data on the A or B data bus, or both, can be stored in the internal registers by the LOW-to-HIGH transitions at the appropriate clock pins. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The FCT163646/A/C have series current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM

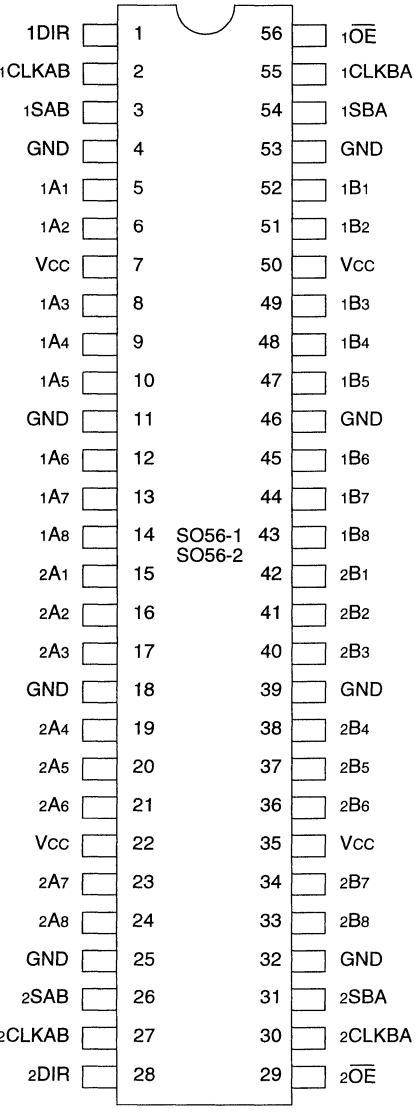


2778 drw 01



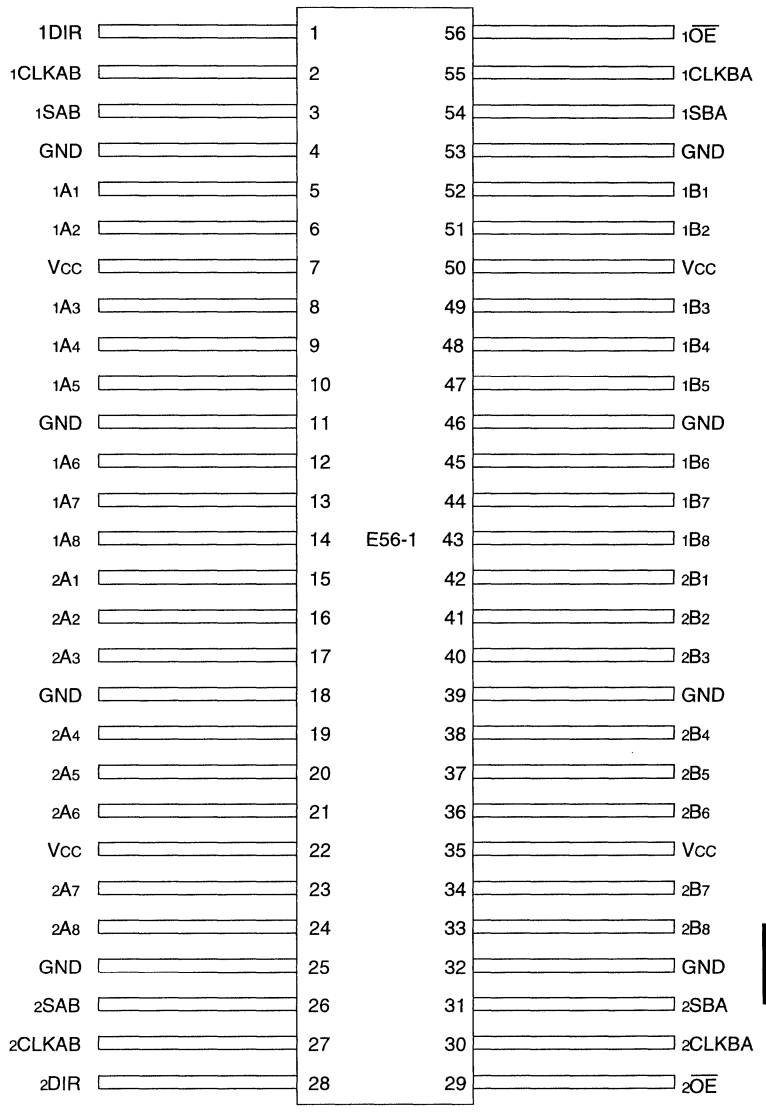
2778 drw 02

PIN CONFIGURATIONS



2778 drw 03

SSOP
TSSOP
TOP VIEW



2778 drw 04

CERPACK
TOP VIEW

8

PIN DESCRIPTION

Pin Names	Description
xAx	Data Register A Inputs Data Register B Outputs
xBx	Data Register B Inputs Data Register A Outputs
xCAB, xCBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xDIR, x$\overline{OE}$	Output Enable Inputs

2778 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE: 2778 lnk 04
1. This parameter is measured at characterization but not tested.

FUNCTION TABLE(2)

Inputs						Data I/O(1)		Operation or Function
x$\overline{OE}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	↑	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

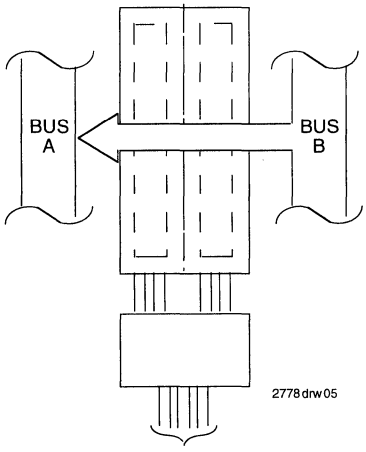
2778 tbl 02

NOTES:
1. The data output functions may be enabled or disabled by various signals at the x$\overline{OE}$ or xDIR inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ =LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS(1)

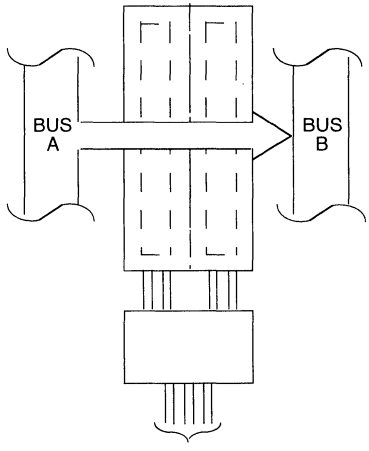
Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 2778 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Output and I/O terminals.



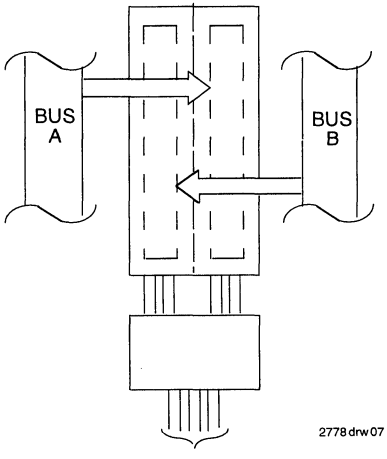
xDIR	$x\overline{OE}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

REAL-TIME TRANSFER BUS B TO A



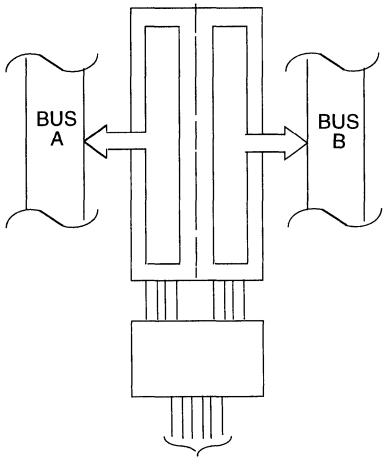
xDIR	$x\overline{OE}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

REAL-TIME TRANSFER BUS A TO B



xDIR	$x\overline{OE}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	↑	X	X	X
L	L	X	↑	X	X
X	H	↑	↑	X	X

STORAGE FROM A AND/OR B



xDIR (1)	$x\overline{OE}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

TRANSFER STORED DATA TO A AND/OR B

NOTE:
1. Cannot transfer data to A bus and B bus simultaneously.

8

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
I_{CCZ}			MIL.	—	0.1	100	

NOTES:

2778 lnk 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open xDIR = x$\overline{OE}$= GND 50% Duty Cycle One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = x$\overline{OE}$ = GND	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.0	mA
		f_i = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.6	1.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = x$\overline{OE}$ = GND	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.0[5]	
		f_i = 2.5MHz 50% Duty Cycle Sixteen Bits Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	3.0	5.3[5]	

2778 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

8

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

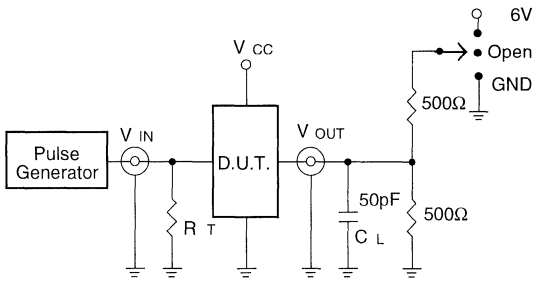
			FCT163646				FCT163646A				FCT163646C				
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	5.4	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR or $x\overline{OE}$ to Bus		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	1.5	7.8	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR or $x\overline{OE}$ to Bus		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	1.5	6.3	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	1.5	5.7	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	1.5	6.2	—	—	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	2.0	—	—	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	—	—	ns
t_W	Clock Pulse Width HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	—	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

2778 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2778 drw 09

SWITCH POSITION

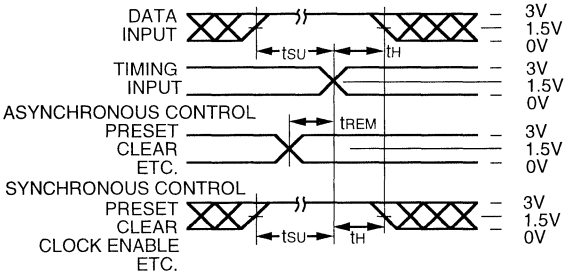
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

2778 lnk 08

DEFINITIONS:

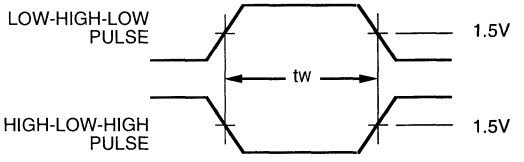
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



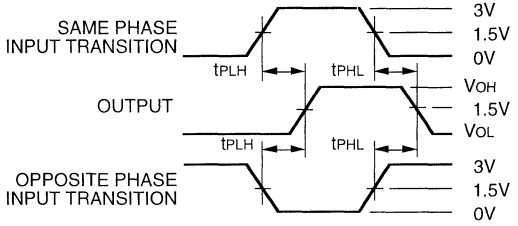
2778 drw 10

PULSE WIDTH



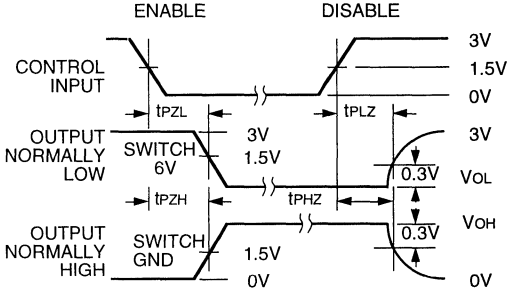
2778 drw 11

PROPAGATION DELAY



2778 drw 12

ENABLE AND DISABLE TIMES



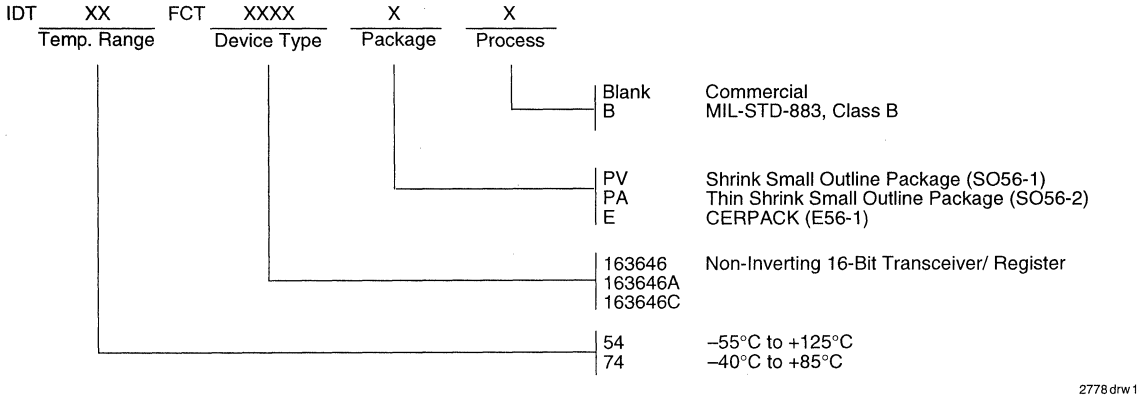
2778 drw 13

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

8

ORDERING INFORMATION



2778 drw 14

Integrated Device Technology, Inc.

3.3V CMOS 20-BIT BUFFERS

IDT54/74FCT163827A/B/C
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

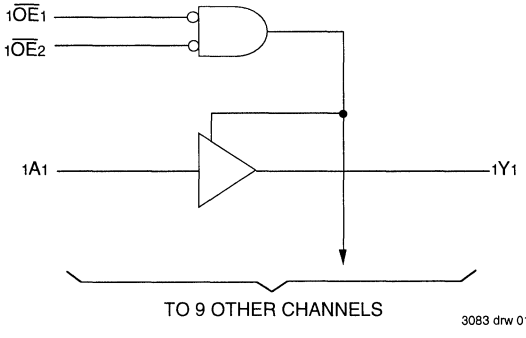
DESCRIPTION:

The FCT163827A/B/C 20-bit buffers are built using advanced dual metal CMOS technology. These 20-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or busses carrying parity. Two pairs of NAND-ed output enable controls offer maximum control flexibility and are organized to operate the device as two 10-bit buffers or one 20-bit buffer. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

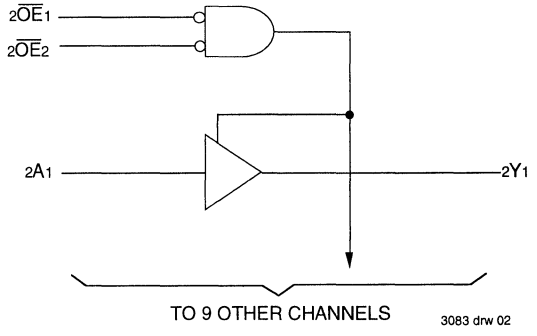
The FCT163827A/B/C have series current limiting resistors. This offers low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors.

The inputs of the FCT163827A/B/C can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

FUNCTIONAL BLOCK DIAGRAM



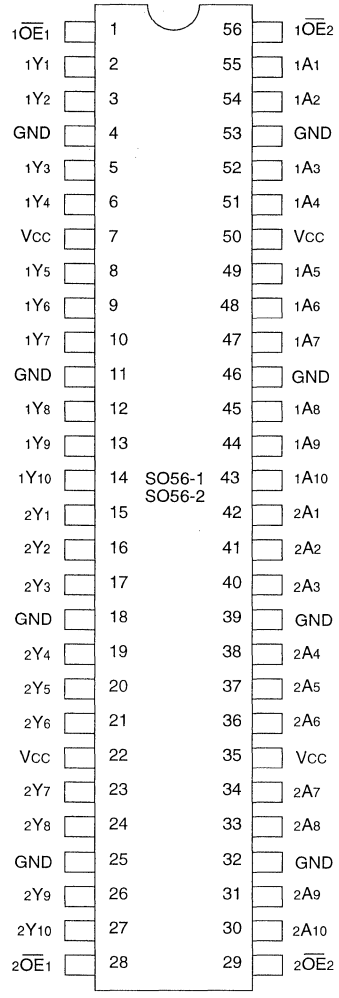
3083 drw 01



3083 drw 02

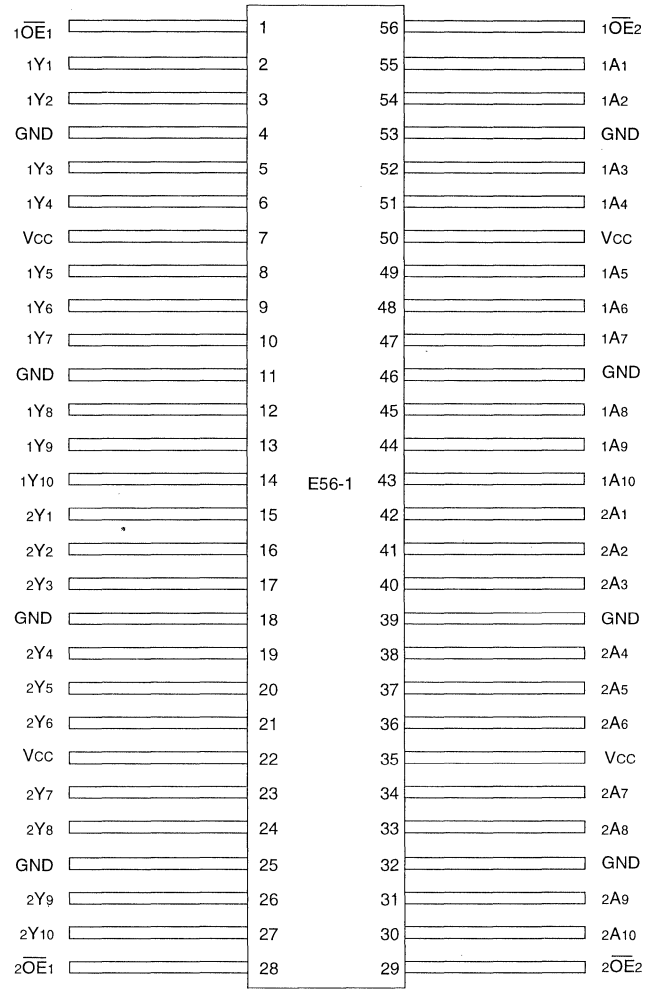
8

PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

3083 drw 03



CERPACK
TOP VIEW

3083 drw 04

PIN DESCRIPTION

Pin Names	Description
xOE_x	Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

3083 tbl 01

FUNCTION TABLE[1]

Inputs			Outputs
xOE_1	xOE_2	xAx	xYx
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE: 3083 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 3083 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8.0	pF

3083 lnk 04

NOTE:

1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

3083 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} –0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	50	75	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.5	0.7	mA
		50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND One Bit Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.5	0.8	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	2.5	3.7[5]	
		50% Duty Cycle $x\overline{OE}_1$ = $x\overline{OE}_2$ = GND Twenty Bits Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	2.5	4.1[5]	

3083 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

8

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[4]

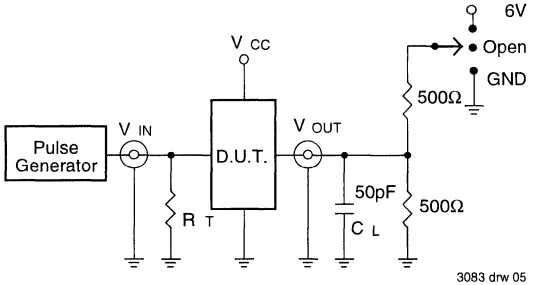
Symbol	Parameter	Conditions[1]	FCT163827A				FCT163827B				FCT163827C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	1.5	4.4	—	—	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	1.5	10.0	—	—	
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$x to xYx	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	1.5	7.0	—	—	ns
		C_L = 300pF[4] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	1.5	14.0	—	—	
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$x to xYx	C_L = 5pF[4] R_L = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	1.5	5.7	—	—	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	1.5	6.0	—	—	
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

3083 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3083 drw 05

SWITCH POSITION

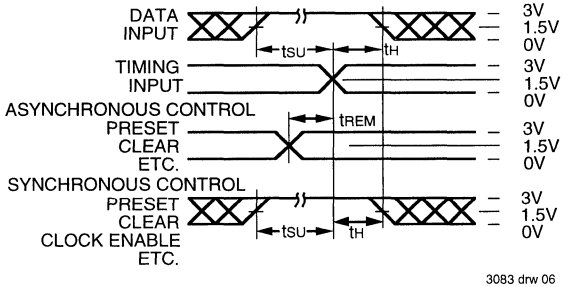
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

3083 lnk 08

DEFINITIONS:

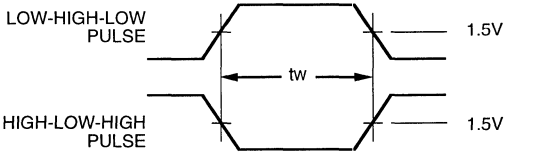
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



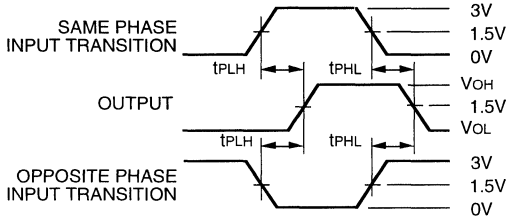
3083 drw 06

PULSE WIDTH



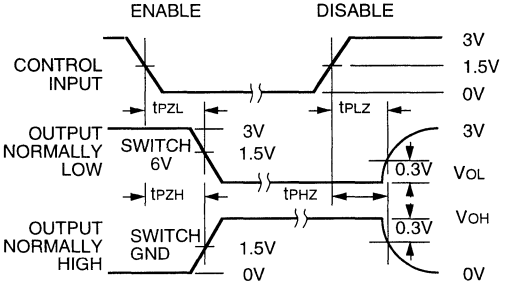
3083 drw 07

PROPAGATION DELAY



3083 drw 08

ENABLE AND DISABLE TIMES



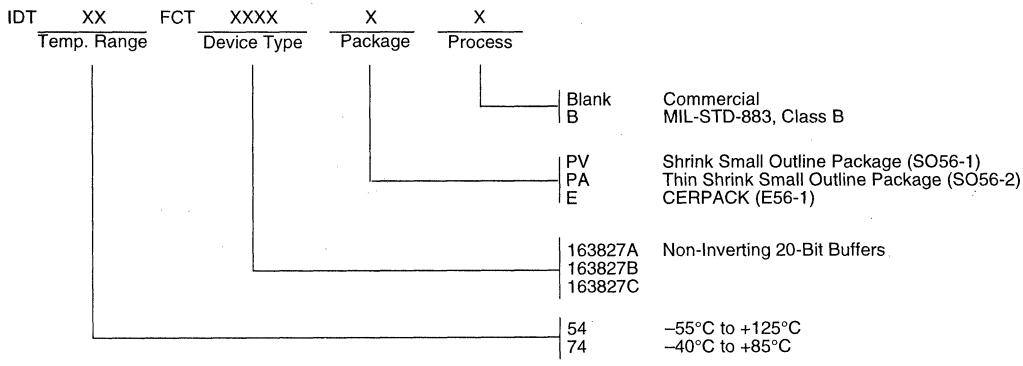
3083 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

8

ORDERING INFORMATION



3083 drw 10

Integrated Device Technology, Inc.

3.3V CMOS 16-BIT REGISTERED TRANSCEIVER

IDT54/74FCT163952A/B/C
ADVANCE INFORMATION

FEATURES:

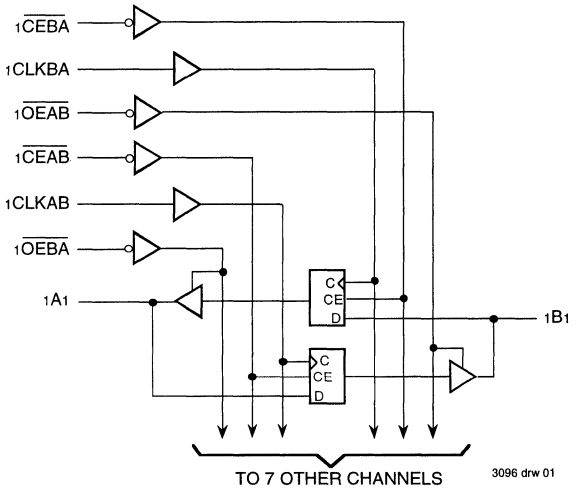
- 0.5 MICRON CMOS Technology
- **Typical $t_{SK(o)}$ (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and 19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7 to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V components

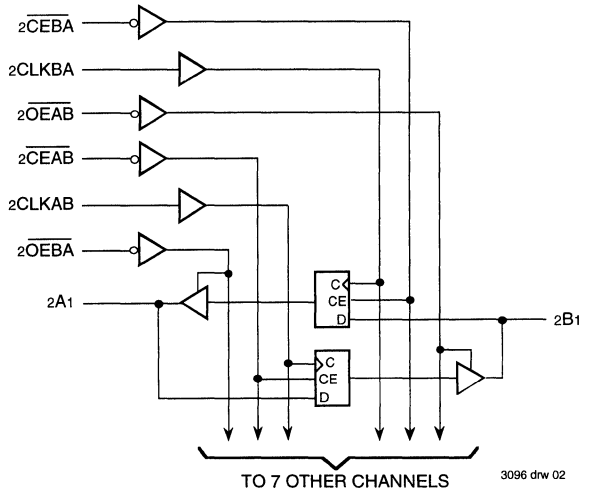
DESCRIPTION:

The FCT163952A/B/C 16-bit registered transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power devices are organized as two independent 8-bit D-type registered transceivers with separate input and output control for independent control of data flow in either direction. For example, the A-to-B Enable ($x\overline{CEAB}$) must be LOW to enter data from the A port. xCLKAB controls the clocking function. When xCLKAB toggles from LOW-to-HIGH, the data present on the A port will be clocked into the register. $x\overline{OEAB}$ performs the output enable function on the B port. Data flow from the B port to A port is similar but requires using $x\overline{CEBA}$, xCLKBA, and $x\overline{OEBA}$ inputs. Full 16-bit operation is achieved by tying the control pins of the independent transceivers together.

The FCT163952A/B/C have series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times–reducing the need for external series terminating resistors.

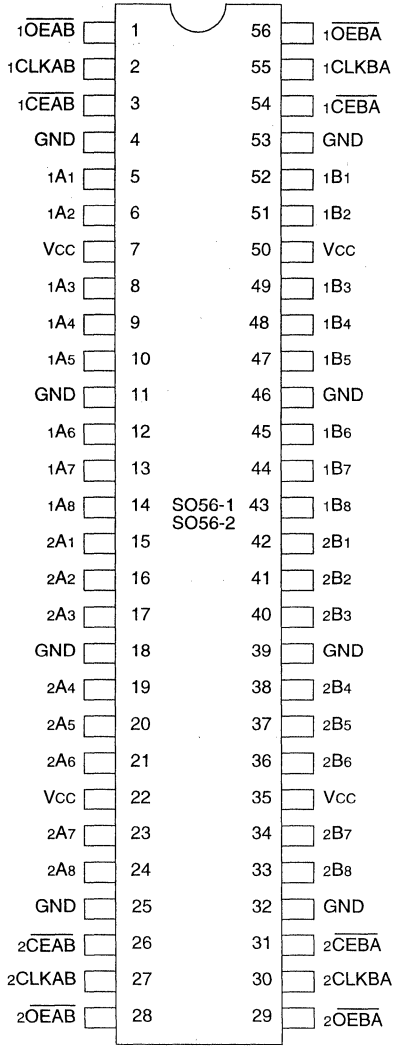
FUNCTIONAL BLOCK DIAGRAM





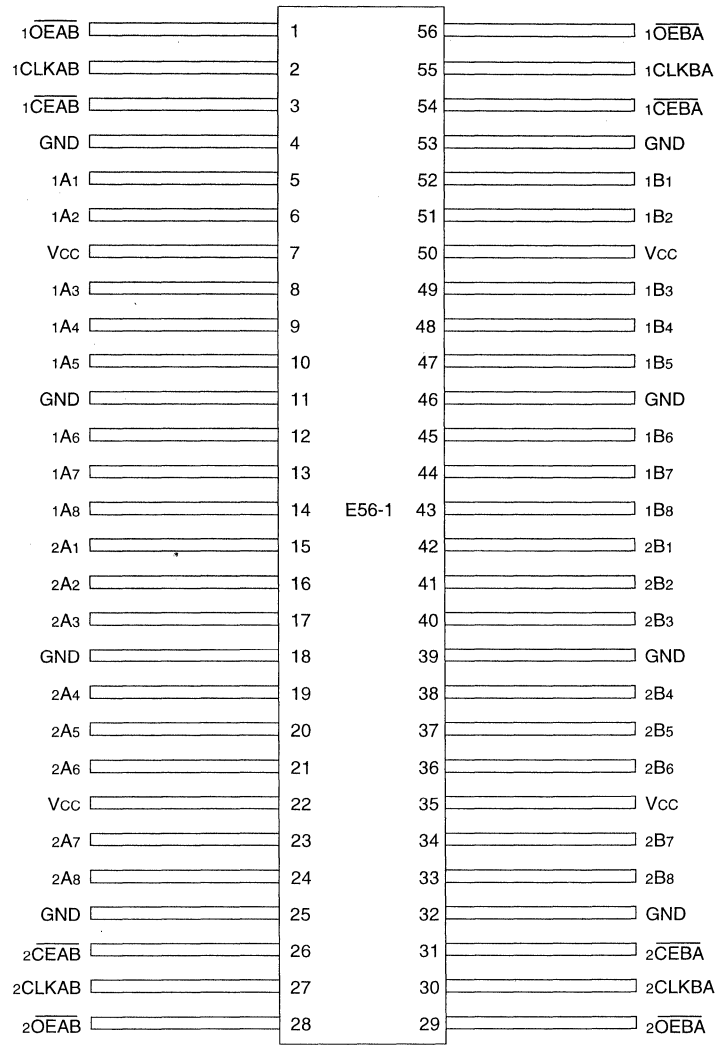
8

PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

3096 drw 03



CERPACK
TOP VIEW

3096 drw 04

PIN DESCRIPTION

Pin Names	Description
$xOEAB$	A-to-B Output Enable Input (Active LOW)
$xOEBA$	B-to-A Output Enable Input (Active LOW)
$xCEAB$	A-to-B Clock Enable Input (Active LOW)
$xCEBA$	B-to-A Clock Enable Input (Active LOW)
xCLKAB	A-to-B Clock Input
xCLKBA	B-to-A Clock Input
xAx	A-to-B Data Inputs or B-to-A 3-State Outputs
xBx	B-to-A Data Inputs or A-to-B 3-State Outputs

3096 tbl 01

FUNCTION TABLE[1,3]

Inputs				Outputs
$xCEAB$	xCLKAB	$xOEAB$	xAx	xBx
H	X	L	X	B[2]
X	L	L	X	B[2]
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

NOTES: 3096 tbl 02

1. A-to-B data flow is shown: B-to-A data flow is similar but uses, $xCEBA$, xCLKBA, and $xOEBA$.
2. Level of B before the indicated steady-state input conditions were established.
3. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High-impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

3096 lnk 03

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

3096 lnk 04

NOTE:

1. This parameter is measured at characterization but not tested.

8

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
I_{CCZ}			MIL.	—	0.1	100	

3096 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply	V_{CC} = Max.	V_{IN} = V_{CC} –0.6V[3]	—	2.0	100	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $x\overline{OEAB}$ or $x\overline{OEBA}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.1	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.6	1.1	
		V_{CC} = Max., Outputs Open f_{CP}= 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{OEBA}$ = V_{CC} Sixteen Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	5.0[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	3.0	5.9[5]	

3096 tbl 07

NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

8

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[5]

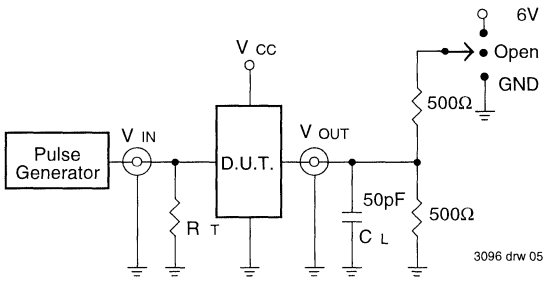
Symbol	Parameter	Condition[1]	FCT163952A				FCT163952B				FCT163952C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLKAB, xCLKBA to xBx, xAx	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	2.0	6.3	2.0	7.3	ns
t_{PZH} t_{PZL}	Output Enable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	1.5	7.0	1.5	8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xAx, xBx		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	1.5	6.5	1.5	7.5	ns
t_{SU}	Set-up Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA		2.0	—	2.0	—	1.5	—	2.0	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW $x\overline{CEAB}$, $x\overline{CEBA}$ to xCLKAB, xCLKBA		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
t_W	Pulse Width HIGH or LOW xCLKAB or xCLKBA[4]		3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
$t_{SK(o)}$	Output Skew[3]		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

3096 tbl 08

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
4. This parameter is guaranteed but not tested.
5. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

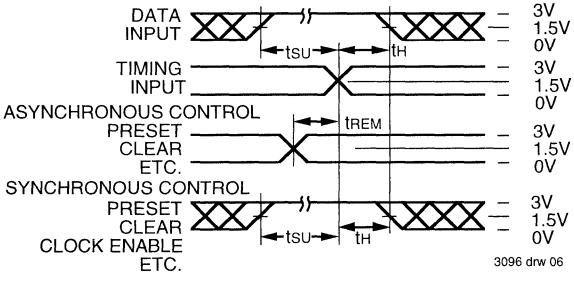
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

3096 lnk 09

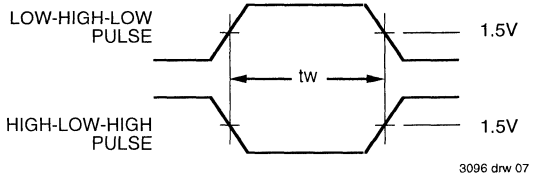
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

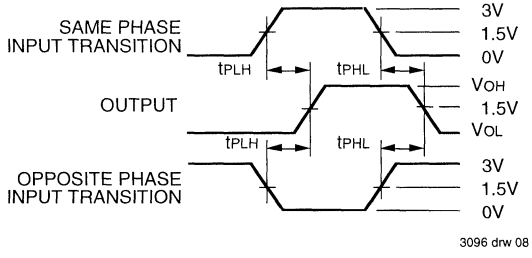
SET-UP, HOLD AND RELEASE TIMES



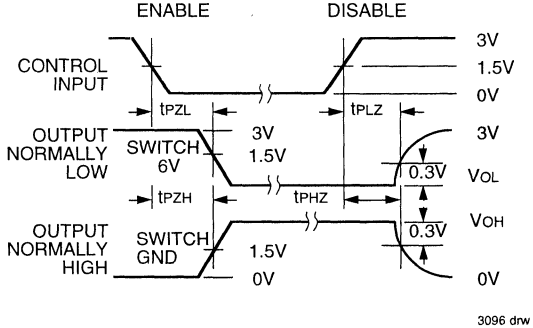
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

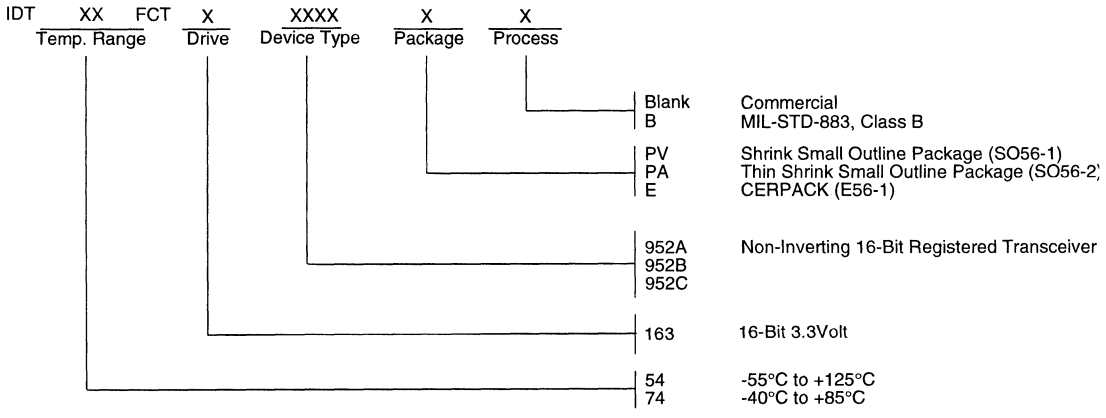


NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

8

ORDERING INFORMATION



3096 drw 10

Integrated Device Technology, Inc.

3.3V CMOS OCTAL BUFFER/LINE DRIVER

IDT54/74FCT3244/A

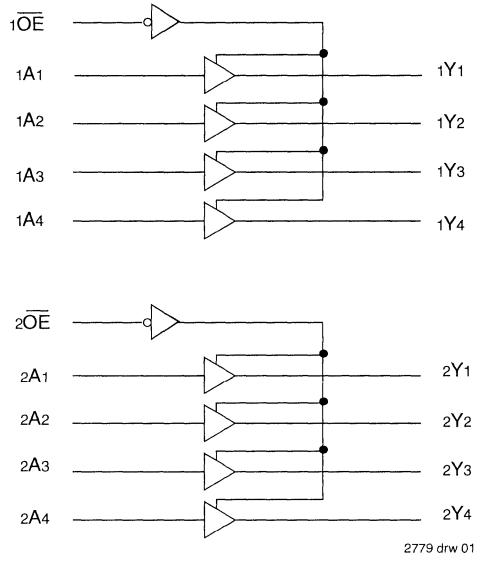
FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

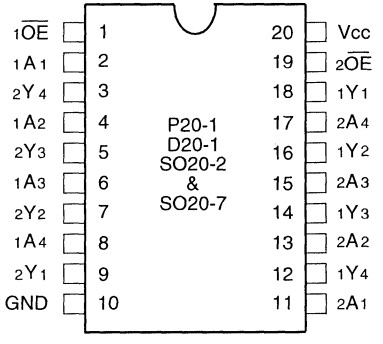
The FCT3244/A octal buffer/line drivers are built using advanced dual metal CMOS technology. These high-speed, low-power buffers are designed to be used as memory data and address drivers, clock drivers, and bus-oriented transmitter/receivers. The three-state controls are designed to operate these devices in a dual-nibble or single-byte mode. All inputs are designed with hysteresis for improved noise margin.

FUNCTIONAL BLOCK DIAGRAM



2779 drw 01

PIN CONFIGURATIONS



DIP/SOIC/SSOP TOP VIEW

2779 drw 02

8

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	3–State Output Enable Inputs (Active LOW)
xAx	Data Inputs
xYx	3-State Outputs

2779 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$x\overline{OE}$	xAx	xYx
L	L	L
L	H	H
H	X	Z

2779 tbl 02

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

2779 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	4.0	8.0	pF

NOTE:
1. This parameter is measured at characterization but not tested.

2779 lnk 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

2779 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limits for this parameter is ± 5µA at T_A = –55°C.

8

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open 50% Duty Cycle $x\overline{OE}$ = GND One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	60	85	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	0.9	mA
		50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.6	0.9	
		V_{CC} = Max. Outputs Open fi = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	1.2	1.7[5]	
		50% Duty Cycle $x\overline{OE}$ = GND Eight Bits Toggling	V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	1.2	1.8[5]	

NOTES:

2779 tbl 06

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3]

			FCT3244				FCT3244A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay xAx to xYx	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.0	1.5	4.8	1.5	5.1	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	8.0	1.5	8.5	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.0	1.5	7.5	1.5	5.6	1.5	5.9	ns

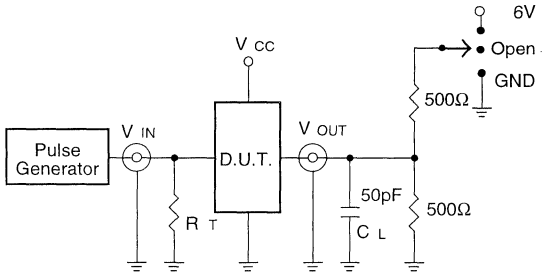
NOTES:

2779 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2779 drw 03

SWITCH POSITION

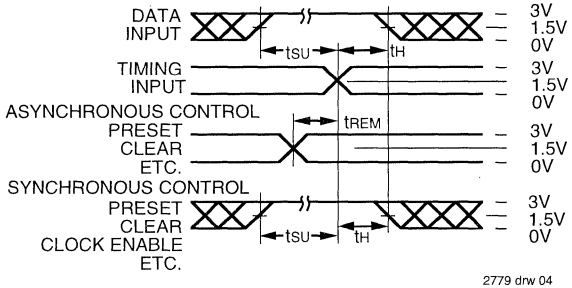
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

2779 lnk 08

DEFINITIONS:

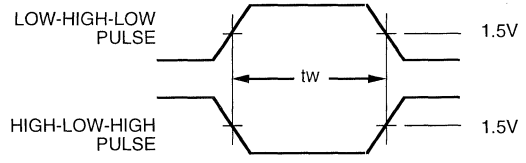
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



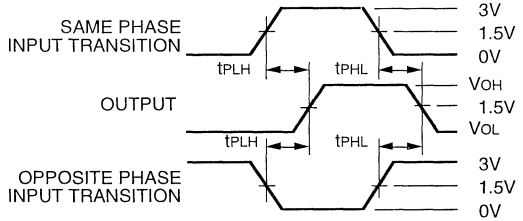
2779 drw 04

PULSE WIDTH



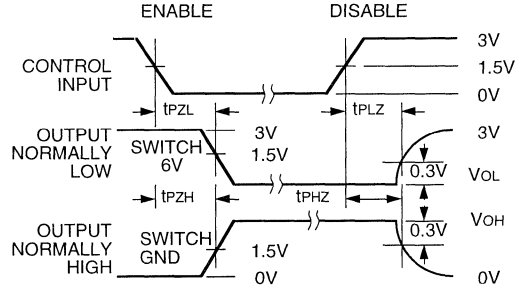
2779 drw 05

PROPAGATION DELAY



2779 drw 06

ENABLE AND DISABLE TIMES



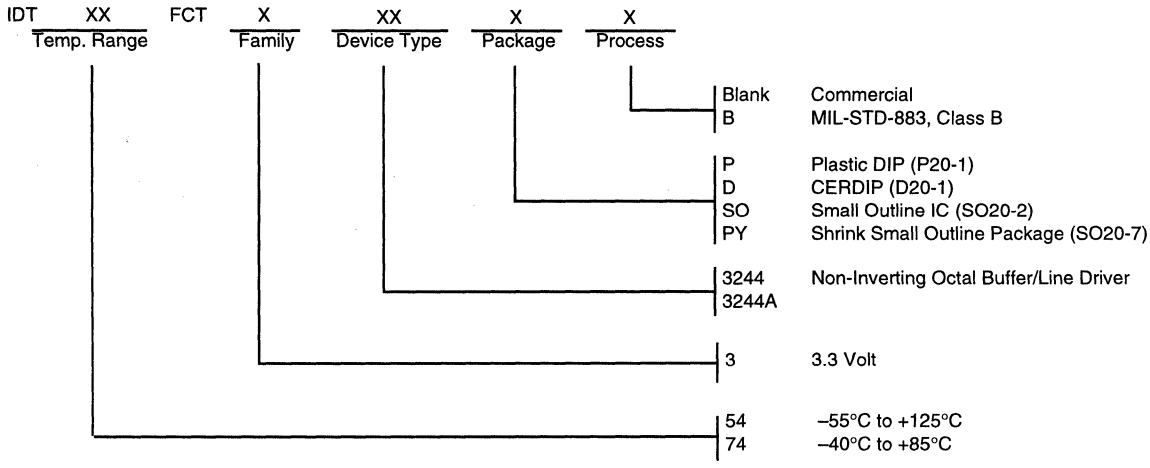
2779 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

8

ORDERING INFORMATION



2779 drw 08

Integrated Device Technology, Inc.

3.3V CMOS OCTAL BIDIRECTIONAL TRANSCEIVERS

IDT54/74FCT3245/A

FEATURES:

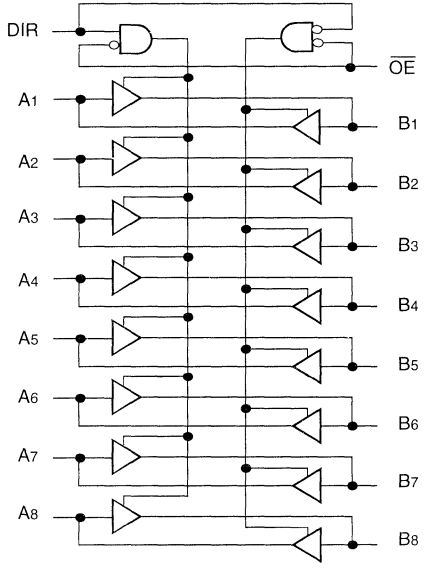
- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP Packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The FCT3245/A octal transceivers are built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two busses (A and B). The direction control pin (DIR) controls the direction of data flow. The output enable pin ($\overline{OE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

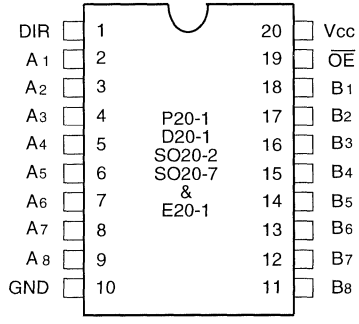
The FCT3245/A have series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM

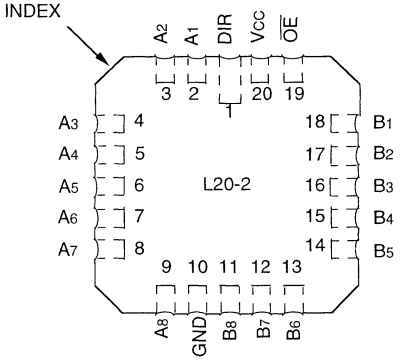


2650 drw 01

PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK TOP VIEW



2650 drw 02

LCC TOP VIEW

2650 drw 03

8

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
DIR	Direction Control Input
Ax	Side A Inputs or 3-State Outputs
Bx	Side B Inputs or 3-State Outputs

2650 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs
$\overline{OE}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

2650 tbl 02

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

2650 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	4.0	8.0	pF

2650 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	Vcc+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

2650 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limits for this parameter is ± 5µA at T_A = –55°C.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = DIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	85	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $\overline{OE}$ = DIR = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	0.9	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.6	0.9	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}$ = DIR = GND Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.2	1.7[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	1.2	1.8[5]	

NOTES:

2650 tbl 06

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3]

			FCT3245				FCT3245A				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	7.5	1.5	4.6	1.5	4.9	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A or B		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A or B		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to A or B[4]		1.5	9.5	1.5	10.0	1.5	6.2	1.5	6.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A or B[4]		1.5	7.5	1.5	10.0	1.5	5.0	1.5	6.0	ns

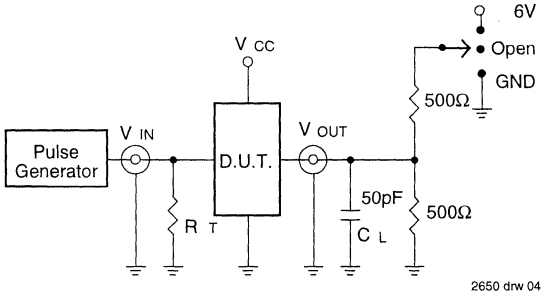
NOTES:

2650 tbl 07

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
4. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2650 drw 04

SWITCH POSITION

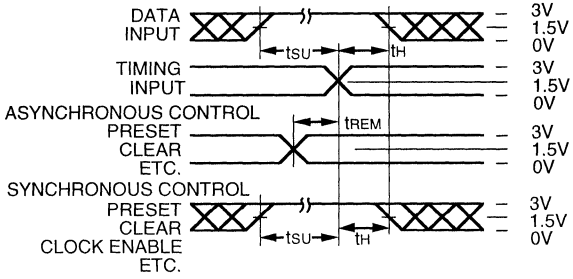
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

2650 lnk 08

DEFINITIONS:

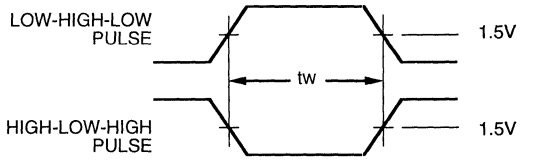
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



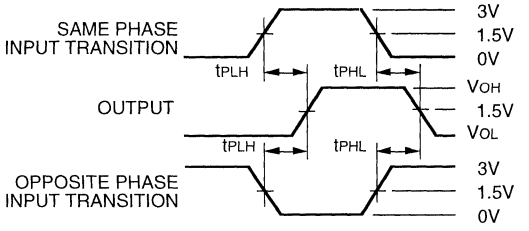
2650 drw 05

PULSE WIDTH



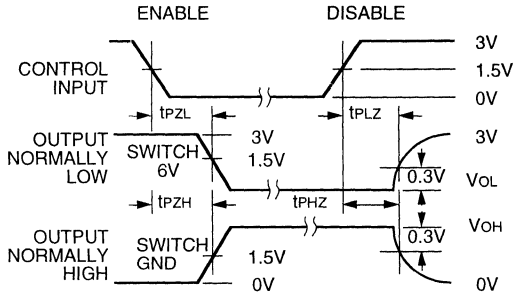
2650 drw 06

PROPAGATION DELAY



2650 drw 07

ENABLE AND DISABLE TIMES



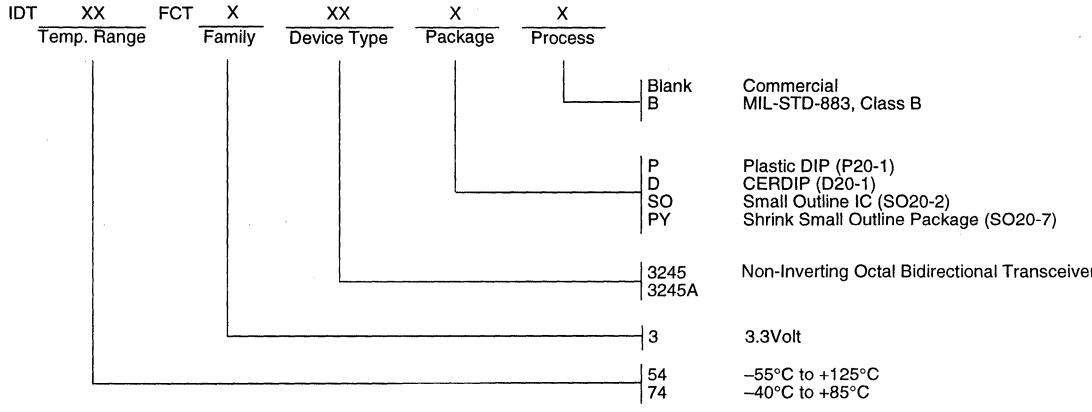
2650 drw 08

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

8

ORDERING INFORMATION



2650 drw 09

Integrated Device Technology, Inc.

3.3V CMOS OCTAL TRANSPARENT LATCHES

IDT54/74FCT3573/A
ADVANCE INFORMATION

FEATURES:

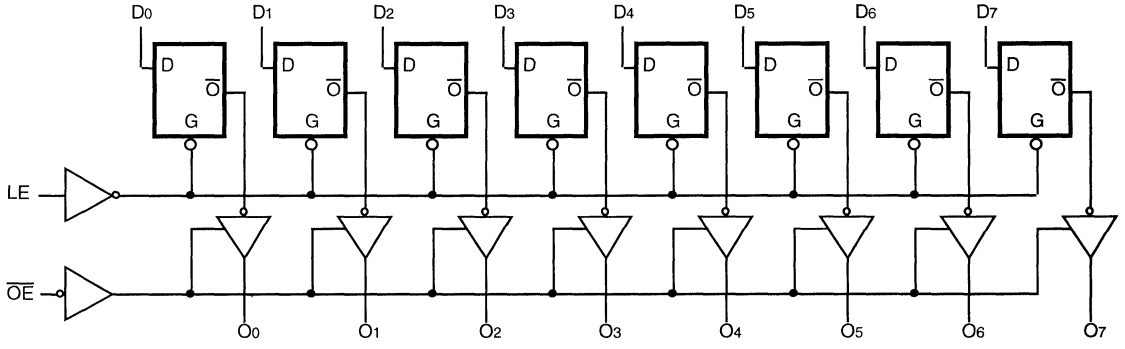
- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP Packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The FCT3573/A are octal transparent latches built using an advanced dual metal CMOS technology.

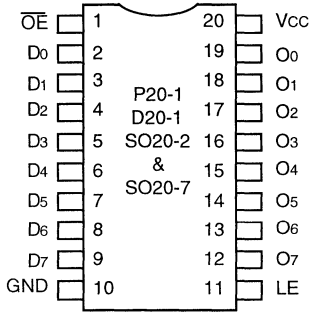
These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high-impedance state.

FUNCTIONAL BLOCK DIAGRAM



3093 drw 01

PIN CONFIGURATION



DIP/SOIC/SSOP
TOP VIEW

3093 drw 02

FUNCTION TABLE (1)

Inputs			Outputs
D_N	LE	$\overline{OE}$	O_N
H	H	L	H
L	H	L	L
X	X	H	Z

3093 tbl 02

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
D_N	Data Inputs
LE	Latch Enable Input (Active HIGH)
$\overline{OE}$	Output Enable Input (Active LOW)
O_N	3-State Outputs
$\overline{O}_N$	Complementary 3-State Outputs

3093 tbl 03

8

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 3093 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	4.0	8.0	pF

NOTE: 3093 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
I_{CCZ}			MIL.	—	0.1	100	

3093 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limits for this parameter is ± 5µA at T_A = –55°C.

8

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]				µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND				µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi =10MHz 50% Duty Cycle $\overline{OE}$ = GND LE = VCC One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = V_{CC} –0.6V V_{IN} = GND				mA
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE}$ = GND LE = V_{CC} Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = V_{CC} –0.6V V_{IN} = GND				

3093 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3]

Symbol	Parameter	Conditions[1]	FCT3573				FCT3573A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_N to O_N	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	8.5	1.5	5.2	1.5	5.6	ns
t_{PLH} t_{PHL}	Propagation Delay LE to O_N		2.0	13.0	2.0	15.0	2.0	8.5	2.0	9.8	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.0	1.5	13.5	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	7.5	1.5	10.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to LE		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to LE		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	LE Pulse Width HIGH		6.0	—	6.0	—	5.0	—	6.0	—	ns

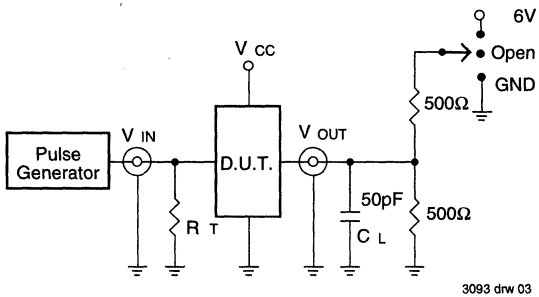
3093 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

8

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3093 drw 03

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

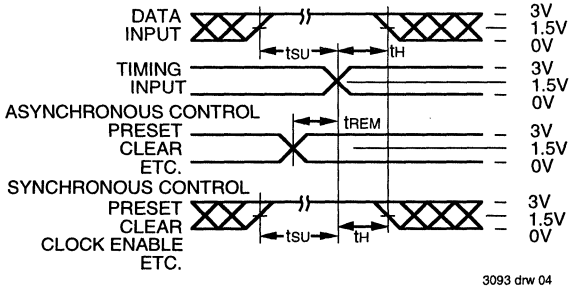
3093 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

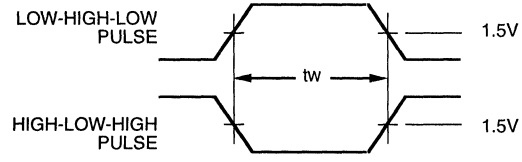
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



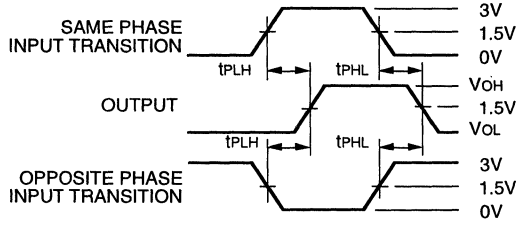
3093 drw 04

PULSE WIDTH



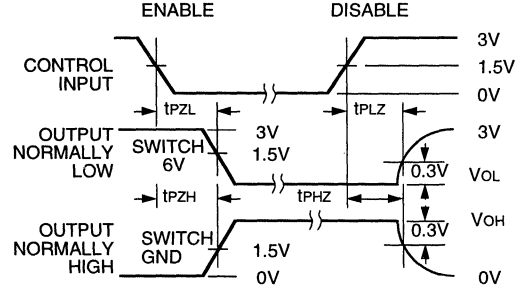
3093 drw 05

PROPAGATION DELAY



3093 drw 06

ENABLE AND DISABLE TIMES

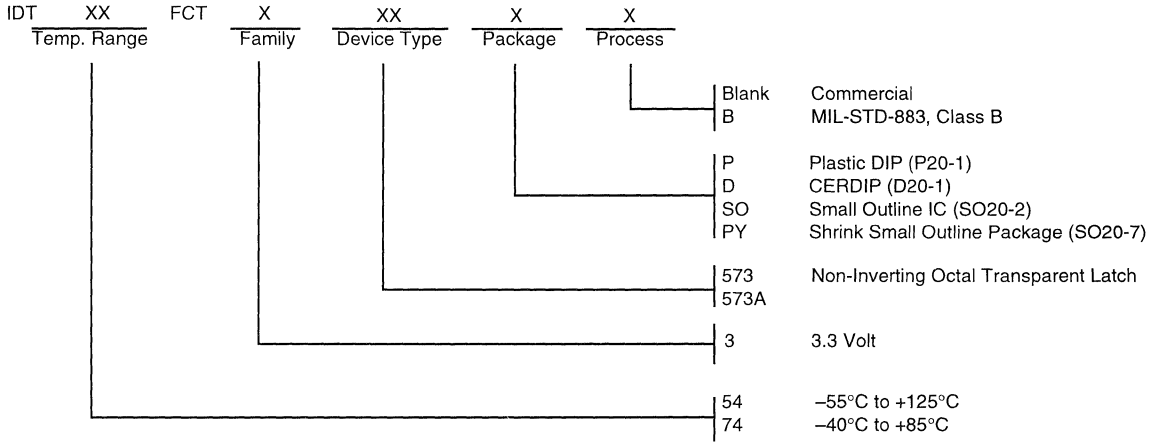


3093 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION



3093 drw 08

8

Integrated Device Technology, Inc.

3.3V CMOS OCTAL D REGISTERS (3-STATE)

IDT54/74FCT3574/A
ADVANCE INFORMATION

FEATURES:

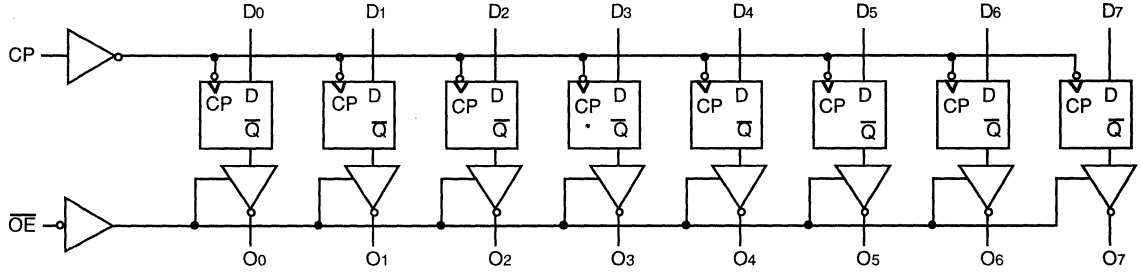
- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP Packages
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The FCT3574/A are 8-bit registers built using an advanced dual metal CMOS technology. These registers consist of eight D-type flip-flops with a buffered common clock and buffered 3-state output control. When the output ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the high-impedance state.

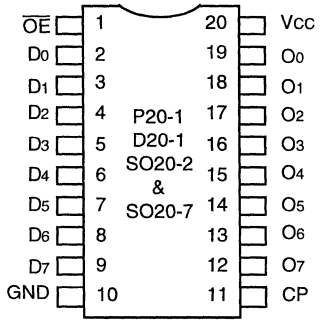
Input data meeting the set-up and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

FUNCTIONAL BLOCK DIAGRAM



3095 drw 01

PIN CONFIGURATION



DIP/SOIC/SSOP TOP VIEW

3095 drw 02

PIN DESCRIPTION

Pin Names	Description
D_N	D flip-flop data inputs
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition.
O_N	3-state outputs, (true)
$\overline{O}_N$	3-state outputs, (inverted)
$\overline{OE}$	Active LOW 3-state Output Enable input

3095 tbl 0

FUNCTION TABLE [1]

Function	Inputs			Outputs	Internal
	$\overline{OE}$	CP	Dn	On	$\overline{Q}n$
HI-Z	H	L	X	Z	NC
	H	H	X	Z	NC
LOAD REGISTER	L	↑	L	L	H
	L	↑	H	H	L
	H	↑	L	Z	H
	H	↑	H	Z	L

NOTE: 3095 tbl 02

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH transition

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	4.0	8.0	pF

NOTE: 3095 tbl 04

1. This parameter is measured at characterization but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 3095 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

8

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

3095 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limits for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} −0.6V[3]				mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}$ = GND 50% Duty Cycle One Input Toggling	V_{IN} = V_{CC} V_{IN} = GND				µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND				mA
		$\overline{OE}$ = GND fi = 5MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} −0.6V V_{IN} = GND				
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND				
		$\overline{OE}$ = GND fi = 2.5MHz 50% Duty Cycle Eight Bits Toggling	V_{IN} = V_{CC} −0.6V V_{IN} = GND				

3095 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

8

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3]

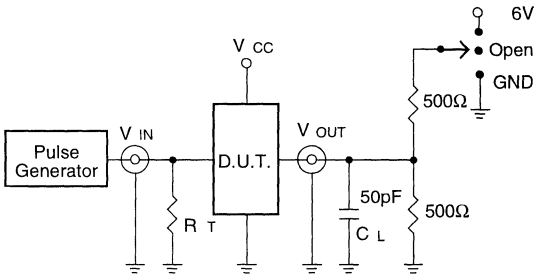
Symbol	Parameter	Conditions[1]	FCT3574				FCT3574A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CP to O_N[3]	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	ns
t_{SU}	Set-up Time HIGH or LOW, D_N to CP		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, D_N to CP		1.5	—	1.5	—	1.5	—	1.5	—	ns
t_W	CP Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	ns

3095 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3095 drw 03

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

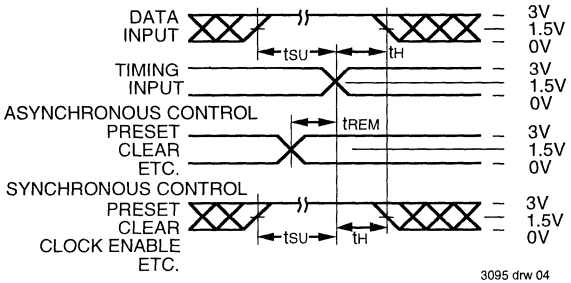
3095 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

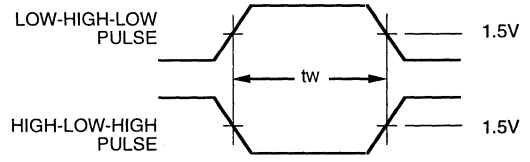
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



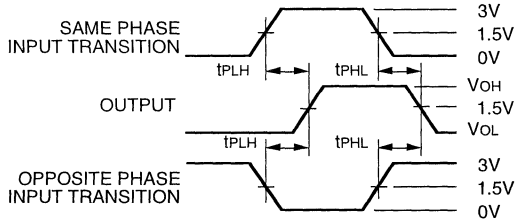
3095 drw 04

PULSE WIDTH



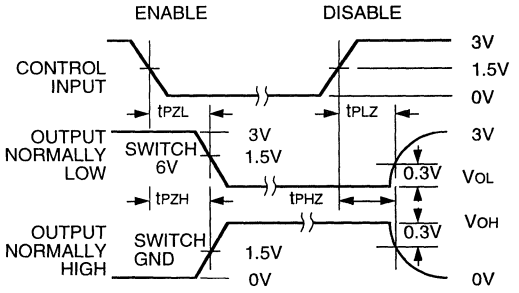
3095 srw 05

PROPAGATION DELAY



3095 drw 06

ENABLE AND DISABLE TIMES



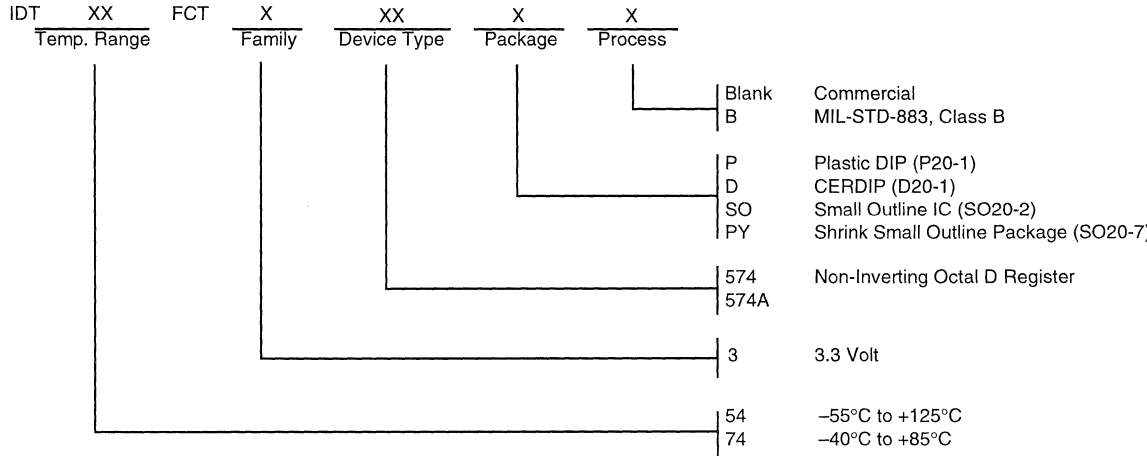
3095 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

8

ORDERING INFORMATION



3095 drw 08

Integrated Device Technology, Inc.

3.3V CMOS 10-BIT BUFFERS

IDT54/74FCT3827A/B

FEATURES:

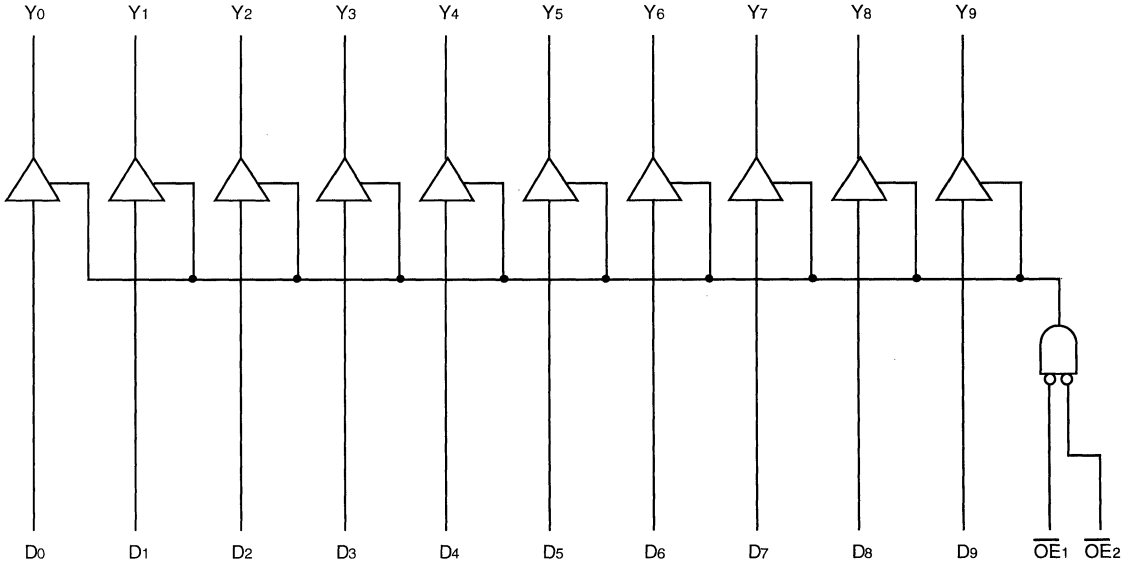
- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP Packages
- Extended commercial range of -40°C to +85°C
- V_{CC} = 3.3V ±0.3V, Normal Range or V_{CC} = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The FCT3827A/B 10-bit bus drivers are built using an advanced dual metal CMOS technology. These high speed, low power buffers are ideal for high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility.

All of the FCT3827 high performance interface components are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs.

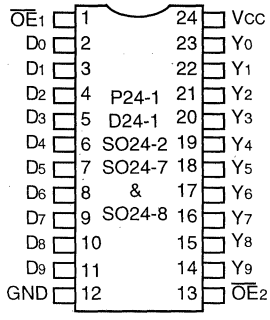
FUNCTIONAL BLOCK DIAGRAM



3092 drw 01

8

PIN CONFIGURATIONS



3092 drw 02

DIP/SOIC/SSOP/QSOP
TOP VIEW

PIN DESCRIPTION

Names	I/O	Description
$\overline{OE}_I$	I	When both are LOW the outputs are enabled. When either one or both are HIGH the outputs are High Z.
D_I	I	10-bit data input.
Y_I	O	10-bit data output.

3092 tbl 01

FUNCTION TABLE[1]

Inputs			Output	
$\overline{OE}_1$	$\overline{OE}_2$	D_I	Y_I	Function
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

NOTE:
1. H = HIGH Voltage Level
   X = Don't Care
   L = LOW Voltage Level
   Z = High Impedance

3092 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

3092 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	4.0	8.0	pF

NOTE:
1. This parameter is measured at characterization but not tested.

3092 lnk 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

3092 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limits for this parameter is ± 5µA at T_A = –55°C.

8

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} –0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	85	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	0.9	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.6	0.9	
		V_{CC} = Max. Outputs Open fi = 2.5MHz 50% Duty Cycle $\overline{OE_1}$ = $\overline{OE_2}$ = GND Ten Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	2.1[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	1.5	2.3[5]	

3092 tbl 06

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3]

Symbol	Parameter	Condition[1]	FCT3827A				FCT3827B				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_I to Y_I	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	9.0	1.5	5.0	1.5	6.5	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	15.0	1.5	17.0	1.5	13.0	1.5	14.0	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_I$ to Y_I	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	13.0	1.5	8.0	1.5	9.0	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	23.0	1.5	25.0	1.5	15.0	1.5	16.0	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_I$ to Y_I	C_L = 5pF[3] R_L = 500Ω	1.5	9.0	1.5	9.0	1.5	6.0	1.5	7.0	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	1.5	7.0	1.5	8.0	

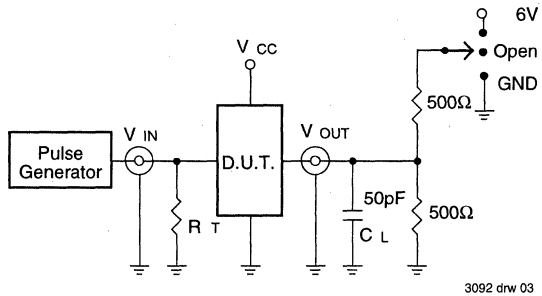
3092 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

8

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3092 drw 03

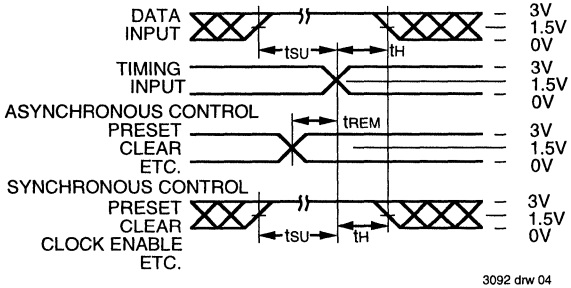
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS: 3092 lnk 08

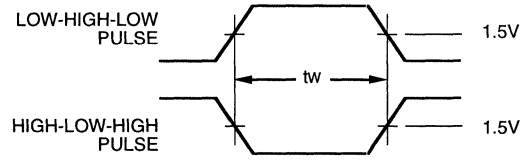
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



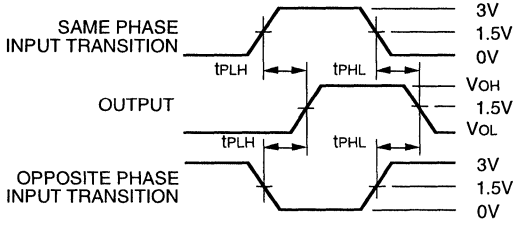
3092 drw 04

PULSE WIDTH



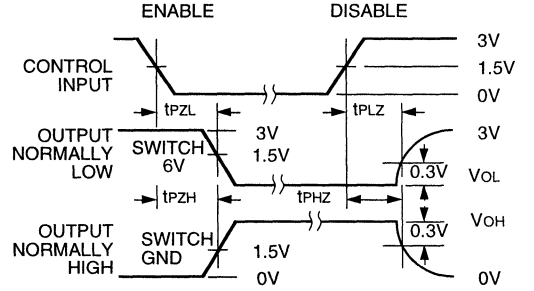
3092 drw 05

PROPAGATION DELAY



3092 drw 06

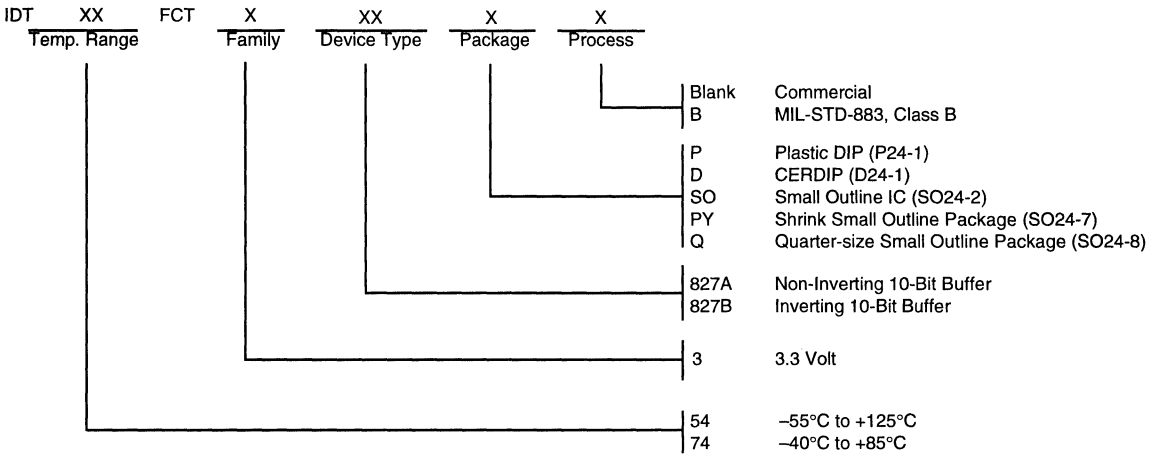
ENABLE AND DISABLE TIMES



3092 drw 07

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

ORDERING INFORMATION



3092 drw 08

8

Integrated Device Technology, Inc.

FAST CMOS 16-BIT BIDIRECTIONAL 3.3V TO 5V TRANSLATOR

IDT54/74FCT164245T

FEATURES:

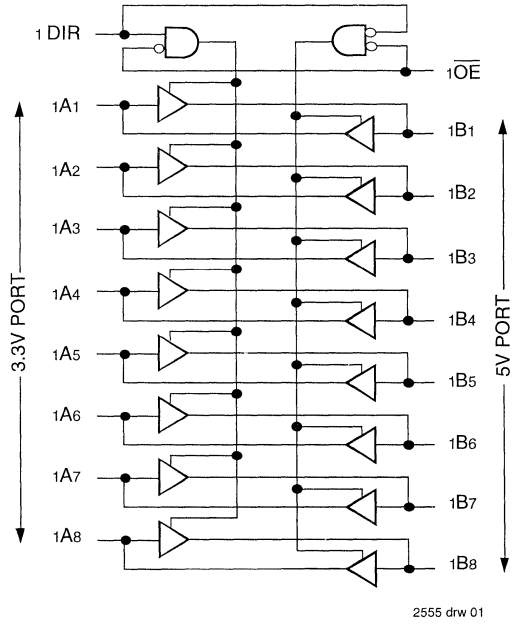
- 0.5 MICRON CMOS Technology
- Bidirectional interface between 3.3V and 5V busses
- Control inputs can be driven from either 3.3V or 5V circuits
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- 25 MIL Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- V_{CC1} = 5V ±10%, V_{CC2} = 2.7V to 3.6V
- High drive outputs (-32mA I_{OH}, 64mA I_{OL}) on 5V port
- Power-off disable on both ports permits "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 0.9V at V_{CC1} = 5V, V_{CC2} = 3.3V, T_A = 25°C

DESCRIPTION:

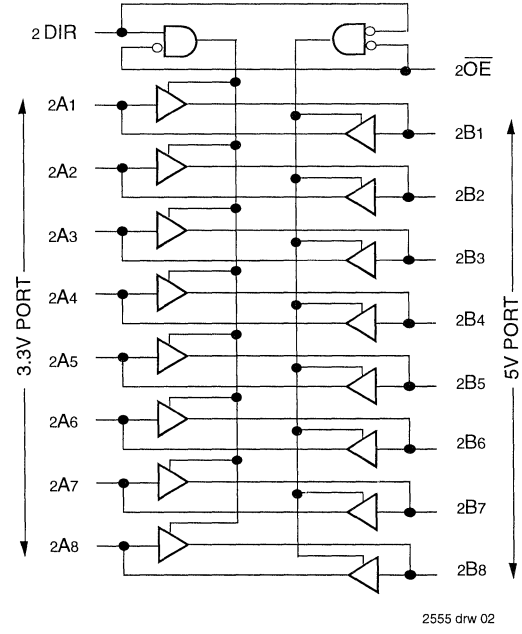
The FCT164245T 16-bit 3.3V-to-5V translator is built using advanced dual metal CMOS technology. This high-speed, low-power transceiver is designed to interface between a 3.3V bus and a 5V bus in a mixed 3.3V/5V supply environment. This enables system designers to interface TTL compatible 3.3V components with 5V components. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The A-port interfaces with the 3.3V bus; the B port interfaces with the 5V bus. The direction control (xDIR) pin controls the direction of data flow. The output enable ($x\overline{OE}$) overrides the direction control and disables both ports. These control signals can be driven from either 3.3V or 5V devices.

The FCT164245T is ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "hot insertion" of boards when used as backplane drivers. They also allow interface between a mixed supply system and external 5V peripherals.

FUNCTIONAL BLOCK DIAGRAM

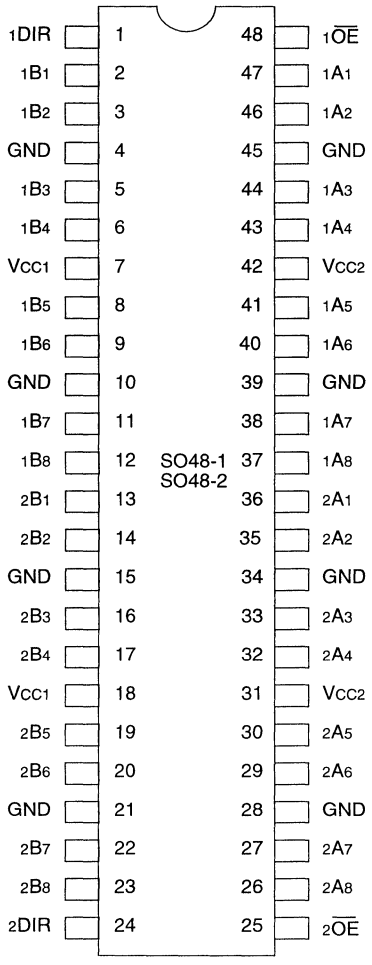


2555 drw 01



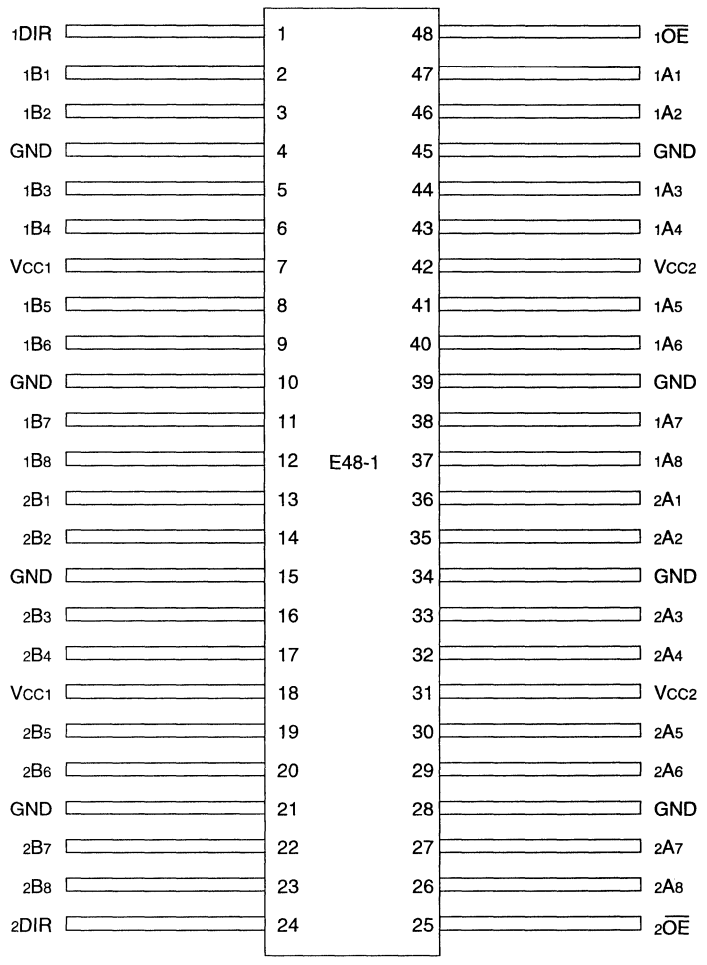
2555 drw 02

PIN CONFIGURATIONS



2555 drw 03

SSOP
TSSOP
TOP VIEW



2555 drw 04

CERPACK
TOP VIEW

POWER SUPPLY SEQUENCING

In the IDT54/74FCT164245T the condition of $V_{CC1} \geq (V_{CC2} - 0.5V)$ must be maintained at all times. For the range of $V_{CC1} = (V_{CC2} - 0.5V)$ to $V_{CC1} = (V_{CC2} + 0.9V)$, both the A and B ports will remain in a high impedance state.

8

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)

2555 tbl 01

FUNCTION TABLE(1)

Inputs		
$x\overline{OE}$	xDIR	Outputs
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

2555 tbl 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC1} +0.5	–0.5 to V_{CC1} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:

2555 lnk 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except V_{CC2}.
3. Power supply terminals V_{CC2}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

NOTE:

2555 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (A PORT - 3.3V)

Following Conditions Apply Unless Otherwise Specified:
V_{CC1} = 5V ± 10%, V_{CC2} = 2.7V to 3.3V; Commercial: T_A = –40°C to +85°C, Military: T_A = –55°C to +125°C,

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC1} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)	V_{CC2} = Max.	V_I = V_{CC2}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
V_{IK}	Clamp Diode Voltage	V_{CC2} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC1} = V_{CC2} = Min.	I_{OH} = –0.1mA	V_{CC2}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA MIL.	2.4	3.0	—	
		V_{CC2} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC1} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{CC2} = Min.	I_{OL} = 16mA	—	0.2	0.4	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OFF}	Input/Output Power Off Leakage	V_{CC1} = 0V, V_{CC2} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA
I_{OS}	Short Circuit Current[4]	V_{CC1} = Max., V_{CC2} = Max., V_O = GND[3]		–70	–105	–150	mA
I_O	Output Drive Current	V_{CC1} = Max., V_{CC2} = Max., V_O = 1.5V[3]		–40	–60	–90	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CC2L} I_{CC2H} I_{CC2Z}	Quiescent Power Supply Current	V_{CC1} = Max., V_{IN} = GND or V_{CC2} V_{CC2} = Max.		—	0.35	2.0	mA

2555 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.

8

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (B PORT - 5V)

Following Conditions Apply Unless Otherwise Specified:
V_{CC1} = 5V ± 10%, V_{CC2} = 2.7V to 3.3V; Commercial: T_A = –40°C to +85°C, Military: T_A = –55°C to +125°C,

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC1} = Max.	V_I = V_{CC1}	—	—	±5	µA
	Input HIGH Current (I/O pins)	V_{CC2} = Max.		—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
V_{IK}	Clamp Diode Voltage	V_{CC1} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC1} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{CC2} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[5]	2.0	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC1} = Min., V_{CC2} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC1} = 0V, V_{CC2} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA
I_{OS}	Short Circuit Current[4]	V_{CC1} = Max., V_{CC2} = Max., V_O = GND[3]		–80	–140	–225	mA
I_O	Output Drive Current	V_{CC1} = Max., V_{CC2} = Max., V_O = 2.5V[3]		–50	–75	–180	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CC1L} I_{CC1H} I_{CC1Z}	Quiescent Power Supply Current	V_{CC1} = Max., V_{IN} = GND or V_{CC2} V_{CC2} = Max.		—	0.08	1.5	mA

2555 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5 Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC1} = Max., V_{CC2} = Max., V_{IN} = V_{CC2} -0.6V[3]		—	12	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC1} = Max., V_{CC2} = Max. Outputs Open $x\overline{OE}$ = xDIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC2} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC1} = Max., V_{CC2} = Max. Outputs Open fi = 10MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = V_{CC2} - 0.6V V_{IN} = GND	—	1.2	4.7	mA
		V_{CC1} = Max., V_{CC2} = Max Outputs Open fi = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND Sixteen Bits Toggling	V_{IN} = V_{CC2} - 0.6V V_{IN} = GND	—	3.5	8.5[5]	

2555 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1}= 5.0V, V_{CC2}= 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC1+} I_{CC2} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC1}= Quiescent Current (I_{CC1L}, I_{CC1H} and I_{CC1Z})
   I_{CC2}= Quiescent Current (I_{CC2L}, I_{CC2H} and I_{CC2Z})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

8

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

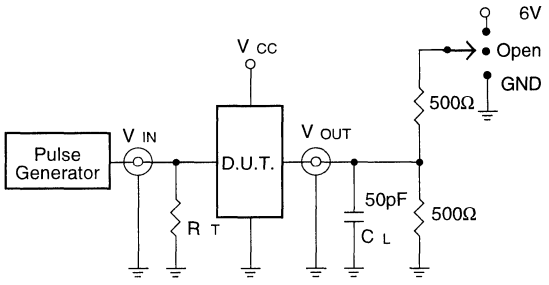
Symbol	Parameter	Condition[1]	Com'l.		Mil.		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B	C_L = 50pF R_L = 500Ω	1.5	5.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay B to A		1.5	5.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to B		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to B		1.5	6.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to A		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to A		1.5	6.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to B[3]		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to B[3]		1.5	6.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to A[3]		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to A[3]		1.5	6.0	—	—	ns

2555 tbl 08

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2555 drw 05

SWITCH POSITION

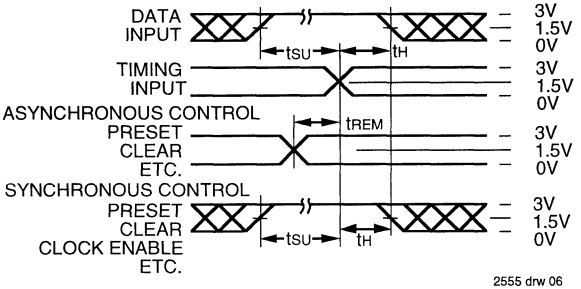
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

2555 lnk 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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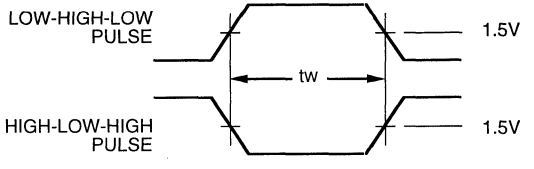
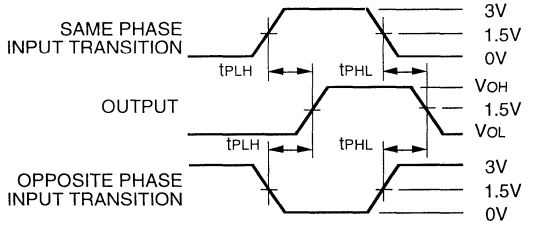
PULSE WIDTH



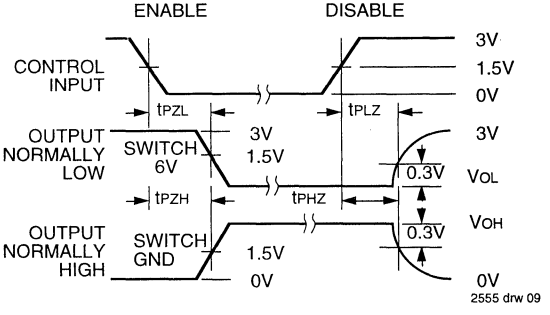
2555 drw 08

PROPAGATION DELAY



2555 drw 07

ENABLE AND DISABLE TIMES



2555 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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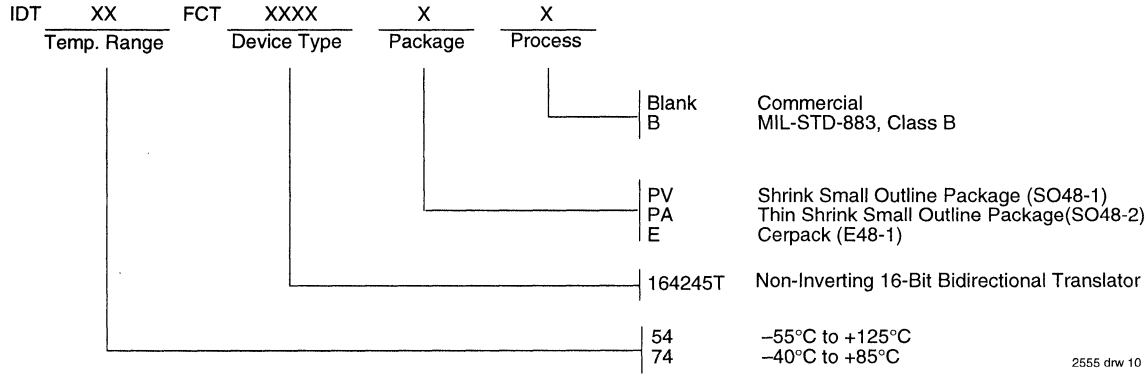
ORDERING INFORMATION



FCT CLOCK MANAGEMENT PRODUCTS

IDT's FCT clock management products are intended for use in high-speed clock distribution applications. These components are designed with tightly controlled output skew, finely tuned output edge rates, and various fanout configurations. Available products include buffers for use in general clock distribution, and PLL clock generators for applications that require zero clock delay or frequency multiplication/division. All components are based upon IDT's advanced FCT CMOS technology, giving superior performance with the lowest power dissipation in the industry. Components are available in both 5-Volt and 3.3-Volt versions, allowing a simple upgrade from 5V designs to 3.3V future applications.

Skew specifications in IDT's clock management products include pin-to-pin skew, pulse skew, and part-to-part skew. Pin-to-pin skew specifications are used in designs to assure accurate clocking of multiple register banks without violating setup, hold, and other timing parameters. Pin-to-pin skew specifications also assure timing margins with very high-speed clocks. Pulse skew specifications assure minimal waveform distortion in high-speed clocks, guaranteeing the signal quality will not degrade when passed through a clock distribution circuit. Pulse skew specifications also guarantee that if a rising clock and falling clock are being used simultaneously, the signal timing will remain tightly controlled. Part to part skew specifications guarantee that if multiple components are used in various locations in a design, the timing signal distribution will remain tightly controlled.

The configuration of IDT's clock buffers and PLLs provide for optimum system design. The multiple ground and Vcc pins, along with the device technology, help maintain low levels of ground bounce, making the clock drivers very quiet, low-noise devices. Low input capacitance avoids loading of the source clock, maintaining high signal quality. Wide fanout capability allows reduced part count and optimized clock distribution. Input hysteresis assists in cleaning up slow or ragged clock edges.

5V FCT PLL Clock Generators

IDT's high-frequency, low-skew PLL clock generators are ideal for applications requiring zero delay clock generation, low-skew clock distribution, frequency multiplication, or frequency division. Output skews of less than 500ps and maximum output frequencies of up to 133MHz are offered.

5V FCT Clock Buffers

IDT's 5V clock buffers are available in a variety of configurations including 1-to-10 fanout buffers, dual 1-to-5 buffers, combined inverting/noninverting buffers and with either CMOS or TTL output levels. IDT offers high-performance clock drivers in a variety of fanout configurations with pin-to-pin skews of less than 250ps and worst case propagation delays of less than 2.5ns.

3.3V FCT Clock Drivers

Several of the 5V PLL clock generators and clock buffers are also available in 3.3V versions, allowing an easy upgrade path from 5V to 3.3V operation. Most IDT 3.3V components will accept 5V signal levels at the device inputs, making 3.3V clock distribution possible from a 5V interface. The 3.3V operating voltage and low power consumption of these devices make them ideal for battery-based operation of portable computing devices.

IDT 3.3V Clock Drivers have output skews under 500ps and support output frequencies up to 150MHz (FCT388915T).

In addition to buffers and PLL-based drivers, the 3.3V Clock family includes configurable PLLs and Clock Synthesizers like the FCT3907. The FCT3932 features 18 outputs organized into 3 banks and 16 programmable frequency configurations. Output banks can be easily configured for frequency multiplication, division or inversion. The FCT3907 synthesizes requisite motherboard frequencies from a 14.31818MHz crystal input.

SECTION 9
CLOCK MANAGEMENT PRODUCTS
TABLE OF CONTENTS

Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT805/A
IDT49FCT806/A

FEATURES:

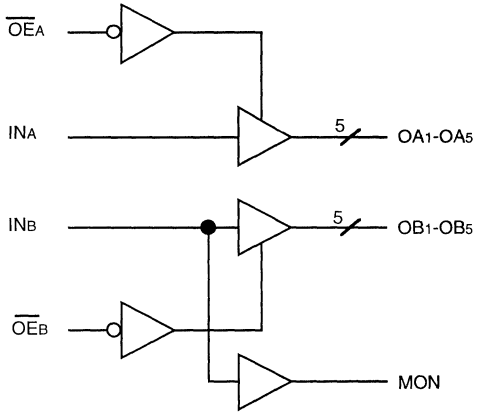
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 700ps (max.)
- Low duty cycle distortion < 1ns (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- Rail-to-rail output voltage swing
- High drive: -24mA I_{OH}, 64mA I_{OL}
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- 'Heartbeat' monitor output
- Available in DIP, SOIC, SSOP (805 only), Cerpack and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49FCT805/A and IDT49FCT806/A are clock drivers built using advanced dual metal CMOS technology. The IDT49FCT805/A is a non-inverting clock driver and the IDT49FCT806/A is an inverting clock driver. Each device consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. The devices feature a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The IDT49FCT805/A and IDT49FCT806/A offer low capacitance inputs with hysteresis. Rail-to-rail output swing improves noise margin and allows easy interface with CMOS inputs.

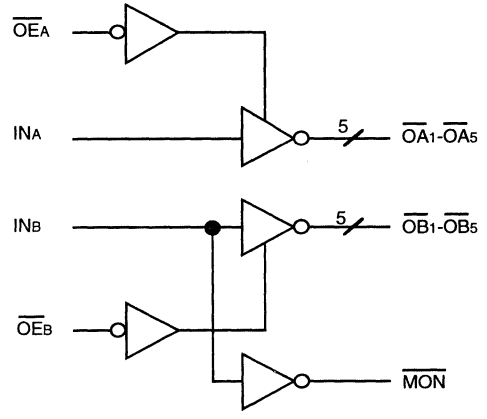
FUNCTIONAL BLOCK DIAGRAMS

IDT49FCT805



2574 drw 01

IDT49FCT806



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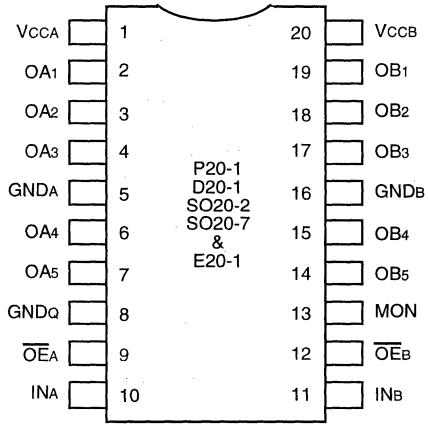
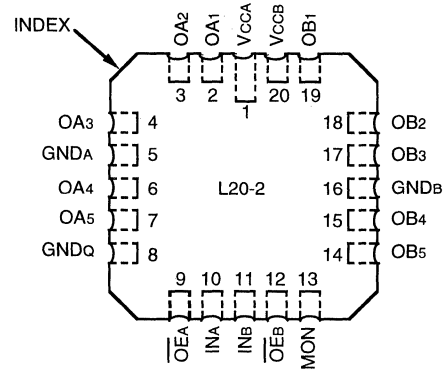
PIN CONFIGURATIONS

IDT49FCT805



DIP/SOIC/SSOP/CERPACK
TOP VIEW

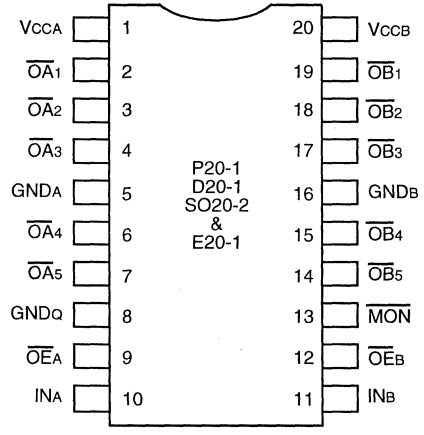
2574 drw 03



LCC
TOP VIEW

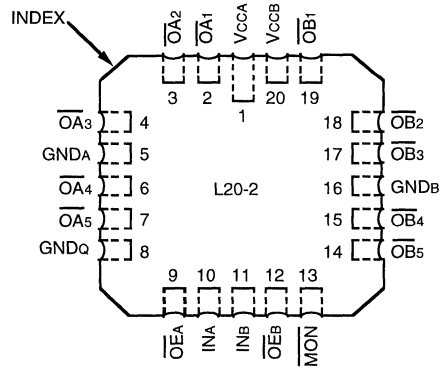
2574 drw 04

IDT49FCT806



DIP/SOIC/CERPACK
TOP VIEW

2574 drw 05



LCC
TOP VIEW

2574 drw 06

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_n, OB_n	Clock Outputs (FCT805)
$\overline{OA}_n$, $\overline{OB}_n$	Clock Outputs (FCT806)
MON	Monitor Output (FCT805)
$\overline{MON}$	Monitor Output (FCT806

2574 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs			
		49FCT805		49FCT806	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OA_n, OB_n	MON	$\overline{OA}_n$, $\overline{OB}_n$	$\overline{MON}$
L	L	L	L	H	H
L	H	H	H	L	L
H	L	Z	L	Z	H
H	H	Z	H	Z	L

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance

2574 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES: 2574 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 2574 lnk 04

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(5)	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current(5)	V_{CC} = Max.	V_I = GND	—	—	±1	µA
I_{OZH}	Off State (HIGH Z)(5)	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	Output Current(5)		V_O = GND	—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	3.6	4.3	—	
			I_{OH} = -24mA MIL. I_{OH} = -24mA COM'L.	2.4	3.8	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OH} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.3	0.55	
V_H	Input Hysteresis for all inputs	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

NOTES: 2574 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	1.0	2.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.20	mA/ MHz/bit
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fo= 10MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ =V_{CC} Mon. Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	2.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.0	3.8	
		V_{CC} = Max. Outputs Open fo = 2.5MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	4.1	6.0[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.1	8.5[5]	

2574 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_o N_O)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   fo= Output Frequency
   No= Number of Outputs at fo
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3,4]

Symbol	Parameter	Condition[1]	IDT49FCT805/806				IDT49FCT805A/806A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	7.5	1.5	5.8	1.5	6.8	ns
t_R	Output Rise Time		—	1.5	—	1.5	—	1.5	—	1.5	ns
t_F	Output Fall Time		—	1.5	—	1.5	—	1.5	—	1.5	ns
$t_{SK(o)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.9	—	0.7	—	0.9	ns
$t_{SK(p)}$	Pulse skew: skew between opposite transitions of same output ($\lvert t_{PHL} - t_{PLH} \rvert$)		—	1.0	—	1.1	—	1.0	—	1.1	ns
$t_{SK(t)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—	1.5	—	1.5	—	1.5	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	8.0	1.5	8.5	1.5	8.0	1.5	8.5	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	7.0	1.5	7.5	1.5	7.0	1.5	7.5	ns

NOTES:

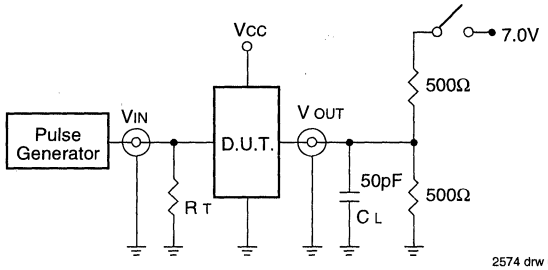
2574 tbl 07

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, t_{SK}(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

9

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2574 drw 07

ENABLE AND DISABLE TIME SWITCH POSITION

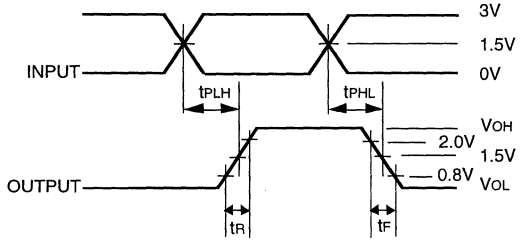
Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	Open

2574 lnk 11

DEFINITIONS:

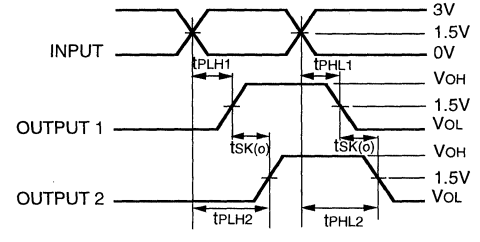
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

PACKAGE DELAY



2574 drw 08

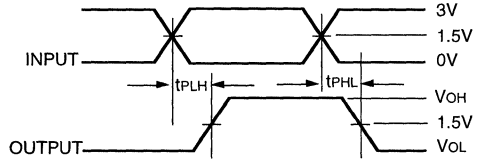
OUTPUT SKEW - tSK(o)



$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

2574 drw 09

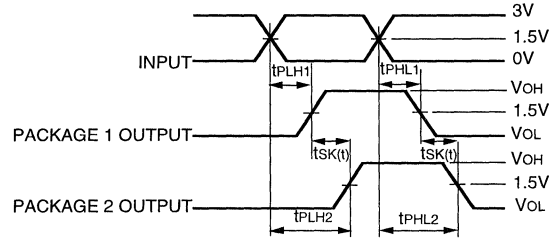
PULSE SKEW - tSK(p)



$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

2574 drw 10

PACKAGE SKEW - tSK(t)

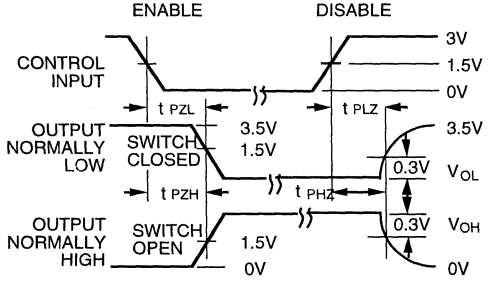


$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Package 1 and Package 2 are same device type and speed grade

2574 drw 11

ENABLE AND DISABLE TIMES

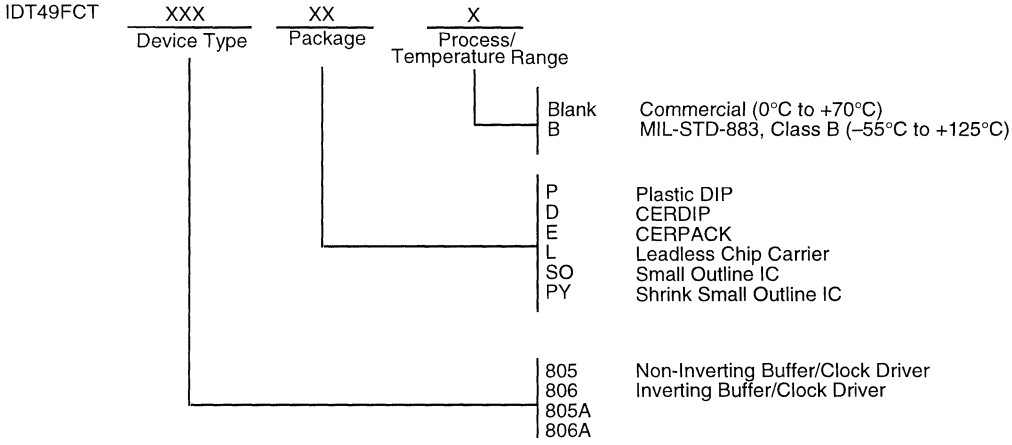


2574 drw 12

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: f ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



2574 drw 17

9

Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT805BT/CT
IDT49FCT806BT/CT

FEATURES:

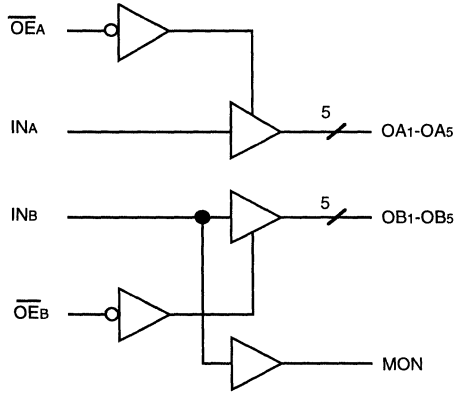
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 600ps (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- TTL level output voltage swings
- High drive: -32mA I_{OH}, 48mA I_{OL}
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- 'Heartbeat' monitor output
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in DIP, SOIC, SSOP, Cerpack and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49FCT805BT/CT and IDT49FCT806BT/CT are clock drivers built using advanced dual metal CMOS technology. The IDT49FCT805BT/CT is a non-inverting clock driver and the IDT49FCT806BT/CT is an inverting clock driver. Each device consists of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. The 805BT/CT and 806BT/CT have extremely low output skew, pulse skew, and package skew. The devices has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The 805BT/CT and 806BT/CT offer low capacitance inputs with hysteresis.

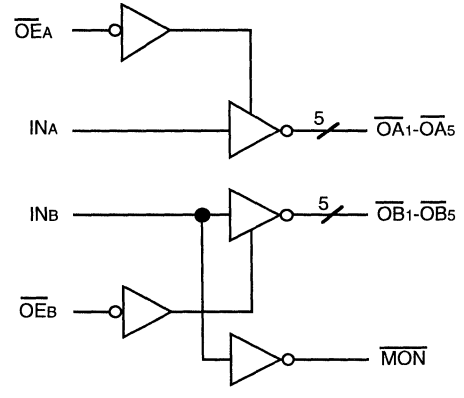
FUNCTIONAL BLOCK DIAGRAMS

IDT49FCT805T



2920 drw 01

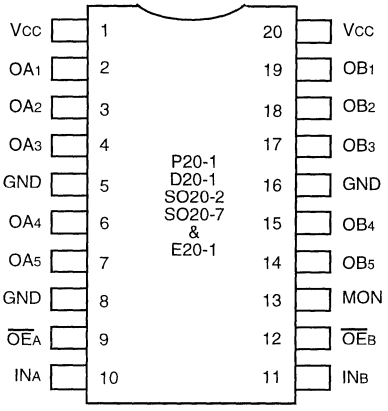
IDT49FCT806T



2920 drw 02

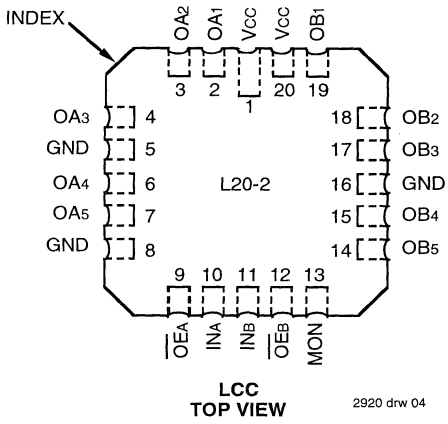
PIN CONFIGURATIONS

IDT49FCT805T



DIP/SOIC/SSOP/CERPACK
TOP VIEW

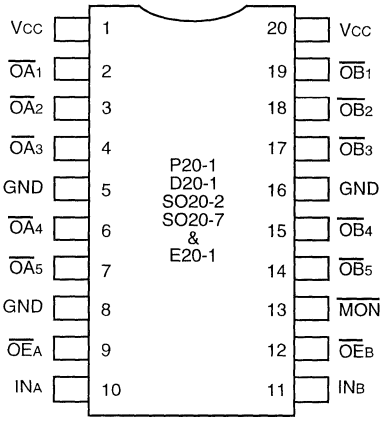
2920 drw 03



LCC
TOP VIEW

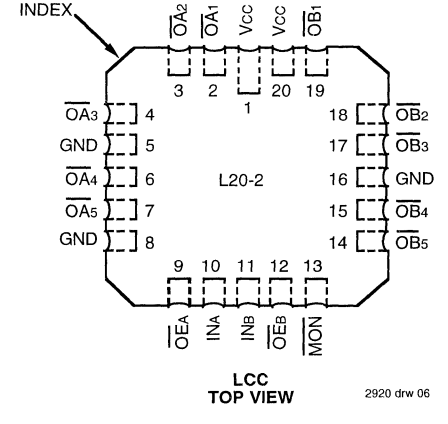
2920 drw 04

IDT49FCT806T



DIP/SOIC/SSOP/CERPACK
TOP VIEW

2920 drw 05



LCC
TOP VIEW

2920 drw 06

PIN DESCRIPTION

Pin Names	Description
$\overline{OE_A}$, $\overline{OE_B}$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_n, OB_n	Clock Outputs (FCT805T)
$\overline{OA_n}$, $\overline{OB_n}$	Clock Outputs (FCT806T)
MON	Monitor Output (FCT805T)
$\overline{MON}$	Monitor Output (FCT806T)

2920 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs			
		49FCT805T		49FCT806T	
$\overline{OE_A}$, $\overline{OE_B}$	IN_A, IN_B	OA_n, OB_n	MON	$\overline{OA_n}$, $\overline{OB_n}$	$\overline{MON}$
L	L	L	L	H	H
L	H	H	H	L	L
H	L	Z	L	Z	H
H	H	Z	H	Z	L

NOTE:
1. H = HIGH, L = LOW, Z = High Impedance

2920 tbl 02

9

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc +0.5	–0.5 to Vcc +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

2920 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

2920 lnk 04

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
Commercial: T_A = 0°C to +70°C, Vcc = 5.0V ± 5%; Military: T_A = –55°C to +125°C, Vcc = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current(5)	Vcc = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current(5)	Vcc = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	Vcc = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)(5)		V_O = 0.5V	—	—	±1	µA
I_I	Input HIGH Current(5)	Vcc = Max., V_I = Vcc (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	Vcc = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	Vcc = Max.(3), V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(4)	2.0	3.0	—	
V_{OL}	Output LOW Voltage	Vcc = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage(5)	Vcc = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis for all inputs	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	Vcc = Max., V_{IN} = GND or Vcc		—	5	500	µA

2920 lnk 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz/bit
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fo = 25MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ =V_{CC} Mon. Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	1.8	4.0	
		V_{CC} = Max. Outputs Open fo = 50MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	33	55.5[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	33.5	57.5[5]	

2920 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (fo N_O)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   fo= Output Frequency
   N_O= Number of Outputs at fo
   All currents are in milliamps and all frequencies are in megahertz.

9

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3,4]

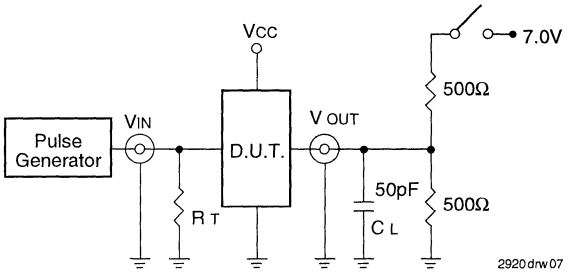
Symbol	Parameter	Condition[1]	IDT49FCT805BT/806BT				IDT49FCT805CT/806CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	5.0	1.5	5.7	1.5	4.5	1.5	5.2	ns
t_R	Output Rise Time		—	1.5	—	2.0	—	1.5	—	2.0	ns
t_F	Output Fall Time		—	1.5	—	1.5	—	1.5	—	1.5	ns
$t_{SK}(o)$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	0.9	—	0.5	—	0.7	ns
$t_{SK}(p)$	Pulse skew: skew between opposite transitions of same output ($\lvert t_{PHL} - t_{PLH} \rvert$)		—	0.7	—	0.9	—	0.6	—	0.8	ns
$t_{SK}(t)$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.2	—	1.5	—	1.0	—	1.2	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	6.0	1.5	6.5	1.5	5.0	1.5	6.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	6.0	1.5	6.5	1.5	5.0	1.5	6.0	ns

2920 tbl 07

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK}(t)$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR ALL OUTPUTS



2920 drw 07

ENABLE AND DISABLE TIME SWITCH POSITION

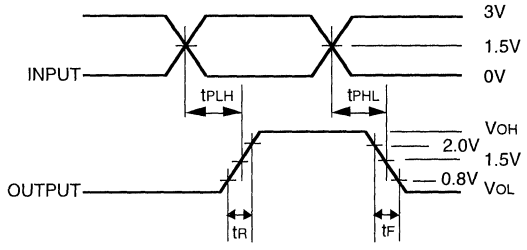
Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	Open

2920 lnk 08

DEFINITIONS:

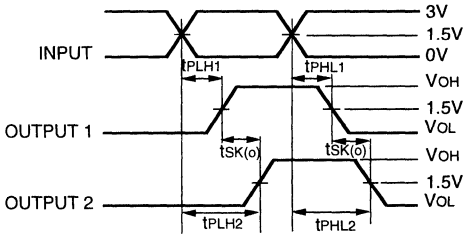
CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

PACKAGE DELAY



2920 drw 08

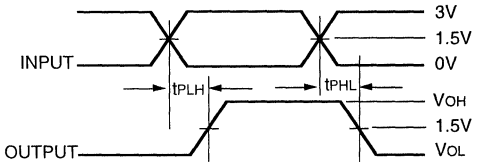
OUTPUT SKEW- tSK(o)



tSK(o) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

2920 drw 09

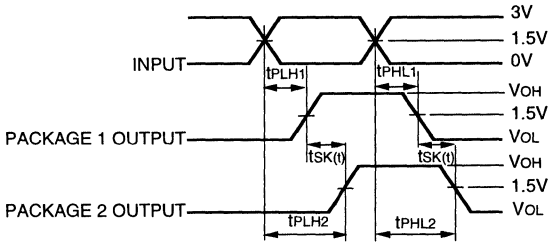
PULSE SKEW - tSK(p)



tSK(p) = |tPHL - tPLH|

2920 drw 10

PACKAGE SKEW - tSK(t)

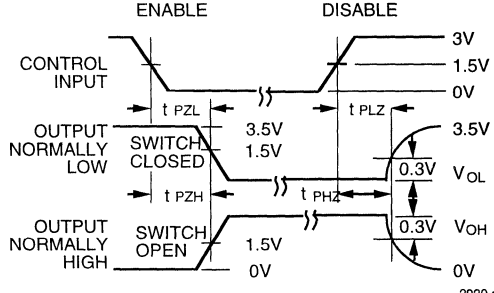


tSK(t) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

Package 1 and Package 2 are same device type and speed grade

2920 drw 11

ENABLE AND DISABLE TIMES



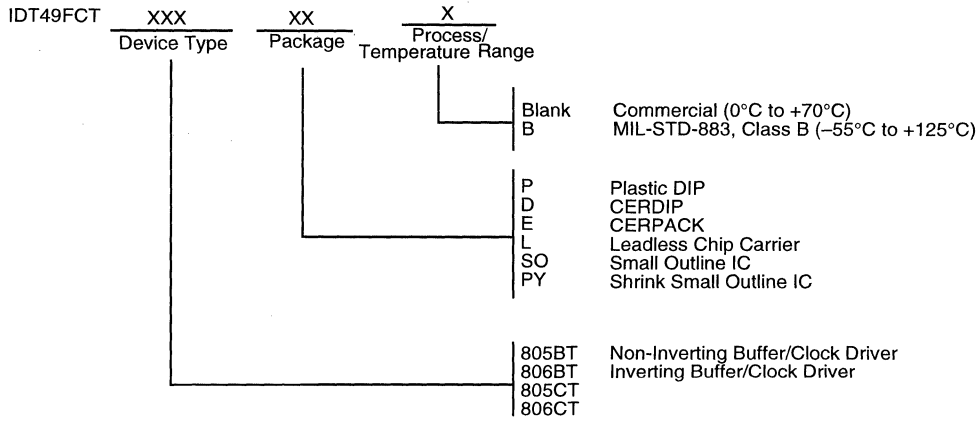
2920 drw 12

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: f ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

9

ORDERING INFORMATION



2920 drw 13

Integrated Device Technology, Inc.

FAST CMOS 1-TO-10 CLOCK DRIVER

IDT54/74FCT807BT/CT

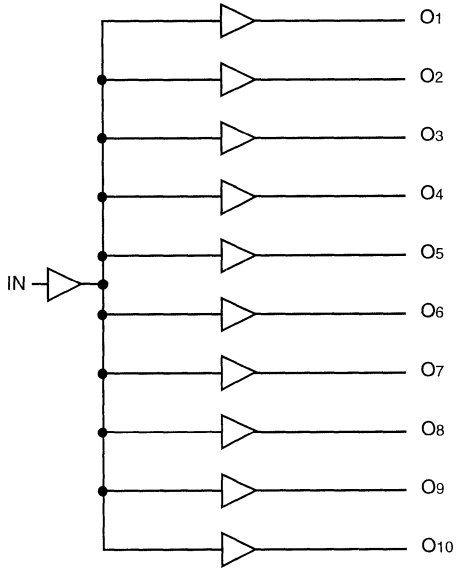
FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 250ps (max.)
- Very low duty cycle distortion < 350ps (max.)
- High speed: propagation delay < 2.5ns (max.)
- 100MHz operation
- TTL compatible inputs and outputs
- TTL level output voltage swings
- 1:10 fanout
- Output rise and fall time < 1.5ns (max.)
- Low input capacitance: 4.5pF typical
- High Drive: -32mA IOH, 48mA IOL
- ESD > 2000V per MIL STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in DIP, SOIC, SSOP, Cerpack and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

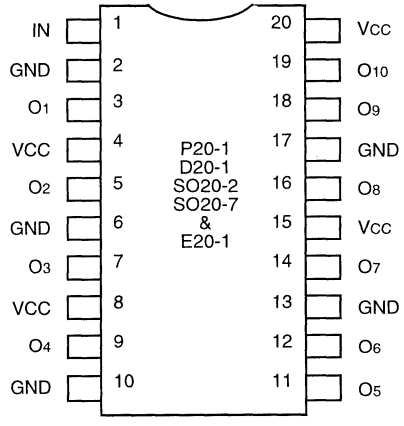
The IDT54/74FCT807BT/CT clock driver is built using advanced dual metal CMOS technology. This low skew clock driver features 1:10 fanout, providing minimal loading on the preceding drivers. The IDT54/74FCT807BT/CT offers low capacitance inputs with hysteresis for improved noise margins. TTL level outputs and multiple power and grounds reduce noise. The device also features -32/48mA drive capability for driving low impedance traces.

FUNCTIONAL BLOCK DIAGRAM



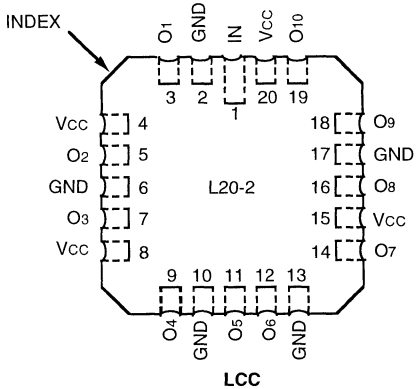
3017 drw 01

PIN CONFIGURATIONS



3017 drw 02

DIP/SOIC/SSOP/CERPACK TOP VIEW



LCC TOP VIEW

3017 drw 03

PIN DESCRIPTION

Pin Names	Description
IN	Input
Ox	Outputs

3017 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

3017 lnk 02

NOTE:
1. This parameter is measured at characterization but not tested.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

3017 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[5]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[5]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	µA
I_I	Input HIGH Current[5]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA
V_H	Input Hysteresis for all inputs	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

3017 lnk 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[3]	V_{CC} = Max. Input toggling 50% Duty Cycle Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—	0.4	0.6	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Input toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	20.0	30.5[4]	mA
		Outputs Open fi = 50MHz	V_{IN} = 3.4V V_{IN} = GND	—	20.3	31.3[4]	

3017 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i= Input Frequency
   All currents are in milliamps and all frequencies are in megahertz.

9

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3,4]

Symbol	Parameter	Conditions[1]	IDT54/74FCT807BT				IDT54/74FCT807CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay	50Ω to Vcc/2, C_L = 10pF	1.3	2.7			1.3	2.5			ns
t_R	Output Rise Time	(See figure 1)	—	1.5	—		—	1.5	—		ns
t_F	Output Fall Time	or 50Ω ac	—	1.5	—		—	1.5	—		ns
t_{SK}(o)	Output skew: skew between outputs of same package (same transition)	termination, C_L = 10pF	—	0.5	—		—	0.25	—		ns
t_{SK}(p)	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)	(See figure 2) f ≤ 100MHz	—	0.5	—		—	0.35	—		ns
t_{SK}(t)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	Outputs connected in groups of two	—	0.9	—		—	0.65	—		ns

3017 tbl 06

Symbol	Parameter	Conditions[1]	IDT54/74FCT807BT				IDT54/74FCT807CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay	C_L = 30pF f ≤ 67MHz	1.5	3.8			1.5	3.5			ns
t_R	Output Rise Time	(See figure 3)	—	1.5	—		—	1.5	—		ns
t_F	Output Fall Time		—	1.5	—		—	1.5	—		ns
t_{SK}(o)	Output skew: skew between outputs of same package (same transition)		—	0.5	—		—	0.25	—		ns
t_{SK}(p)	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		—	0.5	—		—	0.35	—		ns
t_{SK}(t)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	0.9	—		—	0.75	—		ns

3017 tbl 07

Symbol	Parameter	Conditions[1]	IDT54/74FCT807BT				IDT54/74FCT807CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay	C_L = 50pF f ≤ 40MHz	1.5	3.8			1.5	3.5			ns
t_R	Output Rise Time	(See figure 4)	—	1.5	—		—	1.5	—		ns
t_F	Output Fall Time		—	1.5	—		—	1.5	—		ns
t_{SK}(o)	Output skew: skew between outputs of same package (same transition)		—	0.5	—		—	0.35	—		ns
t_{SK}(p)	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		—	0.60	—		—	0.45	—		ns
t_{SK}(t)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.0	—		—	0.75	—		ns

3017 tbl 08

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, t_{SK}(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to Vcc, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS

50Ω TO Vcc/2, CL = 10pF

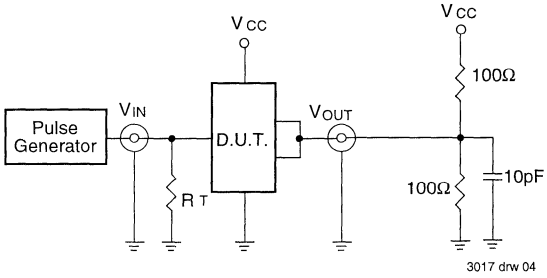
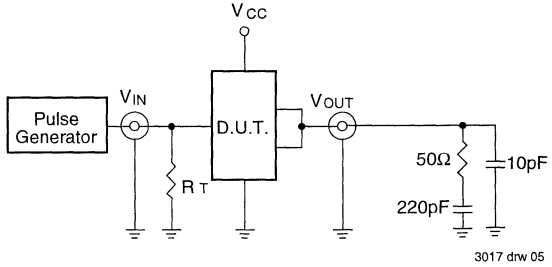


Figure 1.

50Ω AC TERMINATION, CL = 10pF



The capacitor value for ac termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

Figure 2.

CL = 30pF CIRCUIT

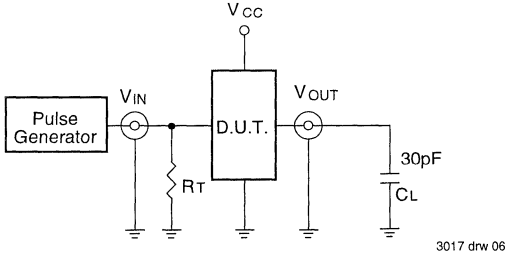


Figure 3.

CL = 50pF CIRCUIT

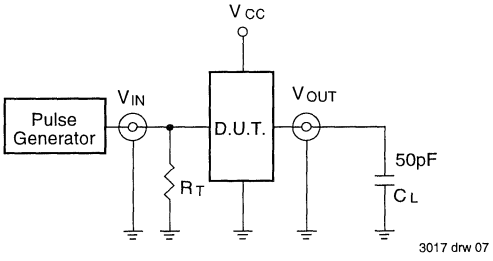


Figure 4.

ENABLE AND DISABLE TIME CIRCUIT

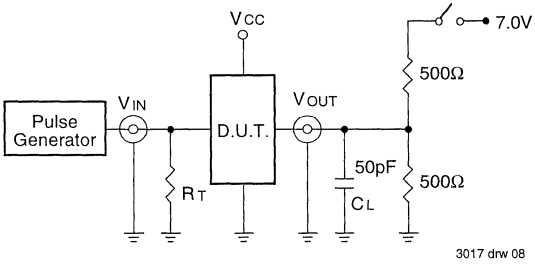


Figure 5.

ENABLE AND DISABLE TIME SWITCH POSITION

Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	Open

3017 lnk 09

DEFINITIONS:

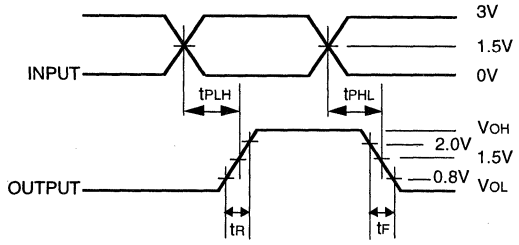
CL= Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

9

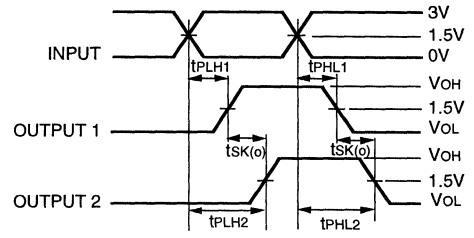
TEST WAVEFORMS

PACKAGE DELAY



3017 drw 09

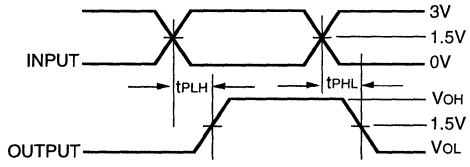
OUTPUT SKEW- tSK(o)



tSK(o) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

3017 drw 10

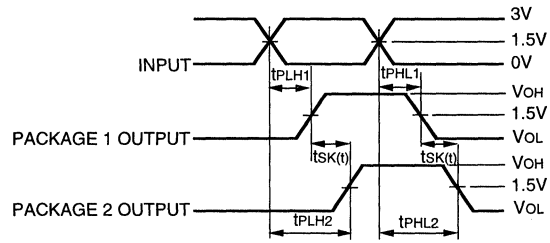
PULSE SKEW - tSK(p)



tSK(p) = |tPHL - tPLH|

3017 drw 11

PACKAGE SKEW - tSK(t)

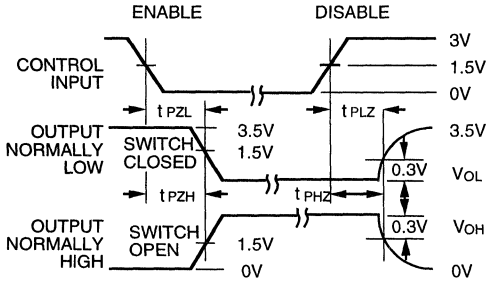


tSK(t) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

Package 1 and Package 2 are same device type and speed grade

3017 drw 12

ENABLE AND DISABLE TIMES

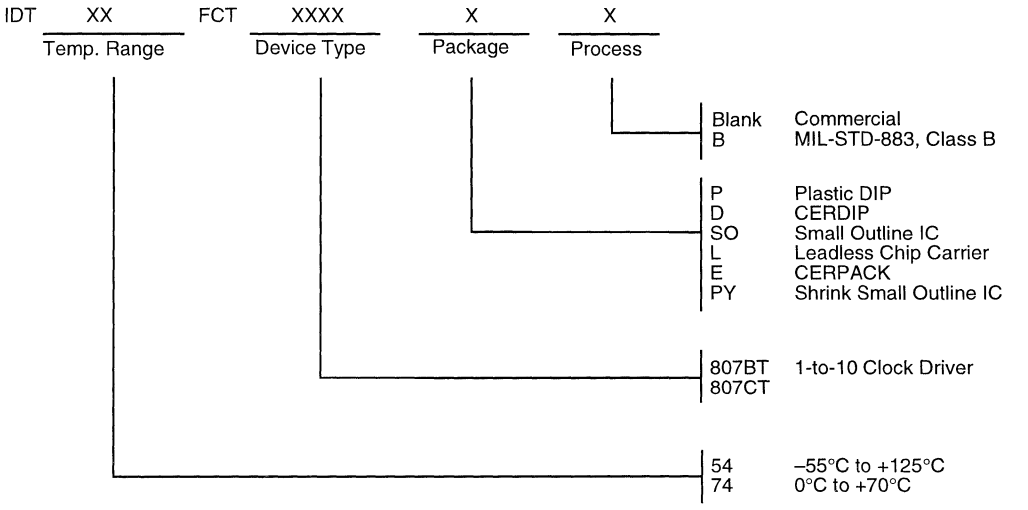


3017 drw 13

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: f ≤ 1.0MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

ORDERING INFORMATION



3017 drw 14

9

Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT54/74FCT810BT/CT

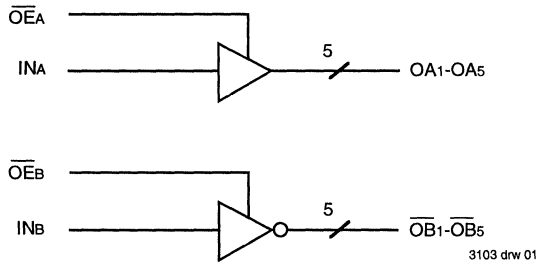
FEATURES:

- 0.5 MICRON CMOS technology
- Guaranteed low skew < 600ps (max.)
- Very low duty cycle distortion < 700ps (max.)
- Low CMOS power levels
- TTL compatible inputs and outputs
- TTL level output voltage swings
- High drive: –32mA I_{OH}, 48mA I_{OL}
- Two independent output banks with 3-state control
  - One 1:5 Inverting bank
  - One 1:5 Non-Inverting bank
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

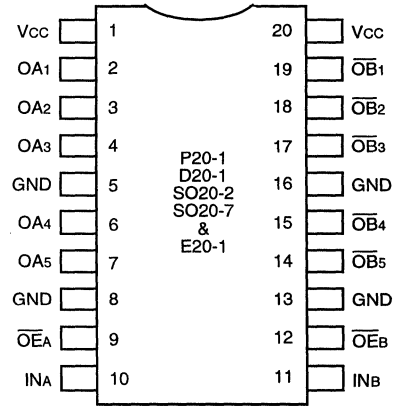
The IDT54/74FCT810BT/CT is a dual bank inverting/ non-inverting clock driver built using advanced dual metal CMOS technology. It consists of two banks of drivers, one inverting and one non-inverting. Each bank drives five output buffers from a standard TTL-compatible input. The IDT54/ 74FCT810BT/CT have low output skew, pulse skew and package skew. Inputs are designed with hysteresis circuitry for improved noise immunity. The outputs are designed with TTL output levels and controlled edge rates to reduce signal noise. The part has multiple grounds, minimizing the effects of ground inductance.

FUNCTIONAL BLOCK DIAGRAMS



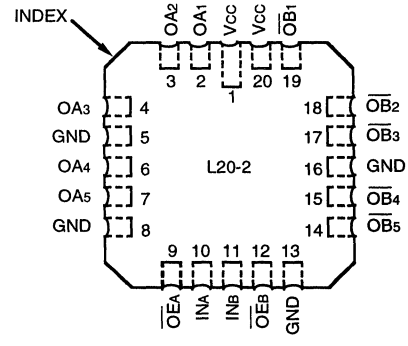
3103 drw 01

PIN CONFIGURATIONS



3103 drw 02

DIP/SOIC/SSOP/CERPACK
TOP VIEW



LCC
TOP VIEW

3103 drw 03

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_n, $\overline{OB}_n$	Clock Outputs

3103 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE:
1. This parameter is measured at characterization but not tested.

3103 lnk 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

NOTES:

3103 lnk 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[5]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[5]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	µA
I_I	Input HIGH Current[5]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_O = GND		–60	–120	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.3	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[4]	2.0	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.55	V
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA
V_H	Input Hysteresis for all inputs	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	5	500	µA

NOTES:

3103 lnk 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ± 5µA at T_A = –55°C.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz/bit
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fo= 25MHz 50% Duty Cycle $\overline{OE}_A$ = GND, $\overline{OE}_B$ =V_{CC}	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	7.5 7.8	13 14.0	mA
		V_{CC} = Max. Outputs Open fo = 50MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND	V_{IN} = V_{CC} V_{IN} = GND V_{IN} = 3.4V V_{IN} = GND	— —	30.0 30.5	50.5[5] 52.5[5]	

3103 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (fo N_O)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   fo= Output Frequency
   N_O= Number of Outputs at fo
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3,4]

Symbol	Parameter	Condition[1]	IDT54/74FCT810BT				IDT54/74FCT810CT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay INA to OA_n, INB to $\overline{OB}_n$	C_L = 50pF R_L = 500Ω	1.5	4.5	1.5	4.9	1.5	4.3	1.5	4.6	ns
t_R	Output Rise Time		—	1.5	—	2.0	—	1.5	—	2.0	ns
t_F	Output Fall Time		—	1.5	—	1.5	—	1.5	—	1.5	ns
$t_{SK1}(o)$	Output skew (same bank): skew between outputs of same bank and same package (same transition)		—	0.5	—	0.9	—	0.3	—	0.7	ns
$t_{SK2}(o)$	Output skew (all banks): skew between outputs of all banks of same package (inputs tied together)		—	0.7	—	1.1	—	0.6	—	1.0	ns
$t_{SK}(p)$	Pulse skew: skew between opposite transitions of same output $\lvert(t_{PHL}-t_{PLH})\rvert$		—	0.7	—	1.2	—	0.7	—	1.1	ns
$t_{SK}(t)$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.2	—	1.5	—	1.0	—	1.2	ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to $\overline{OB}_n$		1.5	6.0	1.5	6.5	1.5	5.0	1.5	6.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to $\overline{OB}_n$		1.5	6.0	1.5	6.5	1.5	5.0	1.5	6.0	ns

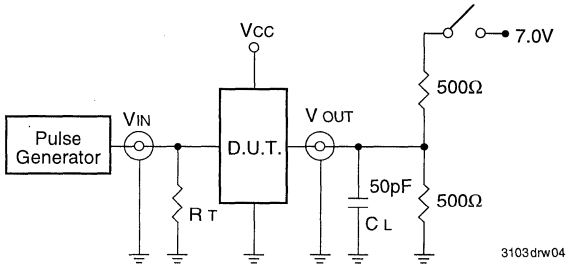
3103 tbl 06

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK}(t)$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

9

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR ALL OUTPUTS



ENABLE AND DISABLE TIME SWITCH POSITION

Test	Switch
Disable LOW Enable LOW	Closed
Disable HIGH Enable HIGH	Open

3103 lnk 07

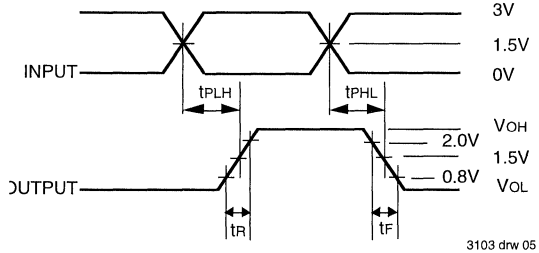
DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

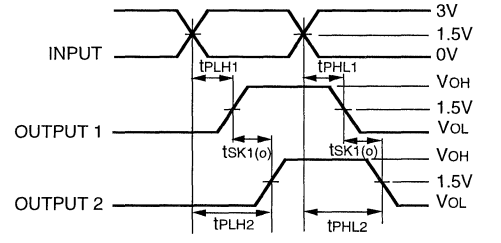
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

TEST WAVEFORMS

PACKAGE DELAY



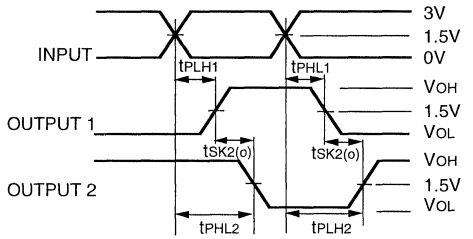
OUTPUT SKEW (SAME BANK) - tSK1(o)



$t_{SK1(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

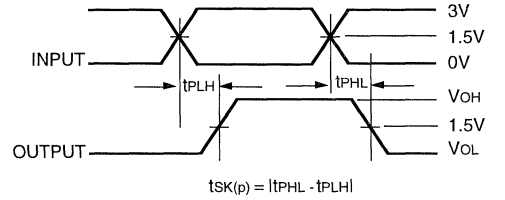
3103 drw 06

OUTPUT SKEW (ALL BANKS) - tSK2(o)



$t_{SK2(o)} = |t_{PHL2} - t_{PLH1}|$ or $|t_{PLH2} - t_{PHL1}|$ 3103 drw 07

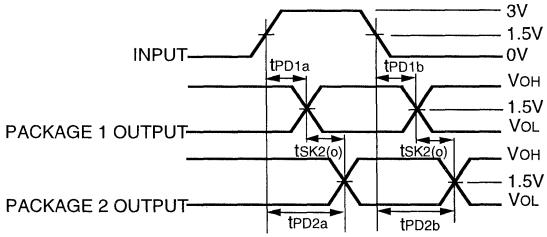
PULSE SKEW - tSK(p)



$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

3103 drw 08

PACKAGE SKEW - tSK(t)

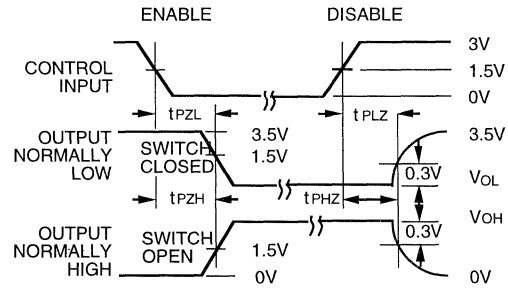


$t_{SK(t)} = |t_{PD2a} - t_{PD1a}|$ or $|t_{PD2b} - t_{PD1b}|$

Package 1 and Package 2 are same device type and speed grade

3103 drw 09

ENABLE AND DISABLE TIMES

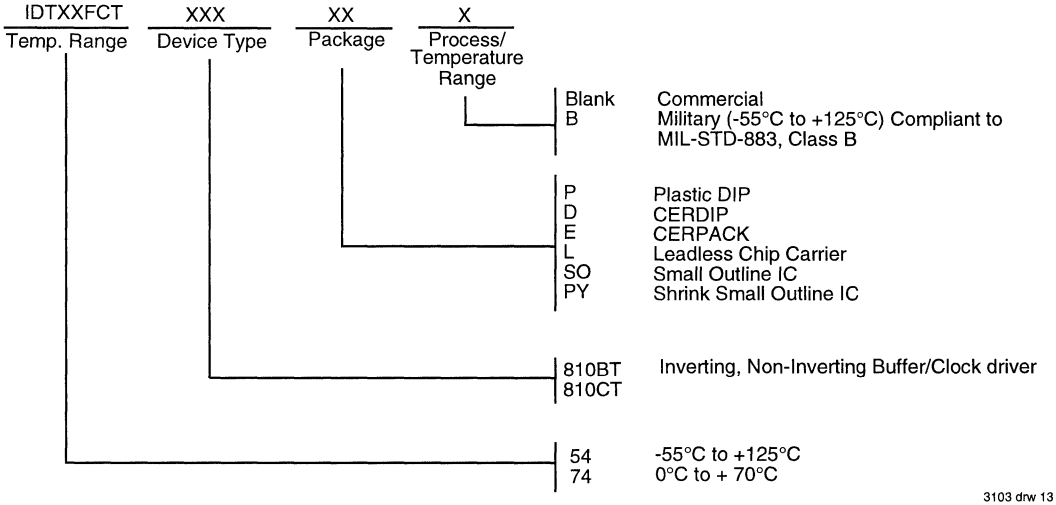


3103 drw 10

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: f ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



3103 drw 13

9

Integrated Device Technology, Inc.

FAST CMOS BUFFER/CLOCK DRIVER

IDT49FCT3805/A

FEATURES:

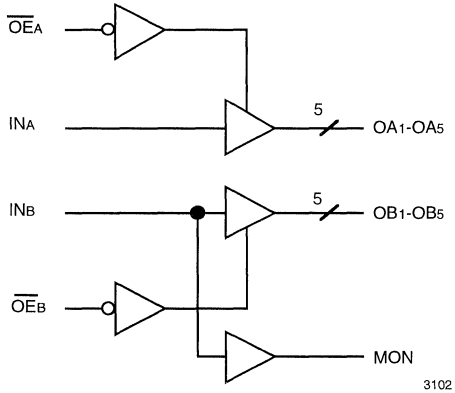
- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 1.0ns (max.)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- Inputs can be driven from 3.3V or 5V components
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- 'Heartbeat' monitor output
- Available in DIP, SOIC, SSOP, Cerpack and LCC packages
- Military product compliant to MIL-STD-883, Class B
- V_{CC} = 3.3V ± 0.3V

DESCRIPTION:

The FCT3805/A is a 3.3 volt, non-inverting clock driver built using advanced dual metal CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The FCT3805/A offers low capacitance inputs with hysteresis.

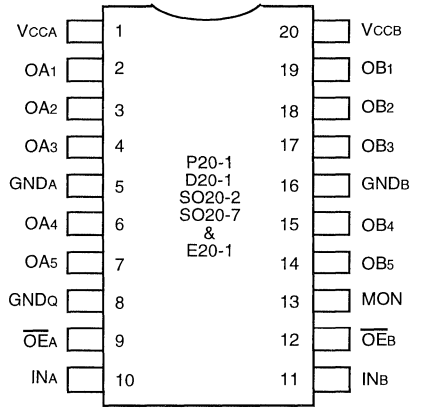
The FCT3805/A is designed for high speed clock distribution where signal quality and skew are critical. The FCT 3805 also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple receivers with low skew and high signal quality.

FUNCTIONAL BLOCK DIAGRAM



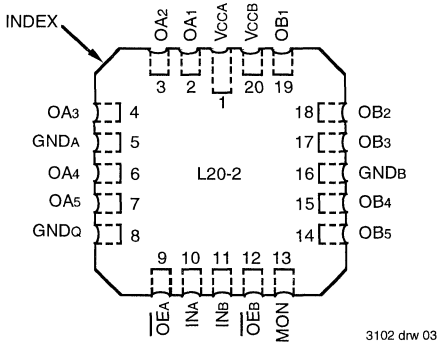
3102 drw 01

PIN CONFIGURATIONS



3102 drw 02

DIP/SOIC/SSOP/CERPACK TOP VIEW



3102 drw 03

LCC TOP VIEW

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
IN_A, IN_B	Clock Inputs
OA_n, OB_n	Clock Outputs
MON	Monitor Output

3102 tbl 01

FUNCTION TABLE[1]

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	IN_A, IN_B	OA_n, OB_n	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE: 3102 tbl 02
1. H = HIGH, L = LOW, Z = High Impedance

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 3102 lnk 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	5.0	pF

NOTE: 3102 lnk 04
1. This parameter is measured at characterization but not tested.

9

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.50	
I_{OFF}	Input Power Off Leakage[6]	V_{CC} = 0V, V_{IN} ≤ 4.5V		—	—	±1	µA
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max.,	COM'L.	—	0.1	10	µA
I_{CCH} I_{CCZ}		V_{IN} = GND or V_{CC}	MIL.	—	0.1	100	

3102 lnk 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} -0.6V at rated current.
6. The test limit for this parameter is ±5µA at TA = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} –0.6V[3]		—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$ = GND Per Output Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.035	0.06	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open fo = 25MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ =V_{CC} Mon. Output Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	0.9	1.6	mA
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	0.9	1.6	
		V_{CC} = Max. Outputs Open fo = 50MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$ = GND Eleven Outputs Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	20.0	33.0[5]	
			V_{IN} = V_{CC} –0.6V V_{IN} = GND	—	20.0	33.0[5]	

3102 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input (V_{IN} = V_{CC} -0.6V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
6. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} (f$_0$N$_0$)
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} -0.6V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   fo = Output Frequency
   No = Number of Outputs at fo
   All currents are in milliamps and all frequencies are in megahertz.

9

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3,4]

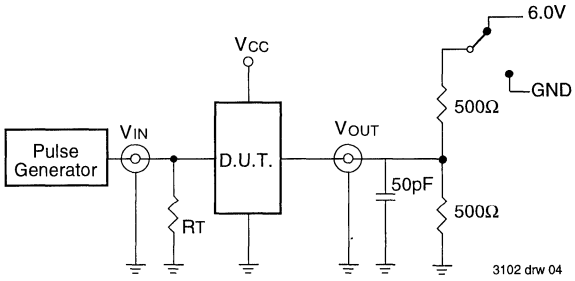
Symbol	Parameter	Condition[1]	FCT3805				FCT3805A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L = 50pF R_L = 500Ω	1.5	5.8			1.5	5.0			ns
t_R	Output Rise Time		—	2.0	—		—	2.0	—		ns
t_F	Output Fall Time		—	2.0	—		—	2.0	—		ns
$t_{SK(o)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.7	—		—	0.5	—		ns
$t_{SK(p)}$	Pulse skew: skew between opposite transitions of same output ($\lvert t_{PHL} - t_{PLH} \rvert$)		—	1.2	—		—	1.0	—		ns
$t_{SK(t)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—		—	1.2	—		ns
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	6.5			1.5	6.0			ns
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	5.5			1.5	5.0			ns

3102 tbl 07

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK(t)}$ production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR ALL OUTPUTS



3102 drw 04

ENABLE AND DISABLE TIME SWITCH POSITION

Test	Switch
Disable LOW Enable LOW	6.0V
Disable HIGH Enable HIGH	GND

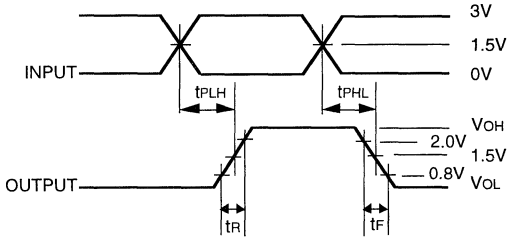
3102 tbl 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

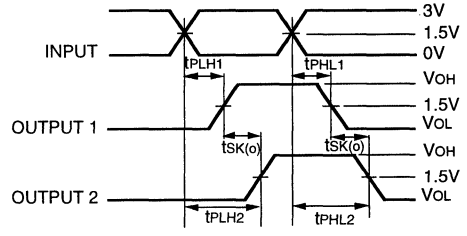
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

PACKAGE DELAY



3102 drw 05

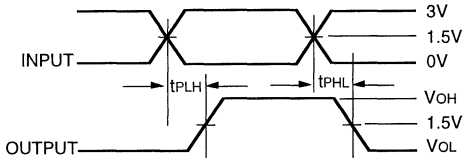
OUTPUT SKEW- tSK(o)



$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

3102 drw 06

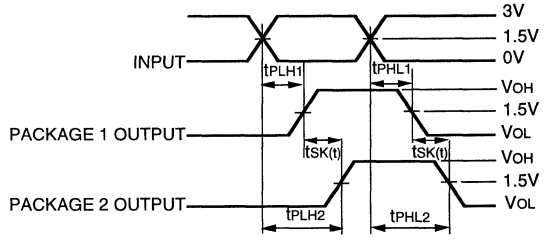
PULSE SKEW- tSK(p)



$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

3102 drw 07

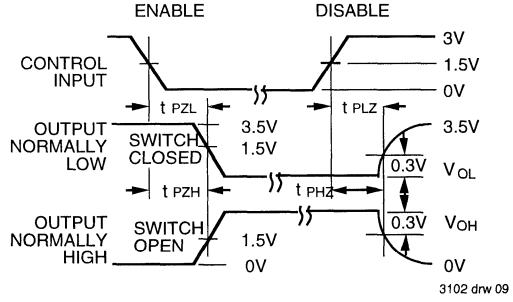
PACKAGE SKEW- tSK(t)



$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

3102 drw 08

ENABLE AND DISABLE TIMES



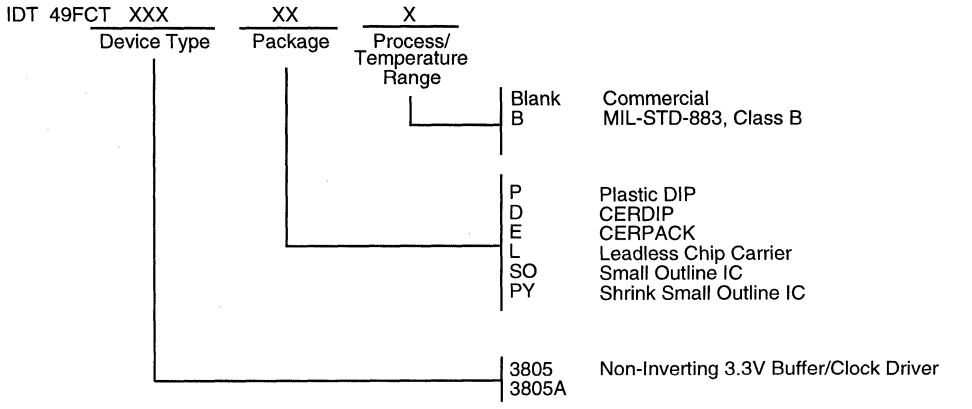
3102 drw 09

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: f ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

9

ORDERING INFORMATION



3102 drw 10

Integrated Device Technology, Inc.

3.3V CMOS 1-TO-10 CLOCK DRIVER

IDT54/74FCT3807/A
PRELIMINARY

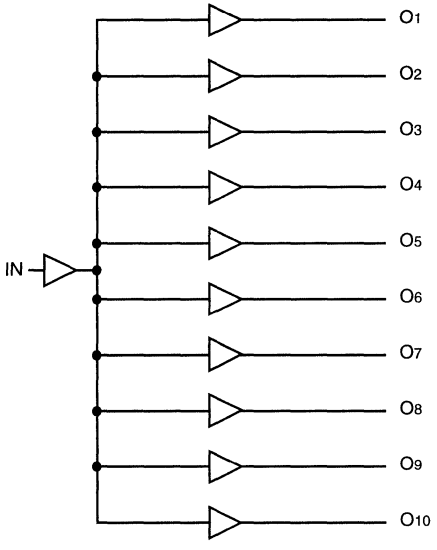
FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 350ps (max.)
- Very low duty cycle distortion < 350ps (max.)
- High speed: propagation delay < 3.0ns (max.)
- 100 MHz operation
- Very low CMOS power levels
- TTL compatible inputs and outputs
- 1:10 fanout
- Maximum output rise and fall time < 1.5ns (max.)
- Low input capacitance: 4.5pF typical
- Vcc = 3.3V ±0.3V
- Inputs can be driven from 3.3V or 5V components
- Available in DIP, SOIC, SSOP, Cerpack and LCC packages
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

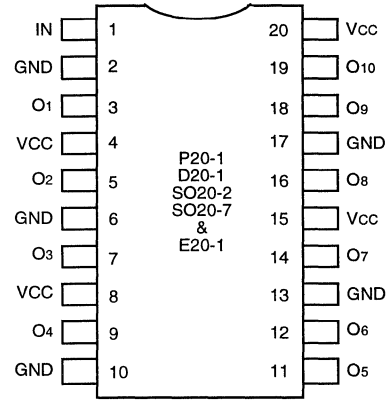
The FCT3807/A 3.3V clock driver is built using advanced dual metal CMOS technology. This low skew clock driver offers 1:10 fanout. The large fanout from a single input reduces loading on the preceding driver and provides an efficient clock distribution network. The FCT807/A offers low capacitance inputs with hysteresis for improved noise margins. Multiple power and grounds reduce noise. Typical applications are clock and signal distribution.

FUNCTIONAL BLOCK DIAGRAM



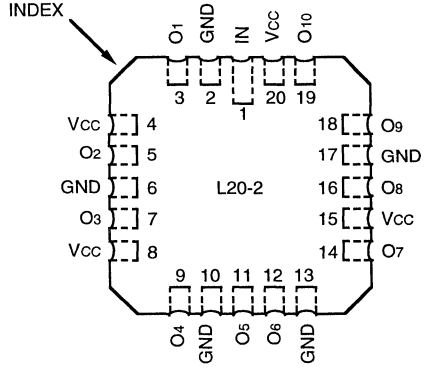
3046 drw 01

PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK
TOP VIEW

3046 drw 02



LCC
TOP VIEW

3046 drw 03

9

PIN DESCRIPTION

Pin Names	Description
IN	Input
Ox	Outputs

3046 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

3046 lnk 02

NOTE:
1. This parameter is measured at characterization but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

3046 lnk 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Output and I/O terminals.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified
Commercial: T_A = 0°C to +70°C, V_{CC} = 3.3V ± 0.3V; Military: T_A = –55°C to +125°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.50	
I_{OFF}	Input Power Off Leakage[6]	V_{CC} = 0V, V_{IN} ≤ 4.5V		—	—	±1	µA
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max.,	COM'L.	—	0.1	10	µA
I_{CCH}		V_{IN} = GND or V_{CC}	MIL.	—	0.1	100	
I_{CCZ}							

3046 lnk 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limit for this parameter is ±5µA at T_A = –55°C.

9

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} -0.6V[3]		—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Input toggling 50% Duty Cycle Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—	0.31	0.45	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Input toggling 50% Duty Cycle Outputs Open fi = 50MHz	V_{IN} = V_{CC} V_{IN} = GND	—	15.5	22.8	mA
			V_{IN} = V_{CC} -0.6V V_{IN} = GND	—	15.5	22.8	

3046 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input (V_{IN} = V_{CC} -0.6V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
6. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} (fi)
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} -0.6V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   fi = Input Frequency
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3,4]

Symbol	Parameter	Conditions[1]	54/74FCT3807				54/74FCT3807A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay	50Ω to Vcc/2, CL = 10pF	1.5	3.5			1.5	3.0			ns
tR	Output Rise Time	(See figure 1)	—	1.5			—	1.5			ns
tF	Output Fall Time	or 50Ω ac	—	1.5			—	1.5			ns
tSK(o)	Output skew: skew between outputs of same package (same transition)	termination, CL = 10pF	—	0.5			—	0.35			ns
tSK(p)	Pulse skew: skew between opposite transitions of same output (|tPHL – tPLH|)	(See figure 2) f ≤ 100MHz	—	0.5			—	0.35			ns
tSK(t)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade	Outputs connected in groups of two	—	0.9			—	0.65			ns

3046 tbl 06

Symbol	Parameter	Conditions[1]	54/74FCT3807				54/74FCT3807A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay	CL = 30pF f ≤ 67MHz	1.5	4.5			1.5	4.0			ns
tR	Output Rise Time	(See figure 3)	—	1.5			—	1.5			ns
tF	Output Fall Time		—	1.5			—	1.5			ns
tSK(o)	Output skew: skew between outputs of same package (same transition)		—	0.5			—	0.35			ns
tSK(p)	Pulse skew: skew between opposite transitions of same output (|tPHL – tPLH|)		—	0.5			—	0.35			ns
tSK(t)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.0			—	0.75			ns

3046 tbl 07

Symbol	Parameter	Conditions[1]	54/74FCT3807				54/74FCT3807A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay	CL = 50pF f ≤ 40MHz	1.5	4.8			1.5	4.3			ns
tR	Output Rise Time	(See figure 4)	—	1.5			—	1.5			ns
tF	Output Fall Time		—	1.5			—	1.5			ns
tSK(o)	Output skew: skew between outputs of same package (same transition)		—	0.5			—	0.35			ns
tSK(p)	Pulse skew: skew between opposite transitions of same output (|tPHL – tPLH|)		—	0.5			—	0.35			ns
tSK(t)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.0			—	0.75			ns

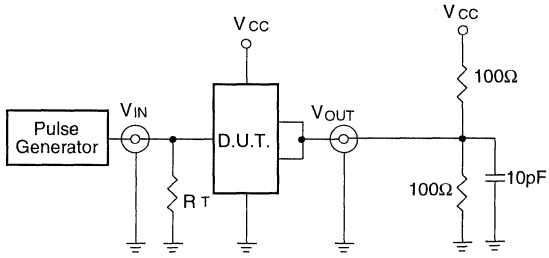
3046 tbl 08

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. tPLH, tPHL, tSK(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to Vcc, operating temperature and process parameters. These propagation delay limits do not imply skew.

9

TEST CIRCUITS

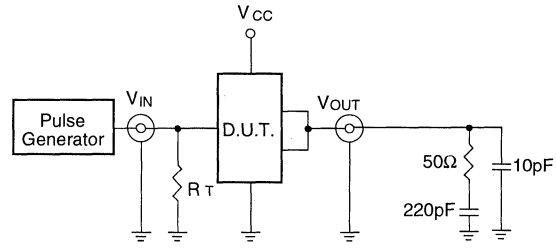
ZO = 50Ω TO VCC/2, CL = 10pF



3046 drw 04

Figure1.

ZO = 50Ω AC TERMINATION, CL = 10pF

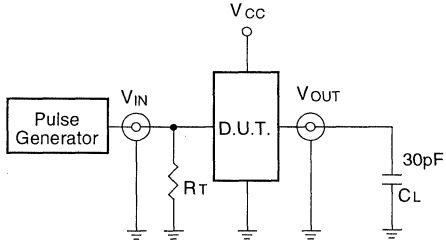


3046 drw 05

The capacitor value for ac termination is determined by the operating frequency. For very low frequencies a higher capacitor value should be selected.

Figure 2.

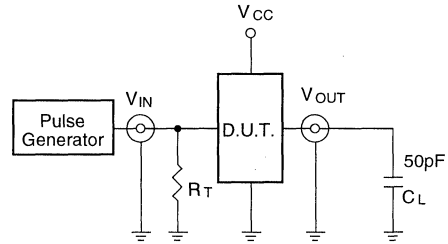
CL = 30pF CIRCUIT



3046 drw 06

Figure 3.

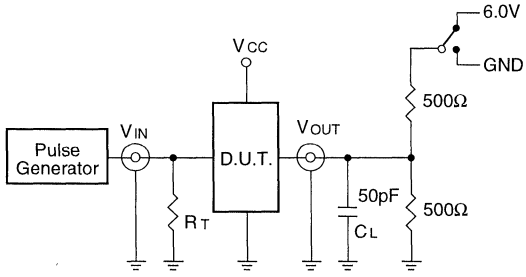
CL = 50pF CIRCUIT



3046 drw 07

Figure 4.

ENABLE AND DISABLE TIME CIRCUIT



3046 drw 08

Figure 5.

ENABLE AND DISABLE TIME SWITCH POSITION

Test	Switch
Disable LOW Enable LOW	6.0V
Disable HIGH Enable HIGH	GND

3046 lnk 09

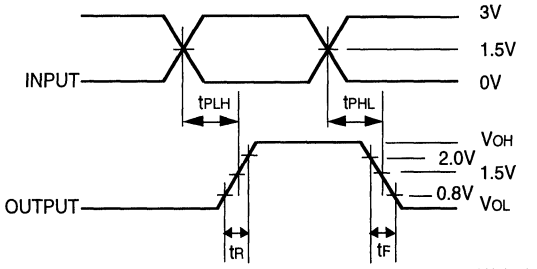
DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

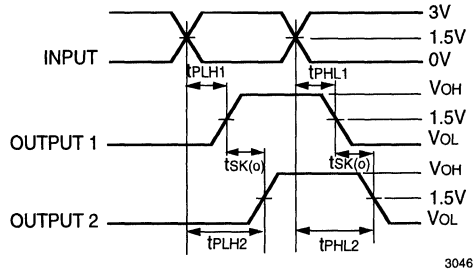
TEST WAVEFORMS

PACKAGE DELAY



3046 drw 09

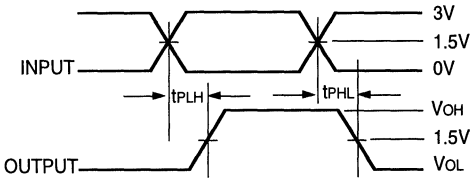
OUTPUT SKEW - tSK(o)



3046 drw 10

$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

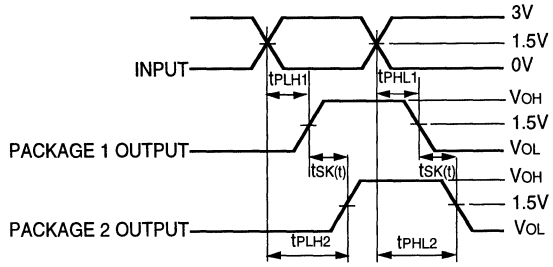
PULSE SKEW - tSK(p)



$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

3046 drw 11

PACKAGE SKEW - tSK(t)

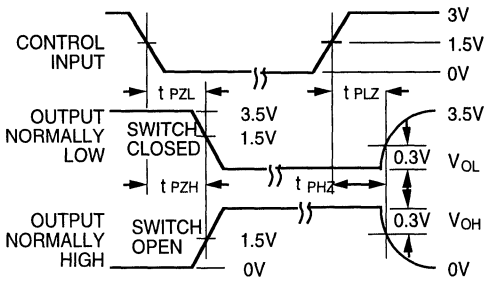


$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Package 1 and Package 2 are same device type and speed grade

3046 drw 12

ENABLE AND DISABLE TIMES

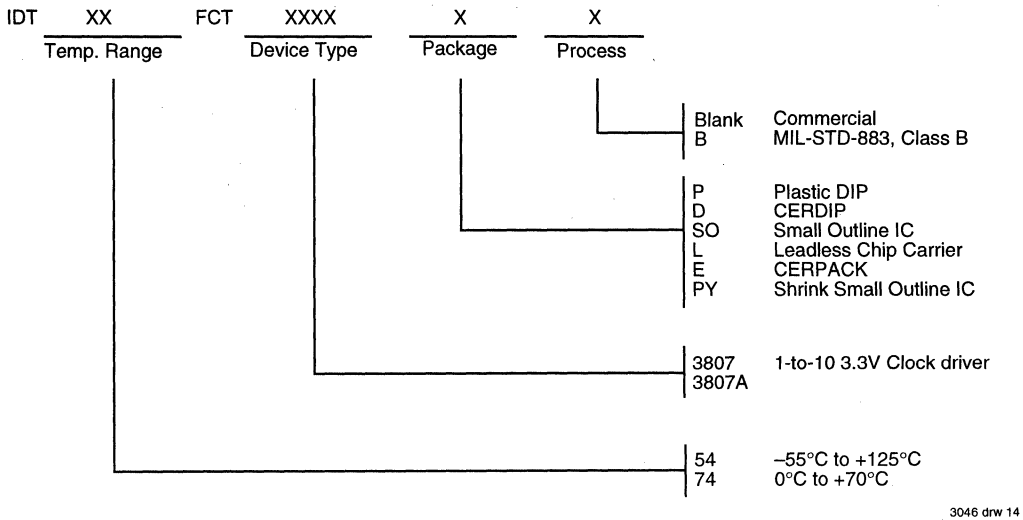


3046 drw 13

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: f ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

9

ORDERING INFORMATION



3046 drw 14

Integrated Device Technology, Inc.

LOW SKEW PLL-BASED CMOS CLOCK DRIVER (WITH 3-STATE)

IDT54/74FCT88915TT
55/70/100/133
PRELIMINARY

FEATURES:

- 0.5 MICRON CMOS Technology
- Input frequency range: 10MHz – f2Q Max. spec (FREQ_SEL = HIGH)
- Max. output frequency: 133MHz
- Pin and function compatible with MC88915T
- 5 non-inverting outputs, one inverting output, one 2x output, one ÷2 output; all outputs are TTL-compatible
- 3-State outputs
- Output skew < 500ps (max.)
- Duty cycle distortion < 500ps (max.)
- Part-to-part skew: 1ns (from tPD max. spec)
- TTL level output voltage swing
- 64/–15mA drive at TTL output voltage levels
- Available in 28 pin PLCC, LCC and SSOP packages

DESCRIPTION:

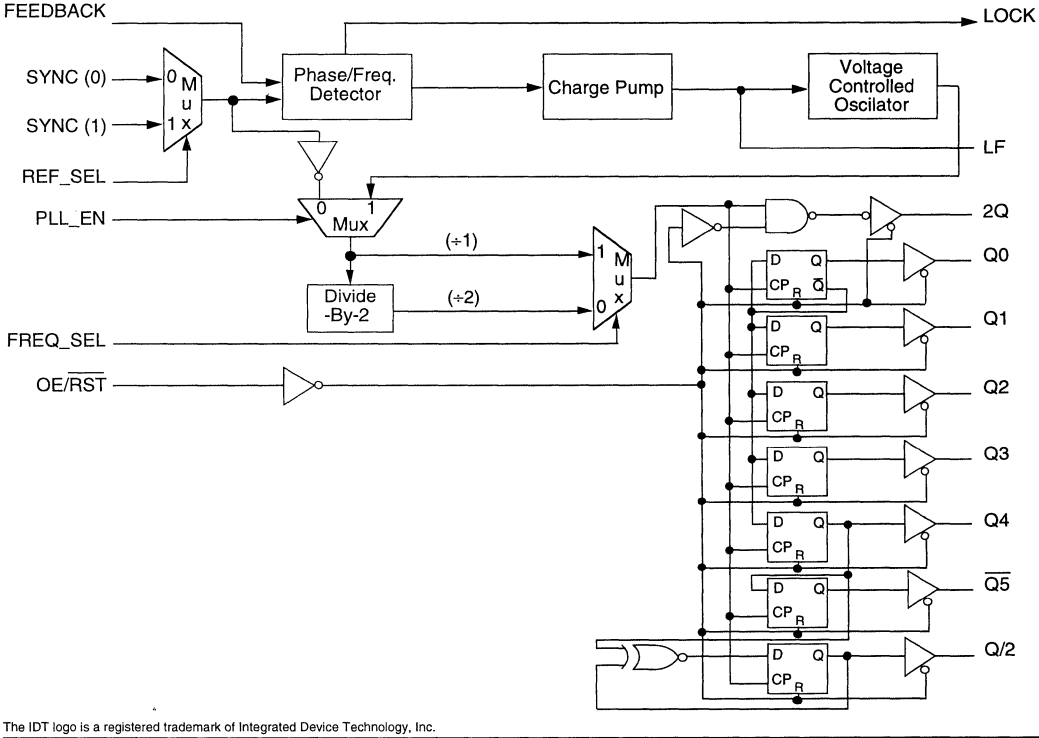
The IDT54/74FCT88915TT uses phase-lock loop technology to lock the frequency and phase of outputs to the input reference clock. It provides low skew clock distribution for high performance PCs and workstations. One of the outputs is fed back to the PLL at the FEEDBACK input resulting in essentially delay across the device. The PLL consists of the phase/frequency detector, charge pump, loop filter and VCO. The VCO is designed for a 2Q operating frequency range of 40MHz to f2Q Max.

The IDT54/74FCT88915TT provides 8 outputs with 500ps skew. The Q5 output is inverted from the Q outputs. The 2Q runs at twice the Q frequency and Q/2 runs at half the Q frequency.

The FREQ_SEL control provides an additional ÷ 2 option in the output path. PLL _EN allows bypassing of the PLL, which is useful in static test modes. When PLL_EN is low, SYNC input may be used as a test clock. In this test mode, the input frequency is not limited to the specified range and the polarity of outputs is complementary to that in normal operation (PLL_EN = 1). The LOCK output attains logic HIGH when the PLL is in steady-state phase and frequency lock. When OE/RST is low, all the outputs are put in high impedance state and registers at Q, Q and Q/2 outputs are reset.

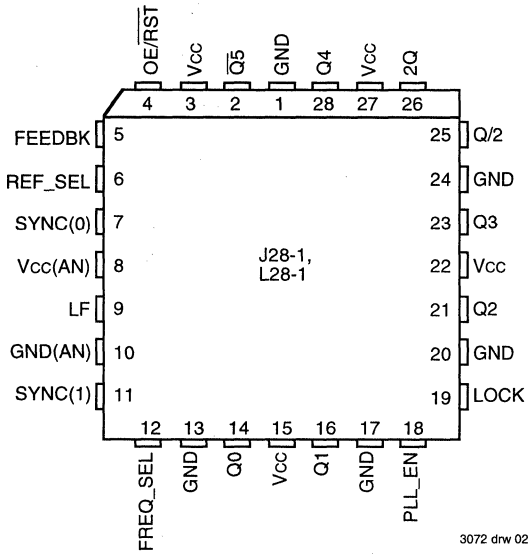
The IDT54/74FCT88915TT requires one external loop filter component as recommended in Figure 1.

FUNCTIONAL BLOCK DIAGRAM

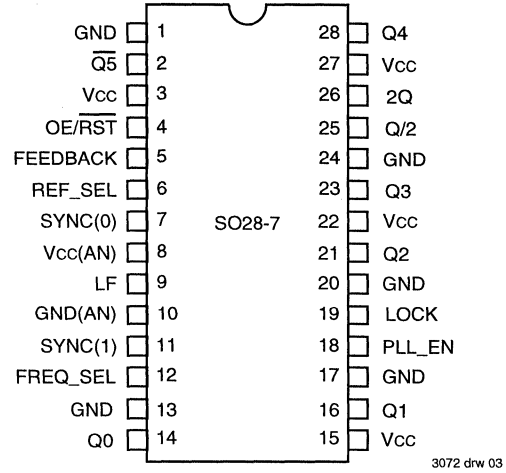


3072 drw 01

PIN CONFIGURATIONS



PLCC/LCC
TOP VIEW



SSOP
TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Description
SYNC(0)	I	Reference clock input.
SYNC(1)	I	Reference clock input.
REF_SEL	I	Chooses reference between SYNC (0) & SYNC (1). (Refer to functional block diagram).
FREQ_SEL	I	Selects between ÷1 and ÷2 frequency options. (Refer to functional block diagram).
FEEDBACK	I	Feedback input to phase detector.
LF	I	Input for external loop filter connection.
Q0-Q4	O	Clock output.
$\overline{Q5}$	O	Inverted clock output.
2Q	O	Clock output (2 x Q frequency).
Q/2	O	Clock output (Q frequency ÷ 2).
LOCK	O	Indicates phase lock has been achieved (HIGH when locked).
OE/$\overline{RST}$	I	Asynchronous reset (active LOW) and output enable (active HIGH). When HIGH, outputs are enabled. When LOW, outputs are in HIGH impedance.
PLL_EN	I	Disables phase-lock for low frequency testing. (Refer to functional block diagram).

3072 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

3072 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Input and V_{CC} terminals.
3. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

3072 lnk 03

NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Current		V_I = GND	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}			V_O = 0.5V	—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	100	—	mV
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	V
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.(3)	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC} (Test mode)		—	2.0	4.0	mA

3072 tbl 04

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Duration of the condition can not exceed one second.

9

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} –2.1V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. All Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—	0.25	0.4	mA/ MHz
C_{PD}	Power Dissipation Capacitance	50% Duty Cycle		—	15	40	pF
I_C	Total Power Supply Current[5,6]	V_{CC} = Max. PLL_EN = 1, LOCK = 1, FEEDBACK = Q/2 SYNC frequency = 20MHz. Q/2 loaded with 50pF All other outputs open		—	25	40	mA
		V_{CC} = Max. PLL_EN = 1, LOCK = 1, FEEDBACK = Q/2 SYNC frequency = 20MHz. Q/2 loaded with 50Ω Thevenin termination. All other outputs open		—	42	60	mA

3072 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. It is derived with Q frequency as the reference.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f) + I_{LOAD}$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f = 2Q frequency
   I_{LOAD} = Dynamic Current due to load.

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit
$T_{RISE/FALL}$	Rise/Fall Times, SYNC inputs (0.8V to 2.0V)	—	3.0	ns
Frequency	Input Frequency, SYNC Inputs	10[1]	2Q fmax	MHz
Duty Cycle	Input Duty Cycle, SYNC Inputs	25%	75%	—

3053 tbl 06

OUTPUT FREQUENCY SPECIFICATIONS

Symbol	Parameter	Min.	Max.[2]				Unit
			55	70	100	133	
f2Q	Operating frequency 2Q Output	40	55	70	100	133	MHz
fQ	Operating frequency Q0-Q4, Q5 Outputs	20	27.5	35	50	66.7	MHz
fQ/2	Operating frequency Q/2 Output	10	13.75	17.5	25	33.3	MHz

3072 tbl 07

NOTES:
1. Note 8 in "General AC Specification Notes" and Figure 2 describes this specification and its actual limits depending on the feedback connection.
2. Maximum operating frequency is guaranteed with the part in a phase locked condition and all outputs loaded.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	Min.	Max.	Unit
$t_{RISE/FALL}$ All outputs	Rise/Fall Time (between 0.8V and 2.0V)	Load = 50Ω to $V_{CC}/2$, C_L = 20pF	0.2[2]	1.2	ns
$t_{PULSE\ WIDTH}$ [3] All outputs[3]	Output Pulse Width Q0-Q4, Q5, Q/2, 2Q @ 1.5V		0.5t_{CYCLE} – 0.5[5]	0.5t_{CYCLE} + 0.5[5]	ns
t_{PD} SYNC-FEEDBACK[3]	SYNC input to FEEDBACK delay (measured at SYNC0 or 1 and FEEDBACK input pins)	Load = 50Ω to $V_{CC}/2$, C_L = 20pF 0.1µF from LF to Analog GND[9]	–0.5	+0.5	ns
t_{SKEWr} (rising)[3,4]	Output to Output Skew between outputs 2Q, Q0-Q4, Q/2 (rising edges only)	Load = 50Ω to $V_{CC}/2$, C_L = 20pF	—	350	ps
t_{SKEWf} (falling)[3,4]	Output to Output Skew between outputs Q0-Q4 (falling edges only)		—	350	ps
$t_{SKEWall}$ [3,4]	Output to Output Skew 2Q, Q/2, Q0-Q4 rising, Q5 falling		—	500	ps
t_{LOCK}[6]	Time required to acquire Phase-Lock from time SYNC input signal is received		1[2]	10	ms
t_{PZH} t_{PZL}	Output Enable Time OE/RST (LOW-to-HIGH) to Q, 2Q, Q/2, Q		3[2]	14	ns
t_{PHZ} t_{PLZ}	Output Disable Time OE/RST (HIGH-to-LOW) to Q, 2Q, Q/2, Q		3[2]	14	ns

3072 tbl 08

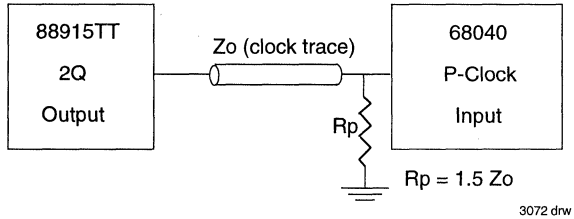
GENERAL AC SPECIFICATION NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. These specifications are guaranteed but not production tested.
4. Under equally loaded conditions, as specified under test conditions, and at a fixed temperature and voltage.
5. t_{CYCLE} = 1/frequency at which each output (Q, Q, Q/2 or 2Q) is expected to run.
6. With V_{CC} fully powered-on and an output properly connected to the FEEDBACK pin. t_{LOCK} Max. is with C1 = 0.1µF, t_{LOCK} Min. is with C1 = 0.01µF. (Where C1 is loop filter capacitor shown in Figure 1).

9

NOTES:

7. These two specs ($t_{RISE/FALL}$ and $t_{PULSE\ WIDTH}$ 2Q output) guarantee that the FCT88915TT meets 68040 P-Clock input specification.



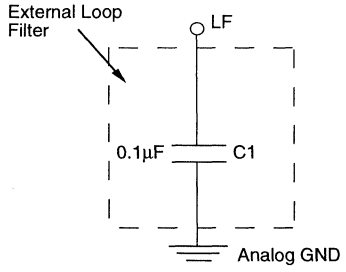
3072 drw 04

8. The wiring diagrams and written explanations of Figure 4 demonstrate the input and output frequency relationships for various possible feedback configurations. The allowable SYNC input range to stay in the phase-locked condition is also indicated. There are two allowable SYNC frequency ranges, depending on whether FREQ_SEL is HIGH or LOW. Also it is possible to feed back the Q5 output, thus creating a 180° phase shift between the SYNC input and the Q outputs. The table below summarizes the allowable SYNC frequency range for each possible configuration.

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHz)	Corresponding 2Q output Frequency Range	Phase Relationship of the Q Outputs to Rising SYNC Edge
HIGH	Q/2	10 to (2Q f_{MAX} Spec)/4	40 to (2Q f_{MAX} Spec)	0°
HIGH	Any Q (Q0-Q4)	20 to (2Q f_{MAX} Spec)/2	40 to (2Q f_{MAX} Spec)	0°
HIGH	$\overline{Q5}$	20 to (2Q f_{MAX} Spec)/2	40 to (2Q f_{MAX} Spec)	180°
HIGH	2Q	40 to (2Q f_{MAX} Spec)	40 to (2Q f_{MAX} Spec)	0°
LOW	Q/2	5 to (2Q f_{MAX} Spec)/8	20 to (2Q f_{MAX} Spec)/2	0°
LOW	Any Q (Q0-Q4)	10 to (2Q f_{MAX} Spec)/4	20 to (2Q f_{MAX} Spec)/2	0°
LOW	$\overline{Q5}$	10 to (2Q f_{MAX} Spec)/4	20 to (2Q f_{MAX} Spec)/2	180°
LOW	2Q	20 to (2Q f_{MAX} Spec)/2	20 to (2Q f_{MAX} Spec)/2	0°

3072 tbl 09

9. The tPD spec describes how the phase offset between the SYNC input and the output connected to the FEEDBACK input, varies with process, temperature and voltage. Measurements were made with a 10MHz SYNC input and Q/2 output as feedback. The phase measurements were made at 1.5V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to V_{CC} and 100Ω to ground.
tPD measurements were made with the loop filter connection shown below:



3072 drw 05

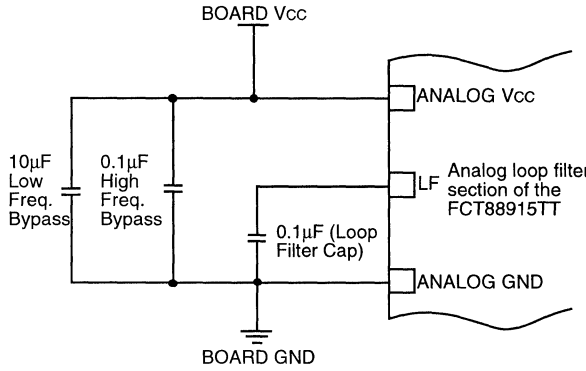


Figure 1. Recommended Loop Filter and Analog Isolation Scheme for the FCT88915TT

NOTES:

1. Figure 1 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

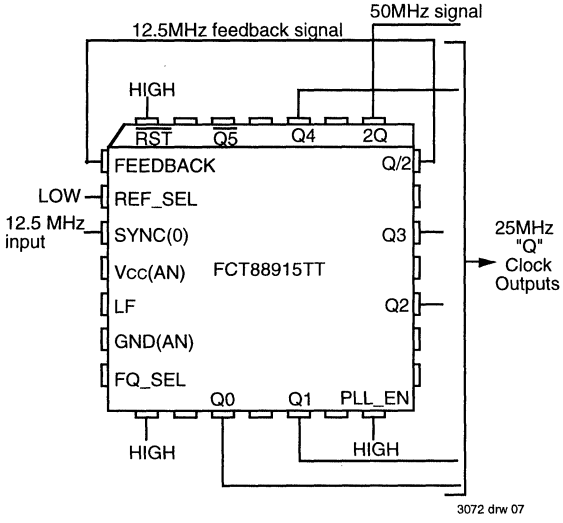
   a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the LF pin.
   b. The 10µF low frequency bypass capacitor and the 0.1µF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88915TT's sensitivity to voltage transients from the system digital Vcc supply and ground planes.
   If good bypass techniques are used on a board design near components which may cause digital Vcc and ground noise, Vcc step deviations should not occur at the 88915TT's digital Vcc supply. The purpose of the bypass filtering scheme shown in figure 1 is to give the 88915TT additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.
   c. The loop filter capacitor (0.1µF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.
2. In addition to the bypass capacitors used in the analog filter of figure 1 there should be a 0.1µF bypass capacitor between each of the other (digital) four Vcc pins and the board ground plane. This will reduce output switching noise caused by the 88915TT outputs, in addition to reducing potential for noise in the "analog" section of the chip. These bypass capacitors should also be tied as close to the 88915TT package as possible.

9

The frequency relationship shown here is applicable to all Q outputs (Q0, Q1, Q2, Q3 and Q4).

1:2 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The Q outputs (Q0-Q4, Q5) will always run at 2X the Q/2 frequency, and the 2Q output will run at 4X the Q/2 frequency.

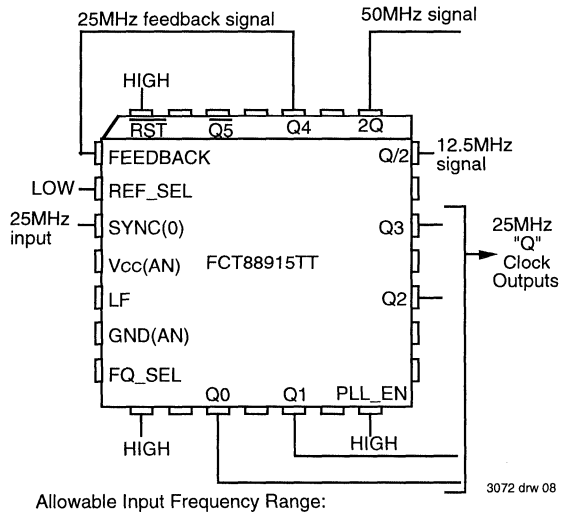


Allowable Input Frequency Range:
10MHz to (f2Q FMAX Spec /4 (for FREQ_SEL HIGH)
5MHz to (f2Q FMAX Spec /8 (for FREQ_SEL LOW)

Figure 2a. Wiring Diagram and Frequency Relationships With Q/2 Output Feedback

1:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the Q frequency, and the 2Q output will run at 2X the Q frequency.

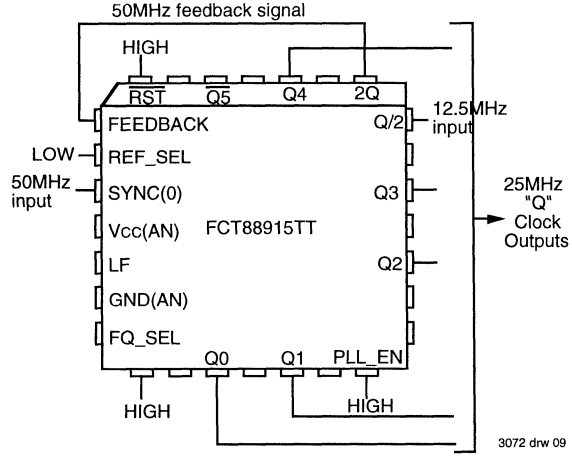


Allowable Input Frequency Range:
20MHz to (f2Q FMAX Spec)/2 (for FREQ_SEL HIGH)
10MHz to (f2Q FMAX Spec)/4 (for FREQ_SEL LOW)

Figure 2b. Wiring Diagram and Frequency Relationships With Q4 Output Feedback

2:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the 2Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2Q and SYNC, thus the 2Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2Q frequency, and the Q output will run at 1/2 the 2Q frequency.



Allowable Input Frequency Range:
40MHz to (f2Q FMAX Spec) (for FREQ_SEL HIGH)
20MHz to (f2Q FMAX Spec)/2 (for FREQ_SEL LOW)

Figure 2c. Wiring Diagram and Frequency Relationships With 2Q Output Feedback

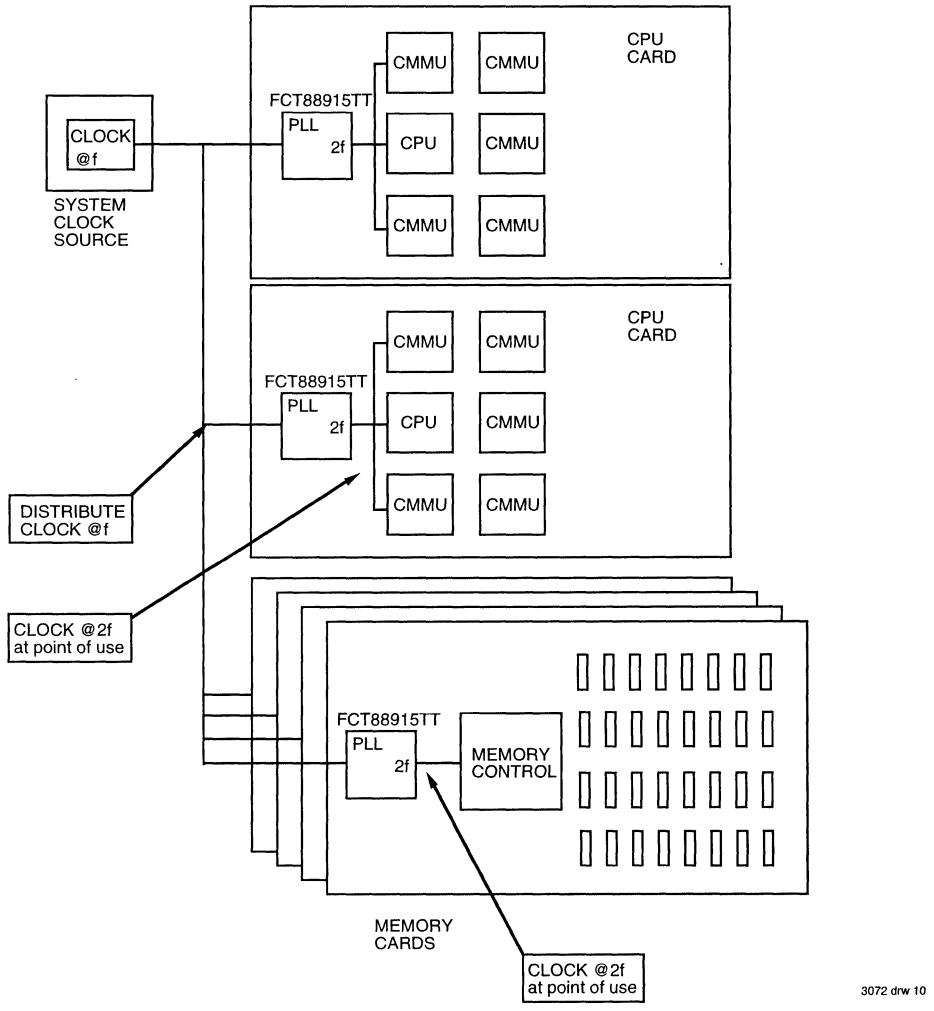


Figure 3. Multiprocessing Application Using the FCT88915TT for Frequency Multiplication and Low Board-to-Board skew

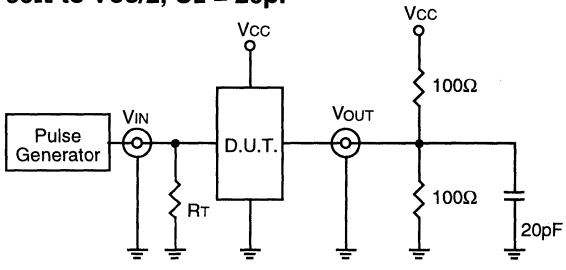
FCT88915TT System Level Testing Functionality

When the PLL_EN pin is LOW, the PLL is bypassed and the FCT88915TT is in low frequency "test mode". In test mode (with FREQ_SEL HIGH), the 2Q output is inverted from the selected SYNC input, and the Q outputs are divide-by-2 (negative edge triggered) of the SYNC input, and the Q/2 output is divide-by-4 (negative edge triggered). With FREQ_SEL LOW the 2Q output is divide-by-2 of the SYNC, the Q outputs divide-by-4, and the Q/2 output divide-by-8. These relationships can be seen in the block diagram. A recommended test configuration would be to use SYNC0 or SYNC1 as the test clock input, and tie PLL_EN and REF_SEL together and connect them to the test select logic.

This functionality is needed since most board-level testers run at 1 MHz or below, and theFCT 88915TT cannot lock onto that low of an input frequency. In the test mode described above, any test frequency test can be used.

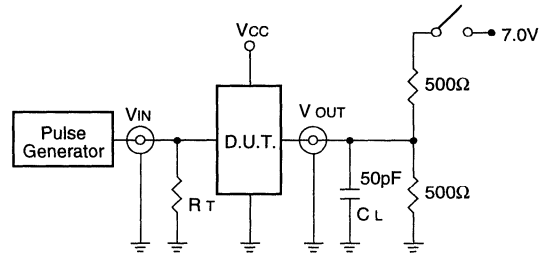
TEST CIRCUITS AND WAVEFORM

50Ω to VCC/2, CL = 20pF



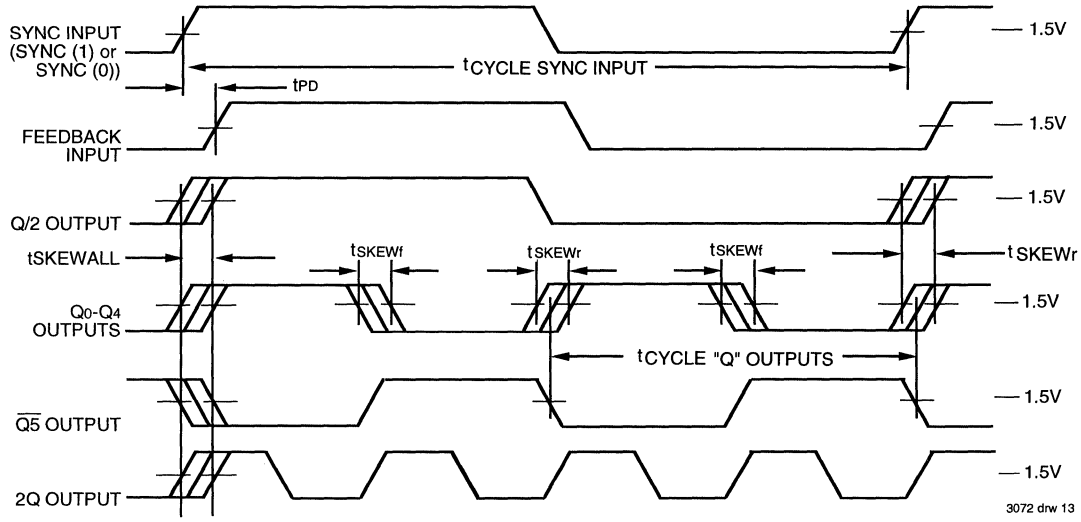
3072 drw 11

ENABLE AND DISABLE TEST CIRCUIT



3072 lnk 12

PROPAGATION DELAY, OUTPUT SKEW

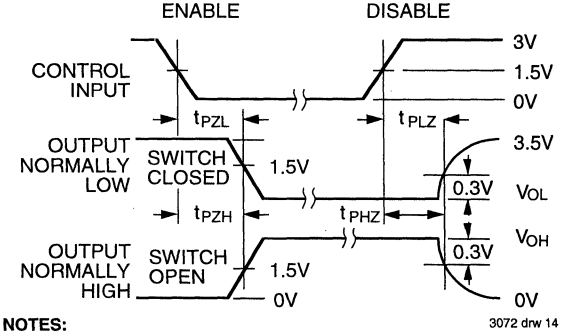


3072 drw 13

NOTES: **(These waveforms represent the hookup of Figure 2a)**

1. The FCT88915TT aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the 1.5V crossing point of the appropriate output edges. All skews are specified as "windows", not as ± deviation around a center point.
3. If a Q output is connected to the FEEDBACK input (this situation is not shown), the Q output frequency would match the SYNC input frequency, the 2Q output would run at twice the SYNC frequency and the Q/2 output would run at half the SYNC frequency.

ENABLE AND DISABLE TIMES



3072 drw 14

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: tF ≤ 2.5ns; tR ≤ 2.5ns

SWITCH POSITION

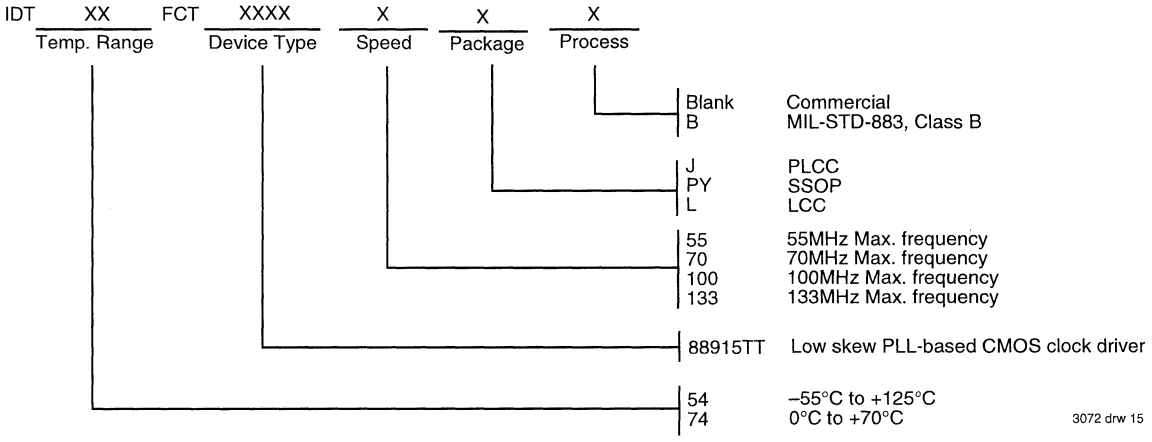
Test	Switch
Disable Low Enable Low	Closed
Disable High Enable High	Open

3072 tbl 10

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

ORDERING INFORMATION



9

Integrated Device Technology, Inc.

3.3V LOW SKEW PLL-BASED CMOS CLOCK DRIVER (WITH 3-STATE)

IDT54/74FCT388915T
70/100/133/150
PRELIMINARY

FEATURES:

- 0.5 MICRON CMOS Technology
- Input frequency range: 10MHz – f2Q Max. spec (FREQ_SEL = HIGH)
- Max. output frequency: 150MHz
- Pin and function compatible with FCT88915T, MC88915T
- 5 non-inverting outputs, one inverting output, one 2x output, one ÷2 output; all outputs are TTL-compatible
- 3-State outputs
- Output skew < 350ps (max.)
- Duty cycle distortion < 500ps (max.)
- Part-to-part skew: 1ns (from t_{PD} max. spec)
- 32/–16mA drive at CMOS output voltage levels
- V_{CC} = 3.3V ± 0.3V
- Inputs can be driven by 3.3V or 5V components
- Available in 28 pin PLCC, LCC and SSOP packages

DESCRIPTION:

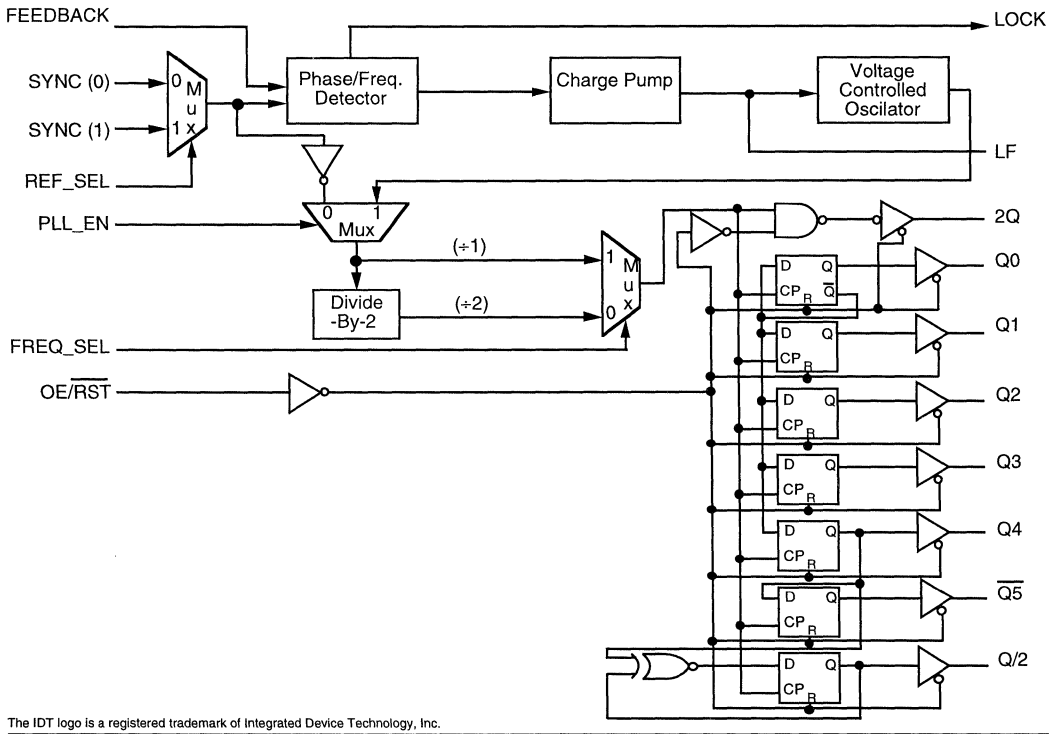
The IDT54/74FCT388915T uses phase-lock loop technology to lock the frequency and phase of outputs to the input reference clock. It provides low skew clock distribution for high performance PCs and workstations. One of the outputs is fed back to the PLL at the FEEDBACK input resulting in essentially zero delay across the device. The PLL consists of the phase/frequency detector, charge pump, loop filter and VCO. The VCO is designed for a 2Q operating frequency range of 40MHz to f2Q Max.

The IDT54/74FCT388915T provides 8 outputs with 350ps skew. The $\overline{Q5}$ output is inverted from the Q outputs. The 2Q runs at twice the Q frequency and Q/2 runs at half the Q frequency.

The FREQ_SEL control provides an additional ÷ 2 option in the output path. PLL _EN allows bypassing of the PLL, which is useful in static test modes. When PLL_EN is low, SYNC input may be used as a test clock. In this test mode, the input frequency is not limited to the specified range and the polarity of outputs is complementary to that in normal operation (PLL_EN = 1). The LOCK output attains logic HIGH when the PLL is in steady-state phase and frequency lock. When OE/$\overline{RST}$ is low, all the outputs are put in high impedance state and registers at Q, $\overline{Q}$ and Q/2 outputs are reset.

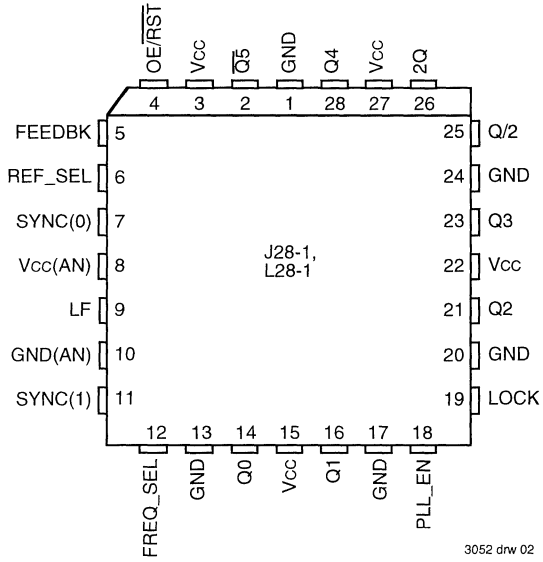
The IDT54/74FCT388915T requires one external loop filter component as recommended in Figure 3.

FUNCTIONAL BLOCK DIAGRAM



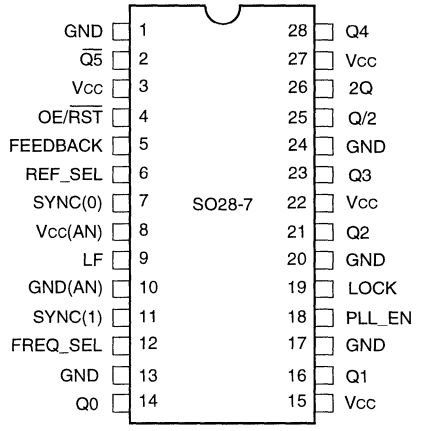
3052 drw 01

PIN CONFIGURATIONS



3052 drw 02

PLCC/LCC
TOP VIEW



SSOP
TOP VIEW

3052 drw 03

PIN DESCRIPTION

Pin Name	I/O	Description
SYNC(0)	I	Reference clock input.
SYNC(1)	I	Reference clock input.
REF_SEL	I	Chooses reference between SYNC (0) & SYNC (1). (Refer to functional block diagram).
FREQ_SEL	I	Selects between ÷ 1 and ÷ 2 frequency options. (Refer to functional block diagram).
FEEDBACK	I	Feedback input to phase detector.
LF	I	Input for external loop filter connection.
Q0-Q4	O	Clock output.
$\overline{Q5}$	O	Inverted clock output.
2Q	O	Clock output (2 x Q frequency).
Q/2	O	Clock output (Q frequency ÷ 2).
LOCK	O	Indicates phase lock has been achieved (HIGH when locked).
OE/$\overline{RST}$	I	Asynchronous reset (active LOW) and output enable (active HIGH). When HIGH, outputs are enabled. When LOW, outputs are in HIGH impedance.
PLL_EN	I	Disables phase-lock for low frequency testing. (Refer to functional block diagram).

3052 tbl 01

9

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

NOTES: 3052 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

NOTE: 3052 lnk 03

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to 70°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	5.5	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
I_{IL}	Input LOW Current		V_I = GND	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output Pins)		V_O = GND	—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V(3)		–36	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Max., V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V(3)		50	—	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –16mA	2.4(5)	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 32mA	—	0.3	0.5	V
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC} (Test mode)		—	2.0	4.0	mA

NOTES: 3052 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} –2.1V[3]	V_{IN} = V_{CC} –0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. All Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—	0.2	0.3	mA/ MHz
C_{PD}	Power Dissipation Capacitance	50% Duty Cycle		—	15	25	pF
I_C	Total Power Supply Current[6]	V_{CC} = Max. PLL_EN = 1, LOCK = 1, FEEDBACK = Q4 SYNC frequency = 50MHz. All bits loaded with 15pF		—	30	60	mA
		V_{CC} = Max. PLL_EN = 1, LOCK = 1, FEEDBACK = Q4 SYNC frequency = 50MHz. All bits loaded with 50Ω Thevenin termination and 20pF		—	90	120	mA

3052 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input. All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. It is derived with Q frequency as the reference.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f) + I_{LOAD}$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f =2Q Frequency
   I_{LOAD} = Dynamic Current due to load.

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit
$T_{RISE/FALL}$	Rise/Fall Times, SYNC inputs (0.8V to 2.0V)	—	3.0	ns
Frequency	Input Frequency, SYNC Inputs	10.0[1]	2Q fmax	MHz
Duty Cycle	Input Duty Cycle, SYNC Inputs	25%	75%	—

3052 tbl 06

OUTPUT FREQUENCY SPECIFICATIONS

Symbol	Parameter	Min.	Max. [2]				Unit
			70	100	133	150	
f2Q	Operating frequency 2Q Output	40	70	100	133	150	MHz
fQ	Operating frequency Q0-Q4, $\overline{Q5}$ Outputs	20	35	50	66.7	75	MHz
fQ/2	Operating frequency Q/2 Output	10	17.5	25	33.3	37.5	MHz

3052 tbl 07

NOTES:
1. Note 7 in "General AC Specification Notes" and Figure 3 describes this specification and its actual limits depending on the feedback connection.
2. Maximum operating frequency is guaranteed with the part in a phase locked condition and all outputs loaded.

9

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	Min.*	Max.*	Unit
$t_{RISE/FALL}$ All Outputs	Rise/Fall Time (between 0.8V and 2.0V)	Load = 50Ω to $V_{CC}/2$, C_L = 20pF	0.2[2]	1.5	ns
$t_{PULSE\ WIDTH}$[3] Q, $\overline{Q}$, Q/2 outputs[3]	Output Pulse Width Q0-Q4, $\overline{Q5}$, Q/2, @ 1.5V	Load = 50Ω to $V_{CC}/2$, C_L = 20pF	$0.5t_{CYCLE} - 0.5$[5]	$0.5t_{CYCLE} + 0.5$[5]	ns
$t_{PULSE\ WIDTH}$ 2Q Output[3]	Output Pulse Width 2Q @ 1.5V		$0.5t_{CYCLE} - 0.7$[5]	$0.5t_{CYCLE} + 0.7$[5]	ns
t_{PD} SYNC-FEEDBACK[3]	SYNC input to FEEDBACK delay (measured at SYNC0 or 1 and FEEDBACK input pins)	Load = 50Ω to $V_{CC}/2$, C_L = 20pF 0.1µF from LF to Analog GND[5]	–0.5	+0.5	ns
t_{SKEWr} (rising)[3,4]	Output to Output Skew between outputs 2Q, Q0-Q4, Q/2 (rising edges only)	Load = 50Ω to $V_{CC}/2$, C_L = 20pF	—	250	ps
t_{SKEWf} (falling)[3,4]	Output to Output Skew between outputs Q0-Q4 (falling edges only)		—	250	ps
$t_{SKEWall}$ [3,4]	Output to Output Skew 2Q, Q/2, Q0-Q4 rising, $\overline{Q5}$ falling		—	350	ps
t_{LOCK}[6]	Time required to acquire Phase-Lock from time SYNC input signal is received		1[2]	10	ms
t_{PZH} t_{PZL}	Output Enable Time OE/$\overline{RST}$ (LOW-to-HIGH) to Q, 2Q, Q/2, $\overline{Q}$		3[2]	14	ns
t_{PHZ} t_{PLZ}	Output Disable Time OE/$\overline{RST}$ (HIGH-to-LOW) to Q, 2Q, Q/2, $\overline{Q}$		3[2]	14	ns

3052 tbl 08

GENERAL AC SPECIFICATION NOTES:

* PRELIMINARY.

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. These specifications are guaranteed but not production tested.
4. Under equally loaded conditions, as specified under test conditions and at a fixed temperature and voltage.
5. t_{CYCLE} = 1/frequency at which each output (Q, $\overline{Q}$, Q/2 or 2Q) is expected to run.
6. With V_{CC} fully powered-on and an output properly connected to the FEEDBACK pin. t_{LOCK} Max. is with C1 = 0.1µF, t_{LOCK} Min. is with C1 = 0.01µF. (Where C1 is loop filter capacitor shown in Figure 2).

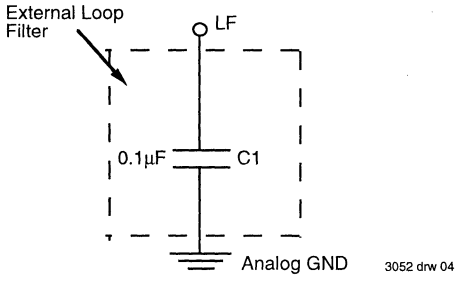
NOTES:

7. The wiring diagrams and written explanations of Figure 3 demonstrate the input and output frequency relationships for various possible feedback configurations. The allowable SYNC input range to stay in the phase-locked condition is also indicated. There are two allowable SYNC frequency ranges, depending on whether FREQ_SEL is HIGH or LOW. Also it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the Q outputs. The table below summarizes the allowable SYNC frequency range for each possible configuration.

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHz)	Corresponding 2Q Output Frequency Range	Phase Relationship of the Q Outputs to Rising SYNC Edge
HIGH	Q/2	10 to (2x _Q f_{MAX} Spec)/4	40 to (2Q f_{MAX} Spec)	0°
HIGH	Any Q (Q0-Q4)	20 to (2x_Q f_{MAX} Spec)/2	40 to (2Q f_{MAX} Spec)	0°
HIGH	$\overline{Q5}$	20 to (2x_Q f_{MAX} Spec)/2	40 to (2Q f_{MAX} Spec)	180°
HIGH	2X_Q	40 to (2x_Q f_{MAX} Spec)	40 to (2Q f_{MAX} Spec)	0°
LOW	Q/2	5 to (2x_Q f_{MAX} Spec)/8	20 to (2Q f_{MAX} Spec)/2	0°
LOW	Any Q (Q0-Q4)	10 to (2x_Q f_{MAX} Spec)/4	20 to (2Q f_{MAX} Spec)/2	0°
LOW	$\overline{Q5}$	10 to (2x_Q f_{MAX} Spec)/4	20 to (2Q f_{MAX} Spec)/2	180°
LOW	2X_Q	20 to (2x_Q f_{MAX} Spec)/2	20 to (2Q f_{MAX} Spec)/2	0°

3052 tbl 09

8. The tPD spec describes how the phase offset between the SYNC input and the output connected to the FEEDBACK input, varies with process, temperature and voltage. Measurements were made with a 10MHz SYNC input and Q/2 output as feedback. The phase measurements were made at 1.5V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to VCC and 100Ω to ground. tPD measurements were made with the loop filter connection shown below:



3052 drw 04

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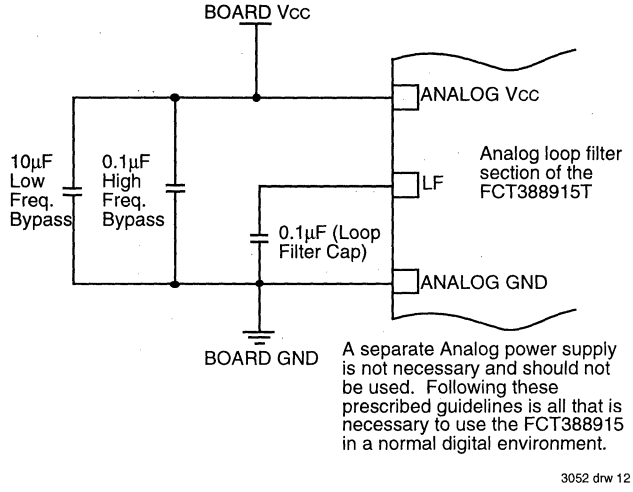


Figure 2. Recommended Loop Filter and Analog Isolation Scheme for the FCT388915T

NOTES:

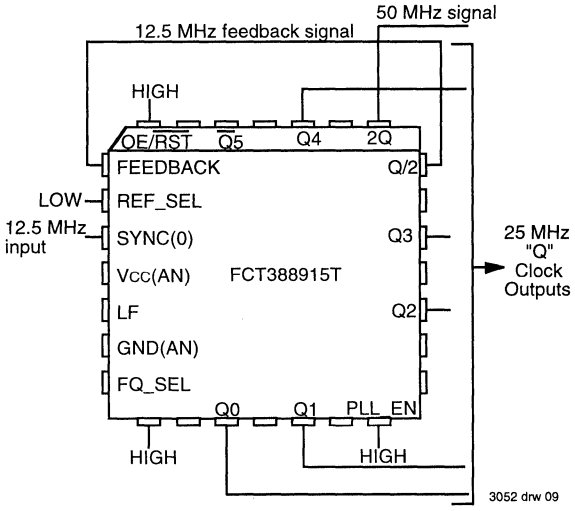
1. Figure 2 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:

   a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the LF pin.
   b. The 10µF low frequency bypass capacitor and the 0.1µF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 388915T's sensitivity to voltage transients from the system digital Vcc supply and ground planes.
   If good bypass techniques are used on a board design near components which may cause digital Vcc and ground noise, Vcc step deviations should not occur at the 388915T's digital Vcc supply. The purpose of the bypass filtering scheme shown in figure 2 is to give the 388915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.
   c. The loop filter capacitor (0.1µF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.
2. In addition to the bypass capacitors used in the analog filter of figure 2 there should be a 0.1µF bypass capacitor between each of the other (digital) four Vcc pins and the board ground plane. This will reduce output switching noise caused by the 388915T outputs, in addition to reducing potential for noise in the "analog" section of the chip. These bypass capacitors should also be tied as close to the 388915T package as possible.

The frequency relationship shown here is applicable to all Q outputs (Q0, Q1, Q2, Q3 and Q4).

1:2 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The Q outputs (Q0-Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2Q output will run at 4X the Q/2 frequency.

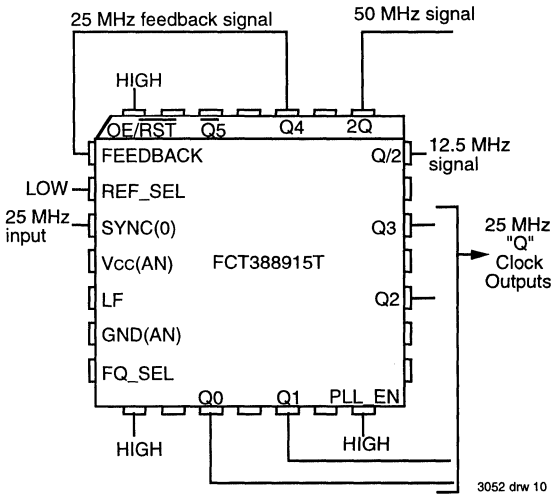


Allowable Input Frequency Range:
10MHz to (f2Q MAX Spec)/4 (for FREQ_SEL HIGH)
5MHz to (f2Q MAX Spec)/8 (for FREQ_SEL LOW)

Figure 3a. Wiring Diagram and Frequency Relationships With Q/2 Output Feedback

1:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the Q frequency, and the 2Q output will run at 2X the Q frequency.

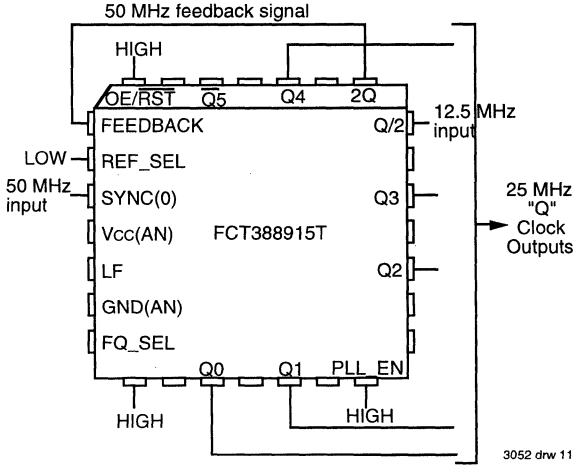


Allowable Input Frequency Range:
20MHz to (f2Q MAX Spec)/2 (for FREQ_SEL HIGH)
10MHz to (f2Q MAX Spec)/4 (for FREQ_SEL LOW)

Figure 3b. Wiring Diagram and Frequency Relationships With Q4 Output Feedback

2:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the 2Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2Q and SYNC, thus the 2Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2Q frequency, and the Q output will run at 1/2 the 2Q frequency.



Allowable Input Frequency Range:
40MHz to (f2Q MAX Spec) (for FREQ_SEL HIGH)
20MHz to (f2Q MAX Spec)/2 (for FREQ_SEL LOW)

Figure 3c. Wiring Diagram and Frequency Relationships With 2Q Output Feedback

9

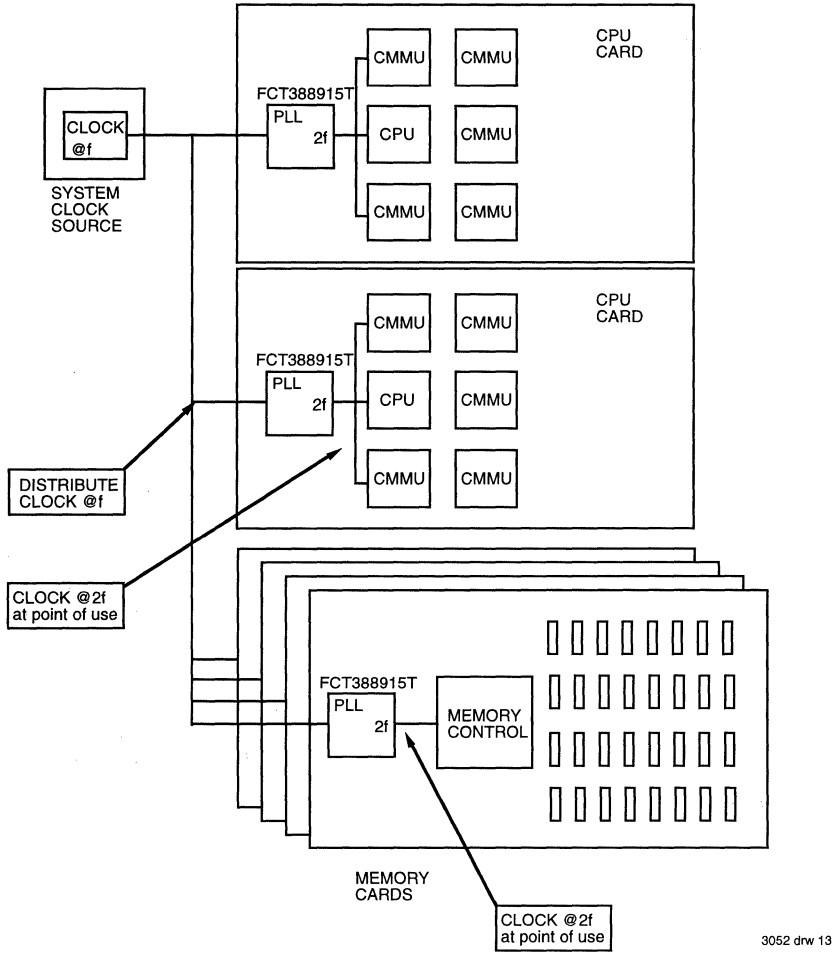


Figure 4. Multiprocessing Application Using the FCT388915T for Frequency Multiplication and Low Board-to-Board skew

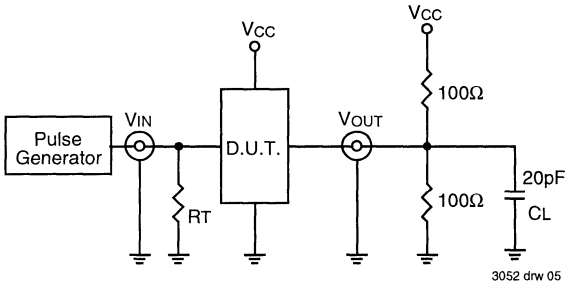
FCT388915T System Level Testing Functionality

When the PLL_EN pin is LOW, the PLL is bypassed and the FCT388915T is in low frequency "test mode". In test mode (with FREQ_SEL HIGH), the 2Q output is inverted from the selected SYNC input, and the Q outputs are divide-by-2 (negative edge triggered) of the SYNC input, and the Q/2 output is divide-by-4 (negative edge triggered). With FREQ_SEL LOW the 2Q output is divide-by-2 of the SYNC, the Q outputs divide-by-4, and the Q/2 output divide-by-8. These relationships can be seen in the block diagram. A recommended test configuration would be to use SYNC0 or SYNC1 as the test clock input, and tie PLL_EN and REF_SEL together and connect them to the test select logic.

This functionality is needed since most board-level testers run at 1 MHz or below, and theFCT 388915T cannot lock onto that low of an input frequency. In the test mode described above, any test frequency test can be used.

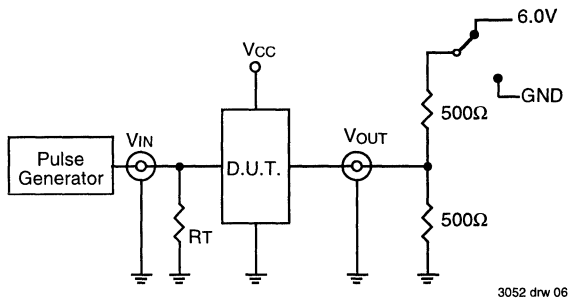
TEST CIRCUITS AND WAVEFORMS

50Ω TO VCC/2, CL = 20PF



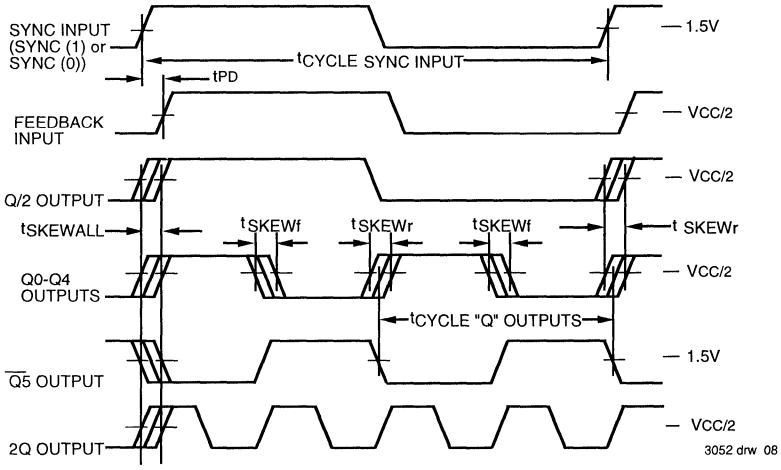
3052 drw 05

ENABLE AND DISABLE TEST CIRCUIT



3052 drw 06

PROPAGATION DELAY, OUTPUT SKEW



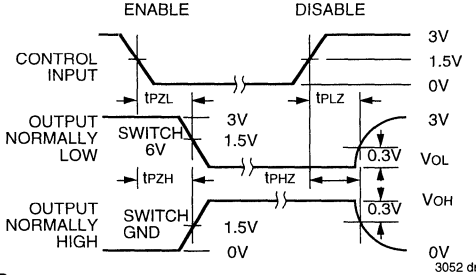
3052 drw 08

(These waveforms represent the configuration of Figure 3a)

NOTES:

1. The FCT388915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the VCC/2 crossing point of the appropriate output edges. All skews are specified as "windows", not as ± deviation around a center point.
3. If a Q ouput is connected to the FEEDBACK input (this situation is not shown), the Q output frequency would match the SYNC input frequency, the 2Q output would run at twice the SYNC frequency and the Q/2 output would run at half the SYNC frequency.

ENABLE AND DISABLE TIMES



3052 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: tF ≤ 2.5ns; tR ≤ 2.5ns

SWITCH POSITION

Test	Switch
Disable Low Enable Low	6V
Disable High Enable High	GND

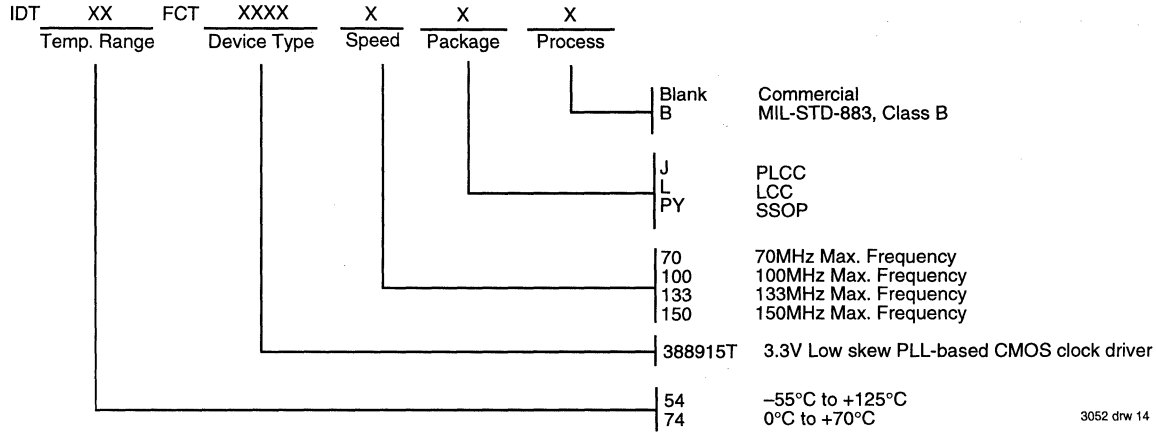
3052 tbl 10

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

9

ORDERING INFORMATION



3052 drw 14

Integrated Device Technology, Inc.

3.3V LOW SKEW PLL-BASED CMOS CLOCK DRIVER

IDT74FCT3932
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew
- 16 programmable frequency configurations
- 17 3-state outputs
- Output configuration:
  - BANK1: 4 outputs
  - BANK2: 8 outputs
  - BANK3: 5 outputs
- Dedicated feedback output (Q_FB)
- Maximum output frequency: 100MHz
- V_{CC} = 3.3V ±0.3V
- Inputs can be driven from 3.3V or 5V components
- Available in 48 SSOP, TSSOP packages
- Suited to SDRAM applications

DESCRIPTION:

The FCT3932 uses phase-lock loop technology to lock the frequency and phase of the feedback to the input reference clock. It provides a large number of low skew outputs that are configurable in 16 different modes using the CNTRL 1-4 inputs. A dedicated output, Q_FB, is provided to supply the PLL feedback and it should be connected to the FEEDBACK input. Q_FB is located adjacent to FEEDBACK to minimize the delay in the feedback path. In order to offset any delay in the output path from the FCT3932 output to a receiving device, feedback path delay should be made to match this output path delay.

The PLL consists of the phase/frequency detector, charge pump, loop filter and VCO. The FCT3932 requires no external loop filter components.

The FCT3932 provides 17 outputs grouped in 3 banks with individual 3-state control and an additional dedicated feedback output with no disable. Connecting Q_FB to FEEDBACK ensures uninterrupted PLL operation when all outputs are disabled.

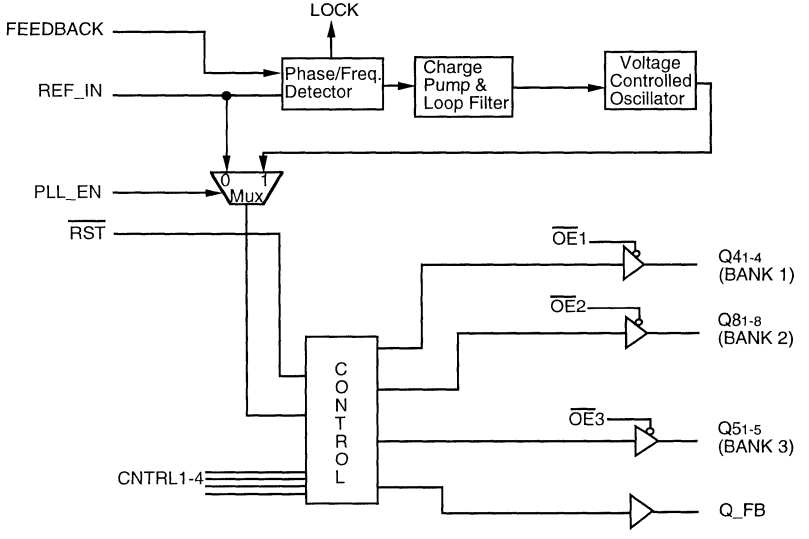
Individual bank 3-state allows users to disable unused outputs in order to limit power dissipation or minimize switching noise. It also allows users to shut down outputs in low power modes while maintaining phase lock.

The FCT3932 provides a LOCK pin that goes high when the device is phase-locked.

The user can bypass the PLL for testability purposes by deasserting PLL_EN. In this "test" mode, the input frequency is not limited to the specified range.

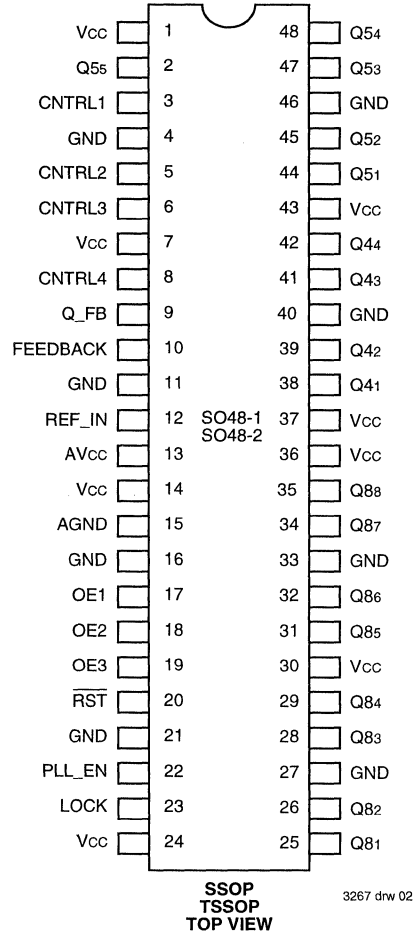
The FCT3932 provides an asynchronous reset input, $\overline{RST}$, which resets all outputs. This initializes all internal registers so that outputs start up in a known state.

FUNCTIONAL BLOCK DIAGRAM



3267 drw 01

PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

3267 drw 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to 70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–60 to +60	mA

3267 tbl 01

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.2	5.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.7	6.0	pF

3267 lnk 02

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Name	I/O	Description
REF_IN	I	Reference clock input.
FEEDBACK	I	Feedback input to phase detector.
$Q4_{1-4}$	O	BANK1 clock outputs.
$Q8_{1-8}$	O	BANK2 clock outputs.
$Q5_{1-5}$	O	BANK3 clock outputs.
$\overline{OE}1-3$	I	Output enable controls for BANKS 1, 2 and 3 (Active LOW).
CNTRL1-4	I	Control lines to select output configuration (see table).
Q_FB	O	Dedicated PLL feedback output.
$\overline{RST}$	I	Asynchronous reset (Active LOW).
PLL_EN	I	Disables phase-lock for low frequency testing (Refer to functional block diagram).
LOCK	O	PLL "LOCK" indicator (HIGH when PLL is locked).

3267 tbl 03

OUTPUT FREQUENCY CONFIGURATION AND INPUT FREQUENCY RANGE TABLE

MODE	CNTRL 4 3 2 1	Q_FEEDBACK	Q_BANK1 (4 outputs)	Q_BANK2 (8 outputs)	Q_BANK3 (5 outputs)	FIN Range
0	0 0 0 0	F (divide-by-1)	$\overline{F}$	F	F	50-100MHz
1	0 0 0 1	F (divide-by-1)	$\overline{F}$	F	F/2	50-100MHz
2	0 0 1 0	F (divide-by-1)	F	F	F	50-100MHz
3	0 0 1 1	F (divide-by-1)	F	F/2	F/2	50-100MHz
4	0 1 0 0	F (divide-by-1)	F	F/3	F	50-100MHz
5	0 1 0 1	F (divide-by-3)	3F	3F	F	16.7-33.3MHz
6	0 1 1 0	F (divide-by-3)	3F	F	3F	16.7-33.3MHz
7	0 1 1 1	F (divide-by-3)	3F	3F	3F	16.7-33.3MHz
8	1 0 0 0	F (divide-by-2)	2F	2F	2F	25-50MHz
9	1 0 0 1	F (divide-by-2)	2F	F	2F	25-50MHz
10	1 0 1 0	F (divide-by-2)	2F	F	F	25-50MHz
11	1 0 1 1	F (divide-by-2)	2F	F	F/2	25-50MHz
12	1 1 0 0	F (divide-by-2)	2F	F/2	F	25-50MHz
13	1 1 0 1	F (divide-by-4)	4F	2F	4F	12.5-25MHz
14	1 1 1 0	F (divide-by-4)	4F	2F	2F	12.5-25MHz
15	1 1 1 1	F (divide-by-4)	4F	2F	F	12.5-25MHz

3267 tbl 04

9

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–75		mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	75		mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.	2.4[4]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	—	—	0.2	V
			I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	—	4	mA

3267 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. V_{OH} = V_{CC} –0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} –0.6V[3]	—	2.0	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. All Outputs Open	V_{IN} = V_{CC} V_{IN} = GND	—			µA/MHz
C_{PD}	Power Dissipation Capacitance	50% Duty Cycle		—			pF
I_C	Total Power Supply Current[5,6]	V_{CC} = Max. PLL_EN = 1, LOCK = 1, MODE 2 REF_IN frequency = 50MHz. 1 bit loaded with 50Ω Thevenin termination. All other outputs open		—			mA

3267 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. It is derived with Q frequency as the reference.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f) + I_{LOAD}$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f = SYNC input frequency
   I_{LOAD} = Dynamic Current due to load.

9

INPUT TIMING REQUIREMENTS

Symbol	Parameter		Min.	Max.	Unit
$t_{RISE/FALL}$	Rise/Fall Times REF_IN input (0.8V to 2.0V)		—	3.0	ns
Frequency	Input Frequency REF_IN input	Modes 0, 1, 2, 3, 4	50	100	MHz
		Modes 5, 6, 7	16.7	33.3	
		Modes 8, 9, 10, 11, 12	25	50	
		Modes 13, 14, 15	12.5	25	
Duty Cycle	Input Duty Cycle, REF_IN input		25	75	%

3267 tbl 07

OUTPUT FREQUENCY SPECIFICATIONS

Mode	Parameter		Min.	Max. 100	Unit
0, 1, 2, 3,4	Operating frequency	F, $\overline{F}$ Outputs	50	100	MHz
		F/2 Outputs	25	50	
		F/3 Outputs	16.7	33.3	
5, 6, 7	Operating frequency	3F Outputs	50	100	
		F Outputs	16.7	33.3	
8, 9, 10, 11, 12	Operating frequency	2F Outputs	50	100	
		F Outputs	25	50	
		F/2 Outputs	12.5	25	
13, 14, 15	Operating frequency	4F Outputs	50	100	
		2F Outputs	25	50	
		F Outputs	12.5	25	

3267 tbl 08

SWITCHING CHARACTERISTICS OVER OPERATING RANGE[7]

Symbol	Parameter	Condition[1]	Min.[2]	Max.	Unit
$t_{RISE/FALL}$ All Outputs	Rise/Fall Time (between 0.8 and 2.0V)	Load = 50Ω to 1.5V, C_L = 20pF	0.5	1.5	ns
t_{PW} [3]	Output Pulse Width		45	55	%
t_{PD}[3] REF_IN-Q	Propagation Delay (REF_IN input to Q outputs)	Load = 50Ω to 1.5V, C_L = 20pF	–0.5	+0.5	ns
t_{SKEWr}[3,4]	Output to Output Skew (All outputs at same frequency rising edge)	Load = 50Ω to 1.5V, C_L = 20pF	—	500	ps
t_{SKEWf}[3,4]	Output to Output Skew (All outputs at same frequency falling edge)		—	500	ps
$t_{SKEWall}$[3,4]	Output to Output Skew (All outputs, rising edge any frequency)		—	1.0	ns
t_{LOCK}[5]	Time required to acquire Phase-Lock from time REF_IN input signal is received		1	10	ms
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$x (LOW-to-HIGH) to Q		3.0	8.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$x (HIGH-to-LOW) to Q		3.0	8.0	ns

3267 tbl 09

GENERAL AC SPECIFICATION NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.
3. These specifications are guaranteed but not production tested.
4. Under equally loaded conditions, as specified under test conditions and at a fixed temperature and voltage.
5. With Vcc fully powered-on and Q_FB properly connected to the FEEDBACK pin.
6. The tPD spec gives the limits of the phase offset between the REF_IN input and the Q_FB output.
7. The AC specifications are only guaranteed with the decoupling scheme shown in figure 2.

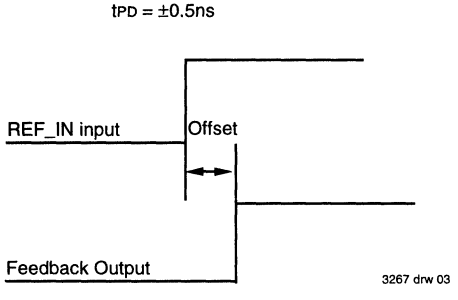


Figure 1.

9

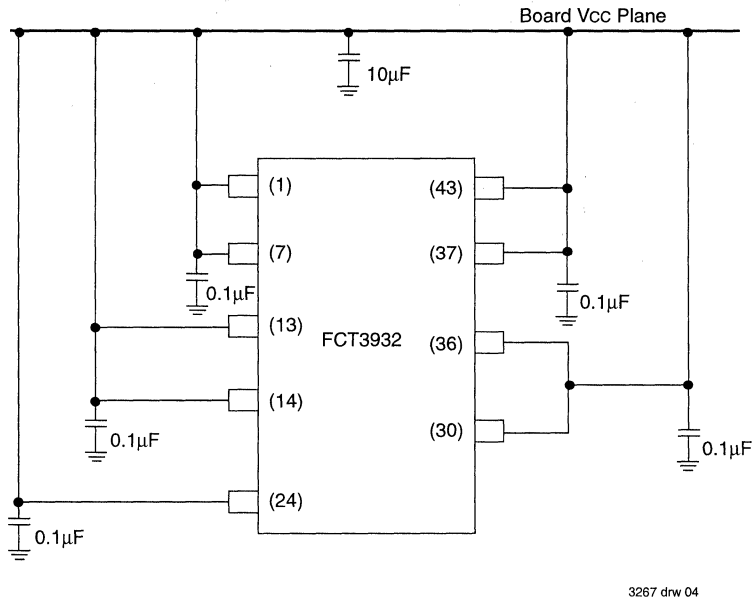


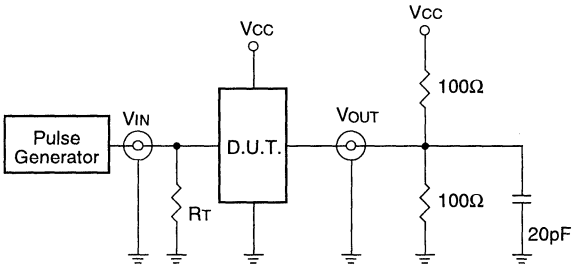
Figure 2. Recommended Decoupling for the FCT3932

NOTES:

1. Figure 2 shows a decoupling scheme which will be effective in most FCT3932 applications. The following guidelines should be followed for stable, jitter-free operation:
   a. All decoupling capacitors should be connected as close to the package as possible. (Preferably at the device pins).
   b. The 10µF and 0.1µF bypass capacitors provide protection from power supply and ground plane transients.

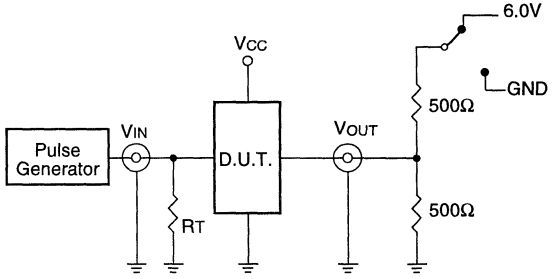
TEST CIRCUITS AND WAVEFORMS

50Ω TO Vcc/2, CL = 20pF



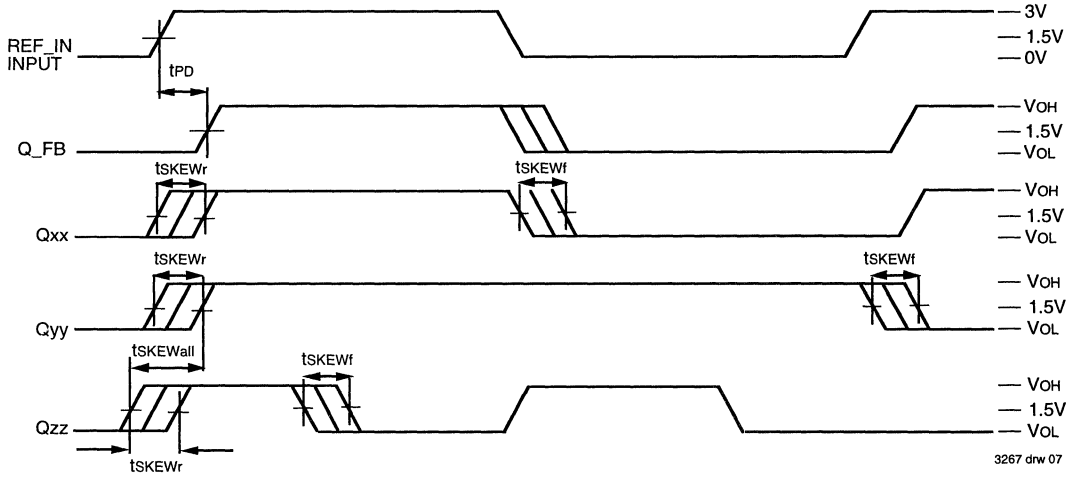
3267 drw 05

ENABLE/DISABLE TEST CIRCUIT



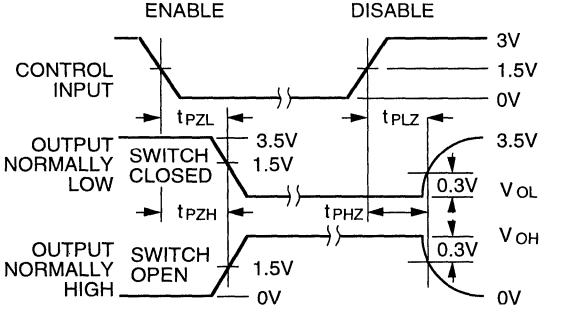
3267 drw 06

PROPAGATION DELAY, OUTPUT SKEW



3267 drw 07

ENABLE AND DISABLE TIMES



3267 drw 08

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: tF ≤ 2.5ns; tR ≤ 2.5ns

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

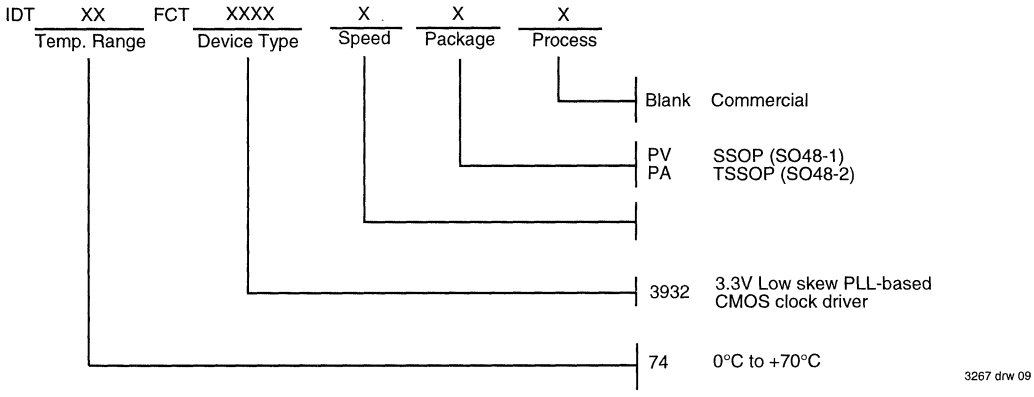
3267 lnk 10

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.

9

ORDERING INFORMATION



Integrated Device Technology, Inc.

3.3V PENTIUM™ CLOCK SYNTHESIZER

IDT74FCT3907
ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- Generates keyboard, floppy disk, system reference, PCI and CPU clocks
- 6 copies of PCI clock & 4 copies of CPU clock available
- 14.31818MHz crystal input
- CPU clock output skew <250ps
  Bus clock output skew <500ps
- 0.03% output frequency accuracy
- Power-on reset
- Selectable CPU clock frequency (50/60/66.66MHz)
- Internal loop filter
- Vcc = 3.3 ±0.3V
- Available in 28 pin SOIC
- Supports Pentium™ processor based designs
- Meets Intel Pentium™ processor 3.3V Clock Driver specification (External Draft 1.0)

DESCRIPTION:

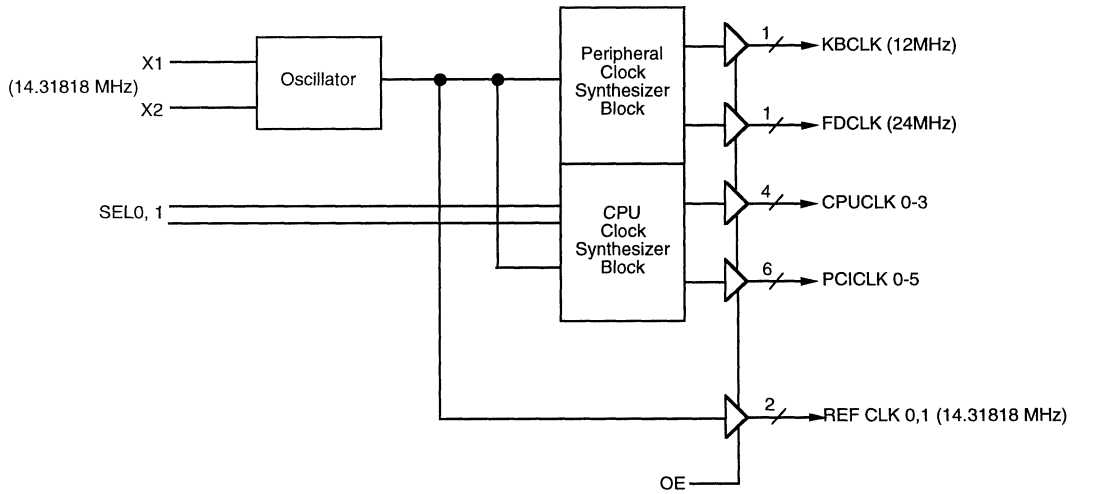
The IDT74FCT3907 Clock synthesizer is built using advanced dual metal CMOS technology. This device uses a 14.31818 MHz crystal input to synthesize the various motherboard clock frequencies.

The output frequencies supported by the IDT74FCT3907 are as follows:

Reference clocks (2) = 14.31818MHz
Keyboard clock (1) = 12MHz
Floppy disk clock (1) = 24MHz
CPU clock (4) = 50/60/66.66 MHz (Selectable by SEL pins)
Bus clock (6) = CPU clock ÷ 2

The SEL0, 1 pins are used to choose appropriate CPUCLK and PCICLK frequencies or to put the device in a test mode. In the test mode, the device outputs various divisors of the test clock frequency. Refer to the function table in this datasheet for details on the different operating modes.

FUNCTIONAL BLOCK DIAGRAM



3245 drw 01

9

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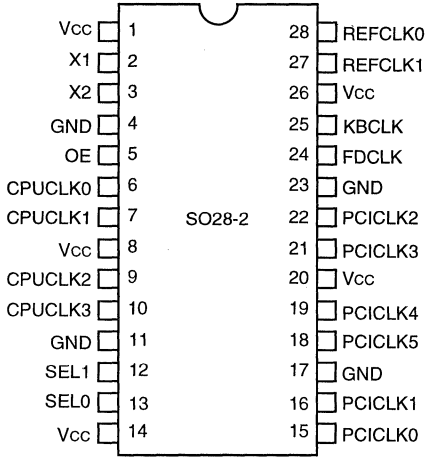
Pentium™ is a trademark of Intel Corp.

PIN CONFIGURATION



3245 drw 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to Vcc + 0.5	V
T_A	Operating Temperature	0 to 70	°C
T_{BIAS}	Temperature Under Bias	0 to +70	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–60 to +60	mA

3245 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input, Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	5.5	8.0	pF

3245 lnk 02

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Name	I/O	Description
X1	I	14.31818 MHz Crystal Input. This is also the test clock input.
X2	O	14.31818 MHz Crystal Output
SEL0, 1	I	CPUCLK Control Inputs
KBCLK	O	Keyboard Clock (12MHz)
FDCLK	O	Floppy Disk Clock (24MHz)
REFCLK 0, 1	O	Reference Clocks (14.31818 MHz)
CPUCLK 0-3	O	CPU Clocks
PCICLK 0-5	O	PCI Bus Clocks
OE	I	Output Enable

3245 tbl 03

FUNCTION TABLE

OE	SEL0	SEL1	INPUT CLK	CPUCLK	PCICLK	REFCLK	FDCLK	KBCLK
0	X	X	14.31818MHz	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	0	14.31818MHz	50MHz	CPUCLK/2	14.31818MHz	24MHz	12MHz
1	0	1	14.31818MHz	60MHz	CPUCLK/2	14.31818MHz	24MHz	12MHz
1	1	0	14.31818MHz	66.66MHz	CPUCLK/2	14.31818MHz	24MHz	12MHz
1	1	1	TCLK (Test Clock)	TCLK/2	TCLK/4	TCLK	TCLK/4	TCLK/8

3245 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.	V_{CC}–0.6V	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4,6]	V_{CC} = Max., V_O = GND[3]		–43	–135	–206	mA
I_{OS}	Short Circuit Current[4,7]	V_{CC} = Max., V_O = GND[3]		–34	–135	–195	mA
I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	3.0	4.0	mA

3245 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. The test limit for this parameter is ±5µA at T_A = –55°C.
6. Applies to CPUCLK.
7. Applies to PCICLK.

DYNAMIC OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODH}	CPUCLK Output HIGH Current	V_{IN} = V_{IH} or V_{IL},	V_{CC} = 3.135V (3.3V –5%)	–23		—	mA
		V_{OUT} = 2.4V	V_{CC} = 3.465V (3.3V +5%)	—		–109	
I_{ODH}	PCICLK Output HIGH Current	V_{IN} = V_{IH} or V_{IL},	V_{CC} = 3.135V	–14.5		—	mA
		V_{OUT} = 2.4V	V_{CC} = 3.465V	—		–100	
I_{ODL}	CPUCLK Output LOW Current	V_{IN} = V_{IH} or V_{IL},	V_{CC} = 3.135V	16		—	mA
		V_{OUT} = 0.4V	V_{CC} = 3.465V	—		40	
I_{ODL}	PCICLK Output LOW Current	V_{IN} = V_{IH} or V_{IL},	V_{CC} = 3.135V	9.4		—	mA
		V_{OUT} = 0.4V	V_{CC} = 3.465V	—		38	

3245 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. The test limit for this parameter is ±5µA at T_A = –55°C.

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OSCILLATOR CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions[1]	Min.	Typ.[2]	Max.	Unit
C_{X1}	X1 Input Capacitance			20		pF
C_{X2}	X2 Output Capacitance			20		pF
I_{IH}	X1 Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		5		µA
I_{IL}	X1 Input LOW Current	V_{CC} = Max., V_{IN} = GND		–5		µA
I_{ODH}	X2 Output HIGH Current	V_{OUT} = V_{CC}		–1		mA
I_{ODL}	X2 Output LOW Current	V_{OUT} = GND		1		mA

3245 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = V_{CC} –0.6V			—	2.0	30	µA
I_C	Total Power Supply Current	V_{CC} = Max.	CPUCLK = 50MHz	V_{IN} = V_{CC}	—			mA
		Outputs Open	CPUCLK = 60MHz	V_{IN} = GND	—			
		50% Duty Cycle OE = V_{CC}	CPUCLK = 66.66MHz		—			

3245 tbl 08

NOTES:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. Per TTL driven input (V_{IN} = V_{CC} -0.6V); all other inputs at V_{CC} or GND.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	74FCT3907						Unit
			66.66MHz		60MHz		50MHz		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{CPU}	CPUCLK Period	TBD	15	—	16.7	—	20	—	ns
t_{CPUH}	CPUCLK HIGH Time[3]		4	—	4	—	4	—	ns
t_{CPUL}	CPUCLK LOW Time[4]		4	—	4	—	4	—	ns
t_{R1}, t_{F1}	CPUCLK Rise, Fall Times (Between 0.4V & 2.4V)		0.8	2.0	0.8	2.0	0.8	2.0	ns
$t_{SK1(o)}$	CPUCLK Output Skew		—	250	—	250	—	250	ps
$t_{SK1(p)}$	CPUCLK Pulse Skew $\lvert t_{PLH}-t_{PHL}\rvert$		—		—		—		ps
t_{PCI}	PCICLK Period		30	—	33.3	—	40	—	ns
t_{PCIH}	PCICLK HIGH Time		12	—	13.3	—	16	—	ns
t_{PCIL}	PCICLK LOW Time		12	—	13.3	—	16	—	ns
t_{R2}, t_{F2}	PCICLK Rise, Fall Time (Between 0.4V & 2.4V)		0.5	2.0	0.5	2.0	0.5	2.0	ns
$t_{SK2(o)}$	PCICLK Output Skew		—	500	—	500	—	500	ps
$t_{SK2(p)}$	PCICLK Pulse Skew $\lvert t_{PLH}-t_{PHL}\rvert$		—		—		—		ps
$t_{SK3(o)}$	CPUCLK to PCICLK Output Delay		1.0	5.0	1.0	5.0	1.0	5.0	ns
t_{PS}	CPUCLK, PCICLK Period Stability		—	250	—	250	—	250	ps
t_{CLOCK}	CPUCLK Lock Time		—	2	—	2	—	2	ms
t_{PLOCK}	PCICLK Lock Time		—	3	—	3	—	3	ms
t_{PZL} t_{PZH}	Output Enable Time OE to KBCLK, FDCLK, REFCLK, CPUCLK, PCICLK (Test Mode)		1.5	8.0	1.5	8.0	1.5	8.0	ns
t_{PLZ} t_{PHZ}	Output Disable Time OE to KBCLK, FDCLK, REFCLK, CPUCLK, PCICLK (Test Mode)		1.5	8.0	1.5	8.0	1.5	8.0	ns

3245 tbl 09

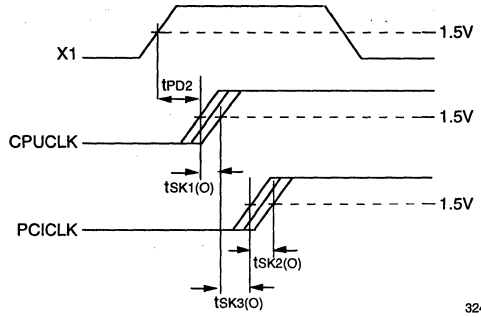
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

9

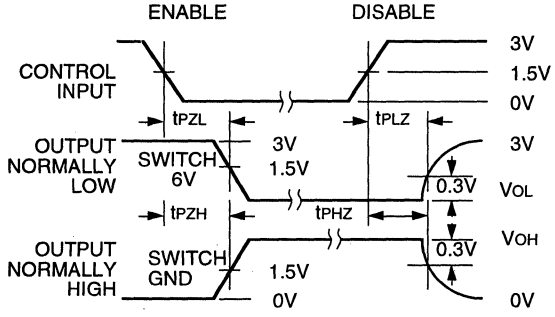
TEST WAVEFORMS

PROPAGATION DELAY, OUTPUT SKEW



3245 drw 03

ENABLE AND DISABLE TIMES

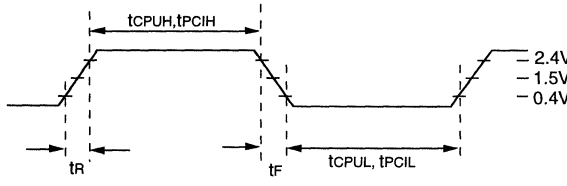


3245 drw 05

NOTES:

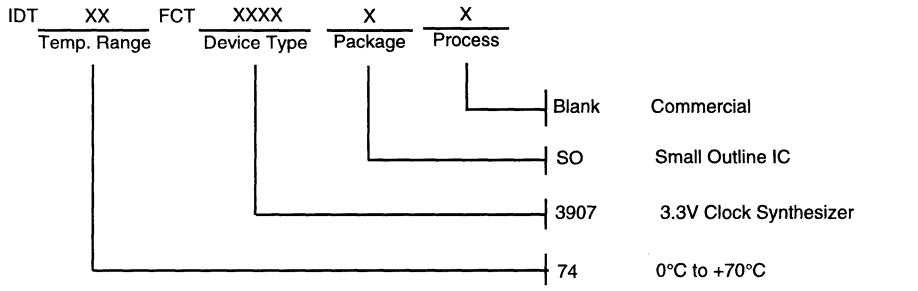
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

PULSE WIDTH, RISE/FALL TIMES



3245 drw 04

ORDERING INFORMATION



3245 drw 06

9

BUS SWITCH LOGIC

Simple, fast and flexible describes FST, a new family of high speed CMOS bus switches from IDT. IDT Bus Switches connect two buses without adding propagation delay or noise.

IDT Bus Switch products can be used in a number of different applications which may be sensitive to delay. This product line implements various configurations of NMOS switches and key features include:

- "Zero Delay" (0.25ns)
- Low on-resistance
- Very low leakage current
- Low power dissipation
- Low noise

The switch is enabled by applying a forward bias on the gate-source junction of the NMOSFET. When ON the switch is the equivalent of a wire connection. When OFF, the switch presents a small load capacitance on the isolated ports.

Bus Switch products are available in two versions.

FSTxxx — 5Ω version
FST32xxx — 28Ω version

The low on-resistance of the switch and the simplicity of the connection between ports reduces the delay through the bus Switch.

The "zero delay" feature of the bus switch can be used to reduce or eliminate performance loss and provide bus isolation. The inherent isolation between ports that the bus switch provide, with the power-off feature is useful in designs requiring hot insertion. Bus switch products are also useful in voltage translation applications and for zero-delay multiplexing and switching. More detail on the characteristics and applications of this family can be found in individual datasheets and IDT's Logic Design Guide.

SECTION 10
BUS SWITCH PRODUCTS
TABLE OF CONTENTS

Integrated Device Technology, Inc.

OCTAL BUS SWITCH

IDT74FST3244/
IDT74FST32244
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance:
  FST3xxx – 5Ω
  FST32xxx – 28Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP, SOIC and PDIP
- Pin-compatible with FCT244/FCT244T

DESCRIPTION:

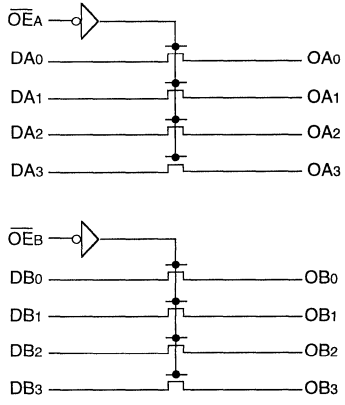
The FST3244/32244 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST32244 integrates terminating resistors in the device, thus eliminating the need for external 25Ω series resistors.

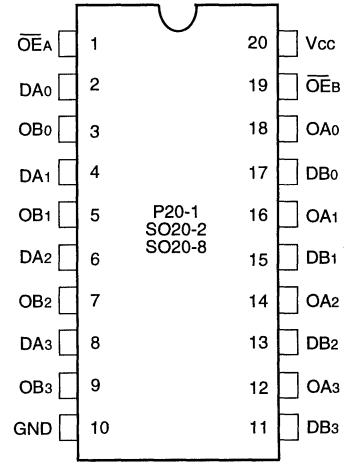
The FST3244 and FST32244 are octal TTL-compatible bus switches. The $\overline{OE}$ pins provide output enable control for all 8 bits.

FUNCTIONAL BLOCK DIAGRAM



3255 drw 01

PIN CONFIGURATION



DIP/SOIC/QSOP
TOP VIEW

3255 drw 02

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A$, $\overline{OE}_B$	Output Enable Inputs (Active LOW)
DA_{0-3}, OA_{0-3}	A Port Bits
DB_{0-3}, OB_{0-3}	B Port Bits

3255 tbl 03

10

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	–60 to +120	mA

3255 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input, I/O and V_{CC} terminals.

FUNCTION TABLE

$\overline{OE}_A$	$\overline{OE}_B$	OA	OB	Description
H	H	Hi-Z	Hi-Z	Disconnect
L	H	DA	Hi-Z	Connect
H	L	Hi-Z	DB	Connect
L	L	DA	DB	Connect

3255 tbl 03

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5		pF

3255 tbl 04

NOTE:
1. Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance(4)	V_{CC} = Min., V_{IN} = 0.0 V	3xxx	—	5	7	Ω
		I_{ON} = 30mA	32xxx	17	28	40	
		V_{CC} = Min., V_{IN} = 2.4 V	3xxx	—	10	15	Ω
		I_{ON} = 15mA	32xxx	20	35	48	
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_I = GND or V_{CC}		—	0.1	10	µA

3255 lnk 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pin Toggling (4 Switches Toggling) fi = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.2	1.6	mA
			V_{IN} = 3.4 V_{IN} = GND	—	1.5	2.4	

3255 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   N = Number of Switches Toggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

			Com'l.				
					Max.		
Symbol	Description	Condition[1]	Min.[2]	Typ.	3244	32244	Unit
t_{PLH} t_{PHL}	Data Propagation Delay DA, DB to OA, OB OA, OB to DA, DB[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	1.25	ns
t_{PZH} t_{PZL}	Switch Turn on Delay $\overline{OE}_A$ to DA, OA, $\overline{OE}_B$ to DB, OB		1.5	—	6.5	7.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay $\overline{OE}_A$ to DA, OA, $\overline{OE}_B$ to DB, OB[3]		1.5	—	5.5	5.5	ns
$\lvert Q_{CH} \rvert$	Charge Injection[5,6]		—	1.5	—	—	pC

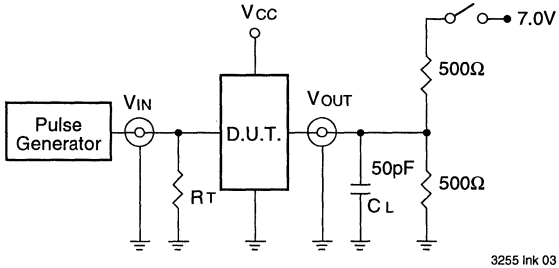
3255 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
6. Characterized parameter. Not 100% tested.

10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3255 lnk 03

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

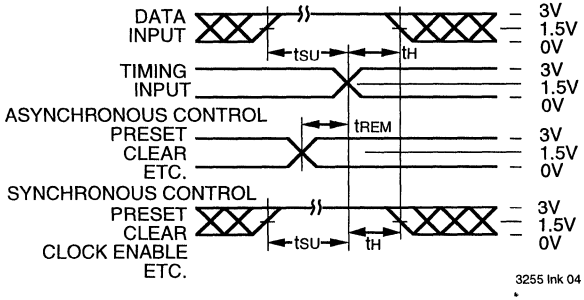
3255 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

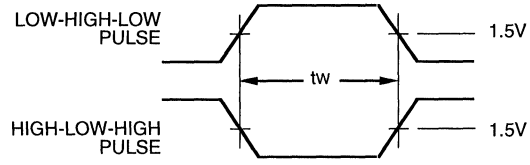
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



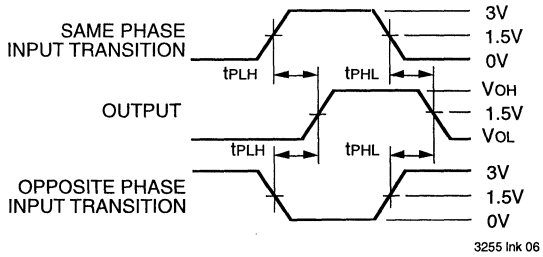
3255 lnk 04

PULSE WIDTH



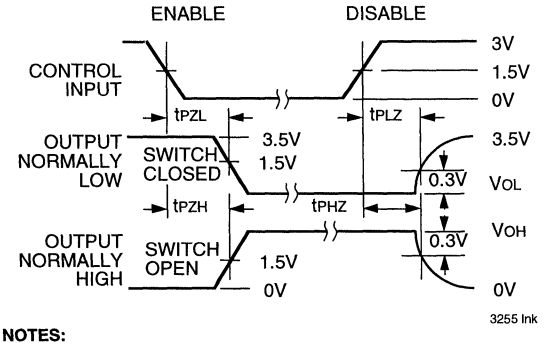
3255 lnk 05

PROPAGATION DELAY



3255 lnk 06

ENABLE AND DISABLE TIMES

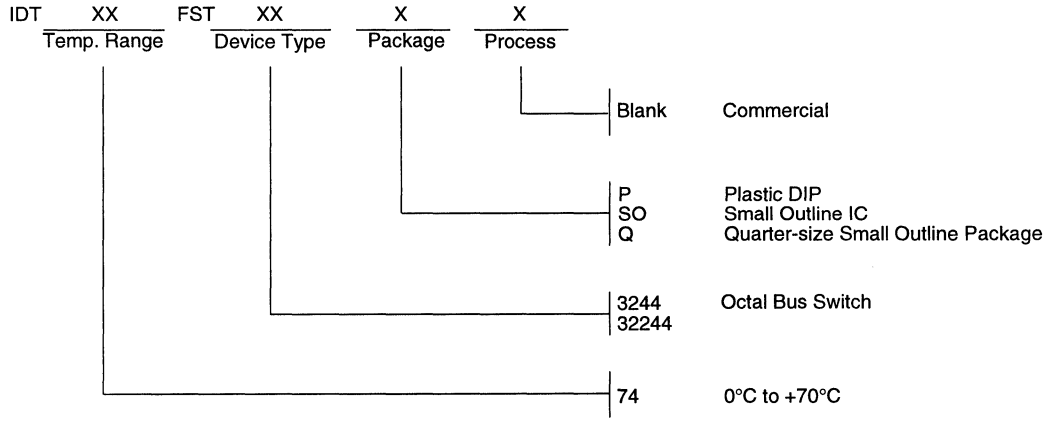


3255 lnk 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



3255 drw 08

10

Integrated Device Technology, Inc.

OCTAL BUS SWITCH

IDT74FST3245/
IDT74FST32245
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance:
  FST3xxx – 5Ω
  FST32xxx – 28Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP, SOIC and PDIP
- Pin-compatible with FCT245/FCT245T

DESCRIPTION:

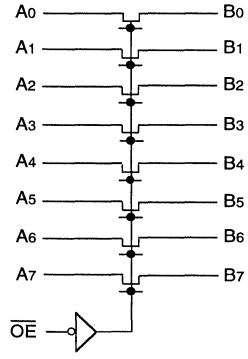
The FST3245/32245 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST32245 integrates terminating resistors in the device, thus eliminating the need for external 25Ω series resistors.

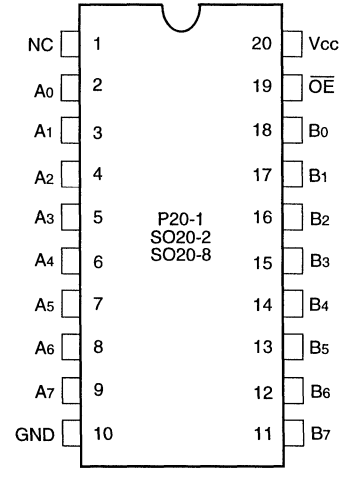
The FST3245 and FST32245 are octal TTL-compatible bus switches. The $\overline{OE}$ pin provides output enable control for all 8 bits. The direction control pin (DIR) of the FCT245/FCT245T is replaced with a "No connect" (NC) in the FST3245/32245. Bus switch devices provide an inherently bidirectional connection between ports, thus eliminating the purpose of the direction control pin.

FUNCTIONAL BLOCK DIAGRAM



3256 drw 01

PIN CONFIGURATION



DIP/SOIC/QSOP
TOP VIEW

3256 drw 02

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
NC	No connect
A0-A7	A Port Bits
B0-B7	B Port Bits

3256 tbl 01

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	–60 to +120	mA

3256 lnk 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input, I/O and V_{CC} terminals.

FUNCTION TABLE

$\overline{OE}$	B_{0-7}	Description
H	X	Disconnect
L	A_{0-7}	Connect

3256 tbl 03

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5		pF

3256 tbl 04

NOTE:
1. Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance[4]	V_{CC} = Min., V_{IN} = 0.0 V	3xxx	—	5	7	Ω
		I_{ON} = 30mA	32xxx	17	28	40	
		V_{CC} = Min., V_{IN} = 2.4 V	3xxx	—	10	15	Ω
		I_{ON} = 15mA	32xxx	20	35	48	
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_I = GND or V_{CC}		—	0.1	10	µA

3256 lnk 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pin Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	3.2	mA
		(8 Switches Toggling) f_i = 10MHz 50% Duty Cycle	V_{IN} = 3.4 V_{IN} = GND	—	2.7	4.0	

NOTES:

3256 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   N = Number of Switches Toggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Description	Condition[1]	Com'l.				Unit
			Min.[2]	Typ.	Max. 3245	Max. 32245	
t_{PLH} t_{PHL}	Data Propagation Delay Ai to Bi, Bi to Ai[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	1.25	ns
t_{PZH} t_{PZL}	Switch Turn on Delay $\overline{OE}$ to Ai, Bi		1.5	—	6.5	7.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay $\overline{OE}$ to Ai, Bi[3]		1.5	—	5.5	5.5	ns
$\lvert Q_{CH} \rvert$	Charge Injection[5,6]		—	1.5	—	—	pC

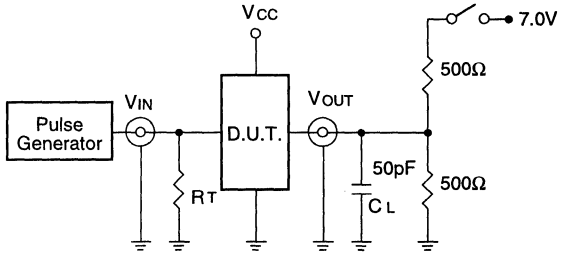
NOTES:

3256 tbl 07

1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
6. Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3256 lnk 04

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

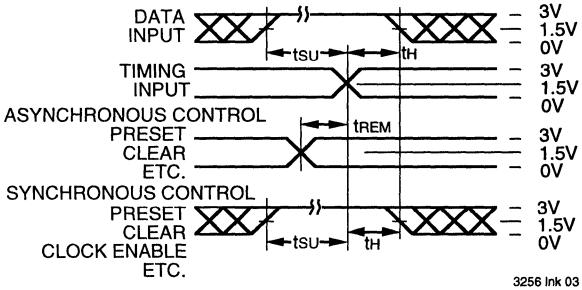
3256 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

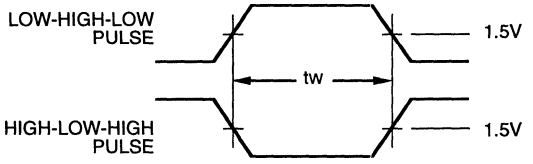
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



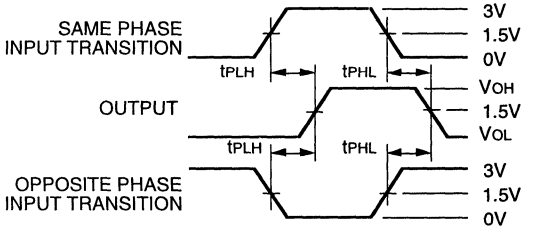
3256 lnk 03

PULSE WIDTH



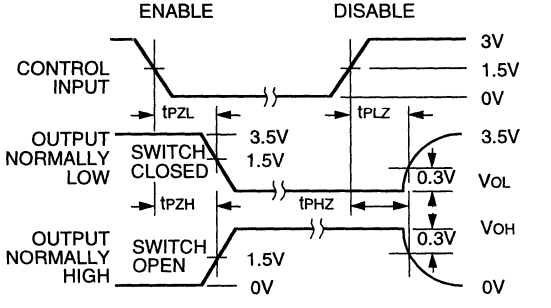
3256 lnk 06

PROPAGATION DELAY



3256 lnk 07

ENABLE AND DISABLE TIMES



3256 lnk 05

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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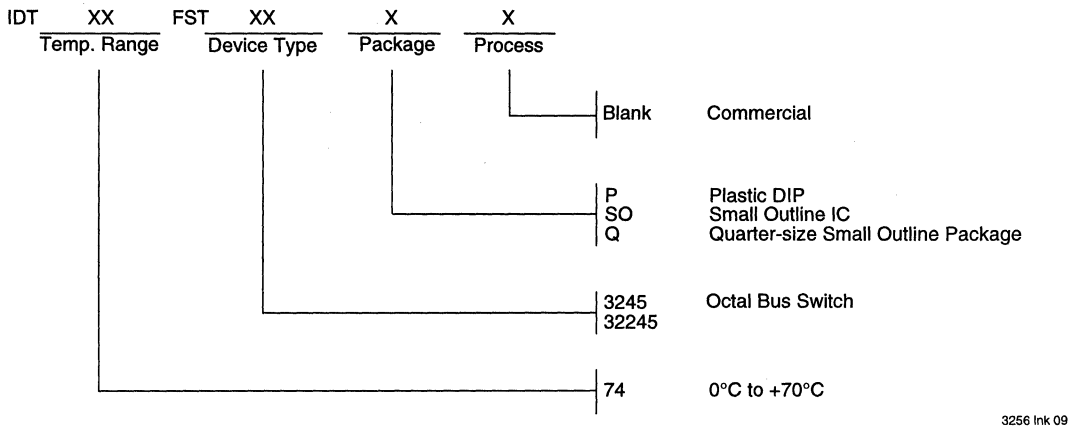
ORDERING INFORMATION



3256 lnk 09

Integrated Device Technology, Inc.

QUAD 2:1 MUX/DEMUX BUS SWITCH

IDT74FST3257
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance:
  FST3xxx – 5Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP and SOIC

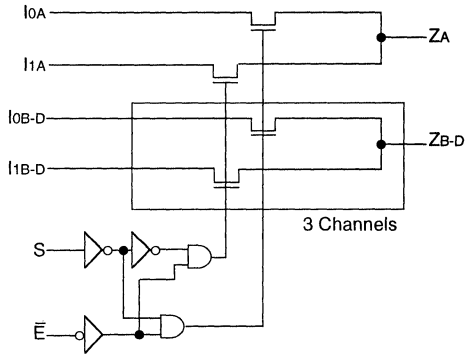
DESCRIPTION:

The FST3257 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

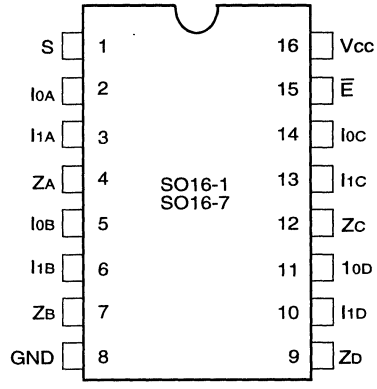
The FST3257 provides a 4-bit 2:1 multiplexer/demultiplexer. The S pin controls the mux select and the $\overline{E}$ pin serves as the switch enable.

FUNCTIONAL BLOCK DIAGRAM



3257 drw 01

PIN CONFIGURATION



SOIC/QSOP
TOP VIEW

3257 drw 02

PIN DESCRIPTION

Pin Names	I/O	Description
I0A-I0D	I/O	Port 0
I1A-I1D	I/O	Port 1
$\overline{E}$	I	Switch Enable (Active Low)
S	I	Mux Select
ZA-ZB	I/O	Port Z

3257 tbl 01

10

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES: 3257 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input, I/O and V_{CC} terminals.

FUNCTION TABLE(1)

$\overline{E}$	S	I_{0A-D}	I_{1A-D}	Z_{A-D}
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

NOTE: 3257 tbl 03

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5		pF

NOTE: 3257 tbl 04

1. Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance(4)	V_{CC} = Min., V_{IN} = 0.0V, I_{ON} = 30mA		—	5	7	Ω
		V_{CC} = Min., V_{IN} = 2.4V, I_{ON} = 15mA		—	10	15	Ω
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.1	10	µA

3257 tbl 05

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pin Toggling (4 Switches Toggling) fi = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.2	1.6	mA
			V_{IN} = 3.4 V_{IN} = GND	—	1.5	2.4	

3257 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   N = Number of Switches Toggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Description	Condition[1]	Com'l. Min.[2]	Com'l. Typ.	Com'l. Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay I to Z, Z to I[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	ns
t_{PLH} t_{PHL}	Switch Multiplex Delay S to I, Z		1.5	—	5.2	ns
t_{PZH} t_{PZL}	Switch Turn on Delay $\overline{E}$ to I, Z		1.5	—	4.8	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay $\overline{E}$ to I, Z[3]		1.5	—	5.0	ns
$\lvert Q_{CI} \rvert$	Charge Injection, Typical[5,6]		—	1.5	—	pC
$\lvert Q_{CDI} \rvert$	Charge Injection, Typical[6,7]		—	0.5	—	pC

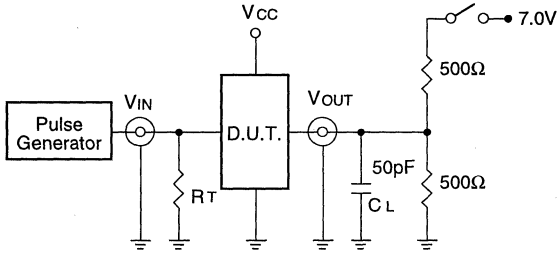
3257 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 mΩ scope probe, V_{IN} = 0.0 volts.
6. Measured at switch turn off through bus multiplexer, (e.g.- I_0 to Z = > I_1 to Z), load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the I_0 to Z switch is compensated by the turn on of the I_1 to Z switch.
7. Characterized parameter. Not 100% tested.

10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3257 lnk 03

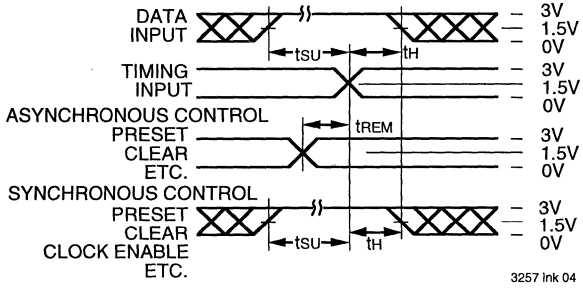
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS: 3257 lnk 08

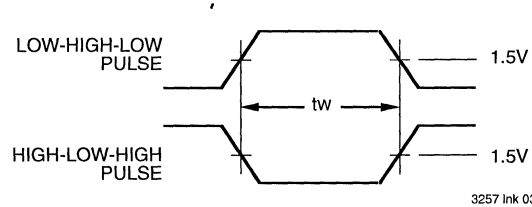
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



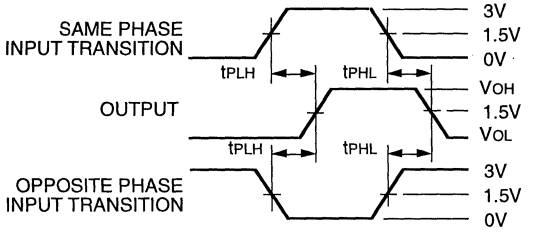
3257 lnk 04

PULSE WIDTH



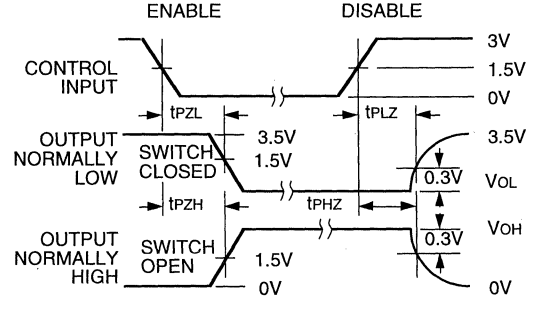
3257 lnk 03

PROPAGATION DELAY



3257 lnk 06

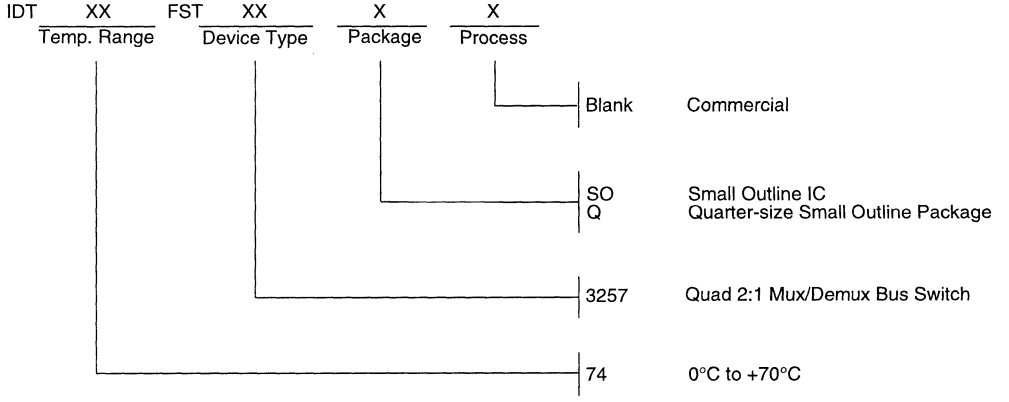
ENABLE AND DISABLE TIMES



3257 lnk 07

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



3257 drw 08

10

Integrated Device Technology, Inc.

OCTAL BUS EXCHANGE SWITCH

IDT74FST3383
IDT74FST32383
PRELIMINARY

FEATURES:

- Bus Switches provide zero delay paths
- Low switch on-resistance:
  FST3xxx – 5Ω
  FST32xxx – 28Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP, SOIC and PDIP

DESCRIPTION:

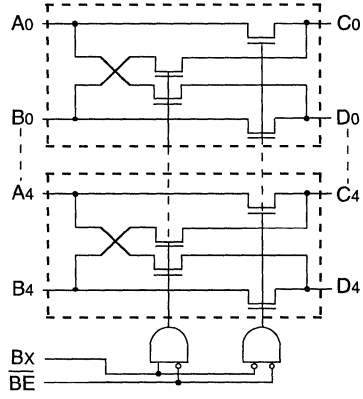
The FST3383/32383 belong to IDT's family of Bus Switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST32383 integrates terminating resistors in the device, thus eliminating the need for external 25Ω series resistors.

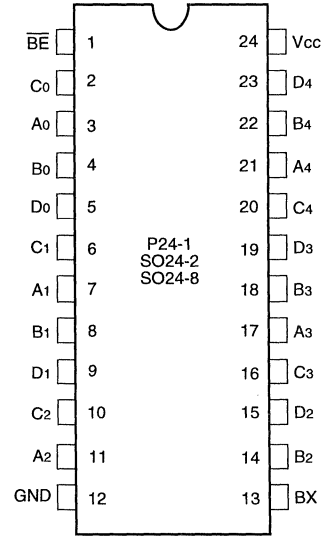
The FST3383 and FST32383 each provide four 5-bit TTL-compatible ports that support 2 way bus exchange. The BX pin controls the bus exchange and the $\overline{BE}$ pin serves as the enable pin.

FUNCTIONAL BLOCK DIAGRAM



3258 drw 01

PIN CONFIGURATION



DIP/SOIC/QSOP
TOP VIEW

3258 drw 02

PIN DESCRIPTION

Pin Names	I/O	Description
A0-4, B0-4	I/O	Buses A, B
C0-4, D0-4	I/O	Buses C, D
$\overline{BE}$	I	Bus Switch Enable (Active LOW)
BX	I	Bus Exchange

3258 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	–60 to +120	mA

3258 lnk 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input, I/O and V_{CC} terminals.

FUNCTION TABLE

$\overline{BE}$	BX	A_{0-4}	B_{0-4}	Description
H	X	Hi-Z	Hi-Z	Disconnect
L	L	C_{0-4}	D_{0-4}	Connect
L	H	D_{0-4}	C_{0-4}	Exchange

3258 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5		pF

3258 tbl 04

NOTE:
1. Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance(4)	V_{CC} = Min., V_{IN} = 0.0 V	3xxx	—	5	7	Ω
		I_{ON} = 30mA	32xxx	17	28	40	
		V_{CC} = Min., V_{IN} = 2.4 V	3xxx	—	10	15	Ω
		I_{ON} = 15mA	32xxx	20	35	48	
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_I = GND or V_{CC}		—	0.1	10	µA

3258 lnk 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pin Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	4.0	mA
		(10 Switches Toggling) fi = 10MHz 50% Duty Cycle	V_{IN} = 3.4 V_{IN} = GND	—	3.3	4.8	

NOTES:

3258 tbl 06

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   N = Number of Switches Toggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Description	Condition[1]	Com'l. Min.[2]	Com'l. Typ.	Com'l. Max. 3383	Com'l. Max. 32383	Unit
t_{PLH} t_{PHL}	Data Propagation Delay Ai to Ci, Di Bi to Ci, Di[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	1.25	ns
t_{BX}	Switch Multiplex Delay BX to Ai, Bi, Ci, Di		1.5	—	6.5	7.5	ns
t_{PZH} t_{PZL}	Switch Turn on Delay BE to Ai, Bi, Ci, Di		1.5	—	6.5	7.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay BE to Ai, Bi[3]		1.5	—	5.5	5.5	ns
$\lvert Q_{CI} \rvert$	Charge Injection, Typical[5,7]		—	1.5	—	—	pC
$\lvert Q_{CDI} \rvert$	Charge Injection, Typical[6,7]		—	0.5	—	—	

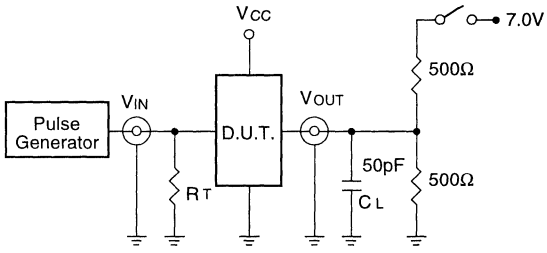
NOTES:

3258 tbl 07

1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
6. Measured at switch turn off through bus multiplexer, (e.g.- A to C = >A to D), load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} at A = 0.0 volts. Charge injection is reduced because the injection from the turn off of the A to C switch is compensated by the turn on of the B to C switch.
7. Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3258 lnk 03

SWITCH POSITION

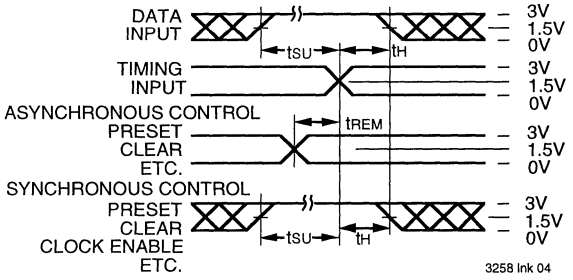
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

3258 lnk 08

DEFINITIONS:

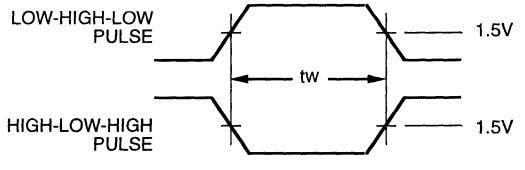
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



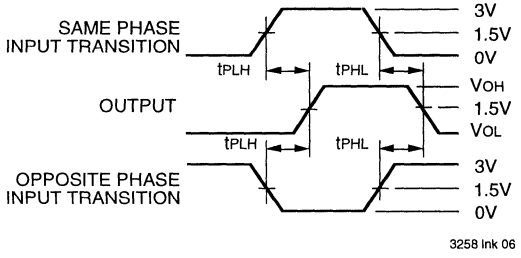
3258 lnk 04

PULSE WIDTH



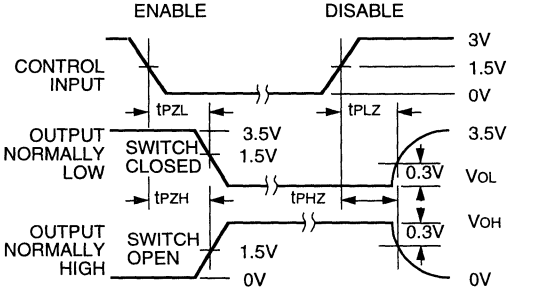
3258 lnk 05

PROPAGATION DELAY



3258 lnk 06

ENABLE AND DISABLE TIMES



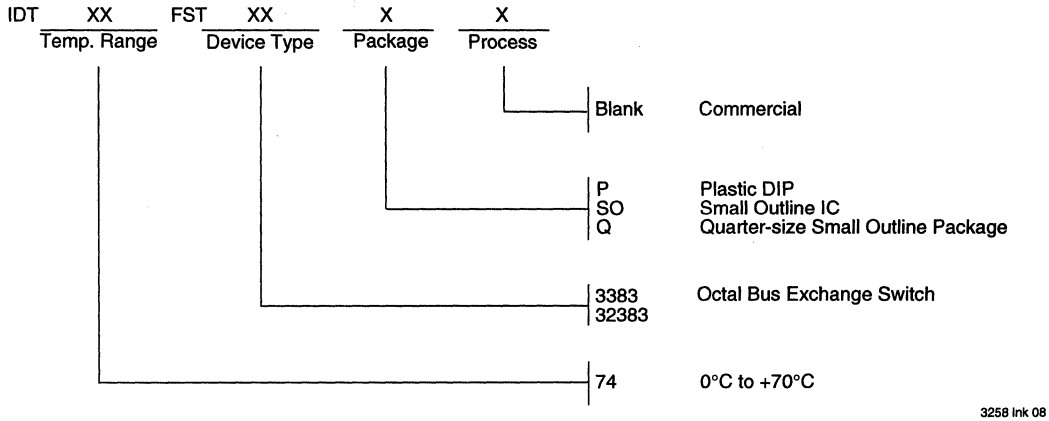
3258 lnk 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

10

ORDERING INFORMATION



3258 lnk 08

Integrated Device Technology, Inc.

10-BIT BUS SWITCH

IDT74FST3384
IDT74FST32384
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance:
  FST3xxx – 5Ω
  FST32xxx – 28Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP, SOIC and PDIP

DESCRIPTION:

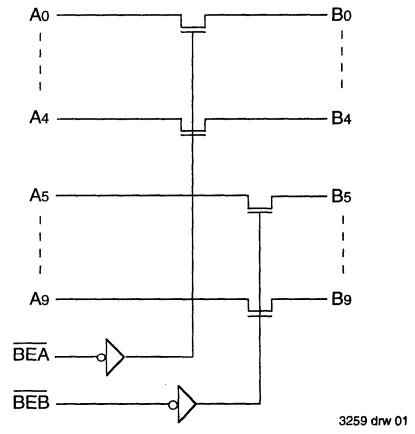
The FST3384/32384 belong to IDT's family of Bus switches. Bus Switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST32384 integrates terminating resistors in the device, thus eliminating the need for external 25Ω series resistors.

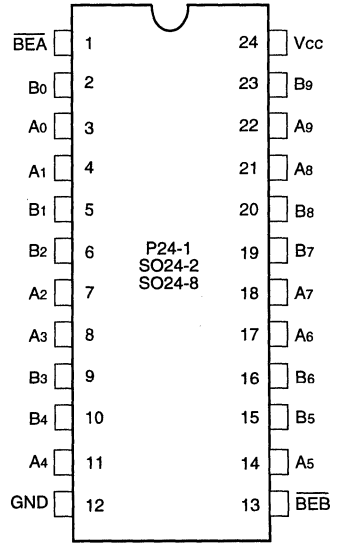
The FST3384 and FST32384 are 10-bit TTL-compatible bus switches. The $\overline{BE}$x pins provide enable control - $\overline{BEA}$ controls the lower 5-bits and $\overline{BEB}$ controls the upper 5-bits.

FUNCTIONAL BLOCK DIAGRAM



3259 drw 01

PIN CONFIGURATION



DIP/SOIC/QSOP
TOP VIEW

3259 drw 02

PIN DESCRIPTION

Pin Names	I/O	Description
A0-9	I/O	Buses A
B0-9	I/O	Buses B
$\overline{BEA}$, $\overline{BEA}$	I	Bus Switch Enable (Active LOW)

3259 tbl 01

10

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES: 3259 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input, I/O and V_{CC} terminals.

FUNCTION TABLE

$\overline{BEA}$	$\overline{BEB}$	B_{0-4}	B_{5-9}	Description
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A_{0-4}	Hi-Z	Connect
H	L	Hi-Z	A_{5-9}	Connect
L	L	A_{0-4}	A_{5-9}	Connect

3259 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5		pF

NOTE: 3259 lnk 04

1. Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance(4)	V_{CC} = Min., V_{IN} = 0.0 V	3xxx	—	5	7	Ω
		I_{ON} = 30mA	32xxx	17	28	40	
		V_{CC} = Min., V_{IN} = 2.4 V	3xxx	—	10	15	Ω
		I_{ON} = 15mA	32xxx	20	35	48	
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_I = GND or V_{CC}		—	0.1	10	µA

NOTES: 3259 lnk 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pin Toggling (10 Switches Toggling) fi = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	4.0	mA
			V_{IN} = 3.4 V_{IN} = GND	—	3.3	4.8	

3259 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   N = Number of Switches Toggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

			Com'l.				
					Max.		
Symbol	Description	Condition[1]	Min.[2]	Typ.	3384	32384	Unit
t_{PLH} t_{PHL}	Data Propagation Delay Ai to Bi, Bi to Ai[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	1.25	ns
t_{PZH} t_{PZL}	Switch Turn on Delay BEx to Ai, Bi		1.5	—	6.5	7.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay BEx to Ai, Bi[3]		1.5	—	5.5	5.5	ns
$\lvert Q_{CI} \rvert$	Charge Injection[5,6]		—	1.5	—	—	pC

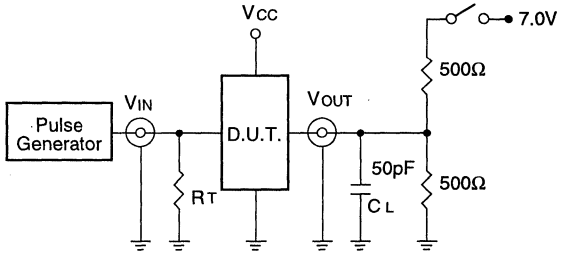
3259 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
6. Characterized parameter. Not 100% tested.

10

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3259 lnk 03

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

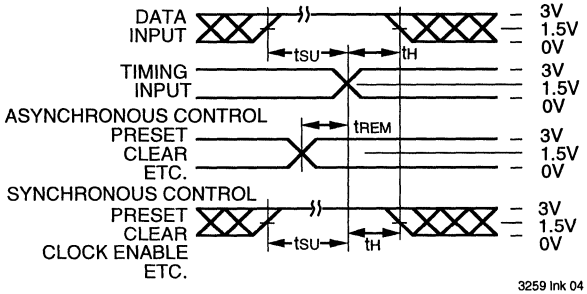
3259 lnk 08

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

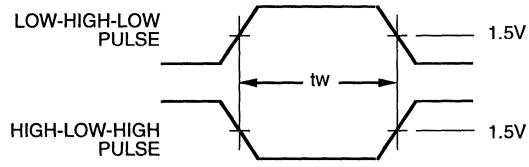
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



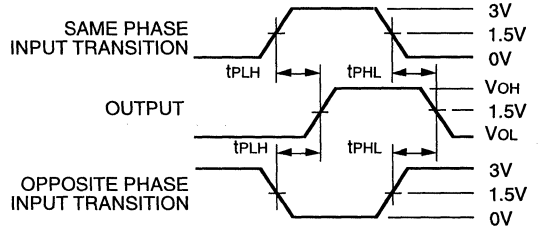
3259 lnk 04

PULSE WIDTH



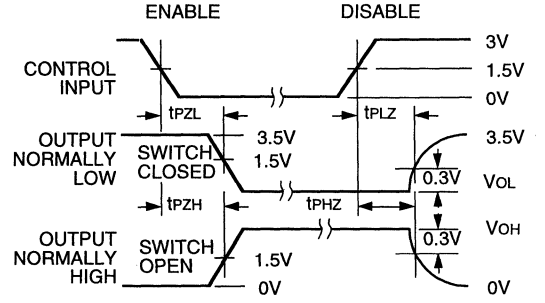
3259 lnk 05

PROPAGATION DELAY



3259 lnk 06

ENABLE AND DISABLE TIMES

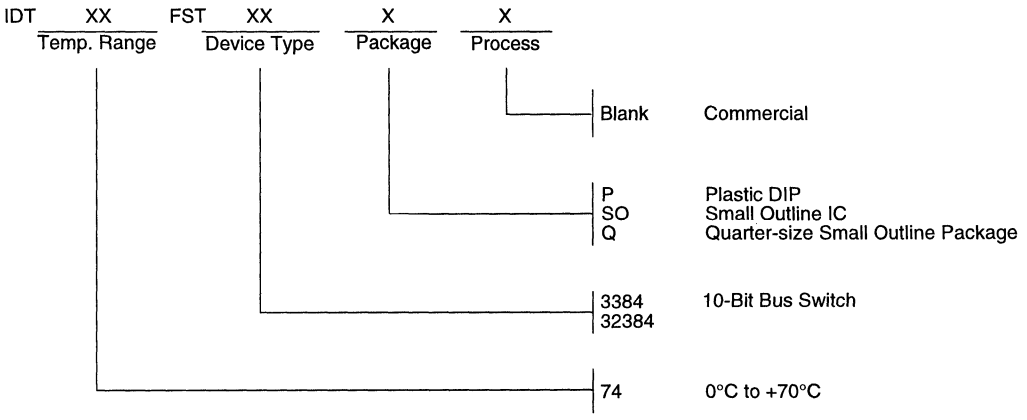


3259 lnk 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



3259 lnk 08

10

Integrated Device Technology, Inc.

OCTAL 2:1 MULTIPLEXER BUS SWITCH

IDT74FST3390
IDT74FST32390
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance:
  FST3xxx – 5Ω
  FST32xxx – 28Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015;
  > 200V using machine model (C = 200pF, R = 0)
- Available in 28-pin QSOP and SOIC

DESCRIPTION:

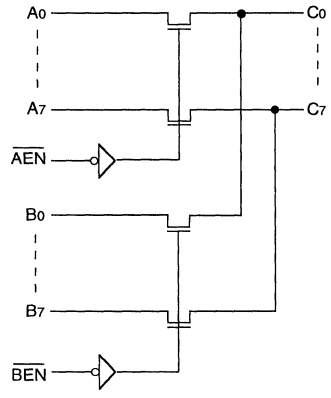
The FST3390/32390 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST32390 integrates terminating resistors in the device, thus eliminating the need for external 25Ω series resistors.

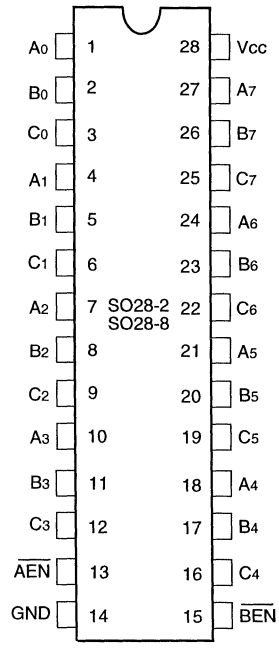
The FST3390 and FST32390 are 8-bit TTL-compatible 2:1 bus multiplexers. $\overline{AEN}$ = 0 connects port A to port C and $\overline{BEN}$ = 0 connects port B to port C. This device can be used to connect ports A & B to a common bus on port C or to broadcast data on port C to both ports A and B.

FUNCTIONAL BLOCK DIAGRAM



3260 drw 01

PIN CONFIGURATION



SOIC/QSOP
TOP VIEW

3260 drw 02

PIN DESCRIPTION

Pin Names	I/O	Description
A0-7	I/O	Bus A
B0-7	I/O	Bus B
C0-7	I/O	Bus C
$\overline{AEN}$, $\overline{BEN}$	I	Bus Switch Enable (Active LOW)

3260 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES: 3260 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input, I/O and Vcc terminals.

FUNCTION TABLE

$\overline{AEN}$	$\overline{BEN}$	A	B	Description
H	H	Off	Off	Disconnect
L	H	On	Off	A to C
H	L	Off	On	B to C
L	L	On	On	A, B to C

3260 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5		pF

NOTE: 3260 tbl 04

1. Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance(4)	V_{CC} = Min., V_{IN} = 0.0 V	3xxx	—	5	7	Ω
		I_{ON} = 30mA	32xxx	17	28	40	
		V_{CC} = Min., V_{IN} = 2.4 V	3xxx	—	10	15	Ω
		I_{ON} = 15mA	32xxx	20	35	48	
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_I = GND or V_{CC}		—	0.1	10	µA

NOTES: 3260 lnk 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pin Toggling (8 Switches Toggling) fi = 10MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	3.2	mA
			V_{IN} = 3.4 V_{IN} = GND	—	2.7	4.0	

3260 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_i = Input Frequency
   N = Number of Switches toggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%

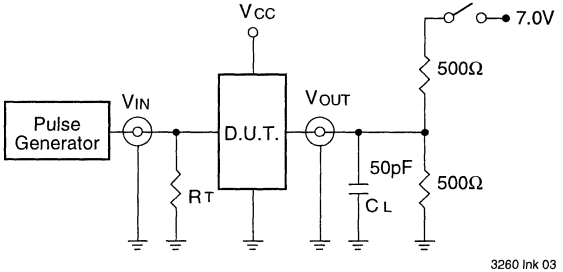
Symbol	Description	Condition[1]	Com'l.				Unit
			Min.[2]	Typ.	Max. 3390	Max. 32390	
t_{PLH} t_{PHL}	Data Propagation Delay A, B to/from C[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	1.25	ns
t_{PZH} t_{PZL}	Switch Turn on Delay $\overline{AEN}$/$\overline{BEN}$ to A, B, C		1.5	—	6.5	7.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay $\overline{AEN}$, $\overline{BEN}$ to A, B, C[3]		1.5	—	5.5	5.5	ns
$\lvert Q_{CH} \rvert$	Charge Injection[5,6]		—	1.5	—	—	pC

3260 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
5. Measured at switch turn off, load = 50 pF in parallel with 10 MΩ scope probe, V_{IN} = 0.0 volts.
6. Characterized parameter. Not 100% tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3260 lnk 03

SWITCH POSITION

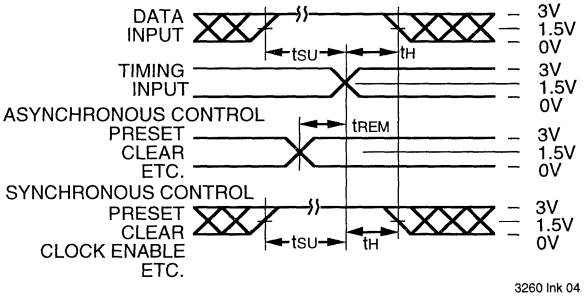
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

3260 lnk 08

DEFINITIONS:

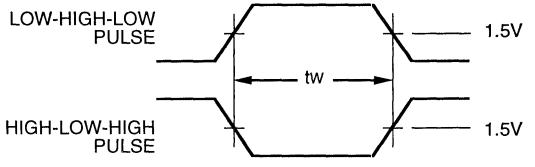
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



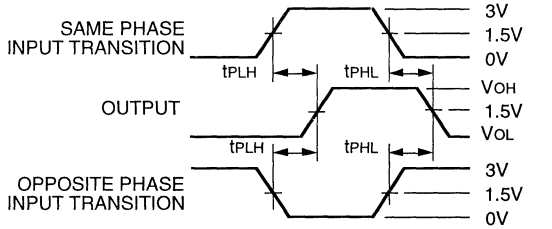
3260 lnk 04

PULSE WIDTH



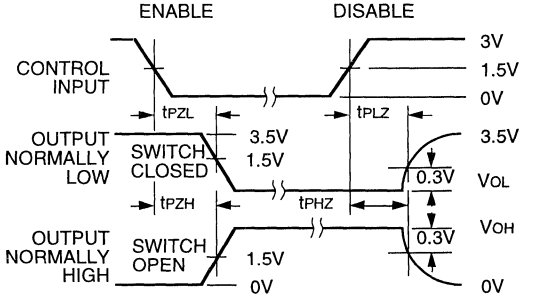
3260 lnk 05

PROPAGATION DELAY



3260 lnk 06

ENABLE AND DISABLE TIMES



3260 lnk 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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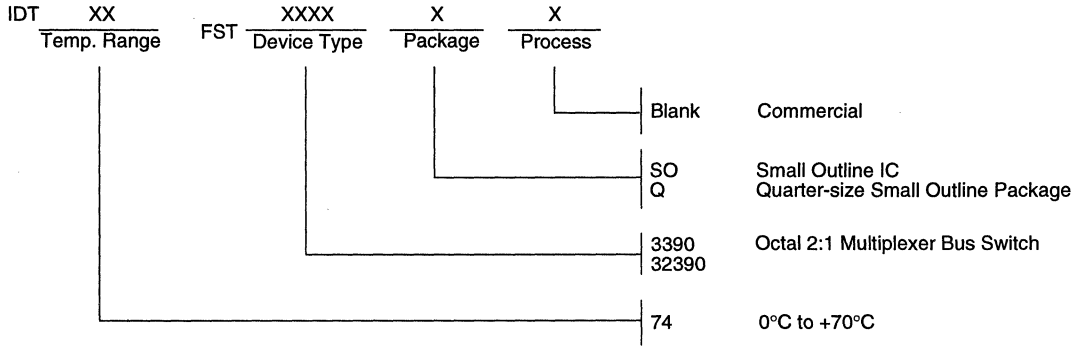
ORDERING INFORMATION



3260 drw 08

Integrated Device Technology, Inc.

10-BIT BUS SWITCH WITH PRECHARGE

IDT74FST6800
PRELIMINARY

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance: 5Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP, SOIC and PDIP

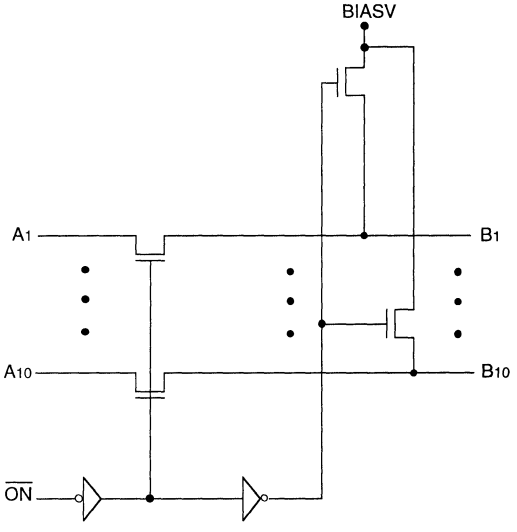
DESCRIPTION:

The FST6800 belong to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

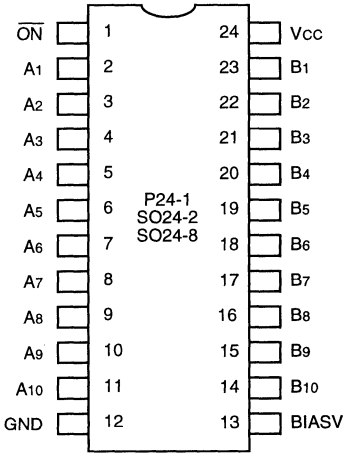
The FST6800 provides a 10-Bit TTL-compatible interface. The $\overline{ON}$ pin serves as the enable pin. When $\overline{ON}$ is high, A and B ports are isolated and B outputs are precharged to the BIASV voltage, through the equivalent of a 10KΩ resistor.

FUNCTIONAL BLOCK DIAGRAM



3261 drw 01

PIN CONFIGURATION



DIP/SOIC/QSOP
TOP VIEW

3261 drw 02

PIN DESCRIPTION

Pin Names	I/O	Description
A1-10, B1-10	I/O	Buses A, B
$\overline{ON}$	I	Bus Switch Enable (Active LOW)
BIASV	I	Bias Voltage

3261 tbl 01

10

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	–60 to +120	mA

3261 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Input, I/O and Vcc terminals.

FUNCTION TABLE

$\overline{ON}$	B_1-B_{10}	Description
L	A_1-A_{10}	Connect
H	BIASV	Precharge

3261 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5		pF

3261 tbl 04

NOTE:
1. Capacitance is characterized but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%; BIASV = 0 to V_{CC}

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
I_{IL}	Input LOW Voltage		V_I = GND	—	—	±1	
I_O	Precharge Output Current	V_{CC} = Min., BIASV = 2.4V, V_O = 0V		0.25	—	—	mA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		—	300	—	mA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		—	–0.7	–1.2	V
R_{ON}	Switch On Resistance(4)	V_{CC} = Min., V_{IN} = 0.0V I_{ON} = 64mA		—	—	6	Ω
		V_{CC} = Min., V_{IN} = 2.4V I_{ON} = 15mA		—	—	12	
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_I = GND or V_{CC}		—	0.1	10	µA

3261 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open Enable Pin Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	30	40	µA/ MHz/ Switch
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open Enable Pin Toggling	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	4.0	mA
		(10 Switches Toggling) fi = 10MHz 50% Duty Cycle	V_{IN} = 3.4 V_{IN} = GND	—	3.3	4.8	

3261 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N = Number of SwitchesToggling at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Description	Condition[1]	Com'l. Min.[2]	Com'l. Typ.	Com'l. Max.	Unit
t_{PLH} t_{PHL}	Data Propagation Delay Ai, Bi to Bi, Ai[3,4]	C_L = 50pF R_L = 500Ω	—	—	0.25	ns
t_{PZH} t_{PZL}	Switch Turn on Delay $\overline{ON}$ to Ai, Bi		1.5	—	6.5	ns
t_{PHZ} t_{PLZ}	Switch Turn off Delay $\overline{ON}$ to Ai, Bi[3]		1.5	—	5.5	ns

3261 tbl 07

NOTES:
1. See test circuit and waveforms.
2. Minimum limits guaranteed but not tested.
3. This parameter is guaranteed by design but not tested.
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

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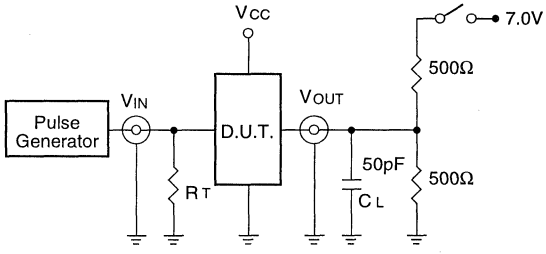
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3261 lnk 03

SWITCH POSITION

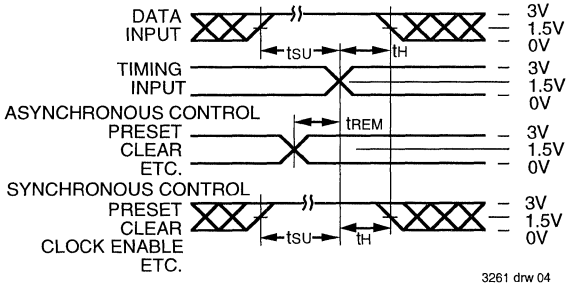
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS: 3261 lnk 08

C_L = Load capacitance: includes jig and probe capacitance.

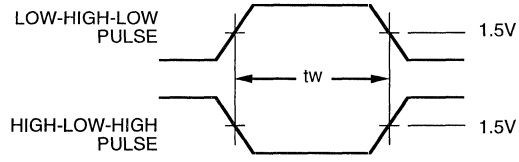
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



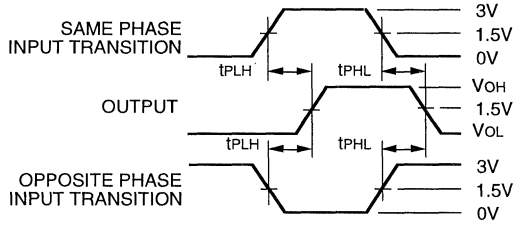
3261 drw 04

PULSE WIDTH



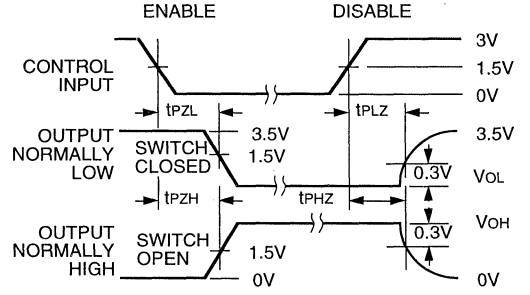
3261 drw 05

PROPAGATION DELAY



3261 drw 06

ENABLE AND DISABLE TIMES

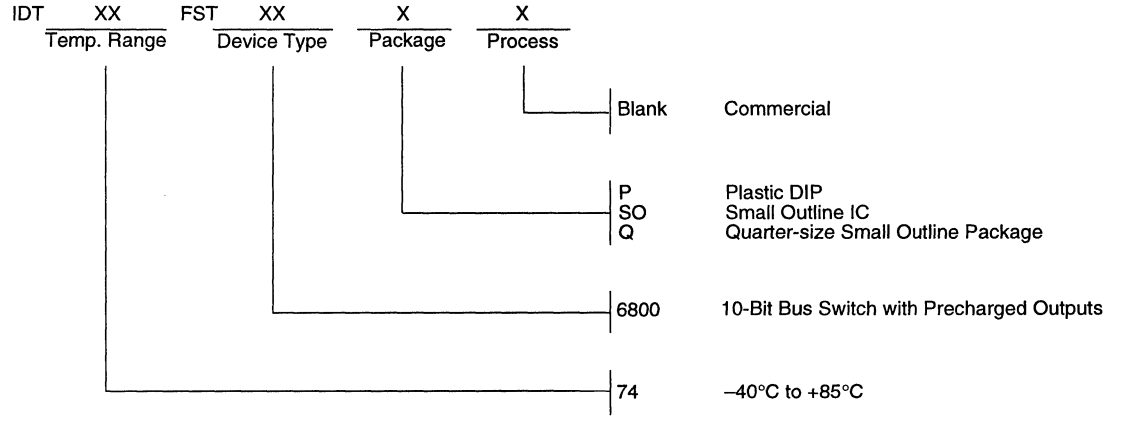


3261 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION



3261 drw 08

10

COMPLEX LOGIC PRODUCTS

IDT's complex Logic products address a wide variety of design applications. In most cases these components provide performance levels that cannot be achieved through more highly-integrated designs. IDT's complex Logic products also provide "off-the-shelf" solutions which can be quickly plugged into an application, avoiding the difficulties associated with new designs. IDT's Complex Logic products are divided into three functional areas:

- Error Detection and Correction
- Read-Write Buffers and Bus Multiplexers
- DSP and Microslice

Error Detection and Correction (EDC)

Today's high-performance systems are becoming increasingly DRAM intensive. IDT offers a full range of high-performance EDC devices that eliminate the performance penalties once associated with these circuits, while assuring the designer continuous, error-free operation which is necessary in high-reliability systems. IDT's EDC products include 16-, 32-, and 64-bit devices with either bus-watch or flow-through architectures. These devices utilize a modified Hamming code which is capable of correcting all single-bit errors and detecting all double-bit errors and some triple-bit errors, with propagation delays as low as 20ns.

The 49C460 and 49C465 are high-speed, low-power, 32-bit EDC units. The 49C460 supports a "Bus-watch" (single data bus) architecture and the 49C465 supports a "Flow-through" (dual data bus) architecture. Both devices are easily cascadable to 64-bits and incorporate built-in diagnostic modes.

The 49C466 is a high-speed 64-bit flow-through EDC unit that ensures data integrity in 64-bit wide memory systems. The 49C466 provides two alternate read and write paths—a transparent latched path and a synchronous path with sixteen-deep read/write FIFOs. Diagnostic features include a check bit register, syndrome registers, a 4-bit error counter (which logs up to 15 errors), and an error data register which stores the complete error data word.

Read-Write Buffers and Bus Multiplexers

The current generation of RISC and CISC microprocessors depend on secondary cache memory for their best performance. IDT has designed the FCT162701T read/write buffer, for this application. With these components, burst writes, characteristic of high speed processors, will not be delayed by slow memories.

Parity checking and generation, which is becoming a requirement in today's systems, can be accomplished using the FCT162511T. This high-speed component can be configured as a buffer, register, or latch with complete bi-directional operation.

IDT provides several bi-directional bus multiplexers for use in high-speed memory interleaving, including the latched FCT16260T, the latched FCT162260T, the registered FCT162H272T, and the registered 73720. The latched components allow fully asynchronous interleaving, while the registered components are capable of higher-speed synchronous operation.

The data sheets for the 73xxx components are contained within the following pages, while the data sheets for the FCT16xxxxT components are located in the Double-Density section of this data book.

DSP and Microslice Processors

Digital signal processing and networking applications have always demanded extremely high-performance building blocks. IDT continues to offer a selection of the world's fastest fixed-point DSP elements (including multipliers, multiplier/accumulators, and ALUs) and Microslice processors. Dicrete component like the 7210, 7216 and 7381 enable the construction of customized, high-performance architectures and instruction sets.

SECTION 11
COMPLEX LOGIC PRODUCTS
TABLE OF CONTENTS

Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

IDT49C402
IDT49C402A
IDT49C402B

FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402B is 60% faster than four 2901Cs and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Fully cascadable
- 84-pin PGA, 80-pin PQFP and 68-pin 25 MIL Center Flatpack
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

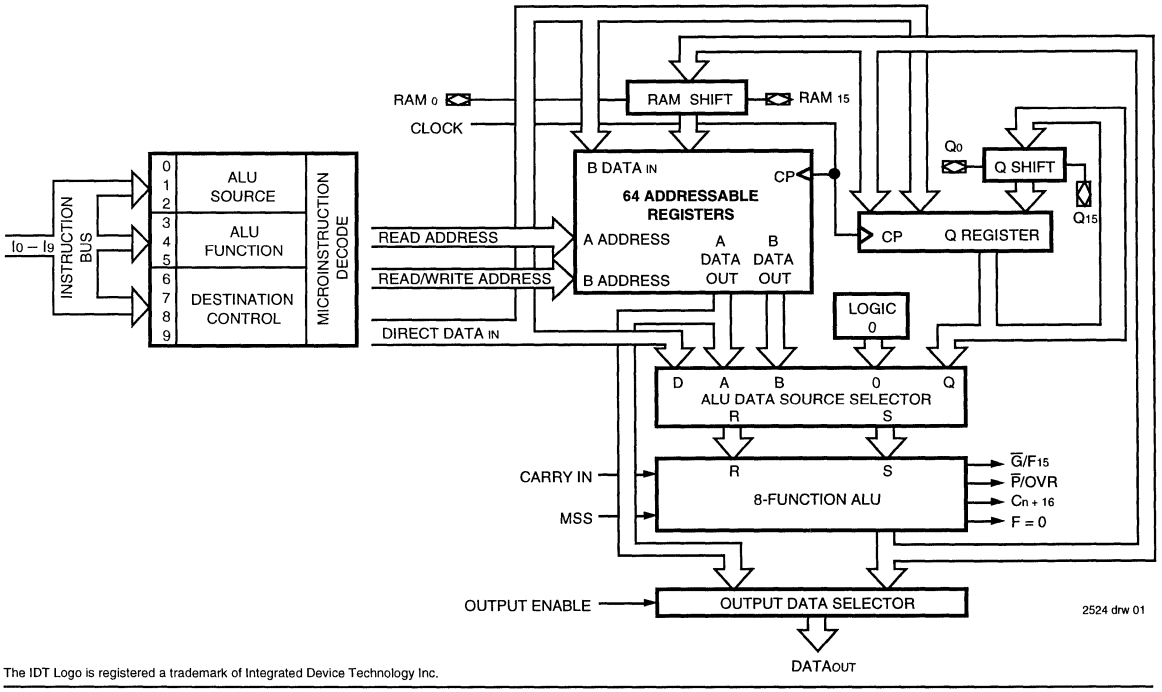
The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

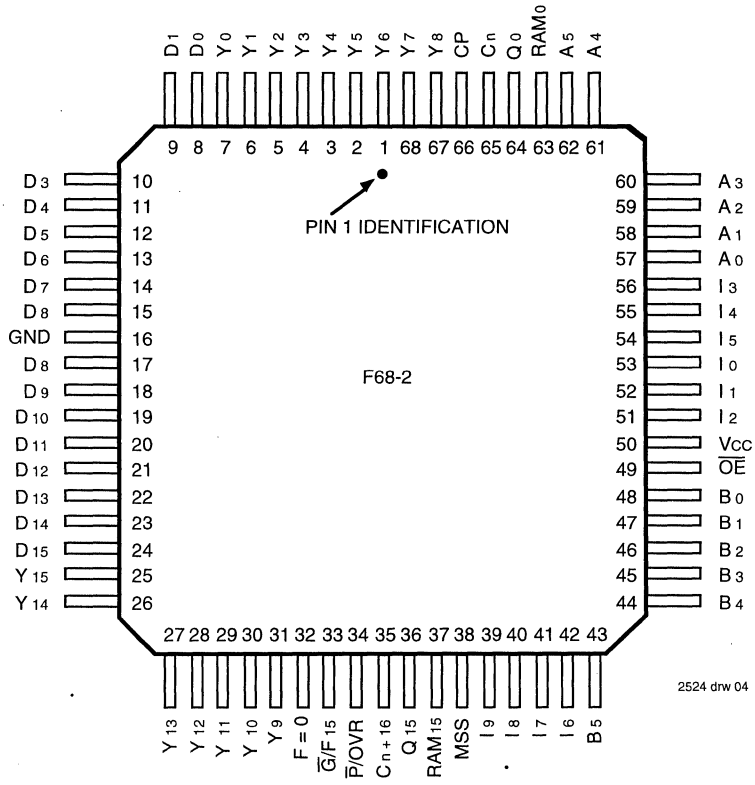
The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: a) a 3-bit instruction field (I_0, I_1, I_2) which controls the source operand selection for the ALU; b) a 3-bit microinstruction field (I_3, I_4, I_5) used to control the eight possible functions of the ALU; c) eight destination control functions which are selected by the microcode inputs (I_6, I_7, I_8); and d) a tenth microinstruction input, I_9, offering eight additional destination control functions. This I_9 input, in conjunction with I_6, I_7 and I_8, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and having the RAM A data output port available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64-words-by-16 bits – four times the number of working registers in a 2901.

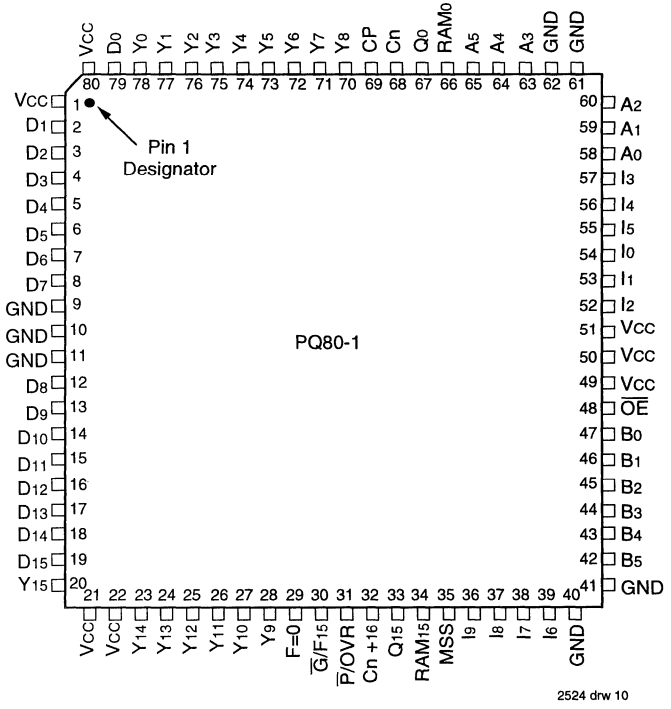
The IDT49C402s are fabricated using CMOS technology designed for high performance and high reliability. These performance-enhanced devices feature both bipolar speed and bipolar output drive capabilities, while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

FUNCTIONAL BLOCK DIAGRAM



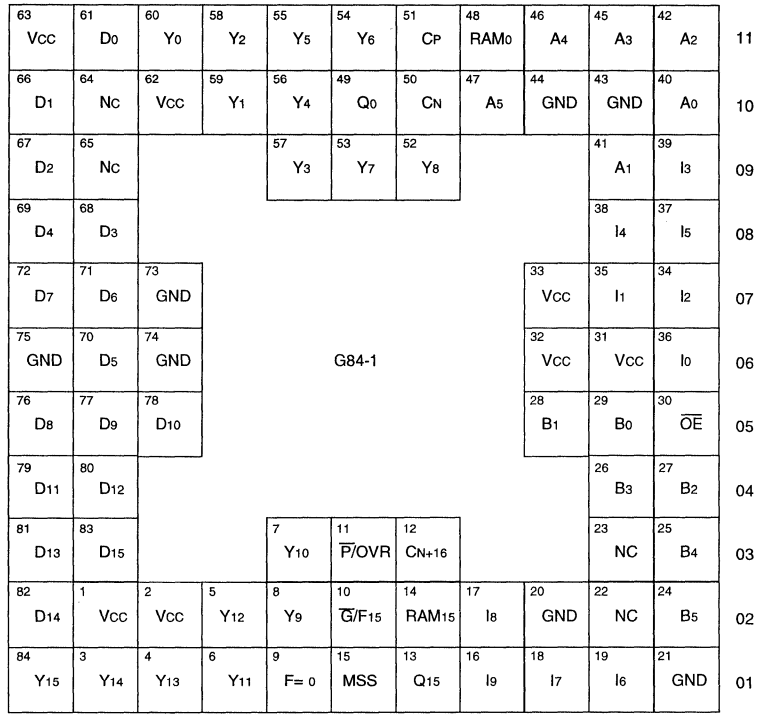


FINE PITCH FLATPACK
TOP VIEW



2524 drw 10

PQFP
TOP VIEW



PGA
TOP VIEW

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PIN DESCRIPTIONS

Pin Name	I/O	Description
A_0 - A_5	I	Six address inputs to the register file which selects one register and displays its contents through the A port.
B_0 - B_5	I	Six address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW.
I_0 - I_9	I	Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0, 1, 2)}$, what function the ALU will perform $I_{(3, 4, 5)}$ and what data is deposited in the Q Register or the register file $I_{(6, 7, 8, 9)}$. Original 2901 destinations are selected if I_9 is disconnected in this mode, proper I_9 bias is achieved by an external pullup resistor to V_{CC} (47K ohms recommended).
D_0 - D_{15}	I	Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. D_0 is the LSB.
Y_0 - Y_{15}	O	Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{(6, 7, 8, 9)}$.
$\overline{G}/F_{15}$	O	A multipurpose pin which indicates the carry generate ($\overline{G}$) function at the least significant and intermediate slices or as F_{15}, the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by the MSS pin. If MSS = HIGH, F_{15} is enabled. If MSS = LOW, $\overline{G}$ is enabled.
F = 0	O	Open drain output which goes HIGH if the F_0 - F_{15} ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+16}	O	Carry-out of the ALU.
Q_{15} RAM_{15}	I/O	Bidirectional lines controlled by $I_{(6, 7, 8, 9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6, 7, 8, 9)}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q_{15} pin and the MSB of the ALU output is available on the RAM_{15} pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_{15} and RAM_{15} lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{P}$/OVR	O	A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled.
CP	I	The clock input LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64 x 16 RAM. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.
MSS	I	When HIGH, enables OVR and F_{15} on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to V_{CC} provides declaration that the device is the most significant slice.

2524 tbl 01

11

DEVICE ARCHITECTURE

The IDT49C402 CMOS bit-slice microprocessor is configured sixteen bits wide and is cascadable to any number of bits (16, 32, 48, 64). Key elements which make up this 16-bit microprocessor slice are the 1) register file (64 x 16 dual-port RAM) with shifter 2) ALU and 3) Q Register and shifter.

REGISTER FILE — A 16-bit data word from one of the 64 RAM registers can read from the A port as selected by the 6-bit A address field. Simultaneously, the same data word, or any other word from the 64 RAM registers, can be read from the B port as selected by the 6-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A port and B port during the clock (CP) LOW time, eliminating any data races. During clock HIGH, these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involves the RAM_{15} and RAM_0 I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled RAM_{15} I/O output, while the RAM_0 I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled RAM_0 I/O output, while the RAM_{15} I/O input is selected as the input to the MSB.

ALU — The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having a zero source operand. Both multiplexers are controlled by the $I_{(0, 1, 2)}$ inputs. This multiplexer configuration enables the user to select the various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3, 4, 5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in (C_n), carry-out (C_{n+16}) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}/OVR$ are aimed at accelerating arithmetic operations. For intermediate and least significant slices, the MSS pin is programmed LOW, selecting the carry-generate ($\overline{G}$) and carry propagate ($\overline{P}$) output functions to be used by carry lookahead logic. For the most significant slice, MSS is programmed HIGH, selecting the sign-bit (F_{15}) and the two's complement overflow (OVR) output functions. The sign bit (F_{15}) allows the ALU sign bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign bit, as logically determined from the Exclusive-OR of the carry-in and carry-out of the most significant bit of the ALU. The ALU data outputs are available at the three-state outputs $Y_{(0\text{-}15)}$ or as inputs to the RAM register file and Q register under control of the $I_{(6, 7, 8, 9)}$ instruction inputs.

Q REGISTER — The Q Register is a separate 16-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift up or shift down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_{15}, which operate comparably to the RAM shifter. They are controlled by the $I_{(6, 7, 8, 9)}$ inputs.

The clock input of the IDT49C402 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW- to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6, 7, 8, 9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

ALU SOURCE OPERAND CONTROL

Mnemonic	Microcode I_2	I_1	I_0	Octal Code	ALU Source Operands R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

2524 tbl 02

ALU FUNCTION CONTROL

Mnemonic	Microcode I_2	I_1	I_0	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S – R
SUBS	L	H	L	2	R Minus S	R – S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX-OR S	R ∇ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \nabla S}$

2524 Tbl 04

ALU ARITHMETIC MODE FUNCTIONS

Octal $I_{5,4,3}$	Octal $I_{2,1,0}$	C_n = L Group	C_n = L Function	C_n = H Group	C_n = H Function
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q – 1	PASS	Q
1	3		B – 1		B
1	4		A – 1		A
2	7		D – 1		D
2	2	1's Comp.	–Q – 1	2's Comp. (Negate)	–Q
2	3		–B – 1		–B
2	4		–A – 1		–A
1	7		–D – 1		–D
1	0	Subtract (1's Comp)	Q – A – 1	Subtract (2's Comp)	Q – A
1	1		B – A – 1		B – A
1	5		A – D – 1		A – D
1	6		Q – D – 1		Q – D
2	0		A – Q – 1		A – Q
2	1		A – B – 1		A – B
2	5		D – A – 1		D – A
2	6		D – Q – 1		D – Q

2524 tbl 03

ALU LOGIC MODE FUNCTIONS

Octal $I_{5,4,3}$	Octal $I_{2,1,0}$	Group	Function
4	0	AND	A ∧ Q
4	1		A ∧ B
4	5		D ∧ A
4	6		D ∧ Q
3	0	OR	A ∨ Q
3	1		A ∨ B
3	5		D ∨ A
3	6		D ∨ Q
6	0	EX–OR	A ∇ Q
6	1		A ∇ B
6	5		D ∇ A
6	6		D ∇ Q
7	0	EX–NOR	$\overline{A \nabla Q}$
7	1		$\overline{A \nabla B}$
7	5		$\overline{D \nabla A}$
7	6		$\overline{D \nabla Q}$
7	2	INVERT	$\overline{Q}$
7	3		$\overline{B}$
7	4		$\overline{A}$
7	7		$\overline{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\overline{A}$ ∧ Q
5	1		$\overline{A}$ ∧ B
5	5		$\overline{D}$ ∧ A
5	6		$\overline{D}$ ∧ Q

2524 Tbl 05

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SOURCE OPERAND AND ALU FUNCTION MATRIX (1)

Octal $I_{5,4,3}$	ALU Function	$I_{2,1,0}$ Octal 0 — ALU Source A, Q	1 — A, B	2 — 0, Q	3 — 0, B	4 — 0, A	5 — D, A	6 — D, Q	7 — D, 0
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q – A – 1 Q – A	B – A – 1 B – A	Q – 1 Q	B – 1 B	A – 1 A	A – D – 1 A – D	Q – D – 1 Q – D	–D – 1 –D
2	C_n = L R Minus S C_n = H	A – Q – 1 A – Q	A – B – 1 A – B	–Q – 1 –Q	–B – 1 –B	–A – 1 –A	D – A – 1 D – A	D – Q – 1 D – Q	D – 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∇ Q	A ∇ B	Q	B	A	D ∇ A	D ∇ Q	D
7	R EX-NOR S	$\overline{A \nabla Q}$	$\overline{A \nabla B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \nabla A}$	$\overline{D \nabla Q}$	$\overline{D}$

2524 Tbl 06

NOTE:
1. + = Plus; – = Minus; ∧ = AND; ∇ = EX-OR; ∨ = OR.

ALU DESTINATION CONTROL(1)

Mnemonic	Microcode I_9	I_8	I_7	I_6	Hex Code	RAM Function Shift	RAM Function Load	Q Register Function Shift	Q Register Function Load	Y Output	RAM Shifter RAM_0	RAM Shifter RAM_{15}	Q Shifter Q_0	Q Shifter Q_{15}	
OREG	H	L	L	L	8	X	NONE	NONE	F → Q	F	X	X	X	X	Existing 2901
NOP	H	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X	Functions
RAMA	H	L	H	L	A	NONE	F → B	X	NONE	A	X	X	X	X	
RAMF	H	L	H	H	B	NONE	F → B	X	NONE	F	X	X	X	X	
RAMQD	H	H	L	L	C	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_{15}	Q_0	IN_{15}	
RAMD	H	H	L	H	D	DOWN	F/2 → B	X	NONE	F	F_0	IN_{15}	Q_0	X	
RAMQU	H	H	H	L	E	UP	2F → B	UP	2Q → Q	F	IN_0	F_{15}	IN_0	Q_{15}	
RAMU	H	H	H	H	F	UP	2F → B	X	NONE	F	IN_0	F_{15}	X	Q_{15}	
DFF	L	L	L	L	0	NONE	D → B	NONE	F → Q	F	X	X	X	X	New Added
DFA	L	L	L	H	1	NONE	D → B	NONE	F → Q	A	X	X	X	X	IDT49C402
FDF	L	L	H	L	2	NONE	F → B	NONE	D → Q	F	X	X	X	X	Functions
FDA	L	L	H	H	3	NONE	F → B	NONE	D → Q	A	X	X	X	X	
XQDF	L	H	L	L	4	X	NONE	DOWN	Q/2 → Q	F	X	X	Q_0	IN_{15}	
DXF	L	H	L	H	5	NONE	D → B	X	NONE	F	X	X	Q_0	X	
XQUF	L	H	H	L	6	X	NONE	UP	2Q → Q	F	X	X	IN_0	Q_{15}	
XDF	L	H	H	H	7	X	NONE	NONE	D → Q	F	X	X	X	Q_{15}	

2524 tbl 07

NOTE:
1. X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the impedance state.
   B = Register Addressed by B inputs.
   UP is toward MSB; DOWN is toward LSB.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2524 tbl 08

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2524 tbl 09

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–0.1	–5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA MIL.	2.4	4.3	–	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8mA MIL.	–	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 10mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	–0.1	–10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V (3)		–15	–30	–70	mA

NOTES: 2524 tbl 10

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.

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DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQH}	Quiescent Power Supply Current	V_{CC} = Max.	MIL.	–	–	10	mA
	CP = H (CMOS Inputs)	V_{IH} = V_{CC}, V_{IL} = 0V	COM'L.	–	–	10	
		f_{CP} = 0, CP = H					
I_{CCQL}	Quiescent Power Supply Current	V_{CC} = Max.	MIL.	–	–	10	mA
	CP = L (CMOS Inputs)	V_{IH} = V_{CC}, V_{IL} = 0V	COM'L.	–	–	10	
		f_{CP} = 0, CP = L					
I_{CCT}	Quiescent Input Power Supply[6]	V_{CC} = Max., V_{IH} = 3.4V, f_{CP} = 0	MIL.	–	–	1.5	mA/
	Current (per Input @ TTL High)		COM'L.	–	–	0.85	Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max.	MIL.	–	–	7.5	mA/
		V_{IH} = V_{CC}, V_{IL} = 0V	COM'L.	–	–	4.5	MHz
		Outputs Open, $\overline{OE}$ = L					
I_{CC}	Total Power Supply Current[7]	V_{CC} = Max.., f_{CP} = 10MHz	MIL.	–	–	85	mA
		Outputs Open, $\overline{OE}$ = L	COM'L.	–	–	55	
		CP = 50 % Duty cycle					
		V_{IH} = V_{CC}, V_{IL} = 0V					
		V_{CC} = Max.., f_{CP} = 10MHz	MIL.	–	–	130	
		Outputs Open, $\overline{OE}$ = L	COM'L.	–	–	95	
		CP = 50 % Duty cycle					
		V_{IH} = 3.4V, V_{IL} = 0.4V					

2524 tbl 11

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. Guaranteed by design, not production tested.
6. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
7. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   I_{CC} = I_{CCQH} (CD_H) +I_{CCQL} (1 – CD_H) + I_{CCT} (N_T x D_H) + I_{CCD} (f_{CP} /2 +fiNi)
   CD_H = Clock duty cycle high period
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{CP} = Clock input frequency
   I_{CCT} = Quiescent Power Supply Current for TTL level inputs
   I_{CCD} =Dynamic Power Supply Current in mA/MHz
   fi =Input frequency
   Ni =Number of inputs switching

AC ELECTRICAL CHARACTERISTICS IDT49C402

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402 over the –55°C to +125°C and 0°C to +70°C temperature ranges. V_{CC} is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil. (6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	50	48	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)	20	21	MHz
Minimum Clock LOW Time	30	25	ns
Minimum Clock HIGH Time	20	20	ns
Minimum Clock Period	50	48	ns

2524 tbl 13

MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

	To Output																
From Input	Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	52	47	47	42	52	47	47	42	38	34	52	47	44	40	–	–	ns
D	35	32	34	31	35	32	34	31	27	25	35	32	28	26	–	–	ns
C_n	29	26	–	–	29	26	27	25	20	18	29	26	23	21	–	–	ns
$I_{0, 1, 2}$	41	37	30	27	41	37	38	35	29	26	41	37	30	27	–	–	ns
$I_{3, 4, 5}$	40	36	28	26	40	36	37	34	27	25	40	36	28	26	–	–	ns
$I_{6, 7, 8, 9}$	26	24	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	42	38	41	37	42	38	41	37	30	27	42	38	41	37	25	23	ns

2524 tbl 14

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		
Input	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Source Address	20	18	2 (3)	1 (3)	50 (4)	50 (4)	2	1	ns
B Destination Address	20	18	Do not change (2)				2	1	ns
D	– (1)	–	–	–	30/40 (5)	26/36 (5)	2	1	ns
C_n	–	–	–	–	35	32	0	0	ns
$I_{0, 1, 2}$	–	–	–	–	45	41	0	0	ns
$I_{3, 4, 5}$	–	–	–	–	45	41	0	0	ns
$I_{6, 7, 8, 9}$	12	11	Do not change (2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	11	0	0	ns

2524 tbl 15

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

AC ELECTRICAL CHARACTERISTICS IDT49C402A

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402A over the –55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.(6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)(6)	23	22	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)(6)	35	41	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period(6)	36	31	ns

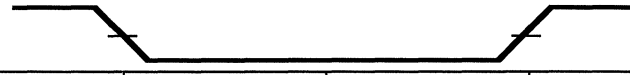
2524 tbl 16

MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

From Input	To Output: Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Address	41	37	39	35	41	37	41	37	37	34	41	37	40	36	–	–	ns
D	32	29	29	26	29	26	31	28	27	25	32	29	28	26	–	–	ns
C_n	28	25	–	–	26	24	25	23	20	18	29	26	23	21	–	–	ns
$I_{0,1,2}$	35	32	30	27	35	32	34	31	29	26	35	32	30	27	–	–	ns
$I_{3,4,5}$	35	32	28	26	34	31	34	31	27	25	35	32	28	26	–	–	ns
$I_{6,7,8,9}$	25	23	–	–	–	–	–	–	–	–	–	–	20	18	20	18	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	30	27	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ↓	34	31	31	28	33	30	34	31	30	27	34	31	34	31	25	23	ns

2524 tbl 17

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	11	10	2 (3)	1 (3)	25 (4)	21 (4)	2	1	ns
B Destination Address	11	10	Do not change (2)				2	1	ns
D	– (1)	–	–	–	12/22 (5)	10/20 (5)	2	1	ns
C_n	–	–	–	–	17	15	0	0	ns
$I_{0,1,2}$	–	–	–	–	28	25	0	0	ns
$I_{3,4,5}$	–	–	–	–	28	25	0	0	ns
$I_{6,7,8,9}$	11	10	Do not change (2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	11	0	0	ns

2524 tbl 18

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

AC ELECTRICAL CHARACTERISTICS IDT49C402B

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT49C402B over the –55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.(6)	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)(6)	22	19	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)(6)	52	60	MHz
Minimum Clock LOW Time	11	9	ns
Minimum Clock HIGH Time	11	9	ns
Minimum Clock Period(6)	24	20	ns

2524 tbl 19

MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

From Input	To Output: Y		(MSS = L) $\overline{G}$, $\overline{P}$		(MSS = H) F_{15}		(MSS = H) OVR		C_{n+16}		F = 0		RAM_0 RAM_{15}		Q_0 Q_{15}		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Address	33	28	31	26	31	28	31	28	28	26	31	28	32	29	–	–	ns
D	26	23	23	21	23	21	25	22	22	20	26	23	24	23	–	–	ns
C_n	22	20	–	–	20	18	19	17	15	14	22	20	18	17	–	–	ns
$I_{0,1,2}$	28	26	24	22	28	26	27	25	23	21	28	26	26	24	–	–	ns
$I_{3,4,5}$	28	26	22	21	27	25	27	25	22	20	28	26	25	23	–	–	ns
$I_{6,7,8,9}$	20	18	–	–	–	–	–	–	–	–	–	–	16	14	16	14	ns
A Bypass ALU (I = AXX, 1XX, 3XX)	24	22	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ↓	27	25	25	22	26	24	27	25	25	22	27	25	27	25	20	18	ns

2524 tbl 20

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	10	9	2 (3)	1 (3)	20 (4)	18 (4)	2	1	ns
B Destination Address	10	9	Do not change(2)				2	1	ns
D	– (1)	–	–	–	12/22(5)	10/20(5)	2	1	ns
C_n	–	–	–	–	16	14	0	0	ns
$I_{0,1,2}$	–	–	–	–	26	24	0	0	ns
$I_{3,4,5}$	–	–	–	–	26	24	0	0	ns
$I_{6,7,8,9}$	10	9	Do not change(2)				0	0	ns
$RAM_{0,15}$, $Q_{0,15}$	–	–	–	–	12	10	0	0	ns

2524 tbl 21

NOTES:

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

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IDT49C402B
MAX. OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at C_L = 50pF, correlated to 5pF

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	18	16	15	13

2524 tbl 22

IDT49C402A
MAX. OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at C_L = 50pF, correlated to 5pF

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	22	20	20	18

2524 tbl 23

IDT49C402
MAX. OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)
Tested at C_L = 50pF, correlated to 5pF

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	25	23	25	23

2524 tbl 24

CRITICAL SPEED PATH ANALYSIS

Critical speed paths for the IDT49C402B versus the equivalent bipolar circuit implementation using four 2901Cs and one 2902A are shown below.

The IDT49C402B operates faster than the theoretically achievable values of the discrete bipolar implementation. Actual speed values for the discrete bipolar circuit will increase due to on-chip/off-chip circuit board delays.

TIMING COMPARISION: IDT49C402B vs 2901C w/2902A

16–Bit µP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402B	28	23	31	25	ns
Speed Savings	43	48	52	55	ns

2524 tbl 26

TIMING COMPARISION: IDT49C402A vs 2901C w/2902A

16–Bit µP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402A	37	36	41	25	ns
Speed Savings	34	35	42.5	43.5	ns

2524 tbl 27

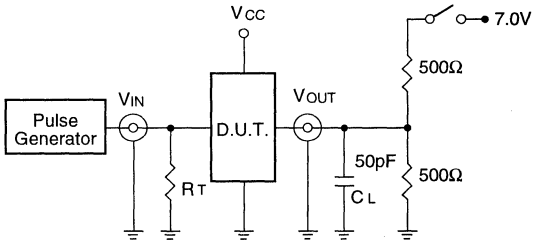
TIMING COMPARISION: IDT49C402 vs 2901C w/2902A

16–Bit µP System	Data Path (Com'l.)		Data Path (Mil.)		Unit
	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	AB ADDR → F = 0	AB ADDR → $RAM_{0, 15}$	
Four 2901Cs + 2902A	≥ 71	≥ 71	≥ 83.5	≥ 83.5	ns
IDT49C402A	47	40	52	44	ns
Speed Savings	24	31	31.5	39.5	ns

2524 tbl 28

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2524 drw 05

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

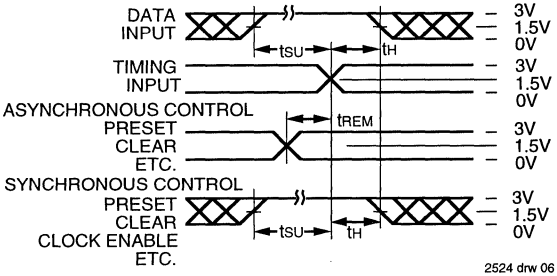
2524 lnk 25

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

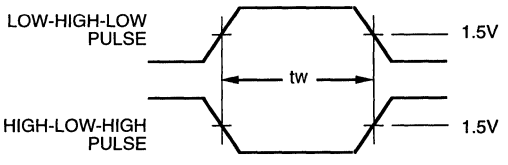
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



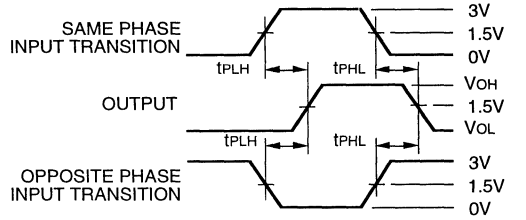
2524 drw 06

PULSE TIMES



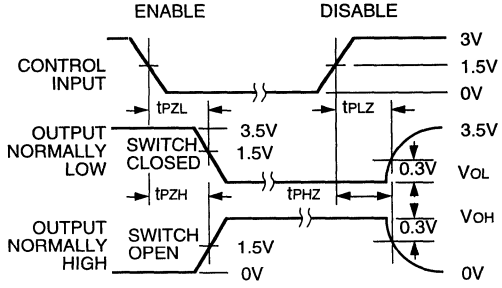
2524 drw 07

PROPAGATION DELAY



2524 drw 08

ENABLE AND DISABLE TIMES



2524 drw 10

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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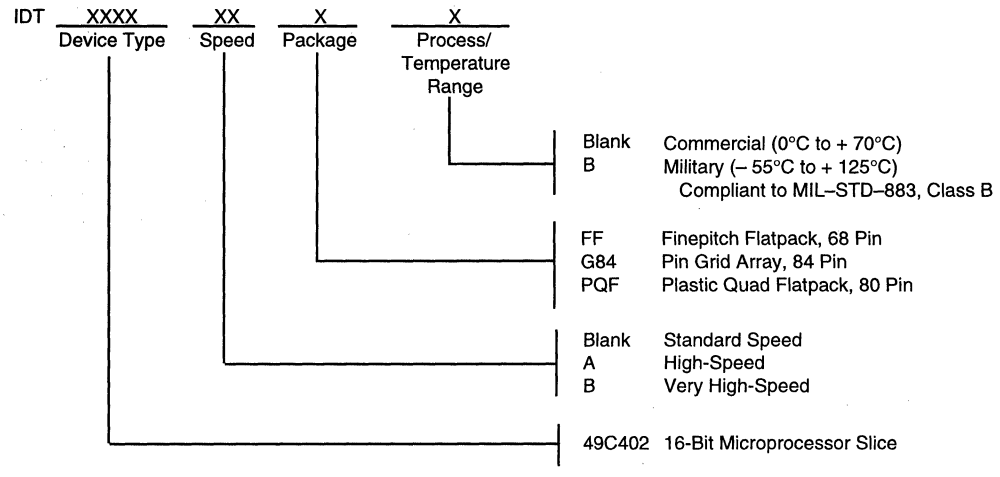
ORDERING INFORMATION



2524 drw 09

Integrated Device Technology, Inc.

16 x 16 PARALLEL CMOS MULTIPLIER-ACCUMULATOR

IDT7210L

FEATURES:

- 16 x 16 parallel multiplier-accumulator with selectable accumulation and subtraction
- High-speed: 20ns multiply-accumulate time
- IDT7210 features selectable accumulation, subtraction, rounding and preloading with 35-bit result
- IDT7210 is pin and function compatible with the TRW TDC1010J, TMC2210, Cypress CY7C510, and AMD AM29510
- Performs subtraction and double precision addition and multiplication
- Produced using advanced CMOS high-performance technology
- TTL-compatible
- Available in topbraze DIP, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88733 is listed on this function
- Speeds available:
  Commercial: L20/25/35/45/55/65
  Military: L25/30/40/55/65/75

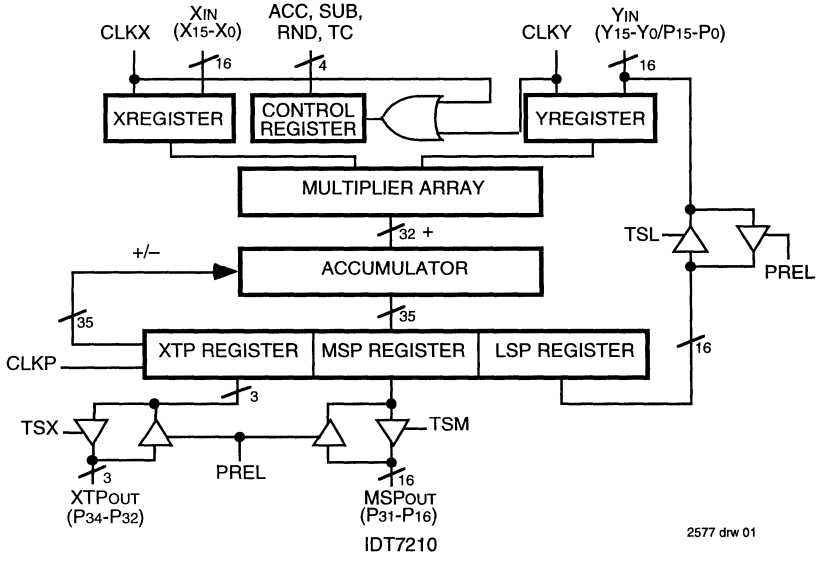
DESCRIPTION:

The IDT7210 is a high-speed, low-power 16 x 16-bit parallel multiplier-accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using CMOS silicon gate technology, this device offers a very low-power alternative to existing bipolar and NMOS counterparts, with only 1/7 to 1/10 the power dissipation and exceptional speed (25ns maximum) performance.

A pin and functional replacement for TRW's TDC1010J the IDT7210 operates from a single 5 volt supply and is compatible with standard TTL logic levels. The architecture of the IDT7210 is fairly straightforward, featuring individual input and output registers with clocked D-type flip-flop, a preload capability which enables input data to be preloaded into the output registers, individual three-state output ports for the Extended Product (XTP) and Most Significant Product (MSP) and a Least Significant Product output (LSP) which is multiplexed with the Y input.

The X_{IN} and Y_{IN} data input registers may be specified through the use of the Two's Complement input (TC) as either a two's complement or an unsigned magnitude, yielding a full-precision 32-bit result that may be accumulated to a full 35-bit result. The three output registers – Extended Product (XTP), Most Most Significant Product (MSP) and Least Significant Product (LSP) – are controlled by the respective TSX, TSM and TSL input lines. The LSP output can be routed through Y_{IN} ports.

FUNCTIONAL BLOCK DIAGRAM



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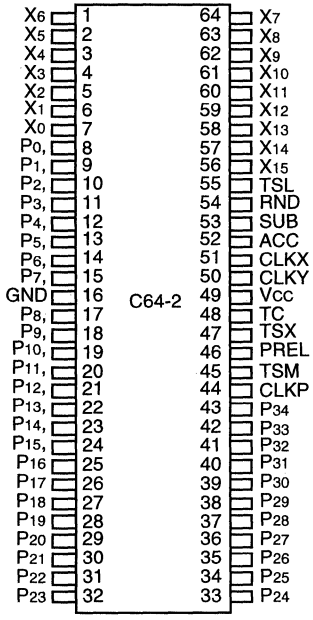
DESCRIPTION (Continued)

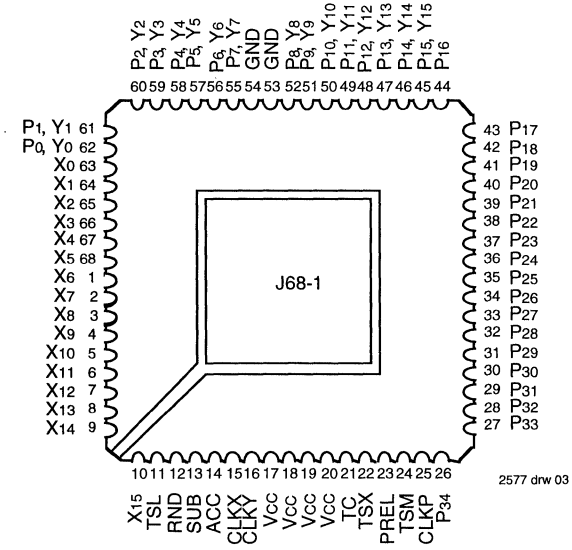
The Accumulate input (ACC) enables the device to perform either a multiply or a multiply-accumulate function. In the multiply-accumulate mode, output data can be added to or subtracted from previous results. When the Subtraction (SUB) input is active simultaneously with an active ACC, a subtraction can be performed. The double precision accumulated result is rounded down to either a single precision or single precision plus 3-bit extended result. In the multiply mode, the Extended Product output (XTP) is sign extended in the two's complement mode or set to zero in the unsigned mode. The Round (RND) control rounds up the Most Significant Product (MSP) and the 3-bit Extended Product (XTP) outputs. When Preload input (PREL) is active, all the output buffers are forced into a high-impedance state (see Preload truth table) and external data can be loaded into the output register by using the TSX, TSL and TSM signals as input controls.

PIN CONFIGURATIONS



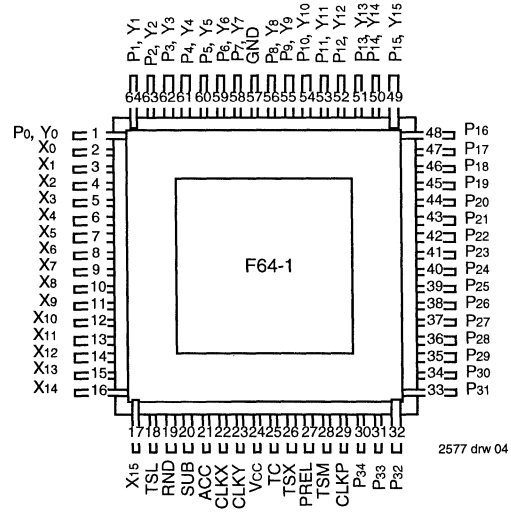
2577 drw 02

DIP
TOP VIEW



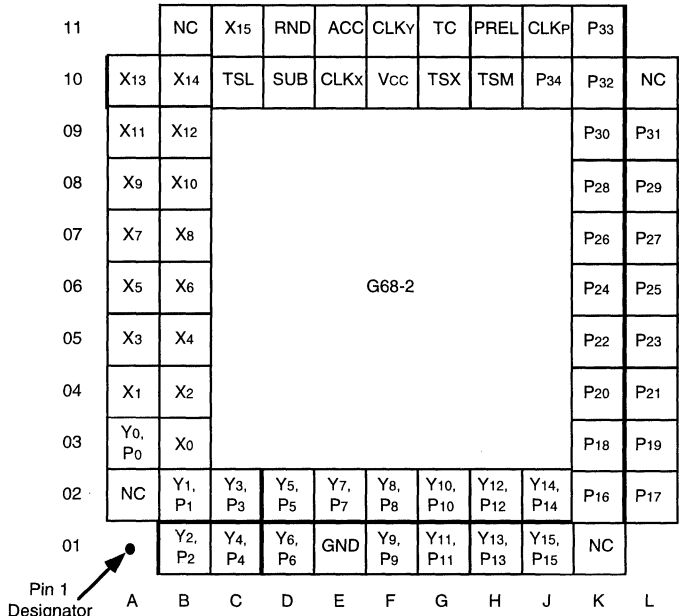
2577 drw 03

PLCC
TOP VIEW



2577 drw 04

FLATPACK
TOP VIEW



PGA
TOP VIEW

2577 drw 05

PIN DESCRIPTIONS

Pin Name	I/O	Description
X_{0-15}	I	Data Inputs
Y_{0-15}/ P_{0-15}	I/O	Multiplexed I/O port. Y_{0-15} are data inputs and can be used to preload LSP register on PREL = 1. P_{0-15} are LSP register outputs - enabled by TSL.
P_{16-31}	I/O	MSP register outputs - enabled by TSM. MSP register can be preloaded when PREL = 1.
P_{32-34}	I/O	XTP register outputs - enabled by TSX. XTP register can be preloaded through these inputs when PREL = 1.
CLKX	I	Input data X_{0-15} loaded in X input register on CLKX rising edge.
CLKY	I	Input data Y_{0-15} loaded in Y input register on CLKY rising edge.
CLKP	I	Output data loaded into output register on rising edge of CLKP.
TSX	I	TSX = 0 enables XTP outputs, TSX = 1 tristates P_{32-34} lines.
TSM	I	TSM = 0 enables MSP outputs, TSM = 1 tristates P_{16-31} lines.
TSL	I	TSL = 0 enables LSP outputs, TSL = 1 tristates P_{0-15} lines.
PREL	I	When PREL= 1 data is input on P_{0-15} lines. When PREL = 0, inputs on these lines are ignored.
ACC	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). When ACC = 1 and SUB = 0 an accumulate operation is performed. When ACC = 1 and SUB = 1, a subtract operation is performed. When ACC = 0, the SUB input is a don't care and the device acts as a simple multipler with no accumulation
SUB	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). This input is active only when ACC = 1. When SUB = 1 the contents of the output register are subtracted from the result and stored back in the output register. When SUB = 0 the contents of the output register are added to the result and stored back in the output register
TC	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). When TC = 1, the X and Y input are assumed to be in two's complement form. When TC = 0, X and Y inputs are assumed to be in unsigned magnitude form
RND	I	This input is loaded into the control register on the rising edge of (CLKX + CLKY). RND is inactive when low. RND = 1, adds a "1" to the most significant bit of the LSP, to round MSP and XTP data

2577 tbl 01

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PRELOAD TRUTH TABLE

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Hi Z
0	0	1	0	Q	Hi Z	Q
0	0	1	1	Q	Hi Z	Hi Z
0	1	0	0	Hi Z	Q	Q
0	1	0	1	Hi Z	Q	Hi Z
0	1	1	0	Hi Z	Hi Z	Q
0	1	1	1	Hi Z	Hi Z	Hi Z
1	0	0	0	Hi Z	Hi Z	Hi Z
1	0	0	1	Hi Z	Hi Z	PL
1	0	1	0	Hi Z	PL	Hi Z
1	0	1	1	Hi Z	PL	PL
1	1	0	0	PL	Hi Z	Hi Z
1	1	0	1	PL	Hi Z	PL
1	1	1	0	PL	PL	Hi Z
1	1	1	1	PL	PL	PL

NOTES: 2577 tbl 02

Hi Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
PL = Output buffers at high impedance or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

NOTES ON TWO'S COMPLEMENT FORMATS

1. In two's complement notation, the location of the binary point that signifies the separation of the fractional and integer fileds is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer filed is provided to extend the utility of the accumulator. In the case of the output rotation, the output binary point is located between the2^0 and 2^1 bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number filed can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.
2. When in the non-accumulating mode, the first four bits (P_{34} to P_{31}) will all indicate the sign of the product. Additionally, the P_{30} term will also indicate the sign with one exception, when multiplying -1 x -1. With the additional bits that are available in this multiplier, the -1×-1 is a valid operation that yields a +1 product.
3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond that available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 35-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{CC} +0.5V	–0.5 to V_{CC} +0.5V	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2577 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2577 tbl 04

1. This parameter is measured at characterization and not 100%tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	Test Conditions[5]	Commercial			Military			Unit
			Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	
V_{IH}	Input High Voltage	Guaranteed Logic HIGH Level	2.0	—	—	2.0	—	—	V
V_{IL}	Input Low Voltage	Guaranteed Logic LOW Level	—	—	0.8	—	—	0.8	V
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0V to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., Outputs Disabled V_{OUT} = 0 to V_{CC}	—	—	10	—	—	10	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}[4]	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_O GND	-20	—	-100	-20	—	-100	mA
I_{CC}[2]	Operating Power Supply Current	V_{CC} = Max., Outputs Enabled f= 10MHz[2] C_L = 50 pF	—	45	90	—	45	110	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	30	—	20	30	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ –0.2V, $V_{IN} \leq$ 0.2V	—	4	10	—	4	12	mA
I_{CC}/f[2,3]	Increase in Power Supply Current MHz	V_{CC} = Max., Outputs Disabled	—	—	6	—	—	8	mA/ MHz

NOTES:
2577 tbl 05

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 90+ 6(f –10)mA, where f = operating frequency in MHz. For the military range, I_{CC} = 110 + 8(f –10). f = operating frequency in MHz, f = 1/t_{MA}.
3. For frequencies greater than 10MHz, guaranteed by design, not production tested.
4. I_{OL} = 4mA for t_{MA} > 55ns.
5. For conditions shown as Max. or Min., use appropriate value specified under electrical characteristics.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0° to +70°C)

Symbol	Parameter	7210L20		7210L25		7210L35		7210L45		7210L55		7210L65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply-Accumulate Time[2]	2.0	20	2.0	25	2.0	35	2.0	45	2.0	55	2.0	65	ns
t_D	Output Delay[2]	2.0	18	2.0	20	2.0	25	2.0	25	2.0	30	2.0	35	ns
t_{ENA}	3-State Enable Time	—	18	–	20	–	25	–	25	–	30	–	30	ns
t_{DIS}	3-State Disable Time[1]	—	18	–	20	–	25	–	25	–	30	–	30	ns
t_S	Input Register Set-up Time	10	—	12	–	12	–	15	–	20	–	25	–	ns
t_H	Input Register Hold Time	3	—	3	–	3	–	3	–	3	–	3	–	ns
t_{PW}	Clock Pulse Width	9	—	10	–	10	–	15	–	20	–	25	–	ns
t_{HCL}	Relative Hold Time	0	—	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
2577 tbl 06

1. Transition is measured ±500mV from steady state voltage.
2. Minimum delays guaranteed but not tested

AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = –55° to +125°C)

Symbol	Parameter	7210L25		7210L30		7210L40		7210L55		7210L65		7210L75		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MA}	Multiply-Accumulate Time[2]	2.0	25	2.0	30	2.0	40	2.0	55	2.0	65	2.0	75	ns
t_D	Output Delay[2]	2.0	20	2.0	20	2.0	25	2.0	30	2.0	35	2.0	35	ns
t_{ENA}	3-State Enable Time	—	20	–	20	–	25	–	30	–	30	–	35	ns
t_{DIS}	3-State Disable Time[1]	—	20	–	20	–	25	–	25	–	30	–	30	ns
t_S	Input Register Set-up Time	12	—	12	–	15	–	20	–	25	–	25	–	ns
t_H	Input Register Hold Time	3	—	3	–	3	–	3	–	3	–	3	–	ns
t_{PW}	Clock Pulse Width	10	—	10	–	15	–	20	–	25	–	25	–	ns
t_{HCL}	Relative Hold Time	0	—	0	–	0	–	0	–	0	–	0	–	ns

NOTES:
2577 tbl 07

1. Transition is measured ±500mV from steady state voltage.
2. Minimum delays guaranteed but not tested

11

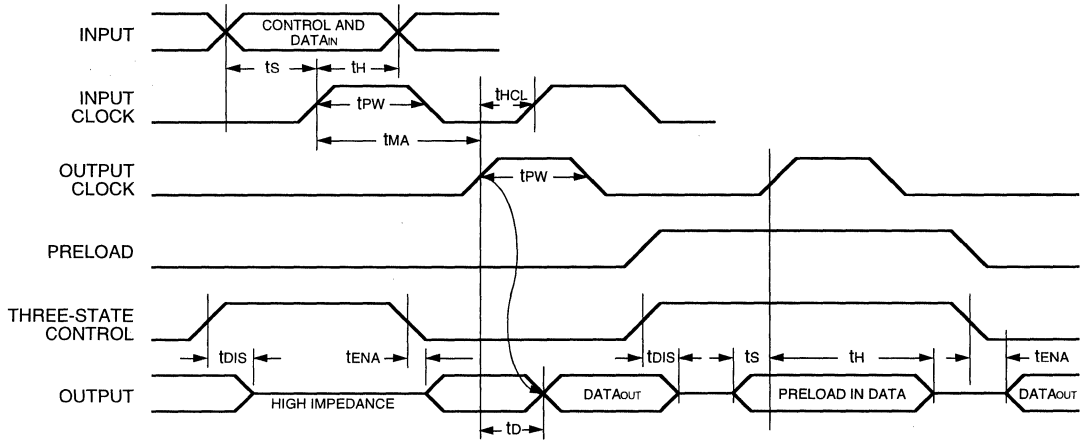


Figure 1. Timing Diagram

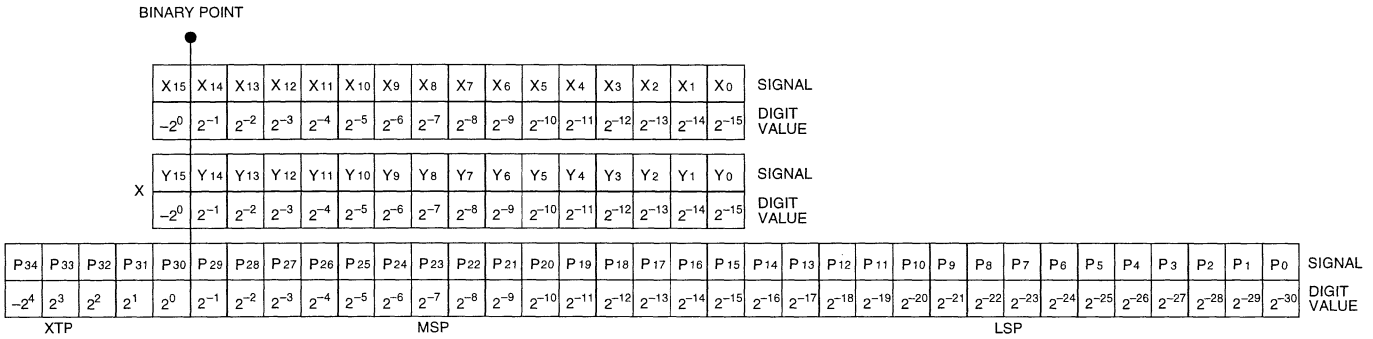


Figure 2. Fractional Two's Complement Notation.

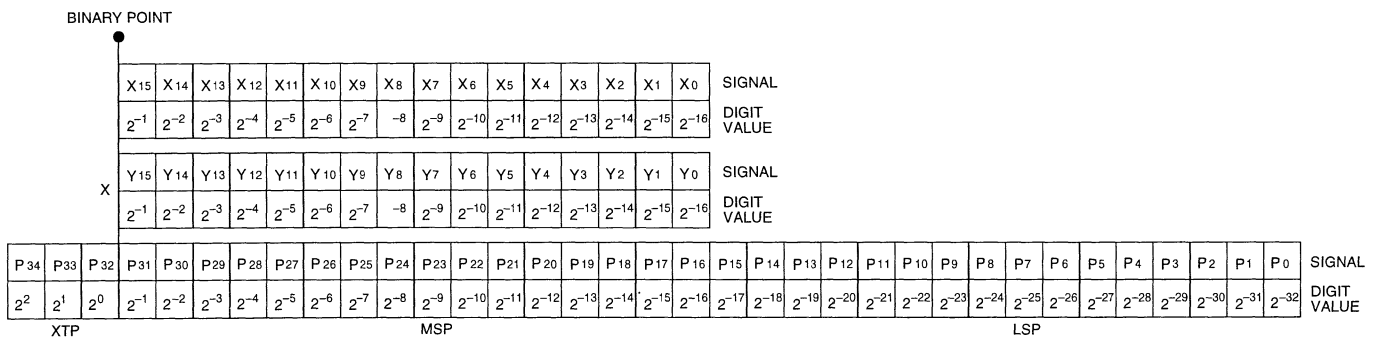


Figure 3. Fractional Unsigned Mgnitude Notation

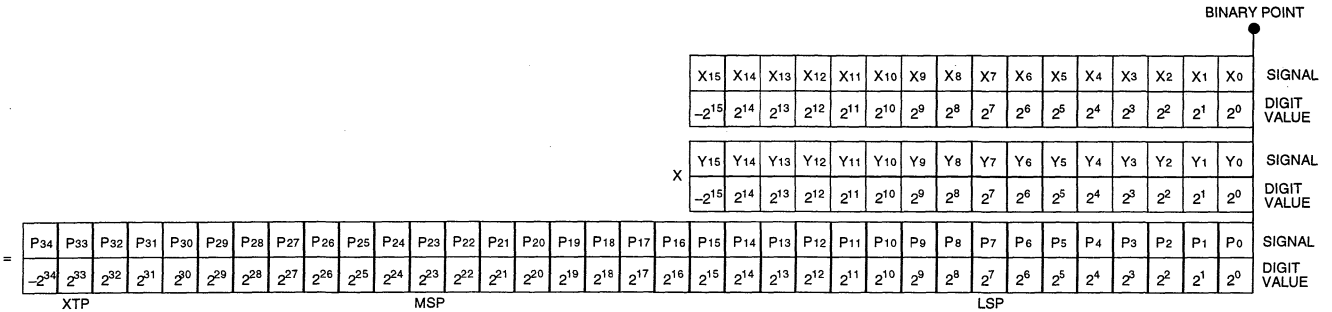


Figure 4. Integer Two's Complement Notation

2577 drw 12

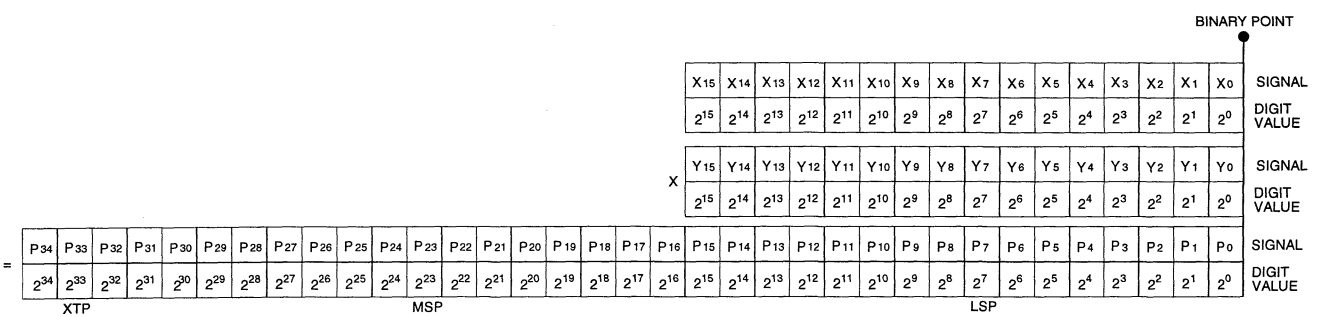
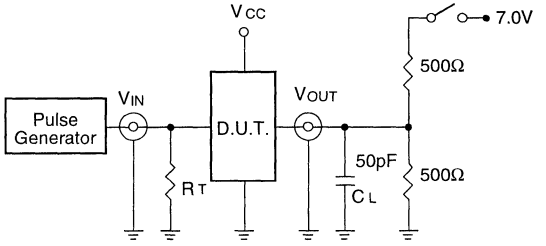


Figure 5. Integer Unsigned Magnitude Notation

2577 drw 13

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2577 drw 06

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

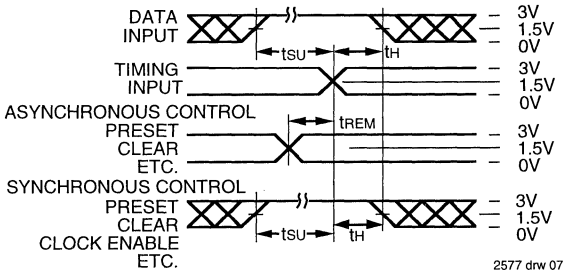
2577 lnk 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

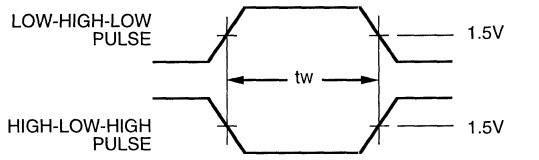
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



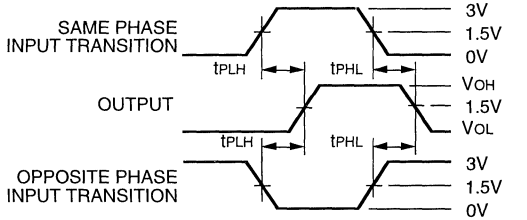
2577 drw 07

PULSE WIDTH



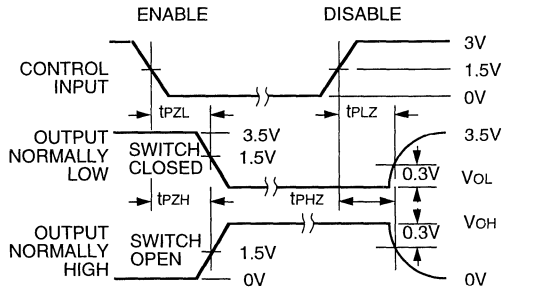
2577 drw 08

PROPAGATION DELAY



2577 drw 09

ENABLE AND DISABLE TIMES



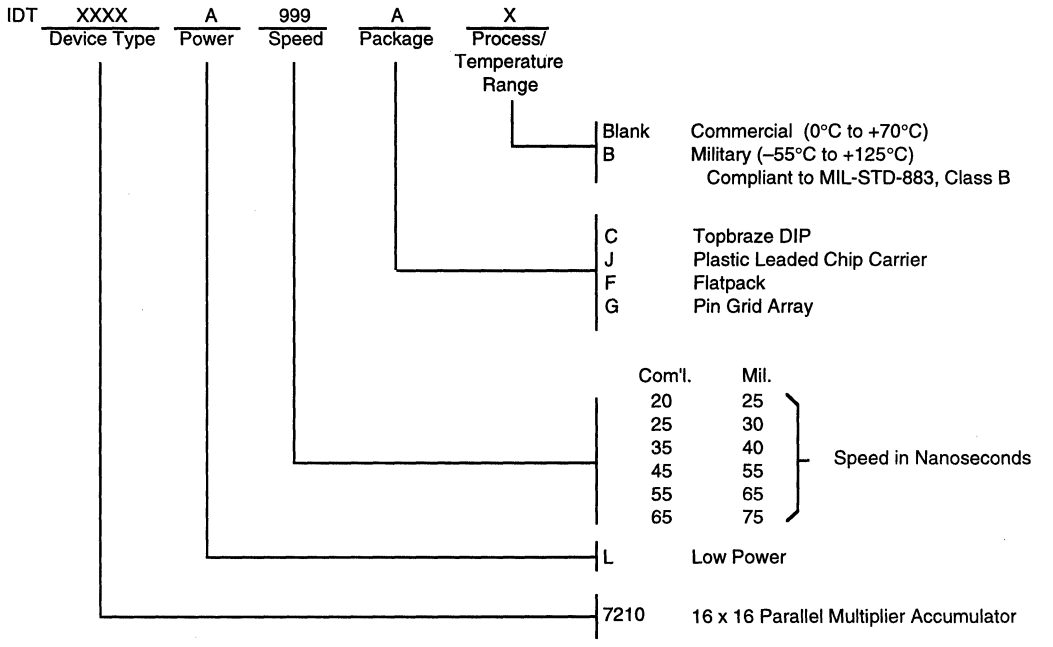
2577 drw 10

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

11

ORDERING INFORMATION



2577 drw 11

Integrated Device Technology, Inc.

16 x 16 PARALLEL CMOS MULTIPLIERS

IDT7216L
IDT7217L

FEATURES:

- 16 x 16 parallel multiplier with double precision product
- 16ns clocked multiply time
- Low power consumption: 120mA
- Produced with advanced submicron CMOS high performance technology
- IDT7216L is pin- and function compatible with TRW MPY016H/K and AMD Am29516
- IDT7217L requires a single clock with register enables making it pin- and function compatible with AMD Am29517
- Configured for easy array expansion
- User-controlled option for transparent output register mode
- Round control for rounding the MSP
- Input and output directly TTL-compatible
- Three-state output
- Available in Top Braze, DIP, PLCC, Flatpack and Pin Grid Array
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86873 is listed on this function for IDT7216 and Standard Military Drawing #5962-87686 is listed for this function for IDT7217.
- Speeds available: Commercial: L16/20/25/35/45/55/65
  Military: L20/25/30/40/55/65/75

DESCRIPTION:

The IDT7216/IDT7217 are high-speed, low-power 16 x 16-bit multipliers ideal for fast, real time digital signal processing applications. Utilization of a modified Booths algorithm and IDT's high-performance, submicron CMOS technology, has achieved speeds comparable to bipolar (20ns max.), at 1/10 the power consumption.

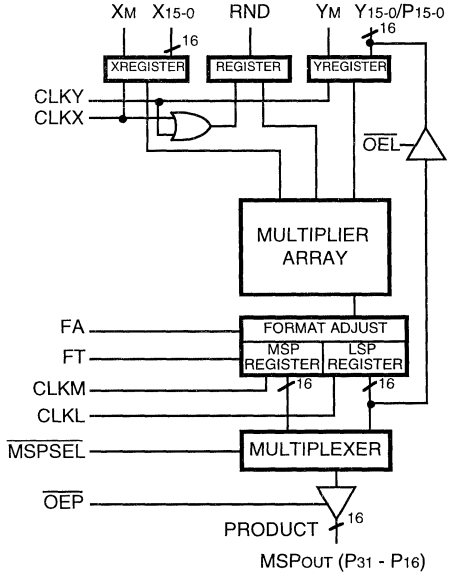
The IDT7216/IDT7217 are ideal for applications requiring high-speed multiplication such as fast Fourier transform analysis, digital filtering, graphic display systems, speech synthesis and recognition and in any system requirement where multiplication speeds of a mini/microcomputer are inadequate.

All input registers, as well as LSP and MSP output registers, use the same positive edge-triggered D-type flip-flop. In the IDT7216, there are independent clocks (CLKX, CLKY, CLKM, CLKL) associated with each of these registers. The IDT7217 has only a single clock input (CLK) and three register enables. $\overline{ENX}$ and $\overline{ENY}$ control the two input registers, while $\overline{ENP}$ controls the entire product.

The IDT7216/IDT7217 offer additional flexibility with the FA control and $\overline{MSPSEL}$ functions. The FA control formats the output for two's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. The

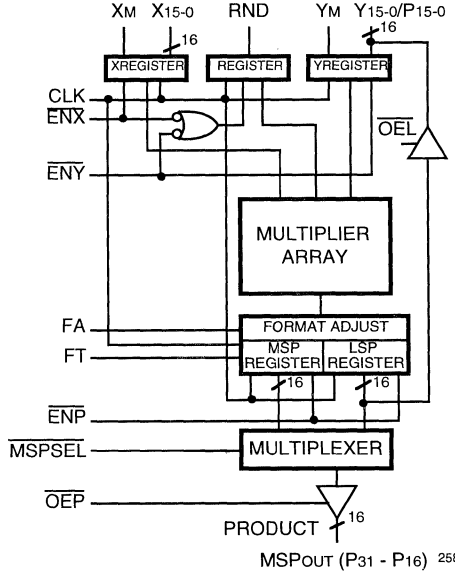
FUNCTIONAL BLOCK DIAGRAMS

IDT7216



2580 drw 01

IDT7217



2580 drw 02

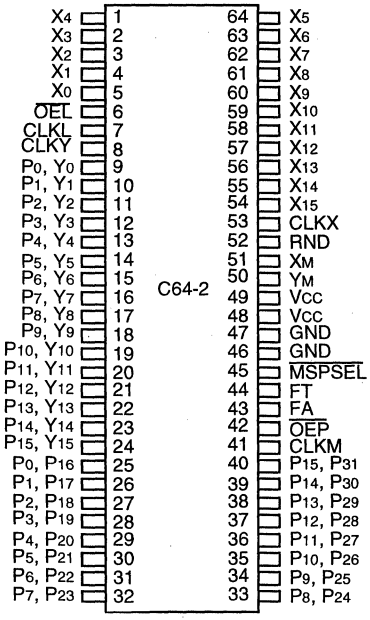
DESCRIPTION (Cont'd.)

$\overline{\text{MSPSEL}}$ low selects the MSP to be available at the product output port, while a high selects the LSP to be available. Keeping this pin low will ensure compatibility with the TRW MPY016H.

The IDT7216/IDT7217 multipliers are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

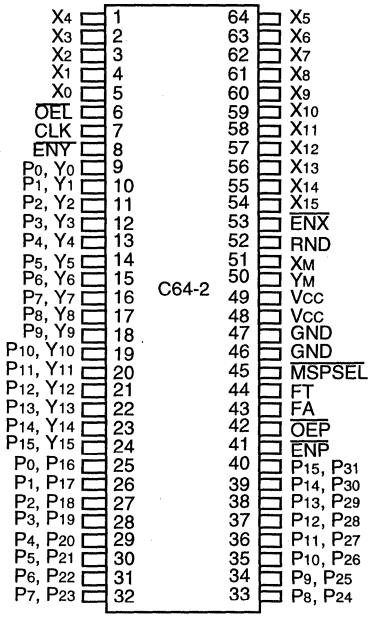
IDT7216



2580 drw 03

64-PIN DIP
TOP VIEW

IDT7217

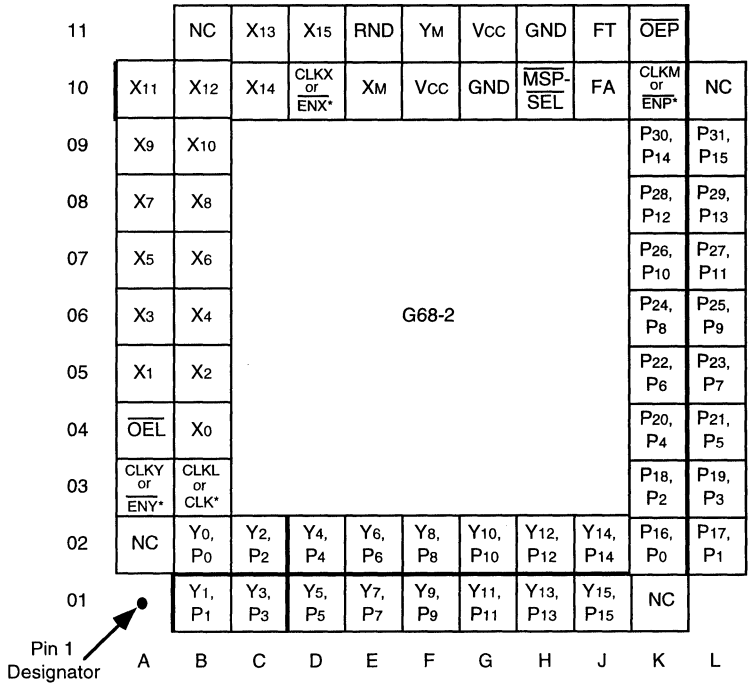


2580 drw 04

64-PIN DIP
TOP VIEW

PIN CONFIGURATIONS (Cont'd.)

IDT7216/IDT7217



*Pin designation for IDT7217

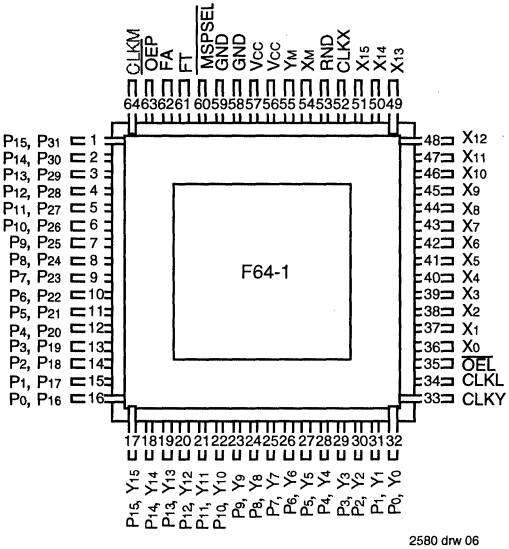
2580 drw 05

PGA
TOP VIEW

11

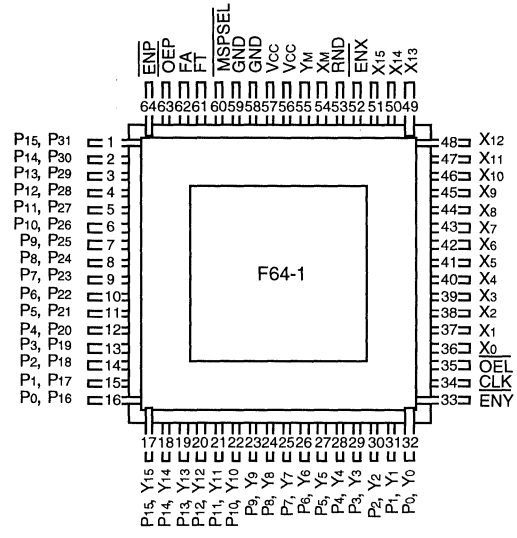
PIN CONFIGURATIONS (Cont'd.)

IDT7216



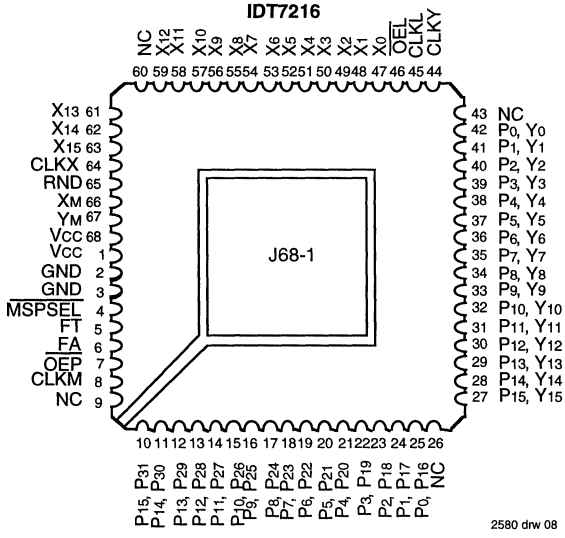
64-LEAD FLATPACK
TOP VIEW

IDT7217



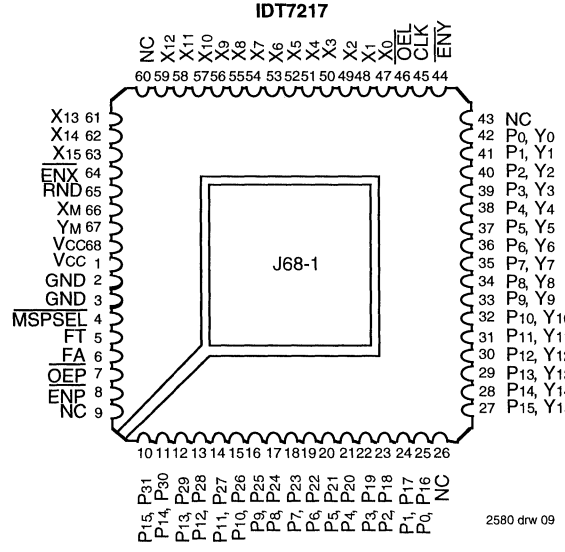
64-LEAD FLATPACK
TOP VIEW

IDT7216



PLCC
TOP VIEW

IDT7217



PLCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
X_0 - X_{15}	I	Data Inputs
Y_0 - Y_{15}/ P_0 - P_{15}	I/O	Y_0 - Y_{15} are data inputs P_0 - P_{15} are LSP register output, enabled when $\overline{OEL}$ = 0
P_{16} - P_{31}	O	Data Output (LSP or MSP)
$\overline{OEL}$	I	Output enable control for LSP (least significant product). When low enables P_0 - P_{15}. When high P_0 - P_{15} tristated.
$\overline{OEP}$	I	Output enable control for MSP (most significant product). When low enables P_{16} - P_{31}. When high P_{16} - P_{31} tristated.
X_M, Y_M	I	Mode control for each data word. Low designates unsigned data input and high designates two's complement.
RND	I	"Round" control for rounding of MSP. When high, 1 is added to the most significant bit of LSP. This signal is affected by the state of FA pin. When FA = 1 and RND = 1, 1 is added to the 2^{-15} bit (P_{15}). When RND = 1 and FA = 0, 1 is added to the 2^{-16} bit (P_{14}). The RND input is registered. It is clocked on the rising edge of the logical OR of CLKX and CLKY in the 7216 and on the rising edge of CLK in the 7217. Rounding always occurs in the positive direction which may introduce a systematic bias.
$\overline{MSPSEL}$	I	When low, MSP is output on P_{16} - P_{31} lines. When high, LSP is output on P_{16} - P_{31}.
FA	I	Format adjust control. When high, a full 32 bit product is selected. When low, a left shifted 31 bit product is selected with the sign bit replicated in the LSP. FA is normally high, except for certain fractional two's complement applications (see multiplier input / output formats).
FT	I	Flow through control. When high, both MSP and LSP registers are by-passed.
CLK	I	7217 X, Y, RND, LSP and MSP register clock input.
CLKX	I	7216 X register clock input. Also clocks RND register.
CLKY	I	7216 Y register clock input. Also clocks RND register.
CLKL	I	7216 LSP register clock input.
CLKM	I	7216 MSP register clock input.
$\overline{ENX}$	I	7217 X register clock enable. Also enables RND register clock.
$\overline{ENY}$	I	7217 Y register clock enable. Also enables RND register clock.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	V_{CC} + 0.5	V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2580 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2580 tbl 04

1. This parameter is measured at characterization and not tested.

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DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	Test Conditions[1]	Commercial			Military			Unit
			Min.	Typ.[1]	Max.	Min.	Typ.[1]	Max.	
V_{IH}	Input High Voltage	Guaranteed Logic High Level	2.0	—	—	2.0	—	—	V
V_{IL}	Input Low Voltage	Guaranteed Logic Low Level	—	—	0.8	—	—	0.8	V
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = 0 to V_{CC}	—	—	10	—	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{OE}$ = 2.0V V_{OUT} = 0 to V_{CC}	—	—	10	—	—	10	µA
I_{CC}	Operating Power Supply Current	V_{CC} = Max., Outputs Disabled f = 10MHz[2]	—	40	80	—	40	100	mA
I_{CCQ1}	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$	—	20	40	—	20	50	mA
I_{CCQ2}	Quiescent Power Supply Current	$V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V	—	4	20	—	4	25	mA
I_{CC}/f[2,3]	Increase in Power Supply Current	V_{CC} = Max., Outputs Disabled	—	—	4	—	—	6	mA/MHz
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –2.0mA	2.4	—	—	2.4	—	—	V
V_{OL}[4]	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_O = GND	-20	—	-120	-20	—	-120	mA

2580 tbl 03

NOTES:

1. Typical implies V_{CC} = 5V and T_A = +25°C.
2. I_{CC} is measured at 10MHz and V_{IN} = 0 to 3V. For frequencies greater than 10MHz, the following equation is used for the commercial range: I_{CC} = 80+ 4(f –10)mA; for the military range, I_{CC} = 100 + 6(f –10). f = operating frequency in MHz, f = 1/t_{MUC} for IDT7216 and f = 1/t_{MC} for IDT7217.
3. For frequencies greater than 10MHz, guaranteed by design, not production tested.
4. I_{OL} = 4mA for t_{MC} >65ns.

AC ELECTRICAL CHARACTERISTICS COMMERCIAL (V_{CC} = 5V ± 10%, T_A = 0° to +70°C)

Symbol	Parameter	7216L16[5] 7217L16		7216L20 7217L20		7216L25 7217L25		7216L35 7217L35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	25	2	30	2	38	2	55	ns
t_{MC}	Clocked Multiply Time[4]	2	16	2	20	2	25	2	35	ns
t_S	X, Y, RND Set-up Time	10	—	11	—	12	—	12	—	ns
t_H	X, Y, RND Hold Time	1	—	1	—	2	—	3	—	ns
t_{PWH}	Clock Pulse Width High	7	—	9	—	10	—	10	—	ns
t_{PWL}	Clock Pulse Width Low	7	—	9	—	10	—	10	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out[4]	2	15	2	18	2	20	2	25	ns
t_{PDP}	Output Clock to P[4]	2	15	2	18	2	20	2	25	ns
t_{PDY}	Output Clock to Y[4]	2	15	2	18	2	20	2	25	ns
t_{ENA}	3-State Enable Time	—	15	—	18	—	20	—	25	ns
t_{DIS}	3-State Disable Time[2]	—	15	—	18	—	20	—	22	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	9	—	10	—	10	—	10	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	0	—	0	—	2	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	0	—	ns

Symbol	Parameter	7216L45 7217L45		7216L55 7217L55		7216L65 7217L65		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	65	2	75	2	85	ns
t_{MC}	Clocked Multiply Time[4]	2	45	2	55	2	65	ns
t_S	X, Y, RND Set-up Time	15	—	20	—	20	—	ns
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	ns
t_{PWH}	Clock Pulse Width High	15	—	15	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	15	—	20	—	20	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out[4]	2	25	2	25	2	30	ns
t_{PDP}	Output Clock to P[4]	2	25	2	30	2	30	ns
t_{PDY}	Output Clock to Y[4]	2	25	2	30	2	30	ns
t_{ENA}	3-State Enable Time	—	25	—	30	—	35	ns
t_{DIS}	3-State Disable Time[2]	—	22	—	25	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	—	10	—	10	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	3	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

NOTES:

2580 tbl 06

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage.
3. Guaranteed by design, not production tested.
4. Minimum propagation delay times are guaranteed, not production tested.
5. This speed is available in PGA and PLCC packages only.

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AC ELECTRICAL CHARACTERISTICS MILITARY (V_{CC} = 5V ± 10%, T_A = –55° to +125°C)

Symbol	Parameter	7216L20[5] 7217L20		7216L25 7217L25		7216L30 7217L30		7216L40 7217L40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	30	2	38	2	43	2	60	ns
t_{MC}	Clocked Multiply Time[4]	2	30	2	25	2	30	2	40	ns
t_S	X, Y, RND Set-up Time	11	—	12	—	12	—	15	—	ns
t_H	X, Y, RND Hold Time	1	—	2	—	2	—	3	—	ns
t_{PWH}	Clock Pulse Width High	9	—	10	—	10	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	9	—	10	—	10	—	15	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out[4]	2	18	2	20	2	20	2	25	ns
t_{PDP}	Output Clock to P[4]	2	18	2	20	2	20	2	25	ns
t_{PDY}	Output Clock to Y[4]	2	18	2	20	2	20	2	25	ns
t_{ENA}	3-State Enable Time	—	18	—	20	—	20	—	25	ns
t_{DIS}	3-State Disable Time[2]	—	20	—	22	—	22	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	10	—	10	—	10	—	12	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	0	—	2	—	2	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	0	—	ns

Symbol	Parameter	7216L55 7217L55		7216L65 7217L65		7216L75 7217L75		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{MUC}	Unclocked Multiply Time[4]	2	75	2	85	2	95	ns
t_{MC}	Clocked Multiply Time[4]	2	55	2	65	2	75	ns
t_S	X, Y, RND Set-up Time	20	—	25	—	25	—	ns
t_H	X, Y, RND Hold Time	3	—	3	—	3	—	ns
t_{PWH}	Clock Pulse Width High	15	—	15	—	15	—	ns
t_{PWL}	Clock Pulse Width Low	15	—	15	—	15	—	ns
t_{PDSEL}	$\overline{MSPSEL}$ to Product Out[4]	2	30	2	35	2	35	ns
t_{PDP}	Output Clock to P[4]	2	30	2	30	2	35	ns
t_{PDY}	Output Clock to Y[4]	2	30	2	30	2	35	ns
t_{ENA}	3-State Enable Time	—	25	—	35	—	40	ns
t_{DIS}	3-State Disable Time[2]	—	25	—	25	—	25	ns
t_S	Clock Enable Set-up Time (IDT7217 only)	15	—	15	—	15	—	ns
t_H	Clock Enable Hold Time (IDT7217 only)	3	—	3	—	3	—	ns
t_{HCL}	Clock Low Hold Time CLKXY Relative to CLKML (IDT7216 only)[1,3]	0	—	0	—	0	—	ns

NOTES:

2580 tbl 07

1. To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.
2. Transition is measured ±500mV from steady state voltage.
3. Guaranteed by design, not production tested.
4. Minimum propagation delay times are guaranteed, not production tested.
5. This speed is available in PGA and Flatpack packages only.

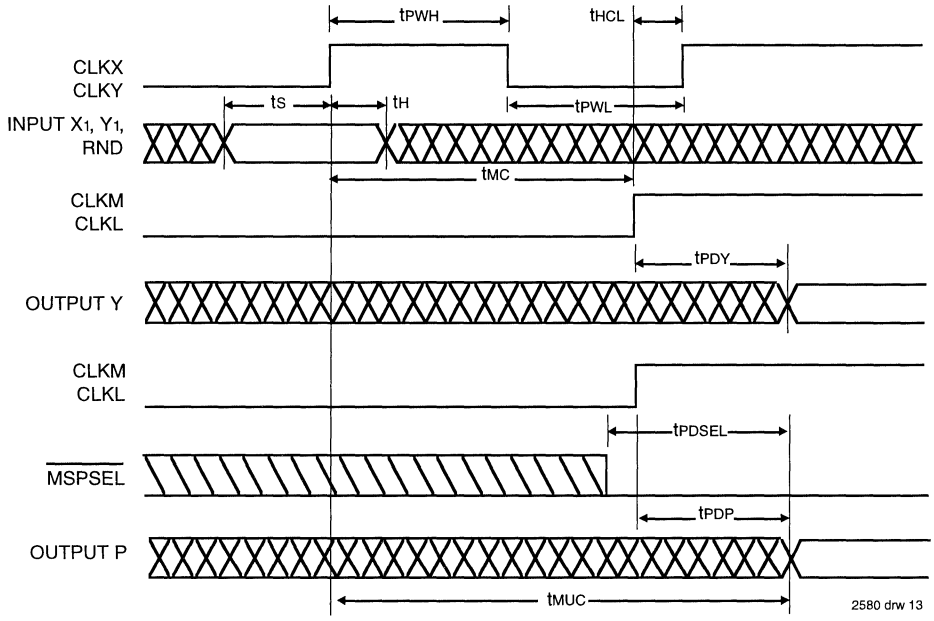


Figure 4. IDT7216 Timing Diagram

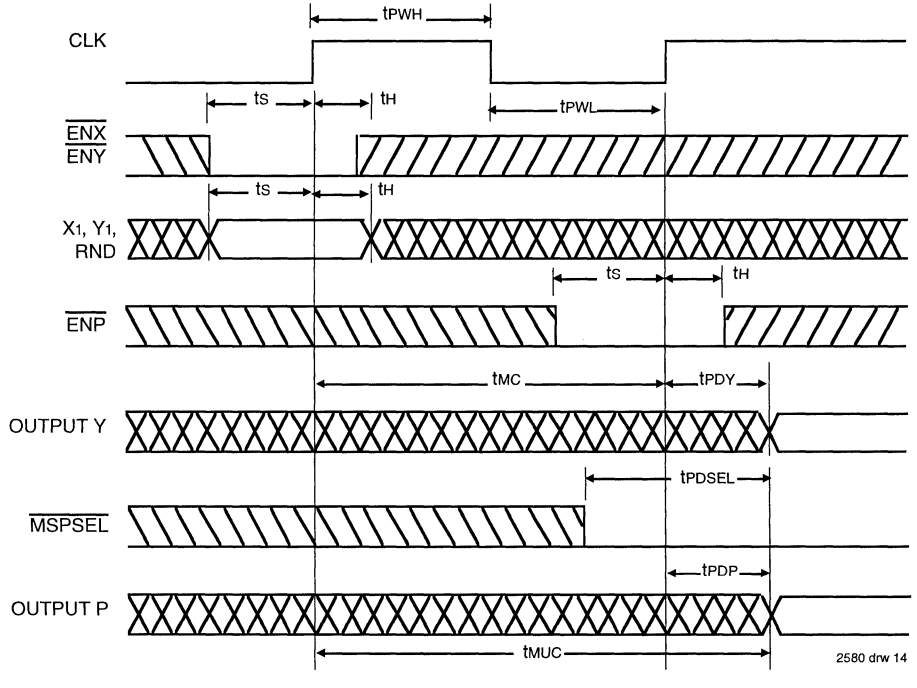


Figure 5. IDT7217 Timing Diagram

11

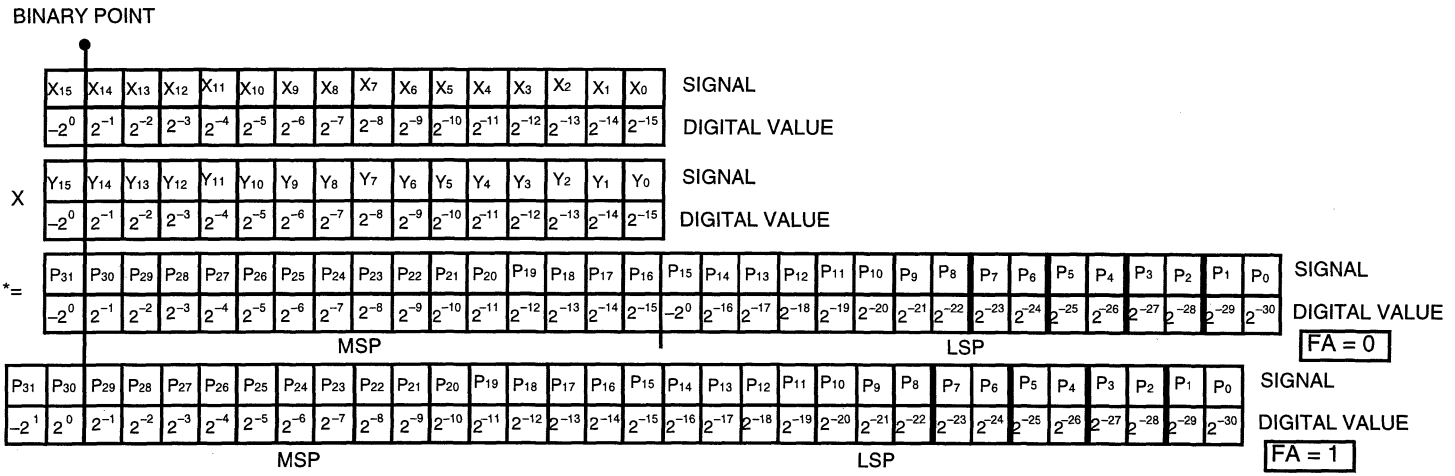


Figure 6. Fractional Two's Complement Notation

2580 drw 16

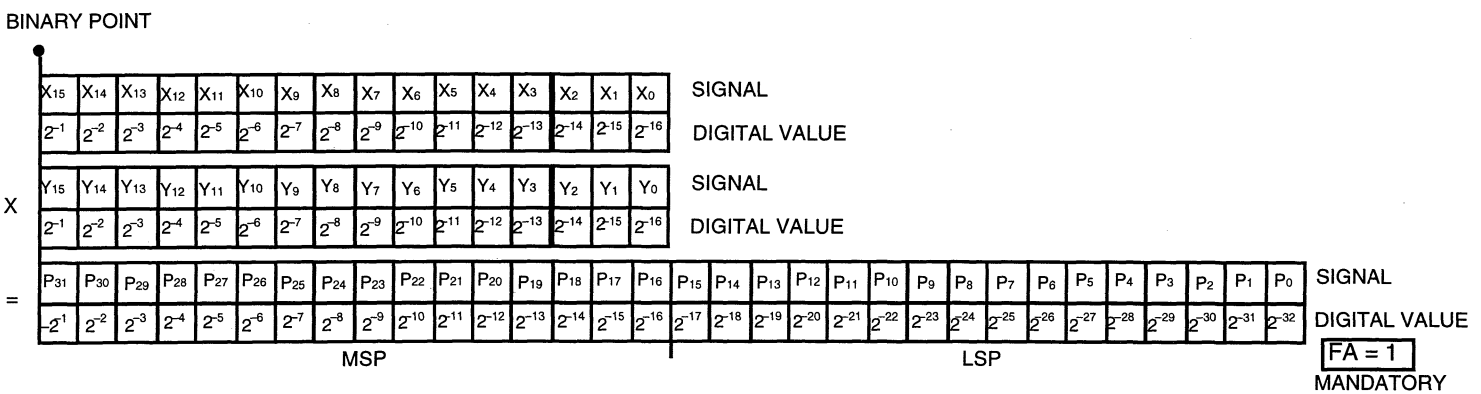


Figure 7. Fractional Unsigned Magnitude Notation

2580 drw17

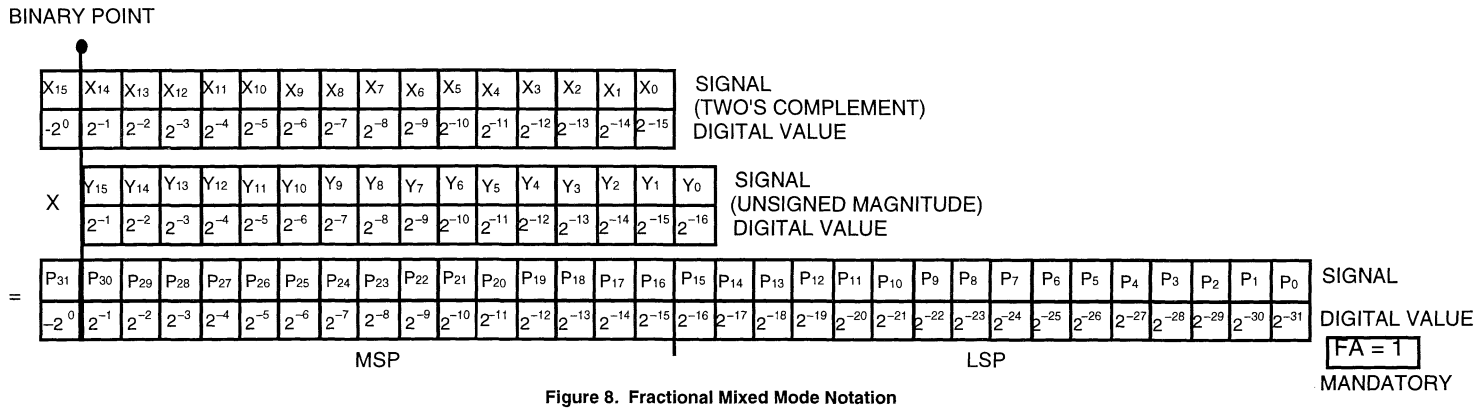


Figure 8. Fractional Mixed Mode Notation

2580 drw 18

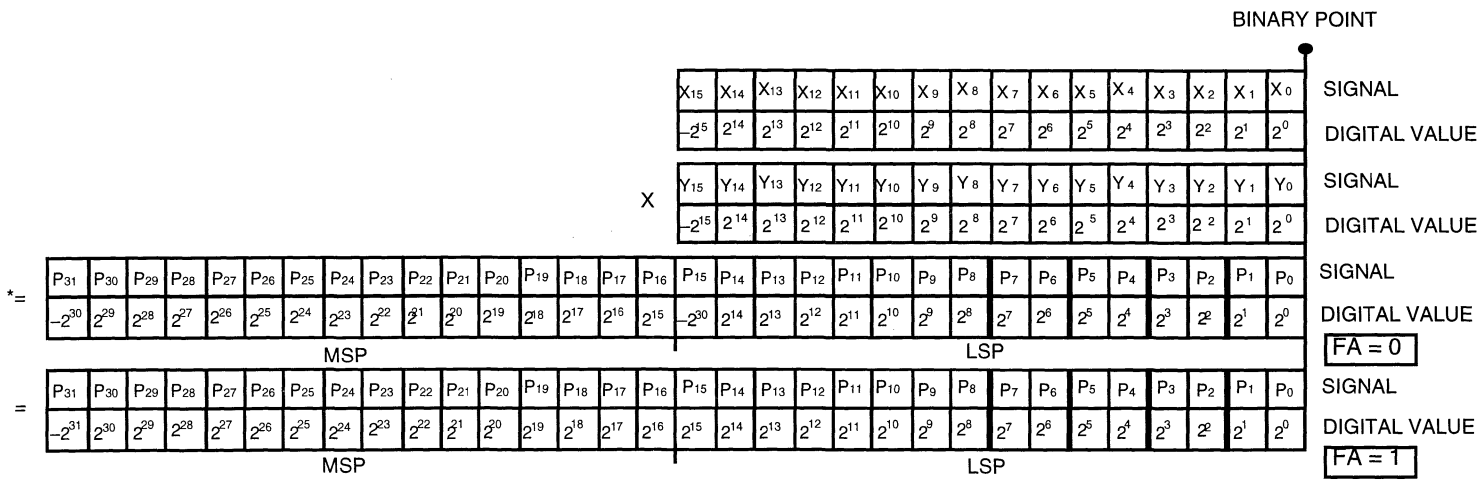


Figure 9. Integer Two's Complement Notation

2580 drw 19

* In this format an overflow occurs in the attempted multiplication of the two's complement number 1,000 . . . 0 with 1,000.0 yielding an erroneous product of –1 in the fraction case and -2^{30} in the integer case.

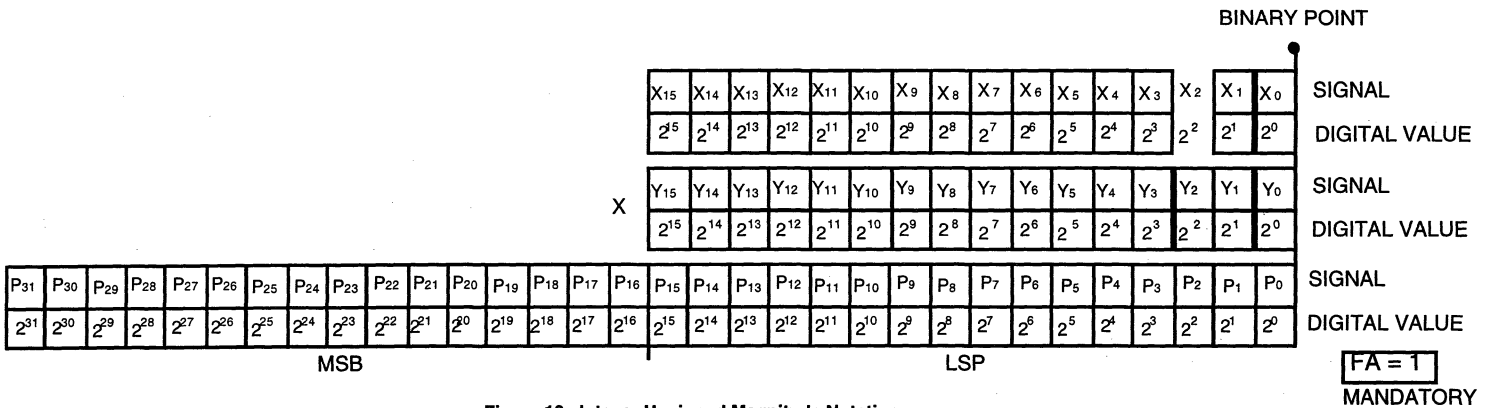


Figure 10. Integer Unsigned Magnitude Notation

2580 drw 20

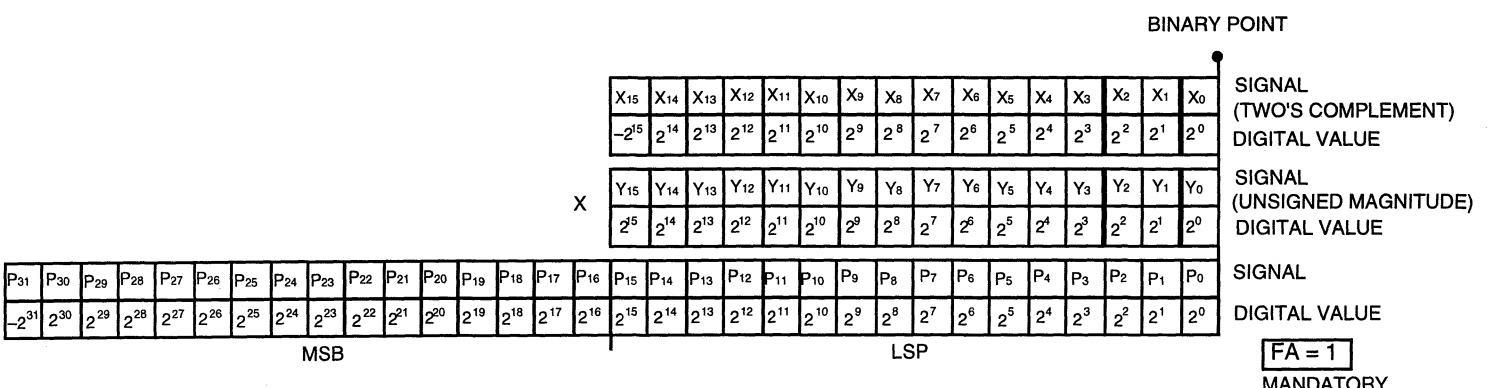


Figure 11. Integer Mixed Mode Notation

2580 drw 21

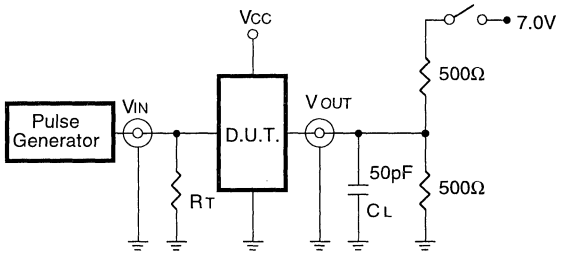


Figure 12. AC Test Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2580 tbl 08

SWITCH POSITION

Test	Switch
Disable Low Enable Low	Closed
All Other Tests	Open

2580 tbl 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

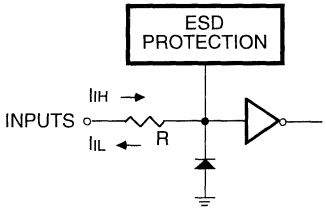


Figure 13. Input Interface Circuit

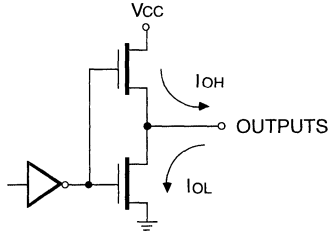
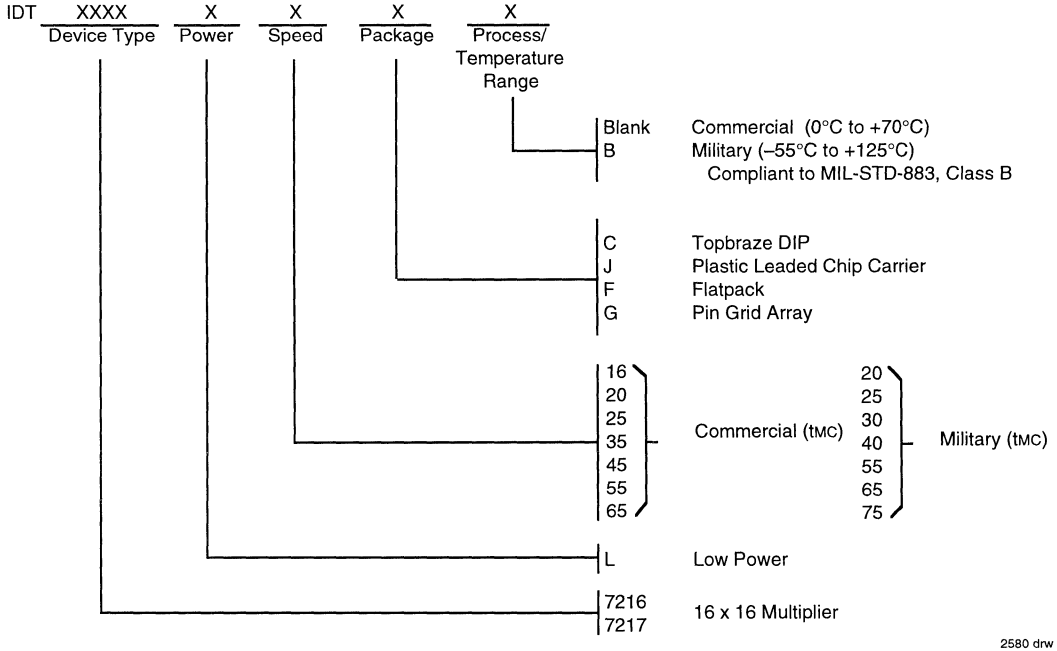


Figure 14. Output Interface Circuit

ORDERING INFORMATION



2580 drw 22

11

Integrated Device Technology, Inc.

16-BIT CMOS CASCADABLE ALU

IDT7381
IDT7383

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 16ns to 55ns clocked ALU operations
- Ideal for radar, sonar or image processing applications
- IDT7381:
  - — 54/74S381 instruction set (8 functions)
  - — Replaces Gould S614381 or Logic Devices L4C381
  - — Cascadable with or without carry look-ahead
- IDT7383:
  - — 32 advanced ALU functions
  - — Cascadable without carry look-ahead
- Pipeline or flow-through modes
- Internal feedback path for accumulation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CMOS technology
- Available in 68-lead PGA, 68-pin surface mount PLCC and 68-pin fine-pitch Flatpack (7383 only)
- Military product compliant to MIL-STD-883, Class B
- Speeds available:
  Commercial: L/16/20/25/30/40/55
  Military: L/20/25/30/35/45/65

DESCRIPTION:

The IDT7381 and IDT7383 are high-speed cascadable Arithmetic Logic Unit (ALUs). Both three-bus devices have two input registers, ultra-fast 16-bit ALUs and 16-bit output registers. With IDT's high-performance CMOS technology, the IDT7381/7383 can do arithmetic or logic operations in 20ns. The IDT7381 functionally replaces four 54/74S381 four-bit ALUs in a 68-pin package.

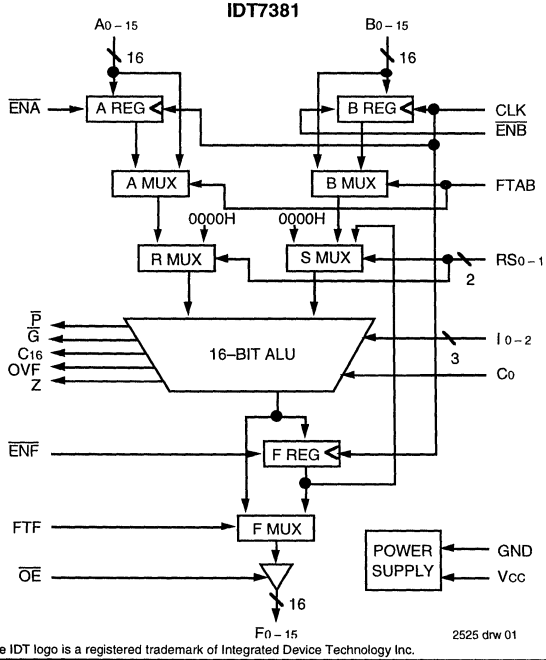
The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F output can also be set into clocked or flow-through mode. An output enable is provided for three-state control of the output port on a bus.

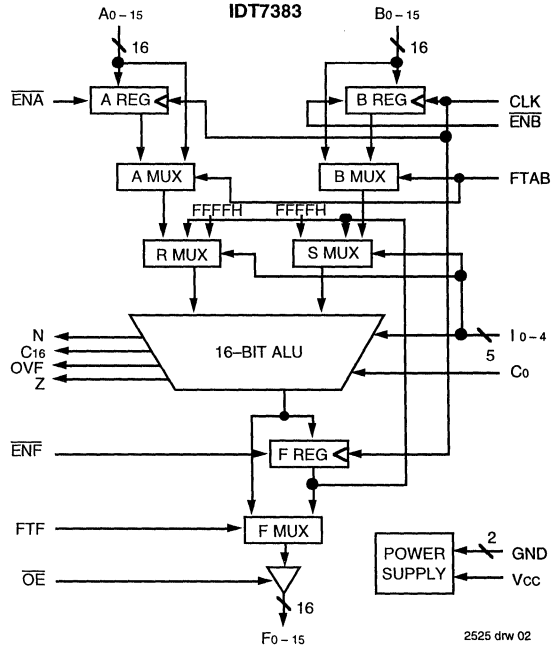
The IDT7381 has three function pins to select 1 of 8 arithmetic or logic operations. The two R and S selection pins determine whether A, B, F or 0 are fed into the ALU. This ALU has carry-out, propagate and generate outputs for cascading using carry look-ahead.

The IDT7383 has five function pins to select 1 of 32 arithmetic or logic operations. This ALU has a carry-out pin for cascading.

The IDT7381 and IDT7383 are available in 68-pin PLCC or PGA packages. Military grade product is manufactured in compliant with the latest revision of MIL-STD-883, Class B, for high reliability systems.

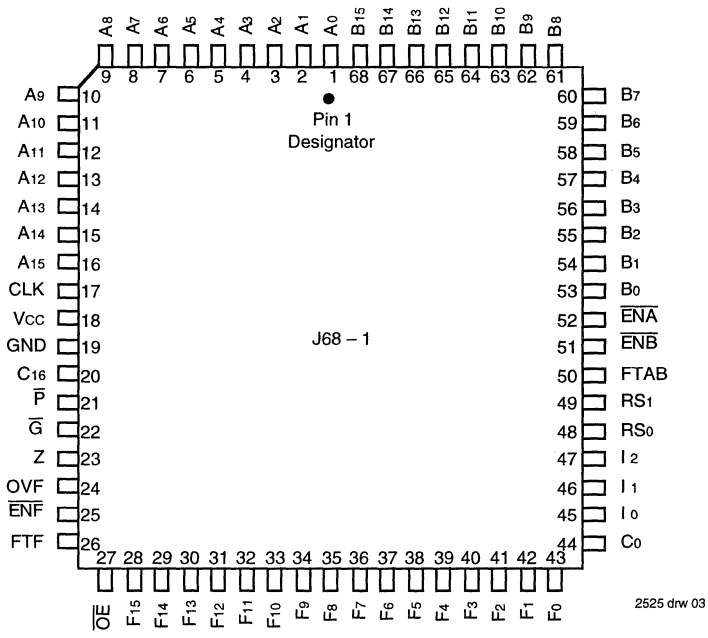
FUNCTIONAL BLOCK DIAGRAM





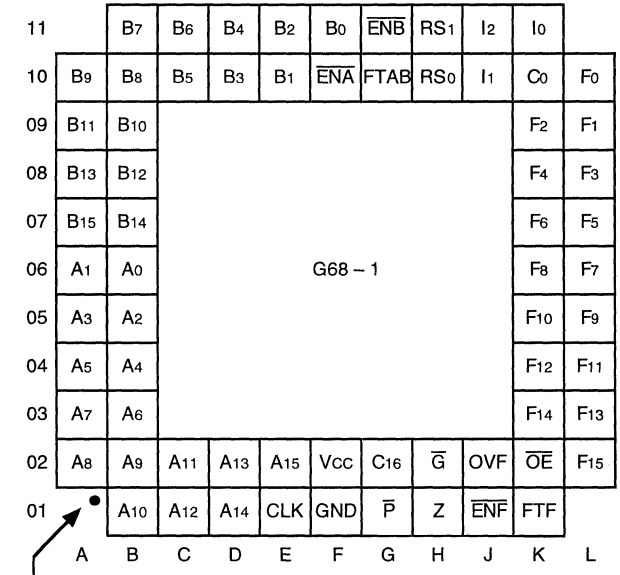
PIN CONFIGURATION

IDT7381



2525 drw 03

PLCC
TOP VIEW

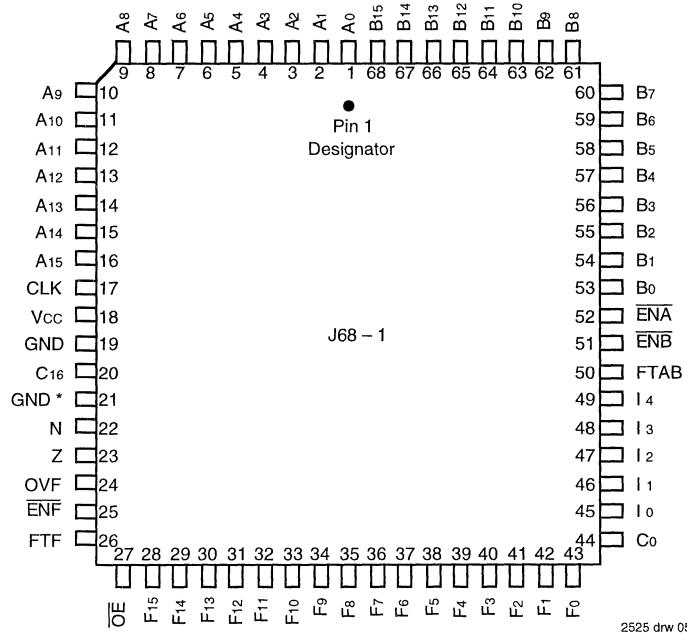


PGA
TOP VIEW

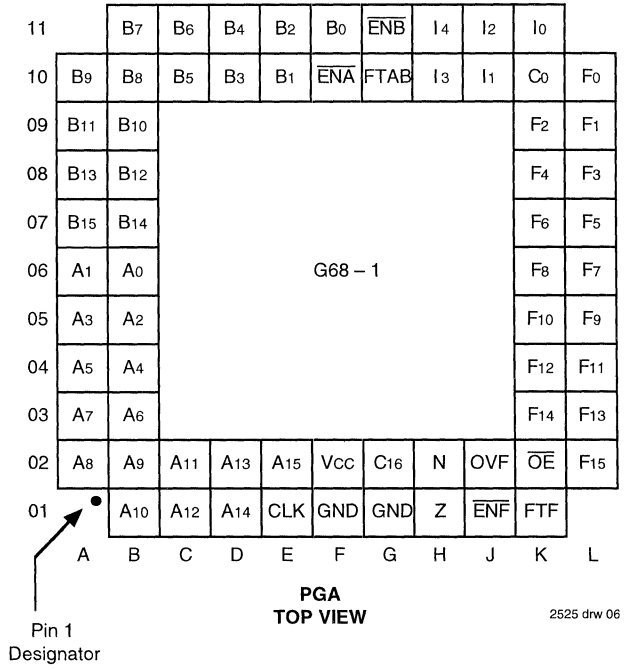
2525 drw 04

11

IDT7383

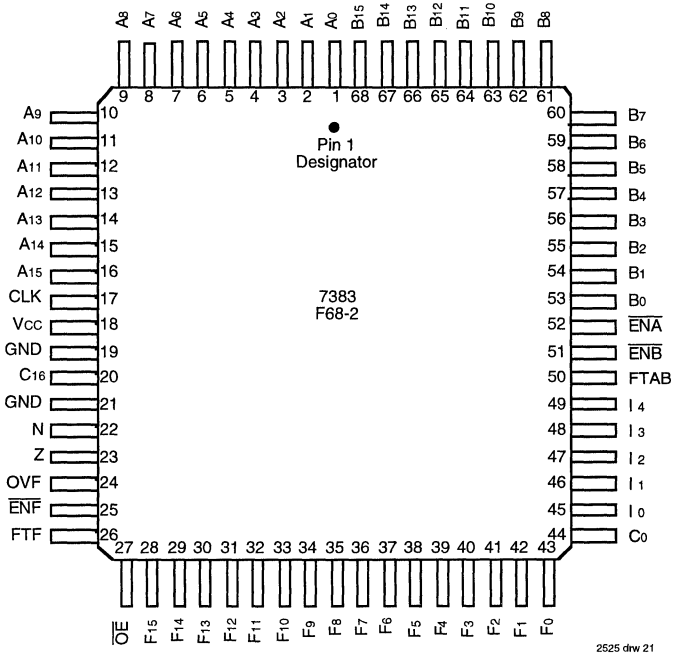


PLCC
TOP VIEW



PGA
TOP VIEW

IDT7383



FINE PITCH FLATPACK
TOP VIEW

11

PIN DESCRIPTIONS

IDT7381 AND IDT7383 PIN DESCRIPTION

Pin Name	I/O	Description
A_0 - A_{15}	I	Sixteen–bit data input port.
B_0 - B_{15}	I	Sixteen–bit data input port.
$\overline{ENA}$	I	Register enable for the A input port; active low pin.
$\overline{ENB}$	I	Register enable for the B input port; active low pin.
FTAB	I	Flow–through control pin. When this pin is high, both register A and B are transparent.
F_0 – F_{15}	O	Sixteen–bit data output port.
$\overline{ENF}$	I	Register enable for the F output port; active low pin.
FTF	I	Flow–through control pin. When this pin is high, the F register is transparent.
CLK	I	Clock input.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
C_0	I	Carry input. This pin receives arithmetic carries from less significant ALU components in a cascade configuration.
C_{16}	O	Carry output. This pin produces arithmetic carries to more significant ALU components in a cascaded configuration.
OVF	O	This pin indicates a two's complement arithmetic overflow, when high.
Z	O	This pin indicates a zero output result, when high.
V_{CC}		Power supply pin, 5V.
GND		Ground pin, 0V. There are two ground pins on the IDT7383.

2525 tbl 01

IDT7381 PINS

Pin Name	I/O	Description
RS_0 – RS_1	I	Two control pins used to select input operands for the R and S multiplexers.
I_0 - I_2	I	Three control pins to select the ALU function performed.
P	O	Indicates the carry propagate output state to the ALU.
$\overline{G}$	O	Indicates the carry generate output state to the ALU.

2525 tbl 02

IDT7383 PINS

Pin Name	I/O	Description
I_0 – I_4	I	Five control pins to select the ALU function performed.
N	O	The sign bit of an ALU operation.

2525 tbl 05

IDT7381 R AND S MUX TABLE

RS_1	RS_0	R Mux	S Mux
0	0	A	F
0	1	A	0
1	0	0	B
1	1	A	B

2525 tbl 03

IDT7381 ALU FUNCTION TABLE

I_2	I_1	I_0	Function
0	0	0	F = 0
0	0	1	$F = \overline{R} + S + C_0$
0	1	0	$F = R + \overline{S} + C_0$
0	1	1	$F = R + S + C_0$
1	0	0	F = R xor S
1	0	1	F = R or S
1	1	0	F = R and S
1	1	1	F = all 1's

2525 tbl 04

IDT7383 ALU FUNCTION TABLE

I_4	I_3	I_2	I_1	I_0	Function
0	0	0	0	0	$F = A + B + C_0$
0	0	0	0	1	F = A or B
0	0	0	1	0	$F = A + \overline{B} + C_0$
0	0	0	1	1	$F = \overline{A} + B + C_0$
0	0	1	0	0	$F = A + C_0$
0	0	1	0	1	$F = \overline{A}$ or F
0	0	1	1	0	$F = A - 1 + C_0$
0	0	1	1	1	$F = \overline{A} + C_0$
0	1	0	0	0	$F = A + F + C_0$
0	1	0	0	1	F = A or F
0	1	0	1	0	$F = A + \overline{F} + C_0$
0	1	0	1	1	$F = \overline{A} + F + C_0$
0	1	1	0	0	$F = F + B + C_0$
0	1	1	0	1	$F = \overline{A}$ or B
0	1	1	1	0	$F = F + \overline{B} + C_0$
0	1	1	1	1	$F = \overline{F} + B + C_0$
1	0	0	0	0	F = A xor B
1	0	0	0	1	F = A and B
1	0	0	1	0	$F = \overline{A}$ and B
1	0	0	1	1	F = A xnor B
1	0	1	0	0	F = A xor F
1	0	1	0	1	F = A and F
1	0	1	1	0	$F = \overline{A}$ and F
1	0	1	1	1	F = all 1's + C_0
1	1	0	0	0	$F = B + C_0$
1	1	0	0	1	F = A and $\overline{B}$
1	1	0	1	0	$F = \overline{B} + C_0$
1	1	0	1	1	$F = B - 1 + C_0$
1	1	1	0	0	$F = F + C_0$
1	1	1	0	1	F = A or $\overline{B}$
1	1	1	1	0	$F = F - 1 + C_0$
1	1	1	1	1	$F = \overline{F} + C_0$

2525 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2525 tbl 07

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Under no circumstances should an input of an I/O Pin be greater than V_{CC} + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Pkg.	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	PGA	10	pF
			Flatpack	2.5	
			PLCC	5	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	PGA	12	pF
			Flatpack	4	
			PLCC	7	

NOTE: 2525 tbl 09

1. This parameter is sampled at initial characterization and is not production tested.

11

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5V		—	—	–10	µA
I_{OS}[3]	Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		–20	—	–100	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.5V	—	–0.1	–20	µA
			V_O = 2.7V	—	–0.1	20	
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –4mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA MIL.	—	—	0.5	V
			I_{OL} = 8mA COM'L.				

2525 tbl 08

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} =GND or V_{CC}	COM'L. MIL.		— —	2 2	6 10	mA
ΔI_{CC}[3]	Quiescent Power Supply Current TTL Input HIGH	V_{CC} = Max. V_{IN} = 3.4V	COM'L. MIL.		— —	0.5 0.5	1.0 1.5	mA/ input
I_{CCD}[4]	Dynamic Power Supply Current	V_{CC} = Max. Outputs disabled V_{IN} = GND or V_{CC} Mode: FTAB = FTF = 1	COM'L MIL.		— —	15 15	48 60	µA/ MHz
I_{CCD1}	Dynamic Power Supply Current	V_{CC} = Max. Outputs Disabled All Data Inputs Disabled f_i = 10MHz, f_{CP} = 10MHz 50% Duty Cycle V_{IL} = GND, V_{IH} = V_{CC} Mode: FTAB = FTF = 1	COM'L. MIL.		— —	20 20	33 40	mA
I_{CCD2}[6]	Dynamic Power Supply Current	V_{CC} = Max. Outputs Enabled. (CL = 50pF) All Data Inputs Sw itching f_i = 10MHz, f_{CP} = 10MHz 50% Duty Cycle V_{IL} = GND, V_{IH} = V_{CC} Mode: FTAB = FTF = 1	COM'L. MIL.		— —	40 40	60 80	mA
I_C[7]	Total Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC} All Data Inputs Switching f_i = 10MHz, f_{CP} = 10MHz 50% Duty Cycle	Outputs Disabled Outputs Enabled	COM'L. MIL. COM'L. MIL.	— — — —	22 22 42 42	39 50 76 90	mA mA

NOTES:

2525 tbl 10

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived from I_{CCD1} for use in Total Power Supply calculations.
5. Total power supply current is calculated as follows:
   $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
6. This parameter is not production tested but is an indicator of the power dissipated with outputs loaded.
7. Values for these conditions are examples of the I_C formula in note 5 above. These are guaranteed but not tested.

11

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

Maximum Combinational Propagation Delays

From Input	IDT7381L16 IDT7383L16				IDT7381L20 IDT7383L20				IDT7381L25 IDT7383L25				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	
FTAB = 0, FTF = 0													
CLK	10	16	16	16	11	20	20	20	13	22	26	22	ns
C_0	—	—	13	13	—	—	14	14	—	—	16	16	ns
I_{0-4}, RS_0, RS_1[1]	—	14	18	14	—	18	20	18	—	22	22	22	ns
FTAB = 0, FTF = 1													
CLK	16	16	16	16	20	20	20	20	27	22	26	22	ns
C_0	14	—	13	13	18	—	14	14	22	—	16	16	ns
I_{0-4}, RS_0, RS_1 [1]	18	14	18	14	20	18	20	18	22	22	22	22	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	—	14	16	15	—	16	20	17	—	18	25	22	ns
CLK	10	—	—	—	11	—	—	—	13	—	—	—	ns
C_0	—	—	13	13	—	—	14	14	—	—	16	16	ns
I_{0-4}, RS_0, RS_1 [1]	—	14	18	14	—	18	20	18	—	22	22	22	ns
FTAB = 1, FTF = 1													
A_0–A_{15}, B_0–B_{15}	16	14	16	15	20	16	20	17	26	18	25	22	ns
C_0	14	—	13	13	18	—	14	14	22	—	16	16	ns
I_{0-4}, RS_0, RS_1 [1]	18	14	18	14	20	18	20	18	22	22	22	22	ns

2525 tb 11

Maximum Combinational Propagation Delays

From Input	IDT7381L30 IDT7383L30				IDT7381L40 IDT7383L40				IDT7381L55 IDT7383L55				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	
FTAB = 0, FTF = 0													
CLK	20	28	30	28	26	30	44	32	32	38	53	36	ns
C_0	—	—	20	20	—	—	28	20	—	—	34	22	ns
I_{0-4}, RS_0, RS_1[1]	—	28	28	28	—	32	34	35	—	42	42	42	ns
FTAB = 0, FTF = 1													
CLK	33	28	30	28	46	30	44	32	56	38	53	36	ns
C_0	28	—	20	20	30	—	28	20	37	—	34	22	ns
I_{0-4}, RS_0, RS_1[1]	28	28	28	28	40	32	34	35	55	42	42	42	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	—	24	30	28	—	30	40	32	—	36	46	37	ns
CLK	19	—	—	—	26	—	—	—	32	—	—	—	ns
C_0	—	—	20	20	—	—	28	20	—	—	34	22	ns
I_{0-4}, RS_0, RS_1[1]	—	28	28	28	—	32	34	35	—	42	42	42	ns
FTAB = 1, FTF = 1													
A_0–A_{15}, B_0–B_{15}	32	24	30	28	40	30	40	32	55	36	46	37	ns
C_0	28	—	20	20	30	—	28	20	37	—	34	22	ns
I_{0-4}, RS_0, RS_1[1]	28	28	28	28	40	32	34	35	55	42	42	42	ns

2525 tb 12

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C) - (Cont'd.)

Minimum Set-up and Hold Times Relative to Clock (CLK)

Input	IDT7381L16 IDT7383L16		IDT7381L20 IDT7383L20		IDT7381L25 IDT7383L25		IDT7381L30 IDT7383L30		IDT7381L40 IDT7383L40		IDT7381L55 IDT7383L55		Unit
	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	
FTAB = 0, FTF = X													
A_0–A_{15}, B_0–B_{15}	4	0	5	0	6	0	6	0	6	0	8	0	ns
C_0 (2)	9	0	12	0	16	0	16	0	16	0	21	0	ns
I_{0-4}, RS_0, RS_1 (1) (2)	11	0	15	0	24	0	29	0	32	0	44	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	4	0	5	0	6	0	6	0	6	0	8	0	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	10	0	14	0	16	0	25	0	28	0	35	0	ns
C_0	9	0	12	0	16	0	16	0	16	0	21	0	ns
I_{0-4}, RS_0, RS_1 (1)	11	0	15	0	24	0	29	0	32	0	44	0	ns
$\overline{ENF}$	4	0	5	0	6	0	6	0	6	0	8	0	ns

2525 tbl 13

Minimum Clock Cycle Times and Pulse Widths

Parameter	IDT7381L16 IDT7383L16	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L40 IDT7383L40	IDT7381L55 IDT7383L55	Unit
Clock LOW Time	5	5	6	8	10	14	ns
Clock HIGH Time	5	5	6	8	10	14	ns
Clock Period	16	18	20	25	34	43	ns

2525 tbl 14

Maximum Output Enable/Disable Times

Parameter	IDT7381L16 IDT7383L16	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L40 IDT7383L40	IDT7381L55 IDT7383L55	Unit
Enable Time	7	8	10	15	18	20	ns
Disable Time	7	8	10	15	18	20	ns

2525 tbl 15

NOTES:
1. For IDT7381, pins I_0 – I_2, RS_0, RS_1 apply. For IDT7383, pins I_0 – I_4 apply.
2. Only for FTF = 0.
3. Minimum propagation delays are not production tested but guaranteed to be greater than or equal to 3ns.

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AC ELECTRICAL CHARACTERISTICS — MILITARY (V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Maximum Combinational Propagation Delays

From Input	IDT7381L20 IDT7383L20				IDT7381L25 IDT7383L25				IDT7381L30 IDT7383L30				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	
FTAB = 0, FTF = 0													
CLK	11	20	20	20	14	24	24	24	26	28	34	28	ns
C_0	—	—	14	14	—	—	18	18	—	—	22	22	ns
I_{0-4}, RS_0, RS_1 (1)	—	18	20	18	—	22	24	22	—	28	28	28	ns
FTAB = 0, FTF = 1													
CLK	20	20	20	20	25	24	24	24	34	28	34	28	ns
C_0	18	—	14	14	21	—	18	18	26	—	22	22	ns
I_{0-4}, RS_0, RS_1 (1)	20	18	20	18	25	22	24	22	30	28	28	28	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	—	16	20	17	—	20	25	22	—	28	28	28	ns
CLK	11	—	—	—	14	—	—	—	26	—	—	—	ns
C_0	—	—	14	14	—	—	18	18	—	—	22	22	ns
I_{0-4}, RS_0, RS_1 (1)	—	18	20	18	—	22	24	22	—	28	28	28	ns
FTAB = 1, FTF = 1													
A_0–A_{15}, B_0–B_{15}	20	16	20	17	25	22	25	22	30	28	28	28	ns
C_0	18	—	14	14	21	—	18	18	26	—	22	22	ns
I_{0-4}, RS_0, RS_1 (1)	20	18	20	18	25	22	24	22	30	28	28	28	ns

2525 tb 16

Maximum Combinational Propagation Delays

From Input	IDT7381L35 IDT7383L35				IDT7381L45 IDT7383L45				IDT7381L65 IDT7383L65				Unit
	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z,OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	F_{0-15}	$\overline{P}$, $\overline{G}$, N	Z, OVF	C_{16}	
FTAB = 0, FTF = 0													
CLK	27	32	45	32	28	34	50	34	37	44	63	45	ns
C_0	—	—	30	23	—	—	32	23	—	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	—	34	34	34	—	38	38	38	—	48	48	48	ns
FTAB = 0, FTF = 1													
CLK	45	32	40	32	56	34	50	34	68	44	63	45	ns
C_0	30	—	30	23	32	—	32	23	42	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	40	34	34	34	46	38	38	38	66	48	48	48	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	—	30	35	32	—	32	46	36	—	44	56	44	ns
CLK	27	—	—	—	28	—	—	—	37	—	—	—	ns
C_0	—	—	30	23	—	—	32	23	—	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	—	34	34	34	—	38	38	38	—	48	48	48	ns
FTAB = 1, FTF = 1													
A_0–A_{15}, B_0–B_{15}	40	30	30	32	45	32	46	36	65	44	56	44	ns
C_0	30	—	30	23	32	—	32	23	42	—	42	25	ns
I_{0-4}, RS_0, RS_1 (1)	40	34	34	34	46	38	38	38	66	48	48	48	ns

2525 tb 17

AC ELECTRICAL CHARACTERISTICS — MILITARY (Vcc = 5V ± 10%, TA = –55°C to +125°C) - (Cont'd)

Minimum Set-up and Hold Times Relative to Clock (CLK)

Input	IDT7381L20 IDT7383L20		IDT7381L25 IDT7383L25		IDT7381L30 IDT7383L30		IDT7381L35 IDT7383L35		IDT7381L45 IDT7383L45		IDT7381L65 IDT7383L65		Unit
	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	
FTAB = 0, FTF = X													
A_0–A_{15}, B_0–B_{15}	6	0	7	0	8	0	8	0	8	0	10	0	ns
C_0 (2)	12	0	14	0	18	0	19	0	20	0	25	0	ns
I_{0-4}, RS_0, RS_1 (1) (2)	15	0	19	0	30	0	32	0	36	0	50	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	6	0	7	0	8	0	8	0	8	0	10	0	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	14	0	14	0	27	0	30	0	33	0	43	0	ns
C_0	12	0	14	0	18	0	19	0	20	0	25	0	ns
I_{0-4}, RS_0, RS_1 (1)	15	0	19	0	30	0	34	0	36	0	50	0	ns
$\overline{ENF}$	6	0	7	0	8	0	8	0	8	0	10	0	ns

2525 tbl 18

Minimum Clock Cycle Times and Pulse Widths

Parameter	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L35 IDT7383L35	IDT7381L45 IDT7383L45	IDT7381L65 IDT7383L65	Unit
Clock LOW Time	6	8	12	13	15	20	ns
Clock HIGH Time	6	8	12	13	15	20	ns
Clock Period	20	20	26	30	38	52	ns

2525 tbl 19

Maximum Output Enable/Disable Times

Parameter	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L35 IDT7383L35	IDT7381L45 IDT7383L45	IDT7381L65 IDT7383L65	Unit
Enable Time	12	14	18	19	20	22	ns
Disable Time	12	14	18	19	20	22	ns

2525 tbl 20

NOTES:
1. For IDT7381, pins I_0 – I_2, RS_0, RS_1 apply. For IDT7383, pins I_0 – I_4 apply.
2. Only for FTF = 0.
3. Minimum propagation delays are not production tested but guaranteed to be greater than or equal to 3ns.

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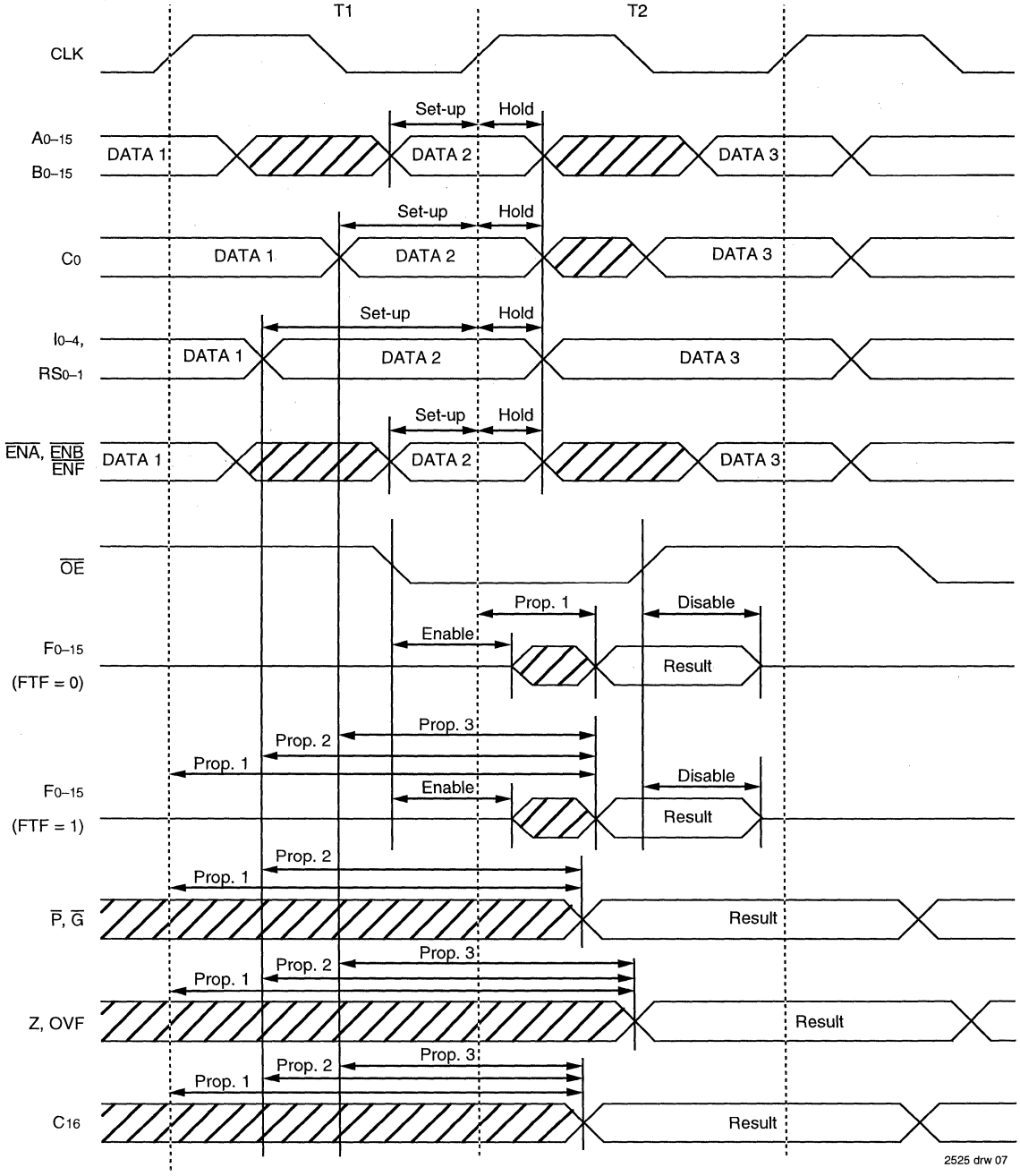
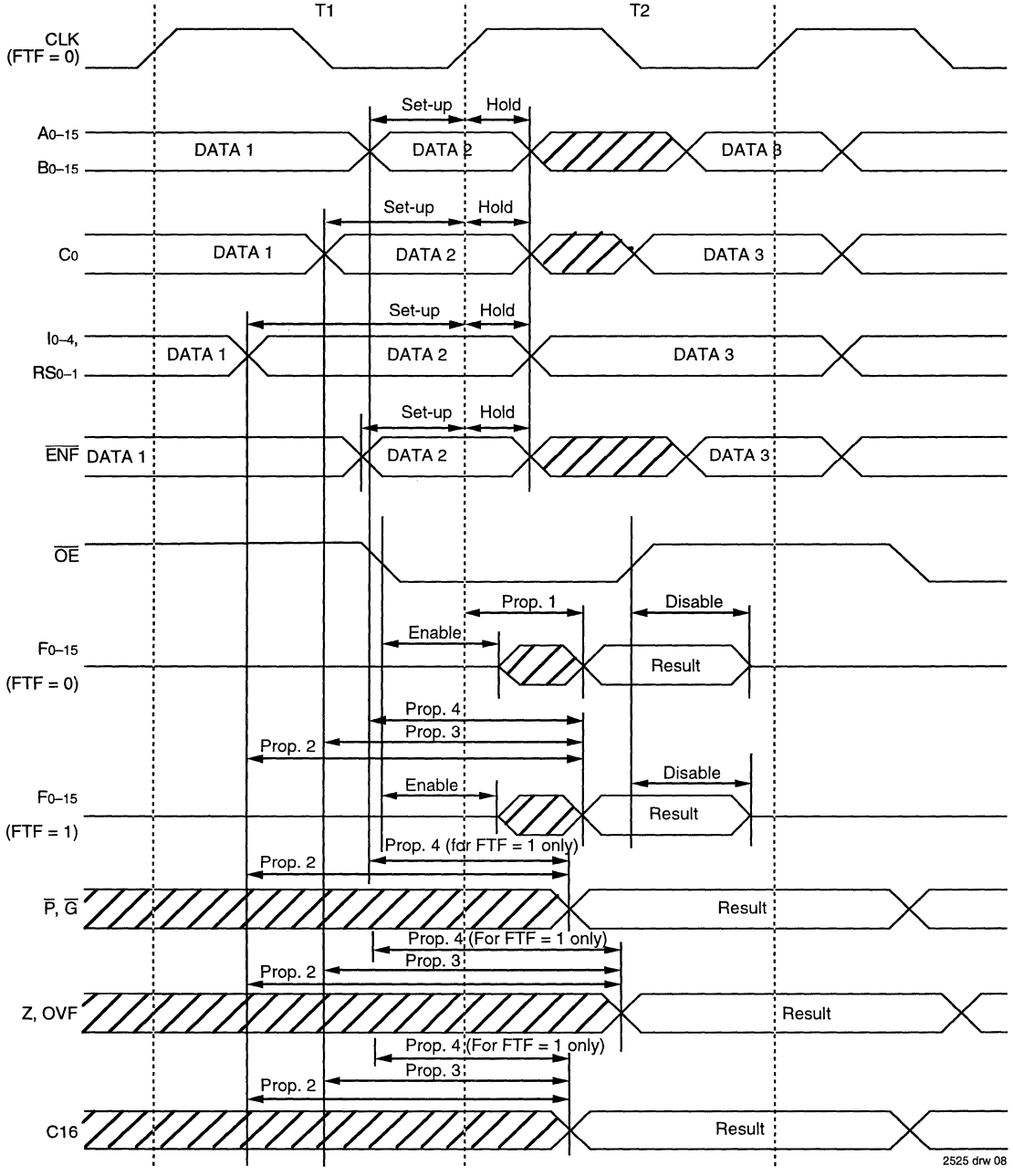
WAVEFORMS FOR FTAB = 0, FTF = X



Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to I0–4, RS0–2.
Prop. 3: Propagation delay with respect to C0.

WAVEFORMS FOR FTAB = 1, FTF = X



Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to I_{0-4}, RS_{0-2}.
Prop. 3: Propagation delay with respect to C_0.
Prop. 4: Propagation delay with respect to A, B.

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PROPAGATION DELAY CALCULATIONS FOR TWO IDT7381/7383s

From Input	To Output		To Set PUT Time
	F_{0-15}	Flags [2]	Relative to Clock (CLK)
FTAB = 0, FTF = 0			
CLK	As in 16-bit case	(Clk → C_{16}) + (C_0 → flag)	. . . .
C_0	. . . .	(C_0 → C16) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	. . . .	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	. . . .	. . . .	As in 16-bit case
ENA, ENB,ENF	. . . .	. . . .	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	(Clk → C_{16}) + (C_0 → F_{0-15})	(Clk → C_{16}) + (C_0 → flag)	. . . .
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	. . . .	. . . .	As in 16-bit case
ENA, ENB,ENF	. . . .	. . . .	As in 16-bit case
FTAB = 1, FTF = 0			
CLK	As in 16-bit case	. . . .	. . . .
C_0	. . . .	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	. . . .	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	. . . .	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	As in 16-bit case
ENA, ENB,ENF	. . . .	. . . .	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	Don't care condition	Don't care condition	. . . .
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	. . . .
I_{0-4}, RS_{0-1} [1]	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	. . . .
A_{0-15}, B_{0-15}	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → F_{0-15})	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	. . . .
ENA, ENB,ENF	. . . .	. . . .	. . . .

2525 tbl 22

NOTES:
1. For IDT7381, pins I_{0-2}, RS_{0-2} apply. For IDT7383, pins I_{0-4} apply.
2. Flags are $\overline{P}$, $\overline{G}$, OVF, Z, C_{16} for IDT7381. Flags are N, OVF, Z C_{16} for IDT7383.

CASCADING THE IDT7381/3

Some applications require 32-bit or wider input operands. Cascading is the hardware solution. It provides a high speed alternative in handling more than 16-bit wide operands.

This section is divided in three parts:

1. Cascading the IDT7381
2. Cascading the IDT7383
3. Time delay considerations

1. Cascading the IDT7381

Cascading to 32-bit wide operands takes only two IDT7381s and no external hardware. However, cascading to data widths greater than 32-bit can be done in two ways: without external hardware (slow method) or by using a carry look ahead generator like FCT182 (fast method).

a) Cascading the IDT7381 without a carry-look-ahead generator: (Figures 1 and 2)

1. Connect the C_{16} output of the least significant device into the C_0 input of the next most significant device.
2. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
3. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
4. The system's zero flag (Z) is obtained by ANDing all zero flag results.

b) Cascading three or more IDT7381s with carry-look-ahead (CLA) generator: (Figure 3)

1. Connect the $\overline{P}$ and $\overline{G}$ outputs of each device to the CLA generator's corresponding inputs.
2. Take the CLA generator outputs into the C_0 inputs of each device (except for the least significant one).
3. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
4. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
5. Carry-in to the system should be connected to the C_0 input of the least significant device and also to the CLA generator.

2. Cascading the IDT7383

(Figures 4 and 5)

1. Connect the C_{16} output of the least significant device into the C_0 input of the next most significant device.
2. Common lines to all devices are: I_{0-4}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
3. Take OVF, C_{16}, N of the most significant device as valid.
4. The system's zero flag (Z) is obtained by ANDing all zero flag results.

3. Time Delay Considerations

Once cascading has taken place, time delays may become critical in high performance systems. Our main interest here is focused on "propagation delays", i.e. calculating the time required for an input signal to propagate through several cascaded devices up to a specific output in another device within the cascaded system.

Propagation Delay

The propagation delay *for two devices* between the input and output of interest (input to output delay) is done as follows:

1. Calculate delay between the input and C_{16} in the first device.
2. Calculate delay between C_0 and the output in the second device.
3. Add both results.

The following table is an example on how to build a propagation delay table for all inputs in a 32-bit IDT7381/3 cascaded system.

Propagation delay calculations can be extended to *n–cascaded* devices as the sum of the delays in all devices between the input and output of interest. That is:

$$(Input)_1 \rightarrow (C_{16})_1 = t_1$$

...

$$(C_0)_i \rightarrow (C_{16})_i = t_i$$

$$(C_0)_{i+1} \rightarrow (C_{16})_{i+1} = t_{i+1}$$

...

$$(C_0)_n \rightarrow (Output)_n = t_n$$

Where the subscript i denotes the device number and the arrow (→) represents the delay in between. Notice that i + 1 is the immediate upper device from device i. Adding the delays t_i we get:

$$\text{Propagation delay} = t_1 + t_2 + \ldots + t_i + t_{i+1} + \ldots + t_n$$

Total Delay

As seen from Figure 10, the propagation delay is within the IDT7381/3 devices only. A complete analysis should also include the delay associated with the transmission line Li (which depends on the line length and its impedance). This line delay should then be added to the propagation delay to obtain the total delay for the cascaded system:

Total delay = Propagation delay + Transmission line delay

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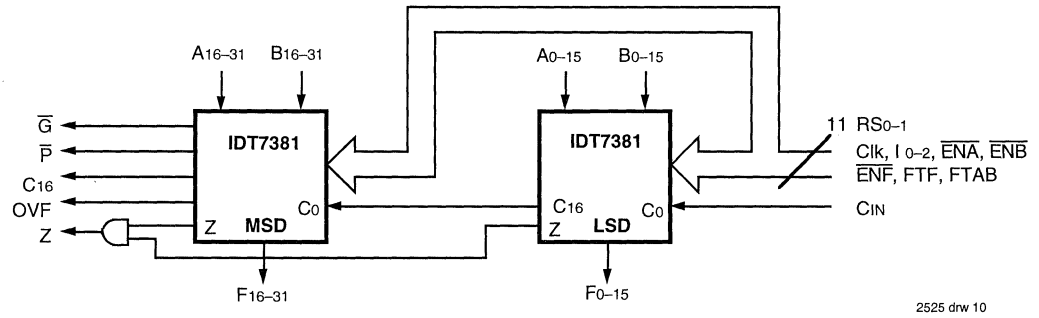

Figure 1. Cascading Two IDT7381s to 32 Bits

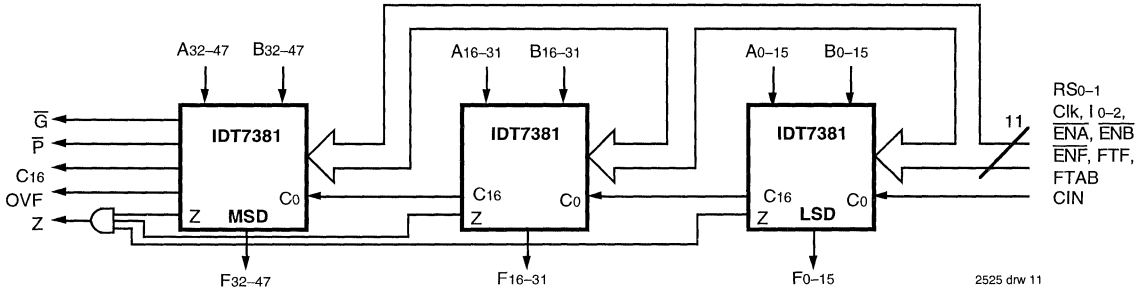

Figure 2. Cascading Three IDT7381s to 48 Bits Wide without a Carry-lookahead Generator

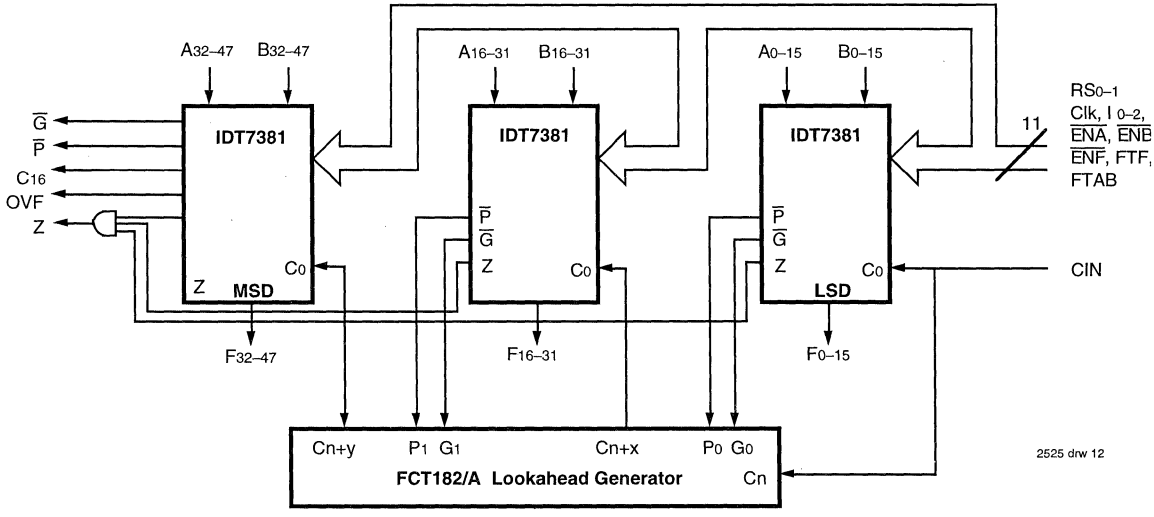

Figure 3. Cascading Three IDT7381s to 48 Bits Wide with a Carry-lookahead Generator

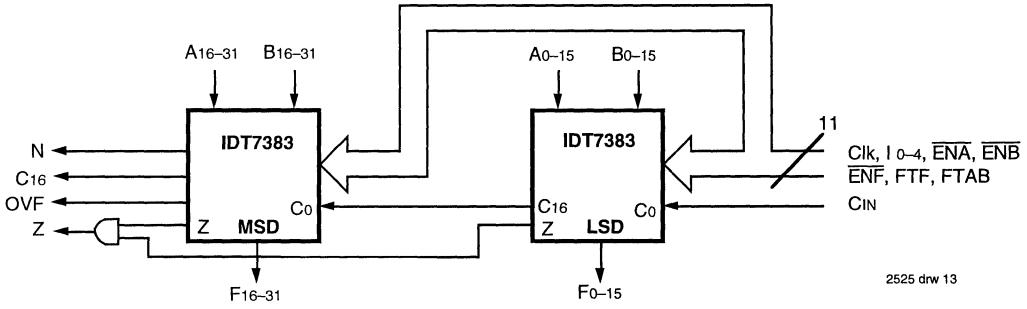

Figure 4. Cascading Two IDT7383s to 32 Bits

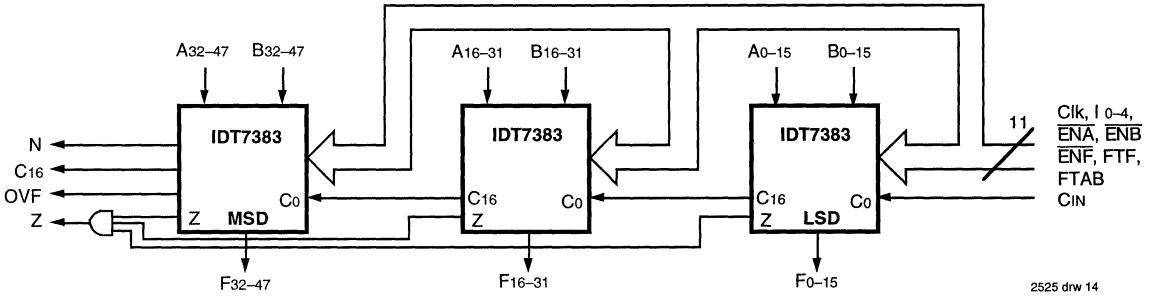

Figure 5. Cascading Three IDT7383s to 48 Bits

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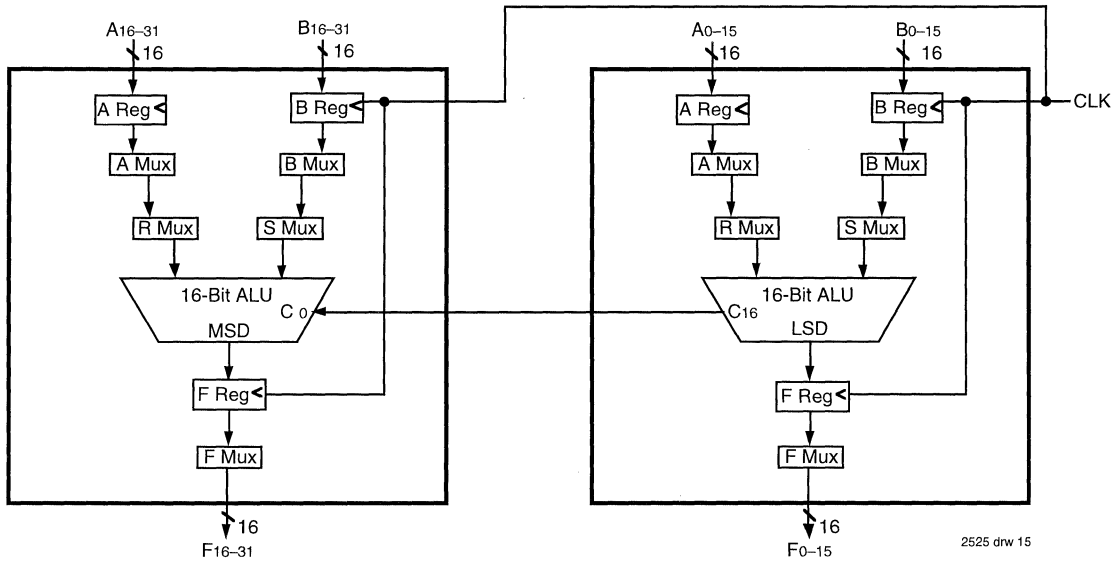


Figure 6. 32-Bit Configuration for FTAB = 0, FTF = 0

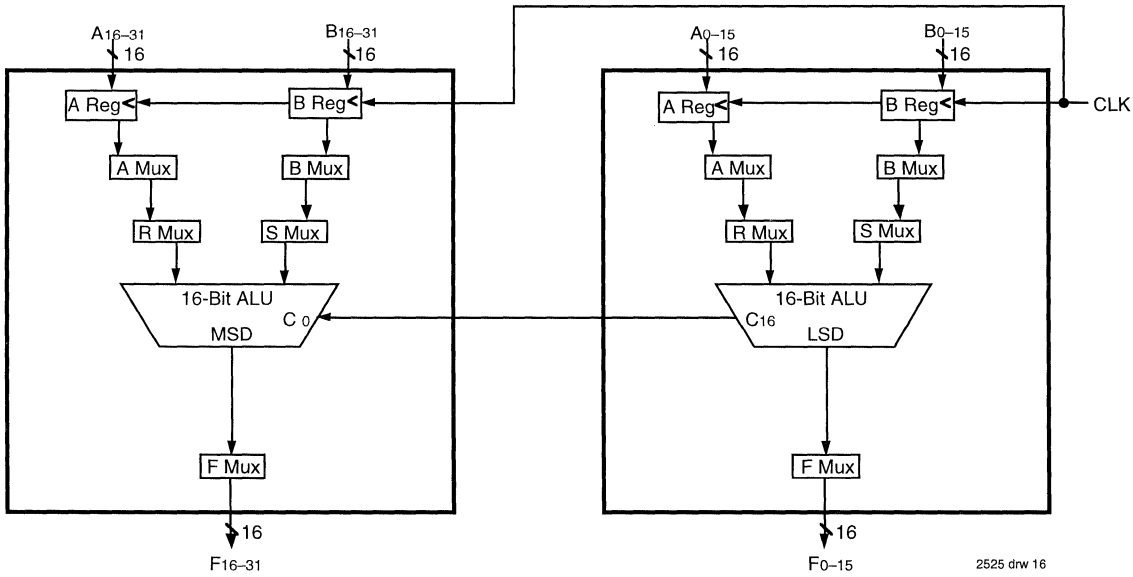


Figure 7. 32-Bit Configuration for FTAB = 0, FTF = 1

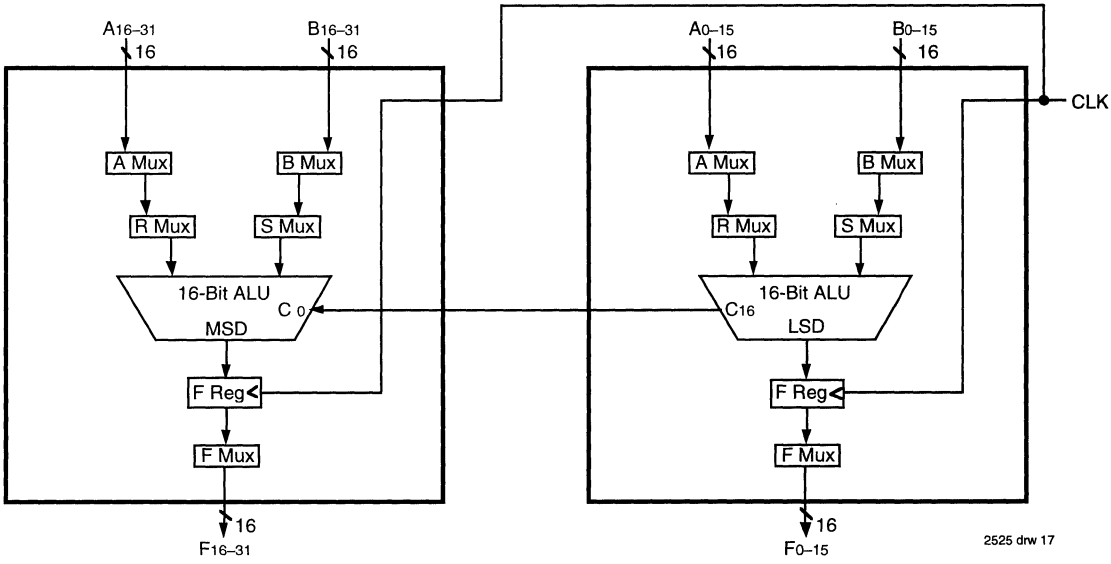


Figure 8. 32-Bit Configuration for FTAB = 1, FTF = 0

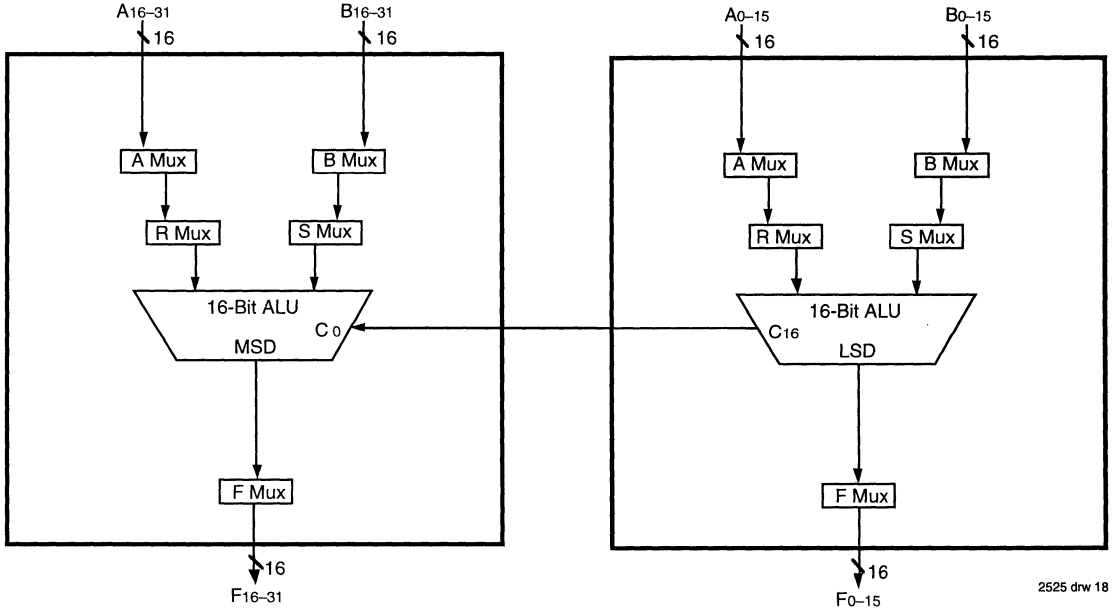


Figure 9. 32-Bit Configuration for FTAB = 1, FTF = 1

11

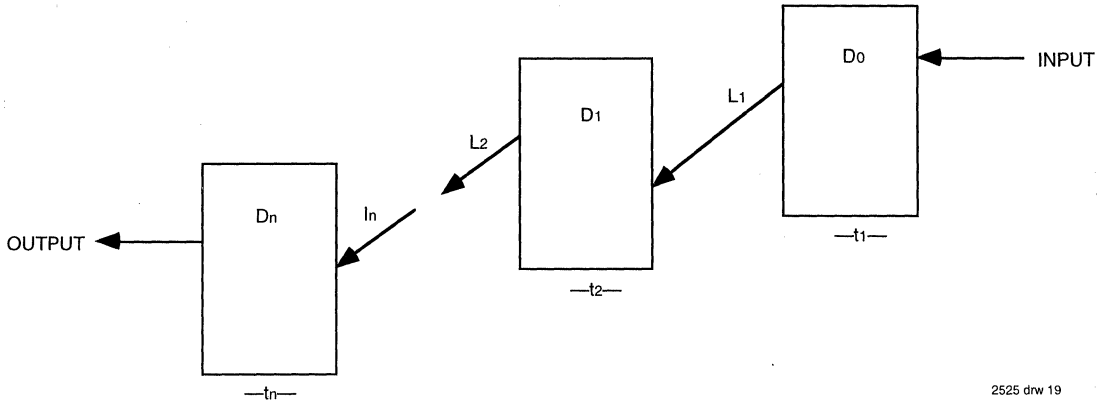


Figure 10. Propagation Delay = t1 + t2 + . . . + tn N-Cascaded Devices

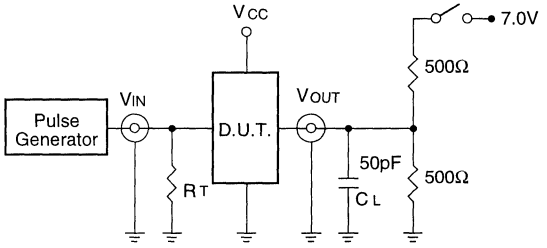
AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2525 tbl 21

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2525 drw 09

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

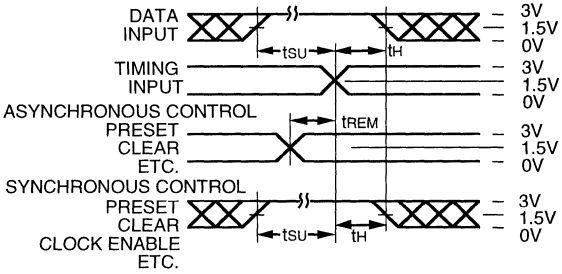
2525 lnk 23

DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.

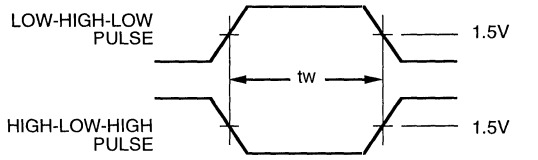
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



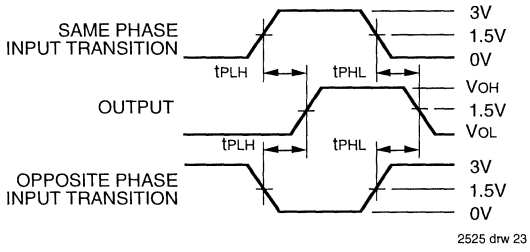
2525 drw 21

PULSE WIDTH



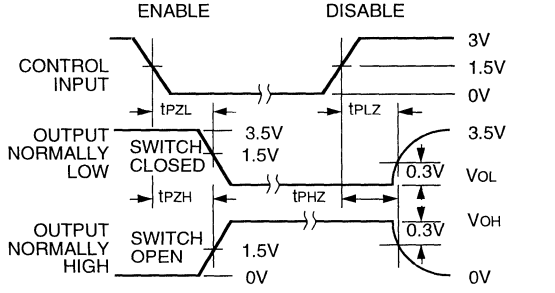
2525 drw 22

PROPAGATION DELAY



2525 drw 23

ENABLE AND DISABLE TIMES



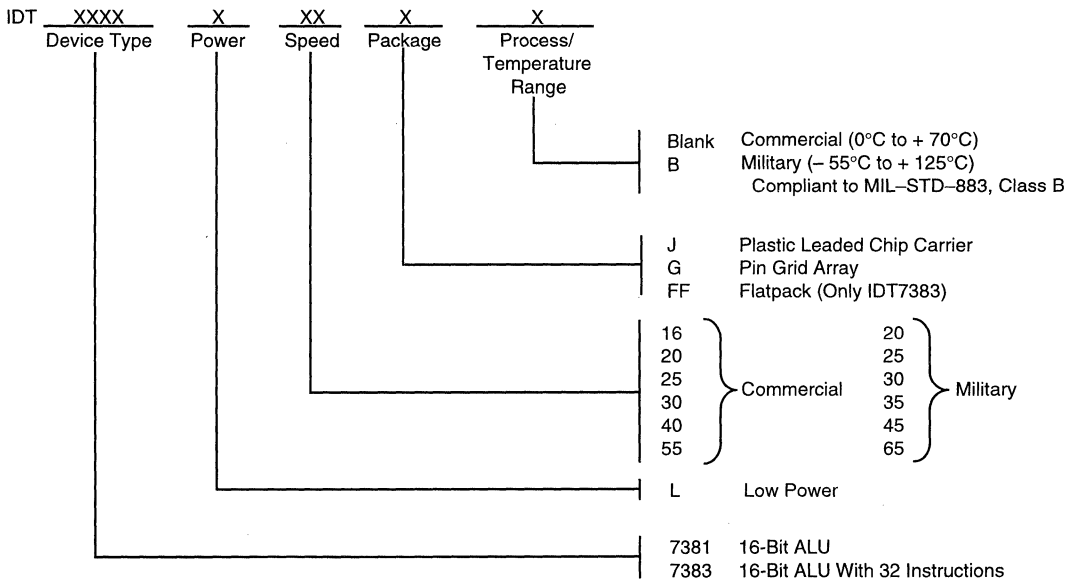
2525 drw 24

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

11

ORDERING INFORMATION



2525 drw 20

Integrated Device Technology, Inc.

16-BIT TRI-PORT BUS EXCHANGER

IDT73720/A

FEATURES:

- High-speed 16-bit bus exchange for interbus communication in the following environments:
  - — Multi-way interleaving memory
  - — Multiplexed address and data busses
- Direct interface to R3051 family RISChipSet™
  - — R3051™ family of integrated RISController™ CPUs
  - — R3721 DRAM controller
- Data path for read and write operations
- Low noise 12mA TTL level outputs
- Bidirectional 3-bus architecture: X, Y, Z
  - — One CPU bus: X
  - — Two (interleaved or banked) memory busses:Y & Z
  - — Each bus can be independently latched
- Byte control on all three busses
- Source terminated outputs for low noise and undershoot control
- 68-pin PLCC and 80-pin PQFP package
- High-performance CMOS technology.

DESCRIPTION:

The IDT73720/A Bus Exchanger is a high speed 16-bit bus exchange device intended for inter-bus communication in interleaved memory systems and high performance multiplexed address and data busses.

The Bus Exchanger is responsible for interfacing between the CPU A/D bus (CPU address/data bus) and multiple memory data busses.

The 73720/A uses a three bus architecture (X, Y, Z), with control signals suitable for simple transfer between the CPU bus (X) and either memory bus (Y or Z). The Bus Exchanger features independent read and write latches for each memory bus, thus supporting a variety of memory strategies. All three ports support byte enable to independently enable upper and lower bytes.

FUNCTIONAL BLOCK DIAGRAM

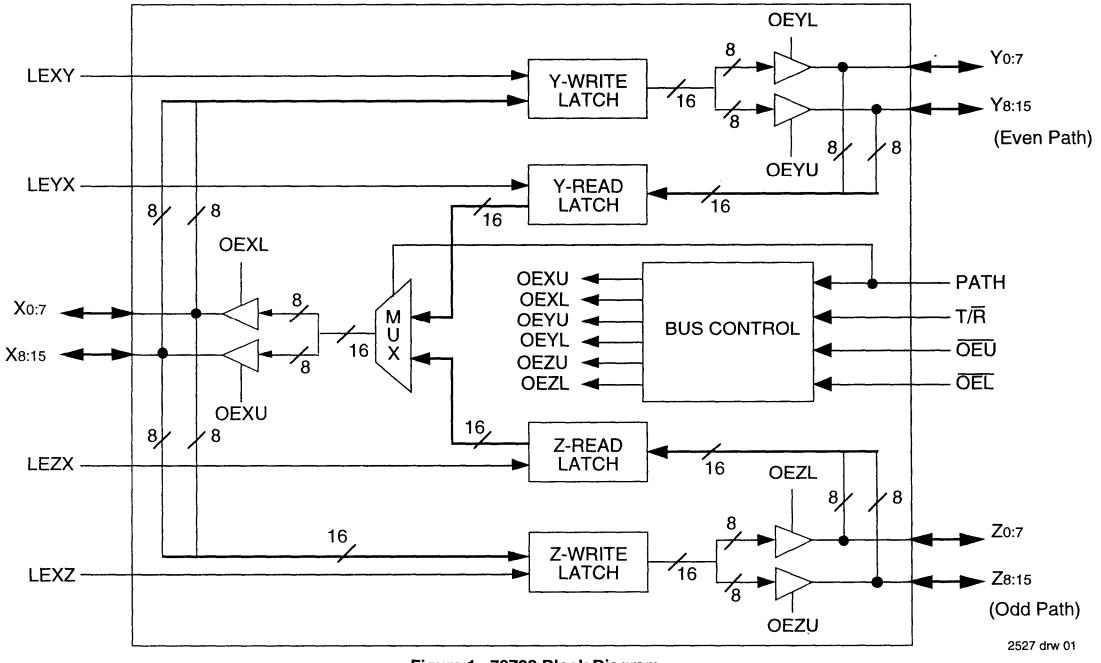


Figure 1. 73720 Block Diagram

NOTE:

1. Logic equations for bus control:
   OEXU = T/R* . OEU*; OEXL = T/R* . OEL*; OEYU = T/R . PATH . OEU*
   OEYL = T/R . PATH . OEL*; OEZU = T/R . PATH* . OEU*; OEZL = T/R . PATH* . OEL*

RISChipSet, RISController, R305x, R3051, R3052 are trademarks and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

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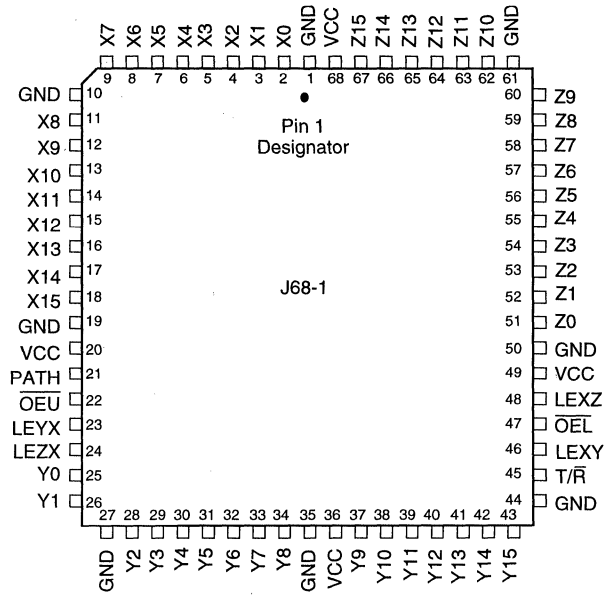
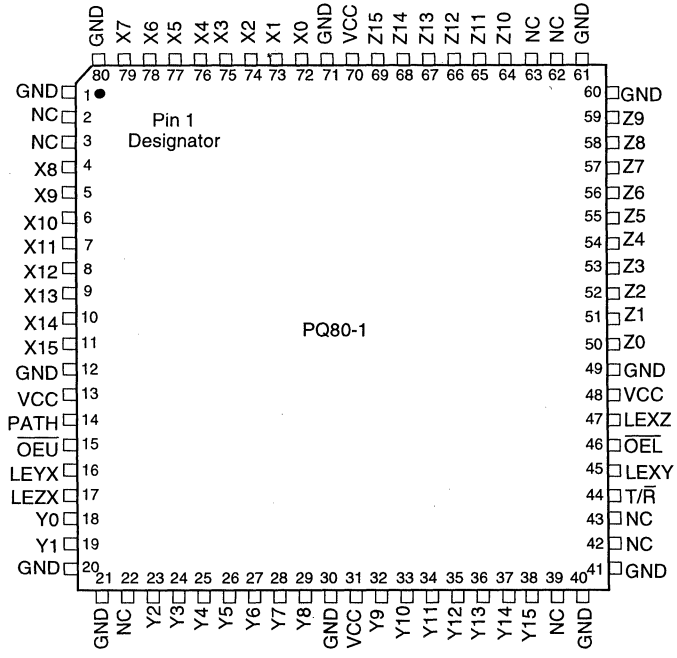
PIN CONFIGURATIONS



PLCC
TOP VIEW



PQFP
TOP VIEW

PIN DESCRIPTION

Signal	I/O	Description
X(0:15)	I/O	Bidirectional Data Port X. Usually connected to the CPU's A/D (Address/Data) bus.
Y(0:15)	I/O	Bidirectional Data port Y. Connected to the even path or even bank of memory.
Z(0:15)	I/O	Bidirectional Data port Z. Connected to the odd path or odd bank of memory.
LEXY	I	Latch Enable input for Y-Write Latch. The Y-Write Latch is open when LEXY is HIGH. Data from the X-port (CPU) is latched on the HIGH-to-LOW transition of LEXY
LEXZ	I	Latch Enable input for Z-Write Latch. The Z-Write Latch is open when LEXZ is HIGH. Data from the X-port (CPU) is latched on the HIGH-to-LOW transition of LEXZ.
LEYX	I	Latch Enable input for the Y-Read Latch. The Y-Read Latch is open when LEYX is HIGH. Data from the even path Y is latched on the HIGH-to-LOW transition of LEYX.
LEZX	I	Latch Enable input for the Z-Read Latch. The Z-Read Latch is open when LEZX is HIGH. Data from the odd path Z is latched on the HIGH-to-LOW transition of LEZX
PATH	I	Even/Odd Path Selection. When high, PATH enables data transfer between the X-Port and the Y-port (even path). When LOW, PATH enables data transfer between the X-Port and the Z-Port (odd path).
T/$\overline{R}$	I	Transmit/Receive Data. When high, Port X is an input Port and either Port Y or Z is an output Port. When LOW, Port X is an output Port while Ports Y & Z are input Ports
$\overline{OEU}$	I	Output Enable for Upper byte. When LOW, the Upper byte of data is transfered to the port specified by PATH in the direction specified by T/$\overline{R}$.
$\overline{OEL}$	I	Output Enable for Lower byte. When LOW, the Lower byte of data is transfered to the port specified by PATH in the direction specified by T/$\overline{R}$.

2527 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +125	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2527 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2527 tbl 04

1. This parameter is guaranteed by device characterization, but is not production tested.

TRUTH TABLE

Path	T/$\overline{R}$	$\overline{OEU}$	$\overline{OEL}$	Functionality
L	L	L	L	Z→X (16-bits)–Read Z(1)
L	H	L	L	X→Z (16 bits)–Write Z(1)
H	L	L	L	Y→X (16-bits)–Read Y(2)
H	H	L	L	X→Y (16 bits)–Write Y(2)
X	X	H	H	All output buffers are disabled
X	X	H	L	Transfer of lower 8 bits (0:7) as per PATH & T/$\overline{R}$
X	X	L	H	Transfer of upper 8 bits (8:15) as per PATH & T/$\overline{R}$

NOTES: 2527 tbl 01

1. For Z→X and X→Z transfers, Y-port output buffers are tristated.
2. For Y→X and X→Y transfers, Z-port output buffers are tristated.

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ARCHITECTURE OVERVIEW

The Bus Exchanger is used to service both read and write operations between the CPU and the dual memory busses. It includes independent data path elements for reads from and writes to each of the memory banks (Y and Z). Data flow control is managed by a simple set of control signals, analogous to a simple transceiver. In short, the Bus Exchanger allows bidirectional communication between ports X and Y and ports X and Z as illustrated in figure 1.

The data path elements for each port include:

Read Latch: Each of the memory ports Y and Z contains a transparent latch to capture the contents of the memory bus. Each latch features an independent latch enable.

Write Latch: Each memory port Y and Z contains an independent latch to capture data from the CPU bus during writes. Each memory port write latch features an independent latch enable, allowing write data to be directed to a specific memory port without disrupting the other memory port.

Data Flow Control Signals

T/$\overline{R}$ (Transmit/$\overline{Receive}$). This signal controls the direction of data transfer. A transmit is used for CPU writes, and a receive is used for read operations.

$\overline{OEU}$, $\overline{OEL}$ are the output enable control signals to select upper or lower bytes of all three ports.

Path: The path control signal is used to select between the even memory path Y and the odd memory path Z during read or write operations. Path selects the memory port to be connected to the CPU bus (X-port), and is independent of the latch enable signals. Thus, it is possible to transfer data from one memory port to the CPU bus (X) while capturing data from the other memory port.

MEMORY READ OPERATIONS

Latch Mode

In this mode the read operation consists of two stages. During the first stage, the data present at the memory port is captured by the read latch for that memory port. During a subsequent stage, data is brought from a selected memory port to the CPU A/D port X by using output enable control.

The read operation is selected by driving T/$\overline{R}$ LOW. The read is managed using the Path input to select the memory port (Y or Z); the LEYX/LEZX enable the data capture into the corresponding Read Latch.

In this way, memory interleaving can be performed. While data from one bank is output onto the CPU bus, data on the other bank is captured in the other memory port. In the next cycle, the Path input is changed, enabling the next data element onto the CPU bus, while the first bank is presented with a new data element.

Transparent Mode

The Bus Exchanger may be used as a data transceiver by leaving all latches open or transparent.

Memory Write Operations

Memory write operations also consist of two distinct stages. During one stage, the write data is captured into the selected memory port write latch. During a later stage, the memory is presented on the memory port bus

The write operation is selected by driving T/$\overline{R}$ HIGH. Writes are thus performed using the Path input to select the memory port (Y or Z). The LEXY/LEXZ capture data in the corresponding Write Latch.

Note that it is possible to utilize the bus exchanger's write resources as an additional write buffer, if desired; the CPU A/D bus can be freed up once the data has been captured by the Bus Exchanger.

APPLICATIONS

Use as Part of the R3051 Family ChipSet

Figure 2 shows the use of the Bus Exchanger in a typical R3051 based system.

In write transactions, the R3051 drives data on the CPU bus. The latch enables are held open through the entire write; thus, the bus exchanger is used like a transceiver. The appropriate LEXY/LEXZ signal is derived from ALE (Logic LOW- indicating that the processor is driving data) and the low order address bit. The rising edge of $\overline{Wr}$ from the CPU, ends the write operation.

During read transactions, the memory system is responsible for generating the input control signals to cause data to be captured at the memory ports. The memory controller is also responsible for acknowledging back to the CPU that the data is available, and causing the appropriate path to be selected.

The R3721 DRAM controller for the R3051 family uses the transparent latches of the read ports. The R3721 directly controls the inputs of the bus exchanger, during both reads and writes. Consult the R3721 data sheet for more information on these control signals.

Use in a general 32-bit System

Figures 3 and 4 illustrate the use of the Bus Exchanger in a 32-bit microprocessor based system. Note the reduced pin count achieved with the Bus Exchanger.

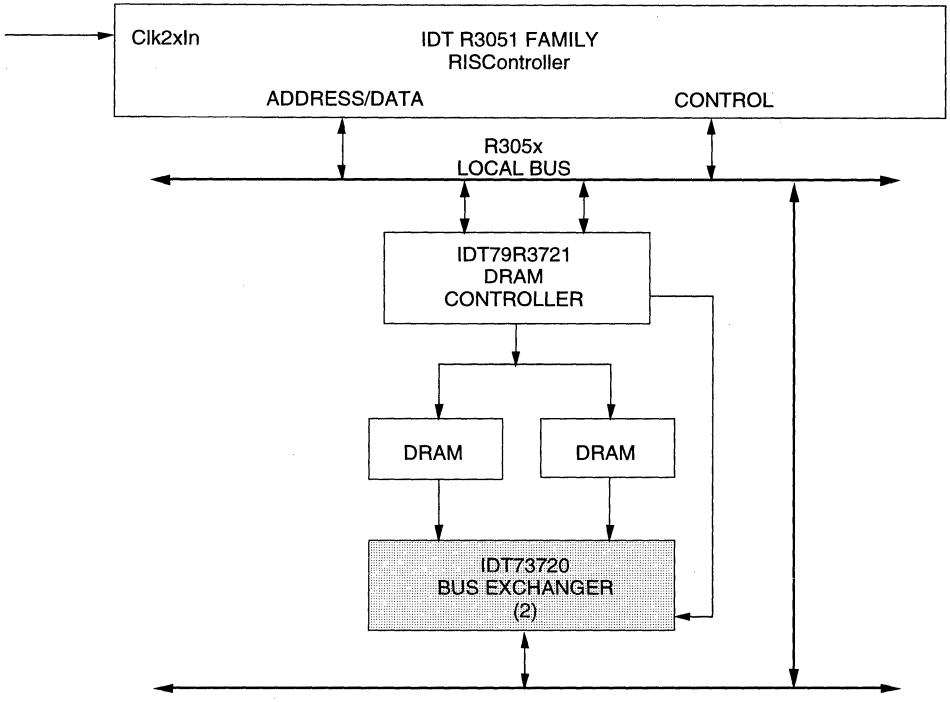
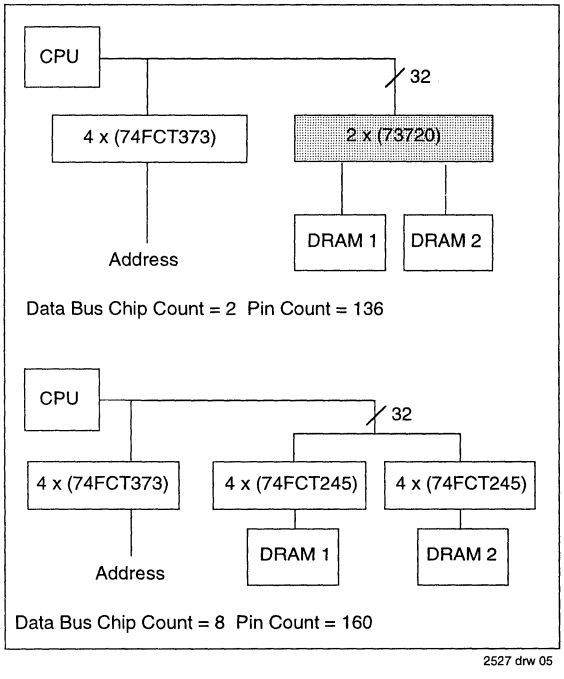


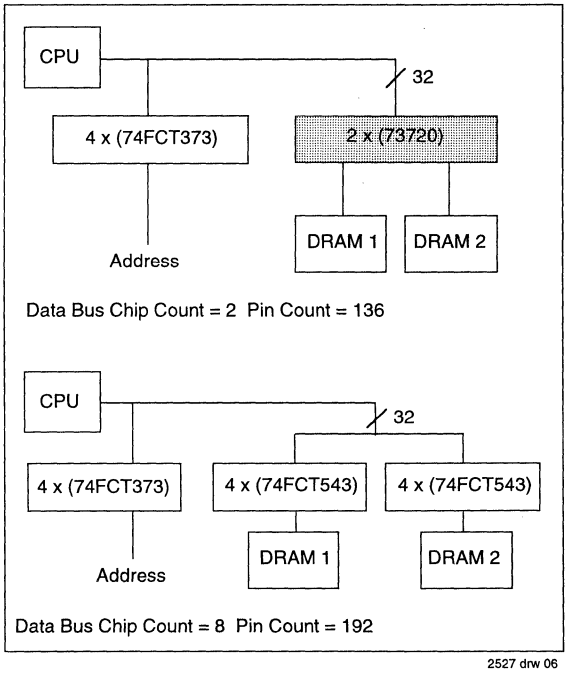
Figure 2. Bus Exchanger Used in R3051 Family System

2527 drw 04



2527 drw 05

Figure 3. CPU System with Transparent Data Path (2-way Interleaving)



2527 drw 06

Figure 4. CPU System with Latched Data Path (2-way Interleaving)

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DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level			2.0	—	—	V
V_{IL}	Input LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IH} = 2.7V	Inputs only	—	—	5.0	µA
			I/O pins	—	—	5.0	
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IL} = 0.5V	Inputs only	—	—	–5.0	µA
			I/O pins	—	—	–5.0	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}[3]	Short Circuit Current	V_{CC} = Max., V_O = GND		–60	—	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OH} = –12mA		2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}, I_{OL} = 12mA		—	0.3	0.5	V
V_H	Input Hysteresis All inputs	V_{CC} = 5V		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} =3.4 V[4]		—	0.5	2.0	mA/ Input
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. V_{IN} = V_{CC} or GND Outputs Disabled $\overline{OE}$ = V_{CC} One Input Toggling 50 % Duty Cycle		—	0.25	0.5	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. V_{IN} = V_{CC} or GND Outputs Disabled 50 % Duty Cycle $\overline{OE}$ = V_{CC} fi = 10MHz One Bit Toggling		—	2.7	6.5	mA

2527 tbl 05

NOTES:

1. For conditions shown as max. or min., use appropriate V_{CC} value.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
5. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megaherz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 5

2527 tbl 06

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

Symbol	Parameter	Test Conditions[1]	73720A		73720		Units
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	X to Y & X to Z Latches enabled	C_L = 50pF R_L = 500 Ohms	2.0	6.0	2.0	7.5	ns
t_{PLH} t_{PHL}	Y to X & Z to X Latches enabled		2.0	6.0	2.0	7.5	ns
t_{PLH} t_{PHL}	Latch Enable to Y & Z Port LEXY to Y LEXZ to Z		2.0	7.0	2.0	8.5	ns
t_{PLH} t_{PHL}	Latch Enable to X LEYX to X LEZX to X		2.0	7.0	2.0	8.5	ns
t_{PLH} t_{PHL}	Path to X Port Propagation Delay		2.0	7.0	2.0	8.5	ns
t_{HZ} t_{LZ}	Y & Z Port Disable Time (T/$\overline{R}$, PATH, $\overline{OEU}$, $\overline{OEL}$)[3]		2.0	8.5	2.0	9.5	ns
t_{ZH} t_{ZL}	Y & Z Port Enable Time (T/$\overline{R}$, PATH, $\overline{OEU}$, $\overline{OEL}$)[3]		2.0	9.5	2.0	10.5	ns
t_{HZ} t_{LZ}	X-Port DisableTime (T/$\overline{R}$, $\overline{OEU}$, $\overline{OEL}$)[3]		2.0	8.5	2.0	9.5	ns
t_{ZH} t_{ZL}	X-Port Enable Time (T/$\overline{R}$, $\overline{OEU}$, $\overline{OEL}$)[3]		2.0	9.5	2.0	10.5	ns
t_{SU}	Port to LE Set-up time		2.0	—	2.0	—	ns
t_H	Port to LE Hold time		1.5	—	1.5	—	ns
t_W	LE Pulse Width, HIGH or LOW[2]		3	—	4	—	ns

2527 tbl 07

NOTES:
1. All timings are referenced to 1.5 V.
2. Minimum Delay Times, Enable Times, Disable Times and Pulse Width are guaranteed by design, but not tested.
3. Bus turnaround times are guaranteed by design, but not tested. (T/$\overline{R}$ enable/disable times).

TEST CIRCUITS AND WAVEFORMS

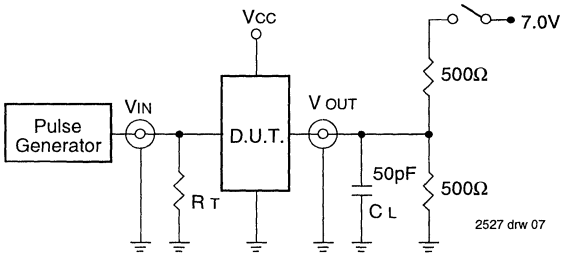


Figure 5. Test Circuit for all outputs

SWITCH POSITION

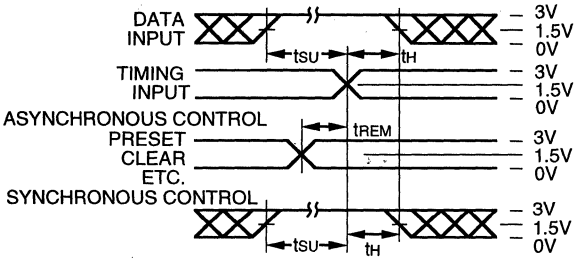
Test	Switch
Disable LOW Enable LOW	Closed
All Other Tests	Open

2527 tbl 08

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

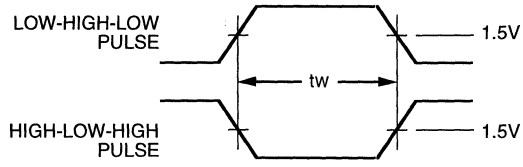
11

SET-UP, HOLD AND RELEASE TIMES



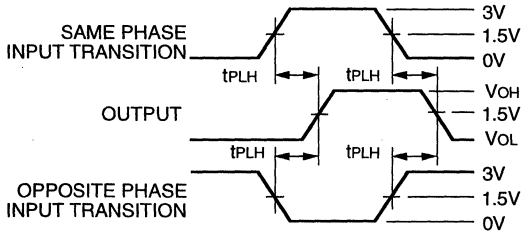
2527 drw 08

PULSE WIDTH



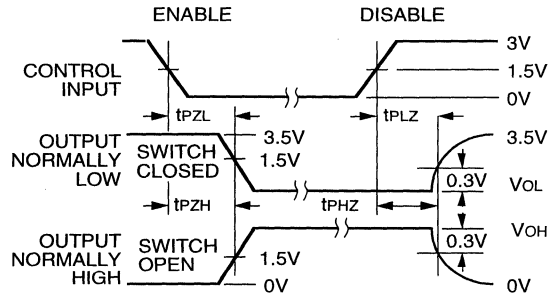
2527 drw 09

PROPAGATION DELAY



2527 drw 10

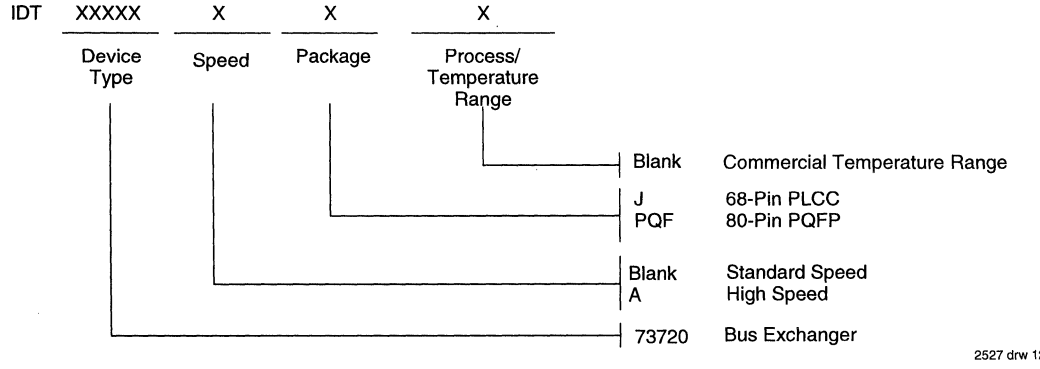
ENABLE AND DISABLE TIMES



2527 drw 11

NOTES:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; ZO ≤ 50Ω; tF ≤ 2.5ns; tR ≤ 2.5ns.

ORDERING INFORMATION



2527 drw 12

Integrated Device Technology, Inc.

32-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT49C460
IDT49C460A
IDT49C460B
IDT49C460C
IDT49C460D
IDT49C460E

FEATURES:

- Fast

	Detect	Correct
— IDT49C460E	10ns (max.)	14ns (max.)
— IDT49C460D	12ns (max.)	18ns (max.)
— IDT49C460C	16ns (max.)	24ns (max.)
— IDT49C460B	25ns (max.)	30ns (max.)
— IDT49C460A	30ns (max.)	36ns (max.)
— IDT49C460	40ns (max.)	49ns (max.)

- Low-power CMOS
  - — Commercial: 95mA (max.)
  - — Military: 125mA (max.)
- Improves system memory reliability
  - — Corrects all single bit errors, detects all double and some triple-bit errors
- Cascadable
  - — Data words up to 64-bits
- Built-in diagnostics
  - — Capable of verifying proper EDC operation via software control
- Simplified byte operations
  - — Fast byte writes possible with separate byte enables
- Functional replacement for 32- and 64-bit configurations of the AM29C60 and AM29C660
- Available in PGA, PLCC and Fine Pitch Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962–88533

DESCRIPTION:

The IDT49C460s are high-speed, low-power, 32-bit Error Detection and Correction Units which generate check bits on a 32-bit data field according to a modified Hamming Code and correct the data word when check bits are supplied. The IDT49C460s are performance-enhanced functional replacements for 32-bit versions of the 2960. When performing a read operation from memory, the IDT49C460s will correct 100% of all single bit errors and will detect all double bit errors and some triple bit errors.

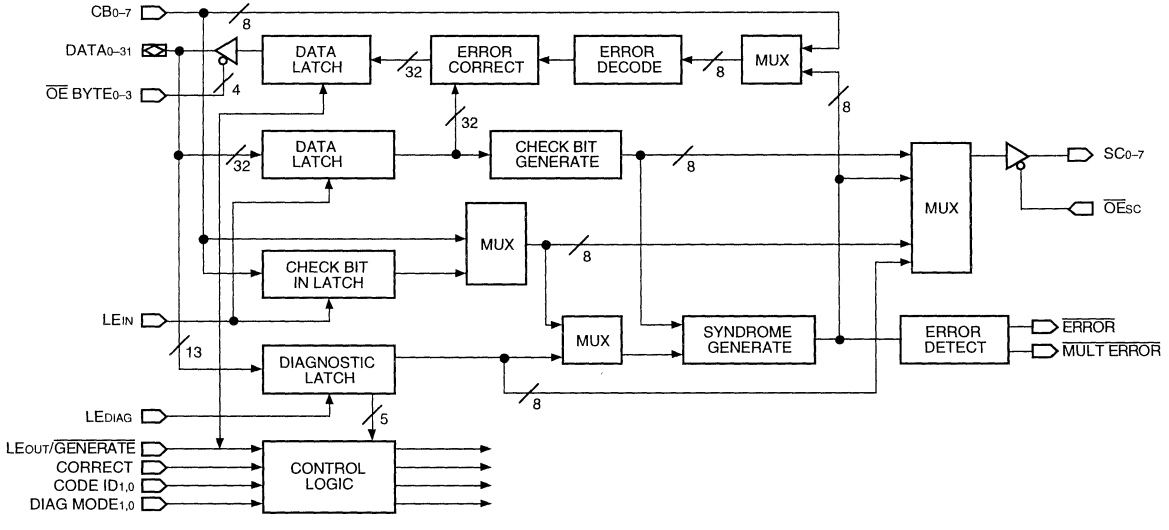
The IDT49C460s are easily cascadable to 64-bits. Thirty-two-bit systems use 7 check bits and 64-bit systems use 8 check bits. For both configurations, the error syndrome is made available.

The IDT49C460s incorporate two built-in diagnostic modes. Both simplify testing by allowing for diagnostic data to be entered into the device and to execute system diagnostics functions.

They are fabricated using a CMOS technology designed for high-performance and high-reliability. The devices are packaged in a 68-pin ceramic PGA, PLCC and Ceramic Quad Flatpack.

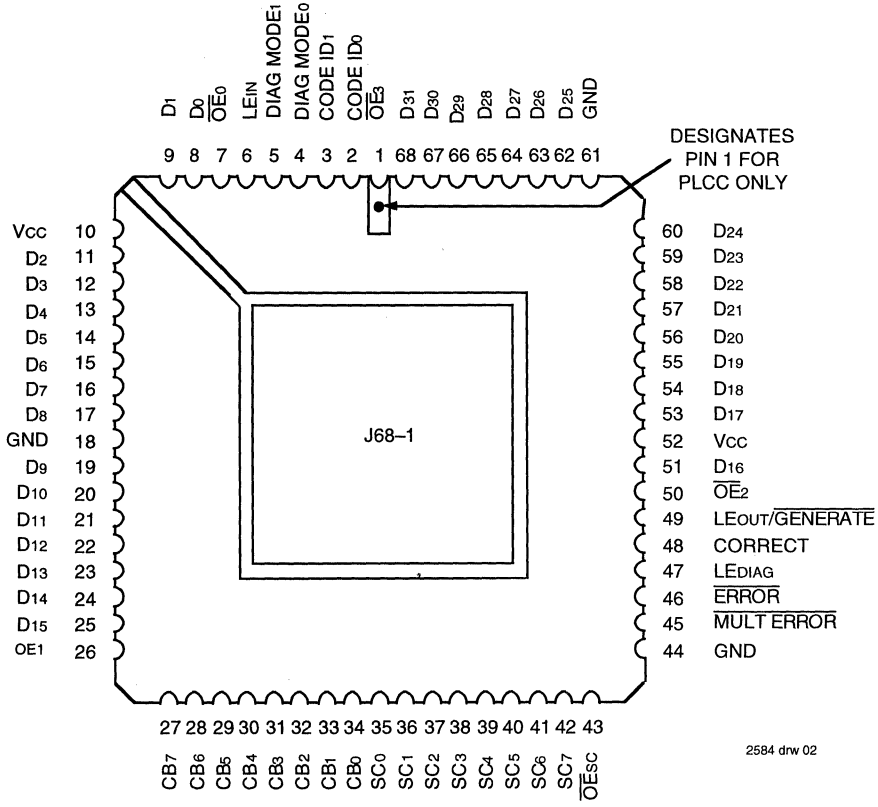
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

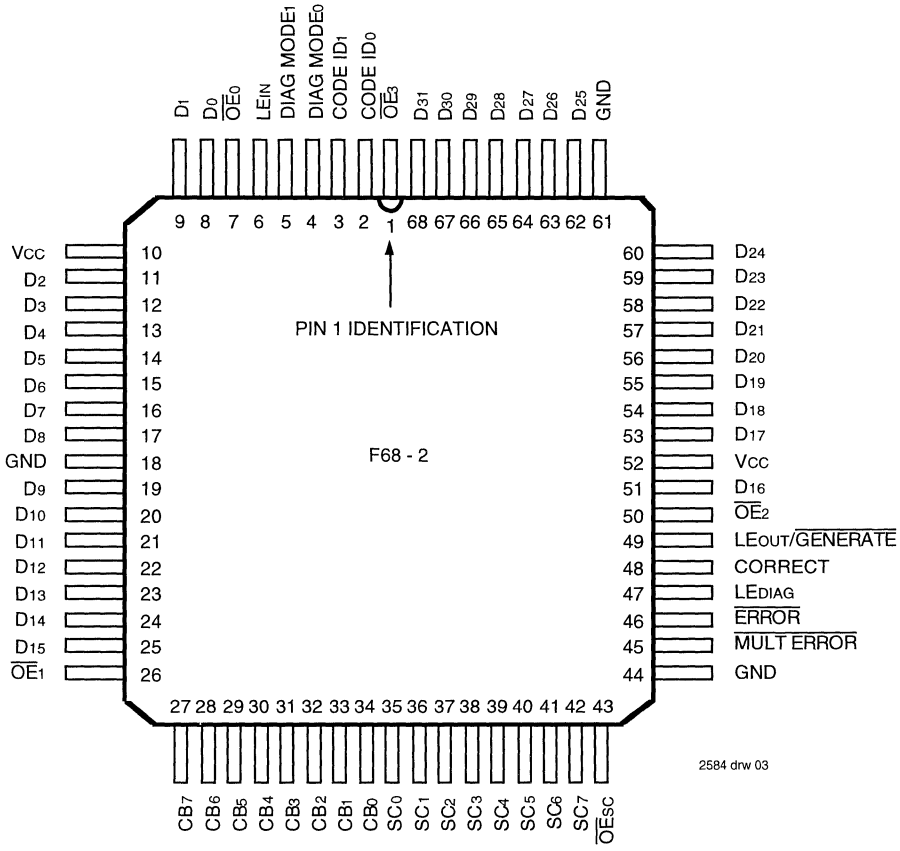


2584 drw 01

PIN CONFIGURATIONS

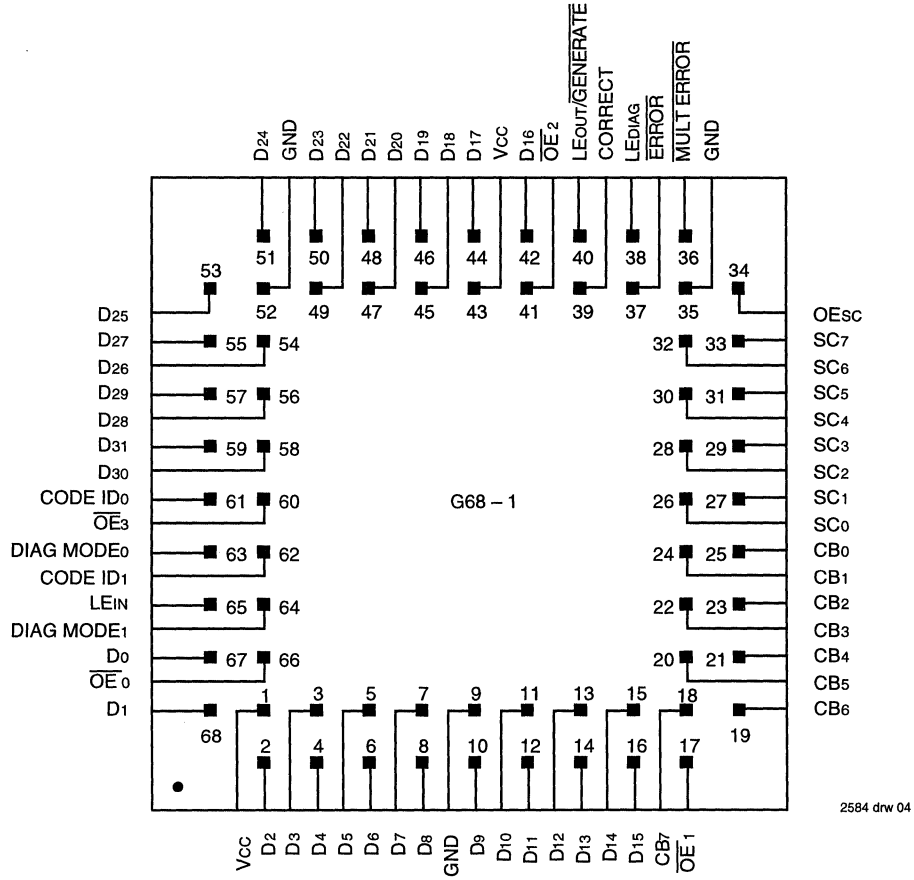


PLCC
TOPVIEW



FINE PITCH FLATPACK
TOPVIEW

11


D24
GND
D23
D22
D21
D20
D19
D18
D17
VCC
D16
OE2
LEOUT/GENERATE
CORRECT
LEDIAG
ERROR
MULT ERROR
GND
D25
D27
D26
D29
D28
D31
D30
CODE ID0
OE3
DIAG MODE0
CODE ID1
LEIN
DIAG MODE1
D0
OE0
D1
OESC
SC7
SC6
SC5
SC4
SC3
SC2
SC1
SC0
CB0
CB1
CB2
CB3
CB4
CB5
CB6
G68 – 1
VCC
D2
D3
D4
D5
D6
D7
D8
GND
D9
D10
D11
D12
D13
D14
D15
CB7
OE1
2584 drw 04

PGA
TOPVIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
$DATA_{0-31}$	I/O	32 bidirectional data lines provide input to the Data Input Latch and Diagnostic Latch and also receive output from the Data Output Latch. $DATA_0$ is the LSB; $DATA_{31}$ is the MSB.
CB_{0-7}	I	Eight check bit input lines input check bits for error detection and also used to input syndrome bits for error correction in 64-bit applications.
LE_{IN}	I	Latch Enable is for the Data Input Latch. Controls latching of the input data. Data Input Latch and Check Bit Input Latch are latched to their previous state when LOW. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits.
LE_{OUT}/ $\overline{GENERATE}$		A multifunction pin which, when LOW, is in the Check Bit Generate Mode. In this mode, the device generates the check bits or GENERATE partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. Also, when LOW, the Data Out Latch is latched to its previous state. When HIGH, the device is in the Detect or Correct Mode. In this mode, the device detects single and multiple errors and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In the Correct Mode, single bit errors are also automatically corrected and the corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the specific bit-in-error. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single bit errors are corrected by the network before being loaded into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The Data Output Latch is disabled, with its contents unchanged, if the EDC is in the Generate Mode.
SC_{0-7}	O	Syndrome Check Bit outputs. Eight outputs which hold the check bits and partial check bits when the EDC is in the Generate Mode and will hold the syndrome/partial syndrome bits when the device is in the Detect or Correct modes. All are 3-state outputs.
$\overline{OE}_{SC}$	I	Output Enable—Syndrome Check Bits. In the HIGH condition, the SC outputs are in the high impedance state. When LOW, all SC output lines are enabled.
$\overline{ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if one or more data or check bits contain an error. When HIGH, no errors have been detected. This pin is forced HIGH in the Generate Mode.
$\overline{MULT}$ $\overline{ERROR}$	O	In the Detect or Correct Mode, this output will go LOW if two or more bit errors have been detected. A HIGH level indicates that either one or no errors have been detected. This pin is forced HIGH in the Generate Mode.
CORRECT	I	The correct input which, when HIGH, allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the device will drive data directly from the Data Input Latch to the Data Output Latch without correction.
$\overline{OE}$ $BYTE_{0-3}$	I	Output Enable—Bytes 0, 1, 2, 3. Data Output Latch. Control the three-state output buffers for each of the four bytes of the Data Output Latch. When LOW, they enable the output buffer of the Data Output Latch. When HIGH, they force the Data Output Latch buffer into the high impedance mode. One byte of the Data Output Latch is easily activated by separately selecting the four enable lines.
DIAG $MODE_{1,0}$	I	Select the proper diagnostic mode. They control the initialization, diagnostic and normal operation of the EDC.
CODE $ID_{1,0}$	I	These two code identification inputs identify the size of the total data word to be processed. The two allowable data word sizes are 32 and 64 bits and their respective modified Hamming Codes are designated 32/39 and 64/72. Special CODE $ID_{1,0}$, input 01 is also used to instruct the EDC that the signals CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT are to be taken from the Diagnostic Latch rather than from the input control lines.
LE_{DIAG}	I	This is the Latch Enable for the Diagnostic Latch. When HIGH, the Diagnostic Latch follows the 32-bit data on the input lines. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT.

2584 tbl 01

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EDC ARCHITECTURE SUMMARY

The IDT49C460s are high-performance cascadable EDCs used for check bit generation, error detection, error correction and diagnostics. The function blocks for this 32-bit device consist of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

DATA INPUT/OUTPUT LATCH

The Latch Enable Input, LE_{IN}, controls the loading of 32 bits of data to the Data In Latch. The data from the DATA lines can be loaded in the Diagnostic Latch under control of the Diagnostic Latch Enable, LE_{DIAG}, giving check bit information in one byte and control information in another byte. The Diagnostic Latch is used in the Internal Control Mode or in one of the diagnostic modes. The Data Output Latch has buffers that place data on the DATA lines. These buffers are split into four 8-bit buffers, each having their own output enable controls. This feature facilitates byte read and byte modify operations.

CHECK BIT GENERATION LOGIC

This generates the appropriate check bits for the 32 bits of data in the Data Input Latch. The modified Hamming Code is the basis for generating the proper check bits.

SYNDROME GENERATION LOGIC

In both the Detect and Correct modes, this logic does a comparison on the check bits read from memory against the newly generated set of check bits produced for the data read in from memory. Matching sets of check bits mean no error was detected. If there is a mismatch, one or more of the data or check bits is in error. Syndrome bits are produced by an exclusive-OR of the two sets of check bits. Identical sets of check bits mean the syndrome bits will be all zeros. If an error results, the syndrome bits can be decoded to determine the number of errors and the specific bit-in-error.

ERROR DETECTION LOGIC

This part of the device decodes the syndrome bits generated by the Syndrome Generation Logic. With no errors in either the input data or check bits, both the $\overline{ERROR}$ and $\overline{MULTERROR}$ outputs are HIGH. ERROR will go low if one error is detected. $\overline{MULTERROR}$ and $\overline{ERROR}$ will both go low if two or more errors are detected.

ERROR CORRECTION LOGIC

In single error cases, this logic complements (corrects) the single data bit-in-error. This corrected data is loaded into the Data Output Latch, which can then be read onto the bidirectional data lines. If the error is resulting from one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed, the EDC must be switched to the Generate Mode.

DATA OUTPUT LATCH AND OUTPUT BUFFERS

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE_{OUT}. The Data Output Latch may also be directly loaded from the Data Input Latch in the PASSTHRU mode. The Data Output Latch buffer is split into 4 individual buffers which can be enabled by $\overline{OE}_{0-3}$ separately for reading onto the bidirectional data lines.

DIAGNOSTIC LATCH

The diagnostic latch is loadable under control of the Diagnostic Latch Enable, LE_{DIAG}, from the bidirectional data lines. Check bit information is contained in one byte while the other byte contains the control information. The Diagnostic Latch is used for driving the device when in the Internal Control Mode, or for supplying check bits when in one of the diagnostic modes.

CONTROL LOGIC

Specifies in which mode the device will be operating in. Normal operation is when the control logic is driven by external control inputs. In the Internal Control Mode, the control signals are read from the Diagnostic Latch. Since LE_{OUT} and $\overline{GENERATE}$ are controlled by the same pin, the latching action (LE_{OUT} from high to low) of the Data Output Latch causes the EDC to go into the Generate Mode.

DETAILED PRODUCT DESCRIPTION

The IDT49C460 EDC units contain the logic necessary to generate check bits on 32 bits of data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 32-bit data to allow correction of any single bit data error and detection of all double (and some triple) bit errors. The IDT49C460s can be used for 32-bit data words (7 check bits) and 64-bit (8 check bits) data words.

WORD SIZE SELECTION

The two code identification pins, CODE $ID_{1,0}$, are used to determine the data word size that is 32 or 64 bits. They also select the Internal Control Mode. Table 4 defines all possible slice identification codes.

CHECK AND SYNDROME BITS

The IDT49C460s provide either check bits or syndrome bits on the three-state output pins, SC_{0-7}. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit in error or that a double (some triple) error was detected. The check bits are labeled:

$C_0, C_1, C_2, C_3, C_4, C_5, C_6$ for the 32-bit configuration
$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$ for the 64-bit configuration

Syndrome bits are similarly labeled S_0 through S_7.

Correct	Diag $Mode_0$	Diag $Mode_1$	Diagnostic Mode Selected
X	0	0	**Non-diagnostic Mode.** Normal EDC function in this mode.
X	0	1	**Diagnostic Generate.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes.
0/1	1	0	**Diagnostic Detect/Correct.** In either mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode.
1	1	1	**Initialize.** The Data Input Latch outputs are forced to zeros and latched upon removal of Initialize Mode.
0	1	1	**PASSTHRU.**

2584 tbl 02

Table 2. Diagnostic Mode Control

Operating Mode	DM_0	DM_1	Generate	Correct	$DATA_{OUT}$ Latch	$\overline{SC}_{0-7}$ ($\overline{OE}_{SC}$ = LOW)	$\overline{ERROR}$ / $\overline{MULT\ ERROR}$
Generate	0 1	0 0	0	X	LE_{OUT} = LOW (1)	Check Bits Generated from $DATA_{IN}$ Latch	High
Detect	0 0	0 1	1	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep (2)
Correct	0 0	0 1	1	1	$DATA_{IN}$ Latch w/ Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Check Bit Latch	Error Dep
PASSTHRU	1	1	1	0	$DATA_{IN}$ Latch	Check Bit Latch	High
Diagnostic Generate	0	1	0	X	—	Check Bits from Diagnostic Latch	High
Diagnostic Detect	1	0	1	0	$DATA_{IN}$ Latch	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Diagnostic Correct	1	0	1	1	$DATA_{IN}$ Latch w/ Single Bit Correction	Syndrome Bits $DATA_{IN}$/ Diagnostic Latch	Error Dep
Initialization	1	1	1	1	$DATA_{IN}$ Latch Set to 0000(3)	—	—
Internal	CODE $ID_{1,0}$ = 01 (Control Signals CODE $ID_{1,0}$, DIAG $MODE_{1,0}$ and CORRECT are taken from Diagnostic Latch.)						

NOTES:
2584 tbl 03

1. In Generate Mode, data is read into the EDC unit and the check bits are generated. The same data is written to memory along with the check bits. Since the $DATA_{OUT}$ Latch is not used in the Generate Mode, LE_{OUT} (being LOW since it is tied to Generate) does not affect the writing of check bits.
2. Error Dep (Error Dependent): $\overline{ERROR}$ will be low for single or multiple errors, with $\overline{MULT\ ERROR}$ low for double or multiple errors. Both signals are high for no errors.
3. LE_{IN} is LOW.

Table 3. IDT49C460 Operating Modes

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OPERATING MODE SELECTION

Tables 2 and 3 describe the nine operating modes of the IDT49C460s. The Diagnostic Mode pins — DIAG MODE$_{0,1}$ — define four basic areas of operation. GENERATE and CORRECT further divide operation into 8 functions, with CODE ID$_{1,0}$ defining the ninth mode as the Internal Mode.

Generate Mode is used to display the check bits on the outputs SC$_{0-7}$. The Diagnostic Generate Mode displays check bits as stored in the Diagnostic Latch.

Detect Mode provides an indication of errors or multiple errors on the outputs ERROR and MULT ERROR. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC$_{0-7}$. For the Diagnostic Detect Mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct Mode is similar to the Detect Mode except that single bit errors will be complemented (corrected) and made available as input to the Data Out Latches. Again, the Diagnostic Correct Mode will correct single bit errors as determined by syndrome bits generated from the data input and contents of the diagnostic latches.

The Initialize Mode provides check bits for all zero bit data. Data Input Latches are set, latched to a logic zero and made available as input to the Data Out Latches.

The Internal Mode disables the external control pins DIAG MODE$_{0,1}$ and CORRECT to be defined by the Diagnostic Latch. Even CODE ID$_{1,0}$, although externally set to the 01 code, can be redefined from the Diagnostic Latch data.

Code ID$_1$	Code ID$_0$	Slice Selected
0	0	32-Bit
0	1	Internal Control Mode
1	0	64-Bit, Lower 32-Bit (0–31)
1	1	64-Bit, Upper 32-Bit (32–63)

2584 tbl 04

Table 4. Slice Identification

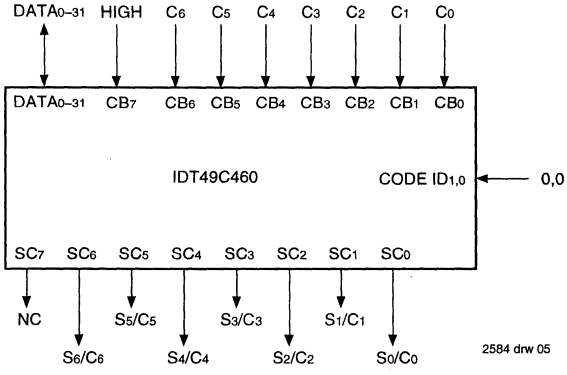

Figure 1. 32-Bit Configuration

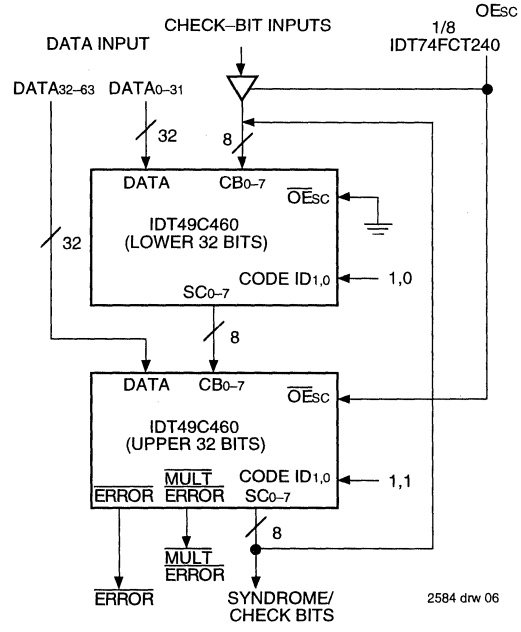

Figure 2. 64-Bit Configuration

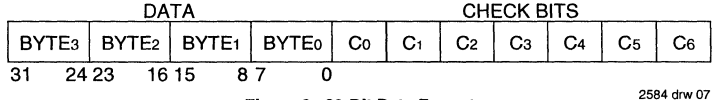

Figure 3. 32-Bit Data Format

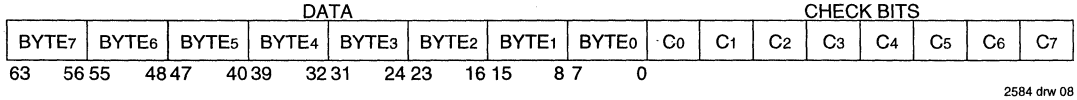

Figure 4. 64-Bit Data Format

32-BIT DATA WORD CONFIGURATION

A single IDT49C460 EDC unit, connected as shown in Figure 1, provides all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code indicates 7 check bits are required. The CB_7 pin should be HIGH.

Figure 3 indicates the 39-bit data format for two bytes of data and 7 check bits. Table 3 describes the operating mode available.

Table 6 indicates the data bits participating in the check bit generation. For example, check bit C_0 is the exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits from the respective latch are passed, unchanged, in the PASSTHRU or Diagnostic Generate Mode.

Syndrome bits are generated by an exclusive-OR or the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 5 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

BIT 0	CB_0 DIAGNOSTIC
BIT 1	CB_1 DIAGNOSTIC
BIT 2	CB_2 DIAGNOSTIC
BIT 3	CB_3 DIAGNOSTIC
BIT 4	CB_4 DIAGNOSTIC
BIT 5	CB_5 DIAGNOSTIC
BIT 6	CB_6 DIAGNOSTIC
BIT 7	CB_7 DIAGNOSTIC
BIT 8	CODE ID_0
BIT 9	CODE ID_1
BIT 10	DIAG $MODE_0$
BIT 11	DIAG $MODE_1$
BIT 12	CORRECT
BIT 13–31	DON'T CARE

2584 drw 05

Table 5. 32-Bit Diagnostic Latch Coding Format

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)	X				X		X	X	X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								

2584 tbl 06

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X					X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X

2584 tbl 07

Table 6. 32–Bit Modified Hamming Code–Check Bit Encode Chart

11

					Hex	0	1	2	3	4	5	6	7
					S_6	0	0	0	0	1	1	1	1
	Syndrome Bits				S_5	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	T
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

NOTES:
1. * = No errors detected
2. Number = The number of the single bit-in-error
3. T = Two errors detected
4. M = Three or more errors detected

2584 tbl 08

Table 7. Syndrome Decode to Bit-in-Error (32-Bit)

64-BIT DATA WORD CONFIGURATION

Two IDT49C460 EDC units, connected as shown in Figure 2, provide all the logic needed for single bit error detection and double bit error detection of a 64-bit data field. Table 4 gives the CODE $ID_{1,0}$ values needed for distinguishing the upper 32 bits from the lower 32 bits. Valid syndrome, check bits and the $\overline{ERROR}$ and $\overline{MULT\ ERROR}$ signals come from the IC with the CODE $ID_{1,0} = 11$. Control signals not indicated are connected to both units in parallel. The EDC with the CODE $ID_{1,0} = 10$ has the $\overline{OE}_{SC}$ grounded. The $\overline{OE}_{SC}$ selects the syndrome bits from the EDC with CODE $ID_{1,0} = 11$ and also controls the check bit buffers from memory.

Data In bits 0 through 31 are connected to the same numbered inputs of the EDC unit with CODE $ID_{1,0} = 10$, while Data In bits 32 through 63 are connected to Data Inputs 0 to 31, respectively, for the EDC unit with CODE $ID_{1,0} = 11$.

Figure 4 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the EDC unit with CODE $ID_{1,0} = 10$ through a three-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits from the upper EDC unit to the lower EDC unit. The MUX shown on the functional block diagram is used to select the CB_{0-7} pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Table 11 indicates the data bits participating in the check bit generation. For example, check bit C_0 is the exclusive-OR function of the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization modes. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate modes.

Syndrome bits are generated by an exclusive-OR of the generated check bits with the read check bits. For example, S_n is the XOR of check bits C_n from those read with those generated. Table 9 indicates the decoding of the 8 syndrome bits to determine the bit in error for a single bit error or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Tables 8A and 8B define the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC_{0-7} outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Performance data is provided in Table 10, relating a single IDT49C460 EDC with the two cascaded units of Figure 2. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Bit	Internal Function
0	CB_0 DIAGNOSTIC
1	CB_1 DIAGNOSTIC
2	CB_2 DIAGNOSTIC
3	CB_3 DIAGNOSTIC
4	CB_4 DIAGNOSTIC
5	CB_5 DIAGNOSTIC
6	CB_6 DIAGNOSTIC
7	CB_7 DIAGNOSTIC
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13–31	DON'T CARE
32–39	DON'T CARE
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45–63	DON'T CARE

2584 tbl 09

Table 8A. 64-Bit Diagnostic Latch–Coding Format (Diagnostic and Correct Mode)

Bit	Internal Function
0–7	DON'T CARE
8	CODE ID_0 LOWER 32-BIT
9	CODE ID_1 LOWER 32-BIT
10	DIAG $MODE_0$ LOWER 32-BIT
11	DIAG $MODE_1$ LOWER 32-BIT
12	CORRECT LOWER 32-BIT
13–31	DON'T CARE
32	CB_0 DIAGNOSTIC
33	CB_1 DIAGNOSTIC
34	CB_2 DIAGNOSTIC
35	CB_3 DIAGNOSTIC
36	CB_4 DIAGNOSTIC
37	CB_5 DIAGNOSTIC
38	CB_6 DIAGNOSTIC
39	CB_7 DIAGNOSTIC
40	CODE ID_0 UPPER 32-BIT
41	CODE ID_1 UPPER 32-BIT
42	DIAG $MODE_0$ UPPER 32-BIT
43	DIAG $MODE_1$ UPPER 32-BIT
44	CORRECT UPPER 32-BIT
45–63	DON'T CARE

2584 tbl 10

Table 8B. 64-Bit Diagnostic Latch–Coding Format (Diagnostic and Correct Mode)

					Hex	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
					S_7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Syndrome Bits					S_6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
					S_5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
					S_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Hex	S_3	S_2	S_1	S_0																	
0	0	0	0	0		*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1		C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0		C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1		T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0		C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1		T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0		T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1		M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0		C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1		T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0		T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1		17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0		T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1		M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0		16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1		T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES:
* = No errors detected
Number = The number of the single bit-in-error
T = Two errors detected
M = Three or more errors detected

2584 tbl 11

Table 9. Syndrome Decode to Bit–In–Error (64–Bit Configuration)

11

64–Bit Propagation Delay		Component Delay for IDT49C460 AC Specifications
From	To	
DATA	Check Bits Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	Corrected $DATA_{OUT}$	(DATA TO SC) + (CB TO SC, CODE ID 11) + (CB TO DATA, CODE ID 10)
DATA	Syndromes Out	(DATA TO SC) + (CB TO SC, CODE ID 11)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{ERROR}}$, CODE ID 11)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA TO SC) + (CB TO $\overline{\text{MULT ERROR}}$, CODE ID 11)

2584 tbl 12

Table 10. Key Calculations for the 64–Bit Configuration

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

2584 tbl 13

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
C_0	Even (XOR)		X	X	X		X			X	X		X			X	
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2584 tbl 14

Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)	X	X	X	X	X	X	X	X								
C_7	Even (XOR)									X	X	X	X	X	X	X	X

2584 tbl 15

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
C_0	Even (XOR)	X				X		X	X			X		X	X		X
C_1	Even (XOR)	X	X	X		X		X		X		X		X			
C_2	Odd (XNOR)	X			X	X			X		X	X			X		X
C_3	Odd (XNOR)	X	X				X	X	X				X	X	X		
C_4	Even (XOR)			X	X	X	X	X	X							X	X
C_5	Even (XOR)									X	X	X	X	X	X	X	X
C_6	Even (XOR)									X	X	X	X	X	X	X	X
C_7	Even (XOR)	X	X	X	X	X	X	X	X								

NOTE:
1. The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

2584 tbl 16

Table 11. 64–Bit Modified Hamming Code–Check Bit Encoding

11

SC OUTPUTS

The tables below indicate how the SC_{0-7} outputs are generated in each control mode of various CODE IDs (Internal Control Mode not applicable).

Generate	CODE $ID_{1,0}$ 00	10	11
$SC_0 \leftarrow$	PH0	PH1	PH2 ⊕ CB_0
$SC_1 \leftarrow$	PA	PA	PA ⊕ CB_1
$SC_2 \leftarrow$	PB	PB	PB ⊕ CB_2
$SC_3 \leftarrow$	PC	PC	PC ⊕ CB_3
$SC_4 \leftarrow$	PD	PD	PD ⊕ CB_4
$SC_5 \leftarrow$	PE	PE	PE ⊕ CB_5
$SC_6 \leftarrow$	PF	PF	PF ⊕ CB_6
$SC_7 \leftarrow$	—	PF	PG ⊕ CB_7
	Final Check Bits	Partial Check Bits	Final Check Bits

2584 tbl 17

Correct/ Detect	CODE $ID_{1,0}$ 00	10	11
$SC_0 \leftarrow$	PH0 ⊕ C_0	PH1 ⊕ C_0	PH2 ⊕ CB_0
$SC_1 \leftarrow$	PA ⊕ C_1	PA ⊕ C_1	PA ⊕ CB_1
$SC_2 \leftarrow$	PB ⊕ C_2	PB ⊕ C_2	PB ⊕ CB_2
$SC_3 \leftarrow$	PC ⊕ C_3	PC ⊕ C_3	PC ⊕ CB_3
$SC_4 \leftarrow$	PD ⊕ C_4	PD ⊕ C_4	PD ⊕ CB_4
$SC_5 \leftarrow$	PE ⊕ C_5	PE ⊕ C_5	PE ⊕ CB_5
$SC_6 \leftarrow$	PF ⊕ C_6	PF ⊕ C_6	PF ⊕ CB_6
$SC_7 \leftarrow$	—	PF ⊕ C_7	PG ⊕ CB_7
	Final Syndrome	Partial Syndrome	Final Syndrome

2584 tbl 19

Diagnostic Generate	CODE $ID_{1,0}$ 00	10	11
$SC_0 \leftarrow$	DL0	DL0	DL32
$SC_1 \leftarrow$	DL1	DL1	DL33
$SC_2 \leftarrow$	DL2	DL2	DL34
$SC_3 \leftarrow$	DL3	DL3	DL35
$SC_4 \leftarrow$	DL4	DL4	DL36
$SC_5 \leftarrow$	DL5	DL5	DL37
$SC_6 \leftarrow$	DL6	DL6	DL38
$SC_7 \leftarrow$	—	DL7	DL39
	Final Check Bits	Partial Check Bits	Final Check Bits

2584 tbl 18

Diagnostic Correct/ Detect	CODE $ID_{1,0}$ 00	10	11
$SC_0 \leftarrow$	PH0 ⊕ DL0	PH1 ⊕ DL0	PH2 ⊕ CB_0
$SC_1 \leftarrow$	PA ⊕ DL1	PA ⊕ DL1	PA ⊕ CB_1
$SC_2 \leftarrow$	PB ⊕ DL2	PB ⊕ DL2	PB ⊕ CB_2
$SC_3 \leftarrow$	PC ⊕ DL3	PC ⊕ DL3	PC ⊕ CB_3
$SC_4 \leftarrow$	PD ⊕ DL4	PD ⊕ DL4	PD ⊕ CB_4
$SC_5 \leftarrow$	PE ⊕ DL5	PE ⊕ DL5	PE ⊕ CB_5
$SC_6 \leftarrow$	PF ⊕ DL6	PF ⊕ DL6	PF ⊕ CB_6
$SC_7 \leftarrow$	—	PF ⊕ DL7	PG ⊕ CB_7
	Final Syndrome	Partial Syndrome	Final Syndrome

2584 tbl 20

PASSTHRU	CODE $ID_{1,0}$ 00	10	11
$SC_0 \leftarrow$	C0	C0	CB_0
$SC_1 \leftarrow$	C1	C1	CB_1
$SC_2 \leftarrow$	C2	C2	CB_2
$SC_3 \leftarrow$	C3	C3	CB_3
$SC_4 \leftarrow$	C4	C4	CB_4
$SC_5 \leftarrow$	C5	C5	CB_5
$SC_6 \leftarrow$	C6	C6	CB_6
$SC_7 \leftarrow$	—	C7	CB_7

2584 tbl 21

Table 12. SC0-7 Outputs For Different Control Modes

DATA CORRECTION

The tables below indicate which data output bits are corrected depending upon the syndromes and the CODE $ID_{1,0}$ position. The syndromes that determine data correction are, in some cases, syndromes input externally via the CB inputs and, in some cases, syndromes input externally by that EDC (S_i are the internal syndromes and are the same as the value of the SC_i output of that EDC if enabled).

FUNCTIONAL EQUATIONS

The equations below describe the IDT49C460 output values as defined by the value of the inputs and internal states.

DEFINITIONS

$$PA = D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{20} \oplus D_{22} \oplus D_{24} \oplus D_{26} \oplus D_{28}$$

$$\overline{PB} = D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{19} \oplus D_{20} \oplus D_{23} \oplus D_{25} \oplus D_{26} \oplus D_{29} \oplus D_{31}$$

$$\overline{PC} = D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{16} \oplus D_{17} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{27} \oplus D_{28} \oplus D_{29}$$

$$PD = D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{14} \oplus D_{15} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{30} \oplus D_{31}$$

$$PE = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$$

$$PF = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$$

$$PG = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23}$$

$$PH0 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$$

$$PH1 = D_1 \oplus D_2 \oplus D_3 \oplus D_5 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{24} \oplus D_{25} \oplus D_{27} \oplus D_{30}$$

$$PH2 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{20} \oplus D_{22} \oplus D_{23} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$$

11

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to VCC + 0.5V	–0.5 to VCC + 0.5V	V
VCC	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	30	30	mA

NOTE: 2584 tbl 24

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = + 25°C, f = 1.0MHz)

Symbol	Parameter (1)	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE: 2584 tbl 25

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: VLC = 0.2V; VHC = VCC – 0.2V
Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = –55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions (1)		Min.	Typ. (2)	Max.	Unit
VIH	Input HIGH Level	Guaranteed Logic HIGH Level(4)		2.0	—	—	V
VIL	Input LOW Level	Guaranteed Logic LOW Level(4)		—	—	0.8	V
IIH	Input HIGH Current	VCC = Max., VIN = VCC		—	0.1	10.0	µA
IIL	Input LOW Current	VCC = Max., VIN = GND		—	–0.1	–10.0	µA
VOH	Output HIGH Voltage	VCC = Min.	IOH = 300µA	VCC	—	—	V
			IOH = –12mA Mil.	2.4	4.3	—	
			IOH = –15mA Com'l.	2.4	4.3	—	
VOL	Output LOW Voltage	VCC = Min.	IOL = 300µA	—	—	GND	V
			IOL = 12mA Mil.	—	0.3	0.5	
			IOL = 16mA Com'l.	—	0.3	0.5	
IOZ	Off State (High Impedance) Output Current	VCC = Max.	VO = 0V	—	–0.1	–20.0	µA
			VO = VCC (Max.)	—	0.1	20.0	
IOS	Output Short Circuit Current	VCC = Max., VOUT = 0V (3)		–30.0	—	—	mA

NOTES: 2584 tbl 26

1. For conditions shown as Max. or Min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, + 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current (CMOS Inputs)	V_{CC} = Max.; All Inputs $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{OP} = 0; Outputs Disabled		—	3.0	10	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High) (5)	V_{CC} = Max., V_{IN} = 3.4V, f_{OP} = 0		—	0.3	0.75	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL. COM'L.	— —	6 6	10 7	mA/ MHz
I_{CC}	Total Power Supply Current (6)	V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50 % Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL. COM'L.	— —	60 60	110 80	mA
		V_{CC} = Max., f_{OP} = 10MHz Outputs Open, $\overline{OE}$ = L 50 % Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL. COM'L.	— —	70 70	125 95	

NOTES: 2584 tbl 27

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQ}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP})$
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
   N_T = Number of dynamic inputs driven at TTL levels.
   f_{OP} = Operating frequency in Megahertz.

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.

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IDT49C460E AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, V_{CC} = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS(1)

	From Input		To Output: SC 0–7	To Output: DATA 0–31	To Output: ERROR	To Output: MULT ERROR	Unit
	DATA0–31(3)		11	14(2)	10	11	ns
	CB0–7 (CODE ID1,0 = 00, 11)		9	12	7	9	ns
	CB0–7 (CODE ID1,0 = 10)		9	10	—	—	ns
	LEOUT/GENERATE	↑	—	9	↓ 7	↓ 8	ns
		↓	13	—	↑ 7	↑ 8	ns
	CORRECT Not Internal Control Mode		—	11	—	—	ns
	DIAG MODE Not Internal Control Mode		11	18	8	14	ns
	CODE ID1,0		13(6)	17	12	15	ns
	LEIN From latched to Transparent		16	19	13	16	ns
	LEDIAG From latched to Transparent	↑	11(6)	17	11	13	ns
Internal Control Mode	LEDIAG (Internal Control Mode) From latched to Transparent	↑	11(6)	16	11	13	ns
	DATA0–31 (Internal Control Mode) Via Diagnostic Latch	↑	11	17(2)	9	11	ns

2584 tbl 70

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)	Set-up Time Min.	Hold Time Min.	Unit
DATA0–31(4)	↓	LEIN	3	3	ns
CB0–7 (4)	↓	LEIN	2	3	ns
DATA0–31(4, 6)	↓	LEOUT/GENERATE	5(15)	0	ns
CB0–7 (CODE ID 00, 11)(4, 6)	↓	LEOUT/GENERATE	11	0	ns
CB0–7 (CODE ID 10)(4, 6)	↓	LEOUT/GENERATE	6	0	ns
CORRECT(4, 6)	↑ ↓	LEOUT/GENERATE	6	0	ns
DIAG MODE(4 6)	↓	LEOUT/GENERATE	13	0	ns
CODE ID1,0(4, 6)	↓	LEOUT/GENERATE	8	0	ns
LEIN(4, 6)	↑ ↓	LEOUT/GENERATE	14	0	ns
DATA0–31(4, 6)		LEDIAG	3	3	ns

NOTE: (15) above applies to correction path.

2584 tbl 71

OUTPUT ENABLE/DISABLE TIMES(5)

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	7	0	6	ns
OESC	↓	↑	SC0–7	0	7	0	6	ns

2584 tbl 72

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive–going pulse)	5		ns

2584 tbl 73

NOTES:
1. CI = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with CI = 5pF and measured to 0.5V change of output level. Testing is performed at CI = 50pF and correlated to CI = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460D AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, V_{CC} = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$[3]		14	18[2]	12	15	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		11	16	10	12	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		12	12	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	9	↓ 7	↓ 8	ns
		↓	14	—	↑ 7	↑ 8	ns
	CORRECT Not Internal Control Mode		—	12	—	—	ns
	DIAG MODE Not Internal Control Mode		12	20	10	15	ns
	$CODE\ ID_{1,0}$		14[6]	18	13	16	ns
	LE_{IN} From latched to Transparent		17	21	14	17	ns
	LE_{DIAG} From latched to Transparent	↑	12[6]	18	12	14	ns
Internal Control Mode	LE_{DIAG} (Internal Control Mode) From latched to Transparent	↑	12[6]	17	12	14	ns
	$DATA_{0-31}$ (Internal Control Mode) Via Diagnostic Latch	↑	12	19[2]	10	12	ns

2584 tbl 28

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$[4]		↓	LE_{IN}	3	3	ns
CB_{0-7} [4]		↓	LE_{IN}	2	3	ns
$DATA_{0-31}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	5[15]	0	ns
CB_{0-7} (CODE ID 00, 11)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	11	0	ns
CB_{0-7} (CODE ID 10)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	6	0	ns
CORRECT[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	6	0	ns
DIAG MODE[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	13	0	ns
$CODE\ ID_{1,0}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	8	0	ns
LE_{IN}[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	14	0	ns
$DATA_{0-31}$[4, 6]			LE_{DIAG}	3	3	ns

NOTE: (15) above applies to correction path. 2584 tbl 29

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE\ Byte}_{0-3}$	↓	↑	$DATA_{0-31}$	0	8	0	10	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	8	0	10	ns

2584 tbl 30

MINIMUM PULSE WIDTHS[6]

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	5		ns

2584 tbl 31

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

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IDT49C460D AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS(1)

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: $\overline{\text{ERROR}}$	To Output: $\overline{\text{MULT ERROR}}$	Unit
	DATA0–3(3)		17	22(2)	16	18	ns
	CB0–7 (CODE ID1,0 = 00, 11)		13	17	12	14	ns
	CB0–7 (CODE ID1,0 = 10)		13	14	—	—	ns
	LEOUT/$\overline{\text{GENERATE}}$	↑	—	10	↓ 8	↓ 8	ns
		↓	15	—	↑ 8	↑ 9	ns
	CORRECT Not Internal Control Mode		—	13	—	—	ns
	DIAG MODE Not Internal Control Mode		14	22	12	17	ns
	CODE ID1,0		16(6)	20	15	18	ns
	LEIN From latched to Transparent		18	24	16	19	ns
	LEDIAG From latched to Transparent	↑	14(6)	20	13	16	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	14(6)	19	14	16	ns
	DATA0–31 Via Diagnostic Latch	↑	14	22 (2)	11	14	ns

2584 tbl 32

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–31(4)		↓	LEIN	3	3	ns
CB0–7(4)		↓	LEIN	2	3	ns
DATA0–31(4, 6)		↓	LEOUT/$\overline{\text{GENERATE}}$	6(15)	0	ns
CB0–7 (CODE ID 00, 11)(4, 6)		↓	LEOUT/$\overline{\text{GENERATE}}$	12	0	ns
CB0–7 (CODE ID 10)(4, 6)		↓	LEOUT/$\overline{\text{GENERATE}}$	8	0	ns
CORRECT(4, 6)	↑	↓	LEOUT/$\overline{\text{GENERATE}}$	7	0	ns
DIAG MODE(4, 6)		↓	LEOUT/$\overline{\text{GENERATE}}$	14	0	ns
CODE ID1,0(4, 6)		↓	LEOUT/$\overline{\text{GENERATE}}$	9	0	ns
LEIN(4, 6)	↑	↓	LEOUT/$\overline{\text{GENERATE}}$	16	0	ns
DATA0–31(4, 6)			LEDIAG	3	3	ns

NOTE: (15) above applies to correction path.

2584 tbl 33

OUTPUT ENABLE/DISABLE TIMES(5)

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{\text{OE}}$ Byte0–3	↓	↑	DATA0–31	0	10	0	12	ns
$\overline{\text{OE}}$SC	↓	↑	SC0–7	0	10	0	12	ns

2584 tbl 34

MINIMUM PULSE WIDTHS(6)

	Min.		
LEIN, LEOUT/$\overline{\text{GENERATE}}$, LEDIAG ↑↓ (Positive–going pulse)	5		ns

2584 tbl 35

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5F.
6. Not production tested, guaranteed by characterization.

IDT49C460C AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, V_{CC} = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS(1)

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$		To Output: $\overline{MULT\ ERROR}$		Unit
	$DATA_{0-31}$(3)		19	24(2)	16		20		ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		14	21	12		16		ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		14	16	—		—		ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	12	↓	9	↓	11	ns
		↓	18	—	↑	9	↑	11	ns
	CORRECT Not Internal Control Mode		—	16	—		—		ns
	DIAG MODE Not Internal Control Mode		16	26	11		20		ns
	$CODE\ ID_{1,0}$		18(6)	23	17		21		ns
	LE_{IN} From latched to Transparent		22	28(2)	19		22		ns
	LE_{DIAG} From latched to Transparent	↑	15(6)	24	15		19		ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	16(6)	22	15		18		ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch	↑	15	25(2)	13		16		ns

2584 tbl 36

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$(4)		↓	LE_{IN}	3	4	ns
CB_{0-7}(4)		↓	LE_{IN}	2	4	ns
$DATA_{0-31}$(4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	6(16)	0	ns
CB_{0-7} (CODE ID 00, 11)(4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	14	0	ns
CB_{0-7} (CODE ID 10)(4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	8	0	ns
CORRECT(4, 6)	↑	↓	$LE_{OUT}/\overline{GENERATE}$	8	0	ns
DIAG MODE(4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
$CODE\ ID_{1,0}$(4, 6)		↓	$LE_{OUT}/\overline{GENERATE}$	10	0	ns
LE_{IN}(4, 6)	↑	↓	$LE_{OUT}/\overline{GENERATE}$	19	0	ns
$DATA_{0-31}$(4, 6)			LE_{DIAG}	3	3	ns

NOTE: (16) above applies to correction path.

2584 tbl 37

OUTPUT ENABLE/DISABLE TIMES(5)

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}\ Byte_{0-3}$	↓	↑	$DATA_{0-31}$	0	10	0	12	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	10	0	12	ns

2584 tbl 38

MINIMUM PULSE WIDTHS(6)

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	6		ns

2584 tbl 39

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

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IDT49C460C AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, V_{CC} = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$[3]		22	29[2]	21	24	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		17	23	16	18	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		17	18	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	13	↓ 10	↓ 12	ns
		↓	20	—	↑ 10	↑ 12	ns
	CORRECT Not Internal Control Mode		—	17	—	—	ns
	DIAG MODE Not Internal Control Mode		18	29	12	23	ns
	CODE $ID_{1,0}$		21 [6]	26	20	24	ns
	LE_{IN} From latched to Transparent		24	32	21	25	ns
	LE_{DIAG} From latched to Transparent	↑	18 [6]	27	17	21	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	19 [6]	25	18	21	ns
	$DATA_{0-31}$ Via Diagnostic Latch	↑	18	29[2]	14	18	ns

2584 tbl 40

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$[4]		↓	LE_{IN}	3	4	ns
CB_{0-7}[4]		↓	LE_{IN}	2	4	ns
$DATA_{0-31}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	7[19]	3	ns
CB_{0-7} (CODE ID 00, 11)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	16	0	ns
CB_{0-7} (CODE ID 10)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	10	0	ns
CORRECT[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	9	0	ns
DIAG MODE[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	19	0	ns
CODE $ID_{1,0}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	12	0	ns
LE_{IN}[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	21	0	ns
$DATA_{0-31}$[4, 6]			LE_{DIAG}	3	3	ns

Note: (19) above applies to correction path.

2584 tbl 41

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}$ $Byte_{0-3}$	↓	↑	$DATA_{0-31}$	0	12	0	14	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	12	0	14	ns

2584 tbl 42

MINIMUM PULSE WIDTHS[6]

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	6		ns

2584 tbl 43

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5F.
6. Not production tested, guaranteed by characterization.

IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, Vcc = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR		To Output: MULT ERROR		Unit
	DATA0–31[3]		25	30[2]	25		27		ns
	CB0–7 (CODE ID1,0 = 00, 11)		14	30	17		20		ns
	CB0–7 (CODE ID1,0 = 10)		16	18	—		—		ns
	LEOUT/GENERATE	↑	—	12	↓	23	↓	23	ns
		↓	21	—	↑	23	↑	23	ns
	CORRECT Not Internal Control Mode		—	23	—		—		ns
	DIAG MODE Not Internal Control Mode		17	26	20		24		ns
	CODE ID1,0		18[6]	26	21		26		ns
	LEIN From latched to Transparent		27	38[2]	30		3		ns
	LEDIAG From latched to Transparent	↑	15[6]	29	19		22		ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	16[6]	32	19		24		ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	16	32[2]	20		25		ns

2584 tbl 44

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–31[4]		↓	LEIN	4	4	ns
CB0–7[4]		↓	LEIN	4	4	ns
DATA0–31[4, 6]		↓	LEOUT/GENERATE	19	0	ns
CB0–7 (CODE ID 00, 11)[4, 6]		↓	LEOUT/GENERATE	15	0	ns
CB0–7 (CODE ID 10)[4, 6]		↓	LEOUT/GENERATE	15	0	ns
CORRECT[4, 6]	↑	↓	LEOUT/GENERATE	11	0	ns
DIAG MODE[4, 6]		↓	LEOUT/GENERATE	17	0	ns
CODE ID1,0[4, 6]		↓	LEOUT/GENERATE	17	0	ns
LEIN[4, 6]	↑	↓	LEOUT/GENERATE	20	0	ns
DATA0–31[4, 6]			LEDIAG	4	3	ns

2584 tbl 45

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	12	0	14	ns
OESC	↓	↑	SC0–7	0	12	0	14	ns

2584 tbl 46

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive–going pulse)	9		ns

2584 tbl 47

NOTES:
1. CI = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with CI = 5pF and measured to 0.5V change of output level. Testing is performed at CI = 50pF and correlated to CI = 5pF.
6. Not production tested, guaranteed by characterization.

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IDT49C460B AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, V_{CC} = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$[3]		28	33[2]	28	30	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		17	33	20	23	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		19	23	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	15	↓ 26	↓ 26	ns
		↓	24	—	↑ 26	↑ 26	ns
	CORRECT Not Internal Control Mode		—	26	—	—	ns
	DIAG MODE Not Internal Control Mode		20	29	23	27	ns
	CODE $ID_{1,0}$		21	29	24	29	ns
	LE_{IN} From latched to Transparent		30	41	33	36	ns
	LE_{DIAG} From latched to Transparent	↑	18	32	22	25	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	19	35	22	27	ns
	$DATA_{0-31}$ Via Diagnostic Latch	↑	19	35[2]	23	28	ns

2584 tbl 48

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$[4]		↓	LE_{IN}	4	4	ns
CB_{0-7}[4]		↓	LE_{IN}	4	4	ns
$DATA_{0-31}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
CB_{0-7} (CODE ID 00, 11)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CB_{0-7} (CODE ID 10)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	18	0	ns
CORRECT[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	14	0	ns
DIAG MODE[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
CODE $ID_{1,0}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
LE_{IN}[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
$DATA_{0-31}$[4, 6]			LE_{DIAG}	4	3	ns

2584 tbl 49

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}$ $Byte_{0-3}$	↓	↑	$DATA_{0-31}$	0	12	0	14	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	12	0	14	ns

2584 tbl 50

MINIMUM PULSE WIDTHS

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	12		ns

2584 tbl 51

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to 70°C, V_{CC} = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$[3]		27	36[2]	30	33	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		16	34	19	23	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		16	20	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	12	↓ 25	↓ 25	ns
		↓	21	—	↑ 25	↑ 25	ns
	CORRECT Not Internal Control Mode		—	23	—	—	ns
	DIAG MODE Not Internal Control Mode		17	26	20	24	ns
	CODE $ID_{1,0}$		18	26	21	26	ns
	LE_{IN} From latched to Transparent		27	38	30	33	ns
	LE_{DIAG} From latched to Transparent	↑	15	29	19	22	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	16	32	29	24	ns
Internal Control Mode	$DATA_{0-31}$ Via Diagnostic Latch	↑	16	32[2]	20	25	ns

2584 tbl 52

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$[4]		↓	LE_{IN}	5	4	ns
CB_{0-7}[4]		↓	LE_{IN}	5	4	ns
$DATA_{0-31}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	23	0	ns
CB_{0-7} (CODE ID 00, 11)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CB_{0-7} (CODE ID 10)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	15	0	ns
CORRECT[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	11	0	ns
DIAG MODE[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
$CODE\ ID_{1,0}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	17	0	ns
LE_{IN}[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	25	0	ns
$DATA_{0-31}$[4, 6]			LE_{DIAG}	5	3	ns

2584 tbl 53

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE\ Byte_{0-3}}$	↓	↑	$DATA_{0-31}$	0	12	0	14	ns
$\overline{OE_{SC}}$	↓	↑	SC_{0-7}	0	12	0	14	ns

2584 tbl 54

MINIMUM PULSE WIDTHS

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	9		ns

2584 tbl 55

NOTES:
1. Cl = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

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IDT49C460A AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, Vcc = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS(1)

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: ERROR	To Output: MULT ERROR	Unit
	DATA0–31(3)		30	39(2)	33	36	ns
	CB0–7 (CODE ID1,0 = 00, 11)		19	37	22	26	ns
	CB0–7 (CODE ID1,0 = 10)		19	23	—	—	ns
	LEOUT/GENERATE	↑	—	15	↓ 28	↓ 28	ns
		↓	24	—	↑ 28	↑ 28	ns
	CORRECT Not Internal Control Mode		—	26	—	—	ns
	DIAG MODE Not Internal Control Mode		20	29	23	27	ns
	CODE ID1,0		21	29	24	29	ns
	LEIN From latched to Transparent		30	41	33	36	ns
	LEDIAG From latched to Transparent	↑	18	32	22	25	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	19	35	22	27	ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	19	35(2)	23	28	ns

2584 tbl 56

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–3(4)		↓	LEIN	5	4	ns
CB0–7(4)		↓	LEIN	5	4	ns
DATA0–31(4, 6)		↓	LEOUT/GENERATE	27	0	ns
CB0–7 (CODE ID 00, 11)(4, 6)		↓	LEOUT/GENERATE	18	0	ns
CB0–7 (CODE ID 10)(4, 6)		↓	LEOUT/GENERATE	18	0	ns
CORRECT(4, 6)	↑	↓	LEOUT/GENERATE	14	0	ns
DIAG MODE(4, 6)		↓	LEOUT/GENERATE	20	0	ns
CODE ID1,0(4, 6)		↓	LEOUT/GENERATE	20	0	ns
LEIN(4, 6)	↑	↓	LEOUT/GENERATE	28	0	ns
DATA0–31(4, 6)			LEDIAG	5	3	ns

2584 tbl 57

OUTPUT ENABLE/DISABLE TIMES(5)

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
OE Byte0–3	↓	↑	DATA0–31	0	12	0	14	ns
OESC	↓	↑	SC0–7	0	12	0	14	ns

2584 tbl 58

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/GENERATE, LEDIAG ↑↓ (Positive–going pulse)	12		ns

2584 tbl 59

NOTES:
1. CI = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with CI = 5pF and measured to 0.5V change of output level. Testing is performed at CI = 50pF and correlated to CI = 5pF.
6. Not production tested, guaranteed by characterization.

IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Commercial Range Performance) Temperature range: 0°C to +70°C, V_{CC} = 5.0V ± 5%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC0–7	To Output: DATA0–31	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	DATA0–31[3]		37	49[2]	40	45	ns
	CB0–7 (CODE ID1,0 = 00, 11)		22	46	26	31	ns
	CB0–7 (CODE ID1,0 = 10)		22	30	—	—	ns
	LEOUT/$\overline{GENERATE}$	↑	—	17	↓ 30	↓ 30	ns
		↓	29	—	↑ 30	↑ 30	ns
	CORRECT Not Internal Control Mode		—	31	—	—	ns
	DIAG MODE Not Internal Control Mode		23	35	27	33	ns
	CODE ID1,0		25	35	29	35	ns
	LEIN From latched to Transparent		37	51	41	45	ns
	LEDIAG From latched to Transparent	↑	21	38	26	30	ns
Internal Control Mode	LEDIAG From latched to Transparent	↑	22	42	26	33	ns
Internal Control Mode	DATA0–31 Via Diagnostic Latch	↑	22	42[2]	27	34	ns

2584 tbl 60

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
DATA0–31[4]		↓	LEIN	6	4	ns
CB0–7[4]		↓	LEIN	5	4	ns
DATA0–31[4, 6]		↓	LEOUT/$\overline{GENERATE}$	30	0	ns
CB0–7 (CODE ID 00, 11)[4, 6]		↓	LEOUT/$\overline{GENERATE}$	20	0	ns
CB0–7 (CODE ID 10)[4, 6]		↓	LEOUT/$\overline{GENERATE}$	20	0	ns
CORRECT[4, 6]	↑	↓	LEOUT/$\overline{GENERATE}$	16	0	ns
DIAG MODE[4, 6]		↓	LEOUT/$\overline{GENERATE}$	23	0	ns
CODE ID1,0[4, 6]		↓	LEOUT/$\overline{GENERATE}$	23	0	ns
LEIN [4, 6]	↑	↓	LEOUT/$\overline{GENERATE}$	31	0	ns
DATA0–31 [4, 6]			LEDIAG	6	3	ns

2584 tbl 61

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}$ Byte0–3	↓	↑	DATA0–31	0	15	0	17	ns
$\overline{OE}$SC	↓	↑	SC0–7	0	15	0	17	ns

2584 tbl 62

MINIMUM PULSE WIDTHS

	Min.		
LEIN, LEOUT/$\overline{GENERATE}$, LEDIAG ↑↓ (Positive–going pulse)	12		ns

2584 tbl 63

NOTES:
1. CI = 50pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with CI = 5pF and measured to 0.5V change of output level. Testing is performed at CI = 50pF and correlated to CI = 5pF.
6. Not production tested, guaranteed by characterization.

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IDT49C460 AC ELECTRICAL CHARACTERISTICS

(Guaranteed Military Range Performance) Temperature range: –55°C to +125°C, V_{CC} = 5.0V ± 10%
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

PROPAGATION DELAYS[1]

	From Input		To Output: SC_{0-7}	To Output: $DATA_{0-31}$	To Output: $\overline{ERROR}$	To Output: $\overline{MULT\ ERROR}$	Unit
	$DATA_{0-31}$[3]		40	52[2]	44	48	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 00, 11)		25	49	29	34	ns
	CB_{0-7} (CODE $ID_{1,0}$ = 10)		25	33	—	—	ns
	$LE_{OUT}/\overline{GENERATE}$	↑	—	20	↓ 33	↓ 33	ns
		↓	32	—	↑ 33	↑ 33	ns
	CORRECT Not Internal Control Mode		—	34	—	—	ns
	DIAG MODE Not Internal Control Mode		26	38	30	36	ns
	$CODE\ ID_{1,0}$		28	38	32	38	ns
	LE_{IN} From latched to Transparent		40	54	44	48	ns
	LE_{DIAG} From latched to Transparent	↑	24	42	29	33	ns
Internal Control Mode	LE_{DIAG} From latched to Transparent	↑	25	47[2]	29	36	ns
	$DATA_{0-31}$ Via Diagnostic Latch	↑	25	47	30	37	ns

2584 tbl 64

SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

From Input		To Input (Latching Data)		Set-up Time Min.	Hold Time Min.	Unit
$DATA_{0-31}$[4]		↓	LE_{IN}	6	4	ns
CB_{0-7}[4]		↓	LE_{IN}	5	4	ns
$DATA_{0-31}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	36	0	ns
CB_{0-7} (CODE ID 00, 11)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	24	0	ns
CB_{0-7} (CODE ID 10)[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	24	0	ns
CORRECT[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	20	0	ns
DIAG MODE[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	28	0	ns
$CODE\ ID_{1,0}$[4, 6]		↓	$LE_{OUT}/\overline{GENERATE}$	28	0	ns
LE_{IN}[4, 6]	↑	↓	$LE_{OUT}/\overline{GENERATE}$	37	0	ns
$DATA_{0-31}$[4, 6]			LE_{DIAG}	6	3	ns

2584 tbl 65

OUTPUT ENABLE/DISABLE TIMES[5]

From Input	Enable	Disable	To Output	Enable Min.	Enable Max.	Disable Min.	Disable Max.	Unit
$\overline{OE}\ Byte_{0-3}$	↓	↑	$DATA_{0-31}$	0	15	0	17	ns
$\overline{OE}_{SC}$	↓	↑	SC_{0-7}	0	15	0	17	ns

2584 tbl 66

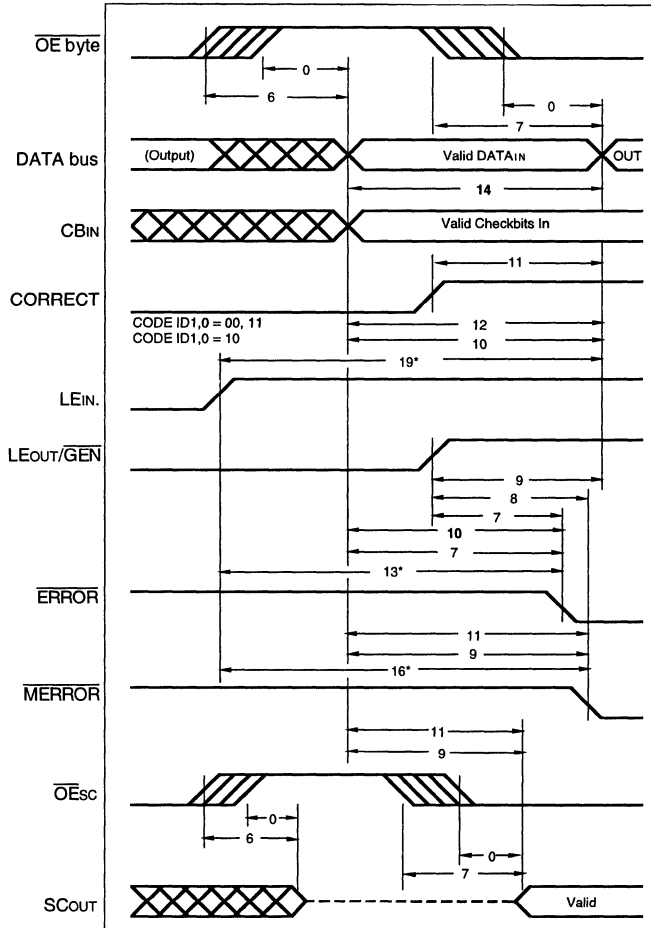
MINIMUM PULSE WIDTHS

	Min.		
LE_{IN}, $LE_{OUT}/\overline{GENERATE}$, LE_{DIAG} ↑↓ (Positive–going pulse)	15		ns

2584 tbl 67

NOTES:
1. Cl = 5pF.
2. These parameters are combinational propagation delay calculations, and are not tested in production.
3. Data In or Correct Data Out measurement requires timing as shown in the Switching Waveforms.
4. Set-up and Hold times relative to Latch Enables (Latching Data).
5. Output tests specified with Cl = 5pF and measured to 0.5V change of output level. Testing is performed at Cl = 50pF and correlated to Cl = 5pF.
6. Not production tested, guaranteed by characterization.

DETECT OR CORRECTION MODE (FROM GENERATE MODE)



Propagation Delay From	To	Min./Max.
$\overline{OE}$ byte	= High to DATAOUT Disabled	Min.
$\overline{OE}$ byte	= High to DATAOUT Disabled	Max.
$\overline{OE}$ byte	= Low to DATAOUT Enabled	Min.
$\overline{OE}$ byte	= Low to DATAOUT Enabled	Max.
(Corrected DATA if Correct Mode) (DATAIN if Detect Mode)		
DATAIN	**to DATAOUT**	**Max.**
CORRECT	= High to DATAOUT	Max.
CBIN	to DATAOUT	Max.
CBIN	to DATAOUT	Max.
*LEIN	= High to DATAOUT	Max.
LEOUT/$\overline{GEN}$	= High to DATAOUT	Max.
LEOUT/$\overline{GEN}$	= High to $\overline{MERROR}$ = Low	Max.
LEOUT/$\overline{GEN}$	= High to $\overline{ERROR}$ = Low	Max.
DATAIN	**to $\overline{ERROR}$ = Low**	**Max.**
CBIN	to $\overline{ERROR}$ = Low	Max.
*LEIN	= High to $\overline{ERROR}$ = Low*	Max.
(Low = Error)		
DATAIN	to $\overline{MERROR}$ = Low	Max.
CBIN	to $\overline{MERROR}$ = Low	Max.
*LEIN	= High to $\overline{MERROR}$ = Low*	Max.
(Low = Error)		
DATAIN	to SCOUT	Max.
CBIN	to SCOUT	Max.
$\overline{OE}$SC	= High to SCOUT Disabled	Min.
$\overline{OE}$SC	= High to SCOUT Disabled	Max.
$\overline{OE}$SC	= Low to SCOUT Enabled	Min.
$\overline{OE}$SC	= Low to SCOUT Enabled	Max.
(Syndrome Bits Come Out)		

NOTES:
1. **BOLD** indicates critical parameters.
2. This is "E" version timing spec. Check appropriate table for other speed versions.
* Assumes "CBIN" and/or "DATAIN" are valid at least 4ns before "LEIN" goes high.

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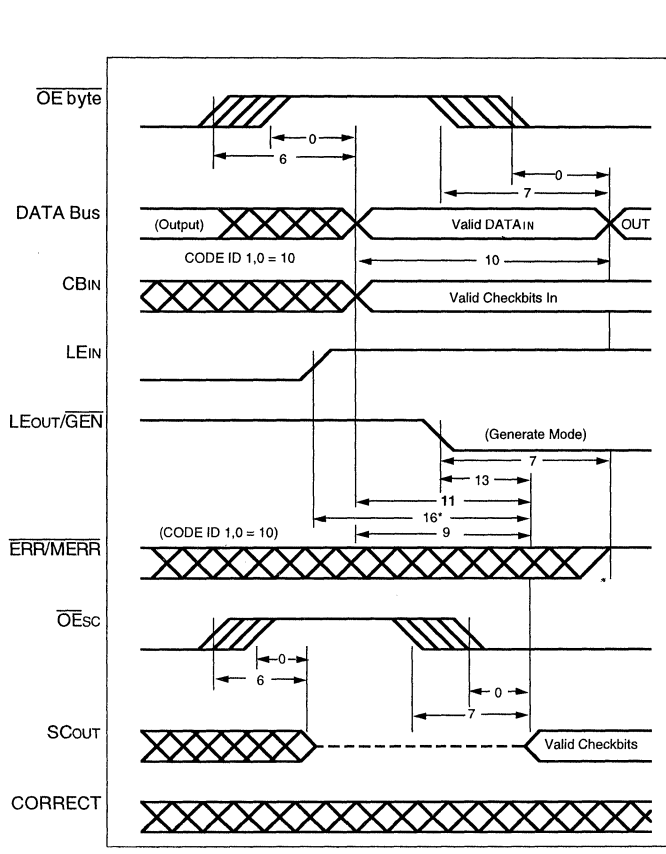
GENERATE MODE (FROM DETECT OR CORRECTION MODE)



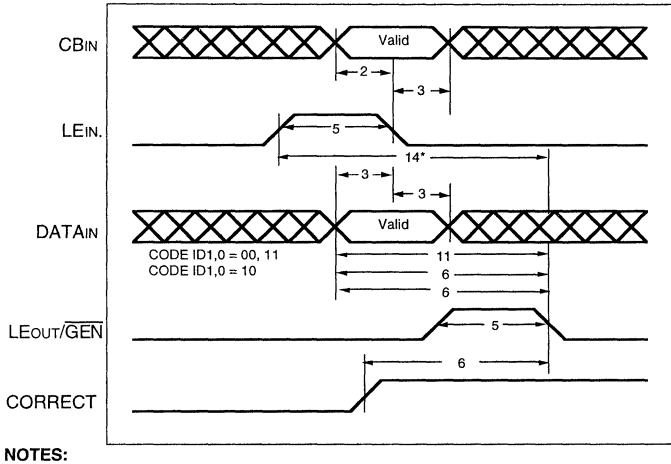
Propagation Delay From	To	Min./Max.
OE byte = High to DATAOUT Disabled		Min.
OE byte = High to DATAOUT Disabled		Max.
OE byte = Low to DATAOUT Enabled		Min.
OE byte = Low to DATAOUT Enabled		Max.
CBIN to DATAOUT		Max.
LEOUT/GENERATE = Low to ERROR = High		Max.
LEOUT/GENERATE = Low to SCOUT		Max.
DATAIN to SCOUT		**Max.**
LEIN = High to SCOUT		Max.
CBIN to SCOUT		Max.
(Forced High)		
OESC = High to SCOUT Disabled		Min.
OESC = High to SCOUT Disabled		Max.
OESC = Low to SCOUT Enabled		Min.
OESC = Low to SCOUT Enabled		Max.
(Check Bits Exit)		
(Don't Care)		

2584 drw 09

NOTES:
1. **BOLD** indicates critical parameters.
2. Valiid "DATA" and valid CBIN" are shown to occur simultaneously, since both buses are latched and opened by the "LEIN" input.
3. This is "E" version timing spec. Check appropriate table for other speed versions.

* Assumes DATA bus becomes input 4ns before LEIN goes high.

SET-UP AND HOLD TIMES AND MINIMUM PULSE WIDTHS



Set-up/Hold Time Of With Respect To	Min./Max.
CBIN Set-up to LEIN = Low	Min.
CBIN Hold to LEIN = Low	Min.
LEIN width	Min.
LEIN = High to LEOUT/$\overline{GEN}$ = Low	Min.
DATA Set-up to LEIN = Low	Min.
DATA Hold to LEIN = Low	Min.
CBIN Set-up to LEOUT/$\overline{GEN}$ = Low	Min.
CBIN Set-up to LEOUT/$\overline{GEN}$ = Low	Min.
DATA Set-up to LEOUT/$\overline{GEN}$ = Low	Min.
LEOUT/$\overline{GENERATE}$ Width	Min.
CORRECT Set-up to LEOUT/$\overline{GEN}$ = Low	Min.

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NOTES:
1. **BOLD** indicates critical parameters.
2. This is "E" version timing spec. Check appropriate table for other speed versions.
* Enable to enable timing requirement to ensure that the last DATA word applied to "DATAIN" is made available as DATAOUT"; assumes that "DATAIN" is valid at least 4ns before "LEIN" goes high.

INPUT/OUTPUT INTERFACE CIRCUIT

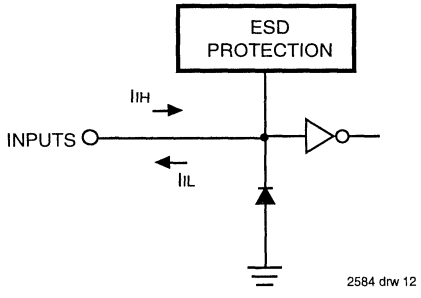

Figure 5. Input Structure (All Inputs)

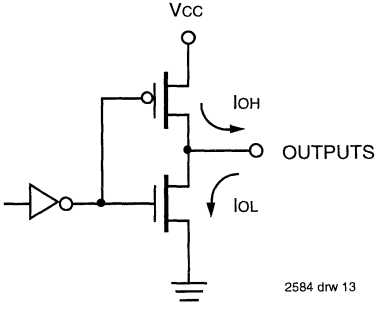

Figure 6. Out put Structure

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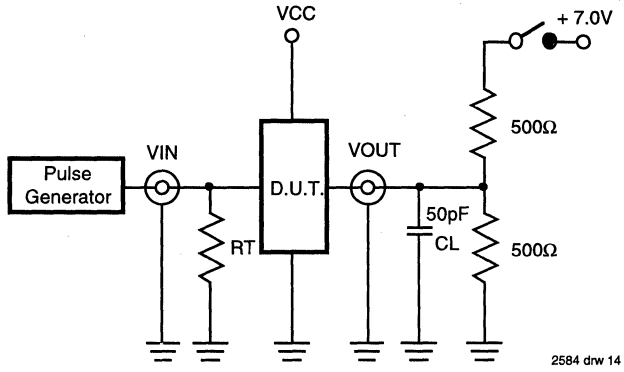
TEST LOAD CIRCUIT



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_L = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 7.

AC TEST CONDITIONS

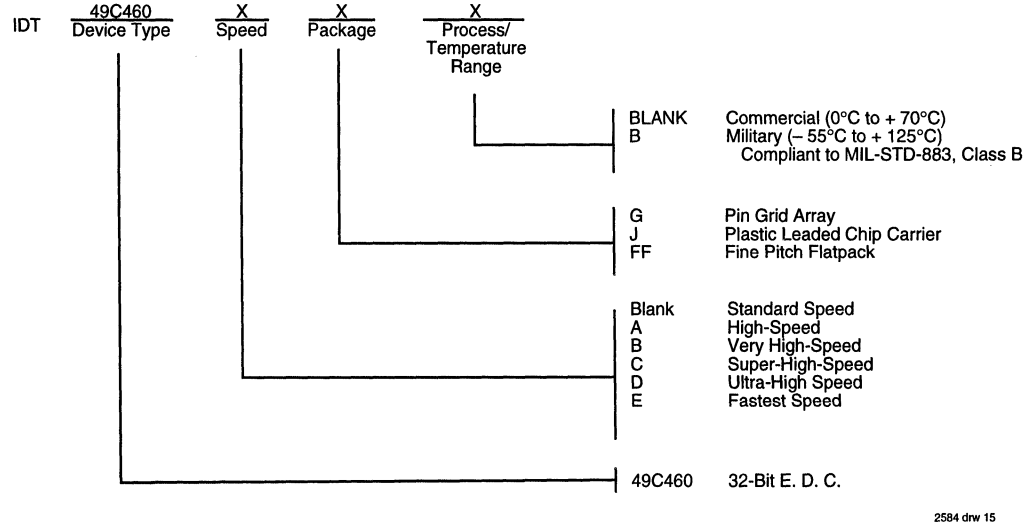
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 7

2584 tbl 69

Test	Switch
Disable Low Enable Low	Closed
All other Tests	Open

2584 tbl 68

ORDERING INFORMATION



Integrated Device Technology, Inc.

32-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

IDT49C465
IDT49C465A

FEATURES

- 32-bit wide Flow-thruEDC™ unit, cascadable to 64 bits
- Single-chip 64-bit Generate Mode
- Separate system and memory buses
- On-chip pipeline latch with external control
- Supports bidirectional and common I/O memories
- Corrects all single-bit errors
- Detects all double-bit errors, some multiple-bit errors
- Error Detection Time — 12ns
- Error Correction Time — 14ns
- On chip diagnostic registers.
- Parity generation and checking on system data bus
- Low power CMOS — 100mA typical at 20MHz
- 144-pin PGA and PQFP packages
- Military product compliant to MIL-STD 883, Class B

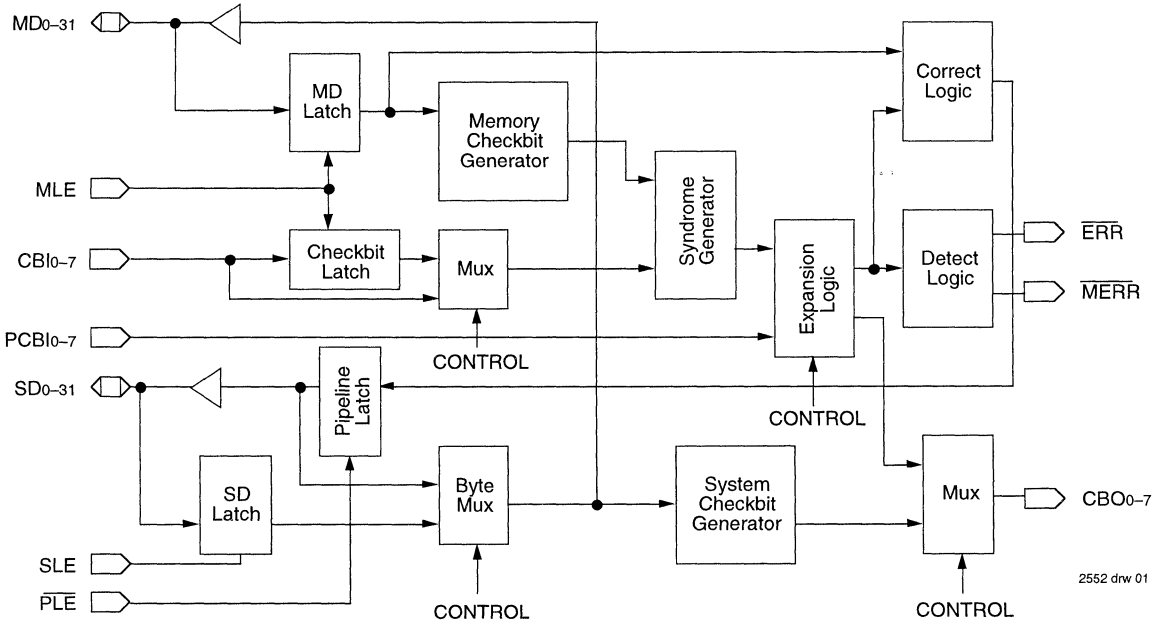
DESCRIPTION

The IDT49C465/A is a 32-bit, two-data bus, Flow-thruEDC unit. The chip provides single-error correction and two and three bit error detection of both hard and soft memory errors. It can be expanded to 64-bit widths by cascading 2 units, without the need for additional external logic. The Flow-thruEDC has been optimized for speed and simplicity of control.

The EDC unit has been designed to be used in either of two configurations in an error correcting memory system. The bidirectional configuration is most appropriate for systems using bidirectional memory buses. A second system configuration utilizes external octal buffers, and is well suited for systems using memory with separate I/O buses.

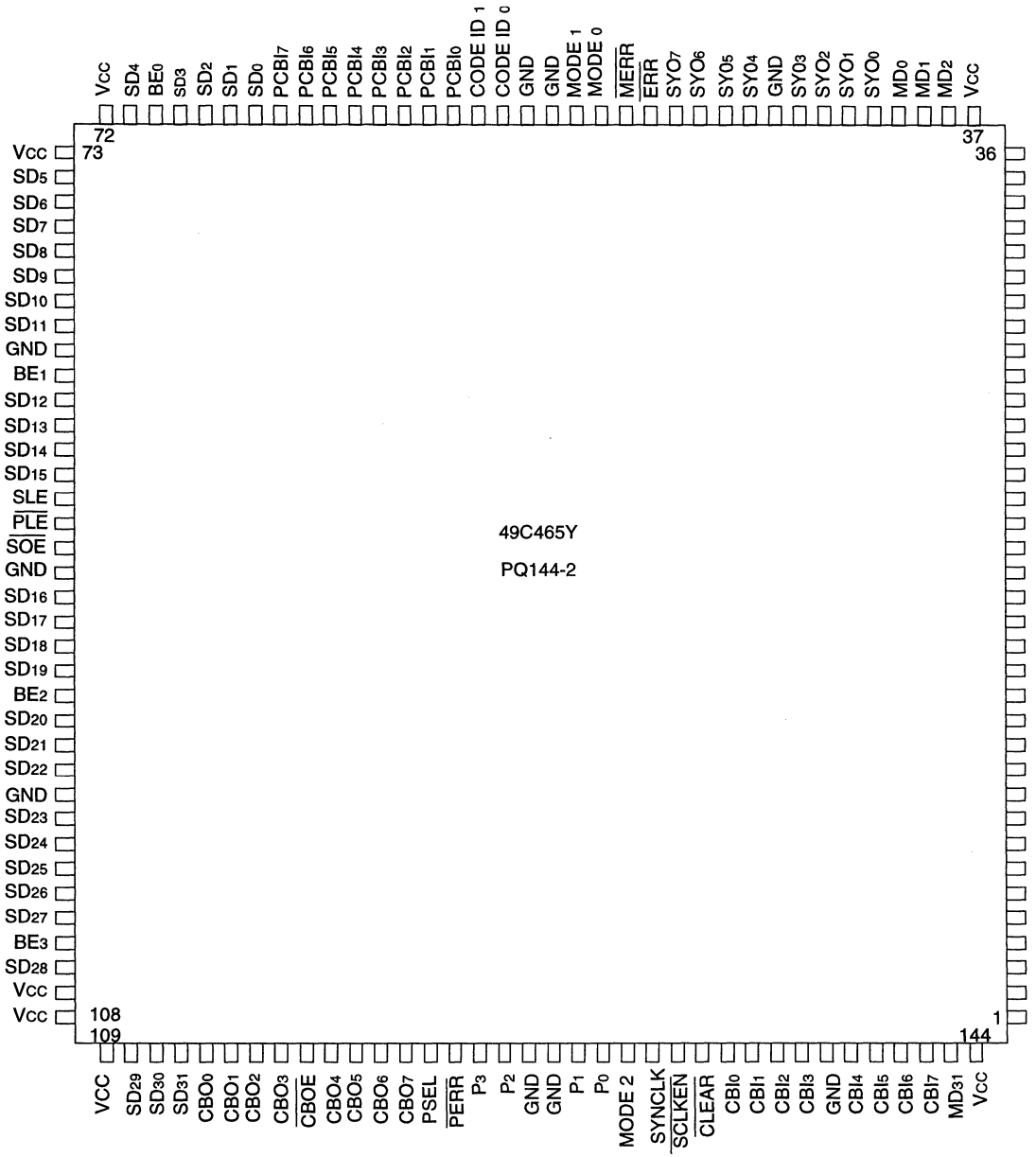
The IDT49C465/A supports partial word writes, pipelining and error diagnostics. It also provides parity protection for data on the system side.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark and Flow-thruEDC is a trademark of Integrated Device Technology Inc.

PIN CONFIGURATION



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PQFP
TOP VIEW

PIN CONFIGURATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
15	V_{CC}	SD_2	$PCBI_6$	$PCBI_5$	$PCBI_3$	$CODE\ ID_1$	$CODE\ ID_0$	$MODE_1$	$\overline{MERR}$	$\overline{ERR}$	SYO_5	SYO_3	SYO_1	MD_1	V_{CC}
14	SD_6	SD_4	SD_1	$PCBI_7$	$PCBI_4$	$PCBI_1$	$PCBI_0$	$MODE_0$	SYO_6	SYO_4	SYO_2	MD_0	MD_2	V_{CC}	MD_5
13	SD_9	SD_5	BE_0	SD_3	SD_0	$PCBI_2$	GND	GND	SYO_7	GND	SYO_0	V_{CC}	MD_3	MD_6	MD_9
12	SD_{11}	SD_7	V_{CC}										MD_4	MD_8	GND
11	SD_{12}	SD_{10}	SD_8										MD_7	MD_{10}	MD_{11}
10	SD_{15}	BE_1	GND										MD_{12}	MD_{13}	MD_{15}
9	SLE	SD_{13}	SD_{14}										$\overline{MOE}$	MD_{14}	MLE
8	$\overline{SOE}$	$\overline{PLE}$	GND			G144-2							GND	MD_{17}	MD_{16}
7	SD_{17}	SD_{19}	SD_{16}										MD_{20}	MD_{21}	MD_{18}
6	SD_{18}	BE_2	SD_{20}										GND	MD_{23}	MD_{19}
5	SD_{21}	SD_{22}	SD_{25}										MD_{27}	MD_{25}	MD_{22}
4	GND	SD_{24}	BE_3	NC*									V_{CC}	MD_{28}	MD_{24}
3	SD_{23}	SD_{26}	SD_{28}	V_{CC}	$CB0_0$	$\overline{CBOE}$	$CB0_7$	GND	GND	$\overline{SCLK}$ $\overline{EN}$	GND	$CB1_6$	$CB1_7$	MD_{30}	MD_{26}
2	SD_{27}	V_{CC}	SD_{29}	SD_{31}	$CB0_2$	$CB0_4$	$CB0_6$	P_3	$MODE_2$	SYN-CLK	$CB1_0$	$CB1_3$	$CB1_4$	MD_{31}	MD_{29}
1	V_{CC}	SD_{30}	$CB0_1$	$CB0_3$	$CB0_5$	PSEL	$\overline{PERR}$	P_2	P_1	P_0	$\overline{CLEAR}$	$CB1_1$	$CB1_2$	$CB1_5$	V_{CC}

*Tied to Vcc internally

PGA (CAVITY UP)
TOP VIEW

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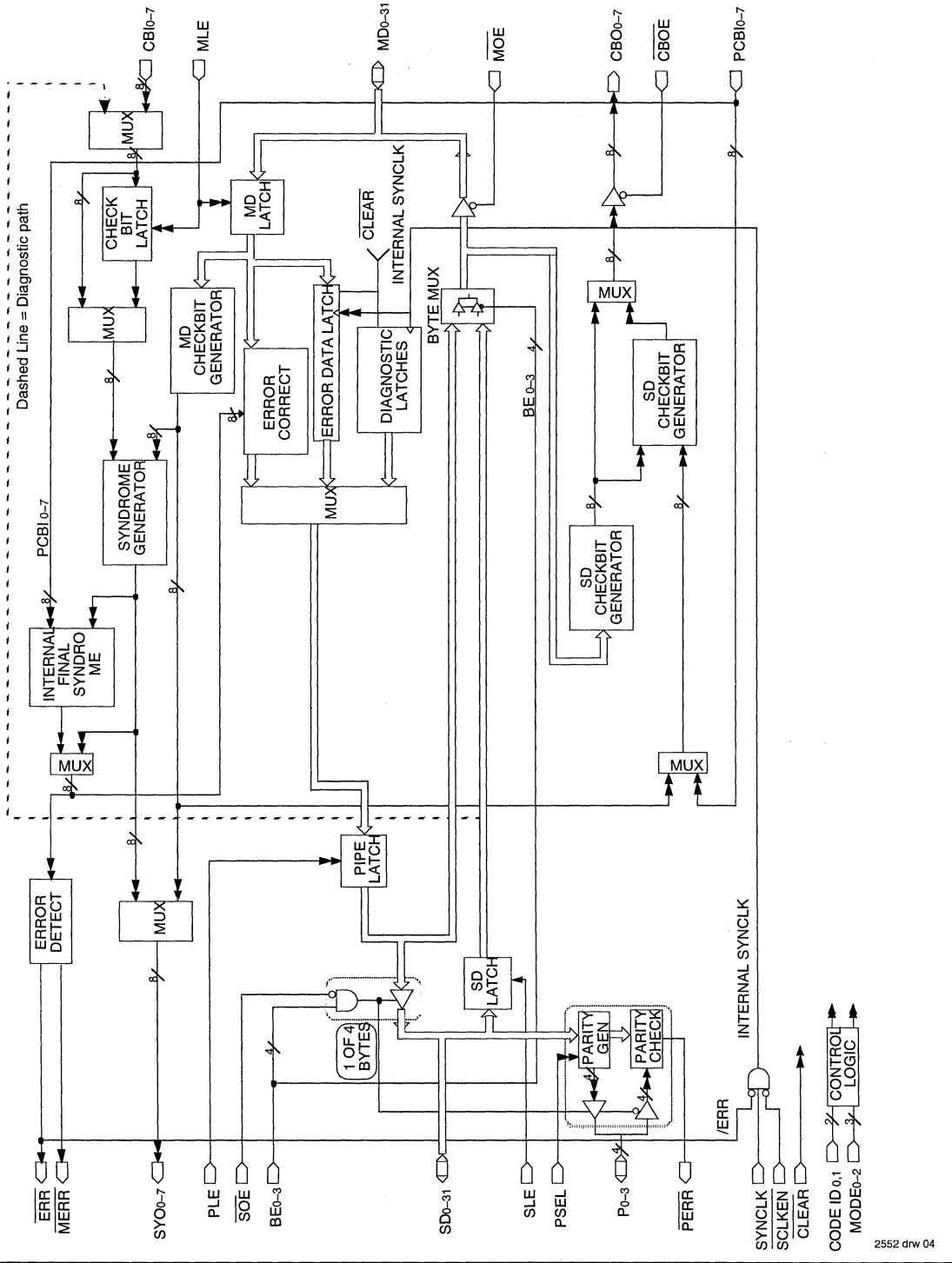
DETAILED FUNCTIONAL BLOCK DIAGRAM



SYSTEM CONFIGURATIONS

The IDT49C465 EDC unit can be used in various configurations in an EDC system. The basic configurations are shown below.

Figure 1 illustrates a bidirectional configuration, which is most appropriate for systems using bidirectional memory buses. It is the simplest configuration to understand and use. During a correction cycle, the corrected data word can be simultaneously output on both the system bus and memory bus. Logically, no other parts are required for the correction function. During partial-word-write operations, the new bytes are internally combined with the corrected old bytes for checkbit generation and writing to memory.

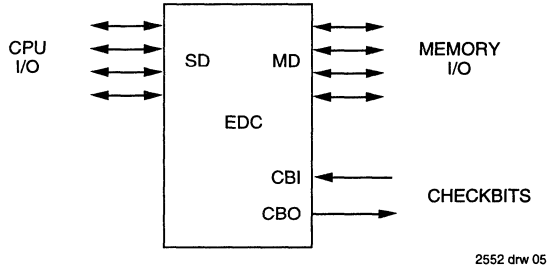


Figure 1. Common I/O Configuration

Figure 2 illustrates a separate I/O configuration. This is appropriate for systems using separate I/O memory buses. This configuration allows separate input and output memory buses to be used. Corrected data is output on the SD outputs for the system and for re-write to memory. Partial word-write bytes are combined externally for writing and checkbit generation.

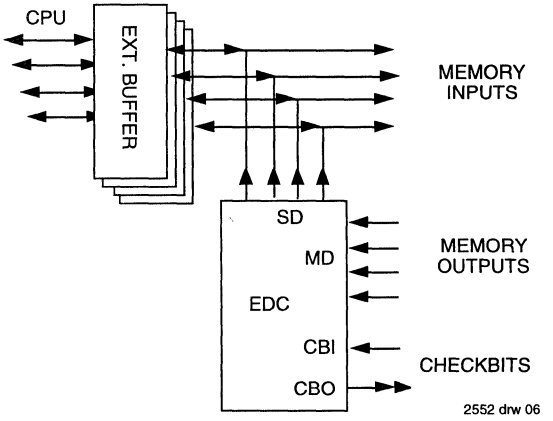


Figure 2. Separate I/O Configuration

Figure 3 illustrates a third configuration which utilizes external buffers and is also well suited for systems using memory with separate I/O buses. Since data from memory does not need to pass through the part on every cycle, the EDC system may operate in "bus-watch" mode. As in the separate I/O configuration, corrected data is output on the SD outputs.

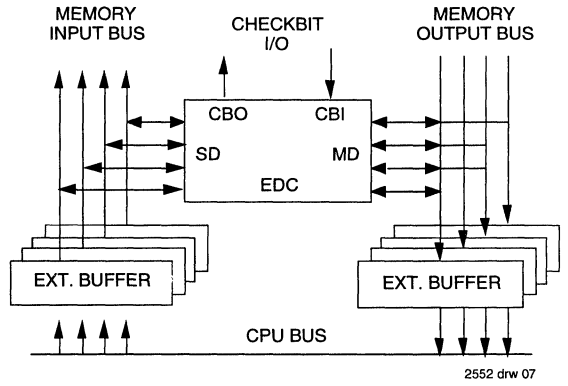


Figure 3. Bypassed Separate I/O Configuration

Figure 4 illustrates the single-chip generate-only mode for very fast 64-bit checkbit generation in systems that use separate checkbit-generate and detect-correct units. If this is not desired, 64-bit checkbit generation and correction can be done with just 2 EDC units. 64-bit correction is also straightforward, fast and requires no extra hardware for the expansion.

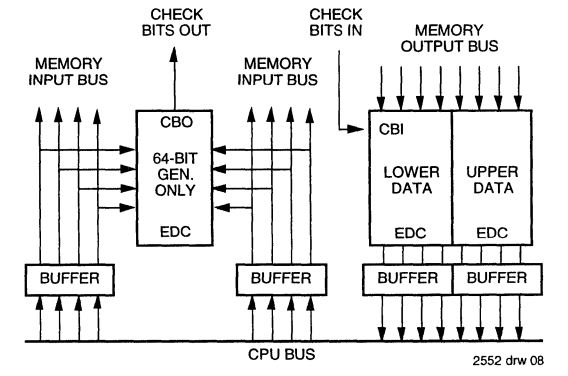


Figure 4. Separate Generate/Correction Units with 64-Bit Checkbit Generation

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FUNCTIONAL DESCRIPTION

The error detection/correction codes consist of a modified Hamming code; it is identical to that used in the IDT49C460.

32-BIT MODE (CODE ID 1,0=00)

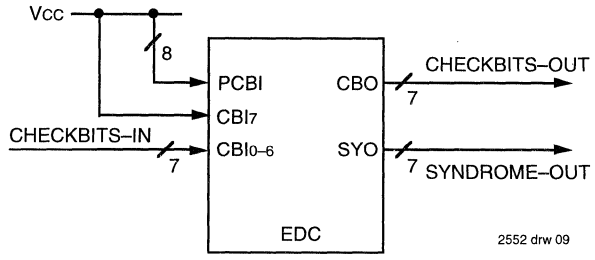

Figure 5. 32-Bit Mode

64-BIT MODE (CODE ID 1,0=10 & 11)

The expansion bus topology is shown in Figure 6. This topology allows the syndrome bits used by the correction logic to be generated simultaneously in both parts used in the expansion. During a 64-bit detection or correction operation, "Partial-Checkbit" data and "Partial-Syndrome" data is simultaneously exchanged between the two EDC units in opposite directions on dedicated expansion buses. This results in very short 64-bit detection and correction times.

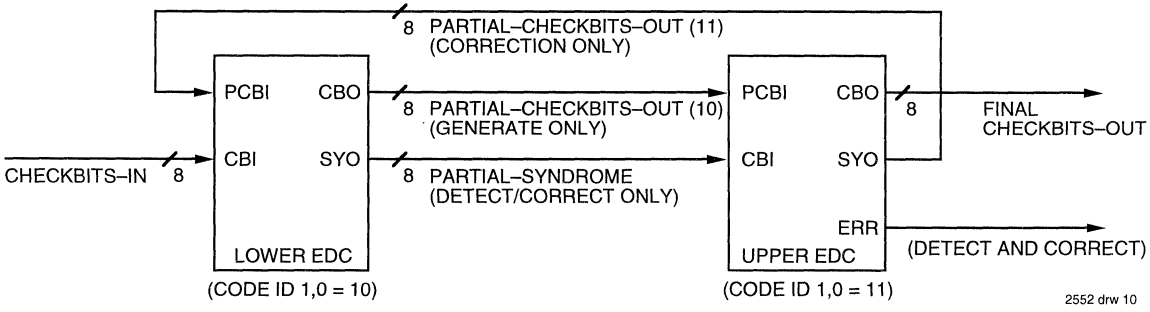

Figure 6. 64-Bit Mode — 2 Cascaded IDT49C465 Devices

64-BIT GENERATE-ONLY MODE (CODE ID 1,0=01)

If the Identity pins CODE ID 1,0 = 01, a single EDC is placed in the 64-bit "Generate-only" mode. In this mode, the lower 32 bits of the 64-bit data word enter the device on the MD_{0-31} inputs and the upper 32-bits of the 64 bit data word enter the device on the SD_{0-31} inputs. This provides the device with the full 64-bit word from memory. The resultant generated checkbits are output on the CBO_{0-7} outputs. The generate time is less than that resulting from using a 2-chip cascade.

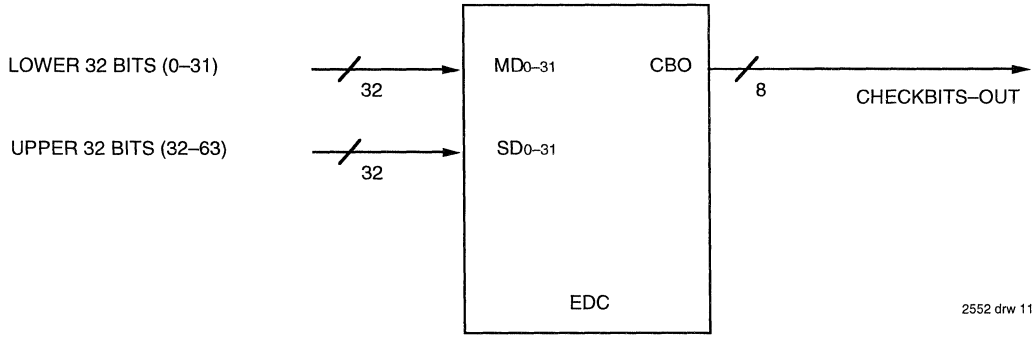

Figure 7. 64-Bit "Generate-Only" Mode (Single Chip)

PIN DESCRIPTIONS

Symbol	I/O		Name and Function
I/O Buses and Controls			
SD_{0-7} SD_{8-15} SD_{16-23} SD_{24-31}	I/O		**System Data Bus**: Data from MD_{0-31} appears at these pins corrected if MODE 2-0 = x11, or uncorrected in the other modes. The BE_n inputs must be high and the $\overline{SOE}$ pin must be low to enable the SD output buffers during a read cycle. (Also, see diagnostic section.) **Separate I/O memory systems:** In a write or partial-write cycle, the byte not-to-be-modified is output on SD_n to n+7 for re-writing to memory, if BE_n is high and $\overline{SOE}$ is low. The new bytes to be written to memory are input on the SD_n pins, for writing checkbits to memory, if BE_n is low. **Bi-directional memory systems:** In a write or partial-write cycle, the byte not-to-be-modified is re-directed to the MD I/O pins, if BE_n is high, for checkbit generation and rewriting to memory via the MD I/O pins. $\overline{SOE}$ must be high to avoid enabling the output drivers to the system bus in this mode. The new bytes to be written are input on the SD_n pins for checkbit generation and writing to memory. BE_n must be low to direct input data from the System Data bus to the MD I/O pins for checkbit generation and writing to the checkbit memory.
SLE	I		**System Latch Enable**: SLE is an input used to latch data at the SD inputs. The latch is transparent when SLE is high; the data is latched when SLE is low.
$\overline{PLE}$	I		**Pipeline Latch Enable**: $\overline{PLE}$ is an input which controls a pipeline latch, which controls data to be output on the SD bus and the MD bus during byte merges. Use of this latch is optional. The latch is transparent when $\overline{PLE}$ is low; the data is latched when $\overline{PLE}$ is high.
$\overline{SOE}$	I		**System Output Enable**: When low, enables System output drivers and Parity output drivers if corresponding Byte Enable inputs are high.
BE_{0-3}	I		**Byte Enables**: In systems using separate I/O memory buses, BE_n is used to enable the SD and Parity outputs for byte n. The BE_n pins also control the "Byte mux". When BE_n is high, the corrected or uncorrected data from the Memory Data latch is directed to the MD I/O pins and used for checkbit generation for byte n. This is used in partial-word-write operations or during correction cycles. When BE_n is low, the data from the System Data latch is directed to the MD I/O pins and used for checkbit generation for byte n. BE_0 controls SD_{0-7} BE_2 controls SD_{16-23} BE_1 controls SD_{8-15} BE_3 controls SD_{24-31}
MD_{0-31}	I/O		**Memory Data Bus:** These I/O pins accept a 32-bit data word from main memory for error detection and/or correction. They also output corrected old data or new data to be written to main memory when the EDC unit is used in a bi-directional configuration.
MLE	I		**Memory Latch Enable**: MLE is used to latch data from the MD inputs and checkbits from the CBI inputs. The latch is transparent when MLE is high; data is latched when MLE is low. When identified as the upper slice in a 64-bit cascade, the checkbit latch is bypassed.
$\overline{MOE}$	I		**Memory Output Enable**: $\overline{MOE}$ enables Memory Data Bus output drivers when low.
P_{0-3}	I/O		**Parity I/O**: The parity I/O pins for Bytes 0 to 3. These pins output the parity of their respective bytes when that byte is being output on the SD bus. These pins also serve as parity inputs and are used in generating the Parity ERRor ($\overline{PERR}$) signal under certain conditions (see Byte Enable definition). The parity is odd or even depending on the state of the Parity SELect pin (PSEL).
PSEL	I		**Parity SELect**: If the Parity SELect pin is low, the parity is even. If the Parity SELect pin is high, the parity is odd.
Inputs			
CBI_{0-7}	I		**CheckBits-In** (00) CheckBits-In-1 (10) Partial-Syndrome-In (11): In a single EDC system or in the lower slice of a cascaded EDC system, these inputs accept the checkbits from the checkbit memory. In the upper slice in a cascaded EDC system, these inputs accept the "Partial-Syndrome" from the lower slice (Detect/Correct path).
PCBI 0-7	I		**Partial-CheckBits-In** (10) Partial-CheckBits-In (11): In a single EDC system, these inputs are unused but should not be allowed to float. In a cascaded EDC system, the "Partial-Checkbits" used by the lower slice are accepted by these inputs (Correction path only). In the upper slice of a cascaded EDC system, "Partial-Checkbits" generated by the lower slice are accepted by these inputs (Generate path).
CODE $ID_{1,0}$	I		**CODE IDentity**: Inputs which identify the slice position/ functional mode of the IDT49C465. (00) Single 32-bit EDC unit (10) Lower slice of a 64-bit cascade (01) 64-bit "Checkbit-generate-only" unit (11) Upper slice of a 64-bit cascade

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PIN DESCRIPTIONS (Con't.)

Symbol	I/O		Name and Function
Inputs (Con't.)			
MODE 2-0	I		**MODE select:** Selects one of four operating modes.
		(x11)	**"Normal" Mode:** Normal EDC operation (Flow-thru correction and generation).
		(x10)	**"Generate-Detect" Mode:** In this mode, error correction is disabled. Error generation and detection are normal.
		(000)	**"Error-Data-Output" Mode:** Allows the uncorrected data captured from an error event by the Error-Data Register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by toggling $\overline{\text{CLEAR}}$ low. The Syndrome Register and Error-Data Register record the syndrome and uncorrected data from the first error that occurs after they are reset by the $\overline{\text{CLEAR}}$ pin. The Syndrome Register and Error-Data Register are updated when there is a positive edge on SYNCLK, an error condition is indicated ($\overline{\text{ERR}}$ = low), and the Error Counter indicates zero. **All-Zero-Data Source:** In Error-Data-Output Mode, clearing the Error-Data Register provides a source of all-zero-data for hardware initialization of memory, if this desired.
		(x01)	**Diagnostic-Output Mode:** In this mode, the contents of the Syndrome Register , Error Counter and Error-Type Register are output on the SD bus. This allows the syndrome bytes for an indicated error to be read by the system for error-logging purposes. The Syndrome Register and the Error-Data Register are updated when there is a positive edge on SYNCLK, an error condition is indicated and the Error Counter indicates zero errors. Thus, the Syndrome Register saves the syndrome that was present when the first error occurred after the Error Counter was cleared. The Syndrome Register and the Error Counter are cleared by toggling $\overline{\text{CLEAR}}$ low. The Error Counter lets the system tell if more than one error has occurred since the last time the Syndrome Register or Error-Data Register was read.
		(100)	**Checkbit-Injection Mode:** In the "Checkbit-Injection" Mode, diagnostic checkbits may be input on System Data Bus bits 0-7 (see Diagnostic Features - Detailed Description).
$\overline{\text{CLEAR}}$	I		**CLEAR**: When the $\overline{\text{CLEAR}}$ pin is taken low, the Error-Data Register, the Syndrome Register, the Error Counter and the Error-Type Register are cleared.
SYNCLK	I		**SYNdrome CLocK**: If $\overline{\text{ERR}}$ is low, and the Error Counter indicates zero errors, syndrome bits are clocked into the Syndrome Register and data from the outputs of the Memory Data input latch are clocked into the Error-Data Register on the low-to-high edge of SYNCLK. If $\overline{\text{ERR}}$ is low, the Error Counter will increment on the low-to-high edge of SYNCLK, unless the Error Counter indicates fifteen errors.
$\overline{\text{SCLKEN}}$	I		**SynCLK ENable**: The $\overline{\text{SCLKEN}}$ enables the SYNCLK signal. SYNCLK is ignored if $\overline{\text{SCLKEN}}$ is high.
Outputs and Enables			
$\text{CBO}_{0\text{-}7}$	O		**CheckBits-Out** (00, 01) Partial-CheckBits-Out (10) Checkbits-Out (11): In a single EDC system, the checkbits are output to the checkbit memory on these outputs. In the lower slice in a cascaded EDC system, the "Partial-checkbits" used by the upper slice are output by these outputs (Generate path only). In the upper slice in a cascade, the "Final-Checkbits" appear at these outputs (Generate path only).
$\overline{\text{CBOE}}$	I		**CheckBits Out Enable**: Enables CheckBit Output drivers when low.
$\text{SYO}_{0\text{-}7}$	O		**SYndrome-Out** (00) Partial-SYndrome-Out (10) Partial-Checkbits-Out (11): In a 32-bit EDC system, the syndrome bits are output on these pins. In the lower slice in a 64-bit cascaded system, the "Partial-Syndrome" bits appear at these outputs (Detect/ Correct path). In the upper slice in a cascaded EDC system, the "Partial-Checkbits" appear at these outputs (Correct path only). In a 64-bit cascaded system, the "Final-Syndrome" may be accessed in the "Diagnostic-Output" Mode from either the lower or the upper slice since the final syndrome is contained in both.
$\overline{\text{ERR}}$	O		**ERROR**: When in "Normal" and "Detect only" modes, a low on this pin indicates that one or more errors have been detected. $\overline{\text{ERR}}$ is not gated or latched internally.
$\overline{\text{MERR}}$	O		**Multiple ERRor**: When in "Normal" and "Detect only" modes, a low on this pin indicates that two or more errors have been detected. $\overline{\text{MERR}}$ is not gated or latched internally.
$\overline{\text{PERR}}$	O		**Parity ERRor**: A low on this pin indicates a parity error which has resulted from the active bytes defined by the 4 Byte Enable pins. Parity ERRor ($\overline{\text{PERR}}$) is not gated or latched internally (see Byte Enable definition).
Power Supply Pins			
$\text{Vcc}_{1\text{-}10}$	P		+5 Volts
$\text{GND}_{1\text{-}12}$	P		Ground

2552 tbl 02

DIAGNOSTIC DATA FORMAT (SYSTEM BUS)

Latched Data																Data Out (Unlatched)															
Error Type		Re-served		Error Counter				Syndrome bits								Partial Checkbits								Checkbits							
Byte 3								Byte 2								Byte 1								Byte 0							
S	M	-	-	2^3	2^2	2^1	2^0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
31	30			27				24	23						16	15							8	7							0

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DIAGNOSTIC FEATURES — DETAILED DESCRIPTION

Mode 2-0	
x11	**"NORMAL" Mode** In this mode, operation is "Normal" or non-diagnostic.
x10	**"GENERATE-DETECT" Mode** When the EDC unit is in the **"Generate-Detect" Mode**, data is not corrected or altered by the error correction network. (Also referred to as the "Detect-only" Mode.)
000	**"ERROR-DATA-OUTPUT" Mode** In this mode, the 32-bit data from the Error-Data Register is output on the SD bus. **Error Data Register**: The uncorrected data from the Memory Data bus input latch is stored in the Error-Data Register if the error counter contents indicates "0" and there is a positive transition on the SYNCLK input when the $\overline{ERR}$ signal is low. Thus, the Error-Data Register contains memory data corresponding to the first error to occur since the register was cleared. This register is cleared by pulling the $\overline{CLEAR}$ input low. The register is read via the System Data bus by entering the **"Error-Data-Output"** Mode and enabling the System Data bus output drivers. **All-Zero-Data**: The Error-Data Register can be used as an "all-zero-data" data source for memory initialization in systems where the initialization process is to be done entirely by hardware.
x01	**"DIAGNOSTIC-OUTPUT" Mode** In this mode, data from the diagnostic registers, the PCBI bus and the CBI bus is output on the SD bus. **Direct Checkbit Readback**: Internal data paths allow both the "Partial-CheckBit-Input" bus and the data in the "CheckBit-Input" latch to be read directly by the system bus for diagnostic purposes. Both the Checkbit Input Bus and the Partial Checkbit Input Bus are read via the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus output drivers. The checkbits are output on System Data bus bits 0-7; the Partial Checkbits are output on bits 8-15. **Syndrome Register:** After an error has been detected, the syndrome bits generated are clocked into the internal Syndrome Register if the error counter contents indicates "0" and there is a positive transition on the SYNCLK input when the $\overline{ERR}$ signal is low. This register is cleared by pulling the $\overline{CLEAR}$ input low. The register is read via the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus outputs. This data is output on SD bits 16-23. **Error Counter**: The 4-bit on-board error counter is incremented if the error counter contents do not indicate FF HEX, which corresponds to a count of 15, and there is a positive transition on the SYNCLK input when the $\overline{ERR}$ signal is low. This counter is cleared by pulling the $\overline{CLEAR}$ input low. The counter is read via the System Data bus by entering the **"Diagnostic-Output" Mode** and enabling the System Data bus output drivers. This data is output on System Data bus bits 24-27. **Test Register**: These 2 bits are reserved for factory diagnostics only and must not be used by system software. This data is output on System Data bus bits 28-29. **Error-Type Register**: The Error-Type Register, clocked by the SYNCLK input, saves 2 bits which indicate whether a recorded error was a single or a multiple-bit error. This register holds only the first error type to occur after the last Clear operation. This data is output on System Data bus bits 30-31.
100	**Direct Read-Path Checkbit Injection**: In the **"Checkbit-Injection" Mode**, bits 0-7 of the System Data input latch are presented to the inputs of the Checkbit Input latch. If MLE is strobed, the checkbit latch will be loaded with this value in place of the checkbits from memory. By inserting various checkbit values, operation of the correction function of the EDC can be verified "on-board". Except for the "Checkbit-Injection" function, operation in this mode is identical to "Normal" Mode operation.

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OPERATING MODE CHARTS

SLICE IDENTIFICATION

CODE ID 1	CODE ID 0	Slice Definition
0	0	32-bit Flow-Thru EDC
0	1	64-bit GENERATE Only EDC
1	0	64-bit EDC- Lower 32 bits (0-31)
1	1	64-bit EDC- Upper 32 bits (32-63)

2552 tbl 04

SLICE POSITION CONTROL

CODE ID	Slice Position/ Functional Operation	$\overline{SOE}$	SD Bus	$\overline{MOE}$	MD Bus	Checkbit Buses: PCBI Bus	CBI Bus	CBO Bus	SYO Bus	P Bus	$\overline{PERR}$
1 0	Width =		32		32	8	8	8	8	4	1
0 0	Single 32-bit EDC unit										
	Generate(1)	1	Sys. 0–31	0	Sys. Byte Mux	—	—	CBs out	—	P in	active
	Detect/Correct(2)	0	Pipe. latch	1	MD 0–31	—	CBs in	—	Syn. out	P out	—
0 1	"64-bit Generate-only"	1	Sys. 32–63	1	Sys. 0–31	—	—	CBs out	—	—	—
1 0	Lower word, 64-bit bus										
	Generate(1)	1	Sys. 0–31	0	MD 0–31	—	—	PCBs out	—	P in	active
	Detect/Correct(2)	0	Pipe. latch	1	MD 0–31	U-SYOout	CBs in	—	Par.Synd	P out	—
1 1	Upper word, 64-bit bus										
	Generate(1)	1	Sys. 32–63	0	MD 32–63	L-CBOout	—	F.CBs out	—	P in	active
	Detect/Correct(2)	0	Pipe. latch	1	MD 32–63	—	L-SYOout	—	Par.Cbits	P out	—

NOTES:
1. Checkbits generated from the data in the SD Latch.
2. Corrected data residing in the Pipe Latch.

2552 tbl 05

FUNCTIONAL MODE CONTROL

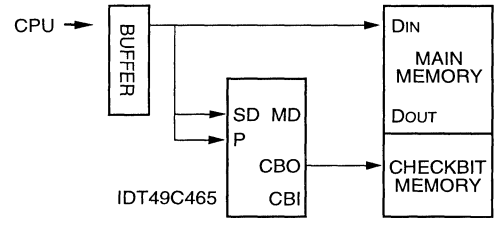
MODE 2	MODE 1	MODE 0	Functional Mode of SD Bus	$\overline{SOE}$	SD Bus	$\overline{MOE}$	MD Bus	Checkbit Buses: PCBI Bus	CBI Bus	CBO Bus	SYO Bus	P Bus	$\overline{PERR}$
2	1	0	Width =		32		32	8	8	8	8	4	1
x	1	1	**"Normal"**										
			Generate	1	CPU Data	0	Pipe. latch	—	—	CB out	—	P in	active
			Correct	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—
x	1	0	**"Generate-Detect"**										
			Generate	1	CPU Data	0	Pipe. latch	—	—	CB out	—	P in	active
			Detect	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—
0	0	0	**"Error-Data-Output"**	0	Err. D. latch	—	—	—	—	—	—	—	—
x	0	1	**"Diagnostic-Output"**	0	CBin latch PCBIin bus Syn. register Err. counter Er. type reg.	—	—	PCBI in	CB in	—	—	—	—
1	0	0	**"Checkbit-Injection"**										
			Generate	1	SDin latch	0	Pipe. latch	—	—	CB out	—	P in	active
			Inject Checkbits	1	SD0–7 in	0	Pipe. latch	—	—	—	—	—	—
			Correct	0	Pipe. latch	1	RAM Data	—	CB in	—	—	P out	—

2552 tbl 06

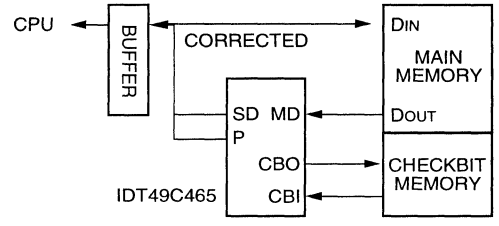
PRIMARY DATA PATH vs. MEMORY CONFIGURATION

SEPARATE I/O MEMORIES:

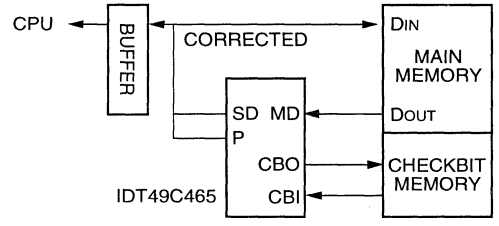
1. Checkbit Generation
Write New Word to Memory



2. Data Correction
Read Memory Word

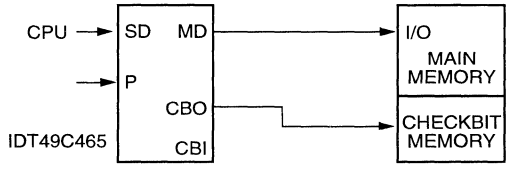


3. Memory Generation
Re-write Corrected Word to Memory

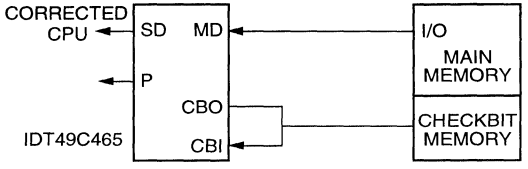


COMMON I/O MEMORIES:

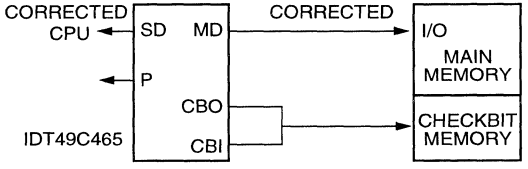
1. Checkbit Generation
Write New Word to Memory



2. Data Correction
Read Memory Word



3. Memory Generation
Re-write Corrected Word to Memory



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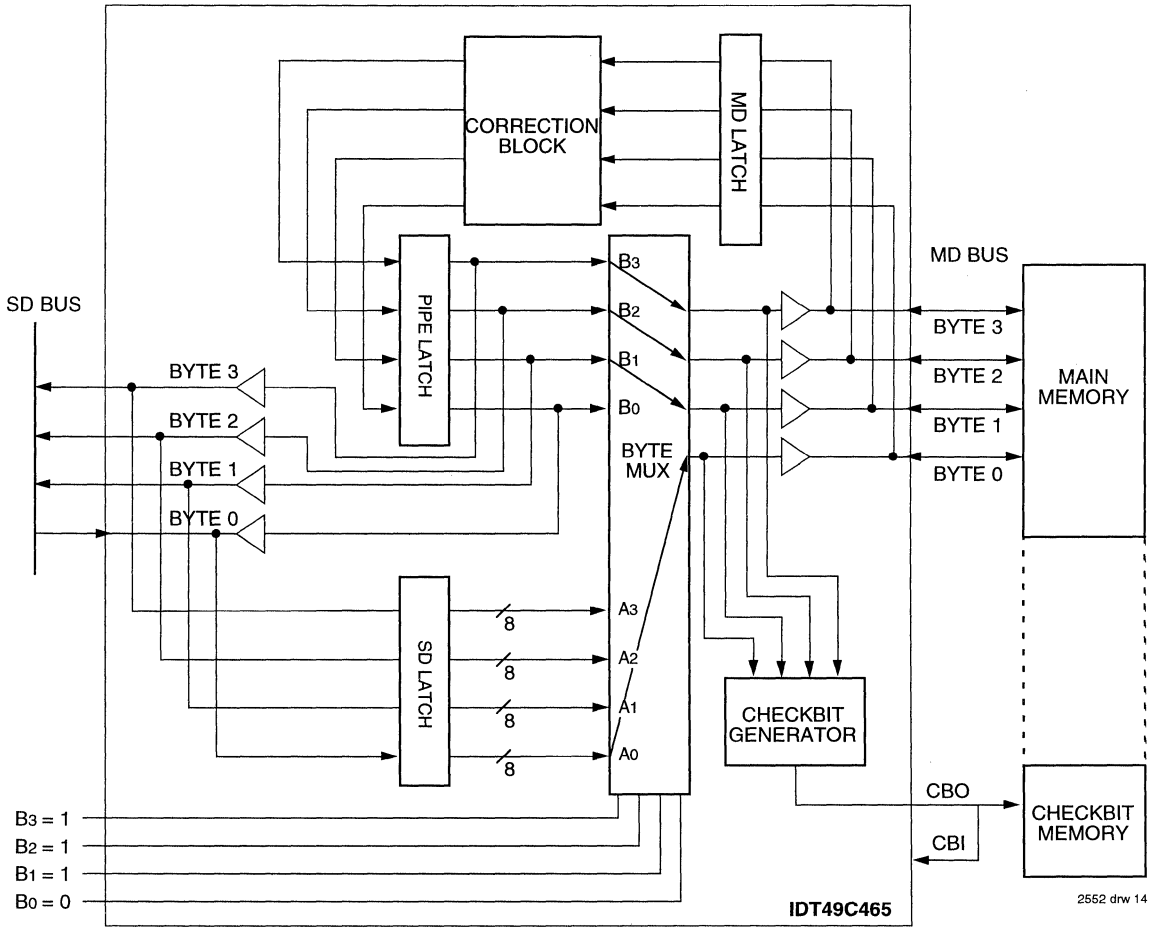
PARTIAL-WORD-WRITE OPERATIONS

FOR COMMON I/O MEMORIES:



In order to perform a partial-word-write operation, the complete word in question must be read from memory. This must be done in order to correct any error which may have occurred in the old word. Once the complete, corrected word is available, with all the bytes verified, the new word may be assembled in the byte mux and the new checkbits generated.

The example shown above illustrates the case of combining 3 bytes from an old word with a new lower order byte to form a new word. The new word, along with the new checkbits, may now be written to memory.

In the separate I/O memory configuration, the situation is similar except that the new word is output on the SD Bus instead of the MD Bus (refer to previous page).

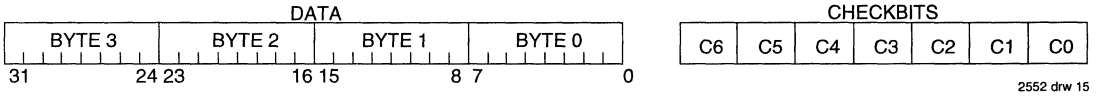
32-BIT DATA WORD CONFIGURATION

A single IDT49C465 EDC unit, connected as shown below, provides all the logic needed for single-bit error correction, and double-bit error detection, of a 32-bit data field. The identification code (00) indicates 7 checkbits are required. The CBI_7 pin should be tied high.

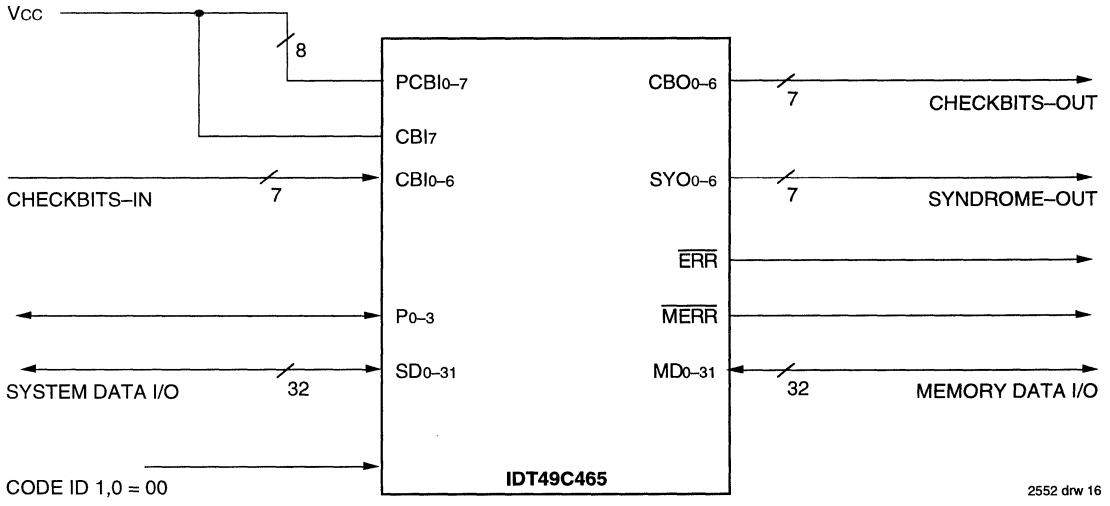
The 39-bit data format for four bytes of data and 7 checkbits is indicated below.

Syndrome bits are generated by an exclusive-OR of the generated checkbits with the checkbits read from memory. For example, Sn is the XOR of checkbits from those read with those generated. During Data Correction, the syndrome bits are used to complement (correct) single-bit errors in the data bits.

32-BIT DATA FORMAT



32-BIT HARDWARE CONFIGURATION



64-BIT DATA WORD CONFIGURATION

Two IDT49C465 EDC units, connected as shown below, provide all the logic needed for single-bit error correction, and double-bit error detection, of a 64-bit data field. The "Slice Identification" Table gives the CODE ID1,0 values needed for distinguishing the upper 32 bits from the lower 32 bits. Final generated checkbits, $\overline{ERR}$ and $\overline{MERR}$ (indicates multiple errors) signals come from the upper slice, the IC with CODE ID1,0=11. Control signals not shown are connected to both units in parallel.

Data-In bits 0 through 31 are connected to the same numbered inputs of the EDC with CODE ID1,0=10, while Data-In bits 32 through 63 are connected to data inputs 0 to 31, respectively, for the EDC unit with CODE ID1,0=11.

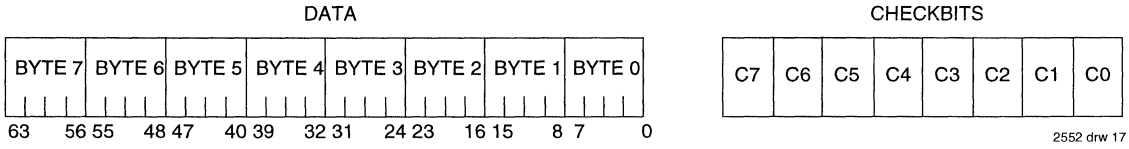
The 72-bit data format of data and checkbits is indicated below.

Correction of single-bit errors in the 64-bit configuration requires a simultaneous exchange of partial checkbits and partial syndrome bits between the upper and lower units.

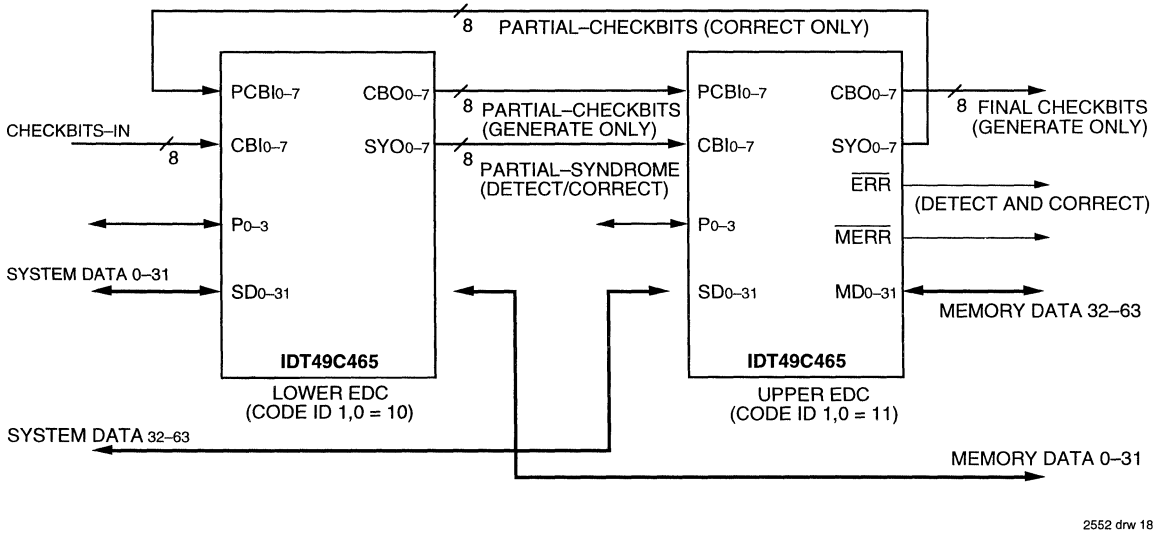
Syndrome bits are generated by an exclusive-OR of the generated checkbits with the checkbits read from memory. For example, Sn is the XOR of checkbits read and checkbits generated. During data correction, the syndrome bits are used to complement (correct) single-bit errors in the data bits. For double or multiple-bit error detection, the data available as output by the Pipeline Latch is not defined.

Critical AC performance data is provided in the Table "Key AC Calculations", which illustrates the delays that are critical to 64-bit cascaded performance. As indicated, a summation of propagation delays is required when cascading these units.

64-BIT DATA FORMAT



64-BIT HARDWARE CONFIGURATION



DEFINITIONS OF TERMS:

$D_0 - D_{31}$ = System Data and/or Memory Data Inputs
$CBI_0 - CBI_7$ = Checkbit Inputs
$PCBI_0 - PCBI_7$ = Partial Checkbit Inputs
$FS_0 - FS_7$ = Final Internal Syndrome bits

FUNCTIONAL EQUATIONS:

The equations below describe the terms used in the IDT49C465 to determine the values of the partial checkbits, checkbits, partial syndromes and final internal syndromes. NOTE: All "⊕" symbols below represent the "EXCLUSIVE-OR" function.

$PA = D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{20} \oplus D_{22} \oplus D_{24} \oplus D_{26} \oplus D_{28}$

$PB = D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{19} \oplus D_{20} \oplus D_{23} \oplus D_{25} \oplus D_{26} \oplus D_{29} \oplus D_{31}$

$PC = D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{16} \oplus D_{17} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{27} \oplus D_{28} \oplus D_{29}$

$PD = D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{14} \oplus D_{15} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23} \oplus D_{30} \oplus D_{31}$

$PE = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$

$PF = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{24} \oplus D_{25} \oplus D_{26} \oplus D_{27} \oplus D_{28} \oplus D_{29} \oplus D_{30} \oplus D_{31}$

$PG = D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15} \oplus D_{16} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{20} \oplus D_{21} \oplus D_{22} \oplus D_{23}$

$PH_0 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$

$PH_1 = D_1 \oplus D_2 \oplus D_3 \oplus D_5 \oplus D_8 \oplus D_9 \oplus D_{11} \oplus D_{14} \oplus D_{17} \oplus D_{18} \oplus D_{19} \oplus D_{21} \oplus D_{24} \oplus D_{25} \oplus D_{27} \oplus D_{30}$

$PH_2 = D_0 \oplus D_4 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15} \oplus D_{16} \oplus D_{20} \oplus D_{22} \oplus D_{23} \oplus D_{26} \oplus D_{28} \oplus D_{29} \oplus D_{31}$

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

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DETAILED DESCRIPTION — CHECKBIT AND SYNDROME GENERATION vs. CODE ID

LOGIC EQUATIONS FOR THE CBO OUTPUTS

Checkbit Generation	CODE ID 1,0		
	00	10	11
	Final Chkbits	Partial Checkbits	Final Checkbits
CBO_0	PH_0	PH_1	$PH_2 \oplus PCBI_0$
CBO_1	PA	PA	$PA \oplus PCBI_1$
CBO_2	$\overline{PB}$	$\overline{PB}$	$PB \oplus PCBI_2$
CBO_3	$\overline{PC}$	$\overline{PC}$	$PC \oplus PCBI_3$
CBO_4	PD	PD	$PD \oplus PCBI_4$
CBO_5	PE	PE	$PE \oplus PCBI_5$
CBO_6	PF	PF	$PF \oplus PCBI_6$
CBO_7	—	PF	$PG \oplus PCBI_7$

2552 tbl 07

LOGIC EQUATIONS FOR THE SYO OUTPUTS

Checkbit/ Syndrome Generation	CODE ID 1,0		
	00	10	11
	Final Syndrome	Partial Syndrome	Partial Checkbits
SYO0	PH0 ⊕ CBI0	PH1 ⊕ CBI0	PH2
SYO1	PA ⊕ CBI1	PA ⊕ CBI1	PA
SYO2	$\overline{PB}$ ⊕ CBI2	$\overline{PB}$ ⊕ CBI2	PB
SYO3	$\overline{PC}$ ⊕ CBI3	$\overline{PC}$ ⊕ CBI3	PC
SYO4	PD ⊕ CBI4	PD ⊕ CBI4	PD
SYO5	PE ⊕ CBI5	PE ⊕ CBI5	PE
SYO6	PF ⊕ CBI6	PF ⊕ CBI6	PF
SYO7	—	PF ⊕ CBI7	PG

2552 tbl 08

LOGIC EQUATIONS FOR THE FINAL SYNDROME (FSn)

Final Syndrome Generation	CODE ID 1,0	
	00	10, 11
	Final Syndrome	Final Internal Syndrome
FS_0	$PH_0 \oplus CBI_0$	PH_1 (L) ⊕ PH_2 (U) ⊕ CBI_0
FS_1	$PA \oplus CBI_1$	PA (L) ⊕ PA (U) ⊕ CBI_1
FS_2	$\overline{PB} \oplus CBI_2$	PB (L) ⊕ PB (U) ⊕ CBI_2
FS_3	$\overline{PC} \oplus CBI_3$	PC (L) ⊕ PC (U) ⊕ CBI_3
FS_4	$PD \oplus CBI_4$	PD (L)⊕ PD (U) ⊕ CBI_4
FS_5	$PE \oplus CBI_5$	PE (L) ⊕ PE (U) ⊕ CBI_5
FS_6	$PF \oplus CBI_6$	PF (L) ⊕ PF (U) ⊕ CBI_6
FS_7	—	PF (L) ⊕ PG (U)⊕ CBI_7

2552 tbl 09

32-BIT SYNDROME DECODE TO BIT-IN-ERROR (1)

					HEX	0	1	2	3	4	5	6	7
					S6	0	0	0	0	1	1	1	1
	Syndrome				S5	0	0	1	1	0	0	1	1
	Bits				S4	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0									
0	0	0	0	0		*	C4	C5	T	C6	T	T	30
1	0	0	0	1		C0	T	T	14	T	M	M	T
2	0	0	1	0		C1	T	T	M	T	2	24	T
3	0	0	1	1		T	18	8	T	M	T	T	M
4	0	1	0	0		C2	T	T	15	T	3	25	T
5	0	1	0	1		T	19	9	T	M	T	T	31
6	0	1	1	0		T	20	10	T	M	T	T	M
7	0	1	1	1		M	T	T	M	T	4	26	T
8	1	0	0	0		C3	T	T	M	T	5	27	T
9	1	0	0	1		T	21	11	T	M	T	T	M
A	1	0	1	0		T	22	12	T	1	T	T	M
B	1	0	1	1		17	T	T	M	T	6	28	T
C	1	1	0	0		T	23	13	T	M	T	T	M
D	1	1	0	1		M	T	T	M	T	7	29	T
E	1	1	1	0		16	T	T	M	T	M	M	T
F	1	1	1	1		T	M	M	T	0	T	T	M

2552 tbl 12

NOTES:

1. The table indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single bit-in-error
   T = Two errors detected
   M = Three or more errors detected

DETAILED DESCRIPTION — 32-BIT CONFIGURATION

32-BIT MODIFIED HAMMING CODE — CHECKBIT ENCODING CHART[1]

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)	X				X		X	X	X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								

2552 tbl 10

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X					X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X

NOTE:

2552 tbl 11

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit C0 is the Exclusive-OR function of the 16 data input bits marked with an X.

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DETAILED DESCRIPTION — 64-BIT CONFIGURATION

64-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART[1, 2]

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2552 tbl 13

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2552 tbl 14

Generated Checkbits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2552 tbl 15

Generated Checkbits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2552 tbl 16

NOTES:

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit C0 is the Exclusive-OR function of the 64 data input bits marked with an X.
2. The checkbit is generated as either an XOR or an XNOR of the 64 data bits noted by an "X" in the table.

DETAILED DESCRIPTION — 64-BIT CONFIGURATION (Con't.)

64-BIT SYNDROME DECODE TO BIT-IN-ERROR(1)

				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			Syndrome	S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			Bits	S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																
0	0	0	0	0	*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES: 2552 tbl 17

1. The table indicates the decoding of the seven syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single bit-in-error
   T = Two errors detected
   M = Three or more detected

KEY AC CALCULATIONS — 64-BIT CASCADED CONFIGURATION

	64-Bit Propagation Delay		Total AC Delay for IDT49C465 in 64-bit Mode
			(L) = Lower slice
Mode	From	To	(U) = Upper slice
Generate	SD Bus	Checkbits out	SD to CBO(L) + PCBI to CBO(U) t SC(L) + t PCC(U)
Detect	MD Bus	$\overline{ERR}$ for 64-bits	MD to SYO(L) + CBI to $\overline{ERR}$ (U) t MSY(L) + t CE (U)
	MD Bus	$\overline{MERR}$ for 64-bits	MD to SYO(L) + CBI to $\overline{M}$ $\overline{ERR}$ t MSY(L) + t CME ($\overline{U}$)
Correct	MD Bus	Corrected data out	MD to SYO(L) + CBI to SD(U) t MSY(L) + t CS (U) (or) → MD to SYO(U) + PCBI to SD(L) t MSY(U) + t PCS(L)

NOTE: 2552 tbl 18

1. (or) = Whichever is worse.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2552 tbl 19

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Ratings for extended periods of time may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Pkg.	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	PGA	10	pF
			PQFP	5	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	PGA	12	pF
			PQFP	7	

NOTE: 2552 tbl 20

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)			Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level(4)	Guaranteed Logic HIGH	Normal Inputs		2.0	—	—	V
			Hysteresis Inputs		3.0	—	—	
V_{IL}	Input LOW Level(4)	Guaranteed Logic LOW			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			—	—	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND			—	—	–5.0	µA
I_{OZ}	Off State (Hi-Z)	V_{CC} = Max.	V_O = 0V		—	—	–10	µA
			V_O = 3V		—	—	10	
I_{OS}	Short Circuit Current	V_{CC} = Max.(3)			–20	—	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –6mA	COM'L.	2.4	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –4mA	MIL.	2.4	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 12mA	COM'L.	—	—	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 6mA	MIL.	—	—	0.5	
V_H	Hysteresis	$\overline{CLEAR}$, MLE, $\overline{PLE}$, SLE, $\overline{SYNCLK}$, $\overline{SCLKEN}$			—	200	—	mV

NOTES: 2552 tbl 21

1. For conditions shown as min. or max., use appropriate value specified above for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient temperature and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Con't.)

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current CMOS Input Levels	V_{IN} = V_{CC} or GND V_{CC} = Max. All Inputs Outputs Disabled		—	—	5	mA
I_{CCQT}	Quiescent Power Supply Current TTL Input Levels	V_{IH} = 3.4V, V_{IL} = 0V V_{CC} = Max. All Inputs Outputs Disabled		—	—	1	mA/ input
I_{CCD1}	Dynamic Power Supply Current f = 10MHz	f_{CP} = 10MHz, 50% Duty Cycle V_{IH} = V_{CC}, V_{IL} = GND Read Mode, Outputs Disabled	COM'L.	—	—	100	mA
			MIL.	—	—	115	
I_{CCD2}	Dynamic Power Supply Current f = 20MHz	f_{CP} = 20MHz, 50% Duty Cycle V_{IH} = V_{CC}, V_{IL} = GND Read Mode, Outputs Disabled	COM'L.	—	—	200	mA
			MIL.	—	—	230	

2552 tbl 22

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified above for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient temperature, and maximum loading.
3. Total supply current is the sum of the Quiescent current and the dynamic current and is calculated as follows:
   $I_{CC} = I_{CCQ} + I_{CCQT} (N_T \times D_T) + I_{CCD} (f_{OP})$
   where: N_T = Total # of quiescent TTL inputs
   D_T = AC Duty cycle – % of time high (TTL)
   f_{OP} = Operating frequency

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AC PARAMETERS - 49C465A

PROPAGATION DELAY TIMES

				32-bit System Standalone Slice		64-bit "Generate only" Slice		64-bit System Lower Slice		64-bit System Upper Slice			
				CODE ID=00		CODE ID=01		CODE ID=10		CODE ID=11			
Number	Parameter Name	Parameter Description From Input (edge)	To Output (edge)	Com. Max.	Mil. Max.	Com. Max.	Mil. Max.	Com. Max.	Mil. Max.	Com. Max.	Mil. Max.	Unit	Refer to Timing Diagram Figure
GENERATE (WRITE) PARAMETERS													
01	t_{BC}	$\overline{BE}_N$	CBO	15	20	—	—	15	20	15	20	ns	—
02	t_{BM}	$\overline{BE}_N$	MD_{OUT}	15	20	—	—	15	20	15	20	ns	—
03	t_{MC}	**MD_{IN}**	**CBO**	—	—	**15**	**18**	—	—	—	—	ns	10
04	t_{PCC}	**PCB_I**	**CBO**	—	—	—	—	—	—	**12**	**18**	ns	7
05	t_{PPE}	P_{XIN}	$\overline{PERR}$	12	18	—	—	12	18	12	18	ns	—
06	t_{SC}		**CBO**	**14**	**18**	**14**	**18**	**14**	**18**	**14**	**18**	ns	7
07	t_{SM}	**SD_{IN}**	MD_{OUT}	12	18	—	—	12	18	12	18	ns	7
08	t_{SPE}		$\overline{PERR}$	12	18	—	—	12	18	12	18	ns	—
DETECT (READ) PARAMETERS													
09	t_{CE}		$\overline{ERR}$ Low	14	18	—	—	—	—	**12**	**18**	ns	8,10
10	t_{CME}	**CBI**	$\overline{MERR}$ = Low	15	20	—	—	—	—	15	20	ns	8,10
11	t_{CSY}		SYO	12	18	—	—	12	18	—	—	ns	8,10
12	t_{ME}		$\overline{ERR}$	**12**	**18**	—	—	—	—	12	18	ns	8,10
13	t_{MME}	**MD_{IN}**	$\overline{MERR}$	16	20	—	—	—	—	16	20	ns	8,10
14	t_{MSY}		**SYO**	16	20	—	—	**12**	**18**	**12**	**18**	ns	8,10
CORRECT (READ) PARAMETERS													
15	t_{CS}	**CBI**	**SD_{OUT}**	16	20	—	—	—	—	**16**	**20**	ns	8,11
16	t_{MP}		Px	18	22	—	—	18	22	18	22	ns	8,11
17	t_{MS}	**MD_{IN}**	**SD_{OUT}**	**14**	**18**	—	—	—	—	—	—	ns	8,11
18	t_{MSY}		**SYO**	16	20	—	—	**12**	**18**	**12**	**18**	ns	8,11
19	t_{PCS}	**PCBI**	**SD_{OUT}**	—	—	—	—	**13**	**18**	—	—	ns	11
DIAGNOSTIC PARAMETERS													
20	t_{CLR}	CLEAR = Low	SD_{OUT}	15	20	—	—	15	20	15	20	ns	15
21	t_{MIS}	MODE ID	SD_{OUT}	15	20	—	—	15	20	15	20	ns	15

NOTES:
1. Where "edge" is not specified, both HIGH and LOW edges are implied.
2. **BOLD** indicates critical system parameters.

2552 tbl 24

AC PARAMETERS - 49C465A

PROPAGATION DELAY TIMES FROM LATCH ENABLES

Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Com.'l. Max.	Mil. Max.	Unit	Refer to Timing Diagram Figure
22	t MLC			CBO	*	16	20	ns	13
23	t MLE			$\overline{ERR}$	*	13	18	ns	8, 10, 11
24	t MLME	MLE =	HIGH	$\overline{MERR}$	*	16	20	ns	8
25	t MLP			Px	*	18	22	ns	8, 11
26	t MLS			SDOUT	*	18	22	ns	8, 10, 11
27	t MLSY			SYO	*	15	20	ns	8, 10
28	t PLS	$\overline{PLE}$ =	LOW	SDOUT	*	10	12	ns	8, 11
29	t PLP	$\overline{PLE}$ =	LOW	Px	*	13	18	ns	8, 11
30	t SLC	SLE =	HIGH	CBO	*	16	20	ns	7, 9
31	t SLM	SLE =	HIGH	MDOUT	*	12	18	ns	7, 9

NOTE: 2552 tbl 27

"*" = Both HIGH and LOW edges are implied.

ENABLE AND DISABLE TIMES

Number	Parameter Name	Parameter Description: From Input	(edge)	To Output	(edge)	Com'l. Min.	Com'l. Max.	Mil. Min.	Mil. Max.	Unit	Refer to Timing Diagram Figure
32	t BESZx	BEN =	HIGH	SDOUT	*	2	13	2	16	ns	8, 10, 11
33	t BESxZ		LOW		Hi – Z	2	11	2	14	ns	
34	t BEPZx	BEN =	HIGH	POUT	*	2	13	2	16	ns	8, 11
35	t BEPxZ		LOW		Hi – Z	2	11	2	14	ns	
36	t CECZx	$\overline{CBOE}$ =	LOW	CBO	*	2	13	2	16	ns	7, 9
37	t CECxZ		HIGH		Hi – Z	2	11	2	14	ns	
38	t MEMZx	$\overline{MOE}$ =	LOW	MDOUT	*	2	13	2	16	ns	7, 9
39	t MEMxZ		HIGH		Hi – Z	2	11	2	14	ns	8, 10
40	t SESZx	$\overline{SOE}$ =	LOW	SDOUT	*	2	13	2	16	ns	8, 10
41	t SESxZ		HIGH		Hi – Z	2	11	2	14	ns	7, 9

NOTE: 2552 tbl 28

"*" = Delay to both edges.

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SET-UP AND HOLD TIMES - 49C465A

Number	Parameter Name	Parameter Description: From Input (edge)	To Output (edge)	Com.'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
42	t SSLS	SDIN Set-up *	before SLE = LOW	3	4	ns	7, 9
43	t SSLH	SDIN Hold *	after SLE = LOW	3	4	ns	7, 9
44	t MMLS	MDIN Set-up *	before MLE =LOW	3	4	ns	8, 10, 11
45	t MMLH	MDIN Hold *	after MLE = LOW	3	4	ns	8, 10, 11
46	t CMLS	CBI Set-up *	before MLE = LOW	3	4	ns	8, 10, 11
47	t CMLH	CBI Hold *	after MLE = LOW	3	4	ns	8, 10, 11
48	t MPLS	MDIN Set-up *	before $\overline{PLE}$ = HIGH	10	12	ns	—
49	t MPLH	MDIN Hold *	after $\overline{PLE}$ = HIGH	0	0	ns	—
50	t CPLS	CBI Set-up *	before $\overline{PLE}$ =HIGH	10	12	ns	—
51	t CPLH	CBI Hold *	after $\overline{PLE}$ = HIGH	0	0	ns	—
52	t PCPLS	PCBI Set-up *	before $\overline{PLE}$ = HIGH	10	12	ns	—
53	t PCPLH	PCBI Hold *	after $\overline{PLE}$ = HIGH	0	0	ns	—
DIAGNOSTIC SET-UP AND HOLD TIMES							
54	t CSCS	CBI Set-up *		10	12	ns	15
55	t MSCS	MDIN Set-up *	before SYNCLK=HIGH	10	12	ns	15
56	t MLSCS	MLE Set-up =HIGH		10	12	ns	15
57	t SESCS	SCLKEN Set-up =LOW		3	4	ns	15
58	t SESCH	SCLKEN Hold =LOW	after SYNCLK =HIGH	3	4	ns	15

NOTE:
"*" = Where "edge" is not specified, both HIGH and LOW edges are implied.

2552 tbl 32

MINIMUM PULSE WIDTH

Number	Parameter Name	Minimum Pulse Width: Input		Conditions	Com'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
59	t CLEAR	Min. $\overline{CLEAR}$ LOW time	to clear diag. registers	Data = Valid	8	10	ns	14
60	t MLE	Min. MLE HIGH time	to strobe new data	MD, CBI = Valid	5	6	ns	—
61	t PLE	Min. $\overline{PLE}$ LOW time	to strobe new data	SD = Valid	5	6	ns	—
62	t SLE	Min. SLE HIGH time	to strobe new data	SD = Valid	5	6	ns	—
63	t SYNCLK	Min. SYNCLK HIGH time	to clock in new data	SCKEN = LOW	5	6	ns	14

2552 tbl 33

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 18

2552 tbl 34

AC PARAMETERS - 49C465

PROPAGATION DELAY TIMES

Number	Parameter Name	Parameter Description From Input (edge)	To Output (edge)	32-bit System Standalone Slice CODE ID=00 Com. Max.	32-bit System Standalone Slice CODE ID=00 Mil. Max.	64-bit "Generate only" Slice CODE ID=01 Com. Max.	64-bit "Generate only" Slice CODE ID=01 Mil. Max.	64-bit System Lower Slice CODE ID=10 Com. Max.	64-bit System Lower Slice CODE ID=10 Mil. Max.	64-bit System Upper Slice CODE ID=11 Com. Max.	64-bit System Upper Slice CODE ID=11 Mil. Max.	Unit	Refer to Timing Diagram Figure
GENERATE (WRITE) PARAMETERS													
01	t_{BC}	$\overline{BE}_N$	CBO	20	25	—	—	20	25	20	25	ns	—
02	t_{BM}	$\overline{BE}_N$	MD_{OUT}	20	25	—	—	20	25	20	25	ns	—
03	t_{MC}	**MD_{IN}**	**CBO**	—	—	**17**	**20**	—	—	—	—	ns	10
04	t_{PCC}	**PC_{BI}**	**CBO**	—	—	—	—	—	—	**15**	**20**	ns	7
05	t_{PPE}	P_{XIN}	$\overline{PERR}$	15	20	—	—	15	20	15	20	ns	—
06	t_{SC}		**CBO**	**16**	**20**	**16**	**20**	**16**	**20**	**16**	**20**	ns	7
07	t_{SM}	**SD_{IN}**	MD_{OUT}	15	20	—	—	15	20	15	20	ns	7
08	t_{SPE}		$\overline{PERR}$	15	20	—	—	15	20	15	20	ns	—
DETECT (READ) PARAMETERS													
09	t_{CE}		$\overline{ERR}$ = LOW	16	20	—	—	—	—	**15**	**20**	ns	8,10
10	t_{CME}	**CBI**	$\overline{MERR}$ = LOW	20	24	—	—	—	—	20	24	ns	8,10
11	t_{CSY}		SYO	15	20	—	—	12	18	—	—	ns	8,10
12	t_{ME}		$\overline{ERR}$ = LOW	**15**	**20**	—	—	—	—	15	20	ns	8,10
13	t_{MME}	**MD_{IN}**	$\overline{MERR}$ = LOW	20	24	—	—	—	—	20	24	ns	8,10
14	t_{MSY}		**SYO**	18	22	—	—	**15**	**20**	**15**	**20**	ns	8,10
CORRECT (READ) PARAMETERS													
15	t_{CS}	**CBI**	**SD_{OUT}**	20	24	—	—	—	—	**20**	**24**	ns	8,11
16	t_{MP}		Px	20	26	—	—	20	26	20	26	ns	8,11
17	t_{MS}	**MD_{IN}**	**SD_{OUT}**	**16**	**20**	—	—	—	—	—	—	ns	8,11
18	t_{MSY}		**SYO**	18	22	—	—	**15**	**20**	**15**	**20**	ns	8,11
19	t_{PCS}	**PCBI**	**SD_{OUT}**	—	—	—	—	**15**	**20**	—	—	ns	11
DIAGNOSTIC PARAMETERS													
20	t_{CLR}	CLEAR = LOW	SD_{OUT}	20	24	—	—	20	24	20	24	ns	15
21	t_{MIS}	MODE ID	SD_{OUT}	20	24	—	—	20	24	20	24	ns	15

2552 tbl 23

NOTES:
1. Where "edge" is not specified, both HIGH and LOW edges are implied.
2. **BOLD** indicates critical system parameters.

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AC PARAMETERS - 49C465

PROPAGATION DELAY TIMES FROM LATCH ENABLES

Number	Parameter Name	Parameter Description: From Input (edge)	To Output (edge)	Com.'l. Max.	Mil. Max.	Unit	Refer to Timing Diagram Figure
22	t MLC	MLE = HIGH	CBO *	20	24	ns	13
23	t MLE		$\overline{ERR}$ *	15	20	ns	8, 10, 11
24	t MLME		$\overline{MERR}$ *	20	24	ns	8
25	t MLP		Px *	20	25	ns	8, 11
26	t MLS		SDOUT *	20	25	ns	8, 10, 11
27	t MLSY		SYO *	18	22	ns	8, 10
28	t PLS	$\overline{PLE}$ = LOW	SDOUT *	12	16	ns	8, 11
29	t PLP	$\overline{PLE}$ = LOW	Px *	16	20	ns	8, 11
30	t SLC	SLE = HIGH	CBO *	20	24	ns	7, 9
31	t SLM	SLE = HIGH	MDOUT *	15	20	ns	7, 9

NOTE:
"*" = Both HIGH and LOW edges are implied.

2552 tbl 25

ENABLE AND DISABLE TIMES

Number	Parameter Name	Parameter Description: From Input (edge)	To Output (edge)	Com'l. Min.	Com'l. Max.	Mil. Min.	Mil. Max.	Unit	Refer to Timing Diagram Figure
32	t BESZx	BEN = HIGH	SDOUT *	2	15	2	18	ns	8, 10, 11
33	t BESxZ	LOW	Hi – Z	2	13	2	16	ns	
34	t BEPZx	BEN = HIGH	POUT *	2	15	2	18	ns	8, 11
35	t BEPxZ	LOW	Hi – Z	2	13	2	16	ns	
36	t CECZx	$\overline{CBOE}$ = LOW	CBO *	2	15	2	18	ns	7, 9
37	t CECxZ	HIGH	Hi – Z	2	13	2	16	ns	
38	t MEMZx	$\overline{MOE}$ = LOW	MDOUT *	2	15	2	18	ns	7, 9
39	t MEMxZ	HIGH	Hi – Z	2	13	2	16	ns	8, 10
40	t SESZx	$\overline{SOE}$ = LOW	SDOUT *	2	15	2	18	ns	8, 10
41	t SESxZ	HIGH	Hi – Z	2	13	2	16	ns	7, 9

NOTE:
"*" = Delay to both edges.

2552 tbl 26

SET-UP AND HOLD TIMES - 49C465

Number	Parameter Name	Parameter Description: From Input (edge)	Parameter Description: To Output (edge)	Com.'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
42	t SSLS	SDIN Set-up *	before SLE =LOW	4	5	ns	7, 9
43	t SSLH	SDIN Hold *	after SLE = LOW	4	5	ns	7, 9
44	t MMLS	MDIN Set-up *	before MLE =LOW	4	5	ns	8, 10, 11
45	t MMLH	MDIN Hold *	after MLE = LOW	4	5	ns	8, 10, 11
46	t CMLS	CBI Set-up *	before MLE =LOW	4	5	ns	8, 10, 11
47	t CMLH	CBI Hold *	after MLE = LOW	4	5	ns	8, 10, 11
48	t MPLS	MDIN Set-up *	before $\overline{PLE}$ =HIGH	12	15	ns	—
49	t MPLH	MDIN Hold *	after $\overline{PLE}$ = HIGH	0	0	ns	—
50	t CPLS	CBI Set-up *	before $\overline{PLE}$ =HIGH	12	15	ns	—
51	t CPLH	CBI Hold *	after $\overline{PLE}$ = HIGH	0	0	ns	—
52	t PCPLS	PCBI Set-up *	before $\overline{PLE}$ =HIGH	12	15	ns	—
53	t PCPLH	PCBI Hold *	after $\overline{PLE}$ = HIGH	0	0	ns	—
DIAGNOSTIC SET-UP AND HOLD TIMES							
54	t CSCS	CBI Set-up *		12	15	ns	15
55	t MSCS	MDIN Set-up *	before SYNCLK=HIGH	12	15	ns	15
56	t MLSCS	MLE Set-up = HIGH		12	15	ns	15
57	t SESCS	SCLKEN Set-up = LOW		4	5	ns	15
58	t SESCH	SCLKEN Hold = LOW	after SYNCLK =HIGH	4	5	ns	15

NOTE:
"*" = Where "edge" is not specified, both HIGH and LOW edges are implied.

2552 tbl 29

MINIMUM PULSE WIDTH

Number	Parameter Name	Minimum Pulse Width Input		Conditions	Com'l. Min.	Mil. Min.	Unit	Refer to Timing Diagram Figure
59	t CLEAR	Min. $\overline{CLEAR}$ LOW time	to clear diag. registers	Data = Valid	8	10	ns	14
60	t MLE	Min. MLE HIGH time	to strobe new data	MD, CBI = Valid	5	6	ns	—
61	t PLE	Min. $\overline{PLE}$ LOW time	to strobe new data	SD = Valid	5	6	ns	—
62	t SLE	Min. SLE HIGH time	to strobe new data	SD = Valid	5	6	ns	—
63	t SYNCLK	Min. SYNCLK HIGH time	to clock in new data	SCLKEN = LOW	5	6	ns	14

2552 tbl 30

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 18

2552 tbl 31

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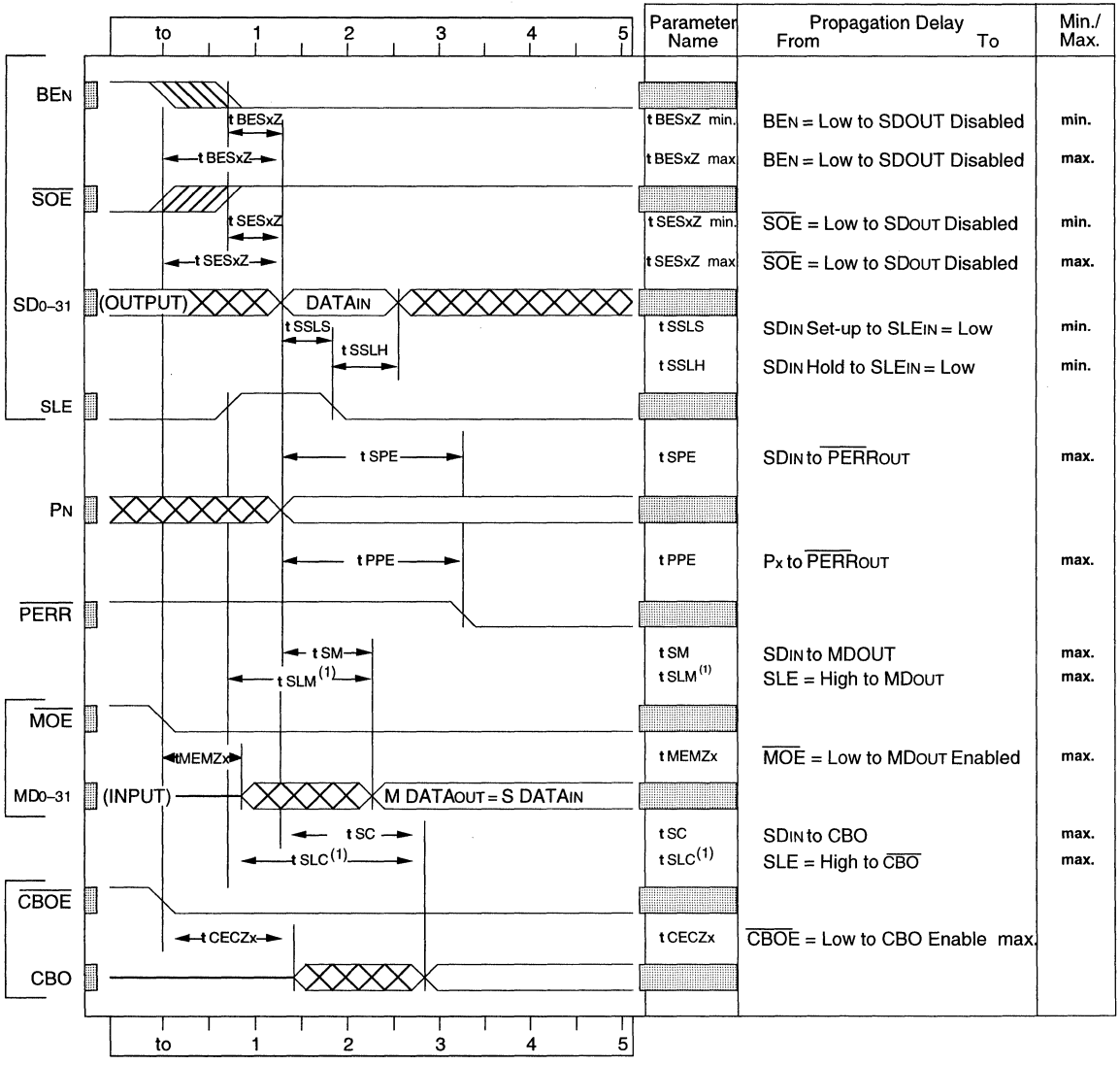
AC TIMING DIAGRAMS — 32-BIT CONFIGURATION

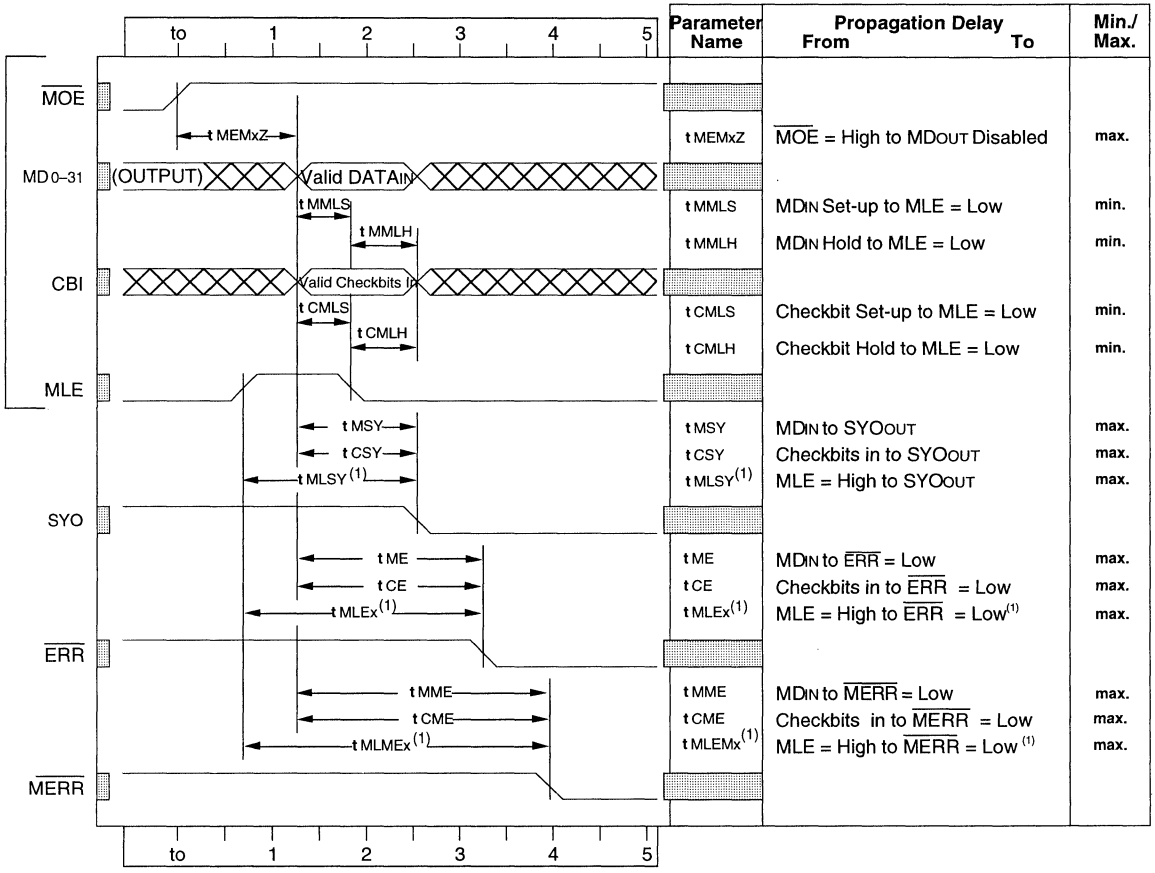


NOTE:
1. Assumes that System Data is valid at least 3ns (Com.) before SLE goes HIGH.

2552 drw 19

Figure 7. 32-Bit Generate Timing

AC TIMING DIAGRAMS — 32-BIT CONFIGURATION



Parameter Name	Propagation Delay From To	Min./ Max.
tMEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
tMMLS	MDIN Set-up to MLE = Low	min.
tMMLH	MDIN Hold to MLE = Low	min.
tCMLS	Checkbit Set-up to MLE = Low	min.
tCMLH	Checkbit Hold to MLE = Low	min.
tMSY	MDIN to SYOOUT	max.
tCSY	Checkbits in to SYOOUT	max.
tMLSY(1)	MLE = High to SYOOUT	max.
tME	MDIN to $\overline{ERR}$ = Low	max.
tCE	Checkbits in to $\overline{ERR}$ = Low	max.
tMLEx(1)	MLE = High to $\overline{ERR}$ = Low(1)	max.
tMME	MDIN to $\overline{MERR}$ = Low	max.
tCME	Checkbits in to $\overline{MERR}$ = Low	max.
tMLEMx(1)	MLE = High to $\overline{MERR}$ = Low (1)	max.

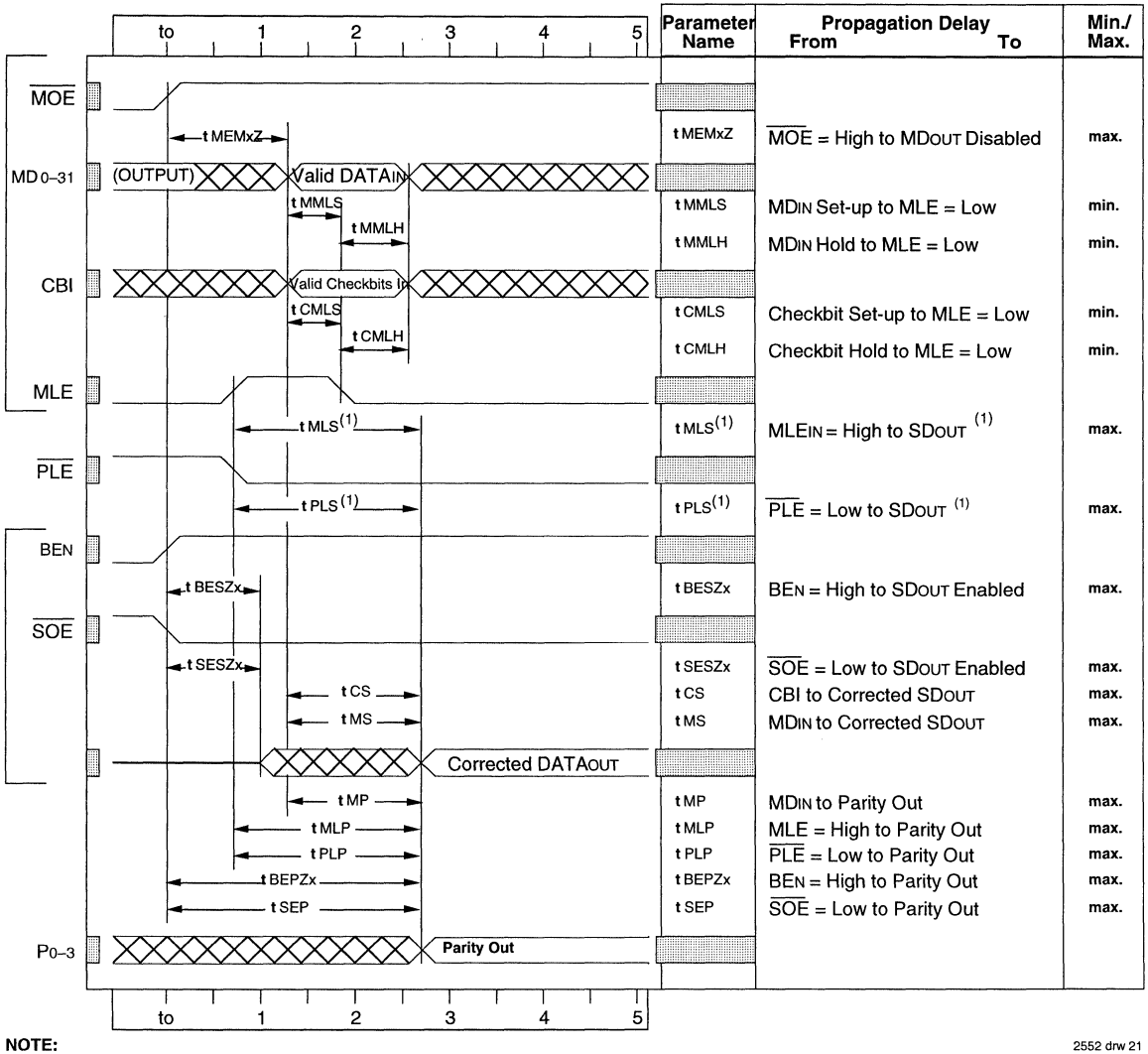
NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 3ns (Com.)/4ns (Mil,) before MLE goes HIGH.

2552 drw 20

Figure 8. 32-Bit Detect Timing

11

AC TIMING DIAGRAMS — 32-BIT CONFIGURATION



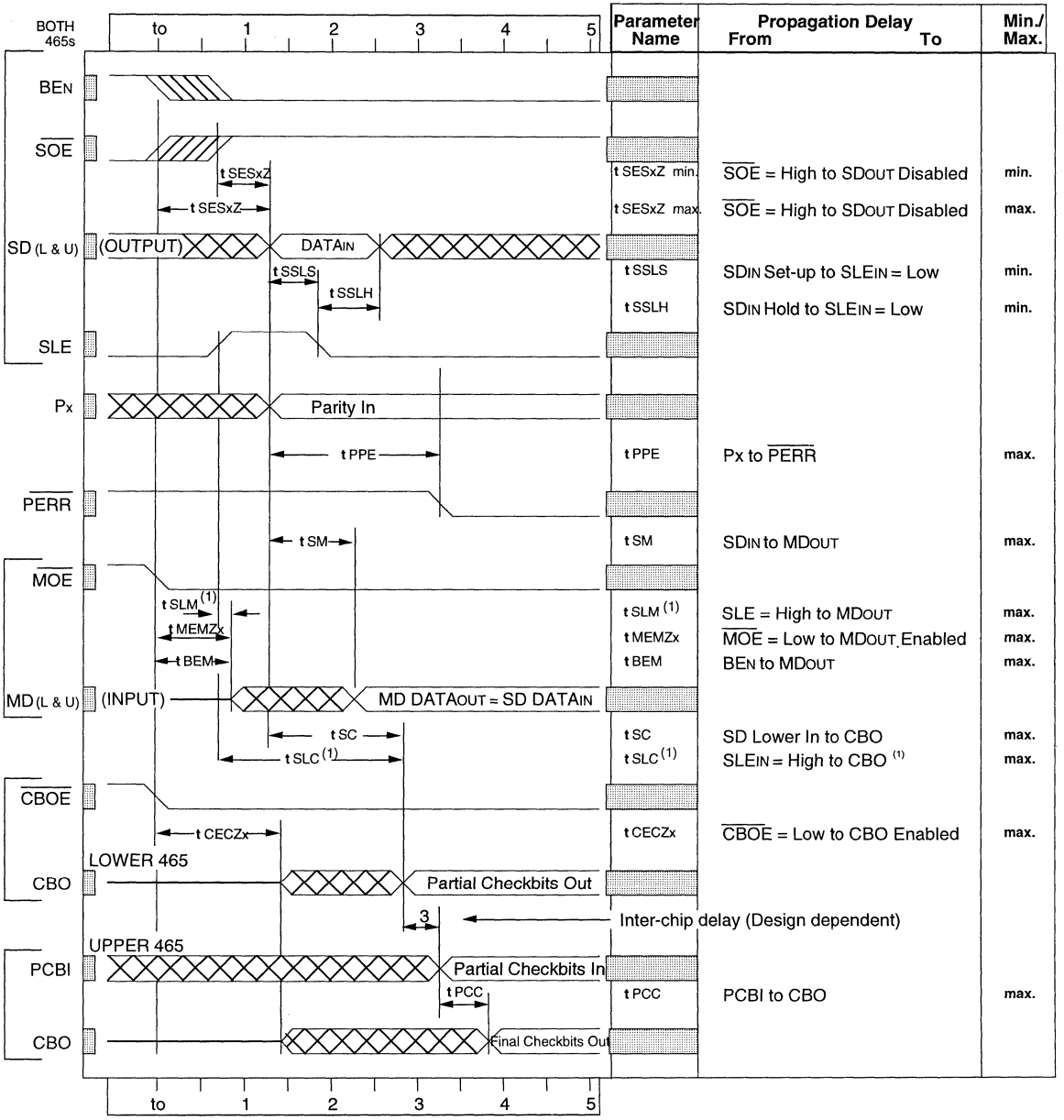
Parameter Name	Propagation Delay From To	Min./ Max.
tMEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
tMMLS	MDIN Set-up to MLE = Low	min.
tMMLH	MDIN Hold to MLE = Low	min.
tCMLS	Checkbit Set-up to MLE = Low	min.
tCMLH	Checkbit Hold to MLE = Low	min.
tMLS(1)	MLEIN = High to SDOUT (1)	max.
tPLS(1)	$\overline{PLE}$ = Low to SDOUT (1)	max.
tBESZx	BEN = High to SDOUT Enabled	max.
tSESZx	$\overline{SOE}$ = Low to SDOUT Enabled	max.
tCS	CBI to Corrected SDOUT	max.
tMS	MDIN to Corrected SDOUT	max.
tMP	MDIN to Parity Out	max.
tMLP	MLE = High to Parity Out	max.
tPLP	$\overline{PLE}$ = Low to Parity Out	max.
tBEPZx	BEN = High to Parity Out	max.
tSEP	$\overline{SOE}$ = Low to Parity Out	max.

NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 3ns (Com.)/4ns (Mil.) before MLE goes HIGH.

2552 drw 21

Figure 9. 32-Bit Correct Timing

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION



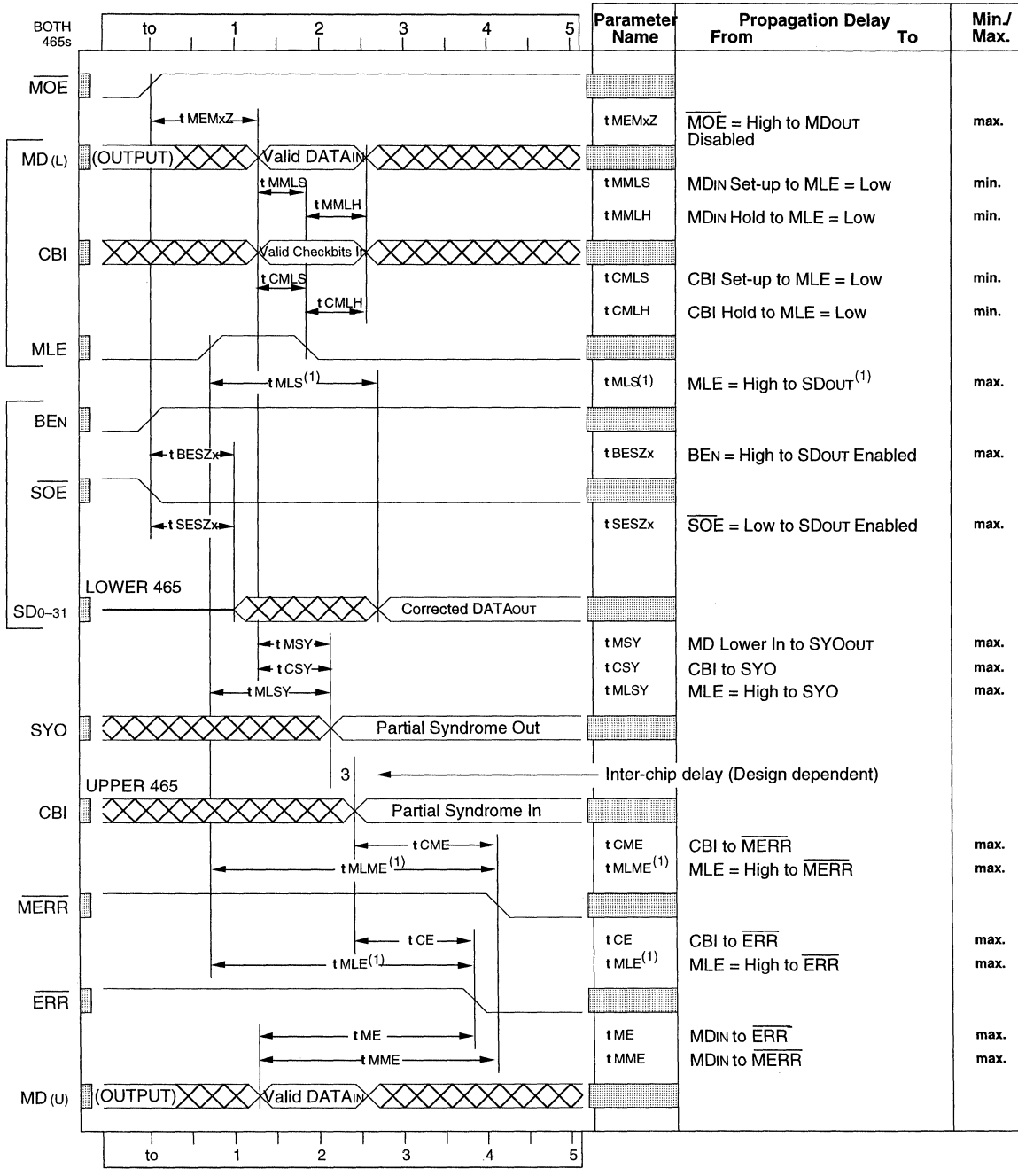
NOTE:
1. Assumes that System Data is valid at least 3ns (Com.)/4ns (Mil.) before SLE goes HIGH.

2552 drw 22

Figure 10. 64-Bit Generate Timing — (64-Bit Cascading System)

11

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION



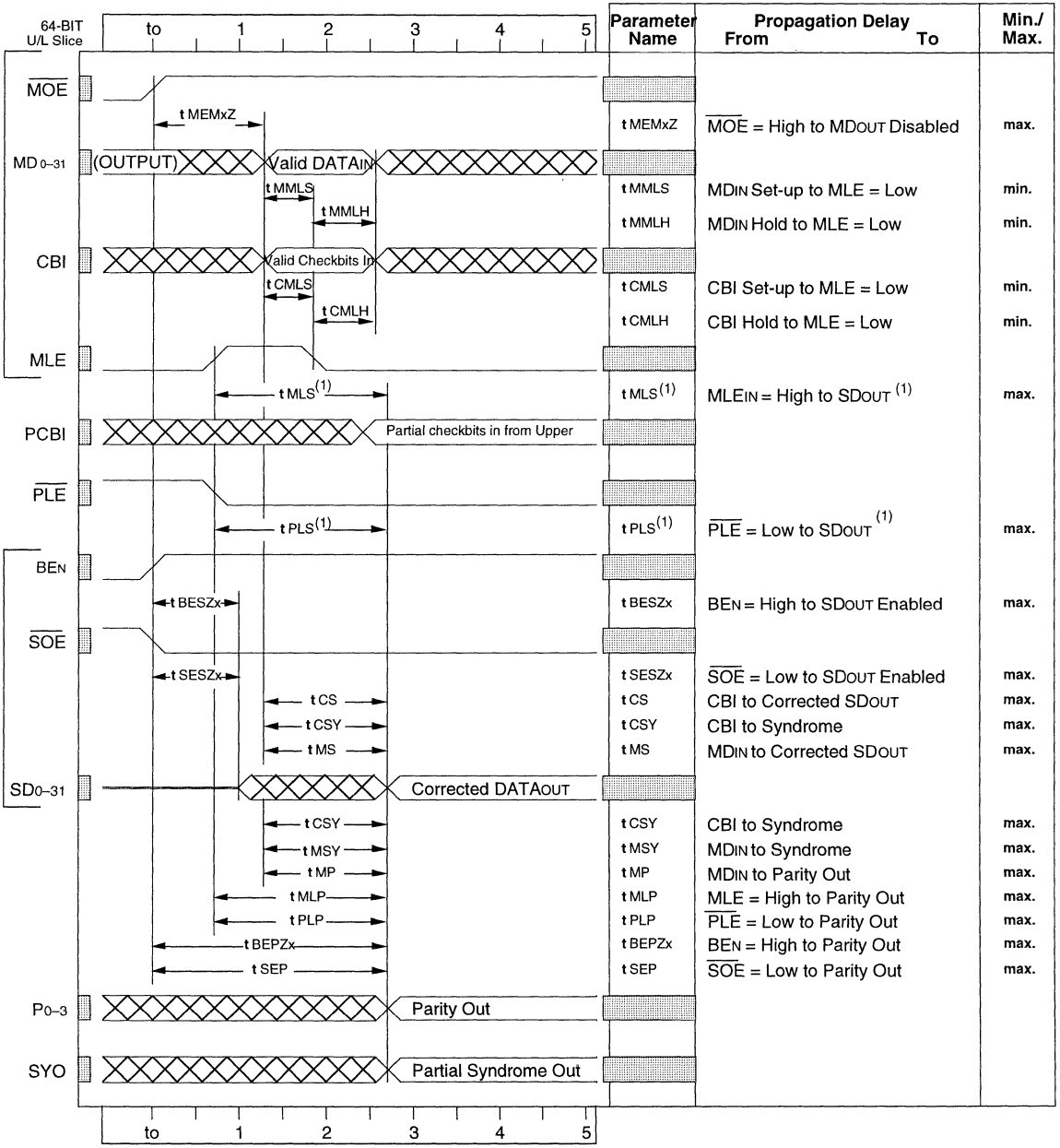
Parameter Name	Propagation Delay From To	Min./ Max.
tMEMxZ	$\overline{MOE}$ = High to MDOUT Disabled	max.
tMMLS	MDIN Set-up to MLE = Low	min.
tMMLH	MDIN Hold to MLE = Low	min.
tCMLS	CBI Set-up to MLE = Low	min.
tCMLH	CBI Hold to MLE = Low	min.
tMLS(1)	MLE = High to SDOUT(1)	max.
tBESZx	BEN = High to SDOUT Enabled	max.
tSESZx	$\overline{SOE}$ = Low to SDOUT Enabled	max.
tMSY	MD Lower In to SYOOUT	max.
tCSY	CBI to SYO	max.
tMLSY	MLE = High to SYO	max.
tCME	CBI to $\overline{MERR}$	max.
tMLME(1)	MLE = High to $\overline{MERR}$	max.
tCE	CBI to $\overline{ERR}$	max.
tMLE(1)	MLE = High to $\overline{ERR}$	max.
tME	MDIN to $\overline{ERR}$	max.
tMME	MDIN to $\overline{MERR}$	max.

NOTE:
1. Assumes that System Data is valid at least 3ns (Com.)/4ns (Mil.) before SLE goes HIGH.

2552 drw 23

Figure 11. 64-Bit Detect Timing

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION



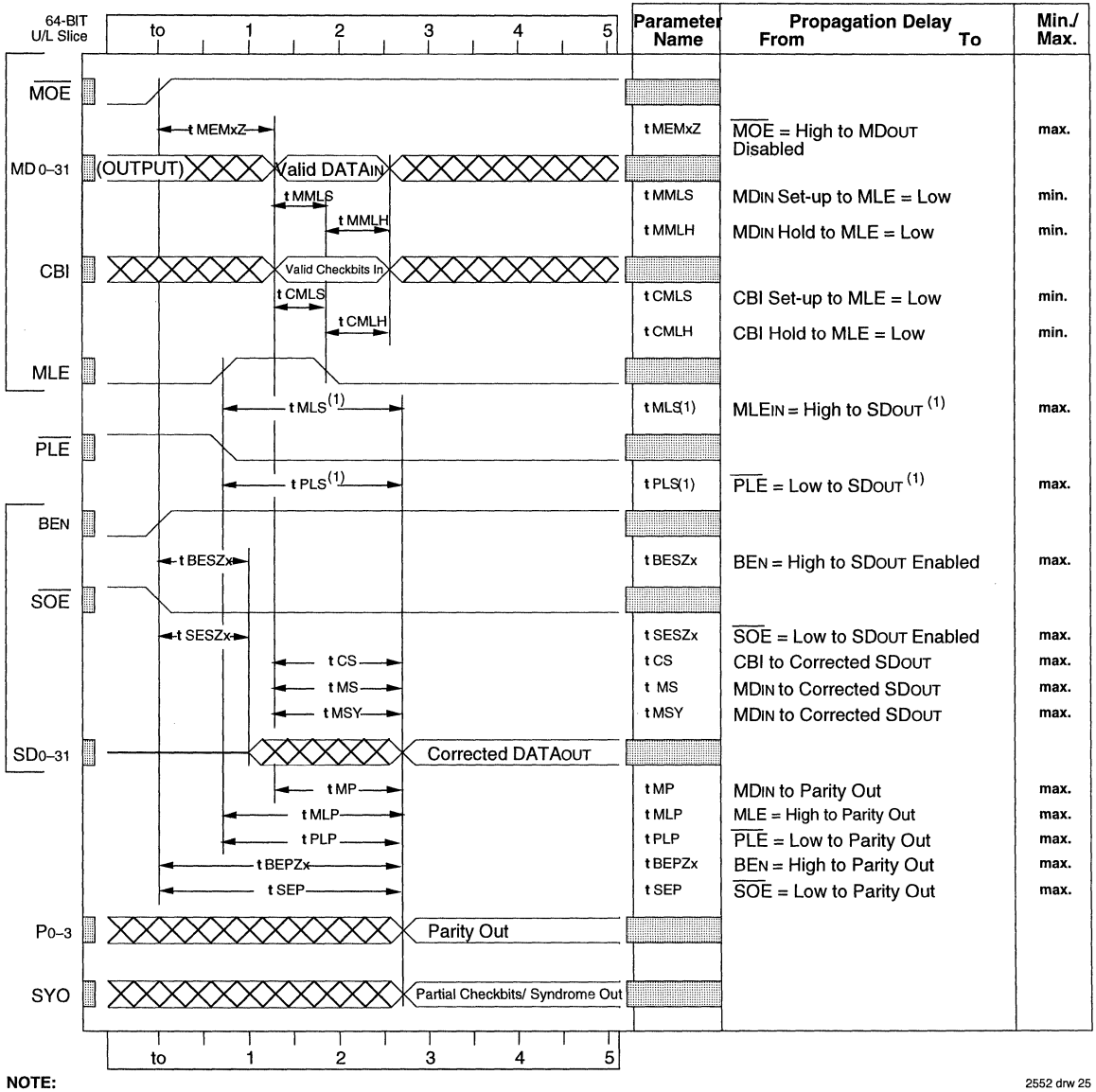
NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns (Com.) before MLE goes HIGH.

2552 drw 24

Figure 12. 64-Bit Correct Timing (Lower Slice)

11

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION

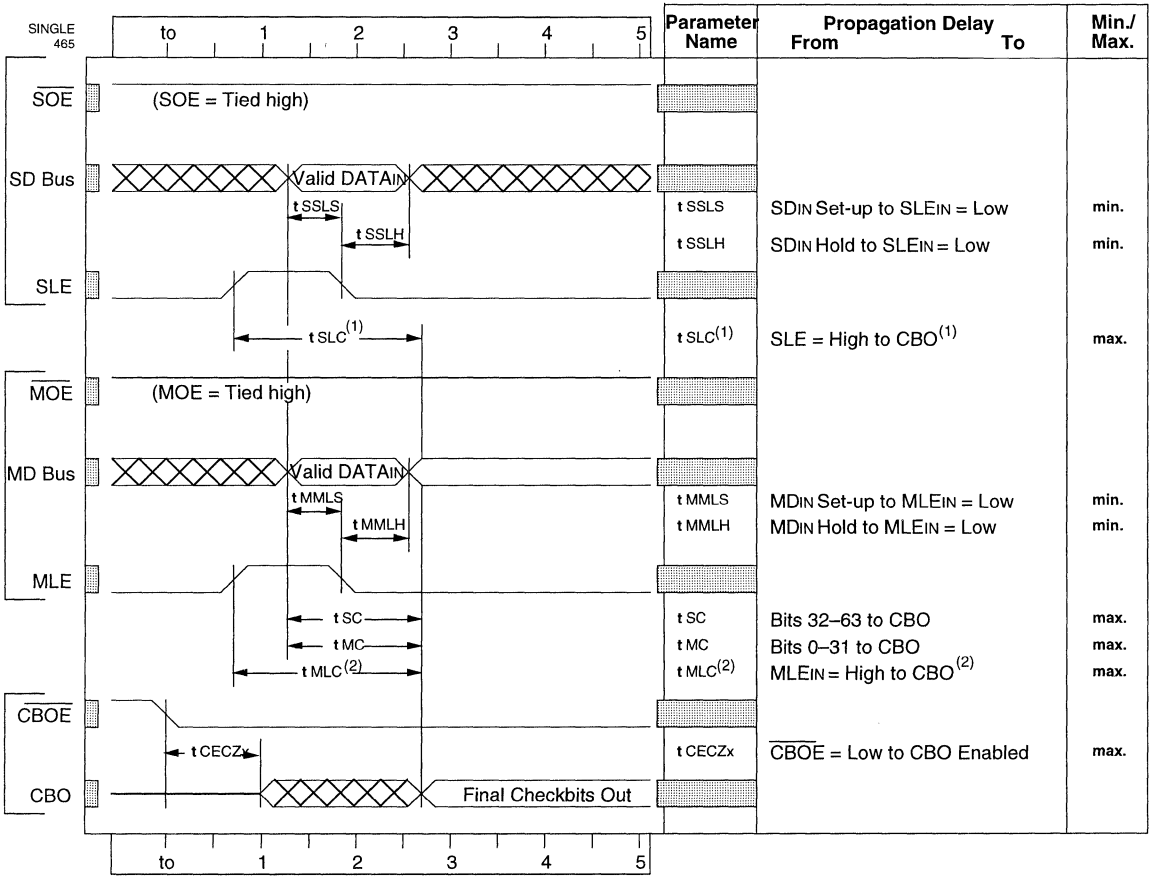


NOTE:
1. Assumes that Memory Data and Checkbits are valid at least 4ns (Com.) before MLE goes HIGH.

2552 drw 25

Figure 13. 64-Bit Correct Timing (Upper Slice)

AC TIMING DIAGRAMS — 64-BIT CONFIGURATION



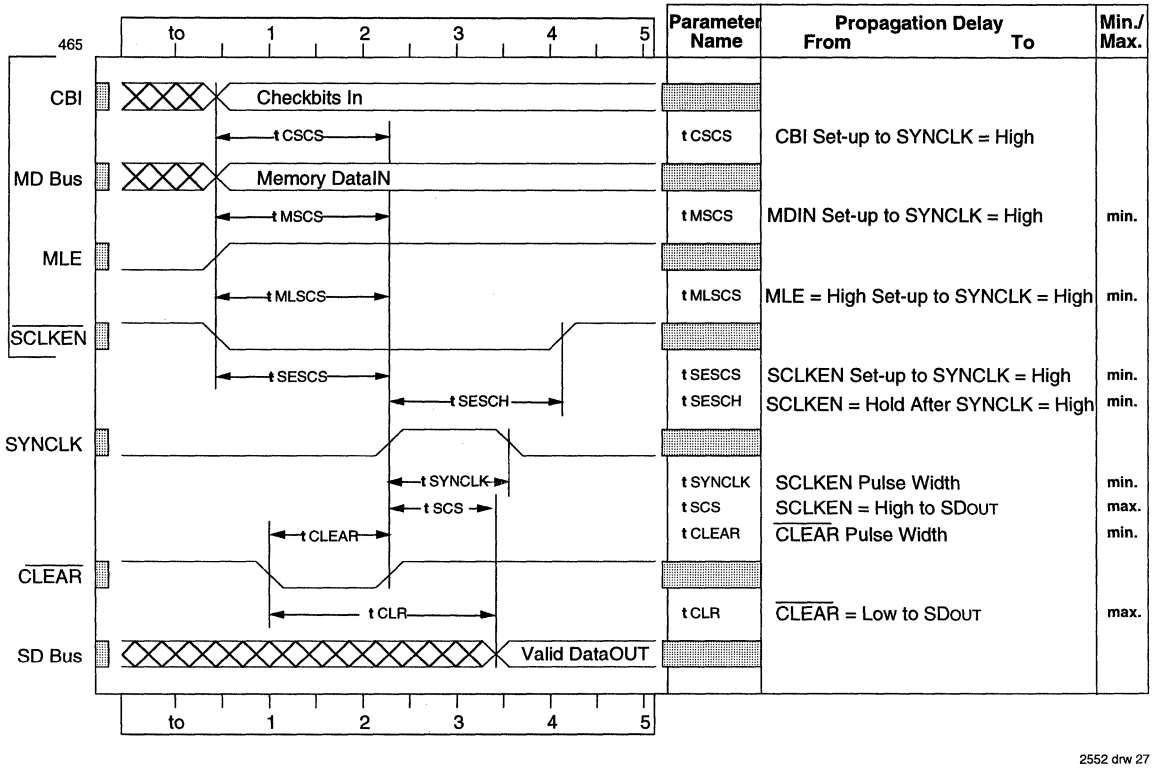
NOTE:
1. Assumes that System Data is valid at least 3ns (Com.) before SLE goes HIGH.
2. Assumes that Memory Data is valid at least 4ns (Com.) before MLE goes HIGH.

2552 drw 26

Figure 14. 64-Bit Single Chip "Generate Only" Timing

11

AC TIMING DIAGRAMS — DIAGNOSTIC TIMING

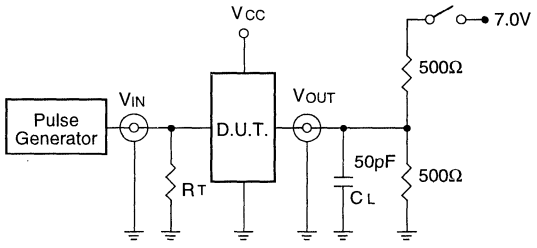


2552 drw 27

Figure 15. 32-Bit Diagnostic Timing

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2552 drw 30

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

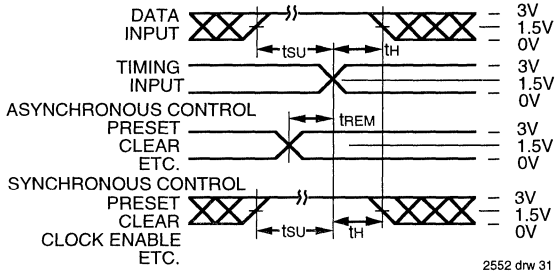
2552 tbl 35

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

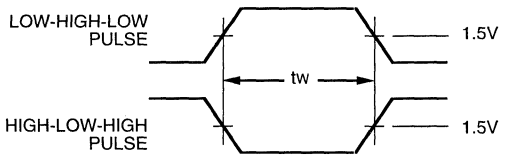
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



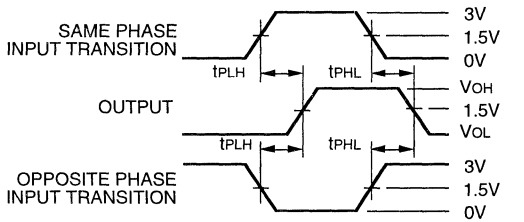
2552 drw 31

PULSE WIDTH



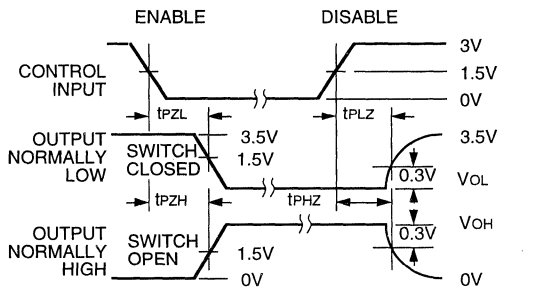
2552 drw 32

PROPAGATION DELAY



2552 drw 33

ENABLE AND DISABLE TIMES



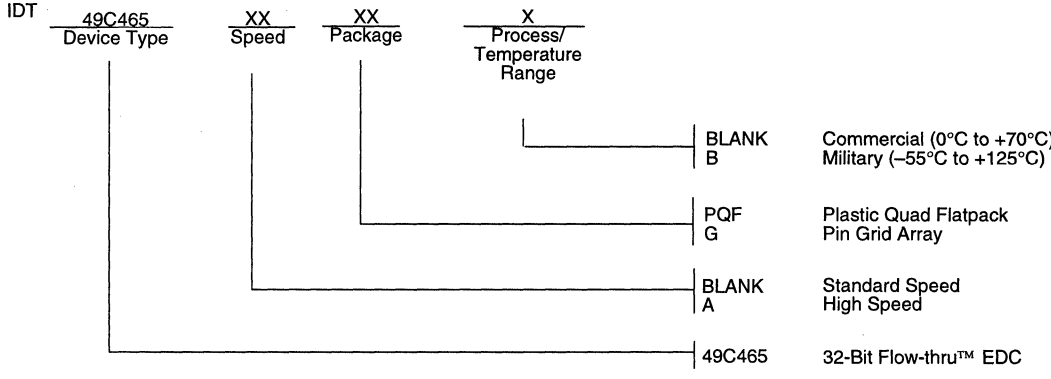
2552 drw 34

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

11

ORDERING INFORMATION



2552 drw 35

Integrated Device Technology, Inc.

64-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

IDT49C466
IDT49C466A
PRELIMINARY

FEATURES:

- 64-bit wide Flow-thruEDC™
- Separate System and Memory Data Input/Output Buses
- — Error Detect Time: 10ns
  — Error Correct Time: 15ns
- Corrects all single bit errors; Detects all double bit errors and some multiple bit errors
- Configurable 16-deep bus read/write FIFOs with flags
- Simultaneous check bit generation and correction of memory data
- Supports partial word writes on byte boundaries
- Low noise output
- Sophisticated error diagnostics and error logging
- Parity generation on system data bus
- 208-pin Pin Grid Array and Plastic Quad Flatpack

DESCRIPTION:

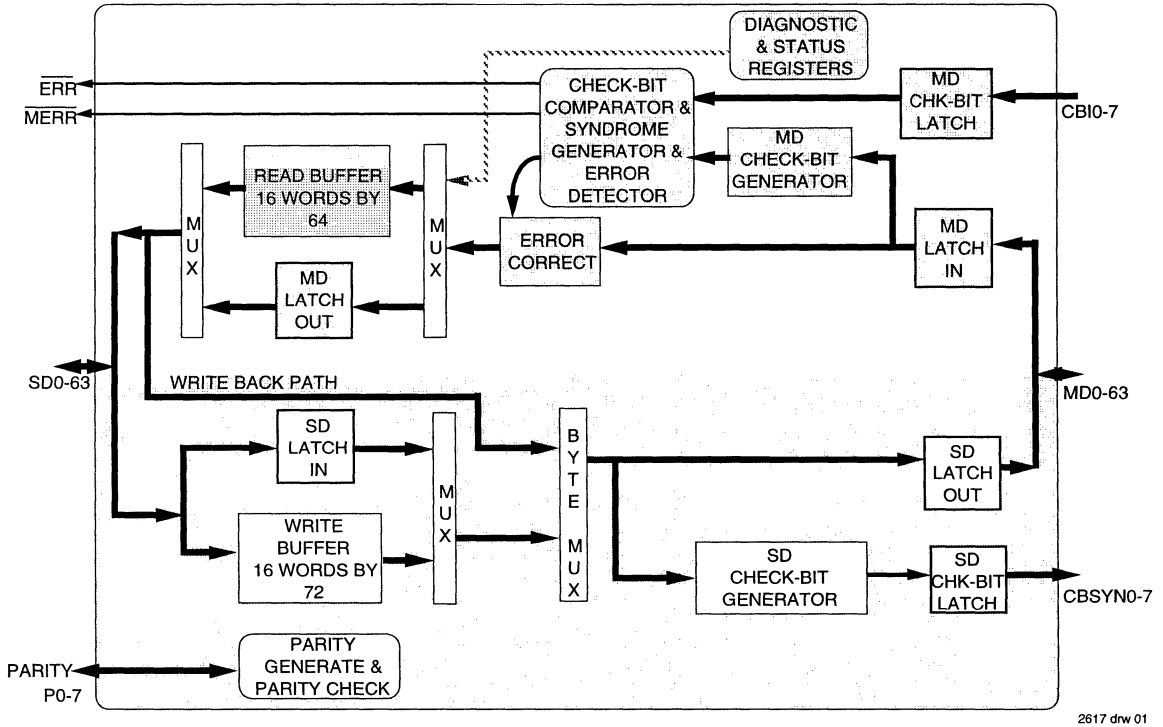
The IDT49C466/A 64-bit Flow-thruEDC is a high-speed error detection and correction unit that ensures data integrity in memory systems. The flow-thru architecture, with separate system and memory data buses, is ideally suited for pipelined memory systems.

Implementing a modified Hamming code, the IDT49C466/A corrects all single bit hard and soft errors, and detects all double bit errors. The read/write FIFOs can store up to sixteen words. FIFO full and empty flags indicate whether additional data can be written to or read from the EDC.

Check bit generation for partial word writes on byte boundaries is supported on the IDT49C466/A.

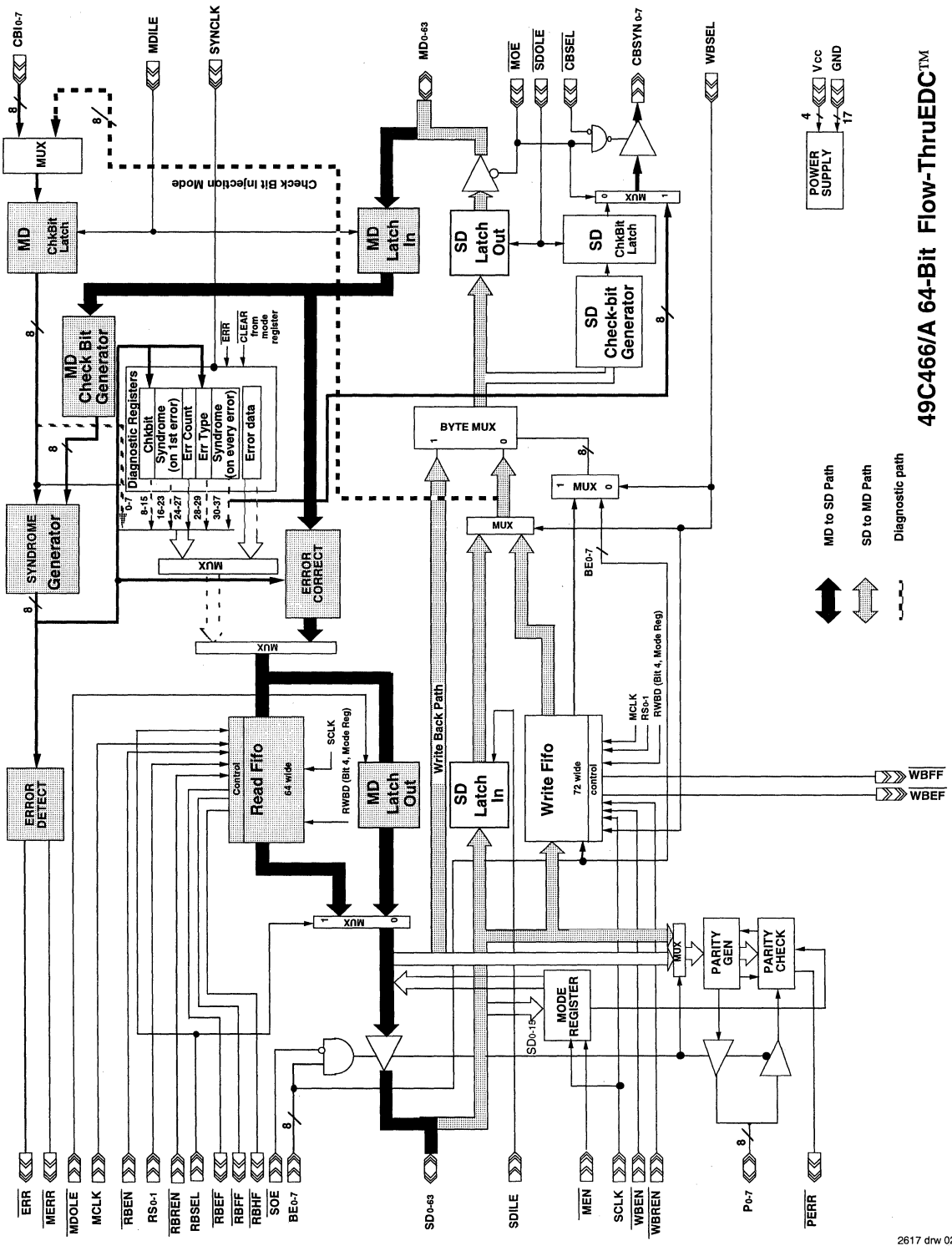
Diagnostic features include a check bit register, syndrome registers, a four bit error counter which logs up to 15 errors, and an error data register which stores the complete error data word. Parity can be generated and checked on the system bus by the IDT49C466/A.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



2617 drw 01

The IDT logo is a registered trademark and Flow-thruEDC is a trademark of Integrated Device Technology Inc.


49C466/A 64-Bit Flow-ThruEDC™
CBI0-7
MDILE
SYNCLK
MDO-63
MOE
SDOLE
CBSEL
CBSYN0-7
WBSEL
Vcc
GND
POWER SUPPLY
MUX
MD ChkBit Latch
Check Bit Injection Mode
MD Latch In
SD Latch Out
SD ChkBit Latch
SD Check-bit Generator
MD Check Bit Generator
ERR
CLEAR from mode register
Diagnostic Registers
Chkbit
Syndrome (on 1st error)
Err Count
Err Type
Syndrome (on every error)
Error data
BYTE MUX
SYNDROME Generator
ERROR CORRECT
BE0-7
MD to SD Path
SD to MD Path
Diagnostic path
Write Back Path
Read Fifo
64-wide
Control
SCLK
RWBD (Bit 4, Mode Reg)
MD Latch Out
SD Latch In
Write Fifo
72 wide
control
MCLK
RSo-1
WBFF
WBEF
ERROR DETECT
PARITY GEN
PARITY CHECK
MODE REGISTER
SDo-15
ERR
MERR
MDOLE
MCLK
RBEN
RSo-1
RBREN
RBSEL
RBEF
RBFF
RBHF
SOE
BE0-7
SDo-63
SDILE
MEN
SCLK
WBEN
WBREN
Po-7
PERR
2617 drw 02

PIN CONFIGURATION

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	MD_10	MD_8	MD_2	MD_1	$\overline{\text{MERR}}$	CBI_6	CBI_1	$\overline{\text{RBEN}}$	RBSEL	$\overline{\text{RBHF}}$	SD_2	SD_3	BE0	SD_9	SD_10	SD_12	SD_15	17
16	MD_13	MD_9	MD_6	MD_3	$\overline{\text{ERR}}$	CBI_3	CBI_2	$\overline{\text{RBREN}}$	$\overline{\text{RBEF}}$	$\overline{\text{RBFF}}$	SD_1	SD_4	SD_6	SD_8	SD_13	SD_16	SD_17	16
15	MD_17	MD_12	MD_11	MD_5	MD_4	CBI_7	CBI_4	CBI_0	GND	SD_0	P0	SD_7	P1	BE1	SD_14	SD_19	SD_21	15
14	MD_18	MD_19	MD_15	GND	MD_7	MD_0	CBI_5	GND	VCC	GND	SD_5	SD_11	GND	GND	P2	BE2	SD_20	14
13	MD_23	MD_20	MD_14	VCC										SD_18	SD_22	SD_24	SD_25	13
12	MD_25	MD_22	MD_21	MD_16										SD_23	SD_26	SD_28	SD_27	12
11	MD_27	MD_28	MD_24	GND										P3	BE3	SD_30	SD_29	11
10	MD_31	MD_30	MD_29	MD_26										SD_31	$\overline{\text{SOE}}$	SDILE	SCLK	10
9	$\overline{\text{SDOLE}}$	$\overline{\text{MOE}}$	MDILE	GND										$\overline{\text{MDOLE}}$	GND	$\overline{\text{MEN}}$	RS_0	9
8	MD_33	MD_32	MD_34	MD_35										GND	SD_33	MCLK	RS_1	8
7	MD_37	MD_36	MD_39	MD_40										SD_37	SD_34	SD_32	$\overline{\text{PERR}}$	7
6	MD_41	MD_38	MD_42	MD_45										SD_42	SD_38	P4	SD_35	6
5	MD_43	MD_44	MD_46	MD_52										GND	P5	BE4	SD_36	5
4	MD_48	MD_49	MD_50	GND	GND	MD_61	CBSYN4	VCC	GND	SD_61	GND	SD_54	SD_49	VCC	SD_43	SD_39	SD_40	4
3	MD_47	MD_51	MD_56	MD_60	MD-59	CBSYN6	GND	GND	$\overline{\text{WBEN}}$	SD_62	SD_59	SD_57	SD_53	SD_51	SD_45	SD_44	SD_41	3
2	MD_53	MD_54	MD_57	CBSYN7	CBSYN5	CBSYN2	CBSYN0	$\overline{\text{WBREN}}$	SYNCLK	$\overline{\text{WBEF}}$	SD_60	BE7	SD_55	BE6	SD_50	SD_47	BE5	2
1	MD_55	MD_58	MD_62	MD_63	CBSYN3	CBSYN1	WBSEL	$\overline{\text{CBSEL}}$	$\overline{\text{WBFF}}$	SD_63	P7	SD_58	SD_56	P6	SD_52	SD_48	SD_46	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

G208-1

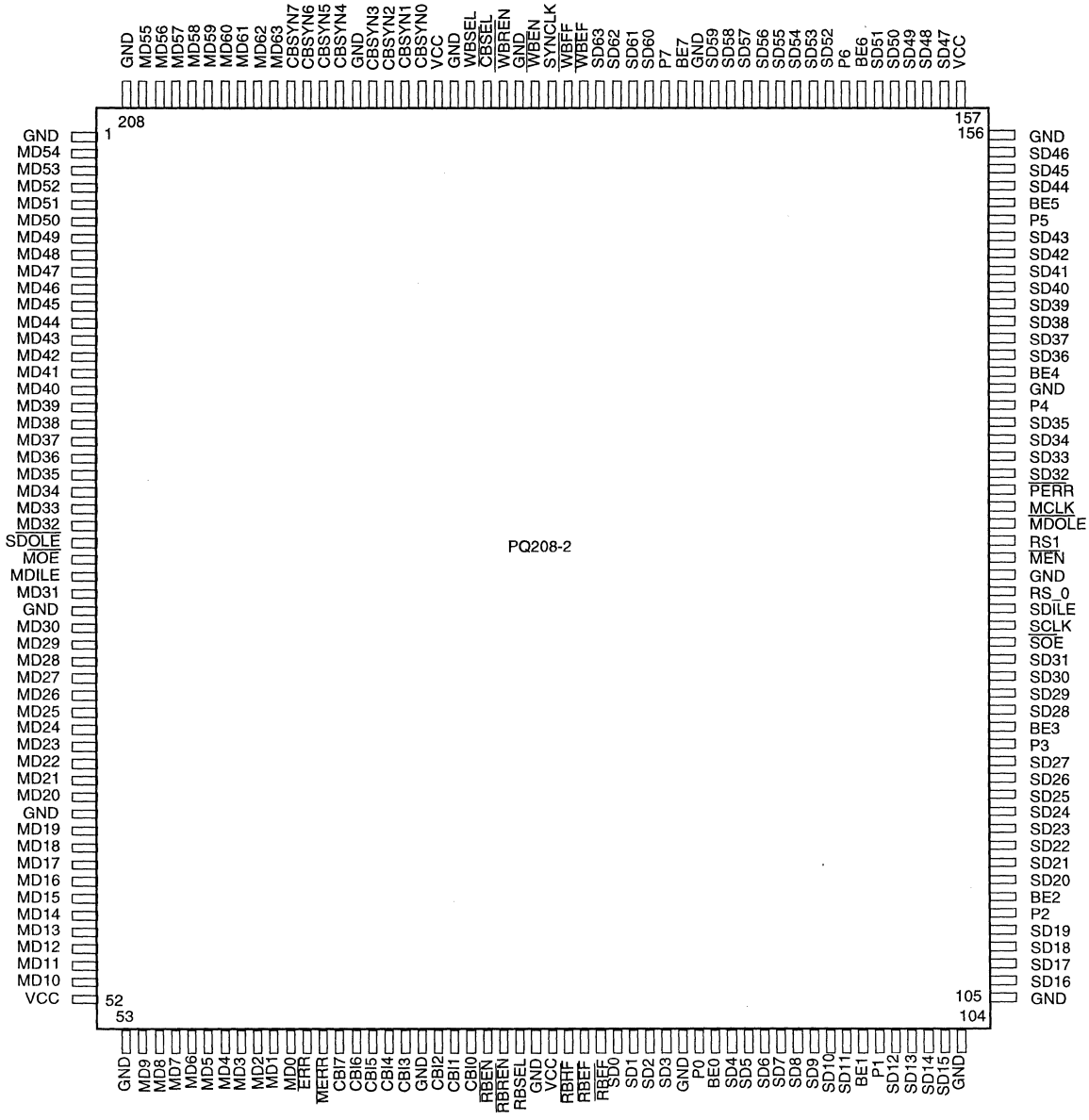
Pin 1 reference

2617 drw 03

208-pin PGA Package
Top View

11

PIN CONFIGURATION



PQFP

Top View

2617 drw 04

PIN DESCRIPTION

Pin Name	I/O	Description
SD_{0-63}	I/O	**System Data Bus:** is a bidirectional 64-bit bus interfacing to the system or CPU. When System Output Enable, $\overline{SOE}$, is HIGH or Byte Enable, BE_{0-7}, is LOW, data can be input. When System Output Enable, $\overline{SOE}$, is LOW and Byte Enable, BE_{0-7}, is HIGH, the SD bus output drivers are enabled.
MD_{0-63}	I/O	**Memory Data Bus:** is a bidirectional 64-bit bus interfacing to the memory. During a read cycle, ($\overline{MOE}$ HIGH) memory data is input for error detection and correction. Data is output on the Memory Data Bus, when $\overline{MOE}$ is LOW.
CBI_{0-7}	I	**Check Bit Inputs:** interface to the check bit memory.
$CBSYN_{0-7}$	O	**Check Bit/Syndrome Output:** When $\overline{MOE}$ is LOW the generated check bits are output. When CBSEL is HIGH and $\overline{MOE}$ is HIGH, the syndrome bits are output. The bus is tristated when $\overline{MOE}$ = 1 and CBSEL = 0.
P_{0-7}	I/O	**Parity for bytes 0 to 7:** These pins are parity inputs when the corresponding Byte Enable (BE) is LOW or $\overline{SOE}$ is HIGH, and are used to generate the parity error signal ($\overline{PERR}$). These pins are outputs when the corresponding Byte Enable (BE) is HIGH and $\overline{SOE}$ is LOW.
Control Inputs		
$\overline{SOE}$	I	**System Output Enable:** enables system data bus output drivers if the corresponding Byte Enable (BE_{0-7}) is HIGH.
BE_{0-7}	I	**Byte Enable:** is used along with $\overline{SOE}$, to enable the System Data outputs for a particular byte. For example, if BE_1 is HIGH, the System data outputs for byte 1 (SD_{8-15}) are enabled. The BE_{0-7} pins also control the byte mux. If a particular BE is HIGH during a memory read cycle, that byte is fed back to the memory data bus. This is used during partial word write operations and writing corrected data back to memory.
$\overline{MOE}$	I	**Memory Output Enable:** when LOW, enables the output buffers of the memory data bus (MD) and CBSYN bus. It also controls the CBSYN mux. When LOW, checkbits are selected, when HIGH, syndrome is selected.
MDILE	I	**Memory Data Input Latch Enable:** on the HIGH-to-LOW transition, latches MD and CBI in MD input latch and MD check bit latch respectively. The latches are transparent when MDILE is HIGH.
$\overline{MDOLE}$	I	**Memory Data Output Latch Enable:** latches data in the MD output latch on the LOW-to-HIGH transition of $\overline{MDOLE}$. When $\overline{MDOLE}$ is LOW, the MD output latch is transparent.
$\overline{SDOLE}$	I	**System Data Output Latch Enable:** latches data in the SD output latch and the SD checkbit latch on the LOW-to-HIGH transition of $\overline{SDOLE}$. The latch is transparent when $\overline{SDOLE}$ is LOW.
SDILE	I	**System Data Input Latch Enable:** latches SD in the SD input latch on the HIGH-to-LOW transition. When SDILE is HIGH, the SD input latch is transparent.
WBSEL	I	**Write FIFO Select:** when HIGH, the write FIFO is selected. When WBSEL is LOW, the SD input latch is selected.
$\overline{WBEN}$	I	**Write FIFO Enable:** when LOW, allows SD data to be written to the write FIFO on the SCLK rising edge.
$\overline{WBREN}$	I	**Write FIFO Read Enable:** when LOW, allows data to be read from the the write FIFO on MCLK rising edge.
RS_{0-1}	I	**Reset and Select pins** (read and write FIFO FIFOs) RS_1 RS_0 Function 0 0 Reset 16-deep FIFO or first 8-deep FIFO 0 1 Reset second 8-deep FIFO 1 0 Select 16-deep FIFO or first 8-deep FIFO 1 1 Select second 8-deep FIFO

2617 tbl 01

11

PIN DESCRIPTION (Continued)

Pin Name	I/O	Description
RBSEL	I	**Read FIFO Select:** when HIGH, read FIFO is selected (data goes through read FIFO, not MD output latch). When LOW, the MD output latch is selected.
$\overline{\text{RBEN}}$	I	**Read FIFO Enable:** when LOW, allows data to be written into the read FIFO on the LOW-to-HIGH transition of the memory clock.
$\overline{\text{RBREN}}$	I	**Read FIFO Enable:** when LOW, allows data to be read from the read FIFO on the LOW-to-HIGH transition of SCLK
$\overline{\text{CBSEL}}$	I	**Checkbit Syndrome Output Enable:** Controls the CBSYN output buffer.When HIGH, the buffer is enabled. When CBSEL is LOW, $\overline{\text{MOE}}$ controls the buffer.
$\overline{\text{MEN}}$	I	**Mode Enable Input:** when LOW, $SD_{0\text{-}15}$ is loaded into the EDC mode register on the LOW-to-HIGH transition of the SCLK. This pin must be held LOW for the entire SCLK HIGH period, as shown in Figure 4.
Clock Inputs		
MCLK	I	**Memory Clock:** on the LOW-to-HIGH transition of MCLK, memory data is written to the read FIFO when $\overline{\text{RBEN}}$ is LOW. Data is read from the write FIFO when $\overline{\text{WBREN}}$ is LOW, on the LOW-to-HIGH transition of MCLK.
SCLK	I	**System Clock:** on the LOW-to-HIGH transition of the SCLK, data is read from the read FIFO when $\overline{\text{RBREN}}$ is LOW. Data on the system data bus is written into the write FIFO when $\overline{\text{WBEN}}$ is LOW on the LOW-to-HIGH transition of SCLK. Clocks data into mode register when $\overline{\text{MEN}}$ is LOW.
SYNCLK	I	**Syndrome Clock:** Used to load diagnostic registers. When an error occurs, Error Counter is incremented on the rising SYNCLK edge (up to 15 errors). On the first error after a diagnostic reset, SYNCLK rising edge clocks data into Check Bit, Syndrome, Error Type and Error Data registers. One of the syndrome registers has new data clocked in on every SYNCLK rising edge.
Status Outputs		
$\overline{\text{WBEF}}$	O	**Write FIFO Empty Flag:** when LOW, indicates that the write FIFO is empty. After a reset, the $\overline{\text{WBEF}}$ goes LOW.
$\overline{\text{WBFF}}$	O	**Write FIFO Full Flag:** when LOW, indicates that the write FIFO is full. After a reset, $\overline{\text{WBFF}}$ goes HIGH.
$\overline{\text{RBEF}}$	O	**Read FIFO Empty Flag:** when LOW, indicates that the read FIFO is empty. After a reset, the $\overline{\text{RBEF}}$ goes LOW.
$\overline{\text{RBHF}}$	O	**Read FIFO Half-full Flag:** when LOW, indicates that there are eight or more data words (in the 16-deep configuration) or four or more data words (in the dual 8-deep configuration) in the read FIFO. The flag will return HIGH when less than eight (or four) data words are in the FIFO.
$\overline{\text{RBFF}}$	O	**Read FIFO Full Flag:** when LOW, indicates that the read FIFO is full. After a reset, $\overline{\text{RBFF}}$ goes HIGH.
$\overline{\text{ERR}}$	O	**Error Flag:** when $\overline{\text{ERR}}$ is LOW, a data error is indicated. The $\overline{\text{ERR}}$ is not latched internally.
$\overline{\text{MERR}}$	O	**Multiple Error Flag:** when $\overline{\text{MERR}}$ is LOW, a multiple data error is indicated. The $\overline{\text{MERR}}$ is not latched internally.
$\overline{\text{PERR}}$	O	**Parity Error Flag:** when LOW, indicates a parity error on the system data bus input.
Power Supply		
V_{CC}	P	Power Supply Voltage.
GND	P	Ground.

2617 tbl 02

DETAILED DESCRIPTION —

64-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART(1, 2)

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2617 tbl 03

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2617 tbl 04

Generated Checkbits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)									X	X	X	X	X	X	X	X

2617 tbl 05

Generated Checkbits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

2617 tbl 06

NOTES:

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit CB0 is the Exclusive-OR function of the 64 data input bits marked with an X.
2. The checkbit is generated as either an XOR or an XNOR of the 64 data bits noted by an "X" in the table.

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DETAILED DESCRIPTION —

64-BIT SYNDROME DECODE TO BIT-IN-ERROR(1)

				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	Syndrome			S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	Bits			S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																
0	0	0	0	0	*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

NOTES:

2617 tbl 07

1. The table indicates the decoding of the eight syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected. The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single data bit-in-error
   T = Two errors detected
   M = Three or more detected
   C# = The number of the single checkbits in error

IDT49C466 OPERATION

The EDC is involved in two types of operation — memory reads and memory writes. With the IDT49C466, both these can be accomplished by utilizing either of two possible data paths — one incorporating the FIFO and the other without the FIFO. These operations are treated separately below.

Memory Write

The involvement of the EDC in this type of operation is relatively minimal since it does not call for any error checking. It only generates the check bits associated with each 64-bit wide data word. The EDC can be in generate-detect or normal mode for this operation.

When a write operation is performed, it must be ensured that the SD output buffer (enabled by $\overline{SOE}$ and BE_{0-7}) is disabled so that no attempt is made to simultaneously transfer read data onto the System Data (SD) Bus.

When the write FIFO (WFIFO) is bypassed (WBSEL LOW), data passes through the SD Latch In. To latch data, the SDILE signal should be pulled LOW. The special case of a partial word write or byte merge is discussed later. Here it is assumed that all 64 bits are being written. Consequently, BE_{0-7} must all be LOW.

The data is fed to the SD Checkbit generator where appropriate checkbits are generated. Both system data and the generated checkbits can be latched by pulling the $\overline{SDOLE}$ signal HIGH. Asserting $\overline{MOE}$ enables the MD output buffer and data is output to the Memory Data (MD) bus. $\overline{CBSEL}$ (=1) or $\overline{MOE}$(=0) need to be asserted to enable the CBSYN output buffer and output checkbits on $CBSYN_{0-7}$.

When the write FIFO is selected (WBSEL = 1), instead of asserting SDILE, $\overline{WBEN}$ is asserted and data is clocked into the write FIFO on the rising edge of SCLK. $\overline{WBFF}$ is asserted when the WFIFO is full and this inhibits further write attempts (see section on "Clock Skew" and "R/W FIFO Operation at Boundaries") to the WFIFO. When $\overline{WBREN}$ is asserted, data can be clocked out of the write FIFO on the rising edge of MCLK. $\overline{WBEF}$ is asserted when the WFIFO is empty and this inhibits further read attempts (see section on "Clock Skew") from the WFIFO.

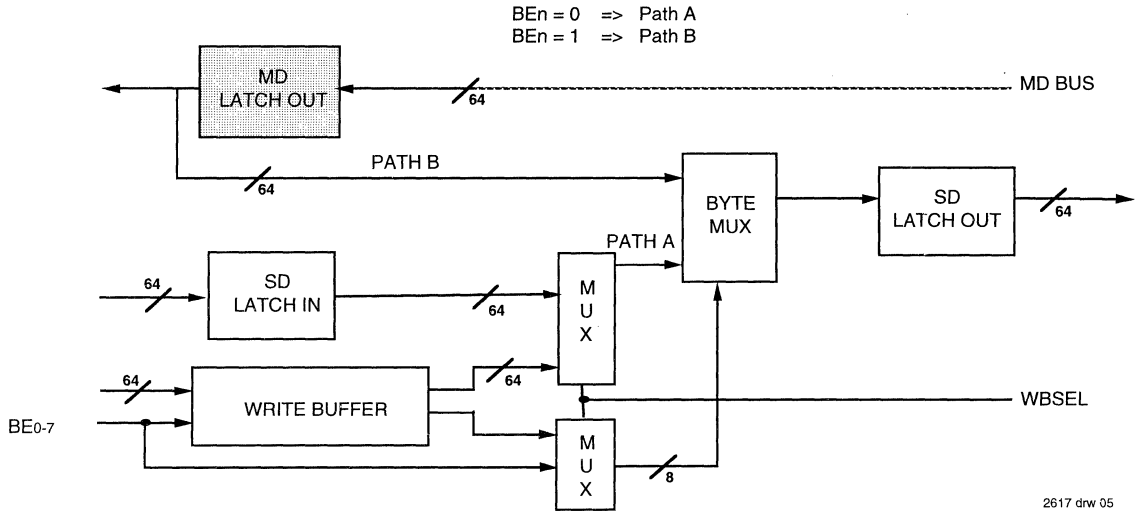

Figure 1. Byte Merge

Memory Read

During a memory read, data and the corresponding input checkbits are read from the MD bus and CBI0-7, respectively. The memory and checkbit data may both be latched as they come in (MD Latch In and MD Checkbit latch) by the MDILE signal. Memory data is sent to the MD checkbit generator (where checkbits corresponding to the input data are generated) and to the error correct circuitry. The generated checkbits are X-ORed with the input checkbits to produce the syndrome word. This is sent to the error correction circuitry which generates the corrected data (normal mode). The corrected data is output to the SD bus via either of two data paths. When RBSEL is LOW, data flows through MD Latch Out. Pulling $\overline{\text{MDOLE}}$ HIGH latches this data. The output buffer is enabled by asserting $\overline{\text{SOE}}$ (=0) and BE0-7 (=1). Corrected data can be written back to memory by enabling the MD output buffer. In order to ensure selection of the write back path (Path B in figure 1) at the byte mux, BEO-7 should be all 1's while WBSEL = 0. If WBSEL = 1, buffered BEO-7 from the output of the write FIFO controls the byte mux.

If the read FIFO (RFIFO) is selected (RBSEL HIGH), data is clocked into the FIFO (Read_FIFO Write) when $\overline{\text{RBEN}}$ is LOW, on the rising edge of MCLK. $\overline{\text{RBFF}}$ is asserted when the RFIFO is full and this inhibits further write attempts to the RFIFO (see section on "Clock Skew" and "R/W FIFO operation at Boundaries"). Data is clocked out of the FIFO (Read_FIFO Read) when $\overline{\text{RBREN}}$ is LOW on the rising edge of SCLK. $\overline{\text{RBEF}}$ is asserted when the RFIFO is empty and this inhibits further read attempts (see section on "Clock Skew") from the RFIFO.

Clock Skew

A skew between the read and write clocks, as specified by tskew, is recommended. This specification is not a stringent one, in the manner of setup and hold times, but is important in preempting latencies at FIFO boundaries. For example – When a word is written to an empty FIFO, there is a finite delay before the FIFO is recognized as no longer being empty and hence allowing a read from the same FIFO. Similarly when a word is read from a full FIFO, there is a delay before a write can successfully be attempted. The tskew specification accounts for these cases. During cycles other than on full/empty FIFO boundaries, the clock skew is not required and the device functions correctly even when the reads and writes occur simultaneously. If the tskew specification is ignored and SCLK and MCLK were permanently tied together, there is an extra cycle latency in the cases mentioned above. Clock skew violation is illustrated in Figure 13.

FIFO Write Latency

The first data written to either of the (read or write) FIFOs, after the FIFO is reset, suffers a single clock latency. Data that is set-up with respect to the first clock is ignored and the data that is set-up with respect to the second clock edge after the reset, is stored as the first data in the FIFO (Refer to Figures 9 and 10). The empty-flag is deasserted after this second clock edge and 15 more data words (in a 16 deep configuration) can be written to the FIFO after this.

The latency can be reduced or eliminated by providing a "dummy" or "set-up" clock edge before the actual write to the FIFO. The dummy write clock can be provided any time after reset and before the next buffer write operation takes place. The latency described here (shown in Figures 10 and 13) occurs only after a FIFO reset. In other cases where the FIFO becomes empty there is no latency.

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R/W FIFO Operation At Boundaries

In the 49C466 the write pointer is incremented on every FIFO write. Similarly the read pointer is incremented on every FIFO read. In most cases on a FIFO read, the last data read remains at the output of the FIFO, until the read pointer is further incremented. On the last (the write that fills the FIFO) FIFO write after the FIFO read, however, this last read data is overwritten by the 16th write following the empty condition and consequently the data at the FIFO output is liable to change. The situation is depicted in the diagram below.

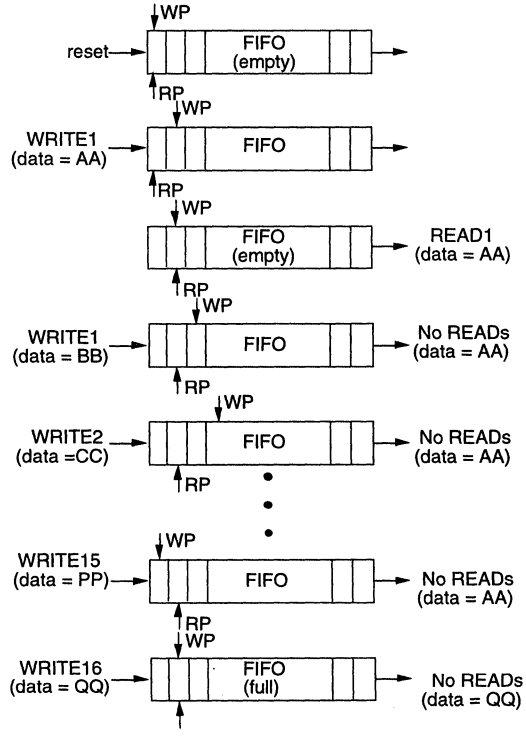

Figure 2. R/W FIFO Operation

The diagram in figure 2 progresses from the FIFO initialization(reset) through a sequence of write operations. After the first write, a read is executed which establishes the data at the FIFO output(AA). On the last write to the FIFO(the write that fills the FIFO), the location of the last read data is overwritten and the FIFO output changes from AA to the data just written, namely QQ.

This operation needs to be taken into account in the design of the system. In case of a burst operation where FIFO data is output at a much slower rate than the rate at which data is input and the full flag is expected to inhibit further writes, the user cannot expect the FIFO output to remain static through the 16th write of the burst. If this is a requisite to the design, the FIFO output should be latched. In the case of the write FIFO this can be accomplished on-chip by latching the FIFO output in the SD output latch. For the read FIFO, the FIFO output must be latched externally to accomplish the same thing, since there is no latch on-chip following the FIFO. If this cannot be done and the situation described above is expected to occur in normal operation, the write must be inhibited one cycle before the FIFO becomes full.

Partial Word Write/Byte Merge

Writing a word shorter than 64 bits to memory is treated as a special case. The checkbits generated for a data word shorter than 64 bits and written to a particular memory location differ from the checkbits that would be generated by the entire 64-bit data word at the same location. Hence, the byte merge operation requires reading of the contents of the memory location to be written to, merging the byte/bytes being written (from SD side) with the other component bytes previously at that memory location (from MD side), generating a checkbit word for this composite word and writing both the composite data word and the generated checkbits to memory. The BEn bits supplied by the user determine the bytes that come from SD and those that come from MD, as illustrated in Figure 1.

EDC Modes

The IDT49C466 has 5 modes of operation. Refer to table below for a description of the modes.

The **Error Data Output** mode is useful for memory initialization as described below. In **Checkbit Injection mode**, the MD Checkbit Latch is loaded with data from the System Bus. This serves to verify the functioning of the EDC. Any discrepancy between the injected checkbits and generated checkbits should result in assertion of the $\overline{ERR}$, $\overline{MERR}$ signals.

These modes and certain other features such as clear, buffer configuration, etc., can be selected by appropriately loading the Mode Register. The Mode Register can be written to by asserting $\overline{MEN}$. Then $SD_{0\text{-}15}$ is clocked into the mode register on the rising edge of SCLK.

MODE REGISTER CONFIGURATION

15 — 7	6	5	4	3	2 — 0
UNUSED	RMODE	PSEL	RWBD	CLEAR	EDCM0-2

EDCM2	EDCM1	EDCM0	OPERATION
0	0	0	ERROR-DATA OUTPUT MODE
0	0	1	DIAGNOSTIC-OUTPUT MODE
0	1	0	GENERATE-DETECT MODE
0	1	1	NORMAL MODE
1	0	0	CHECKBIT-INJECTION MODE

RMODE	OPERATION
0	NOP
1	READ MODE REGISTER ON SD BUS

RWBD	OPERATION
0	DUAL FIFOS (8)
1	SINGLE FIFO (16)

CLEAR	OPERATION
0	NOP
1	CLEAR ALL DIAGNOSTIC REGISTERS

PSEL	OPERATION
0	EVEN PARITY
1	ODD PARITY

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OPERATING MODE DESCRIPTION

Mode	Description
MODE 0	**Error-Data Output Mode:** This mode allows the uncorrected data captured from an error event by the Error-Data Register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by setting the mode register "clear"-bit.
MODE 1	**Diagnostic-Output Mode:** In this mode, contents of latch and five internal registers are read by the system for diagnostic and error logging purposes. Internal data paths allow output from the CBI LATCH to be read directly by the system bus for diagnostic purposes. The contents of the internal diagnostic checkbit register, syndrome registers, error count register and error-type register are also output on the SD bus.
MODE 2	**Generate-Detect Mode:** (Detect-Only) The EDC performs checkbit generation during a memory write, and performs error detection only during a memory read.
MODE 3	**Normal Mode:** The EDC performs checkbit generation during memory writes and error detection and correction during memory reads.
MODE 4	**Checkbit-Injection Mode:** In this mode, the checkbit latch is loaded with desired 8-bit data from the SD bus.This eight bit data passes through SD Latch in or write FIFO to the MD check bit latch. By inserting various checkbit values, correct functioning of the EDC can be verified "on-board". The rest of the operation is similar to regular memory reads. The EDC compares the injected checkbits against the internally generated checkbits. Any discrepancy in the injected checkbits and the internally generated checkbits will cause the $\overline{ERR}$ / $\overline{MERR}$ to go LOW.

2617 tbl 08

Memory Initialization

Memory initialization involves clearing all memory data locations and writing the corresponding checkbits (checkbits corresponding to all zero data = $0C) to checkbit memory. This can be done using the 49C466 to first create an "all-zero-data" source. This is done by setting the CLEAR bit in the mode register. This clears all diagnostic registers. Then this data can be written back to memory in the Diagnostic-output (Mode1) or the Error-Data output (Mode 0) modes. In order to wrap the all-zero data back to the MD bus, BE0-7 should be high and WBSEL =0.

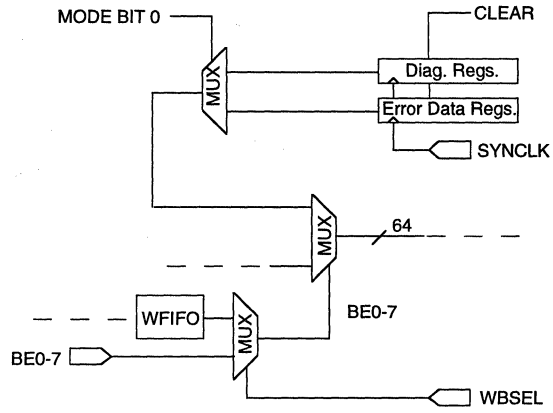
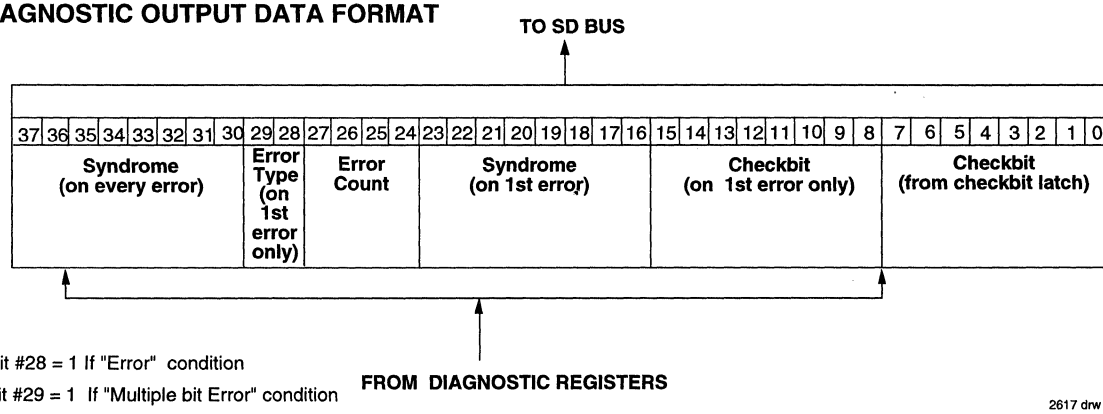


Fig 3. Memory Initialization using Diagnostic Output/Error Data Output Mode

DIAGNOSTIC OUTPUT DATA FORMAT



* Bit #28 = 1 If "Error" condition
Bit #29 = 1 If "Multiple bit Error" condition

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Diagnostics

The diagnostic ability of the IDT49C466 rests on a set of 6 registers that provide error logging information. These include the checkbit register, error count register, error type register, 2 syndrome registers and the error data register. Data is clocked into each of these registers by SYNCLK. The error data register, checkbit register, error type register and one of the syndrome registers are reloaded only in the case of the first error after a clear. The other syndrome register and the error count register are reloaded on every error condition SYNCLK edge. The contents of the Error Data register can be read only in Error Data Output mode. The contents of the other diagnostic registers as well as the checkbit latch can be read in Diagnostic Output mode.

Parity

The IDT49C466 provides a parity check and generation facility. On a memory read the EDC generates parity bits for each data byte and outputs the parity byte on the parity bus, P0-7. During a memory write, parity is checked by comparing the parity bits input on P0-7 and the parity bits generated from the input data word. A discrepancy between these two causes the $\overline{\text{PERR}}$ flag to be asserted. In the case of partial word writes, the PERR flag may be inadvertently asserted because input parity for the merged data word is not available.

DIAG. REGISTER	LOADED BY	CONDITION	OUTPUT
CHECKBIT	SYNCLK ↑	ONLY ON 1st ERROR	SD8-15
SYNDROME (On 1st ERR)	SYNCLK ↑	ONLY ON 1st ERROR	SD16-23
ERR CNT	SYNCLK ↑	ON EVERY ERROR (Up to 15 ERRORS)	SD24-27
ERR TYPE	SYNCLK ↑	ONLY ON 1st ERROR	SD28-29
SYNDROME (On every ERROR)	SYNCLK ↑	ON EVERY ERROR	SD30-37

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
V_{CC}	Power Supply Voltage	–0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to VCC + 0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	30	mA

NOTE: 2617 tbl 09

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Ratings for extended periods of time may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	PGA	10	pF
			PQFP	5	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	PGA	12	pF
			PQFP	7	

NOTE: 2617 tbl 10

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%;

Symbol	Parameter	Test Conditions(1)			Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level			2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V			—	0.1	5.0	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5V			—	-0.1	–5.0	µA
I_{OZ}	Off State (Hi-Z) Output Current	V_{CC} = Max.	V_O = 0V		—	-0.1	–10	µA
			V_O = 3V		—	0.1	10	
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_{OUT}= 0V		COM'L.	–20	—	–100	mA
				MIL.	–15	—	–100	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.,	I_{OH} = –2mA	COM'L.	2.4	3.6	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –1.5mA	MIL.				
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 8mA	COM'L.	—	0.3	0.5	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 6mA	MIL.				
V_H	Input Hysteresis on input control lines				—	200	—	mV

NOTES: 2617 tbl 11

1. For conditions shown as min. or max., use appropriate Vcc value.
2. Typical values are at Vcc = 5.0V, +25°C ambient temperature.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Con't)

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{IN} = V_{CC}, or V_{IN} = GND V_{CC} = Max.		—	3.0	15	mA
I_{CCQT}	Quiescent Power Supply Current TTL Input Levels	V_{IN} = 3.4V V_{CC} = Max.		—	0.3	1	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{IN} = V_{CC}, or V_{IN} = GND	COM'L.	—	—	100	mA
		V_{CC} = Max. f = 10MHz Correct Mode	MIL.	—	—	115	mA

NOTES: 2617 tbl 12

1. For conditions shown as Min. or Max., use appropriate Vcc value.
2. Typical values are at Vcc = 5.0V, +25°C ambient temperature.

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AC PARAMETERS
PROPAGATION DELAY TIMES

Number	Parameter	Description		49C466 Max.		49C466A (50MHz)* Max.		Unit
		From Input[1]	To Output	Com'l.	Mil.	Com'l.	Mil.	
GENERATE (WRITE) PARAMETERS								
Without Write FIFO:								
1	t_{BC}	BEn	CBSYN (chkbit)	20	25	12		ns
2	t_{BM}	BEn	MDOUT	16	25	10		ns
3	t_{PPE}	Pxin	PERR	10	14	8		ns
4	t_{SC}	SDin	CBSYN (chkbit)	22	27	15		ns
5	**t_{SM}**	SDin	MDout	22	27	15		ns
6	t_{SPE}	SDin	$\overline{PERR}$	16	20	10		ns
With Write FIFO:								
7	t_{MC}	MCLK (Lo-Hi)	CBSYN (chkbit)	25	29	15		ns
8	t_{MMD}	MCLK (Lo-Hi)	MDout	25	29	15		ns
9	t_{WBSEL}	WBSEL	MDout	18	22	12		ns
DETECT (READ) PARAMETERS								
Without Read FIFO:								
10	t_{WYC}	SYNCLK (Lo-Hi)	CBSYN (syndr)	16	18	12		ns
11	**t_{ME}**	MDin	$\overline{ERR}$	20	25	10		ns
12	t_{MME}	MDin	$\overline{MERR}$	22	27	12		n
13	t_{CE}	CBI	$\overline{ERR}$	13	20	8		ns
14	t_{CME}	CBI	$\overline{MERR}$	13	20	8		ns
With Read FIFO:								
15	t_{SSD}	SCLK (Lo-Hi)	SDout	22	25	10		ns
16	t_{RBSEL}	RBSEL	SDout	18	20	12		ns
CORRECT (READ) PARAMETERS								
Without Read FIFO:								
17	t_{CS}	CBI	SDout	20	23	14		ns
18	t_{MP}	MDin	Pxout	22	27	15		ns
19	**t_{MS}**	MDin	SDout	22	27	15		ns
With Read FIFO:								
20	t_{SP}	SCLK (Lo-Hi)	Pxout	22	26	15		ns

NOTE:
2617 tbl 13

* PRELIMINARY.
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

PROPAGATION DELAY TIMES FROM LATCH ENABLES

Number	Parameter	Description		49C466 Max.		49C466A (50MHz)* Max.		Unit
		From Input(1)	To Output	Com'l.	Mil.	Com'l.	Mil.	
21	tMLE	MDILE (Lo-Hi)	$\overline{ERR}$	16	20	10		ns
22	tMLME	MDILE (Lo-Hi)	$\overline{MERR}$	18	22	10		ns
23	tMLP	MDILE (Lo-Hi)	Px	24	29	15		ns
24	tMLS	MDILE (Lo-Hi)	SDout	22	26	15		ns
25	tMOLS	$\overline{MDOLE}$ (Hi-Lo)	SDout	18	21	10		ns
26	tMOLP	$\overline{MDOLE}$ (Hi-Lo)	Px	18	21	10		ns
27	tSLC	SDILE (Lo-Hi)	CBSYN (chkbit)	20	26	15		ns
28	tSLM	SDILE (Lo-Hi)	MDout	20	26	12		ns
29	tSOLC	$\overline{SDOLE}$ (Hi-Lo)	CBSYN (chkbit)	12	16	10		ns
30	tSOLM	$\overline{SDOLE}$ (Hi-Lo)	MDout	15	19	10		ns

NOTE:
2617 tbl 14

- PRELIMINARY.

1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

R/W FIFO TIMES

Number	Parameter	Description		49C466				49C466A (50MHz)*				Unit
				Com'l.		Mil.		Com'l.		Mil.		
		From Input(1)	To Output	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
31	tRSF	RS1 (Hi-Lo) during SCLK LOW	$\overline{EF}$ (Hi-Lo)/$\overline{FF}$ (Lo-Hi)	—	16	—	19	—	16	—		ns
32	tSKEW1	RCLK (Lo-Hi) (SCLK or MCLK)	WCLK (Lo-Hi) (SCLK or MCLK)	10	—	12	—	8	—		—	ns
33	tSKEW2	WCLK (Lo-Hi) (SCLK or MCLK)	RCLK (Lo-Hi) (SCLK or MCLK)	10	—	12	—	8	—		—	ns
34	tEF	R/WCLK (Lo-Hi) (SCLK or MCLK)	$\overline{EF}$	—	15	—	19	—	10	—		ns
35	tFF	R/WCLK (Lo-Hi) (SCLK or MCLK)	$\overline{FF}$	—	15	—	19	—	10	—		ns

NOTE:
2617 tbl 15

- PRELIMINARY.

1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

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BYTE MERGE TIMES

Number	Parameter	Description		49C466 Max.		49C466A (50MHz)* Max.		Unit
		From Input(1)	To Output	Com'l.	Mil.	Com'l.	Mil.	
36	tSCM	SCLK (Lo-Hi)	MDout	25	27	15		ns
37	tMDM	$\overline{\text{MDOLE}}$ (Hi-Lo)	MDout	18	23	10		ns
38	tRBM	RBSEL	MDout	23	25	15		ns
39	tSDM	SDILE (Lo-Hi))	MDout	18	20	10		ns

2617 tbl 16

NOTE:
* PRELIMINARY.
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

ENABLE AND DISABLE TIMES

Number	Parameter	Description				49C466				49C466A (50MHz)*				Unit
						Com'l.		Mil.		Com'l.		Mil.		
		From Input(1)		To Output		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
40	tBESZx	BEN =	High	SDout	*	—	22	—	26	—	10			ns
41	tBESxZ		Low		Hi-Z	—	22	—	26	—	8			
42	tBEPZx	BEN =	High	Pout	*	—	15	—	15	—	10			ns
43	tBEPxZ		Low		Hi-Z	—	15	—	15	—	8			
44	tSEPZx	$\overline{\text{SOE}}$ =	Low	Pout	*	—	14	—	15	—	10			ns
45	tSEPxZ		High		Hi-Z	—	14	—	15	—	8			
46	tCECZx	$\overline{\text{MOE}}$ =	Low	CBSYN	*	—	12	—	15	—	10			ns
47	tCECxZ		High		Hi-Z	—	10	—	12	—	8			
48	tMEMZx	$\overline{\text{MOE}}$ =	Low	MDout	*	—	22	—	25	—	10			ns
49	tMEMxZ		High		Hi-Z	—	18	—	25	—	8			
50	tSESZx	$\overline{\text{SOE}}$ =	Low	SDout	*	—	16	—	22	—	10			ns
51	tSESxZ		High		Hi-Z	—	20	—	28	—	8			

2617 tbl 17

NOTES:
* PRELIMINARY.
1. (High-Z) indicates high impedence.
2. * indicates delay to both edges.

SET-UP AND HOLD TIMES

Number	Parameter	Description			49C466 Min.		49C466A (50MHz)* Min.		Unit
		From Input[1]	To Output		Com'l.	Mil.	Com'l.	Mil.	
52	t_{CMLS}	CBI Set-up	before MDILE =	Hi-Lo	2	3	1		ns
53	t_{CMLH}	CBI Hold	after MDILE =	Hi-Lo	6	6	2		ns
54	t_{MMLS}	MDIN Set-up	before MDILE =	Hi-Lo	2	2	1		ns
55	t_{MMLH}	MDIN Hold	after MDILE =	Hi-Lo	6	6	2		ns
56	t_{CMOLS}	CBI Set-up	before $\overline{\text{MDOLE}}$ =	Lo-Hi	10	11	5		ns
57	t_{CMOLH}	CBI Hold	after $\overline{\text{MDOLE}}$ =	Lo-Hi	2	2	0		ns
58	t_{MMOLS}	MDIN Set-up	before $\overline{\text{MDOLE}}$ =	Lo-Hi	10	10	5		ns
59	t_{MMOLH}	MDIN Hold	after $\overline{\text{MDOLE}}$ =	Lo-Hi	4	4	0		ns
60	t_{MMCS}	MDIN Set-up	before MCLK =	Lo-Hi	10	11	6		ns
61	t_{MMCH}	MDIN Hold	after MCLK =	Lo-Hi	4	4	2		ns
62	t_{SSLS}	SDIN Set-up	before SDILE =	Hi-Lo	5	5	1		ns
63	t_{SSLH}	SDIN Hold	after SDILE =	Hi-Lo	3	3	2		ns
64	t_{SSCS}	SDIN Set-up	before SCLK	Lo-Hi	2	2	1		ns
65	t_{SSCH}	SDIN Hold	after SCLK	Lo-Hi	6	6	2		ns
66	t_{SSOLS}	SDIN Set-up	before $\overline{\text{SDOLE}}$ =	Lo-Hi	8	10	5		ns
67	t_{SSOLH}	SDIN Hold	after $\overline{\text{SDOLE}}$ =	Lo-Hi	0	0	0		ns
68	t_{SCSD}	SCLK (Lo-Hi)	before $\overline{\text{SDOLE}}$ =	Lo-Hi	14	15	10		ns
69	t_{MCSD}	MCLK (Lo-Hi)	before $\overline{\text{SDOLE}}$ =	Lo-Hi	14	15	10		ns
70	t_{ENS}	R/W FIFO Enable Set-up	before S/M CLK =	Lo-Hi	4	4	2		ns
71	t_{ENH}	R/W FIFO Enable Hold	after S/M CLK =	Lo-Hi	4	4	1		ns
72	t_{RSS}	RS1 (Lo-Hi)	R/WCLK =	Lo-Hi	6	8	2		ns
73	t_{MODS}	Mode Data Set-up	before SCLK =	Lo-Hi	4	4	2		ns
74	t_{MODH}	Mode Data Hold	after SCLK =	Lo-Hi	4	4	1		ns
75	t_{MENS}	Mode Enable Set-up	before SCLK =	Lo-Hi	4	4	2		ns
76	t_{MENH}	Mode Enable Hold	after SCLK =	Lo-Hi	4	4	1		ns
77	t_{MSD}	MDIN	$\overline{\text{SDOLE}}$ =	Lo-Hi	22	23	10		ns
DIAGNOSTIC SET-UP AND HOLD TIMES									
78	t_{CSCS}	CBI Set-up	before SYNCLK =	Lo-Hi	4	4	2		ns
79	t_{MSCS}	MDIN Set-up			4	4	2		ns
80	t_{MLSCS}[2]	MDILE = Lo-Hi Set-up			4	6	2		ns
81	t_{MLSCS}[2]	MDILE = Lo-Hi Set-up			12	14	10		ns
82	t_{CSCH}[2]	CBI Hold	After SYNCLK=	Lo-Hi					ns
83	t_{MSCH}[2]	MDIN Hold							ns
84	t_{MLSCS}[2]	MDILE = Lo-Hi Hold							ns
85	t_{MLSCS}[2]	MDILE = Lo-Hi Hold							ns

2617 tbl 18

NOTES:

* PRELIMINARY.

1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.
2. Set-up time specified in 81 required only for proper updating of error type register. Updating of all other diagnostic registers require set-up time specified in 80.

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MINIMUM PULSE WIDTH

Number	Parameter	Description			49C466 Min.		49C466A (50MHz)* Min.		Unit
		From Input(1)		Condition	Com'l.	Mil.	Com'l.	Mil.	
86	tRS	Min. RS1 LOW time	to reset buffers	—	6	8	5.0		ns
87	tMLE	Min. MDILE HIGH time	to strobe new data	MD, CBI = Valid	6	8	5.0		ns
88	tMDOLE	Min. $\overline{\text{MDOLE}}$ LOW time	to strobe new data	—	6	8	5.0		ns
89	tSLE	Min. SDILE HIGH time	to strobe new data	SD = Valid	6	8	5.0		ns
90	tCLK	Min. S/MCLK HIGH time	to clock in new data	EN signal LOW	6	8	5.0		ns
91	tSYNCLK	Min. SYNCLK HIGH time	to clock in new data	—	6	8	5.0		ns
92	tSDOLE	Min. $\overline{\text{SDOLE}}$ LOW time	to clock in new data	—	6	8	5.0		ns

NOTE:

2617 tbl 19

* PRELIMINARY.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 15

2617 tbl 21

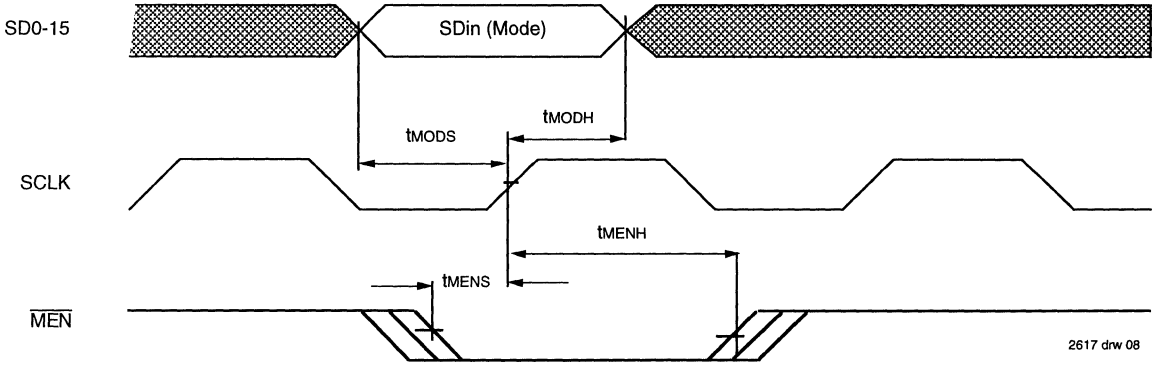


Figure 4. Mode Enable Timing

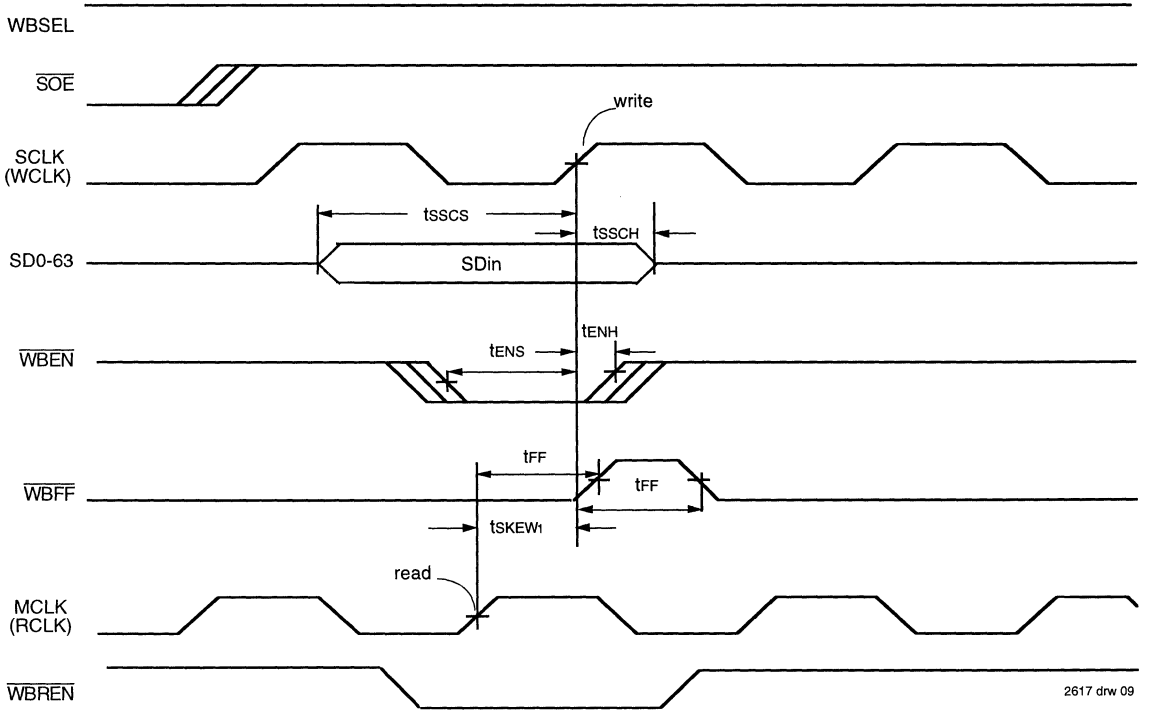
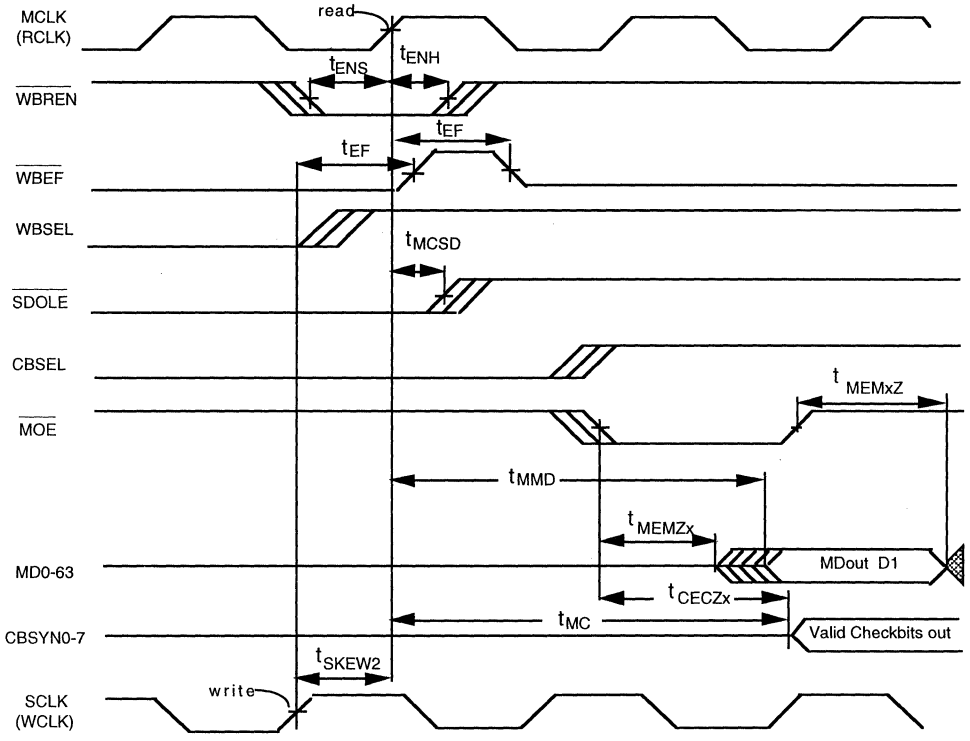


Figure 5. WFIFO Write Timing (Write Cycle)

11



2617 drw 10

Figure 6. WFIFO Read and Checkbit Generate Timing (Write Cycle)

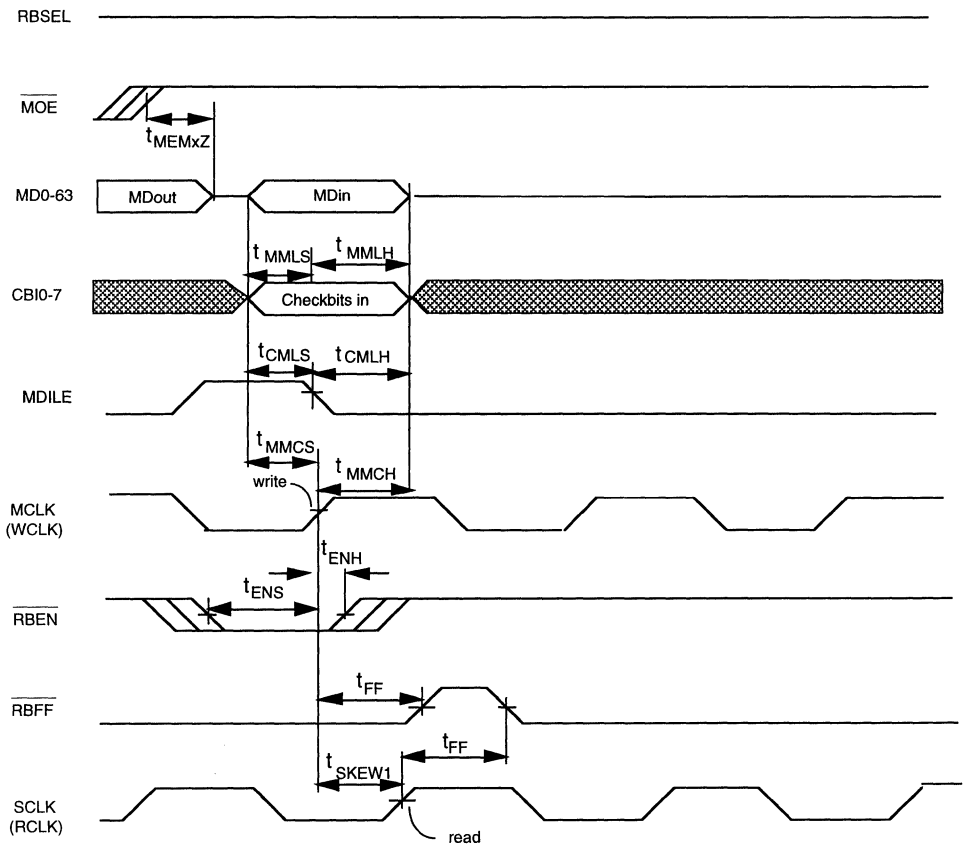


Figure 7. RFIFO Write Timing (Read Cycle)

11

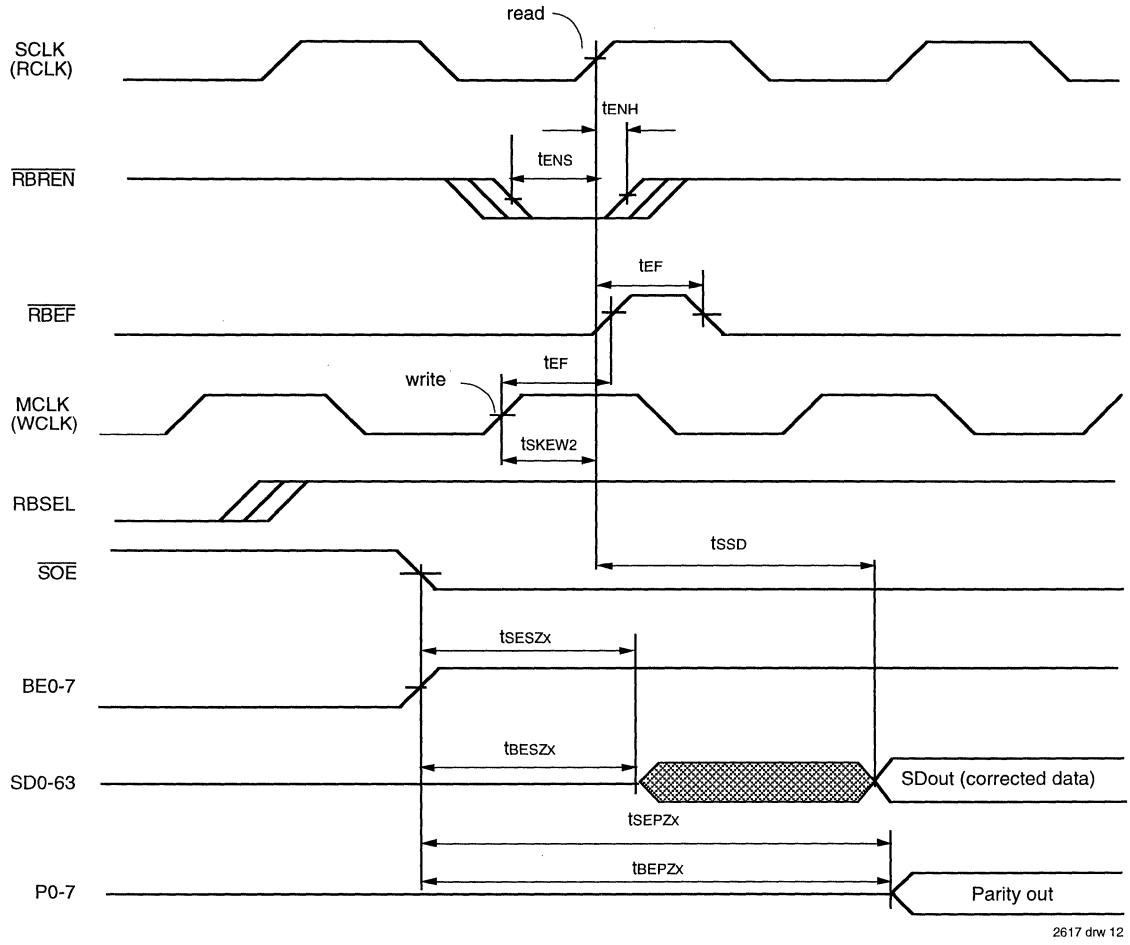


Figure 8. RFIFO Read Timing (Read Cycle)

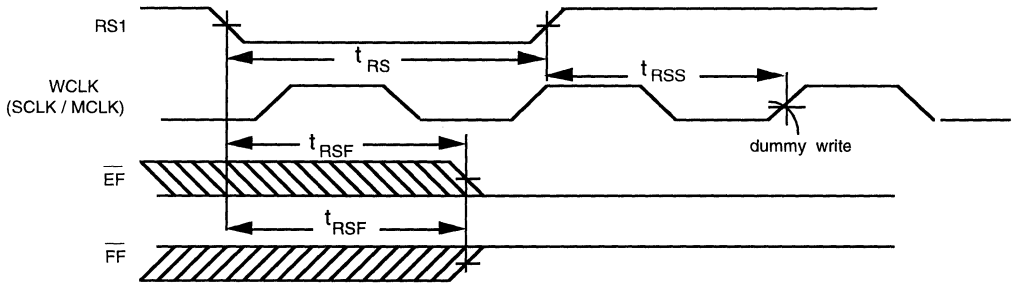
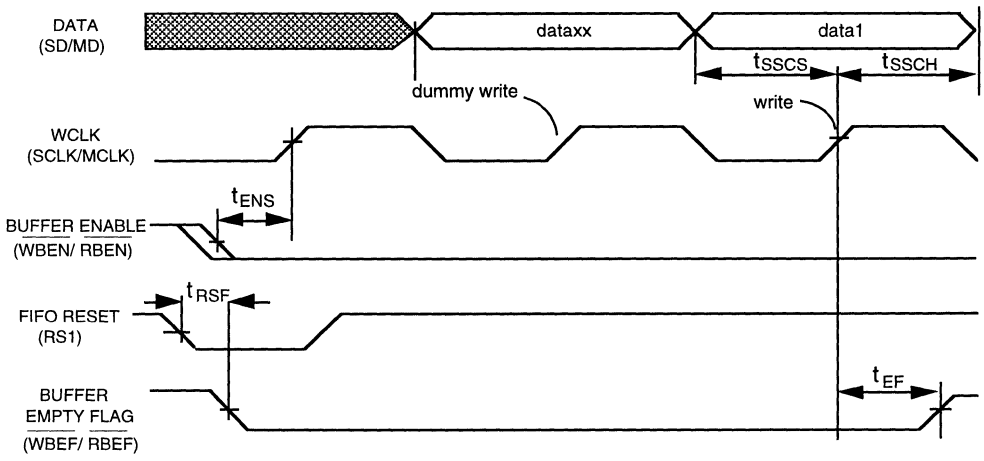


Figure 9. FIFO (WFIFO/RFIFO) Reset Timing



2617 drw 14

Figure 10. FIFO (WFIFO/RFIFO) Write Latency Timing

11

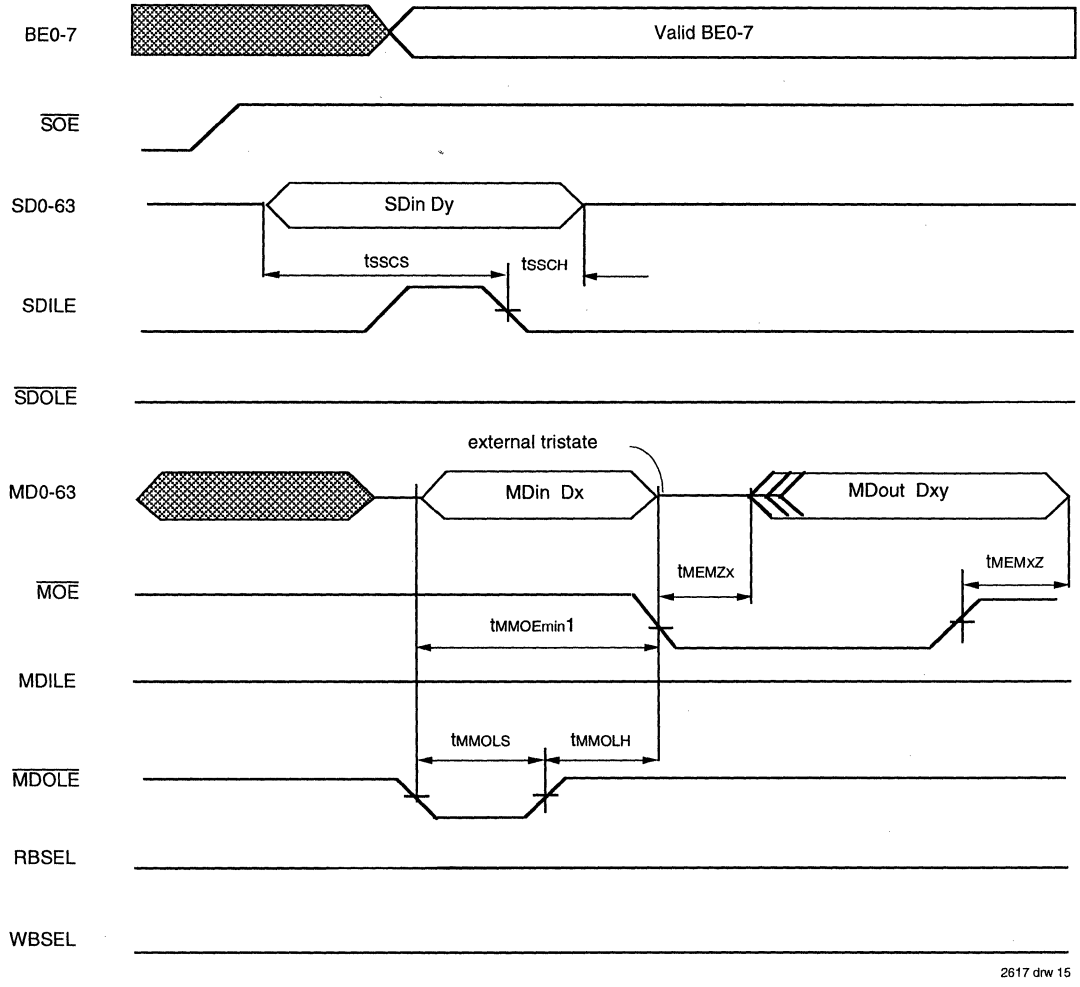


Figure 11. Partial Word Write/Byte Merge Timing

NOTE:
1. t_{MMOE} is not a propagation delay. For partial word write operations $t_{MMOE\ MIN} = t_{MDM}$.

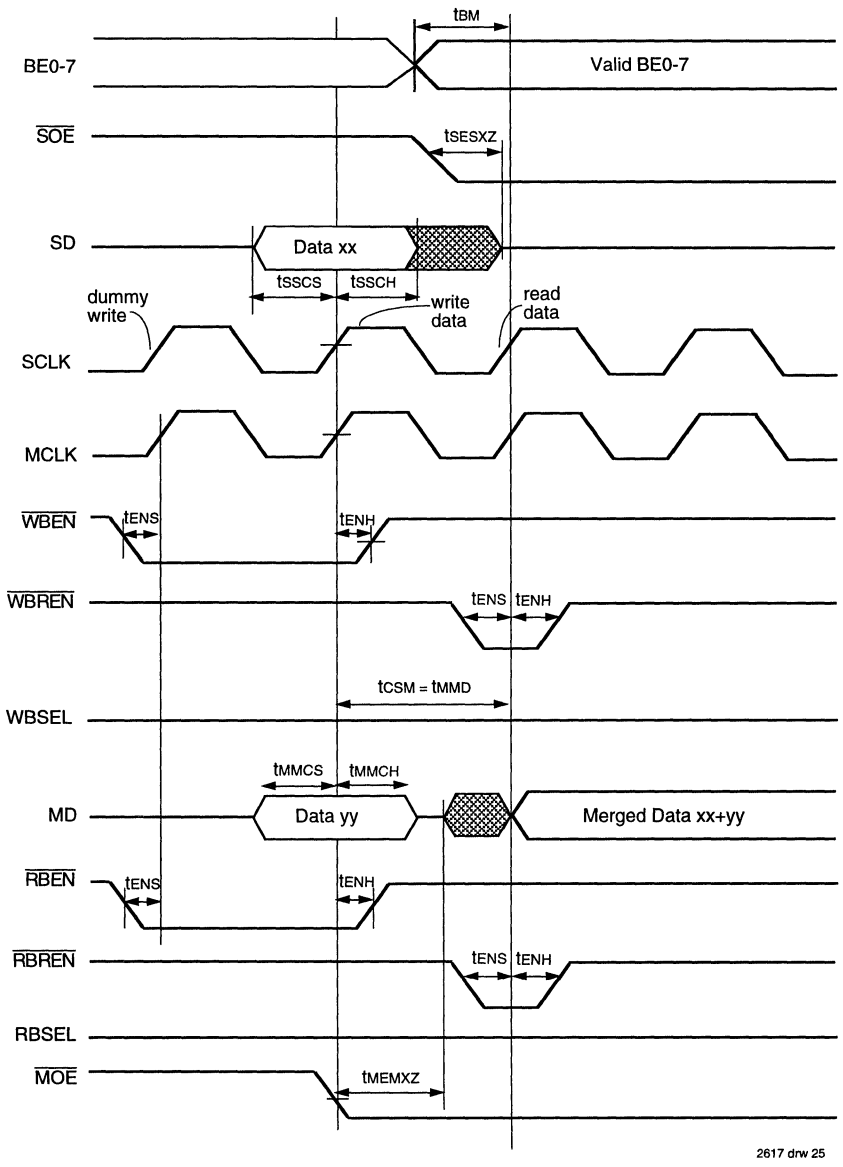
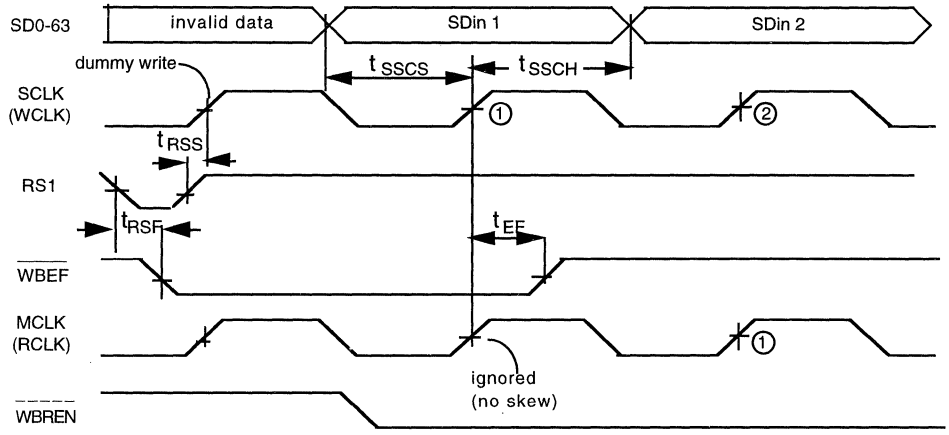


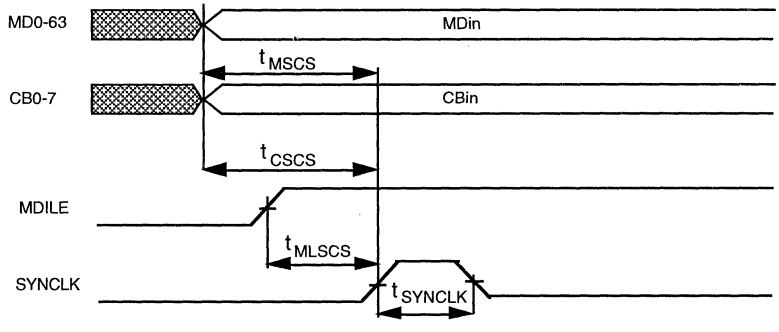
Figure 12. Partial Word Write/Byte Merge Timing using both RFIFO and WFIFO

11



2617 drw 20

Figure 13. Write FIFO Write Timing with Clock Skew Violation

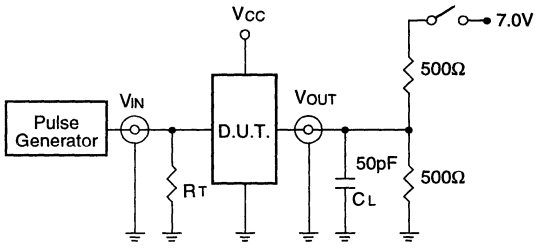


2617 drw 21

Figure 14. Diagnostic Timing

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2617 drw 16

SWITCH POSITION

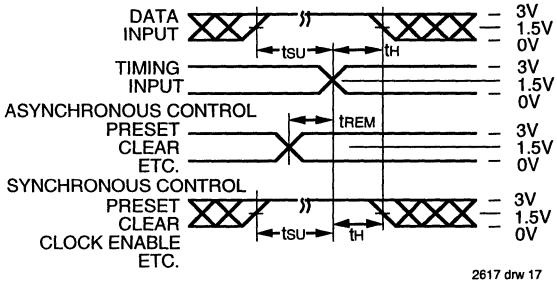
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2617 tbl 20

DEFINITIONS:

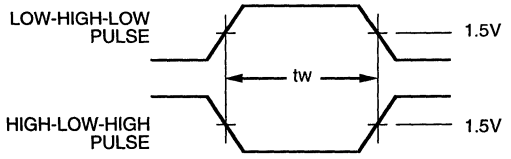
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



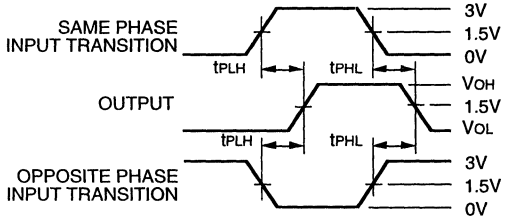
2617 drw 17

PULSE WIDTH



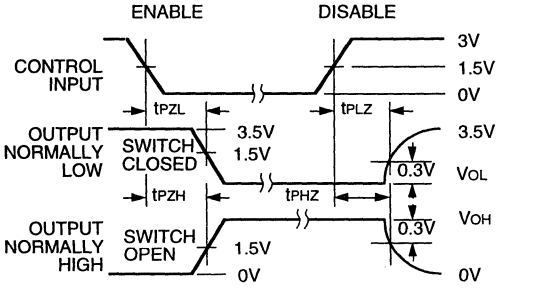
2617 drw 18

PROPAGATION DELAY



2617 drw 26

ENABLE AND DISABLE TIMES



2617 drw 27

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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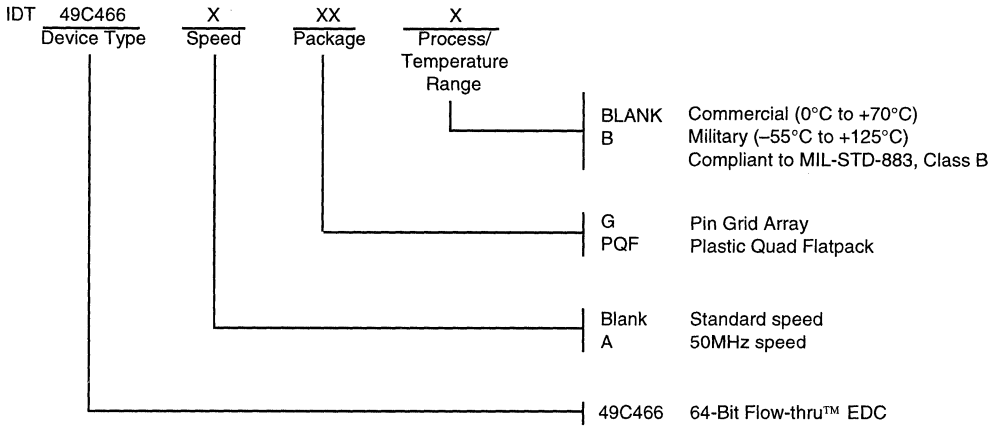
ORDERING INFORMATION



2617 drw 19

Integrated Device Technology, Inc.

3.3V 64-BIT FLOW-THRU ERROR DETECTION AND CORRECTION UNIT

IDT49C3466
ADVANCE INFORMATION

FEATURES:

- 64-bit wide Flow-thruEDC™
- Separate System and Memory Data Input/Output Buses
- — Error Detect Time: 20ns
  — Error Correct Time: 22ns
- Corrects all single bit errors; Detects all double bit errors and some multiple bit errors
- Configurable 16-deep bus read/write FIFOs with flags
- Simultaneous check bit generation and correction of memory data
- Supports partial word writes on byte boundaries
- Low noise output
- Sophisticated error diagnostics and error logging
- Parity generation on system data bus
- VCC = 3.3V ±0.3V
- 208-pin Plastic Quad Flatpack

DESCRIPTION:

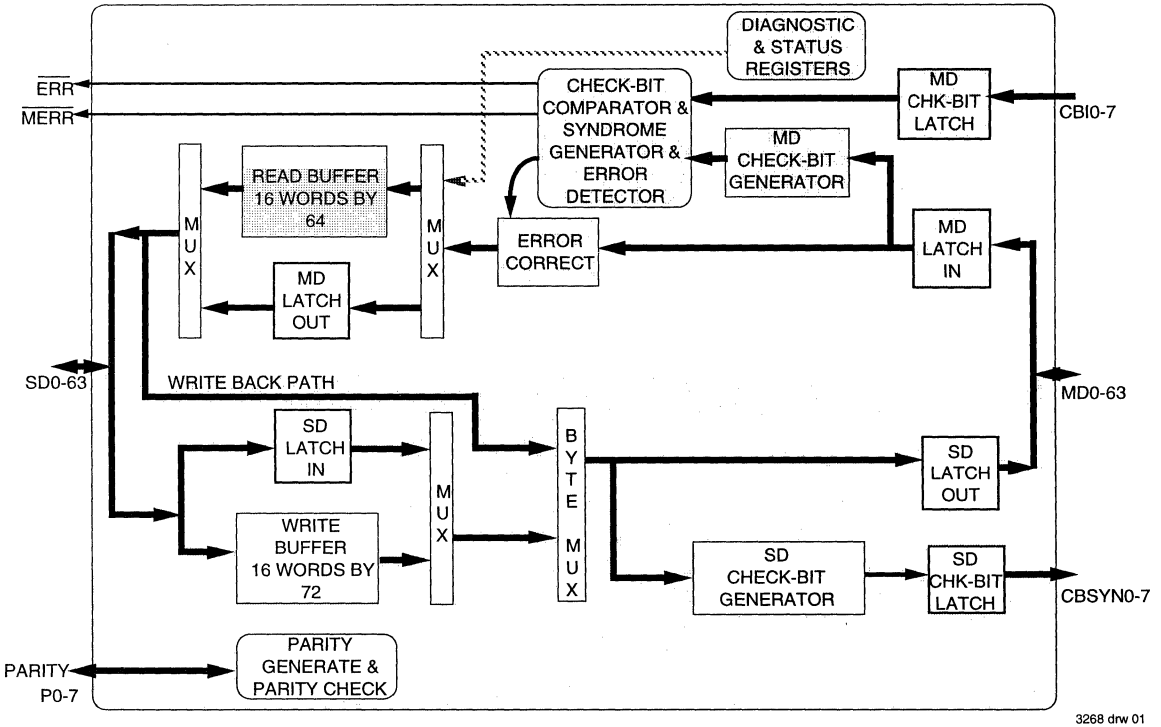
The IDT49C3466 64-bit Flow-thruEDC is a high-speed error detection and correction unit that ensures data integrity in memory systems. The flow-thru architecture, with separate system and memory data buses, is ideally suited for pipelined memory systems.

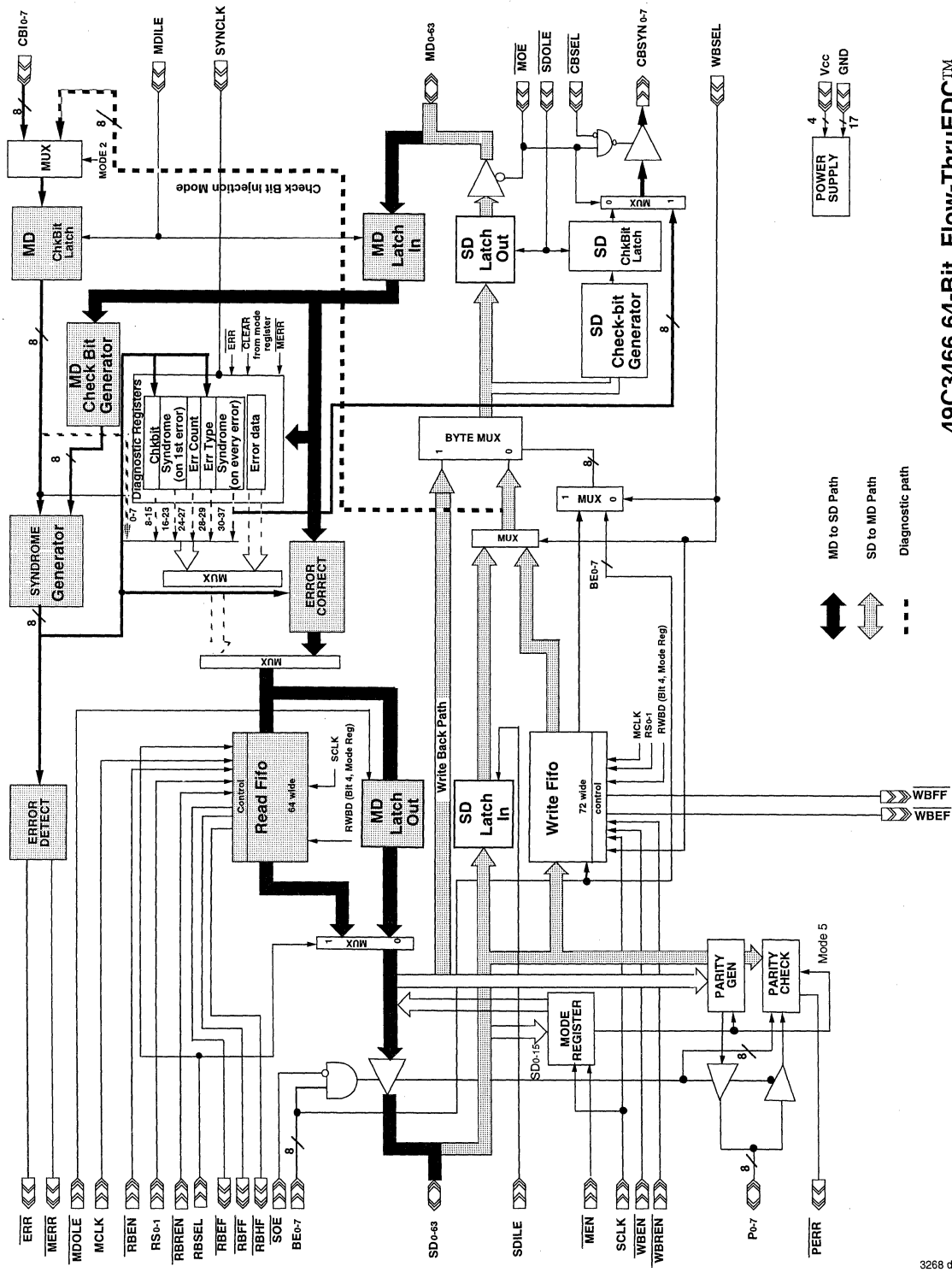
Implementing a modified Hamming code, the IDT49C3466 corrects all single bit hard and soft errors, and detects all double bit errors. The read/write FIFOs can store up to sixteen words. FIFO full and empty flags indicate whether additional data can be written to or read from the EDC.

Check bit generation for partial word writes on byte boundaries is supported on the IDT49C3466.

Diagnostic features include a check bit register, syndrome registers, a four bit error counter which logs up to 15 errors, and an error data register which stores the complete error data word. Parity can be generated and checked on the system bus by the IDT49C3466.

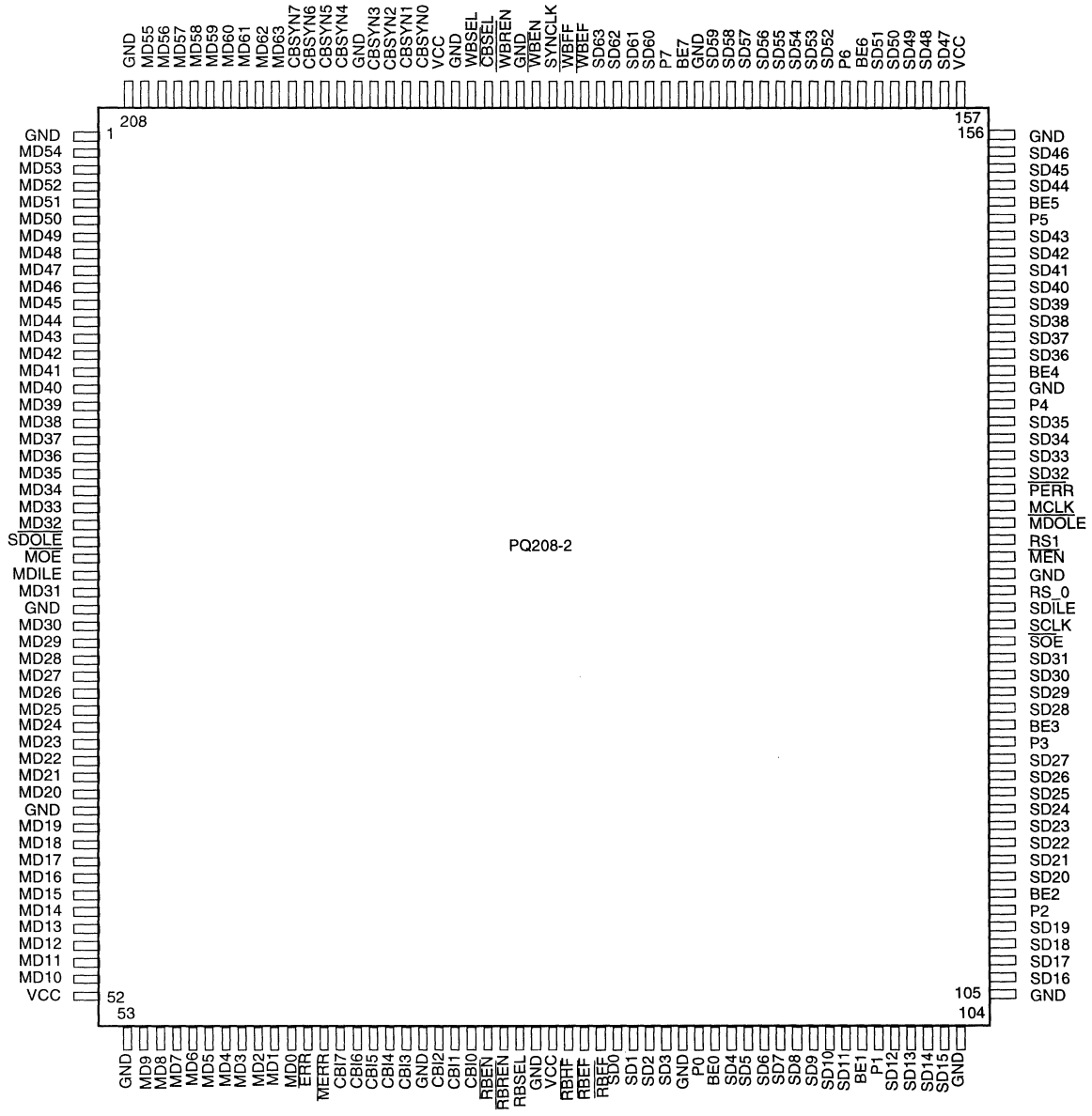
SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM




49C3466 64-Bit Flow-ThruEDC™
CBI0-7
MDILE
SYNCLK
MD0-63
MOE
SDOLE
CBSEL
CBSYN0-7
WBSEL
Vcc
GND
POWER SUPPLY
MUX
MODE 2
Check Bit Injection Mode
MD ChkBit Latch
MD Latch In
SD Latch Out
SD ChkBit Latch
SD Check-bit Generator
MD Check Bit Generator
ERR
CLEAR from mode register
MERR
Diagnostic Registers
Chkbit Syndrome (on 1st error)
Err Count
Err Type
Syndrome (on every error)
Error data
BYTE MUX
SYNDROME Generator
ERROR CORRECT
BE0-7
MD to SD Path
SD to MD Path
Diagnostic path
Write Back Path
Read Fifo
64 wide
Control
SCLK
RWBD (Bit 4, Mode Reg)
MD Latch Out
SD Latch In
Write Fifo
72 wide
control
MCLK
RS0-1
RWBD (Bit 4, Mode Reg)
WBFF
WBEF
ERROR DETECT
PARITY GEN
PARITY CHECK
Mode 5
MODE REGISTER
SD0-15
ERR
MERR
MDOLE
MCLK
RBEN
RS0-1
RBREN
RBSEL
RBEF
RBFF
RBHF
SOE
BE0-7
SD0-63
SDILE
MEN
SCLK
WBEN
WBREN
P0-7
PERR

3268 drw 02

PIN CONFIGURATION



PQFP

Top View

3268 drw 03

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PIN DESCRIPTION

Pin Name	I/O	Description
SD_{0-63}	I/O	**System Data Bus:** is a bidirectional 64-bit bus interfacing to the system or CPU. When System Output Enable, $\overline{SOE}$, is HIGH or Byte Enable, BE_{0-7}, is LOW, data can be input. When System Output Enable, $\overline{SOE}$, is LOW and Byte Enable, BE_{0-7}, is HIGH, the SD bus output drivers are enabled.
MD_{0-63}	I/O	**Memory Data Bus:** is a bidirectional 64-bit bus interfacing to the memory. During a read cycle, ($\overline{MOE}$ HIGH) memory data is input for error detection and correction. Data is output on the Memory Data Bus, when $\overline{MOE}$ is LOW.
CBI_{0-7}	I	**Check Bit Inputs:** interface to the check bit memory.
$CBSYN_{0-7}$	O	**Check Bit/Syndrome Output:** When $\overline{MOE}$ is LOW the generated check bits are output. When CBSEL is HIGH and $\overline{MOE}$ is HIGH, the syndrome bits are output. The bus is tristated when $\overline{MOE}$ = 1 and CBSEL = 0.
P_{0-7}	I/O	**Parity for bytes 0 to 7:** These pins are parity inputs when the corresponding Byte Enable (BE) is LOW or $\overline{SOE}$ is HIGH, and are used to generate the parity error signal ($\overline{PERR}$). These pins are outputs when the corresponding Byte Enable (BE) is HIGH and $\overline{SOE}$ is LOW.
Control Inputs		
$\overline{SOE}$	I	**System Output Enable:** enables system data bus output drivers if the corresponding Byte Enable (BE_{0-7}) is HIGH.
BE_{0-7}	I	**Byte Enable:** is used along with $\overline{SOE}$, to enable the System Data outputs for a particular byte. For example, if BE_1 is HIGH, the System data outputs for byte 1 (SD_{8-15}) are enabled. The BE_{0-7} pins also control the byte mux. If a particular BE is HIGH during a memory read cycle, that byte is fed back to the memory data bus. This is used during partial word write operations and writing corrected data back to memory.
$\overline{MOE}$	I	**Memory Output Enable:** when LOW, enables the output buffers of the memory data bus (MD) and CBSYN bus. It also controls the CBSYN mux. When LOW, checkbits are selected, when HIGH, syndrome is selected.
MDILE	I	**Memory Data Input Latch Enable:** on the HIGH-to-LOW transition, latches MD and CBI in MD input latch and MD check bit latch respectively. The latches are transparent when MDILE is HIGH.
$\overline{MDOLE}$	I	**Memory Data Output Latch Enable:** latches data in the MD output latch on the LOW-to-HIGH transition of $\overline{MDOLE}$. When $\overline{MDOLE}$ is LOW, the MD output latch is transparent.
$\overline{SDOLE}$	I	**System Data Output Latch Enable:** latches data in the SD output latch and the SD checkbit latch on the LOW-to-HIGH transition of $\overline{SDOLE}$. The latch is transparent when $\overline{SDOLE}$ is LOW.
SDILE	I	**System Data Input Latch Enable:** latches SD in the SD input latch on the HIGH-to-LOW transition. When SDILE is HIGH, the SD input latch is transparent.
WBSEL	I	**Write FIFO Select:** when HIGH, the write FIFO is selected. When WBSEL is LOW, the SD input latch is selected.
$\overline{WBEN}$	I	**Write FIFO Enable:** when LOW, allows SD data to be written to the write FIFO on the SCLK rising edge.
$\overline{WBREN}$	I	**Write FIFO Read Enable:** when LOW, allows data to be read from the the write FIFO on MCLK rising edge.
RS_{0-1}	I	**Reset and Select pins** (read and write FIFO FIFOs) RS_1 RS_0 Function 0 0 Reset 16-deep FIFO or first 8-deep FIFO 0 1 Reset second 8-deep FIFO 1 0 Select 16-deep FIFO or first 8-deep FIFO 1 1 Select second 8-deep FIFO

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PIN DESCRIPTION (Continued)

Pin Name	I/O	Description
RBSEL	I	**Read FIFO Select:** when HIGH, read FIFO is selected (data goes through read FIFO, not MD output latch). When LOW, the MD output latch is selected.
$\overline{\text{RBEN}}$	I	**Read FIFO Enable:** when LOW, allows data to be written into the read FIFO on the LOW-to-HIGH transition of the memory clock.
$\overline{\text{RBREN}}$	I	**Read FIFO Enable:** when LOW, allows data to be read from the read FIFO on the LOW-to-HIGH transition of SCLK
$\overline{\text{CBSEL}}$	I	**Checkbit Syndrome Output Enable:** Controls the CBSYN output buffer.When HIGH, the buffer is enabled. When CBSEL is LOW, $\overline{\text{MOE}}$ controls the buffer.
$\overline{\text{MEN}}$	I	**Mode Enable Input:** when LOW, SD_{0-15} is loaded into the EDC mode register on the LOW-to-HIGH transition of the SCLK. This pin must be held LOW for the entire SCLK HIGH period, as shown in Figure 4.
Clock Inputs		
MCLK	I	**Memory Clock:** on the LOW-to-HIGH transition of MCLK, memory data is written to the read FIFO when $\overline{\text{RBEN}}$ is LOW. Data is read from the write FIFO when $\overline{\text{WBREN}}$ is LOW, on the LOW-to-HIGH transition of MCLK.
SCLK	I	**System Clock:** on the LOW-to-HIGH transition of the SCLK, data is read from the read FIFO when $\overline{\text{RBREN}}$ is LOW. Data on the system data bus is written into the write FIFO when $\overline{\text{WBEN}}$ is LOW on the LOW-to-HIGH transition of SCLK. Clocks data into mode register when $\overline{\text{MEN}}$ is LOW.
SYNCLK	I	**Syndrome Clock:** Used to load diagnostic registers. When an error occurs, Error Counter is incremented on the rising SYNCLK edge (up to 15 errors). On the first error after a diagnostic reset, SYNCLK rising edge clocks data into Check Bit, Syndrome, Error Type and Error Data registers. One of the syndrome registers has new data clocked in on every SYNCLK rising edge.
Status Outputs		
$\overline{\text{WBEF}}$	O	**Write FIFO Empty Flag:** when LOW, indicates that the write FIFO is empty. After a reset, the $\overline{\text{WBEF}}$ goes LOW.
$\overline{\text{WBFF}}$	O	**Write FIFO Full Flag:** when LOW, indicates that the write FIFO is full. After a reset; $\overline{\text{WBFF}}$ goes HIGH.
$\overline{\text{RBEF}}$	O	**Read FIFO Empty Flag:** when LOW, indicates that the read FIFO is empty. After a reset, the $\overline{\text{RBEF}}$ goes LOW.
$\overline{\text{RBHF}}$	O	**Read FIFO Half-full Flag:** when LOW, indicates that there are eight or more data words (in the 16-deep configuration) or four or more data words (in the dual 8-deep configuration) in the read FIFO. The flag will return HIGH when less than eight (or four) data words are in the FIFO.
$\overline{\text{RBFF}}$	O	**Read FIFO Full Flag:** when LOW, indicates that the read FIFO is full. After a reset, $\overline{\text{RBFF}}$ goes HIGH.
$\overline{\text{ERR}}$	O	**Error Flag:** when $\overline{\text{ERR}}$ is LOW, a data error is indicated. The $\overline{\text{ERR}}$ is not latched internally.
$\overline{\text{MERR}}$	O	**Multiple Error Flag:** when $\overline{\text{MERR}}$ is LOW, a multiple data error is indicated. The $\overline{\text{MERR}}$ is not latched internally.
$\overline{\text{PERR}}$	O	**Parity Error Flag:** when LOW, indicates a parity error on the system data bus input.
Power Supply		
V_{CC}	P	Power Supply Voltage.
GND	P	Ground.

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DETAILED DESCRIPTION —

64-BIT MODIFIED HAMMING CODE - CHECKBIT ENCODING CHART(1, 2)

Generated Checkbits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

3268 tbl 03

Generated Checkbits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CB0	Even (XOR)		X	X	X		X			X	X		X			X	
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)									X	X	X	X	X	X	X	X

3268 tbl 04

Generated Checkbits	Parity	Participating Data Bits															
		32	33	34	.35	36	37	38	39	40	41	42	43	44	45	46	47
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)	X	X	X	X	X	X	X	X								
CB7	Even (XOR)									X	X	X	X	X	X	X	X

3268 tbl 05

Generated Checkbits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CB0	Even (XOR)	X				X		X	X			X		X	X		X
CB1	Even (XOR)	X	X	X		X		X		X		X		X			
CB2	Odd (XNOR)	X			X	X			X		X	X			X		X
CB3	Odd (XNOR)	X	X				X	X	X				X	X	X		
CB4	Even (XOR)			X	X	X	X	X	X							X	X
CB5	Even (XOR)									X	X	X	X	X	X	X	X
CB6	Even (XOR)									X	X	X	X	X	X	X	X
CB7	Even (XOR)	X	X	X	X	X	X	X	X								

3268 tbl 06

NOTES:

1. The table indicates the data bits participating in the checkbit generation. For example, checkbit CB0 is the Exclusive-OR function of the 64 data input bits marked with an X.
2. The checkbit is generated as either an XOR or an XNOR of the 64 data bits noted by an "X" in the table.

DETAILED DESCRIPTION —

64-BIT SYNDROME DECODE TO BIT-IN-ERROR(1)

				HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				S7	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
				S6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			Syndrome	S5	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			Bits	S4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HEX	S3	S2	S1	S0																
0	0	0	0	0	*	C4	C5	T	C6	T	T	62	C7	T	T	46	T	M	M	T
1	0	0	0	1	C0	T	T	14	T	M	M	T	T	M	M	T	M	T	T	30
2	0	0	1	0	C1	T	T	M	T	34	56	T	T	50	40	T	M	T	T	M
3	0	0	1	1	T	18	8	T	M	T	T	M	M	T	T	M	T	2	24	T
4	0	1	0	0	C2	T	T	15	T	35	57	T	T	51	41	T	M	T	T	31
5	0	1	0	1	T	19	9	T	M	T	T	63	M	T	T	47	T	3	25	T
6	0	1	1	0	T	20	10	T	M	T	T	M	M	T	T	M	T	4	26	T
7	0	1	1	1	M	T	T	M	T	36	58	T	T	52	42	T	M	T	T	M
8	1	0	0	0	C3	T	T	M	T	37	59	T	T	53	43	T	M	T	T	M
9	1	0	0	1	T	21	11	T	M	T	T	M	M	T	T	M	T	5	27	T
A	1	0	1	0	T	22	12	T	33	T	T	M	49	T	T	M	T	6	28	T
B	1	0	1	1	17	T	T	M	T	38	60	T	T	54	44	T	1	T	T	M
C	1	1	0	0	T	23	13	T	M	T	T	M	M	T	T	M	T	7	29	T
D	1	1	0	1	M	T	T	M	T	39	61	T	T	55	45	T	M	T	T	M
E	1	1	1	0	16	T	T	M	T	M	M	T	T	M	M	T	0	T	T	M
F	1	1	1	1	T	M	M	T	32	T	T	M	48	T	T	M	T	M	M	T

3268 tbl 07

NOTES:

1. The table indicates the decoding of the eight syndrome bits to identify the bit-in-error for a single-bit error, or whether a double or triple-bit error was detected.
   The all-zero case indicates no error detected.
   * = No errors detected
   # = The number of the single data bit-in-error
   T = Two errors detected
   M = Three or more detected
   C# = The number of the single checkbits in error

IDT49C3466 OPERATION

The EDC is involved in two types of operation — memory reads and memory writes. With the IDT49C3466, both these can be accomplished by utilizing either of two possible data paths — one incorporating the FIFO and the other without the FIFO. These operations are treated separately below.

Memory Write

The involvement of the EDC in this type of operation is relatively minimal since it does not call for any error checking. It only generates the check bits associated with each 64-bit wide data word. The EDC can be in generate-detect or normal mode for this operation.

When a write operation is performed, it must be ensured that the SD output buffer (enabled by $\overline{SOE}$ and BE_{0-7}) is disabled so that no attempt is made to simultaneously transfer read data onto the System Data (SD) Bus.

When the write FIFO (WFIFO) is bypassed (WBSEL LOW), data passes through the SD Latch In. To latch data, the SDILE signal should be pulled LOW. The special case of a partial word write or byte merge is discussed later. Here it is assumed that all 64 bits are being written. Consequently, BE_{0-7} must all be LOW.

The data is fed to the SD Checkbit generator where appropriate checkbits are generated. Both system data and the generated checkbits can be latched by pulling the $\overline{SDOLE}$ signal HIGH. Asserting $\overline{MOE}$ enables the MD output buffer and data is output to the Memory Data (MD) bus. $\overline{CBSEL}$ (=1) or $\overline{MOE}$(=0) need to be asserted to enable the CBSYN output buffer and output checkbits on $CBSYN_{0-7}$.

When the write FIFO is selected (WBSEL = 1), instead of asserting SDILE, $\overline{WBEN}$ is asserted and data is clocked into the write FIFO on the rising edge of SCLK. $\overline{WBFF}$ is asserted when the WFIFO is full and this inhibits further write attempts (see section on "Clock Skew" and "R/W FIFO Operation at Boundaries") to the WFIFO. When $\overline{WBREN}$ is asserted, data can be clocked out of the write FIFO on the rising edge of MCLK. $\overline{WBEF}$ is asserted when the WFIFO is empty and this inhibits further read attempts (see section on "Clock Skew") from the WFIFO.

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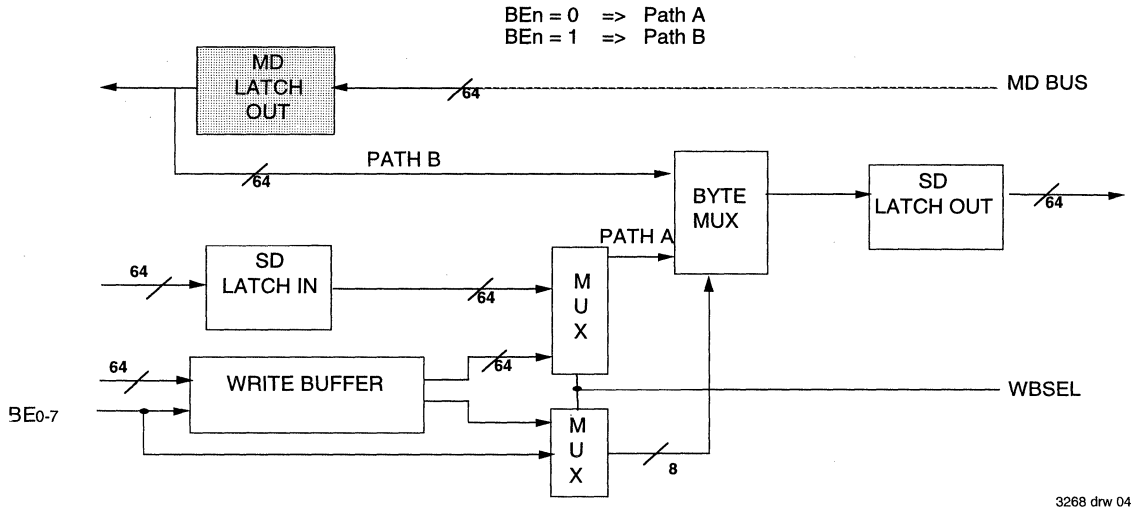

Figure 1. Byte Merge

Memory Read

During a memory read, data and the corresponding input checkbits are read from the MD bus and CBI0-7, respectively. The memory and checkbit data may both be latched as they come in (MD Latch In and MD Checkbit latch) by the MDILE signal. Memory data is sent to the MD checkbit generator (where checkbits corresponding to the input data are generated) and to the error correct circuitry. The generated checkbits are X-ORed with the input checkbits to produce the syndrome word. This is sent to the error correction circuitry which generates the corrected data (normal mode). The corrected data is output to the SD bus via either of two data paths. When RBSEL is LOW, data flows through MD Latch Out. Pulling MDOLE HIGH latches this data. The output buffer is enabled by asserting SOE (=0) and BE0-7 (=1). Corrected data can be written back to memory by enabling the MD output buffer. In order to ensure selection of the write back path (Path B in figure 1) at the byte mux, BEO-7 should be all 1's while WBSEL = 0. If WBSEL = 1, buffered BEO-7 from the output of the write FIFO controls the byte mux.

If the read FIFO (RFIFO) is selected (RBSEL HIGH), data is clocked into the FIFO (Read_FIFO Write) when RBEN is LOW, on the rising edge of MCLK. RBFF is asserted when the RFIFO is full and this inhibits further write attempts to the RFIFO (see section on "Clock Skew" and "R/W FIFO operation at Boundaries"). Data is clocked out of the FIFO (Read_FIFO Read) when RBREN is LOW on the rising edge of SCLK. RBEF is asserted when the RFIFO is empty and this inhibits further read attempts (see section on "Clock Skew") from the RFIFO.

Note: In case of multiple error SD should be ignored in correct mode.

Clock Skew

A skew between the read and write clocks, as specified by tskew, is recommended. This specification is not a stringent one, in the manner of setup and hold times, but is important in preempting latencies at FIFO boundaries. For example – When a word is written to an empty FIFO, there is a finite delay before the FIFO is recognized as no longer being empty and hence allowing a read from the same FIFO. Similarly when a word is read from a full FIFO, there is a delay before a write can successfully be attempted. The tskew specification accounts for these cases. During cycles other than on full/empty FIFO boundaries, the clock skew is not required and the device functions correctly even when the reads and writes occur simultaneously. If the tskew specification is ignored and SCLK and MCLK were permanently tied together, there is an extra cycle latency in the cases mentioned above. Clock skew violation is illustrated in Figure 13.

FIFO Write Latency

The first data written to either of the (read or write) FIFOs, after the FIFO is reset, suffers a single clock latency. Data that is set-up with respect to the first clock is ignored and the data that is set-up with respect to the second clock edge after the reset, is stored as the first data in the FIFO (Refer to Figures 9 and 10). The empty-flag is deasserted after this second clock edge and 15 more data words (in a 16 deep configuration) can be written to the FIFO after this.

The latency can be reduced or eliminated by providing a "dummy" or "set-up" clock edge before the actual write to the FIFO. The dummy write clock can be provided any time after reset and before the next buffer write operation takes place. The latency described here (shown in Figures 10 and 13) occurs only after a FIFO reset. In other cases where the FIFO becomes empty there is no latency.

R/W FIFO Operation At Boundaries

In the 49C3466 the write pointer is incremented on every FIFO write. Similarly the read pointer is incremented on every FIFO read. In most cases on a FIFO read, the last data read remains at the output of the FIFO, until the read pointer is further incremented. On the last (the write that fills the FIFO) FIFO write after the FIFO read, however, this last read data is overwritten by the 16th write following the empty condition and consequently the data at the FIFO output is liable to change. The situation is depicted in the diagram below.

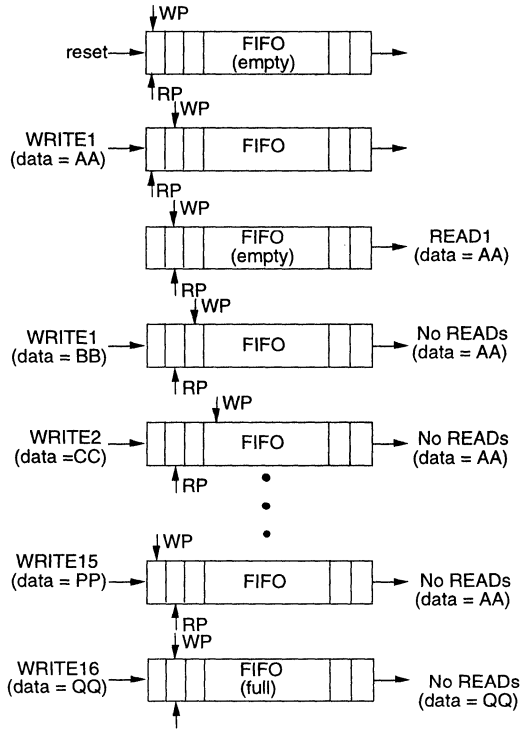

Figure 2. R/W FIFO Operation

The diagram in figure 2 progresses from the FIFO initialization(reset) through a sequence of write operations. After the first write, a read is executed which establishes the data at the FIFO output(AA). On the last write to the FIFO(the write that fills the FIFO), the location of the last read data is overwritten and the FIFO output changes from AA to the data just written, namely QQ.

This operation needs to be taken into account in the design of the system. In case of a burst operation where FIFO data is output at a much slower rate than the rate at which data is input and the full flag is expected to inhibit further writes, the user cannot expect the FIFO output to remain static through the 16th write of the burst. If this is a requisite to the design, the FIFO output should be latched. In the case of the write FIFO this can be accomplished on-chip by latching the FIFO output in the SD output latch. For the read FIFO, the FIFO output must be latched externally to accomplish the same thing, since there is no latch on-chip following the FIFO. If this cannot be done and the situation described above is expected to occur in normal operation, the write must be inhibited one cycle before the FIFO becomes full.

Partial Word Write/Byte Merge

Writing a word shorter than 64 bits to memory is treated as a special case. The checkbits generated for a data word shorter than 64 bits and written to a particular memory location differ from the checkbits that would be generated by the entire 64-bit data word at the same location. Hence, the byte merge operation requires reading of the contents of the memory location to be written to, merging the byte/bytes being written (from SD side) with the other component bytes previously at that memory location (from MD side), generating a checkbit word for this composite word and writing both the composite data word and the generated checkbits to memory. The BEn bits supplied by the user determine the bytes that come from SD and those that come from MD, as illustrated in Figure 1.

EDC Modes

The IDT49C3466 has 5 modes of operation. Refer to table below for a description of the modes.

The **Error Data Output** mode is useful for memory initialization as described below. In **Checkbit Injection mode**, the MD Checkbit Latch is loaded with data from the System Bus. This serves to verify the functioning of the EDC. Any discrepancy between the injected checkbits and generated checkbits should result in assertion of the $\overline{ERR}$, $\overline{MERR}$ signals.

These modes and certain other features such as clear, buffer configuration, etc., can be selected by appropriately loading the Mode Register. The Mode Register can be written to by asserting $\overline{MEN}$. Then $SD_{0\text{-}15}$ is clocked into the mode register on the rising edge of SCLK.

MODE REGISTER CONFIGURATION

15 7	6	5	4	3	2 0
UNUSED	RMODE	PSEL	RWBD	CLEAR	EDCM0-2

EDCM2	EDCM1	EDCM0	OPERATION
0	0	0	ERROR-DATA OUTPUT MODE
0	0	1	DIAGNOSTIC-OUTPUT MODE
0	1	0	GENERATE-DETECT MODE
0	1	1	NORMAL MODE
1	0	0	CHECKBIT-INJECTION MODE

RMODE	OPERATION
0	NOP
1	READ MODE REGISTER ON SD BUS

RWBD	OPERATION
0	DUAL FIFOS (8)
1	SINGLE FIFO (16)

CLEAR	OPERATION
0	NOP
1	CLEAR ALL DIAGNOSTIC REGISTERS

PSEL	OPERATION
0	EVEN PARITY
1	ODD PARITY

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OPERATING MODE DESCRIPTION

Mode	Description
MODE 0	**Error-Data Output Mode:** This mode allows the uncorrected data captured from an error event by the Error-Data Register to be read by the system for diagnostic purposes. The Error-Data Register is cleared by setting the mode register "clear"-bit.
MODE 1	**Diagnostic-Output Mode:** In this mode, contents of latch and five internal registers are read by the system for diagnostic and error logging purposes. Internal data paths allow output from the CBI LATCH to be read directly by the system bus for diagnostic purposes. The contents of the internal diagnostic checkbit register, syndrome registers, error count register and error-type register are also output on the SD bus.
MODE 2	**Generate-Detect Mode:** (Detect-Only) The EDC performs checkbit generation during a memory write, and performs error detection only during a memory read.
MODE 3	**Normal Mode:** The EDC performs checkbit generation during memory writes and error detection and correction during memory reads.
MODE 4	**Checkbit-Injection Mode:** In this mode, the checkbit latch is loaded with desired 8-bit data from the SD bus.This eight bit data passes through SD Latch in or write FIFO to the MD check bit latch. By inserting various checkbit values, correct functioning of the EDC can be verified "on-board". The rest of the operation is similar to regular memory reads. The EDC compares the injected checkbits against the internally generated checkbits. Any discrepancy in the injected checkbits and the internally generated checkbits will cause the $\overline{ERR}$ / $\overline{MERR}$ to go LOW.

3268 tbl 08

Memory Initialization

Memory initialization involves clearing all memory data locations and writing the corresponding checkbits (checkbits corresponding to all zero data = $0C) to checkbit memory. This can be done using the 49C3466 to first create an "all-zero-data" source. This is done by setting the CLEAR bit in the mode register. This clears all diagnostic registers. Then this data can be written back to memory in the Error-Data output (Mode 0) mode. In order to wrap the all-zero data back to the MD bus, BE0-7 should be high and WBSEL =0.

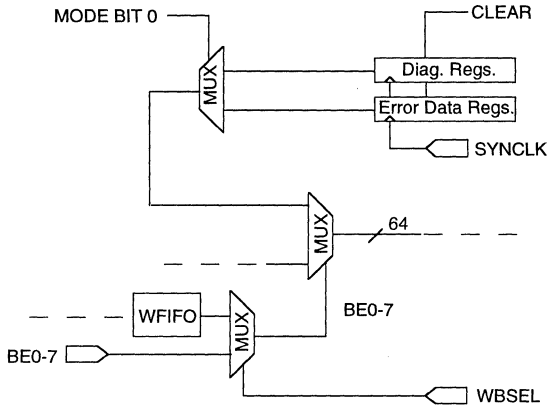
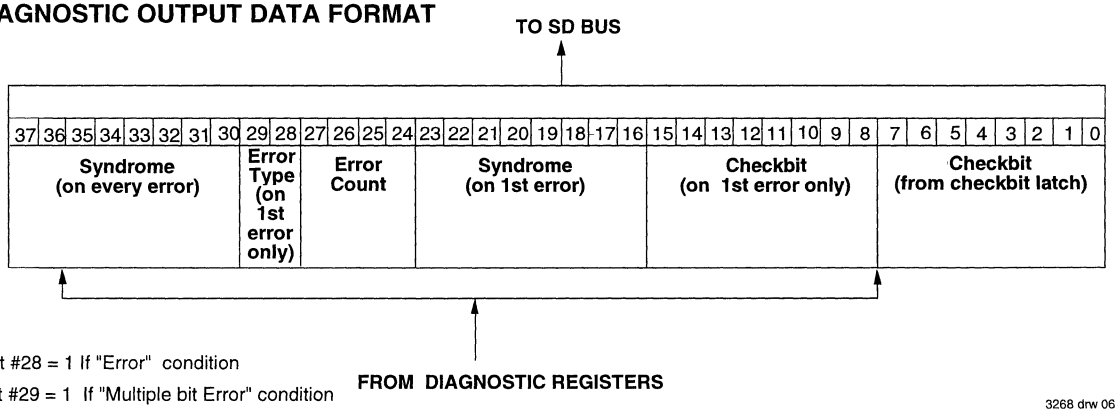


Fig 3. Memory Initialization using Diagnostic Output/Error Data Output Mode

DIAGNOSTIC OUTPUT DATA FORMAT



* Bit #28 = 1 If "Error" condition
Bit #29 = 1 If "Multiple bit Error" condition

3268 drw 06

Diagnostics

The diagnostic ability of the IDT49C3466 rests on a set of 6 registers that provide error logging information. These include the checkbit register, error count register, error type register, 2 syndrome registers and the error data register. Data is clocked into each of these registers by SYNCLK. The error data register, checkbit register, error type register and one of the syndrome registers are reloaded only in the case of the first error after a clear. The other syndrome register and the error count register are reloaded on every error condition SYNCLK edge. The contents of the Error Data register can be read only in Error Data Output mode. The contents of the other diagnostic registers as well as the checkbit latch can be read in Diagnostic Output mode.

Parity

The IDT49C3466 provides a parity check and generation facility. On a memory read the EDC generates parity bits for each data byte and outputs the parity byte on the parity bus, P0-7. During a memory write, parity is checked by comparing the parity bits input on P0-7 and the parity bits generated from the input data word. A discrepancy between these two causes the $\overline{\text{PERR}}$ flag to be asserted. In the case of partial word writes, the $\overline{\text{PERR}}$ flag is based on the parity bits Px and data bytes input on SD bus.

DIAG. REGISTER	LOADED BY	CONDITION	OUTPUT
CHECKBIT	SYNCLK ↑	ONLY ON 1st ERROR	SD8-15
SYNDROME (On 1st ERR)	SYNCLK ↑	ONLY ON 1st ERROR	SD16-23
ERR CNT	SYNCLK ↑	ON EVERY ERROR (Up to 15 ERRORS)	SD24-27
ERR TYPE	SYNCLK ↑	ONLY ON 1st ERROR	SD28-29
SYNDROME (On every ERROR)	SYNCLK ↑	ON EVERY ERROR	SD30-37

11

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	30	mA

3268 tbl 09

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

3268 tbl 10

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	—	±1	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max.[3], V_{OUT} = 0V	COM'L.		—		mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	COM'L. I_{OH} = –1mA	2.4[5]	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	COM'L. I_{OL} = 4mA	—	0.3	0.5	V
V_H	Input Hysteresis on input control lines			—	100	—	mV

3268 tbl 11

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

The following conditions apply unless otherwise specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{IN} = V_{CC}, or V_{IN} = GND V_{CC} = Max.		—	3.0	15	mA
I_{CCQT}	Quiescent Power Supply Current TTL Input Levels	V_{IN} = V_{CC} –0.6 V_{CC} = Max.		—	1.5	100	µA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{IN} = V_{CC}, or V_{IN} = GND V_{CC} = Max. f = 10MHz Correct Mode	COM'L.	—	—	—	mA

3268 tbl 12

NOTES:
1. For conditions shown as Min. or Max., use appropriate Vcc value.
2. Typical values are at Vcc = 3.3V, +25°C ambient temperature.

11

AC PARAMETERS
PROPAGATION DELAY TIMES

Number	Parameter	Description		49C3466 Max.	Unit
		From Input[1]	To Output	Com'l.	
GENERATE (WRITE) PARAMETERS					
Without Write FIFO:					
1	t_{BC}	BEn	CBSYN (chkbit)	20	ns
2	t_{BM}	BEn	MDOUT	16	ns
3	t_{PPE}	Pxin	PERR	10	ns
4	t_{SC}	SDin	CBSYN (chkbit)	22	ns
5	**t_{SM}**	SDin	MDout	22	ns
6	t_{SPE}	SDin	$\overline{PERR}$	16	ns
With Write FIFO:					
7	t_{MC}	MCLK (Lo-Hi)	CBSYN (chkbit)	25	ns
8	t_{MMD}	MCLK (Lo-Hi)	MDout	25	ns
9	t_{WBSEL}	WBSEL	MDout	18	ns
DETECT (READ) PARAMETERS					
Without Read FIFO:					
10	t_{WYC}	SYNCLK (Lo-Hi)	CBSYN (syndr)	16	ns
11	**t_{ME}**	MDin	$\overline{ERR}$	20	ns
12	t_{MME}	MDin	$\overline{MERR}$	22	ns
13	t_{CE}	CBI	$\overline{ERR}$	13	ns
14	t_{CME}	CBI	$\overline{MERR}$	13	ns
18a	t_{MP}	MDin	Pxout	22	ns
19a	**t_{MS}**	MDin	SDout	—	ns
With Read FIFO:					
15	t_{SSD}	SCLK (Lo-Hi)	SDout	22	ns
16	t_{RBSEL}	RBSEL	SDout	18	ns
CORRECT (READ) PARAMETERS					
Without Read FIFO:					
17	t_{CS}	CBI	SDout	20	ns
18	t_{MP}	MDin	Pxout	22	ns
19	**t_{MS}**	MDin	SDout	22	ns
With Read FIFO:					
20	t_{SP}	SCLK (Lo-Hi)	Pxout	22	ns

NOTE:
3268 tbl 13

* PRELIMINARY.
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

PROPAGATION DELAY TIMES FROM LATCH ENABLES

Number	Parameter	Description		49C3466 Max.	Unit
		From Input[1]	To Output	Com'l.	
21	t_{MLE}	MDILE (Lo-Hi)	$\overline{ERR}$	16	ns
22	t_{MLME}	MDILE (Lo-Hi)	$\overline{MERR}$	18	ns
23	t_{MLP}	MDILE (Lo-Hi)	Px (Detect Mode)	24	ns
23a	t_{MLP}	MDILE (Lo-Hi)	Px (Correct Mode)	—	ns
24	t_{MLS}	MDILE (Lo-Hi)	SDout (Detect Mode)	22	ns
24a	t_{MLS}	MDILE (Lo-Hi)	SDout (Correct Mode)	—	ns
25	t_{MOLS}	$\overline{MDOLE}$ (Hi-Lo)	SDout	18	ns
26	t_{MOLP}	$\overline{MDOLE}$ (Hi-Lo)	Px	18	ns
27	t_{SLC}	SDILE (Lo-Hi)	CBSYN (chkbit)	20	ns
28	t_{SLM}	SDILE (Lo-Hi)	MDout	20	ns
29	t_{SOLC}	$\overline{SDOLE}$ (Hi-Lo)	CBSYN (chkbit)	12	ns
30	t_{SOLM}	$\overline{SDOLE}$ (Hi-Lo)	MDout	15	ns

NOTE: 3268 tbl 14

- PRELIMINARY.

1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

R/W FIFO TIMES

Number	Parameter	Description		49C3466 Com'l.		Unit
		From Input[1]	To Output	Min.	Max.	
31	t_{RSF}	RS1 (Hi-Lo) during SCLK LOW	$\overline{EF}$ (Hi-Lo)/$\overline{FF}$ (Lo-Hi)	—	16	ns
32	t_{SKEW1}	RCLK (Lo-Hi) (SCLK or MCLK)	WCLK (Lo-Hi) (SCLK or MCLK)	10	—	ns
33	t_{SKEW2}	WCLK (Lo-Hi) (SCLK or MCLK)	RCLK (Lo-Hi) (SCLK or MCLK)	10	—	ns
34	t_{EF}	R/WCLK (Lo-Hi) (SCLK or MCLK)	$\overline{EF}$	—	15	ns
35	t_{FF}	R/WCLK (Lo-Hi) (SCLK or MCLK)	$\overline{FF}$	—	15	ns
35a	t_{HF}	R/WCLK (Lo-Hi) (SCLK or MCLK)	$\overline{HF}$	—	15	ns

NOTE: 3268 tbl 15

- PRELIMINARY.

1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

11

BYTE MERGE TIMES

Number	Parameter	Description		49C3466 Max.	Unit
		From Input(1)	To Output	Com'l.	
36	tSCM	SCLK (Lo-Hi)	MDout	25	ns
37	tMDM	$\overline{\text{MDOLE}}$ (Hi-Lo)	MDout	18	ns
38	tRBM	RBSEL	MDout	23	ns

3268 tbl 16

NOTE:
* PRELIMINARY.
1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

ENABLE AND DISABLE TIMES

Number	Parameter	Description			49C3466 Com'l.		Unit
		From Input(1)		To Output	Min.	Max.	
40	tBESZx	BEN =	High	SDout *	—	22	ns
41	tBESxZ		Low	Hi-Z	—	22	
42	tBEPZx	BEN =	High	Pout *	—	15	ns
43	tBEPxZ		Low	Hi-Z	—	15	
44	tSEPZx	$\overline{\text{SOE}}$ =	Low	Pout *	—	14	ns
45	tSEPxZ		High	Hi-Z	—	14	
46	tCECZx	$\overline{\text{MOE}}$ =	Low	CBSYN *	—	12	ns
47	tCECxZ		High	Hi-Z	—	10	
48	tMEMZx	$\overline{\text{MOE}}$ =	Low	MDout *	—	22	ns
49	tMEMxZ		High	Hi-Z	—	18	
50	tSESZx	$\overline{\text{SOE}}$ =	Low	SDout *	—	16	ns
51	tSESxZ		High	Hi-Z	—	20	

3268 tbl 17

NOTES:
* PRELIMINARY.
1. (High-Z) indicates high impedence.
2. * indicates delay to both edges.

SET-UP AND HOLD TIMES

Number	Parameter	Description			49C3466 Min.	Unit
		From Input[1]	To Output		Com'l.	
52	tCMLS	CBI Set-up	before MDILE =	Hi-Lo	2	ns
53	tCMLH	CBI Hold	after MDILE =	Hi-Lo	6	ns
54	tMMLS	MDIN Set-up	before MDILE =	Hi-Lo	2	ns
55	tMMLH	MDIN Hold	after MDILE =	Hi-Lo	6	ns
56	tCMOLS	CBI Set-up	before $\overline{\text{MDOLE}}$ =	Lo-Hi	10	1ns
57	tCMOLH	CBI Hold	after $\overline{\text{MDOLE}}$ =	Lo-Hi	2	ns
58	tMMOLS	MDIN Set-up (Detect Mode)	before $\overline{\text{MDOLE}}$ =	Lo-Hi	10	ns
58a	tMMOLS	MDIN Set-up (Correct Mode)	before $\overline{\text{MDOLE}}$ =	Lo-Hi		ns
59	tMMOLH	MDIN Hold	after $\overline{\text{MDOLE}}$ =	Lo-Hi	4	ns
60	tMMCS	MDIN Set-up (Detect Mode)	before MCLK =	Lo-Hi	10	ns
60a	tMMCS	MDIN Set-up (Correct Mode)	before MCLK =	Lo-Hi		ns
61	tMMCH	MDIN Hold	after MCLK =	Lo-Hi	4	ns
62	tSSLS	SDIN Set-up	before SDILE =	Hi-Lo	5	ns
63	tSSLH	SDIN Hold	after SDILE =	Hi-Lo	3	ns
64	tSSCS	SDIN Set-up	before SCLK	Lo-Hi	2	ns
65	tSSCH	SDIN Hold	after SCLK	Lo-Hi	6	ns
66	tSSOLS	SDIN Set-up	before $\overline{\text{SDOLE}}$ =	Lo-Hi	8	ns
67	tSSOLH	SDIN Hold	after $\overline{\text{SDOLE}}$ =	Lo-Hi	0	ns
68	tSCSD	SCLK (Lo-Hi)	before $\overline{\text{SDOLE}}$ =	Lo-Hi	14	ns
69	tMCSD	MCLK (Lo-Hi)	before $\overline{\text{SDOLE}}$ =	Lo-Hi	14	ns
70	tENS	R/W FIFO Enable Set-up	before S/M CLK =	Lo-Hi	4	ns
71	tENH	R/W FIFO Enable Hold	after S/M CLK =	Lo-Hi	4	ns
72	tRSS	RS1 (Lo-Hi)	R/WCLK =	Lo-Hi	6	ns
73	tMODS	Mode Data Set-up	before SCLK =	Lo-Hi	4	ns
74	tMODH	Mode Data Hold	after SCLK =	Lo-Hi	4	ns
75	tMENS	Mode Enable Set-up	before SCLK =	Lo-Hi	4	ns
76	tMENH	Mode Enable Hold	after SCLK =	Lo-Hi	4	ns
77	tMSD	MDIN Set-Up (Detect Mode)	$\overline{\text{SDOLE}}$ =	Lo-Hi		ns
77a	tMSD	MDIN Set-Up (Correct Mode)	$\overline{\text{SDOLE}}$ =	Lo-Hi	22	ns
78	tBES	BE Set-up	before SCLK =	Lo-Hi	2	ns
79	tBEH	BE Hold	after SCLK =	Lo-Hi	6	ns
DIAGNOSTIC SET-UP AND HOLD TIMES						
80	tCSCS	CBI Set-up				ns
81	tMSCS	MDIN Set-up	before SYNCLK =	Lo-Hi		ns
82	tMLSCS	MDILE = Lo-Hi Set-up				ns
83	tCSCH	CBI Hold			0	ns
84	tMSCH	MDIN Hold			0	ns
85	tMLSCH	MDILE = Lo-Hi Hold	After SYNCLK=	Lo-Hi	0	ns

NOTE:

3268 tbl 18

* PRELIMINARY.

1. (Lo-Hi) indicates LOW-to-HIGH transition and vice versa.

11

MINIMUM PULSE WIDTH

Number	Parameter	Description			49C3466 Min.	Unit
		From Input[1]		Condition	Com'l.	
86	tRS	Min. RS1 LOW time	to reset buffers	—	6	ns
87	tMLE	Min. MDILE HIGH time	to strobe new data	MD, CBI = Valid	6	ns
88	tMDOLE	Min. $\overline{\text{MDOLE}}$ LOW time	to strobe new data	—	6	ns
89	tSLE	Min. SDILE HIGH time	to strobe new data	SD = Valid	6	ns
90	tCLK	Min. S/MCLK HIGH time	to clock in new data	EN signal LOW	6	ns
91	tSYNCLK	Min. SYNCLK HIGH time	to clock in new data	—	6	ns
92	tSDOLE	Min. $\overline{\text{SDOLE}}$ LOW time	to clock in new data	—	6	ns

NOTE:

3268 tbl 19

* PRELIMINARY.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 15

2617 tbl 21

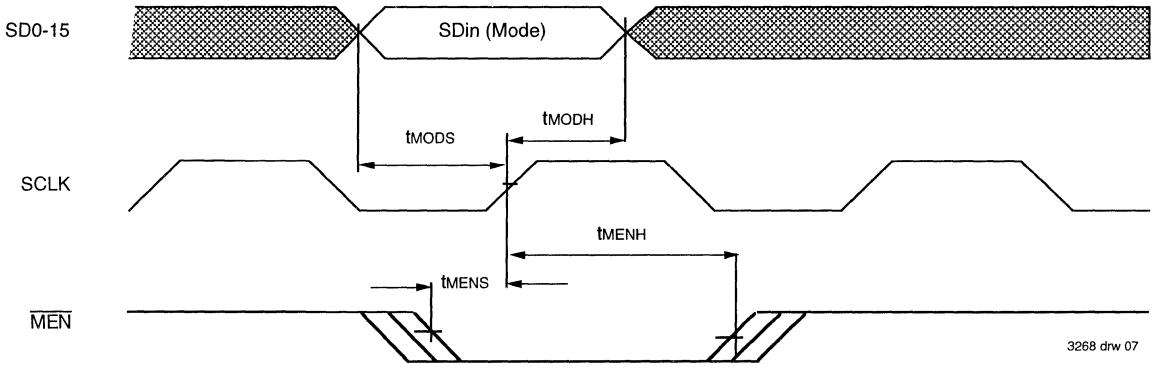


Figure 4. Mode Enable Timing

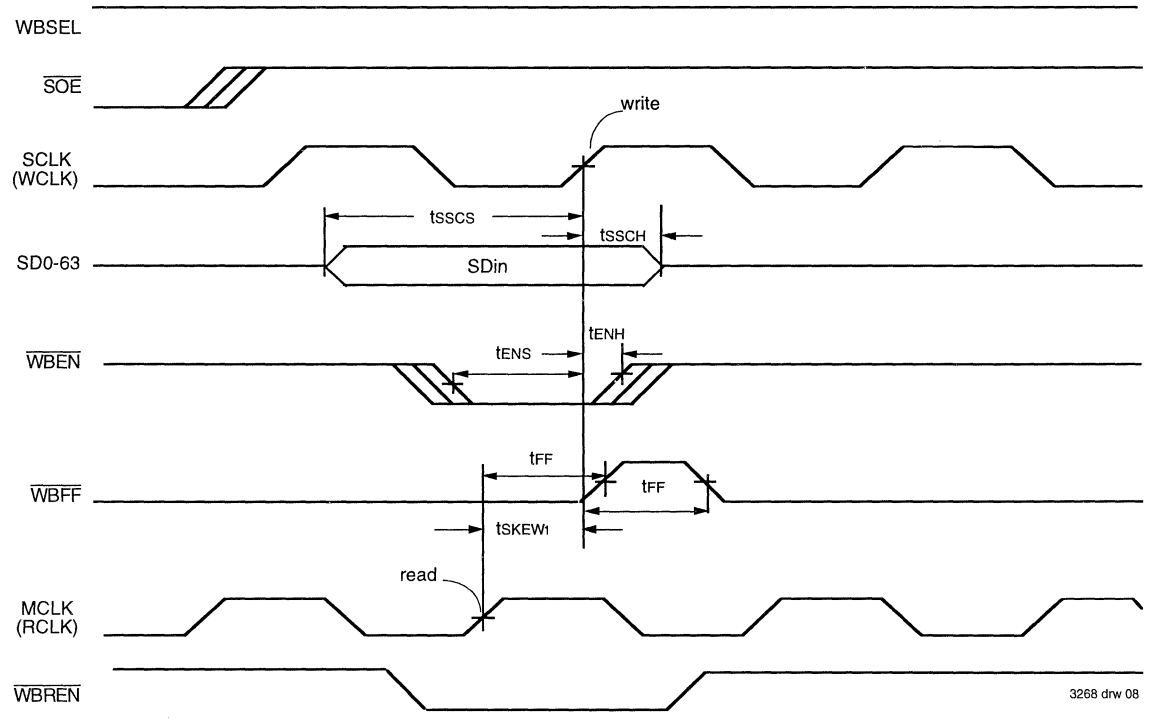


Figure 5. WFIFO Write Timing (Write Cycle)

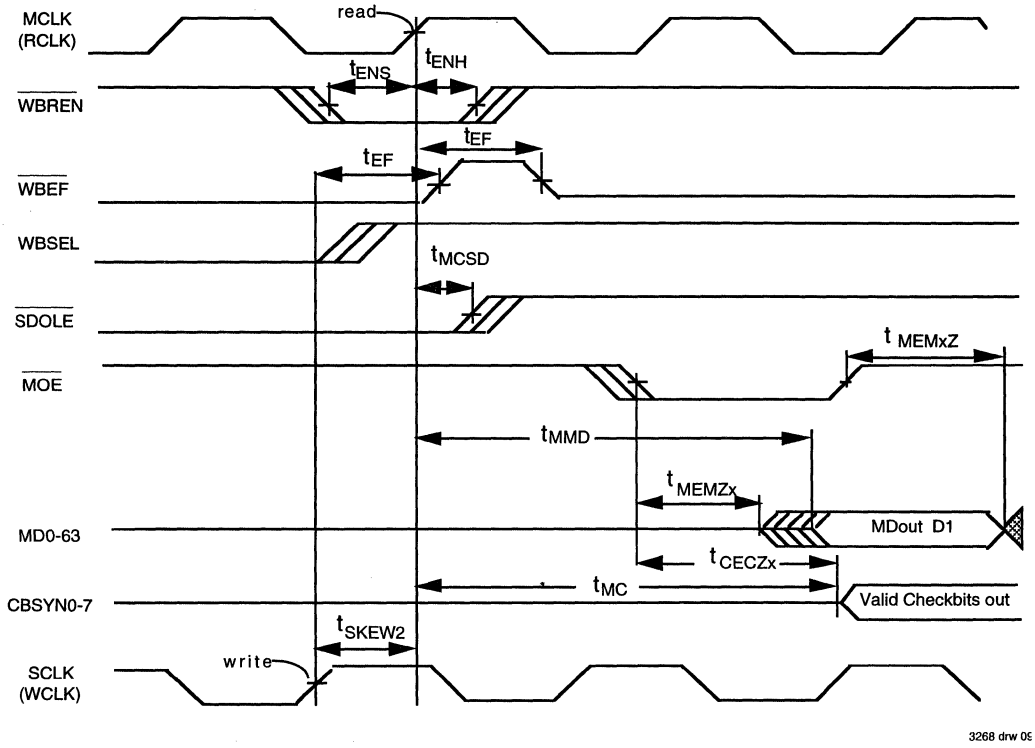


Figure 6. WFIFO Read and Checkbit Generate Timing (Write Cycle)

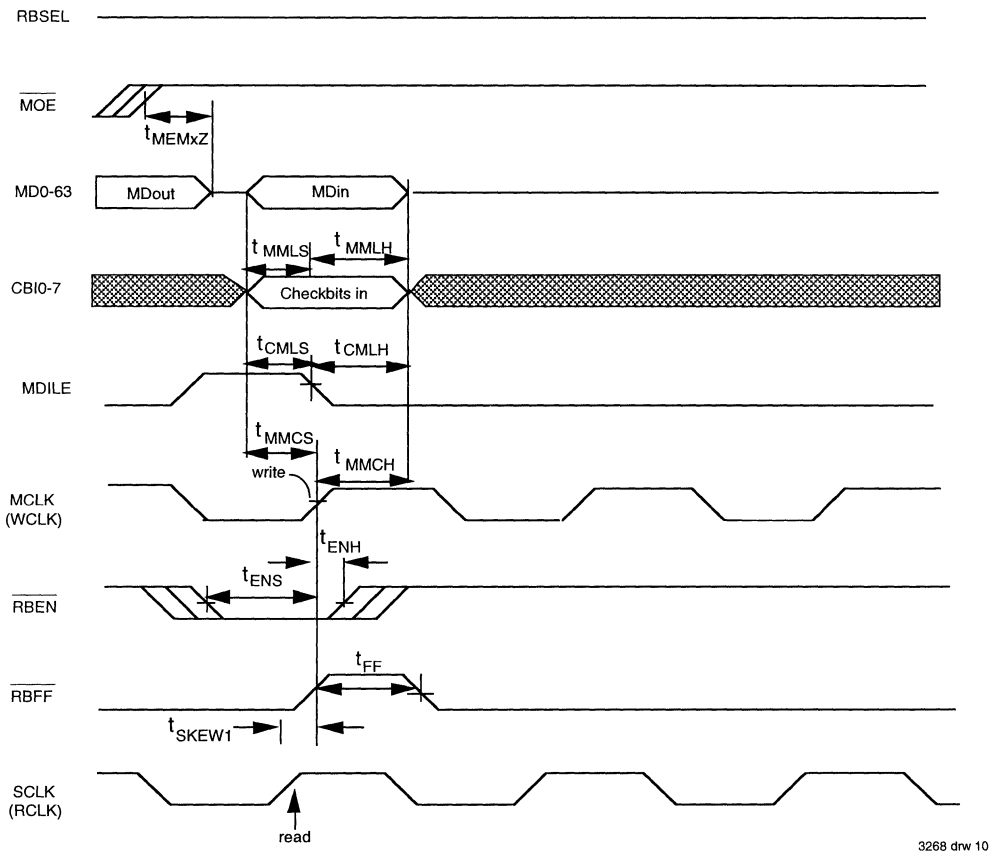


Figure 7. RFIFO Write Timing (Read Cycle)

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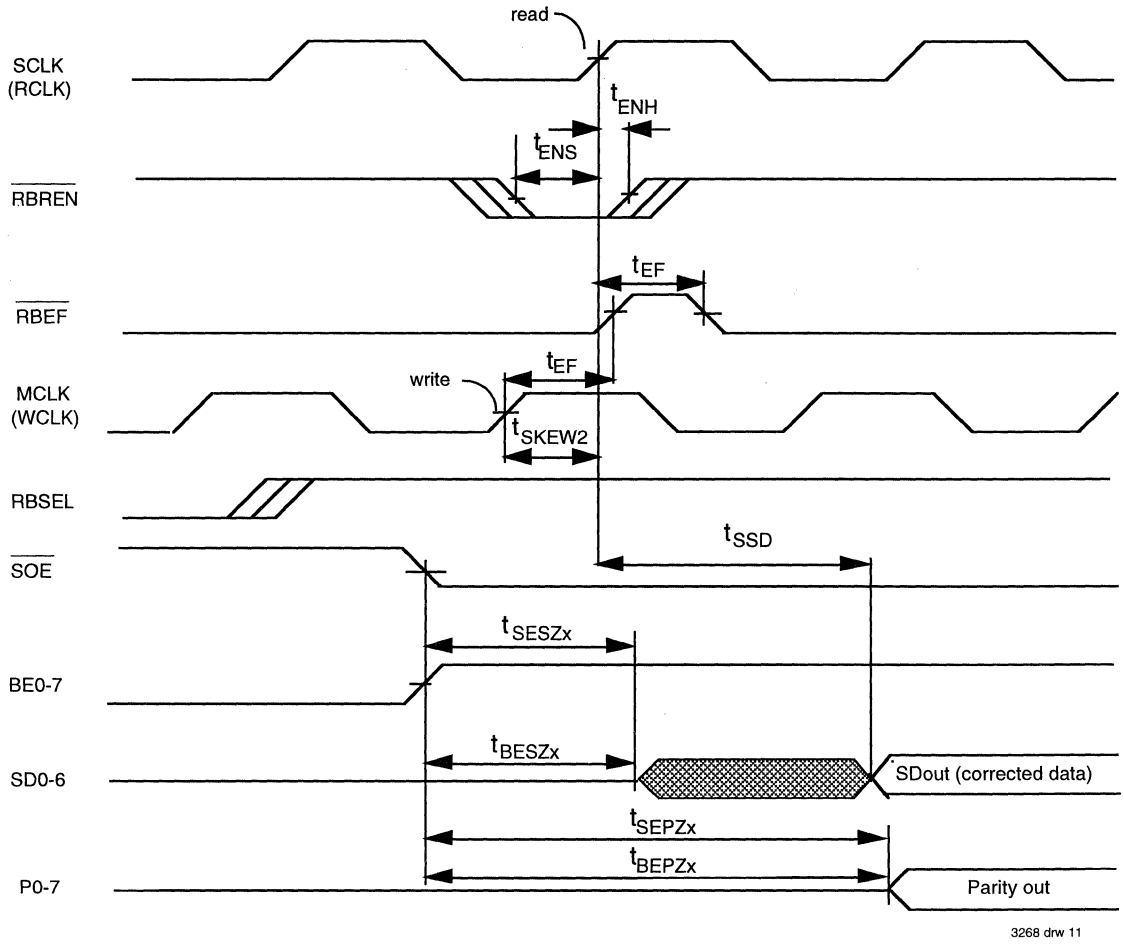

Figure 8. RFIFO Read Timing (Read Cycle)

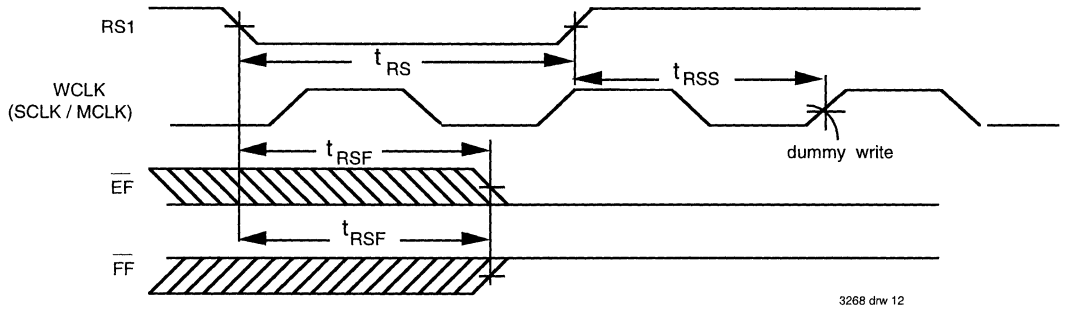

Figure 9. FIFO (WFIFO/RFIFO) Reset Timing

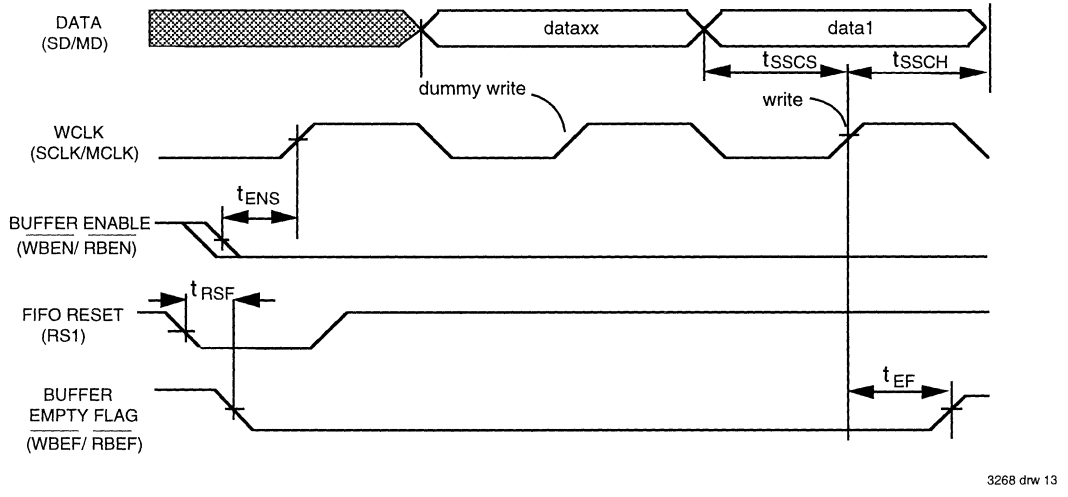

Figure 10. FIFO (WFIFO/RFIFO) Write Latency Timing

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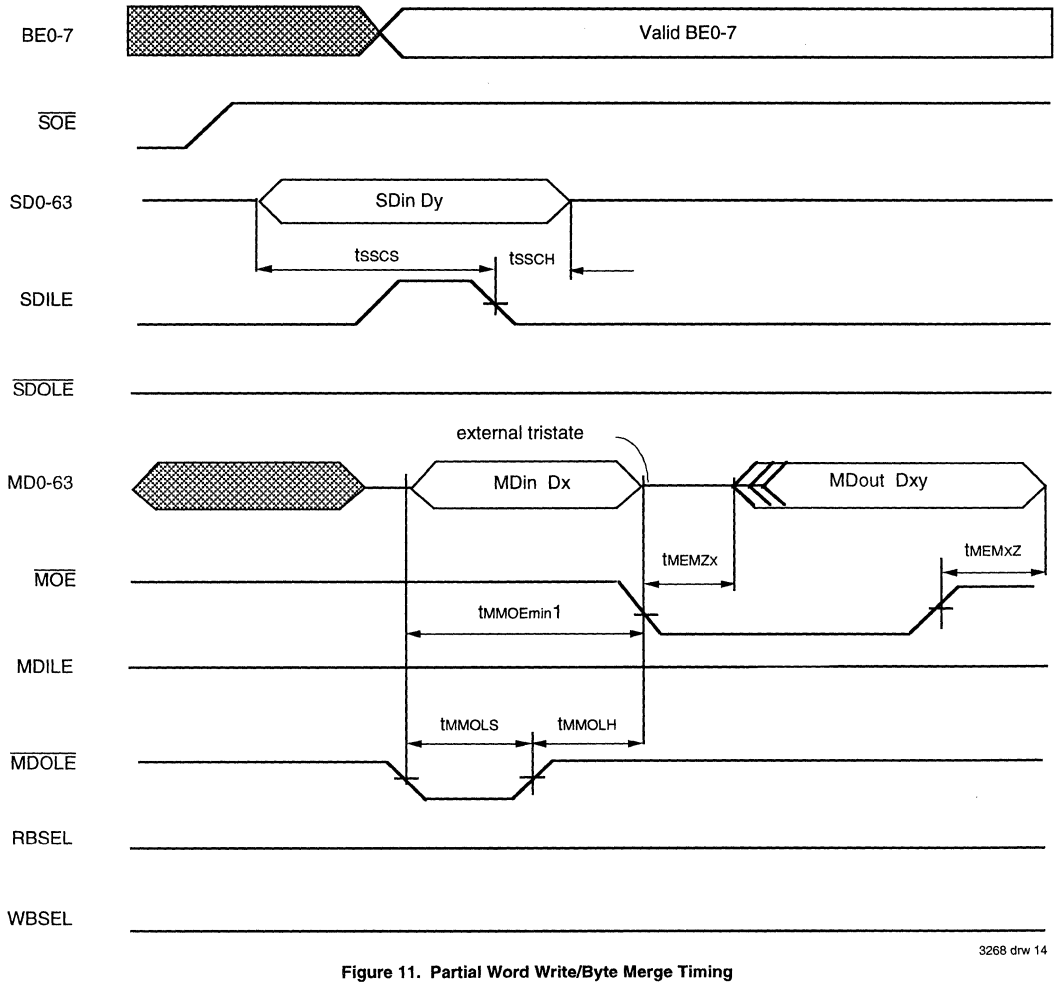

Figure 11. Partial Word Write/Byte Merge Timing

NOTE:
1. t_{MMOE} is not a propagation delay. For partial word write operations $t_{MMOE\ MIN} = t_{MDM}$.

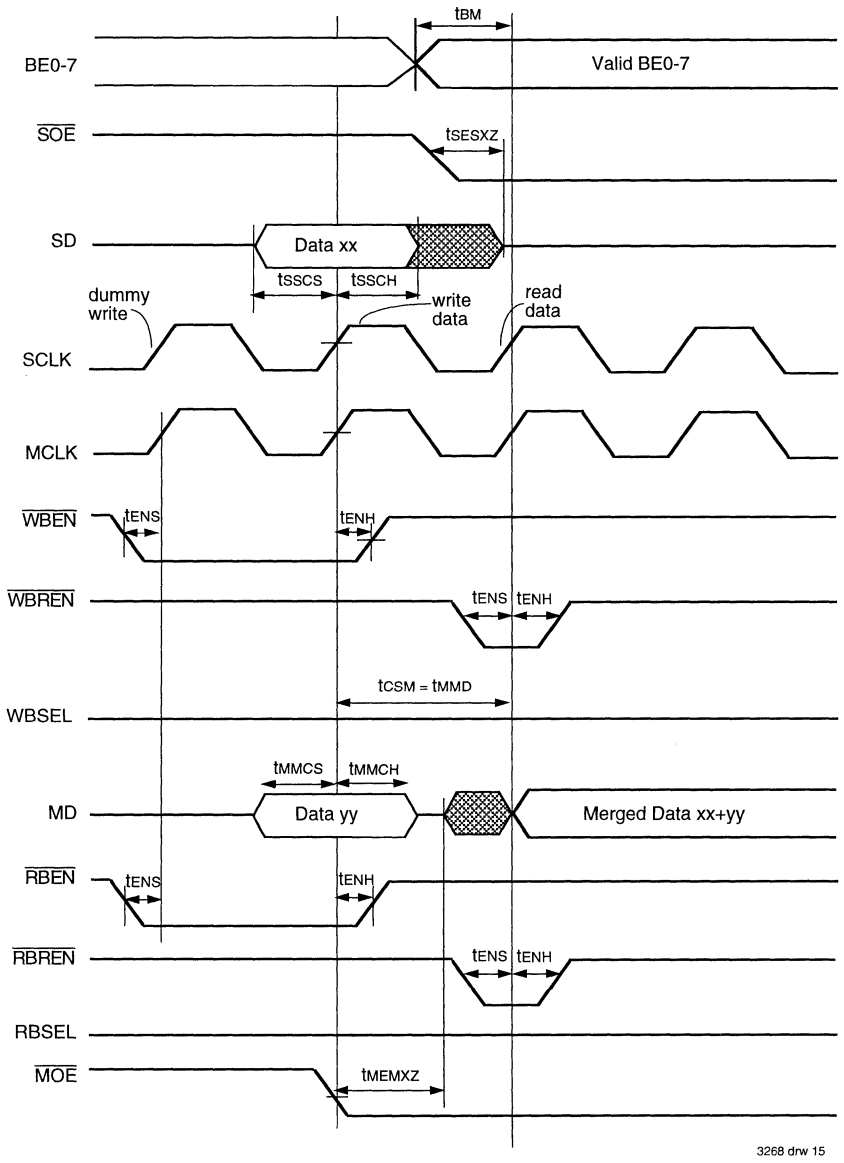

Figure 12. Partial Word Write/Byte Merge Timing using both RFIFO and WFIFO

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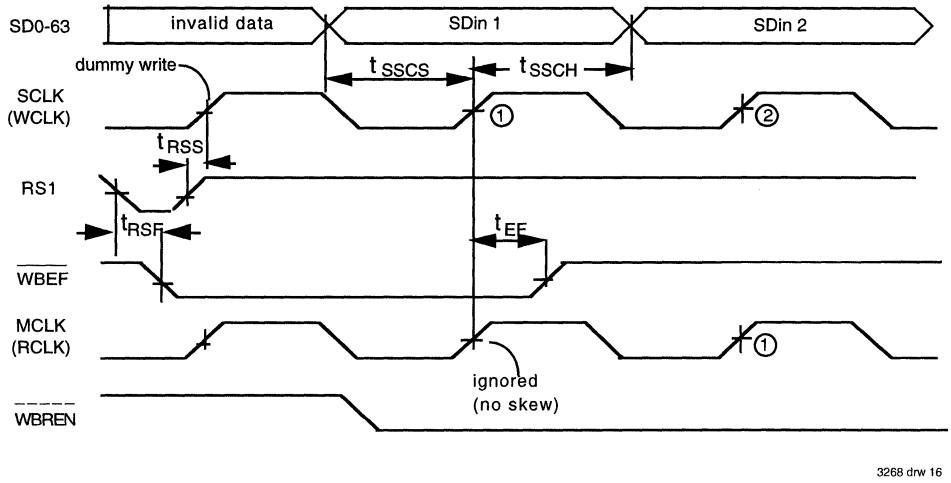


Figure 13. Write FIFO Write Timing with Clock Skew Violation

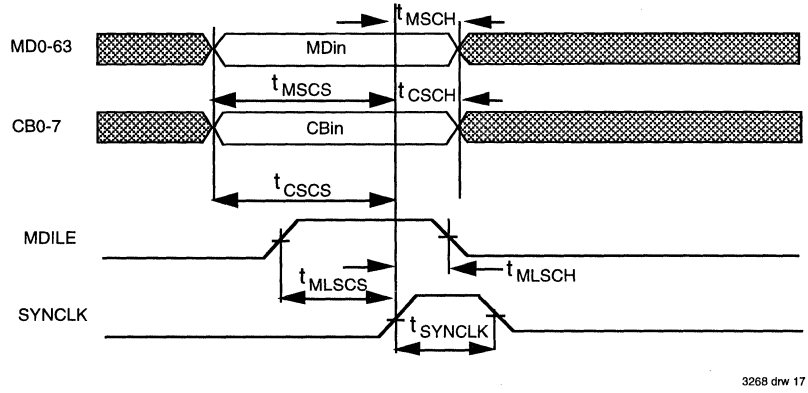
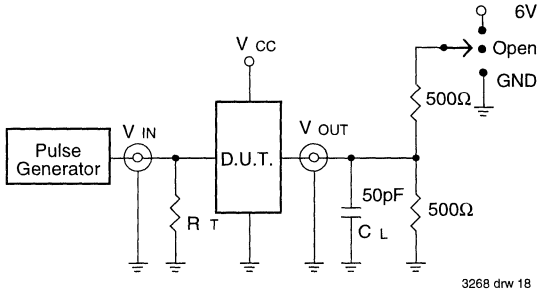


Figure 14. Diagnostic Timing

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



3268 drw 18

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

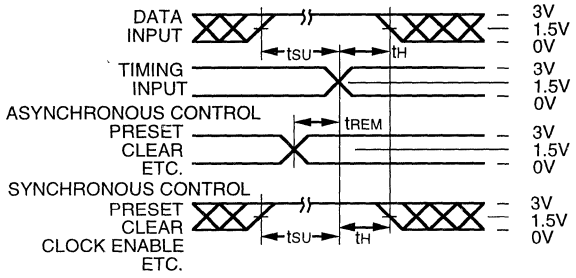
2617 tbl 20

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

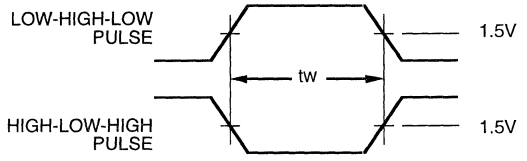
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



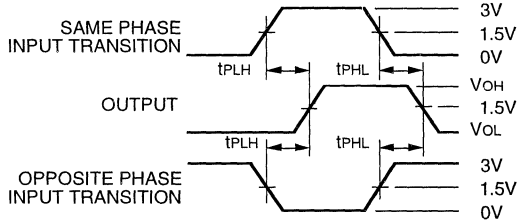
3268 drw 19

PULSE WIDTH



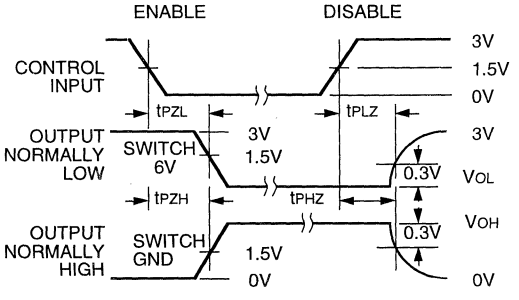
3268 drw 20

PROPAGATION DELAY



3268 drw 21

ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

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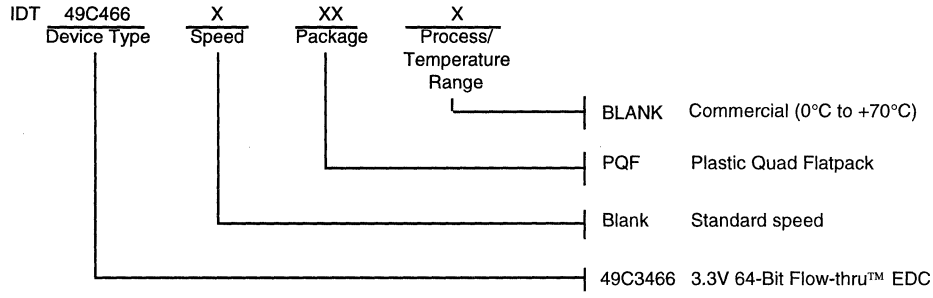
ORDERING INFORMATION



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